MS-7A06-1.0 (244mm*220mm) 4Layer

CPU:

INTEL SKYLAKE-S LGA1151
TDP:65W/35W

System Chipset:

Intel H110

VRD Power:

VRD IMVP8--NCP81203+NCP81161

Main Memory:

Dual chanels DDR4 (2133MHZ) , Max :16GB (Deep Blue)

On Board Chipset:

SIO: NCT6793D

LAN--RTL8111G Giga LAN (support PXE)

Audio: RTL ALC662-VD

Flash ROM: 8M

Expansion Slots:

PCIE3.0 x16 slot *1 (Black)

PCIE2.0 x1 slot *2 (Black)

PCI slot *1 (Black)

M.2 Card *1 (For SATA SSD) Length:2280 & 2260

REAR I/O:

VGA *1 / HDMI *1/DVI*1

USB2.0 *2 / USB3.0 *2

RJ45 *1

COM Port *1

Audio Jack 3 in 1 Jack *1

Other:

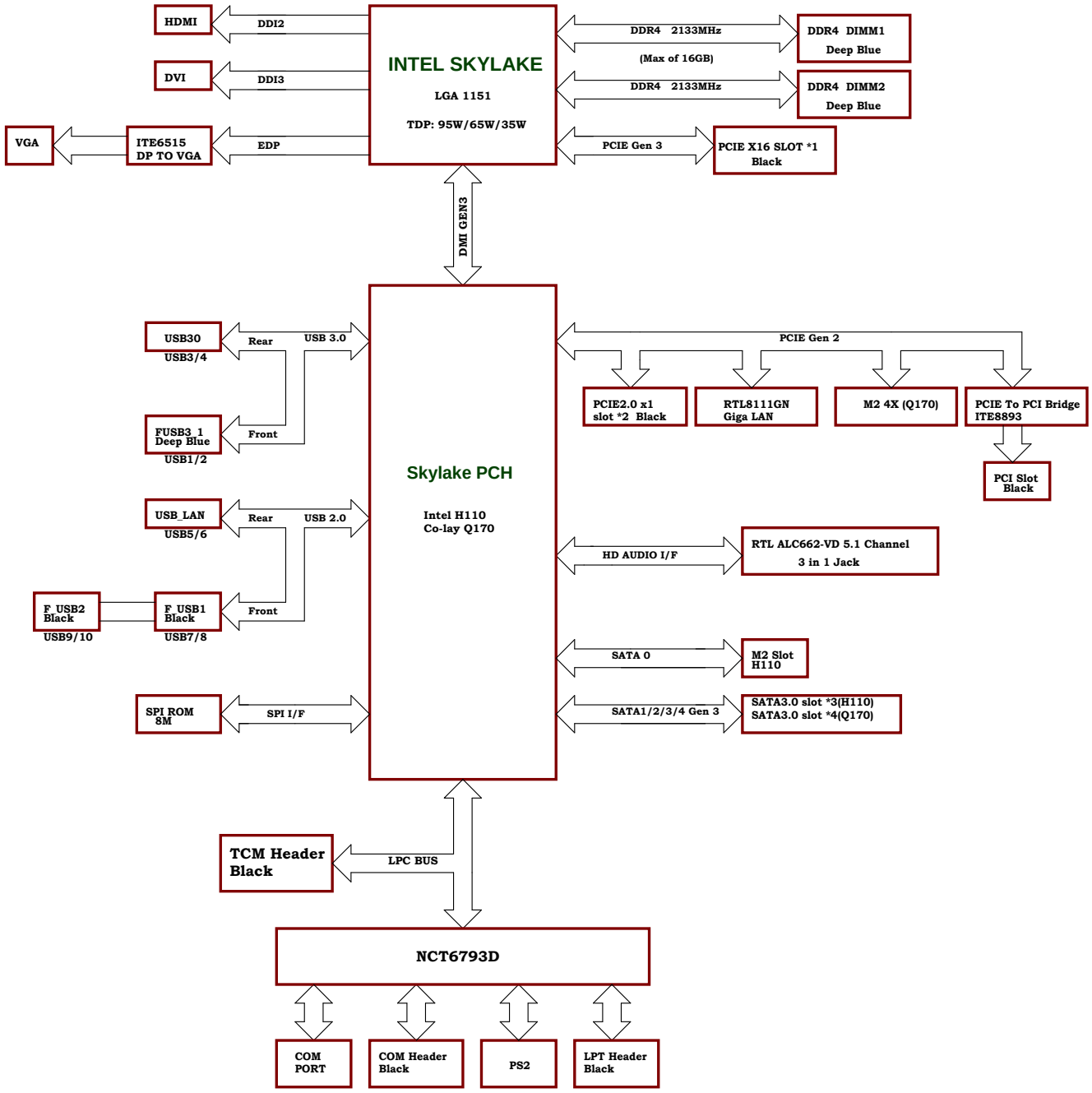
SATA3.0 *3 (Deep Blue)

Buzzer *1

ME Disable:BIOS Control

MSI MICRO-START INT'L CO.,LTD.

Title: Cover Sheet		
Size	Document Number: MS-7A06	Rev: 1.0
Date: Tuesday, December 22, 2015	Sheet 1 of 43	

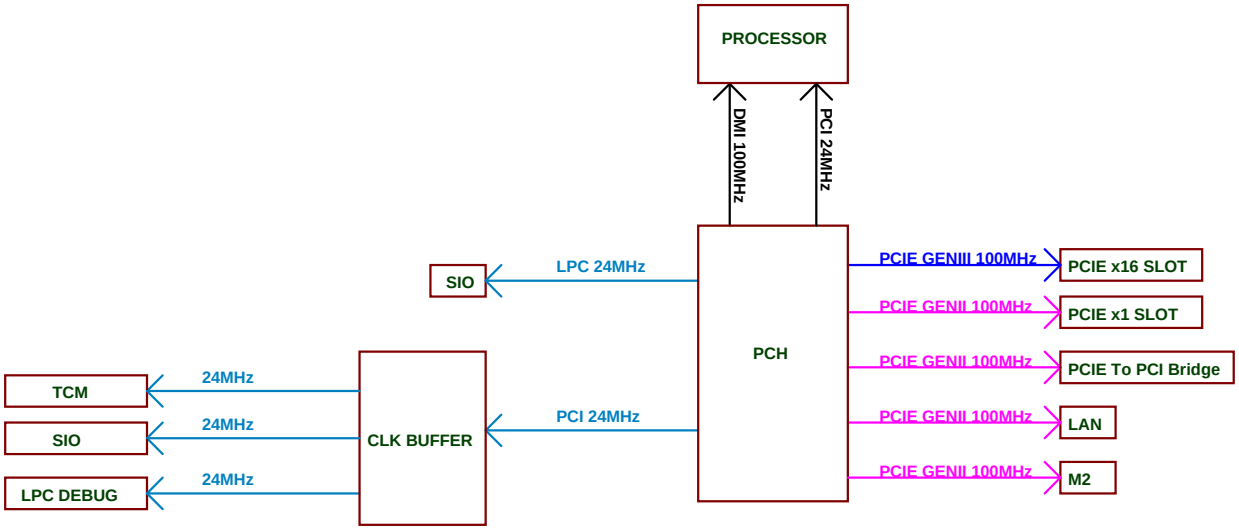


Slot Sequence:

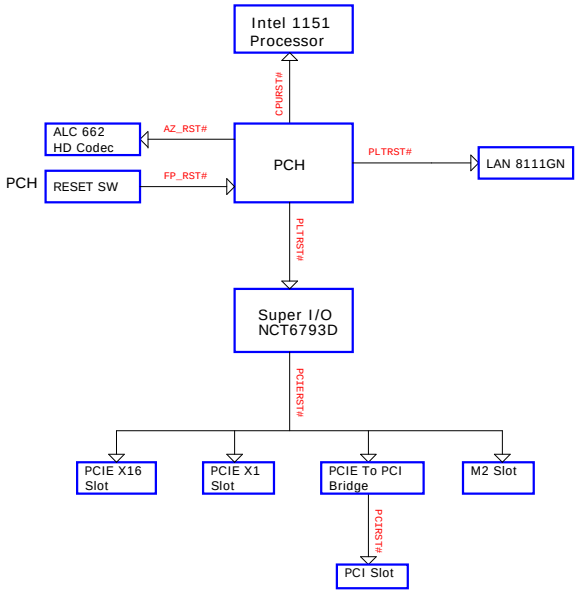
- PCIE X16
- PCIE X1
- PCIE X1
- PCI

MSI *Link to the Future* **MICRO-START INTL CO.,LTD.**

Title: *Block Diagram*		
Size	Document Number: MS-7A06	Rev: 1.0
Date: Tuesday, December 22, 2015	Sheet 2 of 43	



RESET MAP

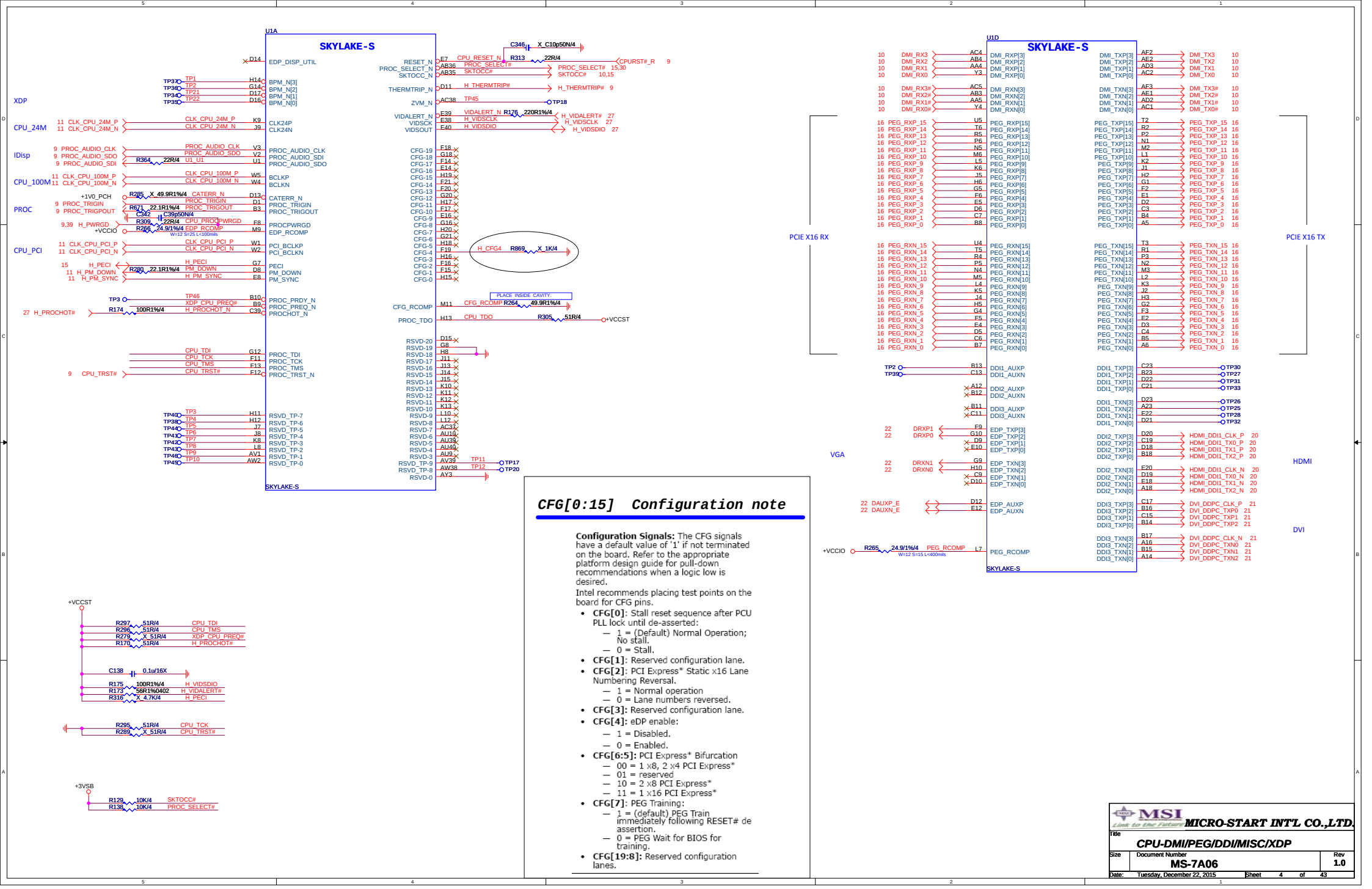


MSI MICRO-START INT'L CO.,LTD.

Title: Clock Distribution

Size | Document Number: MS-7A06 | Rev: 1.0

Date: Tuesday, December 22, 2015 | Sheet 3 of 43



CFG[0:15] Configuration note

Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

Intel recommends placing test points on the board for CFG pins.

- **CFG[0]**: Stall reset sequence after PCU PLL lock until de-asserted:
  - 1 = (Default) Normal Operation; No stall.
  - 0 = Stall.
- **CFG[1]**: Reserved configuration lane.
- **CFG[2]**: PCI Express* Static x16 Lane Numbering Reversal.
  - 1 = Normal operation
  - 0 = Lane numbers reversed.
- **CFG[3]**: Reserved configuration lane.
- **CFG[4]**: eDP enable:
  - 1 = Disabled.
  - 0 = Enabled.
- **CFG[6:5]**: PCI Express* Bifurcation
  - 00 = 1 x8, 2 x4 PCI Express*
  - 01 = reserved
  - 10 = 2 x8 PCI Express*
  - 11 = 1 x16 PCI Express*
- **CFG[7]**: PEG Training:
  - 1 = (default) PEG Train immediately following RESET# de assertion.
  - 0 = PEG Wait for BIOS for training.
- **CFG[19:8]**: Reserved configuration lanes.

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: CPU-DMI/PEG/DDI/MISC/XDP

Size	Document Number	Rev
	MS-7A06	1.0

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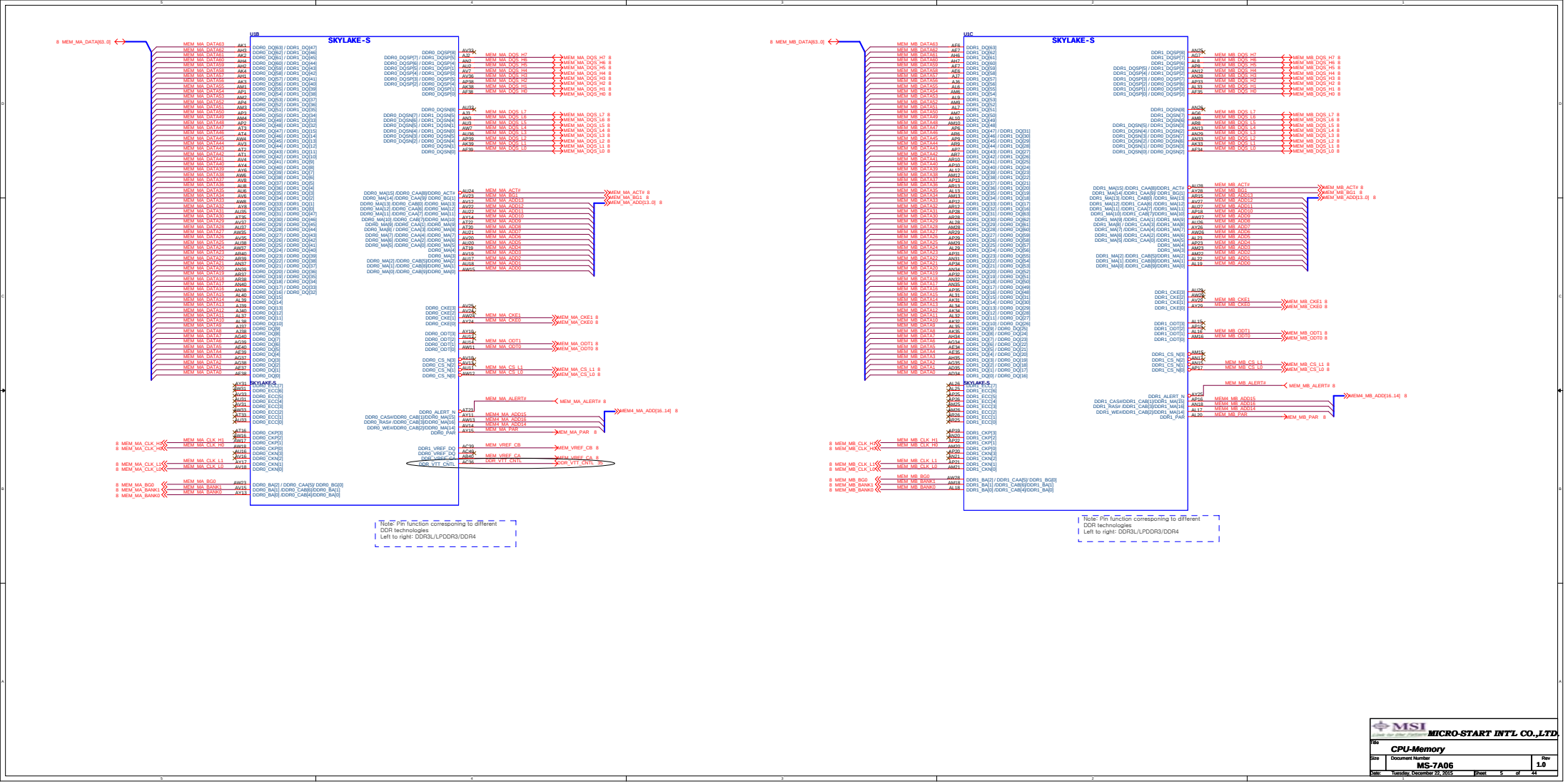
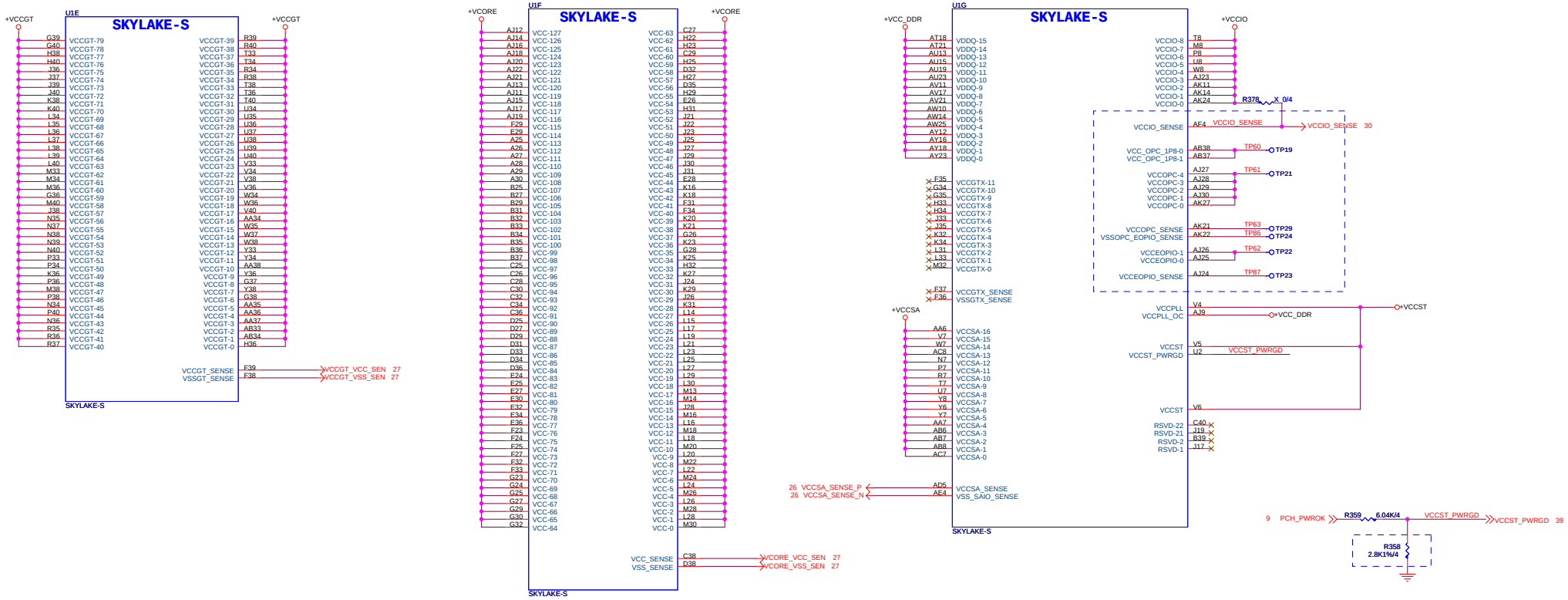


MSI MICRO-START INT'L CO.,LTD.

Title	CPU-Memory	
Size	Document Number MS-7A06	Rev 1.0
Date: Tuesday, December 22, 2015	Sheet 5 of 44	



MICRO-START INT'L CO.,LTD.

Title: CPU-Power

Size	Document Number	Rev
	MS-7A06	1.0

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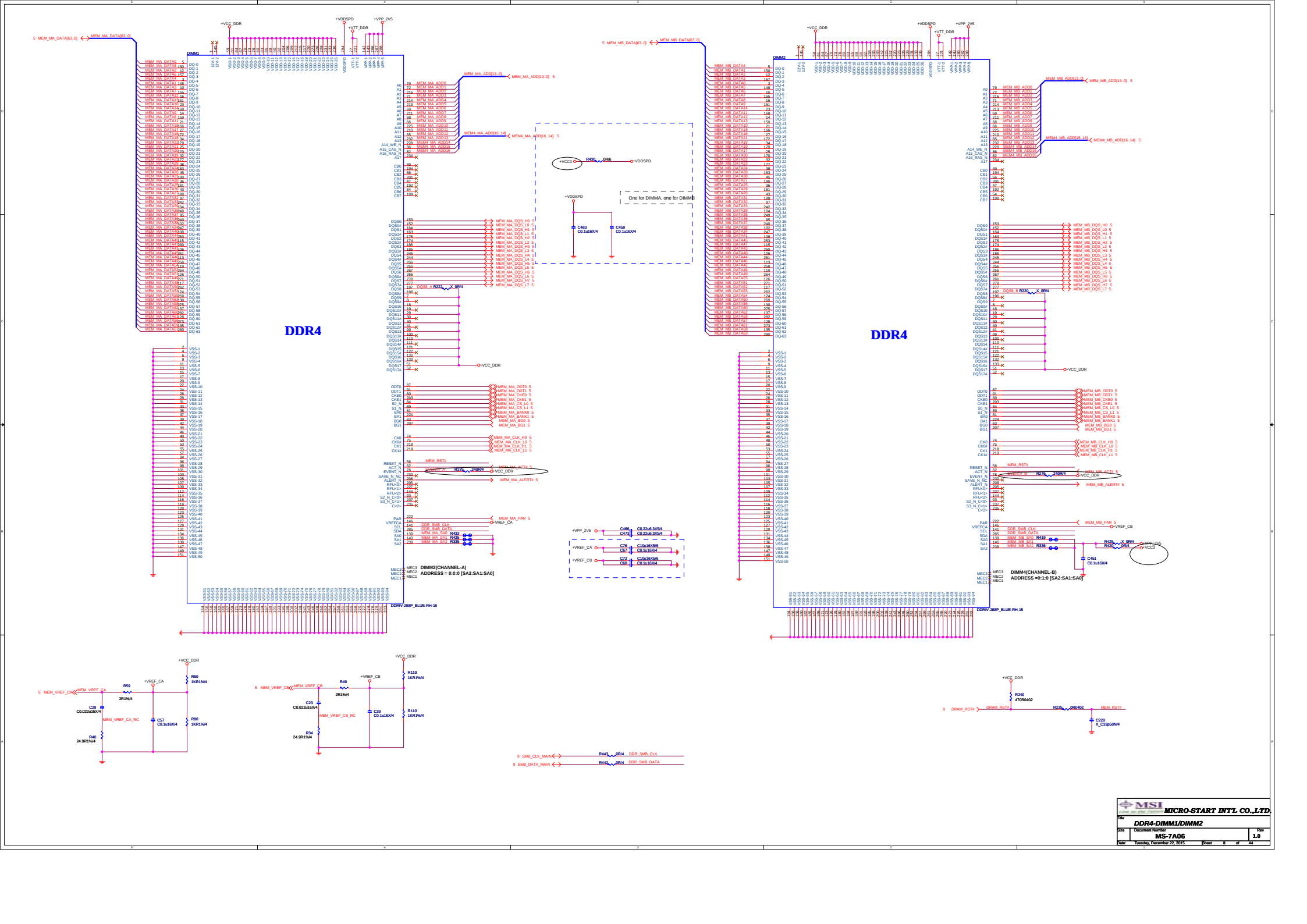
MICRO-START INT'L CO.,LTD.

Title: CPU-GND

Size	Document Number	Rev
	MS-7A06	1.0

Date: Tuesday, December 22, 2015 Sheet 7 of 43


DDR4
DIMM1
DIMM2(CHANNEL-A)
ADDRESS = 0:0:0 [SA2:SA1:SA0]
DIMM4(CHANNEL-B)
ADDRESS =0:1:0 [SA2:SA1:SA0]
One for DIMMA, one for DIMMB
DDR4
DDRIV-288P_BLUE-RH-15
MICRO-START INT'L CO.,LTD.
DDR4-DIMM1/DIMM2
MS-7A06
1.0
Tuesday, December 22, 2015

SPI1 should be used for touch operation interface

U2A

SKYLAKE PCH-H

U2D

SKYLAKE PCH-H

PROC

IDisp

Case Open

	R181	R180	R879
DSW	V	X	X
EUP	X	V	V

DPWROK Generation Schematic

RSMRST# Add 47K to GND to reduce leakage from coin cell battery in G3.

PCH_STRAP

ME_DIS	Intel ME
High	Enable
Low	Disable

ME_DIS

ME Jumper

Unstuff	Normal
1 - 2	BIOS ME(Default)
2 - 3	HW ME

MICRO-STAR INT'L CO.,LTD

Title: PCH-PME/SMBUS/UART/I2C/HDA

Size: | Document Number: MS-7A06 | Rev: 1.0

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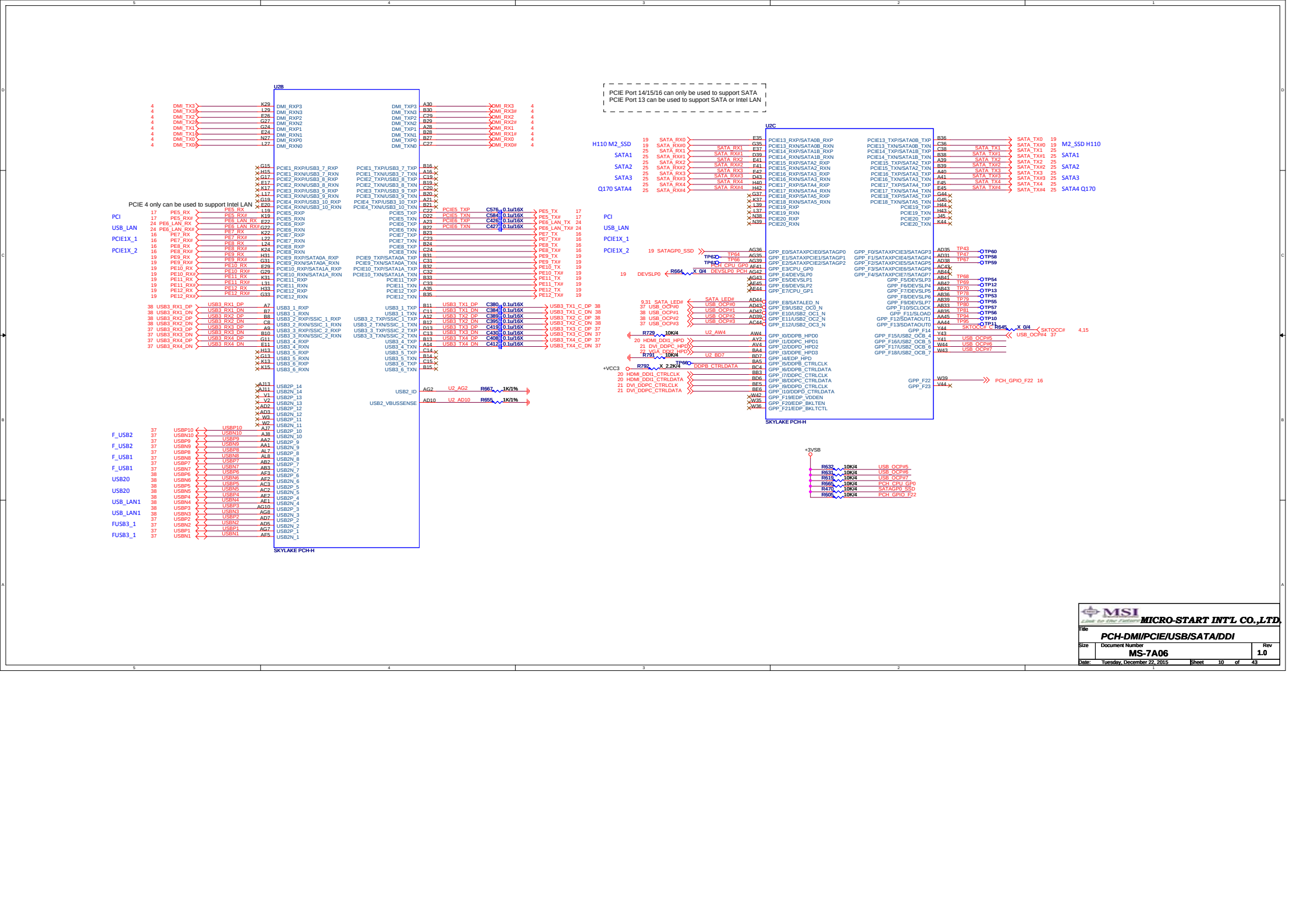
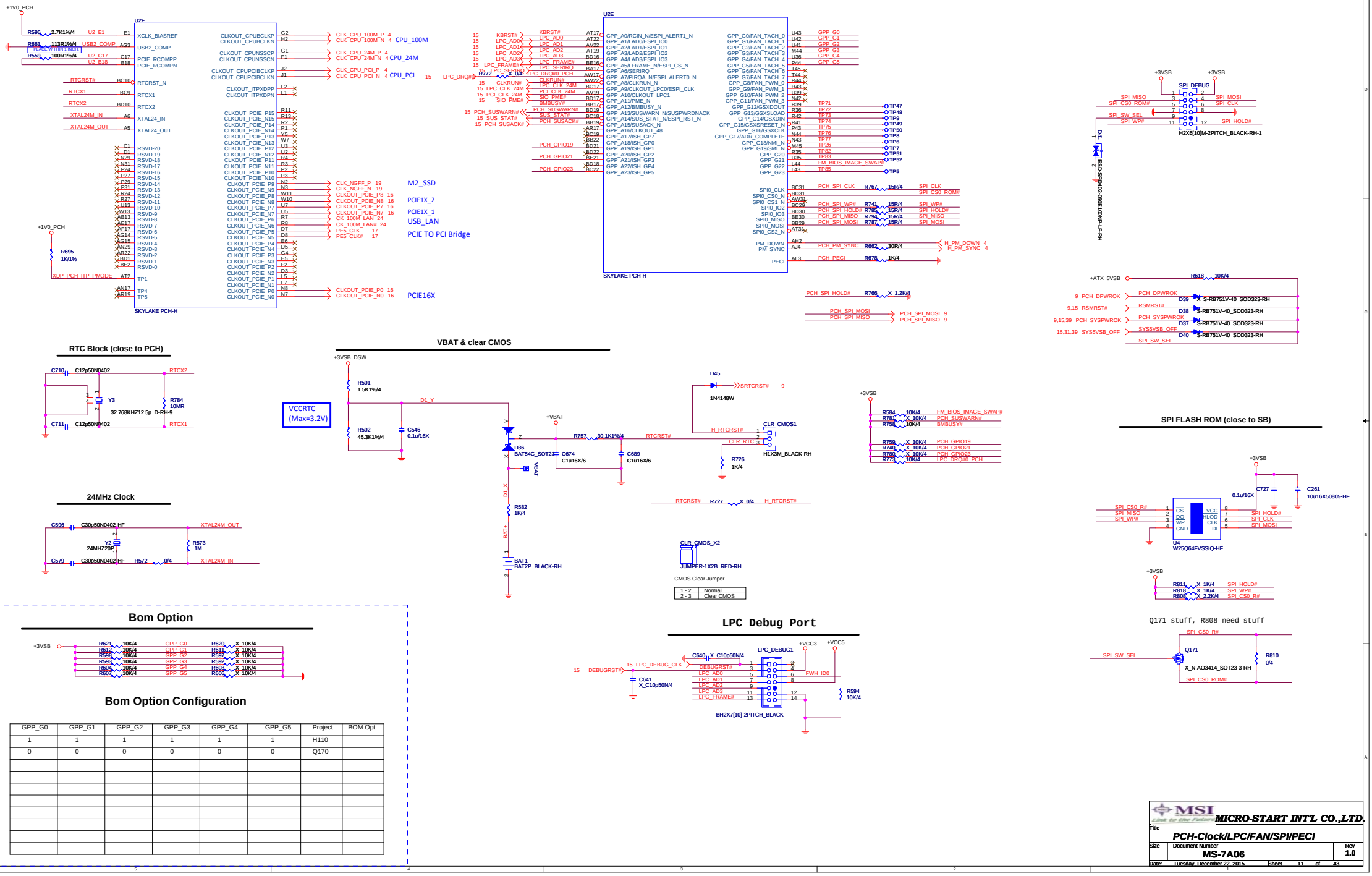
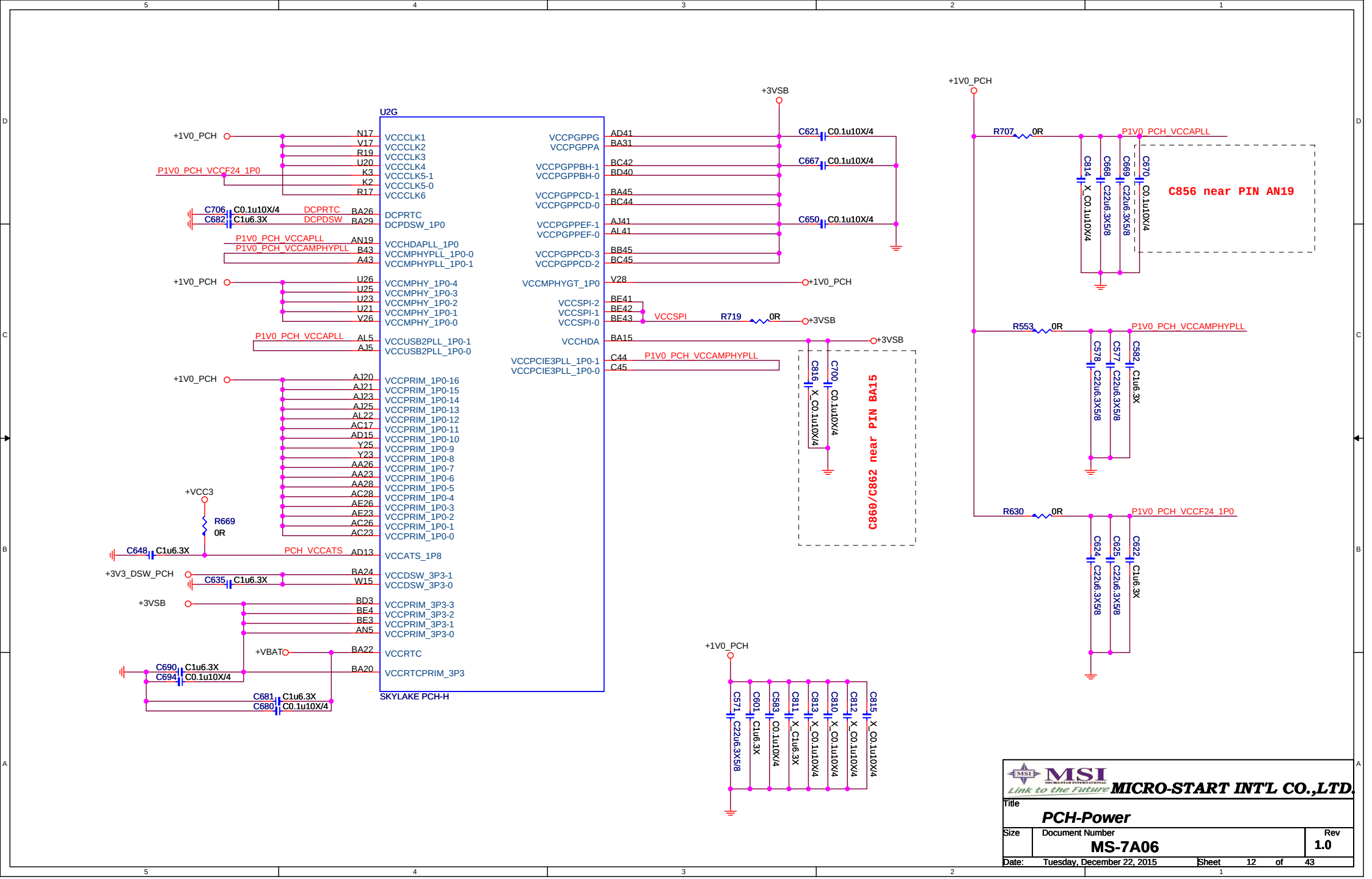

U2B
SKYLAKE PCH-H
PCIE Port 14/15/16 can only be used to support SATA
PCIE Port 13 can be used to support SATA or Intel LAN
PCIE 4 only can be used to support Intel LAN
U2C
SKYLAKE PCH-H
+3VSB
MSI
MICRO-START INT'L CO.,LTD.
Title
PCH-DMI/PCIE/USB/SATA/DDI
Size
Document Number
MS-7A06
Rev
1.0
Date: Tuesday, December 22, 2015
Sheet 10 of 43



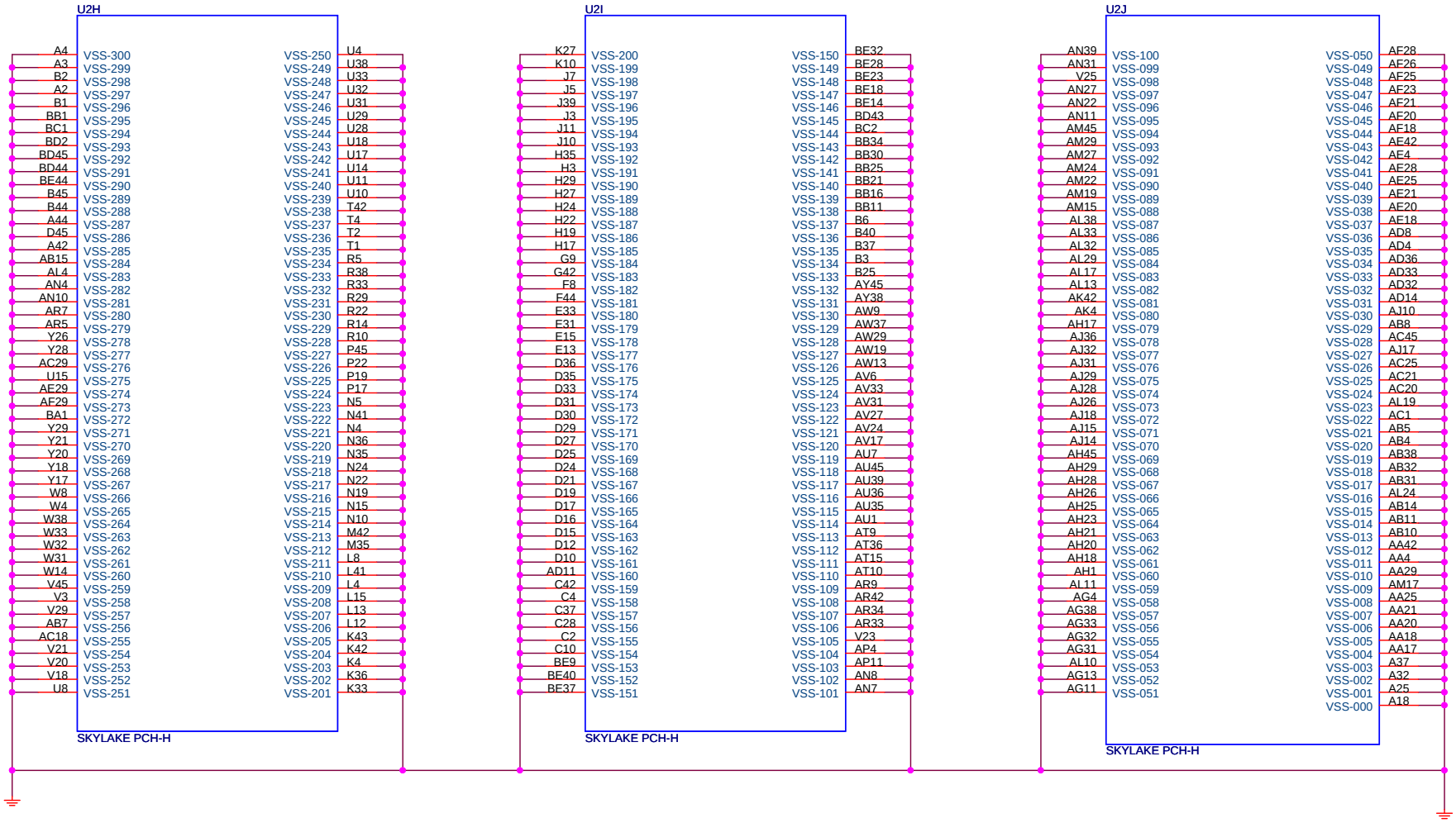
GPP_G0	GPP_G1	GPP_G2	GPP_G3	GPP_G4	GPP_G5	Project	BOM Opt
1	1	1	1	1	1	H110	
0	0	0	0	0	0	Q170	



MICRO-START INT'L CO.,LTD.

Link to the Future

Title: PCH-Power		
Size	Document Number: MS-7A06	Rev: 1.0
Date: Tuesday, December 22, 2015	Sheet 12 of 43	



MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: PCH-GND

Size	Document Number	Rev
	MS-7A06	1.0

Date: Tuesday, December 22, 2015 Sheet 13 of 43

Table 9-1. Functional Strap Definitions (Sheet 1 of 3)

Signal	Usage	When Sampled	Comment
SPKR / GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC). ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GSPI0_MOSI / GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Configuration Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the primary well.
SMBALERT# / GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI / GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap. **Bit 10** — **Boot BIOS Destination** 0 — SPI 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination Select to LPC by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT# / GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** Is selected for EC. 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
HDA_SDO	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.
DDPB_CTRLDATA / GPP_I6	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. 1 = Port B is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA / GPP_I8	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port C is not detected. 1 = Port C is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.

Table 9-1. Functional Strap Definitions (Sheet 3 of 3)

Signal	Usage	When Sampled	Comment
DDPD_CTRLDATA / GPP_I10	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.

Title: Strap			
Size: Custom	Document Number: MS-7A06		Rev: 1.0
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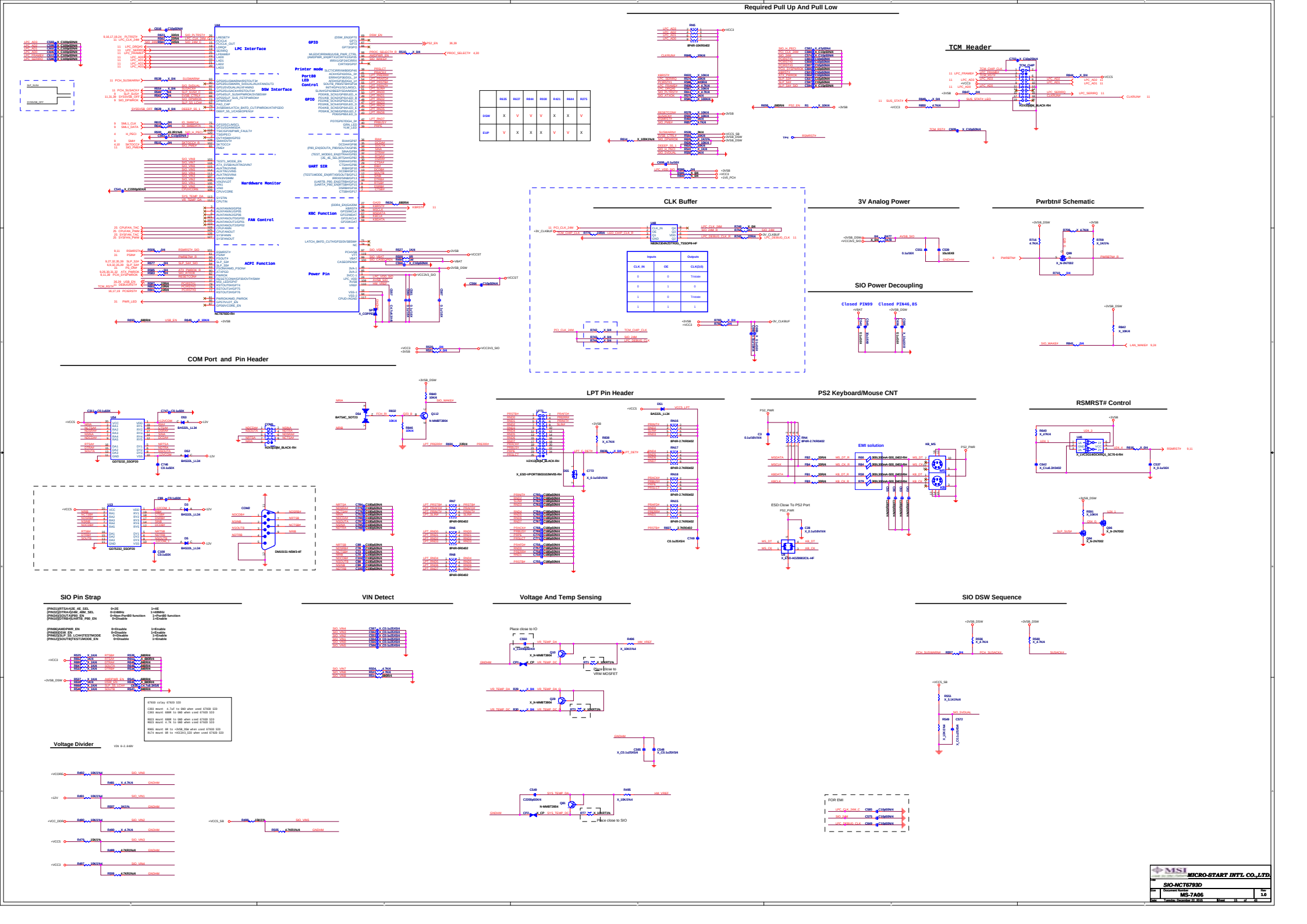
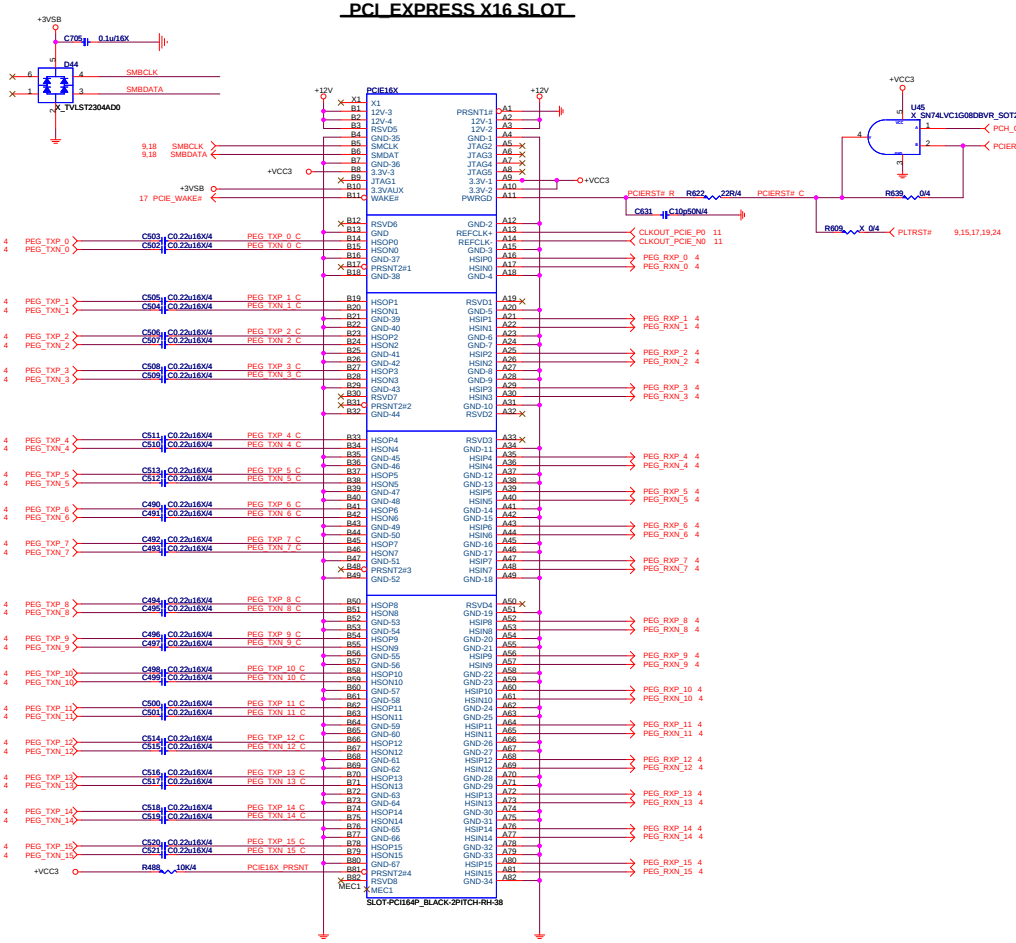
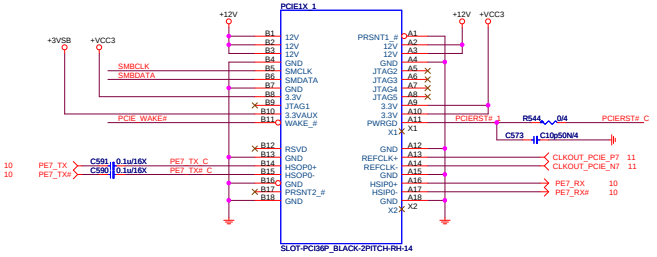

Required Pull Up And Pull Low
TCM Header
CLK Buffer
3V Analog Power
Pwrbtn# Schematic
SIO Power Decoupling
COM Port and Pin Header
LPT Pin Header
PS2 Keyboard/Mouse CNT
RSMRST# Control
SIO Pin Strap
VIN Detect
Voltage And Temp Sensing
SIO DSW Sequence
Voltage Divider
LPC Interface
FDW Interface
Hardware Monitor
FAN Control
ACPI Function
GPIO
Printer mode
Port80
LED
Control
KBC Function
UART SIR
Power Pin
EMI solution
ESD Close To PS2 Port
Closed PIN99
Closed PIN46,85
MICRO-START INTL CO.,LTD.
SIO-NCT6793D
MS-7A06
1.0
Tuesday, December 29, 2015

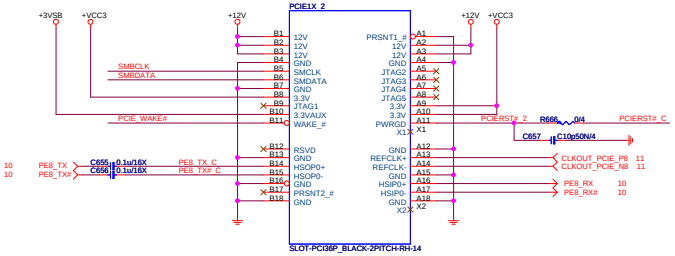
PCI_EXPRESS X16 SLOT

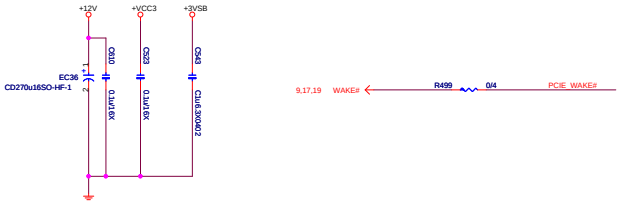


PCI_EXPRESS x1-PORT



PCI_EXPRESS x1-PORT





MSI Lead for the Future	MICRO-START INTL CO.,LTD.		
Title	PCIE x16/x1 slot		
Size	Document Number MS-7A06		Rev 1.0
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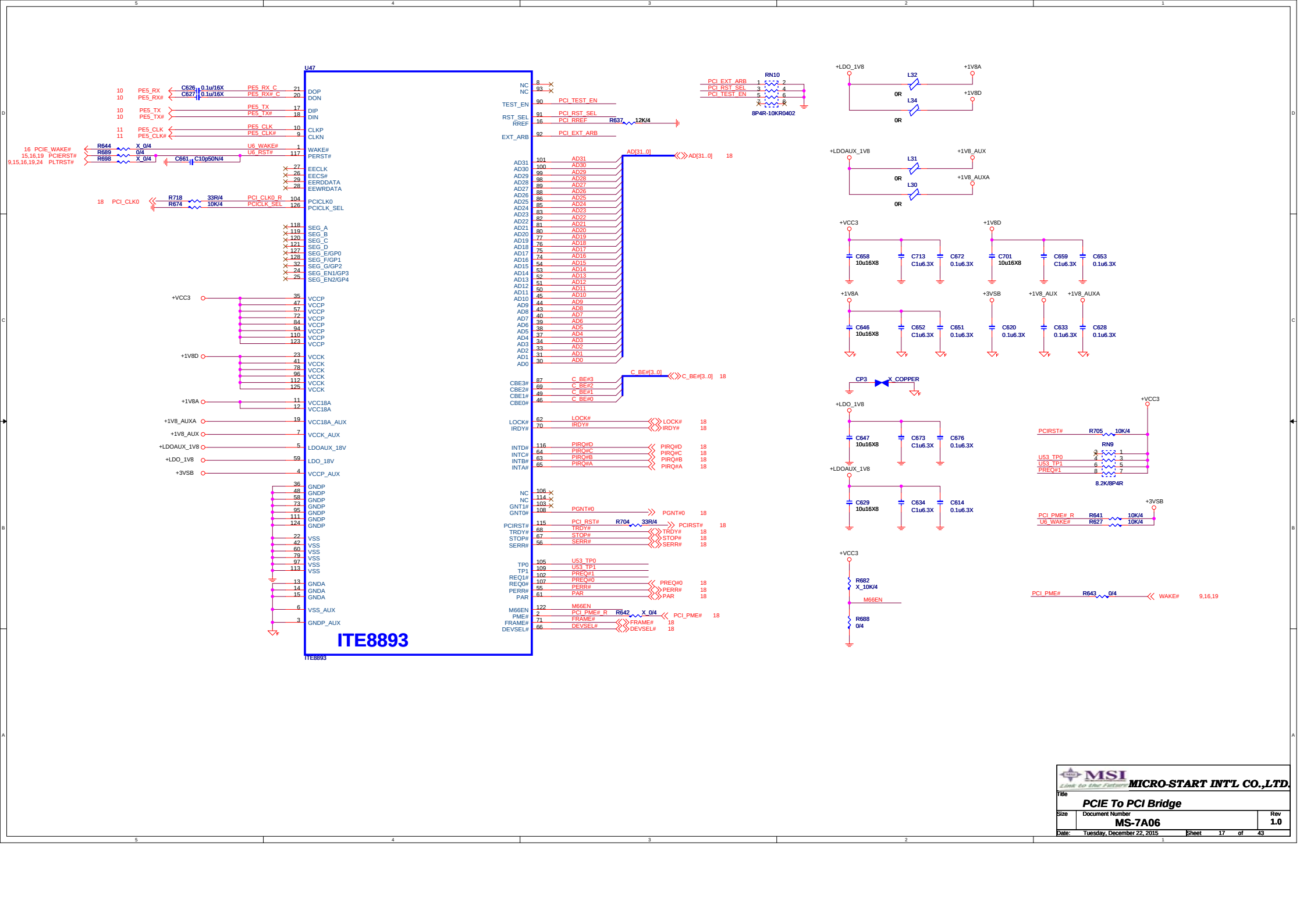
U47
ITE8893
PE5_RX
PE5_RX#
PE5_TX
PE5_TX#
PE5_CLK
PE5_CLK#
C626 0.1u/16X
C627 0.1u/16X
PE5_RX_C
PE5_RX# C
PE5_TX
PE5_TX#
PE5_CLK
PE5_CLK#
DOP
DON
DIP
DIN
CLKP
CLKN
16 PCIE_WAKE#
15,16,19 PCIERST#
9,15,16,19,24 PLTRST#
R644 X_0/4
R689 0/4
R698 X_0/4
C661 C10p50N/4
U6_WAKE#
U6_RST#
WAKE#
PERST#
EECLK
EECS#
EERDDATA
EEWRDATA
18 PCI_CLK0
R718 33R/4
R674 10K/4
PCI_CLK0_R
PCICLK_SEL
PCICLK0
PCICLK_SEL
SEG_A
SEG_B
SEG_C
SEG_D
SEG_E/GP0
SEG_F/GP1
SEG_G/GP2
SEG_EN1/GP3
SEG_EN2/GP4
+VCC3
VCCP
+1V8D
VCCK
+1V8A
VCC18A
+1V8_AUXA
VCC18A_AUX
+1V8_AUX
VCCK_AUX
+LDOAUX_1V8
LDOAUX_18V
+LDO_1V8
LDO_18V
+3VSB
VCCP_AUX
GNDP
VSS
GNDA
VSS_AUX
GNDP_AUX
NC
TEST_EN
PCI_TEST_EN
RST_SEL
RREF
PCI_RST_SEL
PCI_RREF
R637 12K/4
EXT_ARB
PCI_EXT_ARB
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
AD[31..0]
CBE3#
CBE2#
CBE1#
CBE0#
C_BE#3
C_BE#2
C_BE#1
C_BE#0
C_BE#[3..0]
LOCK#
IRDY#
INTD#
INTC#
INTB#
INTA#
PIRQ#D
PIRQ#C
PIRQ#B
PIRQ#A
GNT1#
GNT0#
PGNT#0
PCIRST#
TRDY#
STOP#
SERR#
PCI_RST#
R704 33R/4
TP0
TP1
REQ1#
REQ0#
PERR#
PAR
U53_TP0
U53_TP1
PREQ#1
PREQ#0
M66EN
PME#
FRAME#
DEVSEL#
PCI_PME#_R
R642 X_0/4
PCI_PME#
RN10
PCI_RST_SEL
PCI_TEST_EN
8P4R-10KR0402
+LDO_1V8
+1V8A
+1V8D
L32
L34
0R
+LDOAUX_1V8
+1V8_AUX
+1V8_AUXA
L31
L30
C658 10u16X8
C713 C1u6.3X
C672 0.1u6.3X
C701 10u16X8
C659 C1u6.3X
C653 0.1u6.3X
C646 10u16X8
C652 C1u6.3X
C651 0.1u6.3X
C620 0.1u6.3X
C633 0.1u6.3X
C628 0.1u6.3X
CP3 X_COPPER
C647 10u16X8
C673 C1u6.3X
C676 0.1u6.3X
C629 10u16X8
C634 C1u6.3X
C614 0.1u6.3X
PCIRST#
R705 10K/4
RN9
8.2K/8P4R
U53_TP0
U53_TP1
PREQ#1
PCI_PME#_R
R641 10K/4
U6_WAKE#
R627 10K/4
R682 X_10K/4
M66EN
R688 0/4
PCI_PME#
R643 0/4
WAKE#
9,16,19
MSI
MICRO-START INT'L CO.,LTD.
Title
PCIE To PCI Bridge
Size
Document Number
MS-7A06
Rev
1.0
Date: Tuesday, December 22, 2015
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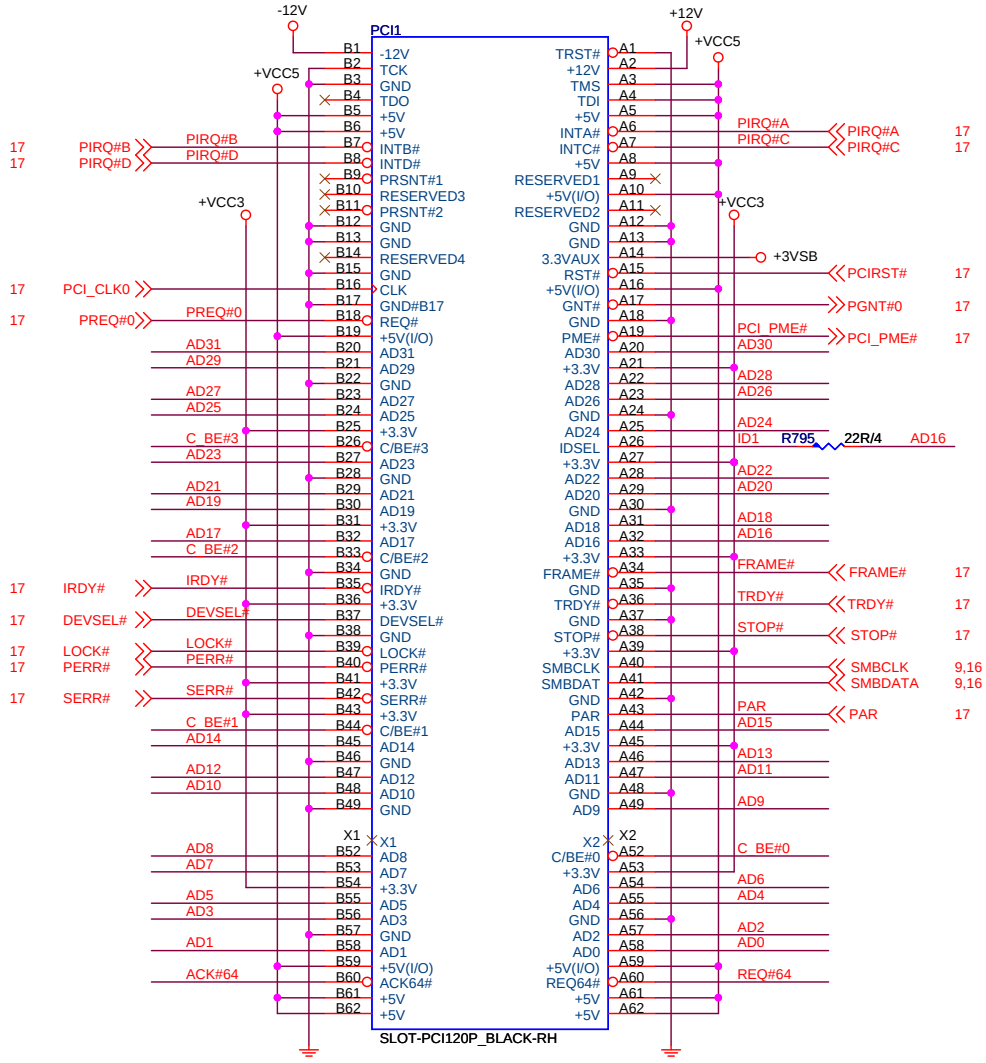
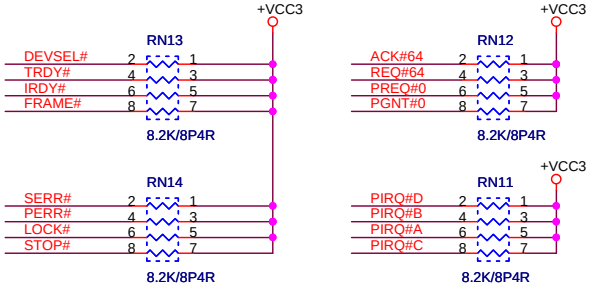


AD[31..0] AD[31..0] 17

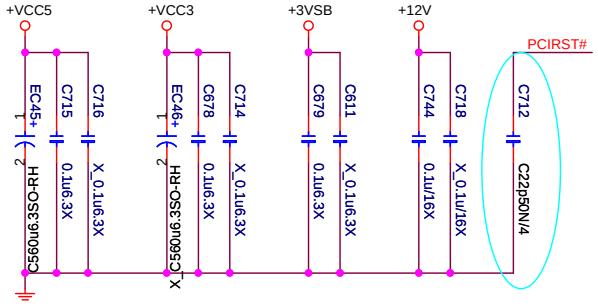
C_BE#[3..0] C_BE#[3..0] 17

IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI PULL-UP / DOWN RESISTORS

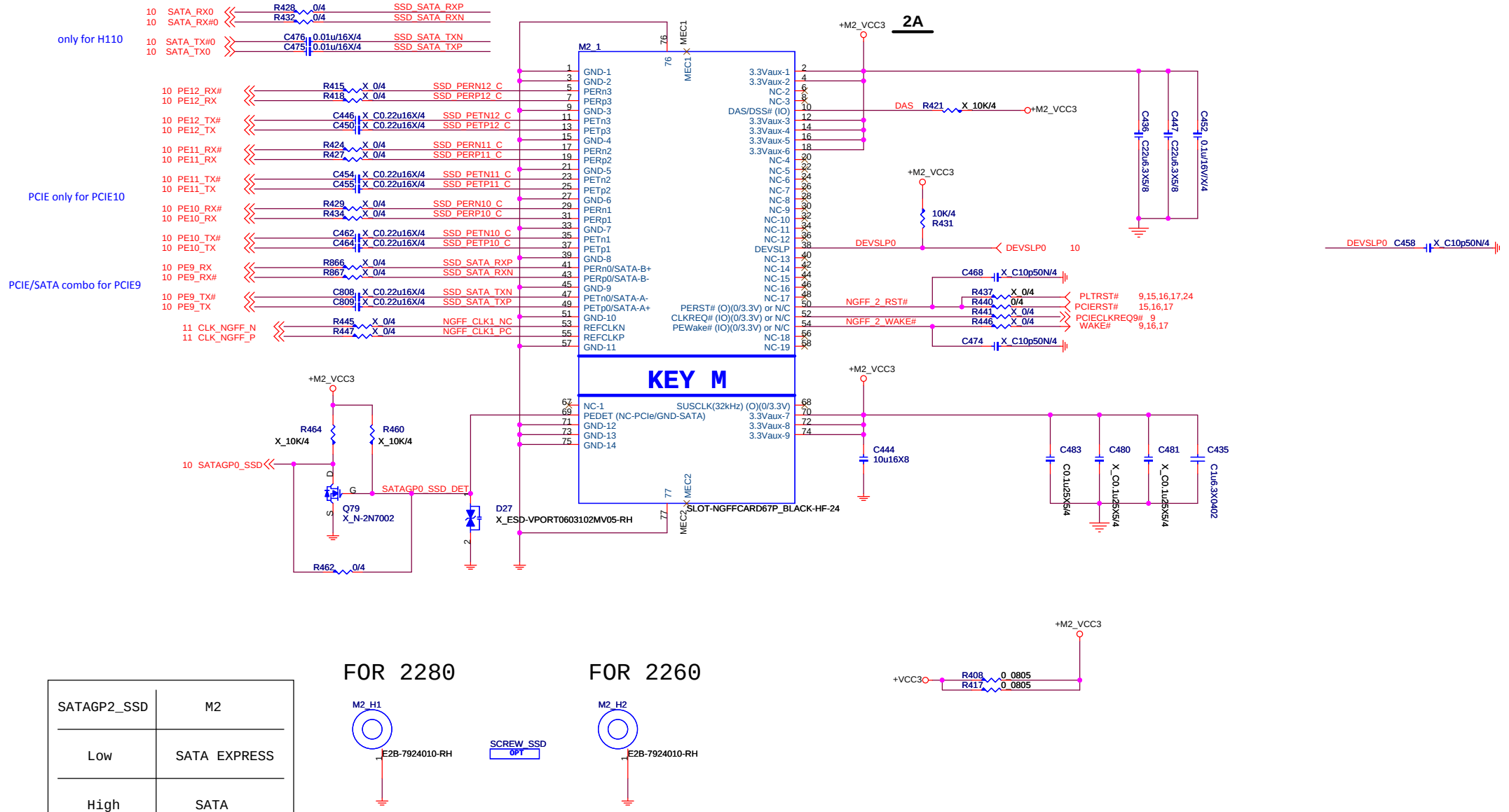


PCI slot		
+3VSB	(wake)	- 375mA
+3VSB	(no wake)	- 20mA
+3.3V		- 7.6A
+5V		- 5A
+12V		- 0.5A



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	PCI Slot		
Size	Document Number MS-7A06		Rev 1.0
Date: Tuesday, December 22, 2015	Sheet 18 of 43		

M2 slot for SSD



SATAGP2_SSD	M2
Low	SATA EXPRESS
High	SATA

MICRO-STAR INT'L CO.,LTD.

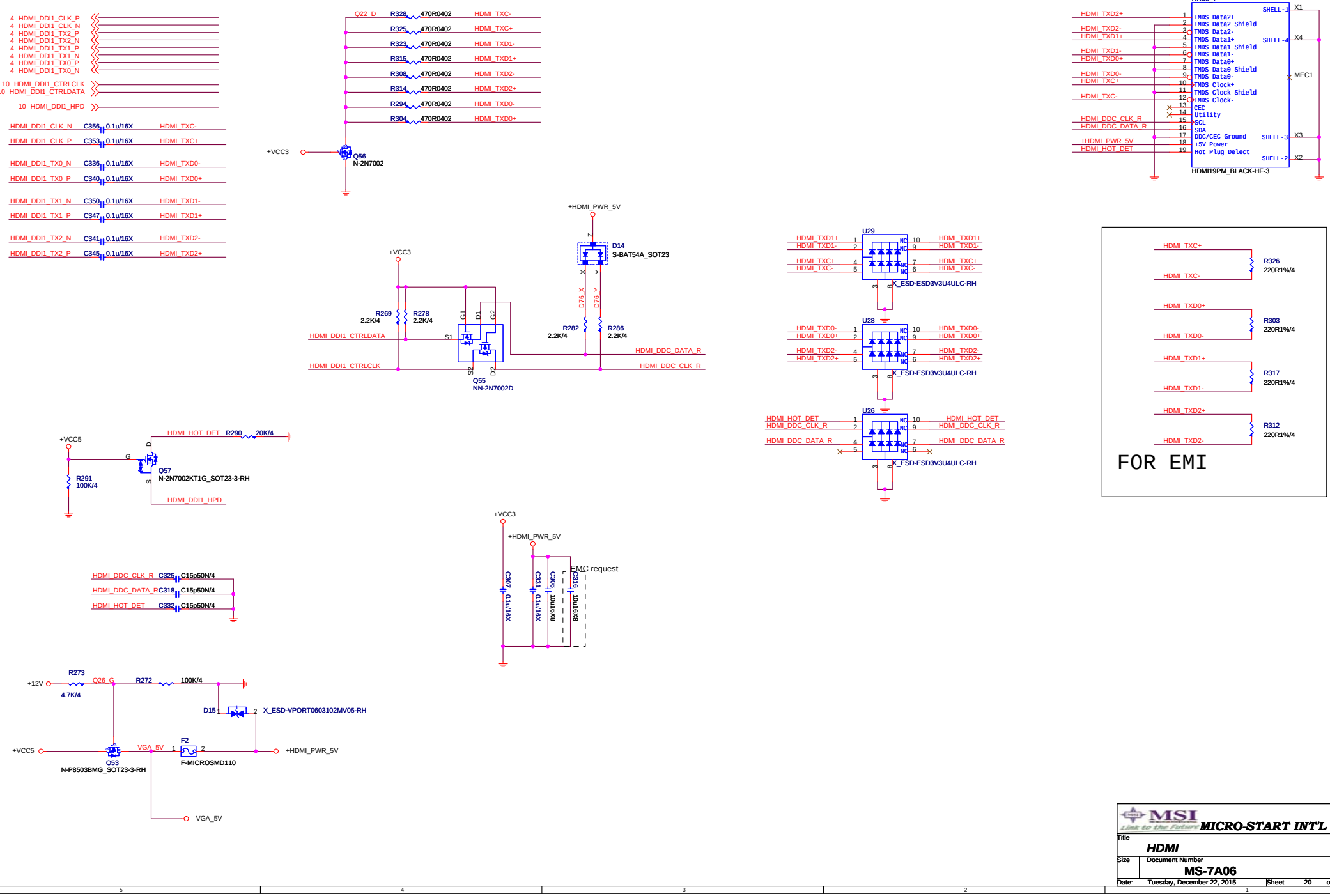
Title: M2 slot for SSD

Size | Document Number: MS-7A06 | Rev: 1.0

Date: Tuesday, December 22, 2015 | Sheet 19 of 43

HDMI Port

AVL : N5Y-19M0721-C67



MICRO-START INT'L CO.,LTD.

Title: HDMI

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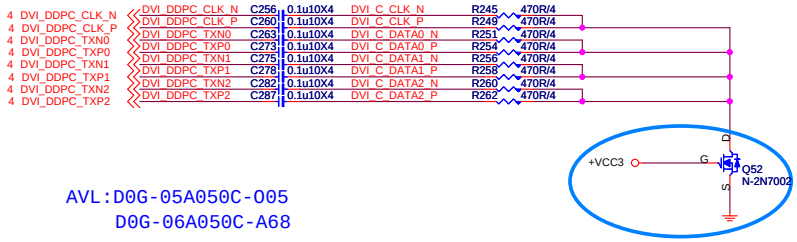
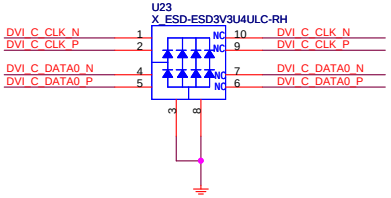
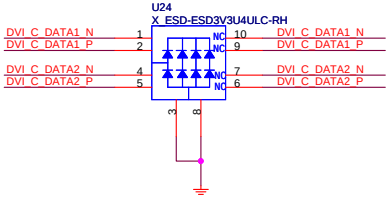
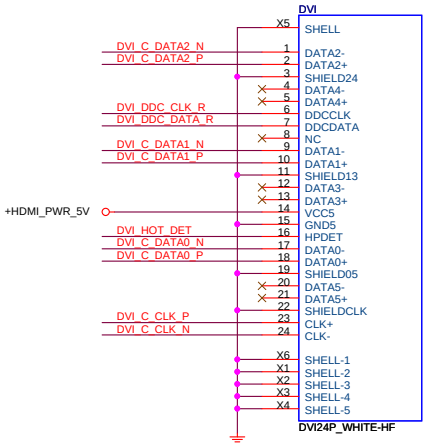
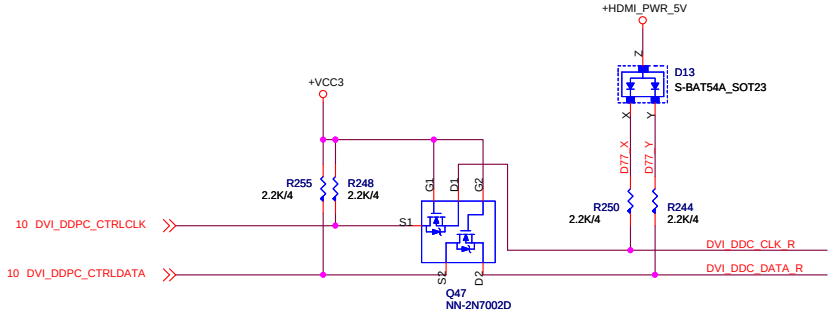


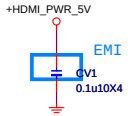
AVL:D0G-05A050C-005
D0G-06A050C-A68

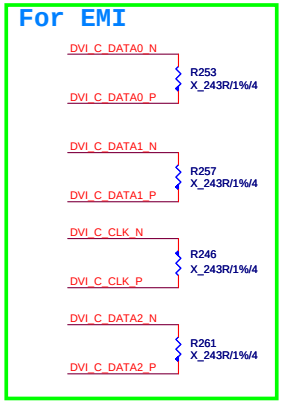


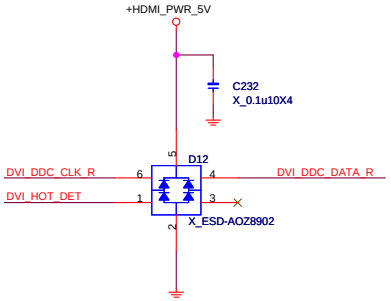


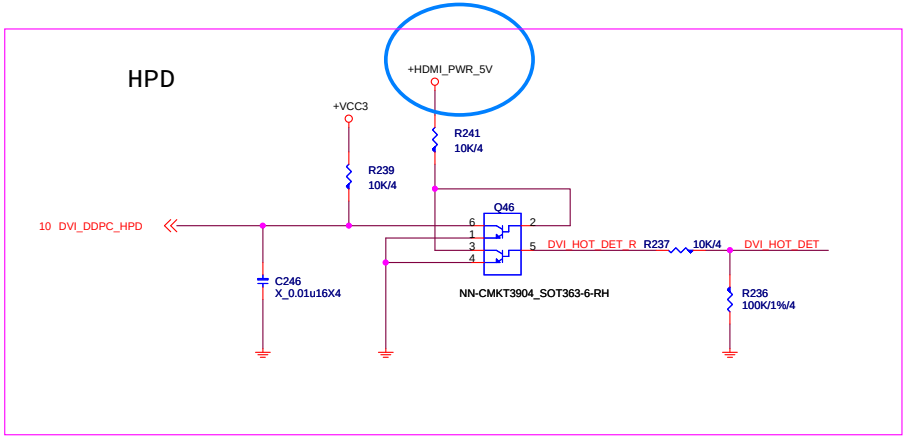


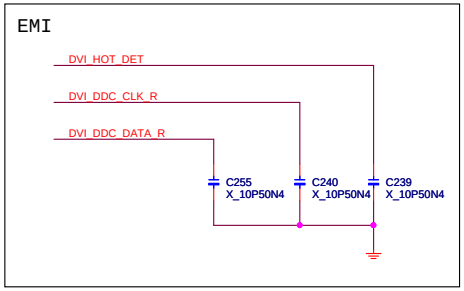












MICRO-START INT'L CO.,LTD.

Title: DVI		
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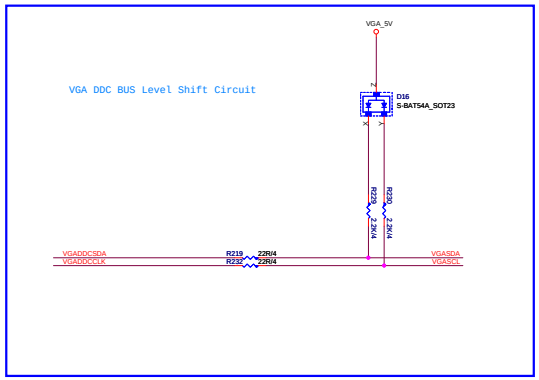

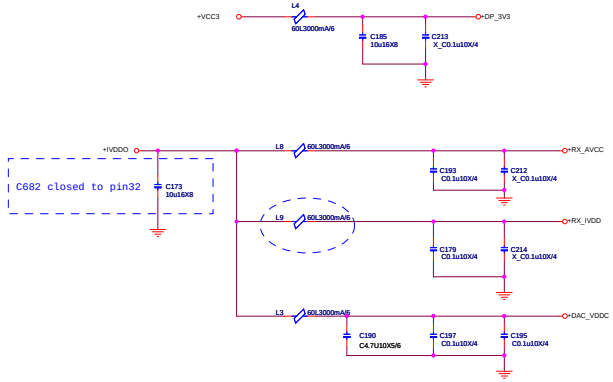

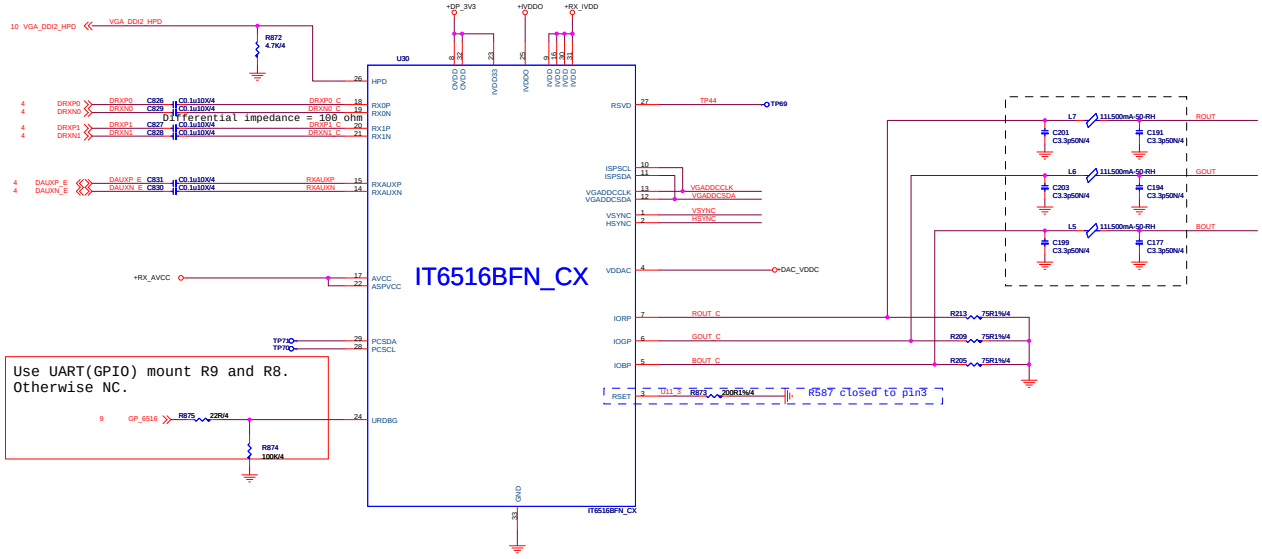

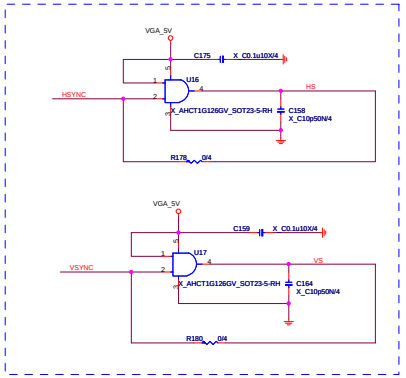

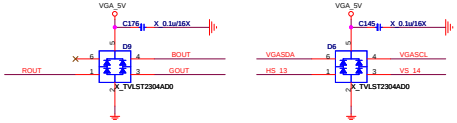

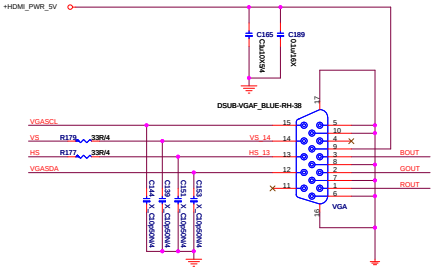

MSI	MICRO-START INTL CO.,LTD		
Title	VGA		
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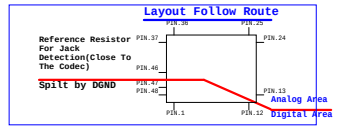
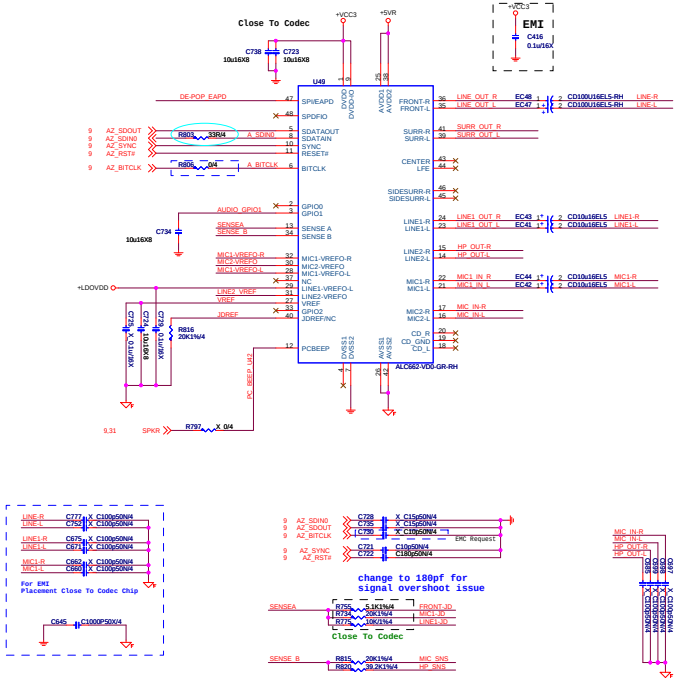
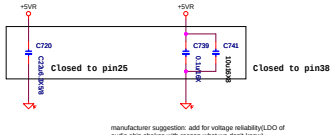
Azalia Codec - ALC662-VD

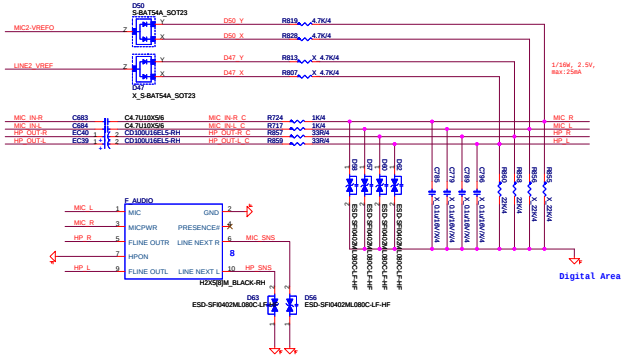






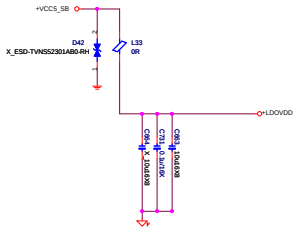
EMC Request

Front Audio Jack

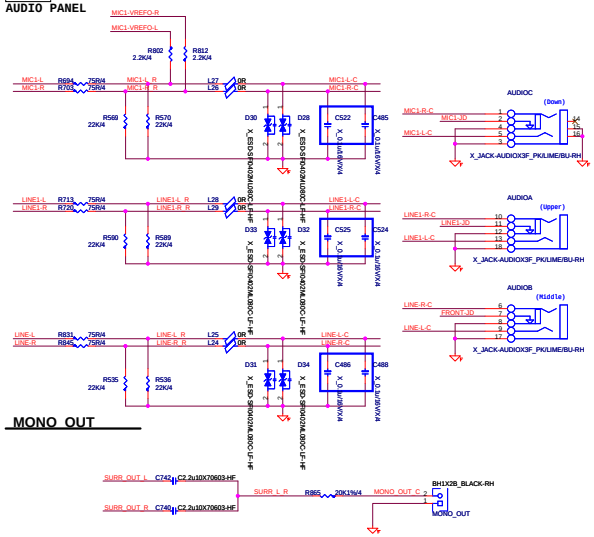


AUDIO CODE REGULATORS

Trace Width 30mils.

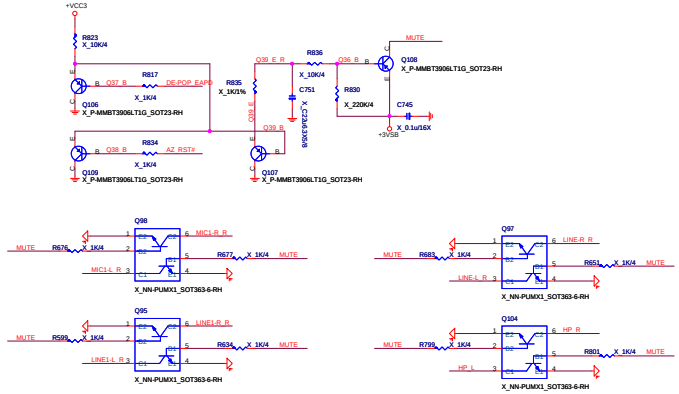


AUDIO PANEL



MONO_OUT

Audio DE-POP



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Title	Audio-ALC662VD
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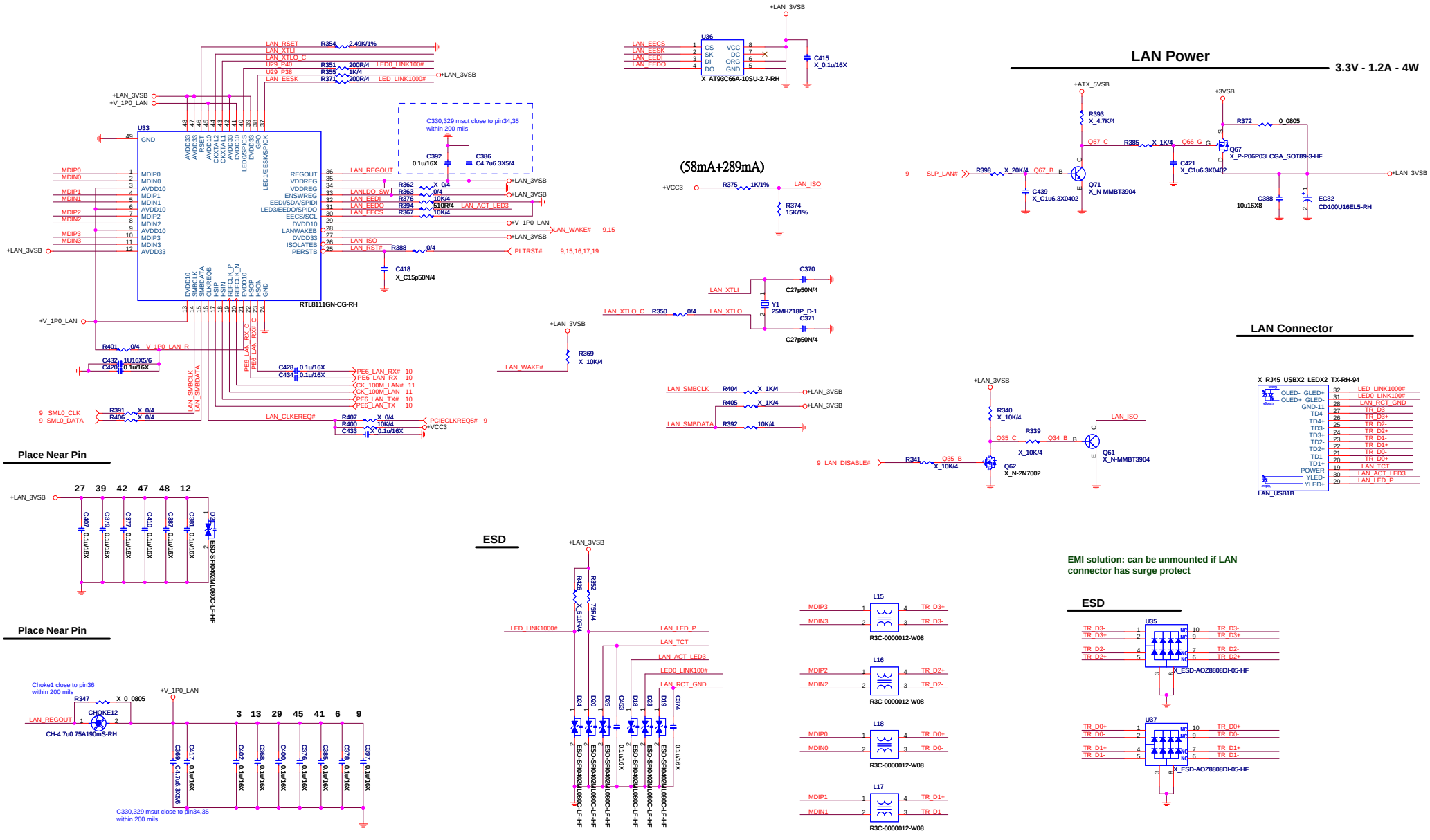
Gigabit LAN RTL8111GN



(58mA+289mA)

LAN Power

3.3V - 1.2A - 4W

LAN Connector

Place Near Pin

Place Near Pin

ESD

EMI solution: can be unmounted if LAN connector has surge protect

ESD

MSI Link to the Future	MICRO-START INTL CO.,LTD.	
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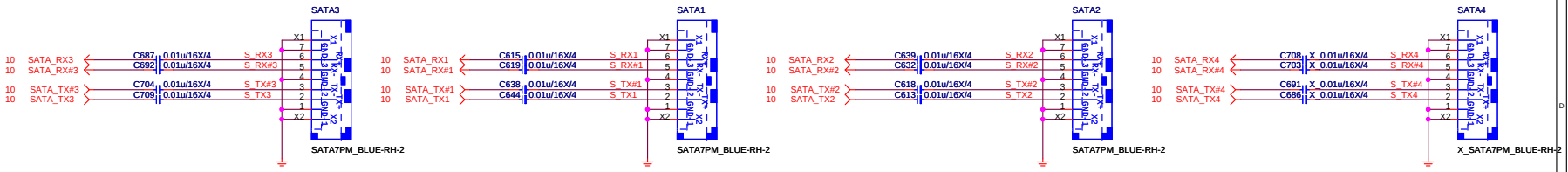
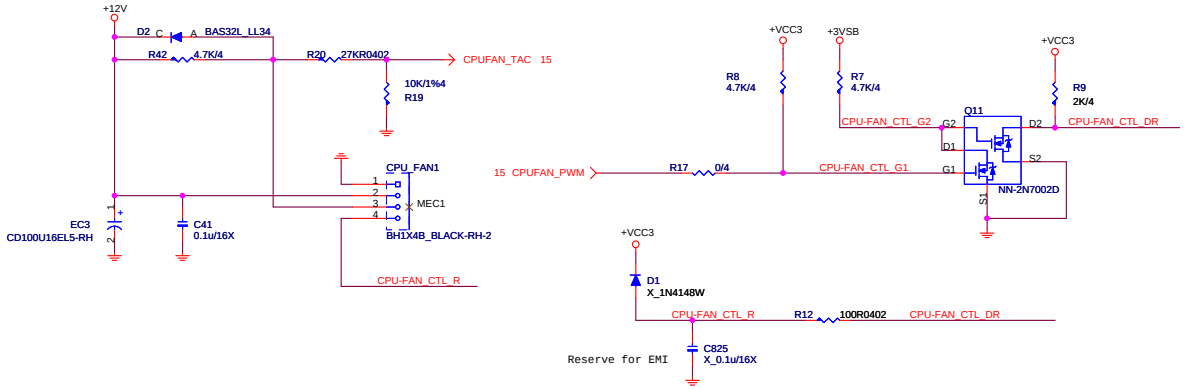
SATA3.0

SATA4 Reserve for Q170

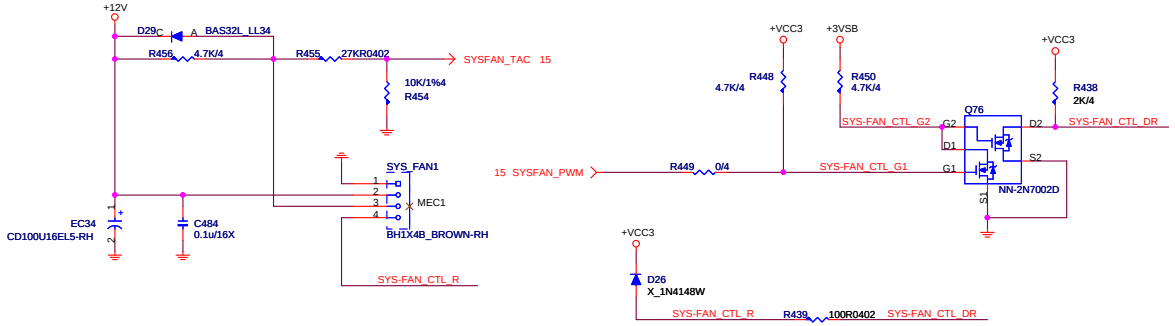


FAN

CPU Fan



System Fan



MICRO-START INTL CO.,LTD.

Title: SATA3.0 /FAN

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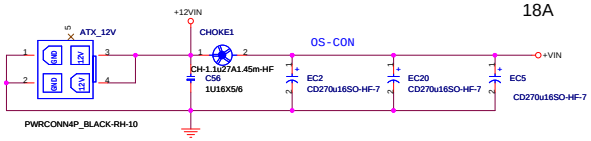
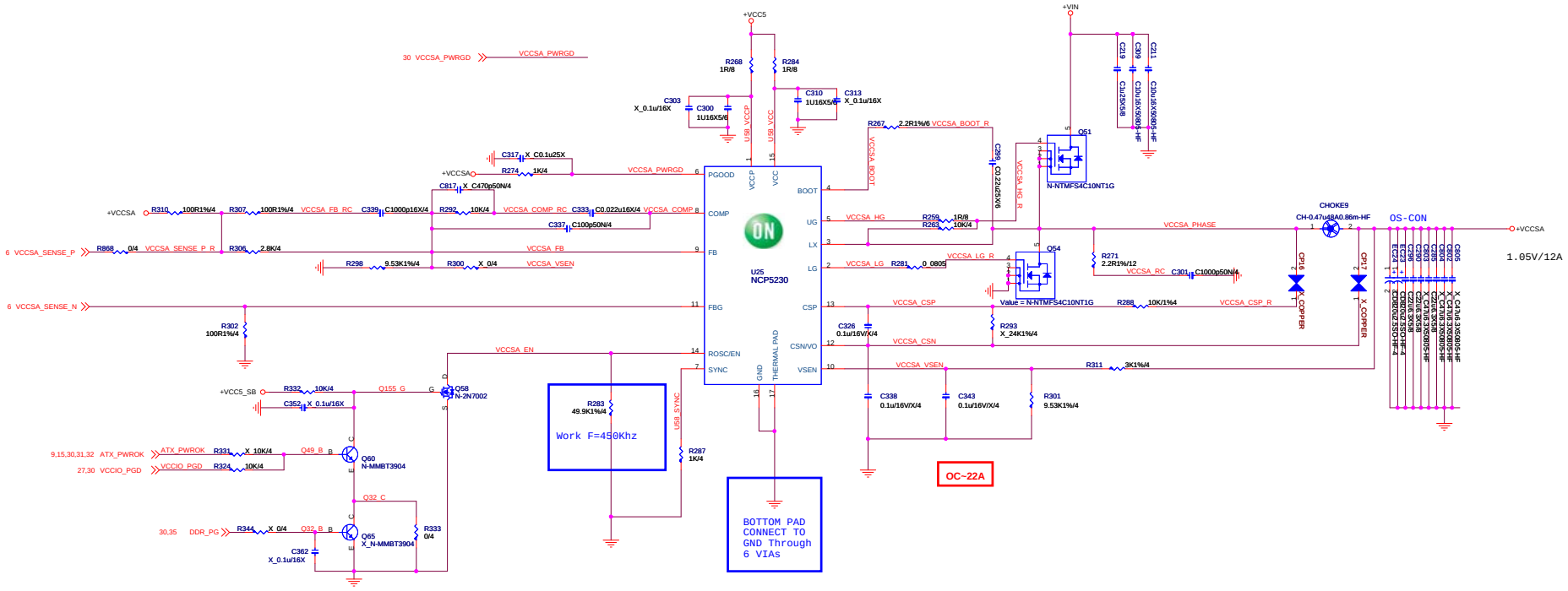


VCCSA



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	CPU Power-VCCSA /ATX_12V		
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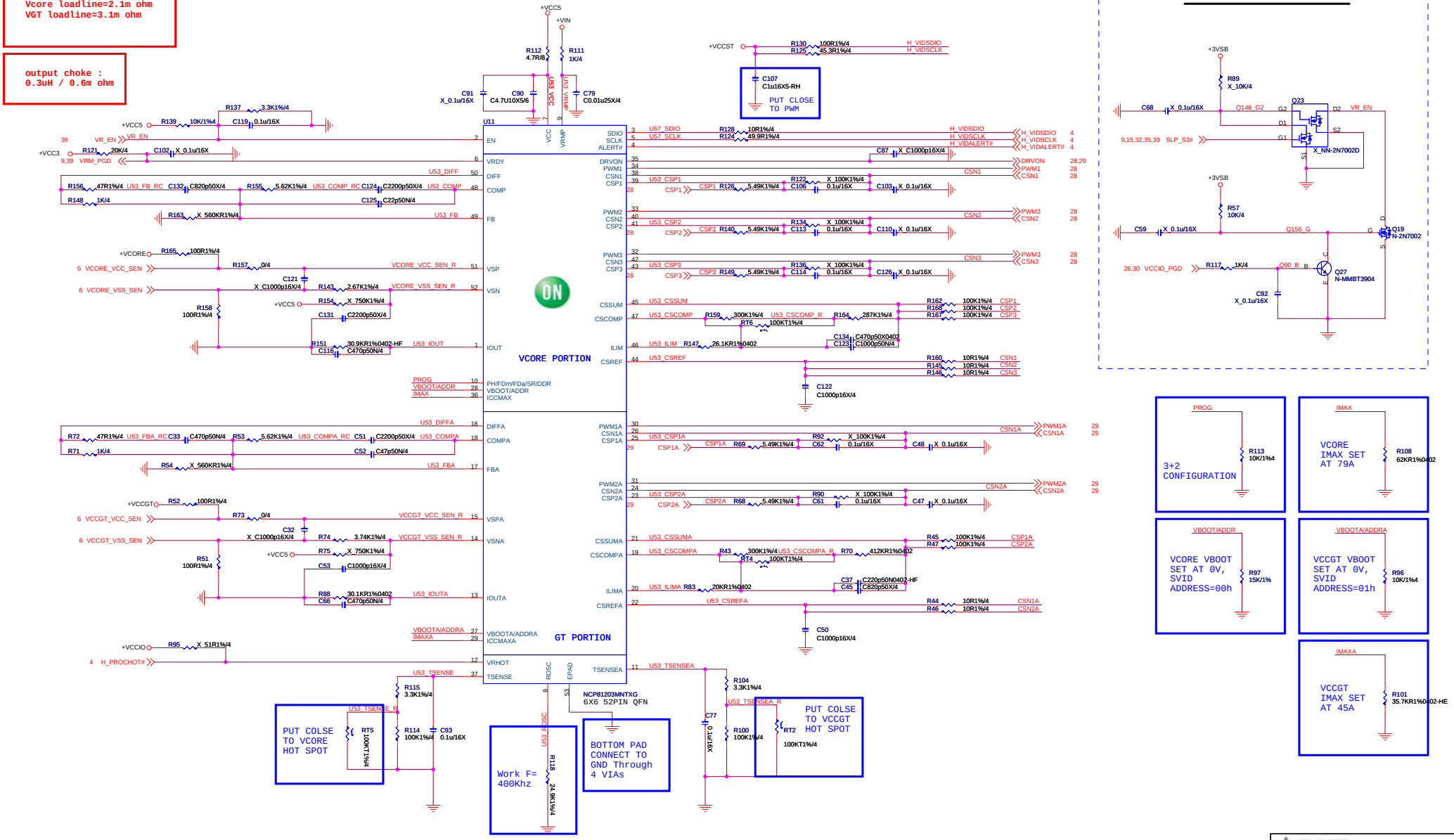
Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE

S-line 42 95W
Vcore loadline=2.1m ohm
VGT loadline=3.1m ohm

output choke :
0.3uH / 0.6m ohm



MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	IMVP8-NCP81203 5 Phase		
Size	Document Number		Rev
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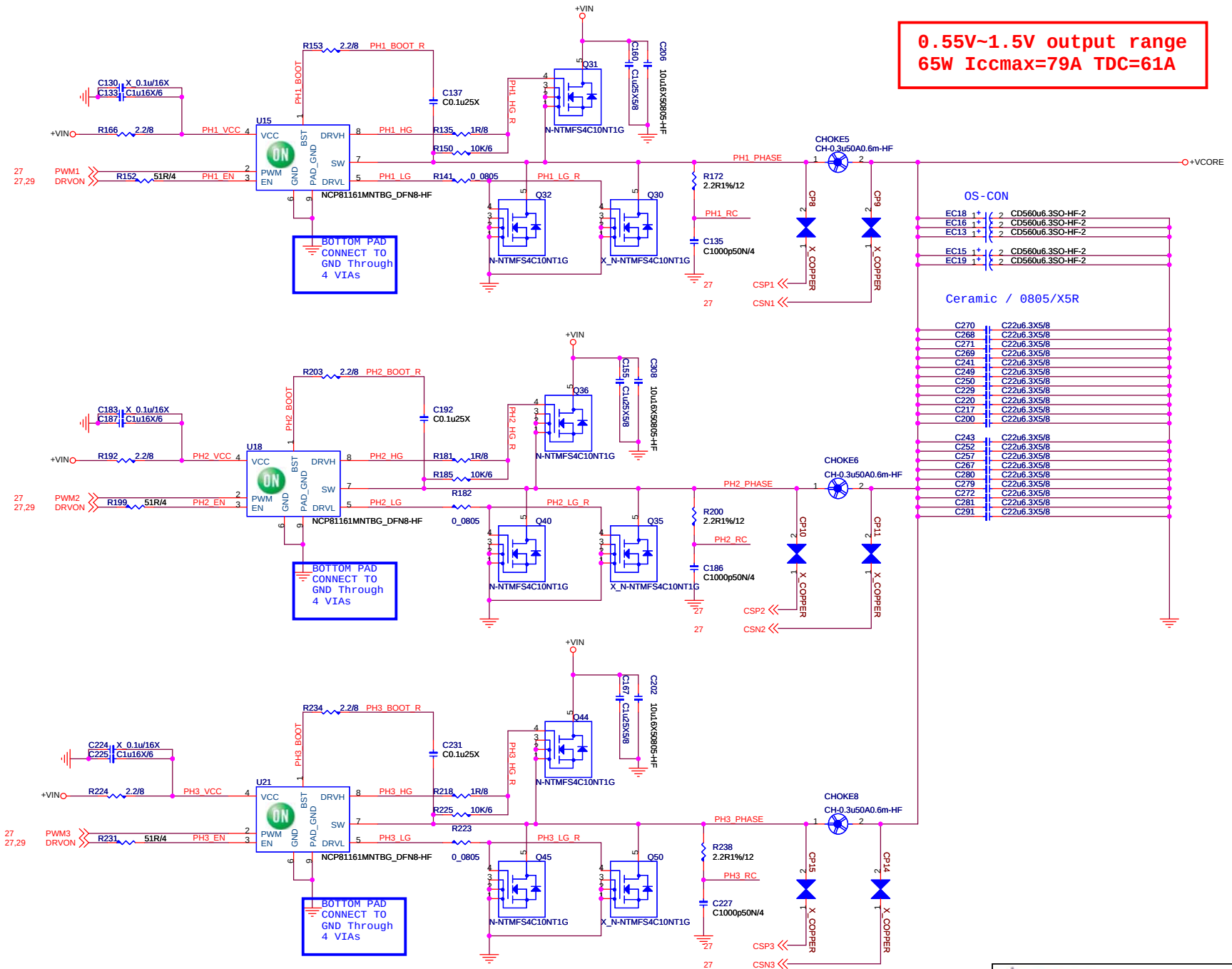

MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	CPU Power-VCORE		
Size	Document Number MS-7A06		Rev 1.0
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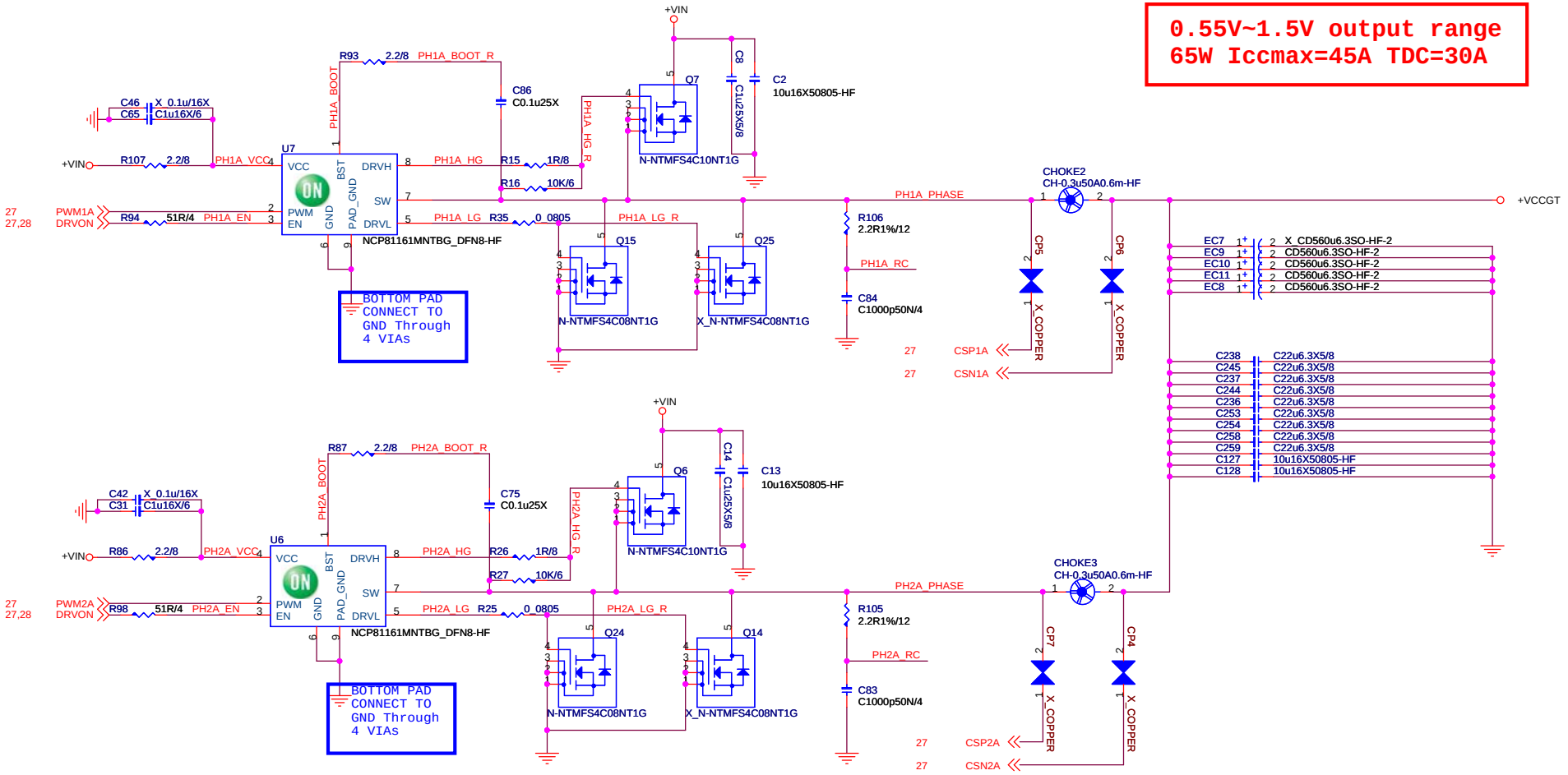

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	CPU Power-VCCGT	
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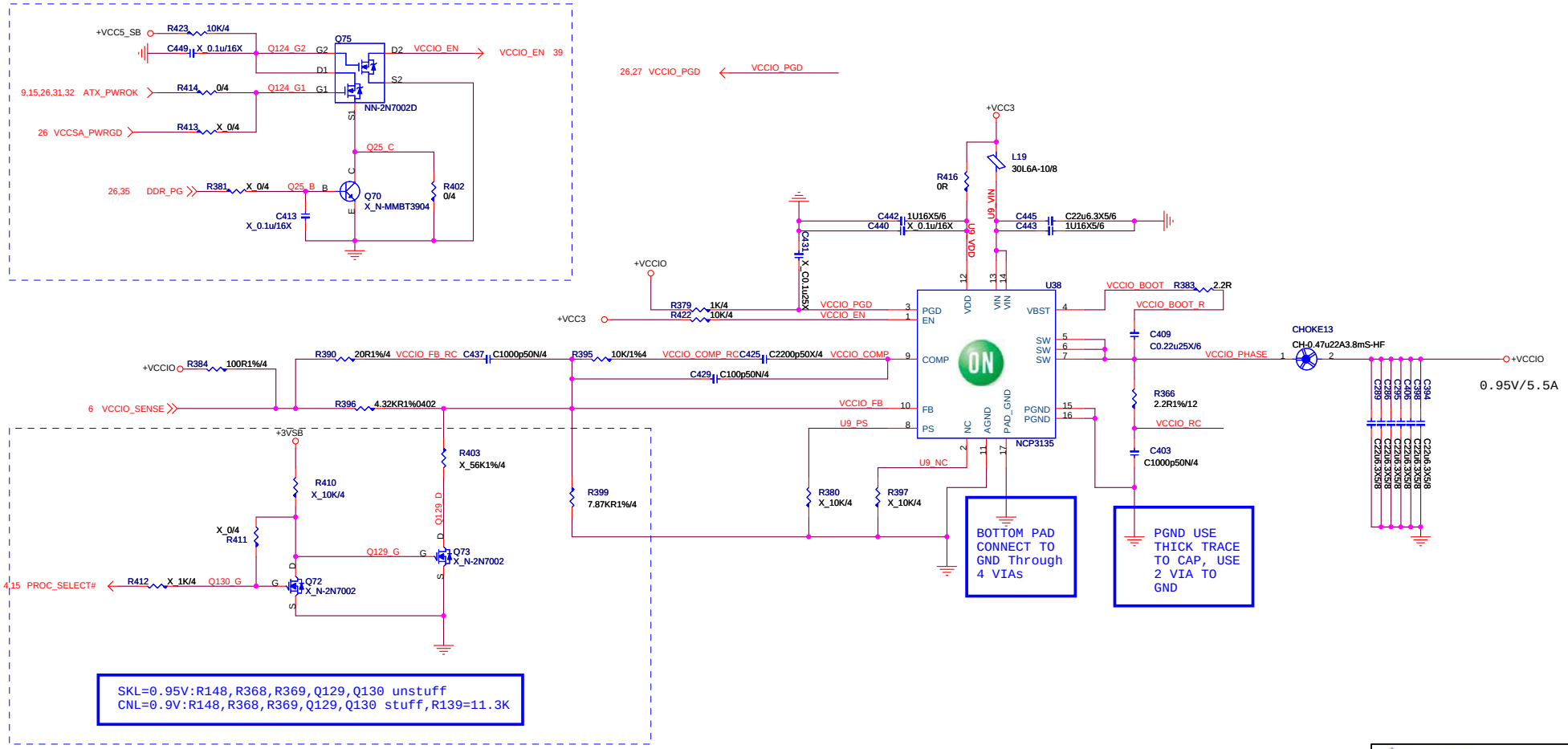
VCCIO



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Title	+VCCIO	
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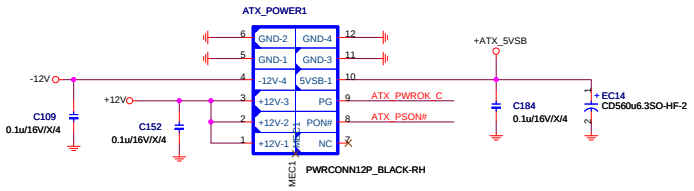
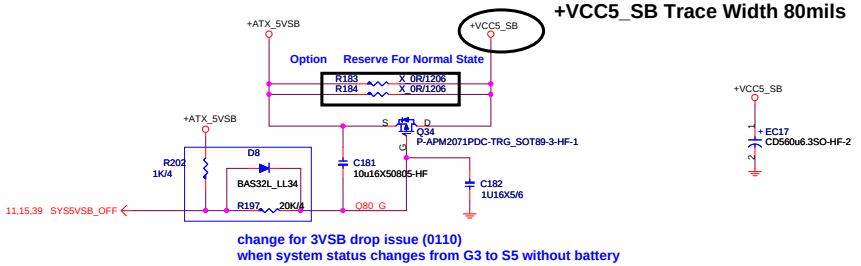
ATX Power Connector / Front Panel / LED/DSW



5VSB Power Switch

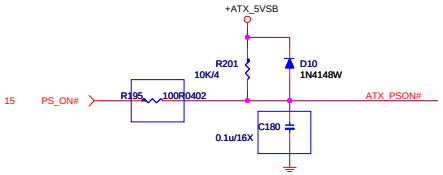
Tune ATX_5VSB inrush current to 2A from 4A

+VCC5_SB Trace Width 80mils



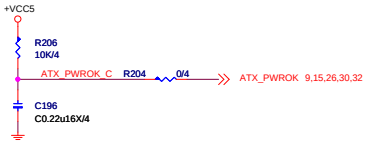
change for 3VSB drop issue (0110)
when system status changes from G3 to S5 without battery

ATX Power On

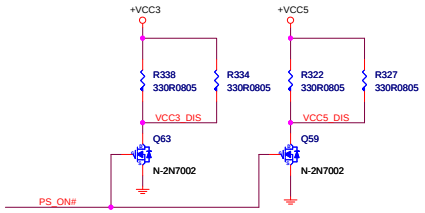


change for ATX_PSON# ring issue when it falls

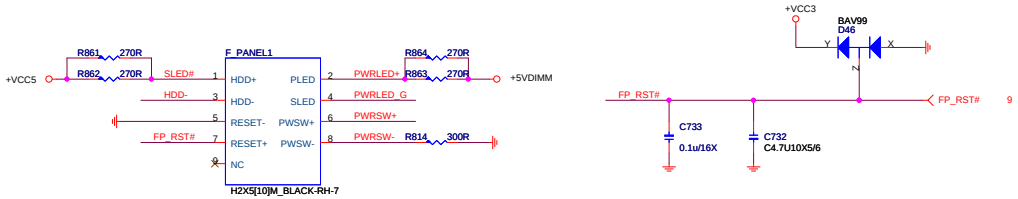
ATX Power OK



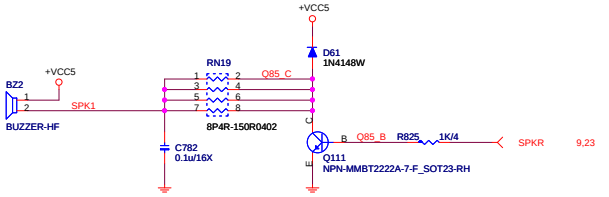
VCC3 } VCC5 Discharge Schematic



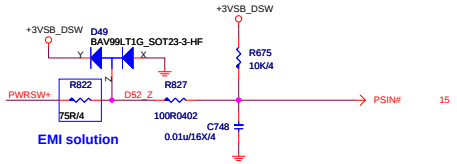
Front Panel Connector



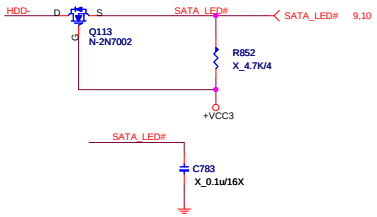
Buzzer Circuit



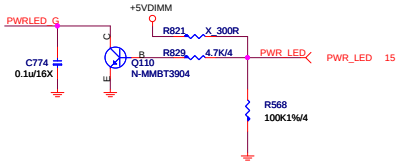
Power Button



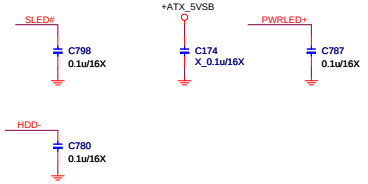
HDD LED



Power LED



Cap For EMI



MICRO-START INT'L CO.,LTD.

Title	ATX Power/Front panel/Buzzer/LED	
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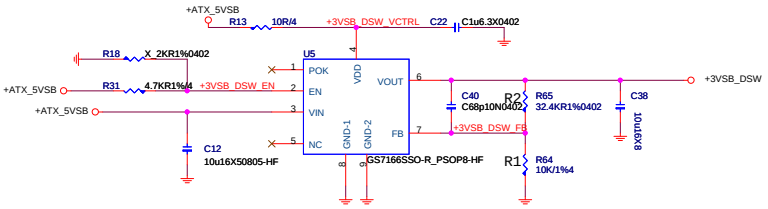
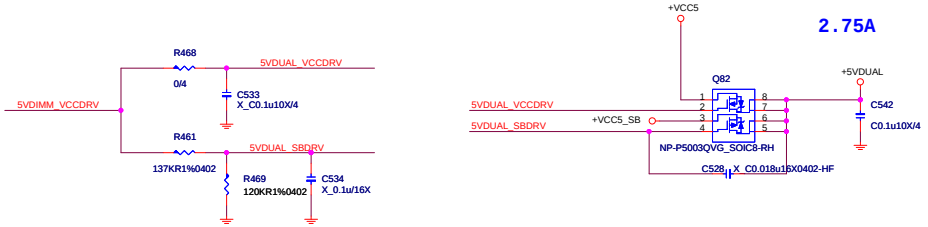
3VDSW

Vout=0.8*(R1+R2)/R1=3.392 V



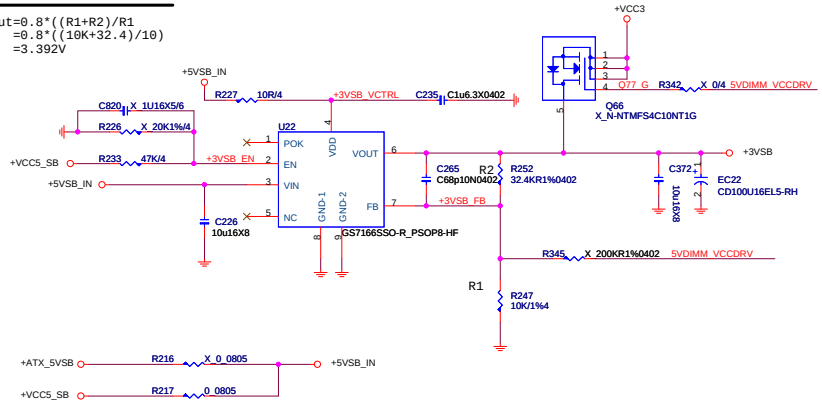
5VDUAL

5VDUAL is power source of PCH_1VSB.

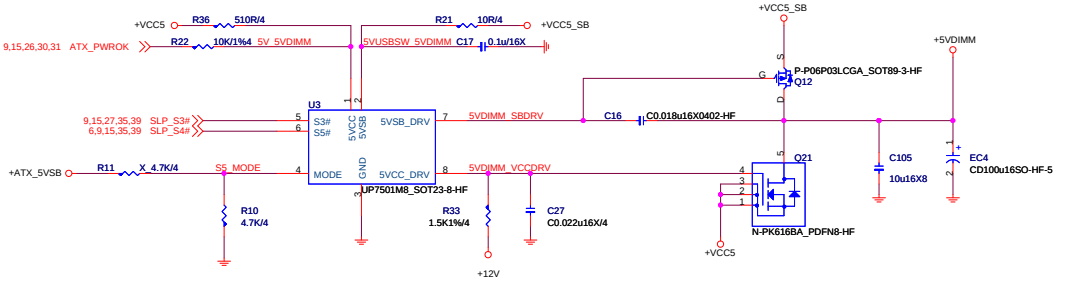


3V Standby Power

Vout=0.8*((R1+R2)/R1
=0.8*((10K+32.4)/10)
=3.392V



5VDIMM FOR DDR



36 5VDIMM_SBDRV >> 5VDIMM_SBDRV

36 5VDIMM_VCCDRV >> 5VDIMM_VCCDRV

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	ACPI Power	
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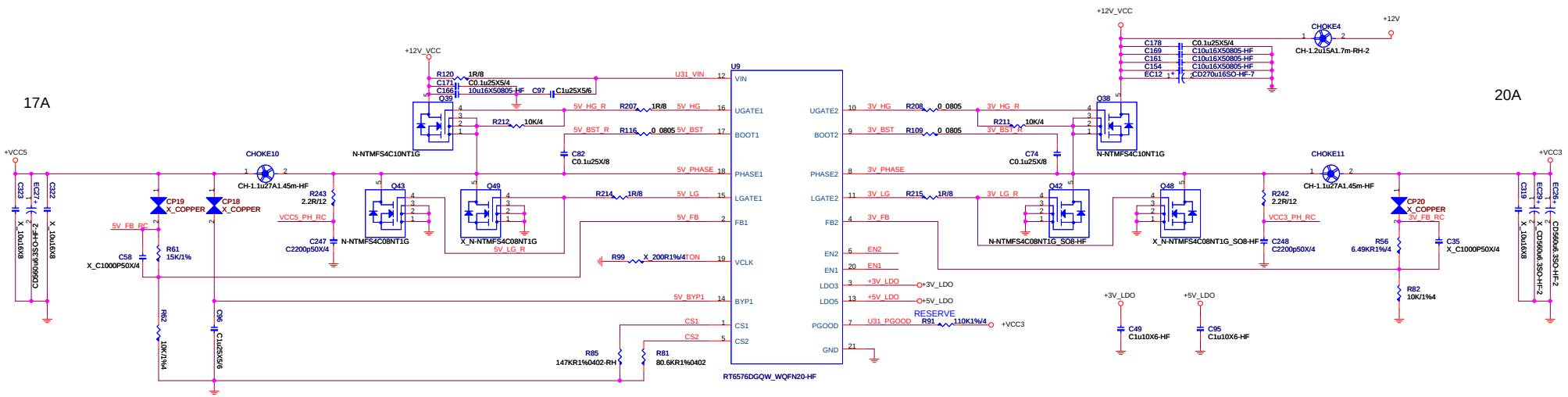
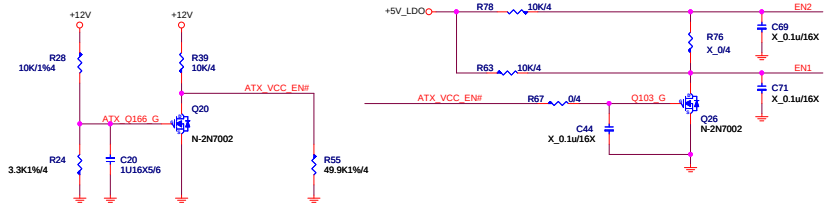
VCC3&VCC5 Power

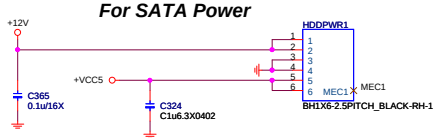


VCC3&VCC5 Power Enable

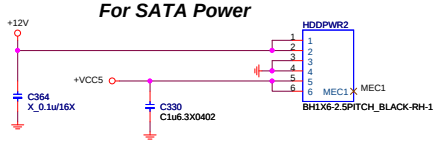


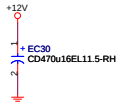
HDD & ODD Power Output Connector

For SATA Power



For SATA Power

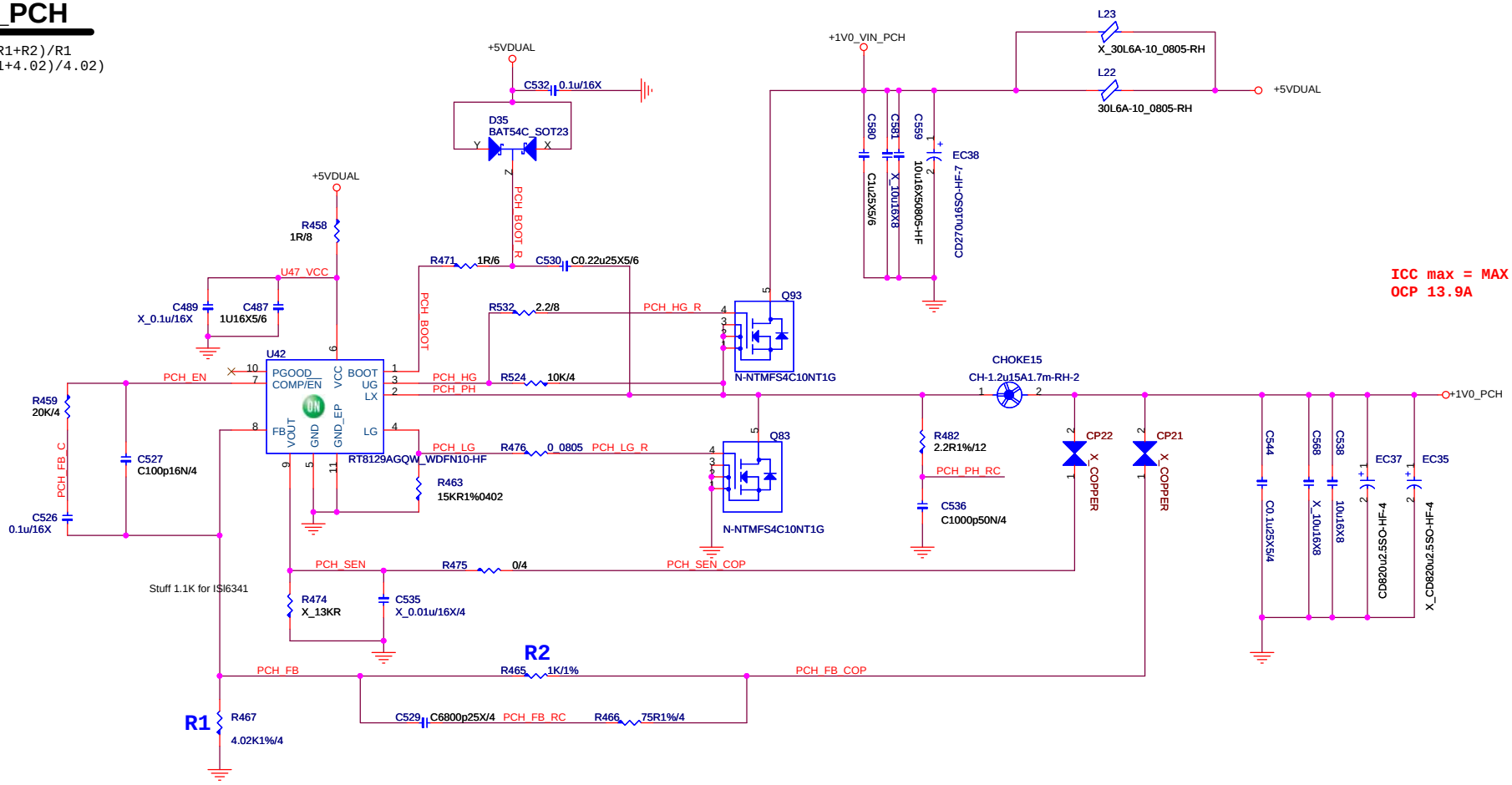




MSI Link to the Future MICRO-START INTL CO.,LTD.		
Title: VCC3 & VCC5		
Size	Document Number: MS-7A06	Rev: 1.0
Date: Tuesday, December 22, 2015	Sheet 33 of 43	

+1V0_PCH

Vout=0.8*((R1+R2)/R1
=0.8*((1+4.02)/4.02)
=1V

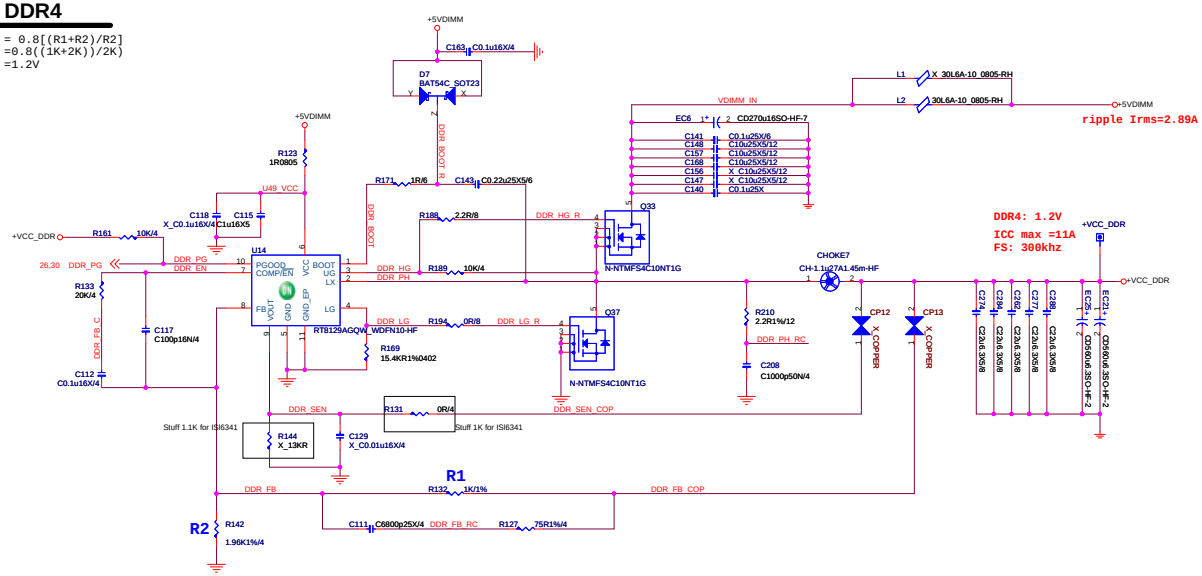


MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	+1V0_PCH	
Size	Document Number: MS-7A06	Rev: 1.0
Date: Tuesday, December 22, 2015	Sheet 34 of 43	

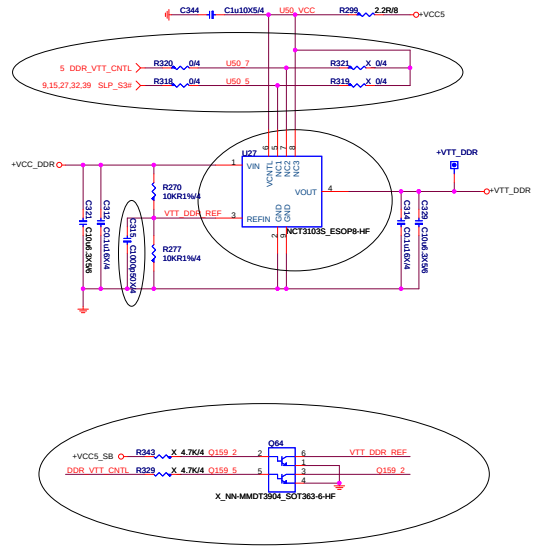
DDR4

Vout = 0.8[(R1+R2)/R2]
=0.8((1K+2K))/2K)
=1.2V



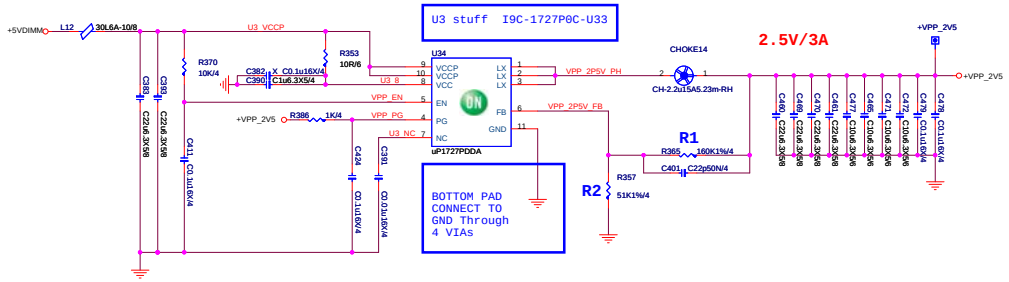
DDR4 Termination Power

0.6V - 1.1A - 0.825W

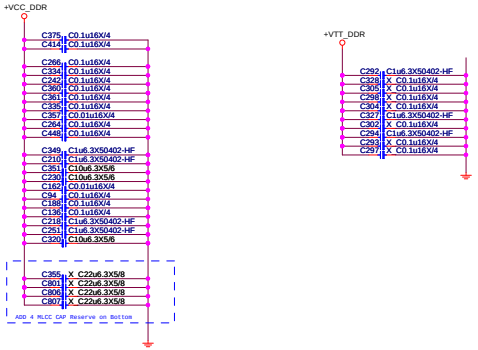


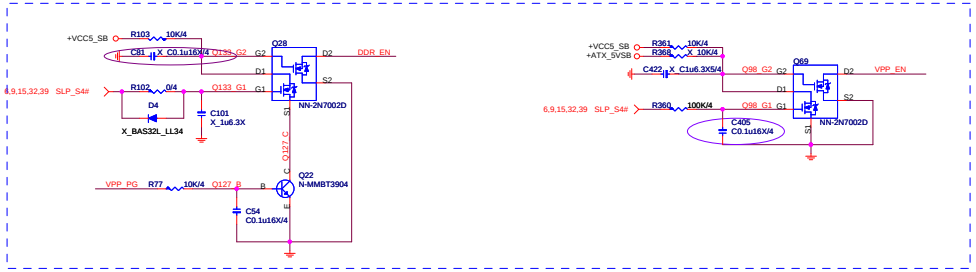
VPP_2.5V

Vout = 0.6[(R1+R2)/R2]
=0.6((10K+3.16K))/3.16K)
=2.5V



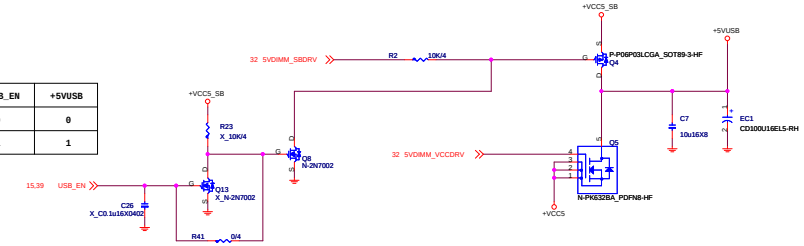
DDR4 I/O power decoulping caps.

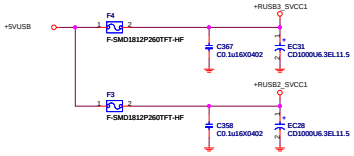


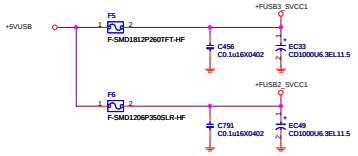


MSI MICRO-START INT'L CO.,LTD.			
Title: DDR3L Power			
Size	Document Number: MS-7A06		Rev: 1.0
Date: Tuesday, December 22, 2015	Sheet 35 of 43		

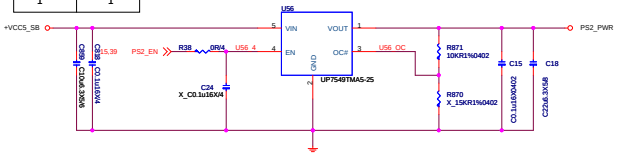
USB_EN	+5VUSB
0	0
1	1





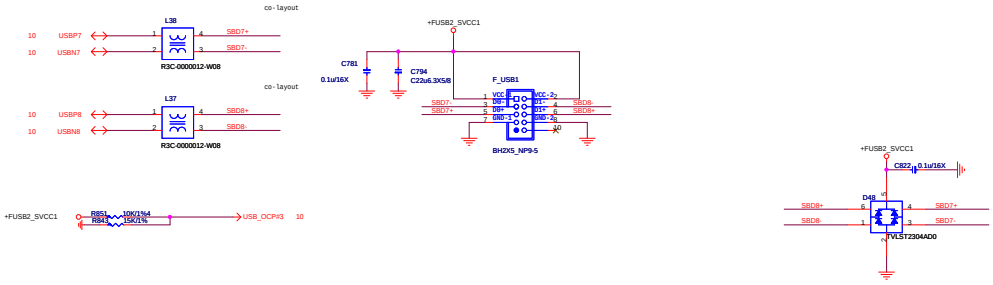


PS2_EN	PS2_PWR
0	0
1	1

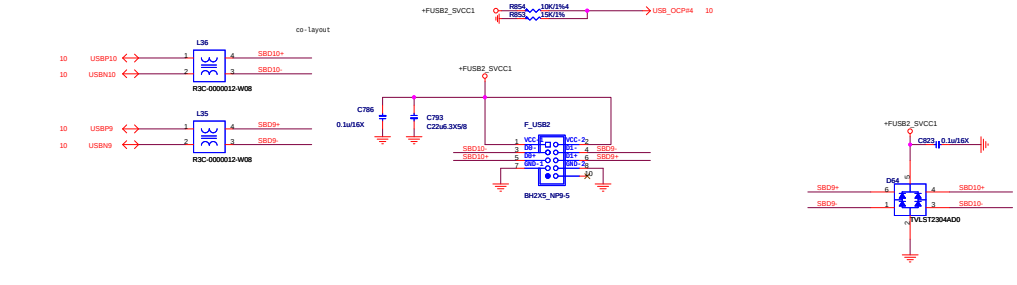


MSI	MICRO-START INTL CO.,LTD	
Title	USB Power	
Size	Document Number: MS-7A06	Rev: 1.0
Date: Tuesday, December 22, 2015	Sheet 36 of 43	

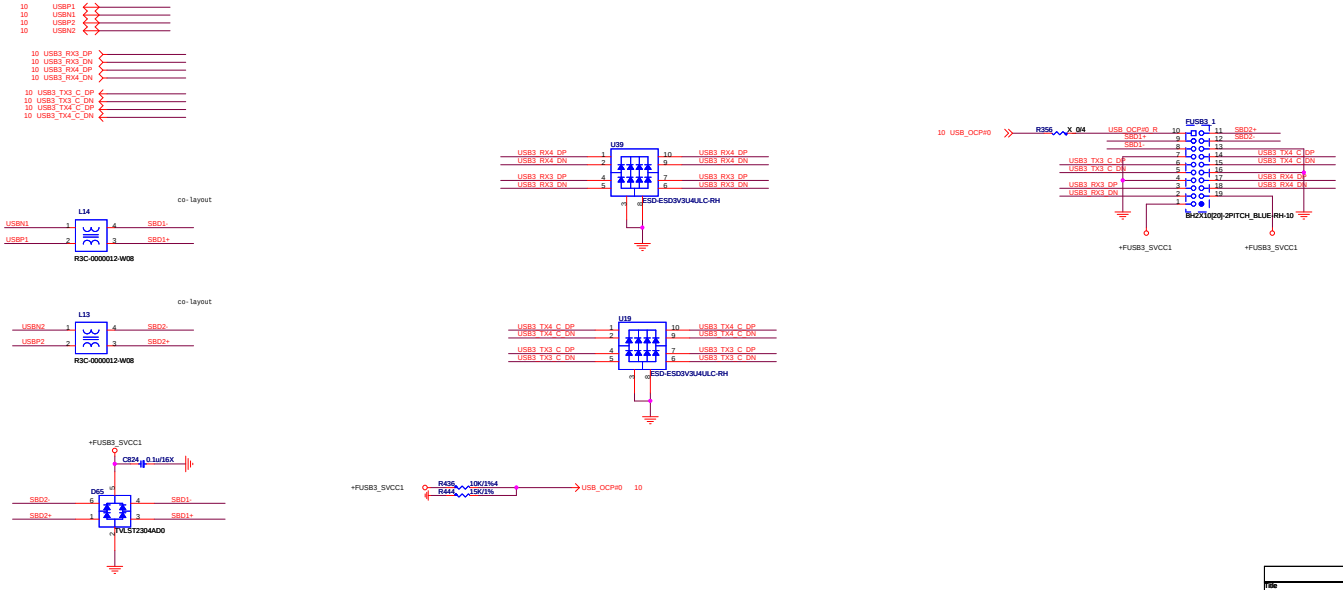
Front Panel USB Connnector For USB Port 2 / 4



Front Panel USB Connnector For USB Port 2 / 4

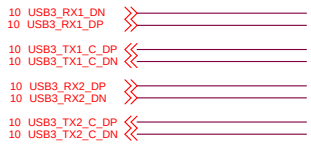


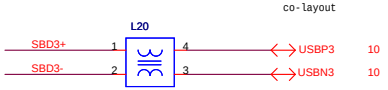
Front Panel USB3.0 Connnector For USB Port 1 / 2

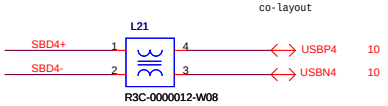


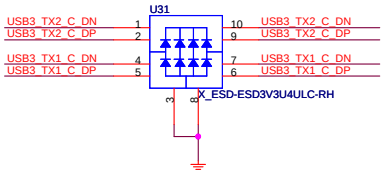
Title	Front USB2.0/3.0		
Size	Document Number		Rev
Custom	MS-7A06		1.0
Date:	Tuesday, December 22, 2015	Sheet 37 of 43	

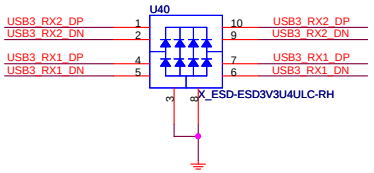
Rear USB3.0 Connnector For USB Port 3 / 4

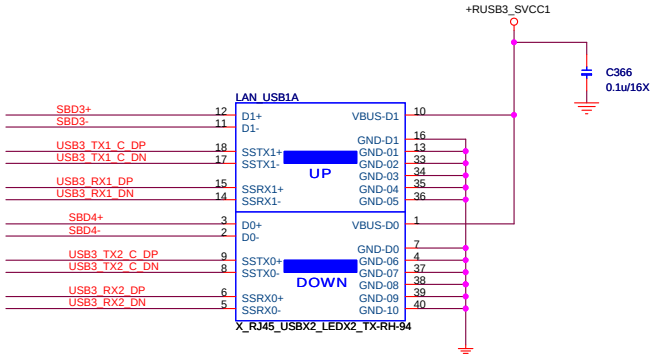


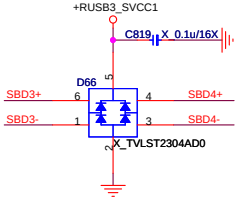


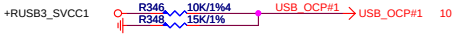




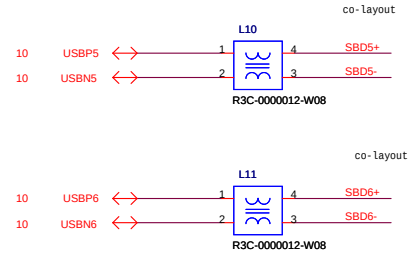


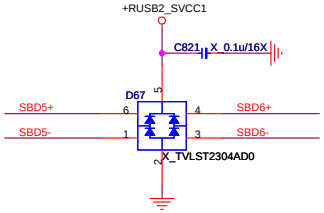


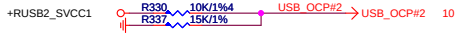


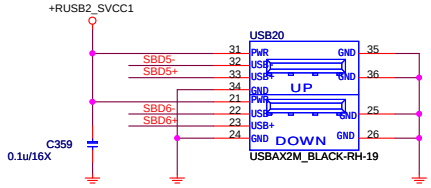


Rear USB2.0 Connnector For USB Port 5 / 6









Title: Rear USB2.0/3.0		
Size: Custom	Document Number: MS-7A06	Rev: 1.0
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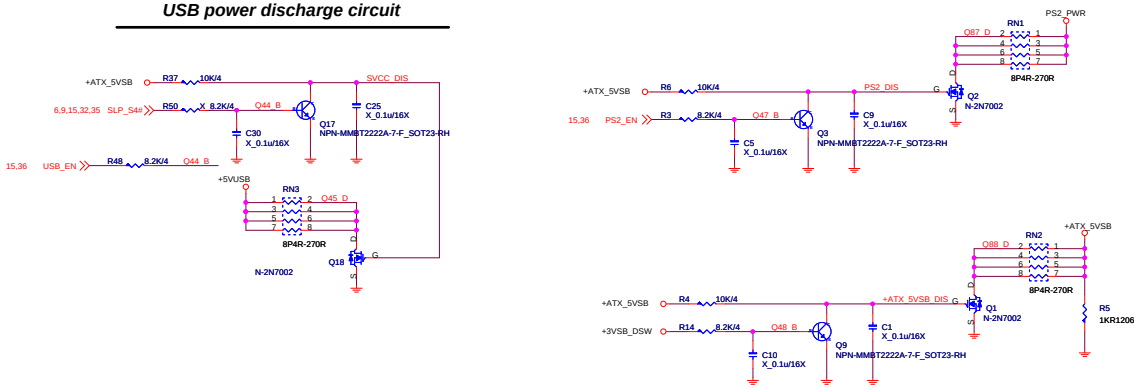
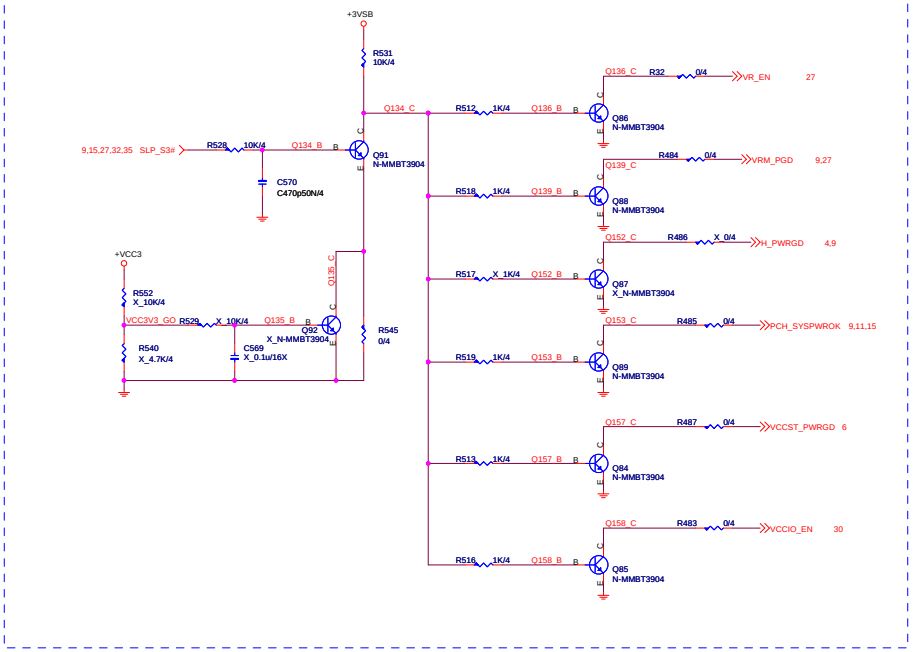
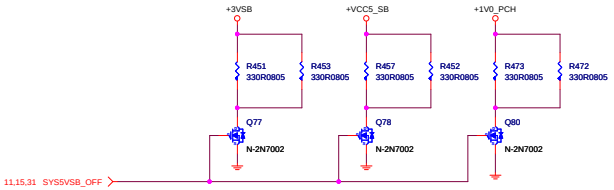
USB power discharge circuit



Power on/down sequencing circuit



Standby Power Discharge Schematic



MSI — MICRO-START INT'L CO.,LTD.

Title: USB Power Dischage

Size	Document Number	Rev
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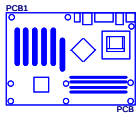
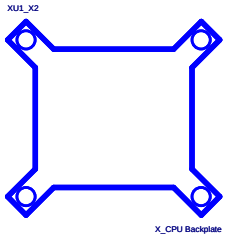
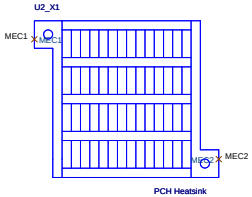
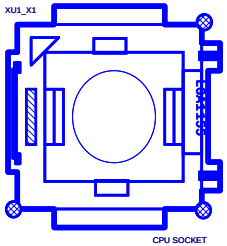
Manual Parts



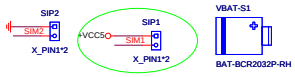
PK0-07A0610-G37/PK0-07A0610-E48







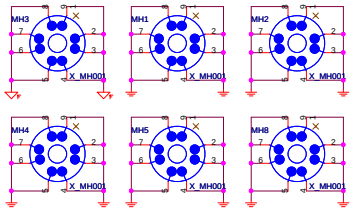
Simulation



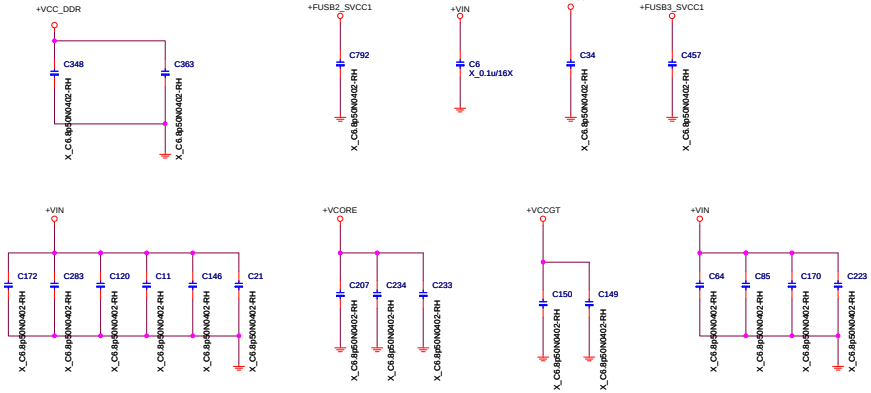
GASKET1 0PT | HDMI_LABEL 0PT | HDMI_LOGO 0PT

BIOS_ROM1 0PT | Q170 0PT | AUDIO 0PT | LAN_USB1 0PT

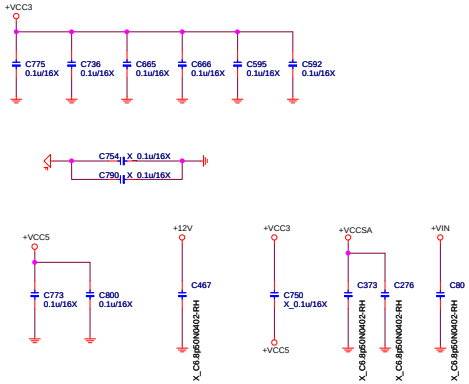
Mounting Holes



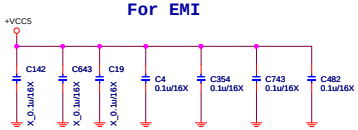
For RF



For EMI



For EMI



Optics Orientation Holes

Optical Fiducial Marks-120

MSI Click On The Future	MICRO-START INT'L CO.,LTD.	
Title: Manual & Option Parts		
Size	Document Number: MS-7A06	Rev: 1.0
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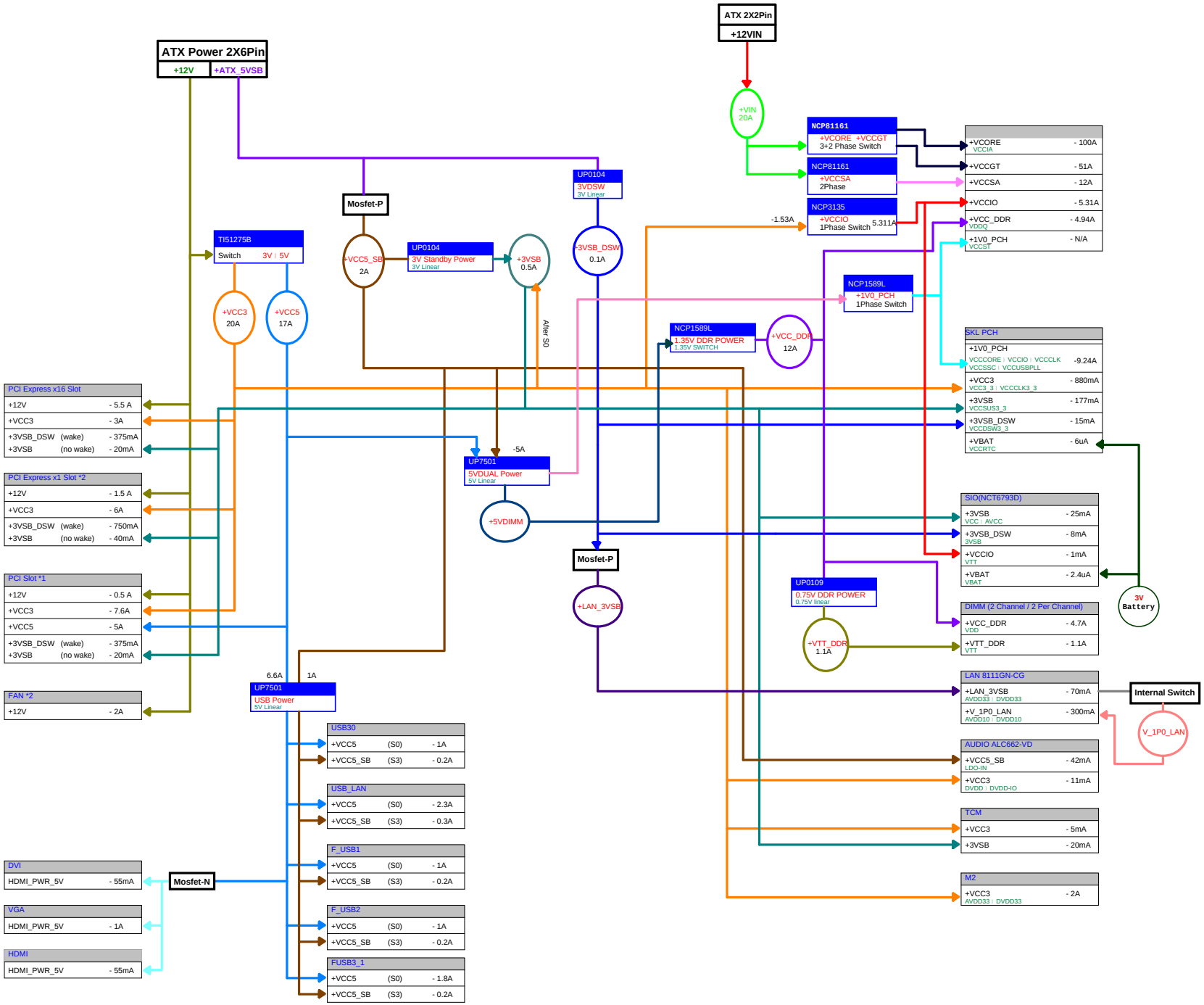
ATX 2X2Pin
+12VIN
ATX Power 2X6Pin
+12V
+ATX_5VSB
+VIN
20A
NCP81161
+VCORE +VCCGT
3+2 Phase Switch
NCP81161
+VCCSA
2Phase
NCP3135
+VCCIO
1Phase Switch
5.311A
-1.53A
+VCORE - 100A
VCCIA
+VCCGT - 51A
+VCCSA - 12A
+VCCIO - 5.31A
+VCC_DDR - 4.94A
VDDQ
+1V0_PCH - N/A
VCCST
Mosfet-P
UP0104
3VDSW
3V Linear
+3VSB_DSW
0.1A
TI51275B
Switch 3V 5V
+VCC3
20A
+VCC5
17A
+VCC5_SB
2A
UP0104
3V Standby Power
3V Linear
+3VSB
0.5A
After S0
NCP1589L
+1V0_PCH
1Phase Switch
NCP1589L
1.35V DDR POWER
1.35V SWITCH
+VCC_DDR
12A
SKL PCH
+1V0_PCH
VCCCORE VCCIO VCCCLK
VCCSSC VCCUSBPLL
-9.24A
+VCC3 - 880mA
VCC3_3 VCCCLK3_3
+3VSB - 177mA
VCCSUS3_3
+3VSB_DSW - 15mA
VCCDSW3_3
+VBAT - 6uA
VCCRTC
PCI Express x16 Slot
+12V - 5.5 A
+VCC3 - 3A
+3VSB_DSW (wake) - 375mA
+3VSB (no wake) - 20mA
PCI Express x1 Slot *2
+12V - 1.5 A
+VCC3 - 6A
+3VSB_DSW (wake) - 750mA
+3VSB (no wake) - 40mA
PCI Slot *1
+12V - 0.5 A
+VCC3 - 7.6A
+VCC5 - 5A
+3VSB_DSW (wake) - 375mA
+3VSB (no wake) - 20mA
FAN *2
+12V - 2A
-5A
UP7501
5VDUAL Power
5V Linear
+5VDIMM
Mosfet-P
+LAN_3VSB
UP0109
0.75V DDR POWER
0.75V linear
+VTT_DDR
1.1A
SIO(NCT6793D)
+3VSB - 25mA
VCC AVCC
+3VSB_DSW - 8mA
3VSB
+VCCIO - 1mA
VTT
+VBAT - 2.4uA
VBAT
3V Battery
DIMM (2 Channel / 2 Per Channel)
+VCC_DDR - 4.7A
VDD
+VTT_DDR - 1.1A
VTT
LAN 8111GN-CG
+LAN_3VSB - 70mA
AVDD33 DVDD33
+V_1P0_LAN - 300mA
AVDD10 DVDD10
Internal Switch
V_1P0_LAN
AUDIO ALC662-VD
+VCC5_SB - 42mA
LDO-IN
+VCC3 - 11mA
DVDD DVDD-IO
TCM
+VCC3 - 5mA
+3VSB - 20mA
M2
+VCC3 - 2A
AVDD33 DVDD33
6.6A
1A
UP7501
USB Power
5V Linear
USB30
+VCC5 (S0) - 1A
+VCC5_SB (S3) - 0.2A
USB_LAN
+VCC5 (S0) - 2.3A
+VCC5_SB (S3) - 0.3A
F_USB1
+VCC5 (S0) - 1A
+VCC5_SB (S3) - 0.2A
F_USB2
+VCC5 (S0) - 1A
+VCC5_SB (S3) - 0.2A
FUSB3_1
+VCC5 (S0) - 1.8A
+VCC5_SB (S3) - 0.2A
Mosfet-N
DVI
HDMI_PWR_5V - 55mA
VGA
HDMI_PWR_5V - 1A
HDMI
HDMI_PWR_5V - 55mA
MSI
MICRO-START INT'L CO.,LTD
Power Map
MS-7A06
1.0

PCH_GPIO

PCH

GPIO	I/O/NC	Power	Tol	Usage
GPP_A0	I/O	Core	3.3V	KBRST#
GPP_A1	I/O	Core	3.3V	LPC_AD0
GPP_A2	I/O	Core	3.3V	LPC_AD1
GPP_A3	I/O	Core	3.3V	LPC_AD2
GPP_A4	I/O	Core	3.3V	LPC_AD3
GPP_A5	I/O	Core	3.3V	LPC_FRAME#
GPP_A6	I/O	Core	3.3V	LPC_SERIRQ
GPP_A7	I/O	Core	3.3V	LPC_DRQ#0
GPP_A8	I/O	Core	3.3V	CLKRUN#
GPP_A9	I/O	Core	3.3V	LPC_CLK_24M
GPP_A10	I/O	Core	3.3V	PCI_CLK_24M
GPP_A11	I/O	Standby	3.3V	SIO_PME#
GPP_A12	I/O	Standby	3.3V	BMBUSY#
GPP_A13	I/O	Standby	5V	PCH_SUSWARN#
GPP_A14	I/O	Core	3.3V	SUS_STAT#
GPP_A15	I/O	Standby	3.3V	PCH_SUSACK#
GPP_A19	I/O	Standby	3.3V	PCH_GPIO19
GPP_A21	I/O	Standby	3.3V	PCH_GPIO21
GPP_A23	I/O	Standby	3.3V	PCH_GPIO23

GPIO	I/O/NC	Power	Tol	Usage
GPP_B2	I/O	Standby	3.3V	PCH_VRALERT#
GPP_B4	I/O	Standby	3.3V	LPT_DET#
GPP_B6	I/O	Standby	3.3V	PCIECLKREQ1#
GPP_B7	I/O	Standby	3.3V	PCIECLKREQ2#
GPP_B10	I/O	Standby	3.3V	PCIECLKREQ5#
GPP_B13	I/O	Standby	3.3V	PLTRST#
GPP_B14	I/O	Core	3.3V	SPKR
GPP_B18	I/O	Standby	3.3V	REBOOT_STRAP
GPP_B20	I/O	Core	3.3V	SMI#
GPP_B22	I/O	Standby	3.3V	BBS_STRAP
GPP_B23	I/O	Standby	3.3V	THERMTRIP_STRAP

GPIO	I/O/NC	Power	Tol	Usage
GPP_C0	I/O	Standby	3.3V	SMBCLK
GPP_C1	I/O	Standby	3.3V	SMBDATA
GPP_C2	I/O	Standby	3.3V	TLS_STRAP
GPP_C3	I/O	Standby	3.3V	SML0_CLK
GPP_C4	I/O	Standby	3.3V	SML0_DATA
GPP_C5	I/O	Standby	3.3V	ESPI_STRAP
GPP_C6	I/O	Standby	3.3V	SML1_CLK
GPP_C7	I/O	Standby	3.3V	SML1_DATA
GPP_C11	I/O	Core	3.3V	PU_PCH_GPP_C_11

GPIO	I/O/NC	Power	Tol	Usage
GPP_D2	Pull Down	NA	NA	PD_PCH_GPP_D_2
GPP_D3	Pull Down	NA	NA	PD_PCH_GPP_D_3
GPP_D14	I/O	Standby	3.3V	PU_FM_LA_TRIGGER#

GPIO	I/O/NC	Power	Tol	Usage
GPP_E0	I/O	Standby	3.3V	SATAGP0_SSD
GPP_E3	I/O	Standby	3.3V	PCH_CPU_GP0
GPP_E4	I/O	Core	3.3V	DEVSLP0
GPP_E8	I/O	Core	3.3V	SATA_LED#
GPP_E9	I/O	Standby	3.3V	USB_OCP#0
GPP_E10	I/O	Standby	3.3V	USB_OCP#1
GPP_E11	I/O	Standby	3.3V	USB_OCP#2
GPP_E12	I/O	Standby	3.3V	USB_OCP#3

GPIO	I/O/NC	Power	Tol	Usage
GPP_F14	I/O	Standby	3.3V	SKTOCC#_C
GPP_F15	I/O	Standby	3.3V	USB_OCP#4
GPP_F16	I/O	Standby	3.3V	USB_OCP#5
GPP_F17	I/O	Standby	3.3V	USB_OCP#6
GPP_F18	I/O	Standby	3.3V	USB_OCP#7
GPP_F22	I/O	Core	3.3V	PCH_GPIO_F22

GPIO	I/O/NC	Power	Tol	Usage
GPP_G0	BOM option	Standby	3.3V	GPP_G0
GPP_G1	BOM option	Standby	3.3V	GPP_G1
GPP_G2	BOM option	Standby	3.3V	GPP_G2
GPP_G3	BOM option	Standby	3.3V	GPP_G3
GPP_G4		Standby	3.3V	GPP_G4
GPP_G5		Standby	3.3V	GPP_G5
GPP_G22	I/O	Standby	3.3V	FM_BIOS_IMAGE_SWAP#

GPIO	I/O/NC	Power	Tol	Usage
GPP_H12	I/O	Standby	3.3V	FM_ESPI_FLASH_MODE
GPP_H15	I/O	Standby	3.3V	PCH_GPP_H15
GPP_H18	I/O	Standby	3.3V	PCH_GPP_H18
GPP_H20	I/O	Core	**3.3V**	CHASSIS_ID1
GPP_H21	I/O	Core	**3.3V**	CHASSIS_ID2
GPP_H23	I/O	Core	**3.3V**	CLR_CMOS

GPIO	I/O/NC	Power	Tol	Usage
GPP_I0	Pull Down	NA	NA	U2_AW4
GPP_I1	I/O	Standby	3.3V	HDMI_DDI1_HPD
GPP_I2	I/O	Standby	3.3V	VGA_DDI2_HPD
GPP_I3	Pull Down	Standby	3.3V	U2_BA4
GPP_I4	Pull Down	Standby	3.3V	U2_BD7
GPP_I5	I/O	Standby	3.3V	TP34
GPP_I6	I/O	Core	3.3V	DDPB_CTRLDATA
GPP_I7	I/O	Standby	3.3V	HDMI_DDI1_CTRLCLK
GPP_I8	I/O	Standby	3.3V	HDMI_DDI1_CTRLDATA
GPP_I9	I/O	Standby	3.3V	TP19
GPP_I10	I/O	Core	3.3V	DDPD_CTRLDATA

GPIO	I/O/NC	Power	Tol	Usage
GPD0	I/O	DSW	3.3V	PCH_BATLOW#
GPD1	I/O	DSW	3.3V	PCH_ACPRESENT
GPD2	I/O	DSW	3.3V	LAN_WAKE#_C
GPD3	I/O	DSW	3.3V	PWRBTN#
GPD4	I/O	Standby	3.3V	SLP_S3#
GPD5	I/O	Standby	3.3V	SLP_S4#
GPD11	I/O	DSW	3.3V	LAN_DISABLE#

SIO_GPIO(NCT6793D)

GP30	Stage	Input/Output	NOTE1	GP31	Stage	Input/Output	NOTE1	GP32	Stage	Input/Output	NOTE1
GP00	N/A	N/A	N/A	GP30	RSTSTC0##	Output	Pull high	GP60	KBR0	I/O	LPT signal
GP01	N/A	N/A	N/A	GP31	IO_SMBDATA	Output	Pull high	GP61	KBR1	I/O	LPT signal
GP02	N/A	N/A	N/A	GP32	IO_SMBCLK	Output	Pull high	GP62	KBR2	I/O	LPT signal
GP03	N/A	N/A	N/A	GP33	N/A	N/A	N/A	GP63	KBR3	I/O	LPT signal
GP04	N/A	N/A	N/A	GP34	PBITS0	Output	LPT signal	GP64	KBR4	I/O	LPT signal
GP05	N/A	N/A	N/A	GP35	PBAT#0	Output	LPT signal	GP65	KBR5	I/O	LPT signal
GP06	N/A	N/A	N/A	GP36	PBUSY#	Input	LPT signal	GP66	KBR6	I/O	LPT signal
GP07	N/A	N/A	N/A	GP40	SLP_IO_LCTR#	Input	Pin strap which disabled test mode	GP67	KBR7	I/O	LPT signal
GP10	KIN#	Input	Com port signal	GP41	PBIRST#	Output	LPT signal	GP70	SIOH_EN	Input	Pin strap which enable SIOH
GP11	PCIRS#	Input	Com port signal	GP42	LPT_ILIM#	Output	LPT signal	GP71	PROC_SELECT#_R	Input	PROC_SELECT
GP12	SOUT0	Output	Com port signal	GP43	PBACK#	Input	LPT signal	GP72	P12_DET0_R	Input	P12 Detect
GP13	SIN0	Input	Com port signal	GP44	PBUSY2	Input	LPT signal	GP73	KBR1_PCIE	Output	KBR1_PCIE signal
GP14	RTS0#	Output	Com port signal	GP45	PAPE	Input	LPT signal	GP74	PCIRST#1	Output	LPC Debug reset signal
GP15	RTS0#	Output	Com port signal	GP46	PSLCT	Input	LPT signal	GP75	PCIRST#2	Output	TPM reset signal
GP16	DCD0#	Input	Com port signal	GP47	N/A	N/A	N/A	GP76	PCIRST#3	Output	PCIE reset signal
GP17	CTS0#	Input	Com port signal	GP50	SPIWAIT##	Input	SIH signal	GP80	CTS1#	Input	COM port signal
GP30	KBDATA	Input	keyboard data in	GP51	SIO_SPIHOLD	Input	SIH signal	GP81	DCD1#	Input	COM port signal
GP31	KBCLK	Output	keyboard clock out	GP52	SPIACK##	Output	SIH signal	GP82	RTS1#	Output	COM port signal
GP32	MSDATA	Input	Mouse data in	GP53	N/A	N/A	N/A	GP83	RTS1#	Output	COM port signal
GP33	MSCLK	Output	Mouse clock out	GP54	SLP_SPIM_C	Input	SIH signal	GP84	SIN1	Input	COM port signal
GP34	SIO_WAKE#	Input	Wake up signal from LAN	GP55	SPIGS_CTRL#	Output	SIH signal	GP85	SOUT1	Output	COM port signal
GP35	ADSPWR_EN	Input	Pin strap which disabled ADS power sequence	GP56	N/A	N/A	N/A	GP86	DCD1#	Input	COM port signal
GP36	N/A	N/A	N/A	GP57	PWR_LED_R	Output	LED drive signal	GP87	RI1#	Input	COM port signal

DDR3L DIMM Config

DEVICE	ADDRESS(SA1:SA0)	CLOCK	
DIMM 1	00	MEM_MA_CLK_H0/L0	MEM_MA_CLK_H1/L1
DIMM 2	10	MEM_MB_CLK_H0/L0	MEM_MB_CLK_H1/L1

MICRO-STAR INT'L CO.,LTD.

GPIO Table

MS-7A05

0C change 1.0

Change VGA Chip IT6515 to IT6516

Add C826,C827,C828,C829,C830,C831,R872,R873,R874,R219,R232,R875,U30

Remove C221,C222,C198,C204,C205,C209,C215,C216,D11,Q41,R191,R221,R228,R186,R196,R187,R190,R193,U20,R198

Change F3,F4,F5,F6,Q5

MSI Link to the Future MICRO-START INT'L CO.,LTD.

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