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# Cars - Berlinetta X4
# Cars - Maranello X4
# Cars - Barchetta X3
uATX(244 mm X 244 mm)
# Cars - Enzo X4
uATX(220 mm X 195 mm)

CPU:
Intel Skylake Processor

System Chipset:
Intel Skylake PCH-H

OnBoard Chipset:
AZALIA Codec: Realtek ALC 221 VB3
LAN: Realtek RTL8111HSH-CG 10/100/1000 NIC
SIO: Nuvoton NPCD315H
DP to VGA: ITE IT6515
Flash ROM: 128 Mb

Main Memory:
DDRIII (1600MHz) * 2 (Dual Channel)

Expansion Slots:
PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 1

PWM:
Controller: IMVP8-NCP81203 5 Phase
Controller:NCP81161MNTBG

Other:
SATA *2
USB3.0 *4 (Rear*2 Front*2)
USB2.0 *5 (Rear*4 Internal*1)
DP PORT*1
VGA PORT *1
COM PORT *1

Marking	Description
I	Install
NI	Not Install
MP	Production Part ONLY
PROTO	Not For Production Part
CRITICAL	Critical Components

BOM DISTRIBUTION RULE
Enzo
(BOM)

BOARD REV	Development Phase	
0	DB-1	
1	DB-2	
2	DB-3	
3	SI-1	
4	SI-2	●
5	SI-3	
6	PV-1	
7	PV-2	

Project	
Berlinetta	
Maranello	
Barchetta	
Enzo	V

PCA P/N, BERLINETTA/MARANELLO/BARCHETTA/ENZO	793305-001/793305-002/793302-001/798930-001
SCH P/N, BERLINETTA/MARANELLO/BARCHETTA/ENZO	793306-000/793306-000/793303-000/798931-000
PCB P/N, BERLINETTA/MARANELLO/BARCHETTA/ENZO	793307-001/793307-001/793304-001/798932-001
SSID, BERLINETTA/MARANELLO/BARCHETTA/ENZO	805F/8061/8060/8062
Board ID, BERLINETTA/MARANELLO/BARCHETTA/ENZO	7/8/9/10

	Berlinetta	Maranello	Barchetta	Enzo
PCH	H170	H110	H110	H110

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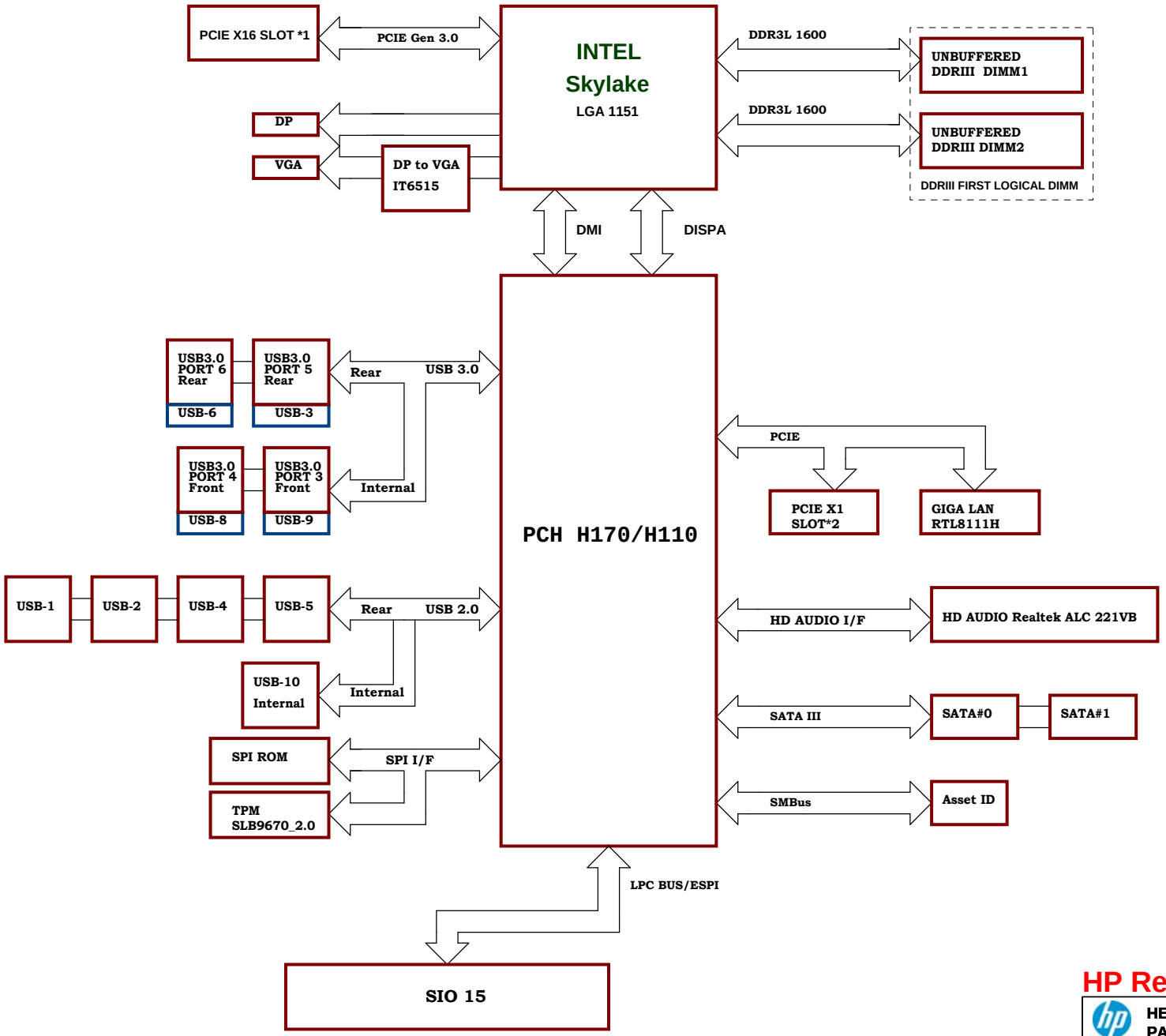
Date: Monday, July 06, 2015 | Sheet 1 of 63



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Berlinetta	
Maranello	
Barchetta	
Enzo	V

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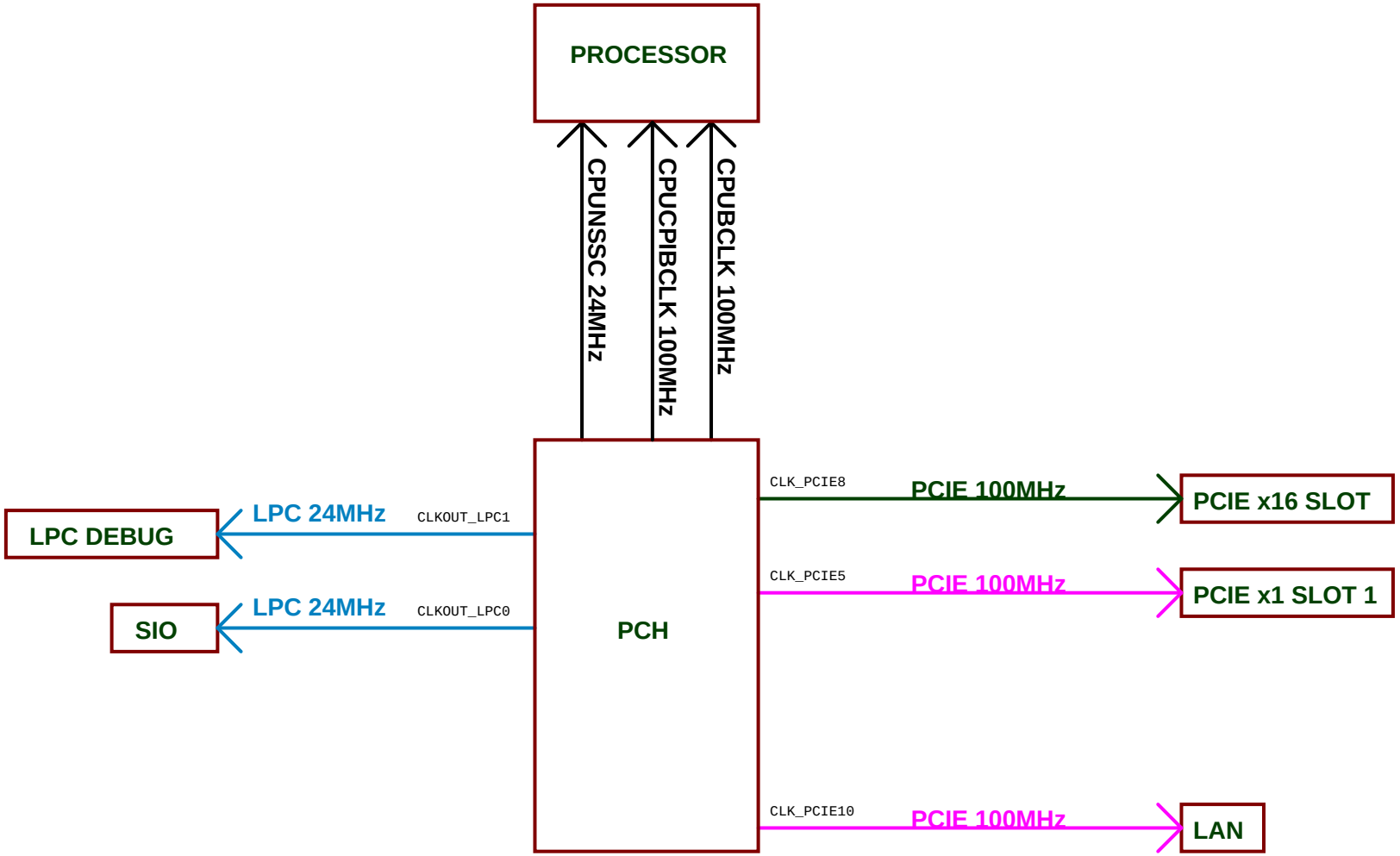

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Maranello	
Barchetta	
Enzo	V

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Title: **Clock Distribution**

Size	Document Number	Rev
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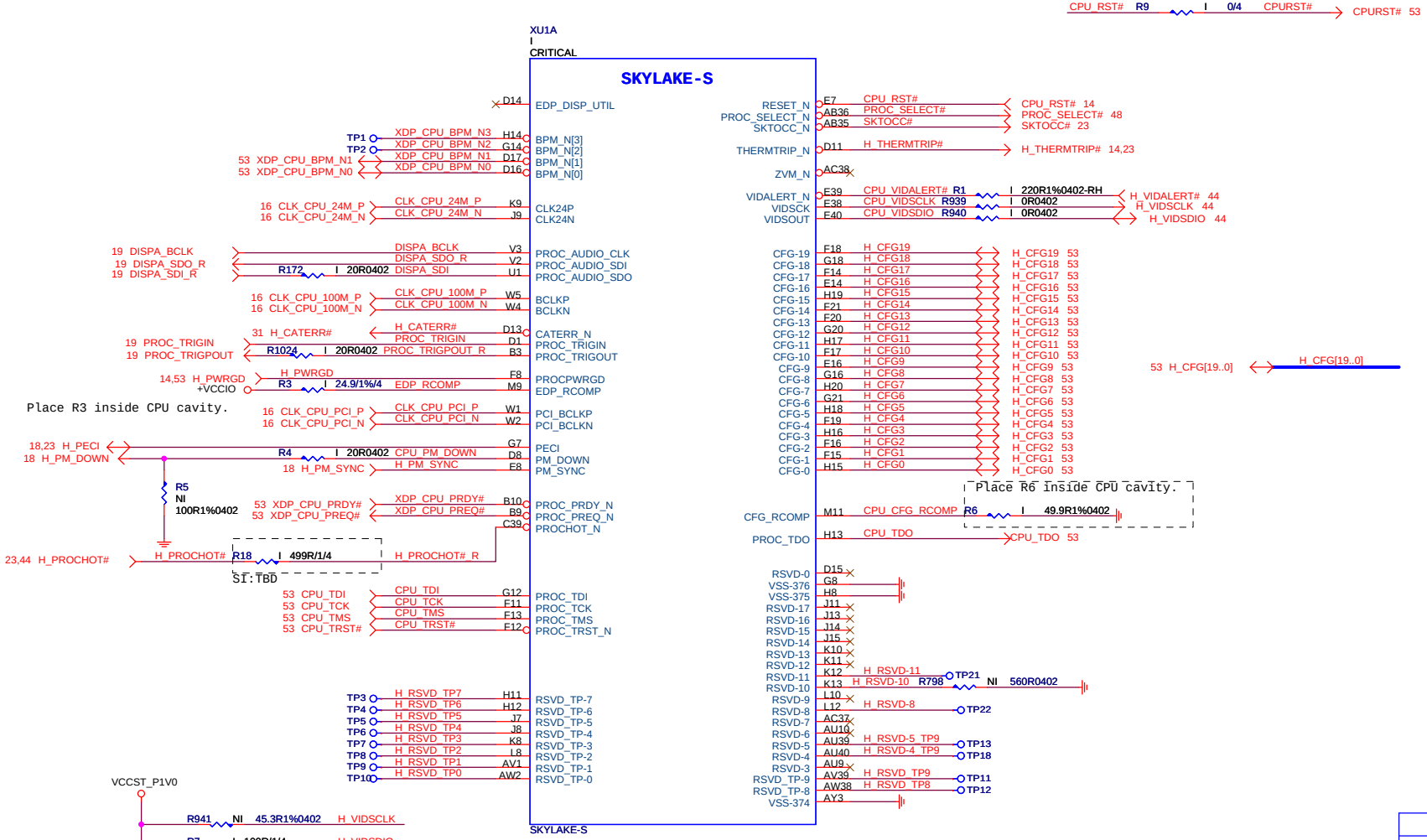

Project	
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Maranello	
Barchetta	
Enzo	V

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Title CPU-CLK/MISC/XDP

Size Custom | Document Number HP SCH P/N: 798931-000(MSI MS-7A02) | Rev X4

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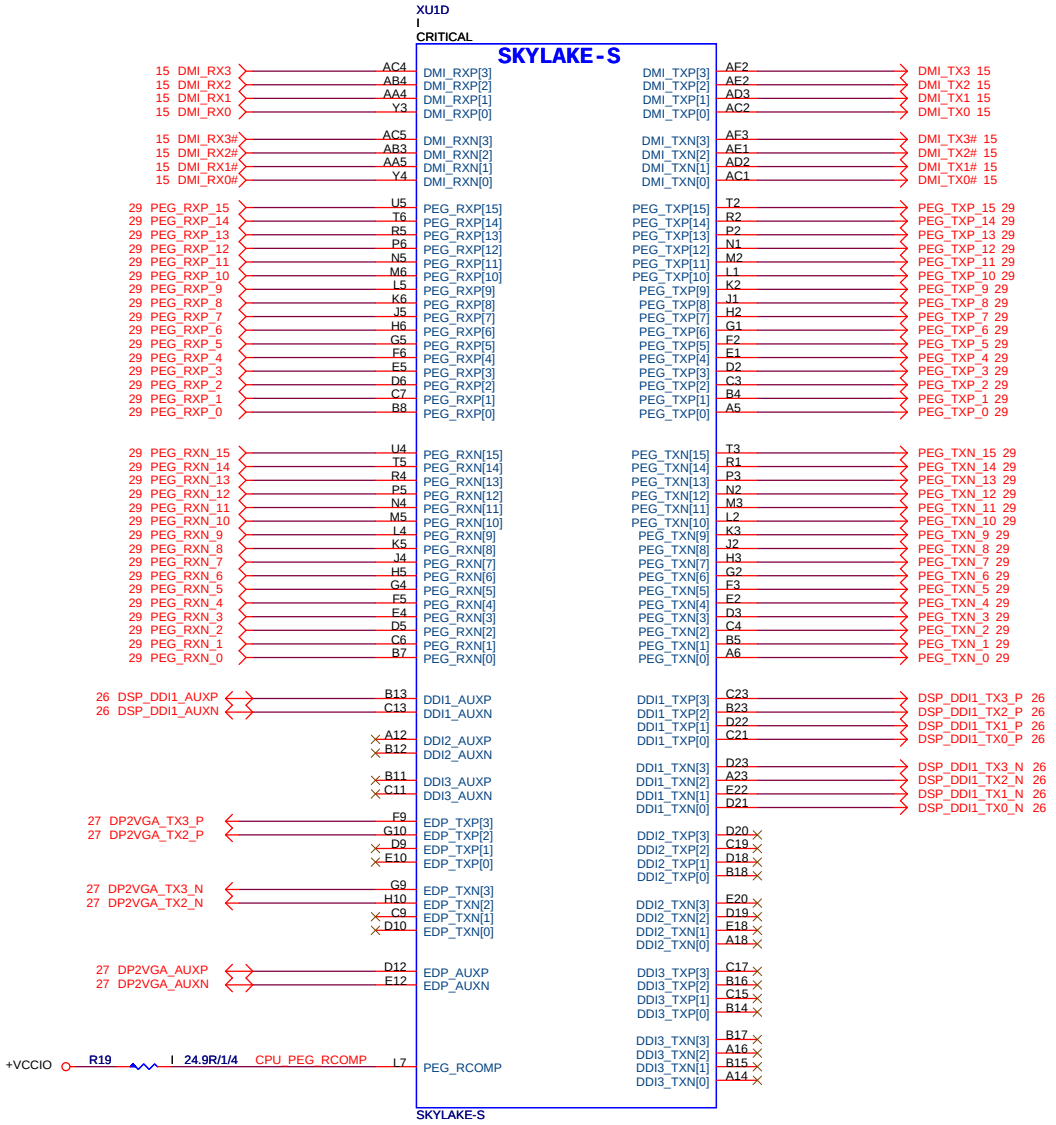

Project	
Berlinetta	
Maranello	
Barchetta	
Enzo	V

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Title: CPU-DMI/PEG/DDI

Size	Document Number	Rev
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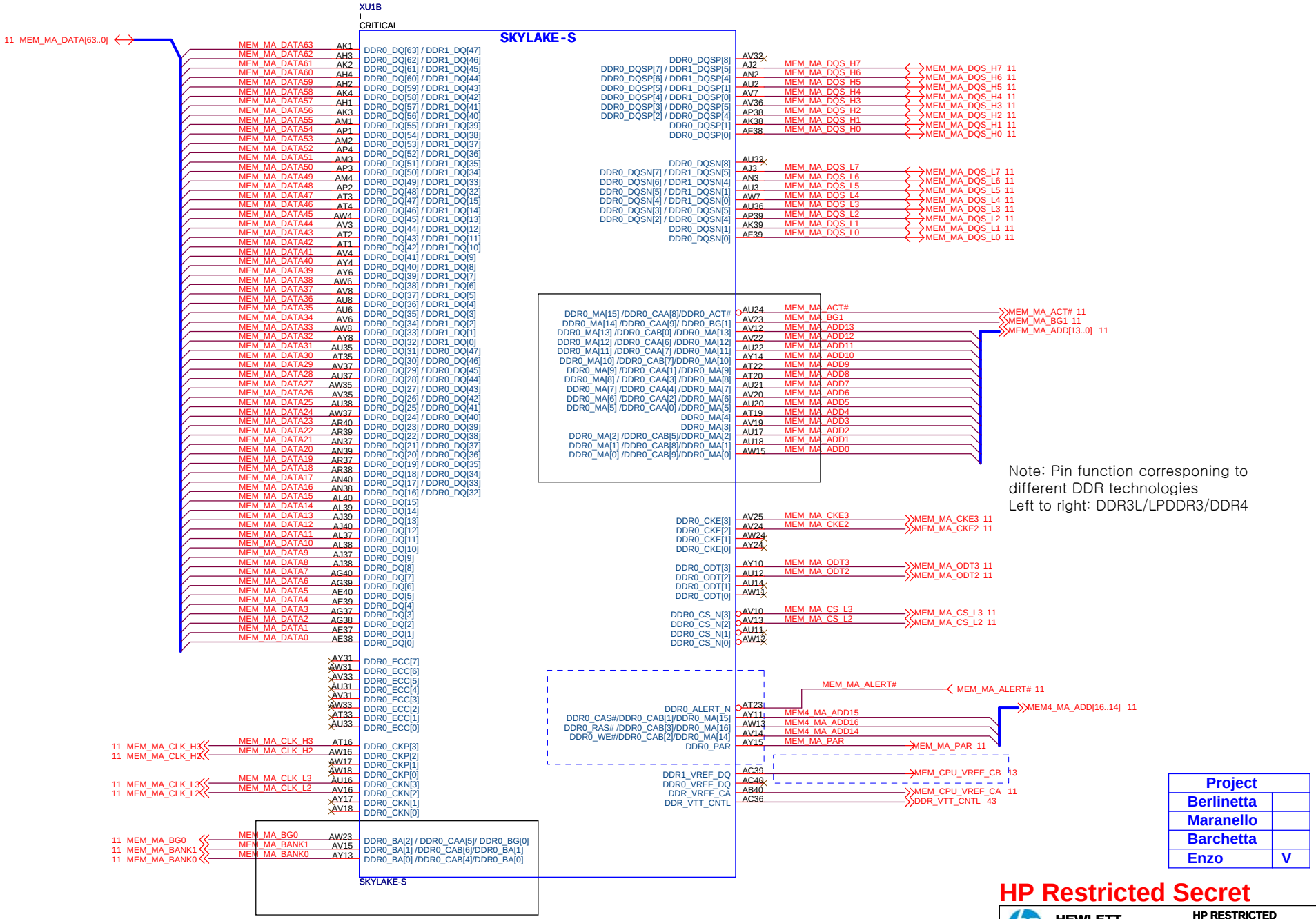
Date: Monday, July 06, 2015 Sheet 5 of 63


XU1B
CRITICAL
SKYLAKE-S
11 MEM_MA_DATA[63..0]
DDR0_DQ[63] / DDR1_DQ[47]
DDR0_DQ[62] / DDR1_DQ[46]
DDR0_DQ[61] / DDR1_DQ[45]
DDR0_DQ[60] / DDR1_DQ[44]
DDR0_DQ[59] / DDR1_DQ[43]
DDR0_DQ[58] / DDR1_DQ[42]
DDR0_DQ[57] / DDR1_DQ[41]
DDR0_DQ[56] / DDR1_DQ[40]
DDR0_DQ[55] / DDR1_DQ[39]
DDR0_DQ[54] / DDR1_DQ[38]
DDR0_DQ[53] / DDR1_DQ[37]
DDR0_DQ[52] / DDR1_DQ[36]
DDR0_DQ[51] / DDR1_DQ[35]
DDR0_DQ[50] / DDR1_DQ[34]
DDR0_DQ[49] / DDR1_DQ[33]
DDR0_DQ[48] / DDR1_DQ[32]
DDR0_DQ[47] / DDR1_DQ[15]
DDR0_DQ[46] / DDR1_DQ[14]
DDR0_DQ[45] / DDR1_DQ[13]
DDR0_DQ[44] / DDR1_DQ[12]
DDR0_DQ[43] / DDR1_DQ[11]
DDR0_DQ[42] / DDR1_DQ[10]
DDR0_DQ[41] / DDR1_DQ[9]
DDR0_DQ[40] / DDR1_DQ[8]
DDR0_DQ[39] / DDR1_DQ[7]
DDR0_DQ[38] / DDR1_DQ[6]
DDR0_DQ[37] / DDR1_DQ[5]
DDR0_DQ[36] / DDR1_DQ[4]
DDR0_DQ[35] / DDR1_DQ[3]
DDR0_DQ[34] / DDR1_DQ[2]
DDR0_DQ[33] / DDR1_DQ[1]
DDR0_DQ[32] / DDR1_DQ[0]
DDR0_DQ[31] / DDR0_DQ[47]
DDR0_DQ[30] / DDR0_DQ[46]
DDR0_DQ[29] / DDR0_DQ[45]
DDR0_DQ[28] / DDR0_DQ[44]
DDR0_DQ[27] / DDR0_DQ[43]
DDR0_DQ[26] / DDR0_DQ[42]
DDR0_DQ[25] / DDR0_DQ[41]
DDR0_DQ[24] / DDR0_DQ[40]
DDR0_DQ[23] / DDR0_DQ[39]
DDR0_DQ[22] / DDR0_DQ[38]
DDR0_DQ[21] / DDR0_DQ[37]
DDR0_DQ[20] / DDR0_DQ[36]
DDR0_DQ[19] / DDR0_DQ[35]
DDR0_DQ[18] / DDR0_DQ[34]
DDR0_DQ[17] / DDR0_DQ[33]
DDR0_DQ[16] / DDR0_DQ[32]
DDR0_DQ[15]
DDR0_DQ[14]
DDR0_DQ[13]
DDR0_DQ[12]
DDR0_DQ[11]
DDR0_DQ[10]
DDR0_DQ[9]
DDR0_DQ[8]
DDR0_DQ[7]
DDR0_DQ[6]
DDR0_DQ[5]
DDR0_DQ[4]
DDR0_DQ[3]
DDR0_DQ[2]
DDR0_DQ[1]
DDR0_DQ[0]
DDR0_ECC[7]
DDR0_ECC[6]
DDR0_ECC[5]
DDR0_ECC[4]
DDR0_ECC[3]
DDR0_ECC[2]
DDR0_ECC[1]
DDR0_ECC[0]
DDR0_CKP[3]
DDR0_CKP[2]
DDR0_CKP[1]
DDR0_CKP[0]
DDR0_CKN[3]
DDR0_CKN[2]
DDR0_CKN[1]
DDR0_CKN[0]
DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]
DDR0_BA[1] /DDR0_CAB[6]/DDR0_BA[1]
DDR0_BA[0] /DDR0_CAB[4]/DDR0_BA[0]
SKYLAKE-S
MEM_MA_DATA63 AK1
MEM_MA_DATA62 AH3
MEM_MA_DATA61 AK2
MEM_MA_DATA60 AH4
MEM_MA_DATA59 AH2
MEM_MA_DATA58 AK4
MEM_MA_DATA57 AH1
MEM_MA_DATA56 AK3
MEM_MA_DATA55 AM1
MEM_MA_DATA54 AP1
MEM_MA_DATA53 AM2
MEM_MA_DATA52 AP4
MEM_MA_DATA51 AM3
MEM_MA_DATA50 AP3
MEM_MA_DATA49 AM4
MEM_MA_DATA48 AP2
MEM_MA_DATA47 AT3
MEM_MA_DATA46 AT4
MEM_MA_DATA45 AW4
MEM_MA_DATA44 AV3
MEM_MA_DATA43 AT2
MEM_MA_DATA42 AT1
MEM_MA_DATA41 AV4
MEM_MA_DATA40 AY4
MEM_MA_DATA39 AY6
MEM_MA_DATA38 AW6
MEM_MA_DATA37 AV8
MEM_MA_DATA36 AU8
MEM_MA_DATA35 AU6
MEM_MA_DATA34 AV6
MEM_MA_DATA33 AW8
MEM_MA_DATA32 AY8
MEM_MA_DATA31 AU35
MEM_MA_DATA30 AT35
MEM_MA_DATA29 AV37
MEM_MA_DATA28 AU37
MEM_MA_DATA27 AW35
MEM_MA_DATA26 AV35
MEM_MA_DATA25 AU38
MEM_MA_DATA24 AW37
MEM_MA_DATA23 AR40
MEM_MA_DATA22 AR39
MEM_MA_DATA21 AN37
MEM_MA_DATA20 AN39
MEM_MA_DATA19 AR37
MEM_MA_DATA18 AR38
MEM_MA_DATA17 AN40
MEM_MA_DATA16 AN38
MEM_MA_DATA15 AL40
MEM_MA_DATA14 AL39
MEM_MA_DATA13 AJ39
MEM_MA_DATA12 AJ40
MEM_MA_DATA11 AL37
MEM_MA_DATA10 AL38
MEM_MA_DATA9 AJ37
MEM_MA_DATA8 AJ38
MEM_MA_DATA7 AG40
MEM_MA_DATA6 AG39
MEM_MA_DATA5 AE40
MEM_MA_DATA4 AE39
MEM_MA_DATA3 AG37
MEM_MA_DATA2 AG38
MEM_MA_DATA1 AE37
MEM_MA_DATA0 AE38
AY31
AW31
AV33
AU31
AV31
AW33
AT33
AU33
11 MEM_MA_CLK_H3
11 MEM_MA_CLK_H2
MEM_MA_CLK_H3 AT16
MEM_MA_CLK_H2 AW16
AW17
AW18
11 MEM_MA_CLK_L3
11 MEM_MA_CLK_L2
MEM_MA_CLK_L3 AU16
MEM_MA_CLK_L2 AV16
AY17
AV18
11 MEM_MA_BG0
11 MEM_MA_BANK1
11 MEM_MA_BANK0
MEM_MA_BG0 AW23
MEM_MA_BANK1 AV15
MEM_MA_BANK0 AY13
DDR0_DQSP[8] AV32
DDR0_DQSP[7] / DDR1_DQSP[5] AJ2
DDR0_DQSP[6] / DDR1_DQSP[4] AN2
DDR0_DQSP[5] / DDR1_DQSP[1] AU2
DDR0_DQSP[4] / DDR1_DQSP[0] AV7
DDR0_DQSP[3] / DDR0_DQSP[5] AV36
DDR0_DQSP[2] / DDR0_DQSP[4] AP38
DDR0_DQSP[1] AK38
DDR0_DQSP[0] AE38
MEM_MA_DQS_H7
MEM_MA_DQS_H6
MEM_MA_DQS_H5
MEM_MA_DQS_H4
MEM_MA_DQS_H3
MEM_MA_DQS_H2
MEM_MA_DQS_H1
MEM_MA_DQS_H0
MEM_MA_DQS_H7 11
MEM_MA_DQS_H6 11
MEM_MA_DQS_H5 11
MEM_MA_DQS_H4 11
MEM_MA_DQS_H3 11
MEM_MA_DQS_H2 11
MEM_MA_DQS_H1 11
MEM_MA_DQS_H0 11
DDR0_DQSN[8] AU32
DDR0_DQSN[7] / DDR1_DQSN[5] AJ3
DDR0_DQSN[6] / DDR1_DQSN[4] AN3
DDR0_DQSN[5] / DDR1_DQSN[1] AU3
DDR0_DQSN[4] / DDR1_DQSN[0] AW7
DDR0_DQSN[3] / DDR0_DQSN[5] AU36
DDR0_DQSN[2] / DDR0_DQSN[4] AP39
DDR0_DQSN[1] AK39
DDR0_DQSN[0] AF39
MEM_MA_DQS_L7
MEM_MA_DQS_L6
MEM_MA_DQS_L5
MEM_MA_DQS_L4
MEM_MA_DQS_L3
MEM_MA_DQS_L2
MEM_MA_DQS_L1
MEM_MA_DQS_L0
MEM_MA_DQS_L7 11
MEM_MA_DQS_L6 11
MEM_MA_DQS_L5 11
MEM_MA_DQS_L4 11
MEM_MA_DQS_L3 11
MEM_MA_DQS_L2 11
MEM_MA_DQS_L1 11
MEM_MA_DQS_L0 11
DDR0_MA[15] /DDR0_CAA[8]/DDR0_ACT# AU24
DDR0_MA[14] /DDR0_CAA[9]/ DDR0_BG[1] AV23
DDR0_MA[13] /DDR0_CAB[0] /DDR0_MA[13] AV12
DDR0_MA[12] /DDR0_CAA[6] /DDR0_MA[12] AV22
DDR0_MA[11] /DDR0_CAA[7] /DDR0_MA[11] AU22
DDR0_MA[10] /DDR0_CAB[7]/DDR0_MA[10] AY14
DDR0_MA[9] /DDR0_CAA[1] /DDR0_MA[9] AT22
DDR0_MA[8] / DDR0_CAA[3] /DDR0_MA[8] AT20
DDR0_MA[7] /DDR0_CAA[4] /DDR0_MA[7] AU21
DDR0_MA[6] /DDR0_CAA[2] /DDR0_MA[6] AV20
DDR0_MA[5] /DDR0_CAA[0] /DDR0_MA[5] AU20
DDR0_MA[4] AT19
DDR0_MA[3] AV19
DDR0_MA[2] /DDR0_CAB[5]/DDR0_MA[2] AU17
DDR0_MA[1] /DDR0_CAB[8]/DDR0_MA[1] AU18
DDR0_MA[0] /DDR0_CAB[9]/DDR0_MA[0] AW15
MEM_MA_ACT#
MEM_MA_BG1
MEM_MA_ADD13
MEM_MA_ADD12
MEM_MA_ADD11
MEM_MA_ADD10
MEM_MA_ADD9
MEM_MA_ADD8
MEM_MA_ADD7
MEM_MA_ADD6
MEM_MA_ADD5
MEM_MA_ADD4
MEM_MA_ADD3
MEM_MA_ADD2
MEM_MA_ADD1
MEM_MA_ADD0
MEM_MA_ACT# 11
MEM_MA_BG1 11
MEM_MA_ADD[13..0] 11
DDR0_CKE[3] AV25
DDR0_CKE[2] AV24
DDR0_CKE[1] AW24
DDR0_CKE[0] AY24
MEM_MA_CKE3
MEM_MA_CKE2
MEM_MA_CKE3 11
MEM_MA_CKE2 11
DDR0_ODT[3] AY10
DDR0_ODT[2] AU12
DDR0_ODT[1] AU14
DDR0_ODT[0] AW11
MEM_MA_ODT3
MEM_MA_ODT2
MEM_MA_ODT3 11
MEM_MA_ODT2 11
DDR0_CS_N[3] AV10
DDR0_CS_N[2] AV13
DDR0_CS_N[1] AU11
DDR0_CS_N[0] AW12
MEM_MA_CS_L3
MEM_MA_CS_L2
MEM_MA_CS_L3 11
MEM_MA_CS_L2 11
MEM_MA_ALERT#
MEM_MA_ALERT# 11
DDR0_ALERT_N AT23
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AY11
DDR0_RAS# /DDR0_CAB[3]/DDR0_MA[16] AW13
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AV14
DDR0_PAR AY15
MEM4_MA_ADD15
MEM4_MA_ADD16
MEM4_MA_ADD14
MEM_MA_PAR
MEM_MA_PAR 11
MEM4_MA_ADD[16..14] 11
DDR1_VREF_DQ AC39
DDR0_VREF_DQ AC40
DDR_VREF_CA AB40
DDR_VTT_CNTL AC36
MEM_CPU_VREF_CB 13
MEM_CPU_VREF_CA 11
DDR_VTT_CNTL 43
Note: Pin function corresponing to
different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4
Note: Pin function corresponing to
different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4
Project
Berlinetta
Maranello
Barchetta
Enzo V
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Title
CPU-Memory-Channel A
Size Custom
Document Number
HP SCH P/N: 798931-000(MSI MS-7A02)
Rev X4
Date: Monday, July 06, 2015
Sheet 6 of 63

XU1C
I
CRITICAL

SKYLAKE-S

13 MEM_MB_DATA[63..0]

MEM_MB_DATA63	AF6	DDR1_DQ[63]
MEM_MB_DATA62	AE7	DDR1_DQ[62]
MEM_MB_DATA61	AH6	DDR1_DQ[61]
MEM_MB_DATA60	AH7	DDR1_DQ[60]
MEM_MB_DATA59	AE7	DDR1_DQ[59]
MEM_MB_DATA58	AE6	DDR1_DQ[58]
MEM_MB_DATA57	AJ7	DDR1_DQ[57]
MEM_MB_DATA56	AJ6	DDR1_DQ[56]
MEM_MB_DATA55	AL6	DDR1_DQ[55]
MEM_MB_DATA54	AM6	DDR1_DQ[54]
MEM_MB_DATA53	AL9	DDR1_DQ[53]
MEM_MB_DATA52	AM9	DDR1_DQ[52]
MEM_MB_DATA51	AL7	DDR1_DQ[51]
MEM_MB_DATA50	AM7	DDR1_DQ[50]
MEM_MB_DATA49	AL10	DDR1_DQ[49]
MEM_MB_DATA48	AM10	DDR1_DQ[48]
MEM_MB_DATA47	AP6	DDR1_DQ[47] / DDR1_DQ[31]
MEM_MB_DATA46	AR6	DDR1_DQ[46] / DDR1_DQ[30]
MEM_MB_DATA45	AP9	DDR1_DQ[45] / DDR1_DQ[29]
MEM_MB_DATA44	AR9	DDR1_DQ[44] / DDR1_DQ[28]
MEM_MB_DATA43	AP7	DDR1_DQ[43] / DDR1_DQ[27]
MEM_MB_DATA42	AR7	DDR1_DQ[42] / DDR1_DQ[26]
MEM_MB_DATA41	AR10	DDR1_DQ[41] / DDR1_DQ[25]
MEM_MB_DATA40	AP10	DDR1_DQ[40] / DDR1_DQ[24]
MEM_MB_DATA39	AL12	DDR1_DQ[39] / DDR1_DQ[23]
MEM_MB_DATA38	AM12	DDR1_DQ[38] / DDR1_DQ[22]
MEM_MB_DATA37	AP13	DDR1_DQ[37] / DDR1_DQ[21]
MEM_MB_DATA36	AR13	DDR1_DQ[36] / DDR1_DQ[20]
MEM_MB_DATA35	AL13	DDR1_DQ[35] / DDR1_DQ[19]
MEM_MB_DATA34	AM13	DDR1_DQ[34] / DDR1_DQ[18]
MEM_MB_DATA33	AP12	DDR1_DQ[33] / DDR1_DQ[17]
MEM_MB_DATA32	AR12	DDR1_DQ[32] / DDR1_DQ[16]
MEM_MB_DATA31	AP28	DDR1_DQ[31] / DDR0_DQ[63]
MEM_MB_DATA30	AR28	DDR1_DQ[30] / DDR0_DQ[62]
MEM_MB_DATA29	AL28	DDR1_DQ[29] / DDR0_DQ[61]
MEM_MB_DATA28	AM28	DDR1_DQ[28] / DDR0_DQ[60]
MEM_MB_DATA27	AR29	DDR1_DQ[27] / DDR0_DQ[59]
MEM_MB_DATA26	AP29	DDR1_DQ[26] / DDR0_DQ[58]
MEM_MB_DATA25	AM29	DDR1_DQ[25] / DDR0_DQ[57]
MEM_MB_DATA24	AL29	DDR1_DQ[24] / DDR0_DQ[56]
MEM_MB_DATA23	AP31	DDR1_DQ[23] / DDR0_DQ[55]
MEM_MB_DATA22	AN31	DDR1_DQ[22] / DDR0_DQ[54]
MEM_MB_DATA21	AP34	DDR1_DQ[21] / DDR0_DQ[53]
MEM_MB_DATA20	AN34	DDR1_DQ[20] / DDR0_DQ[52]
MEM_MB_DATA19	AP32	DDR1_DQ[19] / DDR0_DQ[51]
MEM_MB_DATA18	AN32	DDR1_DQ[18] / DDR0_DQ[50]
MEM_MB_DATA17	AN35	DDR1_DQ[17] / DDR0_DQ[49]
MEM_MB_DATA16	AP35	DDR1_DQ[16] / DDR0_DQ[48]
MEM_MB_DATA15	AL31	DDR1_DQ[15] / DDR0_DQ[31]
MEM_MB_DATA14	AK31	DDR1_DQ[14] / DDR0_DQ[30]
MEM_MB_DATA13	AL34	DDR1_DQ[13] / DDR0_DQ[29]
MEM_MB_DATA12	AK34	DDR1_DQ[12] / DDR0_DQ[28]
MEM_MB_DATA11	AL32	DDR1_DQ[11] / DDR0_DQ[27]
MEM_MB_DATA10	AK32	DDR1_DQ[10] / DDR0_DQ[26]
MEM_MB_DATA9	AL35	DDR1_DQ[9] / DDR0_DQ[25]
MEM_MB_DATA8	AK35	DDR1_DQ[8] / DDR0_DQ[24]
MEM_MB_DATA7	AH34	DDR1_DQ[7] / DDR0_DQ[23]
MEM_MB_DATA6	AG34	DDR1_DQ[6] / DDR0_DQ[22]
MEM_MB_DATA5	AE34	DDR1_DQ[5] / DDR0_DQ[21]
MEM_MB_DATA4	AE35	DDR1_DQ[4] / DDR0_DQ[20]
MEM_MB_DATA3	AH35	DDR1_DQ[3] / DDR0_DQ[19]
MEM_MB_DATA2	AG35	DDR1_DQ[2] / DDR0_DQ[18]
MEM_MB_DATA1	AD35	DDR1_DQ[1] / DDR0_DQ[17]
MEM_MB_DATA0	AD34	DDR1_DQ[0] / DDR0_DQ[16]

	AL26	DDR1_ECC[7]
	AL25	DDR1_ECC[6]
	AP25	DDR1_ECC[5]
	AP26	DDR1_ECC[4]
	AM25	DDR1_ECC[3]
	AM26	DDR1_ECC[2]
	AR26	DDR1_ECC[1]
	AR25	DDR1_ECC[0]

13 MEM_MB_CLK_H3	MEM_MB_CLK_H3	AP19	DDR1_CKP[3]
13 MEM_MB_CLK_H2	MEM_MB_CLK_H2	AN20	DDR1_CKP[2]
		AP22	DDR1_CKP[1]
		AM20	DDR1_CKP[0]
13 MEM_MB_CLK_L3	MEM_MB_CLK_L3	AP20	DDR1_CKN[3]
13 MEM_MB_CLK_L2	MEM_MB_CLK_L2	AN21	DDR1_CKN[2]
		AP21	DDR1_CKN[1]
		AM21	DDR1_CKN[0]

13 MEM_MB_BG0	MEM_MB_BG0	AW28	DDR1_BA[2] / DDR1_CAA[5]/ DDR1_BG[0]
13 MEM_MB_BANK1	MEM_MB_BANK1	AM18	DDR1_BA[1] /DDR1_CAB[6]/DDR1_BA[1]
13 MEM_MB_BANK0	MEM_MB_BANK0	AL18	DDR1_BA[0] /DDR1_CAB[4]/DDR1_BA[0]

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Note: Pin function corresponing to different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

DDR1_DQSP[8]	AN25		
DDR1_DQSP[7]	AG7	MEM_MB_DQS_H7	MEM_MB_DQS_H7 13
DDR1_DQSP[6]	AL8	MEM_MB_DQS_H6	MEM_MB_DQS_H6 13
DDR1_DQSP[5] / DDR1_DQSP[3]	AP8	MEM_MB_DQS_H5	MEM_MB_DQS_H5 13
DDR1_DQSP[4] / DDR1_DQSP[2]	AN12	MEM_MB_DQS_H4	MEM_MB_DQS_H4 13
DDR1_DQSP[3] / DDR0_DQSP[7]	AN28	MEM_MB_DQS_H3	MEM_MB_DQS_H3 13
DDR1_DQSP[2] / DDR0_DQSP[6]	AP33	MEM_MB_DQS_H2	MEM_MB_DQS_H2 13
DDR1_DQSP[1] / DDR0_DQSP[3]	AL33	MEM_MB_DQS_H1	MEM_MB_DQS_H1 13
DDR1_DQSP[0] / DDR0_DQSP[2]	AF35	MEM_MB_DQS_H0	MEM_MB_DQS_H0 13
	AN26		
DDR1_DQSN[8]	AG6	MEM_MB_DQS_L7	MEM_MB_DQS_L7 13
DDR1_DQSN[7]	AM8	MEM_MB_DQS_L6	MEM_MB_DQS_L6 13
DDR1_DQSN[6]	AR8	MEM_MB_DQS_L5	MEM_MB_DQS_L5 13
DDR1_DQSN[5] / DDR1_DQSN[3]	AN13	MEM_MB_DQS_L4	MEM_MB_DQS_L4 13
DDR1_DQSN[4] / DDR1_DQSN[2]	AN29	MEM_MB_DQS_L3	MEM_MB_DQS_L3 13
DDR1_DQSN[3] / DDR0_DQSN[7]	AN33	MEM_MB_DQS_L2	MEM_MB_DQS_L2 13
DDR1_DQSN[2] / DDR0_DQSN[6]	AK33	MEM_MB_DQS_L1	MEM_MB_DQS_L1 13
DDR1_DQSN[1] / DDR0_DQSN[3]	AF34	MEM_MB_DQS_L0	MEM_MB_DQS_L0 13
DDR1_DQSN[0] / DDR0_DQSN[2]			

Note: Pin function corresponing to different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

DDR1_MA[15] /DDR1_CAA[8]/DDR1_ACT#	AU28	MEM_MB_ACT#	MEM_MB_ACT# 13
DDR1_MA[14] /DDR1_CAA[9]/ DDR1_BG[1]	AY28	MEM_MB_BG1	MEM_MB_BG1 13
DDR1_MA[13] /DDR1_CAB[0] /DDR1_MA[13]	AR15	MEM_MB_ADD13	MEM_MB_ADD[13..0] 13
DDR1_MA[12] /DDR1_CAA[6] /DDR1_MA[12]	AV27	MEM_MB_ADD12	
DDR1_MA[11] /DDR1_CAA[7] /DDR1_MA[11]	AU27	MEM_MB_ADD11	
DDR1_MA[10] /DDR1_CAB[7]/DDR1_MA[10]	AP18	MEM_MB_ADD10	
DDR1_MA[9] /DDR1_CAA[1] /DDR1_MA[9]	AW27	MEM_MB_ADD9	
DDR1_MA[8] / DDR1_CAA[3] /DDR1_MA[8]	AU26	MEM_MB_ADD8	
DDR1_MA[7] /DDR1_CAA[4] /DDR1_MA[7]	AY26	MEM_MB_ADD7	
DDR1_MA[6] /DDR1_CAA[2] /DDR1_MA[6]	AW26	MEM_MB_ADD6	
DDR1_MA[5] /DDR1_CAA[0] /DDR1_MA[5]	AL23	MEM_MB_ADD5	
DDR1_MA[4]	AP23	MEM_MB_ADD4	
DDR1_MA[3]	AM23	MEM_MB_ADD3	
DDR1_MA[2] /DDR1_CAB[5]/DDR1_MA[2]	AM22	MEM_MB_ADD2	
DDR1_MA[1] /DDR1_CAB[8]/DDR1_MA[1]	AL22	MEM_MB_ADD1	
DDR1_MA[0] /DDR1_CAB[9]/DDR1_MA[0]	AL19	MEM_MB_ADD0	

DDR1_CKE[3]	AU29	MEM_MB_CKE3	MEM_MB_CKE3 13
DDR1_CKE[2]	AW29	MEM_MB_CKE2	MEM_MB_CKE2 13
DDR1_CKE[1]	AV29		
DDR1_CKE[0]	AY29		
DDR1_ODT[3]	AL15	MEM_MB_ODT3	MEM_MB_ODT3 13
DDR1_ODT[2]	AP15	MEM_MB_ODT2	MEM_MB_ODT2 13
DDR1_ODT[1]	AL16		
DDR1_ODT[0]	AM16		
DDR1_CS_N[3]	AM15	MEM_MB_CS_L3	MEM_MB_CS_L3 13
DDR1_CS_N[2]	AN17	MEM_MB_CS_L2	MEM_MB_CS_L2 13
DDR1_CS_N[1]	AN15		
DDR1_CS_N[0]	AP17		
		MEM_MB_ALERT#	MEM_MB_ALERT# 13
DDR1_ALERT_N	AY25		
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AP16	MEM4_MB_ADD15	MEM4_MB_ADD[16..14] 13
DDR1_RAS# /DDR1_CAB[3]/DDR1_MA[16]	AN18	MEM4_MB_ADD16	
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AL17	MEM4_MB_ADD14	
DDR1_PAR	AL20	MEM_MB_PAR	MEM_MB_PAR 13

Note: Pin function corresponing to different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

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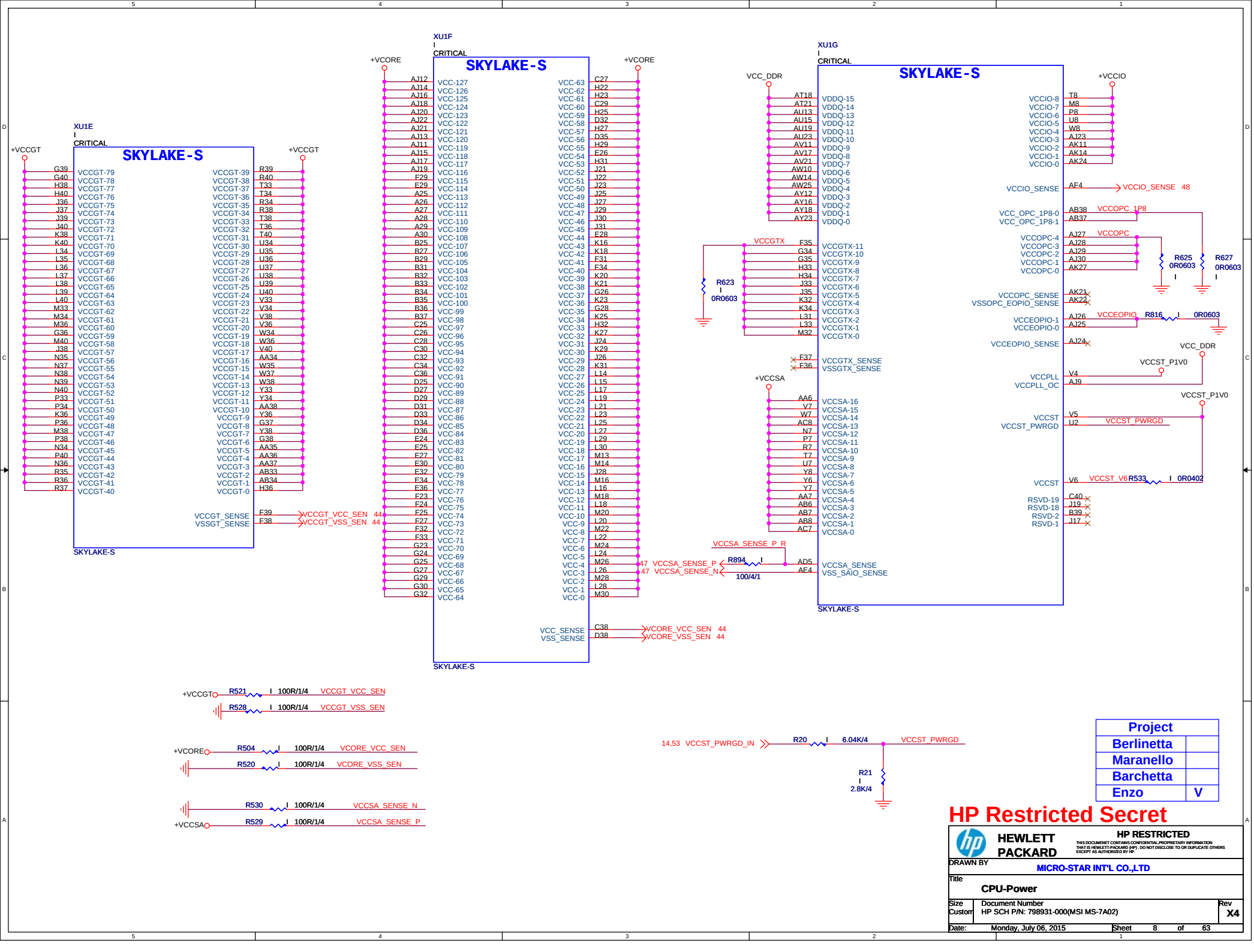
Rev	X4
Date: Monday, July 06, 2015	Sheet 7 of 63



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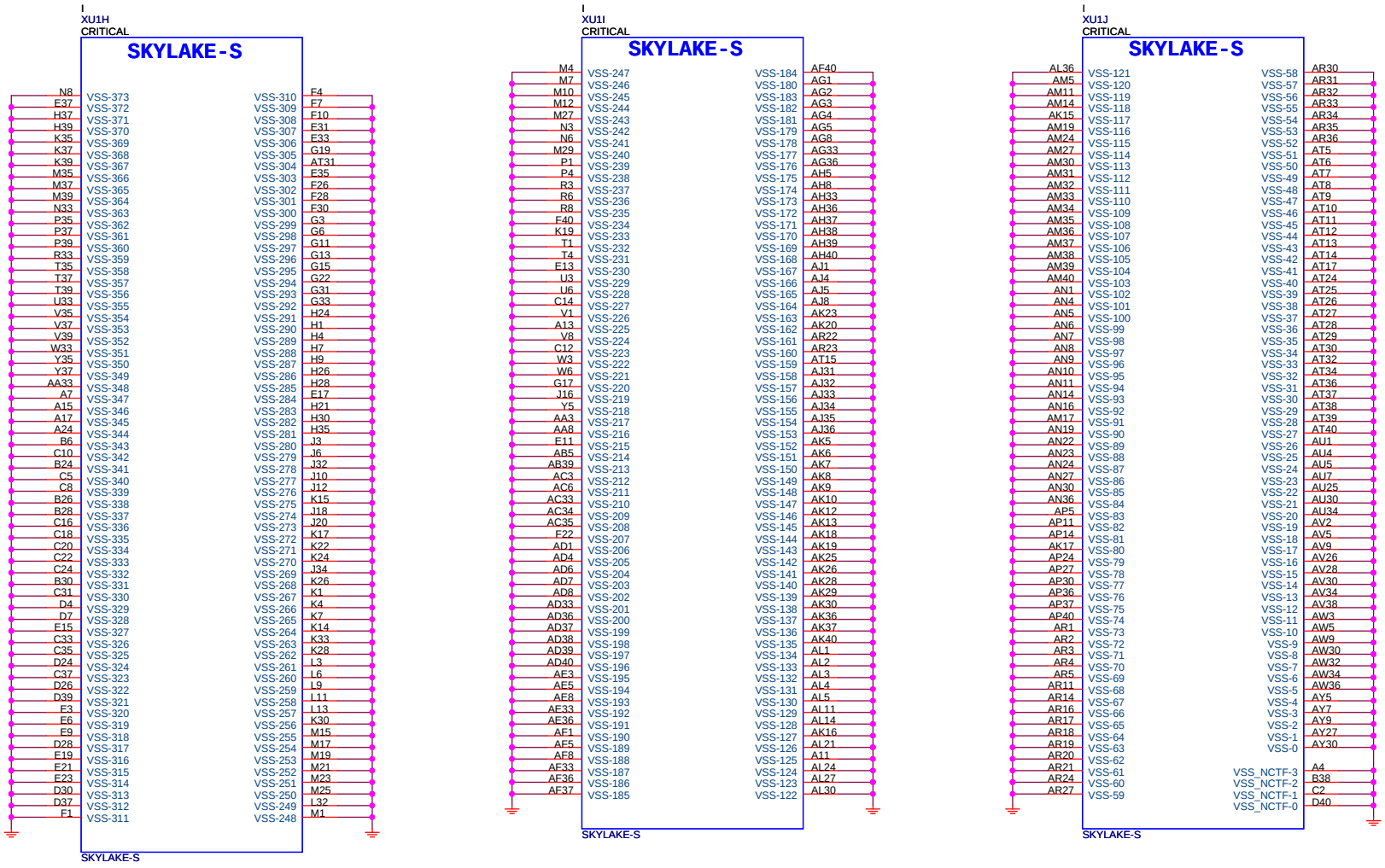

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Title
DDR III XMM4

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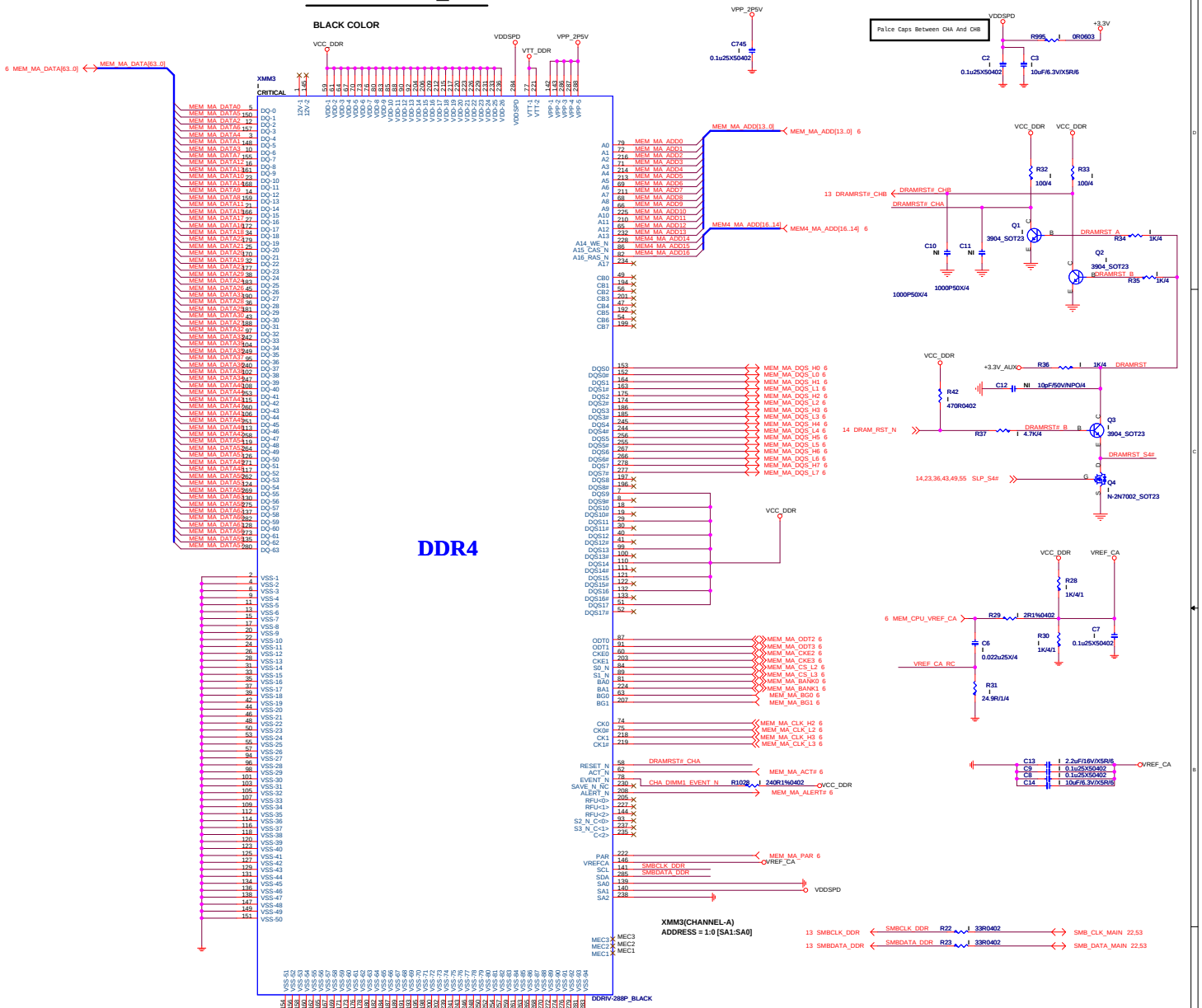
DDR4 DIMM_A2

BLACK COLOR



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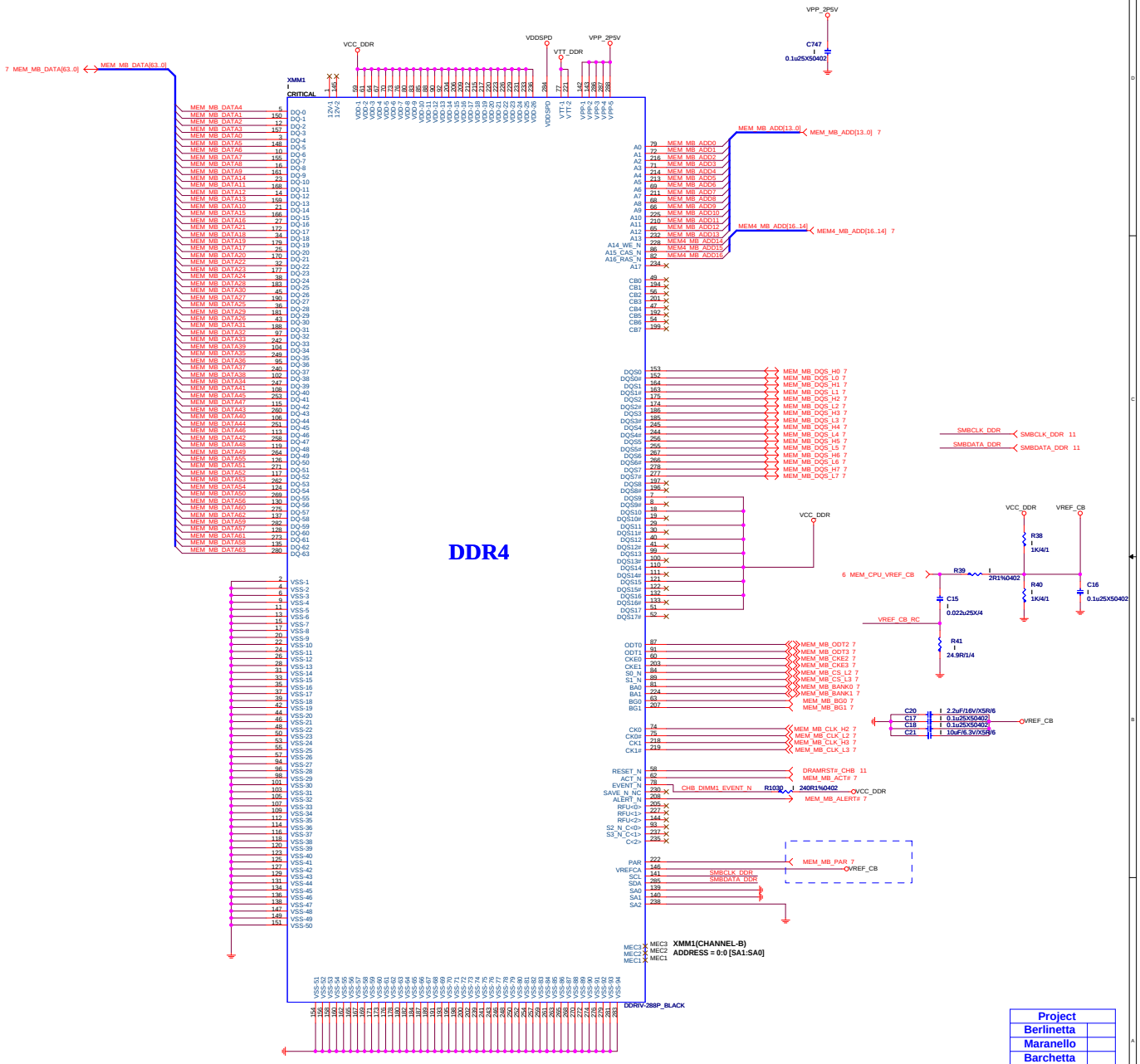
DDR4 DIMM_B2

BLACK COLOR



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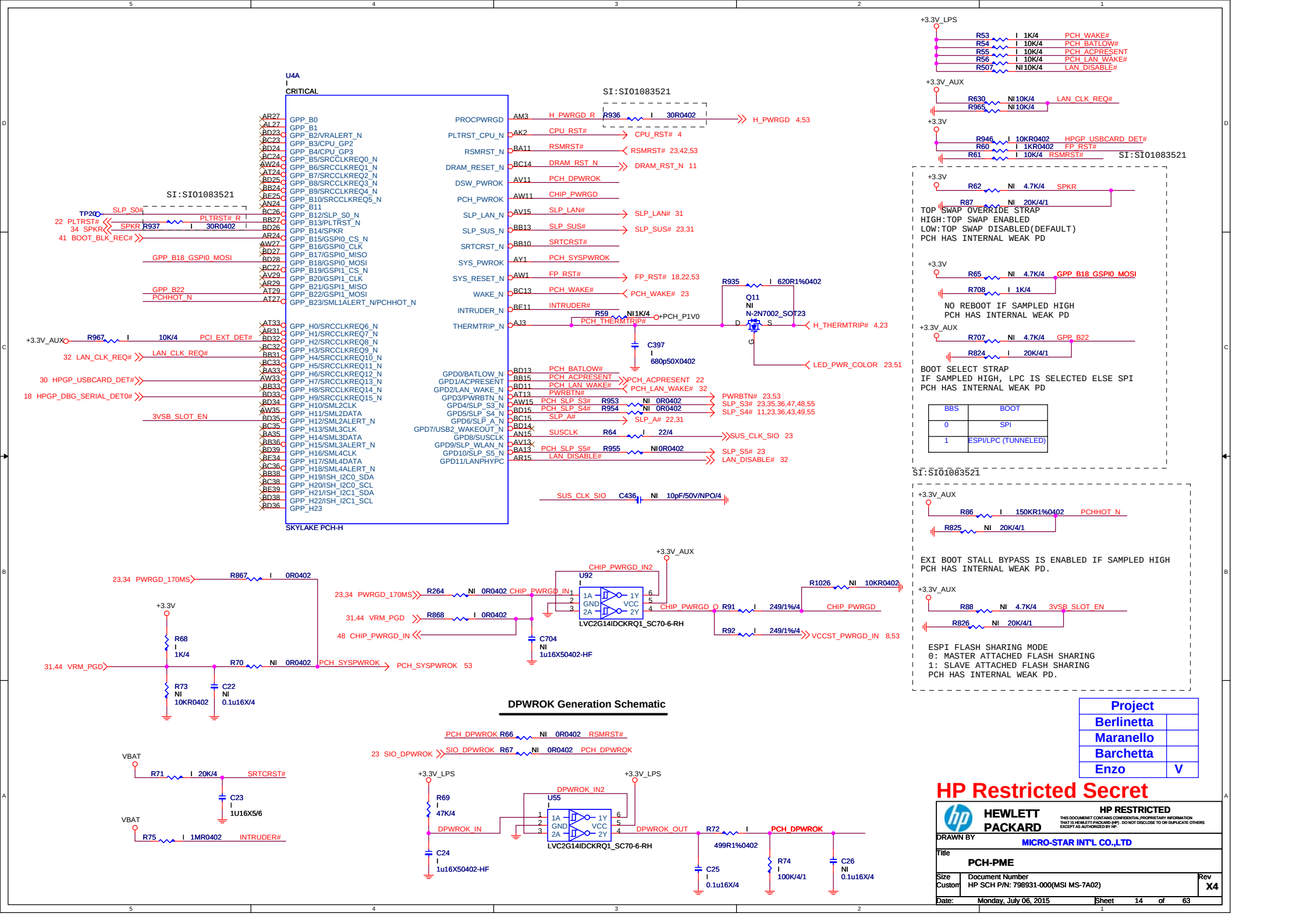

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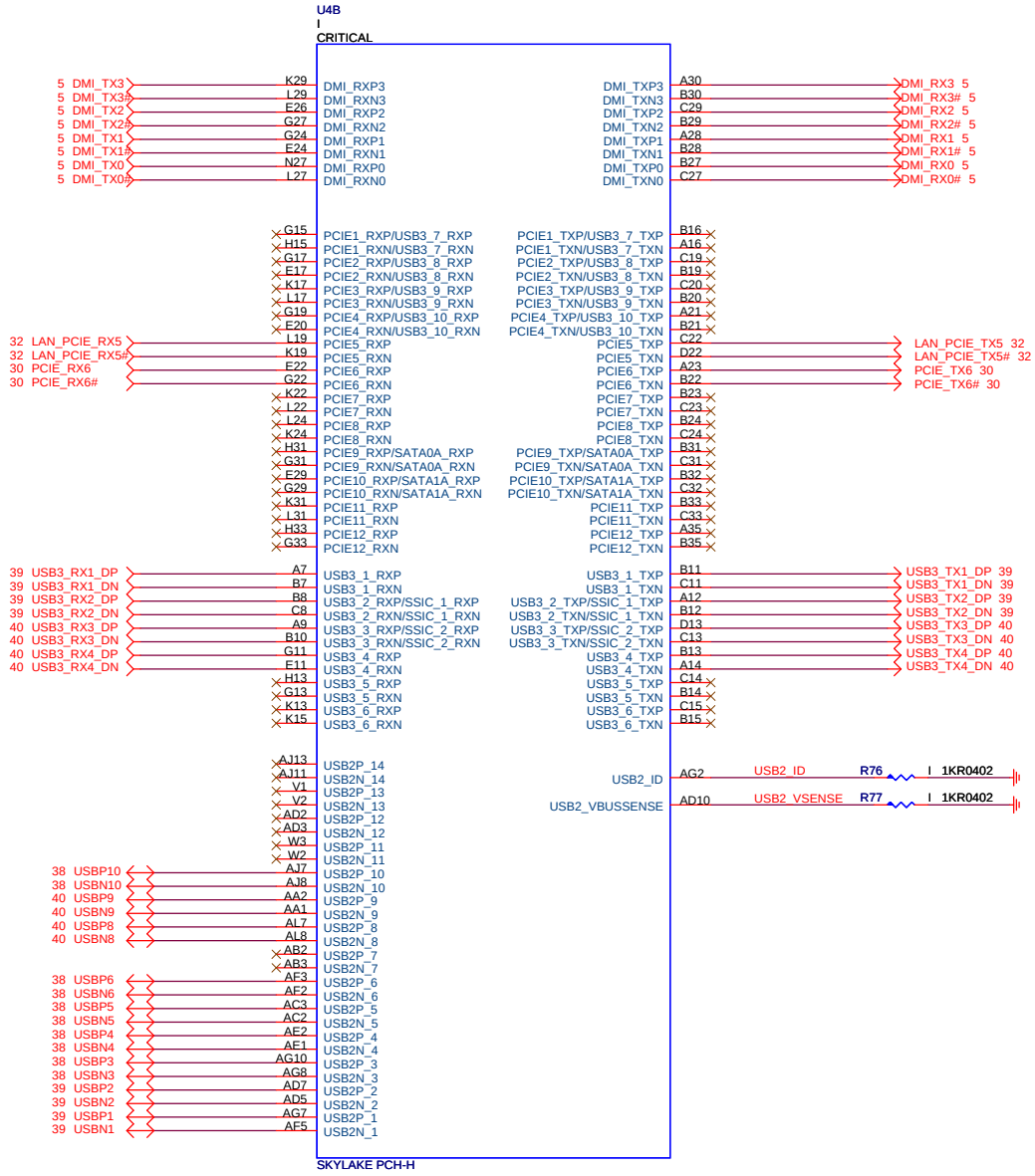

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Title: PCH-DMI/PCIE/USB

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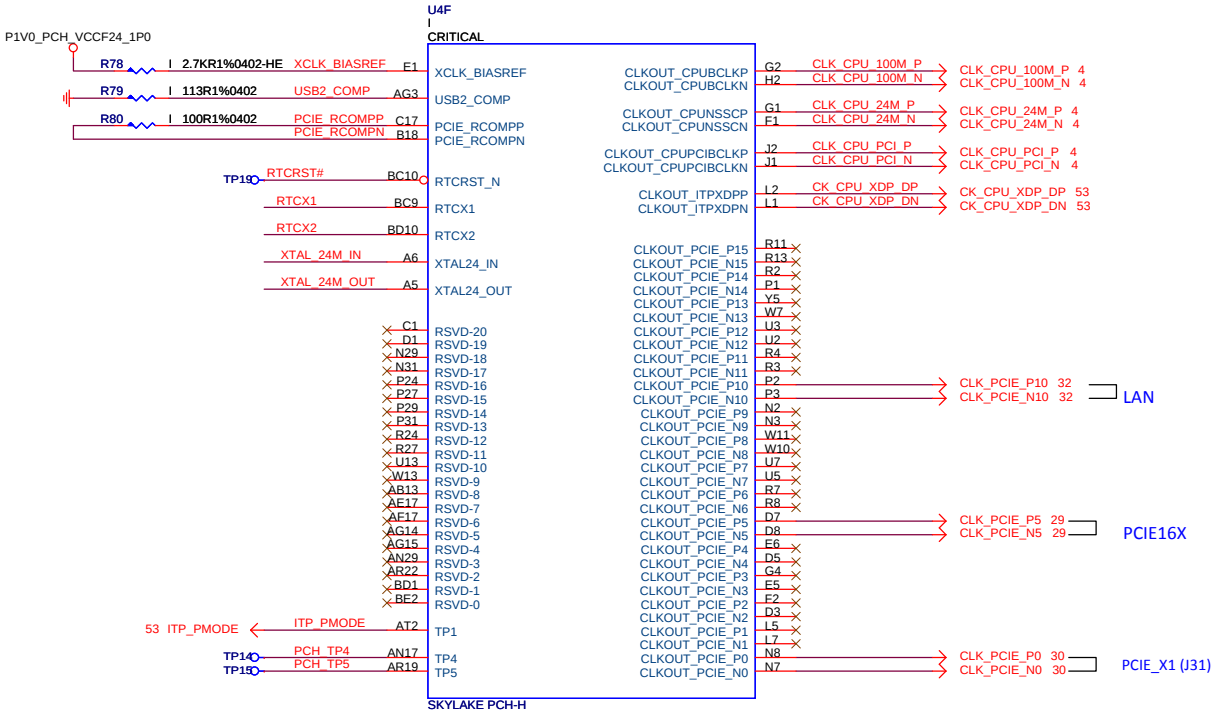
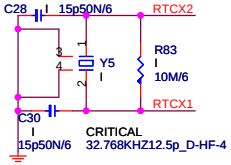
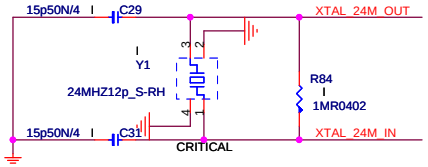
Date: Monday, July 06, 2015 Sheet 15 of 63

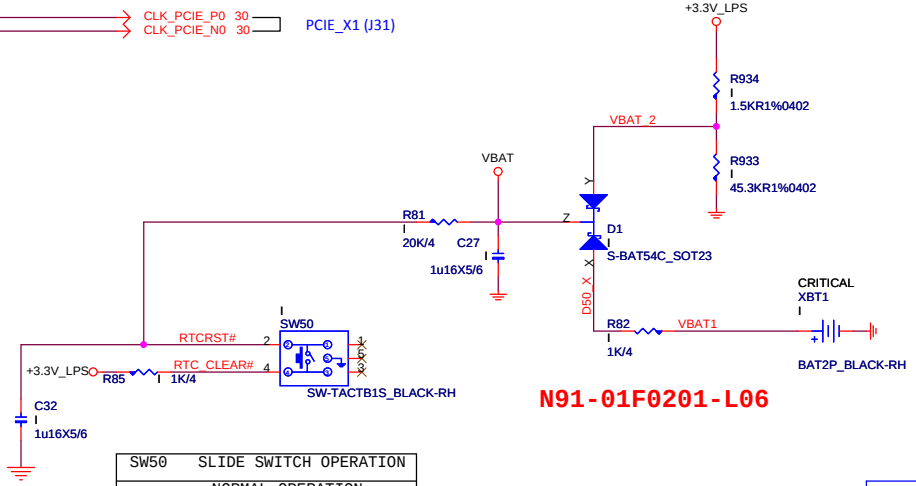


RTC Block

Close to PCH







N91-01F0201-L06

SW50	SLIDE SWITCH OPERATION
	NORMAL OPERATION
	CLEAR CMOS

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Title: PCH-CLK

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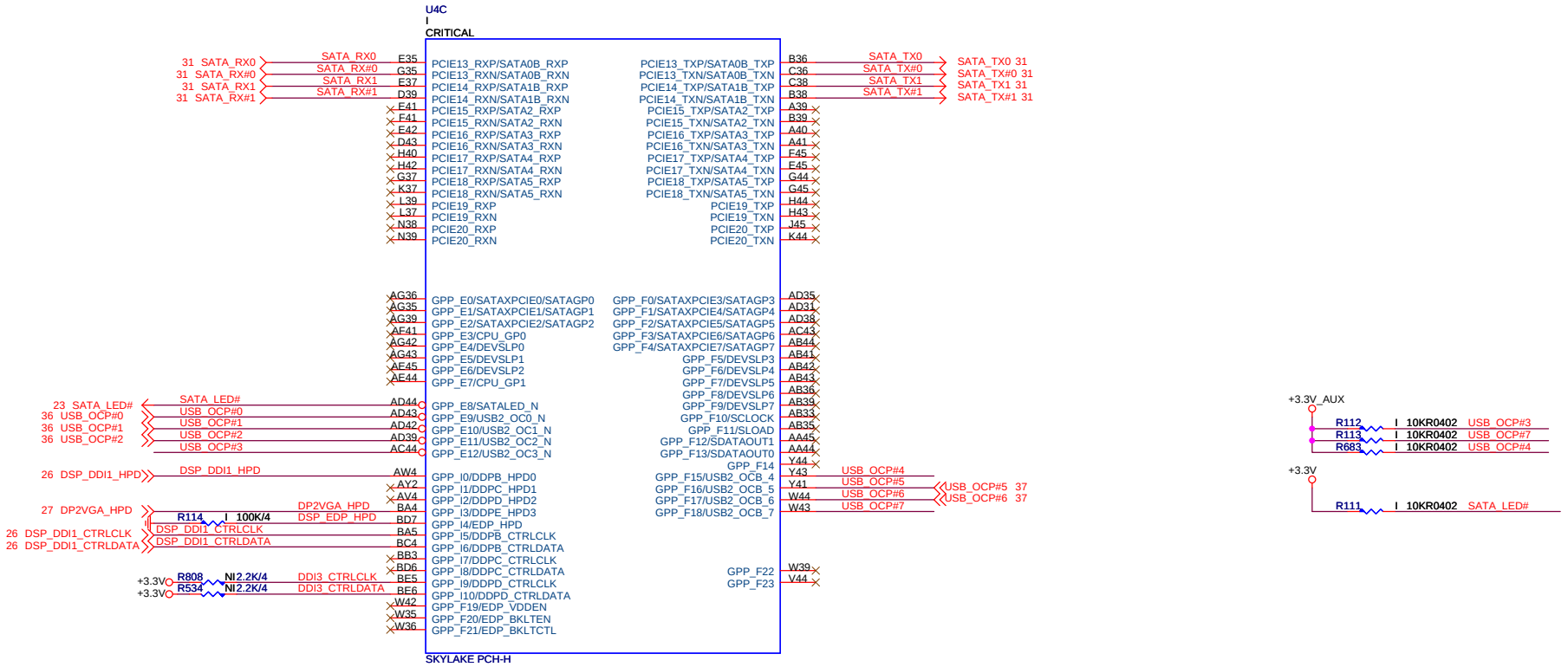

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Title: PCH-DDI/SATA

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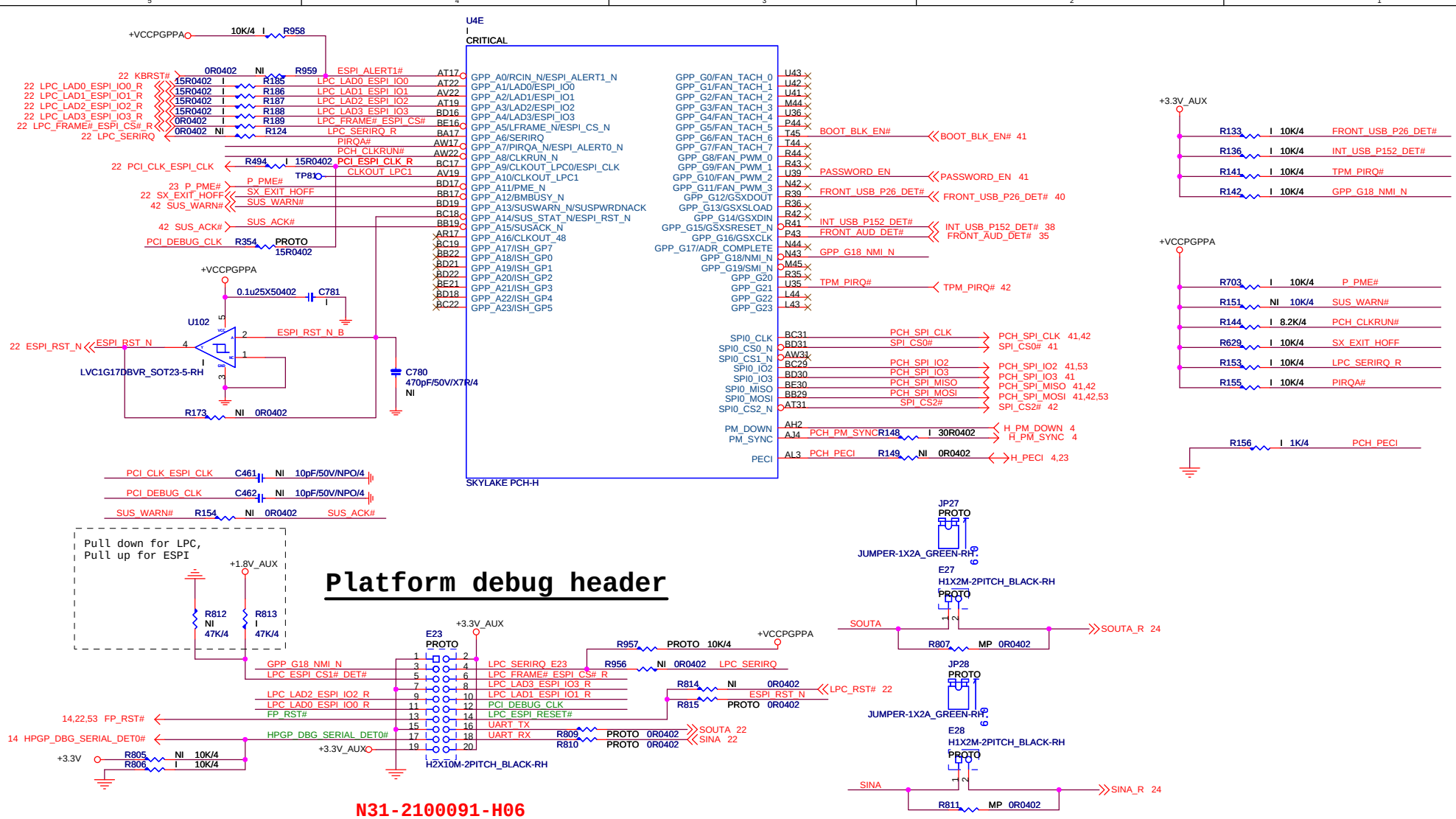

N31-2100091-H06

E25 - PLATFORM DEBUG HEADER - ENT15 PIN DESCRIPTION

PIN #	Voltage Level	Direction	SIGNAL NAME	SIGNAL NAME	Direction	Voltage	PIN #
1	GND	GND	GND	+3.3V_AUX	Power	Power	2
3	O/D	IN	NMI#	eSPI_ALERT#_LPCIRQ	BiDi	1.8V/3.3V	4
5	1.8V/3.3V	OUT	eSPI_CS1#/LPC_detect#	eSPI_CS0#/LPC_LFRAME#	OUT	1.8V/3.3V	6
7	GND	GND	GND	eSPI_DATA3/LPC_AD3	BiDi	1.8V/3.3V	8
9	1.8V/3.3V	BiDi	eSPI_DATA2/LPC_AD2	eSPI_DATA1/LPC_AD1	BiDi	1.8V/3.3V	10
11	1.8V/3.3V	BiDi	eSPI_DATA0/LPC_AD0	eSPI_CLK/LPC_LPC	OUT	1.8V/3.3V	12
13	O/D	IN	System RESET IN#	eSPI_RESET#/LPC_RESET#	OUT	1.8V/3.3V	14
15	GND	GND	GND	UART_TX	OUT	3.3V	16
17	3.3V	IN	HPGP_DBG_SERIAL_DET0#	UART_RX	IN	3.3V	18
19	Power	Power	+3.3V_AUX	+3.3V_AUX	Power	Power	20

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Title	PCH-LPC/SPI
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Maranello	
Barchetta	
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Title: PCH-SMB/AUDIO

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+3.3V_AUX
R536 NI 0R
+1.8V_AUX
R564 0R
+VCCPGPPA

+1.8V_AUX for ESPI.
+3.3V_AUX for LPC.

U4G
CRITICAL

+PCH_P1V0
N17 VCCCLK1
V17 VCCCLK2
R19 VCCCLK3
U20 VCCCLK4
P1V0_PCH_VCCF24_1P0 K3 VCCCLK5-1
K2 VCCCLK5-0
R17 VCCCLK6

C33 0.1u16X/4
C34 1u16X50402-HF
DCPRTC BA26 DCPRTC
DCPDSW BA29 DCPDSW_1P0

P1V0_PCH_VCCAPLL AN19 VCCHDAPLL_1P0
P1V0_PCH_VCCAMPHYPLL B43 VCCMPHYPLL_1P0-0
A43 VCCMPHYPLL_1P0-1

+PCH_P1V0
U26 VCCMPHY_1P0-4
U25 VCCMPHY_1P0-3
U23 VCCMPHY_1P0-2
U21 VCCMPHY_1P0-1
V26 VCCMPHY_1P0-0

P1V0_PCH_VCCAPLL AL5 VCCUSB2PLL_1P0-1
AJ5 VCCUSB2PLL_1P0-0

+PCH_P1V0
AJ20 VCCPRIM_1P0-16
AJ21 VCCPRIM_1P0-15
AJ23 VCCPRIM_1P0-14
AJ25 VCCPRIM_1P0-13
AL22 VCCPRIM_1P0-12
AC17 VCCPRIM_1P0-11
AD15 VCCPRIM_1P0-10
Y25 VCCPRIM_1P0-9
Y23 VCCPRIM_1P0-8
AA26 VCCPRIM_1P0-7
AA23 VCCPRIM_1P0-6
AA28 VCCPRIM_1P0-5
AC28 VCCPRIM_1P0-4
AE26 VCCPRIM_1P0-3
AE23 VCCPRIM_1P0-2
AC26 VCCPRIM_1P0-1
AC23 VCCPRIM_1P0-0

+3.3V
R177 0R
+3.3V_LPS
C40 1u16X50402-HF
PCH_VCCATS AD13 VCCATS_1P8

BA24 VCCDSW_3P3-1
W15 VCCDSW_3P3-0
+3.3V_AUX
BD3 VCCPRIM_3P3-3
BE4 VCCPRIM_3P3-2
BE3 VCCPRIM_3P3-1
AN5 VCCPRIM_3P3-0

VBAT
BA22 VCCRTC
BA20 VCCRTCPRIM_3P3

SKYLAKE PCH-H

VCCPGPPG AD41
VCCPGPPA BA31
+3.3V_AUX
+VCCPGPPA

VCCPGPPBH-1 BC42
VCCPGPPBH-0 BD40

VCCPGPPCD-1 BA45
VCCPGPPCD-0 BC44

VCCPGPPEF-1 AJ41
VCCPGPPEF-0 AL41

VCCPGPPCD-3 BB45
VCCPGPPCD-2 BC45
+PCH_P1V0

VCCMPHYGT_1P0 V28

VCCSPI-2 BE41
VCCSPI-1 BE42
VCCSPI-0 BE43

VCCHDA BA15 PCH_VCCHDA

VCCPCIE3PLL_1P0-1 C44 P1V0_PCH_VCCAMPHYPLL
VCCPCIE3PLL_1P0-0 C45

+3.3V_AUX L9 2.2u100mA-RH/0603 PCH_VCCHDA
C778 0.1u25X50402

+PCH_P1V0 L1 2.2u100mA-RH P1V0_PCH_VCCAPLL
C35 22u6.3X5-HF
C36 22u6.3X5-HF
C779 0.1u25X50402

+PCH_P1V0 L2 2.2u100mA-RH P1V0_PCH_VCCAMPHYPLL
C37 22uF/6.3V/X5R/0805
C38 22uF/6.3V/X5R/0805
C39 1u16X50402-HF
Close PIN A43

P1V0_PCH_VCCF24_1P0
+PCH_P1V0 L3 2.2u100mA-RH P1V0_PCH_VCCF24_1P0
C41 22uF/6.3V/X5R/0805
C42 22uF/6.3V/X5R/0805
C43 1u16X50402-HF
Close PIN K2

+PCH_P1V0
C44 22uF/6.3V/X5R/0805
C45 1u16X50402-HF
C46 1u16X50402-HF
C47 1u16X50402-HF
Close PIN U21

+3.3V_AUX
Close PIN BC42/AJ41/AD41/AN5
C48 0.1u16X/4
C49 0.1u16X/4
C50 0.1u16X/4
C51 0.1u16X/4

+3.3V_AUX
C52 1u16X50402-HF
C396 0.1u16X/4
Close PIN BA20

VBAT
C53 1u16X50402-HF
C395 0.1u16X/4
Close PIN BA22

+3.3V_LPS
C54 1u16X50402-HF
Close PIN W15

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Maranello	
Barchetta	
Enzo	V

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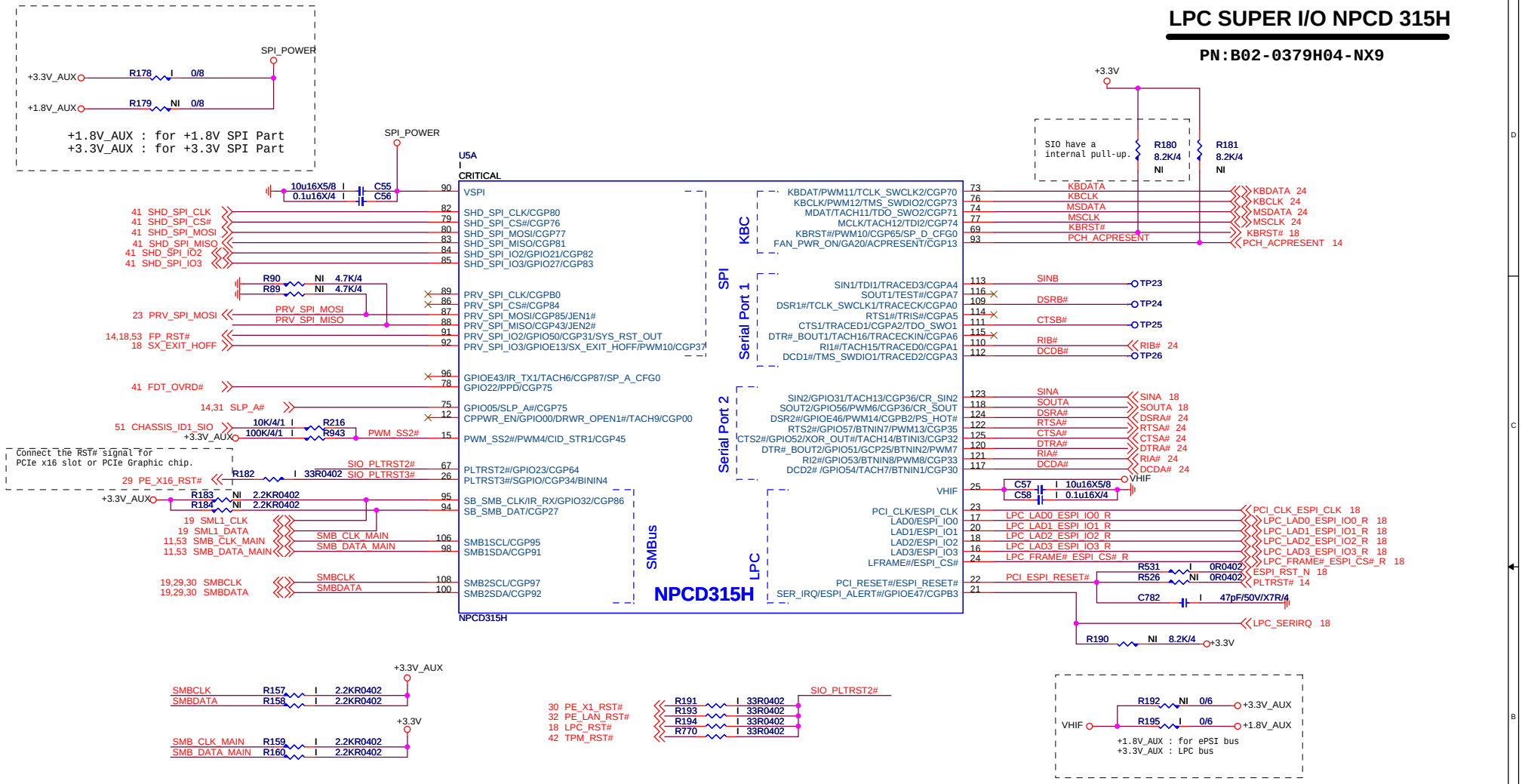
LPC SUPER I/O NPCD 315H

PN:B02-0379H04-NX9



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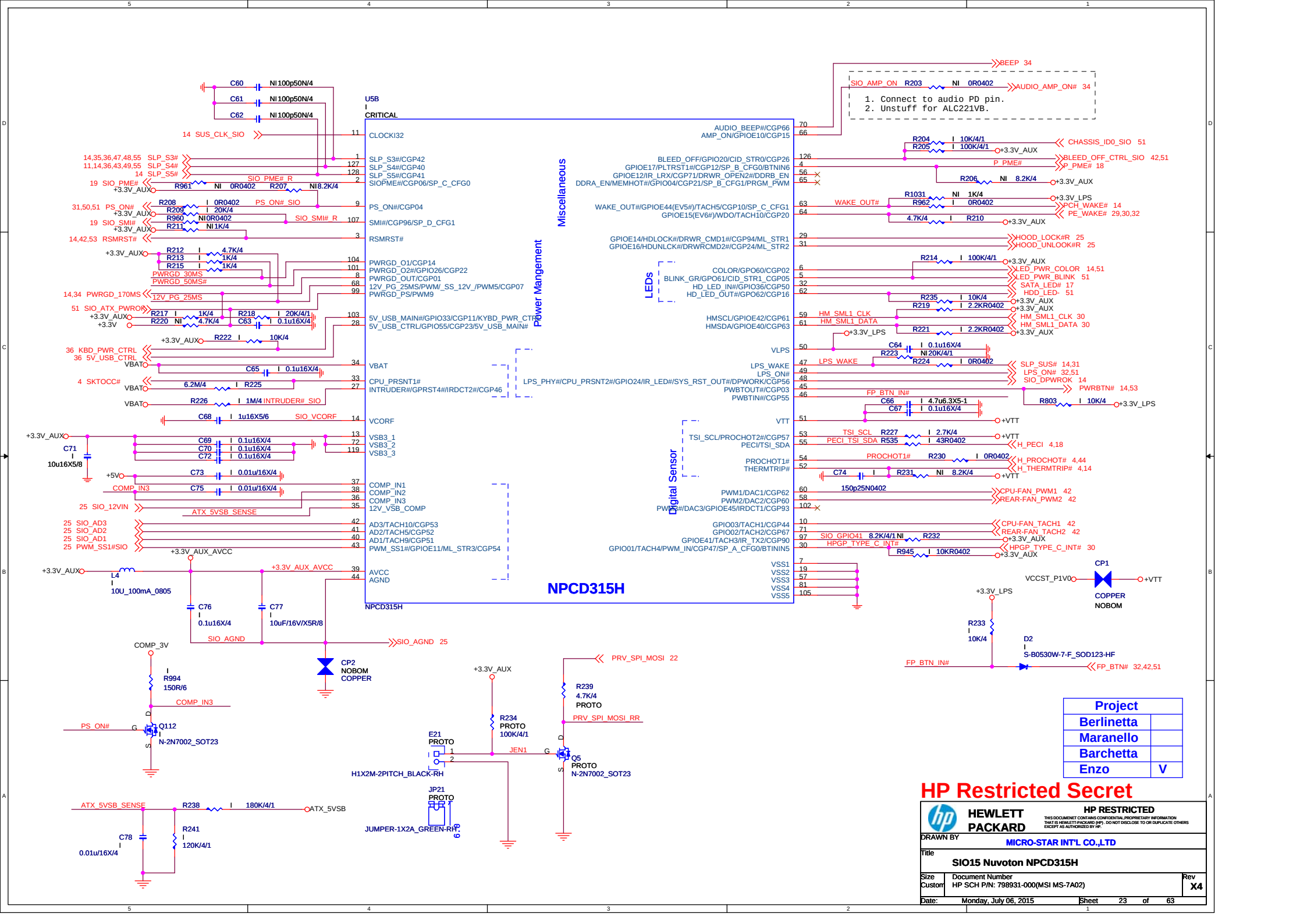
U5B
CRITICAL
NPCD315H
Miscellaneous
Power Mangement
LEDs
Digital Sensor
CLOCKI32
SLP_S3#/CGP42
SLP_S4#/CGP40
SLP_S5#/CGP41
SIOPME#/CGP06/SP_C_CFG0
PS_ON#/CGP04
SMI#/CGP96/SP_D_CFG1
RSMRST#
PWRGD_O1/CGP14
PWRGD_O2#/GPIO26/CGP22
PWRGD_OUT/CGP01
12V_PG_25MS/PWM/_SS_12V_/PWM5/CGP07
PWRGD_PS/PWM9
5V_USB_MAIN#/GPIO33/CGP11/KYBD_PWR_CTRL
5V_USB_CTRL/GPIO55/CGP23/5V_USB_MAIN#
VBAT
CPU_PRSNT1#
INTRUDER#/GPRST4#/IRDCT2#/CGP46
VCORF
VSB3_1
VSB3_2
VSB3_3
COMP_IN1
COMP_IN2
COMP_IN3
12V_VSB_COMP
AD3/TACH10/CGP53
AD2/TACH5/CGP52
AD1/TACH9/CGP51
PWM_SS1#/GPIOE11/ML_STR3/CGP54
AVCC
AGND
AUDIO_BEEP#/CGP66
AMP_ON/GPIOE10/CGP15
BLEED_OFF/GPIO20/CID_STR0/CGP26
GPIOE17/PLTRST1#/CGP12/SP_B_CFG0/BTNIN6
GPIOE12/IR_LRX/CGP71/DRWR_OPEN2#/DDRB_EN
DDRA_EN/MEMHOT#/GPIO04/CGP21/SP_B_CFG1/PRGM_PWM
WAKE_OUT#/GPIOE44(EV5#)/TACH5/CGP10/SP_C_CFG1
GPIOE15(EV6#)/WDO/TACH10/CGP20
GPIOE14/HDLOCK#/DRWR_CMD1#/CGP94/ML_STR1
GPIOE16/HDUNLCK#/DRWRCMD2#/CGP24/ML_STR2
COLOR/GPO60/CGP02
BLINK_GR/GPO61/CID_STR1_CGP05
HD_LED_IN#/GPIO36/CGP50
HD_LED_OUT#/GPO62/CGP16
HMSCL/GPIOE42/CGP61
HMSDA/GPIOE40/CGP63
VLPS
LPS_WAKE
LPS_ON#
PWBTOUT#/CGP03
PWBTIN#/CGP55
VTT
TSI_SCL/PROCHOT2#/CGP57
PECI/TSI_SDA
PROCHOT1#
THERMTRIP#
PWM1/DAC1/CGP62
PWM2/DAC2/CGP60
PWM3#/DAC3/GPIOE45/IRDCT1/CGP93
GPIO03/TACH1/CGP44
GPIO02/TACH2/CGP67
GPIOE41/TACH3/IR_TX2/CGP90
GPIO01/TACH4/PWM_IN/CGP47/SP_A_CFG0/BTININ5
VSS1
VSS2
VSS3
VSS4
VSS5
LPS_PHY#/CPU_PRSNT2#/GPIO24/IR_LED#/SYS_RST_OUT#/DPWORK/CGP56
BEEP 34
SIO_AMP_ON R203 NI 0R0402 AUDIO_AMP_ON# 34
1. Connect to audio PD pin.
2. Unstuff for ALC221VB.
CHASSIS_ID0_SIO 51
BLEED_OFF_CTRL_SIO 42,51
P_PME# 18
WAKE_OUT#
PCH_WAKE# 14
PE_WAKE# 29,30,32
HOOD_LOCK#R 25
HOOD_UNLOOK#R 25
LED_PWR_COLOR 14,51
LED_PWR_BLINK 51
SATA_LED# 17
HDD_LED 51
HM_SML1_CLK 30
HM_SML1_DATA 30
SLP_SUS# 14,31
LPS_ON# 32,51
SIO_DPWROK 14
PWRBTN# 14,53
FP_BTN_IN#
H_PECI 4,18
H_PROCHOT# 4,44
H_THERMTRIP# 4,14
CPU-FAN_PWM1 42
REAR-FAN_PWM2 42
CPU-FAN_TACH1 42
REAR-FAN_TACH2 42
HPGP_TYPE_C_INT# 30
VCCST_P1V0
CP1
COPPER
NOBOM
+VTT
+3.3V_LPS
R233 10K/4
D2
S-B0530W-7-F_SOD123-HF
FP_BTN# 32,42,51
14 SUS_CLK_SIO
14,35,36,47,48,55 SLP_S3#
11,14,36,43,49,55 SLP_S4#
14 SLP_S5#
19 SIO_PME#
SIO_PME# R
R961 NI 0R0402 R207 NI 8.2K/4
31,50,51 PS_ON#
PS_ON# SIO
19 SIO_SMI#
SIO_SMI# R
14,42,53 RSMRST#
PWRGD_30MS
PWRGD_50MS#
14,34 PWRGD_170MS
12V_PG_25MS
51 SIO_ATX_PWROK
36 KBD_PWR_CTRL
36 5V_USB_CTRL
4 SKTOCC#
6.2M/4 R225
R226 1M/4 INTRUDER# SIO
C68 1u16X5/6 SIO_VCORF
C71 10u16X5/8
C69 0.1u16X/4
C70 0.1u16X/4
C72 0.1u16X/4
C73 0.01u/16X/4
C75 0.01u/16X/4
COMP_IN3
25 SIO_12VIN
ATX_5VSB_SENSE
25 SIO_AD3
25 SIO_AD2
25 SIO_AD1
25 PWM_SS1#SIO
L4 10U_100mA_0805
C76 0.1u16X/4
C77 10uF/16V/X5R/8
SIO_AGND 25
CP2 NOBOM COPPER
R994 150R/6
Q112 N-2N7002_SOT23
PS_ON#
E21 PROTO
H1X2M-2PITCH_BLACK-RH
JP21 PROTO
JUMPER-1X2A_GREEN-RH
R234 PROTO 100K/4/1
JEN1
Q5 PROTO N-2N7002_SOT23
R239 4.7K/4 PROTO
PRV_SPI_MOSI 22
PRV_SPI_MOSI_RR
R238 180K/4/1
ATX_5VSB
C78 0.01u/16X/4
R241 120K/4/1
R204 10K/4/1
R205 100K/4/1
R206 NI 8.2K/4
R1031 NI 1K/4
R962 0R0402
4.7K/4 R210
R214 100K/4/1
R235 10K/4
R219 2.2KR0402
R221 2.2KR0402
C64 0.1u16X/4
R223 NI 20K/4/1
R224 0R0402
C66 4.7u6.3X5-1
C67 0.1u16X/4
R803 10K/4
R227 2.7K/4
R535 43R0402
R230 0R0402
C74
R231 NI 8.2K/4
150p25N0402
SIO_GPIO41 8.2K/4/1 NI
R232
R945 10KR0402
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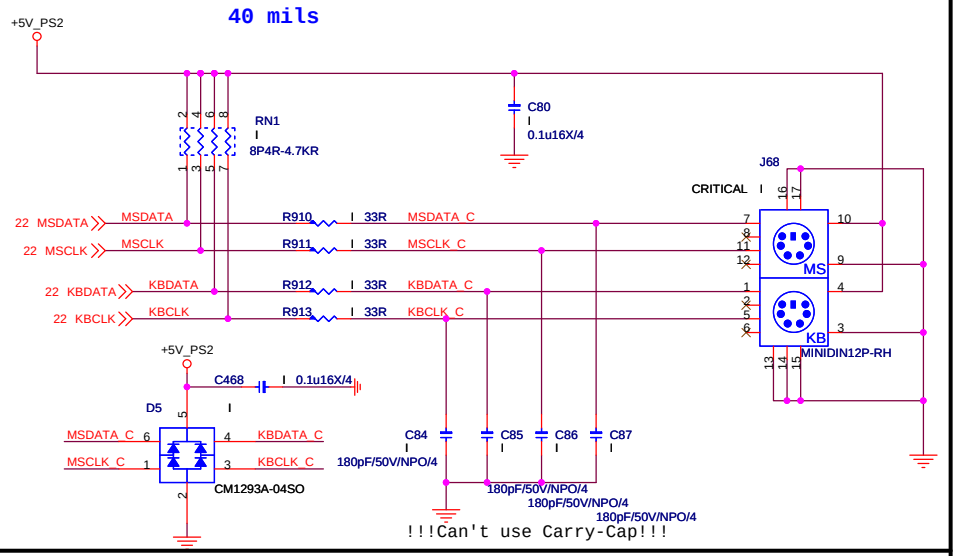
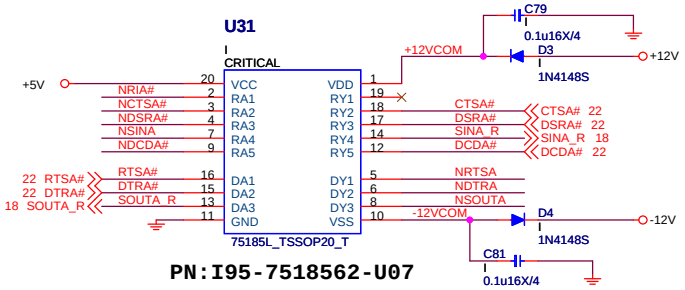
PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL PORT 1



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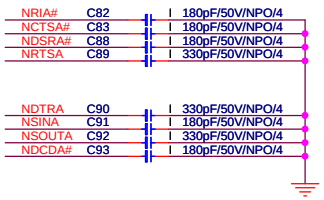

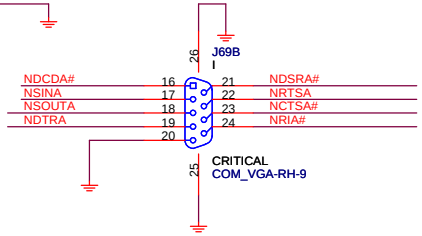

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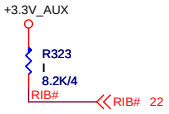

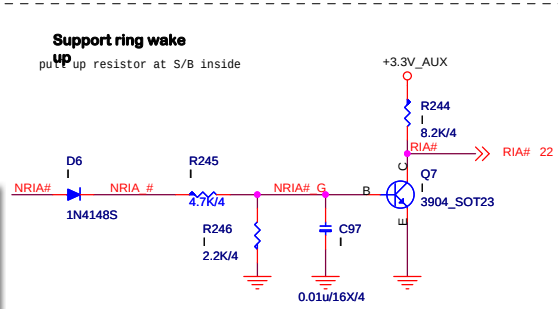

TABLE 12
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

P52

Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	RI#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCD#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

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Maranello	
Barchetta	
Enzo	V

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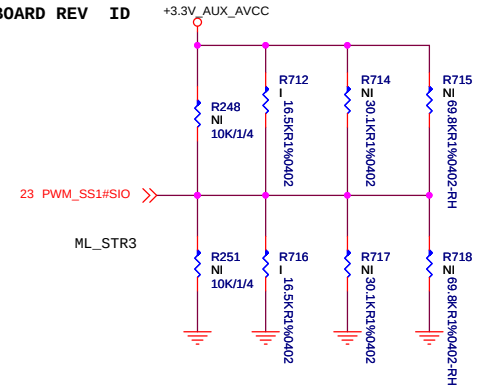
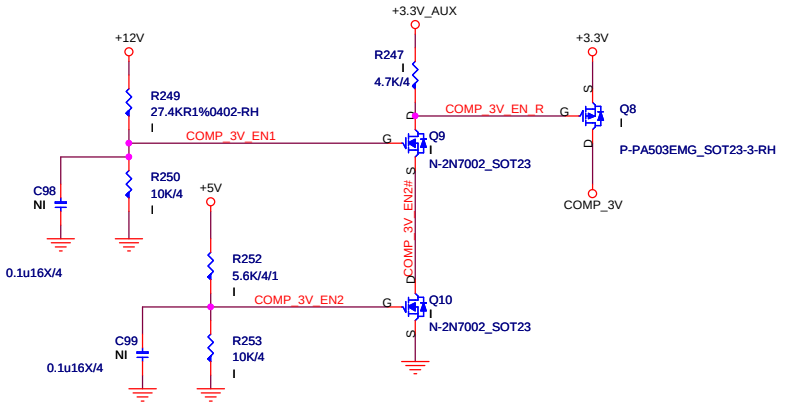
BOARD REV ID

Board REV	Pull-Down	Pull-UP	Development Phase
0	10K	NI	BD-1
1	10k	69.8k	BD-2
2	10k	30.1k	BD-3
3	10k	16.5k	SI-1
4	16.5k	16.5k	SI-2
5	16.5k	10k	SI-3
6	30.1k	10k	PV-1
7	69.8k	10k	PV-2



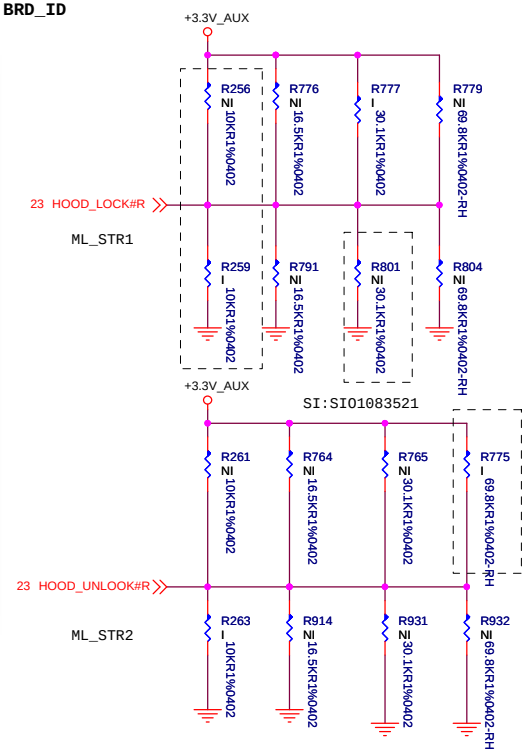


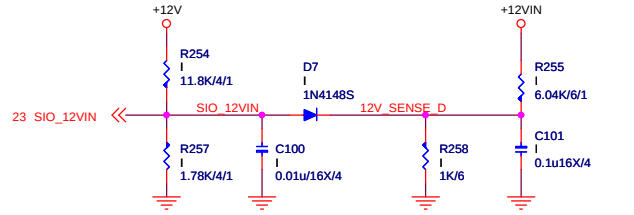
BRD_ID

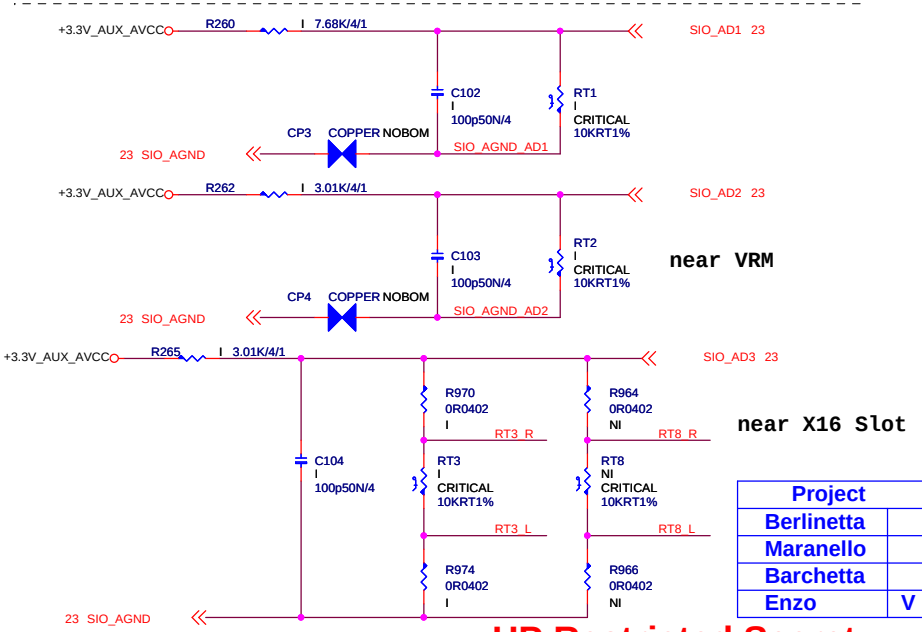
PCA	ML_STR2[2:0] (hex)	ML_STR1[2:0] (hex)
Berlinetta	0	7
Maranello	1	0
Barchetta	1	1
Enzo	1	2

Multi-Voltage Resistor Values (1%) - HP SIO15+

Value (h)	Pull-Down	Pull-UP
0	10K	NI
1	10k	69.8k
2	10k	30.1k
3	10k	16.5k
4	16.5k	16.5k
5	16.5k	10k
6	30.1k	10k
7	69.8k	10k







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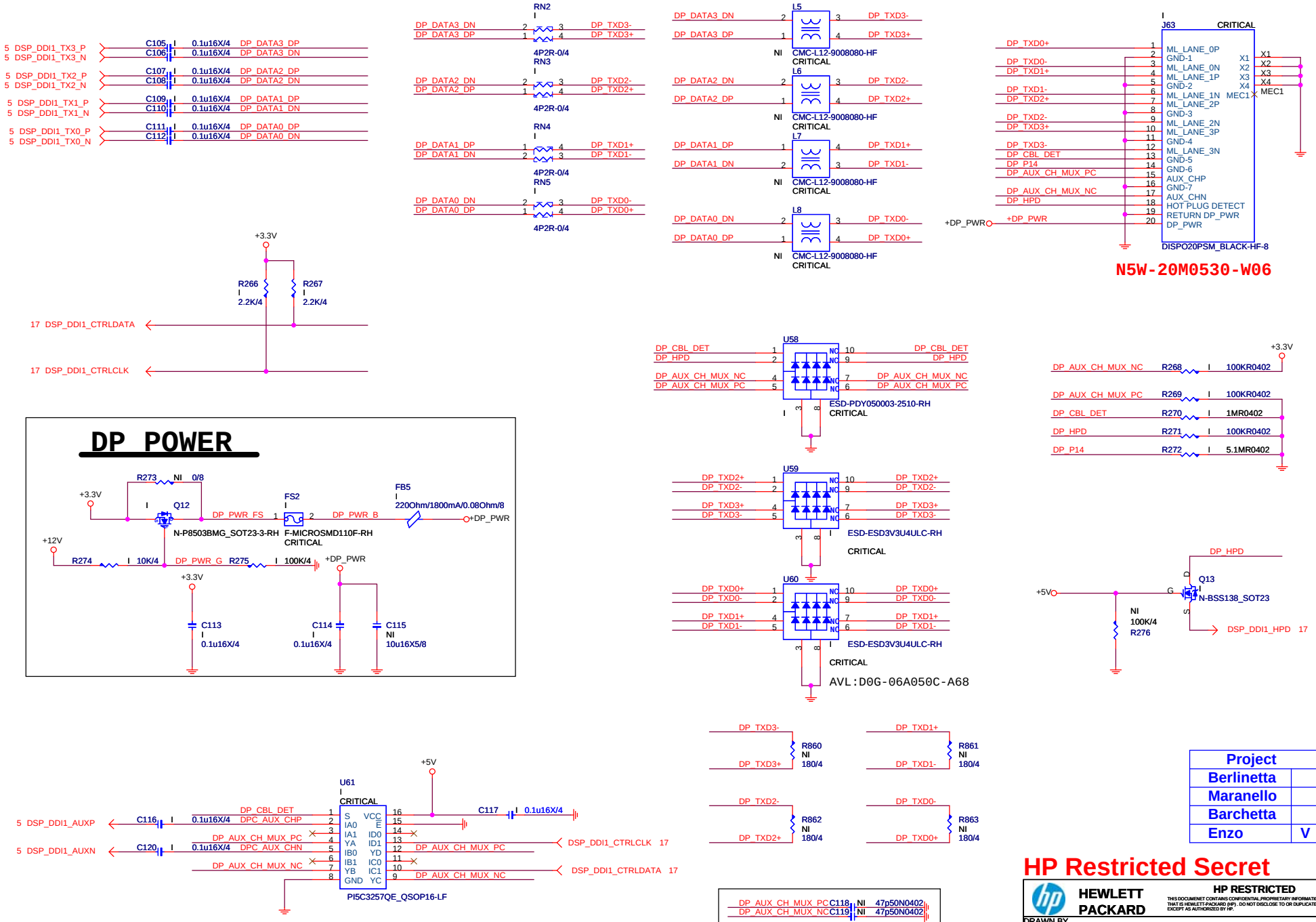
5 DSP_DDI1_TX3_P
5 DSP_DDI1_TX3_N
C105 0.1u16X/4 DP_DATA3_DP
C106 0.1u16X/4 DP_DATA3_DN
5 DSP_DDI1_TX2_P
5 DSP_DDI1_TX2_N
C107 0.1u16X/4 DP_DATA2_DP
C108 0.1u16X/4 DP_DATA2_DN
5 DSP_DDI1_TX1_P
5 DSP_DDI1_TX1_N
C109 0.1u16X/4 DP_DATA1_DP
C110 0.1u16X/4 DP_DATA1_DN
5 DSP_DDI1_TX0_P
5 DSP_DDI1_TX0_N
C111 0.1u16X/4 DP_DATA0_DP
C112 0.1u16X/4 DP_DATA0_DN
RN2
DP_DATA3_DN DP_TXD3-
DP_DATA3_DP DP_TXD3+
4P2R-0/4
RN3
DP_DATA2_DN DP_TXD2-
DP_DATA2_DP DP_TXD2+
4P2R-0/4
RN4
DP_DATA1_DP DP_TXD1+
DP_DATA1_DN DP_TXD1-
4P2R-0/4
RN5
DP_DATA0_DN DP_TXD0-
DP_DATA0_DP DP_TXD0+
4P2R-0/4
L5
DP_DATA3_DN DP_TXD3-
DP_DATA3_DP DP_TXD3+
NI CMC-L12-9008080-HF CRITICAL
L6
DP_DATA2_DN DP_TXD2-
DP_DATA2_DP DP_TXD2+
NI CMC-L12-9008080-HF CRITICAL
L7
DP_DATA1_DP DP_TXD1+
DP_DATA1_DN DP_TXD1-
NI CMC-L12-9008080-HF CRITICAL
L8
DP_DATA0_DN DP_TXD0-
DP_DATA0_DP DP_TXD0+
NI CMC-L12-9008080-HF CRITICAL
J63 CRITICAL
DP_TXD0+
DP_TXD0-
DP_TXD1+
DP_TXD1-
DP_TXD2+
DP_TXD2-
DP_TXD3+
DP_TXD3-
DP_CBL_DET
DP_P14
DP_AUX_CH_MUX_PC
DP_AUX_CH_MUX_NC
DP_HPD
+DP_PWR
ML_LANE_0P
GND-1
ML_LANE_0N
ML_LANE_1P
GND-2
ML_LANE_1N
ML_LANE_2P
GND-3
ML_LANE_2N
ML_LANE_3P
GND-4
ML_LANE_3N
GND-5
GND-6
AUX_CHP
GND-7
AUX_CHN
HOT PLUG DETECT
RETURN DP_PWR
DP_PWR
X1
X2
X3
X4
MEC1
DISPO20PSM_BLACK-HF-8
N5W-20M0530-W06
+3.3V
R266 2.2K/4
R267 2.2K/4
17 DSP_DDI1_CTRLDATA
17 DSP_DDI1_CTRLCLK
DP_POWER
R273 NI 0/8
+3.3V
Q12
N-P8503BMG_SOT23-3-RH
DP_PWR_FS
FS2
F-MICROSMD110F-RH CRITICAL
DP_PWR_B
FB5
220Ohm/1800mA/0.08Ohm/8
+DP_PWR
+12V
R274 10K/4
DP_PWR_G
R275 100K/4
+DP_PWR
+3.3V
C113 0.1u16X/4
C114 0.1u16X/4
C115 NI 10u16X5/8
U58
DP_CBL_DET
DP_HPD
DP_AUX_CH_MUX_NC
DP_AUX_CH_MUX_PC
ESD-PDY050003-2510-RH CRITICAL
U59
DP_TXD2+
DP_TXD2-
DP_TXD3+
DP_TXD3-
ESD-ESD3V3U4ULC-RH CRITICAL
U60
DP_TXD0+
DP_TXD0-
DP_TXD1+
DP_TXD1-
ESD-ESD3V3U4ULC-RH CRITICAL
AVL:D0G-06A050C-A68
+3.3V
DP_AUX_CH_MUX_NC R268 100KR0402
DP_AUX_CH_MUX_PC R269 100KR0402
DP_CBL_DET R270 1MR0402
DP_HPD R271 100KR0402
DP_P14 R272 5.1MR0402
DP_HPD
+5V
Q13
N-BSS138_SOT23
NI 100K/4 R276
DSP_DDI1_HPD 17
+5V
U61
CRITICAL
5 DSP_DDI1_AUXP
C116 0.1u16X/4 DPC_AUX_CHP
5 DSP_DDI1_AUXN
C120 0.1u16X/4 DPC_AUX_CHN
DP_CBL_DET
DP_AUX_CH_MUX_PC
DP_AUX_CH_MUX_NC
S VCC
IA0 E
IA1 ID0
YA ID1
IB0 YD
IB1 IC0
YB IC1
GND YC
C117 0.1u16X/4
DSP_DDI1_CTRLCLK 17
DSP_DDI1_CTRLDATA 17
PI5C3257QE_QSOP16-LF
DP_TXD3- R860 NI 180/4 DP_TXD3+
DP_TXD1+ R861 NI 180/4 DP_TXD1-
DP_TXD2- R862 NI 180/4 DP_TXD2+
DP_TXD0- R863 NI 180/4 DP_TXD0+
DP_AUX_CH_MUX_PC C118 NI 47p50N0402
DP_AUX_CH_MUX_NC C119 NI 47p50N0402
DP_CBL_DET C121 NI 47p50N0402
DP_HPD C122 NI 47p50N0402
Project
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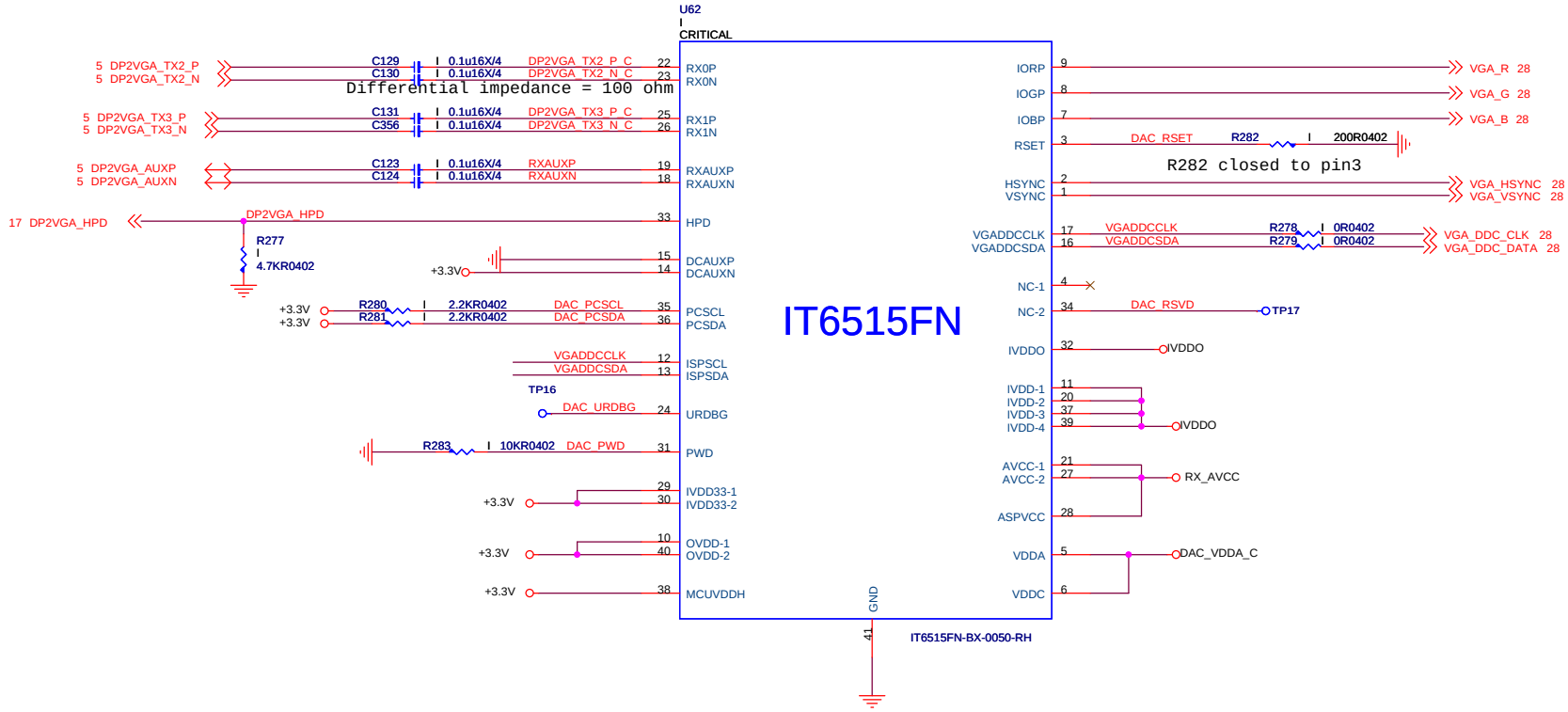

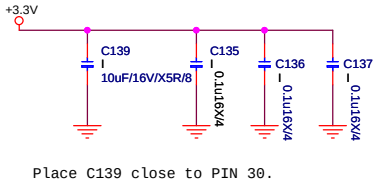

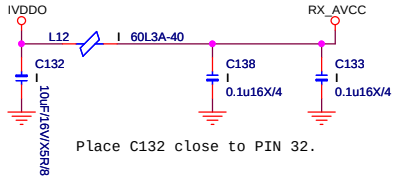

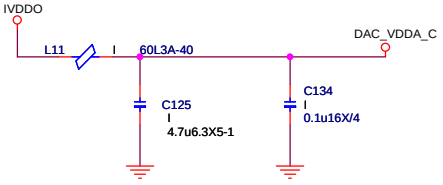

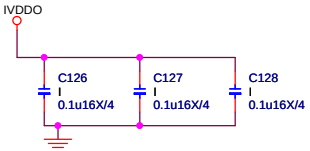

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Title: DP to VGA- ITE IT6515

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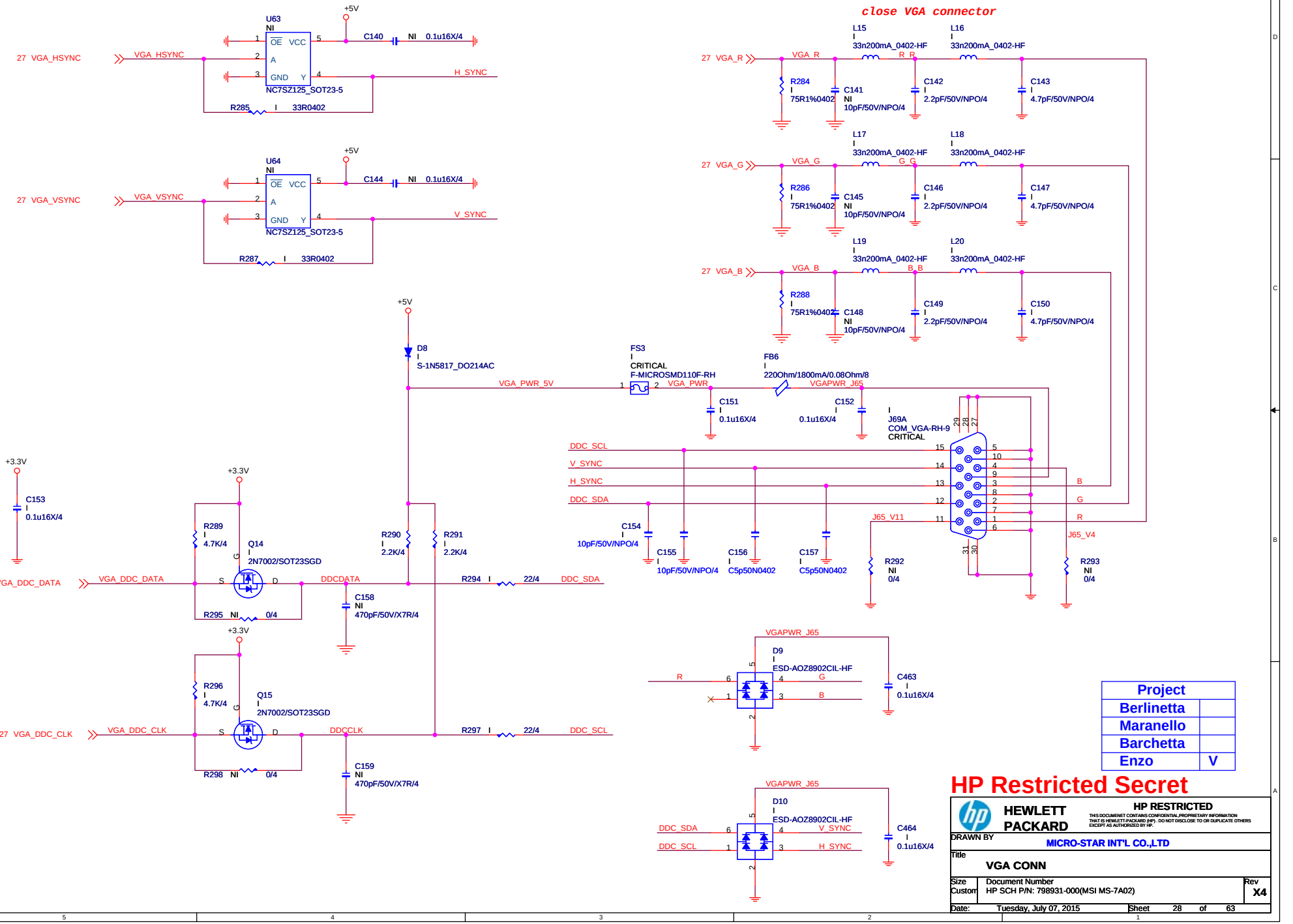
Date: Monday, July 06, 2015 | Sheet 27 of 63

VGA CONN BLOCK



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Title: VGA CONN

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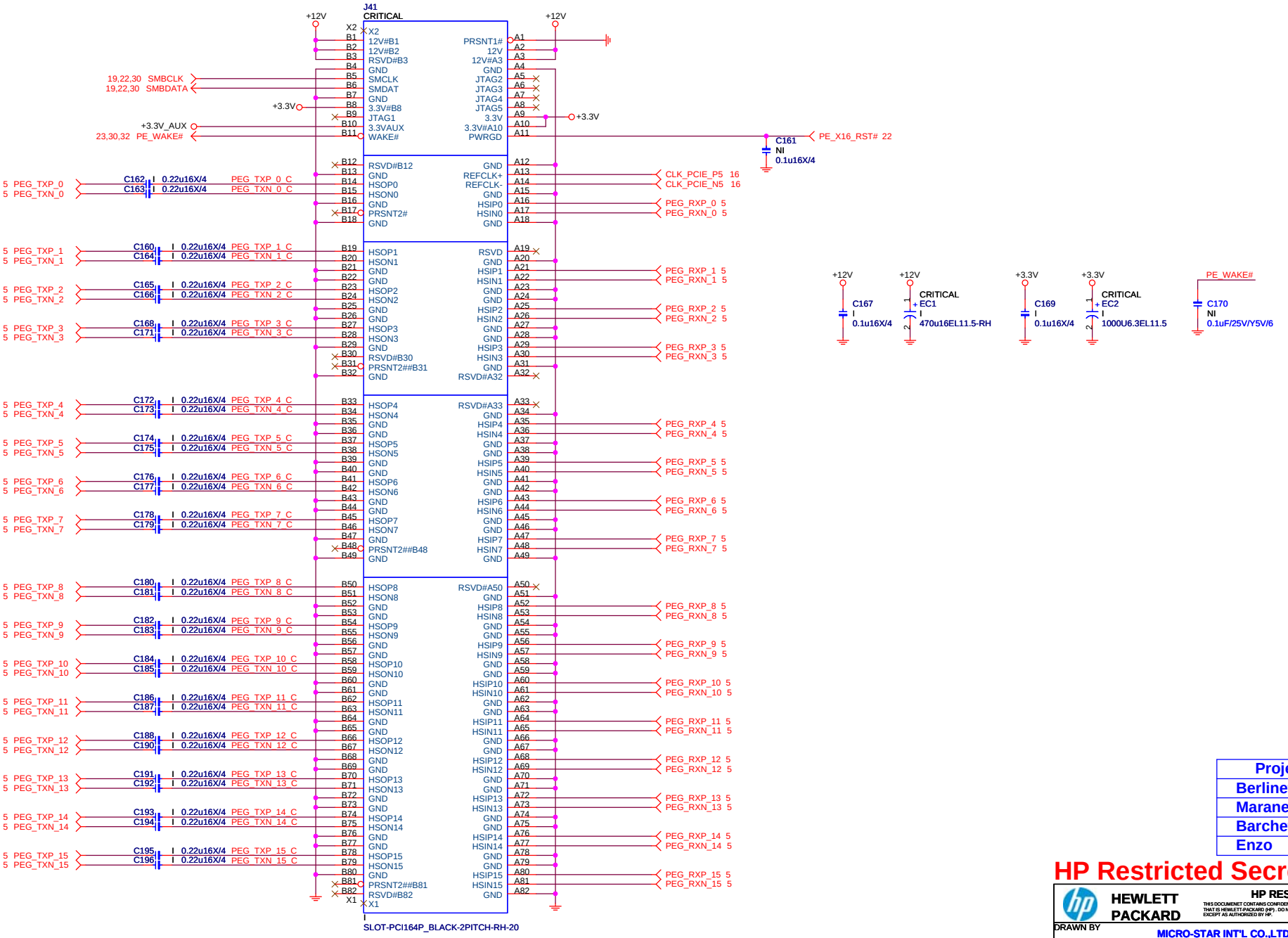
PCI_EXPRESS X16 SLOT



N11-1641151-L06

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Title: PCIE x16 Slot

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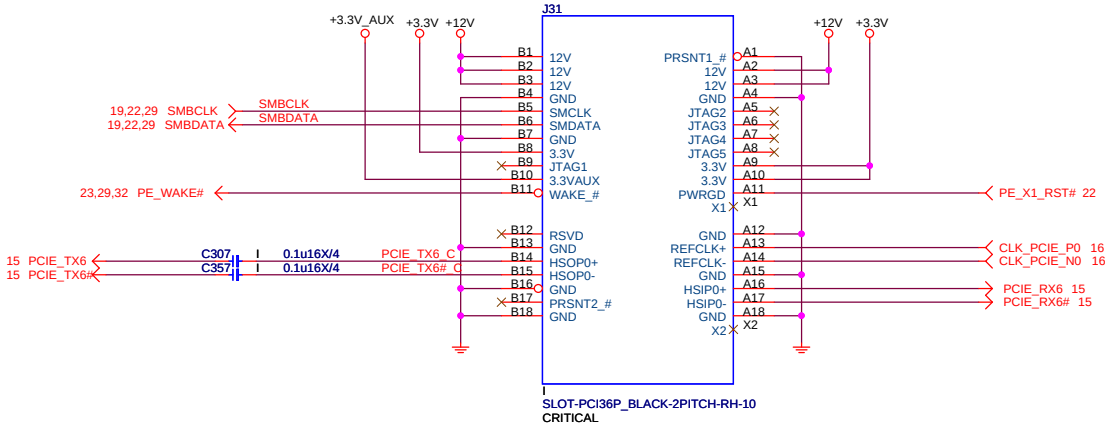
PCI_EXPRESS x1-PORT



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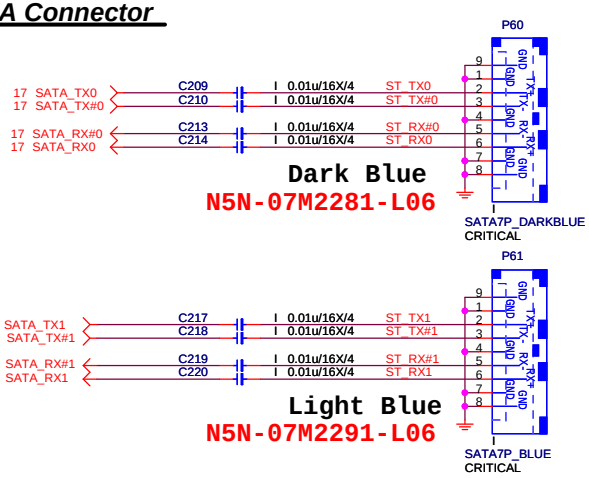
Title: PCIE x1 Slots

Size: Custom | Document Number: HP SCH P/N: 798931-000(MSI MS-7A02) | Rev: X4

Date: Monday, July 06, 2015 | Sheet 30 of 63

SATA Connector



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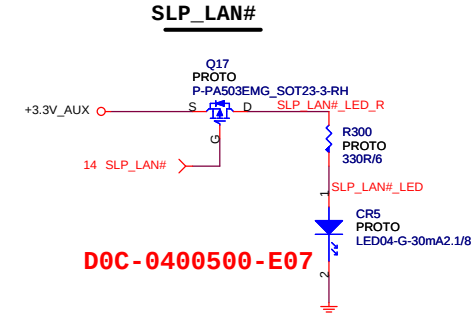

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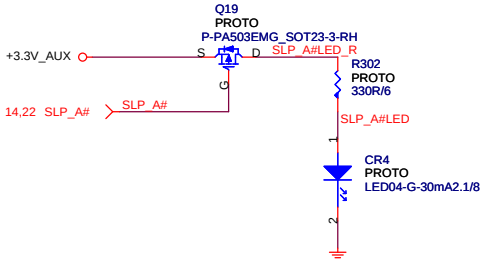
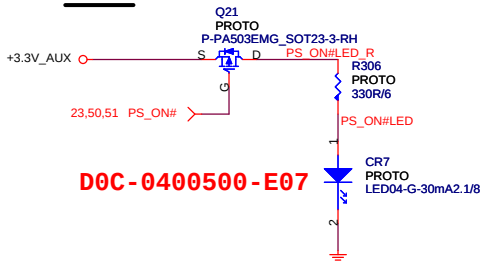
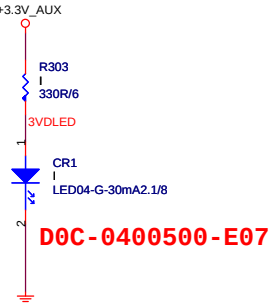


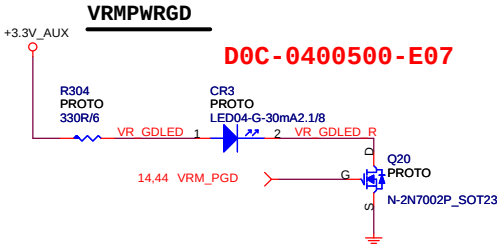
PS_ON#



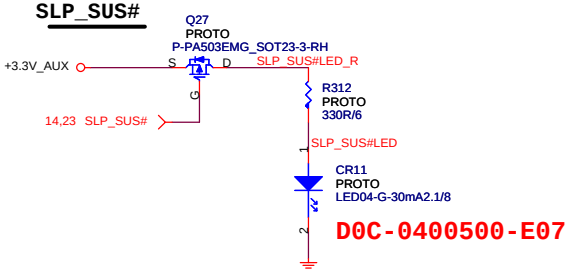
3VSB



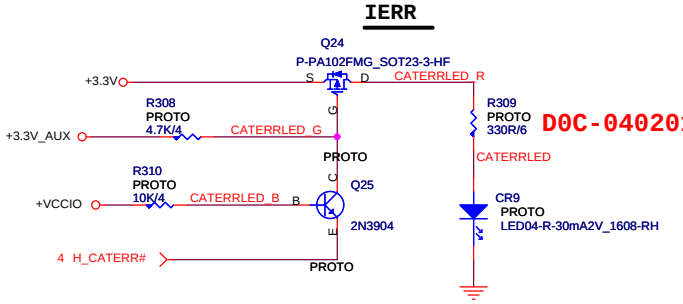
VRMPWRGD



SLP_SUS#



IERR



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Rev	X4
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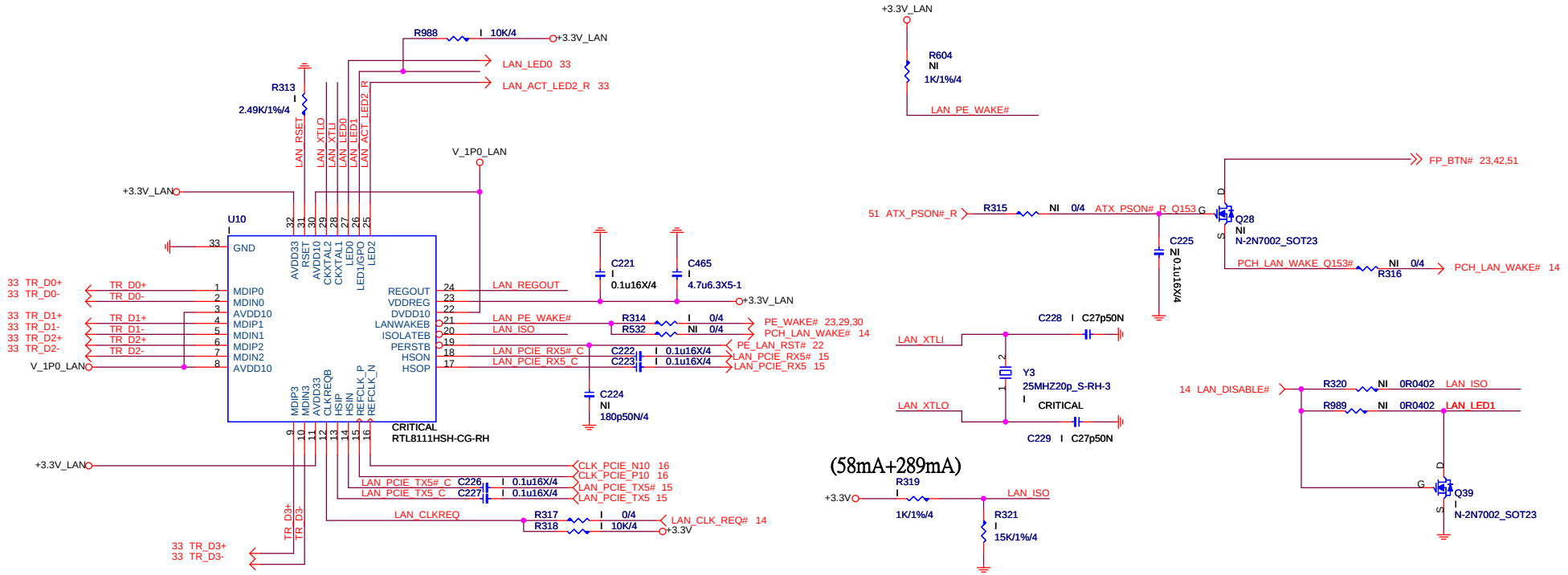
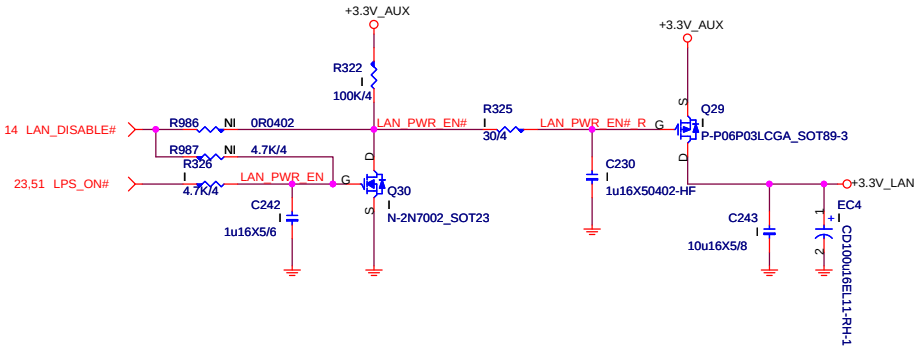
Gigabit LAN RTL8111H-CG

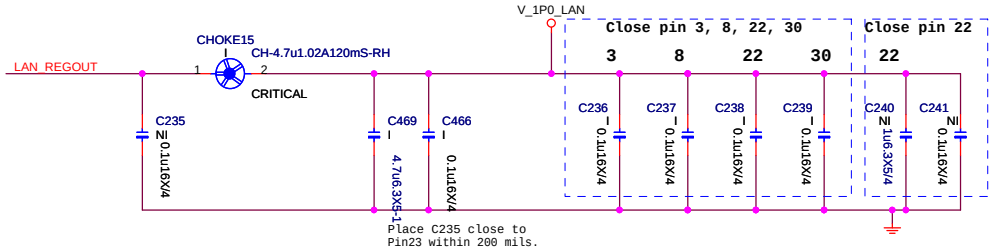


B06-08111CC-R09

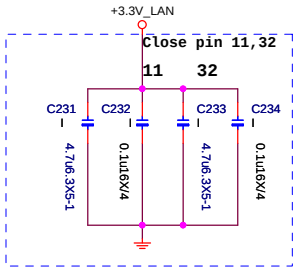
LAN Power



Place Near Pin



Place Near Pin



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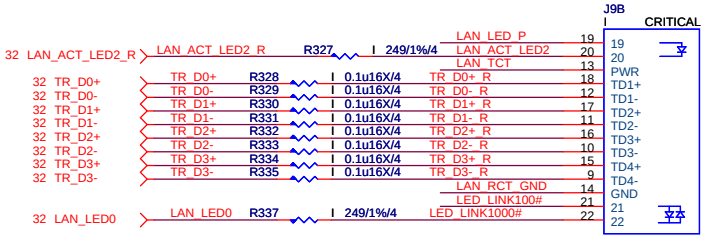
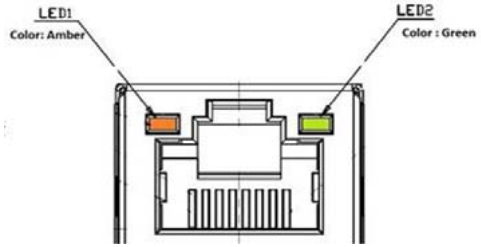
LAN Connector



RJ45_USBX2_LEDX2_TX-GIGA-RH-1

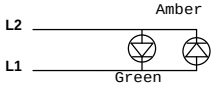
N58-22F0181-U30



Giga-Lan

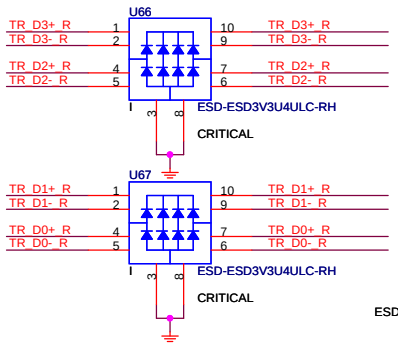
N58-32F0161-U30

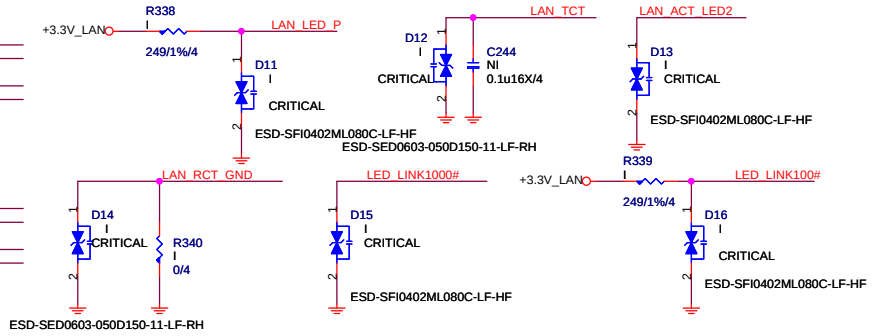
Link	Amber
Active	Blinking
1000	Green
100	Green
10	Green



WOL ON	Speed	Active/Idle Mode		
		S0	S3/S4	S5
Active LED	1G Bit	Blink Amber	Blink Amber	Blink Amber
	100M Bit	Blink Amber	Blink Amber	Blink Amber
	10M Bit	Blink Amber	Blink Amber	Blink Amber
Link Speed LED	1G Bit	Green	Green	Green
	100M Bit	Green	Green	Green
	10M Bit	Green	Green	Green
WOL OFF		S0	S3/S4	S5
Active LED	1G Bit	Blink Amber	OFF	OFF
	100M Bit	Blink Amber	OFF	OFF
	10M Bit	Blink Amber	OFF	OFF
Link Speed LED	1G Bit	Green	OFF	OFF
	100M Bit	Green	OFF	OFF
	10M Bit	Green	OFF	OFF
Link OFF		S0	S3/S4	S5
Active LED	1G Bit	OFF	OFF	OFF
	100M Bit	OFF	OFF	OFF
	10M Bit	OFF	OFF	OFF
Link Speed LED	1G Bit	OFF	OFF	OFF
	100M Bit	OFF	OFF	OFF
	10M Bit	OFF	OFF	OFF

ESD

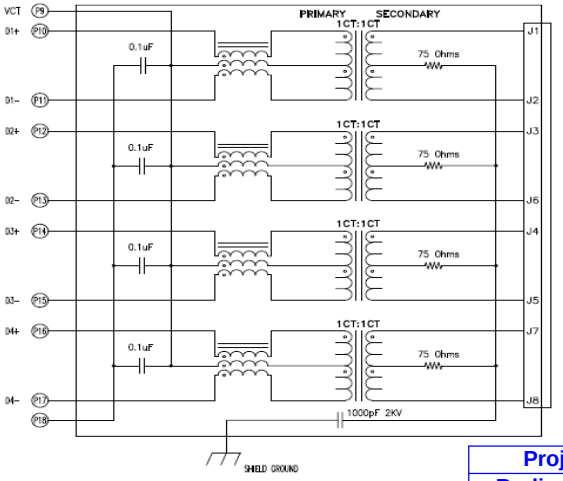




D12,D14,
D0G-1500500-SI0
AVL:D0G-3500510-N47

D11,D13,D15,D16
D0G-2950500-SI0
AVL:D0G-3010510-I05

SCHEMATIC



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Title: LAN CONNECTOR

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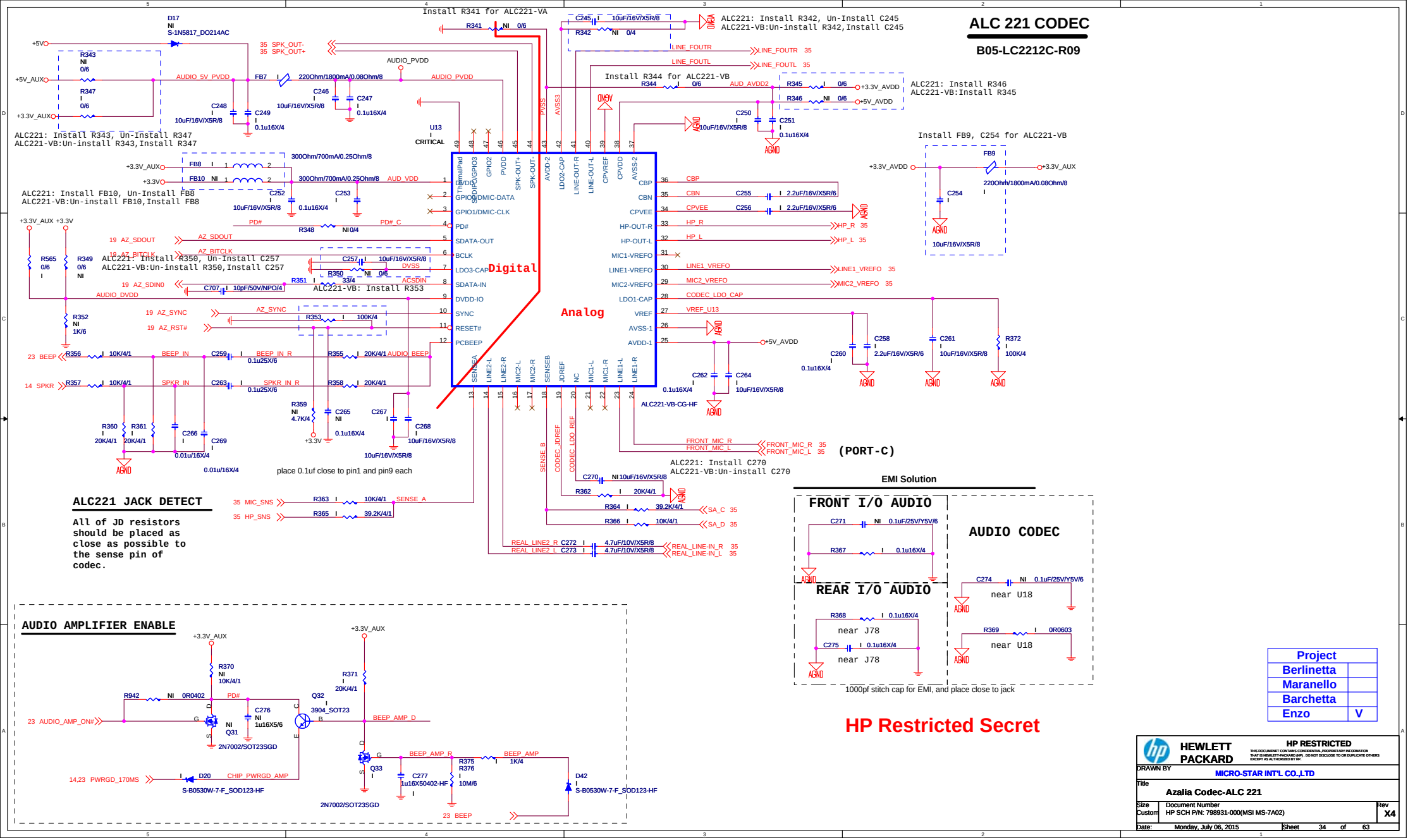
ALC 221 CODEC
B05-LC2212C-R09
Digital
Analog
U13
CRITICAL
ALC221-VB-CG-HF
ALC221: Install R342, Un-Install C245
ALC221-VB:Un-install R342,Install C245
Install R341 for ALC221-VA
Install R344 for ALC221-VB
ALC221: Install R346
ALC221-VB:Install R345
Install FB9, C254 for ALC221-VB
ALC221: Install R343, Un-Install R347
ALC221-VB:Un-install R343,Install R347
ALC221: Install FB10, Un-Install FB8
ALC221-VB:Un-install FB10,Install FB8
ALC221: Install R350, Un-Install C257
ALC221-VB:Un-install R350,Install C257
ALC221-VB: Install R353
ALC221: Install C270
ALC221-VB:Un-install C270
place 0.1uf close to pin1 and pin9 each
(PORT-C)
EMI Solution
FRONT I/O AUDIO
REAR I/O AUDIO
AUDIO CODEC
1000pf stitch cap for EMI, and place close to jack
ALC221 JACK DETECT
All of JD resistors should be placed as close as possible to the sense pin of codec.
AUDIO AMPLIFIER ENABLE
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AUDIO CODEC REGULATORS

PN: I31-5156B09-A30

+12V
R923 0/4 NI
U68 NI CRITICAL APL5156-SOT23-5-HF
U88_VIN
C279 NI 10uF/16V/X5R/8
VIN VOUT GND EN ADJ
5V_AVDD_EN
AGND
+5V_AUX
CRITICAL D21 ESD-TVNS52301AB0-RH
FB11 NI 220Ohm/1800mA/0.08Ohm/8
+5V_AVDD
R379 NI 309K/4/1
R1
5V_AVDD_ADJ
R380 NI 100K/4/1
R2
C281
C282 0.1u16X/4
C285 NI 0.1uF/25V/Y5V/6
10uF/16V/X5R/8
U88_VIN R382 NI 1K/4
14,23,36,47,48,55 SLP_S3# R383 NI 1K/4

SPEAKER HEADER

P/N:N32-1020521-F02

34 SPK_OUT- R377 0/8 MONO_OUT-
34 SPK_OUT+ R381 0/8 MONO_OUT+
C278 NI 100p50N-HF
C284 NI 100p50N-HF
C280 NI 1u16X-HF
R378 NI 100K/4/1
MONO_RC
C283 NI 470pF/50V/X7R/4
P6
BH1X2H-2.5PITCH_WHITE-HF

TABLE 14
SPEAKER HEADER DEFINITION

P6	
SPEAKER-	1
SPEAKER+	2

SPK+- TRACE WIDTH
Speaker 4 ohm ==> 40mils
Speaker 8 ohm ==> 20mils

Azalia Front Audio Connector

N31-2051491-H06

LINE1_VREFO_L R384 4.7K/4
LINE1_VREFO_R R385 4.7K/4
34 LINE1_VREFO
D22 S-BAT54A-7-02-F_SOT23-3-HF

34 FRONT_MIC_R C286 4.7uF/10V/X5R/8 R386 75R1%0402
34 FRONT_MIC_L C287 4.7uF/10V/X5R/8 R387 75R1%0402
Port-C
R388 22K/4
R389 22K/4
D23 CRITICAL ESD-SFI0402ML080C-LF-HF
D24 CRITICAL ESD-SFI0402ML080C-LF-HF
+3.3V
R390 10K/4
R391 NI 0/6
R392 0/6
C288 1000p50X/4
P23
H2X5[8]M_BLUE-HF-1
BLUE
FRONT_AUD_DET#
C289 100pF/50V/NPO/4

34 HP_R R393 75/4/1
34 HP_L R394 75/4/1
Port-I
D25 D26 CRITICAL ESD-SFI0402ML080C-LF-HF

Place those component close to audio connector.

Rear audio jack

J78 | Double-stacked audio jack | line-in (top), headphone/line-out (bottom)

MIC2_VREFO_R R395 4.7K/4
MIC2_VREFO_L R396 4.7K/4
recommend place Mic bias resistor close to code
34 MIC2_VREFO
D27 S-BAT54A-7-02-F_SOT23-3-HF

34 REAL_LINE-IN_L R397 1K/4
34 REAL_LINE-IN_R R398 1K/4
Port-E
J78A
LINE_IN_L_REAL
LINE_IN_R_REAL
SA_C
34 SA_C
JACK-AUDIOX2F_GR/BU-HF-1
LITE BLUE
D28 D29 CRITICAL ESD-SFI0402ML080C-LF-HF

34 LINE_FOUTL R399 75/4/1
34 LINE_FOUTR R400 75/4/1
Port-D
J78B
LINE_OUT_L_REAL
LINE_OUT_R_REAL
SA_D
34 SA_D
JACK-AUDIOX2F_GR/BU-HF-1
GREEN
D30 D31 CRITICAL ESD-SFI0402ML080C-LF-HF
C290 NI 470pF/50V/X7R/4
C291 NI 470pF/50V/X7R/4
FOR EMI
N54-09F0331-L06

D23,D24,D25,D26,D28,D29,D30,D31
D0G-2950500-SI0
AVL:D0G-3010510-I05

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Title AUDIO CONNECTOR
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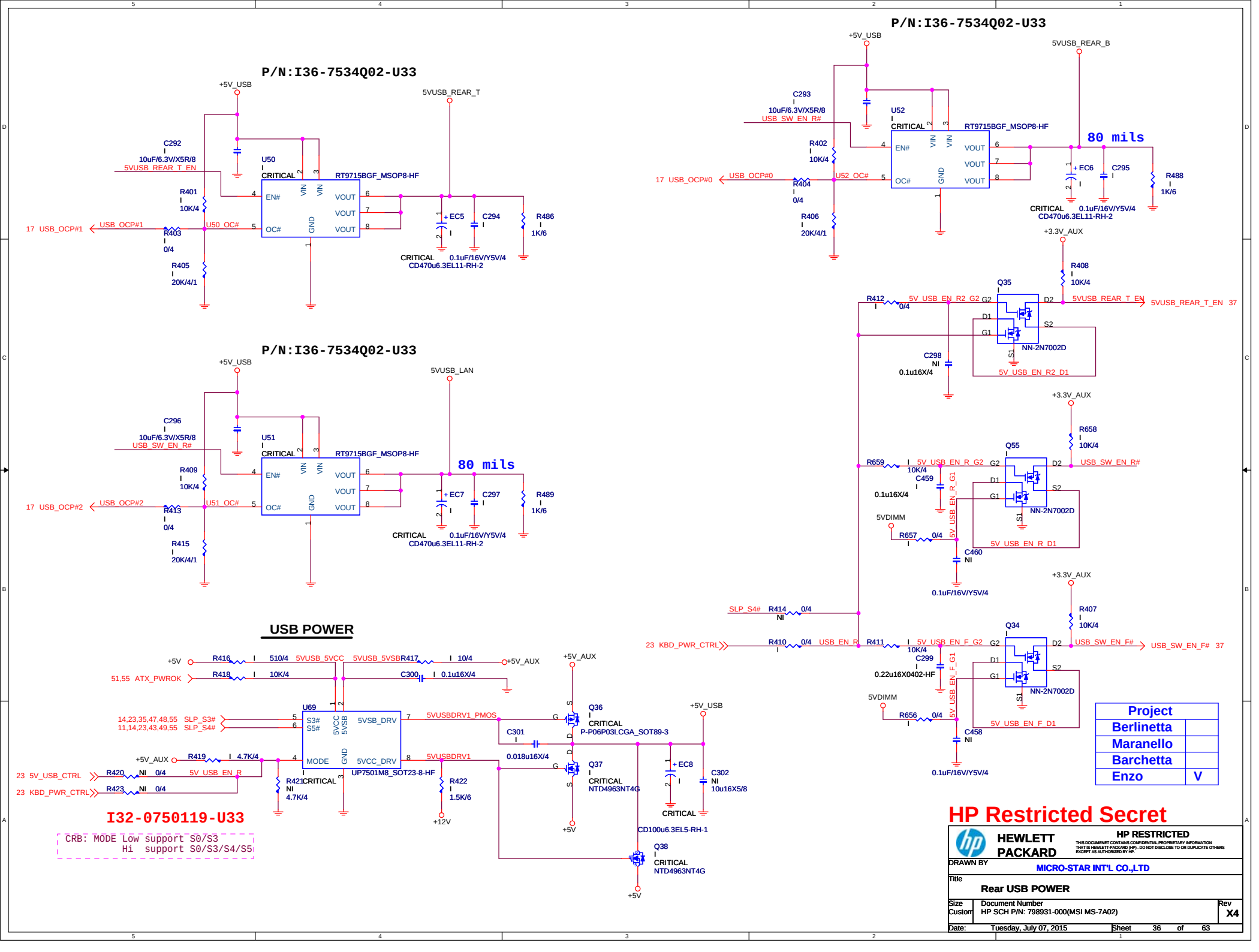
P/N:I36-7534Q02-U33
+5V_USB
5VUSB_REAR_T
C292
10uF/6.3V/X5R/8
5VUSB_REAR_T_EN
U50
CRITICAL
RT9715BGF_MSOP8-HF
R401
10K/4
EN#
VIN
VOUT
GND
OC#
17 USB_OCP#1
USB_OCP#1
U50_OC#
R403
0/4
R405
20K/4/1
+ EC5
C294
R486
1K/6
CRITICAL
0.1uF/16V/Y5V/4
CD470u6.3EL11-RH-2
P/N:I36-7534Q02-U33
+5V_USB
5VUSB_LAN
C296
10uF/6.3V/X5R/8
USB_SW_EN_R#
U51
CRITICAL
RT9715BGF_MSOP8-HF
R409
10K/4
17 USB_OCP#2
USB_OCP#2
U51_OC#
R413
0/4
R415
20K/4/1
80 mils
+ EC7
C297
R489
1K/6
CRITICAL
0.1uF/16V/Y5V/4
CD470u6.3EL11-RH-2
USB POWER
+5V
R416
510/4
5VUSB_5VCC
5VUSB_5VSB
R417
10/4
+5V_AUX
51,55 ATX_PWROK
R418
10K/4
C300
0.1u16X/4
U69
14,23,35,47,48,55 SLP_S3#
11,14,23,43,49,55 SLP_S4#
S3#
S5#
5VCC
5VSB
5VSB_DRV
5VUSBDRV1_PMOS
MODE
5VCC_DRV
UP7501M8_SOT23-8-HF
5VUSBDRV1
+5V_AUX
R419
4.7K/4
23 5V_USB_CTRL
R420
NI
0/4
5V_USB_EN_R
23 KBD_PWR_CTRL
R423
NI
0/4
R421
CRITICAL
NI
4.7K/4
R422
1.5K/6
+12V
C301
0.018u16X/4
Q36
CRITICAL
P-P06P03LCGA_SOT89-3
Q37
CRITICAL
NTD4963NT4G
+5V_USB
+ EC8
C302
NI
10u16X5/8
CRITICAL
CD100u6.3EL5-RH-1
Q38
CRITICAL
NTD4963NT4G
+5V
I32-0750119-U33
CRB: MODE Low support S0/S3
Hi support S0/S3/S4/S5
P/N:I36-7534Q02-U33
+5V_USB
5VUSB_REAR_B
C293
10uF/6.3V/X5R/8
USB_SW_EN_R#
U52
CRITICAL
RT9715BGF_MSOP8-HF
R402
10K/4
17 USB_OCP#0
USB_OCP#0
U52_OC#
R404
0/4
R406
20K/4/1
80 mils
+ EC6
C295
R488
1K/6
CRITICAL
0.1uF/16V/Y5V/4
CD470u6.3EL11-RH-2
+3.3V_AUX
R408
10K/4
Q35
R412
0/4
5V_USB_EN_R2_G2
5VUSB_REAR_T_EN
5VUSB_REAR_T_EN 37
NN-2N7002D
C298
NI
0.1u16X/4
5V_USB_EN_R2_D1
+3.3V_AUX
R658
10K/4
Q55
R659
10K/4
5V_USB_EN_R_G2
USB_SW_EN_R#
C459
0.1u16X/4
5V_USB_EN_R_G1
NN-2N7002D
5VDIMM
R657
0/4
5V_USB_EN_R_D1
C460
NI
0.1uF/16V/Y5V/4
+3.3V_AUX
R407
10K/4
SLP_S4#
R414
0/4
NI
23 KBD_PWR_CTRL
R410
0/4
USB_EN_R
R411
10K/4
5V_USB_EN_F_G2
Q34
USB_SW_EN_F#
USB_SW_EN_F# 37
C299
0.22u16X0402-HF
5V_USB_EN_F_G1
NN-2N7002D
5VDIMM
R656
0/4
5V_USB_EN_F_D1
C458
NI
0.1uF/16V/Y5V/4
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Rear USB POWER
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Custom
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Rev
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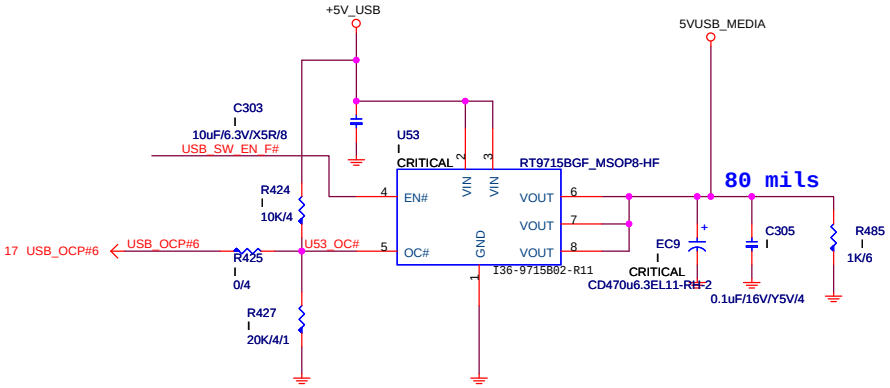
Date:
Tuesday, July 07, 2015
Sheet
36
of
63

P/N:I36-9715B02-R11



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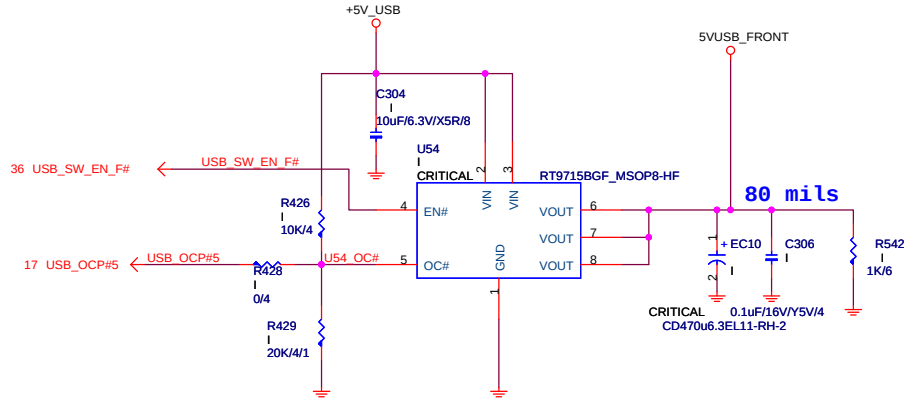

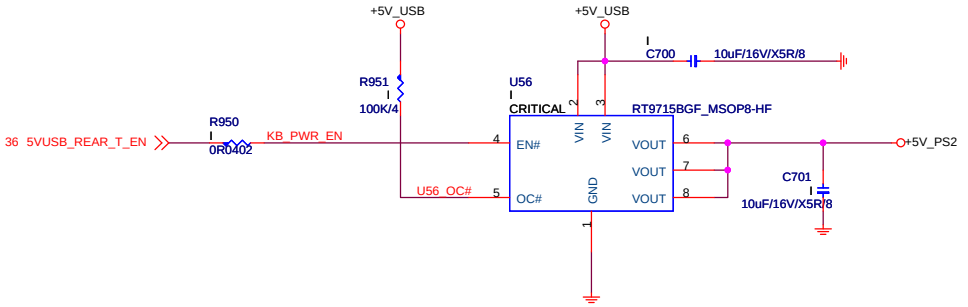

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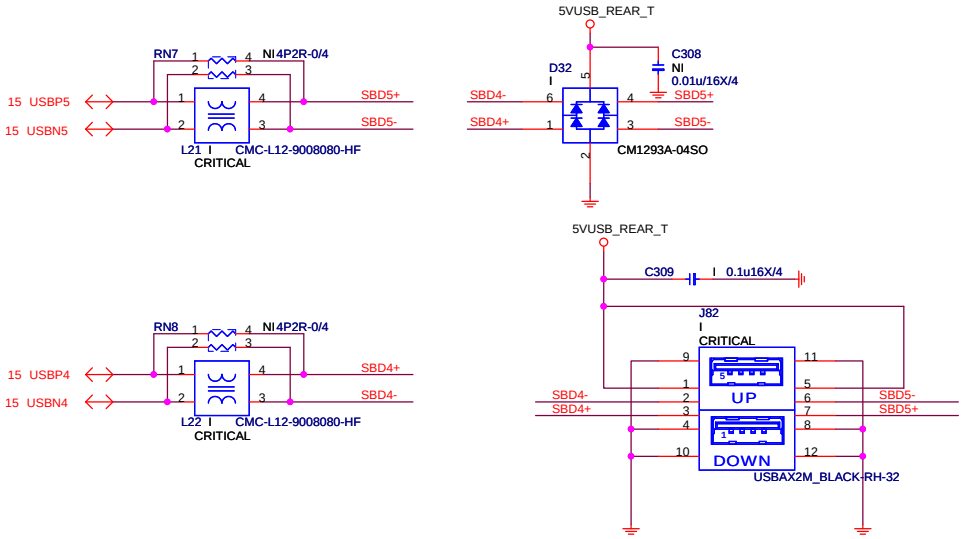
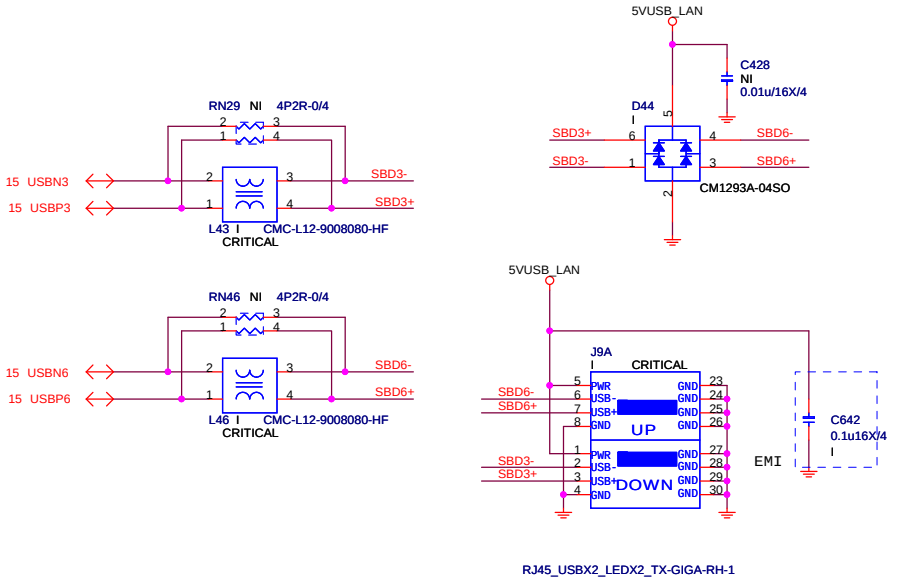
Rear USB Connnector For USB Port 4 / 5

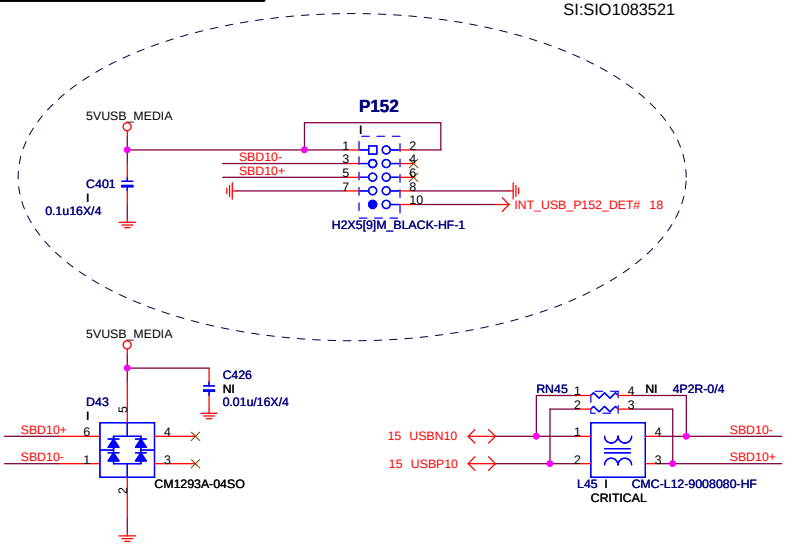


REAR USB2.0 Connnector For USB2.0 Port 1 /2



MEDIA USB2.0 Connnector

SI:SIO1083521



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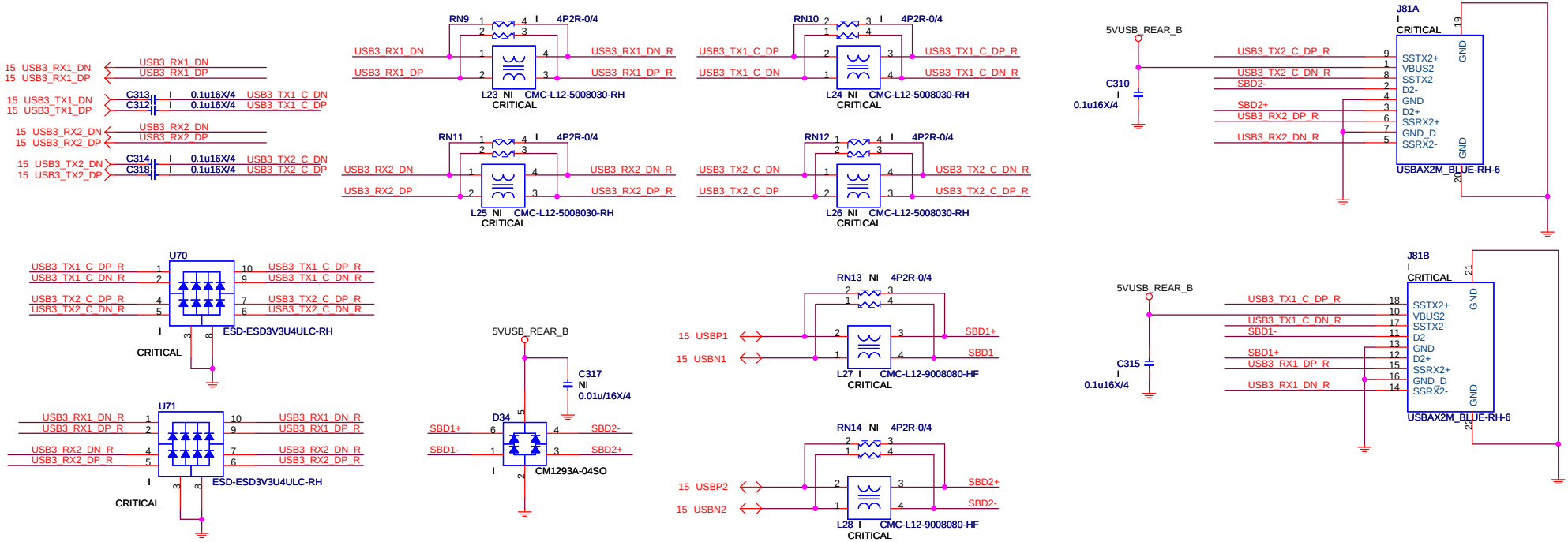
REAR USB3.0 Connnector



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FRONT USB3.0 Connnector

15 USB3_RX3_DN ← USB3_RX3_DN
15 USB3_RX3_DP ← USB3_RX3_DP
15 USB3_TX3_DN — C325 0.1u16X/4 — USB3_TX3_C_DN
15 USB3_TX3_DP — C326 0.1u16X/4 — USB3_TX3_C_DP
15 USB3_RX4_DN ← USB3_RX4_DN
15 USB3_RX4_DP ← USB3_RX4_DP
15 USB3_TX4_DN — C327 0.1u16X/4 — USB3_TX4_C_DN
15 USB3_TX4_DP — C328 0.1u16X/4 — USB3_TX4_C_DP

5VUSB_FRONT
C329 NI 0.01u/16X/4
D35 CM1293A-04SO
SBD8+ SBD8- SBD9- SBD9+

15 USBN8 ↔ RN25 NI 4P2R-0/4 ↔ SBD8-
15 USBP8 ↔ SBD8+
L39 CMC-L12-9008080-HF CRITICAL

U74 ESD-ESD3V3U4ULC-RH CRITICAL
USB3_RX3_DP_R / USB3_RX3_DN_R → USB3_RX3_DP_R / USB3_RX3_DN_R
USB3_RX4_DP_R / USB3_RX4_DN_R → USB3_RX4_DP_R / USB3_RX4_DN_R

U75 ESD-ESD3V3U4ULC-RH CRITICAL
USB3_TX4_C_DN_R / USB3_TX4_C_DP_R → USB3_TX4_C_DN_R / USB3_TX4_C_DP_R
USB3_TX3_C_DN_R / USB3_TX3_C_DP_R → USB3_TX3_C_DN_R / USB3_TX3_C_DP_R

RN21 4P2R-0/4: USB3_TX4_C_DN → USB3_TX4_C_DN_R; USB3_TX4_C_DP → USB3_TX4_C_DP_R
CRITICAL L35 NI CMC-L12-5008030-RH

RN22 4P2R-0/4: USB3_TX3_C_DN → USB3_TX3_C_DN_R; USB3_TX3_C_DP → USB3_TX3_C_DP_R
CRITICAL L36 NI CMC-L12-5008030-RH

RN23 4P2R-0/4: USB3_RX4_DN → USB3_RX4_DN_R; USB3_RX4_DP → USB3_RX4_DP_R
CRITICAL L37 NI CMC-L12-5008030-RH

RN24 4P2R-0/4: USB3_RX3_DN → USB3_RX3_DN_R; USB3_RX3_DP → USB3_RX3_DP_R
CRITICAL L38 NI CMC-L12-5008030-RH

RN26 NI 4P2R-0/4
15 USBP9 ↔ SBD9+
15 USBN9 ↔ SBD9-
L40 CMC-L12-9008080-HF CRITICAL

5VUSB_FRONT
C324 0.1u16X/4
P26 BH2X10[20]-2PITCH_BLUE-RH-2 2X10_CONNECTOR

19	VBUS2		
18	RX2-	X1	USB3_RX3_DN_R
17	RX2+		USB3_RX3_DP_R
16	GND		
15	TX2-		USB3_TX3_C_DN_R
14	TX2+		USB3_TX3_C_DP_R
13	GND		
12	D2-		SBD9-
11	D2+		SBD9+
1	VBUS1		5VUSB_FRONT
2	RX1-		USB3_RX4_DN_R
3	RX1+		USB3_RX4_DP_R
4	GND		
5	TX1-		USB3_TX4_C_DN_R
6	TX1+		USB3_TX4_C_DP_R
7	GND		
8	D1-		SBD8-
9	D1+		SBD8+
10	DETECT#	X2	18 FRONT_USB_P26_DET#

C330 0.1u16X/4

N32-2101521-H06

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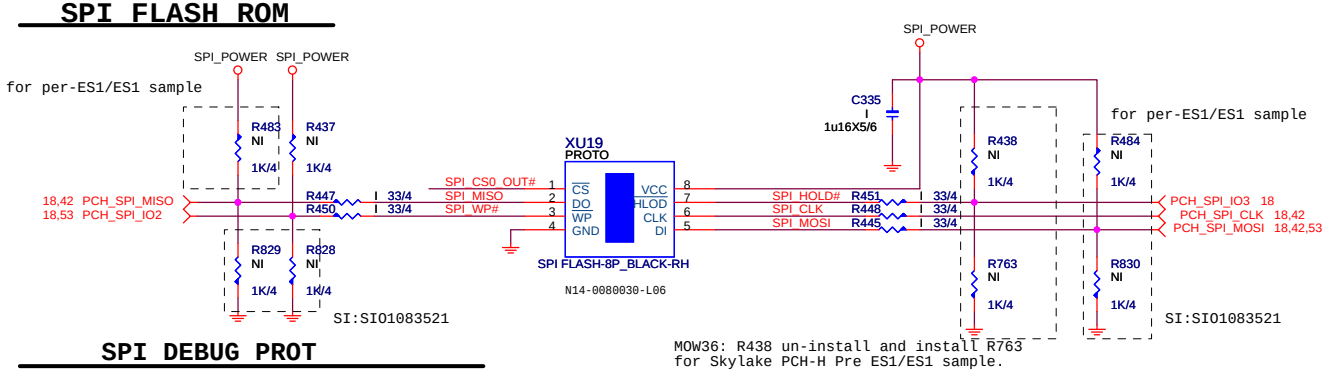
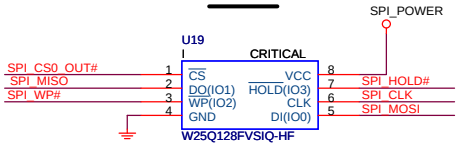
SPI FLASH ROM



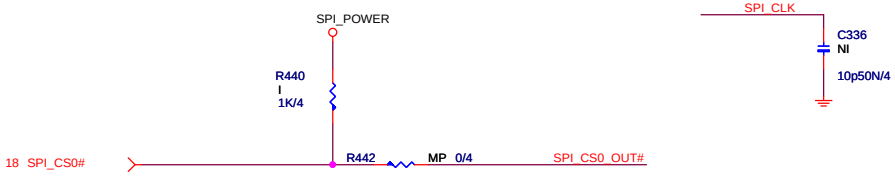
MOW36: R438 un-install and install R763
for Skylake PCH-H Pre ES1/ES1 sample.

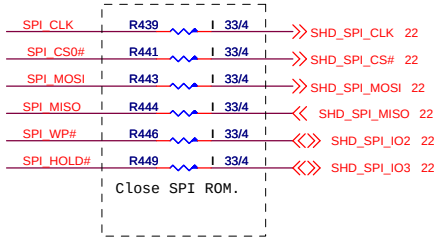
BIOS



M31-2512853-W03

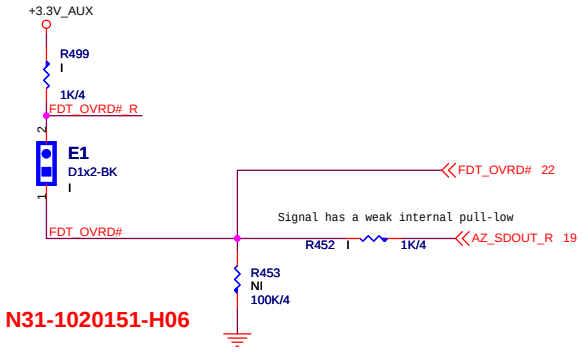
SPI DEBUG PROT





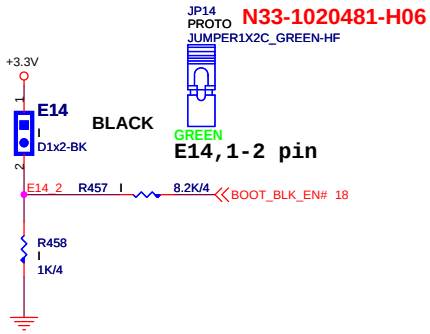
Flash Descriptor Override Header (ME_DIS)

FLASH DESCRIPTOR OVERRIDE

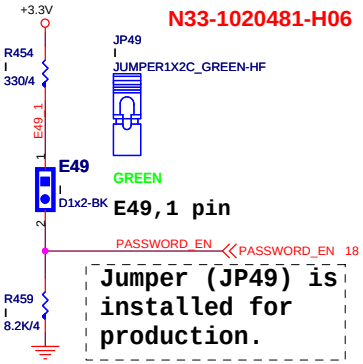


N31-1020151-H06

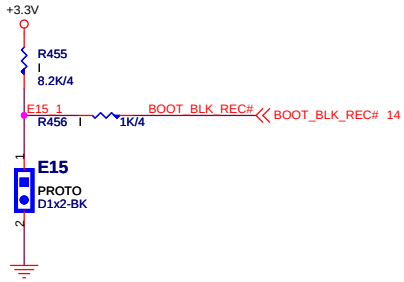
BOOT BLOCK WRITE JUMPER



PASSWORD JUMPER



BOOT BLOCK RECOVERY HEADER



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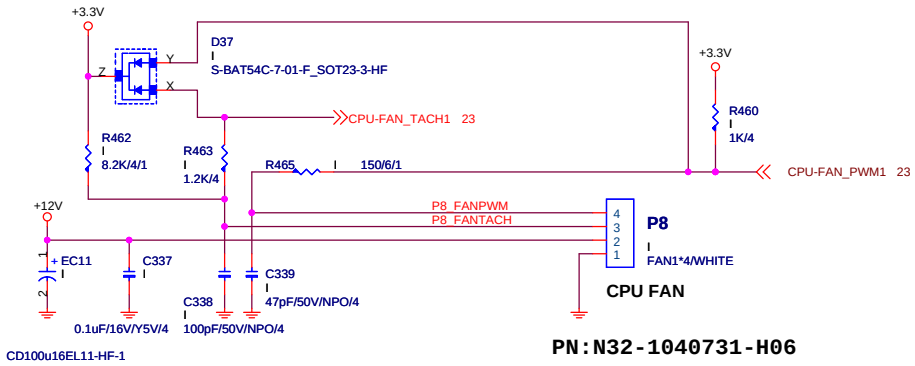
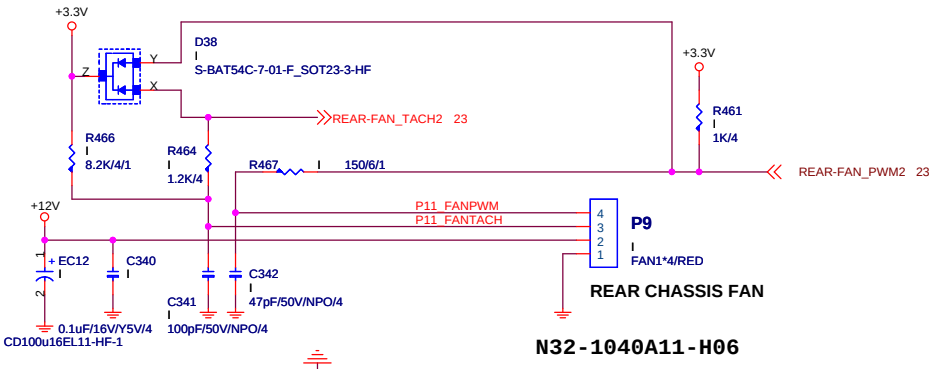
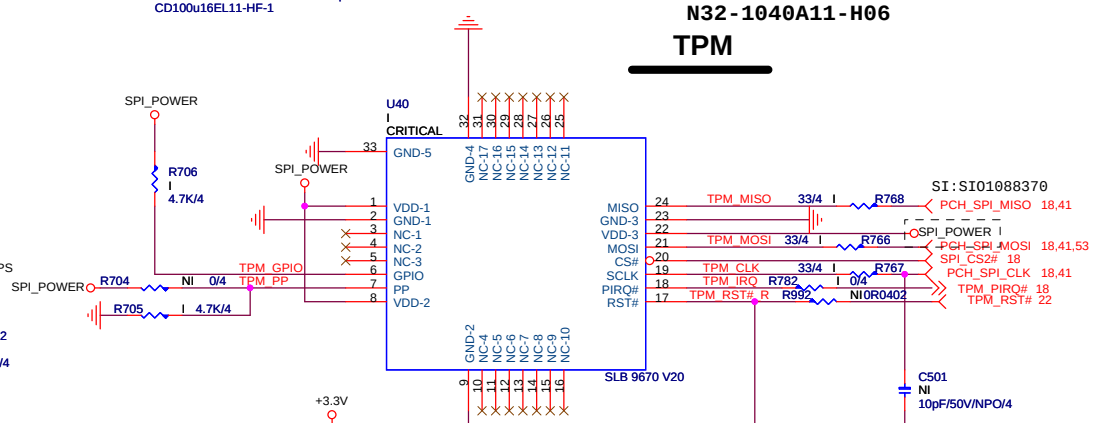
FAN BLOCK





TPM



+5V_USB_SUS_ACK

For board bring up, and to insure that the handshake circuit does not prevent the circuit from going into DeepSLeep, do the following:

R154 Installed

R470 Non-installed

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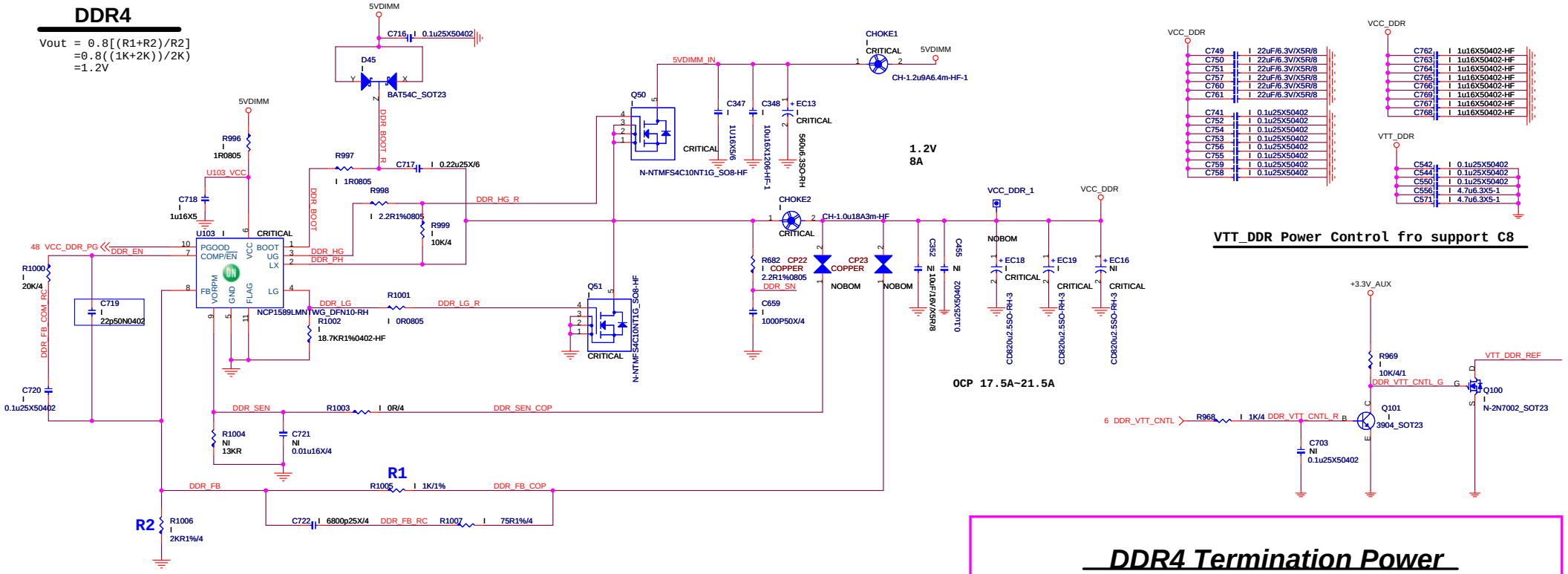
Date:	Monday, July 06, 2015
Sheet	42 of 63

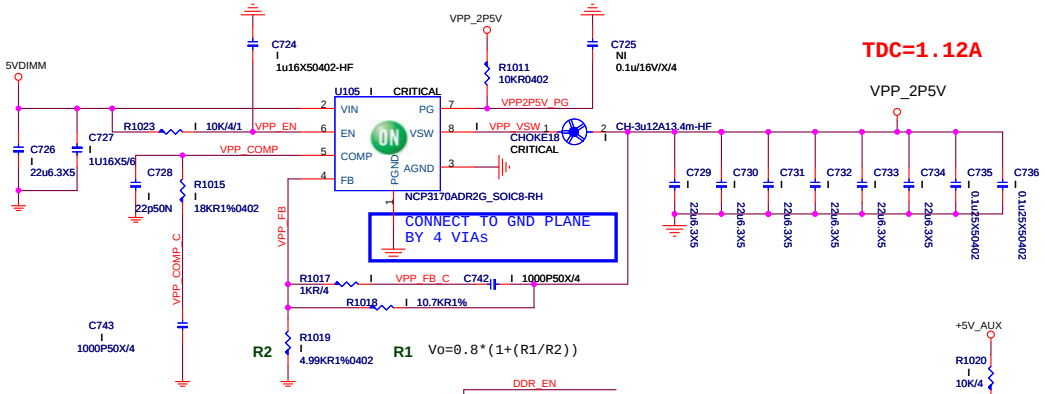
DDR4

Vout = 0.8[(R1+R2)/R2]
=0.8((1K+2K))/2K)
=1.2V



VTT_DDR Power Control fro support C8

VPP_2.5V

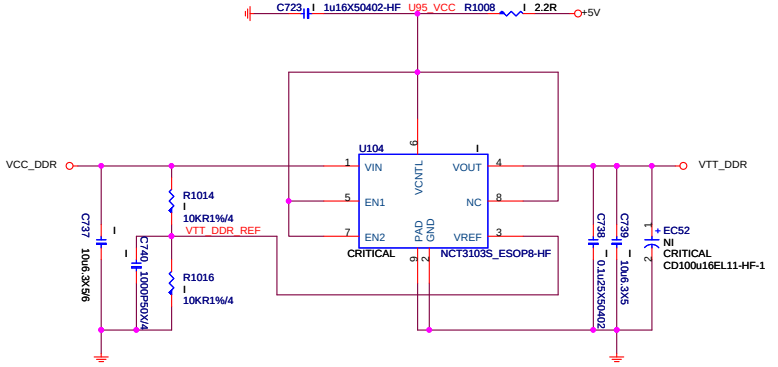


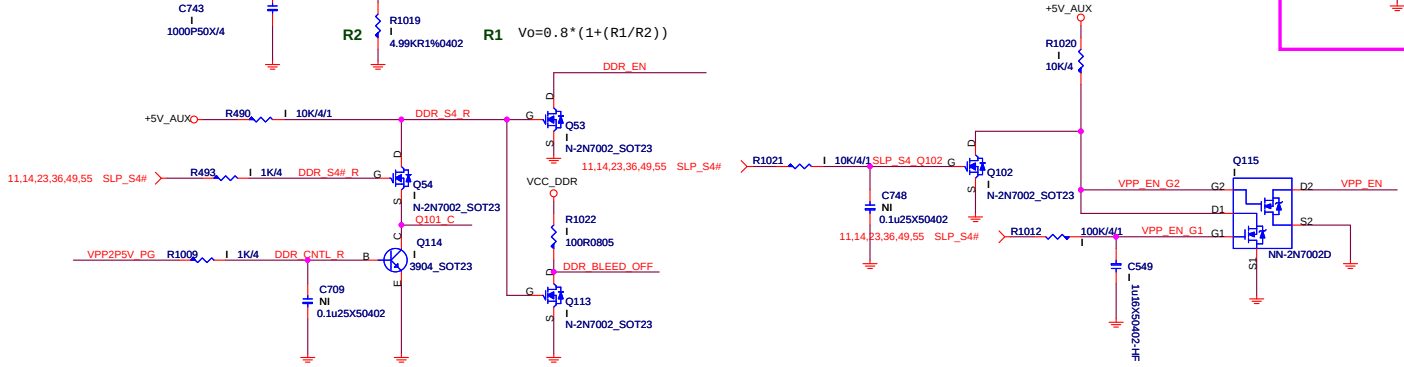
TDC=1.12A

VPP_2P5V

DDR4 Termination Power

0.6V - 0.6A





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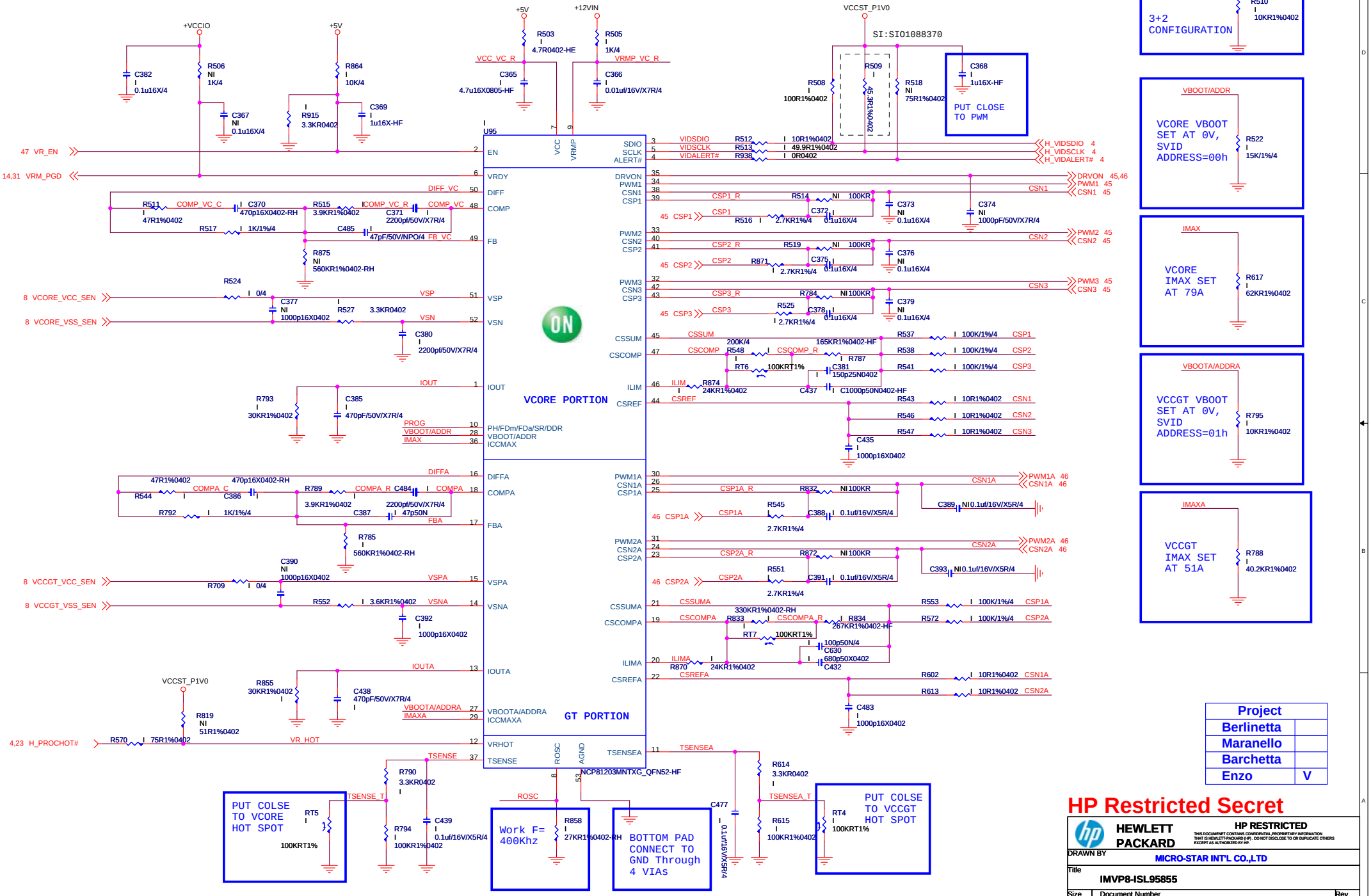
Intel SKYLAKE IMVP8 POWER CKT - 3+2 PHASE



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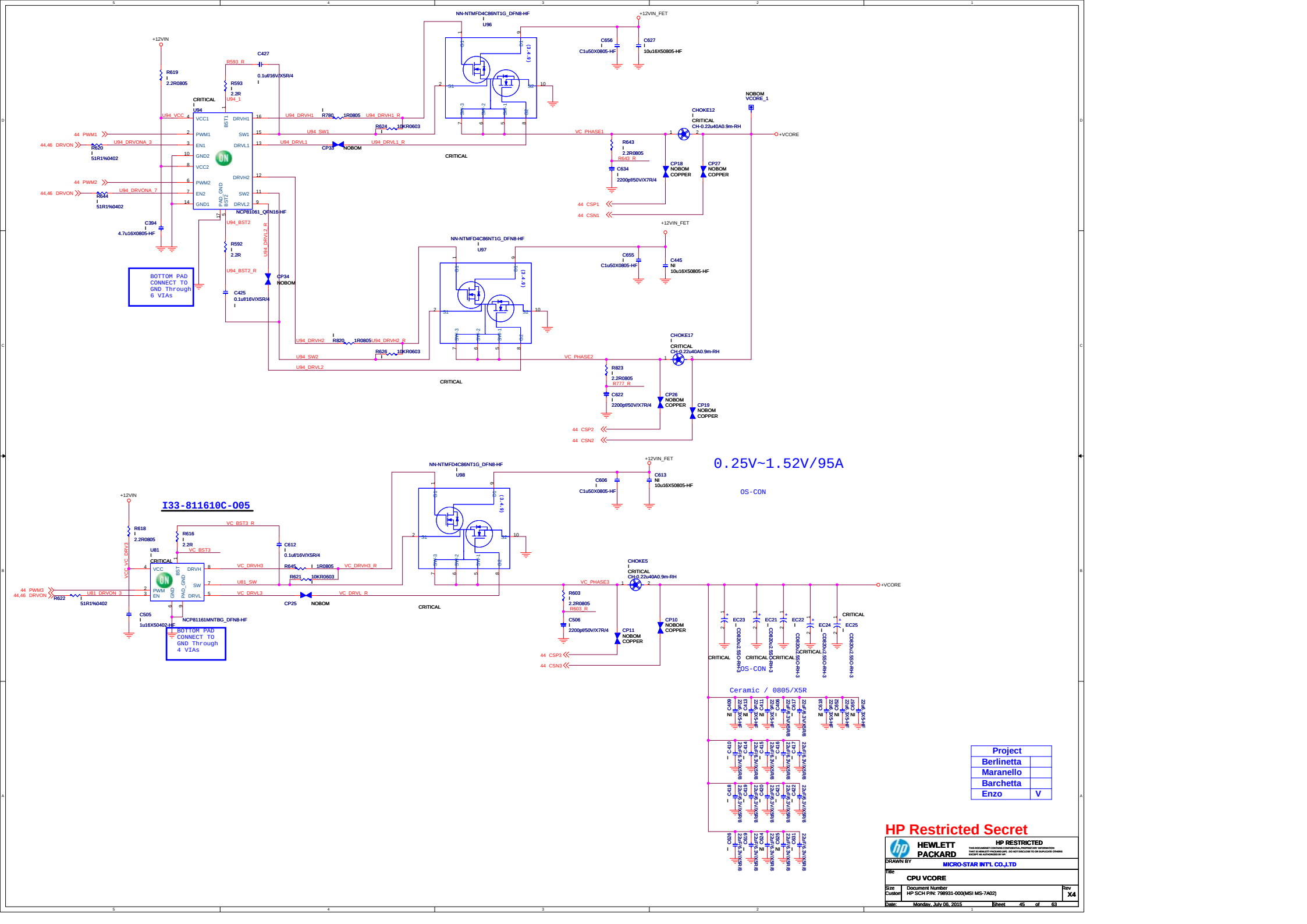

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Title CPU VCORE

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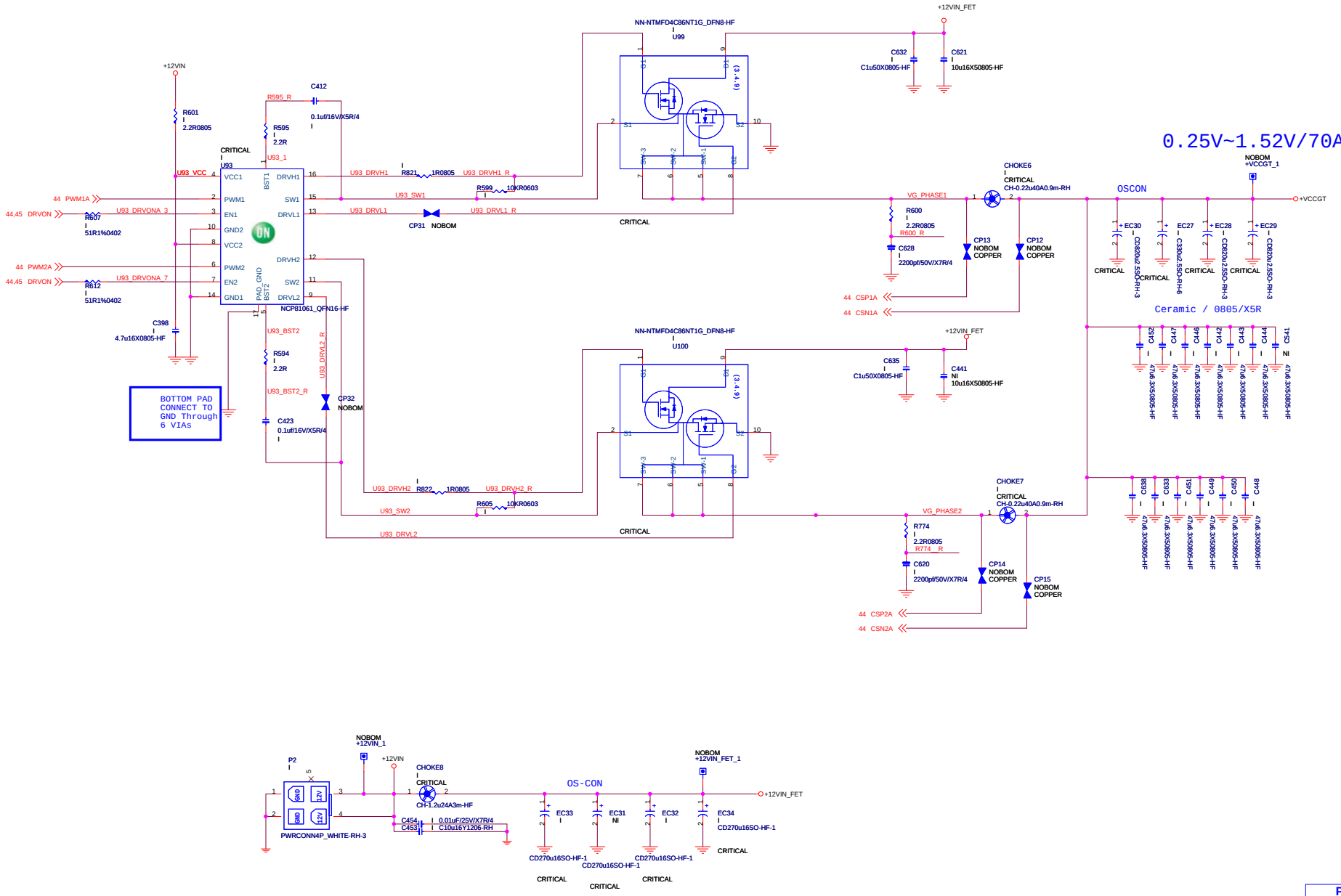

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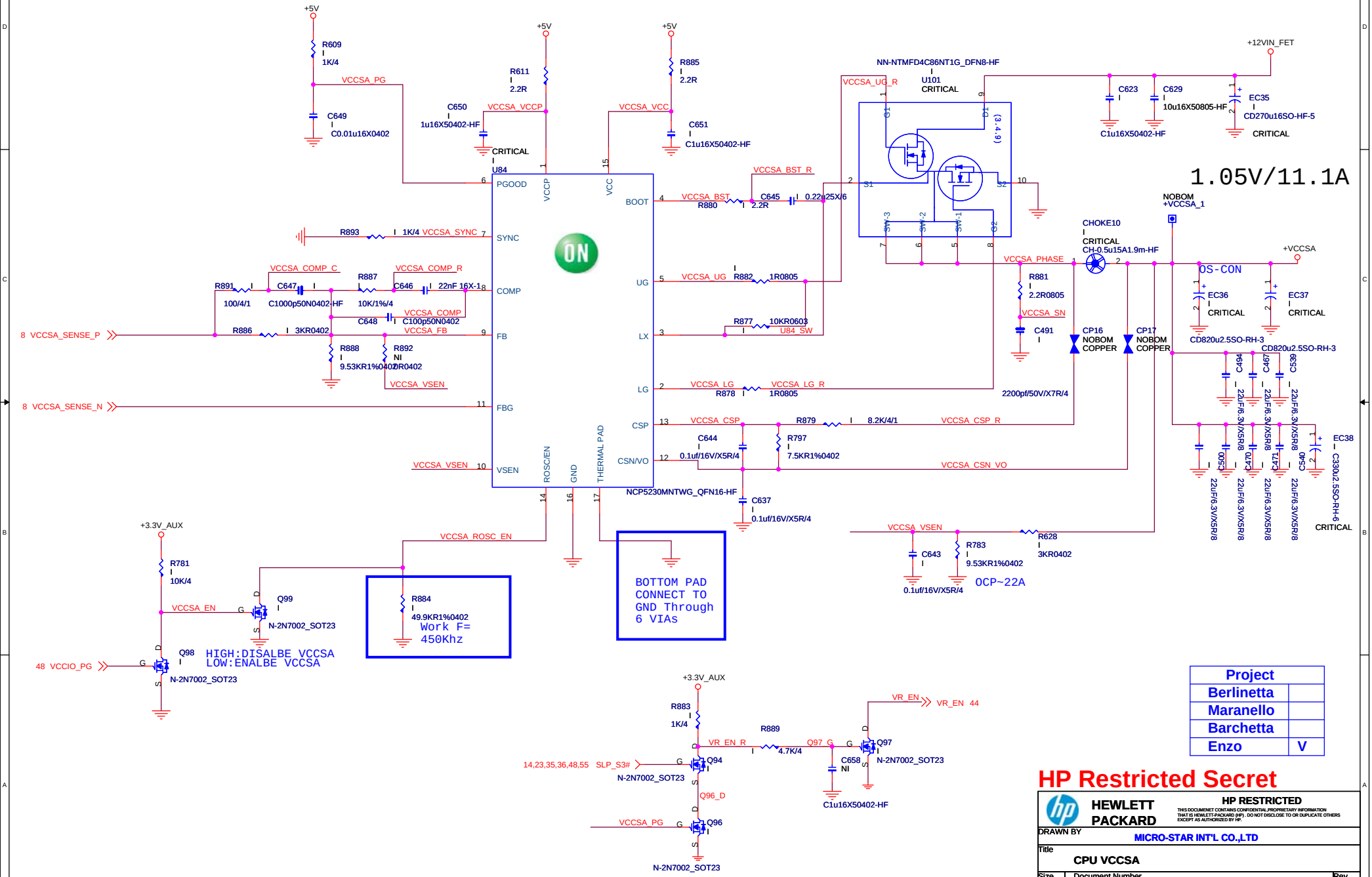
SKYLAKE VCCSA POWER CKT

I32-5230M0C-005



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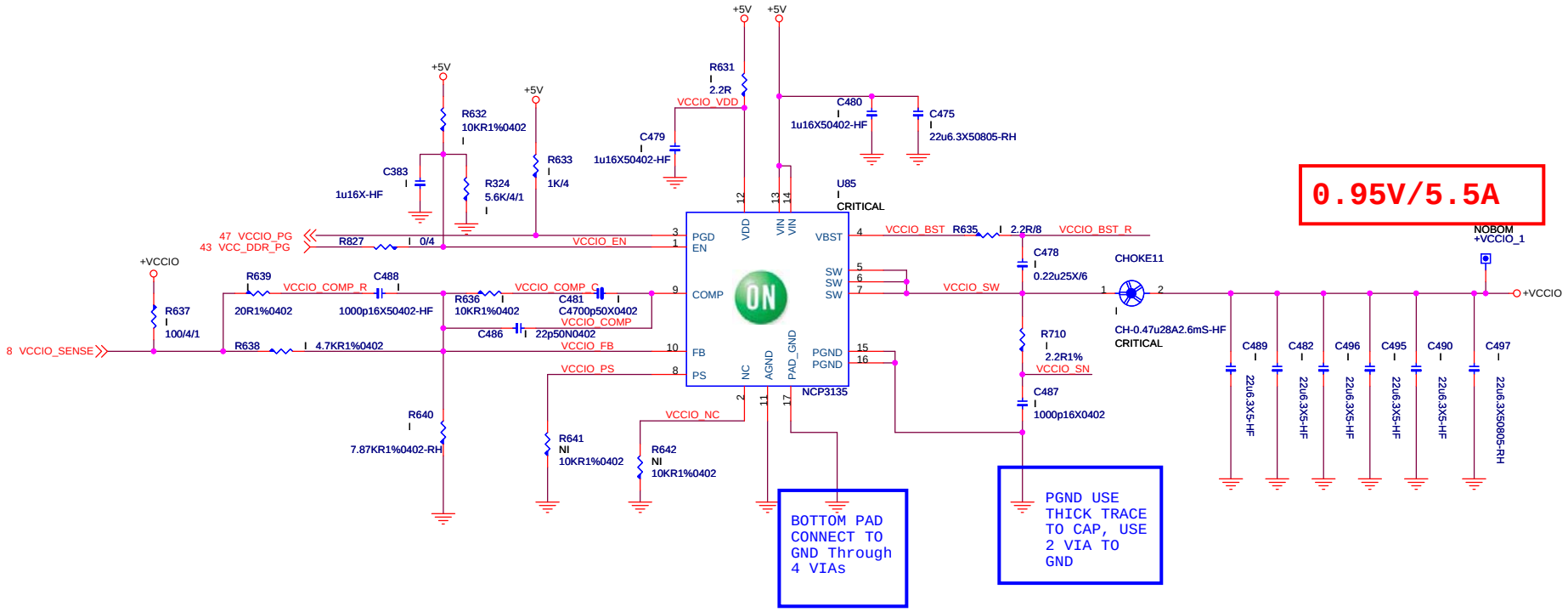
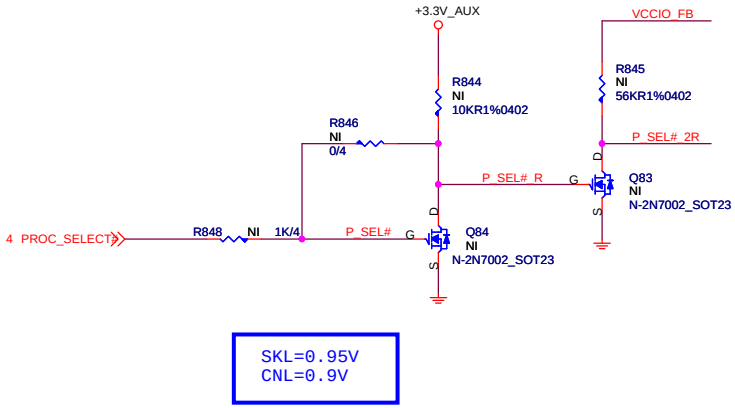
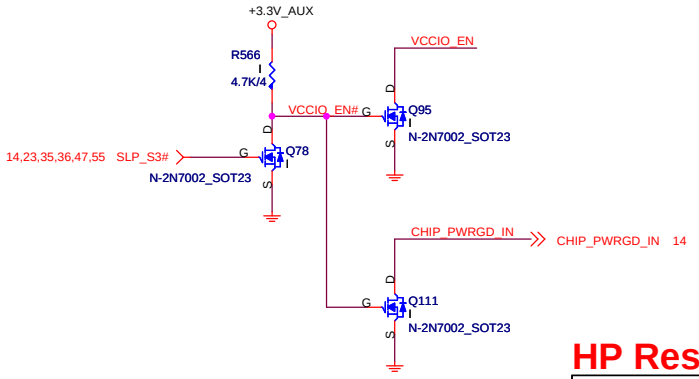
SKYLAKE VCCIO POWER CKT







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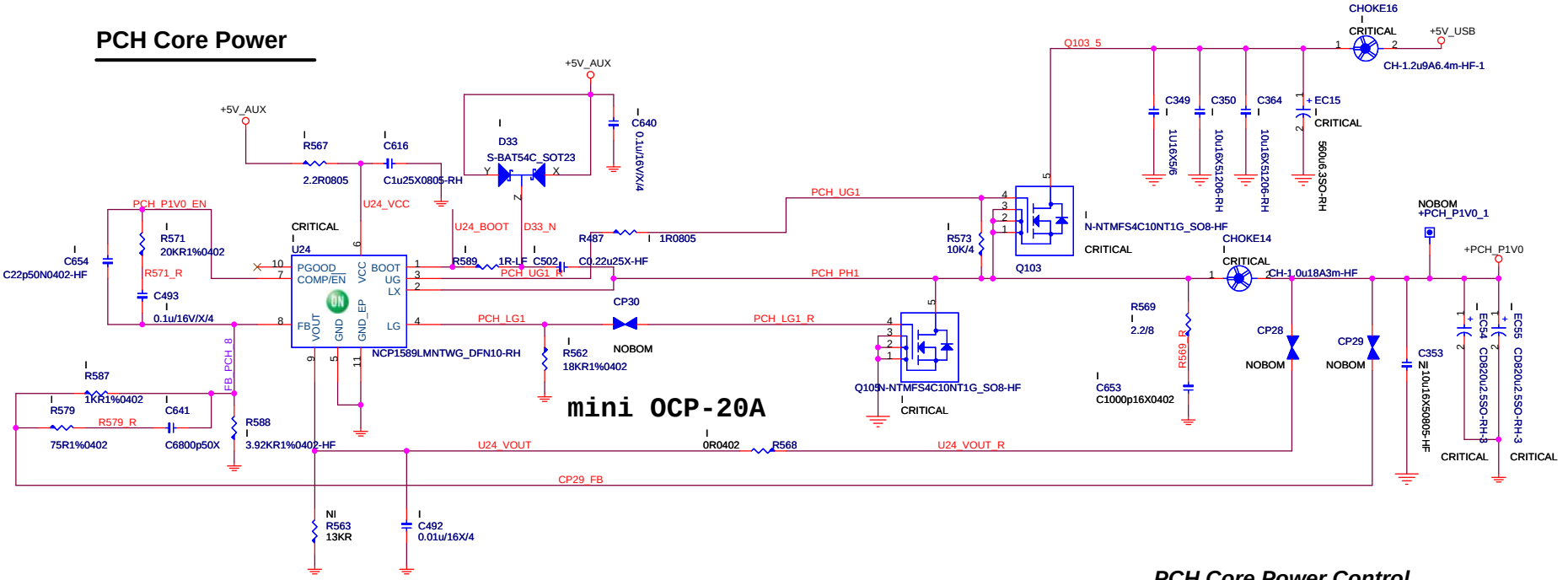
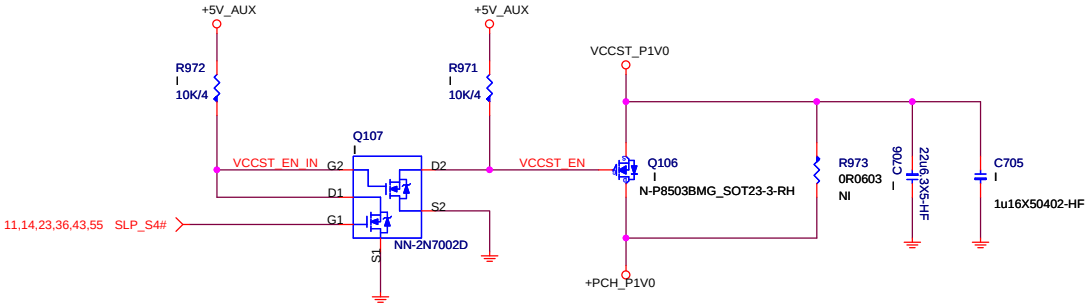
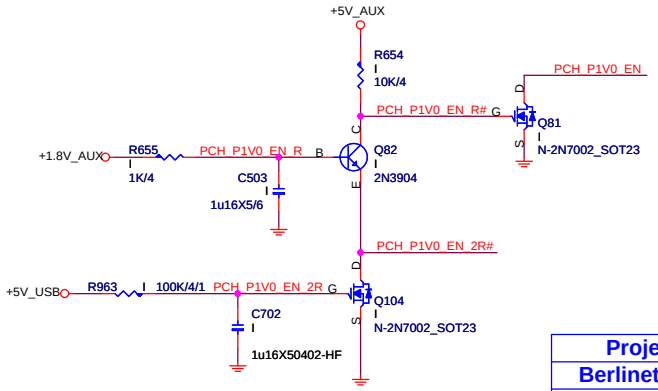
PCH Core Power



PCH Core Power Control





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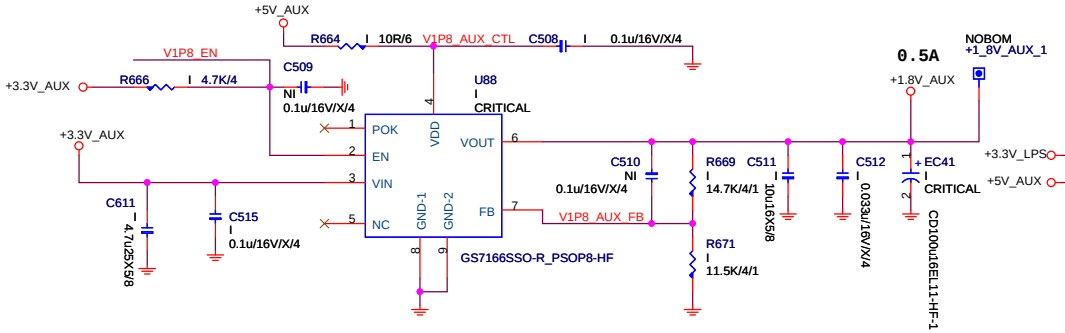
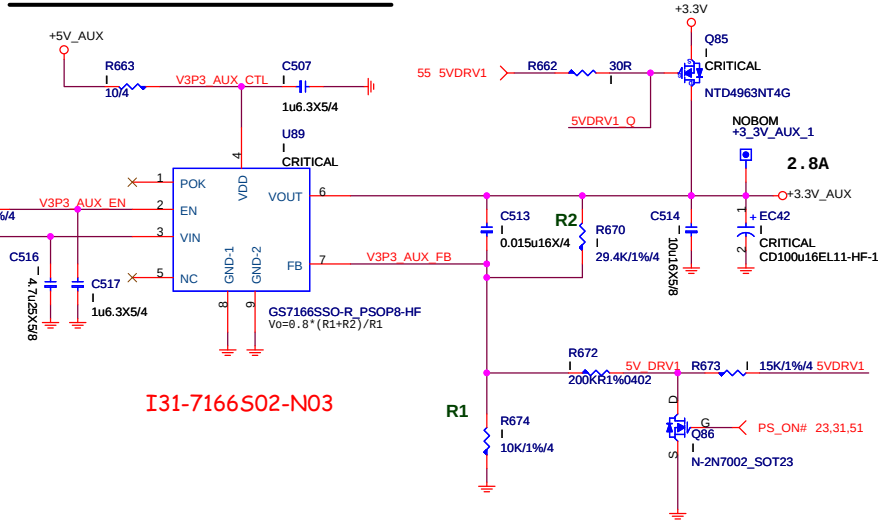
1.8V_AUX Power

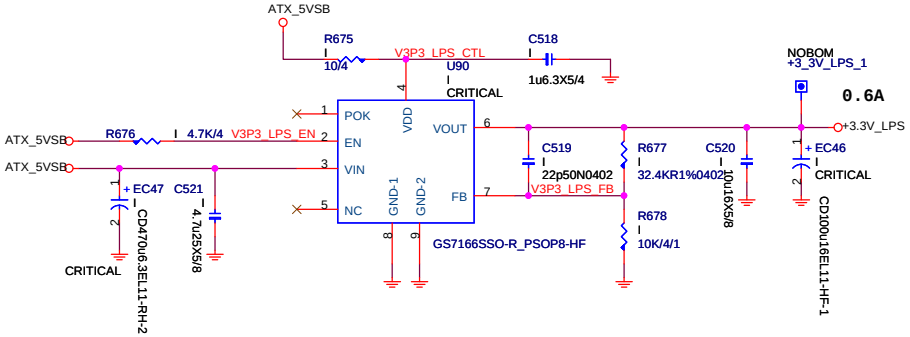


I31-7166S02-N03

3V Standby Power

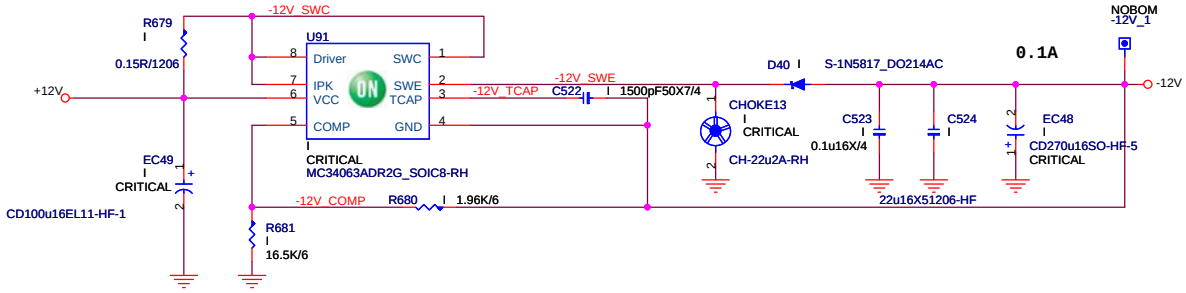


I31-7166S02-N03



I31-7166S02-N03

-12V POWER



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Title	-12V/+3.3V_AUX/+1.8V_AUX
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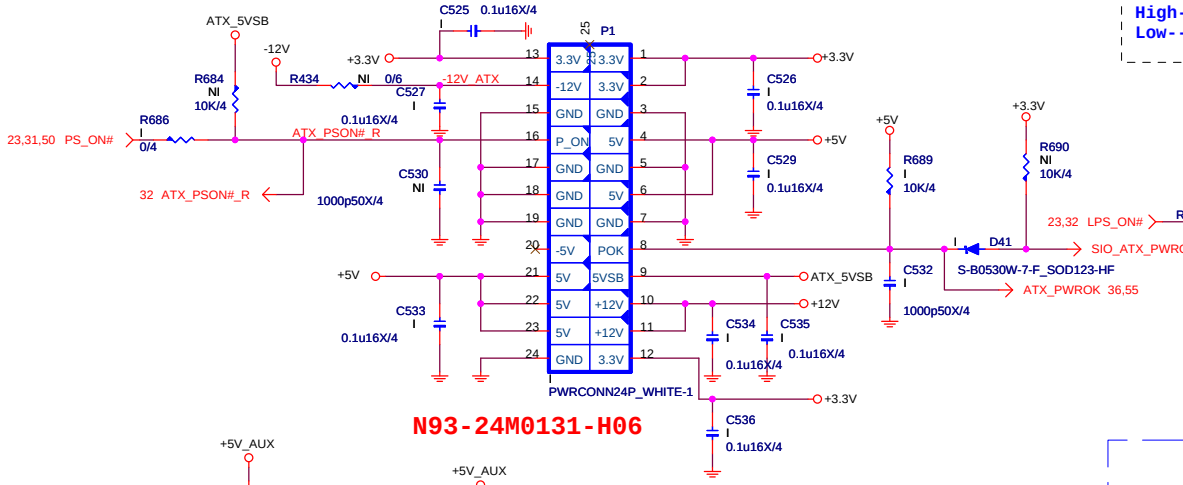
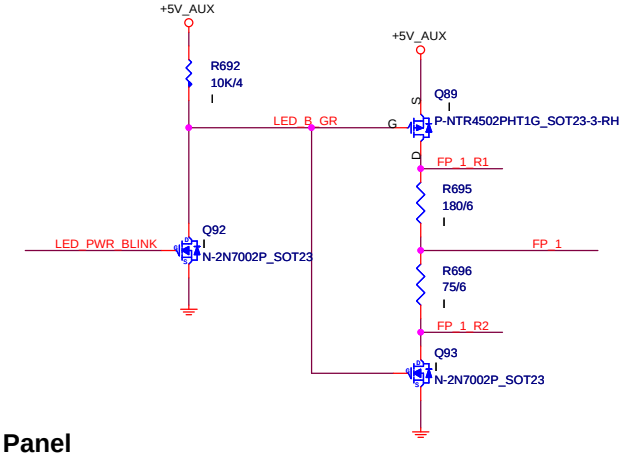
ATX Power Connector / Front Panel / LED/DSW

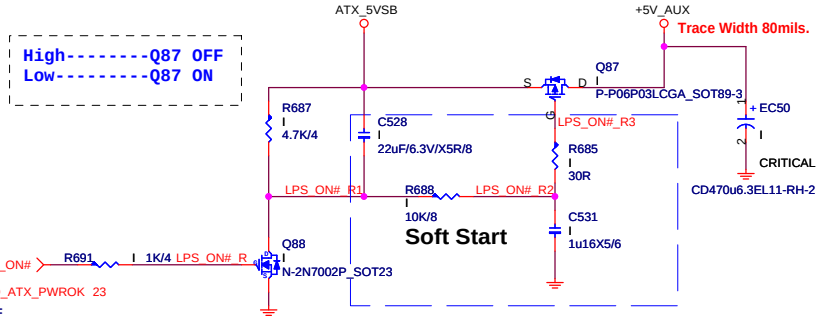
ATX CONNECTOR



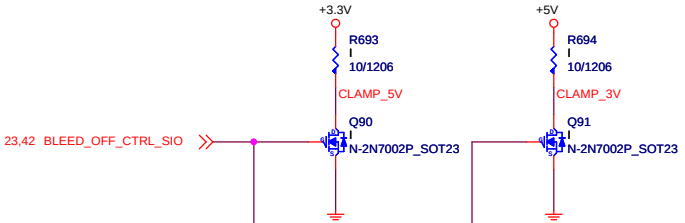
N93-24M0131-H06



+5V_AUX Power Switch

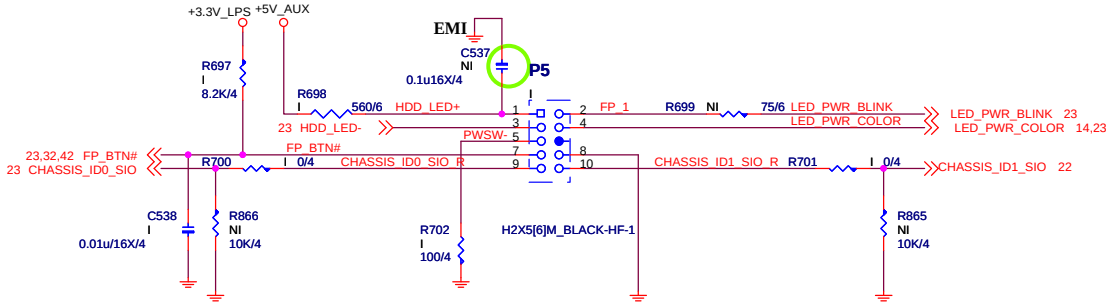


BLEED-OFF CIRCUIT



Front Panel

PN:N31-2051641-H06



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Title	ATX/F_Panel/EMI
Size: Custom	Document Number: HP SCH P/N: 798931-000(MSI MS-7A02)
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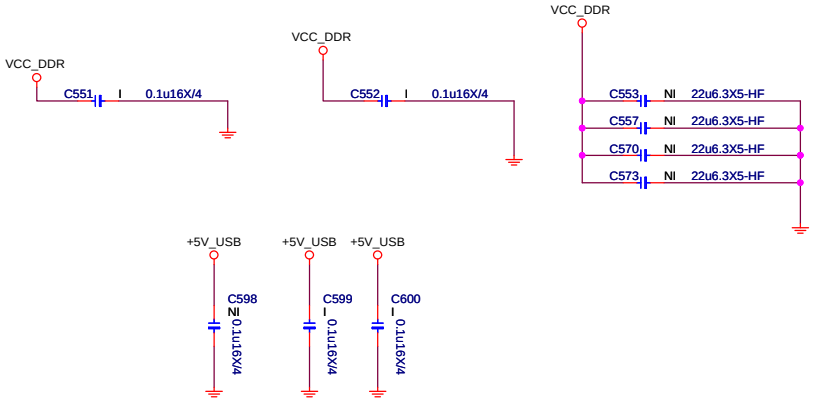
EMI CAPs



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Title: EMI cap

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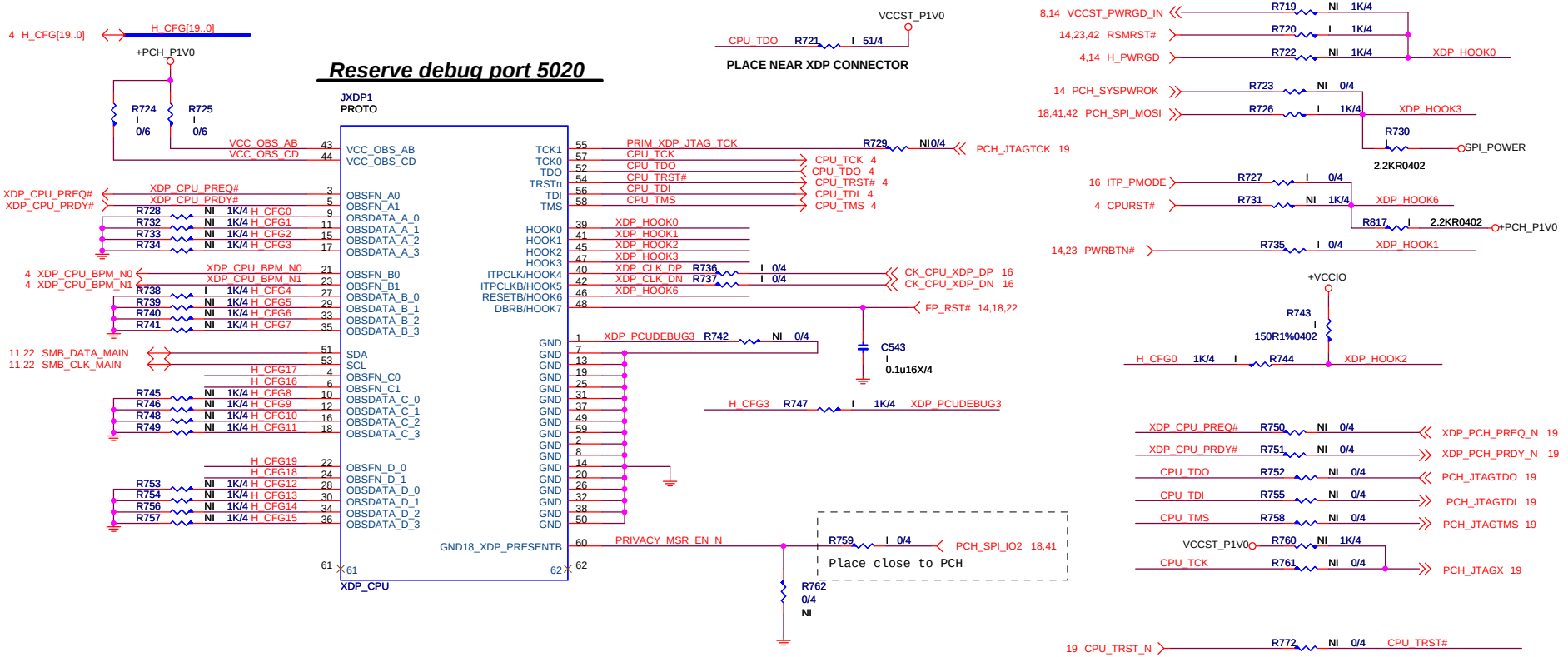

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Title: CPU/PCH/DMI XDP

Size	Document Number	Rev
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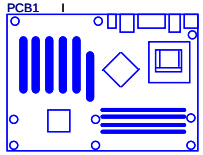
Manual Parts

PCB1 I

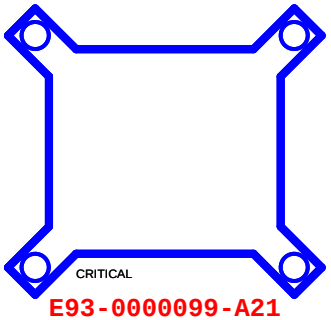


CRITICAL PCB1

XU1_X1

I

E93-0000099-A21

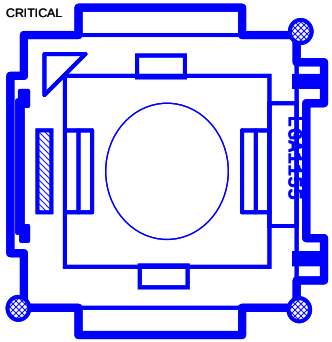


E93-0000099-A21
AVL:E22-B009010-C22

XU1_X2

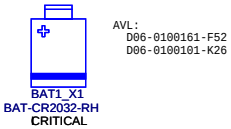
CPU SOCKET I

CRITICAL



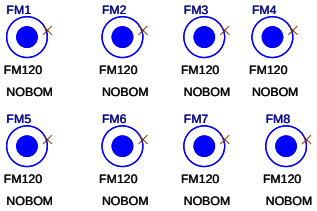
E21-AC71010-L06
AVL:E21-7826010-F02

Simulation

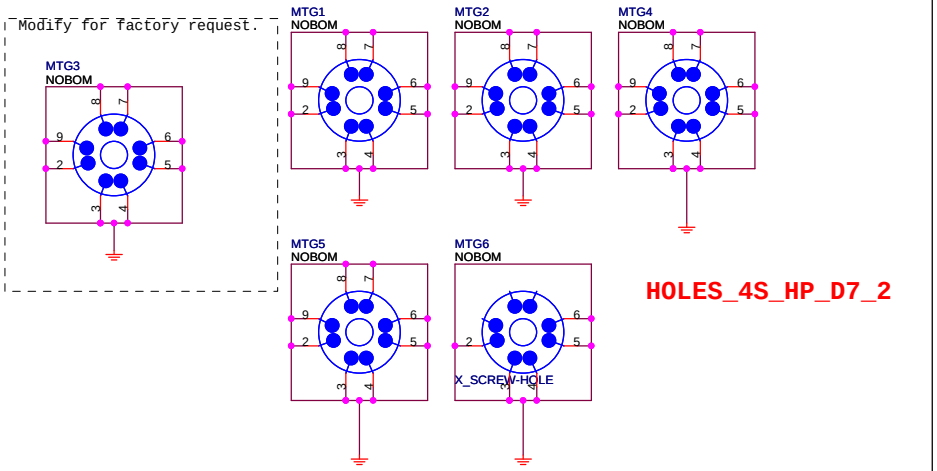


D06-0100101-P01

Optics Orientation Holes



Mounting Holes



HOLES_4S_HP_D7_2

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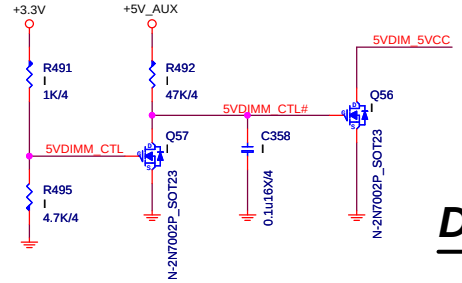
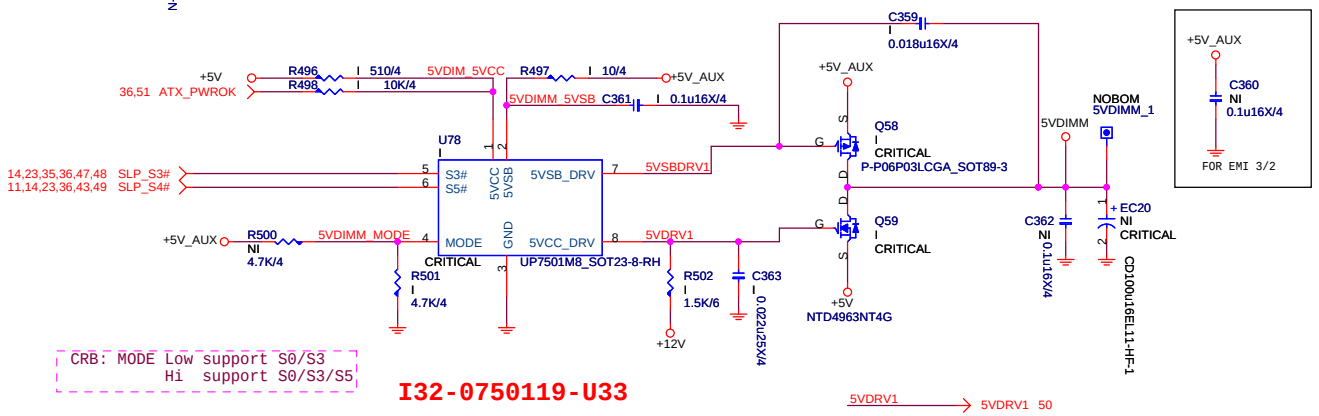
For special PSU sequence



DDR4 Regulator Power Source



CRB: MODE Low support S0/S3
Hi support S0/S3/S5

I32-0750119-U33

5VDRV1 → 5VDRV1 50

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Title: 5VDIMM

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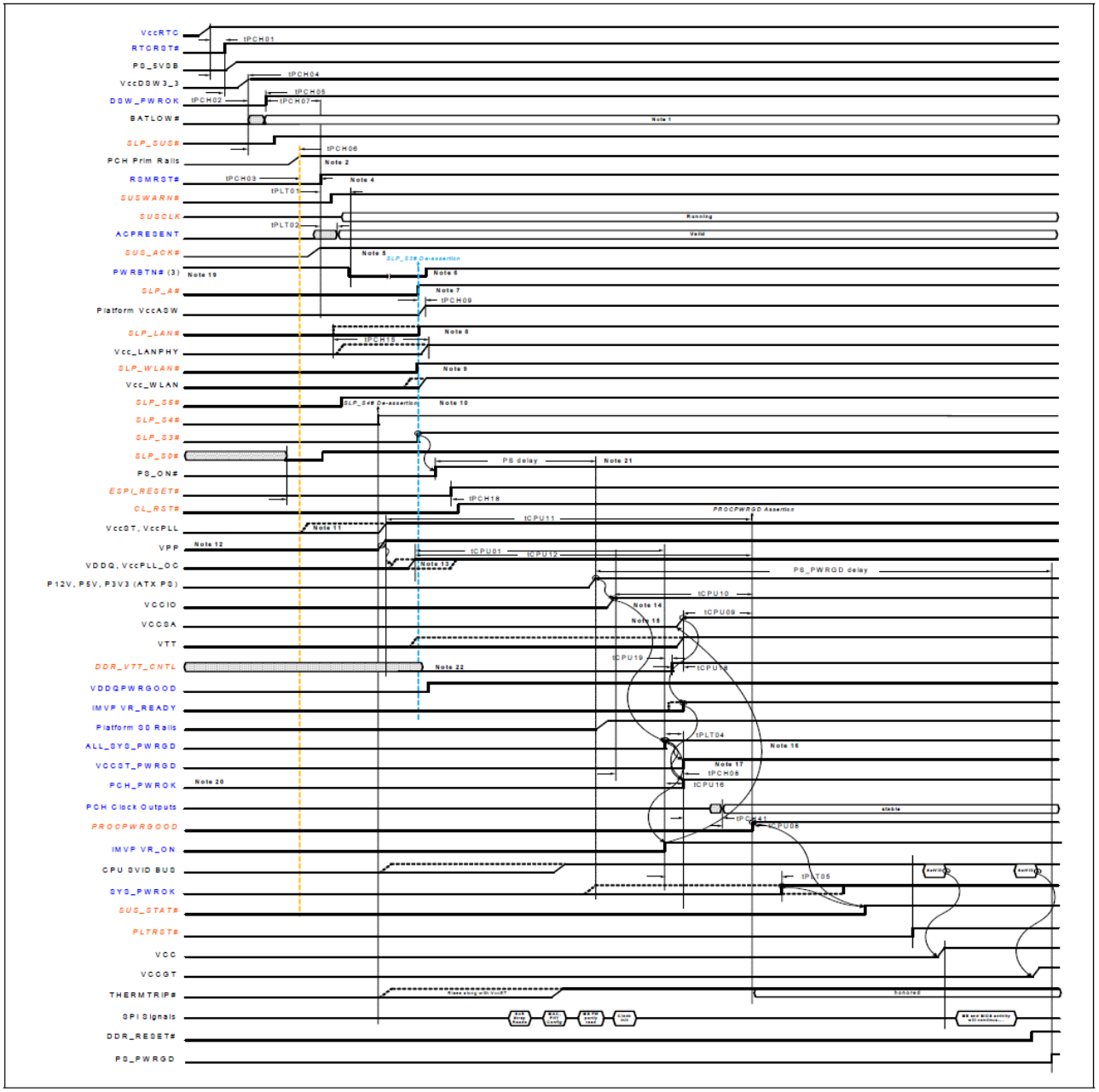

G3-S5

ATX_5VSB
+3.3V_LPS
SLP_SUS#
LPS_ON#
+5V_AUX
+3.3V_AUX/+1.8V_AUX
+PCH_P1V0
RSMRST#

S5-S0

PWBTIN#
PWBTOUT#
SLP_S5/S4/S3
PSON#
+12V/+5V/+3.3V
VCC_DDR
+VCCIO
+VCCP
SYS_PWROK
CHIP_PWRGD
H_PWRGD
PLTRST#

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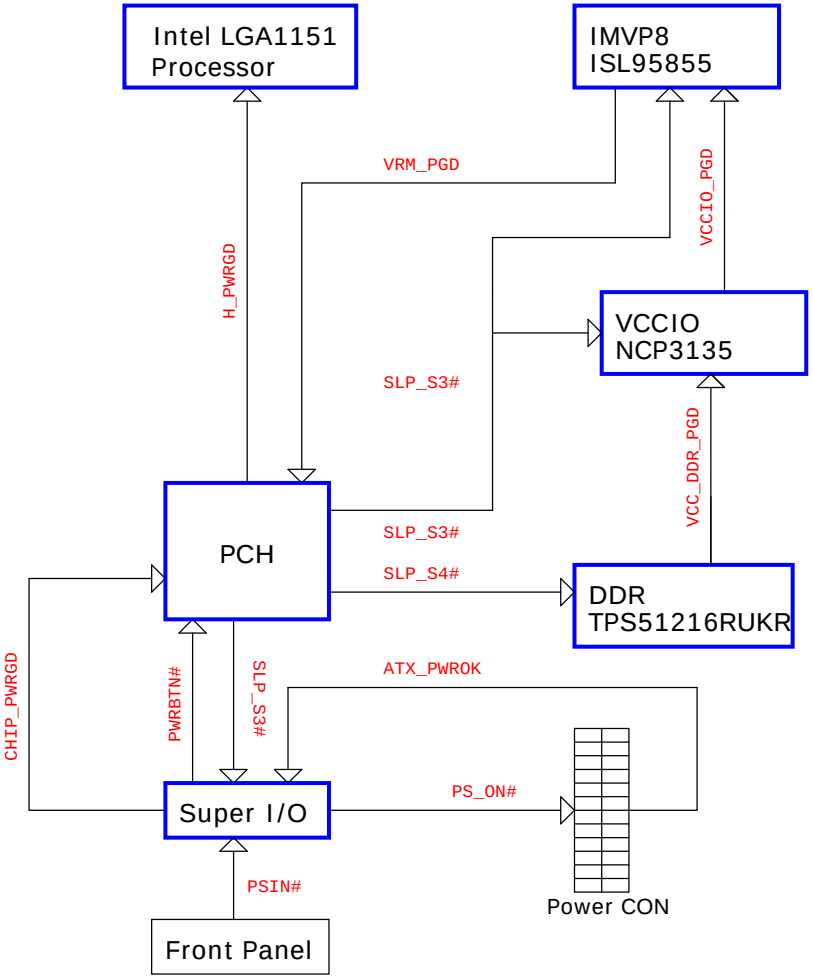
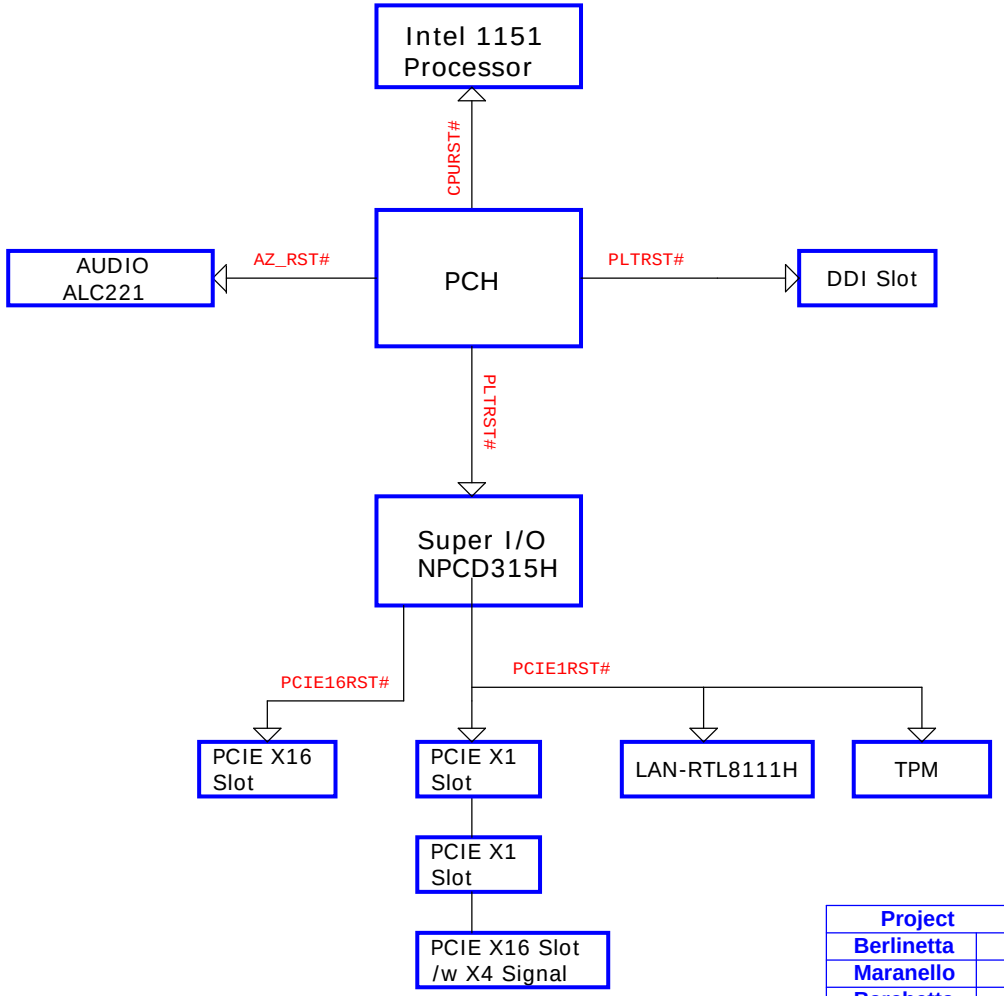
PWROK MAP



RESET MAP



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Title	Pwrok/Reset
Size: Custom	Document Number: HP SCH P/N: 798931-000(MSI MS-7A02)
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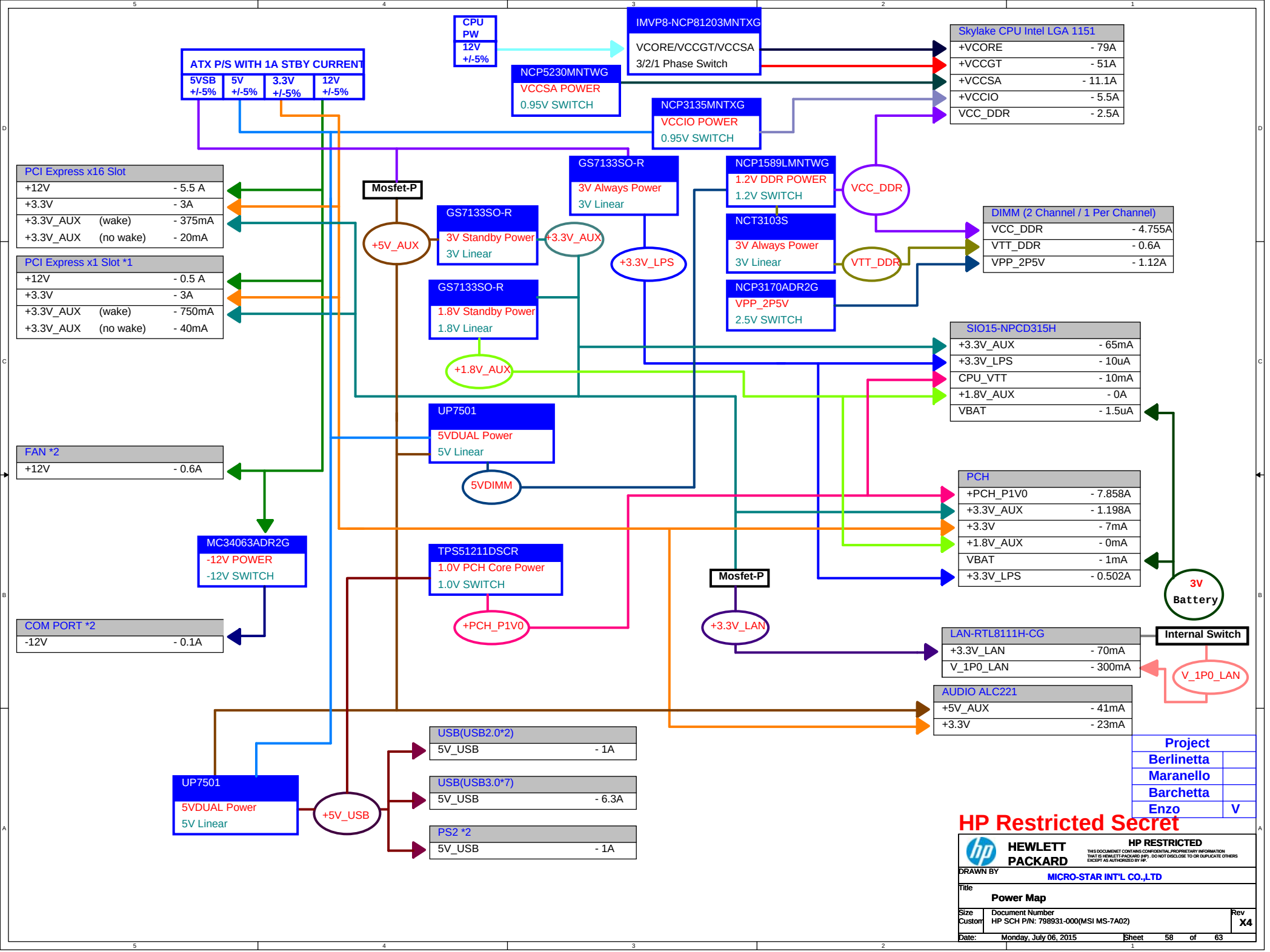
Date: Monday, July 06, 2015	Sheet 57 of 63


CPU PW
12V +/-5%
IMVP8-NCP81203MNTXG
VCORE/VCCGT/VCCSA
3/2/1 Phase Switch
Skylake CPU Intel LGA 1151
+VCORE - 79A
+VCCGT - 51A
+VCCSA - 11.1A
+VCCIO - 5.5A
VCC_DDR - 2.5A
ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
NCP5230MNTWG
VCCSA POWER
0.95V SWITCH
NCP3135MNTXG
VCCIO POWER
0.95V SWITCH
PCI Express x16 Slot
+12V - 5.5 A
+3.3V - 3A
+3.3V_AUX (wake) - 375mA
+3.3V_AUX (no wake) - 20mA
PCI Express x1 Slot *1
+12V - 0.5 A
+3.3V - 3A
+3.3V_AUX (wake) - 750mA
+3.3V_AUX (no wake) - 40mA
Mosfet-P
GS7133SO-R
3V Always Power
3V Linear
GS7133SO-R
3V Standby Power
3V Linear
NCP1589LMNTWG
1.2V DDR POWER
1.2V SWITCH
NCT3103S
3V Always Power
3V Linear
NCP3170ADR2G
VPP_2P5V
2.5V SWITCH
VCC_DDR
VTT_DDR
DIMM (2 Channel / 1 Per Channel)
VCC_DDR - 4.755A
VTT_DDR - 0.6A
VPP_2P5V - 1.12A
+5V_AUX
+3.3V_AUX
+3.3V_LPS
GS7133SO-R
1.8V Standby Power
1.8V Linear
+1.8V_AUX
SIO15-NPCD315H
+3.3V_AUX - 65mA
+3.3V_LPS - 10uA
CPU_VTT - 10mA
+1.8V_AUX - 0A
VBAT - 1.5uA
UP7501
5VDUAL Power
5V Linear
5VDIMM
FAN *2
+12V - 0.6A
PCH
+PCH_P1V0 - 7.858A
+3.3V_AUX - 1.198A
+3.3V - 7mA
+1.8V_AUX - 0mA
VBAT - 1mA
+3.3V_LPS - 0.502A
MC34063ADR2G
-12V POWER
-12V SWITCH
TPS51211DSCR
1.0V PCH Core Power
1.0V SWITCH
+PCH_P1V0
Mosfet-P
+3.3V_LAN
3V Battery
COM PORT *2
-12V - 0.1A
LAN-RTL8111H-CG
+3.3V_LAN - 70mA
V_1P0_LAN - 300mA
Internal Switch
V_1P0_LAN
AUDIO ALC221
+5V_AUX - 41mA
+3.3V - 23mA
USB(USB2.0*2)
5V_USB - 1A
USB(USB3.0*7)
5V_USB - 6.3A
PS2 *2
5V_USB - 1A
UP7501
5VDUAL Power
5V Linear
+5V_USB
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Title: GPIO Table1

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Title: GPIO Table2

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Title: **GPIO Table3**

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Enzo X1

PAGE 34/35: Modify Cap EC5,EC7,EC9 from 1000uF to 470uF.

PAGE 20: Remove Firebird function circuit.

PAGE 5: Change DP to VGA Signal from DDI3 to EDP.

9/30

PAGE 39: SKL Platforms - SPI0_IO3 Signal Implementation Requirement for ES or per-ES1/ES1 Samples.
Add 1kohm R483,R484 pull-up to SPI_POWER. (SI: SIO1083098)

Page 4/12: Add a serial resistor at PROCHOT_N/H_PWRGD/PLTRST# signal according CRB 1.0.
Add R18, R936, R937. (SISIO1083521:)

Page 12: Add a pull-up/down resistor at PCHHOT_N, GPP_H12,GPP_B12,SPKR signal according CRB 1.0.
Add R86,R826,R88,R827,R824,R87. (SI:SIO1083521)

Page 17: Add a pull-down resistor at SMB0ALERT#,SMBALERT# signal according CRB 1.0.
Add R839,R840. (SI:SIO1083521)

Page 39: Add a pull-down resistor at PCH_SPI_MISO,PCH_SPI_MOSI,PCH_SPI_IO2 signal according CRB 1.0.
Add R828,R829,R830. (SI:SIO1083521)

10/01

Page 36:Change P152 pin define from 2x6 2mm to 2x5 2.54mm by HP request.
(SI:SIO1083521)

Page 23:Modify BOARD ID.Change R801 from NI,I to I,R 806 from NI,I to NI.
(SI:SIO1083521)

2014/10/7

PAGE 23:
Modify R256 from I to NI, modify R259 from NI to I, modiyf R801 from I to NI,
modify R796 from NI to I.(SI:SIO1085338)

PAGE 4/17/51: Modify XDP debug port circuit according Intel CRB 1.0.Add R831.
Modify R173,R174,R175,R751,R750,R752,R755,R758,R761,R727,R726,R720 from NI to I,
modify R176,R723,R731R719,R15 from I to NI.(SI:SIO1085338)

2014/10/22

PAGE 42: Modify circuit to power on.
Modify R509 from 45.3k ohm to 45.3 ohm.(SI:SIO1088370)

PAGE 40: Modify circuit to power on.
Modify U22 pin 40 connector from VCC3 to SPI_POWER .(SI:SIO1088370)

Enzo X2

2014/11/24

PAGE 4/44: Modify SVID topology according Intel design guide.
Add R938, R939, R940, R941 (SI:SIO1100439)

PAGE 18: Modify platform debug port header E25 to NB type.
Modify E25 footprint to OWE_FBTB_S20_0_5MM (SI:SIO1100451)

PAGE 34: Modify audio amplifier control circuit.
Reserve modify R370, Q31 from I to NI. (SI:SIO1107289)

PAGE 45/46/47: Marking U93, U94, U96, U97, U98, U99, U100, U101, U24 as CCL parts. (SI:SIO1107293)

Modify SIO15 circuit according SIO15 demo circuit.(SI:SIO1107297)

PAGE 18/23: Pin 4 of U5 connect to pin BD17 and rename PCH_PME# to P_PME#. Modify R206 from I to NI.
(SI:SIO1107293)

PAGE 22/23: Connect chassis ID1 to pin15 of SIO.
move R216 to page 23 and add R943 pull up to +3.3V_AUX.(SI:SIO1107293)

PAGE 22: Connect SIO15 pin 94 to SML1_DATA and pull-up resistor R184 change from I to NI(chipset side have a pull-up resistor).(SI:SIO1107293)

PAGE 23: Connect SIO15 pin 95 to SML1_CLK and pull-up resistor R183 change from I to NI(chipset side have a pull-up resistor).(SI:SIO1107293)

PAGE 23: Connect SIO15 pin 59/61 only pull up to +3.3V.(SI:SIO1107293)

PAGE 36: Keyboard power control change to pin 103 of SIO15.
Change R410 connecting from 5V_USB_CTRL to 5V_USB_MAIN#.(SI:SIO1107293)

PAGE 41: Change JP14 to longer jumper, modify jumper PN from N33-1020271-H06 to N33-1020481-H06.(SI:SIO1107303)

PAGE 32: Modify EC4 PN from C93-10116A1-N07 to C93-10116D1-N07.(SI:SIO1107356)

PAGE 39: Add alone power well +5V_PS2 for PS/2.
Add R950, R951, C700, C701, U56.(SI:SIO1100469)

Page 22: Modify R192,R190,R526 from I to NI for ESPI support.(SI:SIO1107412)

Page 22: Modify R195,R531 from NI to I for ESPI support.(SI:SIO1107412)

Page 20: Modify R564 from NI to I and modify R536 from NI to I for ESPI support.(SI:SIO1107412)

Page 18: Debug header clock connect to U4.BC17.
U4.AV19 connect to a test point TP81. Reserve R956. Add R957. Modify R812 from I to NI.
Modify R813 from NI to I for ESPI support.(SI:SIO1107412)

Page 18: Modify R814 from PROTO to NI and modify R815 from NI to PROTO for ESPI support.(SI:SIO1107412)

Page 18: ESPI_ALERT1# add a pull-up R958 for ESPI support.(SI:SIO1107412)

Page 14: Reserve R953,R954,R955 for ESPI support.(SI:SIO1107412)

Page 19: Modify R165 from 4.7k to 1k and modify from NI to I, modify R839 from I to NI for ESPI support.
(SI:SIO1107412)

Page 23: Reserve R960,R961,R962 for ESPI support.(SI:SIO1107412)

Modify power circuit for improve power quality.

PAGE 44: Modify R793 from 28.7k ohm to 30k ohm. R552 from 4.2k ohm to 3.6k ohm.(SI:SIO1107590)

PAGE 47: Modify R879 from 10k ohm to 8.2k ohm. R797 from 27k ohm to 7.5k ohm, from NI to I.(SI:SIO1107590)

2014/11/27

Page 18: Modify R153 from NI to I for ESPI support.(SI:SIO1107412)

Page 34:Modify R356/R357 from 51k ohm to 10k ohm,
modify R360/R361 from 10k ohm to 20k ohm for no beep sound issue.(SI:SIO1107289)

Page 25: Modify RT3, C104 from NI to I following SIO demo circuit.(SI:SIO1107297)

Page 23: Move R239 to Q5.D pin, modify R234 from 47k ohm to 100k ohm,
delete R236 to follow SIO demo circuit.(SI:SIO1107297)

Modify crystal circuit for improve crystal quality.

Page 16: Modify C28,C30 from 15pF to 18pF for Vendor support,
modify C29,C31 from 27pF to 15 pF for Vendor support.(SIO1097960)

Page 32: Change location from Y6 to Y3 to meet PCA spec.
modify C228,C229 from 27 pF to 12 pF for Vendor support.(SIO1097960)

Page 14: Modify R53 from I to NI for ESPI support.

2014/12/10

Page 51: Modify +1P0V_EN circuit for System can not power on from S5 Max Power Saving mode
Add Q104, R963, C702. (SI:SIO1107604)

PAGE 17: Connect DP to VGA HPD pin to DDPE_HPD3 for no VGA output isssue.(SI:SIO1107624)
PAGE 17: Connect EPD_HPD to GND through R114 for no VGA output isssue.(SI:SIO1107624)

2014/12/15

PAGE 32: Modify LAN power control circuit.(SI:SIO1107635)
R326 connect to LPS_ON#.

PAGE 32: Modify LAN wake circuit.(SI:SIO1107635)
Modify R314 from NI to I, Modify R532 from I to NI

PAGE 14/32: Modify LAN clock request circuit.(SI:SIO1107635)
Modify R317 from NI to I, Modify R630 from I to NI, Reserve R965.

PAGE 26: Modify Q12 from NI to I and modify R273,C115 from I to NI, modify.(SIO1092498)

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2014/12/24

Page 18: Connect R813 to +1.8V_AUX for ESPI support.(SI:SIO1107412)

Page 22/41: Connect FDT_OVRD# to SIO15 Pin 78 GPIO22.(SI:SIO1108001)

Page 41: Modify R484 from I to NI.(SI:SIO1108004)

2014/12/25

Page 44: Connect R478 from 5VDIMM to +5V_AUX.(SI:SIO1108006)

Page 14: Add U92, C704 and modify R868 from 0 ohm to 10k ohm for POS.(SI:SIO1108052)

Add one power rail VCCST_P1V0 for VCC_DDR leakage.
Page 51:Add Q106,Q107,R971,R972,R973,C705,C706.(SI:SIO1108057)

Page 4: Connect R941,R7,R8,R10,R11,R12,R13,R14 from +PCH_P1V0 to VCCST_P1V0.(SI:SIO1108057)
Page 8: Connect XU1 PIN V4/V5/V6 from +PCH_P1V0 to VCCST_P1V0.(SI:SIO1108057)
Page 19: Connect R229,R174,R175 from +PCH_P1V0 to VCCST_P1V0.(SI:SIO1108057)
Page 23: Connect SIO +VTT from +PCH_P1V0 to VCCST_P1V0.(SI:SIO1108057)

Page 44: Connect R819,R508,R509,R518,C368 from +PCH_P1V0 to VCCST_P1V0.(SI:SIO1108057)

Page 53: Connect R721,R760 from +PCH_P1V0 to VCCST_P1V0.(SI:SIO1108057)

2014/12/29

Page 34: Remove D18, Add C707 by CODEC vendor review.(SI:SIO1108244)

2015/01/07

Modify XDP circuit.
Page 53: Modify R729,R752,R755,R758,R761,R772,R750, R751 from I to NI.(SI:SIO1108386)
Page 19: Modify R174, R175 from I to NI.(SI:SIO1108386)
Page 4: Modify R15 from NI to I.(SI:SIO1108386)
Page 14: Modify R86 from 4.7K to 150K and I.(SI:SIO1108386)
Page 25: Modify R715 from NI to I for DB2 revision ID.(SI:SIO1108390)

2015/01/08

Page 36/37: Modify EC6, EC10 from 1000uF to 470uF .(SI:SIO1111301)

Page 16: Modify C29, C31 from C0603 to C0402 .(SI:SIO1111342)

2015/01/14

Page 41: Modify R438 from NI to I and modify R763 from I to NI for PCH ES2 sample.(SI:SIO1111356)

PAGE 14: Use GPP_H2 for PCI_EXT_DET.
Add R967(SI:SIO1111374)

Page 47: Remove R374,R482 and Add C539,C540 by power team review.(SI:SIO1111389)

2015/01/15

Page 50: Modify C511 from 0.1pF to 10uF and modify C511 from C0402 to C0805.(SI:SIO1111389)

2015/01/19

Page 24/28/38/41/42: Modify D5,D9,D10,D32,D39,D40,D43,D44 PN to D0G-03A0509-SI0
for EMC issue.(SI:SIO1111561)

Page 38/39/40: Modify L21,L22,L27,L28,L39,L40,L43,L45,L46
from NI to I for EMC issue.(SI:SIO1111561)

Page 38/39/40: Modify RN7,RN8,RN9,RN10,RN11,RN12,RN13,RN14,RN21,RN22,RN23,RN24,RN25,RN26,RN45,RN46
from I to NI for EMC issue.(SI:SIO1111561)

Page 39/40: Modify L23,L24,L25,L26,L35,L36,L37,L38
from NI to I for EMC issue.(SI:SIO1111561)

Page 39/40: Modify L23,L24,L25,L26,L35,L36,L37,L38
PN to L12-5008030-I05 for EMC isssue.(SI:SIO1111561)

2015/01/19

Page 31: Add RSMRST# debug LED circuit. Add Q108,R984,R985,CR12 by HP request.(SIO1132827)

2015/01/22

Page 24: Add R323 connector to RIB#.(SIO1132855)

2015/01/29

Page 50: Modify R678 from 102k to 10k ohm, modify R677 from 324k to 32.4k ohm,
modify C519 from 0.015uf to 22pf for +3.3V_LPS can't BLEED-OFF in G3 state.(SIO1133146)

Enzo X3

2015/02/26

Page 32/33: Modify LAN circuit by HP request. Add R988, R989, modify R339 from 510 ohm to 249 ohm and
 modify from NI to I,delete R336.(SIO1133218)

2015/03/9
Page 48: Modify C486 from 100pF to 22pF, modify C481 from 2200pF to 4700pF by power solution
(improve phase margin not enough).(SIO1133373)

2015/03/18
Page 28: Modify C147 from 4.7pF to 2.2pF, by VGA SA measure.(SIO1133404)
2015/03/24

Page 32: Chnage C228,C2296 from 12pF to 27pF by Crystal Vendor review.(SIO1133447)

2015/03/25

Page 45/47: Chnage EC31,EC32,EC33,EC34,EC35 P/N form (C71-27116C1-N07)to(C71-2711751-N07)and footprint from
(C_P3_5_D8_H11_5)to(C_P2_5_D6_3_H9_5) by thermal solution. .(SIO1133463)

2015/03/26
Page 45: Chnage +VCORE C409,C411,C413 footprint from C0805 to C0603, reserved C618,C657,C652
for SKL S Processor Decoupling Requirements.(SIO1133533)

Page 46: Chnage VCCGT C442,C443,C444,C448,C449,C450,C452,C447,C466,C638,C633 from 22uF to 47uF, reserved C451
for SKL S Processor Decoupling Requirements.(SIO1133533)

Page 48: Chnage VCCIO C482,C489,C490,C495,C496 footprint from C0805 to C0603
for SKL S Processor Decoupling Requirements.(SIO1133533)

Page 48: Reserved VDDQ C553,C557,C570,C573
for SKL S Processor Decoupling Requirements.(SIO1133533)

Page 36: change the cap pn and footprint to meet thermal request.Chnage EC5 from C93-4711031-N07 to C94-47110B1-N07,
EC7 from C93-4711031-N07 to C94-4710651-N07 by thermal request .(SIO1133463)

2015/03/31

Page 42: TPM SLB9670 will have higher power consumption issue at S3/S4/S5. Add R991,R993,R990,Q109,Q110,R91,R92
by TPM leakage current and power down fixed circuit .(SIO1134609)

Page 14/47: Add Q111 connector to U92.1, add C658,R889 ,Change C704 from I to NI.
by POS tPTT04,tCPU28 .(SIO1136082)

Page 16: HP request change clear cmos(SW50) button location(SIO1136655)

Page 25: Modify Board REV. ID. Change R715 from I to NI, R712 From NI to I.(SIO1140856)

2015/04/9

Page 32: Modify LAN LED circuit. Add Q39 to control LAN wake from G3.(SIO1140929)

2015/04/14

PAGE 50: Modify R669 from 147k ohm to 14.7k ohm and modify R671 from 115k ohm to 11.5k ohm for +1.8V_AUX power quality..(SIO1144994)

PAGE 34: Modify R369 size from 0402 to 0603 and modify C259,C263 from 0.01uF to 0.1uF by audio vender suggestion.(SIO1145006)

2015/04/20

Modify THERMTRIP# control circuit.
PAGE 14: Modify R59 from I to NI and move Q11 to Page 14 and modify to NI.(SIO1144927)

PAGE 30: Modify P81 from PROTO to NI.(SIO1145014)

2015/04/21

PAGE 16: Modify the clear cmos button footprint to add AVL part. Modify SW50 footprint and P/N.(SIO1145020)

2015/04/22

PAGE 36: Modify EC8 footprint from C_P2_5_D6_3_H11 to C_P2_5_D6_3_H5, Change EC8 from high CAP to low CAP to meet ME request .(SIO1145699)

2015/05/7

Add USB type C to PCA.
PAGE 30: Add P81, R945, R946.(SIO1117557)

PAGE 33: Modify LAN circuit by HP request. Add R988, R989, modify R339 from 510 ohm to 249 ohm and modify from NI to I,delete R336.(SIO1133218)

PAGE 29: Remove +3.3V_SLOT power circuit and instead of +3.3V_AUX.Remove RN6,U65,R299,Q16,EC3,C189.(SIO1133218)

PAGE 50: HP request change clear cmos button location.Remove R665,R667,D39. (SIO1136655)

PAGE 51:HP request the RTC battery holder type from Vertical to Lying.Remove E18. (SIO1136090)

PAGE 24/28: RGB EMI issue. Change J69 P/N.Change L15,L16,L17,L18,L19,L20 from 33nH to 22nH,C142,C146,C149 from 2.2pF to
15.pF,C143,C146,C149 from 4.7pF to 1.5pF,C154,C155 from 15pF(NI) to 10pF(I).(SIO1145275)

PAGE 36/46: Change some cap life cycle to meet hp thermal test.EC31 from I to NI, Change EC4,EC5,EC7,EC32,EC33,EC34,EC35 P/N. (SIO1152750)

PAGE 54:Change PCB part from X2 to X3.(SIO1152765)

PAGE :The Purchase suggest change parts .Change Q37,Q38,Q59,Q85,Y1,EC10,EC47,EC50,EC6,EC9,J41,XMM1,XMM3 P/N.(SIO1152797)

PAGE 14~21: Change PCH version from ES2 to QS.Change U4 P/N.(SIO1152828)

PAGE 42:TPM IC change FW version from 6.02 to 6.1.Change U40 P/N.(SIO1152832)

PAGE 22/23:change SIO IC version from A2 to A3.Change U5 P/N.(SIO1152846)

PAGE 40: THE USB3.0 header too loose.Change USB3.0 header P/N.(SIO1152885)

Enzo X4

2015/06/03

Modify PROCHOT# topology.
PAGE 4: Modify R11 from 75 ohm to 1k ohm, modify R18 from 100 ohm to 499 ohm.(SIO1168929)

Modify LAN_DISABLE# pull-up resistor to NI.
PAGE 14: Modify R507 from I to NI.(SIO1168845)

SIO15 COMP_IN3 control update
PAGE 23: Add R994,Q112.(SIO1168804)

2015/06/05

Modify circuit according Intel SR_Rev16.
PAGE 20: Add L9,C778,C779.(SIO1185129)

Add buffer at ESPI RESET signal..
PAGE 18/22: Add C780,C781,U96,R173,R782.(SIO1168908)

2015/06/10

Modify VCCSA circuit by power solution.
PAGE 47:Remove C636,Add EC38,R894.(SIO1185165)

2015/06/15

Modify DDR3L to DDR4 for spec change.
PAGE 6/7/11/13/43: Modify DDR slot and power solution for DDR4(SIO1185176)

Modify Pin K12/L12 of XU1 from GND to test points.(SIO1185190)

Add serial resistor on PROC_TRIGIN/PROC_TRIGOUT following CRB.
PAGE 4/19: Add R1024 and R1025(SIO1185190)

Reserve a pull-down resistor on PCH PWRGD following Intel design guide.
PAGE 14: Add R1026 and NI(SIO1185190)

2015/06/22

DIMM EVENT_N pull up to VCC_DDR with 240ohm following CRB.
PAGE 11/13: Add R1028,R1030.(SIO1185202)

Modify ESPI RESET circuit.
PAGE 18/22: Modiyf C781,U102 from NI to I,modify R173 from I to NI,modify C782 to 47pf and I.(SIO1168908)

Modify XDP circuit following design guide.
PAGE 19: Modiyf R174,R175 from NI to I.(SIO1185242)

Modify PROCHOT# circuit following design guide.
PAGE 44: Modiyf R570 from 0ohm to 75 ohm.(SIO1185254)

Modify the value of ESPI dampping resistor following design guide.
PAGE 18: Modiyf R185,R186,R187,R188,R189,R494,R354 from 0ohm to 15 ohm.()

Modify PCH_WAKE# circuit to fix some PCA auto power on issue.
PAGE14/23 : Modify R53,R962 from NI to I and reserve pull-up resisrotor R1031.(SIO1185310)

Modify PCB revion ID to SI2 state.
PAGE26 : Modify R251 from I to NI, modify R716 from NI to I.(SIO1185349)

Modify SP_IO2/SPI_IO3 circuit.
PAGE41 : Modify R437,R438 from I to NI.(SIO1185374)

Remove the E16 and E20 for DDR4 layout limitation.
PAGE41 : Remove E16,E20,Q18,Q22,Q26,Q108,Q23,Q27,Q19,CR2,CR8,CR10,CR12,CR6,CR11,CR4,R301,R307,R311,R984,R985,R305,R312,R302.(SIO1185390)

2015/07/01
Modify PCH PN to Prime - QS sample.
PAGE 14/~21: Modify UV4 PN from OB1-7957003-IX6 to OB1-7957005-IX6,
.()

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Title: History 2

Size	Document Number	Rev
C	HP SCH P/N: 798931-000(MSI MS-7A02)	X4

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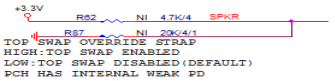
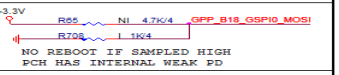
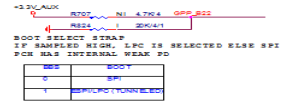
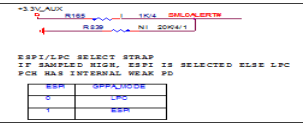
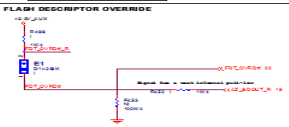
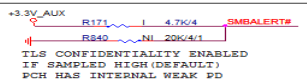
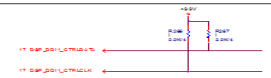
Processor/PCH Strapping

Pin Name	Strap Description	Configuration(Default Value for Each Bit is 1 Unless Specified)	Default Value	V
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Connect a series 1 K Ω resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.		
CFG[1]	Reserved. No connect			Reserved
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal. A test point may be placed on the board for it.	1 = Normal operation 0 = Lane numbers reserved		NI
CFG[3]	Reserved configuration lane			Reserved
CFG[4]	Display Port Presence strap	1:Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0:Enabled - A Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 K Ω ±5% resistor to enable port.	1	
CFG[6:5]	PCI Express* Bifurcation. A test point may be placed on the board for it.	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express* Recommend 1K Ω ±5% pull-down resistor to GND.		NI
CFG[7]	PEG Training. A test point may be placed on the board for them.	1 = (default) PEG train immediately following RESET# de assertion. 0 = PEG wait BIOS for training.	1	NI
CFG[19:8]	Reserved configuration lane			Reserved
SPKR/GPP_B14	Top-Block Swap Override	This signal has an integrated weak pull-down resistor (20 K Ω nominal) to disable Top-Block Sway by default. To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 K Ω ±5% resistor.	0	
GSPI0_MOSI/GPP_B18	No Reboot	This signal has an integrated weak pull-down resistor (20 K Ω nominal) to disable the no reboot strap functionality by default. To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 K Ω ±5% resistor.	0	
GSPI1_MOSI/GPP_B22	Boot BIOS Strap Bit(BBS)	This signal has an integrated weak pull-down resistor (20 K Ω nominal) to default boot from SPI. To enable boot to LPC, this signal should be pulled up to V3.3S through a 1k to 2.2 K Ω ±5% resistor.	0	
SML0ALERT#/GPP_C5	eSPI or LPC	This signal has a weak internal pull-down resistor (20 K Ω nominal) to default LPC is selected for EC.	0	
HDA_SDO	Flash Descriptor Security Override	This signal has an integrated weak pull-down resistor (20 K Ω nominal) to enable security measures in the flash descriptor. To enable Flash Descriptor Security Override, this signal should be pulled up to VCCHDA through a 1 K Ω to 2.2 K Ω ±5% resistor.	0	
SMBALERT#/GPP_C2	TLS Confidentiality	This signal has an integrated weak pull-down resistor (20 K Ω nominal) to disable Intel® ME Cryptographic Transport Layer Security (TLS) cipher suite (no confidentiality). To enable Intel® ME Cryptographic Transport Layer Security (TLS) cipher suite with confidentiality, this signal should be pulled up to V3.3A through a 1k to 2.2 K Ω ±5% resistor.	0	
DDPB_CTRLDATA/GPP_I6	Port B Detected	This signal has an integrated weak pull-down resistor (20 K Ω nominal).When this signal is sampled high, the Digital Display Port B will be detected.	0	
DDPC_CTRLDATA/GPP_I8	Port C Detected	This signal has an integrated weak pull-down resistor (20 K Ω nominal). When this signal is sampled high, the Digital Display Port C will be detected.	0	NI

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Title	Strap pin table
Size: Custom	Document Number: HP SCH P/N: 798931-000(MSI MS-7A02)
Rev	X4
Date:	Monday, July 06, 2015
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