PADME Coffelake Block Diagram

Project Code: 4PD0DY010001
PCB(Raw Card): 17870-SB

External Connector/Socket
Internal Connector/Socket
Switch

PCB Layer Stackup

10 Layers FR4
L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:VCC
L8:Signal 4
L9:GND
L10:Component

Battery Charger/Selector BQ24780SRUYR 85	
VINT20	M-BAT-PWR
System DC/DC TPS51285B-1RUKR 86	
VINT20	VCC5M VCC3M
DC/DC IMVP8 NCP81215MNTXG 87	
VCC5M	
DC/DC VCCCPUCORE NCP302045MNTXG 88	
VINT20	VCCCPUCORE
DC/DC VCCGFXCORE_I NCP302035MNTXG 90	
VINT20	VCCGFXCORE_I
DC/DC VCCSA NCP302035MNTXG 91	
VINT20	VCCSA
DC/DC VCC1R05_SUS NB693GQ-C669-Z 93	
VCC5M	VCC1R05_SUS
DC/DC VCCCPUIO NB694GD-C669-Z 92	
VCC5M	VCCCPUIO
DC/DC VCC1R2A TPS51716RUKR 95	
VINT20	VCC1R2A
DC/DC VCC2R5A NB695GD-C669-Z 96	
VCC5M	VCC2R5A
DC/DC VCC0R6B TPS51716RUKR 95	
VCC1R2A	VCC0R6B
DC/DC VCC1R8_SUS NB695GD-C669-Z 94	
VCC5M	VCC1R8_SUS
DC/DC VCC1R0VIDEO NB695GD-C669-Z 105	
VCC5M	VCC1R0VIDEO
DC/DC VCCGFXCORE_D NCP302045MNTXG 103	
VINT20	VCCGFXCORE_D
DC/DC VCC1R35VIDEO TPS51219RTER 104	
VINT20	VCC1R35VIDEO
LOAD SW VCC1R8VIDEO SSM6K504NU 106	
VCC1R8_SUS	VCC1R8VIDEO
LOAD SW VCCST TPS22971YZPR-GP 97	
VCC1R05_SUS	VCCST

<Variant Name>

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Title: BLOCK DIAGRAM
Size: A2 | Document Number: PADME | Rev: 1
Date: Monday, October 01, 2018 | Sheet 1 of 110

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

DESCRIPTION

BOM control parts :
TEXT with PURPLE color near part reference

BOM control name
Part reference
Symbol name

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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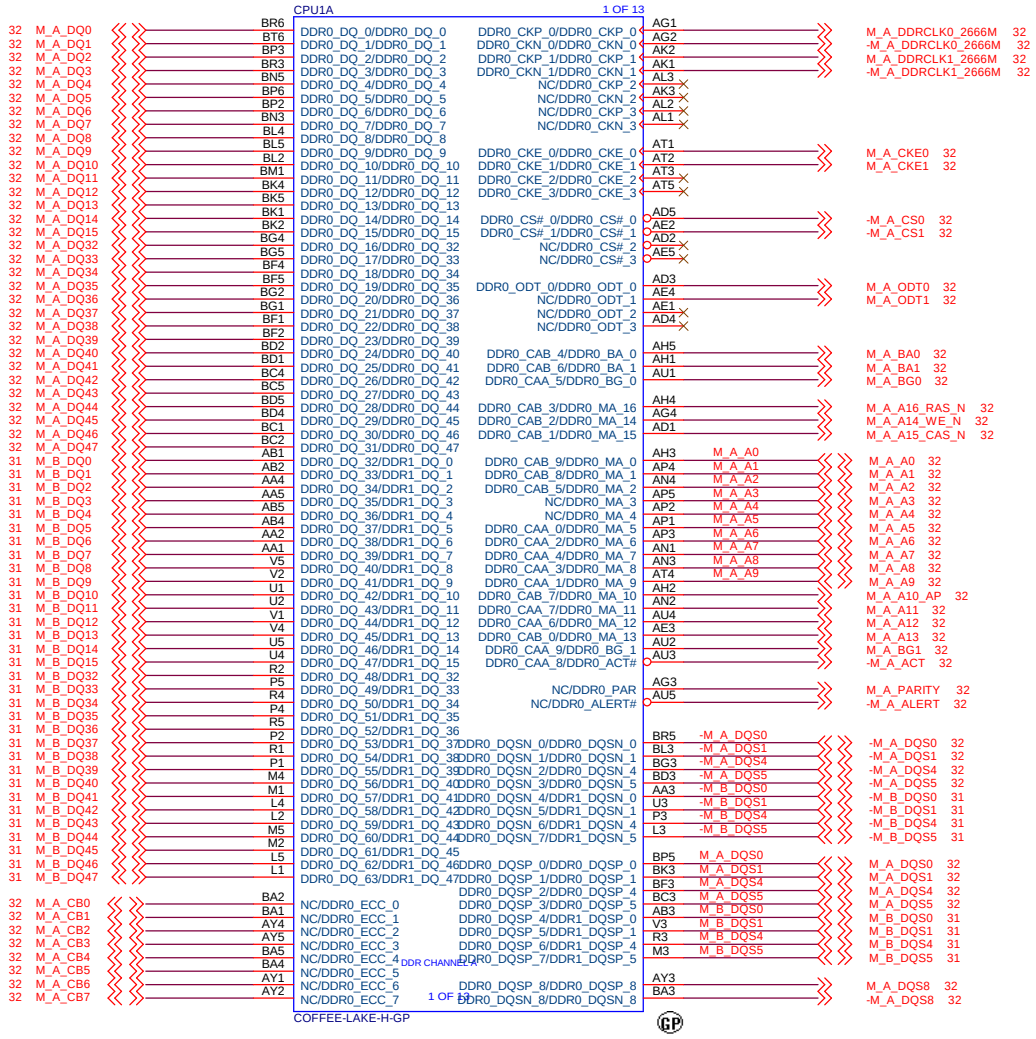
Title ***DESCRIPTION***

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 2 of 110



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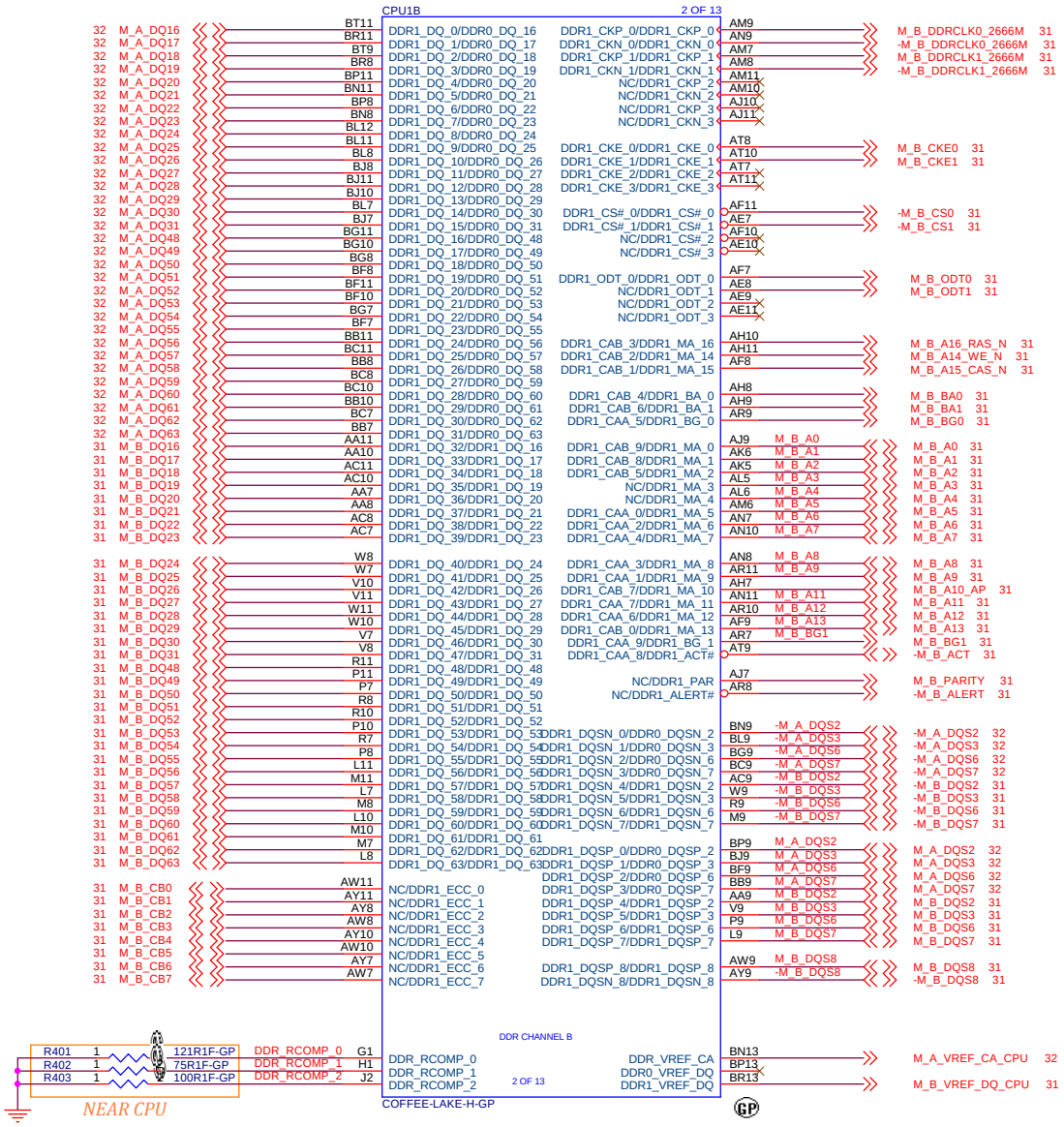
Title: **CPU CFL-H DDR4 CH-A**

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 3 of 110



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Title: CPU CFL-H DDR4 CH-B

Size	Document Number	Rev
A3	PADME	1

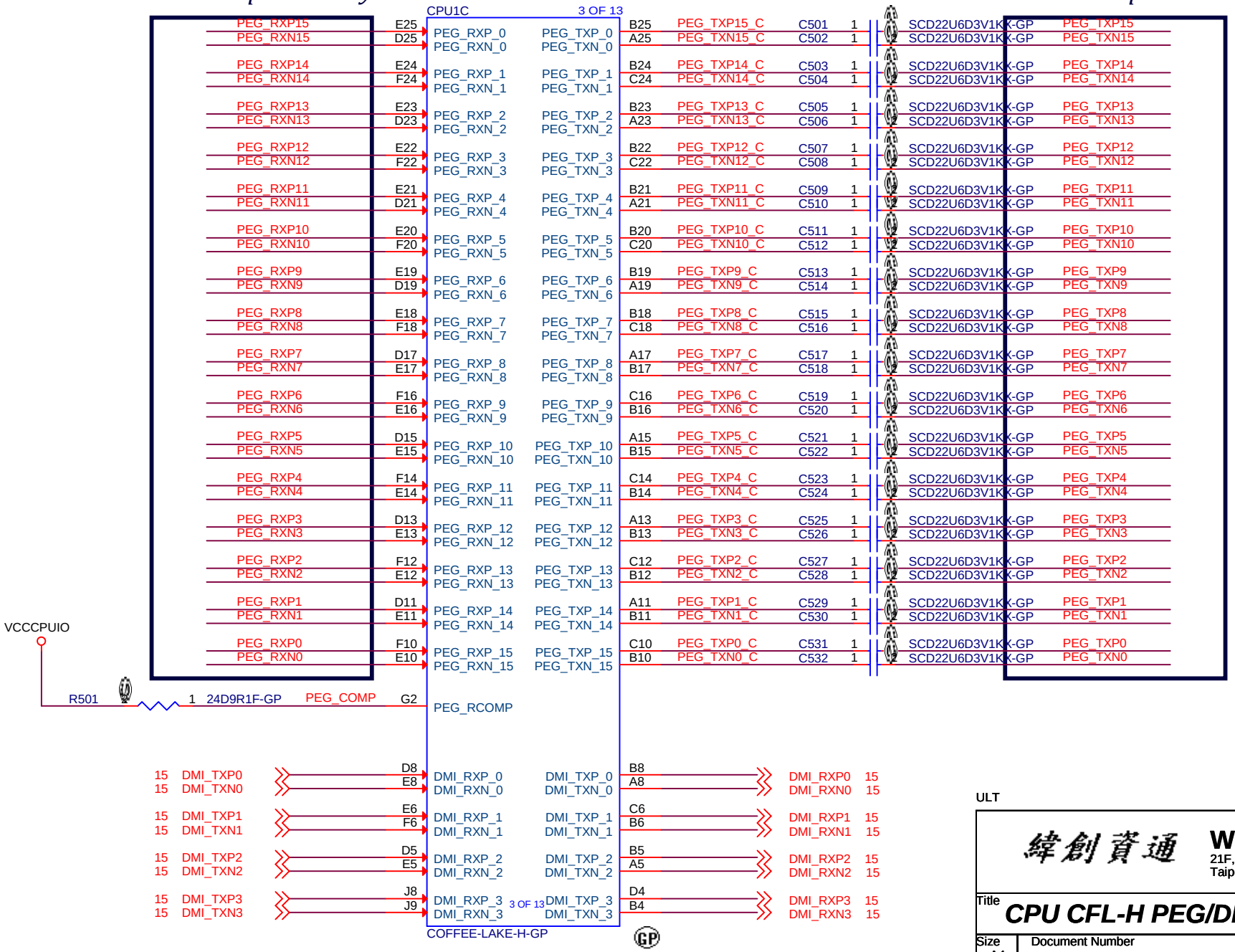
Date: Monday, October 01, 2018 Sheet 4 of 110

33 PEG_RXP[15:0]
33 PEG_RXN[15:0]

33 PEG_TXP[15:0]
33 PEG_TXN[15:0]

Line Reverse : Depend on layout

Line Reverse : Depend on layout



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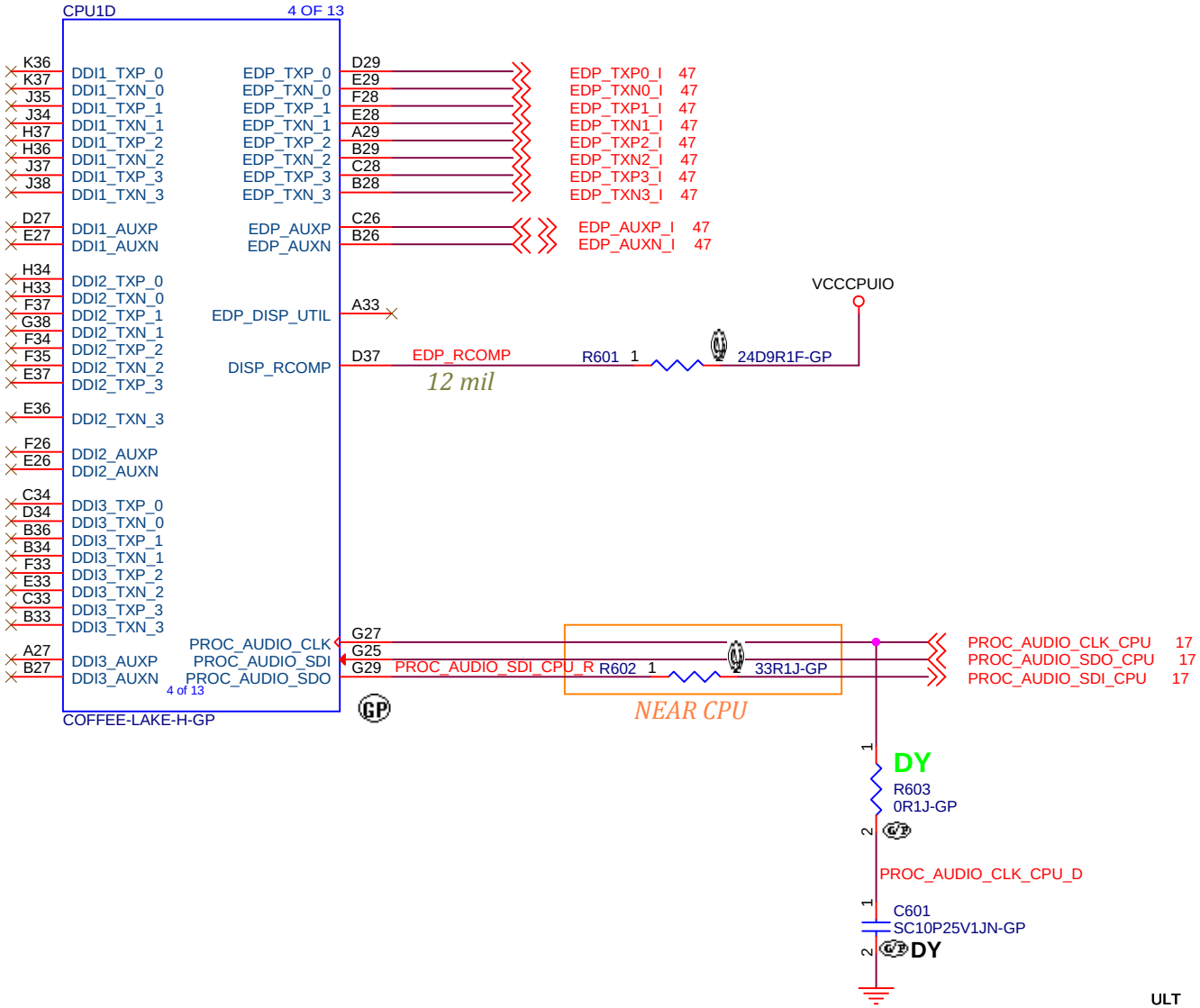
Title **CPU CFL-H PEG/DMI**

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 5 of 110



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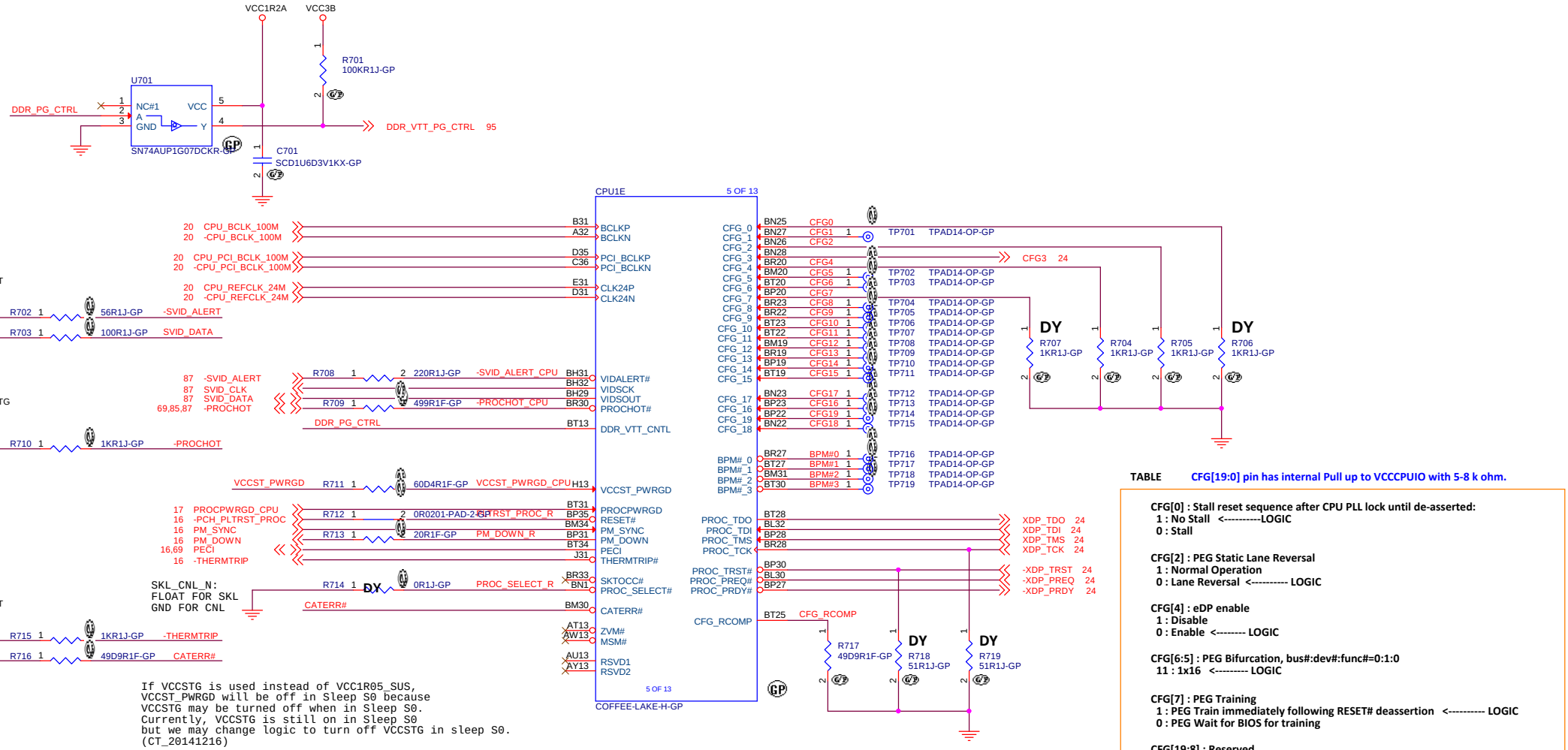
Title: CPU CFL-H DDI/EDP		
Size: A4	Document Number: PADME	Rev: 1
Date: Monday, October 01, 2018	Sheet 6 of 110	



If VCCSTG is used instead of VCC1R05_SUS,
VCCST_PWRGD will be off in Sleep S0 because
VCCSTG may be turned off when in Sleep S0.
Currently, VCCSTG is still on in Sleep S0
but we may change logic to turn off VCCSTG in sleep S0.
(CT_20141216)

TABLE CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:
1 : No Stall <----------LOGIC
0 : Stall

CFG[2] : PEG Static Lane Reversal
1 : Normal Operation
0 : Lane Reversal <---------- LOGIC

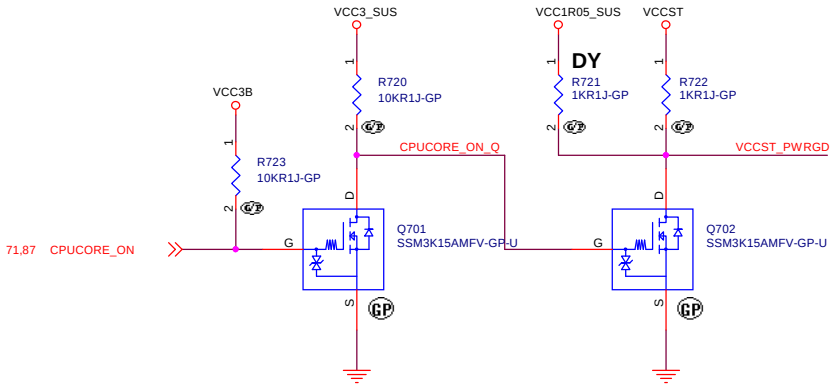
CFG[4] : eDP enable
1 : Disable
0 : Enable <-------- LOGIC

CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0
11 : 1x16 <--------- LOGIC

CFG[7] : PEG Training
1 : PEG Train immediately following RESET# deassertion <---------- LOGIC
0 : PEG Wait for BIOS for training

CFG[19:8] : Reserved

For x16 Reversal Lanes - CFG[6/5/2] setting is 110
For x 4 Reversal Lanes - CFG[6/5/2] setting is 000



VCCST_PWRGD requirements
1) Indication that the VCCST\VDDQ power supplies are stable and within specification
2) VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST
3) VCCST_PWRGD can assert vefore or equal to PCH_PWROK, but must never lag it.

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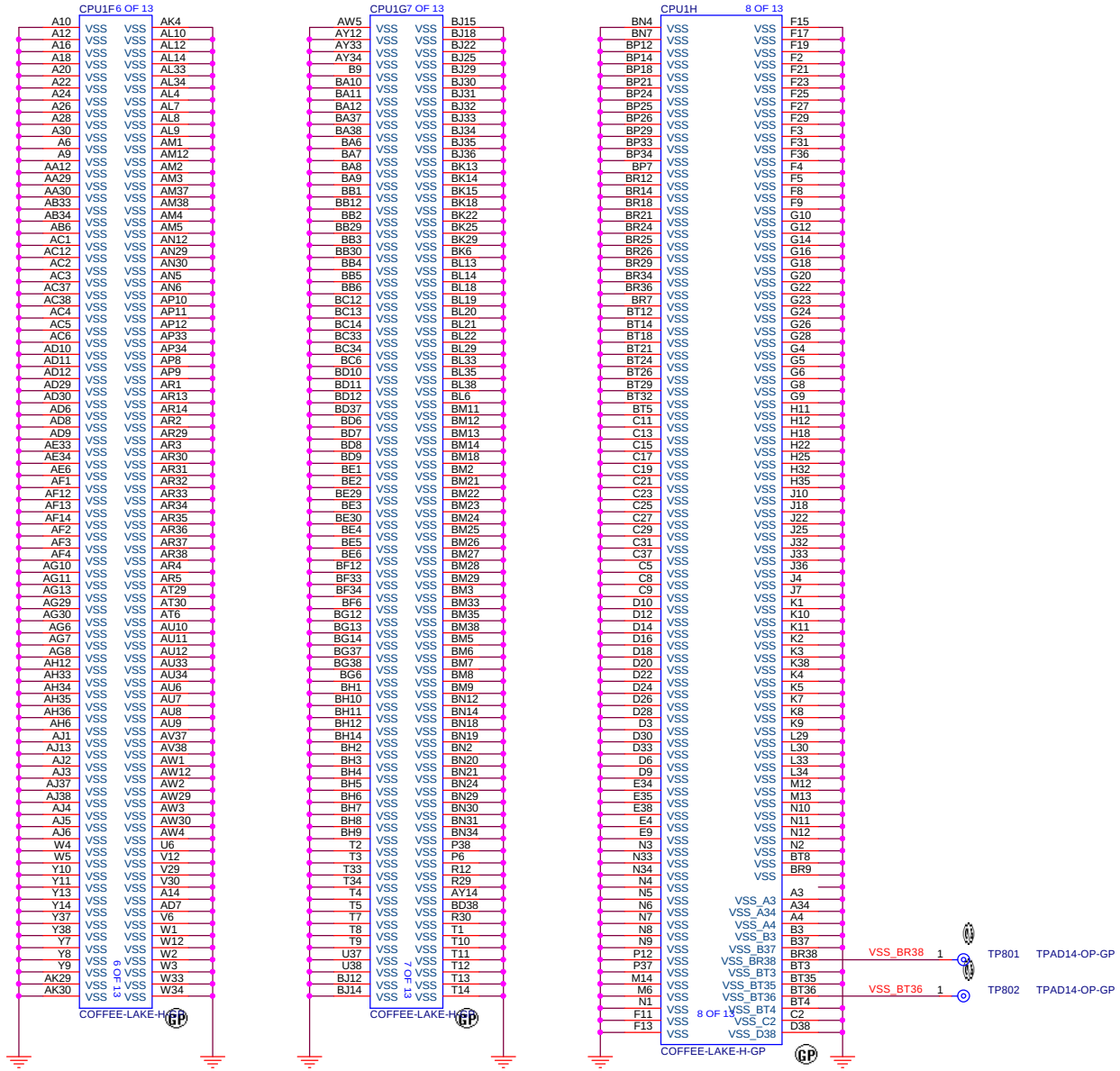
Title: **CPU CFL-H MISC/CLK/JTAG/CFG**

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 7 of 110



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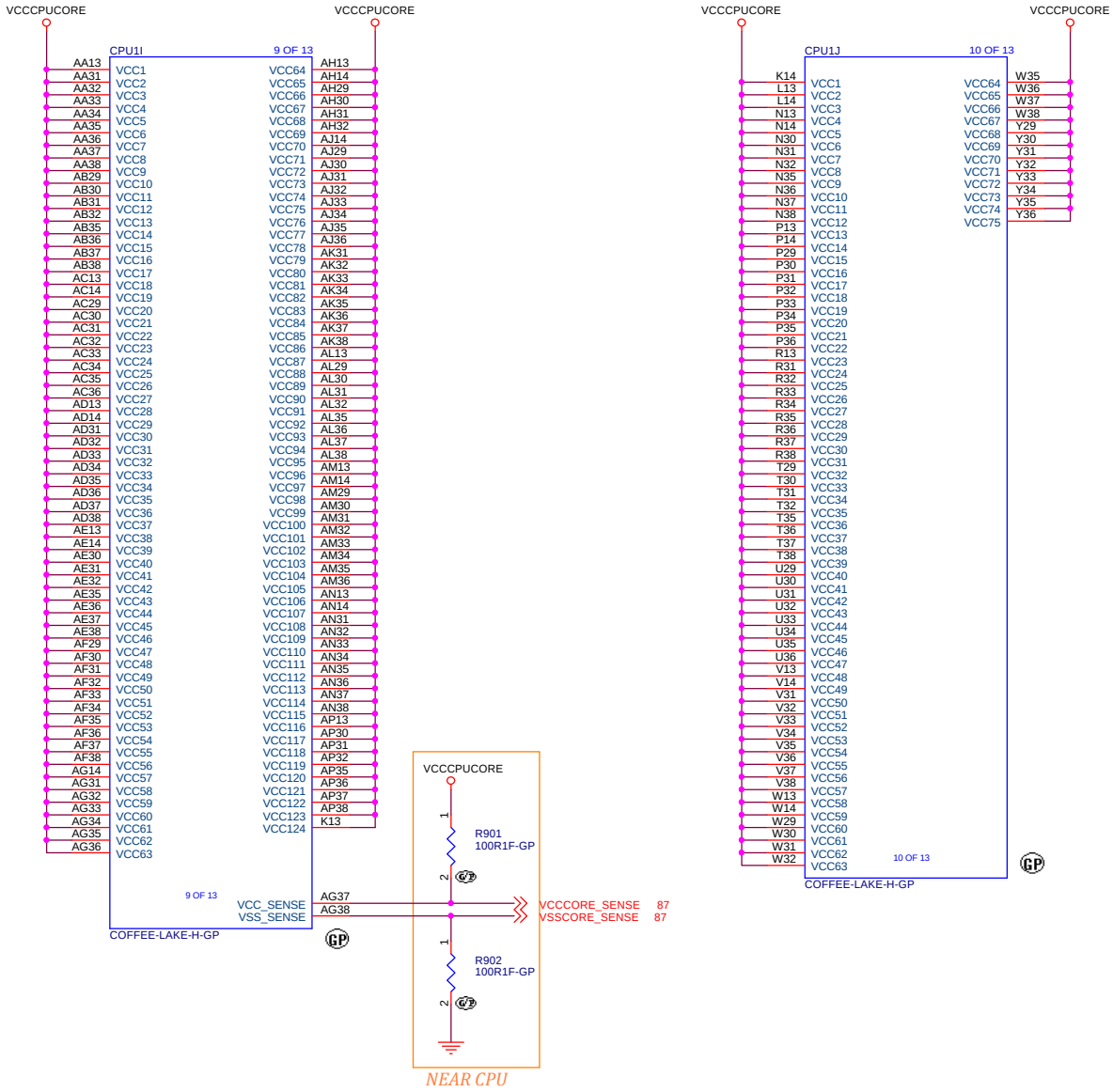
Title: **CPU CFL-H GND**

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 8 of 110



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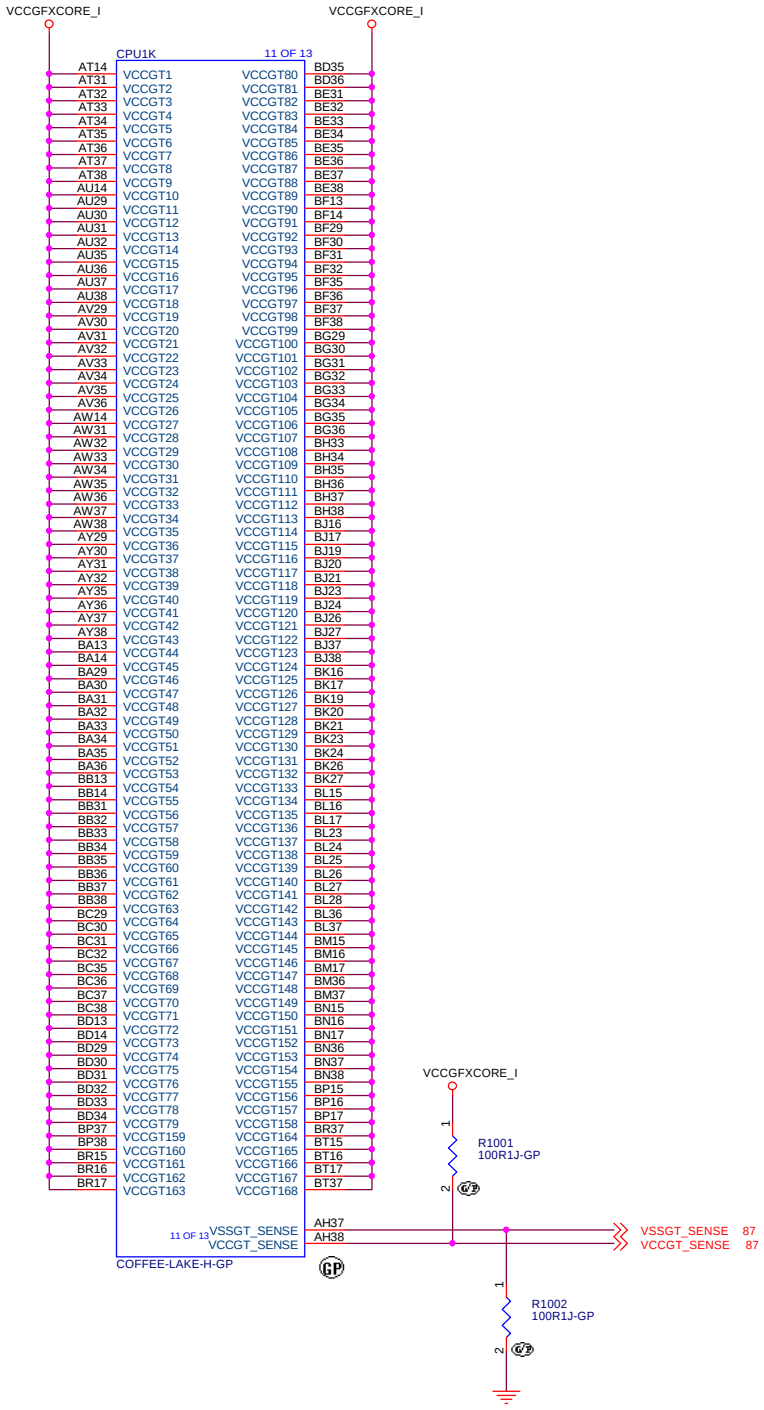
Title: **CPU CFL-H VCC**

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 9 of 110



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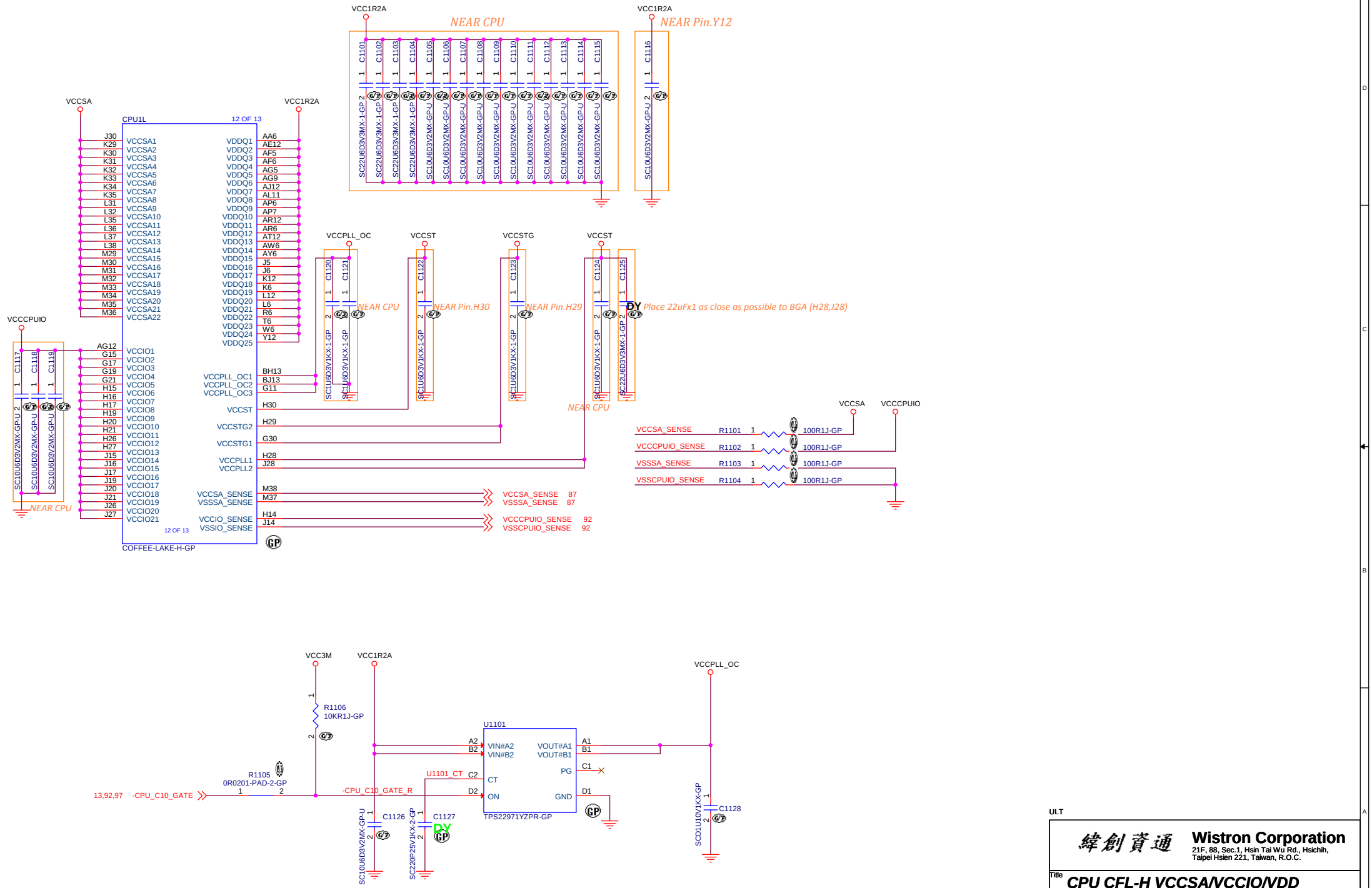
Title: ***CPU CFL-H VCCGT***

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 10 of 110



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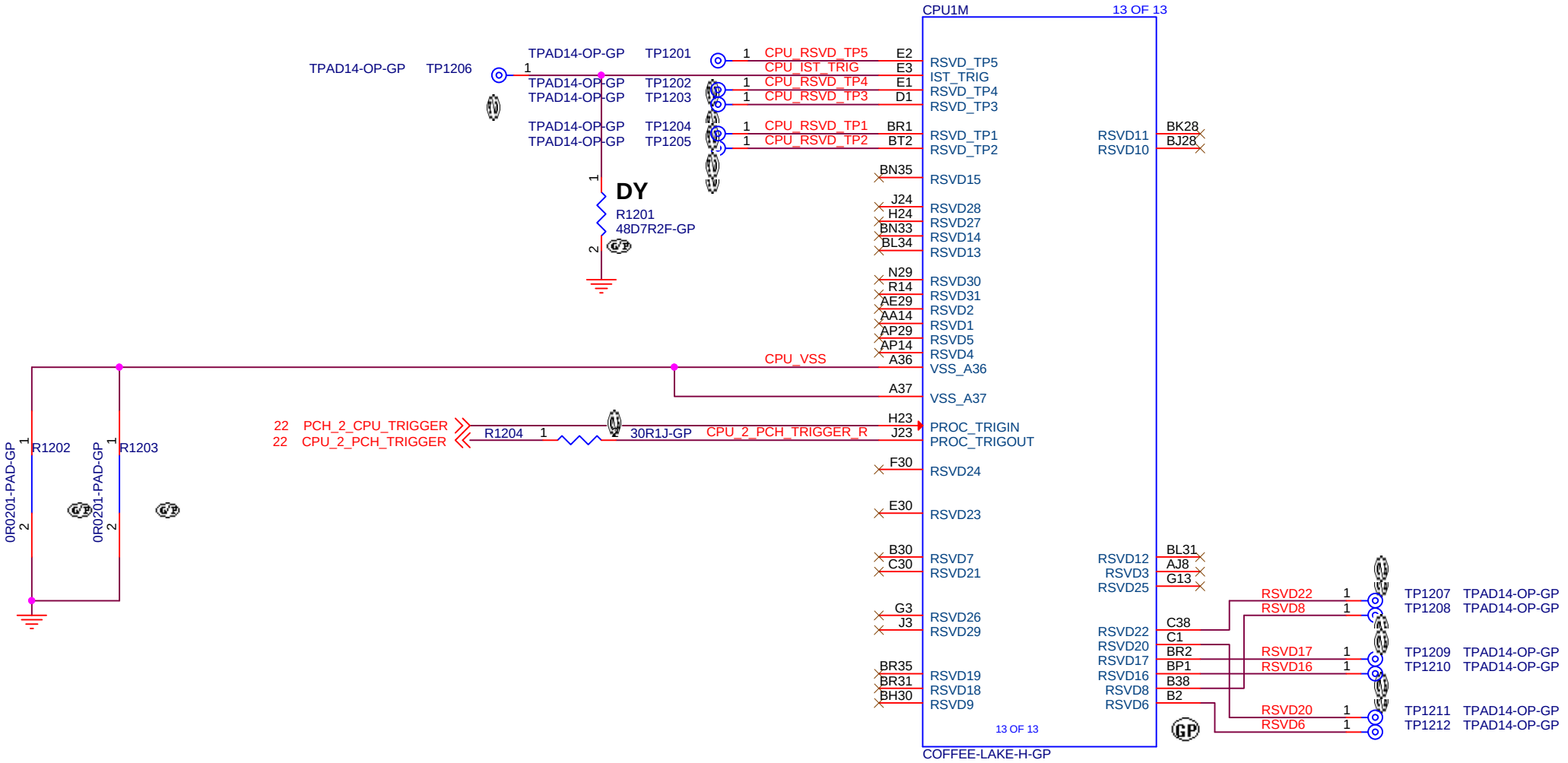
Title: CPU CFL-H VCCSA/VCCIO/VDD

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 11 of 110



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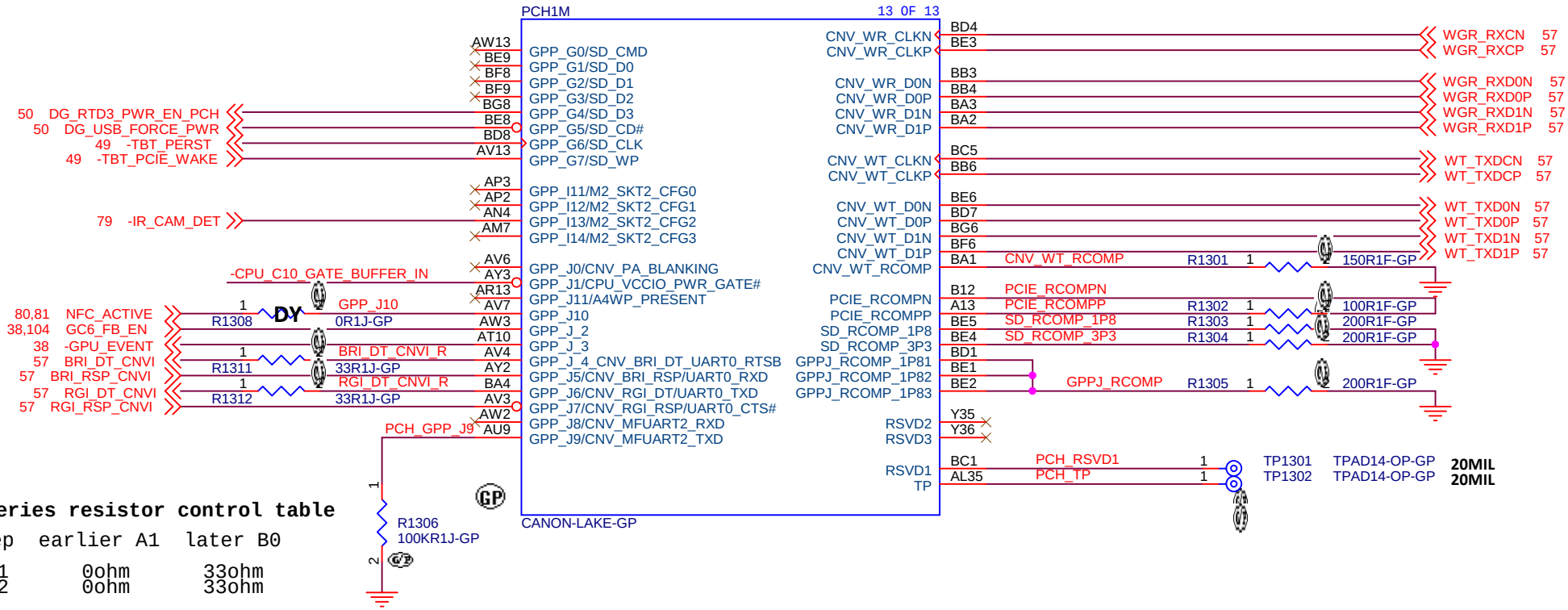
Title: ***CPU CFL-H RSVD***

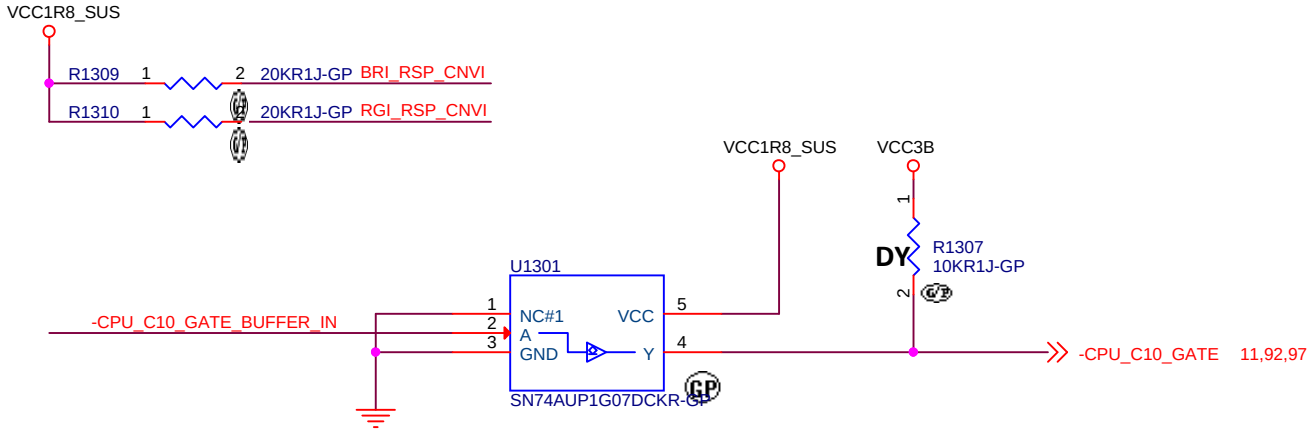
Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 12 of 110



CNVi BT series resistor control table

PCH Step	earlier A1	later B0
R1311	0ohm	33ohm
R1312	0ohm	33ohm



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Title: ***PCH CNL-H CNV***		
Size: A4	Document Number: **PADME**	Rev: 1
Date: Monday, October 01, 2018	Sheet 13 of 110	

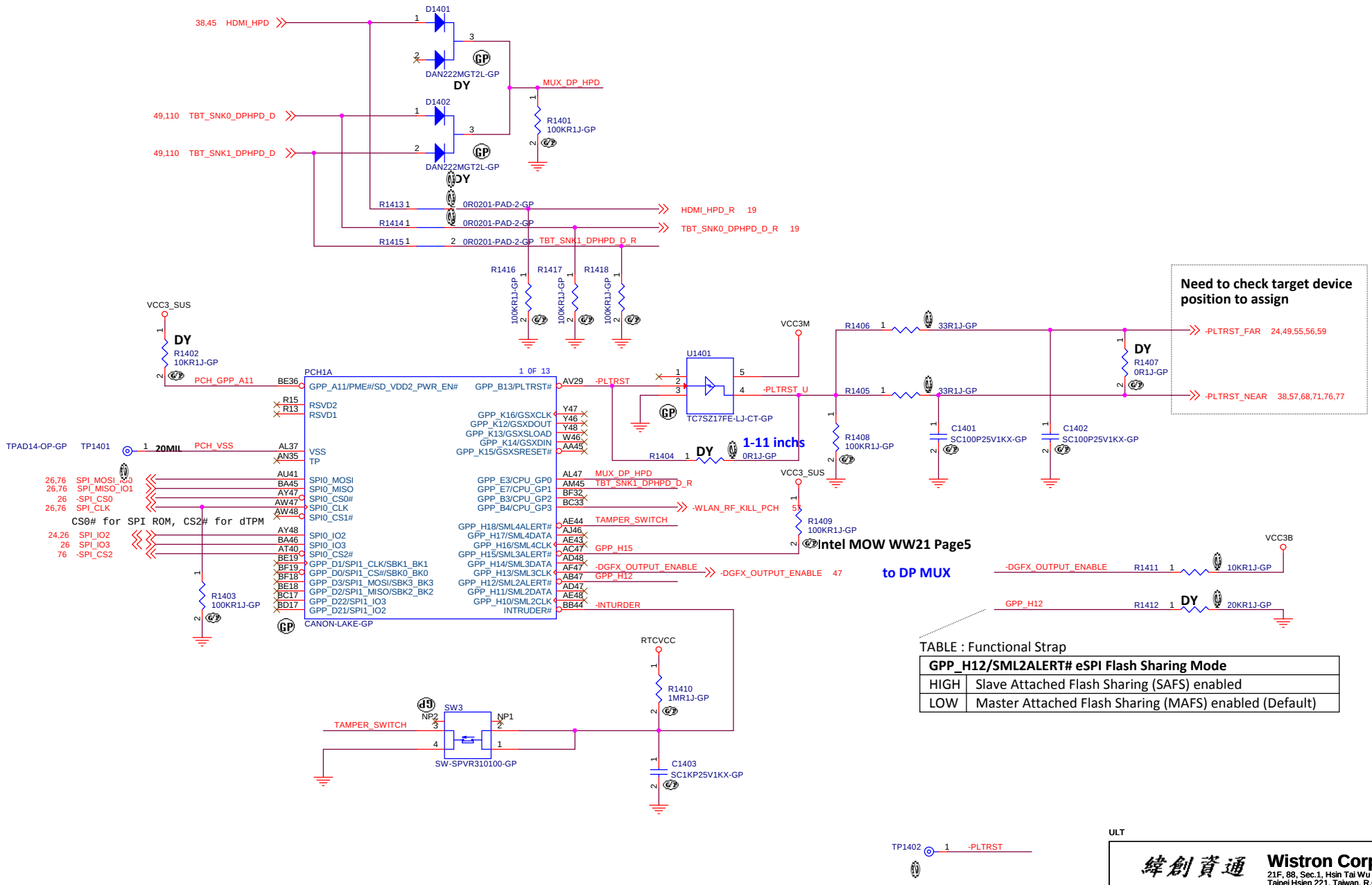

TABLE : Functional Strap

GPP_H12/SML2ALERT# eSPI Flash Sharing Mode	
HIGH	Slave Attached Flash Sharing (SAFS) enabled
LOW	Master Attached Flash Sharing (MAFS) enabled (Default)

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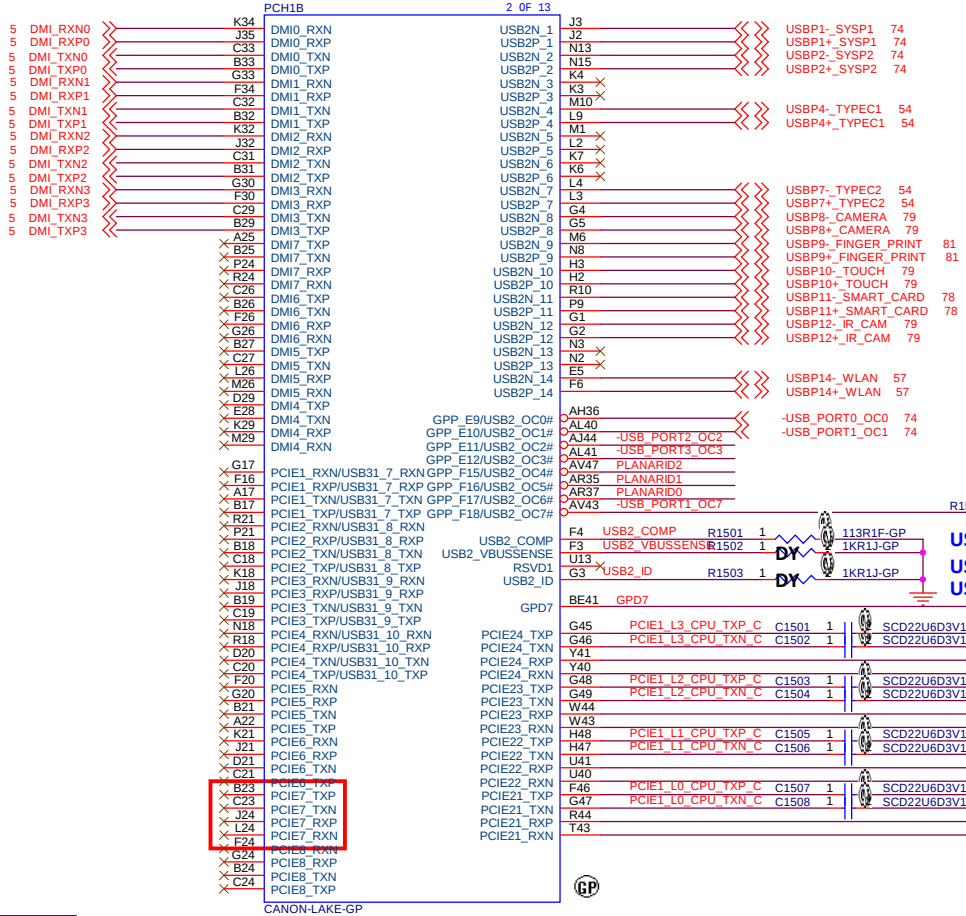
Title: **PCH CNL-H SPI**

Size	Document Number	Rev
A3	PADME	1

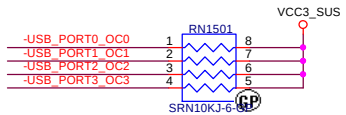
Date: Monday, October 01, 2018 Sheet 14 of 110

HSIO Port	CM246	Net Name
Port0	USB3.1 #1	USB3P1
Port1	USB3.1 #2	USB3P2
Port2	USB3.1 #3	USB3P3
Port3	USB3.1 #4	N/A
Port4	USB3.1 #5	N/A
Port5	USB3.1 #6	N/A
Port6	USB3.1 #7 / PCIe #1	N/A
Port7	USB3.1 #8 / PCIe #2	N/A
Port8	USB3.1 #9 / PCIe #3	N/A
Port9	USB3.1 #10 / PCIe #4	N/A
Port10	PCIe #5 / GbE	N/A
Port11	PCIe #6	N/A
Port12	PCIe #7	N/A
Port13	PCIe #8	N/A
Port14	PCIe #9 / GbE	PCIE12L3
Port15	PCIe #10	PCIE12L2
Port16	PCIe #11 / SATA #0a	PCIE12L1
Port17	PCIe #12 / SATA #1a / GbE	PCIE12L0_SATA1A
Port18	PCIe #13 / SATA #0b / GbE	PCIE13
Port19	PCIe #14 / SATA #1b	N/A
Port20	PCIe #15	PCIE15
Port21	PCIe #16	PCIE16
Port22	PCIe #17 / SATA #4	PCIE17L0_SATA4
Port23	PCIe #18 / SATA #5	PCIE17L1
Port24	PCIe #19 / SATA #6	PCIE17L2
Port25	PCIe #20 / SATA #7	PCIE17L3
Port26	PCIe #21	PCIE21L0
Port27	PCIe #22	PCIE21L1
Port28	PCIe #23	PCIE21L2
Port29	PCIe #24	PCIE21L3

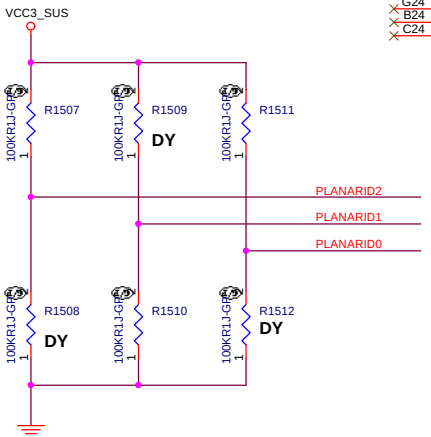
PCIe Port Assignment	
Port9	M.2 SSD0 (PCIe L3)
Port10	M.2 SSD0 (PCIe L2)
Port11	M.2 SSD0 (PCIe L1)
Port12	M.2 SSD0 (PCIe L0)
Port13	GbE PHY
Port14	N/A
Port15	WLAN
Port16	WWAN
Port17	M.2 SSD1 (PCIe L0)
Port18	M.2 SSD1 (PCIe L1)
Port19	M.2 SSD1 (PCIe L2)
Port20	M.2 SSD1 (PCIe L3)
Port21	Thunderbolt (PCIe L0)
Port22	Thunderbolt (PCIe L1)
Port23	Thunderbolt (PCIe L2)
Port24	Thunderbolt (PCIe L3)



USB2.0 Port Assignment	
Port1	System Port (AOU)
Port2	System Port
Port3	N/A
Port4	USB Type-C #1
Port5	N/A
Port6	N/A
Port7	USB Type-C #2
Port8	2D CAMERA
Port9	Fingerprint Reader
Port10	Touch Panel
Port11	Smart Card Reader
Port12	IR Camera
Port13	N/A
Port14	WLAN (Bluetooth)



USB2_COMP RES : Place within 1 inch
USB2_VBUSSENSE / USB2_ID
USB OTG FUNCTION SUPPORT



Planar ID Table

Phase	ID2	ID1	ID0
EVT	0	0	1
FVT	0	1	0
SIT	0	1	1
SIT-R	1	0	0
SVT	1	0	1

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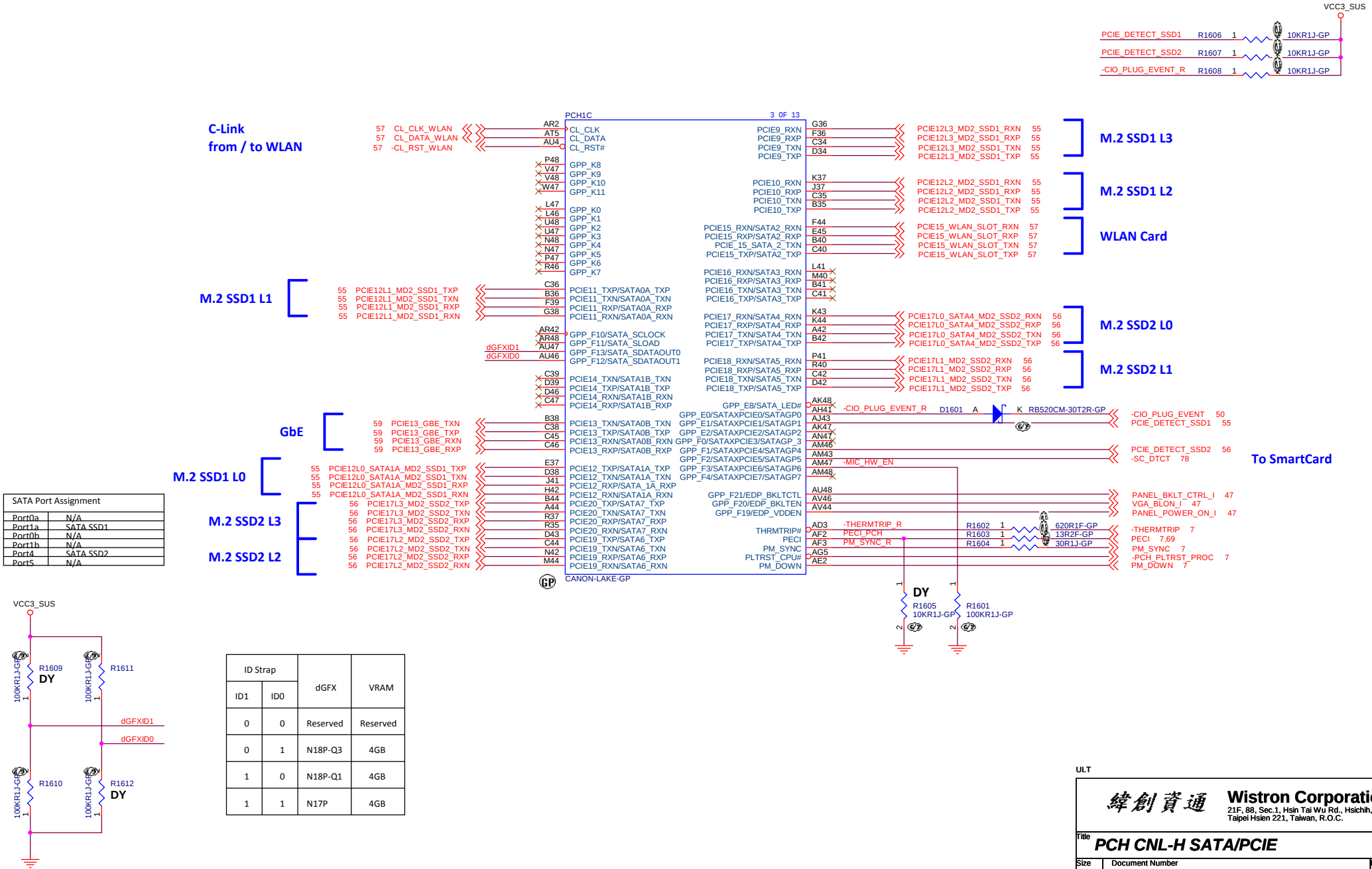
Title: **PCH CNL-H DMI/PCIE/USB**

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 15 of 110



SATA Port Assignment	
Port0a	N/A
Port1a	SATA SSD1
Port0b	N/A
Port1b	N/A
Port4	SATA SSD2
Port5	N/A

ID Strap		dGFX	VRAM
ID1	ID0		
0	0	Reserved	Reserved
0	1	N18P-Q3	4GB
1	0	N18P-Q1	4GB
1	1	N17P	4GB

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Title **PCH CNL-H SATA/PCIE**

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 16 of 110

TABLE : Functional Strap

HDA_SDO/I2S0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descritor and/or the ME regions of the SPI after MFG Done bit is set.

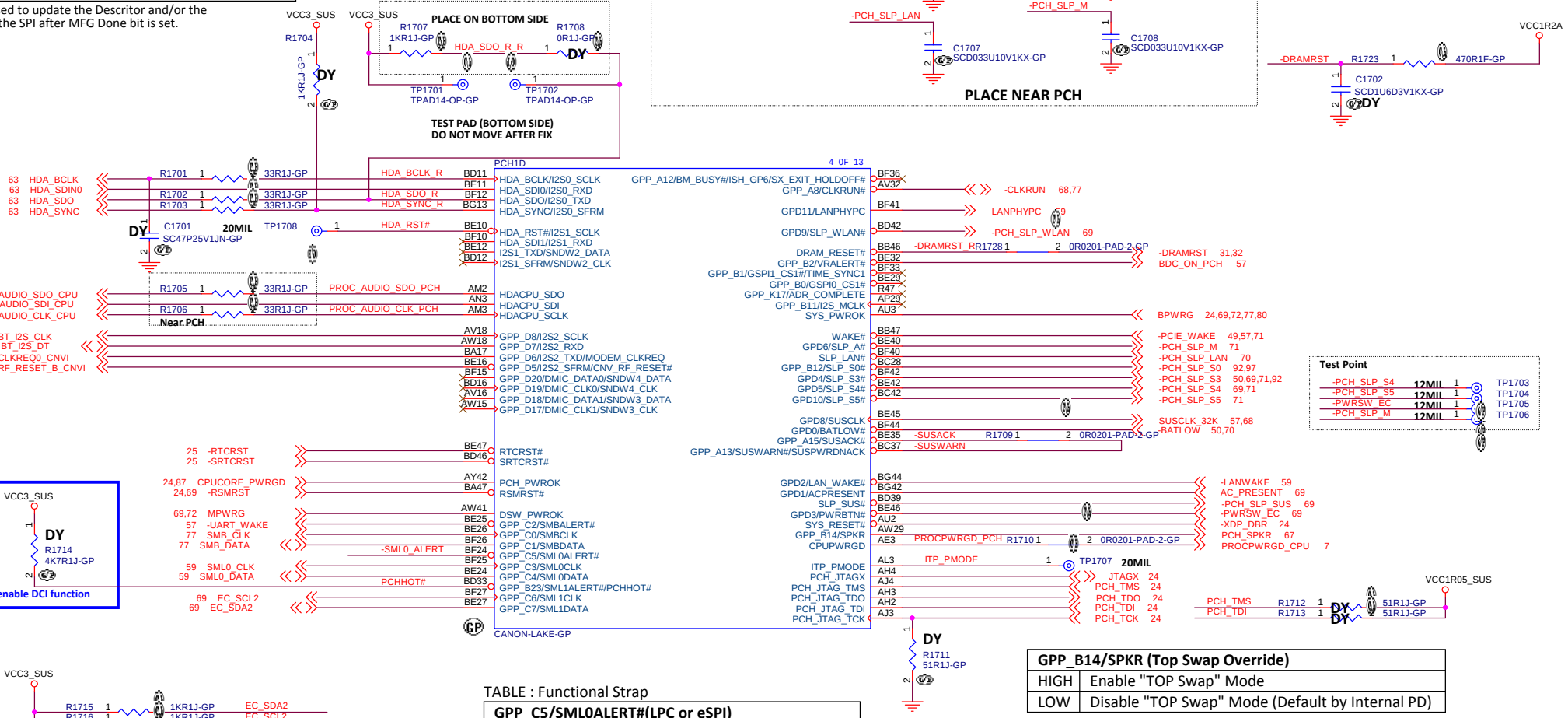

TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

GPP_C2/SMBALERT# (TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confldentlality
LOW	Disable ME Crypto TLS(Default)

TABLE : Functional Strap

GPP_B23/SML1ALERT#/PCHHOT#(Intel DCI-OOB)	
HIGH	Enable Intel DCI-OOB
LOW	Disable Intel DCI-OOB (Default)

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)

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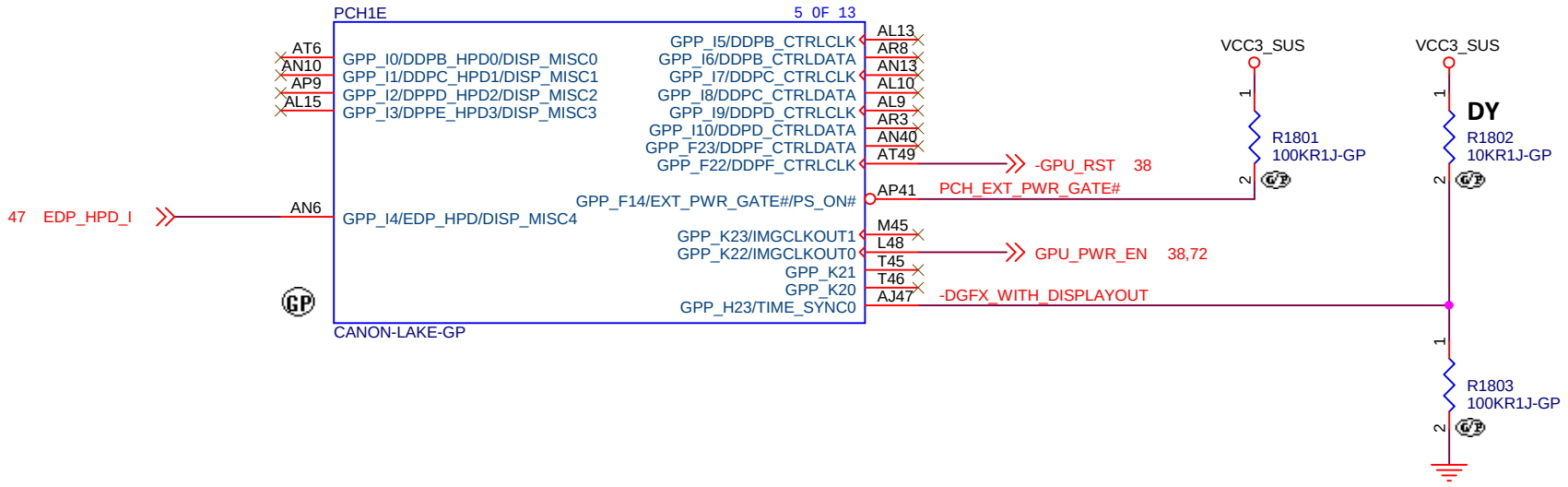
Title: PCH CNL-H AUDIO/SMBUS/JTAG

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 17 of 110



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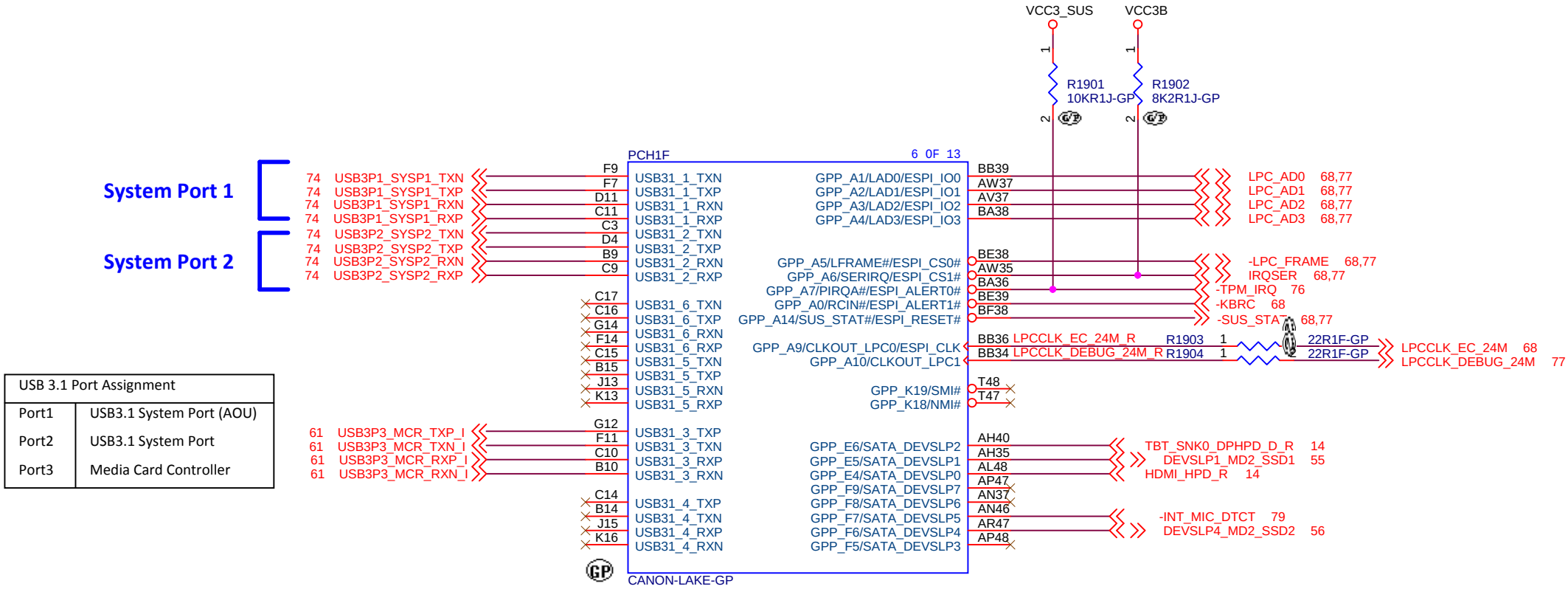
Title **PCH CNL-H DDI CONTROL**

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 18 of 110



USB 3.1 Port Assignment	
Port1	USB3.1 System Port (AOU)
Port2	USB3.1 System Port
Port3	Media Card Controller

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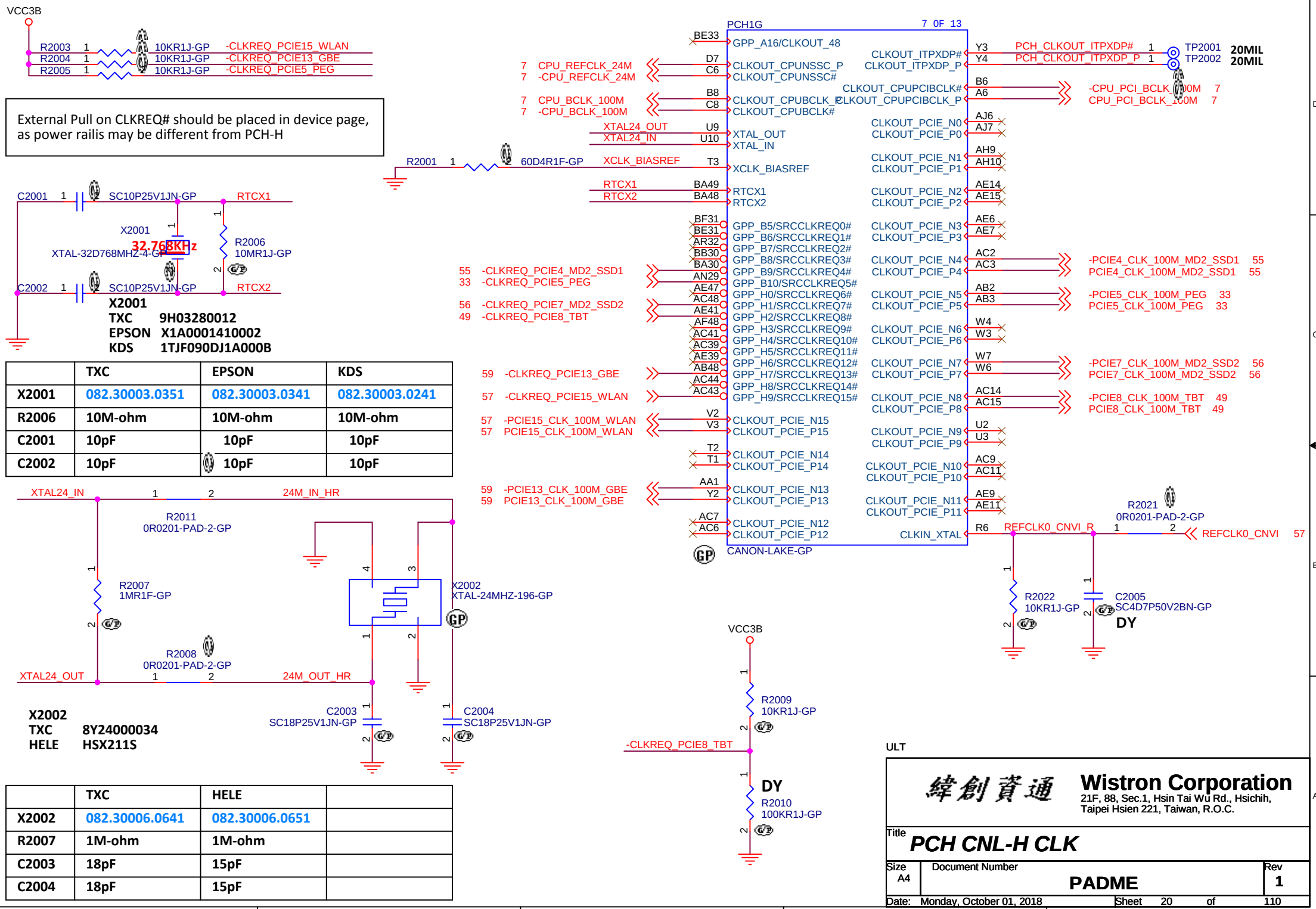
Title **PCH CNL-H USB3/LPC**

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 19 of 110



	TXC	EPSON	KDS
X2001	082.30003.0351	082.30003.0341	082.30003.0241
R2006	10M-ohm	10M-ohm	10M-ohm
C2001	10pF	10pF	10pF
C2002	10pF	10pF	10pF

	TXC	HELE	
X2002	082.30006.0641	082.30006.0651	
R2007	1M-ohm	1M-ohm	
C2003	18pF	15pF	
C2004	18pF	15pF	

ULT

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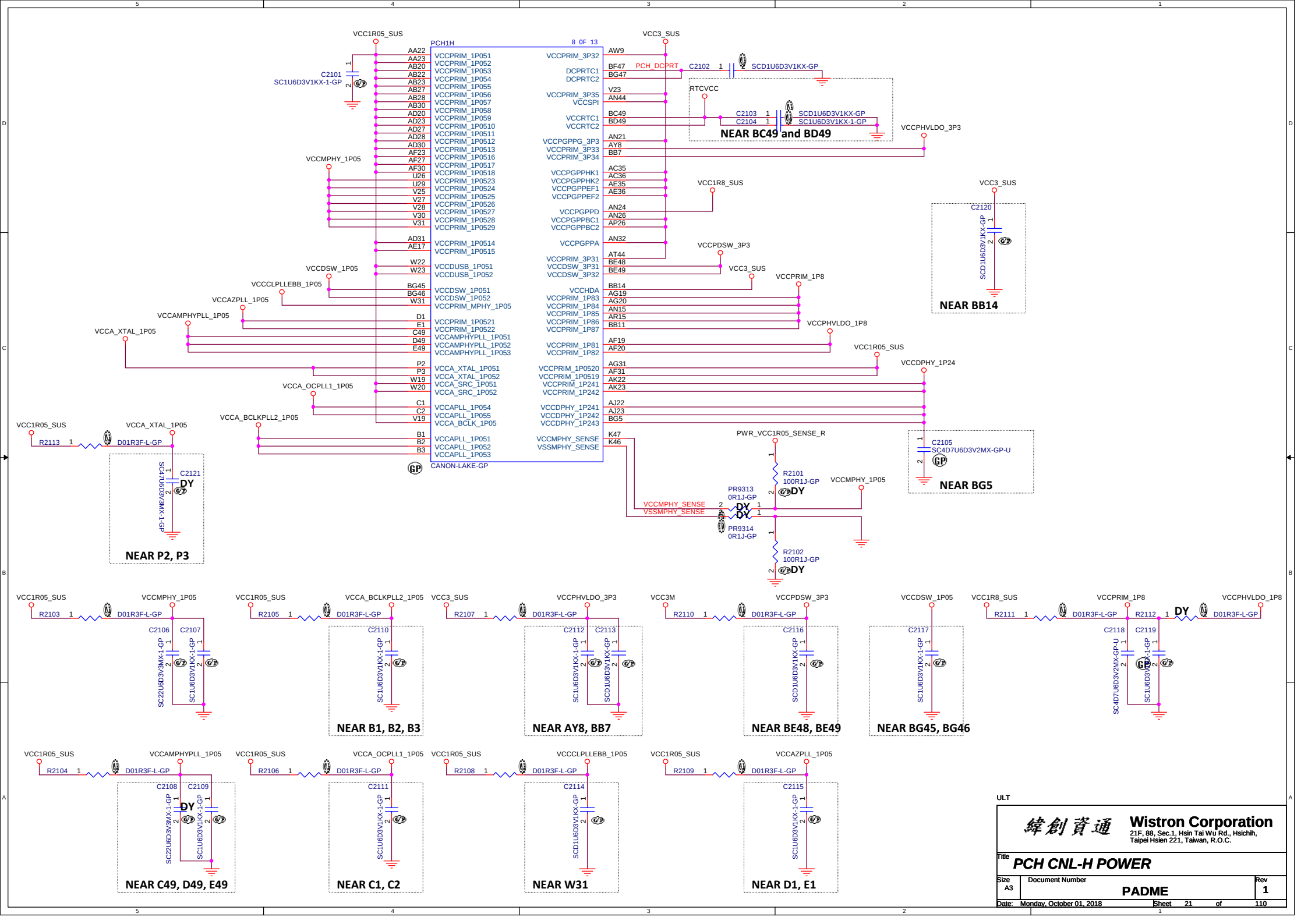
Title **PCH CNL-H CLK**

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 20 of 110


PCH1H
8 OF 13
CANON-LAKE-GP
VCC1R05_SUS
VCC3_SUS
VCCMPHY_1P05
VCCDSW_1P05
VCCCLPLLEBB_1P05
VCCAZPLL_1P05
VCCAMPHYPLL_1P05
VCCA_XTAL_1P05
VCCA_OCPLL1_1P05
VCCA_BCLKPLL2_1P05
VCC1R8_SUS
VCCPDSW_3P3
VCCPRIM_1P8
VCCPHVLDO_1P8
VCCPHVLDO_3P3
VCCDPHY_1P24
RTCVCC
PCH_DCPRT
C2101 SC1U6D3V1KX-1-GP
C2102 SCD1U6D3V1KX-GP
C2103 SCD1U6D3V1KX-GP
C2104 SC1U6D3V1KX-1-GP
NEAR BC49 and BD49
C2120 SCD1U6D3V1KX-GP
NEAR BB14
C2105 SC4D7U6D3V2MX-GP-U
NEAR BG5
R2113 D01R3F-L-GP
C2121 SC47U6D3V3MX-1-GP
DY
NEAR P2, P3
PWR_VCC1R05_SENSE_R
R2101 100R1J-GP
R2102 100R1J-GP
PR9313 0R1J-GP
PR9314 0R1J-GP
VCCMPHY_SENSE
VSSMPHY_SENSE
R2103 D01R3F-L-GP
C2106 SC22U6D3V3MX-1-GP
C2107 SC1U6D3V1KX-1-GP
R2105 D01R3F-L-GP
C2110 SC1U6D3V1KX-GP
NEAR B1, B2, B3
R2107 D01R3F-L-GP
C2112 SC1U6D3V1KX-GP
C2113 SCD1U6D3V1KX-GP
NEAR AY8, BB7
VCC3M
R2110 D01R3F-L-GP
C2116 SCD1U6D3V1KX-GP
NEAR BE48, BE49
C2117 SC1U6D3V1KX-GP
NEAR BG45, BG46
R2111 D01R3F-L-GP
R2112 D01R3F-L-GP
C2118 SC4D7U6D3V2MX-GP-U
C2119 SC1U6D3V1KX-GP
R2104 D01R3F-L-GP
C2108 SC22U6D3V3MX-1-GP
C2109 SC1U6D3V1KX-1-GP
NEAR C49, D49, E49
R2106 D01R3F-L-GP
C2111 SC1U6D3V1KX-GP
NEAR C1, C2
R2108 D01R3F-L-GP
C2114 SCD1U6D3V1KX-GP
NEAR W31
R2109 D01R3F-L-GP
C2115 SC1U6D3V1KX-1-GP
NEAR D1, E1
ULT
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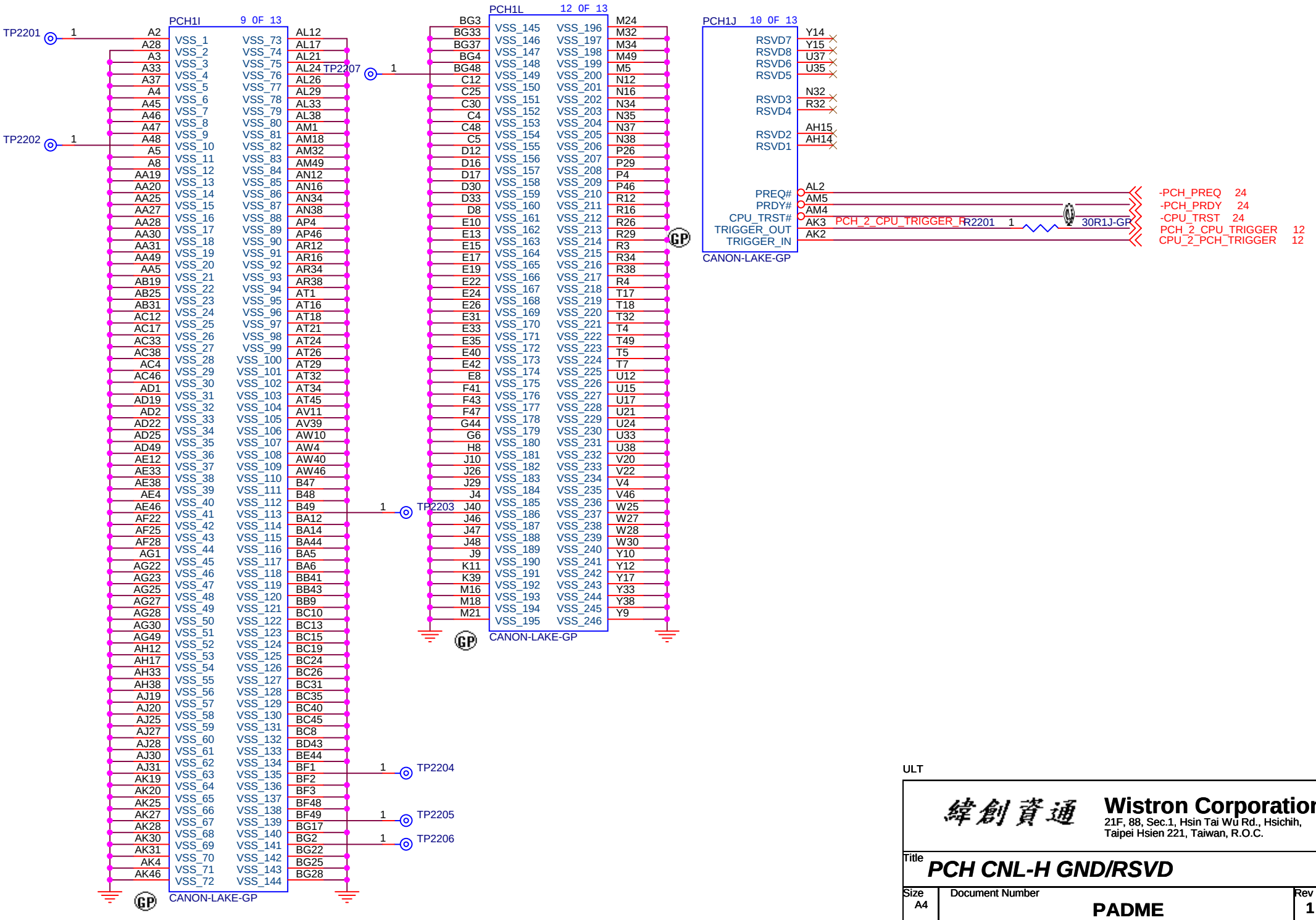
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH CNL-H POWER
Size A3
Document Number
PADME
Rev 1
Date: Monday, October 01, 2018
Sheet 21 of 110



ULT

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Title: **PCH CNL-H GND/RSVD**

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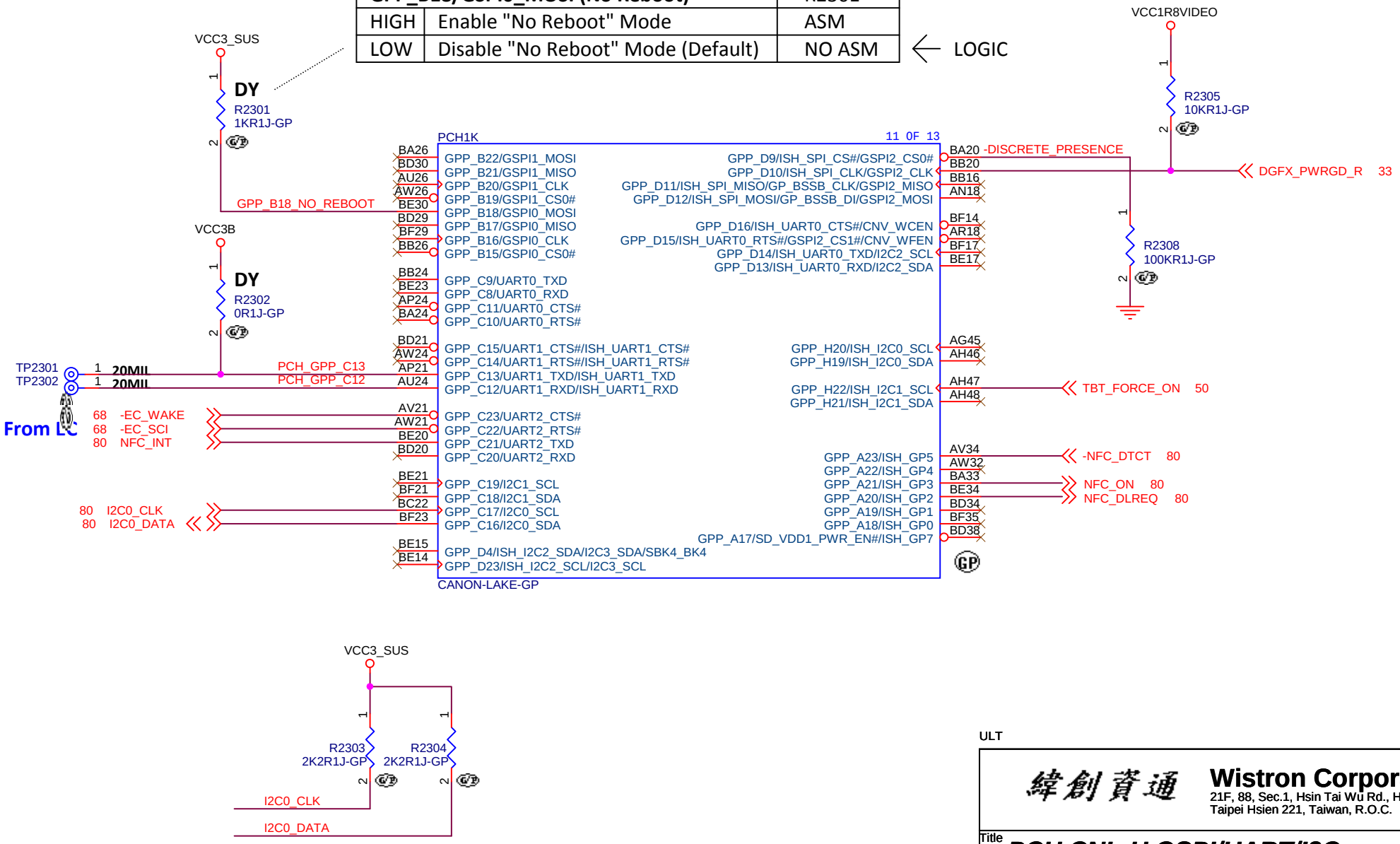
TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R2301
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

← LOGIC



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Title: **PCH CNL-H GSPI/UART/I2C**

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 23 of 110

XDP

TABLE : CPU ITP DEBUG REPORT

		NO Use	Individual Port	DCI 2.0 w/o connector
XDPR1	R2401	NO ASM	NO ASM	ASM
XDPR27	R2428	NO ASM	ASM	NO ASM
XDPR28	R2408	NO ASM	ASM	NO ASM
XDPR11	R2413	NO ASM	ASM	ASM
XDPC1	C2401	NO ASM	ASM	NO ASM
PCHR142	R2411	NO ASM	ASM	ASM
XDPR23	R2424	NO ASM	ASM	NO ASM
XDPR14	R2418	NO ASM	ASM	ASM
XDPR16	R2416	NO ASM	ASM	ASM
XDPR19	R2420	NO ASM	ASM	ASM
XDPR20	R2421	NO ASM	ASM	ASM
XDPR17	R2417	NO ASM	ASM	ASM
XDPR18	R2419	NO ASM	ASM	ASM
XDPR22	R2423	NO ASM	ASM	ASM
XDPR24	R2425	NO ASM	ASM	ASM
XDPR25	R2426	NO ASM	ASM	ASM
XDPR26	R2427	NO ASM	ASM	ASM

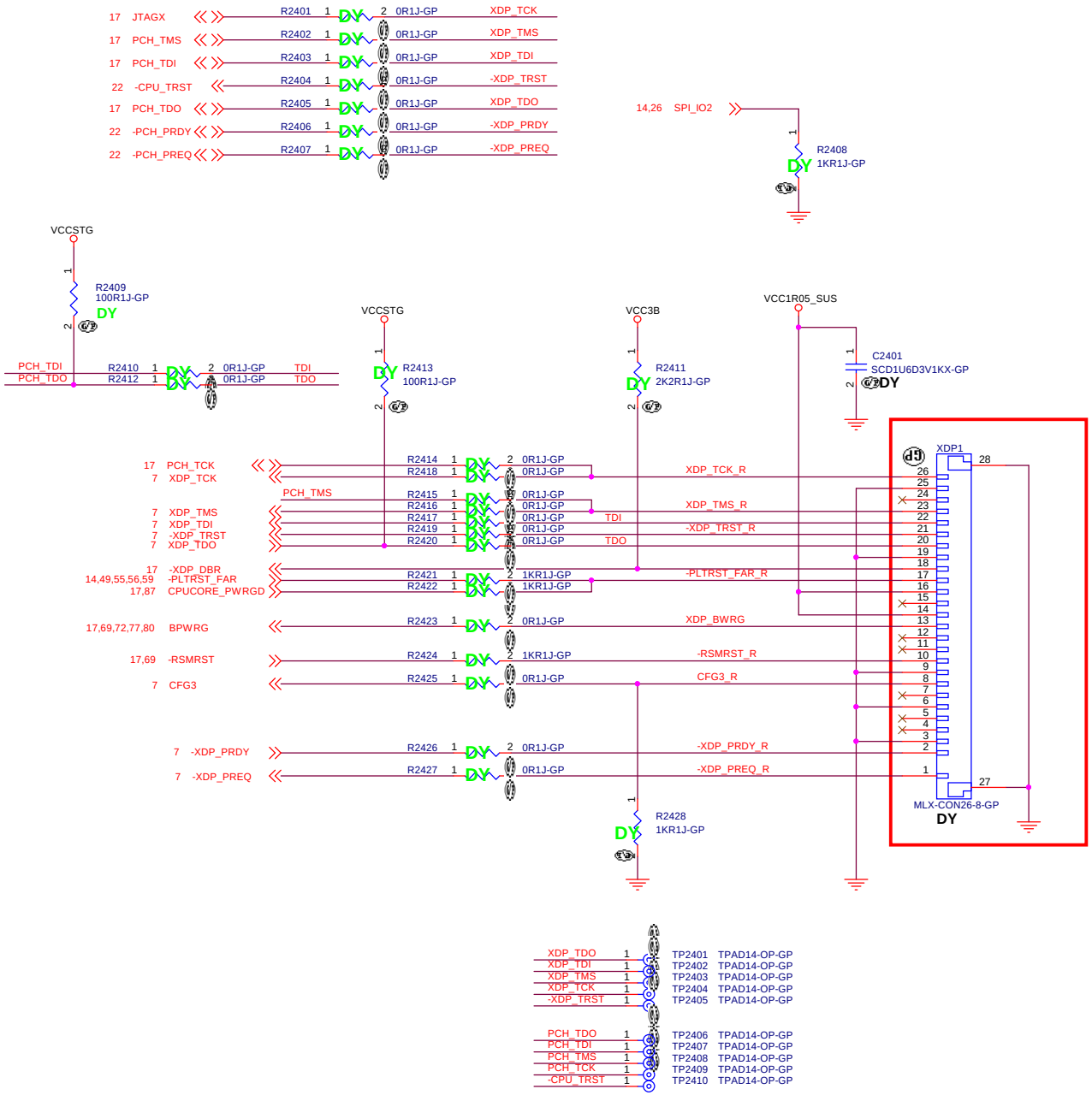
LOGIC

TABLE : PCH ITP DEBUG REPORT

		NO Use	Individual Port	DCI 2.0 w/o connector
XDPR8	R2409	NO ASM	ASM	NO ASM
XDPR21	R2422	NO ASM	ASM	NO ASM
XDPR23	R2424	NO ASM	ASM	NO ASM
XDPR13	R2414	NO ASM	ASM	NO ASM
XDPR15	R2415	NO ASM	ASM	NO ASM
XDPR9	R2410	NO ASM	ASM	NO ASM
XDPR10	R2412	NO ASM	ASM	NO ASM

LOGIC

PCHR31	R1711	NO ASM	ASM	NO ASM
PCHR32	R1712	NO ASM	ASM	NO ASM
PCHR33	R1713	NO ASM	ASM	NO ASM



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Title: XDP CONNECTOR

Size	Document Number	Rev
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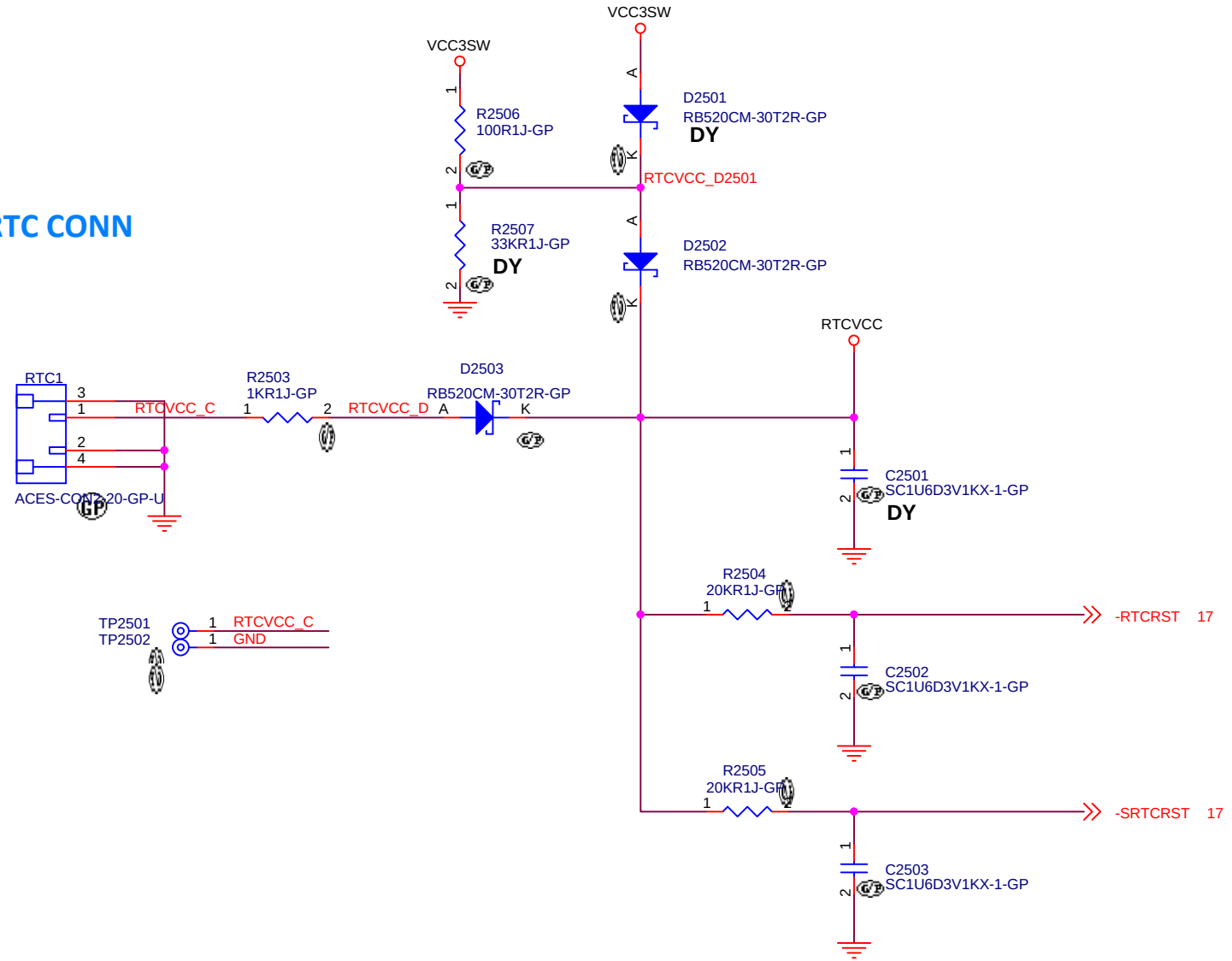
RTC

RTC CONN



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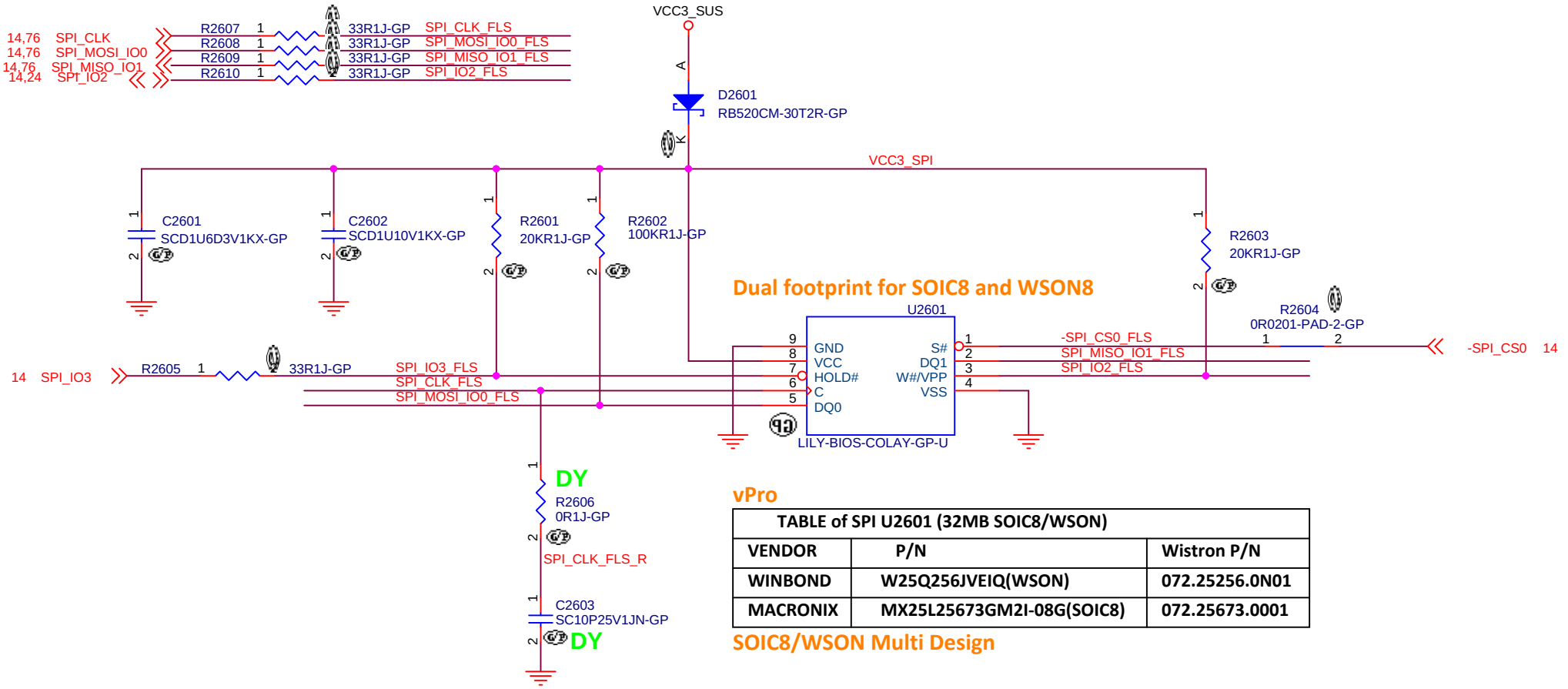
Title: ***RTC BATTERY***		
Size: A4	Document Number: **PADME**	Rev: 1
Date: Monday, October 01, 2018	Sheet 25 of 110	



vPro

TABLE of SPI U2601 (32MB SOIC8/WSON)		
VENDOR	P/N	Wistron P/N
WINBOND	W25Q256JVEIQ(WSON)	072.25256.0N01
MACRONIX	MX25L25673GM2I-08G(SOIC8)	072.25673.0001

SOIC8/WSON Multi Design

non-vPRO

TABLE of SPI U2601 (16MB)		
VENDOR	P/N	Wistron P/N
WINBOND	W25Q128JVSIQ	072.25128.0B71
MACRONIX	MX25L12873FM2I-10G	72.12873.001

ULT

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Title: **SPI FLASH**

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Reserved

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Title ***Reserved***

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Reserved

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Title ***Reserved***

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Title ***Reserved***

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Reserved

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Title ***Reserved***

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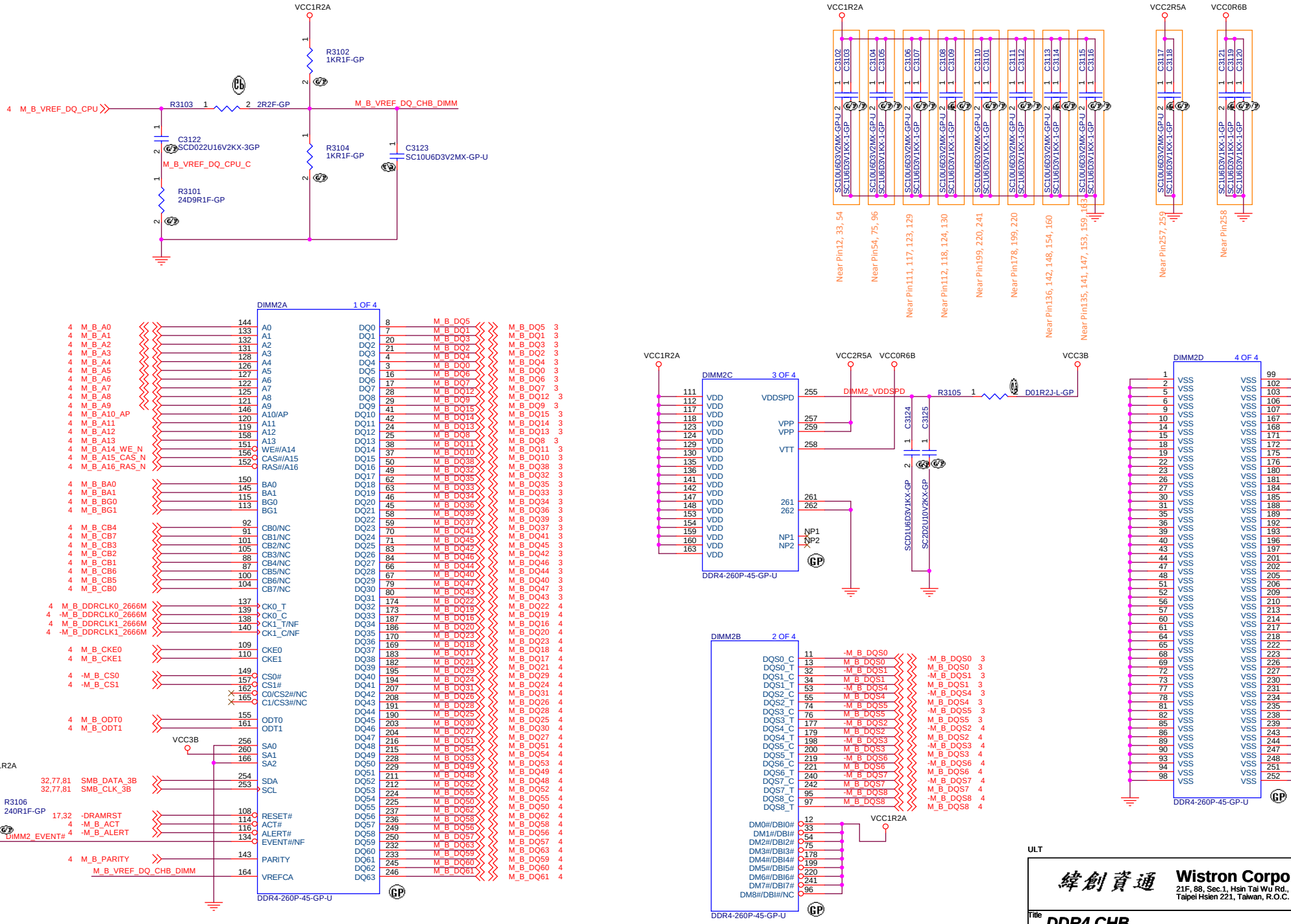
VCC1R2A
R3102
1KR1F-GP
4 M_B_VREF_DQ_CPU
R3103
2R2F-GP
M_B_VREF_DQ_CHB_DIMM
C3122
SCD022U16V2KX-3GP
M_B_VREF_DQ_CPU_C
R3104
1KR1F-GP
C3123
SC10U6D3V2MX-GP-U
R3101
24D9R1F-GP
VCC1R2A
VCC2R5A
VCC0R6B
C3102
C3103
C3104
C3105
C3106
C3107
C3108
C3109
C3110
C3101
C3111
C3112
C3113
C3114
C3115
C3116
C3117
C3118
C3121
C3119
C3120
SC10U6D3V2MX-GP-U
SC1U6D3V1KX-1-GP
Near Pin12, 33, 54
Near Pin54, 75, 96
Near Pin111, 117, 123, 129
Near Pin112, 118, 124, 130
Near Pin199, 220, 241
Near Pin178, 199, 220
Near Pin136, 142, 148, 154, 160
Near Pin135, 141, 147, 153, 159, 163
Near Pin257, 259
Near Pin258
DIMM2A 1 OF 4
DDR4-260P-45-GP-U
VCC1R2A
VCC2R5A
VCC0R6B
VCC3B
DIMM2C 3 OF 4
DIMM2_VDDSPD
R3105
D01R2J-L-GP
SCD1U6D3V1KX-GP
SC22D2U10V2KX-GP
DIMM2D 4 OF 4
DIMM2B 2 OF 4
VCC3B
VCC1R2A
R3106
240R1F-GP
DIMM2_EVENT#
SMB_DATA_3B
SMB_CLK_3B
-DRAMRST
-M_B_ACT
-M_B_ALERT
M_B_VREF_DQ_CHB_DIMM
ULT
緯創資通
Wistron Corporation
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Title
DDR4 CHB
Size
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Document Number
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1
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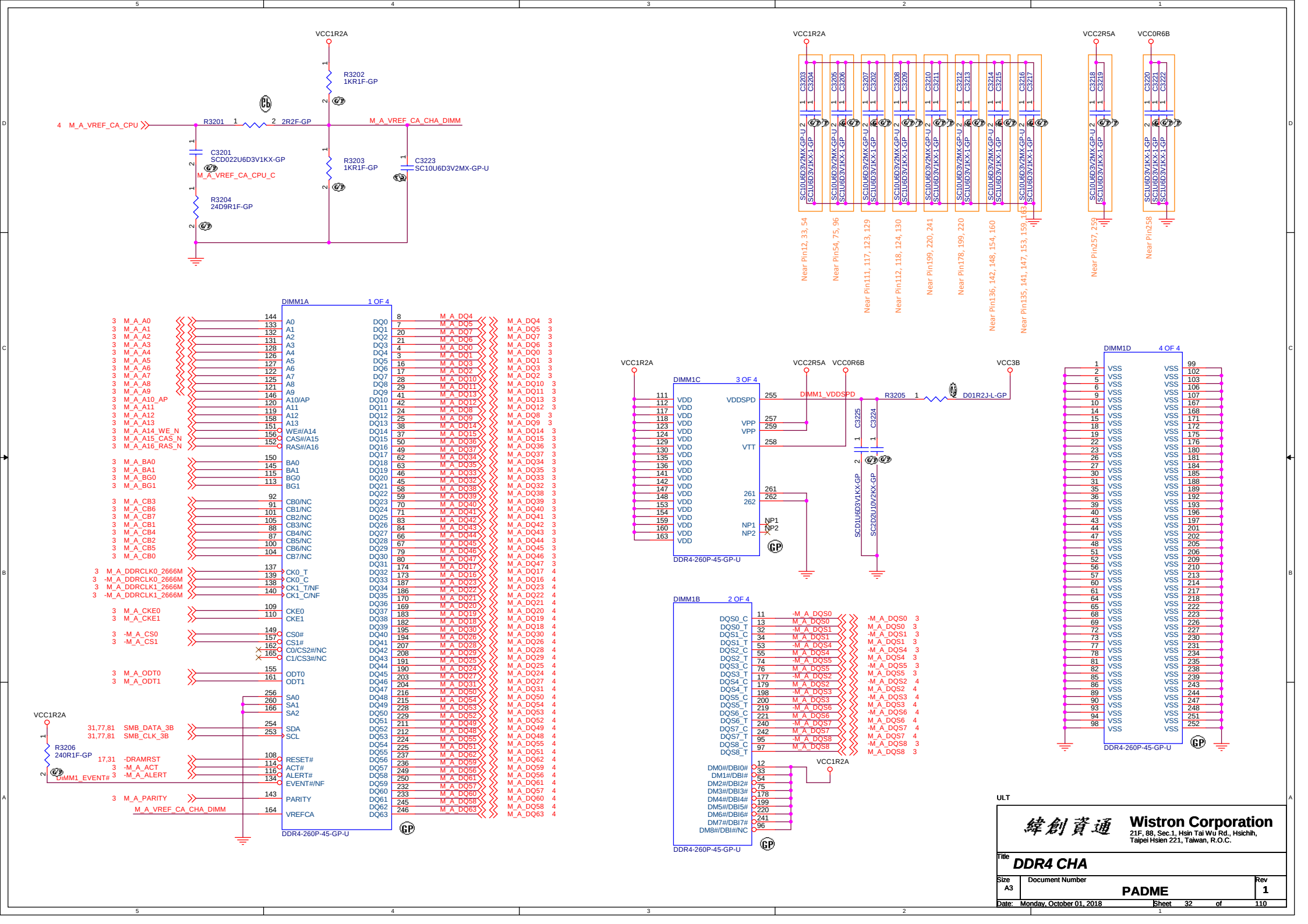
VCC1R2A
R3202
1KR1F-GP
M_A_VREF_CA_CPU
R3201
2R2F-GP
M_A_VREF_CA_CHA_DIMM
C3201
SCD022U6D3V1KX-GP
M_A_VREF_CA_CPU_C
R3203
1KR1F-GP
C3223
SC10U6D3V2MX-GP-U
R3204
24D9R1F-GP
VCC2R5A
VCC0R6B
C3203
C3204
C3205
C3206
C3207
C3208
C3209
C3210
C3211
C3212
C3213
C3214
C3215
C3216
C3217
C3218
C3219
C3220
C3221
C3222
SC10U6D3V2MX-GP-U
SC10U6D3V1KX-1-GP
Near Pin12, 33, 54
Near Pin54, 75, 96
Near Pin111, 117, 123, 129
Near Pin112, 118, 124, 130
Near Pin199, 220, 241
Near Pin178, 199, 220
Near Pin136, 142, 148, 154, 160
Near Pin135, 141, 147, 153, 159, 163
Near Pin257, 259
Near Pin258
DIMM1A
1 OF 4
DDR4-260P-45-GP-U
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10_AP
M_A_A11
M_A_A12
M_A_A13
M_A_A14_WE_N
M_A_A15_CAS_N
M_A_A16_RAS_N
M_A_BA0
M_A_BA1
M_A_BG0
M_A_BG1
M_A_CB3
M_A_CB6
M_A_CB7
M_A_CB1
M_A_CB4
M_A_CB2
M_A_CB5
M_A_CB0
M_A_DDRCLK0_2666M
-M_A_DDRCLK0_2666M
M_A_DDRCLK1_2666M
-M_A_DDRCLK1_2666M
M_A_CKE0
M_A_CKE1
-M_A_CS0
-M_A_CS1
M_A_ODT0
M_A_ODT1
M_A_DQ0
M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ5
M_A_DQ6
M_A_DQ7
M_A_DQ8
M_A_DQ9
M_A_DQ10
M_A_DQ11
M_A_DQ12
M_A_DQ13
M_A_DQ14
M_A_DQ15
M_A_DQ16
M_A_DQ17
M_A_DQ18
M_A_DQ19
M_A_DQ20
M_A_DQ21
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M_A_DQ24
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M_A_DQ26
M_A_DQ27
M_A_DQ28
M_A_DQ29
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M_A_DQ33
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M_A_DQ35
M_A_DQ36
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M_A_DQ52
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M_A_DQ54
M_A_DQ55
M_A_DQ56
M_A_DQ57
M_A_DQ58
M_A_DQ59
M_A_DQ60
M_A_DQ61
M_A_DQ62
M_A_DQ63
VCC1R2A
R3206
240R1F-GP
SMB_DATA_3B
SMB_CLK_3B
-DRAMRST
-M_A_ACT
-M_A_ALERT
DIMM1_EVENT#
M_A_PARITY
M_A_VREF_CA_CHA_DIMM
DIMM1C
3 OF 4
DIMM1_VDDSPD
R3205
D01R2J-L-GP
VCC3B
SC1U6D3V1KX-GP
SC2D2U10V2KX-GP
DIMM1B
2 OF 4
DIMM1D
4 OF 4
ULT
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
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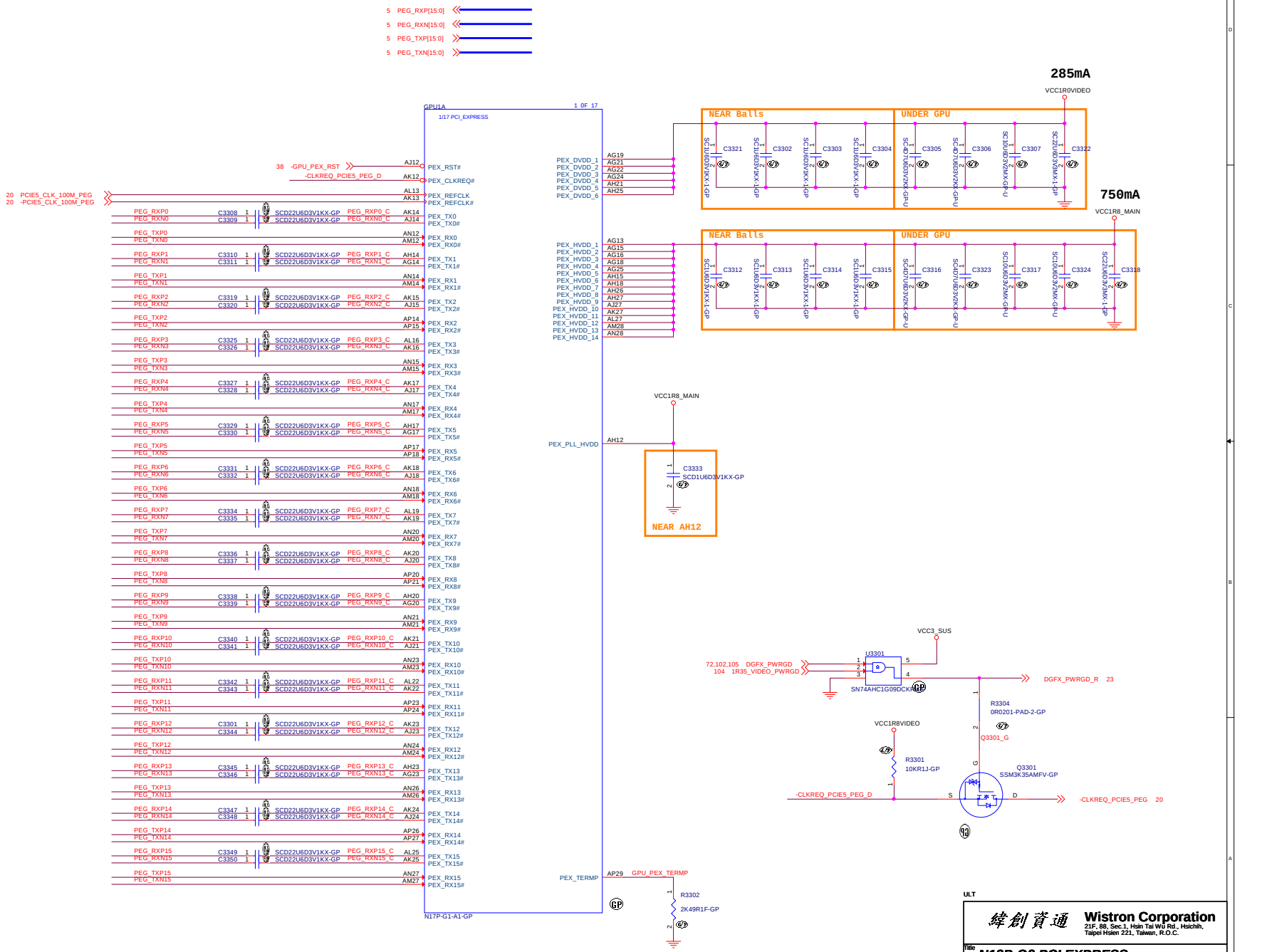
Size
A3
Document Number
PADME
Rev
1
Date: Monday, October 01, 2018
Sheet 32 of 110


5 PEG_RXP[15:0]
5 PEG_RXN[15:0]
5 PEG_TXP[15:0]
5 PEG_TXN[15:0]
285mA
VCC1R0VIDEO
750mA
VCC1R8_MAIN
GPU1A
1 OF 17
1/17 PCI_EXPRESS
NEAR Balls
UNDER GPU
38 -GPU_PEX_RST
-CLKREQ_PCIE5_PEG_D
20 PCIE5_CLK_100M_PEG
20 -PCIE5_CLK_100M_PEG
PEX_RST#
PEX_CLKREQ#
PEX_REFCLK
PEX_REFCLK#
PEX_DVDD_1
PEX_DVDD_2
PEX_DVDD_3
PEX_DVDD_4
PEX_DVDD_5
PEX_DVDD_6
PEX_HVDD_1
PEX_HVDD_2
PEX_HVDD_3
PEX_HVDD_4
PEX_HVDD_5
PEX_HVDD_6
PEX_HVDD_7
PEX_HVDD_8
PEX_HVDD_9
PEX_HVDD_10
PEX_HVDD_11
PEX_HVDD_12
PEX_HVDD_13
PEX_HVDD_14
PEX_PLL_HVDD
PEX_TERMP
GPU_PEX_TERMP
R3302
2K49R1F-GP
N17P-G1-A1-GP
C3333
SCD1U6D3V1KX-GP
NEAR AH12
U3301
SN74AHC1G09DCKR
72,102,105 DGFX_PWRGD
104 1R35_VIDEO_PWRGD
DGFX_PWRGD_R 23
R3304
0R0201-PAD-2-GP
Q3301_G
R3301
10KR1J-GP
Q3301
SSM3K35AMFV-GP
-CLKREQ_PCIE5_PEG 20
ULT
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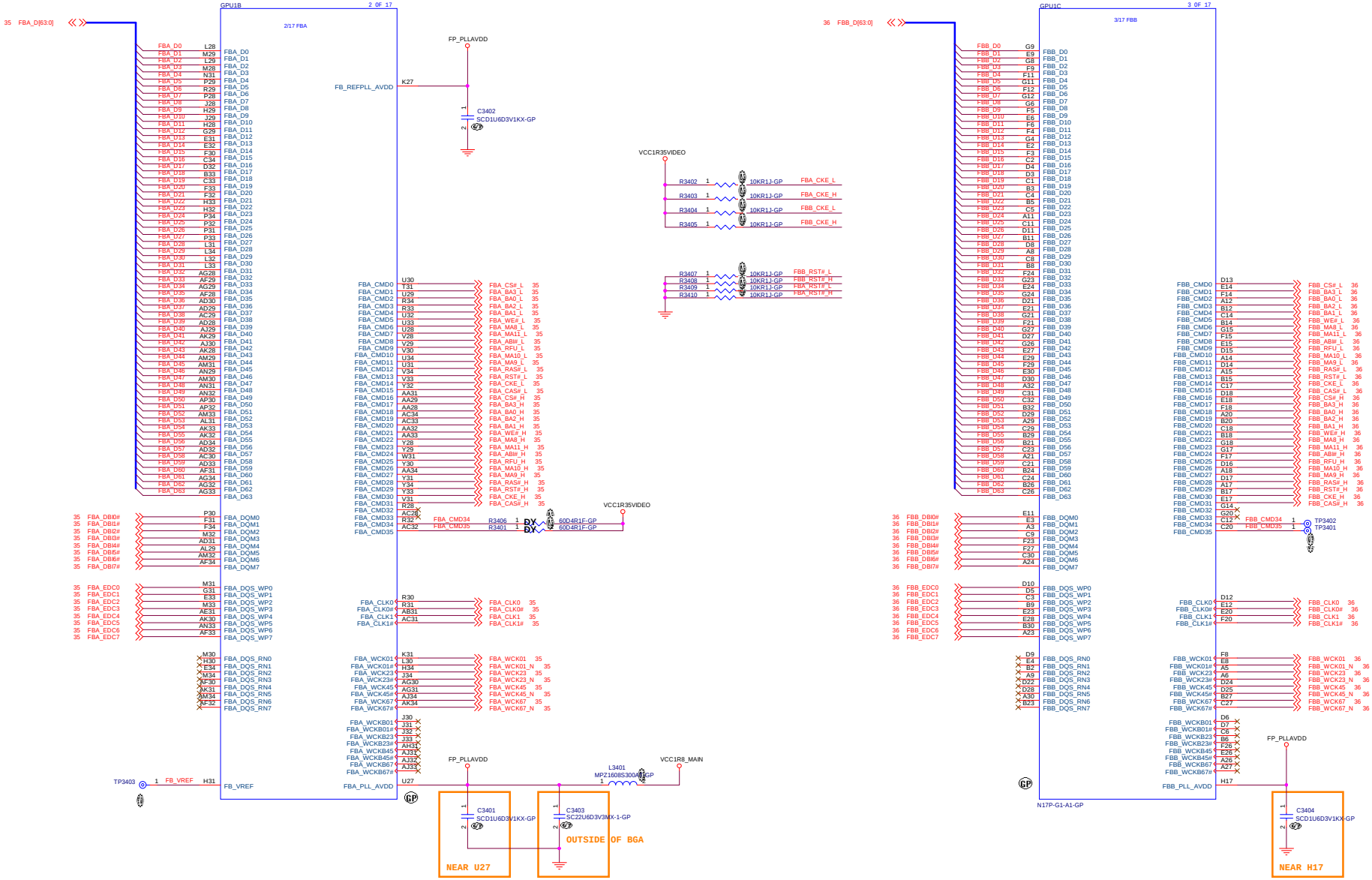
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N18P-Q3 PCI EXPRESS
Size
Custom
Document Number
PADME
Rev
1
Date: Monday, October 01, 2018
Sheet 33 of 110



ULT

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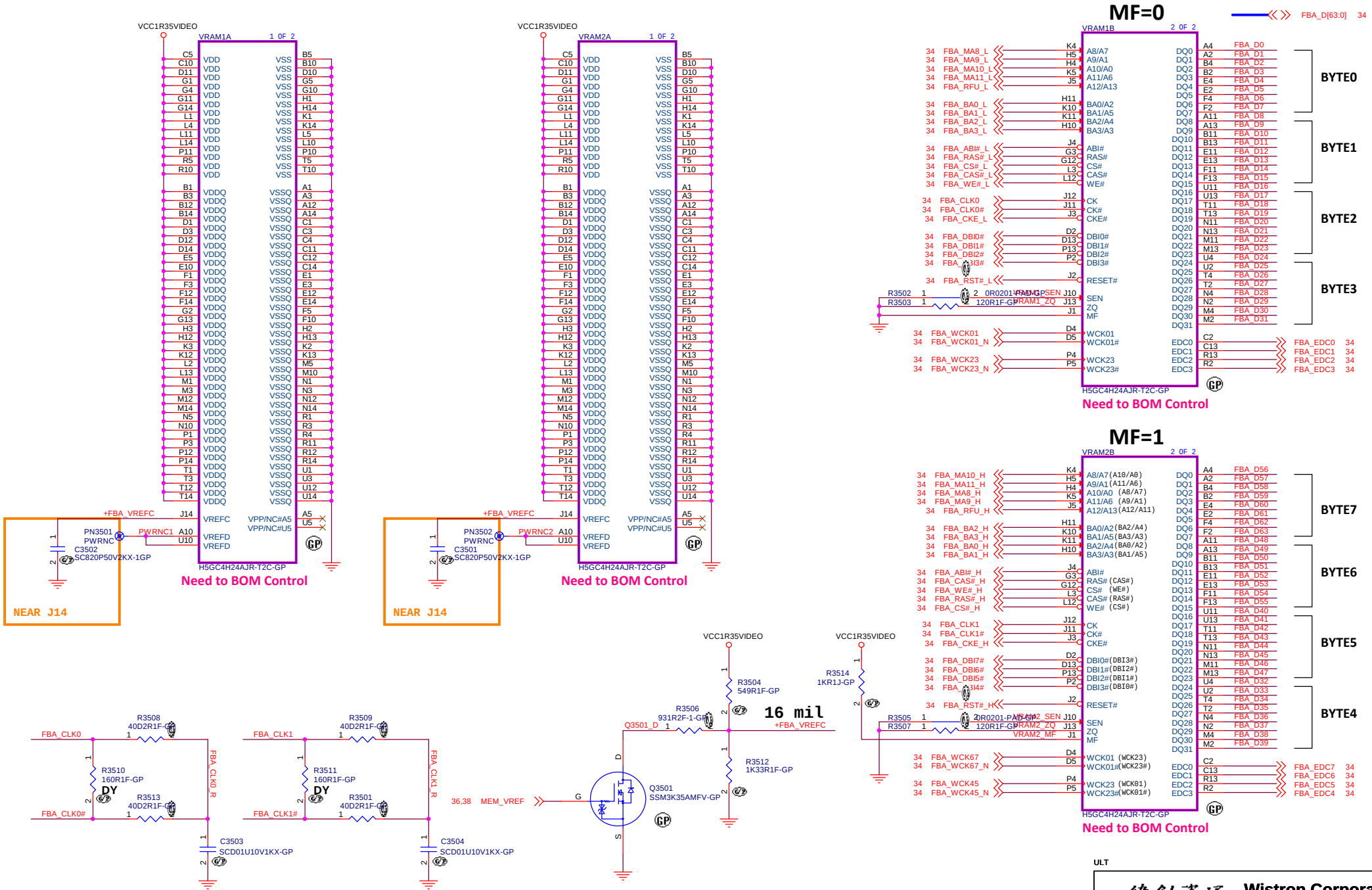
Taipei Hsien 221, Taiwan, R.O.C.

Title	***N18P-Q3 FB A/B***	
Size: A2	Document Number: PADME	Rev: 1
Date: Monday, October 01, 2018	Sheet 34 of 110	



ULT

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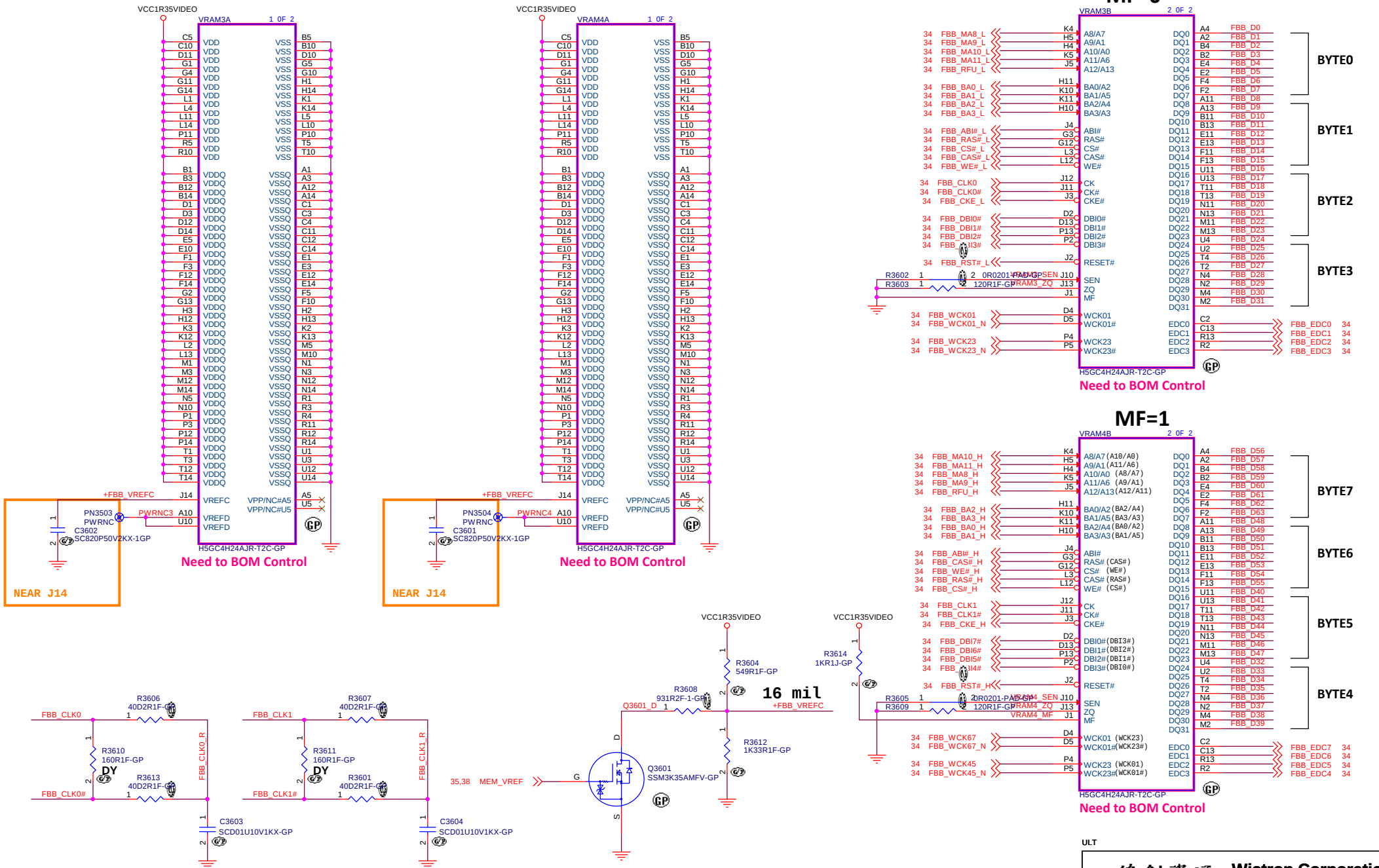
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***N18P-Q3 VRAM CH-A***

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 35 of 110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FBB_D[63:0] 34
VCC1R35VIDEO
VRAM3A 1 0F 2
VRAM4A 1 0F 2
VRAM3B 2 0F 2
VRAM4B 2 0F 2
H5GC4H24AJR-T2C-GP
Need to BOM Control
NEAR J14
+FBB_VREFC
PN3503 PWRNC
PN3504 PWRNC4
C3602 SC820P50V2KX-1GP
C3601 SC820P50V2KX-1GP
PWRNC3
PWRNC4
BYTE0
BYTE1
BYTE2
BYTE3
BYTE4
BYTE5
BYTE6
BYTE7
R3602 120R1F-GP
R3603 120R1F-GP
R3605 120R1F-GP
R3609 120R1F-GP
VRAM3_SEN
VRAM3_ZQ
VRAM4_SEN
VRAM4_ZQ
VRAM4_MF
R3606 40D2R1F-GP
R3607 40D2R1F-GP
R3610 160R1F-GP DY
R3611 160R1F-GP DY
R3613 40D2R1F-GP
R3601 40D2R1F-GP
FBB_CLK0
FBB_CLK0#
FBB_CLK1
FBB_CLK1#
FBB_CLK0_R
FBB_CLK1_R
C3603 SCD01U10V1KX-GP
C3604 SCD01U10V1KX-GP
R3604 549R1F-GP
R3608 931R2F-1-GP
R3612 1K33R1F-GP
R3614 1KR1J-GP
16 mil
+FBB_VREFC
Q3601_D
Q3601 SSM3K35AMFV-GP
35,38 MEM_VREF
ULT
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Title
N18P-Q3 VRAM CH-B
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Title: ***N18P-Q3 VRAM DECOUPING***

Size	Document Number	Rev
A2	PADME	1

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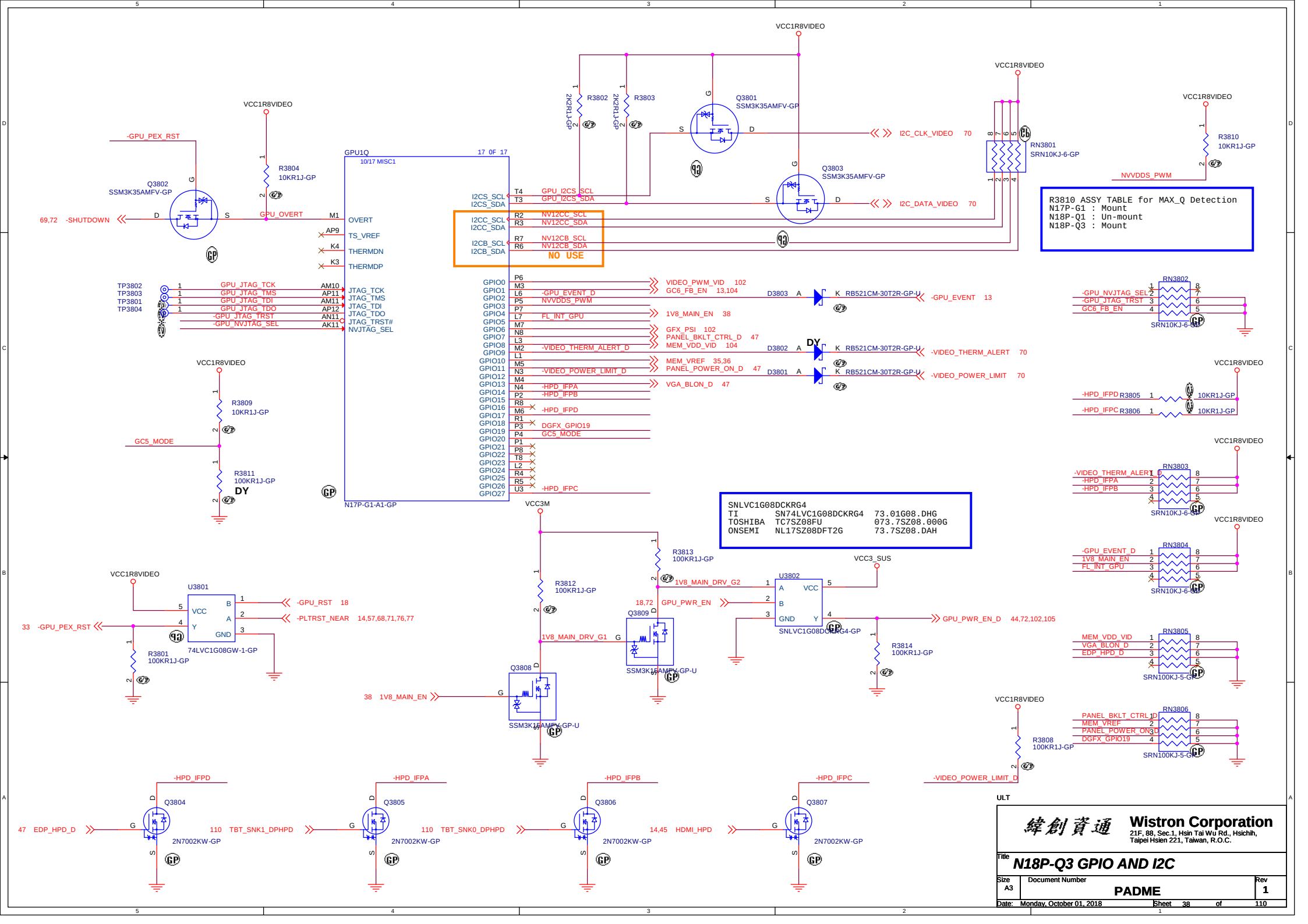
VCC1R8VIDEO
-GPU_PEX_RST
R3804 10KR1J-GP
Q3802 SSM3K35AMFV-GP
69,72 -SHUTDOWN
GPU_OVERT
GPU1Q
10/17 MISC1
17 OF 17
OVERT
TS_VREF
THERMDN
THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
NVJTAG_SEL
TP3802
TP3803
TP3801
TP3804
GPU_JTAG_TCK
GPU_JTAG_TMS
GPU_JTAG_TDI
GPU_JTAG_TDO
-GPU_JTAG_TRST
-GPU_NVJTAG_SEL
R3802 2K2R1J-GP
R3803 2K2R1J-GP
Q3801 SSM3K35AMFV-GP
Q3803 SSM3K35AMFV-GP
I2C_CLK_VIDEO 70
I2C_DATA_VIDEO 70
RN3801 SRN10KJ-6-GP
R3810 10KR1J-GP
NVVDDS_PWM
I2CS_SCL
I2CS_SDA
GPU_I2CS_SCL
GPU_I2CS_SDA
I2CC_SCL
I2CC_SDA
NV12CC_SCL
NV12CC_SDA
I2CB_SCL
I2CB_SDA
NV12CB_SCL
NV12CB_SDA
NO USE
R3810 ASSY TABLE for MAX_Q Detection
N17P-G1 : Mount
N18P-Q1 : Un-mount
N18P-Q3 : Mount
GPIO0 VIDEO_PWM_VID 102
GPIO1 -GPU_EVENT_D
GC6_FB_EN 13,104
GPIO2 NVVDDS_PWM
GPIO3
GPIO4 FL_INT_GPU
1V8_MAIN_EN 38
GPIO5
GPIO6 GFX_PSI 102
GPIO7 PANEL_BKLT_CTRL_D 47
GPIO8 MEM_VDD_VID 104
GPIO9
GPIO10 MEM_VREF 35,36
GPIO11 PANEL_POWER_ON_D 47
GPIO12
GPIO13 VGA_BLON_D 47
GPIO14 -HPD_IFPA
GPIO15 -HPD_IFPB
GPIO16
GPIO17 -HPD_IFPD
GPIO18
GPIO19 DGFX_GPIO19
GPIO20 GC5_MODE
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO26
GPIO27 -HPD_IFPC
N17P-G1-A1-GP
D3803 RB521CM-30T2R-GP-U
-GPU_EVENT 13
D3802 RB521CM-30T2R-GP-U
-VIDEO_THERM_ALERT 70
D3801 RB521CM-30T2R-GP-U
-VIDEO_POWER_LIMIT 70
DY
RN3802 SRN10KJ-6-GP
-GPU_NVJTAG_SEL
-GPU_JTAG_TRST
GC6_FB_EN
R3805 10KR1J-GP
R3806 10KR1J-GP
-HPD_IFPD
-HPD_IFPC
RN3803 SRN10KJ-6-GP
-VIDEO_THERM_ALERT
-HPD_IFPA
-HPD_IFPB
RN3804 SRN10KJ-6-GP
-GPU_EVENT_D
1V8_MAIN_EN
FL_INT_GPU
RN3805 SRN100KJ-5-GP
MEM_VDD_VID
VGA_BLON_D
EDP_HPD_D
RN3806 SRN100KJ-5-GP
PANEL_BKLT_CTRL_D
MEM_VREF
PANEL_POWER_ON_D
DGFX_GPIO19
R3809 10KR1J-GP
R3811 100KR1J-GP
GC5_MODE
SNLVC1G08DCKRG4
TI SN74LVC1G08DCKRG4 73.01G08.DHG
TOSHIBA TC7SZ08FU 073.7SZ08.000G
ONSEMI NL17SZ08DFT2G 73.7SZ08.DAH
VCC3M
VCC3_SUS
R3813 100KR1J-GP
R3812 100KR1J-GP
1V8_MAIN_DRV_G2
1V8_MAIN_DRV_G1
18,72 GPU_PWR_EN
GPU_PWR_EN_D 44,72,102,105
U3802 SNLVC1G08DCKRG4-GP
Q3809 SSM3K15AMFV-GP-U
R3814 100KR1J-GP
Q3808 SSM3K15AMFV-GP-U
38 1V8_MAIN_EN
U3801 74LVC1G08GW-1-GP
33 -GPU_PEX_RST
-GPU_RST 18
-PLTRST_NEAR 14,57,68,71,76,77
R3801 100KR1J-GP
R3808 100KR1J-GP
-VIDEO_POWER_LIMIT_D
Q3804 2N7002KW-GP
Q3805 2N7002KW-GP
Q3806 2N7002KW-GP
Q3807 2N7002KW-GP
47 EDP_HPD_D
110 TBT_SNK1_DPHPD
110 TBT_SNK0_DPHPD
14,45 HDMI_HPD
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Title
N18P-Q3 GPIO AND I2C
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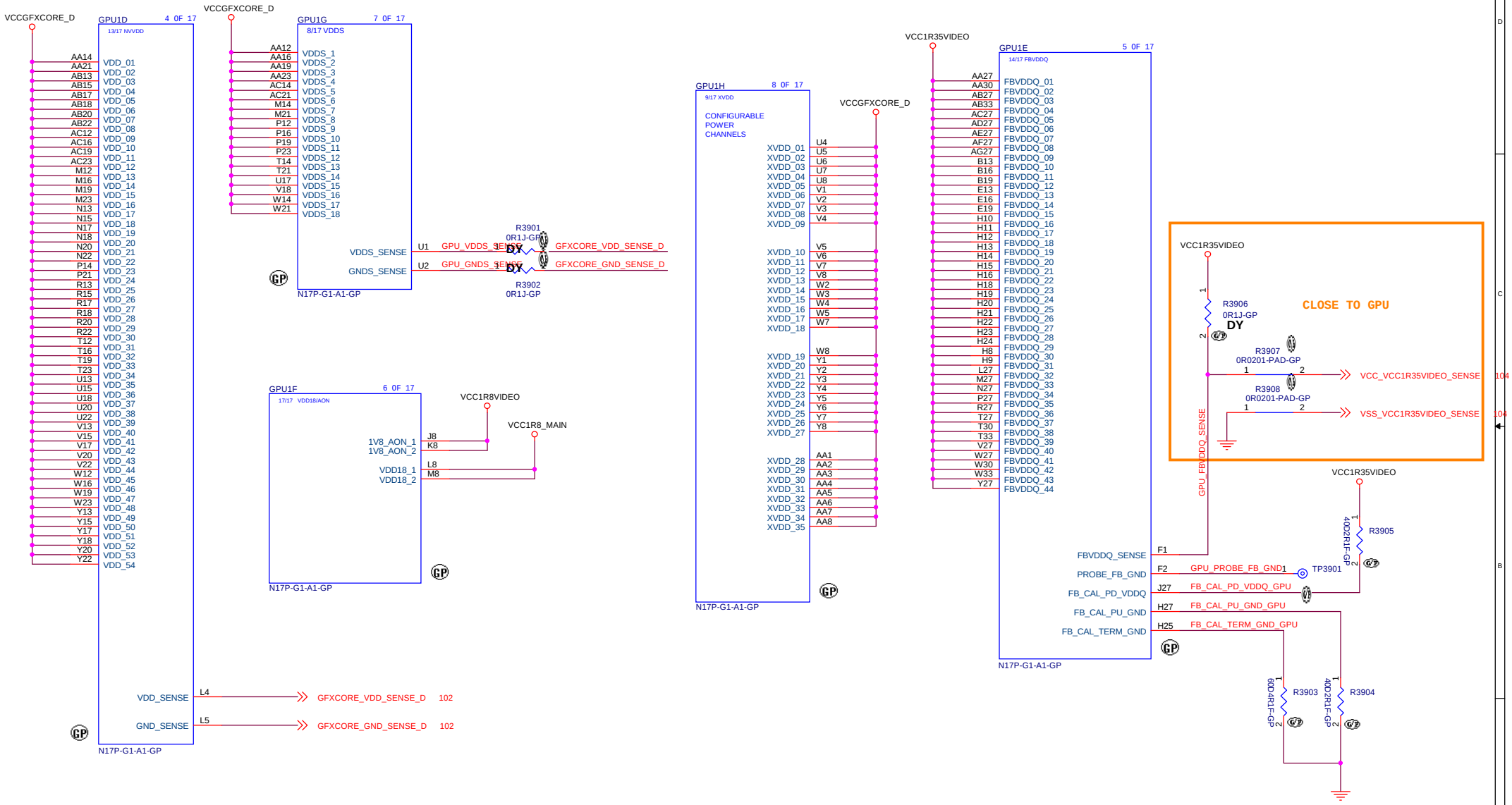

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Title	***N18P-Q3 POWER***	
Size: A3	Document Number: **PADME**	Rev: 1
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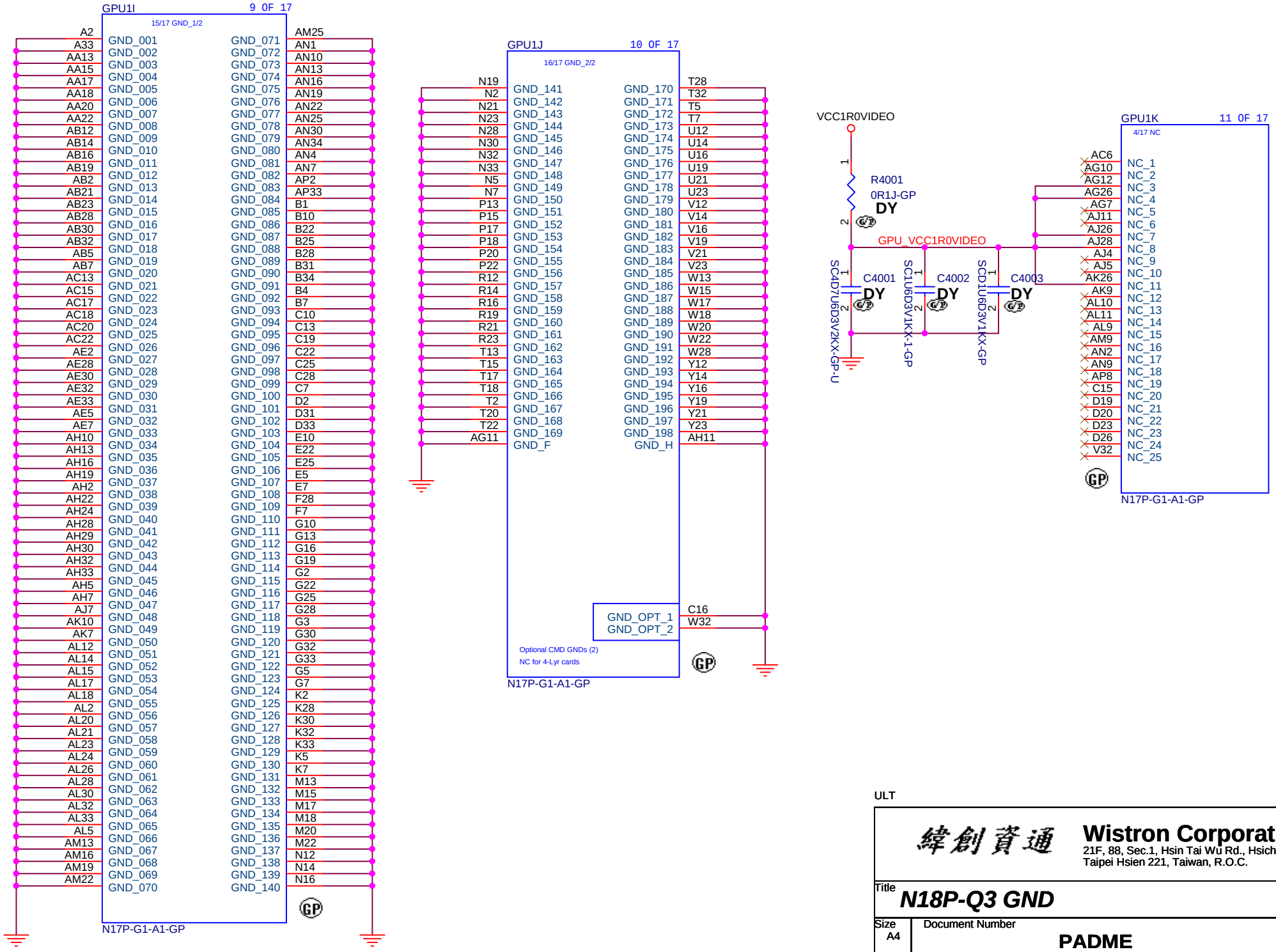

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Title	***N18P-Q3 GND***	
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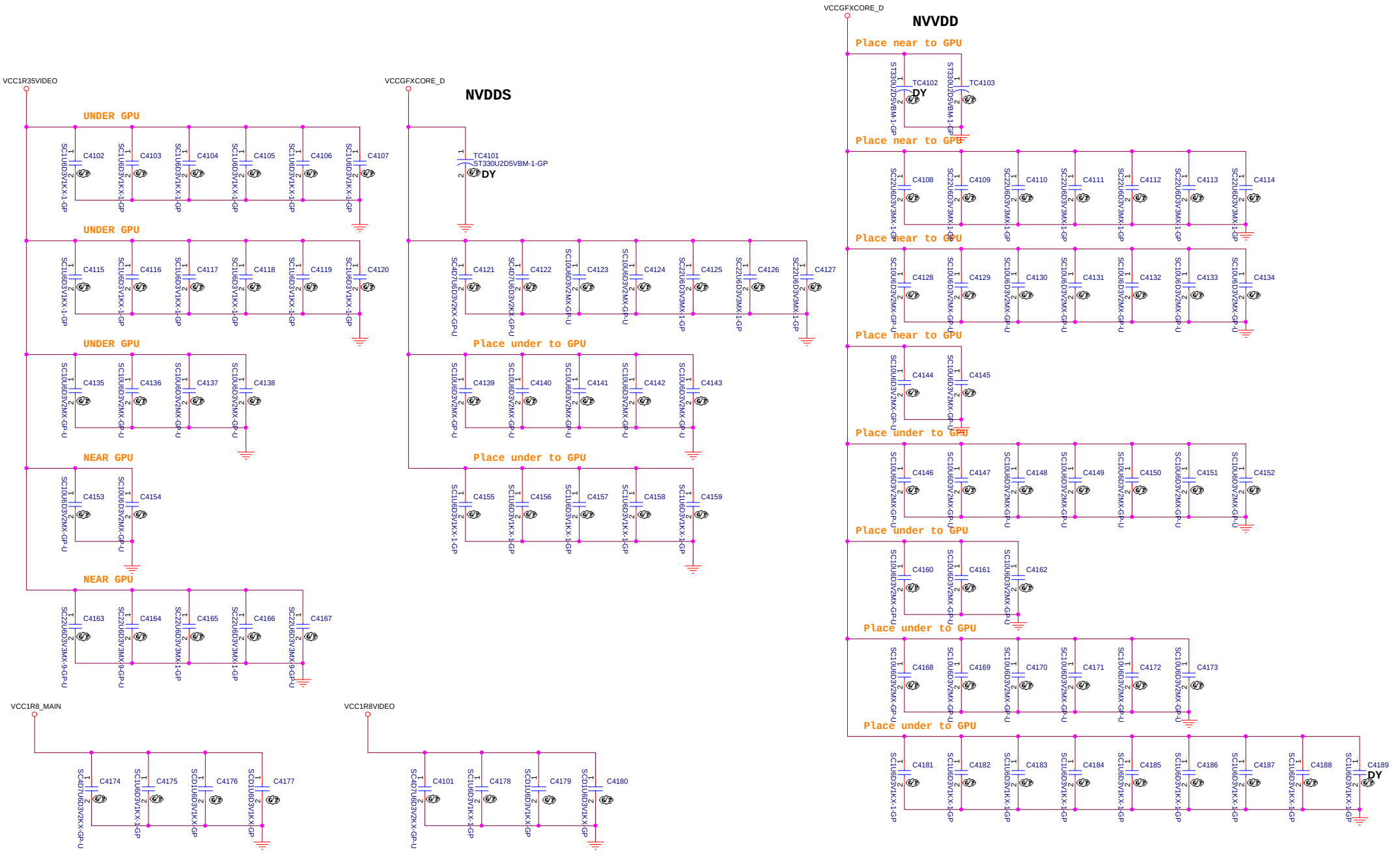

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Title: ***N18P-Q3 DECOUPING***

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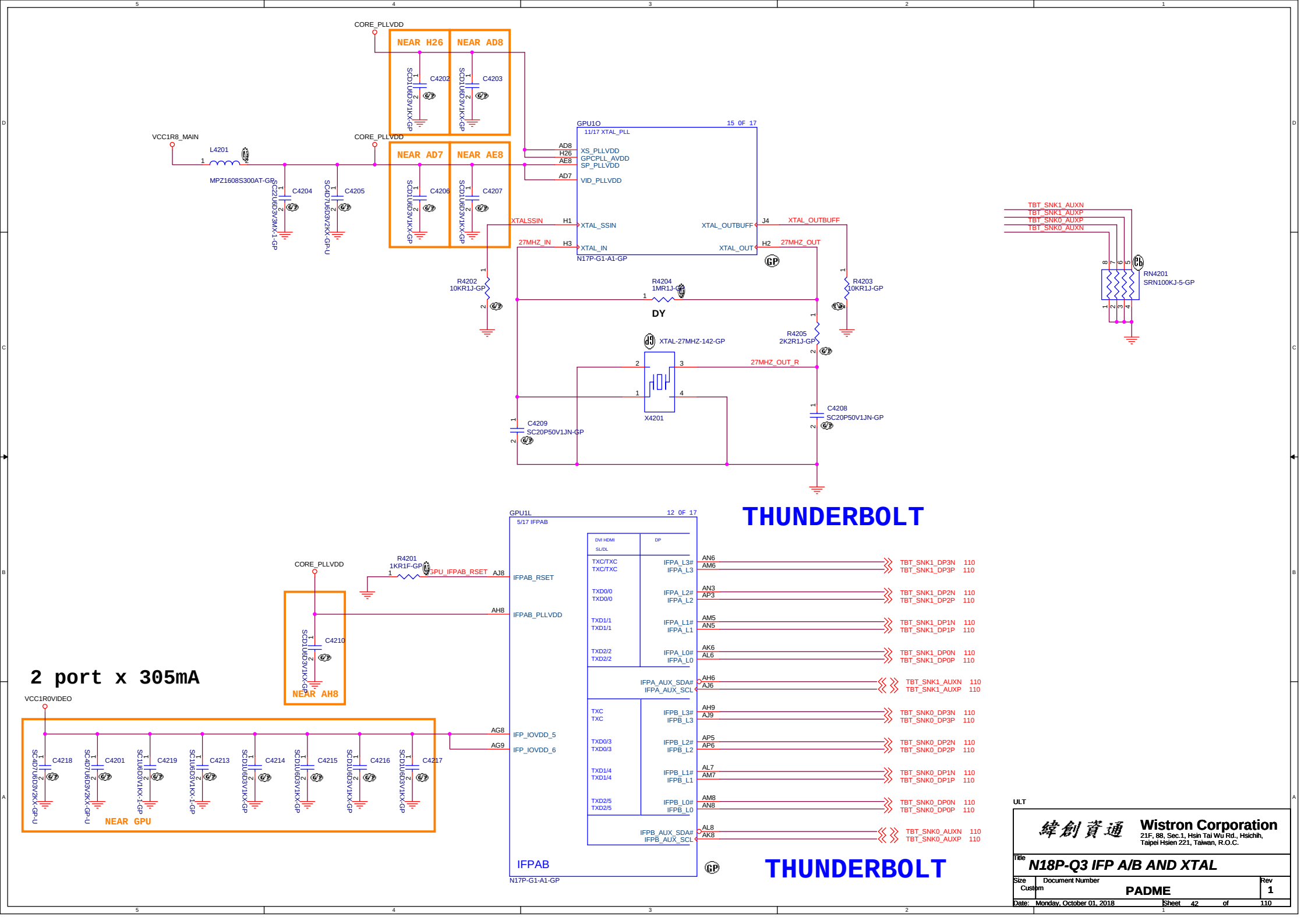

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Size	Document Number	Rev
Custom	PADME	1

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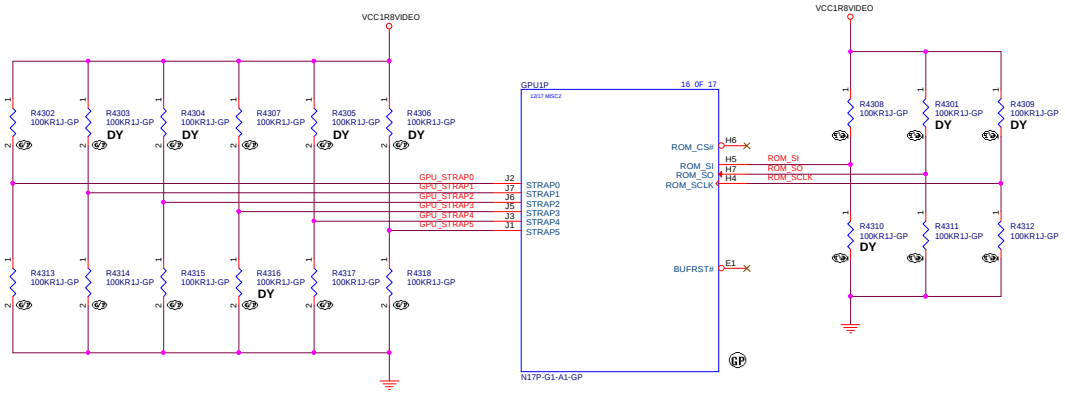

Strap0 table for VRAM vendor		
Vendor	R4302	R4313
Samsung 8S@	NO ASM	100K 1%
Micron 8M@	100K 1%	NO ASM
Micron B-die	NO ASM	100K 1%

Strap1 table for VRAM vendor		
Vendor	R4303	R4314
Samsung 8S@	NO ASM	100K 1%
Micron 8M@	NO ASM	100K 1%
Micron B-die	NO ASM	100K 1%

Strap2 table for VRAM vendor		
Vendor	R4304	R4315
Samsung 8S@	NO ASM	100K 1%
Micron 8M@	NO ASM	100K 1%
Micron B-die	100K 1%	NO ASM

Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
H	M	L	17 (0x0011)
H	M	H	18 (0x0012)
H	H	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Table 5.4 Display Link to SORx_EXPOSED Mapping for Down Designs

Total Display Links (HDMI, DP or DVI)	Total Enabled for Audio (HDMI, DP or DVI)	Is IFPD used? (Only supports eDP.)	See This Row of Table 5.5
4	4	NO	15
4	3	YES	13
3	3	NO	14
3	2	YES	12
2	2	NO	12
2	1	YES	8
1	1	NO	8
1	0	YES	0
No other configurations are supported.			

Table 5.5 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

5.2.2.3 Assorted Configuration Straps

The following configurable characteristics of the graphics circuit share three physical strap pins:

- **SMB_ALT_ADDR Enable**: This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBUS port. The "SMB_ALT_ADDR disabled" setting ('0') is correct for single-GPU graphics circuits. (see Section 13.3.2.1 for the SMBus address.)
- **DEVID_SEL**: NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID defined for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- **PCIE_CFG**: This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing. N17x graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- **VGA_DEVICE**: This strap function is used to report the graphics circuit either as a 3D device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The 3D Device (class code 302, strap='0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits.

Table 5.6 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0

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Title: N18P-Q3 MIO AND ROM

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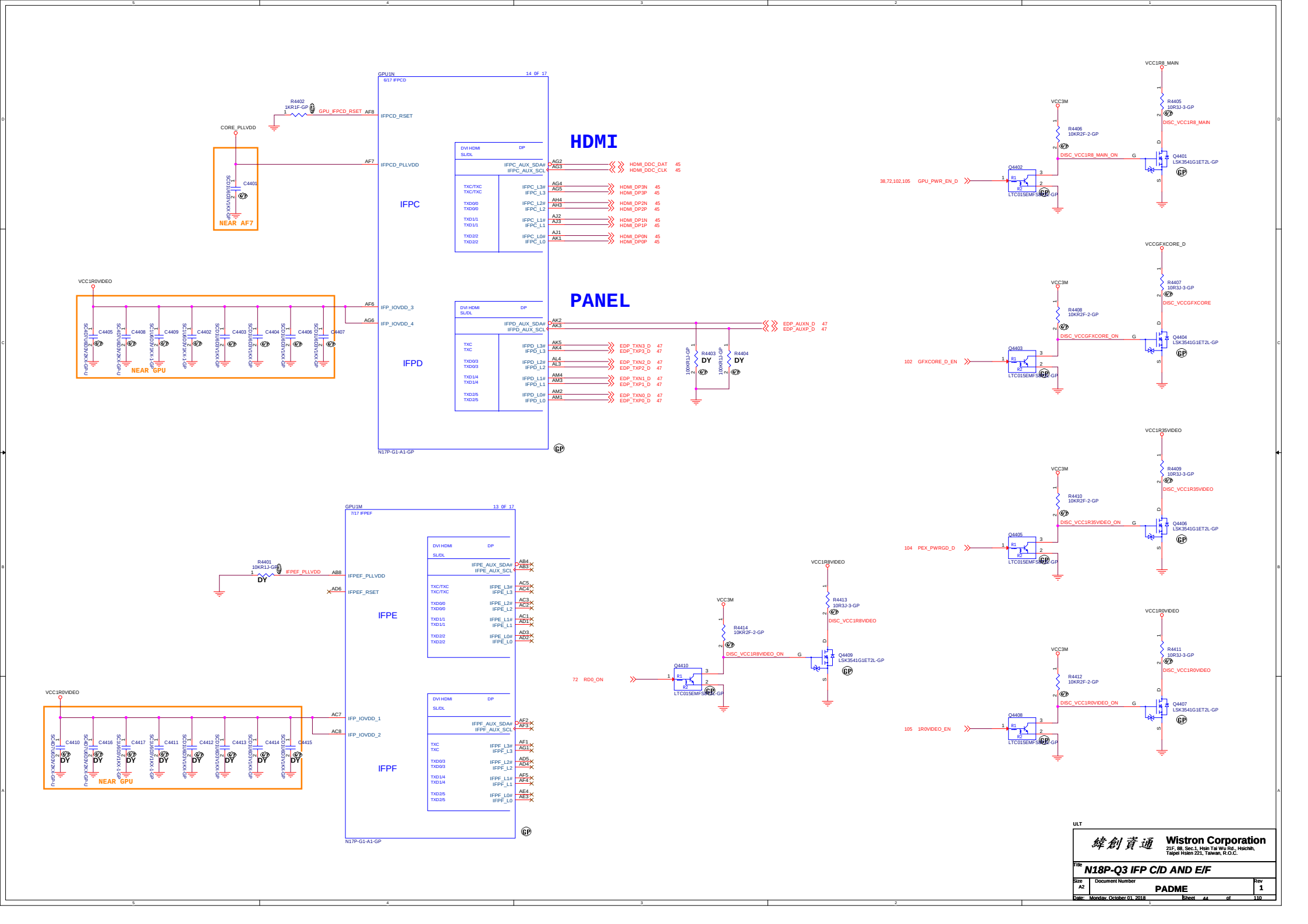

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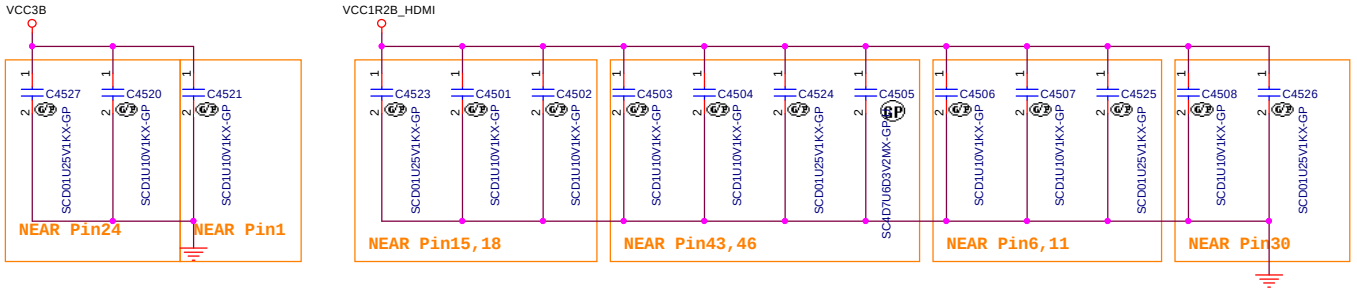
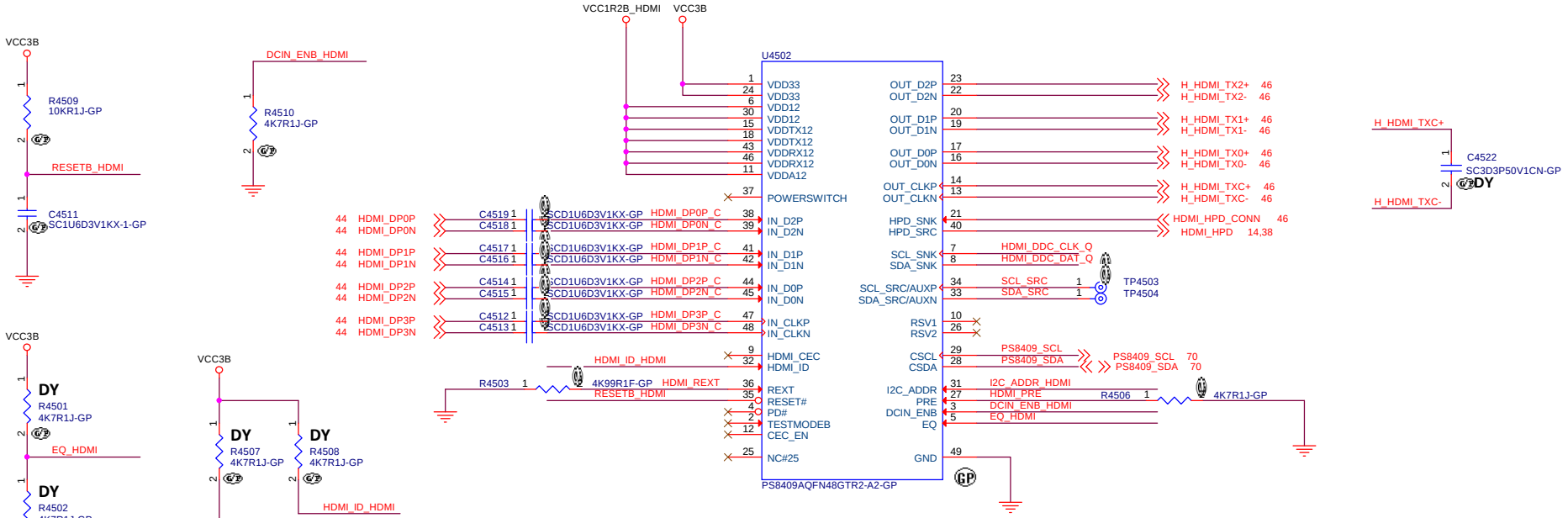
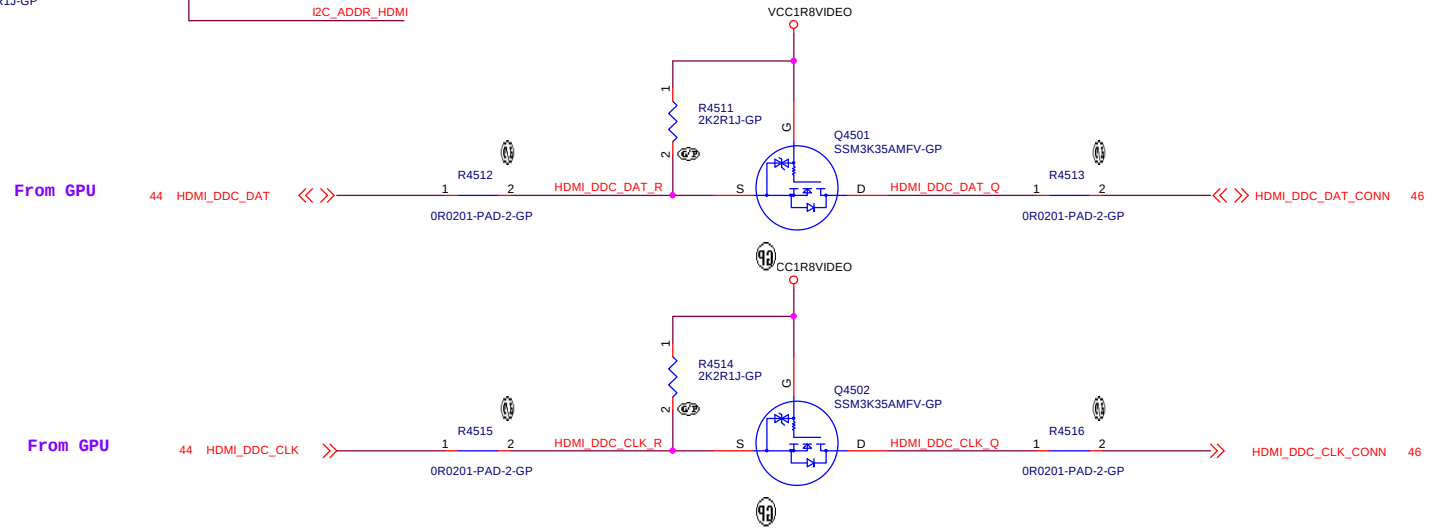
HDMI Re driver







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Title: HDMI RE-DRIVER

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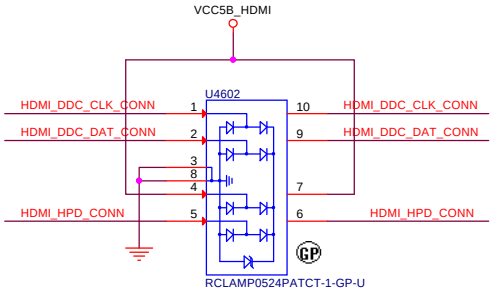
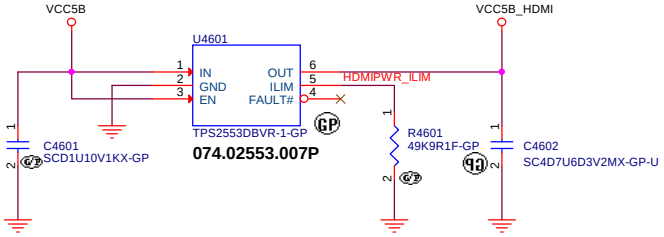
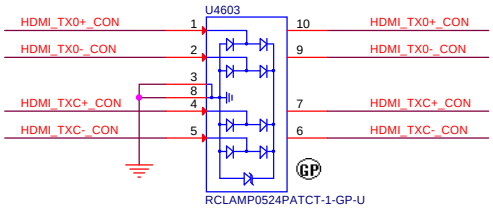
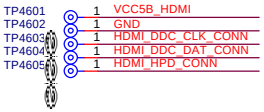
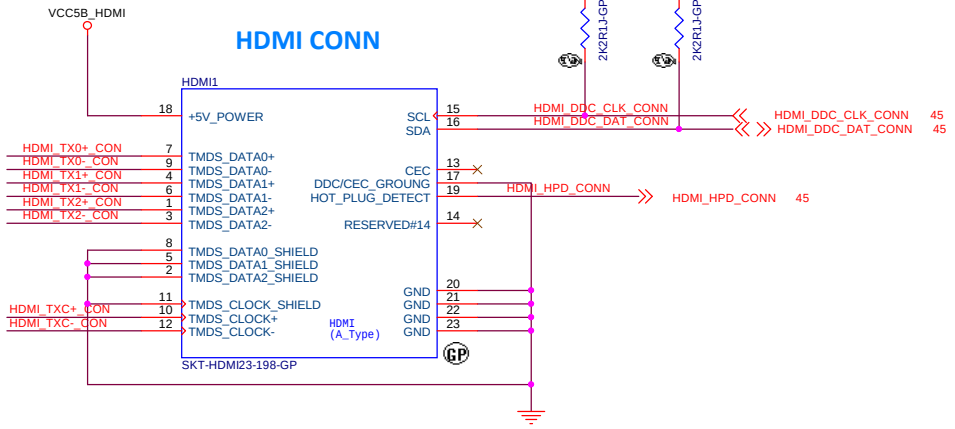
HDMI

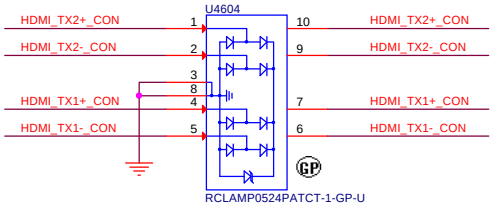


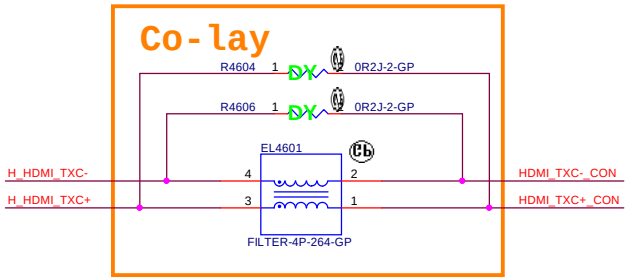


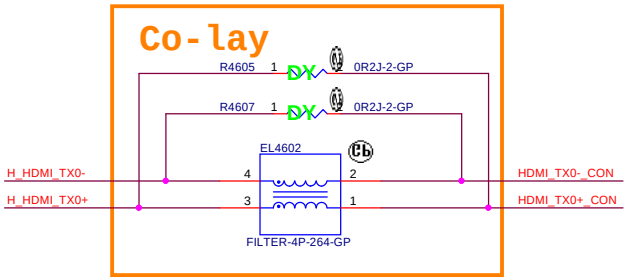


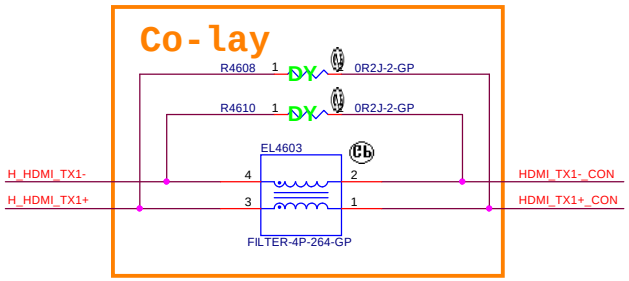


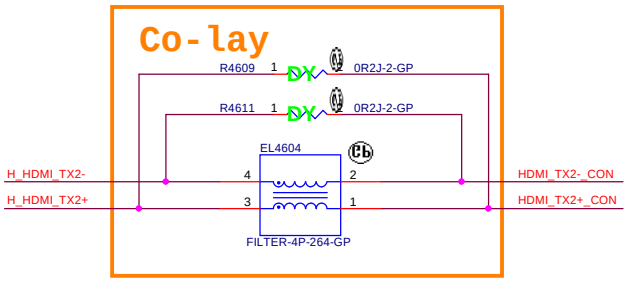


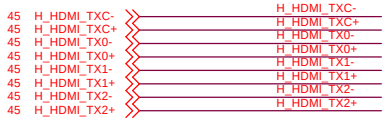












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Title: ***HDMI CONNECTOR***

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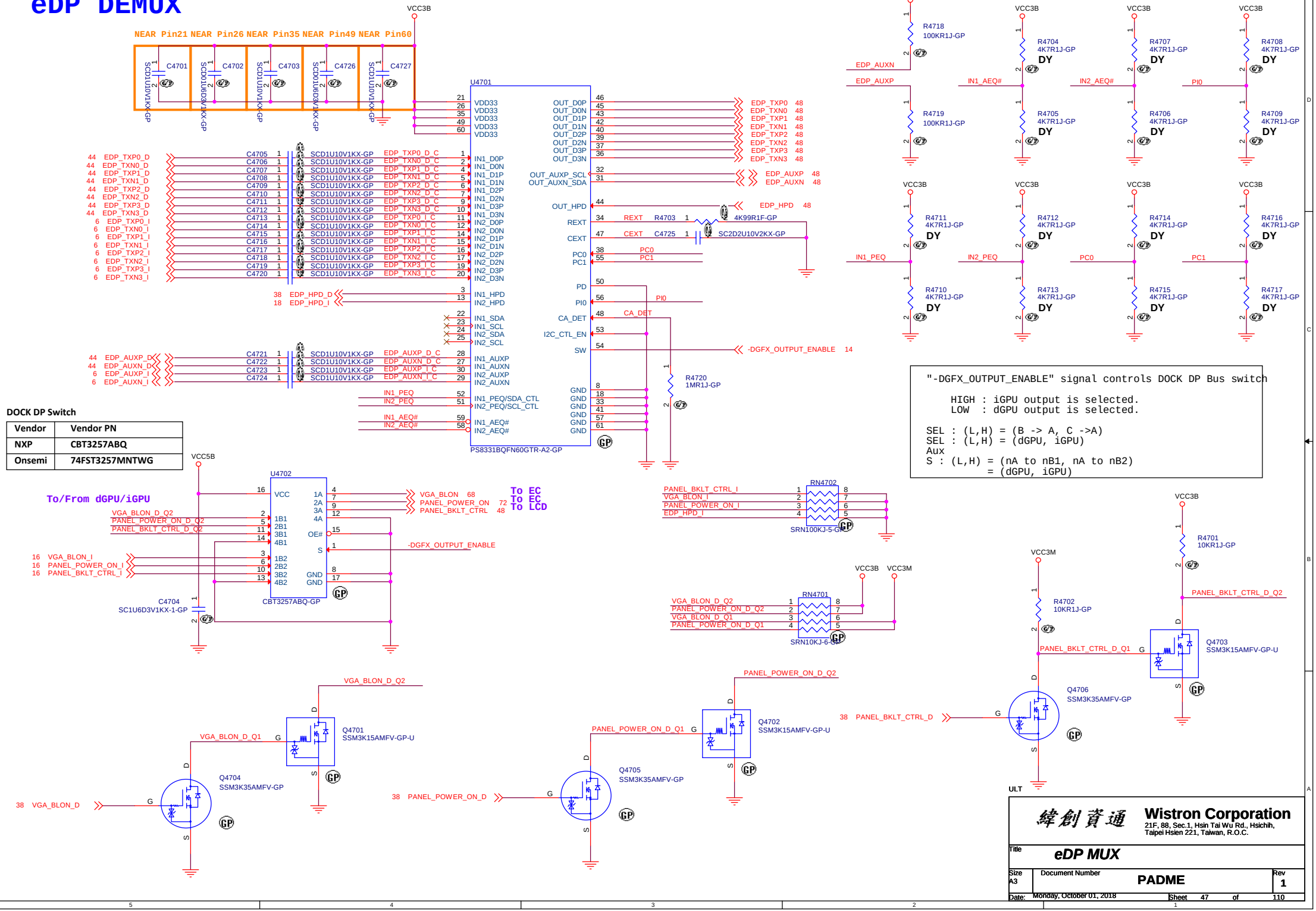
eDP DEMUX



DOCK DP Switch

Vendor	Vendor PN
NXP	CBT3257ABQ
Onsemi	74FST3257MNTWG

"-DGFX_OUTPUT_ENABLE" signal controls DOCK DP Bus switch

HIGH : iGPU output is selected.
LOW : dGPU output is selected.

SEL : (L,H) = (B -> A, C ->A)
SEL : (L,H) = (dGPU, iGPU)
Aux
S : (L,H) = (nA to nB1, nA to nB2)
= (dGPU, iGPU)

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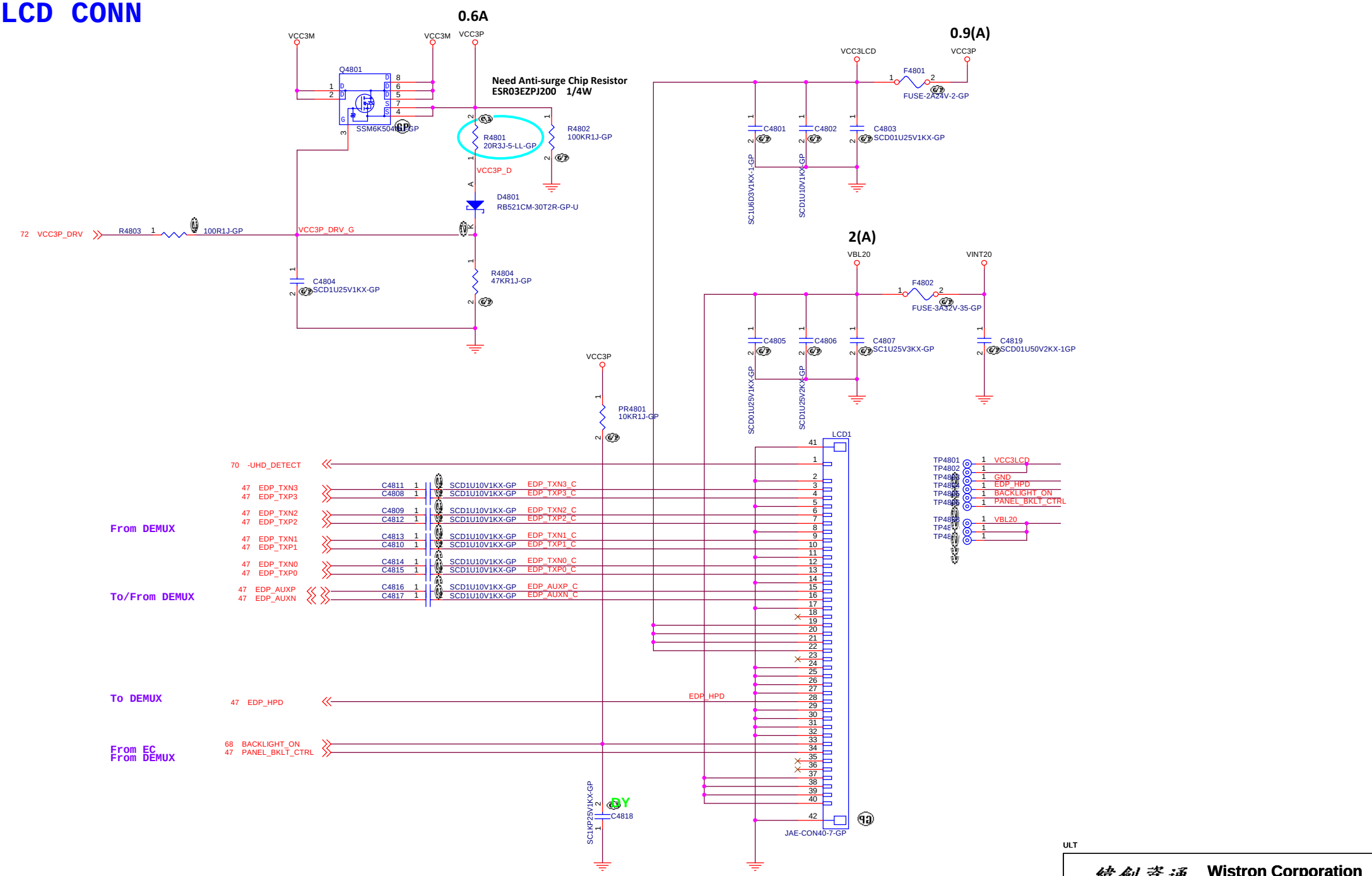
LCD CONN



need 2~3 empty pins between signals or other power net.

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Title: LCD CONNECTOR

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A3	PADME	1

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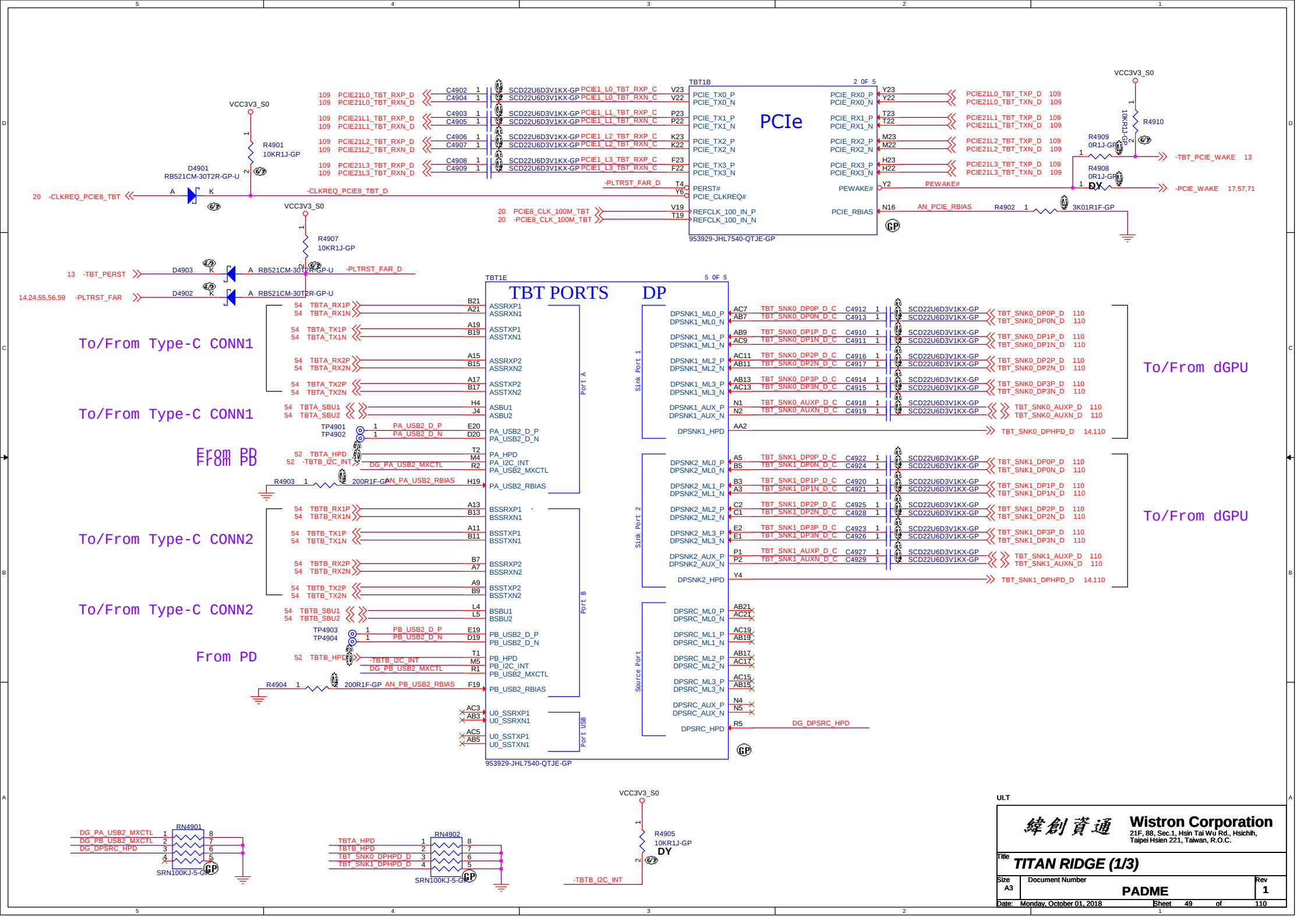
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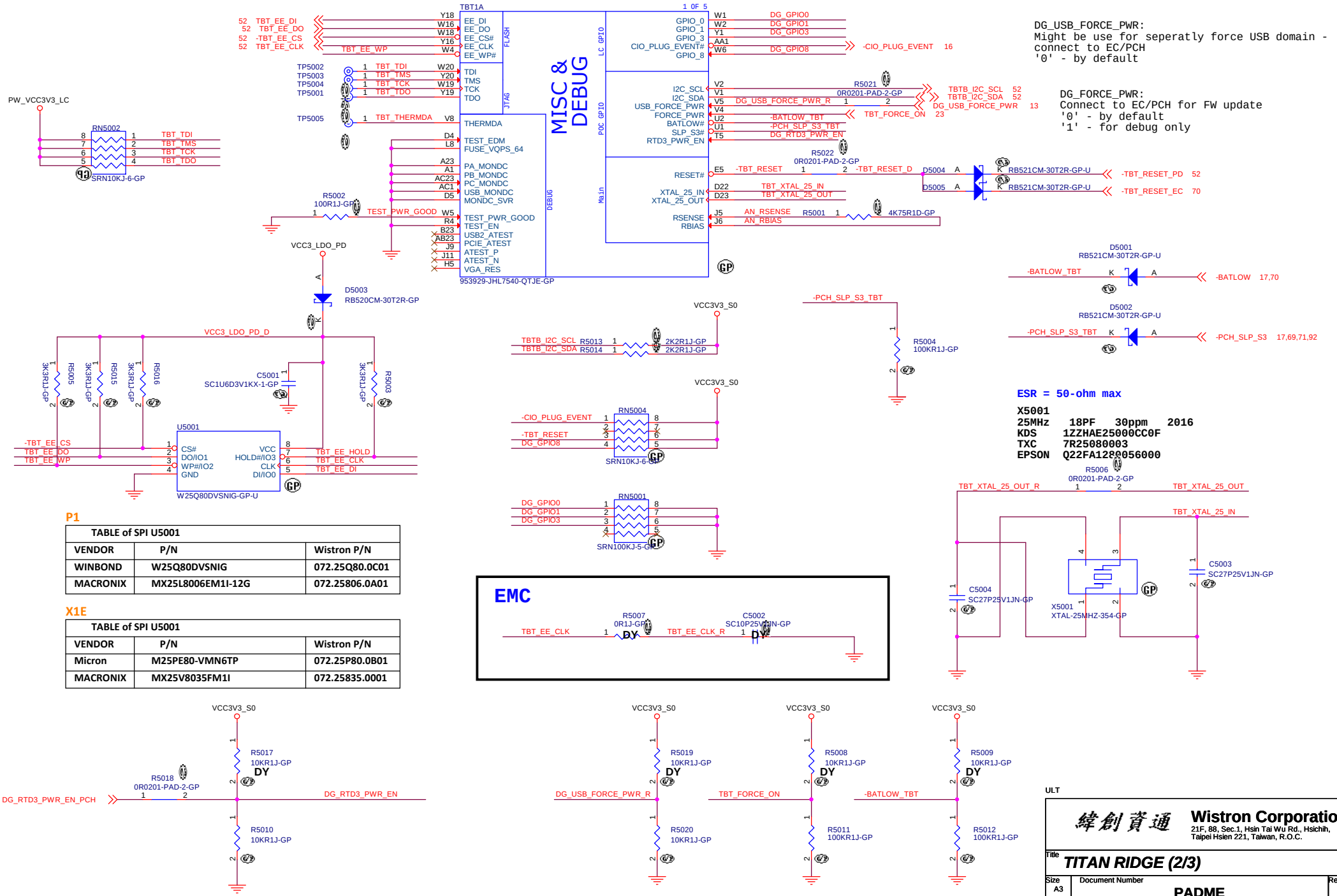
PCIe
2 OF 5
953929-JHL7540-QTJE-GP
TBT1E
TBT PORTS
DP
5 OF 5
953929-JHL7540-QTJE-GP
Port A
Port B
Port USB
Sink Port 1
Sink Port 2
Source Port
To/From Type-C CONN1
To/From Type-C CONN1
From PD
To/From Type-C CONN2
To/From Type-C CONN2
From PD
To/From dGPU
To/From dGPU
PCIE_TX0_P
PCIE_TX0_N
PCIE_TX1_P
PCIE_TX1_N
PCIE_TX2_P
PCIE_TX2_N
PCIE_TX3_P
PCIE_TX3_N
PERST#
PCIE_CLKREQ#
REFCLK_100_IN_P
REFCLK_100_IN_N
PCIE_RX0_P
PCIE_RX0_N
PCIE_RX1_P
PCIE_RX1_N
PCIE_RX2_P
PCIE_RX2_N
PCIE_RX3_P
PCIE_RX3_N
PEWAKE#
PCIE_RBIAS
ASSRXP1
ASSRXN1
ASSTXP1
ASSTXN1
ASSRXP2
ASSRXN2
ASSTXP2
ASSTXN2
ASBU1
ASBU2
PA_USB2_D_P
PA_USB2_D_N
PA_HPD
PA_I2C_INT
PA_USB2_MXCTL
PA_USB2_RBIAS
BSSRXP1
BSSRXN1
BSSTXP1
BSSTXN1
BSSRXP2
BSSRXN2
BSSTXP2
BSSTXN2
BSBU1
BSBU2
PB_USB2_D_P
PB_USB2_D_N
PB_HPD
PB_I2C_INT
PB_USB2_MXCTL
PB_USB2_RBIAS
U0_SSRXP1
U0_SSRXN1
U0_SSTXP1
U0_SSTXN1
DPSNK1_ML0_P
DPSNK1_ML0_N
DPSNK1_ML1_P
DPSNK1_ML1_N
DPSNK1_ML2_P
DPSNK1_ML2_N
DPSNK1_ML3_P
DPSNK1_ML3_N
DPSNK1_AUX_P
DPSNK1_AUX_N
DPSNK1_HPD
DPSNK2_ML0_P
DPSNK2_ML0_N
DPSNK2_ML1_P
DPSNK2_ML1_N
DPSNK2_ML2_P
DPSNK2_ML2_N
DPSNK2_ML3_P
DPSNK2_ML3_N
DPSNK2_AUX_P
DPSNK2_AUX_N
DPSNK2_HPD
DPSRC_ML0_P
DPSRC_ML0_N
DPSRC_ML1_P
DPSRC_ML1_N
DPSRC_ML2_P
DPSRC_ML2_N
DPSRC_ML3_P
DPSRC_ML3_N
DPSRC_AUX_P
DPSRC_AUX_N
DPSRC_HPD
DG_DPSRC_HPD
TBT_SNK0_DPHPD_D
TBT_SNK1_DPHPD_D
VCC3V3_S0
D4901
RB521CM-30T2R-GP-U
D4903
D4902
R4901
10KR1J-GP
R4907
10KR1J-GP
R4910
10KR1J-GP
R4909
0R1J-GP
R4908
0R1J-GP
DY
R4902
3K01R1F-GP
R4903
R4904
200R1F-GP
TP4901
TP4902
TP4903
TP4904
RN4901
SRN100KJ-5-GP
RN4902
SRN100KJ-5-GP
R4905
10KR1J-GP
DY
-CLKREQ_PCIE8_TBT
-CLKREQ_PCIE8_TBT_D
-PLTRST_FAR_D
-TBT_PERST
-PLTRST_FAR
-TBT_PCIE_WAKE
-PCIE_WAKE
PEWAKE#
AN_PCIE_RBIAS
AN_PA_USB2_RBIAS
AN_PB_USB2_RBIAS
DG_PA_USB2_MXCTL
DG_PB_USB2_MXCTL
-TBTB_I2C_INT
ULT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TITAN RIDGE (1/3)
Size
A3
Document Number
PADME
Rev
1
Date: Monday, October 01, 2018
Sheet 49 of 110



P1

TABLE of SPI U5001		
VENDOR	P/N	Wistron P/N
WINBOND	W25Q80DVSNIG	072.25Q80.0C01
MACRONIX	MX25L8006EM1I-12G	072.25806.0A01

X1E

TABLE of SPI U5001		
VENDOR	P/N	Wistron P/N
Micron	M25PE80-VMN6TP	072.25P80.0B01
MACRONIX	MX25V8035FM1I	072.25835.0001

ULT

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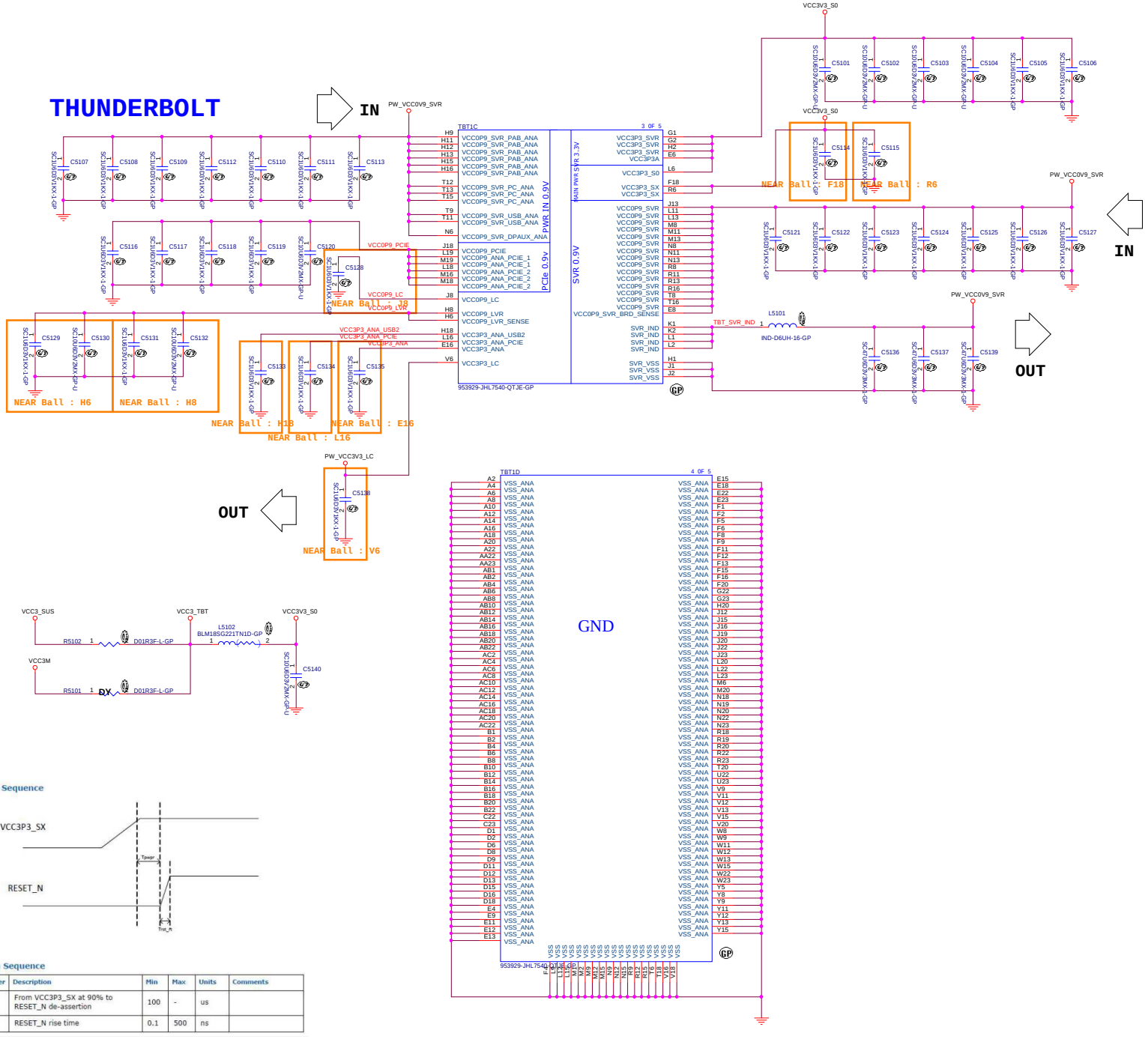
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TITAN RIDGE (2/3)**

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 50 of 110



Power On Sequence

Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

ULT

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Title: **TITAN RIDGE (3/3)**

Size	Document Number	Rev
A2	PADME	1

Date: Monday, October 01, 2018 Sheet 51 of 110

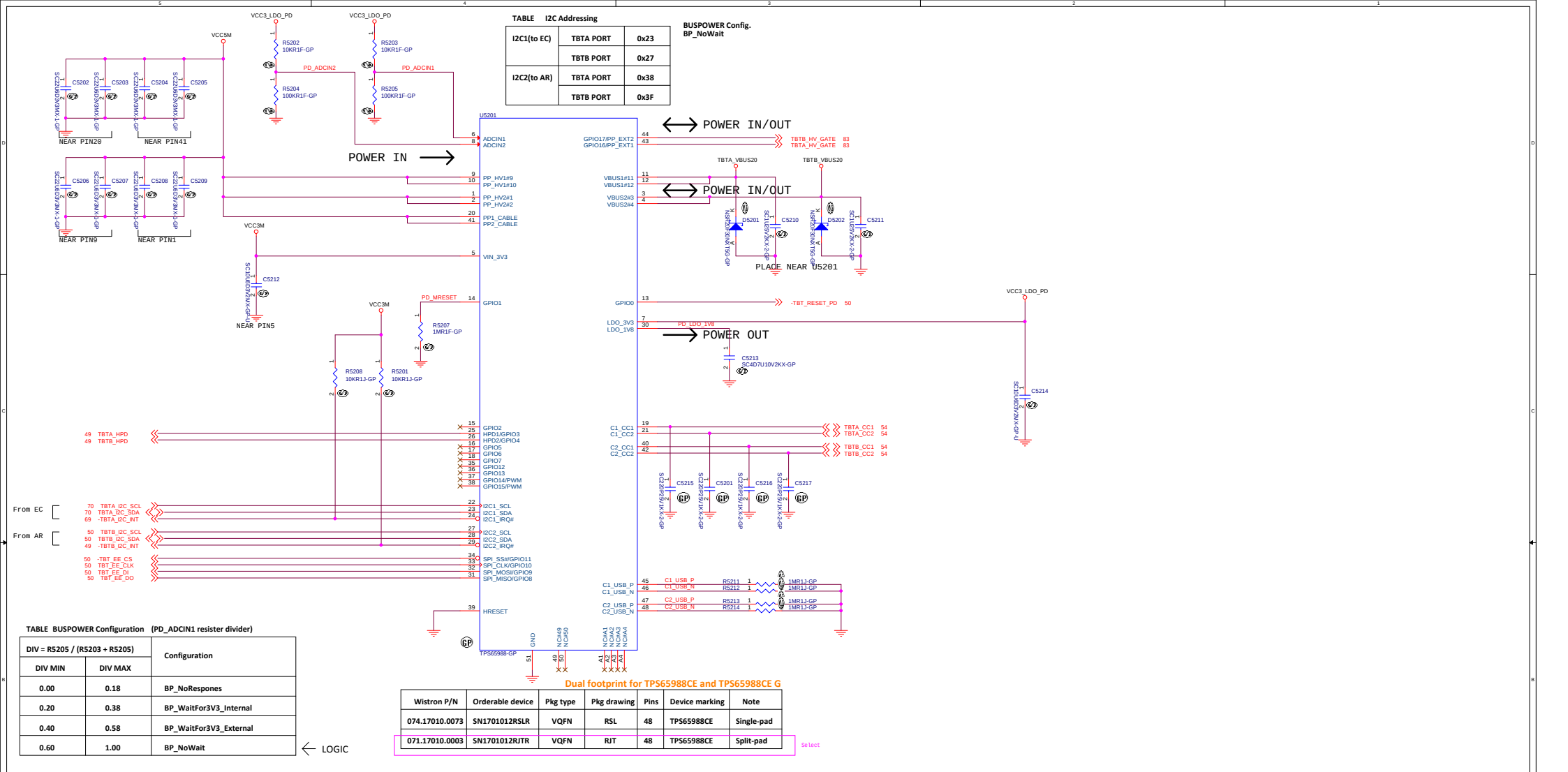

TABLE BUSPOWER Configuration (PD_ADCIN1 resister divider)

DIV = R5205 / (R5203 + R5205)		Configuration
DIV MIN	DIV MAX	
0.00	0.18	BP_NoRespones
0.20	0.38	BP_WaitFor3V3_Internal
0.40	0.58	BP_WaitFor3V3_External
0.60	1.00	BP_NoWait

← LOGIC

Wistron P/N	Orderable device	Pkg type	Pkg drawing	Pins	Device marking	Note
074.17010.0073	SN1701012RSLR	VQFN	RSL	48	TPS65988CE	Single-pad
071.17010.0003	SN1701012RJTR	VQFN	RJT	48	TPS65988CE	Split-pad

Select

ULT

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Taipei Hsien 221, Taiwan, R.O.C.

Title **POWER DELIVERY (1/2)**

Size	Document Number	Rev
A2	PADME	1

Date: Monday, October 01, 2018 Sheet 52 of 110

Reserved

ULT

緯創資通 **Wistron Corporation**
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Title ***Reserved***

Size	Document Number	Rev
A4	**PADME**	1

Date: Monday, October 01, 2018 Sheet 53 of 110

CC PROTECTION

MP version of TPD8S300 075.8S300.0073

ACOK# is not longer monitored on RV3 by EC.

Place on BOTTOM side

Should be placed near Type-C connector

Co-lay

Place near U5403 pin8

Place near U5406 pin8

TS3USB31E is placed for security reason.
When unknown USB Type-C power adapter is attached, utility in OS shuts down USB 2.0 signal from USB Type-C port to avoid computer virus.

TABLE U5403

TI	TS3USB31E	073.00331.0003
ONsemi	NLAS7213MUTBG	073.07213.0003

TABLE U5406

TI	TS3USB31E	073.00331.0003
ONsemi	NLAS7213MUTBG	073.07213.0003

ULT

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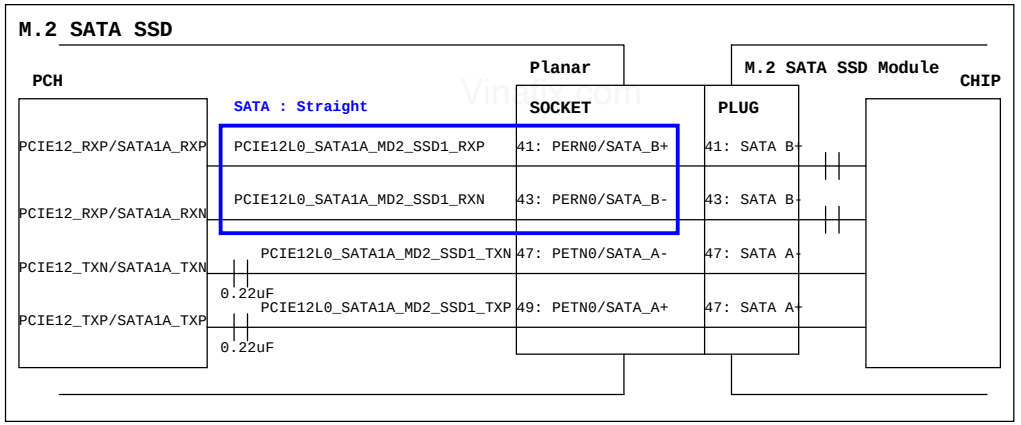
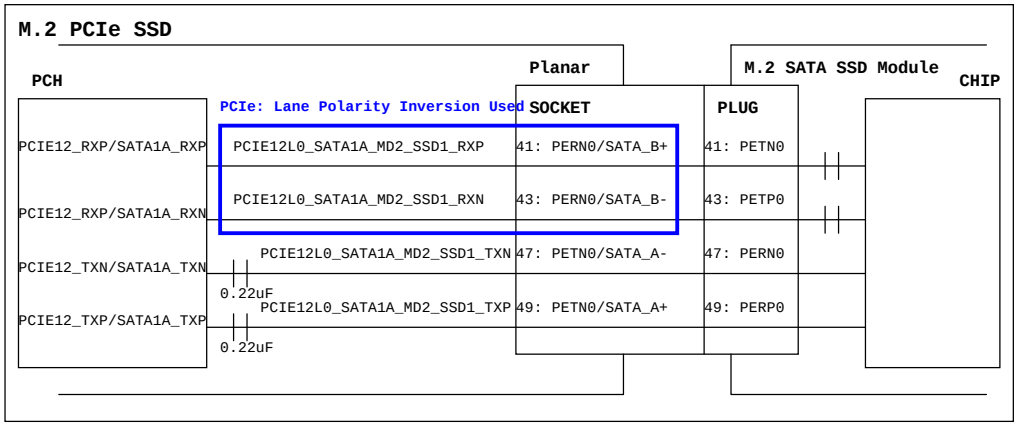
Title: USB TYPE-C CONNECTOR

Size: A2 | Document Number: PADME | Rev: 1

Date: Monday, October 01, 2018 | Sheet 54 of 110

M.2 SSD





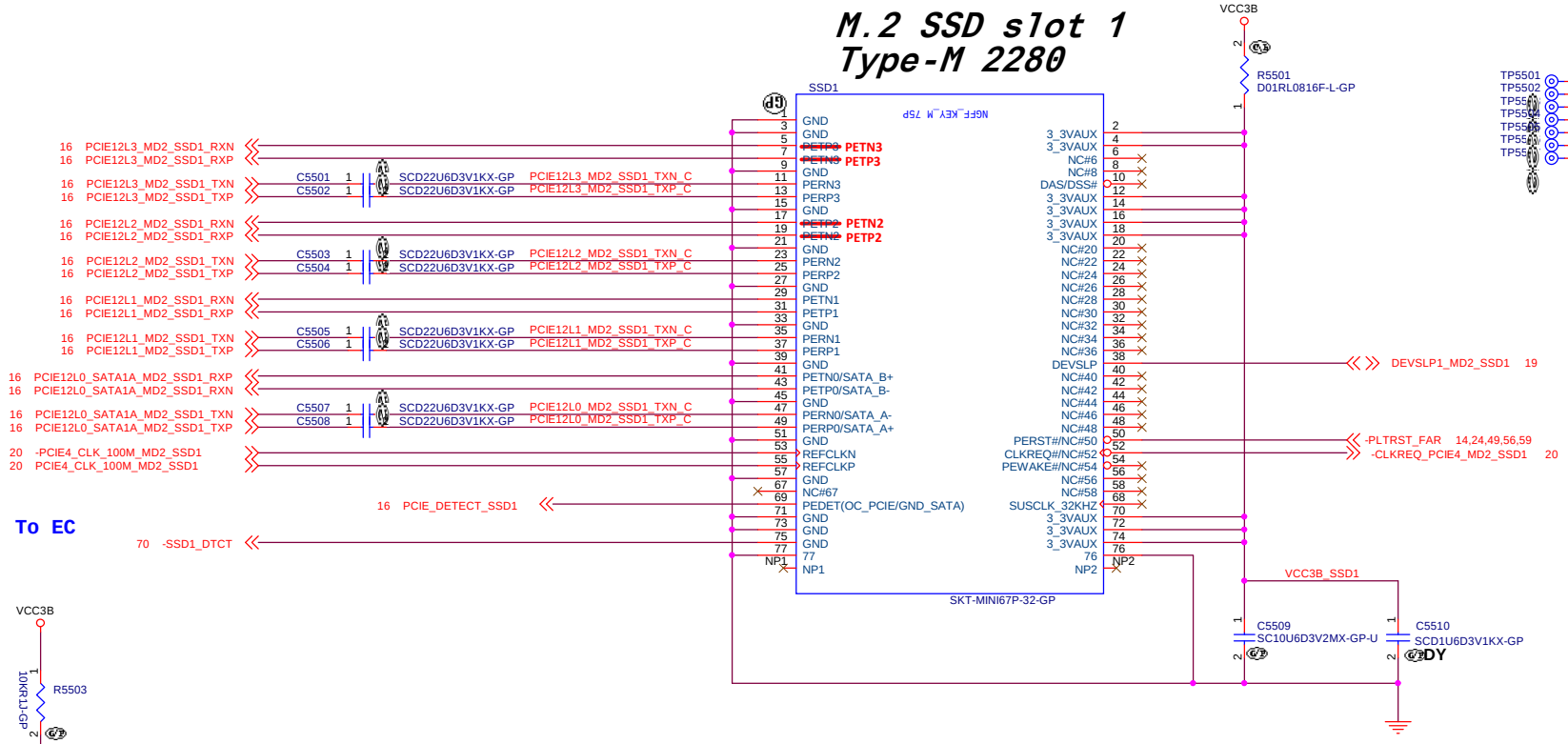
M.2 SSD slot 1
Type-M 2280

M.2 SSD1 L3

M.2 SSD1 L2

M.2 SSD1 L1

M.2 SSD1 L0



TABLE

PCIE_DETECT_SSD1	Device
LOW	SATA SSD
High	PCIe SSD

ULT

緯創資通 Wistron Corporation
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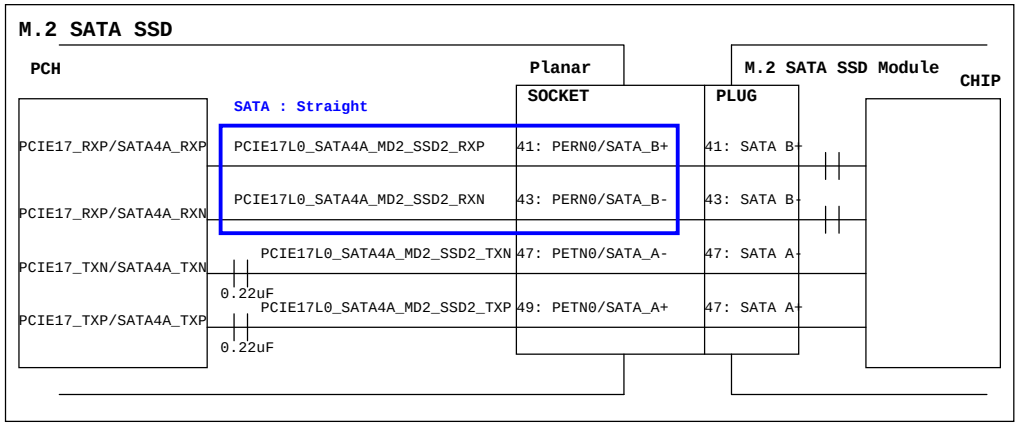
Taipei Hsien 221, Taiwan, R.O.C.

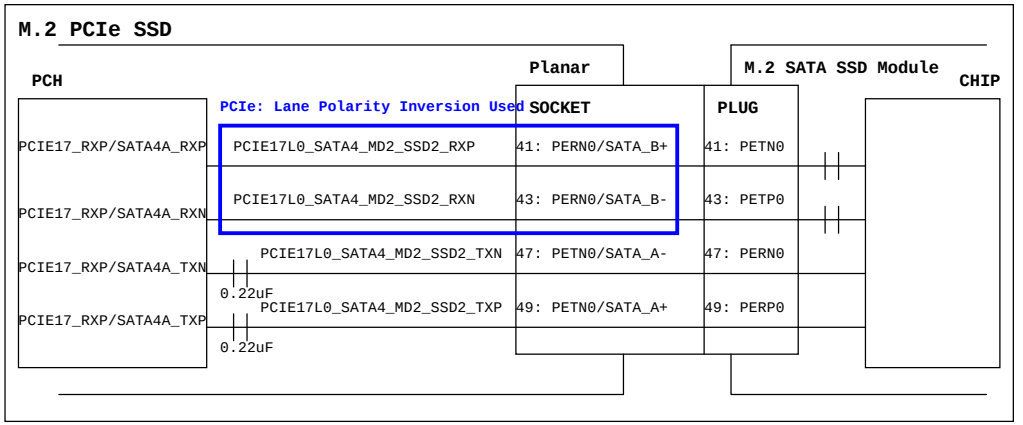
Title: M.2 SATA/PCIE SSD CARDSLOT1

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 55 of 110

M.2 SSD





M.2 SSD slot 2
Type-M 2280

M.2 SSD2 L3

M.2 SSD2 L2

M.2 SSD2 L1

M.2 SSD2 L0

To EC

SSD2

SKT-MINI67P-32-GP

VCC3B

R5601 D01RL0816F-L-GP

R5603 10KR1J-GP

-CLKREQ_PCIE7_MD2_SSD2

C5609 SC10U6D3V2MX-GP-U

C5610 SCD1U6D3V1KX-GP DY

VCC3B_SSD2

TP5601 VCC3B_SSD2
TP5602 DEVSLP4_MD2_SSD2
TP5603 PCIE_DETECT_SSD2
TP5604 -SSD2_DTCT
TP5605 -PLTRST_FAR
TP5606 -CLKREQ_PCIE7_MD2_SSD2
TP5607 GND

DEVSLP4_MD2_SSD2 19

-PLTRST_FAR 14,24,49,55,59

-CLKREQ_PCIE7_MD2_SSD2 20

TABLE

PCIE_DETECT_SSD1	Device
LOW	SATA SSD
High	PCIe SSD

ULT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: M.2 SATA/PCIE SSD CARDSLOT2

Size: A3 | Document Number: PADME | Rev: 1

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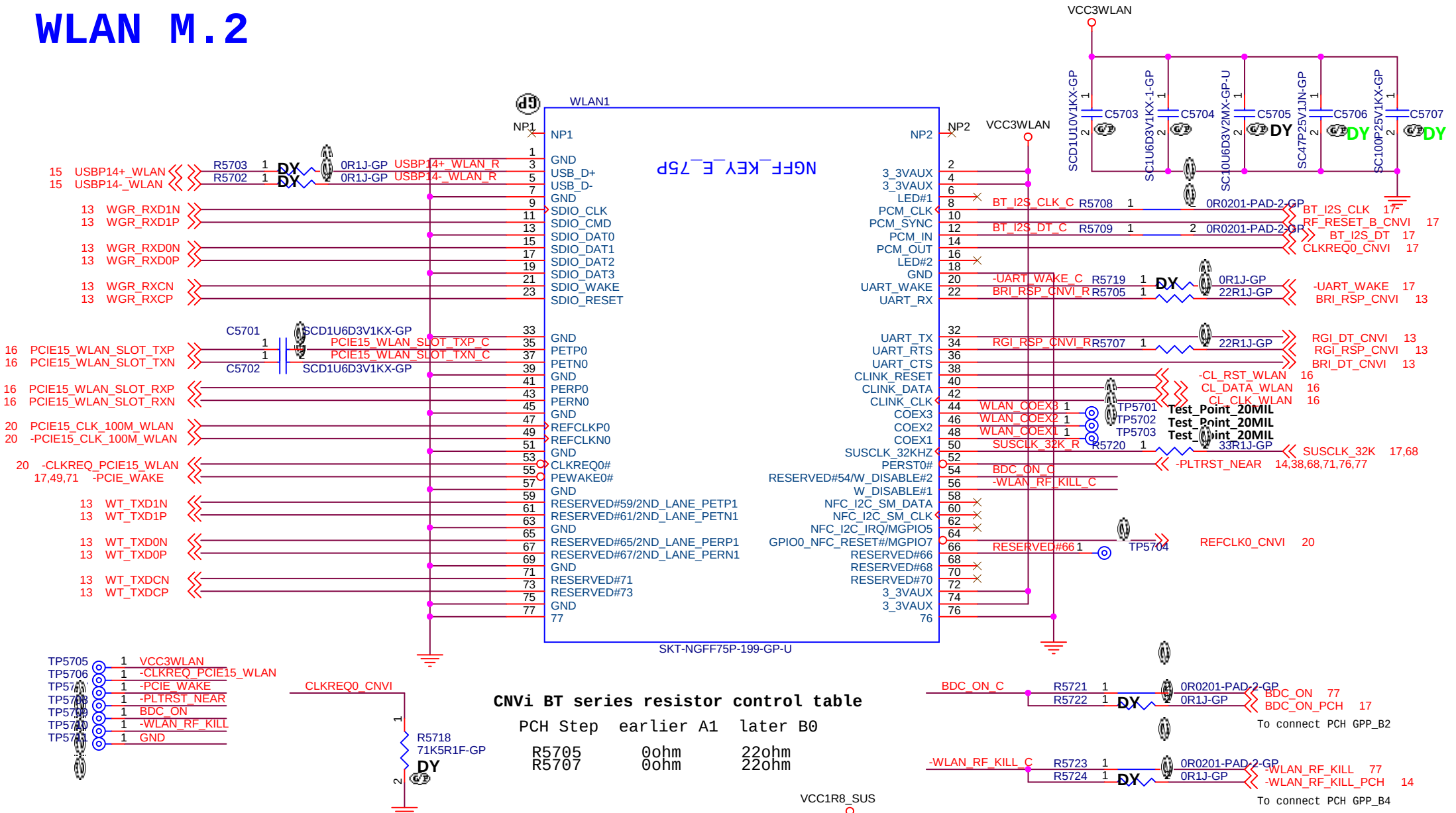
WLAN M.2



ULT

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Title: **WLAN M.2 2230**

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 57 of 110

Reserved

ULT

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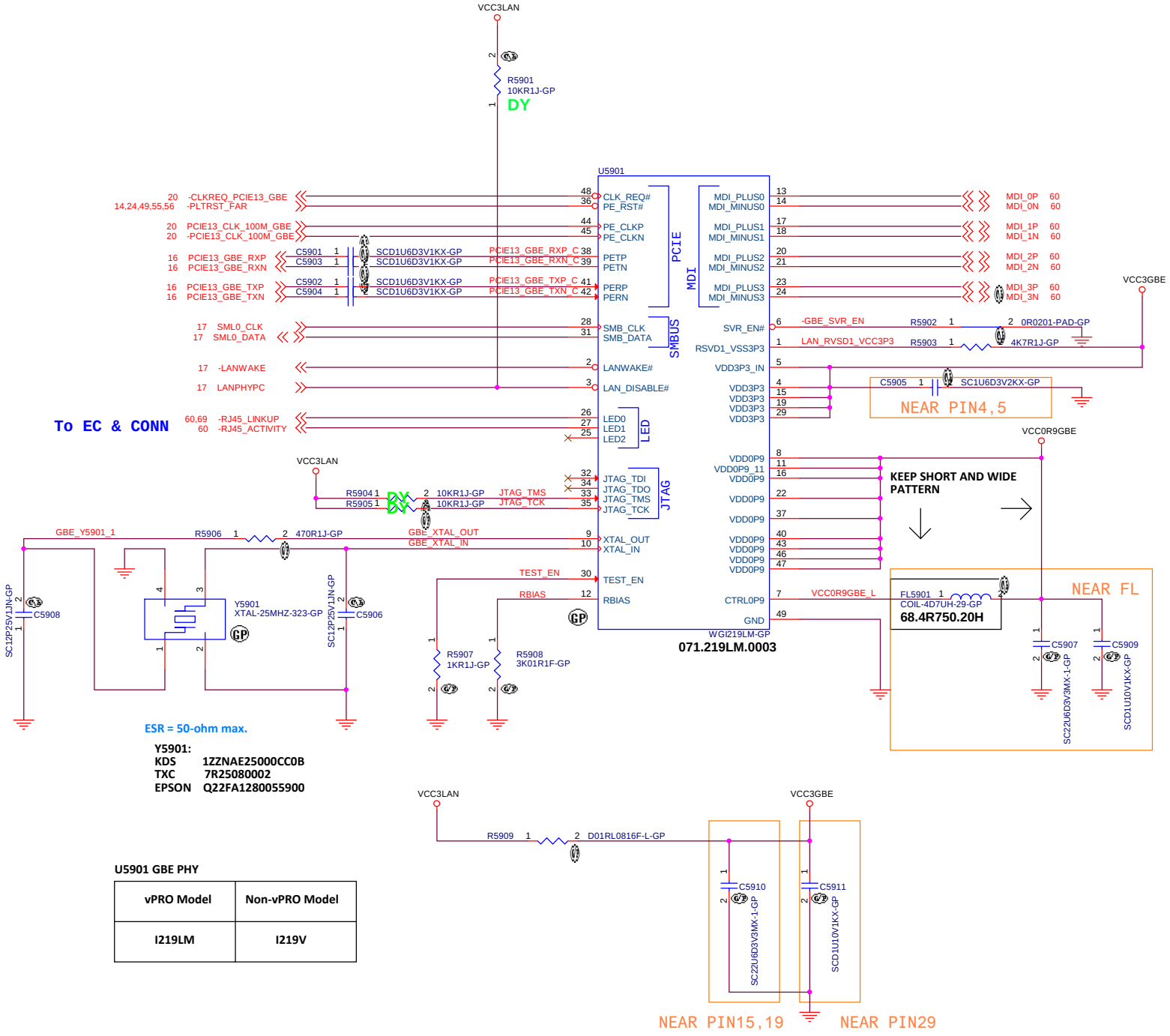
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***M.2 WWAN CARD SLOT***

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 58 of 110

LAN



U5901 GBE PHY

vPRO Model	Non-vPRO Model
I219LM	I219V

ULT

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Taipei Hsien 221, Taiwan, R.O.C.

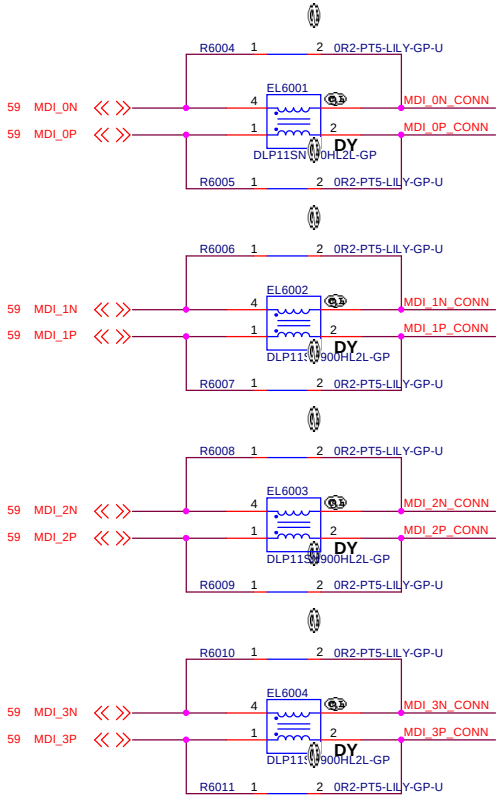
Title: GBE JACKSONVILLE

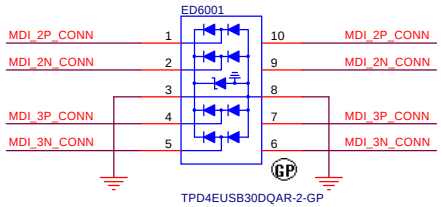
Size	Document Number	Rev
A3	PADME	1

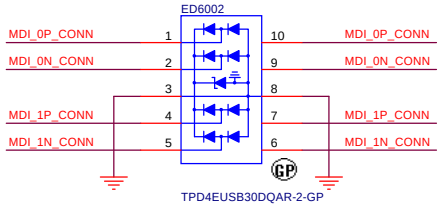
Date: Monday, October 01, 2018 Sheet 59 of 110

TABLE FL85-FL88

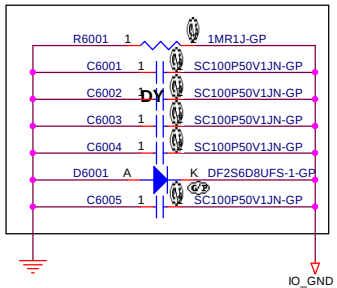
1st: Murata, DLP11SN900HL2
2nd: TDK, MCZ1210AH900L2TA0G



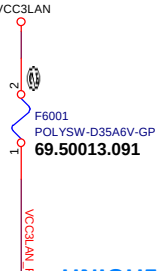




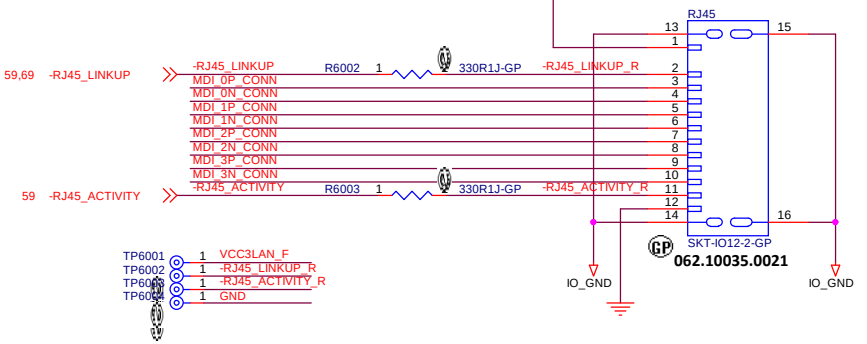
075.00430.0070



	Vendor	Description	Wistron PN
1st	LITTELFUSE	0603L035YR	069.4R350.0001
2nd	BOURNS	MF-FSMF035X-2	69.50013.091
3rd	AEM	PMS0603-035	XXX.



UNIQUE RJ45 CONN (LAN1)



ULT

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***GBE RJ45 CONNECTOR***

Size	Document Number	Rev
A3	PADME	1

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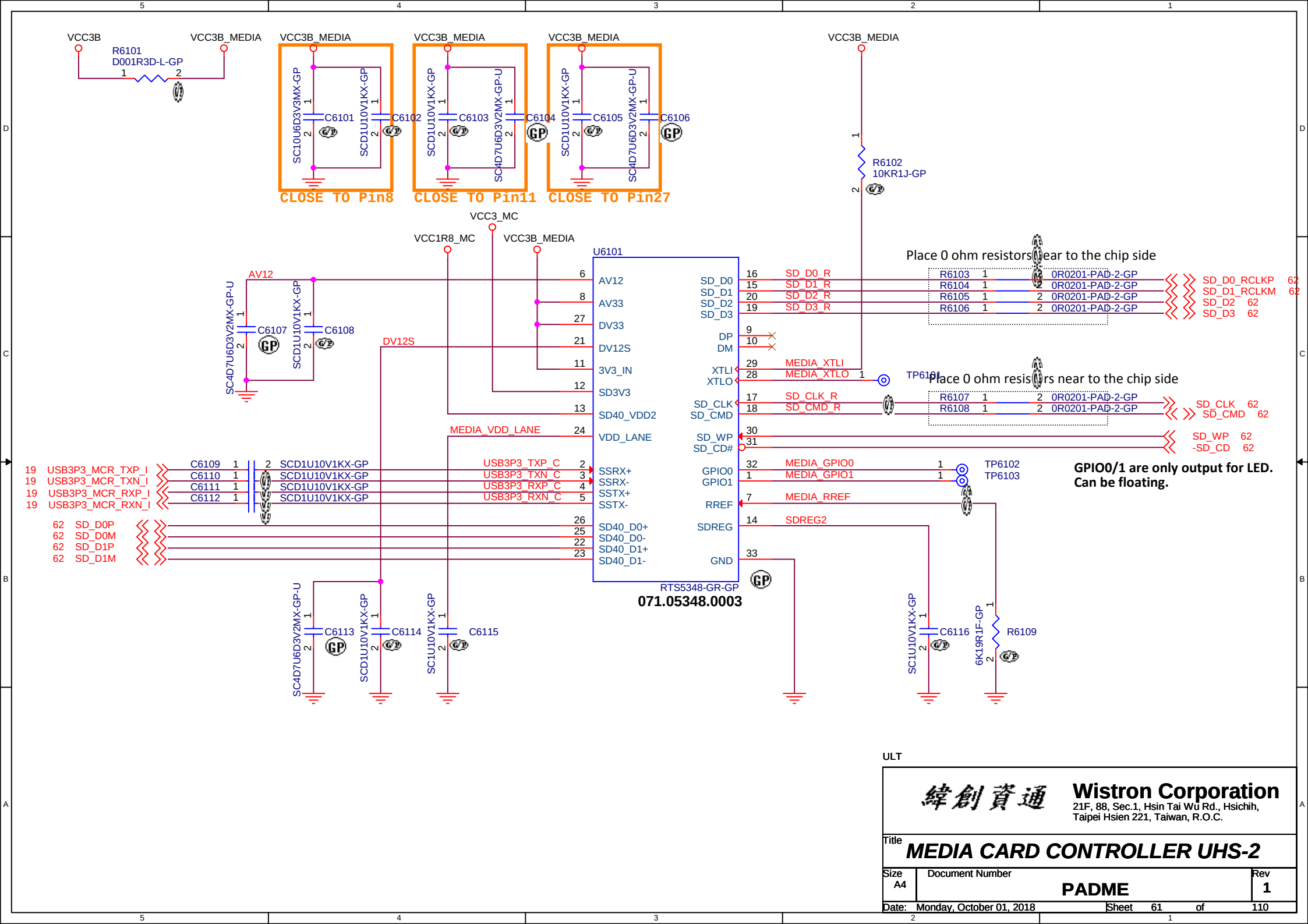
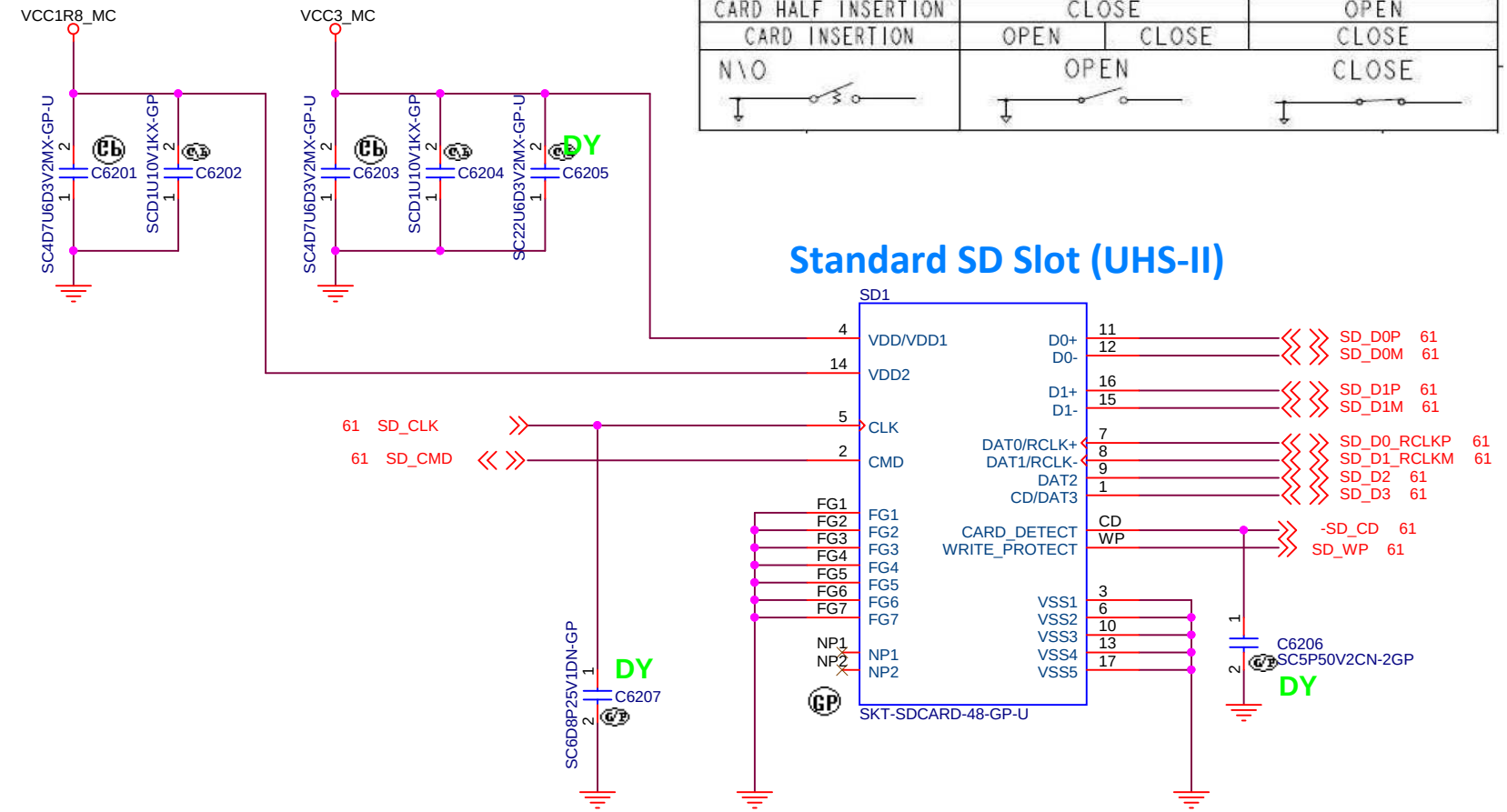


ULT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***MEDIA CARD CONTROLLER UHS-2***	
Size A4	Document Number **PADME**	Rev 1
Date: Monday, October 01, 2018	Sheet 61 of 110	

	WRITE PROTECT SWITCH		CARD DETECT SWITCH
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	OPEN		OPEN
CARD HALF INSERTION	CLOSE		OPEN
CARD INSERTION	OPEN	CLOSE	CLOSE
N\O	OPEN		CLOSE

From RTS5348



ULT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MEDIA CARD INTERFACE UHS-2**

Size	Document Number	Rev
A4	PADME	1

Date: Monday, October 01, 2018 Sheet 62 of 110

AUDIO

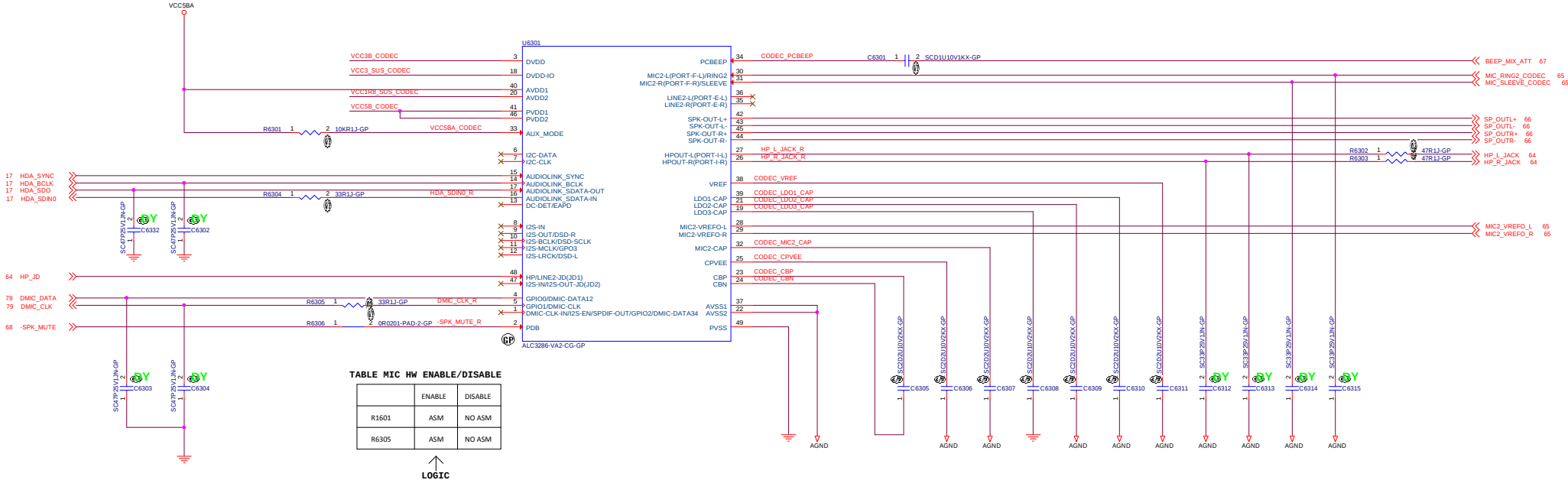
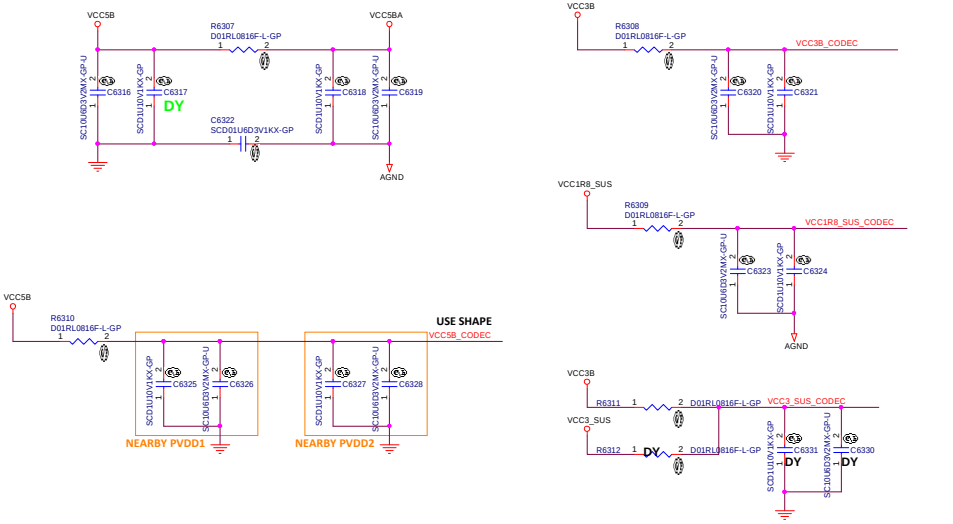
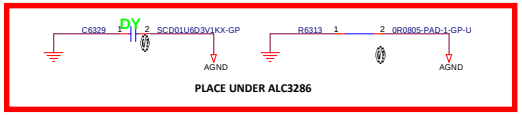


TABLE MIC HW ENABLE/DISABLE

	ENABLE	DISABLE
R1601	ASM	NO ASM
R6305	ASM	NO ASM

LOGIC





ULT

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO ALC3286-CG**

Size	Document Number	Rev
A2	PADME	1

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AUDIO

NEAR AUDIO1 CONN

63 HP_L_JACK
63 HP_R_JACK
L6401 1 2 MMZ1005Y152CT-GP
L6402 1 2 MMZ1005Y152CT-GP
220R1J-GP R6401 DY
220R1J-GP R6402 DY
SC1KP25V1KX-GP C6401
SC1KP25V1KX-GP C6402
VCC3B
R6403 10KR2J-L-GP
AGND
AGND
WIDE AND SHORT PATTERN

Headphone Jack AUDIO CONN

AUD1
3 RING2
1 HP_L_JACK_CONN
5 AUDIO3V
6
2 HP_R_JACK_CONN
4 SLEEVE
MS1
MS2
Audio(IP/NK comb)
NP1
NP2
AUDIO-JK651-GP
R6404 100KR1J-GP
ESD9B3.3DST5G-GP ED6405
AZ5125-01H-R7G-GP ED6401
AZ5125-01H-R7G-GP ED6402
AZ5125-01H-R7G-GP ED6403
AZ5125-01H-R7G-GP ED6404

MIC_RING2 65
HP_JACK_IN 64,68
MIC_SLEEVE 65

TP6401 1 HP_L_JACK_CONN
TP6402 1 HP_R_JACK_CONN
TP6403 1 MIC_RING2
TP6404 1 MIC_SLEEVE
TP6405 1 AUDIO3V
TP6406 1 HP_JACK_IN

R6409 1 2 0R0402-PAD
AGND
R6410 1 2 0R0402-PAD
AGND

AUDIO JACK SENSE

VCC3B
R6405 100KR1J-GP
HP_JD 63
R6406 1 DY 2 0R1J-GP
AGND
R6407 200KR1F-GP
HP_JD_SYS
64,68 HP_JACK_IN
R6408 1 2 22KR1J-GP
HP_JACK_IN_G
Q6401 SSM3K15AMFV-GP-U
C6403 SC2D2U10V2KX-GP DY
AGND

ULT

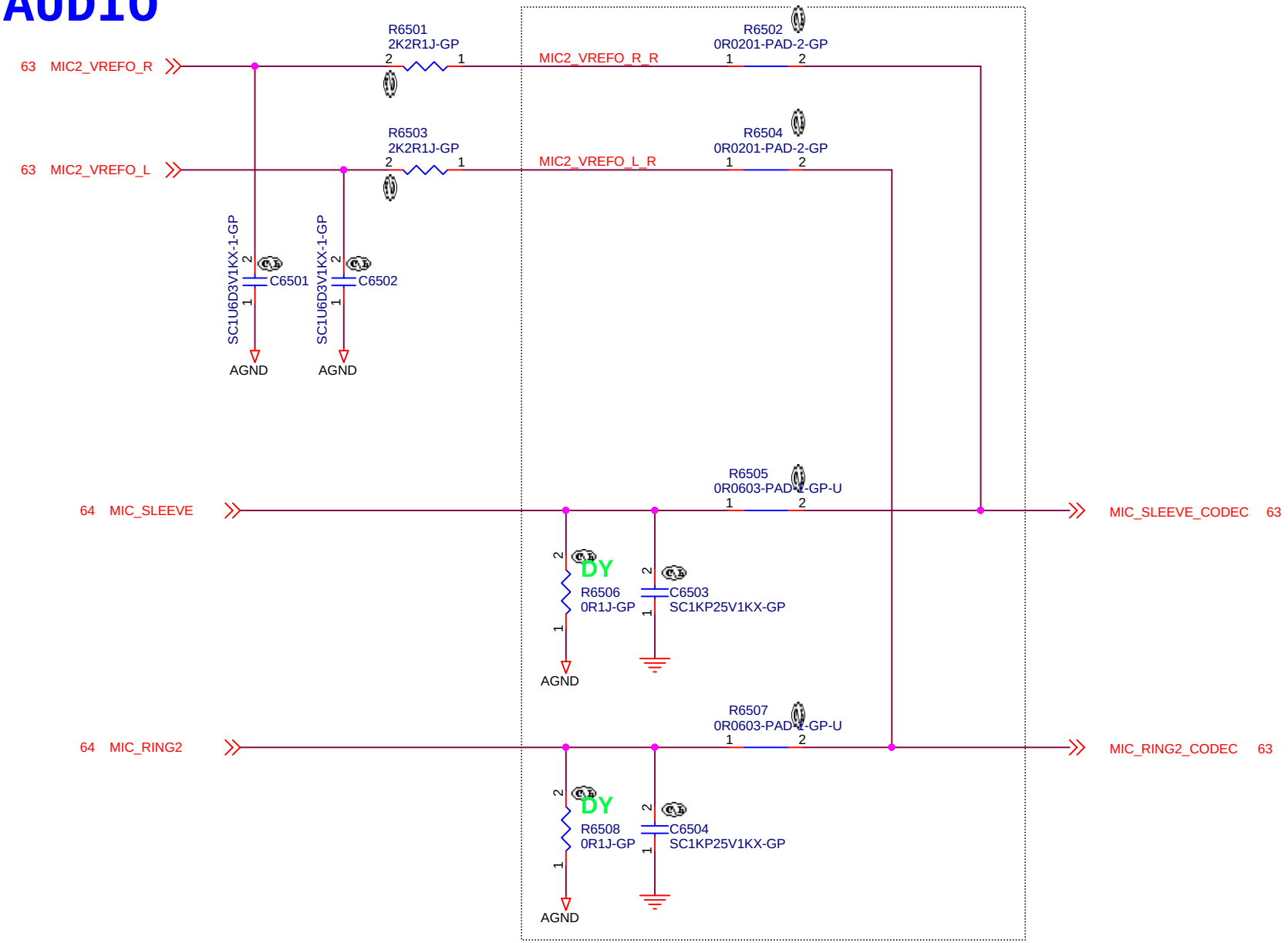
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CONNECTOR/SENSE

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 64 of 110

AUDIO



NEAR EXT MIC CONN

ULT

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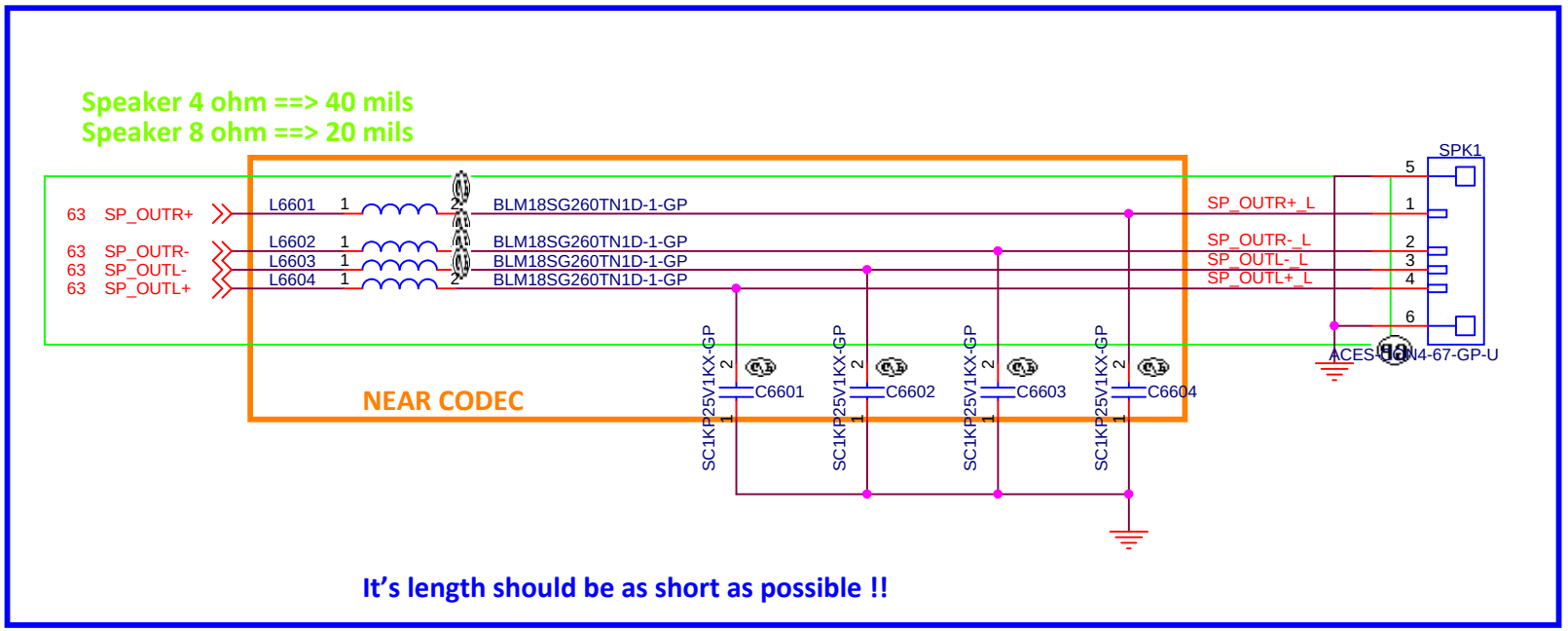
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

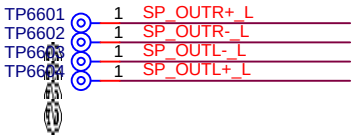
Title: ***AUDIO EXT MIC I/F***

Size	Document Number	Rev
A4	**PADME**	1

Date: Monday, October 01, 2018 Sheet 65 of 110

AUDIO





ULT

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Title: ***AUDIO SPEAKER***

Size	Document Number	Rev
A4	PADME	1

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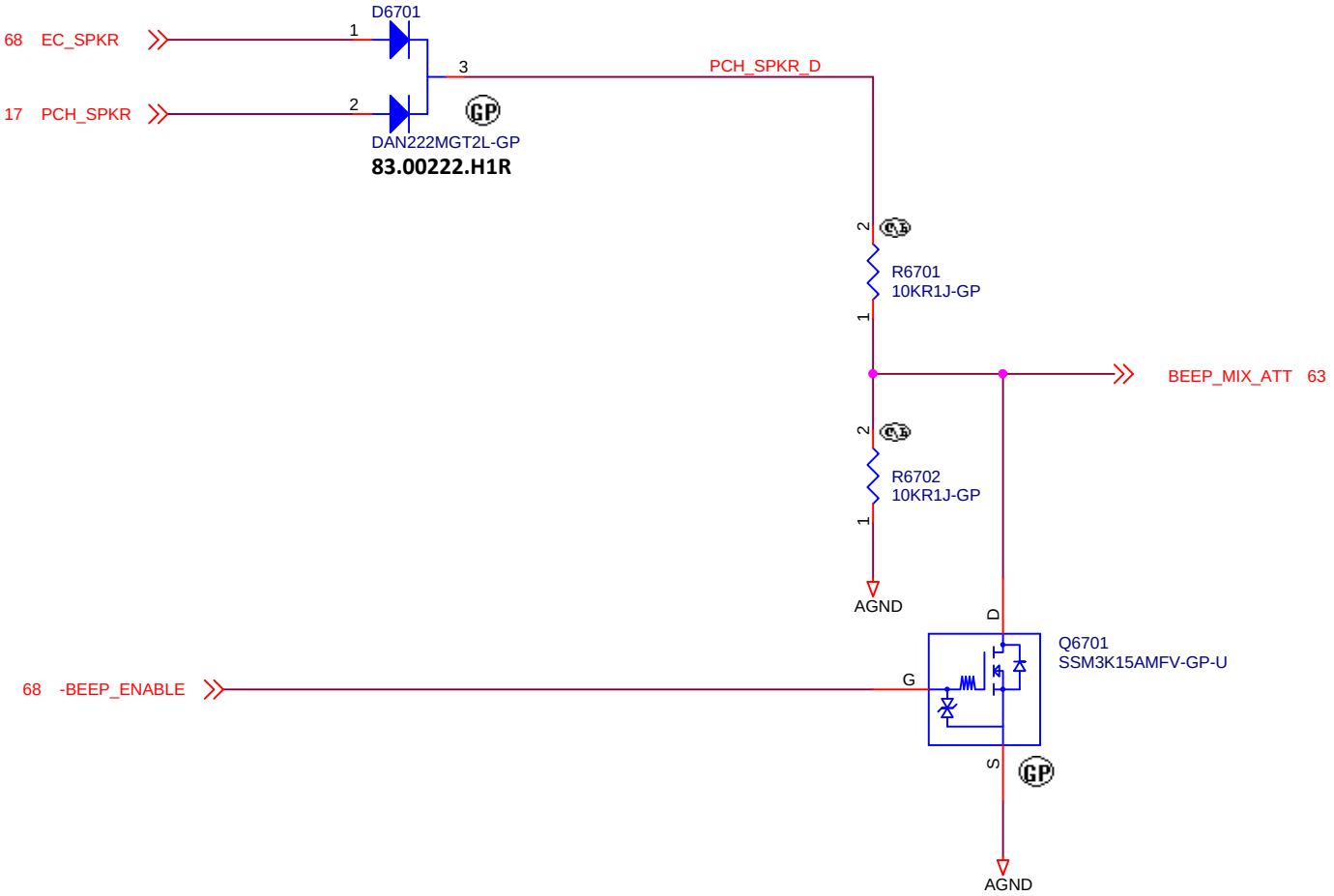
AUDIO



ULT

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Title: ***AUDIO BEEP***

Size	Document Number	Rev
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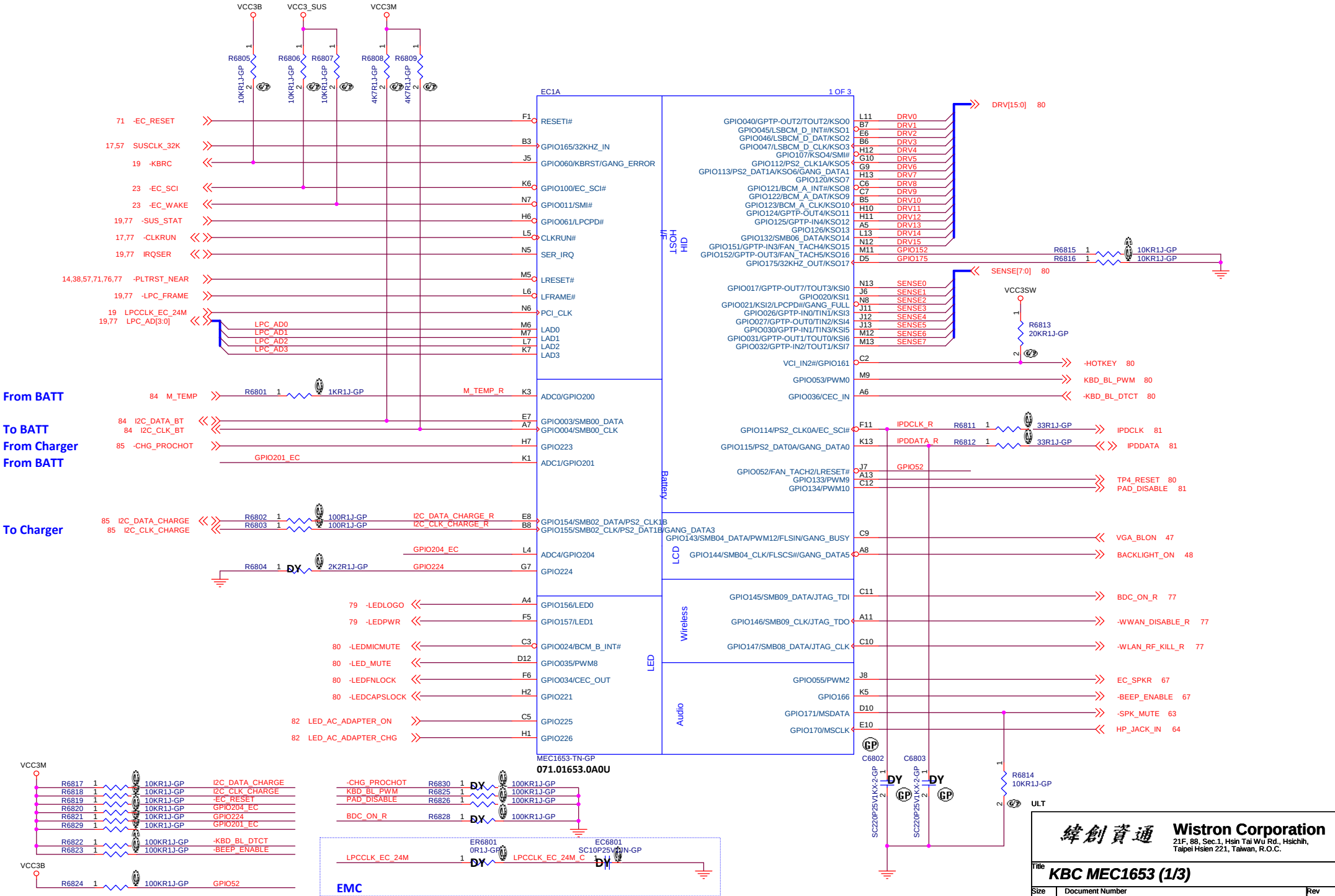
VCC3B
VCC3_SUS
VCC3M
R6805 10KR1J-GP
R6806 10KR1J-GP
R6807 10KR1J-GP
R6808 4K7R1J-GP
R6809 4K7R1J-GP
EC1A
1 OF 3
RESETI#
GPIO165/32KHZ_IN
GPIO060/KBRST/GANG_ERROR
GPIO100/EC_SCI#
GPIO011/SMI#
GPIO061/LPCPD#
CLKRUN#
SER_IRQ
LRESET#
LFRAME#
PCI_CLK
LAD0
LAD1
LAD2
LAD3
ADC0/GPIO200
GPIO003/SMB00_DATA
GPIO004/SMB00_CLK
GPIO223
ADC1/GPIO201
GPIO154/SMB02_DATA/PS2_CLK1B
GPIO155/SMB02_CLK/PS2_DAT1B/GANG_DATA3
ADC4/GPIO204
GPIO224
GPIO156/LED0
GPIO157/LED1
GPIO024/BCM_B_INT#
GPIO035/PWM8
GPIO034/CEC_OUT
GPIO221
GPIO225
GPIO226
MEC1653-TN-GP
071.01653.0A0U
HOST I/F
Battery
LCD
Wireless
LED
Audio
GPIO040/GPTP-OUT2/TOUT2/KSO0
GPIO045/LSBCM_D_INT#/KSO1
GPIO046/LSBCM_D_DAT/KSO2
GPIO047/LSBCM_D_CLK/KSO3
GPIO107/KSO4/SMI#
GPIO112/PS2_CLK1A/KSO5
GPIO113/PS2_DAT1A/KSO6/GANG_DATA1
GPIO120/KSO7
GPIO121/BCM_A_INT#/KSO8
GPIO122/BCM_A_DAT/KSO9
GPIO123/BCM_A_CLK/KSO10
GPIO124/GPTP-OUT4/KSO11
GPIO125/GPTP-IN4/KSO12
GPIO126/KSO13
GPIO132/SMB06_DATA/KSO14
GPIO151/GPTP-IN3/FAN_TACH4/KSO15
GPIO152/GPTP-OUT3/FAN_TACH5/KSO16
GPIO175/32KHZ_OUT/KSO17
GPIO017/GPTP-OUT7/TOUT3/KSI0
GPIO020/KSI1
GPIO021/KSI2/LPCPD#/GANG_FULL
GPIO026/GPTP-IN0/TIN1/KSI3
GPIO027/GPTP-OUT0/TIN2/KSI4
GPIO030/GPTP-IN1/TIN3/KSI5
GPIO031/GPTP-OUT1/TOUT0/KSI6
GPIO032/GPTP-IN2/TOUT1/KSI7
VCI_IN2#/GPIO161
GPIO053/PWM0
GPIO036/CEC_IN
GPIO114/PS2_CLK0A/EC_SCI#
GPIO115/PS2_DAT0A/GANG_DATA0
GPIO052/FAN_TACH2/LRESET#
GPIO133/PWM9
GPIO134/PWM10
GPIO143/SMB04_DATA/PWM12/FLSIN/GANG_BUSY
GPIO144/SMB04_CLK/FLSCS#/GANG_DATA5
GPIO145/SMB09_DATA/JTAG_TDI
GPIO146/SMB09_CLK/JTAG_TDO
GPIO147/SMB08_DATA/JTAG_CLK
GPIO055/PWM2
GPIO166
GPIO171/MSDATA
GPIO170/MSCLK
DRV[15:0] 80
SENSE[7:0] 80
VCC3SW
R6813 20KR1J-GP
R6815 10KR1J-GP
R6816 10KR1J-GP
-HOTKEY 80
KBD_BL_PWM 80
-KBD_BL_DTCT 80
IPDCLK 81
IPDDATA 81
TP4_RESET 80
PAD_DISABLE 81
VGA_BLON 47
BACKLIGHT_ON 48
BDC_ON_R 77
-WWAN_DISABLE_R 77
-WLAN_RF_KILL_R 77
EC_SPKR 67
-BEEP_ENABLE 67
-SPK_MUTE 63
HP_JACK_IN 64
R6814 10KR1J-GP
ULT
C6802 SC220P25V1KX-2-GP
C6803 SC220P25V1KX-2-GP
From BATT
To BATT
From Charger
From BATT
To Charger
71 -EC_RESET
17,57 SUSCLK_32K
19 -KBRC
23 -EC_SCI
23 -EC_WAKE
19,77 -SUS_STAT
17,77 -CLKRUN
19,77 IRQSER
14,38,57,71,76,77 -PLTRST_NEAR
19,77 -LPC_FRAME
19 LPCCLK_EC_24M
19,77 LPC_AD[3:0]
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
84 M_TEMP
R6801 1KR1J-GP
M_TEMP_R
84 I2C_DATA_BT
84 I2C_CLK_BT
85 -CHG_PROCHOT
GPIO201_EC
85 I2C_DATA_CHARGE
85 I2C_CLK_CHARGE
R6802 100R1J-GP
R6803 100R1J-GP
I2C_DATA_CHARGE_R
I2C_CLK_CHARGE_R
R6804 DY 2K2R1J-GP
GPIO204_EC
GPIO224
79 -LEDLOGO
79 -LEDPWR
80 -LEDMICMUTE
80 -LED_MUTE
80 -LEDFNLOCK
80 -LEDCAPSLOCK
82 LED_AC_ADAPTER_ON
82 LED_AC_ADAPTER_CHG
VCC3M
R6817 10KR1J-GP I2C_DATA_CHARGE
R6818 10KR1J-GP I2C_CLK_CHARGE
R6819 10KR1J-GP -EC_RESET
R6820 10KR1J-GP GPIO204_EC
R6821 10KR1J-GP GPIO224
R6829 10KR1J-GP GPIO201_EC
R6822 100KR1J-GP -KBD_BL_DTCT
R6823 100KR1J-GP -BEEP_ENABLE
VCC3B
R6824 100KR1J-GP GPIO52
-CHG_PROCHOT R6830 DY 100KR1J-GP
KBD_BL_PWM R6825 100KR1J-GP
PAD_DISABLE R6826 100KR1J-GP
BDC_ON_R R6828 DY 100KR1J-GP
EMC
LPCCLK_EC_24M
ER6801 0R1J-GP DY
LPCCLK_EC_24M_C
EC6801 SC10P25V1JN-GP DY
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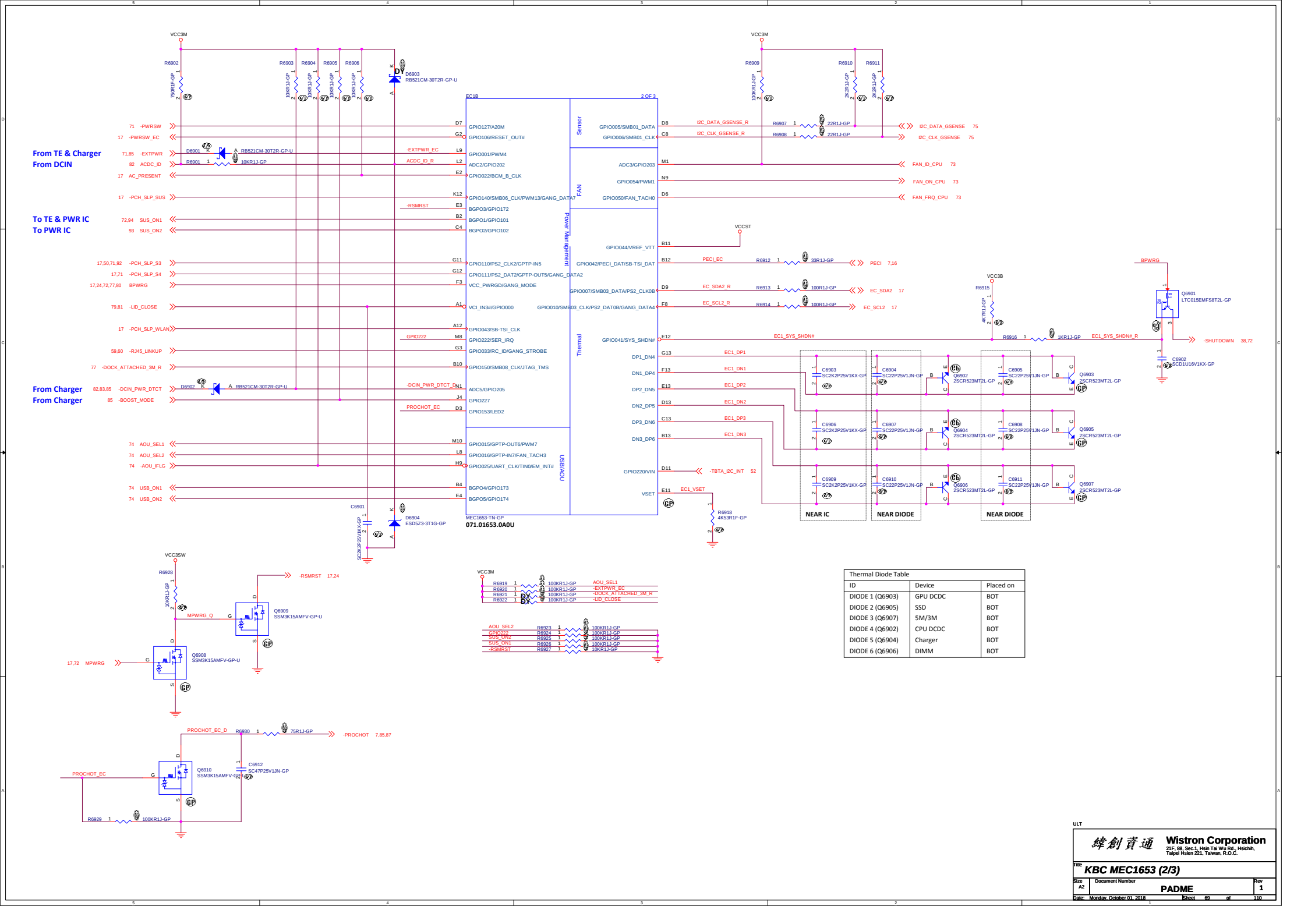
Title
KBC MEC1653 (1/3)
Size A3
Document Number
PADME
Rev 1
Date: Monday, October 01, 2018
Sheet 68 of 110



Thermal Diode Table		
ID	Device	Placed on
DIODE 1 (Q6903)	GPU DCDC	BOT
DIODE 2 (Q6905)	SSD	BOT
DIODE 3 (Q6907)	5M/3M	BOT
DIODE 4 (Q6902)	CPU DCDC	BOT
DIODE 5 (Q6904)	Charger	BOT
DIODE 6 (Q6906)	DIMM	BOT

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Title: **KBC MEC1653 (2/3)**

Size	Document Number	Rev
A2	PADME	1

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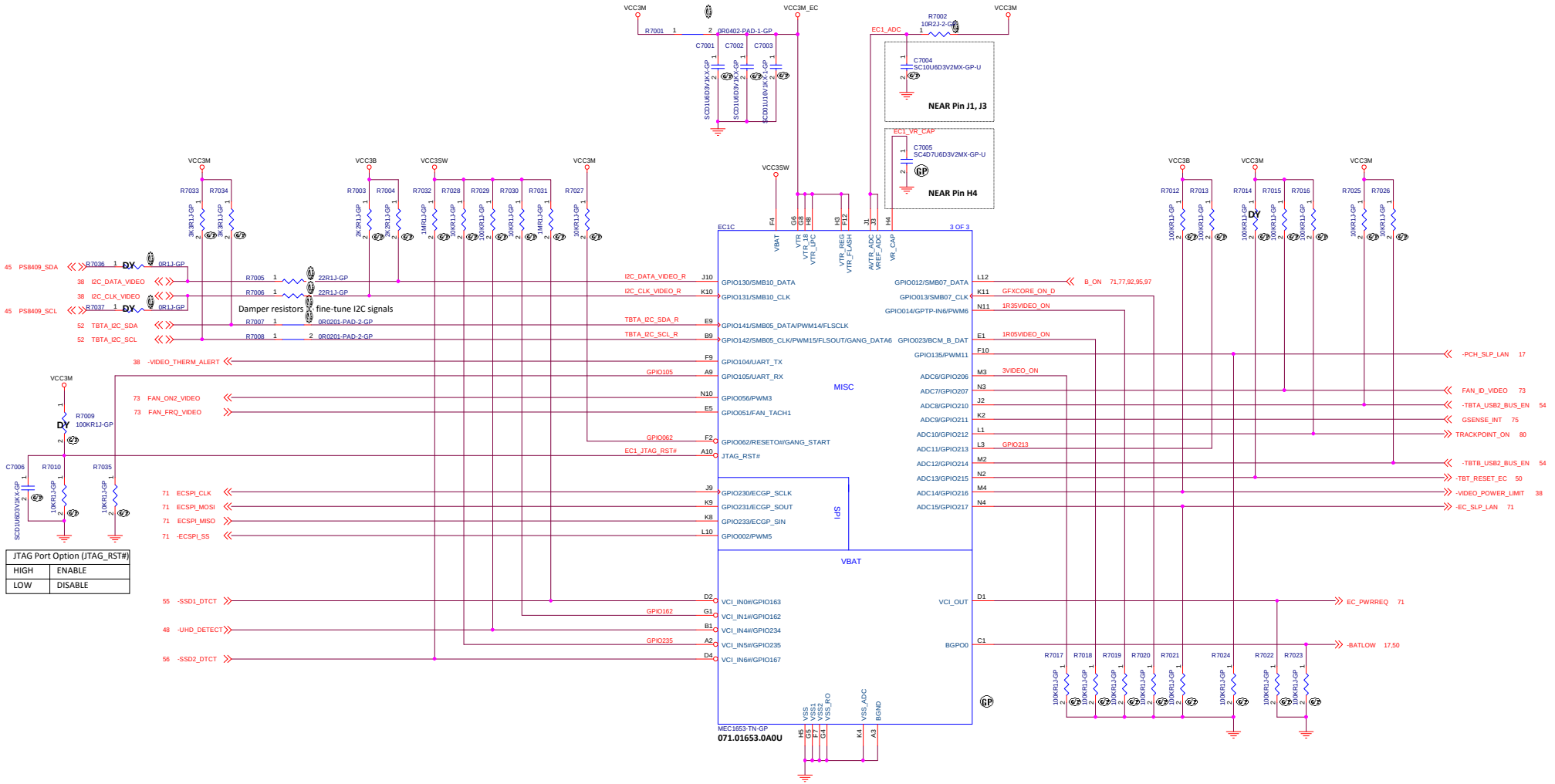

Title	KBC MEC1653 (3/3)
Size	A2
Document Number	PADME
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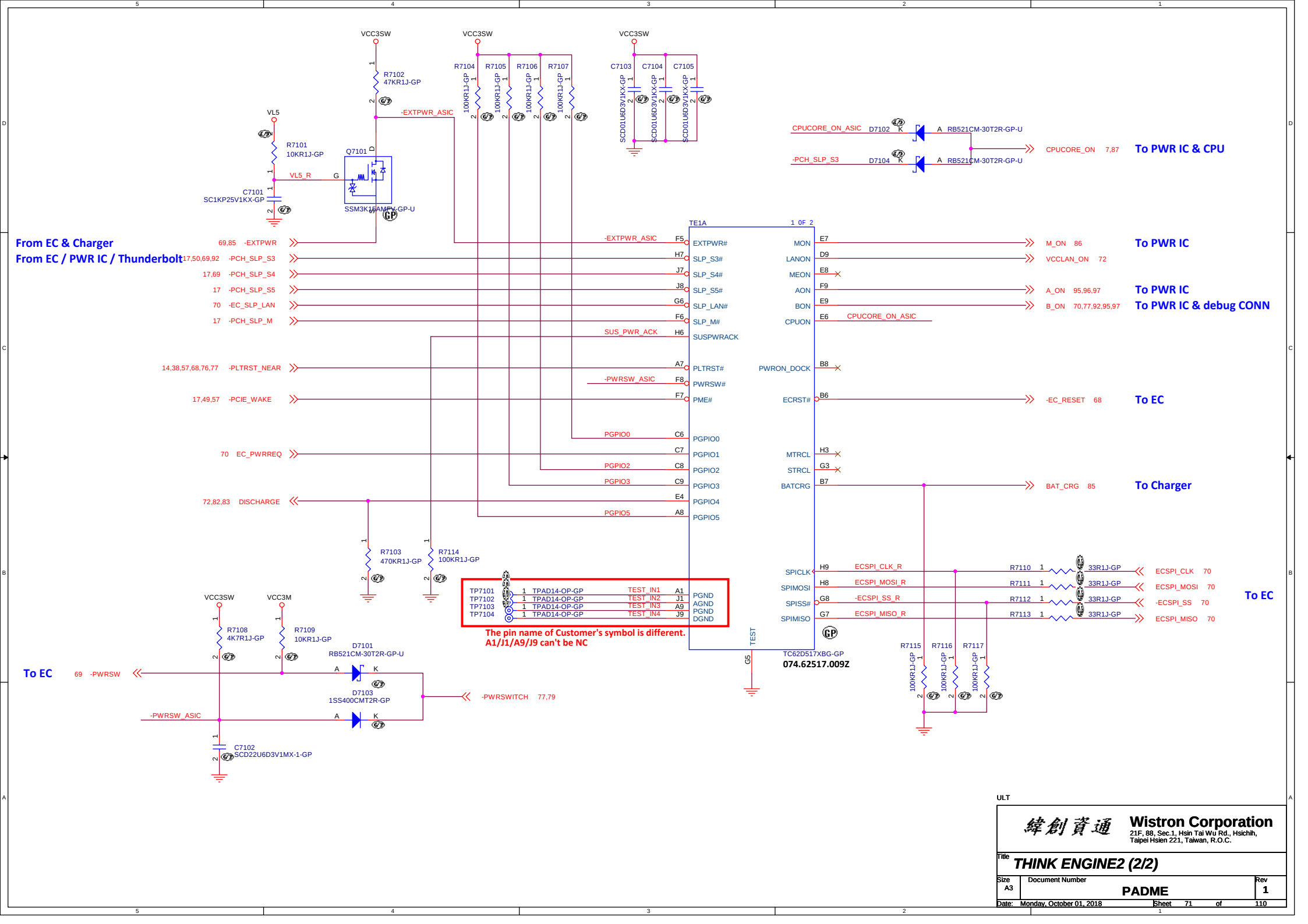
From EC & Charger
From EC / PWR IC / Thunderbolt
To PWR IC & CPU
To PWR IC
To PWR IC
To PWR IC & debug CONN
To EC
To Charger
To EC
To EC
The pin name of Customer's symbol is different.
A1/J1/A9/J9 can't be NC
TC62D517XBG-GP
074.62517.009Z
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Wistron Corporation
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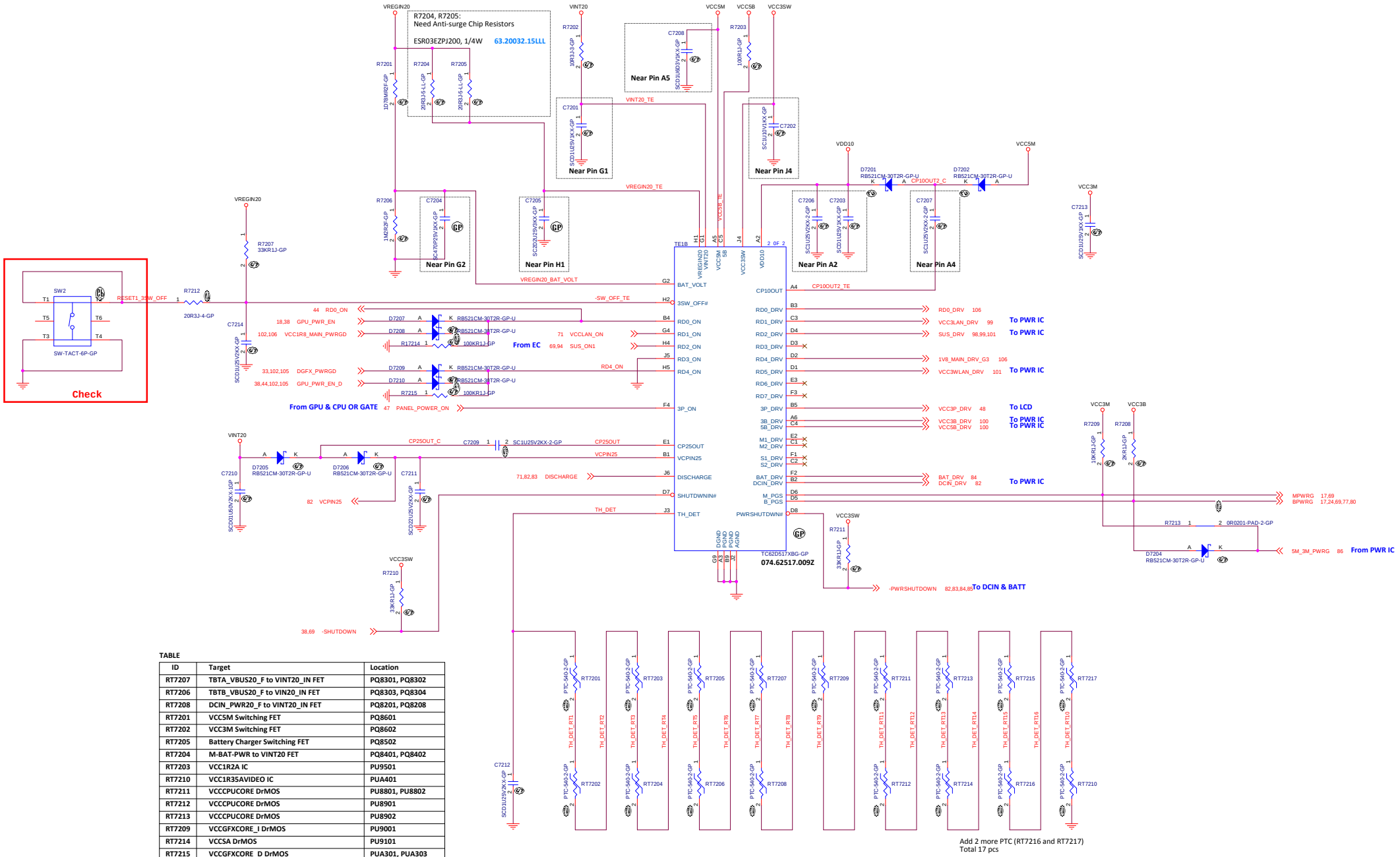
Title
THINK ENGINE2 (2/2)
Size A3
Document Number
PADME
Rev 1
Date: Monday, October 01, 2018
Sheet 71 of 110



TABLE

ID	Target	Location
RT7207	TBTA_VBUS20_F to VINT20_IN FET	PQ8301, PQ8302
RT7206	TBTB_VBUS20_F to VIN20_IN FET	PQ8303, PQ8304
RT7208	DCIN_PWR20_F to VINT20_IN FET	PQ8201, PQ8208
RT7201	VCC5M Switching FET	PQ8601
RT7202	VCC3M Switching FET	PQ8602
RT7205	Battery Charger Switching FET	PQ8502
RT7204	M-BAT-PWR to VINT20 FET	PQ8401, PQ8402
RT7203	VCC1R2A IC	PU9501
RT7210	VCC1R35AVIDEO IC	PUA401
RT7211	VCCCPUCORE DrMOS	PU8801, PU8802
RT7212	VCCCPUCORE DrMOS	PU8901
RT7213	VCCCPUCORE DrMOS	PU8902
RT7209	VCCGFXCORE_I DrMOS	PU9001
RT7214	VCCSA DrMOS	PU9101
RT7215	VCCGFXCORE_D DrMOS	PUA301, PUA303
RT7216	VCCGFXCORE_D DrMOS	PUA302
RT7217	CPU Die	CPU1

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Title: THINK ENGINE3 (2/2)

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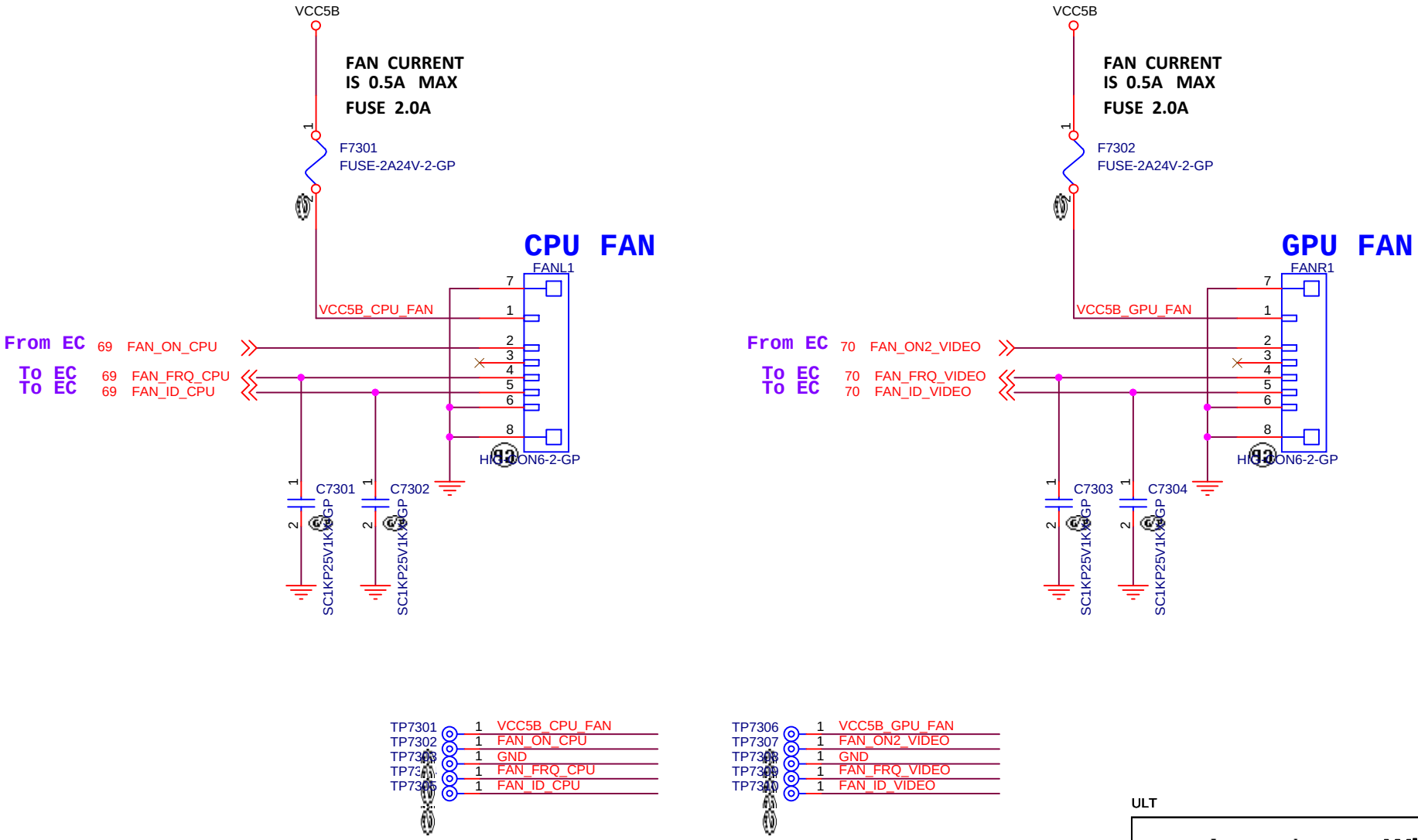
FAN



TP7301	1	VCC5B_CPU_FAN
TP7302	1	FAN_ON_CPU
TP7303	1	GND
TP7304	1	FAN_FRQ_CPU
TP7305	1	FAN_ID_CPU

TP7306	1	VCC5B_GPU_FAN
TP7307	1	FAN_ON2_VIDEO
TP7308	1	GND
TP7309	1	FAN_FRQ_VIDEO
TP7310	1	FAN_ID_VIDEO

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Title **FAN CONNECTOR**

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TABLE of USB Charge	
TI	SN1702001RTER (PG1.1)
Pericom	PI5USB2546HZHEX

TABLE of USB3.0 Single	
GMT	G548A1F51U
TI	TPS2069CDGNR-2

U7402 RCLAMP0524PATCT-1-GP-U

U7401 RCLAMP0524PATCT-1-GP-U

U7403 AOZ8105CI-1-GP

U7405 AOZ8105CI-1-GP

USB_PWR_S1 WIDE PATTERN(MIN 500mA)

USB_PWR_S2 WIDE PATTERN(MIN 500mA)

Co-lay

EL7402 EL7403 EL7404 EL7405 EL7406 COIL-90OHM-100MHZ-5-GP

USB1 USB2 SKT-USB15-9-GP-U

DY

U7404 SN1702001RTER-GP

U7406 TPS2069CDGNR-GP

PAD1 PAD2 PAD3 PAD4 PAD5 PAD6 PAD7 PAD8 PAD9 PAD10 PAD11 PAD12 PAD13 PAD14 PAD15 PAD16 PAD17 PAD18

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Title: USB POWER/CONNECTOR		
Size: A3	Document Number: PADME	Rev: 1
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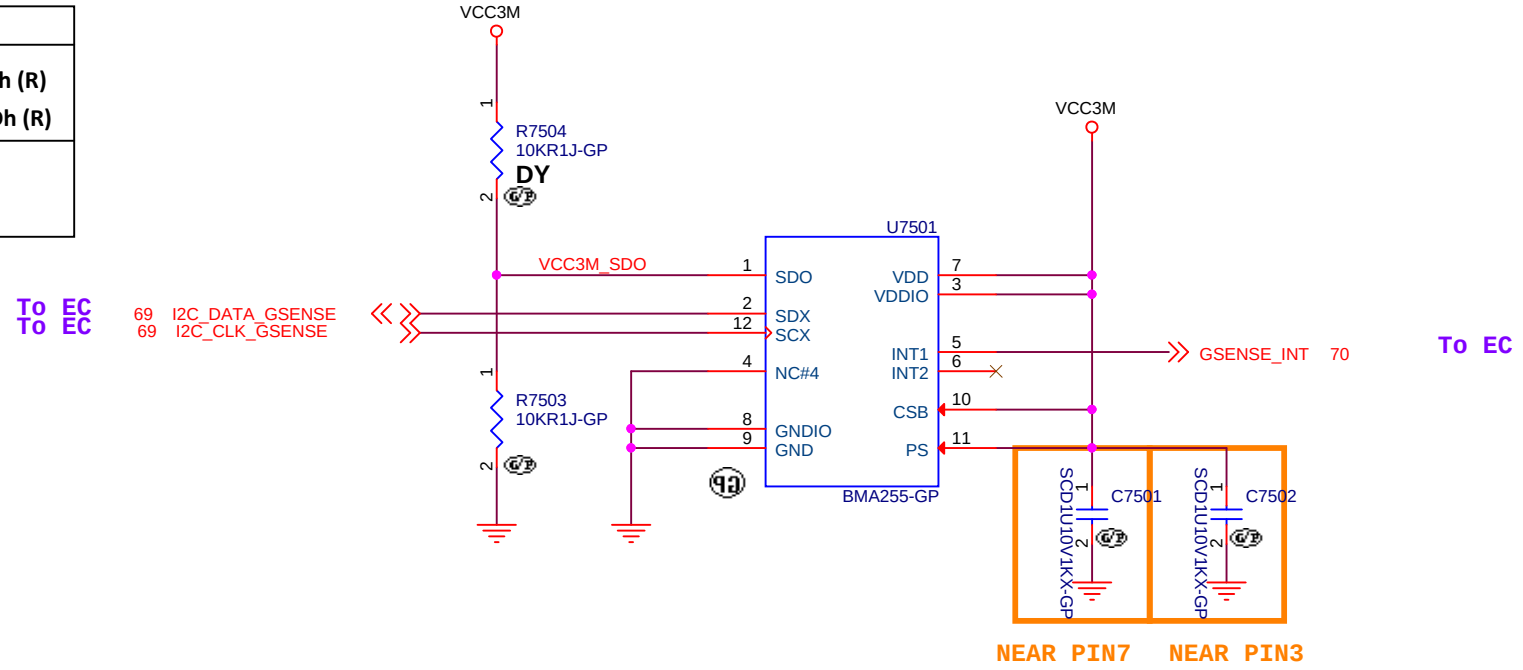
TABLE

P/N	ADDR_SEL	Address
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)
LIS2DWLTR	H	
	L	

TABLE of G-Sensor (U7501)

Vendor	P/N
Kionix	KX022-1020
ST Micro	LIS2DWLTR



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Title: ***APS G-SENSOR P-SENSOR***

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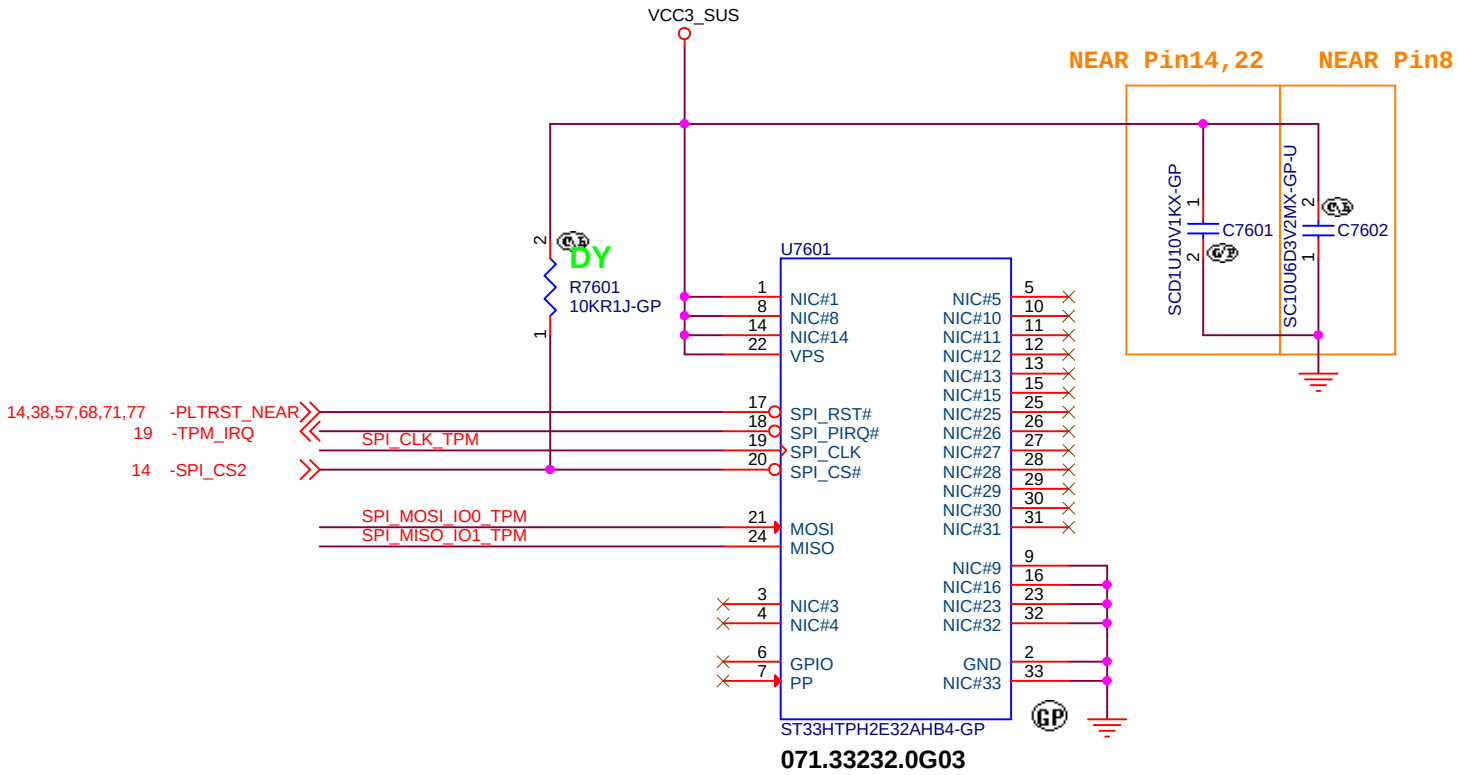
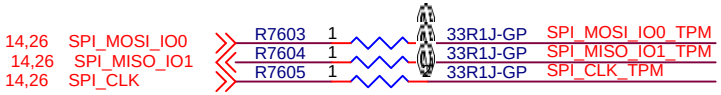
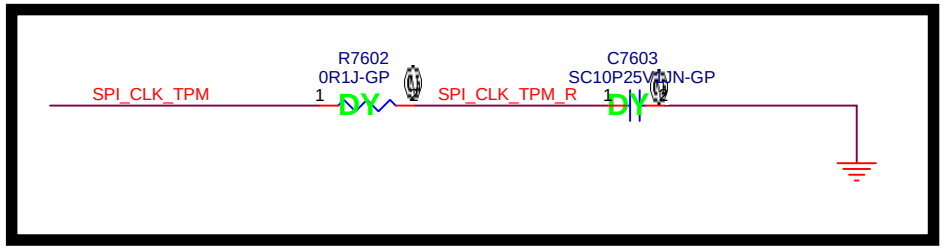
TPM



U7601	Vendor P/N	Lenovo P/N	Wistron P/N
Infineon	SLB9670VQ2.0 FW7.63.3353.00	SL80R44425	071.09670.0I03
ST Micro	ST33HTPH2E32AHB4	SL80L81401	071.33232.0G03





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Title: DISCRETE TPM 2.0		
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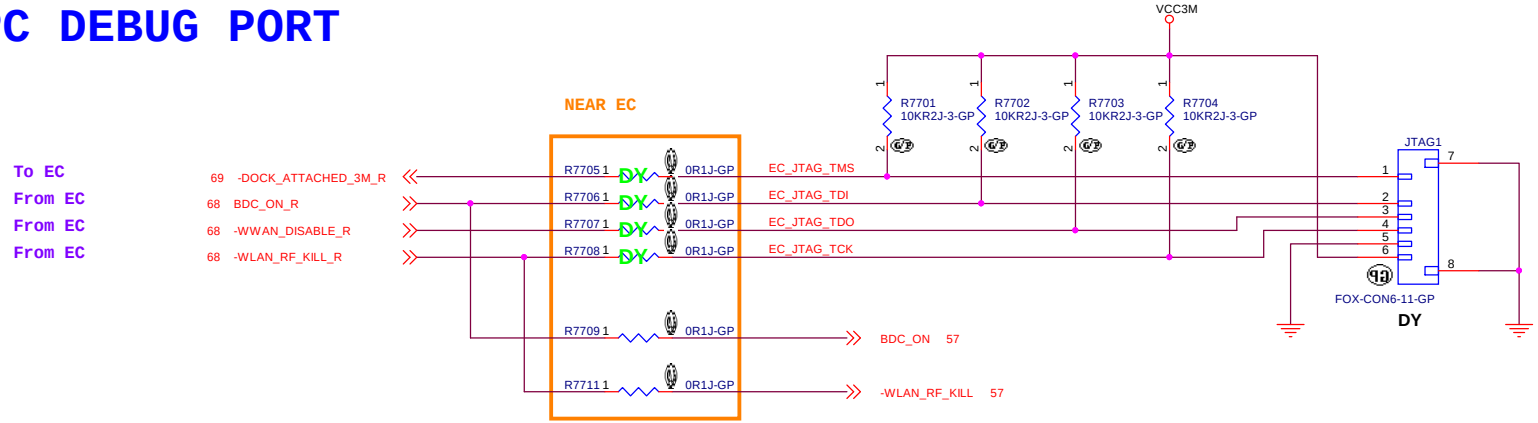
LPC DEBUG PORT



Lenovo Debug Tool I/F

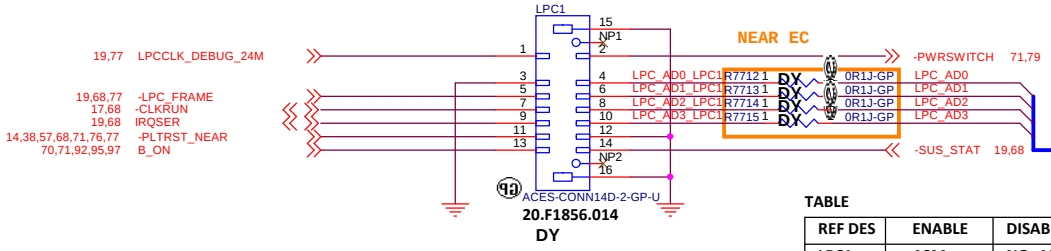


TABLE		
REF DES	ENABLE	DISABLE
LPC1	ASM	NO_ASM
R7712	ASM	NO_ASM
R7713	ASM	NO_ASM
R7714	ASM	NO_ASM
R7715	ASM	NO_ASM

LOGIC

Wistron LPC for Debug Card CONN

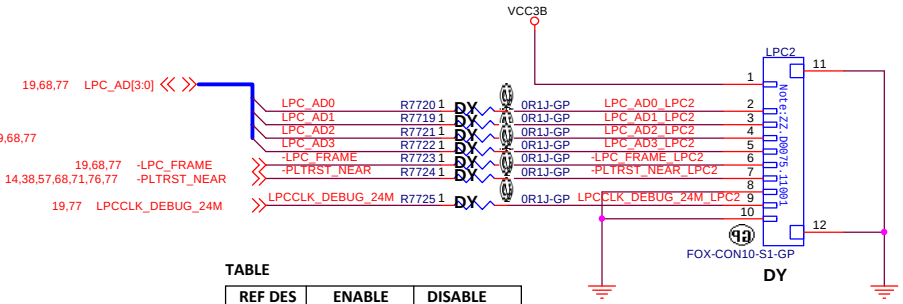
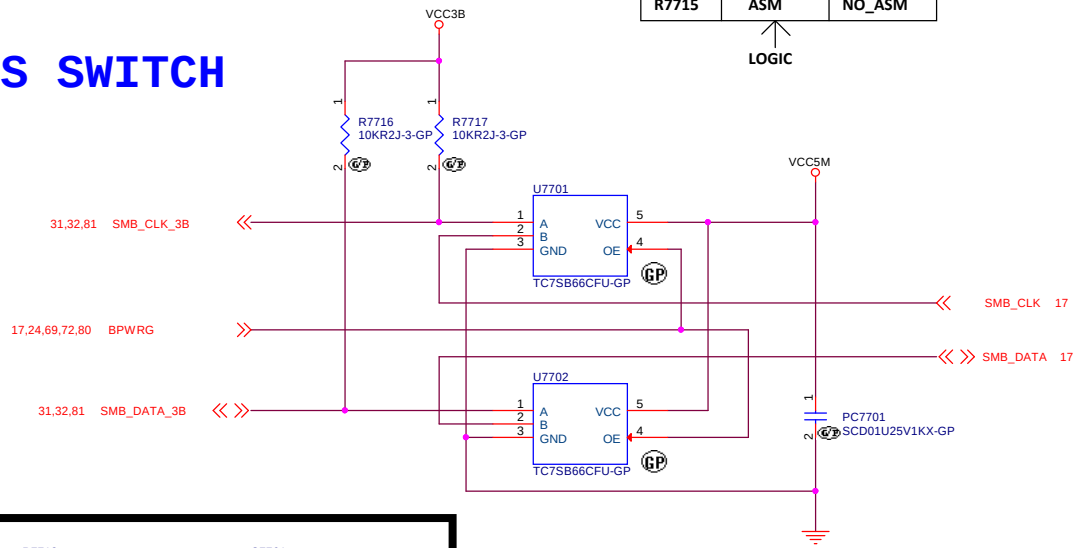


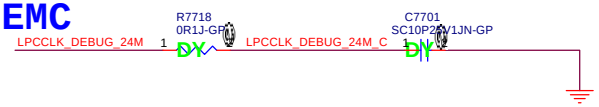
TABLE		
REF DES	ENABLE	DISABLE
R7719	ASM	NO_ASM
R7720	ASM	NO_ASM
R7721	ASM	NO_ASM
R7722	ASM	NO_ASM
R7723	ASM	NO_ASM
R7724	ASM	NO_ASM
R7725	ASM	NO_ASM

LOGIC

SMBUS SWITCH



EMC



ULT

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Title: SMBUS SWITCH/LPC DEBUG PORT

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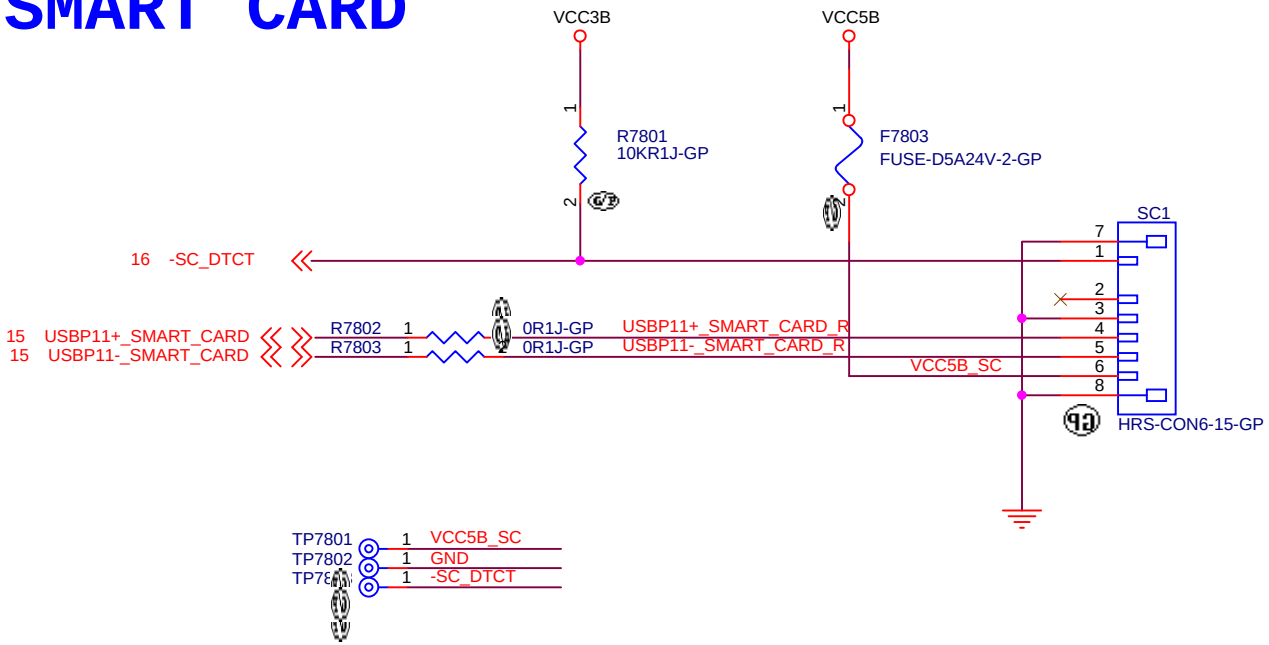
SMART CARD



ULT

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Title: ***SMART CARD***		
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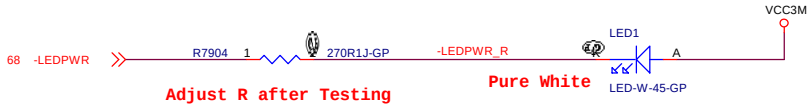
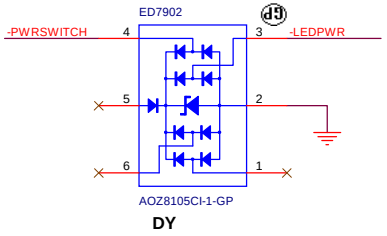
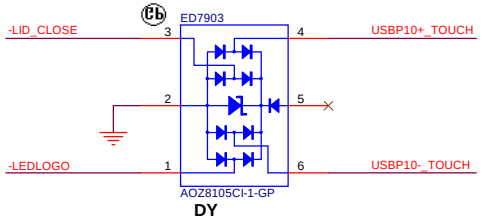
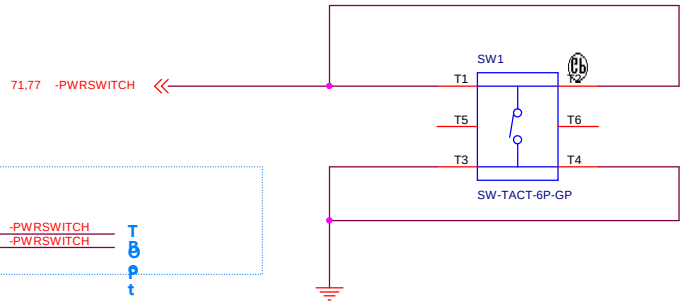
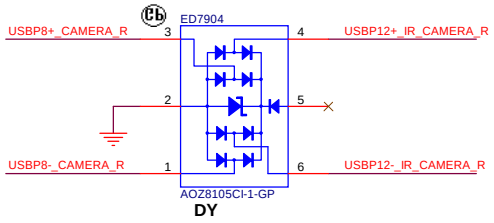
PWR BUTTON



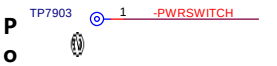




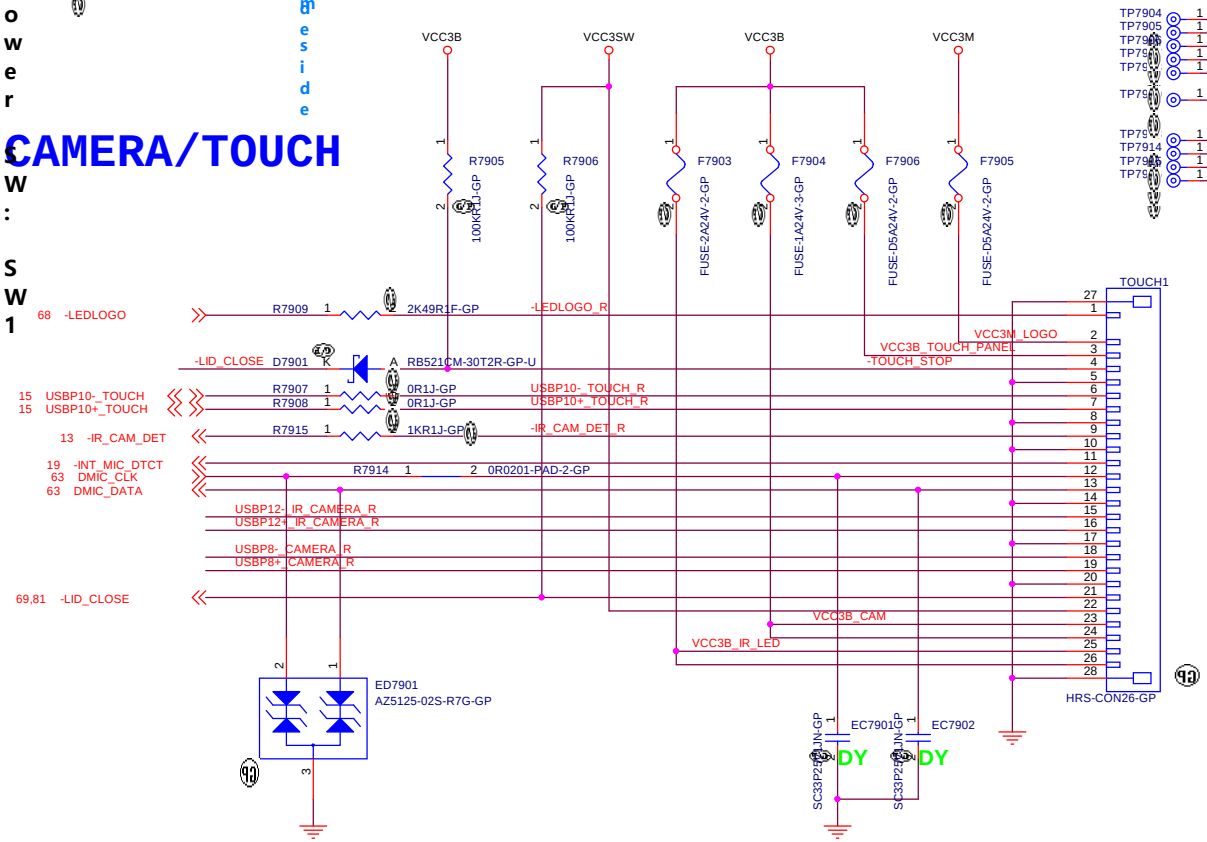


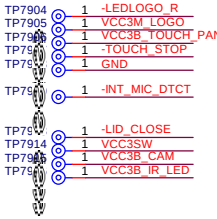


Near Power SW: Test point



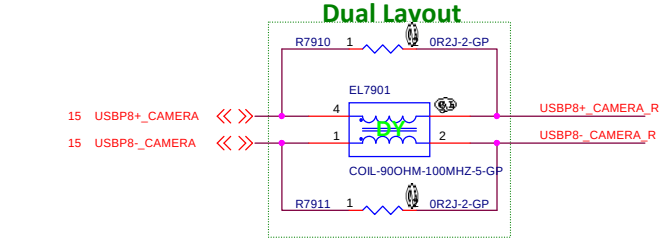
CAMERA/TOUCH





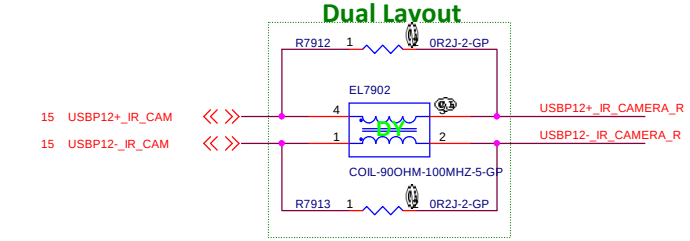
Near CAM1 CONN

Dual Layout



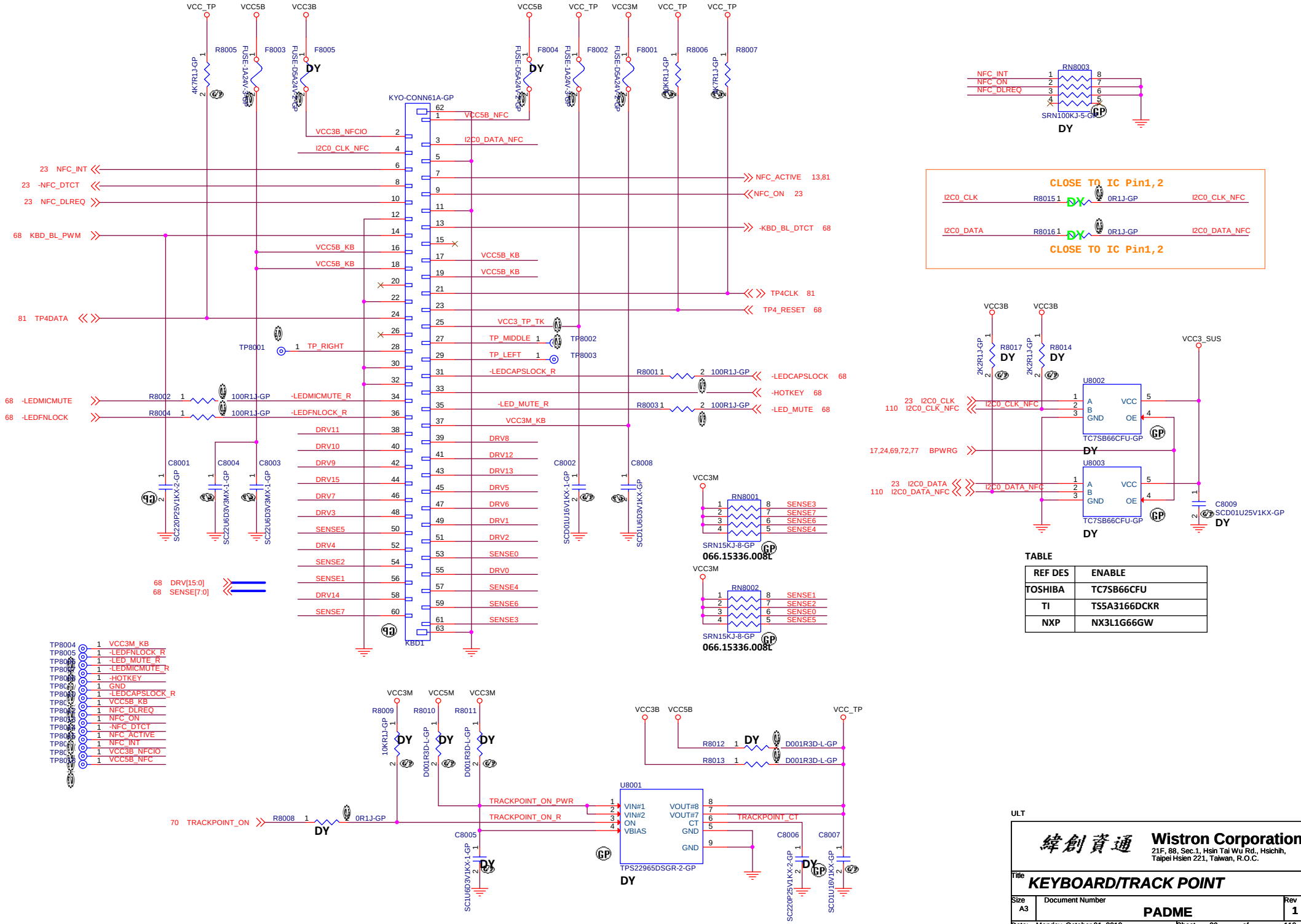
Near CAM1 CONN

Dual Layout

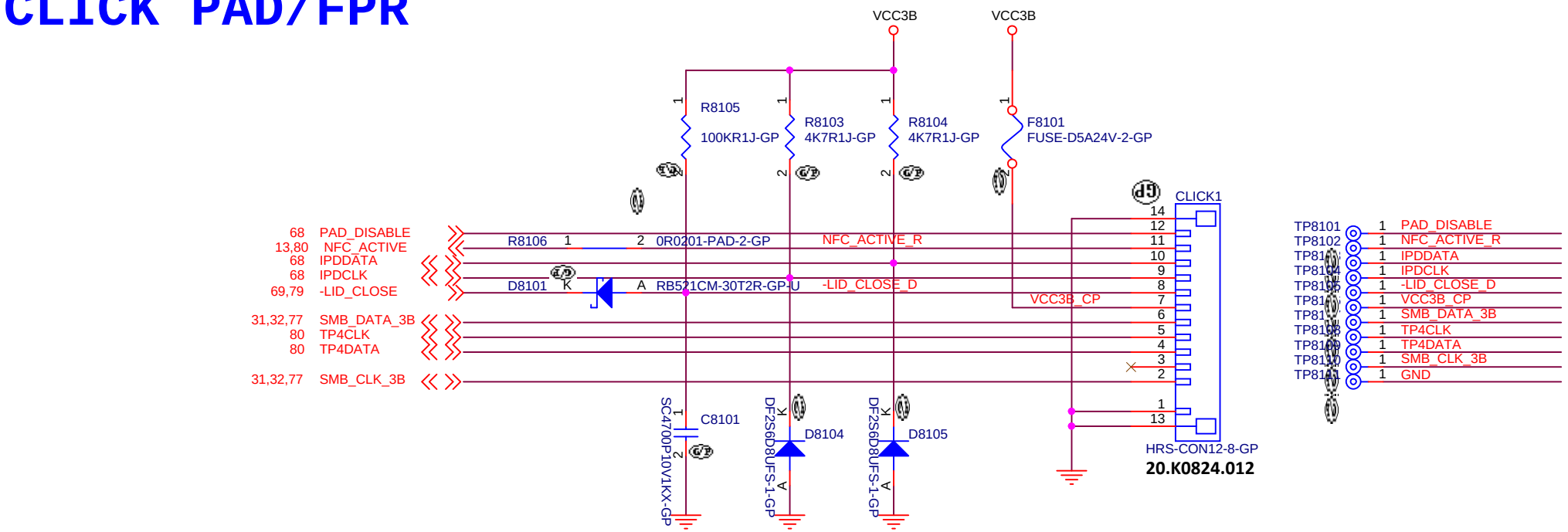


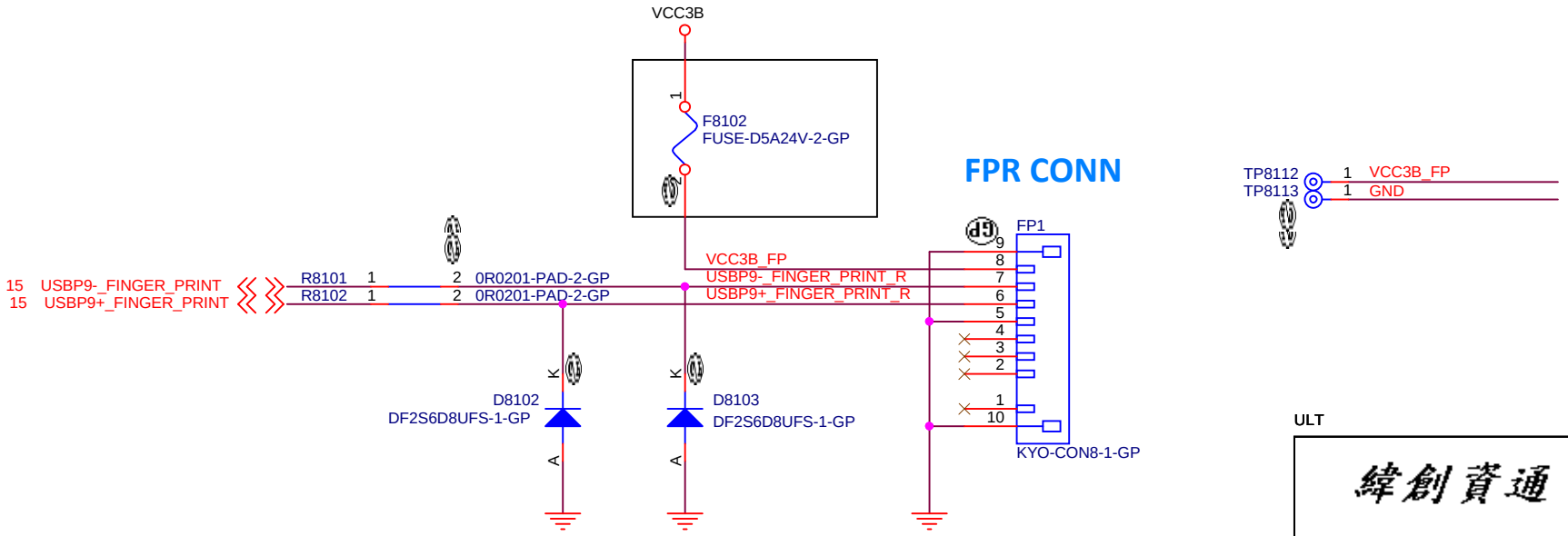
ULT

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CAMERA/TOUCH/PWR BUTTON		
Size: A3	Document Number: PADME	Rev: 1
Date: Monday, October 01, 2018	Sheet 79 of 110	


KYO-CONN61A-GP
KBD1
VCC_TP
VCC5B
VCC3B
VCC3M
R8005
R8003
R8004
R8002
R8001
R8006
R8007
F8003
F8005
F8004
F8002
F8001
VCC5B_NFC
VCC3B_NFCIO
I2C0_CLK_NFC
I2C0_DATA_NFC
NFC_INT
-NFC_DTCT
NFC_DLREQ
NFC_ACTIVE
NFC_ON
-KBD_BL_DTCT
KBD_BL_PWM
VCC5B_KB
TP4CLK
TP4DATA
TP4_RESET
VCC3_TP_TK
TP_MIDDLE
TP_LEFT
TP_RIGHT
TP8001
TP8002
TP8003
-LEDCAPSLOCK_R
-HOTKEY
-LED_MUTE_R
-LED_MUTE
-LEDMICMUTE
-LEDFNLOCK
-LEDMICMUTE_R
-LEDFNLOCK_R
VCC3M_KB
DRV[15:0]
SENSE[7:0]
C8001
C8004
C8003
C8002
C8008
RN8001
RN8002
SRN15KJ-8-GP
066.15336.008L
RN8003
SRN100KJ-5-GP
CLOSE TO IC Pin1,2
I2C0_CLK
I2C0_DATA
R8015
R8016
0R1J-GP
I2C0_CLK_NFC
I2C0_DATA_NFC
U8002
U8003
TC7SB66CFU-GP
VCC3_SUS
BPWRG
C8009
SCD01U25V1KX-GP
TABLE
REF DES
ENABLE
TOSHIBA
TC7SB66CFU
TI
TS5A3166DCKR
NXP
NX3L1G66GW
TP8004
TP8005
TP8006
TP8007
TP8008
TP8009
TP8010
TP8011
TP8012
TP8013
TP8014
TP8015
TP8016
GND
-HOTKEY
-NFC_DTCT
-NFC_ACTIVE
VCC5B_NFC
VCC5M
R8009
R8010
R8011
R8012
R8013
R8008
TRACKPOINT_ON
TRACKPOINT_ON_PWR
TRACKPOINT_ON_R
TRACKPOINT_CT
U8001
TPS22965DSGR-2-GP
C8005
C8006
C8007
D001R3D-L-GP
ULT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KEYBOARD/TRACK POINT
Size
A3
Document Number
PADME
Rev
1
Date: Monday, October 01, 2018
Sheet 80 of 110

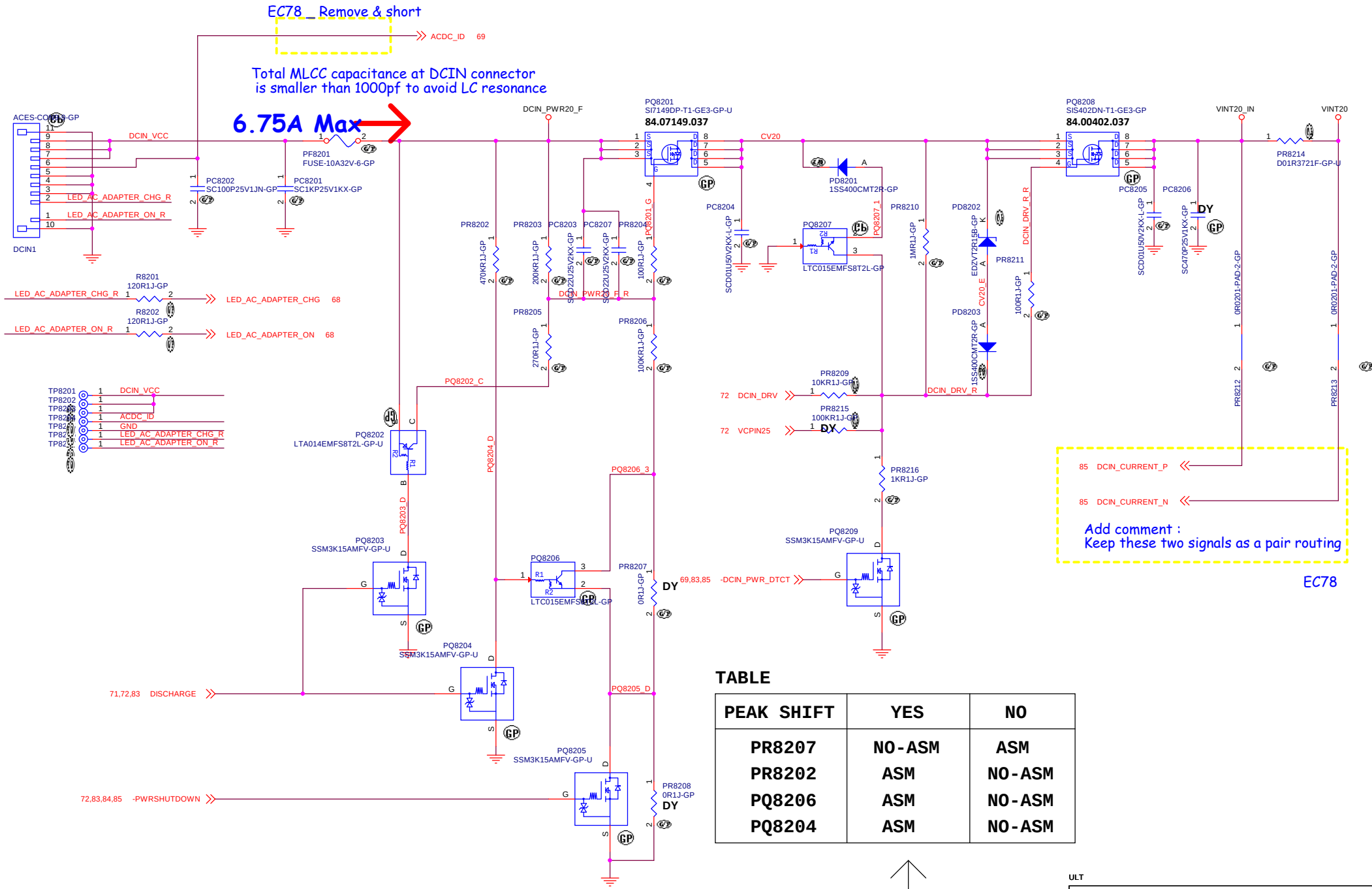
CLICK PAD/FPR





ULT

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CLICK PAD/FPR***	
Size A4	Document Number **PADME**	Rev 1
Date: Monday, October 01, 2018	Sheet 81 of 110	



TABLE

PEAK SHIFT	YES	NO
PR8207	NO-ASM	ASM
PR8202	ASM	NO-ASM
PQ8206	ASM	NO-ASM
PQ8204	ASM	NO-ASM

LOGIC

ULT

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC-IN		
Size: A3	Document Number: PADME	Rev: 1
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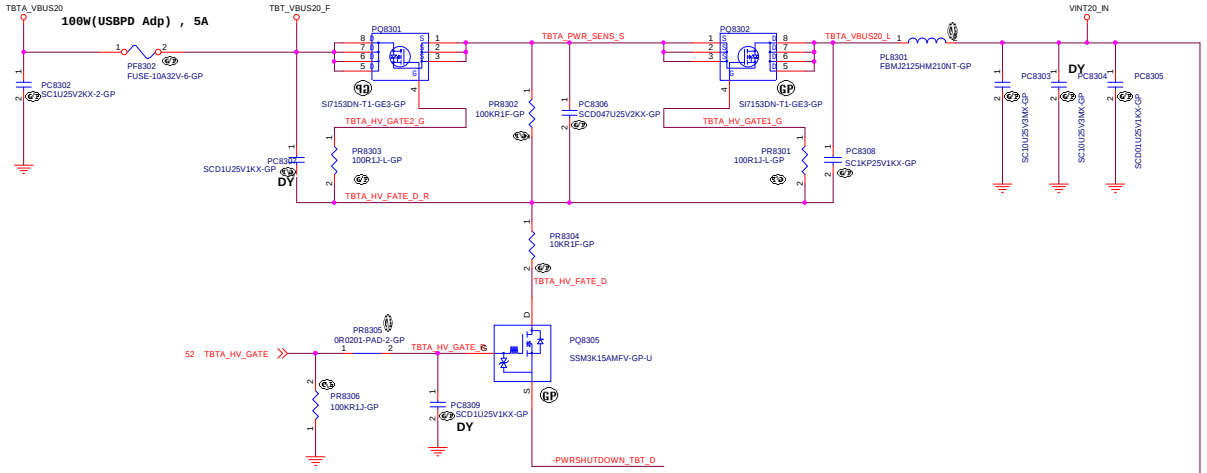
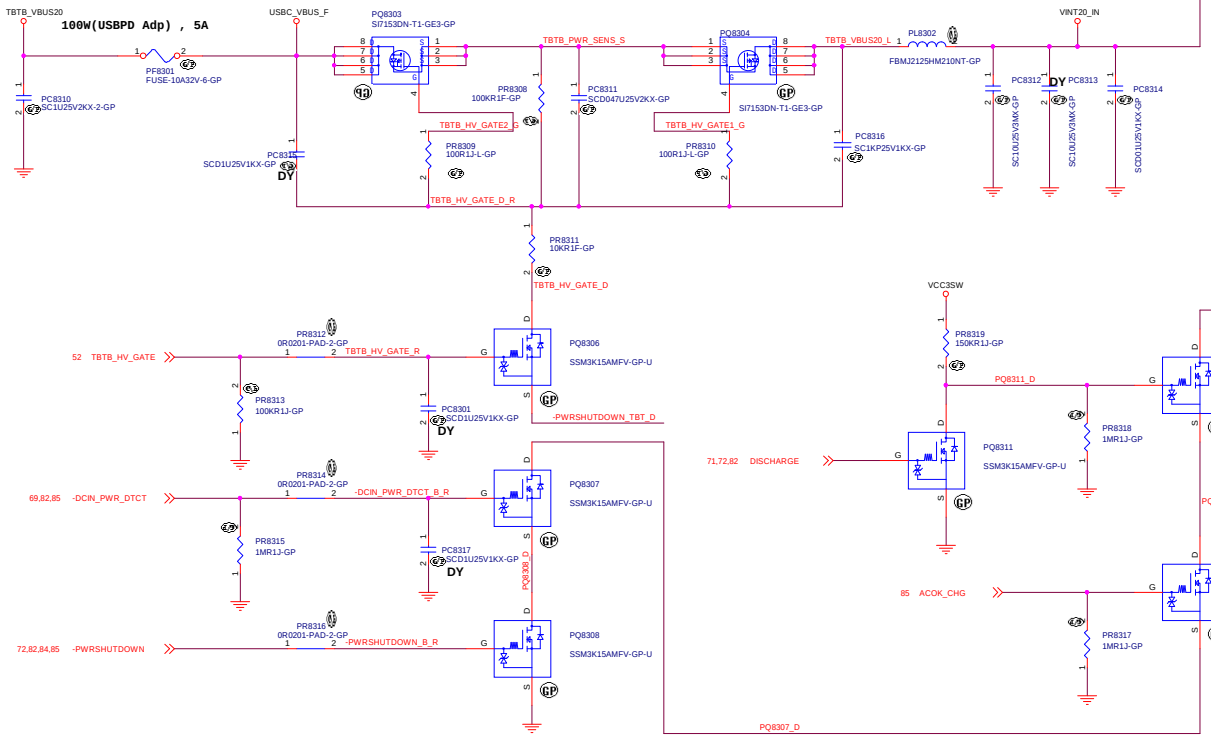
	PQ8301, PQ8302, PQ8303, PQ8304
1st	SI7153DN 084.07153.0037
2nd	TPCC8104 084.08104.B37

	PL8301, PL8302
1st	FBMJ2125HM210NT 068.00046.0061
2nd	





ULT

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: DC-IN		
Size: A2	Document Number: PADME	Rev: 1
Date: Monday, October 01, 2018	Sheet 83 of 110	

RV3_PDV_EC029
RV3_PDV_EC030
RV3_PDV_EC085

MAIN BAT CONN

Max Current = 10 (A)

WIDE PATTERN

10 m ohm 1% 1W 3720

Add comment :
Keep these two signals as a pair routing

EC77

EC77 move circuit

EC77 remove circuit

ULT

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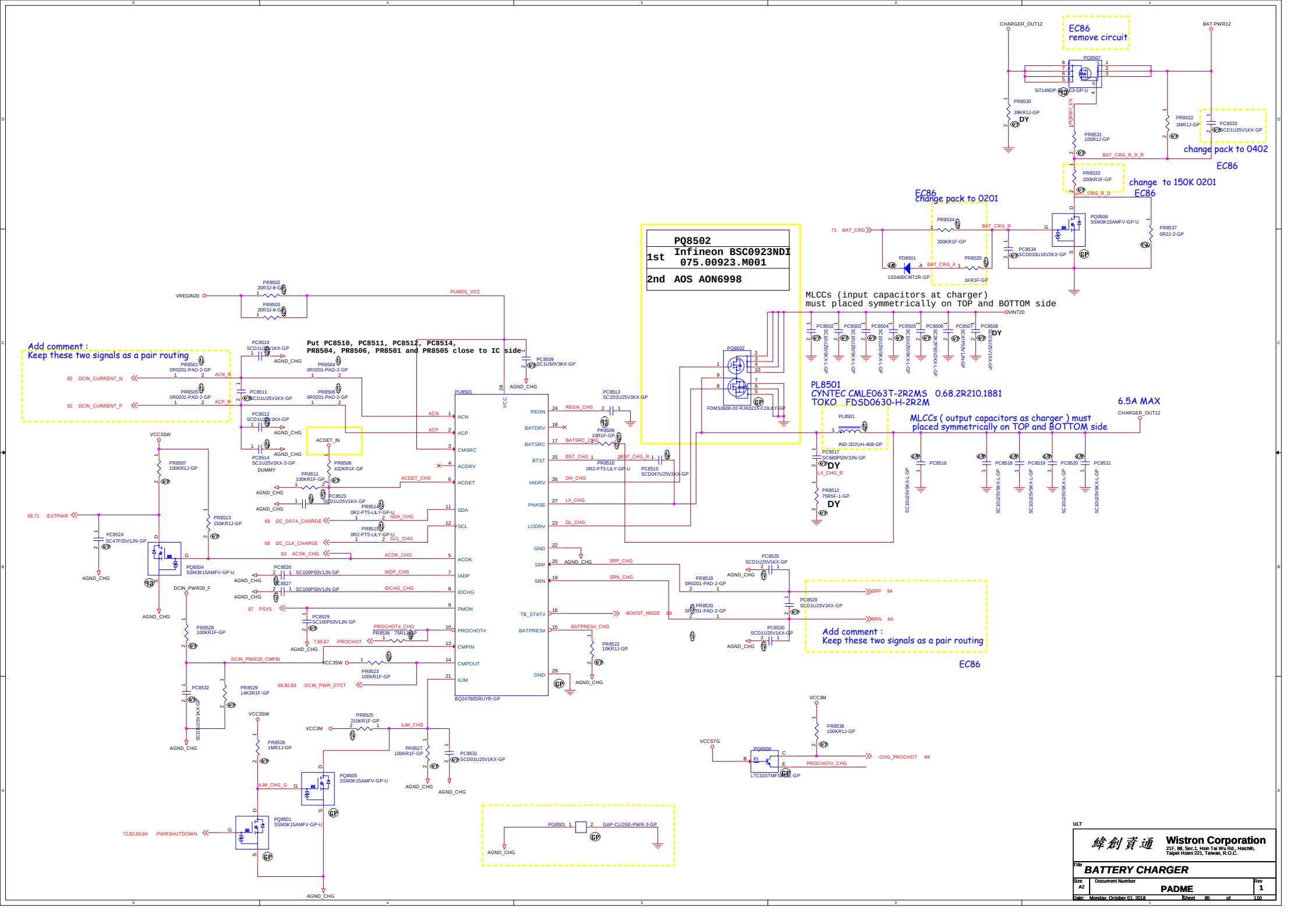
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATTERY INPUT

Size	Document Number	Rev
C	PADME	1

Date: Monday, October 01, 2018 Sheet 84 of 110


EC86
remove circuit
CHARGER_OUT12
BAT-PWR12
PQ8507
SI7149DP-T1-E3-GP-U
PR8530
39KR1J-GP
DY
PQ8507_EN
PR8531
100R1J-GP
PR8532
1MR1J-GP
PC8533
SCD1U25V1KX-GP
change pack to 0402
EC86
BAT_CRG_R_D_R
PR8533
200KR1F-GP
change to 150K 0201
EC86
EC86
change pack to 0201
PR8534
200KR1F-GP
BAT_CRG_R
PQ8506
SSM3K15AMFV-GP-U
PR8537
0R2J-2-GP
PC8534
SCD033U16V2KX-GP
PD8501
1SS400CMT2R-GP
BAT_CRG_A
PR8535
1KR1F-GP
71 BAT_CRG
PQ8502
1st Infineon BSC0923NDI 075.00923.M001
2nd AOS AON6998
MLCCs (input capacitors at charger)
must placed symmetrically on TOP and BOTTOM side
VINT20
PC8502
PC8503
PC8504
PC8505
PC8506
PC8507
PC8508
DY
FDMS3600-02-RJK0215-COLAY-GP
PL8501
CYNTEC CMLE063T-2R2MS 0.68.2R210.1881
TOKO FDSD0630-H-2R2M
6.5A MAX
CHARGER_OUT12
MLCCs (output capacitors as charger) must
placed symmetrically on TOP and BOTTOM side
PL8501
IND-2D2UH-408-GP
PC8517
SC680P50V3JN-GP
DY
LX_CHG_R
PR8512
75R5F-1-GP
DY
PC8516
PC8518
PC8519
PC8520
PC8521
Add comment :
Keep these two signals as a pair routing
EC86
PR8502
20R3J-8-GP
PR8503
20R3J-8-GP
VREGIN20
PU8501_VCC
Add comment :
Keep these two signals as a pair routing
82 DCIN_CURRENT_N
82 DCIN_CURRENT_P
PR8501
0R0201-PAD-2-GP
PR8505
0R0201-PAD-2-GP
ACN_R
ACP_R
Put PC8510, PC8511, PC8512, PC8514,
PR8504, PR8506, PR8501 and PR8505 close to IC side
PC8510
SCD1U25V1KX-GP
PC8511
SCD1U25V1KX-GP
PC8512
SCD1U25V1KX-GP
PC8514
SC1U25V2KX-2-GP
DUMMY
PR8504
0R0201-PAD-2-GP
PR8506
0R0201-PAD-2-GP
ACDET_IN
PR8508
432KR1F-GP
PR8511
100KR1F-GP
PC8523
SCD1U25V1KX-GP
PC8509
SC1U50V3KX-GP
AGND_CHG
PU8501
BQ24780SRUYR-GP
ACN
ACP
CMSRC
ACDRV
ACDET
SDA
SCL
ACOK
IADP
IDCHG
PMON
PROCHOT#
CMPIN
CMPOUT
ILIM
REGN
BATDRV
BATSRC
BTST
HIDRV
PHASE
LODRV
GND
SRP
SRN
TB_STAT#
BATPRES#
GND
VCC
PC8513
SC2D2U25V3KX-GP
REGN_CHG
PR8509
10R1F-GP
BST_CHG
PR8510
0R2-PT5-LILY-GP-U
2BST_CHG_R
PC8515
SCD047U25V2KX-GP
DH_CHG
LX_CHG
DL_CHG
ACDET_CHG
ACOK_CHG
IADP_CHG
IDCHG_CHG
PROCHOT#_CHG
BATPRES#_CHG
SRP_CHG
SRN_CHG
-BOOST_MODE 69
PR8522
10KR1J-GP
PR8514
0R2-PT5-LILY-GP-U
SDA_CHG
PR8515
0R2-PT5-LILY-GP-U
SCL_CHG
68 I2C_DATA_CHARGE
68 I2C_CLK_CHARGE
83 ACOK_CHG
87 PSYS
7,69,87 -PROCHOT
PR8536
75R1J-GP
PC8525
SCD1U25V1KX-GP
PR8518
0R0201-PAD-2-GP
PR8520
0R0201-PAD-2-GP
PC8528
SCD1U25V1KX-GP
PC8530
SCD1U25V1KX-GP
SRP 84
SRN 84
VCC3M
PR8538
100KR1J-GP
VCCSTG
PQ8508
LTC015TMFSM3-GP
-CHG_PROCHOT 68
PROCHOT#_CHG
69 -EXTPWR
PR8507
100KR1J-GP
PR8513
150KR1J-GP
PC8524
SC47P25V1JN-GP
PQ8504
SSM3K15AMFV-GP-U
DCIN_PWR20_F
PR8528
100KR1F-GP
PC8532
SCD1U25V1KX-GP
PR8529
14K3R1F-GP
69,82,83 -DCIN_PWR_DTCT
DCIN_PWR20_CMPIN
PR8523
100KR1F-GP
PC8526
SC100P50V1JN-GP
PC8527
SC100P50V1JN-GP
PC8529
SC100P50V1JN-GP
PR8536
75R1J-GP
VCC3SW
PR8526
1MR1J-GP
PR8525
210KR1F-GP
PR8527
100KR1F-GP
PC8531
SCD01U25V1KX-GP
ILIM_CHG
ILIM_CHG_G
PQ8505
SSM3K15AMFV-GP-U
PQ8501
SSM3K15AMFV-GP-U
72,82,83,84 -PWRSHUTDOWN
PG8501
GAP-CLOSE-PWR-3-GP
ULT
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BATTERY CHARGER
Size A2
Document Number
PADME
Rev 1
Date: Monday, October 01, 2018
Sheet 85 of 110

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

Add comment :
MLCCs (Input capacitiors at charger)
must placed symmetrically on TOP and BOTTOM side

	PQ8601
1st	Infineon BSC0923NDI 75.00923.073
2nd	AOS AON6998

Dual-N standard symbol to colay

FDMS3600-02-RJK0215-COLAY-GP

12A MAX

Table PL8601
TDK SPM6530T-1R0M120 68.1R01A.11A
CYNTEC CMLE063T-1R0MS 068.R1010.1081

IND-1UH-238-GP

	PT8601 PT8602 PT8603
1st	Panasonic 6TPE220MAPB 77.22271.39L
2nd	KEMET T520B227M006ATE025 077.C2271.0041
3rd	TOKIN PSLB20J227M25LQ

PR8621	VCC5M
154K Ohm	5.08 V
158K Ohm	5.16 V
162K Ohm	5.24 V

Add comment :
Current Limit1
25.1A (17.5A - 38.1A)

Add comment :
Current Limit2
23.7A (16.9A - 35A)

TPS51285B-1RUKR-GP

keep more than 2.0mm height for
if acoustic noise suppression MLCC use

	PQ8602
1st	Infineon BSC0923NDI 75.00923.073
2nd	AOS AON6998

Add comment :
MLCCs (Input capacitiors at charger)
must placed symmetrically on TOP and BOTTOM side

Dual-N standard symbol to colay

FDMS3600-02-RJK0215-COLAY-GP

12A MAX

Table PL8602
TDK SPM6530T-1R0M120 68.1R01A.11A
CYNTEC CMLE063T-1R0MS 068.R1010.1081

IND-1UH-238-GP

	PT8604 PT8605 PT8606
1st	Panasonic 6TPE220MAPB 77.22271.39L
2nd	KEMET T520B227M006ATE025 077.C2271.0041
3rd	TOKIN PSLB20J227M25LQ

PR8622	VCC3M
130K Ohm	3.30 V
133K Ohm	3.33 V
137K Ohm	3.37 V

PG8601 GAP-CLOSE-PWR-3-GP

TP8601 VCC5M
TP8602 VCC3M

ULT

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCC5M/VCC3M

Size: Custom | Document Number: PADME | Rev: 1

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OFFPAGE

VCCSA SENSE

VCCCPUCORE SENSE

VCCGFXCORE_I SENSE

Close to VCCSA Choke

Close to Vcore Choke

EC87

VCCCORE Feedback

VBOOT Setting For Core/GT
24.9K ohm -> 0V
169K ohm -> 1.05V

Close to GFX_I Choke

Close to VCORE Dr.MOS

Close to GFX_I Dr.MOS

EC88
Add : PWR GAP
change GND symbol on this page ALL GND

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC IMVP8

Size: Custom | Document Number: PADME | Rev: 1

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TABLE for PT8801~PT8808

NEC TOKIN	PSGB20E337M9 (80.3371V.A2L)
Panasonic	ETPE330MA9L (077.23371.M001)
KEMET	T520B337M2R5ATE009 (077.C3371.0051)

H62-45W
IMAX 128 A / TDC 80 A / OCP 135 A

VCCCPUCORE

PT8802 PT8803 PT8804 PT8805 PT8806 PT8807 PT8808 PT8801 — ST330U2D5VBM-1-GP (DY)

330uF 6 Pcs + 2 Pcs no mount

PC8828 PC8829 PC8817 PC8830 PC8818 PC8819 PC8831 PC8820 — SC47U4V5MX-2-GP

47uF 8 Pcs

PC8835 PC8836 PC8837 PC8834 PC8839 PC8840 PC8841 PC8838 — SC22U6D3V3MX-1-GP

PC8842 PC8843 PC8844 PC8845 — SC22U6D3V3MX-1-GP

22uF 12 Pcs

PC8846 PC8847 PC8848 PC8849 PC8853 PC8850 PC8851 PC8852 — SC10U6D3V2MX-GP-U

PC8854 PC8855 PC8856 PC8863 PC8857 PC8864 PC8801 PC8858 — SC10U6D3V2MX-GP-U

PC8870 PC8871 PC8872 PC8873 PC8874 PC8875 PC8876 PC8877 — SC10U6D3V2MX-GP-U

PC8878 PC8879 PC8880 PC8881 — SC10U6D3V2MX-GP-U

10uF 28 Pcs

VCC5M

PWR_CORE_VCCA — PR8804 2R2J-2-GP

PR8803 3D9R3-GP — PWR_CORE_BOOT_PH1

PC8803 SCD22U25V3KX-GP

PWR_CORE_BOOT_A_PH1 — PWR_CORE_PHASED_PH1

PC8805 SC1U10V2KX-GP

PC8806 SQ1U10V2KX-GP

VINT20

Max Current = 3.50(A)

VSYS_CPUCORE_PH1

PR8801 0R0816-PAD-GP-U

PR8802 0R0816-PAD-GP-U

PC8821 PC8832 PC8833 PC8822 PC8823 PC8824 PC8825 PC8826 PC8827 — SC22U25V3KX-5-GP

SC1U10V1KX-1-GP

SC2KP25V1JN-1GP (DY)

SC68P50V2JN-1GP

PU8802 NCP302045MNTWG-GP

PHASE BOOT VCC VCCD PWM DISB# THWN SMOD# VIN PGND VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22 VSW#23 VSW#24 VSW#25 VSW#26 AGND CGND GL#27 GL#33 NC#6

PU8802_GL

PWR_CORE_DISB#_PH1 — PR8805 0R0201-PAD-2-GP — PWR_VCCCORE_PWM1 87 — DRVON 87,88,89,90,91

TABLE PL8801

TOKIN	MPCH0740LR15D (68.R1510.10F)
CYNTEC	CMLE064T-R15MS0R667

PL8801 — IND-D15UH-9-GP

PR8806 0R0201-PAD-2-GP

PR8807 0R0201-PAD-2-GP

CSN1_4PH_A 87

SW1_4PH_A 87

PWR_CORE_PH1

PC8808 SC680P50V2KX-2GP (DY)

PWR_CORE_SNB_PH1

PR8808 2D2R3F-3-GP (DY)

TABLE PR8808 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

MLCCs must be placed symmetrically on Top and Bottom.

VCC5M

PWR_CORE_VCCB — PR8814 2R2J-2-GP

PR8813 3D9R3-GP — PWR_CORE_BOOT_PH2

PC8813 SCD22U25V3KX-GP

PWR_CORE_BOOT_A_PH2 — PWR_CORE_PHASED_PH2

PC8815 SC1U10V2KX-GP

PC8816 SC1U10V2KX-GP

VINT20

Max Current = 3.50(A)

VSYS_CPUCORE_PH2

PR8811 0R0816-PAD-GP-U

PR8812 0R0816-PAD-GP-U

PC8865 PC8866 PC8867 PC8868 PC8859 PC8860 PC8869 PC8861 PC8862 — SC22U25V3KX-5-GP

SC1U10V1KX-1-GP

SC2KP25V1JN-1GP (DY)

SC68P50V2JN-1GP

PU8801 NCP302045MNTWG-GP

PHASE BOOT VCC VCCD PWM DISB# THWN SMOD# VIN PGND VSW#16 VSW#17 VSW#18 VSW#19 VSW#20 VSW#21 VSW#22 VSW#23 VSW#24 VSW#25 VSW#26 AGND CGND GL#27 GL#33 NC#6

PU8801_GL

PWR_CORE_DISB#_PH2 — PR8815 0R0201-PAD-2-GP — PWR_VCCCORE_PWM2 87 — DRVON 87,88,89,90,91

TABLE PL8802

TOKIN	MPCH0740LR15D (68.R1510.10F)
CYNTEC	CMLE064T-R15MS0R667

PL8802 — IND-D15UH-9-GP

PR8816 0R0201-PAD-2-GP

PR8817 0R0201-PAD-2-GP

CSN2_4PH_A 87

SW2_4PH_A 87

PWR_CORE_PH2

PC8888 SC680P50V2KX-2GP (DY)

PWR_CORE_SNB_PH2

PR8818 2D2R3F-3-GP (DY)

TABLE PR8818 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

MLCCs must be placed symmetrically on Top and Bottom.

ULT

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC/DC VCCCPUCORE (1/2)

Size	Document Number	Rev
C	PADME	1

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H62-45W
IMAX 128 A / TDC 80 A / OCP 135 A

1uF 63 Pcs

Max Current = 3.50(A)

MLCCs must be placed
symmetrically on Top and Bottom.

TABLE PL8901

TOKIN MPCH0740LR15D (68.R1510.10F)
CYNTEC , CMLE064T-R15MS0R667

TABLE PR8906 0603 size

Rohm, ESR03EZPJ2R2
Pana, ERJPA3J2R2V
YDS, RN73S2CL-2R20-F

Max Current = 3.50(A)

MLCCs must be placed
symmetrically on Top and Bottom.

TABLE PL8902

TOKIN MPCH0740LR15D (68.R1510.10F)
CYNTEC , CMLE064T-R15MS0R667

TABLE PR8916 0603 size

Rohm, ESR03EZPJ2R2
Pana, ERJPA3J2R2V
YDS, RN73S2CL-2R20-F

This circuit is for Hexa core.
Please refer to the table in next page.

ULT

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Title: DC/DC VCCCPUCORE (2/2)

Size: C | Document Number: PADME | Rev: 1

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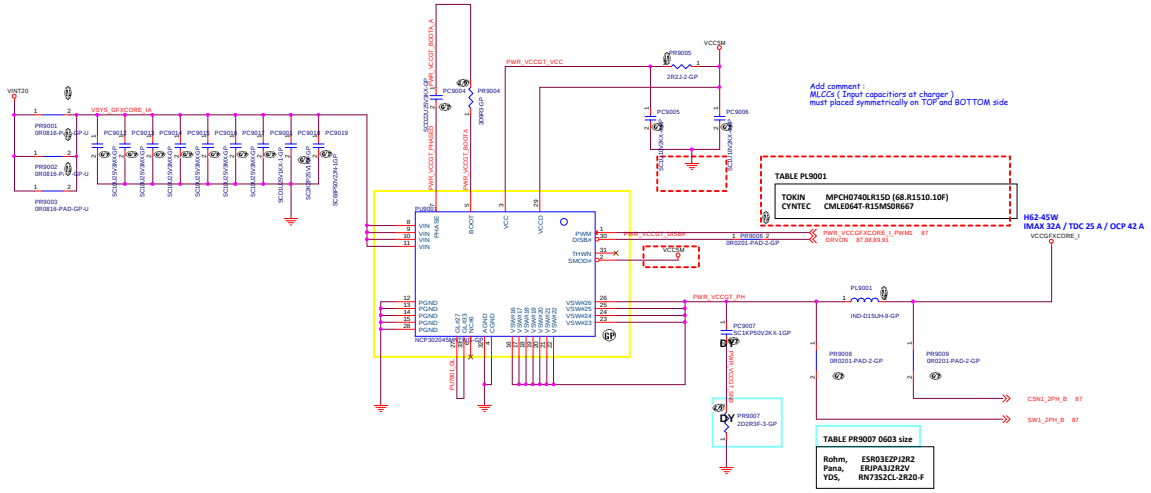
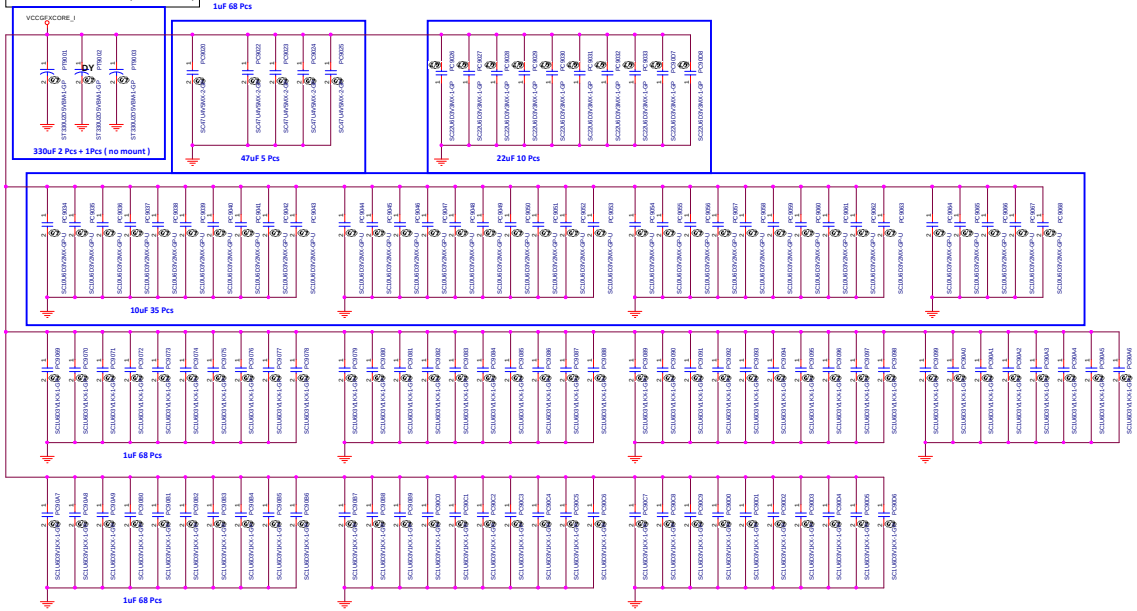


TABLE for PT9001, PT9002, PT9003

NEC TOKIN PSGB20E337M9 (80.3371V.A2L)
Panasonic ETPE330MA9L (No Wistron P/N)
KEMET T520B337M2R5ATE009 (077.C3371.0051)

330uF 2 Pcs + 1Pcs (no mount)
47uF 6 Pcs
22uF 8 Pcs
10uF 35 Pcs
1uF 68 Pcs



TABLE

Connection	Component Name	CPU-H Hexa	CPU-H Quad	Unit	memo
PWR_VCCCORE_ILIM to PWR_VCCCORE_CSCOMP	PR8749	30.1	20.0	Kohm	128Ax1.3 v.s 86Ax1.3
PWR_VCCCORE_PWM1 to AGND_81215	PR8775	100	68.1	Kohm	128A v.s 86A
SW4_4PH_A to PWR_VCCCORE_CSSUM	PR8764	80.6	No asm	Kohm	4phase v.s 3phase
CSN4_4PH_A to PWR_VCCCORE_CSREF	PR8770	10	No asm	ohm	4phase v.s 3phase
SW4_4PH_A to PWR_VCCCORE_CSP4	PR8782	4.42	No asm	Kohm	4phase v.s 3phase
PWR_VCCCORE_CSP4 to PWR_VCCCORE_CSREF	PC8736	0.047	No asm	uF	4phase v.s 3phase
PWR_VCCCORE_CSP4 to VCCSM	PR8798	No asm	1	Kohm	4phase v.s 3phase
PWR_VCCCORE_PWM4	PU8902	asm	No asm	____	4phase v.s 3phase
VCCSM to PWR_CORE_VCCD	PR8914	2.2	No asm	ohm	4phase v.s 3phase
PWR-CORE_VCCD to GND	PC8911	1	No asm	uF	4phase v.s 3phase
VCCSM to AGND_81215	PC8912	1	No asm	uF	4phase v.s 3phase
PWR_CORE_BOOT_PH4 to PWR_CORE_BOOT_A_PH4	PR8913	3.9	No asm	ohm	4phase v.s 3phase
PWR_CORE_BOOT_A_PH4 to PWR_CORE_PHASED_PH	PC8913	0.22	No asm	uF	4phase v.s 3phase
VINT20 to VSYS_CPUCORE_PH4	PR8911	10	No asm	mohm	4phase v.s 3phase
VINT20 to VSYS_CPUCORE_PH4	PR8912	10	No asm	mohm	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8993	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8994	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8995	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8996	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8997	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8998	10	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8990	0.1	No asm	uF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8991	2200	No asm	pF	4phase v.s 3phase
VSYS_CPUCORE_PH4 to GND	PC8992	2200	No asm	pF	4phase v.s 3phase
PWR_CORE_DISB#_PH4 to DRVON	PR8915	0	No asm	ohm	4phase v.s 3phase
VCCCPUCORE to PWR_CORE_PH4	PL8902	0.15	No asm	uH	4phase v.s 3phase
PWR_CORE_PH4 to SW4_4PH_A	PR8917	0	No asm	ohm	4phase v.s 3phase
VCCCPUCORE to CSN4_4PH_A	PR8918	0	No asm	ohm	4phase v.s 3phase

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Title: DC/DC VCCGFXCORE_I(NCP302045)

Size	Document Number	Rev
D	PADME	1

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MLCCs must be placed
symmetrically on Top and Bottom.

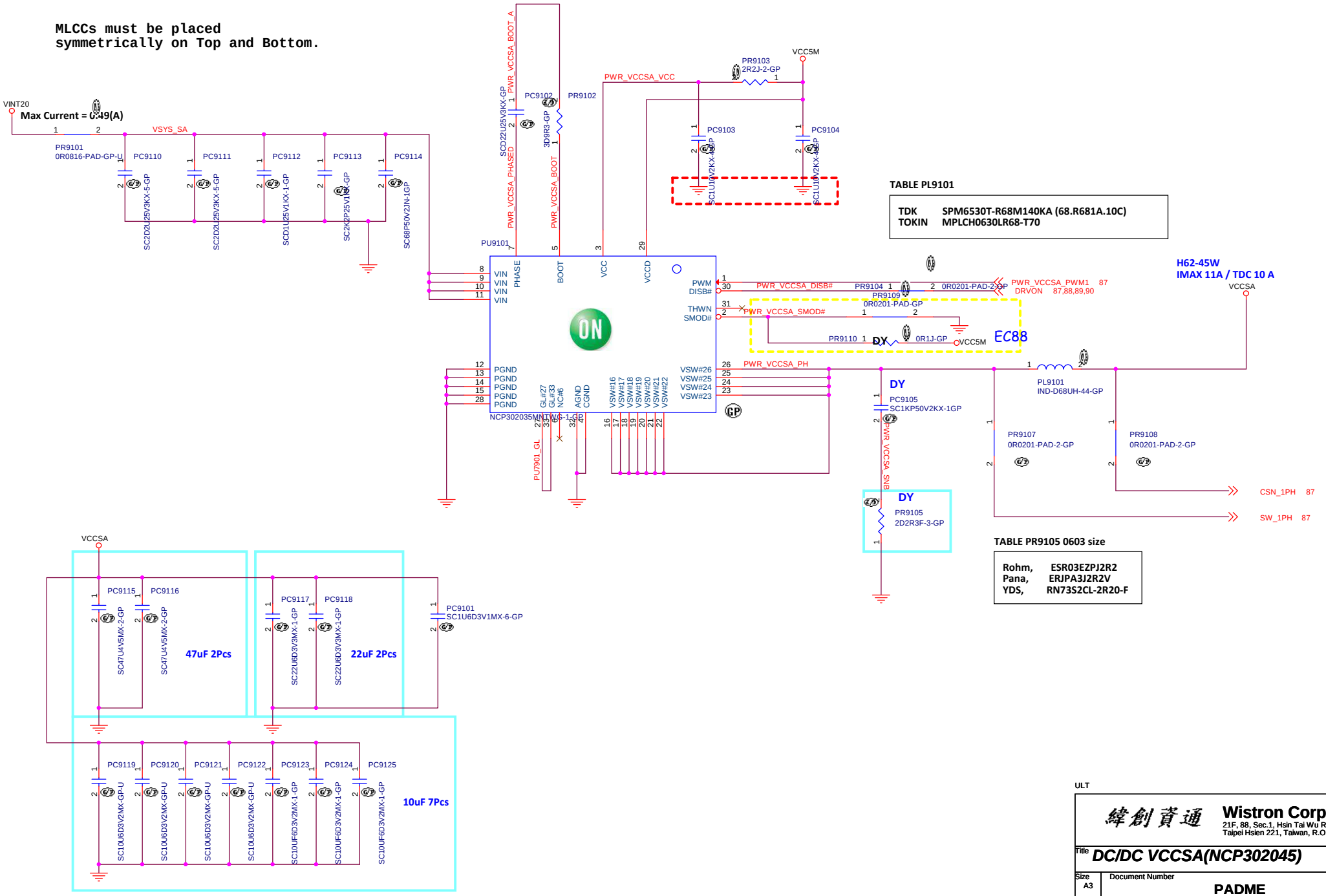

TABLE PL9101

TDK	SPM6530T-R68M140KA (68.R681A.10C)
TOKIN	MPLCH0630LR68-T70

TABLE PR9105 0603 size

Rohm,	ESR03EZPJ2R2
Pana,	ERJPA3J2R2V
YDS,	RN73S2CL-2R20-F

ULT

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Title: ***DC/DC VCCSA(NCP302045)***

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 91 of 110

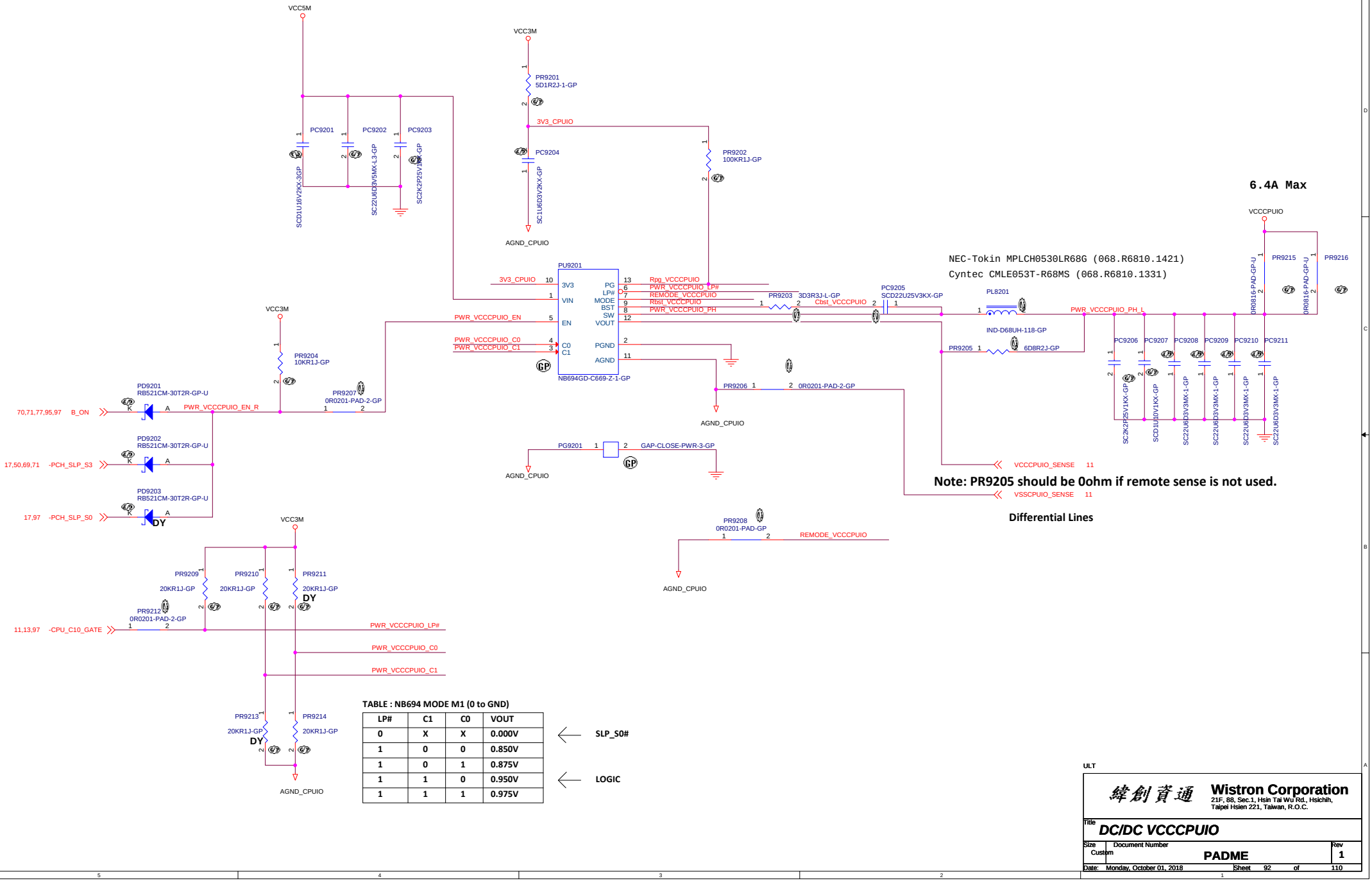

TABLE : NB694 MODE M1 (0 to GND)

LP#	C1	C0	VOUT	
0	X	X	0.000V	← SLP_S0#
1	0	0	0.850V	
1	0	1	0.875V	
1	1	0	0.950V	← LOGIC
1	1	1	0.975V	

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Title: ***DC/DC VCCCPUIO***

Size	Document Number	Rev
Custom	PADME	1

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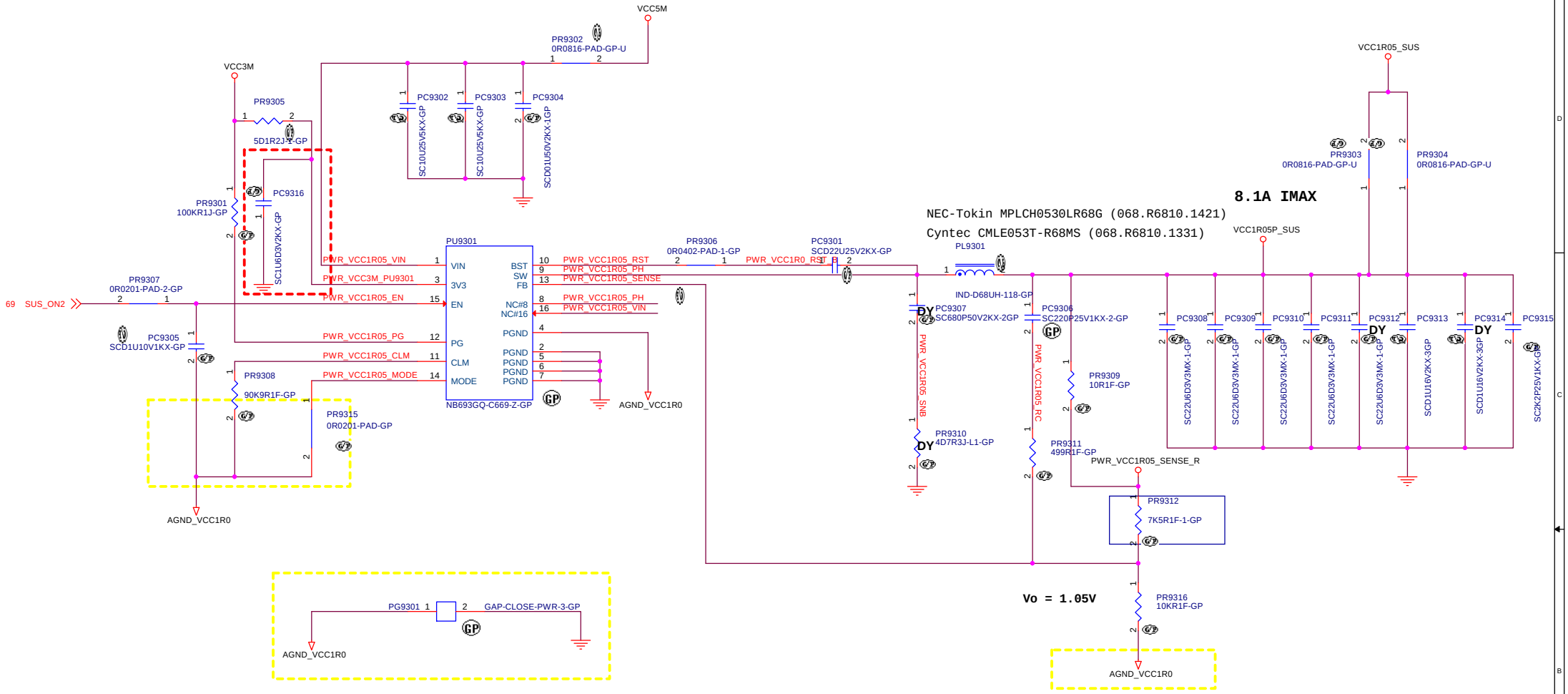

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Title	***DC/DC VCC1R05_SUS***	
Size: A3	Document Number: **PADME**	Rev: 1
Date: Monday, October 01, 2018	Sheet 93 of 110	

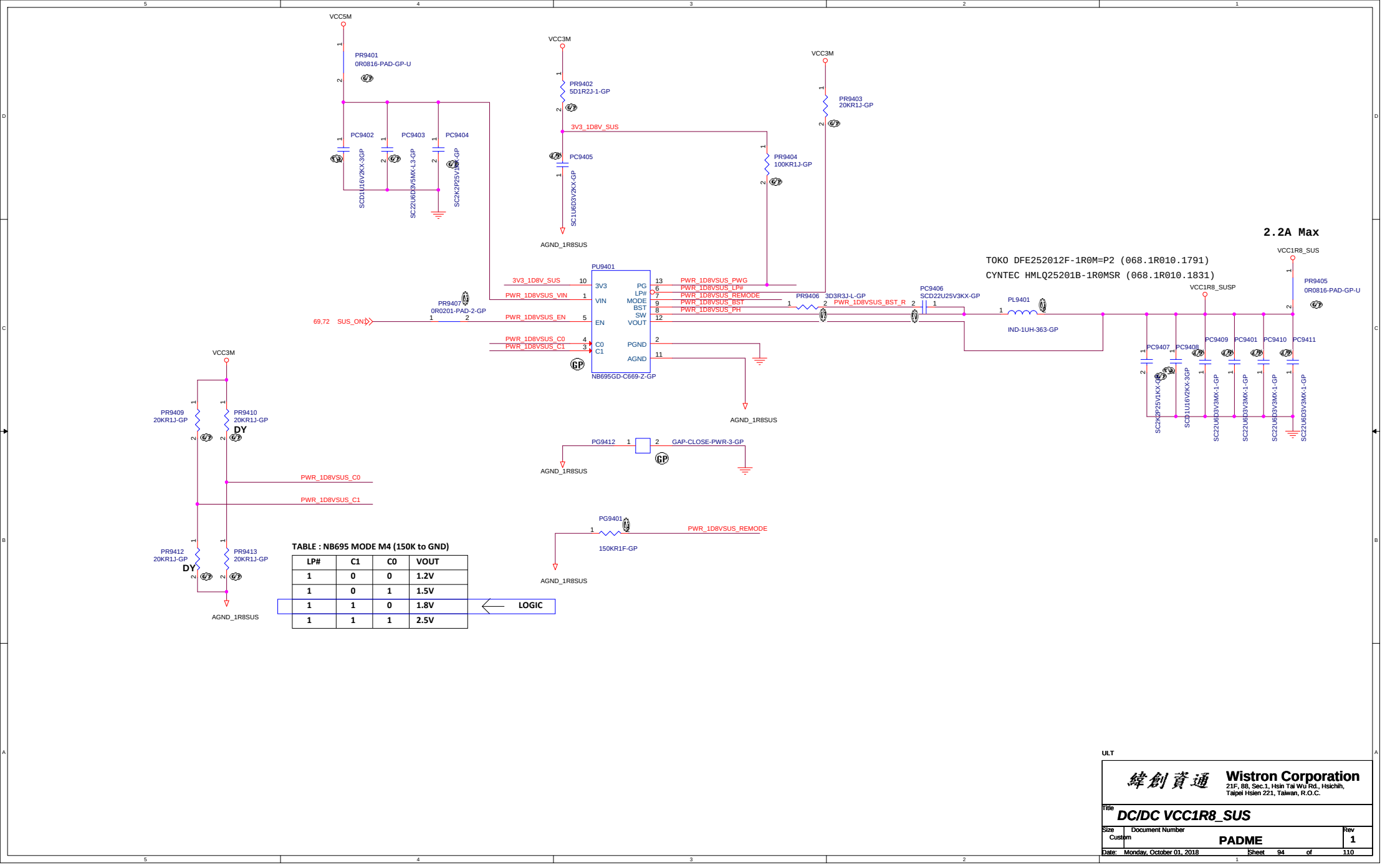

TABLE : NB695 MODE M4 (150K to GND)

LP#	C1	C0	VOUT
1	0	0	1.2V
1	0	1	1.5V
1	1	0	1.8V
1	1	1	2.5V

LOGIC

ULT

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Title: ***DC/DC VCC1R8_SUS***

Size	Document Number	Rev
Custom	PADME	1

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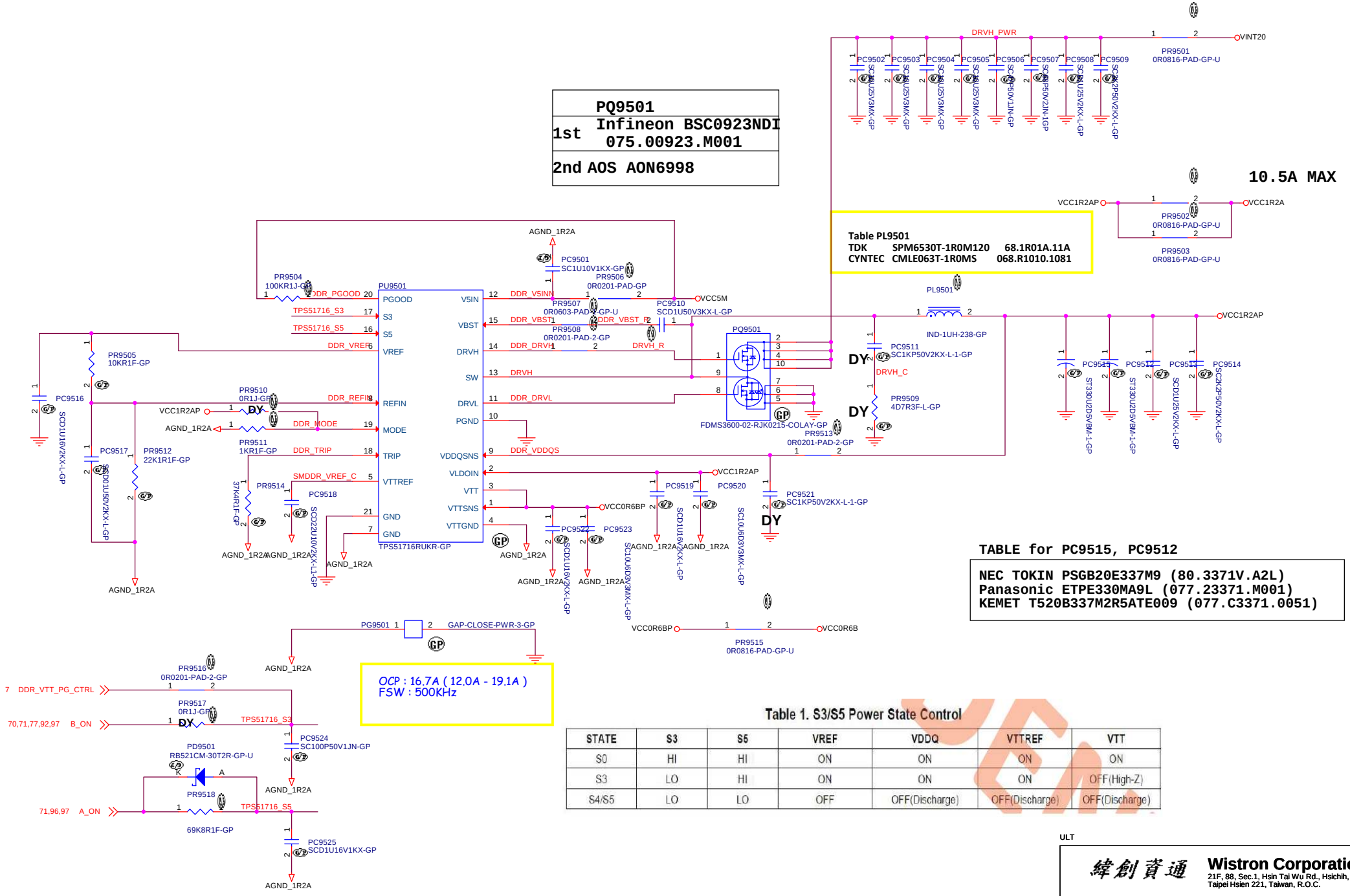

Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

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Title: DC/DC VCC1R2A/VCC0R6B

Size	Document Number	Rev
A3	PADME	1

Date: Monday, October 01, 2018 Sheet 95 of 110

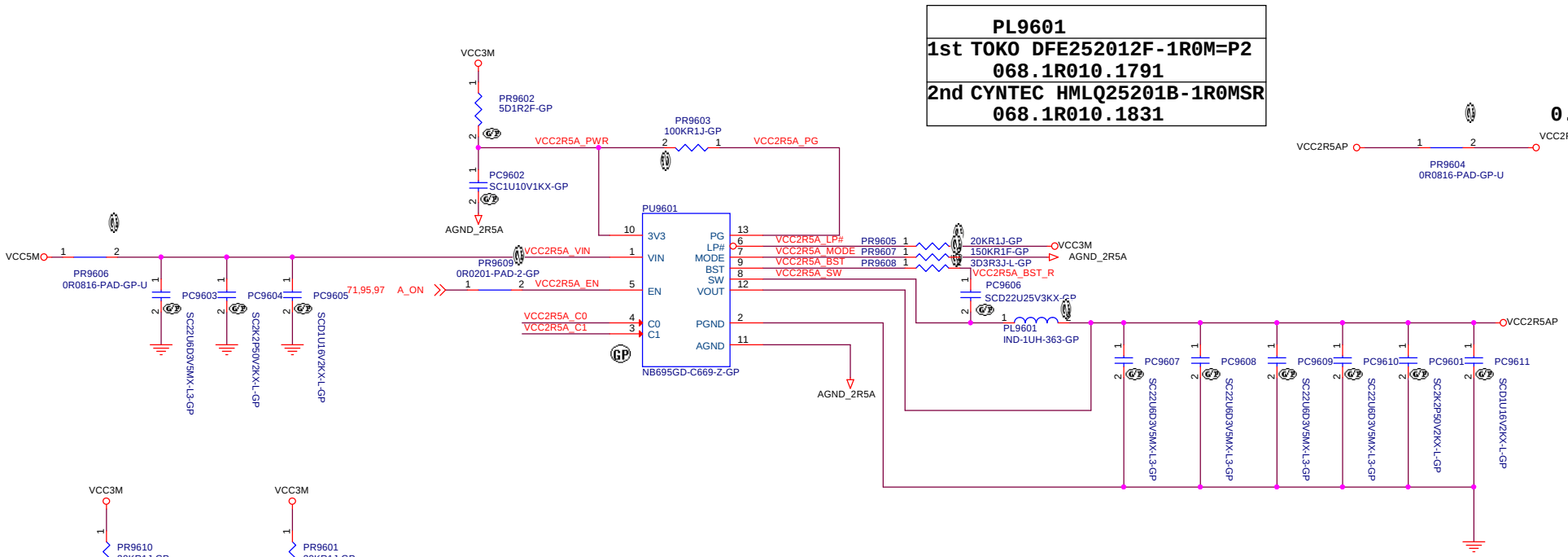

TABLE : NB695 MODE M4 (150K to GND)

LP#	C1	C0	VOUT(V)
1	0	0	1.2V
1	0	1	1.5V
1	1	0	1.8V
1	1	1	2.5V

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Title: ***DC/DC VCC2R5A***

Size	Document Number	Rev
A3	PADME	1

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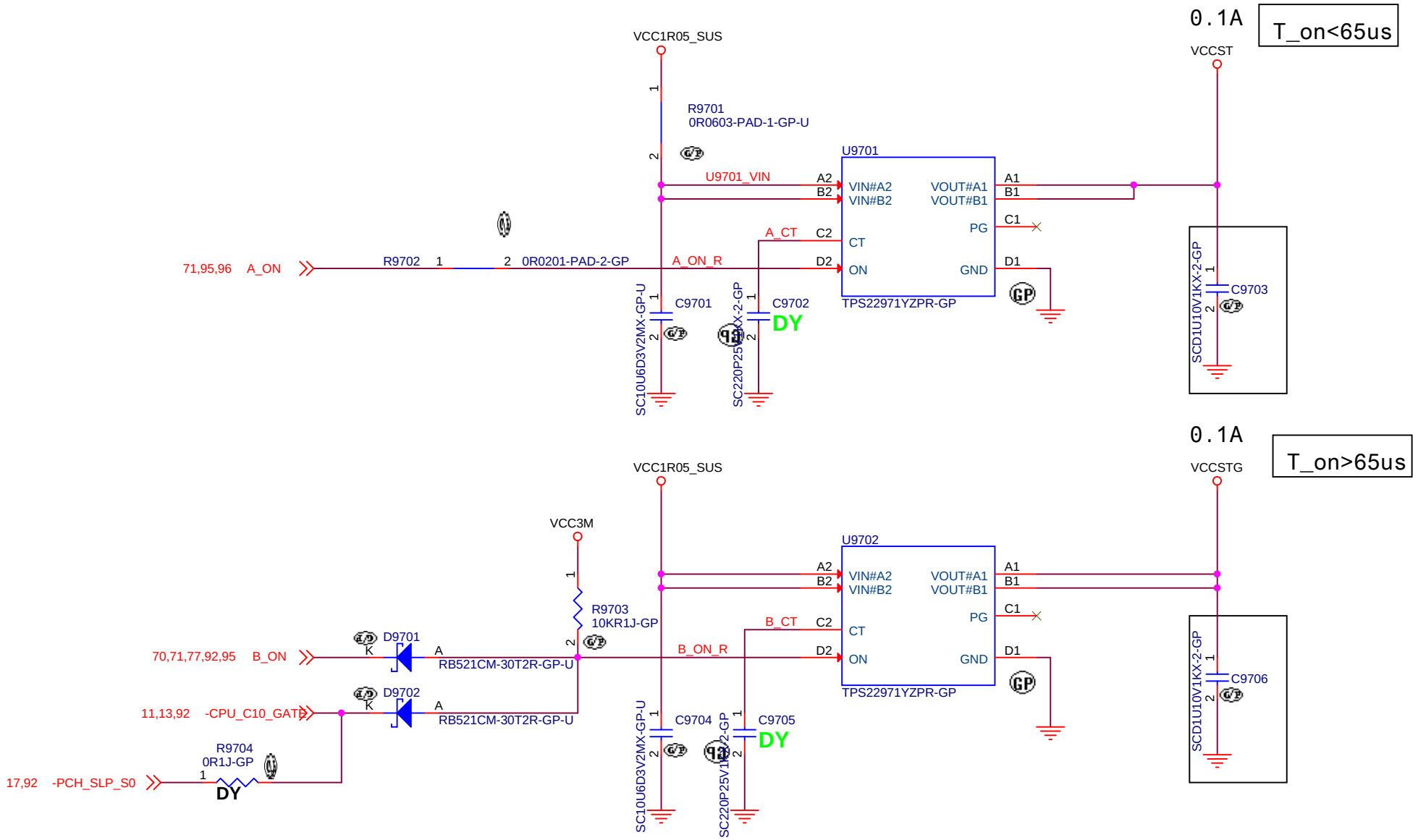

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Title: **LOAD SW VCCST/VCCSTG**

Size	Document Number	Rev
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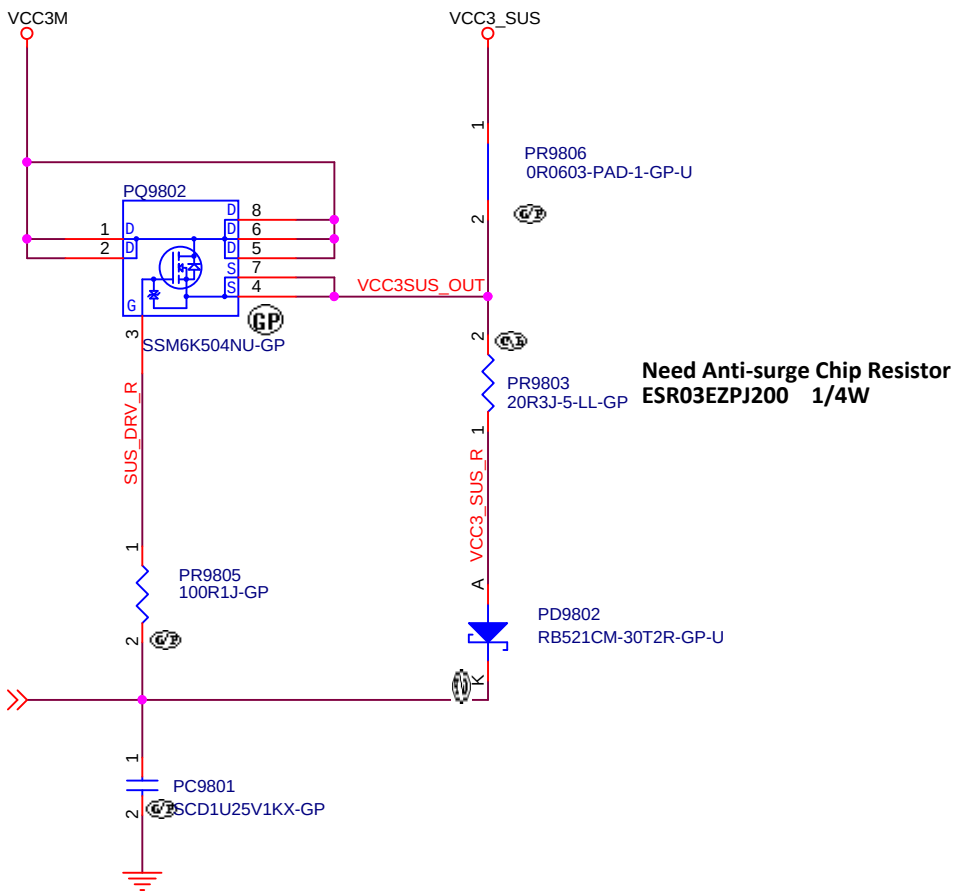
2.4A



ULT

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Title: *LOAD SW PCH SUS/TP*		
Size: A4	Document Number: PADME	Rev: 1
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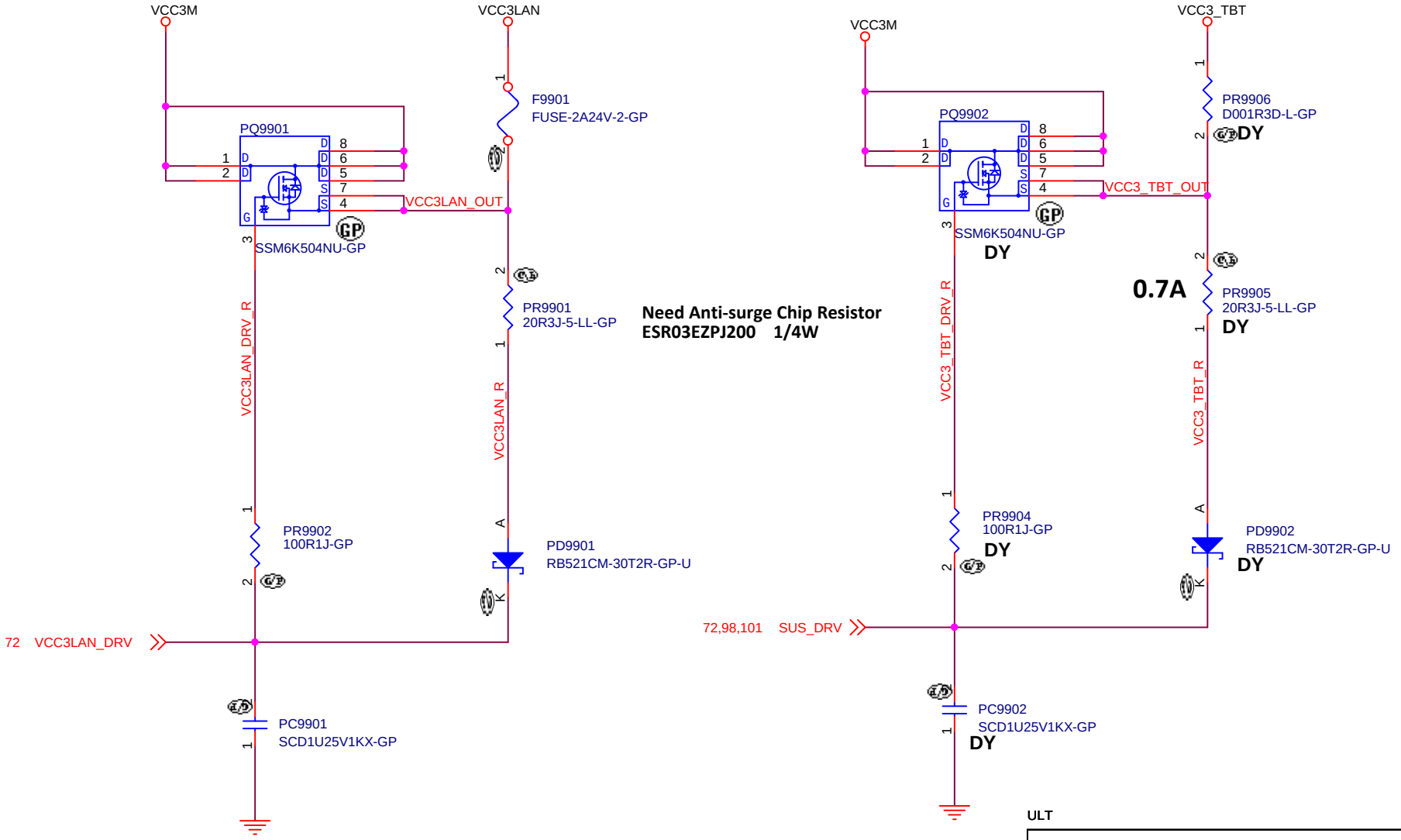
VCC3LAN

0.25A



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Title	***LOAD SW LAN/VCC3_TBT***	
Size A4	Document Number **PADME**	Rev 1
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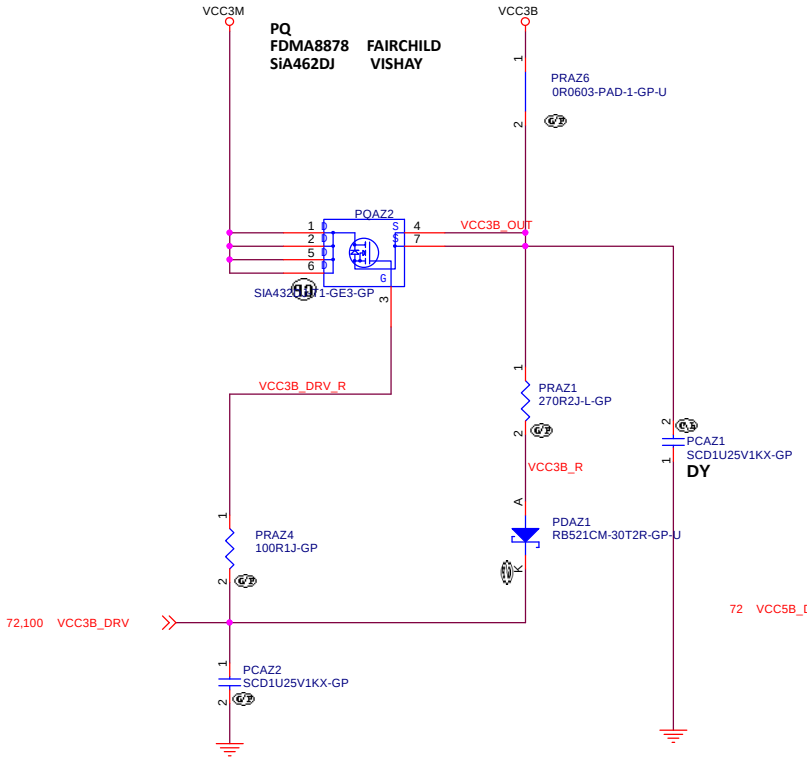
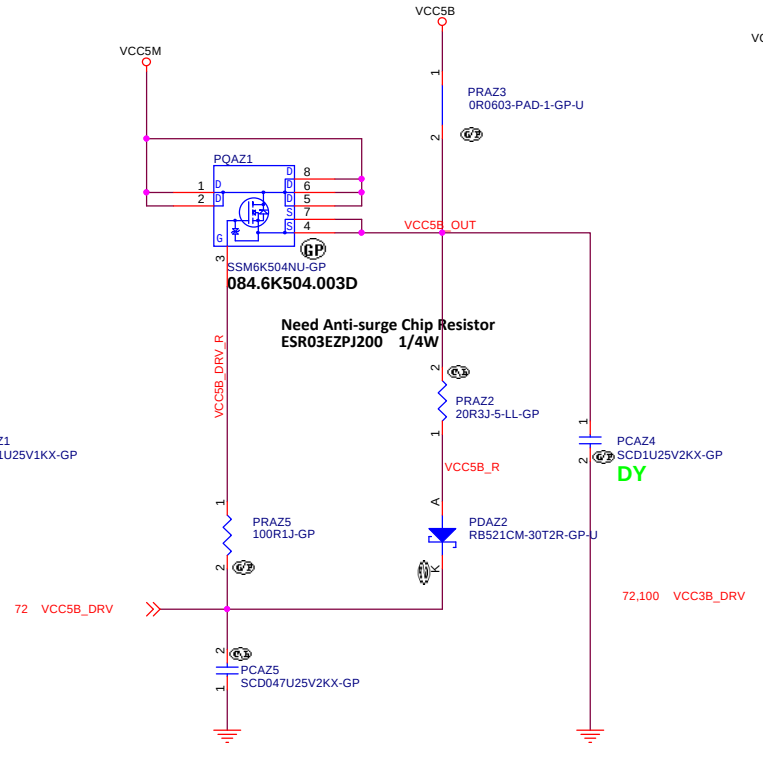
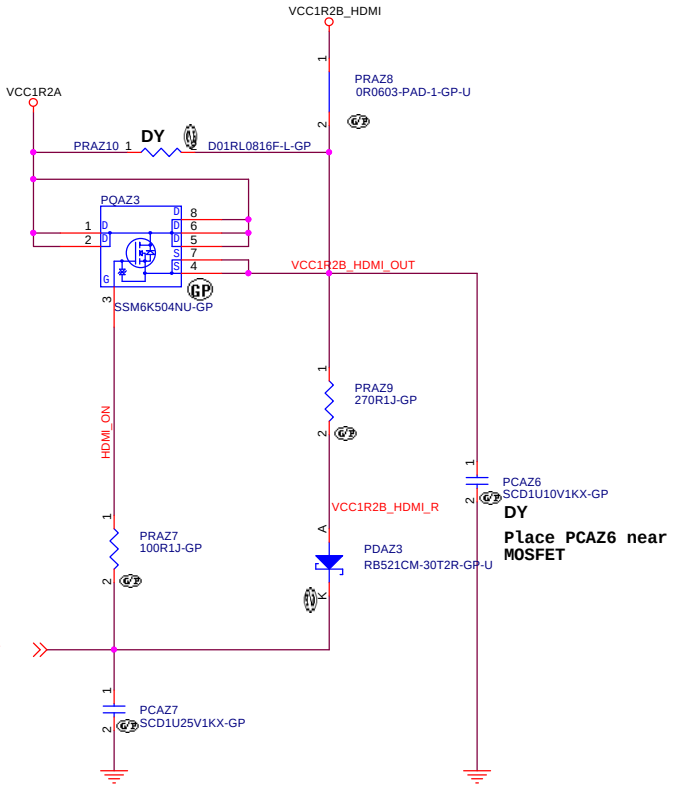
VCC3B
Max Current = 7.4 (A)

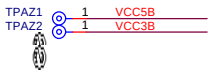


VCC5B
Max Current = 1.5 (A)



HDMI
Max Current = 1.7 (A)





ULT

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Title: LOAD SW B

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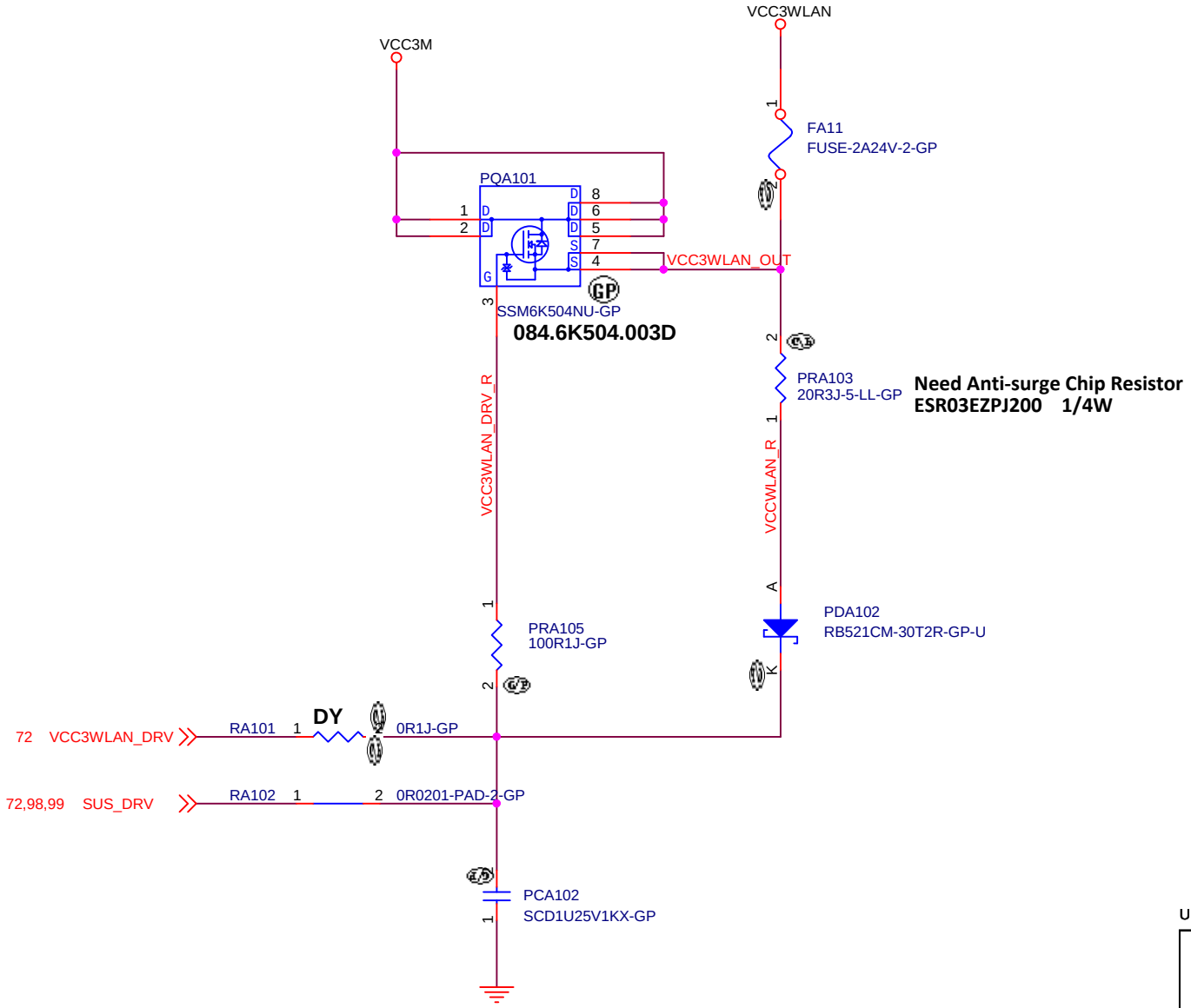
WLAN

1.1A



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Title	***LOAD SW WLAN***	
Size: A4	Document Number: **PADME**	Rev: 1
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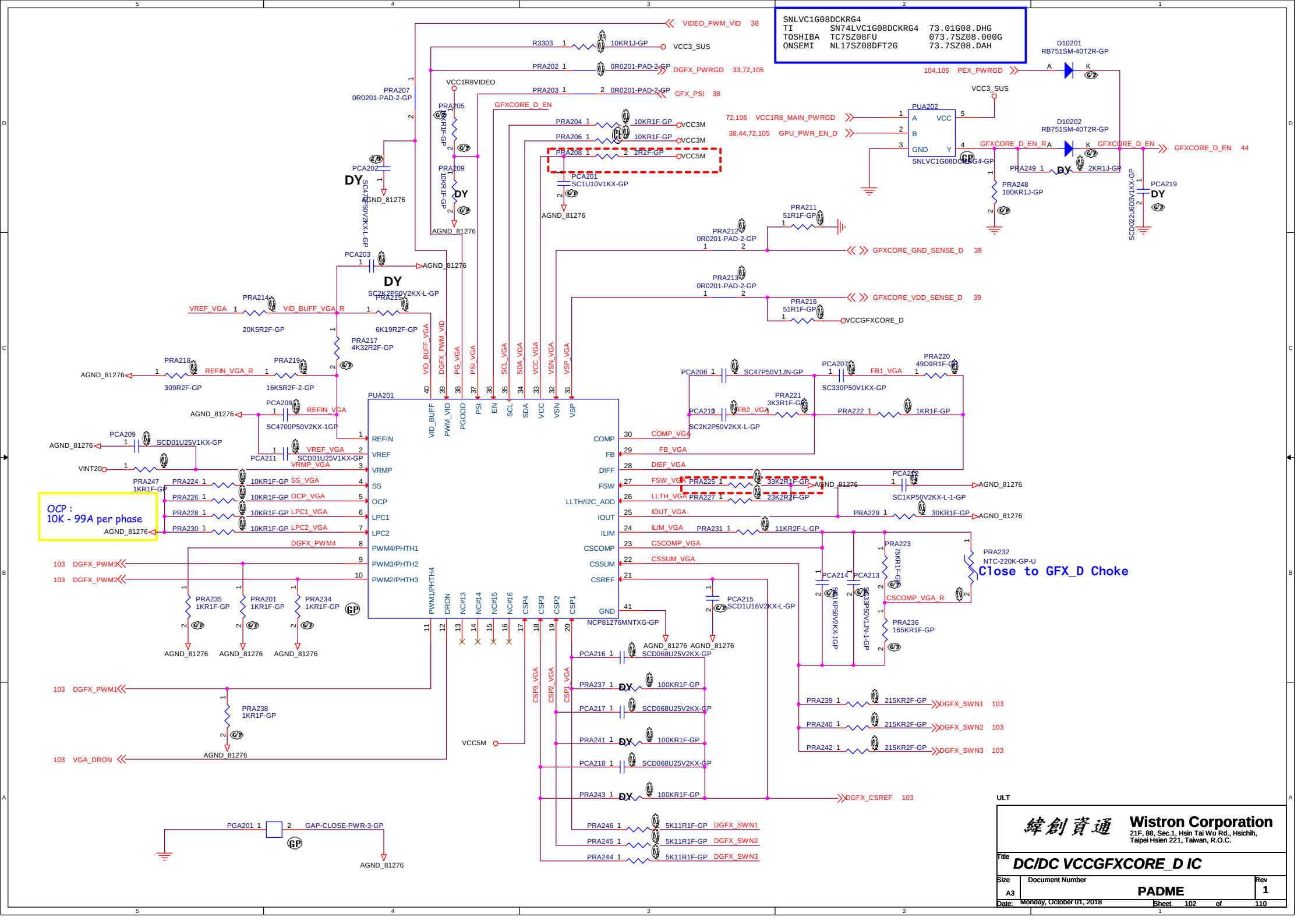
SNLVC1G08DCKRG4
TI SN74LVC1G08DCKRG4 73.01G08.DHG
TOSHIBA TC7SZ08FU 073.7SZ08.000G
ONSEMI NL17SZ08DFT2G 73.7SZ08.DAH
OCP :
10K - 99A per phase
Close to GFX_D Choke
PUA201
PUA202
SNLVC1G08DCKRG4-GP
NCP81276MNTXG-GP
VIDEO_PWM_VID 38
VCC3_SUS
DGFX_PWRGD 33,72,105
GFX_PSI 38
VCC1R8VIDEO
GFXCORE_D_EN
VCC3M
VCC5M
72,106 VCC1R8_MAIN_PWRGD
38,44,72,105 GPU_PWR_EN_D
104,105 PEX_PWRGD
GFXCORE_D_EN 44
GFXCORE_GND_SENSE_D 39
GFXCORE_VDD_SENSE_D 39
VCCGFXCORE_D
VREF_VGA
VID_BUFF_VGA_R
REFIN_VGA_R
REFIN_VGA
VRMP_VGA
SS_VGA
OCP_VGA
LPC1_VGA
LPC2_VGA
DGFX_PWM4
DGFX_PWM3
DGFX_PWM2
DGFX_PWM1
VGA_DRON
COMP_VGA
FB_VGA
DIEF_VGA
FSW_VGA
LLTH_VGA
IOUT_VGA
ILIM_VGA
CSCOMP_VGA
CSSUM_VGA
CSCOMP_VGA_R
FB1_VGA
FB2_VGA
DGFX_SWN1 103
DGFX_SWN2 103
DGFX_SWN3 103
DGFX_CSREF 103
AGND_81276
VINT20
Wistron Corporation
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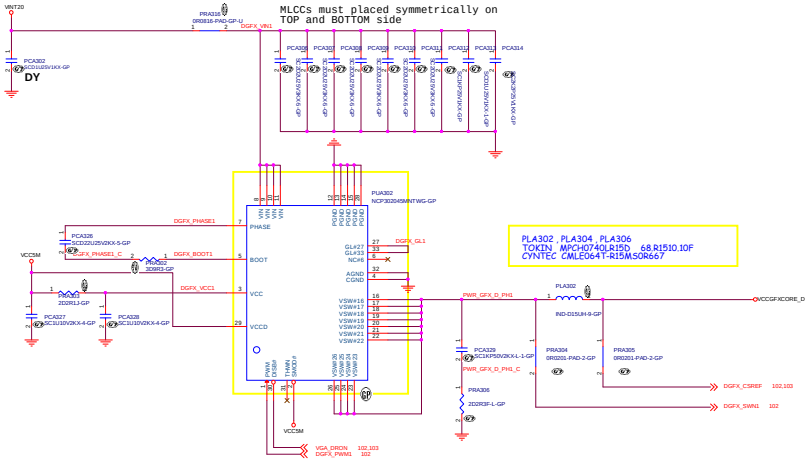
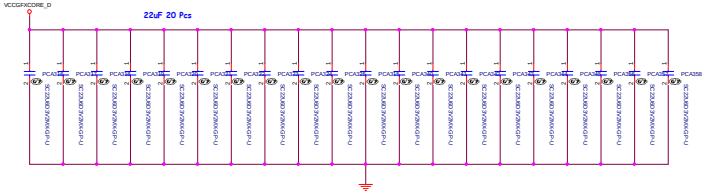
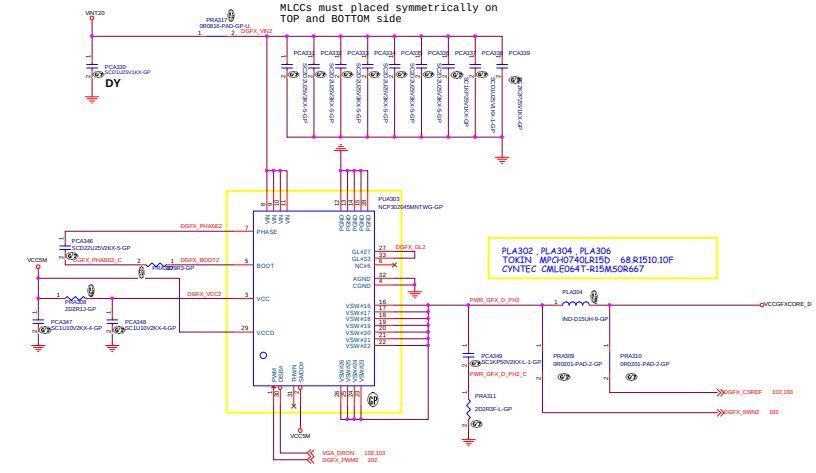
Title DC/DC VCCGFXCORE_D IC
Size A3
Document Number PADME
Rev 1
Date: Monday, October 01, 2018
Sheet 102 of 110

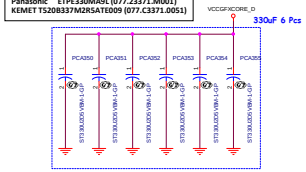


EDP-Continue : 46 A
EDP-Peak : 110 A

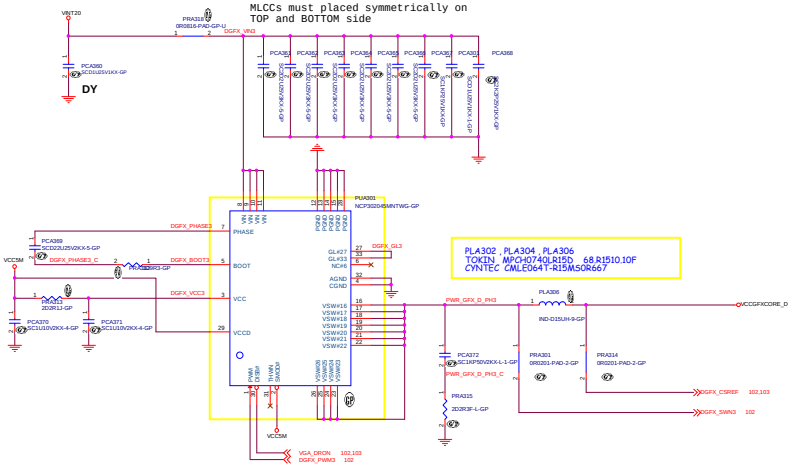




NEC TOKIN PSGB20E337M9 (80.3371V.A2L)
Panasonic ETPE330MA9L (077.23371.M001)
KEMET T520B337M2R5ATE009 (077.C3371.0051)



2017/07/07 - 470uF_D2 change to 330uF_B2



ULT

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File: DC/DC VCCGFXCORE_D

Size	Document Number	Rev
A1	PADME	1

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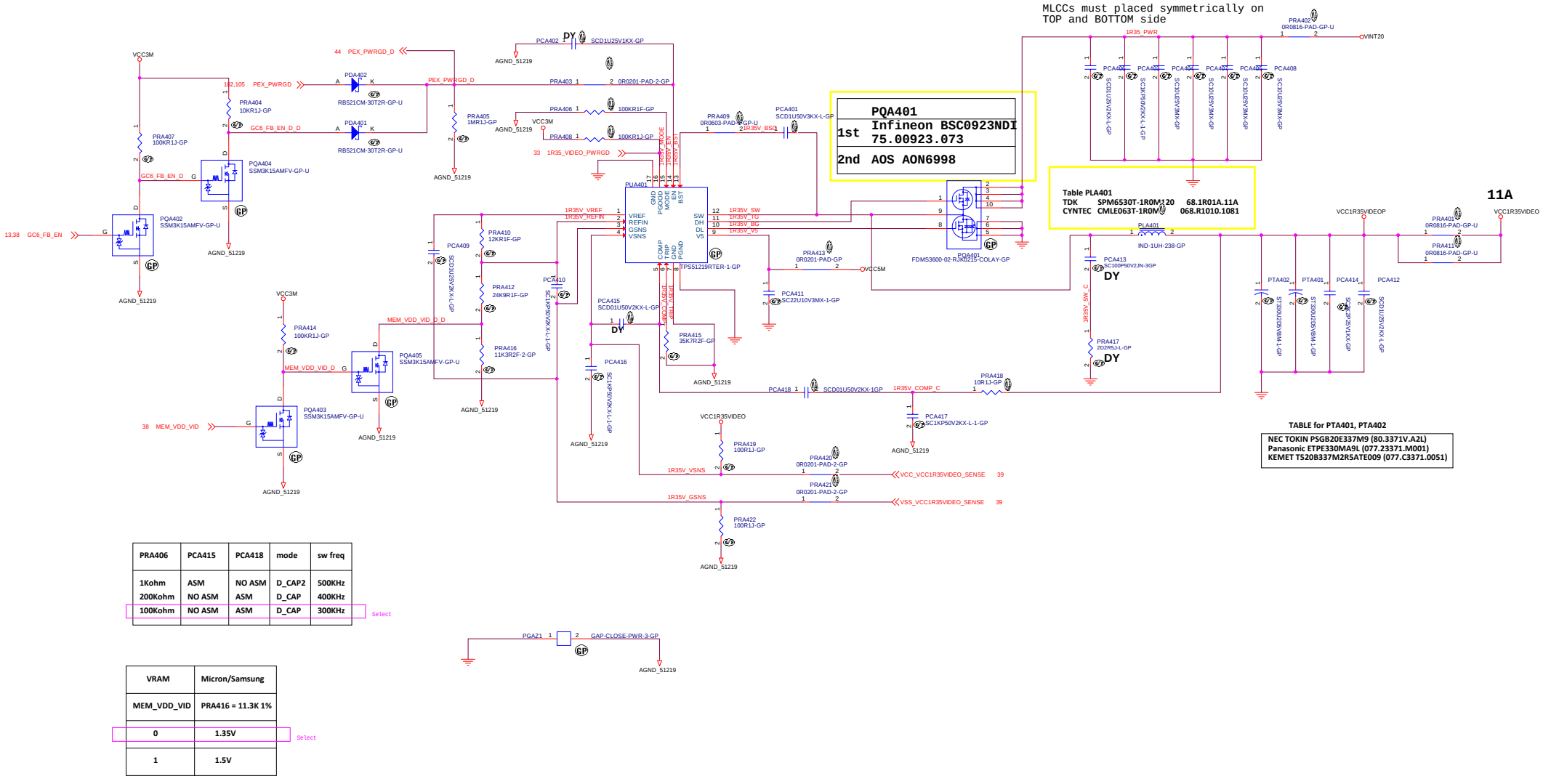

PRA406	PCA415	PCA418	mode	sw freq
1Kohm	ASM	NO ASM	D_CAP2	500KHz
200Kohm	NO ASM	ASM	D_CAP	400KHz
100Kohm	NO ASM	ASM	D_CAP	300KHz

Select

VRAM	Micron/Samsung
MEM_VDD_VID	PRA416 = 11.3K 1%
0	1.35V
1	1.5V

Select

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Title: DC/DC VCC1R35VIDEO

Size	Document Number	Rev
A2	PADME	1

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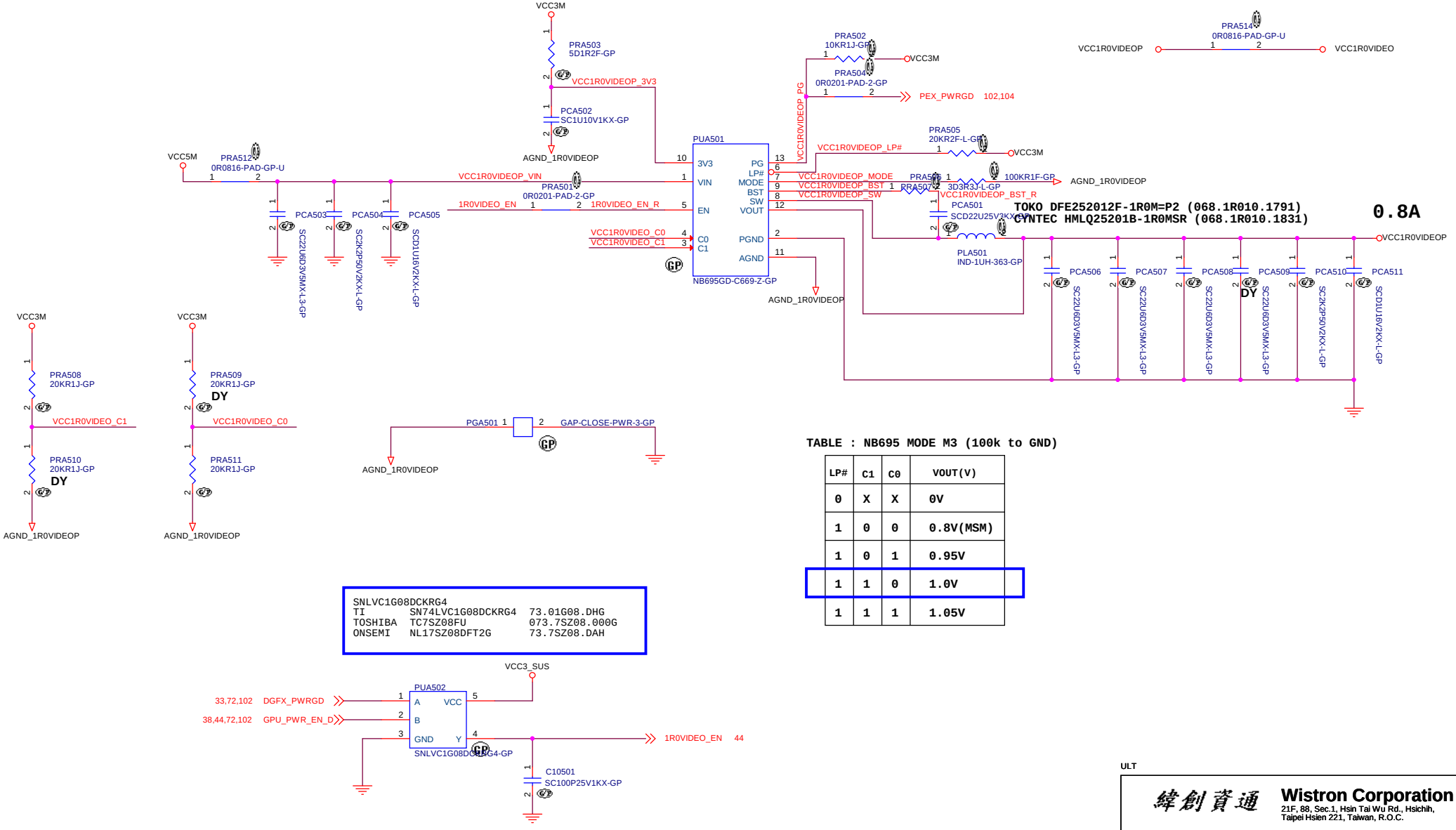

TABLE : NB695 MODE M3 (100k to GND)

LP#	C1	C0	VOUT(V)
0	X	X	0V
1	0	0	0.8V(MSM)
1	0	1	0.95V
1	1	0	1.0V
1	1	1	1.05V

SNLVC1G08DCKRG4		
TI	SN74LVC1G08DCKRG4	73.01G08.DHG
TOSHIBA	TC7SZ08FU	073.7SZ08.000G
ONSEMI	NL17SZ08DFT2G	73.7SZ08.DAH

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Title: ***DC/DC VCC1R0VIDEO***

Size	Document Number	Rev
A3	PADME	1

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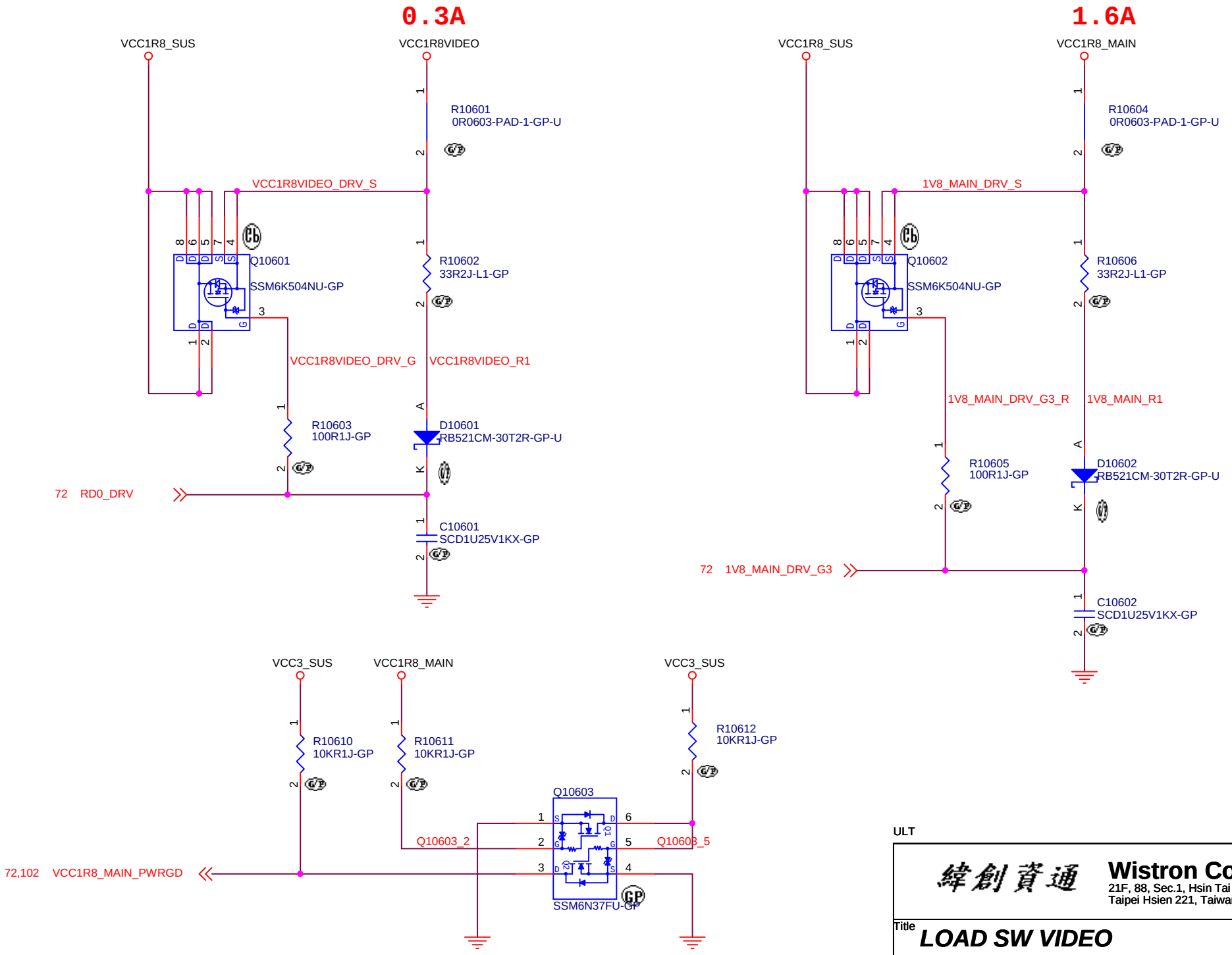

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Title **LOAD SW VIDEO**

Size	Document Number	Rev
A4	PADME	1

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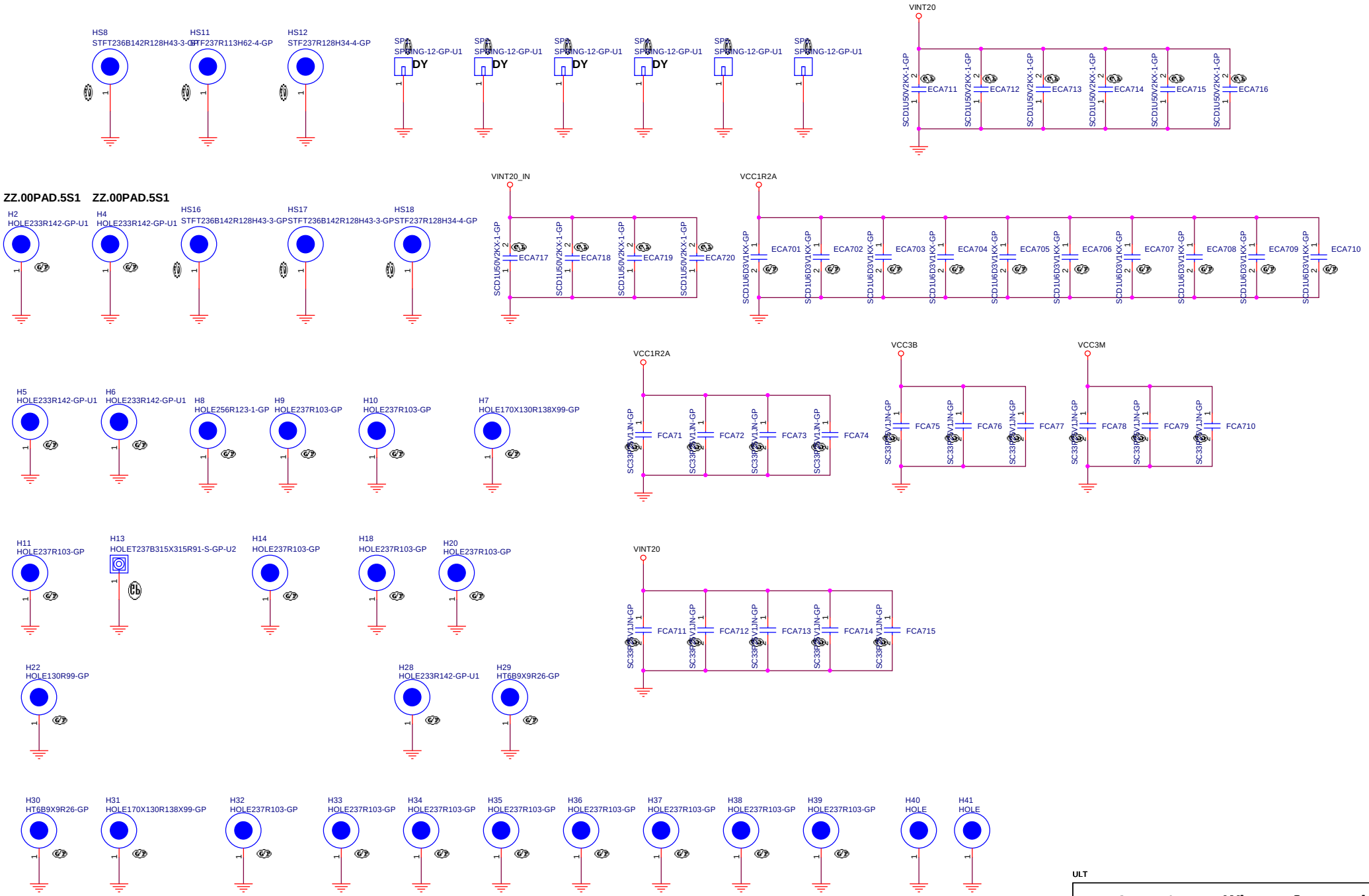

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title	***HOLE/EMC/RF***	
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Title

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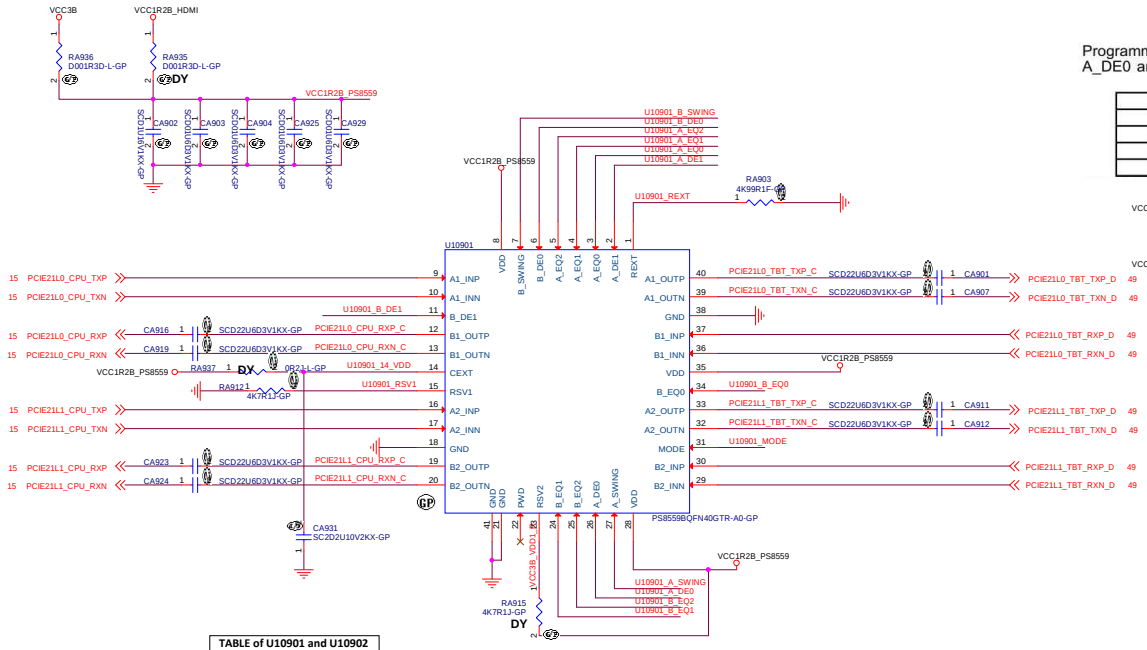
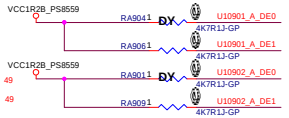


TABLE of U10901 and U10902	
PS8559A	PS8559B
RA936 DY RA935 ASM CA931 DY RA937 ASM	RA936 ASM RA935 DY CA931 ASM RA937 DY

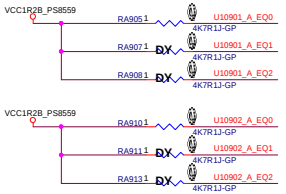
Programmable output de-emphasis level setting for channel A .
A_DE0 and A_DE1: internally pulled down at ~150K

A_DE<1:0>	DE Level
00(default)	-3.5dB
01	-6dB
10	-2.2dB
11	-7.5dB



Equalizer control and program for channel A.
A_EQ0, A_EQ1 and A_EQ2: internally pulled down at ~150K

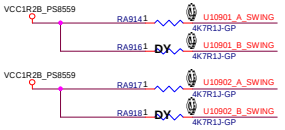
A_EQ<2:0>	EQ Level
000(defult)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB

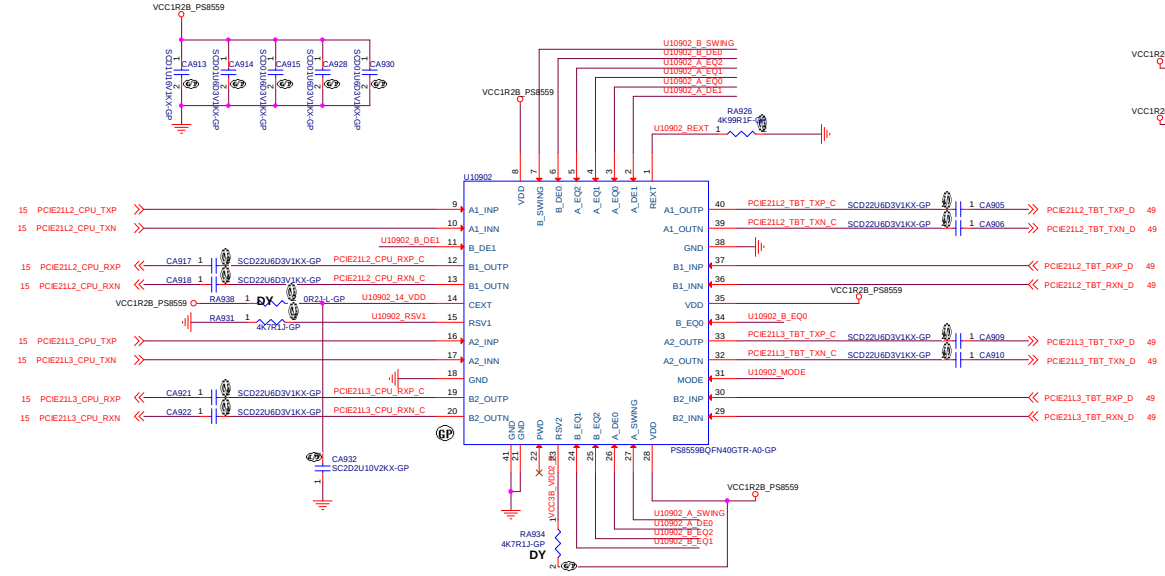


Internally pulled down at ~150KΩ

A_SWING	Swing Adjustment
0(default)	Default
1	Increase 10%

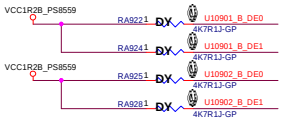
B_SWING	Swing Adjustment
0(default)	Default
1	Increase 10%





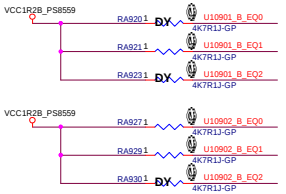
Programmable output de-emphasis level setting for channel B .
B_DE0 and B_DE1: internally pulled down at ~150K

B_DE<1:0>	DE Level
00(default)	-3.5dB
01	-6dB
10	-2.2dB
11	-7.5dB



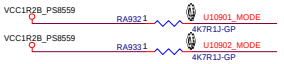
Equalizer control and program for channel B.
B_EQ0, B_EQ1 and B_EQ2: internally pulled down at ~150K

B_EQ<2:0>	EQ Level
000(defult)	14dB
001	10dB
010	8dB
011	4dB
100	16dB
101	17dB
110	19dB
111	21dB



Internally pulled down at ~150KΩ

MODE	Operation Mode
0(default)	SATA
1	PCIe



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Title: PCIE RE-DRIVER

Size	Document Number	Rev
A2	PADME	1

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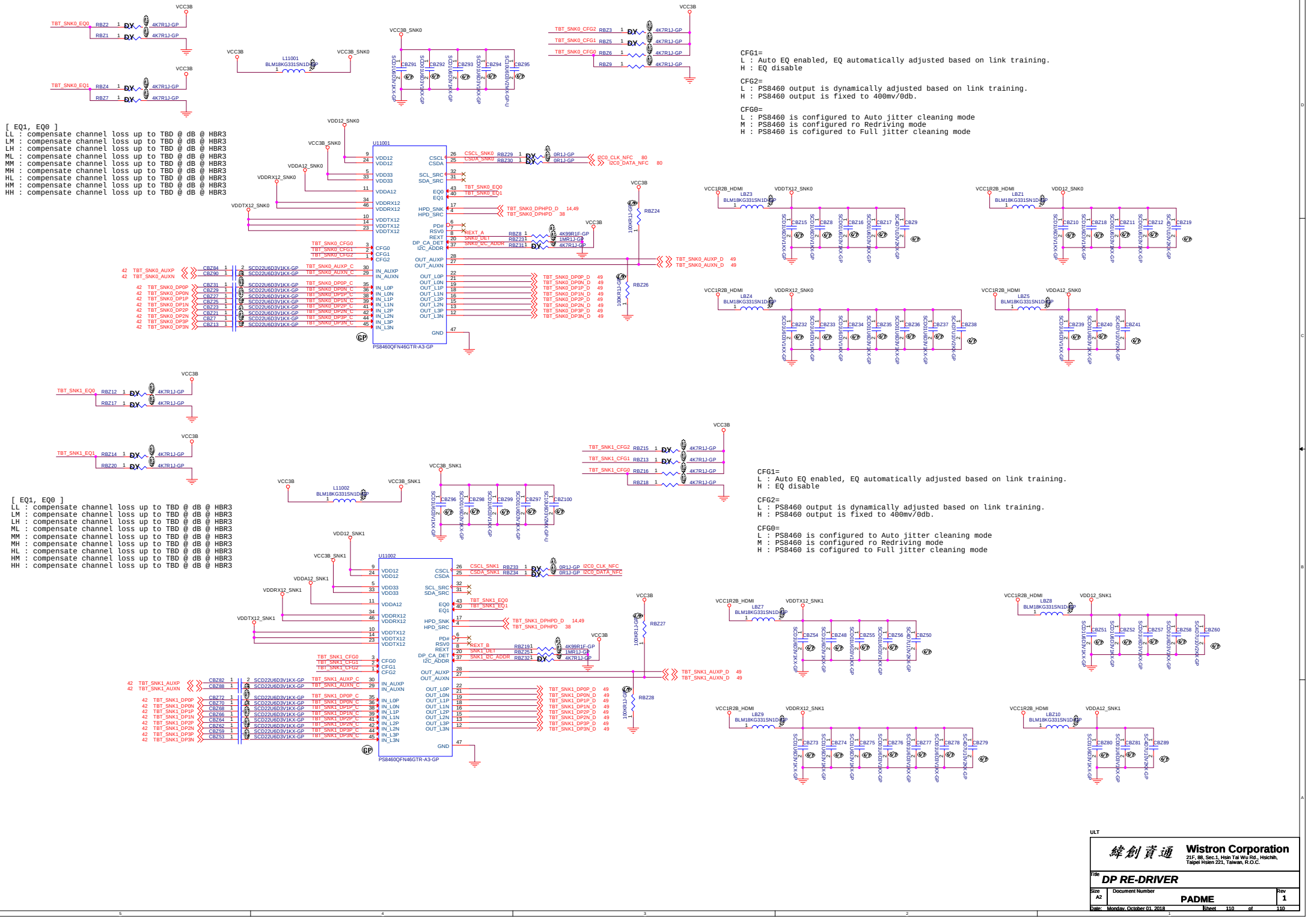
[EQ1, EQ0]
LL : compensate channel loss up to TBD @ dB @ HBR3
LM : compensate channel loss up to TBD @ dB @ HBR3
LH : compensate channel loss up to TBD @ dB @ HBR3
ML : compensate channel loss up to TBD @ dB @ HBR3
MM : compensate channel loss up to TBD @ dB @ HBR3
MH : compensate channel loss up to TBD @ dB @ HBR3
HL : compensate channel loss up to TBD @ dB @ HBR3
HM : compensate channel loss up to TBD @ dB @ HBR3
HH : compensate channel loss up to TBD @ dB @ HBR3
CFG1=
L : Auto EQ enabled, EQ automatically adjusted based on link training.
H : EQ disable
CFG2=
L : PS8460 output is dynamically adjusted based on link training.
H : PS8460 output is fixed to 400mv/0db.
CFG0=
L : PS8460 is configured to Auto jitter cleaning mode
M : PS8460 is configured ro Redriving mode
H : PS8460 is cofigured to Full jitter cleaning mode
U11001
U11002
PS8460QFN46GTR-A3-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DP RE-DRIVER
PADME
Rev 1
Monday, October 01, 2018