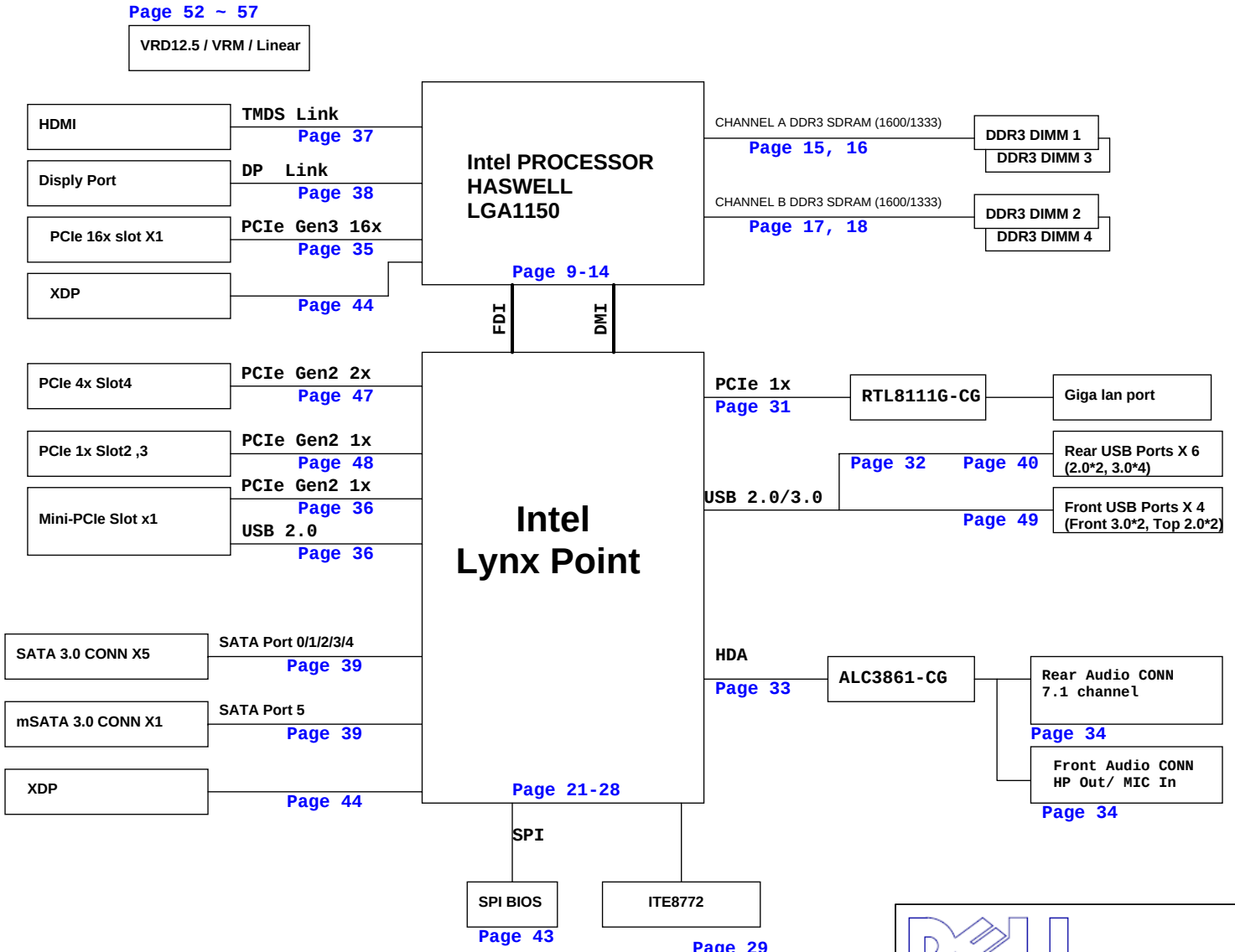
Goodyear



DELL INC.

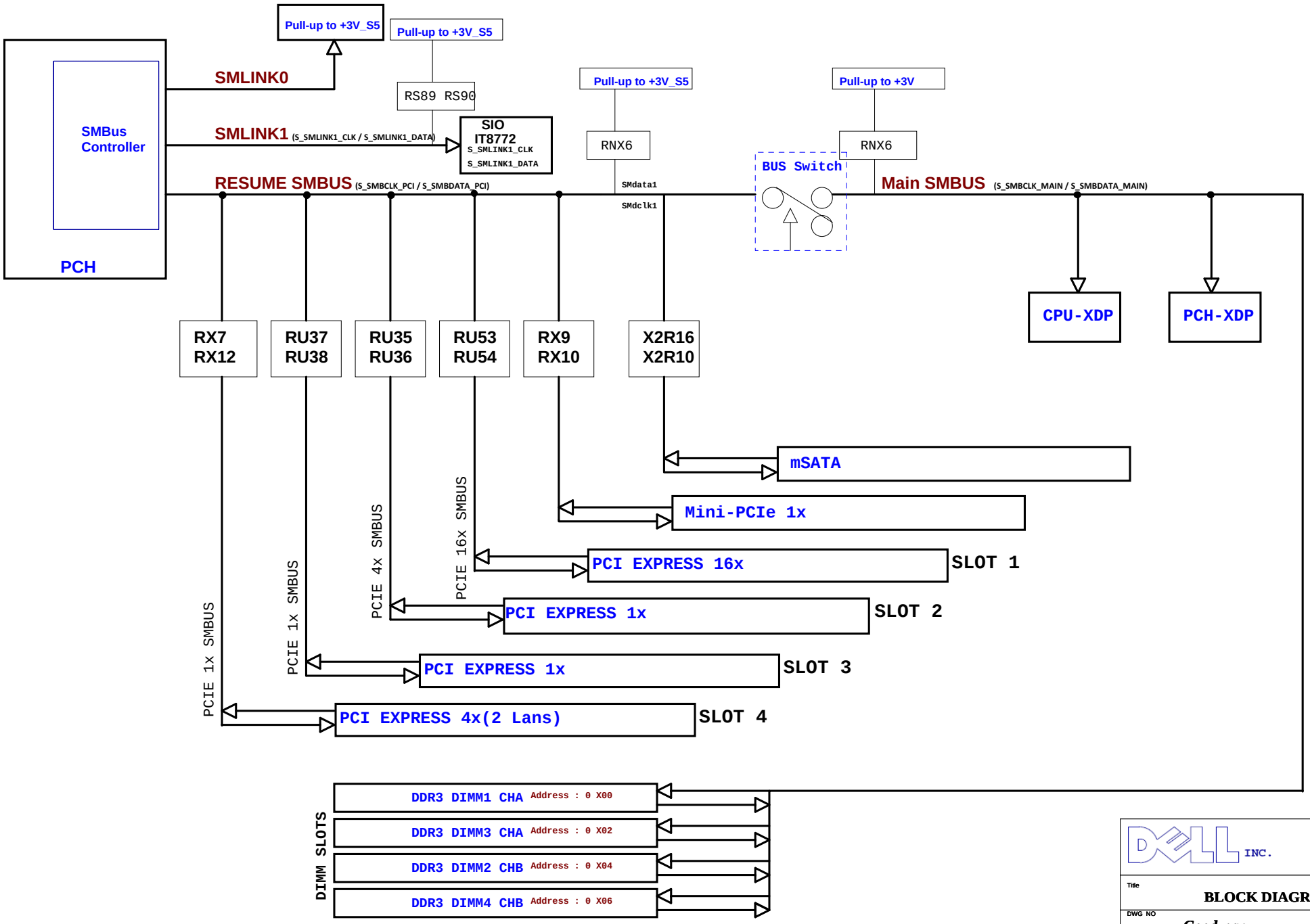
Title: Index / Block diagram

DWG NO: Goodyear

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 1 of 57

SMBUS DIAGRAM



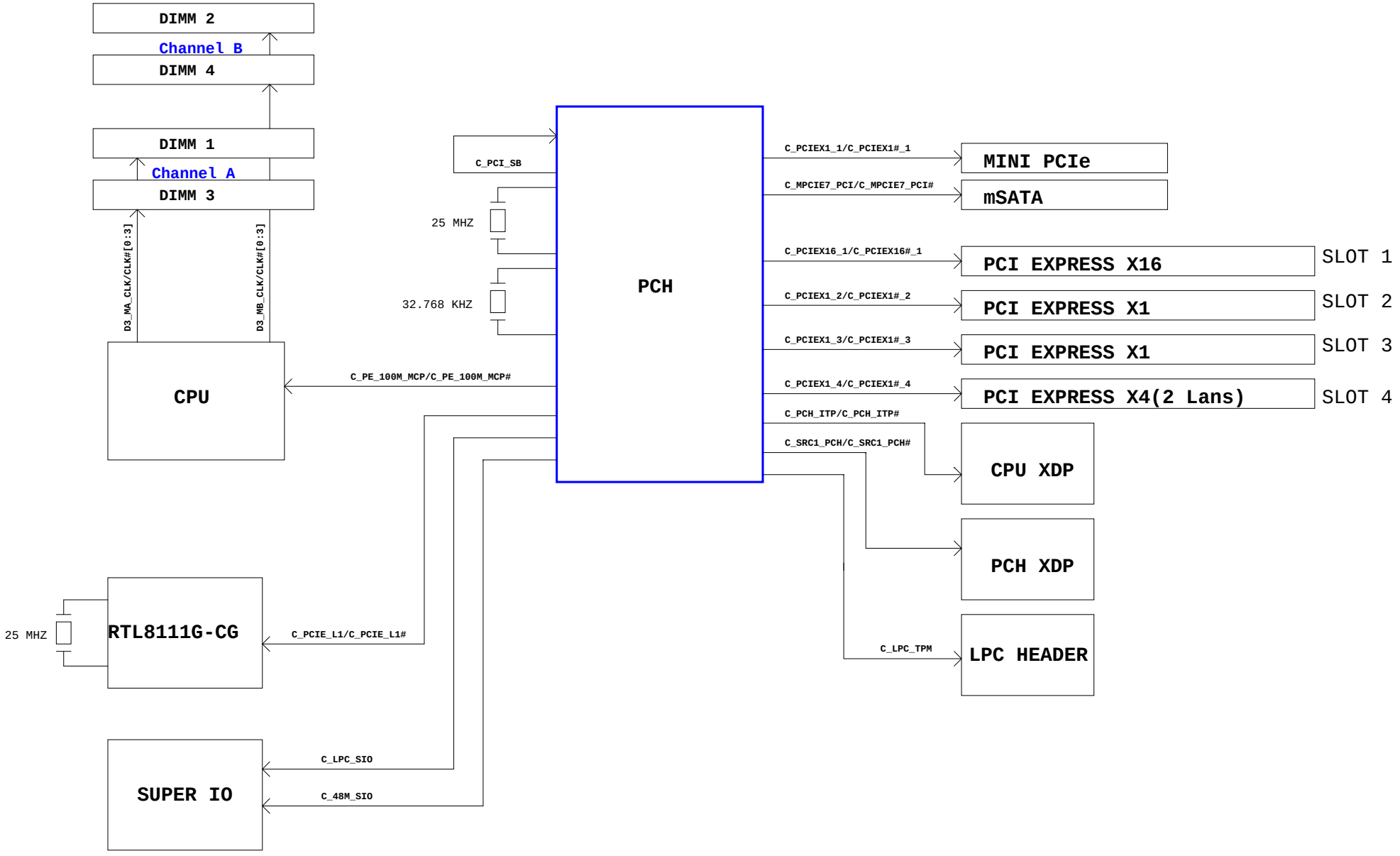
DELL INC.

Title: BLOCK DIAGRAM

DWG NO: Goodyear

Rev: A00

Date: 星期二, 二月 20, 2013 Sheet 2 of 57



DELL INC.

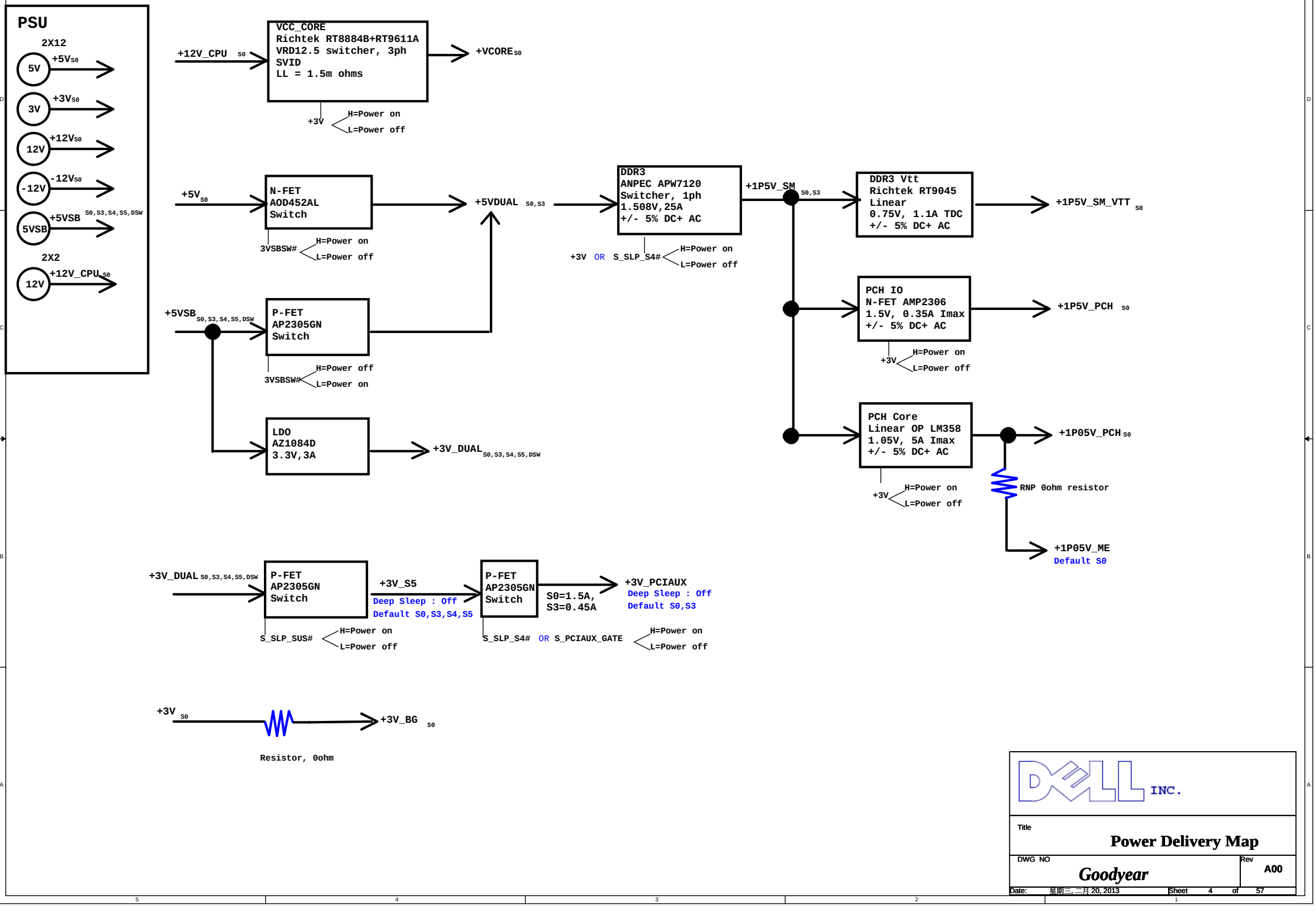
Title: Clock Distribution

DWG NO: Goodyear

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 3 of 57

POWER DELIVERY MAP



DELL INC.

Title: **Power Delivery Map**

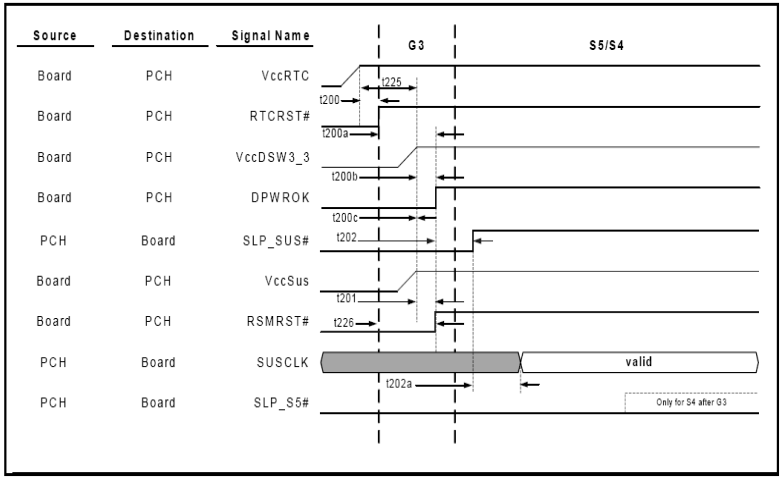
DWG NO: *Goodyear*

Rev: A00

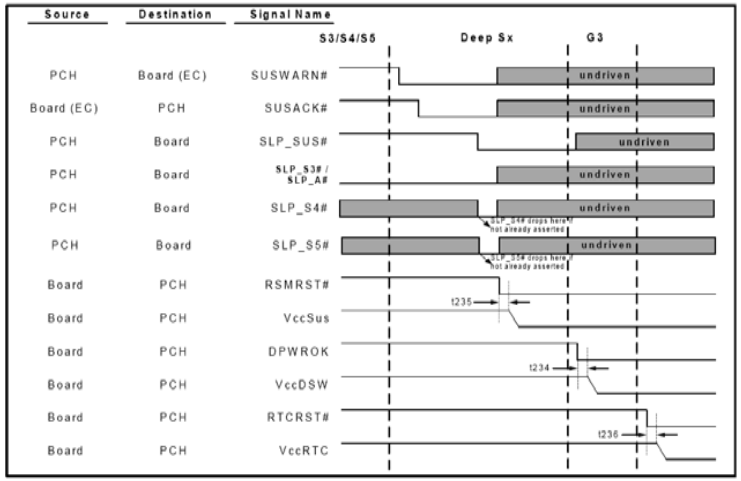
Date: 星期三, 二月 20, 2013 Sheet 4 of 57

POWER ON Timing Diagram

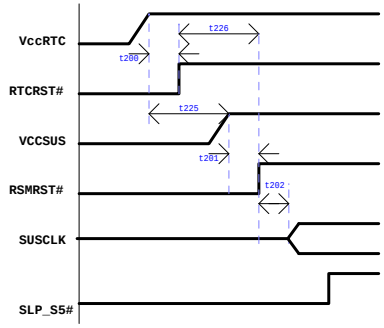
G3 --> S4/S5 (with Deep Sleep support)



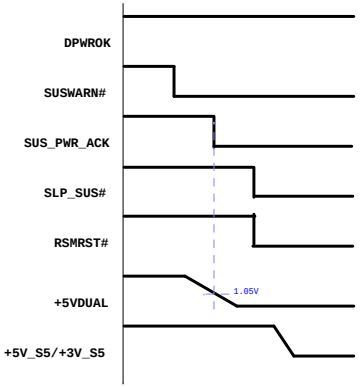
Sx --> Deep S4/S5 -->G3



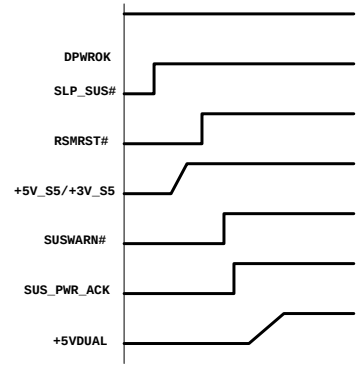
G3 to S4/S5 Timing Diagram



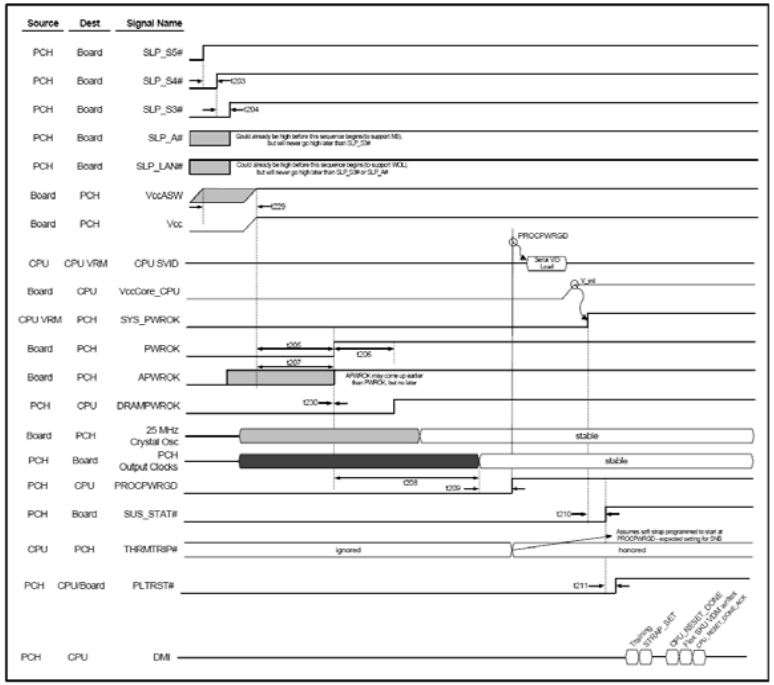
Deep Sleep Entry



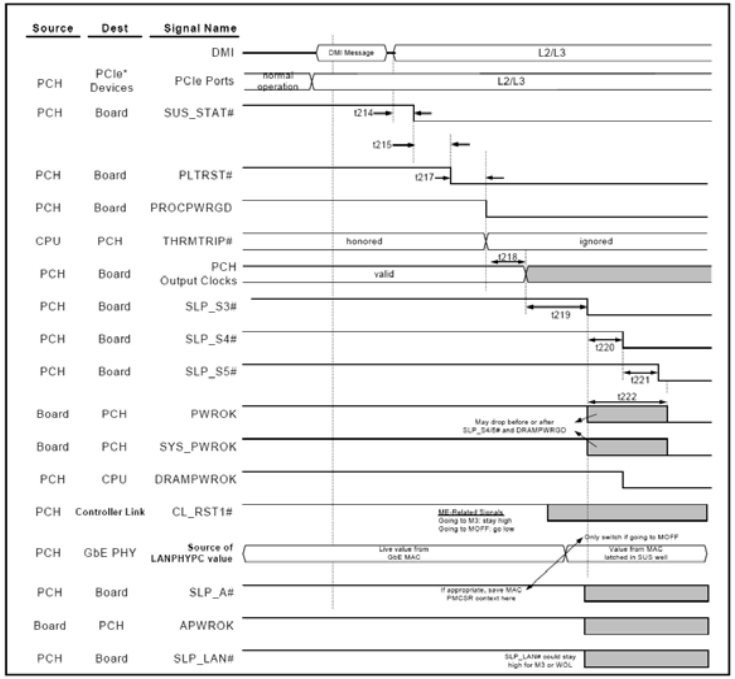
Deep Sleep Exit



S5 --> S0



S0 --> S5



Title	Power On Sequence
DWG NO	Goodyear
Rev	A00
Date:	星期三, 二月 20, 2013
Sheet	5 of 57

RESET / Power Good MAP

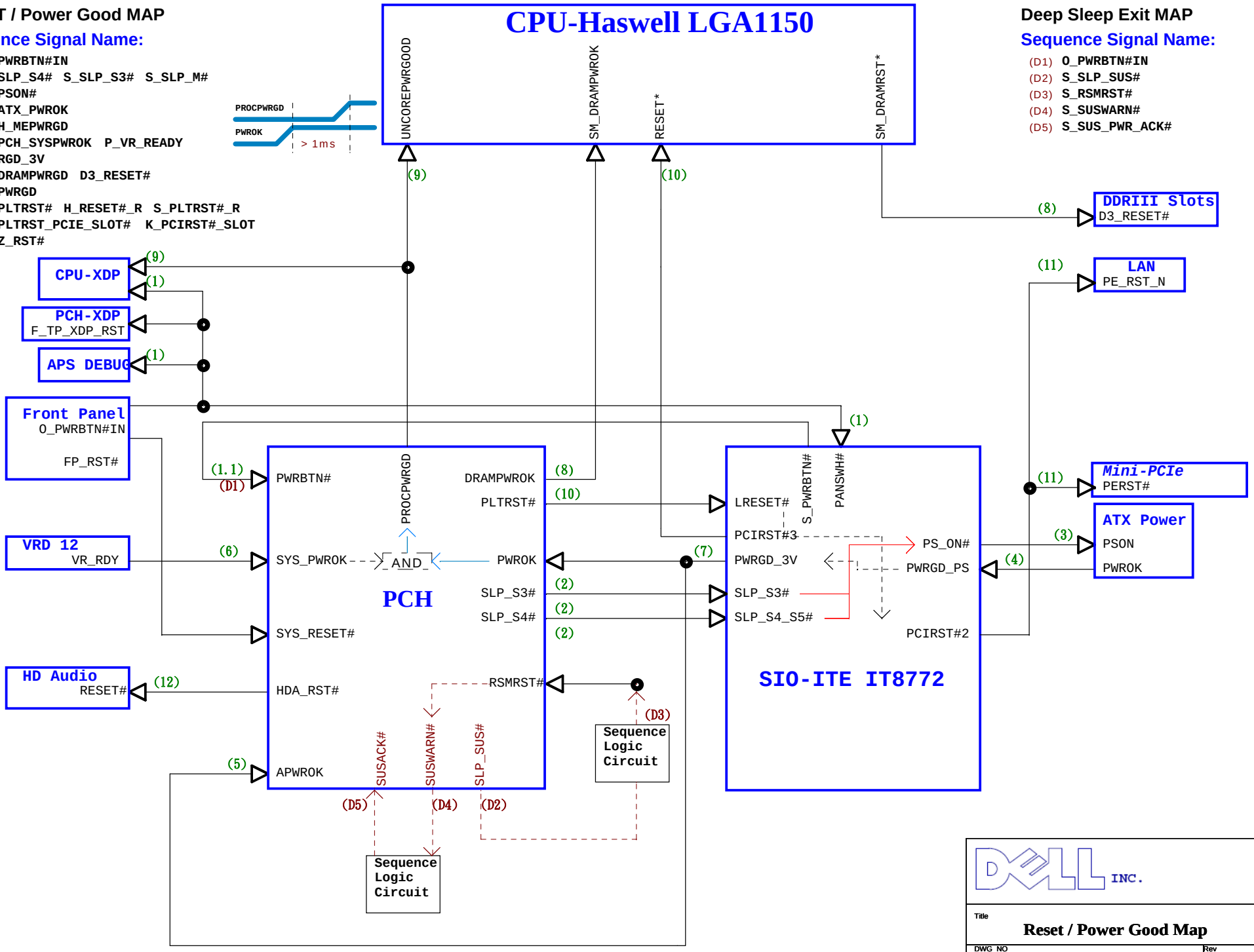
Sequence Signal Name:

(1) O_PWRBTN#IN
(2) S_SLP_S4# S_SLP_S3# S_SLP_M#
(3) O_PSON#
(4) B_ATX_PWROK
(5) PCH_MEPWRGD
(6) S_PCH_SYSPWROK P_VR_READY
(7) PWRGD_3V
(8) H_DRAMPWRGD D3_RESET#
(9) H_PWRGD
(10) S_PLTRST# H_RESET#_R S_PLTRST#_R
(11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
(12) A_Z_RST#

Deep Sleep Exit MAP

Sequence Signal Name:

(D1) O_PWRBTN#IN
(D2) S_SLP_SUS#
(D3) S_RSMRST#
(D4) S_SUSWARN#
(D5) S_SUS_PWR_ACK#



DELL INC.

Title: **Reset / Power Good Map**

DWG NO: *Goodyear*

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 6 of 57

STRAPPING Table

CPU side

CFG[19:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[3]	PCI Express* Static x4 Lane Numbering Reversal	1 = Normal operation Default 0 = Lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

SIO IT8772E/EX

PIN NAME	NET		Strapping description	
JP1 Pin23	JP1	1	EUP	
		0	DSW	DEFAULT
JP2 Pin57	O_RTS1#_R	1	Disable WDT to reset PWRGD	DEFAULT
		0	Enable WDT to reset PWRGD	
JP4 Pin61	O_DTR1#_R	1	Disable K8 power sequence function	DEFAULT
		0	Enable K8 power sequence function	
JP3 Pin59	O_TXD1_R	1	The default value of EC Index 63h/6Bh/73h is 80h	DEFAULT
		0	The default value of EC Index 63h/6Bh/73h is 00h	
JP8 Pin30	S_SLP_S3#	1	RSMRST# output detected by 3VSB	DEFAULT
		0	RSMRST# output detected by SYS_3VSB	

PCH

No Reboot Mode

SPKR (IN-PD)	Description	
High	No reboot mode: Enable	
Low	No reboot mode: Disable	DEFAULT

Topblock Swap Mode

GPIO55 (IN-PU)	Description	
High	Topblock swap mode: Disable	DEFAULT
Low	Topblock swap mode: Enable	

Boot BIOS Destination Selection

GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI

ME Disable (Flash overide)

HDA_SDO	Description	
High	ME Disable (Flash overide): Enable	
Low	ME Disable (Flash overide): Disable	DEFAULT

TLS Confidentiality

SAAT3GP/ GPIO37	Description	
High	ME Crypto TLS cipher suite with confidentiality	
Low	ME Crypto TLS cipher suite with no confidentiality	DEFAULT

On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PU)	Description	
High	Regulator is enabled.	DEFAULT

DMI Rx Termination

GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage

DELL INC.

Title: GPIO/IRQ/IDSEL Table

DWG NO: Goodyear

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 7 of 57

GPIO	Type	Power Well	Default	IN-PU/PD	Mainboby / BOD	
					EX-PU/PD	Schematic net name
GPIO[0]	I/O	Core	GPI		10K pull-up to +3V	S_PECI_REQ#
GPIO[1]	I/O	Core	GPI	20K IN-PU (Only on TACH1)	10K pull-up to +3V(dummy) 1K pull-down to GND	S_GPI_CHASSIS_ID0
GPIO[2]	I/OD	Core	GPI	-	-	V_DDSP_D_HPD
GPIO[3]	I/OD	Core	GPI	-	-	V_DDSP_C_HPD
GPIO[4]	I/OD	Core	GPI	-	8.2K pull-up to +3V	V_GPI_VGA_CBL_DET#
GPIO[5]	I/OD	Core	GPI	-	8.2K pull-up to +3V	PCIE_MINI_CPPE_DETECT#
GPIO[6]	I/O	Core	GPI	20K IN-PU (Only on TACH2)	10K pull-up to +3V	S_GPI_PCH_HS_DET#
GPIO[7]	I/O	Core	GPI	20K IN-PU (Only on TACH3)	10K pull-up to +3V(dummy) 200 pull-down to GND	S_GPI_SKU2
GPIO[8]	I/O	Suspend	GPO	20K IN-PU	use as TP	S_TP_GP8
GPIO[9]	I/O	Suspend	Native	-	use as OC5# 8.2K pull-up to +3V_S5(dummy)	U_USB_OC_R_#5
GPIO[10]	I/O	Suspend	Native	-	10K pull-up to +3V_S5	U_USB_OC_R_#6
GPIO[11]	I/O	Suspend	Native	-	10K pull-up to +3V_S5	X1_WAKE#_2
GPIO[12]	I/O	Suspend	Native	-	10K pull-up to +3V_LAN (dummy) 4.7K pull-down to GND(dummy)	L_LAN_DISABLE#(H=Disable L
GPIO[13]	I/O	Suspend	GPI	-	10K pull-up to +3V_S5	X1_WAKE#_1
GPIO[14]	I/O	Suspend	Native	-	8.2K pull-up to +3V_S5	GPO_WLOM
GPIO[15]	I/O	Suspend	GPO	20K IN-PU	1K pull-up to +3V_S5	S_PCH_GP15
GPIO[16]	I/O	Core	GPI	-	10K pull-up to +3V 10K pull-down to GND	H_SKTOCC_R_#
GPIO[17]	I/O	Core	GPI	20K IN-PU (Only on TACH0)	10K pull-up to +3V(dummy) 1K pull-down to GND	S_GPI_CHASSIS_ID1
GPIO[19]	I/O	Core	GPI	20K IN-PU	10K pull-up to +3V(dummy) 1K pull-down to GND(dummy)	S_SATA1GP
GPIO[20]	I/O	Core	Native	-	10K pull-up to +3V 10K pull-down to GND(dummy)	S_FLEXBAY_HDR_CBL_DET#
GPIO[21]	I/O	Core	GPI	-	10K pull-up to +3V(dummy) 10K pull-down to GND	S_GPI_BRD_REV0
GPIO[22]	I/O	Core	GPI	-	1K pull-up to +3V 4.7K pull-down to GND(dummy)	S_PCH_CONFIG_JUMPER
GPIO[23]	I/O	Core	Native	20K IN-PU	10K pull-up to +3V(dummy)	L_DRQ1#
GPIO[24]	I/O	Suspend	GPO	-	100K pull-up to +3V_S5	H_SKTOCC#
GPIO[27]	I/O	Deep Sleep	GPO	20K IN-PU	10K pull-up to +3V_DUAL 1K pull-down to GND(dummy)	S_GP27_PD
GPIO[28]	I/O	Suspend	GPO	20K IN-PU	10K pull-up to +3V_S5 1K pull-down to GND(dummy)	S_PCH_GP28_PU
GPIO[29]	I/O	Suspend	GPI	-	1K pull-up to +3V_S5(dummy)	S_SLP_LAN#
GPIO[30]	I/O	Deep Sleep	Native	-	10K pull-up to +3V_DUAL(dummy) 1K pull-down to GND(dummy)	S_SUSWARN#
GPIO[31]	I/O	Deep Sleep	GPI	TBD IN-PD	8.2K pull-up to +3V_DUAL	S_PSWD_CLR
GPIO[32]	I/O	Core	GPO	-	10K pull-up to +3V(SKU) 220 pull-down to GND(SKU)	S_GPI_SKU0
GPIO[33]	I/O	Core	GPO	-	use as TP	TPS30
GPIO[34]	I/O	Core	GPI	-	10K pull-up to +3V	PCH_GPI034
GPIO[35]	I/O	Core	GPO	-	10K pull-up to +3V(SKU) 220 pull-down to GND(SKU)	S_GPI_SKU1
GPIO[36]	I/O	Core	GPI	20K IN-PD	use as TP	TPS27
GPIO[37]	I/O	Core	GPI	20K IN-PD	use as TP	TPS39
GPIO[38]	I/O	Core	GPI	-	10K pull-up to +3V(dummy) 10K pull-down to GND	S_GPI_CHASSIS_ID2
GPIO[39]	I/O	Core	GPI	-	10K pull-up to +3V	A_FP_PRES#
GPIO[40]	I/O	Suspend	Native	-	use as OC1#	U_USB_OC_R_#1
GPIO[41]	I/O	Suspend	Native	-	use as OC2#	U_USB_OC_R_#2
GPIO[42]	I/O	Suspend	Native	-	use as OC3#	U_USB_OC_R_#3
GPIO[43]	I/O	Suspend	Native	-	use as OC4# 8.2K pull-up to +3V(dummy)	U_USB_OC_R_#4
GPIO[44]	I/O	Suspend	Native	TBD IN-PD	10K pull-up to +3V_S5 10K pull-down to GND(dummy)	S_INTRUD_CBL_DET#
GPIO[45]	I/O	Suspend	Native	-	10K pull-up to +3V_S5 10K pull-down to GND(dummy)	O_COM_SER2_DET#
GPIO[46]	I/O	Suspend	Native	20K IN-PU	10K pull-up to +3V_S5(dummy) 1K pull-down to GND	S_GPI_BRD_REV1
GPIO[48]	I/O	Core	GPI	-	10K pull-up to +3V	S_GPIO48_PU
GPIO[49]	I/O	Core	GPI	-	8.2K pull-up to +3V	TMIN_SHIFT
GPIO[50]	I/O	Core	Native	-	8.2K pull-up to +3V	K_REQ#1
GPIO[51]	I/O	Core	Native	20K IN-PU	1K pull-up to +3V(dummy) 1K pull-down to GND(dummy)	K_GNT#1
GPIO[52]	I/O	Core	Native	-	8.2K pull-up to +3V	K_REQ#2
GPIO[53]	I/O	Core	Native	20K IN-PU	1K pull-down to GND(dummy)	K_GNT#2
GPIO[54]	I/O	Core	Native	-	8.2K pull-up to +3V	K_REQ#3
GPIO[55]	I/O	Core	Native	20K IN-PU	4.7K pull-down to GND(dummy)	K_GNT#3
GPIO[57]	I/O	Suspend	GPI		10K pull-up to +3V_S5(dummy) 47K pull-down to GND	S_GPIO57_PD
GPIO[58]	I/O	Suspend	Native		10K pull-up to +3V_S5	S_SMLINK1_CLK
GPIO[59]	I/O	Suspend	Native	-	use as OC0#	U_USB_OC_R_#0
GPIO[60]	I/O	Suspend	Native		2.2K pull-up to +3V_S5	GPIO_WIRELESS_DISABLE#
GPIO[61]	I/O	Suspend	Native	-	8.2K pull-up to +3V_S5(dummy)	S_LPCPD#
GPIO[62]	I/O	Suspend	Native		use as switch	S_SUSCLK
GPIO[63]	I/O	Suspend	Native	-	10K pull-up to +3V_S5	S_PCIAUX_GATE
GPIO[64]	I/O	Core	Native	20K IN-PD	use as TP	S_TP_CLKOUTFLEX0
GPIO[65]	I/O	Core	Native	20K IN-PD		C_14M_SIO_R
GPIO[66]	I/O	Core	Native	20K IN-PD	use as TP	S_TP_CLKOUTFLEX2
GPIO[67]	I/O	Core	Native	20K IN-PD	-	C_14M_TPM_R
GPIO[69]	I/O	Core	GPI	20K IN-PU (Only on TACH4)	10K pull-up to +3V(dummy) 220 pull-down to GND	S_GPI_BRD_REV2
GPIO[68]	I/O	Core	GPI	20K IN-PU (Only on TACH5)	10K pull-up to +3V	O_PRT_DET#
GPIO[70]	I/O	Core	GPI	20K IN-PU (Only on TACH6)	8.2K pull-up to +3V	S_FP_CHAS_DET#
GPIO[71]	I/O	Core	GPI	20K IN-PU (Only on TACH7)	10K pull-up to +3V	
GPIO[72]	I/O	Suspend	Native (Mobile Only)	20K IN-PU	10K pull-up to +3V_S5	S_PCH_GP72_PU
GPIO[74]	I/O	Suspend	Native		10K pull-up to +3V_S5	S_MFG_MODE_OR
GPIO[75]	I/O	Suspend	Native	-	10K pull-up to +3V_S5	S_SMLINK1_DATA

GPIO	PIN NAME	Power well	Buffer Type	EX-PU/PD	Signal Name
GP000	(DIAG_LED3#) GP000	VTR	IO	NA	O_DIAG_LED3#
GP001	(DIAG_LED1#) GP001	VTR	IO	NA	O_DIAG_LED1#
GP002	(DIAG_LED2#) GP002	VTR	IO	NA	O_DIAG_LED2#
GP003	(DIAG_LED4#) GP003	VTR	IO	NA	O_DIAG_LED4#
GP004	GP004	VTR	IO	NA	NC
GP005	(H_CPURST#) GP005 / PECI_REQUEST#	VTR	IO/OD	10K pull-up to +3V	O_PECI_REQ#
GP006	YELLOW# / GP006	VTR	O/IO	NA	O_YELLOW#
GP007	GREEN# / GP007	VTR	O/IO	NA	O_GREEN#
GP010	SMBDAT2 / GP010	VTR	IOD/IO	8.2k pull-up to +3V_DUAL(dummy)	S_SMLINK1_DATA_R
GP011	SMBCLK2 / GP011	VTR	IOD/IO	8.2k pull-up to +3V_DUAL (dummy)	S_SMLINK1_CLK_R
GP012	GP012	VTR	IO	8.2k pull-up to +3V_DUAL	SPI_DI
GP013	GP013	VTR	IO	NA	NC
GP014	(TMIN_SHIFT) GP014	VTR	IO	8.2k pull-up to +3V	TMIN_SHIFT
GP015	PWRBTN# / GP015	VTR	IIO	1k pull-up to +3V_DUAL	O_PWRBTN#IN
GP016	PROCHOT_IN#/PROCHOT_OUT#/GP016	VTR	IO/OD/GO	51ohm pull-up to +1P05V_VCCIO	H_PROCHOT#
GP017	TACH1 / GP017	VTR	IIO	1k pull-up to +3V	O_SEN_CPUFAN
GP020	TACH2 / GP020	VTR	IIO	1k pull-up to +3V	O_SEN_CHAFAN
GP021	TACH3 / GP021	VTR	IIO	NA	NC
GP022	PWM1 / GP022	VTR	OD/IO	4.7k pull-up to +3V	O_CPUFAN_PWM
GP023	PWM2 / GP023	VTR	OD/IO	4.7k pull-up to +3V	O_CHAFAN_PWM
GP024	PWM3 / GP024	VTR	OD/IO	NA	NC
GP025	(FP_CBL_OPT#) GP025	VTR	IO	8.2k pull-up to +3V_S5	O_FP_CBL_DET#
GP026	PCI_RST_SYS#/ GP026	VTR	O/IO	NA	K_FLITPST_PCIE_SLOT#
GP027	PCI_RST_SLOT5#/ GP027	VTR	O/IO	NA	H_RESET#
GP030	PS_ON# / GP030	VTR	OD/IO	4.7k pull-up to +5VSB	O_PSON#
GP031	(PC_SPWR_DET) GP031	VTR	IO	8.2k pull-up to +3V_DUAL	O_AUD_PCSPWR_DET#
GP032	GP032	VTR	IO	NA	NC
GP033	PWR_GOOD_3V / GP033	VTR	O/IO	NA	PWRGD_3V
GP034	RSMRST# GP034	VTR	O/IO	10k pull-down to GND	O_RSMRST#
GP035	GP035	VTR	IO	8.2k pull-up to +3V_DUAL	O_BC_CLK
GP036	GP036 / SMB_CLK1	VTR	IO/IOD	8.2k pull-up to +3V_DUAL (dummy)	S_SMBCLK_PCI_R
GP040	GP040 / SMB_DAT1	VTR	IO/IOD	8.2k pull-up to +3V_DUAL (dummy)	S_SMBDATA_PCI_R
GP041	GP041 / IO_PME#	VTR	IO/GD	10k pull-up to +3V_S5	O_IO_PME#
GP042	GP042 / ORVDEN)	VTR	IO/O	100k pull-up to +3V_DUAL(dummy)	F_ERATA_DET#
GP043	DCD1# / GP043 / MCDAT	VTR	IIO/O	NA	O_DCD1#_R
GP044	DSR1# / GP044 / MCCLK	VTR	IIO/O	NA	O_DSR1#_R
GP045	RXD1 / GP045	VTR	IIO	NA	O_RXD1_R
GP046	RTS1# / GP046	VTR	O/IO	NA	O_RTS1#_R
GP047	(5V_PRSNT) GP047 / TXD1	VTR	IO/O	NA	O_TXD1_R
GP050	CTS1# / GP050	VTR	IIO	NA	O_CTS1#_R
GP051	DTR1# (TEST_EN) / GP051	VTR	O/IO	8.2k pull-up to +3V_DUAL(dummy) 20k pull-down to GND	O_DTR1#_R
GP052	RI1# / GP052	VTR	IIO	NA	O_RI1#_R
GP053	GP053 / DCD2#	VTR	IO/I	2.2k pull-up to +3V	O_DCD2#_R
GP054	GP054 / DSR2#	VTR	IO/I	2.2k pull-up to +3V	O_DSR2#_R
GP055	GP055 / RXD2	VTR	IO/I	2.2k pull-up to +3V	O_RXD2_R
GP056	(PWR2_PRSNT) GP056 / RTS2#	VTR	IO/O	30k pull-up to +3V	O_RTS2#_R
GP057	(MB_REG_PG) GP057 / TXD2	VTR	IO/O	30k pull-up to +3V	O_TXD2_R
GP060	CP060 / CTS2#	VTR	IO/I	2.2k pull-up to +3V	O_CTS2#_R
GP061	(MEM_REG_PG) GP061 / DTR2#	VTR	IO/O	30k pull-up to +3V	O_DTR2#_R
GP062	GP062 / RI2#	VTR	IO/I	2.2k pull-up to +3V	O_RI2#_R
GP063	GP063 / KBORST#	VTR	O/IOD	10k pull-up to +3V	O_KB_RST#
GP064	GP064 / A20M	VTR	IO/OD	10k pull-up to +3V	O_GA20
GP065	SLP_S2# / GP065	VTR	IIO	NA	S_SLP_S2#
GP066	SLP_S4_S5# / GP066	VTR	IIO	NA	S_SLP_S4#
GP067	PWROD_NE / GP067	VTP	I/O	1k pull-up to +5V	B_ATX_PWROK
GP070	SPEAKER (DIAG_EN#) / GP070	VTR	O/IO	8.2K pull-up to +3V_DUAL(dummy) 8.25k pull-down to GND	O_SPEAKER
GP071	(SLP_M#) GP071 / IO_SMI#	VTR	IO/OD	NA	S_SLP_M#
GP072	PECI / (VSMB_CLK1 / GP072	VTR	PECI_IO/ODDR0	1k pull-up to +1P05V_VCCIO (dummy)	H_PECI_R
GP073	PECI_READY / (VSMB_DAT1 / GP073	VTR	PECI_IO/ODDR0	1k pull-up to +1P05V_VCCIO	O_GP73_PU

DELL INC.

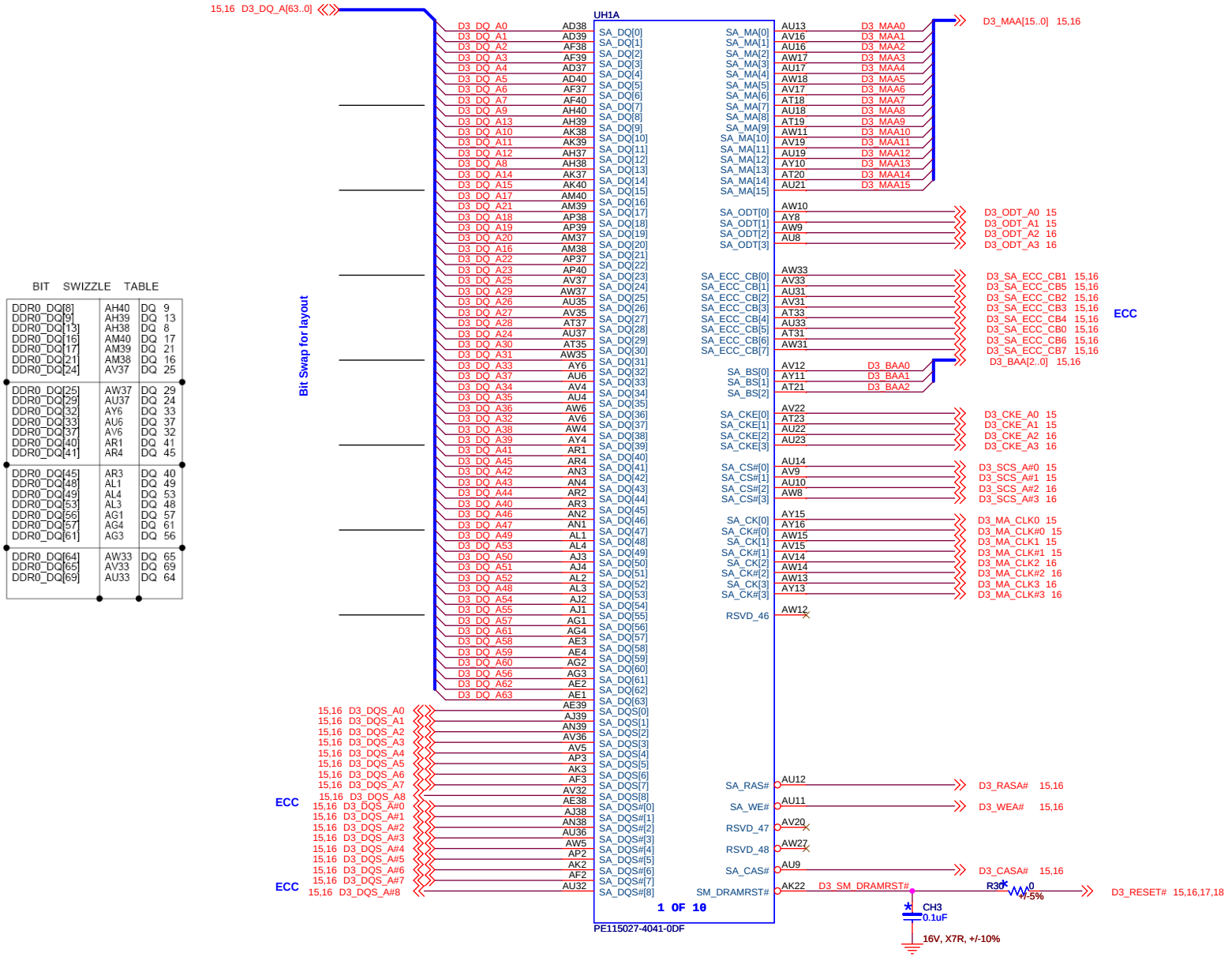
Title: **GPIO Table**

DWG NO: *Goodyear*

Rev: A00

Date: 星期三, 三月 20, 2013 Sheet 8 of 57

DDR3 CH-A



DELL INC.

Title

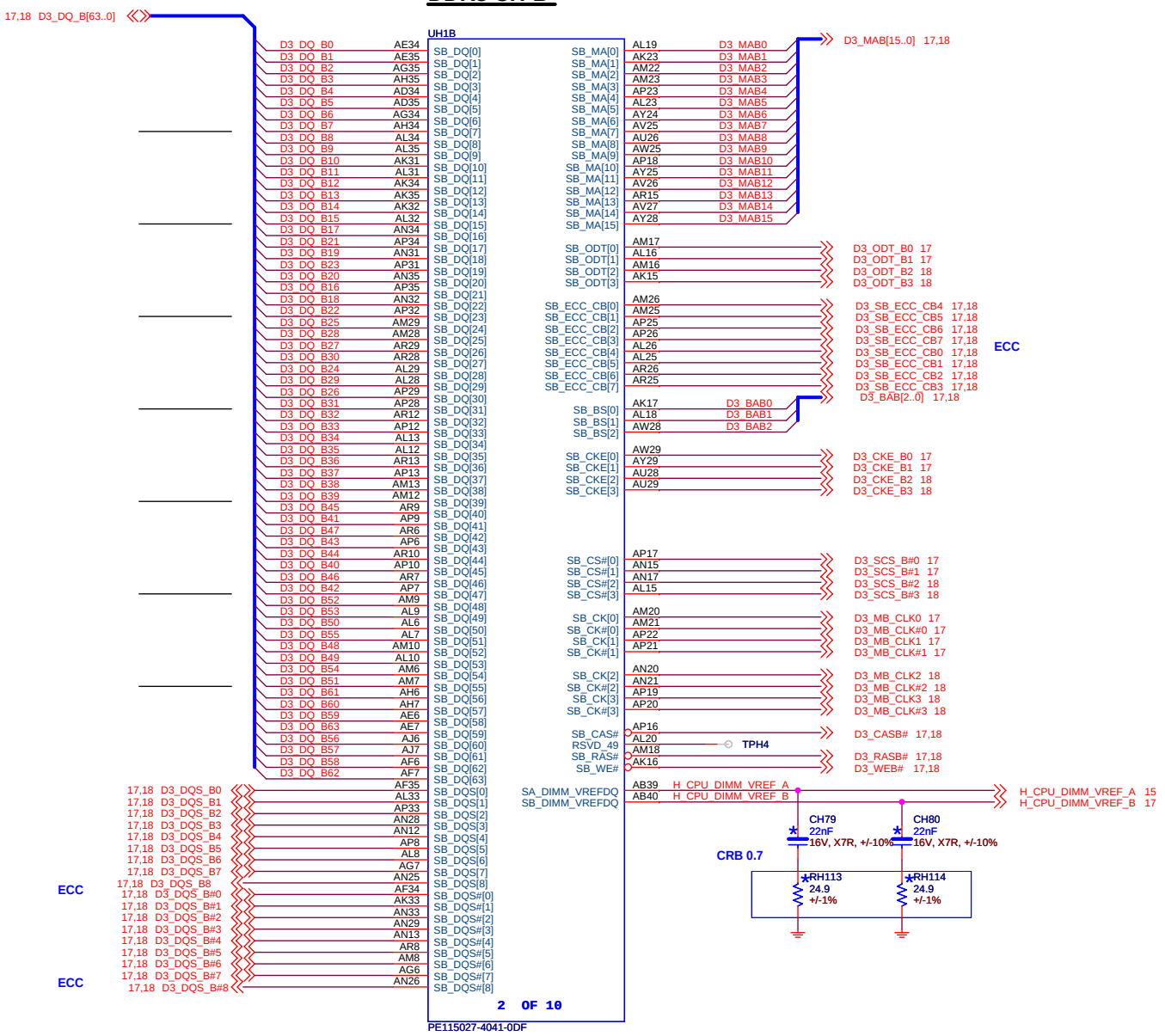
CPU-1: DDR3_CHA

DWG NO *Goodyear*

Rev X02

Date: 星期三, 二月 20, 2013 Sheet 9 of 57

DDR3 CH-B



DELL INC.

Title

CPU-2: DDR3_CHB

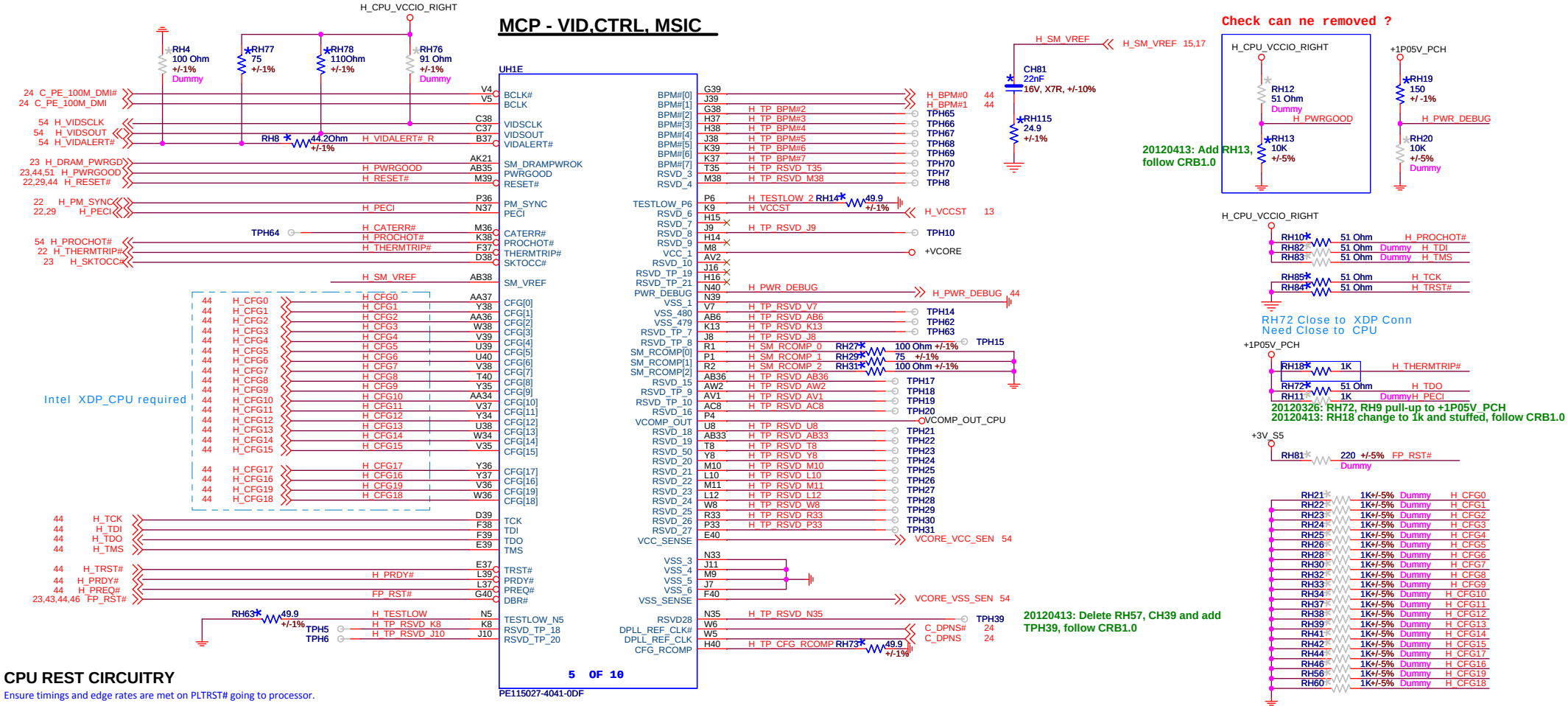
DWG NO

Goodyear

Rev A00

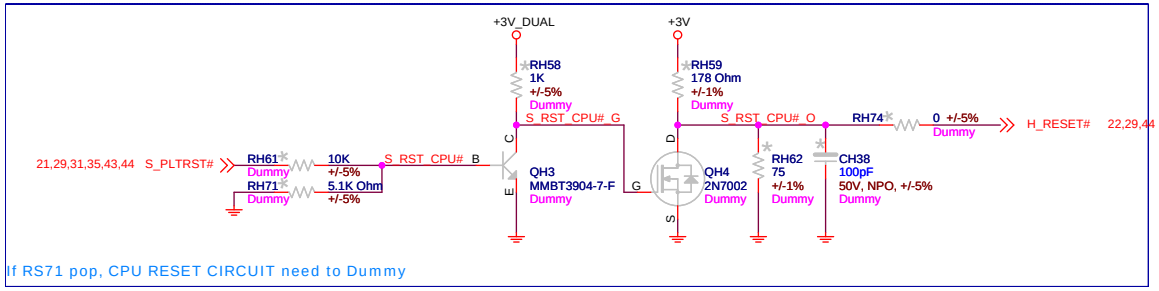
Date: 星期三, 二月 20, 2013 Sheet 10 of 57

MCP - VID,CTRL, MSIC

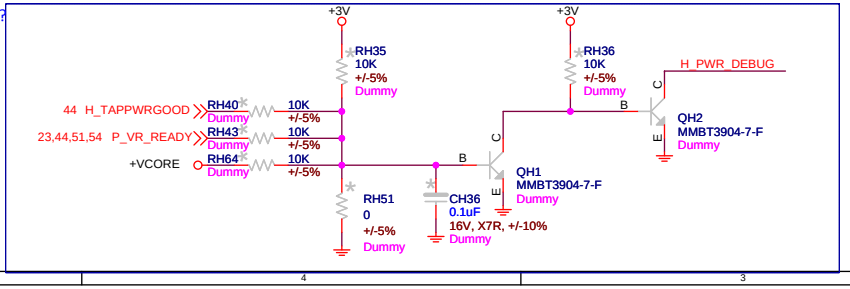


CPU REST CIRCUITRY

Ensure timings and edge rates are met on PLTRST# going to processor.



Check with Intel for this circuit necessary ??



DELL INC.

Title

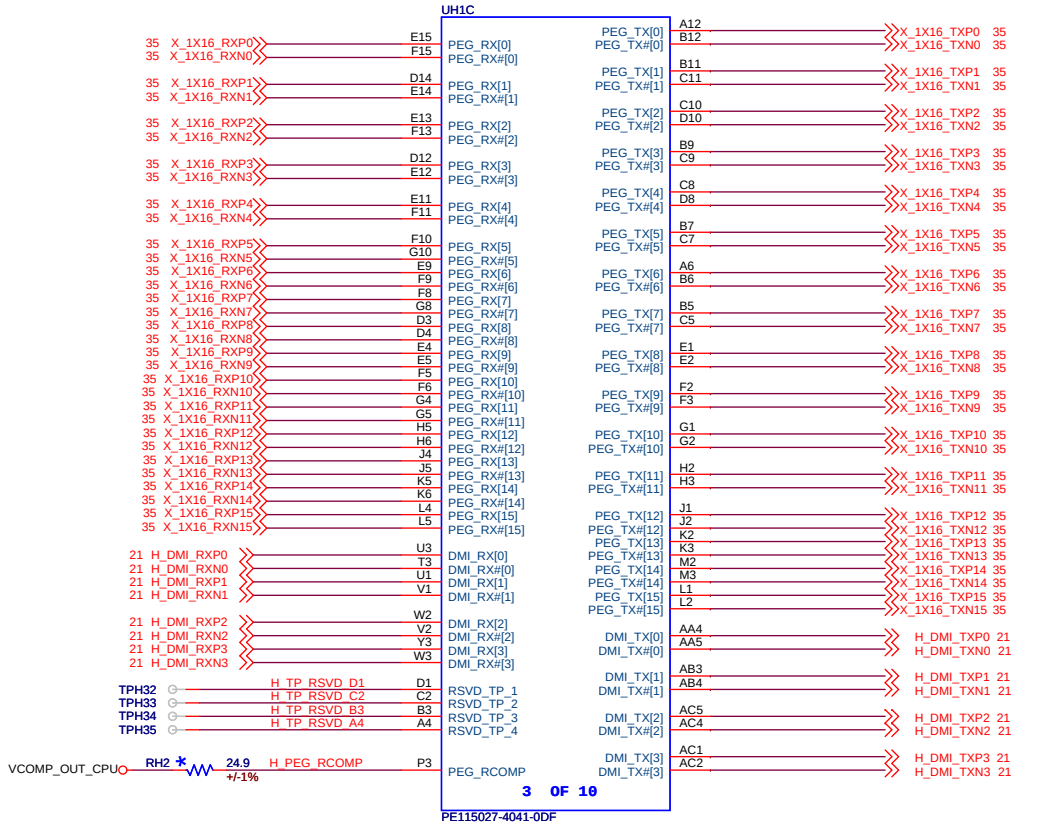
CPU-3: VID/MISC

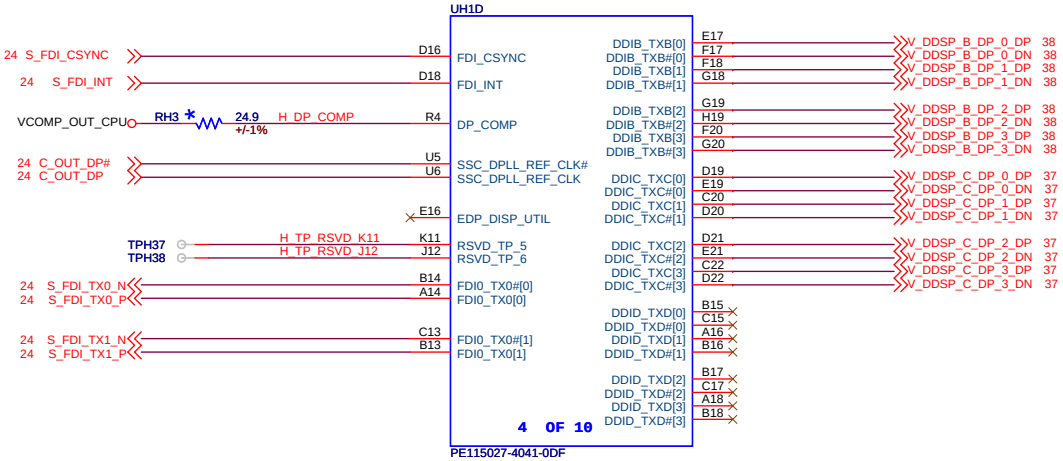
DWG NO

Goodyear

Rev A00

Date: 星期三, 二月 20, 2013 Sheet 11 of 57





Display Port

HDMI

DELL INC.

Title

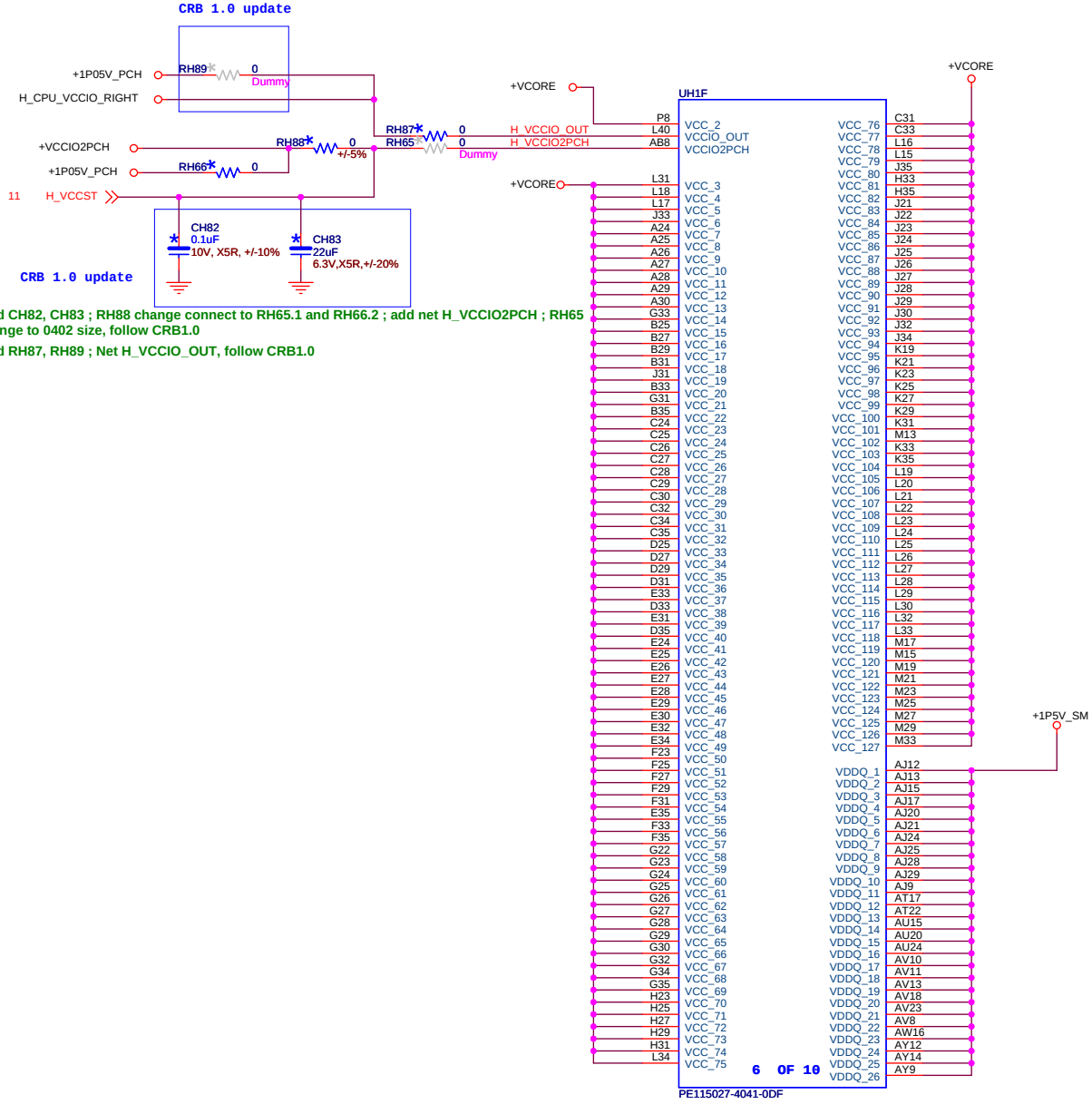
CPU-4: FDI/PCIe/DMI/DP

DWG NO

Goodyear

Rev A00

Date: 星期三, 二月 20, 2013 Sheet 12 of 57



20120413: Add CH82, CH83 ; RH88 change connect to RH65.1 and RH66.2 ; add net H_VCCIO2PCH ; RH65 and RH66 change to 0402 size, follow CRB1.0

20120413: Add RH87, RH89 ; Net H_VCCIO_OUT, follow CRB1.0

DELL INC.

Title

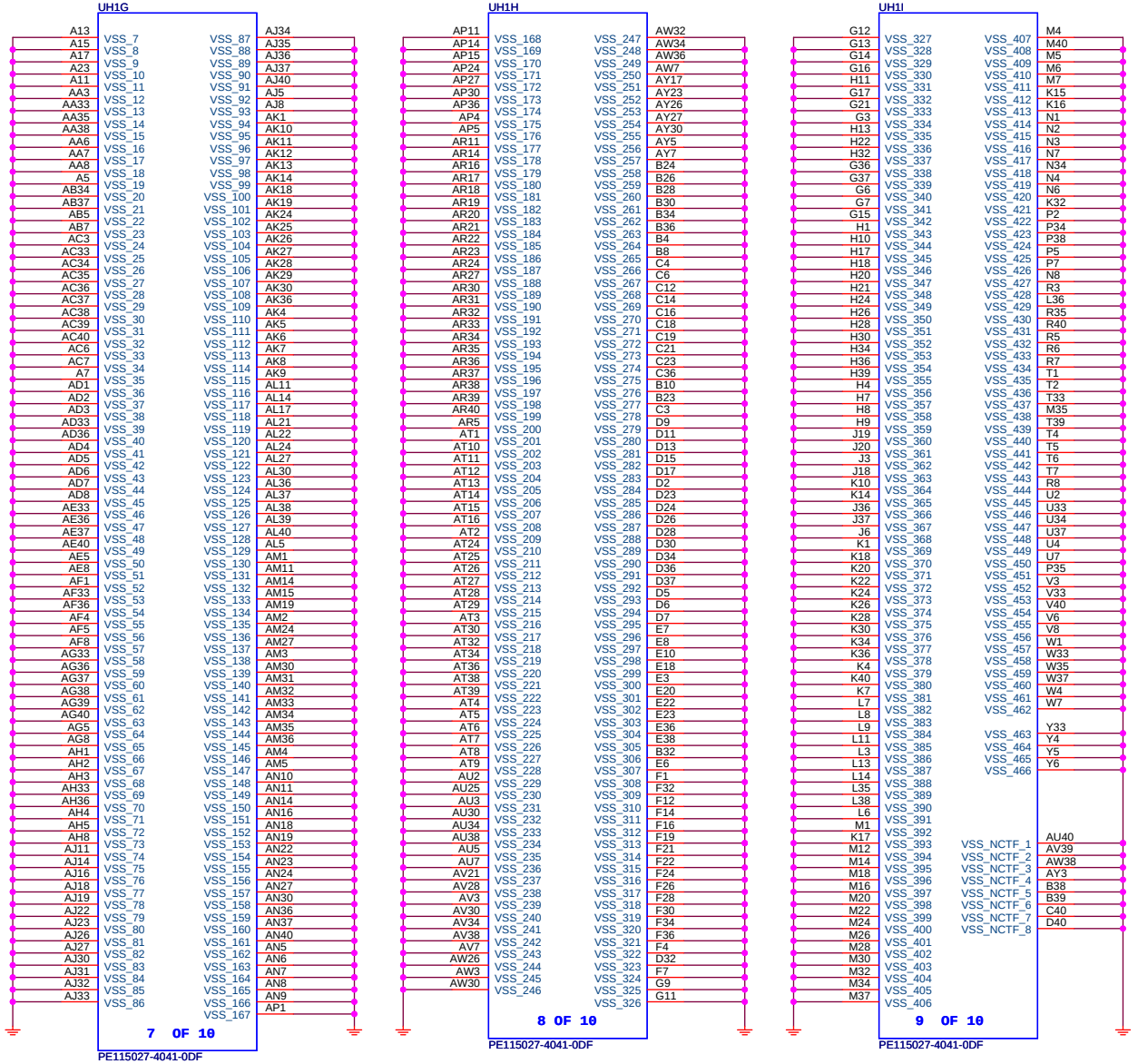
CPU-5: Vcore

DWG NO

Goodyear

Rev A00

Date: 星期三, 二月 20, 2013 Sheet 13 of 57



DELL INC.

Title

CPU-6: GND

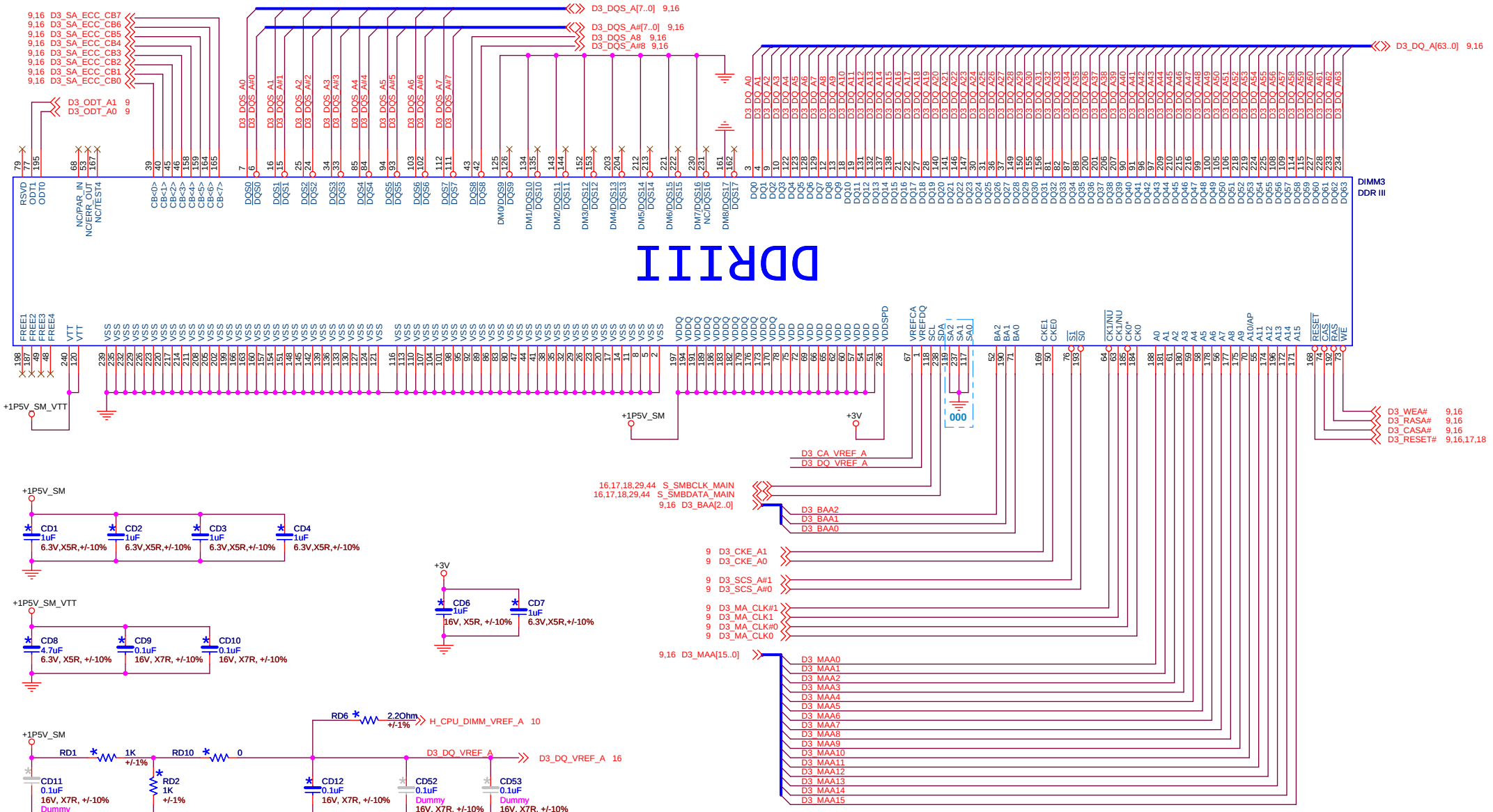
DWG NO

Goodyear

Rev A00

Date: 星期三, 二月 20, 2013 Sheet 14 of 57

CHANNEL A BANK 1
SMB ADDRESS:000



DELL INC.

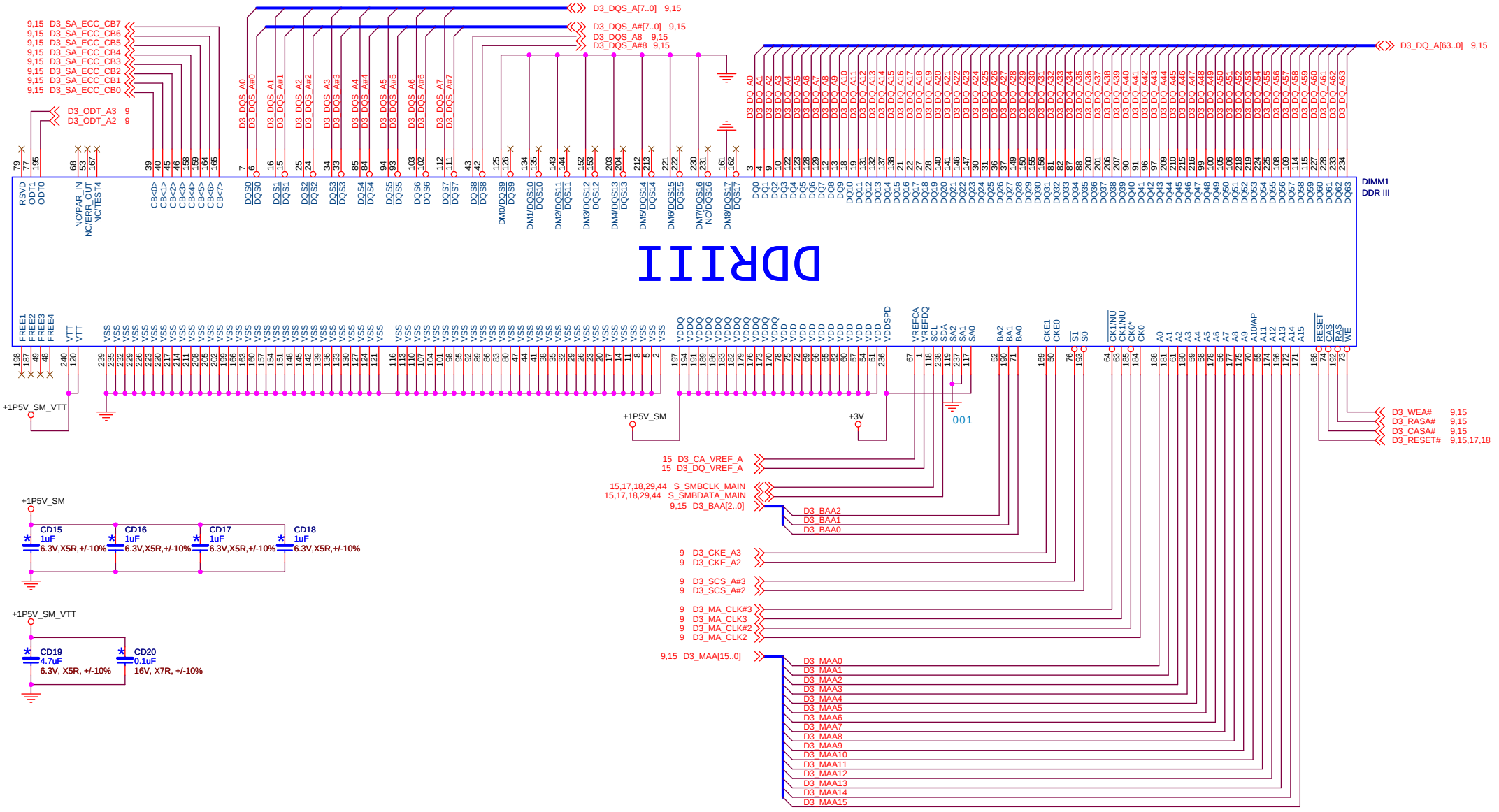
Title
DDR3 Conn: CHA_1 (DIMM3)

DWG NO
Goodyear

Rev
A00

Date: 星期三, 二月 20, 2013 Sheet 15 of 57

CHANNEL A BANK 2
SMB ADDRESS:001



DELL INC.

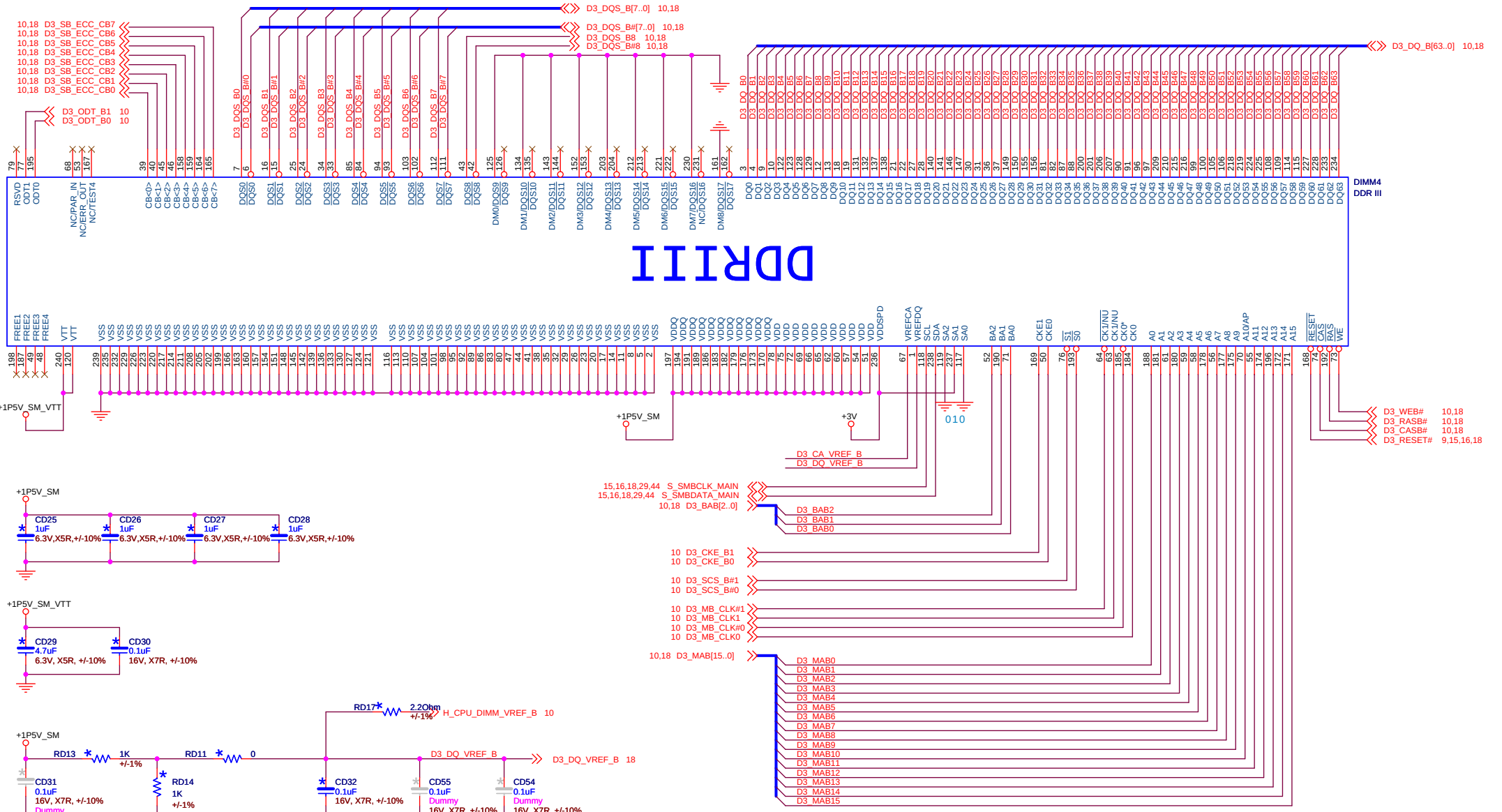
Title
DDR3 Conn: CHA_2 (DIMM1)

DWG NO
Goodyear

Rev
A00

Date: 星期三, 二月 20, 2013 Sheet 16 of 57

CHANNEL B BANK 1
SMB ADDRESS:010



DELL INC.

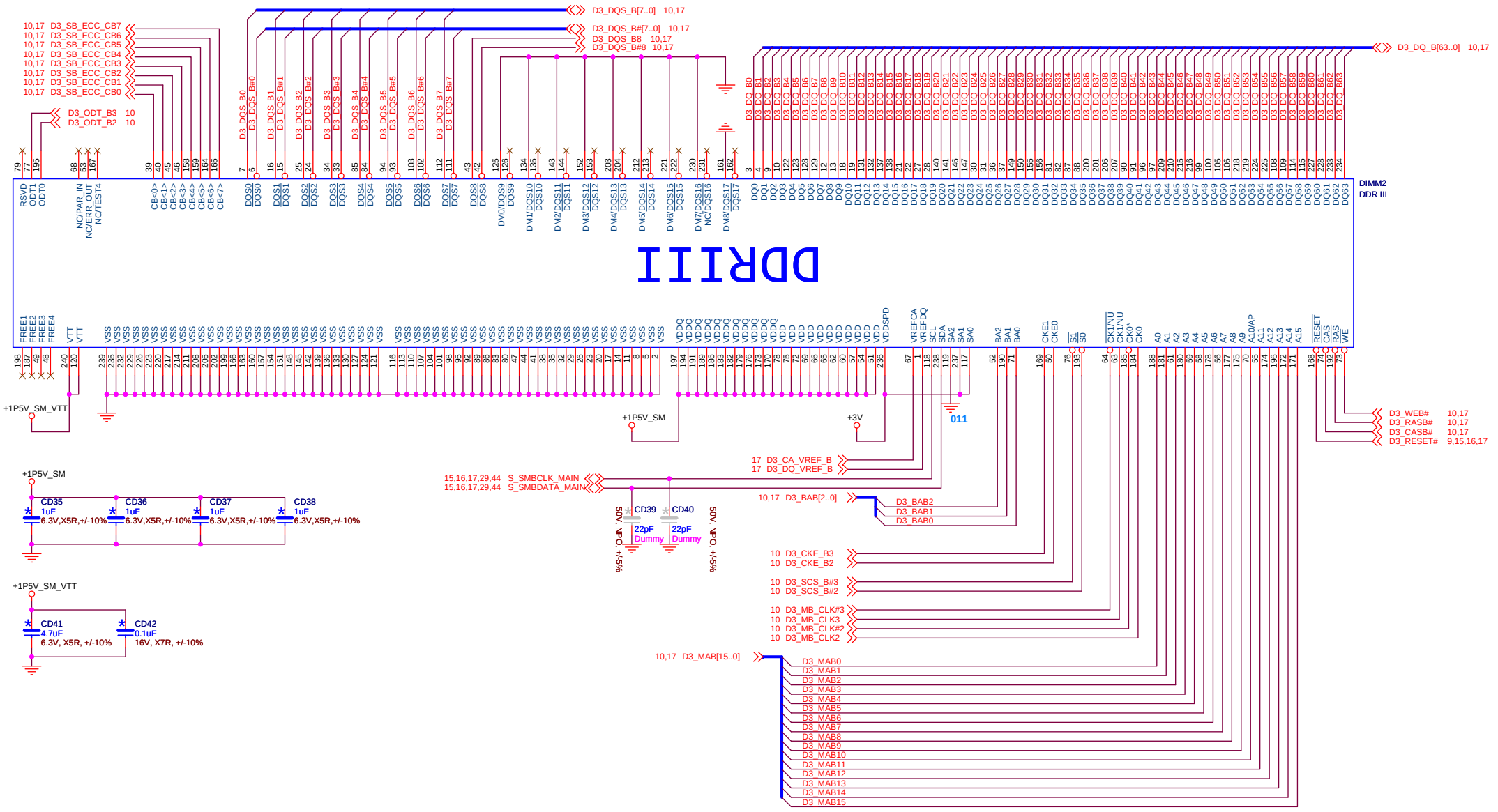
Title
DDR3 Conn: CHB_1 (DIMM4)

DWG NO
Goodyear

Rev
A00

Date: 星期三, 二月 20, 2013 Sheet 17 of 57

CHANNEL B BANK 2
SMB ADDRESS:011



DELL INC.

Title
DDR3 Conn: CHB_2 (DIMM2)

DWG NO
Goodyear

Rev
A00

Date: 星期三, 二月 20, 2013 Sheet 18 of 57

DELL INC.

Title

Label

DWG NO

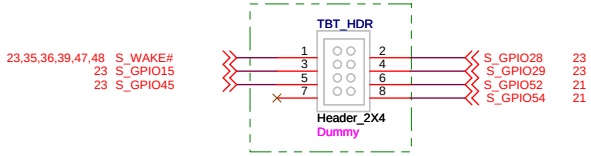
Goodyear

Rev

A00

Date: 星期三, 二月 20, 2013 Sheet 19 of 57

20120626: Add TBT_HDR
20120703: TBT_HDR compoment
REMARK cahnge to Remark



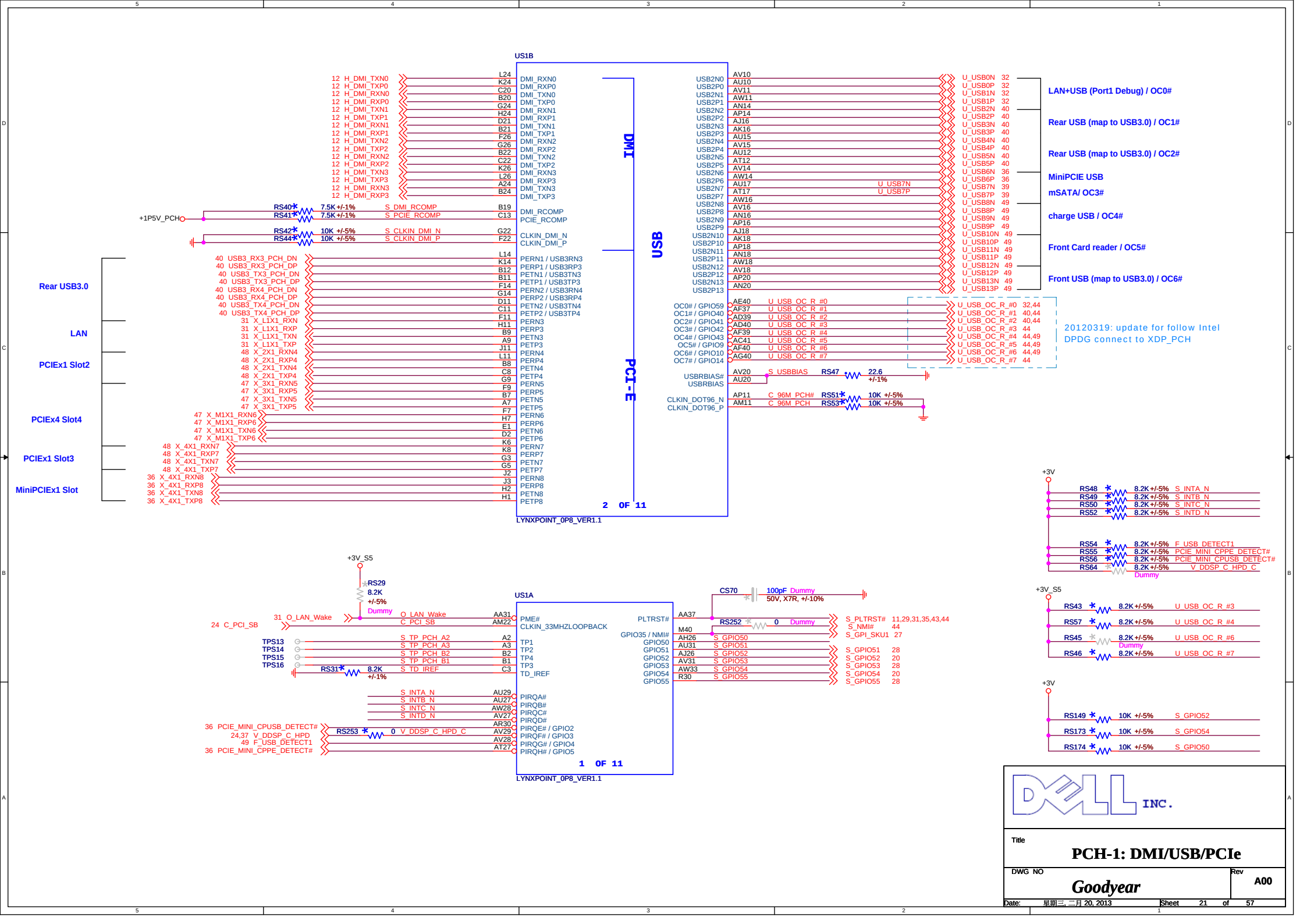
DELL INC.

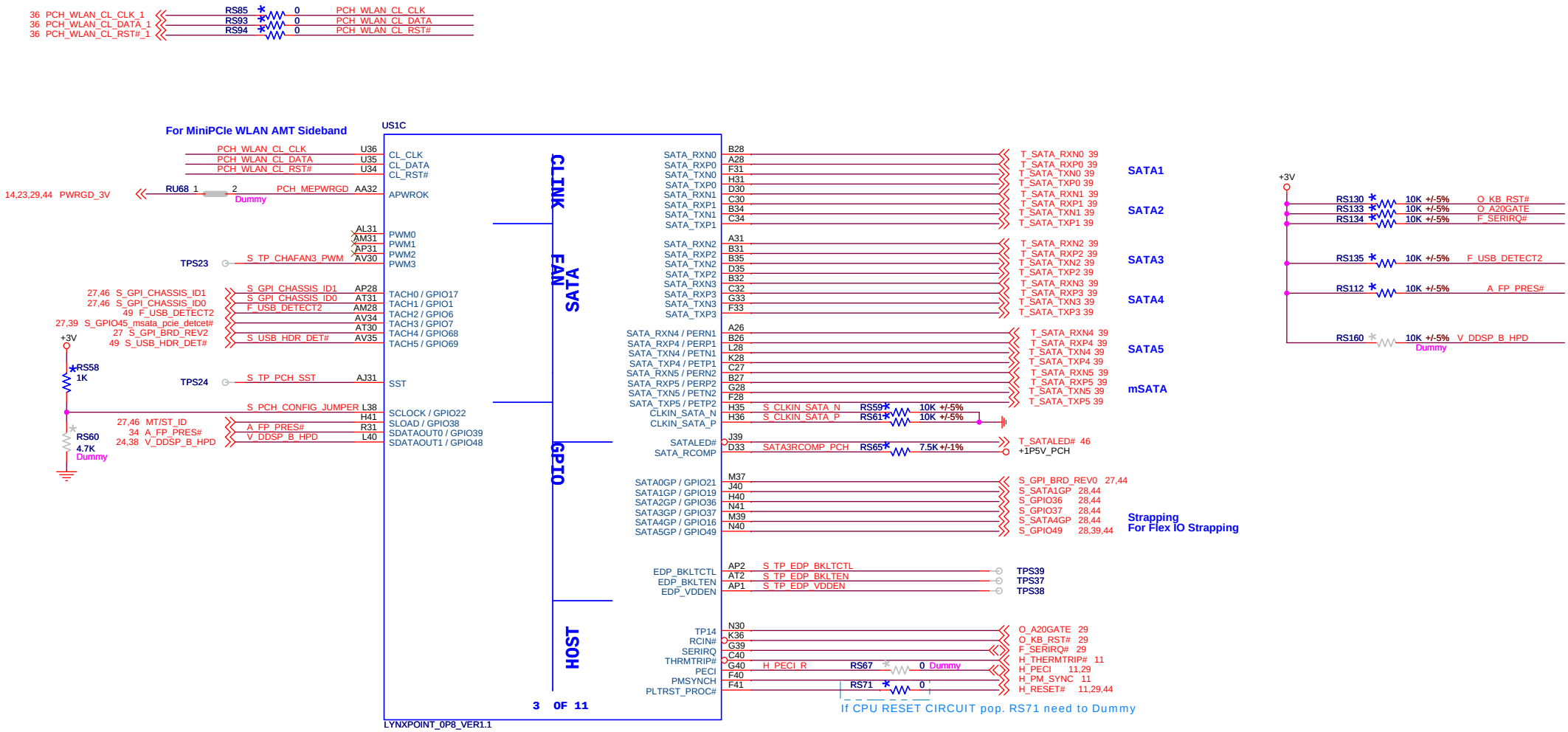
Title
TBD

DWG NO
Goodyear

Rev
A00

Date: 星期三, 二月 20, 2013 Sheet 20 of 57


US1B
DMI
USB
PCI-E
2 OF 11
LYNXPOINT_0P8_VER1.1
DMI_RXN0
DMI_RXP0
DMI_TXN0
DMI_TXP0
DMI_RXN1
DMI_RXP1
DMI_TXN1
DMI_TXP1
DMI_RXN2
DMI_RXP2
DMI_TXN2
DMI_TXP2
DMI_RXN3
DMI_RXP3
DMI_TXN3
DMI_TXP3
DMI_RCOMP
PCIE_RCOMP
CLKIN_DMI_N
CLKIN_DMI_P
PERN1 / USB3RN3
PERP1 / USB3RP3
PETN1 / USB3TN3
PETP1 / USB3TP3
PERN2 / USB3RN4
PERP2 / USB3RP4
PETN2 / USB3TN4
PETP2 / USB3TP4
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
USB2N0
USB2P0
USB2N1
USB2P1
USB2N2
USB2P2
USB2N3
USB2P3
USB2N4
USB2P4
USB2N5
USB2P5
USB2N6
USB2P6
USB2N7
USB2P7
USB2N8
USB2P8
USB2N9
USB2P9
USB2N10
USB2P10
USB2N11
USB2P11
USB2N12
USB2P12
USB2N13
USB2P13
OC0# / GPIO59
OC1# / GPIO40
OC2# / GPIO41
OC3# / GPIO42
OC4# / GPIO43
OC5# / GPIO9
OC6# / GPIO10
OC7# / GPIO14
USBRBIAS#
USBRBIAS
CLKIN_DOT96_N
CLKIN_DOT96_P
U_USB0N 32
U_USB0P 32
U_USB1N 32
U_USB1P 32
U_USB2N 40
U_USB2P 40
U_USB3N 40
U_USB3P 40
U_USB4N 40
U_USB4P 40
U_USB5N 40
U_USB5P 40
U_USB6N 36
U_USB6P 36
U_USB7N 39
U_USB7P 39
U_USB8N 49
U_USB8P 49
U_USB9N 49
U_USB9P 49
U_USB10N 49
U_USB10P 49
U_USB11N 49
U_USB11P 49
U_USB12N 49
U_USB12P 49
U_USB13N 49
U_USB13P 49
U_USB7N
U_USB7P
U_USB_OC_R_#0 32,44
U_USB_OC_R_#1 40,44
U_USB_OC_R_#2 40,44
U_USB_OC_R_#3 44
U_USB_OC_R_#4 44,49
U_USB_OC_R_#5 44,49
U_USB_OC_R_#6 44,49
U_USB_OC_R_#7 44
S_USBBIAS
RS47 22.6 +/-1%
C_96M_PCH#
C_96M_PCH
RS51 10K +/-5%
RS53 10K +/-5%
LAN+USB (Port1 Debug) / OC0#
Rear USB (map to USB3.0) / OC1#
Rear USB (map to USB3.0) / OC2#
MiniPCIE USB
mSATA/ OC3#
charge USB / OC4#
Front Card reader / OC5#
Front USB (map to USB3.0) / OC6#
20120319: update for follow Intel DPDG connect to XDP_PCH
Rear USB3.0
LAN
PCIEx1 Slot2
PCIEx4 Slot4
PCIEx1 Slot3
MiniPCIEx1 Slot
US1A
LYNXPOINT_0P8_VER1.1
1 OF 11
PME#
CLKIN_33MHZLOOPBACK
TP1
TP2
TP4
TP3
TD_IREF
PIRQA#
PIRQB#
PIRQC#
PIRQD#
PIRQE# / GPIO2
PIRQF# / GPIO3
PIRQG# / GPIO4
PIRQH# / GPIO5
PLTRST#
GPIO35 / NMI#
GPIO50
GPIO51
GPIO52
GPIO53
GPIO54
GPIO55
S_PLTRST# 11,29,31,35,43,44
S_NMI# 44
S_GPI_SKU1 27
S_GPIO50
S_GPIO51 28
S_GPIO52 20
S_GPIO53 28
S_GPIO54 20
S_GPIO55 28
CS70 100pF Dummy 50V, X7R, +/-10%
RS252 0 Dummy
RS29 8.2K +/-5% Dummy
O_LAN_Wake
C_PCI_SB
S_TP_PCH_A2
S_TP_PCH_A3
S_TP_PCH_B2
S_TP_PCH_B1
S_TD_IREF
RS31 8.2K +/-1%
S_INTA_N
S_INTB_N
S_INTC_N
S_INTD_N
RS253 0 V_DDSP_C_HPD_C
RS48 8.2K +/-5% S_INTA_N
RS49 8.2K +/-5% S_INTB_N
RS50 8.2K +/-5% S_INTC_N
RS52 8.2K +/-5% S_INTD_N
RS54 8.2K +/-5% F_USB_DETECT1
RS55 8.2K +/-5% PCIE_MINI_CPPE_DETECT#
RS56 8.2K +/-5% PCIE_MINI_CPUSB_DETECT#
RS64 8.2K +/-5% V_DDSP_C_HPD_C Dummy
RS43 8.2K +/-5% U_USB_OC_R_#3
RS57 8.2K +/-5% U_USB_OC_R_#4
RS45 8.2K +/-5% U_USB_OC_R_#6 Dummy
RS46 8.2K +/-5% U_USB_OC_R_#7
RS149 10K +/-5% S_GPIO52
RS173 10K +/-5% S_GPIO54
RS174 10K +/-5% S_GPIO50
+1P5V_PCH
RS40 7.5K +/-1% S_DMI_RCOMP
RS41 7.5K +/-1% S_PCIE_RCOMP
RS42 10K +/-5% S_CLKIN_DMI_N
RS44 10K +/-5% S_CLKIN_DMI_P
+3V_S5
+3V
TPS13
TPS14
TPS15
TPS16
DELL INC.
Title
PCH-1: DMI/USB/PCIe
DWG NO
Goodyear
Rev
A00
Date: 星期三, 二月 20, 2013
Sheet 21 of 57



DELL INC.

Title

PCH-2: SATA/HOST/GPIO

DWG NO

Goodyear

Rev A00

Date: 星期三, 二月 20, 2013 Sheet 22 of 57

GPIO_PCIE_RESET DEFAULT LOW. ACTIVE HIGH
THE SAME GPIO CANNOT BE USED IF THE HDA
INTERFACE IS 1.5V

20120703: S_GPIO13 rename to S_PCIE_RST.

20120703: Add RS199

US1D

LYNXPOINT_0P8_VER1.1

4 OF 11

AZALIA SPI JTAG(SUS)

Tmin_Shift --> PCH HOT for SIO FAN control

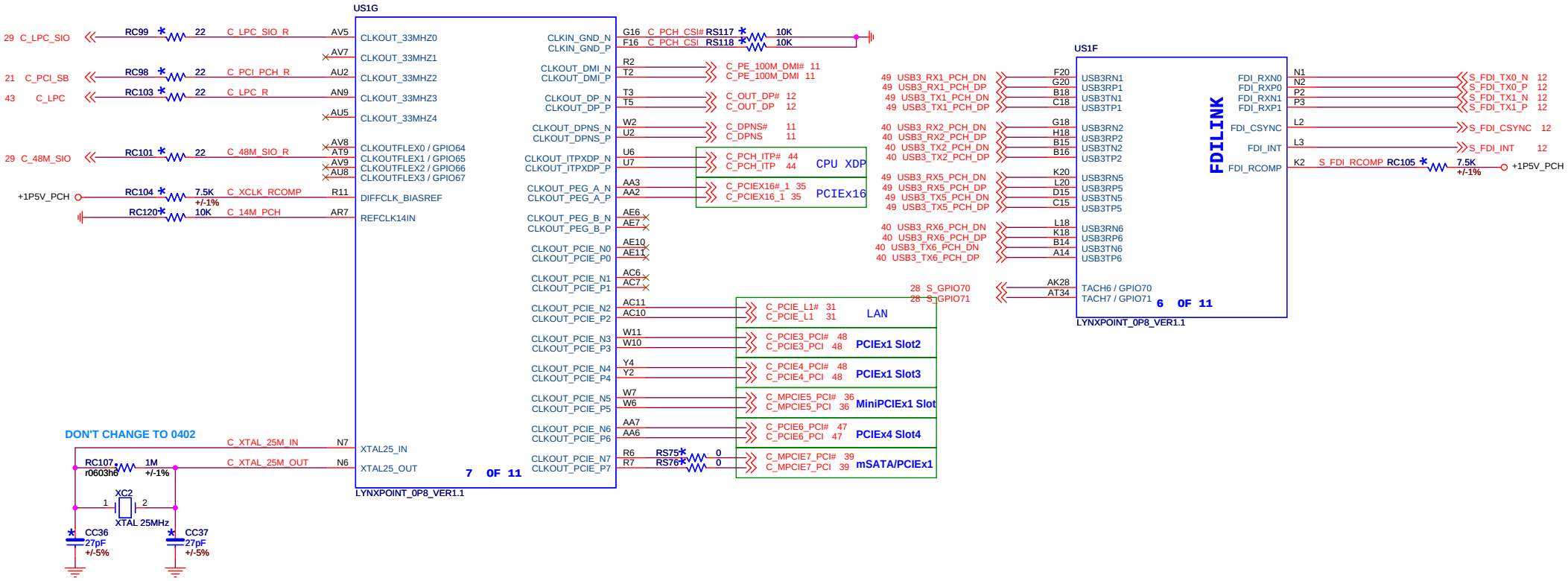
If RS87 pop, CPU RESET CIRCUIT need to Dummy

Used SIO5555 run Deep Sleep S5 Mode: RS85 Dummy , RS86 pop.

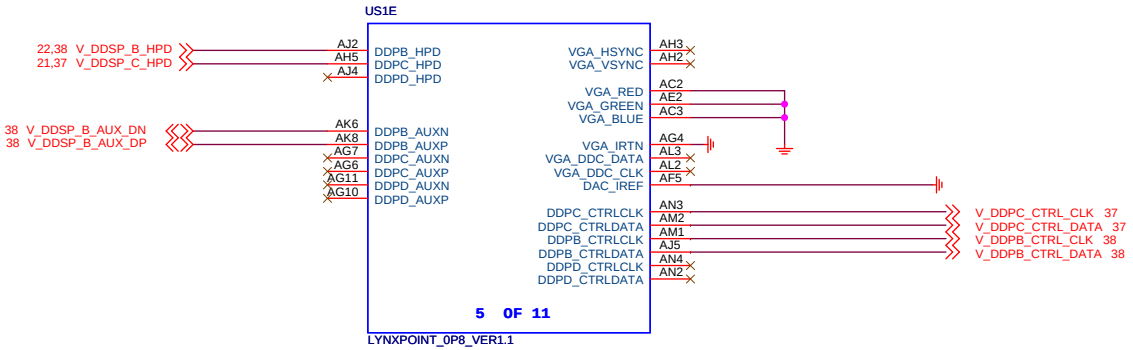
RTC

Title	PCH-3:SPI/HDA/ACPI/MISC
DWG NO	Goodyear
Rev	A00
Date:	星期三, 二月 20, 2013
Sheet	23 of 57

PCH - CLOCK DISTRIBUTION



PCH - DP AND RGB



DELL INC.

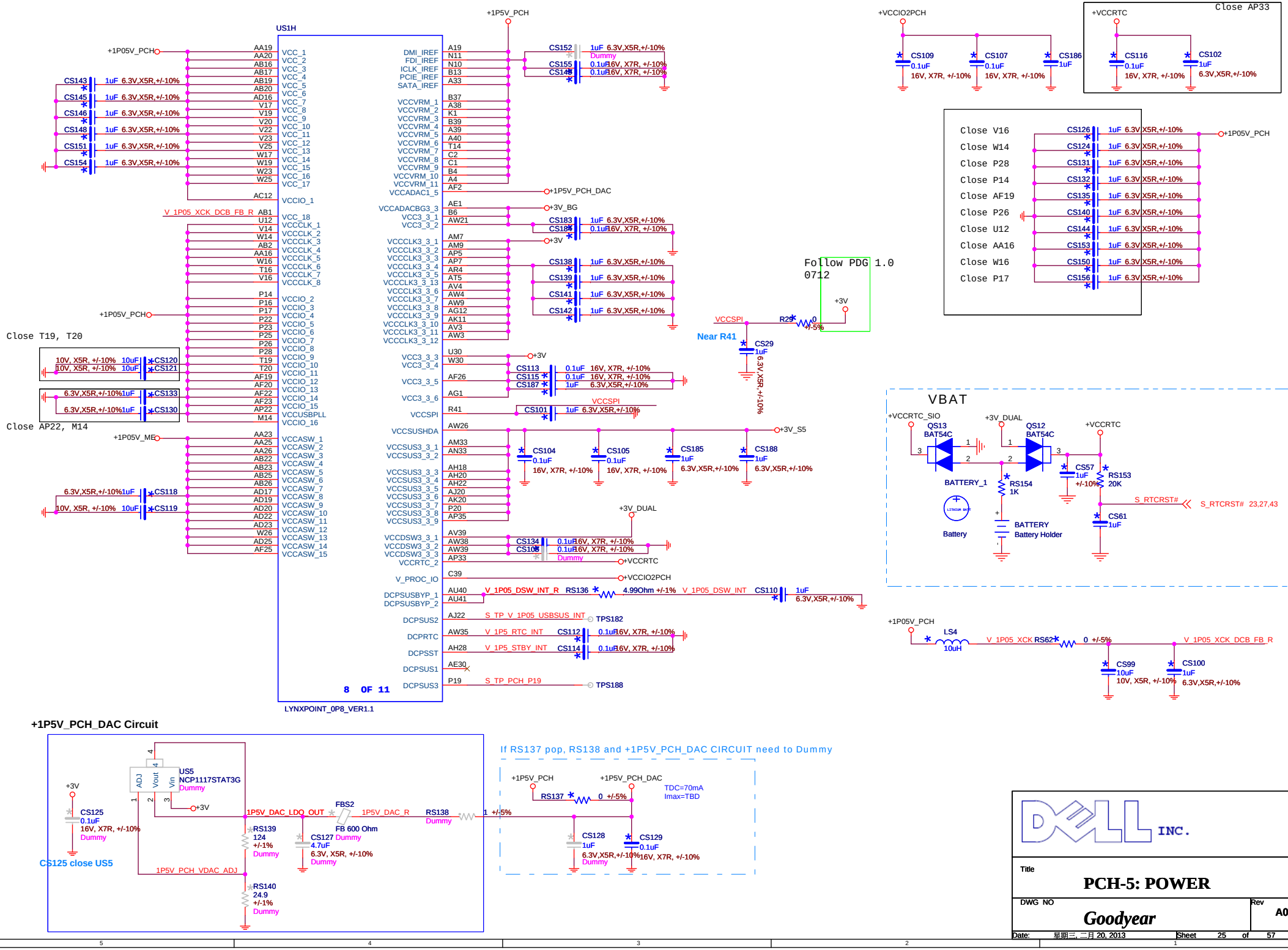
Title

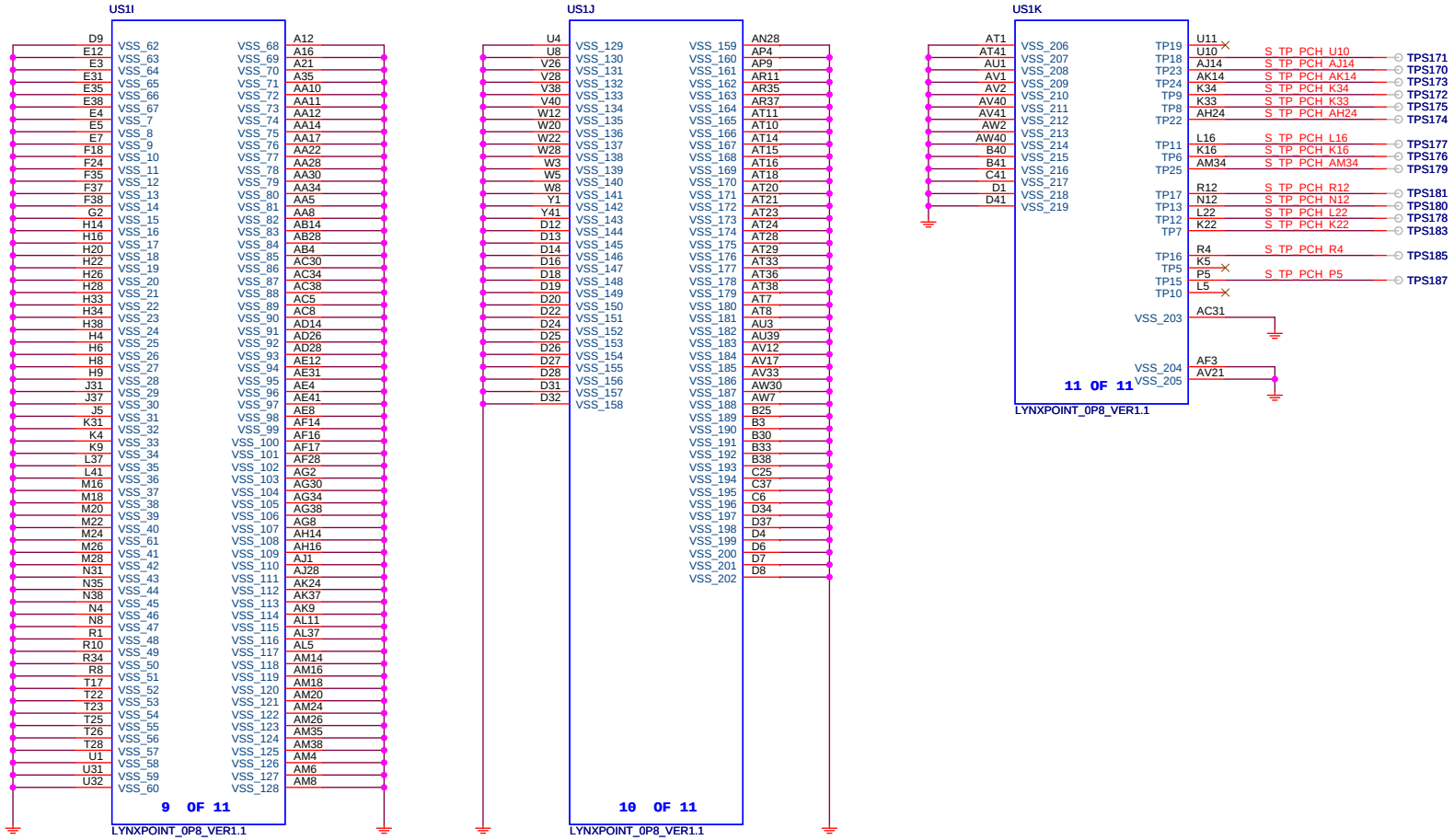
PCH-4: VGA/USB3/CLK/FDI

DWG NO Goodyear

Rev A00

Date: 星期三, 二月 20, 2013 Sheet 24 of 57


US1H
LYNXPOINT_0P8_VER1.1
8 OF 11
Close T19, T20
Close AP22, M14
Close AP33
Close V16
Close W14
Close P28
Close P14
Close AF19
Close P26
Close U12
Close AA16
Close W16
Close P17
Follow PDG 1.0 0712
Near R41
VBAT
Battery
BATTERY
Battery Holder
+1P5V_PCH_DAC Circuit
US5 NCP1117STAT3G Dummy
CS125 close US5
If RS137 pop, RS138 and +1P5V_PCH_DAC CIRCUIT need to Dummy
TDC=70mA Imax=TBD
PCH-5: POWER
Goodyear
DELL INC.
DWG NO
A00
Date: 星期三, 二月 20, 2013
Sheet 25 of 57



DELL INC.

Title

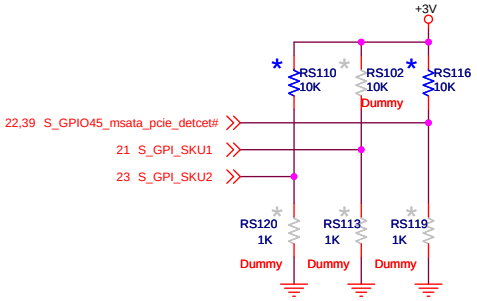
PCH-6: GND

DWG NO

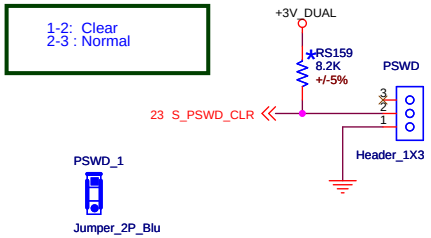
Goodyear

Rev A00

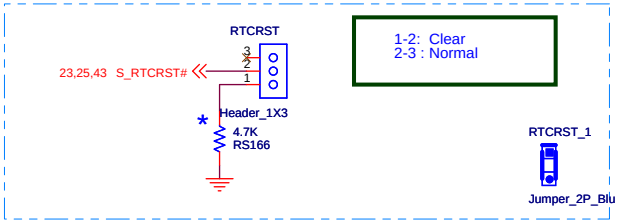
Date: 星期三, 二月 20, 2013 Sheet 26 of 57



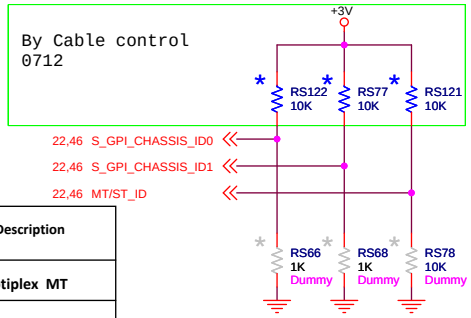
Clear Password



CLR_CMOS

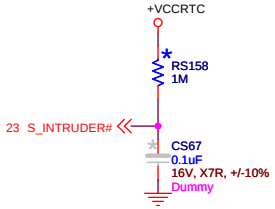


Chassis ID

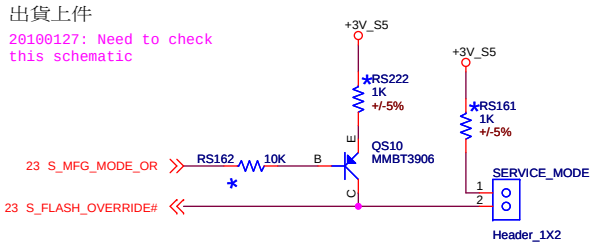


Chassis ID1	Chassis ID0	MT/ST ID	Description
L	L	L	Optiplex MT
L	L	H	Optiplex SFF
L	H	L	Cosumer MT Goodyear
L	H	H	Consumer SFF
H	L	L	SMB MT Riviera
H	L	H	SMB ST
H	H	L	reserved
H	H	H	CBL detect

Chassis Intruder

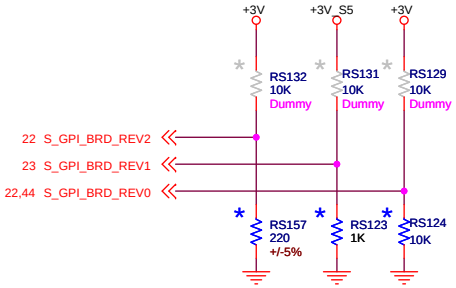


ME Disable (Flash overide)

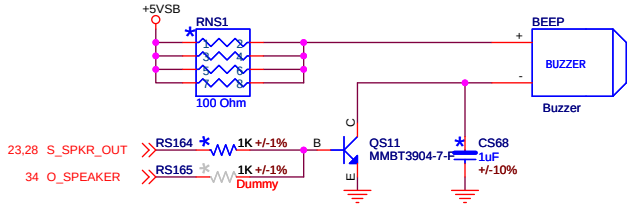


BOARD ID

Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



BEEP



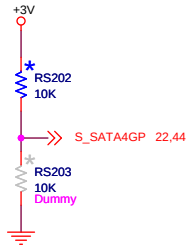
DELL INC.

Title: **PCH-8: MISC CONN/BEEP/ID**

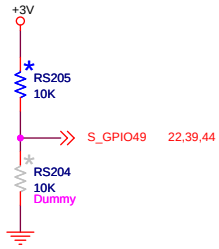
DWG NO: *Goodyear* | Rev: A00

Date: 星期四, 五月 09, 2013 | Sheet 27 of 57

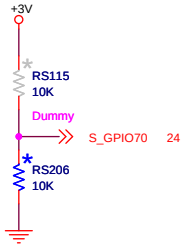
GPIO16 (H-->SATA4 ; L-->PCIe1)



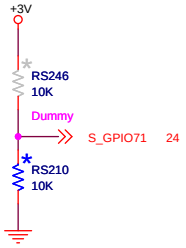
GPIO49 (H-->SATA5 ; L-->PCIe2)



GPIO70 (H-->PCIe1 ; L-->USB3 3)

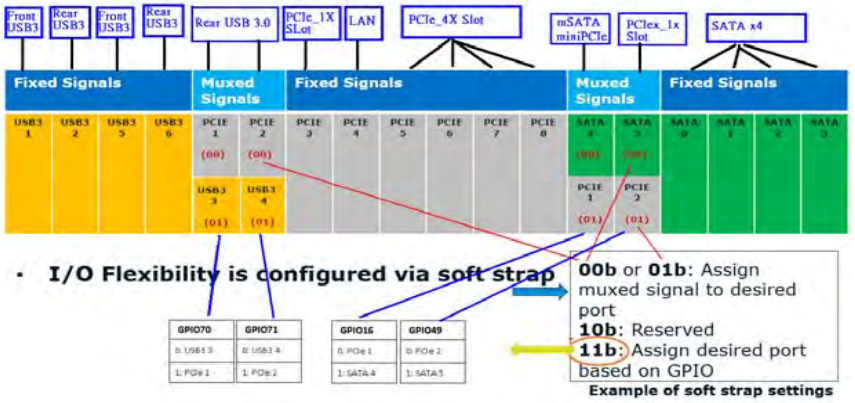


GPIO71 (H-->PCIe2 ; L-->USB3 4)



Lynx Point I/O Flexibility

- New architecture allows some I/O Ports to be configured at time of system design



- I/O Flexibility is configured via soft strap

00b or **01b**: Assign muxed signal to desired port
10b: Reserved
11b: Assign desired port based on GPIO

Example of soft strap settings

No Reboot Mode

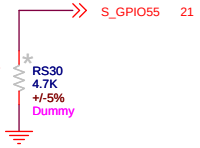
SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable

DEFAULT

Topblock Swap Mode

GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable

DEFAULT



On-Die PLL Voltage Regulator

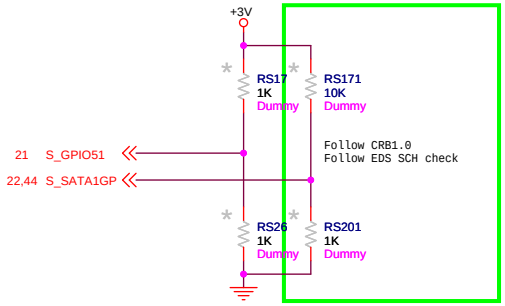
GPIO62/SUSCLK (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.

DEFAULT

Boot BIOS Destination Selection

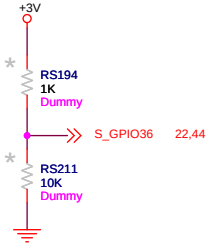
GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI

DEFAULT



DMI Rx Termination

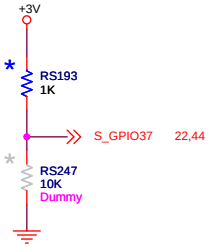
GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality

DEFAULT



DMI AC COUPLING FULL VOLTAGE MODE WHEN SAMPLED LOW

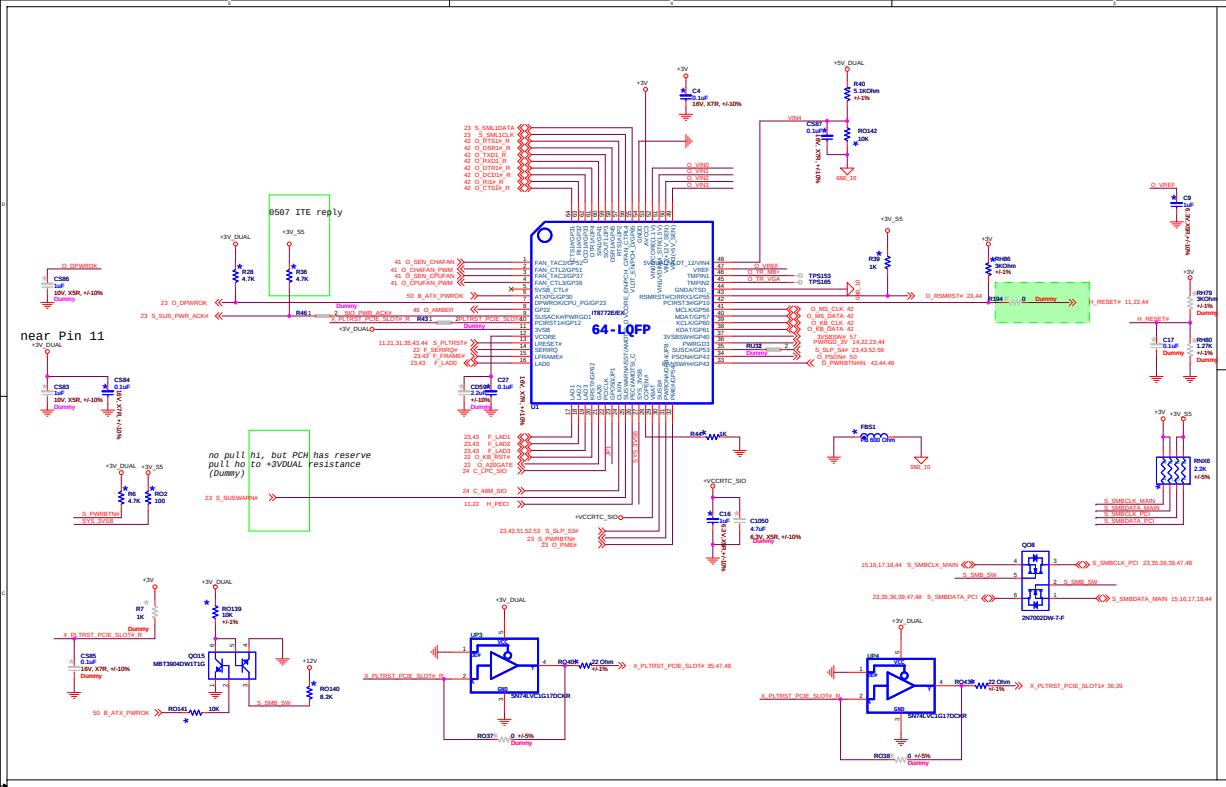
DELL INC.

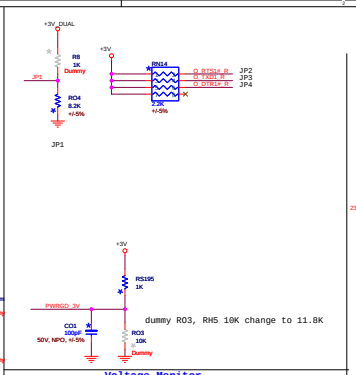
Title
PCH-9: STRAP OPTION

DWG NO
Goodyear

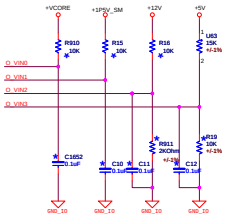
Rev
A00

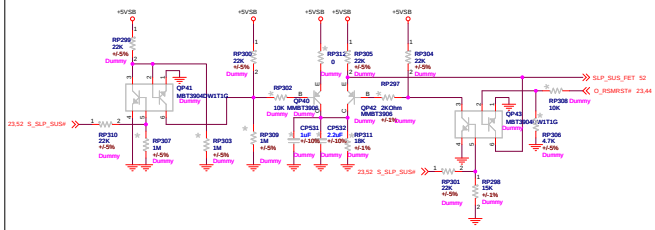
Date: 星期三, 二月 20, 2013 Sheet 28 of 57





Voltage Monitor





Title	SIO-SCH5555-1
DWG NO	Goodyear
Rev	A00
Date:	Sheet 29 of 37

5 4 3 2 1

D C B A

DELL INC.

Title

SIO-SCH5555-2

DWG NO

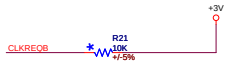
Goodyear

Rev

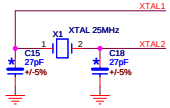
A00

Date: 星期三, 二月 20, 2013 Sheet 30 of 57

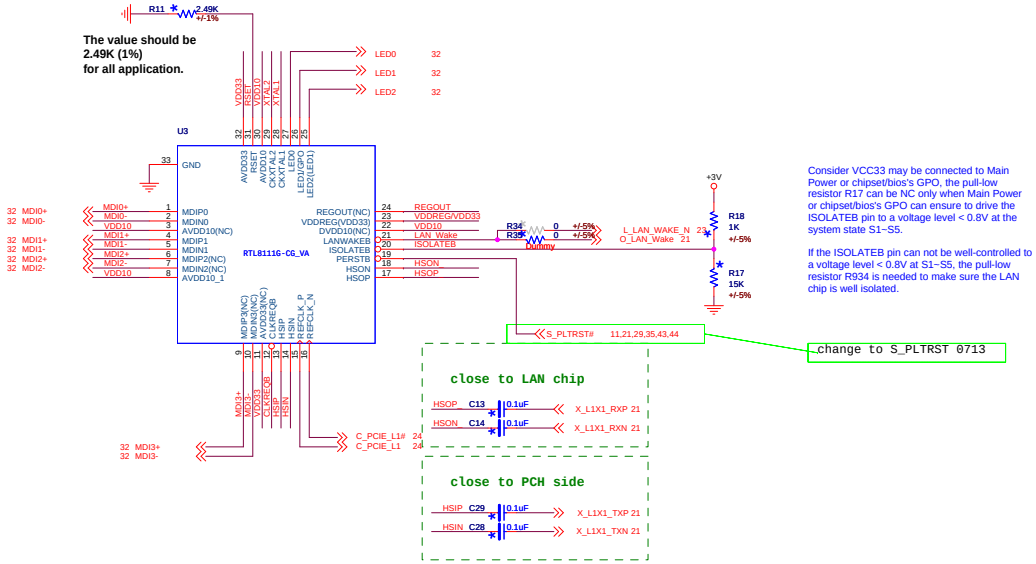
R21, R22 could be saved through sharing the pull-up resistors which might be possibly existed on the motherboard already.



Note: 10K ohm close to Host side



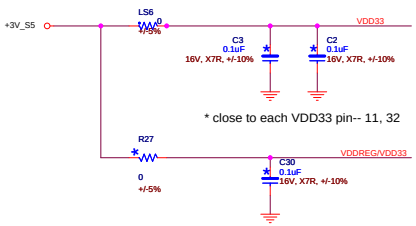
The value should be 2.49K (1%) for all application.

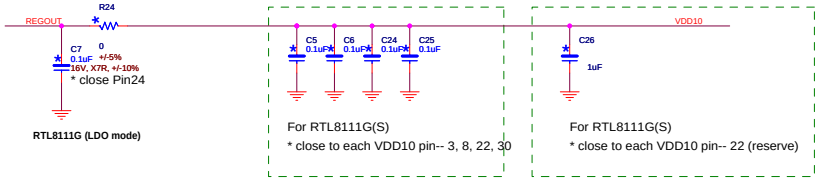


Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R17 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1~S5.

If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1~S5, the pull-low resistor R934 is needed to make sure the LAN chip is well isolated.

LAN POWER





DELL INC.

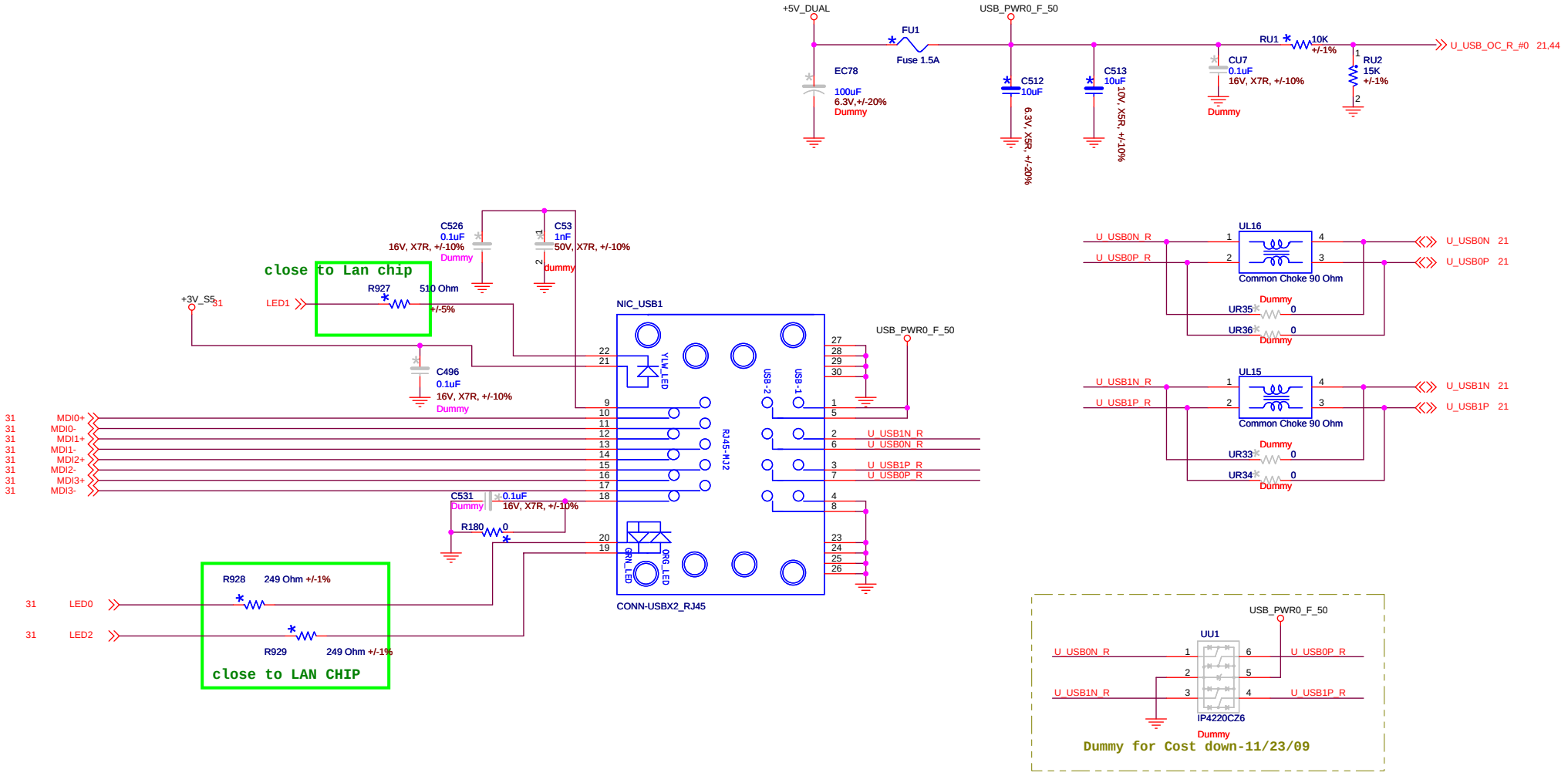
Title: LAN:Intel Clarkville

DWG NO: Goodyear

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 31 of 57

LAN CONNECTOR

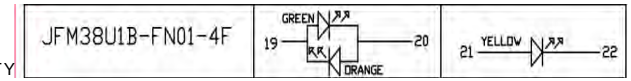


SPEED LED	
LINK 10M	GREEN
LINK 100M	
LINK 1000M	ORANGE

ACTIVE LED

YELLOW = LINK UP
BLINKING = TX/RX ACTIVITY

JFM38U1B-FN01-4F



When implementing customized LEDs:

Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0x0CA9h (0000110010101001b), the LED actions are:

- LED 0: On only in 10M mode, with blinking during TX/RX
- LED 1: On only in 100M mode, with blinking during TX/RX
- LED 2: On only in 1000M mode, with blinking during TX/RX

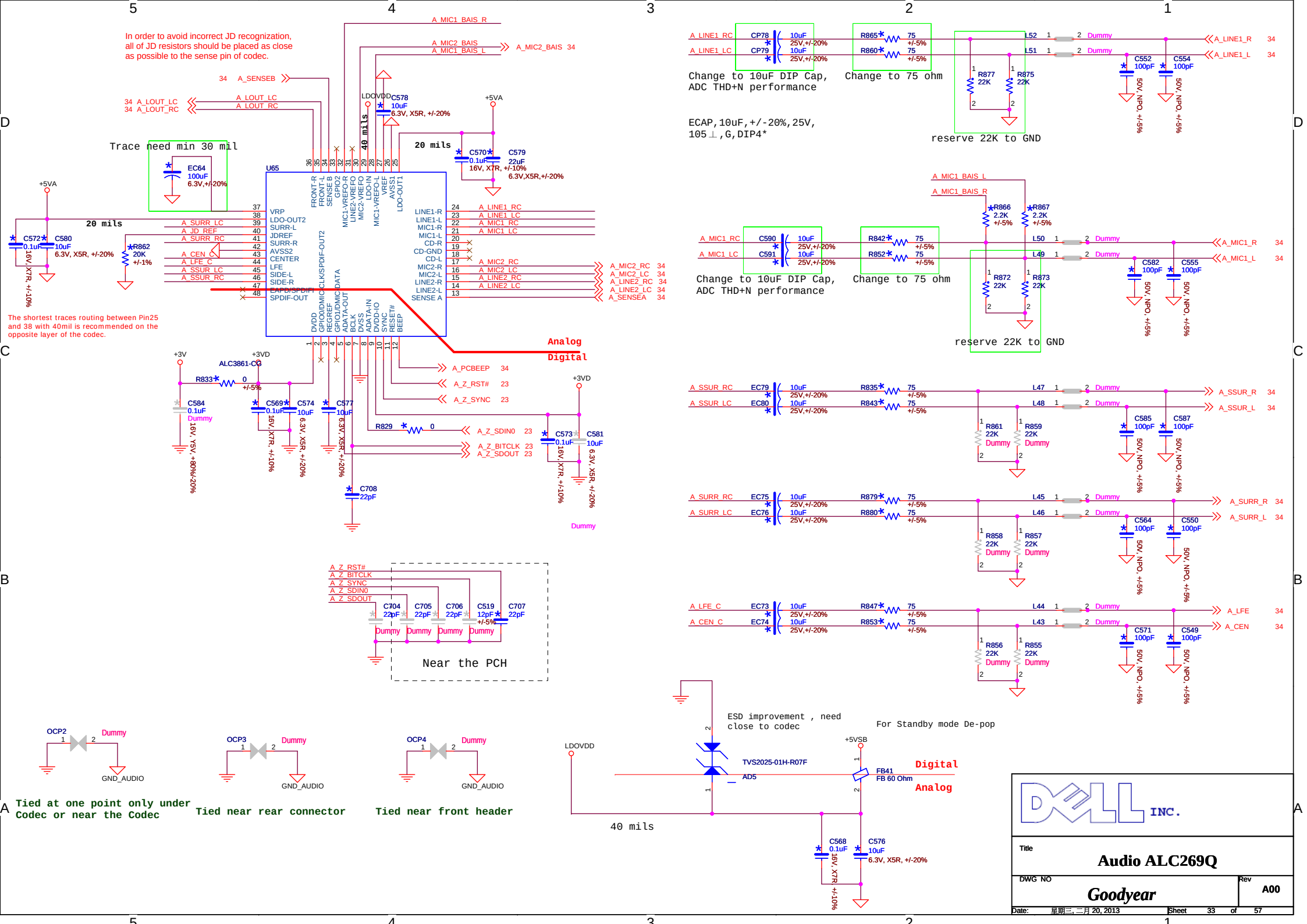
DELL INC.

Title: **LAN Power & LAN/USB Conn**

DWG NO: *Goodyear*

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 32 of 57


In order to avoid incorrect JD recognization, all of JD resistors should be placed as close as possible to the sense pin of codec.
Trace need min 30 mil
20 mils
40 mils
U65
Analog
Digital
Change to 10uF DIP Cap, ADC THD+N performance
Change to 75 ohm
ECAP,10uF,+/-20%,25V, 105⊥,G,DIP4*
reserve 22K to GND
The shortest traces routing between Pin25 and 38 with 40mil is recommended on the opposite layer of the codec.
Near the PCH
ESD improvement , need close to codec
For Standby mode De-pop
Tied at one point only under Codec or near the Codec
Tied near rear connector
Tied near front header
Dummy
GND_AUDIO
TVS2025-01H-R07F
FB 60 Ohm
Title
Audio ALC269Q
DWG NO
Goodyear
Rev
A00
Date: 星期三, 二月 20, 2013
Sheet 33 of 57

JACK SENSE

33 A_SENSEB
R885 5.1KOhm +/-1% A_SSUR_JD Rear SIDE-SURR
R886* 10K +/-1% A_CEN_LFE_JD Rear CEN/LFE
R883* 39.2K +/-1% A_LINE2_JD Front Line Out
R884* 20K +/-1% A_MIC2_JD Front MIC2

33 A_SENSEA
R838* 10K +/-1% A_LINE1_JD Rear LINE1
R839* 20K +/-1% A_MIC1_JD Rear MIC
R840* 39.2K +/-1% A_SURR_JD Rear SURR
R841 5.1KOhm +/-1% A_LOUT_JD Rear Line Out

Front_Audio

MIC II
LINE II
F_AUDIO1 Header_2X5_K8
A_MIC2_L, A_MIC2_R, A_LINE2_R, A_LINE2_L
A_MIC2_JD, A_LINE2_JD
A_FP_PRES# 22
C437 0.1uF Dummy 16V, X7R, +/-10%

Q106 BAT54A
33 A_MIC2_BAIS
R890* 4.7K
R889* 4.7K

33 A_MIC2_LC
33 A_MIC2_RC
C595* 10uF 25V,+/-20%
C596* 10uF 25V,+/-20%
R871* 75 +/-5%
R869* 75 +/-5%
A_MIC2_L
A_MIC2_R
R878 22K
R881* 22K
C583 100pF
C559 100pF

Change to 10uF DIP Cap, ADC THD+N performance
Change to 75 ohm
ECAP,10uF,+/-20%,25V, 105⊥,G,DIP4*
reserve 22K to GND

33 A_LOUT_LC
33 A_LOUT_RC
EC65* 100uF 6.3V,+/-20%
EC66* 100uF 6.3V,+/-20%
R874* 75 +/-5%
R876* 75 +/-5%
L54 Dummy
L53 Dummy
swap R and L trace
A_LOUT_L
A_LOUT_R
R864 22K Dummy
R863 22K Dummy
C551* 100pF 50V, NPO, +/-5%
C553* 100pF 50V, NPO, +/-5%

33 A_LINE2_RC
33 A_LINE2_LC
EC67* 220uF 16V,+/-20%
EC68* 220uF 16V,+/-20%
R831* 18Ohm +/-5%
R832* 18Ohm +/-5%
A_LINE2_R
A_LINE2_L
R870 22K Dummy
R868 22K Dummy
C563* 100pF 50V, NPO, +/-5%
C565* 100pF 50V, NPO, +/-5%

PC BEEP

27 O_SPEAKER
R827* Dummy 47K
C522* Dummy 1uF 10V, X5R, +/-10%
A_PCBEEP 33
R14* 4.7K +/-5% Dummy
C589* 0.1uF 16V, Y5V, +80%/-20% Dummy

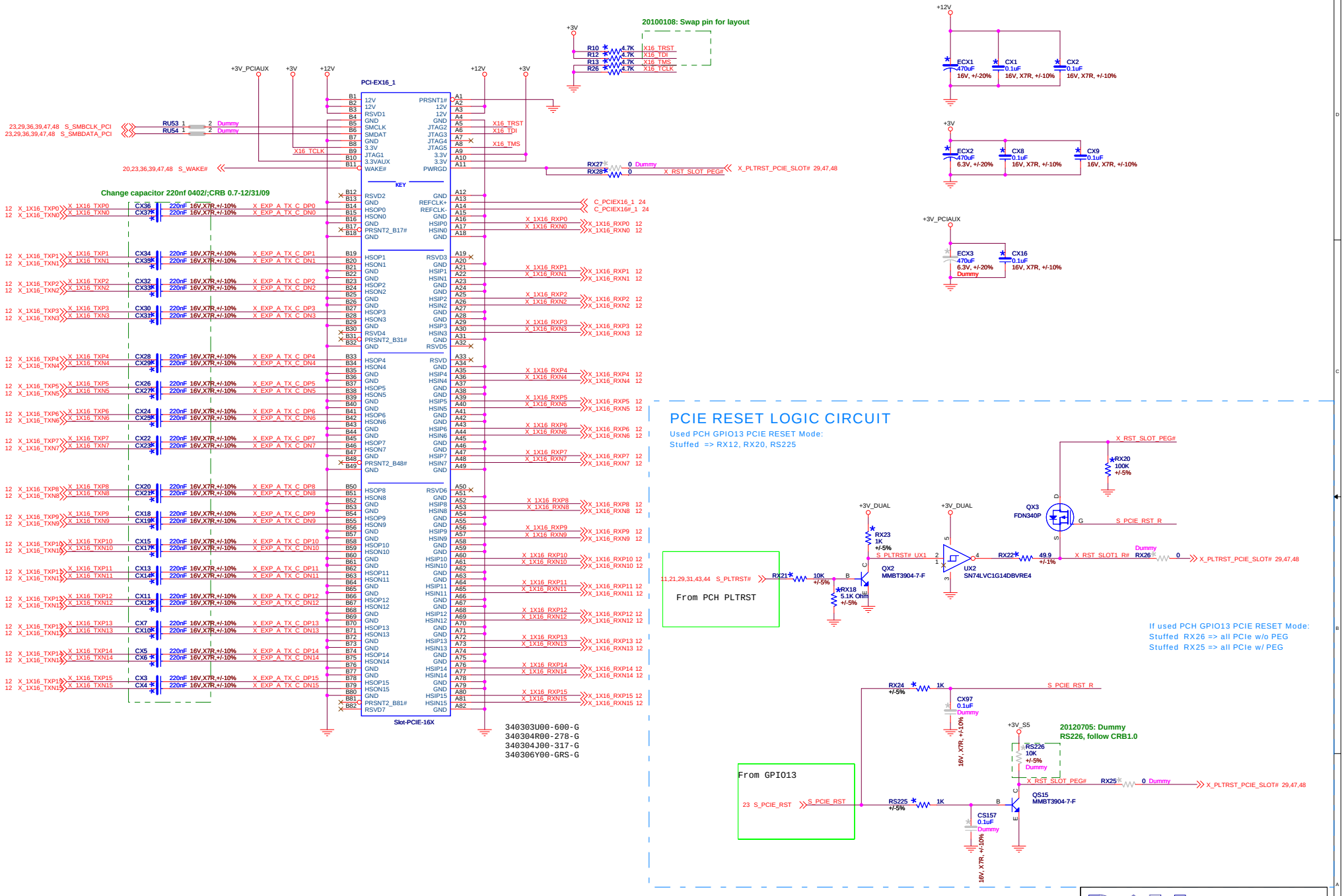
Audio Jack

AUDIO2B CONN-JACK
AUDIO2A CONN-JACK
33 A_LINE1_L
33 A_LINE1_R
33 A_MIC1_L
33 A_MIC1_R
A_LINE1_JD
A_LOUT_L
A_LOUT_JD
A_LOUT_R
A_MIC1_JD
A_CEN_LFE_JD
A_SURR_JD
A_SSUR_JD
A_CEN 33
A_LFE 33
A_SURR_L 33
A_SURR_R 33
A_SSUR_L 33
A_SSUR_R 33

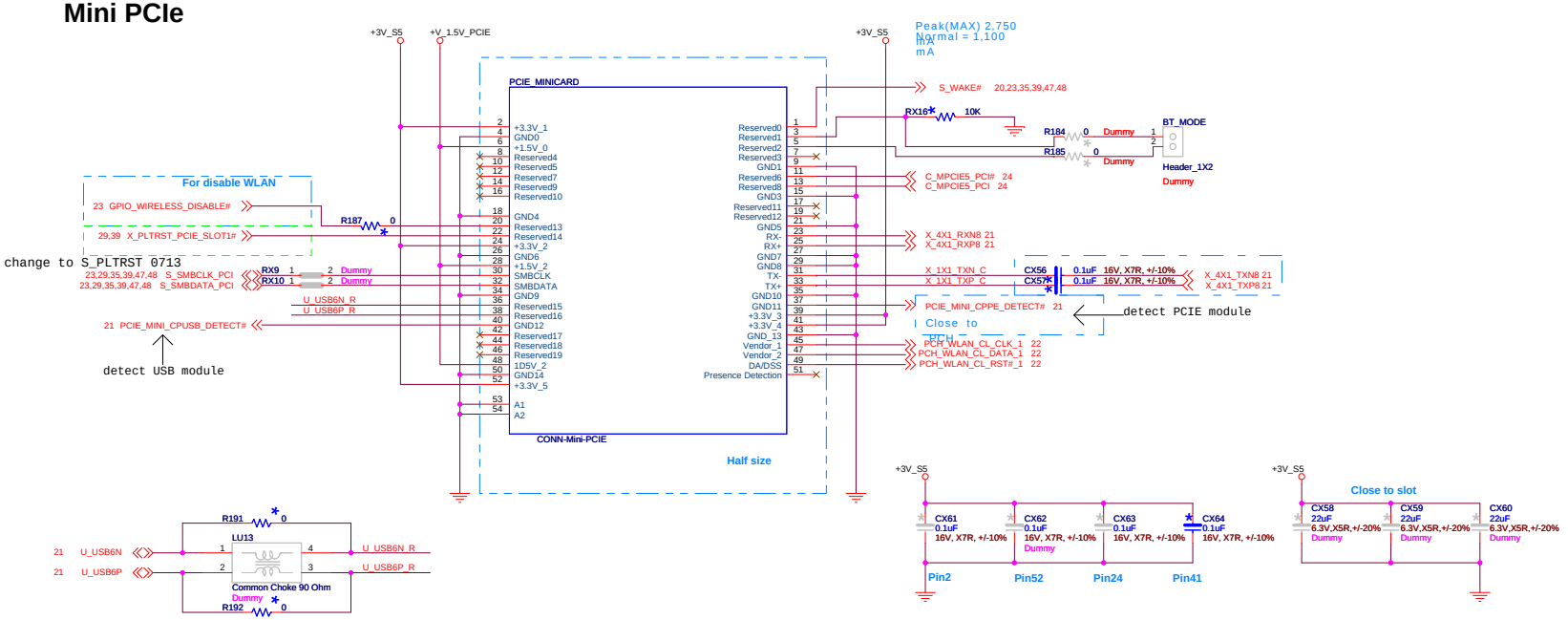
C LINE IN (UAJ)
F CEN/LFE (UAJ)
B LINE OUT (UAJ)
E SURR OUT (UAJ)
A MIC IN (UAJ)
D SIDE SURR OUT (UAJ)

DELL INC.

Title: Audio Conn
DWG NO: Goodyear
Rev: A00
Date: 星期三, 二月 20, 2013
Sheet 34 of 57


20100108: Swap pin for layout
PCI-EX16_1
Change capacitor 220nf 0402/;CRB 0.7-12/31/09
Slot-PCIE-16X
340303U00-600-G
340304R00-278-G
340304J00-317-G
340306Y00-GRS-G
PCIE RESET LOGIC CIRCUIT
Used PCH GPIO13 PCIE RESET Mode:
Stuffed => RX12, RX20, RS225
From PCH PLTRST
From GPIO13
If used PCH GPIO13 PCIE RESET Mode:
Stuffed RX26 => all PCIe w/o PEG
Stuffed RX25 => all PCIe w/ PEG
20120705: Dummy
RS226, follow CRB1.0
Title
Slot1: PCIe 16x
DWG NO
Goodyear
Rev
A00
Date: 星期四, 五月 09, 2013
Sheet 35 of 57

Mini PCIe

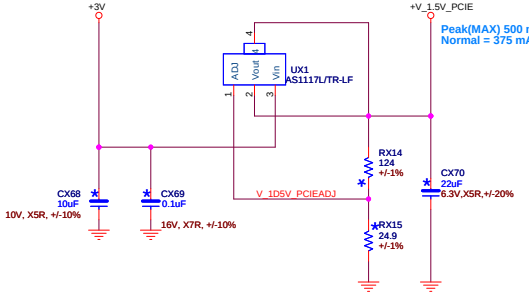


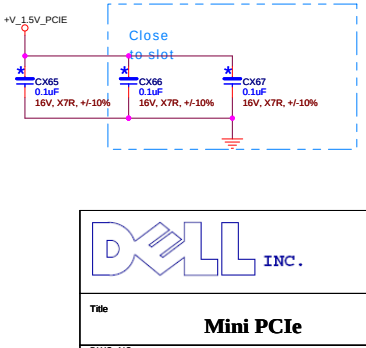
Latch

H4

H3

+V_1.5V_PCIE





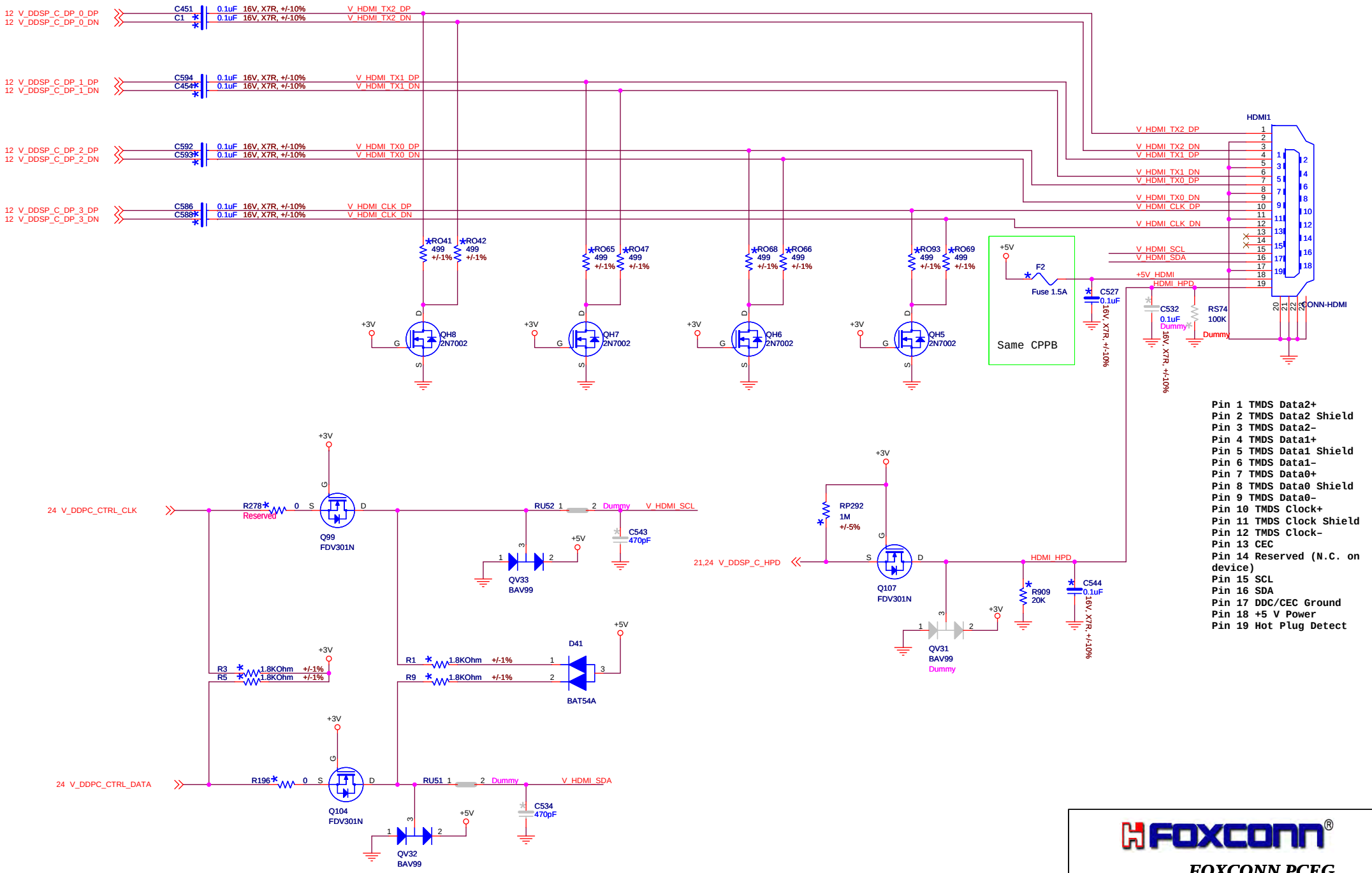
DELL INC.

Title: **Mini PCIe**

DWG NO: *Goodyear*

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 36 of 57



FOXCONN®

FOXCONN PCEG

Title	HDMI	
Size A3	Document Number Goodyear	Rev A00
Date: 星期三, 二月 20, 2013	Sheet 37 of 57	

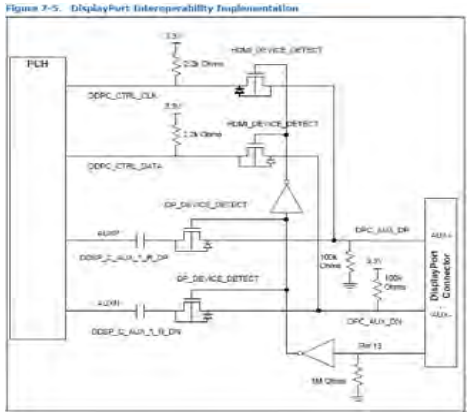
12 V_DDSP_B_DP_0_DP — CV43 0.1uF 16V, X7R, +/-10% — V_DPD_TX0_DP
12 V_DDSP_B_DP_0_DN — CV37 0.1uF 16V, X7R, +/-10% — V_DPD_TX0_DN
12 V_DDSP_B_DP_1_DP — CV42 0.1uF 16V, X7R, +/-10% — V_DPD_TX1_DP
12 V_DDSP_B_DP_1_DN — CV45 0.1uF 16V, X7R, +/-10% — V_DPD_TX1_DN
12 V_DDSP_B_DP_2_DP — CV48 0.1uF 16V, X7R, +/-10% — V_DPD_TX2_DP
12 V_DDSP_B_DP_2_DN — CV36 0.1uF 16V, X7R, +/-10% — V_DPD_TX2_DN
12 V_DDSP_B_DP_3_DP — CV47 0.1uF 16V, X7R, +/-10% — V_DPD_TX3_DP
12 V_DDSP_B_DP_3_DN — CV35 0.1uF 16V, X7R, +/-10% — V_DPD_TX3_DN

UV9: RCLAMP0524P.TCT Dummy
UV10: RCLAMP0524P.TCT Dummy
(O1..O4, GND_2, GND_1, IN1..IN4)

V_DPD_TX0_DP
V_DPD_TX0_DN
V_DPD_TX1_DP
V_DPD_TX1_DN
V_DPD_TX2_DP
V_DPD_TX2_DN
V_DPD_TX3_DP
V_DPD_TX3_DN
DPD_P13
V_DPD_AUX_DP
V_DPD_AUX_DN
V_DPD_HPD_SINK
V_DPD_PWR

RV53 1M
RV56 100K
Close to Connector

DP_PORT2 — CONN - Display port
HOLE3 HOLE2 HOLE4 HOLE1
ML_Lane0_P, GND1, ML_Lane0_N, ML_Lane1_P, GND2, ML_Lane1_N, ML_Lane2_P, GND3, ML_Lane2_N, ML_Lane3_P, GND4, ML_Lane3_N, GND5, GND6, AUX_CH_P, GND7, AUX_CH_N, H_P_DETECT, RETURN, DP_PWR



UV7: RCLAMP0522P.TCT Dummy
V_DPD_AUX_DN 6 → 1 V_DPD_AUX_DN
V_DPD_AUX_DP 5 → 2 V_DPD_AUX_DP
4 GND_2 GND_1 3

UV8: RCLAMP0522P.TCT Dummy
DPD_P13 6 → 1 DPD_P13
V_DPD_HPD_SINK 5 → 2 V_DPD_HPD_SINK
4 GND_2 GND_1 3

24 V_DDSP_B_AUX_DN — CV44 0.1uF 16V, X7R, +/-10% — V_DDSP_D_AUX_DN_C
24 V_DDSP_B_AUX_DP — CV41 0.1uF 16V, X7R, +/-10% — V_DDSP_D_AUX_DP_C

20110211:change 2N7002DW for cost down.

QV42 (2N7002DW)
4 V_DDPB_CTRL_CLK
DPD_P13_POS 5
6 V_DPD_AUX_DP
3, 2, 1
RV40 1M +/-5%

QV41 (2N7002DW)
4 V_DDPB_CTRL_DATA
DPD_P13_POS 5
V_DPD_AUX_DN 6
3, 2, 1
RV48 1M +/-5%

20110211:change 2N7002DW for cost down.

QV40 (2N7002DW)
4 V_DDSP_D_AUX_DP_C
DPD_P13_INV 5
V_DPD_AUX_DP 6
3, 2, 1
RV60 1M +/-5%

QV39 (2N7002DW)
4 V_DDSP_D_AUX_DN_C
DPD_P13_INV 5
V_DPD_AUX_DN 6
3, 2, 1
RV55 1M +/-5%

+3V — FV3 FUSE_1.1A — V_DPD_PWR
CV46 1uF 16V,X5R,+/-20%
CV34 10uF Dummy 10V,X5R,+/-20%
CV38 470pF 50V, X7R, +/-10%
CV40 22uF 6.3V,X5R,+/-20%

+3V — RV46 2.2K +/-5%
+3V — RV58 2.2K +/-5%
24 V_DDPB_CTRL_CLK
24 V_DDPB_CTRL_DATA

+5V — RV51 1K Dummy — V_DPD_HPD_SINK
+5V — QV21 FDV301N (D, G, S) — RV44 100K
V_DDSP_B_HPD 22,24

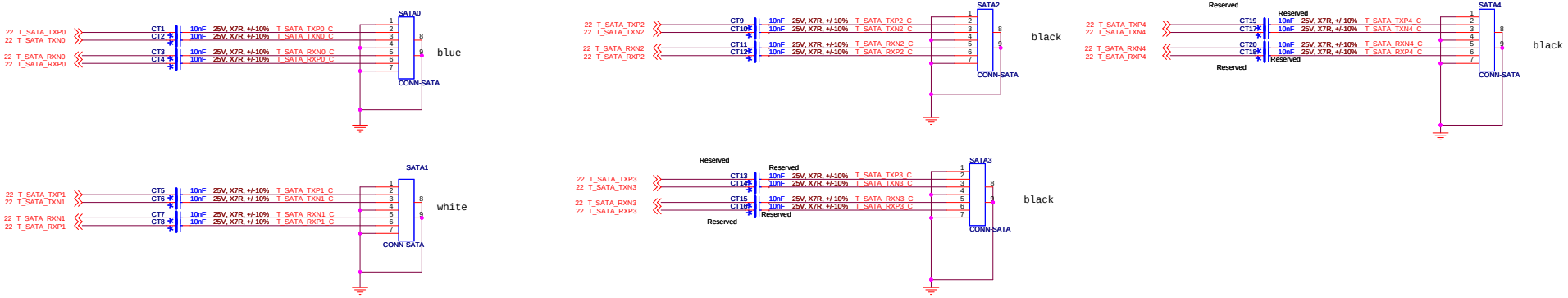
+3V — RV57 100KOhm +/-1%
+3V_DUAL — RV49 100KOhm +/-1% Dummy
+3V — RV52 100KOhm +/-1% Dummy
V_DPD_AUX_DN
V_DPD_AUX_DP
RV43 100KOhm +/-1% Dummy
RV45 100KOhm +/-1%

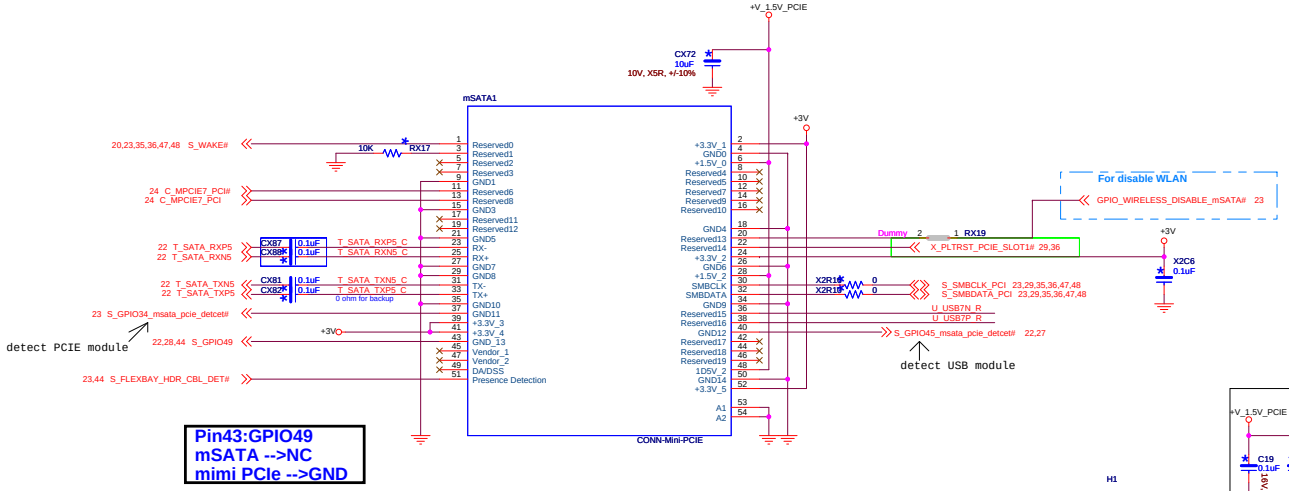
+12V — RV59 4.7K +/-5%
20110211:change 2N7002DW for cost down.
+5V — RV42 1K Dummy
DPD_P13 — RV47 8.2K +/-5%
RV54 1M +/-5%
CV39 0.1uF 16V, X7R, +/-10%
DPD_P13_INV
QV34 2N7002DW (3, 2, 1 / 4, 5, 6)
+12V — RV41 8.2K +/-5% — DPD_P13_POS

DELL INC.

Title: VGA Conn
DWG NO: Goodyear
Rev: A00
Date: 星期三, 二月 20, 2013
Sheet 38 of 57

SATA x 4





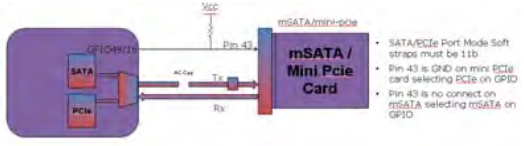
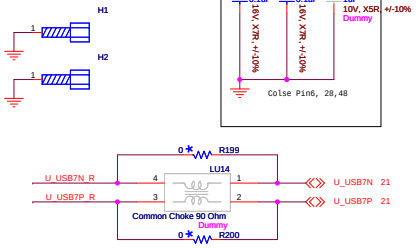


Table below summarizes the AC cap requirement on the motherboard when using SATA/PCIe muxed port.

Condition	PCIe only	SATA only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF (Can be removed if choose NOT to support DC coupled ODDs)	None (put footprint and stuff with zero ohm for backup)



DELL INC.

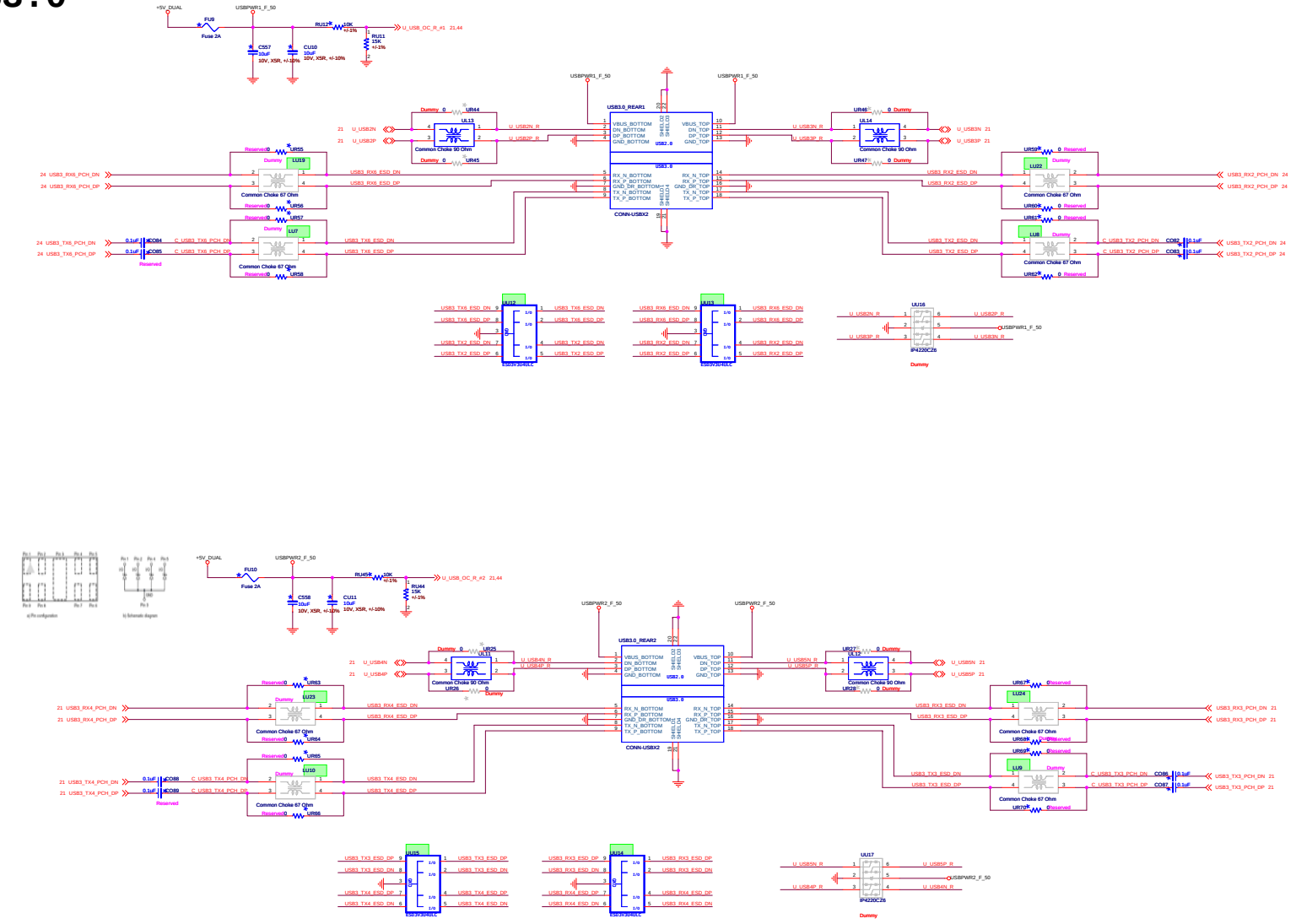
Title: **SATA Conn**

DWG NO: **Goodyear**

Rev: **A00**

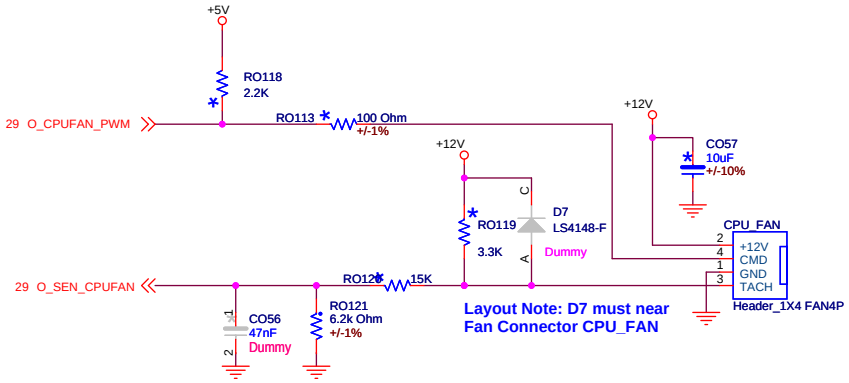
Date: 星期三, 二月 20, 2013 Sheet 39 of 57

Rear USB3.0

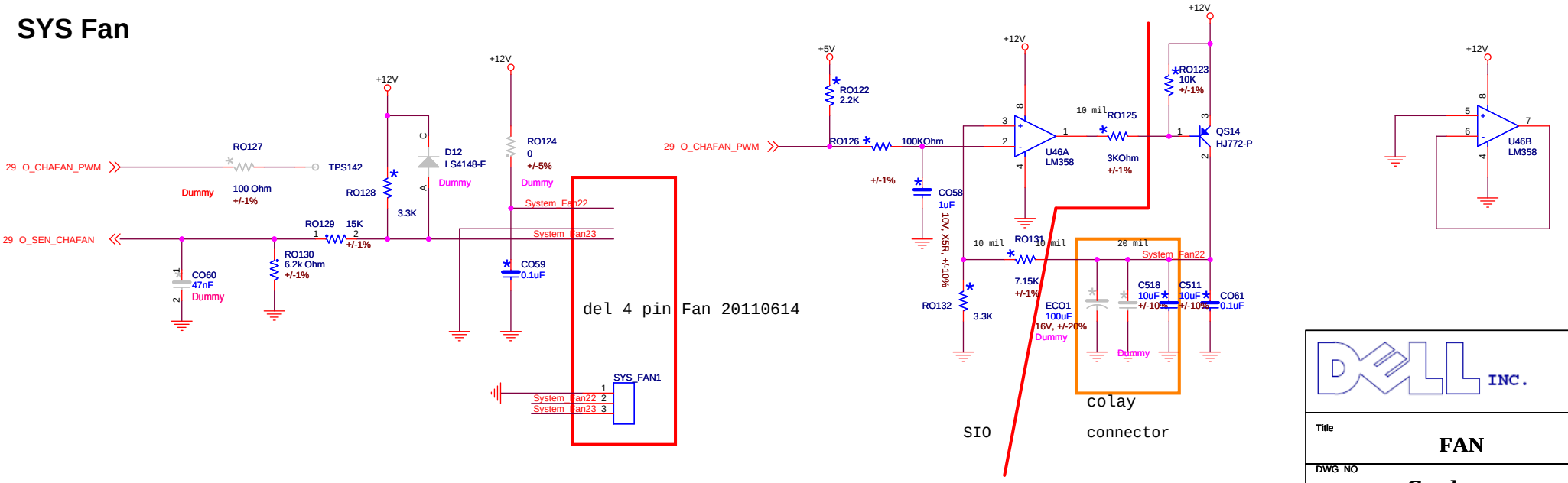


Title	eSATA Conn
DWG NO	Goodyear
Rev	A00
Date:	January 20, 2013
Sheet	40 of 57

CPU Fan



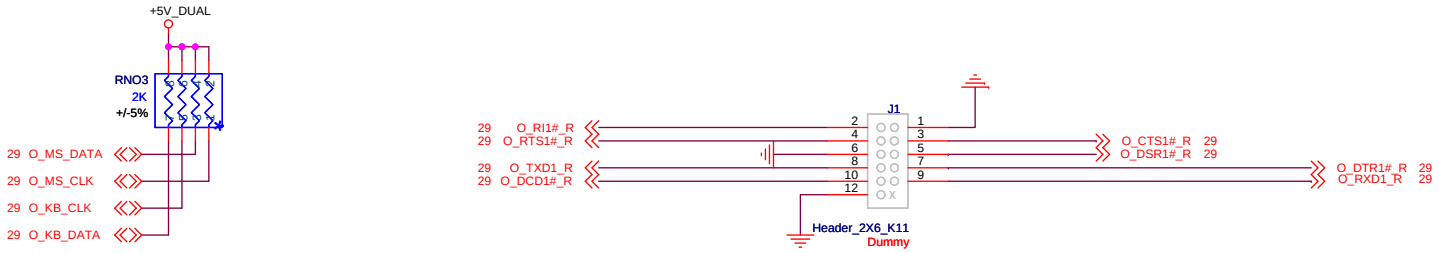
SYS Fan



Title	FAN
DWG NO	Goodyear
Rev	A00
Date:	星期三, 二月 20, 2013
Sheet	41 of 57

Serial

PS2 port



DELL INC.

Title

Serial / PS2 port

DWG NO

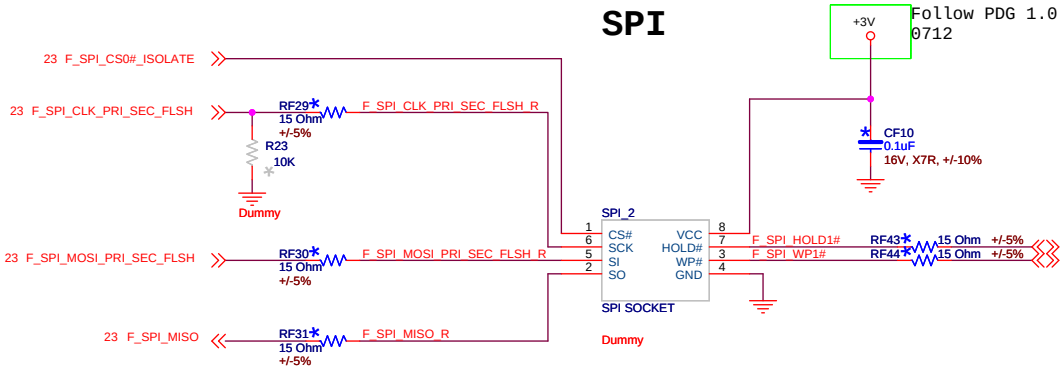
Goodyear

Rev

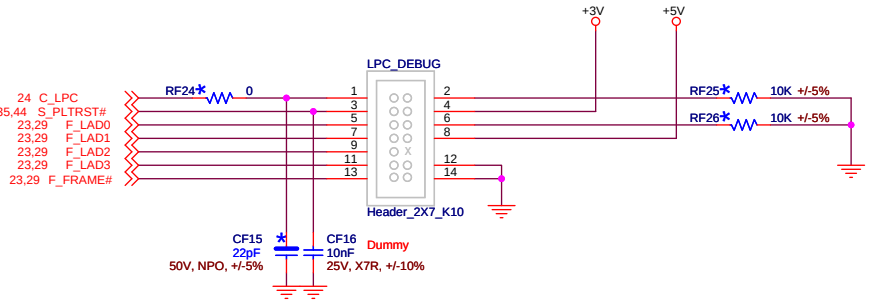
A00

Date: 星期三, 二月 20, 2013 Sheet 42 of 57

SPI

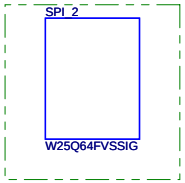


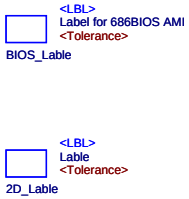
LPC DEBUG

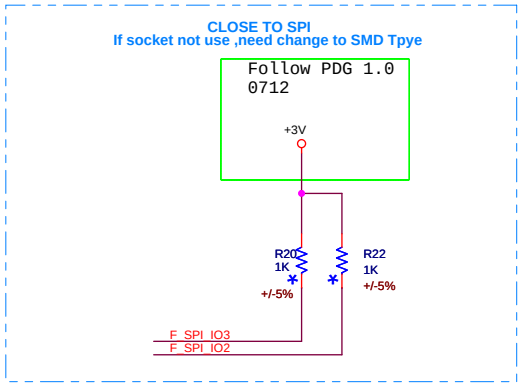


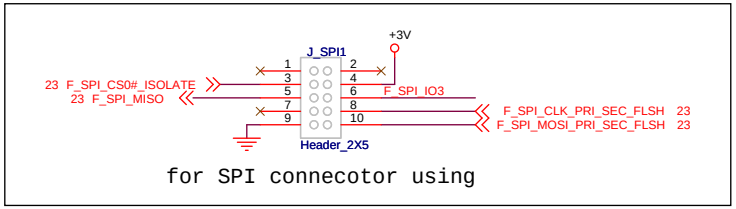
SPI_8MB

變更文字為SPI_2，為改打SMD
20120216: SPI1 Change to WINBOND_W25Q32BVSSIG

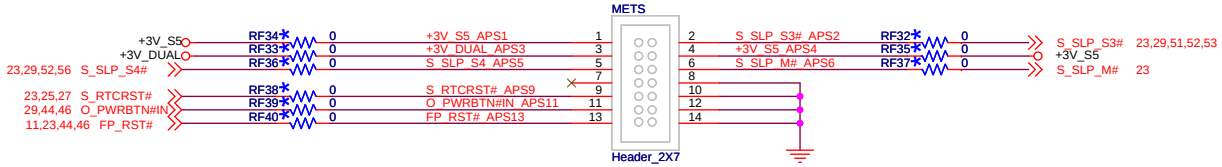








APS DEBUG



Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_S3#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_S4#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7	Unused	
Pin 8	GND	Ground
Pin 9	RTCRST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCRST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

DELL INC.

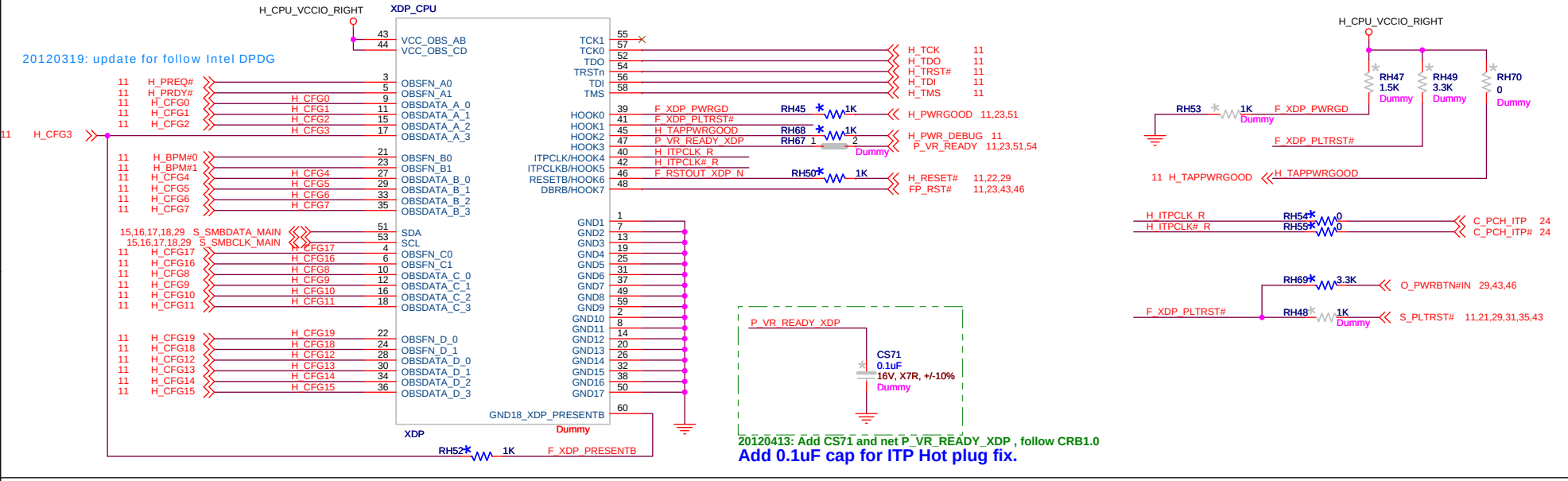
Title: **SPI/LPC DBG**

DWG NO: *Goodyear*

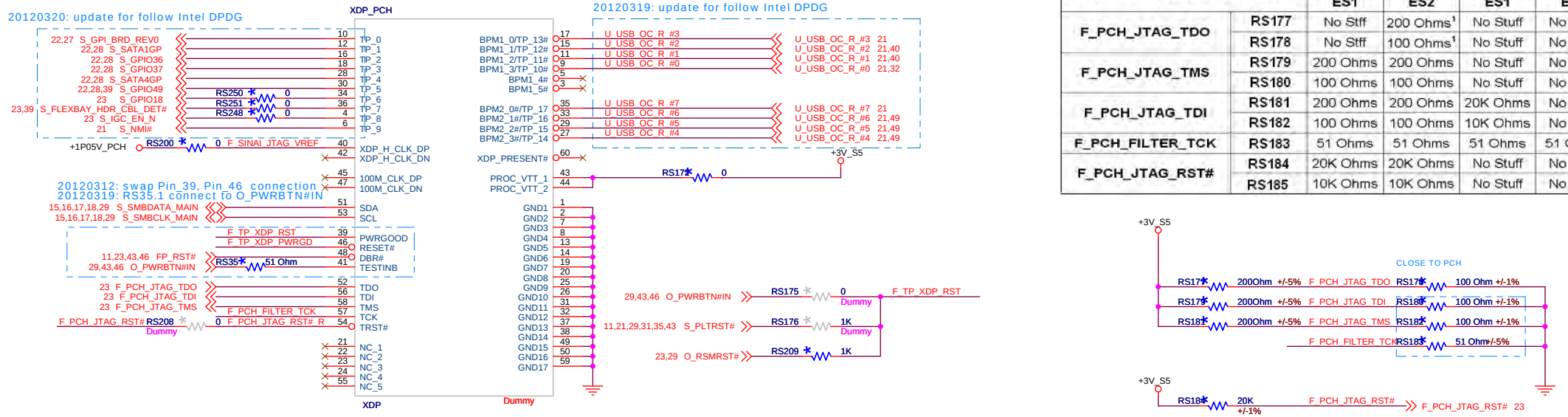
Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 43 of 57

XDP Connector - CPU



XDP Connector - PCH



2009/12/21 Update JTAG Table		PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	RS177	No Stff	200 Ohms[1]	No Stuff	No Stuff
	RS178	No Stff	100 Ohms[1]	No Stuff	No Stuff
F_PCH_JTAG_TMS	RS179	200 Ohms	200 Ohms	No Stuff	No Stuff
	RS180	100 Ohms	100 Ohms	No Stuff	No Stuff
F_PCH_JTAG_TDI	RS181	200 Ohms	200 Ohms	20K Ohms	No Stuff
	RS182	100 Ohms	100 Ohms	10K Ohms	No Stuff
F_PCH_FILTER_TCK	RS183	51 Ohms	51 Ohms	51 Ohms	51 Ohms
F_PCH_JTAG_RST#	RS184	20K Ohms	20K Ohms	No Stuff	No Stuff
	RS185	10K Ohms	10K Ohms	No Stuff	No Stuff

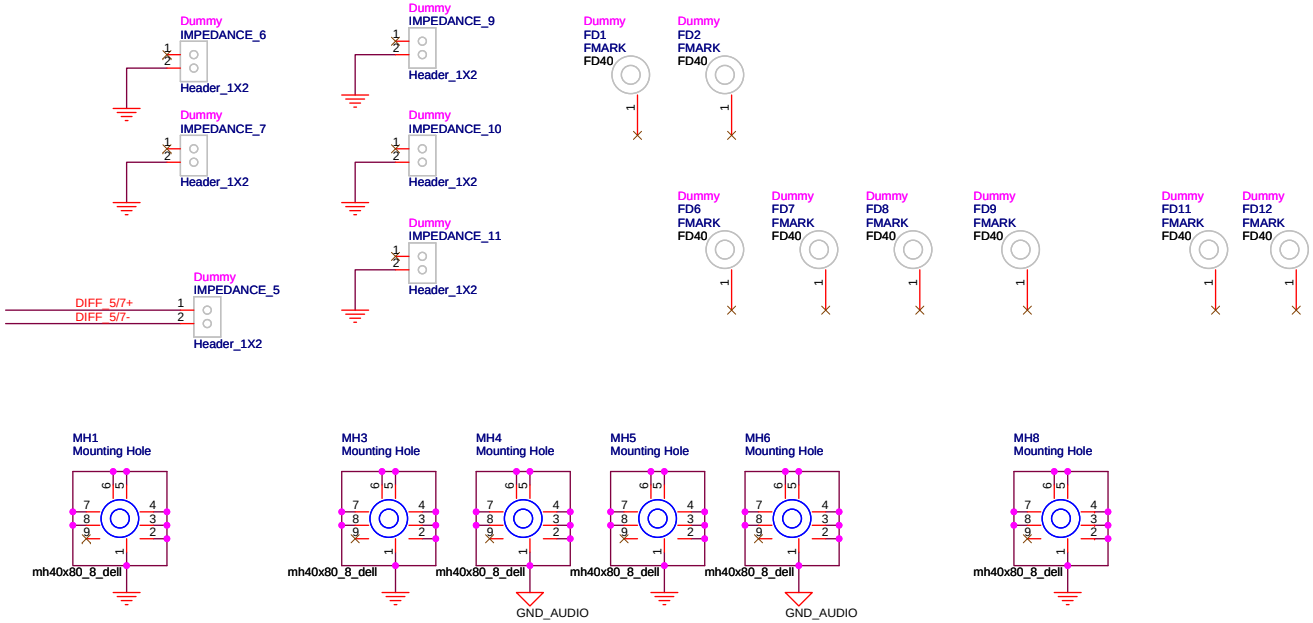
DELL INC.

Title: XDP

DWG NO: Goodyear

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 44 of 57



20100108: Add for EMI

DELL INC.

Title

EMI

DWG NO

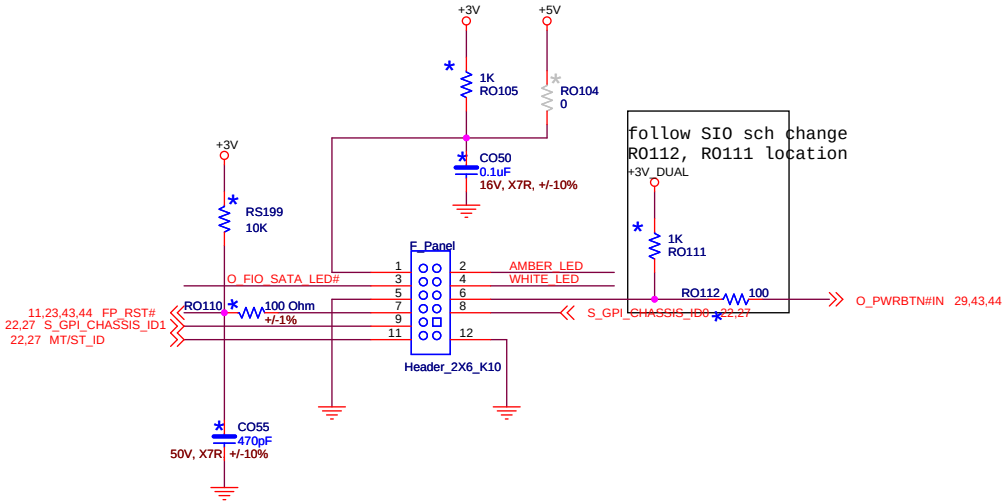
Goodyear

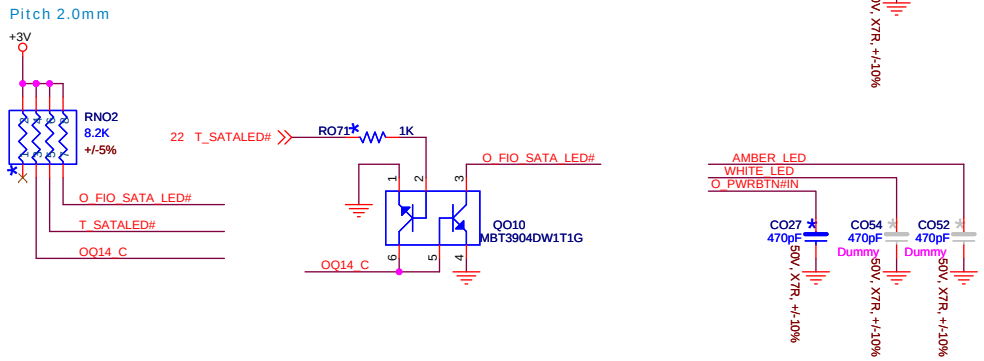
Rev

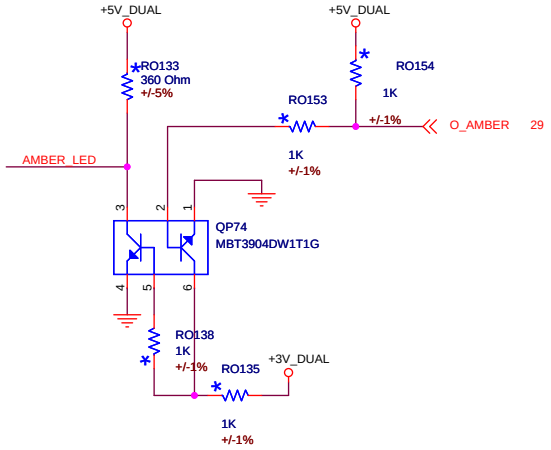
A00

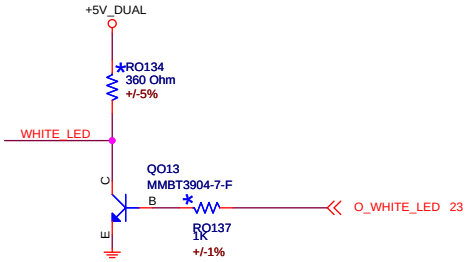
Date: 星期三, 二月 20, 2013 Sheet 45 of 57

Front_IO Header









DELL INC.

Title

Front_Panel

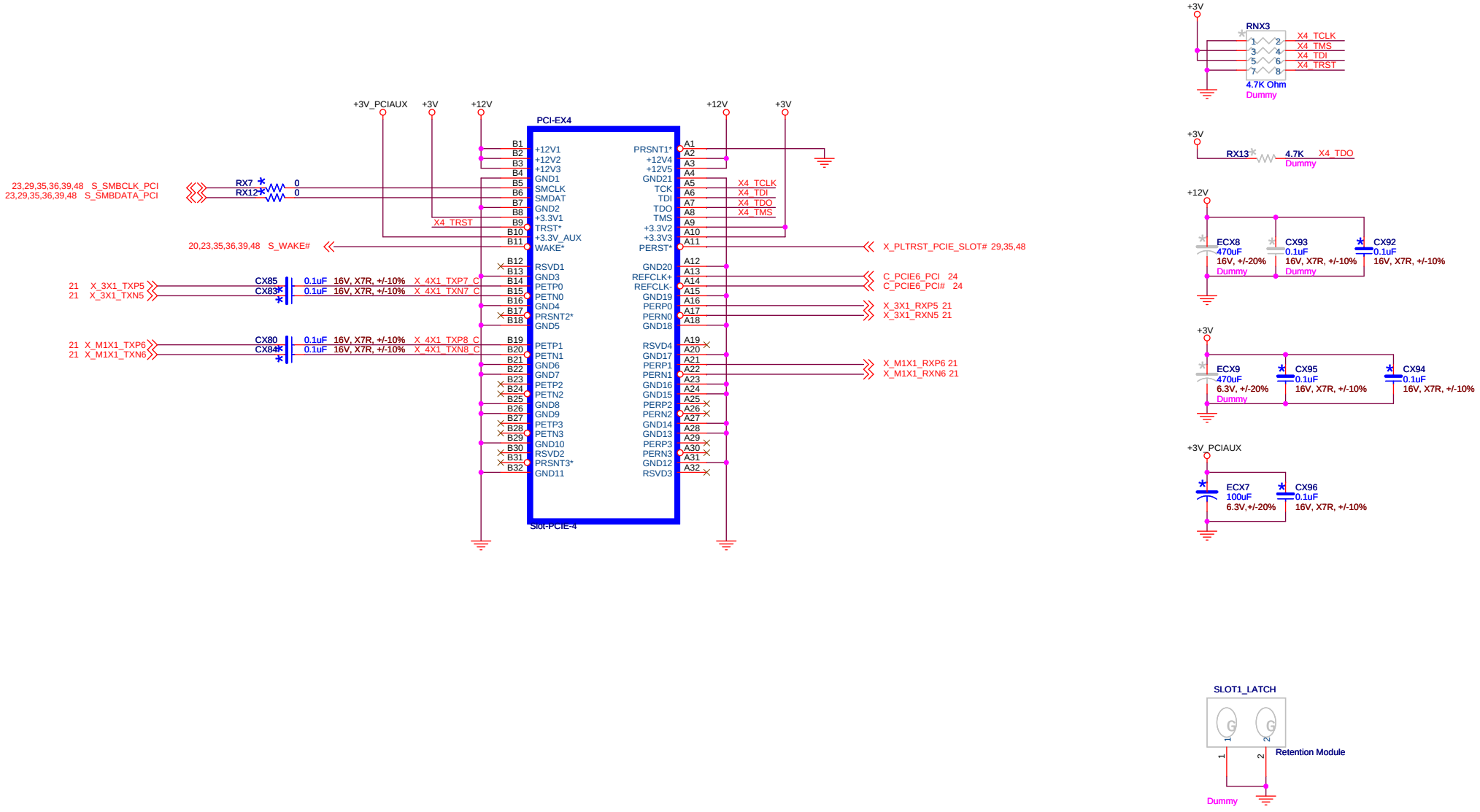
DWG NO

Goodyear

Rev

A00

Date: 星期三, 二月 20, 2013 Sheet 46 of 57



DELL INC.

Title

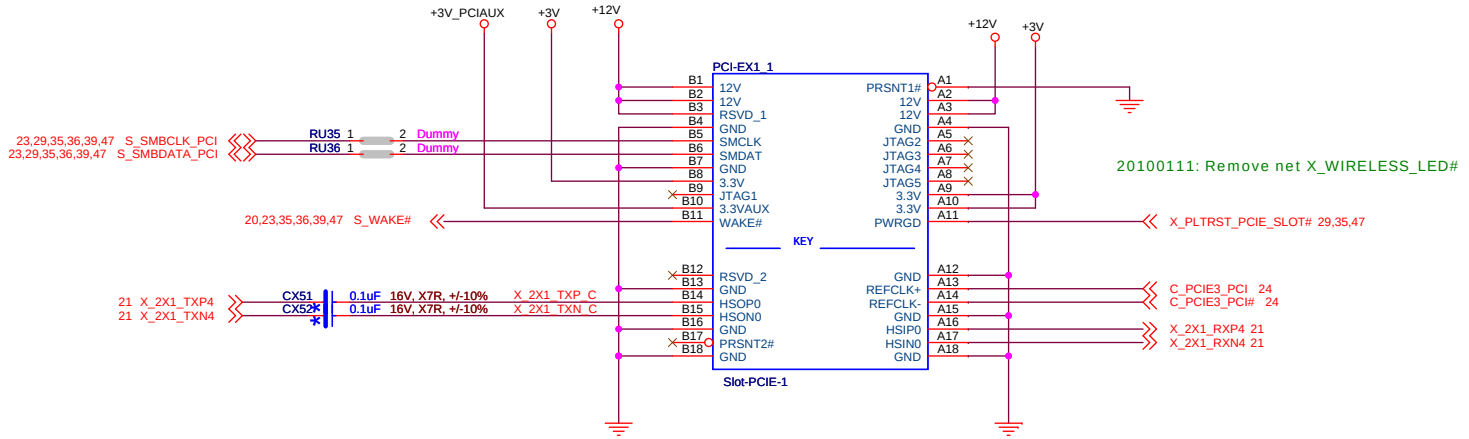
Slot4: PCIEx1

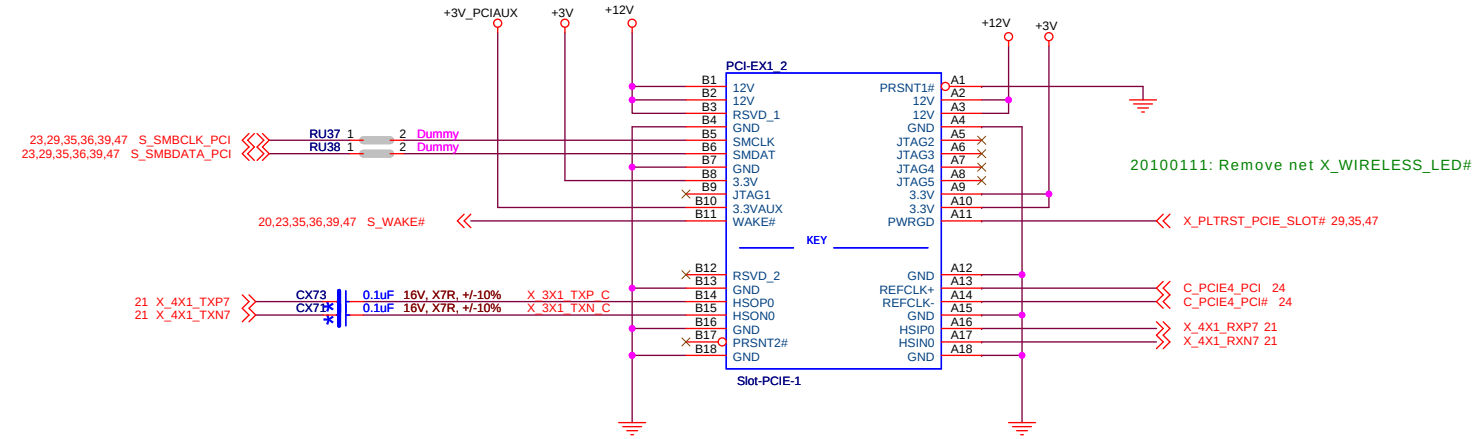
DWG NO

Goodyear

Rev A00

Date: 星期三, 二月 20, 2013 Sheet 47 of 57





DELL INC.

Title

Slot2.3: PCIe 1x

DWG NO

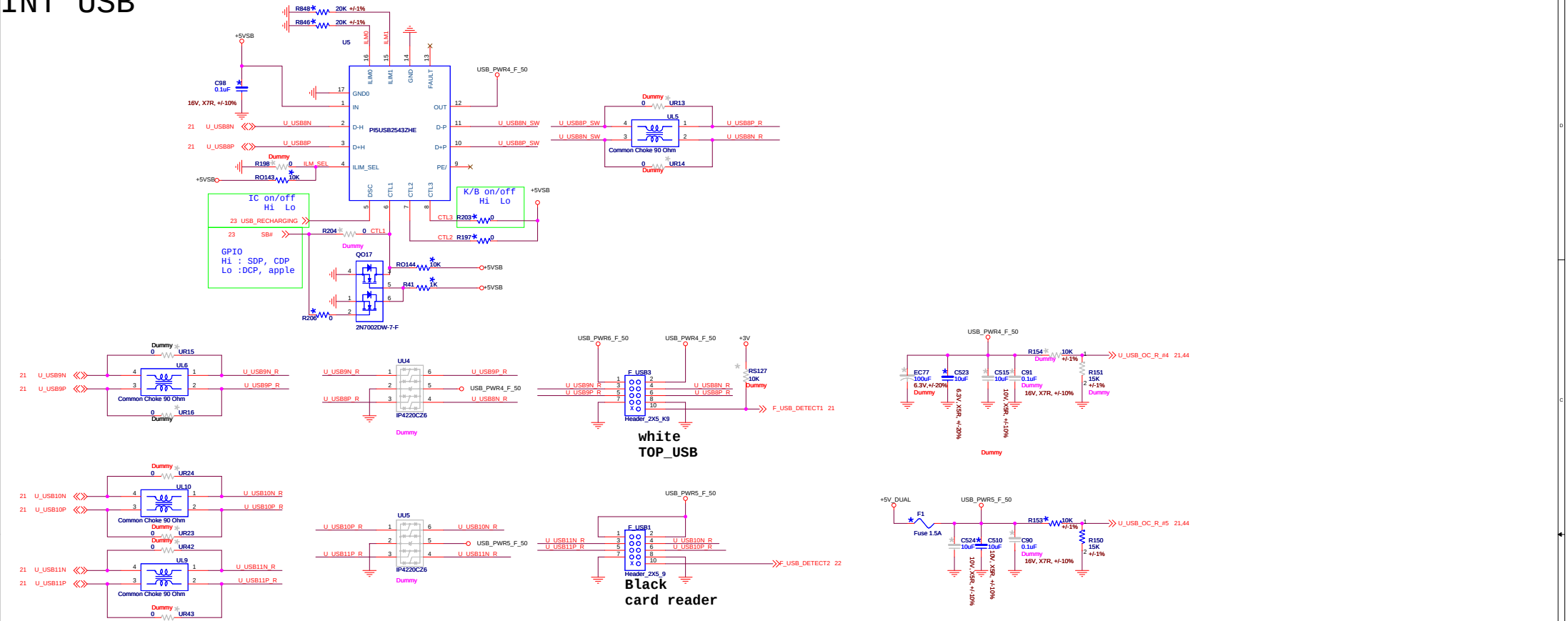
Goodyear

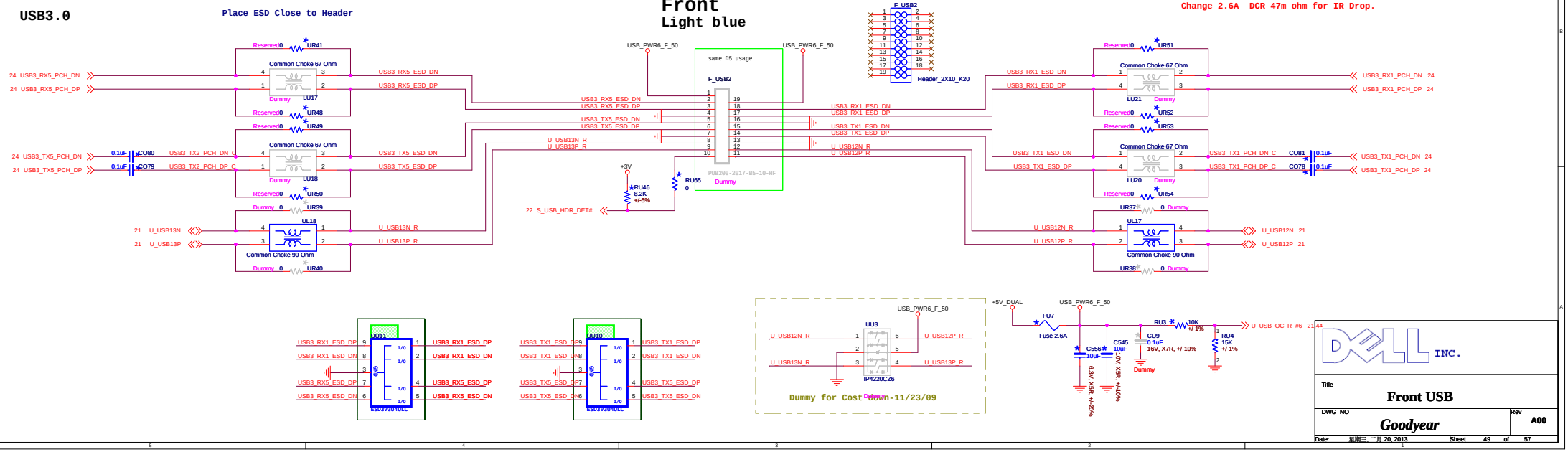
Rev

A00

Date: 星期三, 二月 20, 2013 Sheet 48 of 57

INT USB





DELL INC.

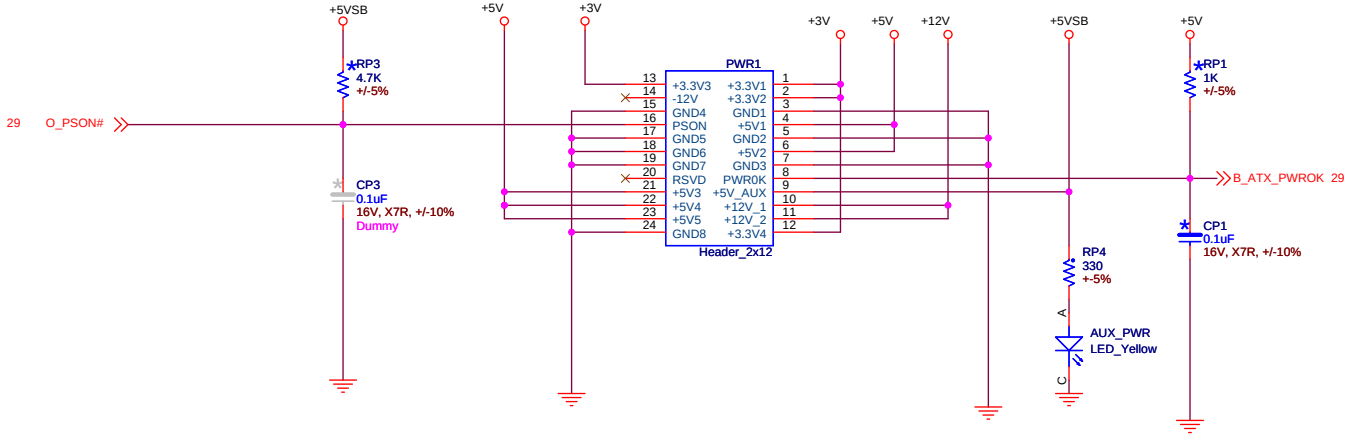
Title: **Front USB**

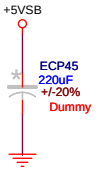
DWG NO: **Goodyear**

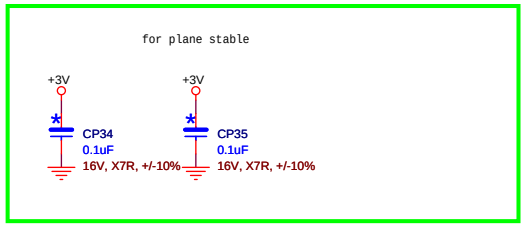
Rev: **A00**

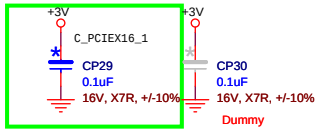
Date: 星期三, 三月 20, 2013 Sheet 49 of 57

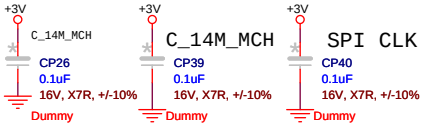
ATX POWER CONNECTOR

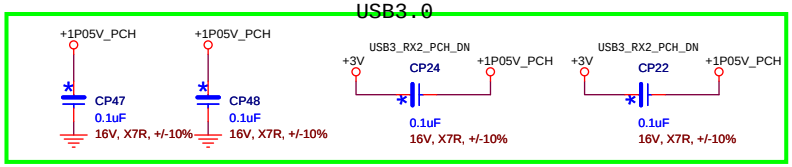


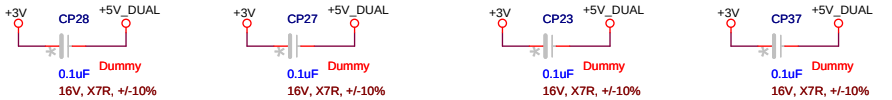


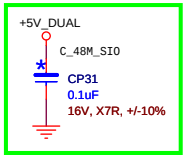


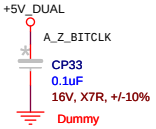


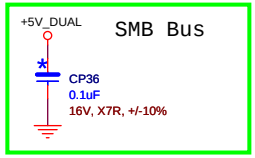


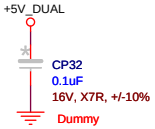


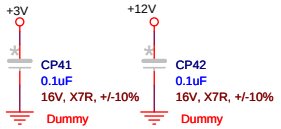












DELL INC.

Title

Power Conn

DWG NO

Goodyear

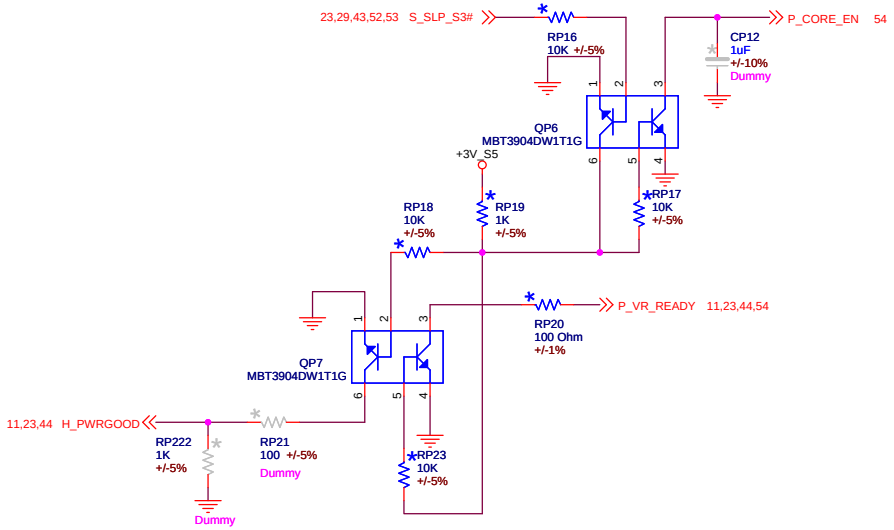
Rev

A00

Date: 星期三, 二月 20, 2013 Sheet 50 of 57

For Deep Sleep

VR_READY DEFENSIVE



DELL INC.

Title

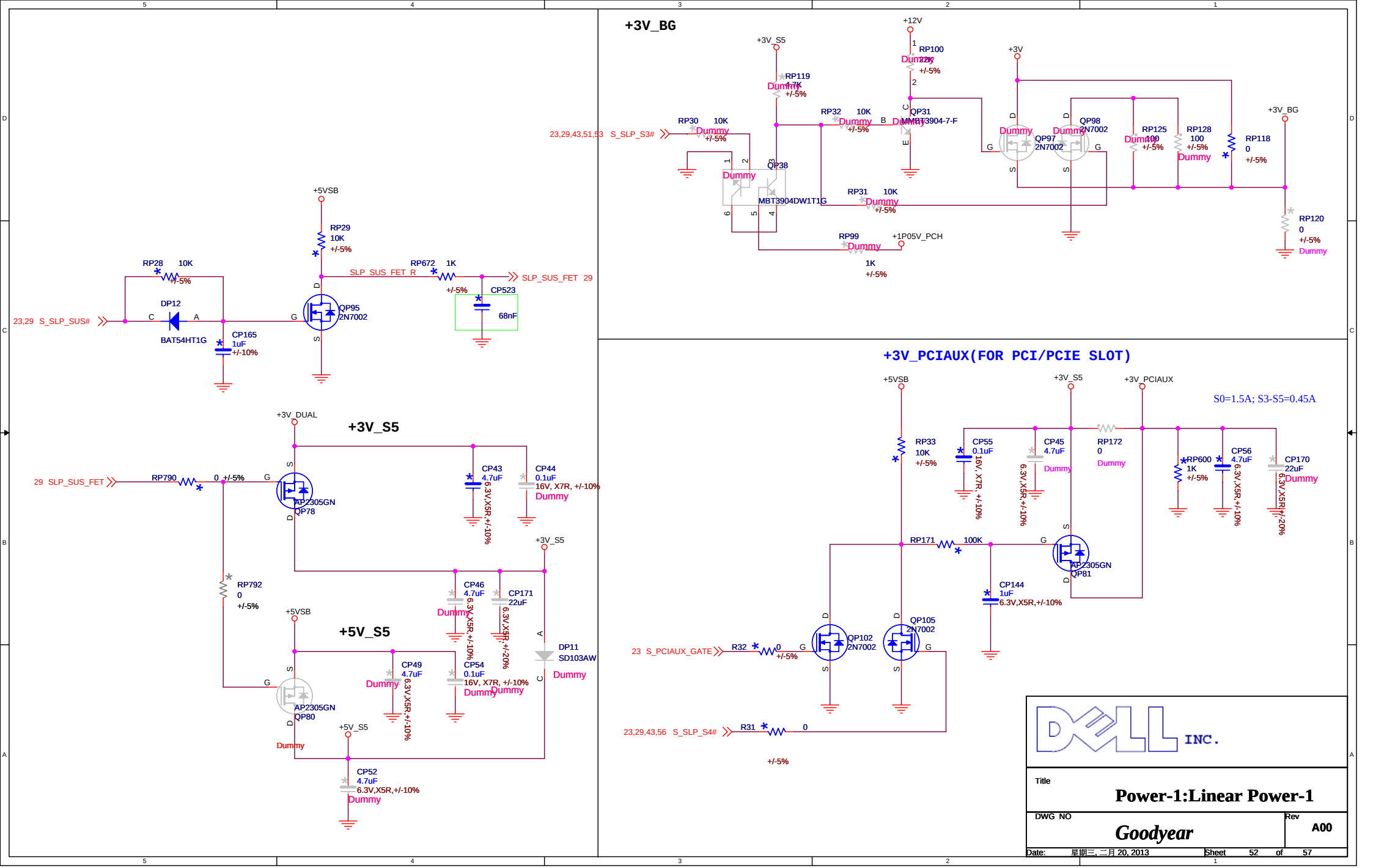
Power Sequence

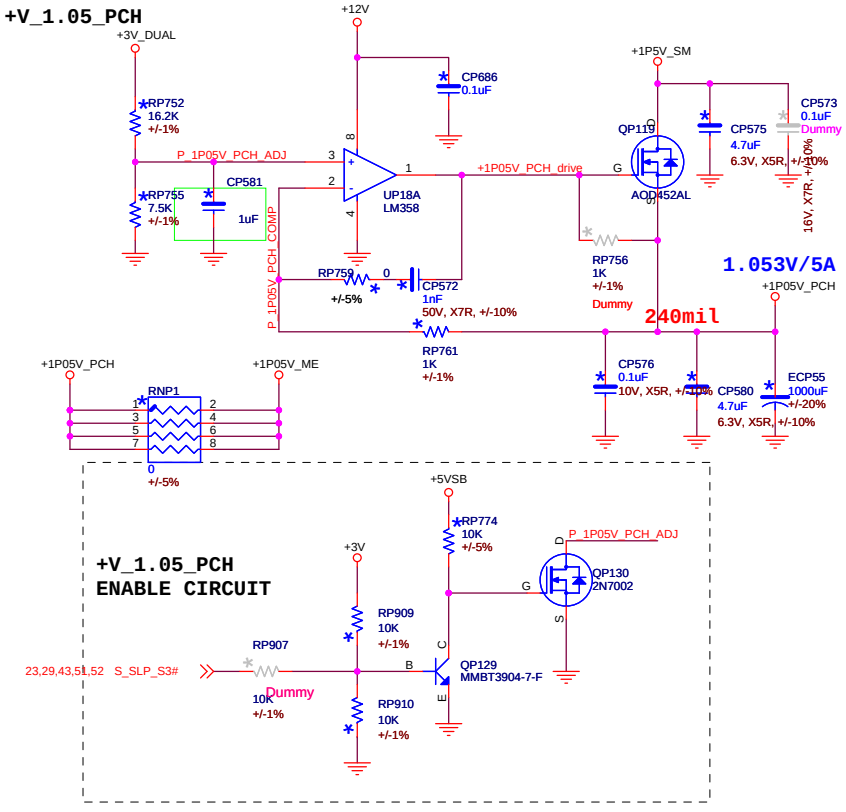
DWG NO

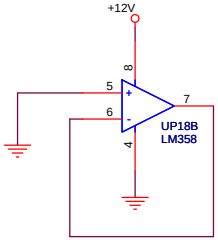
Goodyear

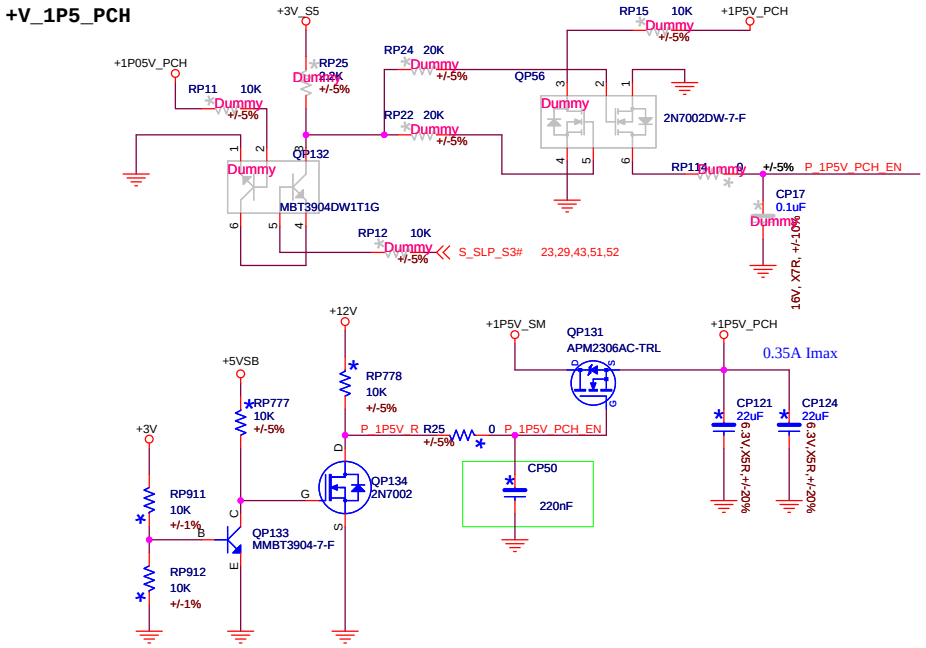
Rev A00

Date: 星期三, 二月 20, 2013 Sheet 51 of 57


+3V_BG
+12V
+3V_S5
RP100
22K
+/-5%
Dummy
RP119
4.7K
+/-5%
Dummy
RP30 10K
Dummy
+/-5%
23,29,43,51,53 S_SLP_S3#
RP32 10K
Dummy
+/-5%
QP31
MMBT3904-7-F
Dummy
+3V
QP98
2N7002
Dummy
QP97
2N7002
Dummy
RP125
100
+/-5%
Dummy
RP128
100
+/-5%
Dummy
RP118
0
+/-5%
+3V_BG
RP120
0
+/-5%
Dummy
QP38
Dummy
MBT3904DW1T1G
RP31 10K
Dummy
+/-5%
RP99
Dummy
+1P05V_PCH
1K
+/-5%
+5VSB
RP29
10K
+/-5%
RP28 10K
+/-5%
SLP_SUS_FET_R
RP672 1K
+/-5%
SLP_SUS_FET 29
CP523
68nF
23,29 S_SLP_SUS#
DP12
BAT54HT1G
CP165
1uF
+/-10%
QP95
2N7002
+3V_DUAL
+3V_S5
29 SLP_SUS_FET
RP790
0 +/-5%
AP2305GN
QP78
CP43
4.7uF
6.3V,X5R,+/-10%
CP44
0.1uF
16V, X7R, +/-10%
Dummy
+3V_S5
RP792
0
+/-5%
CP46
4.7uF
6.3V,X5R,+/-10%
Dummy
CP171
22uF
6.3V,X5R,+/-20%
+5VSB
+5V_S5
DP11
SD103AW
Dummy
CP49
4.7uF
6.3V,X5R,+/-10%
Dummy
CP54
0.1uF
16V, X7R, +/-10%
Dummy
Dummy
AP2305GN
QP80
Dummy
+5V_S5
CP52
4.7uF
6.3V,X5R,+/-10%
Dummy
+3V_PCIAUX(FOR PCI/PCIE SLOT)
S0=1.5A; S3-S5=0.45A
+5VSB
+3V_S5
+3V_PCIAUX
RP33
10K
+/-5%
CP55
0.1uF
16V, X7R, +/-10%
CP45
4.7uF
6.3V,X5R,+/-10%
Dummy
RP172
0
Dummy
RP600
1K
+/-5%
CP56
4.7uF
6.3V,X5R,+/-10%
CP170
22uF
6.3V,X5R,+/-20%
Dummy
RP171
100K
AP2305GN
QP81
CP144
1uF
6.3V,X5R,+/-10%
23 S_PCIAUX_GATE
R32
0
+/-5%
QP102
2N7002
QP105
2N7002
23,29,43,56 S_SLP_S4#
R31
0
+/-5%
DELL INC.
Title
Power-1:Linear Power-1
DWG NO
Goodyear
Rev
A00
Date: 星期三, 二月 20, 2013
Sheet 52 of 57







DELL INC.

Title

Power-2:Linear Power-2

DWG NO

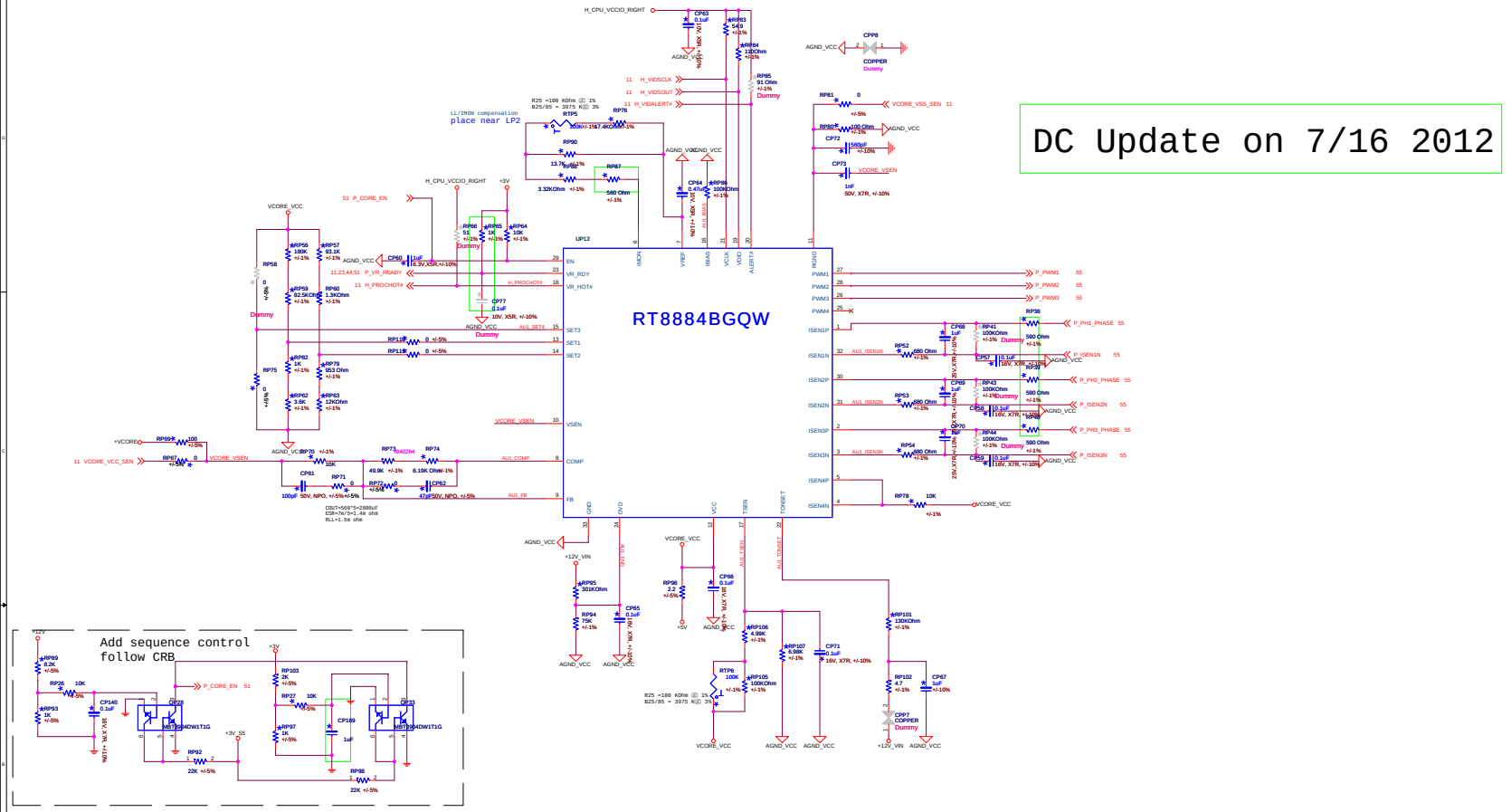
Goodyear

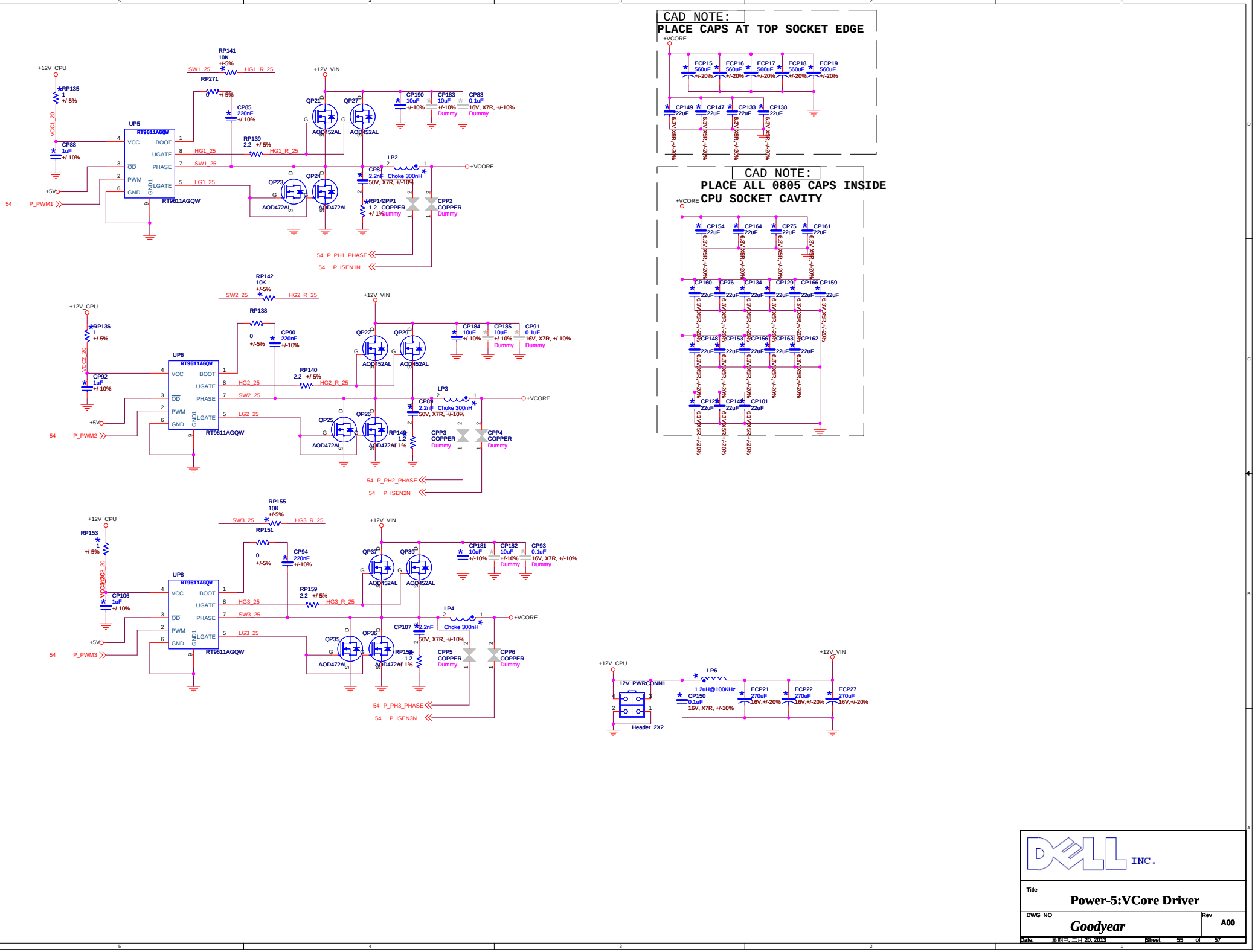
Rev

A00

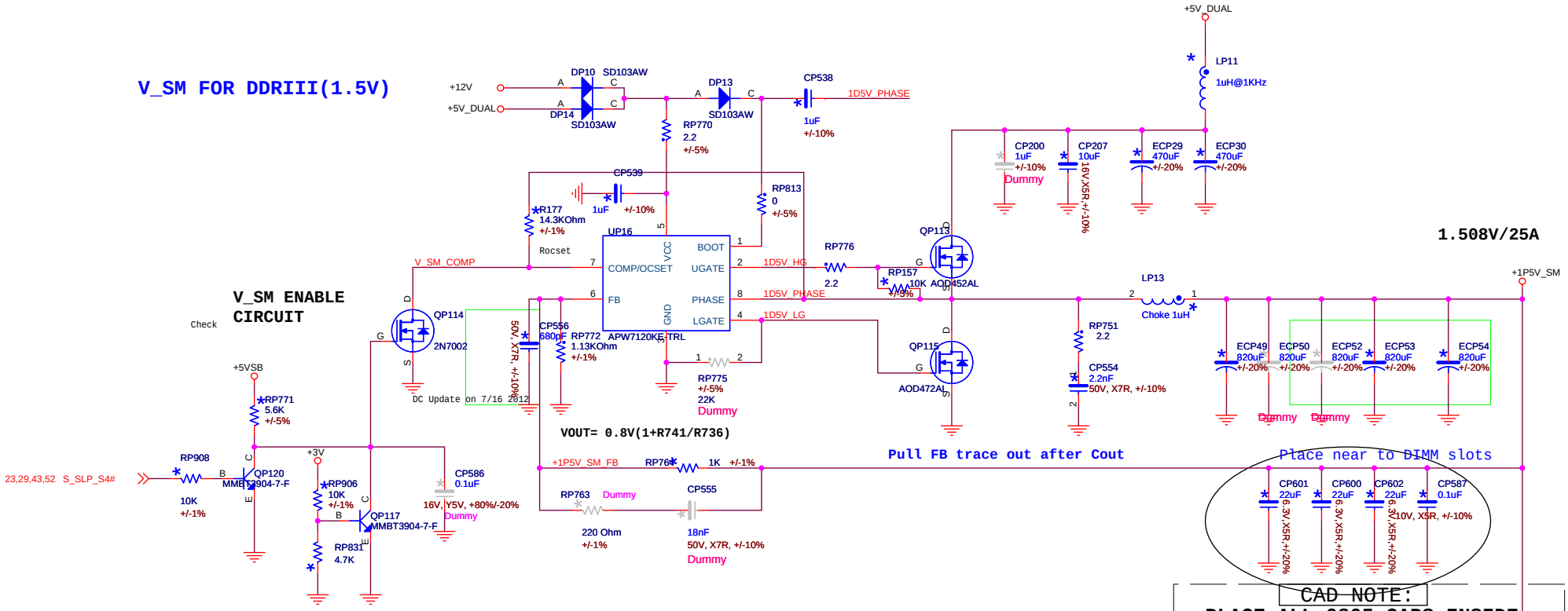
Date: 星期三, 二月 20, 2013

Sheet 53 of 57

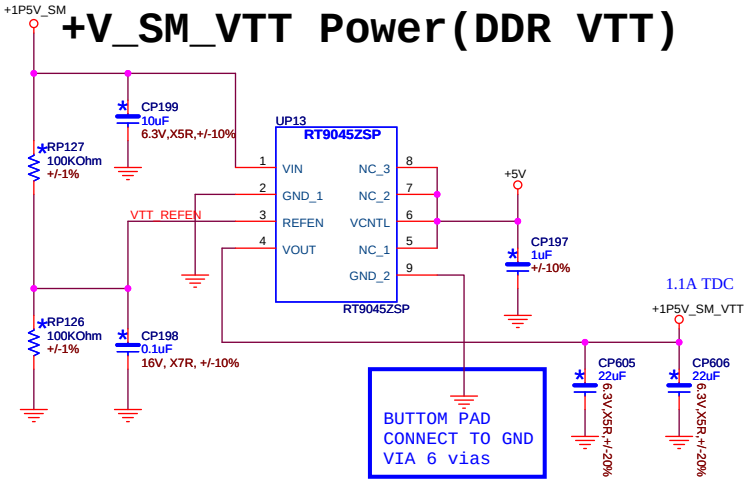

RT8884BGQW
UP12
Add sequence control
follow CRB
LL/IMON compensation
place near LP2
DC Update on 7/16 2012
Power-4:VCore
Goodyear
A00


CAD NOTE:
PLACE CAPS AT TOP SOCKET EDGE
CAD NOTE:
PLACE ALL 0805 CAPS INSIDE
CPU SOCKET CAVITY
+12V_CPU
+12V_VIN
+VCORE
+5V
RT9611AGQW
Header_2X2
Power-5:VCore Driver
Goodyear
A00
Sheet 55 of 57

+V_1.5_SM Power(DDRIII)



+V_SM_VTT Power(DDR VTT)



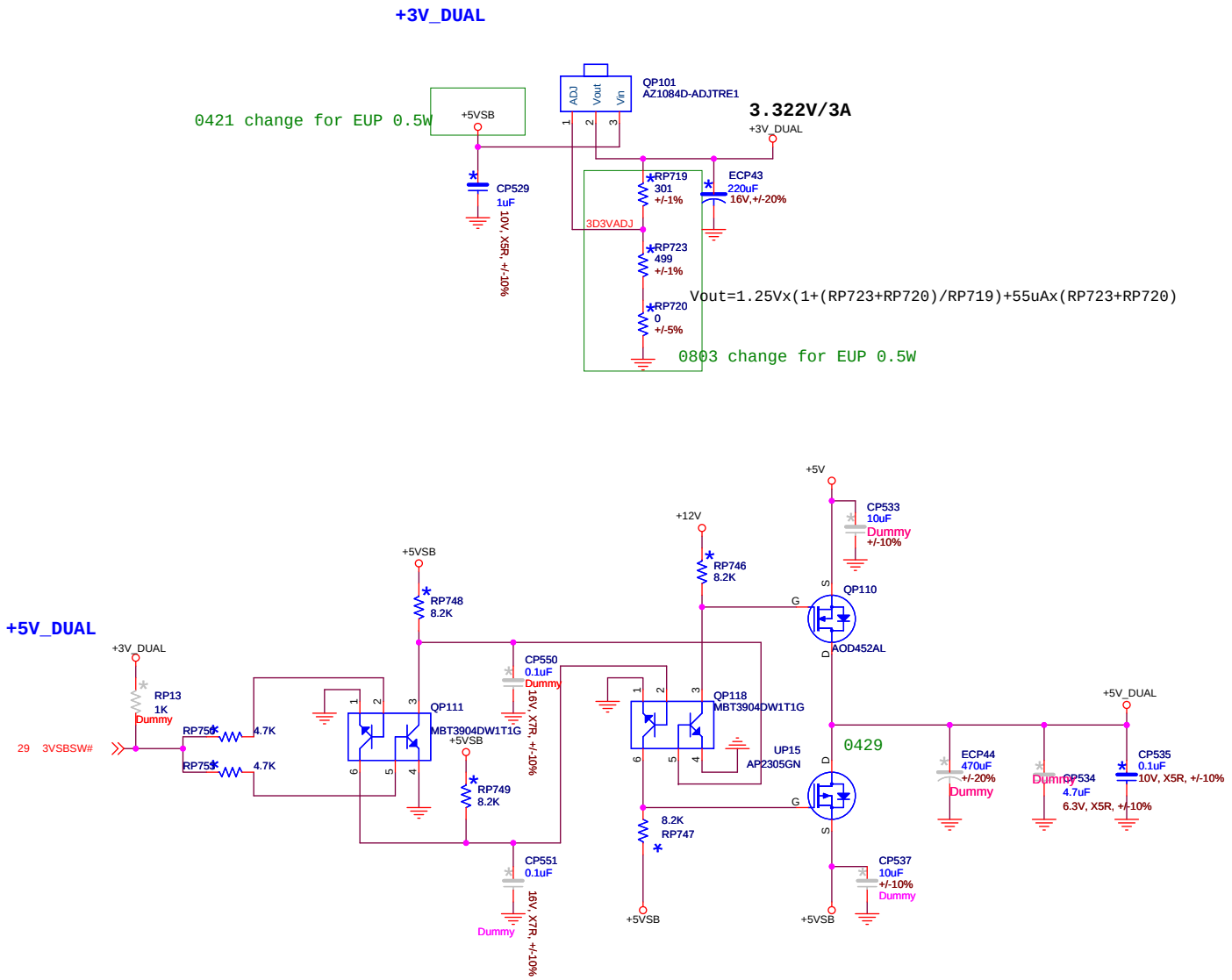
DELL INC.

Title: **Power-6: DDR3**

DWG NO: *Goodyear*

Rev: A00

Date: 星期三, 二月 20, 2013 Sheet 56 of 57



DELL INC.

Title

+5V_DUAL/+3V_DUAL

DWG NO

Goodyear

Rev A00

Date: 星期三, 二月 20, 2013 Sheet 57 of 57