Compal Confidential

** Schematics Document

AMD FP5 with DDR4

AIO M/B

01/21, 2021

REV : 1.0

Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

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Title: *Cover Page*		
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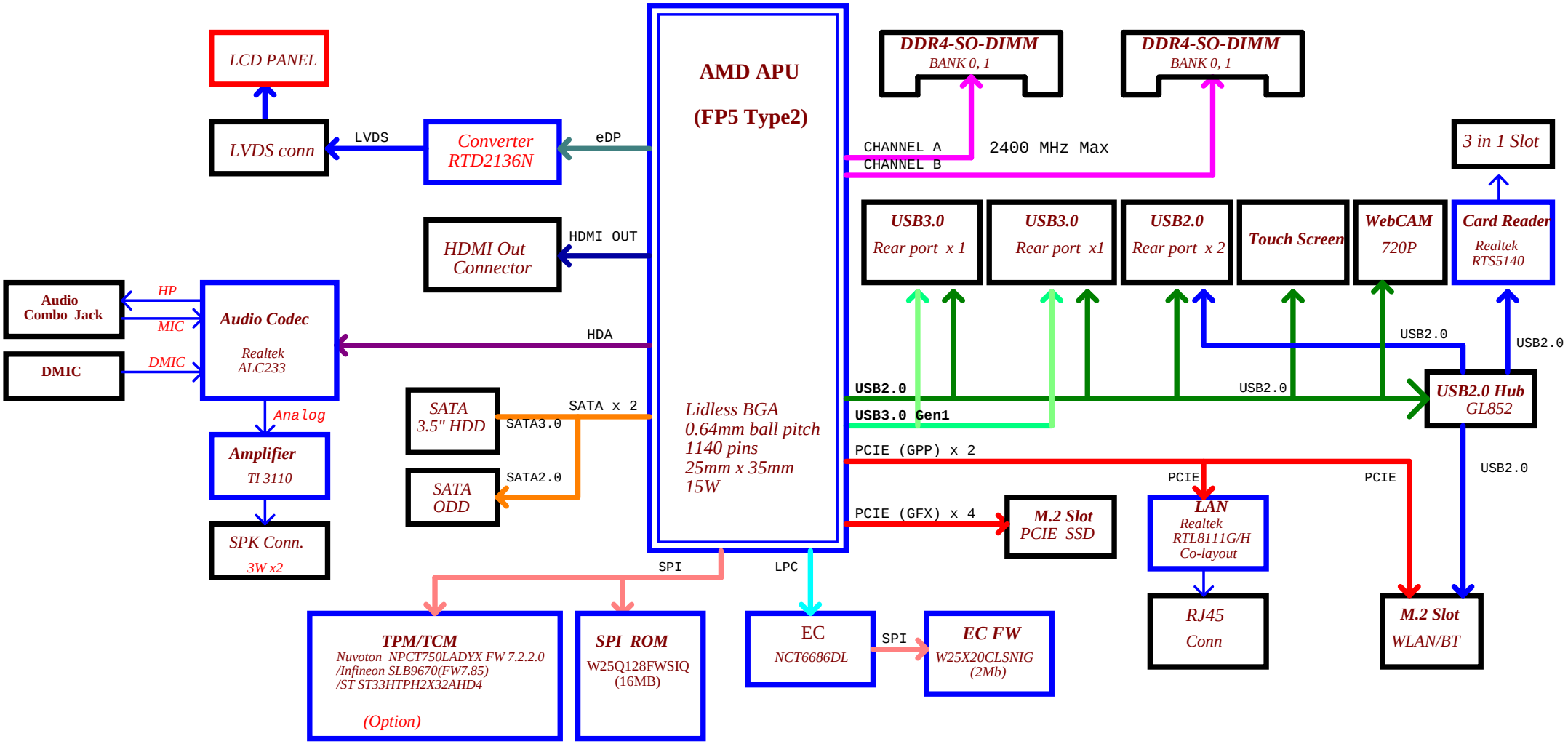
Block Diagram



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Title	Black Diagram		
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PCIE(GFX) Port Table

Port	Device
0	SSD
1	SSD
2	SSD
3	SSD

PCIE(GPP) Port Table

Port	Device
0	LAN
1	WLAN
2	NC
3	NC

SATA Port Table

Port	Device
0	HDD
1	ODD

DP Port Table

Port	Device
0	eDP
1	HDMI
2	NC

USB2.0 Port Table

Port	Device	OC# Pin
0	CAMERA	OC#0
1	USB 2.0 Rear IO Port 2	OC#0
2	USB 3.1 Rear IO Port1	OC#2
3	USB 3.1 Rear IO Port2	OC#3
4	USB 2.0 HUB	NA
5	TOUCH	NA

USB2.0 HUB Port Table

Port	Device
1	WLAN/BT
2	Card Reader
3	USB 2.0 Rear IO Port 1
4	NC

USB3.0 Port Table

Port	Device
0	NC
1	NC
2	USB3.0 (Rear IO)
3	USB3.0 (Side IO)

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	

A

BOM Structure Table

BOM Structure	BTO Item
[illegible]	[illegible]

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+DC20V	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTC_APU_S5	1.5V RTC power	ON	ON	ON*
+3V3_DSW	3.3V DSW on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+1.8VALW_S5	1.8V always on power rail	ON	ON	ON
+0.9VALW_S5	0.9V always on power rail	ON	ON	ON
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+0.6VS_VTT_S0	0.6V switched power rail for DDR4 terminator	ON	OFF	OFF
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+12VS_S0	12V switched power rail	ON	OFF	OFF
+1.8VS_S0	1.8V switched power rail	ON	OFF	OFF
+0.9VS_S0	0.9V switched power rail	ON	OFF	OFF
+APU_VDDSOC	Core voltage for processor core current	ON	OFF	OFF
+APU_VDDCORE	Voltage for processor VDDCR	ON	OFF	OFF
+1.5VS_CODEC_S0	1.5V for Audio Codec AVDD2	ON	OFF	OFF

SKU (UMA&DIS) / GOC50/51 SDV BOM Configure Table

SKU (UMA&DIS)		GOC50/51 SDV BOM Configure Table
431AQ338L01 Converter	(UMA)	[illegible]
431AQ338L02 Converter	(UMA)	[illegible]
431AQ338L03 Converter	(UMA)	[illegible]
431AQ338L04 Converter	(UMA)	[illegible]
X4EAQ338L01	(EMC)	[illegible]

EC SM Bus0 Address

Device	Address	HEX
APU	1001-1000xb	98H

PCH SM Bus Address

Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1

EC SM Bus2 Address

Device	Address	HEX
Converter RTD-2136N	1001-0100xb	94H
LCD Backlight	0110-0010xb	62H

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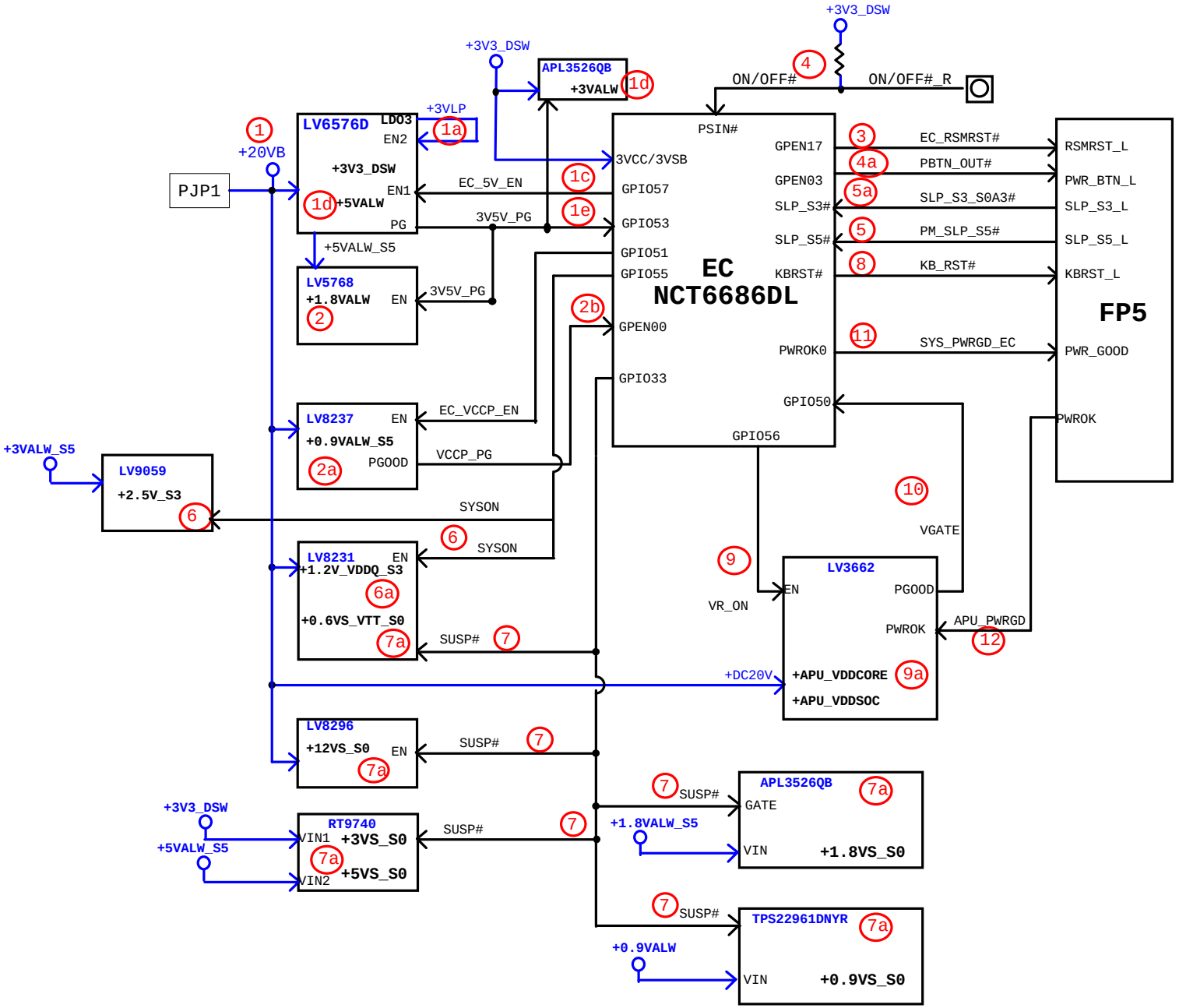

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			Size: Custom; Document Number: LA-K901P; Rev: 0.1
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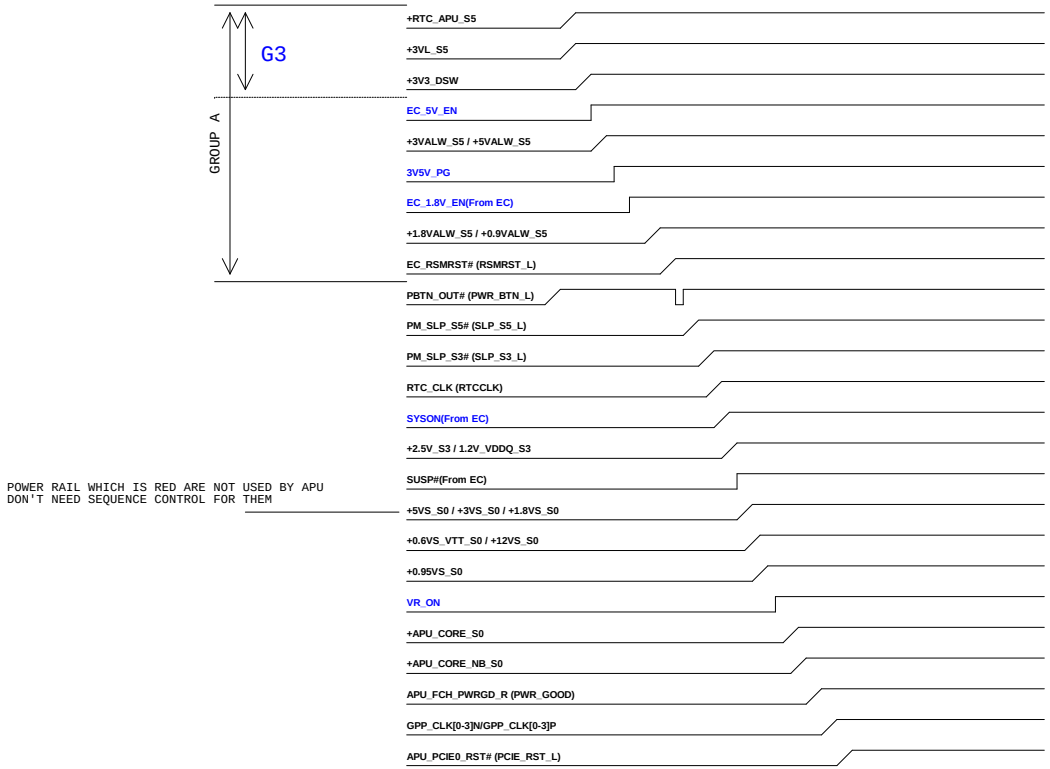
Platform Power Sequence

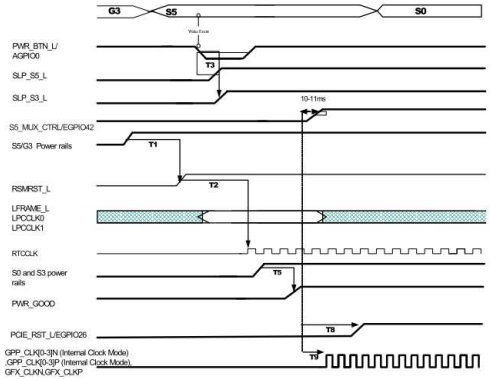
PCB NAME:
REVISION:
DATE:

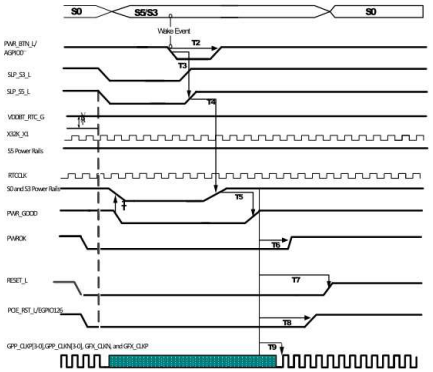
Power Sequence_AMD Dali FP5

G3->S5->S0



POWER RAIL WHICH IS RED ARE NOT USED BY APU
DON'T NEED SEQUENCE CONTROL FOR THEM





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Title: Power Sequence			
Size: Custom	Document Number: LA-K901P		Rev: 0.1
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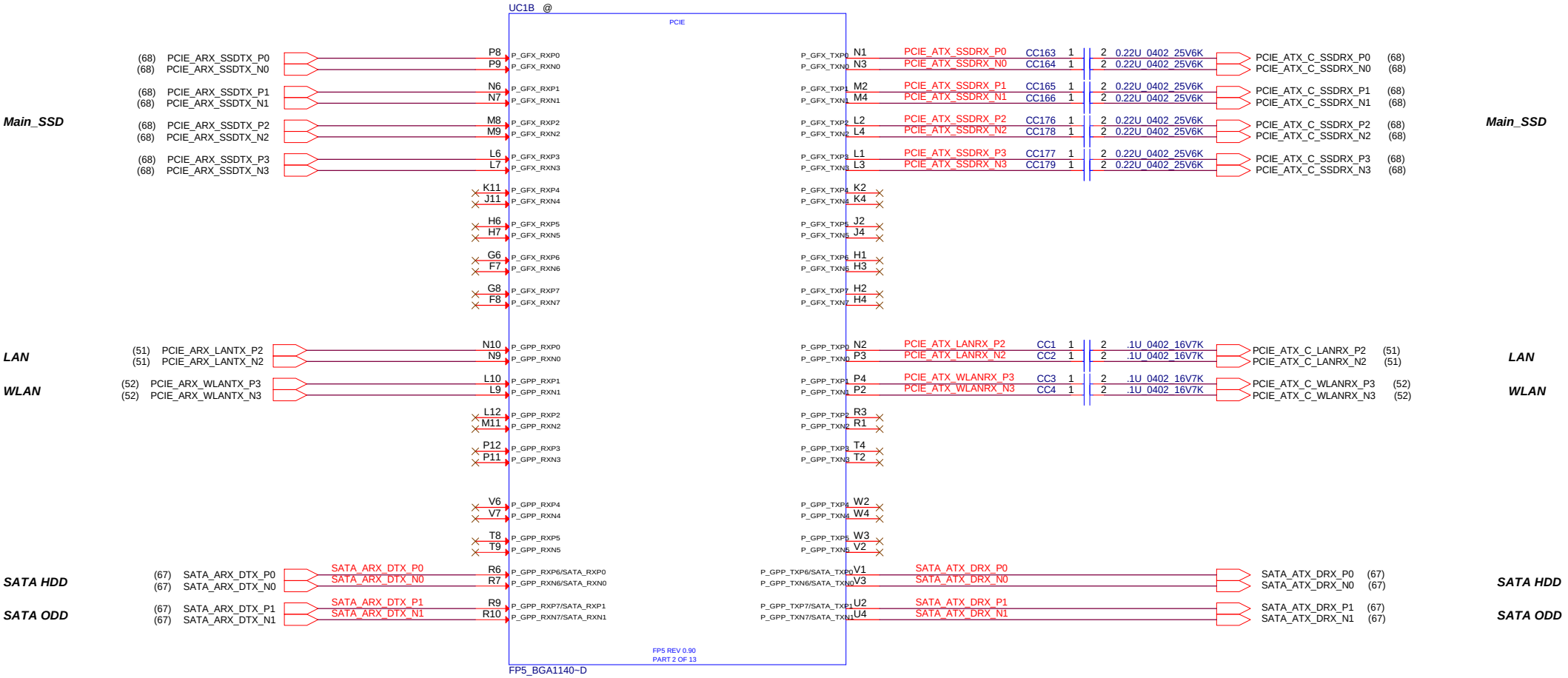
Main Func = CPU



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Title: FP5 PCIE/SATA

Size	Document Number	Rev
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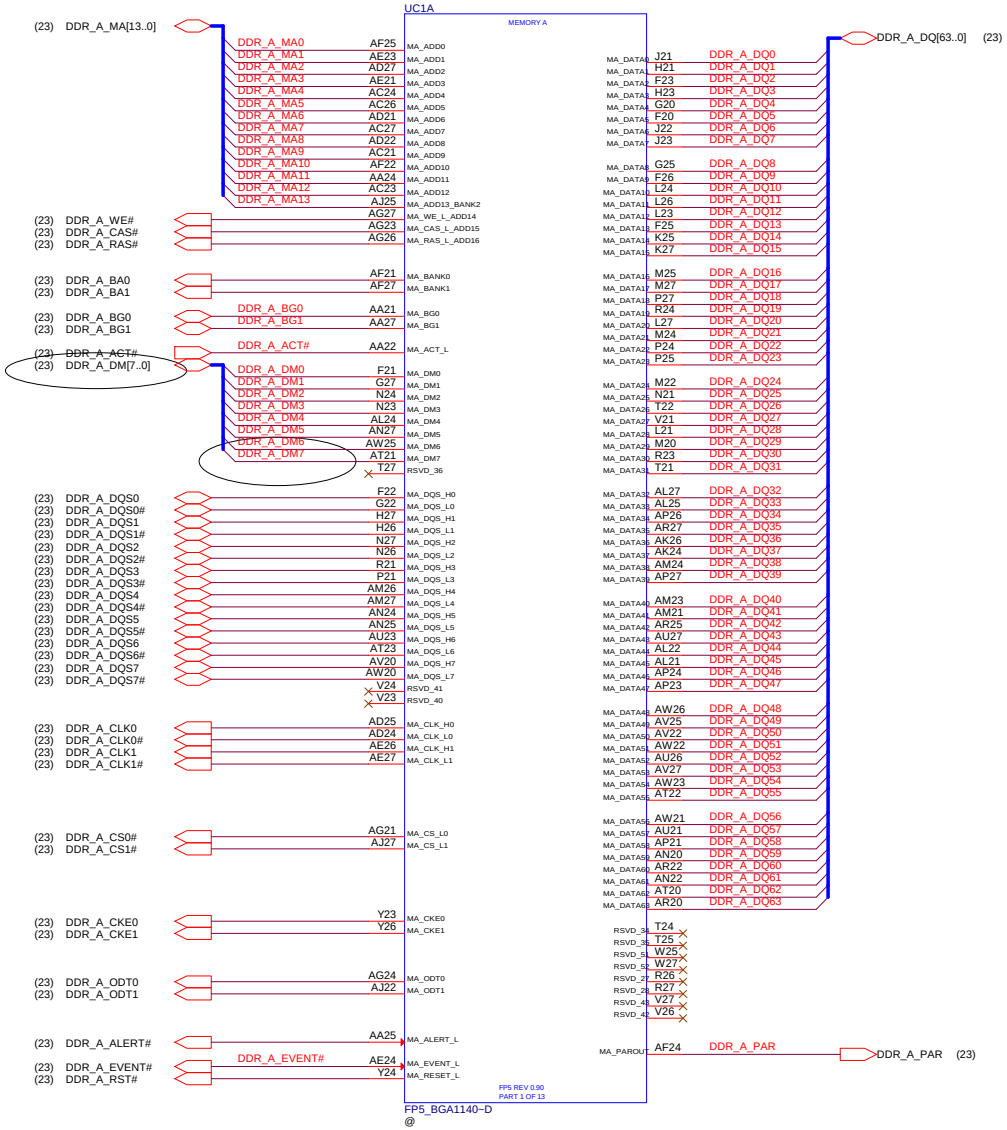

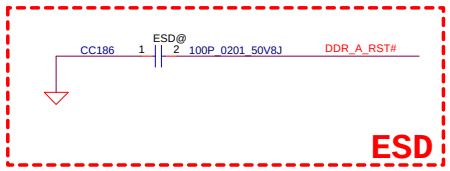

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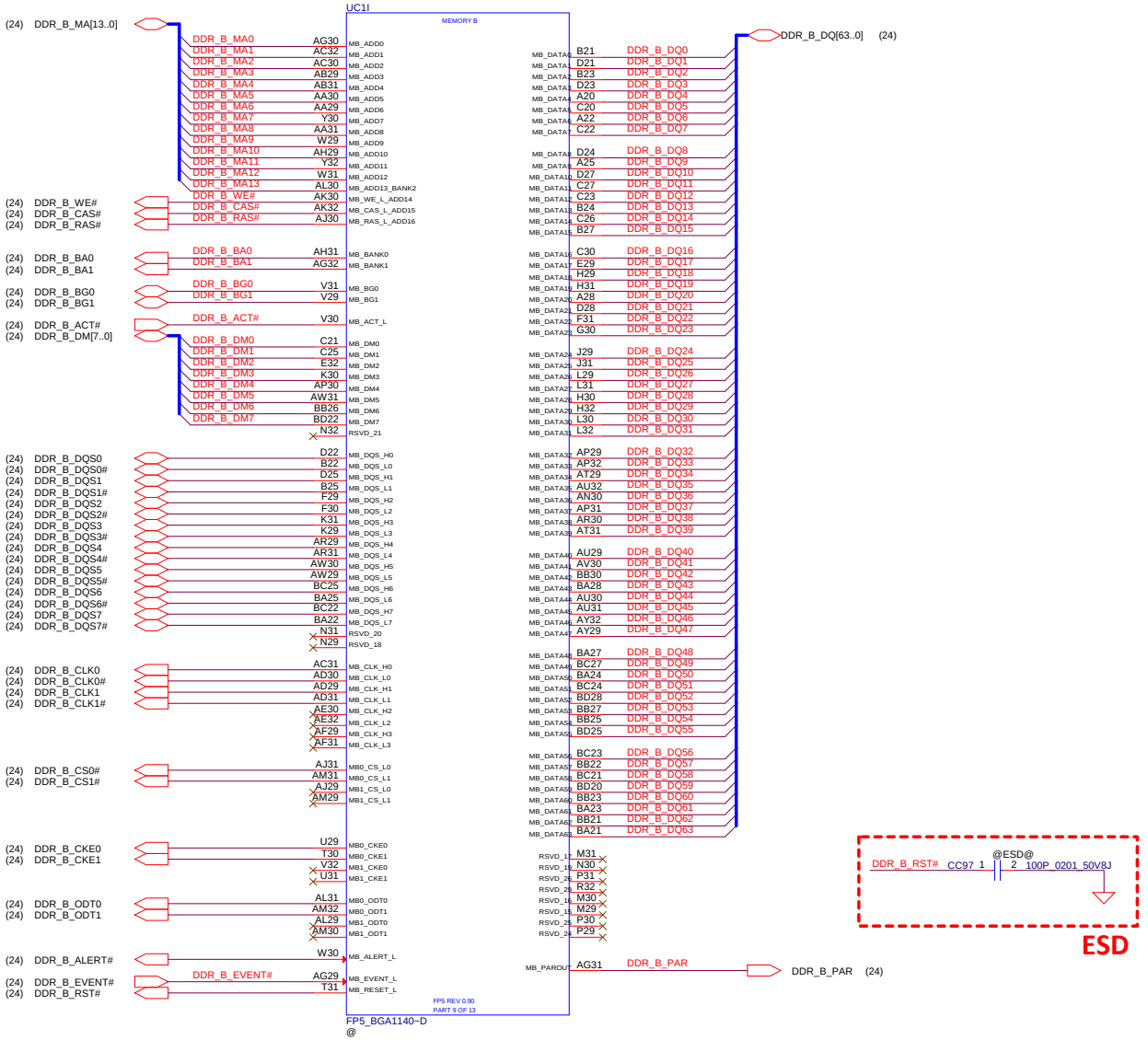
Main Func = CPU



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Main Func = CPU

DP0: eDP
DP1: HDMI
DP2: N/A
DP3: N/A

+LCDVDD_CONN PWR switch enable pin VIH=1.2V

eDP

HDMI

DP	DP x4			
	3	2	1	0
HDMI DP0 and DP1 DP2 and DP3 with retimer/redriver[3]	Channel Clock	Ch 0	Ch 1	Ch 2

20210121 Add CC193/CC194 on APU_SIC/SID to avoid undershoot.

ESD

Reserve for Sequence Tuning

HDT+ (debug + HDT@)

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Issued Date	2019/08/01	Deciphered Date 2019/12/25

Compal Electronics, Inc.

Title: FP5 DISP/MISC/HDT

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Main Func = CPU

ESD

EMI

20201005 SSD1_PWR_EN Pull-down 2.2K

20200910 Add Panel_ID on APU GPIO

20200926 RC181 change to 2.2K follow PDG

20201113 TPM MODE change to AGPIO130

20201005 SSD1_PWR_EN# correct to SSD1_PWR_EN

20201121 VR_ID change to use AGPIO89

20201012 Remove TPM_STSIRQ# route to AGPI085

PU on EC side

STRAPS

STRAPS	DEFINITION
SPI_CLK	1 : Use 48MHZ Crystal Clock and Generate both internal and external clocks (Default) 0 : Use 100MHZ PCIE clock as reference clock and generate internal clocks only
SYS_RST#	1 : Normal reset mode (Default) 0 : short reset mode

Modern Standby STRAPS

Function	Strap GPIO
MSB	1
MSB@	0

20200910 remove MIC_SEL

MIC STRAPS

20200910 remove DSP_SEL

DSP STRAPS

20200929 SMART_PWR_SEL change pull-high to +3VS_S0

Function	Strap GPIO
SMART	1
SMART@	0

SMRT POWER STRAPS

20201113 TPM MODE change pull-high to +3VALW_S5

Function	Strap GPIO
TPM	1
TPM@	0

TPM STRAPS

Reserve

20210121 Remove DGPU_Present

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Compal Electronics, Inc.

Title: FP5 GPIO/AZ/MISC/STRAPS

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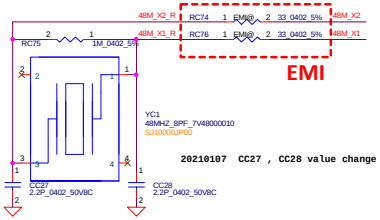
Main Func = CPU

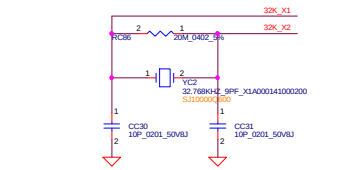
20200929 APU_SPI_TPMCS# reseve 10K pull-up +1.8VALW_S5 (AMD SCL)

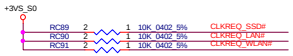
48MHz CRYSTAL

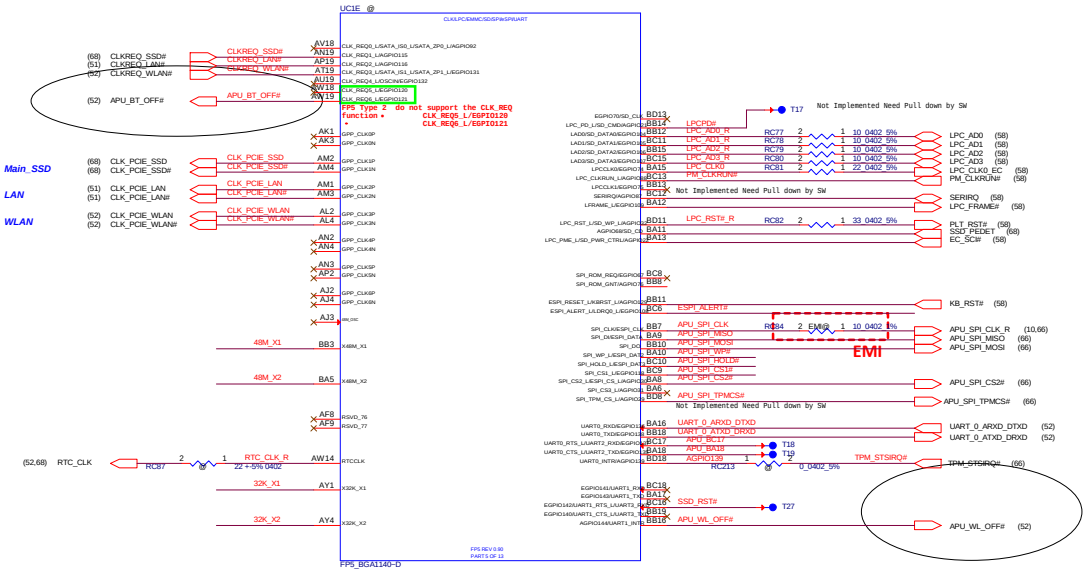


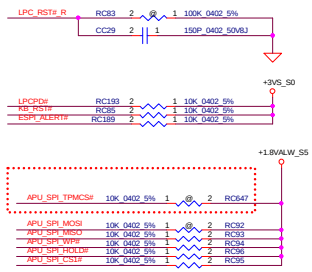
20210107 CC27 , CC28 value change to 2.2P

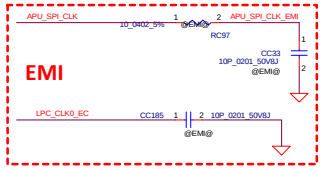
32.768KHz CRYSTAL

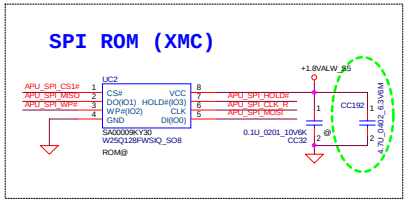




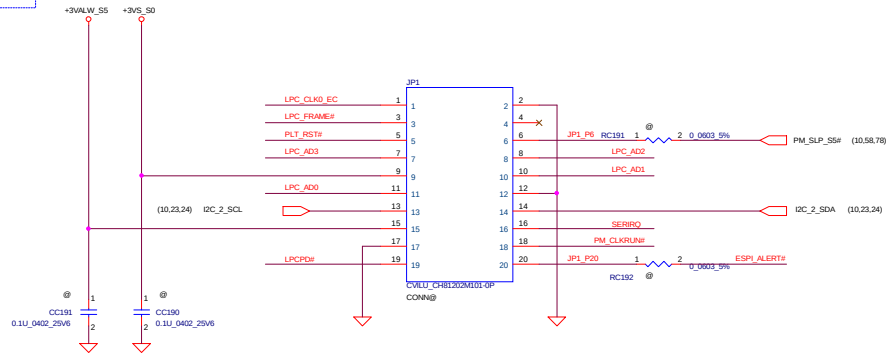








20210120 Remove JROM2



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Issued Date	2019/08/01	Deciphered Date 2019/12/25	Title: FP5 CLK/LPC/SPI
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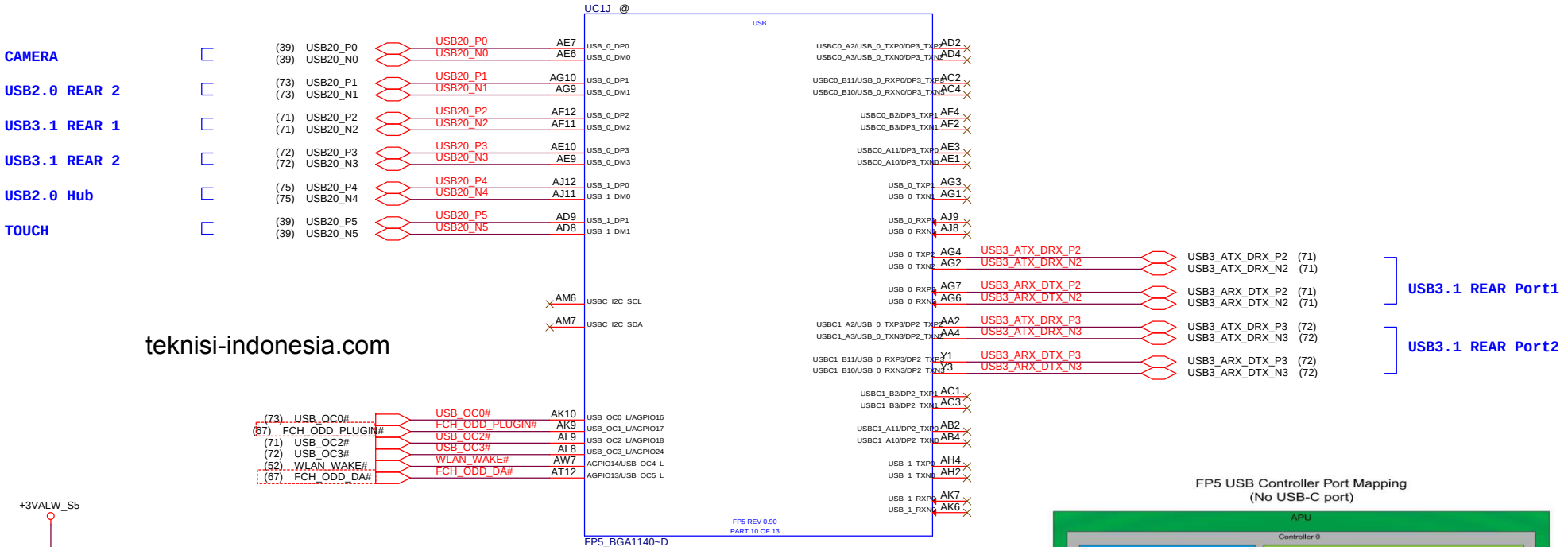

20201117 Add FCH_ODD_PLUGIN# on AGPIO17
20201117 Add FCH_ODD_DA# on AGPIO13

20201117 RC648/RC649 pull-high +3VALW_S5 , FCH_ODD_PLUGIN#/FCH_ODD_DA#

FP5 USB Controller Port Mapping
(No USB-C port)

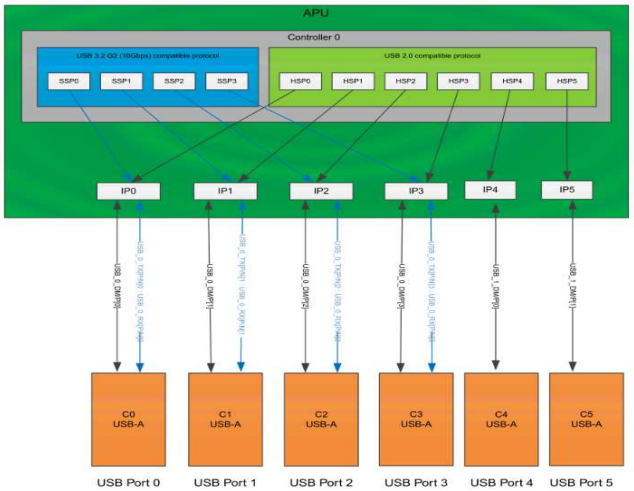

Figure 98. FP5 Type 2 Processor USB Controller to Port Mapping—No USB-C Connector

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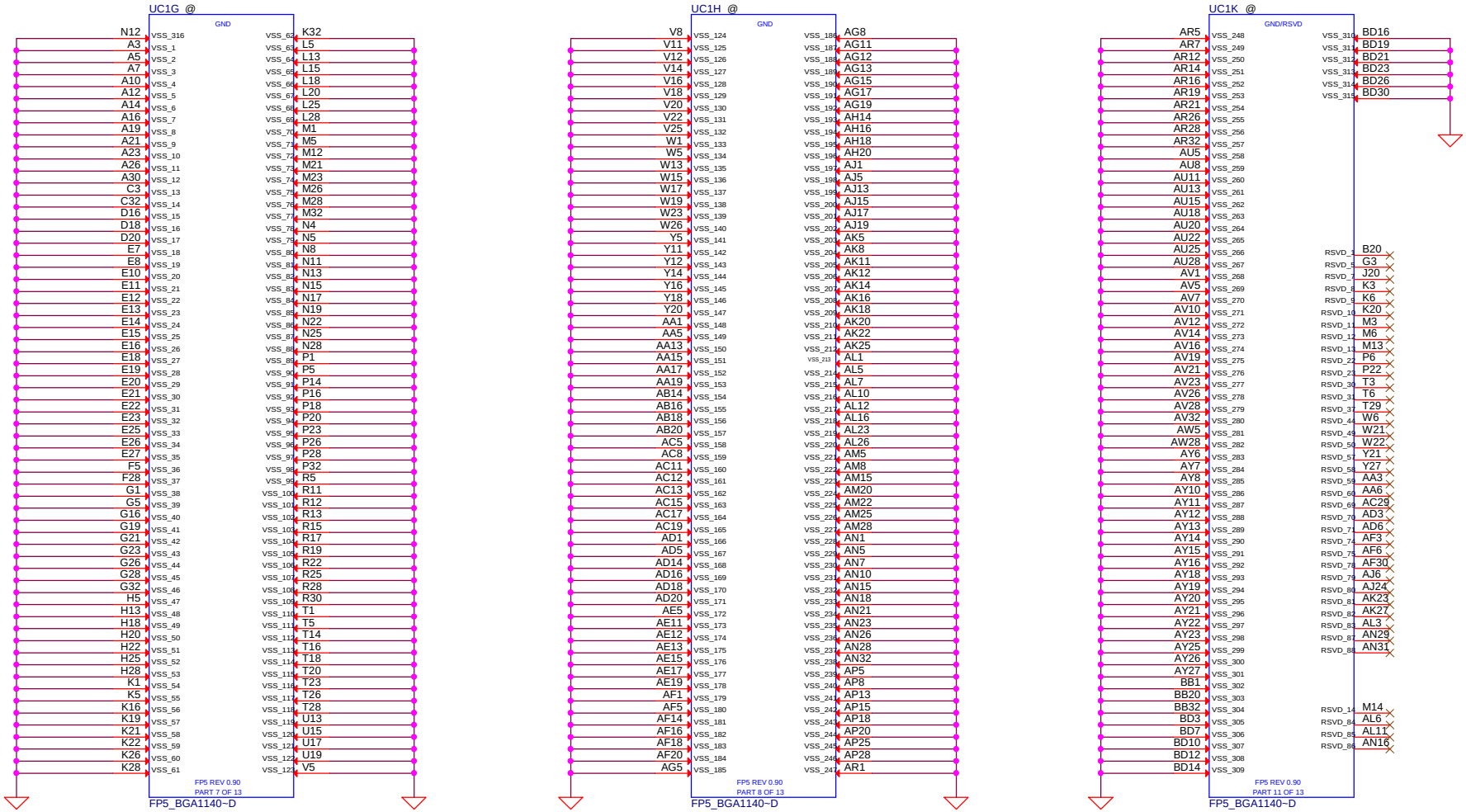

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Title: FP5 GND

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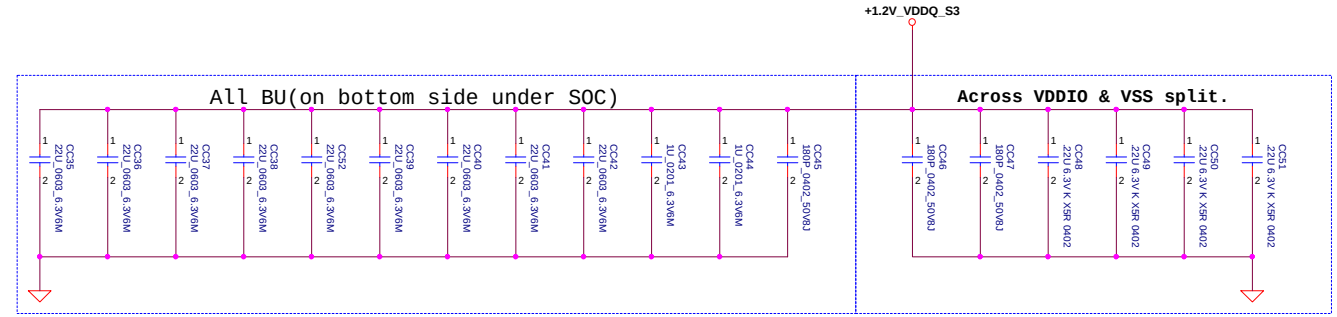
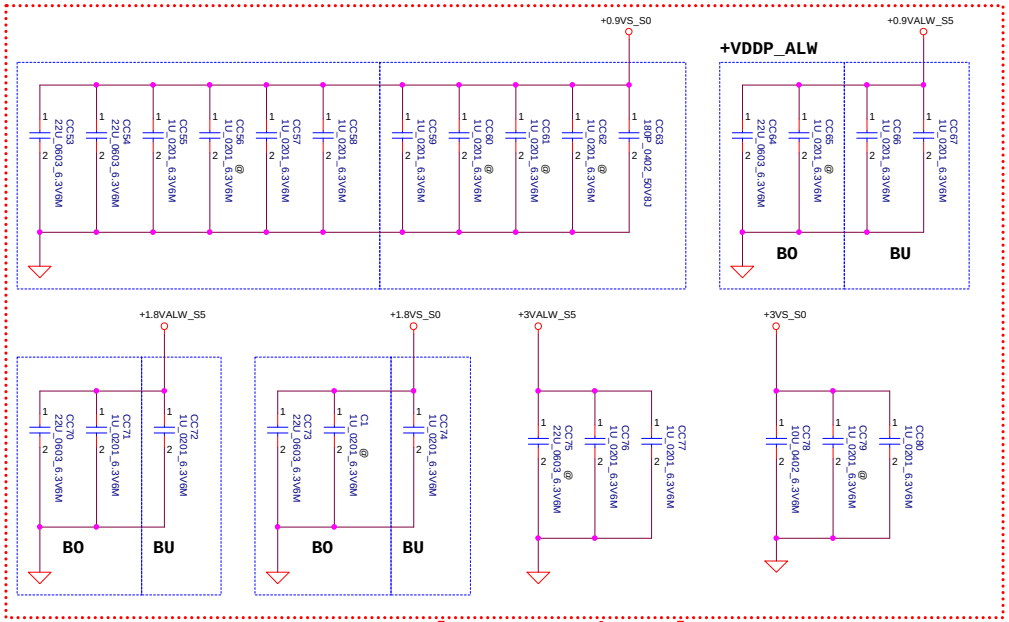
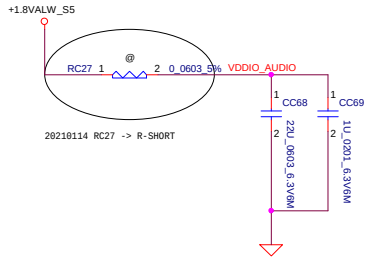
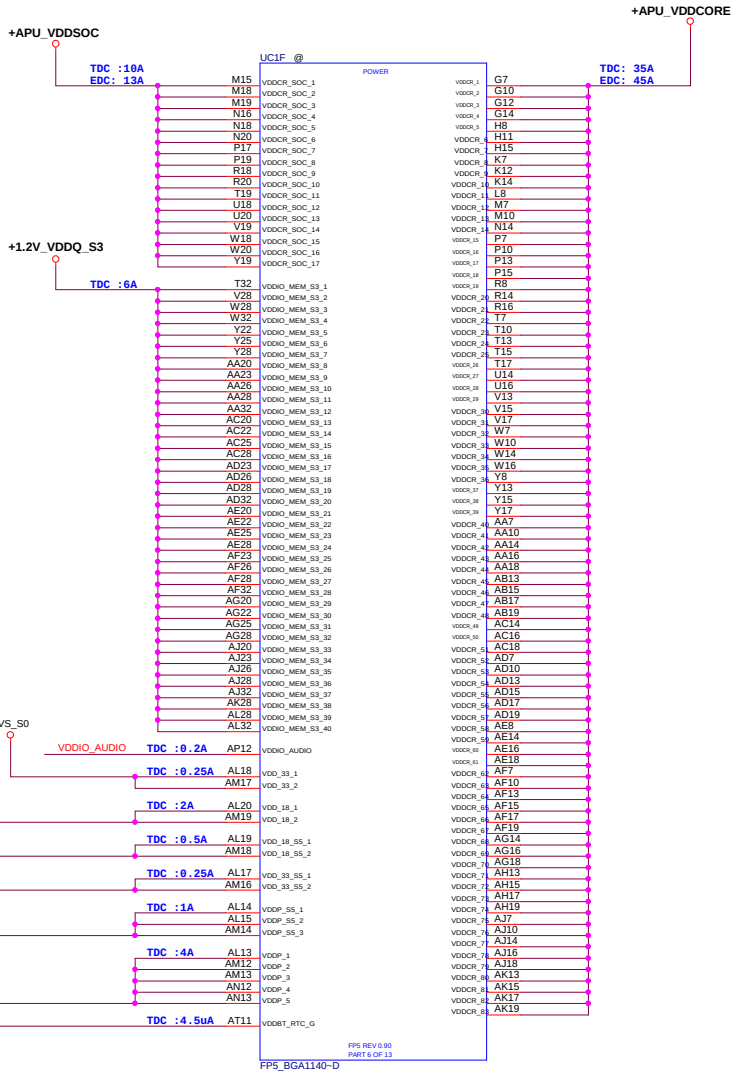
Main Func = CPU



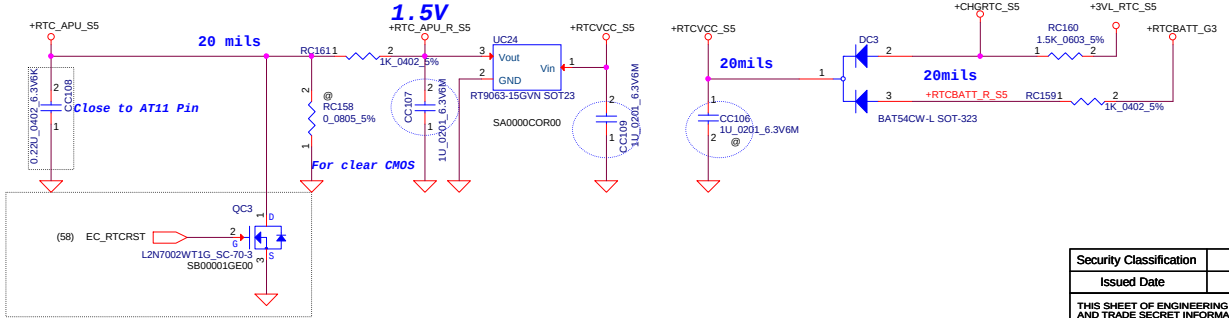


Note : Cap placemet need to close APU





RTC OF APU



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Title	FP4 PWR		
Size	Custom	Document Number	LA-J691P01
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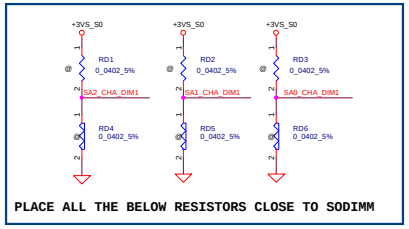
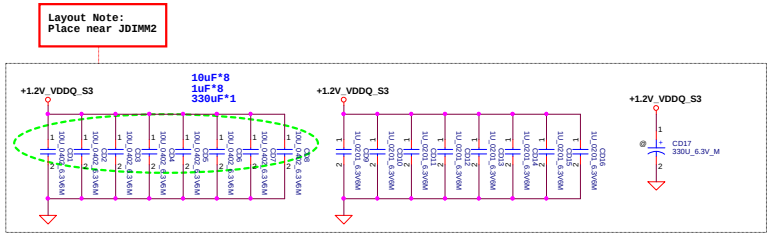
CHANNEL-A

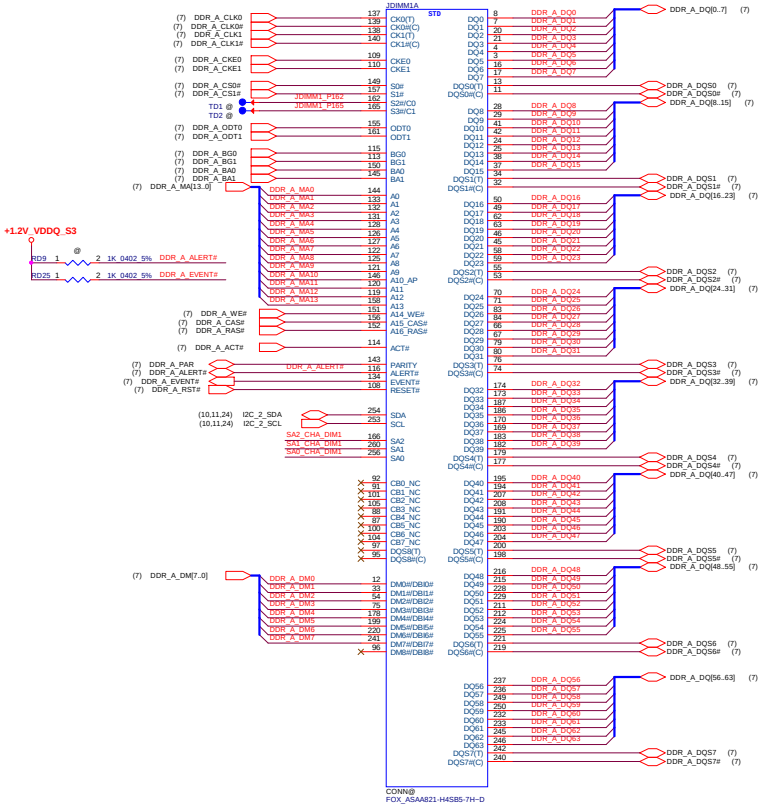


SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:
READ ADDRESS:
SA0 = 1; SA1 = 0; SA2 = 0.

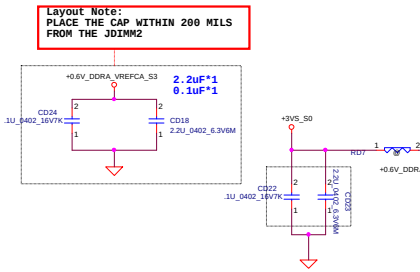


20210114 CD1,CD2,CD3,CD4,CD5,CD6,CD7,CD8 SE000005T80 (10U_0603) --> SE00000UD00 (10U_0402)

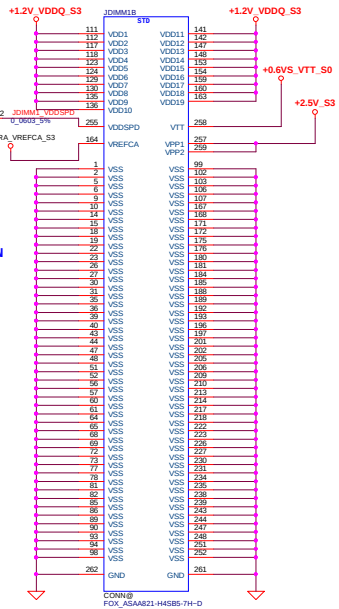
(4.0 mm) STD

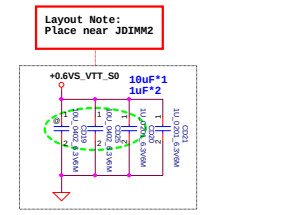


SP07001OK0L

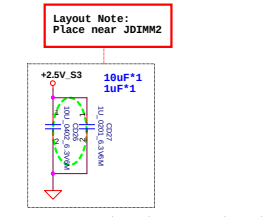


PLACE NEAR TO PIN

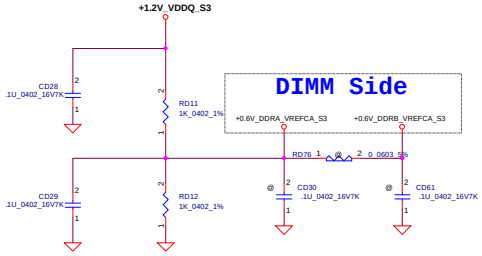




20210114 CD19 , CD25 SE000005T80 (10U_0603) --> SE00000UD00 (10U_0402)



20210114 CD26 SE000005T80 (10U_0603) --> SE00000UD00 (10U_0402)



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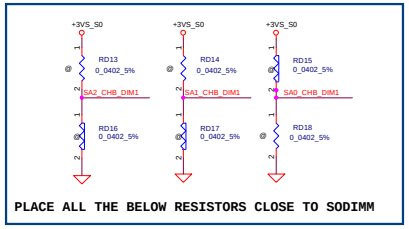
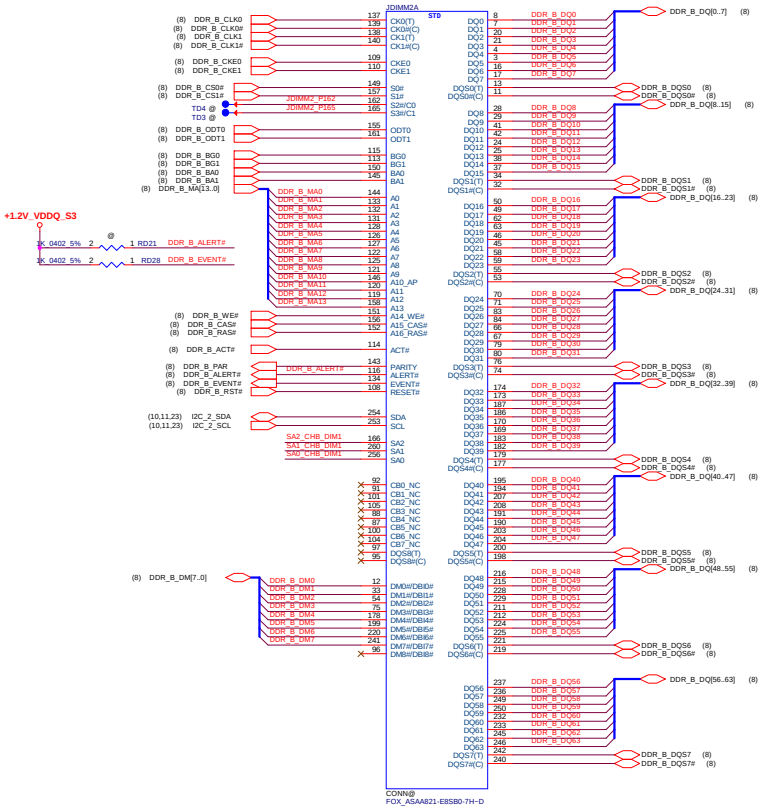
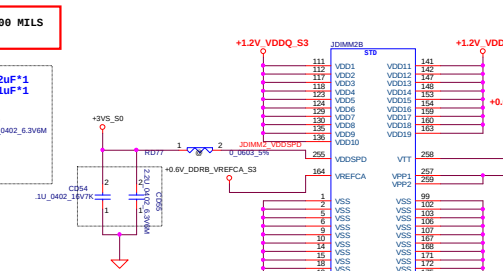
CHANNEL-B

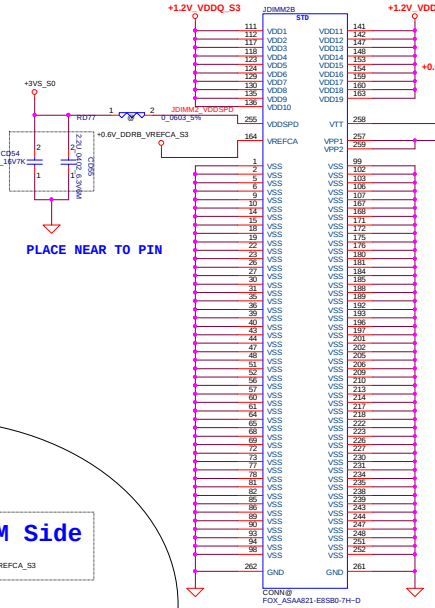


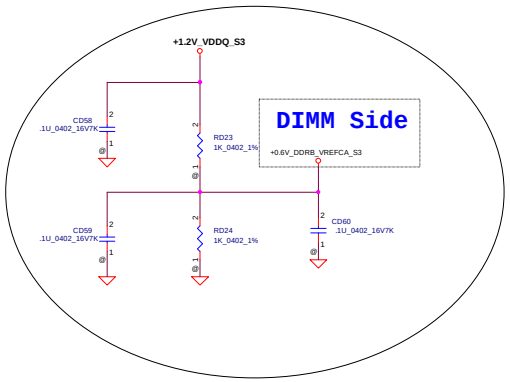
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:
READ ADDRESS:
SA0 = 0; SA1 = 0; SA2 = 0.

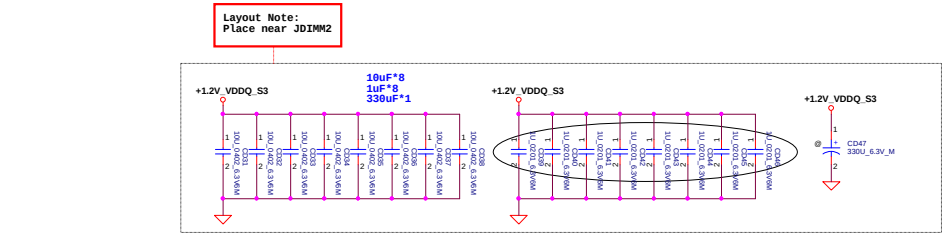
(8.0 mm) STD



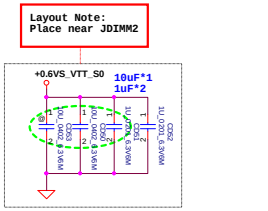




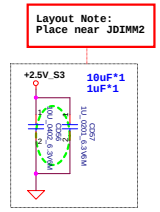




20210114 CD31~38 SE000005T80 (10U_0603) --> SE00000UD00 (10U_0402)



20210114 CD53 , CD50 SE000005T80 (10U_0603) --> SE00000UD00 (10U_0402)



20210114 CD56 SE000005T80 (10U_0603) --> SE00000UD00 (10U_0402)

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/08/01	Deciphered Date 2018/10/01	Title: DDR4_DIMM2
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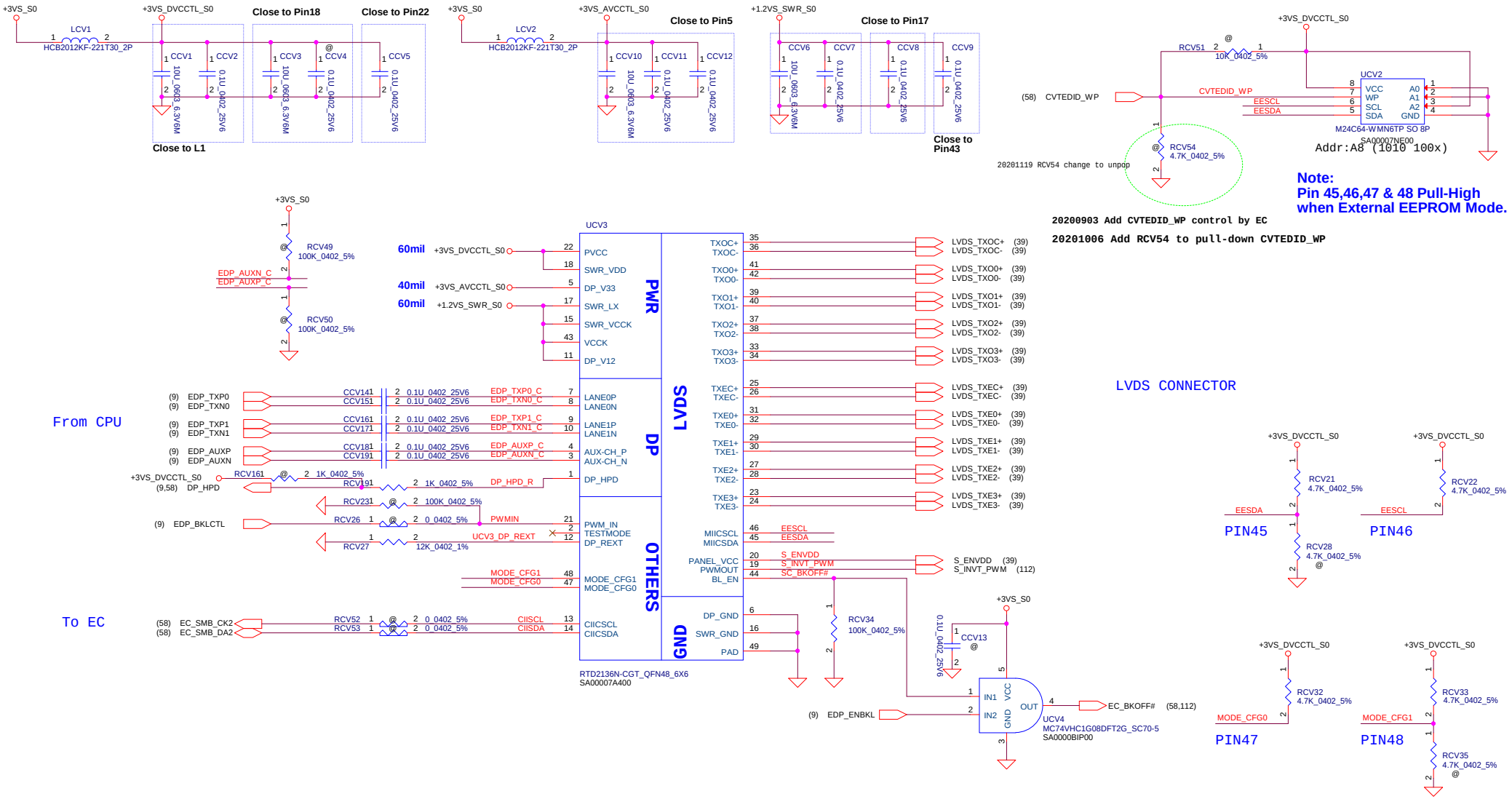
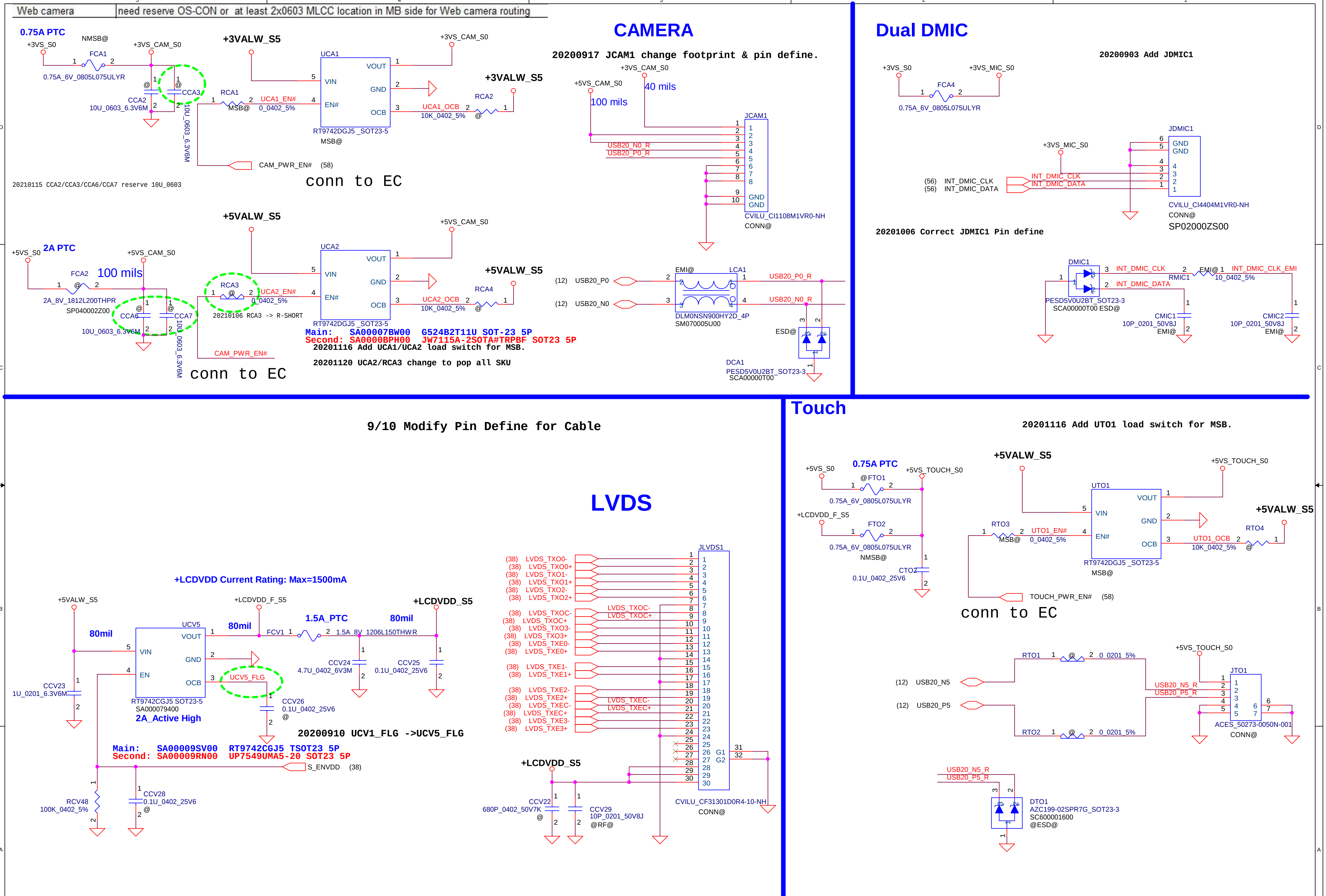
			Date: Monday, January 25, 2021; Sheet 24 of 121



Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.			
Title	LVDS Converter RTD2136N		
Size: Custom	Document Number: LA-K901P		Rev: 0.1
Date: Monday, January 25, 2021	Sheet 38 of 121		


Web camera
need reserve OS-CON or at least 2x0603 MLCC location in MB side for Web camera routing
CAMERA
20200917 JCAM1 change footprint & pin define.
0.75A PTC
+3VS_S0
NMSB@
+3VS_CAM_S0
FCA1
0.75A_6V_0805L075ULYR
CCA2
10U_0603_6.3V6M
CCA3
10U_0603_6.3V6M
+3VALW_S5
UCA1
RCA1
MSB@
UCA1_EN#
0_0402_5%
VIN
EN#
VOUT
GND
OCB
UCA1_OCB
10K_0402_5%
RCA2
RT9742DGJ5 _SOT23-5
MSB@
CAM_PWR_EN# (58)
conn to EC
20210115 CCA2/CCA3/CCA6/CCA7 reserve 10U_0603
+5VS_CAM_S0
100 mils
40 mils
JCAM1
USB20_N0_R
USB20_P0_R
CVILU_CI1108M1VR0-NH
CONN@
+5VALW_S5
UCA2
+5VS_S0
2A PTC
FCA2
100 mils
2A_8V_1812L200THPR
SP040002Z00
CCA6
CCA7
10U_0603_6.3V6M
RCA3
20210106 RCA3 -> R-SHORT
UCA2_EN#
UCA2_OCB
RCA4
CAM_PWR_EN#
conn to EC
Main: SA00007BW00 G524B2T11U SOT-23 5P
Second: SA0000BPH00 JW7115A-2SOTA#TRPBF SOT23 5P
20201116 Add UCA1/UCA2 load switch for MSB.
20201120 UCA2/RCA3 change to pop all SKU
(12) USB20_P0
(12) USB20_N0
EMI@
LCA1
DLM0NSN900HY2D_4P
SM070005U00
USB20_P0_R
USB20_N0_R
ESD@
DCA1
PESD5V0U2BT_SOT23-3
SCA00000T00
Dual DMIC
20200903 Add JDMIC1
+3VS_S0
+3VS_MIC_S0
FCA4
0.75A_6V_0805L075ULYR
JDMIC1
(56) INT_DMIC_CLK
(56) INT_DMIC_DATA
CVILU_CI4404M1VR0-NH
CONN@
SP02000ZS00
20201006 Correct JDMIC1 Pin define
DMIC1
PESD5V0U2BT_SOT23-3
SCA00000T00 ESD@
INT_DMIC_CLK
INT_DMIC_DATA
RMIC1
EMI@
10_0402_5%
INT_DMIC_CLK_EMI
CMIC1
10P_0201_50V8J
EMI@
CMIC2
10P_0201_50V8J
EMI@
Touch
20201116 Add UTO1 load switch for MSB.
+5VS_S0
0.75A PTC
+5VS_TOUCH_S0
@FTO1
0.75A_6V_0805L075ULYR
+LCDVDD_F_S5
FTO2
0.75A_6V_0805L075ULYR
NMSB@
CTO2
0.1U_0402_25V6
+5VALW_S5
UTO1
RTO3
MSB@
UTO1_EN#
0_0402_5%
UTO1_OCB
10K_0402_5%
RTO4
RT9742DGJ5 _SOT23-5
MSB@
TOUCH_PWR_EN# (58)
conn to EC
RTO1
0_0201_5%
(12) USB20_N5
(12) USB20_P5
RTO2
0_0201_5%
USB20_N5_R
USB20_P5_R
JTO1
ACES_50273-0050N-001
CONN@
DTO1
AZC199-02SPR7G_SOT23-3
SC600001600
@ESD@
9/10 Modify Pin Define for Cable
LVDS
+LCDVDD Current Rating: Max=1500mA
+5VALW_S5
80mil
UCV5
CCV23
1U_0201_6.3V6M
RT9742CGJ5 SOT23-5
SA000079400
2A_Active High
+LCDVDD_F_S5
80mil
FCV1
1.5A_PTC
1.5A_8V_1206L150THWR
80mil
+LCDVDD_S5
CCV24
4.7U_0402_6V3M
CCV25
0.1U_0402_25V6
UCV5_FLG
CCV26
0.1U_0402_25V6
20200910 UCV1_FLG ->UCV5_FLG
Main: SA00009SV00 RT9742CGJ5 TSOT23 5P
Second: SA00009RN00 UP7549UMA5-20 SOT23 5P
S_ENVDD (38)
RCV48
100K_0402_5%
CCV28
0.1U_0402_25V6
(38) LVDS_TXO0-
(38) LVDS_TXO0+
(38) LVDS_TXO1-
(38) LVDS_TXO1+
(38) LVDS_TXO2-
(38) LVDS_TXO2+
LVDS_TXOC-
LVDS_TXOC+
(38) LVDS_TXOC-
(38) LVDS_TXOC+
(38) LVDS_TXO3-
(38) LVDS_TXO3+
(38) LVDS_TXE0-
(38) LVDS_TXE0+
(38) LVDS_TXE1-
(38) LVDS_TXE1+
(38) LVDS_TXE2-
(38) LVDS_TXE2+
(38) LVDS_TXEC-
(38) LVDS_TXEC+
(38) LVDS_TXE3-
(38) LVDS_TXE3+
LVDS_TXEC-
LVDS_TXEC+
JLVDS1
+LCDVDD_S5
CCV22
680P_0402_50V7K
CCV29
10P_0201_50V8J
@RF@
CVILU_CF31301D0R4-10-NH
CONN@

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2019/08/01	Deciphered Date	2018/10/01	Title: LVDS/DMIC/CAM/Touch

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Size	Document Number	Rev
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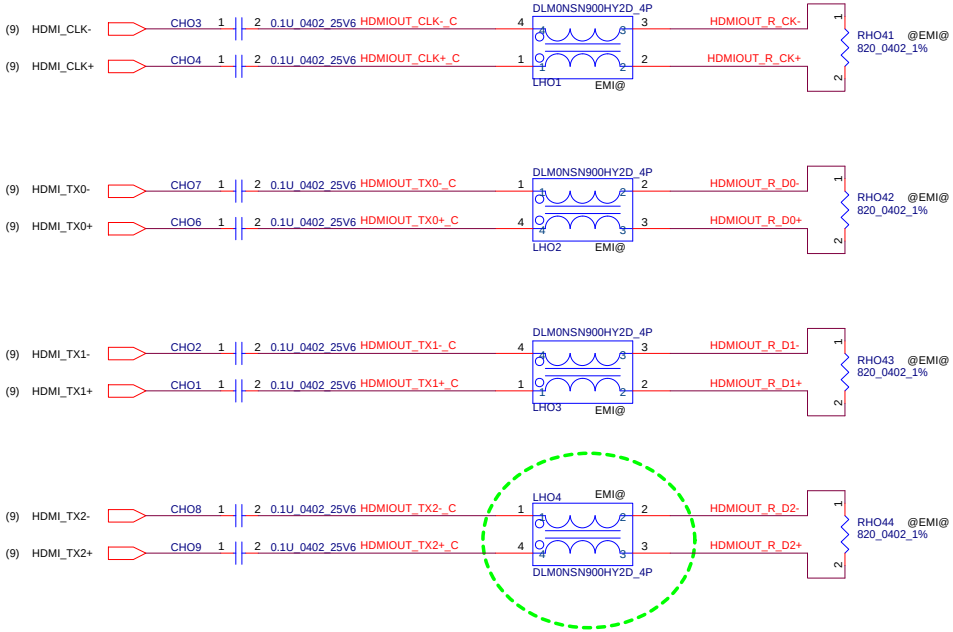
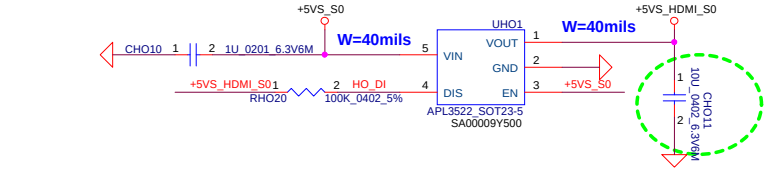
Date: Monday, January 25, 2021 Sheet 39 of 121

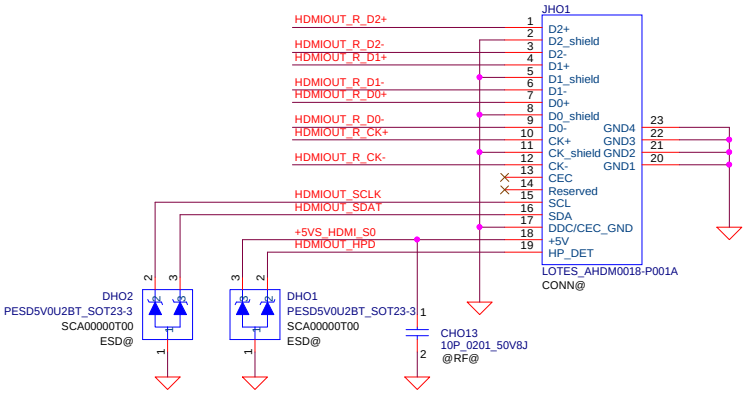


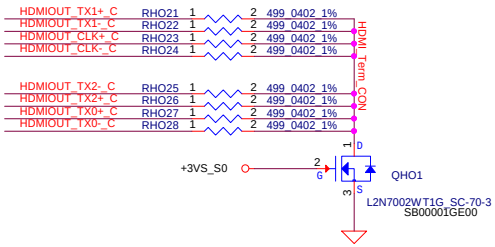
20200922 LHO4 swap pin.



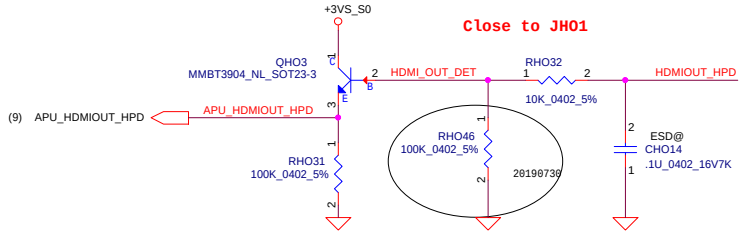
20210114 CHO11 SE000005T80 (10U_0603) --> SE00000UD00 (10U_0402)

HDMI-OUT Connector

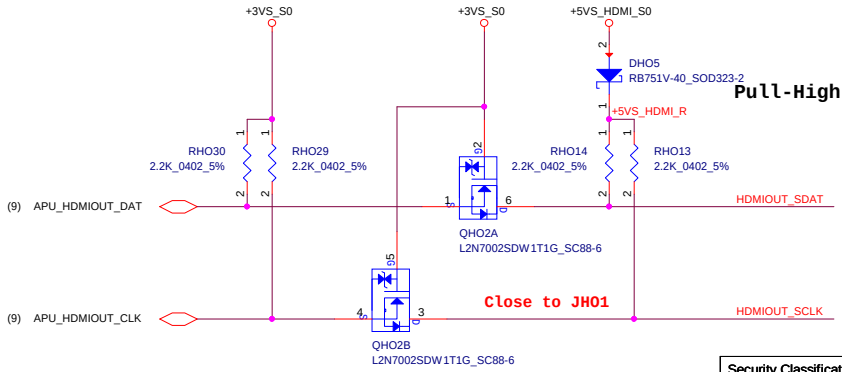




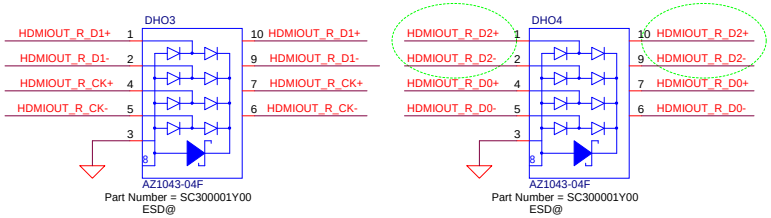
Close to JHO1,<1000mils Length



20200922 DHO4 Pin1/Pin2 , Pin10/Pin9 Swap



Pull-High close JHO1



Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: ***HDMI OUT***

Size	Document Number	Rev
Custom	LA-K901P	0.1

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WOL circuit (Connect +3V_LAN to +3VALW)

20201102 RL29 -> 0603 0 ohm

+3VALW_S5 — 60mil — NMSB@ RL29 0_0603_5% — 60mil — +3.3V_LAN_S5

300mA,120ohm

+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

FOR MSB

+3VALW_S5, +3.3V_LAN_S5, +3VALW_S5

UMS1 RT9742DGJ5_SOT23-5 MSB@ (VOUT, VIN, GND, EN#, OCB)

RMS14 1 2 UMS1_EN# 0_0603_5% @

20210114 RMS14 -> R-SHORT

RL18

UMS1_OCB 2 10K_0402_5% 1 @

LAN_PWR_EN# (58)

conn to EC

Power (Decoupling Cap.)

40 mils — Close to Pin 11,23

+3.3V_LAN_S5

CL1 1 2 .1U_0402_16V7K

CL2 1 2 .1U_0402_16V7K

@EMI@ CL5 1 2 4.7U_0402_6.3V6M

@EMI@ CL8 1 2 4.7U_0402_6.3V6M

CL3 1 2 .1U_0402_16V7K

Close to Pin 32

@EMI@ CL10 1 2 .1U_0402_16V7K

@EMI@ CL11 1 2 .1U_0402_16V7K

@EMI@ CL21 1 2 .1U_0402_16V7K

Close to Pin 32 on TOP side

60 mils — Close to pin 3,8,30,24

+LAN_VDDREG

CL4 1 2 .1U_0402_16V7K

CL6 1 2 .1U_0402_16V7K

CL7 1 2 .1U_0402_16V7K

CL9 1 2 .1U_0402_16V7K

LED Status

WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on

blinking

8111G resistor/8111H capacitor

CRL1 8111G_EMI@ RTL8111G-CG_0ohm resistor

CRL5 8111G_EMI@ RTL8111G-CG_0ohm resistor

CRL2 8111G_EMI@ RTL8111G-CG_0ohm resistor

CRL6 8111G_EMI@ RTL8111G-CG_0ohm resistor

CRL3 8111G_EMI@ RTL8111G-CG_0ohm resistor

CRL7 8111G_EMI@ RTL8111G-CG_0ohm resistor

CRL4 8111G_EMI@ RTL8111G-CG_0ohm resistor

CRL8 8111G_EMI@ RTL8111G-CG_0ohm resistor

20200914 CRL1~CRL8 BOM Structure
0.1U --> 8111H_EMI@
0 ohm --> 8111G_EMI@

CAP close to UL1

Close to pin 22

+3.3V_LAN_S5, +LAN_VDDREG, +LAN_VDDREG

CL12 1 2 1U_0201_6.3V6M

CL20 1 2 .1U_0402_16V7K

UL1 RTL8111H-CG_QFN32_4X4 8111H@

HSOP HSON HSIP HSIN REFCLK_P REFCLK_N CLKREQB LANWAKEB ISOLATEB PERSTB VDDREG RSET CKXTAL2 CKXTAL1 MDIP0 MDIN0 MDIP1 MDIN1 MDIP2 MDIN2 MDIP3 MDIN3 LED2 LED1/GPIO LED0 REGOUT GND

EMC

CRL1 CRL2 CRL3 CRL4 CRL5 CRL6 CRL7 CRL8 8111H_EMI@ 0.1U_0402_25V6

LAN_MIDI0+ LAN_MIDI0- LAN_MIDI1+ LAN_MIDI1- LAN_MIDI2+ LAN_MIDI2- LAN_MIDI3+ LAN_MIDI3-

(6) PCIE_ARX_LANTX_P2 (6) PCIE_ARX_LANTX_N2 CL13 CL14 .1U_0402_16V7K

(6) PCIE_ATX_C_LANRX_P2 (6) PCIE_ATX_C_LANRX_N2

(11) CLK_PCIE_LAN (11) CLK_PCIE_LAN# RL32 RL1 NMSB@ 10K_0402_5%

CLKREQ_LAN#_R

+3VALW_S5 +3.3V_LAN_S5 MSB@

+3VS_S0 RL3 1K_0402_5%

(10,52,58) PCIE_WAKE#

ISOLATE# PCIE_RST#_LAN

RL6 15K_0402_5%

+3.3V_LAN_S5 RL5 2.49K_0402_1%

UL1_RSET_P31 LAN_X2 LAN_X1

LAN_LED_ORG# LAN_PHY_DIS# LAN_LED_YEL#

TP@ TL1 TP@ TL2 TP@ TL3

LAN_PHY_DIS# (58)

+LAN_VDDREG

+3.3V_LAN_S5 RL13 @ 10K_0402_5%

LAN_PHY_DIS#

20200914 JRJ1 footprint --> TUTON_PJ1CW51104I2_14P-T

Footprint:TUTON_PJ1CW51104I2_14P-T

JRJ1 CONN@ SP011312232

TD1+ R1 TD1- R2 TD2+ R3 TD2- R4 CT R5 CT R6 TD3+ R7 TD3- R8 TD4+ R9 TD4- R10 L1 L2 GND GND

LAN_MIDI0+_C LAN_MIDI0-_C LAN_MIDI1+_C LAN_MIDI1-_C JRJ1_CT_RSR6 LAN_MIDI2+_C LAN_MIDI2-_C LAN_MIDI3+_C LAN_MIDI3-_C

RL4 0_0402_5% CL17 .1U_0402_16V7K EMI@

RL7 510_0402_5% LAN_LED_YEL#_R

Yellow 20mils

+3.3V_LAN_S5

LAN_LED_YEL#

DL3 PESD5V0U2BT_SOT23-3 SCA00000T00 ESD@

RL11 RL12 @ 0_0805_5%

LAN_GND

+3.3V_LAN_S5 USD3 SA0000BIP00 MC74VHC1G08DFT2G_SC70-5 MSB@

(10,52,66,68) APU_PCIE_RST#

(58) PLT_RST#_LAN

@ESD@ CL22 .1U_0402_16V7K

RL33 1 2 0_0402_5% NMSB@

DL1 DL2 ESD@ SC300001G00 AZC199-04S.R7G SOT23-6

LAN_MIDI0+_C LAN_MIDI0-_C LAN_MIDI1+_C LAN_MIDI1-_C

LAN_MIDI2+_C LAN_MIDI2-_C LAN_MIDI3+_C LAN_MIDI3-_C

DL1_PWR DL2_PWR RL16 RL17 @ 0_0402_5% +3.3V_LAN_S5

+3VS_S0 +3.3V_LAN_S5

PCH Side pull high at page 14

RL8 10K_0402_5%

20200907 LAN_CLKREQ#_R rename to CLKREQ_LAN#_R

(11) CLKREQ_LAN# QL1 L2N7002WT1G_SC-70-3 SB00001GE00

CLKREQ_LAN#_R

8111G/8111H LAN chip

UL1 8111G@ RTL8111G-CG

LAN_X1 RL10 1M_0402_5% LAN_X2

YL1 XTAL0 XTAL1 NC NC 25MHZ_10PF_7V25000014

CL18 CL19 10P_0201_50V8J

Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

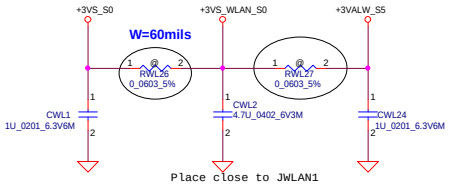
Title: LAN RTL8111G

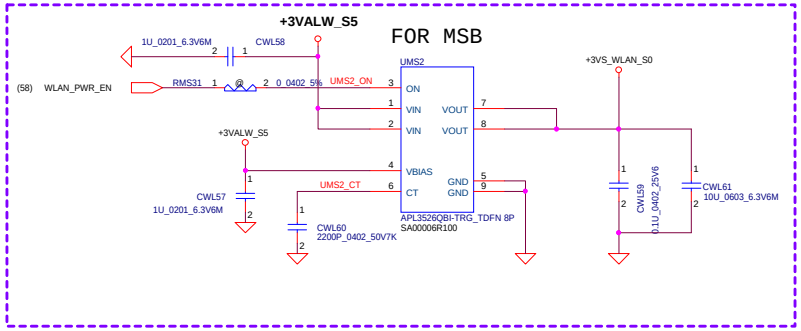
Size: Custom | Document Number: LA-K901P | Rev: 0.1

Date: Monday, January 25, 2021 | Sheet 51 of 121

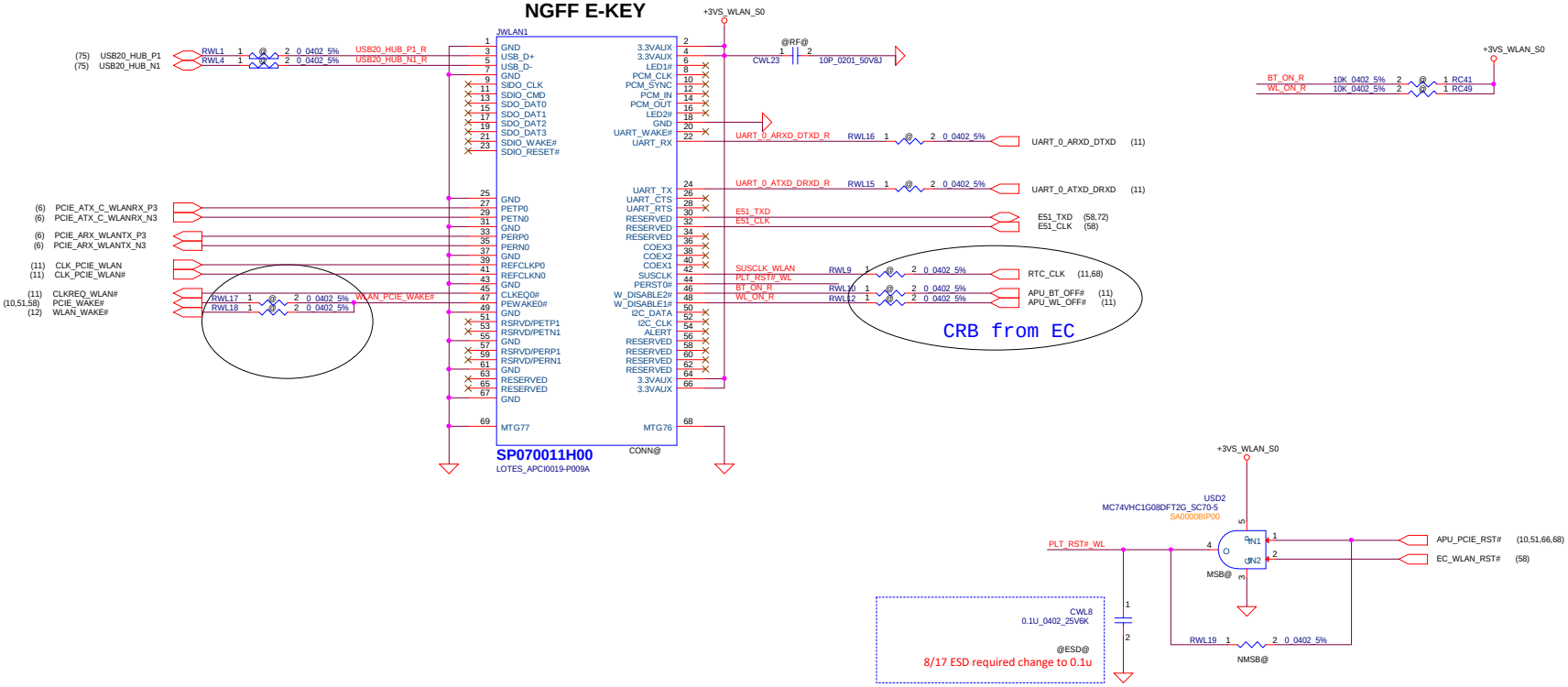
WLAN (WIFI/BT Combo)

20201102 RWL26/RWL27 -> 0603 0 ohm



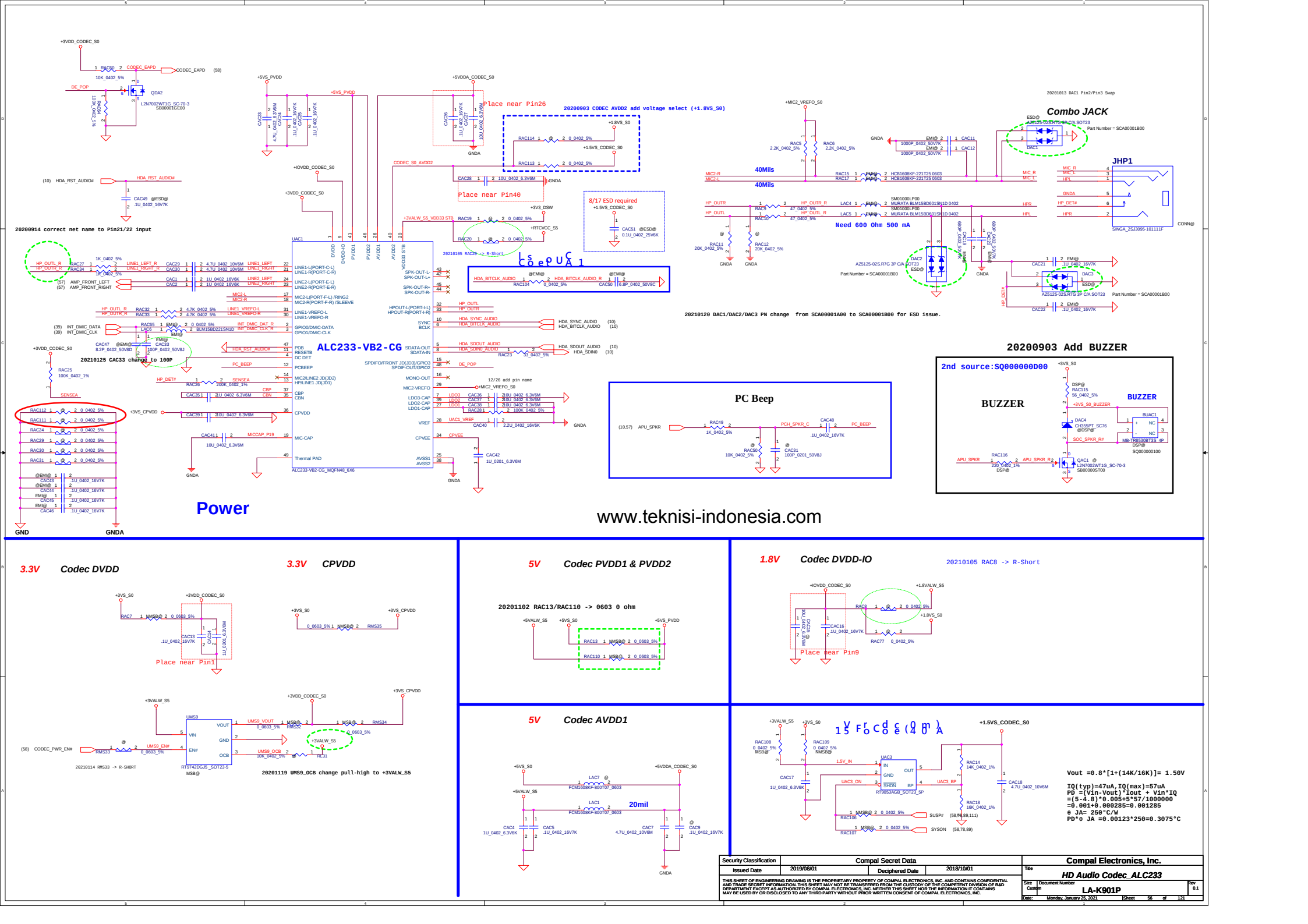


WLAN Conn.



Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.			
Title	WLAN (NGFF)		
Size C	Document Number LA-K901P		Rev 0.1
Date: Monday, January 25, 2021	Sheet 52 of 121		


Power
ALC233-VB2-CG
Combo JACK
JHP1
PC Beep
BUZZER
20200903 Add BUZZER
2nd source:SQ000000D00
20200914 correct net name to Pin21/22 input
20210125 CAC33 change to 100P
20200903 CODEC AVDD2 add voltage select (+1.8VS_S0)
Place near Pin26
Place near Pin40
8/17 ESD required
20210105 RAC26 -> R-Short
20210120 DAC1/DAC2/DAC3 PN change from SCA00001A00 to SCA00001B00 for ESD issue.
20201013 DAC1 Pin2/Pin3 Swap
Need 600 Ohm 500 mA
40Mils
12/26 add pin name
www.teknisi-indonesia.com
3.3V Codec DVDD
3.3V CPVDD
5V Codec PVDD1 & PVDD2
1.8V Codec DVDD-IO
20201102 RAC13/RAC110 -> 0603 0 ohm
20210105 RAC8 -> R-Short
Place near Pin1
5V Codec AVDD1
20mil
Place near Pin9
20210114 RMS33 -> R-SHORT
20201119 UMS9_OCB change pull-high to +3VALW_S5
Vout =0.8*[1+(14K/16K)]= 1.50V
IQ(typ)=47uA,IQ(max)=57uA
PD =(Vin-Vout)*Iout + Vin*IQ
=(5-4.8)*0.005+5*57/1000000
=0.001+0.000285=0.001285
θ JA= 250°C/W
PD*θ JA =0.00123*250=0.3075°C
Security Classification
Compal Secret Data
Issued Date
2019/08/01
Deciphered Date
2018/10/01
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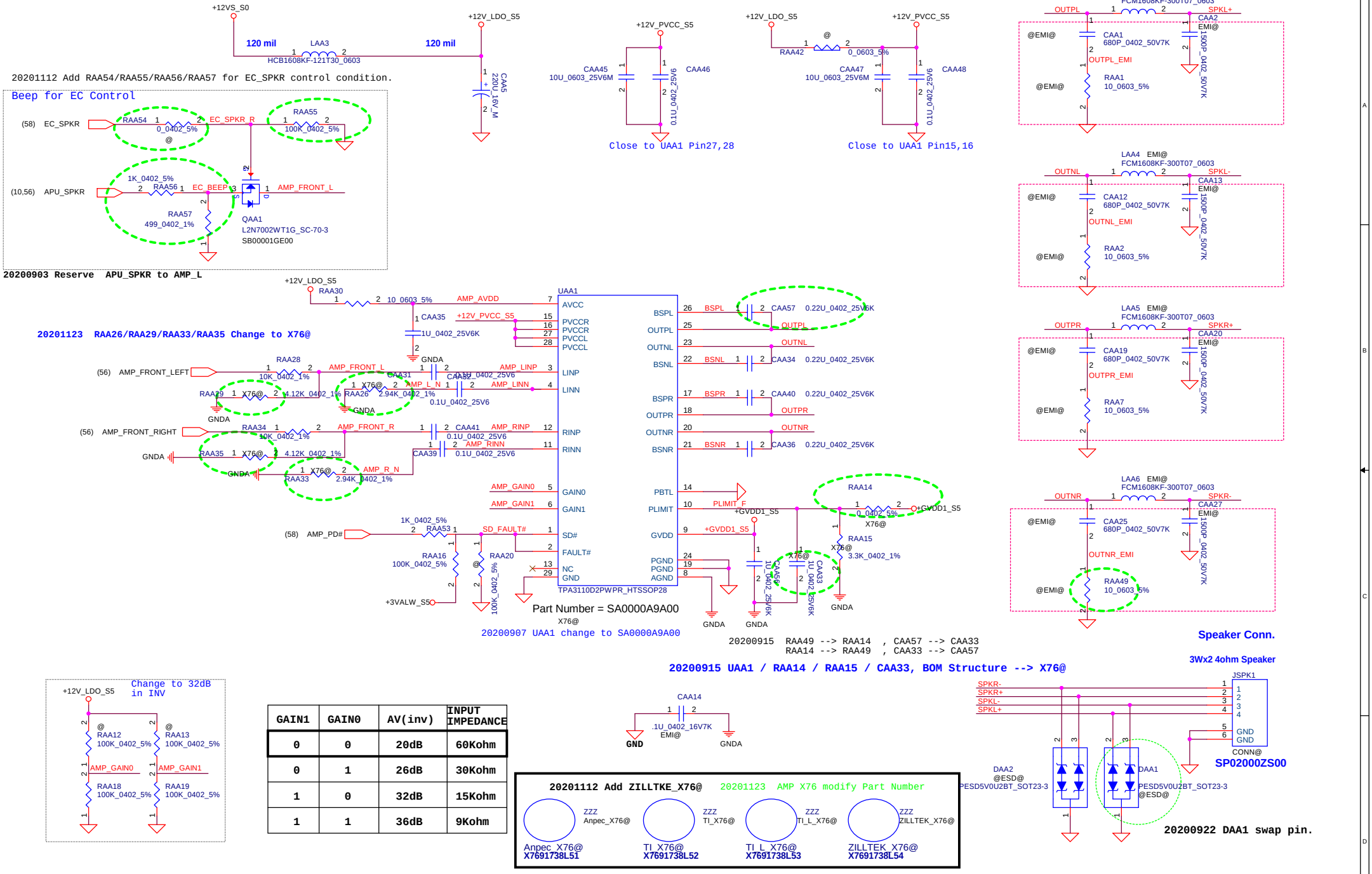
Compal Electronics, Inc.
HD Audio Codec_ALC233
Size Custom
Document Number LA-K901P
Rev 0.1
Date: Monday, January 25, 2021
Sheet 56 of 121



GAIN1	GAIN0	AV(inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/12/15

Compal Electronics, Inc.

Title: Amp TPA3110

Size: Custom | Document Number: LA-K901P | Rev: 0.1

Date: Monday, January 25, 2021 | Sheet 57 of 121

20210106 REC319 -> R-SHORT

Place closely UEC1

reserve pin 25 pull-up & pin 17 pull-down to prevent EC test mode

SKTOCC# need pull-down

20201203 REC330 change to POP

VHIF Power is the same with eSPI interface

20201203 Correct EC_USB_D+/D- Pin

AD Voltage Range: 0 to 2.048 V

V1.0 update

20201119 complement RC circuit for EC_USBDP/DN

Rb value
EVT(v0.1) : 30K Ohm : 0.76V
DVT(v0.2) : 56K Ohm : 1.18V
PVT(v0.3) : 150K Ohm : 1.98V
MP(v1.0) : 100K Ohm : 1.67V

Add 100K pull-down on Pin100 to avoid RTC battery current loss

20201117 Add EC_ODD_DA# on Pin50

20201203 REC341 change to POP

20201117 Add EC_ODD_PLUGIN# on Pin86

20201125 ESD reserve CAPs CEC42/CEC43

20201125 DFB request QEC1 change footprint to L2N7002WT1G_SC70-3

20201119 AGPIO94 initial tri-state need add pull-down

20201113 Correct UEC1 Symbol -> NCT6686D-L

Part Number = SA0000DY000

20201113 ESPI_EN -> pull-down.

2Mb SPI ROM

SA00003GM30

EC DEBUG port

Reserve REC34 for EC debug.

AC in-->One touch -->Power button--> Clear CMOS
Always short-->AC in-->Power button--> Crisis

POWER ON SETTING PIN

PIN	Name	0	1	Strapping Power
31	2E_4E_SEL	IO Address: 2E/2F	IO Address: 4E/4F	VCC
27	eSPI_EN	Disable eSPI Interface	Enable eSPI Interface	VSB
32	DIS_HWACPI_EN	Hardware ACPI could take over related signals	Hardware ACPI never take over related signals	VSB
15	DDR4_EN	Disable DDR4 Function	Enable DDR4 Function	VSB
96	AMD_EN	Disable AMD Mode	Enable AMD Mode	VSB
92	DSW_EN	Disable DSW Function	Enable DSW Function	VSB

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2014/04/01

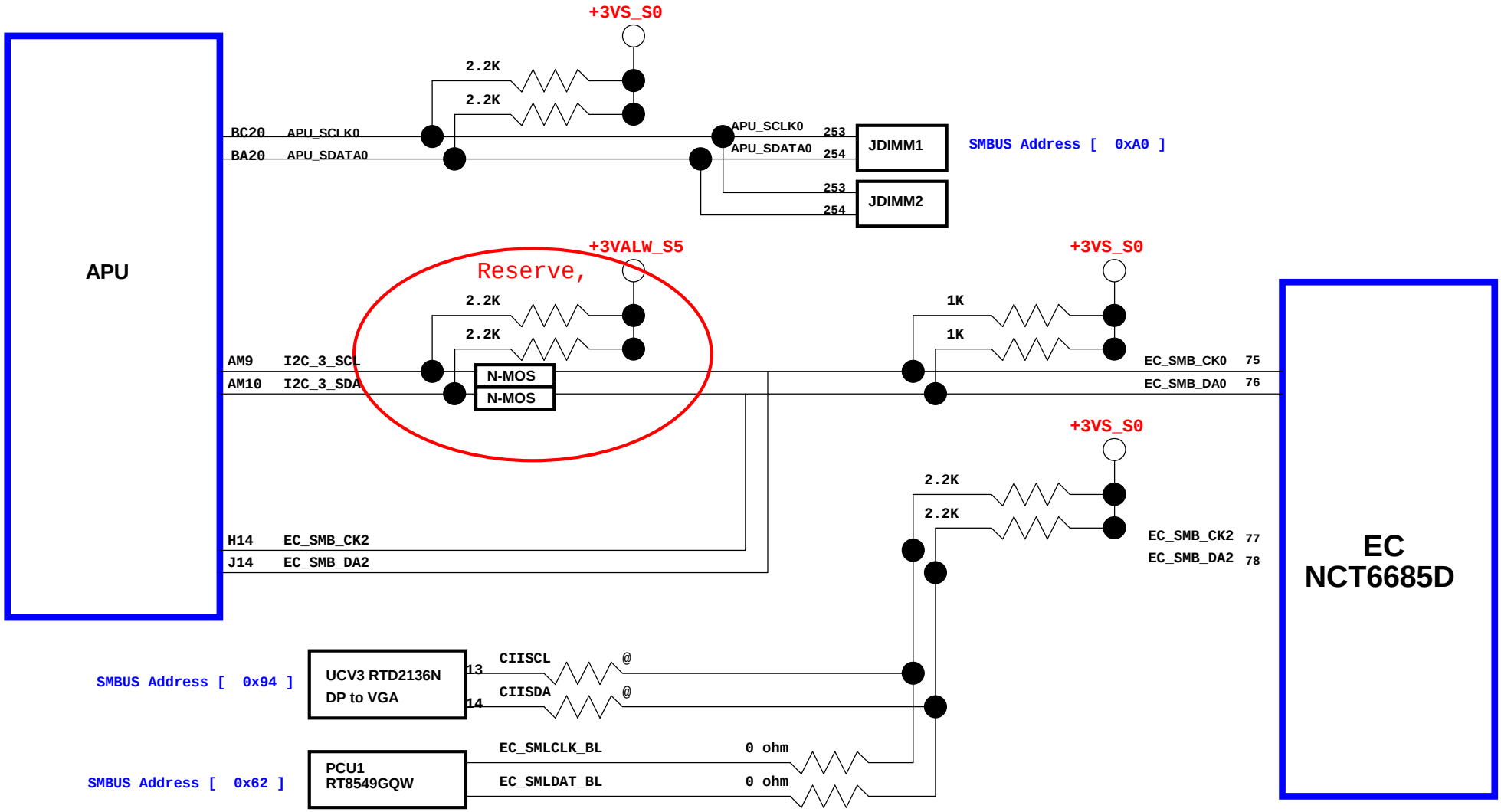
Compal Electronics, Inc.

Title: EC NCT6686D

Size: Custom | Document Number: LA-K531P | Rev: 0.1

Date: Tuesday, January 26, 2021 | Sheet 58 of 121

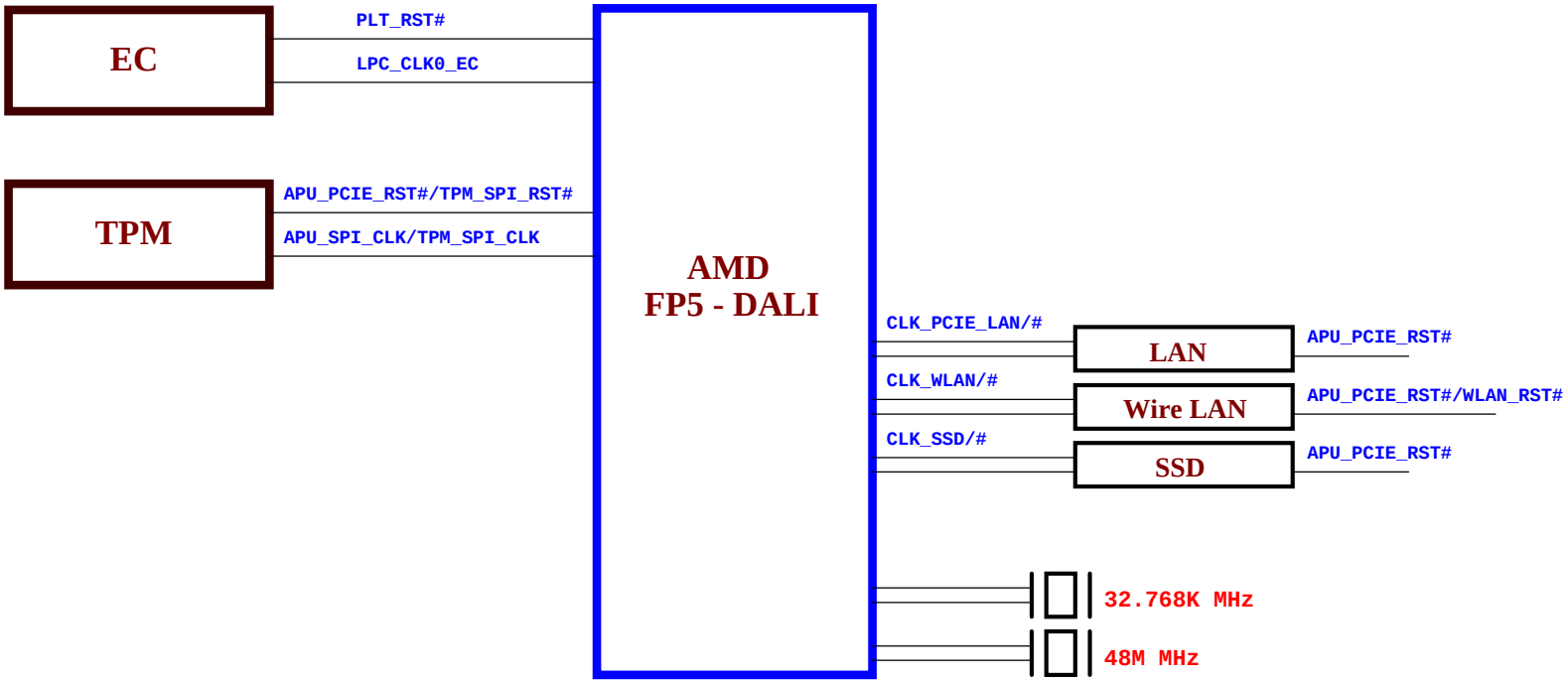
SMBus Block Diagram



Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.			
Title: SMB Block Diagrams			
Size: B	Document Number: LA-K901P		Rev: 0.1
Date: Monday, January 25, 2021	Sheet 61 of 121		

System clock and Reset map



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/08/01	Deciphered Date 2018/10/01	Title: RESERVE
			Size: B; Document Number: LA-K901P; Rev: 0.1
			Date: Monday, January 25, 2021; Sheet 62 of 121

Ball	Signal Name	Default Function	Pin Type	PWR Domain	Power up			FOC51 (LA-J881FP01)		
					Default State	Pull-Up State	Pull-Down State	HW Pin Requirement	Internal PU/PD Requirement	Functional Description
AR15	PWR_BTN_L/AGPIO0	PWR_BTN_L	I-IO3V5-S	3S	Input	Enable	Disable	PBTN_OUT#	External Pull-up 10Kohm to +3VALW_3S	Power button
AP10	SYS_RESET_L/AGPIO1	SYS_RESET_L	I-IO3V5-S	3S	Input	Enable	Disable	SYS_RESET#	External Pull-up 10Kohm to +3VALW_3S, Reserve Pull-down	Used as Strapping (PU : Normal reset mode
AV11	WAKE_L/AGPIO2	WAKE_L	I-IO3V5-S	3S	Input	Enable	Disable	PCIE_WAKE#	Reserve Pull-up 10Kohm to +3.3V_LAN_3S .	PCIE Wake Event
AT15	AGPIO3	AGPIO3		3S	Input	Enable	Disable			
AW20	AGPIO4/SATAE_IFDET	AGPIO4	B-IO3V5-OD	3S	Input	Disable	Enable			
AP8	AGPIO5/DEVSLP0	AGPIO5	B-IO3V5-OD	3S	Input	Disable	Enable	HDD_DEVSLP		For HDD DEEP SLEEP function
AU10	AGPIO6/DEVSLP1	AGPIO6	B-IO3V5-OD	3S	Input	Disable	Enable	SSD1_PWR_EN#	Reserve Pull-up 2.2Kohm to +3VALW_3S	To enable SSD power
AR8	AGPIO7/PCH_ACF_I2S_SDI 0_EC	AGPIO7	B-AUD-S	3S	Input	Disable	Enable			
AP8	AGPIO8/PCH_ACF_I2S_LRC LK_EC	AGPIO8	B-AUD-S	3S	Input	Disable	Enable			
AU7	AGPIO9	AGPIO9		3S	Input	Disable	Enable			
AR8	SOA3_GPIO/AGPIO10	AGPIO10	B-IO3V5-S	3S	Input	Enable	Disable	SOA3_GPIO	External Pull-up 8.2Kohm to +3VALW_3S	Control Modern standby
AV9	BLINK/AGPIO11	AGPIO11	B-IO3V5-S	3S	Input	Enable	Disable			
AN8	LLB_L/AGPIO12	AGPIO12	B-IO3V5-S	3S	Ouput	Disable	Disable	KDBG_MUX_SEL	External Pull-up 10Kohm to +3VALW_3S	Control MUX for debub
AT15	AGPIO13/USB_OC6_L	USB_OC6_L	I-IO3V5-S	3S	Input	Enable	Disable		Internal Pull-down required by SW	
AW7	AGPIO14/USB_OC4_L	USB_OC4_L	I-IO3V5-S	3S	Input	Enable	Disable	WLAN_WAKE#	External Pull-up 8.2Kohm to +3VALW_3S	WLAN Wake
AR10	USB_OC5_L/AGPIO15	USB_OC5_L	I-IO3V5-S	3S	Input	Enable	Disable	USB_OC5#	External Pull-up 10Kohm to +3VALW_3S	USB Over Current
AR9	USB_OC1_L/AGPIO17	USB_OC1_L	I-IO3V5-S	3S	Input	Enable	Disable			
AL9	USB_OC2_L/AGPIO18	USB_OC2_L	I-IO3V5-S	3S	Input	Enable	Disable	USB_OC2#	External Pull-up 10Kohm to +3VALW_3S	USB Over Current
AM8	I2C3_SCL/AGPIO19/SCL1	SCL1	B-DUAL_3S-OD	3S	Input	Disable	Disable	I2C_3_SCL	External Pull-up 2.2Kohm to +3VALW_3S	I2C to EC
AM10	I2C3_SDA/AGPIO20/SDA1	SDA1	B-DUAL_3S-OD	3S	Input	Disable	Disable	I2C_3_SDA	External Pull-up 2.2Kohm to +3VALW_3S	I2C to EC
BE14	LPC_FD_L/SD_CMD/AGPIO2 1	LPC_FD_L	B-DUAL_3S-OD	3S	Ouput	Disable	Disable	LPCFD#	Internal Pull-down required by SW	Test PAD
BA15	LPC_FME_L/SD_PWR_CTRL/ AGPIO22	LPC_FME_L	O-IO3V5-S	3S	Input	Enable	Disable	EC_SCI#	External Pull-up 10 Kohm to +3VALW_3S	EC SCI event
AT10	AC_PRES/AGPIO23	AC_PRES	I-IO3V5-S	3S	Input	Enable	Disable			
AL8	USB_OC3_L/AGPIO24	USB_OC3_L	I-IO3V5-S	3S	Input	Enable	Disable	USB_OC3#	External Pull-up 10Kohm to +3VALW_3S	USB Over Current
BD5	SPI_TPM_CS_L/AGPIO26	SPI_TPM_CS_L	O-IO1V8-S	3S	Input	Disable	Disable	APU_SPI_TPMCS#	External Pull-up 10Kohm to +3VS_3S	CS of SPI for TPM
BA8	SPI_CS2_L/ESPI_CS_L/AGPI O30	SPI_CS2_L	O-IO1V8-OD	3S	Input	Enable	Disable	APU_SPI_CS2#	Internal Pull-down required by SW	CS of SPI for TPM(Reserve)
BA6	SPI_CS3_L/AGPIO31	SPI_CS3_L	O-IO1V8-OD	3S	Input	Enable	Disable			
BD11	LPC_RST_L/SD_WP_L/AGPI O32	LPC_RST_L	O-IO3V5-S	3S	Output	Disable	Disable	PLT_RST#		LPC reset
AU15	AGPIO33/SPI_3S_AGPIO33	AGPIO33	I-IO3V5-S	3S	Input	Enable	Disable			
AU6	AGPIO40	AGPIO40		3S	Input	Disable	Disable	AUX_RESET#	External Pull-down 10Kohm	PCIE Reset for SSD at M3
BA11	AGPIO68/SD_CD	AGPIO68	I-IO3V5-S	3S	Input	Disable	Enable	SSD_FEDET		Reserve
AV18	AGPIO69	AGPIO69		3D	Input	Disable	Enable			
BE8	SPI_ROM_GNT/AGPIO76	SPI_ROM_GNT	O-IO1V8-S	3S	Input	Disable	Enable			
AR18	PAMIN0/AGPIO84	PAMIN0	B-IO3V5-S	3D	Input	Enable	Disable	MIC_SELECT	External Pull-down 10Kohm and Pu down 10k ,depend on M	MIC strap pin
AT18	PAMOUT0/AGPIO85	AGPIO85	B-IO3V5-S	3D	Input	Enable	Disable	TPM_STSIRQ#	External Pull-up 4.7Kohm to +1.8VS_TPM_3D	TPM interrupt
AT16	AGPIO86	AGPIO86		3D	Input	Enable	Disable			
BC12	SERIRQ/AGPIO87	SERIRQ	B-IO3V5-S	3D	Input	Enable	Disable	SERIRQ		Serial IRQ
BC13	LPC_CLKRUN_L/AGPIO88	LPC_CLKRUN_L	B-IO3V5-OD	3D	Ouput	Enable	Disable	PM_CLKRUN#		
AT16	GEMINT1_L/AGPIO89	GEMINT1_L	B-IO3V5-S	3D	Input	Enable	Disable			
BD15	GEMINT2_L/AGPIO90	GEMINT2_L	B-IO3V5-S	3D	Input	Enable	Disable			
AU18	SPKR/AGPIO91	SPKR	O-IO3V5-S	3D	Input	Disable	Enable	APU_SPKR		PC Beep
AV18	CLK_REQ0_L/SATA_IS0_L/S ATA_ZP0_L/AGPIO92	CLK_REQ0_L	B-IO3V5-S	3D	Input	Enable	Disable			
AN19	CLK_REQ1_L/AGPIO115	CLK_REQ1_L	B-IO3V5-S	3D	Input	Enable	Disable	CLKREQ_SSD#	External Pull-up 10Kohm to +3VS_3D	SSD clock request
AP16	CLK_REQ2_L/AGPIO116	CLK_REQ2_L	B-IO3V5-S	3D	Input	Enable	Disable	CLKREQ_LAN#	External Pull-up 10Kohm to +3VS_3D	LAN clock request
BE11	ESPI_RESET_L/KBRST_L/AG PIO129	KBRST_L	B-DUAL-S	3D	Input	Enable	Disable	KB_RST#	Reserve Pull-up 10Kohm to +3VS_3D	KeyBoard reset
AV15	SATA_ACT_L/AGPIO130	SATA_ACT_L	B-IO3V5-OD	3D	Input	Enable	Disable			
BD18	UART0_INTR/AGPIO139	UART0_INTR	B-IO1V8-S	3D	Input	Disable	Enable			
BE18	AGPIO144/UART1_INTR	UART1_INTR	B-IO3V5-S	3D	Input	Disable	Enable	APU_WL_OFF#	Reserve Pull-up 10Kohm to +3VS_WLAN_3D	WLAN Enable
BD5	PCIE_RST0_L/EGPIO26	PCIE_RST0_L	O-IO3V5-S	3S	Output	Disable	Disable	APU_PCIE0_RST#	External Pull-down 10Kohm	APU PCIE reset
BE6	PCIE_RST1_L/EGPIO27	EGPIO27	O-IO3V5-S	3S	Input	Disable	Enable	APU_PCIE1_RST#	Internal Pull-High required by SW	APU PCIE reset (Reserved)
AW12	EGPIO41/SPI_3S_EGPIO41	EGPIO41	I-IO3V5-S	3S	Input	Enable	Disable			
AV8	EGPIO42	EGPIO42		3S	Input	Enable	Disable			
BC8	SPI_ROM_REQ/EGPIO67	SPI_ROM_REQ	I-IO1V8-S	3S	Input	Disable	Enable			
BD18	EGPIO70/SD_CLK	EGPIO70	O-DUAL-S	3D	Input	Disable	Enable			
BA16	LPCCLK0/EGPIO74	LPCCLK0	I-IO3V5-S	3D	Ouput	Disable	Disable	LPC_CLK0		LPC clock for EC
BB13	LPCCLK1/EGPIO75	LPCCLK1	I-IO3V5-S	3D	Ouput	Disable	Disable		Internal Pull-down required by SW	

Ball	Signal Name	Default Function	Pin Type	PWR Domain	Power up			FOC51 (LA-J881FP01)		
					Default State	Pull-Up State	Pull-Down State	HW Pin Requirement	Internal PU/PD Requirement	Functional Description
BB12	LAD0/SD_DATA0/EGPIO104	LAD0	B-DUAL-S	3D	Input	Enable	Disable	LPC_AD0_R		LPC I/F
BC11	LAD1/SD_DATA1/EGPIO105	LAD1	B-DUAL-S	3D	Input	Enable	Disable	LPC_AD1_R		LPC I/F
BB10	LAD2/SD_DATA2/EGPIO106	LAD2	B-DUAL-S	3D	Input	Enable	Disable	LPC_AD2_R		LPC I/F
BC10	LAD3/SD_DATA3/EGPIO107	LAD3	B-DUAL-S	3D	Input	Enable	Disable	LPC_AD3_R		LPC I/F
BC6	ESPI_ALERT_L/LDRQ0_L/EG PIO108	LDRQ0_L	I-DUAL-S	3D	Input	Disable	Enable	ESPI_ALERT#	External Pull-up 10Kohm to +3VS	
BA17	LFRAME_L/EGPIO109	LFRAME_L	O-IO3V5-S	3D	Ouput	Disable	Disable	LPC_FRAME#		LPC I/F
BC20	I2C2_SCL/EGPIO113/SCL0	SCL0	B-DUAL-OD	3D	Input	Disable	Disable	I2C_2_SCL_R	External Pull-up 2.2Kohm to +3VS	SM Bus to SO-DIMM
BA20	I2C2_SDA/EGPIO114/SDA0	SDA0	B-DUAL-OD	3D	Input	Disable	Disable	I2C_2_SDA_R	External Pull-up 2.2Kohm to +3VS	SM Bus to SO-DIMM
BC8	SPI_CS1_L/EGPIO118	SPI_CS1_L	O-IO1V8S-OD	3S	Input	Enable	Disable	APU_SPI_CS1#	External Pull-up 10Kohm to +1.8VALW	SPI I/F
AW15	CLK_REQ5_L/EGPIO120	CLK_REQ5_L	B-IO3V5-S	3D	Input	Disable	Disable		Internal Pull-down required by SW	
AW19	CLK_REQ6_L/EGPIO121	CLK_REQ6_L	B-IO3V5-S	3D	Input	Disable	Enable	APU_BT_OFF#		BlueTooth Enable
AT19	CLK_REQ3_L/SATA_IS1_L/S ATA_ZP1_L/EGPIO131	CLK_REQ3_L	B-IO3V5-S	3D	Input	Enable	Disable	CLKREQ_WLAN#	External Pull-up 10Kohm to +3VS	WLAN clock request
AU19	CLK_REQ4_L/OSCIN/EGPIO 132	CLK_REQ4_L	B-IO3V5-S	3D	Input	Enable	Disable			
BA18	UART0_CTS_L/UART2_TXD /EGPIO155	UART0_CTS_L	I-IO1V8-S	3D	Input	Disable	Enable	T19		Test PAD
BA14	UART0_RXD/EGPIO156	UART0_RXD	I-IO1V8-S	3D	Input	Disable	Enable	UART_0_ARXD_DTXD		UART to NGFF WLAN
BC17	UART0_RTS_L/UART2_RXD/ EGPIO157	UART0_RTS_L	O-IO1V8-S	3D	Input	Enable	Disable	T18		Test PAD
BB18	UART0_TXD/EGPIO158	UART0_TXD	O-IO1V8-S	3D	Input	Enable	Disable	UART_0_ATXD_DRXD		UART to NGFF WLAN
BB16	EGPIO140/UART1_CTS_L/U ART3_TXD	UART1_CTS_L	I-IO3V5-S	3D	Input	Disable	Enable			
BC15	EGPIO141/UART1_RXD	UART1_RXD	I-IO3V5-S	3D	Input	Disable	Enable			
BC16	EGPIO142/UART1_RTS_L/U ART3_RXD	UART1_RTS_L	O-IO3V5-S	3D	Input	Enable	Disable	SSD_RST#		
BA17	EGPIO143/UART1_TXD	UART1_TXD	O-IO3V5-S	3D	Input	Enable	Disable			
AN8	I2C1_SCL/SPI1_I2C_SCL	EGPIO148	B-DUAL-OD	3S	Input	Disable	Disable	T25	Internal Pull-down required by SW	
AN9	I2C1_SDA/SPI1_I2C_SDA	EGPIO150	B-DUAL-OD	3S	Input	Disable	Disable	T24	Internal Pull-down required by SW	
AR15	I2C0_SCL/SPI0_I2C_SCL	EGPIO151	B-DUAL_3S-OD	3S	Input	Disable	Disable	T22	Internal Pull-down required by SW	
AT16	I2C0_SDA/SPI0_I2C_SDA	EGPIO152	B-DUAL_3S-OD	3S	Input	Disable	Disable	T21	Internal Pull-down required by SW	

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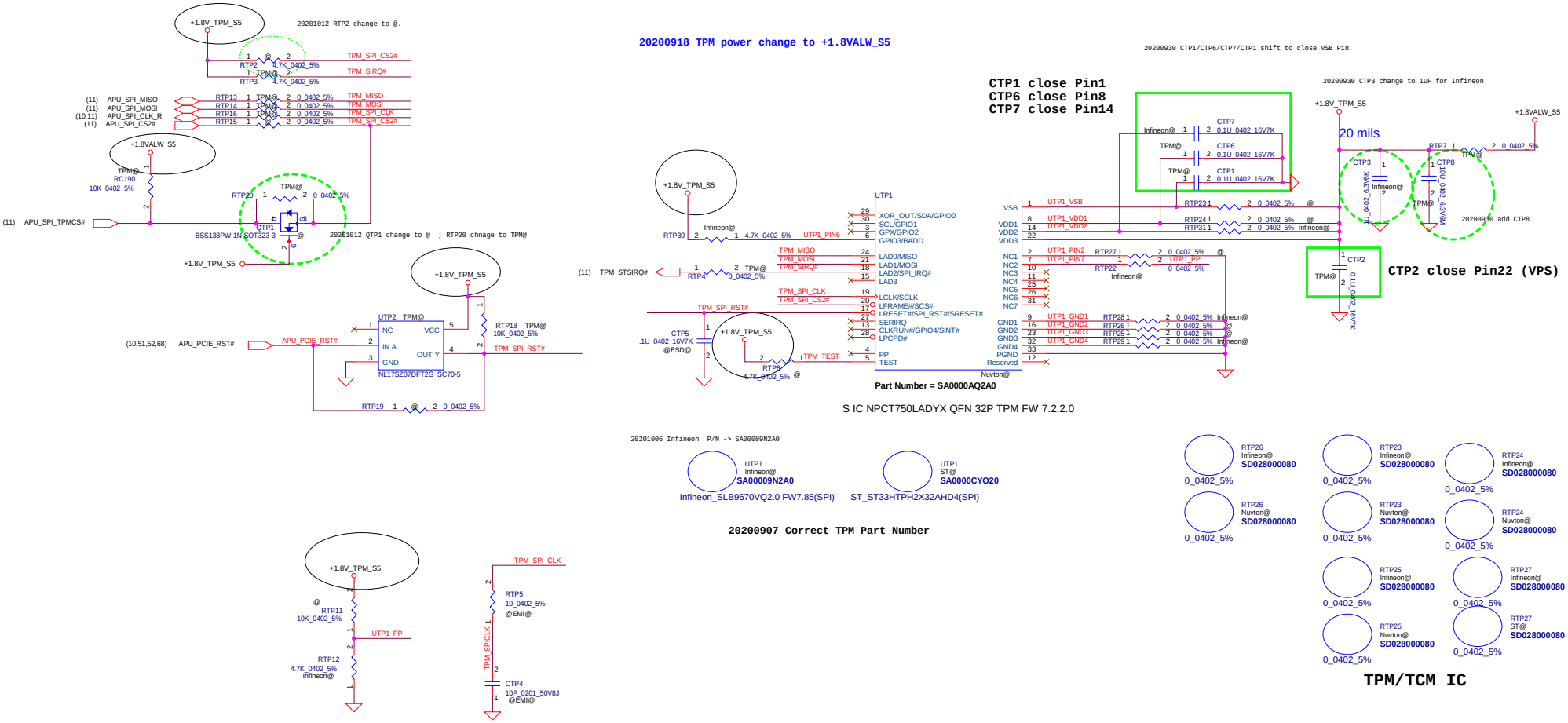
Issued Date	2019/08/01	Deciphered Date	2018/10/01	Title	RESERVE	
				Size B	Document Number LA-K901P	Rev 0.1
				Date: Monday, January 25, 2021	Sheet 63 of 121	

TPM 2.0 Co-lay

1.Nuvton_NPCT650LBAYX
2.ST_ST33HTPH2E32AAE8
3.Infineon_SLB 9670

NEW PART:
Nuvoton NPCT750LABYX
/Infineon SLB9670(FW7.85)
/ST ST33TPHF2ESPI(FW75.00)



(Default)

Pop / Un-pop For Co-lay	RTP22	RTP23	RTP24	RTP25	RTP26	RTP27	RTP28	RTP29	BOM Config
Nuvton_NPCT650LBAYX(SPI)	X	V	V	V	V	X	X	X	Nuvton@+TPM@
ST_ST33HTPH2E32AAE8(SPI)	V	X	X	X	X	V	X	X	ST@+TPM@
Infineon_SLB 9670(SPI)	V	V	V	V	V	V	V	V	Infineon@+TPM@

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Issued Date	2019/08/01	Deciphered Date 2018/10/01	Title: TPM
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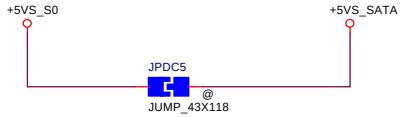
			Date: Monday, January 25, 2021; Sheet 66 of 121

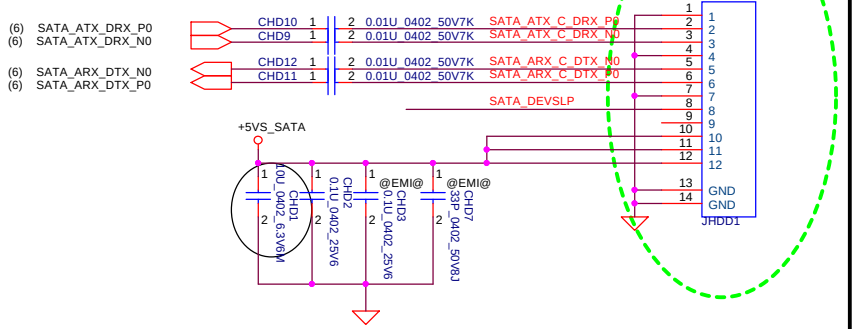
SATA HDD Conn.



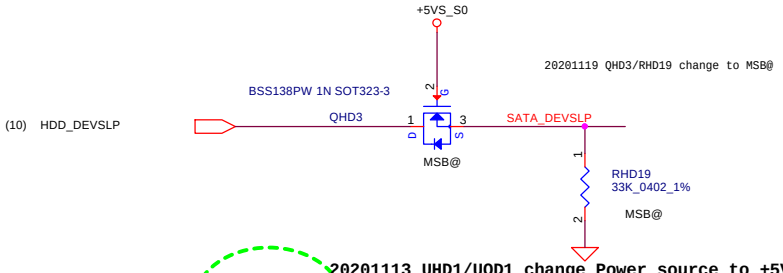
20201006 Correct JHDD1 Pin define

Place CAP close to JHDD1 <100mil

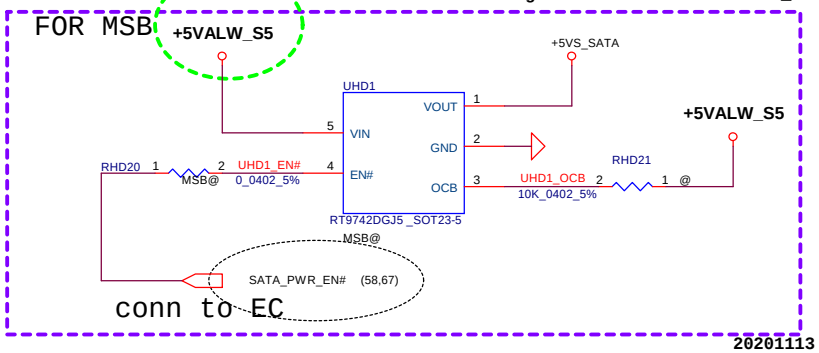
PCB Footprint = CVILU_CF5012FD0R0-05-NH_12P-S



20210114 CHD1,COD1 SE000005T80 (10U_0603) --> SE00000UD00 (10U_0402)

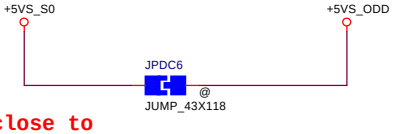


20201113 UHD1/UOD1 change Power source to +5VALW_S5

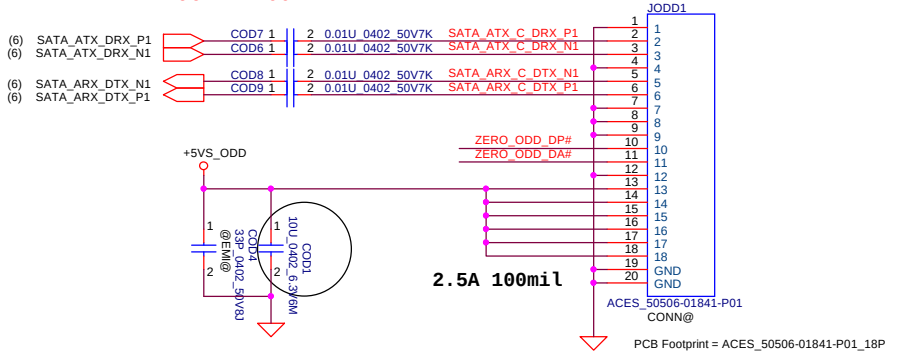


20201113 UHD1/UOD1 change EN# net to SATA_PWR_EN#

SATA ODD FFC Conn

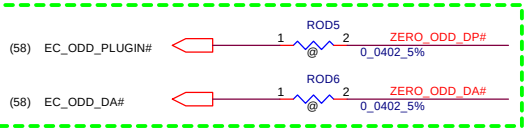


Place CAP close to JODD <100mil



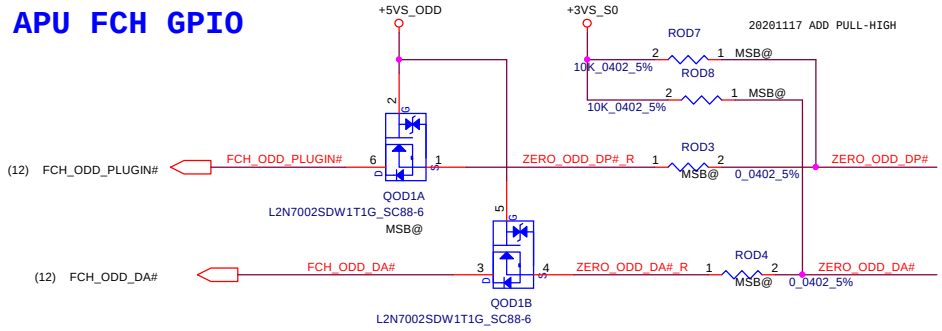
PCB Footprint = ACES_50506-01841-P01_18P

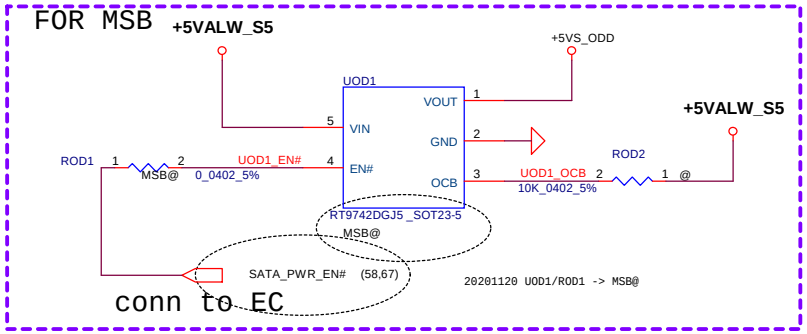
To EC



20201117 ADD ZERO POWER ODD

To APU FCH GPIO





20201120 UOD1/ROD1 -> MSB@

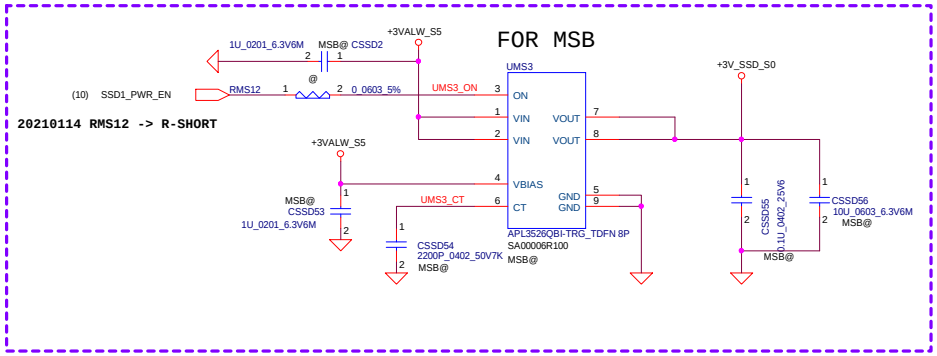
Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

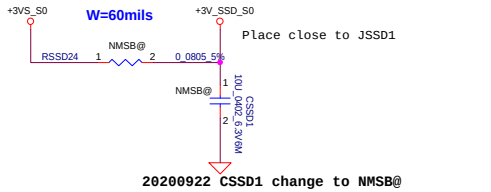
Compal Electronics, Inc.

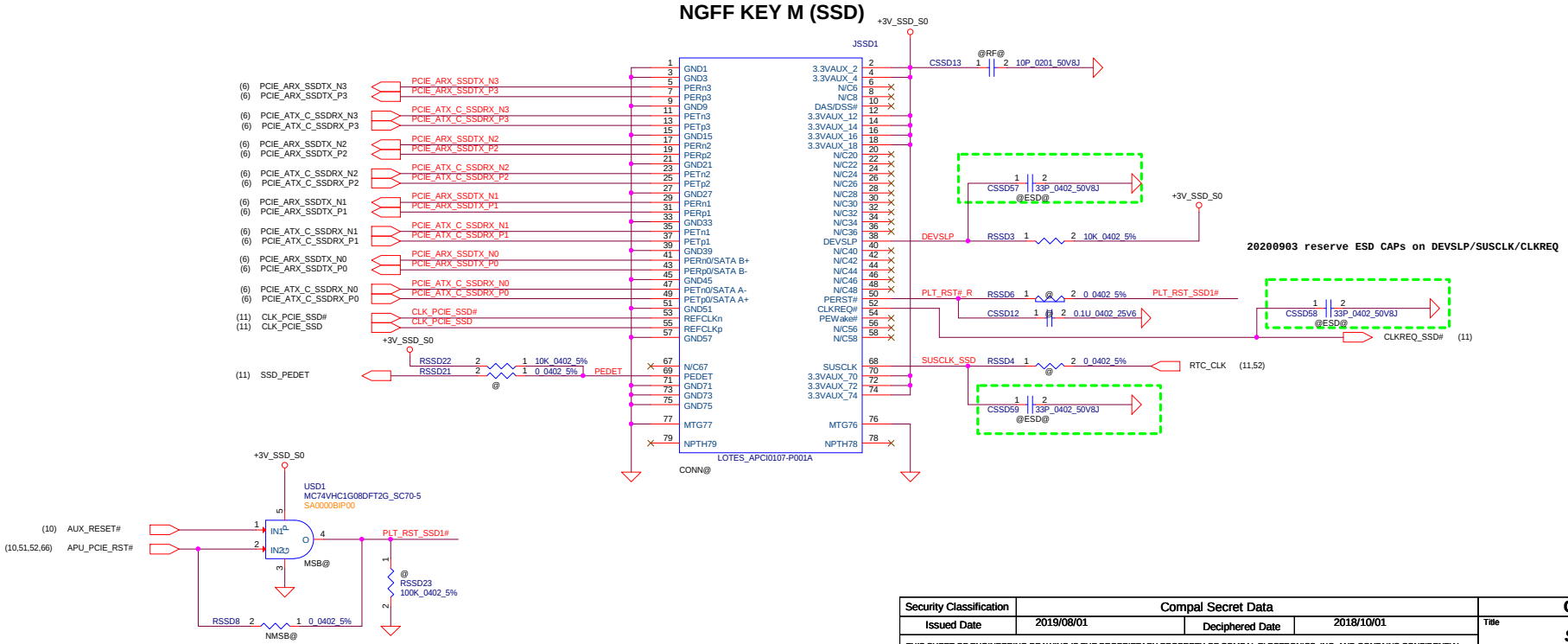
Title: ***HDD/ODD***

Size	Document Number	Rev
Custom	LA-K901P	0.1

Date: Monday, January 25, 2021 Sheet 67 of 121







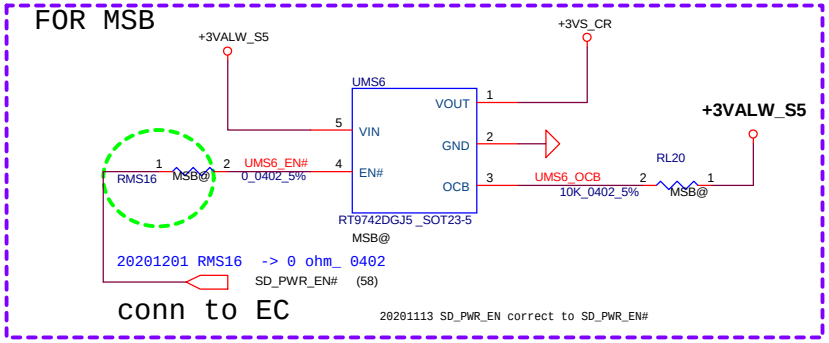
Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

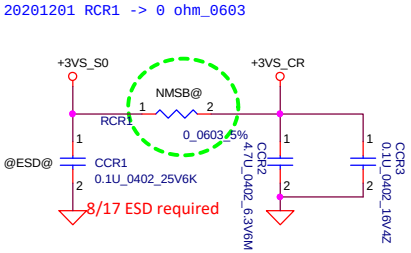
Compal Electronics, Inc.

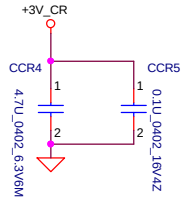
Title: ***SSD (M2) - PCIE SSD***

Size	Document Number	Rev
Custom	LA-K901P	0.1

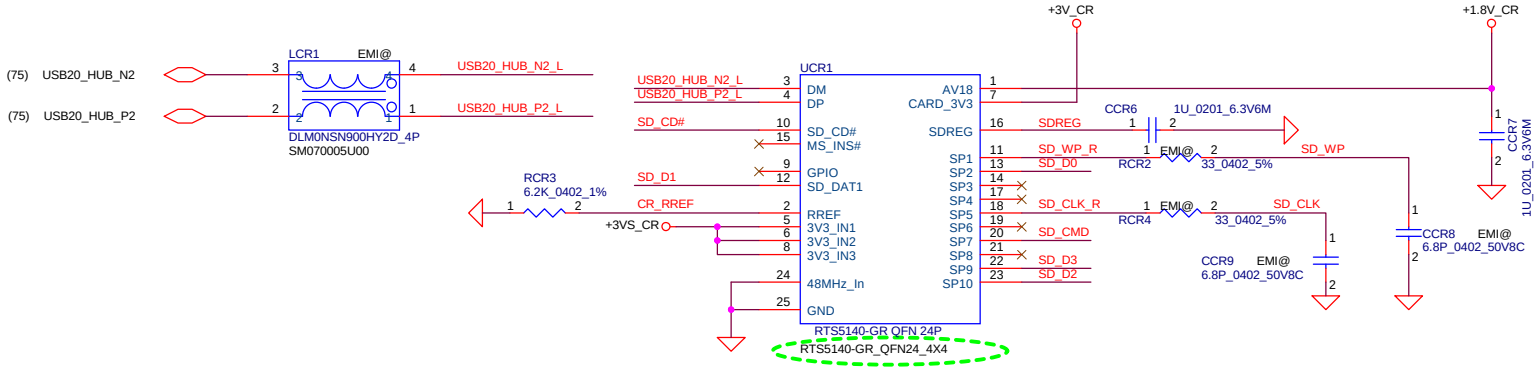
Date: Monday, January 25, 2021 Sheet 68 of 121



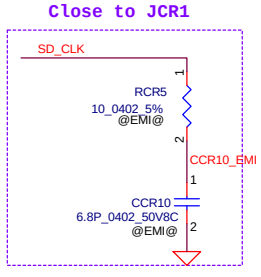


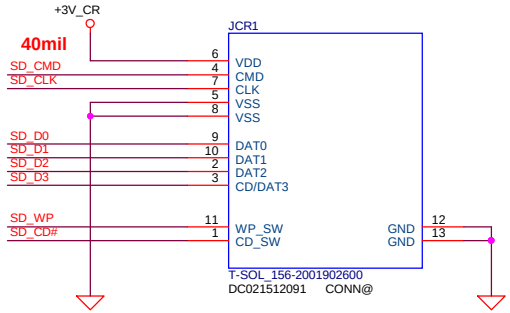


CCR4,CCR5 place close to JCR1.6



20201014 Correct UCR1 Footprint to RTS5140-GR_QFN24_4X4





Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

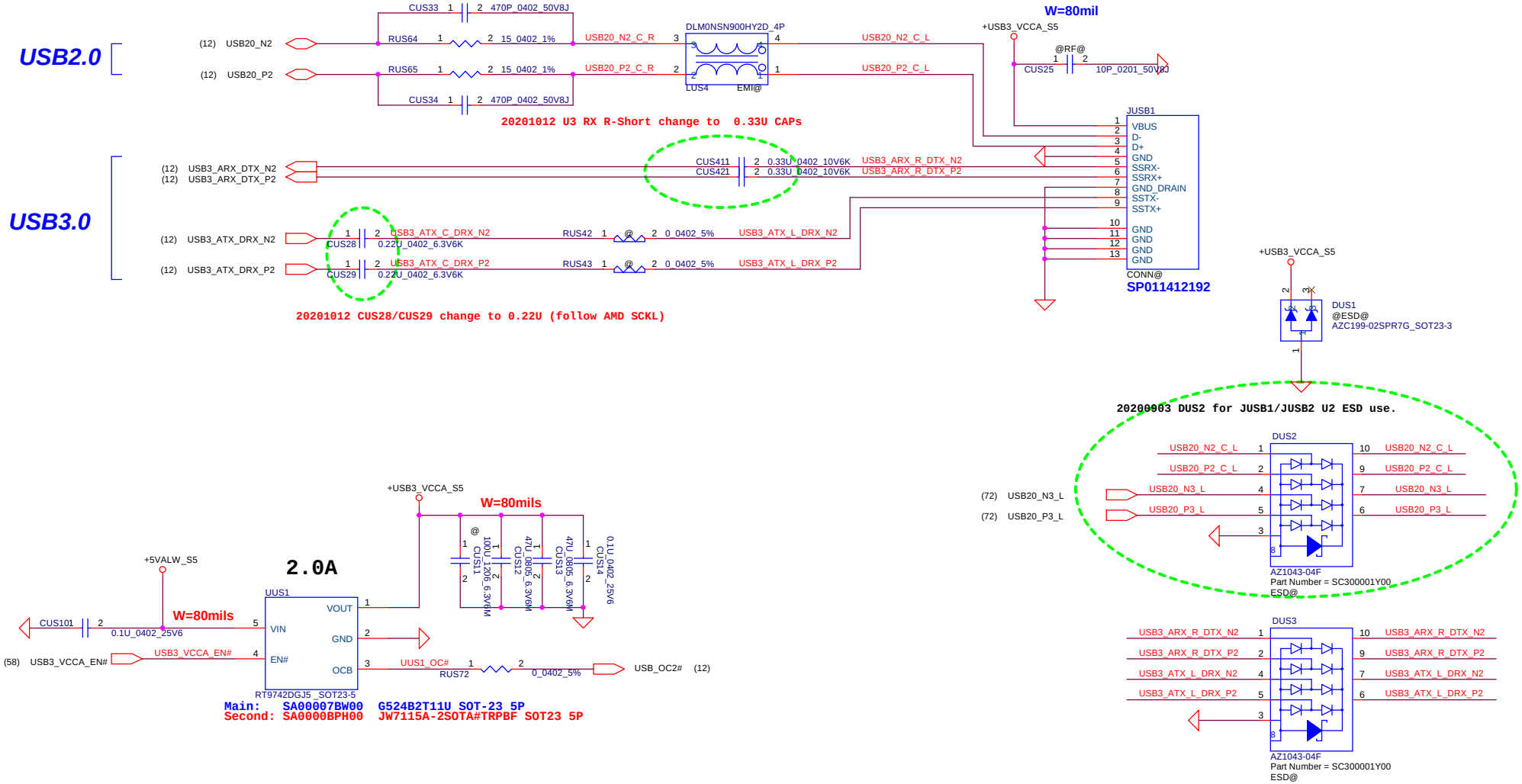
Compal Electronics, Inc.

Title: *CardReader RTS5140*

Size	Document Number	Rev
Custom	LA-K901P	0.1

Date: Monday, January 25, 2021 Sheet 70 of 121

Rear USB3.1 Port 1



Compal Electronics, Inc.

Title: *Rear USB3.1 Port1*

Size: Custom | Document Number: LA-K901P | Rev: 0.1

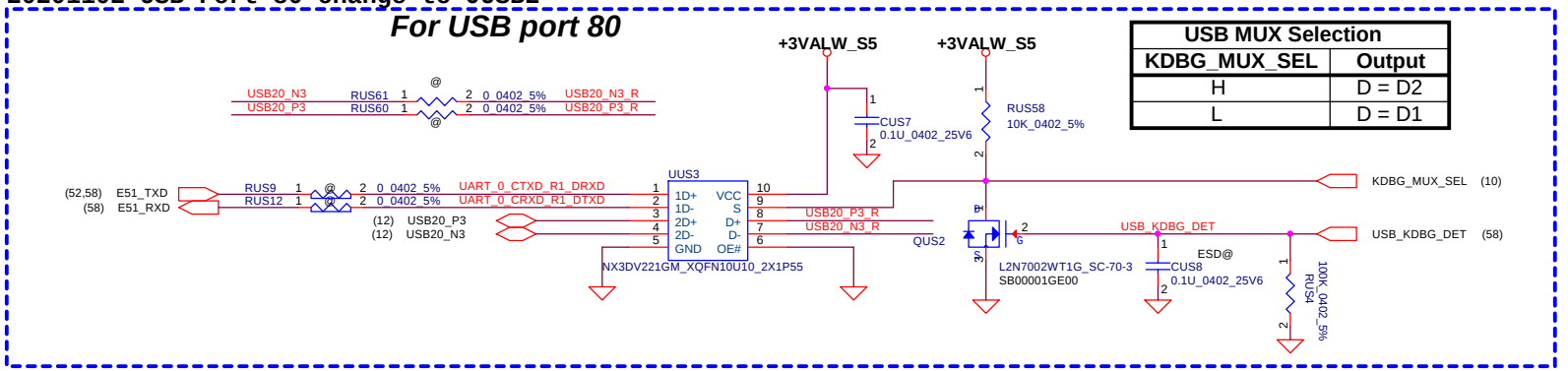
Date: Monday, January 25, 2021 | Sheet 71 of 121

Rear USB3.0 Port2

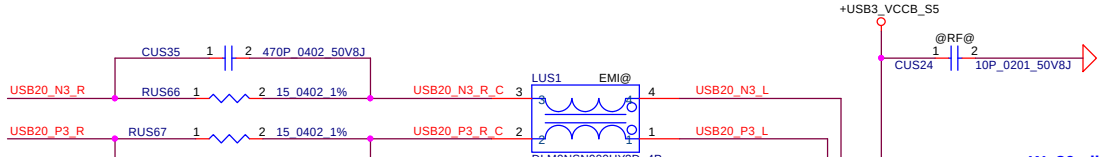
20201102 USB Port 80 change to JUSB2

For USB port 80

USB MUX Selection	
KDBG_MUX_SEL	Output
H	D = D2
L	D = D1

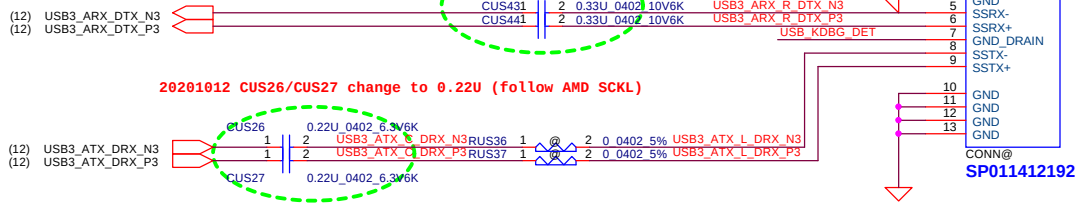


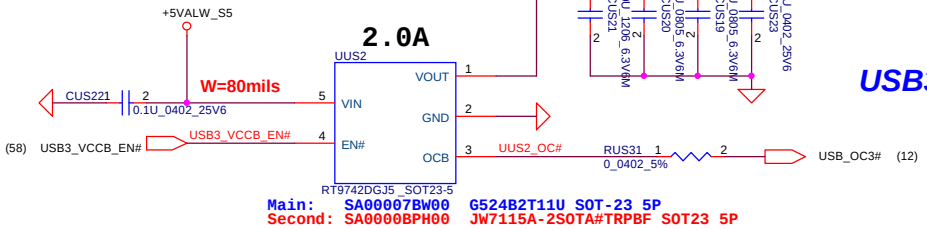
USB2.0



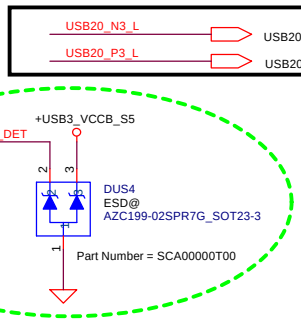
20201012 U3 RX R-Short change to 0.33U CAPs

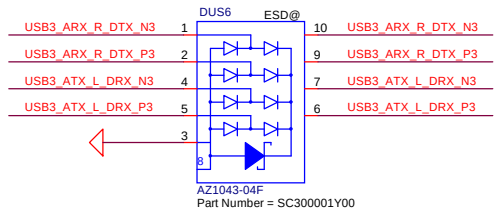
USB3.0





Main: SA00007BW00 G524B2T11U SOT-23 5P
Second: SA0000BPH00 JW7115A-2SOTA#TRPBF SOT23 5P





20201126 USB_KDBG_DET change to connect DUS4 , DUS4 -> ESD@

Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: *Rear USB3.0 Port2 / SMART PWRON*

Size	Document Number	Rev
Custom	LA-K901P	0.1

Date: Monday, January 25, 2021 Sheet 72 of 121

USB2.0 Ports
with SMART POWER ON

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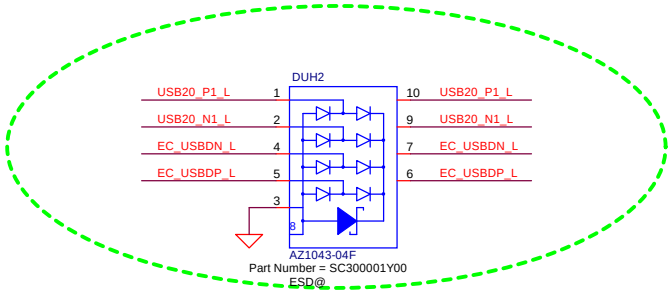
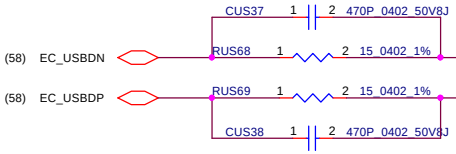
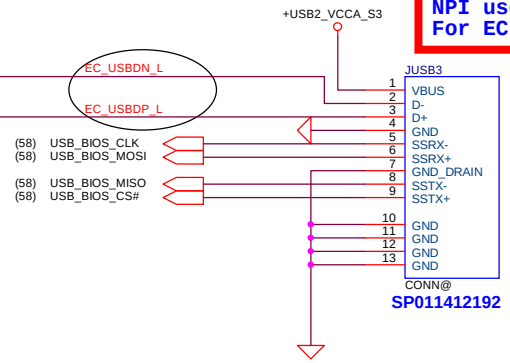
20201126 Remove DUS5 , only use DUH2 for JUSB3/JUSB4 USB2.0.

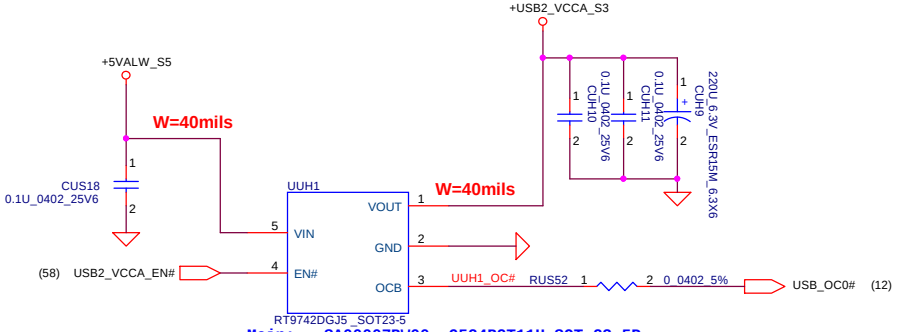




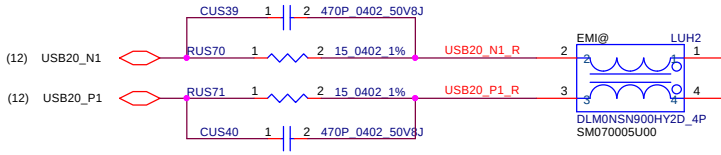


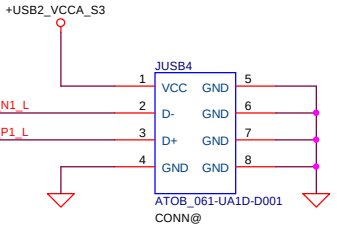
USB2.0 Conn.

NPI use U3 Conn.
For EC Tool



Main: SA00007BW00 G524B2T11U SOT-23 5P
Second: SA0000BPH00 JW7115A-2SOTA#TRPBF SOT23 5P





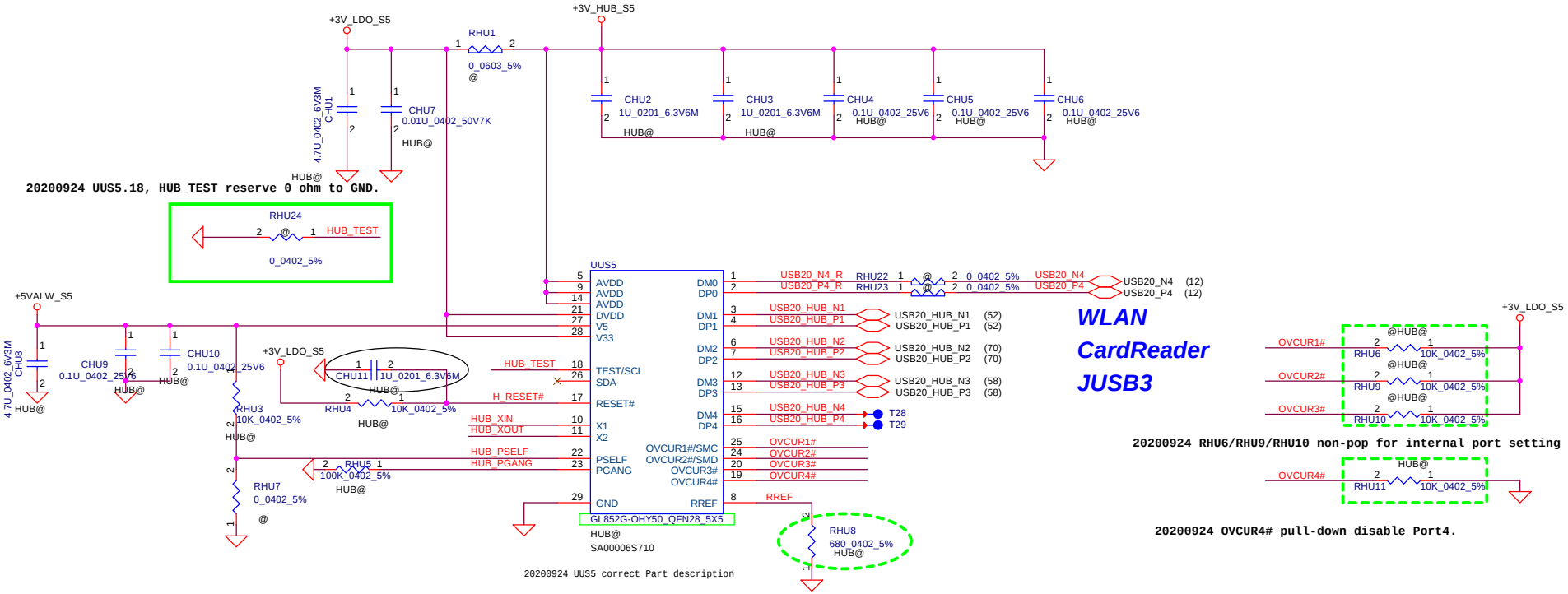
Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: ***Rear USB2.0 x 2***

Size	Document Number	Rev
Custom	LA-K901P	0.1

Date: Monday, January 25, 2021 Sheet 73 of 121



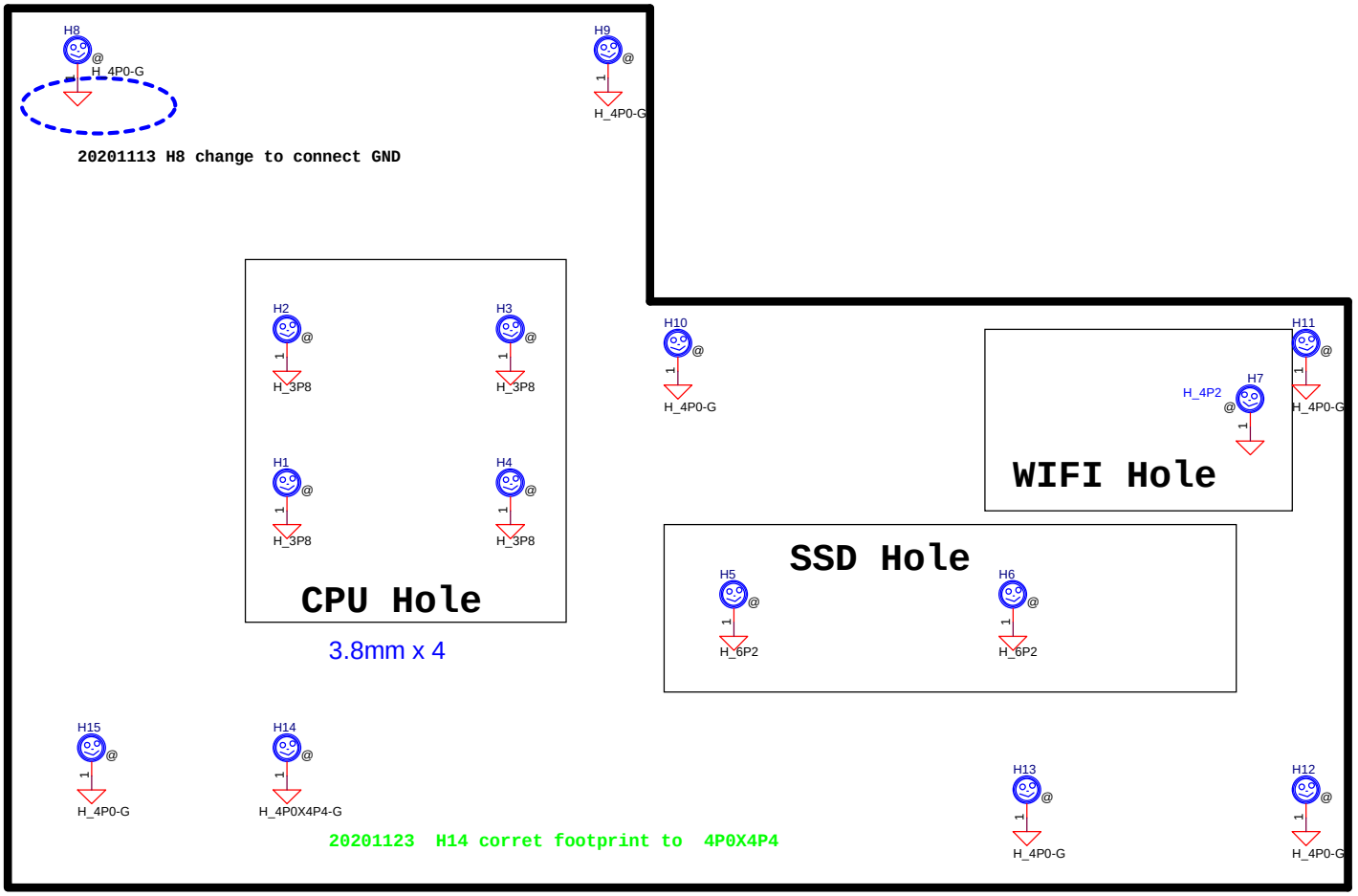
20180321 UUS7 change to SA00006S710
20180129 : UUS5/UUS7 CHANGE TO SA00003OQ10 S IC GL852G-OHG12 QFN28P USB 2.0 MTT HUB

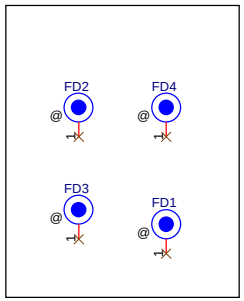
Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2015/01/20

Compal Electronics, Inc.			
Title: USB Hub x2			
Size: Custom	Document Number: LA-K901P		Rev: 0.1
Date: Monday, January 25, 2021	Sheet 75 of 121		

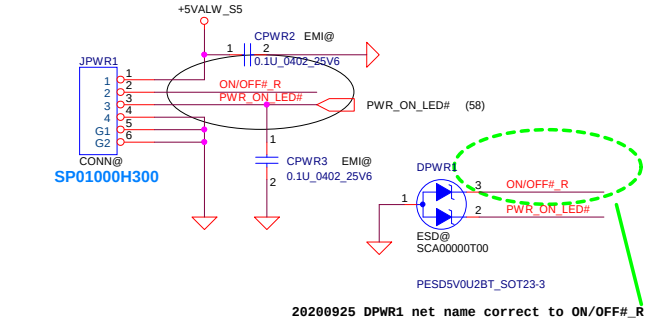
Screw Hole

MB Hole

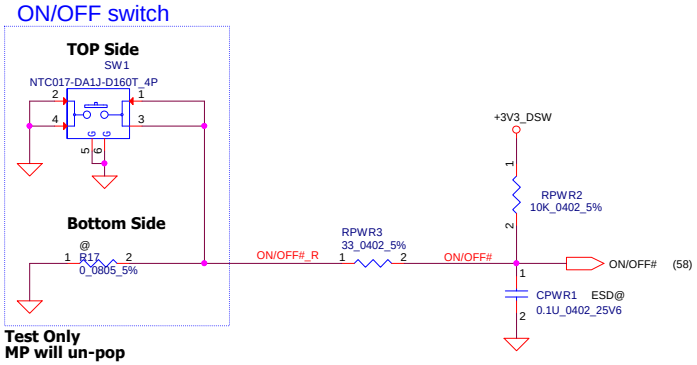




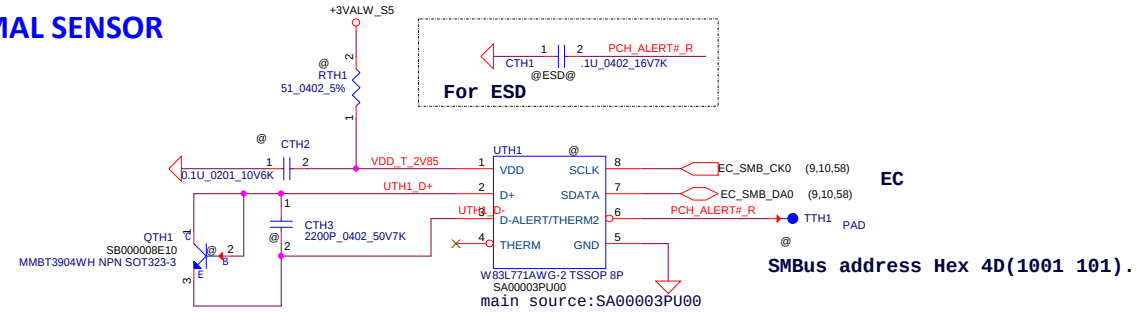
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2019/08/01	Deciphered Date 2018/10/01	Title: Screw Hole
			Size: B / Document Number: LA-K901P / Rev: 0.1
			Date: Monday, January 25, 2021 / Sheet 76 of 121

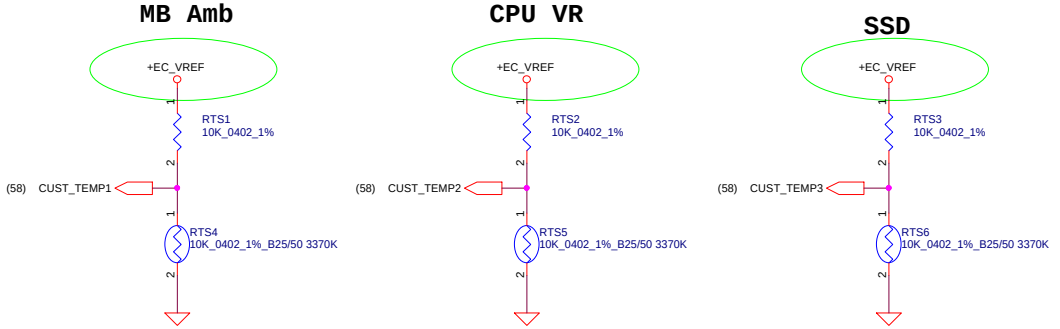


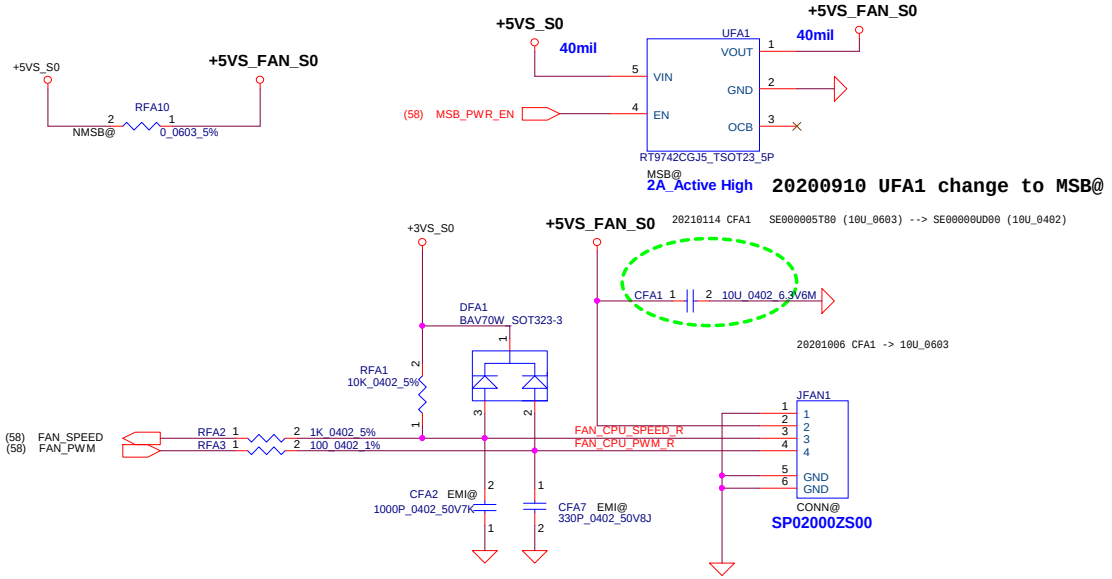
Power Button



THERMAL SENSOR







PCB

ZZZ PCB@

PCB 3B5 LA-K901P REV0 M/B

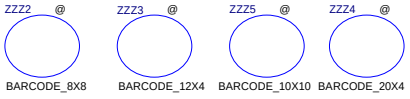
DAZ3B500101

ZZZ 45@

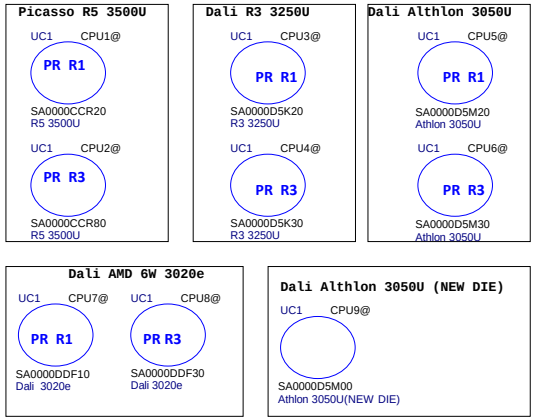
ROYALTY HDMI W/LOGO+HDCP

RO0000003HM

BARCODE



CPU



Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.

Title: *PWR Conn./FAN/Thermel/SCREW*

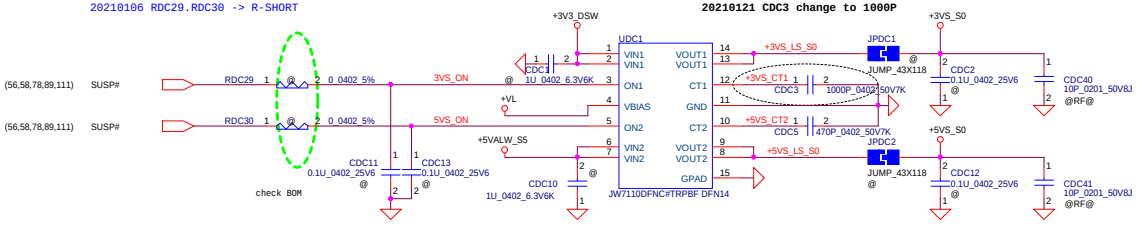
Size	Document Number	Rev
Custom	LA-K901P	0.1

Date: Monday, January 25, 2021 Sheet 77 of 121

VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=21mohm

20210106 RDC29.RDC30 -> R-SHORT

20210121 CDC3 change to 1000P

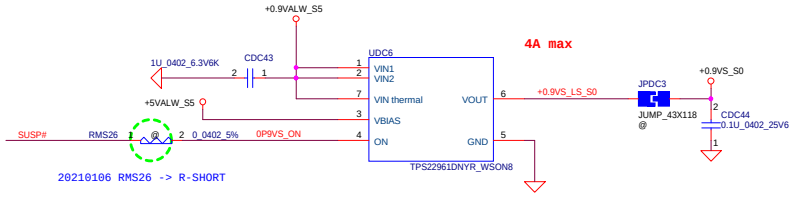


1st source : JW7110DFNC (SA0000BEL00)
2nd source : G2898KD1U (SA0000BKC00)

VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=15mohm

20210121 UDC1 main source change to SA0000BEL00

20200917 UDC6 change solution - TPS22961D

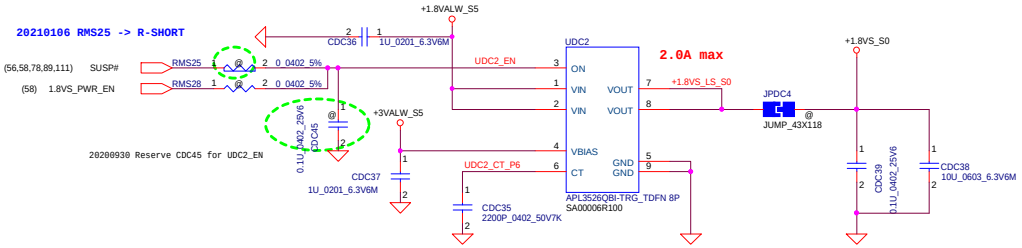


20210106 RMS26 -> R-SHORT

VIN 0.9 (VBIAS=5V),IMAX=6A,Rds=4.4mohm

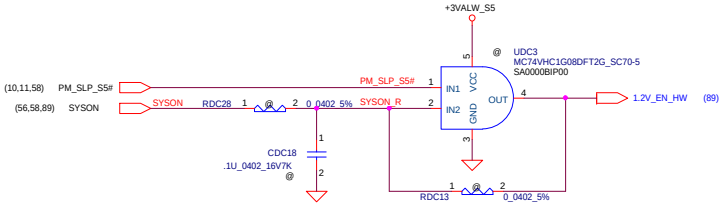
1st source : TPS22961 (SA00007XR00)
2nd source : G5027RD1D (SA0000BMA00)

20210106 RMS25 -> R-SHORT

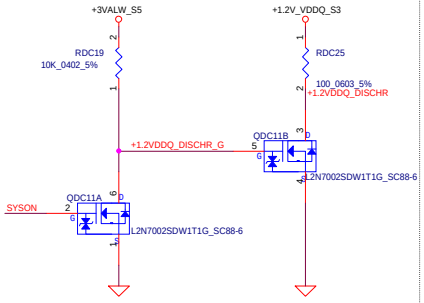


1st source : APL3526 (SA00006R100) Rdson : 27mohm
2nd source : JW7106DFND (SA0000CDD00) Rdson : 30mohm

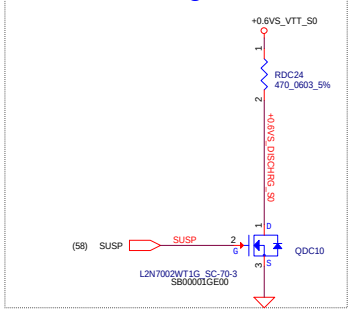
DDR power control



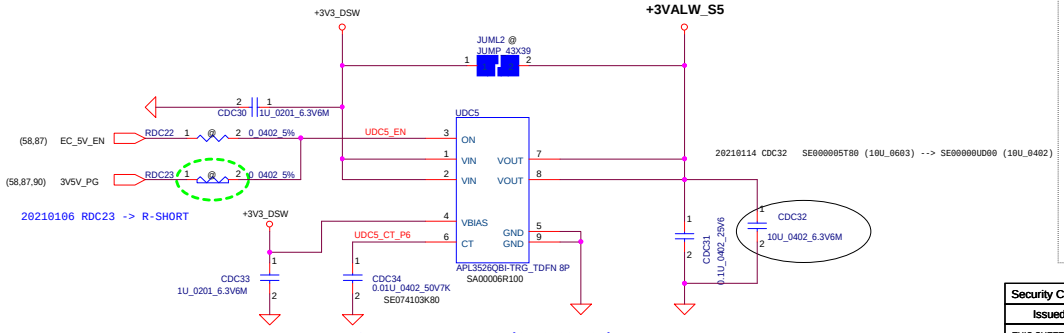
+1.2V Discharge circuit



VTT Discharge circuit



+3VDSW_S5 to +3VALW_S5 Transfer



20210106 RDC23 -> R-SHORT

1st source : APL3526 (SA00006R100) Rdson : 27mohm
2nd source : JW7106DFND (SA0000CDD00) Rdson : 30mohm

Security Classification	Compal Secret Data		
Issued Date	2019/08/01	Deciphered Date	2018/10/01

Compal Electronics, Inc.	
Title	DC INTERFACE
Size	C
Document Number	LA-K901P
Rev	0.1
Date:	Monday, January 25, 2021
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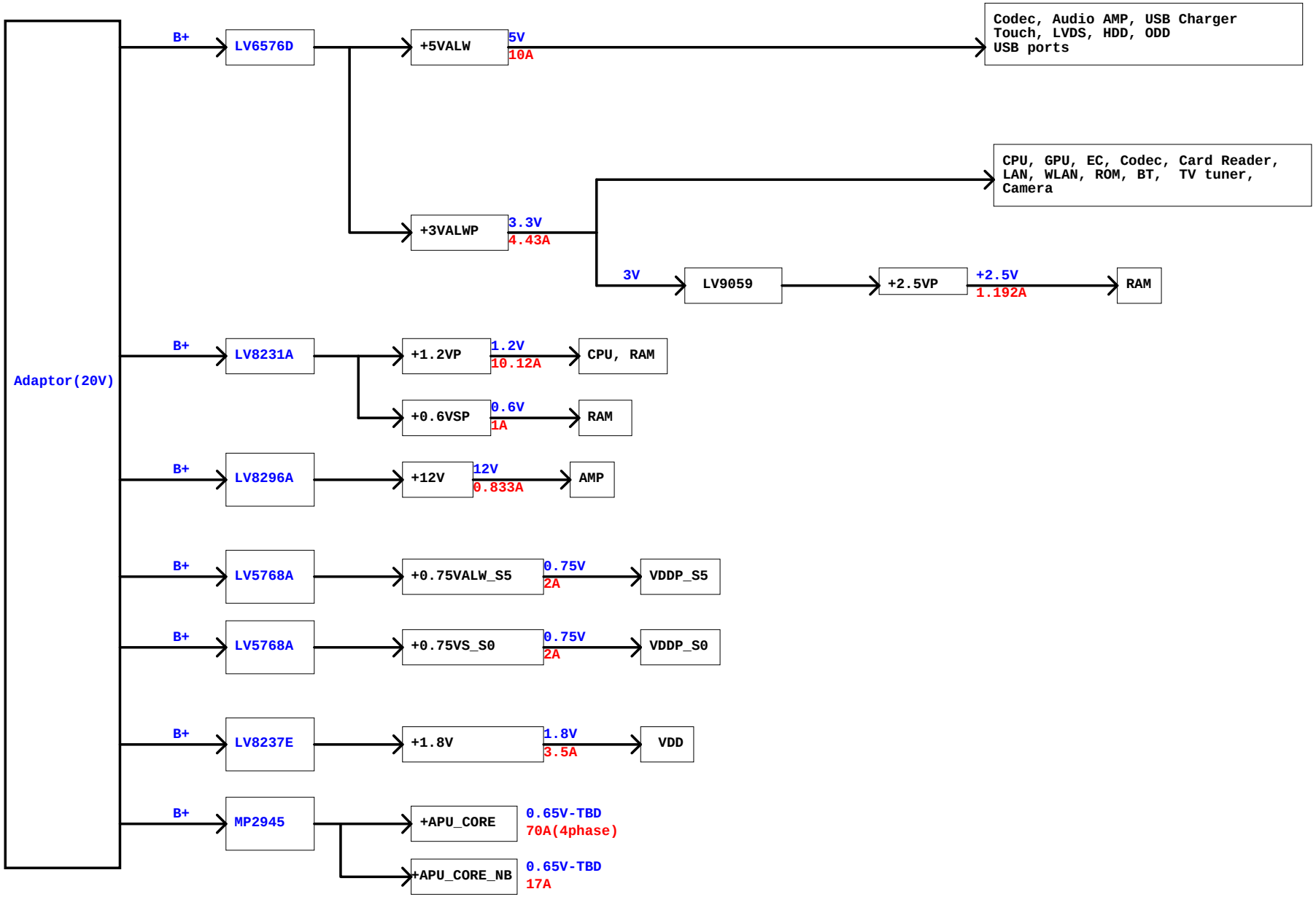

Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: **Power Rail**

Size	Document Number	Rev
Custom		0.1

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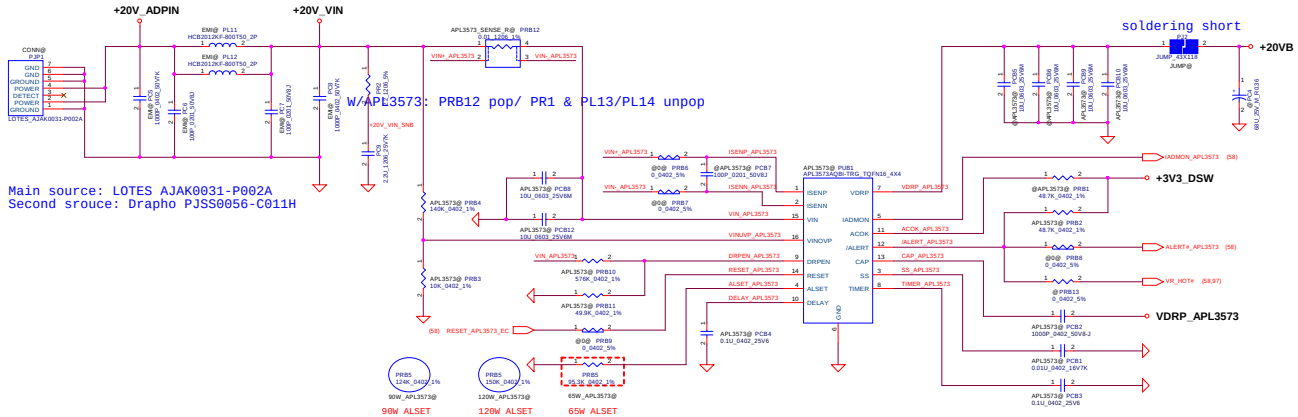
+3VL_S5 +3VL_RTC_S5

@@@ PR11 0_0402_5%

RTC BATT CONNECTER

+RTCBATT_G3 PJP2

LOTES_AAA-BAT-054-K01 CONN@



Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: DCIN / CONN

Size	Document Number	Rev
Custom		0.1

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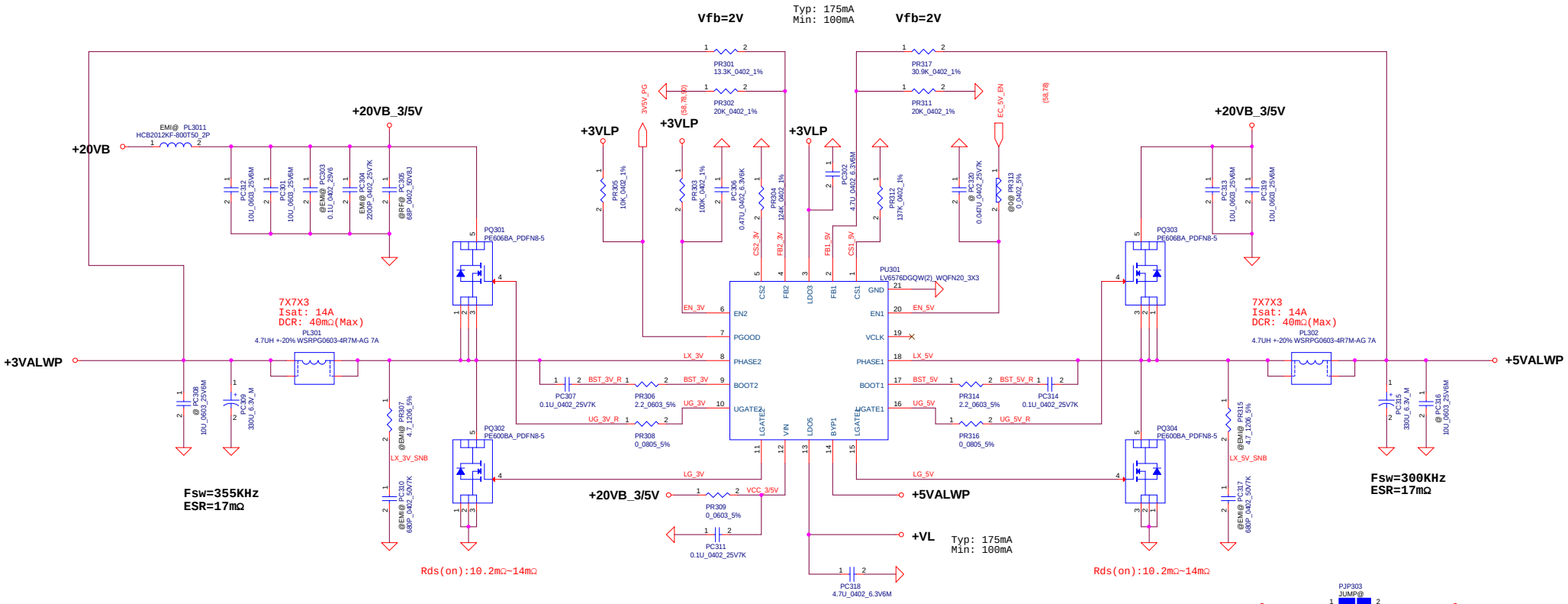
1st source: LV6576D
2nd source: GS7225BTQ-RLV



+3VALWP
Vin = 20V
Iin = 3.3*6/0.85/20
= 1.165A

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(13.3K/20K)]
= 3.3V

+3VALWP
Imax=4.2A, Ipeak=6A; Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10A~14A
Iin_ripple=1.56A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.651A
LIR=Delta IL/Ipeak=0.275
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=269.83uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.56uF

+5VALWP
Vin = 20V
Iin = 5*7/0.85/20
= 2.06A

Vout = Vfb*[1+(Rt/Rb)]
= 2*[1+(30K/20K)]
= 5V

+5VALWP
Imax=4.9A, Ipeak=7A; Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:10.2ohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10A~14A
Iin_ripple=2.08A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.660A
LIR=Delta IL/Ipeak=0.387
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=86.82uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.5uF

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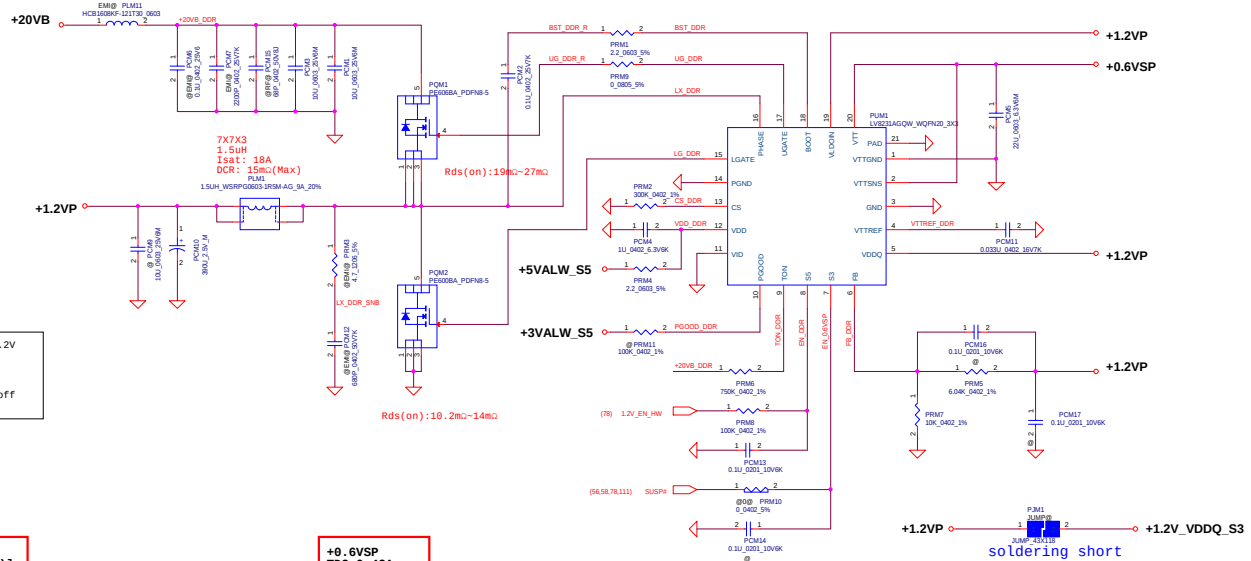
Issued Date	2013/08/15	Deciphered Date	2013/08/29

Title	+3VALWP / +5VALWP		
Size C	Document Number		Rev 0.1
Date: Monday, January 25, 2021	Sheet 87 of 121		

1st source: LV8231AGQW
2nd srouce: GS7272DQ3-RLV



Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

+1.2VP
Vin = 20V
Iin = 1.2*7.8/0.85/20
= 0.55A

Vout = Vfb*[1+(Rt/Rb)]
= 0.75*[1+(6.04K/10K)]
= 1.203V

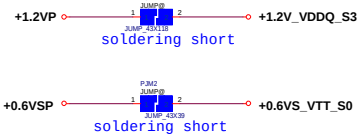
+1.2VP
Imax=5.46A, Ipeak=7.8A ;Fsw=350KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds: L/S --> typ:12.1mohm; max:14mohm
Itrip=9~11 uA
Iocp(set)=11.7~15.6A
Iin_ripple=1.3A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.149A
LIR=Delta IL/Ipeak=0.275
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1100.89uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.44uF

+0.6VSP
TDC=0.42A
Ipeak=0.6A

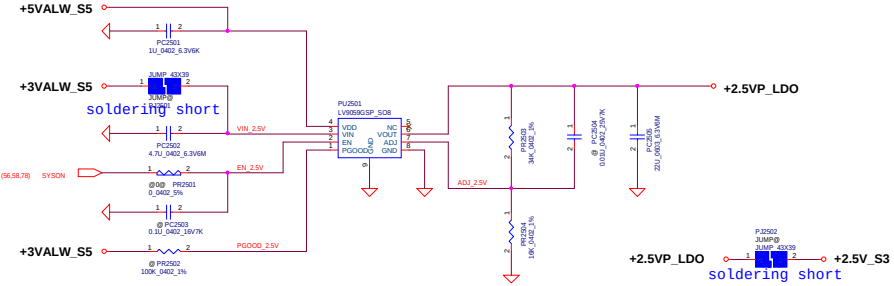
LV8231A:
Quiescent Current (GND Current)
IQ(typ)=0.135mA
PD(MAX) = (TJ(MAX) - TA) / θJA=3.33W
θJA= 30°C/W

GS7272:
Quiescent Current (GND Current)
IQ(typ)=0.4mA
PD(MAX) = (TJ(MAX) - TA) / θJA=1.667W
θJA= 60°C/W

	main	2nd	
Vo	0.6	0.6	V
Vin	1.2	1.2	V
Io	0.6	0.6	A
PD	3.33	3.33	W
θJA	30	60	°C/W



1st source: LV9059GSP
2nd srouce: APL5933CKAI
3rd srouce: GS7166SO-R



Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(34K/16K)]
= 2.5V

+2.5VP
Imax=0.35,Ipeak=0.5A ;
Current Limit=3.6A(Typ)~4.2A(Max)

LV9059:
Quiescent Current (GND Current)
IQ(typ)=0.6mA
PD(MAX) = (TJ(MAX) - TA) / θJA =2.96W
θ JA= 33.7°C/W

APL5933CKAI:
Quiescent Current (GND Current)
IQ(typ)=1mA
PD(MAX) = (TJ(MAX) - TA) / θJA =2W
θ JA= 50°C/W

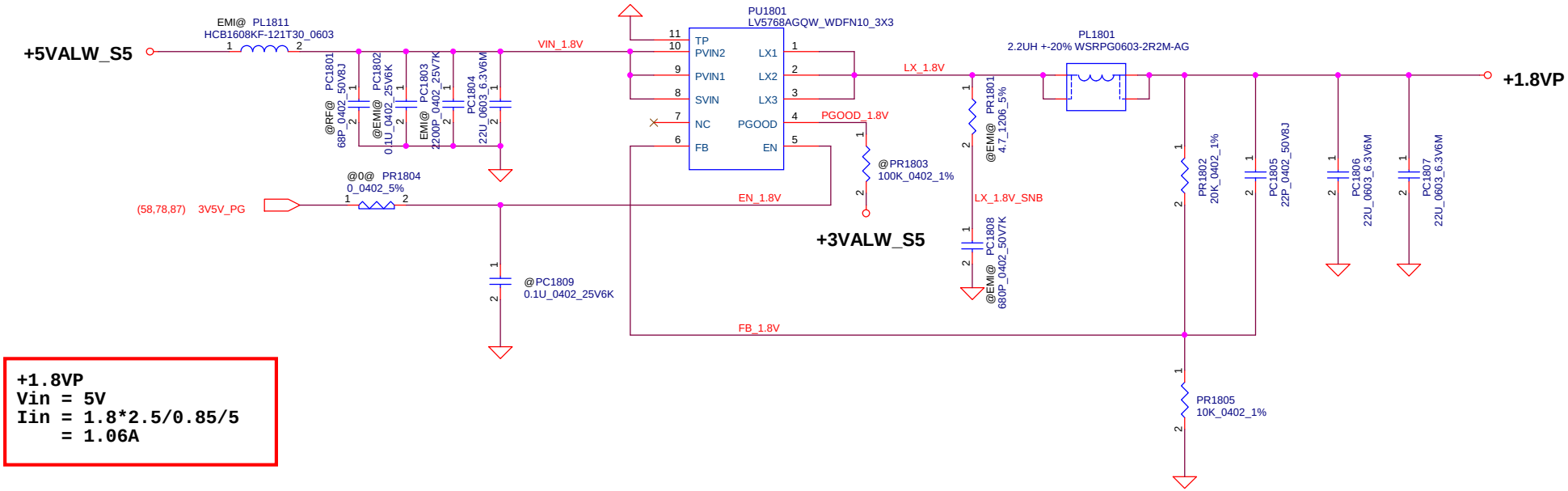
GS7166:
Quiescent Current (GND Current)
IQ(typ)=1mA
PD(MAX) = (TJ(MAX) - TA) / θJA =1.33W
θ JA= 75°C/W

Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.
Title: +1.2VP/+0.6VSP/+2.5VP
Size: Custom | Document Number | Rev: 0.1
Date: Monday, January 25, 2021 | Sheet 89 of 121

1st source: LV5768A
2nd srouce: UP1727P
3rd srouce: GS7302ADTD-R

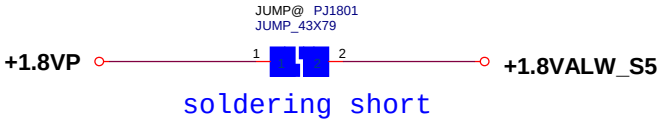
7x7x3
Isat: 18A
DCR: 20mΩ(Max)



+1.8VP
Vin = 5V
Iin = 1.8*2.5/0.85/5
= 1.06A

Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(20K/10K)]
= 1.8V

+1.8VP
Imax=1.75A, Ipeak=2.5A; Fsw=1MHz
Current Limit=4A
Iin_ripple=0.84A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.524A
LIR=Delta IL/Ipeak=0.209
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=68.03uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.81uF



soldering short

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Issued Date	2014/12/26	Deciphered Date	2017/10/19
Title: +1.8V(LV5768)			
Size	Document Number		Rev 0.1
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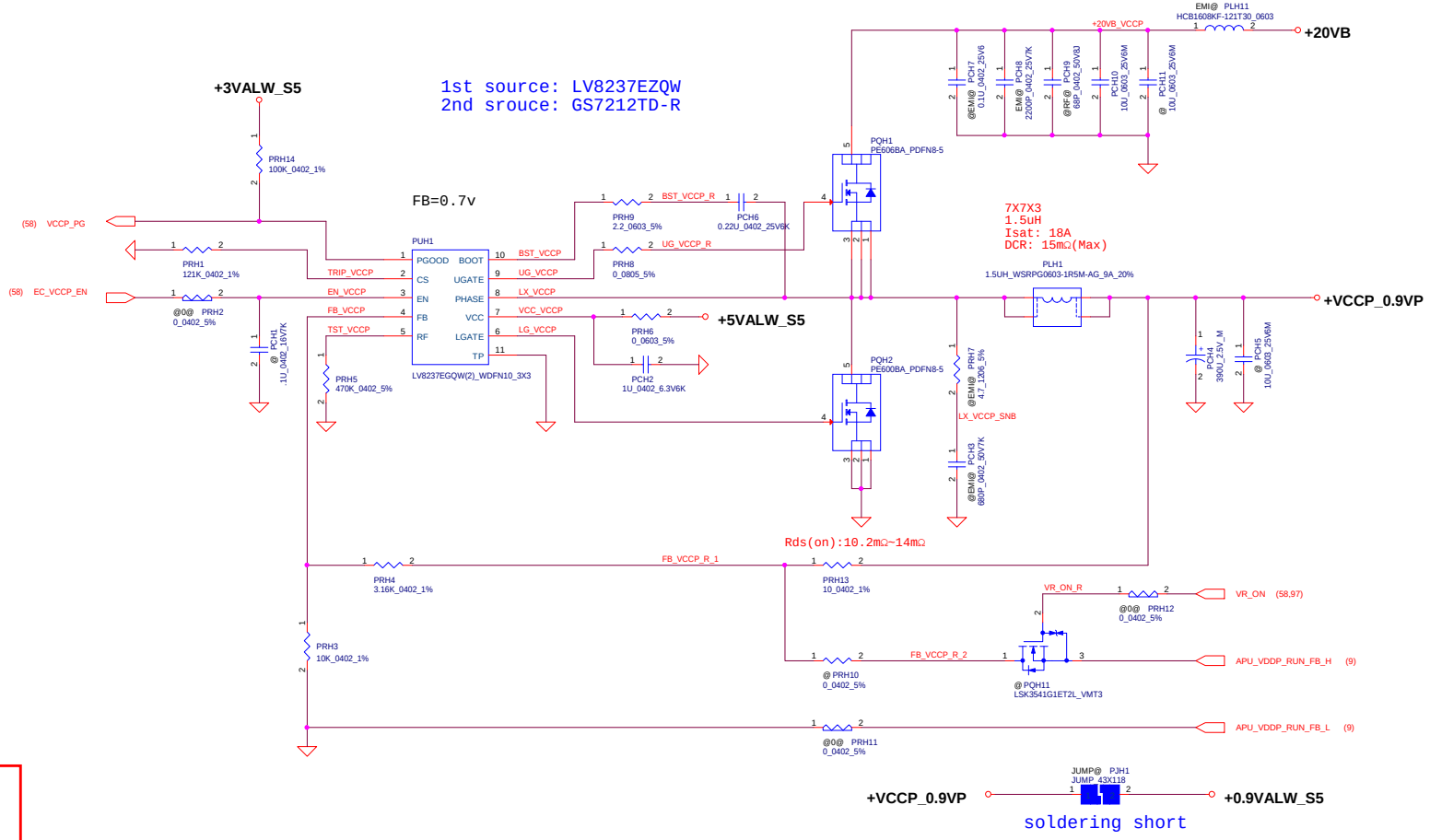

+VCCP_0.9VP
Vin = 20V
Iin = 0.9*5/0.85/20
= 0.271A

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(3.16K/10K)]
= 0.92V

+VCCP_0.92V
Imax=3.5A, Ipeak=5A; Fsw=290K
Rds: L/S --> typ: 12.1mohm; max: 14mohm
Iocp(set)=10A~14A
Iin_ripple=0.73A
Output Cap. ESR=10mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.976A
LIR=Delta IL/Ipeak=0.395
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=923.25uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.26uF

Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

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Title: **+VCCP_0.9VP**

Size	Document Number	Rev
C		0.1

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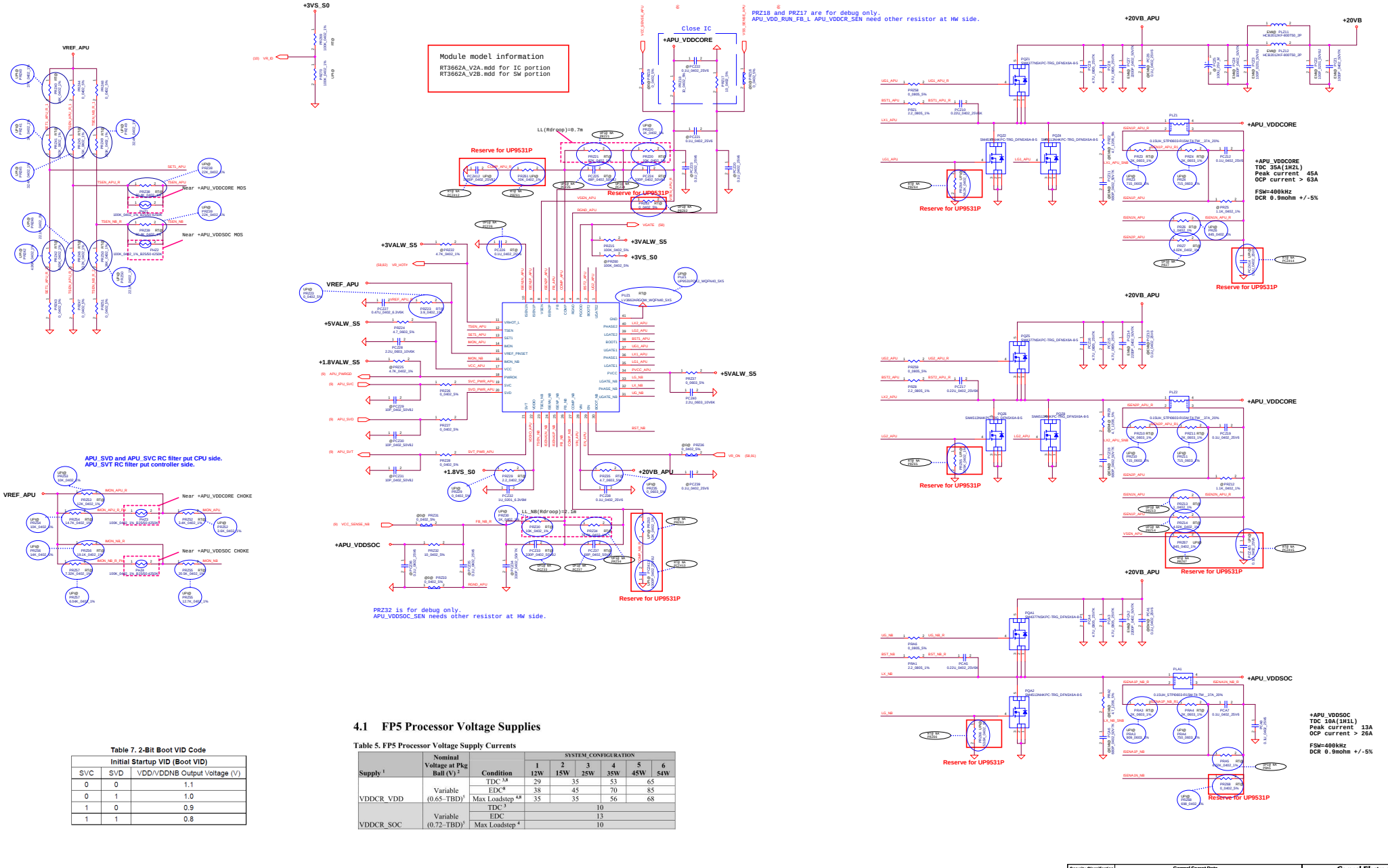

4.1 FP5 Processor Voltage Supplies

Table 5. FP5 Processor Voltage Supply Currents

Supply [1]	Nominal Voltage at Pkg Ball (V) [2]	Condition	SYSTEM_CONFIGURATION 1 12W	2 15W	3 25W	4 35W	5 45W	6 54W
VDDCR_VDD	Variable (0.65–TBD) [5]	TDC [3,8]	29	35		53		65
		EDC [8]	38	45		70		85
		Max Loadstep [4,8]	35	35		56		68
VDDCR_SOC	Variable (0.72–TBD) [5]	TDC [3]	10					
		EDC	13					
		Max Loadstep [4]	10					

Table 7. 2-Bit Boot VID Code

Initial Startup VID (Boot VID)		
SVC	SVD	VDD/VDDNB Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

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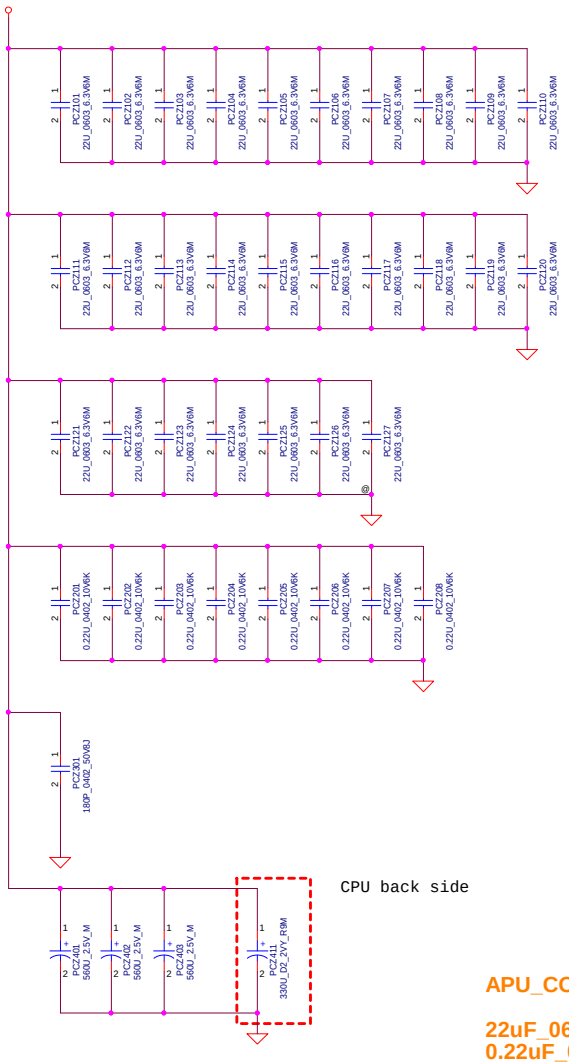
		Size	Document Number / Rev 1.0
		Date	Monday, January 29, 2018 / Sheet 67 of 104

+APU_VDDCORE

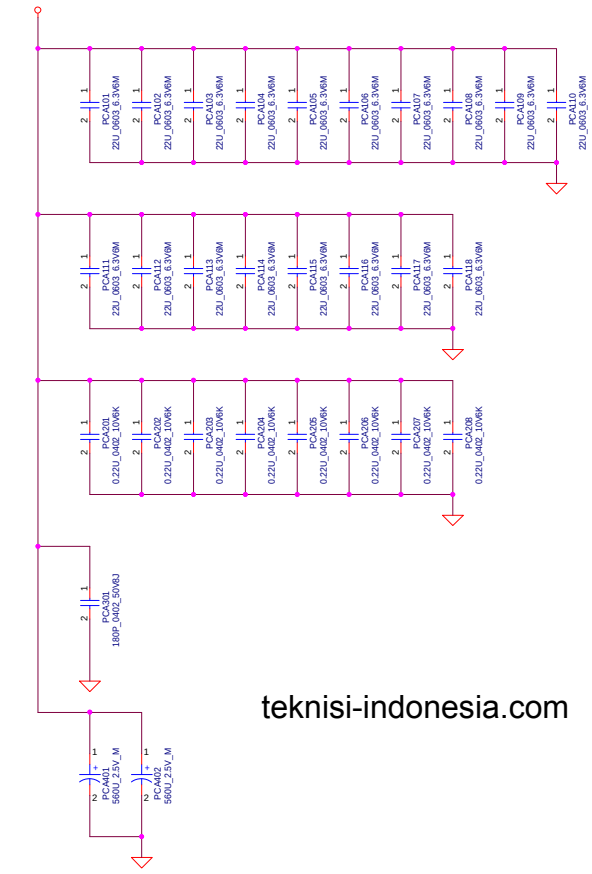
+APU_VDDCORE



CPU back side

+APU_VDDSOC

+APU_VDDSOC



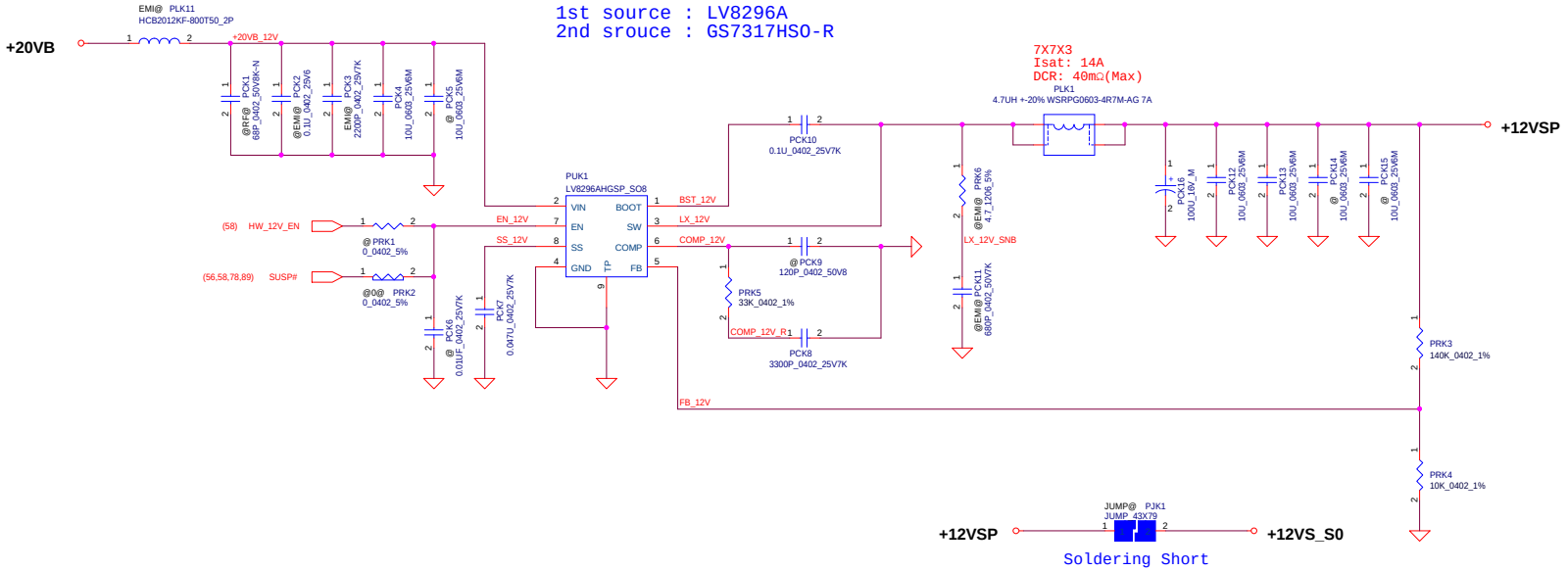
APU_CORE

22uF_0603	27	pcs
0.22uF_0402	8	pcs
180pF_0402	1	pcs
560uF_10m	3	pcs
330uF_9m	1	pcs

APU_CORE_SOC

22uF_0603	18	pcs
0.22uF_0402	8	pcs
180pF_0402	1	pcs
560uF_10m	2	pcs

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2016/12/05	Deciphered Date	2017/12/05
Title	APU_CORE CAP		
Size C	Document Number		Rev 0.1
Date: Monday, January 25, 2021	Sheet 101 of 121		



+12VSP
Vin = 20V
Iin = 12*0.83/0.85/20
= 0.59A

Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(140K/10K)]
= 12V

+12VSP
Imax=0.58A, Ipeak=0.83A; Fsw=340KHz
Current Limit=3.8A(Min)
Iin_ripple=0.86A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.004A
LIR=Delta IL/Ipeak=1.202
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=4.23uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.62uF

Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2017/10/19

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Title: **+12VSP**

Size	Document Number	Rev
C		0.1

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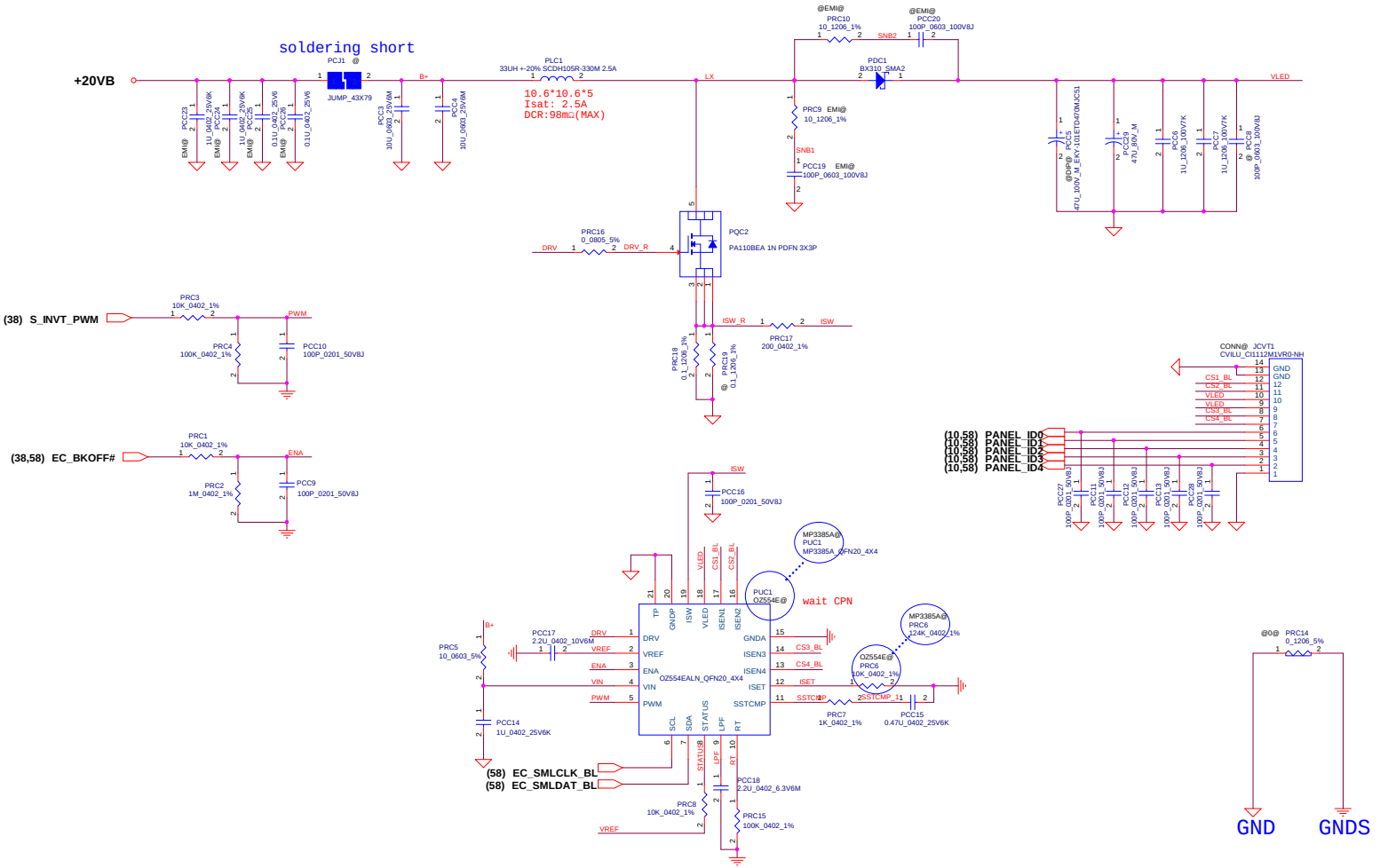

Security Classification	Compal Secret Data		
Issued Date	2020/11/13	Deciphered Date	2020/11/13

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Title: P099-PWR-Backligh(OZ554E)

Size: Custom | Document Number: P099-PWR-Backligh(OZ554E) | Rev: 0.2

Date: | Sheet 112 of 121