Compal Confidential

TESLA 3A
DIS M/B Schematics Document

Intel SkyLake U Processor with DDR3L
Nvidia N16V-GM(920M)

2015-1-26

LA-D061P

REV :1.0

ZZZ BIVS3_PCB

Part Number	Description
DAZ1DD00100	PCB BIVS3 LA-D061P LS-C311P 02, A.2

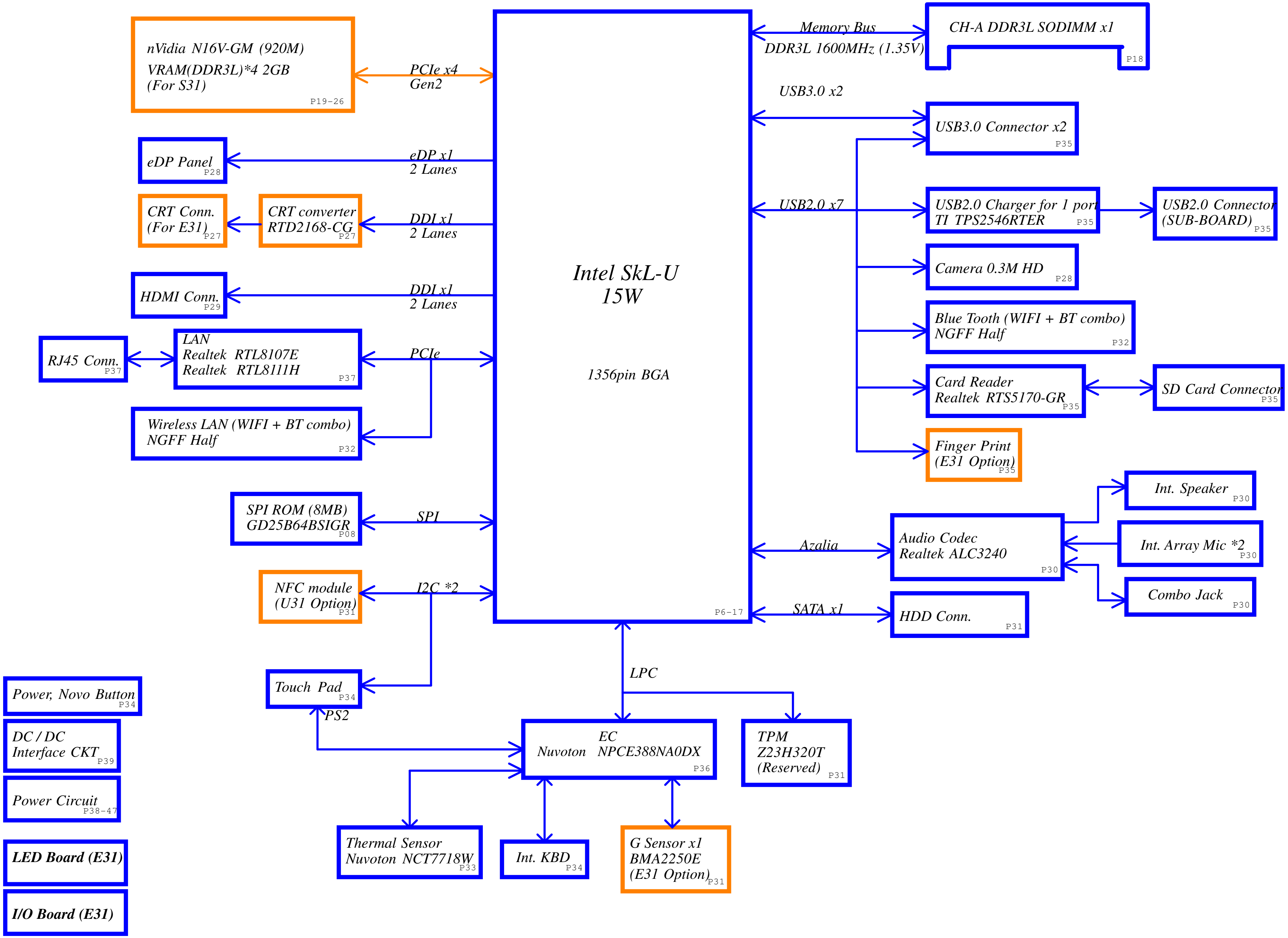
U31@

ZZZ BIVE3_PCB

Part Number	Description
DAZ1DC00100	PCB 1DC LA-D061P REV0 M/B 2

E31@

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: *Cover Page*
				Size: C; Document Number: *LA-D061P*; Rev: 0.3
				Date: Tuesday, August 11, 2015; Sheet 1 of 52



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: MB Block Diagram

Size C | Document Number | Rev 0.3

Date: Friday, August 07, 2015 | Sheet 2 of 52

Voltage Rails

power plane / State	B+	+5VALW +3VALW	+1.5V	+5VS +3VS +1.35VS +1.0VS_VCCOPC +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.0VALW
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
LAN 10/100 Transformer	100@
LAN Giga Transformer	GIGA@
For Giga LAN Chip	8111H@
For 10/100 LAN Chip	8107E@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NOISCT@
For DIS	DIS@
For UMA	UMA@
For TCM	TCM@
No TCM	NOTCM@
For Camera	CMOS@
For NFC Option	NFC@
For G-Senser BOSCH	GSB@
For G-Senser ST	GSST@
No G-Senser	NOGS@
G-Senser	GS@
For FP Option	FP@
For Keyboard backlight	KBL@
No Keyboard backlight	NOKBL@
For USB Charger	CHG@
No USB Charger	NOCHG@
For U31 Option	U31@
For E31 Option	E31@
For Hynix Memory	H2G@
For Samsung Memory	S2G@
For Micron Memory	M2G@
For EMI	EMI@
For ESD	ESD@
No EMI	@EMI@
No ESD	@ESD@
For E31 PWR Button ESD	@E31ESD@
Connector	ME@
For VARM X76	GM_X76@
For Test Point	TP@
for CMC Debug	CMC@
for GT3	GT3@
for 2+3E power	23E@

ZZZ1 @ BARCODE_8X8
ZZZ3 @ BARCODE_12X4
ZZZ2 @ BARCODE_20X4
ZZZ4 @ BARCODE_10X10

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT7718W	1001 100x 98h

EC SM Bus4 address

Device	Address
BMA250E	0001 100X 18h

ME SM Bus address

Device	Address
NFC	0010 1000 28h

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	DGPU	CRT RT2168	NFC	TP	PCH	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	NECP388 +3VALW	X	V +3VALW	V +19V_VIN	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	NECP388 +3VS	V +3VGS	X	X	V +3VS	X	V +3VS	X	X	X	X	V +3VS	X
SMB_EC_CK4 SMB_EC_DA4	NECP388 +3VALW	X	X	X	X	X	X	X	X	X	X	X	V +3VS
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	X	V +3VS	X	X	X	X	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	V +3VS	X	X	X
SML1CLK SML1DATA	PCH +3VALW	X	X	X	V +3VS	X	X	V +3VS	X	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	*HIGH*	*HIGH*	*HIGH*	*HIGH*	*ON*	*ON*	*ON*	*ON*
S1(Power On Suspend)	*LOW*	*HIGH*	*HIGH*	*HIGH*	*ON*	*ON*	*ON*	*LOW*
S3 (Suspend to RAM)	*LOW*	*LOW*	*HIGH*	*HIGH*	*ON*	*ON*	*OFF*	*OFF*
S4 (Suspend to Disk)	*LOW*	*LOW*	*LOW*	*HIGH*	*ON*	*OFF*	*OFF*	*OFF*
S5 (Soft OFF)	*LOW*	*LOW*	*LOW*	*LOW*	*ON*	*OFF*	*OFF*	*OFF*

USB 2.0 Port Table

Port	External USB Port
1	USB2/3 MB(IO_Port1)
2	USB2/3 MB(IO_Port2)
3	FingerPrint(For E31)
4	USB2 IO Board(Charger)
5	Camera
6	CardReader IO Board(Right)
7	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	USB2/3 MB(IO_Port1)
2	USB2/3 MB(IO_Port2)
3	
4	
5	
6	

PCIE Port Table

Port	Lane	
1	1	
2	2	GPU
3	3	
4	4	
5		LAN
6		NGFF WLAN+BT
7		
8		
9		
10		

SATA Port Table

Port	
0	HDD
1	

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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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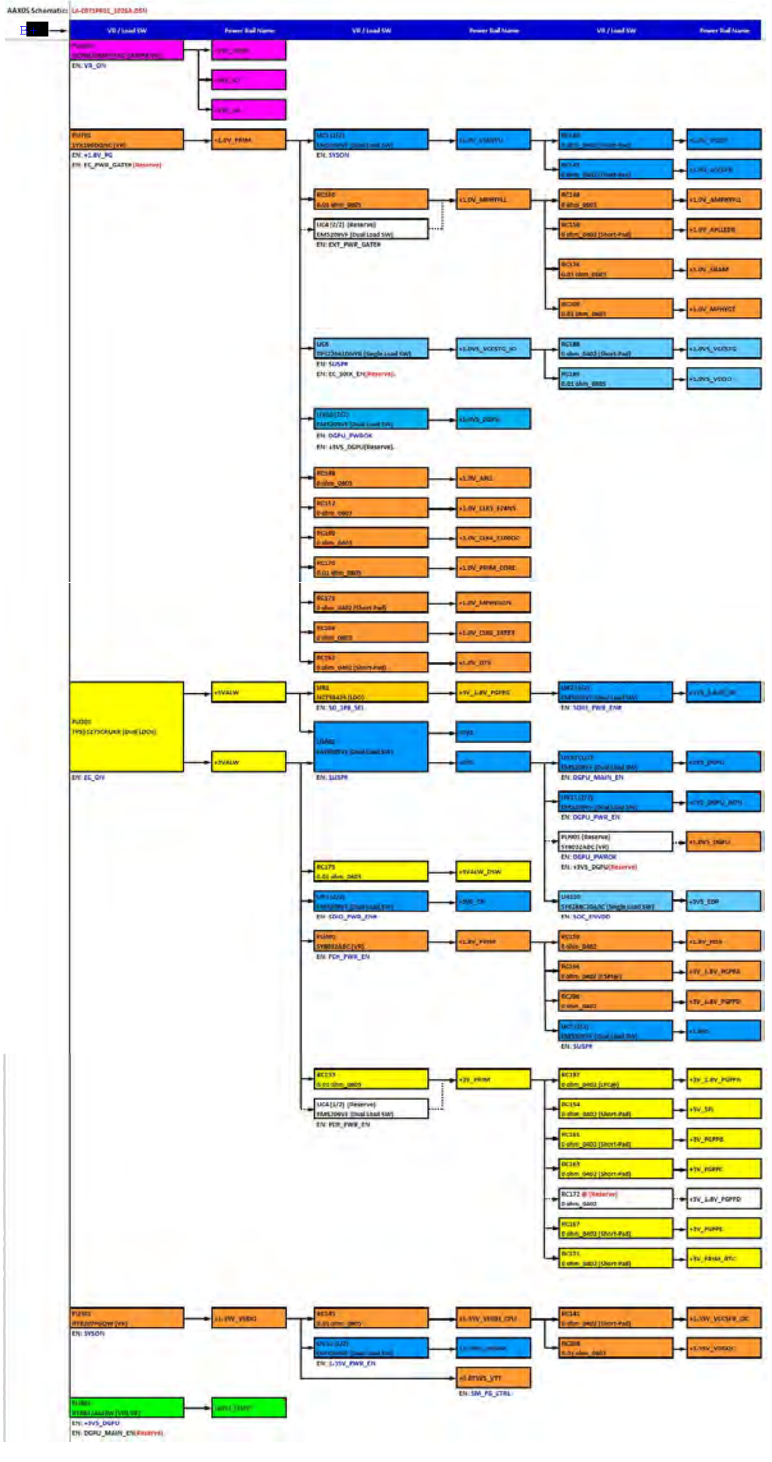
Title: Notes List
Size: C
Document Number: LA-C311P
Rev: 0.3

BIVS3/ VE3 -PowerMap_SKL-U22_DDR3L_Volume_NON CS]



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Issued Date	2013/11/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Power MAP**

Size | Document Number | Rev 0.1

[AAX05-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]

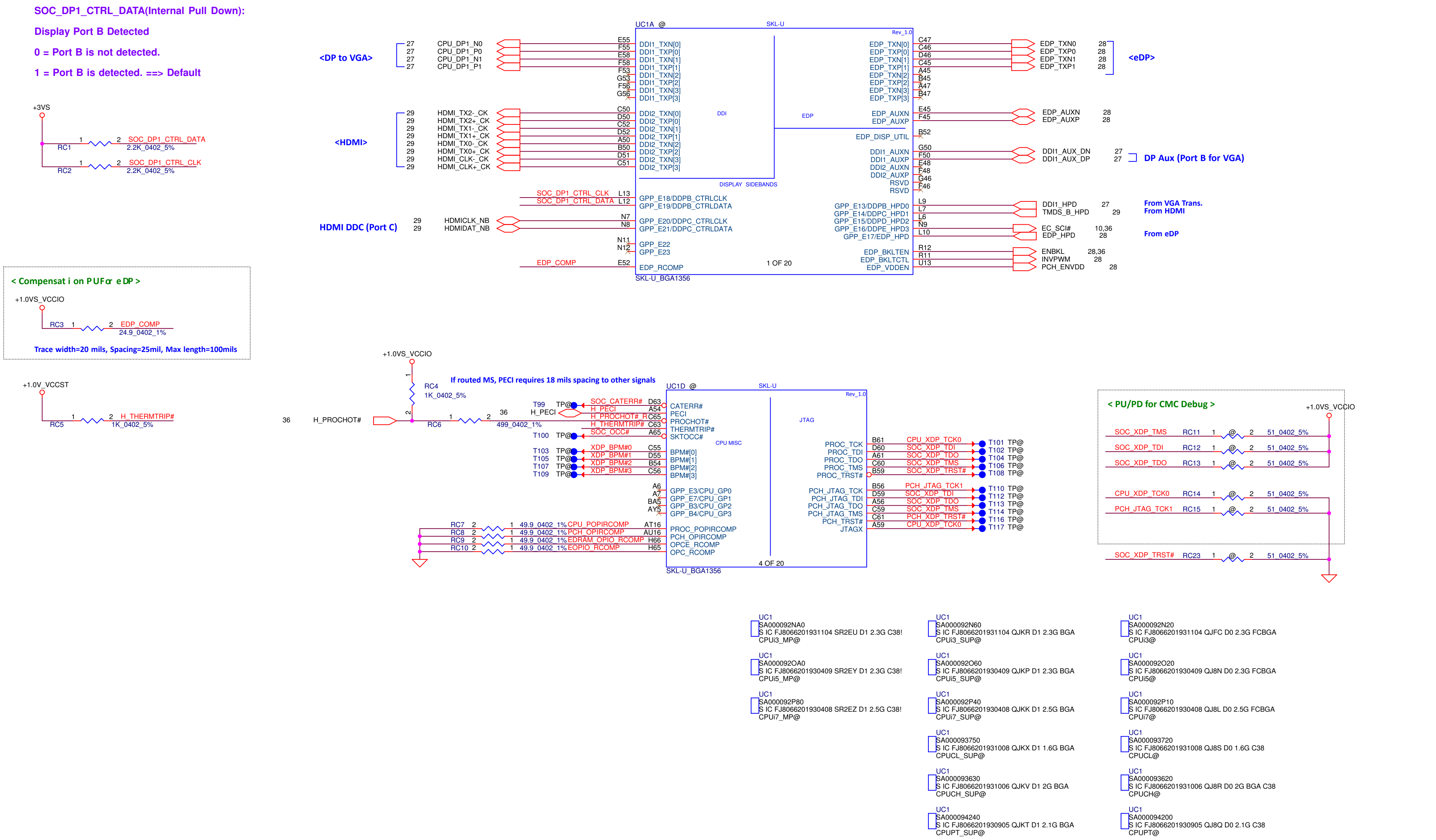
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: *Power Sequence*

Size | Document Number | Rev 0.1

Date: Friday, August 07, 2015 |



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

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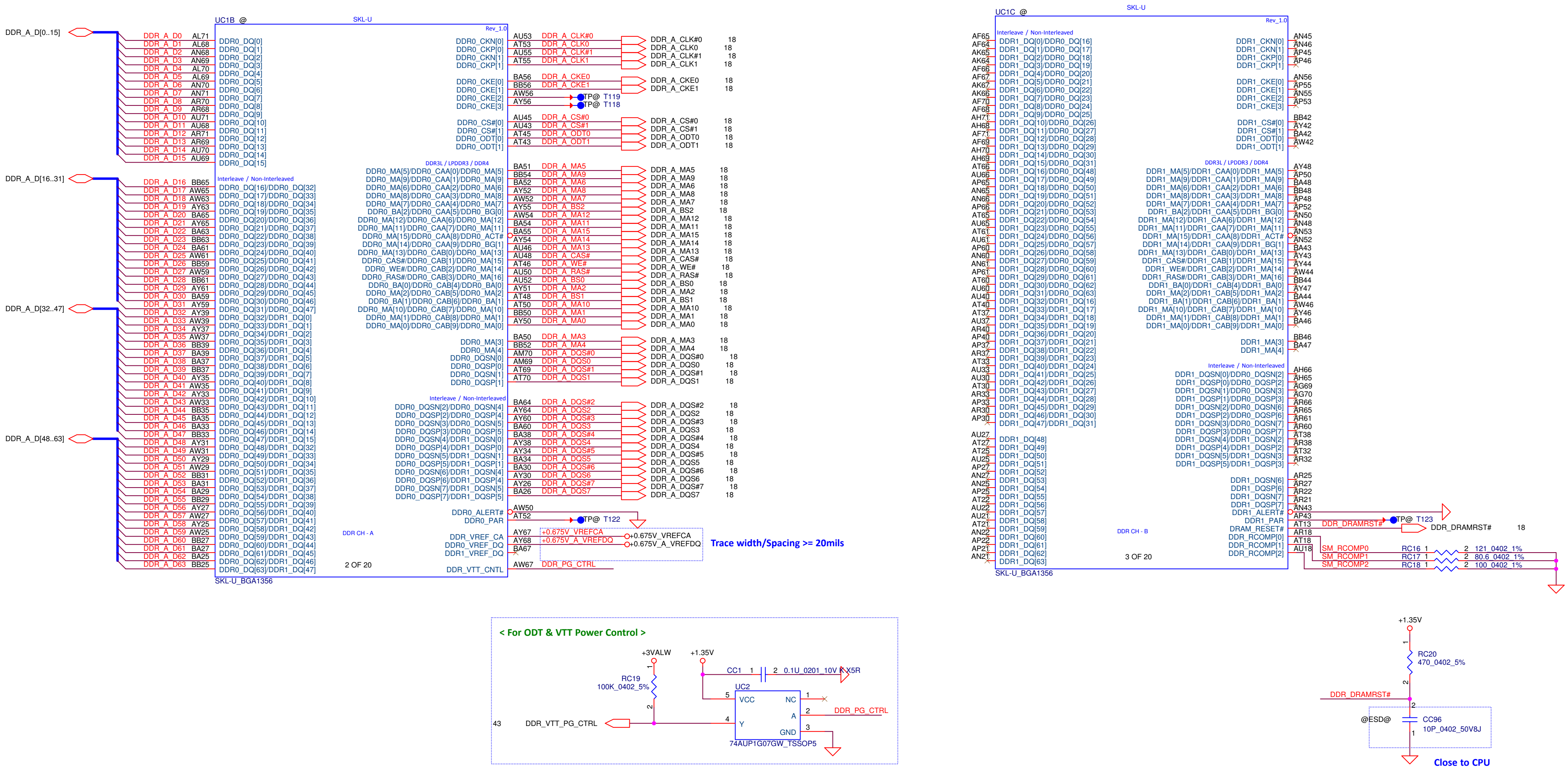
Title: **SKL-U(1/12)DDI,EDP,MISC,CMC**

Size: Custom | Document Number: **LA-C851P** | Rev: 0.1

Interleaved Memory



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: SKL-U(2/12)DDR3L

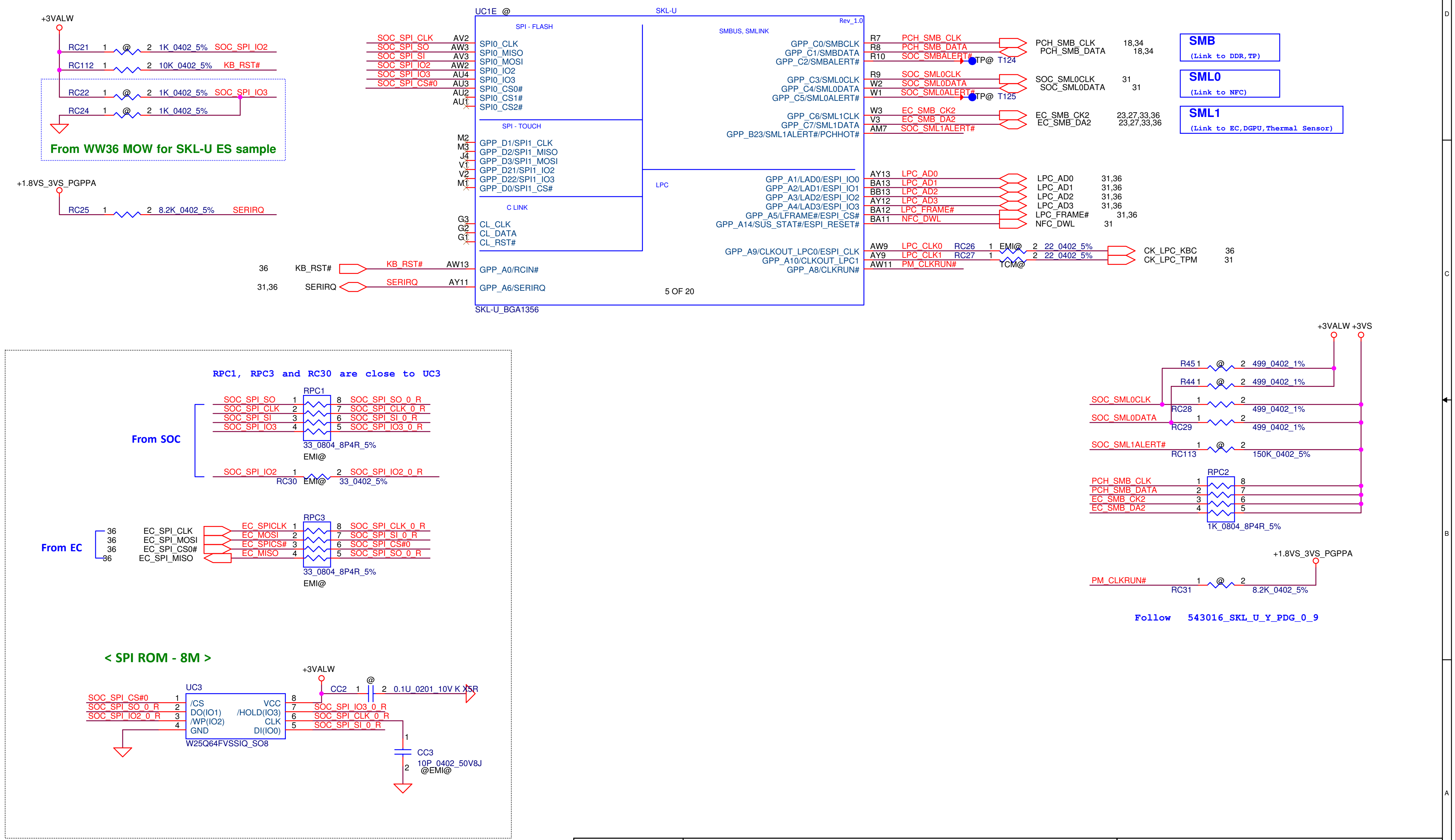
Size: Custom | Document Number: LA-D061P | Rev: 0.1

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC



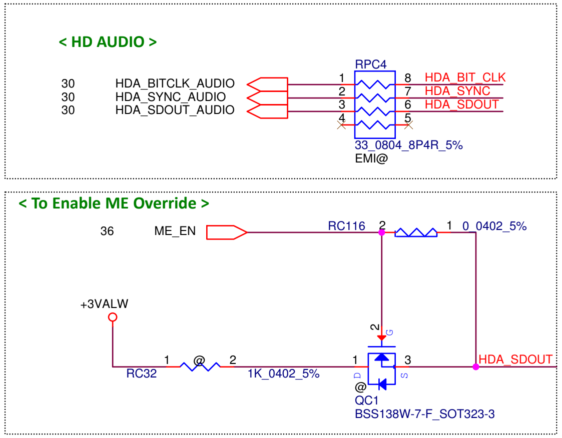
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

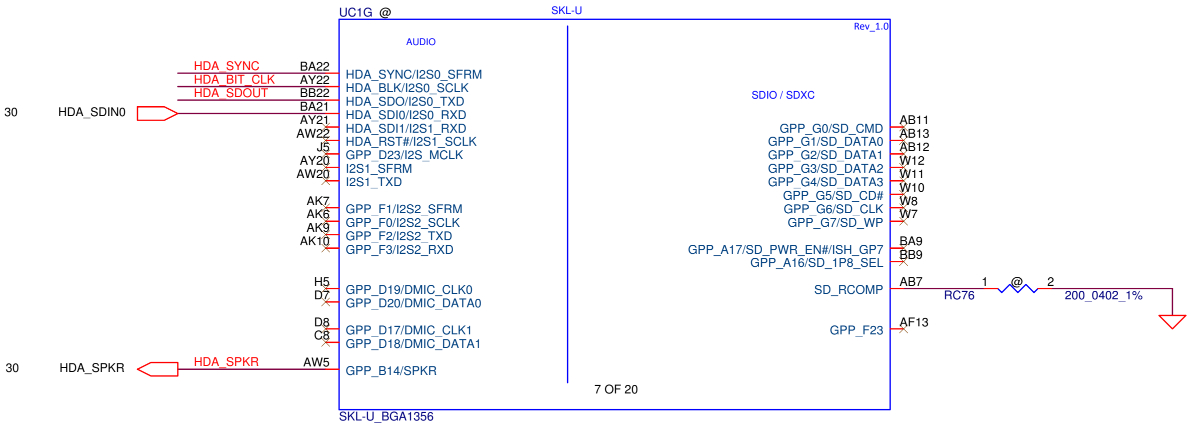
Compal Electronics, Inc.

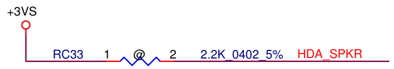
Title: **SKL-U(3/12)SPI,SMB,LPC,ESPI**

Size: Custom | Document Number: **LA-D061P** | Rev: 0.1

Date: Friday, August 07, 2015 |





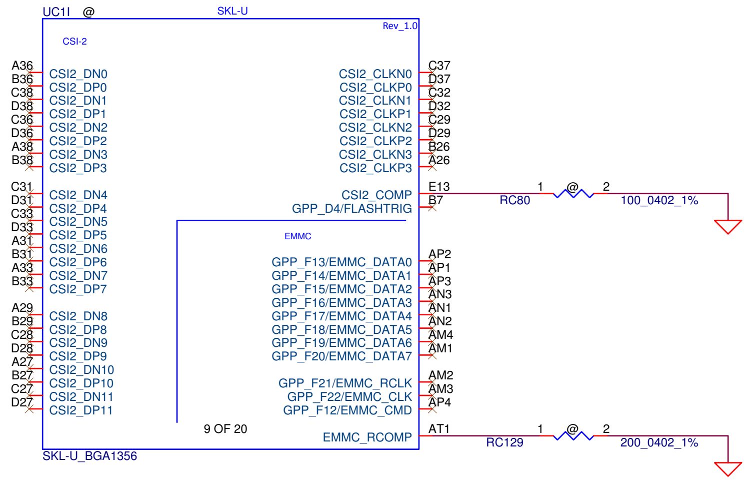


SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

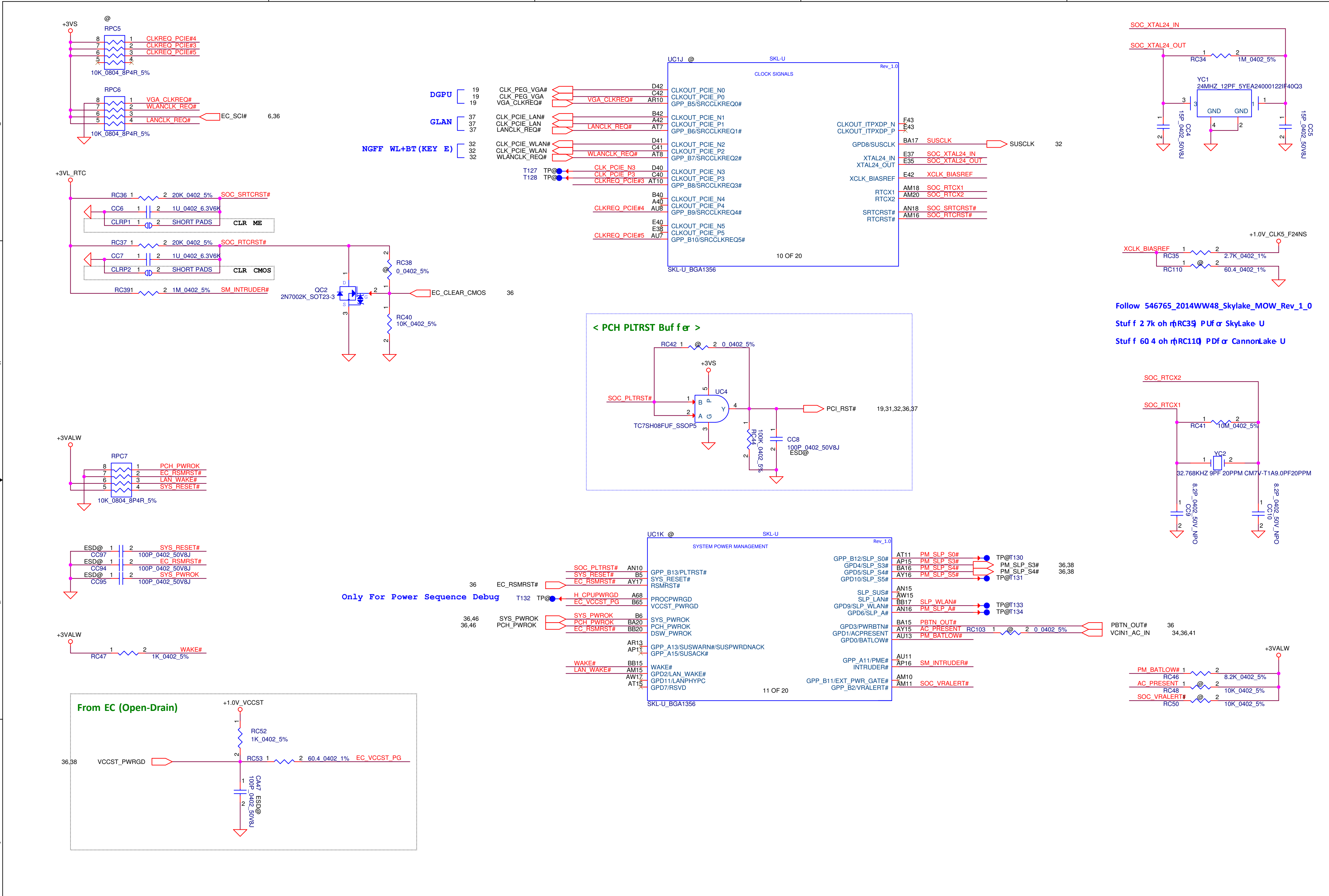


Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(4/12)HDA,EMMC,SDIO,CSI2**

Size: Custom | Document Number: **LA-D061P** | Rev: 0.1



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Title: **SKL-U(5/12)CLK,PM,GPIO**

Size: Custom | Document Number: **LA-D061P** | Rev: 0.1

Date: Friday, August 07, 2015 | Sheet 10 of 52

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

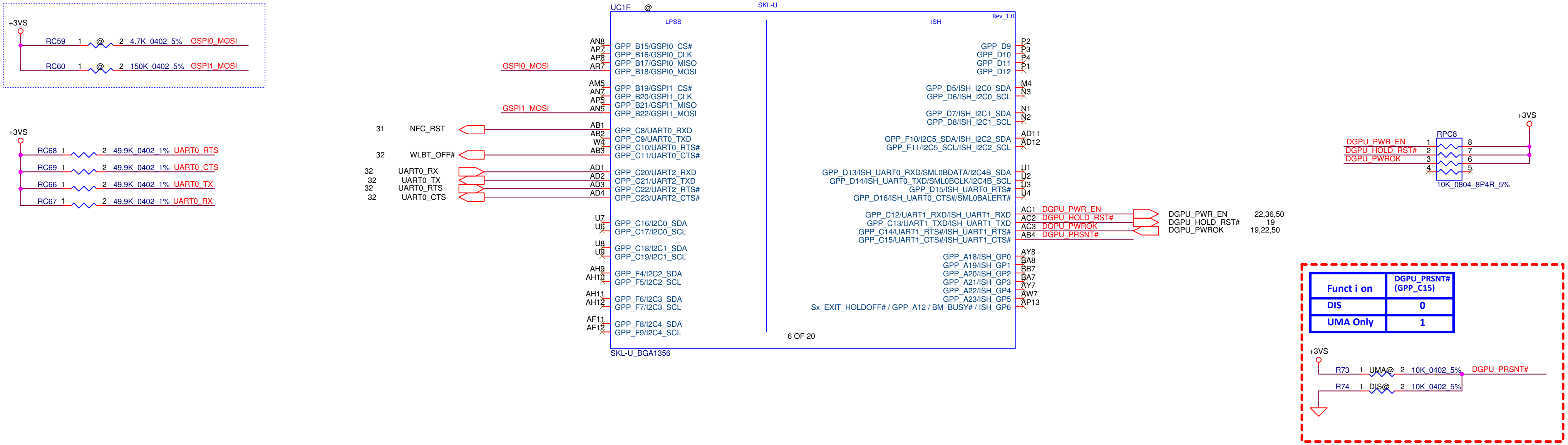
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode ==> Default

1 = LPC Mode



Function	DGPU_PRSNT# (GPP_C15)
DIS	0
UMA Only	1

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(6/12)GPIO,I2C,GSPI**

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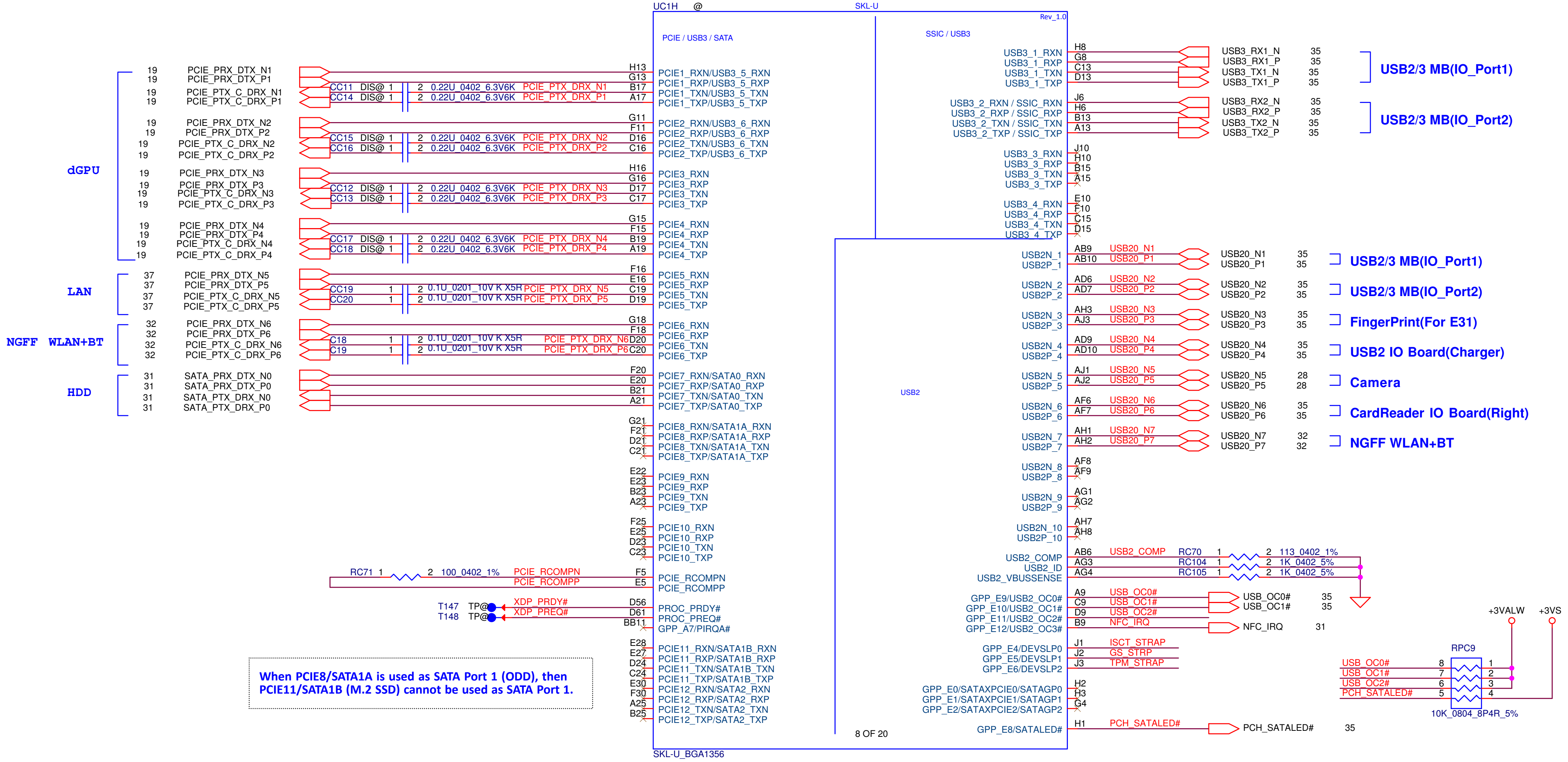
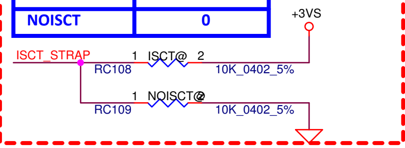
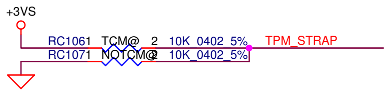


When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

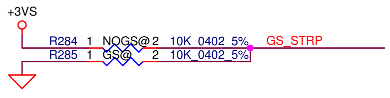
Funct i on	GPIO13
ISCT	1
NOISCT	0



Funct i on	GPIO38
TCM	1
No TCM	0



Funct i on	GPIO44
No G-Sensor	1
G-Sensor	0

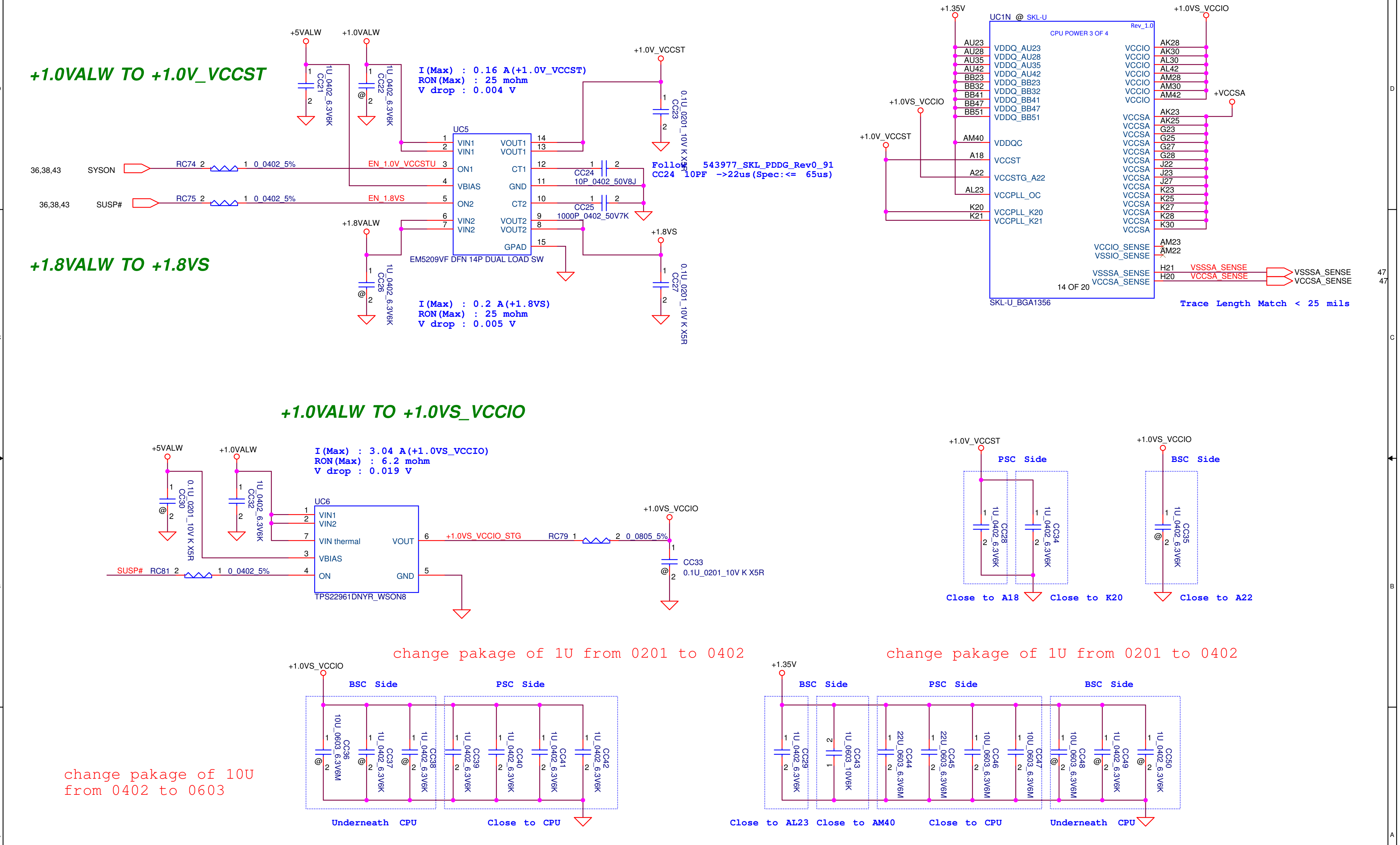


Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(7/12)PCIE,USB,SATA**

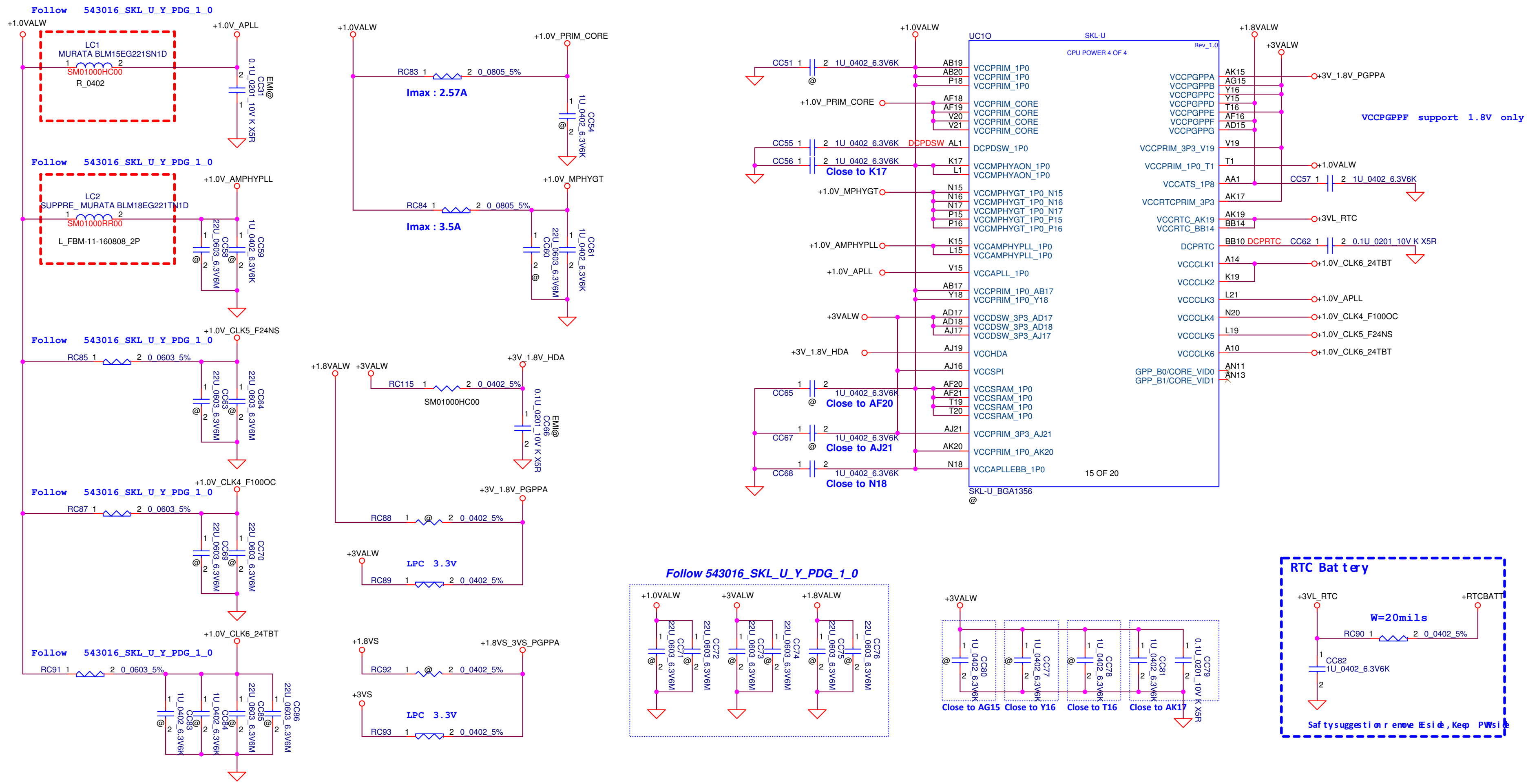
Size: Custom | Document Number: **LA-D061P** | Rev: 0.1



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2014/05/19	Deciphered Date	2015/12/31	Title: SKL-U(8/12)Power

Size: Custom | Document Number: LA-D061P | Rev: 0.1

Date: Friday, August 07, 2015 |

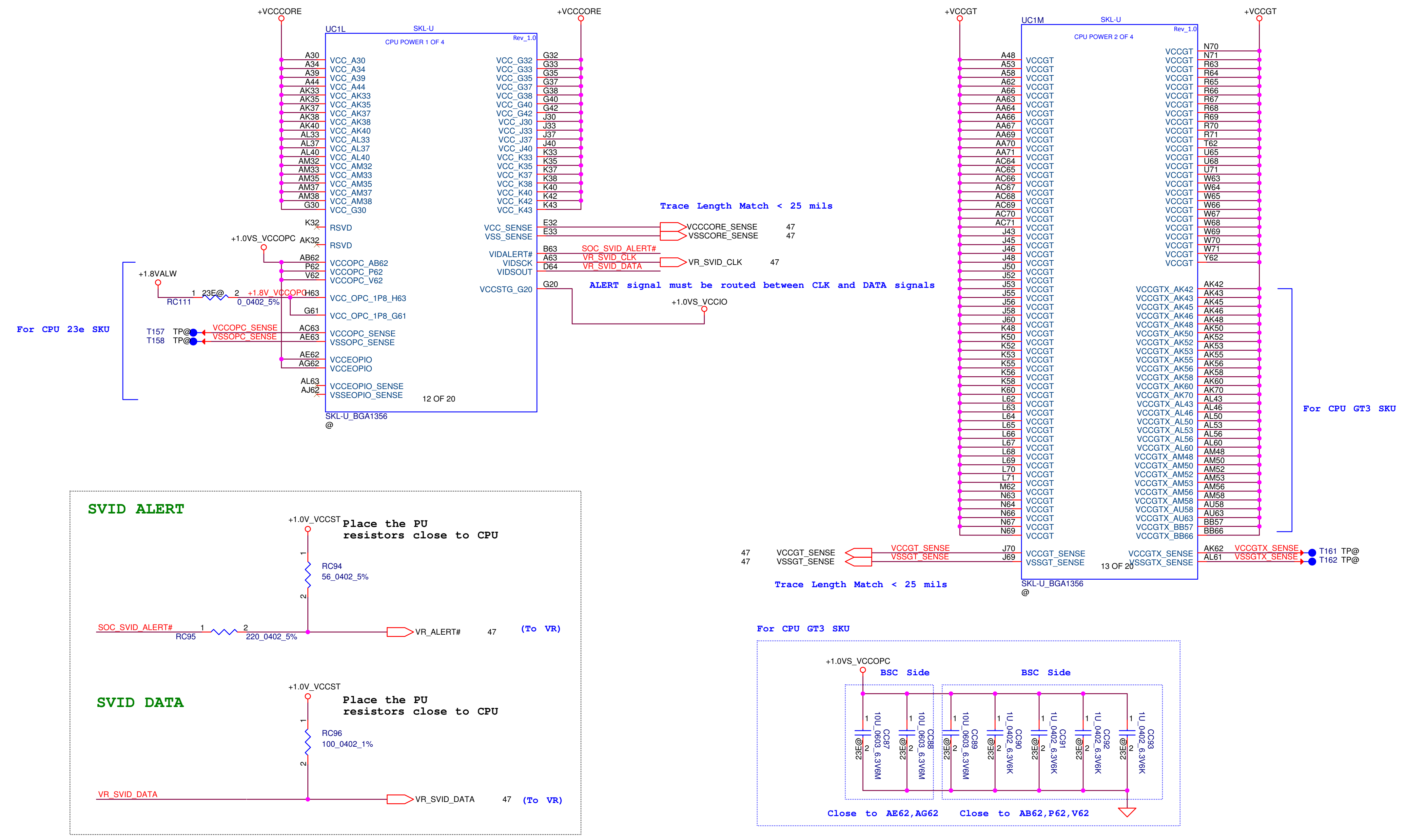


Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(9/12)Power**

Size: Custom | Document Number: **LA-D061P** | Rev: 0.1



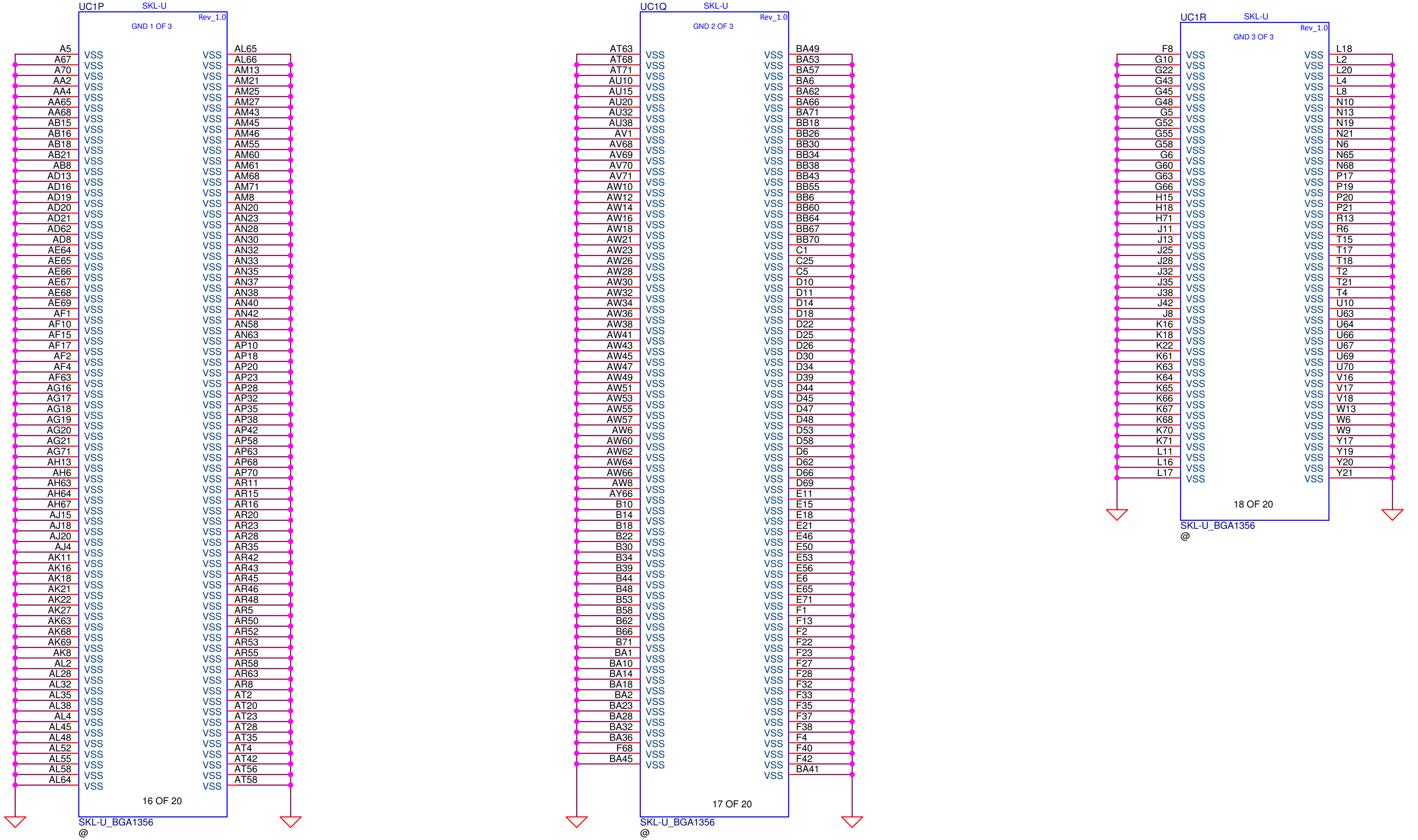
Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(10/12)Power,SVID**

Size: Custom | Document Number: **LA-D061P** | Rev: 0.1

Date: Friday, August 07, 2015 |

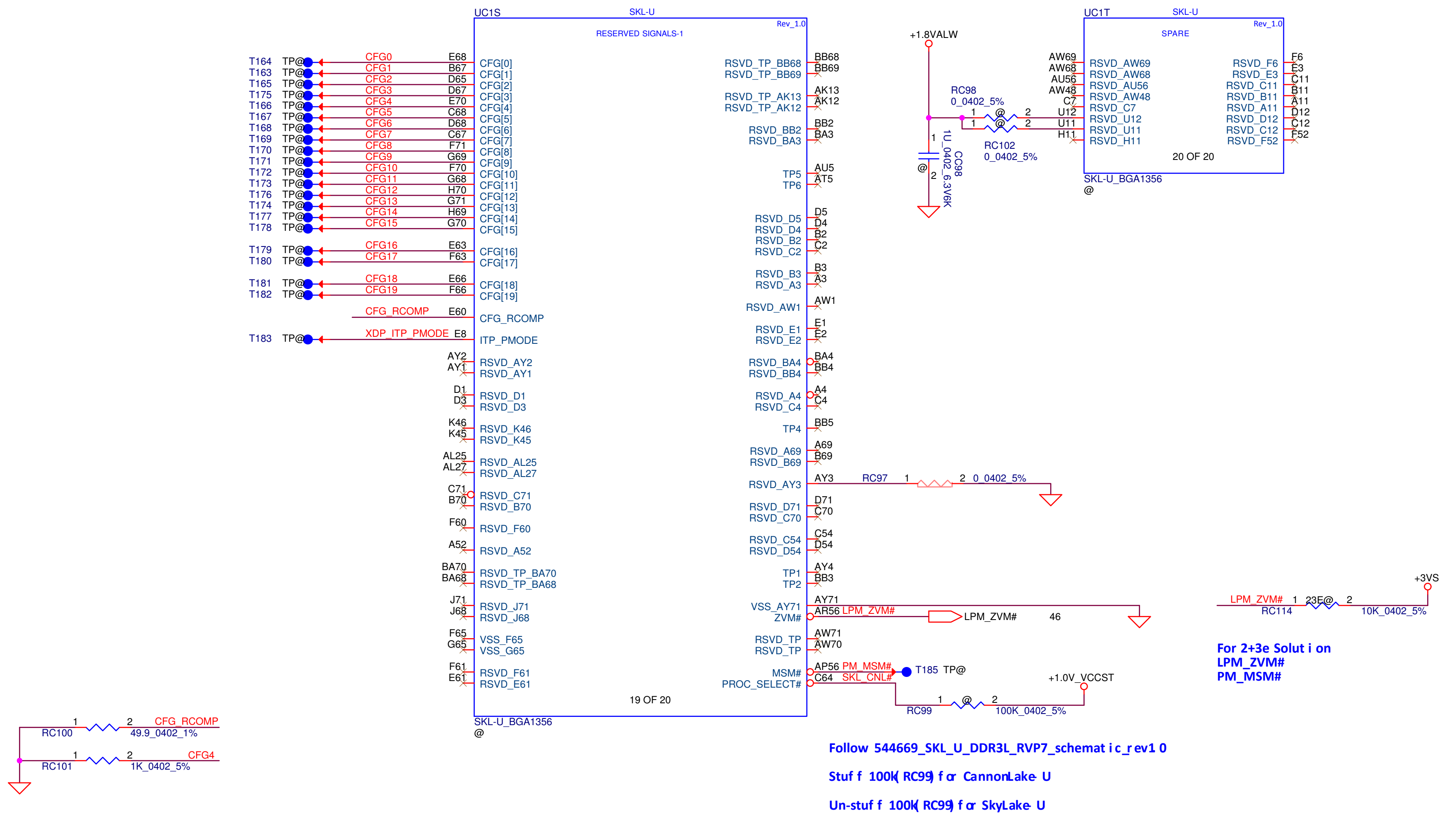


Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(11/12)GND**

Size: Custom | Document Number: **LA-D061P** | Rev: 0.1



For 2+3e Solution
LPM_ZVM#
PM_MSM#

Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1 0

Stuff 100K(RC99) for CannonLake-U

Un-stuff 100K(RC99) for SkyLake-U

Display Port Presence Strap

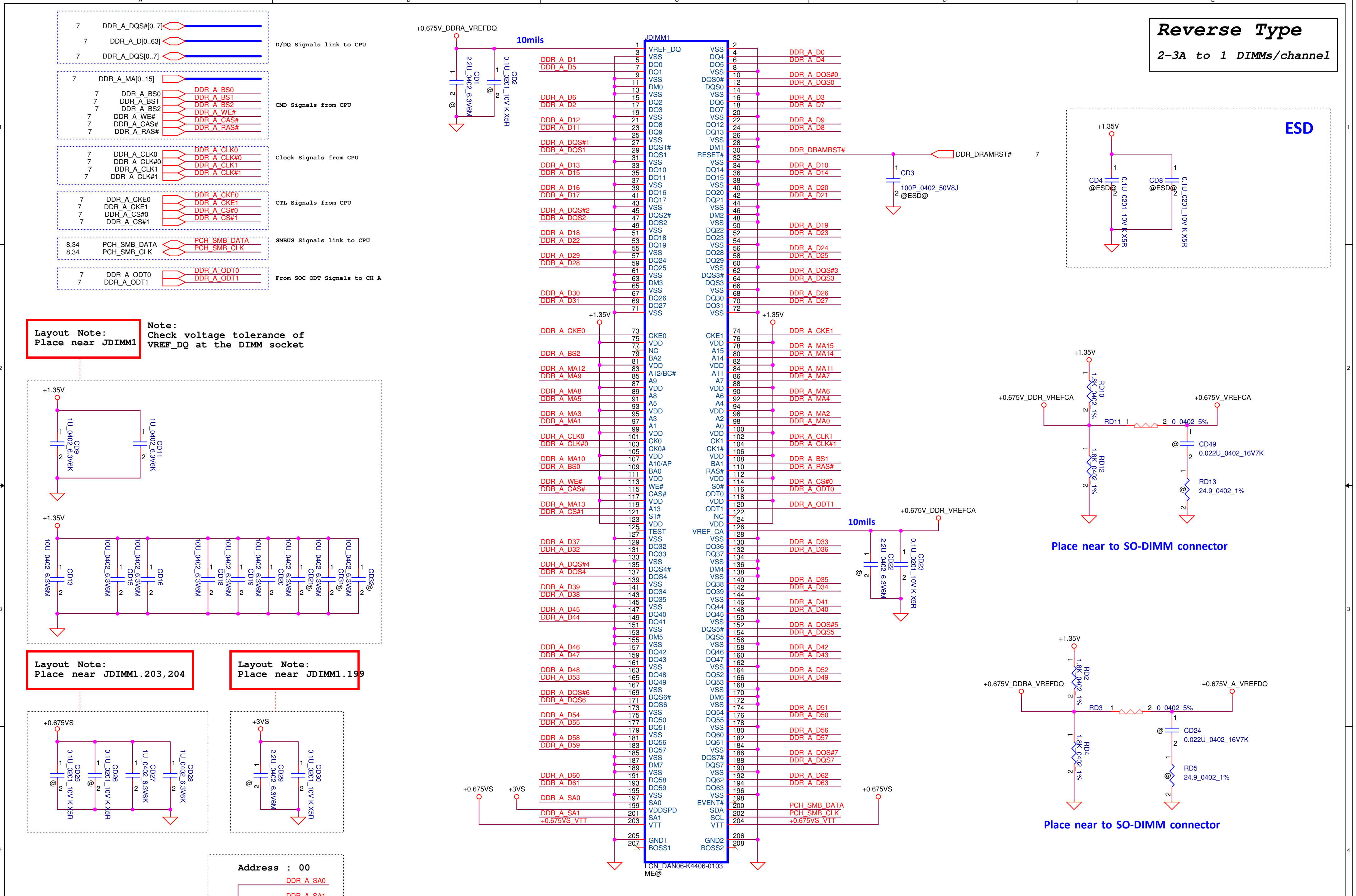
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **SKL-U(12/12)CFG,RSVD**

Size: Custom | Document Number: **LA-D061P** | Rev: 0.1



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Issued Date	2014/05/19	Deciphered Date 2015/12/31	DDR3L DIMMA

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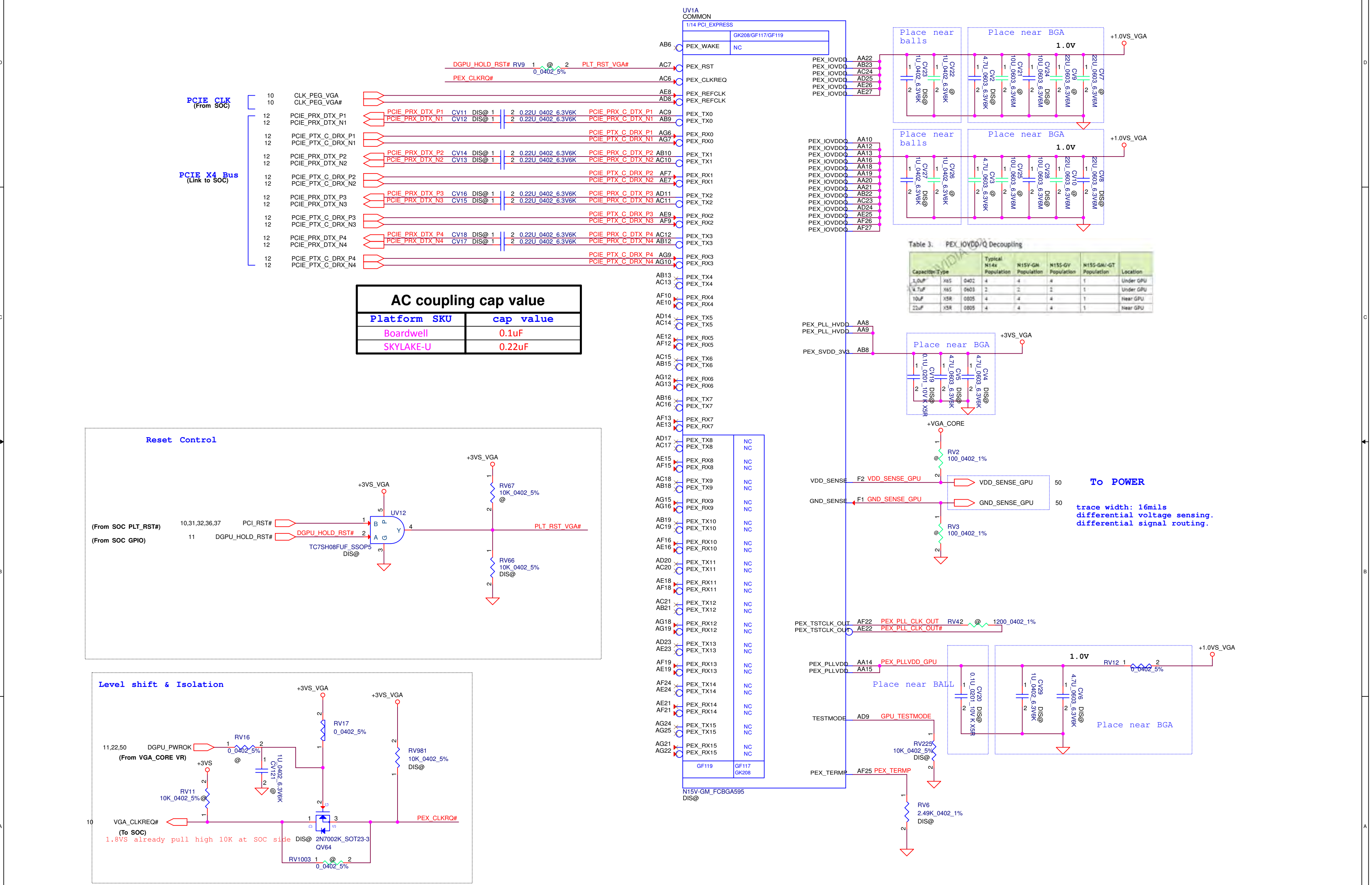
Date: Friday, August 07, 2015 | Sheet 18 of 52



AC coupling cap value

Platform SKU	cap value
Boardwell	0.1uF
SKYLAKE-U	0.22uF

Table 3. PEX_IOVDD/Q Decoupling

Capacitor Type			Typical N14x Population	N15V-GM Population	N15S-GV Population	N15S-GM/-GT Population	Location
1.0uF	X6S	0402	4	4	4	1	Under GPU
4.7uF	X6S	0603	2	2	2	1	Under GPU
10uF	X5R	0805	4	4	4	1	Near GPU
22uF	X5R	0805	4	4	4	1	Near GPU

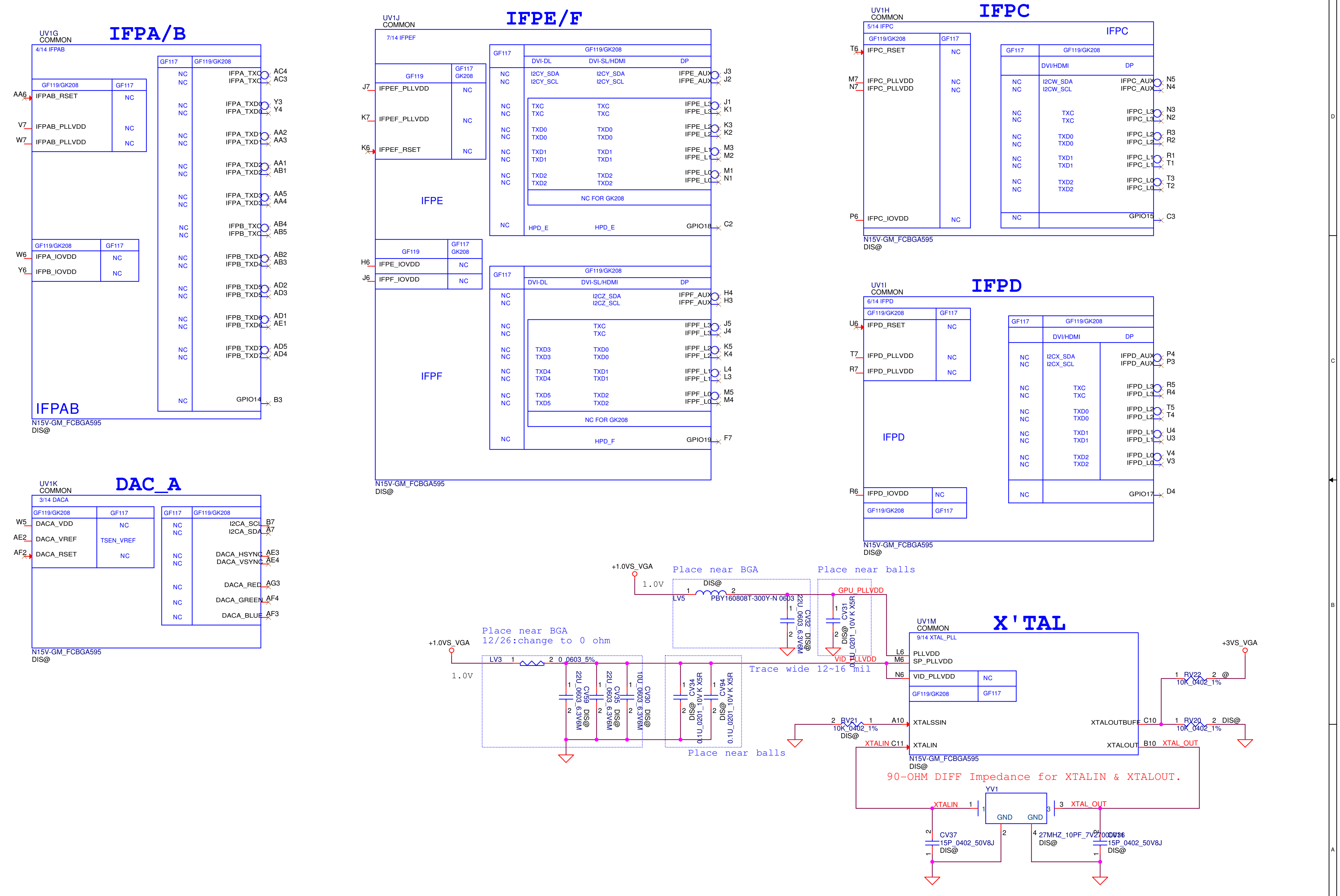
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: NV(1/5)-PCIE

Size: C | Document Number: LA-D061P | Rev: 0.3

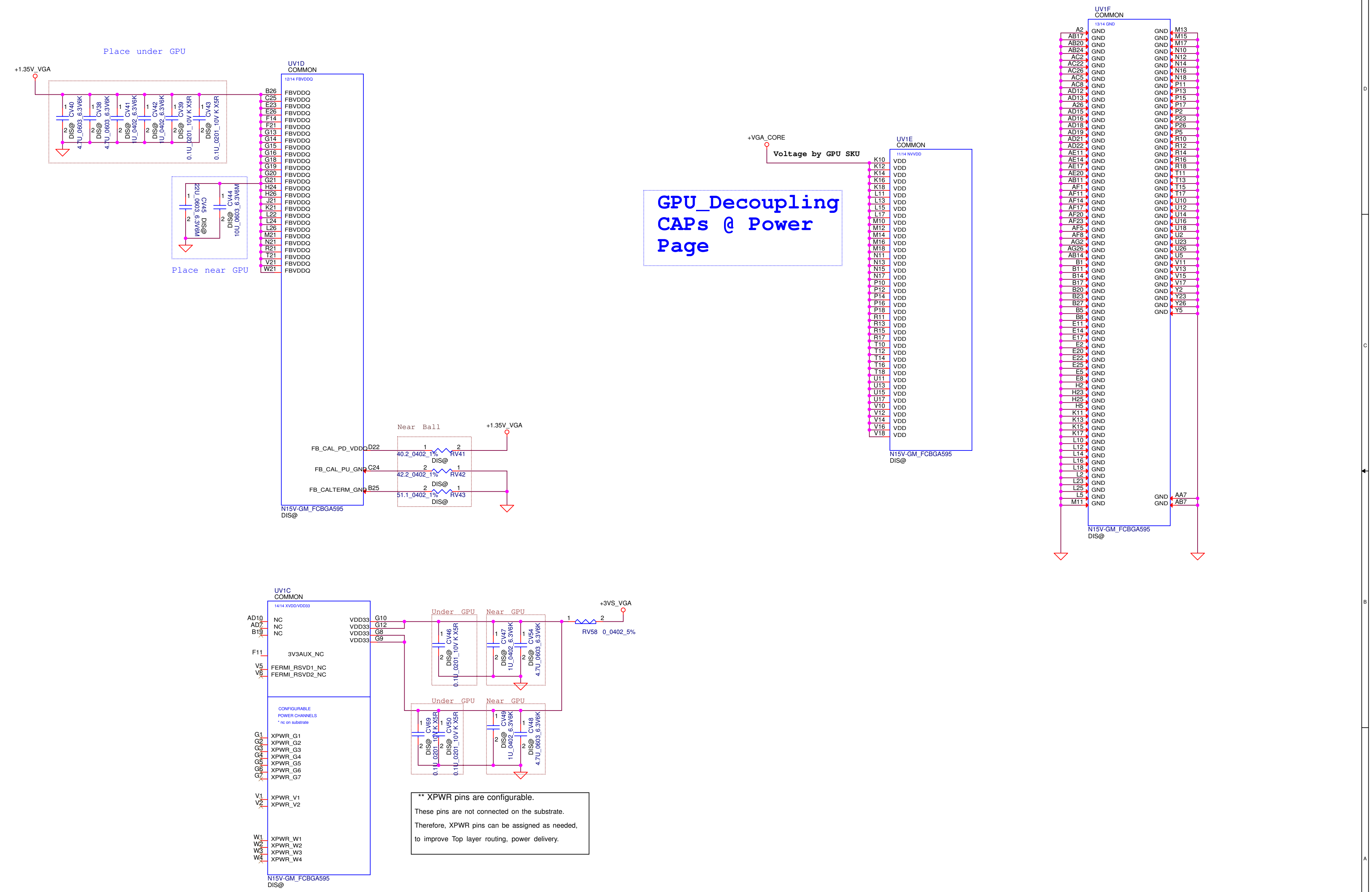
Date: Friday, August 07, 2015



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title: NV(2/5)-IFP ABCDEF DAC XTAL

Size	Document Number	Rev
Custom	LA-D061P	0.3

Date: Friday, August 07, 2015 Sheet 20 of 52



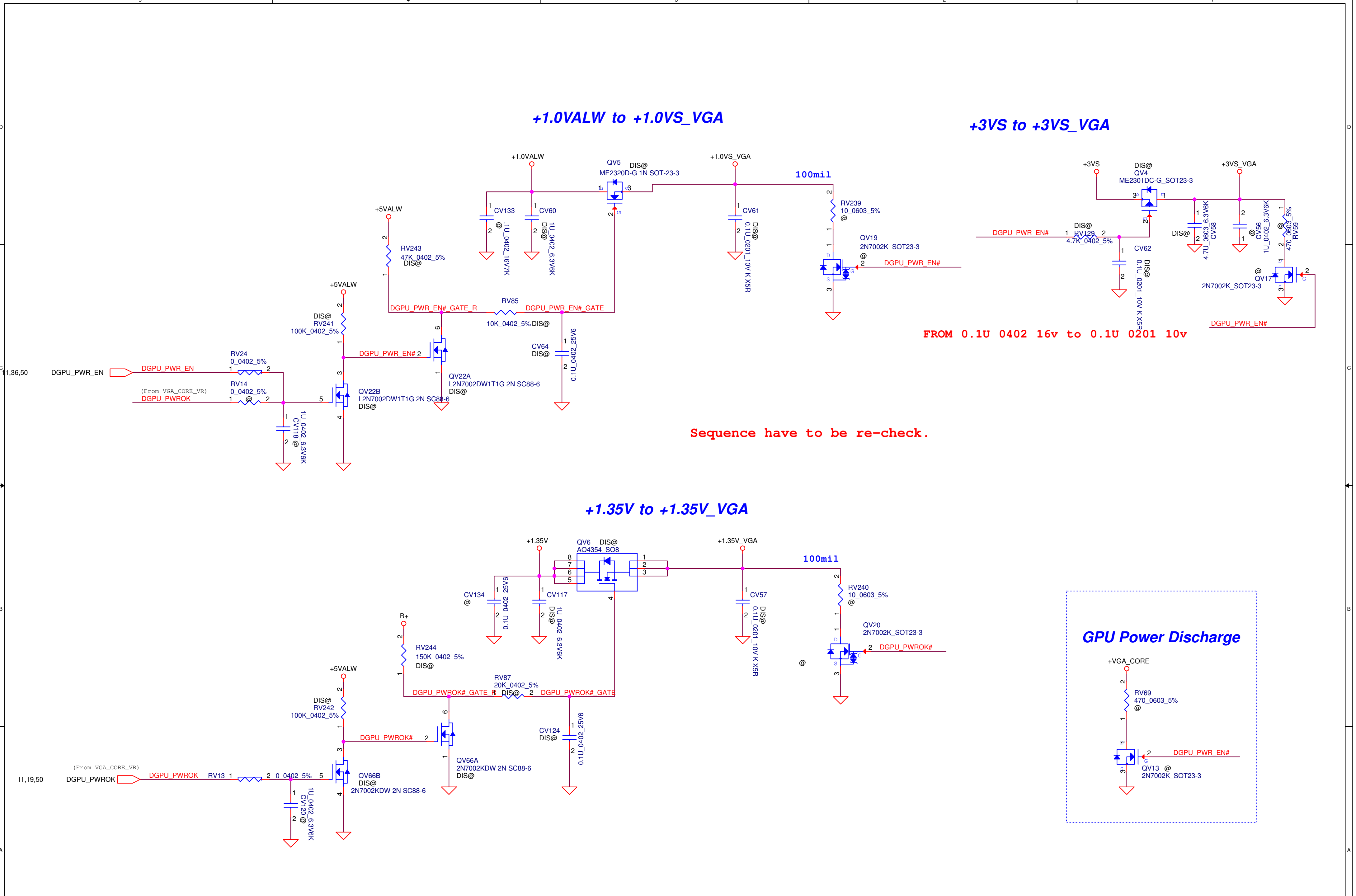
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

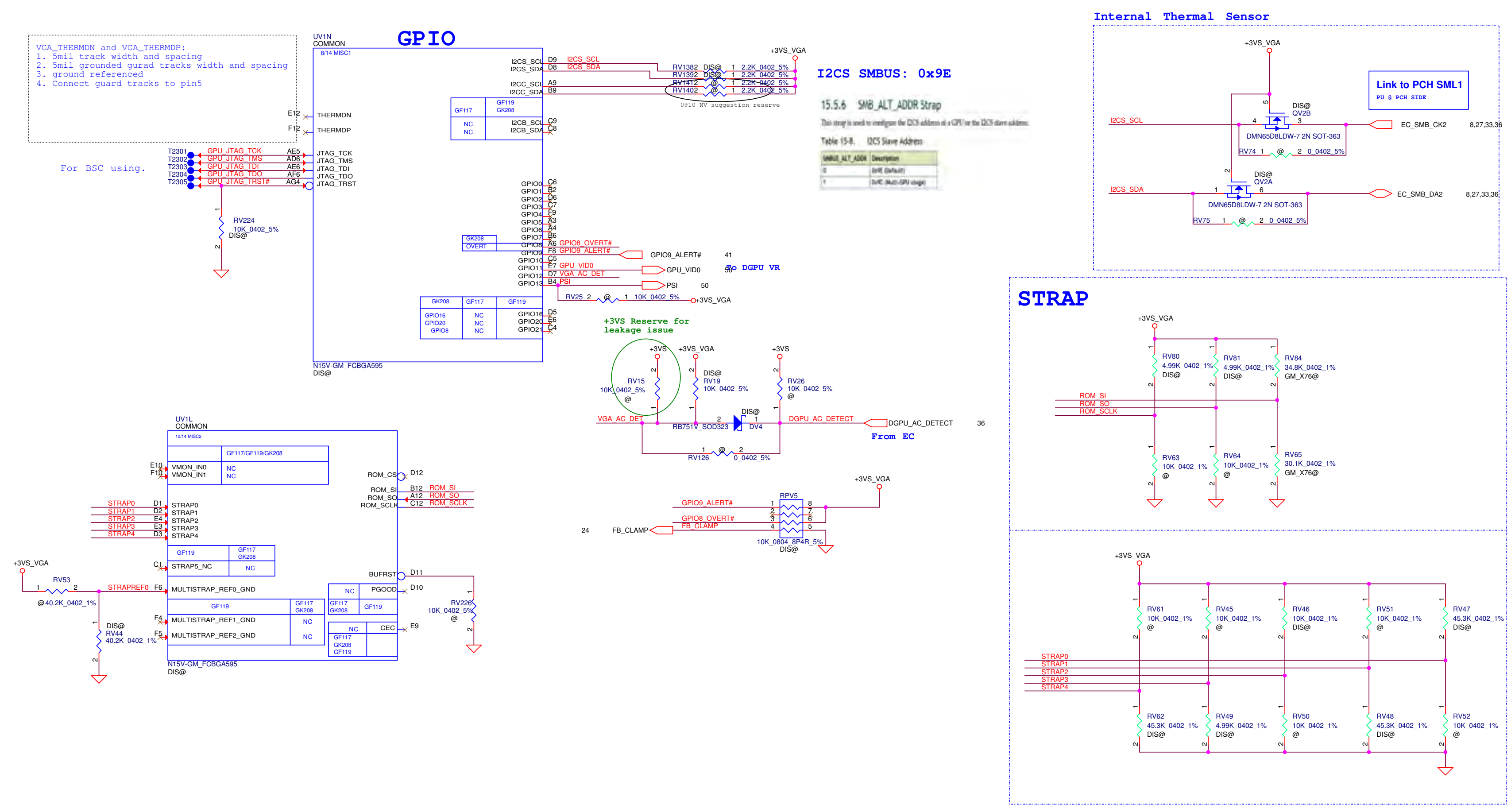
Title: **NV(3/5)-POWER**

Size: C | Document Number: **LA-D061P** | Rev: 0.3

Date: Friday, August 07, 2015 | Sheet 21 of 52



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2011/07/15	Deciphered Date	2012/07/15	Title: DGPU_DC/DC Interface
				Size / Document Number / Rev 0.3
				Date: Friday, August 07, 2015 Sheet 22 of 52

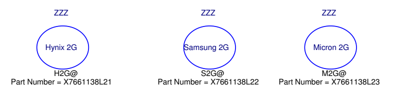


N16V-GM Binary Staps

[illegible]	
Item	N16V-GM-S
Device ID	0X1299
Package	GB2-64
Internal P/N	GK208-620,28nm
ROM_SI	Refer to N16x_RAM_Straps table
ROM_SO	0x8, 5K pull up for Optimus
ROM_SCLK	0x1000,0x8, 4.99Kohm pull up
Strap0	User Strap, 0xf, 45kohm pull up
Strap1	[illegible]
Strap2	Device_ID, 0x1001_ 10Kohm pull UP
Strap3	0x0 for Optimus, 5kohm pull low
Strap4	0x0111, 45kohm pull down(PCIE_SPEED_CHANGE=1)
Open_VRG SKU	Config 8(PSI not supported)
NVVDD Boot Voltage	0.9V

GPU	VRAM Vendor	Type	FBVDO/FBVDDQ	Memory Density	Configuration	VRAM P/N	Max Speed CLK	D/C Mini	Die-Revsion	RAM_CFG	ROM_SI	Status
N16V-GM-S	DDR3L											
	Hynix	DDR3L	1.35V/1.35V	128MX16	Single Rank or Single Rank Stuffing for Dual Rank	H5TC2G63FFR-11C	900Mhz	NA	F-Die	0xB	PU 20K	Production ready
	Micron	DDR3L	1.35V/1.35V	128MX16		MT41J128M16JT-093G:K	900Mhz	1322	K-Die	0X8	PU 4.99K	Production ready
	Samsung	DDR3L	1.35V/1.35V	128MX16		K4W2G1646Q-BC1A	900Mhz	NA	Q-Die	0X7	PD 45.3K	Production ready
	Hynix	DDR3L	1.35V/1.35V	256MX16		H5TC4G63CFR-N0C	900Mhz	NA	C-Die	0X0	PD 4.99K	Production ready
	Micron	DDR3L	1.35V/1.35V	256MX16		MT41J256M16HA-093G:E	900Mhz	NA	E-Die	0XD	PU 30.1K	Production ready
	Sansung	DDR3L	1.35V/1.35V	256MX16		K4W4G1646E-BC1A	900Mhz	NA	E-Die	0X2	PD 15K	Production ready

N16V-GM VRAM Straps: RAM_CFG (3..0) [ROM_SI (3..0)]



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Issued Date	2011/07/15	Deciphered Date 2012/07/15	Title: NV(4/5)-GPIO/Strap
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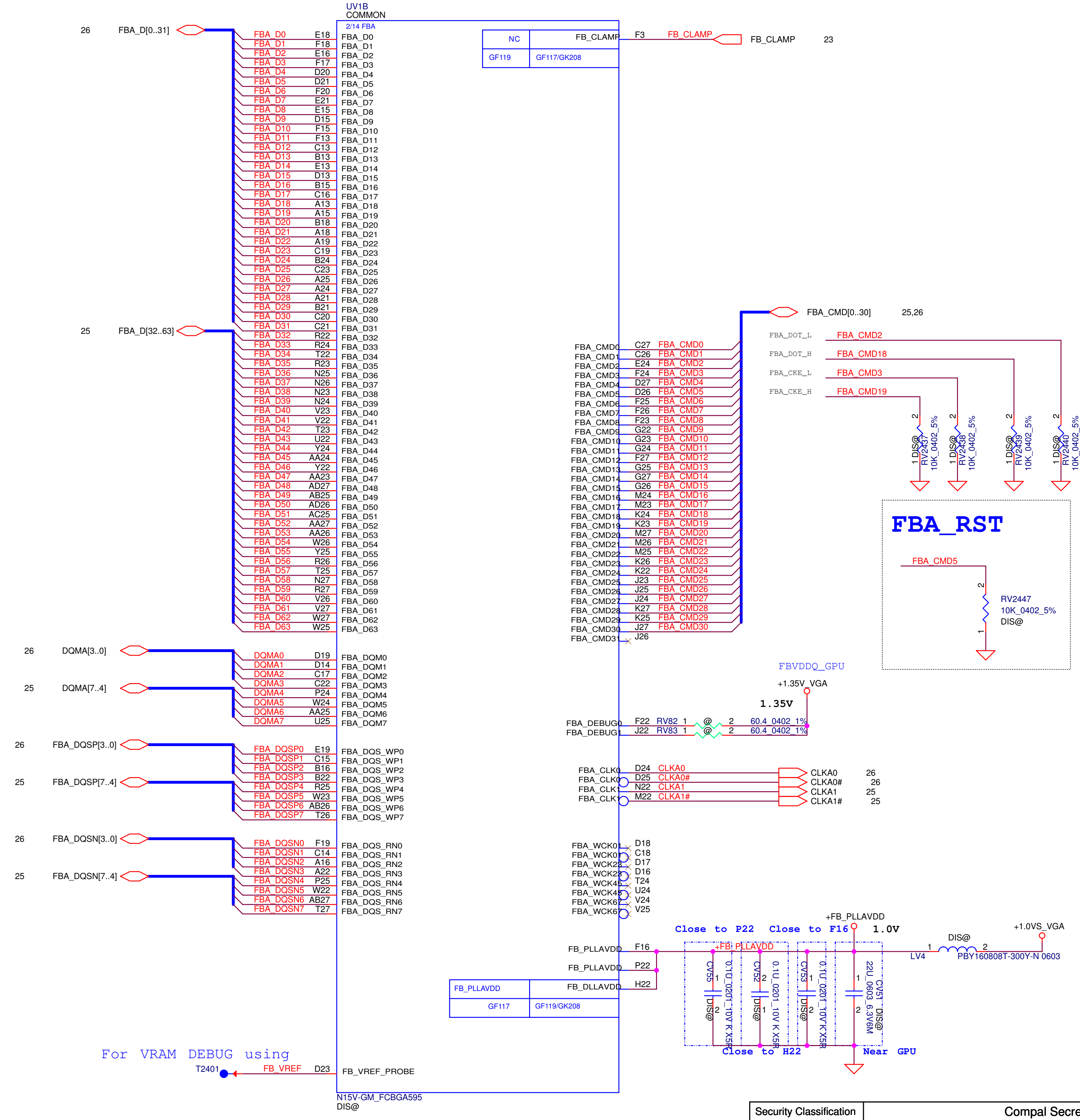
			Date: Friday, August 07, 2015; Sheet 23 of 52



6.1.10 Memory ODTx, CKEx, and RST Termination

DDR3 requires Memory Termination on CKEx, ODTx and Memory Reset (RST). Table 6-8 describes the required termination.

Table 6-8. Memory ODTx, CKEx, and RST Termination

DDR3 Command Bit	Default Pull-Down
ODTx	10 k
CKEx	10 k
RST	10 k
CS*	No Termination

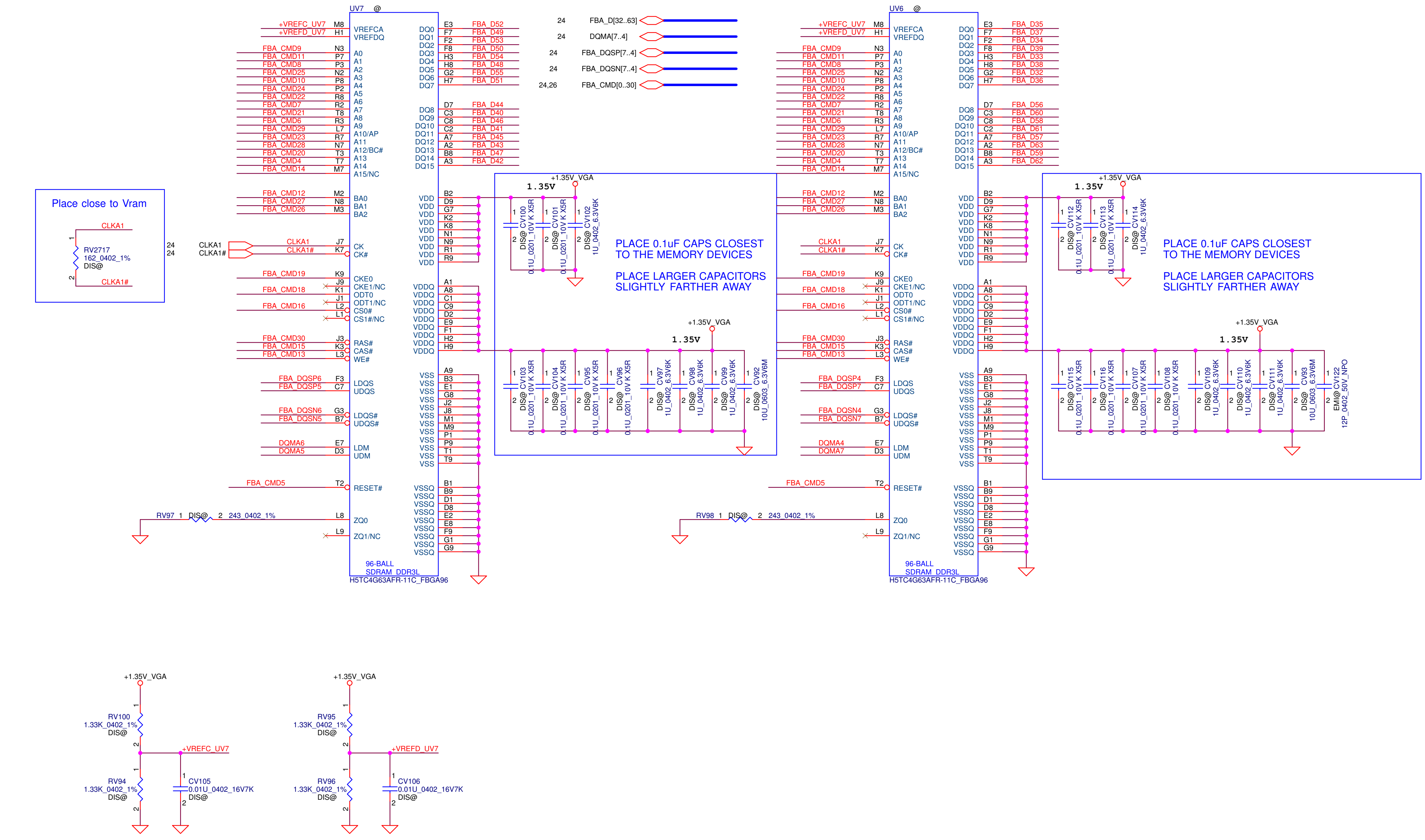
Security Classification	Compal Secret Data		
Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: **NV(2/5)-MEMORY FBA**

Size: Custom | Document Number: LA-D061P | Rev 0.3

Memory Partition A - Upper 32 bits [64..32]



Compal Electronics, Inc.

Title: *VRAM_DDR3_A Upper*

Size: Custom | Document Number: LA-D061P | Rev: 0.3

Memory Partition A - Lower 32 bits [31..0]

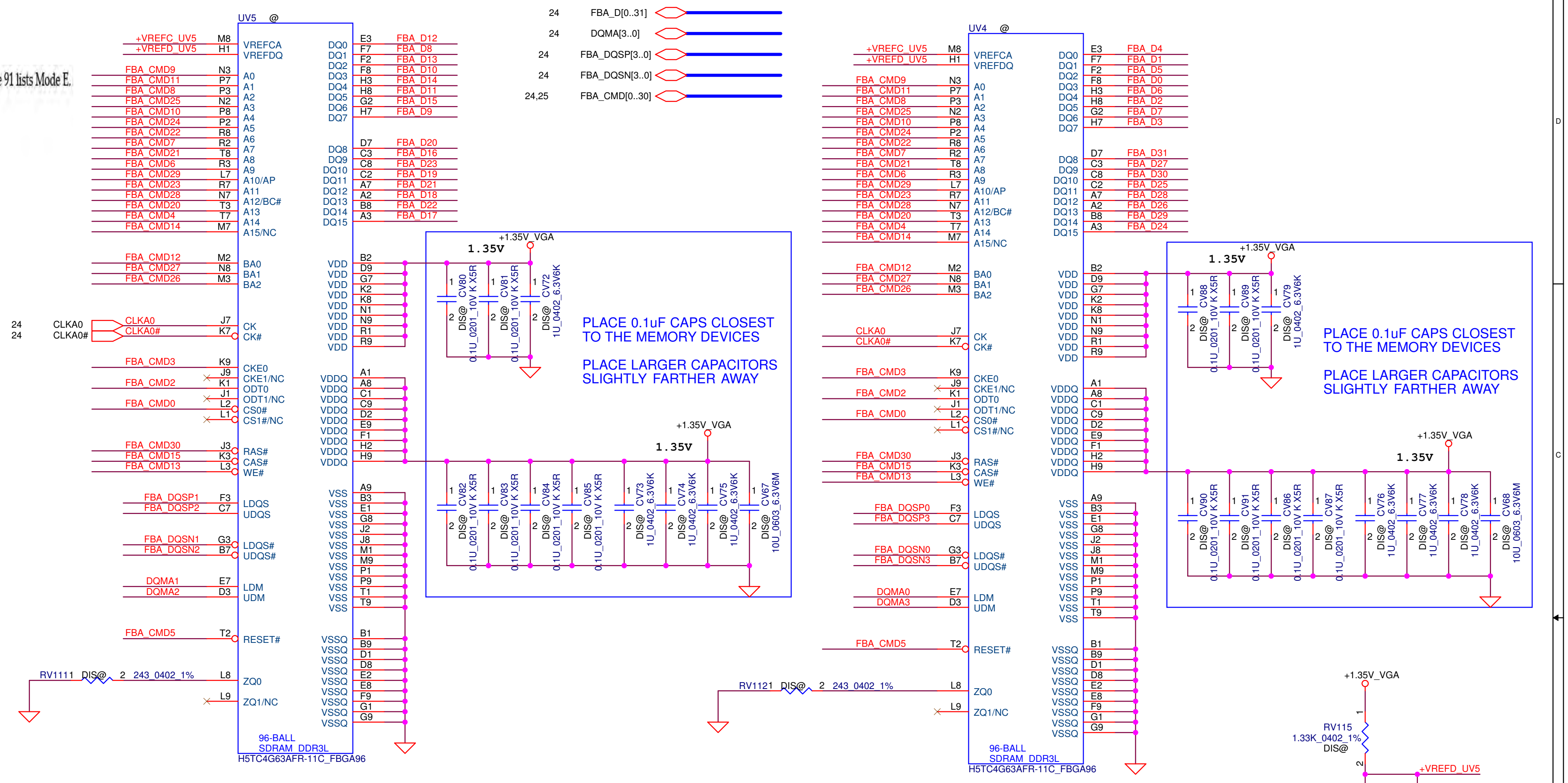
Table 6-3 lists the Mode D command mapping and Table 6-4 on page 91 lists Mode E.

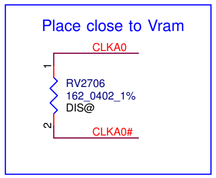
Table 6-3. Mode D Command Mapping

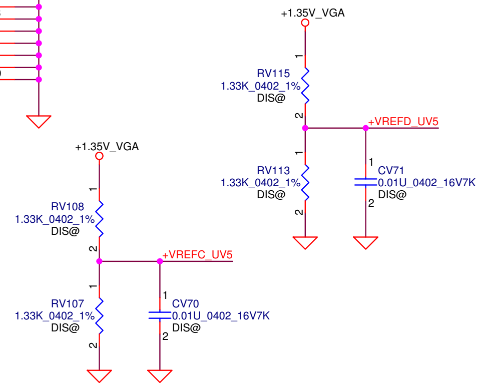
N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*

N15x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2B-64 package.
2. GPU debug pins; not connected to DRAM. See section 6.1.11







6.1.3 DDR3 Frame Buffer Command Mapping

N15x GPUs have generic FBx_CMD[35:0] pins that connect to the memory command/address pins. To optimize the layout for different memory types and packages, the GPUs support different mapping modes (Table 6-2). Choosing the best command mapping will help simplify layout and allow you to reduce layer count and/or area.

Table 6-2. Support Command Mapping by GPU Package

Packages	Supported CMD Mapping for DDR3	Benefits
GB2B-64 GB4B-128	D	Mode D is optimized for N15x using DDR3 memory in the BGA96 package and is supported for single rank designs. Using this mode will allow routing in four signal layers[1]. This compact layout offers a high level of symmetry allowing higher speeds without requiring termination.
GB2B-64 GB4B-128	E	Mode E is optimized for DDR3 dual rank designs.

Note: [1]Not including two additional layers for power planes.

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Issued Date	2011/07/15	Deciphered Date	2012/07/15

Compal Electronics, Inc.

Title: VRAM_DDR3_A Lower

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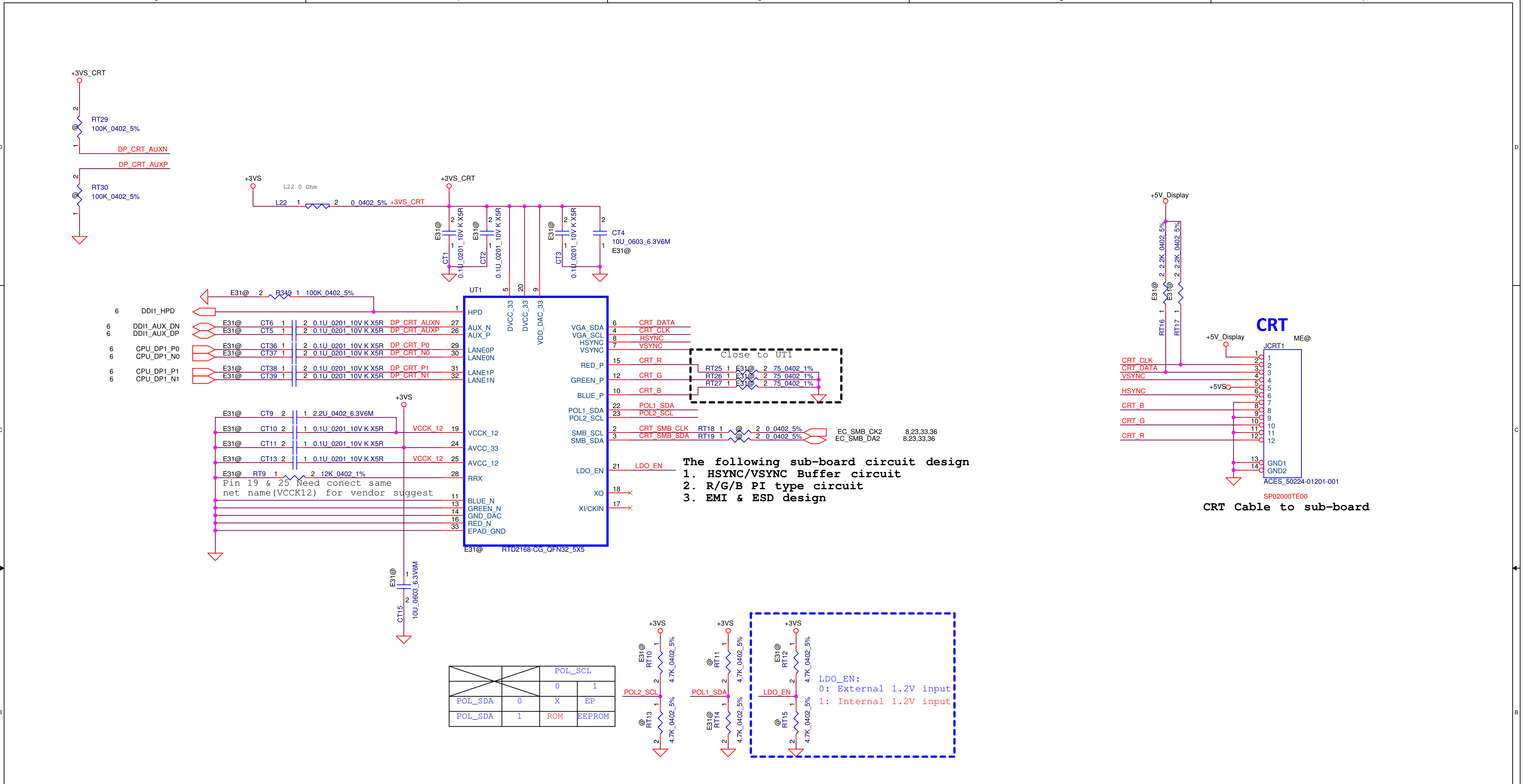

		POL_SCL 0	POL_SCL 1
POL_SDA	0	X	EP
POL_SDA	1	ROM	EEPROM

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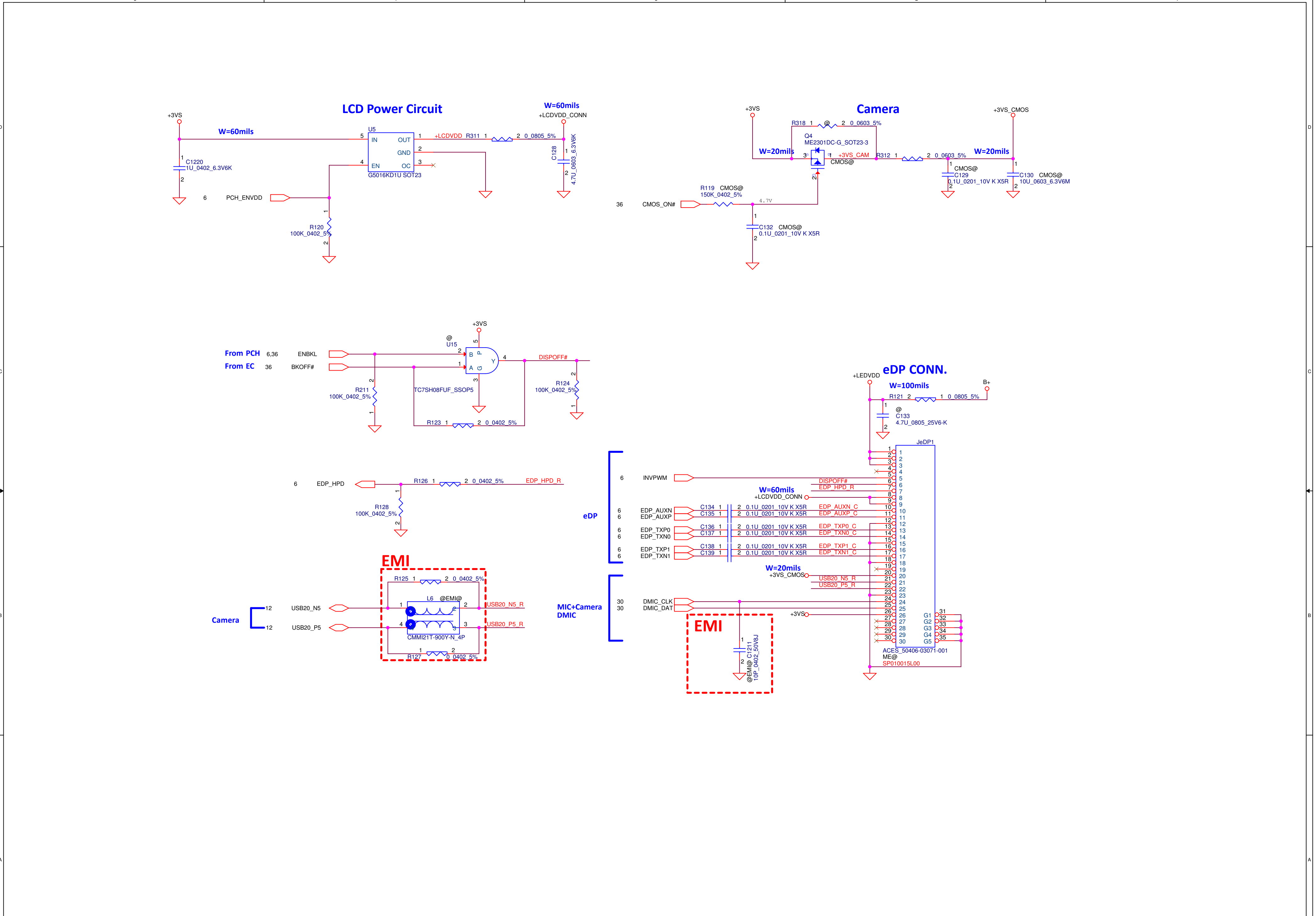
Issued Date	2014/08/16	Deciphered Date	2015/08/16

Compal Electronics, Inc.

Title: DP to VGA - RTD2168

Size: C Document Number: LA-D061P Rev: 0.3

Date: Friday, August 07, 2015



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Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Title: *eDP / Camera*

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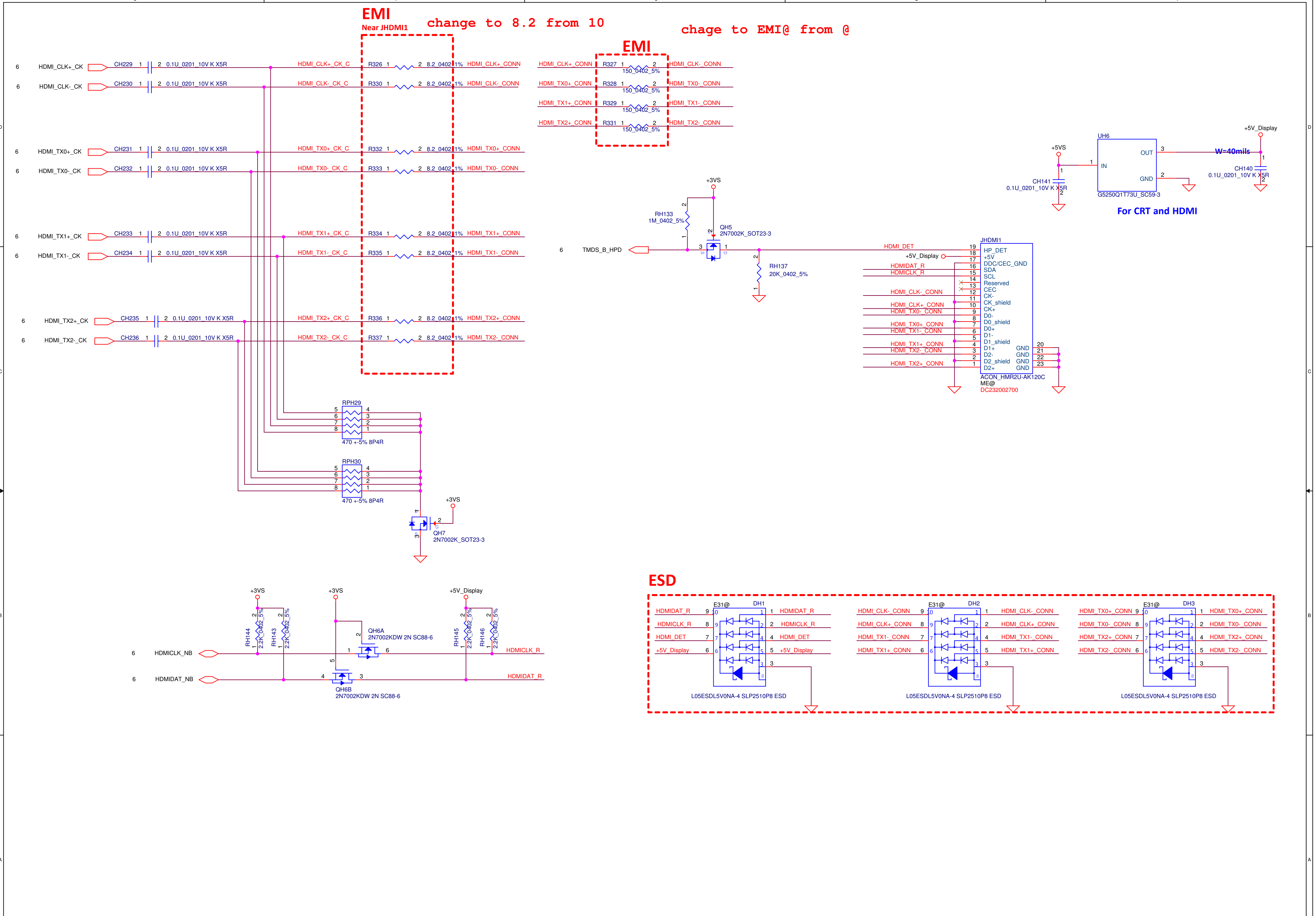
Date: Friday, August 07, 2015 | Sheet 28 of 52



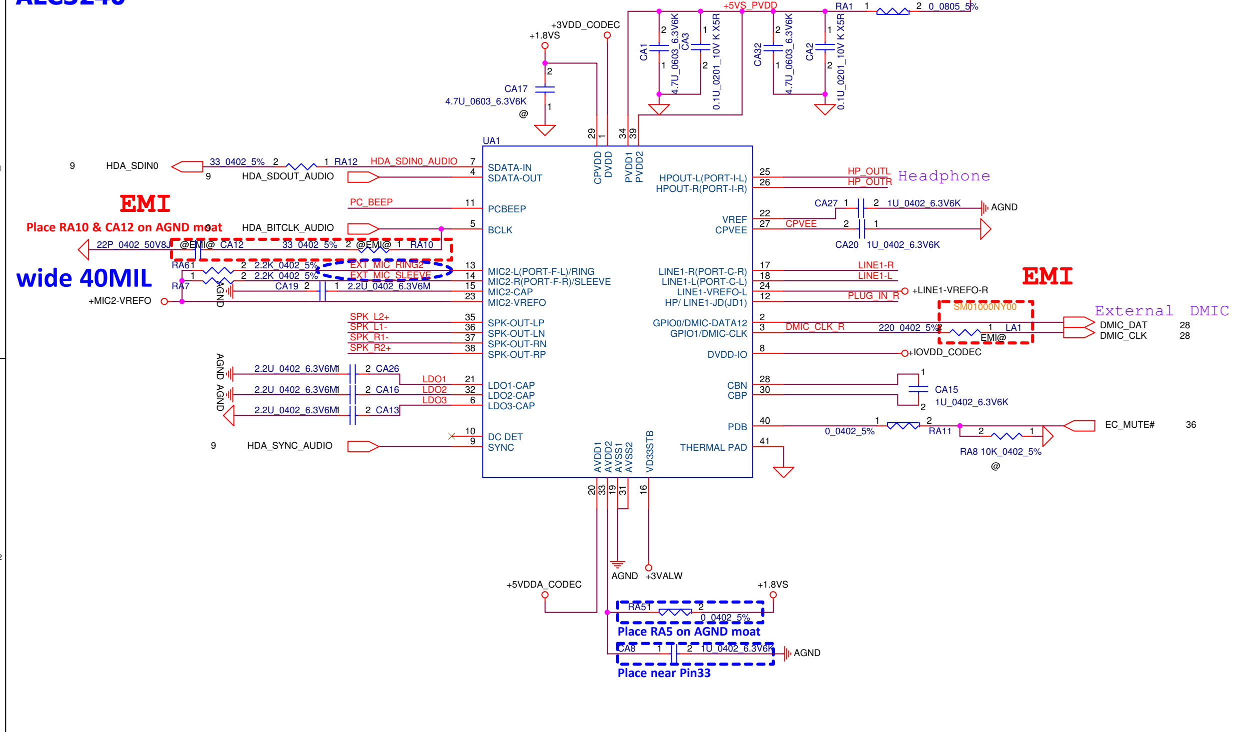
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

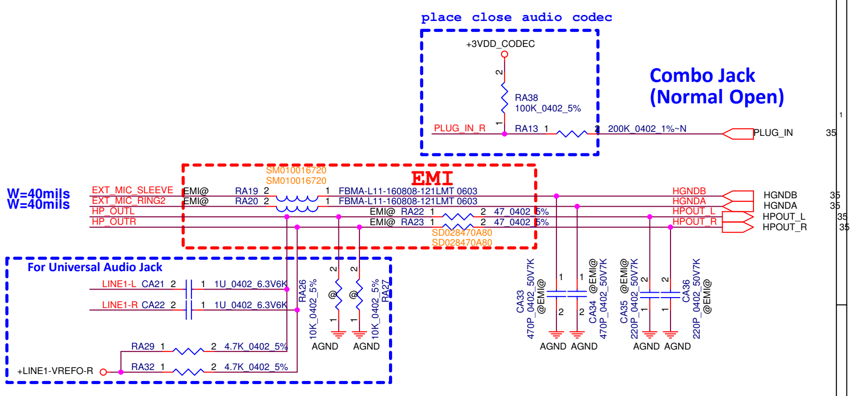
Title: **HDMI**

Size: C | Document Number: **LA-D061P** | Rev: 0.3

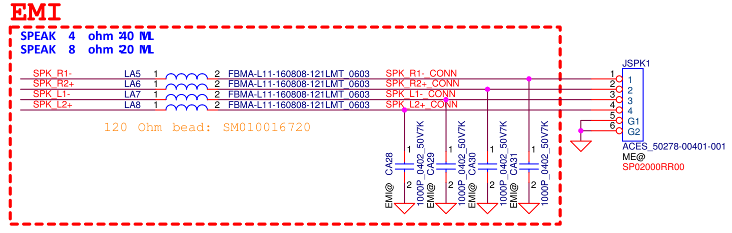
ALC3240



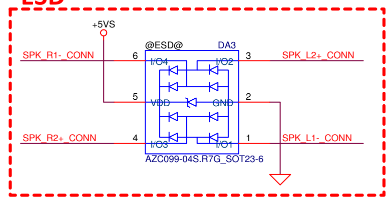
Input



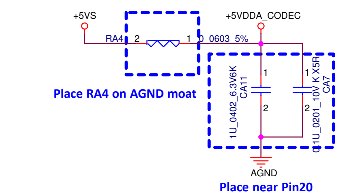
Output



ESD protection needs to be placed near connector side



+5VS → +5VDDA_CODEC



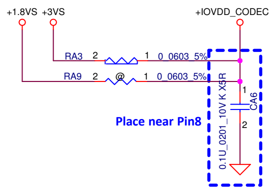
Each Platform Power Net Support list:

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	V
Intel Skylake	X	V	V	V	V

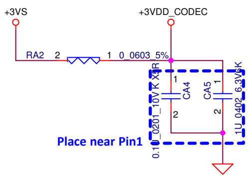
Each Platform HDA Link Voltage Support (Pin 8):

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

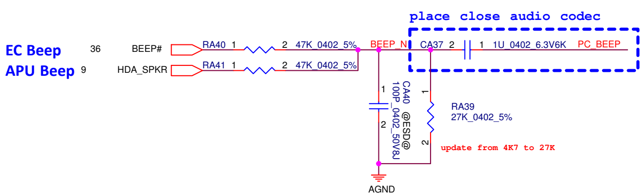
+3VS → +IOVDD_CODEC



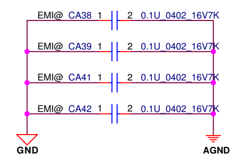
+3VS → +3VDD_CODEC



PC Beep



EMI



Security Classification	Compal Secret Data		
Issued Date	2014/08/04	Deciphered Date	2015/08/04

Compal Electronics, Inc.

Title: HD Audio Codec_ALC3240

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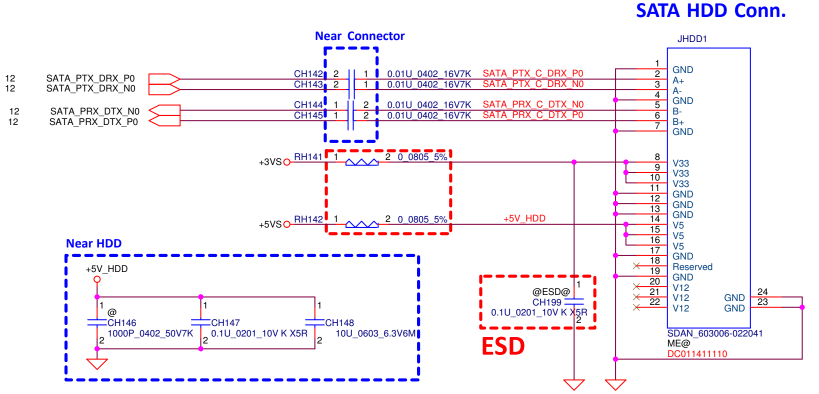
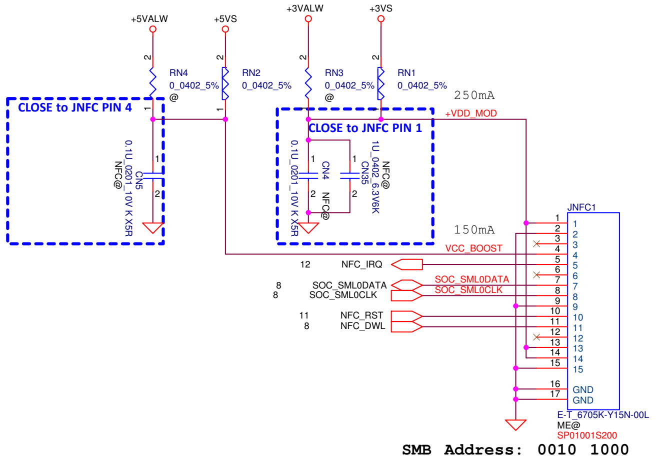
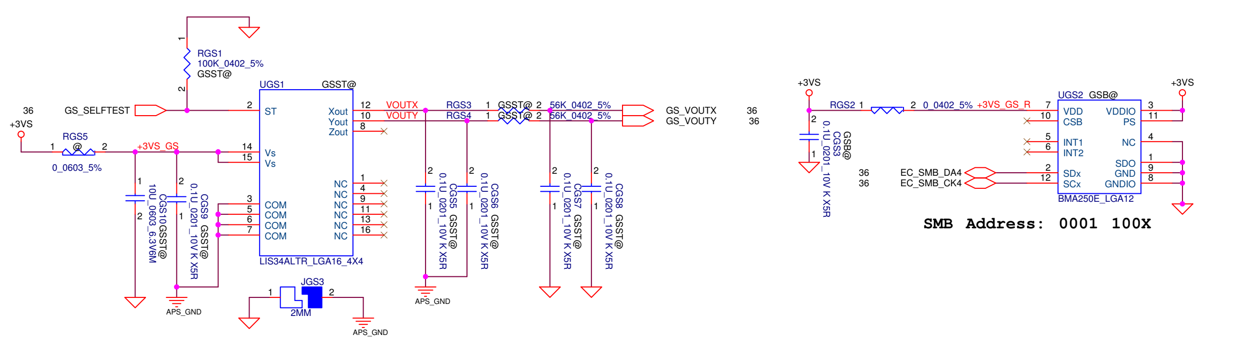
HDD



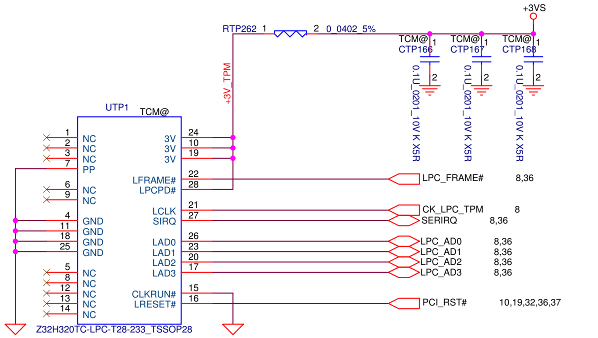
NFC



APS (G-Sensor)



TPM



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

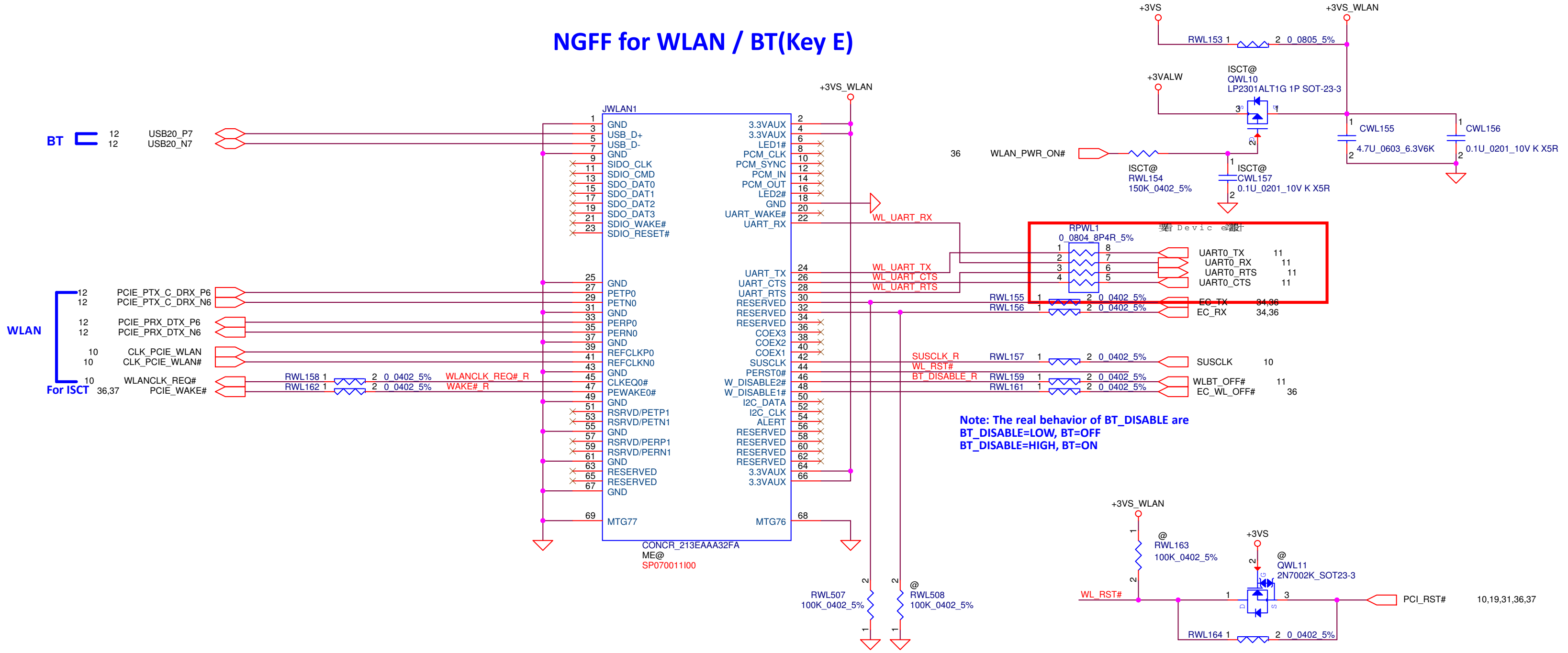
Compal Electronics, Inc.

Title: **HDD/TPM/APS/NFC**

Size	Document Number	Rev
C	LA-D061P	0.3

Date: Friday, August 07, 2015

NGFF for WLAN / BT(Key E)



Security Classification	Compal Secret Data		
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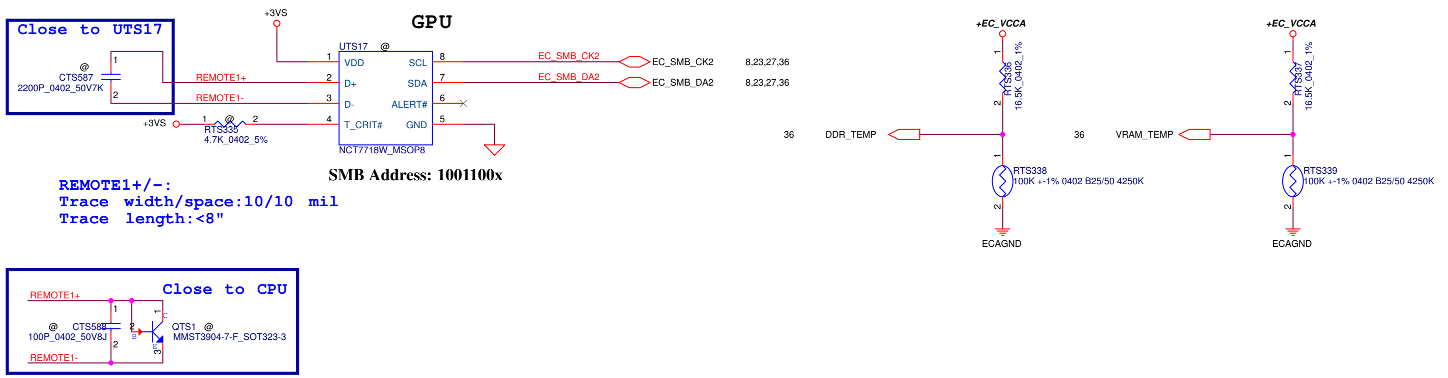
Compal Electronics, Inc.

Title: NGFF WLAN / BT

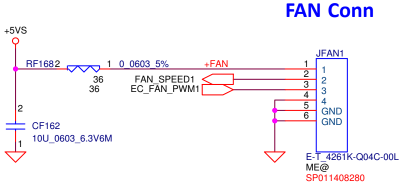
Size | Document Number: LA-D061P | Rev 0.3

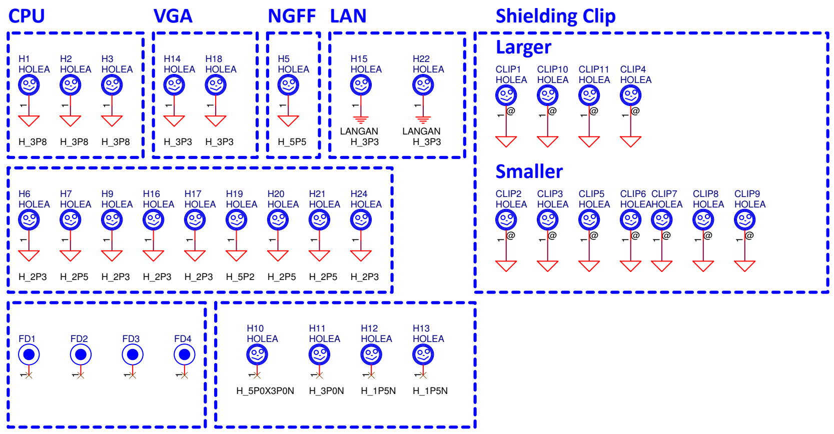
Date: Friday, August 07, 2015 | Sheet 32 of 52

Thermal Sensor



FAN Conn





Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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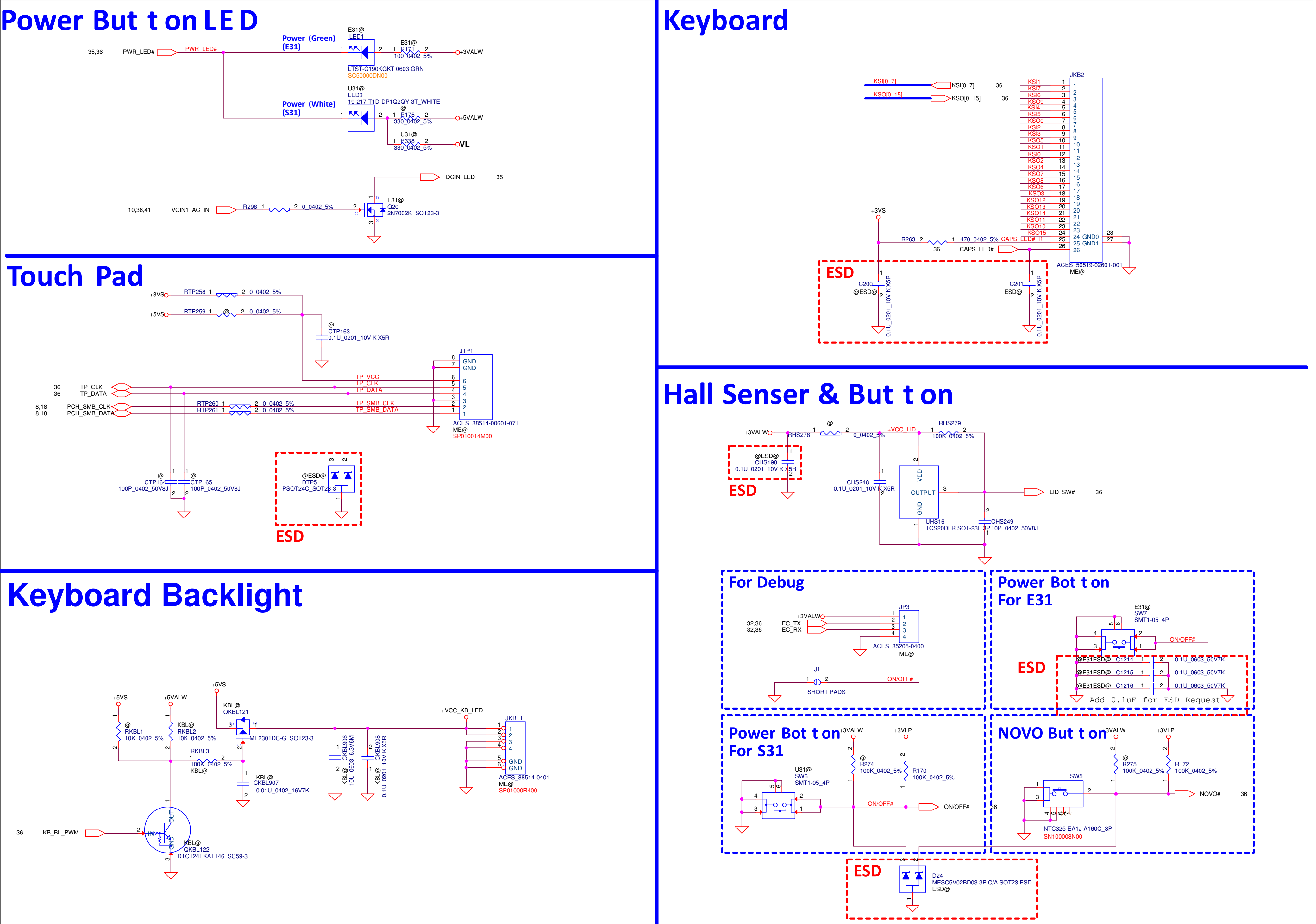
Title	FAN / Thermal Senser	
Size C	Document Number LA-D061P	Rev 0.3
Date: Friday, August 07, 2015	Sheet 33 of 52	



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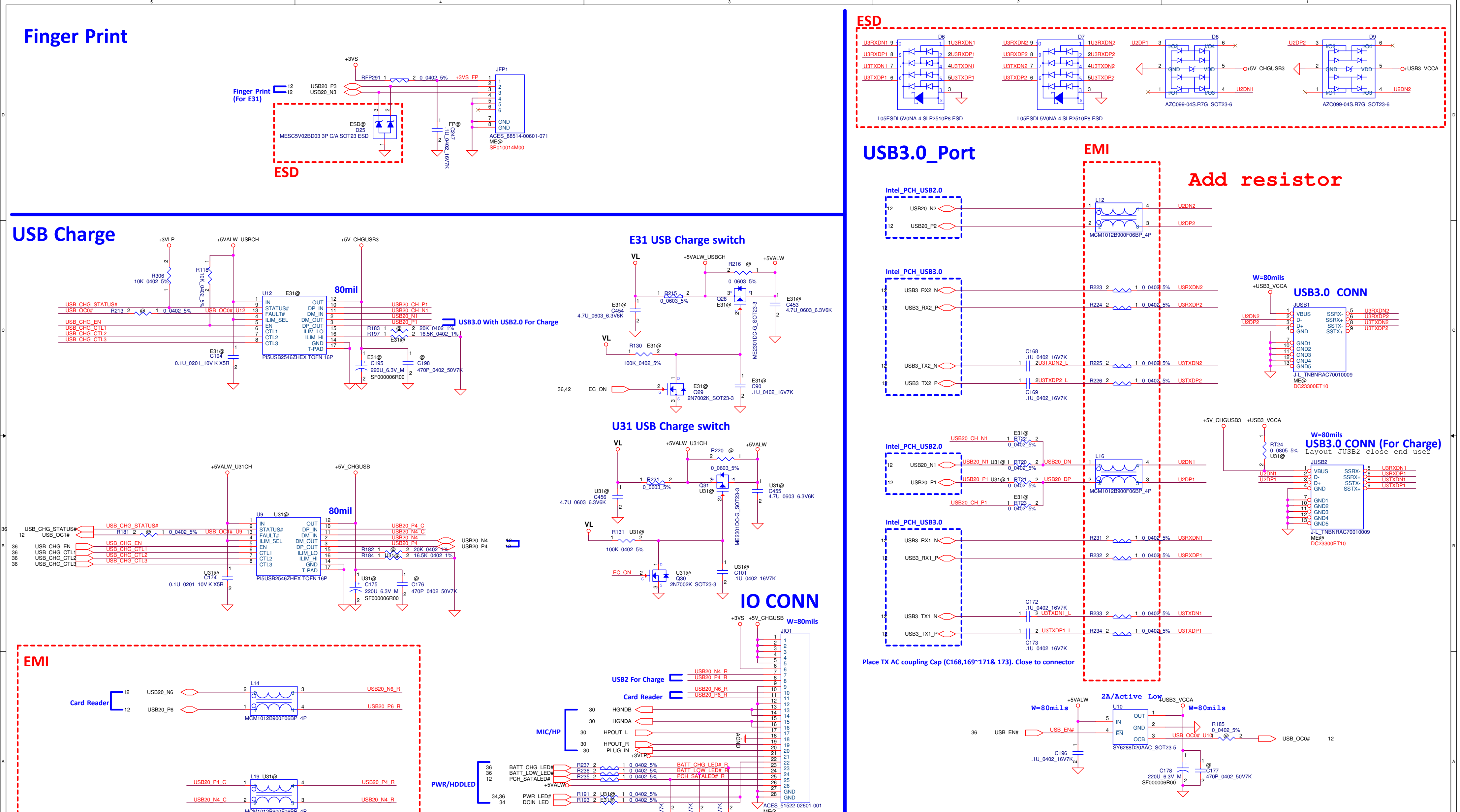
				Date: Friday, August 07, 2015; Sheet 34 of 52



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Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title: USB2 / USB3 / FP / IO Board
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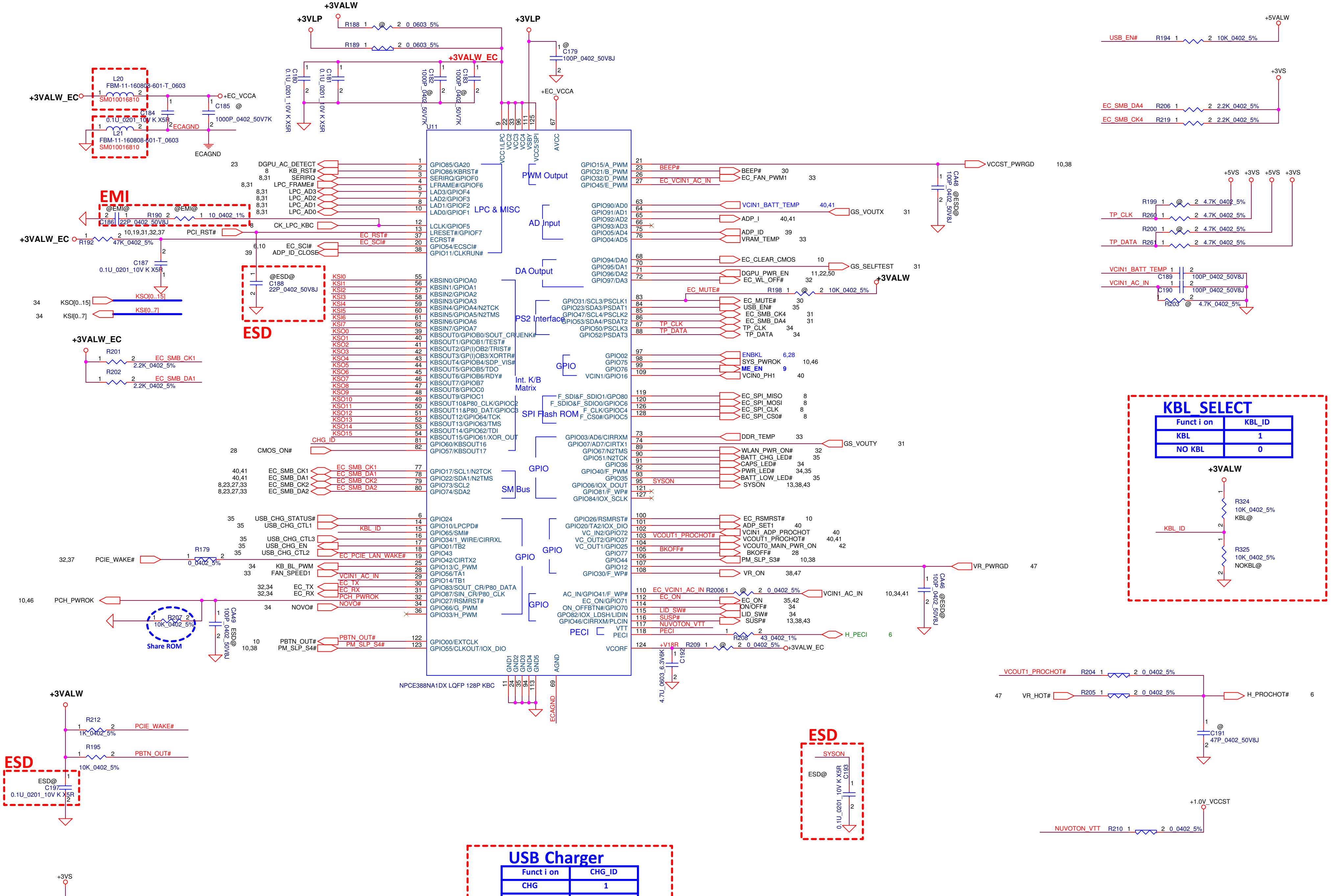
			Date: Friday, August 07, 2015; Sheet 35 of 52



KBL_SELECT

Function	KBL_ID
KBL	1
NO KBL	0

USB Charger

Function	CHG_ID
CHG	1
NO CHG	0

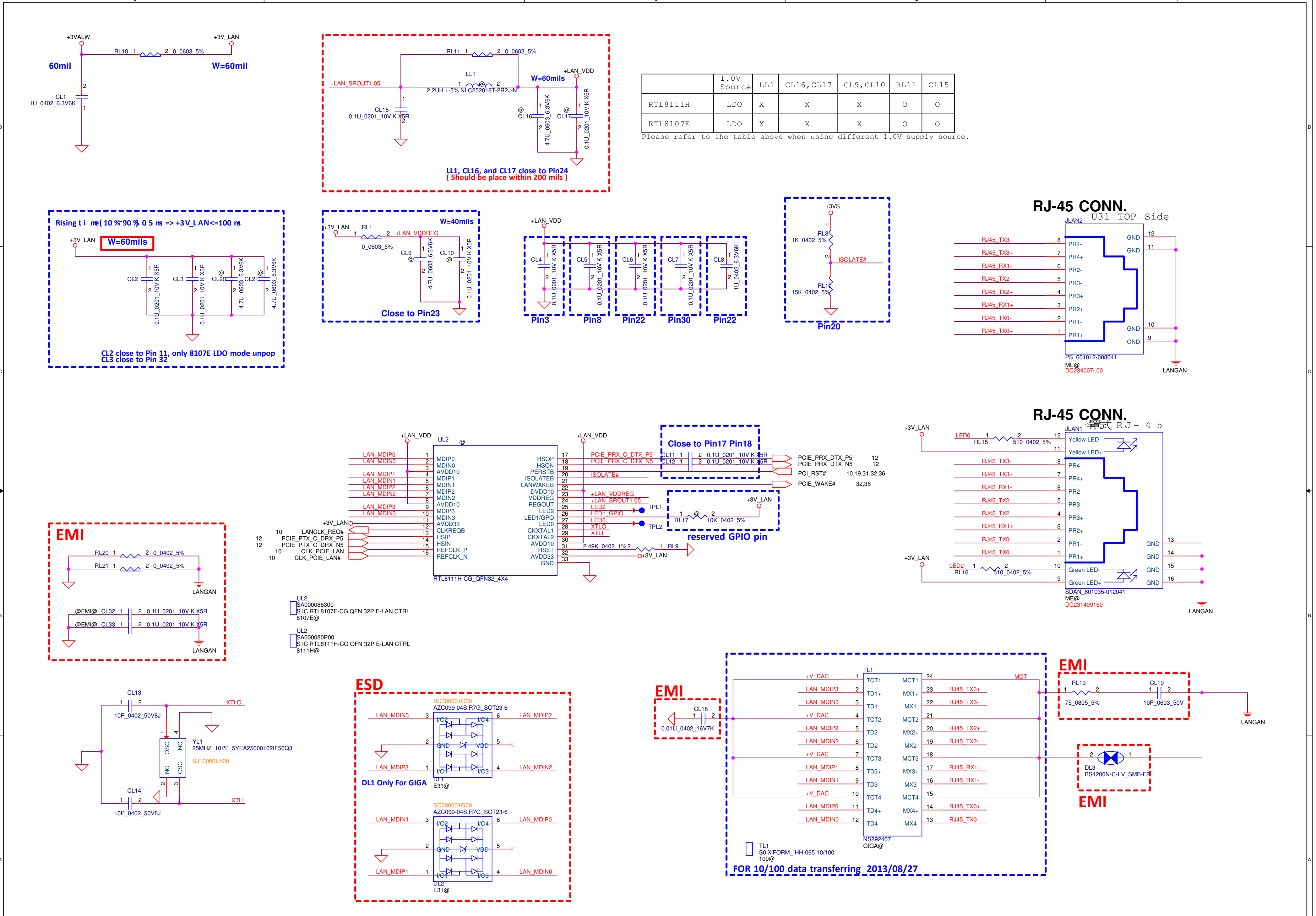
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: EC NPCE388

Size: C | Document Number: LA-C311P | Rev 0.3

Date: Friday, August 07, 2015 |



	1.0V Source	LL1	CL16,CL17	CL9,CL10	RL11	CL15
RTL8111H	LDO	X	X	X	O	O
RTL8107E	LDO	X	X	X	O	O

Please refer to the table above when using different 1.0V supply source.

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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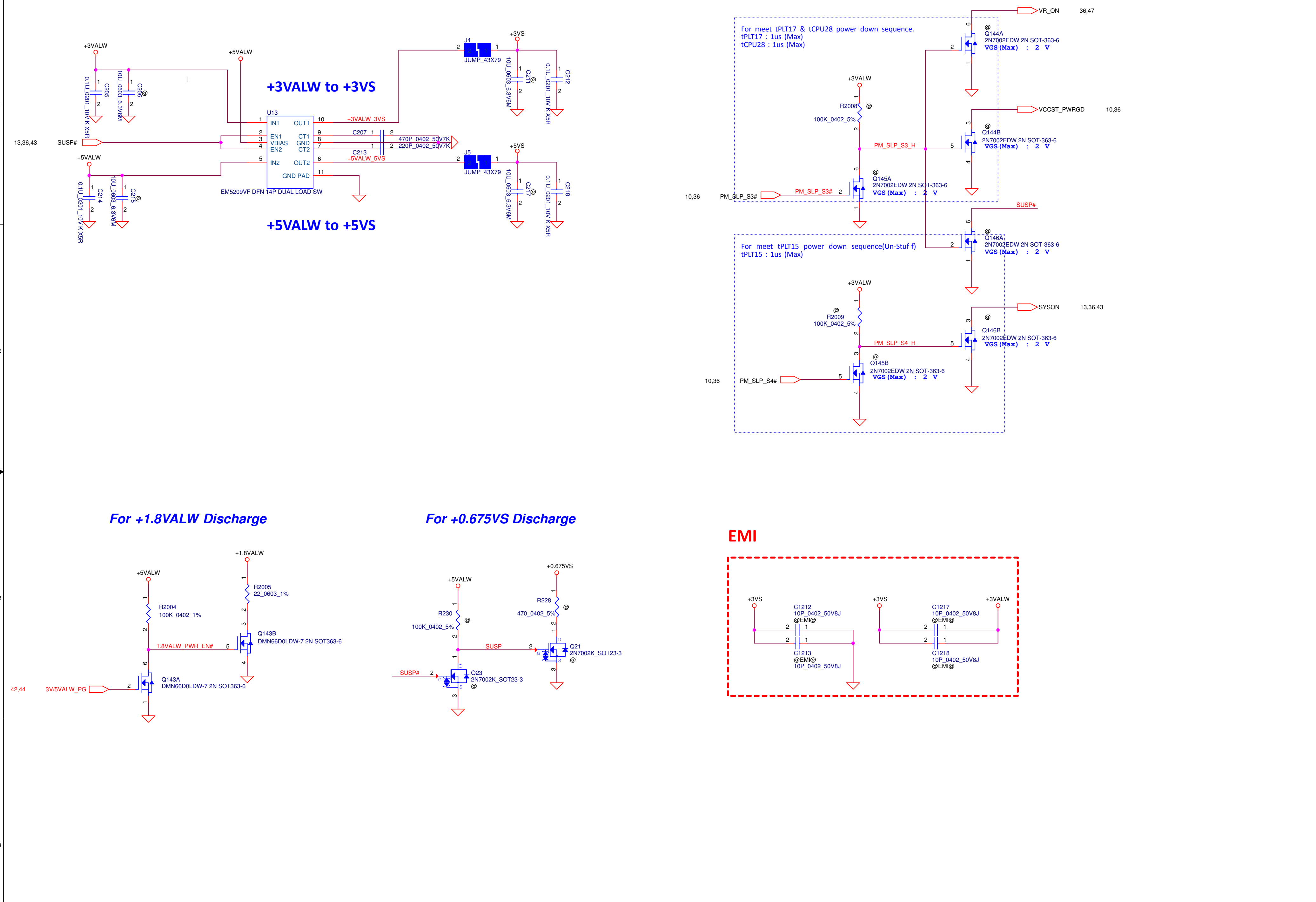
Title: LAN_RTL8111H / RTL8107E

Size: C | Document Number: LA-D061P | Rev: 0.3



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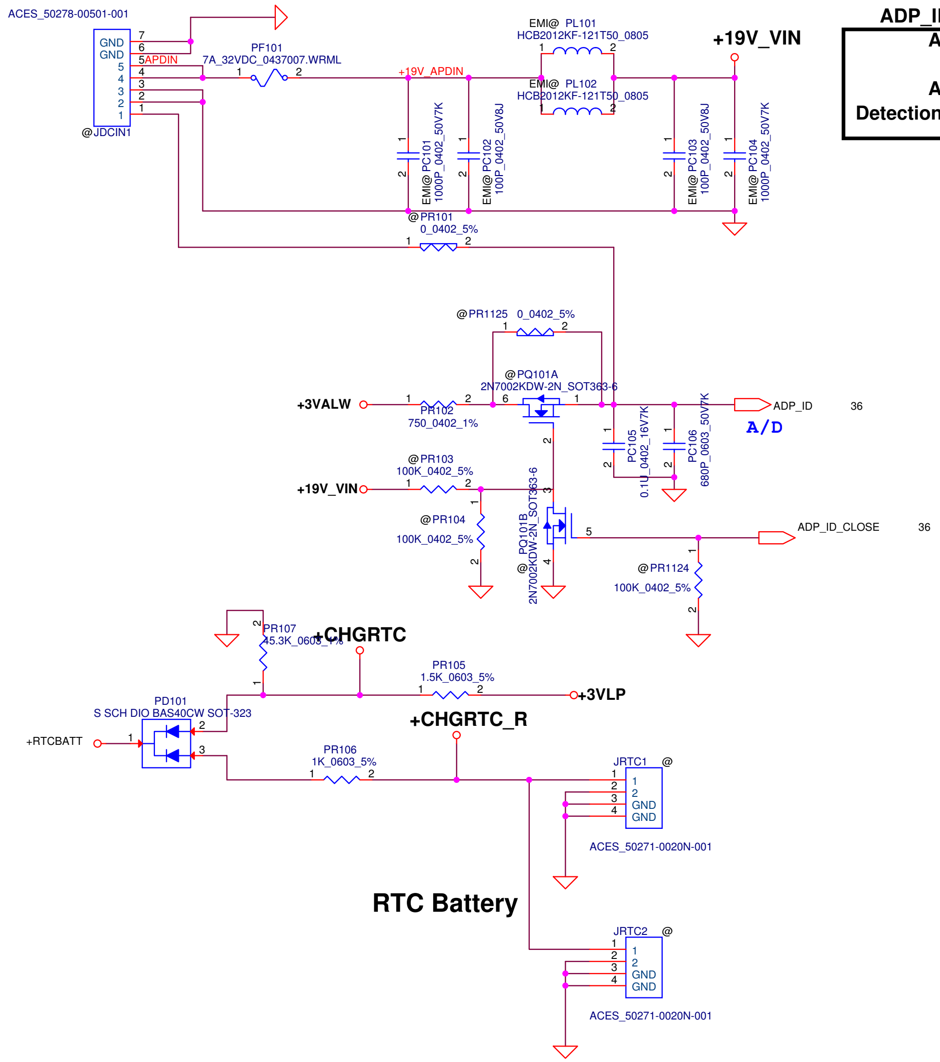
			Date: Friday, August 07, 2015; Sheet 38 of 52



ADP_ID

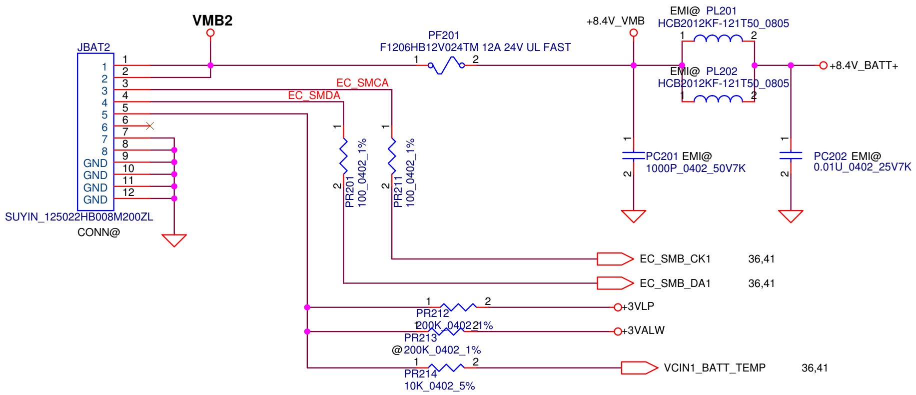
AC Adapter	65W	45W
R(ohm)	287	118
ADP_ID(V)	0.913	0.448
Detection voltage	0.693~1.134	0.234~0.663

Security Classification	Compal Secret Data		
Issued Date	2013/10/24	Deciphered Date	2014/11/14

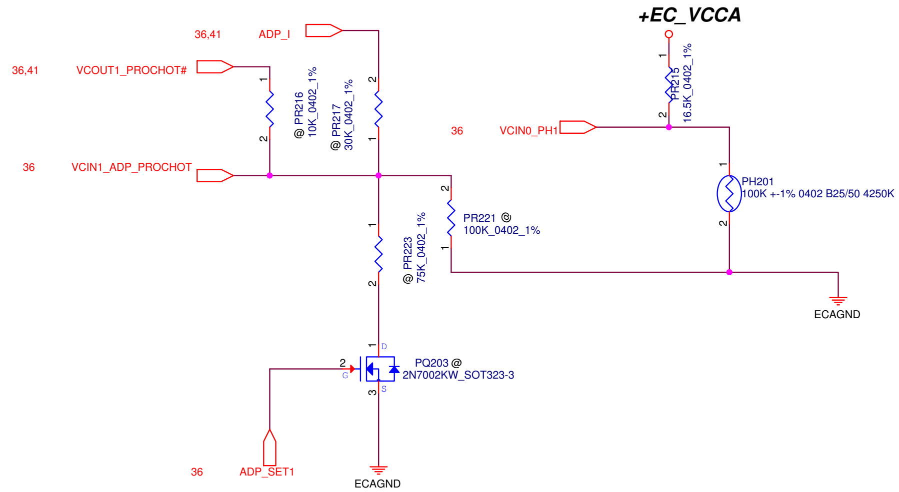
Compal Electronics, Inc.

Title: **PWR DCIN / RTC Battery**

Size: Custom | Document Number: BE_BDW | Rev: 0.2



PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



ADP_SET1 =0 is 45W
ADP_SET1 =1 is 65W

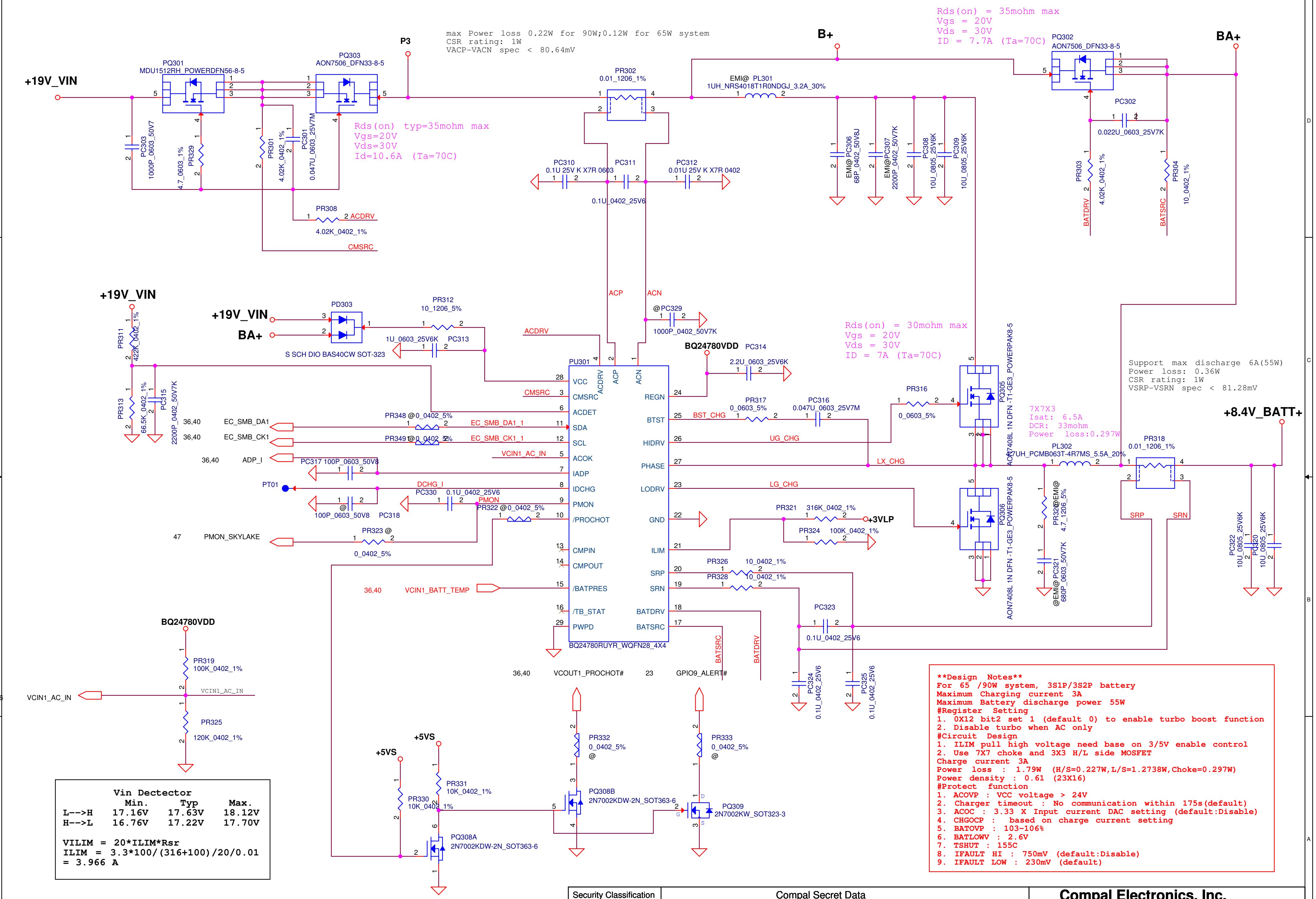
65W : 85W active, 65W recovery(vcin1_adp_procheot 0.7647V)
45W : 65W active, 45W recovery(vcin1_adp_procheot 0.6923V)

Security Classification	Compal Secret Data		
Issued Date	2013/10/24	Deciphered Date	2014/11/14

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: BE_BDW | Rev: 0.2



Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(316+100)/20/0.01
= 3.966 A

Design Notes
For 65 /90W system, 3S1P/3S2P battery
Maximum Charging current 3A
Maximum Battery discharge power 55W
#Register Setting
1. 0X12 bit2 set 1 (default 0) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ILIM pull high voltage need base on 3/5V enable control
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. Charger timeout : No communication within 175s(default)
3. ACOC : 3.33 X Input current DAC setting (default:Disable)
4. CHGOCP : based on charge current setting
5. BATOVP : 103-106%
6. BATLOWV : 2.6V
7. TSHUT : 155C
8. IFAULT HI : 750mV (default:Disable)
9. IFAULT LOW : 230mV (default)

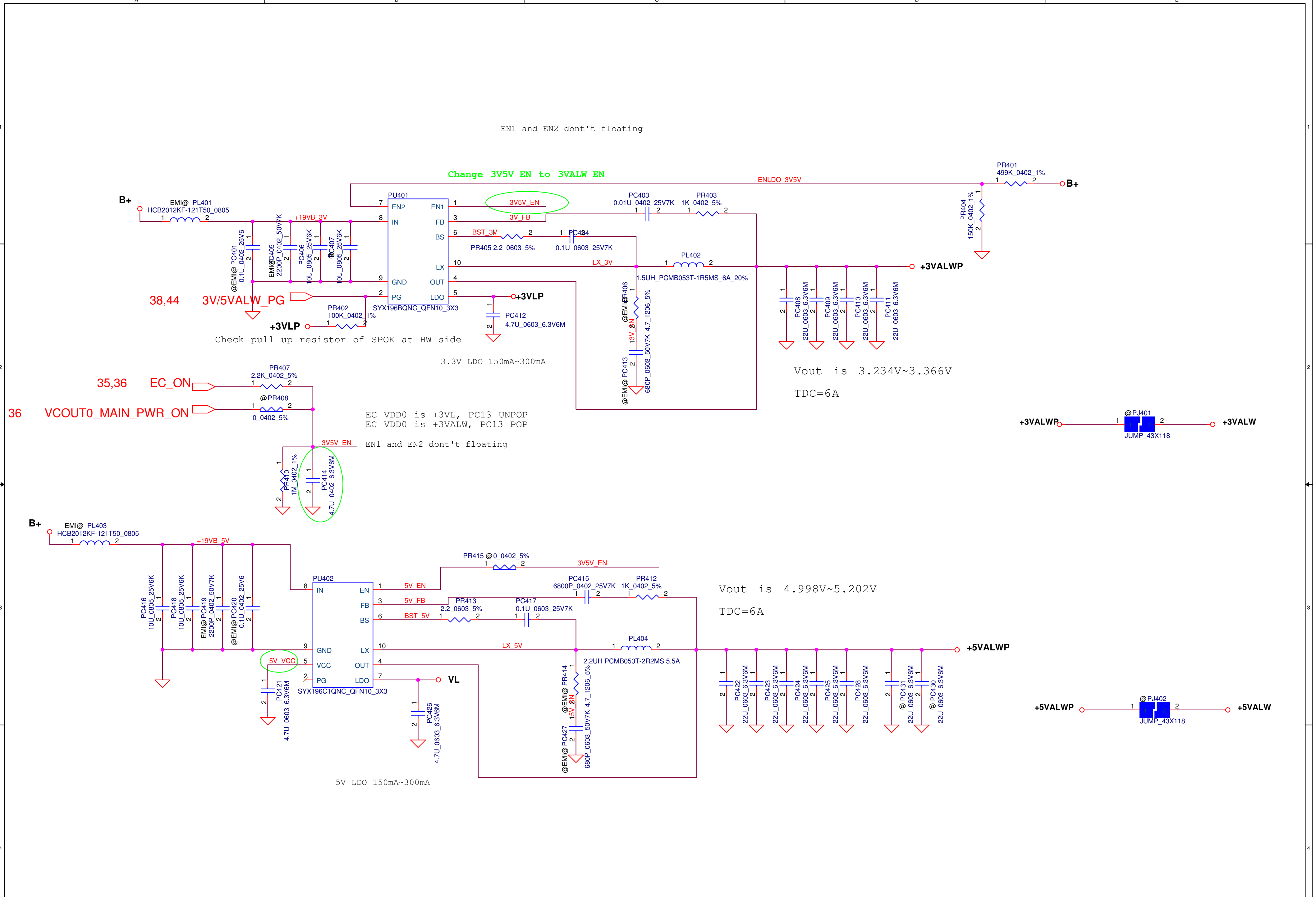
Security Classification	Compal Secret Data		
Issued Date	2013/10/24	Deciphered Date	2014/11/14

Compal Electronics, Inc.

Title: BQ24780

Size: Custom | Document Number | Rev 2.0

Date: Friday, August 07, 2015 |



Security Classification	Compal Secret Data		
Issued Date	2013/10/24	Deciphered Date	2014/11/14

Compal Electronics, Inc.

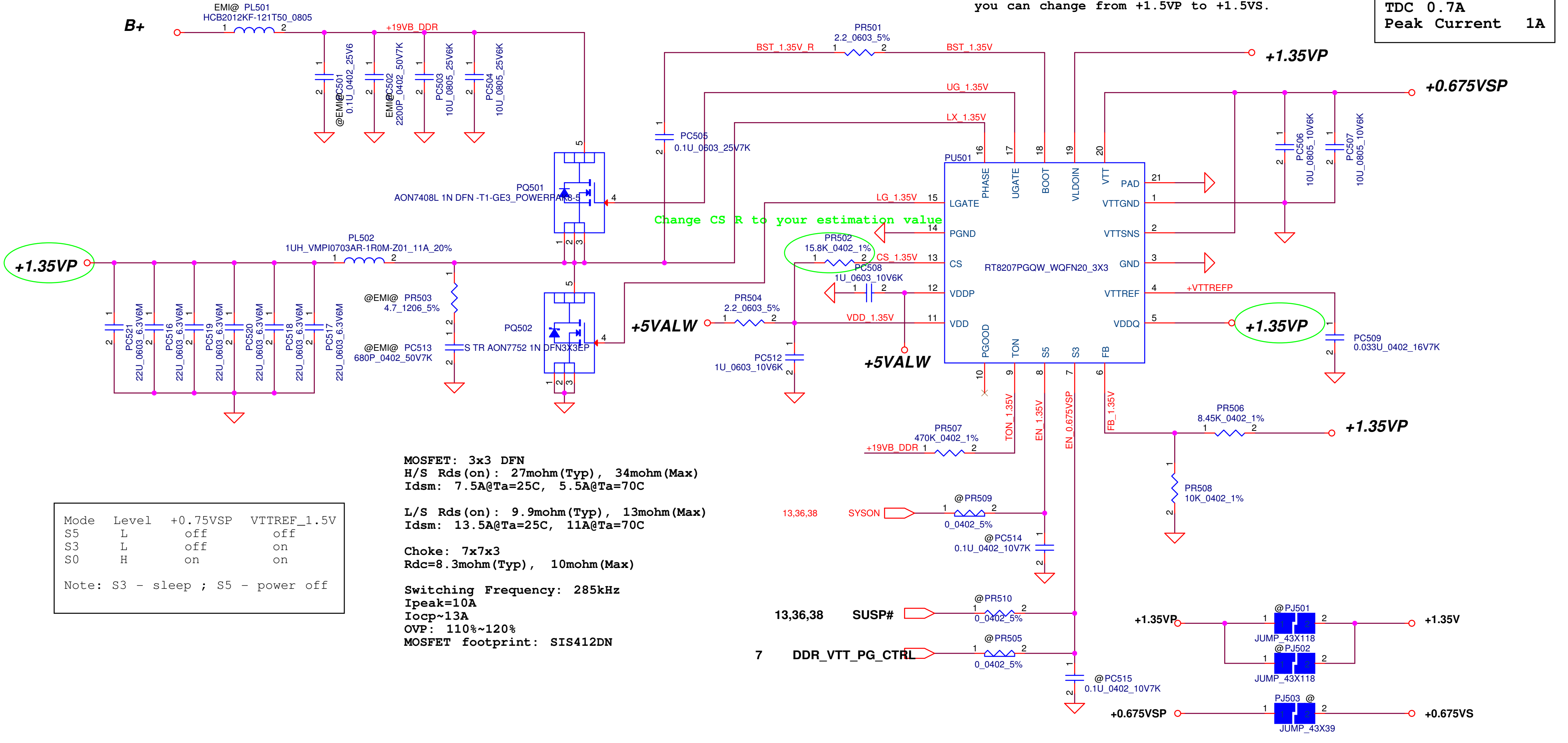
Title: **+3VALW/+5VALW**

Size: Custom | Document Number: BE_BDW | Rev 2.0

Date: Friday, August 07, 2015 | Sheet 42 of 52

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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Issued Date	2013/10/24	Deciphered Date	2014/11/14

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Title: RT8207M

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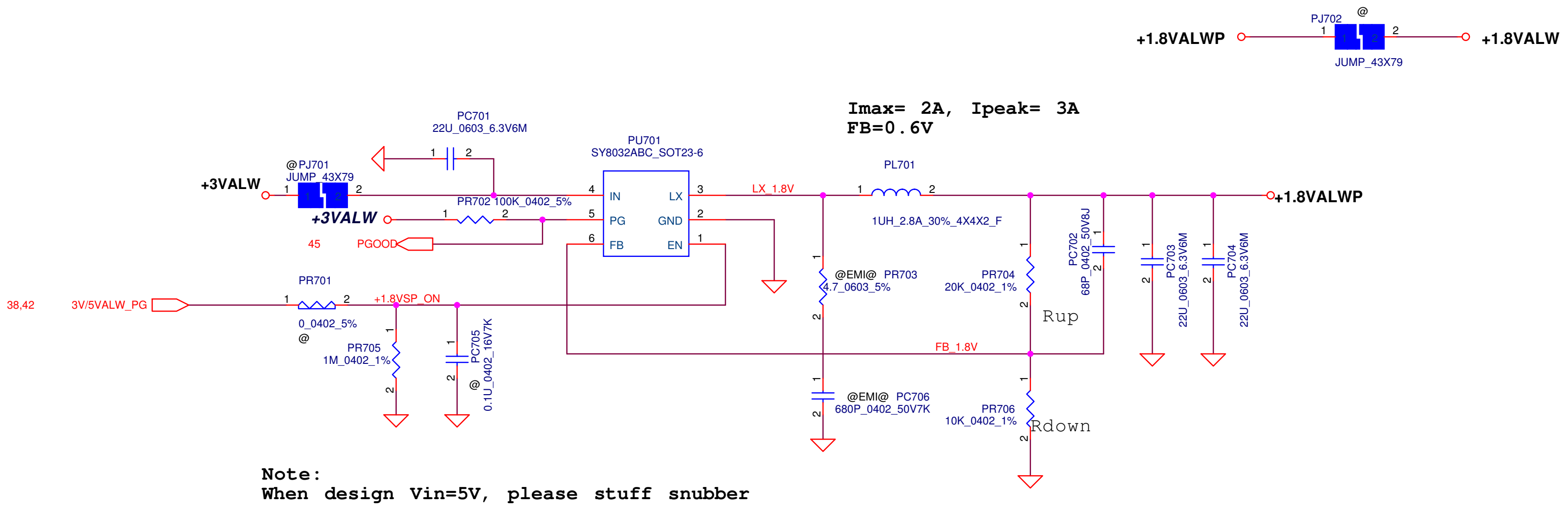

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

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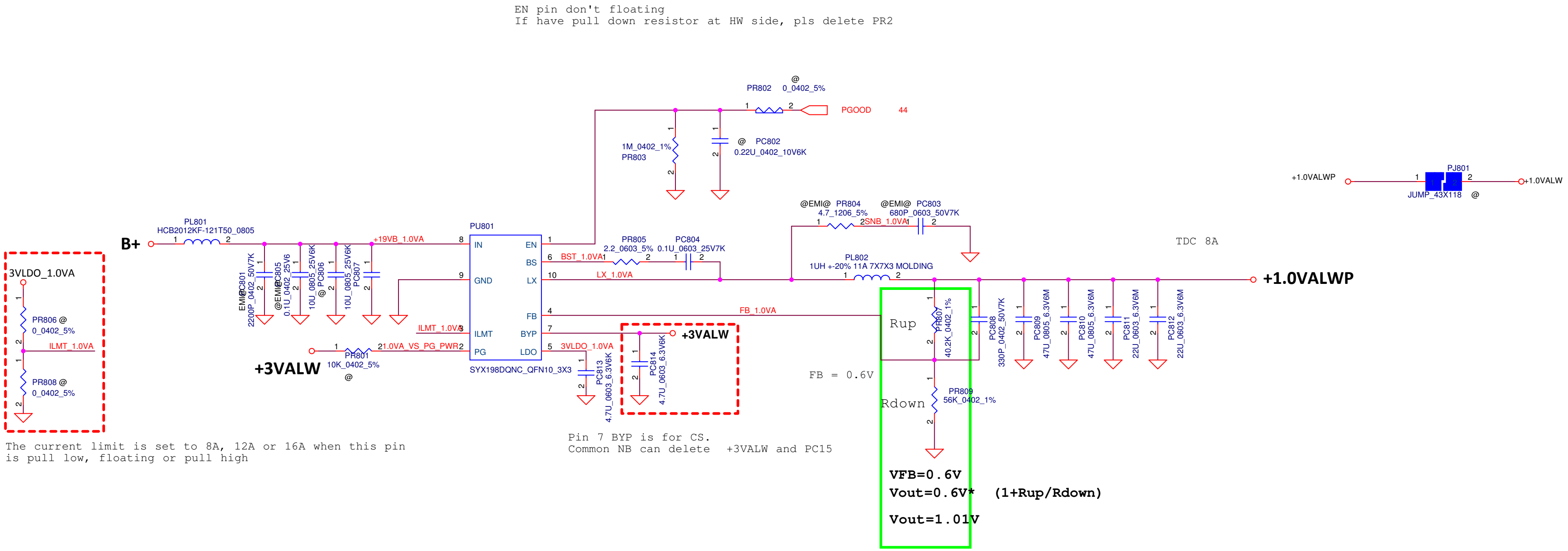
				Date: Friday, August 07, 2015; Sheet 44 of 52



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Module model information

NB681_V1.mdd

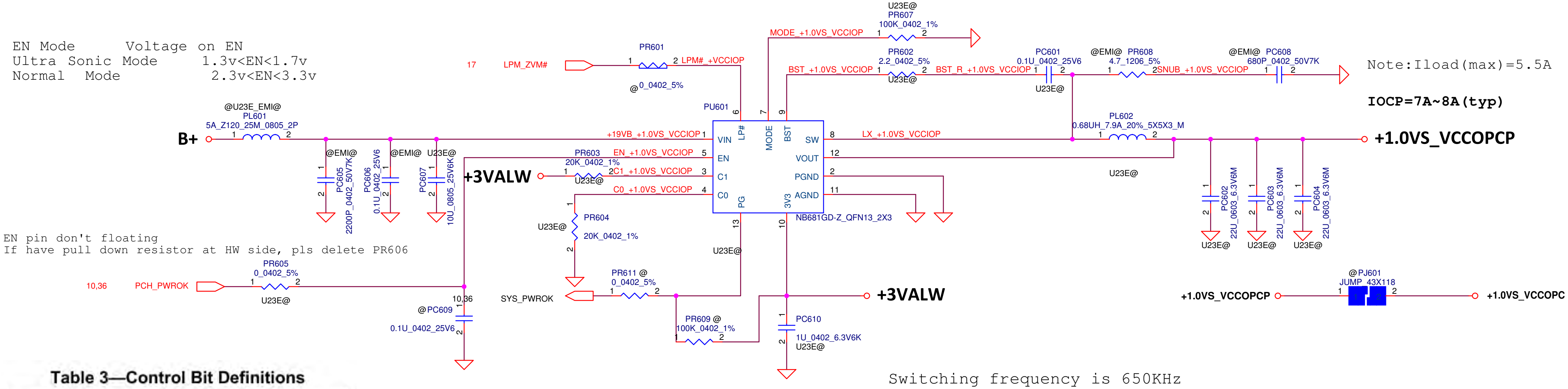

Table 3—Control Bit Definitions

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPCH	0	X	X	0.7
	1	0	0	0.8
	1	0	1	0.85
	1	1	0	0.9
	1	1	1	0.95
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2

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Title: +1.0VS_VCCOPC

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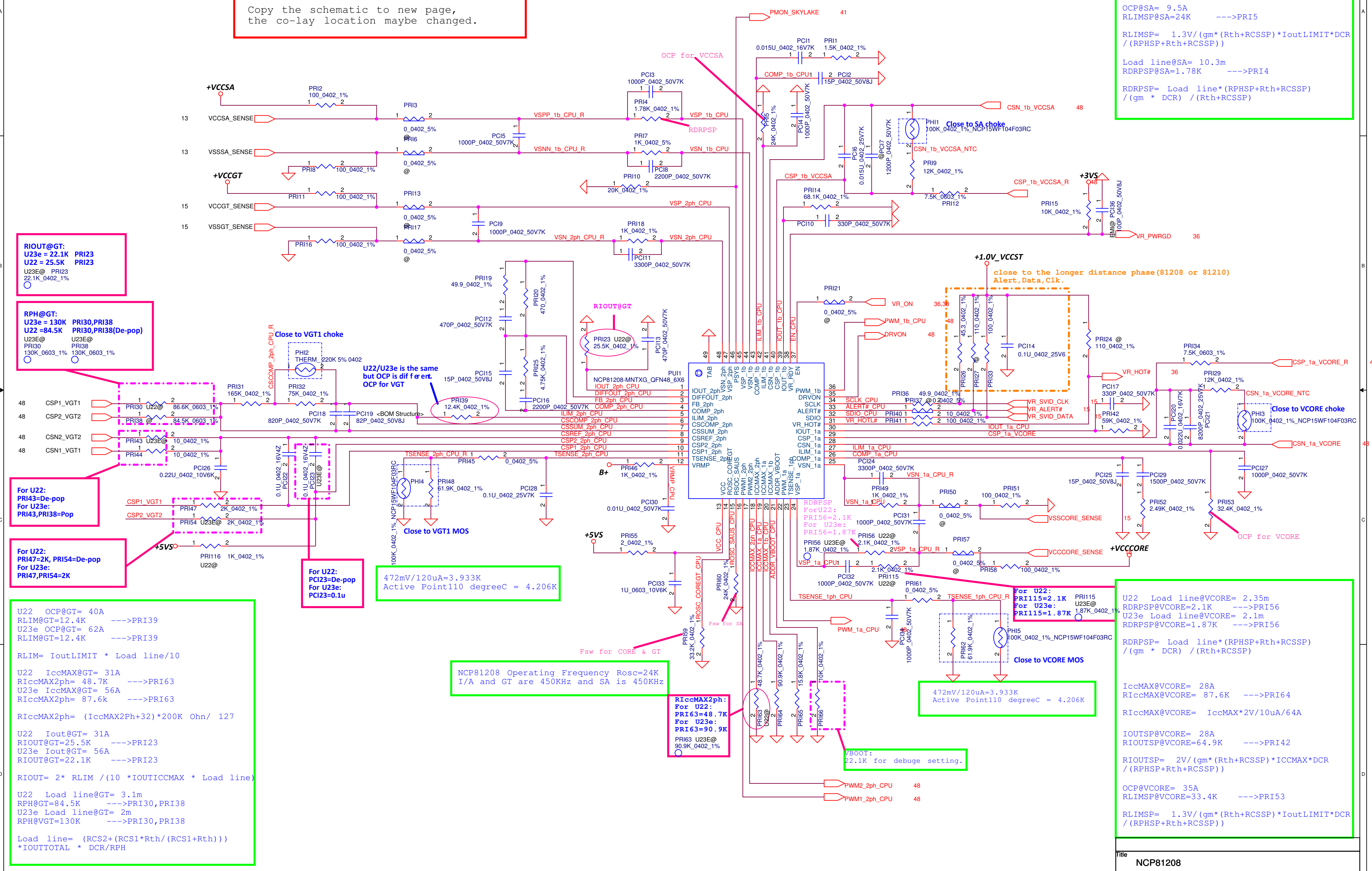
CPU CORE

Module model information

NCP81208_V1A.mdd for IC portion

NCP81208_V1B.mdd for SW portion

Copy the schematic to new page,
the co-lay location maybe changed.



IccMAX@SA= 5A
RIccMAX@SA= 15.8K --->PRI65

RIccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K --->PRI14

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=24K --->PRI5

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
RDRPSP@SA=1.78K --->PRI4

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

RIOUT@GT:
U23e = 22.1K PRI23
U22 = 25.5K PRI23

RPH@GT:
U23e = 130K PRI30,PRI38
U22 =84.5K PRI30,PRI38(De-pop)

For U22:
PRI43=De-pop
For U23e:
PRI43,PRI38=Pop

For U22:
PRI47=2K, PRI54=De-pop
For U23e:
PRI47,PRI54=2K

For U22:
PCI23=De-pop
For U23e:
PCI23=0.1u

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

U22 OCP@GT= 40A
RLIM@GT=12.4K --->PRI39
U23e OCP@GT= 62A
RLIM@GT=12.4K --->PRI39

RLIM= IoutLIMIT * Load line/10

U22 IccMAX@GT= 31A
RIccMAX2ph= 48.7K --->PRI63
U23e IccMAX@GT= 56A
RIccMAX2ph= 87.6k --->PRI63

RIccMAX2ph= (IccMAX2Ph+32)*200K Ohn/ 127

U22 Iout@GT= 31A
RIOUT@GT=25.5K --->PRI23
U23e Iout@GT= 56A
RIOUT@GT=22.1K --->PRI23

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

U22 Load line@GT= 3.1m
RPH@GT=84.5K --->PRI30,PRI38
U23e Load line@GT= 2m
RPH@VGT=130K --->PRI30,PRI38

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))
*IOUTTOTAL * DCR/RPH

NCP81208 Operating Frequency Rosc=24K
I/A and GT are 450KHz and SA is 450KHz

RIccMAX2ph:
For U22:
PRI63=48.7K
For U23e:
PRI63=90.9K

VBOOT:
22.1K for debuge setting.

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

For U22:
PRI115=2.1K
For U23e:
PRI115=1.87K

U22 Load line@VCORE= 2.35m
RDRPSP@VCORE=2.1K --->PRI56
U23e Load line@VCORE= 2.1m
RDRPSP@VCORE=1.87K --->PRI56

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

IccMAX@VCORE= 28A
RIccMAX@VCORE= 87.6K --->PRI64

RIccMAX@VCORE= IccMAX*2V/10uA/64A

IOUTSP@VCORE= 28A
RIOUTSP@VCORE=64.9K --->PRI42

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@VCORE= 35A
RLIMSP@VCORE=33.4K --->PRI53

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Title: NCP81208		
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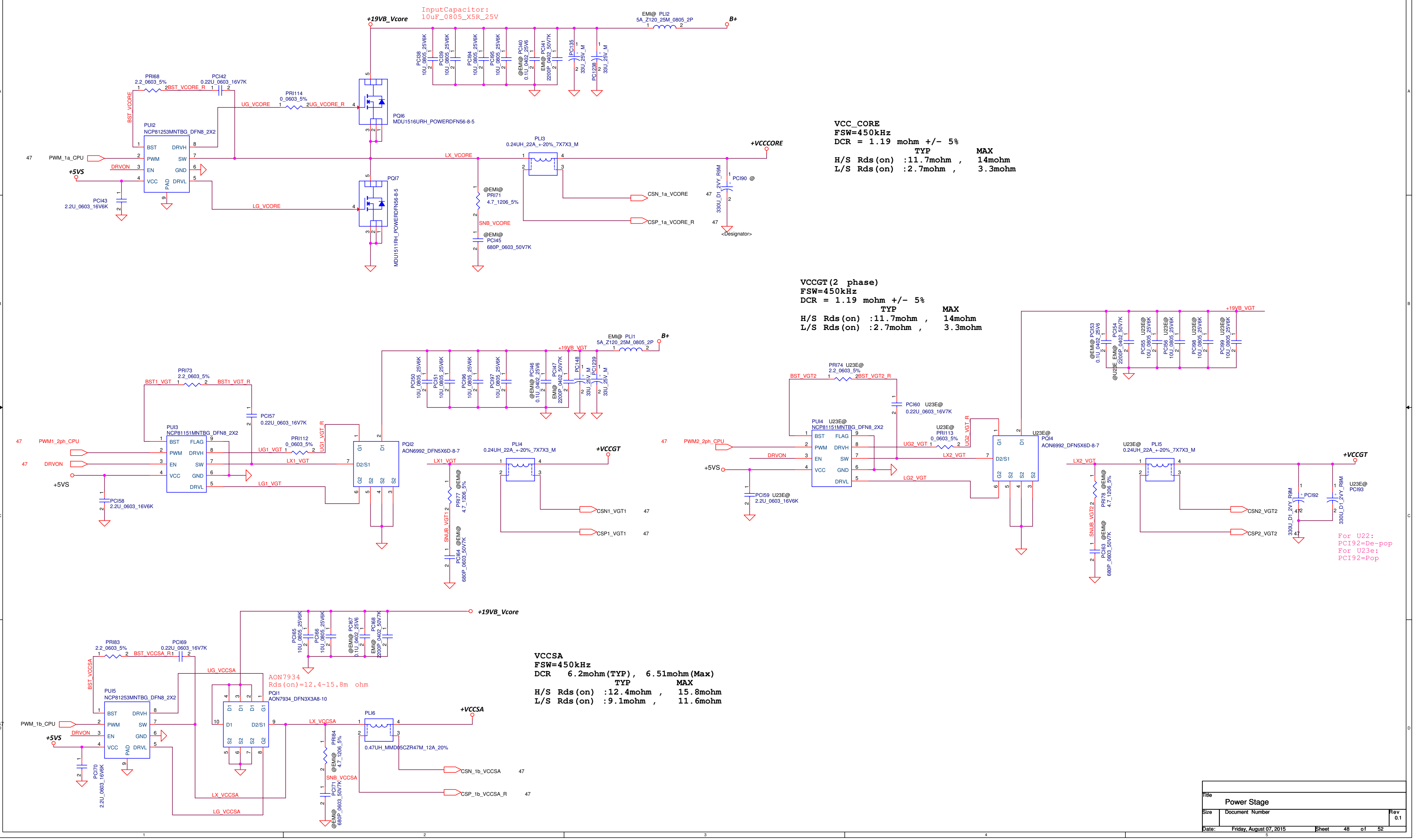
CPU POWER STAGES



VCC_CORE
FSW=450kHz
DCR = 1.19 mohm +/- 5%

	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm

VCCGT(2 phase)
FSW=450kHz
DCR = 1.19 mohm +/- 5%

	TYP	MAX
H/S Rds(on)	:11.7mohm ,	14mohm
L/S Rds(on)	:2.7mohm ,	3.3mohm

VCCSA
FSW=450kHz
DCR 6.2mohm(TYP), 6.51mohm(Max)

	TYP	MAX
H/S Rds(on)	:12.4mohm ,	15.8mohm
L/S Rds(on)	:9.1mohm ,	11.6mohm

Title	Power Stage
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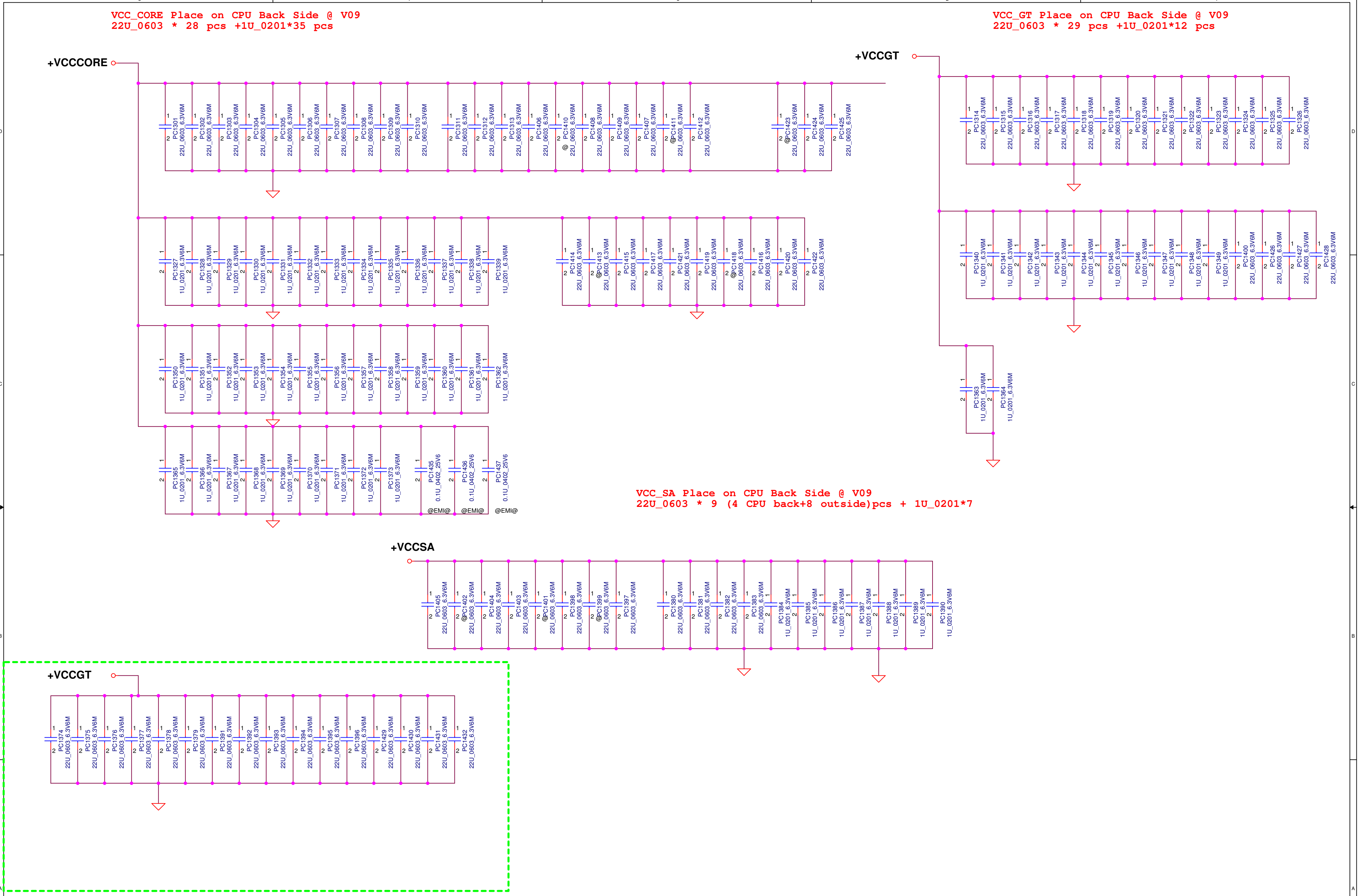

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3.PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B
Vmin		0.6V	0.6V
Vmax		1.2V	1.2V
Vboot		0.875V	0.9V
Voltage step		6.25mV	6.25mV
N of Voltage level		96	96
Rrefadj	PR806	39K	20K
Rref1	PR803	39K	20K
Rboot	PR805	1.5K	2K
Rref2=PR20+PR21	PR809	30K	18K
	PR812	1.5K	0
C	PC829	1.5nf	2.7nf

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

Remark:
1. Switching frequency setting:(Ton pin)
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)
=448Khz

2. Soft-Start:(SS pin)
SS time (Internal) is 0.7ms (PC18 un-pop)
SS time(External): (PC18 pop)
Tss=(Css*Vrefin)/Iss+2.3ms
=0.01U*0.9V/5uA+2.3ms=4.1ms

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

4.Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(20-1.028)*1.028/(448Khz*0.22u*20)=9.89A

OCP=54A/2=27A per phase
Ivalley=27A-9.89A/2=22.055A

H-side MOS:TPCA8065
Rds(on):
11.7mohm@Vgs=10V
9.4mohm@Vgs=4.5V
Id :16A@Ta=25 degC

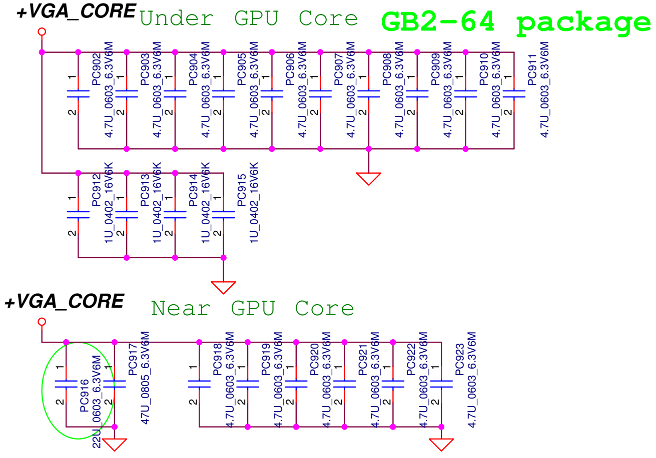
L-side MOS:TPCA8057
Rds(on):
2.0mohm@Vgs=10V
2.6~3.2mohm@Vgs=4.5V
Id :42A@Ta=25 degC

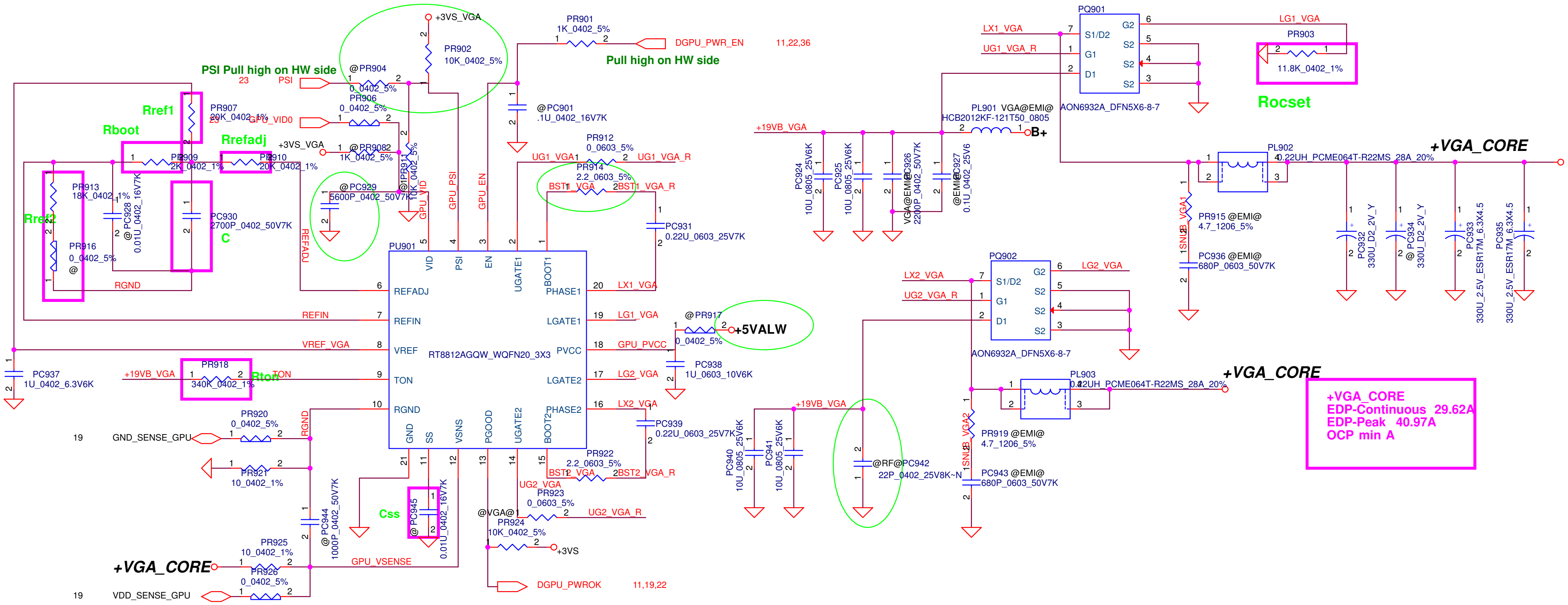
Choke: 0.36uH (Size:10*10*4)
Rdc=1.1mohm +-5%
Heat Rating Current=30A
Saturation Current=50A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=9.89A*3mohm=29.67mV

5.OpenVReg Configurations:(PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V





+VGA_CORE
EDP-Continuous 29.62A
EDP-Peak 40.97A
OCP min A

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	For cost down		Change 0 ohmn to short pad	2015.04.22	SIV
2	Layout space for RF solution	P40	Change PQ302 to AON7506 3X3 for RF solution	2015.04.22	SIV
3	Change +1.0VS_VCCOPCP solution	P45	Use NB681 IC for 1.0VS_VCCOPCP	2015.04.22	SIV
4	Down size	P40	Change PC314 from 2.2u_0805 to 2.2u_0603	2015.04.27	SIT
6	CPU transient	P46	Change PRI7 to 1k and PCI8 to 2200p and PRI14 to 68.1k and PCI11 to 3300p and PRI20 to 470 ohmn and PCI18 to 820p and PCI26 to 0.22u and PCI24 to 3300p	2015.04.27	SIT
7	Combin VCIN1 function to charger IC	P39	UM mount PR217 PR223 PR221 PQ203	2015.04.27	SIT
8	EMI reguest	P48	Reserve PC1435 PC1436 PC1437	2015.04.27	SIT
9	RTC circuit	P38	Reserve PR107	2015.04.27	SIT
10	RF rguest	P45	VR_PWRGD reserve PCI36 on	2015.04.27	SIT
11	change highside mos for cost	P40 P42	Change PQ305 PQ306 PQ501 to AON7508 for main source	2015.04.27	SIT
12	EMI reguest	P46	Add PCI36 for VR_PWRGD	2015.05.29	SIT
13	Change RTC Voltage	P38	Change PR105 form 1k to 1.5k	2015.06.03	SIT
14	Change CPU C and R	P46	Change PRI30 to 86.6K PCI19 to 82P PRI42 to 59K PCI21 to 8200P	2015.07.14	SVT
15					
16					
17					

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Analog G-enseor bypass to EC	36	Remove RV18,RV23,RV27	2015/03/18	SIV=>SIT
2	Reserve OC pin of U9,U10,U12	35	Add R181,R213,R185 and reserve	2015/03/18	SIV=>SIT
3	Audio codec power plant correction	30	Add RA9(0ohm 0603) to +1.8V power plan for +IOVDD_CODEC option	2015/03/18	SIV=>SIT
4	For solve hang up logo issue	14 9	1.Change RC86 from short pad to 0 ohm and add RC115(0ohm) to 3VALW for +3V_1.8V_HDA option. 2.Add RC116(0ohm) to HDA_SDOUT	2015/03/18	SIV=>SIT
5	Add clip pad and capacitor for RF request	33	Add CLIP1~CLIP11,C1212,C1213,C1217,C1218	2015/04/16	SIV=>SIT
6	Delete capacitor for RF requestment	18	1.Remove CD10,CD12,CD14,CD17,CD5,CD6,CD7,CD21 2.Add CD21,CD31,CD32(10U 0402) leave them empty. 3.Change CD13,CD15,CD16,CD18,CD19,CD20 of pakage from 0603 to 0402.	2015/04/16	SIV=>SIT
7	For 2+3E power	17	Modify +1.0VS_VCCOPCP power	2015/04/20	SIV=>SIT
8	Crystal vendor recommend load capacitance	20 10 10	1. CV36, CV37 modify to 12pF 2. CC4, CC5 modify to 15pF YC2(32.678kMZ 12.5PF) change to 32.678kMZ 9PF and CC4,CC5 change to 8.2PF	2015/04/20	SIV=>SIT
9	For ESD requestment	10 36	Add CA46,CA47,CA48,CA49 and reserve	2015/05/12	SIV=>SIT
10	Crystal vendor recommend load capacitance	20	CV36, CV37 modify to 15pF	2015/07/13	SIT=>SVT
11	For RF requestment	14 14 9	1.Remove RC86,CC52,CC53 2.LC1 change pakage form 0603 to0402 3.+3V_1.8V_HDA net change to +3VALW	2015/07/13	SIT=>SVT
12	for MFG requestment remove co-lay	29 35	Remove R196,R222,L13,L15,R227,R229,L17,L18,LH8,LH9,LH10,LH11	2015/07/13	SIT=>SVT

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Size: Custom	Document Number: LA-C311P			Rev: 0.3
Date: Friday, August 07, 2015	Sheet 52 of 52			