Compal Confidential

A940 Schematics Document

INTEL Coffeelake-S CPU with DDR4 + AMD GPU(R17M-G1-50)

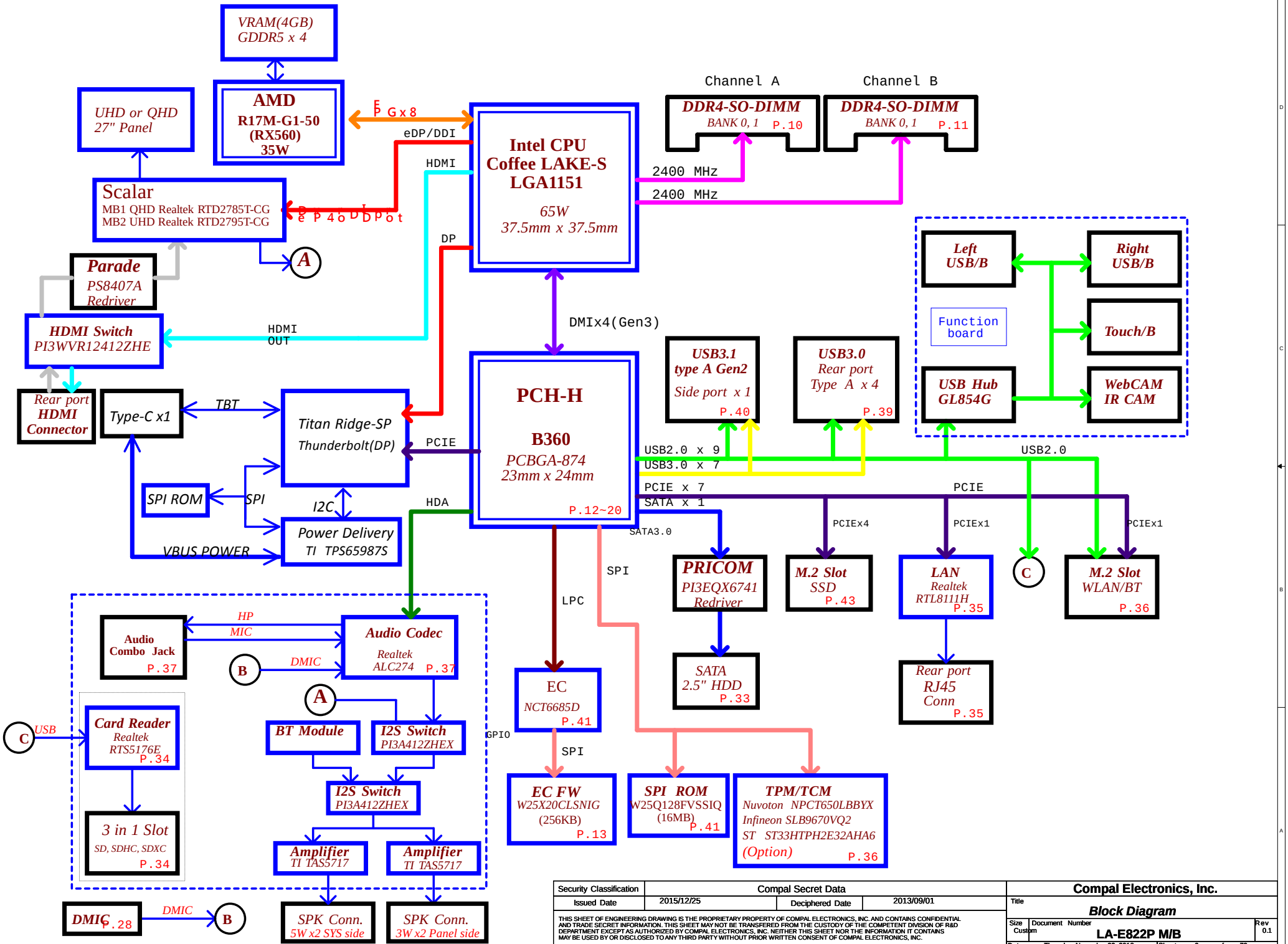
AIO M/B

12/21 , 2018

REV : 1.0

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.		
Title: *Cover Page*		
Size: Custom	Document Number: LA-E822P M/B	Rev: 0.1
Date: Monday, November 26, 2018	Sheet 1 of 73	



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Title: **Block Diagram**

Size	Document Number	Rev
Custom	LA-E822P M/B	0.1

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PCIE Port Table

No.	Port	Device
6	12	LAN
7	13	WLAN
17	23	TBT
18	24	TBT
19	25	TBT
20	26	TBT
21	27	SSD
22	28	SSD
23	29	SSD
24	30	SSD

SATA Port Table

No.	Port	Device
0	19	HDD
1	20	
2	21	
3	22	
4	23	
5	24	

DDI Port Table

No.	Port	Device
1	DDI1	HDMI OUT
2	DDI2	TBT
3	DDI3	NC

USB2.0 Port Table

Port	Device	OC#
1	USB3.1 Gen1 Rear IO Port 1	OC#0
2	USB3.1 Gen1 Rear IO Port 2	OC#1
3	USB3.1 Gen1 Rear IO Port 3	OC#2
4	USB3.1 Gen1 Rear IO Port 4	OC#3
5	USB3.1 Gen1 SIDE IO TYPE-C	NA
6	USB3.1 Gen2 SIDE IO TYPE-A	OC#4
7	TO SB Board	NA
8	Card Reader	NA
9	TBT_PD	NA
10	NC	NA

USB3.0 Port Table

No.	Port	Device
1	1	USB3.0 (Rear IO)
2	2	USB3.0 (IO Board Port 1)
3	3	NC
4	4	NC
5	5	USB3.0 (IO Board Port 2)
6	6	NC

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+DC20V	AC or battery power rail for power circuit.	N/A	N/A	N/A
+RTCVCC_S5	RTC power	ON	ON	ON*
+3V3_DSW	3.3V DSW on power rail	ON	ON	ON*
+3VALW_S5	3.3V always on power rail	ON	ON	ON
+5VALW_S5	5V always on power rail	ON	ON	ON
+12VALW_S5	12V always on power rail	ON	ON	ON
+1.8VS_S0	1.8V always on power rail	ON	OFF	OFF
+1.0VALW_S5	1.0V always on power rail	ON	ON	ON
+1.0V_VCCST_S3	1.0V power rail for CPU VCCST	ON	ON	OFF
+1.2V_VDDQ_S3	1.2V power rail for DDR4	ON	ON	OFF
+2.5V_S3	2.5V power rail for DDR4	ON	ON	OFF
+CPU_VCCIO_S0	0.95V power rail for CPU VCCIO	ON	OFF	OFF
+5VS_S0	5V switched power rail	ON	OFF	OFF
+3VS_S0	3.3V switched power rail	ON	OFF	OFF
+12VS_S0	12V switched power rail	ON	OFF	OFF
+1.05VS_S0	+1.5VS on power rail for CPU VCCSA	ON	OFF	OFF
+CPU_CORE	VCC Core voltage for CPU	ON	OFF	OFF
+VCC_GT_S0	Core voltage for CPU graphic	ON	OFF	OFF
+3VS_DGPU_S0	3.3V power rail for DIS graphic	ON	OFF	OFF
+VGA_CORE_S0	VCC Core voltage for GPU	ON	OFF	OFF
+1.05VS_DGPU_S0	1.05V power rail for DIS graphic	ON	OFF	OFF
+1.35VS_VGA_S0	1.35V power rail for VRAM	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

BOM Structure Table

BOM Structure	BTO Item

SKU ID(Project) Table

SKU (Only DIS)	C7 DVT QHD BOM Configure Table
431ADS38L01 SAMSUNG 4G (DIS)	
431ADS38L02 MICRON 4G (DIS)	
X4EADS38L01	
X7679238L01 SAMSUNG 4G	SAMSUNG - SA000092D10 S IC D5 256M32 K4G80325FB-HC28 FBGA 170P
X7679238L02 HYNIX 4G	HYNIX - SA00009U150 S IC D5 256M32 H5GC8H24AJR-R0C BGA 170P
X7679238L03 MICRON 4G	MiCRON - SA00009TV60 S IC D5 256M32 MT51J256M32HF-70:B FBGA

EC SM Bus0 Address

Device	Address	HEX
Converter RTD-2136N	0110-0010xb	62
GPU	1001-1110xb	9E

EC SM Bus2 Address

Device	Address	HEX
Scalar RTD-2506S	1001-0100xb	94
LCD Backlight		

PCH SM Bus Address

Device	Address	HEX
DDR(JDIMM1)	WRITE:0xA0	READ: 0xA1
DDR(JDIMM2)	WRITE:0xA4	READ: 0xA5

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Title: Notes List

Size: C | Document Number: LA-E881P M/B | Rev: 0.1

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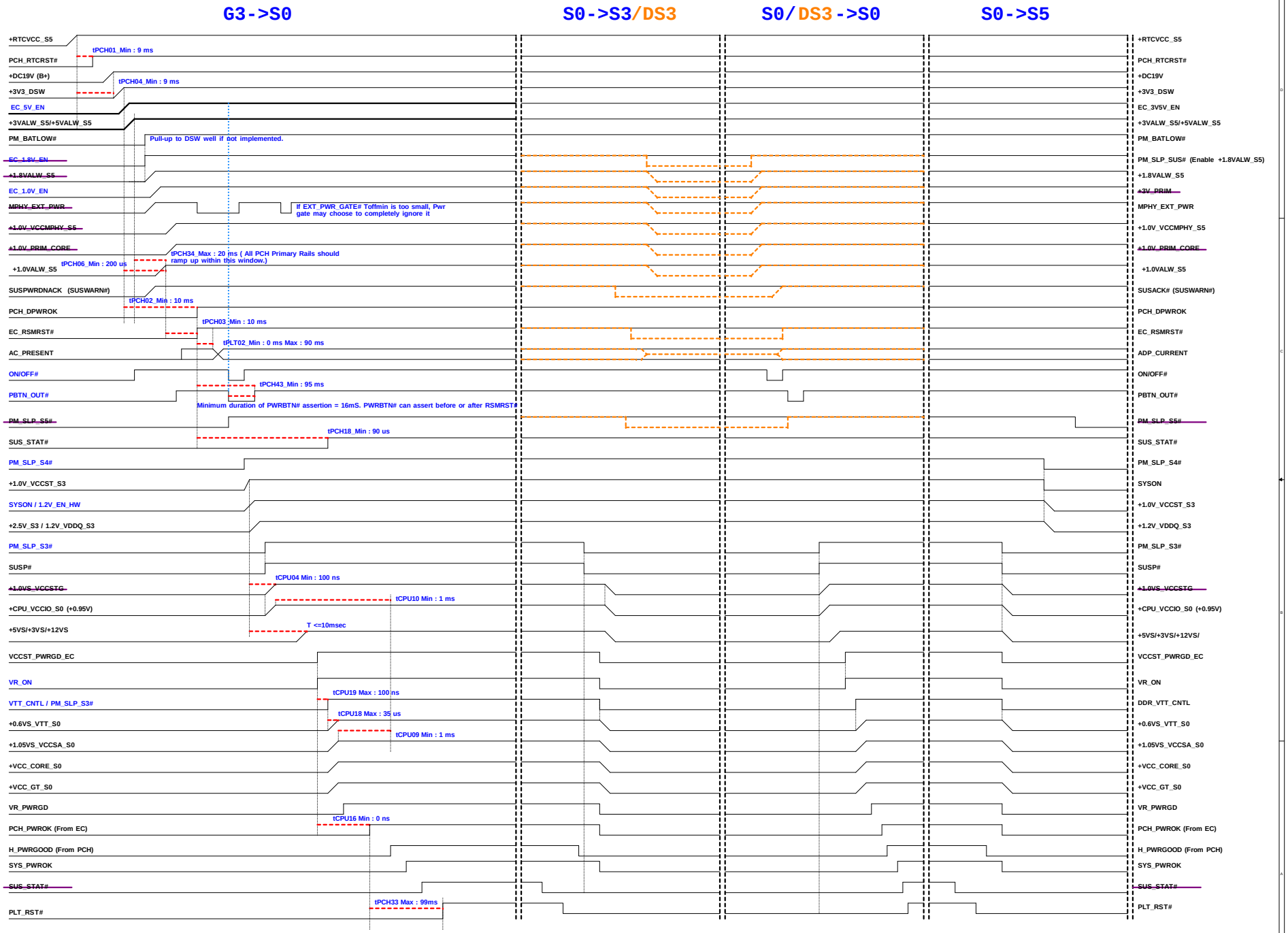
Power Sequence_SKL-S [Deep Sx Platform]



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Issued Date	2015/12/25	Deciphered Date	2013/09/01
Title	PWR Sequence		
Size: Custom	Document Number: LA-E881P M/B		Rev: 0.1
Date: Thursday, November 22, 2018	Sheet 4 of 73		

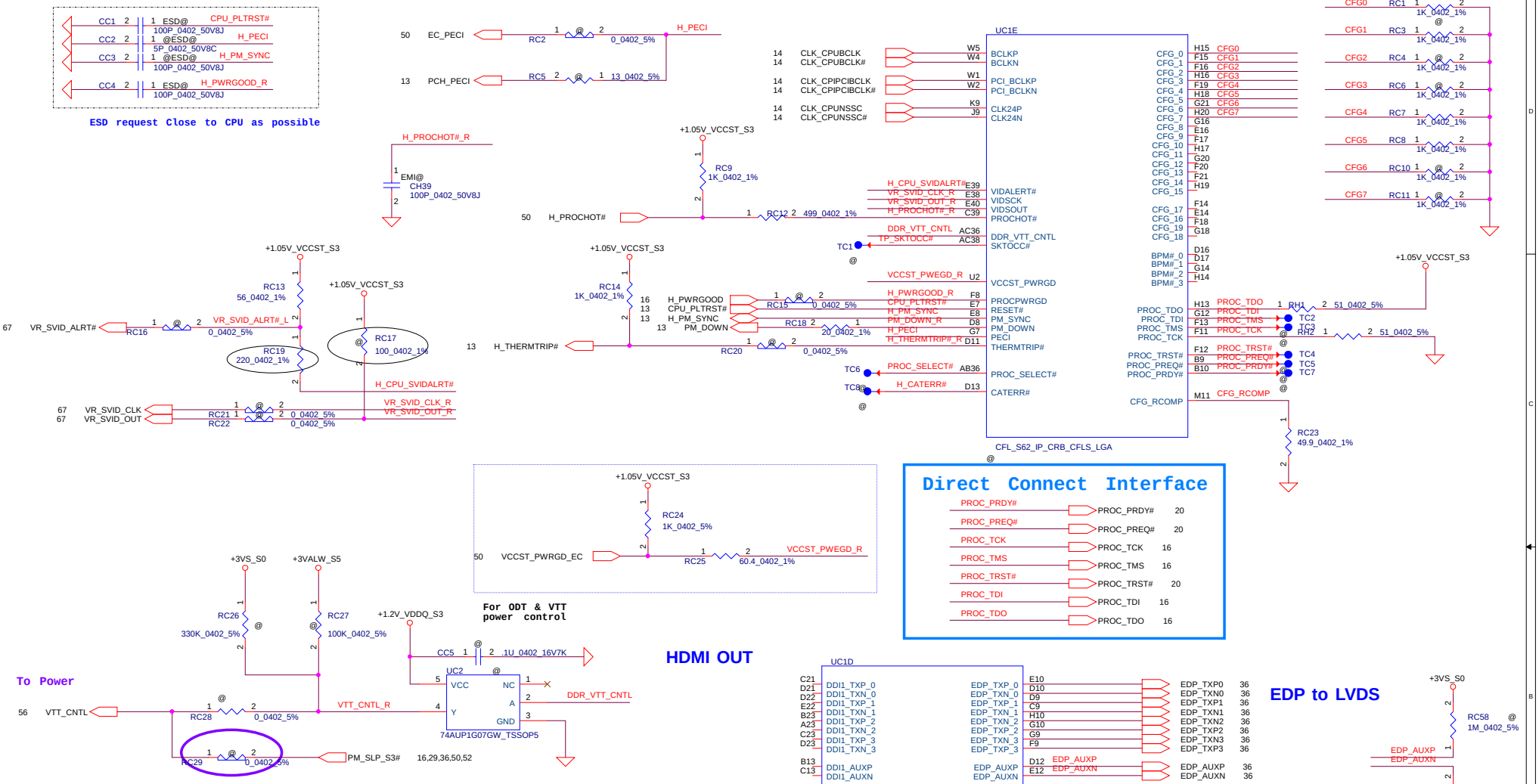

Table 7-1. Mapping of HDMI* Signals for DDI Ports

Port	Digital Display Interface Pins	CRB Digital Display Interface Signals	HDMI* Signals
Port 1	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIx_TX2_DP
	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIx_TX2_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIx_TX1_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIx_TX1_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIx_TX0_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIx_TX0_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIx_CLK_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIx_CLK_DN
	Hot plug detect used by HDMI Port 1	DDPB_HPD	DDI1_HPD_Q
	HDMI DDC lines for Port 1	DDPB_CTRLCLK	DDI1_CTRL_CK
		DDPB_CTRLDATA	DDI1_CTRL_DATA

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Title: *Skylake JTAG/XDP/DDI*

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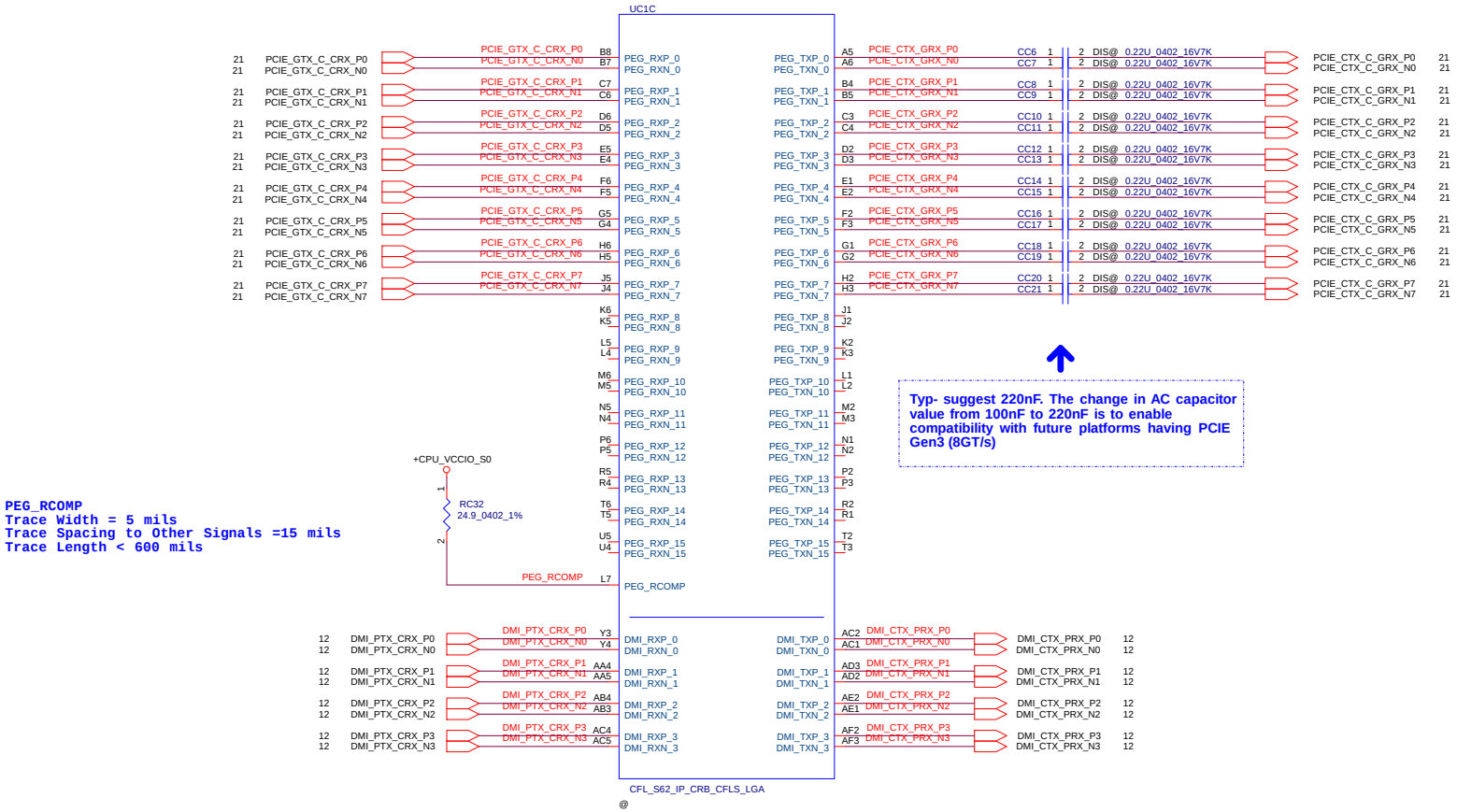

Security Classification	Compal Secret Data		
Issued Date	2012/09/01	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***Skylake DMI/PEG/FDI***

Size	Document Number	Rev
Custom	LA-F901P M/B	0.1

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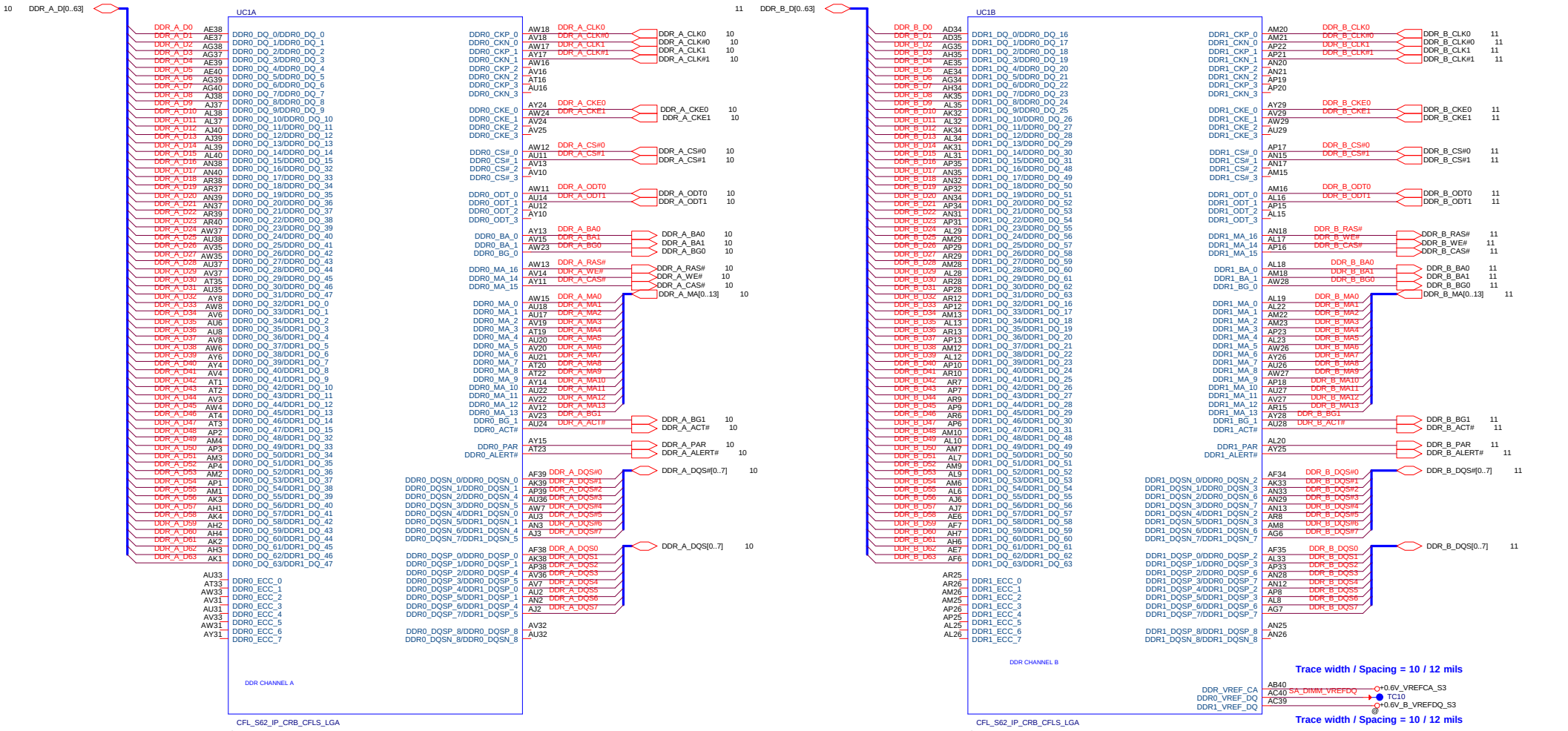

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

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Title: ***Skylake DDR4***

Size	Document Number	Rev
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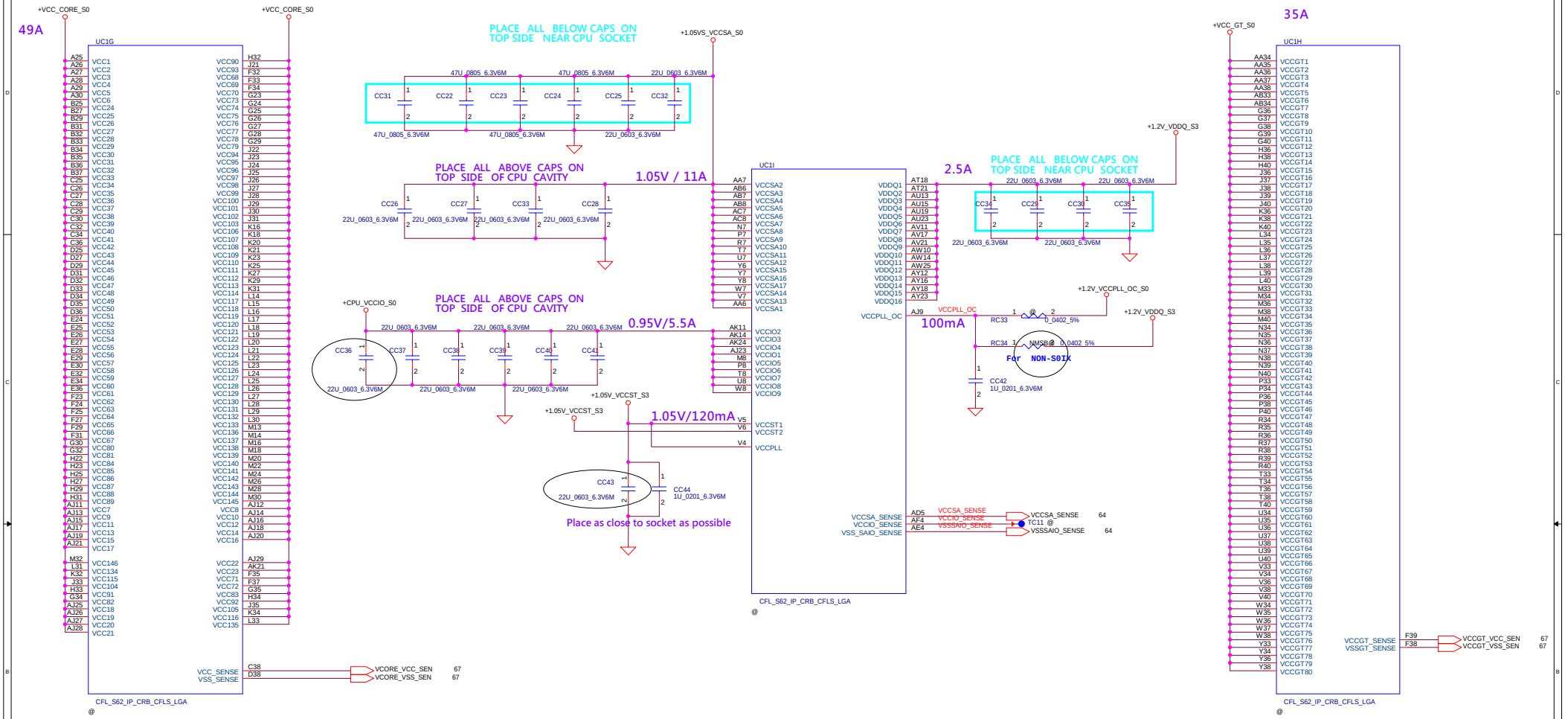
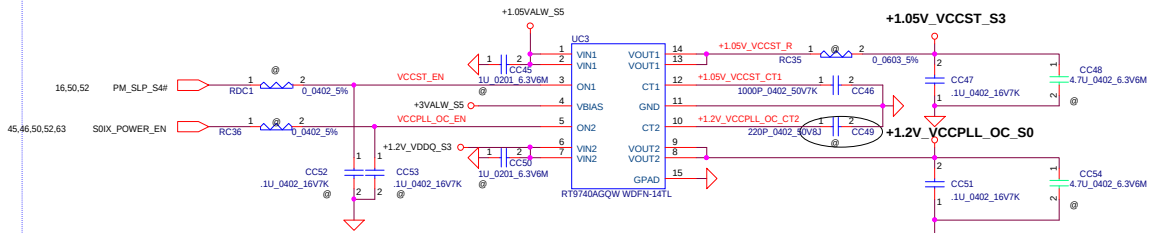


VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm

+1.05VALW_S5 to +1.05V_VCCST



1st source : RT9740AGQW (SA00007VD00)
2nd source : TPS22966DPUR (SA00004MM00)

+1.2V_VDDQ_S3 to +1.2V_VCCPLL_OC

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Title: Skylake POWER

Size: C | Document Number: LA-F901P M/B | Rev: 0.1

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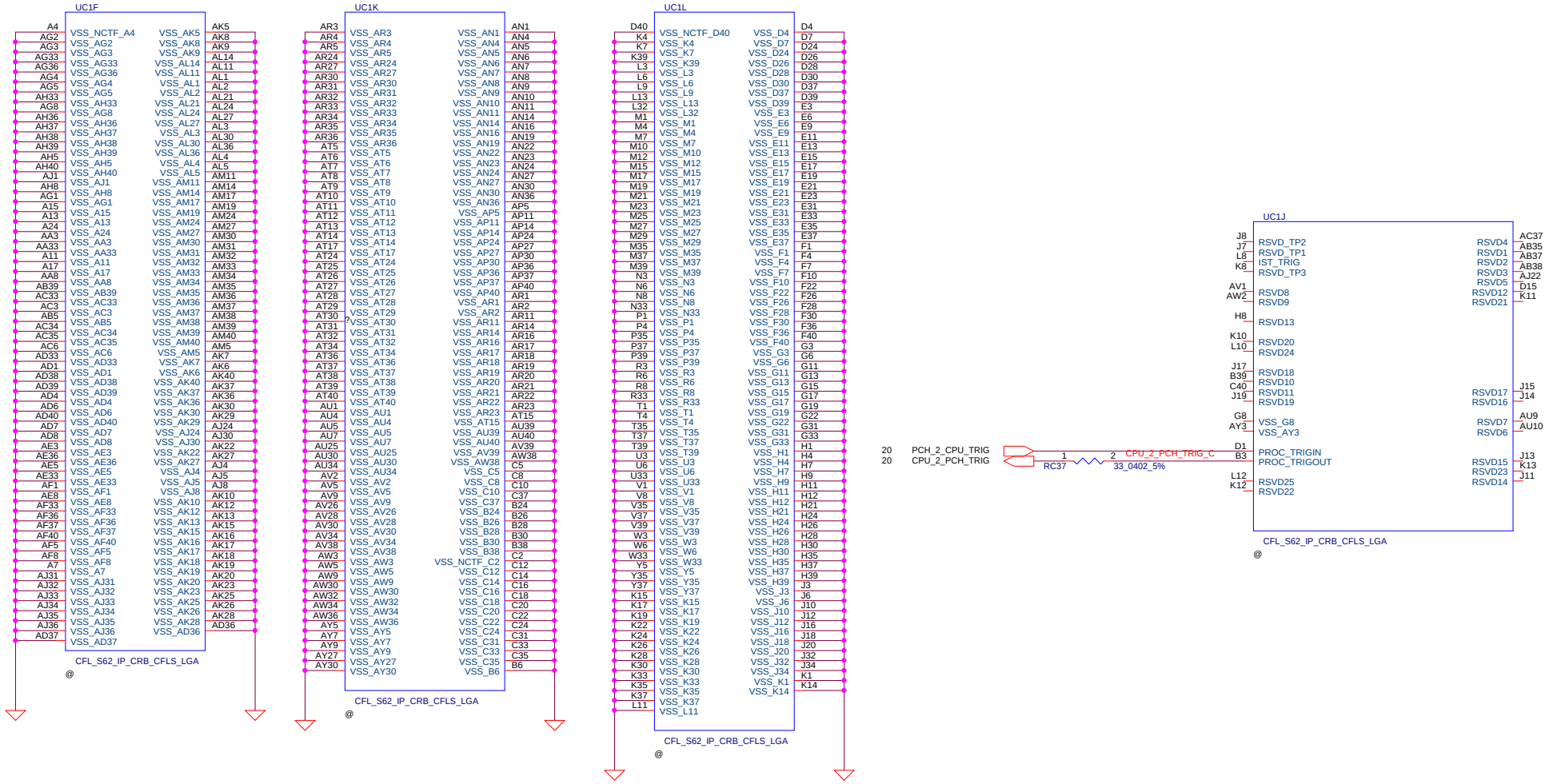

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Title: ***Skylake GND/RSVD***

Size	Document Number	Rev
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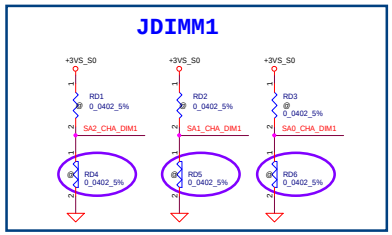
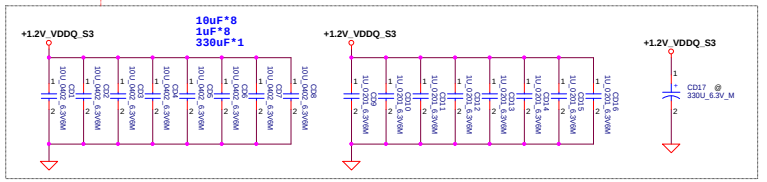
INTERLEAVE
CHANNEL-A



PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

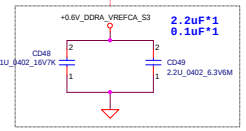
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS:0xA0
READ ADDRESS: 0xA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

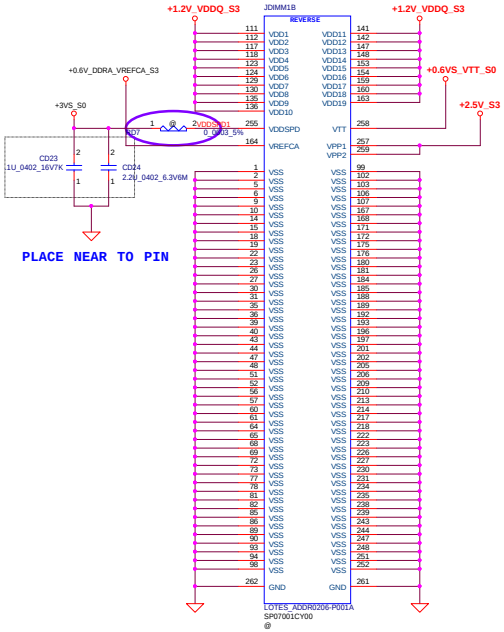
Layout Note:
Place near JDIMM1



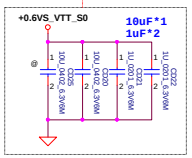
(4.0 mm) Reverse Type

Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM1

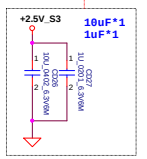


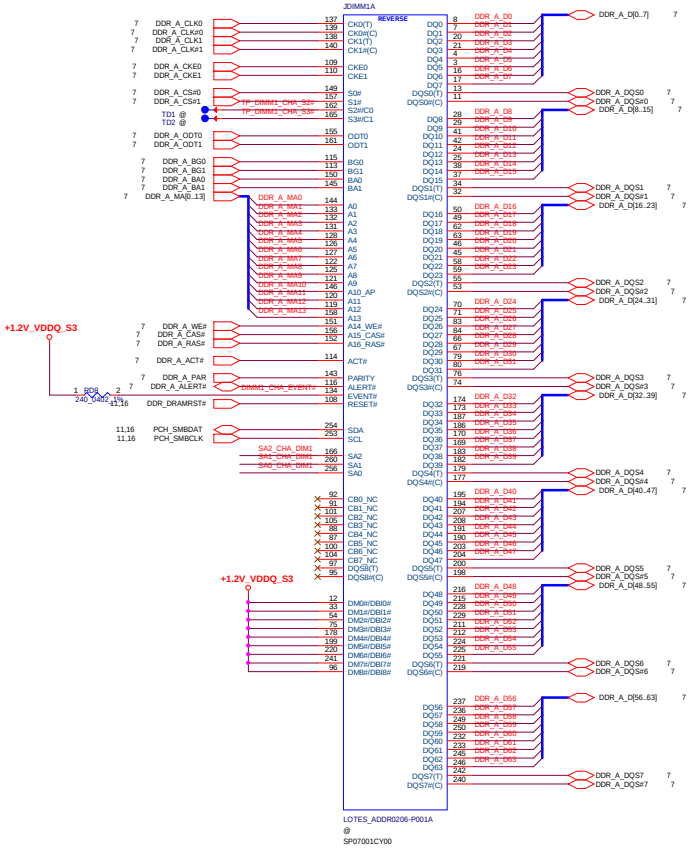


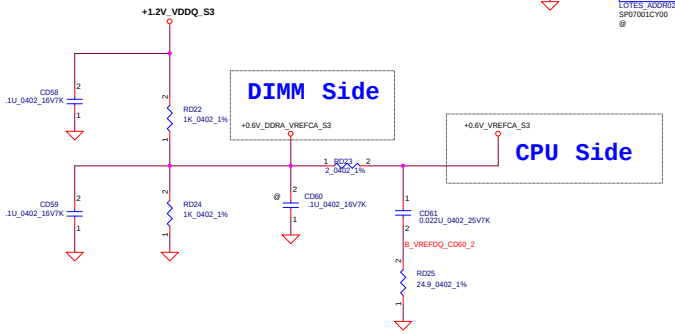
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1







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Title: DDR4 DIMMB

Size: Custom | Document Number: LA-F901P M/B | Rev: 0.1

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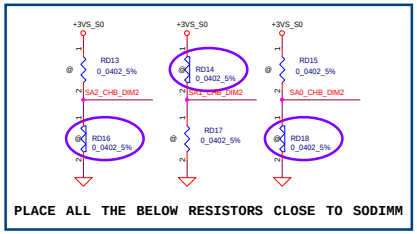
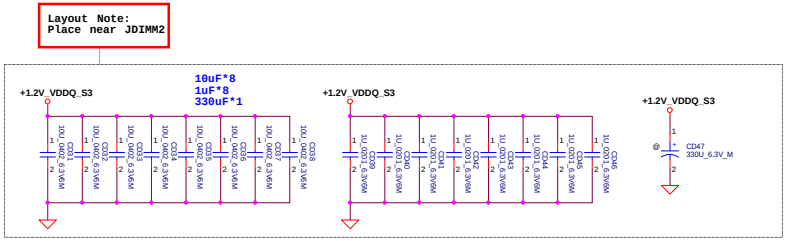
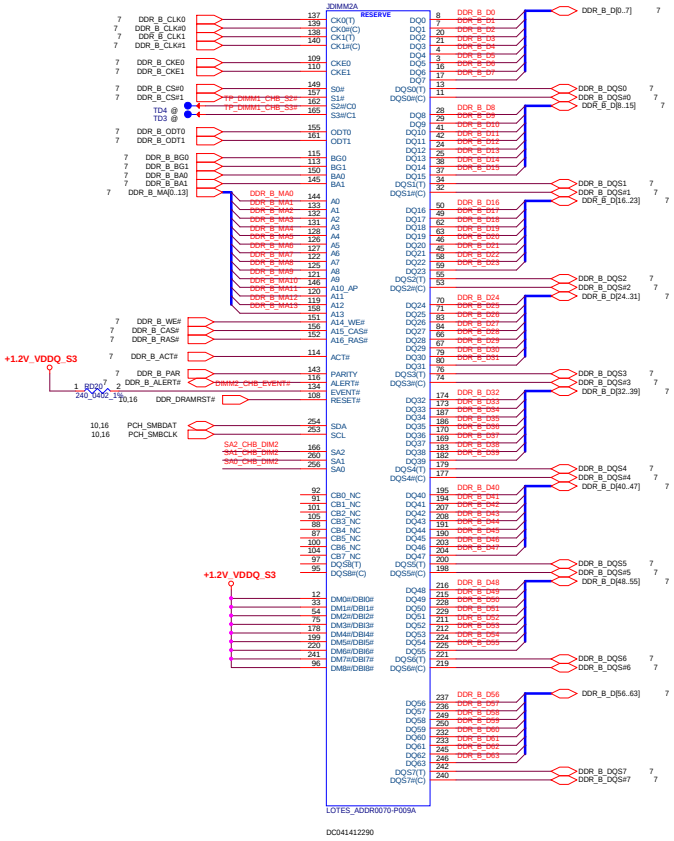
INTERLEAVE CHANNEL-B

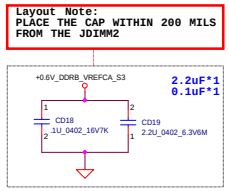


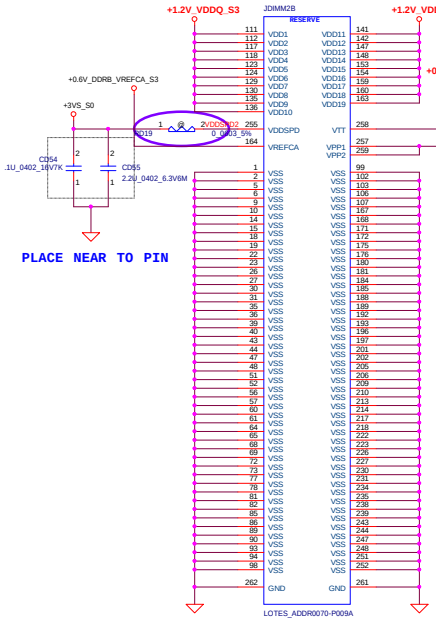
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS:0xA4
READ ADDRESS: 0xA5
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

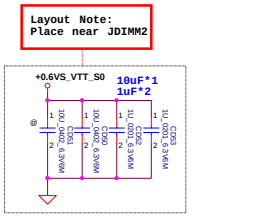


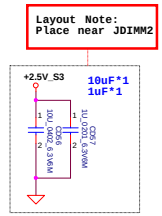
(8.0 mm) Reverse Type

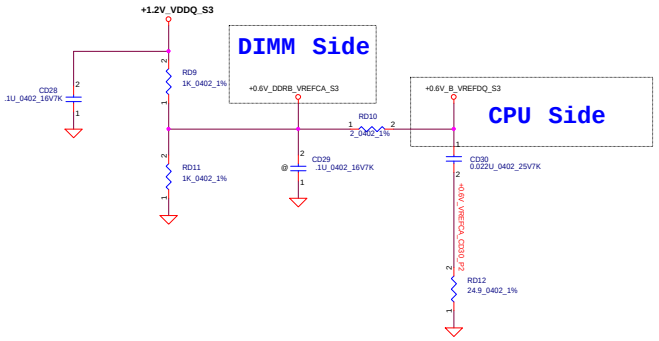


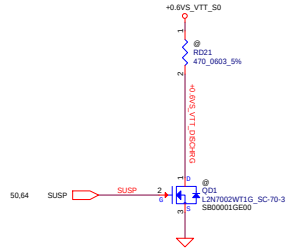












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Compal Electronics, Inc.			
Title: DDR4_DIMMA			
Size: Custom	Document Number: LA-F901P M/B		Rev: 0.1
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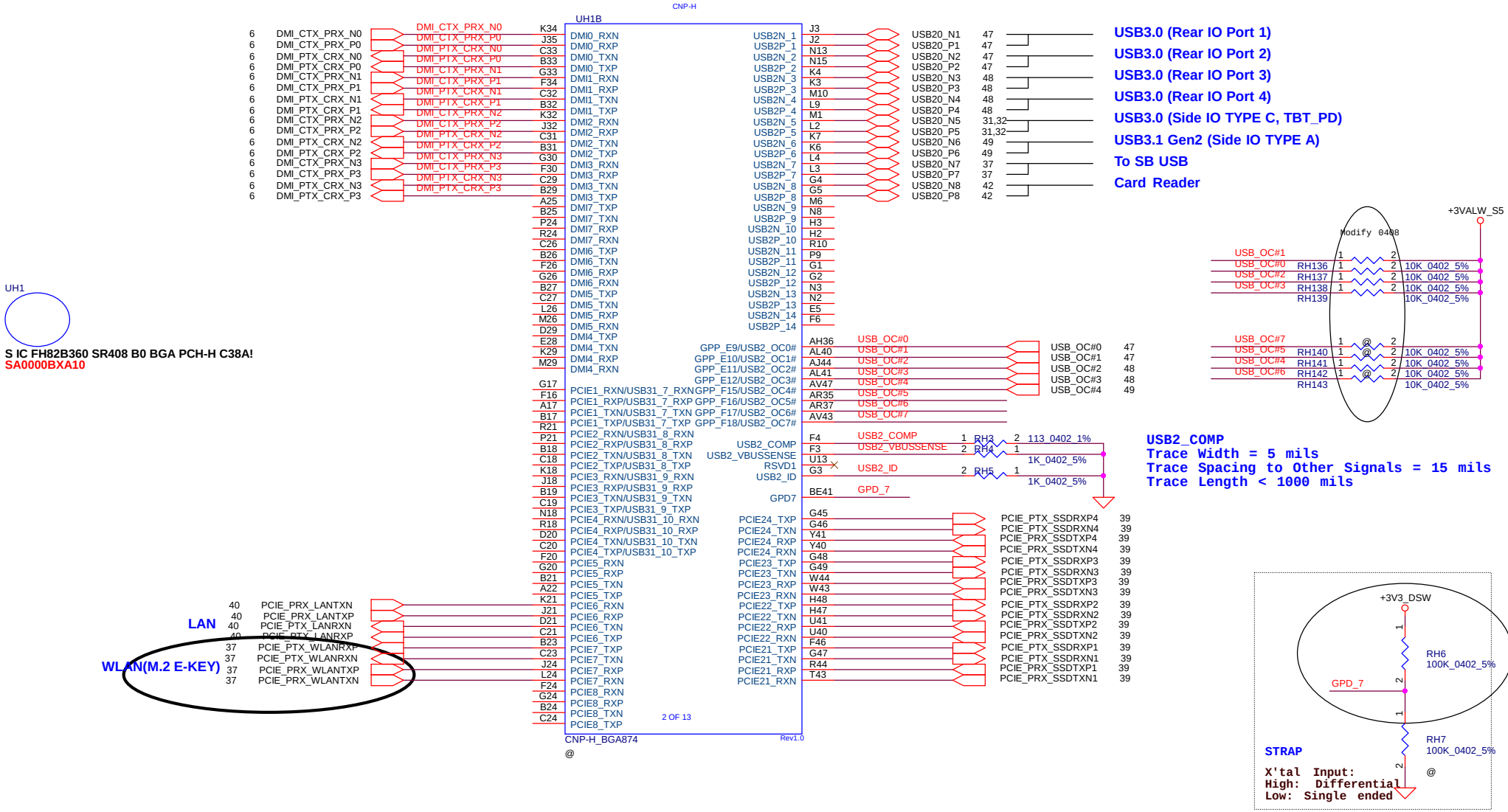

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

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Title: *PCH_DMI/USB2/PCIE*

Size	Document Number	Rev
B	LA-F901P M/B	0.1

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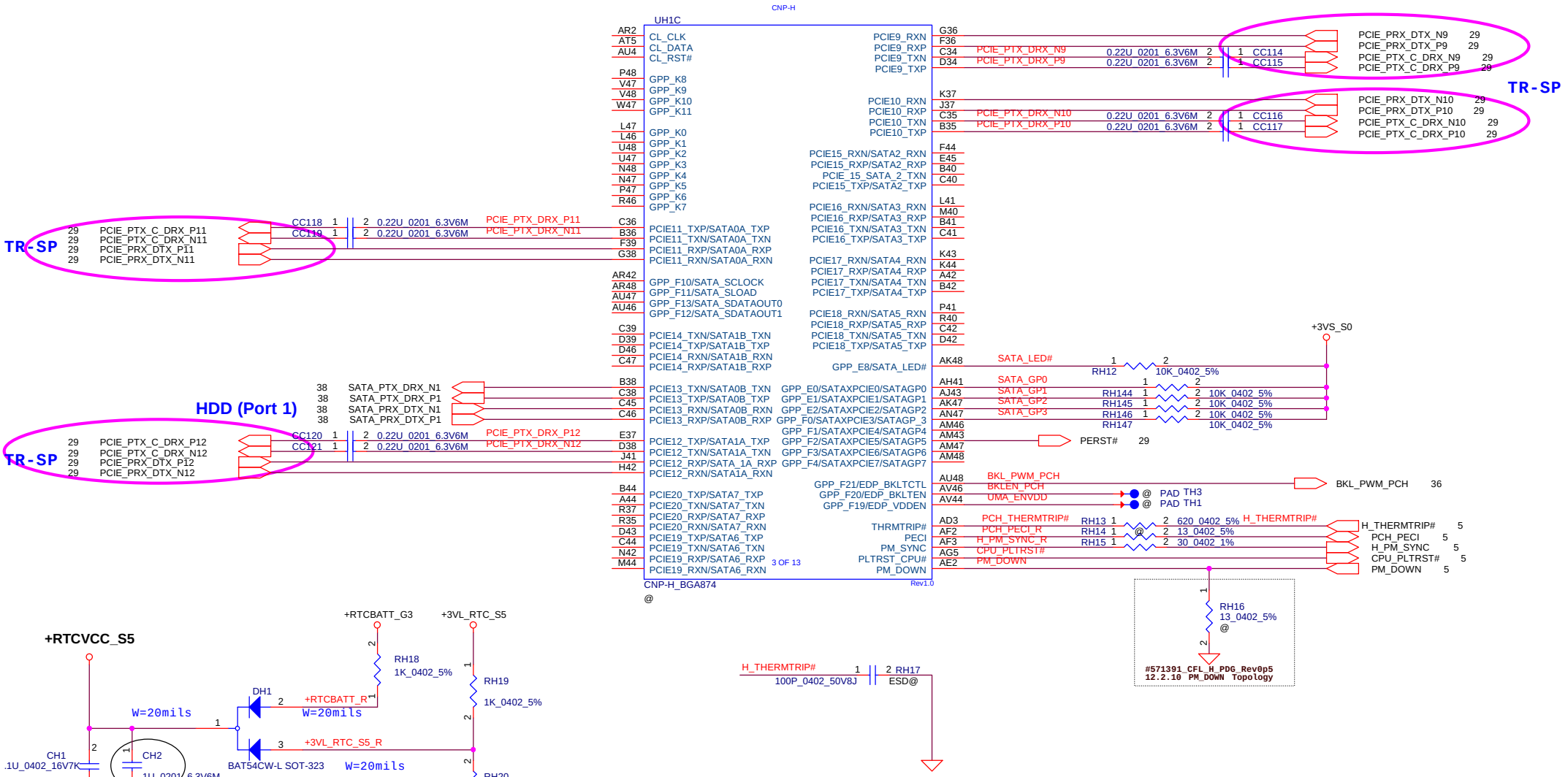

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***PCH_HDA/JTAG/SATA***

Size	Document Number	Rev
B	LA-F901P M/B	0.1

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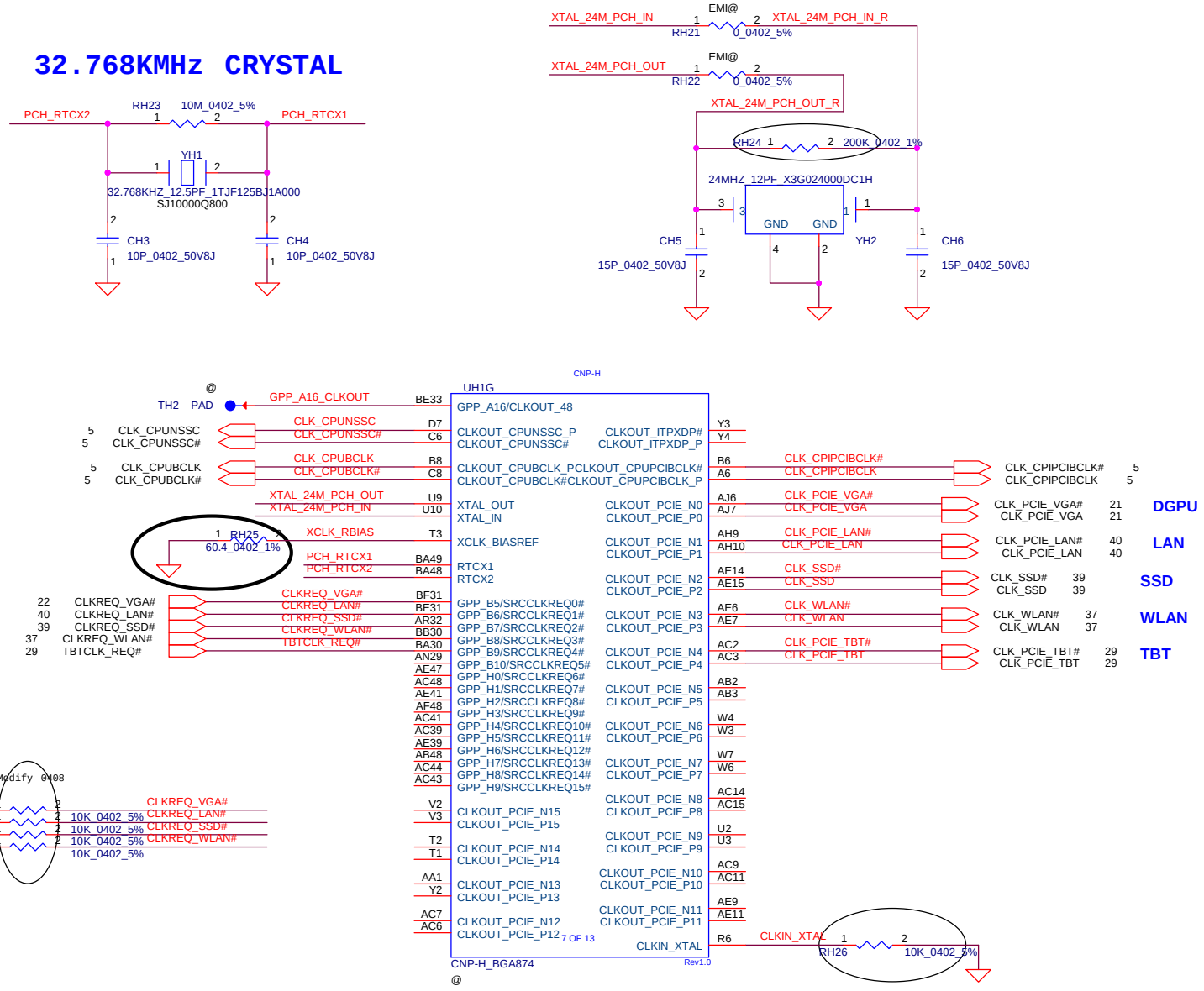

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

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Title: *PCH_CLK\LPC\SPI\SMBUS*

Size	Document Number	Rev
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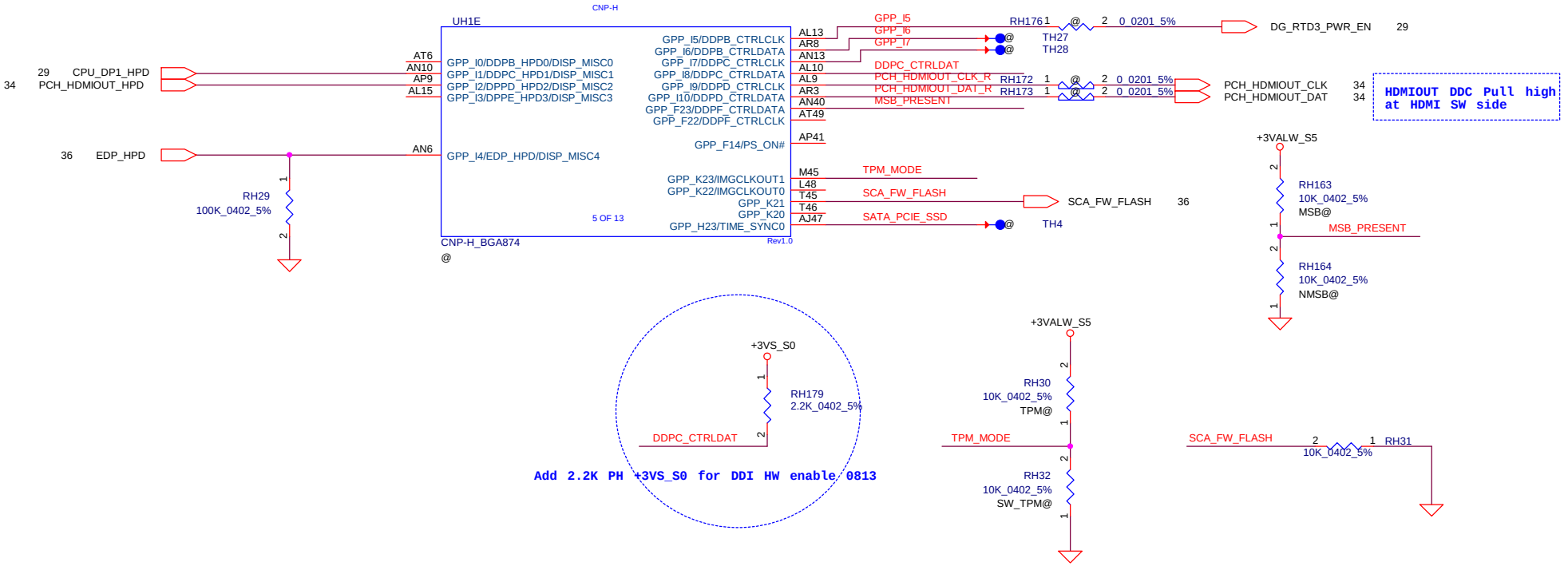
DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B is not detected. (Default)
1 = Port B is detected.
Notes:
1. The internal Pull-down is disabled after PCH_PWROK de-asserts.
2. This signal is in the primary well.



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Title: ***PCH_CRT/DDC***

Size	Document Number	Rev
B	LA-F901P M/B	0.1

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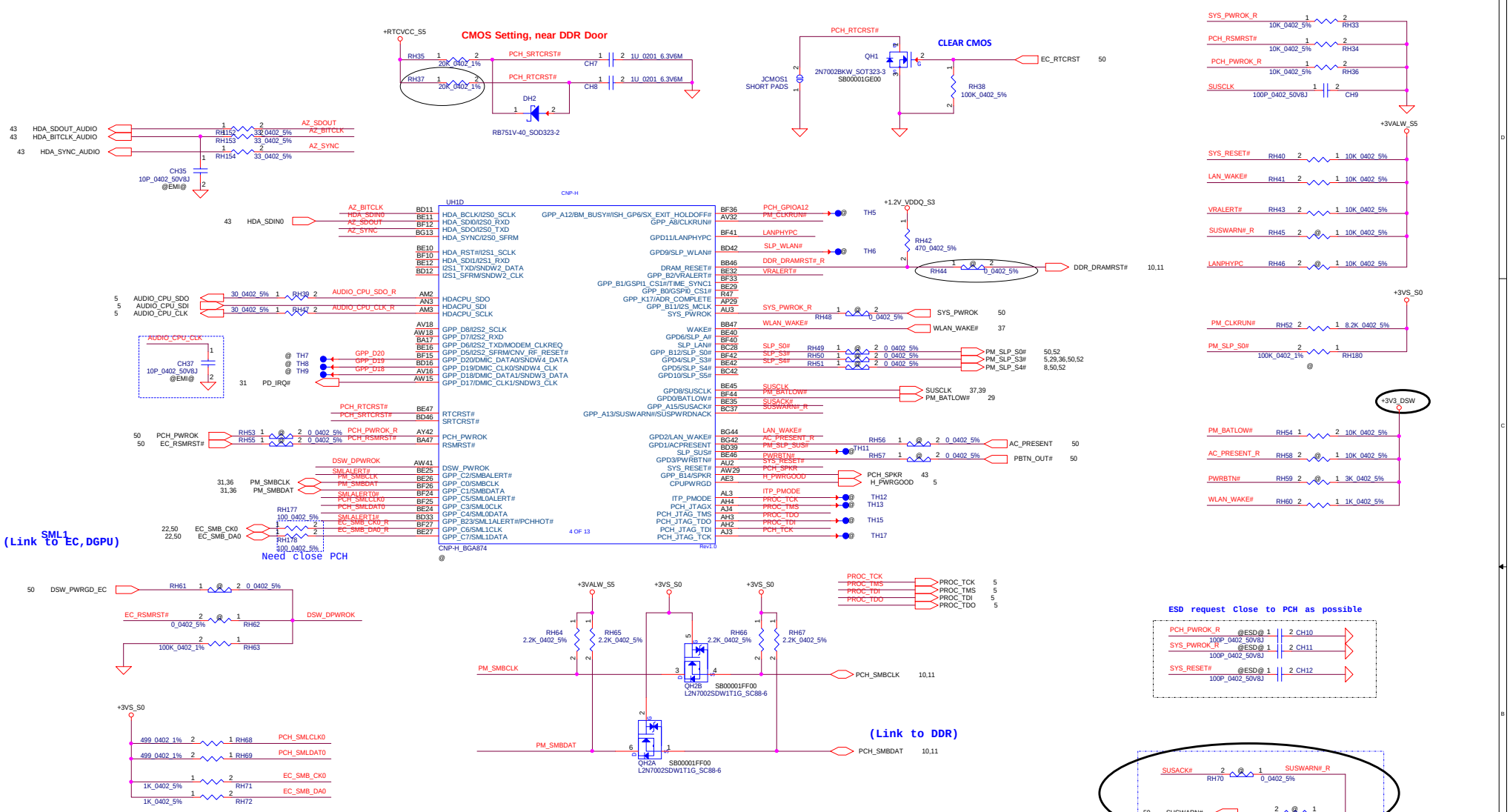

Functional Strap Definitions

SMLALERT#
This signal has a weak internal Pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Functional Strap Definitions

SMLALERT0#
This signal has a weak internal Pull-down.
0 = LPC is selected (for EC 9022).
1 = eSPI is selected (for EC 9042). (Default)
Notes:
1. The internal Pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

SMLALERT1#
This signal has an internal pull-down.
0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.

Strap Pin

Top Swap Override
0 = Disable " Top Swap" mode (Default)
1 = Enable " Top Swap" mode
The internal Pull-down is disabled after PCH_PWROK is high.

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: *PCH_HDA\SMBUS\PM*

Size: C | Document Number: LA-F901P M/B | Rev: 0.1

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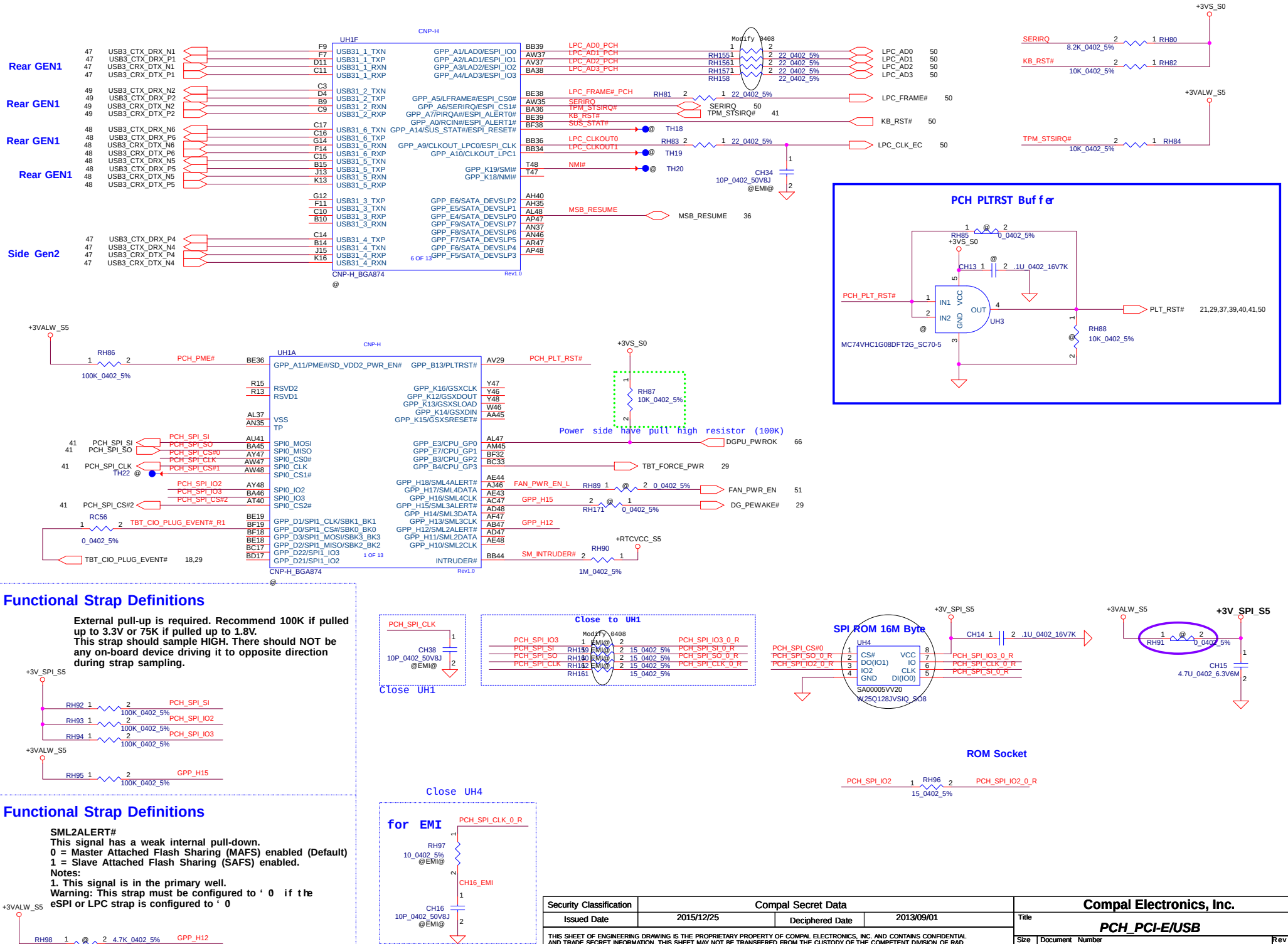
Rear GEN1
Rear GEN1
Rear GEN1
Rear GEN1
Side Gen2
UH1F
CNP-H
CNP-H_BGA874
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Rev1.0
LPC_AD0_PCH
LPC_AD1_PCH
LPC_AD2_PCH
LPC_AD3_PCH
LPC_FRAME#_PCH
SERIRQ
TPM_STSIRQ#
KB_RST#
SUS_STAT#
LPC_CLKOUT0
LPC_CLKOUT1
NMI#
MSB_RESUME
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
KB_RST#
LPC_CLK_EC
MSB_RESUME
TH18
TH19
TH20
CH34
10P_0402_50V8J
@EMI@
+3VS_S0
+3VALW_S5
SERIRQ
KB_RST#
TPM_STSIRQ#
8.2K_0402_5%
10K_0402_5%
RH80
RH82
RH84
PCH PLTRST Buffer
PCH_PLT_RST#
PLT_RST#
MC74VHC1G08DFT2G_SC70-5
UH3
RH85
RH88
CH13
.1U_0402_16V7K
UH1A
PCH_PME#
RH86
100K_0402_5%
PCH_SPI_SI
PCH_SPI_SO
PCH_SPI_CS#0
PCH_SPI_CLK
PCH_SPI_CS#1
PCH_SPI_IO2
PCH_SPI_IO3
PCH_SPI_CS#2
TH22
RC56
TBT_CIO_PLUG_EVENT#_R1
TBT_CIO_PLUG_EVENT#
0_0402_5%
Power side have pull high resistor (100K)
RH87
10K_0402_5%
DGPU_PWROK
TBT_FORCE_PWR
FAN_PWR_EN_L
FAN_PWR_EN
DG_PEWAKE#
RH89
RH171
GPP_H15
GPP_H12
SM_INTRUDER#
RH90
1M_0402_5%
+RTCVCC_S5
Functional Strap Definitions
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
+3V_SPI_S5
RH92
RH93
RH94
RH95
100K_0402_5%
+3VALW_S5
Functional Strap Definitions
SML2ALERT#
This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled (Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.
Notes:
1. This signal is in the primary well.
Warning: This strap must be configured to ' 0 if the eSPI or LPC strap is configured to ' 0
RH98
4.7K_0402_5%
Close UH1
Close to UH1
CH38
10P_0402_50V8J
@EMI@
15_0402_5%
Close UH4
for EMI
RH97
10_0402_5%
CH16_EMI
CH16
SPI ROM 16M Byte
UH4
SA00005VV20
W25Q128JVSIQ_SO8
CH14
CH15
4.7U_0402_6.3V6M
ROM Socket
RH96
Security Classification
Compal Secret Data
Issued Date
2015/12/25
Deciphered Date
2013/09/01
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Title
PCH_PCI-E/USB
Size
Custom
Document Number
LA-F901P M/B
Rev
0.1
Date:
Thursday, November 22, 2018
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17
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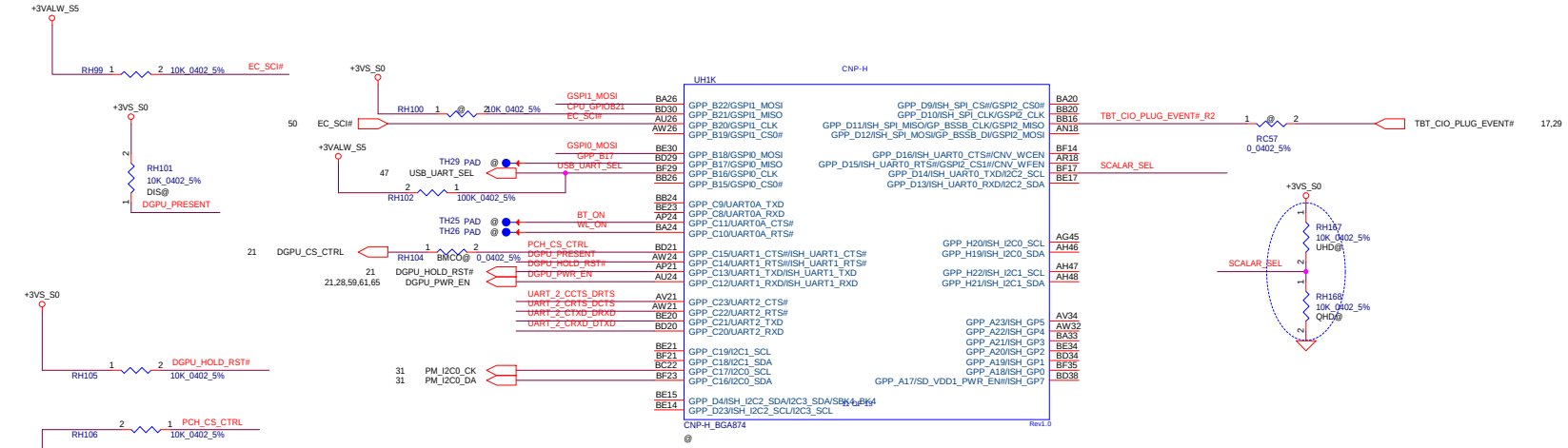
73



Functional Strap Definitions

GSPI0_MOSI
The signal has a weak internal Pull-down.
0 = Disable "No Reboot" mode (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
Notes:
1. The internal Pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

GSPI1_MOSI
This Signal has a weak internal Pull-down.
0: SPI (Default)
1: LPC
Notes:
1. The internal Pull-down is disabled after PCH_PWROK is high.
2. This signal is in the primary well.

Strap Pin

Intel® 300 Series Chipset Preliminary HSIO Lane Assignments

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
USB 3.1 Gen 1 / Gen 2 #1	USB 3.1 Gen 1 / Gen 2 #2	USB 3.1 Gen 1 / Gen 2 #3	USB 3.1 Gen 1 / Gen 2 #4	USB 3.1 Gen 1 / Gen 2 #5	USB 3.1 Gen 1 / Gen 2 #6	USB 3.1 Gen 1 #7	USB 3.1 Gen 1 #8	USB 3.1 Gen 1 #9	USB 3.1 Gen 1 #10	PCIe 3.0 #5	PCIe 3.0 #6	PCIe 3.0 #7	PCIe 3.0 #8	PCIe 3.0 #9	PCIe 3.0 #10	PCIe 3.0 #11	PCIe 3.0 #12	PCIe 3.0 #13	PCIe 3.0 #14	PCIe 3.0 #15	PCIe 3.0 #16	PCIe 3.0 #17	PCIe 3.0 #18	PCIe 3.0 #19	PCIe 3.0 #20	PCIe 3.0 #21	PCIe 3.0 #22	PCIe 3.0 #23	PCIe 3.0 #24
						PCIe 3.0 #1	PCIe 3.0 #2	PCIe 3.0 #3	PCIe 3.0 #4	GbE (LAN)				GbE (LAN)		SATA #01	SATA #11 / GbE (LAN)	SATA #0 / GbE (LAN)	SATA #1	SATA #2	SATA #3	SATA #4	SATA #5						
						x4				x4				x4				x4				x4				x4			
						x2		x2		x2		x2		x2				x2		x2		x2				x2		x2	
						No Remapping				No Remapping				Intel® RST for PCIe Storage				No Remapping				Intel® RST for PCIe Storage				Intel® RST for PCIe Storage			

SKU

H310	USB3.1 Gen 1	USB3.1 Gen 1	USB3.1 Gen 1	USB3.1 Gen1	N/A	N/A	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	LAN Only	N/A	PCIe	PCIe LAN	SATA LAN	SATA	SATA	SATA	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B360	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1 / Gen 2	USB3.1 Gen 1	USB3.1 Gen 1	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	SATA LAN	SATA	SATA	SATA	SATA	SATA	N/A	N/A	PCIe	PCIe	PCIe	PCIe

SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14.

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Title	PCH_UART/I2C		
Size C	Document Number LA-F901P M/B		Rev 0.1
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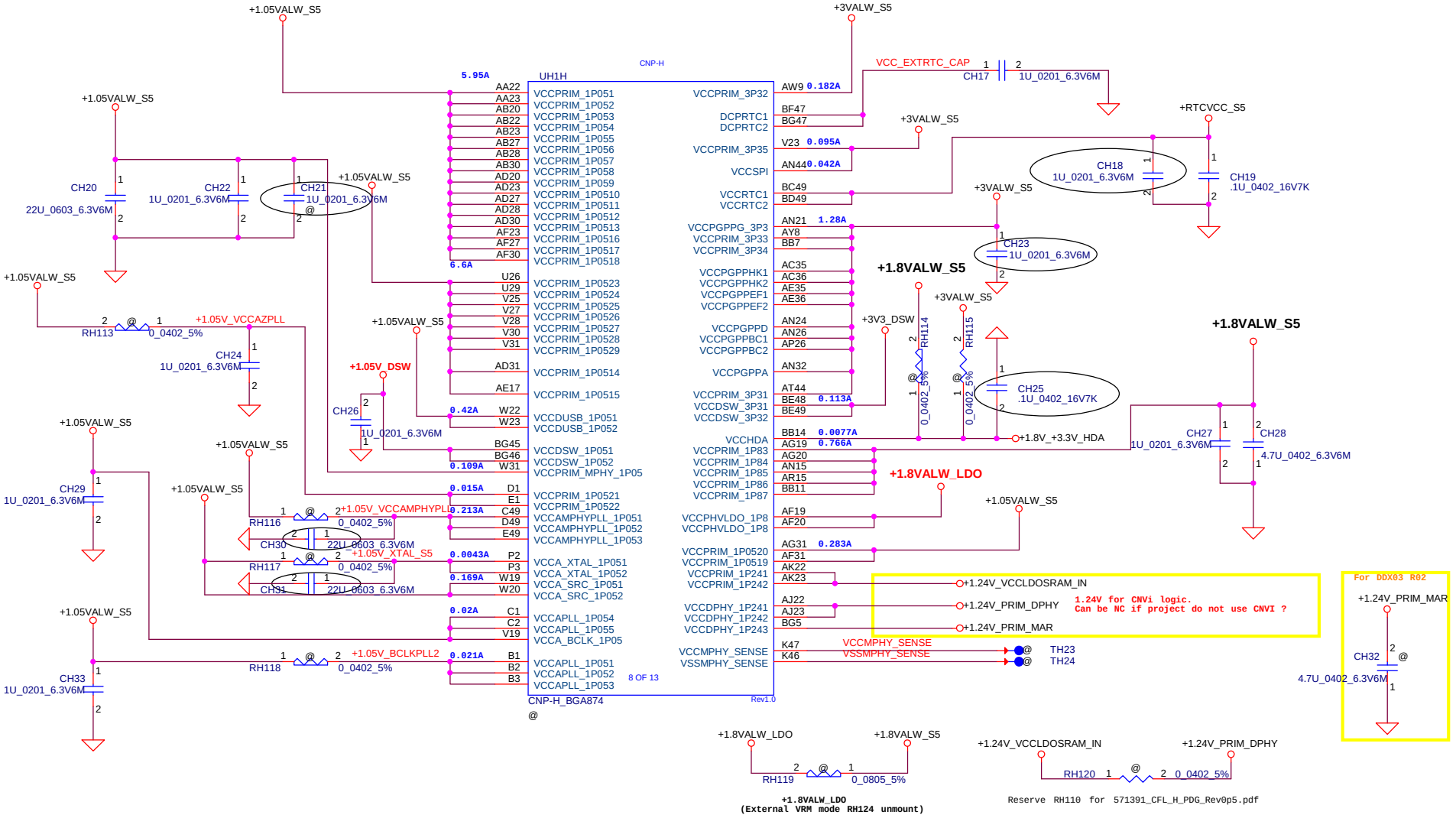

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Title: ***PCH_POWER***

Size	Document Number	Rev
B	LA-F901P M/B	0.1

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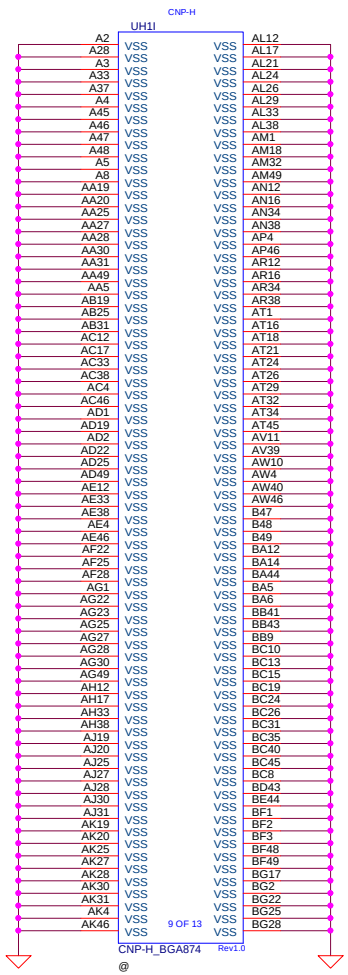

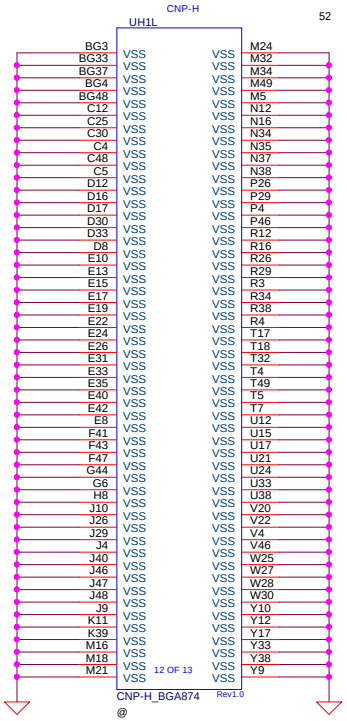

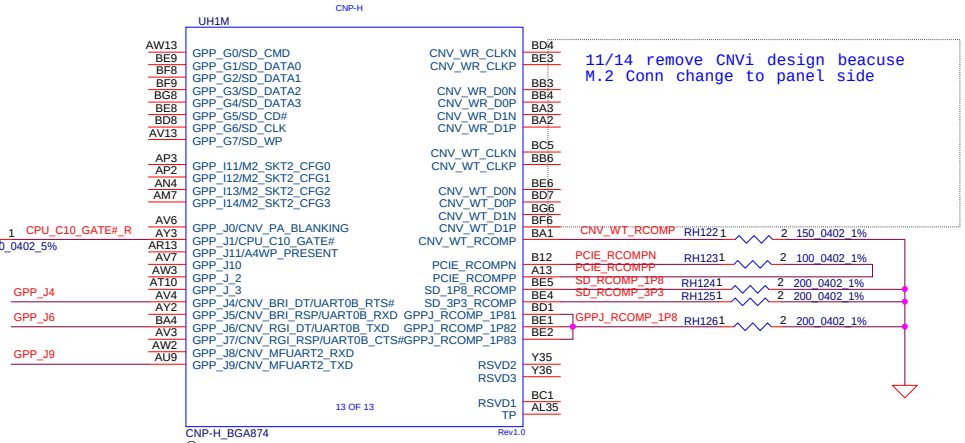

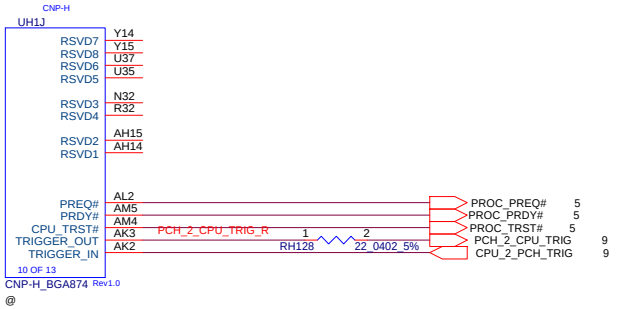

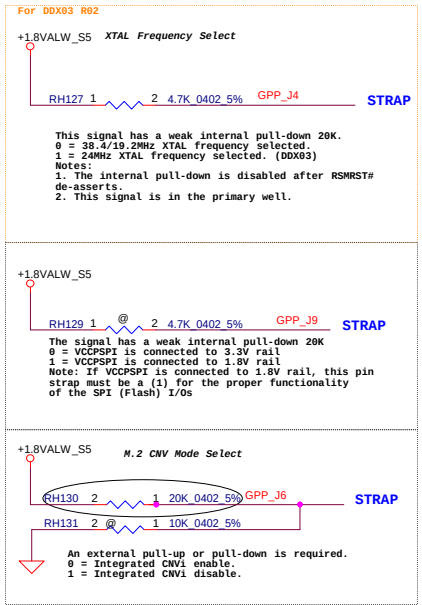

Table 18-1. GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group G (GPP_G)	VCCPGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H) Primary Well Group K (GPP_K)	VCCPGPPHK	1.8V or 3.3V
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSW_3P3	3.3V Only

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

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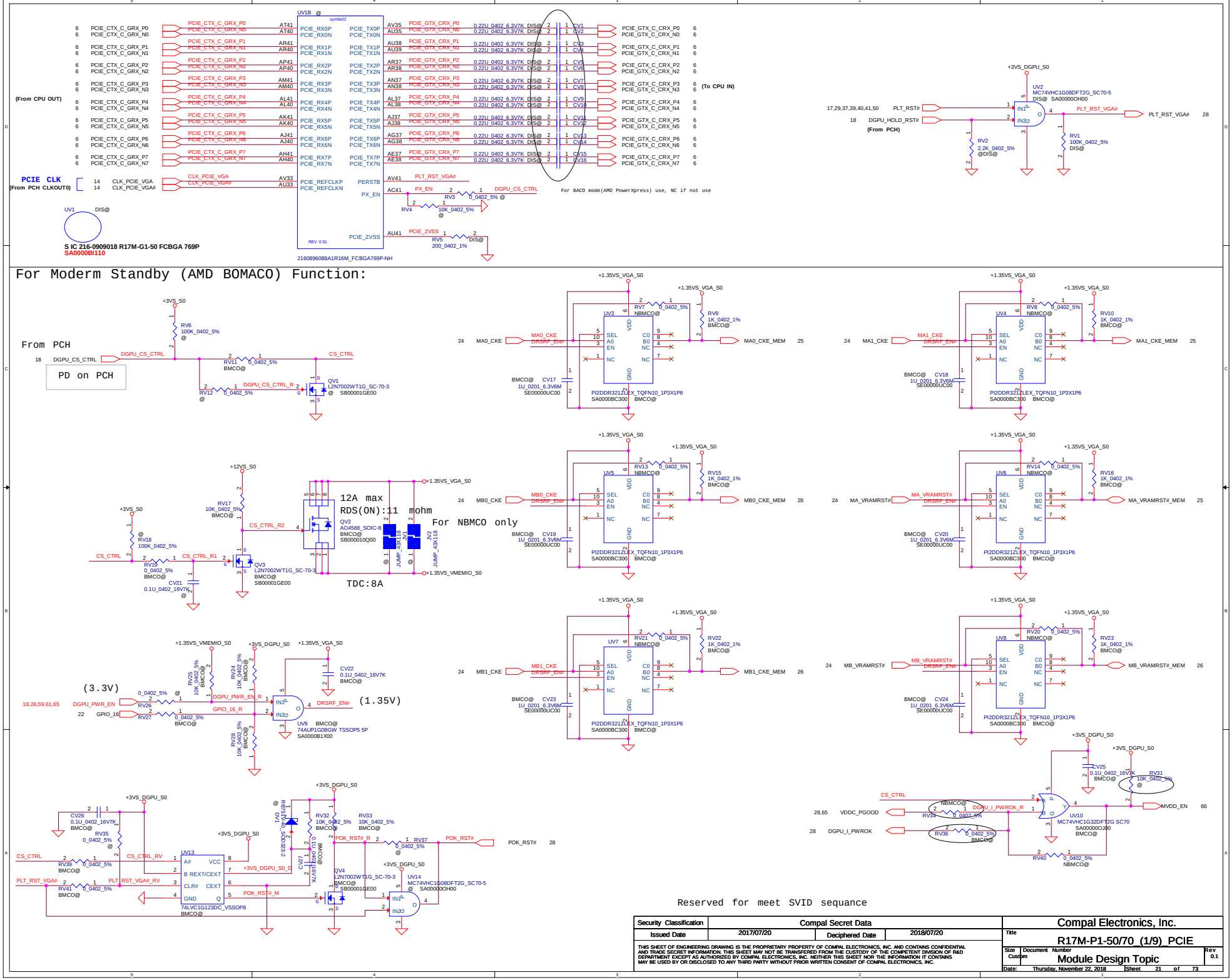

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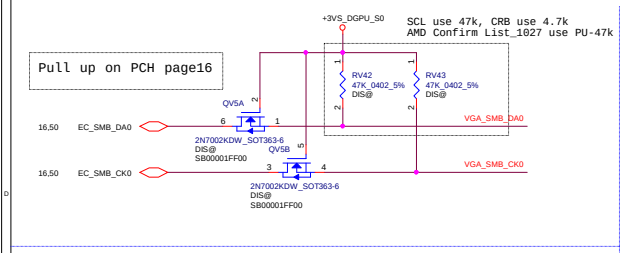
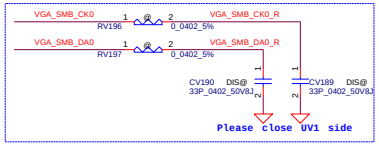
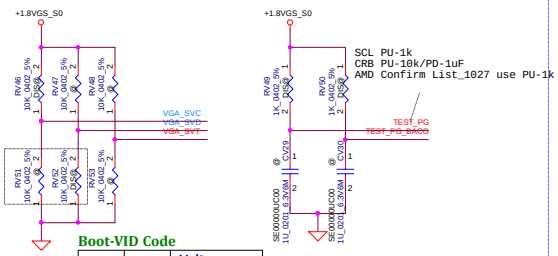
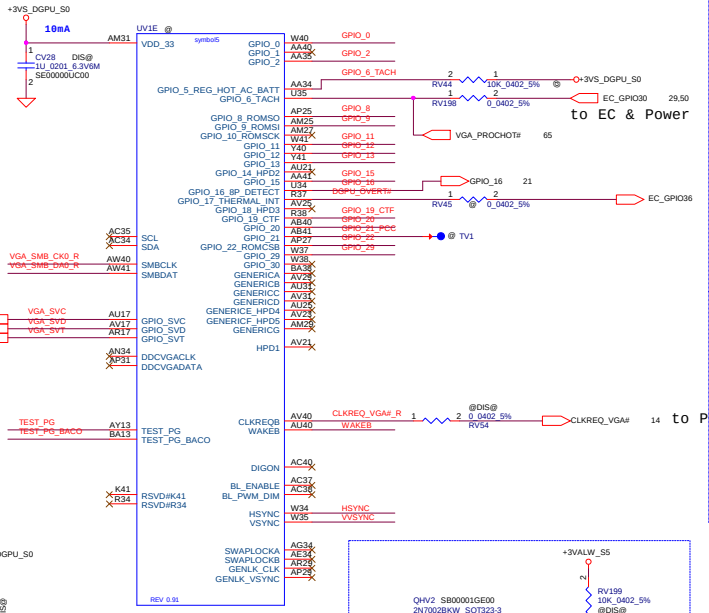


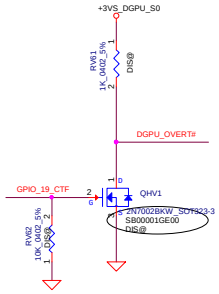


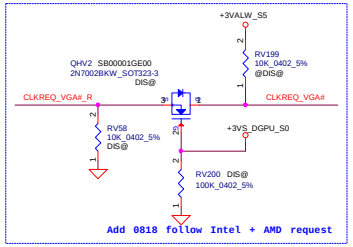


Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8







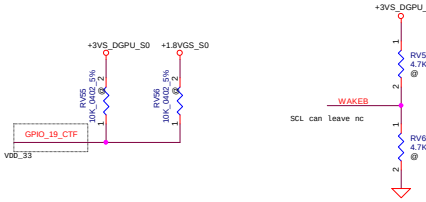
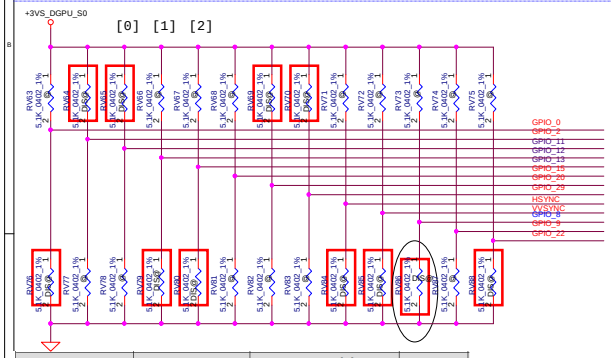


Table 5–2 Regulator Guidelines

Rail Name		Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDDC	"R17M-P1-50" 18W	0.700 V to 0.887 V	VID_VDDCI_VDDC × 0.6 mΩ ± 20 mV	Overshoot: 120 mV Undershoot: 90 mV	20 A (TDC) 50 A (EDC)	1, 4, 8
	"R17M-P1-50" 25W	0.700 V to 0.963 V			30 A (TDC) 60 A (EDC)	
	"R17M-P1-50" 35W	0.700 V to 1.075 V			40 A (TDC) 70 A (EDC)	
	"R17M-P1-70" 25W	0.700 V to 1.000 V			30 A (TDC) 70 A (EDC)	
	"R17M-P1-70" 40W	0.700 V to 1.144 V			45 A (TDC) 92 A (EDC)	
	"R17M-M2-70"	0.700 V to 0.800 V			16 A (TDC) 35 A (EDC)	



BIF_GEN3_EN_A	GPIO_2	PCIe Gen3 capability. 1: PCIe Gen3 is supported. 0: PCIe Gen3 is not supported.	1 (Internal pull-up)	
BIF_CLK_PM_EN	GPIO_8_ROMSO	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0: The CLKREQB power management capability is disabled. 1: The CLKREQB power management capability is enabled.	0 (Internal pull-down)	1 Provide a pull-up resistor option to VDD_33 on the PCB.

Table 3–27 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

VRAM 4 pcs total 4GB

3.22.2 ROM Configurations

For designs that have a dedicated ROM device for the GPU video BIOS:

- Use the GPU default strap on GPIO_22_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO_13, GPIO_12, and GPIO_11 (i.e., 101).

BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device. 0: Disable external BIOS ROM device. 1: Enable external BIOS ROM device. **Note:** When an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low).	1 (Internal pull-up)	
TX_HALF_SWING	GPIO_0	Controls the transmitter full/half swing mode. 0: The transmitter full-swing is enabled. 1: The transmitter half-swing is enabled.	0 (Internal pull-down)	
BIF_VGA_DIS	GPIO_29	Determine whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space). 0: VGA Controller capacity enabled. 1: The device will not be recognized as the system's VGA controller (for headless designs).	0 (Internal pull-down)	
TX_DEEMPH_EN	GPIO_20	PCI Express transmitter de-emphasis enable 0: Tx de-emphasis disabled. 1: Tx de-emphasis enabled.	0 (Internal pull-down)	1 Through pull-up resistor to VDD_33.

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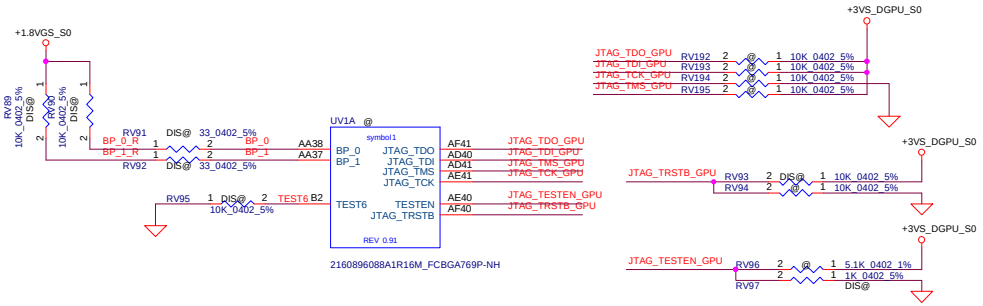

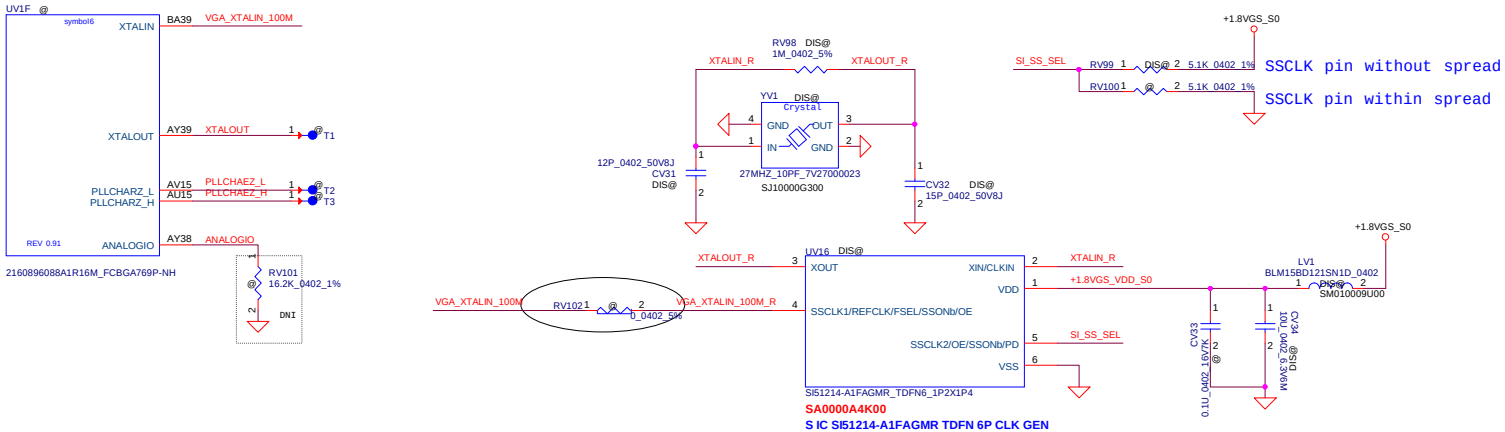

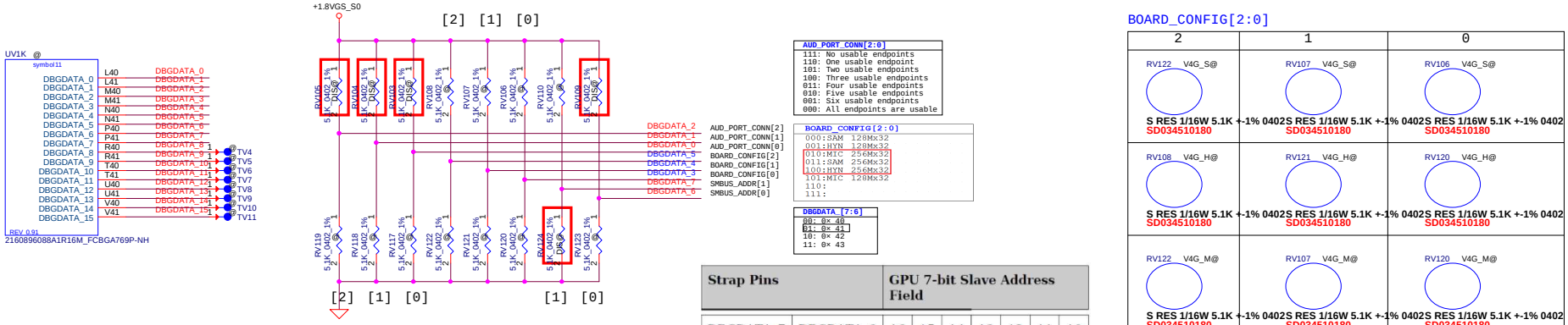

BOARD_CONFIG[2:0]

2	1	0
RV122 V4G_S@ S RES 1/16W 5.1K +-1% 0402 SD034510180	RV107 V4G_S@ S RES 1/16W 5.1K +-1% 0402 SD034510180	RV106 V4G_S@ S RES 1/16W 5.1K +-1% 0402 SD034510180
RV108 V4G_H@ S RES 1/16W 5.1K +-1% 0402 SD034510180	RV121 V4G_H@ S RES 1/16W 5.1K +-1% 0402 SD034510180	RV120 V4G_H@ S RES 1/16W 5.1K +-1% 0402 SD034510180
RV122 V4G_M@ S RES 1/16W 5.1K +-1% 0402 SD034510180	RV107 V4G_M@ S RES 1/16W 5.1K +-1% 0402 SD034510180	RV120 V4G_M@ S RES 1/16W 5.1K +-1% 0402 SD034510180

Strap Pins		GPU 7-bit Slave Address Field						
DBGDATA_7	DBGDATA_6	A6	A5	A4	A3	A2	A1	A0
LOW	LOW	1	0	0	0	0	0	0
LOW	HIGH	**1**	**0**	**0**	**0**	**0**	**0**	**1**
HIGH	LOW	1	0	0	0	0	1	0
HIGH	HIGH	1	0	0	0	0	1	1

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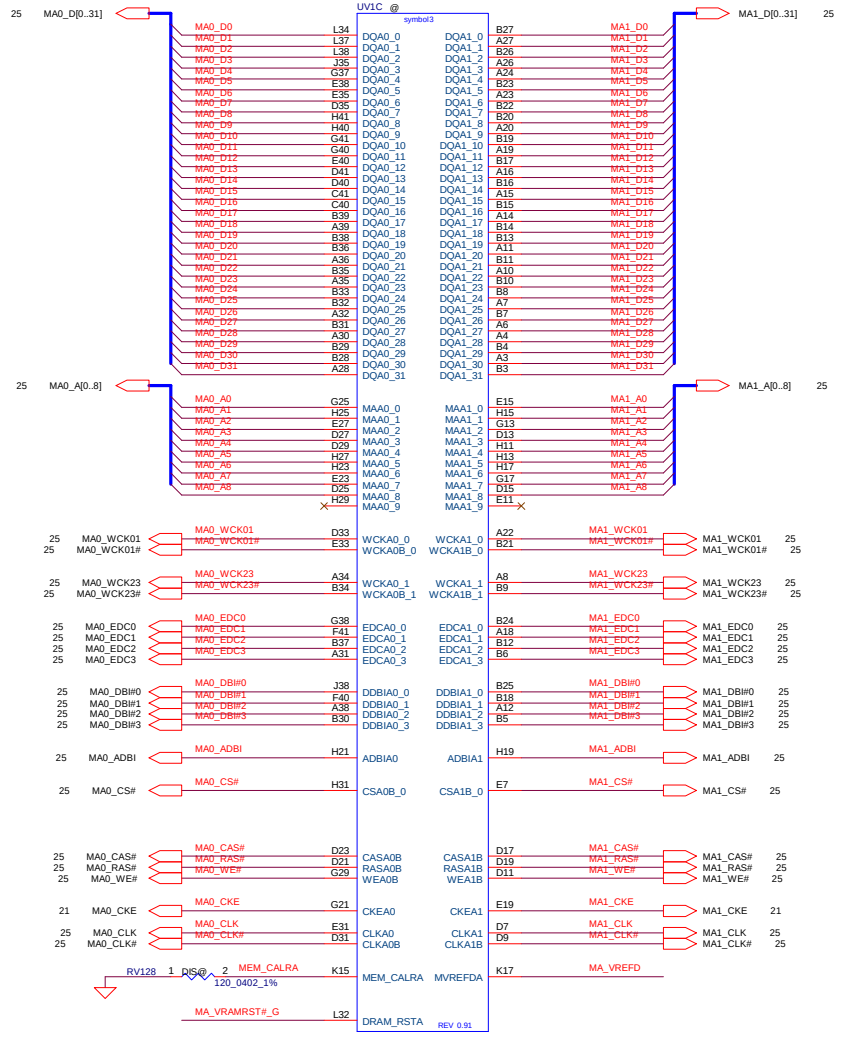
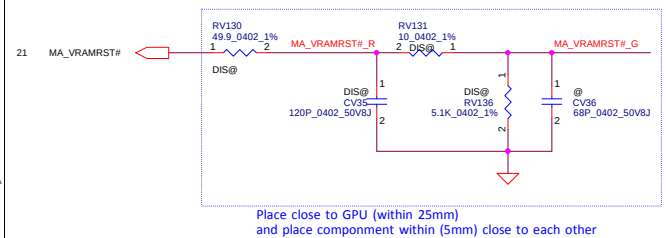
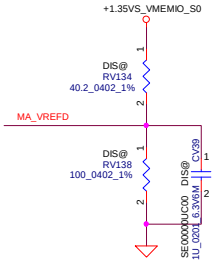
A0/1 Channel

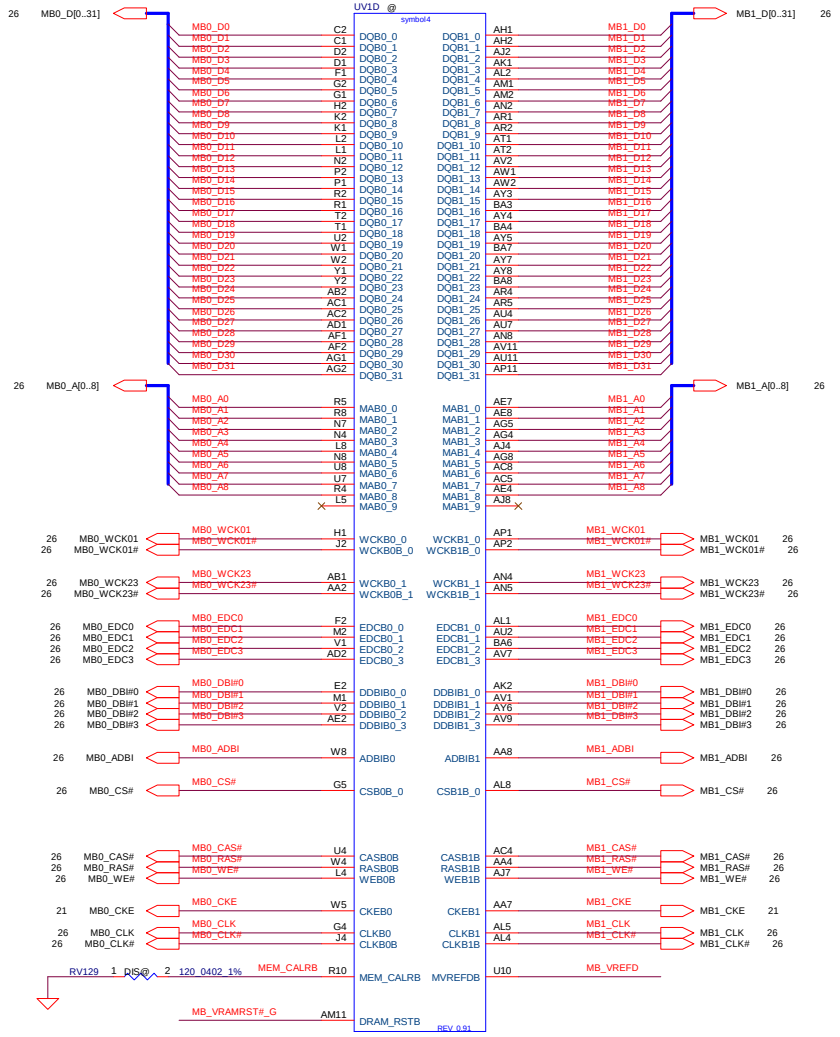


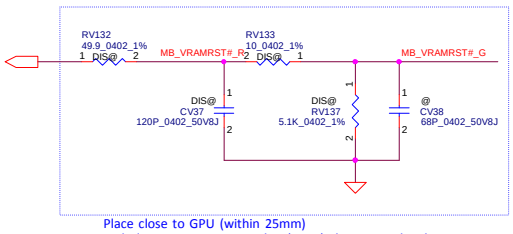


Place close to GPU (within 25mm)
and place compponent within (5mm) close to each other

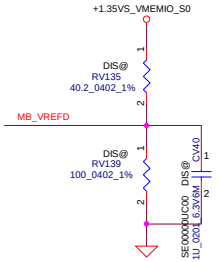


B0/1 Channel





Place close to GPU (within 25mm)
and place compponent within (5mm) close to each other



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A0 Channel

A1 Channel

MF=0

MF=1

UV18

UV17

170-BALL SGRAM GDDR5

H5GC4H24AJR-R0C_BGA170

Can NC For GDDR5 Spec.

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Issued Date	2017/07/20	Deciphered Date 2018/07/20

Compal Electronics, Inc.

Title: R17M-P1-50/70_(5/9)_CH A

Size: Custom | Document Number: Module Design Topic | Rev: 0.1

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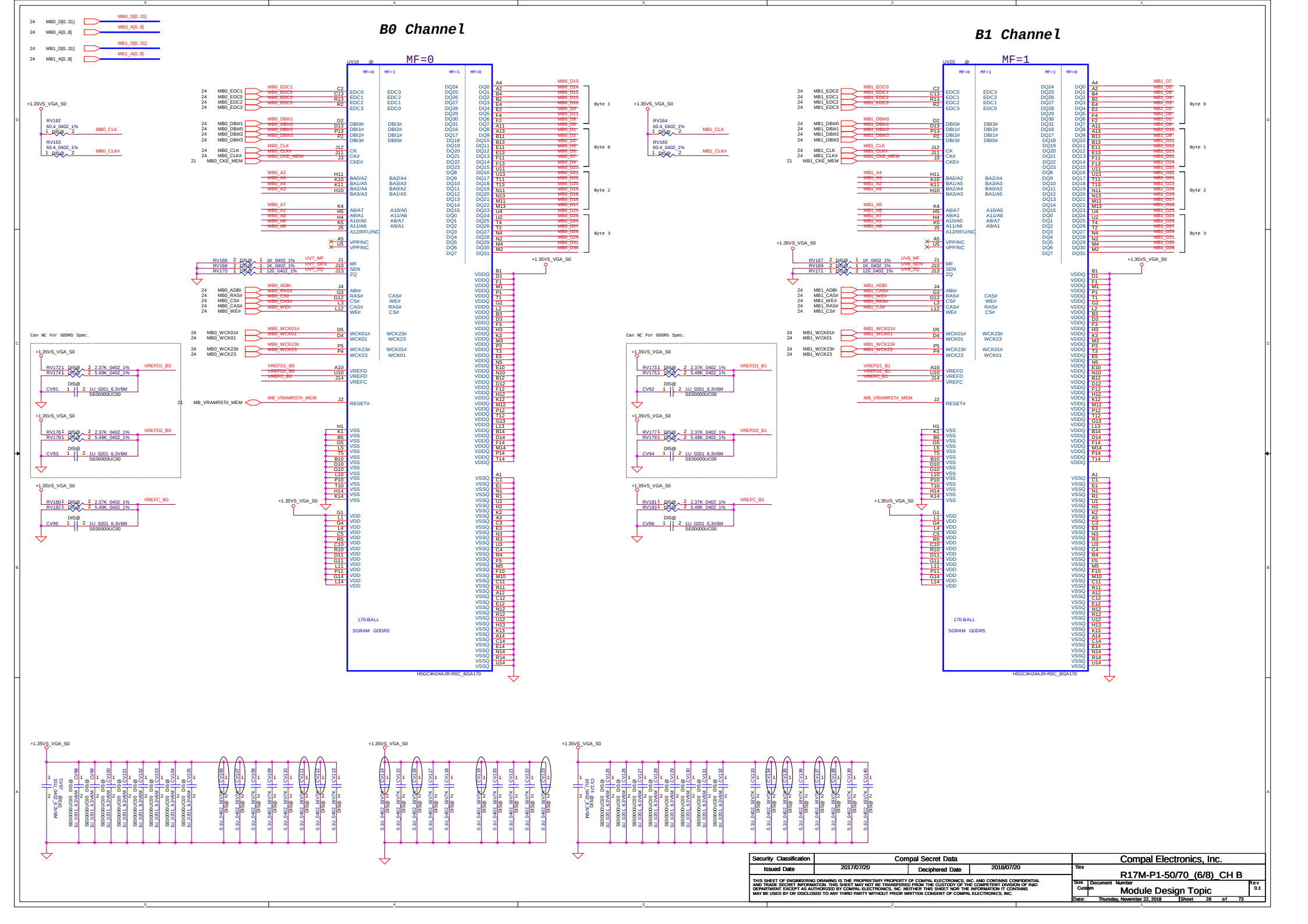

Security Classification	Compal Secret Data		
Issued Date	2017/07/20	Deciphered Date	2018/07/20

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Compal Electronics, Inc.

Title: R17M-P1-50/70_(6/8)_CH B

Size: Custom | Document Number: Module Design Topic | Rev: 0.1

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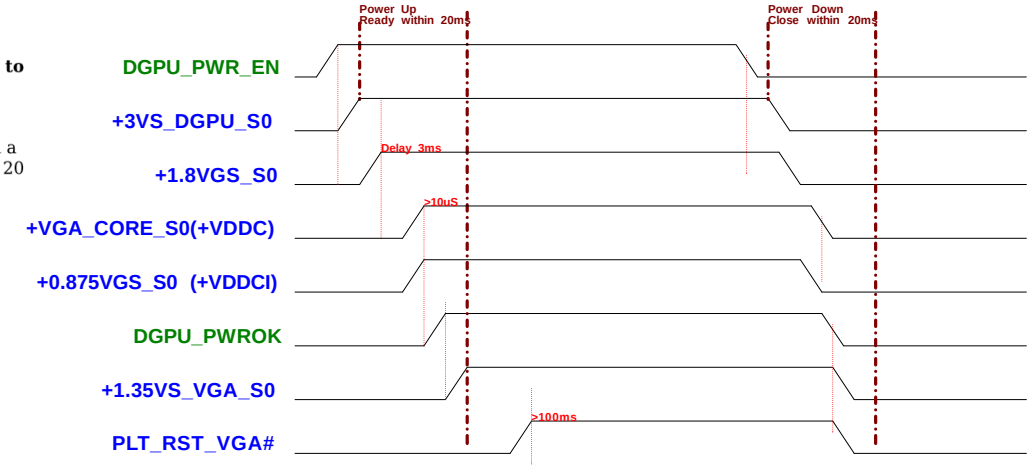
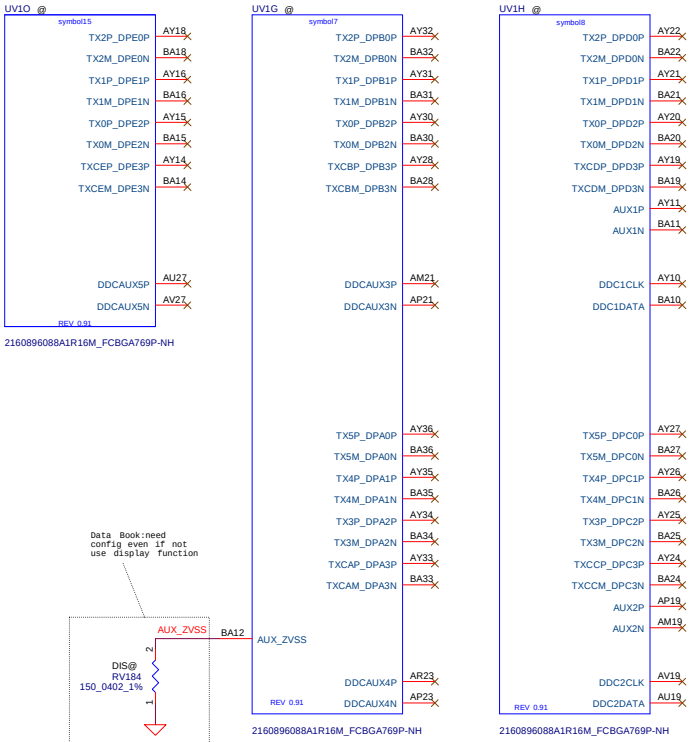
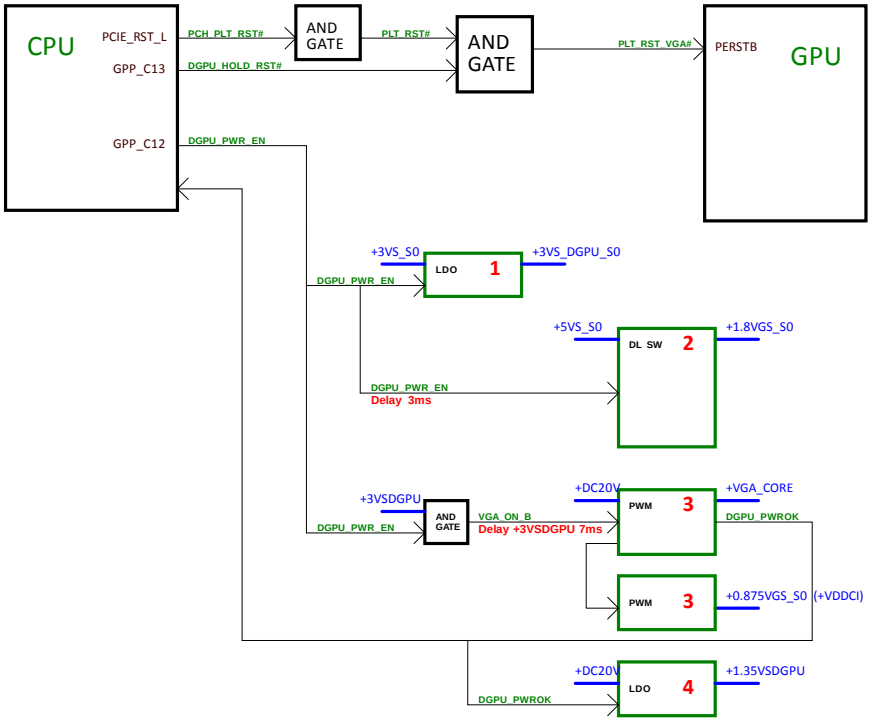
5.3 Power-up/down Sequence

"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

- All the GPU supplies, except for VDD_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/µs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 µs before VDDC, VDDCI, VDD_08, and VMEMIO start to ramp up.

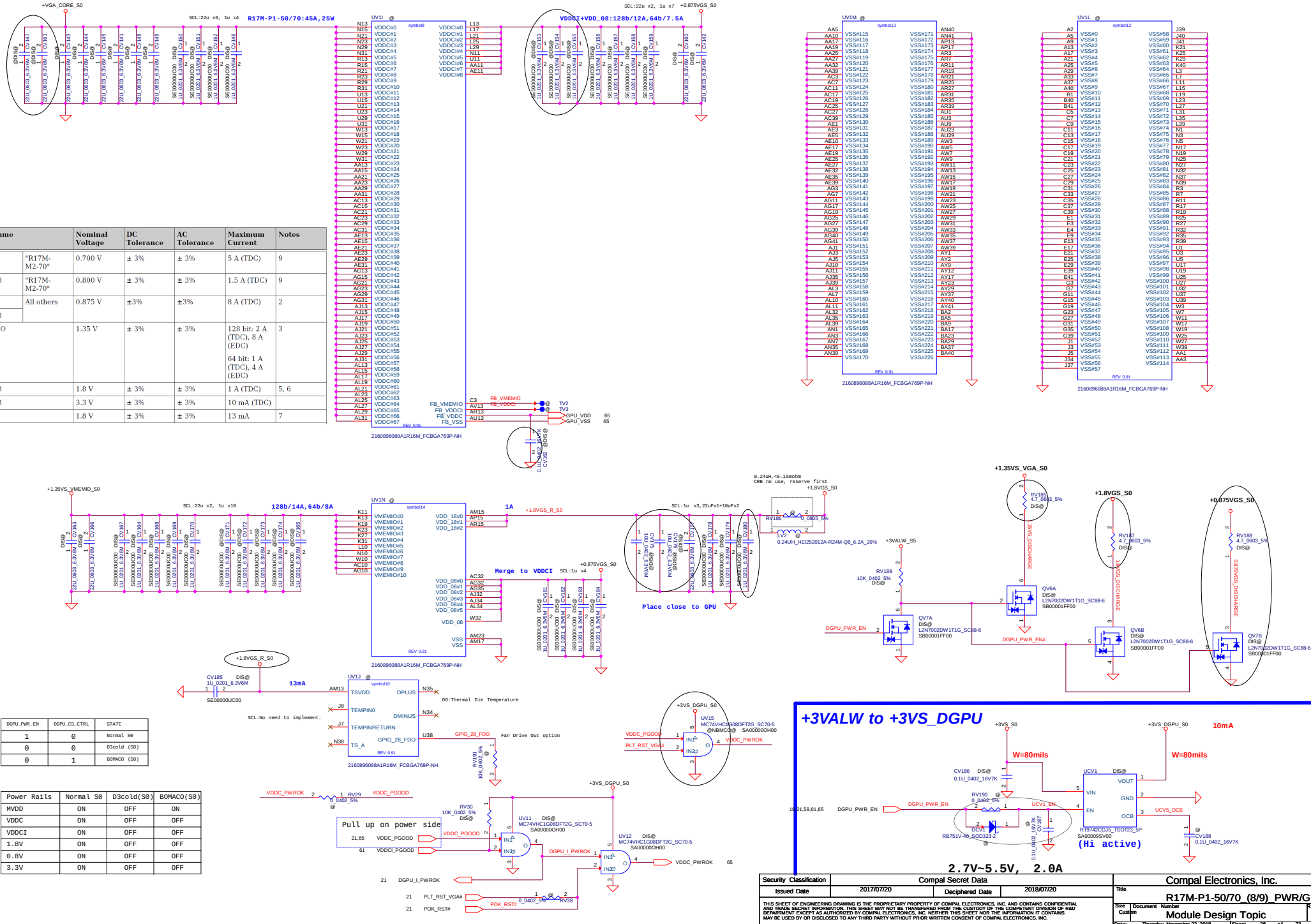






Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2017/07/20	Deciphered Date	2018/07/20

Title	R17M-P1-50/70_(7/9)_DISPLAY		
Size	Document Number		Rev
Custom	Module Design Topic		0.1
Date:	Thursday, November 22, 2018	Sheet	27 of 73



Rail Name		Nominal Voltage	DC Tolerance	AC Tolerance	Maximum Current	Notes
VDDCI	"R17M-M2-70"	0.700 V	± 3%	± 3%	5 A (TDC)	9
VDD_08	"R17M-M2-70"	0.800 V	± 3%	± 3%	1.5 A (TDC)	9
VDDCI	All others	0.875 V	±3%	±3%	8 A (TDC)	2
VDD_08						
VMEMIO		1.35 V	± 3%	± 3%	128 bit: 2 A (TDC), 8 A (EDC) 64 bit: 1 A (TDC), 4 A (EDC)	3
VDD_18		1.8 V	± 3%	± 3%	1 A (TDC)	5, 6
VDD_33		3.3 V	± 3%	± 3%	10 mA (TDC)	
TSVDD		1.8 V	± 3%	± 3%	13 mA	7

DGPU_PWR_EN	DGPU_CS_CTRL	STATE
1	0	Normal S0
0	0	D3cold (S0)
0	1	BOMACO (S0)

Power Rails	Normal S0	D3cold(S0)	BOMACO(S0)
MVDD	ON	OFF	ON
VDDC	ON	OFF	OFF
VDDCI	ON	OFF	OFF
1.8V	ON	OFF	OFF
0.8V	ON	OFF	OFF
3.3V	ON	OFF	OFF

Security Classification	Compal Secret Data	
Issued Date	2017/07/20	Deciphered Date 2018/07/20

Compal Electronics, Inc.

Title: R17M-P1-50/70_(8/9)_PWR/GND

Size: Custom | Document Number: Module Design Topic | Rev: 0.1

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Titan Ridge SP Collateral - TBT, USB & DP Part

Add DP AUX Pull high / low 0813

Reserve EC control RESET_N

Pull high / Pull low change to @ 0813

Close to UT1

Near UT1

RT44 close to Pin N16

I2C address: 0x50 for I2C Master

Close UT1

Type-C CONN

Polarity Reversal is allowed on CIO/USB/DP domains.
Need to be configured on NVM.

In case of unused high speed interface, please leave pins open. No need for termination.

Change Crystal USE AVL part 06/04

Table 12. Supported types of Flash Memory

Manufacturer	Type	Volume, Mbit	Supply, V
AMIC	A25L080	8.0	3.0-3.6
Spansion	S25FL208K	8.0	2.7-3.6
Winbond	W25Q80DVSNIG	8.0 (8pin SOIC150 mil)	2.7-3.6
Macronix	MX25L8006EM1I	8.0 (150mil, 8-SOP)	2.7-3.6
Micron	M25PE80-VMN6TP	8.0 (150mil, SO8N)	2.7-3.6
Micron	M25PX80-VMN6TP	8.0 (150mil, SO8N)	2.3-3.6

Figure 32. Power On Sequence

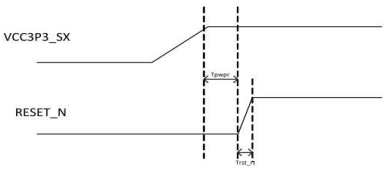

Table 436. Power On Sequence

Parameter	Description	Min	Max	Units	Comments
Tpwpr	From VCC3P3_SX at 90% to RESET_N de-assertion	100	-	us	
Trst_rt	RESET_N rise time	0.1	500	ns	

Compal Electronics, Inc.

Title: Thunderbolt TR(1/4)

Size: | Document Number: LA-G801P | Rev: 0.1

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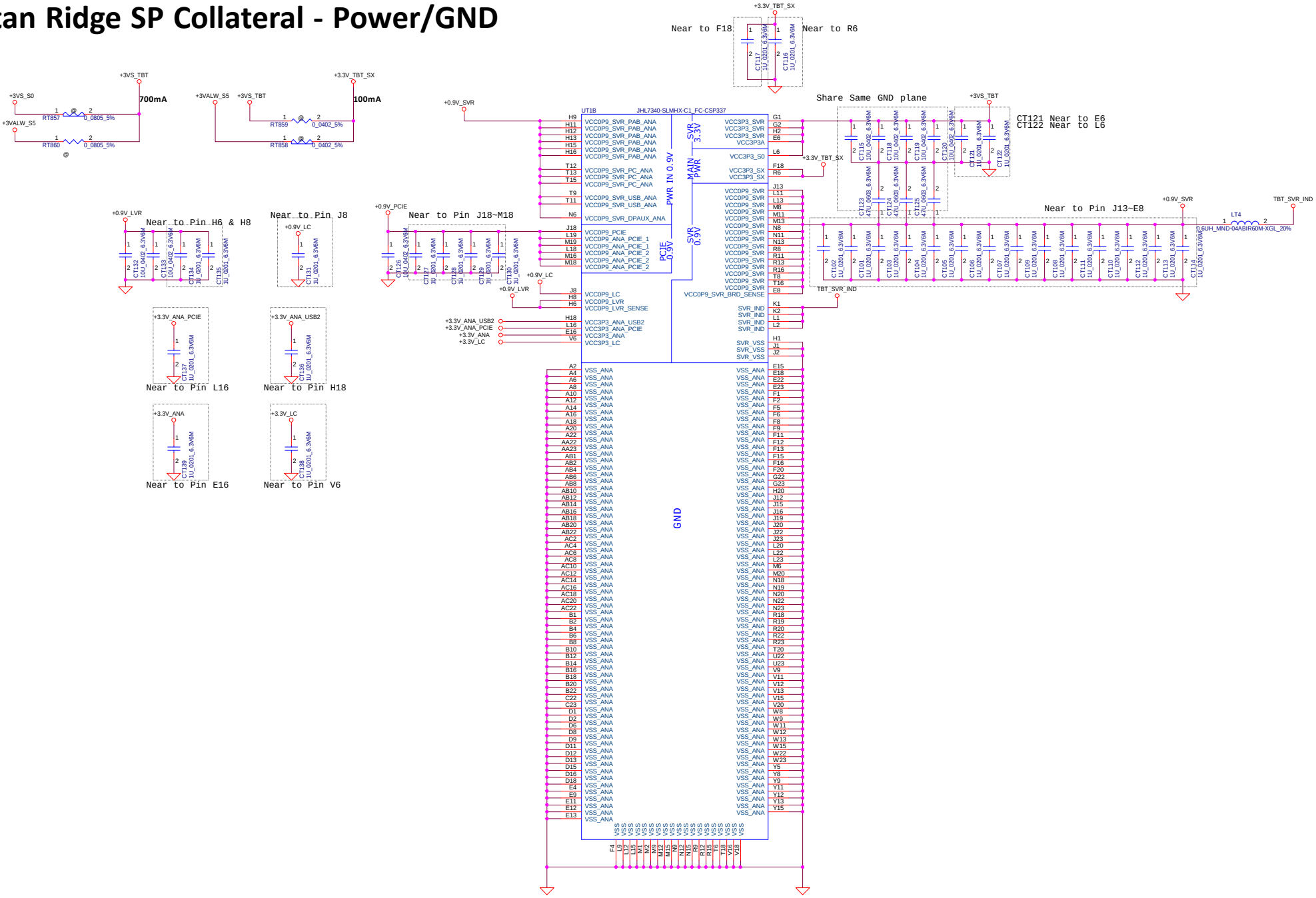
Titan Ridge SP Collateral - Power/GND



Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

Compal Electronics, Inc.

Title: **Thunderbolt TR(2/4)**

Size: | Document Number: **LA-G801P** | Rev: 0.1

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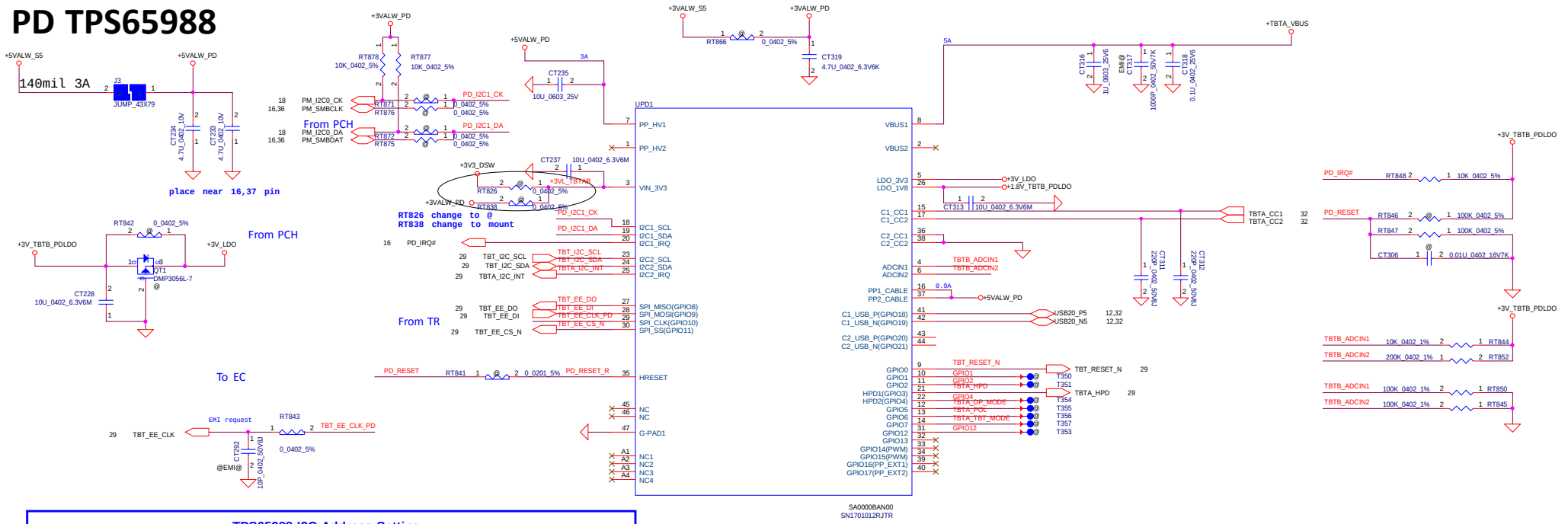
PD TPS65988



TPS65988 I2C Address Setting

Table 8. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

Table 4. I²C Default Unique Address I2C1 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C1[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

Table 5. I²C Default Unique Address I2C1 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C2[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							

For the I2C2 interface, the unique I²C address is a fixed value as shown in Table 6 and Table 7.

Table 6. I²C Default Unique Address I2C2 - Port 1

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	0	0	0	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 7. I²C Default Unique Address I2C2 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	1	1	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Compal Electronics, Inc.

Title: Thunderbolt PD(3/4)

Size | Document Number: LA-G801P | Rev: 0.1

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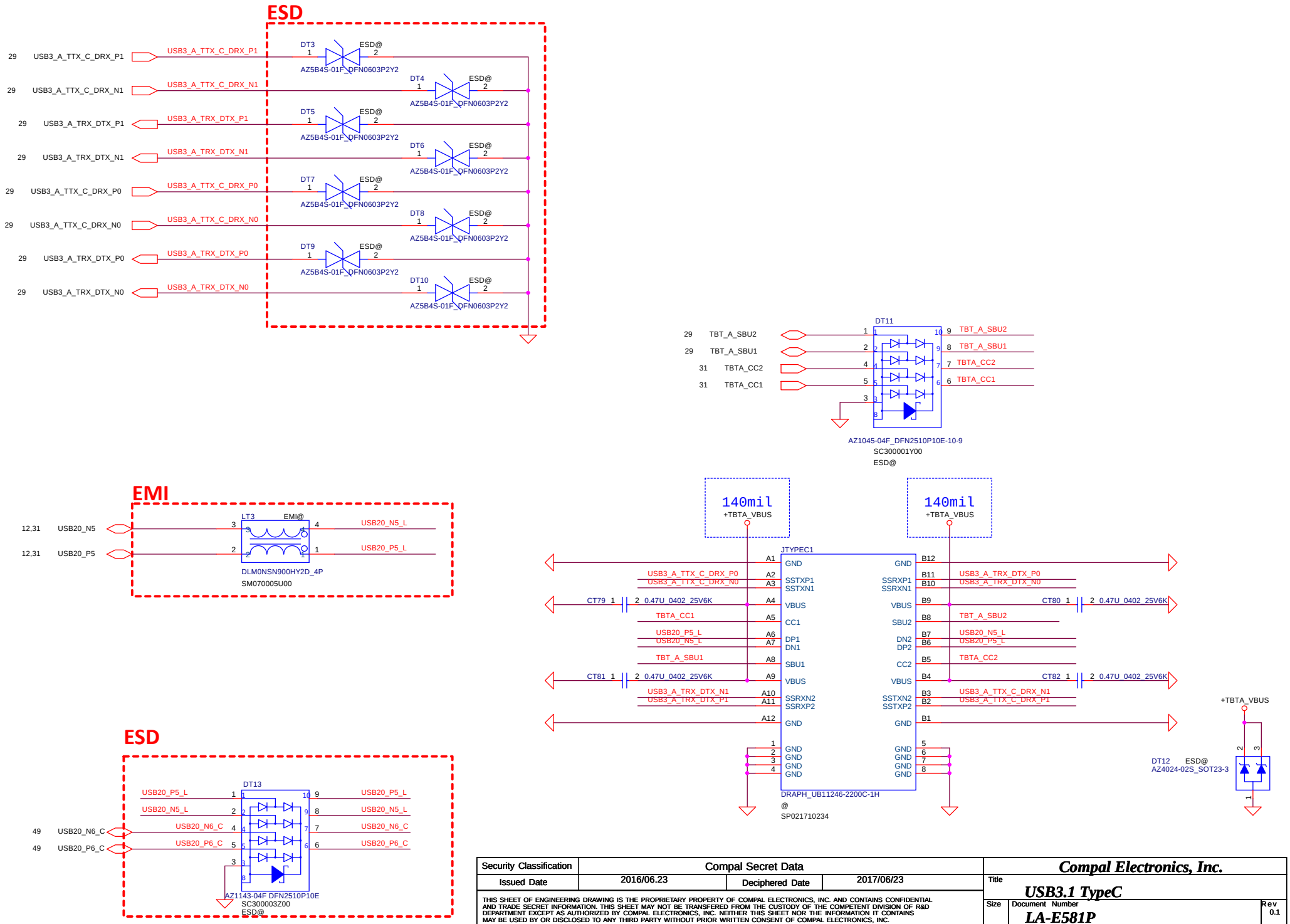

Security Classification	Compal Secret Data		
Issued Date	2016/06.23	Deciphered Date	2017/06/23

Compal Electronics, Inc.

Title: **USB3.1 TypeC**

Size	Document Number	Rev
	LA-E581P	0.1

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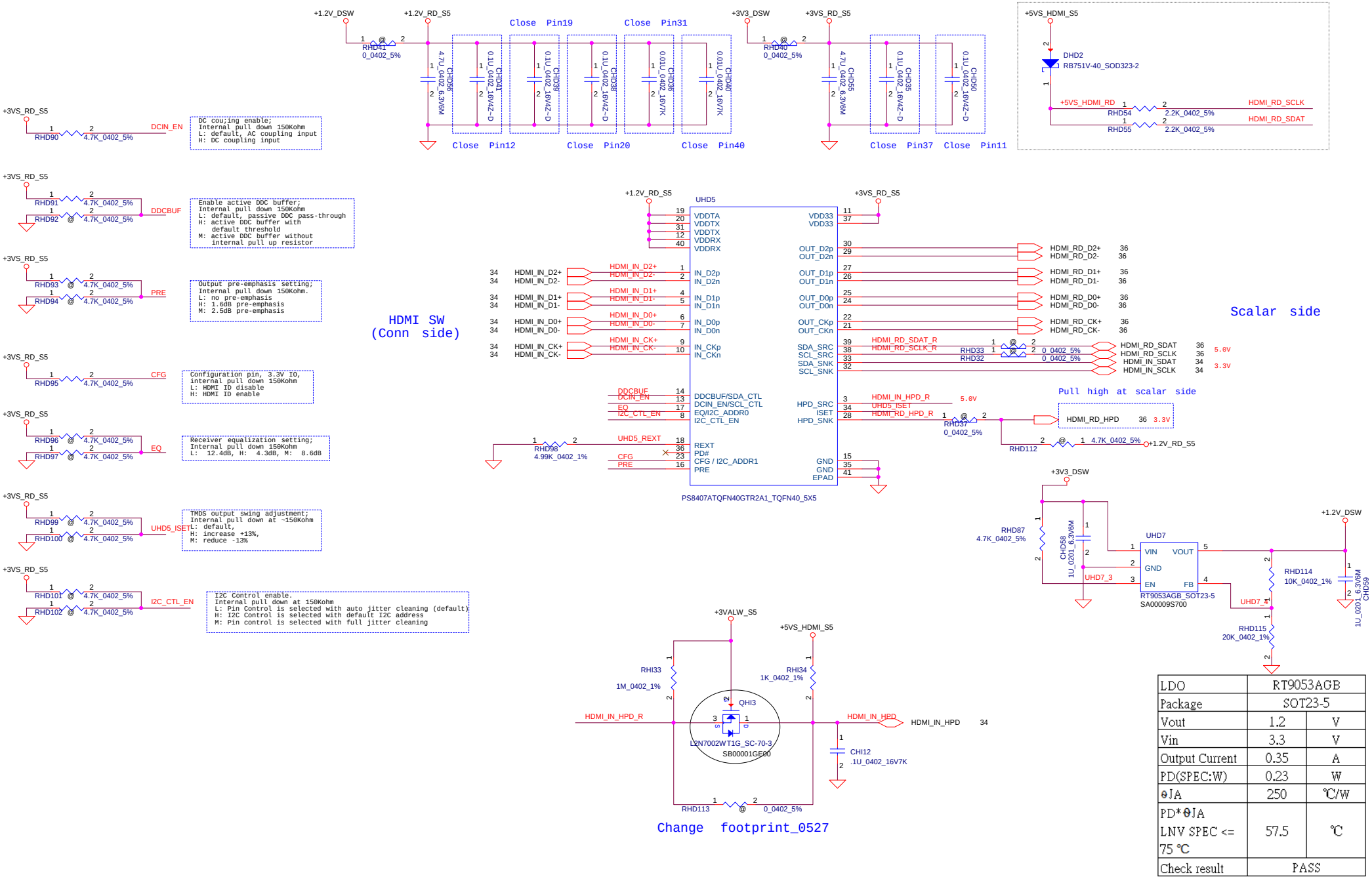

LDO	RT9053AGB	
Package	SOT23-5	
Vout	1.2	V
Vin	3.3	V
Output Current	0.35	A
PD(SPEC:W)	0.23	W
θJA	250	℃/W
PD*θJA LNV SPEC <= 75 ℃	57.5	℃
Check result	PASS	

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2015/10/02

Compal Electronics, Inc.

Title: **HDMI OUT LEVEL shift**

Size	Document Number	Rev
	LA-F881P M/B	0.1
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Control			Switch Function		
OE	GPU_ SEL	AUX_ HPD_ SEL	D0-D3	AUX	HPD
High	Low	Low	A	AUX A	HPD A
High	Low	High	A	AUX B	HPD B
High	High	Low	B	AUX A	HPD A
High	High	High	B	AUX B	HPD B
Low	X	X	Hi-Z	Hi-Z	Hi-Z

HDMI Input/Output Connector

RTD2785
RTD2795

CPU HDMI-OUT

2.2k 5V Pull-High on Connector side

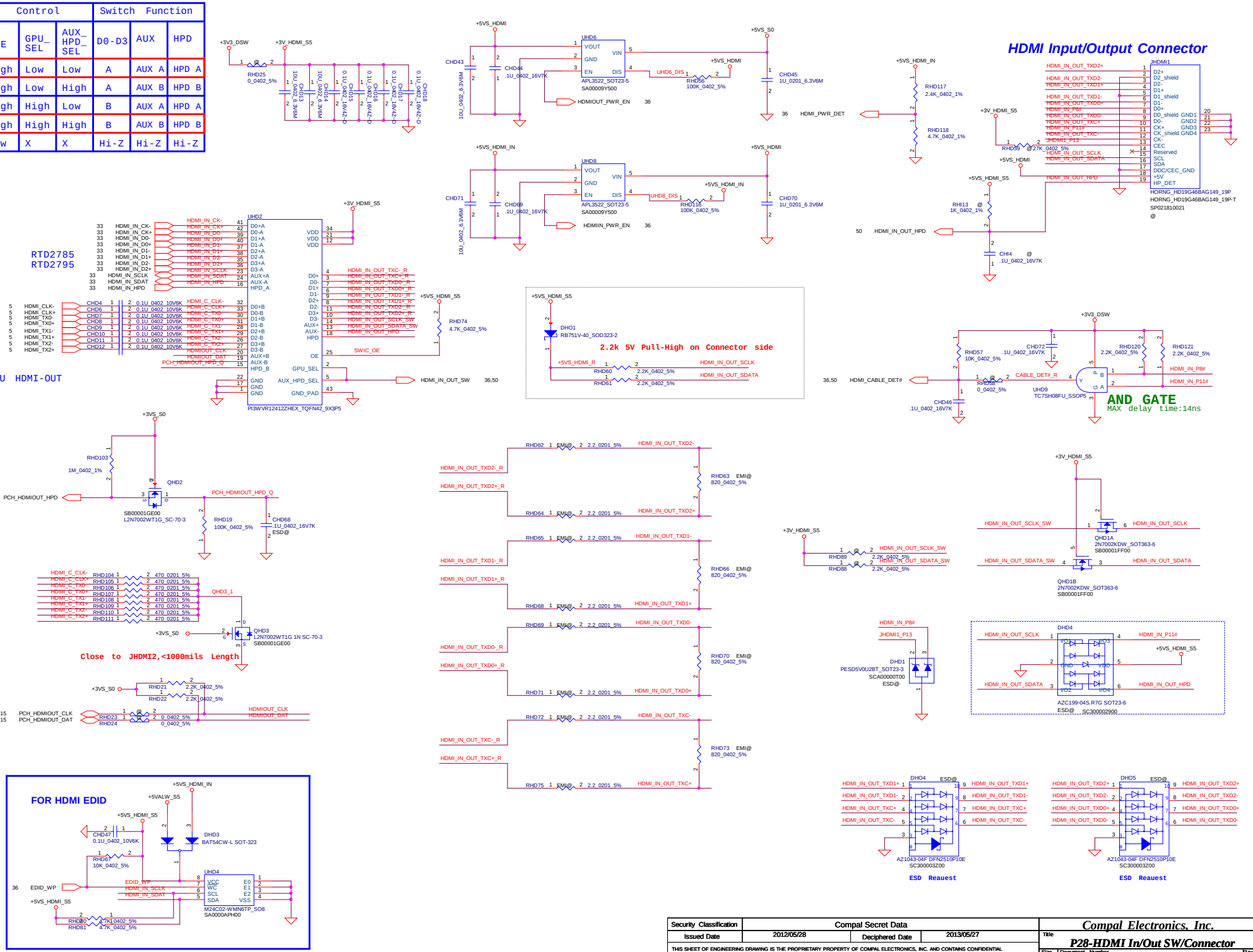
AND GATE
MAX delay time:14ns

Close to JHDMI2,<1000mils Length

FOR HDMI EDID

ESD Reauest

ESD Reauest



Security Classification	Compal Secret Data		
Issued Date	2012/05/28	Deciphered Date	2013/05/27

Compal Electronics, Inc.

Title: P28-HDMI In/Out SW/Connector

Size	Document Number	Rev
Custom	LA-F881P M/B	0.5

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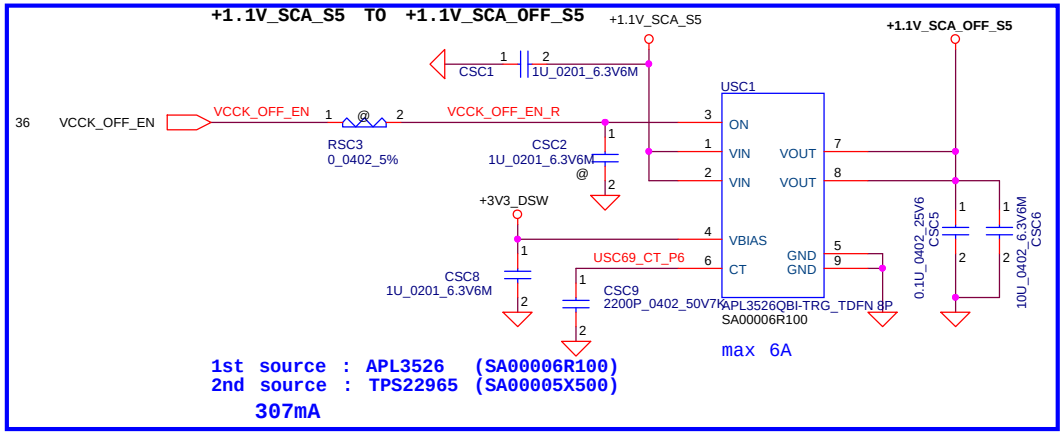
1474mA (RTD2785)
1960mA (RTD2795)

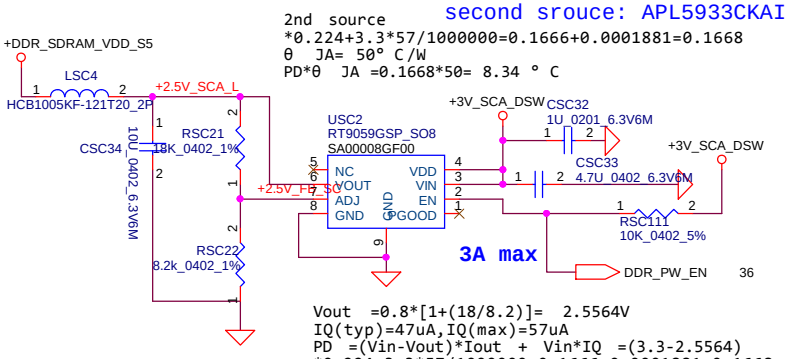
+1.1V_SCA_S5 TO +1.1V_SCA_OFF_S5



+3V_SCA_DSW TO +DDR_SDRAM_VDD_S5

main source : RT9059GSP
second srouce: APL5933CKAI

2nd source
*0.224+3.3*57/1000000=0.1666+0.0001881=0.1668
θ JA= 50° C/W
PD*θ JA =0.1668*50= 8.34 ° C

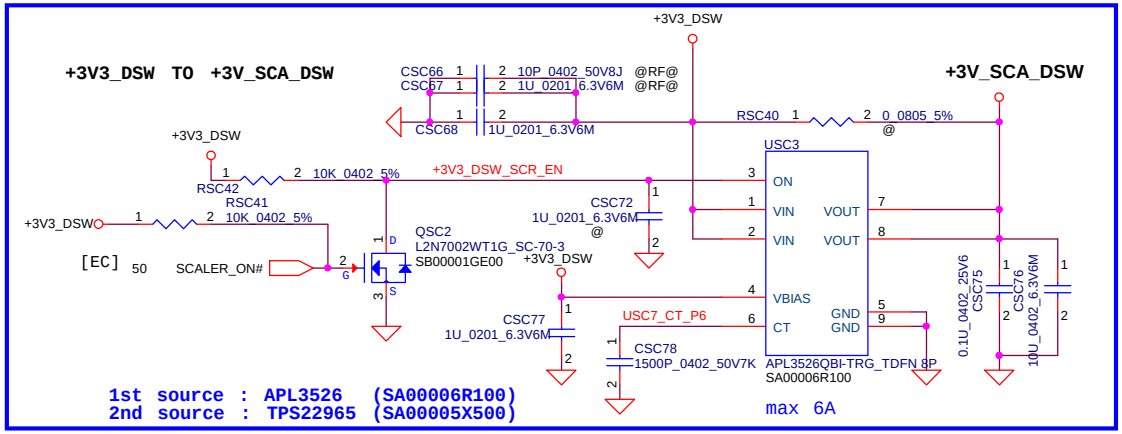


224mA 2.5V (RTD2785)
676mA 1.8V (RTD2795)

Vout =0.8*[1+(18/8.2)]= 2.5564V
IQ(typ)=47uA,IQ(max)=57uA
PD =(Vin-Vout)*Iout + Vin*IQ =(3.3-2.5564)
*0.224+3.3*57/1000000=0.1666+0.0001881=0.1668
θ JA=33.7 ° C/W
PD*θ JA=0.1668*33.7=5.6° C

Vout =0.8*[1+(18/14)]= 1.8285V
IQ(typ)=47uA,IQ(max)=57uA
PD =(Vin-Vout)*Iout + Vin*IQ =(3.3-1.8285)
*0.676+3.3*57/1000000=0.1666+0.0001881=0.9949
θ JA=33.7 ° C/W
PD*θ JA=0.1668*33.7=5.6° C

+3V3_DSW TO +3V_SCA_DSW



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: *Scalar RTD2785T_CG*

Size	Document Number	Rev
B	LA-XXXX M/B	0.1

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FOR Scalar Firmware Code

SPI 16M

Change SPI ROM from 8M bits to 16M bits.
11/29 by Mike

1st source : W25Q16JVSSIM (SA00003F050)
2nd source : W25Q16JVSSIQ (SA00003F040)

For EMI

EEPROM 16K

FOR OSD/HDCP Parameter Value

Add pull high 2018/05/23

HDMI IN

HDMI1.4 [P/N swap]
(Scalar Code need follow swap)

For QHD LVDS Panel LANx4

From CPU

50ohm

NC

LVDS x4 port

Aux pull Hi/low on CPU side

pull up on CPU side

918mA (RTD2785)

Audio

Audio

[EC/Converter]
[LVDS Panel]
[Converter BL]
[PCH]

close to USC3 (Scaler IC)

Pull up on EC

SMBus [link EC]

Firmware update by SMBUS

Pull up on HDMI Redriver

pull Low 100k on CPU side

50ohm

	PANEL_ID1	PANEL_ID2
LM270WQ4-SSB1 (LG)	L	L
~~LTM270DL08- M01~~ (Samsung)	L	H

	SC_MODE1	SC_MODE2	SC_MODE3
PC mode	L	L	
Monitor mode	L	H	
AMP Mute	H	L	
S5 Mode	H	H	
PC On			H
PC Off			L

Security Classification	Compal Secret Data
Issued Date	2015/12/25
Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: *Scalar RTD2785T_CG*

Size: Custom | Document Number: **LA-XXXX M/B** | Rev: 0.1

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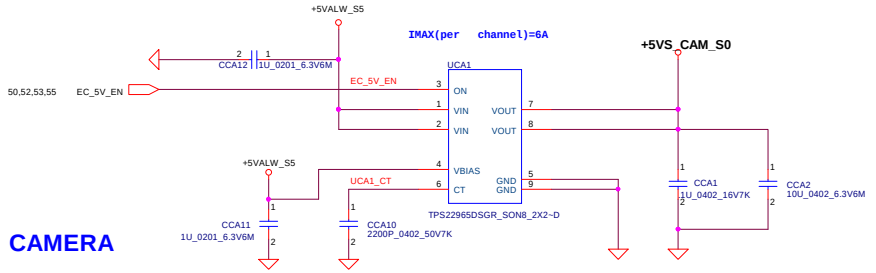
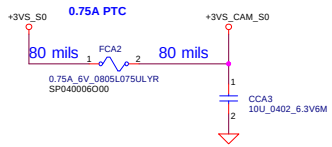
+5VALW_S5 to +5VS_CAM_S0 Transfer

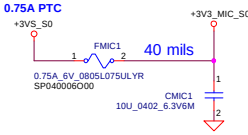


CAMERA

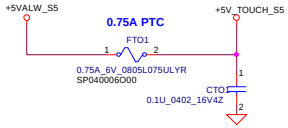
1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X50L)

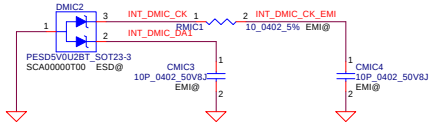


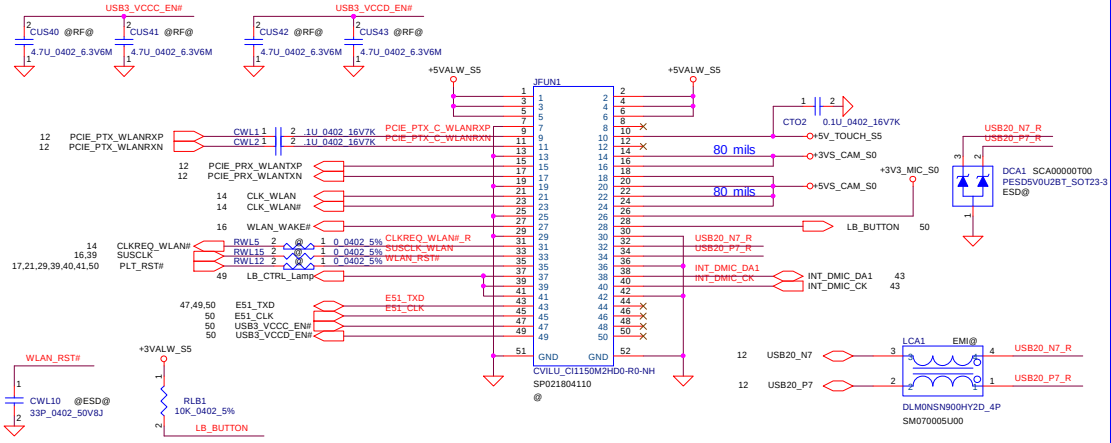
MIC



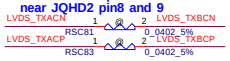
Touch



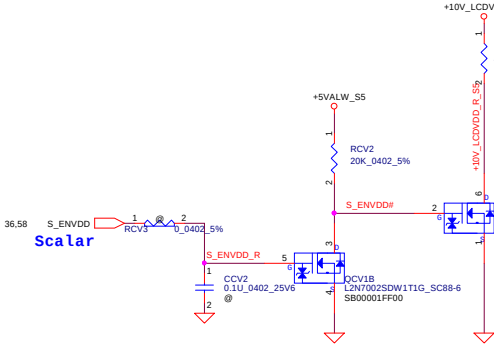


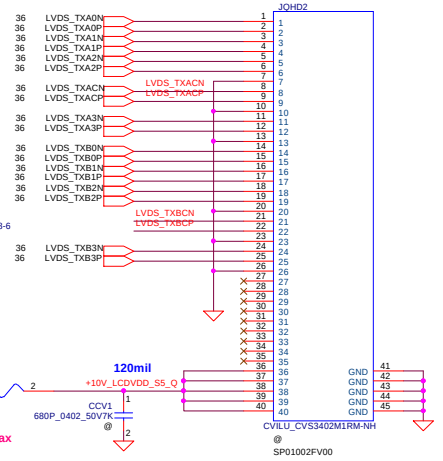


RSC81/RSC83 place Bottom side near JQHD2 pin8 and 9

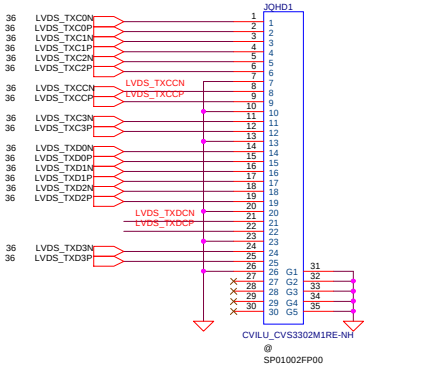


RSC82/RSC84 place Bottom side near JQHD1 pin8 and 9





Panel side Pin7 need contact to GND SPEC
H(3.3V)= MSTAR Concept, L=normal
(Connect High or low, No NC Condition)



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.	
Title	LVDS/Convertor/CAM/Touch/MIC
Size: Custom	Document Number: LA-E631P M/B
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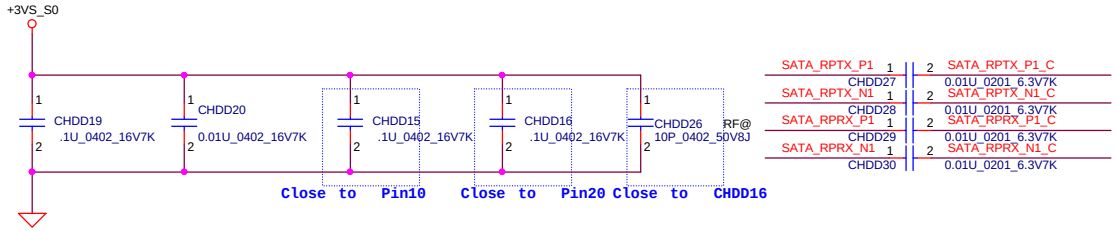
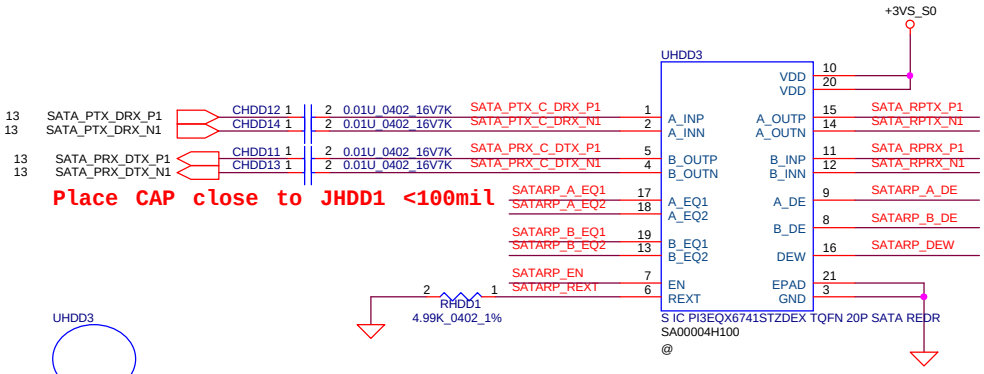
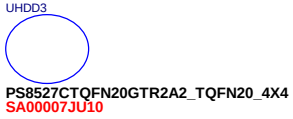
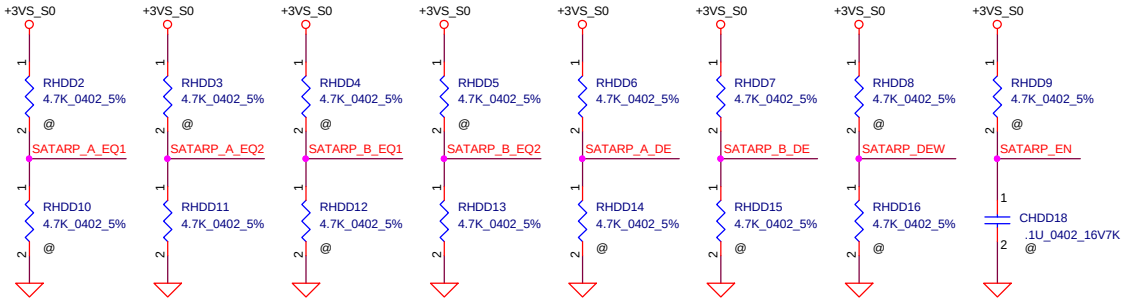
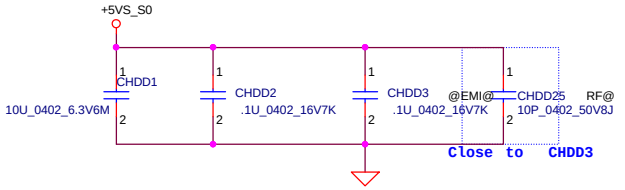
SATA HDD Conn.

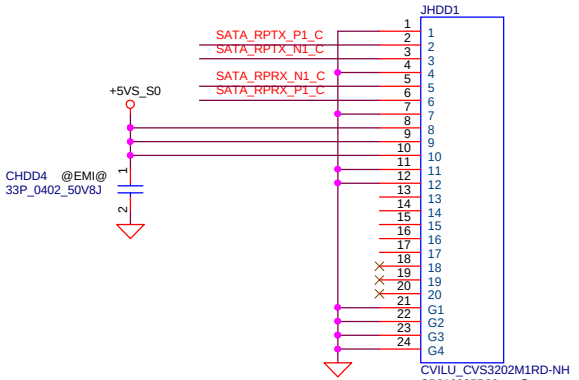












A_EQ2	A_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

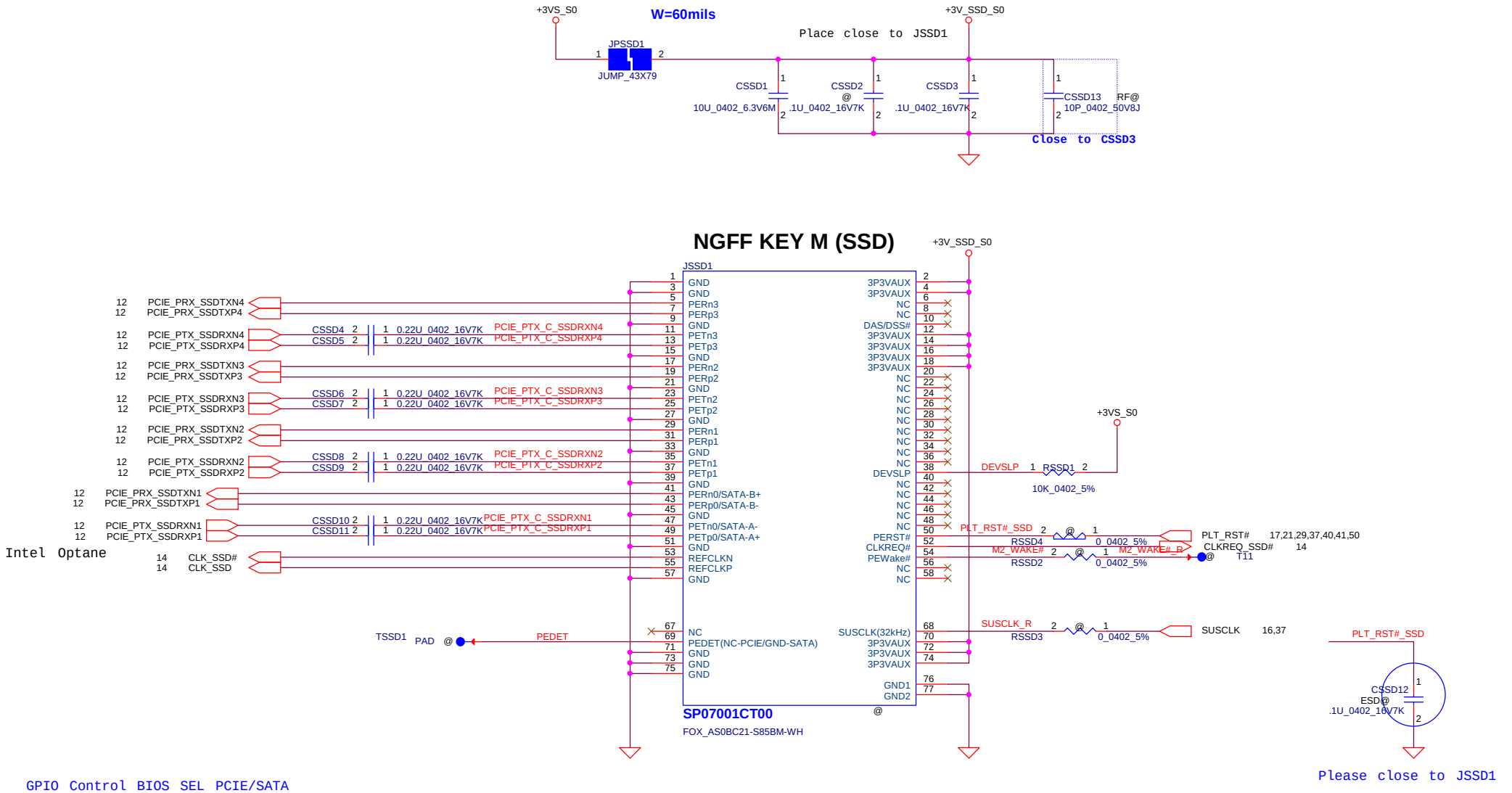
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***HDD/ODD***

Size: Custom | Document Number: **LA-F881P M/B** | Rev: 0.1

Date: Thursday, November 22, 2018 | Sheet 38 of 73



GPIO Control BIOS SEL PCIE/SATA

Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

Compal Electronics, Inc.

Title: ***SSD (M2)***

Size	Document Number	Rev
B	LA-F881P M/B	0.1

Date: Thursday, November 22, 2018 Sheet 39 of 73

WOL circuit (Connect +3V_LAN to +3VALW)

+3VALW_S5 — JUML1 @ JUMP_43X39 — +3.3V_LAN_S5

60mil — 60mil

300mA,120ohm

close to UL1 pin11

+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.

Power (Decoupling Cap.)

40 mils — Close to Pin 11,23

+3.3V_LAN_S5

CL1 1 2 .1U_0402_16V7K
CL2 1 2 .1U_0402_16V7K
@ CL5 1 2 4.7U_0402_6.3V6M
@ CL21 1 2 4.7U_0402_6.3V6M
@ CL8 1 2 4.7U_0402_6.3V6M
CL3 1 2 .1U_0402_16V7K

Close to Pin 32

60 mils

+LAN_VDDREG

CL4 1 2 .1U_0402_16V7K
CL6 1 2 .1U_0402_16V7K
CL7 1 2 .1U_0402_16V7K
CL9 1 2 .1U_0402_16V7K

Close to pin 3,8,30,24

LED Status

WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on

blinking

8111G resistor/8111H capacitor

RL14 LANG@ SD028000080 RTL8111G-CG_0ohm resistor
RL17 LANG@ SD028000080 RTL8111G-CG_0ohm resistor
RL20 LANG@ SD028000080 RTL8111G-CG_0ohm resistor
RL15 LANG@ SD028000080 RTL8111G-CG_0ohm resistor
RL18 LANG@ SD028000080 RTL8111G-CG_0ohm resistor
RL21 LANG@ SD028000080 RTL8111G-CG_0ohm resistor
RL16 LANG@ SD028000080 RTL8111G-CG_0ohm resistor
RL19 LANG@ SD028000080 RTL8111G-CG_0ohm resistor

Close to pin 22

+3.3V_LAN_S5 — +LAN_VDDREG — +LAN_VDDREG

@ CL12 1 2 SE00000UC00 1U_0201_6.3V6M
CL20 1 2 .1U_0402_16V7K

CL13~ CL16 need colse to UL1

12 PCIE_PRX_LANTXP — CL13 1 2 .1U_0402_16V7K — PCIE_PRX_C_LANTXP — 17 HSOP
12 PCIE_PRX_LANTXN — CL14 1 2 .1U_0402_16V7K — PCIE_PRX_C_LANTXN — 18 HSON
12 PCIE_PTX_LANRXP — CL15 1 2 .1U_0402_16V7K — PCIE_PTX_C_LANRXP — 13 HSIP
12 PCIE_PTX_LANRXN — CL16 1 2 .1U_0402_16V7K — PCIE_PTX_C_LANRXN — 14 HSIN

14 CLK_PCIE_LAN — 15 REFCLK_P
14 CLK_PCIE_LAN# — 16 REFCLK_N

+3.3V_LAN_S5 — RL1 1 2 10K_0402_5% — LAN_CLKREQ#_R — 12 CLKREQB

+3VS_S0 — RL3 1 2 1K_0402_5% — 29,50 PCIE_WAKE# — 21 LANWAKEB

ISOLATE# — 20 ISOLATEB

17,21,29,37,39,41,50 PLT_RST# — 19 PERSTB

+3.3V_LAN_S5 — RL5 1 2 2.49K_0402_1% — UL1_RSET_P31 — 23 VDDREG / 31 RSET

RL6 15K_0402_5%

LAN_X2 — 29 CKXTAL2
LAN_X1 — 28 CKXTAL1

UL1

3	AVDD10	11	AVDD33
8	AVDD10	32	AVDD33
30	AVDD10	22	DVDD10

MDIP0 1 LAN_MIDI0+_R — RL14 1 2 S0IX_EMI@ 0.1U_0402_25V6 — LAN_MIDI0+
MDIN0 2 LAN_MIDI0-_R — RL15 1 2 S0IX_EMI@ 0.1U_0402_25V6 — LAN_MIDI0-
MDIP1 4 LAN_MIDI1+_R — RL16 1 2 S0IX_EMI@ 0.1U_0402_25V6 — LAN_MIDI1+
MDIN1 5 LAN_MIDI1-_R — RL17 1 2 S0IX_EMI@ 0.1U_0402_25V6 — LAN_MIDI1-
MDIP2 6 LAN_MIDI2+_R — RL18 1 2 S0IX_EMI@ 0.1U_0402_25V6 — LAN_MIDI2+
MDIN2 7 LAN_MIDI2-_R — RL19 1 2 S0IX_EMI@ 0.1U_0402_25V6 — LAN_MIDI2-
MDIP3 9 LAN_MIDI3+_R — RL20 1 2 S0IX_EMI@ 0.1U_0402_25V6 — LAN_MIDI3+
MDIN3 10 LAN_MIDI3-_R — RL21 1 2 S0IX_EMI@ 0.1U_0402_25V6 — LAN_MIDI3-

LED2 25 LAN_LED_ORG# — @ TL1
LED1/GPIO 26 LAN_PHY_DIS# — @ TL2 — LAN_PHY_DIS# 50
LED0 27 LAN_LED_YEL# — @ TL3

+LAN_VDDREG — REGOUT 24

GND 33

RTL8111H-CG QFN 32P_4X4
SA000080P00
LANH@

UL1 LANG@
RTL8111G-CG
SA00005V700

Pull up on PCH page14

+3VS_S0 — +3.3V_LAN_S5 — RL8 10K_0402_5%

14 CLKREQ_LAN# — QL1 L2N7002WT1G_SC-70-3 SB00001GE00 — LAN_CLKREQ#_R

LAN_MIDI0+ — DL1 — LAN_MIDI1-
LAN_MIDI1+ — ESD@ SC300001G00 AZC099-04S.R7G SOT23-6 — LAN_MIDI0-
+3.3V_LAN_S5

LAN_MIDI2+ — DL2 — LAN_MIDI3-
LAN_MIDI3+ — ESD@ SC300001G00 AZC099-04S.R7G SOT23-6 — LAN_MIDI2-
+3.3V_LAN_S5

+3.3V_LAN_S5 — RL13 @ 10K_0402_5% — LAN_PHY_DIS#

LAN_X1 — RL10 1M_0402_5% — LAN_X2

YL1 OSC NC NC OSC — 25MHZ_10PF_X3G025000DA1H-X SJ10000DE00

CL18 10P_0402_50V8J
CL19 10P_0402_50V8J

JRJ1

RL4 @ 0_0402_5%
CL17 .1U_0402_16V7K EMI@

LAN_MIDI0+ — TD1+ R1
LAN_MIDI0- — TD1- R2
LAN_MIDI1+ — TD2+ R3
LAN_MIDI1- — TD2- R4
JRJ1_CT_R5R6 — CT R5
CT R6
LAN_MIDI2+ — TD3+ R7
LAN_MIDI2- — TD3- R8
LAN_MIDI3+ — TD4+ R9
LAN_MIDI3- — TD4- R10

Yellow — LAN_LED_YEL# — RL7 510_0402_5% — LAN_LED_YEL#_R — 11 L1

20mils

+3.3V_LAN_S5 — 12 L2

+3.3V_LAN_S5 — LAN_LED_YEL# — DCA3 PESD5V0U2BT_SOT23-3 SCA00000T00 ESD@

GND 13
GND 14

UDE_RT9-CP-0002_14P
UDE_RT9-CP-0002_14P-T
SP011810021
@

LAN_GND

RL11 1 @ 2 0_0805_5%
RL12 1 @ 2 0_0805_5%
LAN_GND

Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/12/15

Compal Electronics, Inc.

Title: LAN RTL8111G/H

Size: Custom | Document Number: LA-E881P M/B | Rev: 0.1

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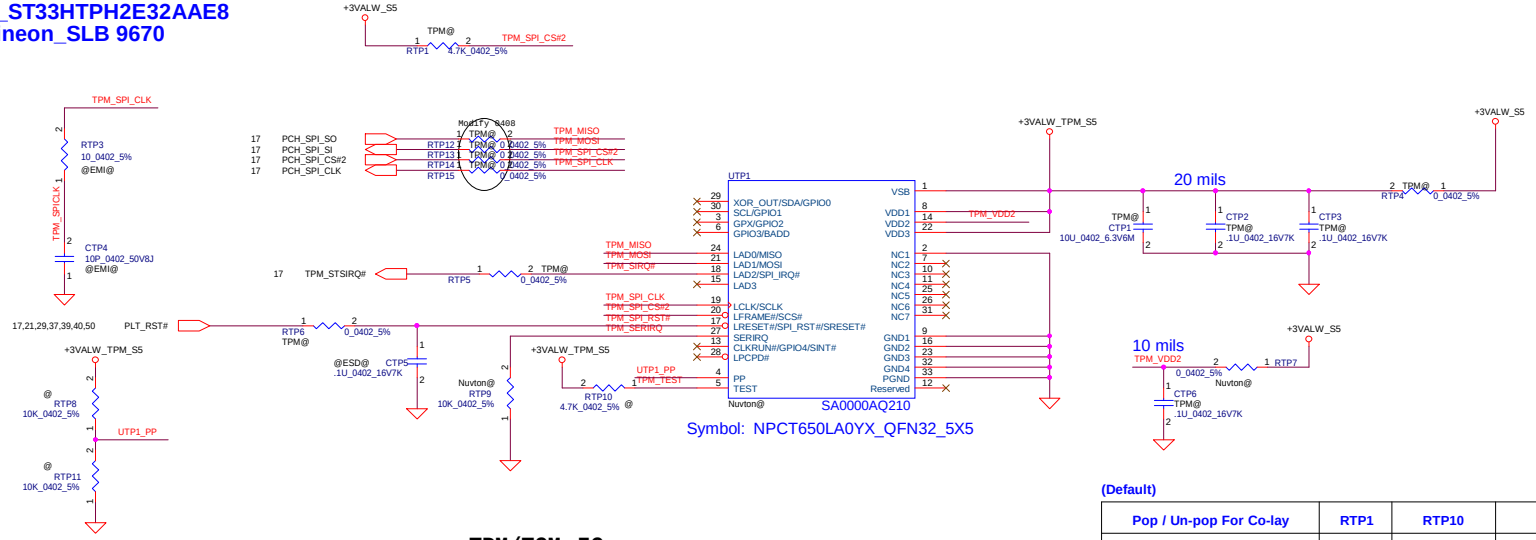
WLAN (WIFI/BT Combo)

TPM 2.0 Co-lay

1.Nuvton_NPCT650LBAYX
2.ST_ST33HTPH2E32AAE8
3.Infineon_SLB 9670

NEW PART: Nuvoton NPCT650LBAYX (Default)
Infineon SLB 9670
ST ST33HTPH2E32AAE8



TPM/TCM IC

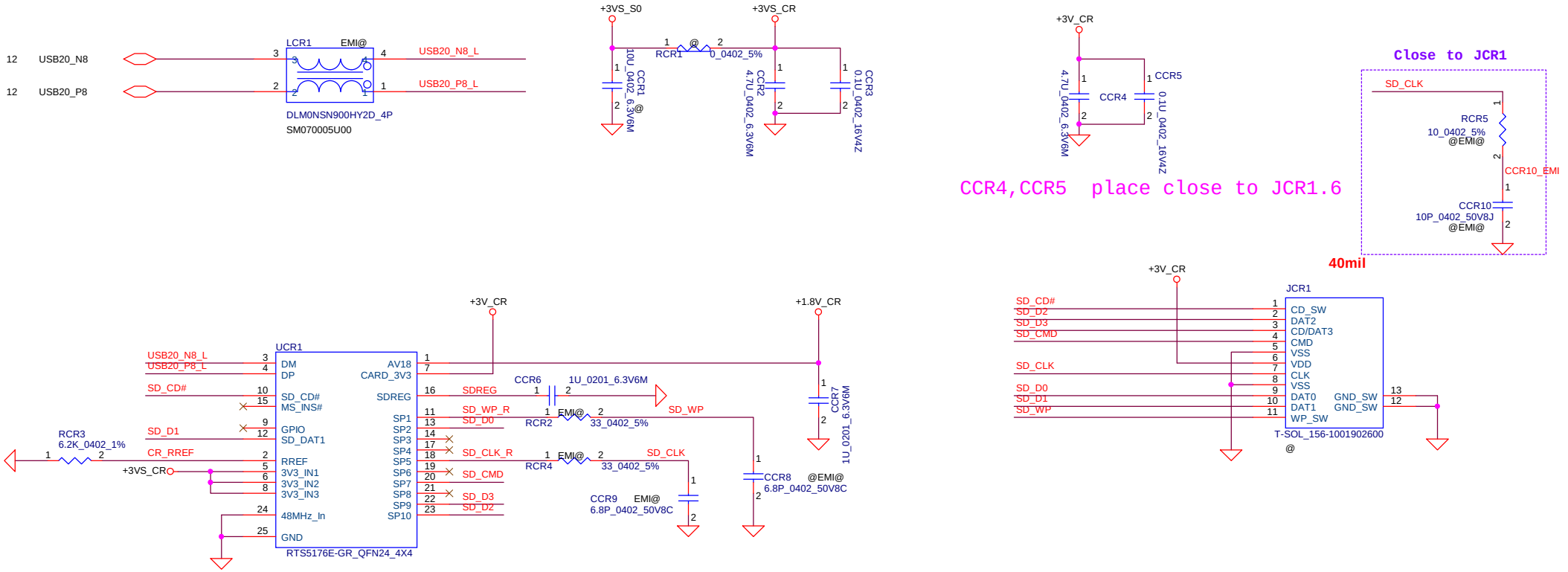
ST_ST33HTPH2E32AAE8(SPI) SA00009SO40

Infineon_SLB 9670(SPI) SA00009N230

(Default)

Pop / Un-pop For Co-lay	RTP1	RTP10	BOM Config
Nuvton_NPCT650LBAYX (SPI)	V	V	Nuvton@+TPM@
ST_ST33HTPH2E32AAE8(SPI)	X	X	ST@+TPM@
Infineon_SLB 9670(SPI)	X	X	Infineon@+TPM@

Compal Electronics, Inc.
Title: WLAN (NGFF) / TPM
Size: Document Number: LA-F881P M/B Rev: 0.1
Date: Thursday, November 22, 2018 Sheet 41 of 73



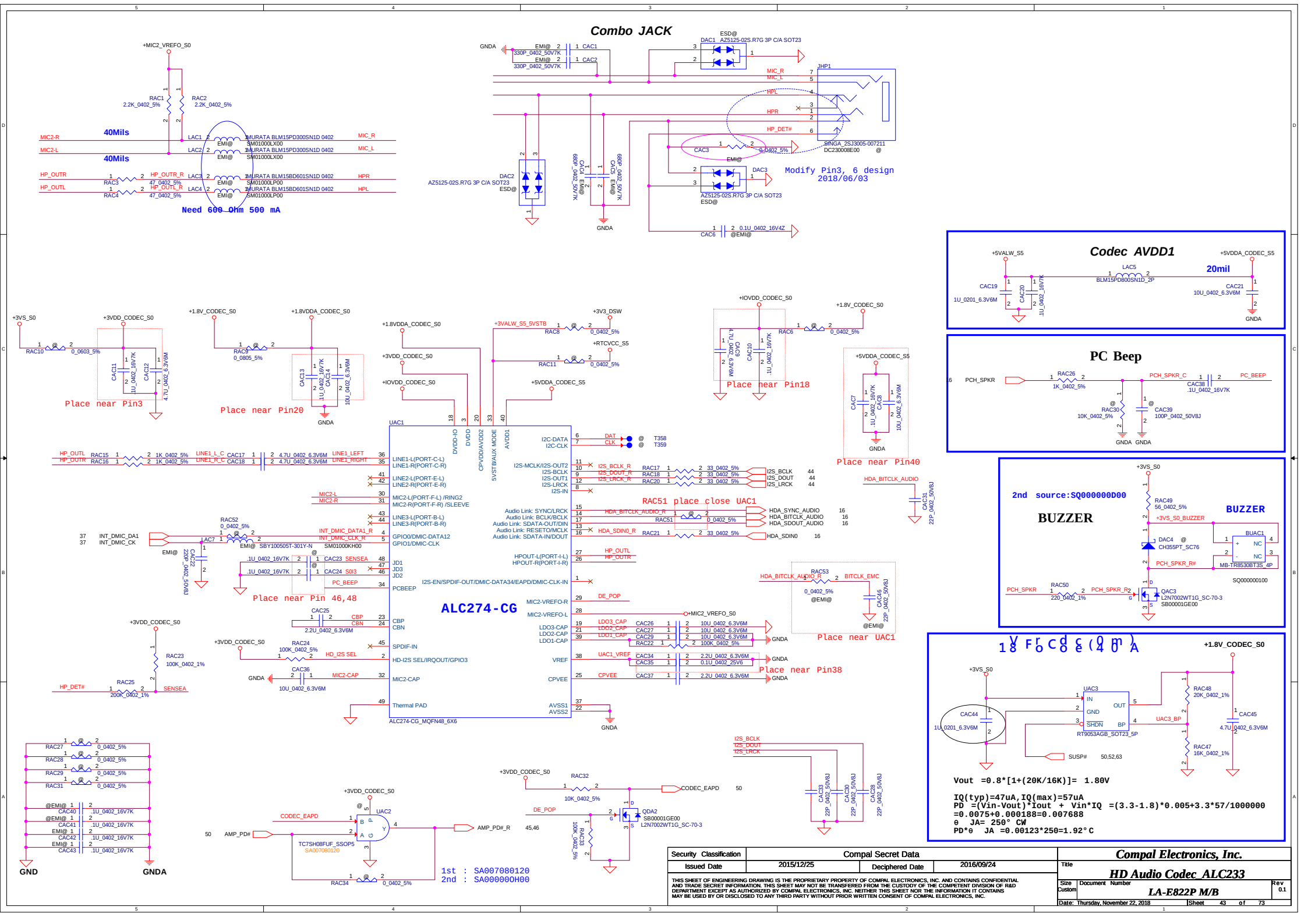
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2013/09/01

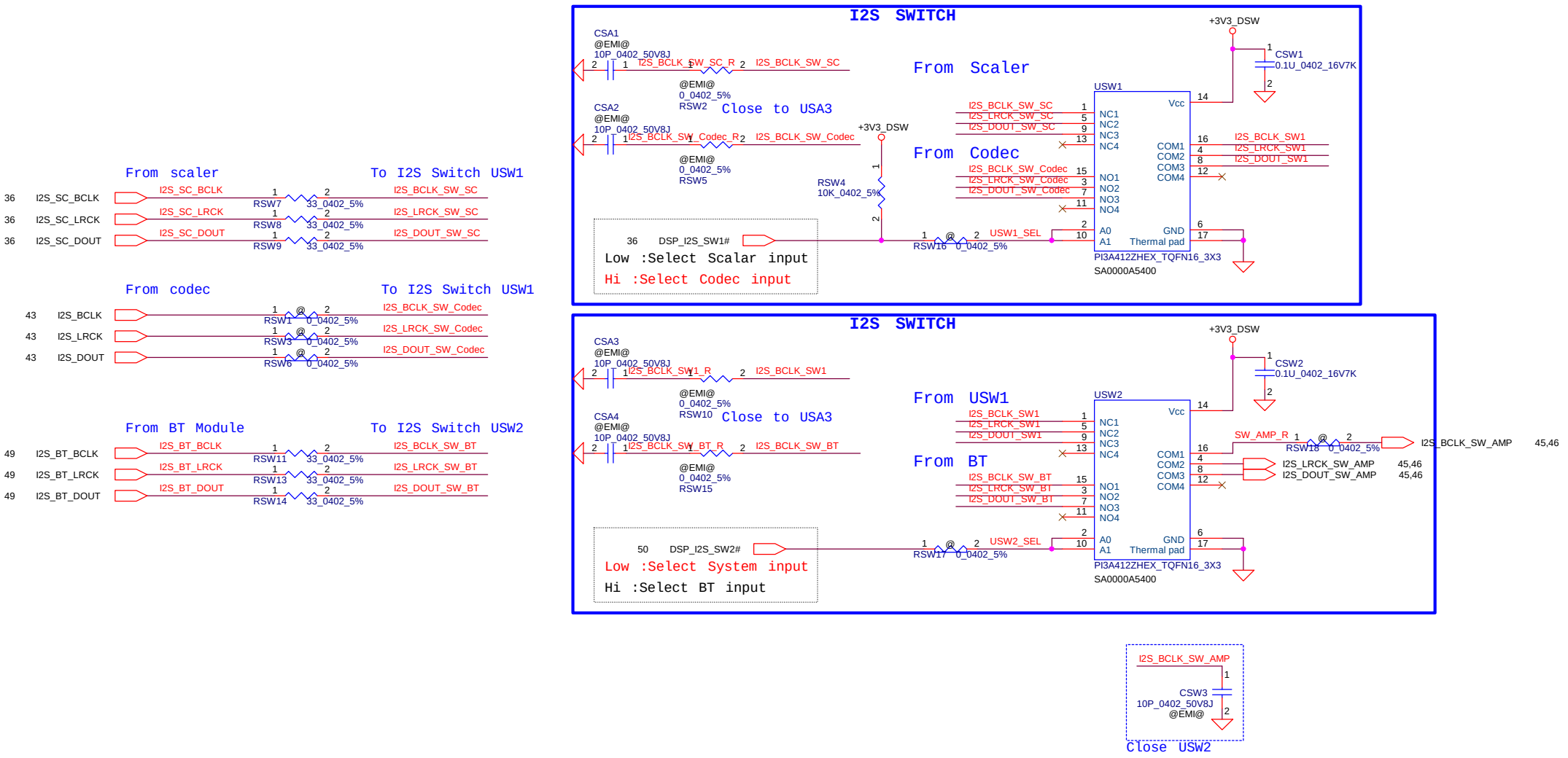
Compal Electronics, Inc.

Title: ***CardReader RTS5176***

Size	Document Number	Rev
Custom	LS-E881P	1.0

Date: Thursday, November 22, 2018 Sheet 42 of 73


Combo JACK
ALC274-CG
ALC274-CG_MQFN48_6X6
Codec AVDD1
PC Beep
BUZZER
2nd source:SQ000000D00
Place near Pin3
Place near Pin20
Place near Pin18
Place near Pin40
Place near Pin 46,48
Place near UAC1
Place near Pin38
RAC51 place close UAC1
Need 600 Ohm 500 mA
Modify Pin3, 6 design
2018/06/03
1st : SA007080120
2nd : SA000000H00
Vout =0.8*[1+(20K/16K)]= 1.80V
IQ(typ)=47uA,IQ(max)=57uA
PD =(Vin-Vout)*Iout + Vin*IQ =(3.3-1.8)*0.005+3.3*57/1000000
=0.0075+0.000188=0.007688
θ JA= 250° C/W
PD*θ JA =0.00123*250=1.92° C
Compal Electronics, Inc.
HD Audio Codec_ALC233
LA-E822P M/B
Compal Secret Data
2015/12/25
2016/09/24
Thursday, November 22, 2018
Sheet 43 of 73



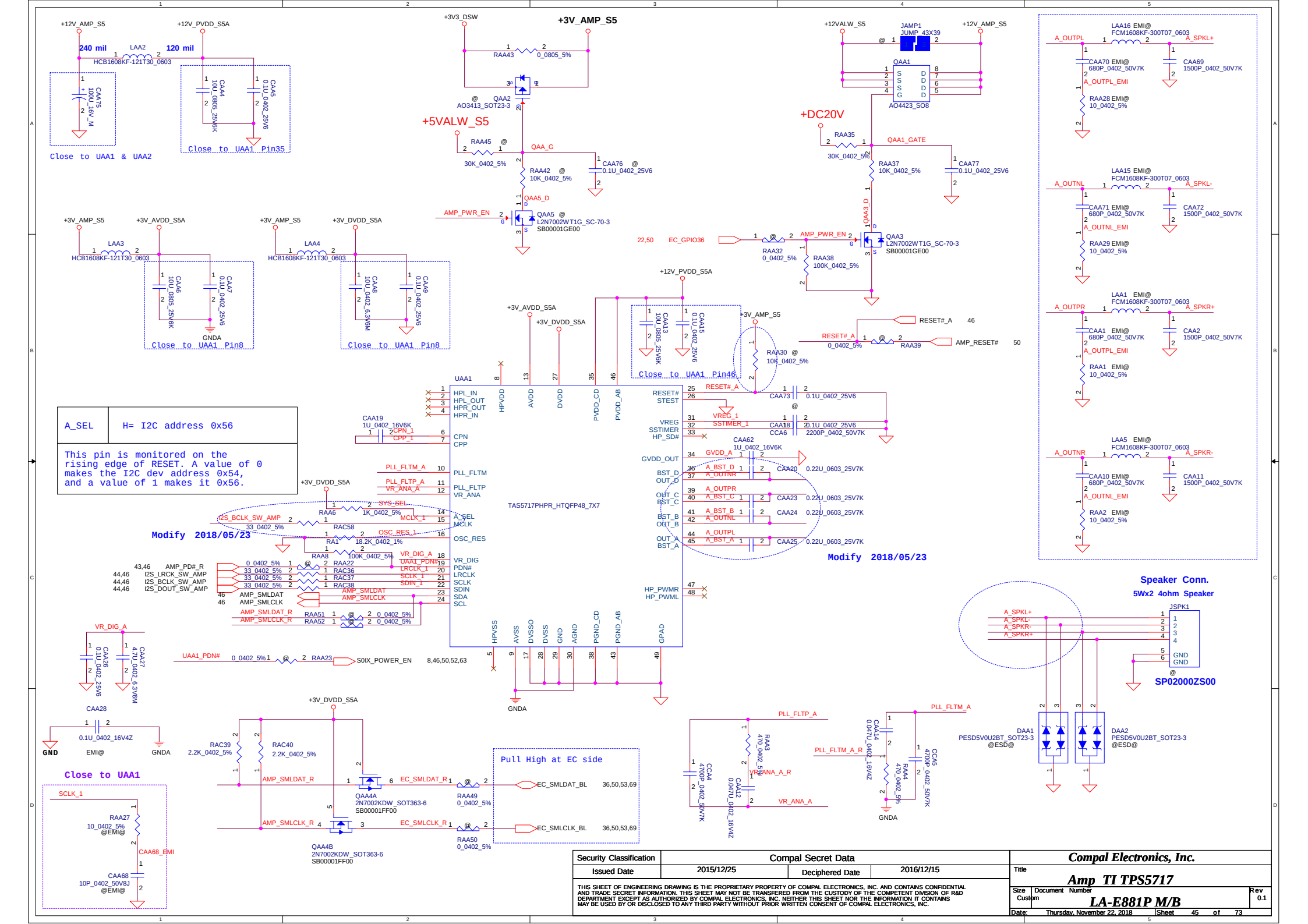
Security Classification	Compal Secret Data		
Issued Date	2014/12/15	Deciphered Date	2016/12/15

Compal Electronics, Inc.

Title: SMART AMP TAS5766MRMTR

Size	Document Number	Rev
B	C7 AIO-530	0.1

Date: Thursday, November 22, 2018 Sheet 44 of 73



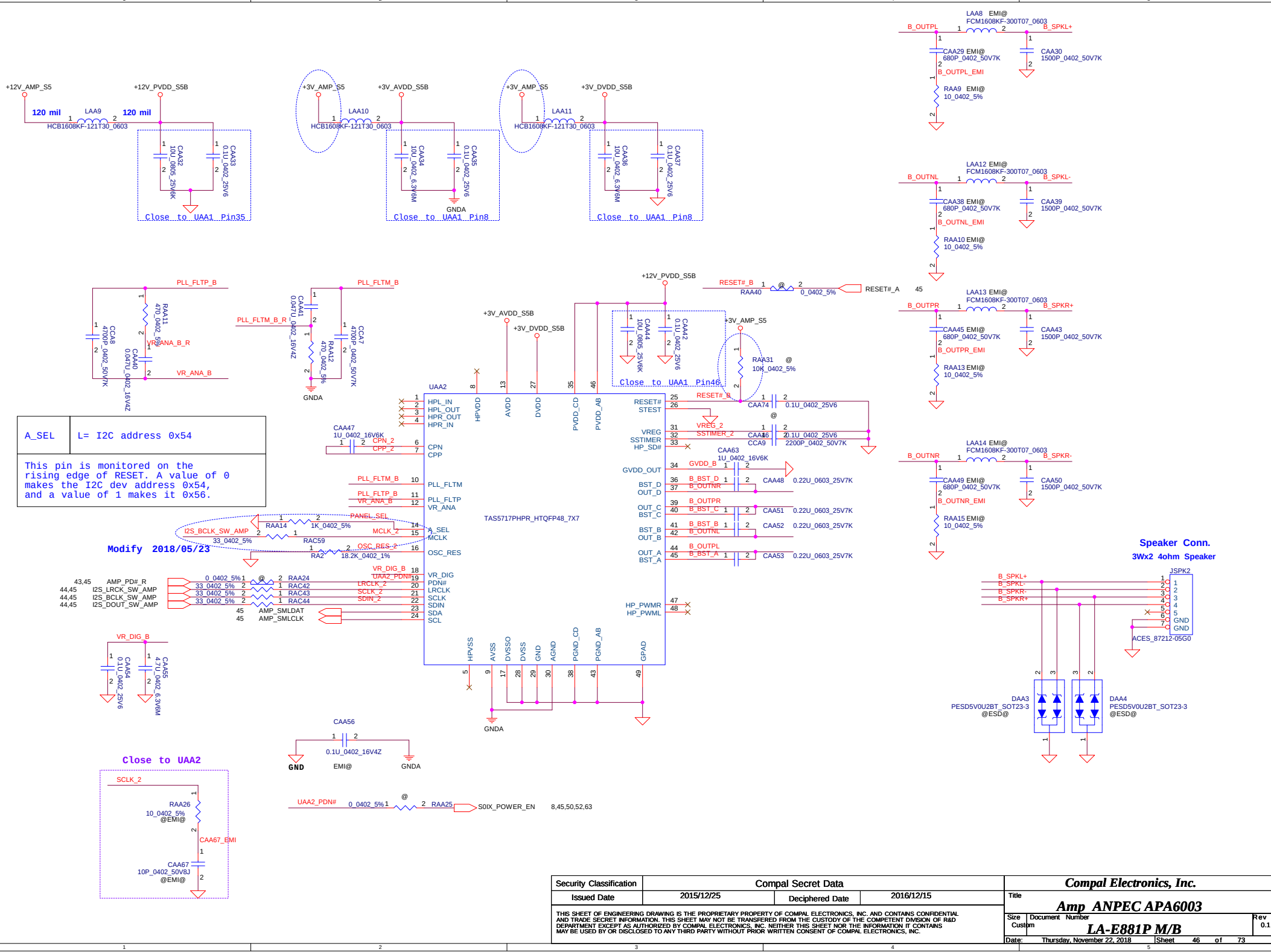
Security Classification	Compal Secret Data
Issued Date	2015/12/25
Deciphered Date	2016/12/15

Compal Electronics, Inc.

Title: **Amp TI TPS5717**

Size	Document Number	Rev
Custom	LA-E881P M/B	0.1

Date: Thursday, November 22, 2018 Sheet 45 of 73



A_SEL	L= I2C address 0x54
This pin is monitored on the rising edge of RESET. A value of 0 makes the I2C dev address 0x54, and a value of 1 makes it 0x56.	

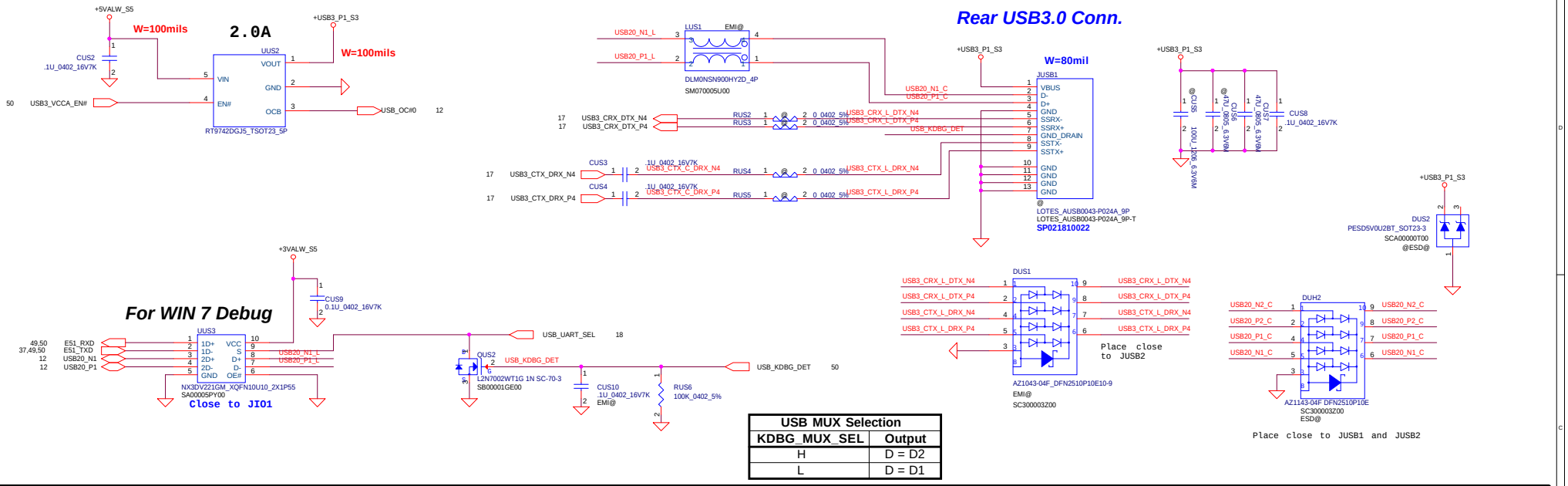
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/12/15

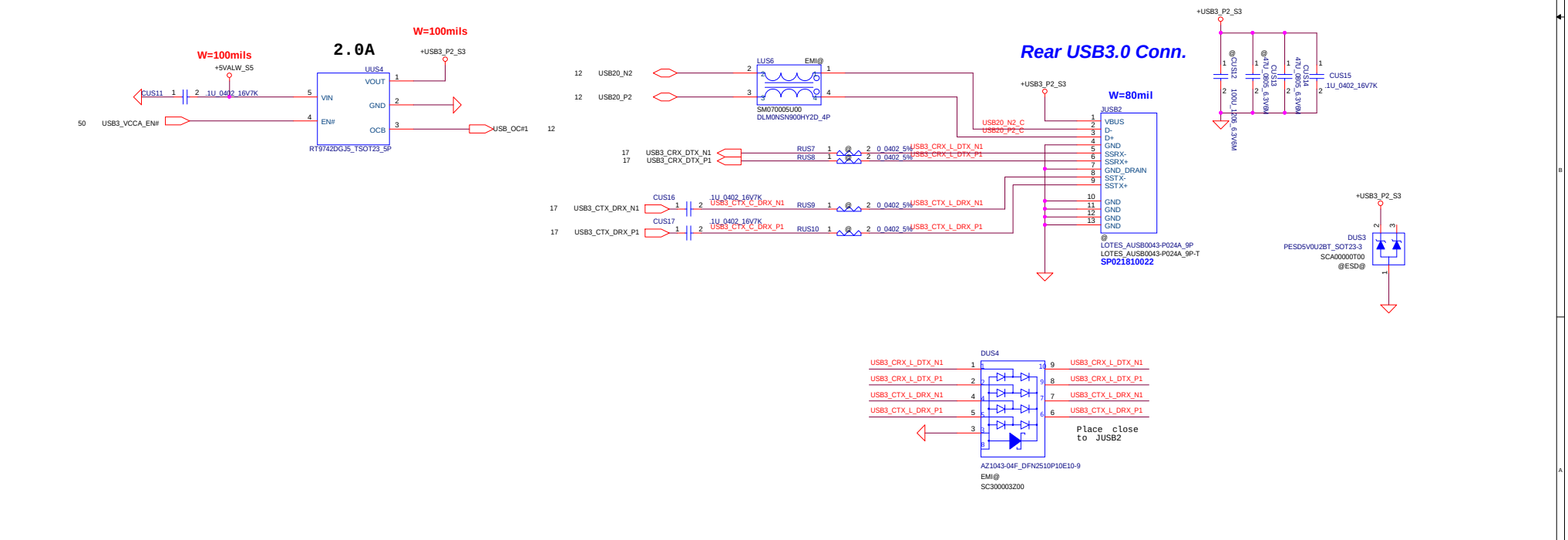
Compal Electronics, Inc.

Title: **Amp ANPEC APA6003**

Size	Document Number	Rev
Custom	LA-E881P M/B	0.1

Date: Thursday, November 22, 2018 Sheet 46 of 73





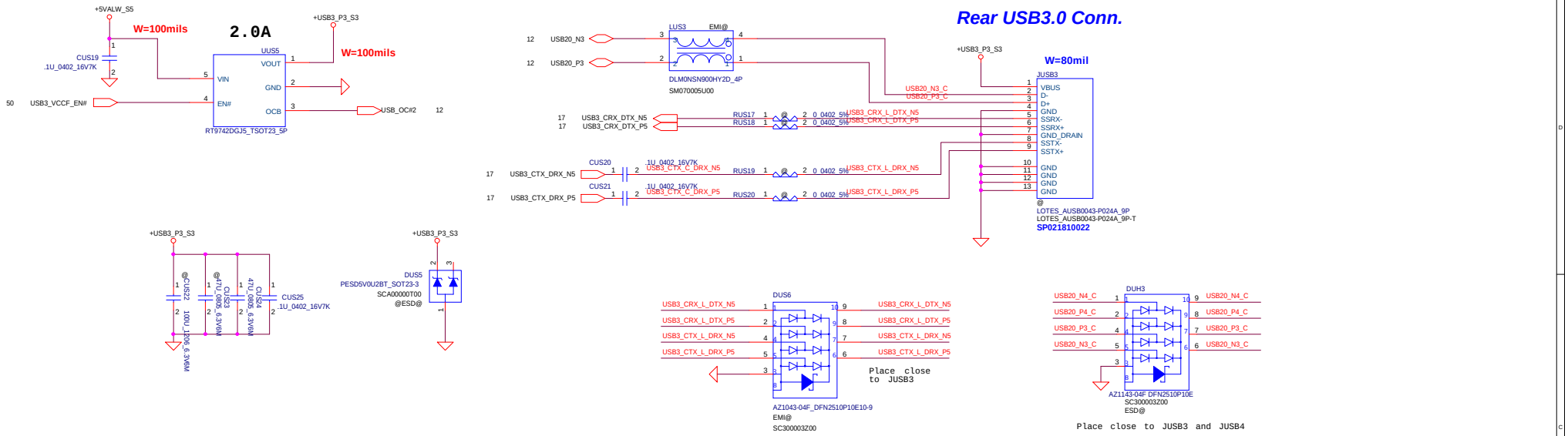
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

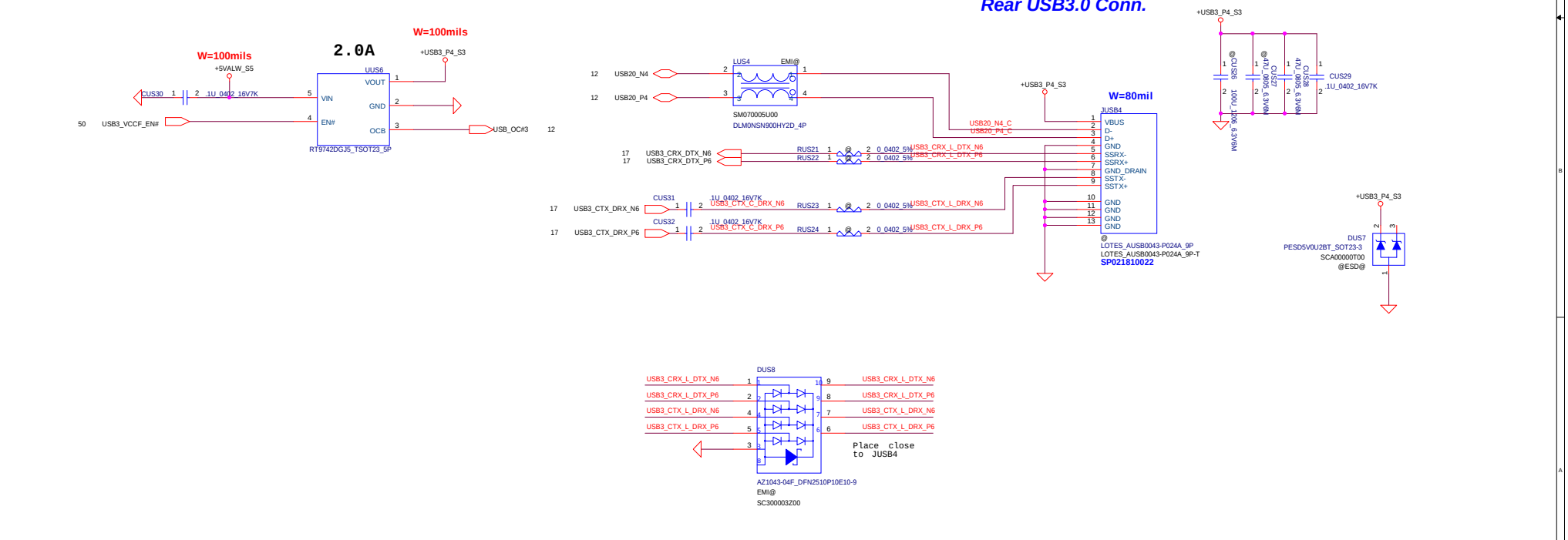
Compal Electronics, Inc.

Title: **Side USB3.0 x 2**

Size	Document Number	Rev
C	LA-E881P M/B	0.1

Date: Thursday, November 22, 2018 | Sheet 47 of 73

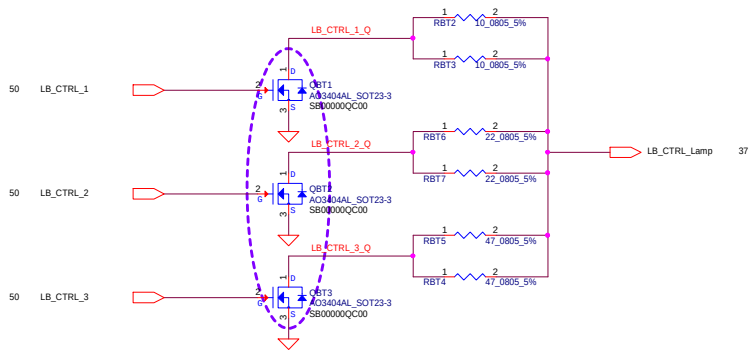




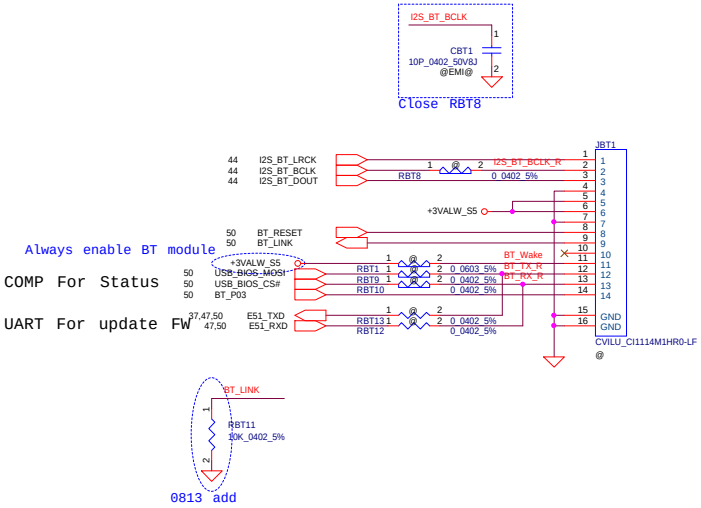
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.	
Title	Side USB3.0 x 2
Size	C
Document Number	LA-E881P M/B
Rev	0.1
Date:	Thursday, November 22, 2018
Sheet	48 of 73

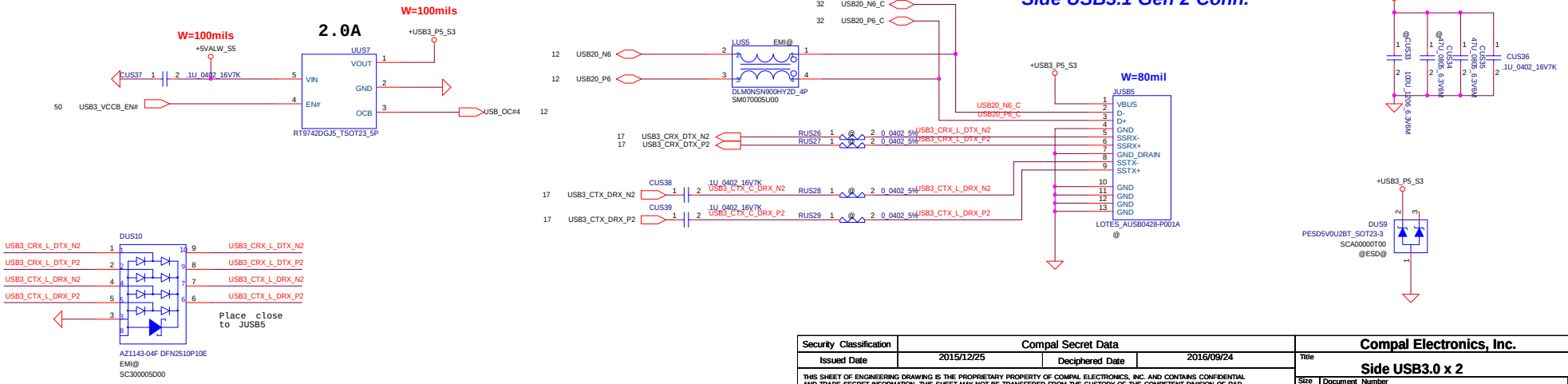
Lamp control



To BT module



Side USB3.1 Gen 2 Conn.



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.			
Title: Side USB3.0 x 2			
Size: C	Document Number: LA-E881P M/B		Rev: 0.1
Date: Thursday, November 22, 2018	Sheet 49 of 73		

Place closely UEC1

LPC_CLK_EC
EC_SPI_CLK
REC2 10_0402_5% @EMI@ REC2_CEC13
REC3 10_0402_5% @EMI@ REC15_CEC8
CEC12 6.8P_0402_50V8C @EMI@
CEC13 33P_0402_50V8J @EMI@
ESD@ CEC18 EC_RSMRST# 5P_0402_50V8C
ESD@ CEC14 VR_ON 1U_0402_16V7K
ESD@ CEC15 PWR_ON_LED# 100P_0402_50V8J
ESD@ CEC16 ON/OFF# 100P_0402_50V8J

V1.0 update

+3V3_DSW
REC1 0_0603_5%
CEC2 10U_0402_6.3V6M
CEC3 1U_0402_16V7K
CEC4 1U_0402_16V7K
CEC5 1U_0402_16V7K
+RTCVCC_S5
REC5 0_0603_5%
+3V3_S0
REC4 0_0603_5%
+RTC_EC_S5
REC7 0_0603_5%
10U_0402_6.3V6M
CEC8
CEC9 1U_0402_16V7K
EC_3VCC_PG
+3V3_EC_DSW
+EC_AVCC
+1.05VS_EC
REC6 0_0603_5%
CEC10 1U_0402_16V7K
CEC11 10U_0402_6.3V6M
+1.05VS_VCCSA_S0
CEC6 1U_0402_16V7K
LEC1 BLM15PD800SN1D_2P
CEC7 @ 10U_0402_6.3V6M
ECAGND

2Mb SPI ROM

+3V3_EC_DSW
CEC1 1U_0402_16V7K
UEC1
EC_SPI_CS# EC_SPI_DO EC_SPI_WP#
CS# DO WP# GND
VCC HOLD# CLK DI
EC_SPI_HOLD# EC_SPI_CLK EC_SPI_DI
W25X20CLSNIG_SO8
SA00003GM30
EC_SPI_HOLD# REC8 4.7K_0402_5%
EC_SPI_WP# REC9 4.7K_0402_5%
+3V3_EC_DSW

A930S modify HDMI-IN function to HDMI_IN_SW

AD Voltage Range: 0 to 2.048 V

EC_SPI_CLK_R REC48 22_0402_5% EC_SPI_CLK
EC_SPI_DO_R REC49 22_0402_5% EC_SPI_DO
EC_SPI_DI_R REC46 22_0402_5% EC_SPI_DI
EC_SPI_CS#_R REC47 22_0402_5% EC_SPI_CS#

Please Close UEC2

UEC2

PANEL_ID1 KB_RST# LPC_FRAME# LPC_AD3 LPC_AD2 LPC_AD1 LPC_AD0 SERIRQ SC_MODE2 EC_SCI# LPC_CLK_EC PLT_RST#
CEC17 ESD@ 100P_0402_50V8J
LPC & MISC
GA20 / SPI_WP# / GPIO11
KBRST# / SPI_HOLD# / GPIO12
LFRAME#
LAD3
LAD2
LAD1
LAD0
SERIRQ#
LDRQ# / GPIO10
PME# / GPEN02
PCICLK
LRESET#
KBC Interface
CTSA# / CIRRX / GPIO20
DSRA# / CIRWB / GPIO21
RTSA# / CIRTX1 / GPIO22 (2E_4E_SEL)
DTRA# / CIRTX2 / GPIO23 (DIS_HWACPI)
SINA / GPIO24
SOUTA_P80 / SOUTA / GPIO25
DCDA# / GPIO26
RIA# / GPIO27
Strapping
Strapping
EC_SIO_SEL HWACPI_DIS E51_RXD E51_TXD
Serial Port Interface
CTSB# / TACHIN / PWMOUT / GPIO50
DSRB# / TACHIN / PWMOUT / GPIO51
RTSB# / TACHIN / PWMOUT / GPIO52
DTRB# / TACHIN / PWMOUT / GPIO53
IRRX / SINB / TACHIN / PWMOUT / GPIO54
IRTX / SOUTB / TACHIN / PWMOUT / GPIO55
DCDB# / TACHIN / PWMOUT / GPIO56
RIB# / TACHIN / PWMOUT / GPIO57
SO1<MOSI>
SI1<MISO>
SCK1
SCE1#
SPI Flash ROM
GPIO70 / TACHIN / PWMOUT / CIRRX
TACHIN / PWMOUT / CIRWB / GPIO71
GPIO72 / TACHIN / PWMOUT / CIRTX1 / TACHPWM
GPIO73 / TACHIN / PWMOUT / CIRTX2 / TACHPWM
GPIO74 / TACHIN / PWMOUT / TACHPWM
GPIO77 / SKTOCC#
Intel PECI/PWR Fault
AMD SB-TSI Int
AMDSIC / PWR_FAULT#
AMDSID / PECI
EC_SMB_DA0 EC_SMB_CK0
SM Bus
GPIO62 / MSDA0
GPIO63 / MSCL0
ON/OFF# PBTN_OUT# EC_RSMRST# PM_SLP_S3# PM_SLP_S4# SYS_PWROK DSW_PWRGD_EC SUSWARN# EC_SMB_DA2 EC_SMB_CK2
ACPI
PSIN# / GPEN04
PSOUT# / GPEN03
RSMRST# / GPEN17
SLP_S3# / GPEN01
SLP_S5# / GPEN06
ATXPGD / GPEN10
GPEN16 / DPWROK
RESETCON# / GPEN05
GPIO95 / BKFD_CUT
RSTOUT0# / GPEN11
GPEN12 / RSTOUT1# / MSDA2
GPEN13 / RSTOUT2# / MSCL2
EC_XIN EC_XOUT
XIN
XOUT
DSP_I2S_SW2# USB_KDBG_DET
DEEP_S5_0 / 3VSBSW / LATCH_BKFD_CUT / GPIO66
3VSBSW# / LATCH_BKFD_CUT# / GPEN07
DEEPS5_1 / CASEOPEN1#
NCT6685D_LQFP128_14X14
VBAT 3VCC 3VSB 3VSB 3VSB AVSB VTT
PWM
GPIO81 / PWMOUT / TACHIN / USB_LED
GPIO82 / PWMOUT / TACHIN / TACHPWM
PWMOUT / TACHIN / GPIO00 / TACHPWM
PWMOUT / TACHIN / GPIO01 / TACHPWM
Strapping
CIRTX1/(AMDPWR_EN) / CIRTX1 / GPIO05
TACHIN / PWMOUT / GPIO83
TACHIN / PWMOUT / GPIO84
AD Input
V_COMP0 / THR0 / VIN0
V_COMP1 / THR1 / VIN1
V_COMP2 / THR2 / VIN2
V_COMP3 / THR3 / VIN3
THR16 / VIN16 / TD2P
THR15 / VIN15 / TD1P
THR14 / VIN14 / TD0P
SMI# / OVT# / GPIO85
STB# / GPIO13 / GRN_LED
GPIO67 / CASEOPEN#
GPIO80
USB
USB_D+
USB_D-
KBC Interface
MCLK / MCU_TDI / DB_SO / USB_MISO
MDAT / MCU_TDO / DB_SI / DB_TX / USB_CS#
MCU_TCK / DB_SCK / KCLK / USB_SCK
DB_RX / MCU_TMS / DB_SCE# / KDAT / USB_MOSI
TACHIN / PWMOUT / TACHPWM / GPIO03
MSDA1 / VCORE_EN / GPIO76 (s)
TACHIN / PWMOUT / TACHPWM / GPIO02
MSCL1 / VLDT_EN / GPIO75 (s)
GPIO
SLCT / GPIO30 / YLW_LED
P2_DGL# / PE / GPIO31
P2_DGL# / BUSY / GPIO32
P2_DGH# / ACK# / GPIO33
P2_DGH# / PD7 / GPIO34
LED_A / PD6 / GPIO35
LED_B / PD5 / GPIO36
LED_C / PD4 / GPIO37
LED_D / PD3 / GPIO40 / CSOUT#
LED_E / PD2 / GPIO41 / CHPST_MOSI
LED_F / PD1 / GPIO42
LED_G / PD0 / GPIO43 / CHPST_SCK
P1_DGL# / SLIN# / GPIO44
P1_DGL# / INIT# / GPIO45 / CHPST_MISO
P1_DGH# / ERR# / GPIO46
P1_DGH# / AFD# / GPIO47 / CHPST_CS#
DSW
PCHVSB
GPIO90 / SUSWARN#
5VDUAL
GPIO91 / SUSWARN_5VDUAL
GPIO92 / SUSACK#
SLP_SUS# / GPIO93 / 3VSUSW#
GPIO94 / SLP_SUS_FET
AMD Power-On Sequence
VCORE / THR5 / VIN5
VLDT / THR6 / VIN6
VDIMM / THR7 / VIN7
PSON# / AMD_PSON# / GPEN00
PWROK0 / AMD_PWROK0 / GPEN14
PWROK1 / AMD_PWROK1 / GPEN15
VREF PAD_CAP
VSS VSS AGND
+EC_VREF EC_PAD_CAP CEC19 4.7U_0402_6.3V6M CEC20 4.7U_0402_6.3V6M
LEC2 BLM15PD800SN1D_2P
ECAGND

A930S modify HDMI-IN function to HDMI_IN_SW

HDMI_IN_SW PCIE_WAKE# FAN_SPEED FAN_PWM
AMDPWR_EN REC101 4.7K_0402_5% LB_BUTTON LB_CTRL_3
AD_BID REC111 10K_0402_5%
PANEL_ID0 LAN_PHY_DIS# SCALER_ON#
USB_BIOS_MISO USB_BIOS_CS# USB_BIOS_CLK USB_BIOS_MOSI
REC51 REC52 REC53 REC54 33_0402_5%
INA300_LATCH H_PROCHOT#_EC
HDMI_IN_OUT_HPD
EC_GPIO30 SUSP EC_GPIO36 AMP_PD#
EC_1.05V_EN
SUSP# EC_BKOFF# PWR_ON_LED# EC_GPIO36 AMP_PD#
SLP_S0#_R REC30 0_0402_5%
PM_SLP_S0# EC_GPIO41 INA300_ALERT# S0IX_POWER_EN
REC32 0_0402_5%
CODEC_EAPD BT_RESET HW_12V_EN USB3_VCCD_EN#
EC_PCHVSB REC36 4.7K_0402_5% +3V3_EC_DSW
USB3_VCCA_EN#
EC_CRISIS EC_CRISIS_KSO0 SC_MODE1 EC_5V_EN
AC_PRESENT PCH_PWROK VCCST_PWRGD_EC

EC debug only

Ra (100K) REC12 100K_0402_5%
AD_BID
Rb (Max:150k) REC15 100K_0402_5%

EVT(v0.1) : 30K Ohm : 0.76V
DVT(v0.2) : 56K Ohm : 1.18V
PVT (v1.0) : 150K Ohm : 1.98V
MP(v1.1) : 100K Ohm : 1.67V

JDB1
USB_BIOS_CLK USB_BIOS_MISO USB_BIOS_CS# USB_BIOS_MOSI
EC debug only
CVILU_CH31052VA00-NH

LPC Address Select:
0: 2Eh/2Fh
1: 4Eh/4Fh

+3VS_S0
REC14 4.7K_0402_5%
EC_SIO_SEL
REC17 @ 4.7K_0402_5%

EC DEBUG port

REC18 100K_0402_5% E51_TXD

A930S ADD for charger

+3V3_EC_DSW
REC251 10K_0402_5% SUSP
REC27 4.7K_0402_5% HWACPI_DIS
REC28 4.7K_0402_5% EC_CRISIS

CEC26 .1U_0402_16V7K EC_RTCRST
REC35 10K_0402_5% AC_PRESENT
REC37 4.7K_0402_5% SYSON
REC38 10K_0402_5% VR_ON
REC39 10K_0402_5% SUSP#
REC231 10K_0402_5% HW_12V_EN

+3V3_EC_DSW
REC40 2.2K_0402_5%
REC41 2.2K_0402_5%
CEC21 100P_0402_50V8J
CEC22 100P_0402_50V8J
EC_SMB_CK2
EC_SMB_DA2
REC43 0_0402_5% EC_SMLCLK_BL
REC45 0_0402_5% EC_SMLDAT_BL

EC_XOUT REC44 1M_0402_5% EC_XIN
YEC1 OSC NC NC OSC 14.31818MHZ_12PF_X3G01431ADC1H
CEC24 15P_0402_50V8J
CEC25 15P_0402_50V8J

VR_HOT From power CPU_CORE
REC42 0_0402_5% H_PROCHOT#
H_PROCHOT#_EC
QEC1 2N7002BKW_SOT323-3 SB00001GE00
CEC23 47P_0402_50V8J

AC in-->One touch -->Power button--> Clear CMOS
Always short-->AC in-->Power button--> Crisis

JCRIS1
EC_CRISIS_KSO0 EC_CRISIS
CVI_CH31022M107-0P

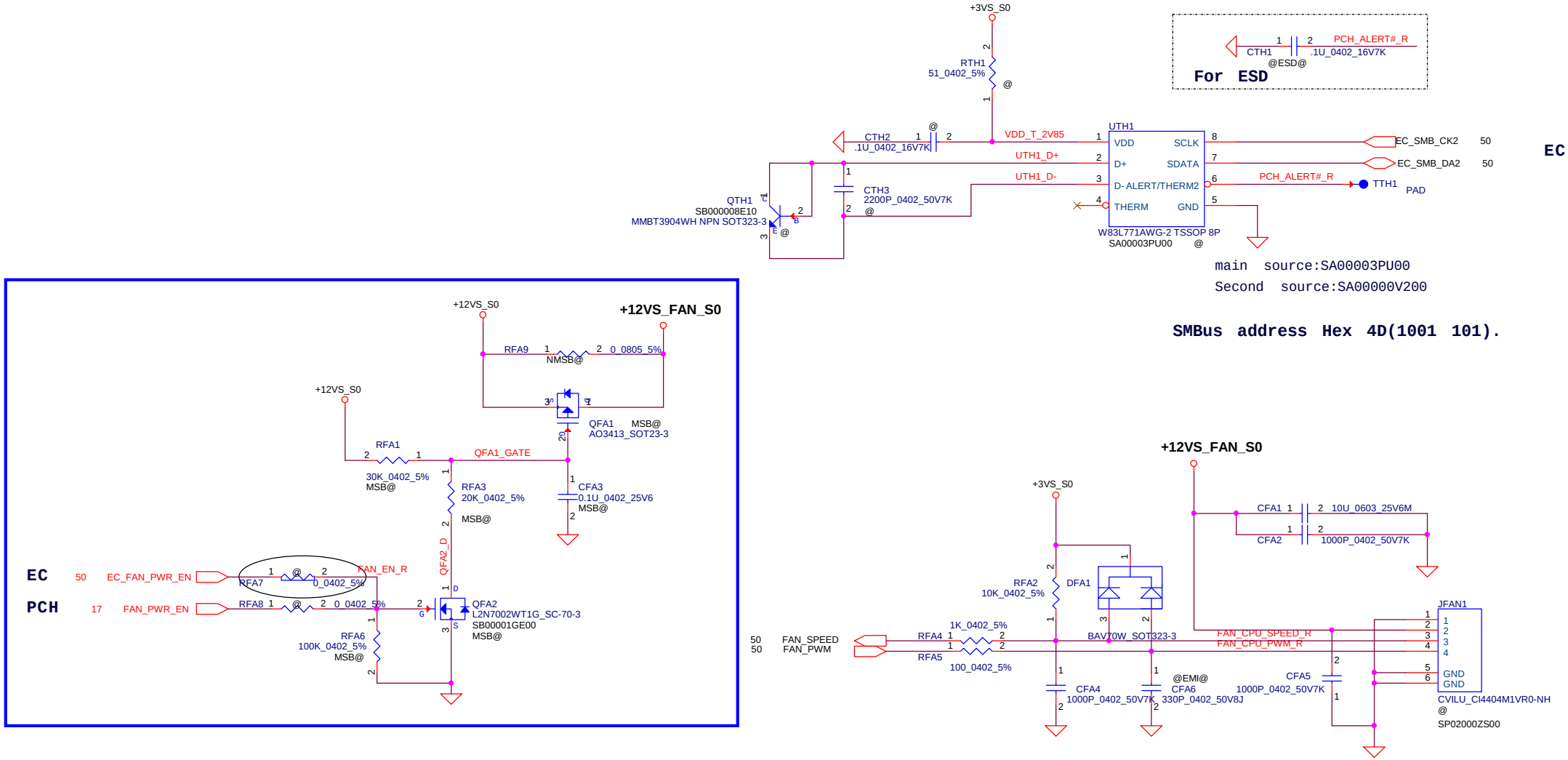
Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: EC NCT6685

Size	Document Number	Rev
Custom	LA-E881P M/B	0.1

Date: Thursday, November 22, 2018 Sheet 50 of 73



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2015/10/02

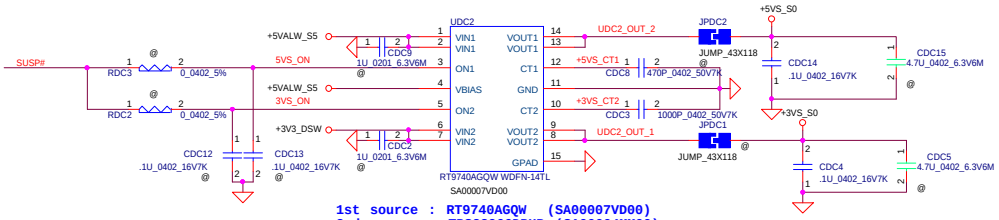
Compal Electronics, Inc.

Title: **FAN/Thermal Sensor**

Size	Document Number	Rev
	LA-E881P M/B	0.1

Date: Thursday, November 22, 2018 Sheet 51 of 73

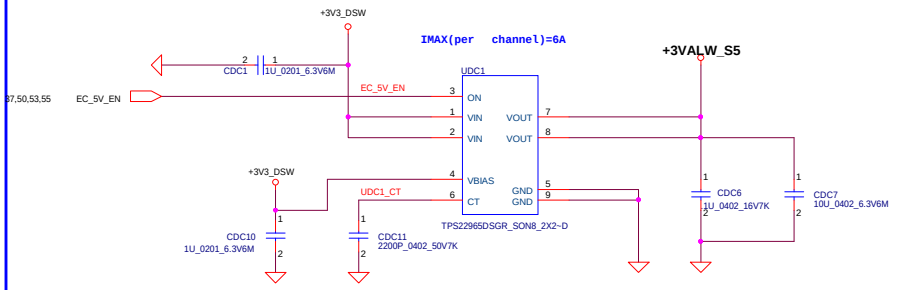
VIN 5V and 3.3V (VBIAS=5V),IMAX(per channel)=6A,Rds=18mohm



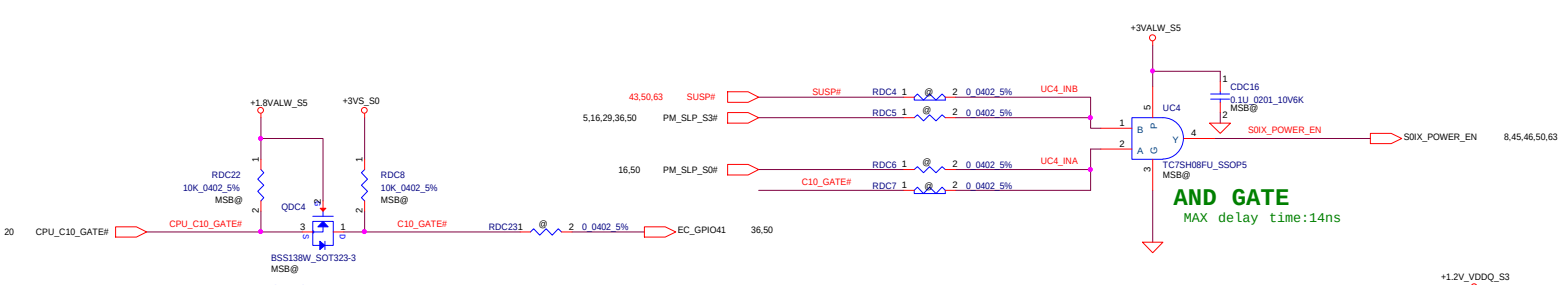
1st source : RT9740AGQW (SA00007VD00)
2nd source : TPS22966DPUR (SA00004MM00)

+3VDSW_S5 to +3VALW_S5 Transfer

IMAX(per channel)=6A

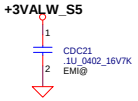


1st source : APL3526 (SA00006R100)
2nd source : TPS22965 (SA00005X50L)



Vgs(max)=1.5V

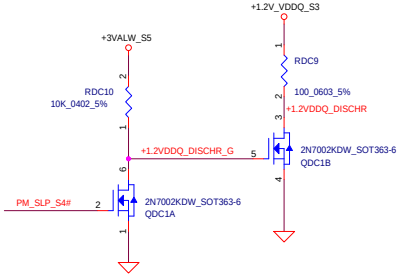
1nd source : BSS138W_PANJIT (SB00000T000)
2st source : LBSS139WT1G_LRC (SB00001GC00)

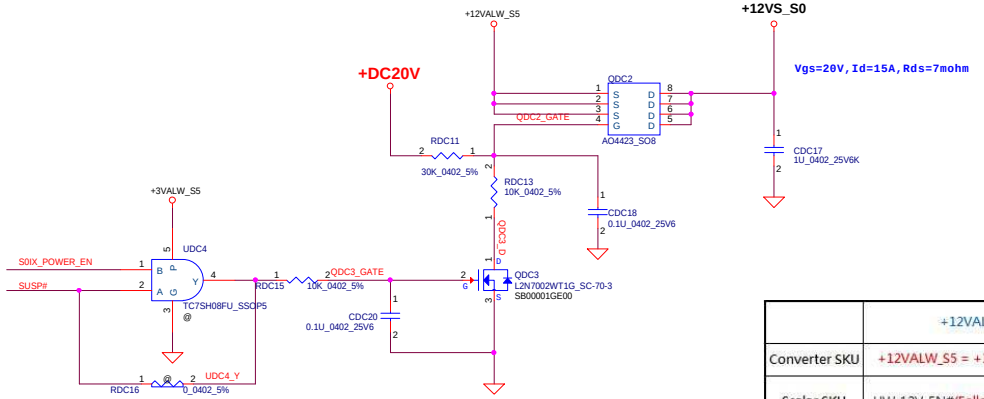


AND GATE

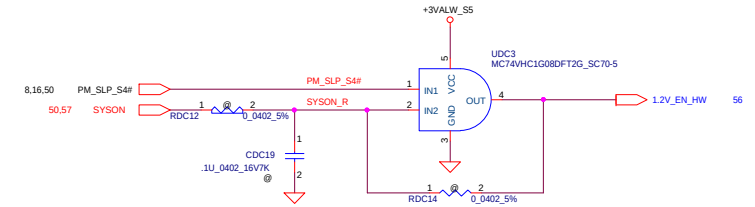
MAX delay time:14ns

+12VALW_S5 TO +12VS_S0 (PMOS)





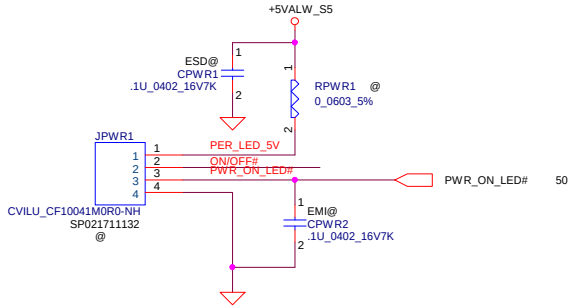
Vgs=20V,Id=15A,Rds=7mohm

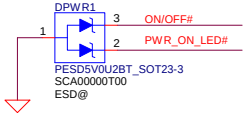


	+12VALW_S5	+12VS_S0	BOM
Converter SKU	+12VALW_S5 = +12VS_S0 , Enable: HW_12V_EN# (Follow SPL_S3#)		RDC7,RDC8,RDC9
Scalar SKU	HW_12V_EN#(Follow SCALER_ON#)	SUSP# (Follow SPL_S3#)	QDC2,RDC10,RDC16,RDC17,CDC19,CDC17

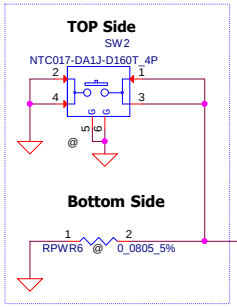
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2015/12/25	Deciphered Date 2016/03/27	Title: DC INTERFACE
			Size: C; Document Number: LA-E881P M/B; Rev: 0.1
			Date: Thursday, November 22, 2018; Sheet 52 of 73

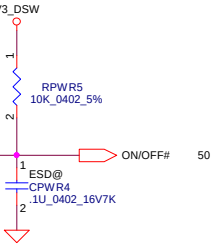
Power Button



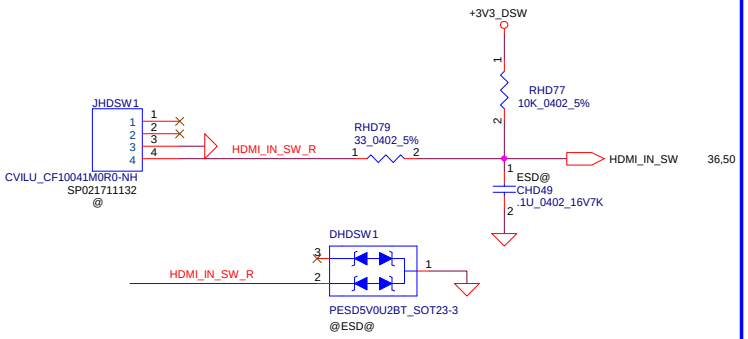


ON/OFF switch

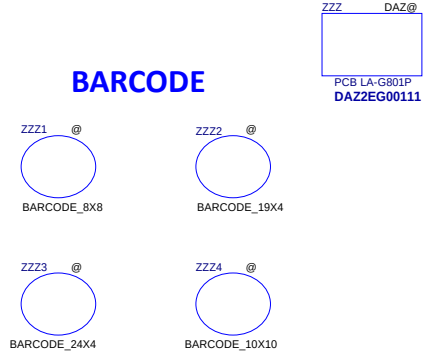


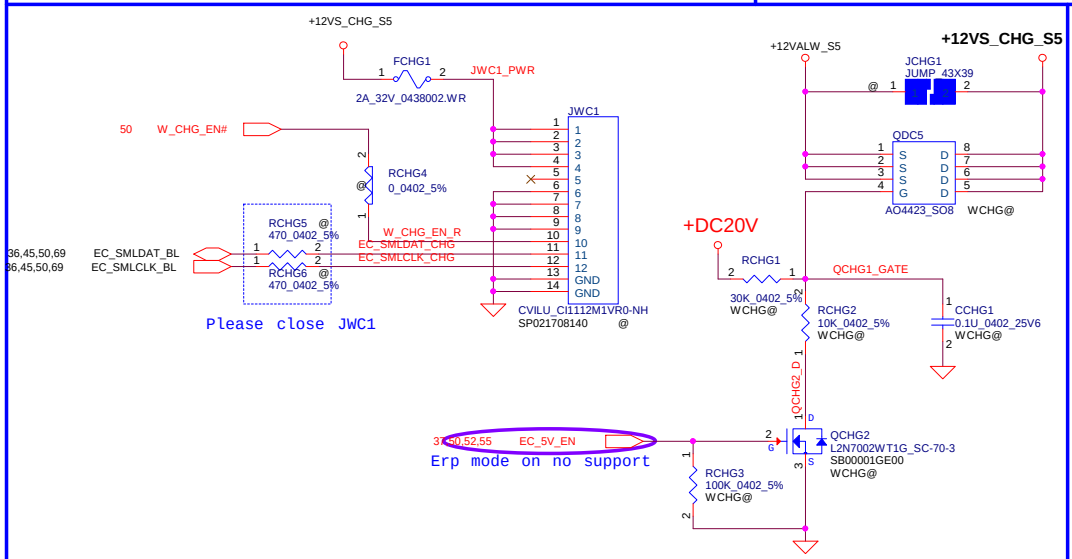


HDMI Button board

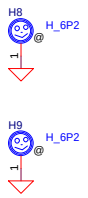


BARCODE



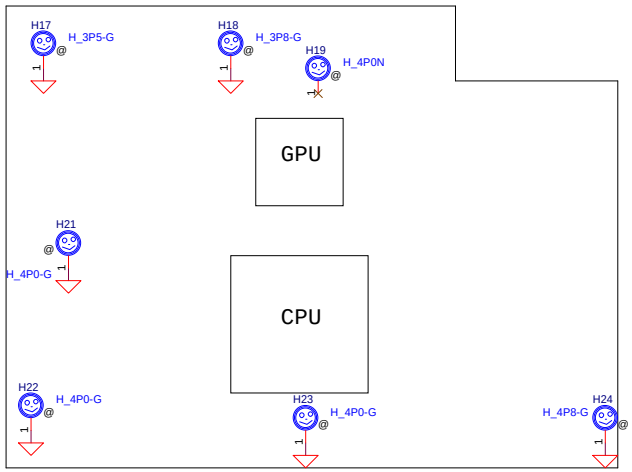


SSD Hole



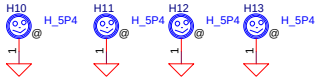
Screw Hole

5.4mm x 2 4.0 mm x 11

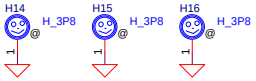


CPU Hole

5.4mm x 4

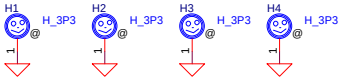


3.8 mm x 3

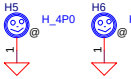


GPU Hole

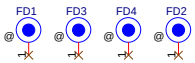
3.3 mm x 4



Speaker



FAN



Security Classification	Compal Secret Data		
Issued Date	2015/12/25	Deciphered Date	2016/09/24

Compal Electronics, Inc.

Title: **PWR SW/LED/SCREW**

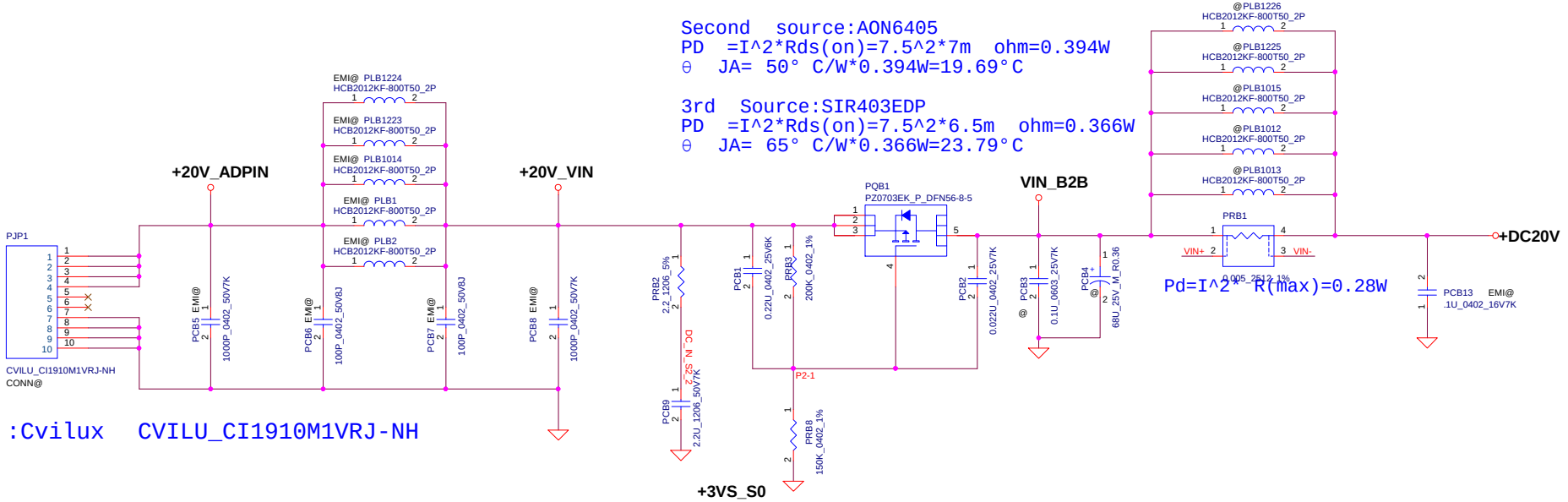
Size	Document Number	Rev
Custom	LA-E881P M/B	0.1

Date: Thursday, November 22, 2018 Sheet 53 of 73

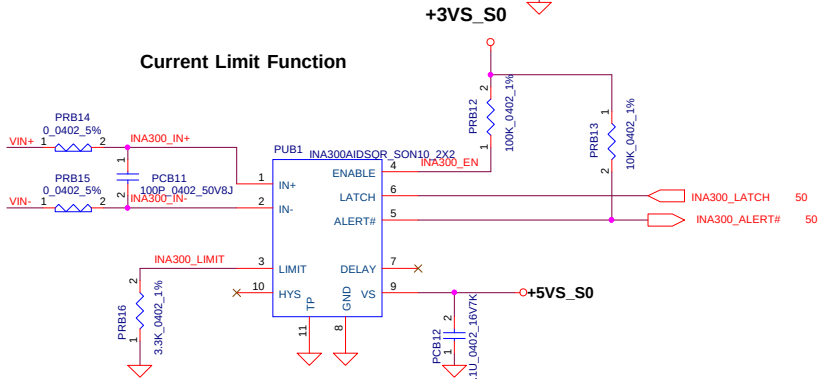
Main source:PZ0703EK
PD =I^2*Rds(on)=7.5^2*7m ohm=0.394W
θ JA= 50° C/W*0.394W=19.69°C

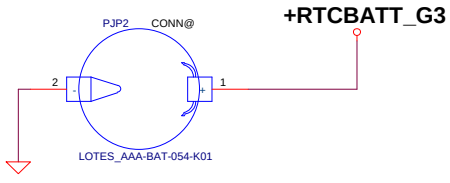
Second source:AON6405
PD =I^2*Rds(on)=7.5^2*7m ohm=0.394W
θ JA= 50° C/W*0.394W=19.69°C

3rd Source:SIR403EDP
PD =I^2*Rds(on)=7.5^2*6.5m ohm=0.366W
θ JA= 65° C/W*0.366W=23.79°C



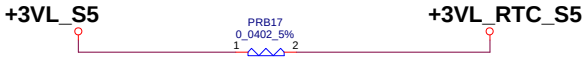
main source :Cvilux CVILU_CI1910M1VRJ-NH





DIS SKU 230W:
Full Load(100%) --> 11.5A
Vtrip=7.5*5m=57.5mV
VLimit=Vtrip; Rlimit=(57.5mV+0.5mV)/20uA= 2.9K

Trigger(120%) --> 13.1A (@262W)
Vtrip=13.1*5m=65.5mV
Rlimit=(65.5mV+0.5mV)/20uA=3.475K
Select Rlimit=3.3K
I_Trigger-->13.1A



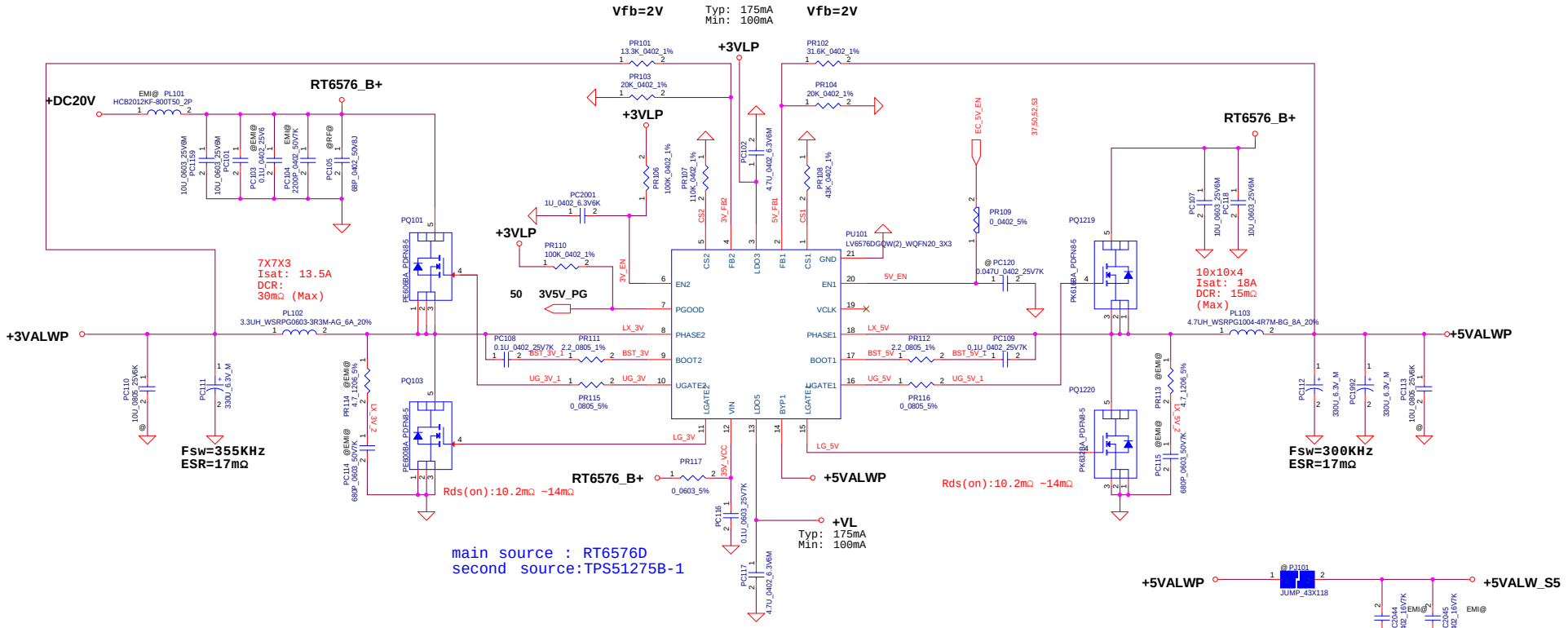
Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: ***DCIN/CONN***

Size	Document Number	Rev
Custom		0.1

Date: Thursday, November 22, 2018 Sheet 54 of 73




```
+3VALWP
Vin = 20V
Iin  =3.3*6.8/0.85/20
     = 1.32A
```

```
Vout  =  Vfb*[1+(Rt/Rb)]
      = 2*[1+(13.3K/20K)]
      = 3.3V
```

```
+3VALWP
Imax=4.9A  ;  Ipeak=7A  ;Fsw=355KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds  :  L/S  -->  typ:10.2mohm  ;  max:  14mohm
Itrip=9~11  uA
Iocp(set)=10A~13.5A
Iin_ripple=1.66A
Output  Cap.  ESR=17mohm
Delta   IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.352A
LIR=Delta  IL/Ipeak=0.367
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=240.02uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.87uF
```

```
+5VALWP
Vin = 20V
Iin  =5*10.76/0.85/20
     = 3.16A
```

```
Vout  =  Vfb*[1+(Rt/Rb)]
      = 2*[1+(30K/20K)]
     =5V
```

```
+5VALWP
Imax=7.53A,Ipeak=10.76A   ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds  :  L/S  -->  typ:3 ohm  ;  max:  4mohm
Itrip=9~11  uA
Iocp(set)=17.2A~21A
Iin_ripple=2.56A
Output  Cap.  ESR=17mohm
Delta   IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.660A
LIR=Delta  IL/Ipeak=0.315
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=243.73uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.85uF
```

Security Classification	Compal Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: 3V/5V (RT6576D)

Size: C | Document Number | Rev: 0.1

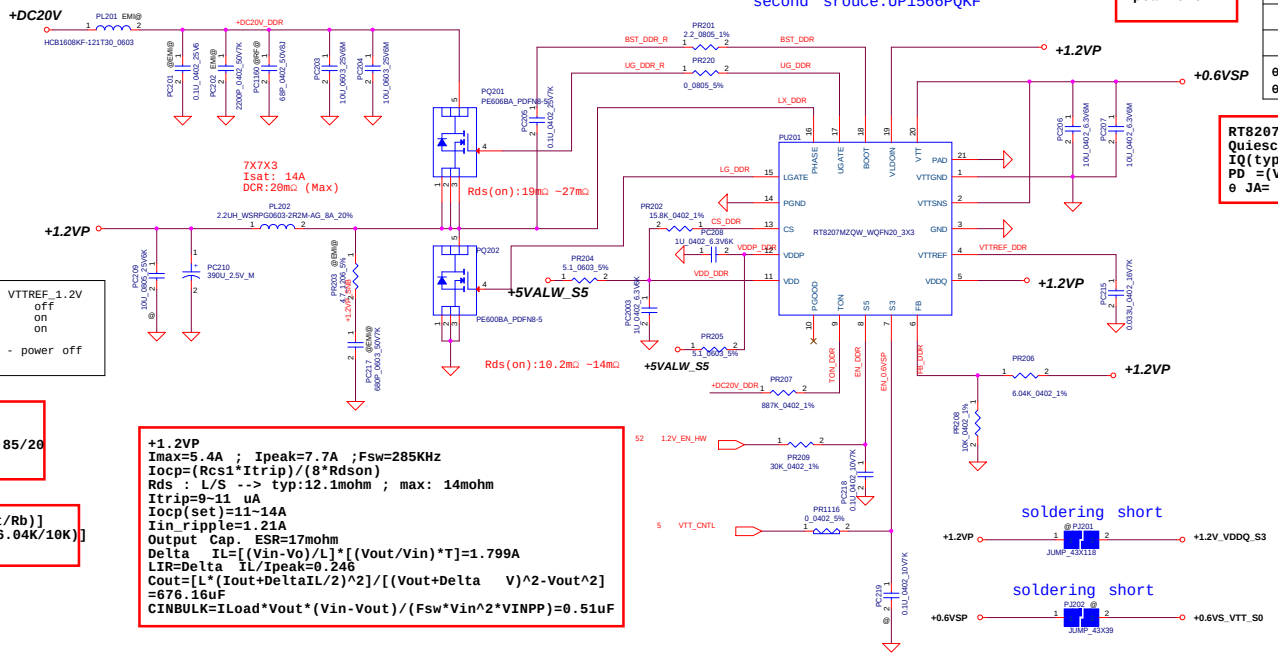
Date: Thursday, November 22, 2018 | Sheet 55 of 73

main source : RT8207MZQW
second srouce:UP1566PQKF

+0.6VSP
TDC=0.42A
Ipeak=0.6A

Vo	0.6	
Vin	1.2	
Io	0.75	
PD	0.455	
θ JA(main)	52	° C/W
θ JA(2nd)	68	° C/W

RT8207M:
Quiescent Current (GND Current)
IQ(typ)=0.47mA,IQ(max)=1mA
PD =(Vin-Vout)*Iout + Vin*IQ =0.455W
θ JA= 33.7° C/W*0.903=23.66°C



Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

+1.2VP
Vin = 20V
Iin = 7.3*1.2/0.85/20
= 0.51A

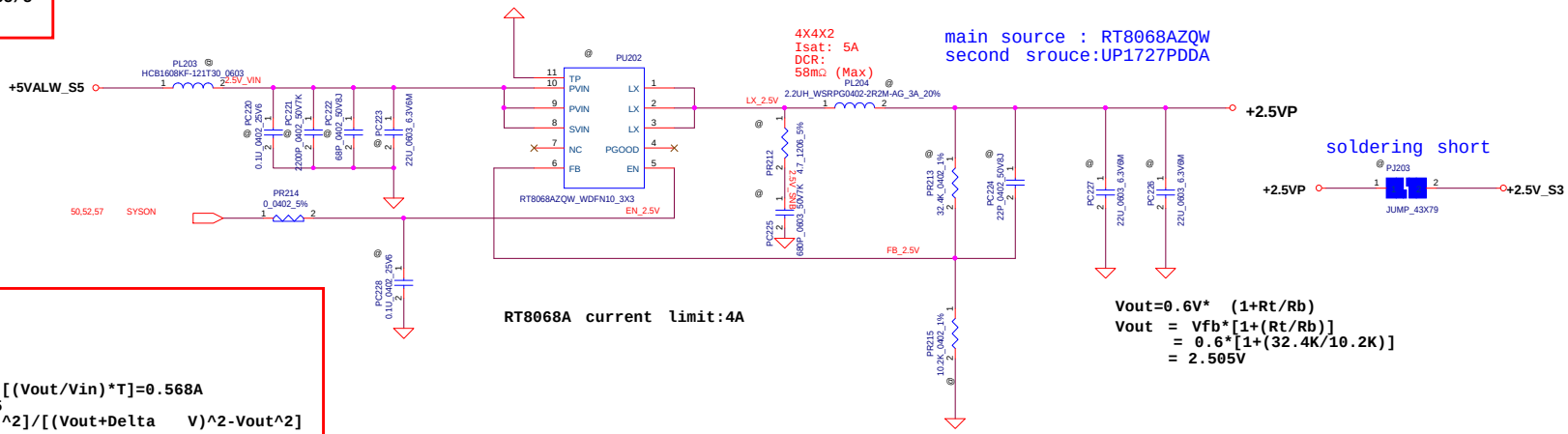
Vout = Vfb*[1+(Rt/Rb)]
= 0.75*[1+(6.04K/10K)]
= 1.203V

+1.2VP
Imax=5.4A ; Ipeak=7.7A ;Fsw=285KHz
Iocp=(Rcs1*Itrip)/(8*Rdson)
Rds : L/S --> typ:12.1mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11~14A
Iin_ripple=1.21A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.799A
LIR=Delta IL/Ipeak=0.246
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=676.16uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.51uF

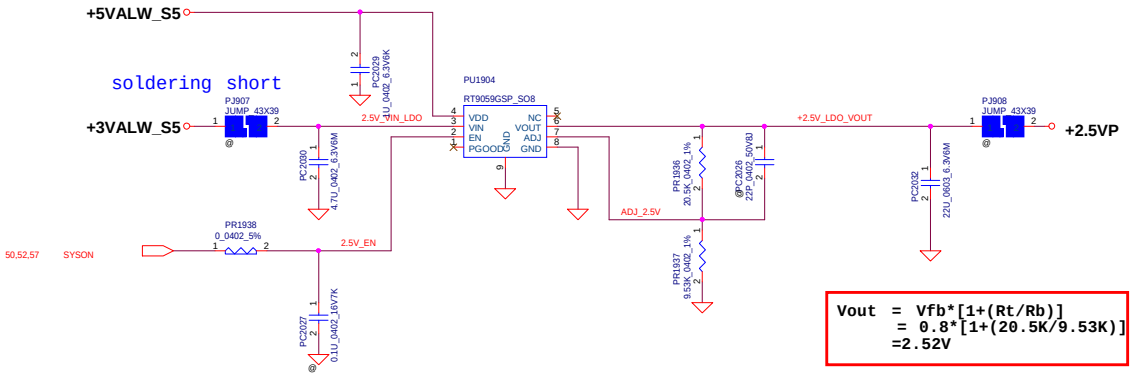
Security Classification	Compal Secret Data		
Issued Date	2015/07/27	Deciphered Date	2016/07/27

Compal Electronics, Inc.
Title: 1.2VP/0.6VSP(RT8207M)
Size: Custom | Document Number | Rev: 0.1
Date: Thursday, November 22, 2018 | Sheet 56 of 73

+2.5VP
Vin =5V
Iin = 2.5*2.24/0.85/5
=1.32A



+2.5VP
Ipeak=1.5A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.75A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.568A
LIR=Delta IL/Ipeak=0.25
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=11.8uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.78uF



Security Classification	Compal Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/29

Compal Electronics, Inc.

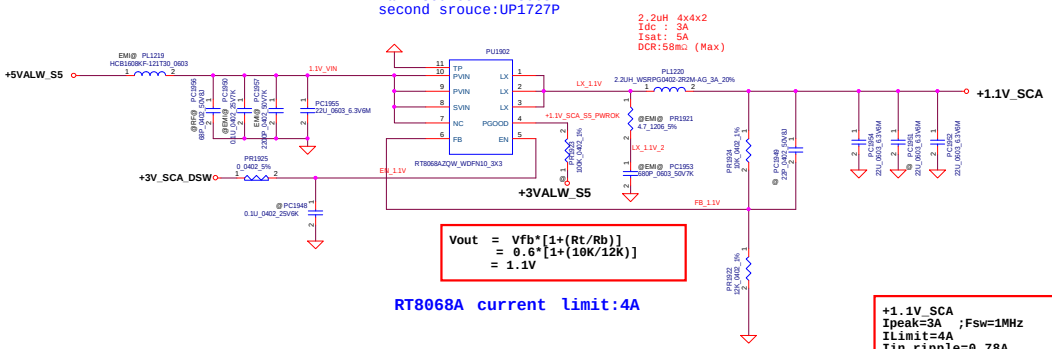
Title: 2.5VP(RT8068A)

Size: C | Document Number | Rev: 0.1

Date: Thursday, November 22, 2018 | Sheet 57 of 73

+1.1V_SCA
Vin =5V
Iin =1.1*1.94/0.9/5
=0.58A

main source : RT8068A
second srouce:UP1727P



Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(10K/12K)]
= 1.1V

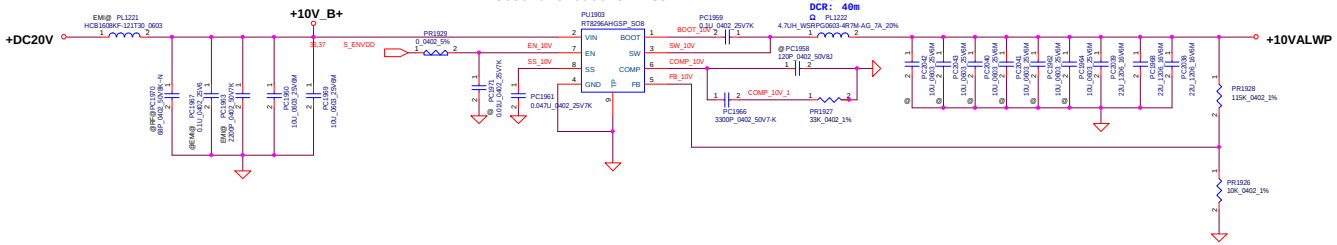
RT8068A current limit:4A

+1.1V_SCA ⟷ +1.1V_SCA_S5
soldering short

+1.1V_SCA
Ipeak=3A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.78A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.39A
LIR=Delta IL/Ipeak=0.163
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=77.75uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

+10VALWP
Vin =20V
Iin = 10*1.04/0.85/20
=0.61A

main source : RT8296A
second srouce:UP1735P



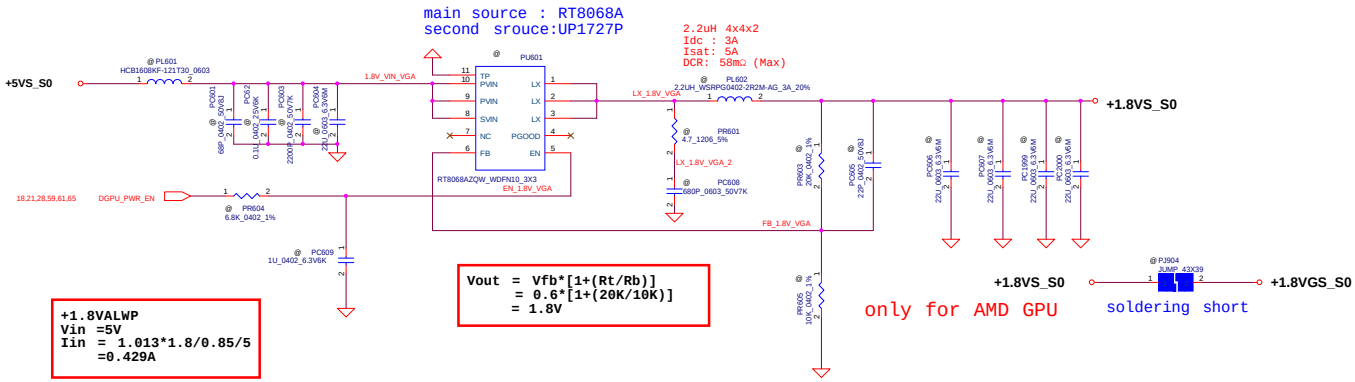
Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(115K/10K)]
= 10V

+10VALWP ⟷ +10V_LCDVDD_S5
Soldering Short

+10VALWP
Imax=0.84A,Ipeak=1.2A ; Fsw=340KHz
Current Limit=4.1A(Min)
in_ripple=0.78A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.12A
LIR=Delta IL/Ipeak=3
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=6.11uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.27uF

Security Classification	Compal Secret Data		
Issued Date	2013/08/15	Deciphered Date	<Deciphered_Date>

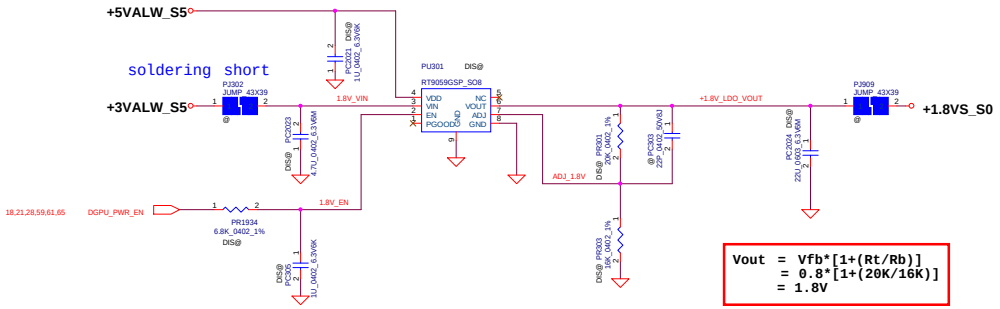
Title	1V1(RT8068)/10V(RT8296)		
Size Custom	Document Number		Rev 0.1
Date: Thursday, November 22, 2018	Sheet 58	of 73	



Vout = Vfb*[1+(Rt/Rb)]
= 0.6*[1+(20K/10K)]
= 1.8V

+1.8VALWP
Vin =5V
Iin = 1.013*1.8/0.85/5
=0.429A

+1.8VALWP
Ipeak=1.013A ;Fsw=1MHz
ILimit=4A
Iin_ripple=0.4A
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=0.745A
LIR=Delta IL/Ipeak=0.372
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=20.81uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.06uF



Vout = Vfb*[1+(Rt/Rb)]
= 0.8*[1+(20K/16K)]
= 1.8V

Security Classification	Compal Secret Data		
Issued Date	2014/12/26	Deciphered Date	2016/12/26

Compal Electronics, Inc.

Title: 1.8V(RT8068/RT9059)

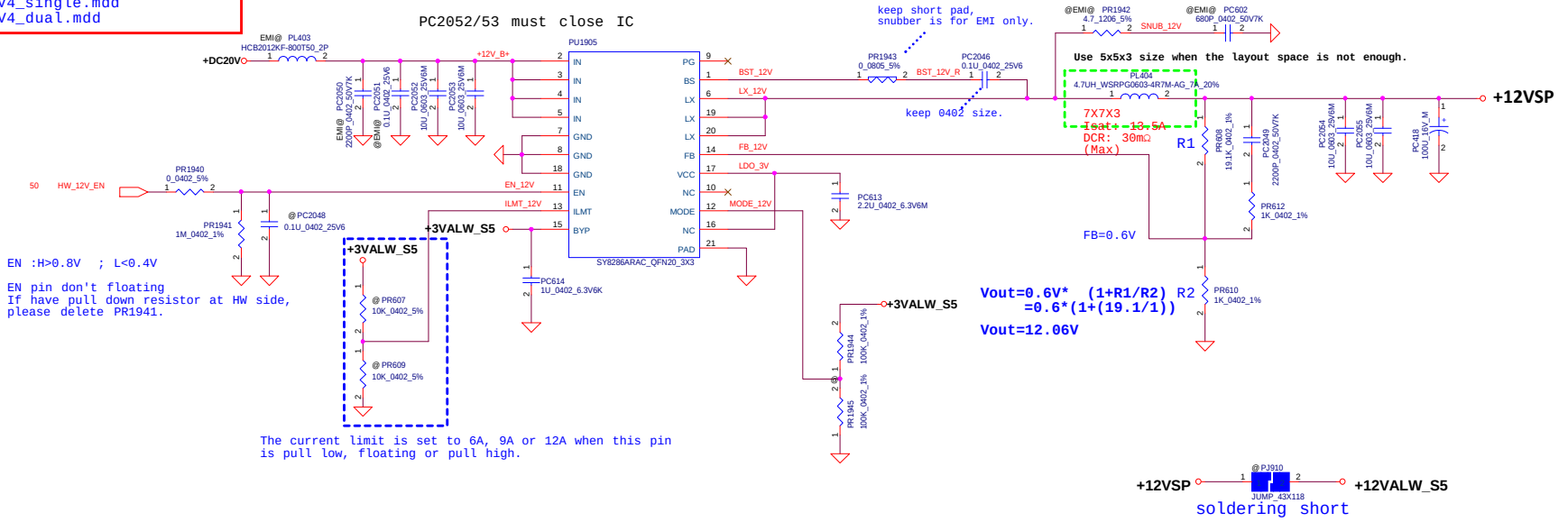
Size | Document Number | Rev 0.1

Date: Thursday, November 22, 2018 | Sheet 59 of 73

Module model information

SY8286_V4_single.mdd
SY8286_V4_dual.mdd

main source : SY8286A
second srouce:JW5069A




```
+12VSP
Imax=2.607,Ipeak=3.724A   ;Fsw=300KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:12.1mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=10~13.5A
Iin_ripple=0.97A
Output Cap. ESR=24mohm
Delta   IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=3.404A
LIR=Delta  IL/Ipeak=0.914
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=15uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.04uF
```

```
Vout  =  Vfb*[1+(Rt/Rb)]
      =  0.8*[1+(2.1K/150)]
      = 12V
```

```
+12VSP
Vin = 20V
Iin  =  12*2.1/0.85/20
     = 2.63A
```

Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

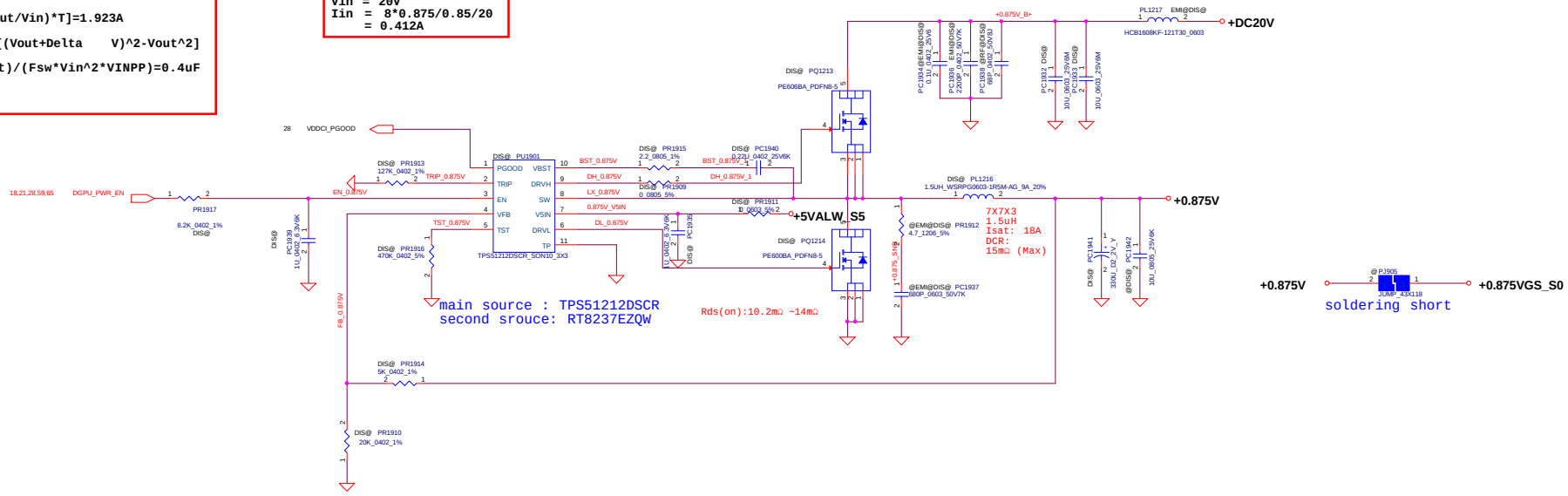
Title: 12V(RT8130B)

Size: C | Document Number | Rev: 0.1

Date: Thursday, November 22, 2018 | Sheet 60 of 73

```
+0.875V
Imax=5.6,Ipeak=8A   ;Fsw=290KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=12~16A
Iin_ripple=1.15A
Output Cap. ESR=17mohm
Delta   IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.923A
LIR=Delta  IL/Ipeak=0.24
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=822.98uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.4uF
```

```
+0.875V
Vin = 20V
Iin  =  8*0.875/0.85/20
     = 0.412A
```




```
Vout  =  Vfb*[1+(Rt/Rb)]
      = 0.7*[1+(5K/20K)]
      = 0.875V
```

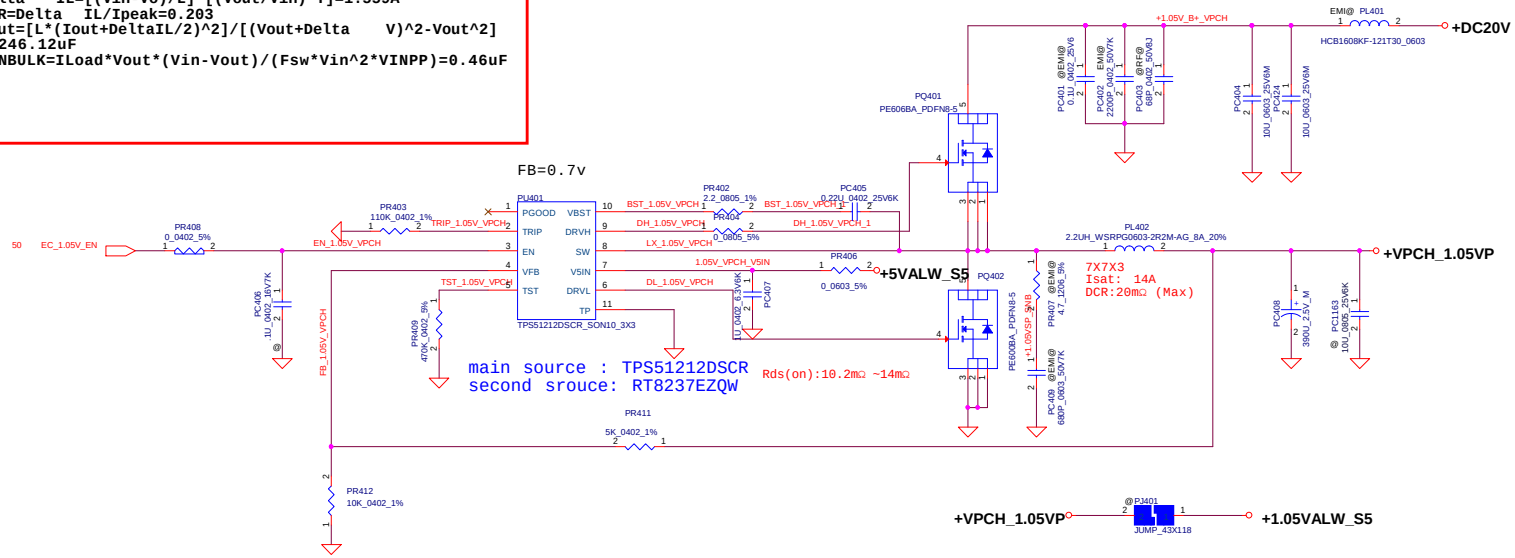
Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.			
Title	0.875V(TPS51212)		
Size: Custom	Document Number		Rev: 0.1
Date: Thursday, November 22, 2018	Sheet 61 of 73		

```
+VPCH_1.05VP
Ipeak=7.696A,Imax=5.387A  ;  Iocp=11.6A~14A
Fsw=290K
Iin_ripple=  1.28A
Output  Cap.  ESR=17mohm
Rds   L/S  --> typ:  12.1mohm  ;  max:  14mohm
Delta    IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=1.559A
LIR=Delta   IL/Ipeak=0.203
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta    V)^2-Vout^2]
=1246.12uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.46uF
```

```
Vout  =  Vfb*[1+(Rt/Rb)]
      =  0.7*[1+(5K/10K)]
      =  1.05V
```

```
+VPCH_1.05VP
Vin  =  20V
Iin  =  1.0*10.24/0.85/20
     =  0.602A
```



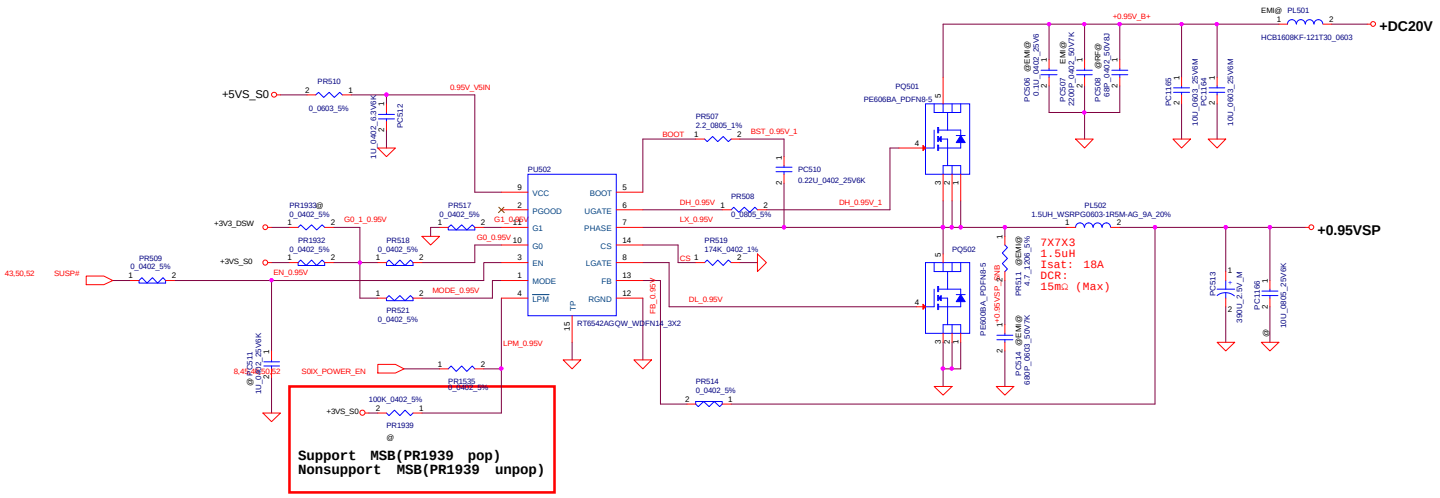
Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: VPCH1.05V(TPS51212)

Size	Document Number	Rev
Custom		0.1

Date: Thursday, November 22, 2018 Sheet 62 of 73



+0.95VSP
Imax=4.48A Ipeak=6.4A ;Fsw=290KHz
Iocp=(Rcs1*Itrip)/Rdson
Rds : L/S --> typ:10.2mohm ; max: 14mohm
Itrip=9~11 uA
Iocp(set)=11.3~13.59A
Iin_ripple=1.24A
Output Cap. ESR=17mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=2.08A
LIR=Delta IL/Ipeak=0.249
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1293.74uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.46uF

+0.95VSP
Vin = 20V
Iin =0.95*8.35/0.85/20
= 0.466A

Vout = Vfb*[1+(Rt/Rb)]
= 0.7*[1+(5K/14.3K)]
= 0.95V

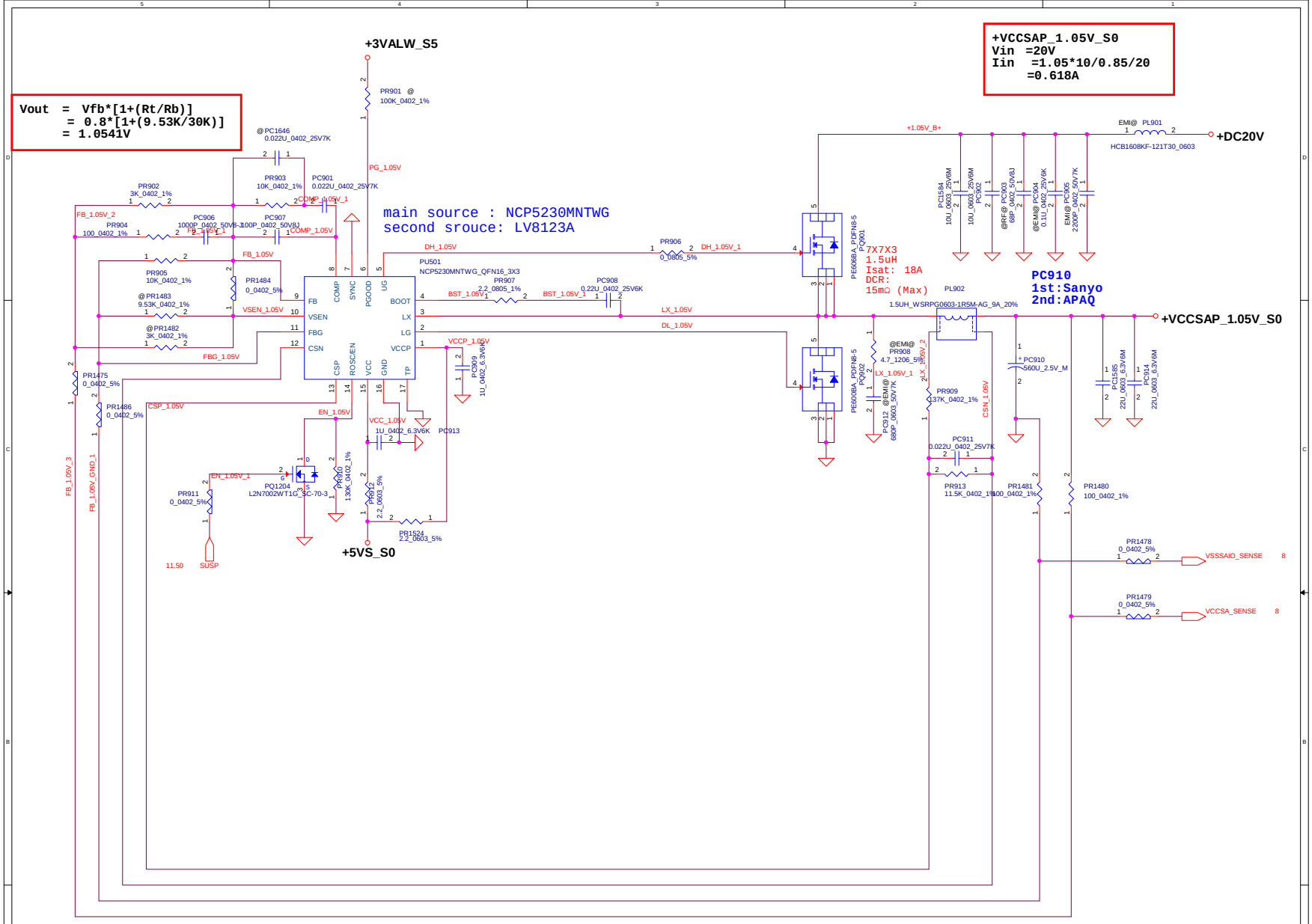
Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: **VCCIO_0.95V(TPS51212)**

Size	Document Number	Rev
Custom		0.1

Date: Thursday, November 22, 2018 Sheet 63 of 73



Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

Compal Electronics, Inc.

Title: VCCSA_1.05VSP(NCP5230M)

Size	Document Number	Rev
Custom		1.0

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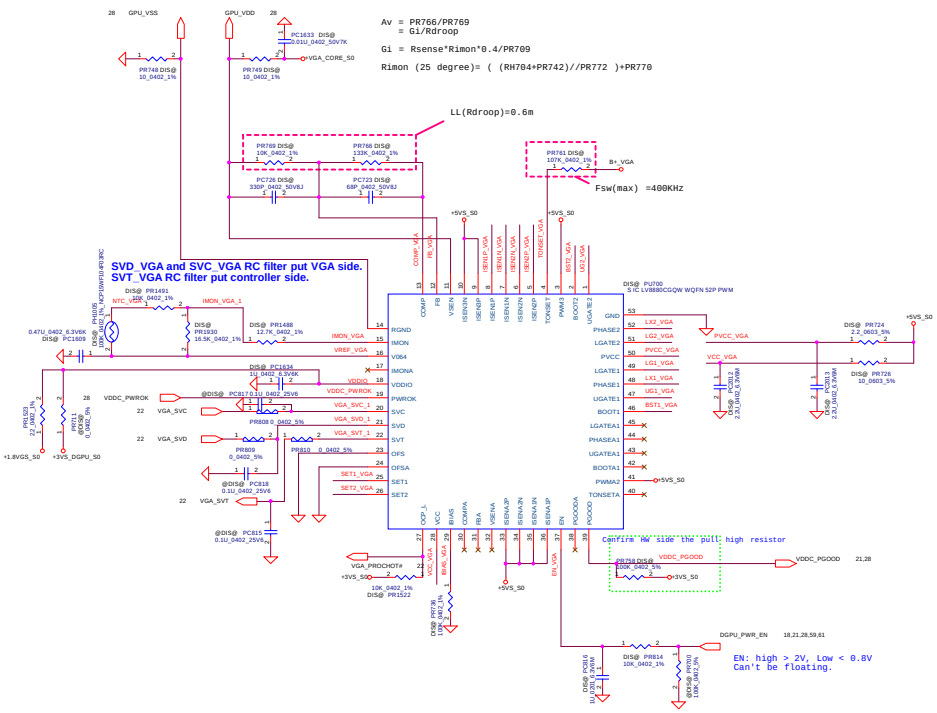
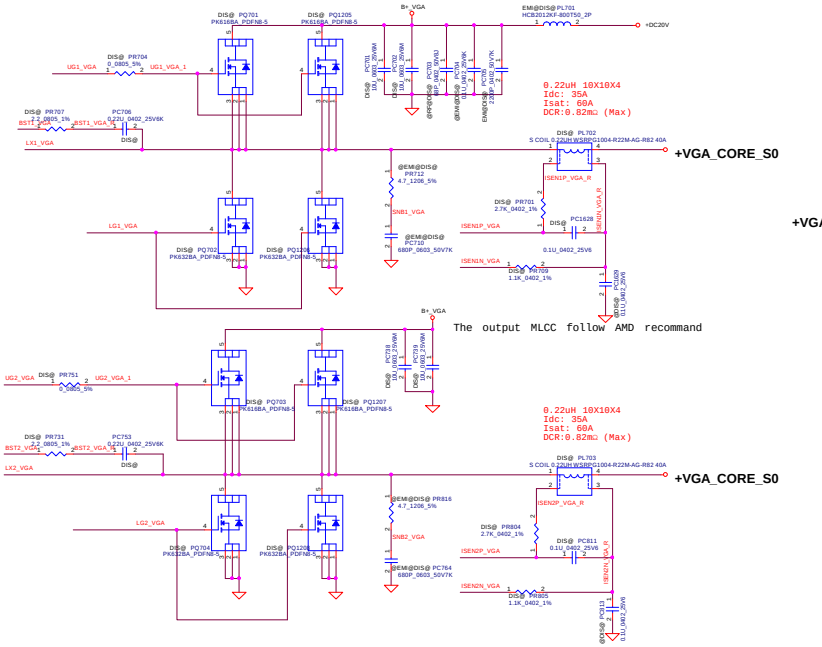
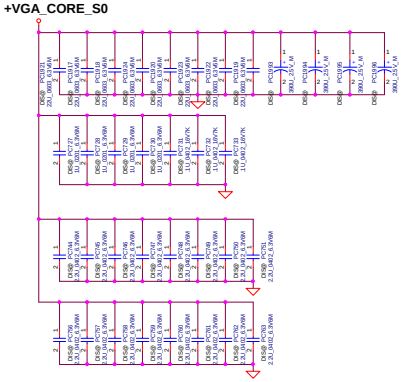


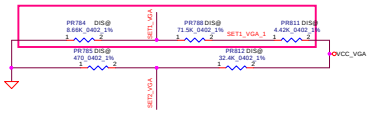




Iocp_spike = (3.19375 - 0.64)*PR789/ (DCR*Rimon)

Iocp_TDC has relation between ocp_spike and Δ VSET1

Δ VSET1 = VCC_VGA*(PR788//PR784)



+VGA_CORE [AMD R17M-G1-50]
TDC=38A ; Ipeak=70A ; Iocp>=90A
Fsw=400K
Inductor DCR=1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=8.727A
LIR=Delta IL/Ipeak=0.388
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2]
=1356.75uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.76uF

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Issued Date	2013/08/29	Deciphered Date	2013/08/29
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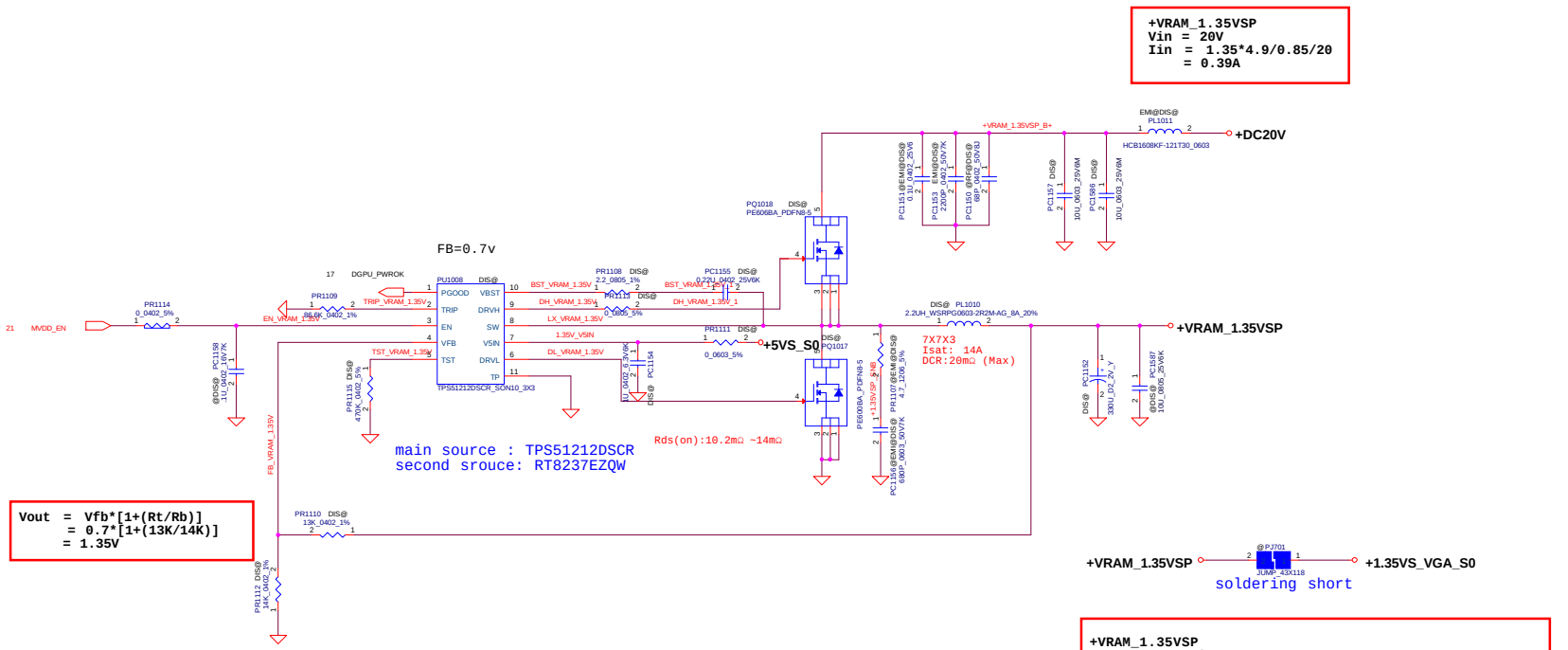
			Size: Document Number: Rev: 0.1
			Date: Thursday, November 22, 2018 Sheet 65 of 73



Security Classification	Compal Secret Data		
Issued Date	2013/08/29	Deciphered Date	2013/08/29

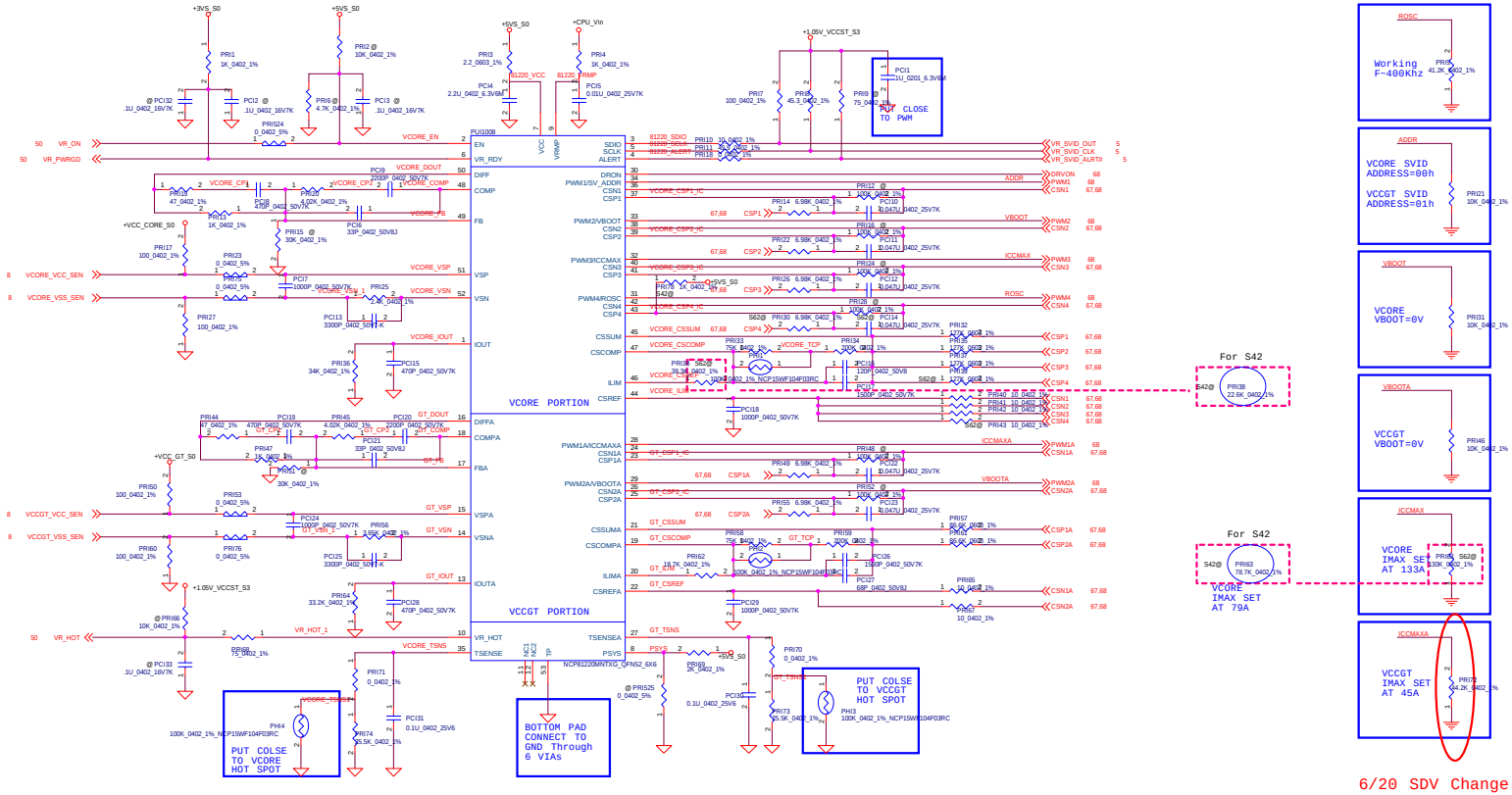
Compal Electronics, Inc.			
Title	VRAM_1.35V(TPS51212)		
Size Custom	Document Number		Rev 0.1
Date: Thursday, November 22, 2018	Sheet 66 of 73		

Intel Coffeelake IMVP8 POWER CFL - S-LINE 62 35W 4+2 PHASE

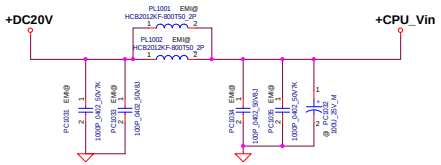
S-Line 62 65W CPU power spec
Vcore ICCMAX=133A, TDC=91A
VccGT ICCMAX=45A, TDC=30A

Intel Coffeelake IMVP8 POWER CFL - S-LINE 42 35W 3+2 PHASE

S-Line 42 65W CPU power spec
Vcore ICCMAX=79A, TDC=61A
VccGT ICCMAX=45A, TDC=30A



6/20 SDV Change



CFL - S-LINE 62 65W

+CPU_CORE
TDC=91A,Ipeak=133A Fsw=350K,OCP=180A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.255A
LIR=Delta IL/Ipeak=0.394
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =811.08
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.03uF

+GFX_CORE
TDC=30A,Ipeak=45A Fsw=350K,OCP=60A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=6.267A
LIR=Delta IL/Ipeak=0.358
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =577.19uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

CFL - S-LINE 42 65W

+CPU_CORE
TDC=61A,Ipeak=79A Fsw=350K,OCP=107A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=10.255A
LIR=Delta IL/Ipeak=0.394
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =811.08
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=1.03uF

+GFX_CORE
TDC=30A,Ipeak=45A Fsw=350K,OCP=60A
Inductor DCR=1.1mohm
Output Cap. ESR=10mohm
Rds H/S --> typ: 4.8mohm ; max: 7mohm
L/S --> typ: 2.1mohm ; max: 3.3mohm
Delta IL=[(Vin-Vo)/L]*[(Vout/Vin)*T]=6.267A
LIR=Delta IL/Ipeak=0.358
Cout=[L*(Iout+DeltaIL/2)^2]/[(Vout+Delta V)^2-Vout^2] =577.19uF
CINBULK=ILoad*Vout*(Vin-Vout)/(Fsw*Vin^2*VINPP)=0.69uF

Security Classification	Compal Secret Data	
Issued Date	2019/01/25	Deciphered Date 2009/04/28

Compal Electronics, Inc.

Title	CPU_CORE (NCP81220M)		
Size Custom	Document Number		Rev 0.1
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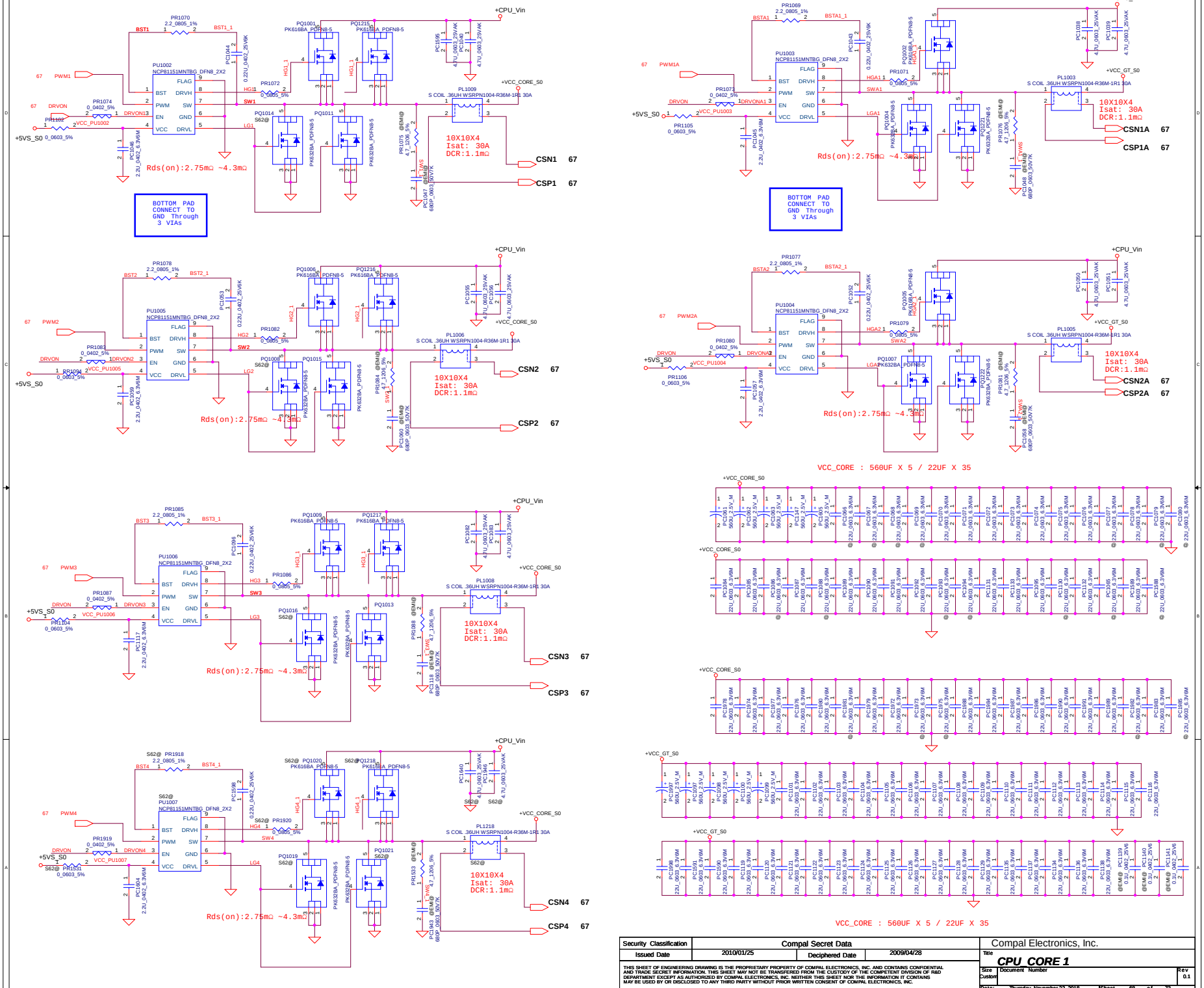
+CPU_Vin
PR1070 2.2_0805_1%
BST1
PU1002 NCP81151MNTBG_DFN8_2X2
FLAG
BST DRVH
PWM SW
EN GND
VCC DRVL
PWM1
DRVON
PR1074 0_0402_5%
PR1102
VCC_PU1002
+5VS_S0 0_0603_5%
PC1046 2.2U_0402_6.3V6M
PC1044 0.22U_0402_25V6K
PR1072 0_0805_5%
HG1
SW1
LG1
PQ1001 PK616BA_PDFN8-5
PQ1215 PK616BA_PDFN8-5
PC1096 4.7U_0603_25VAK
PC1097 4.7U_0603_25VAK
+VCC_CORE_S0
PL1009 S COIL_36UH WSRPN1004-R36M-1R1 30A
PQ1014 S62@
PQ1011
PK6328A_PDFN8-5
PR1075 @EM@ 4.7_1206_5%
PC1047 @EM@ 680P_0603_50V7K
SW1A
10X10X4
Isat: 30A
DCR:1.1mΩ
CSN1 67
CSP1 67
Rds(on):2.75mΩ ~4.3mΩ
BOTTOM PAD CONNECT TO GND Through 3 VIAs
PR1069 2.2_0805_1%
BSTA1
PU1003 NCP81151MNTBG_DFN8_2X2
PWM1A
DRVONA
PR1073 0_0402_5%
VCC_PU1003
PR1105 0_0603_5%
PC1045 2.2U_0402_6.3V6M
PC1043 0.22U_0402_25V6K
PR1071 0_0805_5%
HGA1
SWA1
LGA1
PQ1002 PK616BA_PDFN8-5
PQ1221 PK6328A_PDFN8-5
PR1076 @EM@ 4.7_1206_5%
PC1048 @EM@ 680P_0603_50V7K
SW1AS
PC1038 4.7U_0603_25VAK
PC1039 4.7U_0603_25VAK
+VCC_GT_S0
PL1003 S COIL_36UH WSRPN1004-R36M-1R1 30A
10X10X4
Isat: 30A
DCR:1.1mΩ
CSN1A 67
CSP1A 67
Rds(on):2.75mΩ ~4.3mΩ
BOTTOM PAD CONNECT TO GND Through 3 VIAs
PR1078 2.2_0805_1%
BST2
PU1005 NCP81151MNTBG_DFN8_2X2
PWM2
DRVON
PR1081 0_0402_5%
RR1094
VCC_PU1005
+5VS_S0
PC1099 2.2U_0402_6.3V6M
PC1063 0.22U_0402_25V6K
PR1082 0_0805_5%
HG2
SW2
LG2
PQ1006 PK616BA_PDFN8-5
PQ1216 PK616BA_PDFN8-5
PC1095 4.7U_0603_25VAK
PC1098 4.7U_0603_25VAK
+VCC_CORE_S0
PL1006 S COIL_36UH WSRPN1004-R36M-1R1 30A
PQ1008 S62@
PQ1015
PK6328A_PDFN8-5
PR1084 @EM@ 4.7_1206_5%
PC1060 @EM@ 680P_0603_50V7K
SW2A
10X10X4
Isat: 30A
DCR:1.1mΩ
CSN2 67
CSP2 67
Rds(on):2.75mΩ ~4.3mΩ
PR1077 2.2_0805_1%
BSTA2
PU1004 NCP81151MNTBG_DFN8_2X2
PWM2A
DRVONA
PR1080 0_0402_5%
VCC_PU1004
PR1106 0_0603_5%
PC1057 2.2U_0402_6.3V6M
PC1052 0.22U_0402_25V6K
PR1079 0_0805_5%
HGA2
SWA2
LGA2
PQ1005 PK616BA_PDFN8-5
PQ1007 PK632BA_PDFN8-5
PQ1222 PK6328A_PDFN8-5
PR1081 @EM@ 4.7_1206_5%
PC1058 @EM@ 680P_0603_50V7K
SW2AS
PC1050 4.7U_0603_25VAK
PC1051 4.7U_0603_25VAK
+VCC_GT_S0
PL1005 S COIL_36UH WSRPN1004-R36M-1R1 30A
10X10X4
Isat: 30A
DCR:1.1mΩ
CSN2A 67
CSP2A 67
Rds(on):2.75mΩ ~4.3mΩ
VCC_CORE : 560UF X 5 / 22UF X 35
PR1085 2.2_0805_1%
BST3
PU1006 NCP81151MNTBG_DFN8_2X2
PWM3
DRVON
PR1087 0_0402_5%
VCC_PU1006
+5VS_S0
PR1104 0_0603_5%
PC1117 2.2U_0402_6.3V6M
PC1096 0.22U_0402_25V6K
PR1086 0_0805_5%
HG3
SW3
LG3
PQ1009 PK616BA_PDFN8-5
PQ1217 PK616BA_PDFN8-5
PC1082 4.7U_0603_25VAK
PC1083 4.7U_0603_25VAK
+VCC_CORE_S0
PL1008 S COIL_36UH WSRPN1004-R36M-1R1 30A
PQ1016 S62@
PQ1013
PK6328A_PDFN8-5
PR1088 @EM@ 4.7_1206_5%
PC1118 @EM@ 680P_0603_50V7K
SW3A
10X10X4
Isat: 30A
DCR:1.1mΩ
CSN3 67
CSP3 67
Rds(on):2.75mΩ ~4.3mΩ
PR1918 2.2_0805_1%
BST4
PU1007 NCP81151MNTBG_DFN8_2X2
PWM4
DRVON
PR1919 0_0402_5%
VCC_PU1007
+5VS_S0
PR1151 0_0603_5%
PC1104 2.2U_0402_6.3V6M
PC1598 0.22U_0402_25V6K
PR1920
HG4
SW4
LG4
PQ1020 PK616BA_PDFN8-5
PQ1218 PK616BA_PDFN8-5
PC1640 4.7U_0603_25VAK
PC1946 4.7U_0603_25VAK
PL1218 S COIL_36UH WSRPN1004-R36M-1R1 30A
PQ1019 S62@
PQ1021 S62@
PR1933 @EM@ 4.7_1206_5%
PC1943 @EM@ 680P_0603_50V7K
SW4A
10X10X4
Isat: 30A
DCR:1.1mΩ
CSN4 67
CSP4 67
Rds(on):2.75mΩ ~4.3mΩ
VCC_CORE : 560UF X 5 / 22UF X 35
Security Classification
Compal Secret Data
Issued Date
2010/01/25
Deciphered Date
2009/04/28
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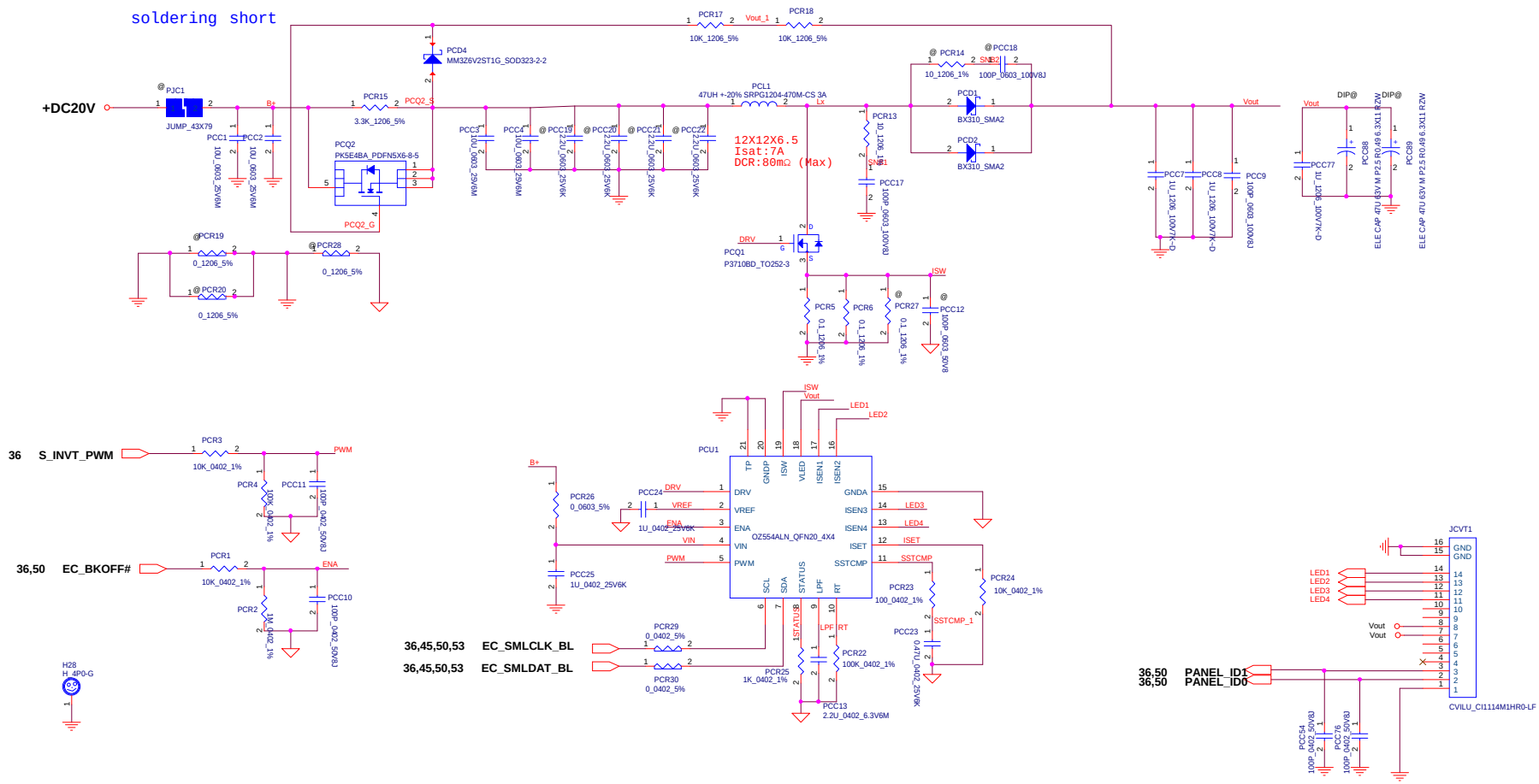
Title
CPU_CORE 1
Size Custom
Document Number
Rev 0.1
Date: Thursday, November 22, 2018
Sheet 68 of 73



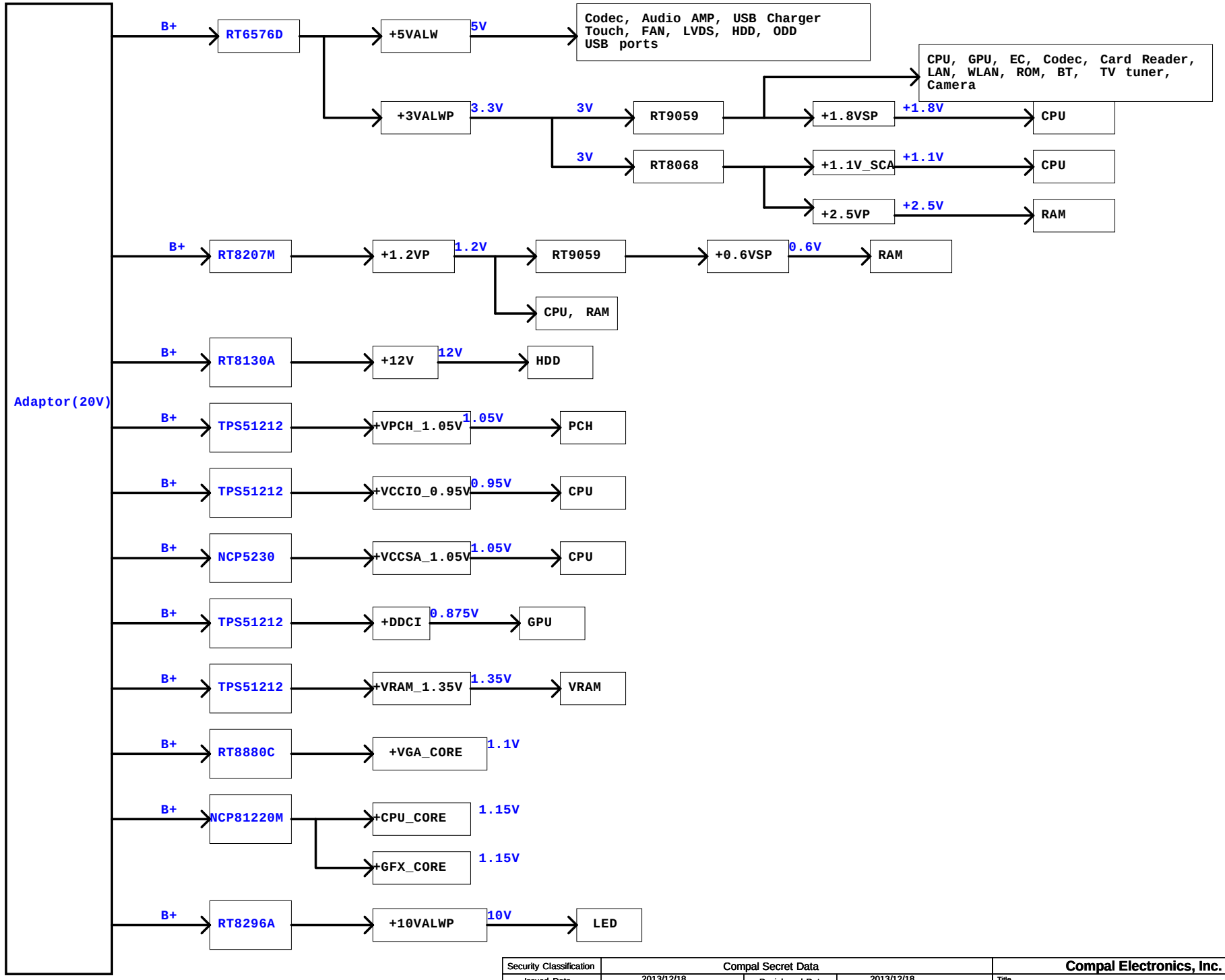
Security Classification	Compal Secret Data		
Issued Date	2015/11/30	Deciphered Date	2015/11/30

Compal Electronics, Inc.

Title: CONVERTER/B

Size	Document Number	Rev
C	C7 Converter/B	0.2

Date: | Sheet 69 of 73



Security Classification	Compal Secret Data		
Issued Date	2013/12/18	Deciphered Date	2013/12/18

Compal Electronics, Inc.

Title: ***Power Rail***

Size	Document Number	Rev
Custom		0.1

Date: Thursday, November 22, 2018 Sheet 70 of 73

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	9/15	P.57	EN Pin CPU_C10_GATE# change to C10_GATE#	HW request
2	9/18	P.61	PSYS Pin Add PRI525 to GND	
3	9/19	P.62	PL1218 Bom structure : S62@	
4				
5				

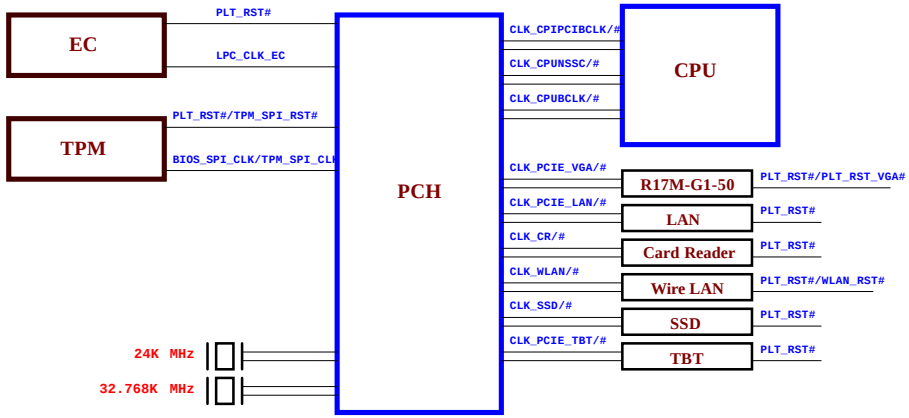
Compal Electronics, Inc.

Title: PWR PIR

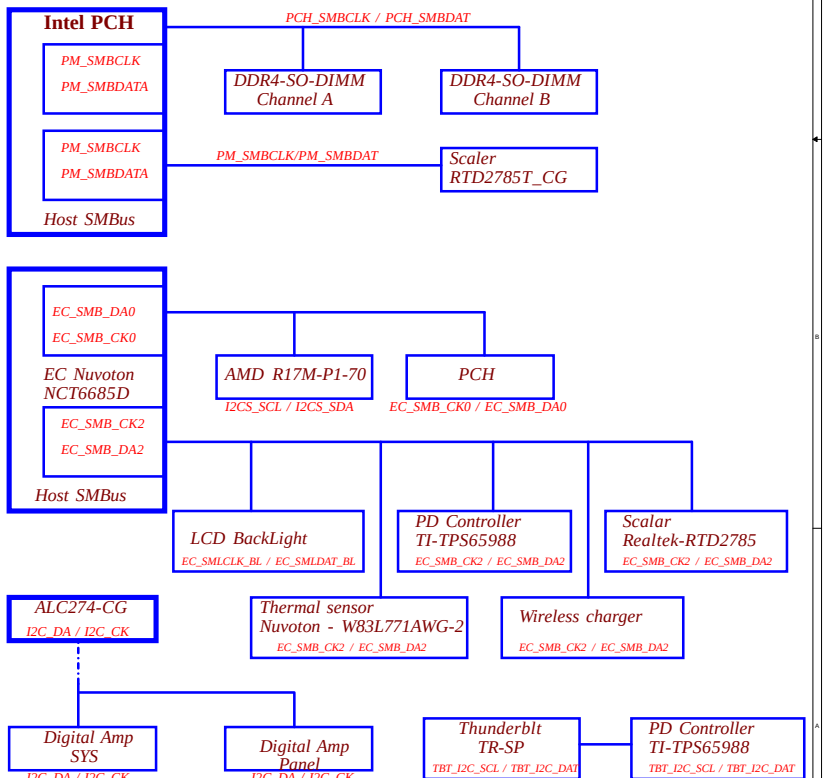
Size	Document Number	Rev
Custom		0.5

Date: Thursday, November 29, 2012 Sheet 71 of 73

System clock and Reset map



SMBUS Block Diagram



Group	Pin	ULT SPEC	Power well	Default Internal Pull H / L	Strapping Usage	Default	SCI / SMI / NMI	BBA10	BBA10 Default Internal Pull H / L
GPD	BD13	GPD0 / BATLOW#	DSW			Native		PM_BATLOW# PU 8.2K to +3VALW_DSW_S5	
	BB15	GPD1 / ACPRESENT	DSW			Native		AC_PRESENT_R PU 10K to +3VALW_DSW_S5(@)	
	BD11	GPD2 / LAN_WAKE#	DSW			Native		LAN_WAKE# PU 10K to +3VALW_DSW_S5	
	AT13	GPD3 / PWRBTN#	DSW			Native		PBTN_OUT#_R PU 100K to +3VALW_DSW_S5	
	AW15	GPD4 / SLP_S3#	DSW			Native		PM_SLP_S3#	
	BD15	GPD5 / SLP_S4#	DSW			Native		PM_SLP_S4#	
	BC15	GPD6 / SLP_A#	DSW			Native		PM_SLP_A# Testpoint	
	BD14	GPD7 / RSVD	DSW			N/A			
	AN15	GPD8 / SUSCLK	DSW			Native		SUSCLK PD 1K(@)	
	AV13	GPD9 / SLP_WLAN#	DSW			Native		PM_SLP_LAN# Testpoint	
	BA13	GPD10 / SLP_S5#	DSW			Native		PM_SLP_S5# Testpoint	
	AR15	GPD11 / LANPHYPC	DSW			Native		LANPHYPC Testpoint	
GPE_A	AT17	GPP_A0 / RCIN#	Primary(3.3V/1.8V)			Native	SCI	KB_RST# PU 10K to +3VS_S0	
	AT22	GPP_A1 / LAD0 / ESPI_IO0	Primary(3.3V/1.8V)			Native	SCI	LPC_AD0	
	AV22	GPP_A2 / LAD1 / ESPI_IO1	Primary(3.3V/1.8V)			Native	SCI	LPC_AD1	
	AT19	GPP_A3 / LAD2 / ESPI_IO2	Primary(3.3V/1.8V)			Native	SCI	LPC_AD2	
	BD16	GPP_A4 / LAD3 / ESPI_IO3	Primary(3.3V/1.8V)			Native	SCI	LPC_AD3	
	BE16	GPP_A5 / LFRAME# / ESPI_CS#	Primary(3.3V/1.8V)			Native	SCI	LPC_FRAME#	
	BA17	GPP_A6/SERIRQ/ESPI_CS1#	Primary(3.3V/1.8V)			Native	SCI	SERIRQ PU 10K to +3VS_S0	
	AW17	GPP_A7/PIRQA#/ESPI_ALERT0#	Primary(3.3V/1.8V)			Native	SCI	LPC_PIRQA# PU 10K to +3VALW_S5	
	AW22	GPP_A8 / CLKRUN#	Primary(3.3V/1.8V)			Native	SCI	TPM_CLKRUN# PU 8.2K to +3VS_TPM_S0	
	BC17	GPP_A9 / CLKOUT_LPC0 / ESPI_CLK	Primary(3.3V/1.8V)			Native	SCI	LPC_CLKOUT0	
	AV19	GPP_A10 / CLKOUT_LPC1	Primary(3.3V/1.8V)			Native	SCI	LPC_CLKOUT1	
	BD17	GPP_A11 /PME#	Primary(3.3V/1.8V)			Native	SCI	PCH_PME# PU 100K to +3V_1.8V_PGPPA_S5	
	BB17	GPP_A12/BM_BUSY#/ISH_GP6/SX_EXIT_HOLDOFF#	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPIO#12 Testpoint	
	BD19	GPP_A13 / SUSWARN# / SUSPWRDNACK	Primary(3.3V/1.8V)			Native	SCI	SUSWARN#_R	
	BC18	GPP_A14/SUS_STAT#/ESPI_RESET#	Primary(3.3V/1.8V)			Native	SCI	SUS_STAT#	
	BB19	GPP_A15 / SUSACK#	Primary(3.3V/1.8V)			Native	SCI	SUSACK#	
	AR17	GPP_A16/CLKOUT_48	Primary(3.3V/1.8V)			GPI	SCI	GPP_A16_CLKOUT Testpoint	
	BC19	GPP_A17 / ISH_GP7	Primary(3.3V/1.8V)			GPI	SCI		
	BB22	GPP_A18 / ISH_GP0	Primary(3.3V/1.8V)			GPI	SCI		
	BD21	GPP_A19 / ISH_GP1	Primary(3.3V/1.8V)			GPI	SCI		
	BD22	GPP_A20 / ISH_GP2	Primary(3.3V/1.8V)			GPI	SCI		
	BE21	GPP_A21 / ISH_GP3	Primary(3.3V/1.8V)			GPI	SCI		
	BD18	GPP_A22 / ISH_GP4	Primary(3.3V/1.8V)			GPI	SCI		
	BC22	GPP_A23 / ISH_GP5	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPIO#23 Testpoint	
GPP_B	AR27	GPP_B0	Primary(3.3V/1.8V)			GPO	SCI		
	AL27	GPP_B1	Primary(3.3V/1.8V)			GPO	SCI		
	BD20	GPP_B2 / VRALERT#	Primary(3.3V/1.8V)			GPI	SCI	VRALERT# PU 10K to +3VALW_DSW_S5(@)	Enable Pull H
	BC23	GPP_B3 / CPU_GP2	Primary(3.3V/1.8V)			GPI	SCI		
	BD24	GPP_B4 / CPU_GP3	Primary(3.3V/1.8V)			GPI	SCI		
	BC24	GPP_B5 / SRCCLKREQ0#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_VGA# PU 10K to +3VS+S0	Enable Pull H
	AW24	GPP_B6 / SRCCLKREQ1#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_LAN# PU 10K to +3VS+S0	Enable Pull H
	AT24	GPP_B7 / SRCCLKREQ2#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_CR# PU 10K to +3VS+S0	Enable Pull H
	BD25	GPP_B8 / SRCCLKREQ3#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_WLAN# PU 10K to +3VS+S0	Enable Pull H
	BB24	GPP_B9 / SRCCLKREQ4#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE4# PU 10K to +3VS+S0	Enable Pull H
	BE25	GPP_B10 / SRCCLKREQ5#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#5 PU 10K to +3VS+S0	
	AN24	GPP_B11	Primary(3.3V/1.8V)			GPO	SCI	MPHY_DAT_PWR PU 200K to +3VALW_S5	
	BC26	GPP_B12 / SLP_S0#	Primary(3.3V/1.8V)			Native	SCI	PM_SLP_S0#	
	BB27	GPP_B13 / PLTRST#	Primary(3.3V/1.8V)			Native	SCI	PCH_PLT_RST#	
	BD26	GPP_B14 / SPKR	Primary(3.3V/1.8V)	L(20K)	Yes	GPO	Yes	PCH_SPKR Strap for Top Swap override H=Enable, L=Disable(Default) PU 100K to +3VS_S0(@)	L(20K)
	AR24	GPP_B15 / GSPI0_CS#	Primary(3.3V/1.8V)			GPI	SCI		
	AW27	GPP_B16 / GSPI0_CLK	Primary(3.3V/1.8V)			GPI	SCI	USB_UART_SEL PU 100K to +3VALW_S5	
	BD27	GPP_B17 / GSPI0_MISO	Primary(3.3V/1.8V)			GPI	SCI		
	BD28	GPP_B18 / GSPI0_MOSI	Primary(3.3V/1.8V)	L(20K)	Yes	GPO	SCI	GSPI0_MOSI Strap for No Reboot H=Disable(Default), L=Enable PU 4.7K to +3VS_S0(@)	L(20K)
	BC27	GPP_B19 / GSPI1_CS#	Primary(3.3V/1.8V)			GPI	SCI	WLAN_PWREN PD 100K(@)	
	AV29	GPP_B20 / GSPI1_CLK	Primary(3.3V/1.8V)			GPI	Yes	NGAN_IMG_DFU	
	AR29	GPP_B21 / GSPI1_MISO	Primary(3.3V/1.8V)			GPI	SCI	GPU_GPIO#21 PU 10K to +3VS	
	AT29	GPP_B22 / GSPI1_MOSI	Primary(3.3V/1.8V)	L(20K)	Yes	GPO	SCI	GSPI1_MOSI Strap for BIOS Boot H=PCI, L=SPI(Default) PU 10K to +3VS_S0 (@)	L(20K)
	AT27	GPP_B23 / SML1ALERT# / PCHHOT#	Primary(3.3V/1.8V)	L(20K)		GPO	Yes	SML1ALERT1# Testpoint	L(20K)
	AW44	GPP_C0 / SMBCLK	Primary(3.3V/1.8V)			Native	SCI	PM_SMBCLK PU 2.2K to +3VALW_S5	
	BB43	GPP_C1 / SMBDATA	Primary(3.3V/1.8V)			Native	SCI	PM_SMBDATA PU 2.2K to +3VALW_S5	
	BB41	GPP_C2 / SMBALERT#	Primary(3.3V/1.8V)	hpd	Yes	GPO	SCI	SMLALERT# Strap for TLS Confidentiality H=Enable, L=Disable(Default) PU 4.7K to +3VALW_S5	L(20K)
	AY44	GPP_C3 / SML0CLK	Primary(3.3V/1.8V)			Native	SCI	PCH_SML0CLK0 PU 499 to +3VS_S0	
	BB39	GPP_C4 / SML0DATA	Primary(3.3V/1.8V)			Native	SCI	PCH_SML0DATA0 PU 499 to +3VS_S0	
	BA40	GPP_C5 / SML0ALERT#	Primary(3.3V/1.8V)	L(20K)	Yes	GPO	SCI	SML0ALERT0# Strap for eSPI/LPC mode selection H=eSPI(Default), L=LPC PU 4.7K to +3VALW_S5(@)	L(20K)
	AW42	GPP_C6 / SML1CLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML1CLK1 PU 1K to +3VS_S0	
	AW45	GPP_C7 / SML1DATA	Primary(3.3V/1.8V)			GPO	SCI	PCH_SML0DATA1 PU 1K to +3VS_S0	
	BA41	GPP_C8 / UART0_RXD	Primary(3.3V/1.8V)			GPI	SCI		
GPP_C	AV43	GPP_C10 / UART0_RTS#	Primary(3.3V/1.8V)			GPI	SCI		
	AU44	GPP_C11 / UART0_CTS#	Primary(3.3V/1.8V)			GPI	SCI	EC_ON +3VS_WLAN_S0	
	AU43	GPP_C12 / UART1_RXD / ISH_UART1_RXD	Primary(3.3V/1.8V)			GPI	SCI	GSPI1_PWR_EN	
	AT43	GPP_C13 / UART1_TXD / ISH_UART1_TXD	Primary(3.3V/1.8V)			GPI	SCI	GSPI1_RESET#	
	AT44	GPP_C14 / UART1_RTS# / ISH_UART1_RTS#	Primary(3.3V/1.8V)			GPI	SCI		
	AU41	GPP_C15 / UART1_CTS# / ISH_UART1_CTS#	Primary(3.3V/1.8V)			GPI	SCI		Enable Pull H
	AT42	GPP_C16 / I2C0_SDA	Primary(3.3V/1.8V)			GPI	SCI		
	AR38	GPP_C17 / I2C0_SCL	Primary(3.3V/1.8V)			GPI	SCI		
	AR44	GPP_C18 / I2C1_SDA	Primary(3.3V/1.8V)			GPI	SCI		
	AR41	GPP_C19 / I2C1_SCL	Primary(3.3V/1.8V)			GPI	SCI		
	AR45	GPP_C20 / UART2_RXD	Primary(3.3V/1.8V)			GPI	SCI	UART_2_CRXD_DTXD PU 49.9K to +3VS_S0	
GPP_D	AR39	GPP_C21 / UART2_TXD	Primary(3.3V/1.8V)			GPI	SCI	UART_2_CTXD_DRXD PU 49.9K to +3VS_S0	
	AN44	GPP_C22 / UART2_RTS#	Primary(3.3V/1.8V)			GPI	Yes	UART_2_CRTS_DCTS PU 49.9K to +3VS(@)	
	AN43	GPP_C23 / UART2_CTS#	Primary(3.3V/1.8V)			GPI	Yes		
	AL39	GPP_D0 / SPI1_CS#	Primary(3.3V/1.8V)			GPI	Yes		
	AN39	GPP_D1 / SPI1_CLK	Primary(3.3V/1.8V)			GPI	Yes		
	AN38	GPP_D2 / SPI1_MISO	Primary(3.3V/1.8V)			GPI	Yes		
	AN41	GPP_D3 / SPI1_MOSI	Primary(3.3V/1.8V)			GPI	Yes		
	AM44	GPP_D4/ISH_I2C2_SDA/ISH_I2C1_SDA	Primary(3.3V/1.8V)			GPI	Yes		
	AJ33	GPP_D5/SD2_SFRM	Primary(3.3V/1.8V)			GPI	SCI		
	AM43	GPP_D6/SD2_TXD	Primary(3.3V/1.8V)			GPI	SCI		
	AN42	GPP_D7/SD2_RXD	Primary(3.3V/1.8V)			GPI	SCI		
	AL42	GPP_D8/SD2_SCLK	Primary(3.3V/1.8V)			GPI	SCI		
	AL44	GPP_D9	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPIO#35 Testpoint	
	AL36	GPP_D10	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPIO#10 Testpoint	
	AL35	GPP_D11	Primary(3.3V/1.8V)			GPI	SCI	GPU_GPIO#11 Testpoint	
	AJ39	GPP_D12	Primary(3.3V/1.8V)			GPI	SCI	GPU_GPIO#12 Testpoint	
	AE45	GPP_D13/ISH_UART0_RXD/SML0BDAT	Primary(3.3V/1.8V)			GPI	SCI	GPU_GPIO#13 Testpoint	
	AK44	GPP_D14/ISH_UART0_TXD/SML0BCLK	Primary(3.3V/1.8V)			GPI	SCI	GPU_GPIO#14 Testpoint	
	AL43	GPP_D15 / ISH_UART0_RTS#	Primary(3.3V/1.8V)			GPI	SCI	GPU_GPIO#15 Testpoint	
	AJ43	GPP_D16 / ISH_UART0_CTS# / SML0BALERT#	Primary(3.3V/1.8V)			GPI	SCI	GPU_GPIO#16 Testpoint	
	AJ42	GPP_D17 / DMIC_CLK1	Primary(3.3V/1.8V)			GPI	SCI	PCH_DMICCLK1 Testpoint	
	AJ38	GPP_D18 / DMIC_DATA1	Primary(3.3V/1.8V)			GPI	SCI	PCH_DMICDAT1 Testpoint	
	AJ35	GPP_D19 / DMIC_CLK0	Primary(3.3V/1.8V)			GPI	SCI	PCH_DMICCLK0 Testpoint	
	AH44	GPP_D20 / DMIC_DATA0	Primary(3.3V/1.8V)			GPI	SCI	PCH_DMICDAT0 Testpoint	
	AG44	GPP_D21 / SPI1_IO2	Primary(3.3V/1.8V)			GPI	SCI		
	AH43	GPP_D22 / SPI1_IO3	Primary(3.3V/1.8V)			GPI	SCI		
	AJ44	GPP_D23/ISH_I2C2_SCL/ISH_UART0_CTS#	Primary(3.3V/1.8V)			GPI	SCI		
GPP_E	AG36	GPP_E0 / SATAXPCIE0 / SATAGP0	Primary(3.3V/1.8V)			Native	Yes	SATA_GP0 PU 10K to +3VS_S0	
	AG35	GPP_E1 / SATAXPCIE1 / SATAGP1	Primary(3.3V/1.8V)			Native	Yes	SATA_GP1 PU 10K to +3VS_S0	
	AG39	GPP_E2 / SATAXPCIE2 / SATAGP2	Primary(3.3V/1.8V)			Native	Yes	SATA_GP2 PU 10K to +3VS_S0	
	AF41	GPP_E3 / CPU_GP0	Primary(3.3V/1.8V)			GPI	Yes	DGPU_PWROK PU 10K to +3VS_S0	
	AG43	GPP_E4 / DEVSLP0	Primary(3.3V/1.8V)			GPI	Yes		
	AG43	GPP_E5 / DEVSLP1	Primary(3.3V/1.8V)			GPI	Yes		
	AE45	GPP_E6 / DEVSLP2	Primary(3.3V/1.8V)			GPI	Yes		
	AE44	GPP_E7 / CPU_GP1	Primary(3.3V/1.8V)			GPI	Yes		
	AD44	GPP_E8 / SATALED#	Primary(3.3V/1.8V)			GPI	Yes	SATA_LED# PU 10K to +3VS_S0	
	AD43	GPP_E9 / USB2_OC0#	Primary(3.3V/1.8V)	L(20K)		GPI	SCI	USB_OC0# PU 10K to +3VALW_S5	L(20K)
	AD42	GPP_E10 / USB2_OC1#	Primary(3.3V/1.8V)	L(20K)		GPI	SCI	USB_OC1# PU 10K to +3VALW_S5	L(20K)
	AD39	GPP_E11 / USB2_OC2#	Primary(3.3V/1.8V)	L(20K)		GPI	SCI	USB_OC2# PU 10K to +3VALW_S5	L(20K)
GPP_F	AC46	GPP_F12 / USB2_OC3#	Primary(3.3V/1.8V)	L(20K)		GPI	SCI	USB_OC3# PU 10K to +3VALW_S5	L(20K)
	AD35	GPP_F0/SATAXPCIE3/SATAGP3	Primary(3.3V/1.8V)			Native	SCI	SATA_GP3 PU 10K to +3VS_S0	
	AD31	GPP_F1/SATAXPCIE4/SATAGP4	Primary(3.3V/1.8V)			Native	SCI	SATA_GP4 Testpoint	
	AD38	GPP_F2/SATAXPCIE5/SATAGP5	Primary(3.3V/1.8V)			Native	SCI	SATA_GP5 Testpoint	
	AC43	GPP_F3/SATAXPCIE6/SATAGP6	Primary(3.3V/1.8V)			Native	SCI	SATA_GP6 Testpoint	
	AB44	GPP_F4/SATAXPCIE7/SATAGP7	Primary(3.3V/1.8V)			Native	SCI	SATA_GP7 Testpoint	
	AB41	GPP_F5/DEVSLP3	Primary(3.3V/1.8V)			GPI	SCI		
	AB42	GPP_F6/DEVSLP4	Primary(3.3V/1.8V)			GPI	SCI		
	AB43	GPP_F7/DEVSLP5	Primary(3.3V/1.8V)			GPI	SCI		
	AB36	GPP_F8/DEVSLP6	Primary(3.3V/1.8V)			GPI	SCI		
	AB39	GPP_F9/DEVSLP7	Primary(3.3V/1.8V)			GPI	SCI		
	AB33	GPP_F10/SLCLOCK	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_F10 Testpoint	
	AB35	GPP_F11/SLOAD	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_F11 Testpoint	
	AA45	GPP_F12/SDATAOUT1	Primary(3.3V/1.8V)			GPI	SCI		
	AA44	GPP_F13/SDATAOUT0	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_F13 Testpoint	
	Y44	GPP_F14	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_F14 Testpoint	
	Y43	GPP_F15/USB2_OC0_4	Primary(3.3V/1.8V)			GPI	SCI	USB_OC4# Testpoint	
	Y41	GPP_F16/USB2_OC0_5	Primary(3.3V/1.8V)			GPI	SCI	USB_OC4# Testpoint	
	W44	GPP_F17/USB2_OC0_6	Primary(3.3V/1.8V)			GPI	SCI	USB_OC4# Testpoint	
	W43	GPP_F18/USB2_OC0_7	Primary(3.3V/1.8V)			GPI	SCI	USB_OC4# Testpoint	
	W42	GPP_F19/EDP_VDDEN	Primary(3.3V/1.8V)			GPI	SCI	LIMA_ENVDD Testpoint	
	W45	GPP_F20/EDP_BKLTEN	Primary(3.3V/1.8V)			GPI	SCI	BKLTEN_PCH	
	W46	GPP_F21/EDP_BKLTCTL	Primary(3.3V/1.8V)			GPI	SCI	BKL_PWM_PCH	
	W39	GPP_F22	Primary(3.3V/1.8V)			GPI	SCI		
	Y46	GPP_F23	Primary(3.3V/1.8V)			GPI	SCI		
GPP_G	U43	GPP_G0/FAN_TACH_0	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G0 Testpoint	
	U42	GPP_G1/FAN_TACH_1	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G1 Testpoint	
	U41	GPP_G2/FAN_TACH_2	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G2 Testpoint	
	M44	GPP_G3/FAN_TACH_3	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G3 Testpoint	
	U36	GPP_G4/FAN_TACH_4	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G4 Testpoint	
	P41	GPP_G5/FAN_TACH_5	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G5 Testpoint	
	T45	GPP_G6/FAN_TACH_6	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G6 Testpoint	
	T44	GPP_G7/FAN_TACH_7	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G7 Testpoint	
	R46	GPP_G8/FAN_PWM_0	Primary(3.3V/1.8V)			Native	SCI	PCH_GPP_G8 Testpoint	
	R43	GPP_G9/FAN_PWM_1	Primary(3.3V/1.8V)			Native	SCI	PCH_GPP_G9 Testpoint	
	U39	GPP_G10/FAN_PWM_2	Primary(3.3V/1.8V)			Native	SCI	PCH_GPP_G10 Testpoint	
	N42	GPP_G11/FAN_PWM_3	Primary(3.3V/1.8V)			Native	SCI	PCH_GPP_G11 Testpoint	
	R39	GPP_G12/GSXDOUT	Primary(3.3V/1.8V)			GPI	SCI		
	R36	GPP_G13/GSXSLOAD	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G13 Testpoint	
	R42	GPP_G14/GSXDIN	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G14 Testpoint	
GPP_H	R41	GPP_G15/GSXSRESET#	Primary(3.3V/1.8V)			GPI	SCI	PCH_GPP_G15	
	P43	GPP_G16/GSXCLK	Primary(3.3V/1.8V)			GPI	SCI		
	N44	GPP_G17/ADR_COMPLETE	Primary(3.3V/1.8V)			GPI	SCI	GPP_G17 Testpoint	
	N43	GPP_G18/NMI#	Primary(3.3V/1.8V)			GPI	SCI	NMI# Testpoint	
	M45	GPP_G19/SMI#	Primary(3.3V/1.8V)			GPI	SCI	EC_SMI#	
	R35	GPP_G20	Primary(3.3V/1.8V)			GPI	SCI		
	L35	GPP_G21	Primary(3.3V/1.9V)			GPI	SCI	SIO_SCKAP_EN	
	L44	GPP_G22	Primary(3.3V/1.10V)			GPI	SCI		
	L43	GPP_G23	Primary(3.3V/1.11V)			GPI	SCI		
	AT33	GPP_H0/SRCCLKREQ6#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#6 PU 10K to +3VS_S0	
	AR31	GPP_H1/SRCCLKREQ7#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#7 PU 10K to +3VS_S0	
	BD32	GPP_H2/SRCCLKREQ8#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#8 PU 10K to +3VS_S0	
	BC32	GPP_H3/SRCCLKREQ9#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#9 PU 10K to +3VS_S0	
	BB31	GPP_H4/SRCCLKREQ10#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#10 PU 10K to +3VS_S0	
	BC33	GPP_H5/SRCCLKREQ11#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#11 PU 10K to +3VS_S0	
	BA33	GPP_H6/SRCCLKREQ12#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#12 PU 10K to +3VS_S0	
	AW33	GPP_H7/SRCCLKREQ13#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#13 PU 10K to +3VS_S0	
	BB33	GPP_H8/SRCCLKREQ14#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#14 PU 10K to +3VS_S0	
	BD33	GPP_H9/SRCCLKREQ15#	Primary(3.3V/1.8V)			GPI	SCI	CLKREQ_PCIE#15 PU 10K to +3VS_S0	
	BD34	GPP_H10/SML2CLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML2CLK0 Testpoint	
	AW35	GPP_H11/SML2DATA	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML2DATA0 Testpoint	
	BD35	GPP_H12/SML2ALERT#	Primary(3.3V/1.8V)	L(20K)		GPO	SCI	SML2ALERT0# Testpoint	L(20K)
	BC35	GPP_H13/SML3CLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML3CLK0 Testpoint	
	BA35	GPP_H14/SML3DATA	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML3DATA0 Testpoint	
	BB36	GPP_H15/SML3ALERT#	Primary(3.3V/1.8V)			GPI	SCI	SML3ALERT0# Testpoint	
	BD39	GPP_H16/SML4CLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML4CLK0 Testpoint	
	BE34	GPP_H17/SML4DATA	Primary(3.3V/1.8V)			GPI	SCI	PCH_SML4DATA0 Testpoint	
	BC36	GPP_H18/SML4ALERT#	Primary(3.3V/1.8V)			GPI	SCI	SML4ALERT0# Testpoint	
	BB38	GPP_H19/ISH_I2C0_SDA	Primary(3.3V/1.8V)			GPI	SCI	ISH_I2C_0_SCL Testpoint	
	BC38	GPP_H20/ISH_I2C0_SCL	Primary(3.3V/1.8V)			GPI	SCI	ISH_I2C_0_SDA Testpoint	
	BE39	GPP_H21/ISH_I2C1_SDA	Primary(3.3V/1.9V)			GPI	SCI	ISH_I2C1_SCL Testpoint	
	BD38	GPP_H22/ISH_I2C1_SCL	Primary(3.3V/1.10V)			GPI	SCI	ISH_I2C1_SDA Testpoint	
	BD36	GPP_H23	Primary(3.3V/1.11V)			GPI	SCI	BIOSWA PW	
GPP_I	AW4	GPP_I0/DDPB_HPD0	Primary(3.3V/1.8V)			GPI	SCI	PCH_HDMIOUT_HPD PU 100 to +3VS_S0	
	AY2	GPP_I1/DDPC_HPD1	Primary(3.3V/1.8V)			GPI	SCI	DDPC_HPD Testpoint	
	AV4	GPP_I2/DDPD_HPD2	Primary(3.3V/1.8V)			GPI	SCI	DDPD_HPD Testpoint	
	BA4	GPP_I3/DDPE_HPD3	Primary(3.3V/1.8V)			GPI	SCI	EC_SCI#	
	BD7	GPP_I4/EDP_HPD	Primary(3.3V/1.8V)			GPI	SCI	EDP_HPD_R PD 100K	
	BA5	GPP_I5/DDPB_CTRLCLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_HDMIOUT_CLK PU 2.2K to +3VS_S0	
	BC4	GPP_I6/DDPB_CTRLDATA	Primary(3.3V/1.8V)	L(20K)		GPO	SCI	PCH_HDMIOUT_DATA PU 2.2K to +3VS_S0	L(20K)
	BB3	GPP_I7/DDPC_CTRLCLK	Primary(3.3V/1.8V)			GPI	SCI	PCH_DPC_CLK PU 2.2K to +3VS_S0	

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Compal Electronics, Inc.			
Title	GPIO Table & SMBUS BD		
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Date: Thursday, November 22, 2018	Sheet 72 of 73		

Note Color **Version change list (P.I.R. List)** **EVT to DVT for HW**

Item	Page	Modify List	Reason for change	Date
1	37	JFUN1 change to CI1150M2HD0-R0-NH follow conn list		2018/04/17
2	36	Remove HP_det circuit, Remove Pin99, 100 SC_HPL,SC_HPR I2S audio from Pin164, 165, 167 change to Pin 103, 104, 106		2018/04/17
3	43	Remove Monitor mode Headphone Switch circuit		2018/04/17
4	50	Remove Pin70 HP_SEL, Pin122 PD_RESET		2018/04/17
5	45	UAA1 Pin15 add RAC58 to I2S_BLK_SW_AMP		2018/04/17
6	46	UAA2 Pin15 add RAC59 to I2S_BLK_SW_AMP		2018/04/17
7	21 28	Below item from Page 21 change to 28 RV29 NBMCO@ change to @ UV11, UV12, RV30, RV38 BMCO@ change DIS@		2018/04/17
8	03, 15, 40 50, 51, 52,	Change S0IX@ & NS0IX@ to MSB@ & NMSB@		2018/05/30
9	49	BT Wake = BT MFB need change to +3V3_DSW pull high		2018/04/17
8	page	Value		2018/04/17

Note Color **Version change list (P.I.R. List)** **DVT to PVT for HW**

Item	Page	Modify List	Reason for change	Date
1	34	RHI13 RHD88 RHD89 change to @ RHD62, RHD64, RHD65, RHD68, RHD69, RHD71, RHD72, RHD75 0ohm change to 2.2ohm LHD1, LHD2, LHD3, LHD4 change to @ RHD63, RHD66, RHD70, RHD73 91ohm change to 820ohm		2018/07/30
2	32	DT11 @ESD@ change to ESD@		2018/07/30
3	32, 47, 48	DT13,DUH2,DUH3 from SC300004G00 change to SC300003Z00		2018/07/30
4	46	RAA14 from 100Kohm change to 1Kohm		2018/07/30
5	53	JHDSW1 Pin3, Pin4 SWAP for HDMI-SW always keep low		2018/07/30
6	38	SATA redriver remove source for PARADE		
7	15	Add 2.2K PH +3VS_S0 for DDI HW enable		
8	22	VGA_PROCHOT# EC pin name change to EC_GPIO30 Add 0ohm(RT881) to VGA reserve EC GPIO control TBT RESET_N		
9	29	Add RT879, RT880 for TBT DP AUX_P PD and AUX_N PH Add RT881 for EC GPIO control TBT RESET_N Follow Intel suggest remove RT855, RT856		
10	31	RT826 change to @, RT838 change to mount Change PD VIN_3V3 from +3V3_DSW to +3VALW_S5		
11	32	JTYPEC1 SBU1, SBU2 SWAP for TBT device no function		
12	45	UAA2 A_SEL RAA14 pull high from 100K change to 1K		
13	46	UAA1 A_SEL RAA6 pull down from 100K change to 1K		
14	47	JUSB1 Pin7 change from GND to USB_KDBG_DET for debug card no function		
15	49	Add RBT11 10K for BT_LINK pull low		
16	53	JHDSW1 Pin3 and Pin4 SWAP		
17	22	Add CLKREQ_VGA# circuit follow Intel and AMD request RV199, RV200, QHV2		
18	5	Add CH39 for H_PROCHOT#_R follow EMI request		
19	22,50	EC_GPIO36 change form DGPU_OVERT# reseve to AMP +12V power control RAA32		
20	45	Add QAA1, RAA35, RAA37, CAA77, QAA3, RAA38, RAA32 for AMP +12V control Add RAA33, RAA36, RAA34, CAA76, QAA2 for AMP +3V control Add QAA4, RAC39, RAC40 for AMP SMBUS level shift		
21	36	Change Scalar SC_MODE3 link to PM_SLP_S3# RSC177		
22	5, 15	HDMI function from DDI1 + DDPB change to DDI3 + DDPD, HPD From DDPB_HPD0 change to DDPD_HPD2		

PVT to SVT for HW

Item	Page	Modify List	Reason for change	Date
1		Cahnge 0_0402_5% to short pad RAA22, RAA24, RAA32, RAA39, RAA40, RAA49, RAA50, RAA51, RAA52, RAC6, RAC27, RAC28, RAC29, RAC31, RAC34, RAC51, RBT8, RBT9, RBT10, RC2, RC15, RC16, RC20, RC21, RC22, RC29, RC36, RCHG4, RCR1, CV3, RDC12, RDC16, RH44, RH48, RH49, RH50, RH51, RH53, RH55, RH56, RH57, RH61, RH70, RH73, RH85, RH91, RH113, RH114, RH116, RH117, RH118, RHD23, RHD24, RHD25, RHD32, RHD33, RHD37, RHD40, RHD41, RHD58, RSSD4, RSW1, RSW3, RSW6, RSW16, RSW17, RSW18, RT13, RT838, RT842, RT858,RT861 ,RT866, RT871, RT872, RV38, RV196, RV197, RWL5, RWL12, RAC11, RSC3, RSC81, RSC82, RSC83, RSC84, RSC121, RSC122, RSC123, RSC126,RSC149, RSC129, RSC130, RSC135, RSC138, RSC144, RSC146, RSC151, RSC159, RSC163, RSC170,RSC175, RSC177, RSC178, RC33, RDC4, RDC7, REC30, REC32, RD4, RD5, RD6, RD14, RD16, RD18		2018/10/30
2		Cahnge 0_0603_5% to short pad RBT1, RC35, RD7, RD19, RPWR1		2018/10/30
3		Cahnge 0_0805_5% to short pad RH119, RT857, RV186		2018/10/30
4	17, 36	UH1,AL48 connect Scalar pin 94 PCH notify scalar, system resume from MSB		2018/10/30
5	21	TBT BSBU1,2 reserve 100Kohm to GND Follow Intel request		2018/10/30
6	34	HDMI Conn pin8 connect to DHD1 ESD diode pin3 Follow EMC request		2018/10/30
7	37	Touch power from +5VS_S0 change to +5VALW_S5 Solve Touch resume issue		2018/10/30
8	45	RAA45, pin2 change +3V3_DSW to +5VALW_S5 For power control status change power source		2018/10/30
9	53	SW2 change to unmount This power switch only for NPI phase		2018/10/30

Pre-PVT to PVT for HW

Item	Page		Reason for change	Date
1	14	RPH3 Pin1 net CLKREQ_VGA# remove change pull high to pull low		2018/02/02
2	43	JFA1 JUMP change to RFA8 0 ohm for bom control		2018/02/02
3	28	Reserved LV8 for AMD request		2018/02/02

SIT to SVT for HW

Item	Page		Reason for change	Date
1	08	CC30, CC32 from 0805 change to 0603		2018/03/12
2	42	For MP REC15 change to 150K ohm (SD028150380)		2018/03/12
3	48~65	Combine Power schematic 0320 modify item for HW 1. Add DGPU_PWROK PU1008 pin1 2. Change PU700 pin19 to VDDC_PWROK pin39 to VDDC_PGOOD		2018/03/12
4	3	Update note list for SKU Bom config		2018/03/12