Model:TIGRIS_SFF
PCB Ver: A00
PCB Number: 12125 -2
PCB P/N:
SCH Ver: A00
PCBA:

PCB BOARD SIZE
4 Layers
200mmX 244mm

BOM Configuration
Unmount : (R)

1 BUILD
Shark Bay :
LGA1150 : Haswell
Chipset : Lynx Point H81
LAN : Gb LAN RTL8151GD

PAGE	TITLE	Quantity
01	Cover Page	
02	BLOCK DIAGRAM	
03	Power Delivery	
04	POWER GOOD AND RESET DIAGRAM	
05	CLOCKS DIAGRAM	
06	Power Sequence	
07	POWER Map	
08	GPIO TABLE	
09	TBD	
10	CPU uLGA 1150_1	
11	CPU uLGA 1150_2	
12	CPU uLGA 1150_3	
13	CPU uLGA 1150_4	
14	XDP/80 PORT HEADER	
15	DDR3 CHA DIMM 0	
16	TBD	
17	DDR3 CHB DIMM 0	
18	TBD	
19	Lynxpoint_AUDIO/GPIO/SPI	
20	Lynxpoint_CLK	
21	Lynxpoint_SATA/FAN/DP/VGA	
22	Lynxpoint_FDI/PCIE/DMI/USB	
23	Lynxpoint_GND/STRAPS	
24	Lynxpoint_POWER	
25	SATA Port	
26	PCIEX16 CONNECTOR	
27	VGA Port	
28	Display Port	
29	HDMI PORT	
30	FRONT USB20 HEADER	

PAGE	TITLE	Quantity
31	TPM&TCM	
32	USB+RJ45	
33	REAR USB30_1	
34	REAR USB20_2	
35	LAN RTL8151G	
36	AUDIO CODEC_ALC3220	
37	AUDIO CODEC JACKS	
38	DSW	
39	SIO_SCH55553	
40	FAN CIRCUITS/HOLE	
41	KB/MS/Serial Port	
42	PCIEX1_ CONN	
43	MINI PCIE SLOT	
44	EMC	
45	PWR/FNT PNL	
46	DUAL POWER	
47	DC to DC_5V/3D3V(RT8243B)	
48	Run power/USB power	
49	DDR POWER	
50	SYSTEM POWER	
51	CPU_VRD 12-5_1	
52	CPU_VRD 12-5_2	

<Variant Name>

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Title: Cover Page

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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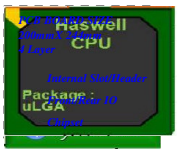

VRM 12.5
(3 Phase 95W)

PCIE_X16 Gen2

PCI EXPRESS Gen2

Display Port v1.2

Port B

INTEL
Haswell
SOCKET H3 uLGA LGA1150
(65W)
0.9144mmX0.9144mm

Channel A

1600MHZ/1333MHZ

DDR3 DIMM
Unbuffered 8GB

Channel B

1600MHZ/1333MHZ

DDR3 DIMM
Unbuffered 8GB

14.318MHz
33MHz
24MHz or 48MHz
100 MHz
120 MHz
133 MHz

PCH
CLOCK
Buffer

25M

100MHz
100MHz

PDMI X2

PDMI X4

8 PIN PWR CONN FOR
SINGLE POWER RAIL PSU

CPU-4PIN CONN

D-SUB PORT

RGB

INTEL PCH

Lynx Point
H81

FCBGA 708PIN
23 mm x 22 mm

PCIE Port3

PCIE Gen2 Interface 5.0Gbps

PCIE X1

PCIE Port4

PCIE Gen1 Interface 2.5Gbps

Intel LAN
RTL8151GD

RJ45

25M

USB3.0x2 REAR

USB2.0X2 FRONT HEADER

USB2.0x2 REAR (+RJ45)

USB2.0X2 REAR

USB 3.0 *2

5.0GbS

USB 2.0 *8

480MbS

SPI Flash ROM
8MB

Quad reader SPI BUS

GPIO

SMBus 2.0

SATA0-HDD
(Blue color)

SATA3.0 BUS

SATA1-ODD
(White color)

SATA2.0 BUS

HDA CODEC
ALC3220

High Definition Audio

REAR
Line - IN /
MIC -IN

REAR
Line - Out

FRONT
HP - OUT

FRONT
MIC -IN

Internal
SPEAKER

133MHz
100MHz
96MHz
14.318MHz
32.768KHz

32.7K

TPM 1.2
ST33ZP24AR

LPC BUS

LPC BUS

SIO SCH5553

FAN CNTL/TACH

CPU 1X5 FAN

SYS 1X5 FAN

KB/MS/COM

<Variant Name>

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Title: Block Diagram

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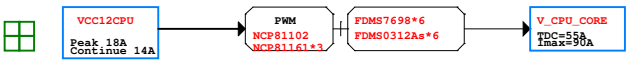
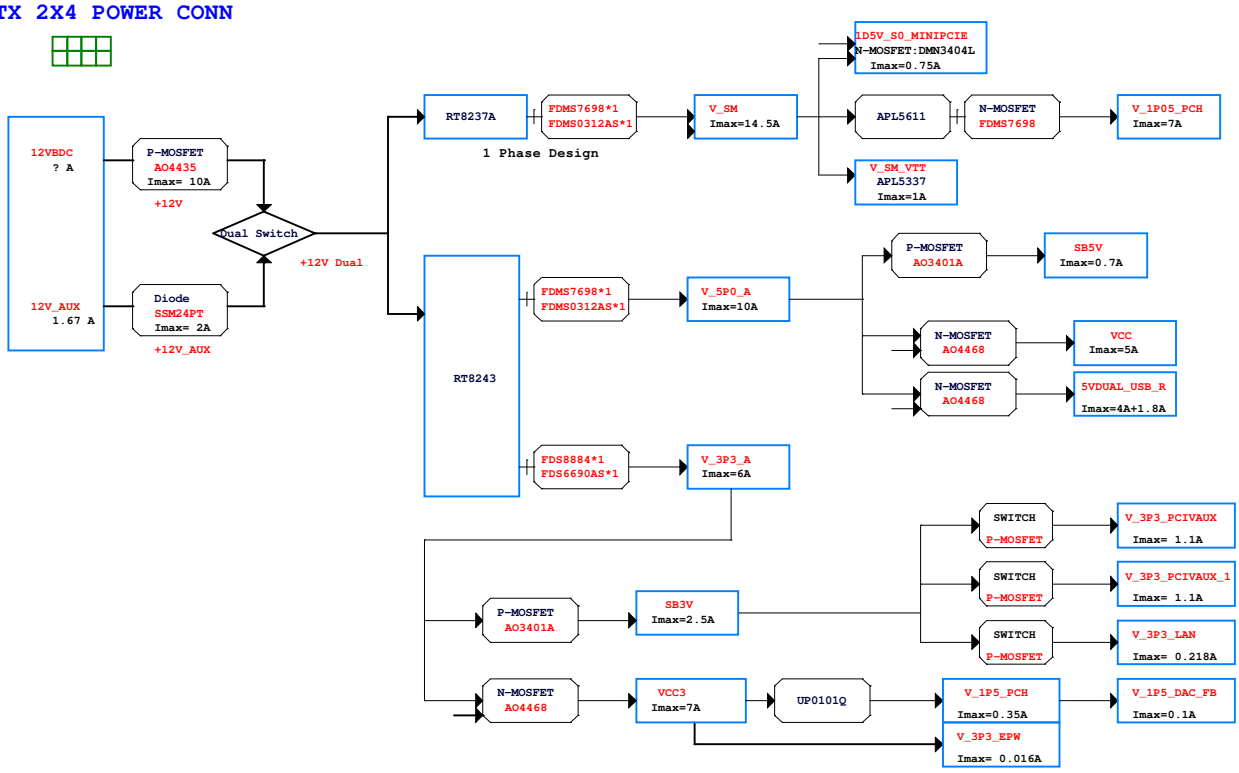
CPU 2X2 POWER CONN



3 Phase Design

ATX 2X4 POWER CONN



<Variant Name>

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Title: Power Delivery

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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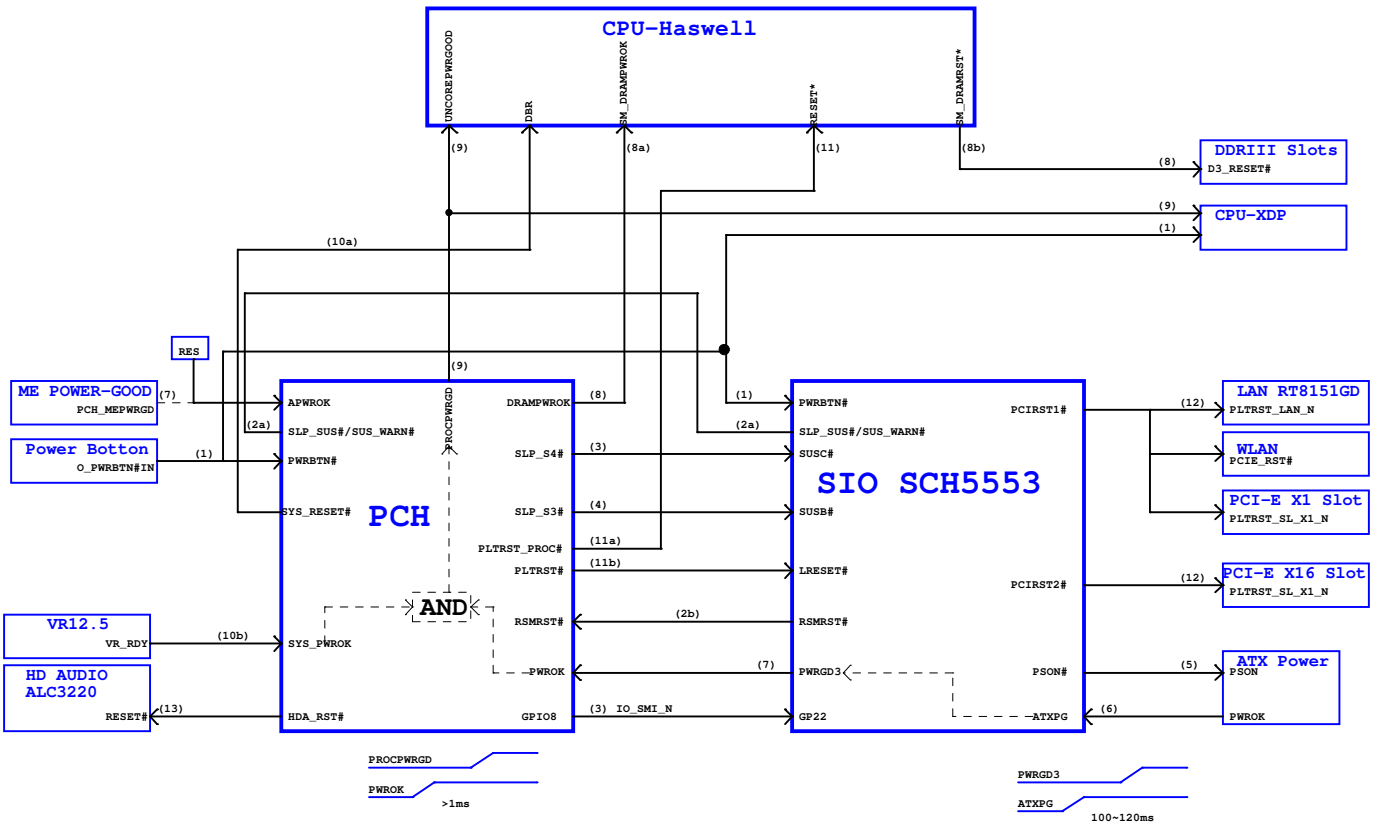
RESET / Power Good MAP



<Variant Name>

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Title: RESET / Power Good MAP

Size: C | Document Number: ROSA TIGRIS SFF | Rev: 1

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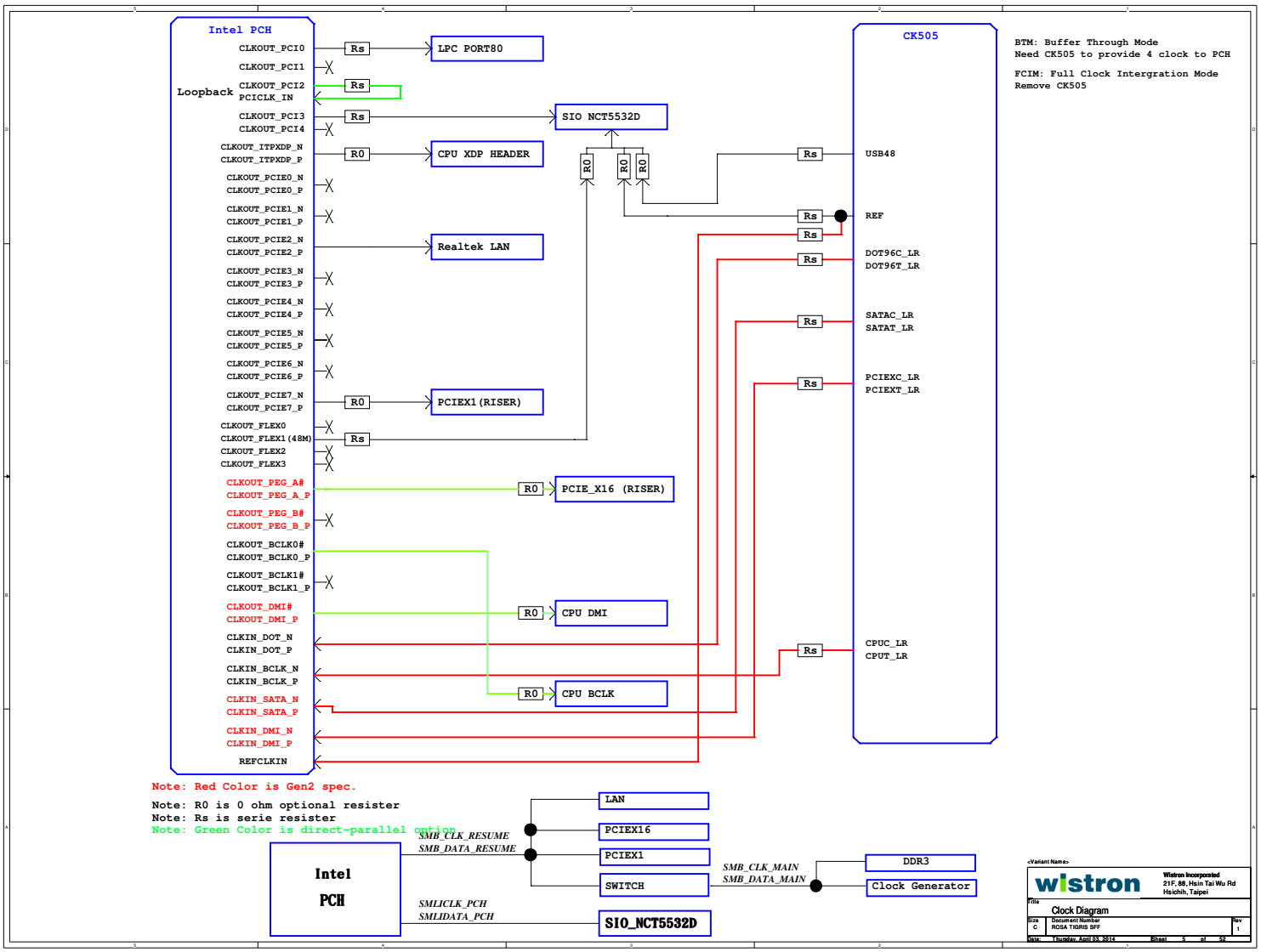
Intel PCH
CLKOUT_PCI0
CLKOUT_PCI1
Loopback
CLKOUT_PCI2
PCICLK_IN
CLKOUT_PCI3
CLKOUT_PCI4
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_PCIE0_N
CLKOUT_PCIE0_P
CLKOUT_PCIE1_N
CLKOUT_PCIE1_P
CLKOUT_PCIE2_N
CLKOUT_PCIE2_P
CLKOUT_PCIE3_N
CLKOUT_PCIE3_P
CLKOUT_PCIE4_N
CLKOUT_PCIE4_P
CLKOUT_PCIE5_N
CLKOUT_PCIE5_P
CLKOUT_PCIE6_N
CLKOUT_PCIE6_P
CLKOUT_PCIE7_N
CLKOUT_PCIE7_P
CLKOUT_FLEX0
CLKOUT_FLEX1(48M)
CLKOUT_FLEX2
CLKOUT_FLEX3
CLKOUT_PEG_A#
CLKOUT_PEG_A_P
CLKOUT_PEG_B#
CLKOUT_PEG_B_P
CLKOUT_BCLK0#
CLKOUT_BCLK0_P
CLKOUT_BCLK1#
CLKOUT_BCLK1_P
CLKOUT_DMI#
CLKOUT_DMI_P
CLKIN_DOT_N
CLKIN_DOT_P
CLKIN_BCLK_N
CLKIN_BCLK_P
CLKIN_SATA_N
CLKIN_SATA_P
CLKIN_DMI_N
CLKIN_DMI_P
REFCLKIN
Rs
R0
LPC PORT80
SIO NCT5532D
CPU XDP HEADER
Realtek LAN
PCIEX1(RISER)
PCIE_X16 (RISER)
CPU DMI
CPU BCLK
CK505
USB48
REF
DOT96C_LR
DOT96T_LR
SATAC_LR
SATAT_LR
PCIEXC_LR
PCIEXT_LR
CPUC_LR
CPUT_LR
BTM: Buffer Through Mode
Need CK505 to provide 4 clock to PCH
FCIM: Full Clock Intergration Mode
Remove CK505
Note: Red Color is Gen2 spec.
Note: R0 is 0 ohm optional resister
Note: Rs is serie resister
Note: Green Color is direct-parallel option
Intel
PCH
SMB_CLK_RESUME
SMB_DATA_RESUME
SMLICLK_PCH
SMLIDATA_PCH
LAN
PCIEX16
PCIEX1
SWITCH
SIO_NCT5532D
SMB_CLK_MAIN
SMB_DATA_MAIN
DDR3
Clock Generator
<Variant Name>
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Hsichih, Taipei
Title
Clock Diagram
Size
C
Document Number
ROSA TIGRIS SFF
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1
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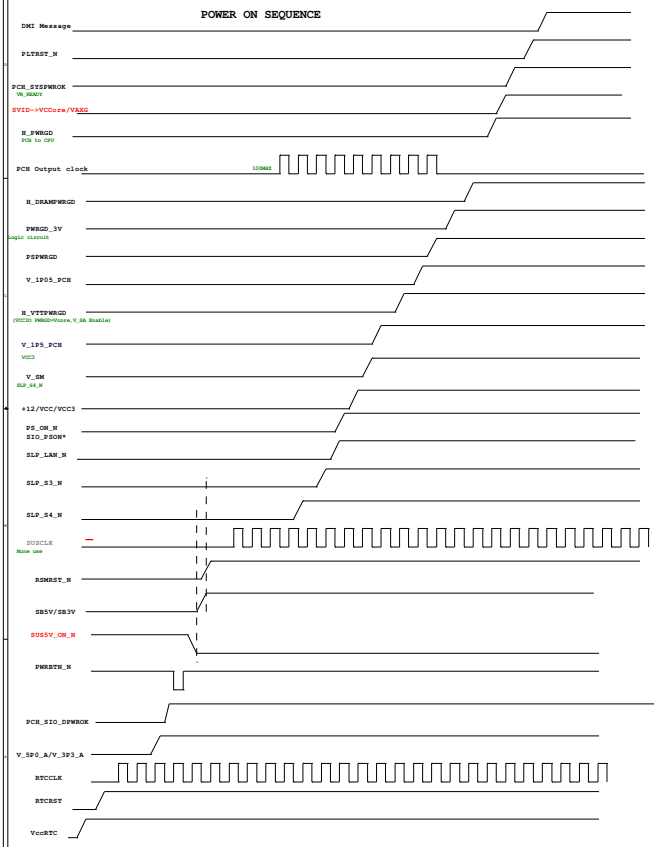

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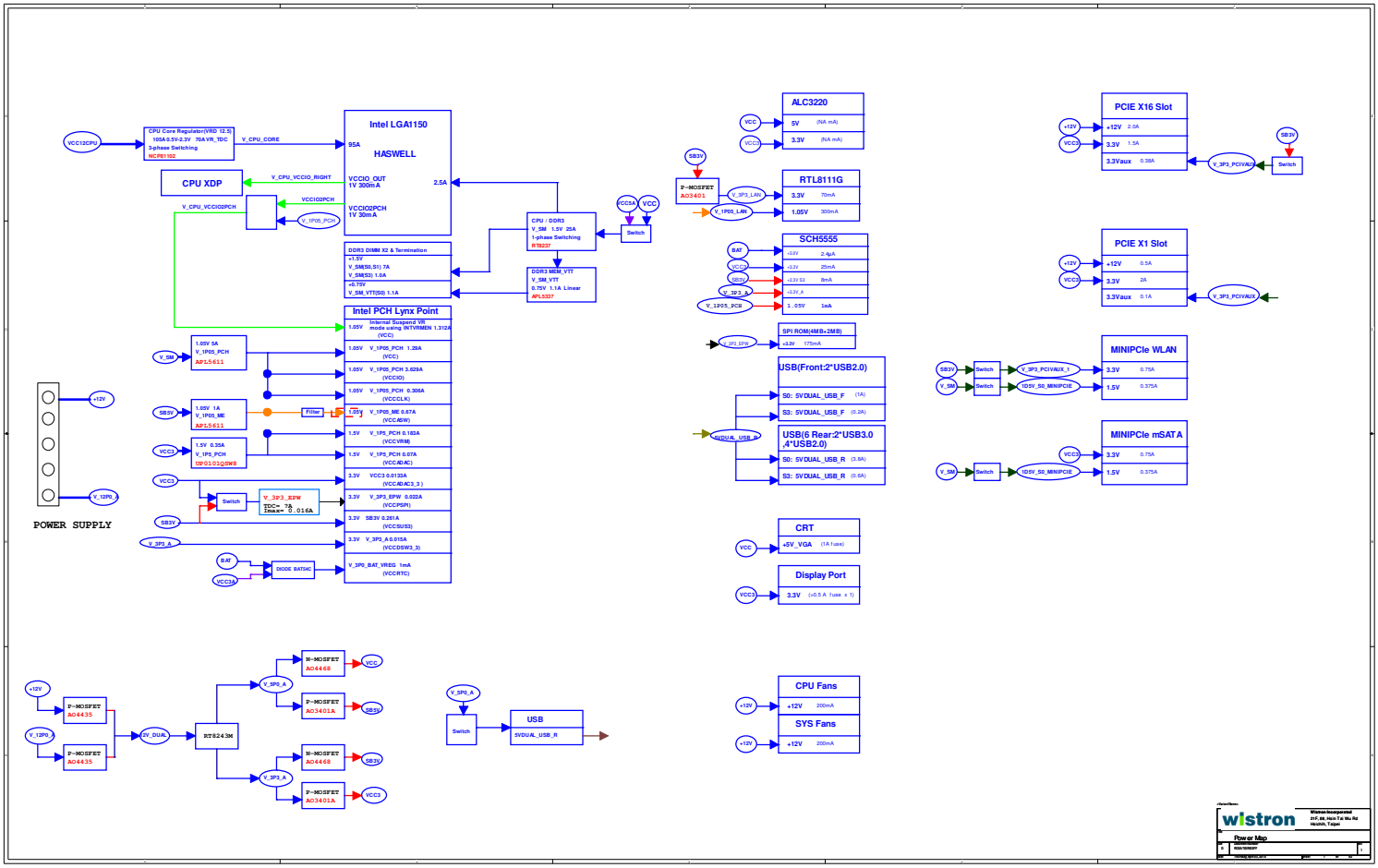
Power Sequence


Intel LGA1150
HASWELL
CPU XDP
Intel PCH Lynx Point
POWER SUPPLY
ALC3220
RTL8111G
SCH5555
USB(Front:2*USB2.0)
USB(6 Rear:2*USB3.0 ,4*USB2.0)
CRT
Display Port
PCIE X16 Slot
PCIE X1 Slot
MINIPCIe WLAN
MINIPCIe mSATA
CPU Fans
SYS Fans
USB
RT8243M
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Power Map

TBD

<Variant Name>

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Title

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<Variant Name>

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Title
TBD

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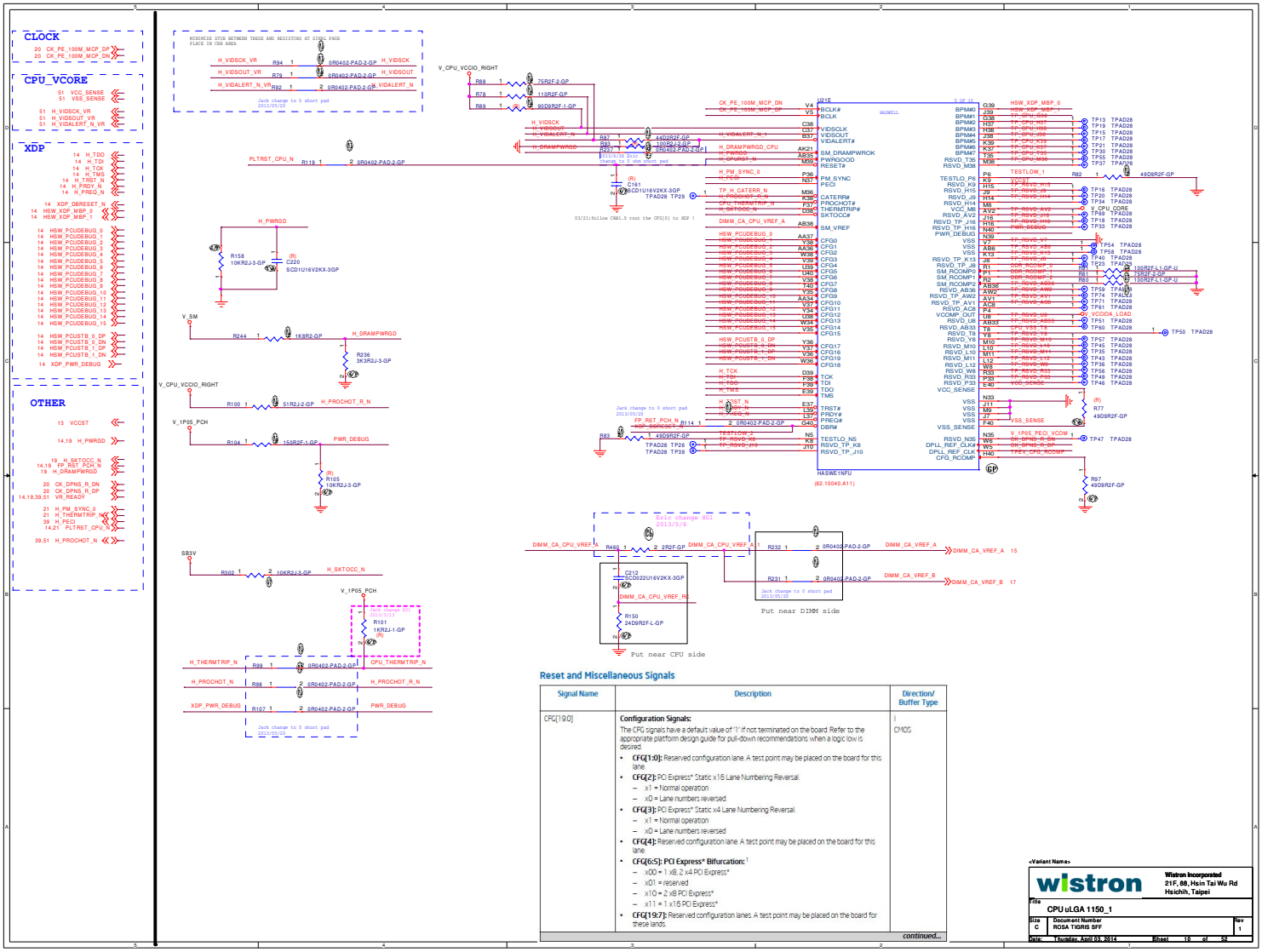
CLOCK
CPU_VCORE
XDP
OTHER
Reset and Miscellaneous Signals
Signal Name
Description
Direction/ Buffer Type
CFG[19:0]
Configuration Signals:
The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.
CFG[1:0]: Reserved configuration lane. A test point may be placed on the board for this lane.
CFG[2]: PCI Express* Static x16 Lane Numbering Reversal.
– x1 = Normal operation
– x0 = Lane numbers reversed.
CFG[3]: PCI Express* Static x4 Lane Numbering Reversal.
– x1 = Normal operation
– x0 = Lane numbers reversed
CFG[4]: Reserved configuration lane. A test point may be placed on the board for this lane.
CFG[6:5]: PCI Express* Bifurcation:
– x00 = 1 x8, 2 x4 PCI Express*
– x01 = reserved
– x10 = 2 x8 PCI Express*
– x11 = 1 x16 PCI Express*
CFG[19:7]: Reserved configuration lanes. A test point may be placed on the board for these lands.
I
CMOS
continued...
Put near CPU side
Put near DIMM side
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Hsichih, Taipei
CPU uLGA 1150_1
Size C
Document Number ROSA TIGRIS SFF
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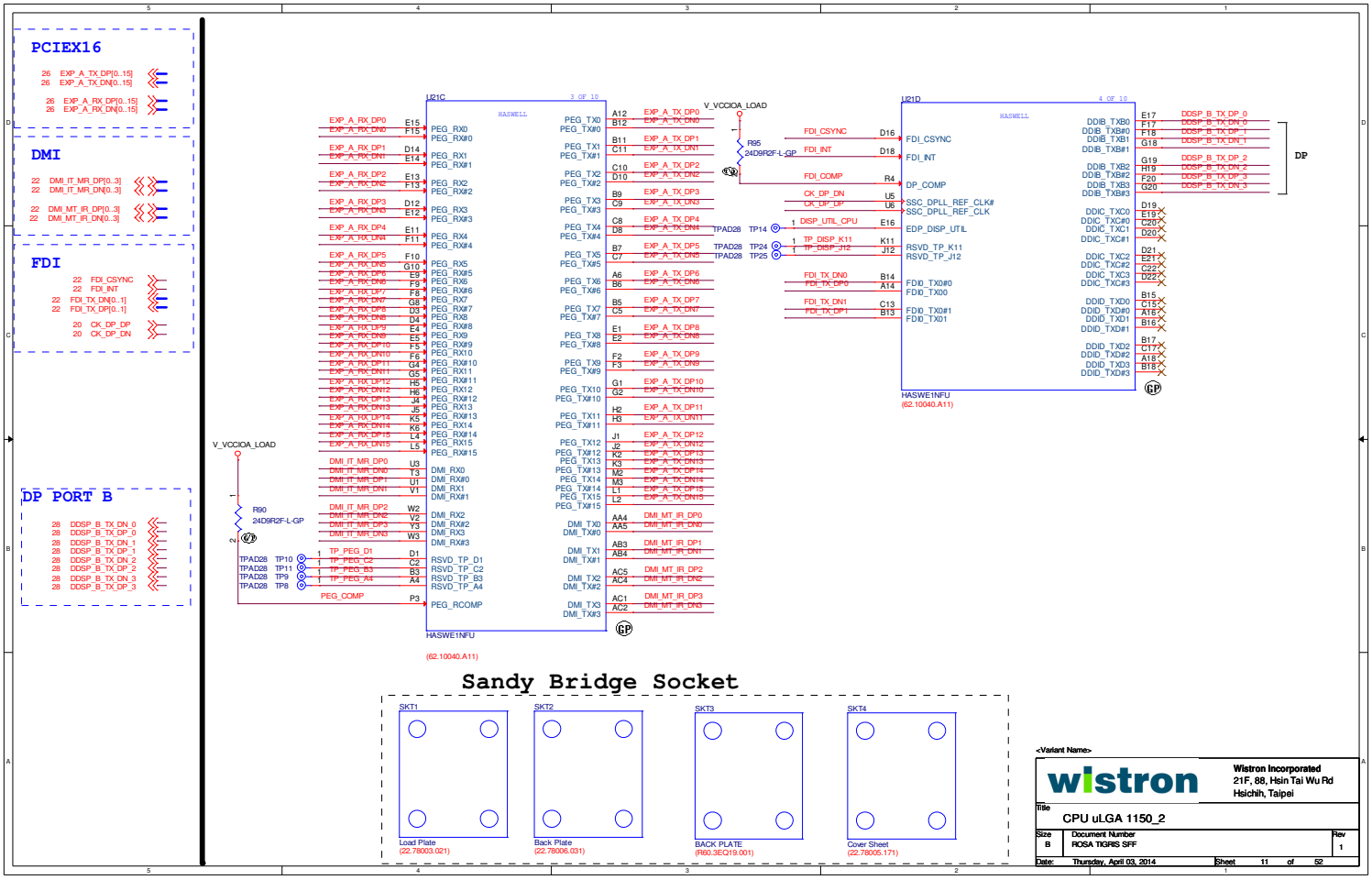
PCIEX16
26 EXP_A_TX_DP[0..15]
26 EXP_A_TX_DN[0..15]
26 EXP_A_RX_DP[0..15]
26 EXP_A_RX_DN[0..15]
DMI
22 DMI_IT_MR_DP[0..3]
22 DMI_IT_MR_DN[0..3]
22 DMI_MT_IR_DP[0..3]
22 DMI_MT_IR_DN[0..3]
FDI
22 FDI_CSYNC
22 FDI_INT
22 FDI_TX_DN[0..1]
22 FDI_TX_DP[0..1]
20 CK_DP_DP
20 CK_DP_DN
DP PORT B
28 DDSP_B_TX_DN_0
28 DDSP_B_TX_DP_0
28 DDSP_B_TX_DN_1
28 DDSP_B_TX_DP_1
28 DDSP_B_TX_DN_2
28 DDSP_B_TX_DP_2
28 DDSP_B_TX_DN_3
28 DDSP_B_TX_DP_3
U21C
3 OF 10
HASWELL
EXP_A_RX_DP0
EXP_A_RX_DN0
EXP_A_RX_DP1
EXP_A_RX_DN1
EXP_A_RX_DP2
EXP_A_RX_DN2
EXP_A_RX_DP3
EXP_A_RX_DN3
EXP_A_RX_DP4
EXP_A_RX_DN4
EXP_A_RX_DP5
EXP_A_RX_DN5
EXP_A_RX_DP6
EXP_A_RX_DN6
EXP_A_RX_DP7
EXP_A_RX_DN7
EXP_A_RX_DP8
EXP_A_RX_DN8
EXP_A_RX_DP9
EXP_A_RX_DN9
EXP_A_RX_DP10
EXP_A_RX_DN10
EXP_A_RX_DP11
EXP_A_RX_DN11
EXP_A_RX_DP12
EXP_A_RX_DN12
EXP_A_RX_DP13
EXP_A_RX_DN13
EXP_A_RX_DP14
EXP_A_RX_DN14
EXP_A_RX_DP15
EXP_A_RX_DN15
PEG_RX0
PEG_RX#0
PEG_RX1
PEG_RX#1
PEG_RX2
PEG_RX#2
PEG_RX3
PEG_RX#3
PEG_RX4
PEG_RX#4
PEG_RX5
PEG_RX#5
PEG_RX6
PEG_RX#6
PEG_RX7
PEG_RX#7
PEG_RX8
PEG_RX#8
PEG_RX9
PEG_RX#9
PEG_RX10
PEG_RX#10
PEG_RX11
PEG_RX#11
PEG_RX12
PEG_RX#12
PEG_RX13
PEG_RX#13
PEG_RX14
PEG_RX#14
PEG_RX15
PEG_RX#15
DMI_IT_MR_DP0
DMI_IT_MR_DN0
DMI_IT_MR_DP1
DMI_IT_MR_DN1
DMI_IT_MR_DP2
DMI_IT_MR_DN2
DMI_IT_MR_DP3
DMI_IT_MR_DN3
DMI_RX0
DMI_RX#0
DMI_RX1
DMI_RX#1
DMI_RX2
DMI_RX#2
DMI_RX3
DMI_RX#3
RSVD_TP_D1
RSVD_TP_C2
RSVD_TP_B3
RSVD_TP_A4
PEG_RCOMP
PEG_TX0
PEG_TX#0
PEG_TX1
PEG_TX#1
PEG_TX2
PEG_TX#2
PEG_TX3
PEG_TX#3
PEG_TX4
PEG_TX#4
PEG_TX5
PEG_TX#5
PEG_TX6
PEG_TX#6
PEG_TX7
PEG_TX#7
PEG_TX8
PEG_TX#8
PEG_TX9
PEG_TX#9
PEG_TX10
PEG_TX#10
PEG_TX11
PEG_TX#11
PEG_TX12
PEG_TX#12
PEG_TX13
PEG_TX#13
PEG_TX14
PEG_TX#14
PEG_TX15
PEG_TX#15
DMI_TX0
DMI_TX#0
DMI_TX1
DMI_TX#1
DMI_TX2
DMI_TX#2
DMI_TX3
DMI_TX#3
HASWE1NFU
(62.10040.A11)
V_VCCIOA_LOAD
R90
24D9R2F-L-GP
TPAD28 TP10
TPAD28 TP11
TPAD28 TP9
TPAD28 TP8
TP_PEG_D1
TP_PEG_C2
TP_PEG_B3
TP_PEG_A4
V_VCCIOA_LOAD
R95
24D9R2F-L-GP
FDI_CSYNC
FDI_INT
FDI_COMP
CK_DP_DN
CK_DP_DP
DISP_UTIL_CPU
TP_DISP_K11
TP_DISP_J12
FDI_TX_DN0
FDI_TX_DP0
FDI_TX_DN1
FDI_TX_DP1
TPAD28 TP14
TPAD28 TP24
TPAD28 TP25
U21D
4 OF 10
HASWELL
FDI_CSYNC
FDI_INT
DP_COMP
SSC_DPLL_REF_CLK#
SSC_DPLL_REF_CLK
EDP_DISP_UTIL
RSVD_TP_K11
RSVD_TP_J12
FDI0_TX0#0
FDI0_TX00
FDI0_TX0#1
FDI0_TX01
HASWE1NFU
(62.10040.A11)
DDIB_TXB0
DDIB_TXB#0
DDIB_TXB1
DDIB_TXB#1
DDIB_TXB2
DDIB_TXB#2
DDIB_TXB3
DDIB_TXB#3
DDSP_B_TX_DP_0
DDSP_B_TX_DN_0
DDSP_B_TX_DP_1
DDSP_B_TX_DN_1
DDSP_B_TX_DP_2
DDSP_B_TX_DN_2
DDSP_B_TX_DP_3
DDSP_B_TX_DN_3
DP
DDIC_TXC0
DDIC_TXC#0
DDIC_TXC1
DDIC_TXC#1
DDIC_TXC2
DDIC_TXC#2
DDIC_TXC3
DDIC_TXC#3
DDID_TXD0
DDID_TXD#0
DDID_TXD1
DDID_TXD#1
DDID_TXD2
DDID_TXD#2
DDID_TXD3
DDID_TXD#3
Sandy Bridge Socket
SKT1
SKT2
SKT3
SKT4
Load Plate
(22.78003.021)
Back Plate
(22.78006.031)
BACK PLATE
(R60.3EQ19.001)
Cover Sheet
(22.78005.171)
<Variant Name>
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21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
CPU uLGA 1150_2
Size B
Document Number
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DDR DATA

15 M_DATA_A[0..63]
17 M_DATA_B[0..63]

15 M_DQS_A_DP[0..7]
15 M_DQS_A_DN[0..7]

17 M_DQS_B_DP[0..7]
17 M_DQS_B_DN[0..7]

DDR CMD/ADD

15 M_MAA_A[0..15]
17 M_MAA_B[0..15]

15 M_WE_A_N
15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
15 M_SBS_A2

17 M_WE_B_N
17 M_CAS_B_N
17 M_RAS_B_N
17 M_SBS_B0
17 M_SBS_B1
17 M_SBS_B2

DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1

15 M_SCKE_A0
15 M_SCKE_A1

15 M_ODT_A0
15 M_ODT_A1

17 M_SCS_B_N0
17 M_SCS_B_N1

17 M_SCKE_B0
17 M_SCKE_B1

17 M_ODT_B0
17 M_ODT_B1

DDR CLOCK

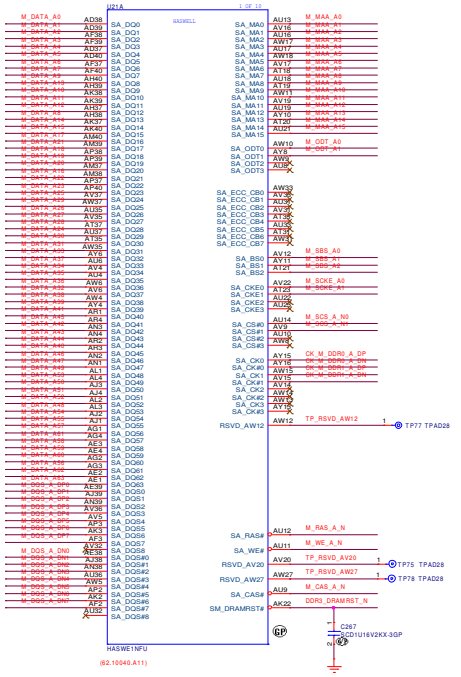
15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

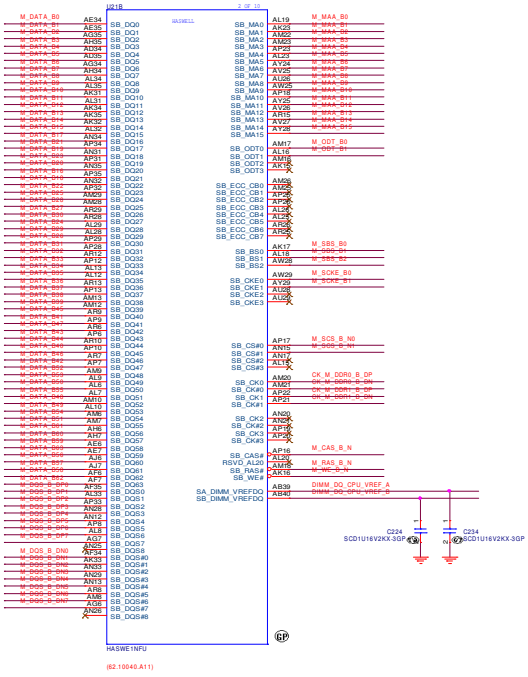
17 CK_M_DDR0_B_DP
17 CK_M_DDR0_B_DN
17 CK_M_DDR1_B_DP
17 CK_M_DDR1_B_DN

DDR OTHERS

15,17 DDR3_DRAMRST_N

17 DIMM_DQ_CPU_VREF_B
15 DIMM_DQ_CPU_VREF_A





<variant_name>

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Hsichih, Taipei

Title: CPU uLGA 1150_3

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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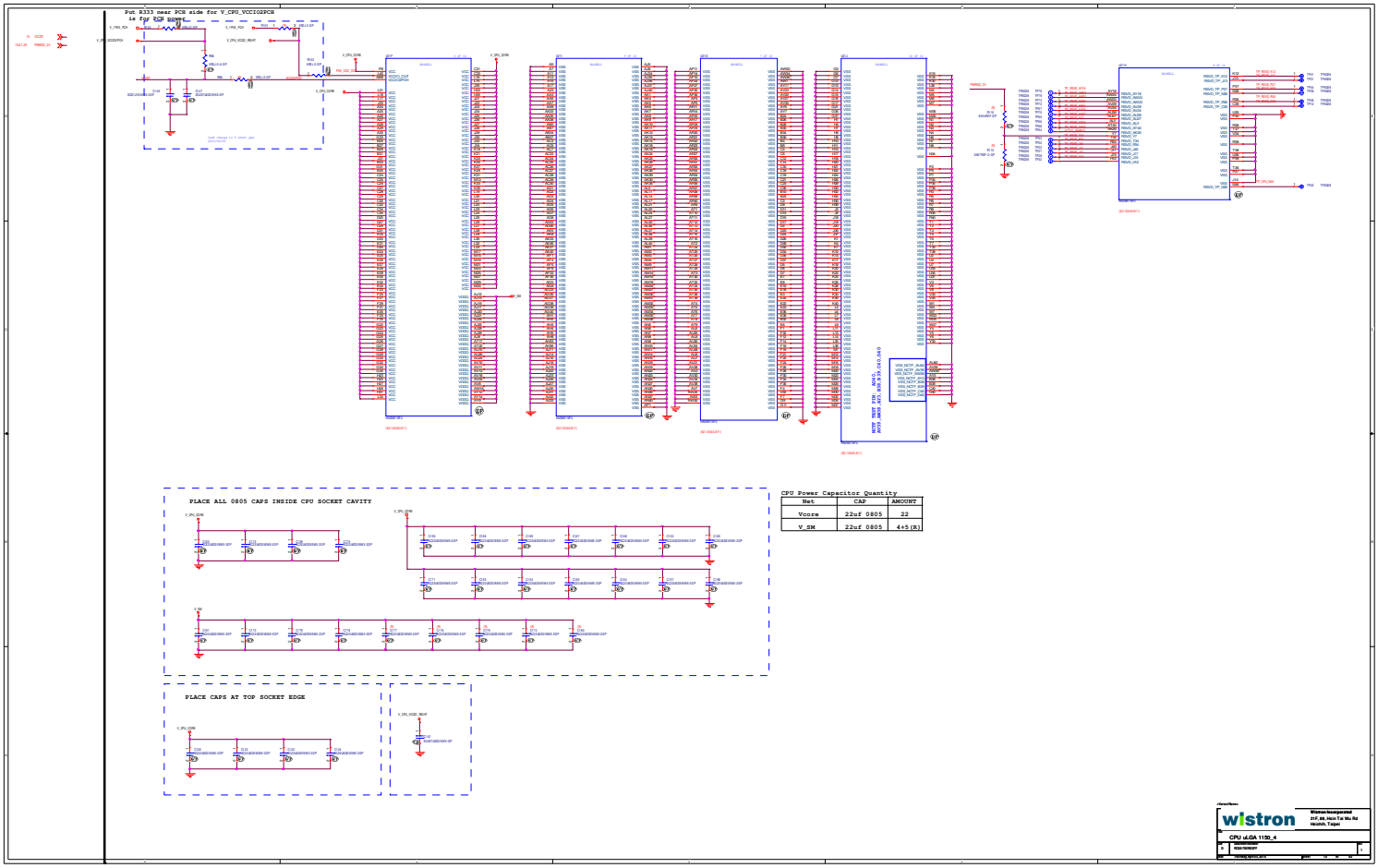
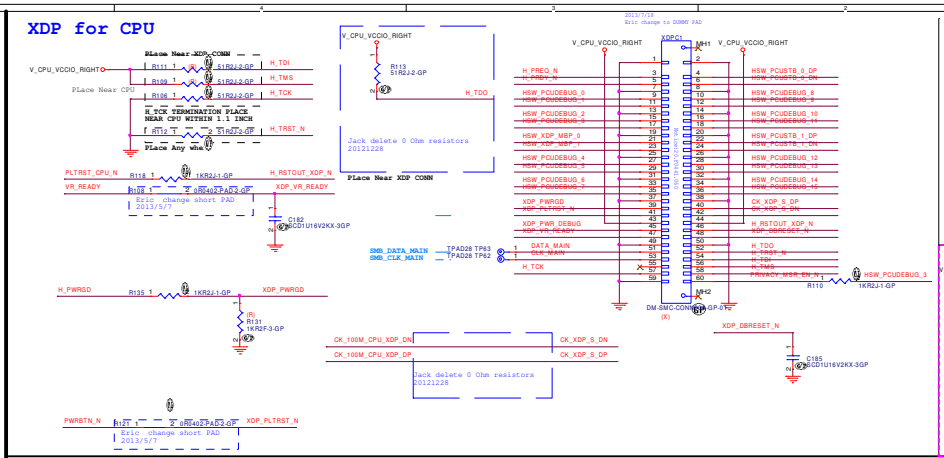


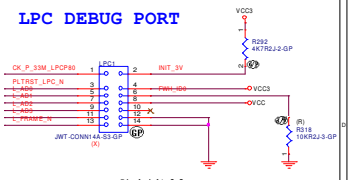
CPU Power Capacitor Quantity

Net	CAP	AMOUNT
Vcore	22uf 0805	22
V_SM	22uf 0805	4+5(R)

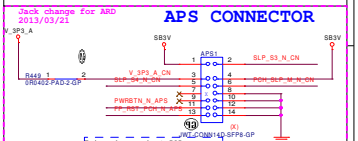
XDP for CPU



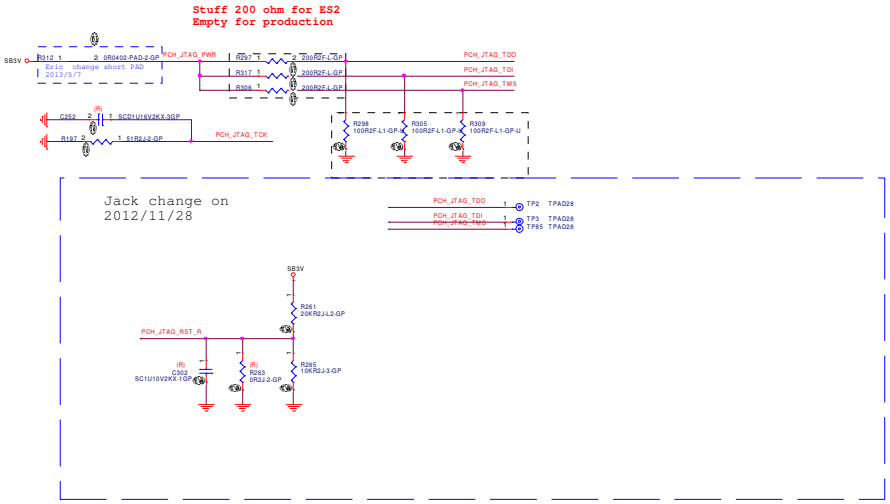
LPC DEBUG PORT



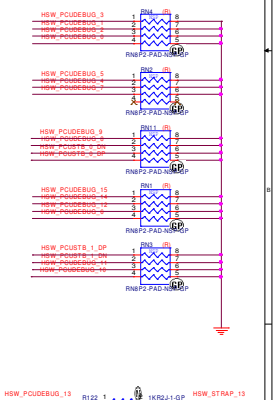
APS CONNECTOR



XDP for PCH



MCP TERMINATION



<Variant Name>

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Title: XDP/80 PORT HEADER/APS

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

Date: Thursday, April 03, 2014 Sheet 14 of 52

DDR DATA

12 M_DATA_A[0..63]
12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]

DDR CMD/ADD

12 M_MAA_A[0..15]
12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

DDR CTRL

12 M_SCS_A_N0
12 M_SCS_A_N1
12 M_SCKE_A0
12 M_SCKE_A1
12 M_ODT_A0
12 M_ODT_A1

DDR CLOCK

12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

DDR OTHERS

10 DIMM_CA_VREF_A
12 DIMM_DQ_CPU_VREF_A
12,17 DDR3_DRAMRST_N
17,39 SMB_DATA_MAIN
17,39 SMB_CLK_MAIN

DIMM1A 1 OF 3
DDR3-240P-4-GP (022.10010.0001)
Black color
Pin Height is 2.7mm

Trace: 12/12 mils

DIMM1C 3 OF 3
DDR3-240P-4-GP (022.10010.0001)
DNS must connect to GND

DIMM1B 2 OF 3
DDR3-240P-4-GP (022.10010.0001)

V_SM_VTT

CHANNEL A DIMM1

SMB ADDRESS: 000
SPD R/W: 0*A1, 0*A0

DIMM VREF DQ A (To DIMM/CPU)

R247 1KR2F-3-GP
C295 SCD1U16V2KX-3GP
R238 0R0402-PAD-2-GP
R242 1KR2F-3-GP
C271 SCD1U16V2KX-3GP
R172 2R2F-GP
C238 SCD22U16V2KX-3GP
R188 24D9R2F-L-GP
Layout NOTE: place above the DIMM side

T3 CE820U2D5VM-6-GP
C250 SC4D7U6D3V3KX-GP
C251 SCD1U16V2KX-3GP

C247 SCD1U16V2KX-3GP
C280 SCD1U16V2KX-3GP
C245 SCD1U16V2KX-3GP
C253 SCD1U16V2KX-3GP
C282 SCD1U16V2KX-3GP

Place Near Power Pin

Net	CAP	Qty
V_SM	0.1uf 0402 Y5V	5+4
V_SM_VTT	4.7uf 0603 X5R	1
V_SM_VTT	0.1uf 0402 Y5V	1

DIMM VREF CA A (To DIMM)

R234 1KR2F-3-GP
C248 SCD1U16V2KX-3GP
C342 SCD1U16V2KX-3GP
Eric add C342 2013/5/6
R235 1KR2F-3-GP
Eric del R233 2013/5/6
C270 SCD1U16V2KX-3GP
C426 SC4D7U6D3V2MX-GP-U
Eric add C426 2013/7/5

CAPS FOR DIMM

C299 SC22U6D3V5MX-2GP
C298 SC22U6D3V5MX-2GP
C297 SC22U6D3V5MX-2GP
C300 SC22U6D3V5MX-2GP

<Variant Name>

wistron
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Title: DDR3 CHA DIMM 0
Size: C
Document Number: ROSA TIGRIS SFF
Rev: 1
Date: Thursday, April 03, 2014
Sheet 15 of 52

<Variant Name>

wistron

Wistron Incorporated
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Title
TBD

Size	Document Number	Rev
A	ROSA TIGRIS SFF	1

Date: Thursday, April 03, 2014 Sheet 16 of 52

DDR DATA

12 M_DATA_B[0..63]
12 M_DQS_B_DP[0..7]
12 M_DQS_B_DN[0..7]

DDR CMD/ADD

12 M_MAA_B[0..15]
12 M_WE_B_N
12 M_CAS_B_N
12 M_RAS_B_N
12 M_SBS_B0
12 M_SBS_B1
12 M_SBS_B2

DDR CTRL

12 M_SCS_B_N0
12 M_SCS_B_N1
12 M_SCKE_B0
12 M_SCKE_B1
12 M_ODT_B0
12 M_ODT_B1

DDR CLOCK

12 CK_M_DDR0_B_DP
12 CK_M_DDR0_B_DN
12 CK_M_DDR1_B_DP
12 CK_M_DDR1_B_DN

DDR OTHERS

10 DIMM_CA_VREF_B
12 DIMM_DQ_CPU_VREF_B
12,15 DDR3_DRAMRST_N
15,39 SMB_DATA_MAIN
15,39 SMB_CLK_MAIN

DIMM2A 1 OF 3

DIMM2C 3 OF 3

DIMM2B 2 OF 3

DDR3-240P-4-GP (022.10010.0001)

Black color
Pin Height is 2.7mm

Trace: 12/12 mils

DMB must connect to GND

CHANNEL B DIMM1

SMB ADDRESS: 010
SPD R/W: 0*A5, 0*A4

DIMM VREF DQ B (To DIMM/CPU)

DIMM VREF CA B (To DIMM)

Eric Unmount R229,R229,C288 2013/5/6

Eric del R230 2013/5/6

Place Near Power Pin

Net	CAP	Qty
V_SM	0.1uf 0402 Y5V	9
V_SM	1uf 0402 X5R	5
V_SM_VTT	0.1uf 0402 Y5V	1
V_SM_VTT	4.7uf 0603 X5R	1

<Variant Name>

Wistron Incorporated
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Title: DDR3 CHB DIMM 0

Size: C | Document Number: ROSA TIGRIS SFF | Rev: 1

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<Variant Name>

wistron

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Title
TBD

Size	Document Number	Rev
A	ROSA TIGRIS SFF	1

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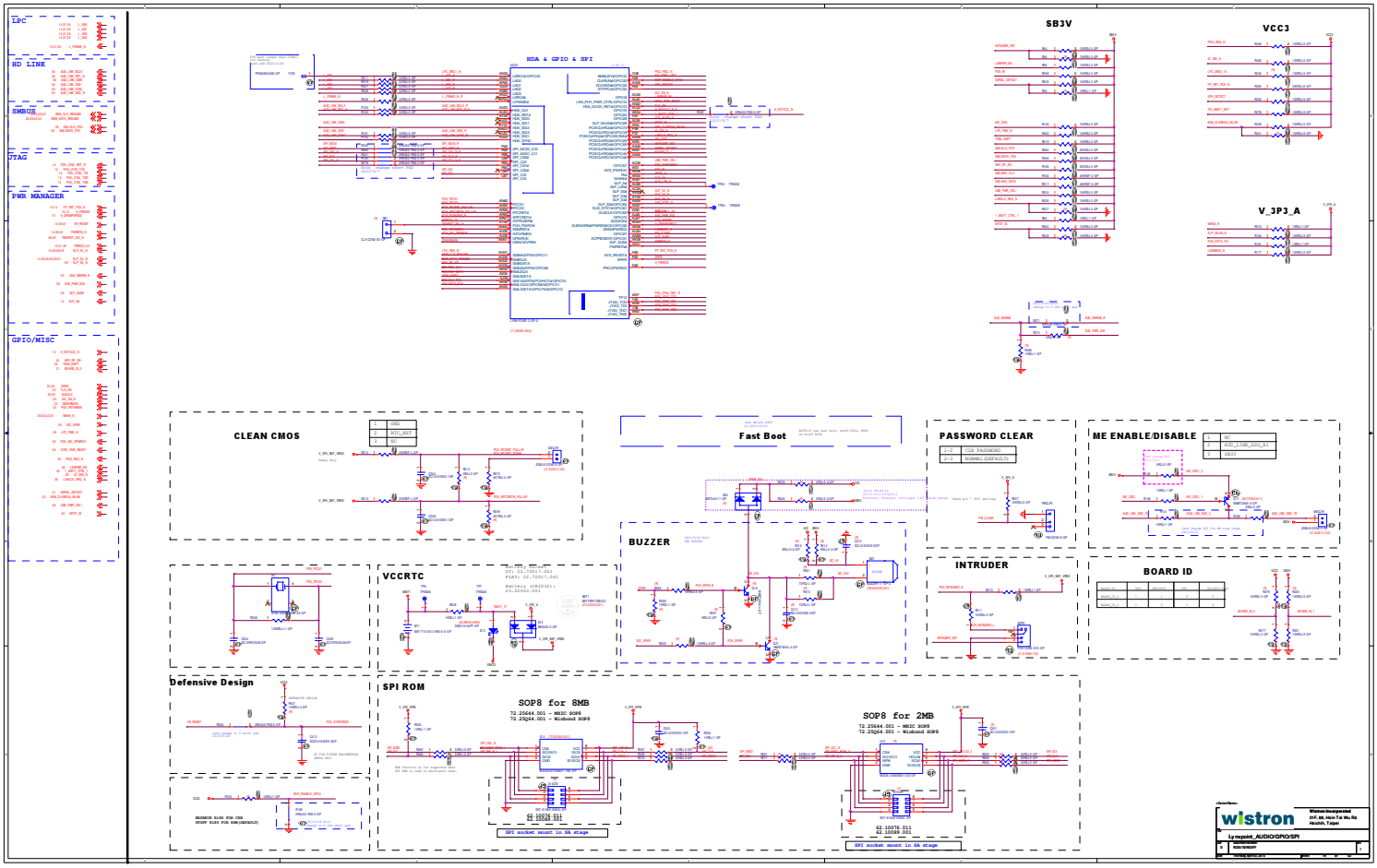

LPC
HD LINK
SMBUS
JTAG
PWR MANAGER
GPIO/MISC
HDA & GPIO & SPI
SB3V
VCC3
V_3P3_A
CLEAN CMOS
Fast Boot
PASSWORD CLEAR
ME ENABLE/DISABLE
BUZZER
INTRUDER
BOARD ID
VCCRTC
Defensive Design
SPI ROM
SOP8 for 8MB
T2.25644.001 - MXIC SOP8
T2.25J44.001 - Winbond SOP8
SOP8 for 2MB
T2.25644.001 - MXIC SOP8
T2.25J44.001 - Winbond SOP8
62.10076.011
62.10589.001
SPI socket mount in SA stage
wistron
Lynxpoint_AUDIO/GPIO/SPI

CPU CLOCK

14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP

PCI CLOCK

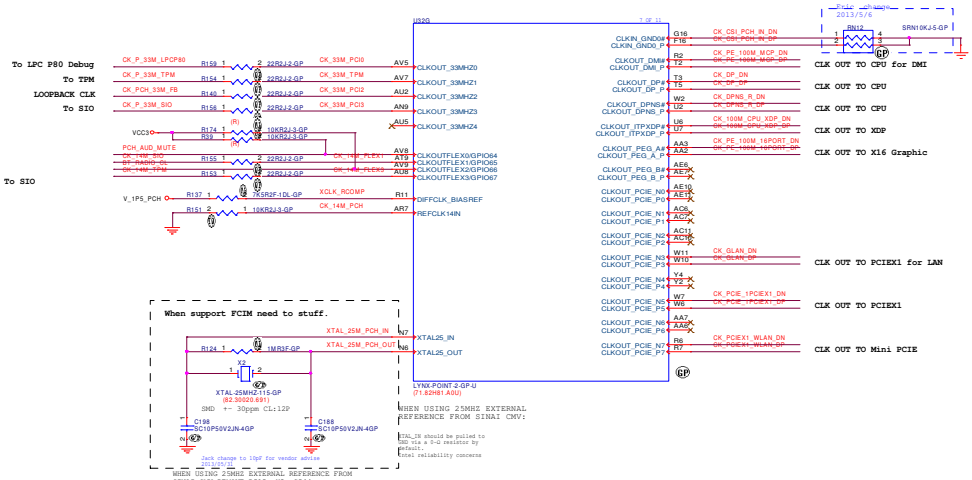
14 CK_P_33M_LPCP80
22 CK_PCH_33M_FB
39 CK_P_33M_SIO
31 CK_P_33M_TPM

PCIE CLOCK

10 CK_DPNS_R_DN
10 CK_DPNS_R_DP
10 CK_PE_100M_MCP_DN
10 CK_PE_100M_MCP_DP
11 CK_DP_DN
11 CK_DP_DP
26 CK_PE_100M_16PORT_DP
26 CK_PE_100M_16PORT_DN
35 CK_GLAN_DN
35 CK_GLAN_DP
42 CK_PCIE_1PCIEX1_DN
42 CK_PCIEX1_1PCIEX1_DP
43 CK_PCIEX1_WLAN_DN
43 CK_PCIEX1_WLAN_DP

GPIO

36 PCH_AUD_MUTE
43 BT_RADIO_CL
39 CK_14M_SIO
31 CK_14M_TPM



<Variant Name>

Wistron Incorporated
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Title: Lynxpoint_CLK

Size: C | Document Number: ROSA TIGRIS SFF | Rev: 1

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SATA5 Port (H81)

	SATA 3.0 PORT	SATA 2.0 Port
PORT0	Support	Support
PORT1	Support	Support
PORT2		Disabled
PORT3		Disabled
PORT4		Support
PORT5		Support

Pull-up on MB

DP PORT B
28 DDPB_CTRL_CLK
28 DDPB_CTRL_DATA
28 DDPB_AUX_DN
28 DDPB_AUX_DP
28 DDSP_B_HPD

VGA
27 VGA_HSYNC_3V_L
27 VGA_VSYNC_3V_L
27 VGA_RED
27 VGA_GREEN
27 VGA_BLUE
27 VGA_PCH_DDCSDA
27 VGA_PCH_DDCSCL
22,27 VGA_DET

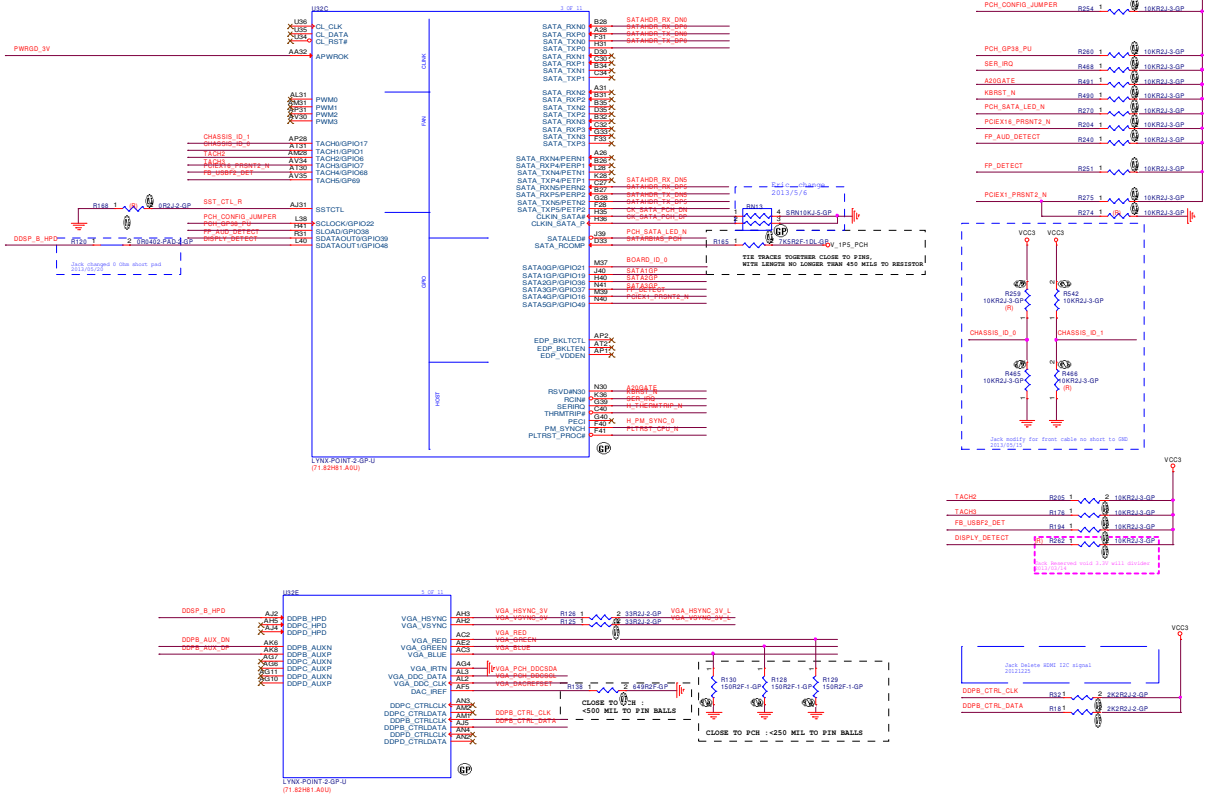
SATA
25 SATAHDR_RX_DN0
25 SATAHDR_RX_DP0
25 SATAHDR_TX_DN0
25 SATAHDR_TX_DP0
45 PCH_SATA_LED_N
25 SATAHDR_RX_DN5
25 SATAHDR_RX_DP5
25 SATAHDR_TX_DN5
25 SATAHDR_TX_DP5

mSATA

OTHERS
10 H_PM_SYNC_0
10 H_THERMTRIP_N
30 FB_USBF2_DET
13,19,39 PWRGD_3V
37 FP_AUD_DETECT
39 A20GATE
39 KBRST_N
31,39 SER_IRQ
10,14 PLTRST_CPU_N

ID
45 CHASSIS_ID_0
45 CHASSIS_ID_1
19 BOARD_ID_0

Straps
23 SATA1GP
23 SATA2GP
23 SATA3GP



<Variant Name>

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Hsichih, Taipei

Title: Lynxpoint_SATA/FAN/DP/VGA

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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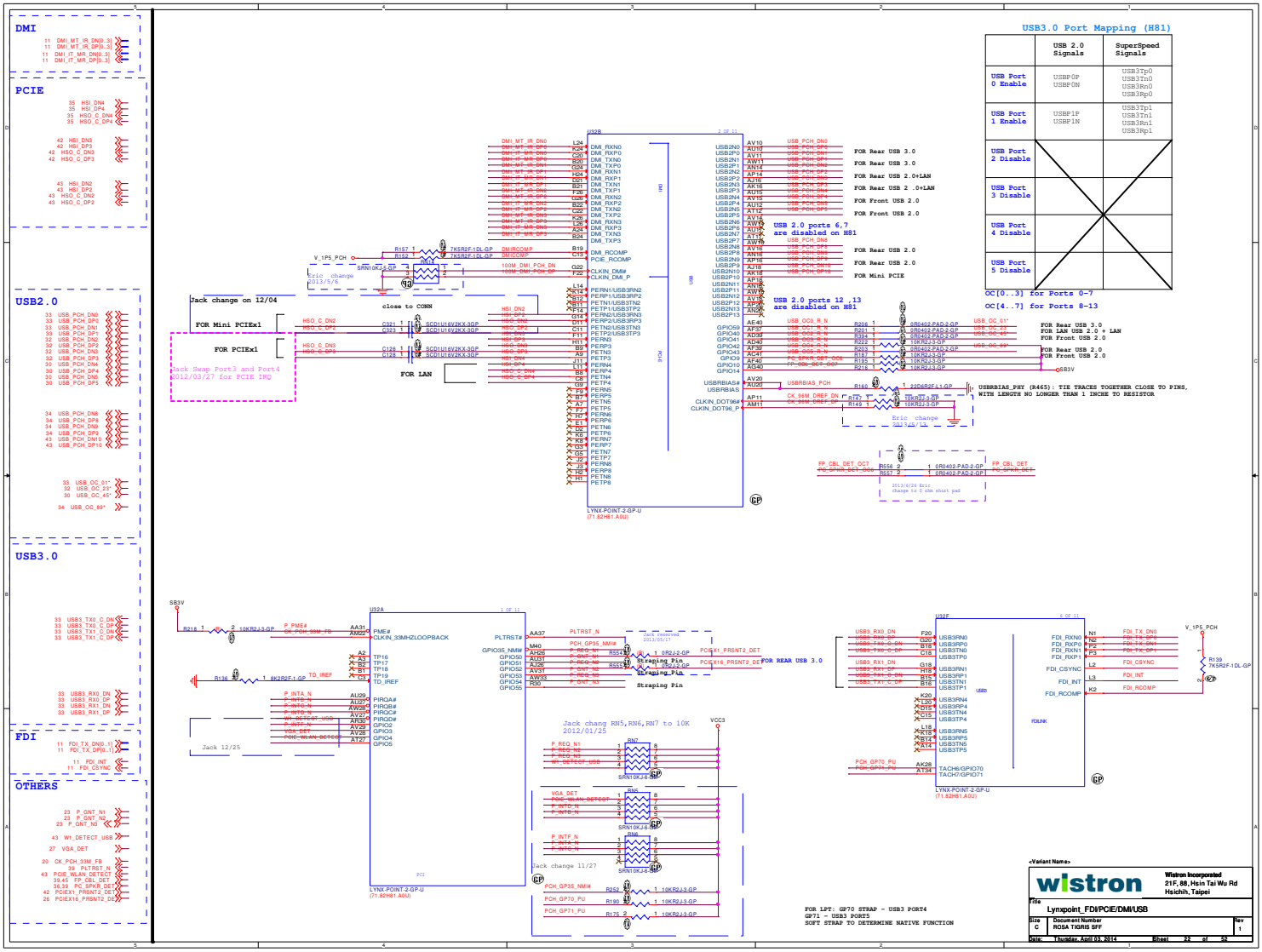
DMI
PCIE
USB2.0
USB3.0
FDI
OTHERS
USB3.0 Port Mapping (H81)
USB 2.0 Signals
SuperSpeed Signals
USB Port 0 Enable
USB Port 1 Enable
USB Port 2 Disable
USB Port 3 Disable
USB Port 4 Disable
USB Port 5 Disable
OC[0..3] for Ports 0~7
OC[4..7] for Ports 8~13
USB 2.0 ports 6,7 are disabled on H81
USB 2.0 ports 12 ,13 are disabled on H81
Jack change on 12/04
close to CONN
FOR Mini PCIEx1
FOR PCIEx1
FOR LAN
Jack Swap Port3 and Port4 2012/03/27 for PCIE IRQ
Jack change 11/27
Jack chang RN5,RN6,RN7 to 10K 2012/01/25
Straping Pin
FOR REAR USB 3.0
FOR LPT: GP70 STRAP - USB3 PORT4
GP71 - USB3 PORT5
SOFT STRAP TO DETERMINE NATIVE FUNCTION
Wistron Incorporated
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Hsichih, Taipei
Lynxpoint_FDI/PCIE/DMI/USB
Size C
Document Number ROSA TIGRIS SFF
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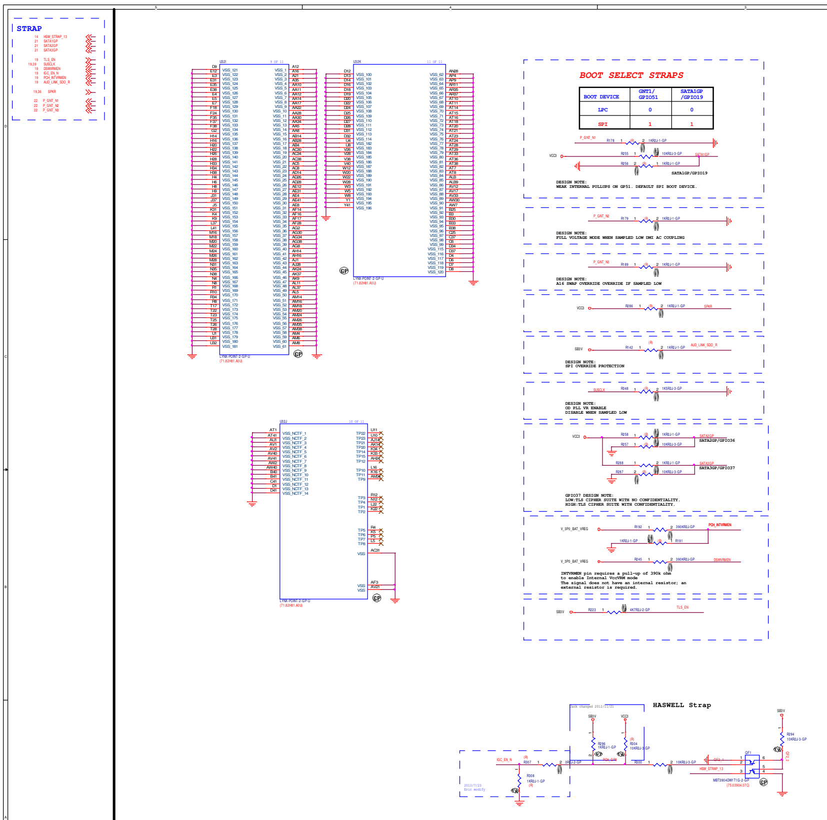

Table 2-27. Functional Strap Definitions (Sheet 1 of 4)

Signal	Usage	When Sampled	Comment
SPKR	No Reboot	Rising edge of PWROK	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: RCBA+Offset 3410h:Bit 5).
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST#	THis has a weak internal pull-up **NOTE:** The internal pull-up is disabled after RSMRST#

SATA3GP/GPIO37	TLS Confidentiality	Rising edge of PWROK pin	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality This signal has a weak internal pull-down. **NOTES:** 1. A strong pull-up may be needed for GPIO functionality 2. This signal must be pulled up to support Intel AMT with TLS. Intel ME configuration parameters also need to be set correctly to enable TLS.
DDPB_CTRLDATA	Port B Detected	Rising edge of PWROK	When '1'- Port B is detected; When '0'- Port B is not detected. This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	When '1'- Port C is detected; When '0'- Port C is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	When '1'- Port D is detected; When '0'- Port D is not detected This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	Always	If strap is sampled high, the Integrated Deep Sx Well (DSW) On-Die VR mode is enabled.
SATA2GP/GPIO36	Reserved	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTES:** 1. The internal pull-down is disabled after PLTRST# deasserts. 2. This signal should not be pulled high when strap is sampled.
GPIO8	Reserved	Rising edge of RSMRST#	This signal has a weak internal pull-up. **NOTES:** 1. The internal pull-up is disabled after RSMRST# deasserts. 2. This signal should not be pulled low when strap is sampled.

	ME Debug Mode		PLTRST# deasserts. 2. Asserting the HDA_SDO high on the rising edge of PWROK will also halt Intel® Management Engine after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug.
GPIO36	RSVD	Rising edge of PWROK	This signal has a weak internal pull-down. **NOTE:** The internal pull-down is disabled after PLTRST# deasserts.

<Variant Name>

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Title	Lynxpoint_GND/STRAPS	
Size: D	Document Number: ROSATIGRISSFF	Rev: 1
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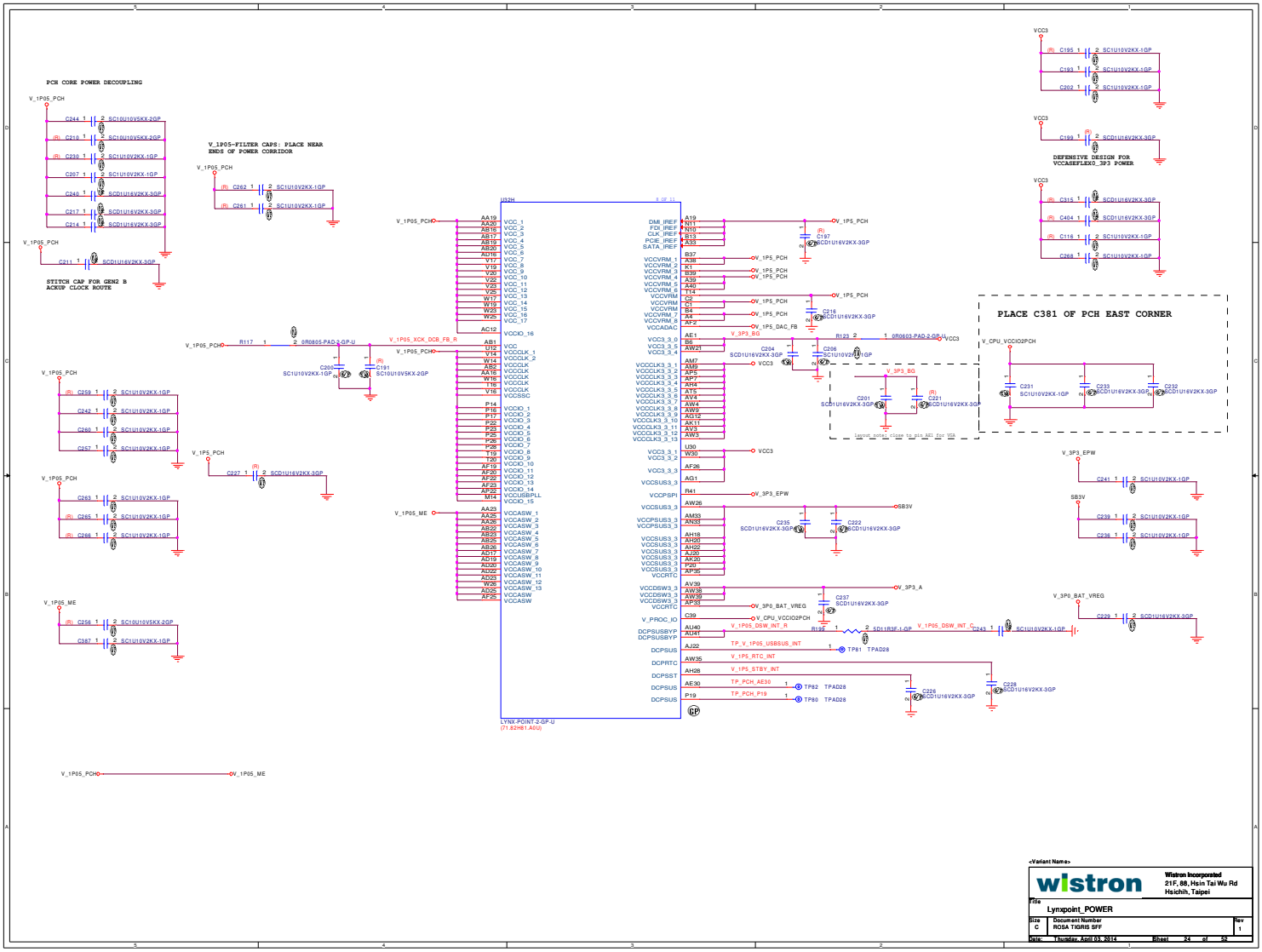
PCH CORE POWER DECOUPLING
V_1P05_PCH
C244 1 2 SC10U10V5KX-2GP
(R) C210 1 2 SC10U10V5KX-2GP
(R) C230 1 2 SC1U10V2KX-1GP
C207 1 2 SC1U10V2KX-1GP
C240 1 2 SCD1U16V2KX-3GP
C217 1 2 SCD1U16V2KX-3GP
C214 1 2 SCD1U16V2KX-3GP
C211 1 2 SCD1U16V2KX-3GP
STITCH CAP FOR GEN2 B
ACKUP CLOCK ROUTE
V_1P05-FILTER CAPS: PLACE NEAR
ENDS OF POWER CORRIDOR
(R) C262 1 2 SC1U10V2KX-1GP
(R) C261 1 2 SC1U10V2KX-1GP
R117 1 2 0R0805-PAD-2-GP-U
C200 SC1U10V2KX-1GP
(R) C191 SC10U10V5KX-2GP
V_1P05_XCK_DCB_FB_R
(R) C259 1 2 SC1U10V2KX-1GP
C242 1 2 SC1U10V2KX-1GP
C260 1 2 SC1U10V2KX-1GP
C257 1 2 SC1U10V2KX-1GP
C263 1 2 SC1U10V2KX-1GP
(R) C265 1 2 SC1U10V2KX-1GP
(R) C266 1 2 SC1U10V2KX-1GP
(R) C227 1 2 SCD1U16V2KX-3GP
(R) C256 1 2 SC10U10V5KX-2GP
C267 1 2 SC1U10V2KX-1GP
V_1P05_ME
V_1P05_PCH
V_1P05_ME
U32H
9 OF 11
LYNX-POINT-2-GP-U
(71.82H81.A0U)
VCC3
(R) C195 1 2 SC1U10V2KX-1GP
C193 1 2 SC1U10V2KX-1GP
C202 1 2 SC1U10V2KX-1GP
C199 1 2 SCD1U16V2KX-3GP
DEFENSIVE DESIGN FOR
VCCASEPLEXO_3P3 POWER
(R) C315 1 2 SCD1U16V2KX-3GP
(R) C404 1 2 SCD1U16V2KX-3GP
(R) C116 1 2 SC1U10V2KX-1GP
C268 1 2 SC1U10V2KX-1GP
C197 SCD1U16V2KX-3GP
C216 SCD1U16V2KX-3GP
C204 SCD1U16V2KX-3GP
C206 SC1U10V2KX-1GP
R123 2 1 0R0603-PAD-2-GP-U
C201 SCD1U16V2KX-3GP
(R) C221 SCD1U16V2KX-3GP
layout note: place to pin AE1 for VGA
PLACE C381 OF PCH EAST CORNER
V_CPU_VCCIO1PCH
C231 SC1U10V2KX-1GP
C233 SCD1U16V2KX-3GP
C232 SCD1U16V2KX-3GP
V_3P3_EPW
C241 1 2 SC1U10V2KX-1GP
SB3V
C239 1 2 SC1U10V2KX-1GP
C236 1 2 SC1U10V2KX-1GP
C235 SCD1U16V2KX-3GP
C222 SCD1U16V2KX-3GP
C237 SCD1U16V2KX-3GP
R199 1 2 5D1IR3F-1-GP
V_1P05_DSW_INT_C
C243 1 SC1U10V2KX-1GP
V_3P0_BAT_VREG
C229 1 2 SCD1U16V2KX-3GP
TP_V_1P05_USBSUS_INT
TP81 TPAD28
V_1P5_RTC_INT
V_1P5_STBY_INT
TP_PCH_AE30
TP82 TPAD28
TP_PCH_P19
TP80 TPAD28
C226 SCD1U16V2KX-3GP
C228 SCD1U16V2KX-3GP
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
Lynxpoint_POWER
Size C
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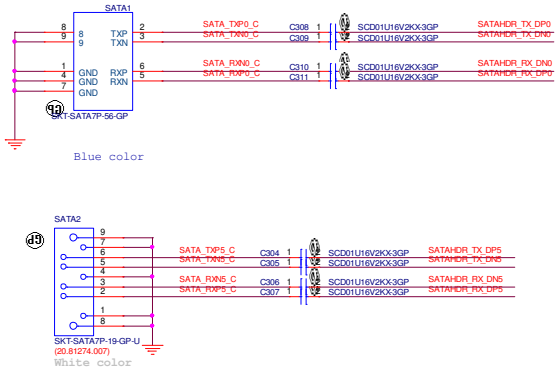
SATA

21 SATAHDR_RX_DP0
21 SATAHDR_RX_DN0

21 SATAHDR_TX_DN0
21 SATAHDR_TX_DP0

21 SATAHDR_RX_DP5
21 SATAHDR_RX_DN5

21 SATAHDR_TX_DN5
21 SATAHDR_TX_DP5



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	SATA Port	
Size: B	Document Number: ROSA TIGRIS SFF	Rev: 1
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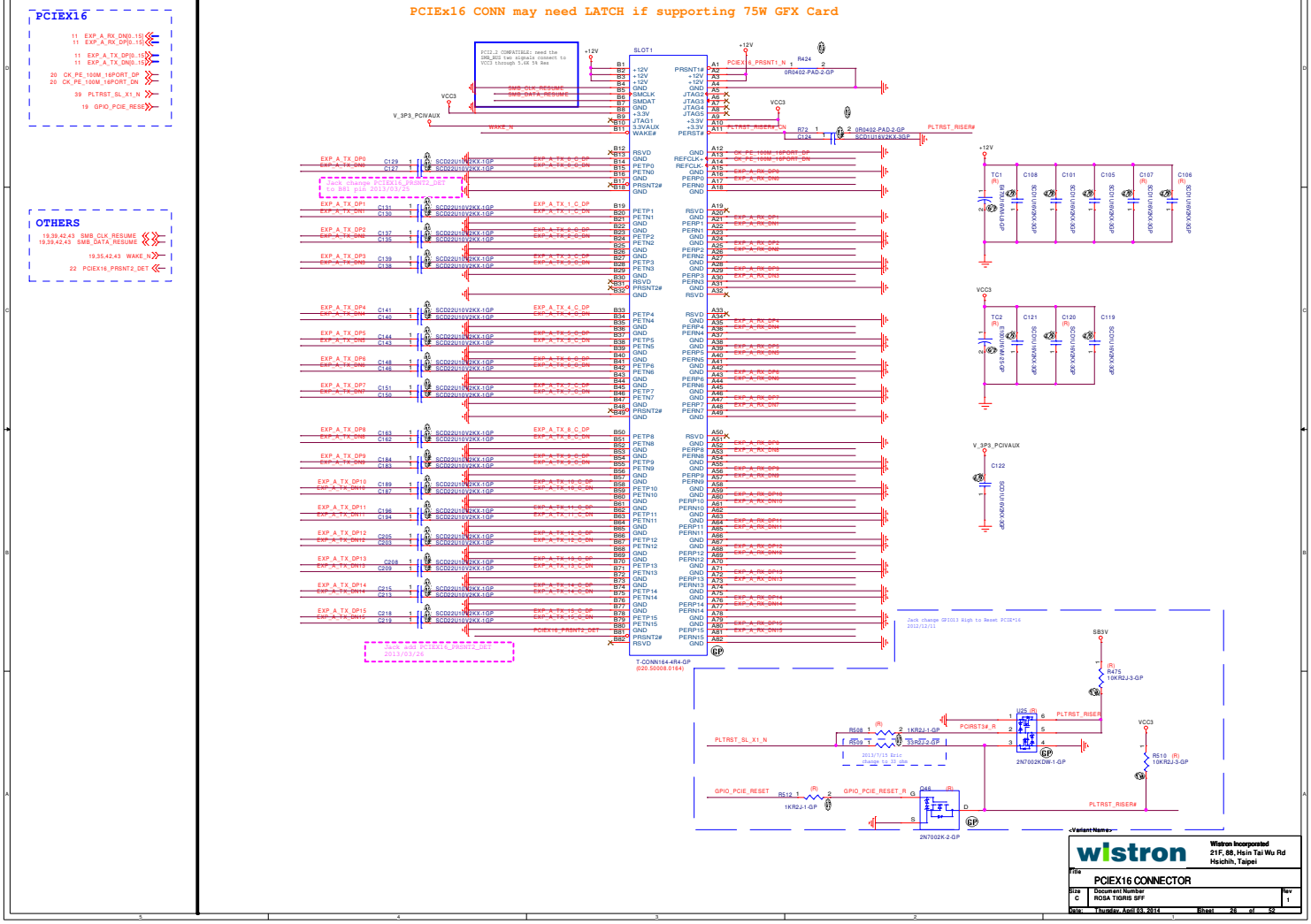
w/o Latch: 20.50352.164
with Latch: 20.50356.164

PCIEx16 CONN may need LATCH if supporting 75W GFX Card



Wistron Incorporated
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Hsichih, Taipei

Title: PCIEX16 CONNECTOR

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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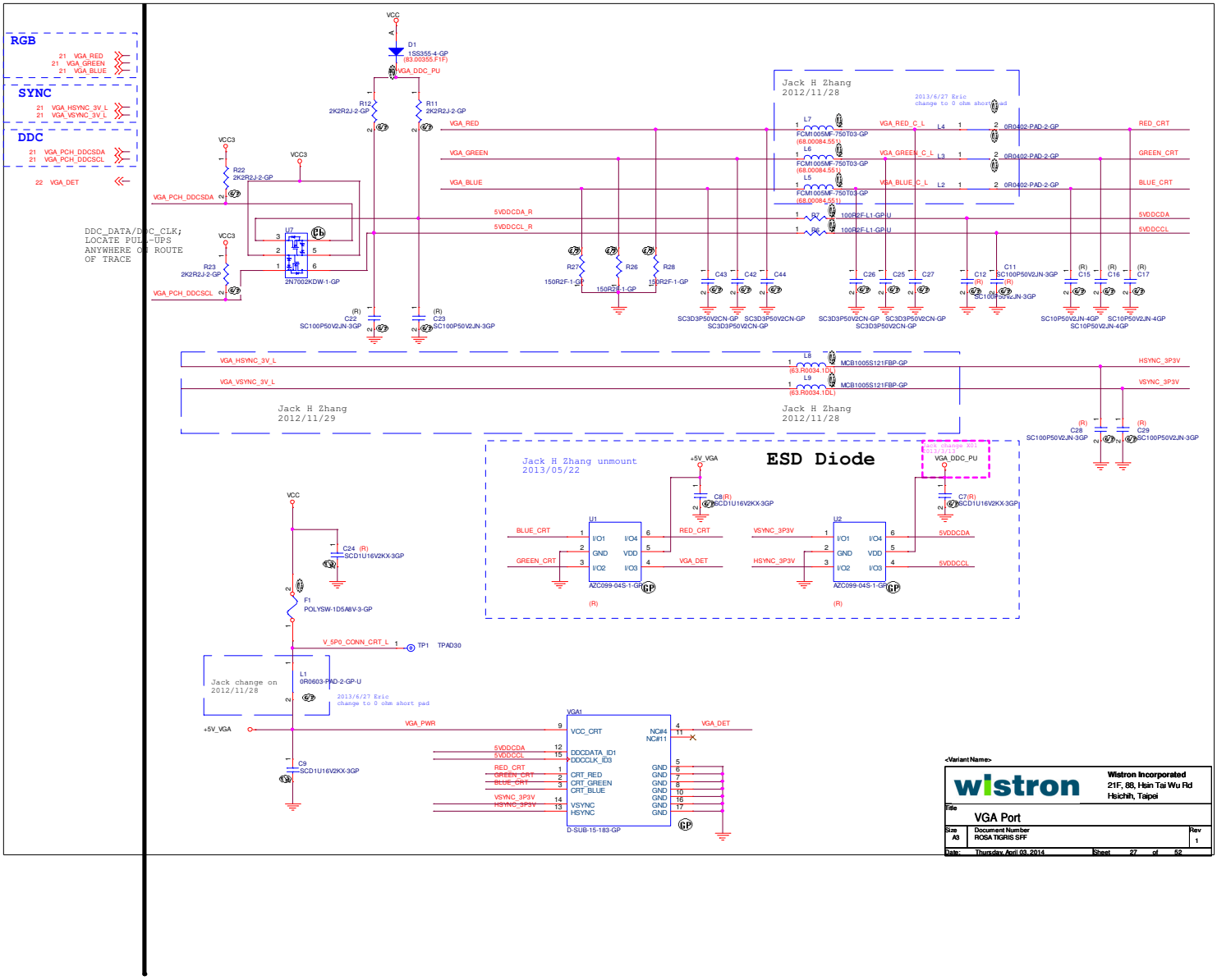
RGB
21 VGA_RED
21 VGA_GREEN
21 VGA_BLUE
SYNC
21 VGA_HSYNC_3V_L
21 VGA_VSYNC_3V_L
DDC
21 VGA_PCH_DDCSDA
21 VGA_PCH_DDCSCL
22 VGA_DET
DDC_DATA/DDC_CLK;
LOCATE PULL-UPS
ANYWHERE ON ROUTE
OF TRACE
VCC
D1
1SS355-4-GP
(83.00355.F1F)
VGA_DDC_PU
R12
2K2R2J-2-GP
R11
2K2R2J-2-GP
VGA_RED
VGA_GREEN
VGA_BLUE
VCC3
R22
2K2R2J-2-GP
VGA_PCH_DDCSDA
U7
2N7002KDW-1-GP
R23
2K2R2J-2-GP
VGA_PCH_DDCSCL
C22
SC100P50V2JN-3GP
C23
SC100P50V2JN-3GP
Jack H Zhang
2012/11/28
2013/6/27 Eric
change to 0 ohm short pad
L7
FCM1005MF-750T03-GP
(68.00084.55)
L6
FCM1005MF-750T03-GP
(68.00084.55)
L5
FCM1005MF-750T03-GP
(68.00084.55)
VGA_RED_C_L
VGA_GREEN_C_L
VGA_BLUE_C_L
L4
L3
L2
0R0402-PAD-2-GP
RED_CRT
GREEN_CRT
BLUE_CRT
5VDDCDA_R
5VDDCCL_R
R4
R5
100R2F-L1-GP-U
5VDDCDA
5VDDCCL
R27
R26
R28
150R2F-1-GP
C43
C42
C44
SC3D3P50V2CN-GP
C26
C25
C27
C12
C11
SC100P50V2JN-3GP
C15
C16
C17
SC10P50V2JN-4GP
VGA_HSYNC_3V_L
VGA_VSYNC_3V_L
L8
L9
MCB1005S121FBP-GP
(63.R0034.1DL)
HSYNC_3P3V
VSYNC_3P3V
C28
C29
SC100P50V2JN-3GP
Jack H Zhang
2012/11/29
Jack H Zhang
2012/11/28
Jack H Zhang unmount
2013/05/22
ESD Diode
+5V_VGA
C8(R)
SCD1U16V2KX-3GP
U1
U2
BLUE_CRT
GREEN_CRT
RED_CRT
VGA_DET
VSYNC_3P3V
HSYNC_3P3V
5VDDCDA
5VDDCCL
I/O1
I/O2
I/O3
I/O4
GND
VDD
AZC099-04S-1-GP
C24 (R)
SCD1U16V2KX-3GP
F1
POLYSW-1D5/8V-3-GP
V_5P0_CONN_CRT_L
TP1
TP/AD30
L1
0R0603-PAD-2-GP-U
Jack change on
2012/11/28
2013/6/27 Eric
change to 0 ohm short pad
+5V_VGA
VGA_PWR
C9
SCD1U16V2KX-3GP
VGA1
VCC_CRT
DDCDATA_ID1
DDCCLK_ID3
CRT_RED
CRT_GREEN
CRT_BLUE
VSYNC
HSYNC
NC#4
NC#11
GND
D-SUB-15-183-GP
C7(R)
SCD1U16V2KX-3GP
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
VGA Port
Size
A3
Document Number
ROSA TIGRIS SFF
Rev
1
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Display Port

11 DDSP_B_TX_DP_0
11 DDSP_B_TX_DN_0
11 DDSP_B_TX_DP_1
11 DDSP_B_TX_DN_1
11 DDSP_B_TX_DP_2
11 DDSP_B_TX_DN_2
11 DDSP_B_TX_DP_3
11 DDSP_B_TX_DN_3
21 DDPB_CTRL_CLK
21 DDPB_CTRL_DATA
21 DDSP_B_HPD
21 DDPB_AUX_DP
21 DDPB_AUX_DN

Place all CAP near DP Connector

DDSP_B_TX_DP_0 — C34 — SCD1U16V2KX-3GP — DDSP_B_TX_DP_0_C
DDSP_B_TX_DN_0 — C35 — SCD1U16V2KX-3GP — DDSP_B_TX_DN_0_C
DDSP_B_TX_DP_1 — C36 — SCD1U16V2KX-3GP — DDSP_B_TX_DP_1_C
DDSP_B_TX_DN_1 — C37 — SCD1U16V2KX-3GP — DDSP_B_TX_DN_1_C
DDSP_B_TX_DP_2 — C38 — SCD1U16V2KX-3GP — DDSP_B_TX_DP_2_C
DDSP_B_TX_DN_2 — C39 — SCD1U16V2KX-3GP — DDSP_B_TX_DN_2_C
DDSP_B_TX_DP_3 — C40 — SCD1U16V2KX-3GP — DDSP_B_TX_DP_3_C
DDSP_B_TX_DN_3 — C41 — SCD1U16V2KX-3GP — DDSP_B_TX_DN_3_C
DDPB_AUX_DN — C61 — SCD1U16V2KX-3GP — DDPB_AUX_DN_C
DDPB_AUX_DP — C62 — SCD1U16V2KX-3GP — DDPB_AUX_DP_C

VCC — R16 (R) 100KR2J-1-GP — Q1 2N7002K-2-GP — DDSP_B_HPD — DDSP_B_HPD_CONN
PLACE NEAR CONNECTOR PIN
R37 100KR2J-1-GP

Jack H Zhang change
2012/11/28

VCC — R10 (R) 1KR2J-1-GP — HDMI_DEVICE_DETECT
+12V — R36 10KR2J-3-GP — HDMI_Q64_PINS
DP_Dongle_DET — R35 4K7R2J-2-GP
R9 1MR2J-1-GP
C60 SC470P50V2KX-3GP (R)
Q7 MBT3904DW1T1G-2-GP (75.03904.07C) — Q64_PIN2 — DP_DEVICE_DETECT
+12V — R25 20KR2J-L2-GP — R24 15KR2F-GP — R34 4K99R2F-L-GP

VCC3 — R14 100KR2J-1-GP — DDSP_1_AUX_DN_C — DP_DEVICE_DETECT — DDPB_AUX_DP_C
Q5 2N7002KDW-1-GP — DDPB_AUX_DN_C — DP_DEVICE_DETECT — DDSP_1_AUX_DP_C
R13 100KR2J-1-GP

DDSP_1_AUX_DN_C — HDMI_DEVICE_DETECT — DDSP_1_AUX_DP_C
Q6 2N7002KDW-1-GP — DDPB_CTRL_DATA — HDMI_DEVICE_DETECT — DDPB_CTRL_CLK

DP connector

Impedance 85 ohm

VCC3 — 30mil 500mA (Max.) — F2 POLYSW-1D5A6V-3-GP — R8 1MR2J-1-GP — DP_PWR
C20 (R) SC470P50V2KX-3GP — C19 SCD1U16V2KX-3GP

DP1
DDSP_B_TX_DP_0_C — ML_LANE0P — SHELL1 — X1
DDSP_B_TX_DN_0_C — GND — SHELL2 — X2
DDSP_B_TX_DP_1_C — ML_LANE0N
DDSP_B_TX_DN_1_C — ML_LANE1P
DDSP_B_TX_DP_2_C — GND
DDSP_B_TX_DN_2_C — ML_LANE1N
DDSP_B_TX_DP_3_C — ML_LANE2P
DDSP_B_TX_DN_3_C — GND
DP_Dongle_DET — ML_LANE2N
DDSP_1_AUX_DP_C — ML_LANE3P
DDSP_1_AUX_DN_C — GND
DDSP_B_HPD_CONN — GND
AUX_CHP
GND
AUX_CHN
HP_DETECT
RETURN — SHELL3 — X3
DP_PWR — SHELL4 — X4
DISPLAYPORT-1-GP
(022.10008.0011)

Jack H Zhang unmount
2013/05/22

ESD Diodes

J4 AZ1045-04F-R7G-GP (R)
DDSP_1_AUX_DN_C — DDSP_1_AUX_DP_C — DDSP_B_HPD_CONN — DP_Dongle_DET
LINE_1 LINE_2 GND LINE_3 LINE_4 NC#10 NC#9 GND NC#7 NC#6

J3 AZ1045-04F-R7G-GP (R)
DDSP_B_TX_DP_2_C — DDSP_B_TX_DN_2_C — DDSP_B_TX_DP_3_C — DDSP_B_TX_DN_3_C

J5 AZ1045-04F-R7G-GP (R)
DDSP_B_TX_DP_0_C — DDSP_B_TX_DN_0_C — DDSP_B_TX_DP_1_C — DDSP_B_TX_DN_1_C

<Variant Name>

wistron — Wistron Incorporated, 21F, 88, Hsin Tai Wu Rd, Hsichih, Taipei

Title: HDMI Port
Size: C — Document Number: ROSA TIGRIS SFF — Rev: 1
Date: Thursday, April 03, 2014 — Sheet 28 of 52

Jack Delete HDMI
20121225

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: TBD

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FRONT USB

22 USB_OC_45*
22 USB_PCH_DP5
22 USB_PCH_DN5
22 USB_PCH_DN4
22 USB_PCH_DP4
21 FB_USBF2_DET

FRONT_USB_PORT

Eric F74F10 co-lay
2013/5/7

5VDUAL_USB_RO — F10 POLYSW-1DS48V-3-GP — USBVCC45

R391 10KR2J-3-GP

USB_OC_45* — C348 SC1KP50V2KX-1GP — R392 15KR2F-GP — C349 SCD1U16V2KX-3GP — TC4 E220U16VM-L8-GP

Jack H Zhang change
2012/11/27

EMI

USB_PCH_DN5 / USB_PCH_DP5 — LR12 MCM1012B900FBP-GP-U (68.01012.20B) — USB_EXT_DN5 / USB_EXT_DP5

Jack H Zhang delete
2013/1/11

Jack H Zhang delete
2013/1/11

USB_PCH_DN4 / USB_PCH_DP4 — LR11 MCM1012B900FBP-GP-U (68.01012.20B) — USB_EXT_DN4 / USB_EXT_DP4

Jack H Zhang delete
2013/1/11

UU4 AZC099-04S-1-GP

USB_EXT_DN5 — I/O1 — I/O4 — USB_EXT_DP5
USBVCC45 — VDD
GND
USB_EXT_DP4 — I/O2 — I/O3 — USB_EXT_DN4

UC11 SCD1U16V2KX-3GP

USBF2

USBVCC45 — 1
USB_EXT_DN4 — 3
USB_EXT_DP4 — 5
7
9

2 — USB_EXT_DN5
4 — USB_EXT_DP5
6
8
10 — Down

UP

DVD-CONN10A-SB-GP (21.62735.205) — FB_USBF2_DET

Green

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: FRONT USB20 HEADER

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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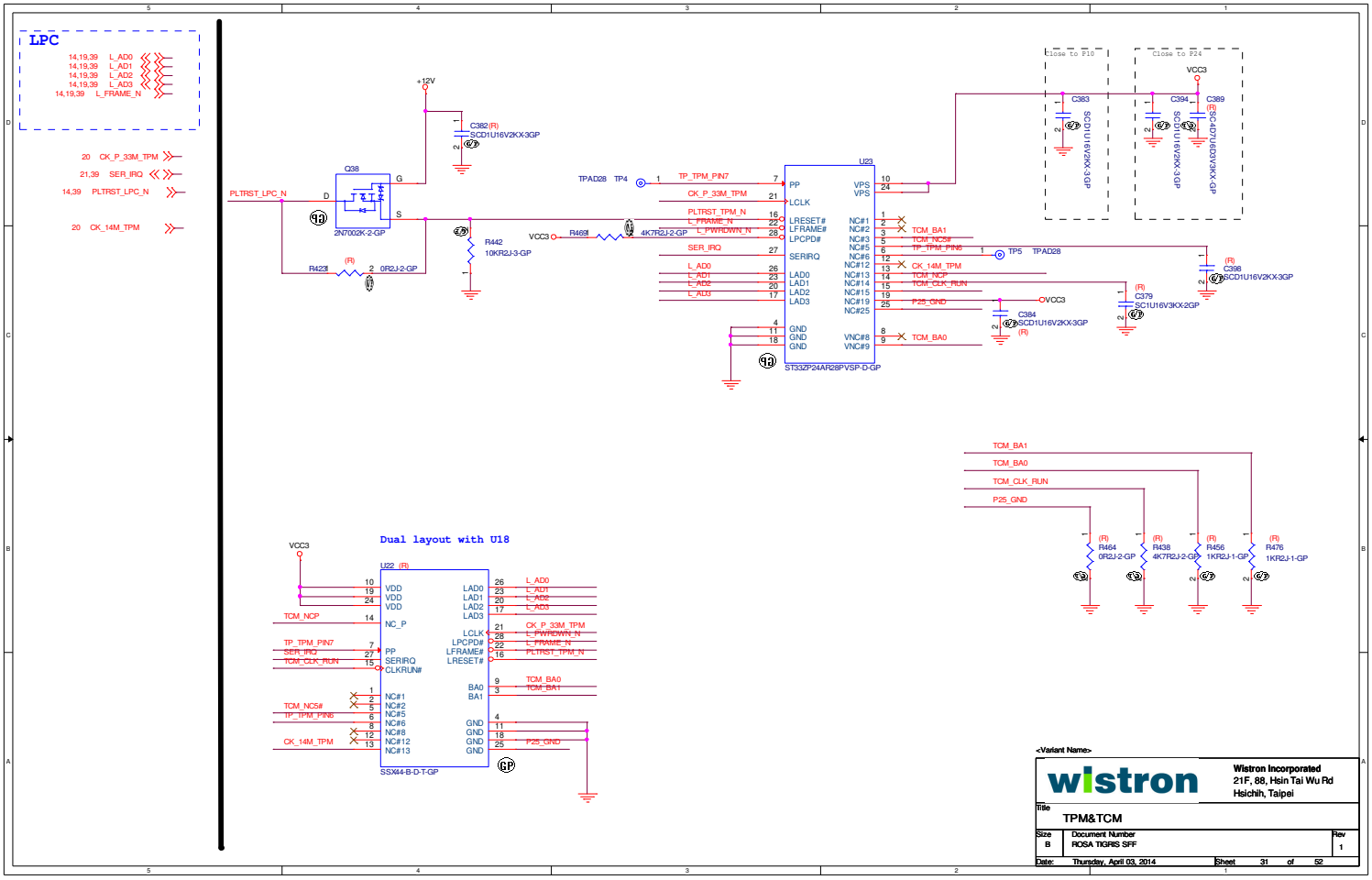
LPC
14,19,39 L_AD0
14,19,39 L_AD1
14,19,39 L_AD2
14,19,39 L_AD3
14,19,39 L_FRAME_N
20 CK_P_33M_TPM
21,39 SER_IRQ
14,39 PLTRST_LPC_N
20 CK_14M_TPM
+12V
C382 (R) SCD1U16V2KX-3GP
Q38
2N7002K-2-GP
PLTRST_LPC_N
R423 (R) 0R2J-2-GP
R442 10KR2J-3-GP
R469 4K7R2J-2-GP
VCC3
TPAD28 TP4
TP_TPM_PIN7
CK_P_33M_TPM
PLTRST_TPM_N
L_FRAME_N
L_PWRDWN_N
SER_IRQ
L_AD0
L_AD1
L_AD2
L_AD3
U23
PP
LCLK
LRESET#
LFRAME#
LPCPD#
SERIRQ
LAD0
LAD1
LAD2
LAD3
VPS
GND
NC#1
NC#2
NC#3
NC#5
NC#6
NC#12
NC#13
NC#14
NC#15
NC#19
NC#25
VNC#8
VNC#9
TCM_BA1
TCM_NC5#
TP_TPM_PIN6
TP5 TPAD28
CK_14M_TPM
TCM_NCP
TCM_CLK_RUN
P25_GND
TCM_BA0
ST33ZP24AR28PVSP-D-GP
Close to P10
Close to P24
C383 SCD1U16V2KX-3GP
C394 SCD1U16V2KX-3GP
C389 (R) SCD1U16V2KX-3GP
C398 (R) SCD1U16V2KX-3GP
C379 (R) SC1U16V3KX-2GP
C384 SCD1U16V2KX-3GP (R)
TCM_BA1
TCM_BA0
TCM_CLK_RUN
P25_GND
R464 (R) 0R2J-2-GP
R438 (R) 4K7R2J-2-GP
R456 (R) 1KR2J-1-GP
R476 (R) 1KR2J-1-GP
Dual layout with U18
U22 (R)
VDD
NC_P
LAD0
LAD1
LAD2
LAD3
LCLK
LPCPD#
LFRAME#
LRESET#
BA0
BA1
SERIRQ
CLKRUN#
NC#1
NC#2
NC#5
NC#6
NC#8
NC#12
NC#13
GND
SSX44-B-D-T-GP
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
TPM&TCM
Size B
Document Number
ROSA TIGRIS SFF
Rev 1
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REAR USB

22 USB_PCH_DP2
22 USB_PCH_DN2
22 USB_PCH_DN3
22 USB_PCH_DP3
22 USB_OC_23*

RJ45

35 LAN_MDI2_DP
35 LAN_MDI2_DN
35 LAN_MDI1_DP
35 LAN_MDI1_DN
35 LAN_MDI0_DP
35 LAN_MDI0_DN
35 LAN_MDI3_DP
35 LAN_MDI3_DN
35 SPEED_100_N
35 SPEED_1000_N
35 LINK_ACTIVITY_N

REAR USB+LAN

Eric F6&F9 co-lay 2013/5/7

5VDUAL_USB_RO
F9 POLYSW-1DS48V-3-GP
UR8 10KR2J-3-GP
UR9 15KR2F-GP
UC9 SC1KP50V2KX-1GP
UTC3 E220U16VM-L8-GP
UC10 SCD1U16V2KX-3GP
USBVCC23
USB_OC_23*

Jack H Zhang change 2012/11/27

U3 AZC099-04S-1-GP
USB_EXT_DN2
USB_EXT_DP3
USB_EXT_DP2
USB_EXT_DN3
USBVCC23
UC8 SCD1U16V2KX-3GP

V_3P3_LAN
U12 AZC099-04S-1-GP
LINK_ACTIVITY
SPEED_1000
SPEED_100
C73 SCD1U16V2KX-3GP

swap U16 net 2013/01/03

Jack H Zhang change U16 near LAN connector 2012/11/27

ESD Diodes

U11 AZC099-04S-1-GP (075.003V3.0071)
LAN_MDI0_DN_C
LAN_MDI0_DP_C
LAN_MDI1_DN_C
LAN_MDI1_DP_C
C83 SCD1U16V2KX-3GP

U10 AZC099-04S-1-GP (075.003V3.0070)
LAN_MDI2_DN_C
LAN_MDI2_DP_C
LAN_MDI3_DN_C
LAN_MDI3_DP_C
C84 SCD1U16V2KX-3GP

EMI

LR6 MCM1012B900FBP-GP-U (68.01012.20B)
USB_PCH_DN2
USB_PCH_DP2
USB_EXT_DN2
USB_EXT_DP2

LR5 MCM1012B900FBP-GP-U (68.01012.20B)
USB_PCH_DN3
USB_PCH_DP3
USB_EXT_DN3
USB_EXT_DP3

Jack change on 2012/11/28

EMI

LR7 MCM1012B900FBP-GP-U (66.R0036.04L)
LAN_MDI0_DN
LAN_MDI0_DP
LAN_MDI0_DN_C
LAN_MDI0_DP_C

LR8 MCM1012B900FBP-GP-U (66.R0036.04L)
LAN_MDI1_DN
LAN_MDI1_DP
LAN_MDI1_DN_C
LAN_MDI1_DP_C

LR10 MCM1012B900FBP-GP-U (66.R0036.04L)
LAN_MDI2_DN
LAN_MDI2_DP
LAN_MDI2_DN_C
LAN_MDI2_DP_C

LR9 MCM1012B900FBP-GP-U (66.R0036.04L)
LAN_MDI3_DN
LAN_MDI3_DP
LAN_MDI3_DN_C
LAN_MDI3_DP_C

USB+RJ45

LNUSB1
Orange
Green
SPEED_1000
SPEED_100
UR7 249R2F-GP
UR6 249R2F-GP
SPEED_1000_N
SPEED_100_N
USBVCC23
USB_EXT_DN2
USB_EXT_DP2
USB_EXT_DN3
USB_EXT_DP3
LAN_MDI0_DN_C
LAN_MDI0_DP_C
LAN_MDI1_DN_C
LAN_MDI1_DP_C
LAN_MDI2_DN_C
LAN_MDI2_DP_C
LAN_MDI3_DN_C
LAN_MDI3_DP_C
CHASSIS_GND
RJ45_ADT
V_3P3_LAN
LINK_ACTIVITY
UR5 330R2J-3-GP
LINK_ACTIVITY_N
SKT-RJ45-USB-9-GP

UP

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

UC5 SCD1U16V2KX-3GP

Jack H Zhang delete UC9 2013/01/02

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: USB+RJ45

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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Rear USB3.0

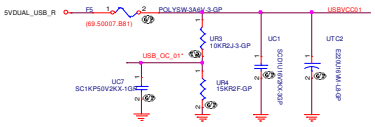
22 USB3_RX0_DN
22 USB3_RX0_DP
22 USB3_TX0_C_DN
22 USB3_TX0_C_DP

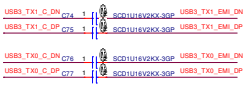
22 USB3_RX1_DN
22 USB3_RX1_DP
22 USB3_TX1_C_DN
22 USB3_TX1_C_DP

22 USB_PCH_DP0
22 USB_PCH_DN0
22 USB_PCH_DP1
22 USB_PCH_DN1

22 USB_OC_01*

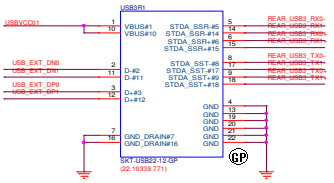
REAR USB3.0





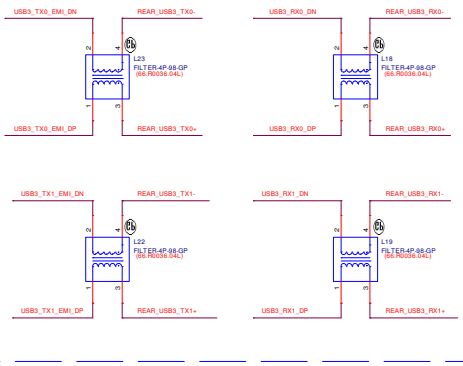
Jack H Zhang change CONN
2012/11/29

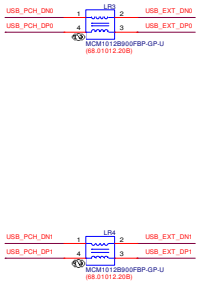
REAR USB3.0 CONN



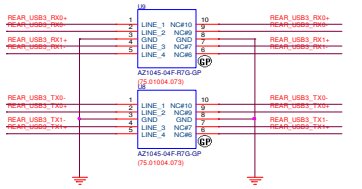
Jack H Zhang change
2012/11/28

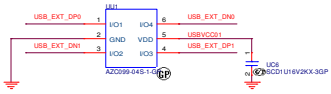
EMI





ESD Diodes





<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: REAR USB30_1

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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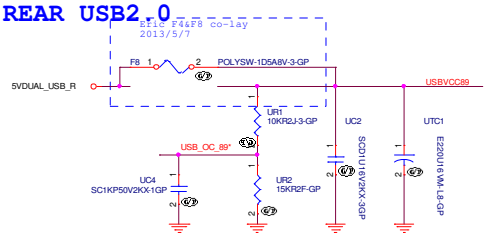
Rear USB2.0

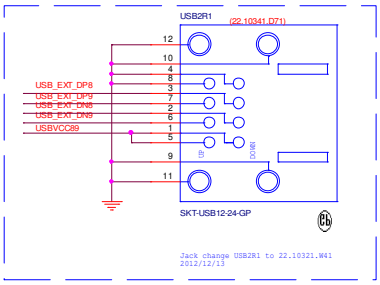
22 USB_PCH_DP8
22 USB_PCH_DN8
22 USB_PCH_DP9
22 USB_PCH_DN9

22 USB_OC_89*

REAR USB2.0

Eric F4&F8 co-lay
2013/5/7

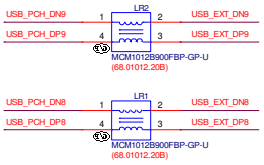




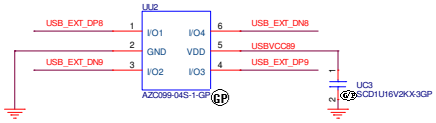
Jack change USB2R1 to 22.10321.W41
2012/12/13

Jack H Zhang change
2012/11/27

EMI



ESD Diodes



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: REAR USB20_1

Size	Document Number	Rev
B	ROSA TIGRIS SFF	1

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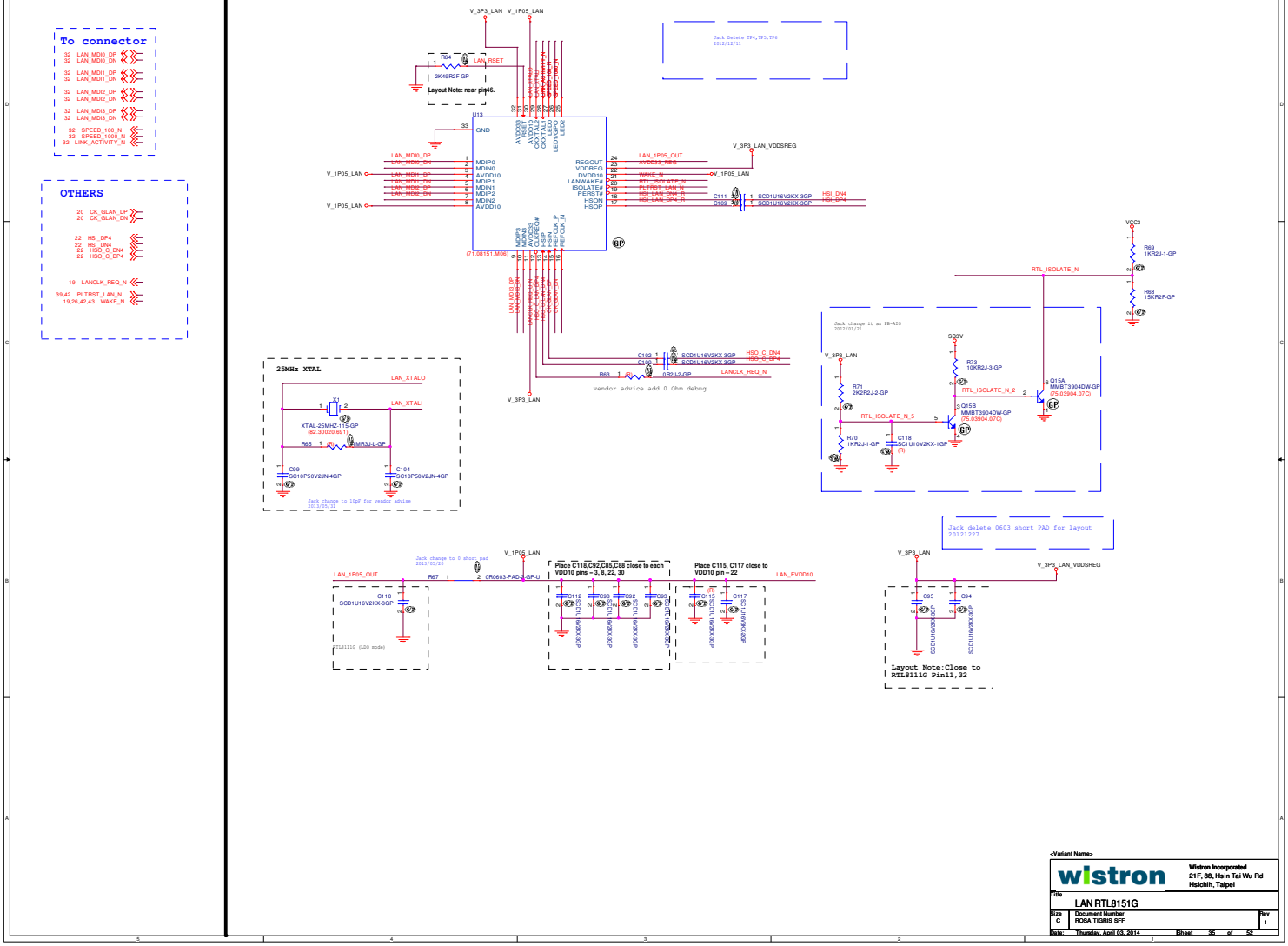

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: LAN RTL8151G

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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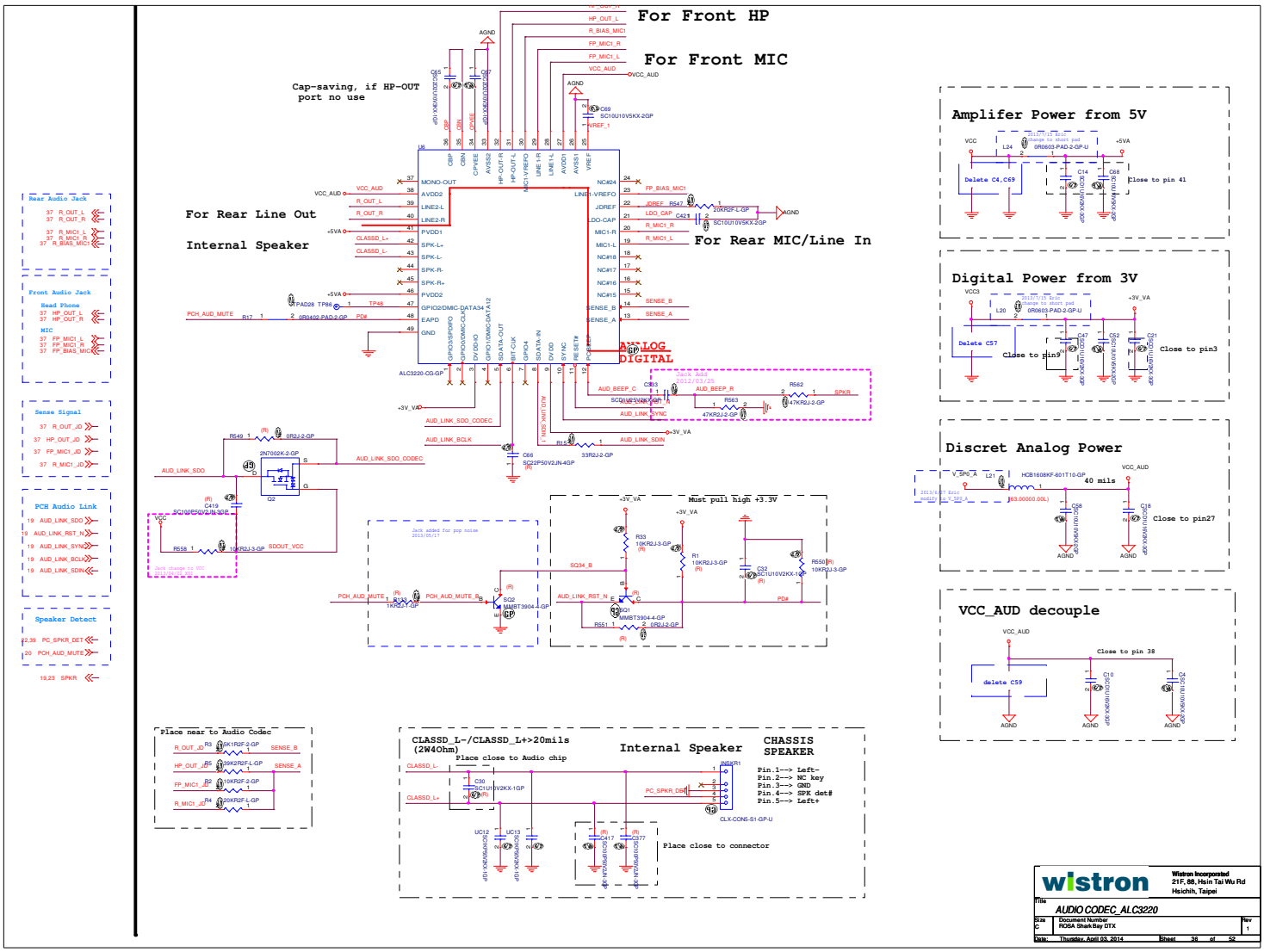

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO CODEC_ALC3220

Size: C | Document Number: ROSA Shark Bay DTX | Rev: 1

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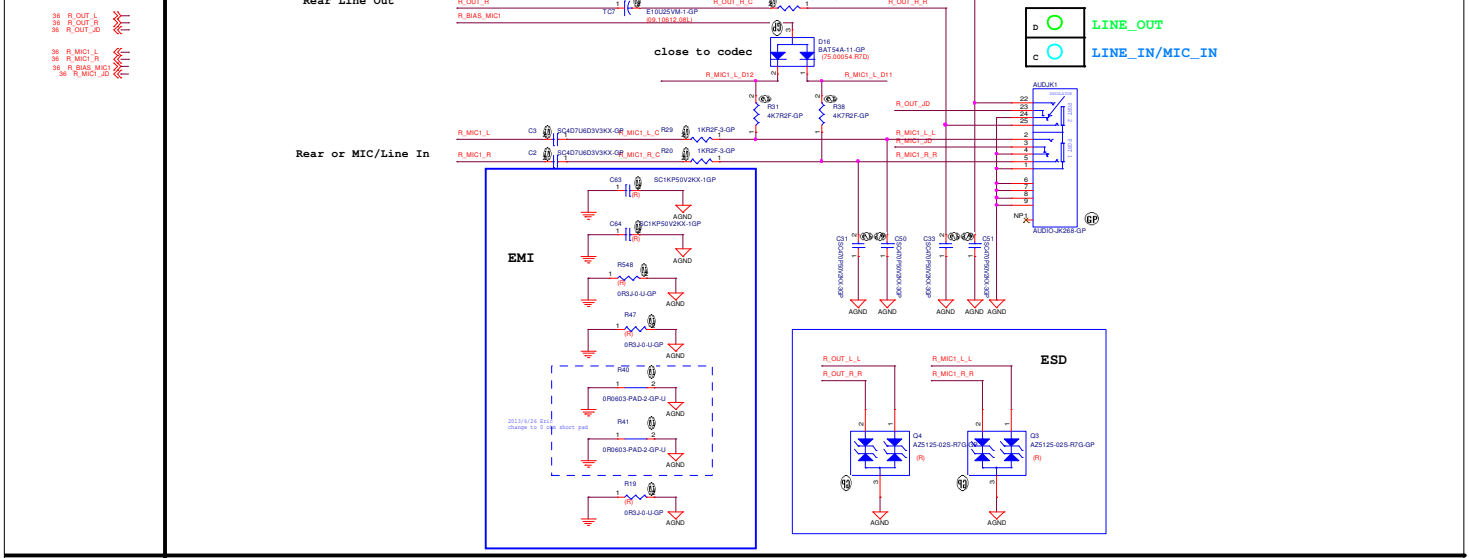
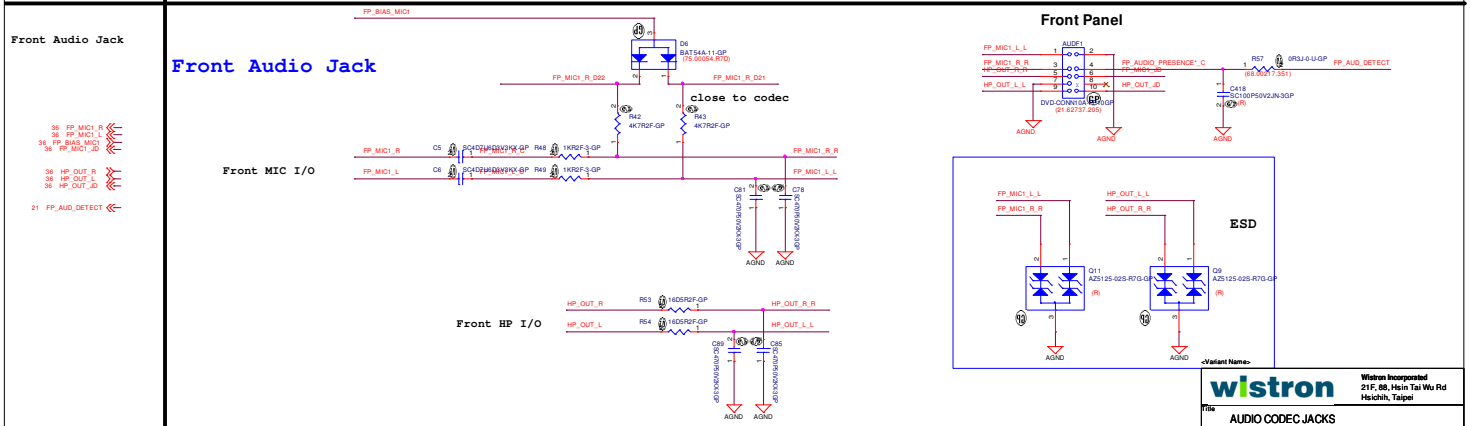
Rear Audio Jack

Rear Audio Jack



Front Audio Jack

Front Audio Jack



<variant_name>

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: AUDIO CODEC JACKS

Size: D | Document Number: RIOSA Shark Bay DTX | Rev: 1

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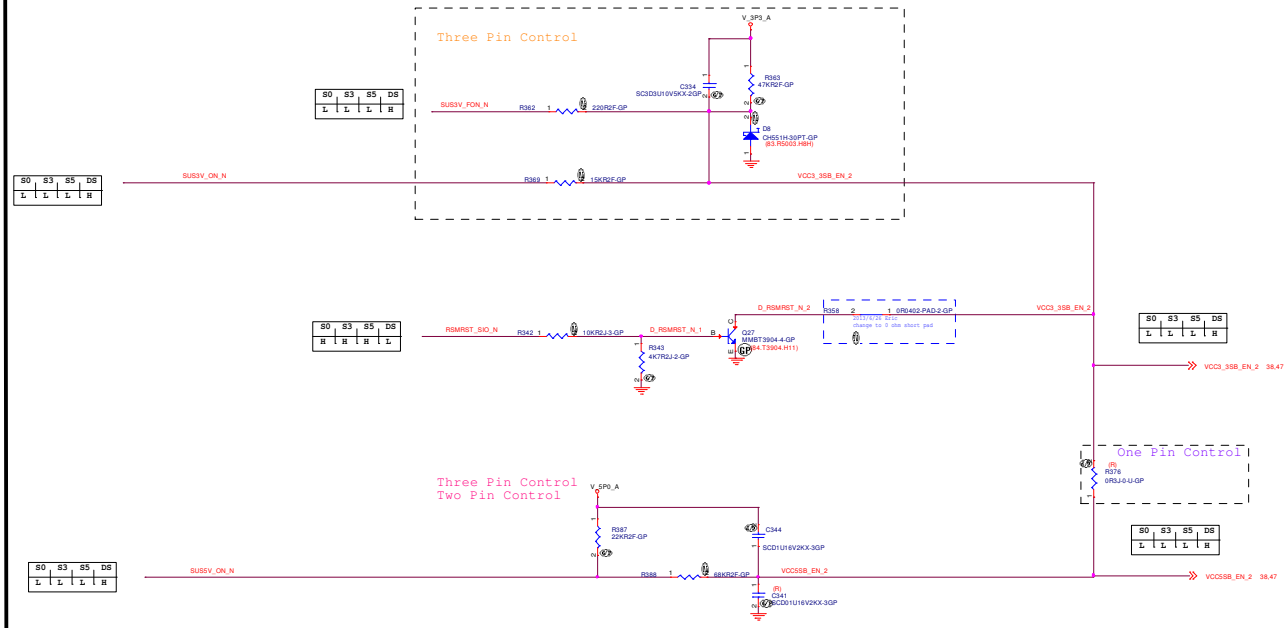
39 SUS3V_ON_N
39 SUS3V_FON_N
39 SUS5V_ON_N
38,47 VCC3_3SB_EN_2
38,47 VCCSSB_EN_2
19,39 RSMRST_SIO_N



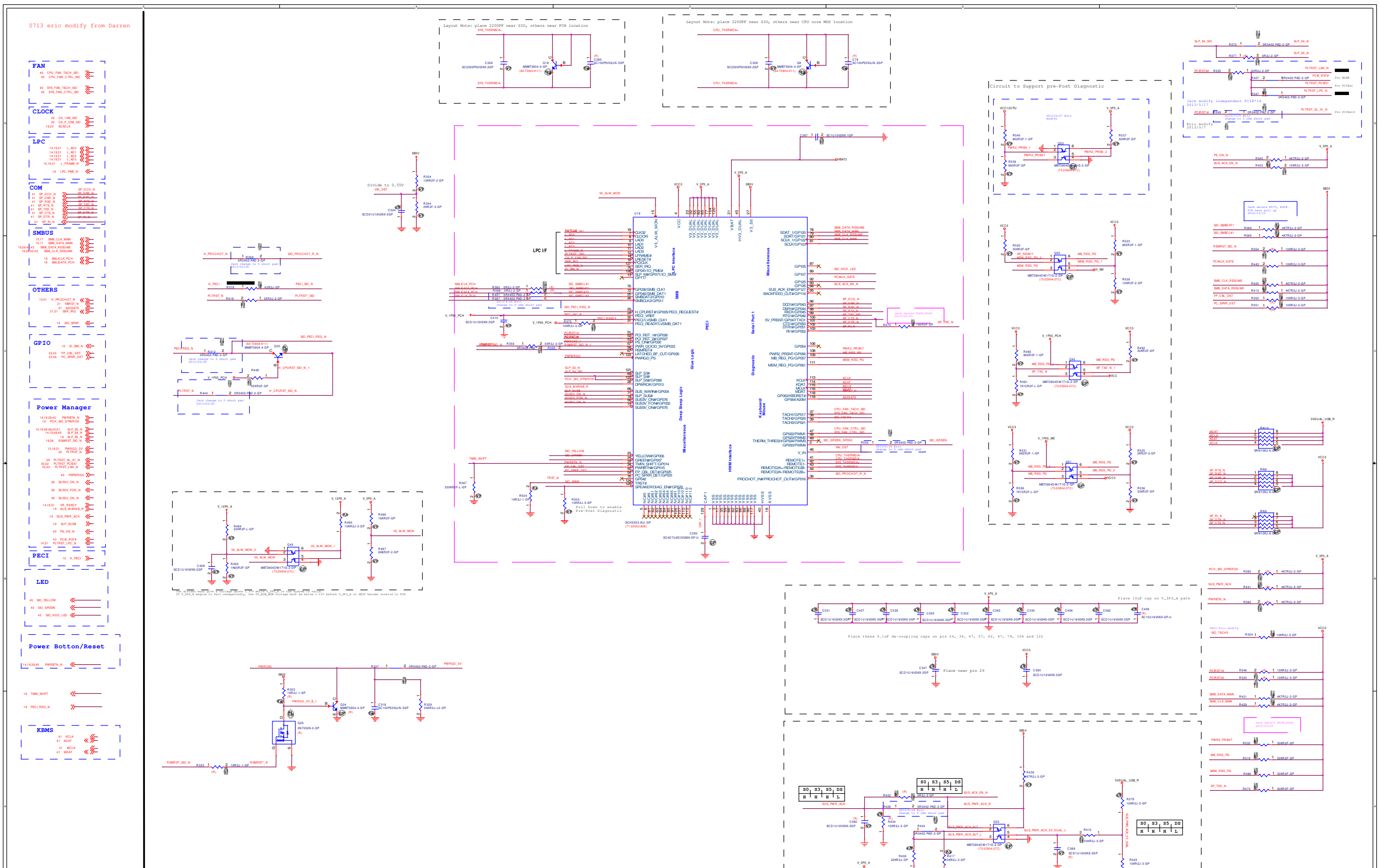
<Variant Name>

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DSW

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

Date: Thursday, April 03, 2014 Sheet 38 of 52



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wistron — Wistron Incorporated, 21F, 88, Hsin Tai Wu Rd, Hsichih, Taipei

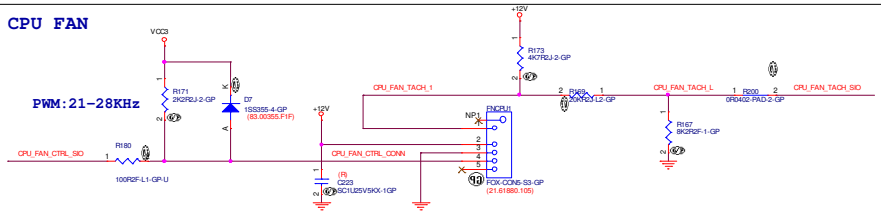
Title	SIO_SCH5555(NEW)	
Size: Custom	Document Number: ROSATIGRIS SFF	Rev: 1
Date: Thursday, April 03, 2014	Sheet 39 of 52	

SIO FAN CONTROL

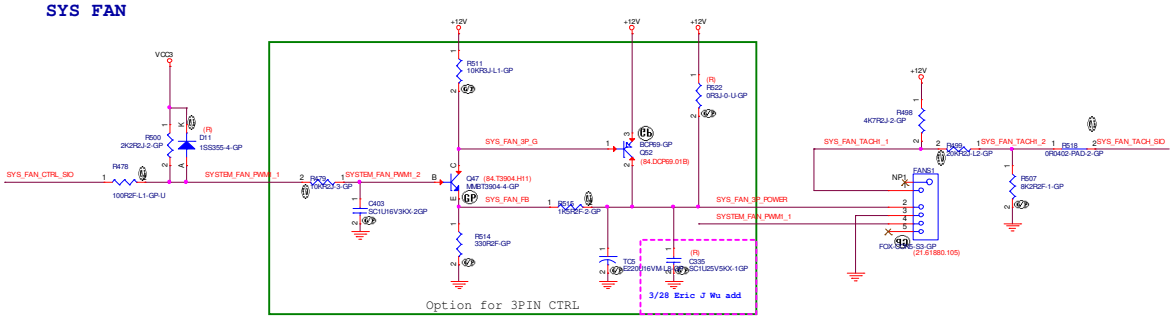
39 CPU_FAN_CTRL_SIO
39 CPU_FAN_TACH_SIO
39 SYS_FAN_CTRL_SIO
39 SYS_FAN_TACH_SIO

CPU FAN

PWM:21-28KHz

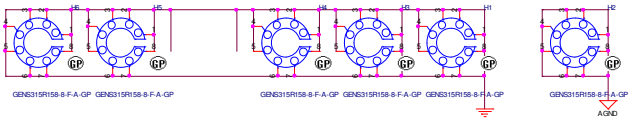


SYS FAN



PCB MOUNTING HOLES

2012/12/10
change H2 from GND to AGND



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: FAN CIRCUITS/HOLE

Size: Custom | Document Number: R05A TIGR6 SFF | Rev: 1

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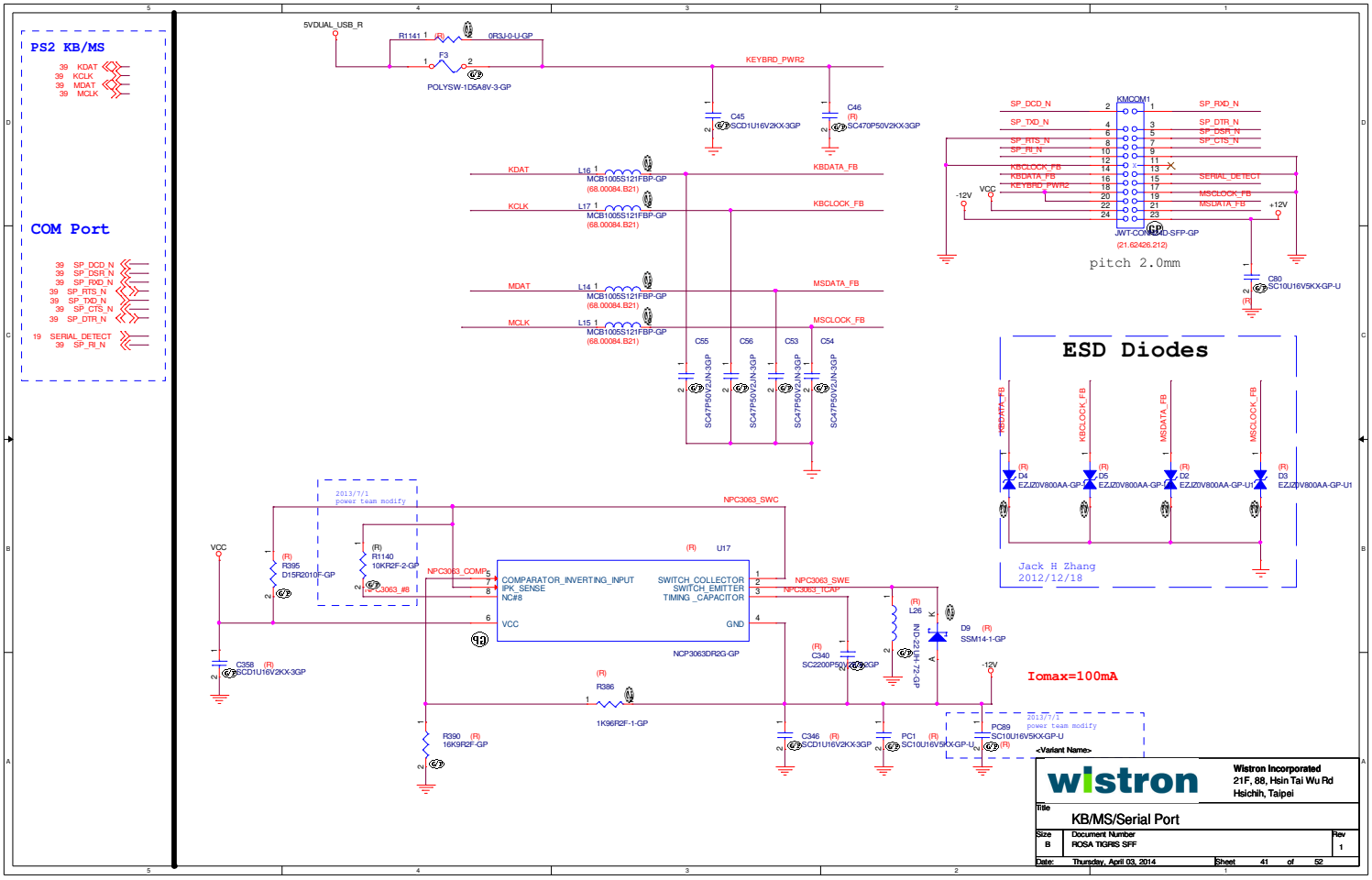
PS2 KB/MS
39 KDAT
39 KCLK
39 MDAT
39 MCLK
COM Port
39 SP_DCD_N
39 SP_DSR_N
39 SP_RXD_N
39 SP_RTS_N
39 SP_TXD_N
39 SP_CTS_N
39 SP_DTR_N
19 SERIAL_DETECT
39 SP_RI_N
5VDUAL_USB_R
R1141 0R3J-0-U-GP
F3
POLYSW-1D5A8V-3-GP
KEYBRD_PWR2
C45 SCD1U16V2KX-3GP
C46 SC470P50V2KX-3GP
KDAT
KCLK
MDAT
MCLK
L16 MCB1005S121FBP-GP (68.00084.B21)
L17 MCB1005S121FBP-GP (68.00084.B21)
L14 MCB1005S121FBP-GP (68.00084.B21)
L15 MCB1005S121FBP-GP (68.00084.B21)
KBDATA_FB
KBCLOCK_FB
MSDATA_FB
MSCLOCK_FB
C55 C56 C53 C54 SC47P50V2JN-3GP
KMCOM1
SP_DCD_N
SP_RXD_N
SP_TXD_N
SP_DTR_N
SP_DSR_N
SP_RTS_N
SP_CTS_N
SP_RI_N
KBCLOCK_FB
KBDATA_FB
KEYBRD_PWR2
SERIAL_DETECT
MSCLOCK_FB
MSDATA_FB
-12V
VCC
+12V
JWT-CONN-SD-SFP-GP
(21.62426.212)
pitch 2.0mm
C80 SC10U16V5KX-GP-U
ESD Diodes
D4 D5 D2 D3 EZJZ0V800AA-GP-U1
Jack H Zhang
2012/12/18
2013/7/1
power team modify
R395 D15R2010F-GP
R1140 10KR2F-2-GP
NPC3063_#8
NPC3063_COMP
NPC3063_SWC
U17
COMPARATOR_INVERTING_INPUT
IPK_SENSE
NC#8
VCC
SWITCH_COLLECTOR
SWITCH_EMITTER
TIMING _CAPACITOR
GND
NCP3063DR2G-GP
NPC3063_SWE
NPC3063_TCAP
L26 IND-22UH-7Z-GP
D9 SSM14-1-GP
C340 SC2200P50V2GP
C358 SCD1U16V2KX-3GP
R386 1K96R2F-1-GP
R390 16K9R2F-GP
C346 SCD1U16V2KX-3GP
PC1 SC10U16V5KX-GP-U
PC89 SC10U16V5KX-GP-U
Iomax=100mA
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
KB/MS/Serial Port
Size B
Document Number
ROSA TIGRIS SFF
Rev 1
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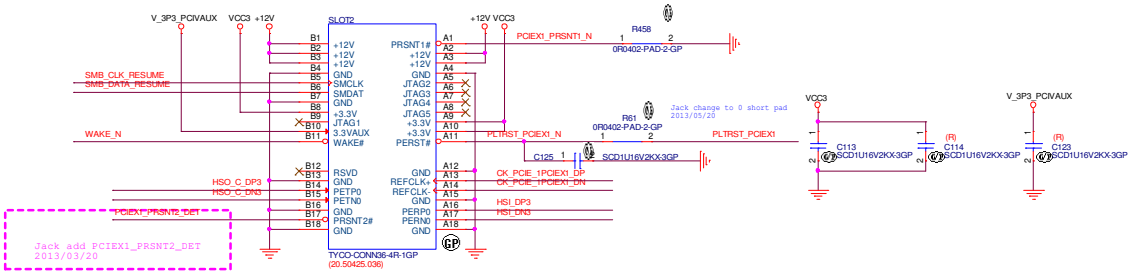
PCIEX1 CONN



PCIEX1

22	HSO_C_DP3
22	HSO_C_DN3
22	HSI_DP3
22	HSI_DN3
20	CK_PCIE_1PCIEX1_DP
20	CK_PCIE_1PCIEX1_DN

Others

35,39	PLTRST_PCIEX1
19,26,39,43	SMB_CLK_RESUME
19,26,39,43	SMB_DATA_RESUME
19,26,35,43	WAKE_N
22	PCIEX1_PRSNT2_DET

Delete mSATA circuit on X01
Jack 2013/03/14

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	PCIEX1_CONN	
Size: B	Document Number: ROSA TIGRIS SFF	Rev: 1
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Wireless Card(Present support EP/SP)

USB2.0

22 USB_PCH_DP10
22 USB_PCH_DN10

PCIEX1

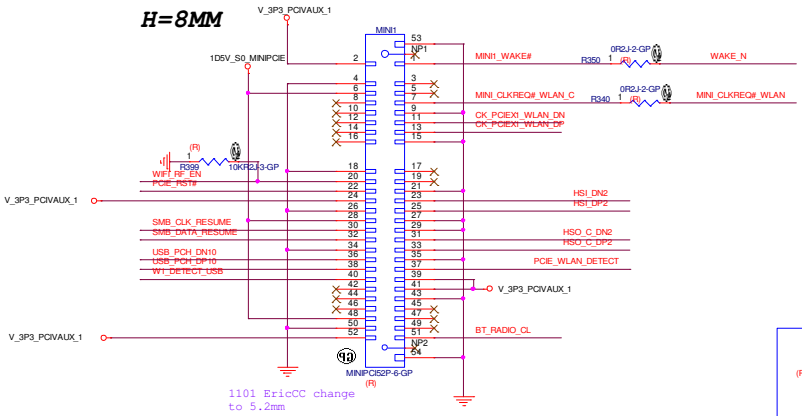
22 HSI_DN2
22 HSI_DP2
22 HSO_C_DN2
22 HSO_C_DP2

20 CK_PCIEX1_WLAN_DP
20 CK_PCIEX1_WLAN_DN

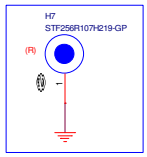
OTHERS

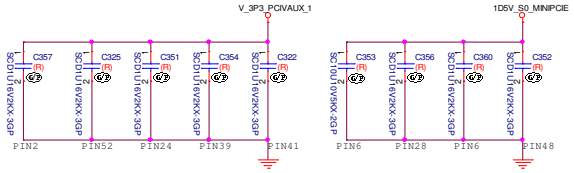
19,26,39,42 SMB_CLK_RESUME
19,26,39,42 SMB_DATA_RESUME
19,26,35,42 WAKE_N
39 PCIE_RST#
19 MINI_CLKREQ#_WLAN
19 WIFI_RF_EN
20 BT_RADIO_CL
22 W1_DETECT_USB
22 PCIE_WLAN_DETECT

H=8MM



1101 EricCC change to 5.2mm





Jack Delete one 0 Ohm resistor
2013/01/14

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title	TBD	
Size: B	Document Number: ROSA TIGRIS SFF	Rev: 1
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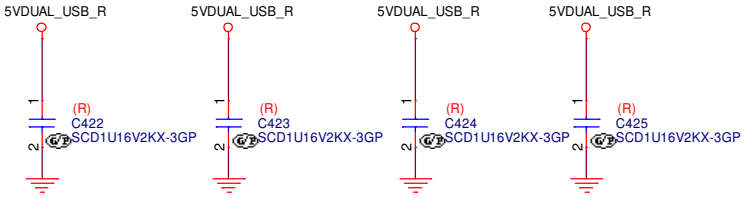

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: EMC			
Size: A	Document Number: ROSA TIGRIS SFF		Rev: 1
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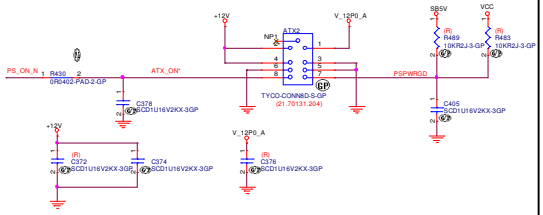
39 PS_ON_N
21 PCH_SATA_LED_N
39 PSPWRGD
14,19,39 PWRBTN_N
39 SIO_HDD_LED
39 SIO_GREEN
39 SIO_YELLOW
19 MTST_ID
21 CHASSIS_ID_0
21 CHASSIS_ID_1
22,39 FP_CBL_DET

ATX CONNECTOR

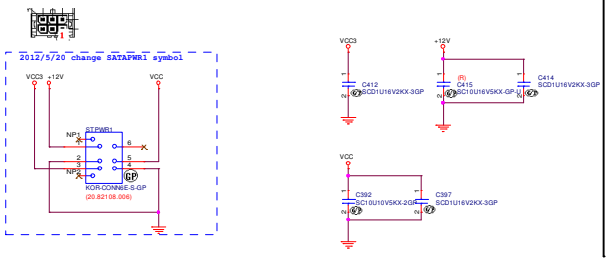
PSU

PIN 1

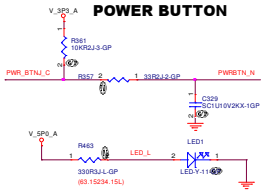
1	+12VSB	5	+12VSDC
2	COM	6	+12VSDC
3	COM	7	COM
4	P_OK	8	PS_ON



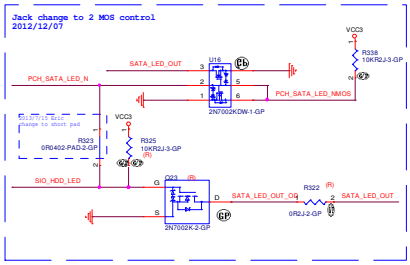
SATA POWER CONNECTOR



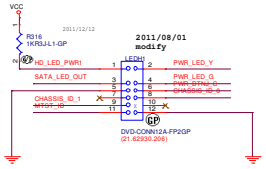
POWER BUTTON

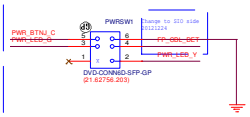


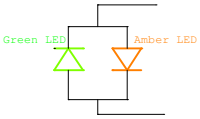
HDD LED



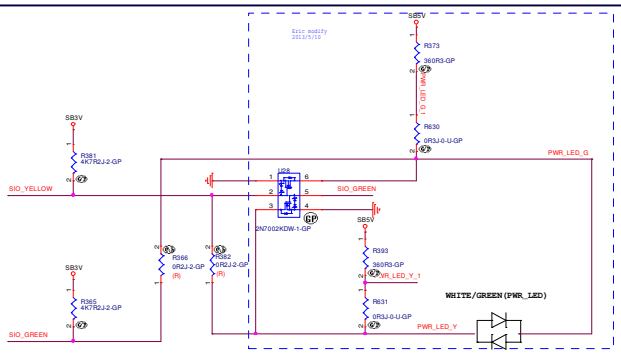
FRONT PANEL HEADER







S0	White
S3	Amber
S4	LED off
No Post	Amber
Failure to Post	Amber (blinking)



ORANGE/YELLOW (SUS_LED)

	LED_YELLOW	LED_GREEN
ORANGE (SUS_LED)	L	H
WHITE (PWR_LED)	H	L

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: PWR/FNT PNL

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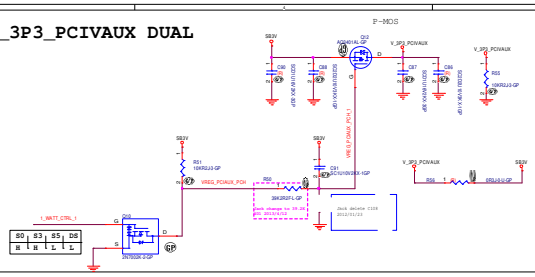
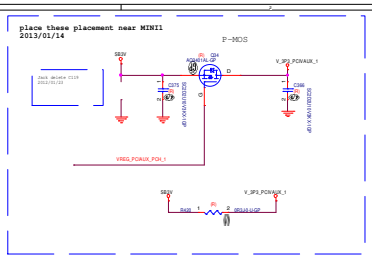
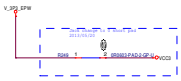
V_3P3_PCIVAUX_DUAL



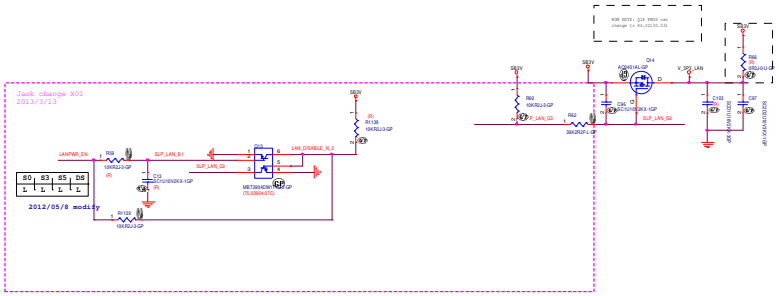


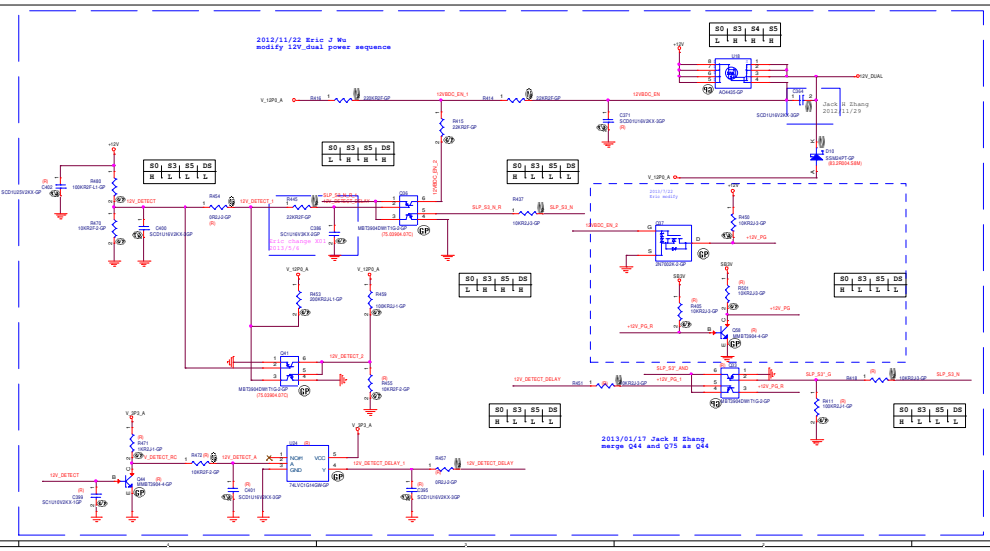
V_3P3_EPW



Stuff w/o AMT
None stuff w/ AMT

V_3P3_LAN



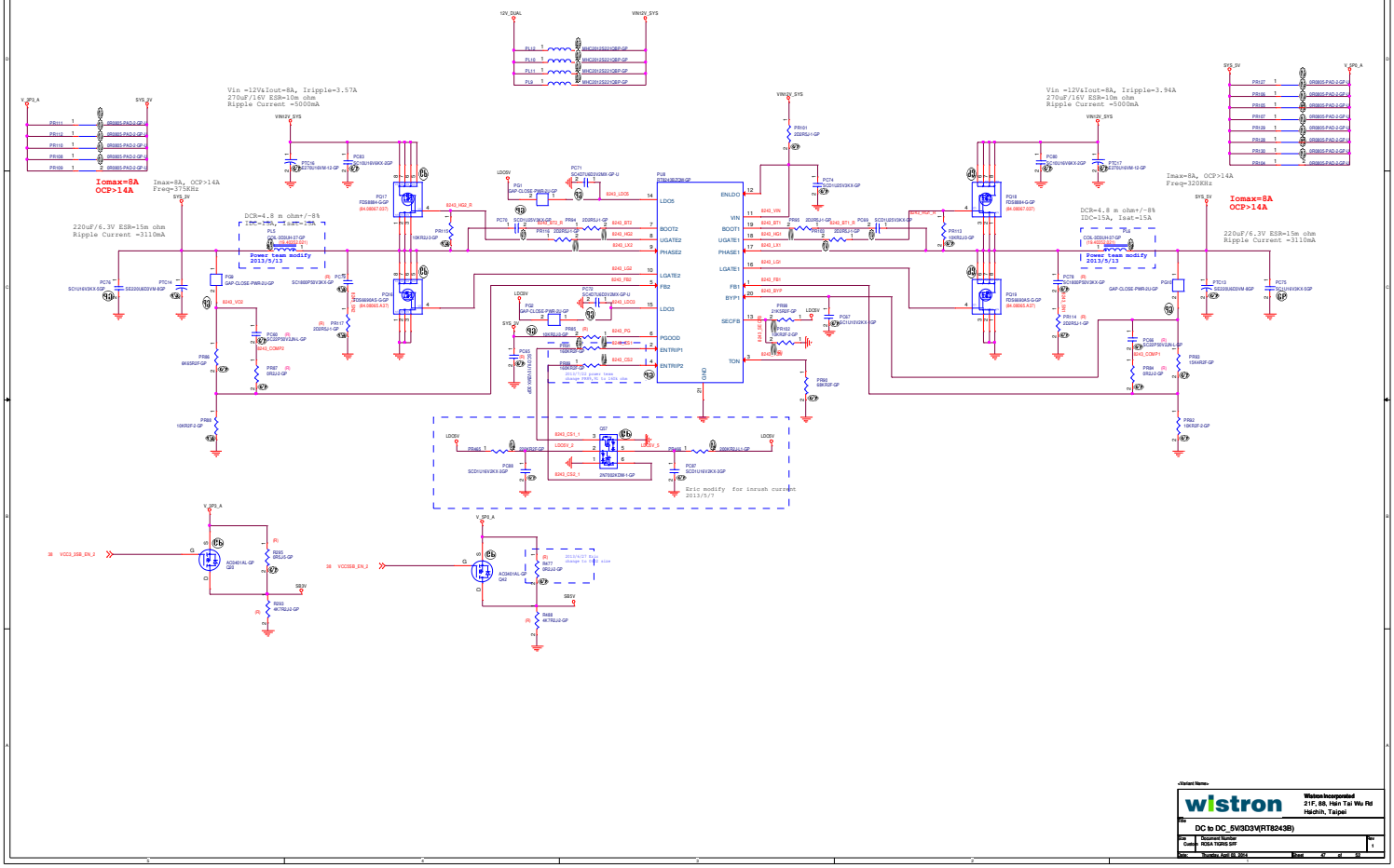


wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

DUAL POWER

Size: Custom | Document Number: ROSA 76GRS SFF | Rev: 1

Date: Thursday, April 11, 2013 | Sheet 46 of 53



«Variant Name»

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

File: DC to DC_5V/3V(RT8243B)

Size: | Document Number: ROSA TIGRIS SPF | Rev: 1

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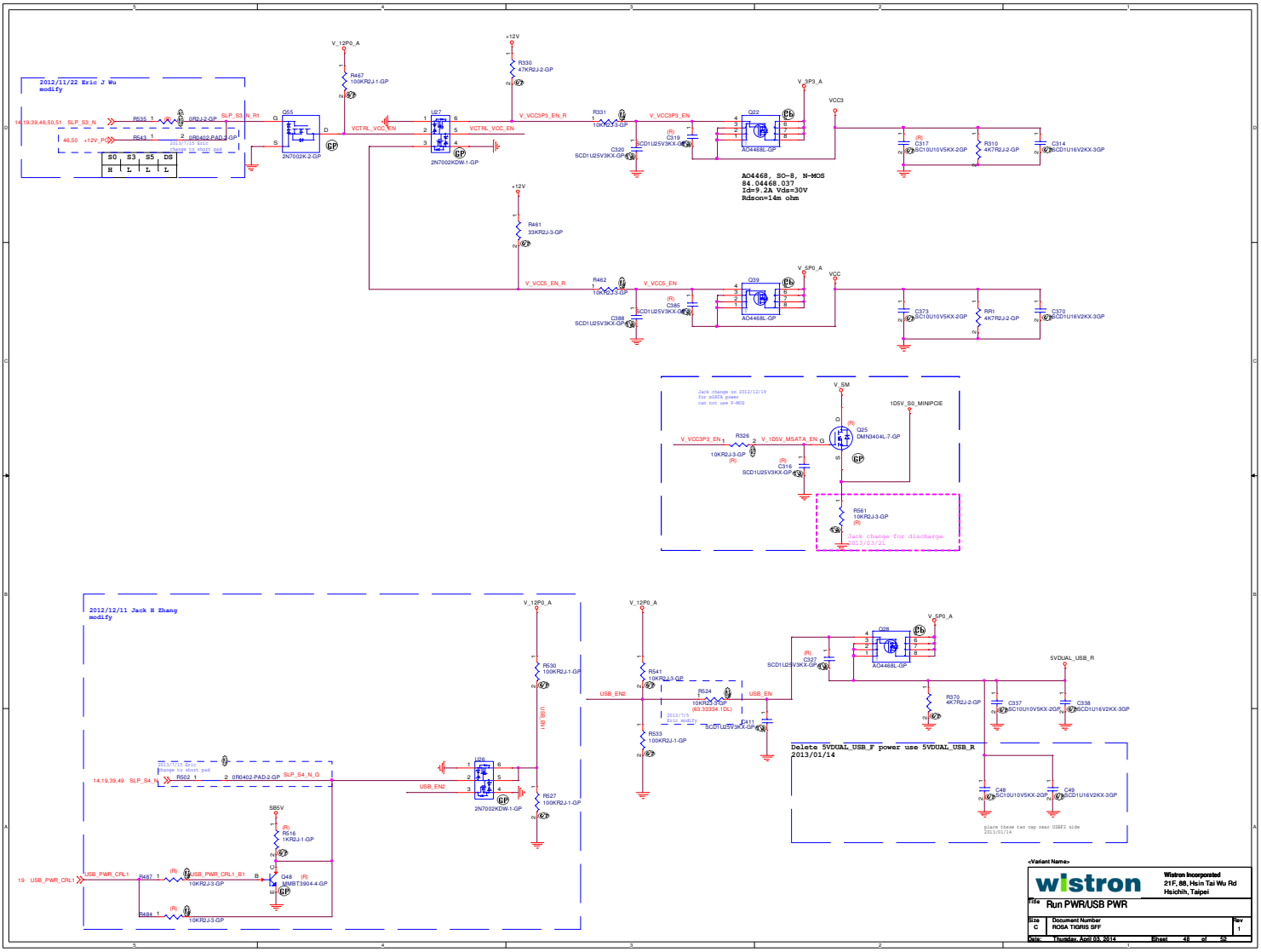

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: Run PWR/USB PWR

Size	Document Number	Rev
C	ROSA TIGRIS SFF	1

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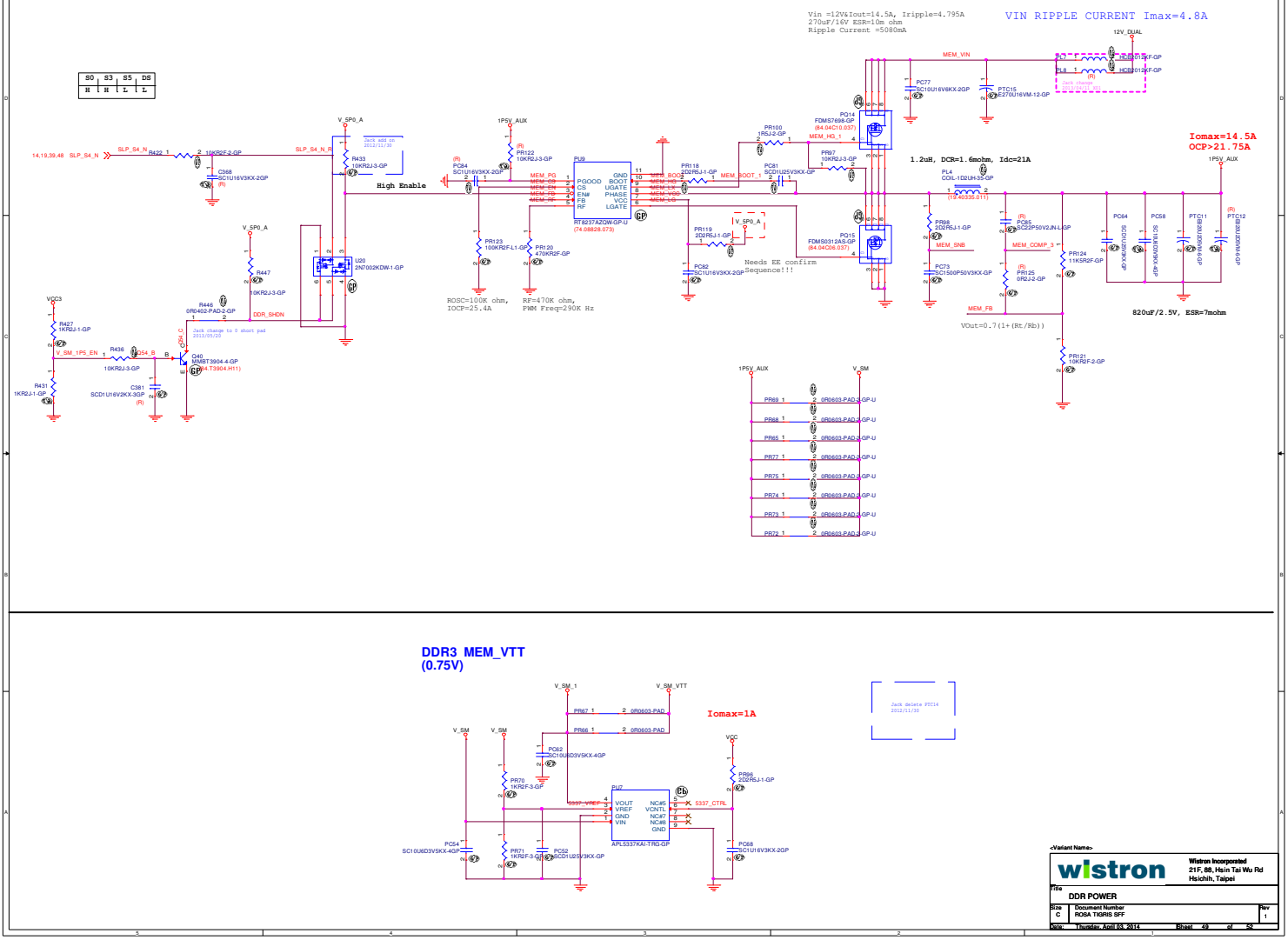

<Variant Name>			
wistron	Wistron Incorporated 21F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
Title	DDR POWER		
Size: C	Document Number: ROSA TIGRIS SFF		Rev: 1
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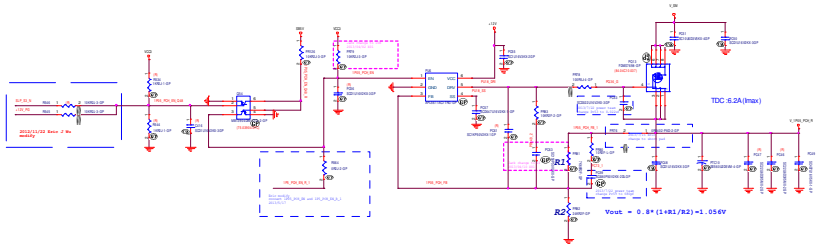
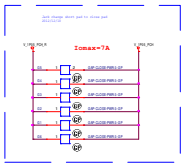
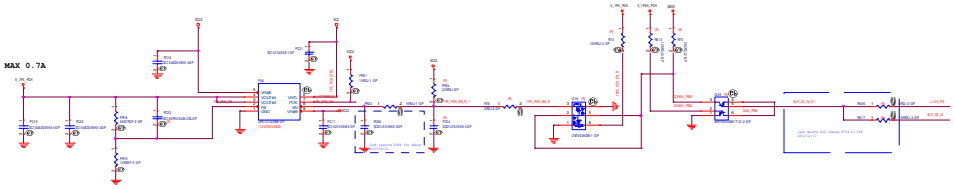
V_1P05_PCH



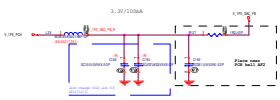


Jack change on
2012/11/28

V_1P5



V_1P5_DAC_FB_R



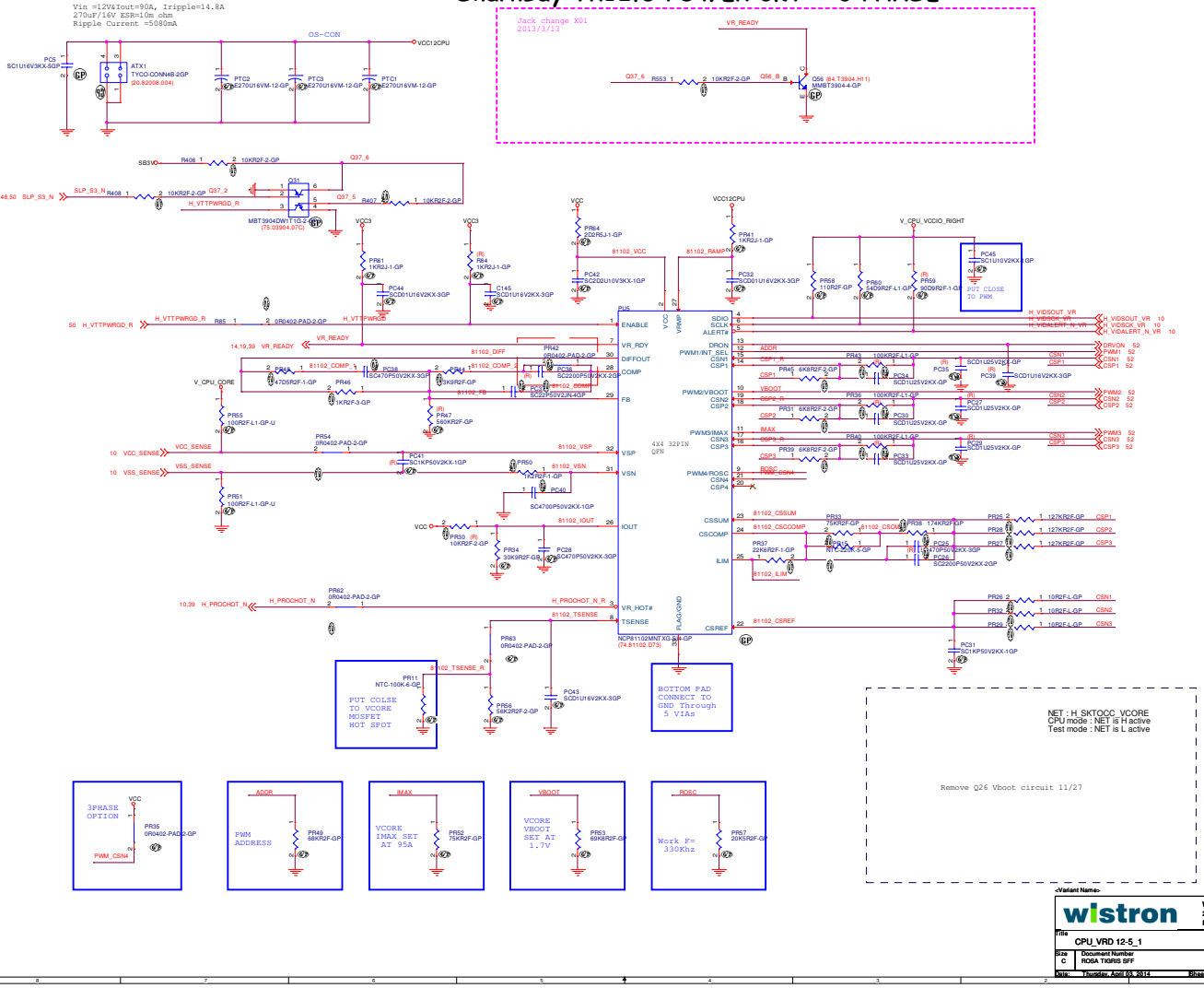
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
SYSTEM POWER

SharkBay VR12.5 POWER CKT - 3 PHASE

VCC_CORE

Vin =12V&Iout=90A, Iripple=14.8A
270uF/16V ESR=10m ohm
Ripple Current =5080mA

Jack change X01
2013/3/13



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU_VRD 12-5_1

Size	Document Number	Rev
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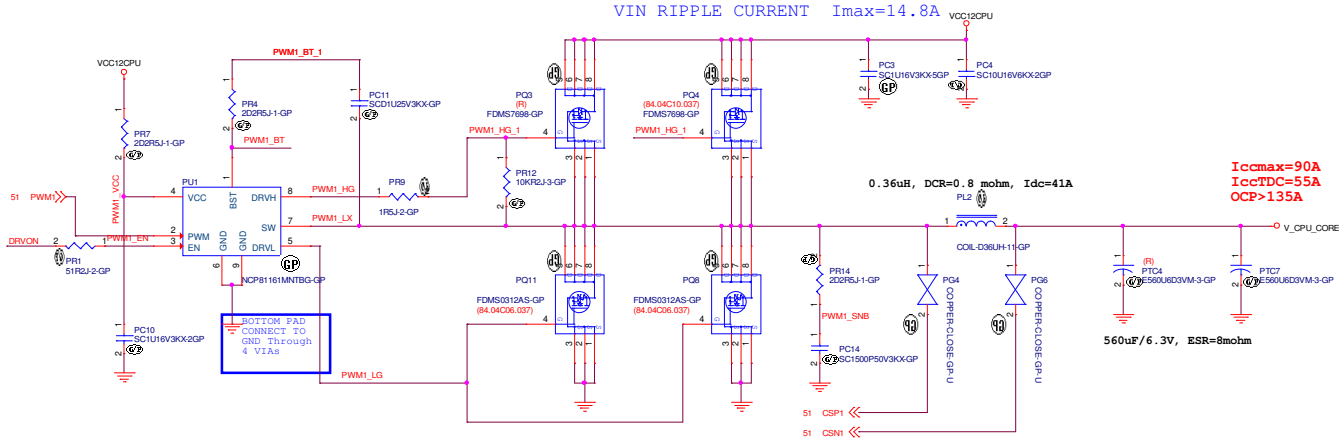
84.04927.A37 NTMFS4927
Vgs @ 4.5V,
Id = 13.7A,
Rds(on) = 9.2~13mohm,

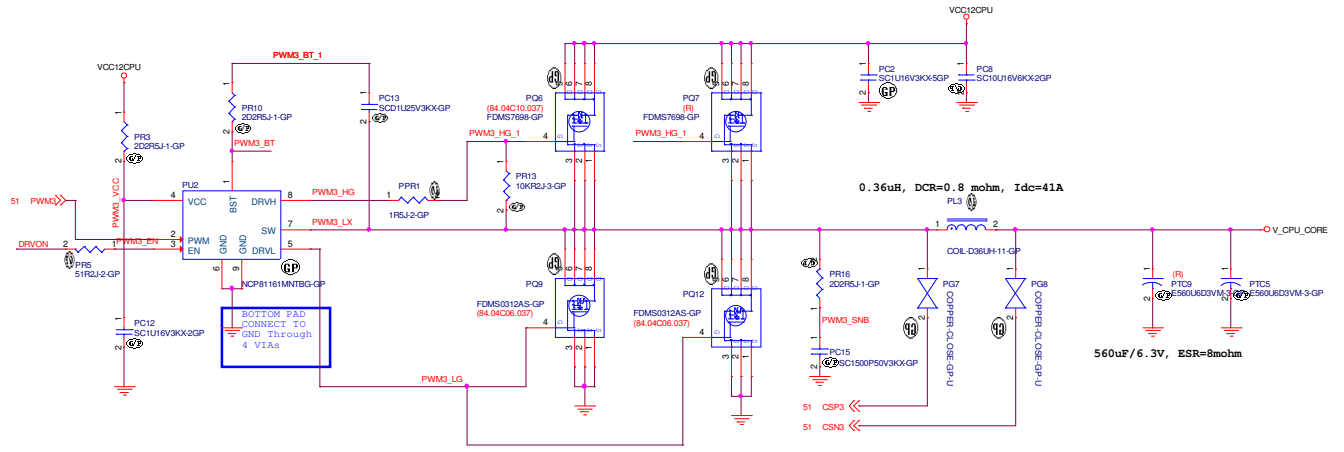
84.04925.031 NTMFS4925
Vgs @ 4.5V,
Id = 15.9A,
Rds(on) = 6.4~10mohm,

VIN RIPPLE CURRENT Imax=14.8A



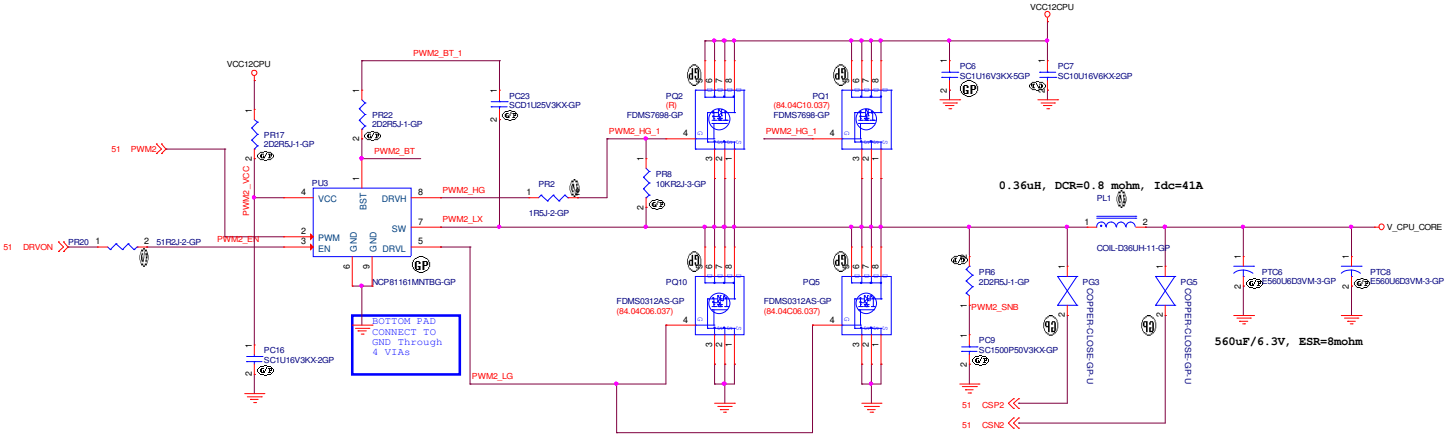
84.04927.A37 NTMFS4927
Vgs @ 4.5V,
Id = 13.7A,
Rds(on) = 9.2~13mohm,

84.04925.031 NTMFS4925
Vgs @ 4.5V,
Id = 15.9A,
Rds(on) = 6.4~10mohm,



84.04927.A37 NTMFS4927
Vgs @ 4.5V,
Id = 13.7A,
Rds(on) = 9.2~13mohm,

84.04925.031 NTMFS4925
Vgs @ 4.5V,
Id = 15.9A,
Rds(on) = 6.4~10mohm,



<Variant Name>

wistron

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Title: CPU_VRD 12-5_2

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