PCB Number: 10086-1M

PAGE	TITLE	Quantity
01	Cover Page	
02	BLOCK DIAGRAM	
03	Power Delivery	
04	POWER GOOD AND RESET DIAGRAM	
05	CLOCKS DIAGRAM	
06	Power Sequence	
07	POWER Map	
08	GPIO	
09	RESERVE	
10	CPU LGA 1155_1	
11	CPU LGA 1155_2	
12	CPU LGA 1155_3	
13	CPU LGA 1155_4	
14	XDP/80 PORT HEADER	
15	DDR3 CHA DIMM 0	
16	DDR3 CHA DIMM 1	
17	PCH_Cougar_AUDIO/GPIO/SPI	
18	PCH_Cougar_CLK/FDI/ONFI	
19	PCH_Cougar_SATA/FAN/DP	
20	PCH_Cougar_PCI/PCIE/DMI/USB	
21	PCH_Cougar_GND/STRAPS	
22	PCH_Cougar_POWER	
23	SIO 8728	
24	Reserve	
25	AUDIO CODEC ALC 269	
26	GIGA LAN	
27	Reserve	
28	MINI PCIE SLOT	
29	BTN / SATA IF	
30	SIDE USB	
31	FAN	
32	WEBCAM/BT/TOUCH PANEL	
33	CR Connector	
34	Reserver	
35	REAR IO	
36	PWR_ATX_IN	
37	DUAL POWER	
38	POWER_AUX3V/AUX5V RT8205A	
39	POWER RUN TIME POWER	
40	POWER DDR POWER	
41	POWER 1P05ME/1P05PCH	
42	POWER CPU VTT/1D8V	
43	POWER CPU SA	
44	VRM CONTROLLER L6131 AXG	
45	VRM_OUT	
46	POWER LOGIC	
47	SCALAR RTD2281_1	
48	SCALAR RTD2281_2	
49	LVDS 5V	
50	ATI_Power rail	
51	ATI_Mad_PCIE	
52	ATI_Mad_IO	
53	ATI_Mad_POWER	
54	ATI_DP POWER	
55	ATI_Mad_MEMORY	
56	ATI_DDR3 64MX16 A	
57	ATI_DDR3 64MX16 B	
58	ATI_THERM & STRAPS	
59	GPU_ISL_IN_GFX_VCORE	
60	GPU RT8015 VGA 1.0/1.8V	
61	DISPLAY PORT SWITCH	
62	VGA IN	

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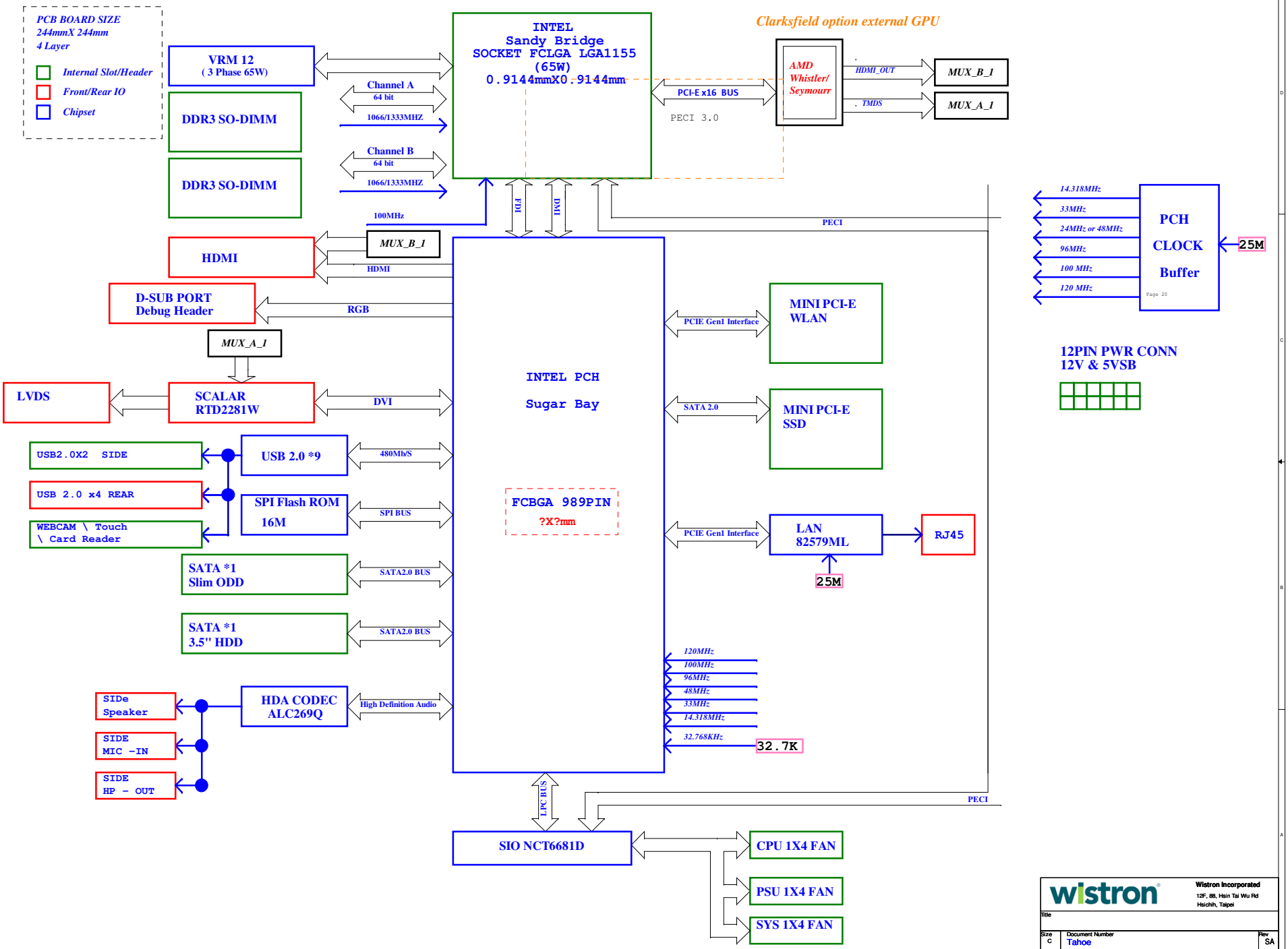
PCB BOARD SIZE
244mmX 244mm
4 Layer
Internal Slot/Header
Front/Rear IO
Chipset
VRM 12
(3 Phase 65W)
DDR3 SO-DIMM
DDR3 SO-DIMM
Channel A
64 bit
1066/1333MHZ
Channel B
64 bit
1066/1333MHZ
INTEL
Sandy Bridge
SOCKET FCLGA LGA1155
(65W)
0.9144mmX0.9144mm
PCI-E x16 BUS
PECI 3.0
Clarksfield option external GPU
AMD
Whistler/
Seymourr
HDMI_OUT
TMDS
MUX_B_1
MUX_A_1
14.318MHz
33MHz
24MHz or 48MHz
96MHz
100 MHz
120 MHz
PCH
CLOCK
Buffer
25M
Page 20
12PIN PWR CONN
12V & 5VSB
100MHz
FDI
DMI
PECI
HDMI
MUX_B_1
HDMI
D-SUB PORT
Debug Header
RGB
MUX_A_1
LVDS
SCALAR
RTD2281W
DVI
INTEL PCH
Sugar Bay
FCBGA 989PIN
?X?mm
PCIE Gen1 Interface
MINI PCI-E
WLAN
SATA 2.0
MINI PCI-E
SSD
PCIE Gen1 Interface
LAN
82579ML
RJ45
25M
USB2.0X2 SIDE
USB 2.0 x4 REAR
WEBCAM \ Touch
\ Card Reader
USB 2.0 *9
480Mb/S
SPI Flash ROM
16M
SPI BUS
SATA *1
Slim ODD
SATA2.0 BUS
SATA *1
3.5" HDD
SATA2.0 BUS
120MHz
100MHz
96MHz
48MHz
33MHz
14.318MHz
32.768KHz
32.7K
SIDe
Speaker
SIDE
MIC -IN
SIDE
HP - OUT
HDA CODEC
ALC269Q
High Definition Audio
LPC BUS
PECI
SIO NCT6681D
CPU 1X4 FAN
PSU 1X4 FAN
SYS 1X4 FAN
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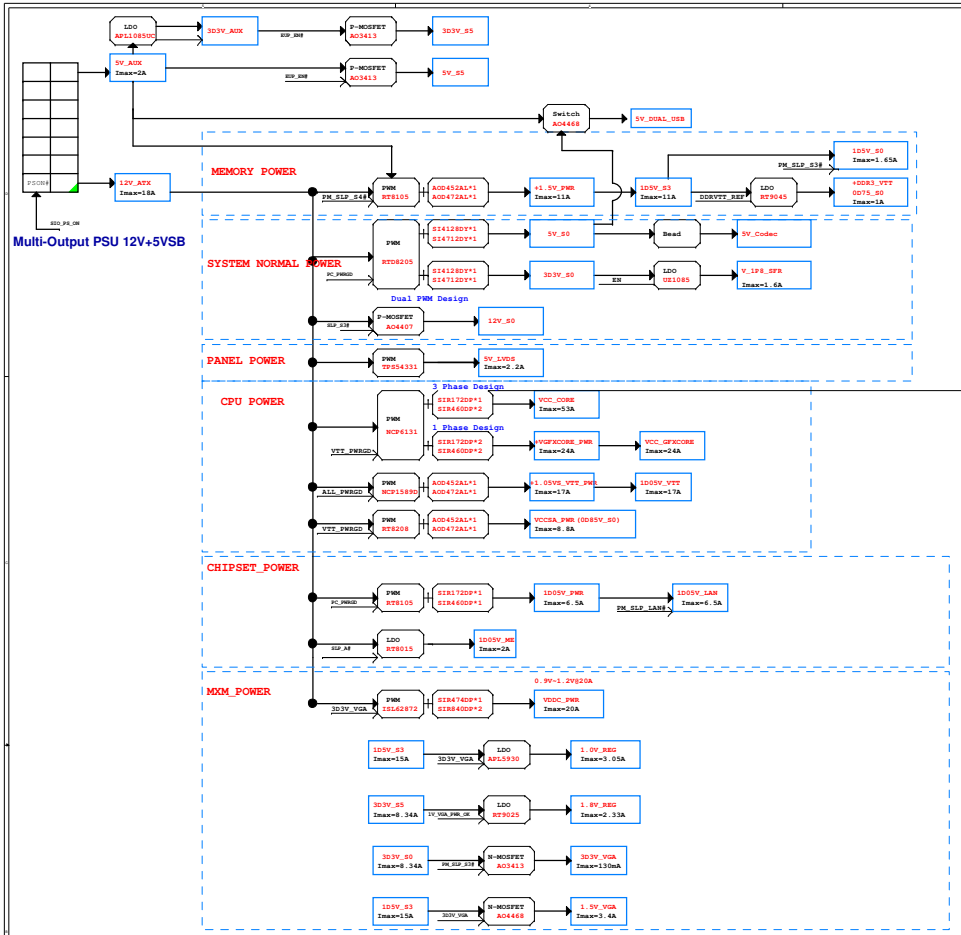
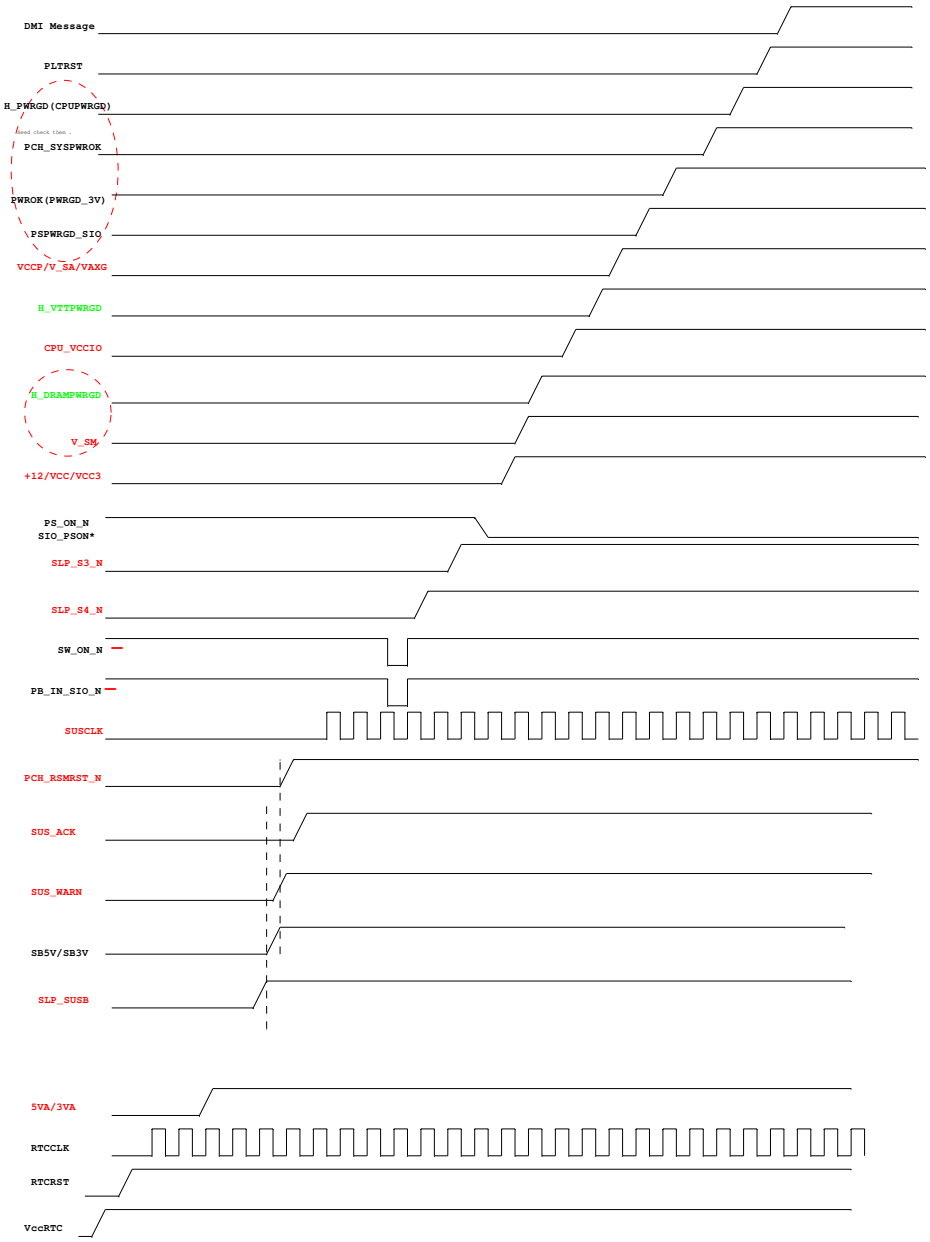
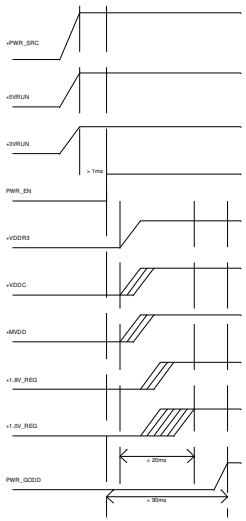

Multi-Output PSU 12V+5VSB
MEMORY POWER
SYSTEM NORMAL POWER
PANEL POWER
CPU POWER
CHIPSET_POWER
MXM_POWER
Dual PWM Design
3 Phase Design
3 Phase Design
0.9V~1.2V@20A

POWER ON SEQUENCE



GPU CEDAR POWER SEQUENCE

POWER UP SEQUENCE(not to scale)



VDDR3, A2VDD +VDDR3 should ramp before or simultaneously with +VDDC.
+VDDC should ramp before +1.8V_REG and +1.0V_REG.

VDDC, VDDCI

VDDR1, MVDDQ/C

VDDR4, VDD_CT, TSVDD, PCIE_VDDR, PCIE_PVDD, DPLL_PVDD, DPx_PVDD, DPx_VDD18, MPV18, SPV18, AVDD, VDD1DI, A2VDDQ, VDD2DI

PCIE_VDDC, DPLL_VDDC, DPx_VDD10, SPV10

+1.0V_REG AND +1.8V_REG RAMP UP SEQUENCE CAN BE INTERCHANGED.

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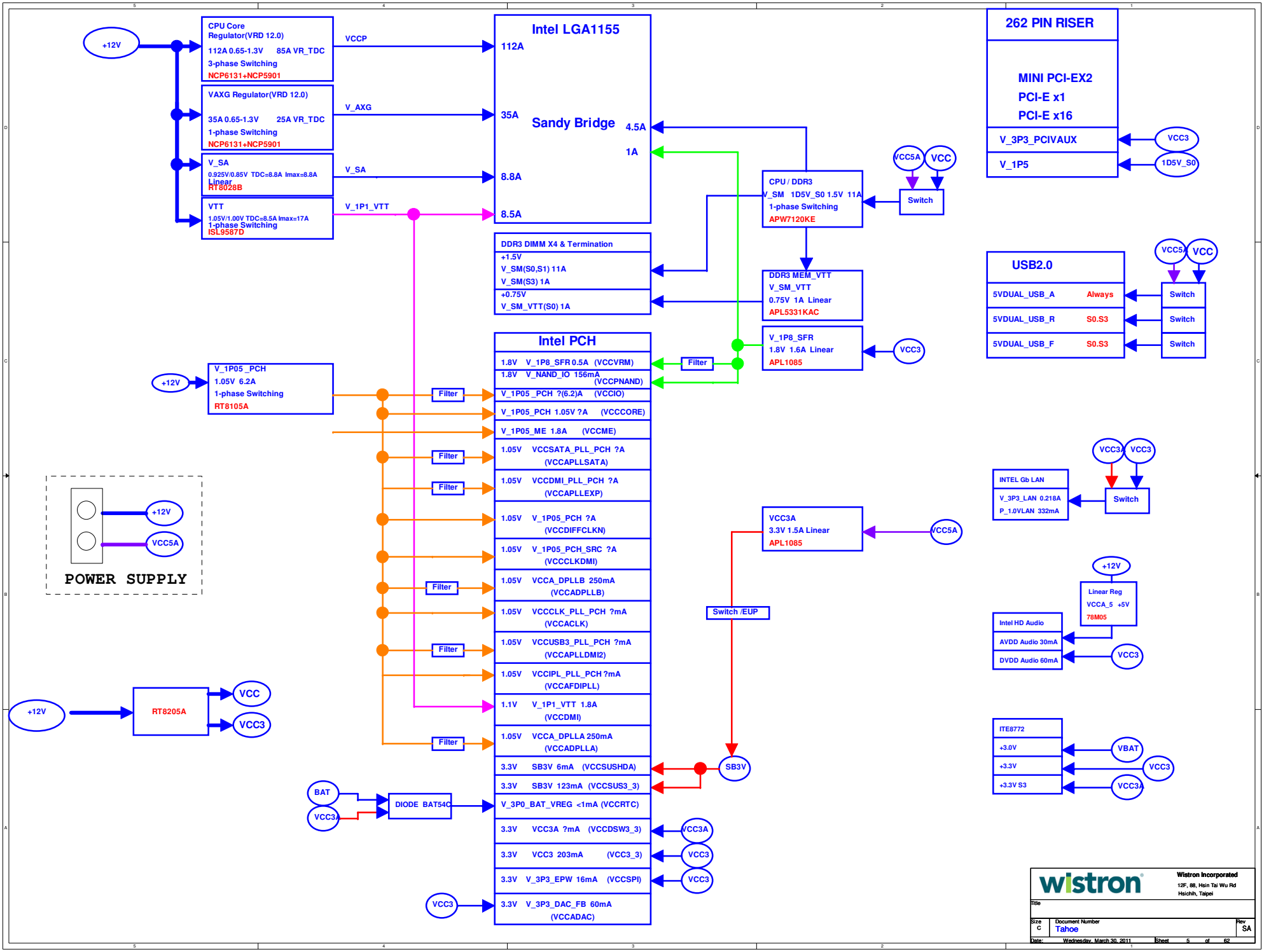

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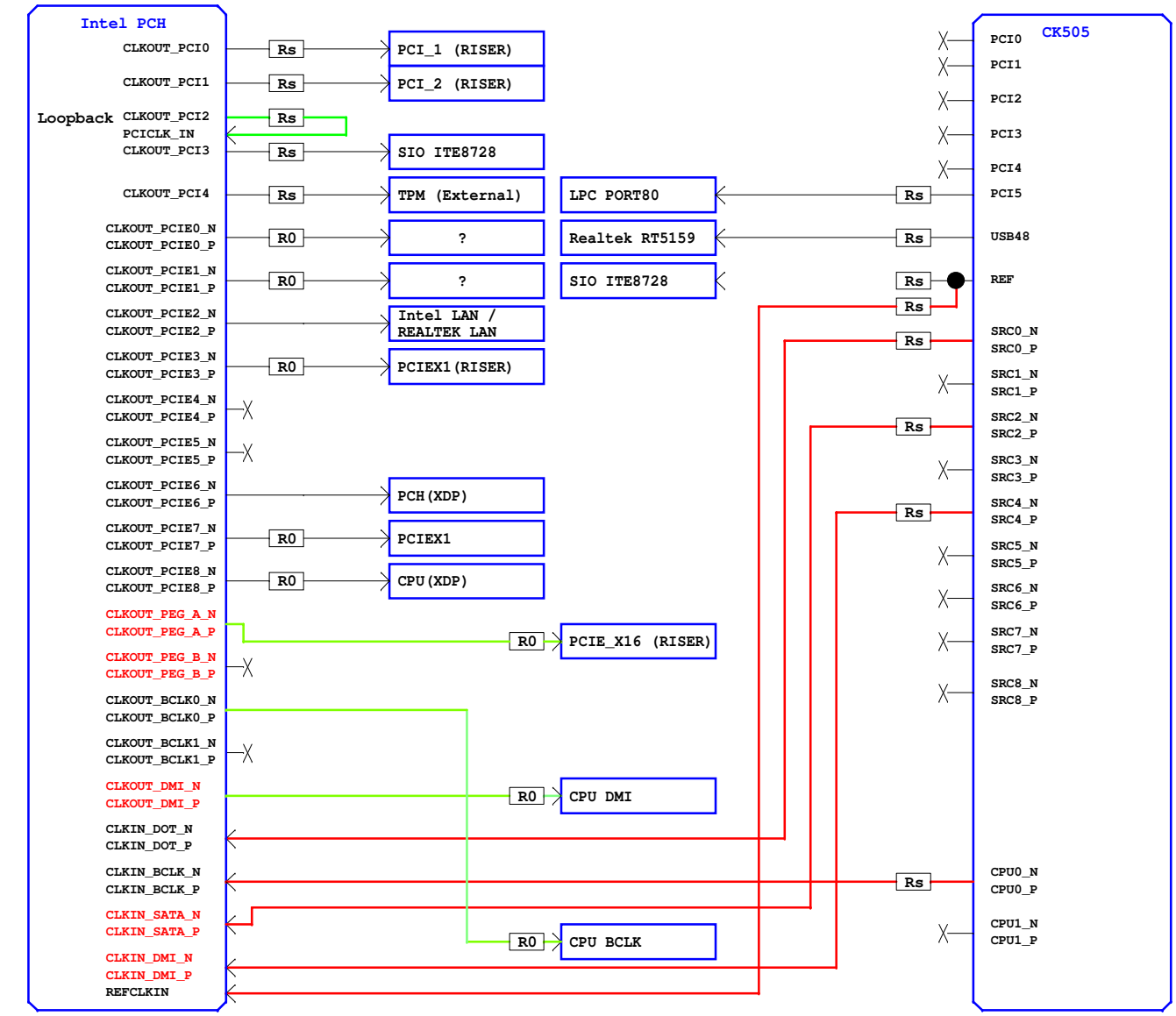


BTM: Buffer Through Mode
Need CK505 to provide 4 clock to PCH

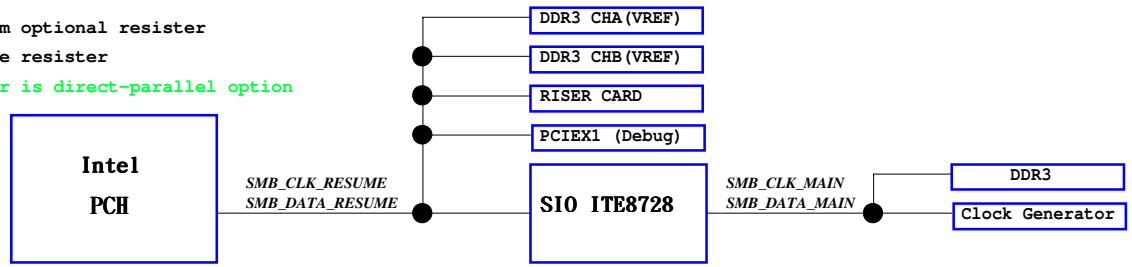
FCIM: Full Clock Intergration Mode
Remove CK505

Note: Red Color is Gen2 spec.

Note: R0 is 0 ohm optional resister

Note: Rs is serie resister

Note: Green Color is direct-parallel option



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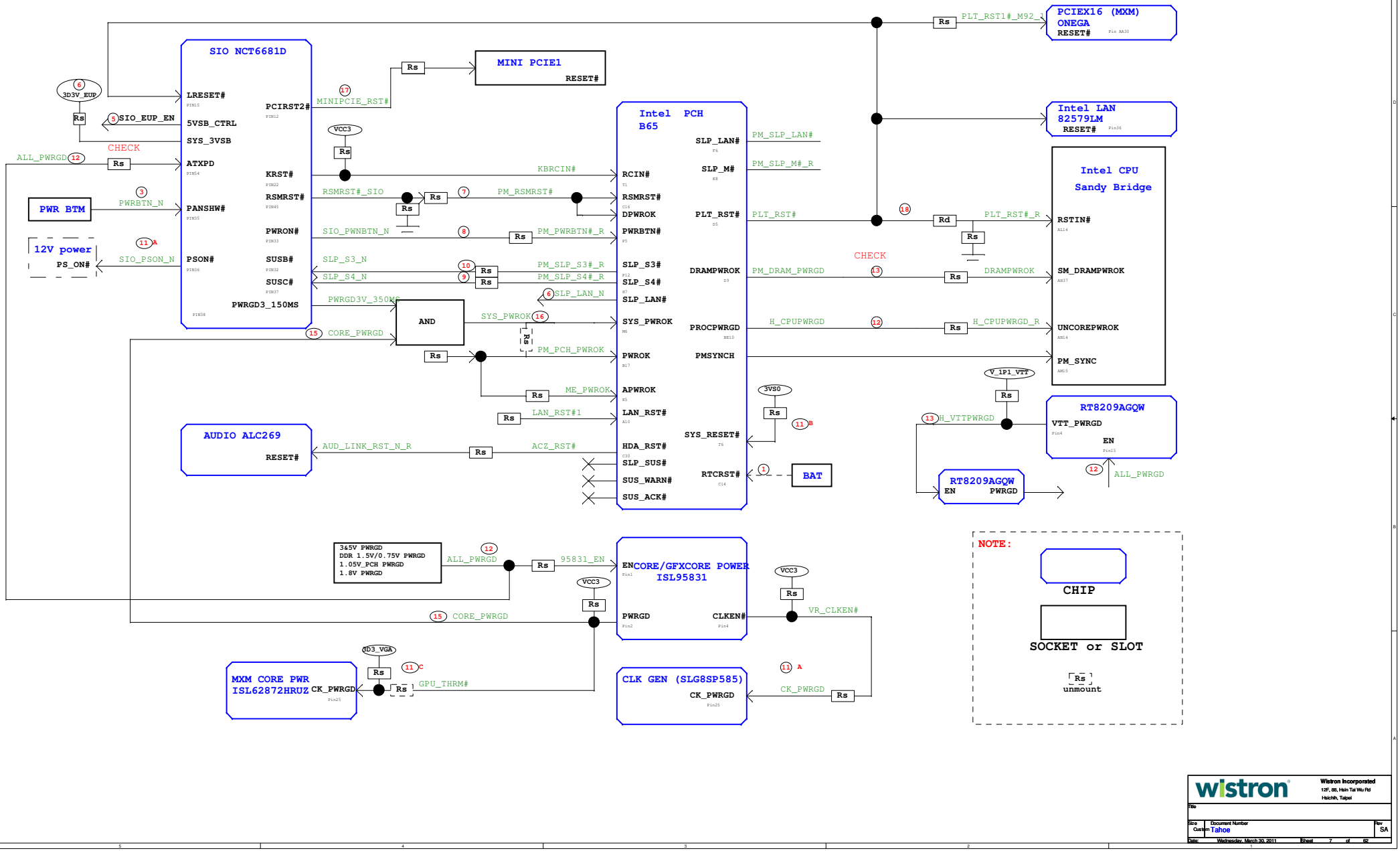
SIO NCT6681D
LRESET#
5VSB_CTRL
SYS_3VSB
ATXPD
PANSHW#
PSON#
PCIRST2#
KRST#
RSMRST#
PWRON#
SUSB#
SUSC#
PWRGD3_150MS
MINIPCIE_RST#
MINI PCIE1
RESET#
3D3V_EUP
SIO_EUP_EN
CHECK
ALL_PWRGD
PWR BTM
PWRBTN_N
12V power
PS_ON#
SIO_PSON_N
VCC3
KBRCIN#
RSMRST#_SIO
PM_RSMRST#
SIO_PWNBTN_N
PM_PWRBTN#_R
SLP_S3_N
SLP_S4_N
PM_SLP_S3#_R
PM_SLP_S4#_R
SLP_LAN_N
PWRGD3V_350MS
AND
CORE_PWRGD
SYS_PWROK
PM_PCH_PWROK
ME_PWROK
LAN_RST#1
AUDIO ALC269
RESET#
AUD_LINK_RST_N_R
ACZ_RST#
Intel PCH
B65
RCIN#
RSMRST#
DPWROK
PWRBTN#
SLP_S3#
SLP_S4#
SLP_LAN#
SYS_PWROK
PWROK
APWROK
LAN_RST#
HDA_RST#
SLP_SUS#
SUS_WARN#
SUS_ACK#
SLP_LAN#
SLP_M#
PLT_RST#
DRAMPWROK
PROCPWROK
PMSYNCH
SYS_RESET#
RTCRST#
PM_SLP_LAN#
PM_SLP_M#_R
PLT_RST#
PM_DRAM_PWRGD
H_CPUPWRGD
3VS0
BAT
PCIEX16 (MXM)
ONEGA
RESET#
Intel LAN
82579LM
RESET#
Intel CPU
Sandy Bridge
RSTIN#
SM_DRAMPWROK
UNCOREPWROK
PM_SYNC
PLT_RST#_R
DRAMPWROK
H_CPUPWRGD_R
V_1P1_VTT
RT8209AGQW
VTT_PWRGD
EN
H_VTTPWRGD
RT8209AGQW
EN
PWRGD
3&5V PWRGD
DDR 1.5V/0.75V PWRGD
1.05V_PCH PWRGD
1.8V PWRGD
95831_EN
ENCORE/GFXCORE POWER
ISL95831
PWRGD
CLKEN#
VR_CLKEN#
MXM CORE PWR
ISL62872HRUZ
CK_PWRGD
GPU_THRM#
3D3_VGA
CLK GEN (SLG8SP585)
CK_PWRGD
NOTE:
CHIP
SOCKET or SLOT
Rs
unmount
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Size
Custom
Document Number
Tahoe
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CLOCK
20 CK_DMI_BUF_CPU_DP
20 CK_DMI_BUF_CPU_DN

VID
44 H_VIDSCK_VR
44 H_VIDSOUT_VR
44 H_VIDALERT_VR

CPU_SA
43 VCCSA_VID
43 VCCSA_SENSE

CPU_VTT
42 VCCIO_SEL
42 VCCIO_SENSE
42 VSSIO_SENSE

CPU_AXG
44 VCCAXG_SENSE
44 VSSAXG_SENSE

CPU_VCORE
44 VCC_SENSE
44 VSS_SENSE

20101031 Richard
24 H_SKTOCC_N

XDP_RST
14,17 XDP_DBRESET_N

OTHER
24,44 H_PROCHOT_N
21 H_SNB_N

SMBUS

PWR MANAGER
14,17 H_PWRGD
17 H_DRAMPWRGD_CPU
14,17,24,51 PLT_RST_N

19 H_PM_SYNC_0

Thermal
19,24 H_PECI
19 H_THERMTRIP_N

ITP
14 H_TDO
14 H_TDI
14 H_TCK
14 H_TMS
14 H_TRST_N
14 H_PRDY_N
14 H_PREQ_N

14,17 XDP_DBRESET_N
14 CK_XDP_S_DN
13,14 CK_XDP_S_DP

14 H_BPM#0
14 H_BPM#1
14 H_BPM#2
14 H_BPM#3
14 H_BPM#4
14 H_BPM#5
14 H_BPM#6
14 H_BPM#7

14 H_CPURST_N

14 TPEV_SNB_PCUDEBUG_0
13/21:follow CRB1.0 rout the CFG[0] to CPU !

V_CPU_VCCIO
R95 1 (R) 1KR2J-1-GP H_PECI
R118 1 (R) 1KR2J-1-GP H_CATERR_N
R88 1 (R) 51R2J-2-GP H_PROCHOT_R_N
R111 1 (R) 51R2J-2-GP CPU_THERMTRIP_N
R96 1 (R) 51R2J-2-GP H_PWRGD
R100 1 1KR2J-1-GP
need check R738 stuff or unstuff ?

1D5V_S3
R123 1KR2F-3-GP
SNB_DDR_VREF
R125 1KR2F-3-GP
C54 SCD1U10V2KX-4-LL-GP

20101010 Richard
H_VIDSCK_VR R706 1 2 0R0402-PAD H_VIDSCK
H_VIDSOUT_VR R707 1 2 0R0402-PAD H_VIDSOUT
H_VIDALERT_VR R705 1 2 0R0402-PAD H_VIDALERT
H_PROCHOT_N R89 1 2 0R0402-PAD H_PROCHOT_R_N
H_THERMTRIP_N R112 1 2 0R0402-PAD CPU_THERMTRIP_N

Buffered reset to CPU
2010.0824.Richard
20101024 Richard
20101031 Richad
V_CPU_VCCIO
R79 1KR2J-1-GP
H_CPURST_N_BUF
R63 2 0R0402-PAD CPURST_N
R59 2KR2F-3-GP (R)
C43 SCD1U16V2ZY-2LGP
R65 0R0402-PAD
PLT_RST_N
R62 2 1 10KR2J-3-GP PLTRST_H1
H_CPURST_N_1
3D3V_S5
R85 10KR2J-3-GP
PLTRST_H
(84.2N702.A3F) 2N7002DW-1-GP Q7
1A 20110213 Richard
Change R63 & R65 to short-pad

V_CPU_VCCIO
R135 1 75R2F-2-GP
R128 1 110R2F-GP
R129 1 (R) 90D9R2F-1-GP
Place the 3pcs Res near CPU

PECI ADDR:0X30
3D3V_S5
R941 100KR2J-1-GP
20101031 Richard
H_SKTOCC_N
20101020 Richard
CFG2 PD --> PEG BUS REVERSAL
13/21:follow CRB1.0 rout the CFG[0] to CPU !
SNB_DDR_VREF
TPEV_SNB_PCUDEBUG_0

R136 1 H_VIDALERT_N
R127 1 (R) 2 44D2R2F-GP
100R2J-2-GP

R98 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_1 H36 CFG_0
R97 1 1KR2J-1-GP TPEV_SNB_PCUDEBUG_2 J37 CFG_1
R83 1 1KR2J-1-GP TPEV_SNB_PCUDEBUG_3 K36 CFG_2
R103 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_4 L36 CFG_3
R116 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_5 N35 CFG_4
R117 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_6 L37 CFG_5
R122 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_7 M36 CFG_6
R110 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_8 J38 CFG_7
R104 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_9 L35 CFG_8
R126 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_10 M38 CFG_9
R99 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_11 N36 CFG_10
R101 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_12 N38 CFG_11
R113 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_13 N39 CFG_12
R121 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_14 N37 CFG_13
R105 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_15 N40 CFG_14
R132 1 (R) 1KR2J-1-GP TPEV_SNB_PCUSTB_0 G37 CFG_15
R102 1 (R) 1KR2J-1-GP TPEV_SNB_PCUSTB_1 G36 CFG_16
R106 1 (R) 1KR2J-1-GP CFG_17

AT14 RSVD#AT14
H7 RSVD#H7
H8 RSVD#H8

U7E 5 OF 11
SANDY BRIDGE
CK_DMI_BUF_CPU_DP W2 BCLK_0
CK_DMI_BUF_CPU_DN W1 BCLK#_0
H_VIDSCK C37 VIDSCLK
H_VIDSOUT B37 VIDSOUT
H_VIDALERT_N A37 VIDALERT#
H_PWRGD J40 UNCOREPWRGOOD
H_DRAMPWRGD_CPU AJ19 SM_DRAMPWROK
H_CPURST_N F36 RESET#
H_PM_SYNC_0 E38 PM_SYNC
H_PECI J35 PECI
H_CATERR_N E37 CATERR#
H_PROCHOT_R_N H34 PROCHOT#
CPU_THERMTRIP_N G35 THERMTRIP#
H_SNB_N K32 PROC_SEL
SNB_DDR_VREF AJ22 SM_VREF
H_SKTOCC_N AJ33 SKTOCC#

VCCIO_SEL P33
VCCSA_VID P34
VCCSA_SENSE T2
VCC_SENSE A36
VSS_SENSE B36
VCCIO_SENSE AB4
VSSIO_SENSE AB3
VCCAXG_SENSE L32
VSSAXG_SENSE M32
TDO L39 H_TDO
TDI L40 H_TDI
TCK M40 H_TCK
TMS L38 H_TMS
TRST# J39 H_TRST_N
PRDY# K38 H_PRDY_N
PREQ# K40 H_PREQ_N
DBR# E39 XDP_DBRESET_N
BCLK_ITP# D40 ITP_CLKINN
R131 1 (R) 2 0R2J-2-GP CK_XDP_S_DN
XDP_DBRESET_N
R261 need stuff the 0ohm?

BPM#_0 H40 H_BPM#0
BPM#_1 H38 H_BPM#1
BPM#_2 G38 H_BPM#2
BPM#_3 G40 H_BPM#3
BPM#_4 G39 H_BPM#4
BPM#_5 F38 H_BPM#5
BPM#_6 E40 H_BPM#6
BPM#_7 F40 H_BPM#7

RSVD#J33 J33
RSVD#L34 L34
RSVD#L33 L33
RSVD#K34 K34
RSVD#N33 N33
RSVD#M34 M34
RSVD#L9 L9
RSVD#J9 J8
RSVD#K9 K9
RSVD#L31 L31
RSVD#J31 J31
RSVD#K31 K31
RSVD#AD34 AD34
RSVD#AD35 AD35

SAN-1U2NF
(62.10055.441)

SB 20101223 Richard
Remove R727

5V_S0
R768 10KR2J-3-GP
R769 4K7R2J-2-GP

PEG CONFIG TABLE Default is X16

CFG	H	L	DESCRIPTION
0	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED
2	NORM	RESERVE	PEG REVERSAL[0]
3,4,7-17	RESERVED	RESERVED	RESERVED

CFG5/SEL0	CFG6/SEL1	PCIE CONFIG
1	1	1 X 16
0	1	1 X 8

* NOA[6:5] 11:DEFAULT X16; 10:2X8; 01:RESERVED; 00:X8,X4,X4 *
if follow CRB1.0 please confirm the table still need or not ?

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DMI

20 DMI_PCH_CPU_DN[0..3]
20 DMI_PCH_CPU_DP[0..3]
20 DMI_CPU_PCH_DP[0..3]
20 DMI_CPU_PCH_DN[0..3]

FDI

18 FDI_FSYNC_0
18 FDI_LSYNC_0
18 FDI_FSYNC_1
18 FDI_LSYNC_1
18 FDI_INT
18 FDI_TX_DP[0..7]
18 FDI_TX_DN[0..7]

51 PEG_RXN[15..0]
PEG_RXN15
PEG_RXN14
PEG_RXN13
PEG_RXN12
PEG_RXN11
PEG_RXN10
PEG_RXN9
PEG_RXN8
PEG_RXN7
PEG_RXN6
PEG_RXN5
PEG_RXN4
PEG_RXN3
PEG_RXN2
PEG_RXN1
PEG_RXN0

51 PEG_RXP[15..0]
PEG_RXP15
PEG_RXP14
PEG_RXP13
PEG_RXP12
PEG_RXP11
PEG_RXP10
PEG_RXP9
PEG_RXP8
PEG_RXP7
PEG_RXP6
PEG_RXP5
PEG_RXP4
PEG_RXP3
PEG_RXP2
PEG_RXP1
PEG_RXP0

U7C — 3 OF 11 — SANDY BRIDGE

PEG_RXP15	B11	PEG_RX_0	PEG_TX_0	C13	PEG_C_TXP15
PEG_RXN15	B12	PEG_RX#_0	PEG_TX#_0	C14	PEG_C_TXN15
PEG_RXP14	D12	PEG_RX_1	PEG_TX_1	E14	PEG_C_TXP14
PEG_RXN14	D11	PEG_RX#_1	PEG_TX#_1	E13	PEG_C_TXN14
PEG_RXP13	C10	PEG_RX_2	PEG_TX_2	G14	PEG_C_TXP13
PEG_RXN13	C9	PEG_RX#_2	PEG_TX#_2	G13	PEG_C_TXN13
PEG_RXP12	E10	PEG_RX_3	PEG_TX_3	F12	PEG_C_TXP12
PEG_RXN12	E9	PEG_RX#_3	PEG_TX#_3	F11	PEG_C_TXN12
PEG_RXP11	B8	PEG_RX_4	PEG_TX_4	J14	PEG_C_TXP11
PEG_RXN11	B7	PEG_RX#_4	PEG_TX#_4	J13	PEG_C_TXN11
PEG_RXP10	C6	PEG_RX_5	PEG_TX_5	D8	PEG_C_TXP10
PEG_RXN10	C5	PEG_RX#_5	PEG_TX#_5	D7	PEG_C_TXN10
PEG_RXP9	A5	PEG_RX_6	PEG_TX_6	D3	PEG_C_TXP9
PEG_RXN9	A6	PEG_RX#_6	PEG_TX#_6	C3	PEG_C_TXN9
PEG_RXP8	E2	PEG_RX_7	PEG_TX_7	E6	PEG_C_TXP8
PEG_RXN8	E1	PEG_RX#_7	PEG_TX#_7	E5	PEG_C_TXN8
PEG_RXP7	F4	PEG_RX_8	PEG_TX_8	F8	PEG_C_TXP7
PEG_RXN7	F3	PEG_RX#_8	PEG_TX#_8	F7	PEG_C_TXN7
PEG_RXP6	G2	PEG_RX_9	PEG_TX_9	G10	PEG_C_TXP6
PEG_RXN6	G1	PEG_RX#_9	PEG_TX#_9	G9	PEG_C_TXN6
PEG_RXP5	H3	PEG_RX_10	PEG_TX_10	G6	PEG_C_TXP5
PEG_RXN5	H4	PEG_RX#_10	PEG_TX#_10	G5	PEG_C_TXN5
PEG_RXP4	J1	PEG_RX_11	PEG_TX_11	K7	PEG_C_TXP4
PEG_RXN4	J2	PEG_RX#_11	PEG_TX#_11	K8	PEG_C_TXN4
PEG_RXP3	K3	PEG_RX_12	PEG_TX_12	J5	PEG_C_TXP3
PEG_RXN3	K4	PEG_RX#_12	PEG_TX#_12	J6	PEG_C_TXN3
PEG_RXP2	L1	PEG_RX_13	PEG_TX_13	M8	PEG_C_TXP2
PEG_RXN2	L2	PEG_RX#_13	PEG_TX#_13	M7	PEG_C_TXN2
PEG_RXP1	M3	PEG_RX_14	PEG_TX_14	L6	PEG_C_TXP1
PEG_RXN1	M4	PEG_RX#_14	PEG_TX#_14	L5	PEG_C_TXN1
PEG_RXP0	N1	PEG_RX_15	PEG_TX_15	N5	PEG_C_TXP0
PEG_RXN0	N2	PEG_RX#_15	PEG_TX#_15	N6	PEG_C_TXN0

PEG

DMI_PCH_CPU_DP0	W5	DMI_RX_0	DMI_TX_0	V7	DMI_CPU_PCH_DP0
DMI_PCH_CPU_DN0	W4	DMI_RX#_0	DMI_TX#_0	V6	DMI_CPU_PCH_DN0
DMI_PCH_CPU_DP1	V3	DMI_RX_1	DMI_TX_1	W7	DMI_CPU_PCH_DP1
DMI_PCH_CPU_DN1	V4	DMI_RX#_1	DMI_TX#_1	W8	DMI_CPU_PCH_DN1
DMI_PCH_CPU_DP2	Y3	DMI_RX_2	DMI_TX_2	Y6	DMI_CPU_PCH_DP2
DMI_PCH_CPU_DN2	Y4	DMI_RX#_2	DMI_TX#_2	Y7	DMI_CPU_PCH_DN2
DMI_PCH_CPU_DP3	AA4	DMI_RX_3	DMI_TX_3	AA7	DMI_CPU_PCH_DP3
DMI_PCH_CPU_DN3	AA5	DMI_RX#_3	DMI_TX#_3	AA8	DMI_CPU_PCH_DN3

DMI

	P3	PE_RX_0	PE_TX_0	P8	
	P4	PE_RX#_0	PE_TX#_0	P7	
	R2	PE_RX_1	PE_TX_1	T7	
	R1	PE_RX#_1	PE_TX#_1	T8	
	T4	PE_RX_2	PE_TX_2	R6	
	T3	PE_RX#_2	PE_TX#_2	R5	
	U2	PE_RX_3	PE_TX_3	U5	
	U1	PE_RX#_3	PE_TX#_3	U6	

GEN

PEG_ICOMPO
PEG_RCOMPO
PEG_COMPI

V_CPU_VCCIO
R725 1 — 24D9R2F-L-GP — PEG_COMP — B5 C4 B4
Add layout note item

SAN-1U2NF
(62.10055.441)

PEG Static Lane Reversal

PEG_C_TXN15	C124	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN15
PEG_C_TXN14	C140	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN14
PEG_C_TXN13	C126	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN13
PEG_C_TXN12	C142	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN12
PEG_C_TXN11	C122	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN11
PEG_C_TXN10	C136	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN10
PEG_C_TXN9	C116	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN9
PEG_C_TXN8	C132	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN8
PEG_C_TXN7	C114	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN7
PEG_C_TXN6	C134	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN6
PEG_C_TXN5	C128	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN5
PEG_C_TXN4	C144	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN4
PEG_C_TXN3	C120	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN3
PEG_C_TXN2	C146	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN2
PEG_C_TXN1	C118	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN1
PEG_C_TXN0	C148	1	D1U10V2KX4-LL-GP	(S)	PEG_TXN0

PEG_TXN[15..0] 51

PEG_C_TXP15	C125	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP15
PEG_C_TXP14	C141	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP14
PEG_C_TXP13	C127	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP13
PEG_C_TXP12	C143	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP12
PEG_C_TXP11	C123	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP11
PEG_C_TXP10	C137	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP10
PEG_C_TXP9	C117	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP9
PEG_C_TXP8	C133	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP8
PEG_C_TXP7	C115	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP7
PEG_C_TXP6	C135	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP6
PEG_C_TXP5	C129	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP5
PEG_C_TXP4	C145	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP4
PEG_C_TXP3	C121	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP3
PEG_C_TXP2	C147	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP2
PEG_C_TXP1	C119	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP1
PEG_C_TXP0	C149	1	D1U10V2KX4-LL-GP	(S)	PEG_TXP0

PEG_TXP[15..0] 51

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

U7D — 4 OF 11 — SANDY BRIDGE

FDI_FSYNC_0	AC5	FDI_FSYNC_0	FDI_TX_0	AC8	FDI_TX_DP0
FDI_LSYNC_0	AC4	FDI_LSYNC_0	FDI_TX#_0	AC7	FDI_TX_DN0
			FDI_TX_1	AC2	FDI_TX_DP1
			FDI_TX#_1	AC3	FDI_TX_DN1
			FDI_TX_2	AD2	FDI_TX_DP2
			FDI_TX#_2	AD1	FDI_TX_DN2
			FDI_TX_3	AD4	FDI_TX_DP3
			FDI_TX#_3	AD3	FDI_TX_DN3
FDI_FSYNC_1	AE5	FDI_FSYNC_1	FDI_TX_4	AD7	FDI_TX_DP4
FDI_LSYNC_1	AE4	FDI_LSYNC_1	FDI_TX#_4	AD6	FDI_TX_DN4
			FDI_TX_5	AE7	FDI_TX_DP5
			FDI_TX#_5	AE8	FDI_TX_DN5
			FDI_TX_6	AF3	FDI_TX_DP6
			FDI_TX#_6	AF2	FDI_TX_DN6
			FDI_TX_7	AG2	FDI_TX_DP7
			FDI_TX#_7	AG1	FDI_TX_DN7

FDI LINK

V_CPU_VCCIO
R243 1 — 24D9R2F-L-GP
FDI_INT — AG3 — FDI_INT
FDI_COMP — AE2 — FDI_COMPIO
AE1 — FDI_ICOMPO

SAN-1U2NF
(62.10055.441)

Sandy Bridge Socket

SKT1 SKT2

Load Plate
(22.78003.011)

Back Plate
(22.78002.011)

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU 2

Size: C | Document Number: Tahoe | Rev: SA

Date: Wednesday, March 30, 2011 | Sheet 11 of 62

DDR DATA

15 M_DATA_A[0..63]
16 M_DATA_B[0..63]

15 M_DQS_A_DP[0..7]
15 M_DQS_A_DN[0..7]

16 M_DQS_B_DP[0..7]
16 M_DQS_B_DN[0..7]

DDR CMD/ADD

15 M_MAA_A[0..15]
16 M_MAA_B[0..15]

15 M_WE_A_N
15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
15 M_SBS_A2

16 M_WE_B_N
16 M_CAS_B_N
16 M_RAS_B_N
16 M_SBS_B0
16 M_SBS_B1
16 M_SBS_B2

DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1
15 M_SCKE_A0
15 M_SCKE_A1

15 M_ODT_A0
15 M_ODT_A1

16 M_SCS_B_N0
16 M_SCS_B_N1
16 M_SCKE_B0
16 M_SCKE_B1
16 M_ODT_B0
16 M_ODT_B1

DDR CLOCK

15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

16 CK_M_DDR0_B_DP
16 CK_M_DDR0_B_DN
16 CK_M_DDR1_B_DP
16 CK_M_DDR1_B_DN

DDR OTHERS

15,16 DDR3_DRAMRST_N

U7A — 1 OF 11 — SANDY BRIDGE

M_MAA_A0	AV27	SA_MA_0	SA_DQ_0	AJ3	M_DATA_A0
M_MAA_A1	AY24	SA_MA_1	SA_DQ_1	AJ4	M_DATA_A1
M_MAA_A2	AW24	SA_MA_2	SA_DQ_2	AL3	M_DATA_A2
M_MAA_A3	AW23	SA_MA_3	SA_DQ_3	AL4	M_DATA_A3
M_MAA_A4	AY23	SA_MA_4	SA_DQ_4	AJ2	M_DATA_A4
M_MAA_A5	AT24	SA_MA_5	SA_DQ_5	AJ1	M_DATA_A5
M_MAA_A6	AT23	SA_MA_6	SA_DQ_6	AL2	M_DATA_A6
M_MAA_A7	AU22	SA_MA_7	SA_DQ_7	AL1	M_DATA_A7
M_MAA_A8	AV22	SA_MA_8	SA_DQ_8	AN1	M_DATA_A8
M_MAA_A9	AT22	SA_MA_9	SA_DQ_9	AN4	M_DATA_A9
M_MAA_A10	AV28	SA_MA_10	SA_DQ_10	AR3	M_DATA_A10
M_MAA_A11	AU21	SA_MA_11	SA_DQ_11	AR4	M_DATA_A11
M_MAA_A12	AT21	SA_MA_12	SA_DQ_12	AN2	M_DATA_A12
M_MAA_A13	AW32	SA_MA_13	SA_DQ_13	AN3	M_DATA_A13
M_MAA_A14	AU20	SA_MA_14	SA_DQ_14	AR2	M_DATA_A14
M_MAA_A15	AT20	SA_MA_15	SA_DQ_15	AR1	M_DATA_A15
			SA_DQ_16	AV2	M_DATA_A16
M_WE_A_N	AW29	SA_WE#	SA_DQ_17	AW3	M_DATA_A17
M_CAS_A_N	AV30	SA_CAS#	SA_DQ_18	AV5	M_DATA_A18
M_RAS_A_N	AU28	SA_RAS#	SA_DQ_19	AW5	M_DATA_A19
			SA_DQ_20	AU2	M_DATA_A20
M_SBS_A0	AU29	SA_BS_0	SA_DQ_21	AL9	M_DATA_A21
M_SBS_A1	AW28	SA_BS_1	SA_DQ_22	AU5	M_DATA_A22
M_SBS_A2	AV20	SA_BS_2	SA_DQ_23	AY5	M_DATA_A23
			SA_DQ_24	AY7	M_DATA_A24
			SA_DQ_25	AU7	M_DATA_A25
M_SCS_A_N0	AU29	SA_CS#_0	SA_DQ_26	AV9	M_DATA_A26
M_SCS_A_N1	AV32	SA_CS#_1	SA_DQ_27	AU9	M_DATA_A27
	AW30	SA_CS#_2	SA_DQ_28	AV7	M_DATA_A28
	AU33	SA_CS#_3	SA_DQ_29	AW7	M_DATA_A29
			SA_DQ_30	AW9	M_DATA_A30
M_SCKE_A0	AV19	SA_CKE_0	SA_DQ_31	AY9	M_DATA_A31
M_SCKE_A1	AT19	SA_CKE_1	SA_DQ_32	AU35	M_DATA_A32
	AU18	SA_CKE_2	SA_DQ_33	AW37	M_DATA_A33
	AV18	SA_CKE_3	SA_DQ_34	AU39	M_DATA_A34
			SA_DQ_35	AU36	M_DATA_A35
M_ODT_A0	AV31	SA_ODT_0	SA_DQ_36	AW35	M_DATA_A36
M_ODT_A1	AU32	SA_ODT_1	SA_DQ_37	AY36	M_DATA_A37
	AU30	SA_ODT_2	SA_DQ_38	AU38	M_DATA_A38
	AW33	SA_ODT_3	SA_DQ_39	AU37	M_DATA_A39
			SA_DQ_40	AR40	M_DATA_A40
			SA_DQ_41	AR37	M_DATA_A41
			SA_DQ_42	AN38	M_DATA_A42
			SA_DQ_43	AN37	M_DATA_A43
CK_M_DDR0_A_DP	AY25	SA_CK_0	SA_DQ_44	AR39	M_DATA_A44
CK_M_DDR0_A_DN	AW25	SA_CK#_0	SA_DQ_45	AR38	M_DATA_A45
CK_M_DDR1_A_DP	AU24	SA_CK_1	SA_DQ_46	AN39	M_DATA_A46
CK_M_DDR1_A_DN	AU25	SA_CK#_1	SA_DQ_47	AN40	M_DATA_A47
	AW27	SA_CK_2	SA_DQ_48	AL40	M_DATA_A48
	AY27	SA_CK#_2	SA_DQ_49	AL37	M_DATA_A49
	AV26	SA_CK_3	SA_DQ_50	AJ38	M_DATA_A50
	AW26	SA_CK#_3	SA_DQ_51	AJ37	M_DATA_A51
			SA_DQ_52	AL39	M_DATA_A52
			SA_DQ_53	AL38	M_DATA_A53
			SA_DQ_54	AJ39	M_DATA_A54
			SA_DQ_55	AJ40	M_DATA_A55
			SA_DQ_56	AG40	M_DATA_A56
			SA_DQ_57	AG37	M_DATA_A57
			SA_DQ_58	AE38	M_DATA_A58
			SA_DQ_59	AE37	M_DATA_A59
			SA_DQ_60	AG39	M_DATA_A60
			SA_DQ_61	AG38	M_DATA_A61
			SA_DQ_62	AE39	M_DATA_A62
			SA_DQ_63	AE40	M_DATA_A63
	AV13	SA_DQS_8	SA_DQS_0	AK3	M_DQS_A_DP0
	AV12	SA_DQS#_8	SA_DQS_1	AP3	M_DQS_A_DP1
			SA_DQS_2	AW4	M_DQS_A_DP2
	AU12	SA_ECC_CB_0	SA_DQS_3	AV8	M_DQS_A_DP3
	AU14	SA_ECC_CB_1	SA_DQS_4	AV37	M_DQS_A_DP4
	AW13	SA_ECC_CB_2	SA_DQS_5	AP38	M_DQS_A_DP5
	AY13	SA_ECC_CB_3	SA_DQS_6	AK38	M_DQS_A_DP6
	AU13	SA_ECC_CB_4	SA_DQS_7	AF38	M_DQS_A_DP7
	AU11	SA_ECC_CB_5			
	AY12	SA_ECC_CB_6		AK2	M_DQS_A_DN0
	AW12	SA_ECC_CB_7	SA_DQS#_0	AP2	M_DQS_A_DN1
			SA_DQS#_1	AV4	M_DQS_A_DN2
			SA_DQS#_2	AW8	M_DQS_A_DN3
			SA_DQS#_3	AV36	M_DQS_A_DN4
			SA_DQS#_4	AP39	M_DQS_A_DN5
			SA_DQS#_5	AK39	M_DQS_A_DN6
			SA_DQS#_6	AF39	M_DQS_A_DN7
			SA_DQS#_7		

DDR_0

SAN-1U2NF

(62.10055.441)

DDR3_DRAMRST_N — 1 R152 2 0R0402-PAD — DDR3_DRAMRST_N-1 — AW18 — SM_DRAMRST#

(R) C100 SCD1U10V2KX-4GP

U7B — 2 OF 11 — SANDY BRIDGE

M_MAA_B0	AK24	SB_MA_0	SB_DQ_0	AG7	M_DATA_B0
M_MAA_B1	AM20	SB_MA_1	SB_DQ_1	AG8	M_DATA_B1
M_MAA_B2	AM19	SB_MA_2	SB_DQ_2	AJ8	M_DATA_B2
M_MAA_B3	AK18	SB_MA_3	SB_DQ_3	AJ8	M_DATA_B3
M_MAA_B4	AP19	SB_MA_4	SB_DQ_4	AG5	M_DATA_B4
M_MAA_B5	AP18	SB_MA_5	SB_DQ_5	AG6	M_DATA_B5
M_MAA_B6	AM18	SB_MA_6	SB_DQ_6	AJ6	M_DATA_B6
M_MAA_B7	AL18	SB_MA_7	SB_DQ_7	AJ7	M_DATA_B7
M_MAA_B8	AN18	SB_MA_8	SB_DQ_8	AL7	M_DATA_B8
M_MAA_B9	AY17	SB_MA_9	SB_DQ_9	AM7	M_DATA_B9
M_MAA_B10	AN23	SB_MA_10	SB_DQ_10	AM10	M_DATA_B10
M_MAA_B11	AU17	SB_MA_11	SB_DQ_11	AL10	M_DATA_B11
M_MAA_B12	AT18	SB_MA_12	SB_DQ_12	AL6	M_DATA_B12
M_MAA_B13	AP26	SB_MA_13	SB_DQ_13	AM6	M_DATA_B13
M_MAA_B14	AY16	SB_MA_14	SB_DQ_14	AL9	M_DATA_B14
M_MAA_B15	AV16	SB_MA_15	SB_DQ_15	AM9	M_DATA_B15
			SB_DQ_16	AP7	M_DATA_B16
M_WE_B_N	AR25	SB_WE#	SB_DQ_17	AR7	M_DATA_B17
M_CAS_B_N	AK25	SB_CAS#	SB_DQ_18	AP10	M_DATA_B18
M_RAS_B_N	AP24	SB_RAS#	SB_DQ_19	AR10	M_DATA_B19
			SB_DQ_20	AP5	M_DATA_B20
M_SBS_B0	AP23	SB_BS_0	SB_DQ_21	AR6	M_DATA_B21
M_SBS_B1	AM24	SB_BS_1	SB_DQ_22	AP9	M_DATA_B22
M_SBS_B2	AW17	SB_BS_2	SB_DQ_23	AR9	M_DATA_B23
			SB_DQ_24	AM12	M_DATA_B24
			SB_DQ_25	AM13	M_DATA_B25
M_SCS_B_N0	AN25	SB_CS#_0	SB_DQ_26	AR13	M_DATA_B26
M_SCS_B_N1	AN26	SB_CS#_1	SB_DQ_27	AP13	M_DATA_B27
	AL25	SB_CS#_2	SB_DQ_28	AL12	M_DATA_B28
	AT26	SB_CS#_3	SB_DQ_29	AL13	M_DATA_B29
			SB_DQ_30	AR12	M_DATA_B30
M_SCKE_B0	AU16	SB_CKE_0	SB_DQ_31	AP12	M_DATA_B31
M_SCKE_B1	AY15	SB_CKE_1	SB_DQ_32	AR28	M_DATA_B32
	AW15	SB_CKE_2	SB_DQ_33	AR29	M_DATA_B33
	AV15	SB_CKE_3	SB_DQ_34	AL28	M_DATA_B34
			SB_DQ_35	AL29	M_DATA_B35
M_ODT_B0	AL26	SB_ODT_0	SB_DQ_36	AP28	M_DATA_B36
M_ODT_B1	AP26	SB_ODT_1	SB_DQ_37	AP29	M_DATA_B37
	AM26	SB_ODT_2	SB_DQ_38	AM28	M_DATA_B38
	AK26	SB_ODT_3	SB_DQ_39	AM29	M_DATA_B39
			SB_DQ_40	AP32	M_DATA_B40
			SB_DQ_41	AP31	M_DATA_B41
			SB_DQ_42	AP35	M_DATA_B42
			SB_DQ_43	AP34	M_DATA_B43
			SB_DQ_44	AR32	M_DATA_B44
CK_M_DDR0_B_DP	AL21	SB_CK_0	SB_DQ_45	AR31	M_DATA_B45
CK_M_DDR0_B_DN	AL22	SB_CK#_0	SB_DQ_46	AR35	M_DATA_B46
CK_M_DDR1_B_DP	AL20	SB_CK_1	SB_DQ_47	AR34	M_DATA_B47
CK_M_DDR1_B_DN	AK20	SB_CK#_1	SB_DQ_48	AM32	M_DATA_B48
	AL23	SB_CK_2	SB_DQ_49	AM31	M_DATA_B49
	AM22	SB_CK#_2	SB_DQ_50	AL35	M_DATA_B50
	AP21	SB_CK_3	SB_DQ_51	AL32	M_DATA_B51
	AN21	SB_CK#_3	SB_DQ_52	AM34	M_DATA_B52
			SB_DQ_53	AL31	M_DATA_B53
			SB_DQ_54	AM35	M_DATA_B54
			SB_DQ_55	AL34	M_DATA_B55
			SB_DQ_56	AH35	M_DATA_B56
			SB_DQ_57	AH34	M_DATA_B57
			SB_DQ_58	AE34	M_DATA_B58
			SB_DQ_59	AE35	M_DATA_B59
			SB_DQ_60	AJ35	M_DATA_B60
			SB_DQ_61	AJ34	M_DATA_B61
			SB_DQ_62	AF33	M_DATA_B62
			SB_DQ_63	AF35	M_DATA_B63
	AN16	SB_DQS_8	SB_DQS_0	AH7	M_DQS_B_DP0
	AN15	SB_DQS#_8	SB_DQS_1	AM8	M_DQS_B_DP1
			SB_DQS_2	AR8	M_DQS_B_DP2
	AL16	SB_ECC_CB_0	SB_DQS_3	AN13	M_DQS_B_DP3
	AM16	SB_ECC_CB_1	SB_DQS_4	AN29	M_DQS_B_DP4
	AP16	SB_ECC_CB_2	SB_DQS_5	AP33	M_DQS_B_DP5
	AR16	SB_ECC_CB_3	SB_DQS_6	AL33	M_DQS_B_DP6
	AL15	SB_ECC_CB_4	SB_DQS_7	AG35	M_DQS_B_DP7
	AM15	SB_ECC_CB_5			
	AR15	SB_ECC_CB_6		AH6	M_DQS_B_DN0
	AP15	SB_ECC_CB_7	SB_DQS#_0	AL8	M_DQS_B_DN1
			SB_DQS#_1	AP8	M_DQS_B_DN2
			SB_DQS#_2	AN12	M_DQS_B_DN3
			SB_DQS#_3	AN28	M_DQS_B_DN4
			SB_DQS#_4	AR33	M_DQS_B_DN5
			SB_DQS#_5	AM33	M_DQS_B_DN6
			SB_DQS#_6	AG34	M_DQS_B_DN7
			SB_DQS#_7		

DDR_1

SAN-1U2NF

(62.10055.441)

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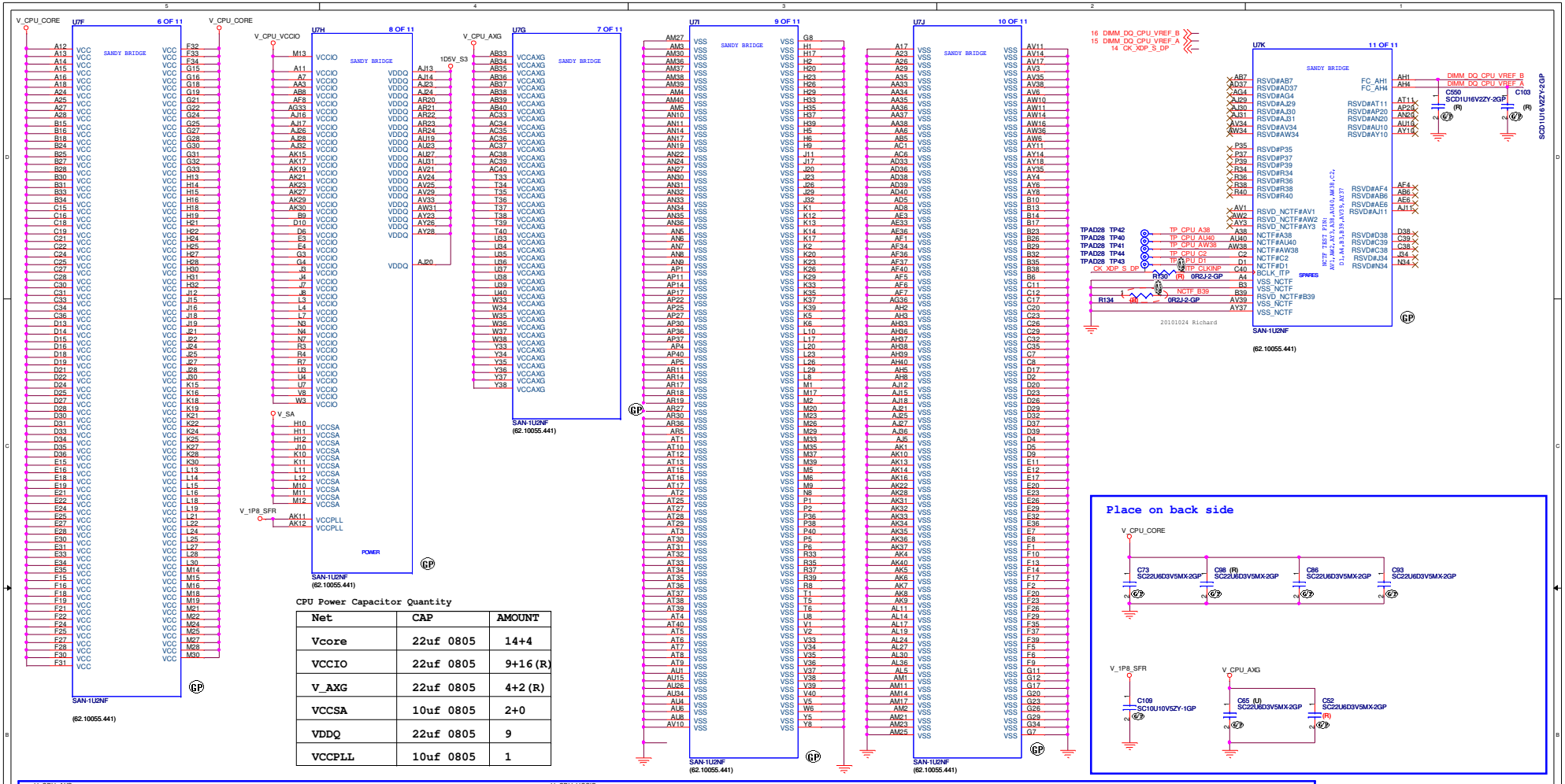
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU 3

Size: C | Document Number: Tahoe | Rev: SA

Date: Wednesday, March 30, 2011 | Sheet 12 of 62



CPU Power Capacitor Quantity

Net	CAP	AMOUNT
Vcore	22uf 0805	14+4
VCCIO	22uf 0805	9+16(R)
V_AXG	22uf 0805	4+2(R)
VCCSA	10uf 0805	2+0
VDDQ	22uf 0805	9
VCCPLL	10uf 0805	1

Wistron Incorporated	12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
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XDP(ITP) for CPU

17,44,59,60 CPU_CORE_PWRGD

10 H_TDO
10 H_TDI
10 H_TMS
10 H_TCK
10 H_TRST_N
10 H_CPURST_N
10 H_PREQ_N
10 H_PRDY_N
10,17 H_PWRGD
17,24 SIO_PWNBTN_N
10,17,24,51 PLT_RST_N

15,16,17,28,58 SMB_DATA_MAIN
15,16,17,28,58 SMB_CLK_MAIN

10,17 XDP_DBRESET_N

10 H_BPM#0
10 H_BPM#1
10 H_BPM#2
10 H_BPM#3
10 H_BPM#4
10 H_BPM#5
10 H_BPM#6
10 H_BPM#7

18 CK_100M_CPU_XDP_DN
18 CK_100M_CPU_XDP_DP

13 CK_XDP_S_DP
10 CK_XDP_S_DN

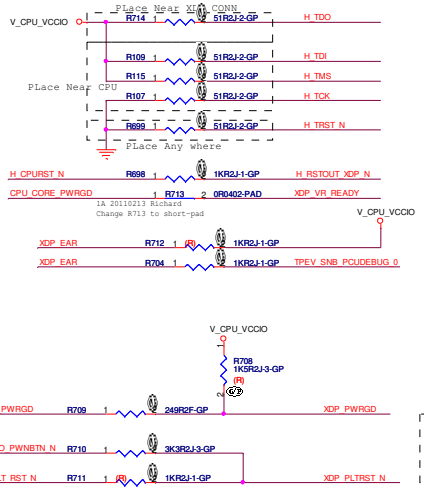
18 CK_PCH_33M_P80

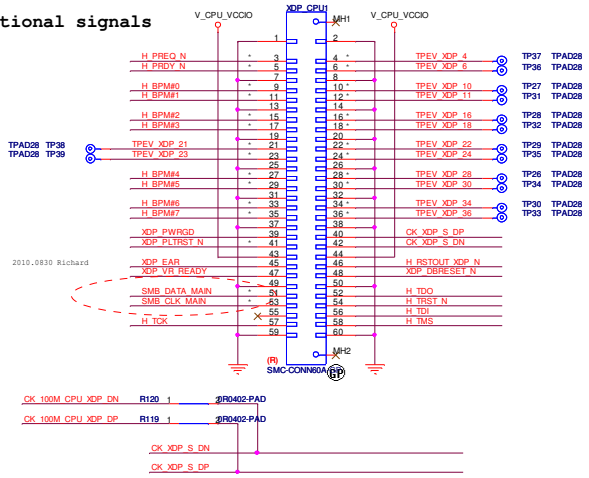
24 LPC_RST_N
17,24 LPC_LAD0
17,24 LPC_LAD1
17,24 LPC_LAD2
17,24 LPC_LAD3
17,24 LPC_LFRAME_N

10 TPEV_SNB_PCUDEBUG_0

* : Optional signals

XDP(ITP) for CPU



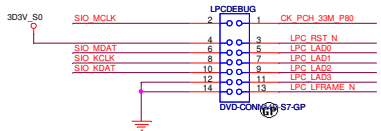


All parts can be placed at back side

LPC DEBUG PORT

24 SIO_MCLK
24 SIO_MDAT
24 SIO_KCLK
24 SIO_KDAT

SB 20101222 Richard
Combine SIO F/W PIN



Pin height 2.3mm

CRT Header for Debug

SB 20101219 Richard
Remove 0ohm

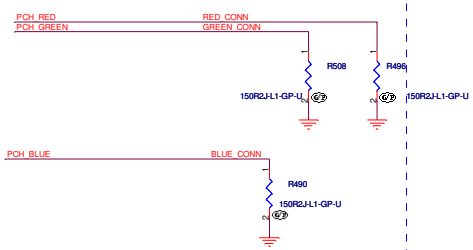
From PCH

19 PCH_HSYNC
19 PCH_VSYNC
19 PCH_DDCCLK
19 PCH_DDCDATA
19 PCH_RED
19 PCH_GREEN
19 PCH_BLUE

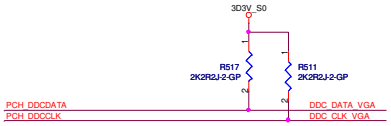
20101102 Richard
Remove MXM RGB

20101027 Richard
DEL DEBUG VGA DDC _CLK DATA

RGB



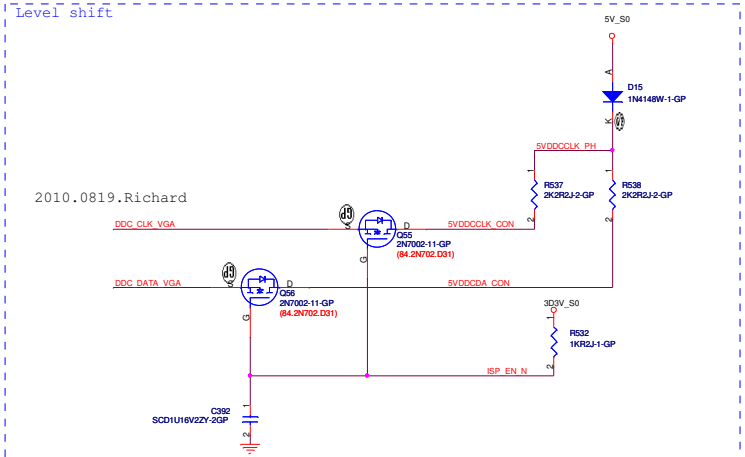
DDC



SYNC

2010.0908.Richard

Level shift



2010.0819.Richard

20101011 Richard
CRT Reserve TP

RED_CONN TP16 TPAD28
GREEN_CONN TP19 TPAD28
BLUE_CONN TP17 TPAD28
5VDDCCLK_CON TP23 TPAD28
5VDDCDA_CON TP21 TPAD28
VSYNC_3P3V TP20 TPAD28
HSYNC_3P3V TP18 TPAD28

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Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: XDP DEBUG

Size: C | Document Number: Tahoe | Rev: SA

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SSID = MEMORY

3D3V_S0 3D3V_S0
1D5V_S3 1D5V_S3
0D75V_S0 V_SM_VTT
20101010 Richard

DDR DATA
12 M_DATA_A[0..63]
12 M_DQS_A_DP[0..7]
12 M_DQS_A_DN[0..7]

DDR CMD/ADD
12 M_MAA_A[0..15]
12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

DDR CTRL
12 M_SCS_A_N0
12 M_SCS_A_N1
12 M_SCKE_A0
12 M_SCKE_A1
12 M_ODT_A0
12 M_ODT_A1

DDR CLOCK
12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

DDR OTHERS
12,16 DDR3_DRAMRST_N
14,16,17,28,58 SMB_DATA_MAIN
14,16,17,28,58 SMB_CLK_MAIN
13 DIMM_DQ_CPU_VREF_A

1D5V_S3
DIMM VREF OP1
R153 1KR2F-3-GP
C540 SCD1U16V2ZY-2GP (R)
DIMM_DQ_VREF_A_L R157 0R0402-PAD DIMM_DQ_VREF_A
C102 SCD1U10V2KX-4GP
R154 1KR2F-3-GP
DIMM_DQ_CPU_VREF_A R158 (R) 0R2J-2-GP

1D5V_S3
C511 SCD1U16V2ZY-2GP (R)
R724 1KR2F-3-GP
DIMM_CA_VREF_A_L R720 0R0402-PAD DIMM_CA_VREF_A
C503 SCD1U10V2KX-4GP
R723 1KR2F-3-GP

0D75V_S0
Place these caps close to VTT1 and VTT2.
C494 C490 C489 C493 C491 (R) SCD1U16D3V2KX-GP

DIMM2
M_MAA_A0 M_MAA_A1 M_MAA_A2 M_MAA_A3 M_MAA_A4 M_MAA_A5 M_MAA_A6 M_MAA_A7 M_MAA_A8 M_MAA_A9 M_MAA_A10 M_MAA_A11 M_MAA_A12 M_MAA_A13 M_MAA_A14 M_MAA_A15 M_SBS_A2
M_SBS_A0 M_SBS_A1
M_DATA_A0 … M_DATA_A63
M_DQS_A_DN0 … M_DQS_A_DN7
M_DQS_A_DP0 … M_DQS_A_DP7
M_ODT_A0 M_ODT_A1
DIMM_CA_VREF_A DIMM_DQ_VREF_A
12,16 DDR3_DRAMRST_N
0D75V_S0
NP1 NP2
M_RAS_A_N M_WE_A_N M_CAS_A_N
M_SCS_A_N0 M_SCS_A_N1
M_SCKE_A0 M_SCKE_A1
CK_M_DDR0_A_DP CK_M_DDR0_A_DN
CK_M_DDR1_A_DP CK_M_DDR1_A_DN
SMB_DATA_MAIN SMB_CLK_MAIN
TS#_DIMM0_1 16
SA0_DIM0 SA1_DIM0
1D5V_S3
DDR3-204P-55-GP (62.10017.N71)

2010.0830 Richard

SA0_DIM0
SA1_DIM0
R140 10KR2J-3-GP
R142 10KR2J-3-GP

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

3D3V_S0
SCD1U10V2KX-5GP C56 C499 (R) SC2D2U10V3KX-1GP

Thermal EVENT
TS#_DIMM0_1 R718 10KR2J-3-GP 3D3V_S0

SODIMM A DECOUPLING
1D5V_S3
TC13 E820U2D5VM-6-GP (R)
C530 C532 C509 (R) C534 C538 C542 (R) C504 (R) C506 (R) SC10U6D3V3MX-GP
C539 C543 C545 C510 SC1U18V2ZY-2LLGP SC2D2U16V3ZY-2LLGP

Layout Note:
Place these Caps near SO-DIMMA.

H=9.2mm REV

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Title: DIMM 1
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DDR DATA

12 M_DATA_B[0..63]
12 M_DQS_B_DP[0..7]
12 M_DQS_B_DN[0..7]

DDR CMD/ADD

12 M_MAA_B[0..15]
12 M_WE_B_N
12 M_CAS_B_N
12 M_RAS_B_N
12 M_SBS_B0
12 M_SBS_B1
12 M_SBS_B2

DDR CTRL

12 M_SCS_B_N0
12 M_SCS_B_N1
12 M_SCKE_B0
12 M_SCKE_B1
12 M_ODT_B0
12 M_ODT_B1

DDR CLOCK

12 CK_M_DDR0_B_DP
12 CK_M_DDR0_B_DN
12 CK_M_DDR1_B_DP
12 CK_M_DDR1_B_DN

DDR OTHERS

12,15 DDR3_DRAMRST_N

13 DIMM_DQ_CPU_VREF_B

14,15,17,26,58 SMB_DATA_MAIN
14,15,17,26,58 SMB_CLK_MAIN

SSID = MEMORY

DIMM VREF OP1

1D5V_S3
V_SM
R735 1KR2F-3-GP
C549 SCD1U16V2ZY-2GP (R)
DIMM_DQ_VREF_B_L
R733 0R0402-PAD
DIMM_DQ_VREF_B
C551 SCD1U10V2KX-4GP
R732 1KR2F-3-GP
DIMM_DQ_CPU_VREF_B
R734 (R) 0R2J-2-GP

1D5V_S3
V_SM
R722 1KR2F-3-GP
C505 SCD1U16V2ZY-2GP (R)
DIMM_CA_VREF_B_L
R721 0R0402-PAD
DIMM_CA_VREF_B
C507 SCD1U10V2KX-4GP
R719 1KR2F-3-GP

Place these caps close to VTT1 and VTT2.

0D75V_S0
C496 (R) SC1UKD3V2KX-GP
C497 SC1UKD3V2KX-GP
C495 (R) SC1UKD3V2KX-GP
C492 SC1UKD3V2KX-GP

DIMM1

M_MAA_B0	98	A0	
M_MAA_B1	97	A1	
M_MAA_B2	96	A2	
M_MAA_B3	95	A3	
M_MAA_B4	92	A4	
M_MAA_B5	91	A5	
M_MAA_B6	90	A6	
M_MAA_B7	86	A7	
M_MAA_B8	89	A8	
M_MAA_B9	85	A9	
M_MAA_B10	107	A10/AP	
M_MAA_B11	84	A11	
M_MAA_B12	83	A12	
M_MAA_B13	119	A13	
M_MAA_B14	80	A14	
M_MAA_B15	78	A15	
M_SBS_B2	79	A16/BA2	
M_SBS_B0	109	BA0	
M_SBS_B1	108	BA1	
M_DATA_B0	5	DQ0	
M_DATA_B1	7	DQ1	
M_DATA_B2	15	DQ2	
M_DATA_B3	17	DQ3	
M_DATA_B4	4	DQ4	
M_DATA_B5	6	DQ5	
M_DATA_B6	16	DQ6	
M_DATA_B7	18	DQ7	
M_DATA_B8	21	DQ8	
M_DATA_B9	23	DQ9	
M_DATA_B10	33	DQ10	
M_DATA_B11	35	DQ11	
M_DATA_B12	22	DQ12	
M_DATA_B13	24	DQ13	
M_DATA_B14	34	DQ14	
M_DATA_B15	36	DQ15	
M_DATA_B16	39	DQ16	
M_DATA_B17	41	DQ17	
M_DATA_B18	51	DQ18	
M_DATA_B19	53	DQ19	
M_DATA_B20	40	DQ20	
M_DATA_B21	42	DQ21	
M_DATA_B22	50	DQ22	
M_DATA_B23	52	DQ23	
M_DATA_B24	57	DQ24	
M_DATA_B25	59	DQ25	
M_DATA_B26	67	DQ26	
M_DATA_B27	69	DQ27	
M_DATA_B28	56	DQ28	
M_DATA_B29	58	DQ29	
M_DATA_B30	68	DQ30	
M_DATA_B31	70	DQ31	
M_DATA_B32	129	DQ32	
M_DATA_B33	131	DQ33	
M_DATA_B34	141	DQ34	
M_DATA_B35	143	DQ35	
M_DATA_B36	130	DQ36	
M_DATA_B37	132	DQ37	
M_DATA_B38	140	DQ38	
M_DATA_B39	142	DQ39	
M_DATA_B40	147	DQ40	
M_DATA_B41	149	DQ41	
M_DATA_B42	157	DQ42	
M_DATA_B43	159	DQ43	
M_DATA_B44	146	DQ44	
M_DATA_B45	148	DQ45	
M_DATA_B46	158	DQ46	
M_DATA_B47	160	DQ47	
M_DATA_B48	153	DQ48	
M_DATA_B49	165	DQ49	
M_DATA_B50	175	DQ50	
M_DATA_B51	177	DQ51	
M_DATA_B52	164	DQ52	
M_DATA_B53	166	DQ53	
M_DATA_B54	174	DQ54	
M_DATA_B55	176	DQ55	
M_DATA_B56	181	DQ56	
M_DATA_B57	183	DQ57	
M_DATA_B58	191	DQ58	
M_DATA_B59	193	DQ59	
M_DATA_B60	180	DQ60	
M_DATA_B61	182	DQ61	
M_DATA_B62	192	DQ62	
M_DATA_B63	194	DQ63	
M_DQS_B_DN0	10	DQS0#	
M_DQS_B_DN1	27	DQS1#	
M_DQS_B_DN2	45	DQS2#	
M_DQS_B_DN3	62	DQS3#	
M_DQS_B_DN4	135	DQS4#	
M_DQS_B_DN5	152	DQS5#	
M_DQS_B_DN6	169	DQS6#	
M_DQS_B_DN7	186	DQS7#	
M_DQS_B_DP0	12	DQS0	
M_DQS_B_DP1	29	DQS1	
M_DQS_B_DP2	47	DQS2	
M_DQS_B_DP3	64	DQS3	
M_DQS_B_DP4	137	DQS4	
M_DQS_B_DP5	154	DQS5	
M_DQS_B_DP6	171	DQS6	
M_DQS_B_DP7	188	DQS7	
M_ODT_B0	116	ODT0	
M_ODT_B1	120	ODT1	
DIMM_CA_VREF_B	126	VREF_CA	
DIMM_DQ_VREF_B	1	VREF_DQ	
DDR3_DRAMRST_N	30	RESET#	
0D75V_S0	203	VTT1	
	204	VTT2	

NP1 NP2

RAS# 110 M_RAS_B_N
WE# 113 M_WE_B_N
CAS# 115 M_CAS_B_N

CS0# 114 M_SCS_B_N0
CS1# 121 M_SCS_B_N1

CKE0 73 M_SCKE_B0
CKE1 74 M_SCKE_B1

CK0 101 CK_M_DDR0_B_DP
CK0# 103 CK_M_DDR0_B_DN

CK1 102 CK_M_DDR1_B_DP
CK1# 104 CK_M_DDR1_B_DN

DM0 11
DM1 28
DM2 46
DM3 63
DM4 136
DM5 153
DM6 170
DM7 187

SDA 200 SMB_DATA_MAIN
SCL 202 SMB_CLK_MAIN

EVENT# 198 TS#_DIMM0_1 15

VDDSPD 199

SA0 197 SA0_DIM1
SA1 201 SA1_DIM1

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2, 3, 8, 9, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 43, 44, 48, 49, 54, 55, 60, 61, 65, 66, 71, 72, 127, 128, 133, 134, 138, 139, 144, 145, 150, 151, 155, 156, 161, 162, 167, 168, 172, 173, 178, 179, 184, 185, 189, 190, 195, 196, 205, 206

DDR3-204P-47-GP
(62.10017.N91)

2010.0830 Richard

TS#_DIMM0_1(EVENT#)must be connected to ECE.(PH)

3D3V_S0
C498 SCD1U10V2KX-4GP
C500 DY SC2D2U10V3ZY-1-LL-GP

3D3V_S0
R716 10KR2J-3-GP
SA1_DIM1
SA0_DIM1
R717 10KR2J-3-GP

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

1D5V_S3
SODIMM B DECOUPLING
C528 (R) SCD1U06V3KX-GP
C516 (R) SCD1U06V3KX-GP
C519 SCD1U06V3KX-GP
C521 SCD1U06V3KX-GP
C527 SCD1U06V3KX-GP
C544 (R) SCD1U06V3KX-GP
C536 SCD1U06V3KX-GP
C513 (R) SCD1U06V3KX-GP
C522 SCD1U18V2ZY-2LLGP
C525 SCD1U18V2ZY-2LLGP
C526 SCD1U18V2ZY-2LLGP
C523 SCD1U18V2ZY-2LLGP

Layout Note:
Place these Caps near SO-DIMMB.

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

H=5.2mm REV

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Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: DIMM 2
Size: C
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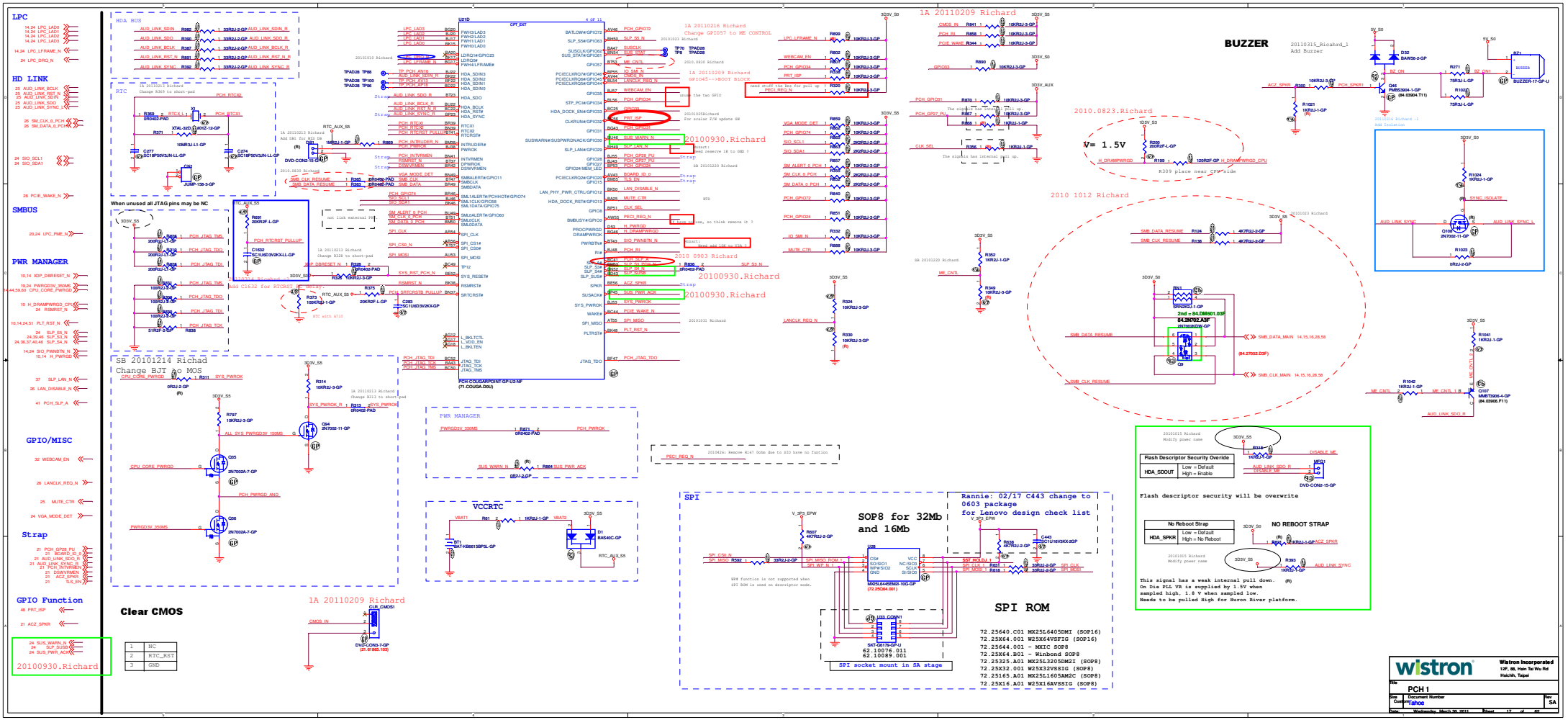

LPC
HD LINK
SMBUS
PWR MANAGER
GPIO/MISC
Strap
GPIO Function
HDA BUS
RTC
When unused all JTAG pins may be NC
SB 20101214 Richad
Change BJT to MOS
Clear CMOS
1A 20110209 Richard
1A 20110216 Richard
Change GPI057 to ME CONTROL
1A 20110209 Richard
GPIO45-->BOOT Block
20100930.Richard
2010 0903 Richard
20100930.Richard
20100930.Richard
2010.0823.Richard
V= 1.5V
2010 1012 Richard
BUZZER
20110315_Richard_1
Add Buzzer
SPI
SOP8 for 32Mb
and 16Mb
Rannie: 02/17 C443 change to
0603 package
for Lenovo design check list
SPI ROM
72.25640.C01 MX25L6405DMI (SOP16)
72.25x64.001 W25X64VSFIG (SOP16)
72.25644.001 - MXIC SOP8
72.25X64.B01 - Winbond SOP8
72.25325.A01 MX25L3205DM2I (SOP8)
72.25X32.001 W25X32VSSIG (SOP8)
72.25165.A01 MX25L1605AM2C (SOP8)
72.25X16.A01 W25X16AVSSIG (SOP8)
SPI socket mount in SA stage
Flash Descriptor Security Override
HDA_SDOUT
Low = Default
High = Enable
Flash descriptor security will be overwrite
No Reboot Strap
HDA_SPKR
Low = Default
High = No Reboot
NO REBOOT STRAP
This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled high for Huron River platform.
PCH_COUGARPOINT_GP_U2_NF
(71.COUGA.D0G)
Wistron Incorporated
19F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
PCH 1
Tahoe
SA
Wednesday, March 30, 2011

FDI

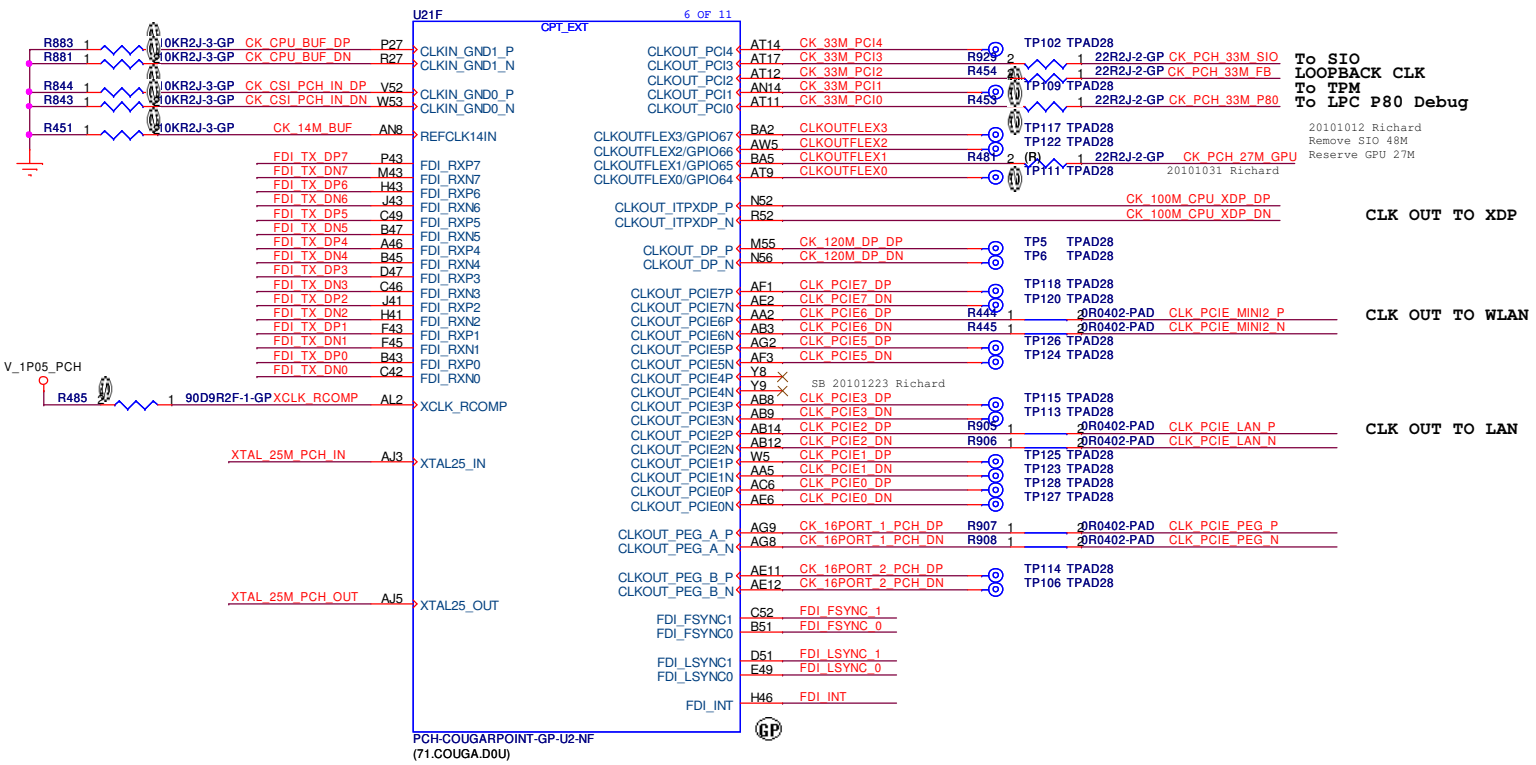
11 FDI_TX_DN[0..7]
11 FDI_TX_DP[0..7]
11 FDI_FSYNC_0
11 FDI_FSYNC_1
11 FDI_LSYNC_0
11 FDI_LSYNC_1
11 FDI_INT

PCI CLOCK

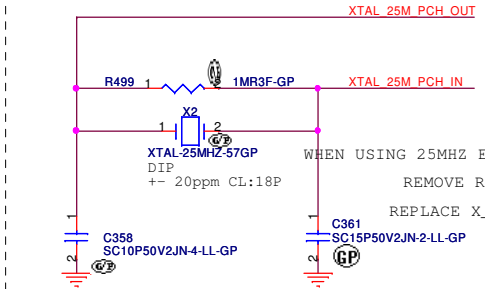
20 CK_PCH_33M_FB
14 CK_PCH_33M_P80
24 CK_PCH_33M_SIO

PCIE CLOCK

26 CLK_PCIE_LAN_P
26 CLK_PCIE_LAN_N
28 CLK_PCIE_MINI2_P
28 CLK_PCIE_MINI2_N
14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP
51 CLK_PCIE_PEG_P
51 CLK_PCIE_PEG_N
52 CK_PCH_27M_GPU



NOTE:The 1Mohm Damping Resistor
Use 0603 and Can't change to 0402!



When support FCIM need to stuff.

WHEN USING 25MHZ EXTERNAL REFERENCE FROM SINAI CMV:
REMOVE R63CK, Y5LB, C56LB
REPLACE X_in WITH 50OHM RES 0402 PACKAGE

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SATA

29 SATA_RXN0
29 SATA_RXP0
29 SATA_TXN0
29 SATA_TXP0

29 SATA_RXN1
29 SATA_RXP1
29 SATA_TXN1
29 SATA_TXP1

28 SATA_RXN3
28 SATA_RXP3
28 SATA_TXN3
28 SATA_TXP3

PCH_SATA_LED_N

17,24 PWRGD3V_350MS

41 PCH_MEPWROK

DP PORT B to SCALAR

61 SDVO_CTRLCLK
61 SDVO_CTRLDATA

47 PCH_B_HPD

VGA

14 PCH_HSYNC
14 PCH_VSYNC
14 PCH_RED
14 PCH_GREEN
14 PCH_BLUE
14 PCH_DDCDATA
14 PCH_DDCCLK

OTHERS

24 A20GATE
21 INIT3_3VB
24 KBRST_N
24 INT_SERIRQ
10 H_THERMTRIP_N
10,24 H_PECI
10 H_PM_SYNC_0

GPIO

32 TP_DET_N
33 CR_DET

28 WIFI_RF_EN

32 CAM_DET_N

Strap

21 BOARD_ID_1
21 SATA1GP
21 SATA2GP
21 SATA3GP

21 NVR_CLE

DP PORT D

61 PCH_D_HPD

61 PCH_CTRL_CLK
61 PCH_CTRL_DATA

SST

U21C
CPT_EXT
3 OF 11

SATA_RXP3
SATA_RXN3
SATA_RXP1
SATA_RXN1
SATA_RXP0
SATA_RXN0
SATARBIAS_PCH
SATA3COMP
CK_SATA_PCH_DP
CK_SATA_PCH_DN

RN2
SRN10KJ-5-GP

CLOCK TERMINATION FOR FCIM
Need to close PCH possiblely

SATA_TXP3
SATA_TXN3
SATA_TXP1
SATA_TXN1
SATA_TXP0
SATA_TXN0
SATARBIAS_PCH
SATA3COMP
PCH_SATA_LED_N
PCH_GPIO49
PCH_GPIO16
SATA3GP
SATA2GP
SATA1GP
WIFI_RF_EN
TP13
TP14
TP15
TP16
SATA3RBIAS
GPIO48
GPIO39
A20GATE
INIT3_3VB
RCIN#
SERIRQ
THRMTRIP#
PECI
PECI_PCH
PM_SYNC_0

2010/0422: use the 2 pin for usb_det function

TP71 TPAD28
TP76 TPAD28
TP75 TPAD28
TP69 TPAD28
R842 75R2F-GP

2010 0903 Richard
Have no WIFI

TPAD28 TP67
TPAD28 TP66
TPAD28 TP72
TP_CL_CLK
TP_CL_DATA1
TP_CL_RST1#
CL_CLK1
CL_DATA1
CL_RST1#

PWRGD3V_350MS
0R2J-2-GP
R299
PCH_MEPWROK_R
PCH_MEPWROK
R298
APWROK

PWM3
PWM2
PWM1
PWM0

TP_DET_N
CR_DET
TACH5
TACH4
TACH3
TACH2
TACH1
TACH0

TACH7/GPIO71
TACH6/GPIO70
TACH5/GPIO69
TACH4/GPIO68
TACH3/GPIO7
TACH2/GPIO6
TACH1/GPIO1
TACH0/GPIO17

SST
SCLOCK/GPIO22
SLOAD/GPIO38
NC#AY20

2010.1012Richard
Modify Net Name

3D3V_S0
R502 10KR2J-3-GP
CAM_DET_N
BOARD_ID_1
GPIO

1A Richard 0209
Add PH RESISTOR

PCH-COUGARPOINT-GP-U2-NF
(71.COUGA.D0U)

Pull-up on MB

3D3V_S0

TACH0 R395 10KR2J-3-GP
TACH1 R391 10KR2J-3-GP
TACH2 R892 10KR2J-3-GP
TACH3 R406 10KR2J-3-GP
TACH4 R399 10KR2J-3-GP
TACH5 R398 10KR2J-3-GP
CR_DET R396 10KR2J-3-GP
TP_DET_N R410 10KR2J-3-GP

PCH_SATA_LED_N R827 10KR2J-3-GP
PCH_GPIO49 R336 10KR2J-3-GP
PCH_GPIO16 R319 10KR2J-3-GP
WIFI_RF_EN R339 10KR2J-3-GP
GPIO48 R335 10KR2J-3-GP
GPIO39 R814 10KR2J-3-GP

A20GATE
2010/0422: TPAD28 have pulled up to VCC3 at SIO, so remove this
KBRST_N R805 10KR2J-3-GP
ITE suggest to pull-up to VCC3 !
INT_SERIRQ R839 10KR2J-3-GP

V_1P05_PCH
SATARBIAS_PCH 37D4R2F-GP R317
SATA3COMP 49D9R2F-GP R345

2010.0804 Richard
20101024 Richard

R449 PCH_B_HPD 10KR2J-3-GP PCH_B_HPD_C
PCH_D_HPD

20101007 Richard
Remove DP function

SB 20101201 Richard

Port D: Place near connector

61 PCH_HDMI_CLK+
61 PCH_HDMI_CLK-
61 PCH_HDMI_DATA0+
61 PCH_HDMI_DATA0-
61 PCH_HDMI_DATA1+
61 PCH_HDMI_DATA1-
61 PCH_HDMI_DATA2+
61 PCH_HDMI_DATA2-

SB 20101201 Richard

61 PCH_TMDS_CLKP
61 PCH_TMDS_CLKN
61 PCH_TMDS_00P
61 PCH_TMDS_00N
61 PCH_TMDS_01P
61 PCH_TMDS_01N
61 PCH_TMDS_02P
61 PCH_TMDS_02N

20101028 Richard
PCH DVI LEVEL SHIFT & AC CAP
Combine with MXM

U21E
CPT_EXT
5 OF 11

CRT_HSYNC
CRT_VSYNC
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_DDC_DATA
CRT_DDC_CLK
CRT_IRTN
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPD_CTRLCLK
DDPD_CTRLDATA
SDVO_CTRLCLK
SDVO_CTRLDATA
SDVO_INTP
SDVO_INTN
SDVO_STALLP
SDVO_STALLN
SDVO_TVCLKINP
SDVO_TVCLKINN
NVR_CLE

PCH_HSYNC
PCH_VSYNC
PCH_RED
PCH_GREEN
PCH_BLUE
PCH_DDCDATA
PCH_DDCCLK
HDMI_SCL_IN_INNAL
HDMI_SDA_IN_INNAL
PCH_CTRL_CLK
PCH_CTRL_DATA
SDVO_CTRLCLK
SDVO_CTRLDATA

R488 150R2F-1-GP
R450 150R2F-1-GP
R482 150R2F-1-GP
CLOSE TO PCH :<250 MIL TO PIN BALLS

TP101 TPAD28
TP104 TPAD28
TP105 TPAD28
TP103 TPAD28
TP112 TPAD28
TP108 TPAD28

2010.0819 Richard
2010.1028 Richard

PCH-COUGARPOINT-GP-U2-NF
(71.COUGA.D0U)

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PCI CLOCK LOOPBACK

18 CK_PCH_33M_FB

PWR Manager

Strap

21 P_GNT_N0
21 P_GNT_N1
21 P_GNT_N2
21 P_GNT_N3

24 LPC_PME_N

2010.0830 Richard
P_PCIRST_N

DMI

11 DMI_CPU_PCH_DN[0..3]
11 DMI_CPU_PCH_DP[0..3]
11 DMI_PCH_CPU_DN[0..3]
11 DMI_PCH_CPU_DP[0..3]

10 CK_DMI_BUF_CPU_DP
10 CK_DMI_BUF_CPU_DN

PCIE

26 PCIE_RXP1
26 PCIE_RXN1
26 PCIE_TXP1
26 PCIE_TXN1

28 PCIE_RXP2
28 PCIE_RXN2
28 PCIE_TXP2
28 PCIE_TXN2

USB

32 USB_PCH_DP0
32 USB_PCH_DN0

33 USB_PCH_DP1
33 USB_PCH_DN1

35 USB_PCH_DP2
35 USB_PCH_DN2
35 USB_PCH_DP3
35 USB_PCH_DN3
35 USB_PCH_DP4
35 USB_PCH_DN4
35 USB_PCH_DP5
35 USB_PCH_DN5

32 USB_PCH_DP8
32 USB_PCH_DN8

30 USB_PCH_DP9
30 USB_PCH_DN9

32 USB_PCH_DP10
32 USB_PCH_DN10

30 USB_PCH_DP11
30 USB_PCH_DN11

USB OC

30 USB_OC_9_11_N
35 USB_OC_45_N
35 USB_OC_23_N

U21A
CPT_EXT
1 OF 11

TPAD28 TP116 TP_BH8 BH6
P_DEVSEL_N BH9
CK_PCH_33M_FB BD15
P_IRDY_N BE11
24 LPC_PME_N AV15
P_SERR_N BR6
P_STOP_N BC12
P_PLOCK_N BA17
P_TRDY_N BC8
P_PERR_N BM3
P_FRAME_N BC11

P_GNT_N3 BE2
P_GNT_N2 BU12
P_GNT_N1 AV8
P_GNT_N0 BA15

P_REQ_N3 AV11
P_REQ_N2 BK8
P_REQ_N1 BT5
P_REQ_N0 BG5

P_INTA_N BK10
P_INTB_N BJ5
P_INTC_N BM15
P_INTD_N BP5
P_INTE_N BN8
P_INTF_N AV9
P_INTG_N BT15
P_INTH_N BR4

TPAD28 TP98 TP1 P22
TPAD28 TP86 TP2 L31
VGA_DACREFSET AT3
TPAD28 TP82 TP3 L33
TPAD28 TP77 TP4 M38
TPAD28 TP61 TP5 L36

R25 VSS
P25 VSS
R36 VSS
P36 VSS
AL43 VSS
AL44 VSS

3D3V_S0
R918 10KR2J-3-GP
TPAD28 TP92 P_PCIRST_N AV14
TP11 BA27
A54
A52
F57
D57

TPAD28 TP80 TP18 AY36
TPAD28 TP83 TP17 BA36

TPAD28 TP110 TP20 Y12
TPAD28 TP107 TP19 Y14

PCH-COUGARPOINT-GP-U2-NF
(71.COUGA.D0U)

PIRQA# AD31
PIRQB# AD30
PIRQC# AD29
PIRQD# AD28
PIRQE#/GPIO2 AD27
PIRQF#/GPIO3 AD26
PIRQG#/GPIO4 AD25
PIRQH#/GPIO5 AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0

GNT3#/GPIO55 BK12
GNT2#/GPIO53 AV12
GNT1#/GPIO51 BF8
GNT0# BA8
BF9
BA9
BM13
REQ3#/GPIO54 BC2
REQ2#/GPIO52 BL4
REQ1#/GPIO50 BC4
REQ0# BL2
BA14
BT11
BC6
BG15
BE6
BE4
BN2
BF3
BM8
BJ10
BR9
BJ3
BR12
BU8
BJ12
BN1
BG12
BT13
BT7
BF17
BF15
TP1 BP13
TP2 BG2
DAC_IREF BP7
TP3 BN4
TP4 C/BE1#
TP5 C/BE0#

TP10 BM46 TP10 TP73 TPAD28
DCPRTC_NCTF BT56 DCPRTC_NCTF
C708 SCD1U16V2ZY-2GP

Layout Note: Near PCI Slot
3D3V_S0
P_DEVSEL_N R439 8K2R2J-3-GP
P_IRDY_N R441 8K2R2J-3-GP
P_SERR_N R430 8K2R2J-3-GP
P_STOP_N R459 8K2R2J-3-GP
P_PLOCK_N R486 8K2R2J-3-GP
P_TRDY_N R452 8K2R2J-3-GP
P_PERR_N R456 8K2R2J-3-GP
P_FRAME_N R458 8K2R2J-3-GP

P_INTA_N R413 8K2R2J-3-GP
P_INTB_N R457 8K2R2J-3-GP
P_INTC_N R414 8K2R2J-3-GP
P_INTD_N R418 8K2R2J-3-GP
P_INTE_N R419 8K2R2J-3-GP
P_INTF_N R501 8K2R2J-3-GP
P_INTG_N R405 8K2R2J-3-GP
P_INTH_N R437 8K2R2J-3-GP

Layout Note: Near PCI Slot
P_REQ_N0 R455 8K2R2J-3-GP
P_REQ_N1 R429 8K2R2J-3-GP
P_REQ_N2 R420 8K2R2J-3-GP
P_REQ_N3 R498 8K2R2J-3-GP

Layout Note: Near PCI Slot
VGA_DACREFSET R472 1KR2F-3-GP
CLOSE TO PCH AT3 pin:<500 MIL

V_1P05_PCH
DMICOMP R385 49D9R2F-GP

DMI/PCIE/USB

U21B
CPT_EXT
2 OF 11

DMI_CPU_PCH_DP3 F38
DMI_CPU_PCH_DN3 E37
DMI_CPU_PCH_DP2 C36
DMI_CPU_PCH_DN2 B37
DMI_CPU_PCH_DP1 B35
DMI_CPU_PCH_DN1 A36
DMI_CPU_PCH_DP0 B33
DMI_CPU_PCH_DN0 D33
DMICOMP E31
DMI_ZCOMP
DMI_IRCOMP B31 DMICOMP

DMI3RXP
DMI3RXN
DMI2RXP
DMI2RXN
DMI1RXP
DMI1RXN
DMI0RXP
DMI0RXN

DMI3TXP P41 DMI_PCH_CPU_DP3
DMI3TXN M41 DMI_PCH_CPU_DN3
DMI2TXP J38 DMI_PCH_CPU_DP2
DMI2TXN H38 DMI_PCH_CPU_DN2
DMI1TXP R38 DMI_PCH_CPU_DP1
DMI1TXN P38 DMI_PCH_CPU_DN1
DMI0TXP H36 DMI_PCH_CPU_DP0
DMI0TXN J36 DMI_PCH_CPU_DN0

RN9 SRN10KJ-5-GP
CK_DMI_PCH_DP R33
CK_DMI_PCH_DN P33
CLKIN_DMI_P
CLKIN_DMI_N
CLOCK TERMINATION FOR FCIM
Need to close PCH possiblely

CLKOUT_DMI_P R31 CK_DMI_BUF_DP R880 2DR0402-PAD CK_DMI_BUF_CPU_DP
CLKOUT_DMI_N P31 CK_DMI_BUF_DN R882 2DR0402-PAD CK_DMI_BUF_CPU_DN
CLK OUT TO CPU for DMI

PERP8 J10
PERN8 H10
PERP7 H12
PERN7 J12
PERP6 L15
PERN6 J15
PERP5 M15
PERN5 N15
PERP4 M17
PERN4 P17
PERP3 J17
PERN3 H17
PERP2 R20
PERN2 P20
PERP1 L20
PERN1 J20

PETP8 D13
PETN8 B13
PETP7 F13
PETN7 E15
PETP6 B15
PETN6 A16
PETP5 C16
PETN5 B17
PETP4 E17
PETN4 F18
PETP3 B21
PETN3 E21
PETP2 A22 PCIE_TXP2_C SCD1U10V2KX-4GP C804 PCIE_TXP2 FOR WLAN
PETN2 C22 PCIE_TXN2_C SCD1U10V2KX-4GP C803 PCIE_TXN2
PETP1 F23 PCIE_TXP1_C SCD1U10V2KX-4GP C777 PCIE_TXP1 FOR LAN
PETN1 F25 PCIE_TXN1_C SCD1U10V2KX-4GP C775 PCIE_TXN1

FOR WLAN
FOR LAN
PCIE_RXP2
PCIE_RXN2
PCIE_RXP1
PCIE_RXN1

20110318 Richard -1
Modify PH power to S5

TPAD28 TP97 TP28 J22 TP28
TPAD28 TP95 TP24 L22 TP24
TPAD28 TP89 TP27 L25 TP27
TPAD28 TP91 TP23 J25 TP23
TPAD28 TP87 TP26 L27 TP26
TPAD28 TP90 TP22 J27 TP22
TPAD28 TP84 TP25 J31 TP25
TPAD28 TP9 TP21 H31 TP21

TP32 B25 TP32 TP99 TPAD28
TP31 C26 TP31 TP93 TPAD28
TP30 F28 TP30 TP94 TPAD28
TP29 C29 TP29 TP10 TPAD28

TP36 D25 TP36 TP14 TPAD28
TP35 B27 TP35 TP12 TPAD28
TP34 E27 TP34 TP13 TPAD28
TP33 E29 TP33 TP11 TPAD28

3D3V_S5
R1038 10KR2J-3-GP USB_OC_UN2
USB_OC_9_11_N BM45
USB_OC_UN1 BT46
R1039 10KR2J-3-GP BJ41
BP43
BK43
BG41
USB_OC_45_N BD41
USB_OC_23_N BM43

OC7#/GPIO14
OC6#/GPIO10
OC5#/GPIO9
OC4#/GPIO43
OC3#/GPIO42
OC2#/GPIO41
OC1#/GPIO40
OC0#/GPIO59

SB 20101218 Richard

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USBP13P BK27
USBP13N BJ27
USBP12P BD27
USBP12N BF27
USBP11P BK31 USB_PCH_DP11
USBP11N BJ31 USB_PCH_DN11
USBP10P BJ25 USB_PCH_DP10
USBP10N BK25 USB_PCH_DN10
USBP9P BT27 USB_PCH_DP9
USBP9N BR26 USB_PCH_DN9
USBP8P BR29 USB_PCH_DP8
USBP8N BN27 USB_PCH_DN8
USBP7P BD31
USBP7N BF31
USBP6P BJ33
USBP6N BK33
USBP5P BM30 USB_PCH_DP5
USBP5N BN29 USB_PCH_DN5
USBP4P BT31 USB_PCH_DP4
USBP4N BR32 USB_PCH_DN4
USBP3P BU32 USB_PCH_DP3
USBP3N BT33 USB_PCH_DN3
USBP2P BM35 USB_PCH_DP2
USBP2N BM33 USB_PCH_DN2
USBP1P BA33 USB_PCH_DP1
USBP1N BC33 USB_PCH_DN1
USBP0P BD36 USB_PCH_DP0
USBP0N BF36 USB_PCH_DN0

Port 10,11,12 FOR SIDE USB
Port 9 FOR TOUCH PANEL BOARD
Port 8 FOR WEBCAM
Port 2,3,4,5 FOR REAL USB
Port 1 FOR CR
Port 0 FOR touch

SB 20101221 Richard
R386 22D6R2F-L1-GP
BM25 USBRBIAS_PCH
BP25
USBRBIAS
USBRBIAS#

USBRBIAS (R63LB): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

RBIAS_PHY (R211LB): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

BF38 CK_96M_PCH_DP
BD38 CK_96M_PCH_DN
RN8 SRN10KJ-5-GP
CLKIN_DOT_96P
CLKIN_DOT_96N
R377 750R2F-GP
A32 RBIAS_CPY
DMI2RBIAS

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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

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6' serial straping define

PCH Functional Straps

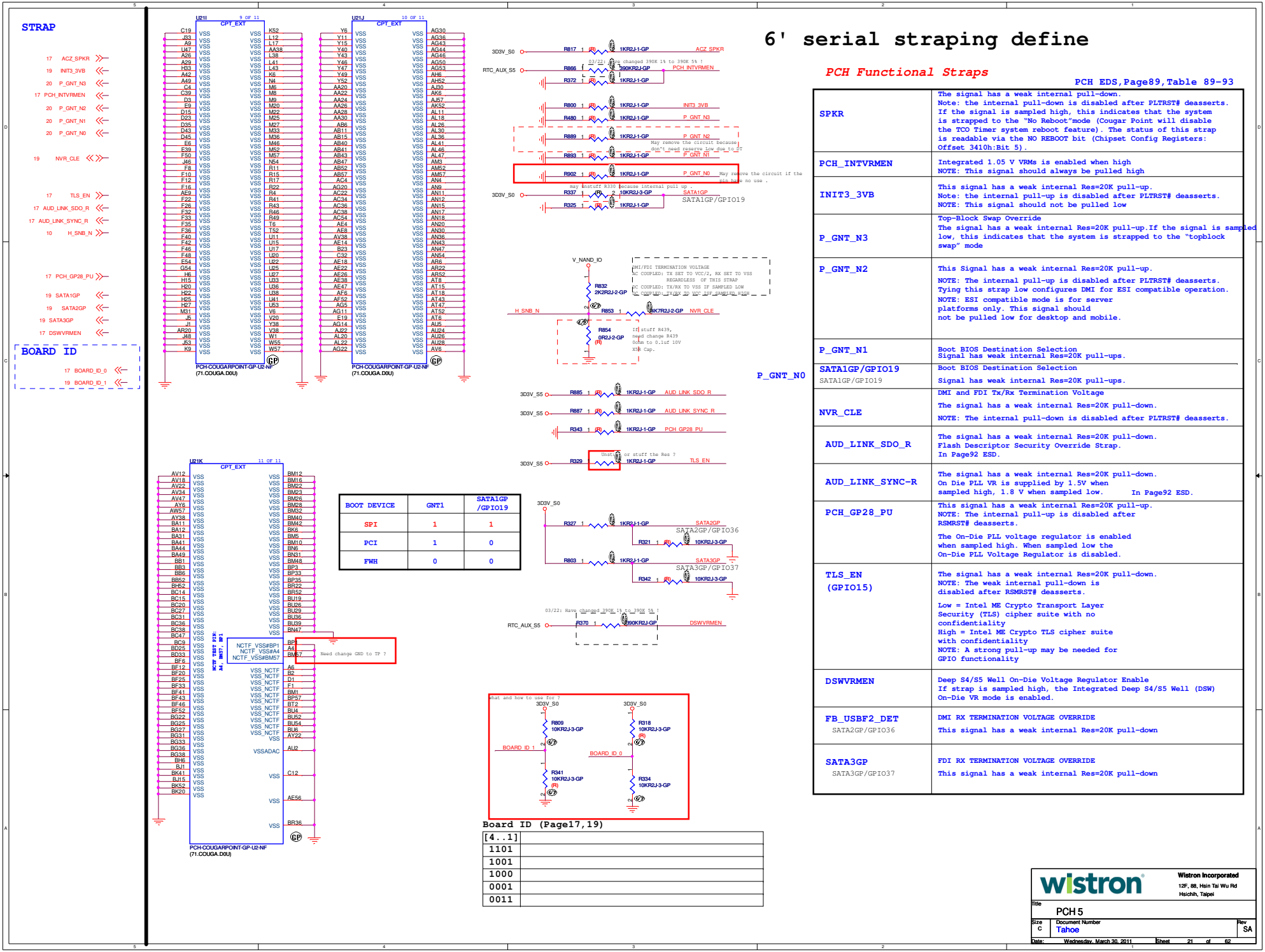
PCH EDS,Page89,Table 89-93

SPKR	The signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot"mode (Cougar Point will disable the TCO Timer system reboot feature). The status of this strap is readable via the NO REBOOT bit (Chipset Config Registers: Offset 3410h:Bit 5).
PCH_INTVRMEN	Integrated 1.05 V VRMs is enabled when high NOTE: This signal should always be pulled high
INIT3_3VB	This signal has a weak internal Res=20K pull-up. Note: the internal pull-up is disabled after PLTRST# deasserts. NOTE: This signal should not be pulled low
P_GNT_N3	Top-Block Swap Override The signal has a weak internal Res=20K pull-up.If the signal is sampled low, this indicates that the system is strapped to the "topblock swap" mode
P_GNT_N2	This Signal has a weak internal Res=20K pull-up. NOTE: The internal pull-up is disabled after PLTRST# deasserts. Tying this strap low configures DMI for ESI compatible operation. NOTE: ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
P_GNT_N1	Boot BIOS Destination Selection Signal has weak internal Res=20K pull-ups.
SATA1GP/GPIO19 SATA1GP/GPIO19	Boot BIOS Destination Selection Signal has weak internal Res=20K pull-ups.
NVR_CLE	DMI and FDI Tx/Rx Termination Voltage The signal has a weak internal Res=20K pull-down. NOTE: The internal pull-down is disabled after PLTRST# deasserts.
AUD_LINK_SDO_R	The signal has a weak internal Res=20K pull-down. Flash Descriptor Security Override Strap. In Page92 ESD.
AUD_LINK_SYNC-R	The signal has a weak internal Res=20K pull-down. On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low. In Page92 ESD.
PCH_GP28_PU	This signal has a weak internal Res=20K pull-up. NOTE: The internal pull-up is disabled after RSMRST# deasserts. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.
TLS_EN (GPIO15)	The signal has a weak internal Res=20K pull-down. NOTE: The weak internal pull-down is disabled after RSMRST# deasserts. Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel ME Crypto TLS cipher suite with confidentiality NOTE: A strong pull-up may be needed for GPIO functionality
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
FB_USBF2_DET SATA2GP/GPIO36	DMI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal Res=20K pull-down
SATA3GP SATA3GP/GPIO37	FDI RX TERMINATION VOLTAGE OVERRIDE This signal has a weak internal Res=20K pull-down

BOOT DEVICE	GNT1	SATA1GP /GPIO19
SPI	1	1
PCI	1	0
FWH	0	0

Board ID (Page17,19)

[4..1]	
1101	
1001	
1000	
0001	
0011	



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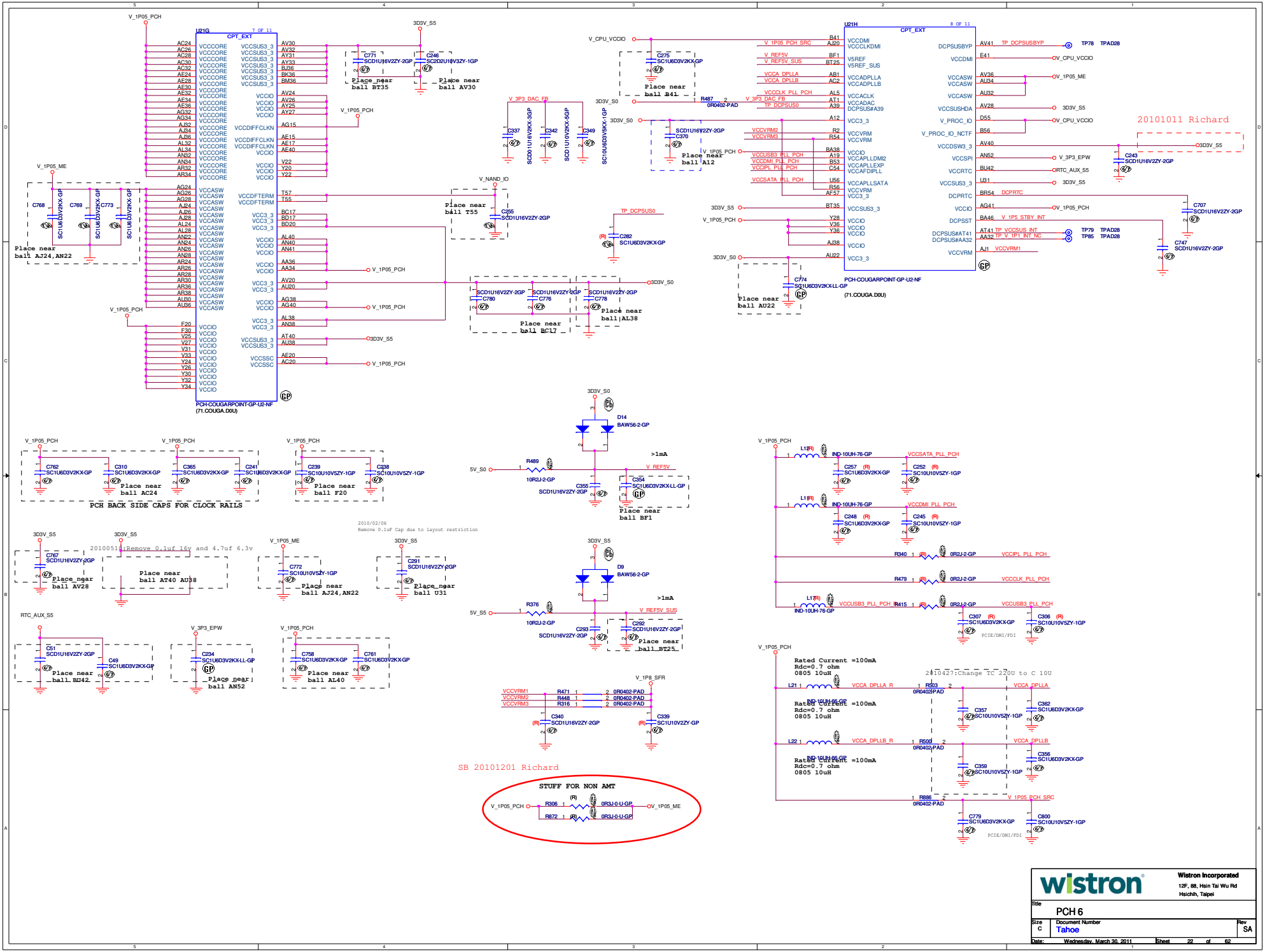
U21G
CPT_EXT
7 OF 11
PCH-COUGARPOINT-GP-U2-NF
(71.COUGA.D0U)
U21H
8 OF 11
PCH-COUGARPOINT-GP-U2-NF
(71.COUGA.D0U)
V_1P05_PCH
3D3V_S5
V_1P05_ME
V_NAND_IO
V_3P3_DAC_FB
V_CPU_VCCIO
3D3V_S0
TP_DCPSUS0
20101011 Richard
PCH BACK SIDE CAPS FOR CLOCK RAILS
20100511:Remove 0.1uf 16v and 4.7uf 6.3v
2010/02/05
Remove 0.1uF Cap due to layout restriction
SB 20101201 Richard
STUFF FOR NON AMT
20101027:Change TC 220U to C 10U
Rated Current =100mA
Rdc=0.7 ohm
0805 10uH
PCIE/DMI/FDI
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
PCH 6
Tahoe
Wednesday, March 30, 2011
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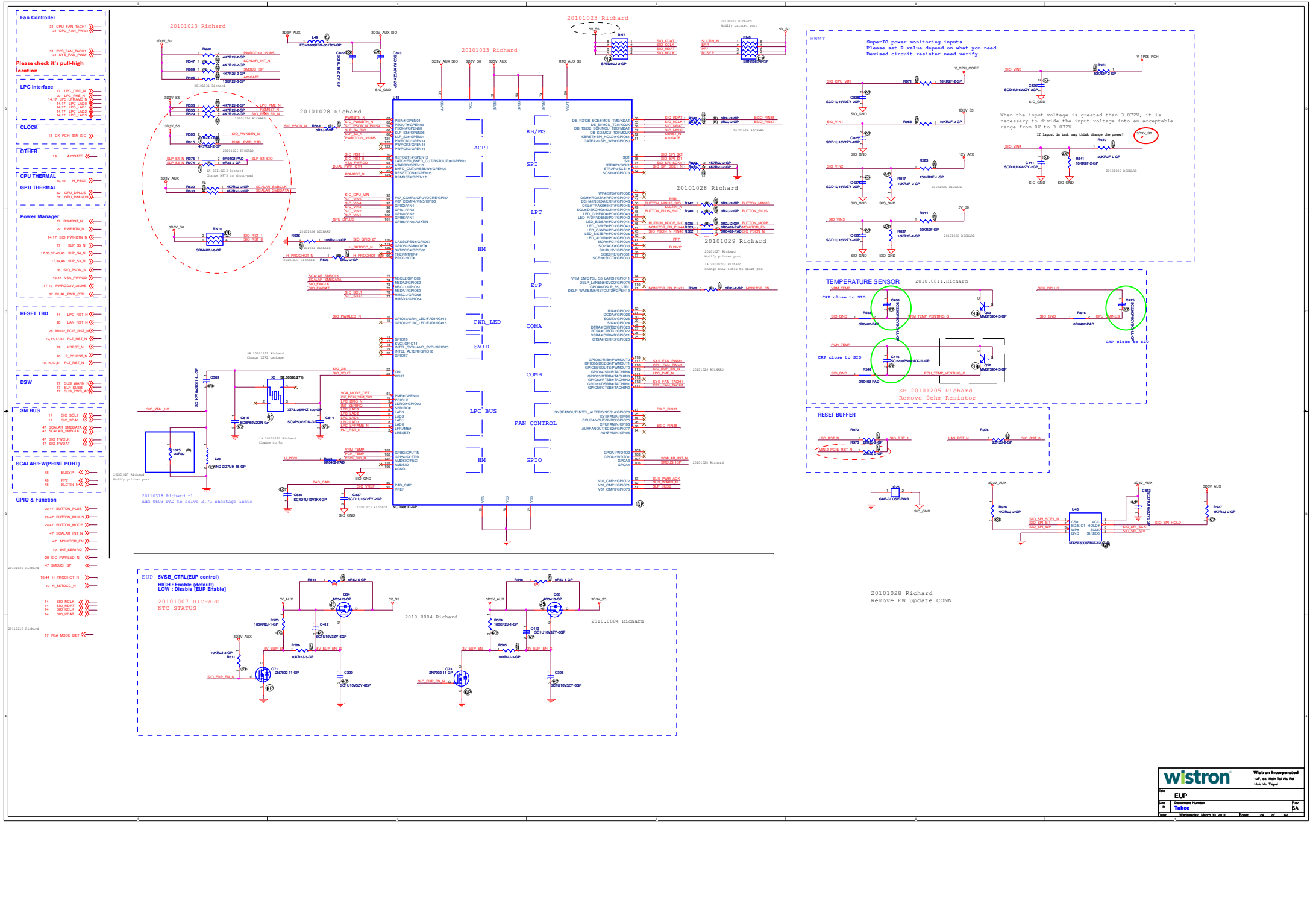
wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SIO

Size: D | Document Number: Tahoe | Rev: SA

Date: Wednesday, March 30, 2011 | Sheet 23 of 62


Fan Controller
Please check it's pull-high location
LPC interface
CLOCK
OTHER
CPU THERMAL
GPU THERMAL
Power Manager
RESET TBD
DSW
SM BUS
SCALAR/FW(PRINT PORT)
GPIO & Function
20101023 Richard
20101028 Richard
20101029 Richard
ACPI
KB/MS
SPI
LPT
HM
ErP
PWR_LED
COMA
SVID
COMB
LPC BUS
FAN CONTROL
GPIO
NCT6683D-GP
HWMT
SuperIO power monitoring inputs
Please set R value depend on what you need.
Devised circuit resister need verify.
When the input voltage is greated than 3.072V, it is necessary to divide the input voltage into an acceptable range from 0V to 3.072V.
TEMPERATURE SENSOR
2010.0811.Richard
SB 20101205 Richard
Remove 0ohm Resistor
RESET BUFFER
EUP 5VSB_CTRL(EUP control)
HIGH : Enable (default)
LOW : Disable (EUP Enable)
20101007 RICHARD
NTC STATUS
2010.0804 Richard
20101028 Richard
Remove FW update CONN
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
EUP
Size D
Document Number
Tahoe
Rev SA
Date: Wednesday, March 30, 2011
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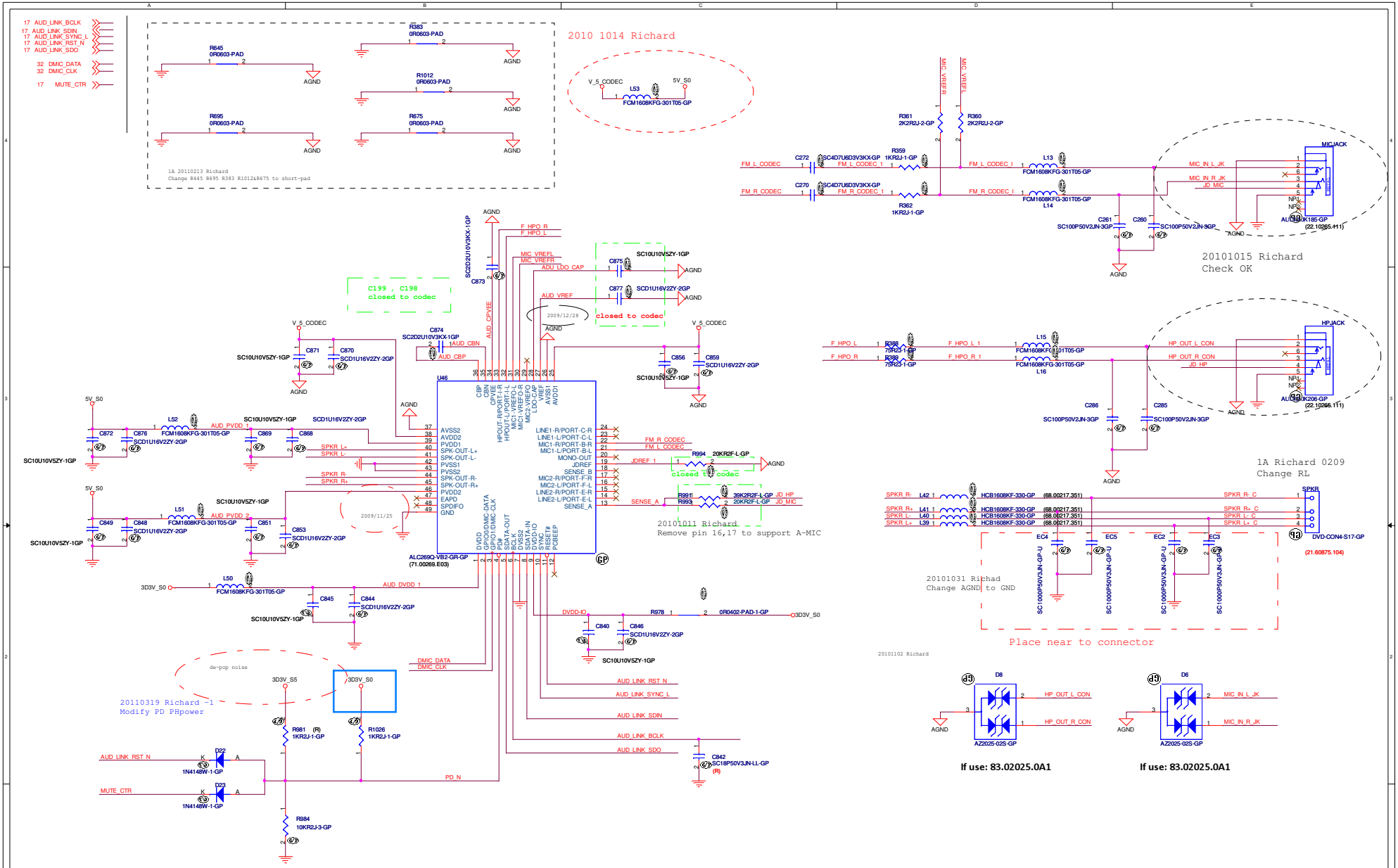
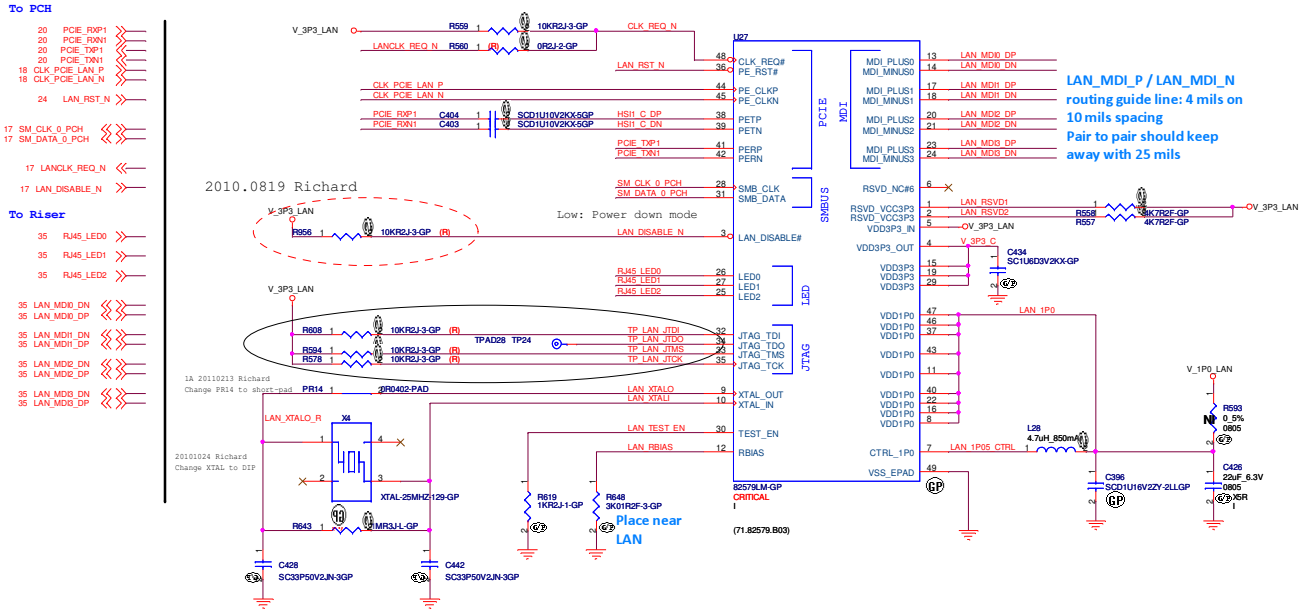
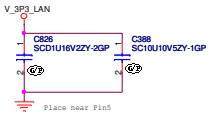
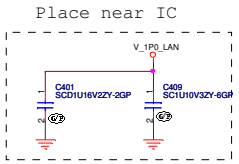
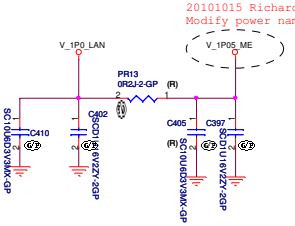


wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: AUDIO		
Size: C	Document Number: Tahoe	Rev: SA
Date: Wednesday, March 30, 2011	Sheet 25 of 62	

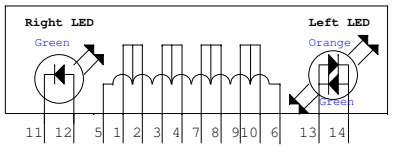








Layout note
Keep LAN chip at least 1" from the RJ45



	Giga	100	10
Left LED / Link	Orange	Green	X
Right LED / Act	Blink	Blink	Blink

wistron	Wistron Incorporated	12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	GIGA LAN	
Size C	Document Number Tahoe	Rev SA
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wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei
Title	RESERVE
Size: C	Document Number: Tahoe
Rev: SA	
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Mini PCI-E Connector

WLAN

20 PCIE_RXP2
20 PCIE_RXN2
20 PCIE_TXP2
20 PCIE_TXN2

18 CLK_PCIE_MINI2_P
18 CLK_PCIE_MINI2_N

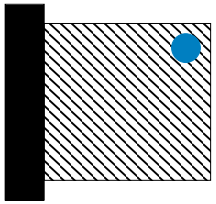
24 MINI2_PCIE_RST_N

SMBUS

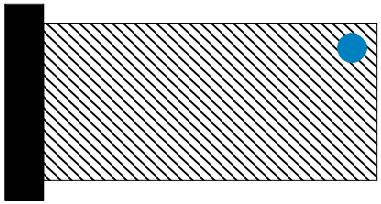
14,15,16,17,58 SMB_DATA_MAIN
14,15,16,17,58 SMB_CLK_MAIN

20,33 USB_PCH_DP1
20,33 USB_PCH_DN1

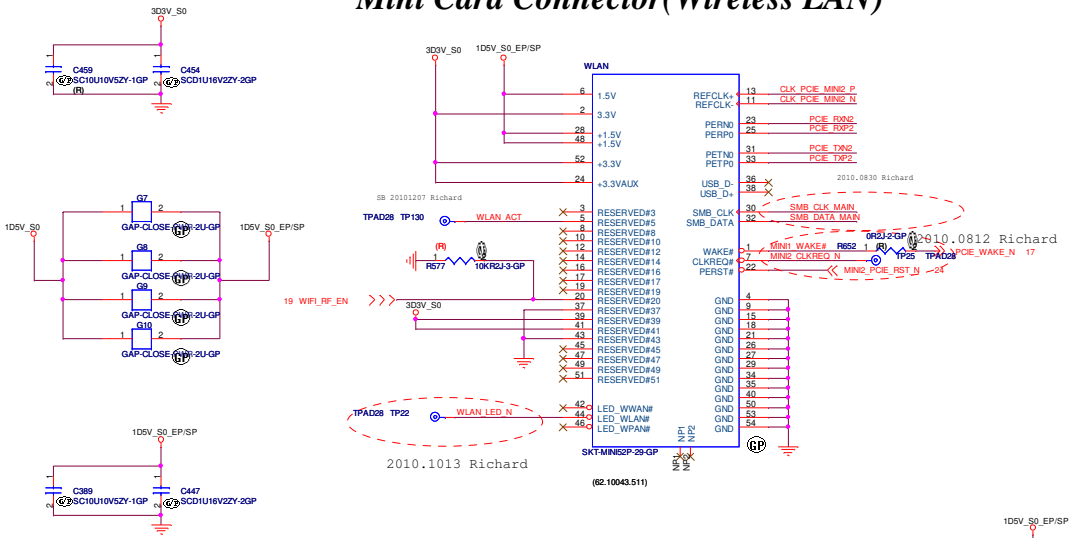
Half_Mini PCI-E CARD



Full_Mini PCI-E CARD

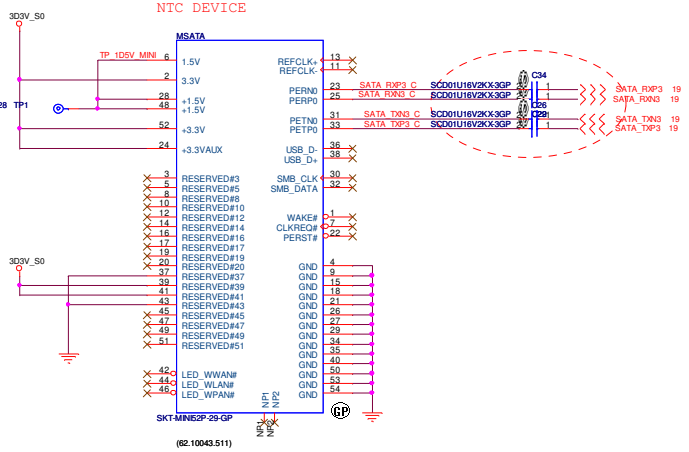


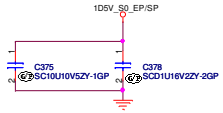
Mini Card Connector(Wireless LAN)

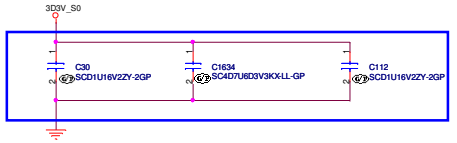


Mini Card Connector(mSATA SSD)

20101011 Richard
NTC DEVICE

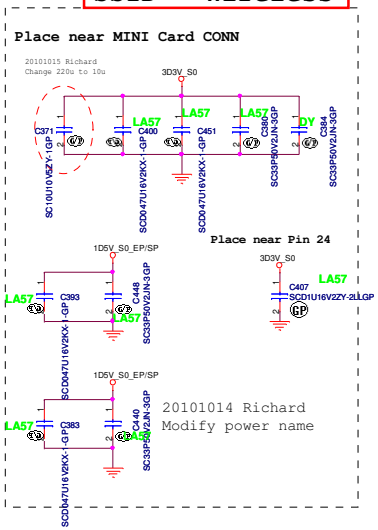






SSID = Wireless

Place near MINI Card CONN



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: MINI PCIE

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POWER_BTN to SIO

24 PWRBTN_N
24 SIO_PWRLED_N

BUTTON key to SCALAR

24,47 BUTTON_PLUS
24,47 BUTTON_MINUS
24,47 BUTTON_MODE

PCH SATA

19 SATA_RXN0
19 SATA_RXP0
19 SATA_TXN0
19 SATA_TXP0

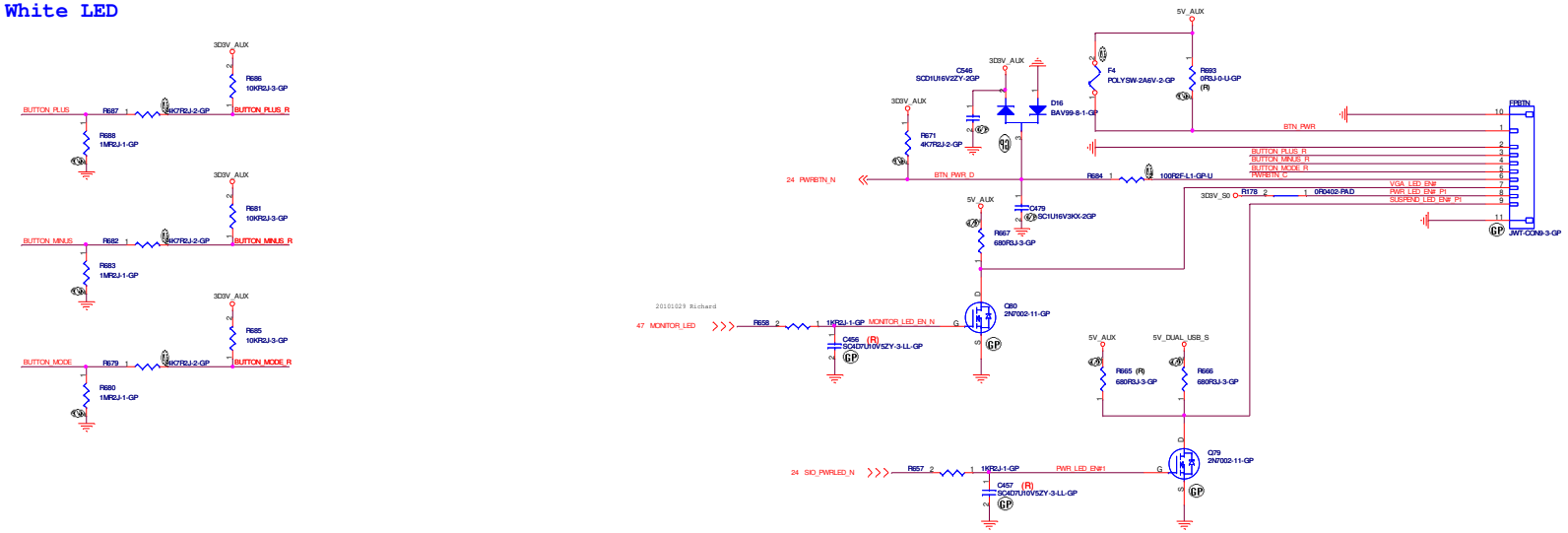
19 SATA_RXN1
19 SATA_RXP1
19 SATA_TXN1
19 SATA_TXP1

47 MONITOR_LED

20101029 Richard

PWRBTN BUTTON with White LED

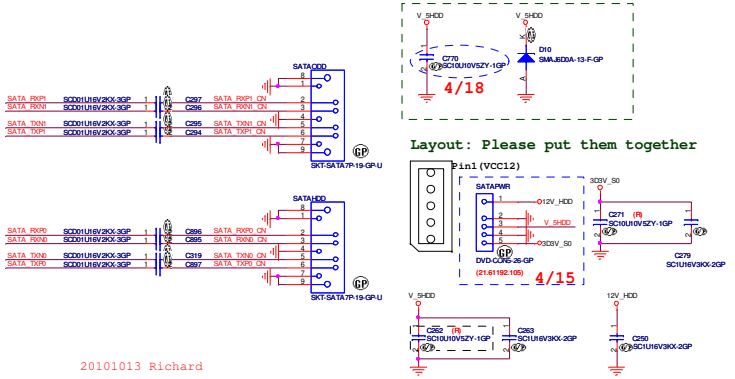
20101021 Richard



SATA CONNECTORS

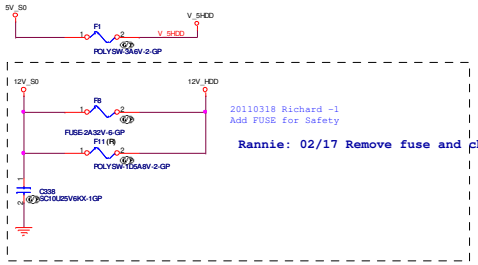
SB 120808 Richard
SWAP SATA PORT

1A 20110216 Richard
Remove SATA Driver IC



Layout: Please put them together

20101013 Richard



20110318 Richard -1
Add FUSE for Safety

Rannie: 02/17 Remove fuse and change to 0603 short pad

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BTN SATA

Size: Custom | Document Number: Tahoe | Rev: SA

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USB Power Enable

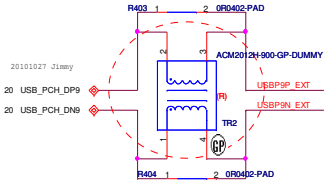
24,36,37,40,46 SLP_S4_N

USB signal

20 USB_PCH_DP11
20 USB_PCH_DN11

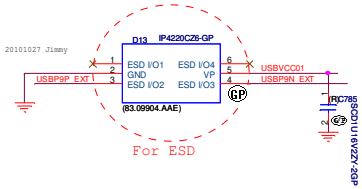
20 USB_PCH_DP9
20 USB_PCH_DN9

20 USB_OC_9_11_N

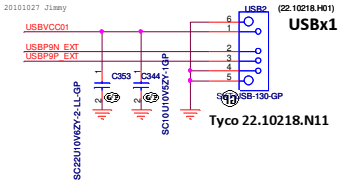


68.00201.141 Murata
69.10087.011 Chilisin

For EMI



For ESD



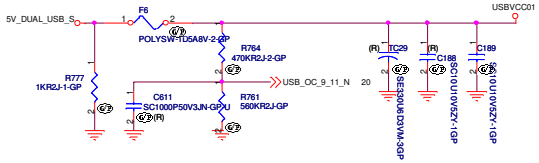
USBx1

Tyco 22.10218.N11

USB Power (S0,S3)

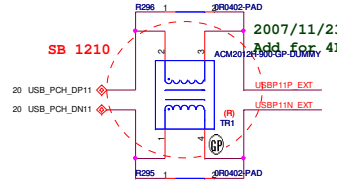
2010.0811 Richard

Use 69.50007.801 (Littelfuse)



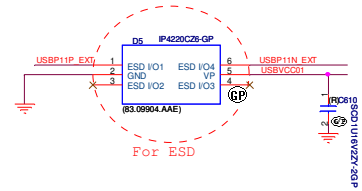
SB 1210

2007/11/23,
Add for 4L

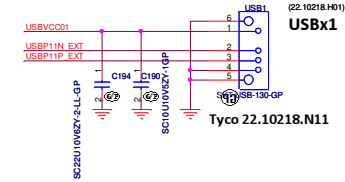


68.00201.141 Murata
69.10087.011 Chilisin

For EMI



For ESD



USBx1

Tyco 22.10218.N11

wistron

Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

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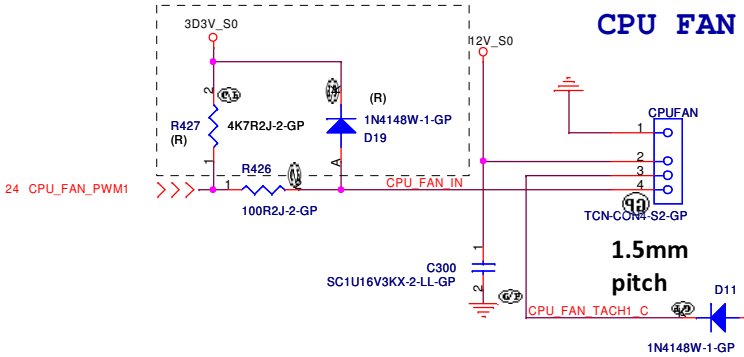
SIO FAN CONTROL

24 CPU_FAN_TACH1
24 CPU_FAN_PWM1

24 SYS_FAN_TACH1
24 SYS_FAN_PWM1

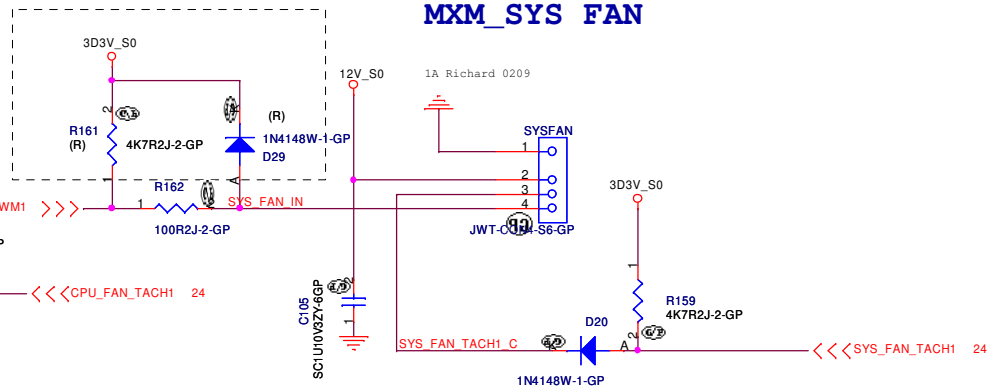
Rannie: 02/17 Lenovo ask to remove
pull high resistor and add ESD protector

CPU FAN



Rannie: 02/17 Lenovo ask to remove
pull high resistor and add ESD protector

MXM_SYS FAN



SB 20101207 Richard
Remove PSU FAN

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: FAN		
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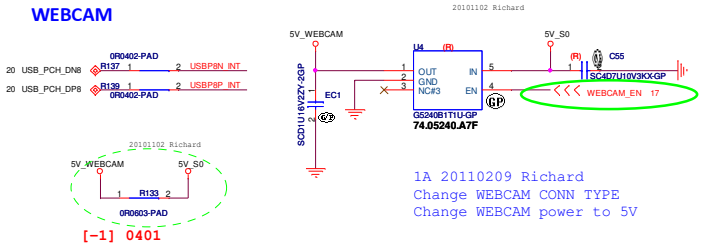
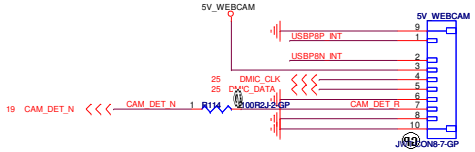
WEBCAM
20 USB_PCH_DN10
20 USB_PCH_DP10
17 WEBCAM_EN
Touch Panel
20 USB_PCH_DN10
20 USB_PCH_DP10
BlueTooth
20 USB_PCH_DN8
20 USB_PCH_DP8
LED
24,29 SIO_PWRLED_N
19 PCH_SATA_LED_N
NTD
19 CAM_DET_N
19 TP_DET_N
20 USB_PCH_DP0
20 USB_PCH_DN0

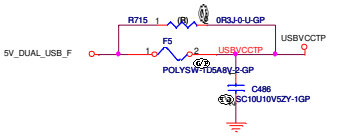
WEBCAM

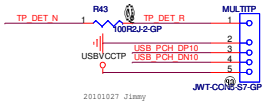


1A 20110209 Richard
Change WEBCAM CONN TYPE
Change WEBCAM power to 5V



Touch Panel



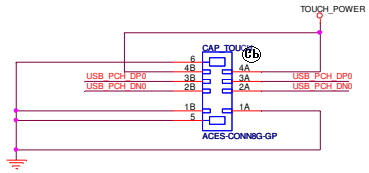


BTRF

RF->Wireless
KB/MS
REMOVE!!

SB 20101207 Richard
Remove bt

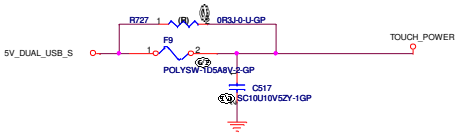
20110322 Richard -1
SWAP pin define



LED

20101007 Richard
DEL BT,WLAN,HDD LED

Blue Tooth Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CAMER BT TOUCH
Size: C
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Date: Wednesday, March 30, 2011
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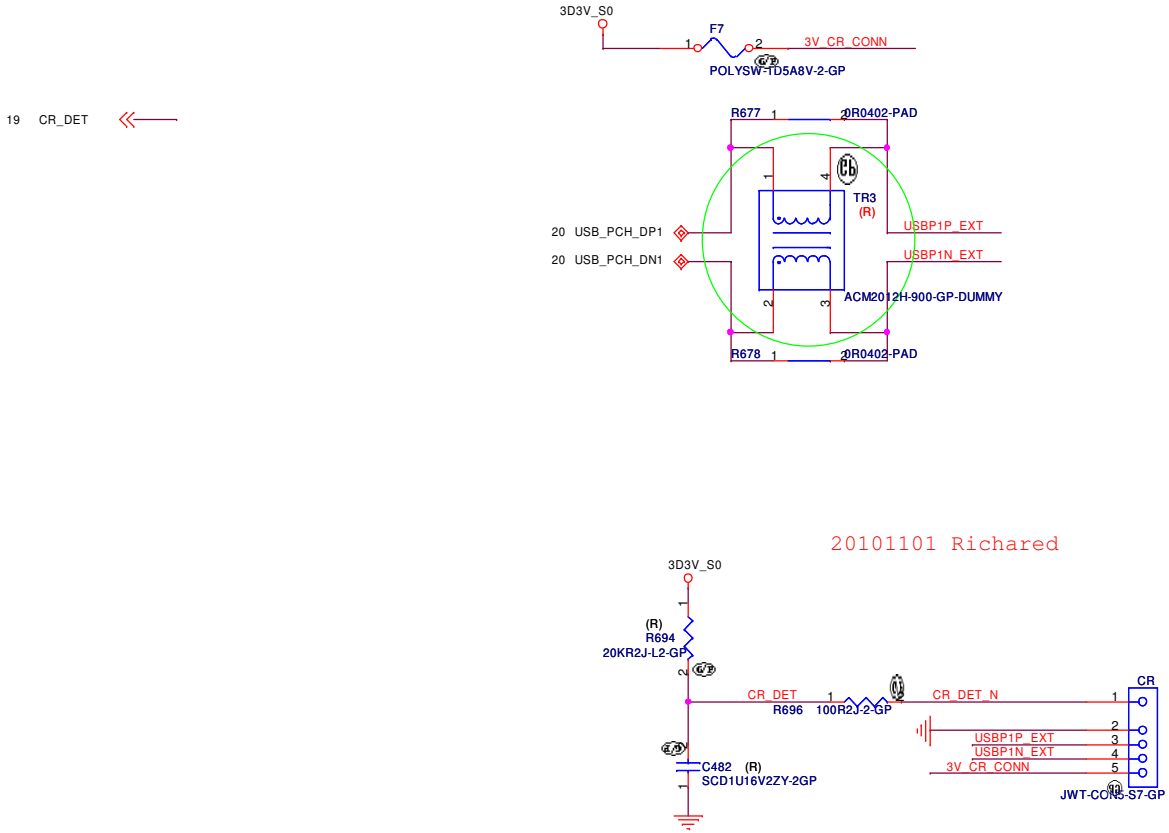

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CR		
Size: B	Document Number: Tahoe	Rev: SA
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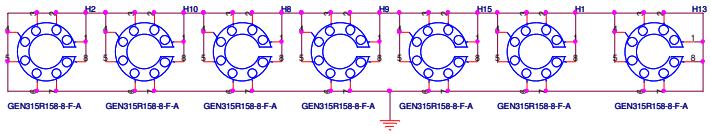
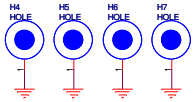
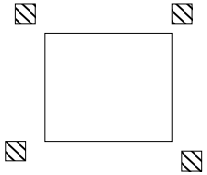
PCB MOUNTING HOLES-PTH

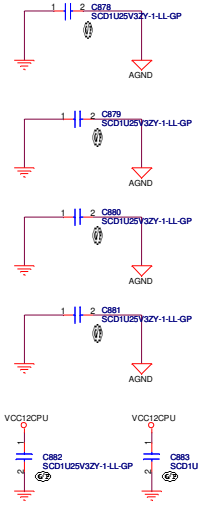


HOLE205R158

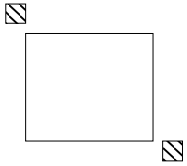


CPU MOUNTING HOLE-PTH

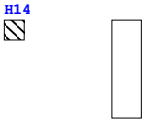




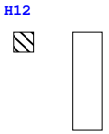
PCH MOUNTING HOLE-PTH



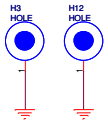
MINI PCIE 1 MOUNTING HOLE-PTH



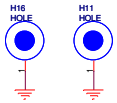
MINI PCIE 1 MOUNTING HOLE-PTH



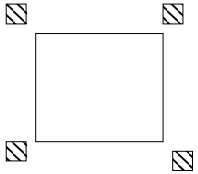
HOLE197R102



HOLE197R122



GPU MOUNTING HOLE-PTH



PCH MOUNTING HOLE-PTH

SYS FAN HOLE-PTH

<Variant Name>

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Title: SCALAR FW

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Display Port

61 DDSP_D_TX_DP_0
61 DDSP_D_TX_DN_0
61 DDSP_D_TX_DP_1
61 DDSP_D_TX_DN_1
61 DDSP_D_TX_DP_2
61 DDSP_D_TX_DN_2
61 DDSP_D_TX_DP_3
61 DDSP_D_TX_DN_3
61 DDPD_CTRL_CLK
61 DDPD_CTRL_DATA
61 DDSP_D_HPD

VGA Port

62 RED_IN_CONN
62 GREEN_IN_CONN
62 BLUE_IN_CONN
62 HSYNC_IN_CON
62 VSYNC_IN_CON
47,62 CRT_DDC_IN_CLK
47,62 CRT_DDC_IN_DATA

USB Port

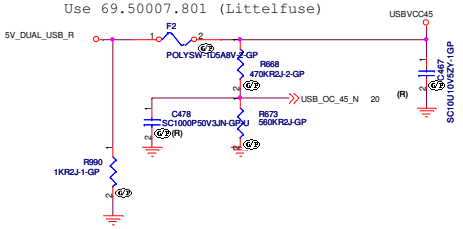
20 USB_PCH_DP2
20 USB_PCH_DN2
20 USB_PCH_DP3
20 USB_PCH_DN3
20 USB_PCH_DP4
20 USB_PCH_DN4
20 USB_PCH_DP5
20 USB_PCH_DN5

LAN Port

26 RJ45_LED0
26 RJ45_LED1
26 RJ45_LED2
26 LAN_MDI0_DN
26 LAN_MDI0_DP
26 LAN_MDI1_DN
26 LAN_MDI1_DP
26 LAN_MDI2_DN
26 LAN_MDI2_DP
26 LAN_MDI3_DN
26 LAN_MDI3_DP

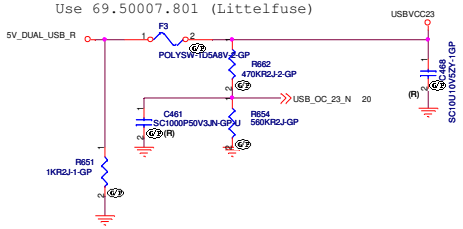
USB PORT4/5 Power

Use 69.50007.801 (Littelfuse)

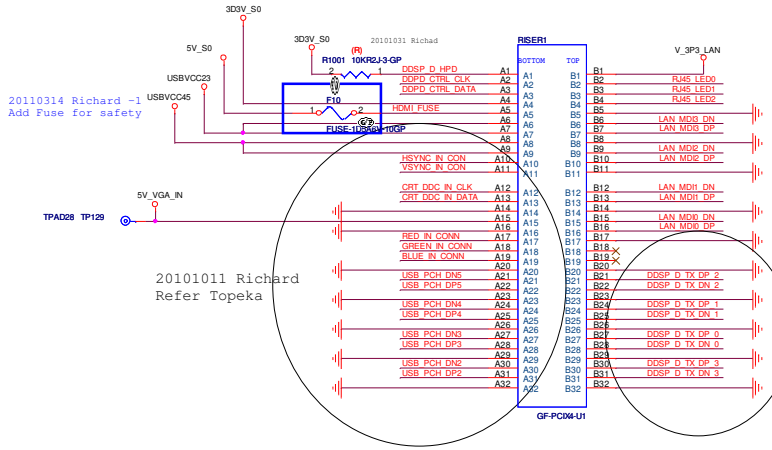


USB PORT2/3 Power

Use 69.50007.801 (Littelfuse)



20110314 Richard -1
Add Fuse for safety



20101011 Richard
Refer Topeka

20101011 Richard
Don't support Display port

20101027 Richard
Refer RISER

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Title		
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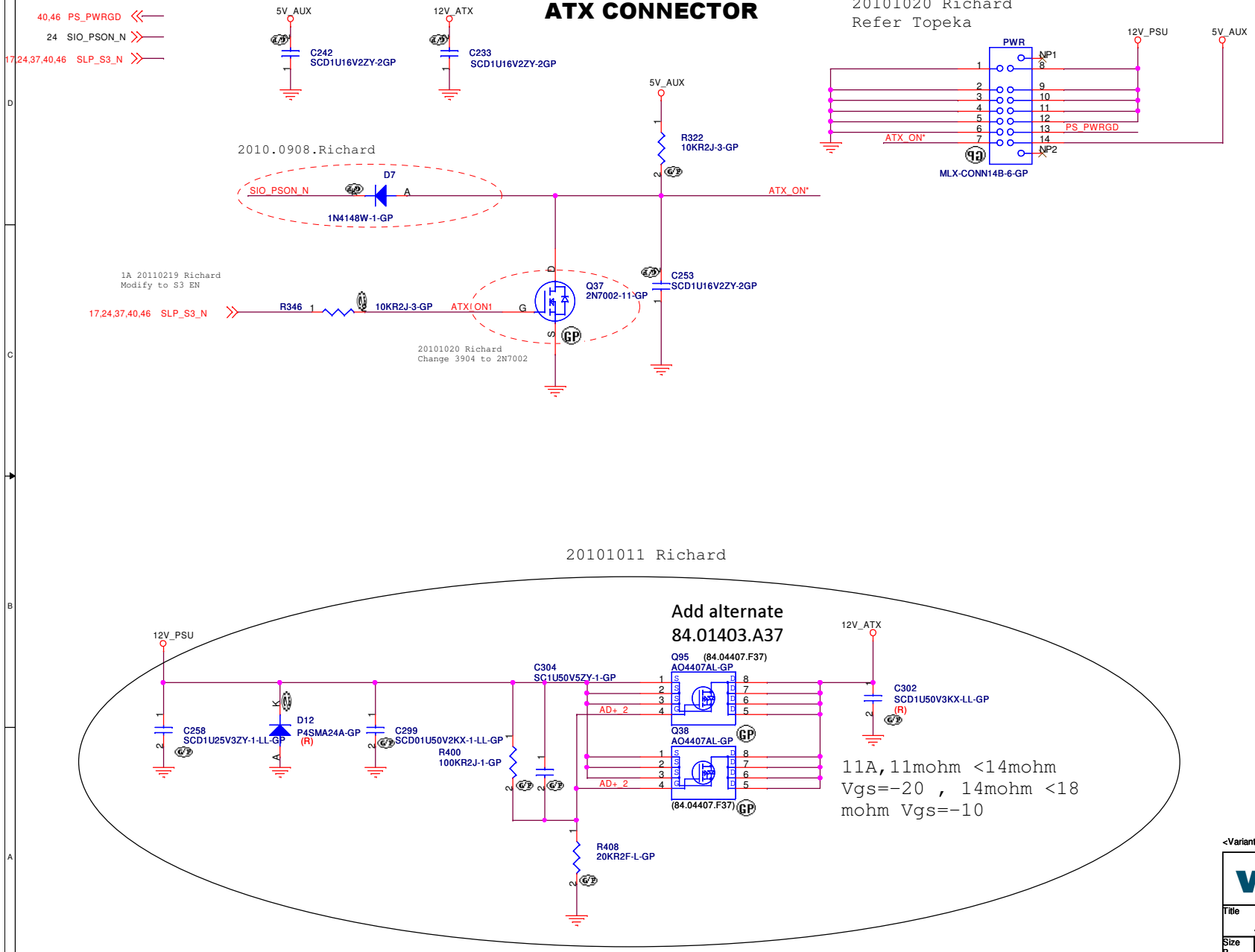
ATX CONNECTOR



<Variant Name>

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: ATX IN		
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SB 20101203 Richard

38,41,46,60 PC_PWRGD
46 LATCHED_BACKFEED_CUT
17 SLP_LAN_N
46 BACKFEED_CUT_N
24 DUAL_PWR_CTR
17,24,36,40,46 SLP_S4_N

+3.3VSB 0.96A

U31 SC10U10V5ZY-1-U-GP
APL1085UC-GP
ADJ VOUT VIN
VCC3_3SBREF

1.25/(R1/(R1+R2))=3.36V

S3/S4/S5 : Low Only . (Standby Power)
S0 : High_11.7V (Normal Power)

5V_AUX
C466
C463 SCD1U16V2ZY-2LLGP
3D3V_AUX
R649 124R2F-U-GP
R1
C455 SCAD71U10V5ZY-3GP
TC35 E220U10VM-4-GP
R646 210R2F-L-GP
R2

V_3P3_LAN/EPW DUAL

2010.0823.Richard

3D3V_S5 R288 0R5J-5-GP V_3P3_EPW

S0 S3 S5
L H H

BACKFEED_CUT_N R542 4K7R2J-2-GP LAN_S1 Q51 2N7002-11-GP
R549 4K7R2J-2-GP LAN_S4
5V_AUX R514 4K7R2J-2-GP LAN_S2
C368 SC1U6D3V2KX-GP
SLP_LAN_N R512 4K7R2J-2-GP LAN_S3 Q50 MMBT3904-3-GP
C367 SC1U6D3V2KX-GP
S0 S3 S5
H H

12V_ATX
R552 8K2R2J-3-GP
R545 0R2J-2-GP
Q58 2N7002-11-GP
VREG_LANP1 R536 0R2J-2-GP
C377 SC1U6D3V2KX-GP

N-MOS
P-MOS
U26 P5003QVG-GP
3D3V_S0
3D3V_AUX
VREG_LANDUAL_NCH
VREG_LANDUAL_PCH
V_3P3_LAN
R531 0R2J-2-GP
V_3P3_EPW
R518 0R5J-5-GP
C373 SCD1U16V2ZY-2GP
C376 SC2D2U10V3ZY-1GP
17 SLP_LAN_N

5V_AUX
R579 10KR2J-3-GP
SLP_LAN_C 20101031 Richad
1A 20110213 Richard
Change Q66 from NPN to PNP
Q66 PMBS3906-GP
R554 10KR2J-3-GP
SLP_PN1_M
R606 0R0402-PAD
SLP_PN1_M_G
R1020 10KR2J-3-GP
C417 SC1U16V3KX-2GP
3D3V_AUX
R572 (R) 0R3J-0-U-GP
Q76 (R) AO3413-GP
V_3P3_LAN

5V_DUAL USB CONTROL

20101028 Richard
Remove USB charger power

12V_ATX
D21 1N4148WS-7-F-GP
USB_PWR_GATE_12V
R778 2K2R2J-2-GP
5V_AUX
R784 20KR2J-L2-GP
USB_P_GATE
R783 0R0402-PAD
Q93 2N7002-11-GP
USB_PWR_SW
USB_PWR_SW_S
R791 0R0402-PAD

S0 S3 S5
L H L
2010.0830_Richard
LATCHED_BACKFEED_CUT R793 0R2J-2-GP
DUAL_PWR_CTR R794 0R0402-PAD
1A 20110211_richard
Change R794 to short-pad

SIDE USB PWR

U17 P5003QVG-GP
USB_PWR_GATE1
5V_AUX
5V_S0
5V_DUAL_USB_S
C225 SCD1U16V2ZY-2GP
Place neasr Connecter

U33 P5003QVG-GP
USB_PWR_GATE1
5V_AUX
5V_S0
5V_DUAL_USB_F
C488 SCD1U16V2ZY-2GP
0714

FRONT USB PWR

U44 P5003QVG-GP
USB_PWR_GATE1
5V_AUX
5V_S0
5V_DUAL_USB_R
C852 SCD1U16V2ZY-2GP
0714

REAR USB PWR

5V_AUX
R473 8K2R2J-3-GP
+5V_DUAL_USB_S_R
C360 SCD1U16V2ZY-2GP (R)
Q113 2N7002-11-GP
R493 8K2R2J-3-GP
SLP_S4_N
SLP_S4_N_R1
C541 SCD1U16V2ZY-2GP (R)
Q118 2N7002-11-GP
DIS_5V_DUAL_USB_S
R1217 470R3J-2-GP
R1218 470R3J-2-GP
5V_DUAL_USB_S

DIS_5V_DUAL_USB_R
R1220 470R3J-2-GP
R1219 470R3J-2-GP
Q114 2N7002-11-GP
+5V_DUAL_USB_S_R
5V_DUAL_USB_R

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Hsichih, Taipei

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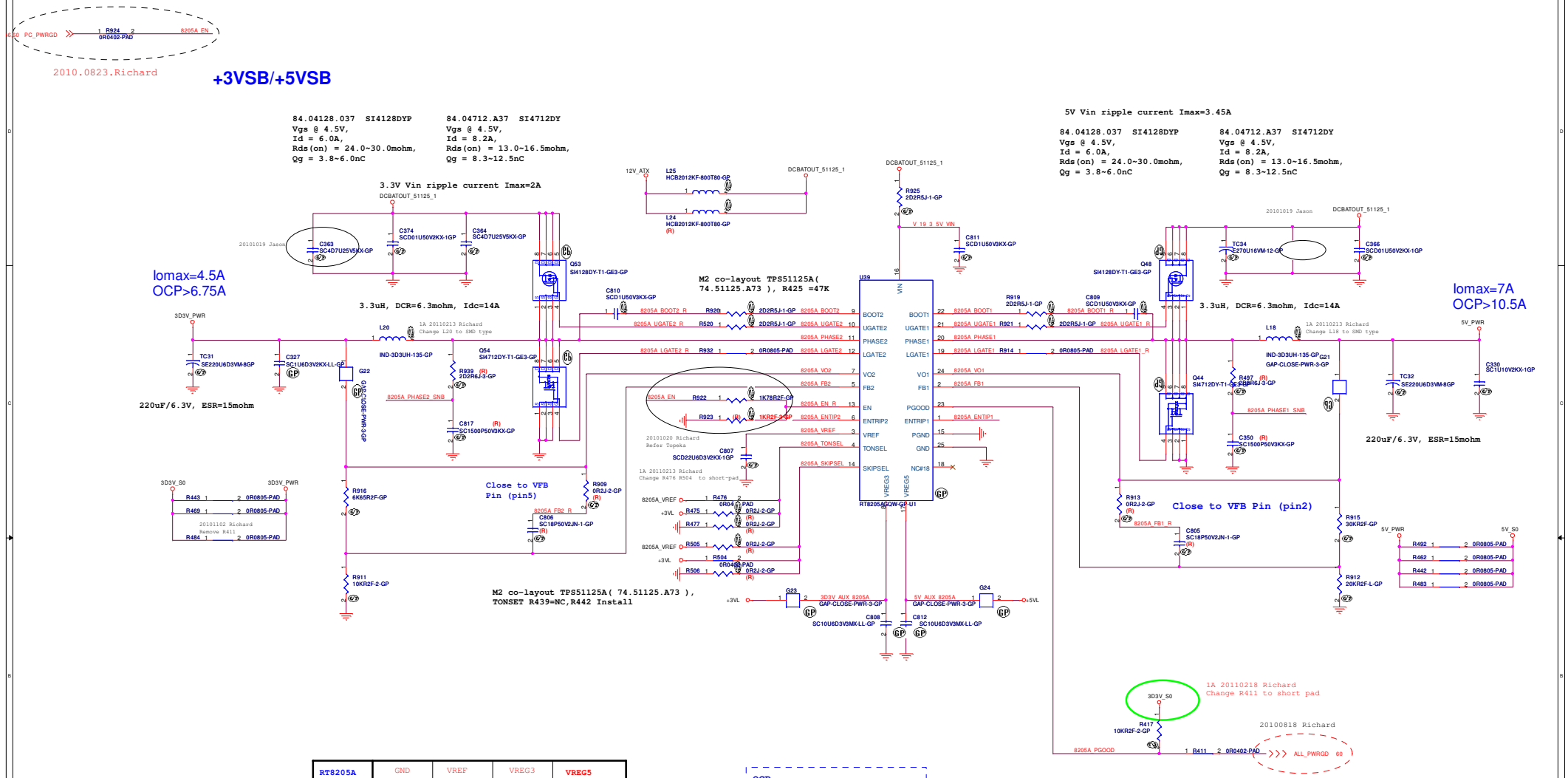
PC_PWRGD
R924 0R0402-PAD
8205A EN
2010.0823.Richard
+3VSB/+5VSB
84.04128.037 SI4128DYP
Vgs @ 4.5V,
Id = 6.0A,
Rds(on) = 24.0~30.0mohm,
Qg = 3.8~6.0nC
84.04712.A37 SI4712DY
Vgs @ 4.5V,
Id = 8.2A,
Rds(on) = 13.0~16.5mohm,
Qg = 8.3~12.5nC
3.3V Vin ripple current Imax=2A
5V Vin ripple current Imax=3.45A
Iomax=4.5A
OCP>6.75A
Iomax=7A
OCP>10.5A
3.3uH, DCR=6.3mohm, Idc=14A
220uF/6.3V, ESR=15mohm
M2 co-layout TPS51125A(74.51125.A73), R425 =47K
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
M2 co-layout TPS51125A(74.51125.A73), TONSET R439=NC,R442 Install
RT8205A
1A 20110218 Richard
Change R411 to short pad
20100818 Richard
OCP
RT8205A GND VREF VREG3 VREG5
SKIPSEL PWM SKIP 00A AUTOSKIP 00A AUTOSKIP
TONSEL 200k/CH1 250k/CH2 330k/CH1 375k/CH2 400k/CH1 500k/CH2 400k/CH1 500k/CH2
TPS51125A GND VREF VREG3 VREG5
SKIPSEL PWM SKIP 00A AUTOSKIP 00A AUTOSKIP
TONSEL 200k/CH1 250k/CH2 245k/CH1 305k/CH2 300k/CH1 375k/CH2 365k/CH1 460k/CH2
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
Size A2
Document Number Tahoe
Rev SA
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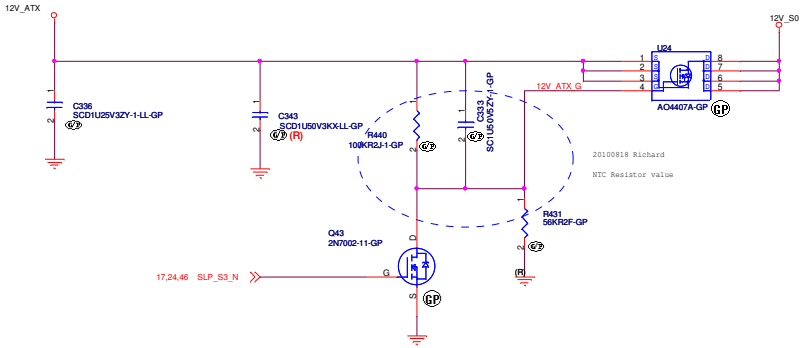

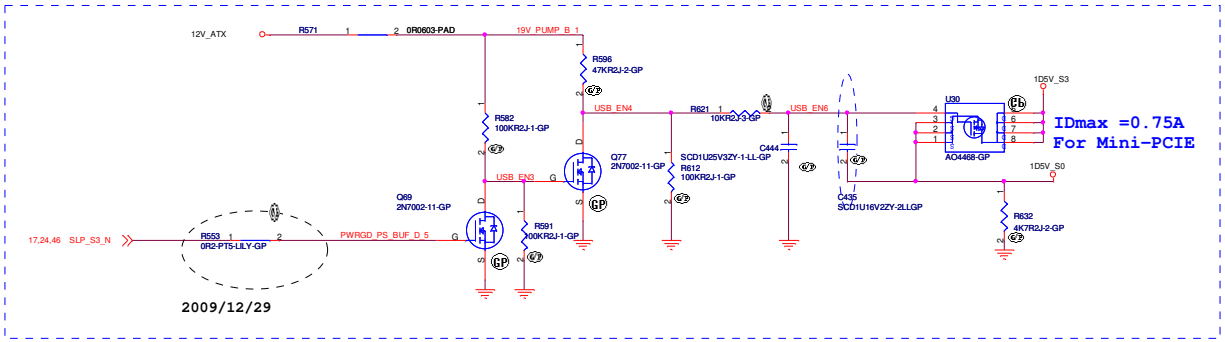

<Variant Name>

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Hsichih, Taipei

Title: RUN POWER

Size: C | Document Number: Tahoe | Rev: SA

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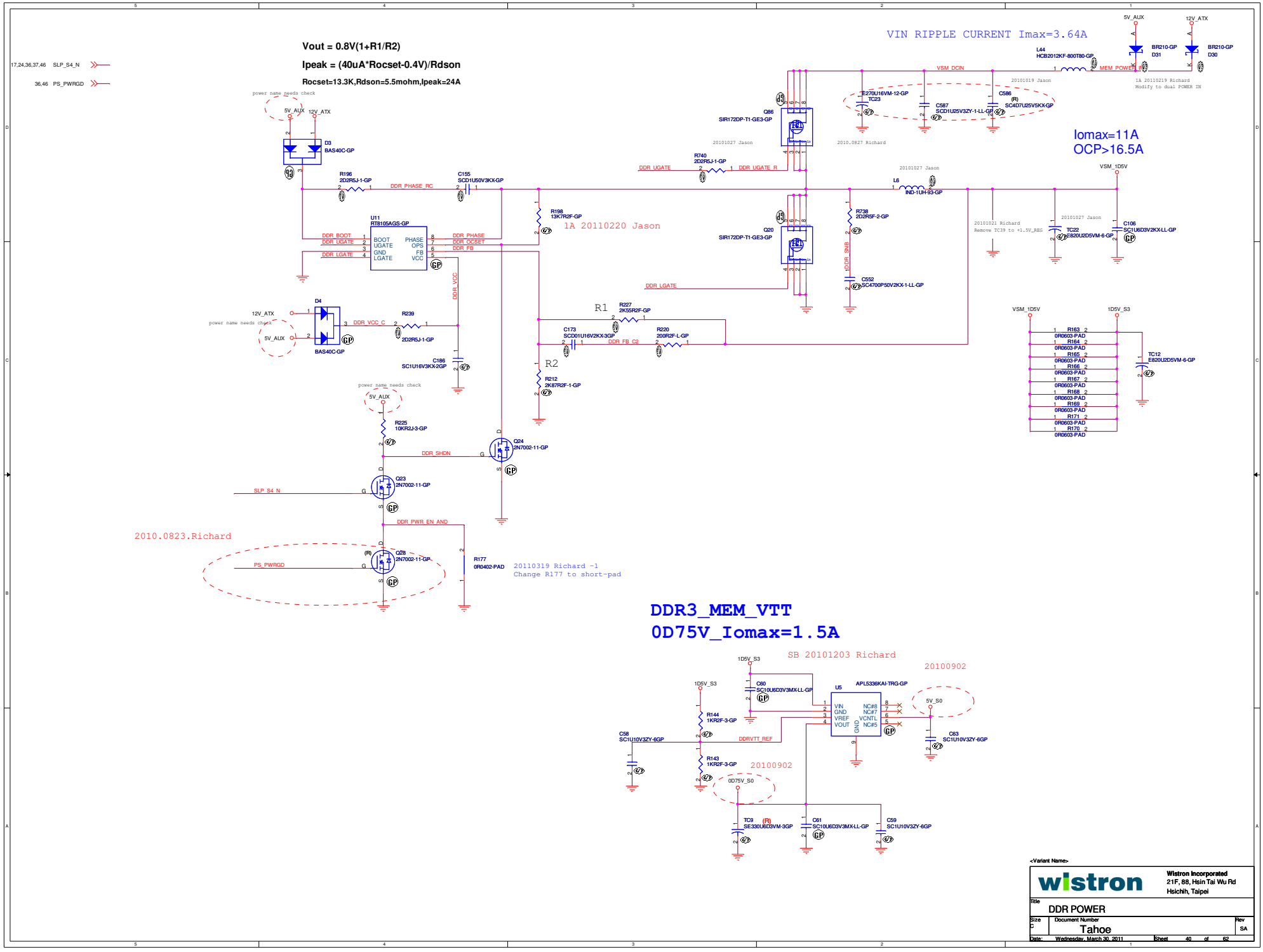
Vout = 0.8V(1+R1/R2)
Ipeak = (40uA*Rocset-0.4V)/Rdson
Rocset=13.3K,Rdson=5.5mohm,Ipeak=24A
17,24,36,37,46 SLP_S4_N
36,46 PS_PWRGD
VIN RIPPLE CURRENT Imax=3.64A
Iomax=11A
OCP>16.5A
1A 20110220 Jason
2010.0823.Richard
20110319 Richard -1
Change R177 to short-pad
DDR3_MEM_VTT
0D75V_Iomax=1.5A
SB 20101203 Richard
20100902
1A 20110219 Richard
Modify to dual POWER IN
20101021 Richard
Remove TC39 to +1.5V_REG
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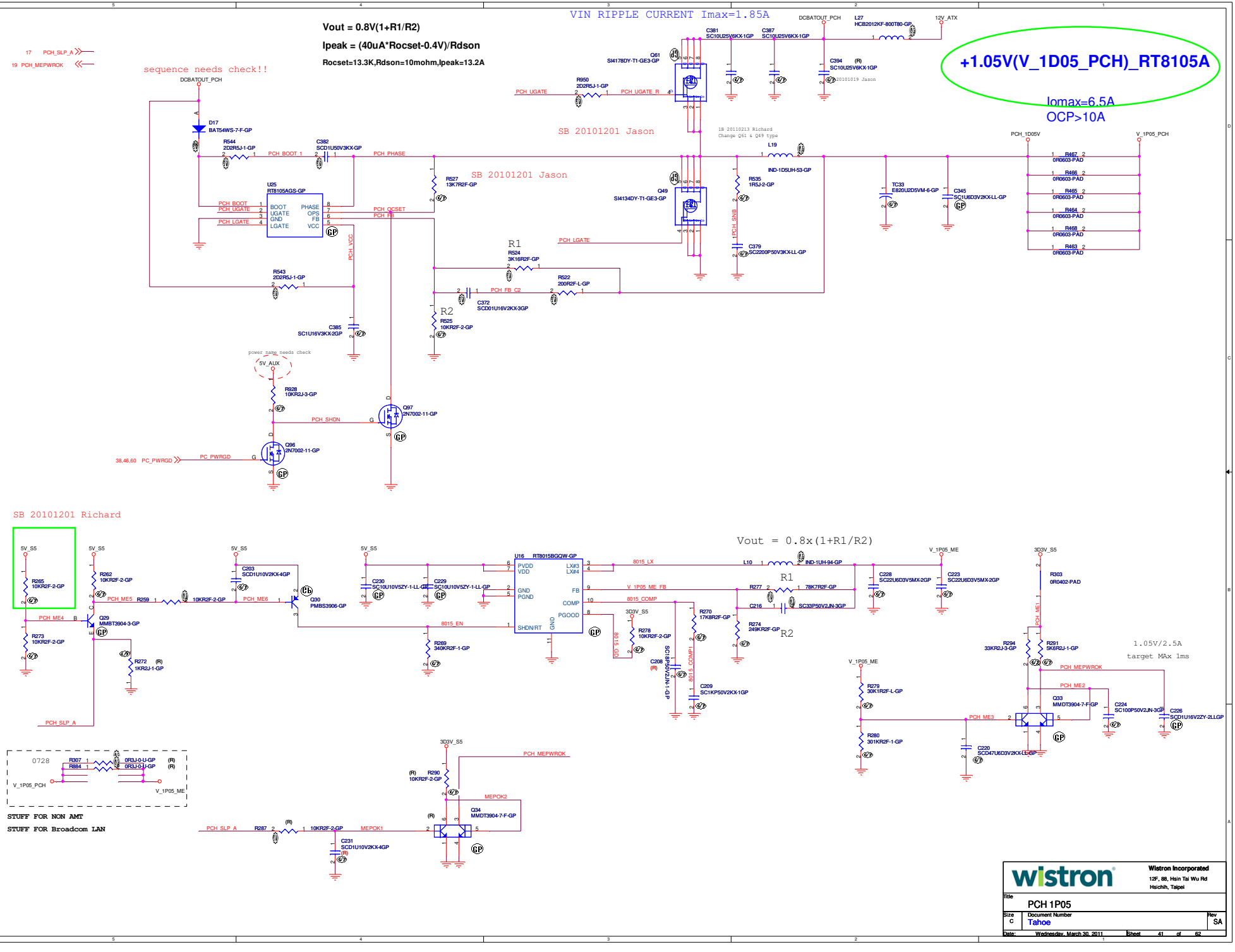
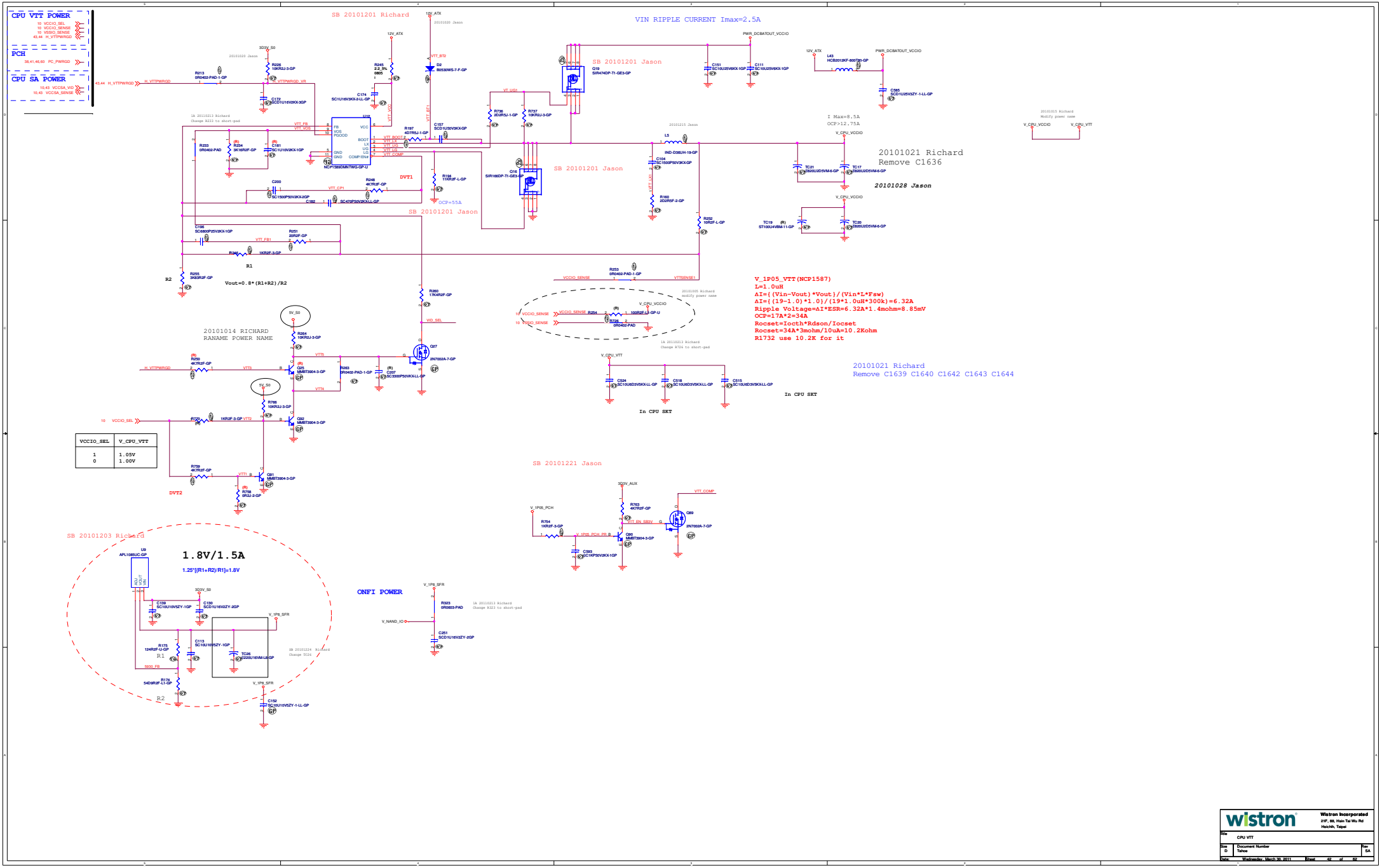
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
DDR POWER
Tahoe
Wednesday, March 30, 2011


VIN RIPPLE CURRENT Imax=1.85A
Vout = 0.8V(1+R1/R2)
Ipeak = (40uA*Rocset-0.4V)/Rdson
Rocset=13.3K,Rdson=10mohm,Ipeak=13.2A
+1.05V(V_1D05_PCH)_RT8105A
Iomax=6.5A
OCP>10A
sequence needs check!!
SB 20101201 Jason
SB 20101201 Richard
power name needs check
Vout = 0.8x(1+R1/R2)
1.05V/2.5A
target MAx 1ms
STUFF FOR NON AMT
STUFF FOR Broadcom LAN
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
PCH 1P05
Tahoe
Wednesday, March 30, 2011


CPU VTT POWER
10 VCCIO_SEL
10 VCCIO_SENSE
10 VSSIO_SENSE
43,44 H_VTTPWRGD
PCH
38,41,46,60 PC_PWRGD
CPU SA POWER
10,43 VCCSA_VID
10,43 VCCSA_SENSE
SB 20101201 Richard
VIN RIPPLE CURRENT Imax=2.5A
SB 20101201 Jason
20101021 Richard
Remove C1636
20101028 Jason
20101014 RICHARD
RANAME POWER NAME
Vout=0.8*(R1+R2)/R2
R1
R2
V_1P05_VTT(NCP1587)
L=1.0uH
ΔI={(Vin-Vout)*Vout}/(Vin*L*Fsw)
ΔI={(19-1.0)*1.0}/(19*1.0uH*300k)=6.32A
Ripple Voltage=ΔI*ESR=6.32A*1.4mohm=8.85mV
OCP=17A*2=34A
Rocset=Iocth*Rdson/Iocset
Rocset=34A*3mohm/10uA=10.2Kohm
R1732 use 10.2K for it
20101021 Richard
Remove C1639 C1640 C1642 C1643 C1644
In CPU SKT
In CPU SKT
SB 20101221 Jason
SB 20101203 Richard
1.8V/1.5A
1.25*[(R1+R2)/R1]=1.8V
ONFI POWER
VCCIO_SEL
V_CPU_VTT
1
1.05V
0
1.00V
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Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
CPU VTT
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PWR Manager

24,44 VSA_PWRGD
38,60 ALL_PWRGD
42,44 H_VTTPWRGD

+0.85V(0D85V_S0)_APL5611 for VCCSA

SB 20101208
Change Power Solution

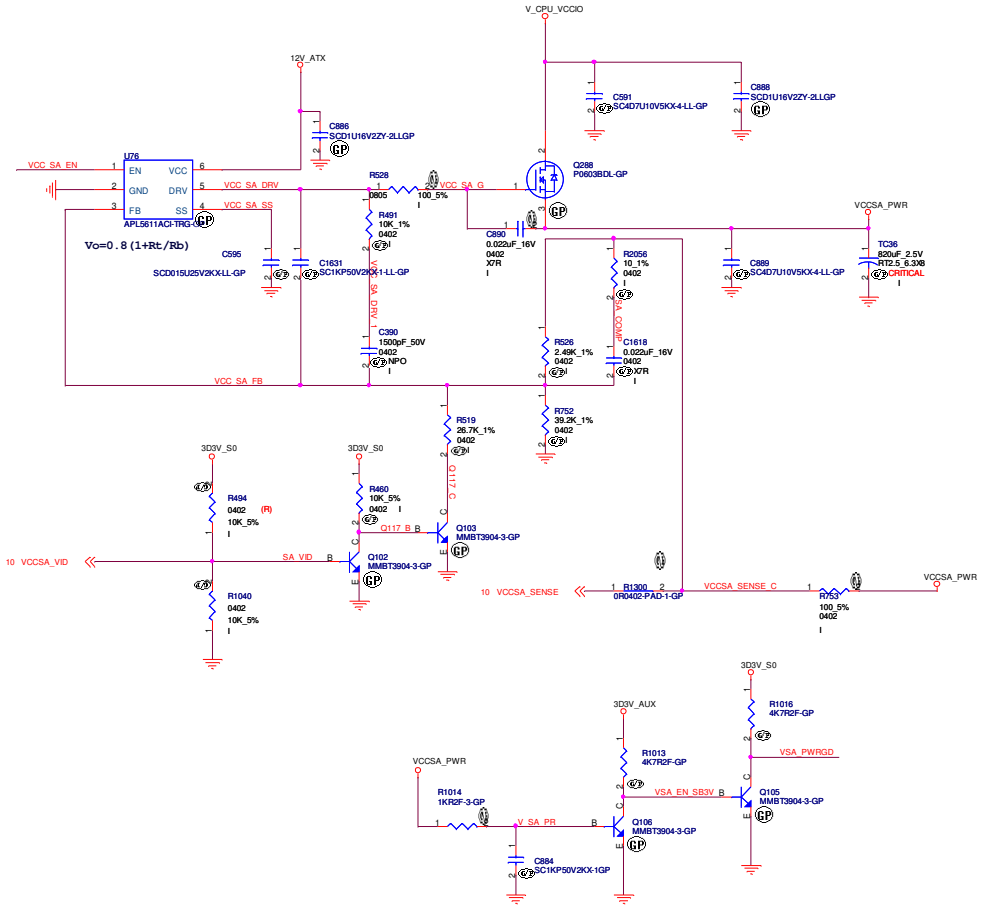
VCCSA_SENSE

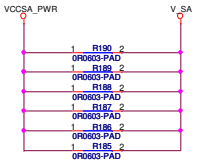
10 VCCSA_SENSE

VCCSA_LEVEL_VID

10 VCCSA_VID

VID	V_SA
0	0.925V(Default)
1	0.85V





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12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU VSA

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CPU VCORE POWER

42,43 H_VTTPWRGD
24,43 VSA_PWRGD
10 VCC_SENSE
10 VSS_SENSE
10 H_VIDSOUT_VR
10 H_VIDSCK_VR
10 H_VIDALERT_VR
45 PWM1
45 CSN1
45 CSP1
45 PWM2
45 CSN2
45 CSP2
45 PWM3
45 CSN3
45 CSP3
14,17,59,60 CPU_CORE_PWRGD

CPU AXG POWER

10 VCCAXG_SENSE
10 VSSAXG_SENSE

HOT

10,24 H_PROCHOT_N

20101011 Richard

2010.0823.Richard

VCC_CORE

VCORE PORTION

V_GT PORTION

UMA MXM SKU option

SB 20101201 Jason

add phase 4 application

EVT2

2010427:Add Res to GND, but need confirm its value

VCC_AXG

Option: Disalbe VCC_AXG

Put colse to VCC_AXG hot spot

Work F=270Khz

Bottom PAD connect to GND Through 4 Vias

Put colse to VCORE hot spot

PWM ADDRESS		
Resistor Value	SVID address for Vcore rail	SVID address for VCC_AXG rail
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
124K	1010	1011
165K	1100	1101

BOOT VOLTAGE	
Resistor value	Boot Voltage
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
124K	1.1V
165K	1.5V

VBOOT
VCORE VBOOT SET AT 1.1V

IMAX
VCORE IMAX SET AT 112A

ADDR
PWM ADDRESS

PWM_IMAX
VCC_AXG IMAX SET AT 35A

3 Phase option

VCC_AXG

VCCP Vin ripple current Imax=7.7A

84.04809.036 NTD4809
Vgs @ 4.5V,
Id = 45A,
Rds(on) = 12~14mohm,
Qg = 11~13nC

84.04806.036 NTD4806
Vgs @ 4.5V,
Id = 59A,
Rds(on) = 7.9~9.4mohm,
Qg = 15~23nC

1.0uH, DCR=2.2mohm, Idc=29A

820uF/2.5V, ESR=7.0mohm

0.65V~1.3V, TDC=25A

Bottom PAD connect to GND through 4 Vias

Wistron Incorporated
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Hsichih, Taipei

Title: VRM 1
Size: D
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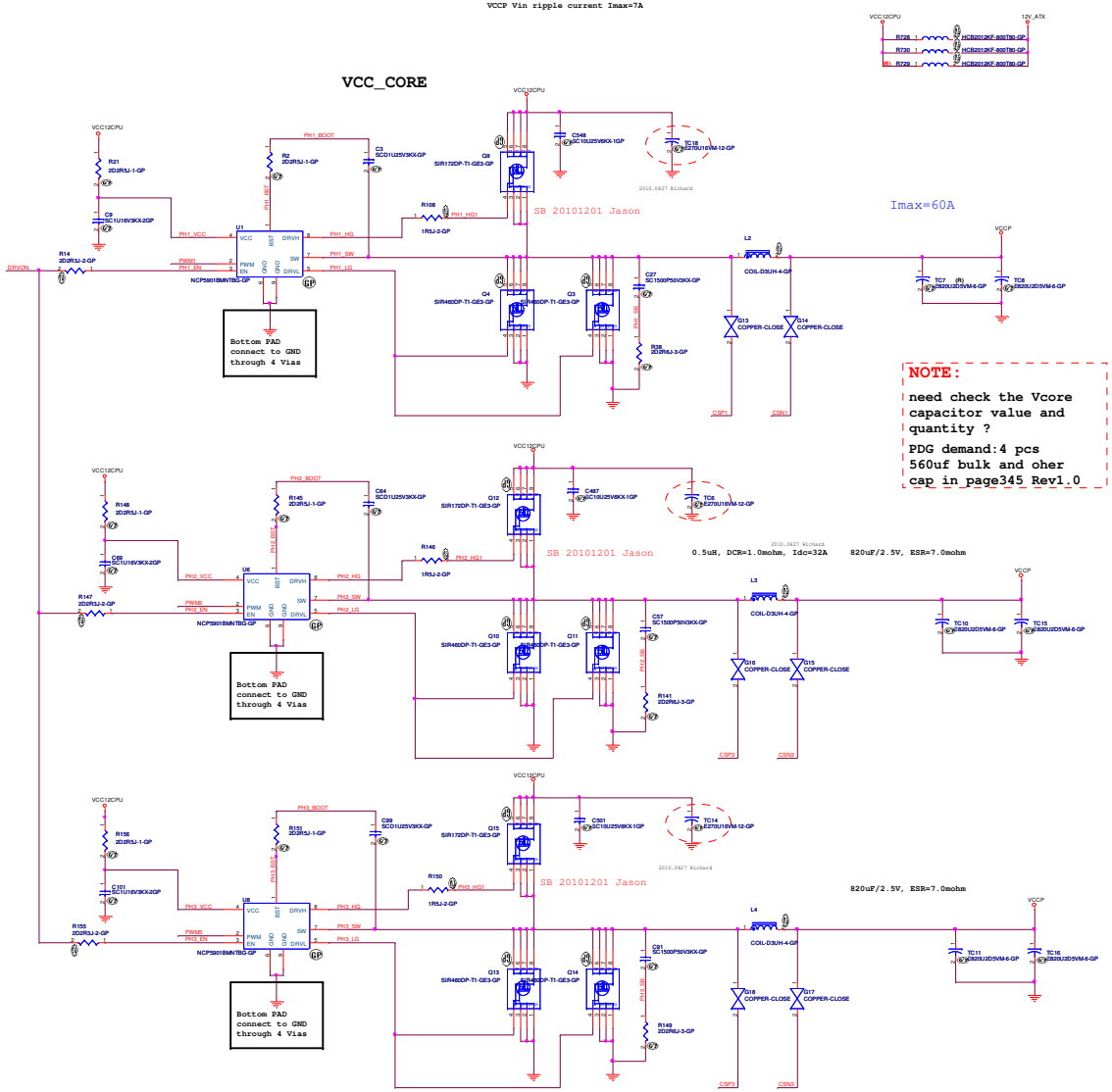
CPU VCORE POWER

44 DRVON
44 PWM1
44 CSP1
44 CSN1
44 PWM2
44 CSP2
44 CSN2
44 PWM3
44 CSP3
44 CSN3

VCCP Vin ripple current Imax=7A

VCC_CORE



wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: VRM 2
Size: Custom/Yellow
Document Number
Rev: SA
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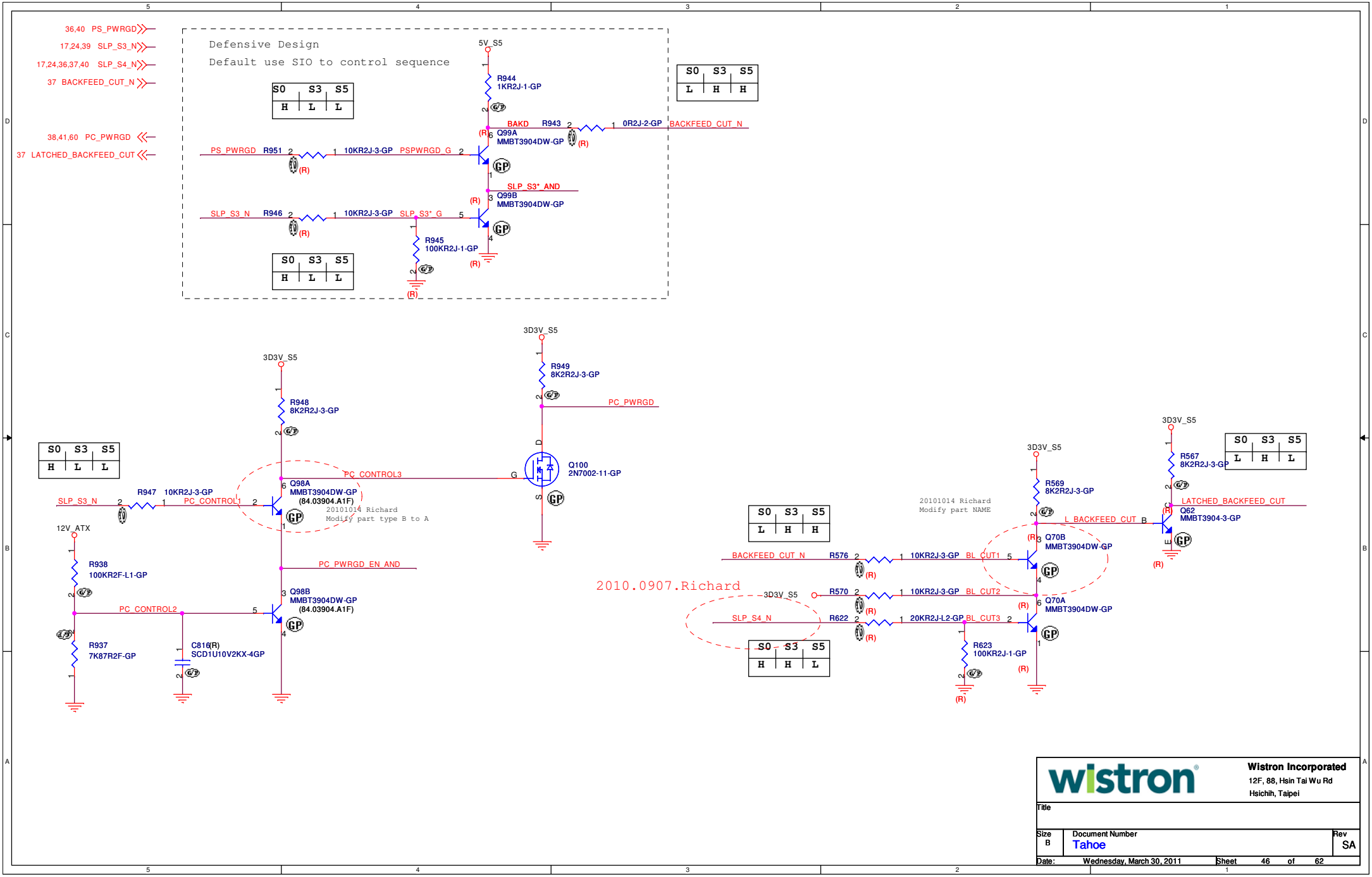
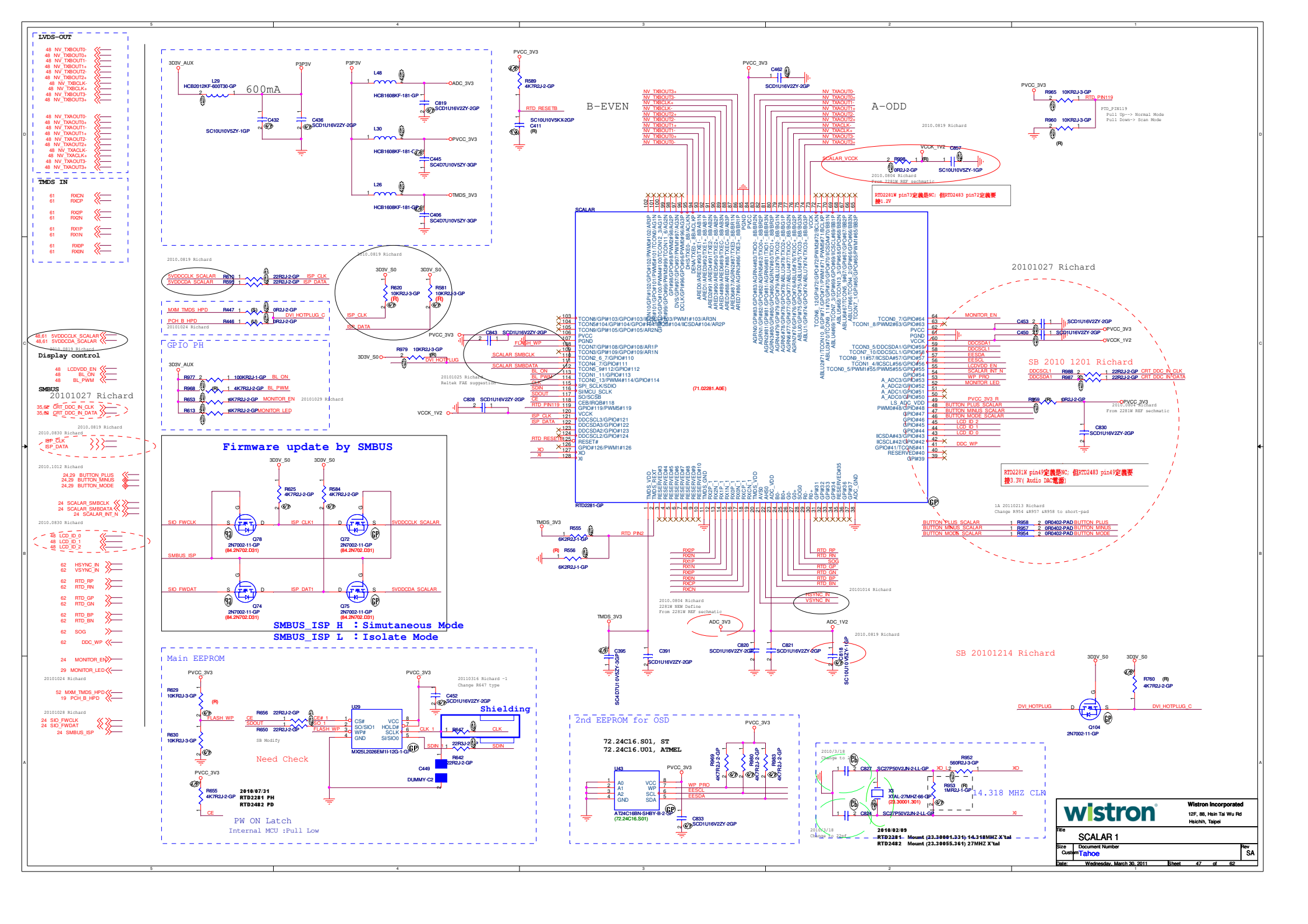
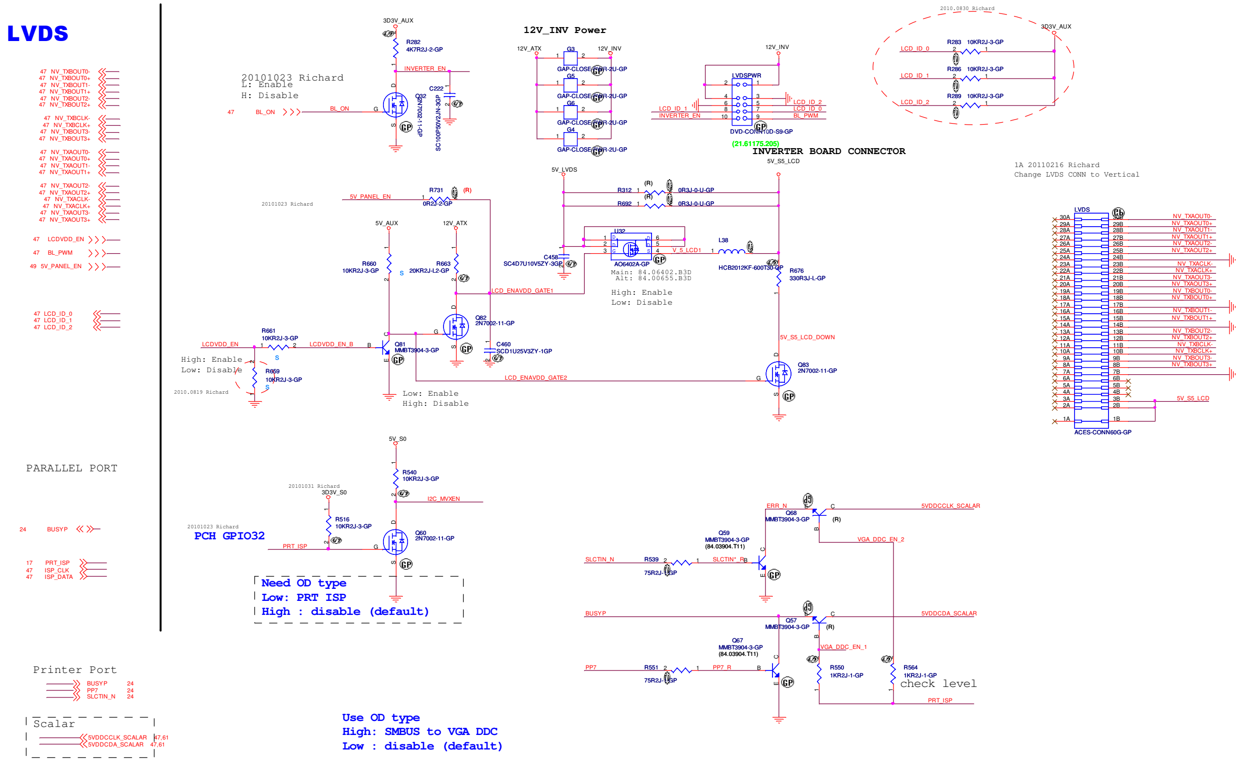

36,40 PS_PWRGD
17,24,39 SLP_S3_N
17,24,36,37,40 SLP_S4_N
37 BACKFEED_CUT_N
38,41,60 PC_PWRGD
37 LATCHED_BACKFEED_CUT
Defensive Design
Default use SIO to control sequence
5V_S5
R944 1KR2J-1-GP
BAKD
R943 0R2J-2-GP
BACKFEED_CUT_N
Q99A MMBT3904DW-GP
PS_PWRGD
R951 10KR2J-3-GP
PSPWRGD_G
SLP_S3* AND
Q99B MMBT3904DW-GP
SLP_S3_N
R946 10KR2J-3-GP
SLP_S3*_G
R945 100KR2J-1-GP
S0 S3 S5
H L L
L H H
3D3V_S5
R948 8K2R2J-3-GP
R949 8K2R2J-3-GP
PC_PWRGD
Q100 2N7002-11-GP
PC_CONTROL3
Q98A MMBT3904DW-GP (84.03904.A1F)
SLP_S3_N
R947 10KR2J-3-GP
PC_CONTROL1
20101014 Richard
Modify part type B to A
12V_ATX
R938 100KR2F-L1-GP
PC_CONTROL2
PC_PWRGD_EN_AND
Q98B MMBT3904DW-GP (84.03904.A1F)
R937 7K87R2F-GP
C816(R) SCD1U10V2KX-4GP
2010.0907.Richard
20101014 Richard
Modify part NAME
R569 8K2R2J-3-GP
L_BACKFEED_CUT_B
Q70B MMBT3904DW-GP
Q70A MMBT3904DW-GP
BACKFEED_CUT_N
R576 10KR2J-3-GP
BL_CUT1
R570 10KR2J-3-GP
BL_CUT2
SLP_S4_N
R622 20KR2J-L2-GP
BL_CUT3
R623 100KR2J-1-GP
R567 8K2R2J-3-GP
LATCHED_BACKFEED_CUT
Q62 MMBT3904-3-GP
wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
Size B
Document Number
Tahoe
Rev SA
Date: Wednesday, March 30, 2011
Sheet 46 of 62


LVDS-OUT
TMDS IN
Display control
SMBUS
20101027 Richard
Firmware update by SMBUS
SMBUS_ISP H : Simutaneous Mode
SMBUS_ISP L : Isolate Mode
Main EEPROM
Need Check
PW ON Latch
Internal MCU :Pull Low
2nd EEPROM for OSD
72.24C16.S01, ST
72.24C16.U01, ATMEL
Shielding
B-EVEN
A-ODD
SCALAR
RTD2281-GP
SB 2010 1201 Richard
SB 20101214 Richard
14.318 MHZ CLK
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
SCALAR 1
Tahoe
Wednesday, March 30, 2011



wistron

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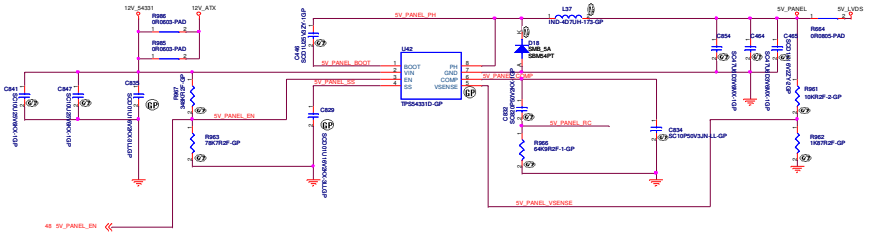
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: SCALAR 2

Size: D | Document Number: Tahoe | Rev: SA

Date: Wednesday, March 30, 2011 | Sheet 48 of 62



wistron

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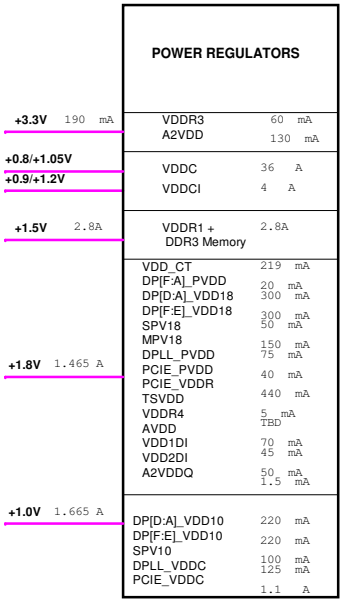
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

Size	Document Number	Rev
D	Tahoe	SA

Date: Wednesday, March 30, 2011 Sheet 49 of 62



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_Power rail

Size	Document Number	Rev
C	Tahoe	SA

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PCI_E x16

11 PEG_TXP[15..0]

PEG_TXP0
PEG_TXP1
PEG_TXP2
PEG_TXP3
PEG_TXP4
PEG_TXP5
PEG_TXP6
PEG_TXP7
PEG_TXP8
PEG_TXP9
PEG_TXP10
PEG_TXP11
PEG_TXP12
PEG_TXP13
PEG_TXP14
PEG_TXP15

11 PEG_TXN[15..0]

PEG_TXN0
PEG_TXN1
PEG_TXN2
PEG_TXN3
PEG_TXN4
PEG_TXN5
PEG_TXN6
PEG_TXN7
PEG_TXN8
PEG_TXN9
PEG_TXN10
PEG_TXN11
PEG_TXN12
PEG_TXN13
PEG_TXN14
PEG_TXN15

11 PEG_RXP[15..0]

PEG_RXP0
PEG_RXP1
PEG_RXP2
PEG_RXP3
PEG_RXP4
PEG_RXP5
PEG_RXP6
PEG_RXP7
PEG_RXP8
PEG_RXP9
PEG_RXP10
PEG_RXP11
PEG_RXP12
PEG_RXP13
PEG_RXP14
PEG_RXP15

11 PEG_RXN[15..0]

PEG_RXN0
PEG_RXN1
PEG_RXN2
PEG_RXN3
PEG_RXN4
PEG_RXN5
PEG_RXN6
PEG_RXN7
PEG_RXN8
PEG_RXN9
PEG_RXN10
PEG_RXN11
PEG_RXN12
PEG_RXN13
PEG_RXN14
PEG_RXN15

18 CLK_PCIE_PEG_N
18 CLK_PCIE_PEG_P

10,14,17,24 PLT_RST_N — R209 1 2 0R0402-PAD — ATI_RST#

A710-SA_0627_CWH

SB 1202

U18A — 1 OF 8

PCI EXPRESS INTERFACE

PEG_TXP0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_T_TXP0	DIS	C580	SCD1U10V2KX-4GP	PEG_RXP0
PEG_TXN0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_T_TXN0	DIS	C579	SCD1U10V2KX-4GP	PEG_RXN0
PEG_TXP1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_T_TXP1	DIS	C557	SCD1U10V2KX-4GP	PEG_RXP1
PEG_TXN1	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_T_TXN1	DIS	C558	SCD1U10V2KX-4GP	PEG_RXN1
PEG_TXP2	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_T_TXP2	DIS	C581	SCD1U10V2KX-4GP	PEG_RXP2
PEG_TXN2	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_T_TXN2	DIS	C582	SCD1U10V2KX-4GP	PEG_RXN2
PEG_TXP3	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_T_TXP3	DIS	C559	SCD1U10V2KX-4GP	PEG_RXP3
PEG_TXN3	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_T_TXN3	DIS	C560	SCD1U10V2KX-4GP	PEG_RXN3
PEG_TXP4	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_T_TXP4	DIS	C583	SCD1U10V2KX-4GP	PEG_RXP4
PEG_TXN4	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_T_TXN4	DIS	C584	SCD1U10V2KX-4GP	PEG_RXN4
PEG_TXP5	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_T_TXP5	DIS	C567	SCD1U10V2KX-4GP	PEG_RXP5
PEG_TXN5	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_T_TXN5	DIS	C568	SCD1U10V2KX-4GP	PEG_RXN5
PEG_TXP6	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_T_TXP6	DIS	C571	SCD1U10V2KX-4GP	PEG_RXP6
PEG_TXN6	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_T_TXN6	DIS	C572	SCD1U10V2KX-4GP	PEG_RXN6
PEG_TXP7	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_T_TXP7	DIS	C554	SCD1U10V2KX-4GP	PEG_RXP7
PEG_TXN7	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_T_TXN7	DIS	C553	SCD1U10V2KX-4GP	PEG_RXN7
PEG_TXP8	N38	PCIE_RX8P	PCIE_TX8P	N33	PEG_T_TXP8	DIS	C569	SCD1U10V2KX-4GP	PEG_RXP8
PEG_TXN8	M37	PCIE_RX8N	PCIE_TX8N	N32	PEG_T_TXN8	DIS	C570	SCD1U10V2KX-4GP	PEG_RXN8
PEG_TXP9	M35	PCIE_RX9P	PCIE_TX9P	N30	PEG_T_TXP9	DIS	C555	SCD1U10V2KX-4GP	PEG_RXP9
PEG_TXN9	L36	PCIE_RX9N	PCIE_TX9N	N29	PEG_T_TXN9	DIS	C556	SCD1U10V2KX-4GP	PEG_RXN9
PEG_TXP10	L38	PCIE_RX10P	PCIE_TX10P	L33	PEG_T_TXP10	DIS	C573	SCD1U10V2KX-4GP	PEG_RXP10
PEG_TXN10	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_T_TXN10	DIS	C574	SCD1U10V2KX-4GP	PEG_RXN10
PEG_TXP11	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_T_TXP11	DIS	C563	SCD1U10V2KX-4GP	PEG_RXP11
PEG_TXN11	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_T_TXN11	DIS	C561	SCD1U10V2KX-4GP	PEG_RXN11
PEG_TXP12	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_T_TXP12	DIS	C575	SCD1U10V2KX-4GP	PEG_RXP12
PEG_TXN12	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_T_TXN12	DIS	C578	SCD1U10V2KX-4GP	PEG_RXN12
PEG_TXP13	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_T_TXP13	DIS	C565	SCD1U10V2KX-4GP	PEG_RXP13
PEG_TXN13	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_T_TXN13	DIS	C566	SCD1U10V2KX-4GP	PEG_RXN13
PEG_TXP14	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_T_TXP14	DIS	C576	SCD1U10V2KX-4GP	PEG_RXP14
PEG_TXN14	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_T_TXN14	DIS	C577	SCD1U10V2KX-4GP	PEG_RXN14
PEG_TXP15	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_T_TXP15	DIS	C564	SCD1U10V2KX-4GP	PEG_RXP15
PEG_TXN15	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_T_TXN15	DIS	C562	SCD1U10V2KX-4GP	PEG_RXN15

CLOCK

CLK_PCIE_PEG_P	AB35	PCIE_REFCLKP
CLK_PCIE_PEG_N	AA36	PCIE_REFCLKN

	AJ21	NC#AJ21
	AK21	NC#AK21
PWRGOOD_ATI	AH16	PWRGOOD
ATI_RST#	AA30	PERST#

CALIBRATION

PCIE_CALRP	Y30	GPU_PCIE_CALRP	R758	1K27R2F-L-GP
PCIE_CALRN	Y29	GPU_PCIE_CALRN	R760	2KR2F-3-GP

1.0V_REG

R806 (S) PWRGOOD_ATI 10KR2J-3-GP

C167 (R) SC47P50V2JN-3GP

MADISON-PRO-GP

(M71.ONEGA.M01)

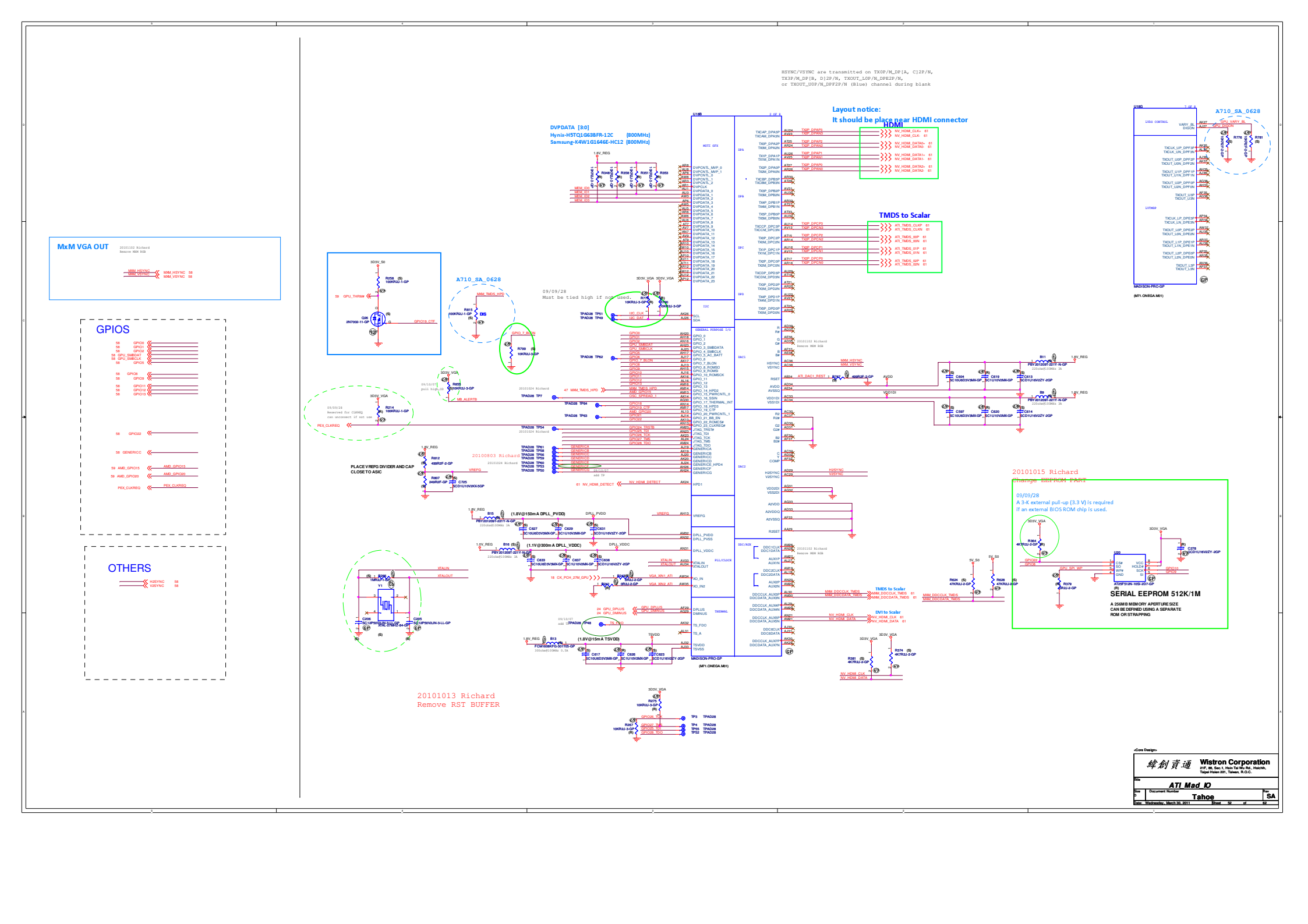
<Core Design>

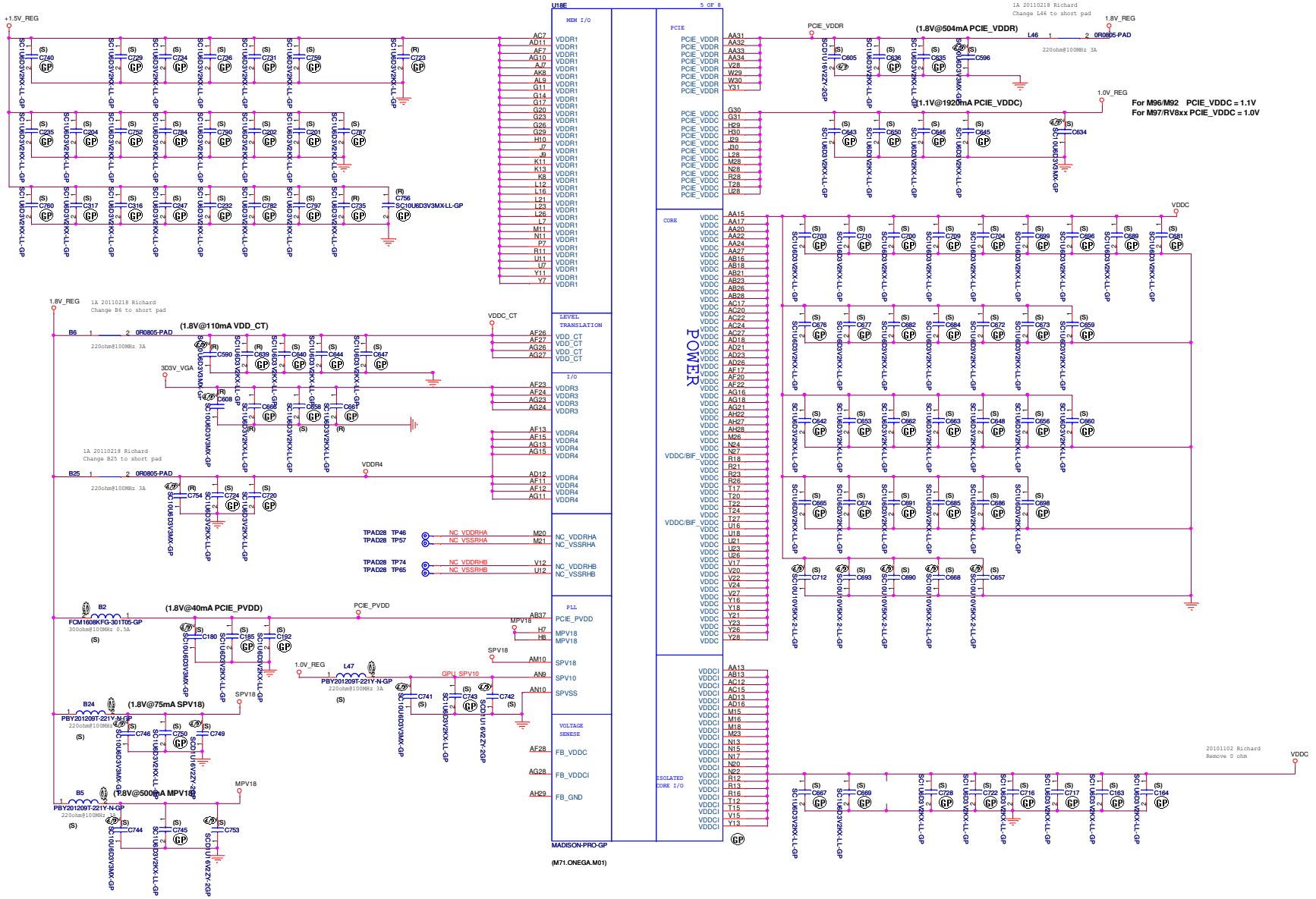
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI Mad PCIE

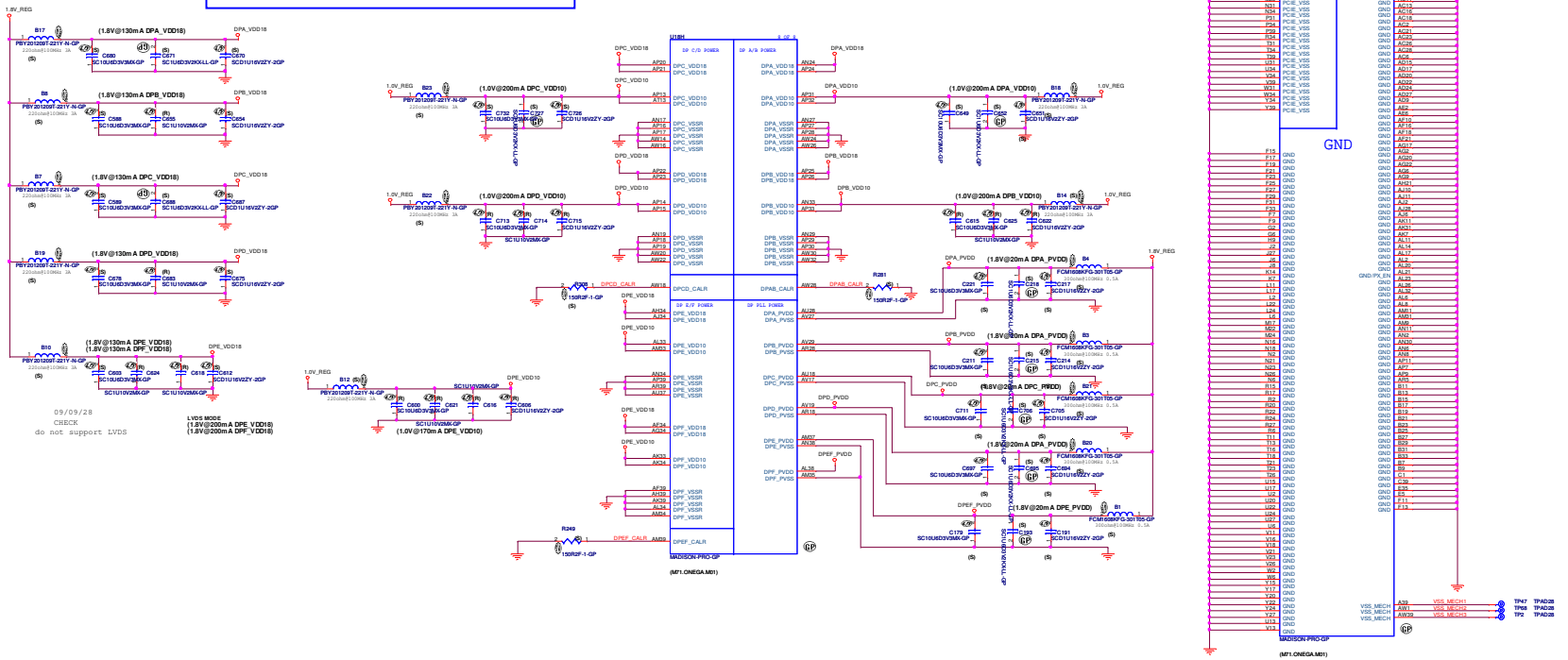
Size: C | Document Number: Tahoe | Rev: SA

Date: Wednesday, March 30, 2011 | Sheet 51 of 62


HSYNC/VSYNC are transmitted on TX0P/M_DP[A, C]2P/N,
TX3P/M_DP[B, D]2P/N, TXOUT_L0P/N_DPE2P/N,
or TXOUT_U0P/N_DPF2P/N (Blue) channel during blank
Layout notice:
It should be place near HDMI connector
HDMI
TMDS to Scalar
DVDATA [3:0]
Hynix-H5TQ1G63BFR-12C (800MHz)
Samsung-K4W1G1646E-HC12 (800MHz)
MxM VGA OUT
GPIOS
OTHERS
09/09/28
Must be tied high if not used.
20101013 Richard
Remove RST BUFFER
20101015 Richard
Change EEPROM PART
09/09/28
A 3-K external pull-up (3.3 V) is required
If an external BIOS ROM chip is used.
SERIAL EEPROM 512K/1M
A 256MB MEMORY APERTURE SIZE
CAN BE DEFINED USING A SEPARATE
ROM OR STRAPPING
PLACE VREFG DIVIDER AND CAP
CLOSE TO ASIC
20100803 Richard
A710_SA_0628
MADISON-PRO-GP
(M71.ONEGA.M01)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATI Mad IO
Tahoe
Wednesday, March 30, 2011

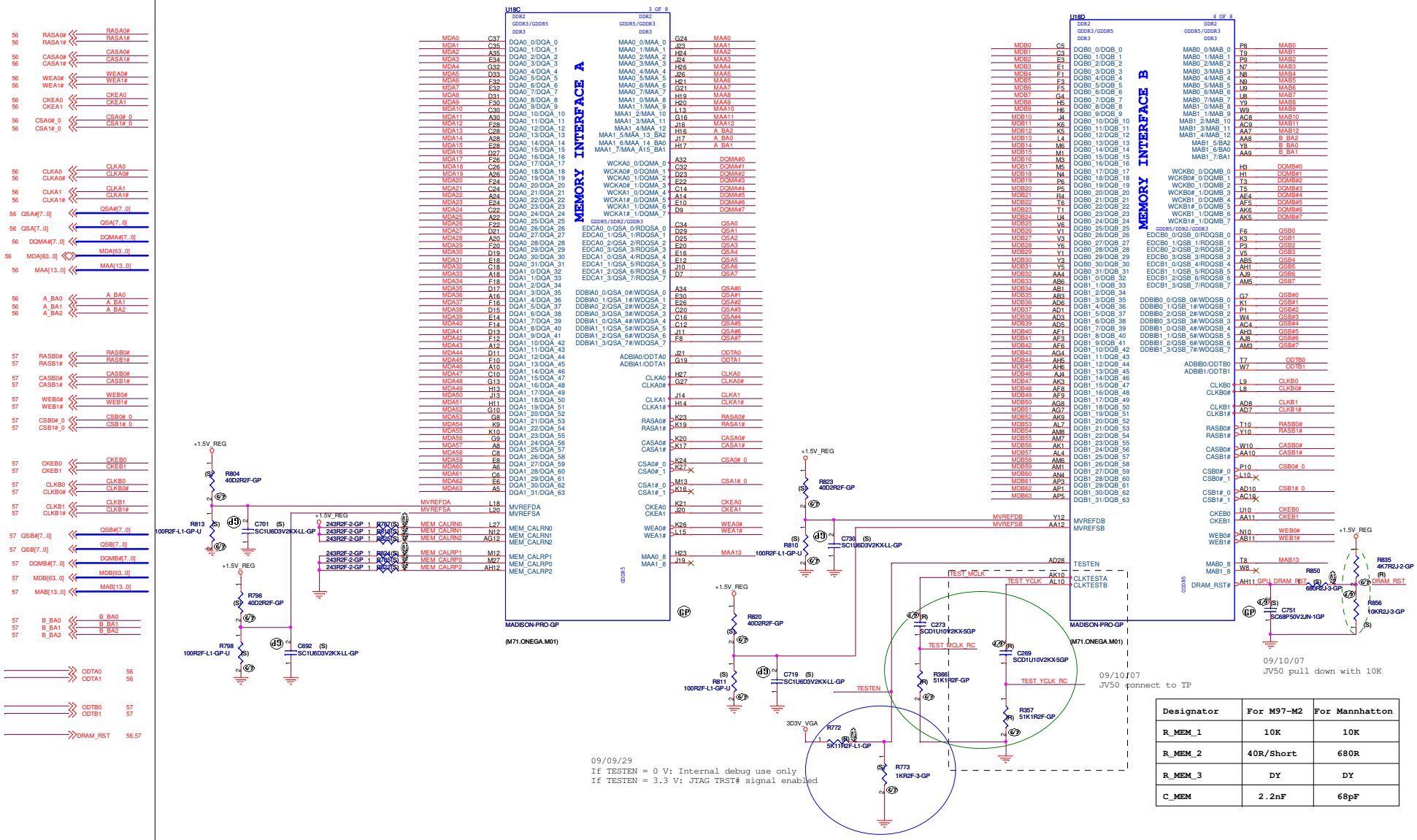

+1.5V_REG
U18E
MEM I/O
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
MADISON-PRO-GP
(M71.ONEGA.M01)
5 OF 8
PCIE
CORE
POWER
VDDC/BIF
ISOLATED CORE I/O
1.8V_REG
1A 20110218 Richard
Change B6 to short pad
(1.8V@110mA VDD_CT)
VDDC_CT
3D3V_VGA
1A 20110218 Richard
Change B25 to short pad
VDDR4
(1.8V@40mA PCIE_PVDD)
PCIE_PVDD
(1.8V@75mA SPV18)
SPV18
1.0V_REG
GPU_SPV10
(1.8V@500mA MPV18)
MPV18
PCIE_VDDR
(1.8V@504mA PCIE_VDDR)
(1.1V@1920mA PCIE_VDDC)
1.0V_REG
For M96/M92 PCIE_VDDC = 1.1V
For M97/RV8xx PCIE_VDDC = 1.0V
VDDC
20101102 Richard
Remove 0 ohm
BACO
needed??
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI_Mad_POWER
Size
C
Document Number
Tahoe
Rev
SA
Date: Wednesday, March 30, 2011
Sheet 53 of 62

09/09/28
For dual-link TMDS, the associated power supply rails can
share the filters/decoupling capacitors.
We use single HDMI, share or ?
need check!



<Core Design>

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ATI DP POWER		
Size: D	Document Number: Tahoe	Rev: SA
Date: Wednesday, March 30, 2011	Sheet 54 of 62	



Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

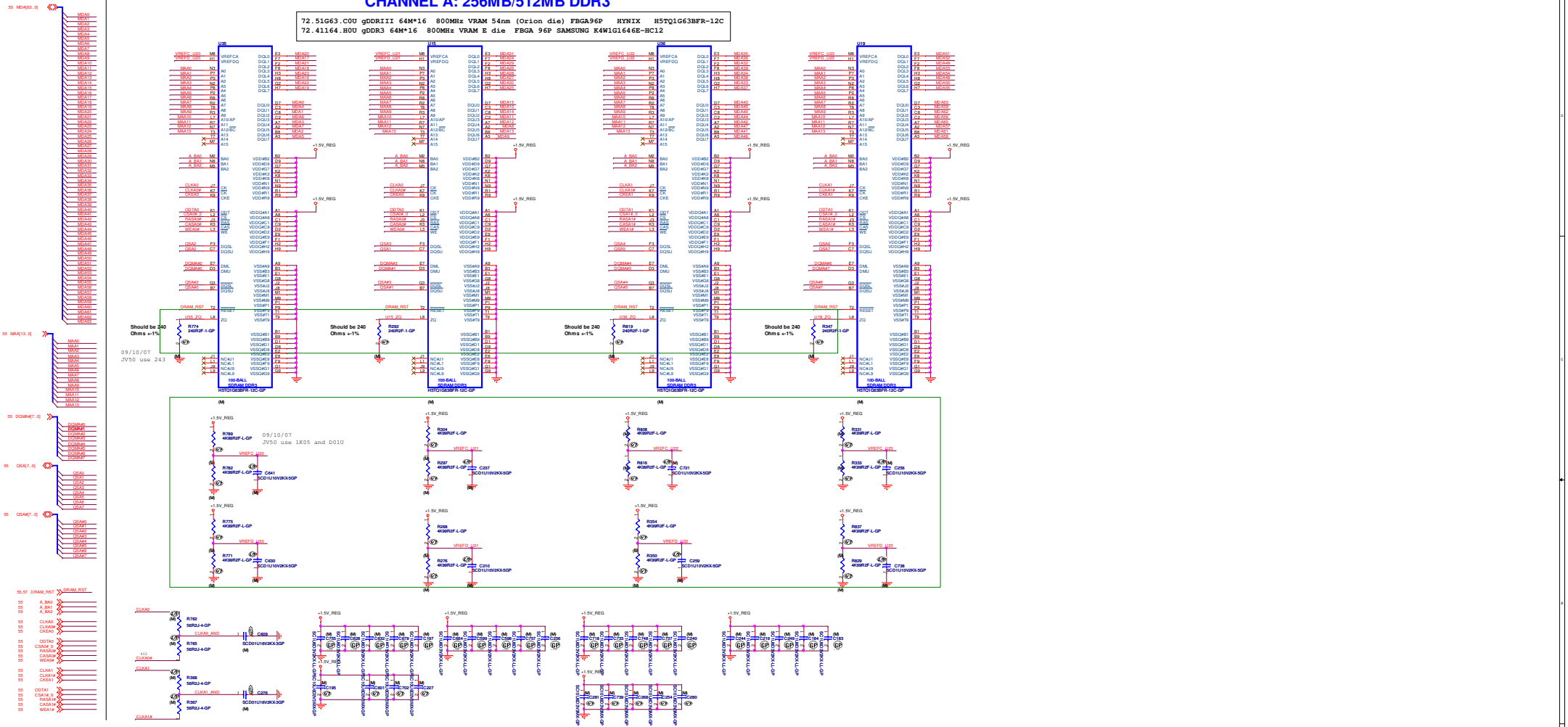
Title: ATI_Mad_MEMORY

Size	Document Number	Rev
C	Tahoe	SA

Date: Wednesday, March 30, 2011 Sheet 55 of 62

CHANNEL A: 256MB/512MB DDR3

72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.H0U gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12



<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI DDR3 64MX16 A

Size	Document Number	Rev
D	Tahoe	SA

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CHANNEL B: 256MB/512MB DDR3

72.51G63.C0U gDDRIII 64M*16 800MHz VRAM 54nm (Orion die) FBGA96P HYNIX H5TQ1G63BFR-12C
72.41164.H0U gDDR3 64M*16 800MHz VRAM E die FBGA 96P SAMSUNG K4W1G1646E-HC12

55 MDB[63..0]
MDB0 MDB1 MDB2 MDB3 MDB4 MDB5 MDB6 MDB7 MDB8 MDB9 MDB10 MDB11 MDB12 MDB13 MDB14 MDB15 MDB16 MDB17 MDB18 MDB19 MDB20 MDB21 MDB22 MDB23 MDB24 MDB25 MDB26 MDB27 MDB28 MDB29 MDB30 MDB31 MDB32 MDB33 MDB34 MDB35 MDB36 MDB37 MDB38 MDB39 MDB40 MDB41 MDB42 MDB43 MDB44 MDB45 MDB46 MDB47 MDB48 MDB49 MDB50 MDB51 MDB52 MDB53 MDB54 MDB55 MDB56 MDB57 MDB58 MDB59 MDB60 MDB61 MDB62 MDB63

55 MAB[13..0]
MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13

55 DQMB#[7..0]
DQMB#0 DQMB#1 DQMB#2 DQMB#3 DQMB#4 DQMB#5 DQMB#6 DQMB#7

55 QSB[7..0]
QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7

55 QSB#[7..0]
QSB#0 QSB#1 QSB#2 QSB#3 QSB#4 QSB#5 QSB#6 QSB#7

55 B_BA0 B_BA1 B_BA2
55 CLKB0 CLKB0# CKEB0
55 ODTB0 CSB0#_0 RASB0# CASB0# WEB0#
55 CLKB1 CLKB1# CKEB1
55 ODTB1 CSB1#_0 RASB1# CASB1# WEB1#

U22 / U38 / U37 / U23
100-BALL SDRAM DDR3
H5TQ1G63BFR-12C-GP (S)

VREFC_U24 VREFD_U24 VREFC_U25 VREFD_U25 VREFC_U26 VREFD_U26 VREFC_U27 VREFD_U27

MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13

B_BA0 B_BA1 B_BA2

CLKB0 CLKB0# CKEB0

ODTB0 CSB0#_0 RASB0# CASB0# WEB0#

CLKB1 CLKB1# CKEB1

ODTB1 CSB1#_0 RASB1# CASB1# WEB1#

+1.5V_REG

Should be 240 Ohms +-1%

55,56 DRAM_RST

R380 240R2F-1-GP
R898 240R2F-1-GP
R875 240R2F-1-GP
R433 240R2F-1-GP

09/10/07
JV50 use 1K05 and D01U

R378 4K99R2F-L-GP
R384 4K99R2F-L-GP
C284 SCD1U10V2KX-5GP
R896 4K99R2F-L-GP
R897 4K99R2F-L-GP
C791 SCD1U10V2KX-5GP
R873 4K99R2F-L-GP
R874 4K99R2F-L-GP
C763 SCD1U10V2KX-5GP
R422 4K99R2F-L-GP
R432 4K99R2F-L-GP
C322 SCD1U10V2KX-5GP
R424 4K99R2F-L-GP
R438 4K99R2F-L-GP
C313 SCD1U10V2KX-5GP
R879 4K99R2F-L-GP
R877 4K99R2F-L-GP
C766 SCD1U10V2KX-5GP
R423 4K99R2F-L-GP
R436 4K99R2F-L-GP
C323 SCD1U10V2KX-5GP
R878 4K99R2F-L-GP
R876 4K99R2F-L-GP
C764 SCD1U10V2KX-5GP

R434 56R2J-4-GP
R435 56R2J-4-GP
R894 56R2J-4-GP
R895 56R2J-4-GP
CLKB0_AND
CLKB1_AND
C324(S) SCD01U50V2KX-1GP
C789(S) SCD01U50V2KX-1GP

SCD1U10V2KX-LL-GP
SCD1U10V3MX-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_DDR3 64MX16 B
Size: C | Document Number: Tahoe | Rev: SA
Date: Wednesday, March 30, 2011 | Sheet 57 of 62

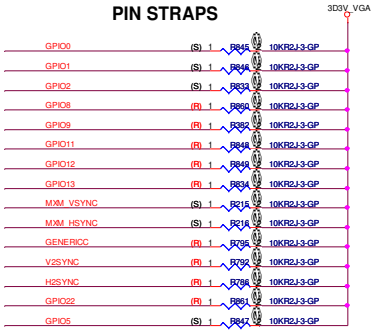
52 GPIO0
52 GPIO1
52 GPIO2
52 GPIO8
52 GPIO9
52 GPIO11
52 GPIO12
52 GPIO13
52 MXM_VSYNC
52 MXM_HSYNC
52 GENERICC
52 V2SYNC
52 H2SYNC
52 GPIO22
52 GPIO5

14,15,16,17,28 SMB_CLK_MAIN
14,15,16,17,28 SMB_DATA_MAIN

59,60 DGPU_PWROK — DGPU_PWROK

52 GPU_SMBCLK — GPU_SMBCLK
52 GPU_SMBDAT — GPU_SMBDAT

PIN STRAPS



	Manufacturer	Part Number	Size	CONFIG[2:0]
STRAP	ST Microelectronics	M25P05A	512 kbit	100

		HSYNC VSYNC
STRAP	Audio for both DisplayPort and HDMI.	11
	Audio for DisplayPort and HDMI if dongle is detected	10

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
BIF_RX_PLL_CALIB_BP	GPIO21	BIF_RX_PLL_CALIB_BP	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	1 0 0
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
SMS_EN_HARD	H2SYNC		0
CCBYPASS	GENERICC		0
AUD[1]	HSYNC	built-in HDMI connector	1
AUD[0]	VSYNC	Audio functiuon present	1

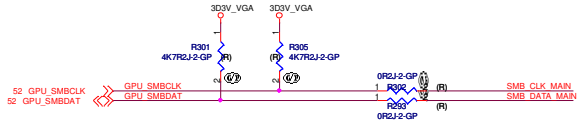
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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For GPU Core and GPIO15/20 relationship as below:

VID1(GPIO20)	VID0(GPIO15)	Core
0	0	1.22V
0	1	1.12V
1	0	1.02V
1	1	0.92V

84.00172.037 SIR172DP
Vgs @ 4.5V,
Id = 13.6A,
Rds(on) = 10.3~12.4mohm,

84.00460.037 SIR460DP
Vgs @ 4.5V,
Id = 10.0A,
Rds(on) = 4.9~6.1mohm,

Vin ripple current Imax=6.04A

DCR=1.6~1.8mohm, Idc=25A

0.92V~1.22V@20A

A710_SA_0624
Change to DIP
820uF/2.5V, ESR=7mohm

VGA power sequence modify!!

20101014 Richard

SB 20101201 Richard

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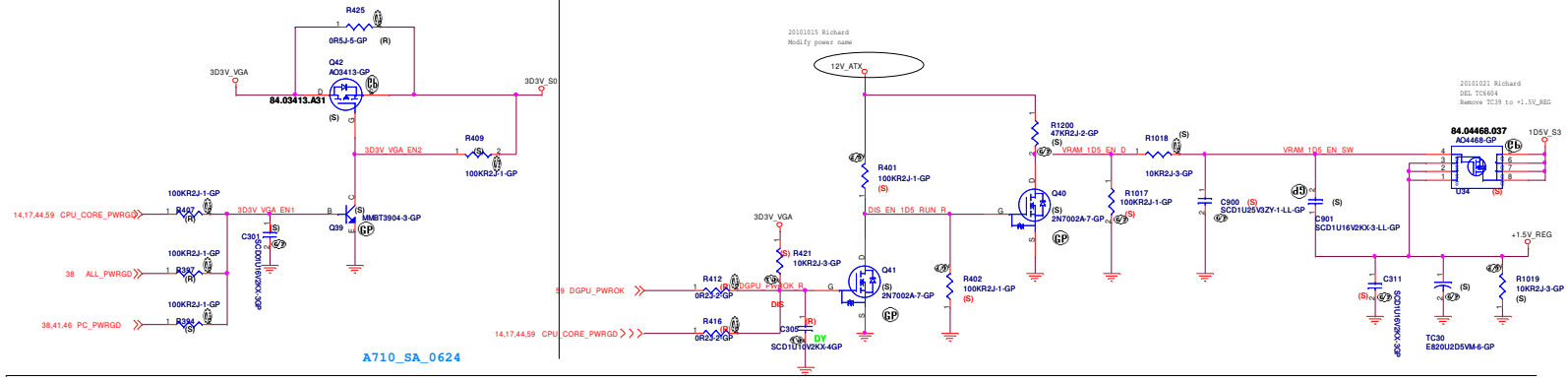
3D3V_S0 to 3D3V_DELAY Transfer

AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm

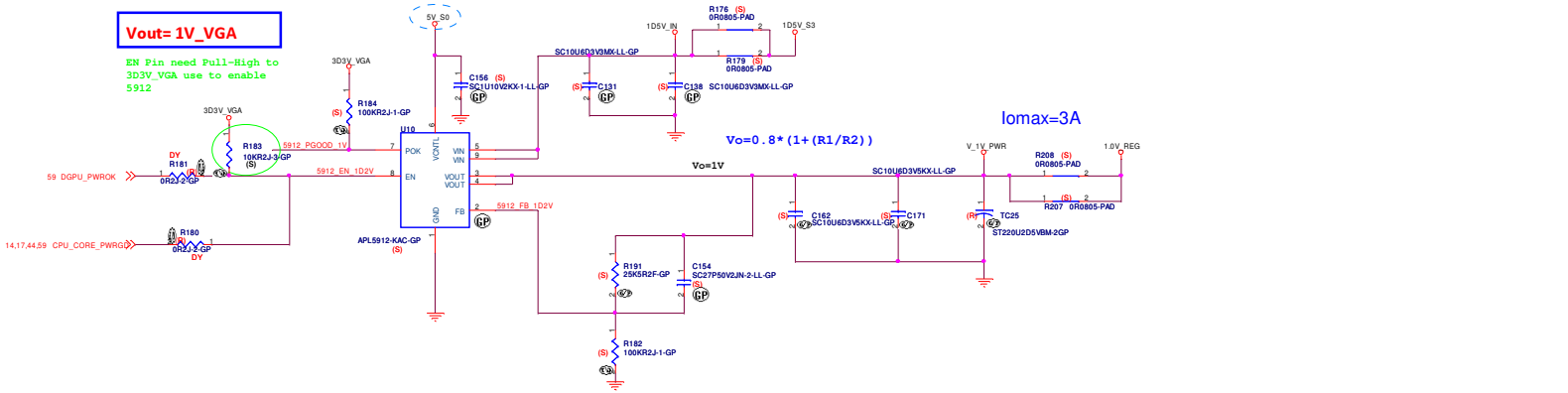
SB 20101214 Richad



A710_SA_0624

Vout= 1V_VGA

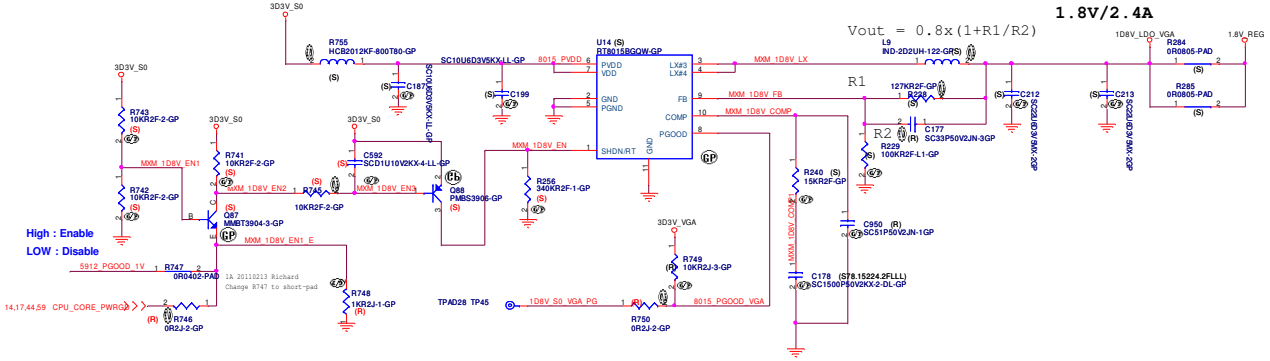
EN Pin need Pull-High to 3D3V_VGA use to enable 5912



1D8V_VGA
(RT8015)

1.8V/2.4A

Vout = 0.8x(1+R1/R2)



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FROM PCH DISPLAY

19 PCH_HDMI_DATA1+
19 PCH_HDMI_DATA1-
19 PCH_HDMI_DATA2+
19 PCH_HDMI_DATA2-
19 PCH_HDMI_CLK+
19 PCH_HDMI_CLK-
19 PCH_HDMI_DATA0+
19 PCH_HDMI_DATA0-
19 PCH_D_HPD
19 PCH_CTRL_CLK
19 PCH_CTRL_DATA

FROM MXM DISPLAY

52 NV_HDMI_DATA1+
52 NV_HDMI_DATA1-
52 NV_HDMI_DATA2+
52 NV_HDMI_DATA2-
52 NV_HDMI_CLK+
52 NV_HDMI_CLK-
52 NV_HDMI_DATA0+
52 NV_HDMI_DATA0-
52 NV_HDMI_DETECT
52 NV_HDMI_CLK
52 NV_HDMI_DATA

To RISER

35 DDSP_D_TX_DP_0
35 DDSP_D_TX_DN_0
35 DDSP_D_TX_DP_1
35 DDSP_D_TX_DN_1
35 DDSP_D_TX_DP_2
35 DDSP_D_TX_DN_2
35 DDSP_D_TX_DP_3
35 DDSP_D_TX_DN_3
35 DDPD_CTRL_CLK
35 DDPD_CTRL_DATA
35 DDSP_D_HPD

PCH DVI-IN

19 PCH_TMDS_00P
19 PCH_TMDS_00N
19 PCH_TMDS_01P
19 PCH_TMDS_01N
19 PCH_TMDS_02P
19 PCH_TMDS_02N
19 PCH_TMDS_CLKP
19 PCH_TMDS_CLKN

ATI DVI-IN

52 ATI_TMDS_00P
52 ATI_TMDS_00N
52 ATI_TMDS_01P
52 ATI_TMDS_01N
52 ATI_TMDS_02P
52 ATI_TMDS_02N
52 ATI_TMDS_CLKP
52 ATI_TMDS_CLKN

TMDS OUT

47 RXCN
47 RXCP
47 RX2P
47 RX2N
47 RX1P
47 RX1N
47 RX0P
47 RX0N

19 SDVO_CTRLDATA
19 SDVO_CTRLCLK
52 MXM_DDCDATA_TMDS
52 MXM_DDCCLK_TMDS
47,48 5VDDCDA_SCALAR
47,48 5VDDCCLK_SCALAR

HDMI

3D3V_S0
R689 2K2R2J-2-GP
PCH_CTRL_CLK R672 (U) 0R2J-2-GP
NV_HDMI_CLK R674 (S) 0R2J-2-GP
DDPD_CTRL_CLK
C480 SC470P50V2KX-3GP (R)

3D3V_S0
R690 2K2R2J-2-GP
PCH_CTRL_DATA R670 (U) 0R2J-2-GP
NV_HDMI_DATA R669 (S) 0R2J-2-GP
DDPD_CTRL_DATA
C469 SC470P50V2KX-3GP (R)

PCH_D_HPD R1003 (U) 0R2J-2-GP
NV_HDMI_DETECT R1002 (S) 0R2J-2-GP
DDSP_D_HPD

3D3V_S0
R515 10KR2J-3-GP
SDVO_CTRLDATA R521 (U) 33R2J-2-GP 5VDDCDA_SCALAR
MXM_DDCDATA_TMDS R826 (S) 33R2J-2-GP

3D3V_S0
R513 10KR2J-3-GP
SDVO_CTRLCLK R510 (U) 33R2J-2-GP 5VDDCCLK_SCALAR
MXM_DDCCLK_TMDS R827 (S) 33R2J-2-GP

20101028 Richard
PCH DVI LEVEL SHIFT & AC CAP
Combine with MXM

SB 20101201 Richard

PCH_HDMI_DATA0+ C863(U) SCD1U10V2KX-5GP → DDSP_D_TX_DP_0
PCH_HDMI_DATA0- C862(U) SCD1U10V2KX-5GP → DDSP_D_TX_DN_0
NV_HDMI_DATA0+ C474(S) SCD1U10V2KX-5GP
NV_HDMI_DATA0- C475(S) SCD1U10V2KX-5GP

PCH_HDMI_DATA1+ C865(U) SCD1U10V2KX-5GP → DDSP_D_TX_DP_C_1 → DDSP_D_TX_DP_1
PCH_HDMI_DATA1- C864(U) SCD1U10V2KX-5GP → DDSP_D_TX_DN_C_1 → DDSP_D_TX_DN_1
NV_HDMI_DATA1+ C472(S) SCD1U10V2KX-5GP
NV_HDMI_DATA1- C473(S) SCD1U10V2KX-5GP

PCH_HDMI_DATA2+ C867(U) SCD1U10V2KX-5GP → DDSP_D_TX_DP_C_2 → DDSP_D_TX_DP_2
PCH_HDMI_DATA2- C866(U) SCD1U10V2KX-5GP → DDSP_D_TX_DN_C_2 → DDSP_D_TX_DN_2
NV_HDMI_DATA2+ C470(S) SCD1U10V2KX-5GP
NV_HDMI_DATA2- C471(S) SCD1U10V2KX-5GP

PCH_HDMI_CLK+ C861(U) SCD1U10V2KX-5GP → DDSP_D_TX_DP_C_3 → DDSP_D_TX_DP_3
PCH_HDMI_CLK- C860(U) SCD1U10V2KX-5GP → DDSP_D_TX_DN_C_3 → DDSP_D_TX_DN_3
NV_HDMI_CLK+ C476(S) SCD1U10V2KX-5GP
NV_HDMI_CLK- C477(S) SCD1U10V2KX-5GP

5V_S0 R997 DIS 100KR2J-1-GP HDMI_LEVEL_G
R964 100KR2J-1-GP DIS
2N7002-11-GP Q101
HDMI_LEVEL
R1004 R1005 R1010 R1011 R1008 R1009 R1006 R1007 10KR2F-2-GP

20101028 Richard
PCH DVI LEVEL SHIFT & AC CAP
Combine with MXM

DIGITAL SIGNAL IN

ATI_TMDS_CLKN C347(S) SCD1U10V2KX-5GP
PCH_TMDS_CLKN C348(U) SCD1U10V2KX-5GP
ATI_TMDS_CLKP C351(S) SCD1U10V2KX-5GP
PCH_TMDS_CLKP C352(U) SCD1U10V2KX-5GP
ATI_TMDS_02P C802(S) SCD1U10V2KX-5GP
PCH_TMDS_02P C341(U) SCD1U10V2KX-5GP
ATI_TMDS_02N C801(S) SCD1U10V2KX-5GP
PCH_TMDS_02N C346(U) SCD1U10V2KX-5GP
ATI_TMDS_01P C328(S) SCD1U10V2KX-5GP
PCH_TMDS_01P C329(U) SCD1U10V2KX-5GP
ATI_TMDS_01N C325(S) SCD1U10V2KX-5GP
PCH_TMDS_01N C326(U) SCD1U10V2KX-5GP
ATI_TMDS_00P C331(S) SCD1U10V2KX-5GP
PCH_TMDS_00P C332(U) SCD1U10V2KX-5GP
ATI_TMDS_00N C334(S) SCD1U10V2KX-5GP
PCH_TMDS_00N C335(U) SCD1U10V2KX-5GP
Place near SCALAR

RXCN
RXCP
RX2P
RX2N
RX1P
RX1N
RX0P
RX0N

5V_S0 R507 DIS 100KR2J-1-GP TMDS_LEVEL_G
R509 100KR2J-1-GP DIS
2N7002-11-GP Q45
TMDS_LEVEL
R904 R903 R900 R901 R470 R461 R917 R910 10KR2F-2-GP

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VGA IN

35 RED_IN_CONN
35 GREEN_IN_CONN
35 BLUE_IN_CONN
35 HSYNC_IN_CON
35 VSYNC_IN_CON
35,47 CRT_DDC_IN_CLK
35,47 CRT_DDC_IN_DATA

VGA To Scalar

47 RTD_RP
47 RTD_RN
47 RTD_GP
47 RTD_GN
47 RTD_BP
47 RTD_BN
47 SOG
47 DDC_WP
47 HSYNC_IN
47 VSYNC_IN

RGB

LPF place near Scalar

RED_IN_CONN → L36 0R0603-PAD → VGA_RED_1 → C439(R) SC5P50V2CN-2GP, R636(R) 75R2F-2-GP → L33 0R0603-PAD → VGA_RED_2 → C431(R) SC5P50V2CN-2GP → R605 75R2F-2-GP → C424 SCD047U16V2KX-1-GP → RTD_RP 47

VGA_RED- → R604 100R2F-L1-GP-U → VGA_RED-_1 → C423 SCD047U16V2KX-1-GP → RTD_RN 47

GREEN_IN_CONN → L35 0R0603-PAD → VGA_GREEN_1 → C438 SC5P50V2CN-2GP (R), R635(R) 75R2F-2-GP → L32 0R0603-PAD → VGA_GREEN_2 → C430(R) SC5P50V2CN-2GP → R602 75R2F-2-GP → C421 SCD047U16V2KX-1-GP → RTD_GP 47

VGA_GRN- → R601 100R2F-L1-GP-U → VGA_GRN-_1 → C420 SCD047U16V2KX-1-GP → RTD_GN 47

Use 11 ohm(monitor)

Use75ohm now
Use 50 ohm(monitor)

20110320 Richard -1
Change L31 L32 L33 to short pad

R603 475R2F-L1-GP → VGA_GREEN_5 → C422 SCD047U16V2KX-1-GP → SOG 47

Use 470 ohm

R580 1MR2J-1-GP (R)

BLUE_IN_CONN → L34 0R0603-PAD → VGA_BLUE_1 → C437 SC5P50V2CN-2GP (R), R634(R) 75R2F-2-GP → L31 0R0603-PAD → VGA_BLUE_2 → C429(R) SC5P50V2CN-2GP → R600 75R2F-2-GP → C419 SCD047U16V2KX-1-GP → RTD_BP 47

VGA_BLU- → R599 100R2F-L1-GP-U → VGA_BLU-_1 → C418 SCD047U16V2KX-1-GP → RTD_BN 47

SYNC

HSYNC_IN_CON → R614 0R0402-PAD → HSYNC_IN_CON1 → R588 100R2J-2-GP → HSYNC_IN
VSYNC_IN_CON → R587 100R2J-2-GP → VSYNC_IN

R597 2KR2J-1-GP, R598 2KR2J-1-GP
C414 SC22P50V2JN-4GP, C415 SC22P50V2JN-4GP

EDID

20101014 RICHARD
RANAME POWER NAME

2010/02/01
VGA connector
PIN 5 (GND)

5V_S0 → D26 RB751V-40-2-GP → DDC5V_VGA
5V_VGA_IN → D24 BAT54C-GP-U
D25 BZX84-C6V8-GP, C831 SCD1U16V2KX-3GP (R)

R999 4K7R2J-2-GP, R995 4K7R2J-2-GP
C850 SCD1U16V2ZY-2GP

R989 10KR2J-3-GP → R992 100R2J-2-GP → DDC_WP 47

VGA_WP

CRT_DDC_IN_CLK → R996 22R2J-2-GP → DDC_SCL_VGA1
CRT_DDC_IN_DATA → R1000 22R2J-2-GP → DDC_SDA_VGA1

U45 M24C02-WMN6TP-GP-U
VCC, WC#, SCL, SDA, E0, E1, E2, VSS

D28 BZX84-C6V8-GP, D27 BZX84-C6V8-GP
C858, C855(V) SC47P50V2JN-3GP

Use 33ohm,replace47

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