GA-MA785GMT-UD2H

Revision : 3.3

PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRIII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRIII CHANNEL A
09	DDRIII CHANNEL B
10	RS880 HT-LINK I/F
11	RS880 PCIE I/F
12	RS880 SYSTEM I/F
13	RS880 STRAP ,SPMEM
14	RS880 POWER & GND
15	ICS9LPRS477
16	ATI SB710 PCIE/PCI/CPU/LPC
17	ATI SB710 ACPI/USB/GPIO/AUDIO
18	ATI SB710 SATA/SPI/IDE/HWM
19	ATI SB710 POWER & GND
20	PCI EXPRESS x16 ,x1
21	PCI SLOT 1, 2
22	RGB Connector
23	IDE ,FDD ,HDMI ,DVI Connector
24	COM/LPT/F_USB
25	ALC889A

PAGE	TITLE
26	AUDIO JACK
27	IT8718 LPC IO ,Dual-BIOS
28	FAN/HWMO KB/USB
29	ATX, FRONT PANEL
30	VCORE (PWMISL6324A+6612A)
31	POWER SEQUENCE ,EUP
32	NB/SB POWER, VCC12HT, VDDA25 ,VCC12_Dual
33	DDR POWER, VCC18
34	REALTK RTL8111C/8101E
35	TI TSB43AB23 1394A

GIGABYTE

Title: COVER SHEET		
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 1 of 35	

Model Name:GA-MA785GMT-UD2H

Component value change history

Version: 3.3

P-Code: U97028-0

Date	Change Item	Reason
2008.05.08	0.1 New BOM Release.	Modify from 9MMA78G2H-00-11C
2008.05.30	1.0A BOM Release.	Fixed CPU C1 reset issue ,Add SB OV
2008.09.16	1.0B BOM Release.	Improve PWM ISL6324 Comp/APA value for Intersil recommend
2008.10.29	0.1 New BOM Release.	Modify from MA78GPM-DS2H 1.0
2008.11.26	0.2 New BOM Release.	Modify from MA78GPM-UD2H 0.1 , Change spec.
2008.12.22	1.0A BOM Release	Modify SPI BIOS I/F FROM SB
2009.04.23	2.0A BOM Release	Modify from 9MMA78PU2-00-10A Co-Lay PCB GA-MA78GPM-UD2H/GA-MA78GM-UD2H/GA-MA78GM-US2H
2009.05.07	0.1 BOM Release	Modify from 9MMA78PU2-00-20A
2009.06.11	1.0A BOM Release	Modify from 9MMA78TU2-00-01
2009.06.18	1.0B BOM Release	Co-Lay EC-Cap
2009.08.05	1.0H BOM Release.	Change Sideport memory from Elpida to Hynix
2009.10.22	1.1A BOM Release	Add EUP function ,Colay ALC892
2009.10.23	1.1A BOM Release	share PCB FROM MA785GPMT-UD2H 1.1A ,remove sideport memory
2009.11.16	1.1B BOM Release	Modify 5VDual protect schematic
2010.03.01	1.3A BOM Release	For Turbo 3D feature ,Modify NB_HS ,Add Sticker
2010.04.20	3.3A BOM Release	Modify Fuse F1,F2,F5 to 3.5A for F_USB port 3倍力

Circuit or PCB layout change for next version

Date	Change Item	Reason
2008.05.07	Rev0.1 Gerber-out	Modify from GA-MA78GM-S2H Rev1.1
2008.05.30	Rev1.0 Gerber-out	Modify NP 孔距 Foot-print ,Remove 未上件 DIP EC-cap , Modify DBIOS_RST- signal
2008.11.26	Rev0.2 Gerber-out	Change SB Chipset to SB750 and Add ACC Function / RAID 5
2008.12.22	Rev1.0 Gerber-out	Modify SPI BIOS I/F FROM SB
2009.04.22	Rev2.0 Gerber-out	Modify from GA-MA78GPM-UD2H Rev1.0 Co-Lay PCB GA-MA78GPM-UD2H/GA-MA78GM-UD2H/GA-MA78GM-US2H
2009.05.06	Rev0.1 Gerber-out	Modify from GA-MA78GPM-UD2H Rev2.0
2009.06.10	Rev1.0 Gerber-out	Modify from GA-MA78GMT-UD2H Rev0.1
2009.06.11	Rev1.0 Gerber-out	Co-Lay PCB GA-MA785GPMT-UD2H/GA-MA785GMT-UD2H
2009.06.16	Rev1.01 Gerber-out	Co-Lay EC-Cap
2009.10.21	Rev1.1 Gerber-out	Add EUP function ,Colay ALC892
2009.11.13	Rev1.11 Gerber-out	Modify 5VDual protect schematic
2010.02.26	Rev1.3 Gerber-out	For Turbo 3D feature ,Modify NB_HS ,Add Sticker
2010.04.19	Rev3.3 Gerber-out	Modify silk-screen for F_USB port 3倍力

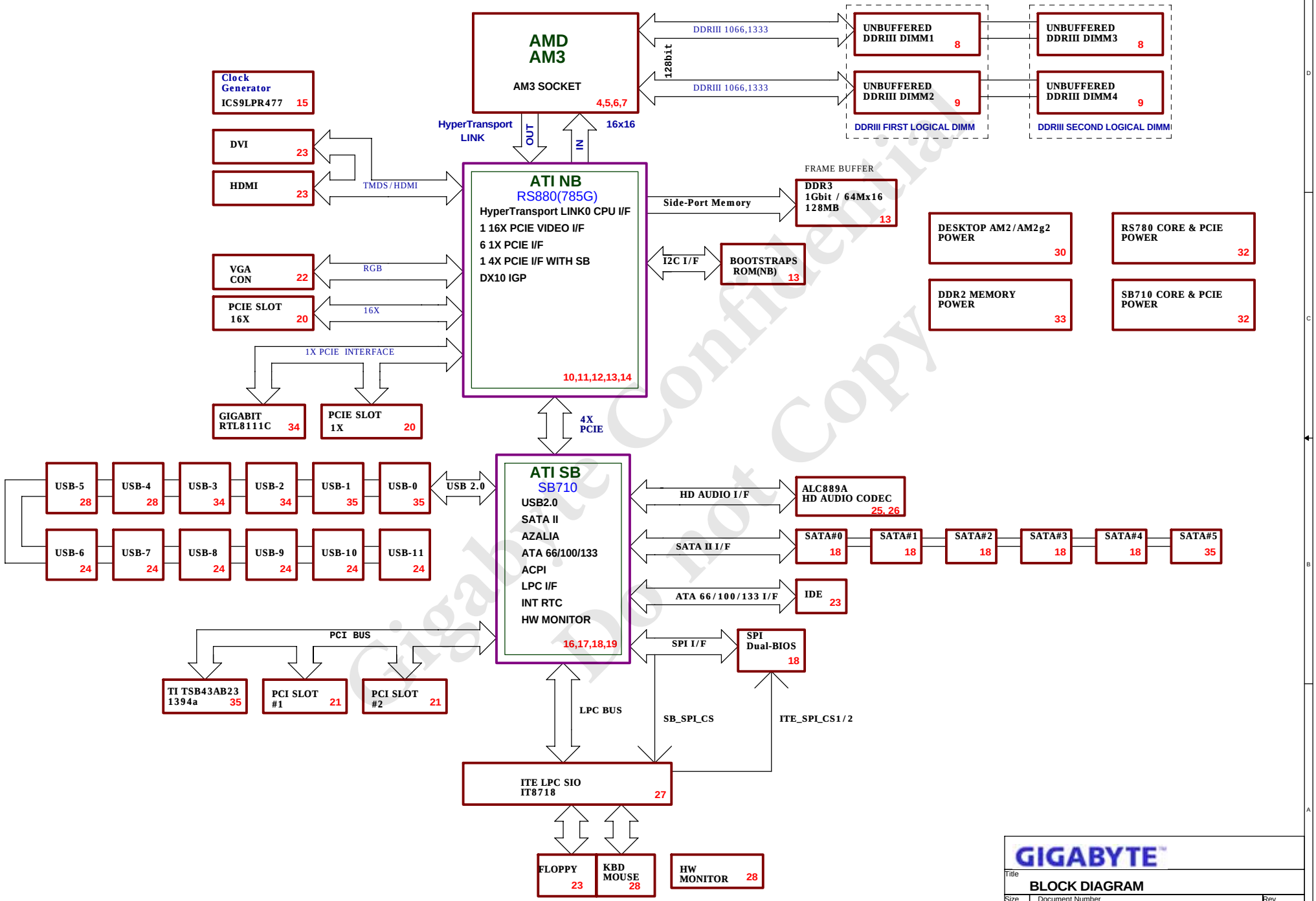
GIGABYTE

Title: BOM & PCB HISTORY

Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

Date: Monday, April 19, 2010 | Sheet 2 of 35

RS880 CUSTOMER DESKTOP REFERENCE DESIGN



GIGABYTE

Title: BLOCK DIAGRAM

Size	Document Number	Rev
Custom	GA-MA785GMT-UD2H	3.3

Date: Monday, April 19, 2010 Sheet 3 of 35

L0_CADIN_L[0..15]
L0_CADIN_H[0..15]
L0_CADOUT_L[0..15]
L0_CADOUT_H[0..15]

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AE6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE5	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF4	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AH6	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AG6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AH5	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH4	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)		L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AF1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/GF/[10SC1-A01941-01R]

M2CPU

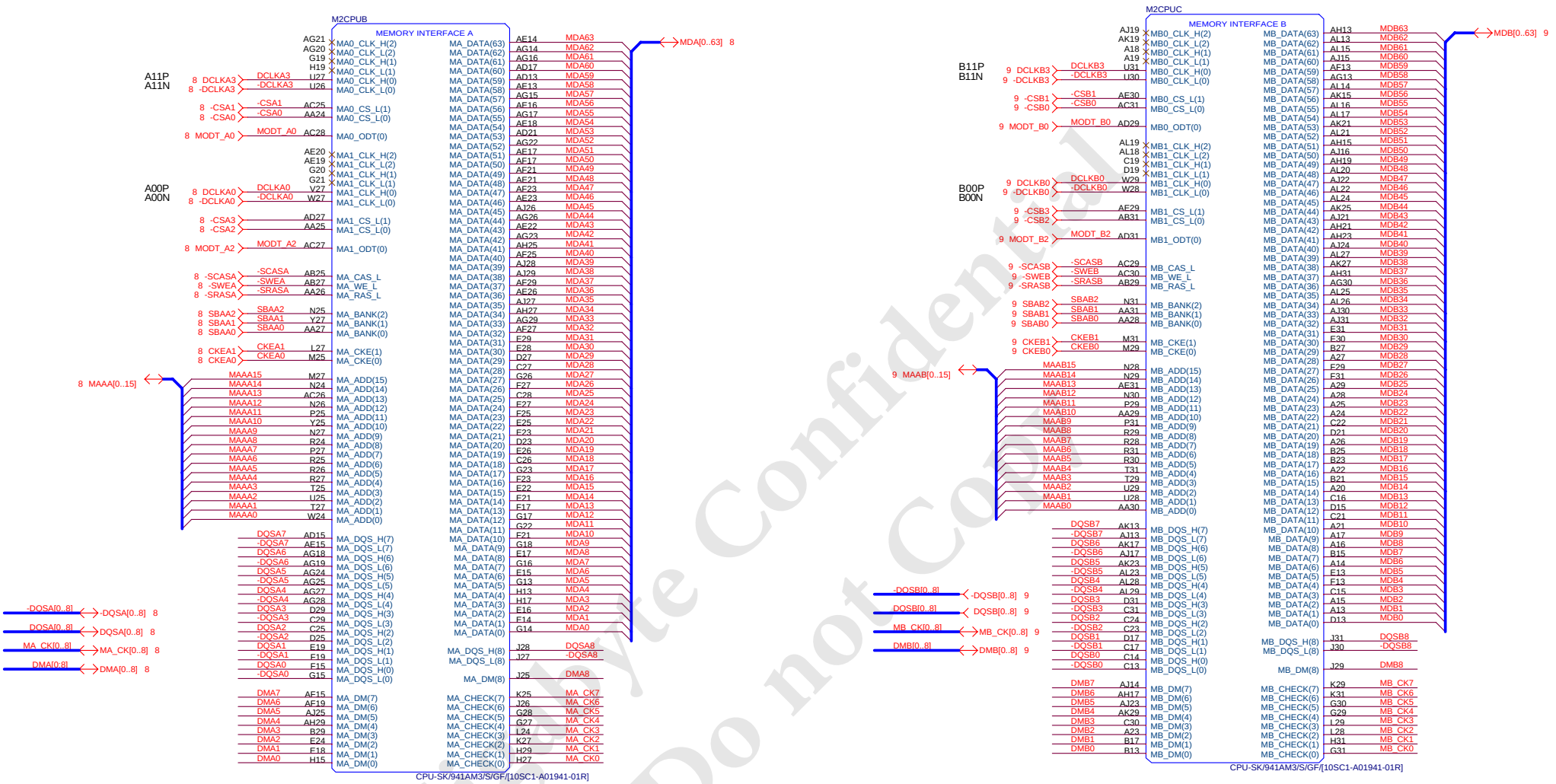
AM2RM/PP/BU/PB/[12KRC-04K812-11R]

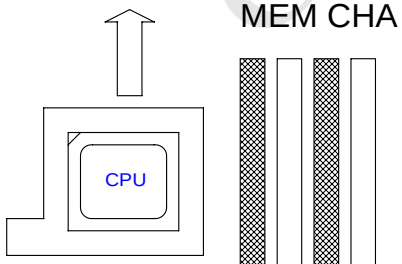
GIGABYTE

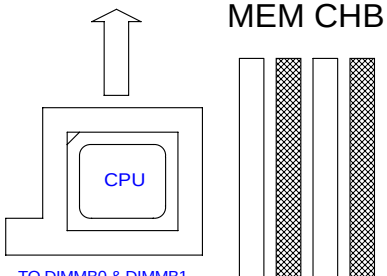
Title: CPU HYPER TRANSPORT

Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

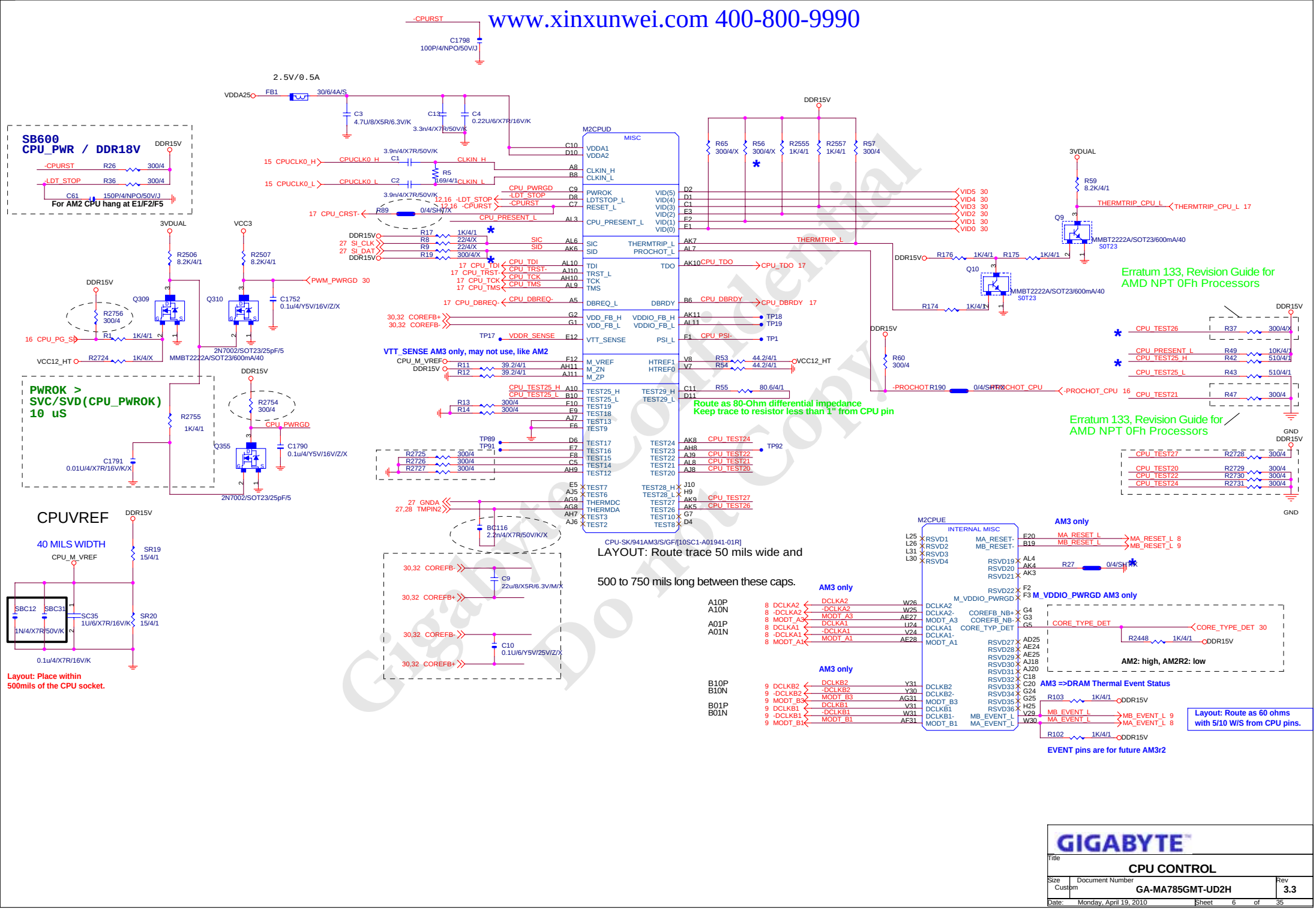
Date: Monday, April 19, 2010 | Sheet 4 of 35







GIGABYTE			
Title: CPU DDRIII MEMORY			
Size: Custom	Document Number: GA-MA785GMT-UD2H		Rev: 3.3
Date: Monday, April 19, 2010	Sheet 5 of 35		



VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.

M2CPUE
VDD1

VCORE_NB
VCORE

AE9 Missing pins on package and socket used for mechanical keying. =>AM3

M2CPUG
VDD2
VCORE

H22 Missing pins on package and socket used for mechanical keying. =>AM3

M2CPUH
VDD3
VCORE

B2 NB/RSVD
AM3 Only
H20 NP/VSS1
AF7 NP/VSS2

M2CPUI
VDDIO
VCC12_HT
CPU_VDDR12
DDR15V

VCORE_NB
C1347 22u/8/X5R/6.3V/M
C1344 22u/8/X5R/6.3V/M
C1343 1U/6/X7R/16V/K
C1342 0.1u/4/X7R/16V/K
C1345 0.01U/4/X7R/25V/K
C1346 180P/4/NPO/50V/J
GND

HT12B
BC795 4.7U/8/X5R/6.3V/K
GND

CPU_VDDR12

DDR15V
BUTTOM SIDE
SC2 0.22U/6/X7R/16V/K
SC4 0.22U/6/X7R/16V/K
SC5 0.01U/4/X7R/25V/K
SC6 180P/4/NPO/50V/J
SC9 22u/8/X5R/6.3V/M
SC10 22u/8/X5R/6.3V/M
SC7 4.7U/8/X5R/6.3V/K
SC8 4.7U/8/X5R/6.3V/K
SC31 180P/4/NPO/50V/J
GND

VCORE
BUTTOM SIDE
SC11 0.22U/6/X7R/16V/K
SC12 0.22U/6/X7R/16V/K
SC13 0.22U/6/X7R/16V/K
SC14 0.01U/4/X7R/25V/K
SC15 180P/4/NPO/50V/J
GND

VCORE
BUTTOM SIDE
SC16 22u/8/X5R/6.3V/M
SC17 22u/8/X5R/6.3V/M
SC18 22u/8/X5R/6.3V/M
SC19 22u/8/X5R/6.3V/M
SC20 22u/8/X5R/6.3V/M
SC21 22u/8/X5R/6.3V/M
SC22 22u/8/X5R/6.3V/M
SC23 22u/8/X5R/6.3V/M
SC24 22u/8/X5R/6.3V/M
SC25 22u/8/X5R/6.3V/M
SC26 22u/8/X5R/6.3V/M
SC27 22u/8/X5R/6.3V/M
SC28 22u/8/X5R/6.3V/M
SC29 22u/8/X5R/6.3V/M
SC30 22u/8/X5R/6.3V/M
GND

VCC12_HT
C1328 4.7U/8/X5R/6.3V/K
C1329 4.7U/8/X5R/6.3V/K
C1330 0.22U/6/X7R/16V/K
C1331 0.22U/6/X7R/16V/K
C1332 180P/4/NPO/50V/J
C1333 180P/4/NPO/50V/J
GND

DDR15V
C1324 4.7U/8/X5R/6.3V/K
C1325 4.7U/8/X5R/6.3V/K
C1326 0.22U/6/X7R/16V/K
C1327 0.22U/6/X7R/16V/K
C1337 0.22U/6/X7R/16V/K
C1319 0.22U/6/X7R/16V/K
GND

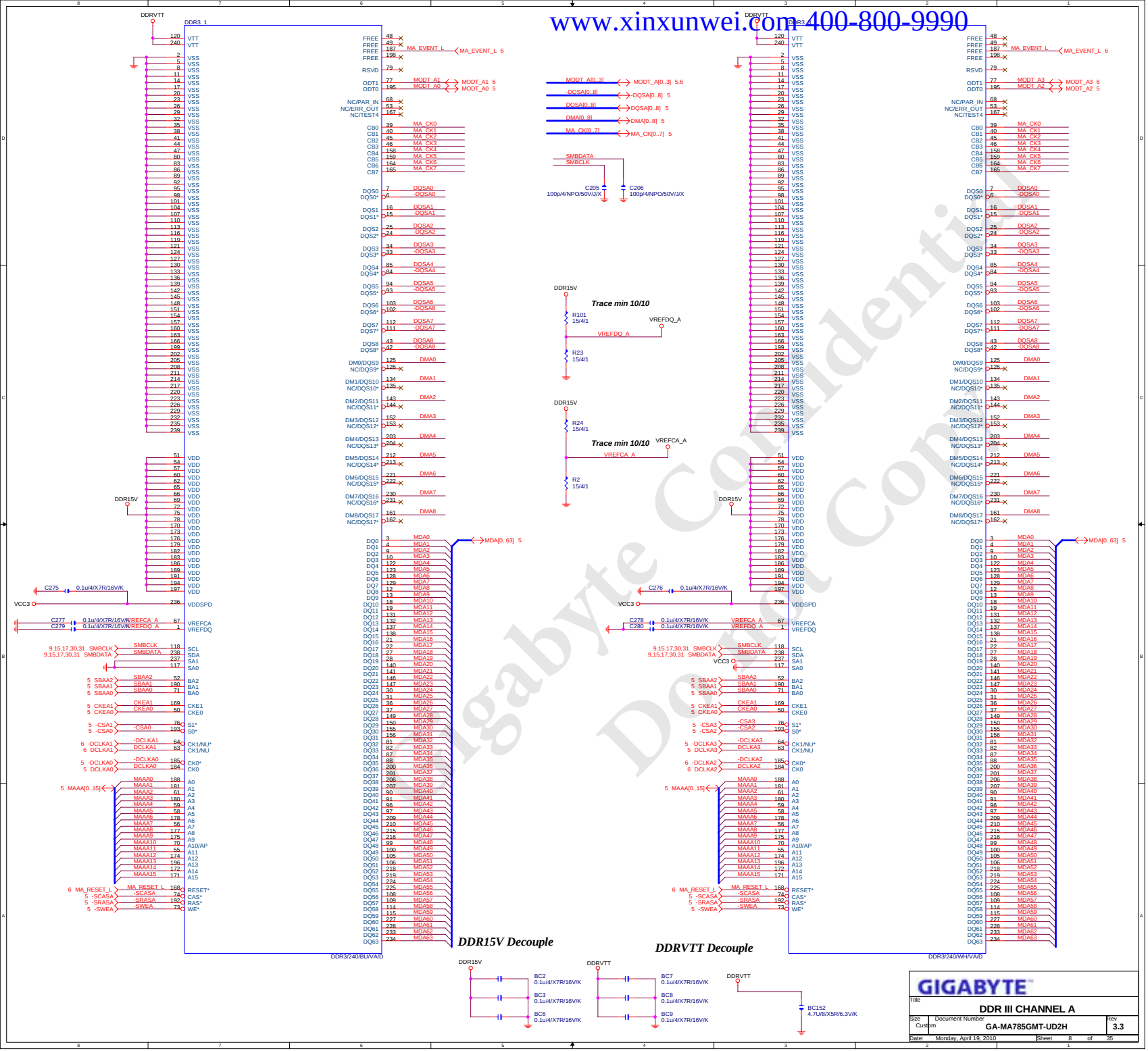
CPU_VDDR12
C1316 4.7U/8/X5R/6.3V/K
C1317 4.7U/8/X5R/6.3V/K
C1318 0.22U/6/X7R/16V/K
C1320 1N/4/X7R/50V/K
C1321 1N/4/X7R/50V/K
C1322 180P/4/NPO/50V/J
C1323 180P/4/NPO/50V/J
GND

CPU_VDDR12
C1334 4.7U/8/X5R/6.3V/K
C1335 4.7U/8/X5R/6.3V/K
C1336 0.22U/6/X7R/16V/K
C1338 1N/4/X7R/50V/K
C1339 1N/4/X7R/50V/K
C1340 180P/4/NPO/50V/J
C1341 180P/4/NPO/50V/J
GND

1021 EMI
CPU_VDDR12
BC20 100P/4/NPO/50V/J
BC23 100P/4/NPO/50V/J
BC24 100P/4/NPO/50V/J
BC25 100P/4/NPO/50V/J
GND

GIGABYTE

Title	CPU POWER & GND	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 7 of 35	

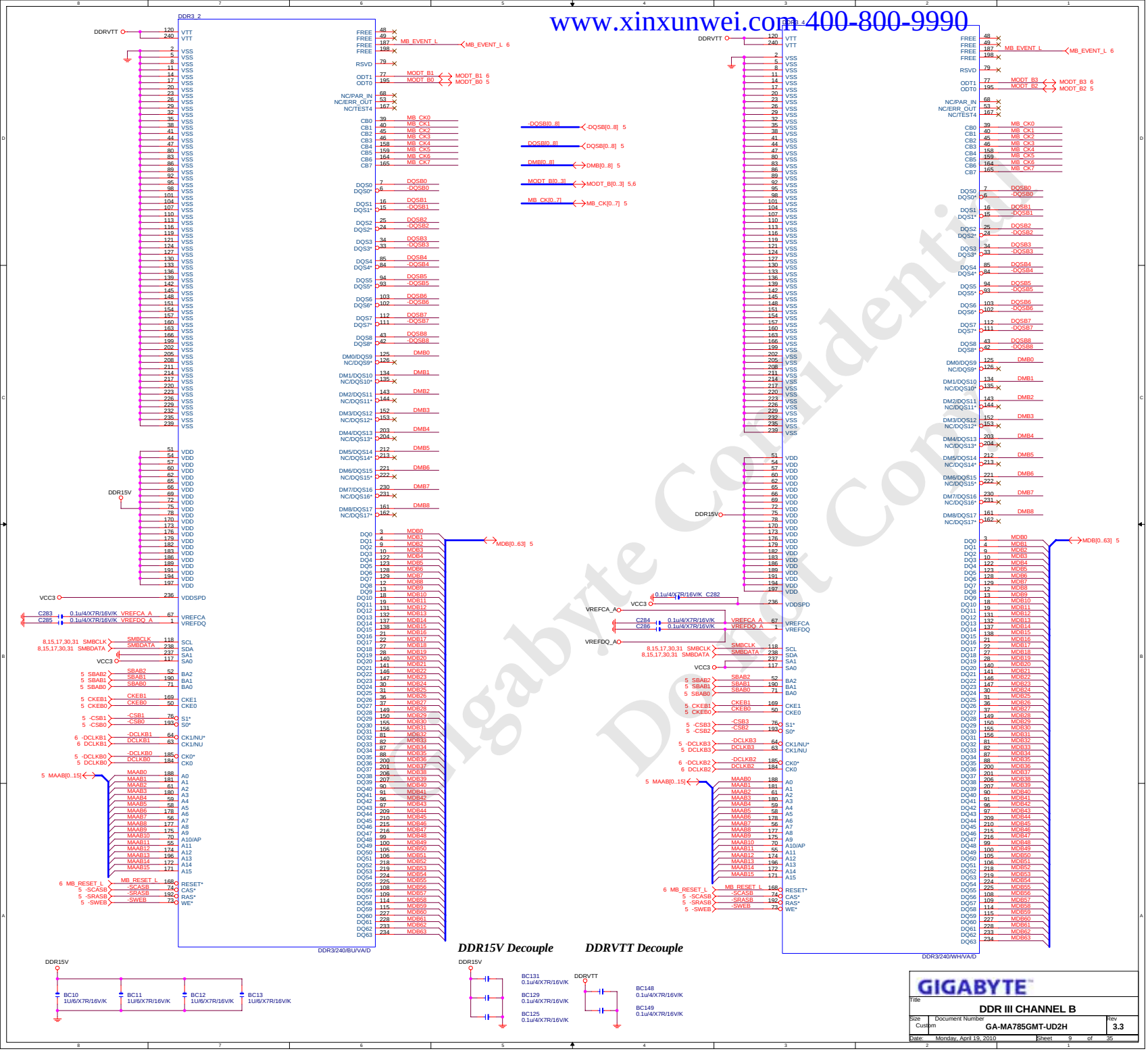


GIGABYTE

Title: DDR III CHANNEL A

Size	Document Number	Rev
Custom	GA-MA785GMT-UD2H	3.3

Date: Monday, April 19, 2010 Sheet 8 of 35

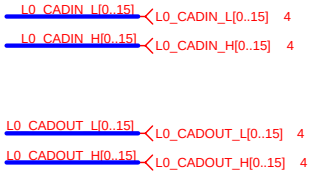


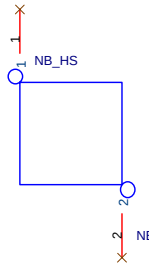
GIGABYTE

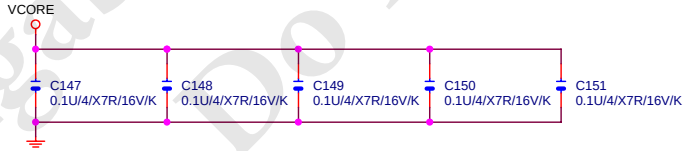
Title: DDR III CHANNEL B

Size	Document Number	Rev
Custom	GA-MA785GMT-UD2H	3.3

Date: Monday, April 19, 2010 Sheet 9 of 35







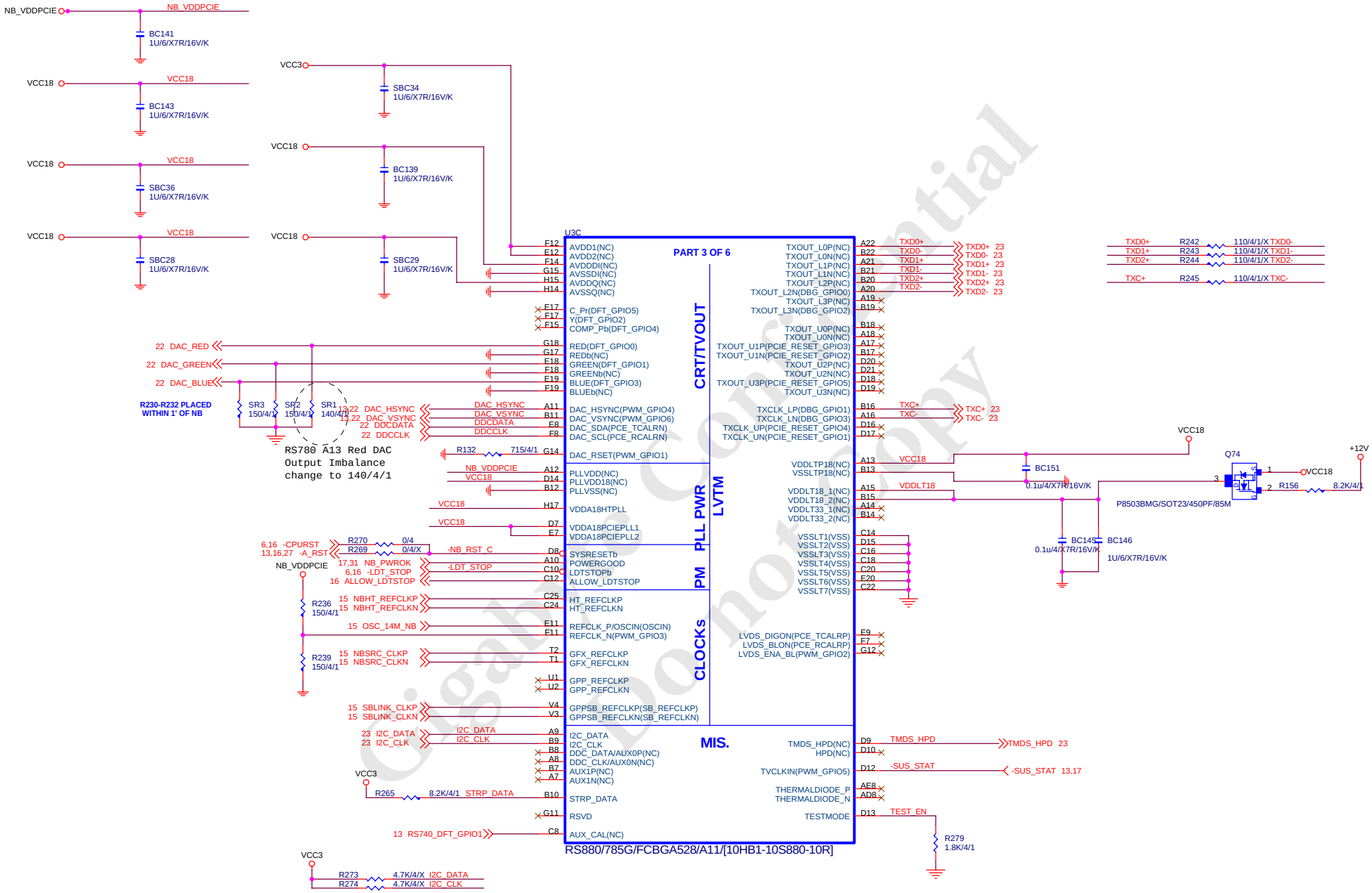
HT Link Stitching Caps

GIGABYTE

Title: RS880 HT-LINK I/F		
Size: B	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 10 of 35	

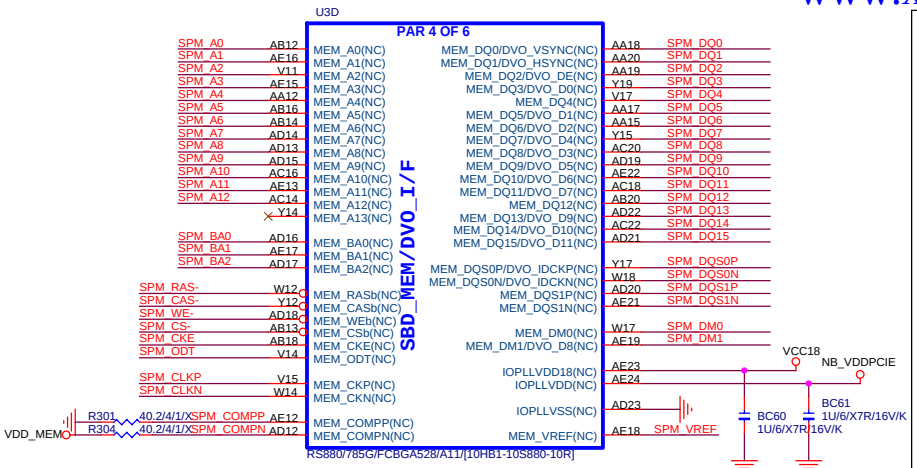
GIGABYTE

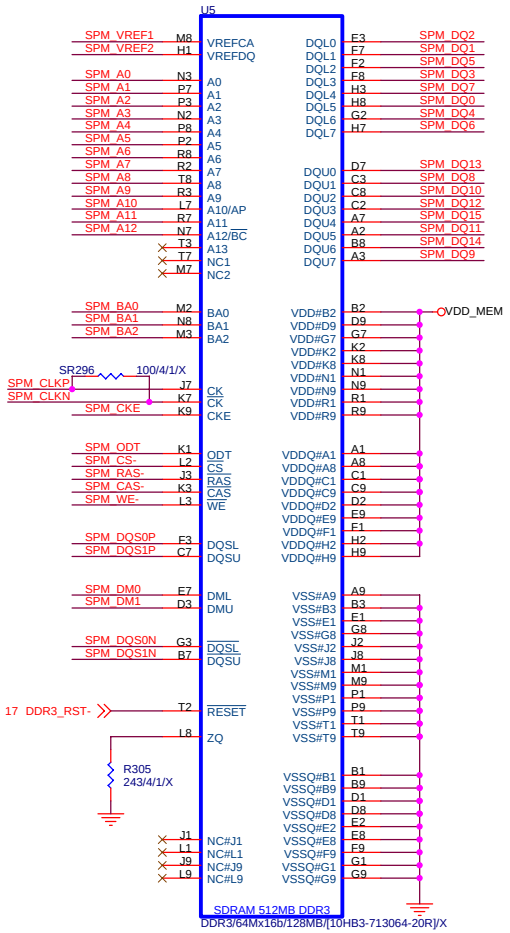
Title: RS880 PCIE I/F		
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 11 of 35	

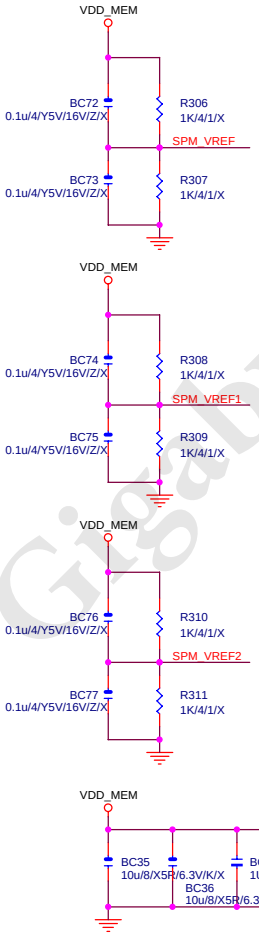


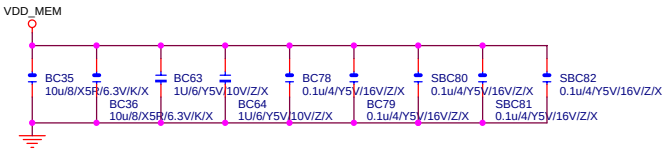
GIGABYTE

Title	RS880 SYSTEM I/F	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 12 of 35	



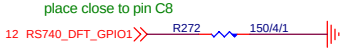






RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8



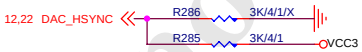
Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)



Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable  (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```
These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)   default
110: 4-0-0-0-0   Config A
101: 4-4-0-0-0   Config B
100: 4-2-2-0-0   Config C
011: 4-2-1-1-0   Config D
010: 4-1-1-1-1   Config E
others: register defined (default to Config E)
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1   Mode L   default
110: 1-1-1-1-1-1   Mode L
101: 2-0-2-0-2-0   Mode C2
100: 2-0-2-0-1-1   Mode K
011: 2-0-1-1-1-1   Mode E
010: 1-1-1-1-1-1   Mode L
001: 4-0-0-0-1-1   Mode C
000: 4-0-0-0-2-0   Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

```
1-1-1-1-1-1   Mode L   default
1-1-1-1-1-1   Mode L
2-0-2-0-2-0   Mode C2
2-0-2-0-1-1   Mode K
2-0-1-1-1-1   Mode E
1-1-1-1-1-1   Mode L
4-0-0-0-1-1   Mode C
4-0-0-0-2-0   Mode B
```

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740:  pin DFT_GPIO0
RS780:  pin HSYNC
RX780:  Not Appicable
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
     thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
            setting only
RS740: Not supported
```


GIGABYTE

Title: RS880 STRAP		
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 13 of 35	

RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U3F — PART 6/6 — GROUND

RS880/785G/FCBGA528/A11/[10HB1-10S880-10R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E — PART 5/6 — POWER

RS880/785G/FCBGA528/A11/[10HB1-10S880-10R]

NB_VCC, NB_VDDPCIE, VCC_SB, VCC18, VDD_MEM, VCC3

GIGABYTE

Title: RS880 POWER & GND

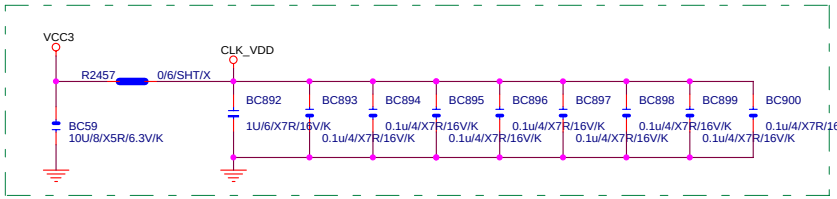
Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

Date: Monday, April 19, 2010 | Sheet 14 of 35

NB CLOCK INPUT TABLE

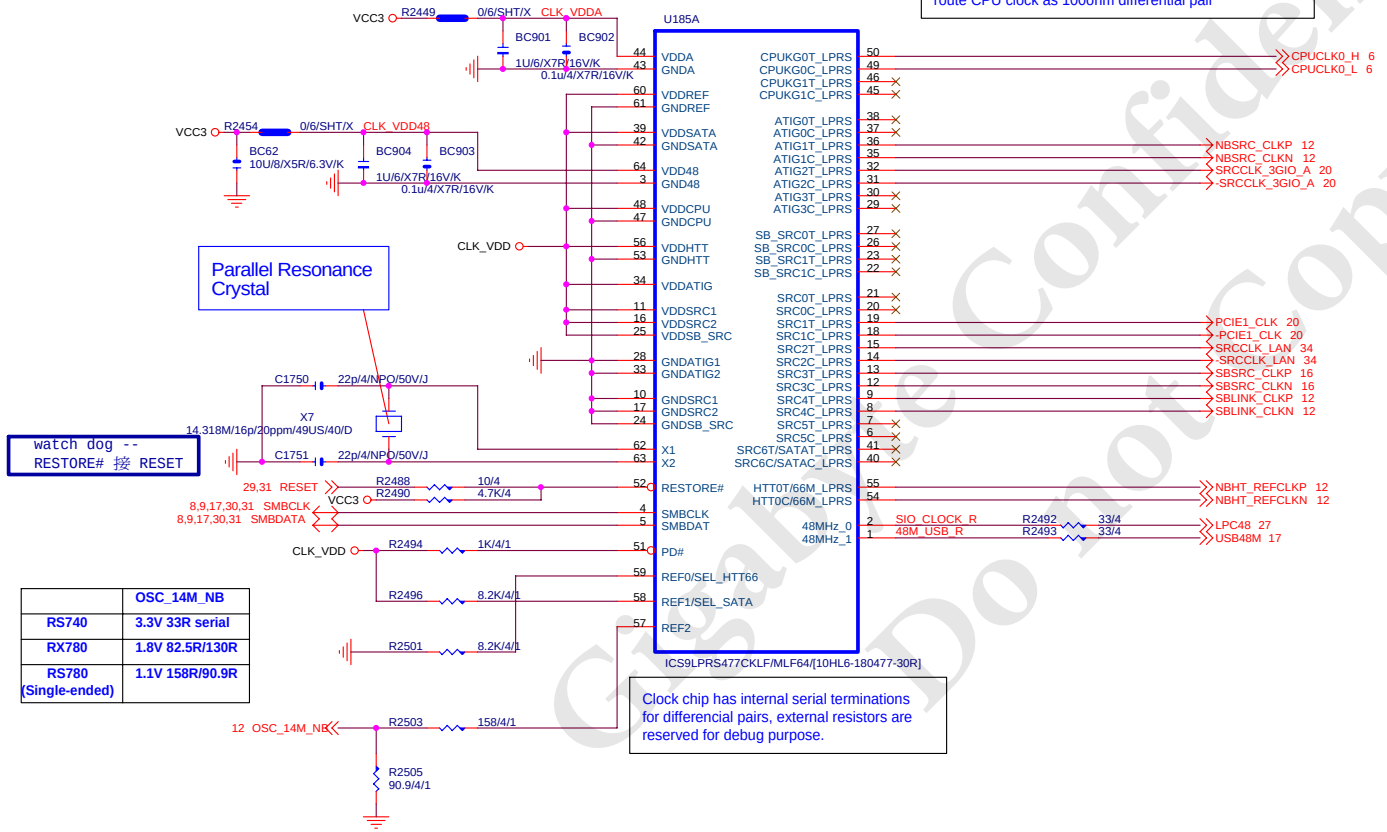
NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



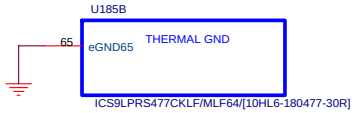
1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R



REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE

Title: ICS9LPRS477

Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

Date: Monday, April 19, 2010 | Sheet 15 of 35

PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030030-51R_12SP2-030030-52R_12SP2-030030-53R]

U2A

SB700

Part 1 of 5

A_RST#

PCIE_TX0P PCIE_TX0N PCIE_TX1P PCIE_TX1N PCIE_TX2P PCIE_TX2N PCIE_TX3P PCIE_TX3N

PCIE_RX0P PCIE_RX0N PCIE_RX1P PCIE_RX1N PCIE_RX2P PCIE_RX2N PCIE_RX3P PCIE_RX3N

PCIE_CALRP PCIE_CALRN

PCIE_PVDD PCIE_PVSS

PCIE_RCLKP/NB_LNK_CLKP PCIE_RCLKN/NB_LNK_CLKN

NB_DISP_CLKP NB_DISP_CLKN NB_HT_CLKP NB_HT_CLKN CPU_HT_CLKP CPU_HT_CLKN SLT_GFX_CLKP SLT_GFX_CLKN GPP_CLK0P GPP_CLK0N GPP_CLK1P GPP_CLK1N GPP_CLK2P GPP_CLK2N GPP_CLK3P GPP_CLK3N 25M_48M_66M_OSC 25M_X1 25M_X2

RTC_XI RTC_XO

ALLOW_LDTSTP PROCHOT# LDT_PG LDT_STP# LDT_RST#

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

RTC XTAL

LPC

CPU

RTC

SB710/FCBGA528/A14/[10HB1-06B710-11R]

PCICLK0 PCICLK1 PCICLK2 PCICLK3 PCICLK4 PCICLK5/GPIO41

PCIRST#

AD[0..31] 21,35

C_BE0 C_BE1 C_BE2 C_BE3 FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR#

REQ0# REQ1# REQ2# REQ3#/GPIO70 REQ4#/GPIO71

GNT0# GNT1# GNT2# GNT3#/GPIO72 GNT4#/GPIO73 CLKRUN# LOCK#

INTA# INTB# INTC# INTD#

INTE#/GPIO33 INTF#/GPIO34 INTG#/GPIO35 INTH#/GPIO36

LPCCLK0 LPCCLK1 LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#/GNT5#/GPIO68 BMREQ#/REQ5#/GPIO65 SERIRQ

RTCCLK INTRUDER_ALERT# VBAT

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

X4 32.768K/12.5p/20ppm/TF38/35K/D

SHW/D0.64*5.08*6.74

PCLK2 PCLK3 PCLK4

LPC33 27 PCICLK1 21 PCICLK2 21 1394CLK 35

PCLK2 PCLK3

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

LPC_CLK0 LPC_CLK1 Rev.A12

	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

BIOS after boot setting
EC AOD-ACC

20mil 20mil 20mil

BAT54C/SOT23/200mA BC783 0.1u/6X7R/25V/K BC22 1U/6/X7R/16V/K

BAT-SK/BK/P/S/D/SN CR2032 BAT

PH/1*2/BK/2.54/VA/D

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

-PCI_CLKRUN R172 8.2K/4/X

RTC_CLK R171 8.2K/4/1

GIGABYTE

Title: ATI SB710 PCIE/PCI/CPU/LPC

Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

Date: Monday, April 19, 2010 | Sheet 16 of 35

USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals can be used for power-up sequencer

IMC_GPIO17 IMC_GPIO16

ROM TYPE:

H, H = Reserved

H, L = SPI ROM DEFAULT

L, H = LPC ROM

L, L = FWH ROM

AZ_RST# Rev.A12

PULL HIGH	ENABLE PCI MEM BOOT
PULL LOW	DISABLE PCI MEM BOOT DEFAULT

SB700 Part 4 of 5

SB710/FCBGA528/A14/[10HB1-06B710-11R]

AOD Extreme

Title	ATI SB710 ACPI/USB/GPIO/AUDIO
Size	Custom
Document Number	GA-MA785GMT-UD2H
Rev	3.3
Date:	Monday, April 19, 2010
Sheet	17 of 35

SATA2_0_1 — SATA2/7/YL/H/P/VA/D/2/B/GBT

SATA2_2_3 — SATA2/7/YL/H/P/VA/D/2/B/GBT

SP_TX0P_C C1310 0.01U/4/X7R/25V/K
SP_TX0M_C C1309 0.01U/4/X7R/25V/K
SP_RX0M_C C1308 0.01U/4/X7R/25V/K
SP_RX0P_C C1302 0.01U/4/X7R/25V/K
SP_TX2P_C C1279 0.01U/4/X7R/25V/K
SP_TX2M_C C1278 0.01U/4/X7R/25V/K
SP_RX2M_C C1282 0.01U/4/X7R/25V/K
SP_RX2P_C C1283 0.01U/4/X7R/25V/K

C1307 0.01U/4/X7R/25V/K SP_RX1P_C
C1311 0.01U/4/X7R/25V/K SP_RX1M_C
C1300 0.01U/4/X7R/25V/K SP_TX1M_C
C1286 0.01U/4/X7R/25V/K SP_TX1P_C
C1284 0.01U/4/X7R/25V/K SP_RX3P_C
C1285 0.01U/4/X7R/25V/K SP_RX3M_C
C1281 0.01U/4/X7R/25V/K SP_TX3M_C
C1280 0.01U/4/X7R/25V/K SP_TX3P_C

PLACE SATA AC COUPLING CAPS CLOSE TO SB600

SATA2_4 — SATA2/7/810C/H/OP/VA/D/1/B

SP_TX4P_C C97 0.01U/4/X7R/25V/K
SP_TX4M_C C89 0.01U/4/X7R/25V/K
SP_RX4M_C C96 0.01U/4/X7R/25V/K
SP_RX4P_C C98 0.01U/4/X7R/25V/K

35 SATA5RXPC SATA5RXPC 0.01U/4/X7R/25V/K C165 SP_RX5P_C
35 SATA5RXNC SATA5RXNC 0.01U/4/X7R/25V/K C166 SP_RX5M_C
35 SATA5TXNC SATA5TXNC 0.01U/4/X7R/25V/K C169 SP_TX5M_C
35 SATA5TXPC SATA5TXPC 0.01U/4/X7R/25V/K C177 SP_TX5P_C

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

U2B

SB700
Part 2 of 5

SP_TX0P_C AD9 SATA_TX0P
SP_TX0M_C AE9 SATA_TX0N
SP_RX0M_C AB10 SATA_RX0N
SP_RX0P_C AC10 SATA_RX0P
SP_TX1P_C AE10 SATA_TX1P
SP_TX1M_C AD10 SATA_TX1N
SP_RX1M_C AD11 SATA_RX1N
SP_RX1P_C AE11 SATA_RX1P
SP_TX2P_C AB12 SATA_TX2P
SP_TX2M_C AC12 SATA_TX2N
SP_RX2M_C AE12 SATA_RX2N
SP_RX2P_C AD12 SATA_RX2P
SP_TX3P_C AD13 SATA_TX3P
SP_TX3M_C AE13 SATA_TX3N
SP_RX3M_C AB14 SATA_RX3N
SP_RX3P_C AC14 SATA_RX3P
SP_TX4P_C AE14 SATA_TX4P
SP_TX4M_C AD14 SATA_TX4N
SP_RX4M_C AD15 SATA_RX4N
SP_RX4P_C AE15 SATA_RX4P
SP_TX5P_C AB16 SATA_TX5P
SP_TX5M_C AC16 SATA_TX5N
SP_RX5M_C AE16 SATA_RX5N
SP_RX5P_C AD16 SATA_RX5P

R2194 1K/4/1 SATA_CAL V12 SATA_CAL
SATA_X1 Y12 SATA_X1
SATA_X2 AA12 SATA_X2
29 -SATA_LED -SATA_LED W11 SATA_ACT#/GPIO67
VCC_SB AA11 PLLVDD_SATA
VCC3 W12 XTLVDD_SATA

SERIAL ATA
SATA PWR

IDE_IORDY AA24 PIORDY — PIORDY 23
IDE_IRQ AA25 IRQ14 — IRQ14 23
IDE_A0 Y22 PDA0 — PDA0 23
IDE_A1 AB23 PDA1 — PDA1 23
IDE_A2 Y23 PDA2 — PDA2 23
IDE_DACK# AB24 -PDDACK — -PDDACK 23
IDE_DRQ AD25 PDDREQ — PDDREQ 23
IDE_IOR# AC25 -PDIOR — -PDIOR 23
IDE_IOW# AC24 -PDIOW — -PDIOW 23
IDE_CS1# Y25 -PCS1 — -PCS1 23
IDE_CS3# Y24 -PCS3 — -PCS3 23

IDE_D0/GPIO15 AD24 PDD0
IDE_D1/GPIO16 AD23 PDD1
IDE_D2/GPIO17 AE22 PDD2
IDE_D3/GPIO18 AC22 PDD3
IDE_D4/GPIO19 AD21 PDD4
IDE_D5/GPIO20 AE20 PDD5
IDE_D6/GPIO21 AB20 PDD6
IDE_D7/GPIO22 AD19 PDD7
IDE_D8/GPIO23 AE19 PDD8
IDE_D9/GPIO24 AC20 PDD9
IDE_D10/GPIO25 AD20 PDD10
IDE_D11/GPIO26 AE21 PDD11
IDE_D12/GPIO27 AB22 PDD12
IDE_D13/GPIO28 AD22 PDD13
IDE_D14/GPIO29 AE23 PDD14
IDE_D15/GPIO30 AC23 PDD15

PDD[0..15] — PDD[0..15] 23

ATA 66/100/133

SPI_DI/GPIO12 G6 SB_SPI_DI_R R97 22/4 SB_SPI_DI
SPI_DO/GPIO11 D2 SB_SPI_DO_R R100 22/4 SB_SPI_DO
SPI_CLK/GPIO47 D1 SB_SPI_CLK_R R92 22/4 SB_SPI_CLK
SPI_HOLD#/GPIO31 E4
SPI_CS1#/GPIO32 E3 SB_SPI_CS R94 22/4 -SB_SPI_CS_ITE — SB_SPI_CS_ITE 27
LAN_RST#/GPIO13 U15
ROM_RST#/GPIO14 J1

SPI ROM

FANOUT0/GPIO3 M8
FANOUT1/GPIO48 M5
FANOUT2/GPIO49 M7
FANIN0/GPIO50 P5
FANIN1/GPIO51 P8
FANIN2/GPIO52 R8

TEMP_COMM C6
TEMPIN0/GPIO61 B6 — VDD_MEM_OV2 33
TEMPIN1/GPIO62 A6 — VCC_SB_OV2 32
TEMPIN2/GPIO63 A5 — VCC_SB_OV1 32
TEMPIN3/TALERT#/GPIO64 B5

VIN0/GPIO53 A4 — HDMI_DVI_BIOS 23
VIN1/GPIO54 B4 — VDD_MEM_OV1 33
VIN2/GPIO55 C4 — NB_VCC_OV2 32
VIN3/GPIO56 D4 — NB_VCC_OV1 32
VIN4/GPIO57 D5 — DDR18V_OV4 33
VIN5/GPIO58 D6 — DDR18V_OV3 33
VIN6/GPIO59 A7 — DDR18V_OV2 33
VIN7/GPIO60 B7 — DDR18V_OV1 33

HW MONITOR

AVDD F6 — 3VDUAL
AVSS G7

BC119 0.1u/4/X7R/16V/K
BC117 1U/6/X7R/16V/K

SB710/FCBGA528/A14/[10HB1-06B710-11R]

M_BIOS
1 -ITE_SPI_CS
2 SB_SPI_DI
3 -BIOS_WP
4 VSS
CS# VDD 8 — VCC3 — BC203 0.1u/4/X7R/16V/K
SO HOLD# 7 -SPI_HOLD0
WP# SCK 6 SB_SPI_CLK
SI 5 SB_SPI_DO
8M/SPI/SO8/200mil/S
MAIN BIOS

27 -ITE_SPI_CS

B_BIOS
1 -ITE_SPI_CS1
2 SB_SPI_DI
3 -BIOS_WP
4 VSS
CS# VDD 8 — VCC3
SO HOLD# 7 -SPI_HOLD0
WP# SCK 6 SB_SPI_CLK
SI 5 SB_SPI_DO
8M/SPI/SO8/200mil/S
BACKUP BIOS

27 -ITE_SPI_CS1

SATA_X2 — R168 10M/4 — SATA_X1
X6 1 2 25M/20p/30ppm/49US/20/D
C115 10P/4/NPO/50V/J
C119 10P/4/NPO/50V/J

VCC_SB — BC124 1U/6/X7R/16V/K — BC123 0.1u/4/X7R/16V/K
VCC3 — BC112 1U/6/X7R/16V/K — BC110 0.1u/4/X7R/16V/K

VCC3
-SPI_HOLD0 R29 1K/4/1
SB_SPI_DO R34 1K/4/X
-BIOS_WP R38 1K/4/1
SB_SPI_DI R39 1K/4/X
-ITE_SPI_CS R28 1K/4/1
-ITE_SPI_CS1 R33 1K/4/1

GIGABYTE

Title	ATI SB710 SATA/IDE/HWM/SPI	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 18 of 35	

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE

For SB700 A12

U2C

SB700 Part 3 of 5

POWER

1.8V: Flash module mode
3.3V: IDE mode

SB710/FCBGA528/A14/[10HB1-06B710-11R]

U2E

SB700 Part 5 of 5

GROUND

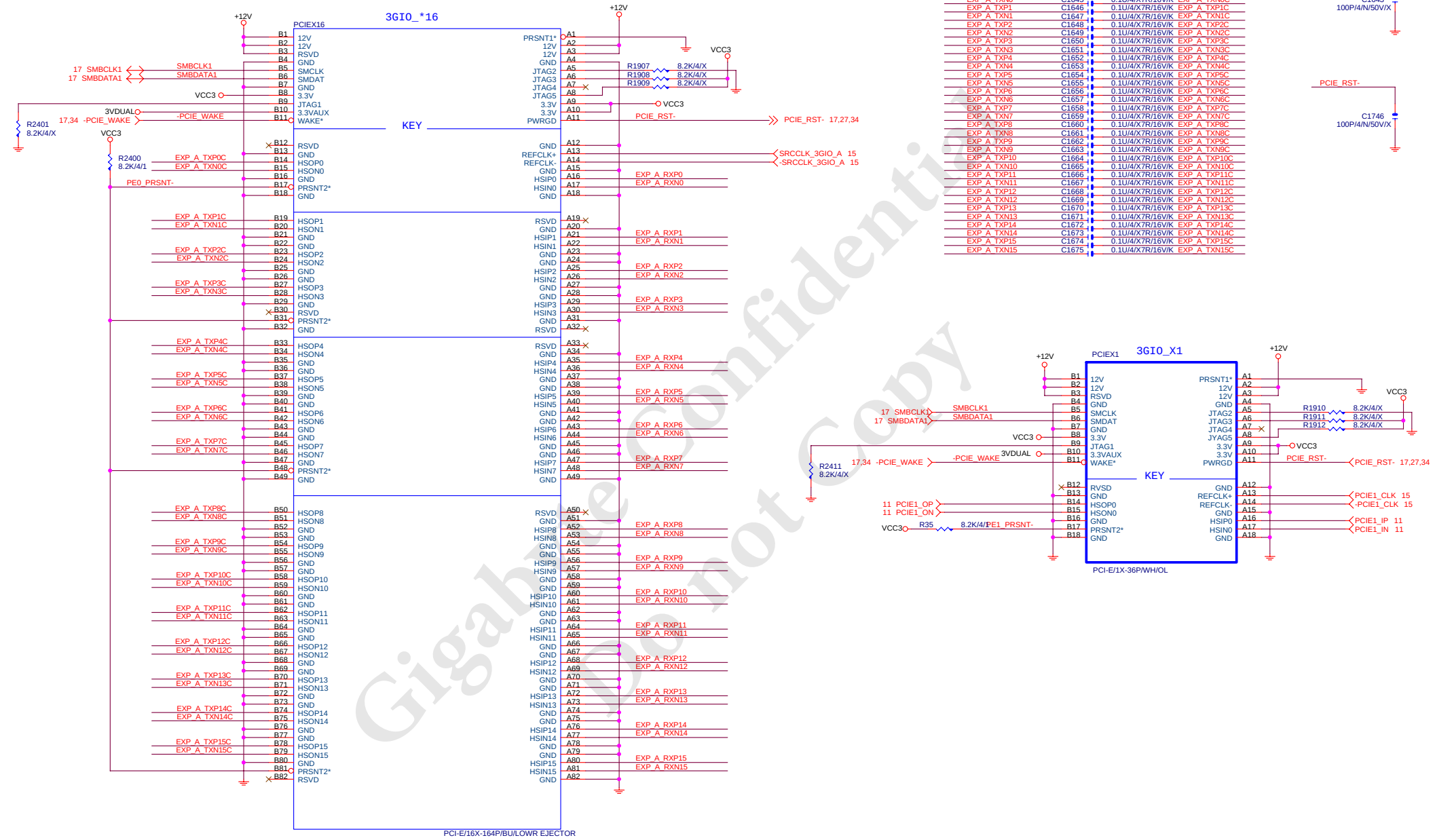
SB710/FCBGA528/A14/[10HB1-06B710-11R]

GIGABYTE

Title: ATI SB710 POWER & GND

Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

Date: Monday, April 19, 2010 | Sheet 19 of 35



GIGABYTE

Title: PCI EXPRESS X 16 ,X1

Size	Document Number	Rev
Custom	GA-MA785GMT-UD2H	3.3

Date: Monday, April 19, 2010 Sheet 20 of 35

PCI SLOT 1,2

PCI SLOT2

PCI2

PCI/120/P/IV/VA

IDSEL[AD22], GNT/REQ[0], INT[A]

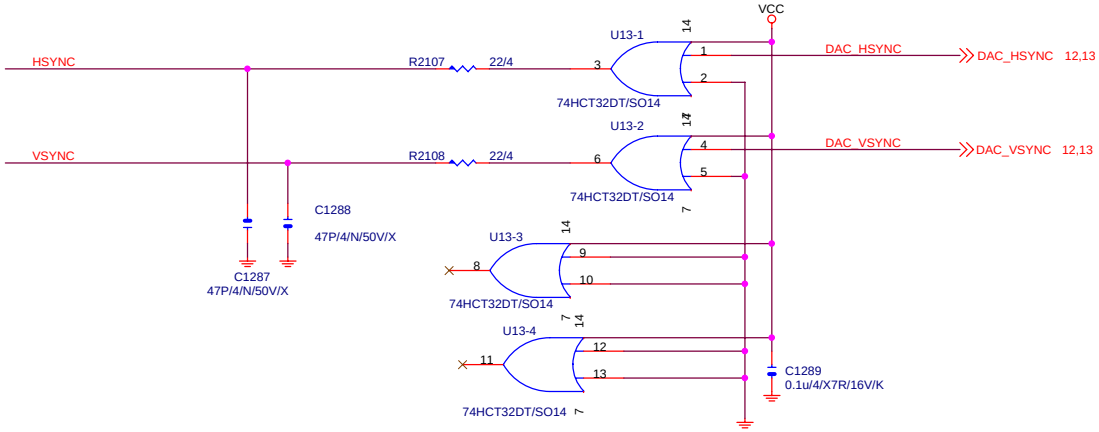
PCI SLOT1

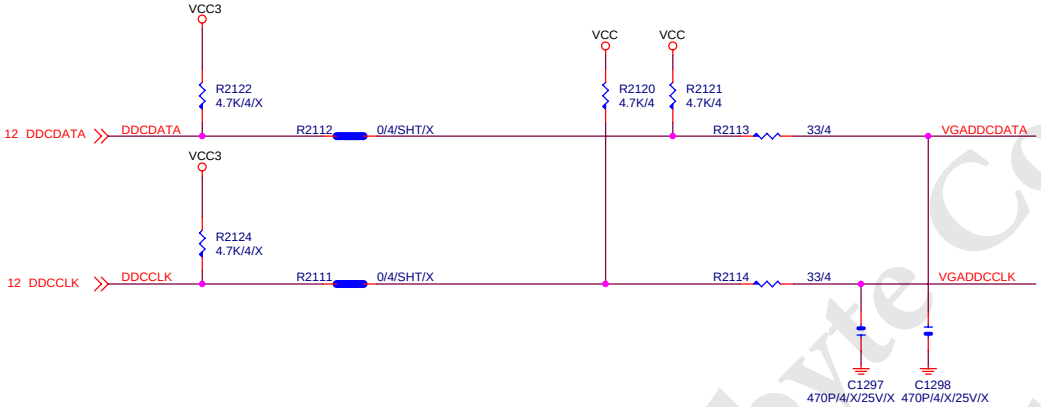
PCI1

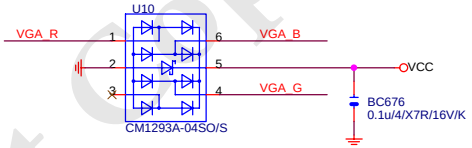
PCI/120/P/IV/VA

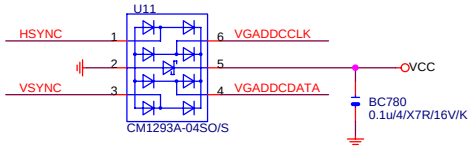
IDSEL[AD23], GNT/REQ[1], INT[B]

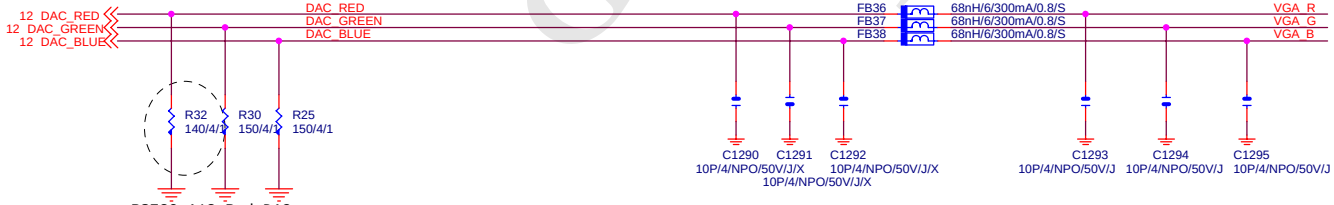
Title	PCI SLOT 1,2
Size	Custom
Document Number	GA-MA785GMT-UD2H
Rev	3.3
Date:	Monday, April 19, 2010
Sheet	21 of 35



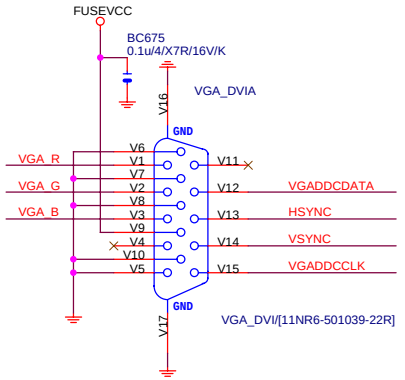








RS780 A13 Red DAC
Output Imbalance
change to 140/4/1



GIGABYTE

Title: RGB		
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 22 of 35	

CLOSE HDMI CONNECTOR

VCC3 D1 B140/SMA/1A VCC3SW

BC719 1U/6/X7R/16V/K BC299 0.1u/4/X7R/16V/K BC300 0.1u/4/X7R/16V/K BC301 0.1u/4/X7R/16V/K

U8 PI3HDMI412FT-B

VDD ×8 A0+ A0- A1+ A1- A2+ A2- A3+ A3-

SW_HDMI_TXD1+ SW_HDMI_TXD1- SW_HDMI_TXD2+ SW_HDMI_TXD2- SW_HDMI_TXD0+ SW_HDMI_TXD0- SW_HDMI_TXC+ SW_HDMI_TXC-

12 TXD1+ TXD1+ 12 TXD1- TXD1- 12 TXD2+ TXD2+ 12 TXD2- TXD2- 12 TXD0+ TXD0+ 12 TXD0- TXD0- 12 TXC+ TXC+ 12 TXC- TXC-

D0+ D0- D1+ D1- D2+ D2- D3+ D3-

B0+ B0- B1+ B1- B2+ B2- B3+ B3-

SW_DVI_TXD1+ SW_DVI_TXD1- SW_DVI_TXD2+ SW_DVI_TXD2- SW_DVI_TXD0+ SW_DVI_TXD0- SW_DVI_TXC+ SW_DVI_TXC-

SEL HDMI SW

VSS15 ×9 VSS15PAD

PI3HDMI412FT-BZHE/TQFN42/[10TA1-083412-10R]

VCC3 R321 1.8K/4/1 SW_SEL R322 150K/4 R323 8.2K/4/1 S0T23 HDMI_HPD Q82 MMBT2222A/SOT23/600mA/40 R325 1.5K/4/1

BC720 0.1u/4/X7R/16V/K BC302 0.1u/4/X7R/16V/K

SEL="0"-->A-->HDMI;
SEL="1"-->B-->DVI;(DEFAULT)

VCC3 C103 0.1u/4/X7R/16V/K Q13 G9131-15T73UF/SOT23/0.3A S0T23 VSS15 C75 1U/6/X7R/16V/K R3 120/6

FUSEVCC BC678 0.1u/4/X7R/16V/K

HDMI SHELL1 SHELL3 SHELL5 SHELL6 SHELL4 SHELL2

D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET

HDMI/19P/BK/S/RA/D

SW_HDMI_TXD2+ SW_HDMI_TXD2- SW_HDMI_TXD1+ SW_HDMI_TXD1- SW_HDMI_TXD0+ SW_HDMI_TXD0- SW_HDMI_TXC+ SW_HDMI_TXC-

HDMI_DDC_CLK HDMI_DDC_DATA HDMI_HPD R113 39.2K/4/1

VCC VCC R2127 4.7K/4 R2128 4.7K/4

12 I2C_CLK I2C_CLK R2119 0/4/SHT/X R281 0/4/SHT/X HDMI_DVI_BIOS 18

DVI_HPD R116 39.2K/4/1 Q67 BAT54C/SOT23/200mA S0T23

12 I2C_DATA I2C_DATA R2115 0/4/SHT/X

12 TMDS_HPD TMDS_HPD R312 33/4 R337 4.7K/4 D9 R331 100K/4/1

LM385-2.5/SOT23/[10DZ2-130385-21R]

U12 CM1293A-04SO/S/X HDMI_DDC_DATA HDMI_DDC_CLK VCC BC677 0.1U/4/Y5V/16V/Z/X

IDERST- R182 33/4 -RST1

VCC3 R183 4.7K/4 PIORDY

VCC3 R2195 8.2K/4/X R185 8.2K/4/1 IRQ14 R189 8.2K/4/1 PDD7 R191 5.6K/4 PDDREQ R192 470/4/1 IDEPU0 R194 15K/4/1 P66DET

PRIMARY IDE CONNECTOR

18 PDD[0..15] PDD[0..15] -IDERST R213 0/4/X

IDE

-RST1 PDD7 PDD6 PDD5 PDD4 PDD3 PDD2 PDD1 PDD0 PDD8 PDD9 PDD10 PDD11 PDD12 PDD13 PDD14 PDD15

18 PDDREQ PDDREQ 18 -PDIOW -PDIOW 18 -PDIOR -PDIOR PIORDY 18 PIORDY -PDDACK 18 -PDDACK IRQ14 18 IRQ14 PDA1 18 PDA1 PDA0 18 PDA0 -PCS1 18 -PCS1 -IDEACTP

IDEPU0 PDA2 -PCS3 P66DET P66DET 17

C111 0.047U/4/X7R/16V/K

BH/2*20K20/WH/SHN/2.54/VA/PA46

VCC RN3 1K/8P4R/4 R180 1K/4/1

FDD

DENSEL- 27 INDEX- 27 MOTEA- 27 DRVA- 27 DIR- 27 STEP- 27 WDATA- 27 WGATE- 27 TK00- 27 WPT- 27 RDATA- 27 SIDE1- 27 DSKCHG- 27

BH/2*17K5/WH/SHN/2.54/VA/PA46

VCC Q84 2N7002/SOT23/25pF/5 R224 1K/4/1 R327 8.2K/4/1 HDMI_HPD

VCC VCC R2129 4.7K/4 R2130 4.7K/4

Q55 2N7002/SOT23/25pF/5 HDMI_DDC_CLK DVI_DDC_CLK

Q56 2N7002/SOT23/25pF/5 HDMI_DDC_DATA DVI_DDC_DATA

VCC R196 1K/4/1 IDERST- R197 1K/4/1 Q7 MMBT2222A/SOT23/600mA/40 S0T23 Q6 MMBT2222A/SOT23/600mA/40 S0T23

D2 -IDEACTP -HDLED -HDLED 29 BAW56/SOT23/300mA S0T23 C112 180P/4/N/50V/X

Close to connector

17,27 -IDERST R200 8.2K/4/1 C109 1000P/4/X/50V/X

FUSEVCC SHIELD1 SHIELD3 VGA_DVIB SHIELD2 SHIELD4

SW_DVI_TXD0- SW_DVI_TXD0+ SW_DVI_TXD1- SW_DVI_TXD1+ SW_DVI_TXD2- SW_DVI_TXD2+ DVI_DDC_CLK DVI_DDC_DATA SW_DVI_TXC- SW_DVI_TXC+ DVI_HPD

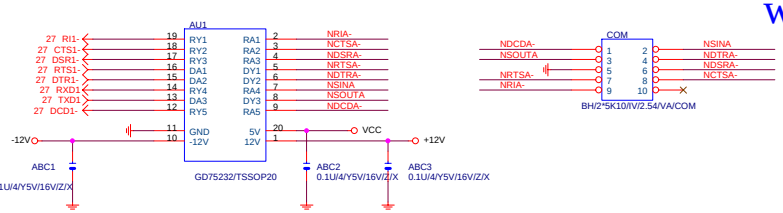
D17 TX0- D18 TX0+ D9 TX1- D10 TX1+ D1 TX2- D2 TX2+ D3 SHLD24 D11 SHLD13 D19 SHLD05 D12 TX3- D13 TX3+ D4 TX4- D5 TX4+ D20 TX5- D21 TX5+ D6 DDCC D7 DDCD D14 VDDC D15 GND D22 SHLDC D24 TXC- D23 TXC+ D8 VSYNC D16 HPD

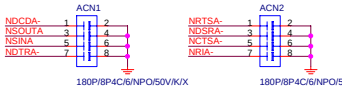
C1 R C2 G C3 B C5 AGND1 C6 AGND2 C4 HSYNC

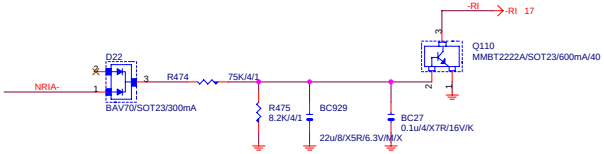
VGA_DVI/[11NR6-501039-22R]

GIGABYTE

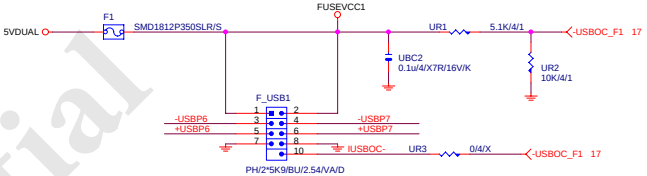
Title	IDE ,FDD ,HDMI ,DVI CONNECTOR	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 23 of 35	

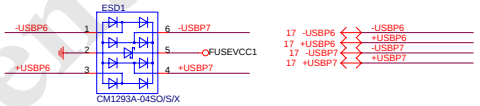


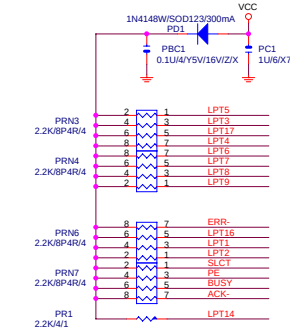




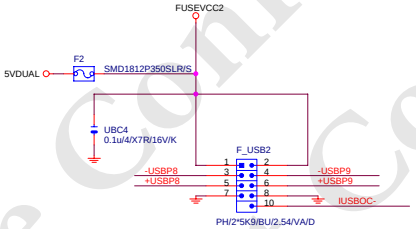
FRONT SIDE USB1



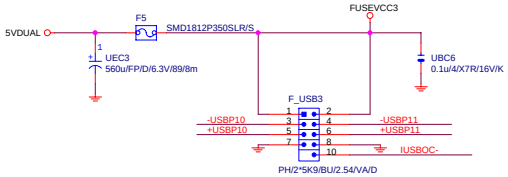


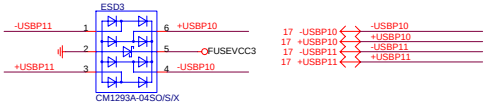


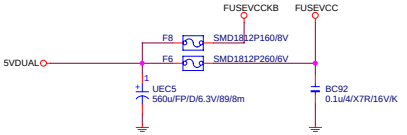
FRONT SIDE USB2

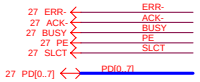


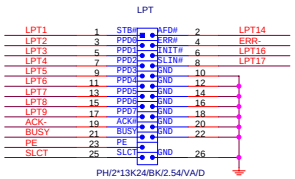
FRONT SIDE USB3









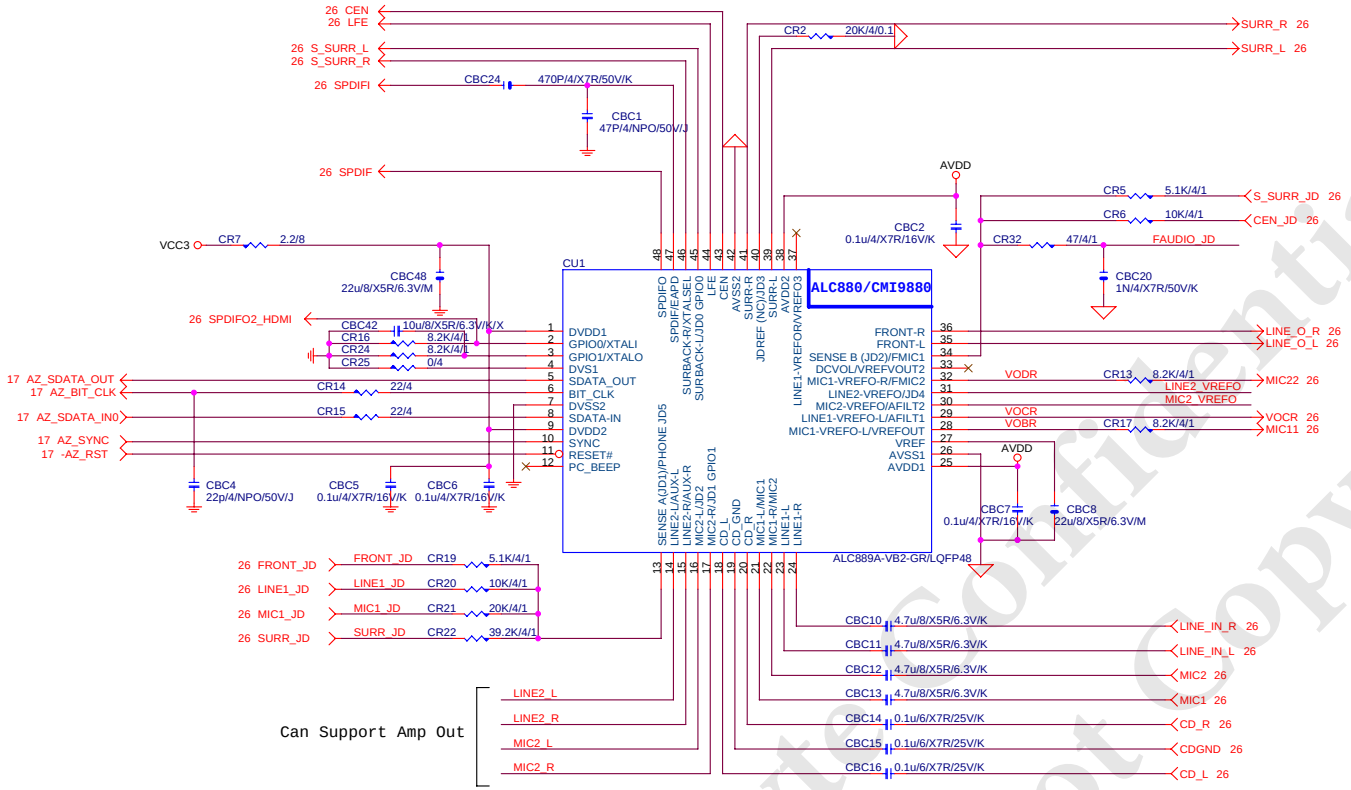


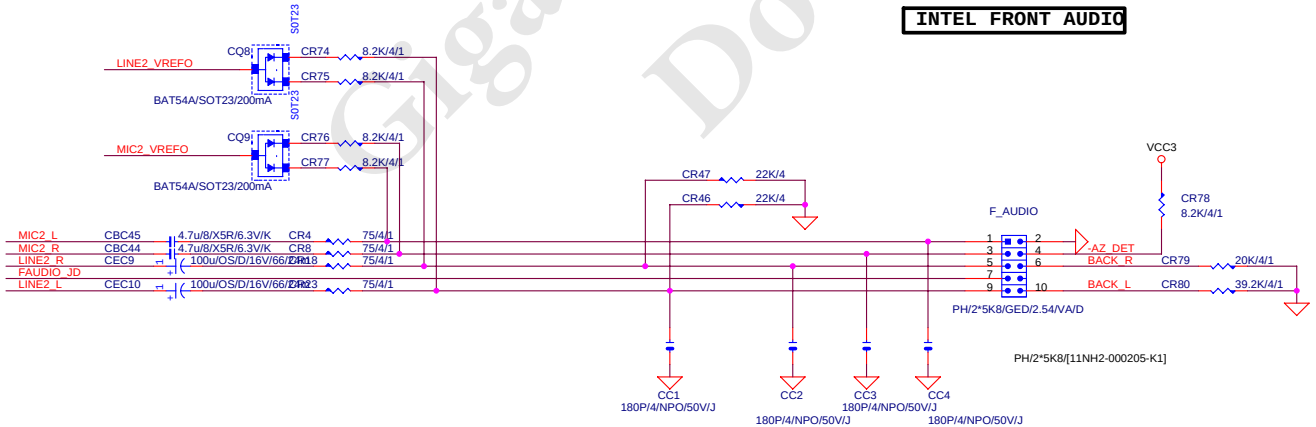
GIGABYTE

Title	COM/LPT/F_USB	
Size C	Document Number GA-MA785GMT-UD2H	Rev 3.3
Date: Monday, April 19, 2010	Sheet 24 of 35	

AZALIA CODEC *ALC892/ALC889A/ Colay*

	ALC892		ALC889A
CR16	X		0
CR24	X		0
CR25	X		0
CBC42	10uF/X5R		X
CR2	20K/1%		20K/0.1%
CR9	0		X
CR10	X		0
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R		4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR28/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm		75 ohm



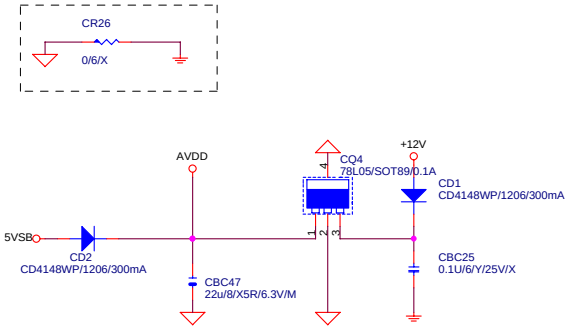


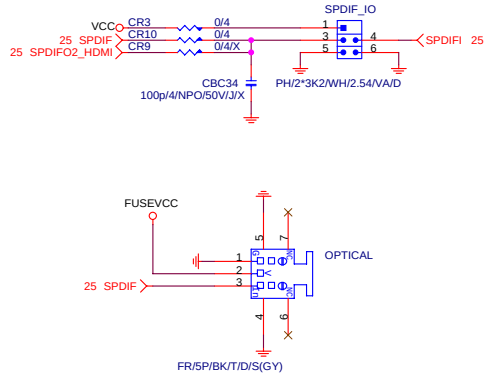
GIGABYTE

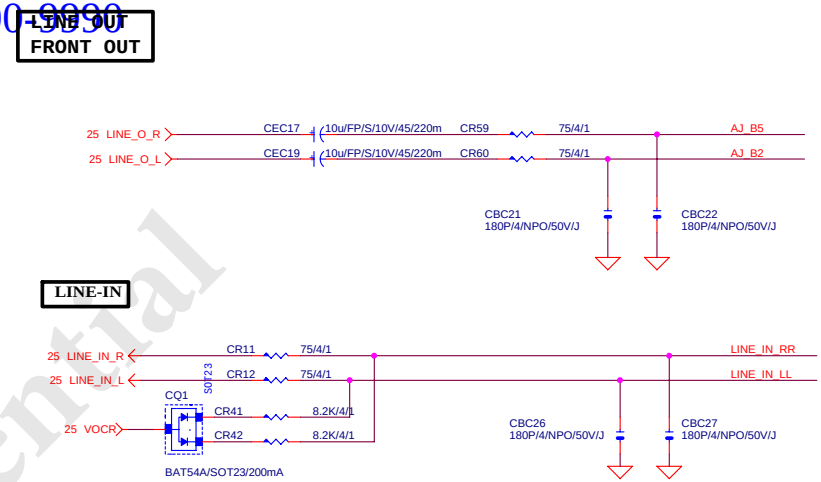
Title: ALC889A CODEC

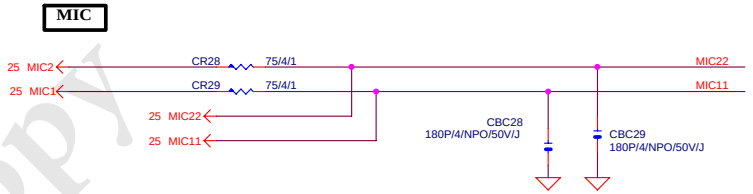
Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

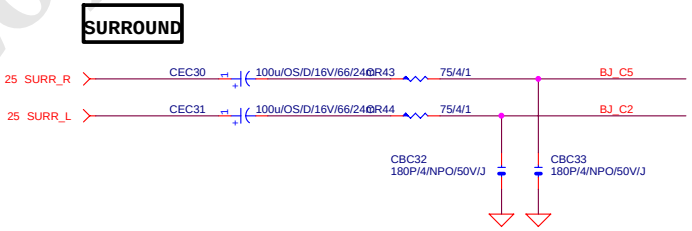
Date: Monday, April 19, 2010 | Sheet 25 of 35

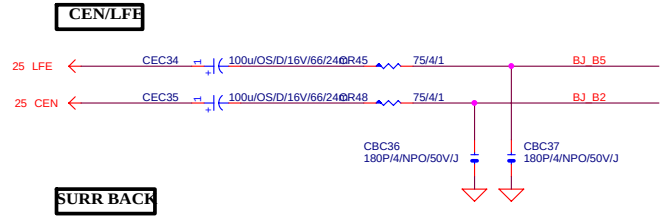


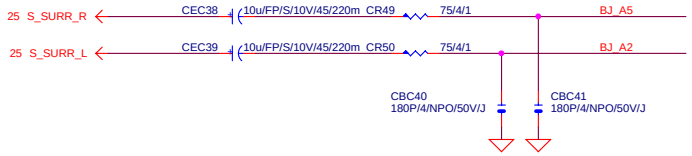


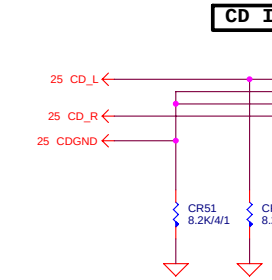


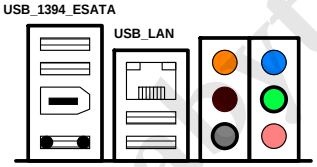


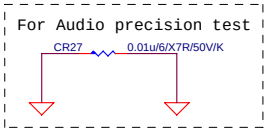


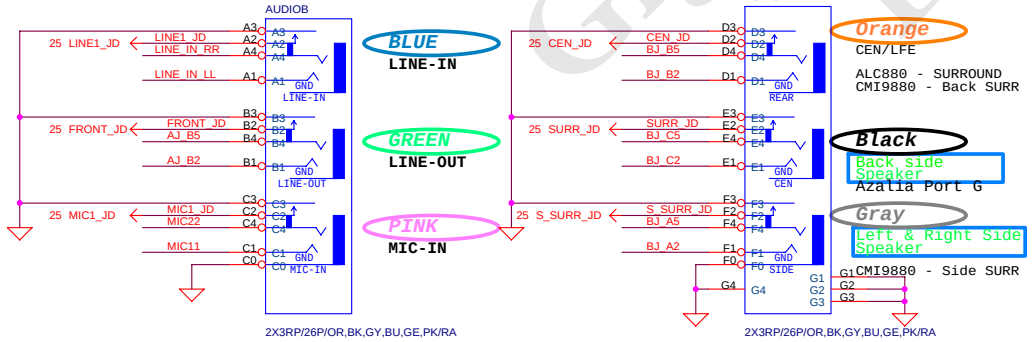










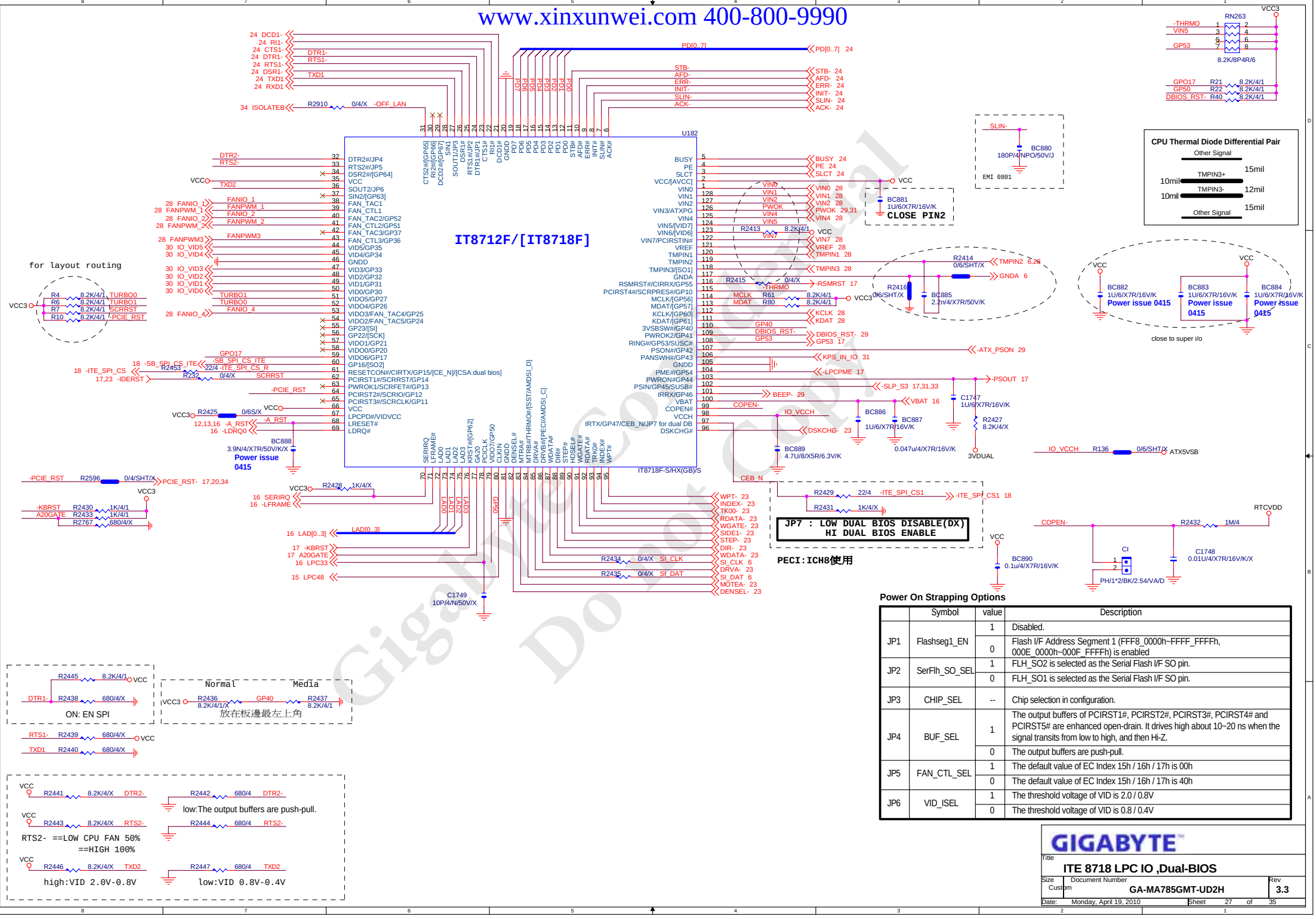


GIGABYTE

Title: AUDIO JACK

Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

Date: Monday, April 19, 2010 | Sheet 26 of 35



Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

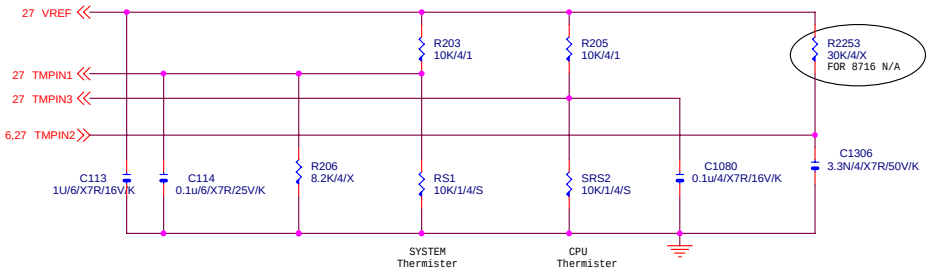
GIGABYTE

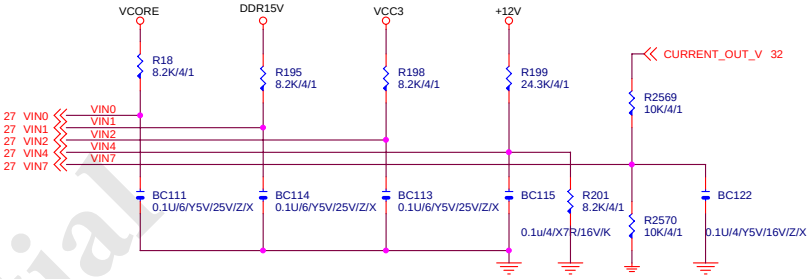
Title: ITE 8718 LPC IO ,Dual-BIOS

Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

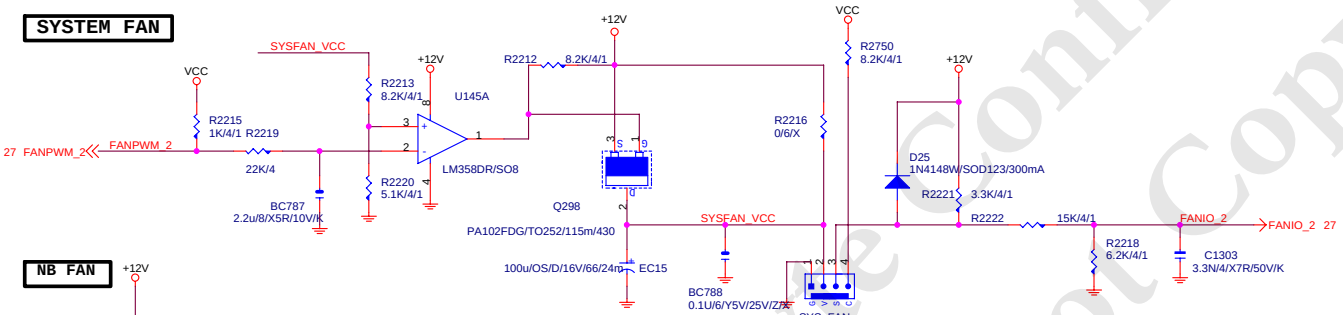
Date: Monday, April 19, 2010 | Sheet 27 of 35

Hardware Monitor circuits

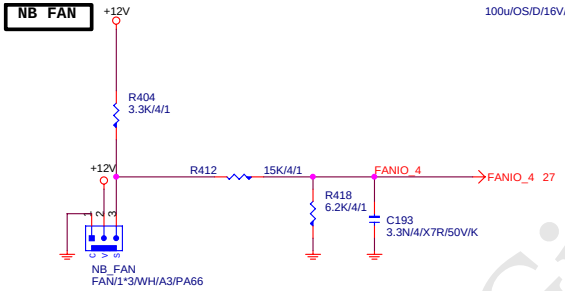




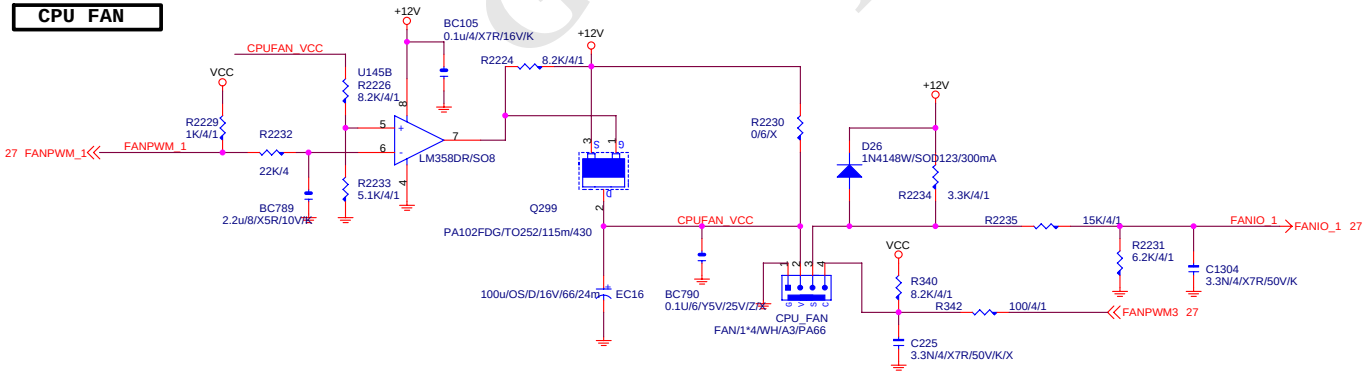
SYSTEM FAN



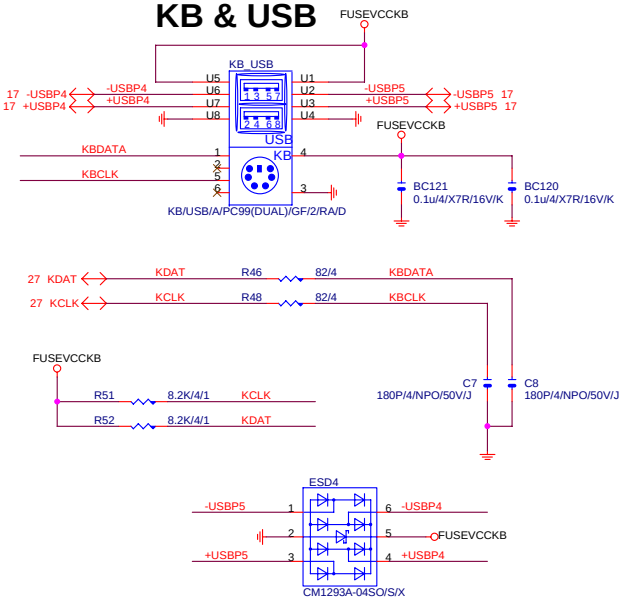
NB FAN



CPU FAN

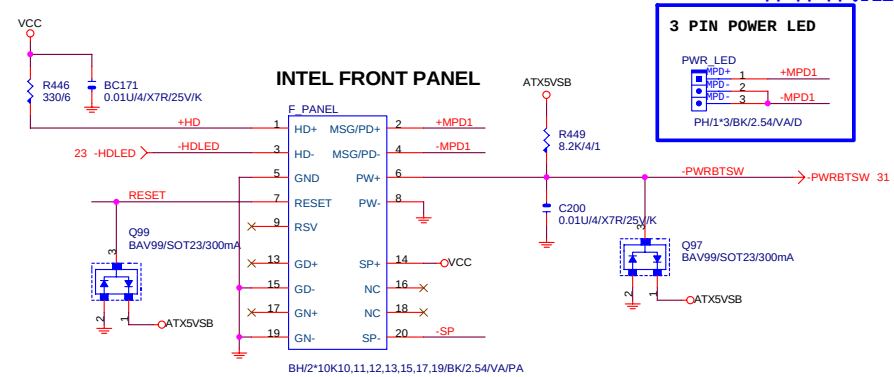


KB & USB

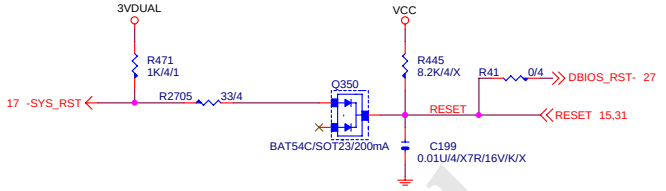


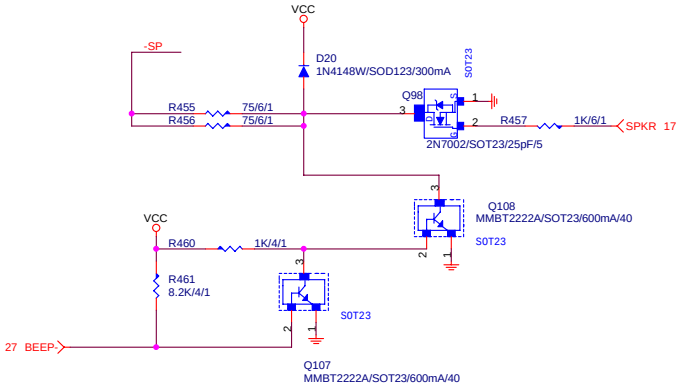
GIGABYTE			
Title: FAN/HWMO KB/USB			
Size: Custom	Document Number: GA-MA785GMT-UD2H		Rev: 3.3
Date: Monday, April 19, 2010		Sheet 28 of 35	

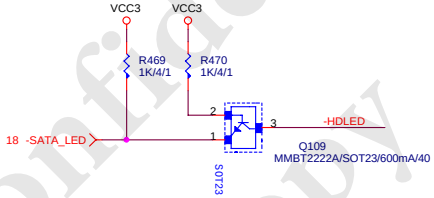
INTEL FRONT PANEL

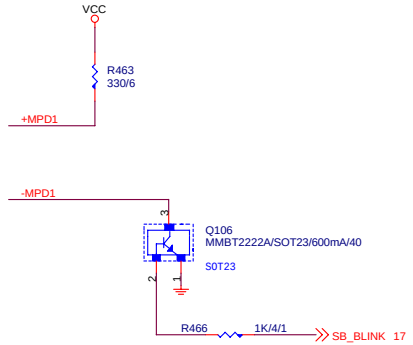


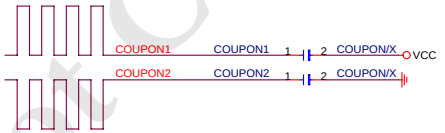
3 PIN POWER LED



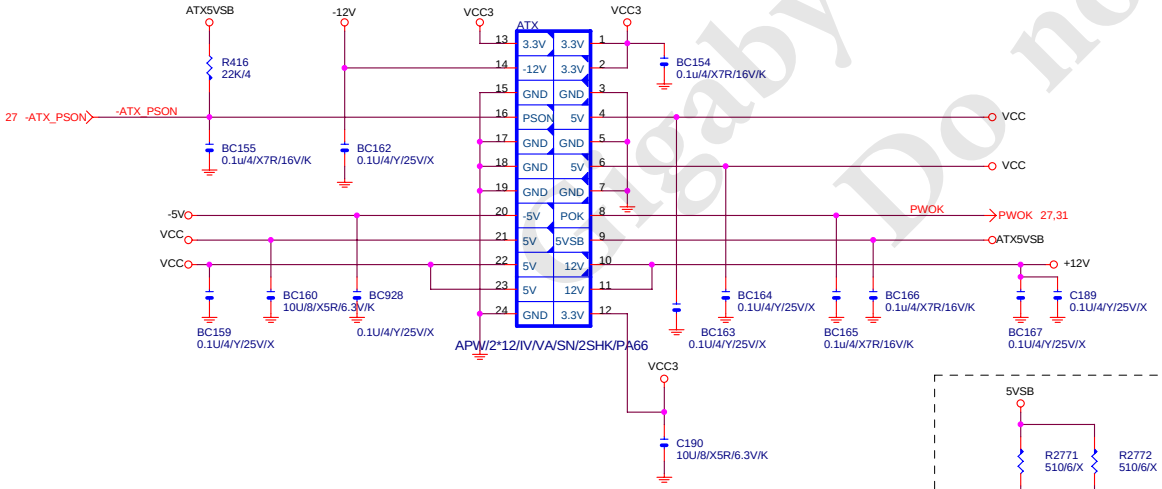


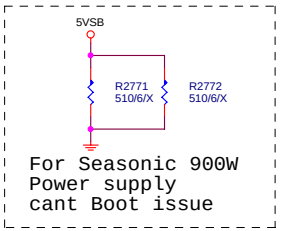


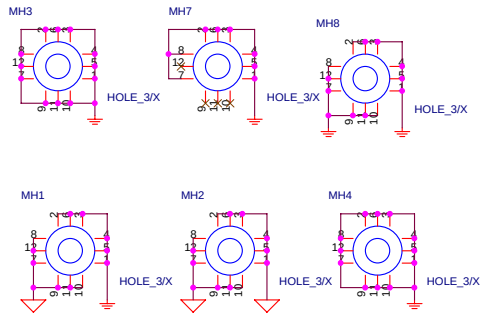


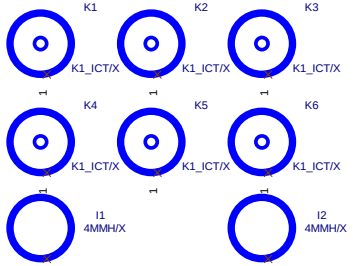


ATX POWER CONNECTOR









GIGABYTE

Title: ATX, FRONT PANEL		
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 29 of 35	

AM2: high, AM2R2: low

0.8V on

PWROK (SVI) — EN rising edge :
Low : "metal VID" — Hi : PVI mode
High : running protocol — Low : SVI mode
Pin 34 Input, Pin 37 Output

U1 ISL6324ACRAQFN48

for 6324

BOTTOM PAD CONNECT TO GND THROUGH 8 VIA

ISL6612ACBZ-T/SO8

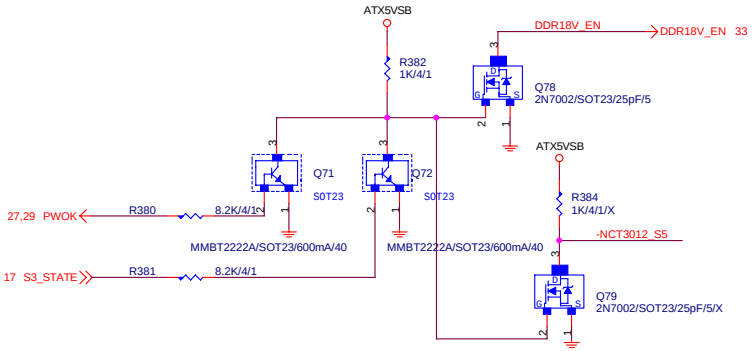
APW/2*4/IV/OC/P/4.2/VA/SN/OH

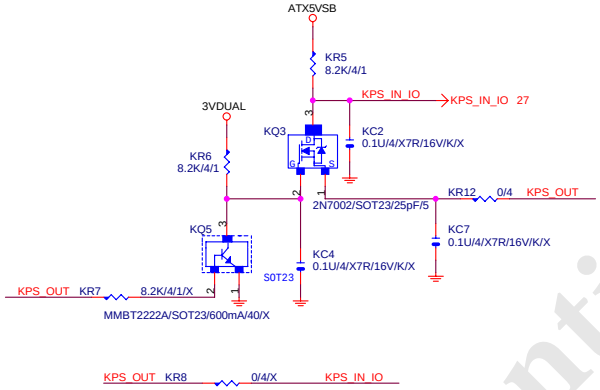
GIGABYTE

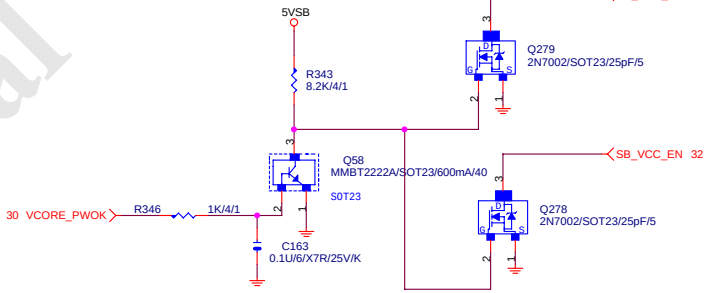
Title: VCORE (PWM ISL6324A+6612A)

Size: C | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

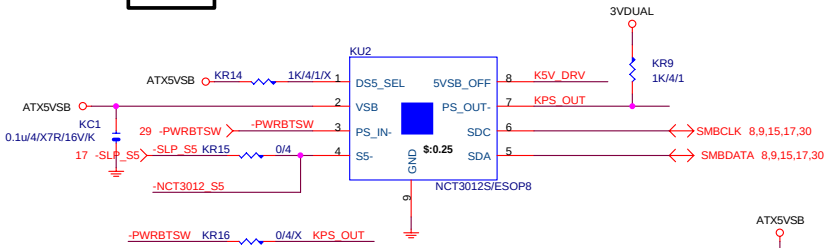
Date: Monday, April 19, 2010 | Sheet 30 of 35

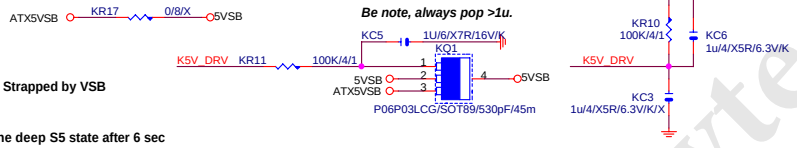


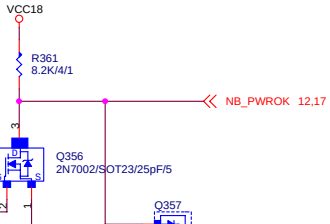




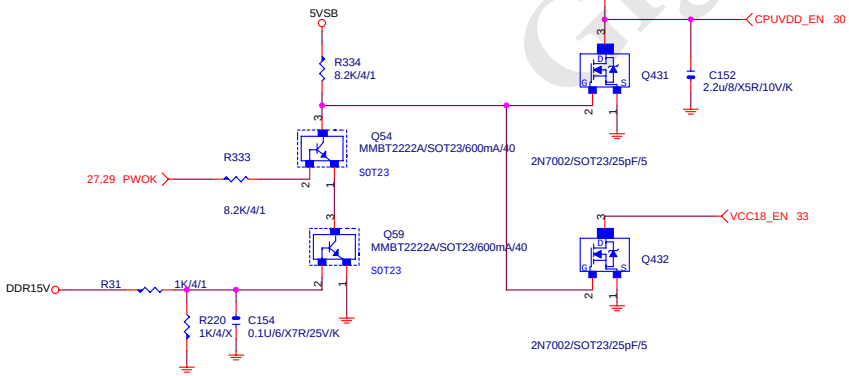
EUP



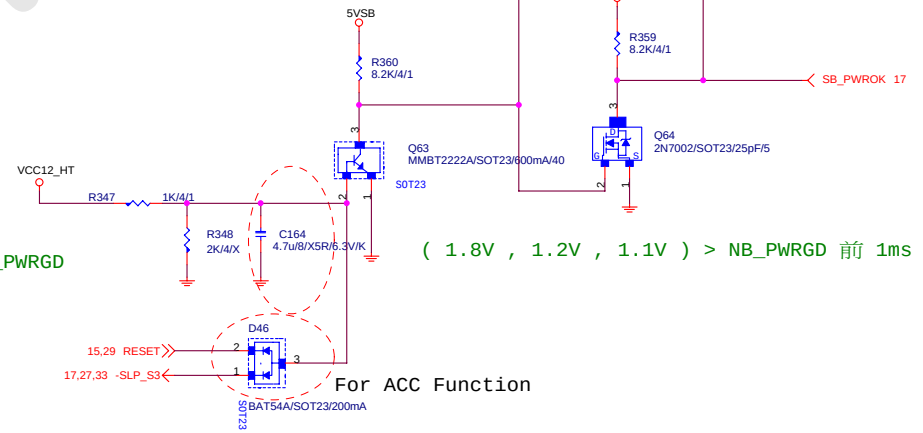




Function Selection. Strapped by VSB
Strapped to high :
DeepS5_Sel = 1:
System will enter the deep S5 state after 6 sec delays when AC power on.
Strapped to low : (Default)
DeepS5_Sel = 0:
System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.



PWOK > NB_PWRGD / SB_PWRGD

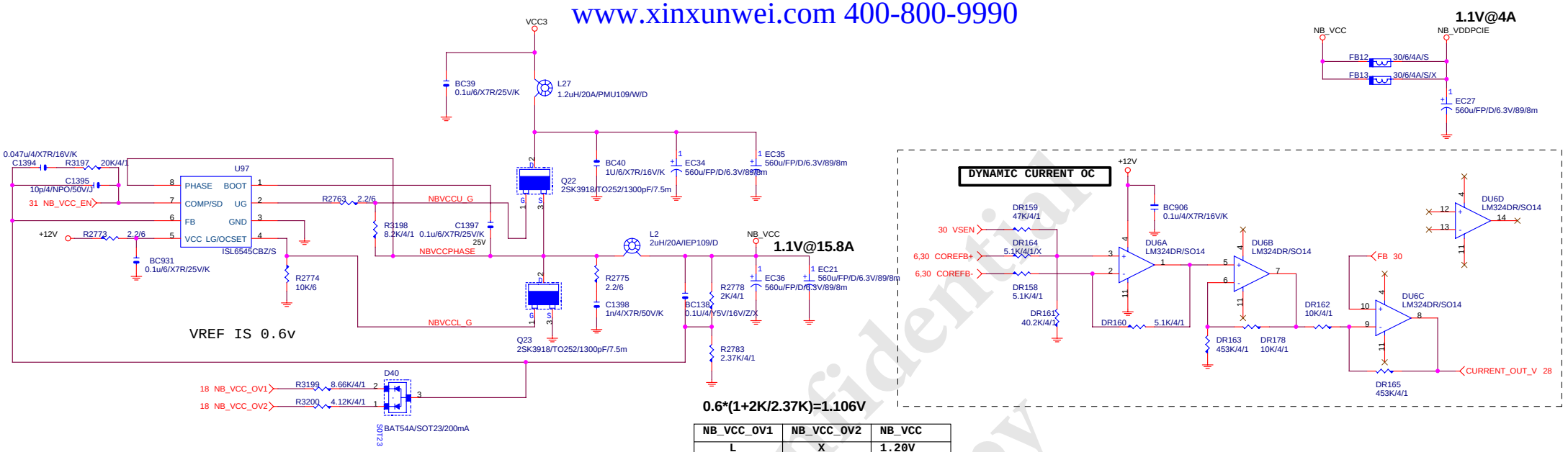


(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms

For ACC Function

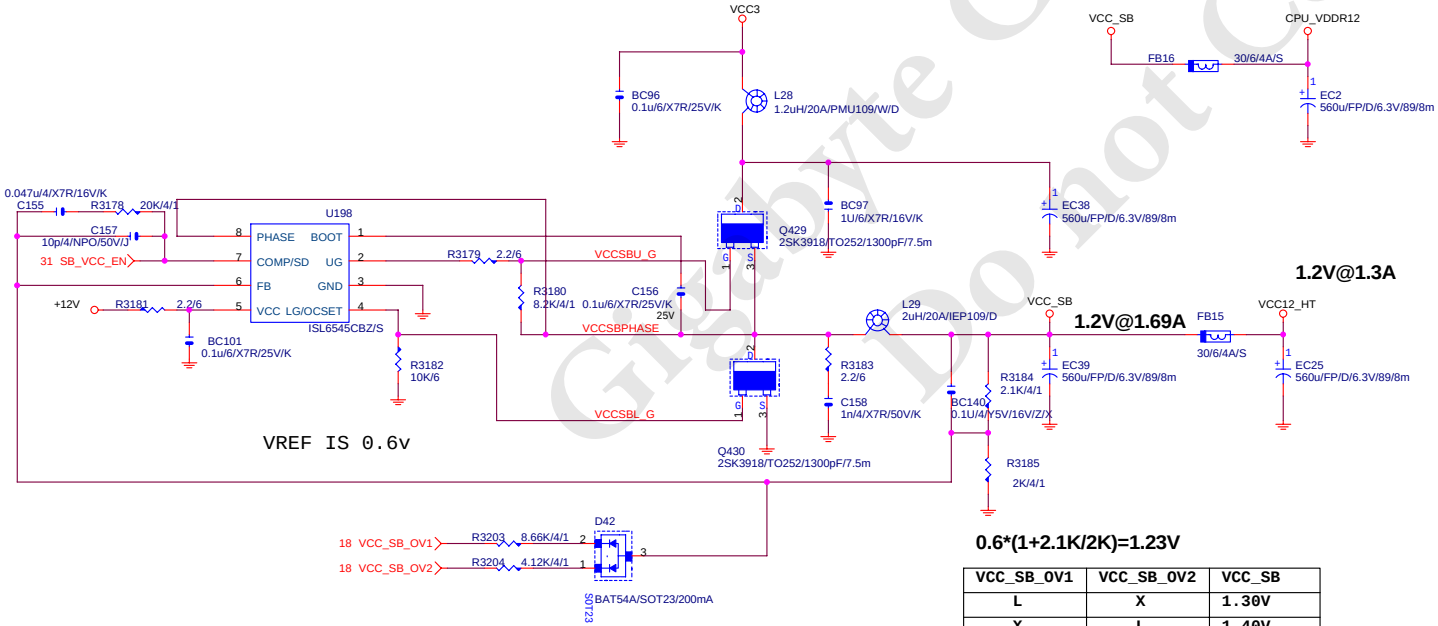
GIGABYTE

Title: POWER SEQUENCE ,EUP		
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 31 of 35	



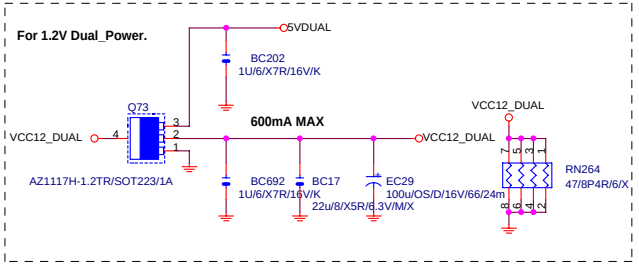
0.6*(1+2K/2.37K)=1.106V

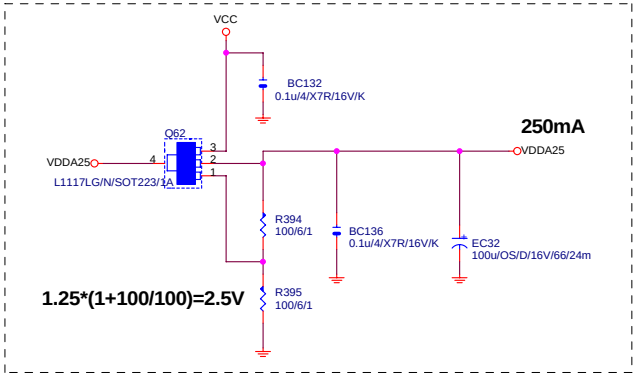
NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V



0.6*(1+2.1K/2K)=1.23V

VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V





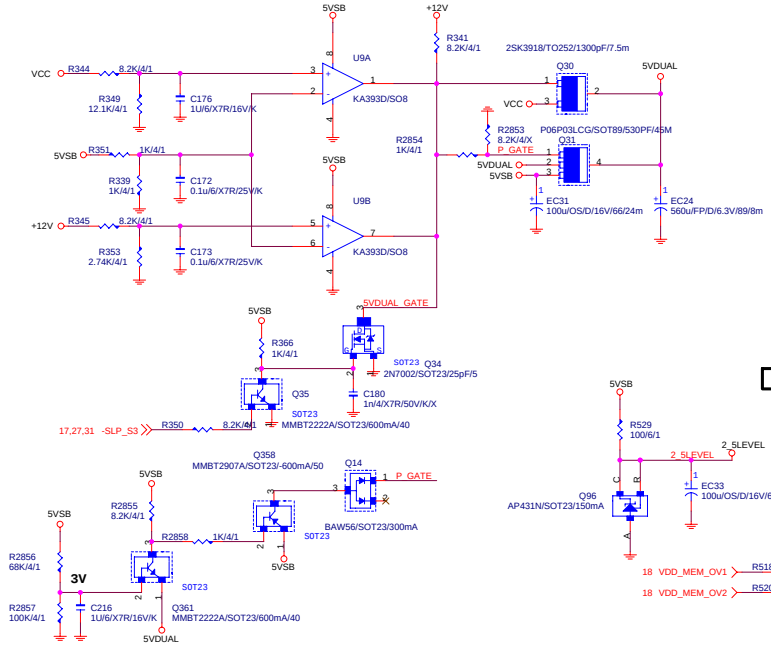
GIGABYTE

Title: NB/SB POWER,VCC12HT,VDDA25,VCC12Dual

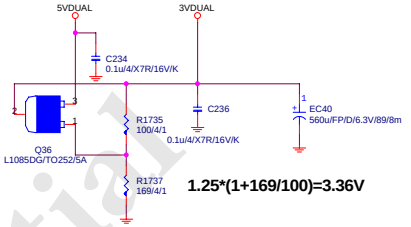
Size	Document Number	Rev
Custom	GA-MA785GMT-UD2H	3.3

Date: Monday, April 19, 2010 Sheet 32 of 35

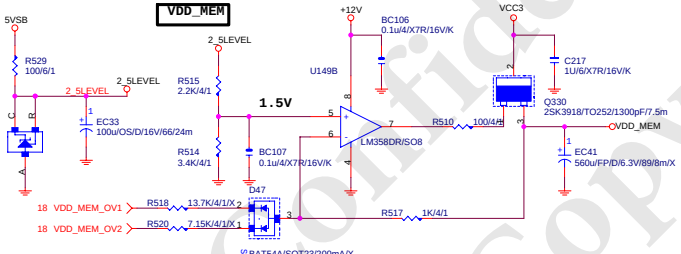
5VDUAL



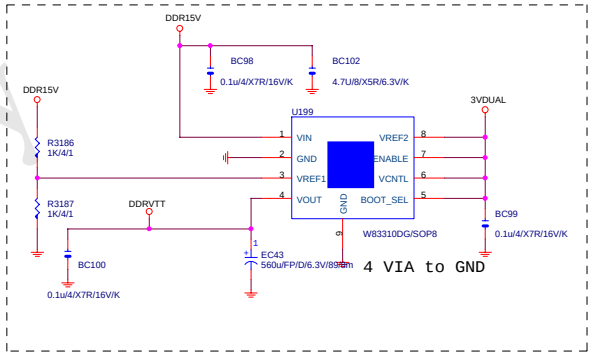
3VDUAL

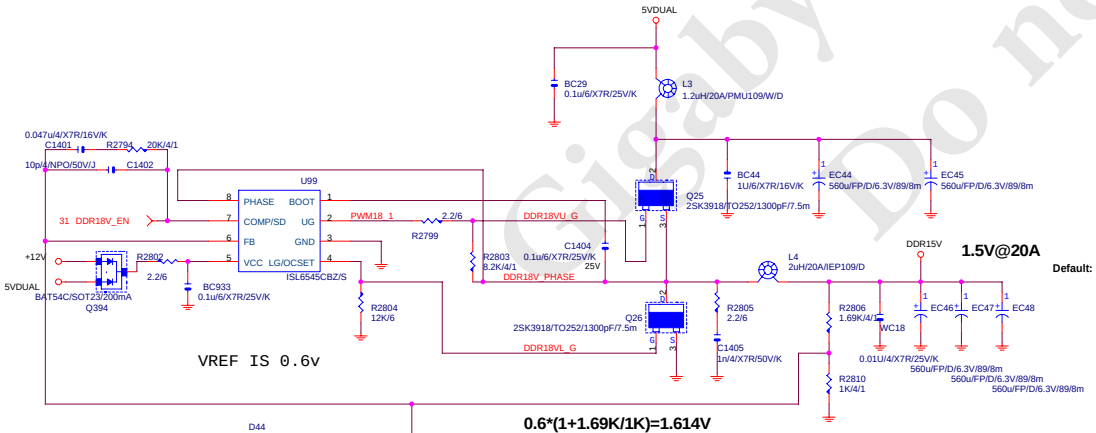


VDD_MEM



VDD_MEM_OV1	VDD_MEM_OV2	VDD_MEM
L	X	1.60V
X	L	1.70V
L	L	1.80V



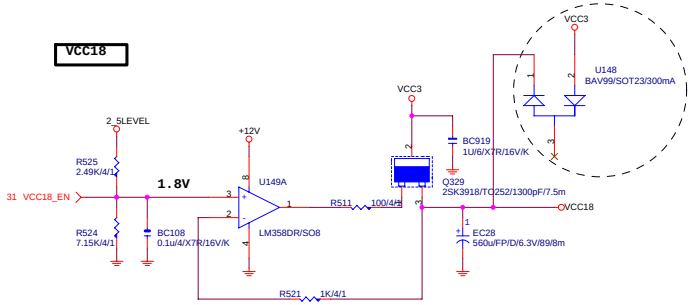


DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
L	X	X	X	1.65V
X	L	X	X	1.70V
L	L	X	X	1.75V
X	X	L	X	1.80V
L	X	L	X	1.85V
X	L	L	X	1.90V
L	L	L	X	1.95V

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
X	X	X	L	2.00V
L	X	X	L	2.05V
X	L	X	L	2.10V
L	L	X	L	2.15V
X	X	L	L	2.20V
L	X	L	L	2.25V
X	L	L	L	2.30V
L	L	L	L	2.35V

VCC18

ATI for vcc3/vcc18 power ramp-up 2.1V



GIGABYTE

Title: DDRII POWER , VCC18

Size	Document Number	Rev
C	GA-MA785GMT-UD2H	3.3

Date: Monday, April 19, 2010 Sheet 33 of 35

PCIE-1G LAN

RTL8111C

LR36:
RTL8101E/8102E -->X
RTL8111C-->0

LR33:0/6 DISABLE SWICHING REG

LR16:
RTL8101E-->2K/4/1
RTL8111C/8102E-->2.49K/4/1

LU1

RTL8111C-VCO-GR/QFN64

Dual Color LED

Single Color LED

P35-152-19W9

YELLOW ORANGE (+,-) GREEN (-,+)

CLOSE LAN CHIP

LL1/LFB10 CO-LAYOUT CLOSE

CHOKE4U7-500MA

LL1/LBC64/LBC63
CLOSE LU1 PIN1

RTL8102E LFB7-->X

FOR 93C46 OR BIOS DETECT
RTL8102E -->X

USB_LAN CONNECTOR

RTL8101E:LR38/LC5/LR43/LC6-->0
RTL8102E:LC5/LC6-->0
RTL8111C:LC6-->0

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1

RTL8102E -->X

CLOSE LAN CHIP

LC6:
100M:0.1U
1G:0.01U

USB_LAN

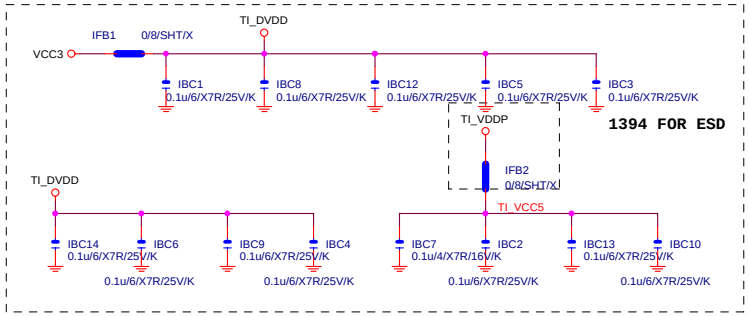
USB+LAN/1G/GO,Y/OS/RA/D/8C

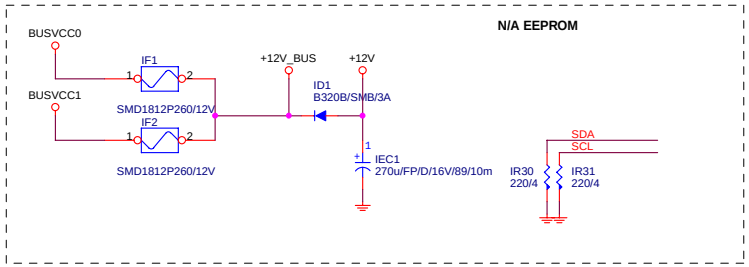
EC要靠近USB_PORT的FUSEVCC

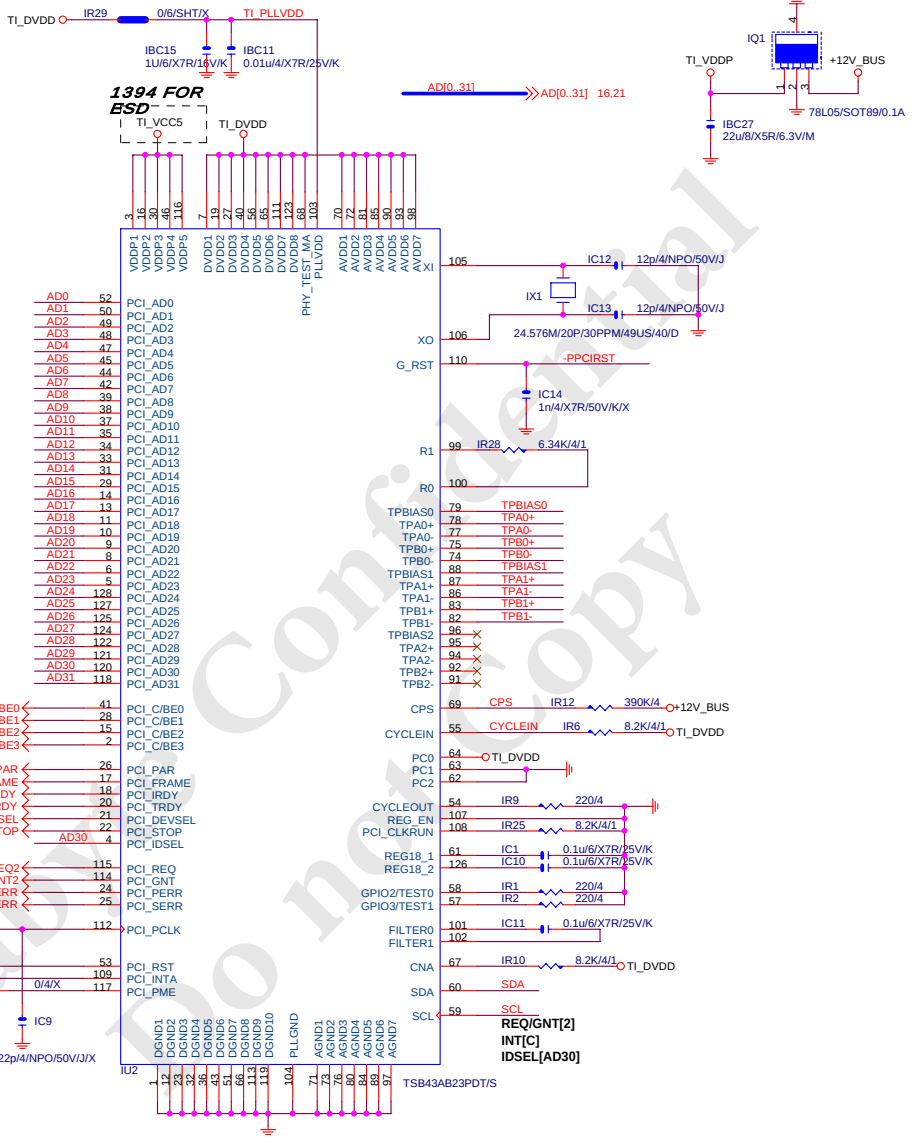
USB_LAN

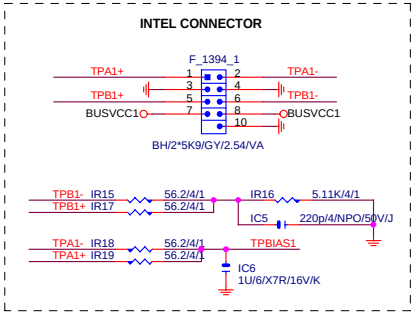
EMI

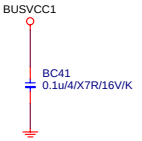
Title	REALTK RTL8111C/8101E
Size	Custom
Document Number	GA-MA785GMT-UD2H
Rev	3.3
Date:	Monday, April 19, 2010
Sheet	34 of 35

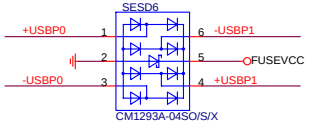


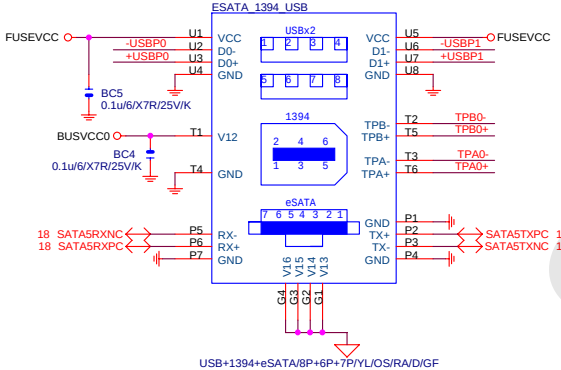


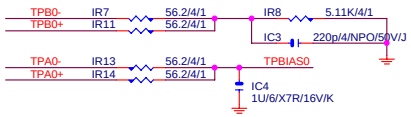


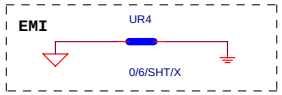












GIGABYTE

Title	TI TSB43AB23 1394A	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 35 of 35	