GA-MA785GMT-UD2H

Revision : 3.3

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Title: COVER SHEET		
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Model Name:GA-MA785GMT-UD2H

Component value change history

Version: 3.3

P-Code: U97028-0

Date	Change Item	Reason
2008.05.08	0.1 New BOM Release.	Modify from 9MMA78G2H-00-11C
2008.05.30	1.0A BOM Release.	Fixed CPU C1 reset issue ,Add SB OV
2008.09.16	1.0B BOM Release.	Improve PWM ISL6324 Comp/APA value for Intersil recommend
2008.10.29	0.1 New BOM Release.	Modify from MA78GPM-DS2H 1.0
2008.11.26	0.2 New BOM Release.	Modify from MA78GPM-UD2H 0.1 , Change spec.
2008.12.22	1.0A BOM Release	Modify SPI BIOS I/F FROM SB
2009.04.23	2.0A BOM Release	Modify from 9MMA78PU2-00-10A Co-Lay PCB GA-MA78GPM-UD2H/GA-MA78GM-UD2H/GA-MA78GM-UD2H
2009.05.07	0.1 BOM Release	Modify from 9MMA78PU2-00-20A
2009.06.11	1.0A BOM Release	Modify from 9MMA78TU2-00-01
2009.06.18	1.0B BOM Release	Co-Lay EC-Cap
2009.08.05	1.0H BOM Release.	Change Sideport memory from Elpida to Hynix
2009.10.22	1.1A BOM Release	Add EUP function ,Colay ALC892
2009.10.23	1.1A BOM Release	share PCB FROM MA785GPMT-UD2H 1.1A ,remove sideport memory
2009.11.16	1.1B BOM Release	Modify 5VDual protect schematic
2010.03.01	1.3A BOM Release	For Turbo 3D feature ,Modify NB_HS ,Add Sticker
2010.04.20	3.3A BOM Release	Modify Fuse F1,F2,F5 to 3.5A for F_USB port 3倍力

Circuit or PCB layout change for next version

Date	Change Item	Reason
2008.05.07	Rev0.1 Gerber-out	Modify from GA-MA78GM-S2H Rev1.1
2008.05.30	Rev1.0 Gerber-out	Modify NP 孔距 Foot-print ,Remove 未上件 DIP EC-cap , Modify DBIOS_RST- signal
2008.11.26	Rev0.2 Gerber-out	Change SB Chipset to SB750 and Add ACC Function / RAID 5
2008.12.22	Rev1.0 Gerber-out	Modify SPI BIOS I/F FROM SB
2009.04.22	Rev2.0 Gerber-out	Modify from GA-MA78GPM-UD2H Rev1.0 Co-Lay PCB GA-MA78GPM-UD2H/GA-MA78GM-UD2H/GA-MA78GM-UD2H
2009.05.06	Rev0.1 Gerber-out	Modify from GA-MA78GPM-UD2H Rev2.0
2009.06.10	Rev1.0 Gerber-out	Modify from GA-MA78GMT-UD2H Rev0.1
2009.06.11	Rev1.0 Gerber-out	Co-Lay PCB GA-MA785GPMT-UD2H/GA-MA785GMT-UD2H
2009.06.16	Rev1.01 Gerber-out	Co-Lay EC-Cap
2009.10.21	Rev1.1 Gerber-out	Add EUP function ,Colay ALC892
2009.11.13	Rev1.11 Gerber-out	Modify 5VDual protect schematic
2010.02.26	Rev1.3 Gerber-out	For Turbo 3D feature ,Modify NB_HS ,Add Sticker
2010.04.19	Rev3.3 Gerber-out	Modify silk-screen for F_USB port 3倍力

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Title: BOM & PCB HISTORY

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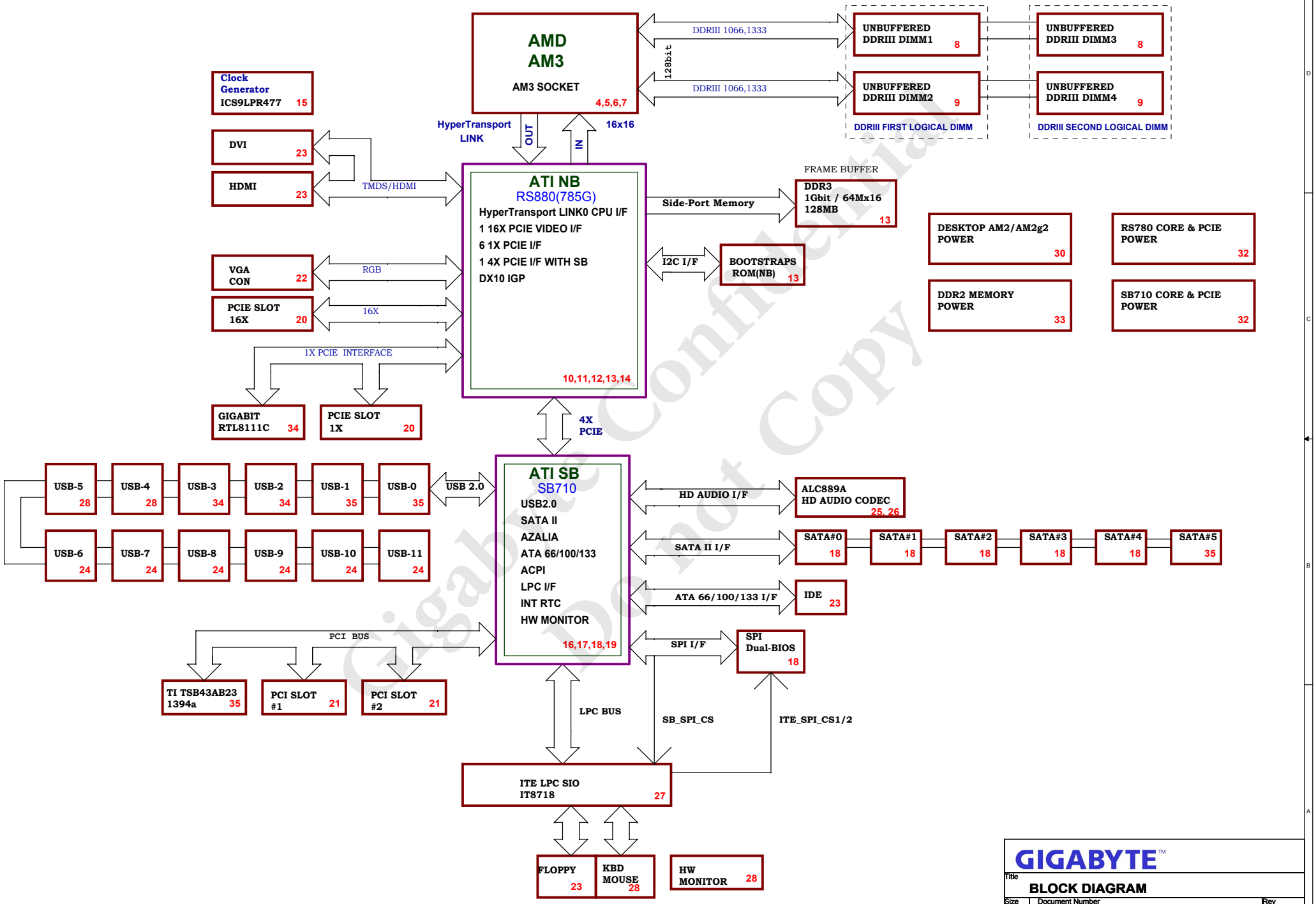
RS880 CUSTOMER DESKTOP REFERENCE DESIGN



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Title	BLOCK DIAGRAM	
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L0_CADIN_L[0..15] L0_CADIN_L[0..15] 10
L0_CADIN_H[0..15] L0_CADIN_H[0..15] 10
L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 10
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 10

CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR15V
CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
VLDT_B = HT12B

M2CPUA

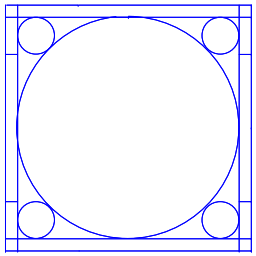
HYPERTRANSPORT

10 L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1 10
10 L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1 10
10 L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0 10
10 L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0 10
10 L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1 10
10 L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1 10
10 L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0 10
10 L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0 10
	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	
	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	
	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	
	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AA6	L0_CADOUT_L14	
	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	
	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	
	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	
	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	
	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	
	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	
	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10	
	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	
	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	
	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	
	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	
	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	
	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	
	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	
	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	
	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	
	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	
	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	
	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	
	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	
	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	
	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	
	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	
	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	
	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	
	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	
	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	
	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	

CPU-SK/941AM3/S/GF/[10SC1-A01941-01R]

M2CPU

AM2RM/PP/BU/PB/[12KRC-04K812-11R]



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Title	CPU HYPER TRANSPORT	
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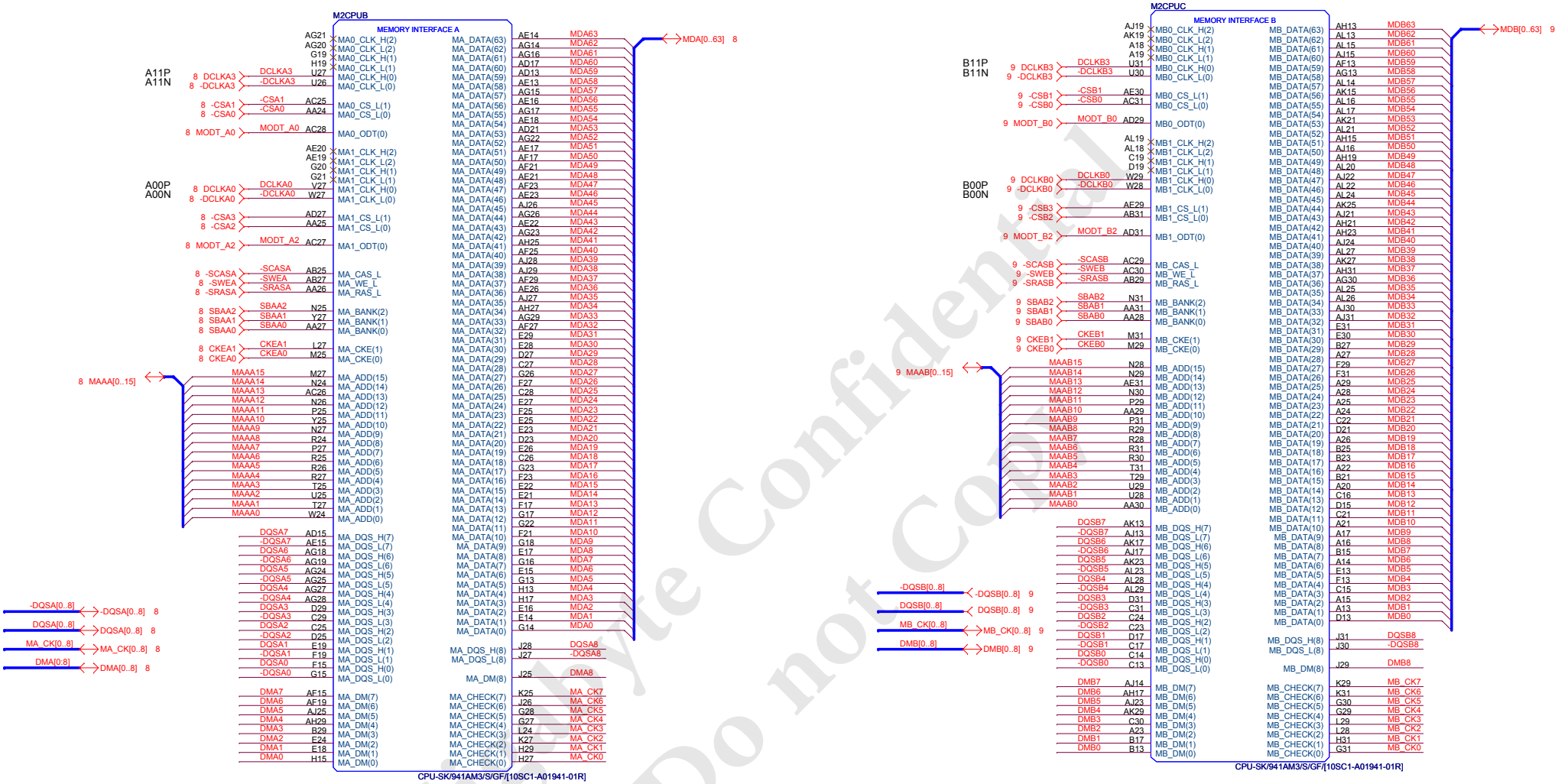

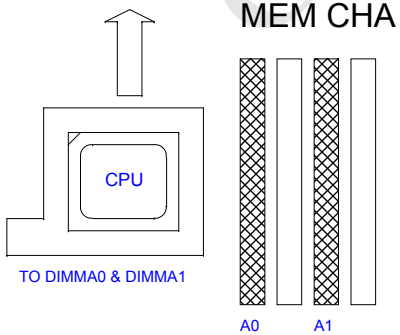

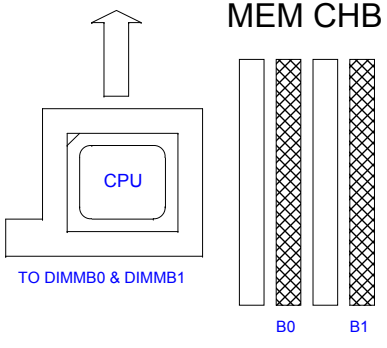

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Title	CPU DDRIII MEMORY	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
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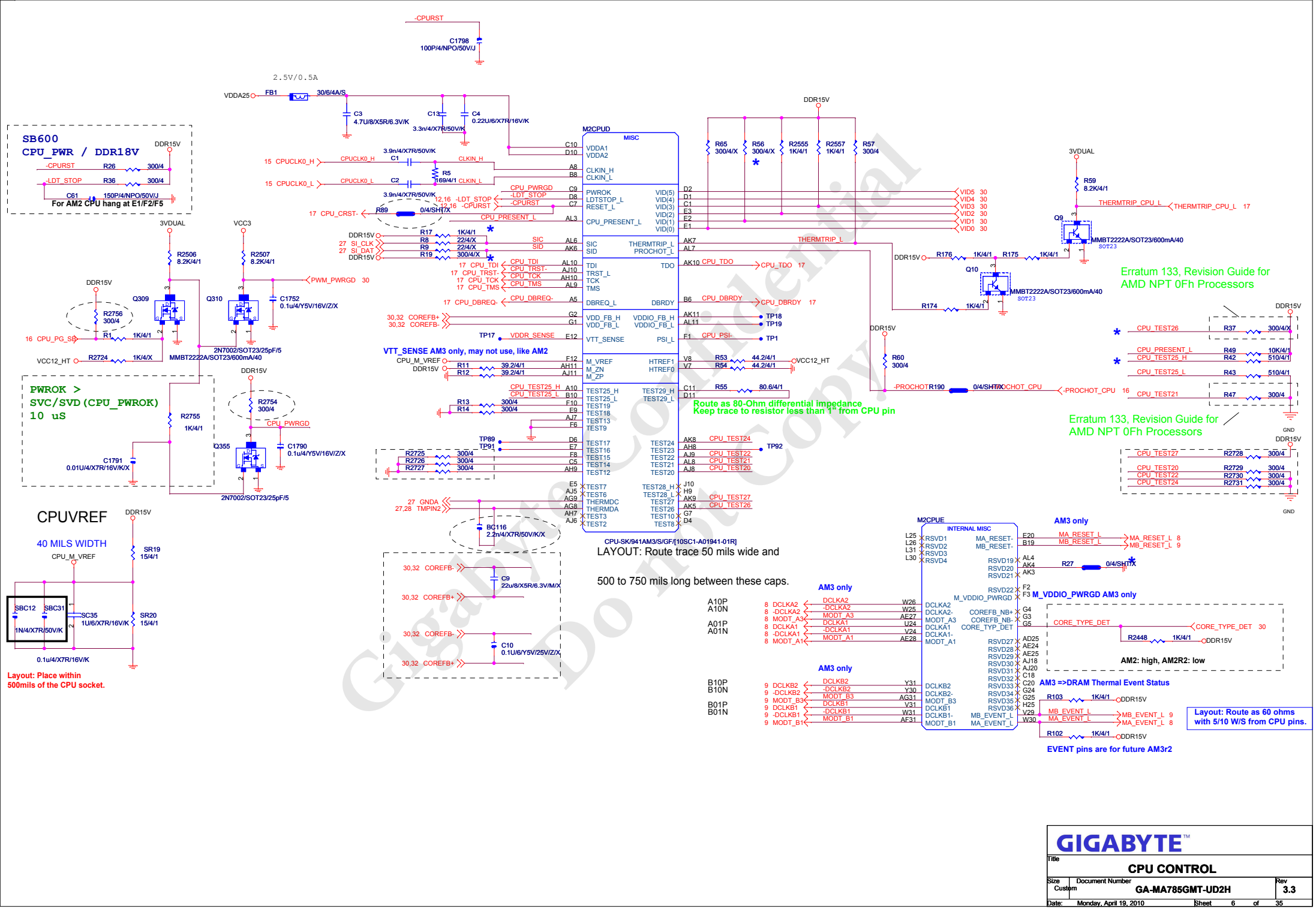
SB600
CPU_PWR / DDR18V
For AM2 CPU hang at E1/F2/F5
PWROK > SVC/SVD(CPU_PWROK) 10 uS
CPUVREF
40 MILS WIDTH
Layout: Place within 500mils of the CPU socket.
VTT_SENSE AM3 only, may not use, like AM2
Route as 80-Ohm differential impedance
Keep trace to resistor less than 1" from CPU pin
LAYOUT: Route trace 50 mils wide and
500 to 750 mils long between these caps.
Erratum 133, Revision Guide for AMD NPT 0Fh Processors
AM3 only
M_VDDIO_PWRGD AM3 only
AM2: high, AM2R2: low
AM3 =>DRAM Thermal Event Status
EVENT pins are for future AM3r2
Layout: Route as 60 ohms with 5/10 W/S from CPU pins.
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CPU CONTROL
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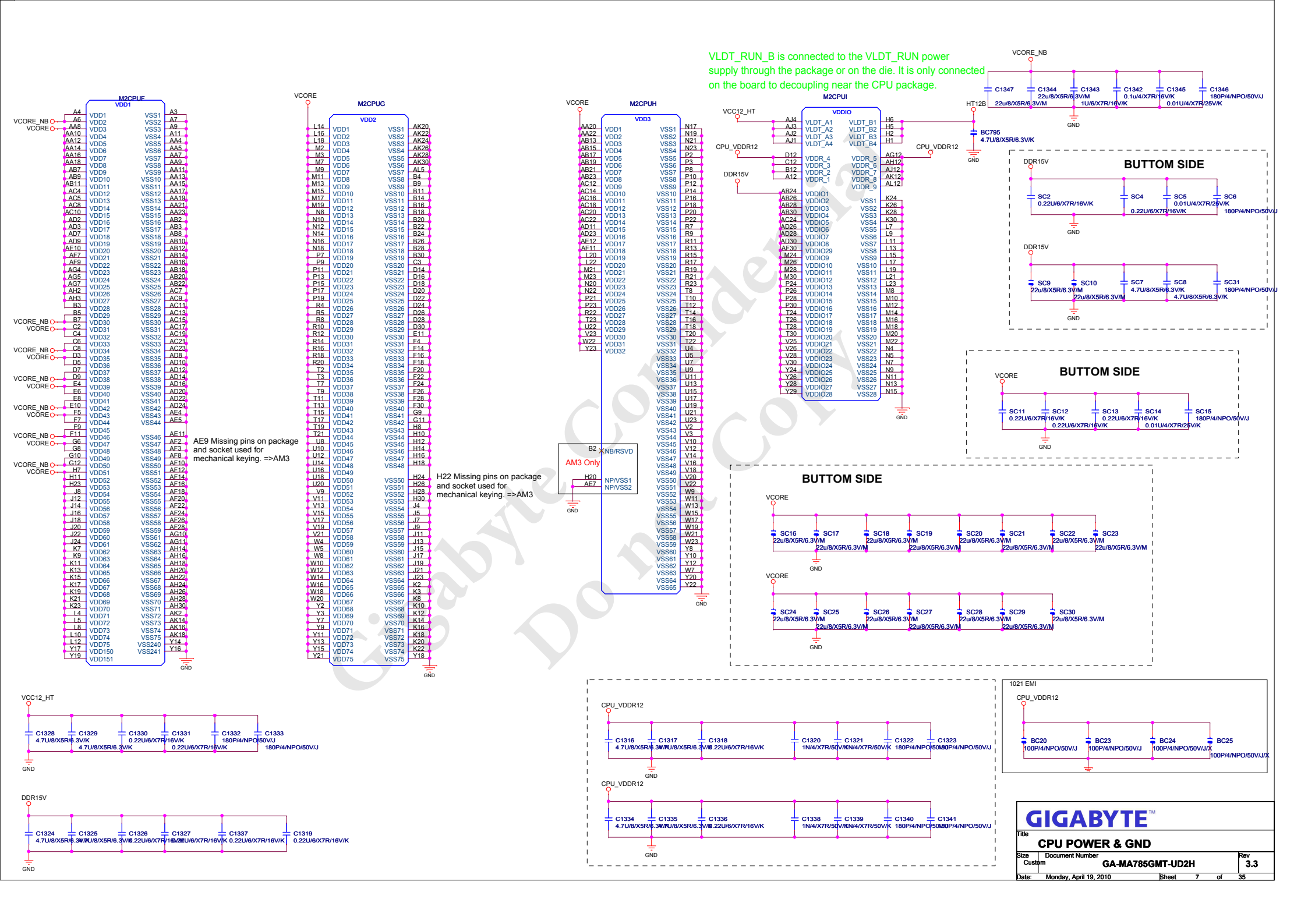
M2CPUF
VDD1
M2CPUG
VDD2
M2CPUH
VDD3
M2CPUI
VDDIO
VCORE
VCORE_NB
CPU_VDDR12
VCC12_HT
DDR15V
HT12B
BC795
4.7U/8/X5R/6.3V/K
AE9 Missing pins on package and socket used for mechanical keying. =>AM3
H22 Missing pins on package and socket used for mechanical keying. =>AM3
B2
NB/RSVD
AM3 Only
H20
NP/VSS1
AE7
NP/VSS2
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.
BUTTOM SIDE
BUTTOM SIDE
BUTTOM SIDE
1021 EMI
GND
Gigabyte Confidential
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GIGABYTE
Title
CPU POWER & GND
Size
Custom
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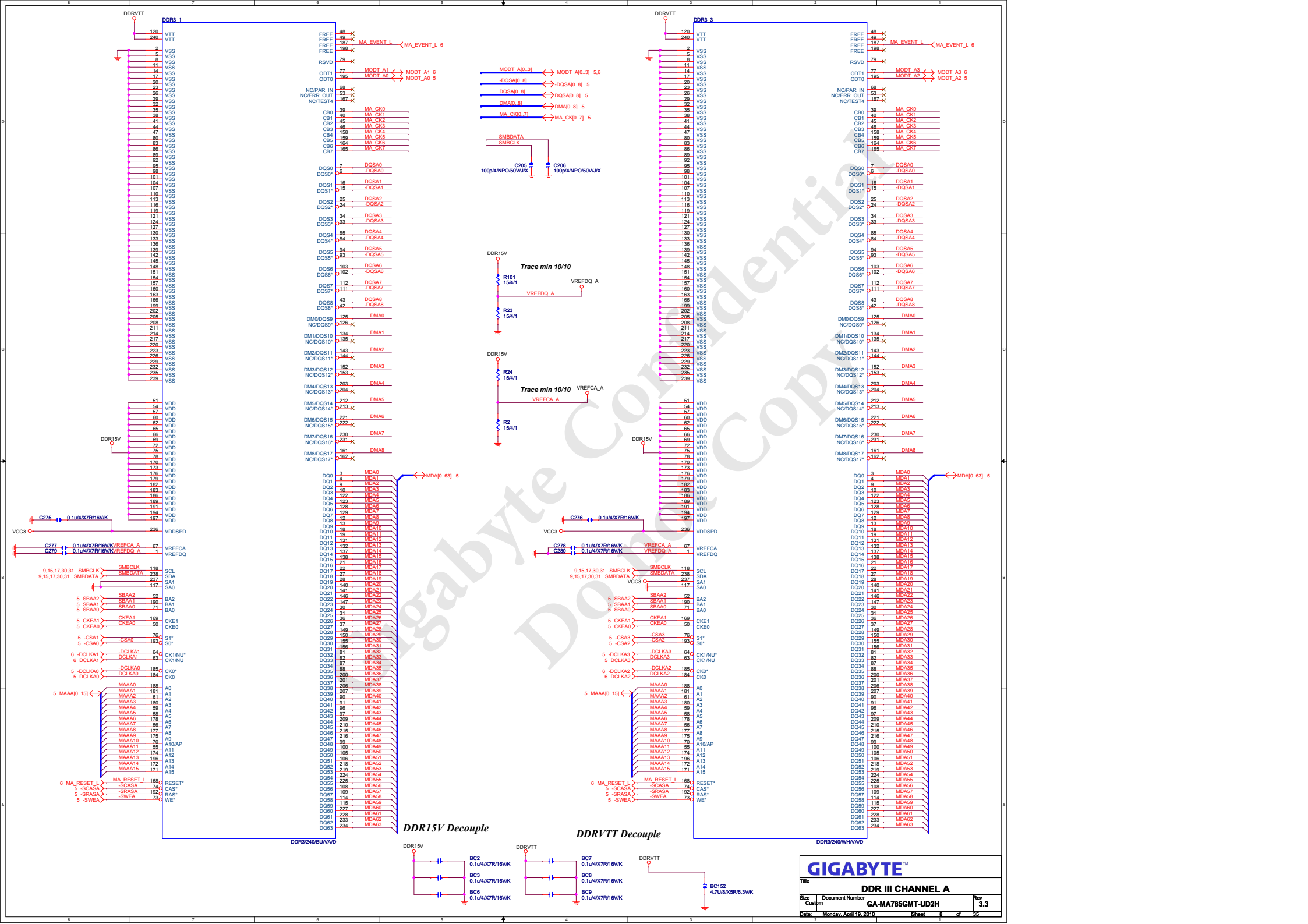

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Title: DDR III CHANNEL A

Size	Document Number	Rev
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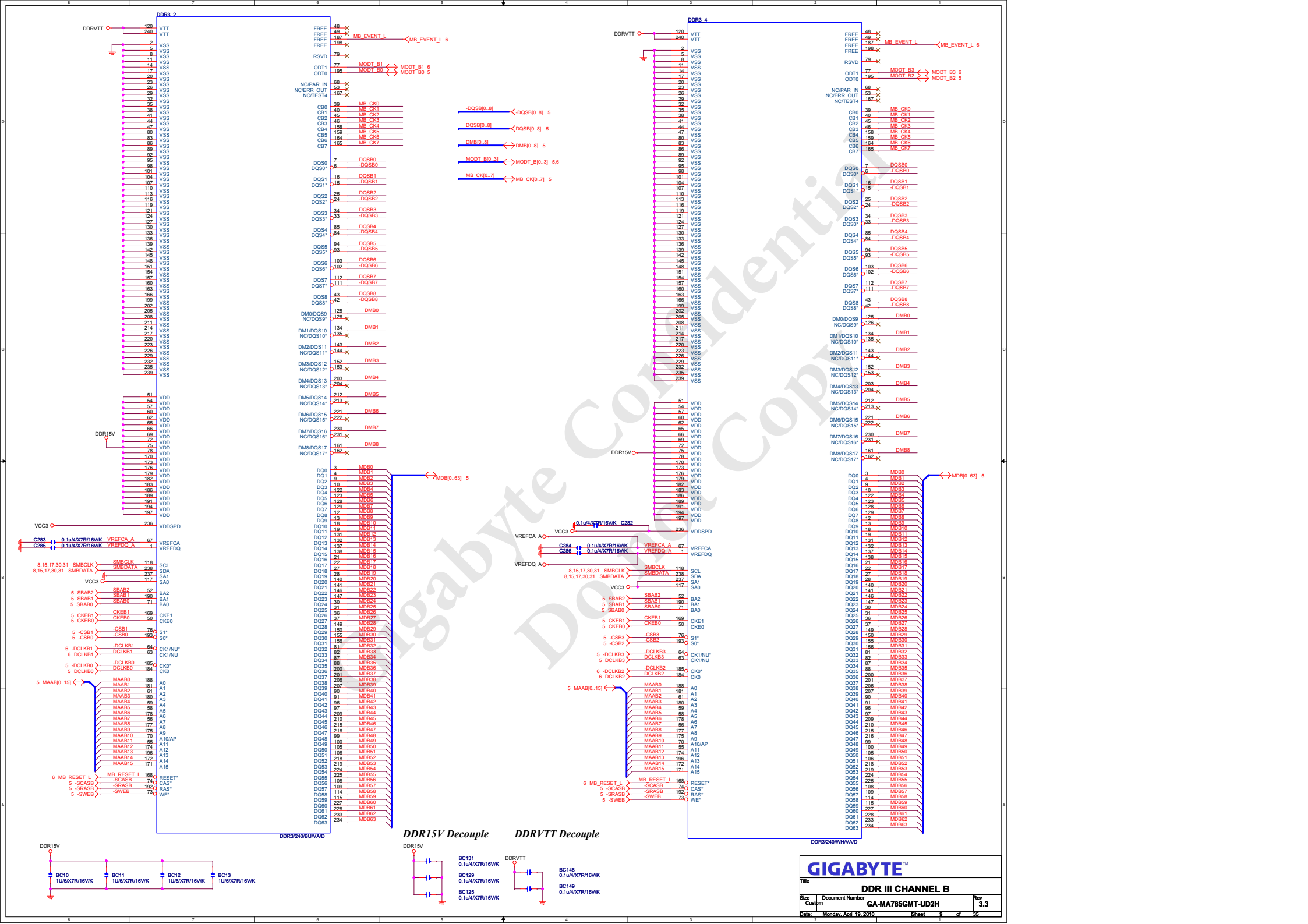

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Title	DDR III CHANNEL B		
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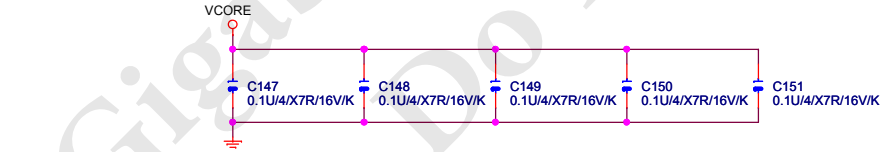
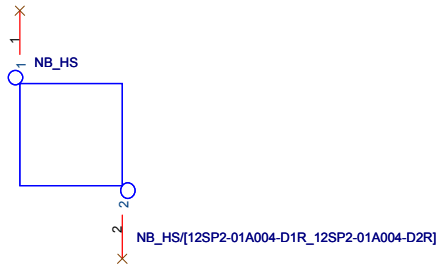


HT Link Stitching Caps

L0_CADIN_L[0..15] L0_CADIN_L[0..15] 4
L0_CADIN_H[0..15] L0_CADIN_H[0..15] 4

L0_CADOUT_L[0..15] L0_CADOUT_L[0..15] 4
L0_CADOUT_H[0..15] L0_CADOUT_H[0..15] 4



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Title: RS880 HT-LINK I/F		
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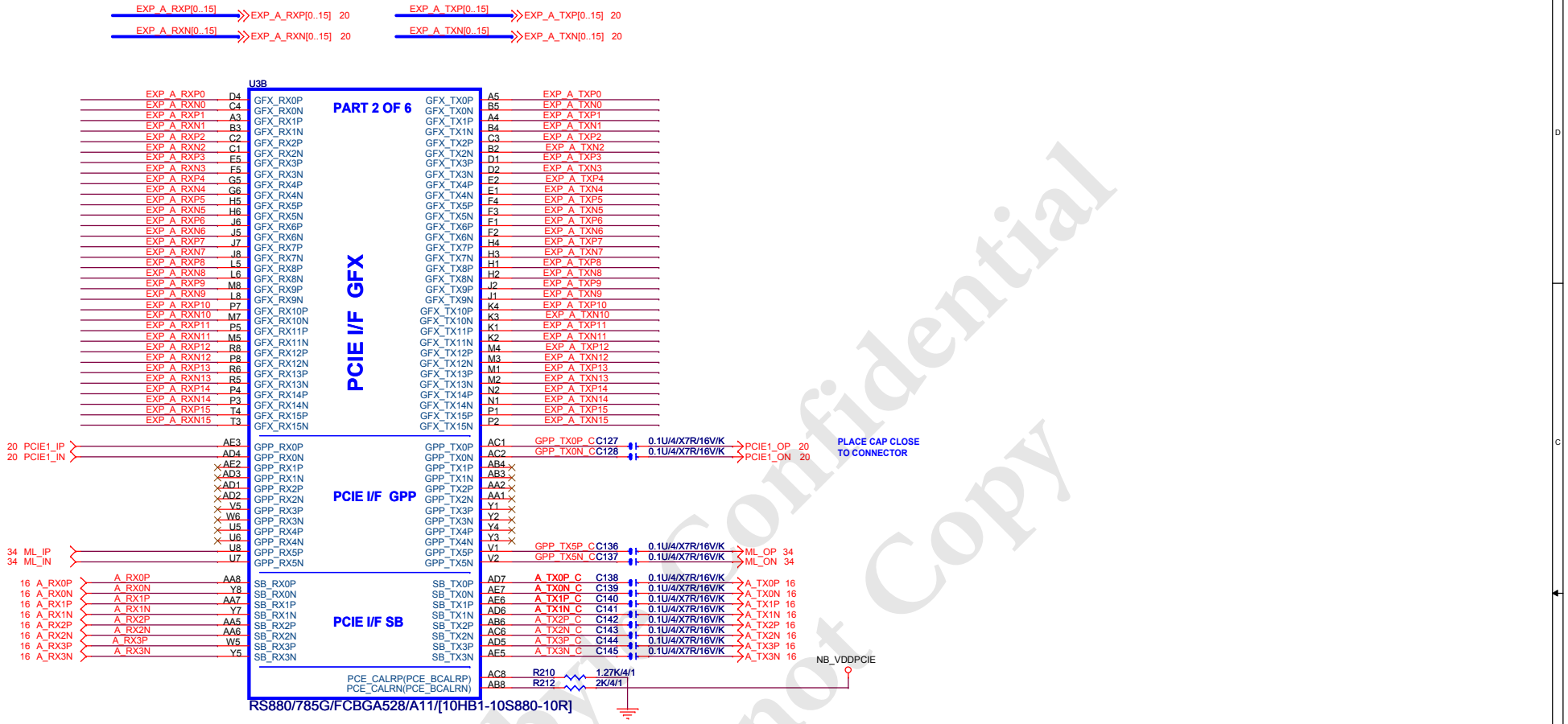

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Title: RS880 PCIE I/F		
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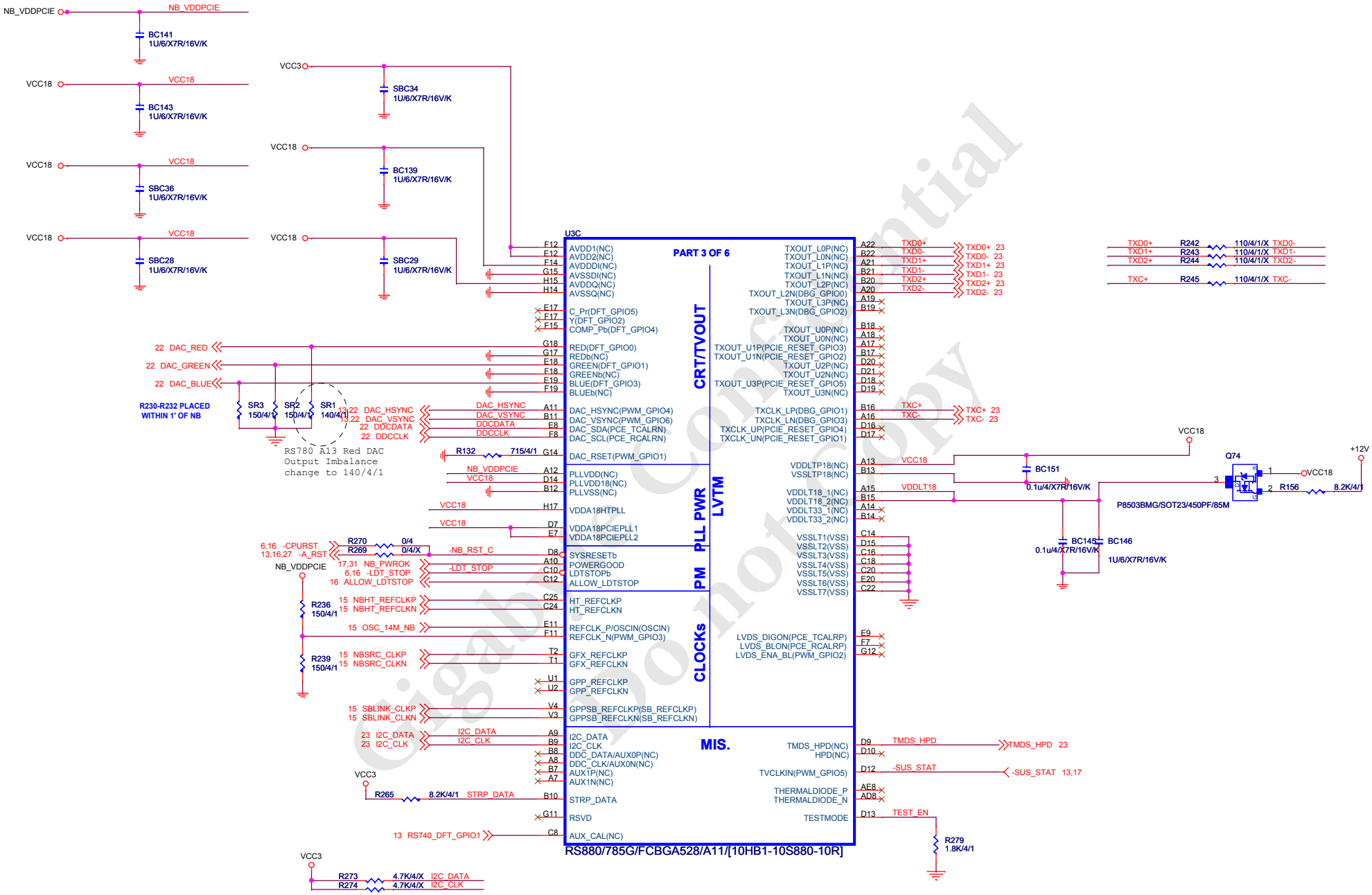

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Title	RS880 SYSTEM I/F	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
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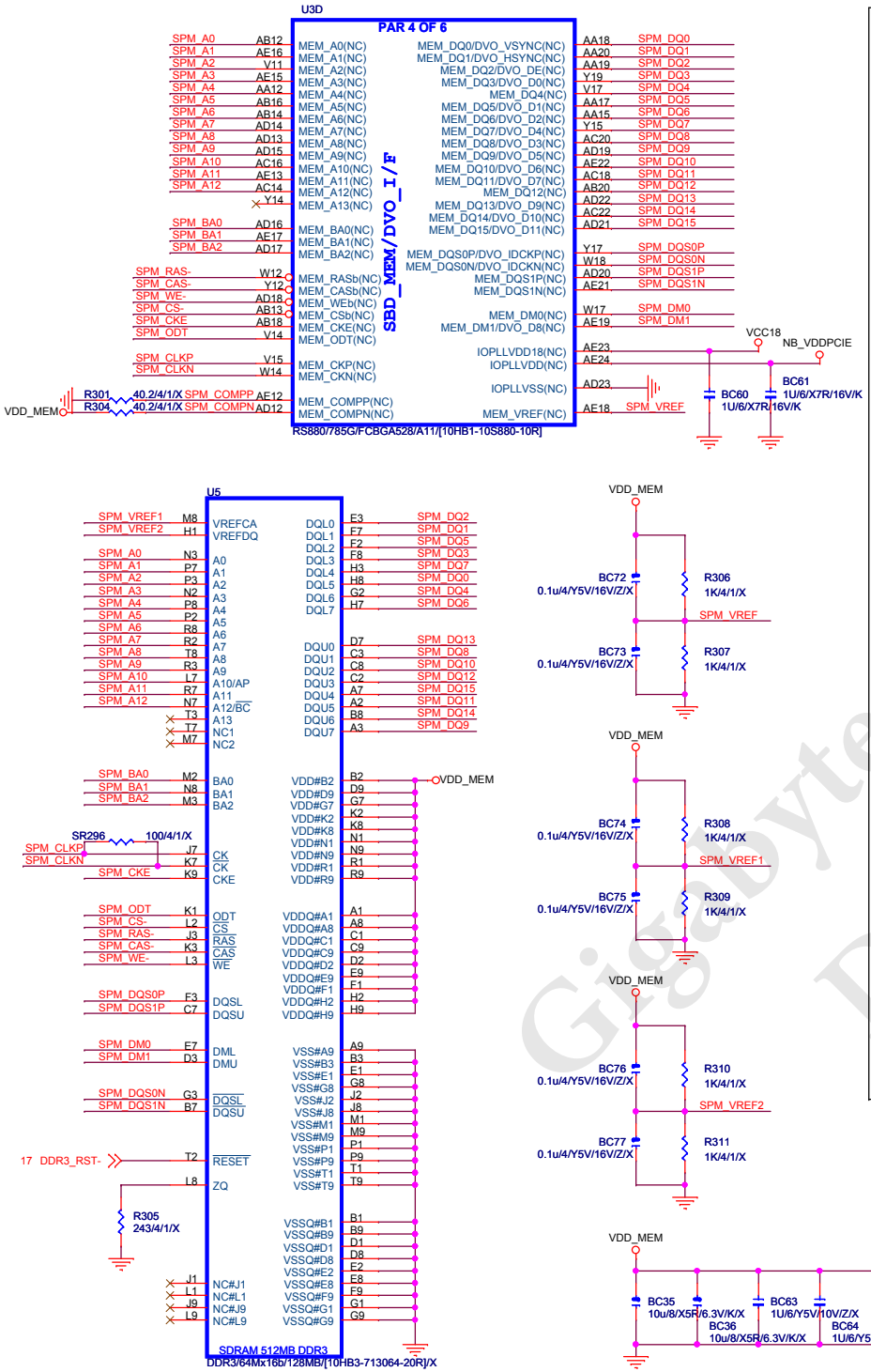

RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL, place close to pin C8

12 RS740_DFT_GPIO1 — R272 150/4/1

Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K accordingly

12,17 -SUS_STAT — D5 CD4148WP/1206/300mA/X — -A_RST 12,16,27

R276 3K/4/1 VCC3
12,22 DAC_VSYNC
R282 3K/4/X

Note: for RX780, change following pull-down resistor to 3K accordingly

R912 (RX780_DFT_GPIO5)

Note: for RX780, change following pull-down resistor to 3K accordingly

R913 (RX780_DFT_GPIO4)
R218 (RX780_DFT_GPIO3)
R911 (RX780_DFT_GPIO2)

12,22 DAC_HSYNC
R286 3K/4/1/X
R285 3K/4/1 VCC3

Note: for RX780, change following pull-down resistor to 3K accordingly

R219 (RX780_DFT_GPIO0)

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable  (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```
These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)   default
110: 4-0-0-0-0   Config A
101: 4-4-0-0-0   Config B
100: 4-2-2-0-0   Config C
011: 4-2-1-1-0   Config D
010: 4-1-1-1-1   Config E
others: register defined (default to Config E)
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1   Mode L   default
110: 1-1-1-1-1-1   Mode L
101: 2-0-2-0-2-0   Mode C2
100: 2-0-2-0-1-1   Mode K
011: 2-0-1-1-1-1   Mode E
010: 1-1-1-1-1-1   Mode L
001: 4-0-0-0-1-1   Mode C
000: 4-0-0-0-2-0   Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0] (configure thru register setting)

```
1-1-1-1-1-1   Mode L   default
1-1-1-1-1-1   Mode L
2-0-2-0-2-0   Mode C2
2-0-2-0-1-1   Mode K
2-0-1-1-1-1   Mode E
1-1-1-1-1-1   Mode L
4-0-0-0-1-1   Mode C
4-0-0-0-2-0   Mode B
```

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1.  Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740:  pin DFT_GPIO0
RS780:  pin HSYNC
RX780:  Not Appicable
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
     thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
                setting only
RS740: Not supported
```


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RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC

U3F

PART 6/6

GROUND

RS880/785G/FCBGA528/A11/[10HB1-10S880-10R]

Please use 1mm pad size, place all ELT test pads on bottom side only

U3E

PART 5/6

POWER

RS880/785G/FCBGA528/A11/[10HB1-10S880-10R]

NB_VCC, NB_VDDPCIE, VCC_SB, VCC18, VDD_MEM, VCC3

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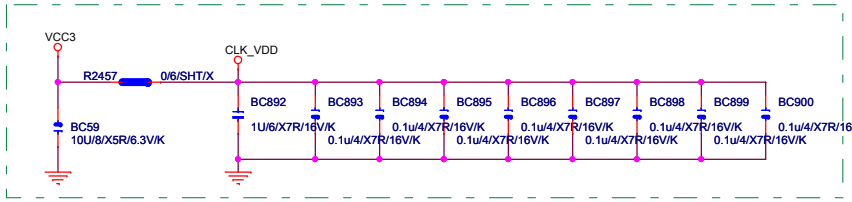
Title: RS880 POWER & GND		
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 14 of 35	

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases

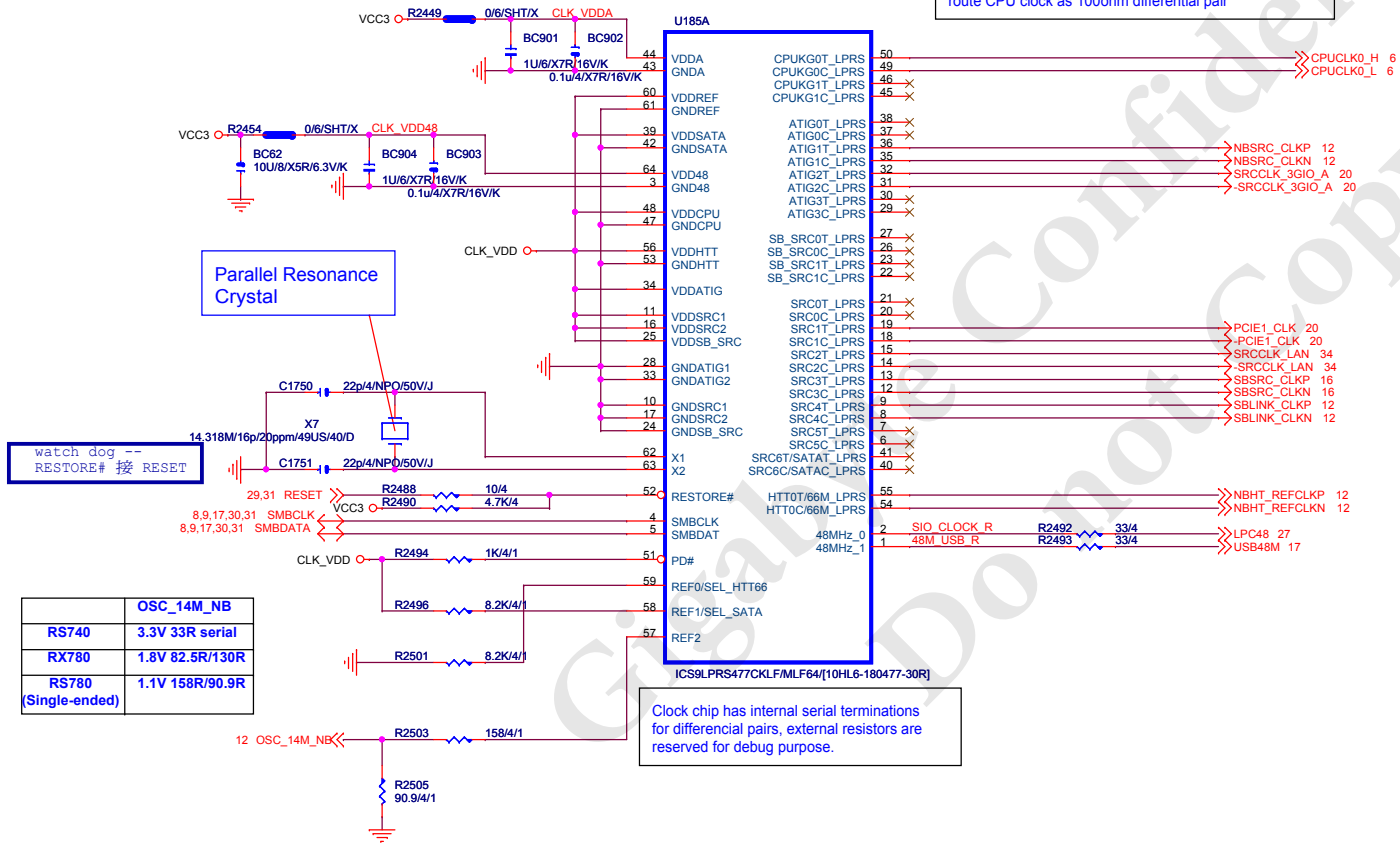


1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

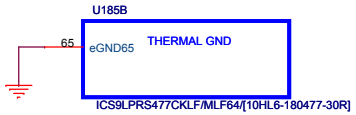
3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R



REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

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Title: ICS9LPRS477

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PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600

S.B HEATSINK

SB_HS

SB_HS/[12SP2-030030-51R_12SP2-030030-52R_12SP2-030030-53R]

U2A

SB700

Part 1 of 5

SB710/FCBGA528/A14/[10HB1-06B710-11R]

PCI CLKS

PCI EXPRESS INTERFACE

PCI INTERFACE

CLOCK GENERATOR

LPC

RTC XTAL

CPU

RTC

Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.

	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

BIOS after boot setting EC AOD-ACC

	LPC_CLK0 Rev.A12	LPC_CLK1
PULL HIGH	IMC ENABLED AOD Extreme	CLKGEN ENABLED
PULL LOW	IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT

20mil 20mil 20mil

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

Title	ATI SB710 PCIE/PCI/CPU/LPC
Size	Custom
Document Number	GA-MA785GMT-UD2H
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Date:	Monday, April 19, 2010
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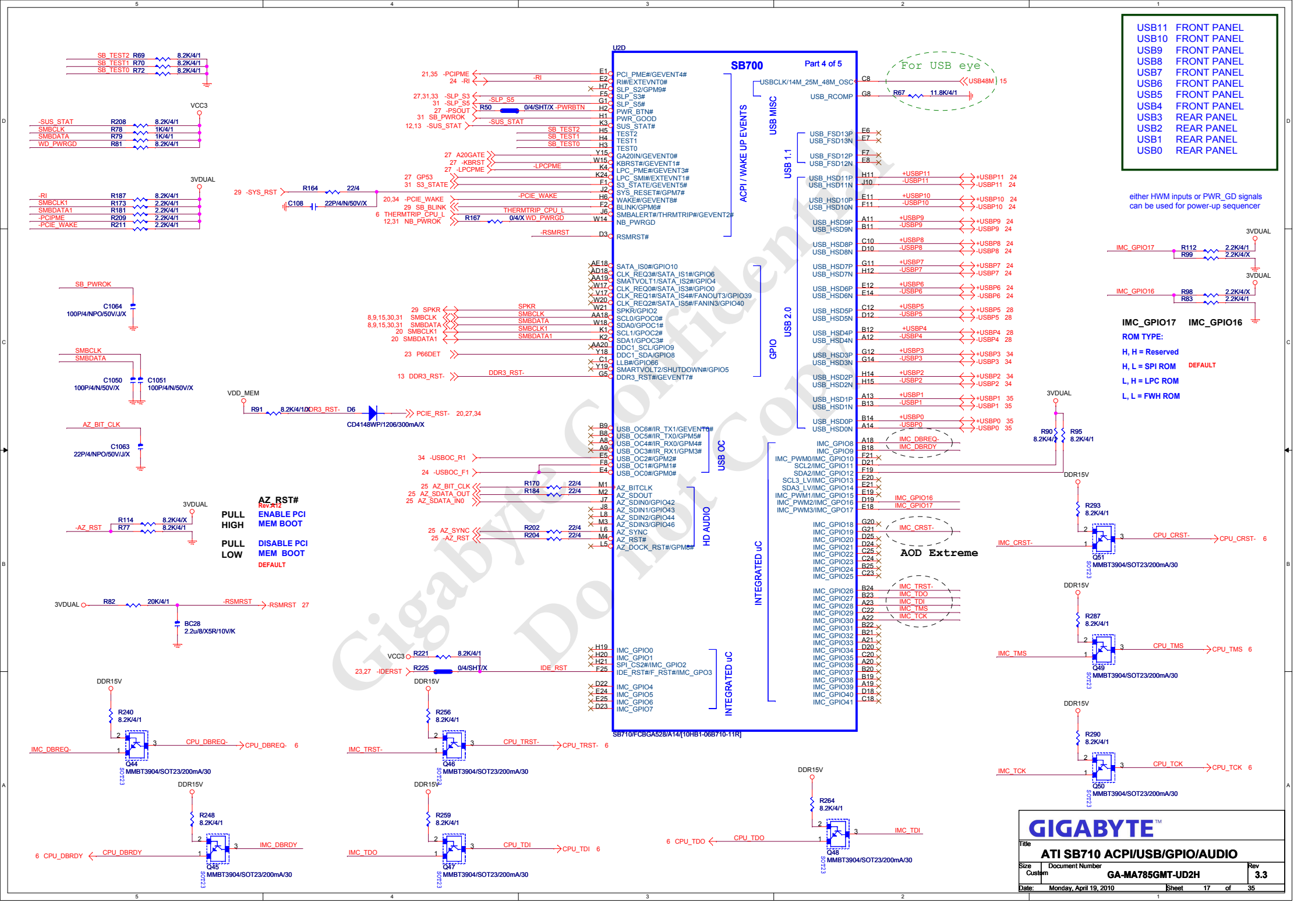
USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 FRONT PANEL
USB4 FRONT PANEL
USB3 REAR PANEL
USB2 REAR PANEL
USB1 REAR PANEL
USB0 REAR PANEL
either HWM inputs or PWR_GD signals can be used for power-up sequencer
IMC_GPIO17 IMC_GPIO16
ROM TYPE:
H, H = Reserved
H, L = SPI ROM DEFAULT
L, H = LPC ROM
L, L = FWH ROM
AZ_RST#
PULL HIGH ENABLE PCI MEM BOOT
PULL LOW DISABLE PCI MEM BOOT DEFAULT
U2D
SB700
Part 4 of 5
For USB eye
AOD Extreme
SB710/FCBGA528/A14/[10HB1-06B710-11R]
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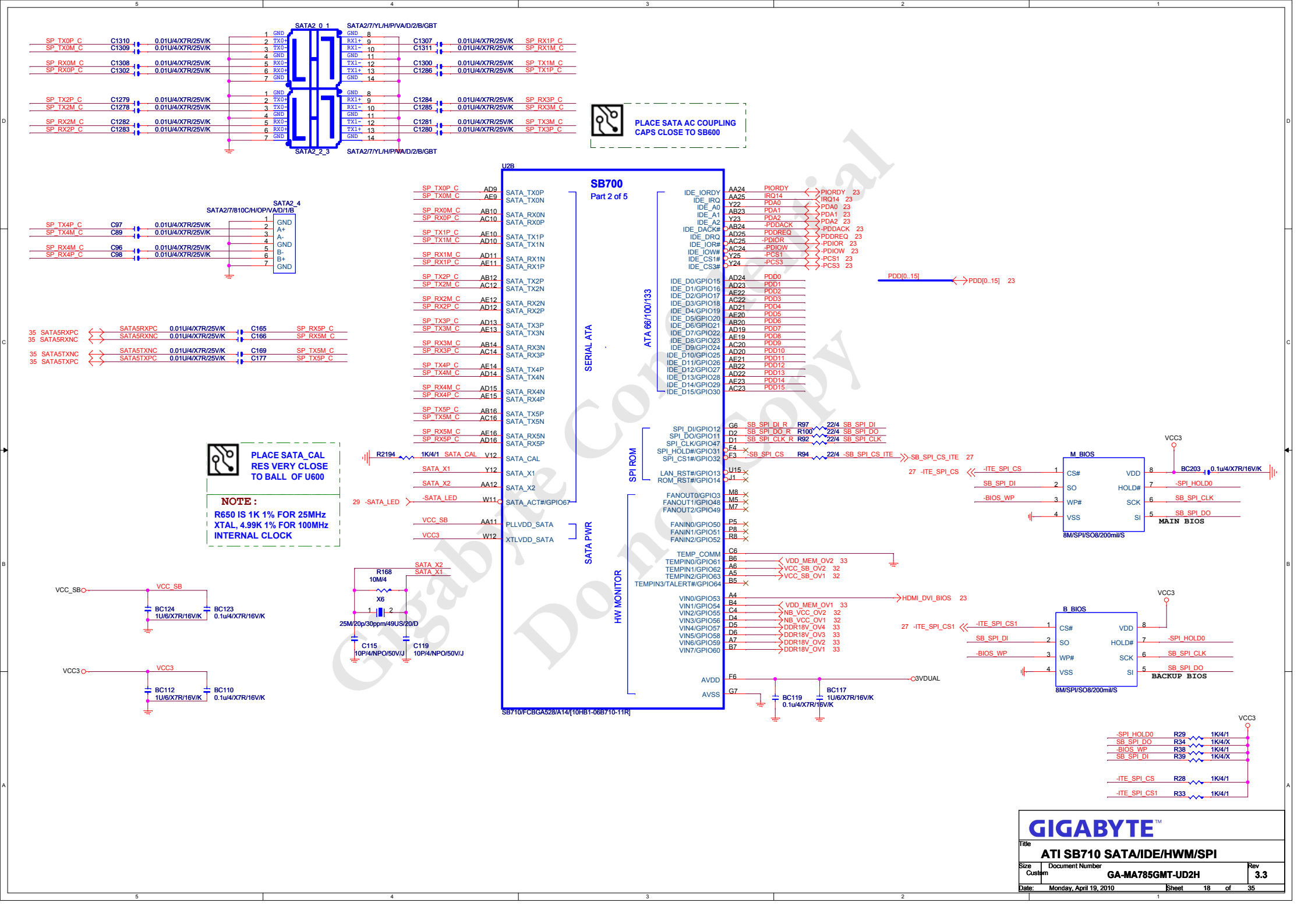
GIGABYTE
Title
ATI SB710 ACPI/USB/GPIO/AUDIO
Size Custom
Document Number GA-MA785GMT-UD2H
Rev 3.3
Date: Monday, April 19, 2010
Sheet 17 of 35


SATA2_0_1
SATA2/7/YL/H/P/VA/D/2/B/GBT
SATA2_2_3
SATA2/7/YL/H/P/VA/D/2/B/GBT
PLACE SATA AC COUPLING CAPS CLOSE TO SB600
SATA2_4
SATA2/7/810C/H/OP/VA/D/1/B
U2B
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
SATA PWR
HW MONITOR
SB710/FCBGA528/A14/[10HB1-06B710-11R]
PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600
NOTE :
R650 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK
M_BIOS
B_BIOS
MAIN BIOS
BACKUP BIOS
8M/SPI/SO8/200mil/S
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ATI SB710 SATA/IDE/HWM/SPI
GA-MA785GMT-UD2H
3.3
Monday, April 19, 2010
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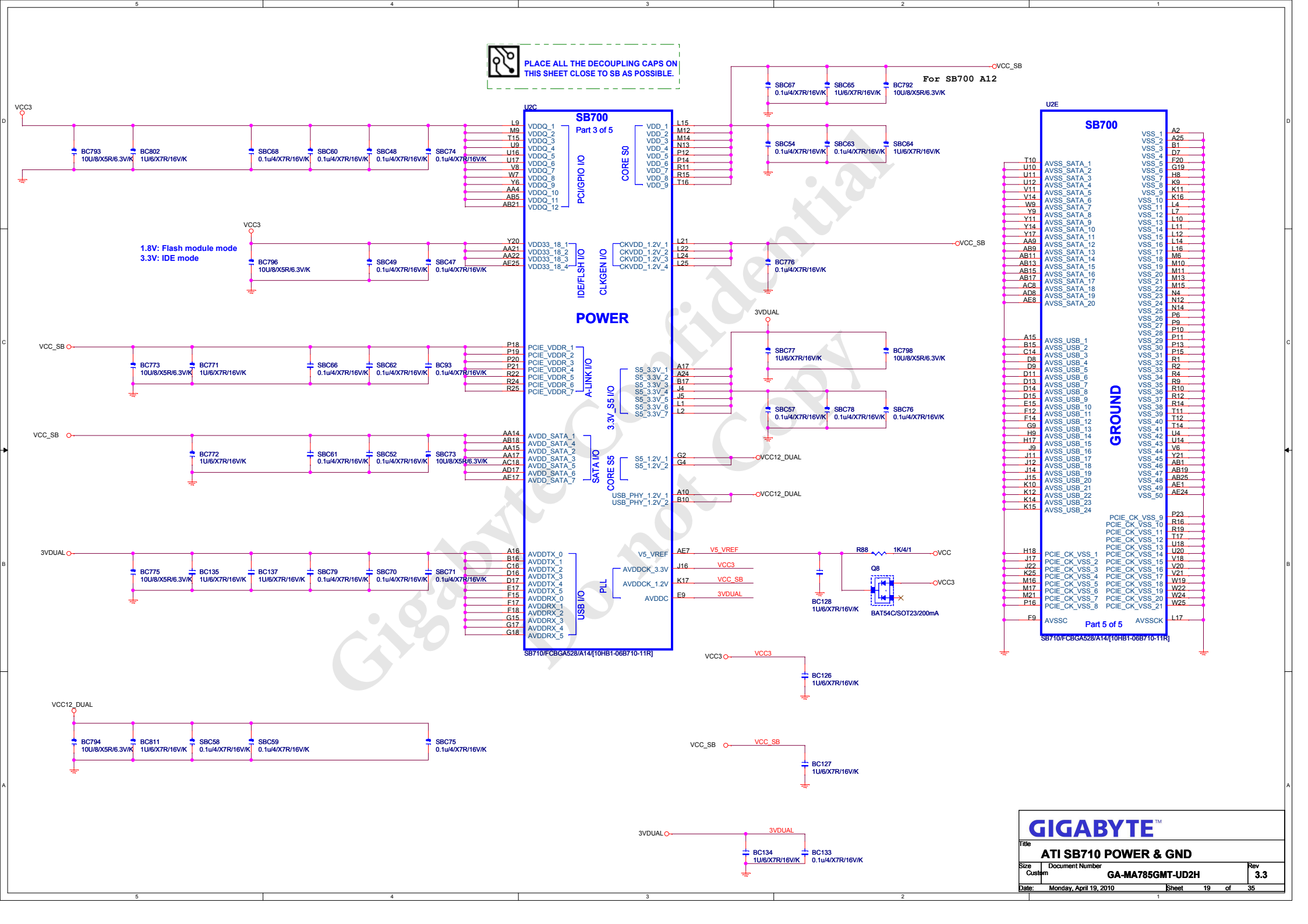
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
For SB700 A12
SB700
Part 3 of 5
POWER
GROUND
Part 5 of 5
1.8V: Flash module mode
3.3V: IDE mode
SB710/FCBGA528/A14/[10HB1-06B710-11R]
BAT54C/SOT23/200mA
GIGABYTE
ATI SB710 POWER & GND
GA-MA785GMT-UD2H
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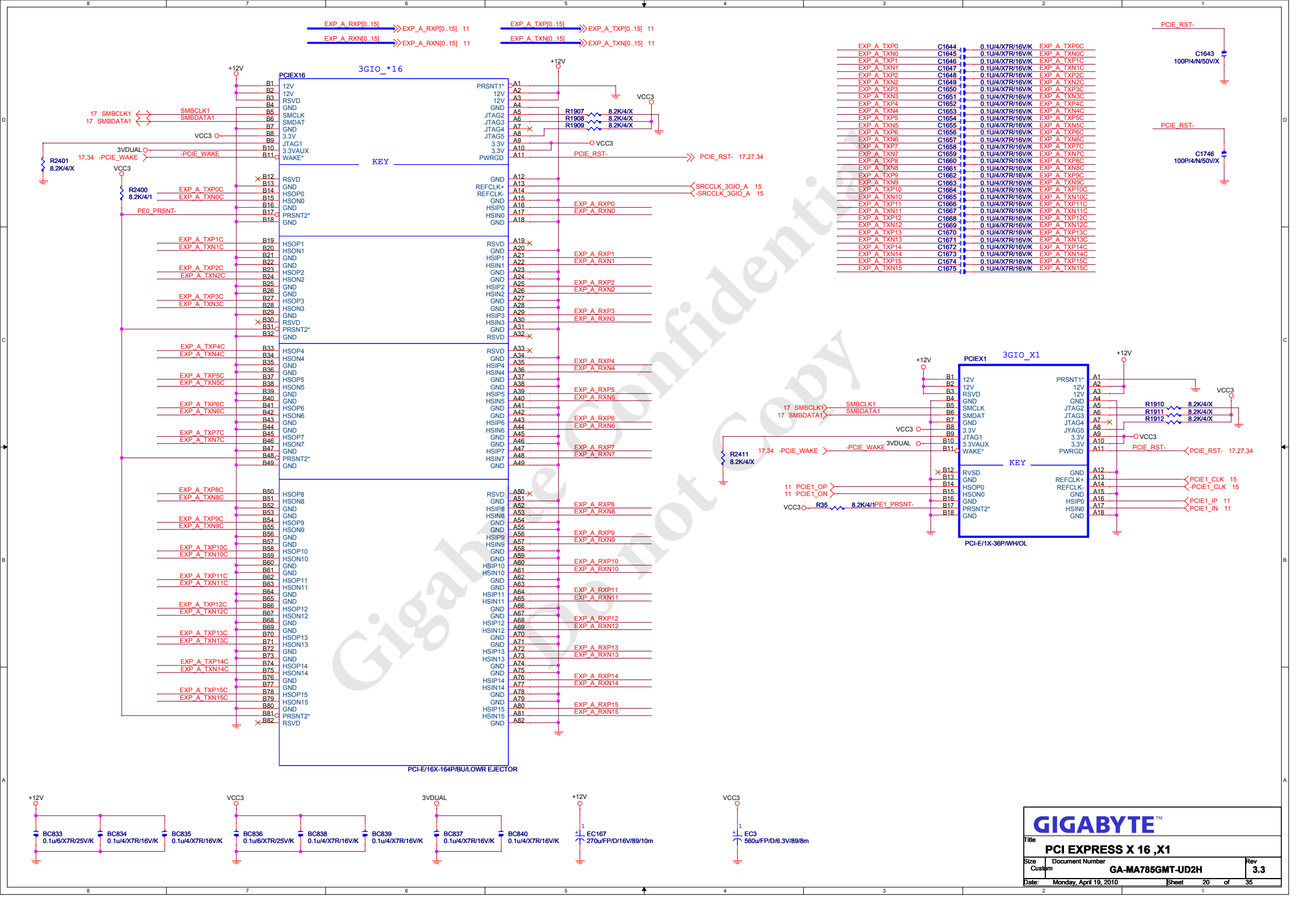

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Title	PCI EXPRESS X 16 ,X1	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
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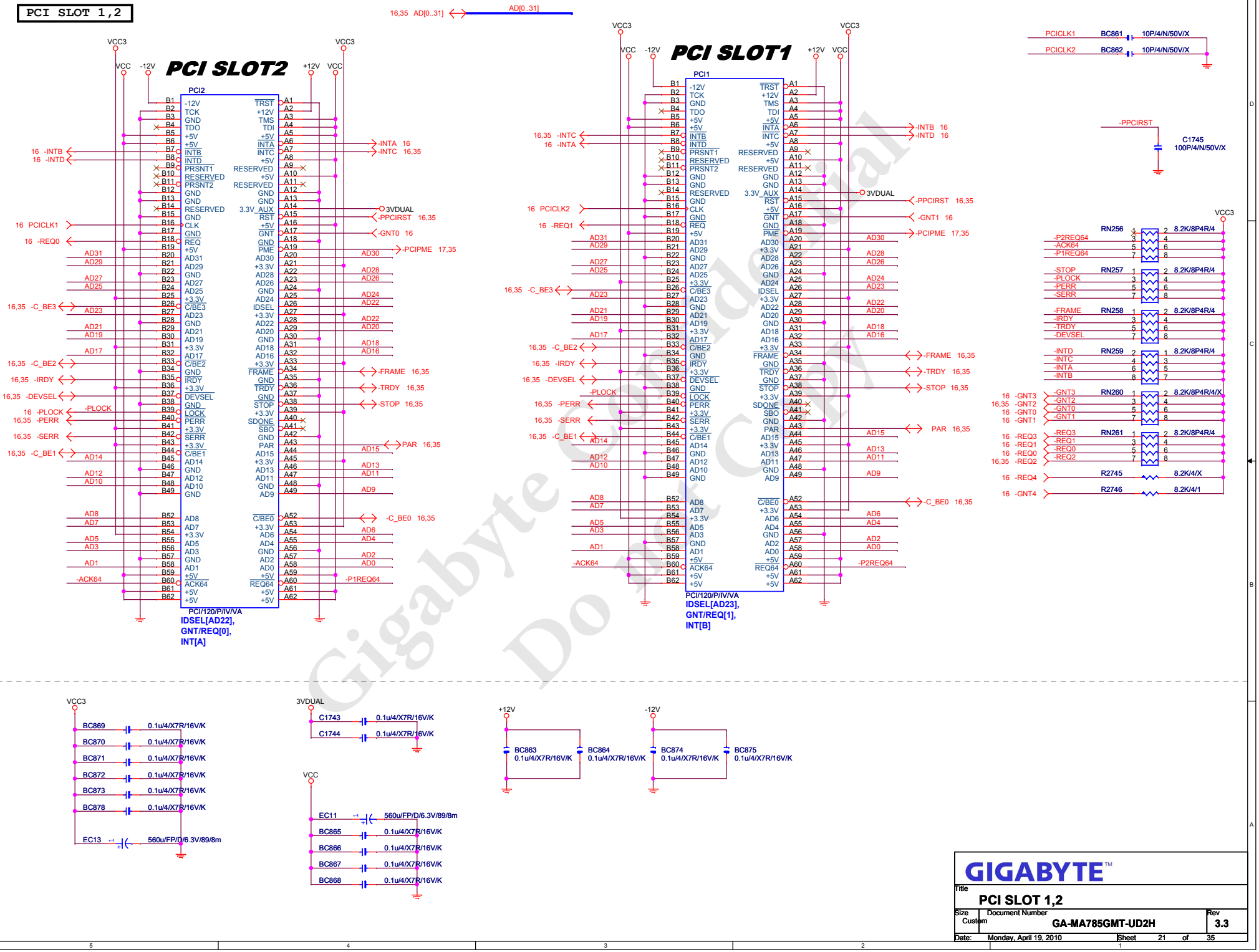
PCI SLOT 1,2



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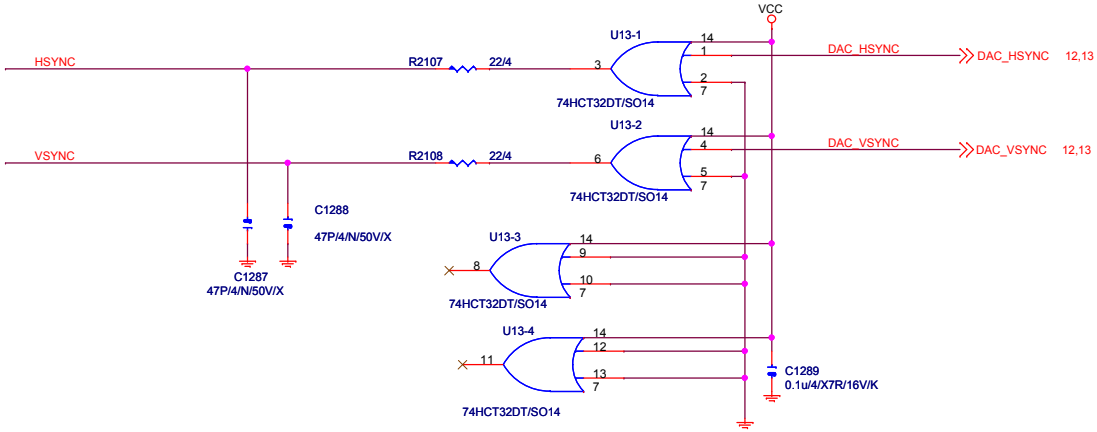
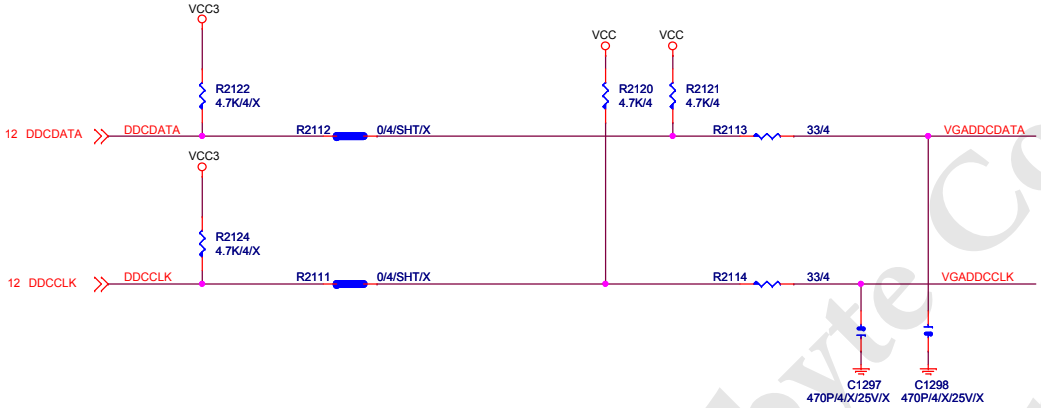
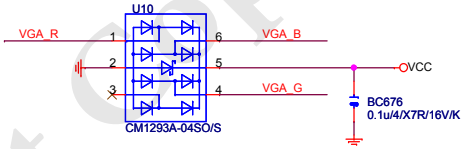
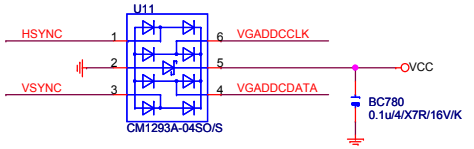
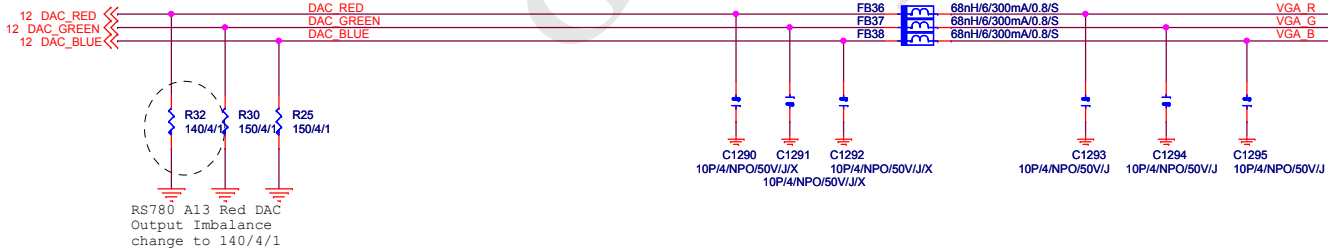
Title	PCI SLOT 1,2	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 21 of 35	

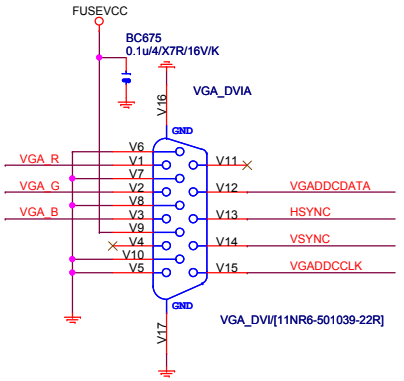












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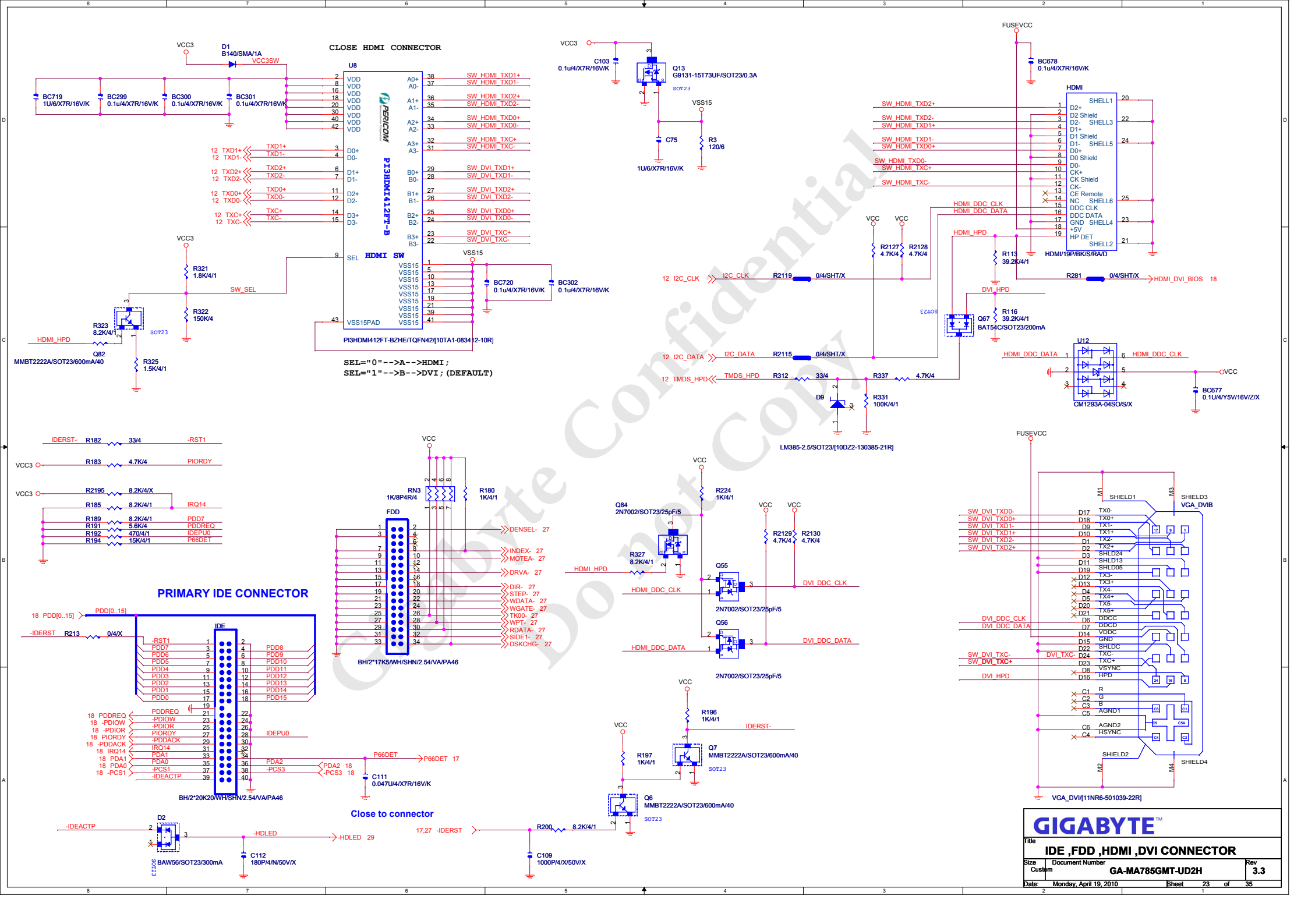
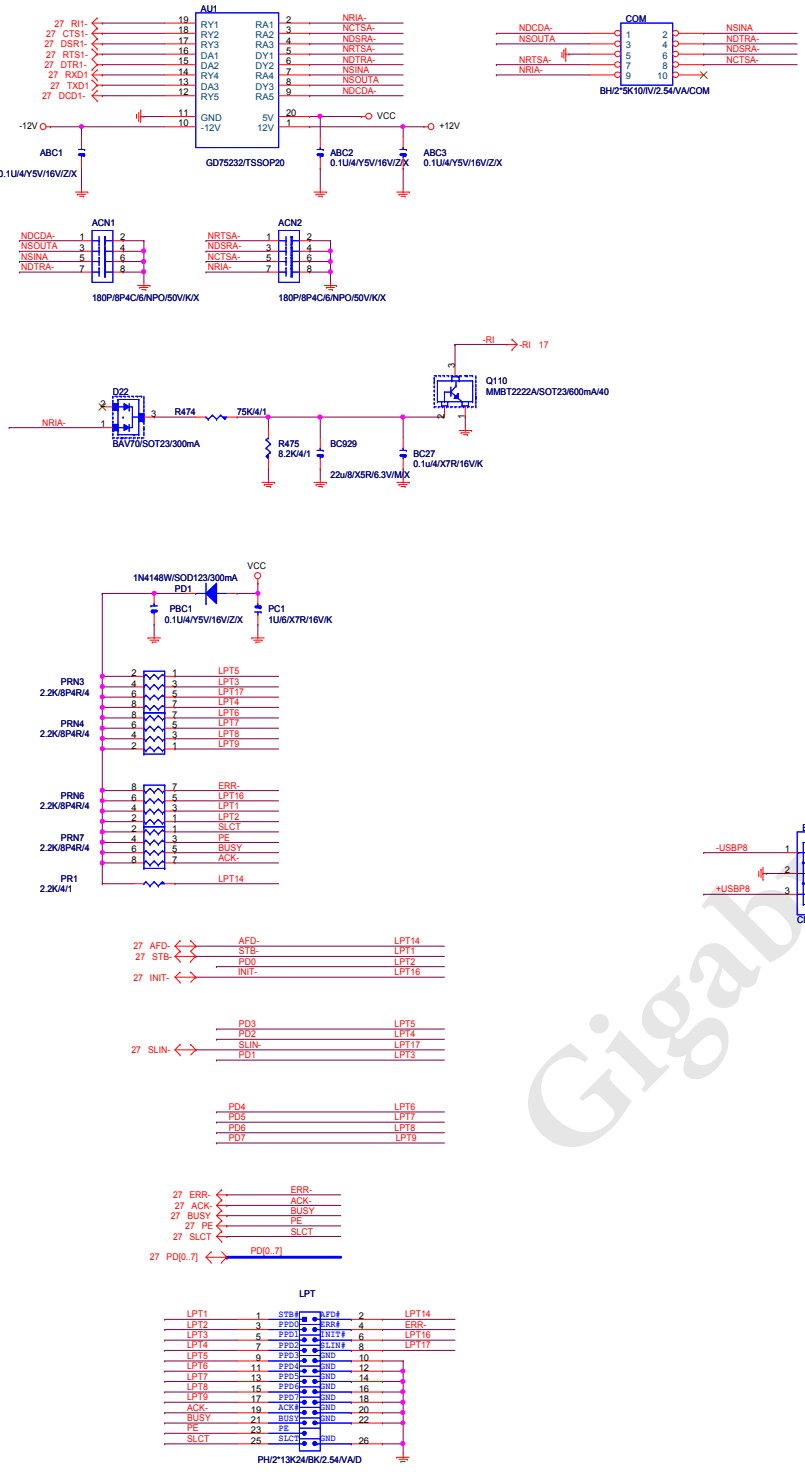
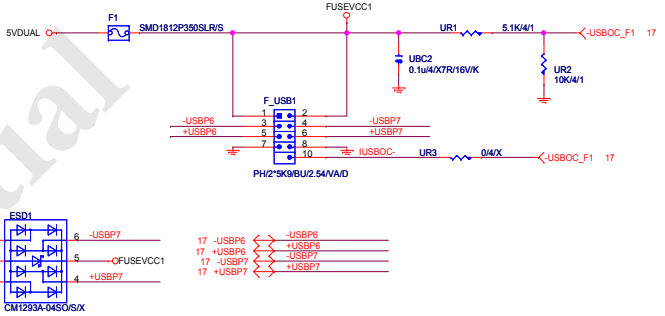
Title: RGB		
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 22 of 35	

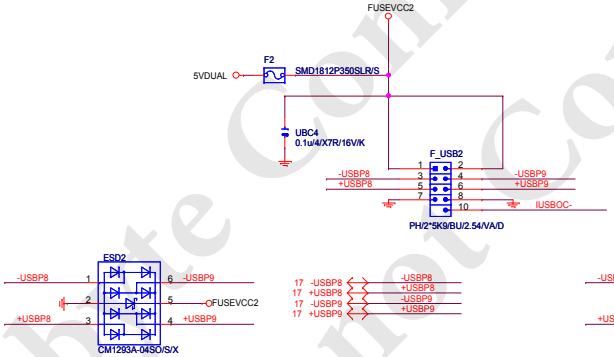




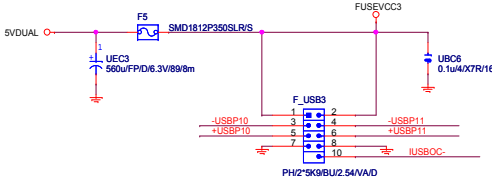
FRONT SIDE USB1

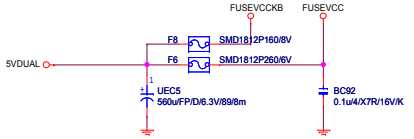


FRONT SIDE USB2



FRONT SIDE USB3





GIGABYTE		
Title: COM/LPT/F_USB		
Size: C	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
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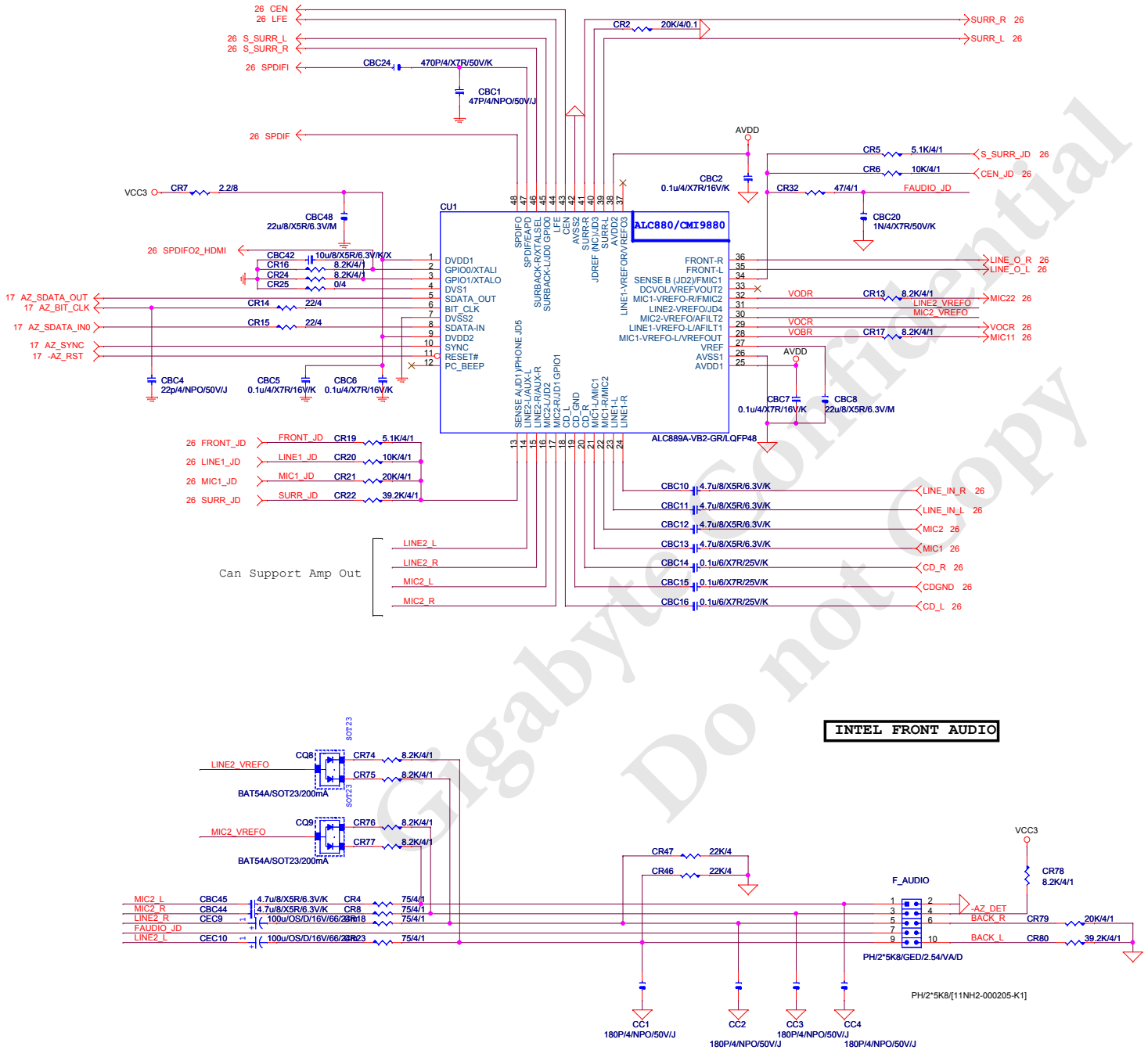

AZALIA CODEC *ALC892/ALC889A/ Colay*

	ALC892		ALC889A
CR16	X		O
CR24	X		O
CR25	X		O
CBC42	10uF/X5R		X
CR2	20K/1%		20K/0.1%
CR9	O		X
CR10	X		O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R		4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR28/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm		75 ohm

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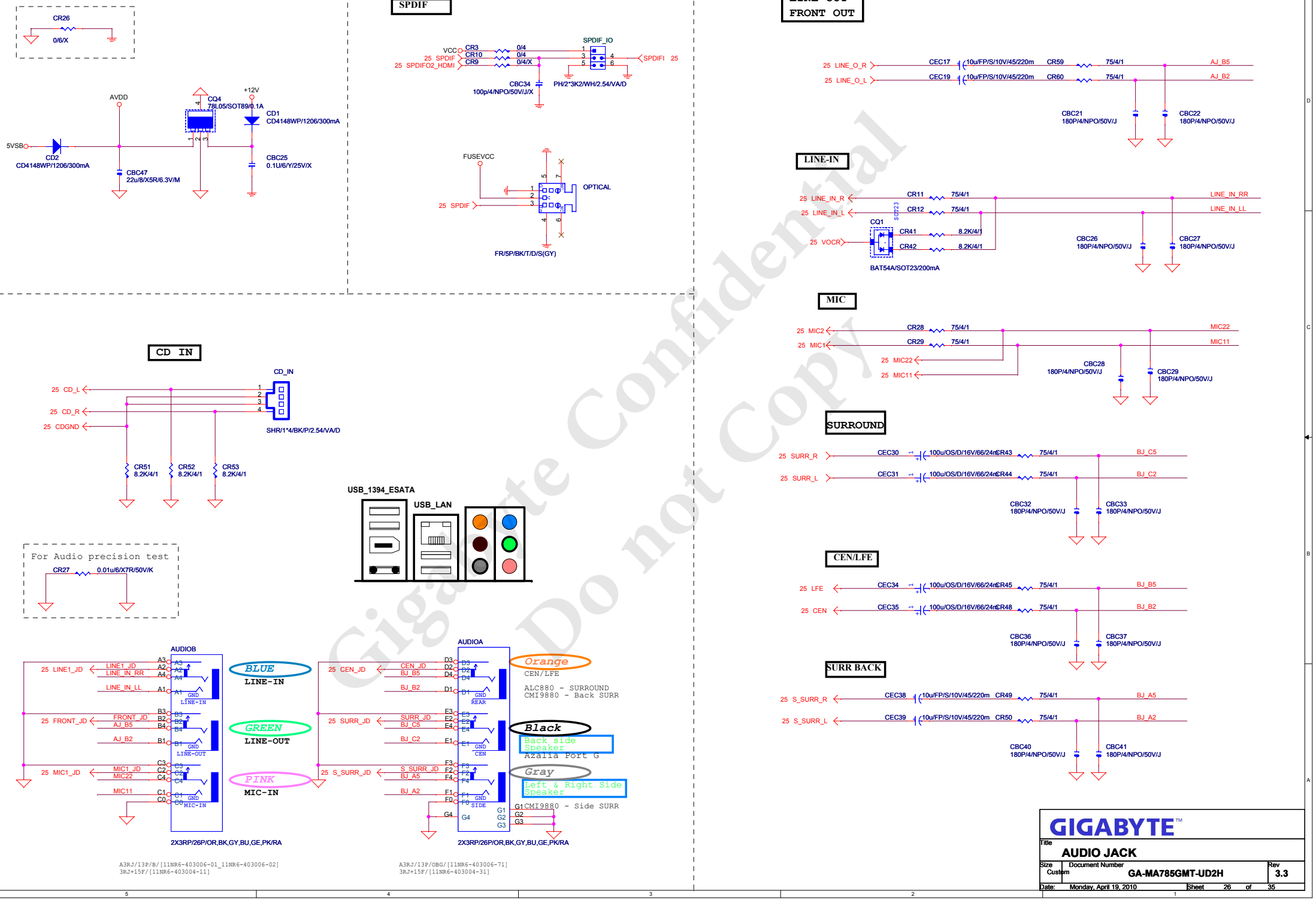
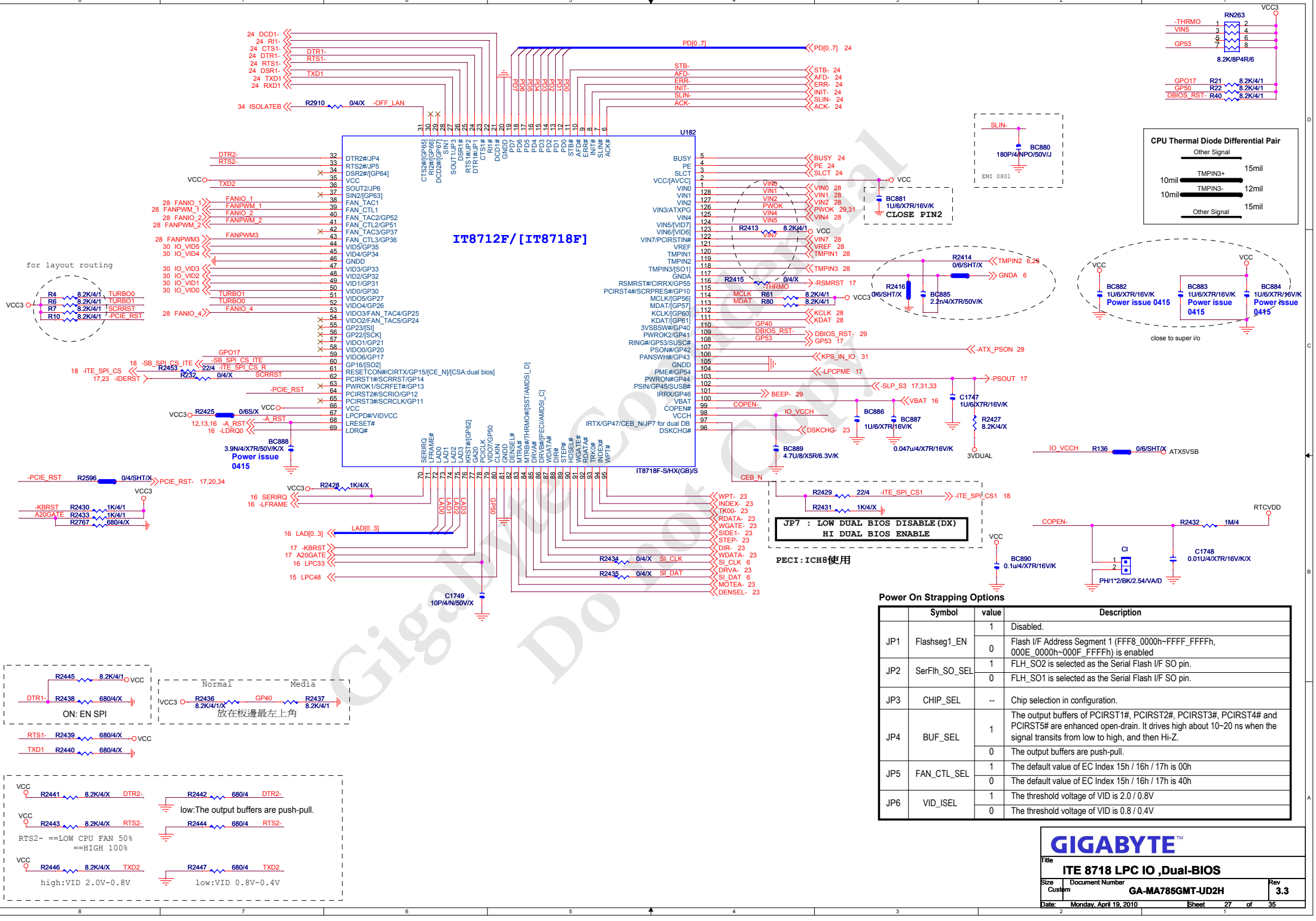
Title	ALC889A CODEC	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 25 of 35	





Power On Strapping Options

	Symbol	value	Description
JP1	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2	SerFlh_SO_SEL	1	FLH_SO2 is selected as the Serial Flash I/F SO pin.
		0	FLH_SO1 is selected as the Serial Flash I/F SO pin.
JP3	CHIP_SEL	--	Chip selection in configuration.
JP4	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# and PCIRST5# are enhanced open-drain. It drives high about 10~20 ns when the signal transits from low to high, and then Hi-Z.
		0	The output buffers are push-pull.
JP5	FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
		0	The default value of EC Index 15h / 16h / 17h is 40h
JP6	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V

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Title: ITE 8718 LPC IO ,Dual-BIOS

Size: Custom | Document Number: GA-MA785GMT-UD2H | Rev: 3.3

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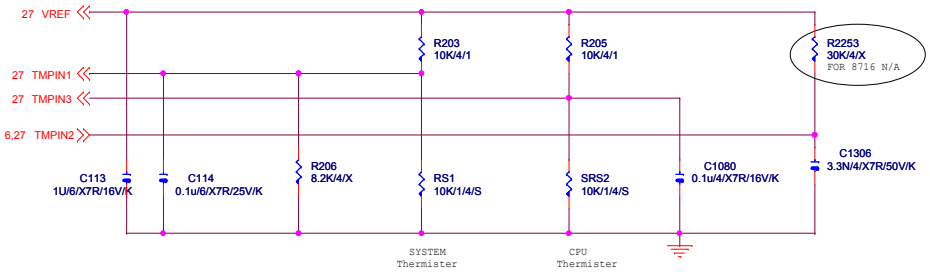
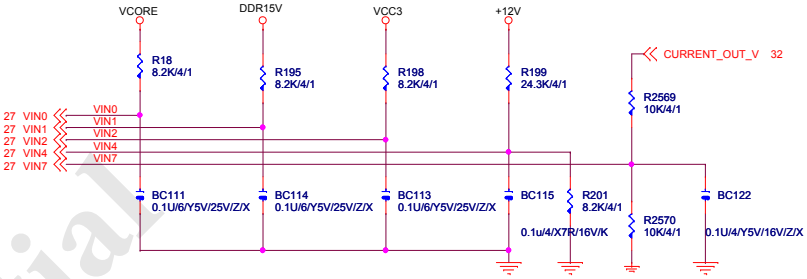
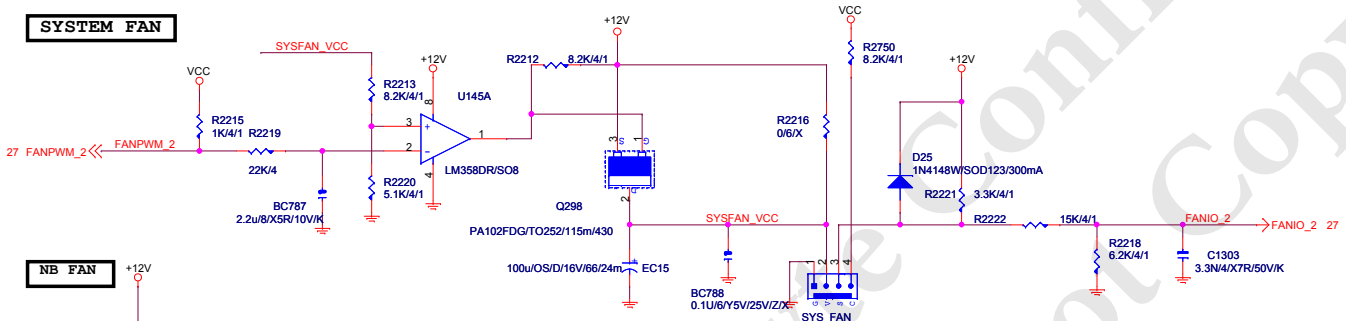
Hardware Monitor circuits

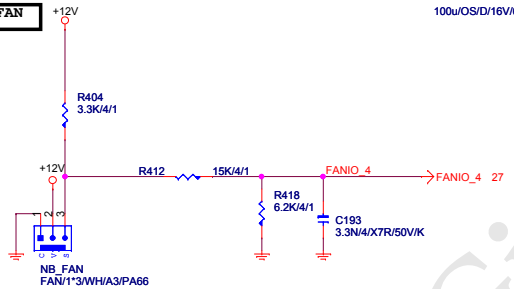




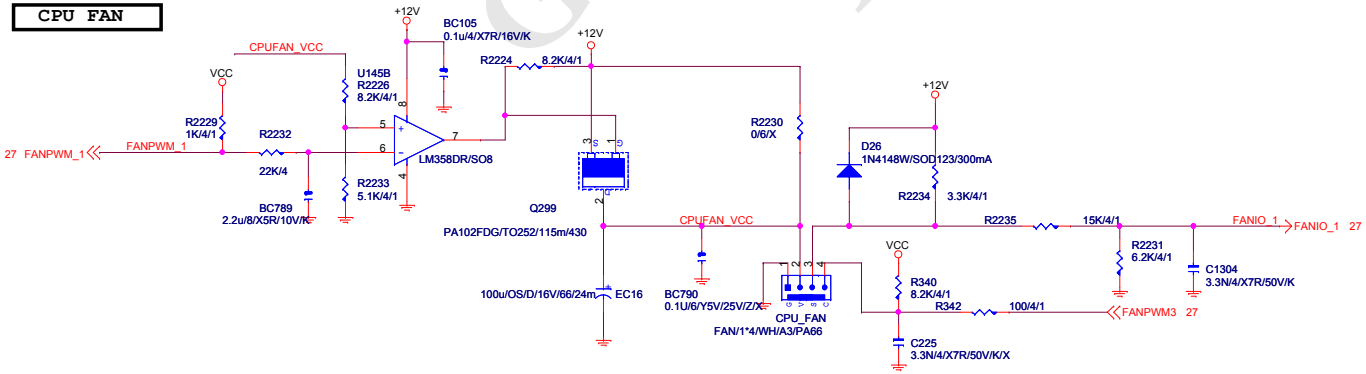
SYSTEM FAN



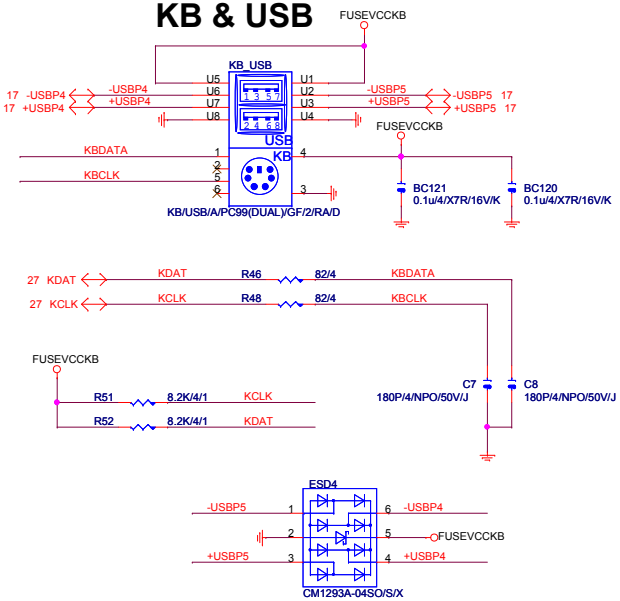
NB FAN



CPU FAN



KB & USB



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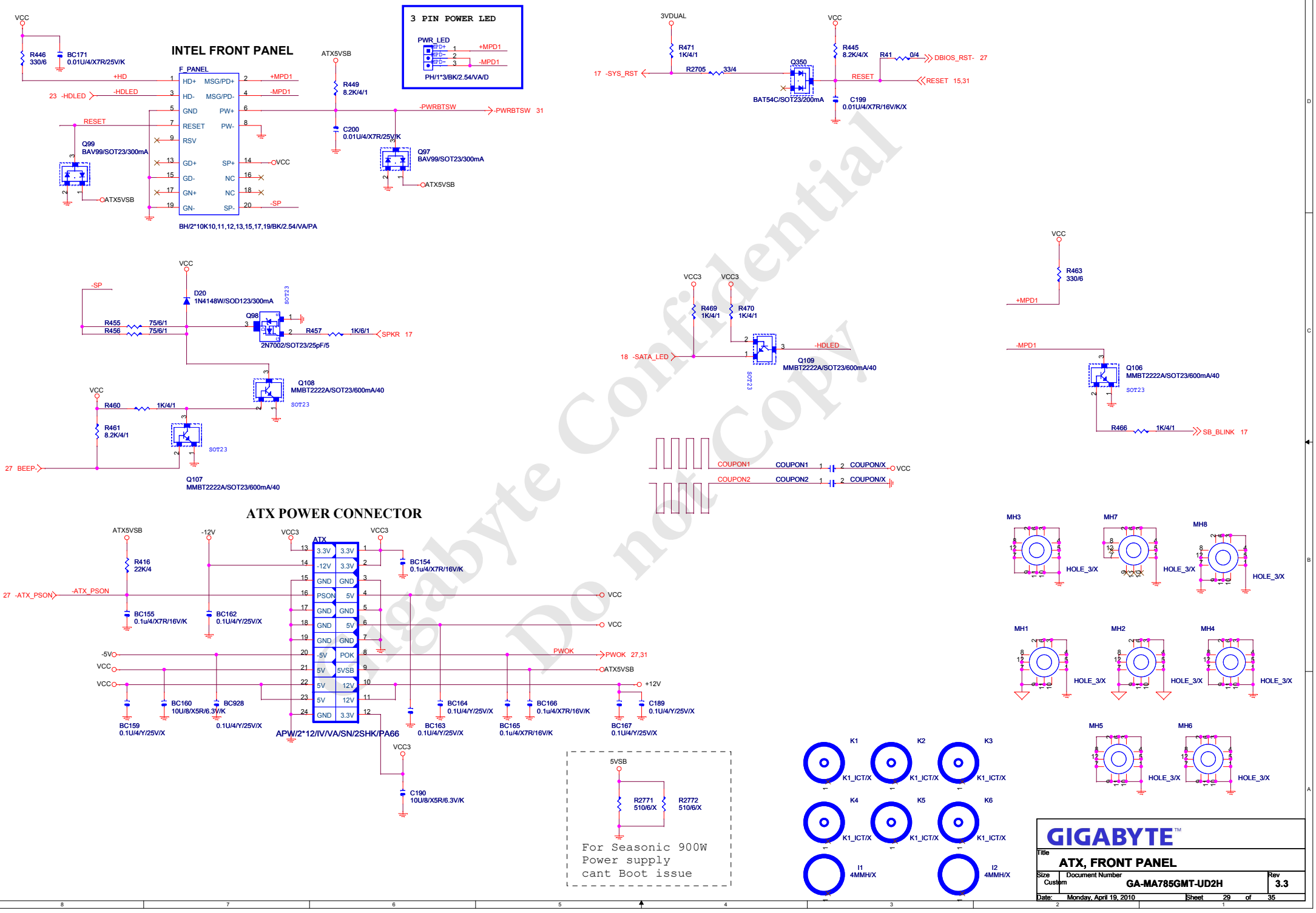
Title	FAN/HWMO KB/USB	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 28 of 35	


INTEL FRONT PANEL
F_PANEL
BH/2*10K10,11,12,13,15,17,19/BK/2.54/VA/PA
3 PIN POWER LED
PWR_LED
PH/1*3/BK/2.54/VA/D
ATX POWER CONNECTOR
APW/2*12/IV/VA/SN/2SHK/PA66
For Seasonic 900W
Power supply
cant Boot issue
GIGABYTE
ATX, FRONT PANEL
GA-MA785GMT-UD2H
Rev 3.3
Monday, April 19, 2010
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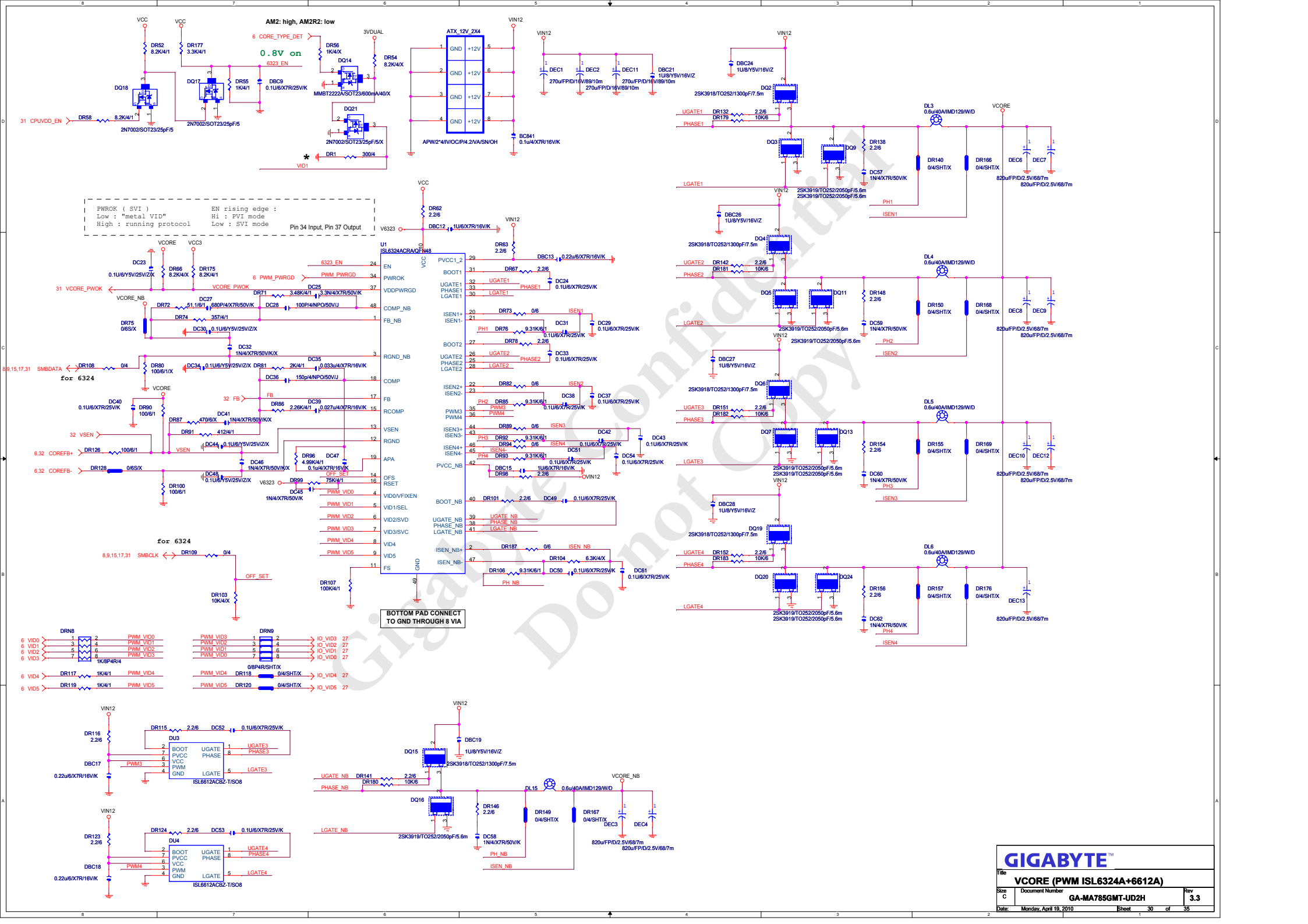

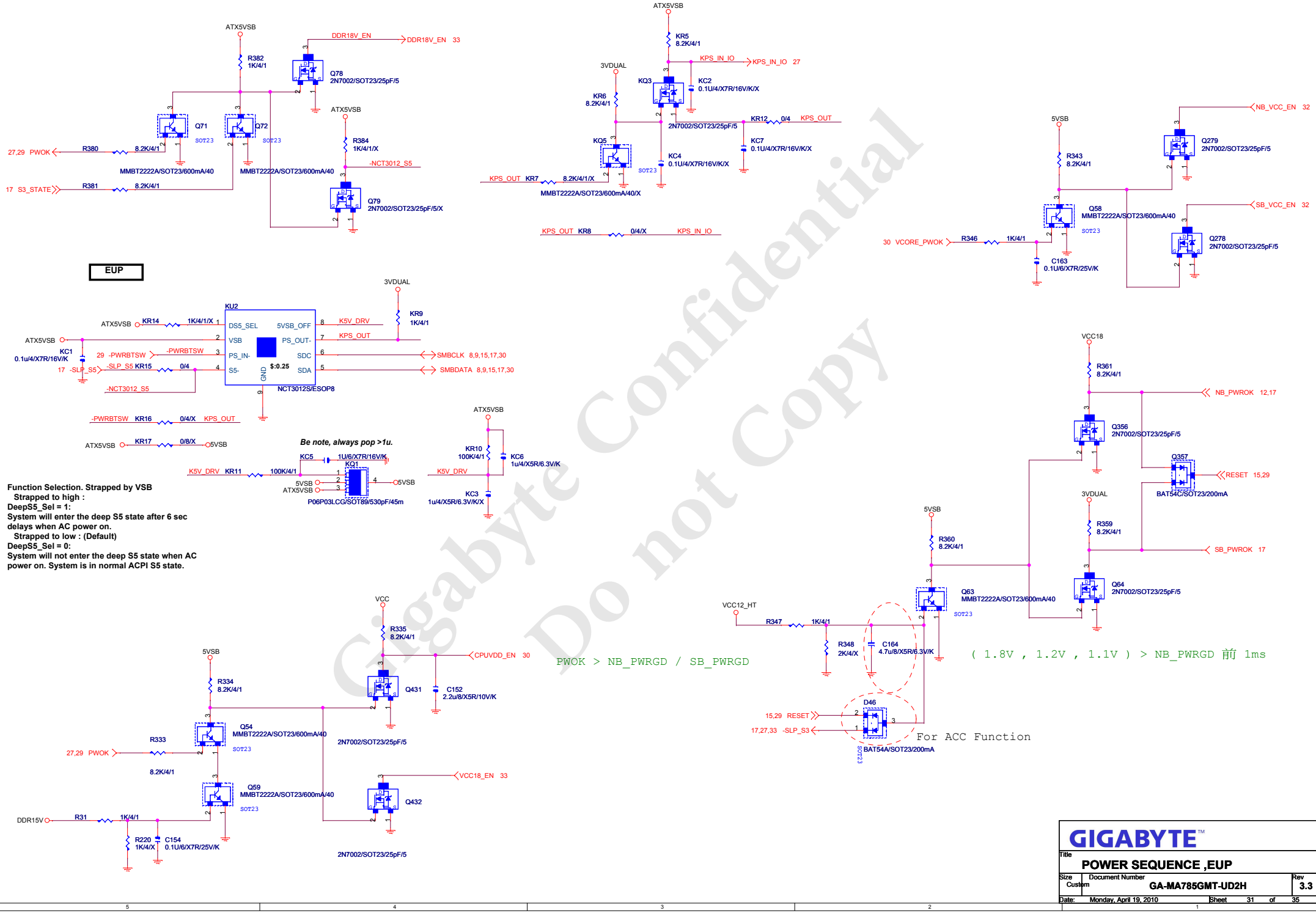

Function Selection. Strapped by VSB
Strapped to high :
DeepS5_Sel = 1:
System will enter the deep S5 state after 6 sec delays when AC power on.
Strapped to low : (Default)
DeepS5_Sel = 0:
System will not enter the deep S5 state when AC power on. System is in normal ACPI S5 state.

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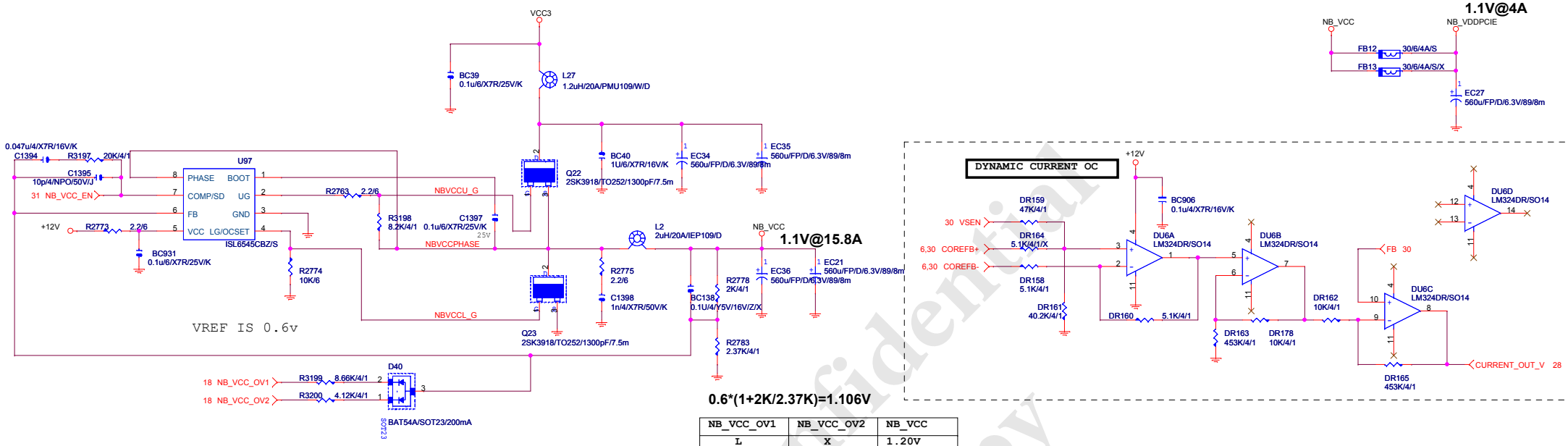
Title	POWER SEQUENCE ,EUP	
Size: Custom	Document Number: GA-MA785GMT-UD2H	Rev: 3.3
Date: Monday, April 19, 2010	Sheet 31 of 35	



NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V

VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

GIGABYTE™

Title: NB/SB POWER,VCC12HT,VDDA25,VCC12Dual

Size	Document Number	Rev
Custom	GA-MA785GMT-UD2H	3.3

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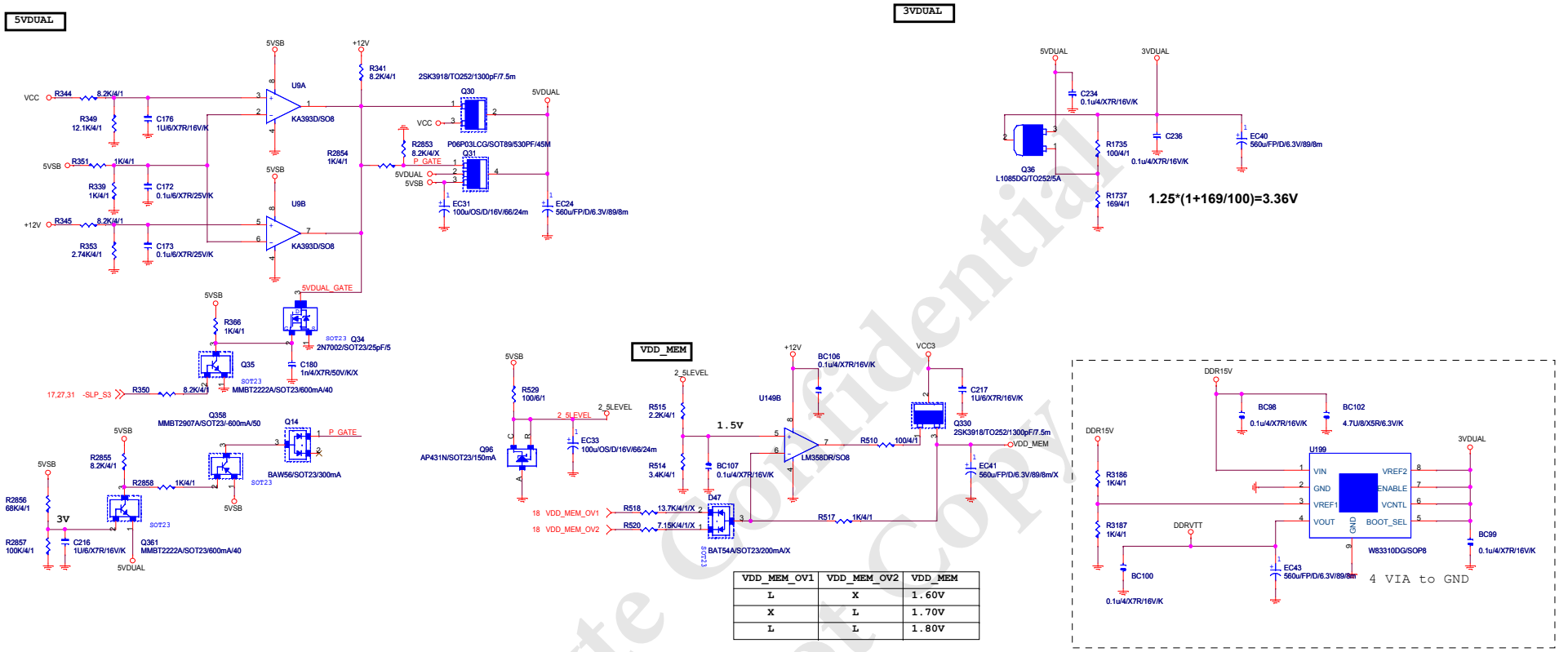
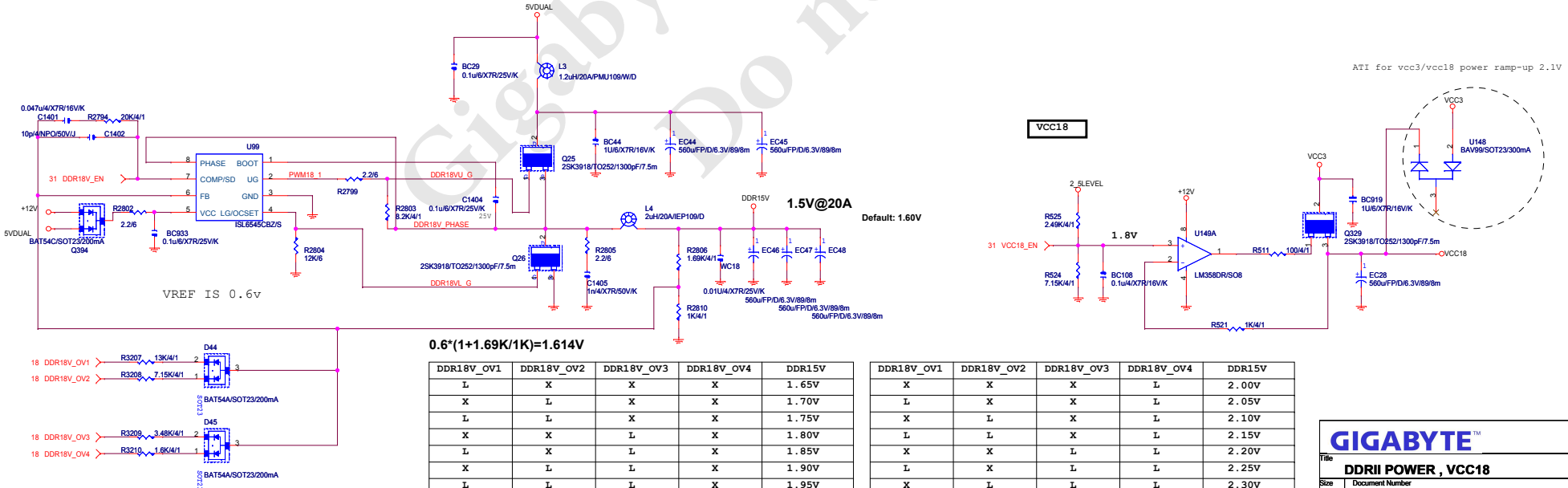


VDD_MEM_OV1	VDD_MEM_OV2	VDD_MEM
L	X	1.60V
X	L	1.70V
L	L	1.80V



DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
L	X	X	X	1.65V
X	L	X	X	1.70V
L	L	X	X	1.75V
X	X	L	X	1.80V
L	X	L	X	1.85V
X	L	L	X	1.90V
L	L	L	X	1.95V

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
X	X	X	L	2.00V
L	X	X	L	2.05V
X	L	X	L	2.10V
L	L	X	L	2.15V
X	X	L	L	2.20V
L	X	L	L	2.25V
X	L	L	L	2.30V
L	L	L	L	2.35V

GIGABYTE™

Title: DDRII POWER , VCC18

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PCIE-1G LAN

RTL8111C

LR36:
RTL8101E/8102E -->X
RTL8111C-->O

LR33:0/6 DISABLE SWICHING REG

LR16:
RTL8101E-->2K/4/1
RTL8111C/8102E-->2.49K/4/1

LU1

RTL8111C-VCO-GR/QFN64

Dual Color LED

Single Color LED

P35-152-19W9

CLOSE LAN CHIP

LL1/LFB10 CO-LAYOUT CLOSE

CHOKE4U7-500MA

LL1/LBC64/LBC63
CLOSE LU1 PIN1

RTL8102E LFB7-->X

FOR 93C46 OR BIOS DETECT
RTL8102E -->X

USB_LAN CONNECTOR

RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8102E:LC5/LC6-->O
RTL8111C:LC6-->O

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1

RTL8102E -->X

CLOSE LAN CHIP

LC6:
100M:0.1U
1G:0.01U

USB_LAN

USB+LAN/1G/GO,Y/OS/RA/D/8C

EC要靠近USB_PORT的FUSEVCC

USB_LAN

CM1293A-04SO/S/X

GIGABYTE

Title: REALTK RTL8111C/8101E

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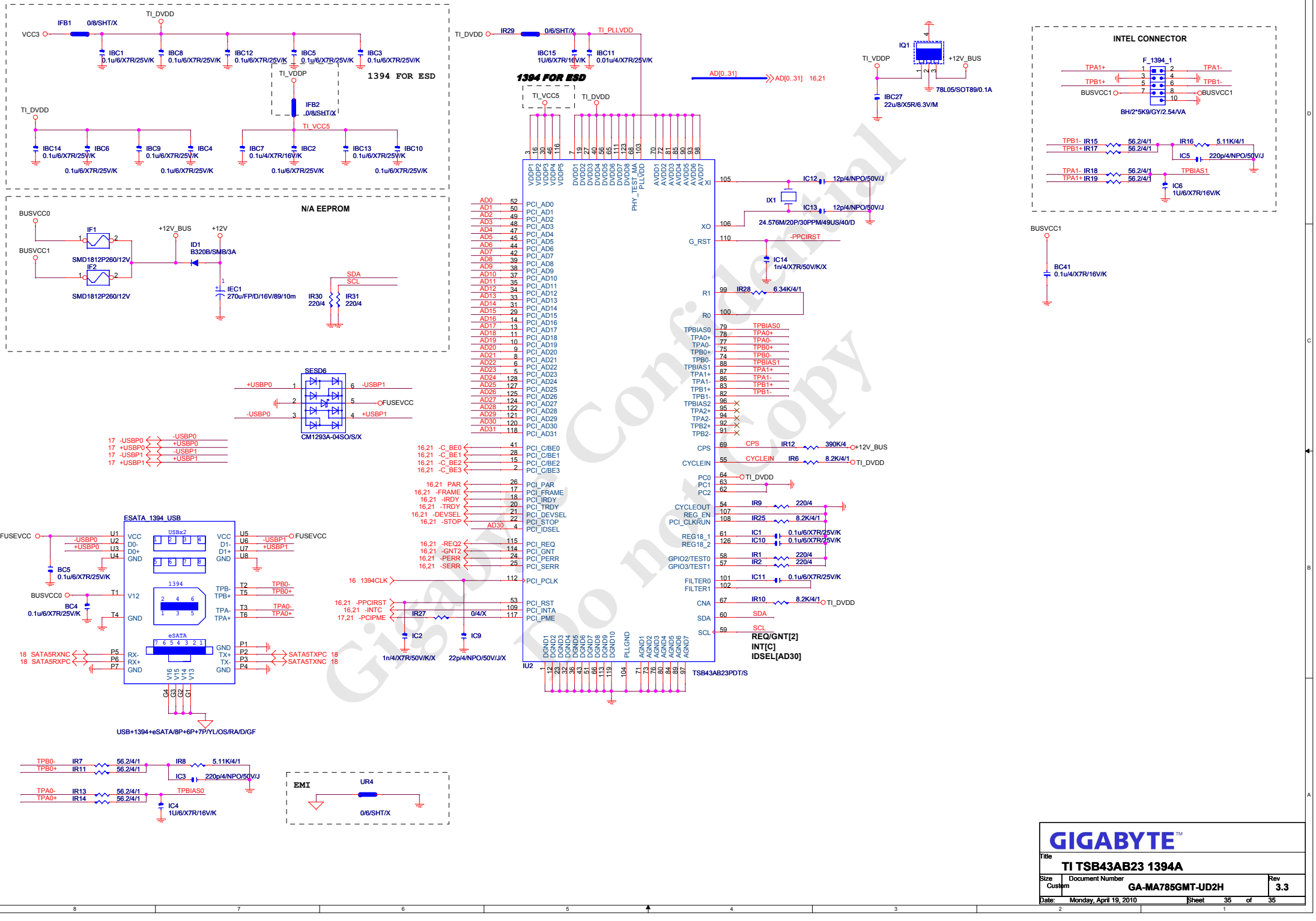

Title	TI TSB43AB23 1394A		
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