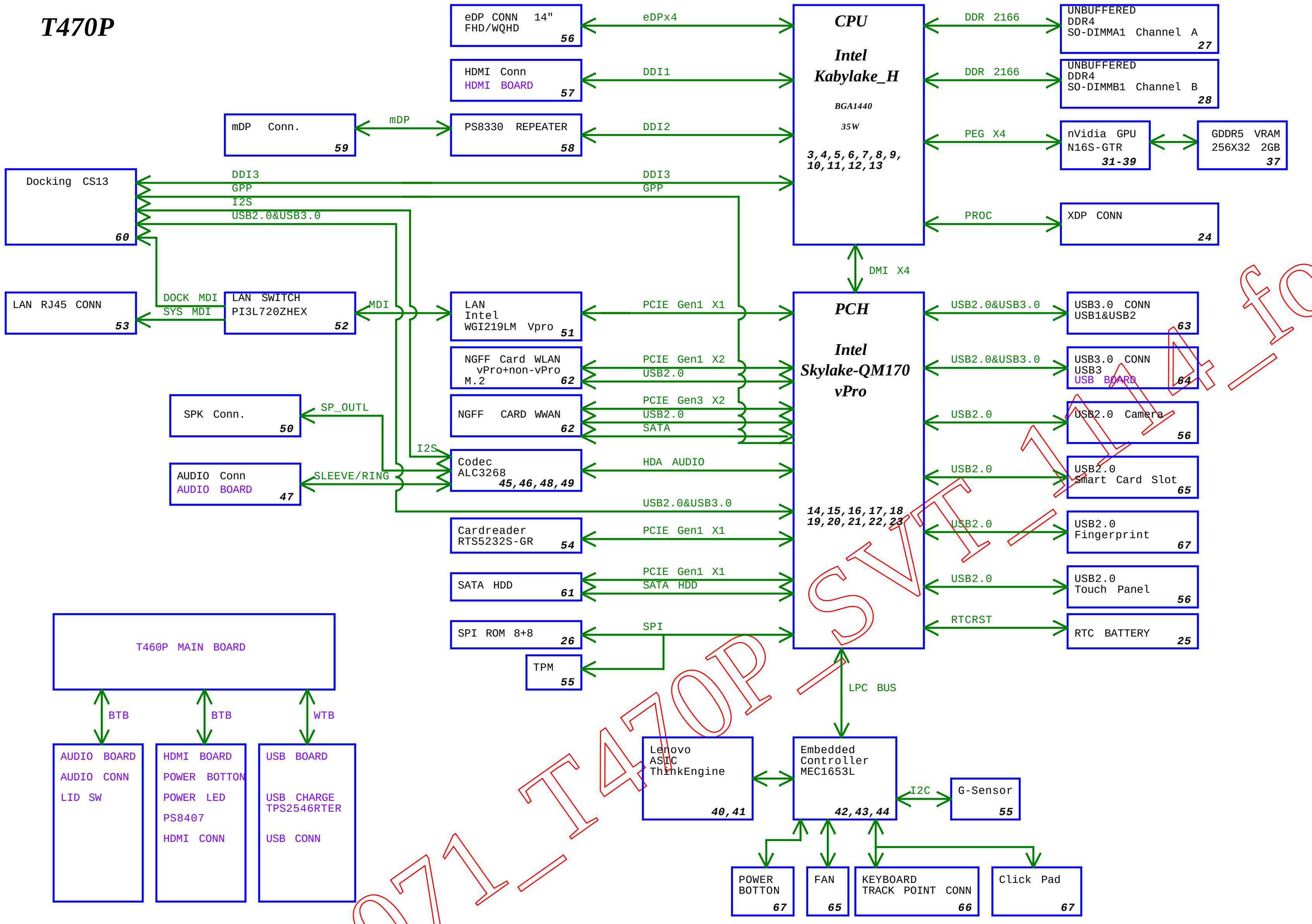
T470P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mDP
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BGA1440
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AUDIO Conn
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RTC BATTERY 25
TPM 55
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BTB
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AUDIO BOARD
AUDIO CONN
LID SW
HDMI BOARD
POWER BOTTON
POWER LED
PS8407
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TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
G1	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	Suspend-to-RAM (STR)
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	
	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	Suspend-to-Disk (STD)
	Deep S4	M-OFF	ON	ON	OFF	OFF	ON	OFF		
G2	S5	M3	ON	ON	ON	ON	OFF	OFF	Hibernation or Shutdown	Soft Off
	Deep S5	M-OFF	ON	ON	OFF	OFF	ON	OFF		
	S5 EC OFF	M-OFF	ON	OFF	OFF	OFF	OFF	OFF		
G3	---	---	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical Off

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b

EC SMBus1 address

Device	Address
G-Senor (LIS3DH)	0011 000Xb
G-Senor (KX023)	0011 110Xb

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

Device		Address
CH-A	DDR DIMM1	1001 0000b
CH-B	DDR DIMM2	1001 0010b

PCH SM Bus0 address

Device	Address
Intel Lan_I219	0XC8

Schematics Mark Definition

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX

- Tolerance
- Temperature Characteristics
- Rated Voltage
- Package Size

Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NPO	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SL	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+-0.05PF	+-0.1PF	+-0.25PF	+-0.5PF	+-1%	+-2%	+-3%	+-5%	+-10%	+-20%	+-30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100, -0%	+30, -10%	+20, -10%	+40, -20%	+80, -20%	+50, -20%	-30% ~ 10%

ZZZ1 PCB@
DT473
DAZ13700100

UL5101 NVPRO@
S IC WGI219V SLKJ4 A0 QFN LAN PHY 01!
SA000072Z10

UC1 SR32S@
CL8067702870309 SR32S
SA000087220

UC1 SR32R@
CL8067702870214 SR32R
SA000087110

BOM Structure Table

BOM Structure	NOTE
DEBUG@	For EE DEBUG
DPRE@	DP re-driver function
NODPRE@	Disable DP re-driver
GC6@	For GC6 function
NGC6@	NON GC6 function
ME@	ME Connector
EMC@	For EMI Solution
RF@	For RF Solution
VSE2G@	For SAMSUNG VRAM Setting
VME2G@	For Micron VRAM Setting
VHC2G@	For RF HYNIX VRAM Setting
X76_VSE2G@	K4W4G1646E-BC1A x4 + 24.9K
X76_VME2G@	MT41J256M16HA-093G x4 +10k
X76_VHC2G@	H5TC4G63CFR-N0C x4 +30.1k
CS@	For CURRENT SENSE
UMA@	For UMA
DIS@	For DIS
UC1@	For CPU

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Title: EC HISTORY

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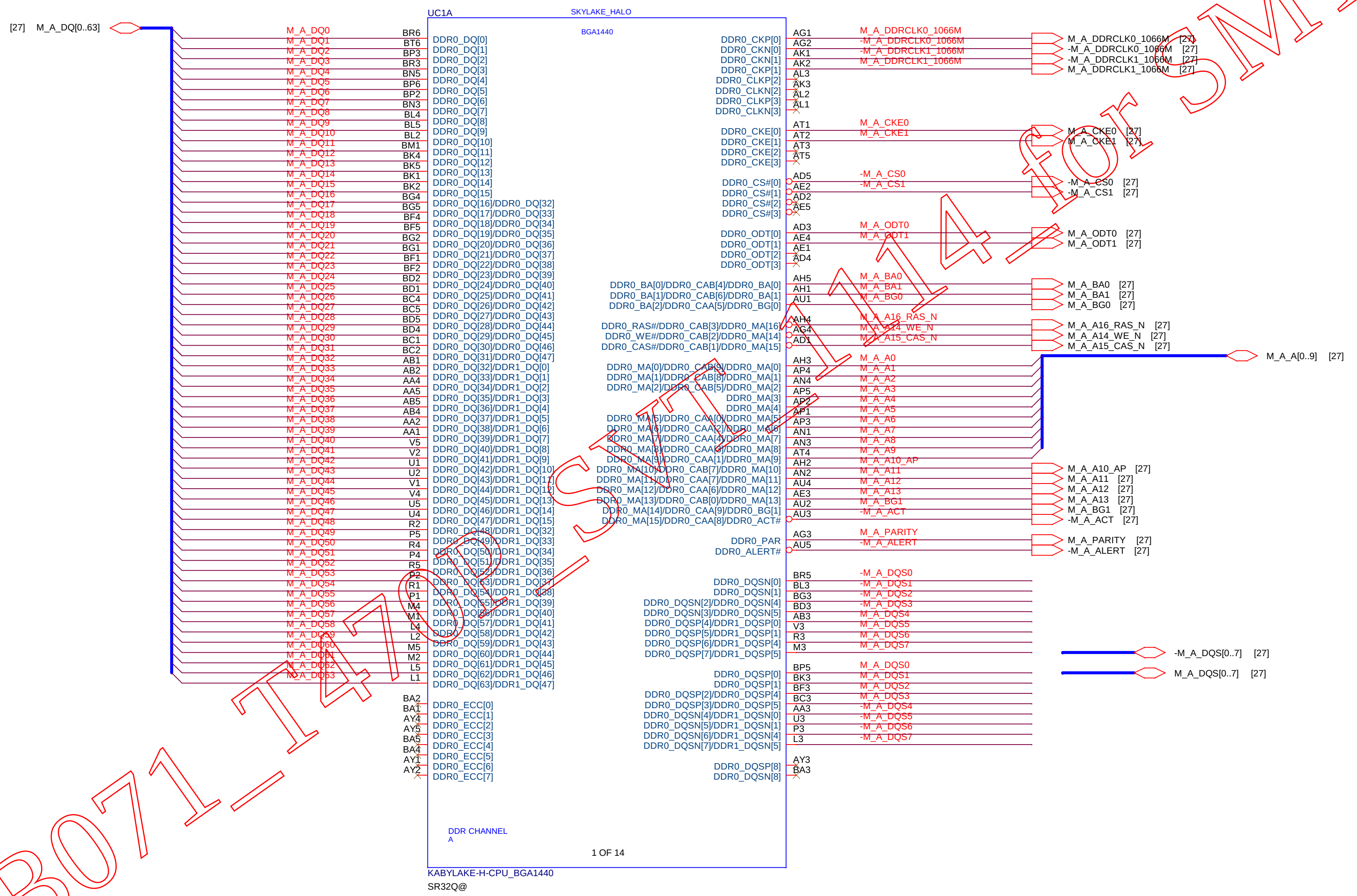

DDR4 INTERLEAVE IMPLEMENTATION

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Title		
CPU KBL-H : DDR4 CH-A		
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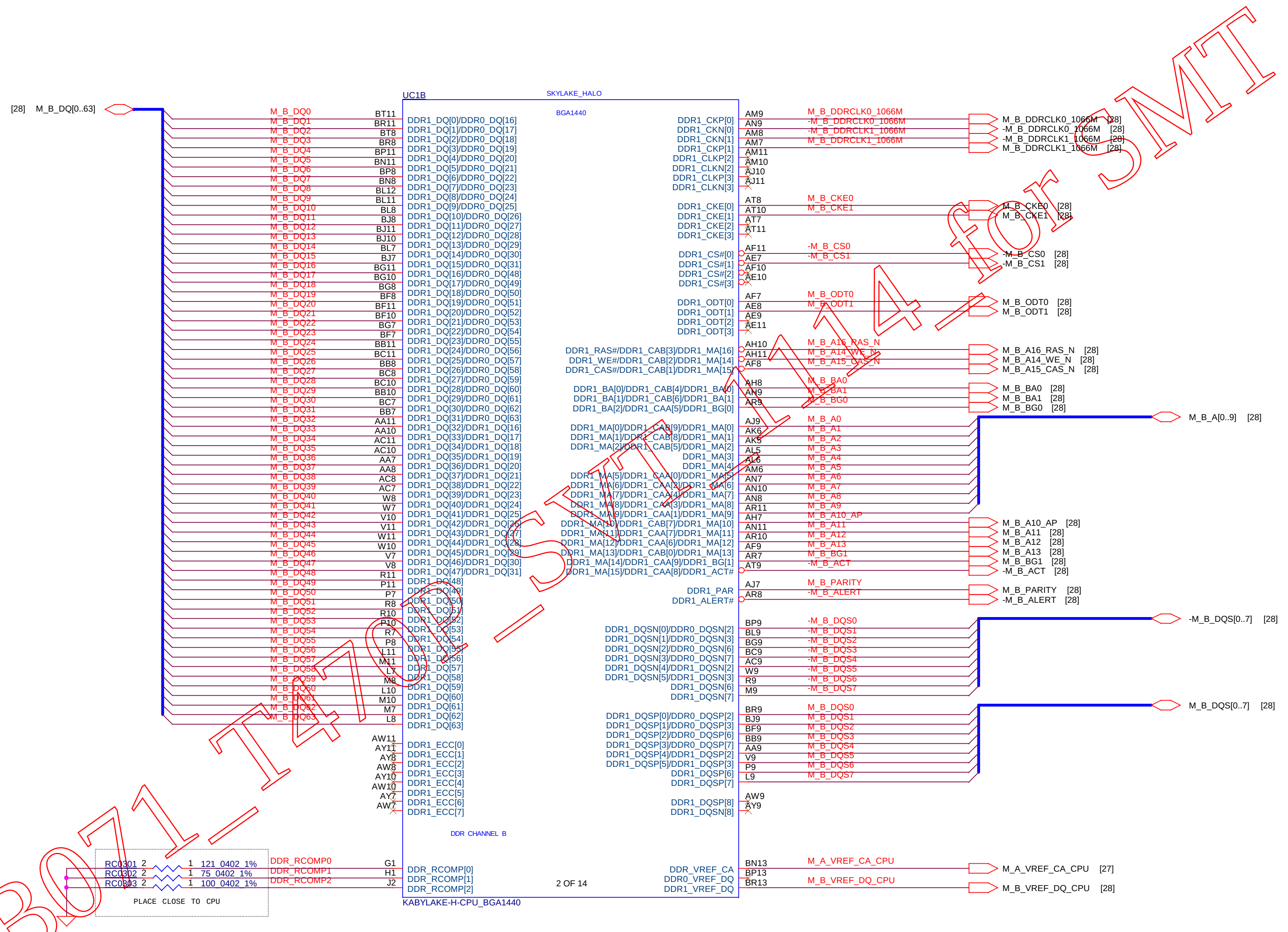

DDR_VREF_CA : Connected to VREF_CA on DIMM CH-A
DDR0_VREF_DQ : NC
DDR1_VREF_DQ : Connected to VREF_CA on DIMM CH-B

Security Classification	LC Future Center Secret Data		
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Title: CPU KBL-H : DDR4 CH-B

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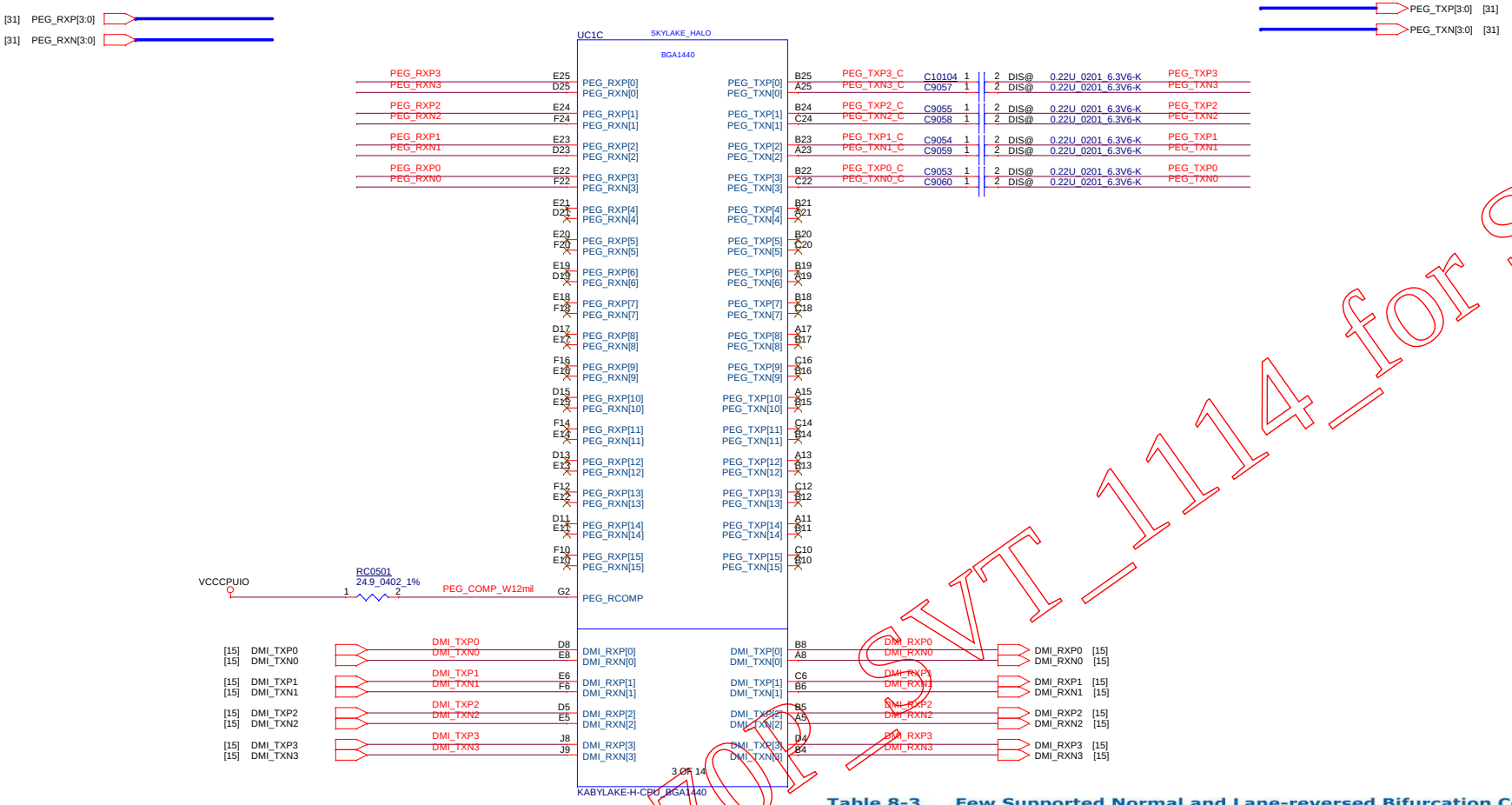

Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Pro-cessor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

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Title			
CPU KBL-H : PEG/DMI			
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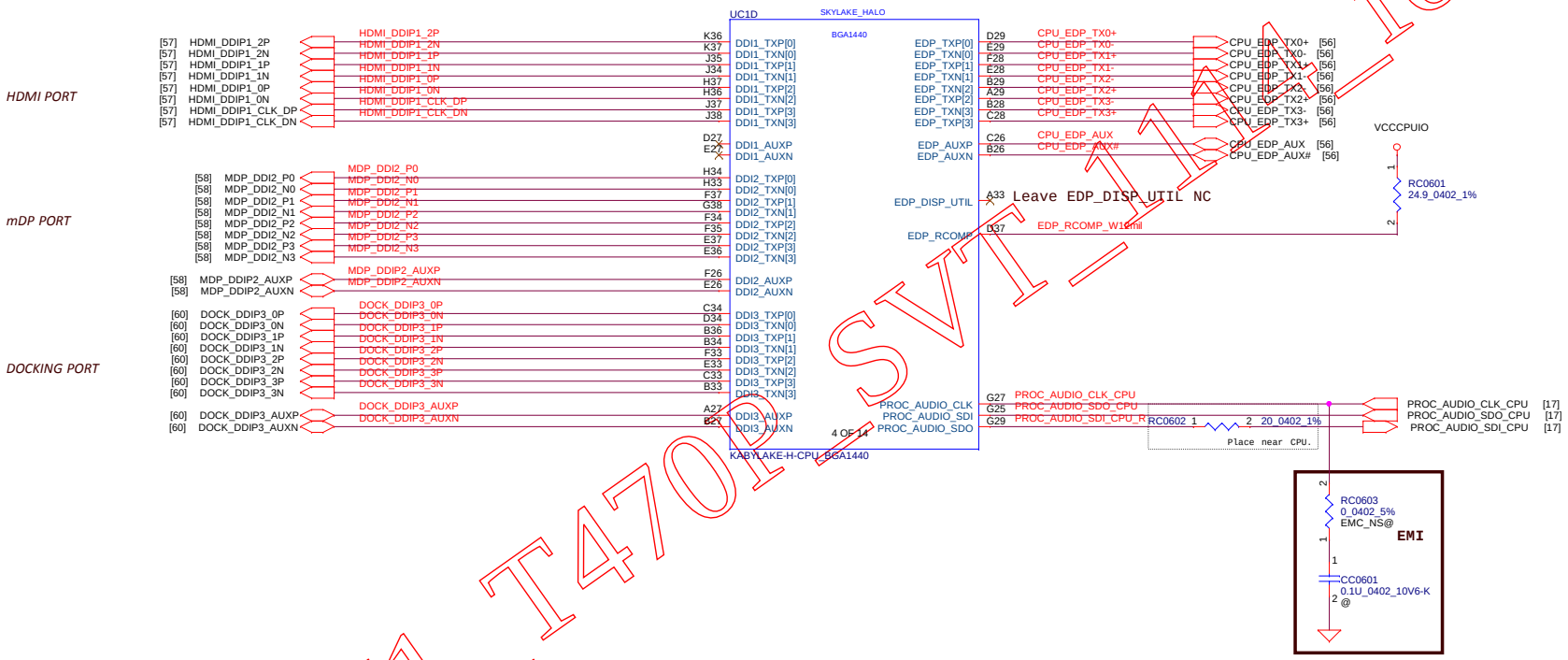

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Title: CPU KBL-H : DDI/EDP

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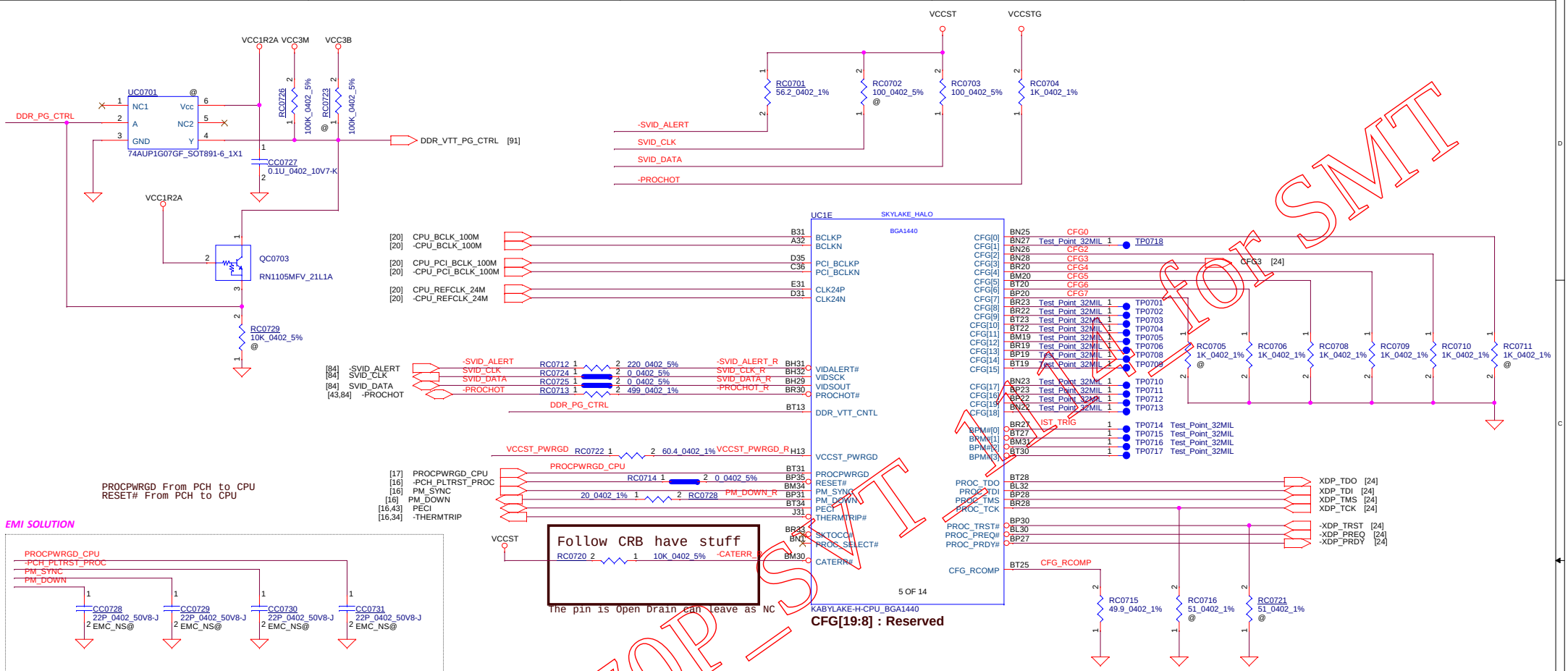

TABLE CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:
1 : No Stall <---------- LOGIC
0 : Stall

CFG[2] : PEG Static Lane Reversal
1 : Normal Operation
0 : Lane Reversal <---------- LOGIC

CFG[4] : eDP enable
1 : Disabled
0 : Enabled <---------- LOGIC

CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:2(CONFIRM BIOS)
00 : 1x4 <---------- LOGIC

CFG[7] : PEG Training(CONFIRM BIOS)
1 : PEG Train immediately following RESET# deassertion <---------- LOGIC
0 : PEG Wait for BIOS for training

CFG[19:8] : Reserved

For x16 Reversal Lanes - CFG[6/5/2] setting is 110
For x4 Reversal Lanes - CFG[6/5/2] setting is 000
For x4 Normal Lanes - CFG[6/5/2] setting is 001

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title	CPU KBL-H : MISC/CLK/JTAG/CFG		
Size	Document Number		Rev
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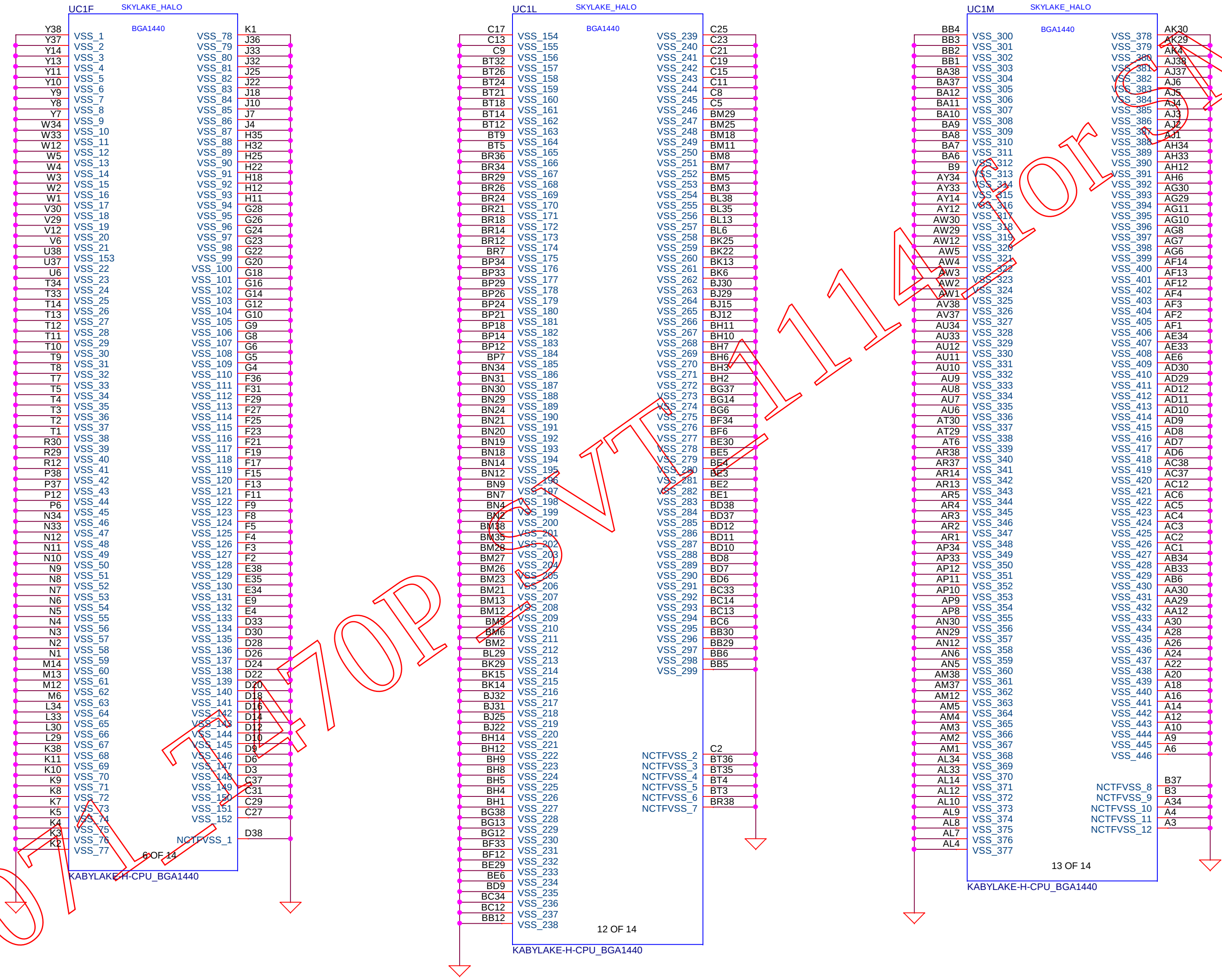
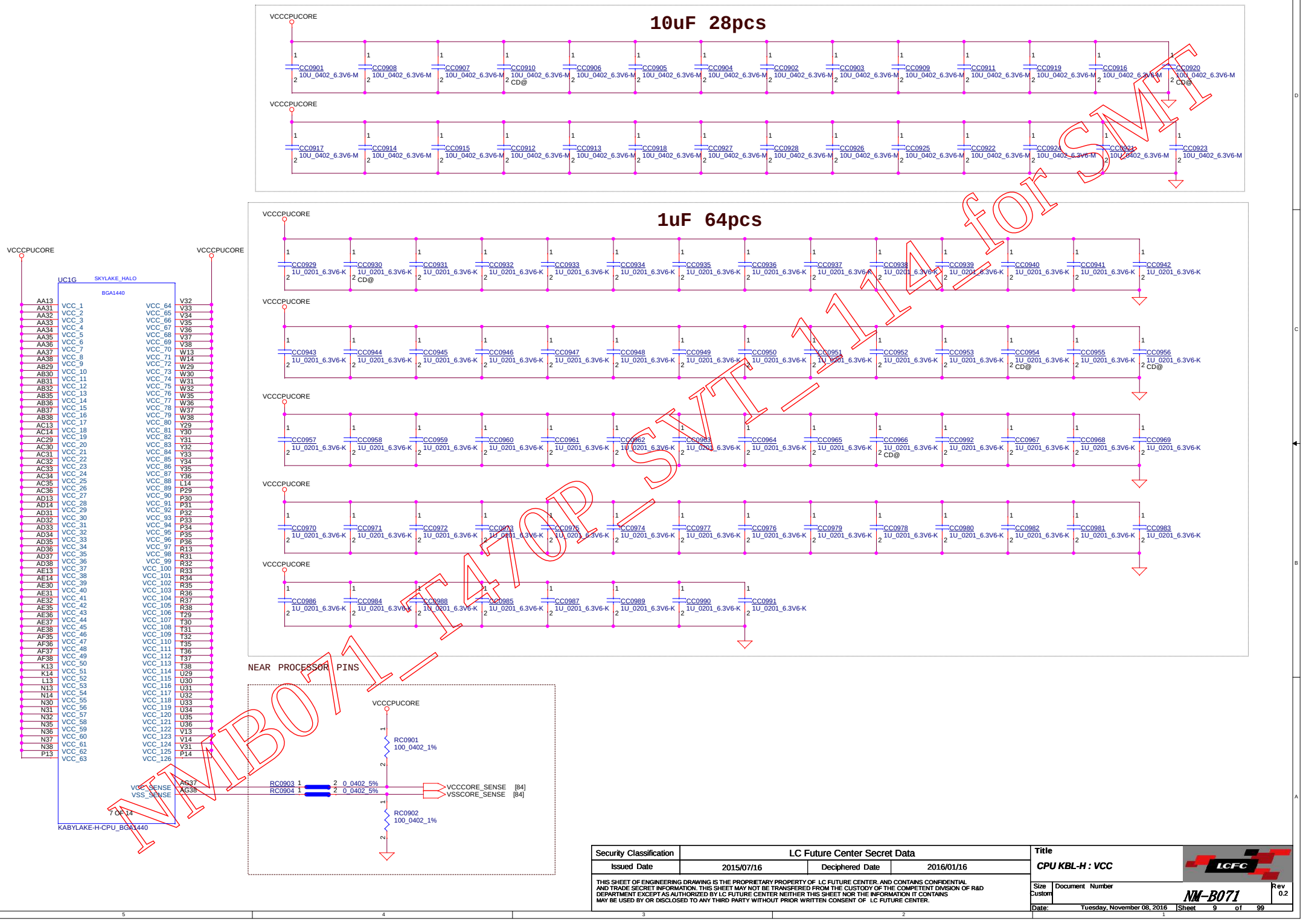


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: CPU KBL-H : GND

Size: Custom | Document Number: NM-B071 | Rev: 0.2

Date: Tuesday, November 08, 2016 |



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Title: CPU KBL-H : VCC

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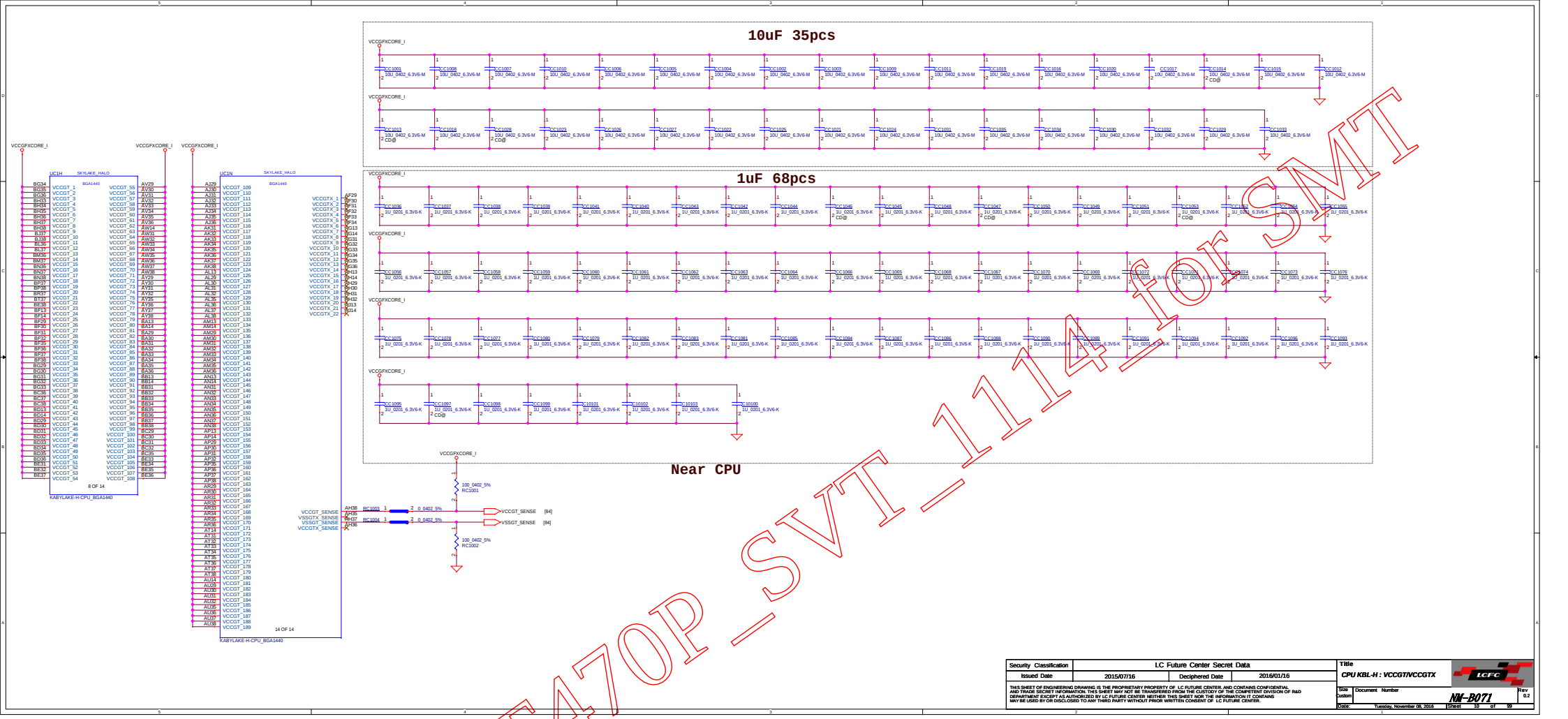

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Title	CPU KBL-H : VCCGT/VCCGTX		
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VCCSA DECOUPLING

VCCSA

10uF 7pcs

CC1125 10U_0402_6.3V6-M
CC1130 10U_0402_6.3V6-M
CC1129 10U_0402_6.3V6-M
CC1131 10U_0402_6.3V6-M
CC1128 10U_0402_6.3V6-M
CC1127 10U_0402_6.3V6-M
CC1126 10U_0402_6.3V6-M

VCCSA

1uF 3pcs

CC1133 1U_0402_6.3V6-K
CC1132 1U_0402_6.3V6-K
CC1134 1U_0402_6.3V6-K

VDDQ DECOUPLING

VCC1R2A

10uF 10pcs

CC1111 10U_0402_6.3V6-M
CC1112 10U_0402_6.3V6-M
CC1113 10U_0402_6.3V6-M
CC1114 10U_0402_6.3V6-M
CC1115 10U_0402_6.3V6-M
CC1116 10U_0402_6.3V6-M
CC1117 10U_0402_6.3V6-M
CC1118 10U_0402_6.3V6-M
CC1119 10U_0402_6.3V6-M
CC1120 10U_0402_6.3V6-M

VCC1R2A

22uF 4pcs

CC1121 22U_0603_6.3V6M
CC1122 22U_0603_6.3V6M
CC1123 22U_0603_6.3V6M
CC1124 22U_0603_6.3V6M

VCCSA
VCC1R2A

UC1I SKYLAKE_HALO BGA1440

VCCSA_1 J30
VCCSA_2 K29
VCCSA_3 K30
VCCSA_4 K31
VCCSA_5 K32
VCCSA_6 K33
VCCSA_7 K34
VCCSA_8 K35
VCCSA_9 L31
VCCSA_10 L32
VCCSA_11 L35
VCCSA_12 L36
VCCSA_13 L37
VCCSA_14 L38
VCCSA_15 M29
VCCSA_16 M30
VCCSA_17 M31
VCCSA_18 M32
VCCSA_19 M33
VCCSA_20 M34
VCCSA_21 M35
VCCSA_22 M36

VDDQ_1 AA6
VDDQ_2 AE12
VDDQ_3 AF5
VDDQ_4 AF6
VDDQ_5 AG5
VDDQ_6 AG9
VDDQ_7 AJ12
VDDQ_8 AL11
VDDQ_9 AP6
VDDQ_10 AP7
VDDQ_11 AR12
VDDQ_12 AR6
VDDQ_13 AT12
VDDQ_14 AW6
VDDQ_15 AY6
VDDQ_16 J5
VDDQ_17 J6
VDDQ_18 K12
VDDQ_19 K6
VDDQ_20 L12
VDDQ_21 L6
VDDQ_22 R6
VDDQ_23 T6
VDDQ_24 W6

VDDQC Y12
VCCPLL_OC_1 BH13
VCCPLL_OC_2 G11
VCCST H30
VCCSTG_1 H29
VCCSTG_2 G30
VCCPLL_1 H28
VCCPLL_2 J28
VCCSA_SENSE M38
VSSSA_SENSE M37
VCCIO_SENSE H14
VSSIO_SENSE J14

VCCIO_1 AG12
VCCIO_2 G15
VCCIO_3 G17
VCCIO_4 G19
VCCIO_5 G21
VCCIO_6 H15
VCCIO_7 H16
VCCIO_8 H17
VCCIO_9 H19
VCCIO_10 H20
VCCIO_11 H21
VCCIO_12 H26
VCCIO_13 H27
VCCIO_14 J15
VCCIO_15 J16
VCCIO_16 J17
VCCIO_17 J19
VCCIO_18 J20
VCCIO_19 J21
VCCIO_20 J26
VCCIO_21 J27

9 OF 14
KABYLAKE-H-CPU_BGA1440

VDDQC : Memory Control Clock Power
VCCPLL_OC : CPU digital PLL power rails

VCCPCPUIO

CC1108 10U_0603_6.3V6-M
CC1109 10U_0603_6.3V6-M
CC1110 10U_0603_6.3V6-M

VCC1R2A

CC1107 10U_0603_6.3V6-M
CC1105 1U_0402_6.3V6-K
CC1106 1U_0402_6.3V6-K

VCCST

CC1101 1U_0402_6.3V6-K
CC1102 1U_0402_6.3V6-K
CC1103 1U_0402_6.3V6-K

VCCSTG

RC1115 0_0402_5%
RC1116 0_0402_5%

VCCPCPUIO
VCCSA

RC1111 100_0402_1%
RC1112 100_0402_1%
RC1113 100_0402_1%
RC1114 100_0402_1%

VCCSA_SENSE [84]
VSSSA_SENSE [84]
VCCPCPUIO_SENSE [89]
VSSCPUIO_SENSE [89]

RESISTORS CLOSE TO CPU PINS

VCCST

CC1104 1U_0402_6.3V6-K

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Title: CPU KBL-H : VCCSA/VCCIO/VDDQ

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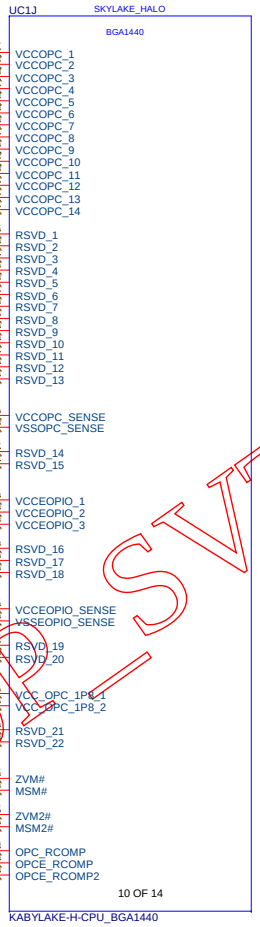

OPC_RCOM Support 4+4e
If not use can't conector

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Title: **CPU KBL-H : VCCOPC/RSVD**

Size	Document Number	Rev
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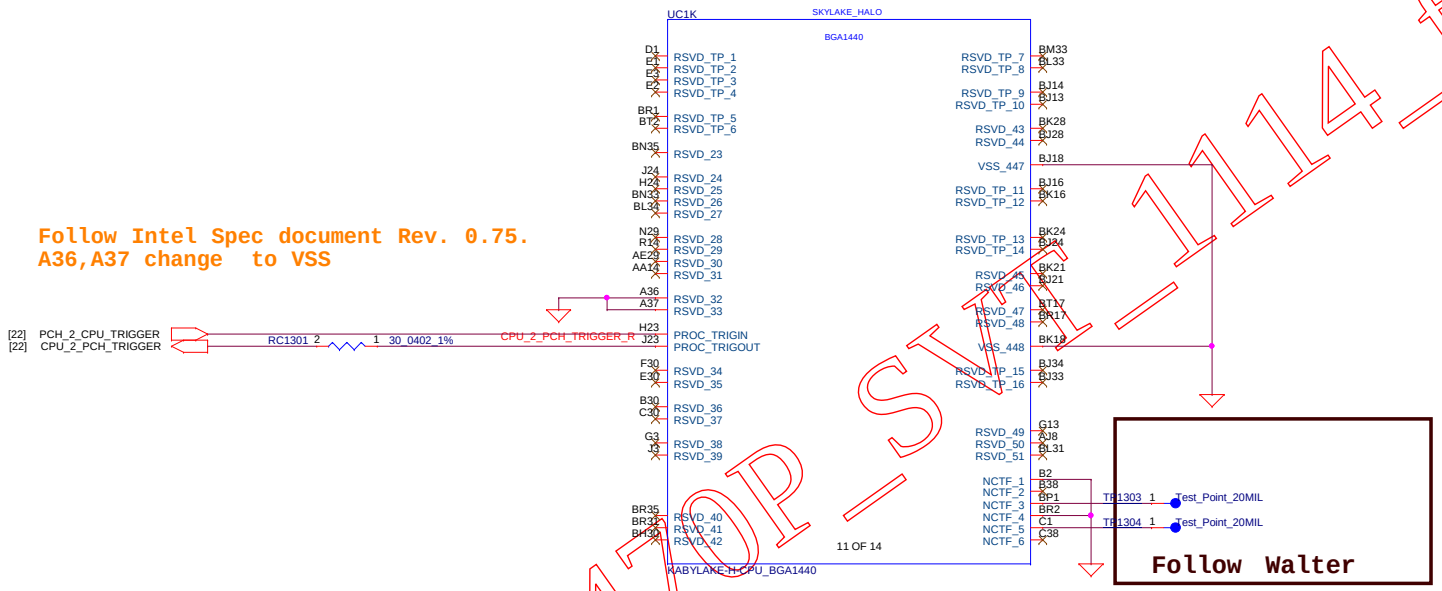

Follow Intel Spec document Rev. 0.75.
A36,A37 change to VSS

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Title: CPU KBL-H : RSVD

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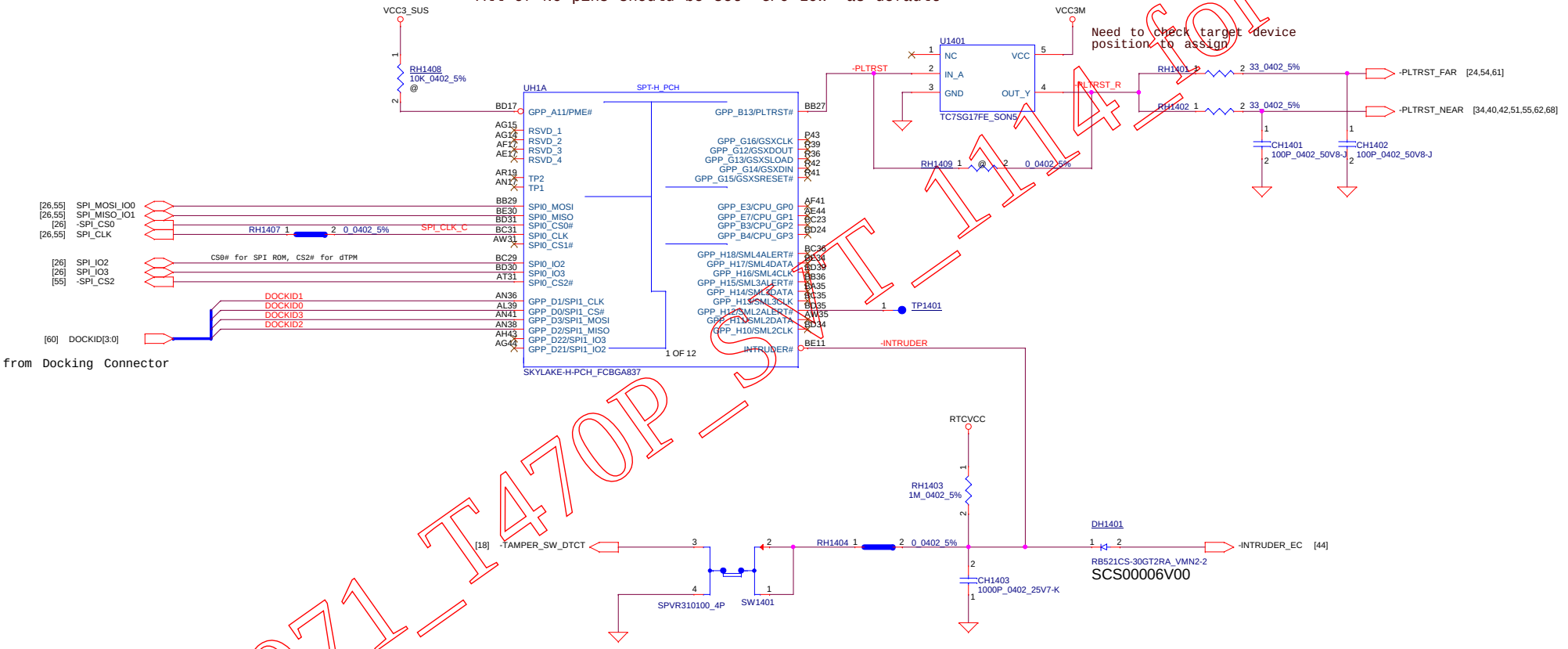
All of NC pins should be set "GPO LOW" as default

Need to check target device position to assign



DOOR	SWITCH	-INTRUDER
CLOSE	OPEN	HIGH
OPEN	CLOSE	LOW (ACTIVE)

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Title: **PCH SKL-H : SPI**

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USB2.0	Port Assignment	OC#
USB2 #1	Non-AOU port 1	OC0#
USB2 #2	Non-AOU port 2	OC0#
USB2 #3	Docking USB2	
USB2 #4	AOU port	OC1#
USB2 #5	WWAN	
USB2 #6	Finger printer	
USB2 #7	BT	
USB2 #8	Camera	
USB2 #9	Smart card reader	
USB2 #10	Touch panel	
USB2 #11		
USB2 #12		

Security Classification	LC Future Center Secret Data		
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Title: PCH SKL-H : DMI/PCIE/USB

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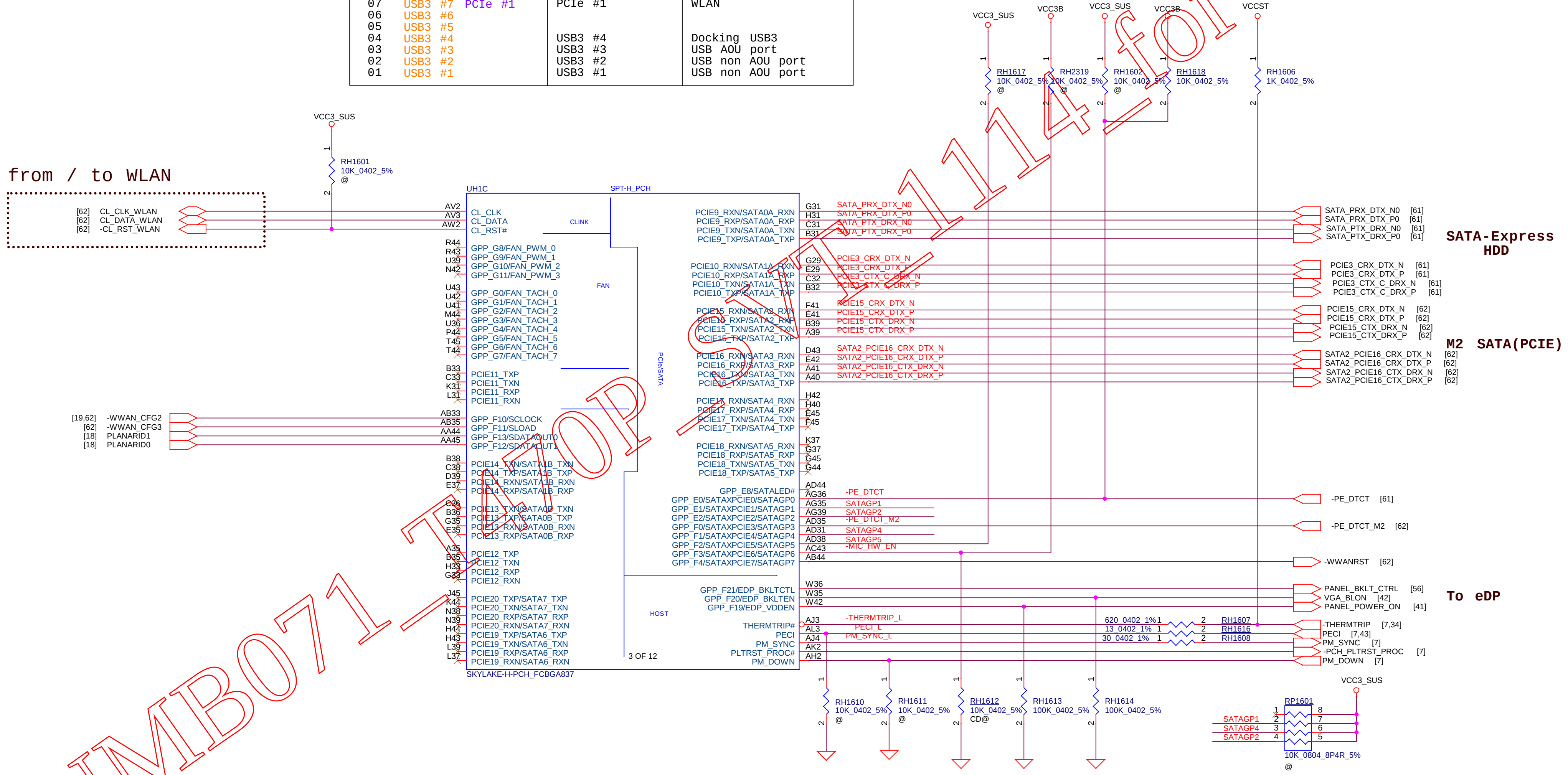
Port#	Flexible I/O	Configration	Port Assignment
22	PCIe #16 SATA #3	SATA #3 /PCIe #13	M.2 SATA SSD / Optane
21	PCIe #15 SATA #2	PCIe #14(Reversal)	Optane
20	PCIe #14 SATA #1		
19	PCIe #13 SATA #0 GbE		
18	PCIe #12 GbE		
17	PCIe #11		
16	PCIe #10 SATA #1	PCIe #10	SATA-Express
15	PCIe #9 SATA #0 GbE	SATA #0/PCIe #9	SATA-Express
14	PCIe #8		
13	PCIe #7		
12	PCIe #6		
11	PCIe #5 GbE	PCIe #5	Card reader
10	USB3 #10 PCIe #4 GbE	PCIe #4	GbE PHY
09	USB3 #9 PCIe #3		
08	USB3 #8 PCIe #2		
07	USB3 #7 PCIe #1	PCIe #1	WLAN
06	USB3 #6		
05	USB3 #5		
04	USB3 #4	USB3 #4	Docking USB3
03	USB3 #3	USB3 #3	USB AOU port
02	USB3 #2	USB3 #2	USB non AOU port
01	USB3 #1	USB3 #1	USB non AOU port



Notes:
1. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
2. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCHSKL-H : SATA/PCIE

LCFC

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Date: Tuesday, November 01, 2016 | Sheet 16 of 99

TABLE : Functional Strap

HDA_SDO	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.

TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or SPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

GPP_C5/SML0ALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confldentlality
LOW	Disable ME Crypto TLS(Default)

PLACE ON BOTTOM SIDE

TEST PAD
BOTTOM SIDE
DO NOT MOVE AFTER FIX

20140730: As of now, we cannot get information about these pins from SKL-H RVP and other documents. We need to confirm about them later.

From RTC Reset circuits
From CPU DCDC
From ASIC
From ASIC
From/to DIMM and TP
From/to GBE
From/to EC

FOLLOW WALTER CONNECTER TO GBE

from LPC Device(EC) to GBE
to M.2 WLAN

TABLE : Functional Strap

GPP_B14/SPKR(Top Swap Owerride)	
HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)

important

LPC is selected for EC. (Default)
This PD is insurance in case internal PD doesn't work well.

Pullups on SMB are located in SMBUS Switch page.

INTEL FAE ADVICE

RH1739 Pull up 150K follow MOW

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCH SKL-H : AUDIO/SMBUS/JTAG

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to be confirm on SDV

RH1816 1 @ 2 100K_0402_5% HDMI_DDIP1_HPD
RH1814 NODPRE@ 1 2 100K_0402_5% MDP_DDIP2_HPD
RH1817 1 2 100K_0402_5% DOCK_DDIP3_HPD
RH1815 1 2 100K_0402_5% CPU_EDP_HPD

DDIP2_HPD : PS8330 has Int.PD 150K

VCC3B VCC3B

RH1818 2.2K_0402_5% @
RH1812 2.2K_0402_5%
RH1813 2.2K_0402_5%
RH1807 2.2K_0402_5% @
RH1806 2.2K_0402_5% @
RH1810 2.2K_0402_5%
RH1811 2.2K_0402_5%

[57] HDMI_DDIP1_HPD
[58,59] MDP_DDIP2_HPD
[60] DOCK_DDIP3_HPD
RH1805 1 2 0_0402_5% EXT_DP_HPD_I
RH1823 1 2 0_0402_5%

[56] CPU_EDP_HPD

UH1E SPT-H_PCH

AW4 GPP_I0/DDPB_HPD0
AY2 GPP_I1/DDPC_HPD1
AV4 GPP_I2/DDPD_HPD2
BA4 GPP_I3/DDPE_HPD3
BD7 GPP_I4/EDP_HPD

GPP_I7/DDPC_CTRLCLK BB3
GPP_I8/DDPC_CTRLDATA BD6
GPP_I5/DDPB_CTRLCLK BA5
GPP_I6/DDPB_CTRLDATA BC4
GPP_I9/DDPD_CTRLCLK BE5
GPP_I10/DDPD_CTRLDATA BE6

MDP_DDIP2_CTRLCLK [58,59]
MDP_DDIP2_CTRLDATA [58,59]
HDMI_DDIP1_CTRLCLK [57]
HDMI_DDIP1_CTRLDATA [57]
DOCK_DDIP3_CTRLCLK [60]
DOCK_DDIP3_CTRLDATA [60]

GPP_F14 Y44
GPP_F23 V44
GPP_F22 W39
-SC_DTCT [65]
-TAMPER_SW_DTCT [14]
SmartCard

GPP_G23 L43
GPP_G22 L44
GPP_G21 G35
GPP_G20 G34
GPP_H23 BD36
-DGFX_WITH_DISPLAYOUT

5 OF 12

SKYLAKE-H-PCH_FCBGA837

VCC3_SUS
RH1808 10K_0402_5% @
RH1809 10K_0402_5% @

VCC3B

Modify PLANARID[3:0] to Int. PU 20K

RH1801 1 @ 2 10K_0402_5% PLANARID0
RH1802 1 @ 2 10K_0402_5% PLANARID1
RH1803 1 @ 2 10K_0402_5% PLANARID2
RH1804 1 @ 2 10K_0402_5% PLANARID3

PLANARID0 [16]
PLANARID1 [16]
PLANARID2 [15]
PLANARID3 [15]

RH1819 1 @ 2 0_0402_5% PLANARID0
RH1822 1 @ 2 0_0402_5% PLANARID1
RH1820 1 @ 2 0_0402_5% PLANARID2
RH1821 1 @ 2 0_0402_5% PLANARID3

TABLE

	PLANAR ID			
	3	2	1	0
SDV	0	0	0	0
FVT	0	0	0	1
SIT	0	0	1	0
SVT	1	1	1	1

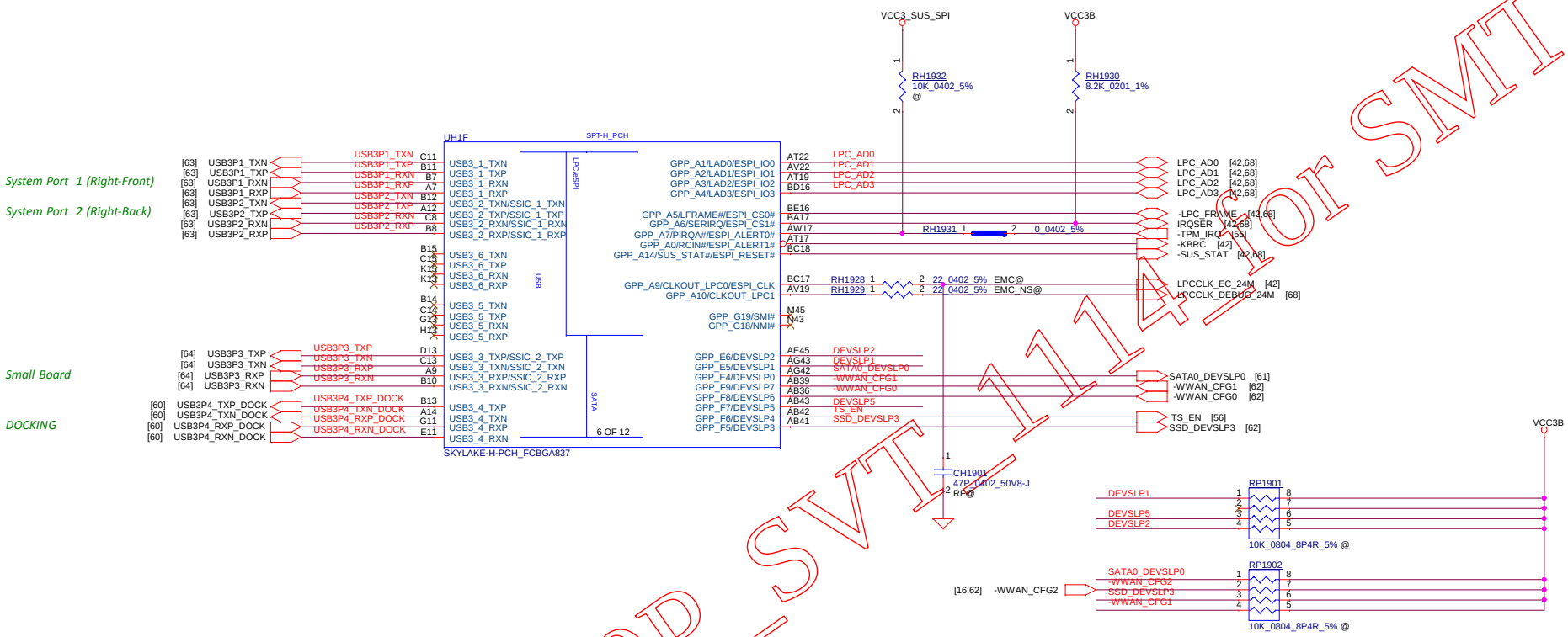
SVT internal PU

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCH SKL-H : DDI CONTROL

Size: Custom | Document Number: NM-B071 | Rev: 0.2

Date: Tuesday, November 01, 2016 | Sheet 18 of 99

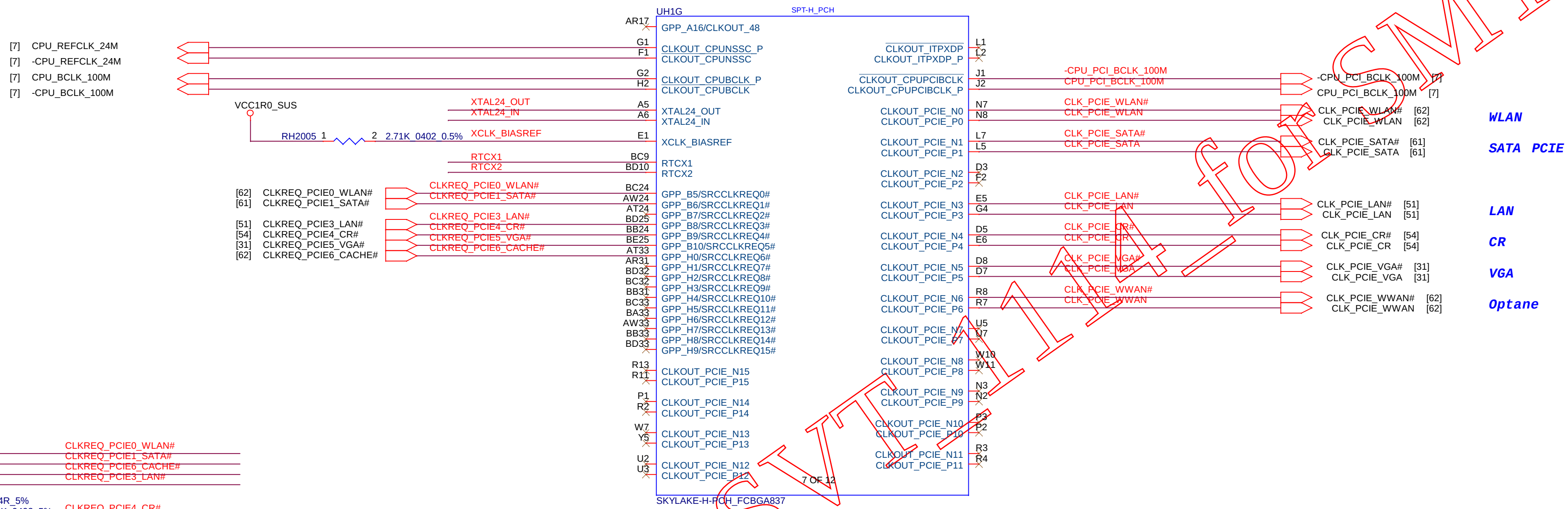


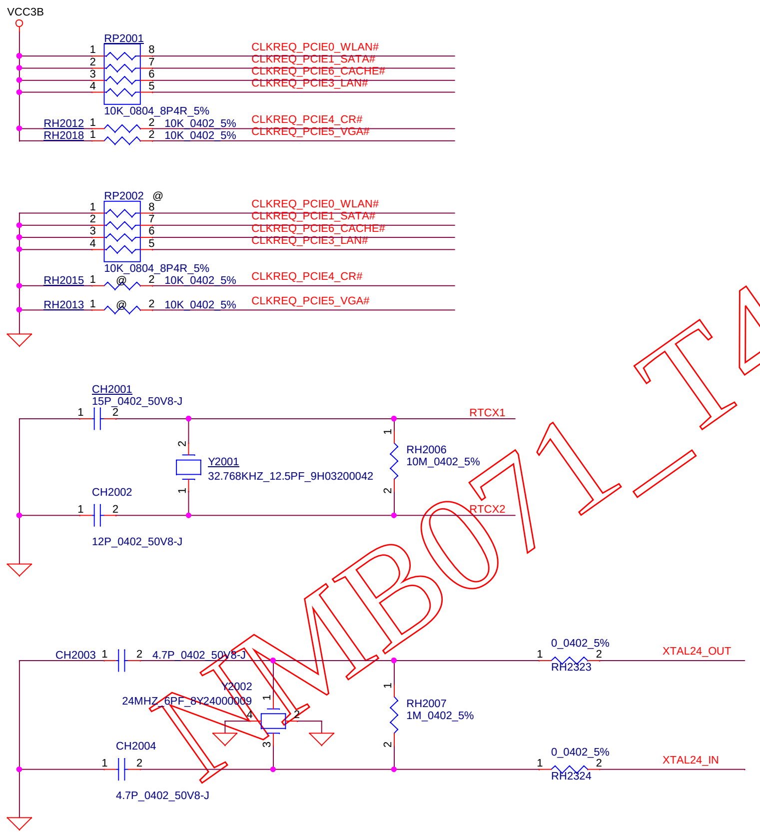
Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCH SKL-H : USB3/LPC

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Tuesday, November 01, 2016 Sheet 19 of 99



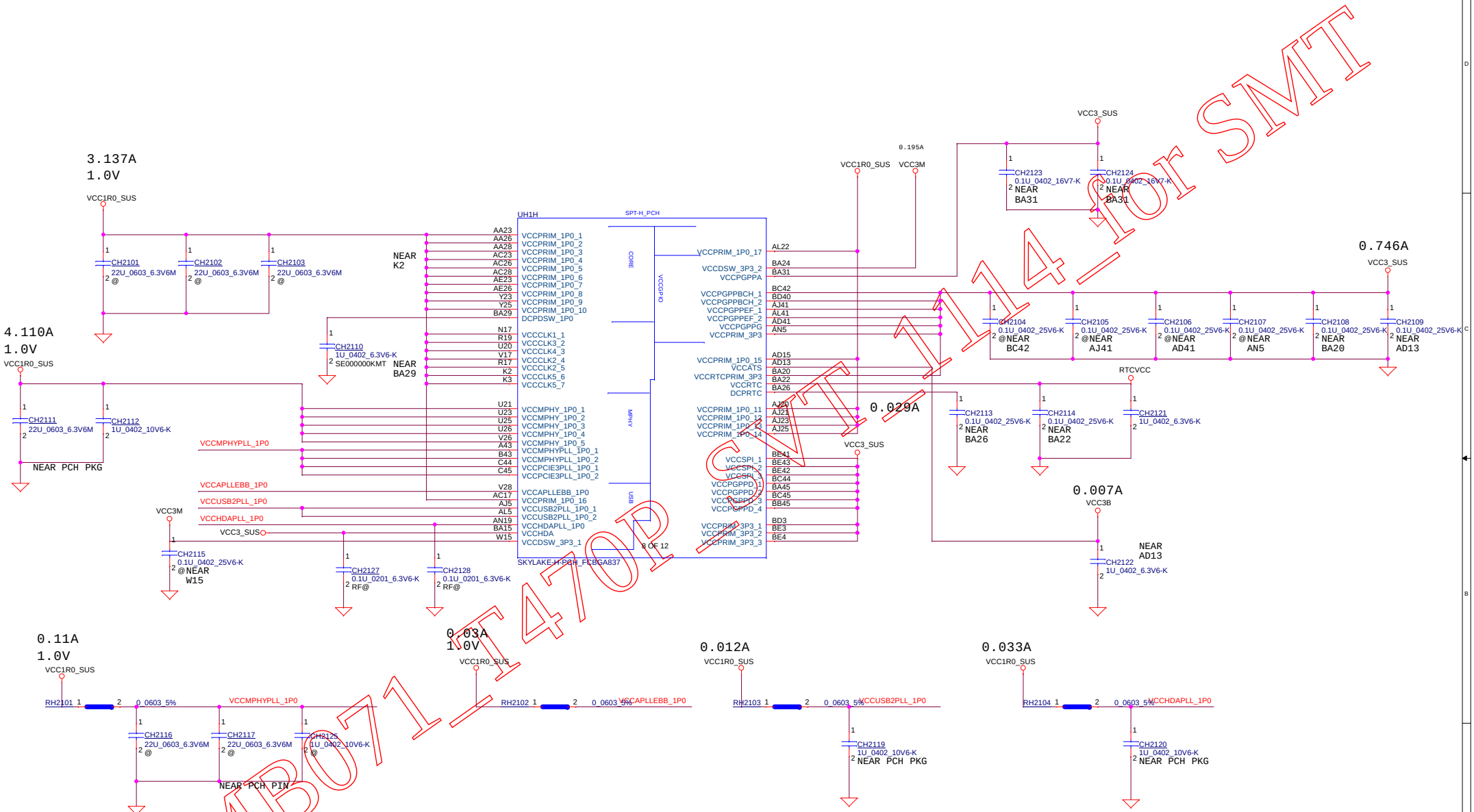


PCIE Clock Assignment	Clock Request
Clock 0 : WLAN	CLKREQ0#
Clock 1 : SATA-Express	CLKREQ1#
Clock 3 : Giga LAN	CLKREQ3#
Clock 4 : CARD READER	CLKREQ4#
Clock 5 : GPU N16S-GTR	CLKREQ5#
Clock 6 : Optane	CLKREQ6#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **PCH SKL-H : CLK**

Size: Custom | Document Number: NM-B071 | Rev: 0.2

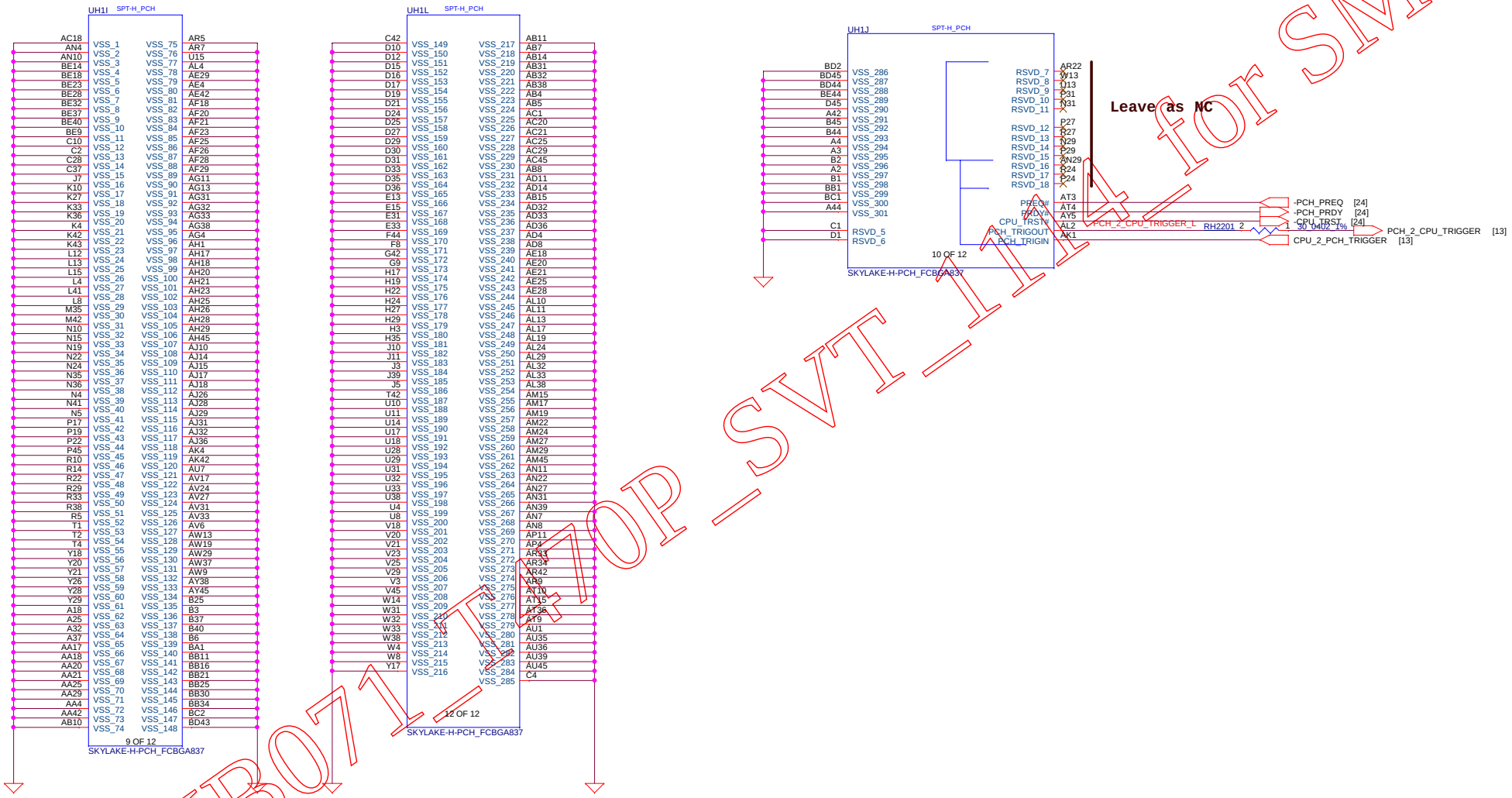


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **PCH SKL-H : POWER**

Size	Document Number	Rev
Custom	T460P NM-B071	0.2

Date: Tuesday, November 01, 2016 Sheet 21 of 99

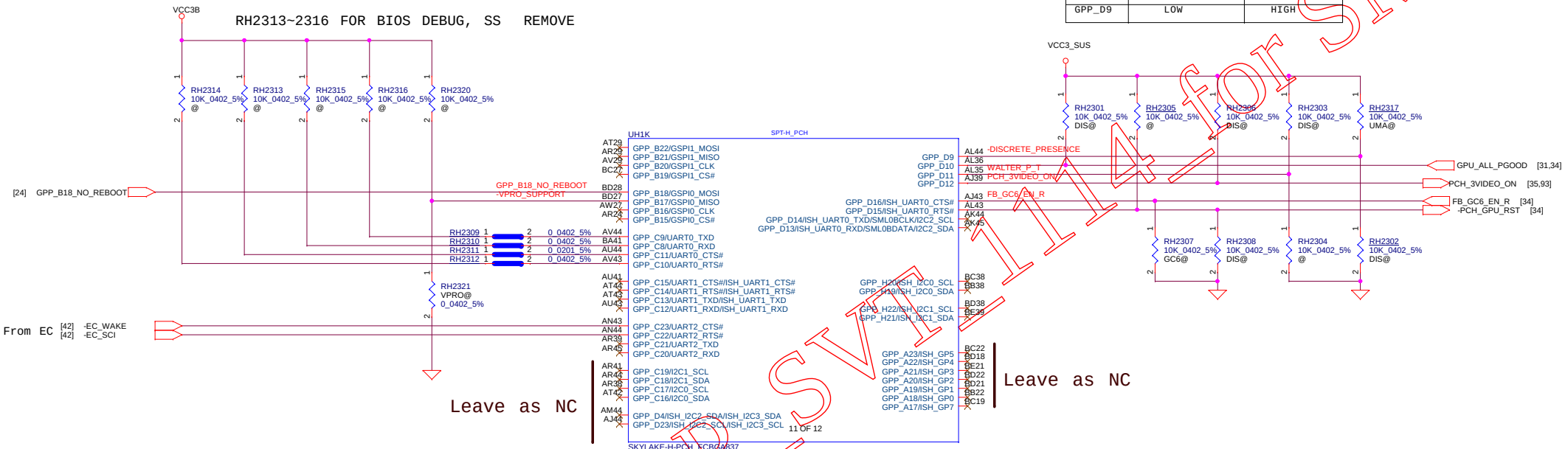


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **PCH SKL-H : GND/RSVD**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Tuesday, November 01, 2016 Sheet 22 of 99



	DIS	UMA
GPP_D9	LOW	HIGH

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: PCH SKL-H : GSPI/UART/I2C

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Tuesday, November 01, 2016 Sheet 23 of 99

R2420,R2422,R2423,R2407,R2410,R2413,R2415,R2401 NEAR BY PCH

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

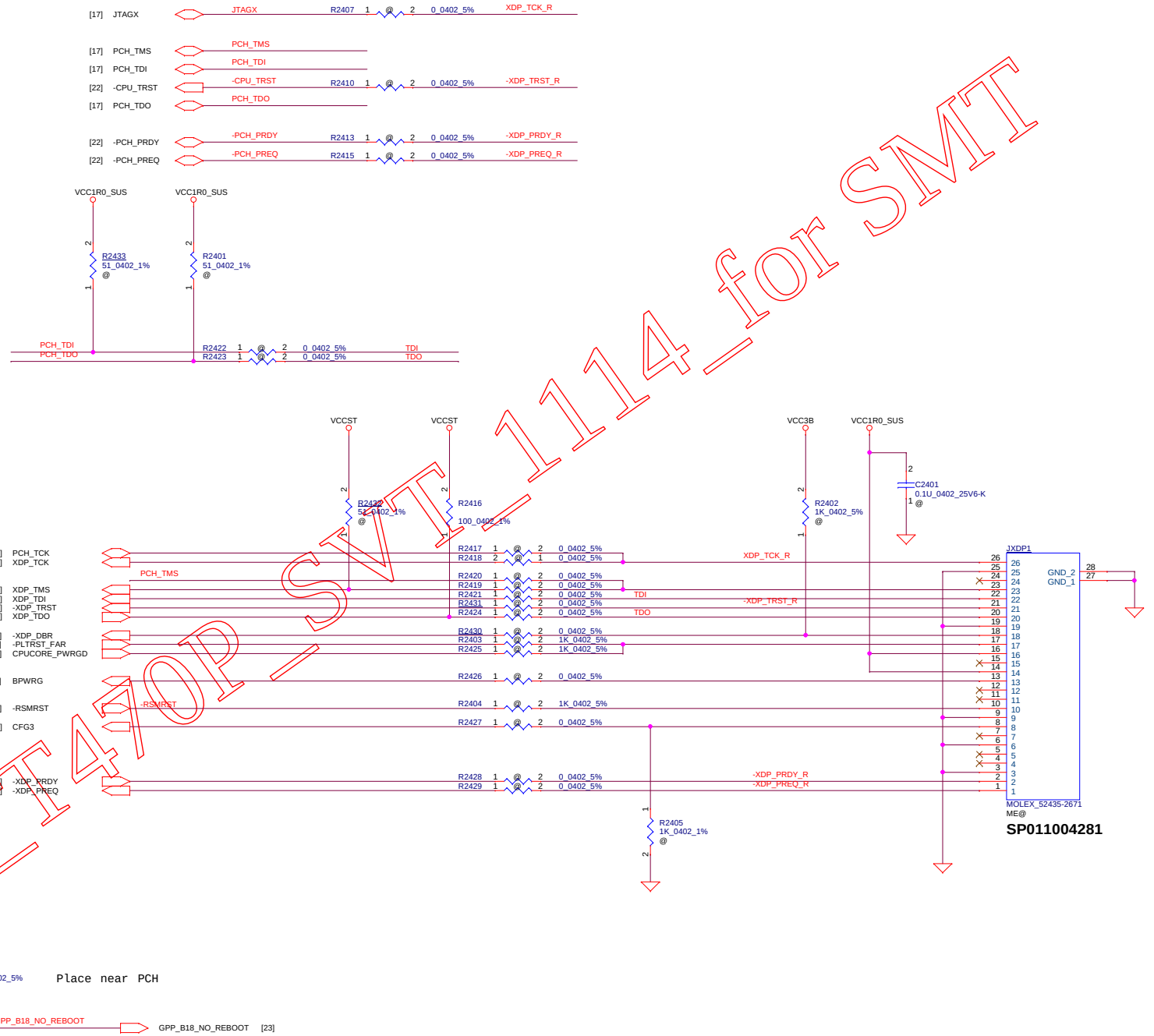
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R2406
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

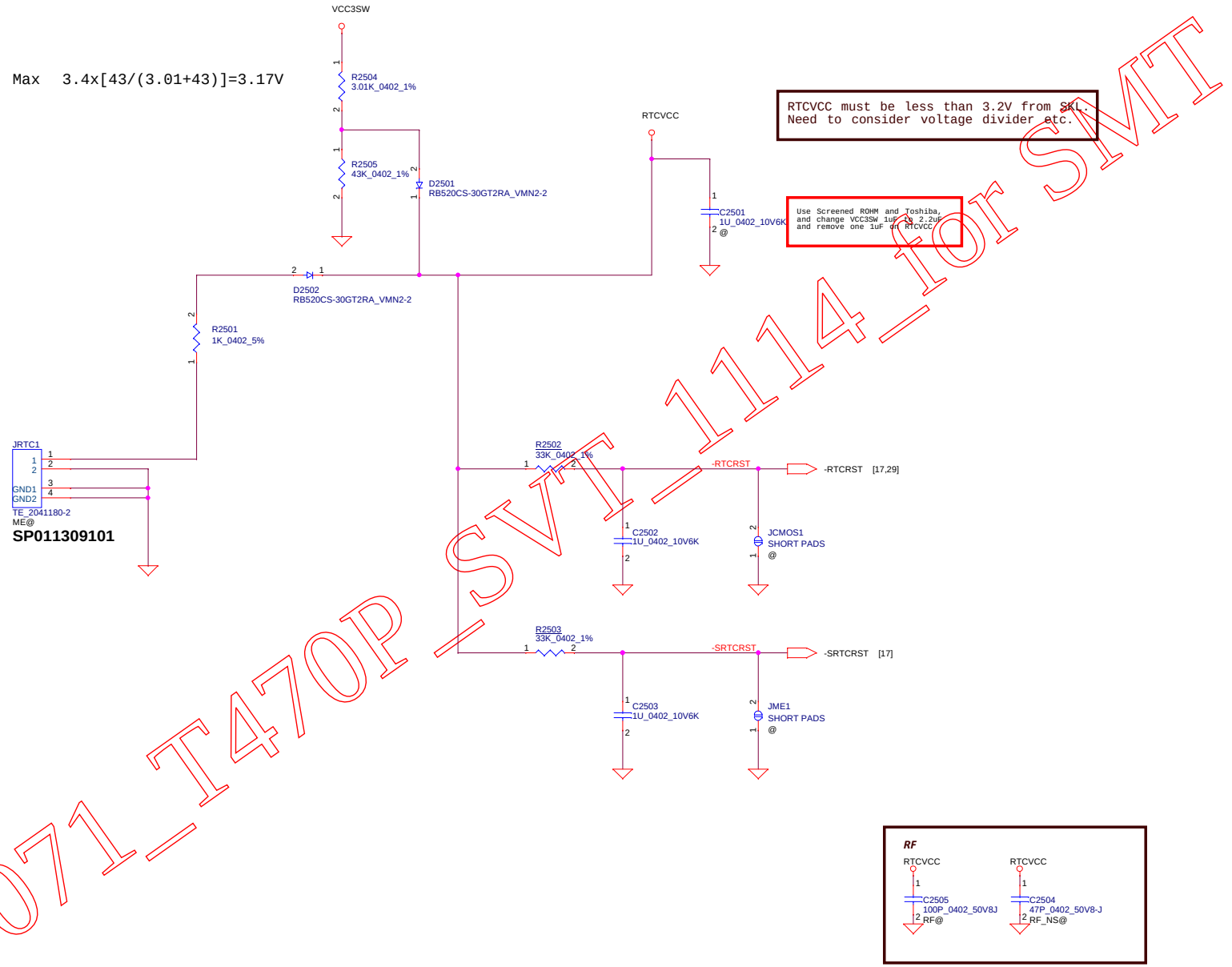
LOGIC



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **XDP CONNECTOR**

Size	Document Number	Rev
Custom	T470P	NM-B071 0.2
Date: Wednesday, October 12, 2016	Sheet 24 of 99	

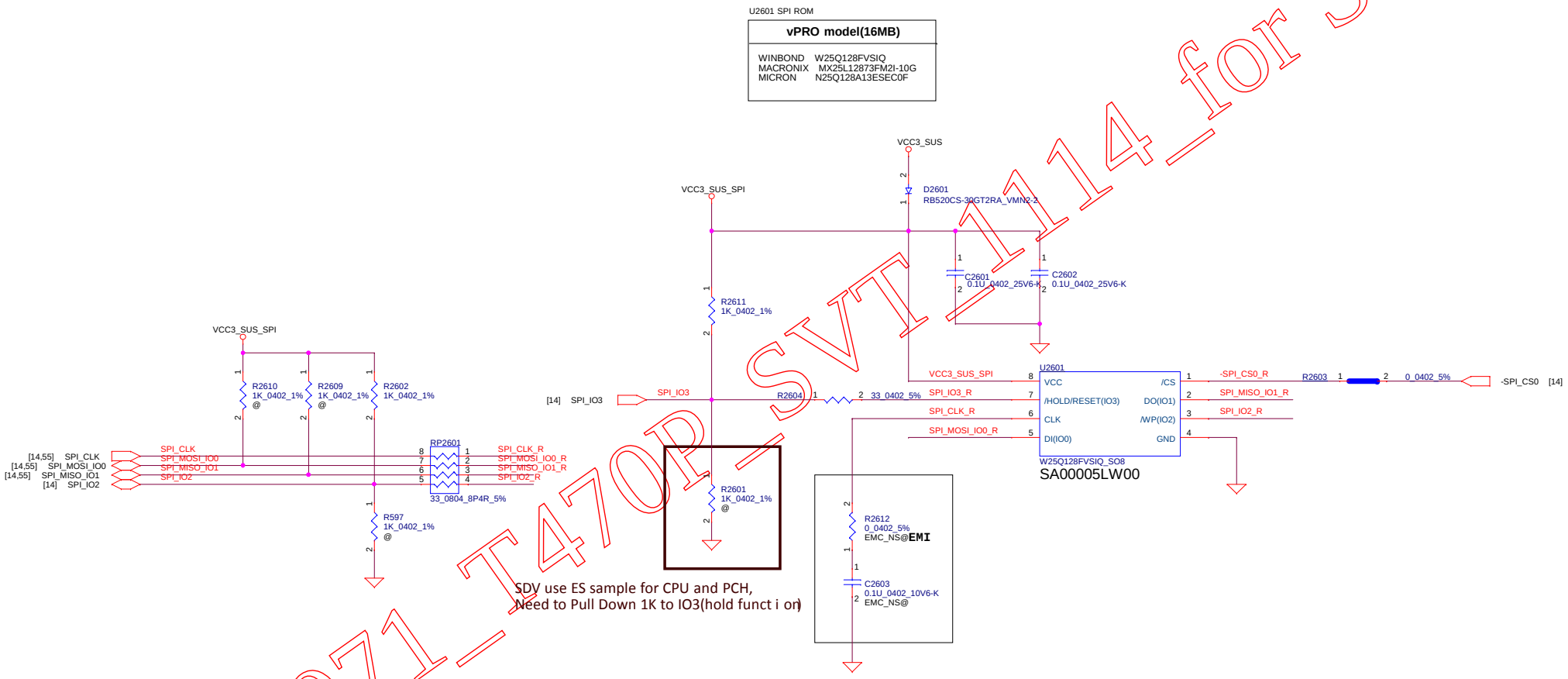


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **RTC BATTERY**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 25 of 99

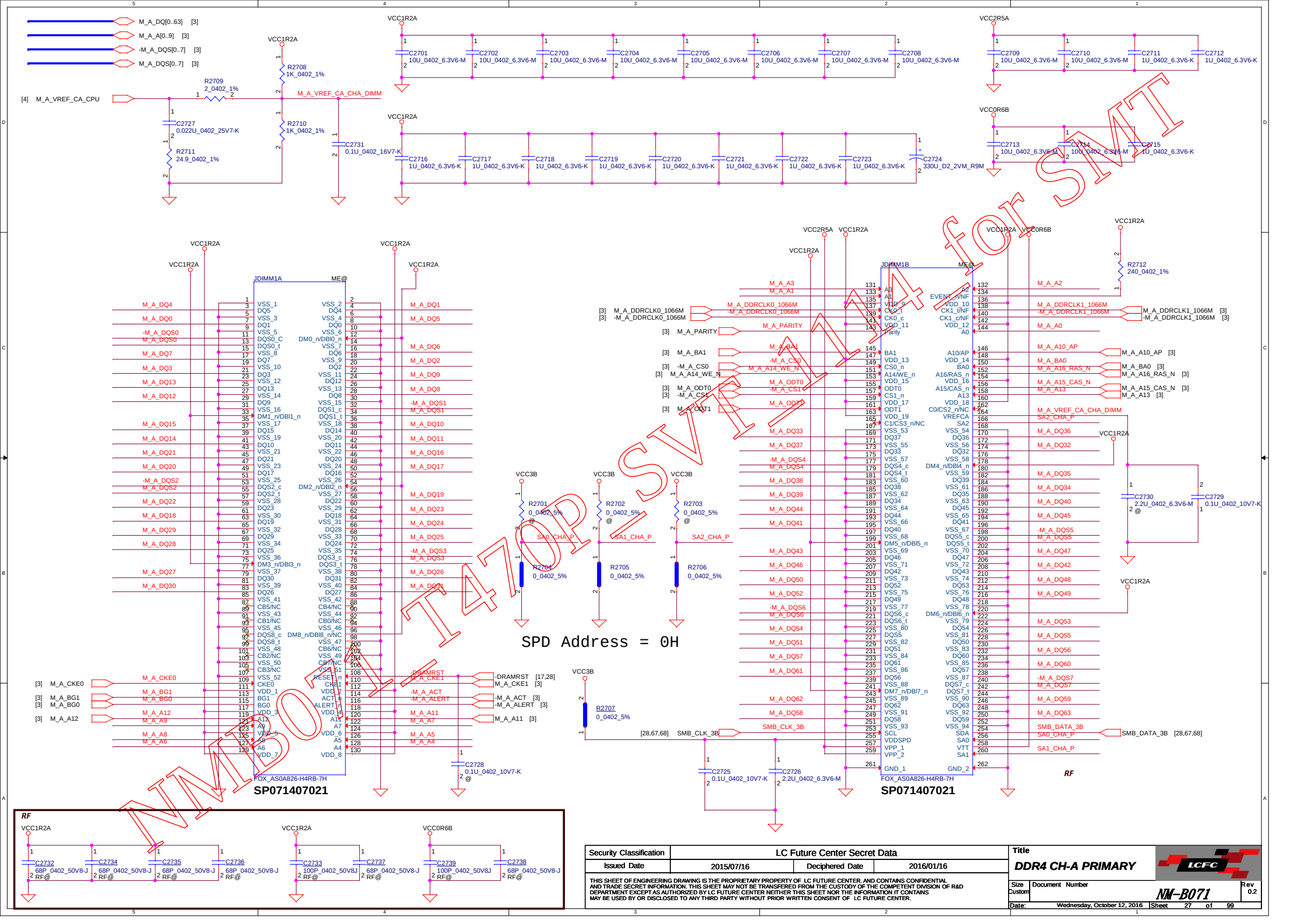


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **SPI FLASH**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, November 09, 2016 Sheet 26 of 99

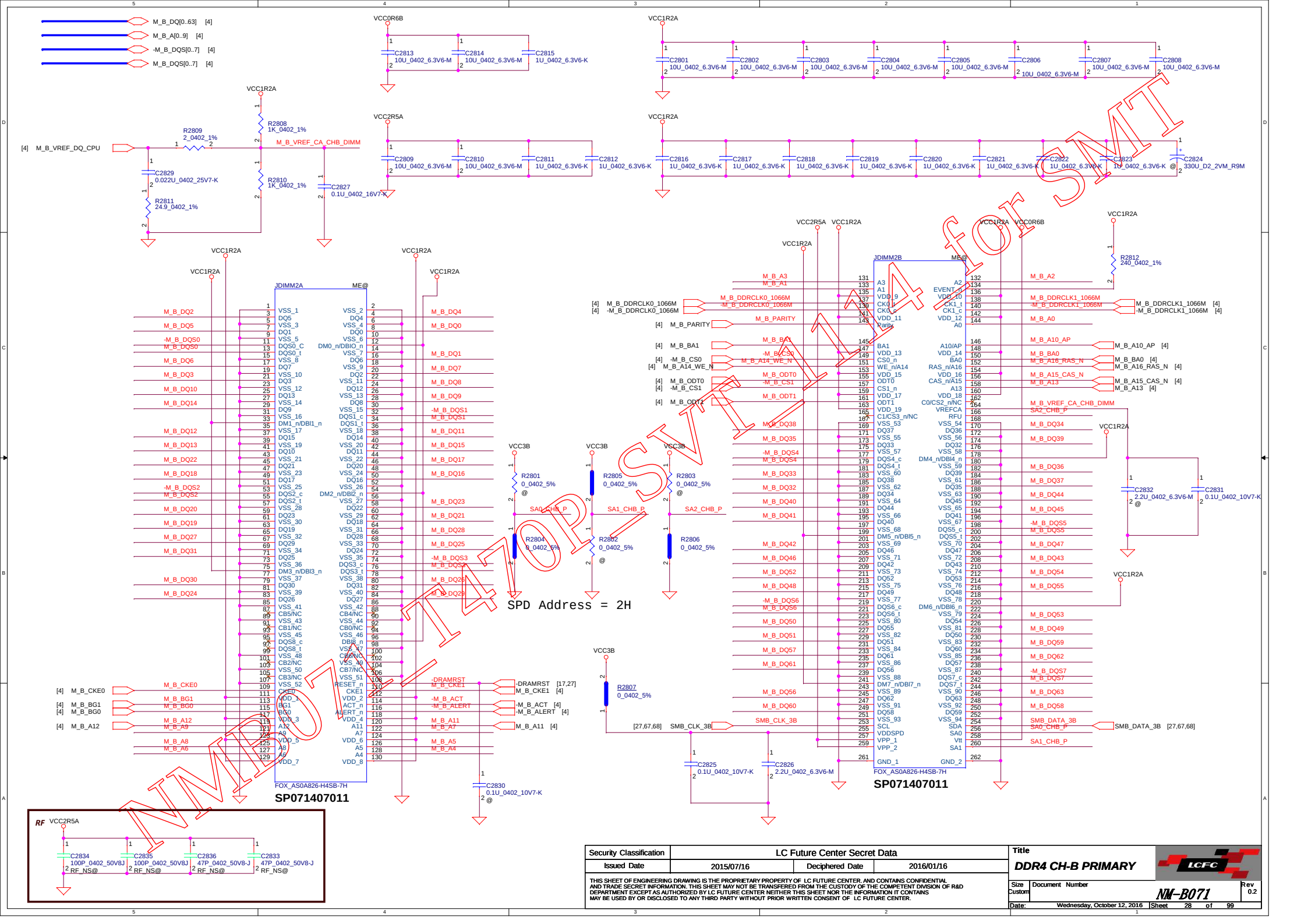


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **DDR4 CH-A PRIMARY**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 27 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

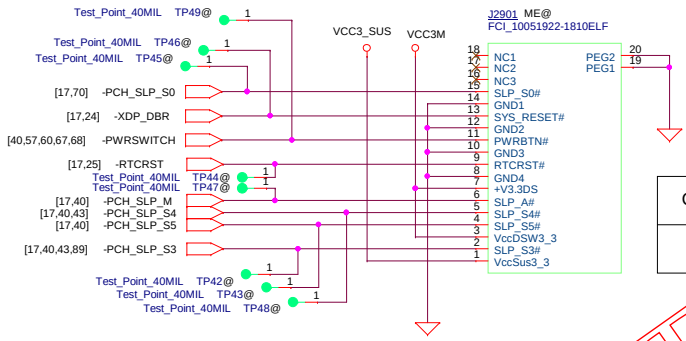
Title: **DDR4 CH-B PRIMARY**

LCFC

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 28 of 99

APS/PETS interface



Connector	Planar	Box
J2901	**ASM**	**NO ASM**

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title		
Size: Custom	Document Number: NM-B071	Rev: 0.2
Date: Wednesday, October 12, 2016	Sheet 29 of 99	

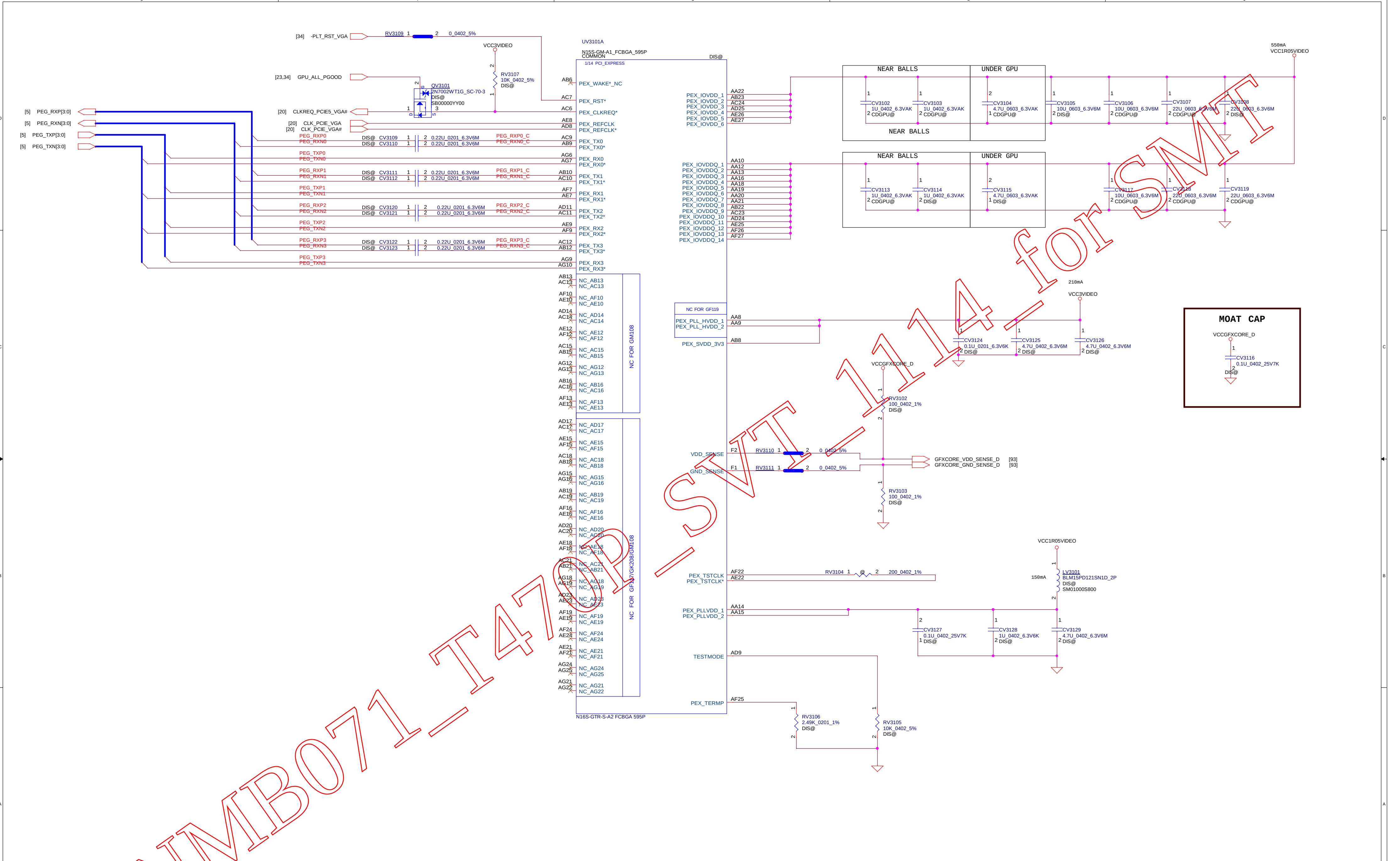
Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title

LCFC

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 30 of 99

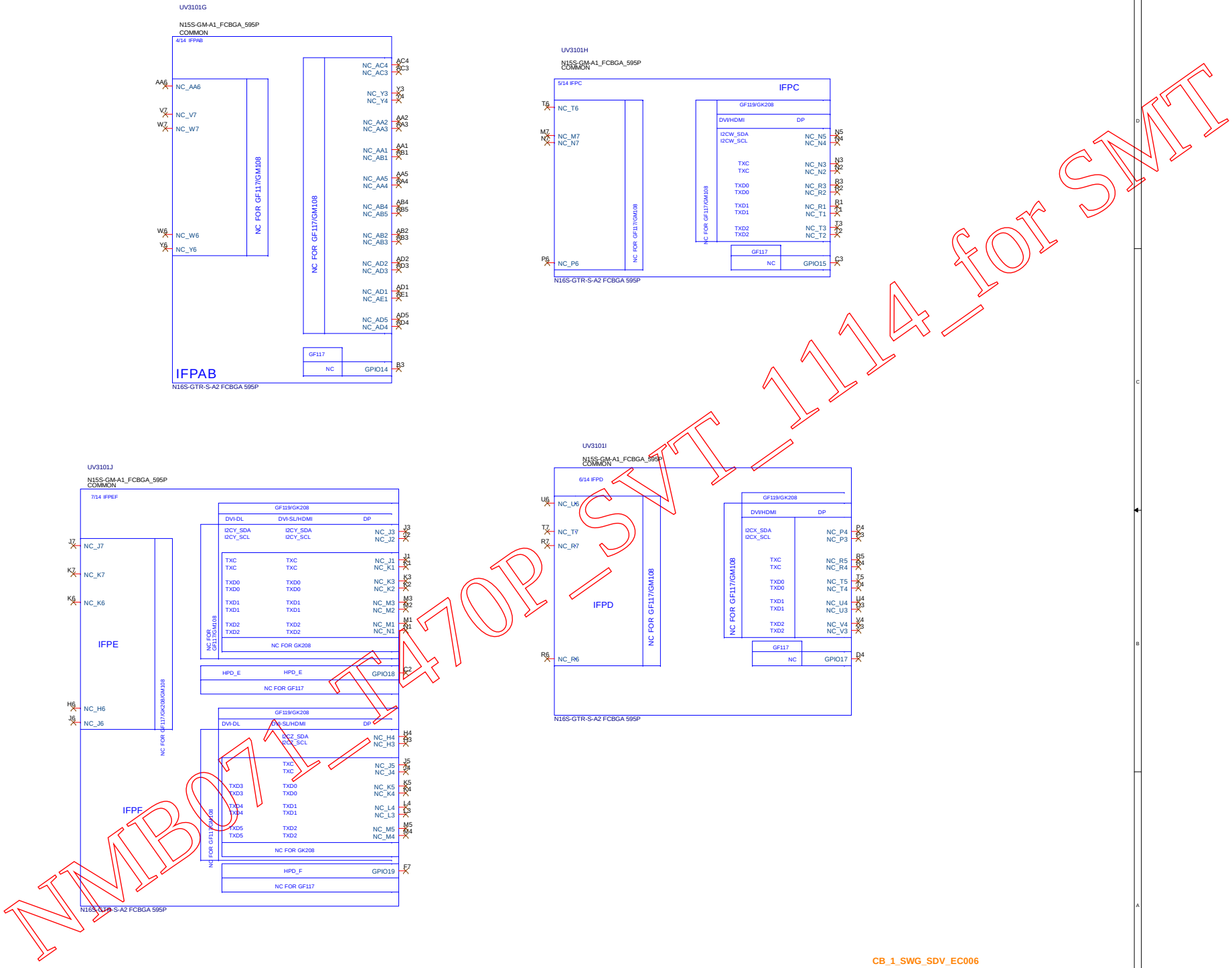

UV3101A
N15S-GM-A1_FCBGA_595P
COMMON
1/14 PCI_EXPRESS
DIS@
[34] -PLT_RST_VGA
RV3109 0_0402_5%
VCC3VIDEO
RV3107 10K_0402_5% DIS@
[23,34] GPU_ALL_PGOOD
QV3101 2N7002WT1G_SC-70-3 DIS@ SB00000YY00
[20] CLKREQ_PCIE5_VGA#
[20] CLK_PCIE_VGA
[20] CLK_PCIE_VGA#
[5] PEG_RXP[3:0]
[5] PEG_RXN[3:0]
[5] PEG_TXP[3:0]
[5] PEG_TXN[3:0]
PEX_WAKE*_NC
PEX_RST*
PEX_CLKREQ*
PEX_REFCLK
PEX_REFCLK*
PEX_TX0
PEX_TX0*
PEX_RX0
PEX_RX0*
PEX_TX1
PEX_TX1*
PEX_RX1
PEX_RX1*
PEX_TX2
PEX_TX2*
PEX_RX2
PEX_RX2*
PEX_TX3
PEX_TX3*
PEX_RX3
PEX_RX3*
CV3109 0.22U_0201_6.3V6M
CV3110 0.22U_0201_6.3V6M
CV3111 0.22U_0201_6.3V6M
CV3112 0.22U_0201_6.3V6M
CV3120 0.22U_0201_6.3V6M
CV3121 0.22U_0201_6.3V6M
CV3122 0.22U_0201_6.3V6M
CV3123 0.22U_0201_6.3V6M
NC FOR GM108
NC FOR GF117/GK208/GM108
N16S-GTR-S-A2 FCBGA 595P
PEX_IOVDD_1 … PEX_IOVDD_6
PEX_IOVDDQ_1 … PEX_IOVDDQ_14
NEAR BALLS
UNDER GPU
550mA
VCC1R05VIDEO
CV3102 1U_0402_6.3VAK CDGPU@
CV3103 1U_0402_6.3VAK CDGPU@
CV3104 4.7U_0603_6.3VAK CDGPU@
CV3105 10U_0603_6.3V6M DIS@
CV3106 10U_0603_6.3V6M CDGPU@
CV3107 22U_0603_6.3V6M CDGPU@
CV3108 22U_0603_6.3V6M DIS@
CV3113 1U_0402_6.3VAK CDGPU@
CV3114 1U_0402_6.3VAK DIS@
CV3115 4.7U_0603_6.3VAK DIS@
CV3117 10U_0603_6.3V6M CDGPU@
CV3118 22U_0603_6.3V6M CDGPU@
CV3119 22U_0603_6.3V6M CDGPU@
NC FOR GF119
PEX_PLL_HVDD_1
PEX_PLL_HVDD_2
PEX_SVDD_3V3
210mA
VCC3VIDEO
CV3124 0.1U_0201_6.3V6K DIS@
CV3125 4.7U_0402_6.3V6M DIS@
CV3126 4.7U_0402_6.3V6M DIS@
MOAT CAP
VCCGFXCORE_D
CV3116 0.1U_0402_25V7K DIS@
RV3102 100_0402_1% DIS@
VDD_SENSE
GND_SENSE
RV3110 0_0402_5%
RV3111 0_0402_5%
GFXCORE_VDD_SENSE_D [93]
GFXCORE_GND_SENSE_D [93]
RV3103 100_0402_1% DIS@
VCC1R05VIDEO
PEX_TSTCLK
PEX_TSTCLK*
RV3104 200_0402_1%
150mA
LV3101 BLM15PD121SN1D_2P DIS@ SM01000S800
PEX_PLLVDD_1
PEX_PLLVDD_2
CV3127 0.1U_0402_25V7K DIS@
CV3128 1U_0402_6.3V6K DIS@
CV3129 4.7U_0402_6.3V6M DIS@
TESTMODE
PEX_TERMP
RV3106 2.49K_0201_1% DIS@
RV3105 10K_0402_5% DIS@

Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title: N16S-GT(1/6) PEG I/F

Size: Custom | Document Number: NM-B071 | Rev: 0.2

Date: Wednesday, October 12, 2016 | Sheet 31 of 99



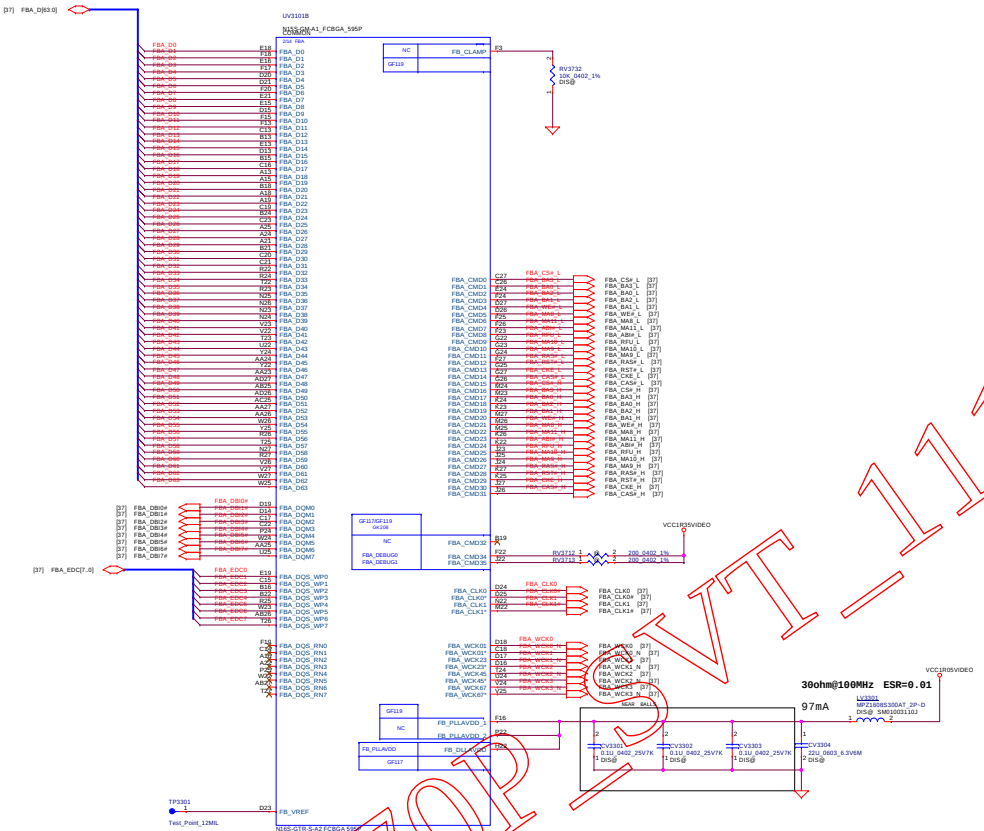
CB_1_SWG_SDV_EC006

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: *N16S-GT(2/6) DIGITAL OUT I/F*

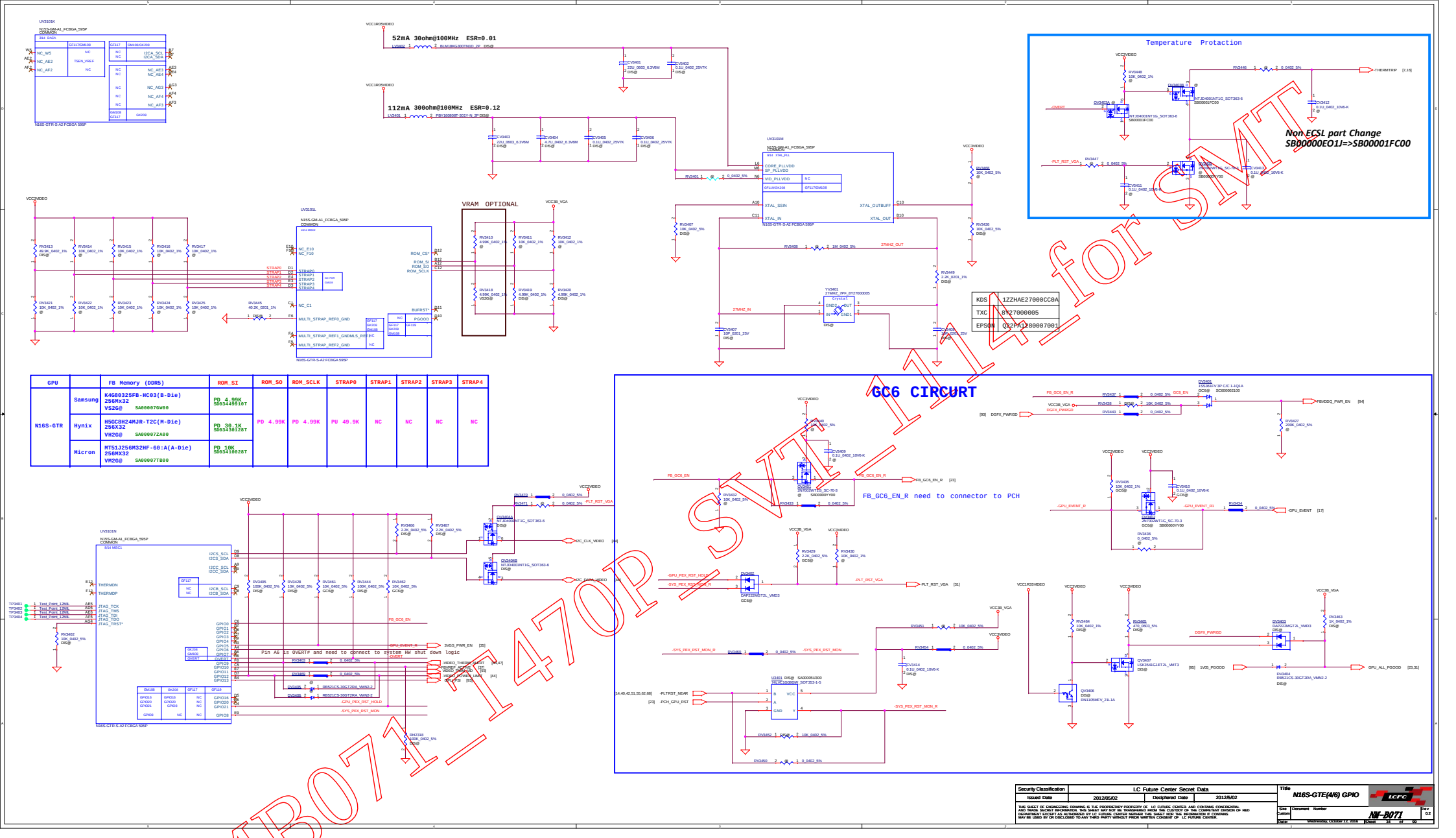
Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 32 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title	N16S-GT(3/6) VRAM I/F		
Size	Document Number		Rev
D	NM-B071		0.2
Date:	Wednesday, October 24, 2012	Sheet	33 of 99



GPU		FB Memory (DDR5)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16S-GTR	Samsung	K4G80325FB-HC03(B-Die) 256Mx32 VS26@ SA00007GW00	PD 4.99K SD03499I0T	PD 4.99K	PD 4.99K	PU 49.9K	NC	NC	NC	NC
	Hynix	H5GC8H24MJR-T2C(M-Die) 256X32 VH26@ SA00007ZA00	PD 30.1K SD03430I2BT							
	Micron	MT51J256M32HF-60:A(A-Die) 256MX32 VM26@ SA00007T800	PD 10K SD03410I28T							

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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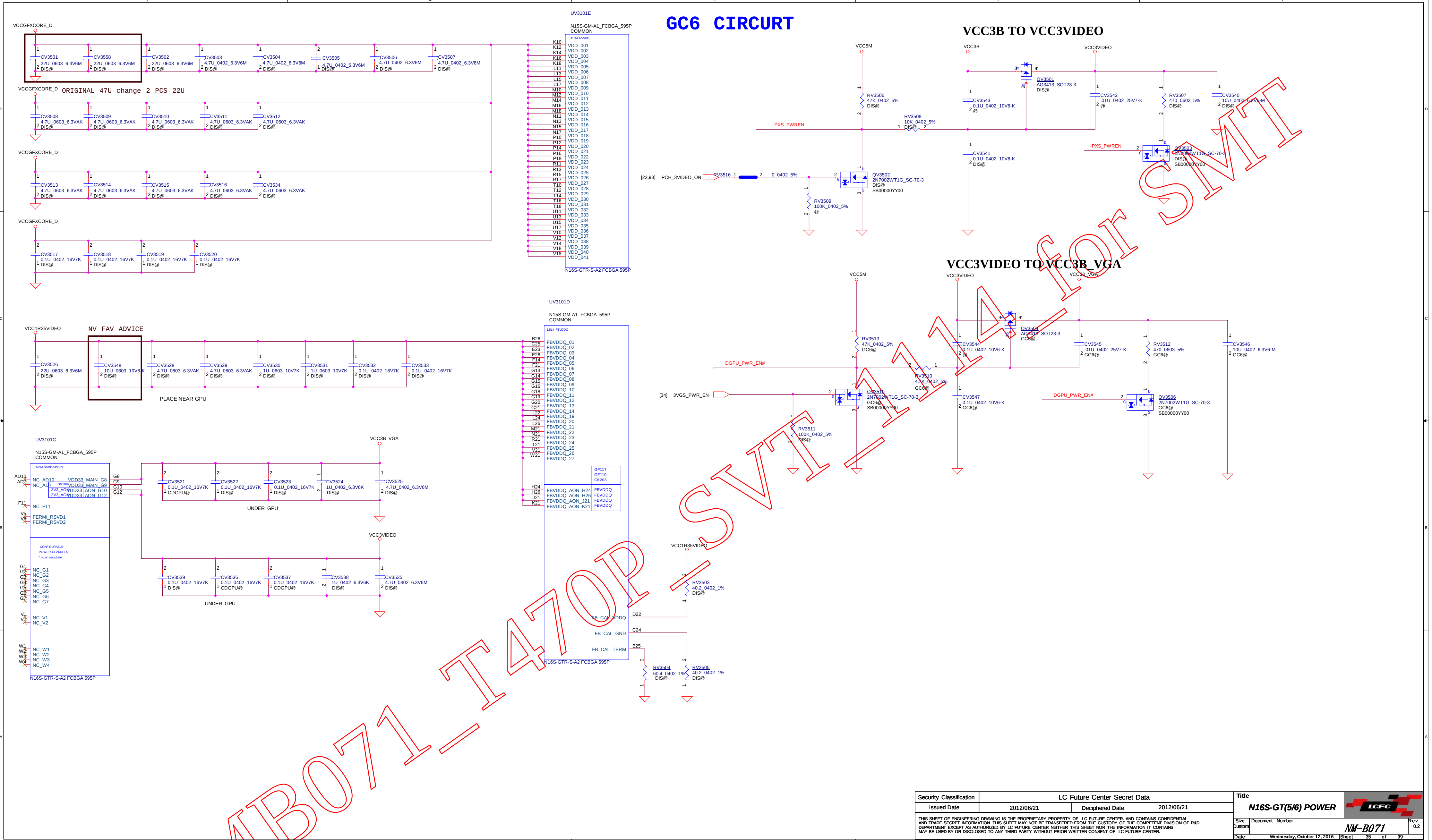
Title	N16S-GTE(4/6) GPIO		
Size	Document Number		Rev
Custom		NM-B071	0.2
Date:	Wednesday, October 03, 2012	Sheet 38 of 50	



Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

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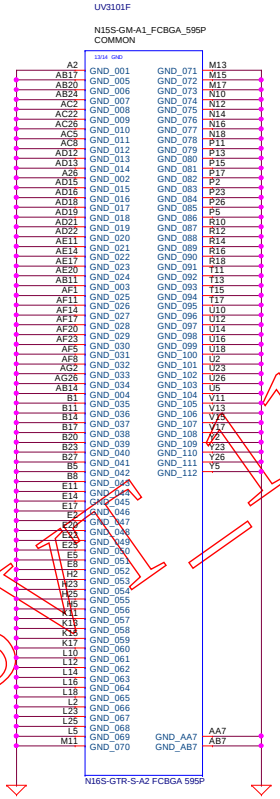
Title: N16S-GT(5/6) POWER

LCFC

Size: Custom | Document Number: NM-B071 | Rev 0.2

Date: Wednesday, October 12, 2016 | Sheet 35 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title: **N16S-GT(6/6) GND**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 36 of 99

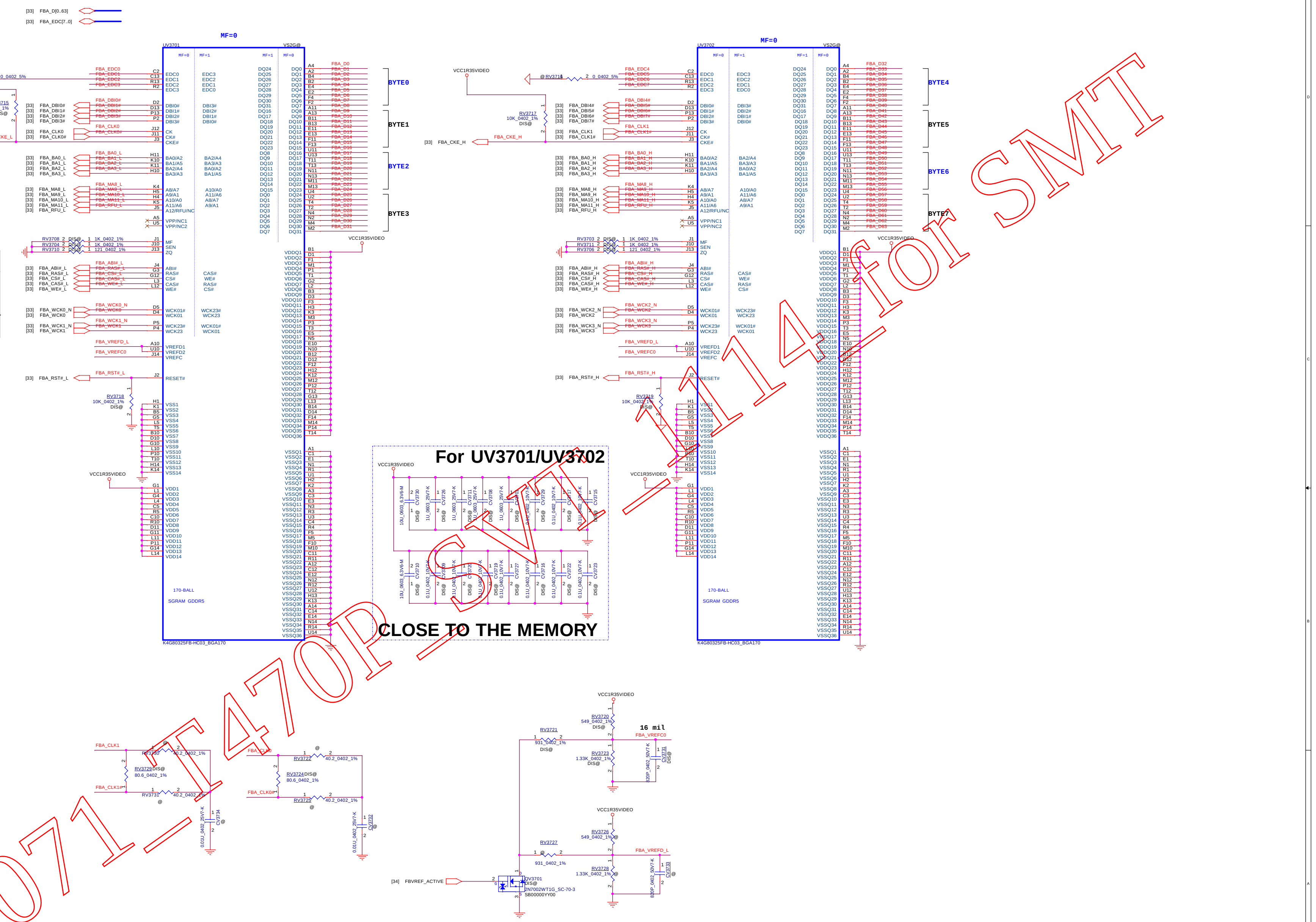


TABLE
GDDR5 VIDEO MEMORY

	Micron 4GBITS (256Mx32)	HYNIX 4GBITS(256Mx32)	SAMSUNG 4GBITS(256Mx32)
UV3701 UV3702	MT51J256M32HF-60:A (A-Die)256X32 SA00007TB00	H5GC8H24MJR-T2C (M-Die)256X32 SA00007ZA00	K4G80325FB-HC03 (B-Die)256Mx32 SA00007GW00
BOM Structure	VM2G@	VH2G@	VS2G@

Table 12. N16V-GMR1 and N16S-LG/-GMR/-GTR GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	256Mx16	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		128Mx32	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
		512Mx16	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production candidate
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready

Note: For N16V-GMR1 and N16S-LG/-GMR/-GTR, the maximum allowable memory case temperature is 85 °C.

Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title: VRAM CHANNEL-A

Size: D | Document Number: NM-B071 | Rev: 0.2

Security Classification	LC Future Center Secret Data		Title: N16S-GT VRAM CHANNEL-A
Issued Date	2012/06/21	Deciphered Date: 2012/06/21	

Size: A3	Document Number: NM-B071		Rev: 0.3
Date: Wednesday, October 31, 2012	Sheet 28 of 47		

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title

N16S-GT MEMORY TERMINATION

Size	Document Number	Rev
B	NM-B071	0.2

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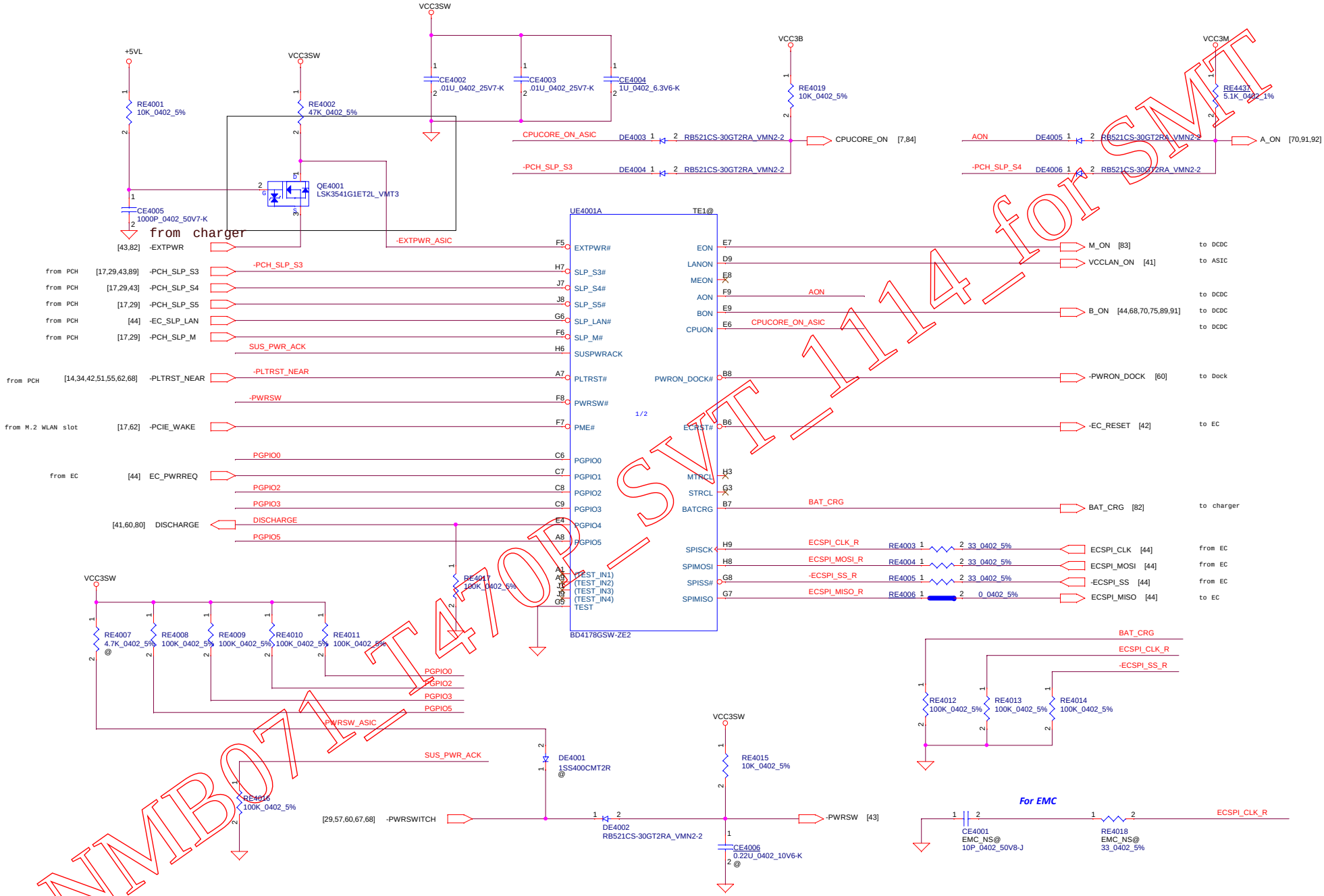
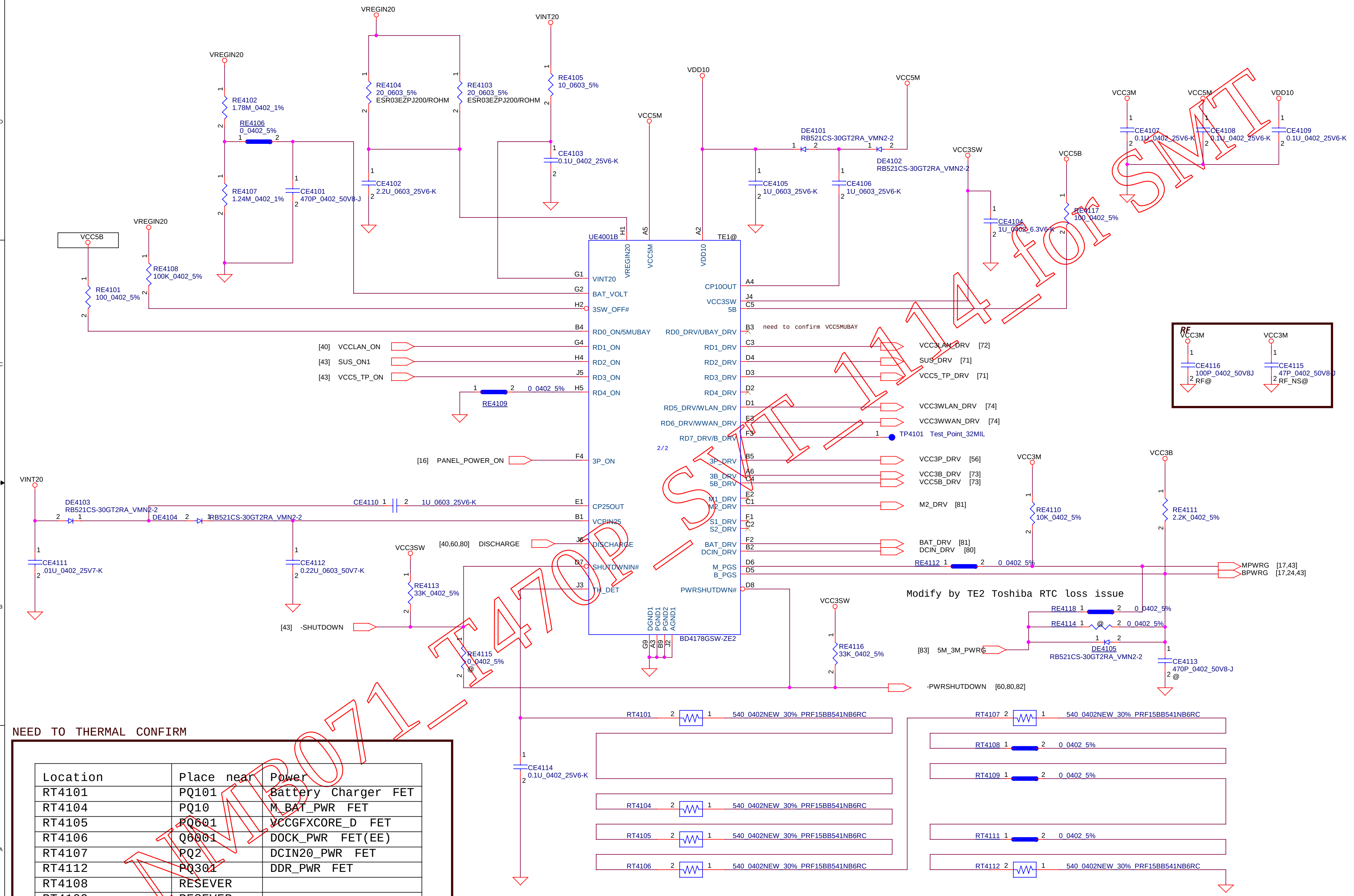


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: THINK ENGINE 2(1/2)

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 40 of 99



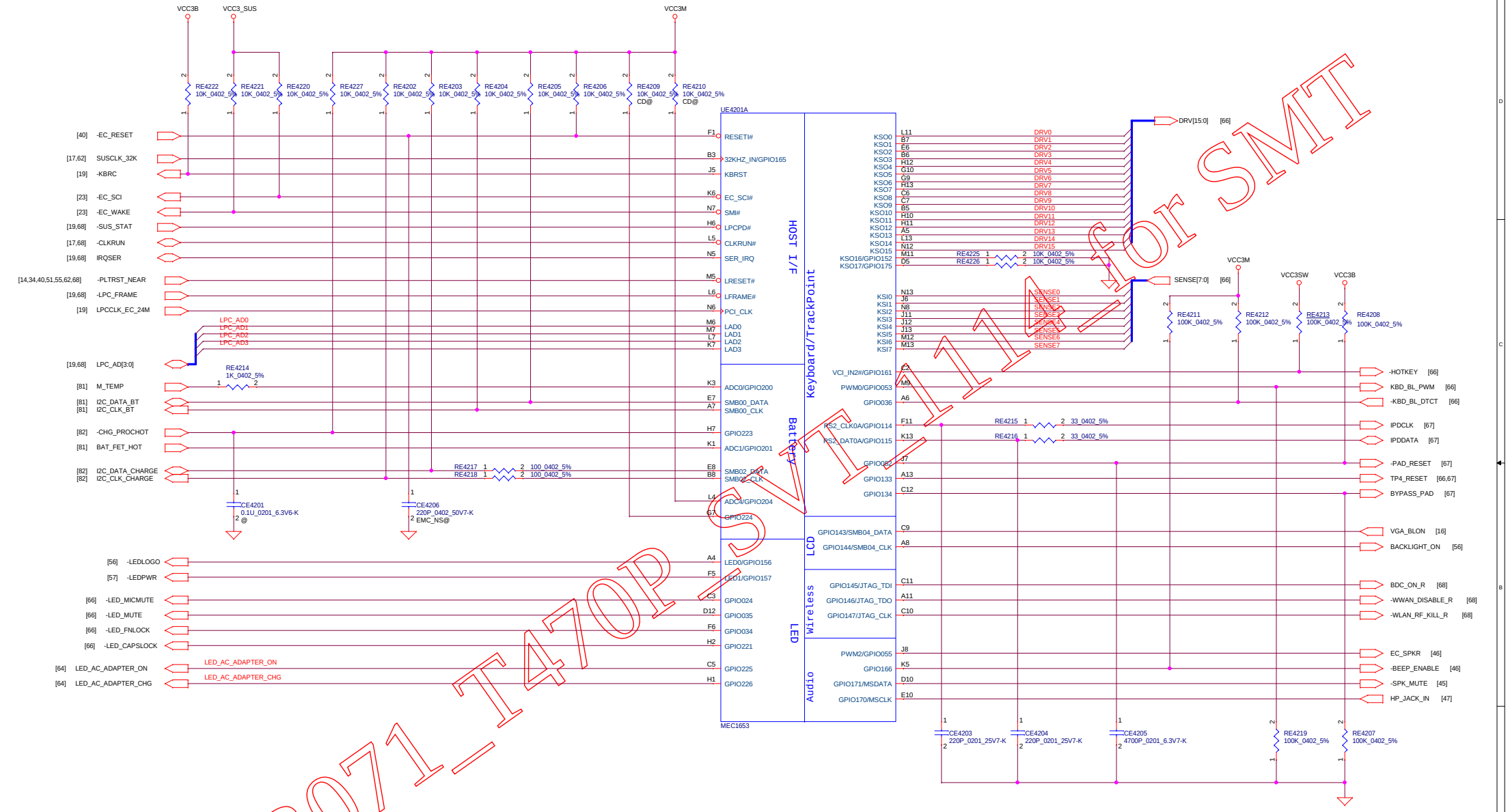
NEED TO THERMAL CONFIRM

Location	Place near	Power
RT4101	PQ101	Battery Charger FET
RT4104	PQ10	M_BAT_PWR FET
RT4105	PQ601	VCCGFXCORE_D FET
RT4106	Q6001	DOCK_PWR FET(EE)
RT4107	PQ2	DCIN20_PWR FET
RT4112	PQ301	DDR_PWR FET
RT4108	RESEVER	
RT4109	RESEVER	
RT4111	RESEVER	

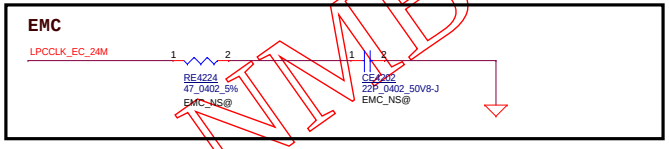
Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: THINK ENGINE 2(2/2)

Size: Custom | Document Number: NM-B071 | Rev: 0.2



EMC



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

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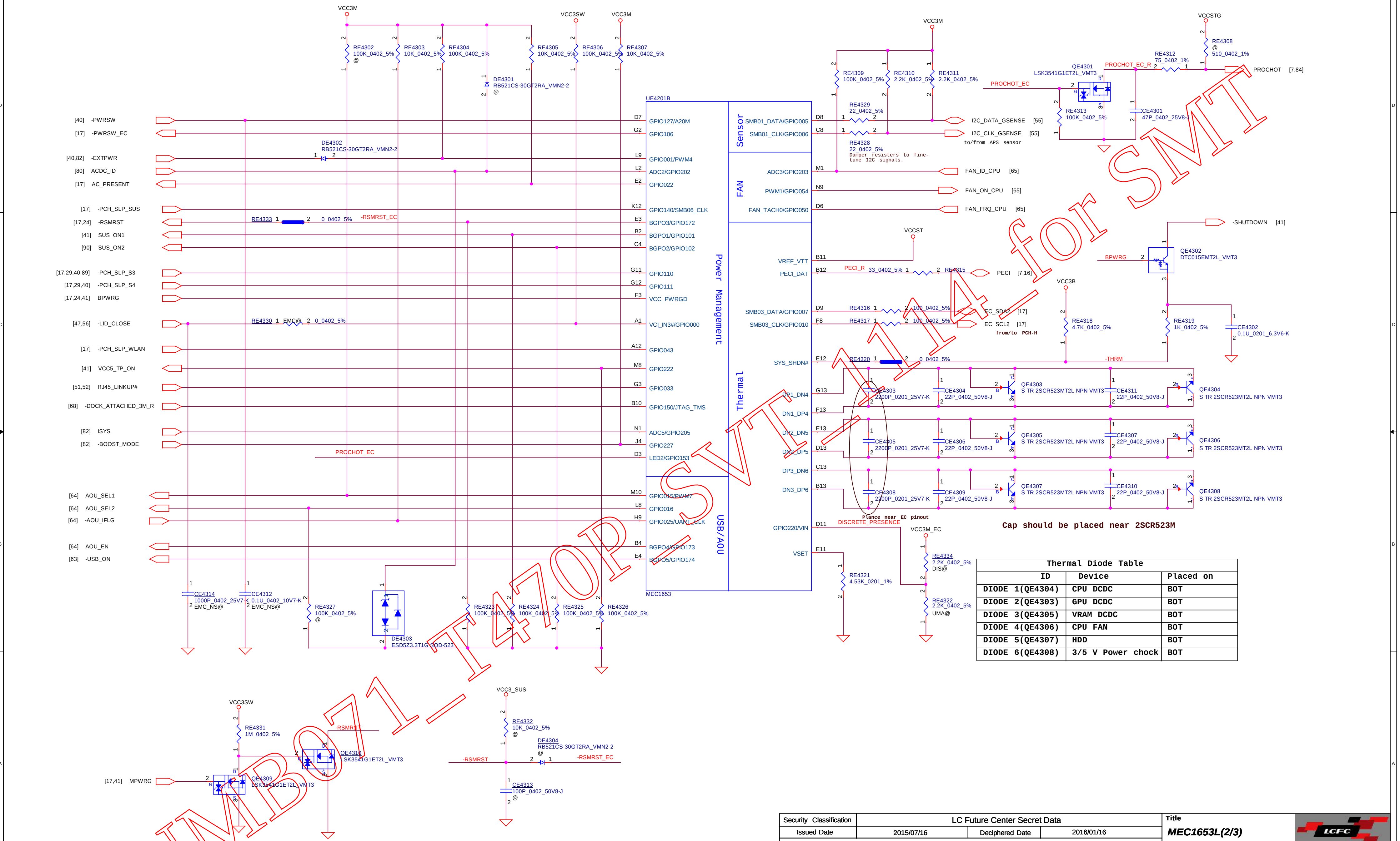
Title: **MEC1653L(1/3)**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 42 of 99



Thermal Diode Table

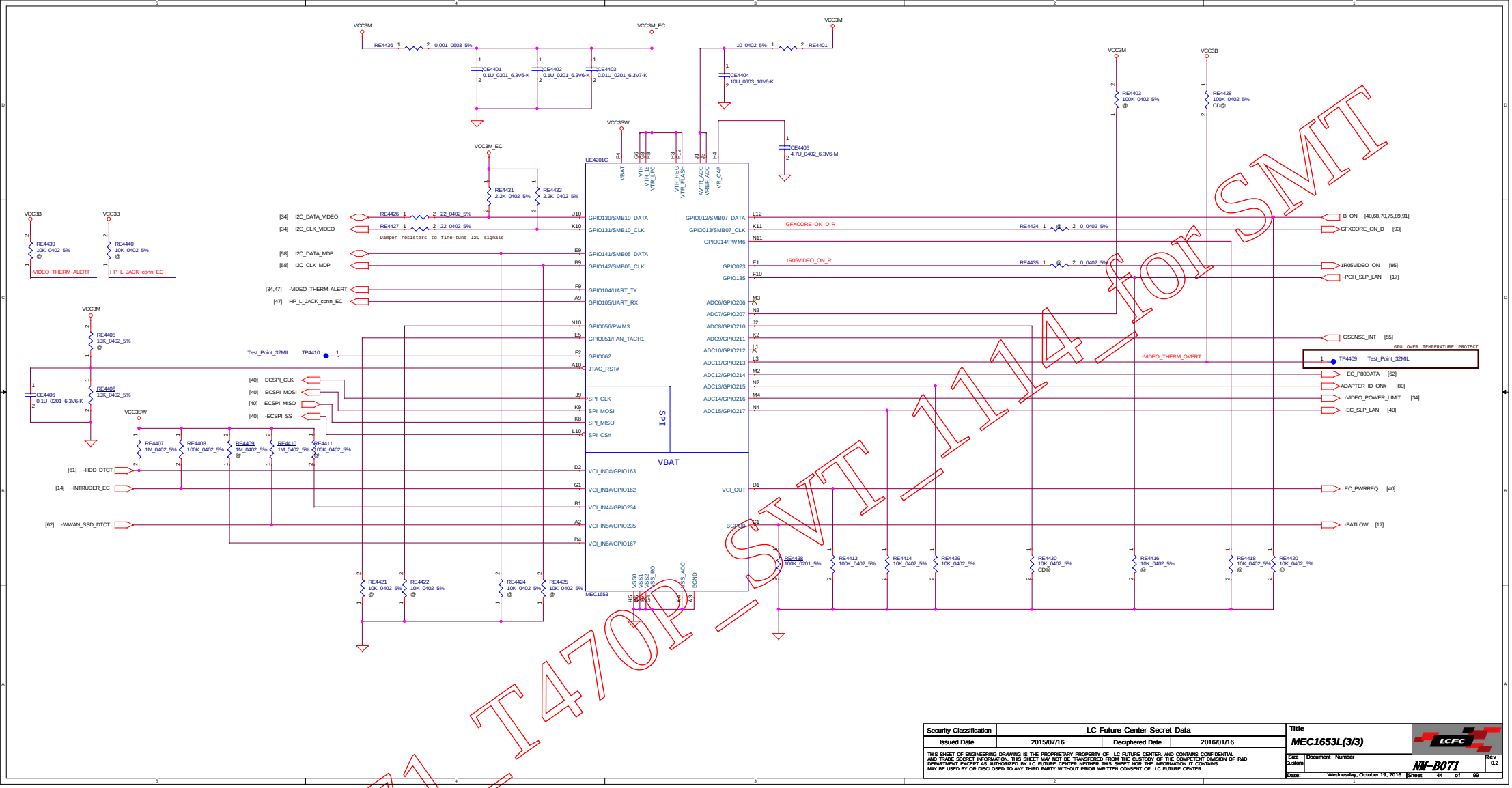
ID	Device	Placed on
DIODE 1(QE4304)	CPU DCDC	BOT
DIODE 2(QE4303)	GPU DCDC	BOT
DIODE 3(QE4305)	VRAM DCDC	BOT
DIODE 4(QE4306)	CPU FAN	BOT
DIODE 5(QE4307)	HDD	BOT
DIODE 6(QE4308)	3/5 V Power chock	BOT

Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: MEC1653L(2/3)

LCFC

Size: Custom | Document Number: NM-B071 | Rev: 0.2



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: **MEC1653L(3/3)**

Size	Document Number	Rev
Custom	NM-B071	0.2

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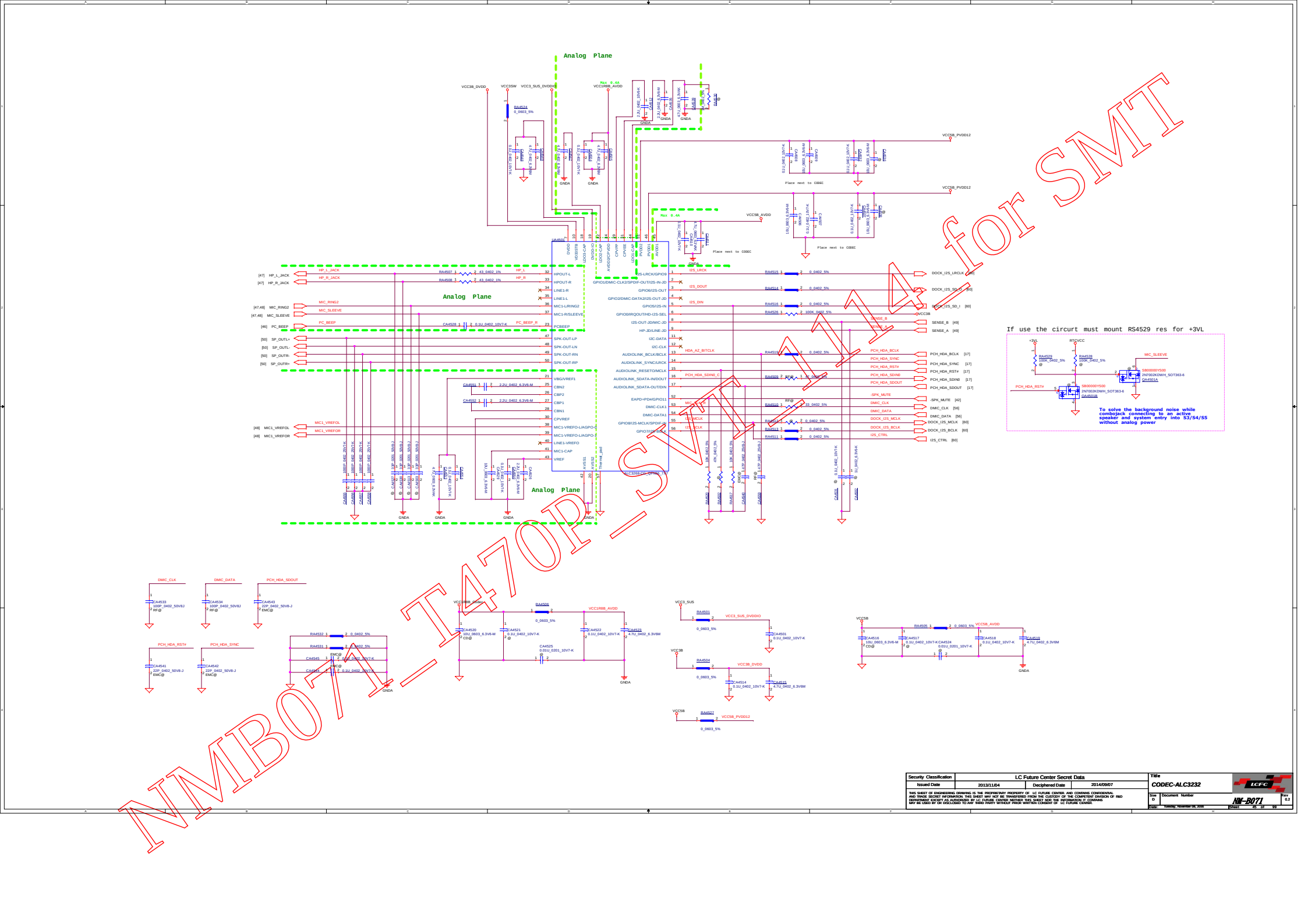
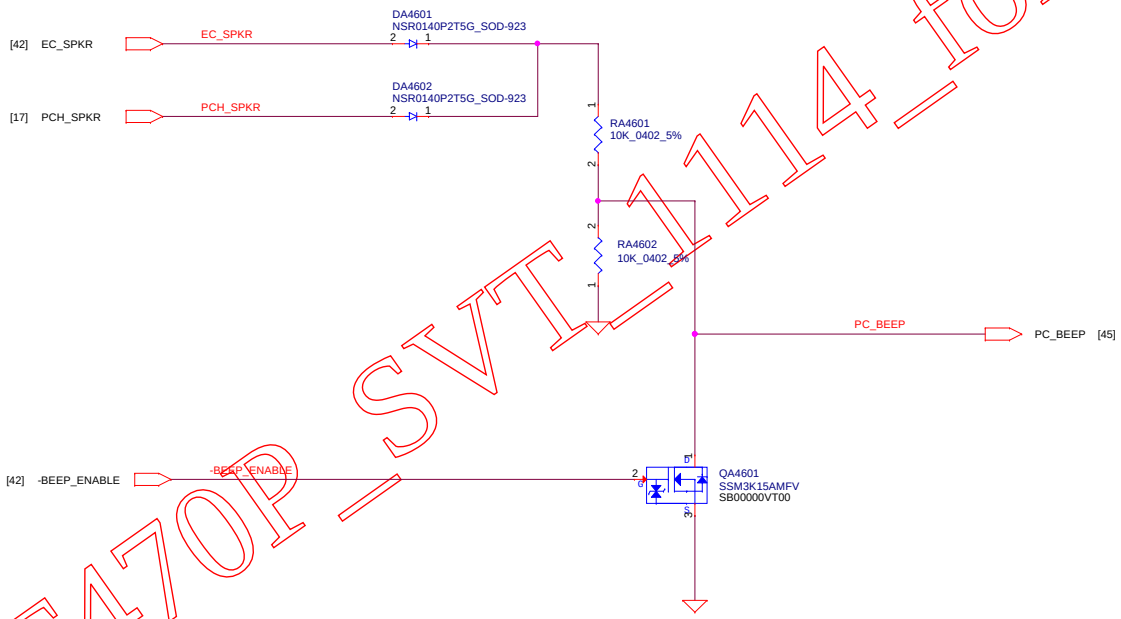


PC-BEEP

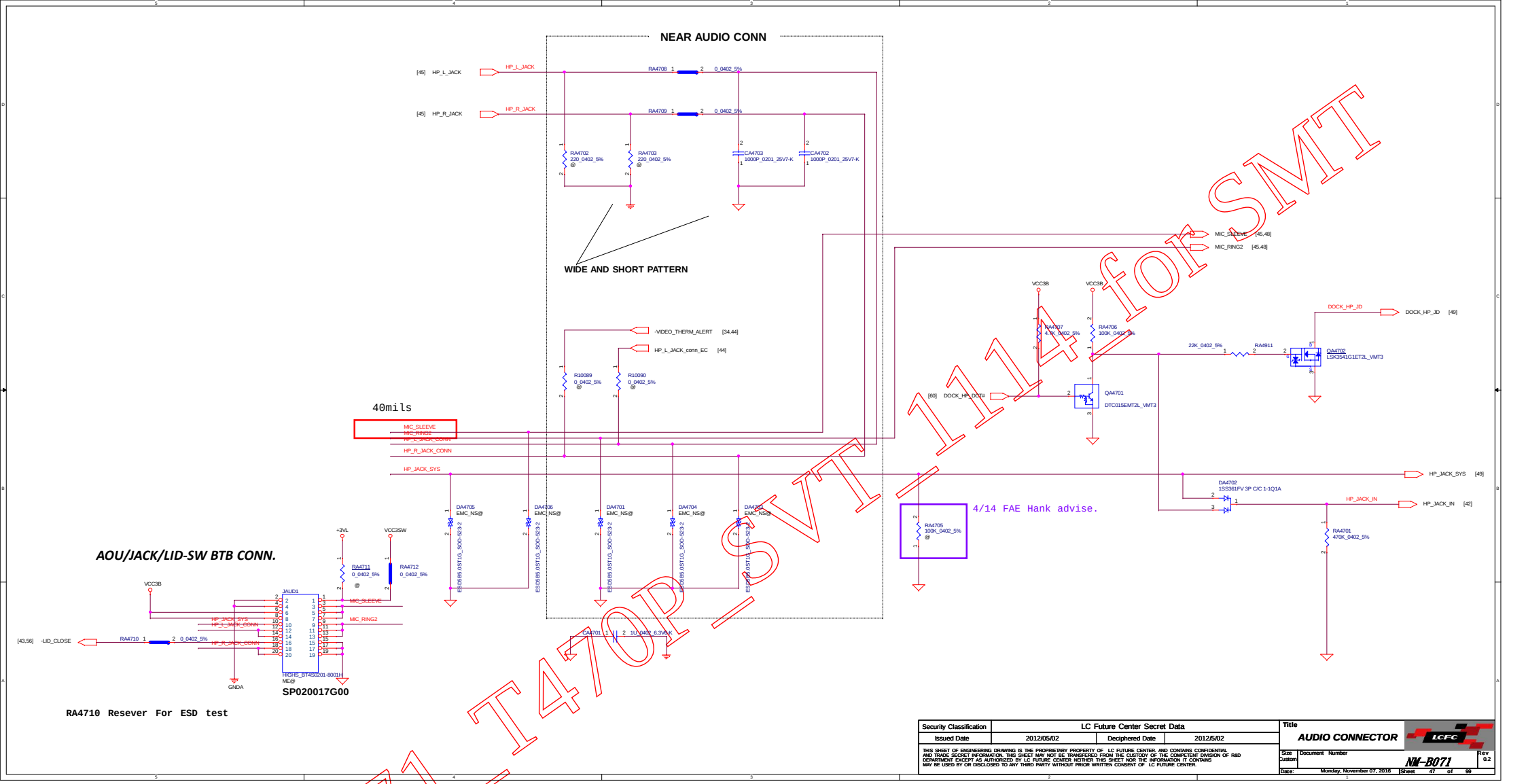


Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: **AUDIO BEEP**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 46 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

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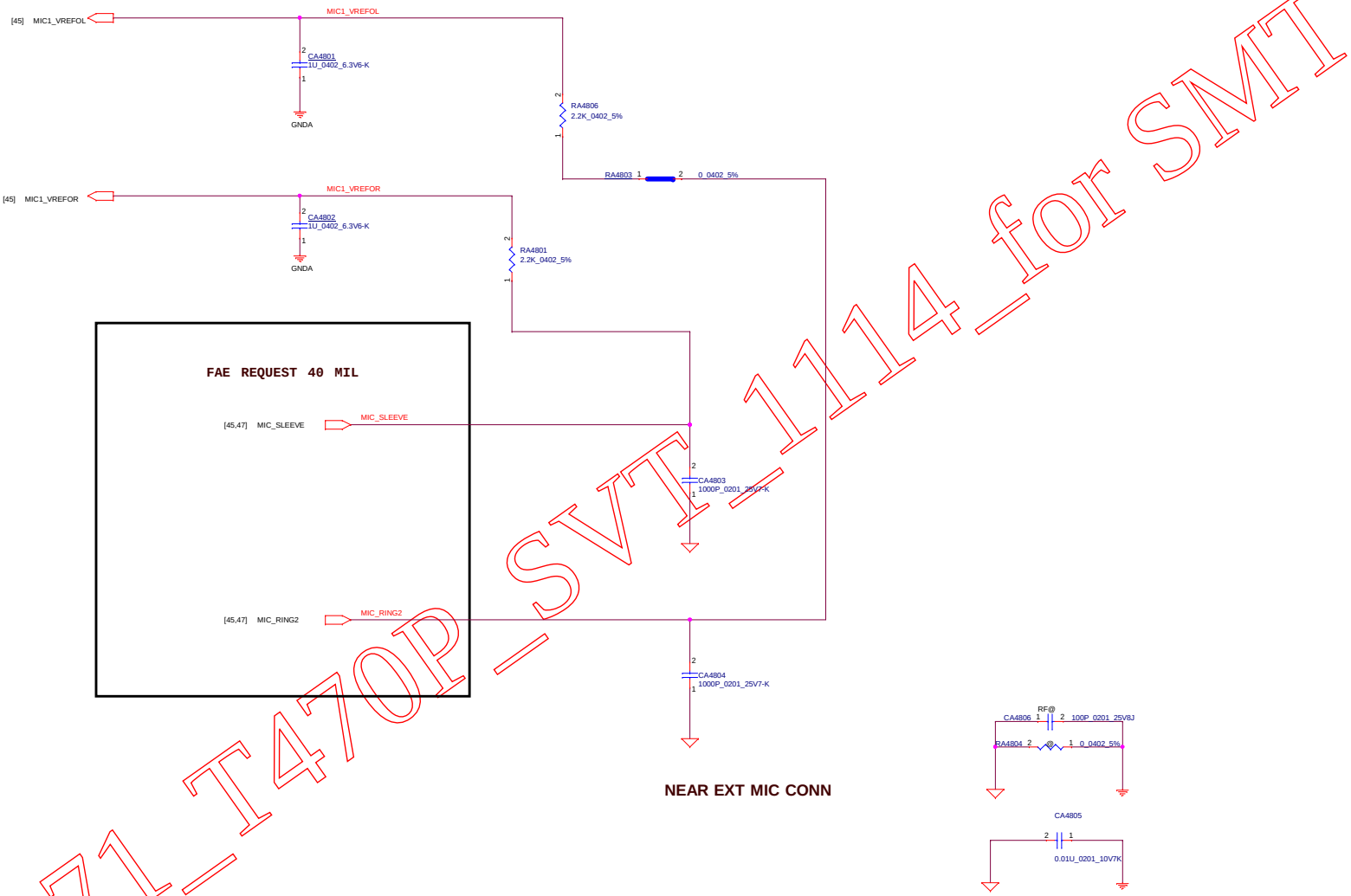
Title: **AUDIO CONNECTOR**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Monday, November 07, 2016 Sheet 47 of 99

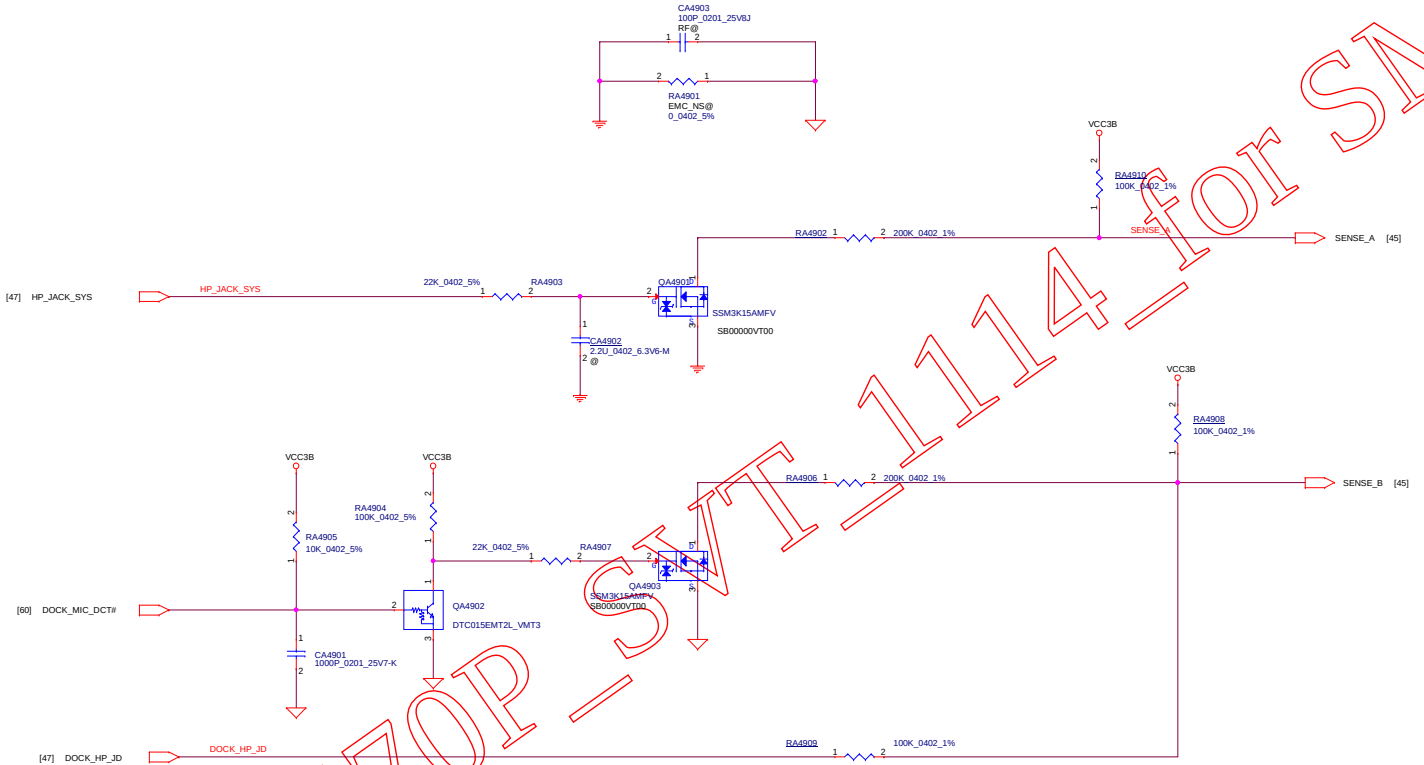


Security Classification	LC Future Center Secret Data		
Issued Date	2012/06/21	Deciphered Date	2012/06/21

Title: AUDIO EXT MIC I/F

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 48 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: **AUDIO JACK SENSE**

Size: Custom	Document Number: C NM-B071	Rev: 0.2
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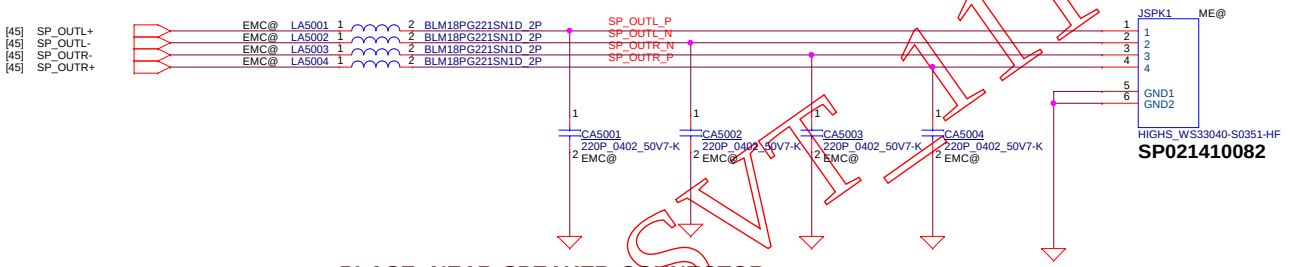
SPEAKER CONN.

Speaker 4 ohm ==> 40 mils



PLACE, NEAR SPEAKER CONNECTOR

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/02	Deciphered Date	2012/5/02

Title: **AUDIO SPEAKER**

Size: Custom	Document Number: NM-B071	Rev: 0.2
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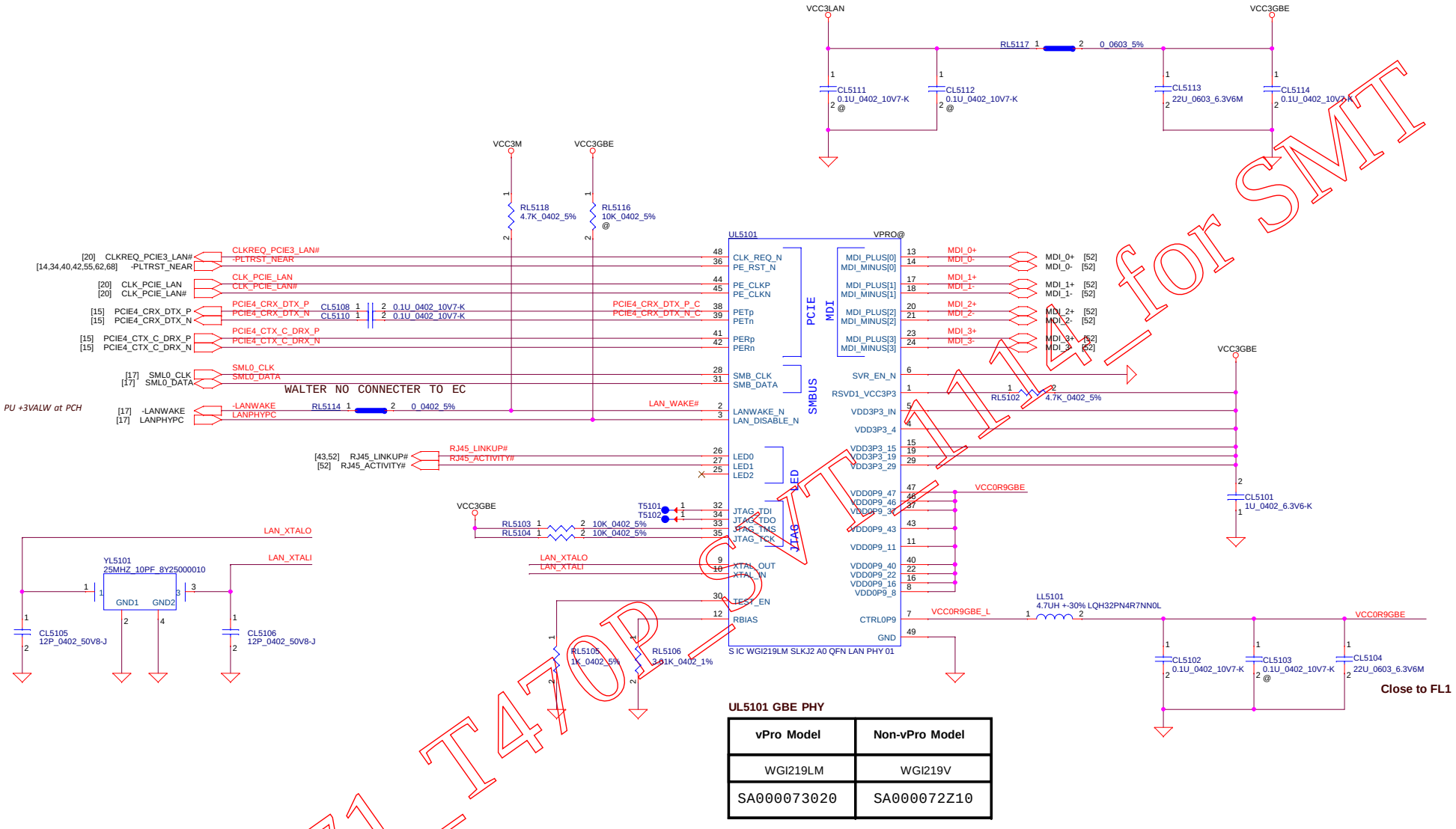


UL5101 GBE PHY

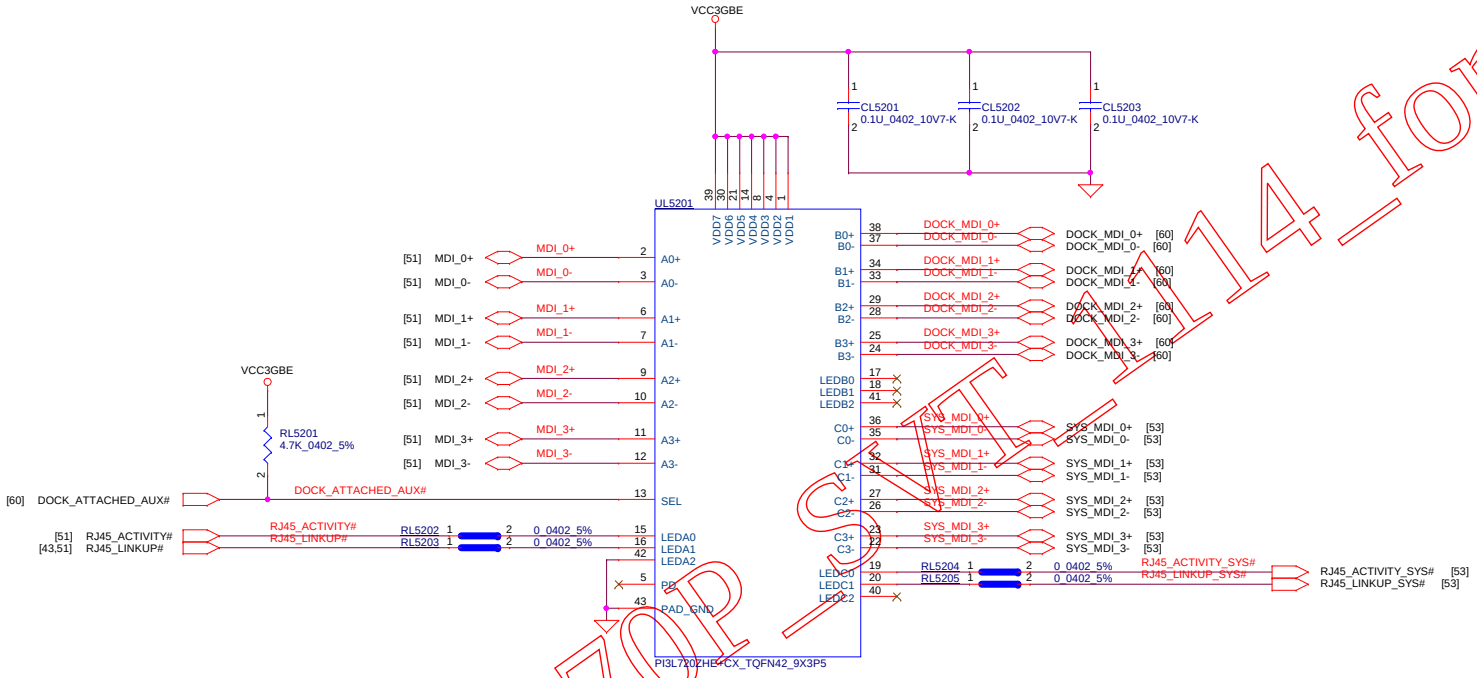
vPro Model	Non-vPro Model
WGI219LM	WGI219V
SA000073020	SA000072Z10

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **GBE LAN PHY**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 51 of 99



UL5201

Vendor	P/N	NOTE
Pericom	PI3L720ZHE, SA00003B20J	Main Source
ONSemi	NCN7201 , SA00005TF00	2nd Source (FVT)

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: GBE LAN SWITCH

Size	Document Number	Rev
Custom	NM-B071	0.2

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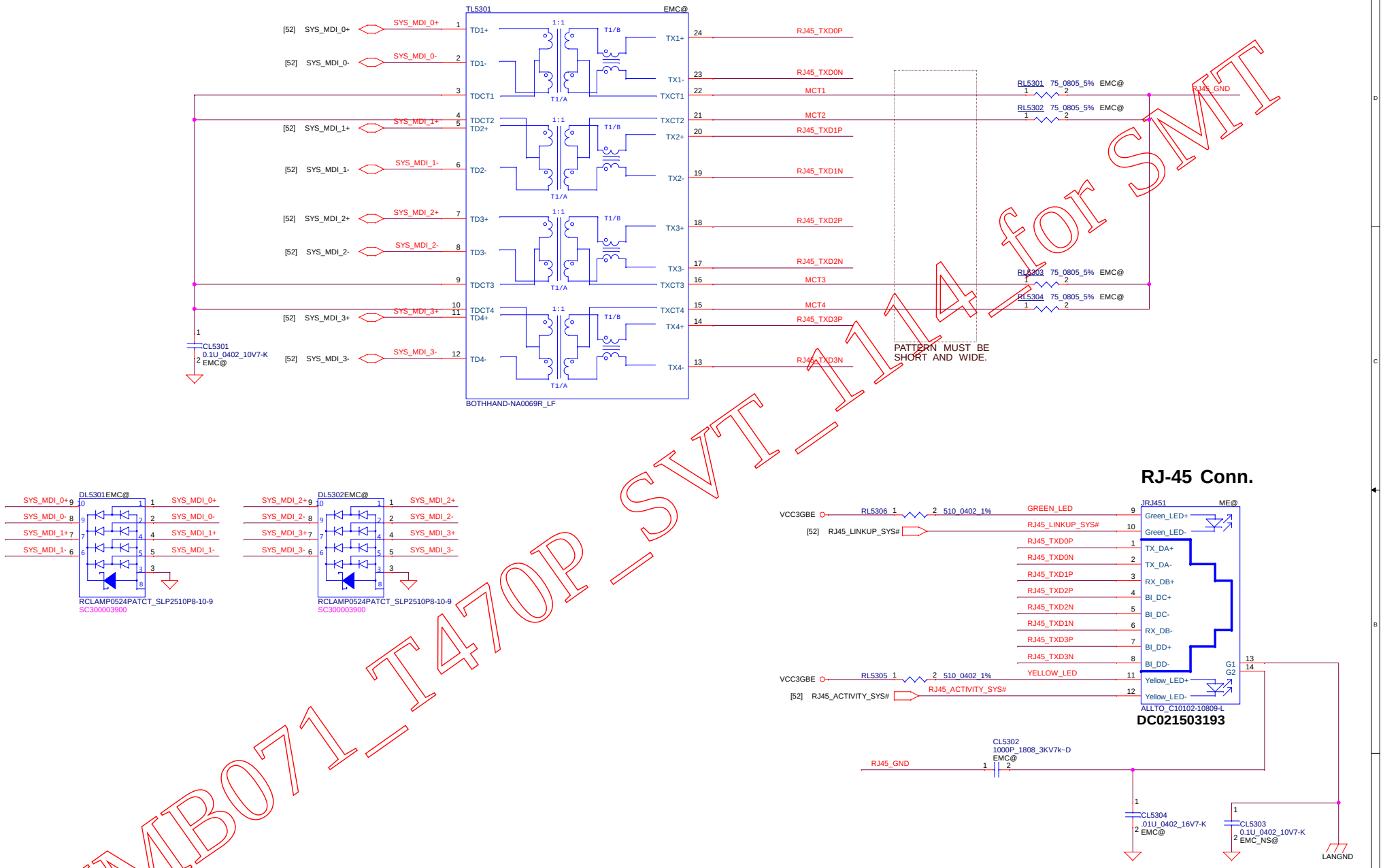

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **RJ45 CONN.**

LCFC

Size	Document Number	Rev
Custom	NM-B071	0.2

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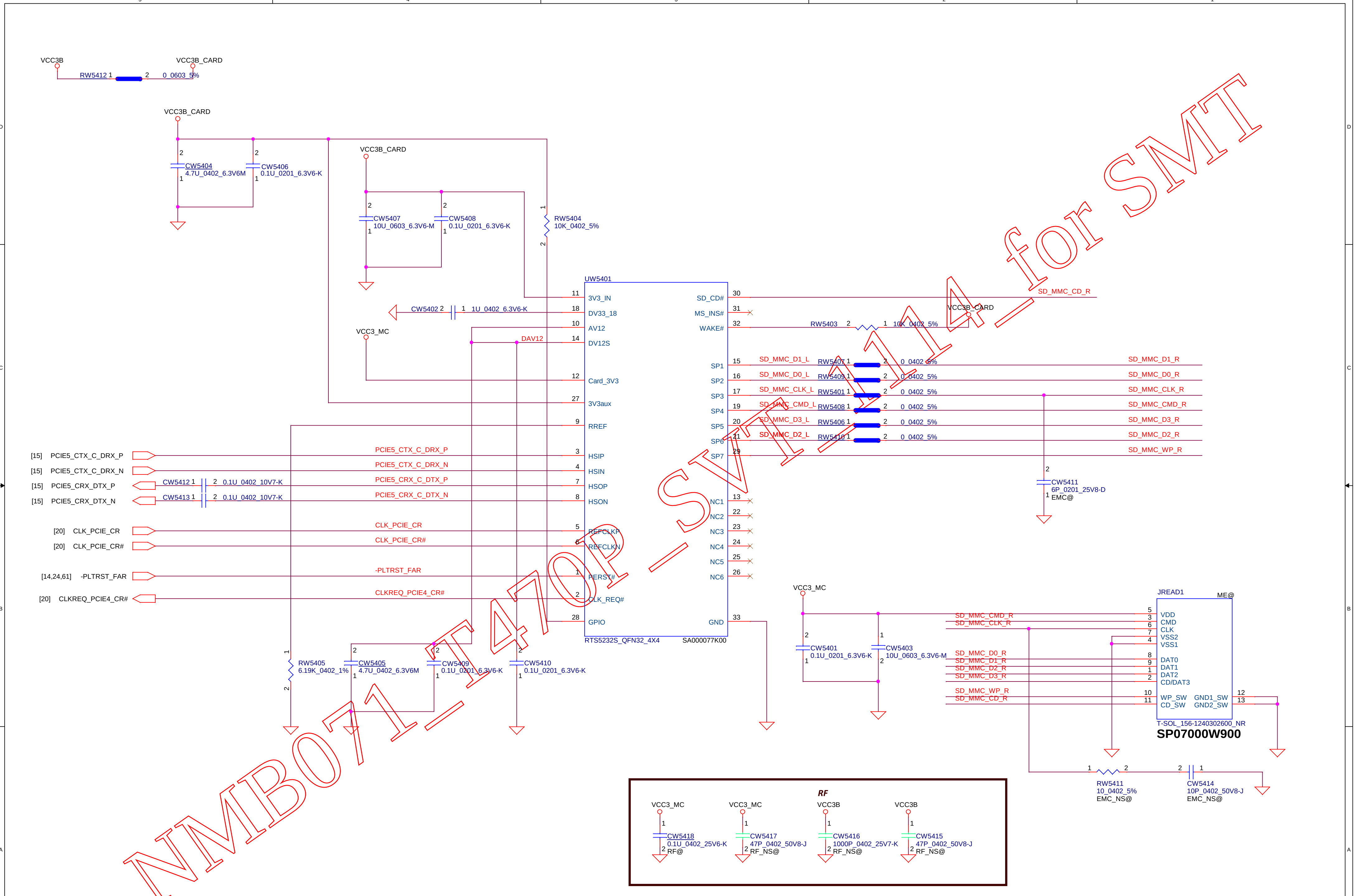

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/01	Deciphered Date	2012/12/01

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Title: RTS5232S-GR

LCFC

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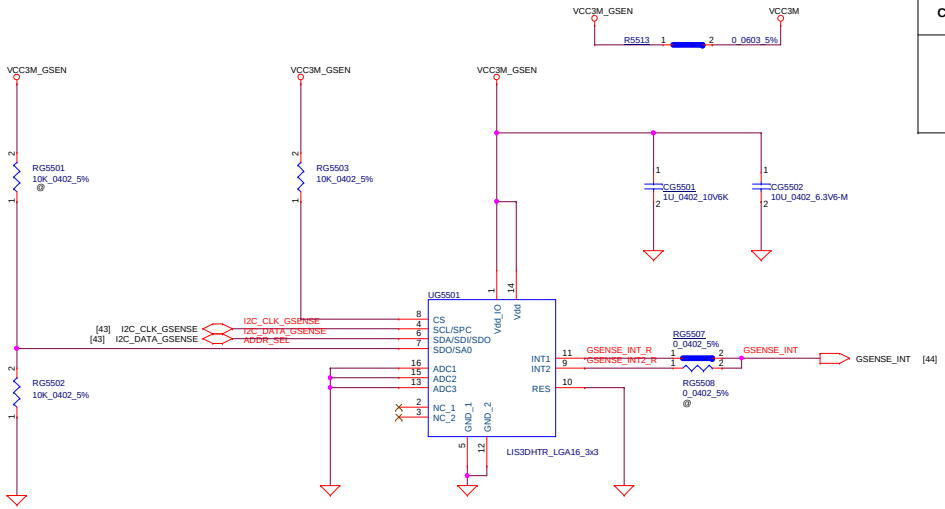
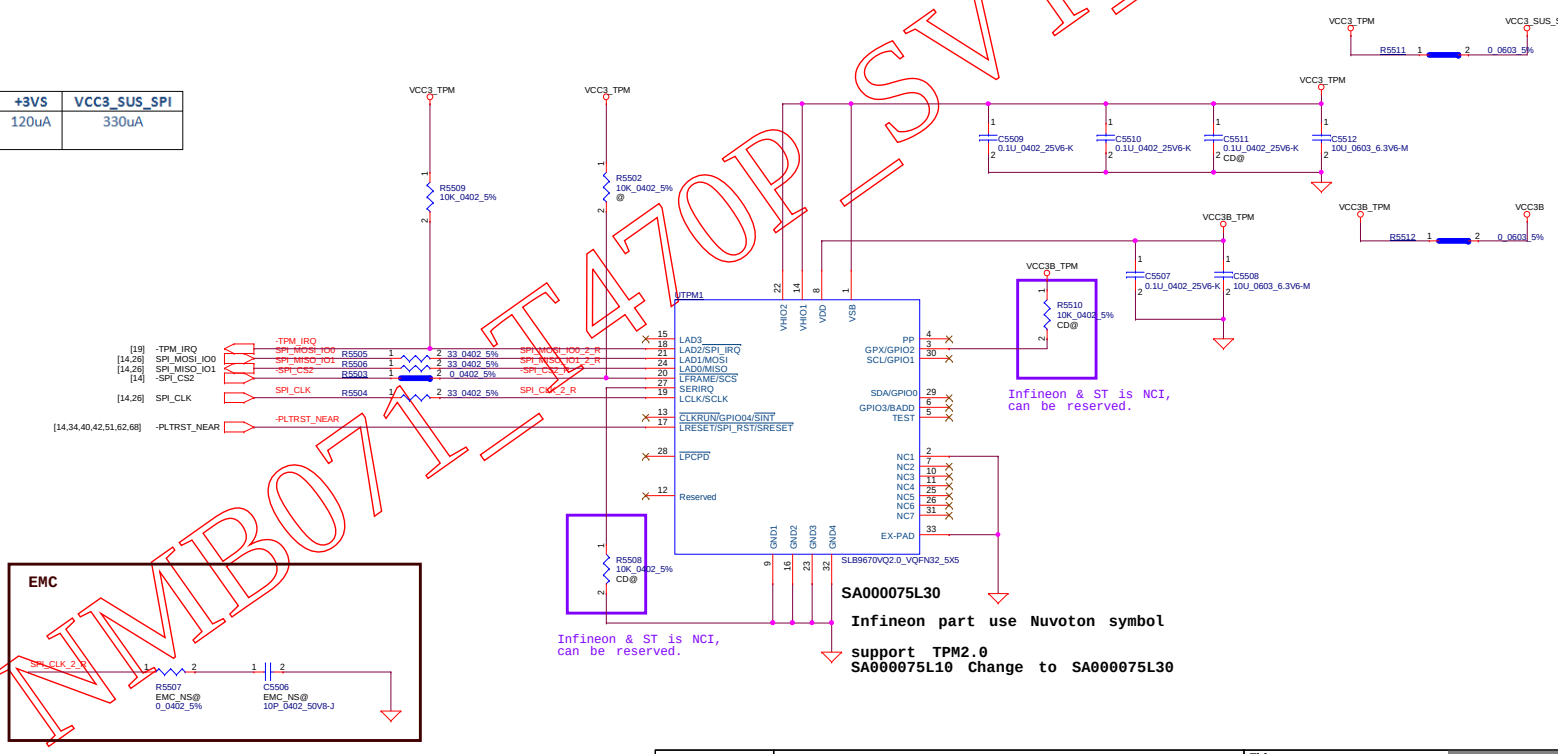
APS G-Sensor

TABLE	
CS	Mode Selection
H	I2C Mode
L	SPI Mode



TPM IC

TPM Pin8	+3VS	VCC3_SUS_SPI
S3~S5 current	120uA	330uA



SA000075L30

Infineon part use Nuvoton symbol

support TPM2.0

SA000075L10 Change to SA000075L30

Security Classification	LC Future Center Secret Data		
Issued Date	2012/05/01	Deciphered Date	2012/12/01

Title: G SENSOR/TPM

Size: Custom | Document Number: NM-B071 | Rev: 0.2

Date: Wednesday, November 02, 2016 | Sheet 55 of 99

Rds(on)=32m ohm
Max current continue=257 mA

VCC3M
VCC3P
Q5601
TPCF8002_2-3U1A
R5608 47_0402_5%
R5609 100_0402_5%
D5602 RB521CS-30GT2RA_VMN2-2
[41] VCC3P_DRV
VCC3P_DRV
C5619 0.068U_0402_25V
R5610 47K_0402_5%
VINT20
C5627 0.01U_0402_25V7K
C5628 0.1U_0402_25
C5629 1UF_25V_0603
C5624 1U_0402_10V6K
C5625 0.1U_0402_25V6-K
C5626 .01U_0402_25V7-K

eDP/CMOS/LOGO-LED CONN.

VCC3B
R5615 100K_0402_5%
R5611 10K_0402_5%
+LEDVDD
W= 80 mil
W= 40 mil
W= 60 mil
JEDP1 ME@
I-PEX_20525-040E-01
SP011408042

VINT20
2A, 80 mil
R5604 0_0603_5%
R5613 0_0603_5%
C5603 4.7U_0805_25V6-K

eDP TO BE CONFIRM

R5603 100K_0402_5%
VCC3B R5605 0_0603_5% VCC3B_DMIC
VCC3B R5601 0_0603_5% VCC3B_CMOS
VCC3P VCC3P
VCC3M R5606 1K_0402_5% VCC3M_LOGO
R5617 0_0402_5%
R5618 0_0603_5%

[42] -LEDLOGO -LEDLOGO
[42] BACKLIGHT_ON BACKLIGHT_ON
[16] PANEL_BKLT_CTRL PANEL_BKLT_CTRL
[45] DMIC_DATA DMIC_DATA
[45] DMIC_CLK DMIC_CLK
R5619 EMC@ 33_0402_5%
R5612 0_0402_5%
USB20_N7_CMOS
USB20_P7_CMOS

[15] USB20_N7 USB20_N7 L5601 EMC@
[15] USB20_P7 USB20_P7
EXC24CH900U_4P
SM070003X00

[6] CPU_EDP_AUX# CPU_EDP_AUX#
[6] CPU_EDP_AUX CPU_EDP_AUX
[18] CPU_EDP_HPD CPU_EDP_HPD
C5604 0.1U_0402_10V7-K
C5605 0.1U_0402_10V7-K
CPU_EDP_AUX#_CON
CPU_EDP_AUX_CON

[6] CPU_EDP_TX0- CPU_EDP_TX0-
[6] CPU_EDP_TX0+ CPU_EDP_TX0+
C5608 0.1U_0402_10V7-K
C5609 0.1U_0402_10V7-K
CPU_EDP_TX0-_CON
CPU_EDP_TX0+_CON

[6] CPU_EDP_TX1- CPU_EDP_TX1-
[6] CPU_EDP_TX1+ CPU_EDP_TX1+
C5606 0.1U_0402_10V7-K
C5607 0.1U_0402_10V7-K
CPU_EDP_TX1-_CON
CPU_EDP_TX1+_CON

[6] CPU_EDP_TX2- CPU_EDP_TX2-
[6] CPU_EDP_TX2+ CPU_EDP_TX2+
C5621 0.1U_0402_10V7-K
C5620 0.1U_0402_10V7-K
CPU_EDP_TX2-_CON
CPU_EDP_TX2+_CON

[6] CPU_EDP_TX3- CPU_EDP_TX3-
[6] CPU_EDP_TX3+ CPU_EDP_TX3+
C5623 0.1U_0402_10V7-K
C5622 0.1U_0402_10V7-K
CPU_EDP_TX3-_CON
CPU_EDP_TX3+_CON

[15] USB20_N9_TP USB20_N9_TP L5602 EMC@
[15] USB20_P9_TP USB20_P9_TP
EXC24CH900U_4P
SM070003X00
USB20_N9_TP_R
USB20_P9_TP_R

[19] TS_EN
[43,47] -LID_CLOSE
D5603
DAP222MGT2L_VMD3

VCC3B R5614 0_0603_5% VCC3B_TS
VCC3P R5616 @ 0_0603_5%

C5633 EMC_NS@ 33P_0402_50V8-J
C5631 EMC_NS@ 33P_0402_50V8-J
C5632 EMC_NS@ 1000P_0402_25V7-K
C5630 @ 1000P_0402_25V7-K
D5601 PESD5V0U2BT_SOT23-3 EMC@

RF
+LEDVDD
VCC3B_CMOS
C5610 100P_0402_50V8J RF@
C5611 47P_0402_50V8-J RF_NS@
C5612 100P_0402_50V8J RF@
C5613 47P_0402_50V8-J RF_NS@

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title	eDP/CMOS/LOGO-LED CONN.		
Size	Document Number		Rev
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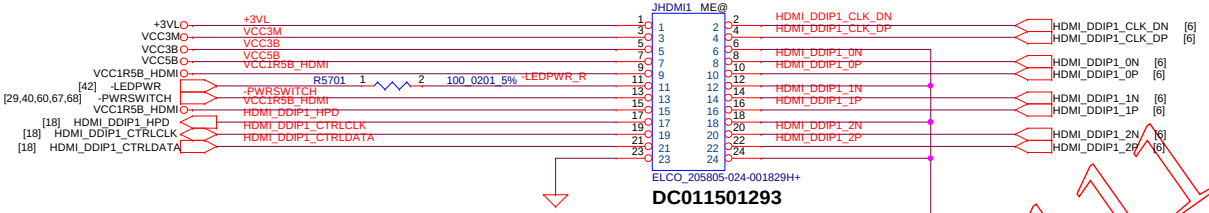
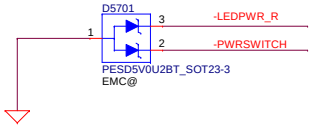
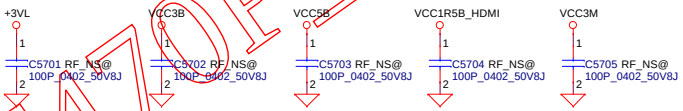
M/B TO HDMI/B BTB CONN.



DC011501293





Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: HDMI BTB CONN.

Size	Document Number	Rev
Custom	NM-B071	0.2

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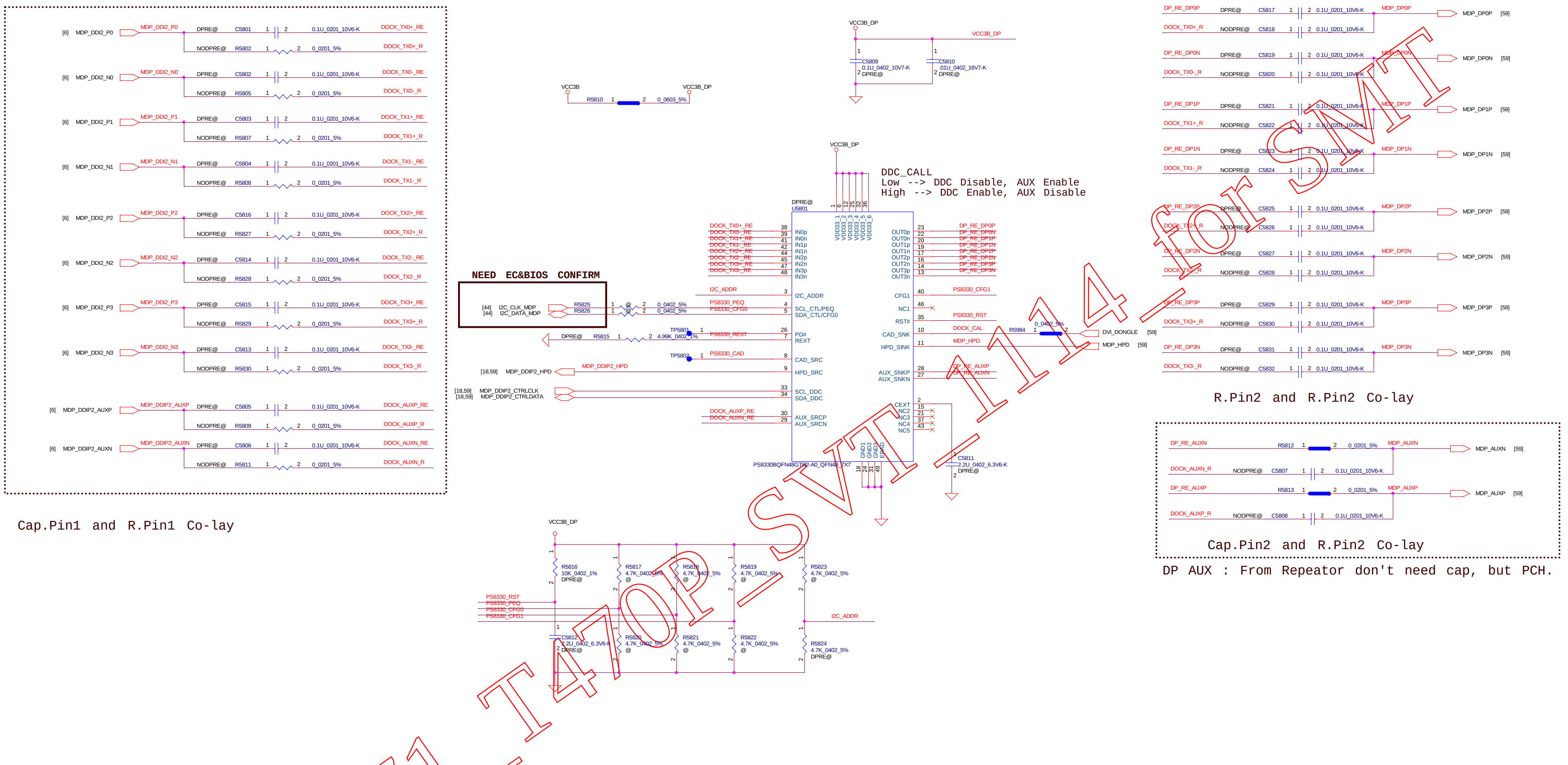
MDP_DDI2_P0
MDP_DDI2_N0
MDP_DDI2_P1
MDP_DDI2_N1
MDP_DDI2_P2
MDP_DDI2_N2
MDP_DDI2_P3
MDP_DDI2_N3
MDP_DDIP2_AUXP
MDP_DDIP2_AUXN
DOCK_TX0+_RE
DOCK_TX0+_R
DOCK_TX0-_RE
DOCK_TX0-_R
DOCK_TX1+_RE
DOCK_TX1+_R
DOCK_TX1-_RE
DOCK_TX1-_R
DOCK_TX2+_RE
DOCK_TX2+_R
DOCK_TX2-_RE
DOCK_TX2-_R
DOCK_TX3+_RE
DOCK_TX3+_R
DOCK_TX3-_RE
DOCK_TX3-_R
DOCK_AUXP_RE
DOCK_AUXP_R
DOCK_AUXN_RE
DOCK_AUXN_R
DPRE@
NODPRE@
0.1U_0201_10V6-K
0_0201_5%
Cap.Pin1 and R.Pin1 Co-lay
NEED EC&BIOS CONFIRM
I2C_CLK_MDP
I2C_DATA_MDP
MDP_DDIP2_HPD
MDP_DDIP2_CTRLCLK
MDP_DDIP2_CTRLDATA
VCC3B
VCC3B_DP
R5810
0_0603_5%
C5809
0.1U_0402_10V7-K
C5810
.01U_0402_16V7-K
DDC_CALL
Low --> DDC Disable, AUX Enable
High --> DDC Enable, AUX Disable
U5801
PS8330BQFN48GTR2-A0_QFN48_7X7
I2C_ADDR
PS8330_PEQ
PS8330_CFG0
PS8330_REXT
PS8330_CAD
PS8330_CFG1
PS8330_RST
DOCK_CAL
MDP_HPD
DVI_DONGLE
R5984
0_0402_5%
C5811
2.2U_0402_6.3V6-K
DP_RE_DP0P
DP_RE_DP0N
DP_RE_DP1P
DP_RE_DP1N
DP_RE_DP2P
DP_RE_DP2N
DP_RE_DP3P
DP_RE_DP3N
DP_RE_AUXP
DP_RE_AUXN
MDP_DP0P
MDP_DP0N
MDP_DP1P
MDP_DP1N
MDP_DP2P
MDP_DP2N
MDP_DP3P
MDP_DP3N
MDP_AUXP
MDP_AUXN
R.Pin2 and R.Pin2 Co-lay
Cap.Pin2 and R.Pin2 Co-lay
DP AUX : From Repeator don't need cap, but PCH.
R5816
10K_0402_1%
R5817
R5818
R5819
R5823
R5820
R5821
R5822
R5824
4.7K_0402_5%
C5812
2.2U_0402_6.3V6-K

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

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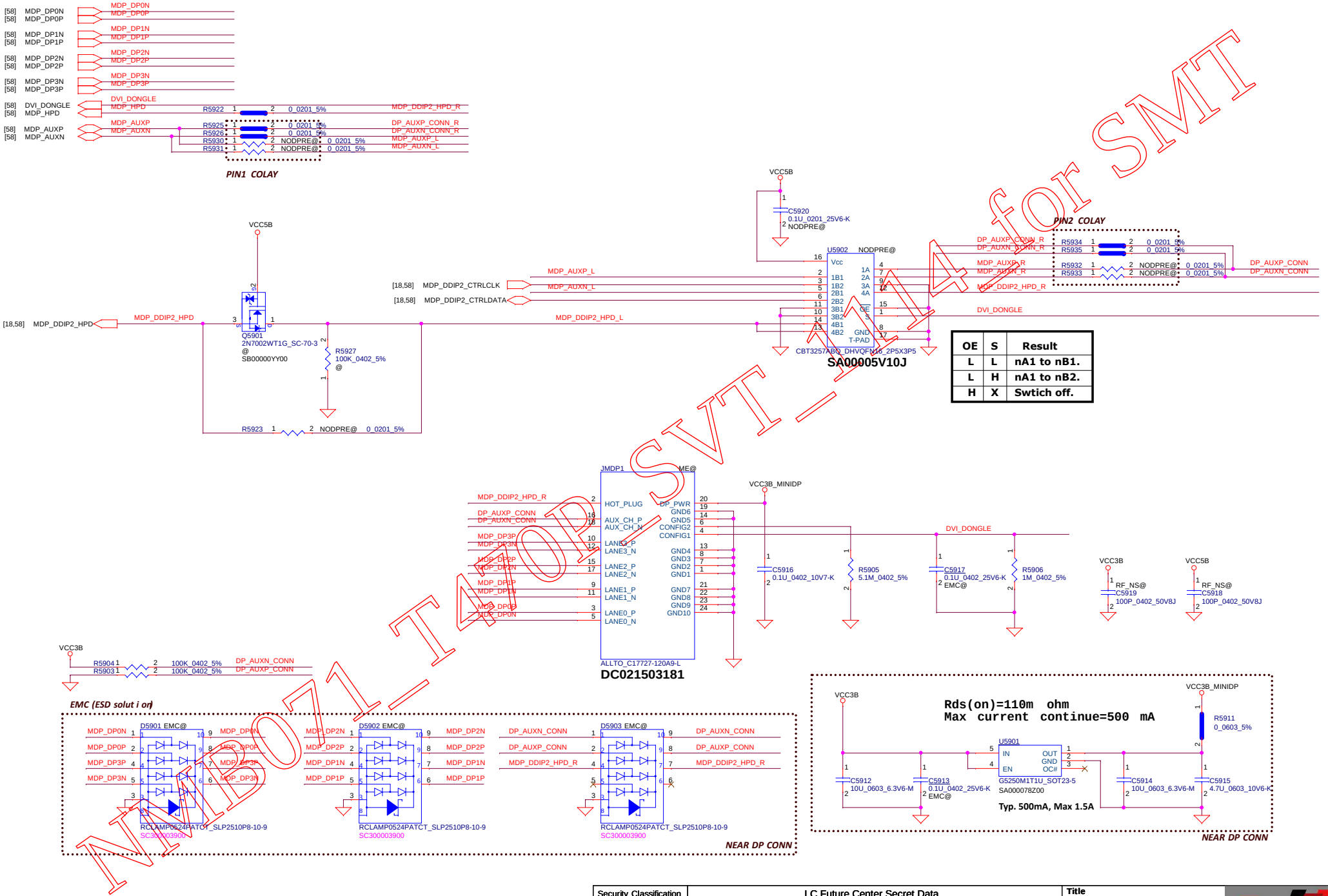
Title: **PS8330B REPEATER**

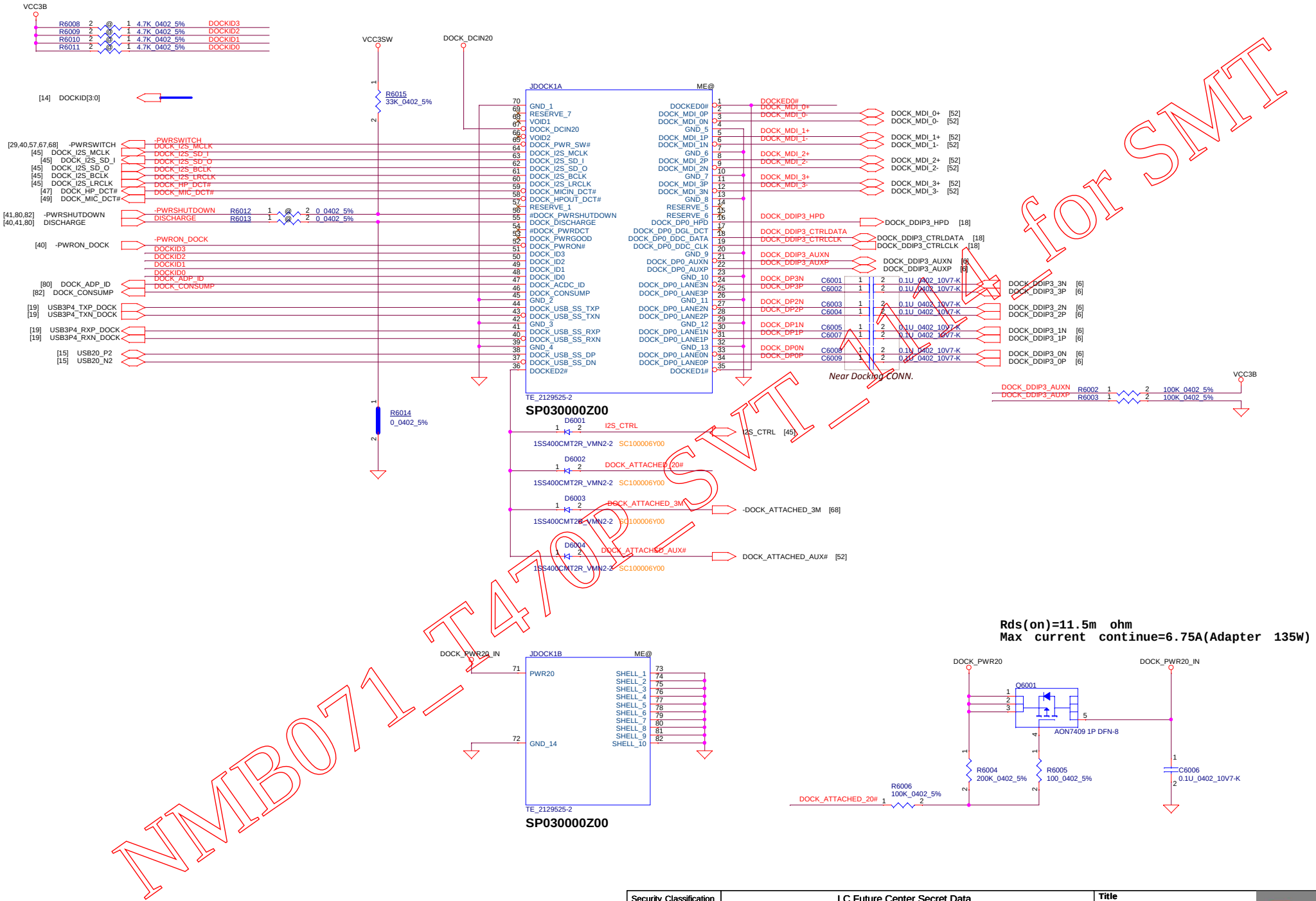
Size: Custom — Document Number: NM-B071 — Rev 0.2

Date: Wednesday, October 12, 2016 — Sheet 58 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title	MINI-DP/CONN.		
Size	Document Number		Rev
Custom	NM-B071		0.2
Date:	Wednesday, October 12, 2016	Sheet	59 of 99



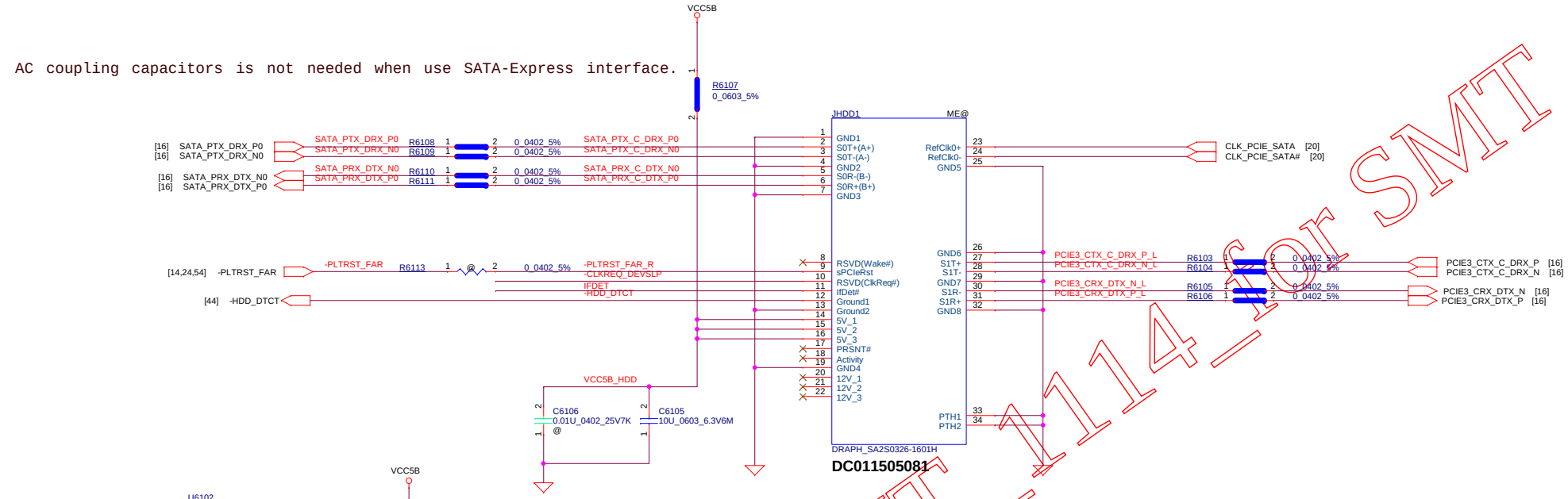
Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

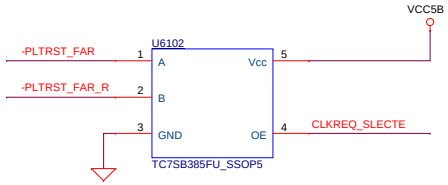
Title: **DOCKING CONN.**

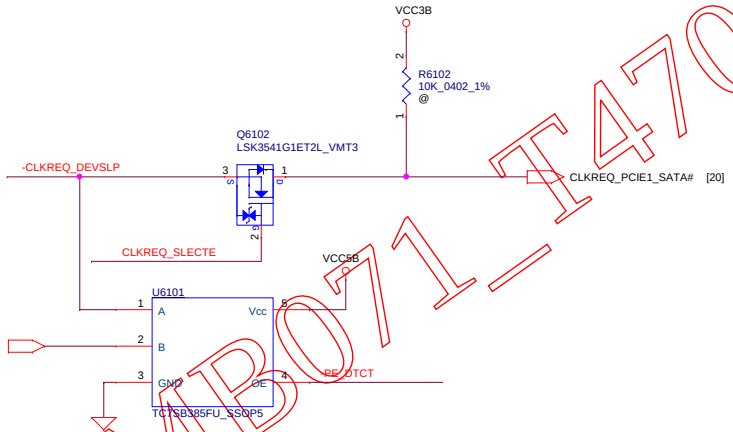
Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 60 of 99

AC coupling capacitors is not needed when use SATA-Express interface.

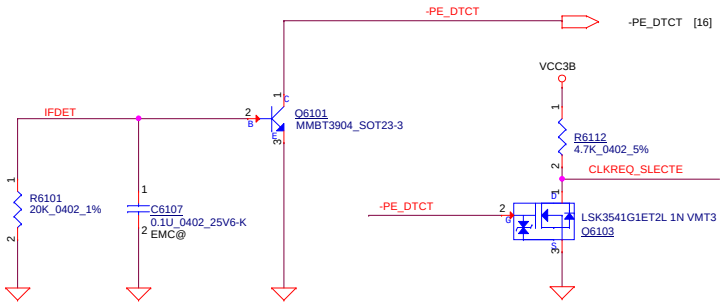






Input	Function
OE	
L	Disconnect
H	A port = B port

IFDET
SATA Device GND
PCIe Device 5K PU to Vsource



Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: **SATA HDD CONN.**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 61 of 99

TYPE-B NGFF SLOT FOR WWAN/SSD 3.2H CONNECTOR

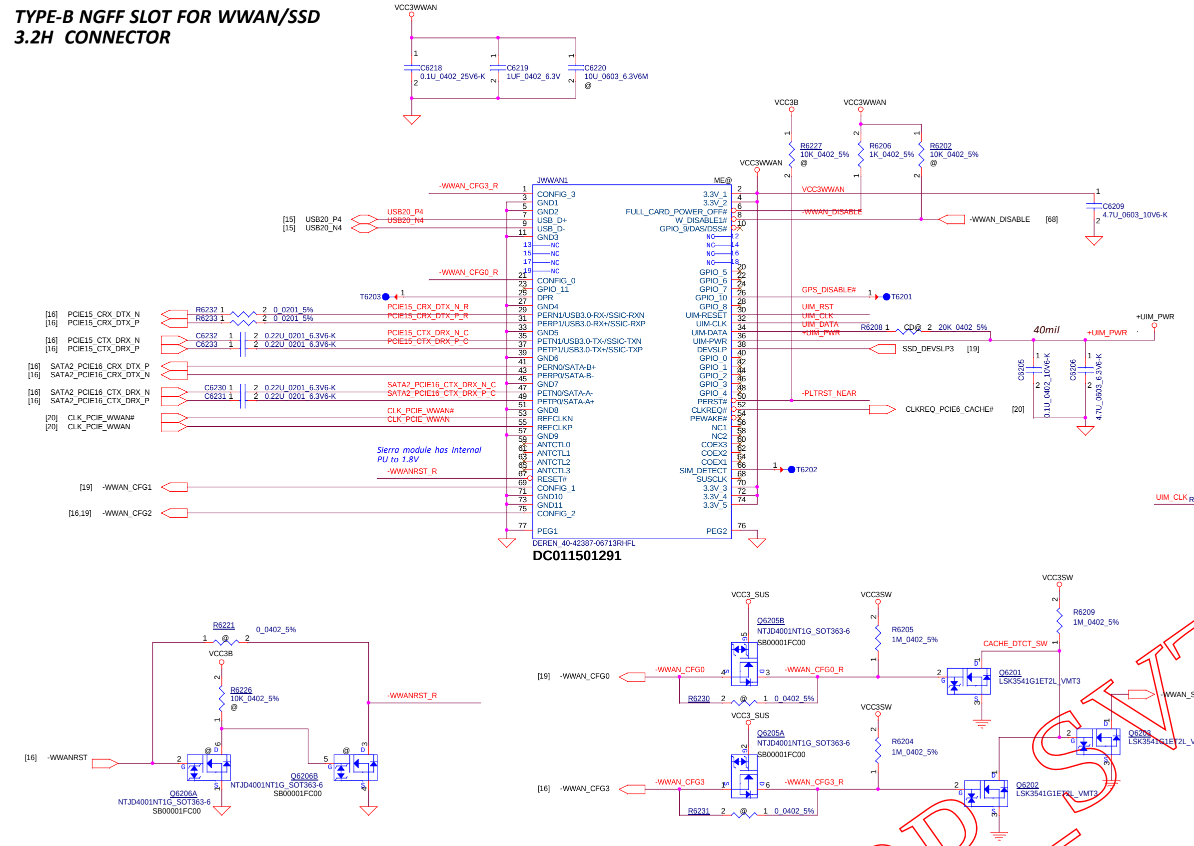
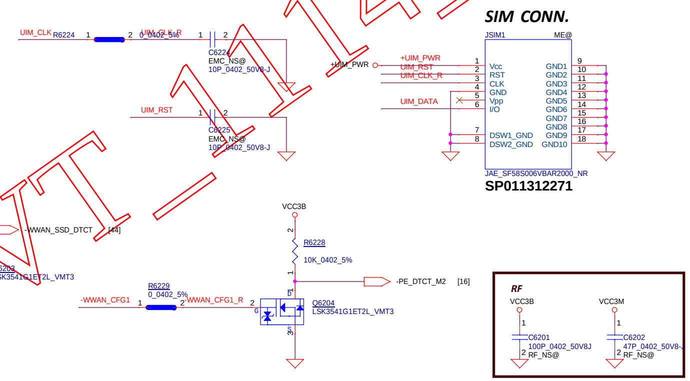


Table 27. Socket 2 Module Configuration

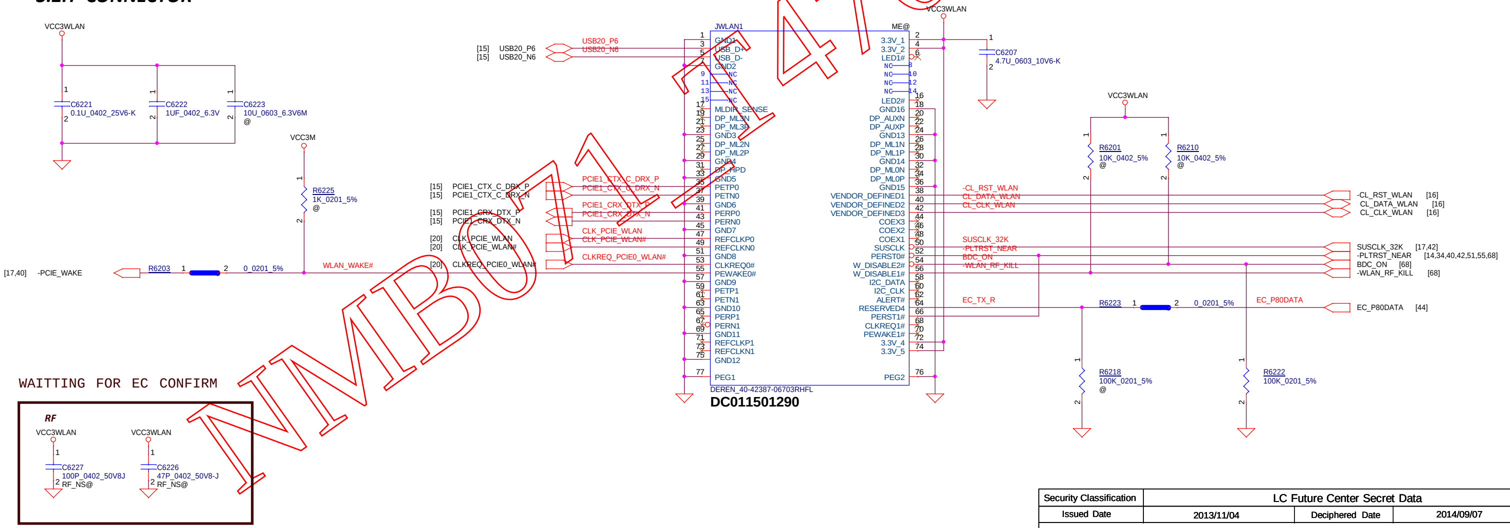
State #	Module Configuration Decodes: CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	NC	GND	GND	SSD – PCIe	N/A
2	GND	GND	NC	GND	WWAN – PCIe	0
3	GND	NC	NC	GND	WWAN – PCIe	1
4	GND	GND	GND	NC	WWAN – USB 3.0	0
5	GND	NC	GND	NC	WWAN – USB 3.0	1
6	GND	GND	NC	NC	WWAN – USB 3.0	2
7	GND	NC	NC	NC	WWAN – USB 3.0	3
8	NC	GND	GND	GND	WWAN – SSIC	0
9	NC	NC	GND	GND	WWAN – SSIC	1
10	NC	GND	NC	GND	WWAN – SSIC	2
11	NC	NC	NC	GND	WWAN – SSIC	3
12	NC	GND	GND	NC	WWAN – PCIe	2
13	NC	NC	GND	NC	WWAN – PCIe	3
14	NC	GND	NC	NC	RFU	N/A
15	NC	NC	NC	NC	No Module Present	N/A

[1] USB 2.0 supported on all WWAN configurations (HSIC supported on WWAN configuration 3)
[2] Applicable to WWAN only

SIM CONN.



TYPE-A NGFF SLOT FOR WLAN 3.2H CONNECTOR



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Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: **WWAN/WLAN NGFF CONN.**

LCFC

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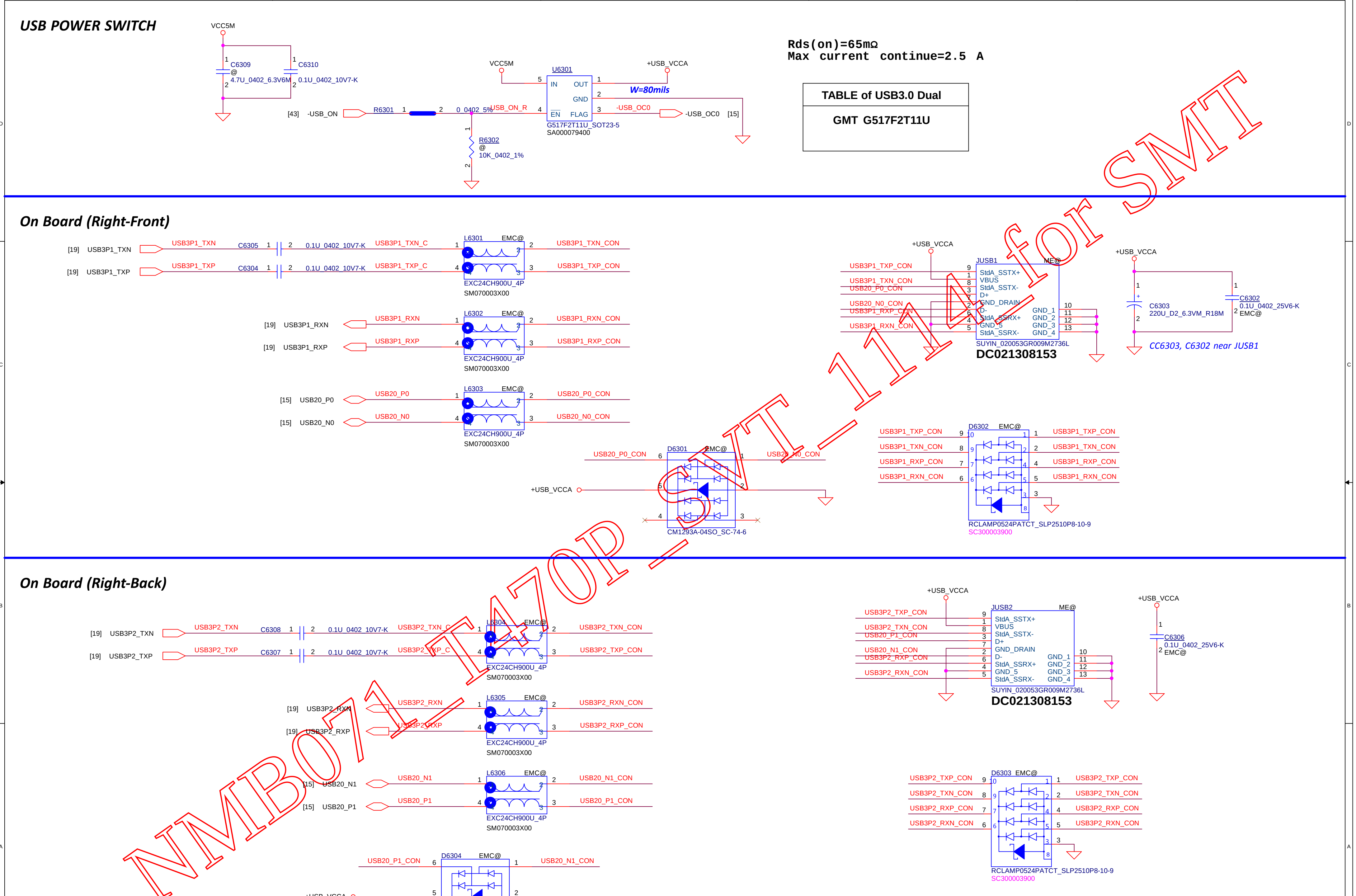


Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: **USB3 P1/2 CONN.**

LCFC

Size: Custom | Document Number: NM-B071 | Rev: 0.2

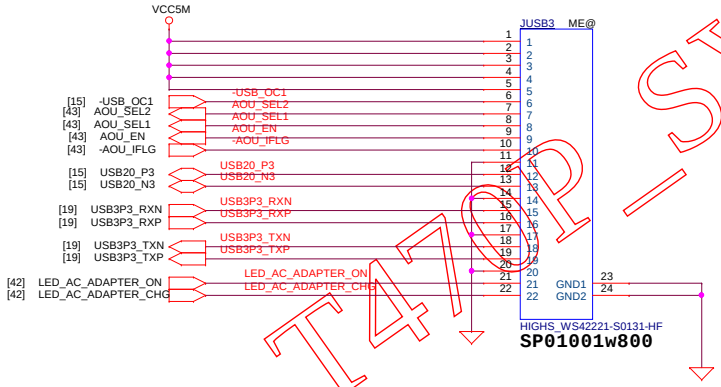
*

MB PIN number	MB PIN name	SB board pin name	SB PIN number
pin1~5	VCC5M	VCC5M	pin1~5
pin6	-USB_OC1	-USB_OC1	pin6
pin7	AOU_SEL2	AOU_SEL2	pin7
pin8	AOU_SEL1	AOU_SEL1	pin8
pin9	AOU_EN	AOU_EN	pin9
pin10	-AOU_IFLG	-AOU_IFLG	pin10
pin11	GND	GND	pin11
pin12	USB20_P3	USB20_P3	pin12
pin13	USB20_N3	USB20_N3	pin13
pin14	GND	GND	pin14
pin15	USB3P3_RXN	USB3P3_RXN	pin19
pin16	USB3P3_RXP	USB3P3_RXP	pin18
pin17	GND	GND	pin17
pin18	USB3P3_TXN	USB3P3_TXN	pin16
pin19	USB3P3_TXP	USB3P3_TXP	pin15
pin20	GND	GND	pin20
pin21	LED_AC_ADAPTER_ON	LED_AC_ADAPTER_ON	pin21
pin22	LED_AC_ADAPTER_CHG	LED_AC_ADAPTER_CHG	pin22

*

USB board and MB board is wire to board connector.
Due to USB board layout issue so pin define can*t meet MB

USB LEFT PORT



Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: USB3 P3 CONN.

Size	Document Number	Rev
Custom	NM-B071	0.2

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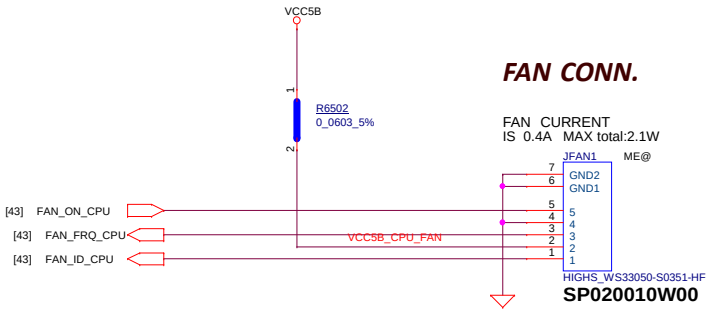

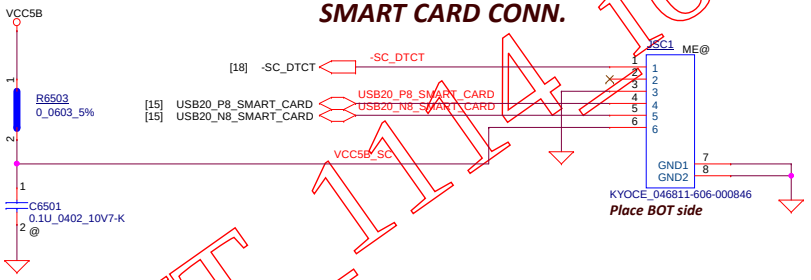

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: FAN/SC CONN

Size	Document Number	Rev
Custom	NM-B071	0.2

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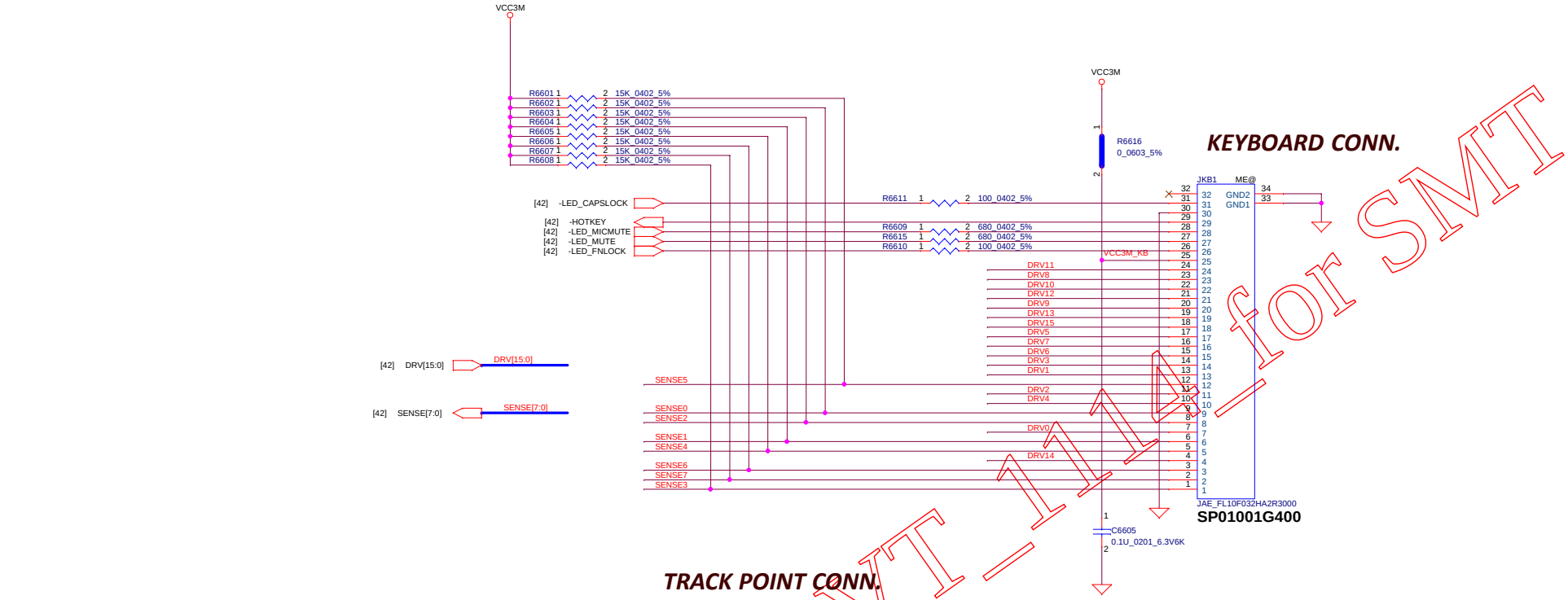

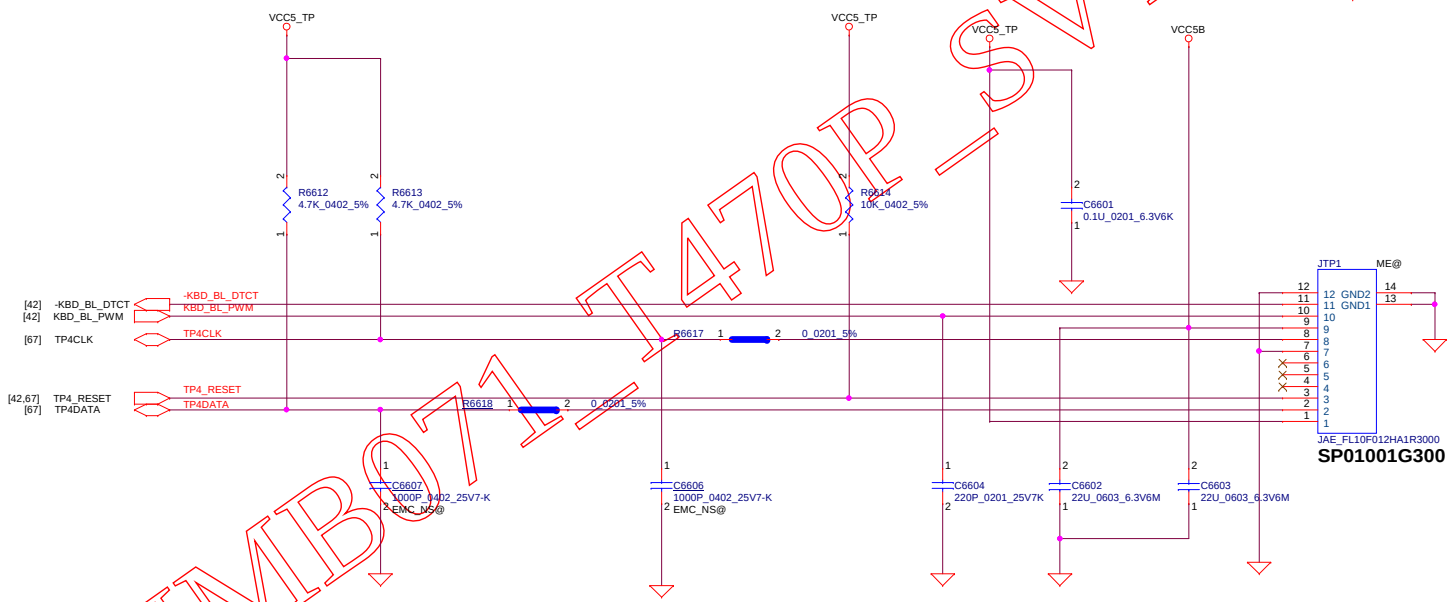

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: KEYBOARD/TRACK POINT

Size	Document Number	Rev
Custom	NM-B071	0.2
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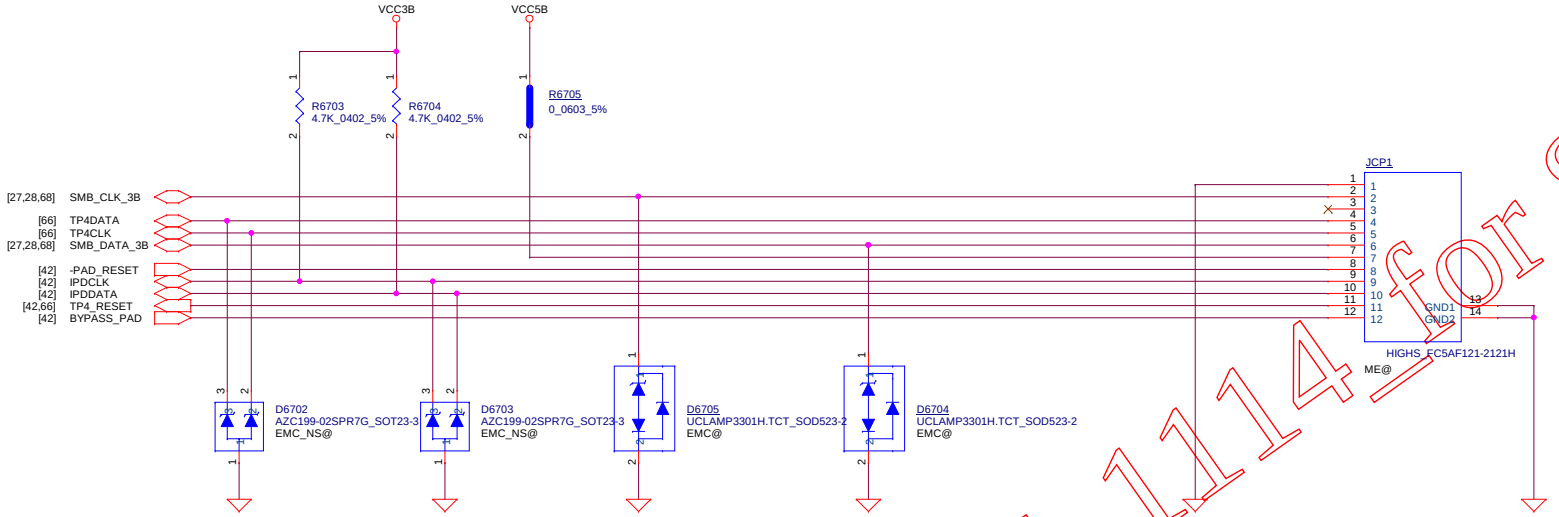
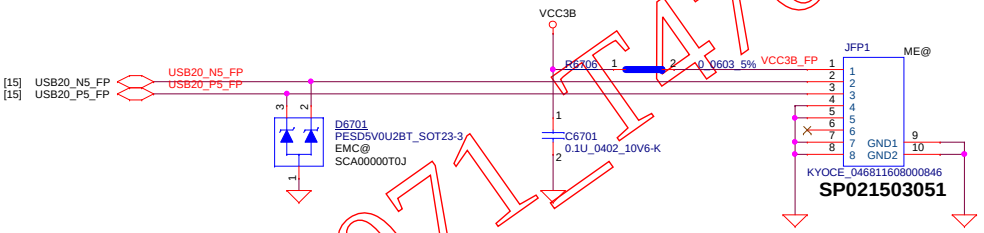
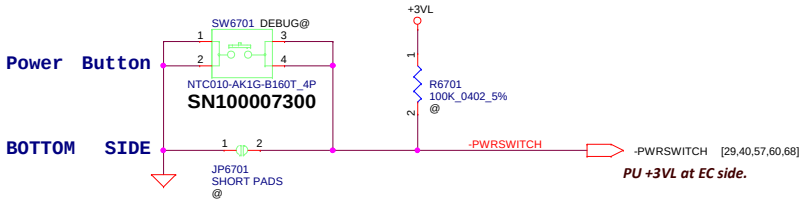
Click Pad



FingerPrint CONN.



PWRBTN FOR DEBUG



Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: Click Pad/FPR/PBTN

Size	Document Number	Rev
Custom	NM-B071	0.2

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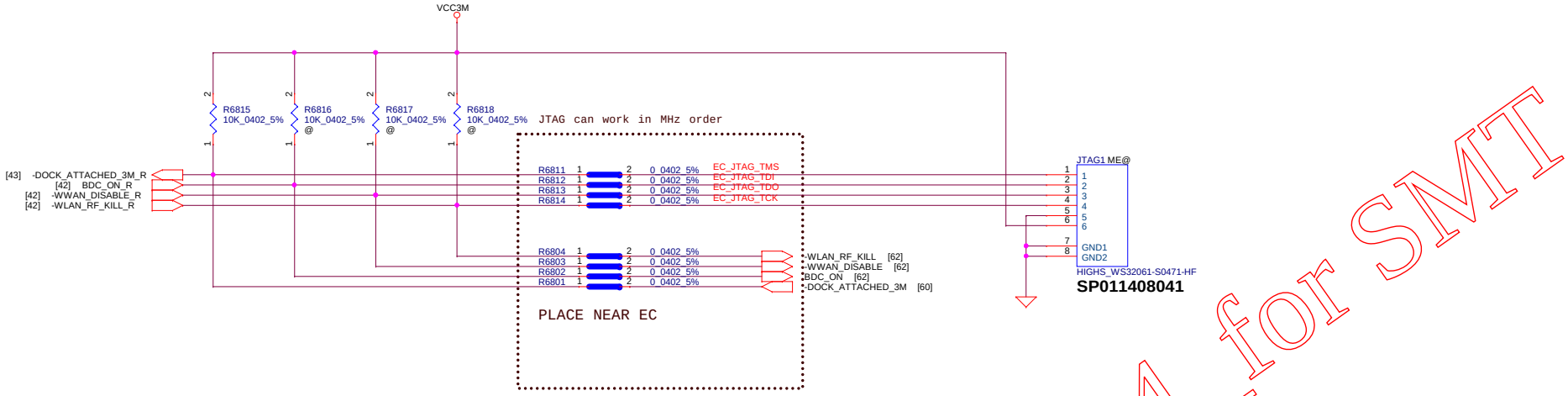
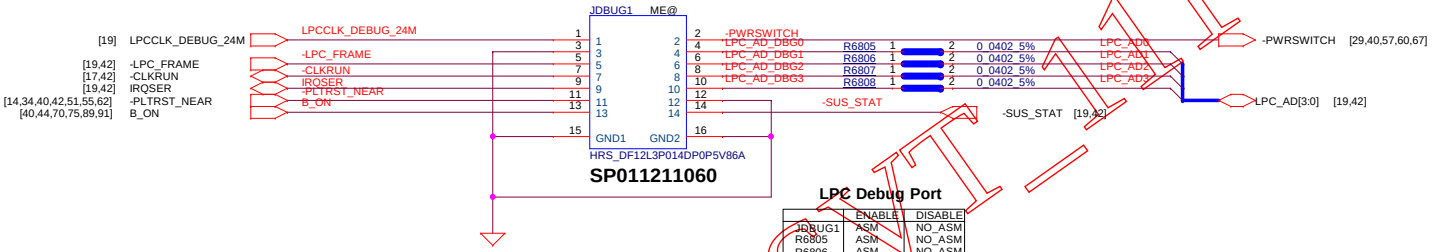
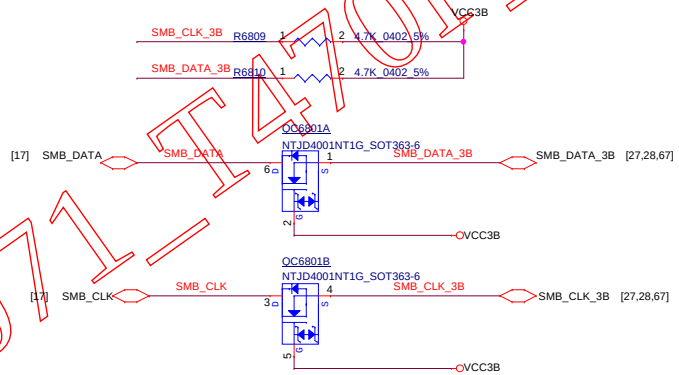




LPC Debug Port

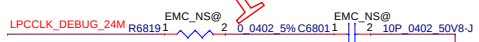
	ENABLE	DISABLE
JDBUG1	ASM	NO_ASM
R6805	ASM	NO_ASM
R6806	ASM	NO_ASM
R6807	ASM	NO_ASM
R6808	ASM	NO_ASM

LOGIC



Non ECSL part Change
SB00000EO1J=>SB00000YN00

EMC



Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

Title: ***SMBUS SWITCH/LPC DEBUG***

Size	Document Number	Rev
Custom	NM-B071	0.2

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Issued Date	2013/11/04	Deciphered Date	2014/12/31

Title: EMC

Size	Document Number	Rev
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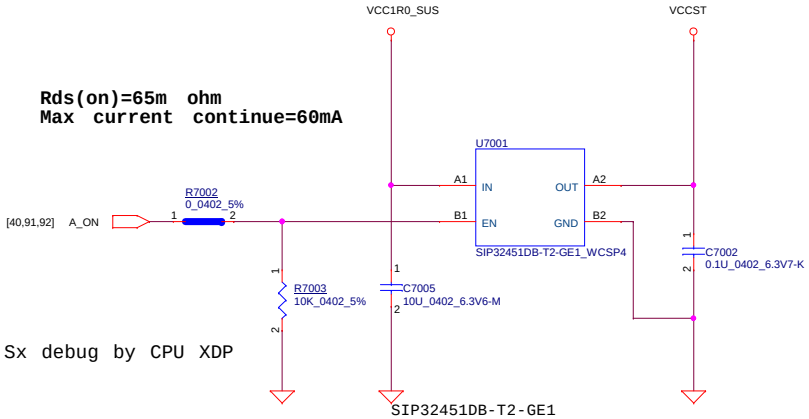
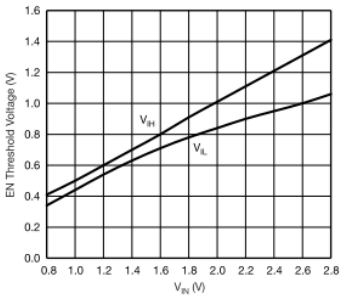
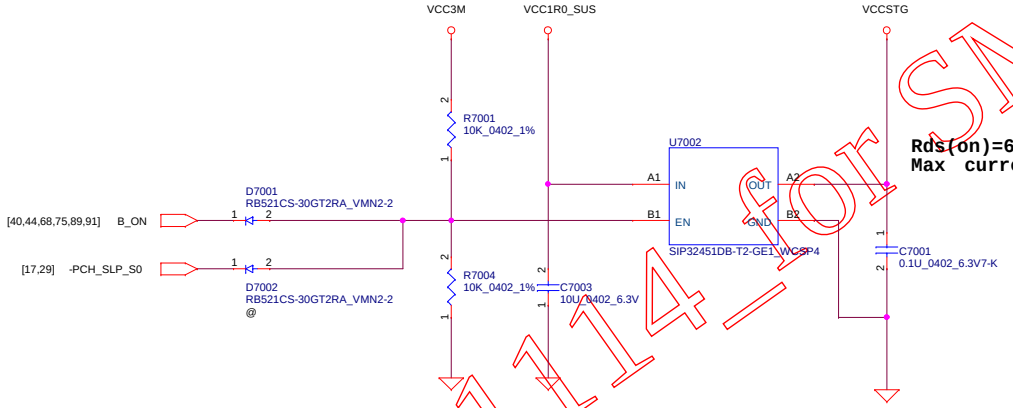
Rds(on)=65m ohm
Max current continue=60mA



For Sx debug by CPU XDP

SIP32451DB-T2-GE1
EN pin Max Voltage Rating is 2.75V





Rds(on)=65m ohm
Max current continue=60mA

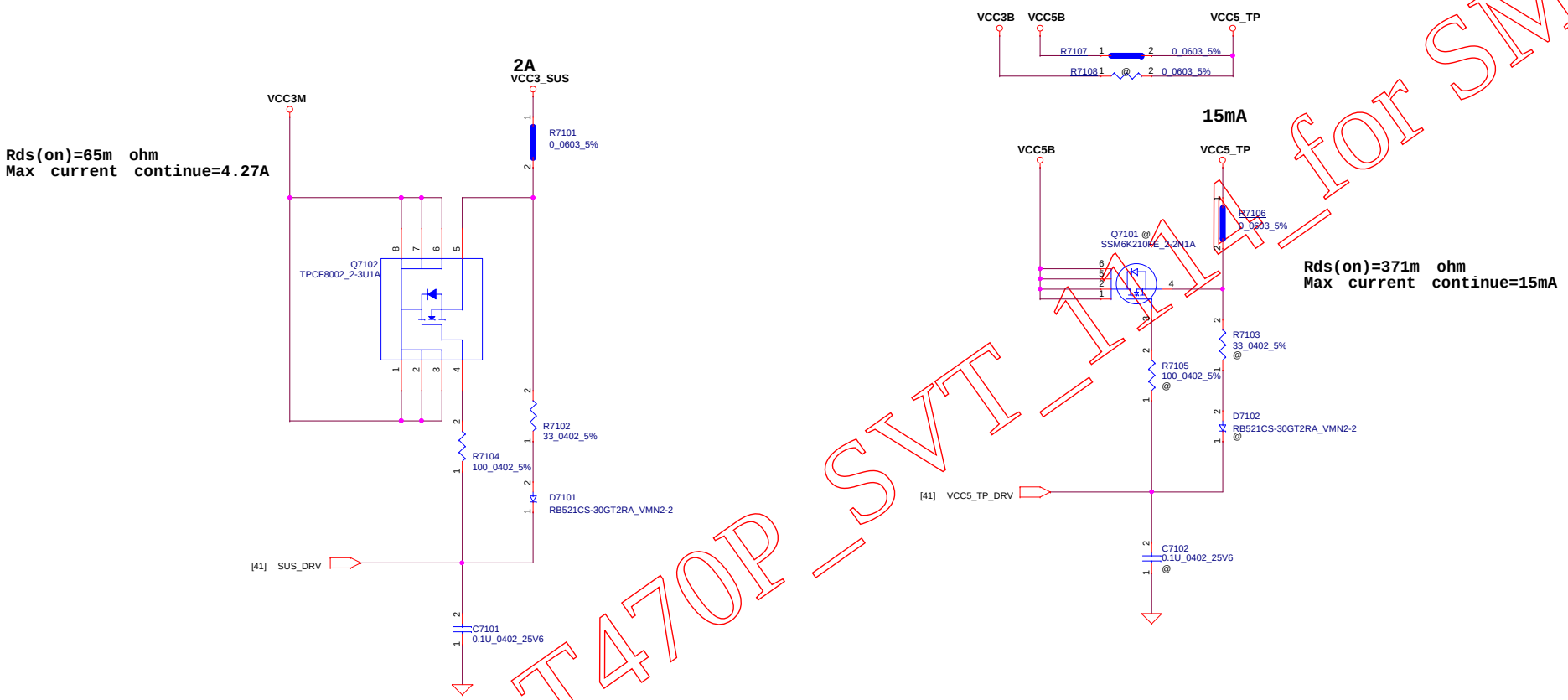
SIP32451DB-T2-GE1
EN pin Max Voltage Rating is 2.75V

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW VCCST/VCCSTG

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 70 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW PCH SUS/TRACK POINT

Size: Custom	Document Number: NM-B071	Rev: 0.2
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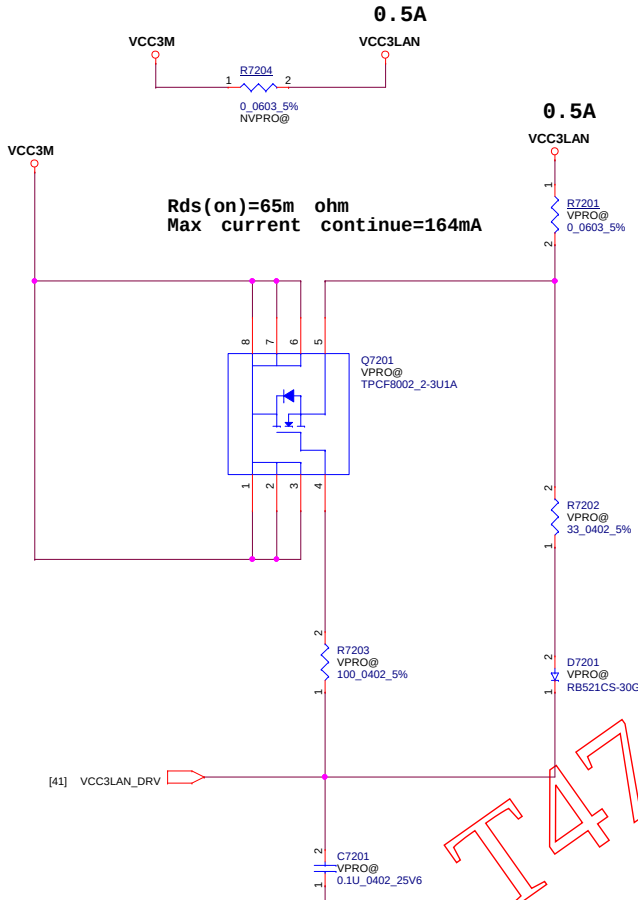

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW LAN

Size	Document Number	Rev
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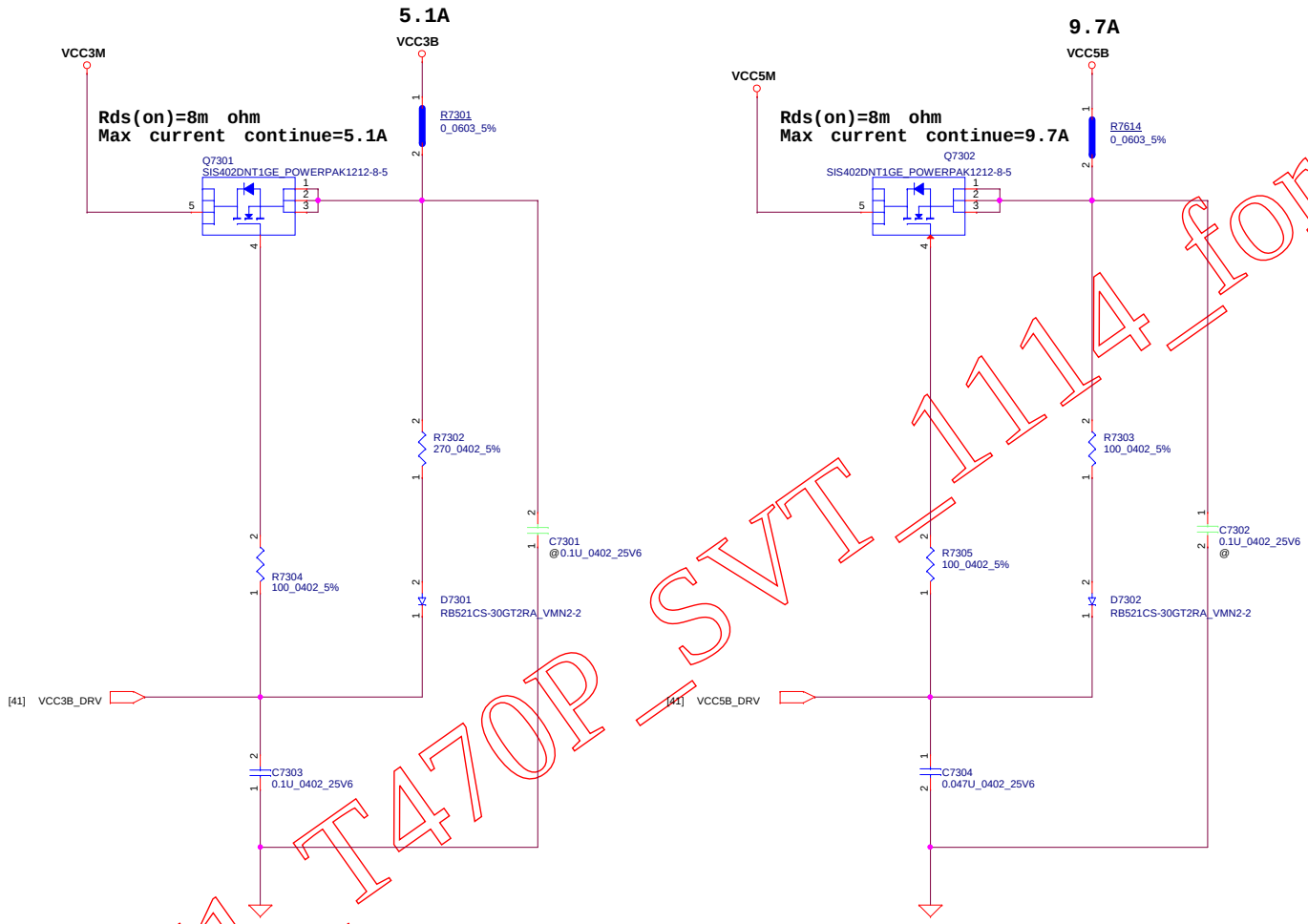
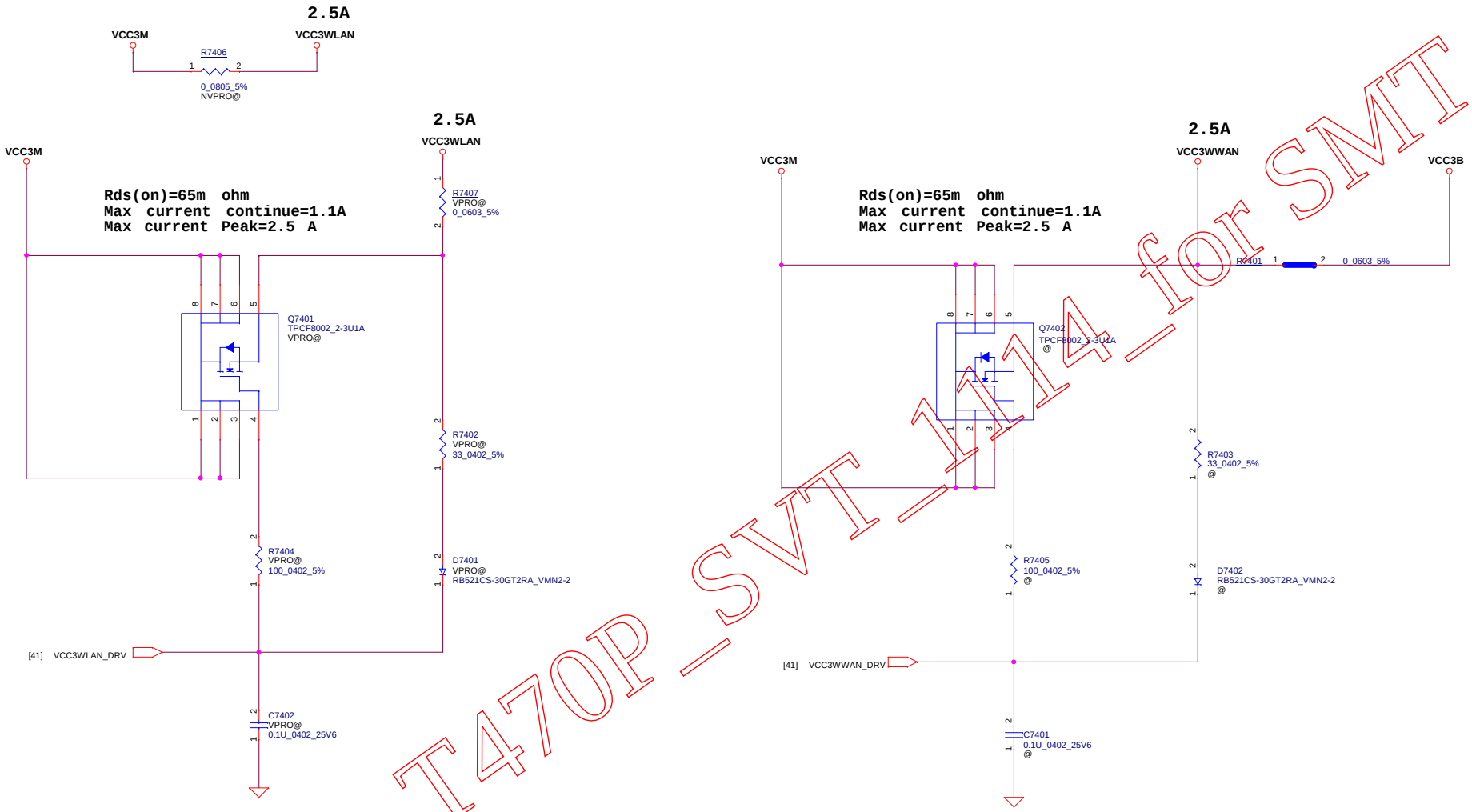


Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW B

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 73 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW WWAN&WLAN

Size	Document Number	Rev
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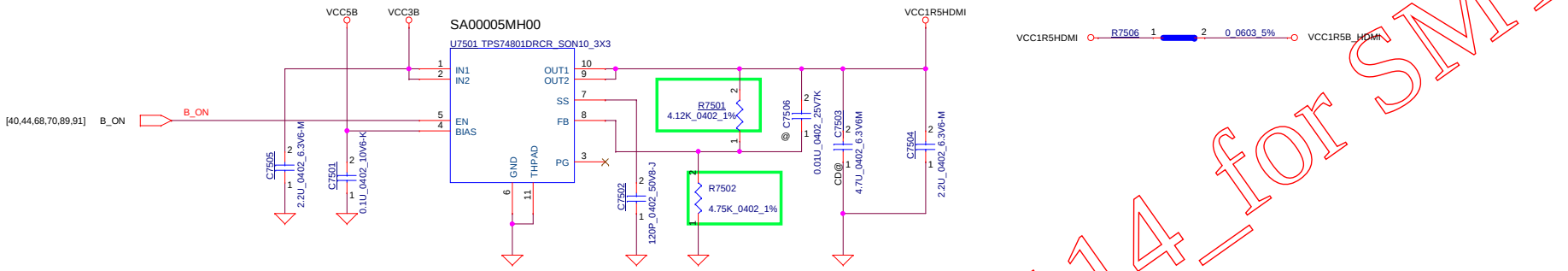
Date: Wednesday, October 12, 2016 Sheet 74 of 99

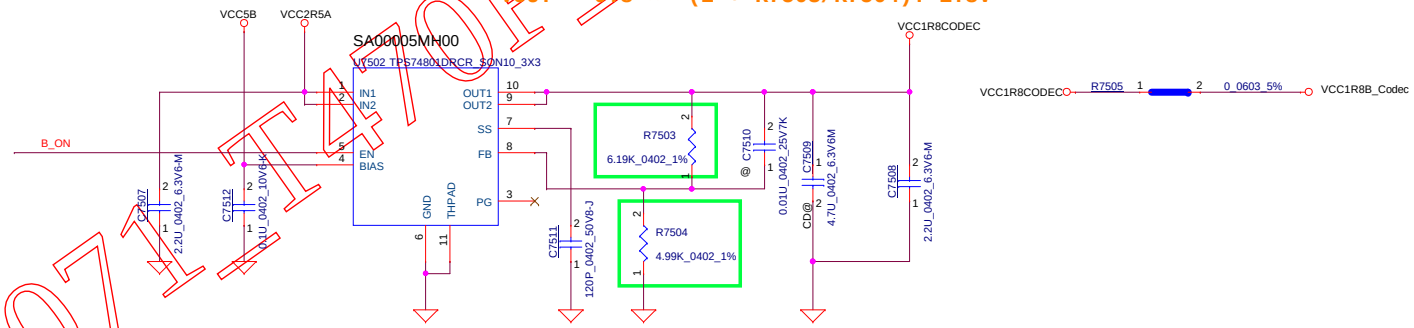
VCC3B transform 1.5V to HDMI

VOUT = 0.8 × (1 + R7501/R7502)=1.5V



VCC2R5A transform 1.8V to Codec

VOUT = 0.8 × (1 + R7503/R7504).=1.8V

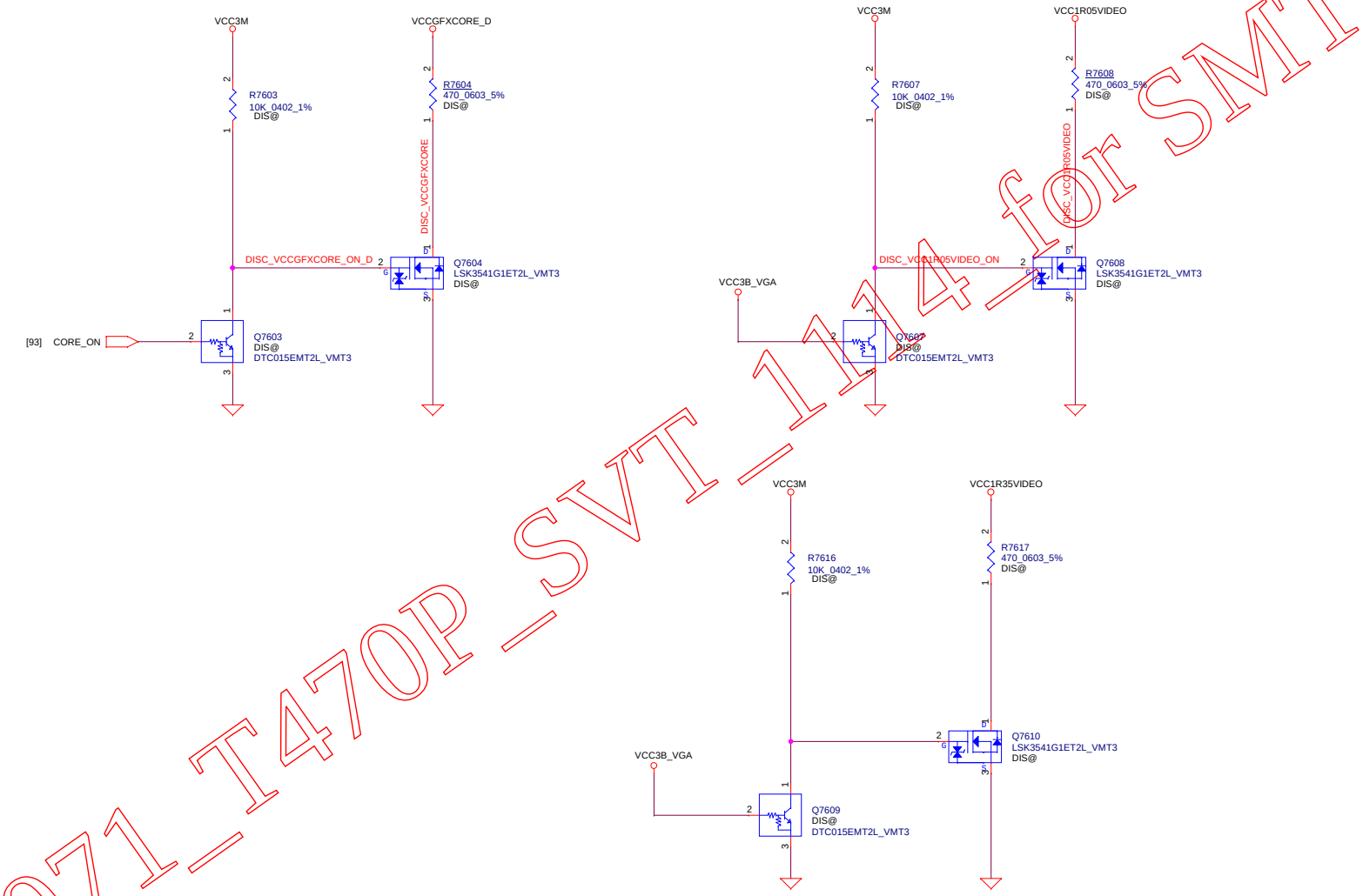


Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: LOAD SW VIDEO&FBVDD

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 75 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: **DISCHARGE CIRCUIT VIDEO**

Size	Document Number	Rev
Custom	NM-B071	0.2

Date: Wednesday, October 12, 2016 Sheet 76 of 99

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Title

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Debug connector

BIOS ROM socket	S SOCKET ACES 50960-0084N-001 BIOS ROM	J2601	LTCX0049G00
BIOS debug conn	S H-CONN HIROSE DF12L(3.0)-14DP-0.5V(86)	JDBUG1	SP01001H10T
EC debug conn	S H-CONN HIGHSTAR WS32061-S0471-HF P1.25	JTAG1	SP01001VA00
Power botton in MB	S TACT SW NTC010-AK1G-B160T SPST H3.1 4P	SW6701	SN100007300
SW/ME debug conn	FCI_10051922-1810ELF Kyocera 04-6809- 618-220-846+	J2901	

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DEBUG CONN

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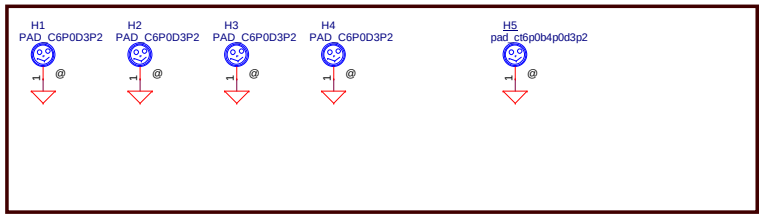
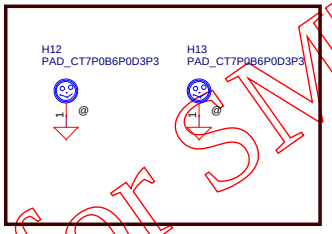
Screw Hole

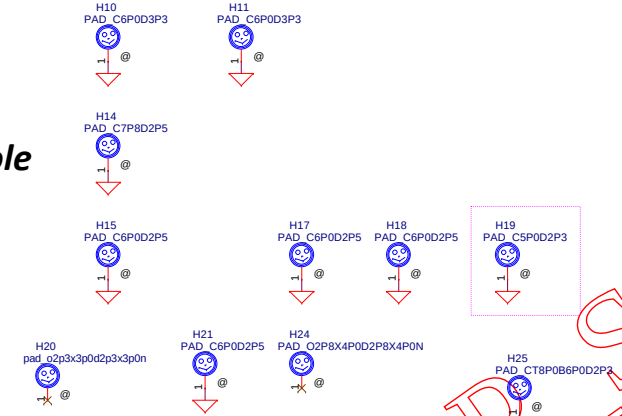
For CPU and GPU



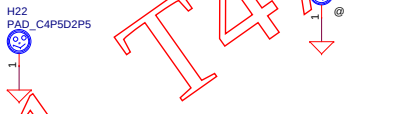
AUDIO SCREW



For ME GND hole



For ME hole



PCB Fedical Mark PAD

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/12/31

Title: **SCREW HOLE**

Size	Document Number	Rev
Custom	NM-B071	0.2

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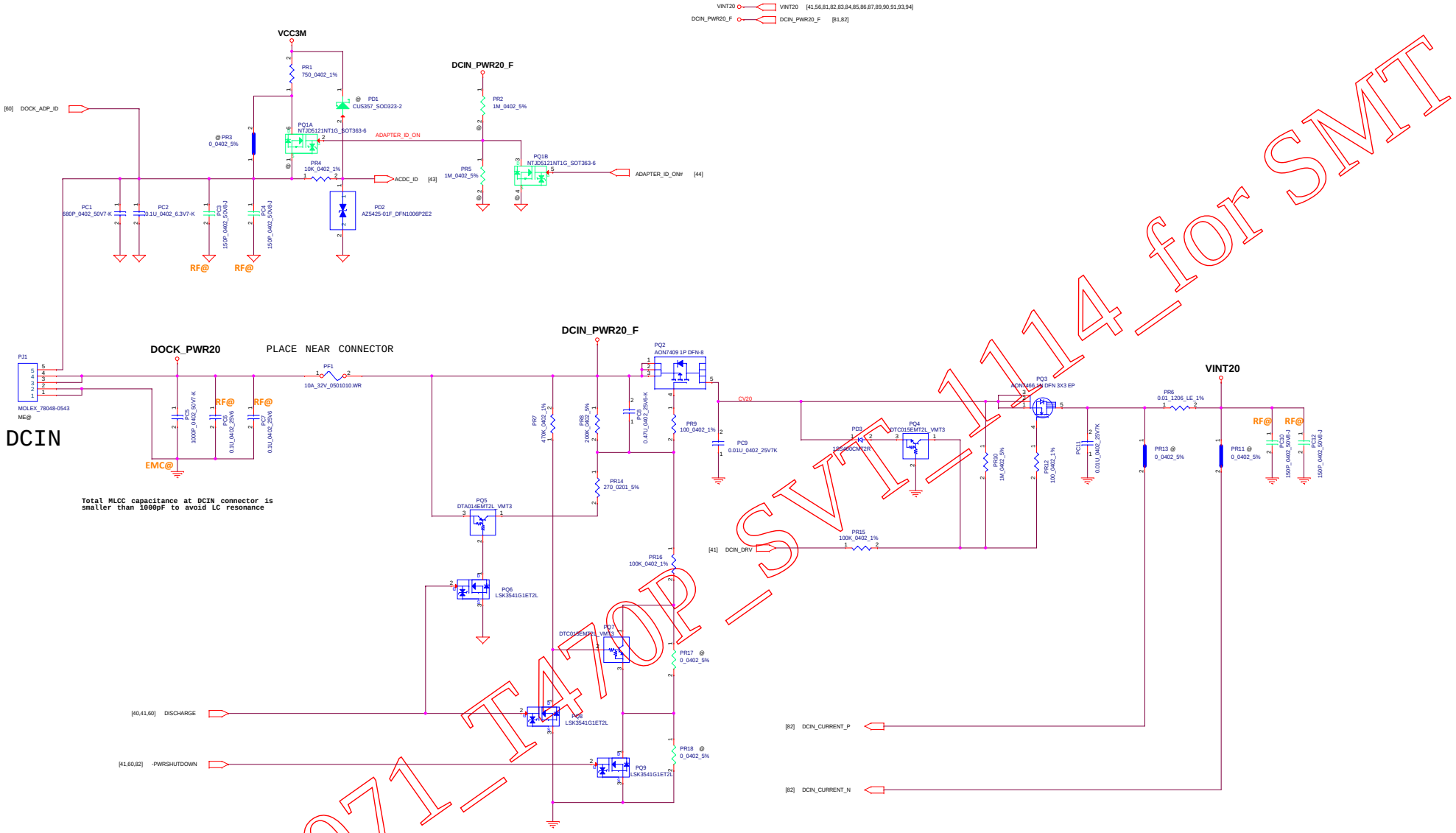


NMB071_T470P_SVT_1114_for SMT

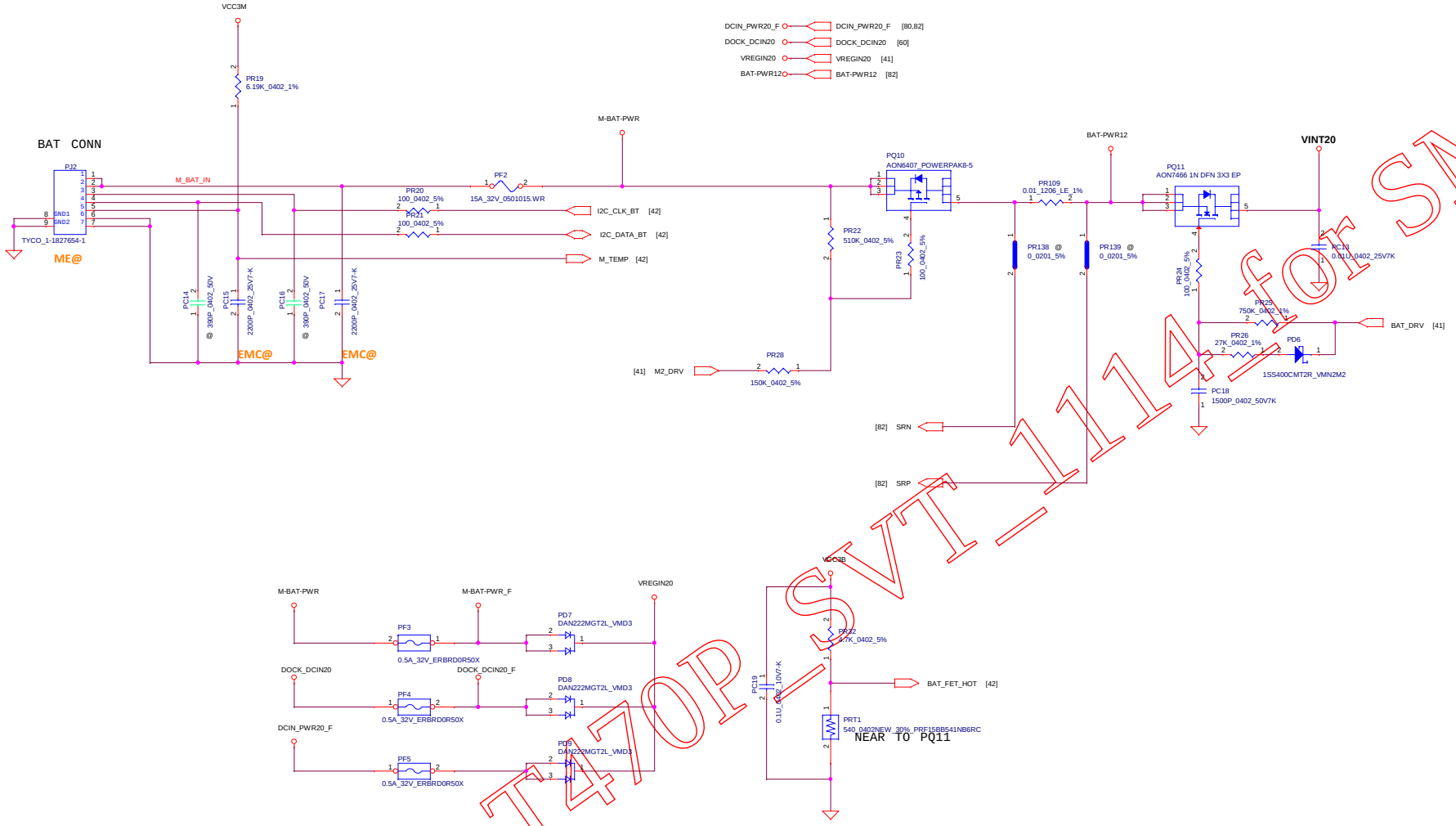
TABLE

PEAK SHIFT	YES	NO
PR17	NO-ASM	ASM
PR7	ASM	NO-ASM
PQ8	ASM	NO-ASM
PQ7	ASM	NO-ASM

LOGIC

Security Classification	LC Future Center Secret Data	Title	DC-IN
Issued Date	Deciphered Date	Size: Custom	Document Number: NM-A611
		Rev: 0.1	
Date: Monday, November 14, 2016	Sheet 80 of 99		

Payton Common

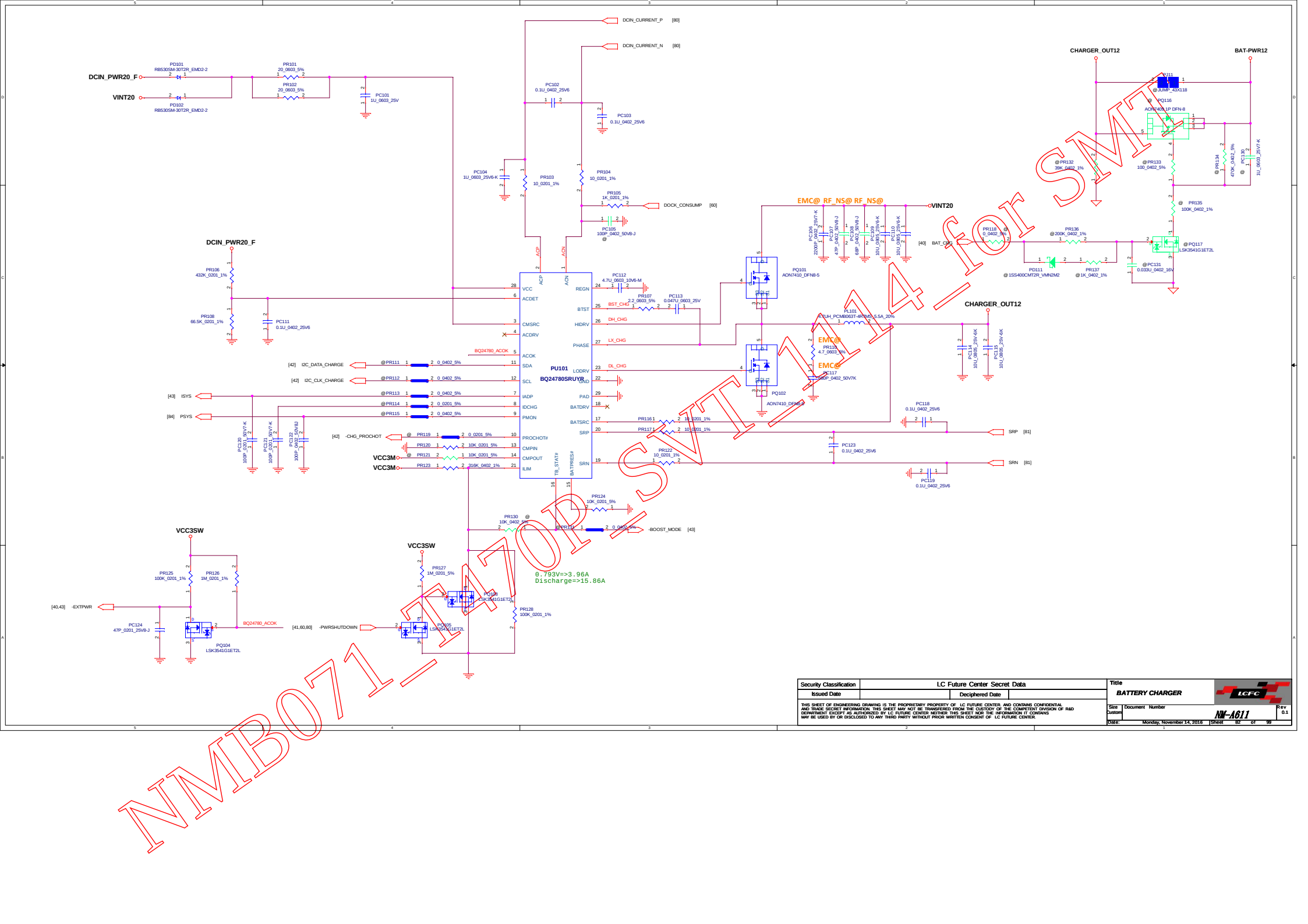


Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: **BATTERY INPUT**

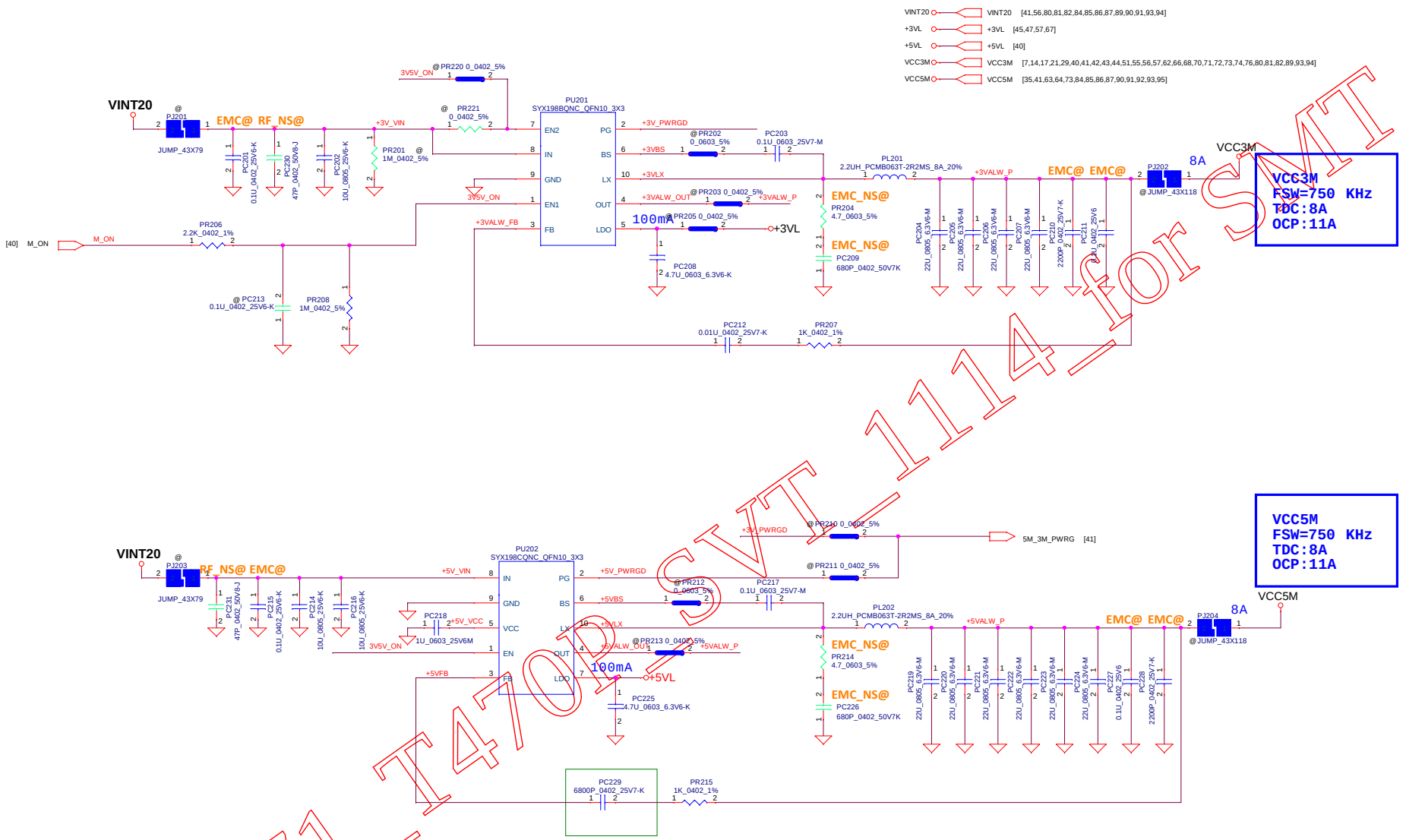
Size	Document Number	Rev
Custom	NM-A611	0.1

Date: Monday, November 14, 2016 Sheet 81 of 99



Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

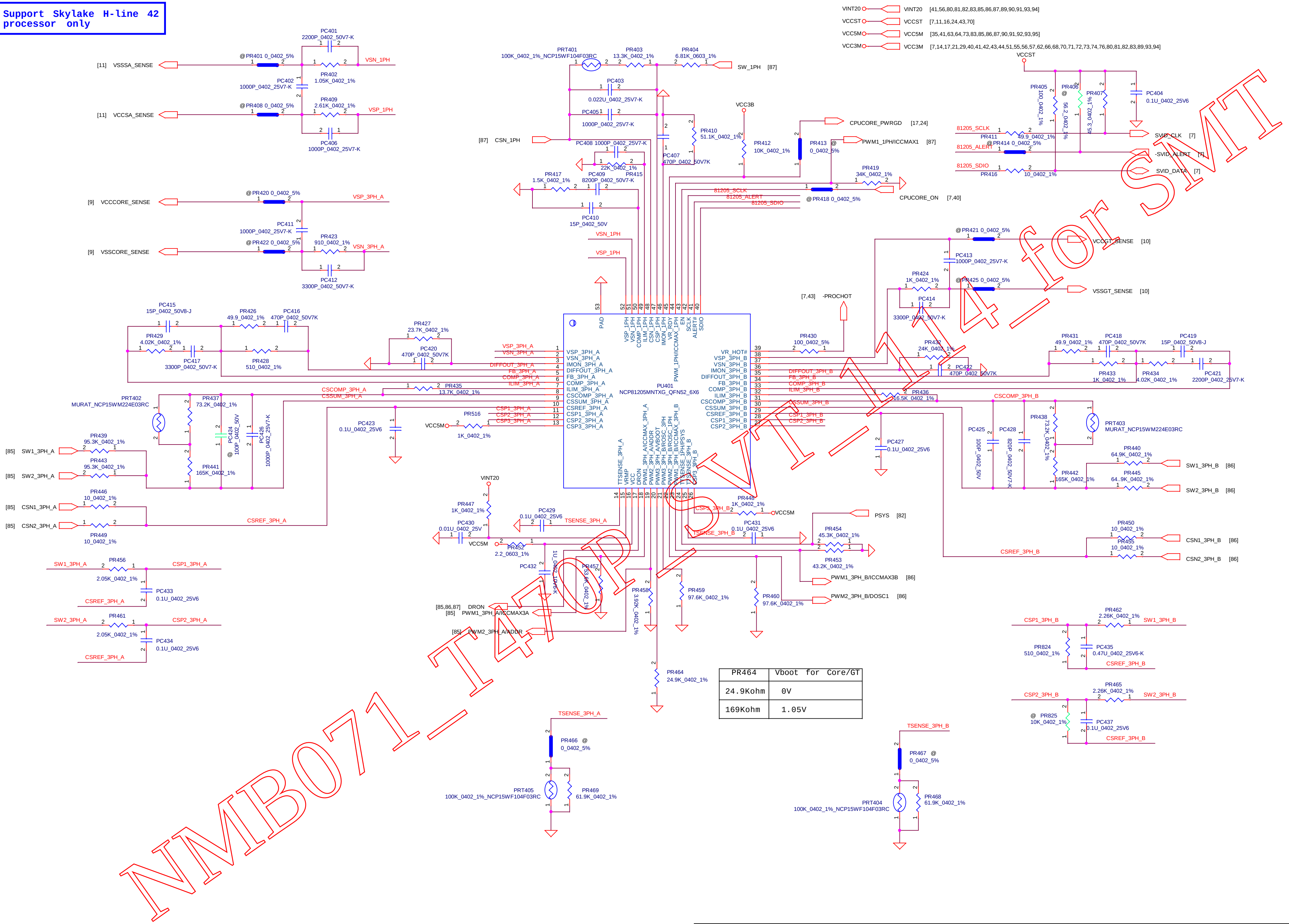
Title	BATTERY CHARGER		
Size	Document Number		Rev
Custom	NM-A611		0.1
Date:	Monday, November 14, 2016	Sheet	82 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	3VALWP/5VALWP		
Size	Document Number		Rev
Custom	NM-A611		0.2
Date:	Monday, November 14, 2016	Sheet	83 of 99

Support Skylake H-line 42 processor only



PR464	Vboot for Core/GT
24.9Kohm	0V
169Kohm	1.05V

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: **DC/DC IMVP8**

Size: Custom | Document Number: NM-A611 | Rev: 0.1

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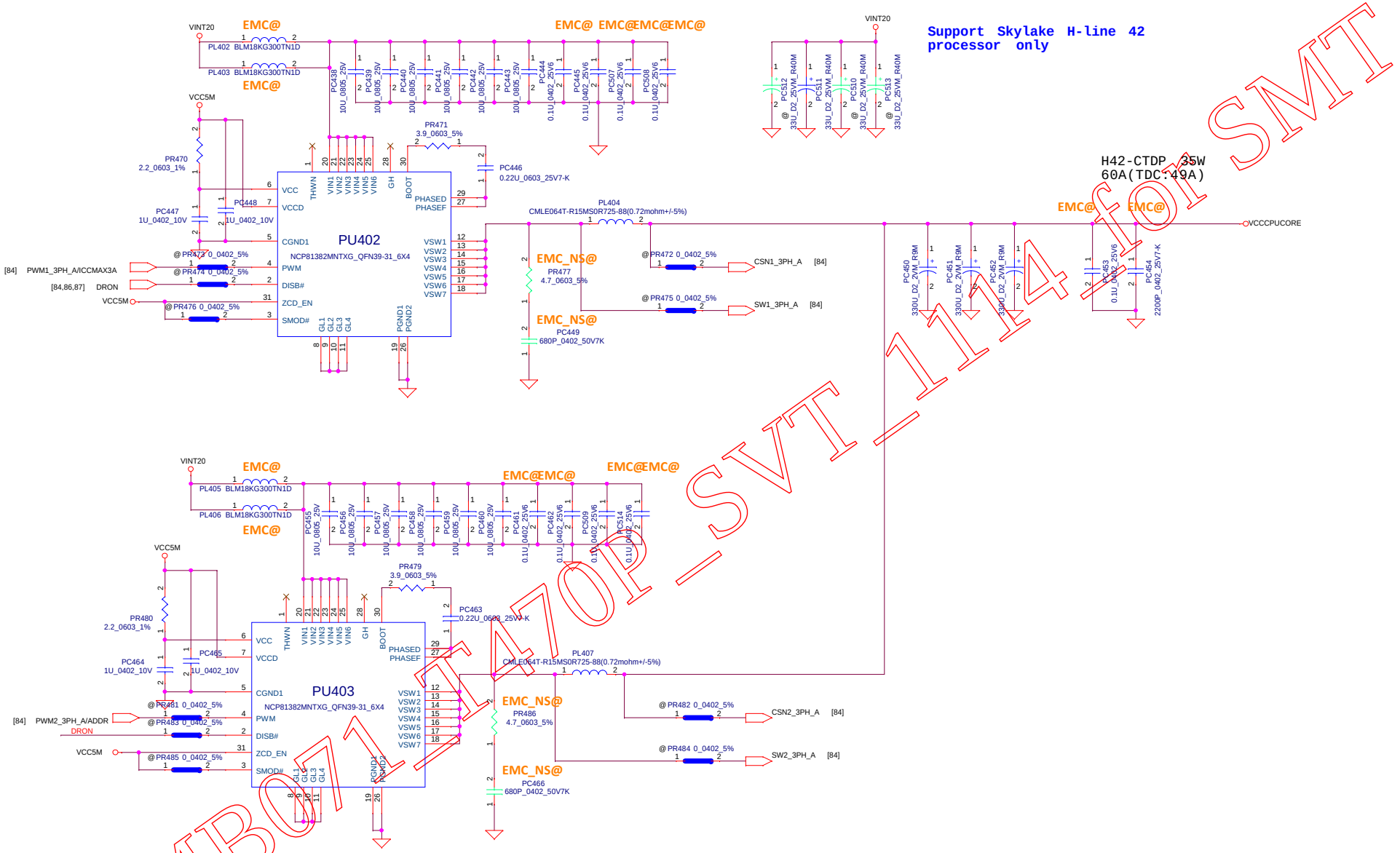

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DC/DC VCCPUCORE

Size	Document Number	Rev
Custom	NM-A611	0.1

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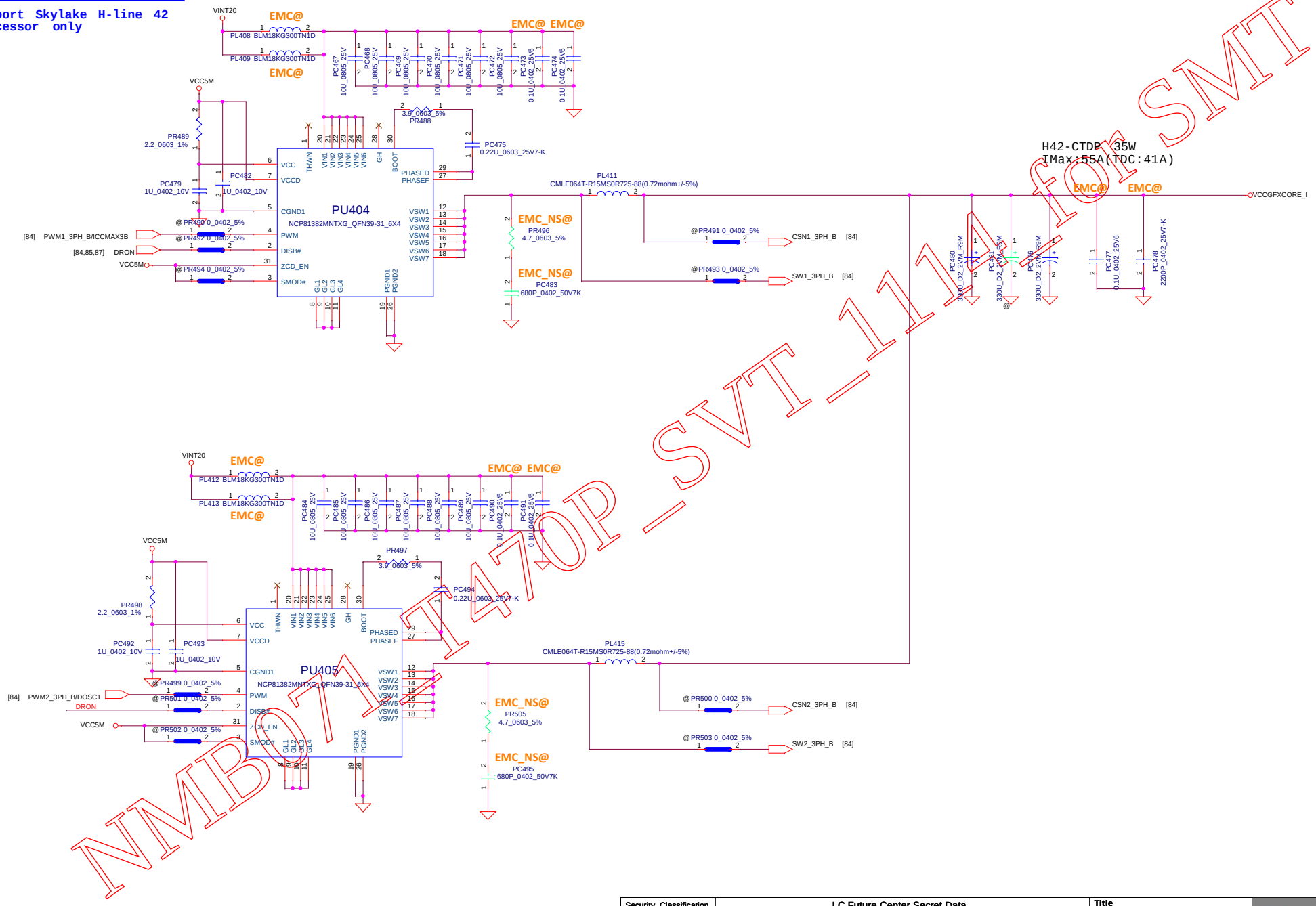
Walter Unique

Support Skylake H-line 42 processor only

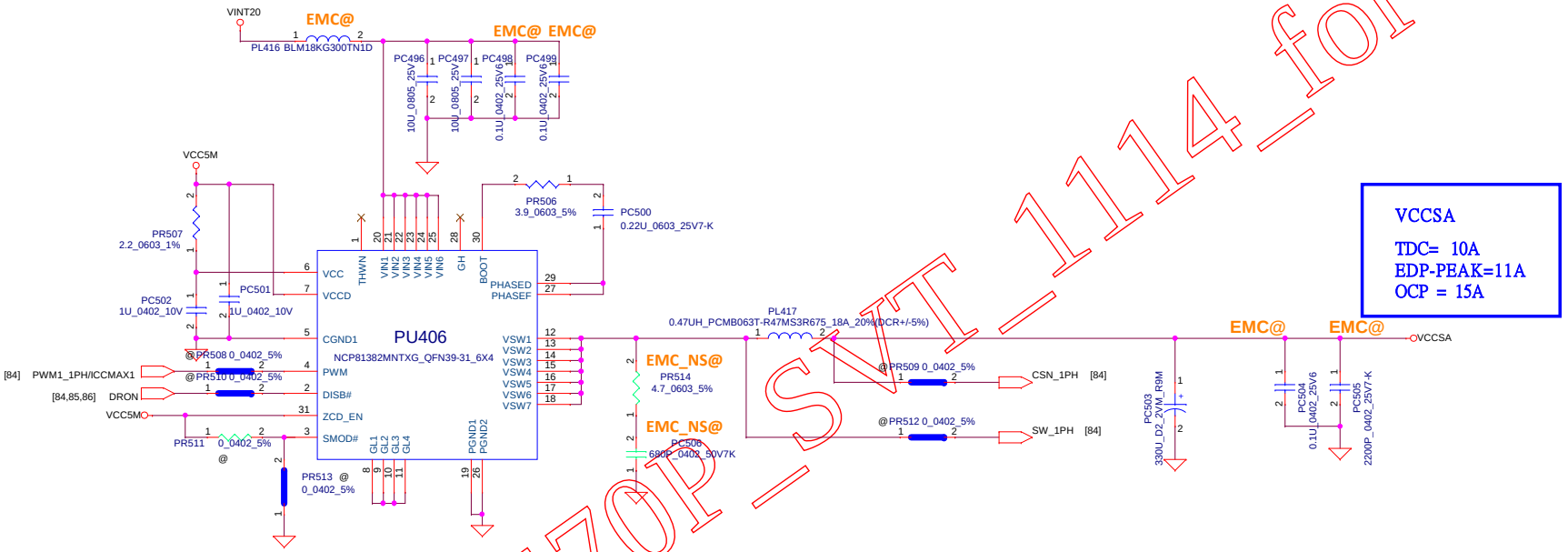


Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title	DC/DC VCCGFXCORE_I		
Size: Custom	Document Number: NM-A611		Rev: 0.1
Date: Monday, November 14, 2016	Sheet 86 of 99		

Walter Unique

Support Skylake H-line 42 processor only



VCCSA

TDC= 10A
EDP-PEAK=11A
OCP = 15A

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DC/DC VCCSA

Size	Document Number	Rev
Custom	NM-A611	0.1

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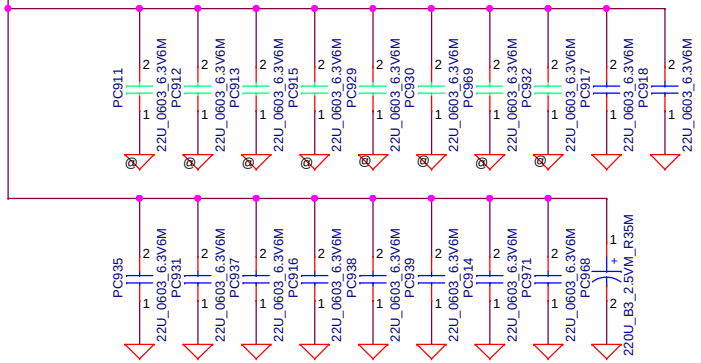
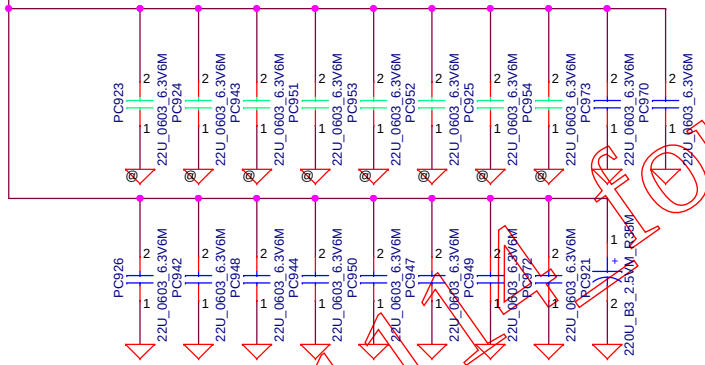
VCCCPUCORE

VCCCPUCORE
22uF 10pcs + 220uF/3528 1pcs



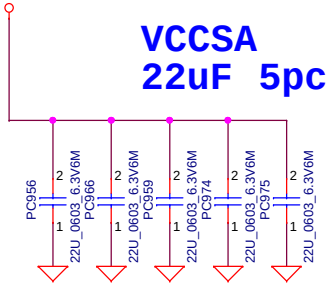
VCCGFXCORE_I

VCCGFXCORE_I
22uF 10pcs + 220uF/3528 1pcs

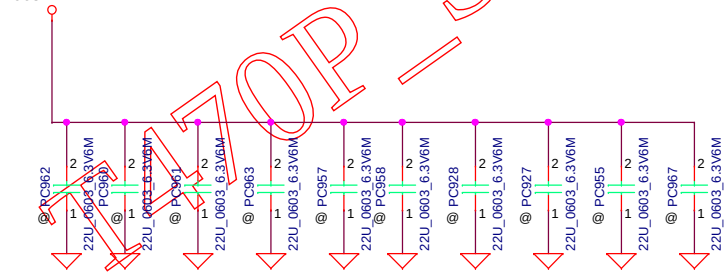


VCCSA

VCCSA
22uF 5pcs



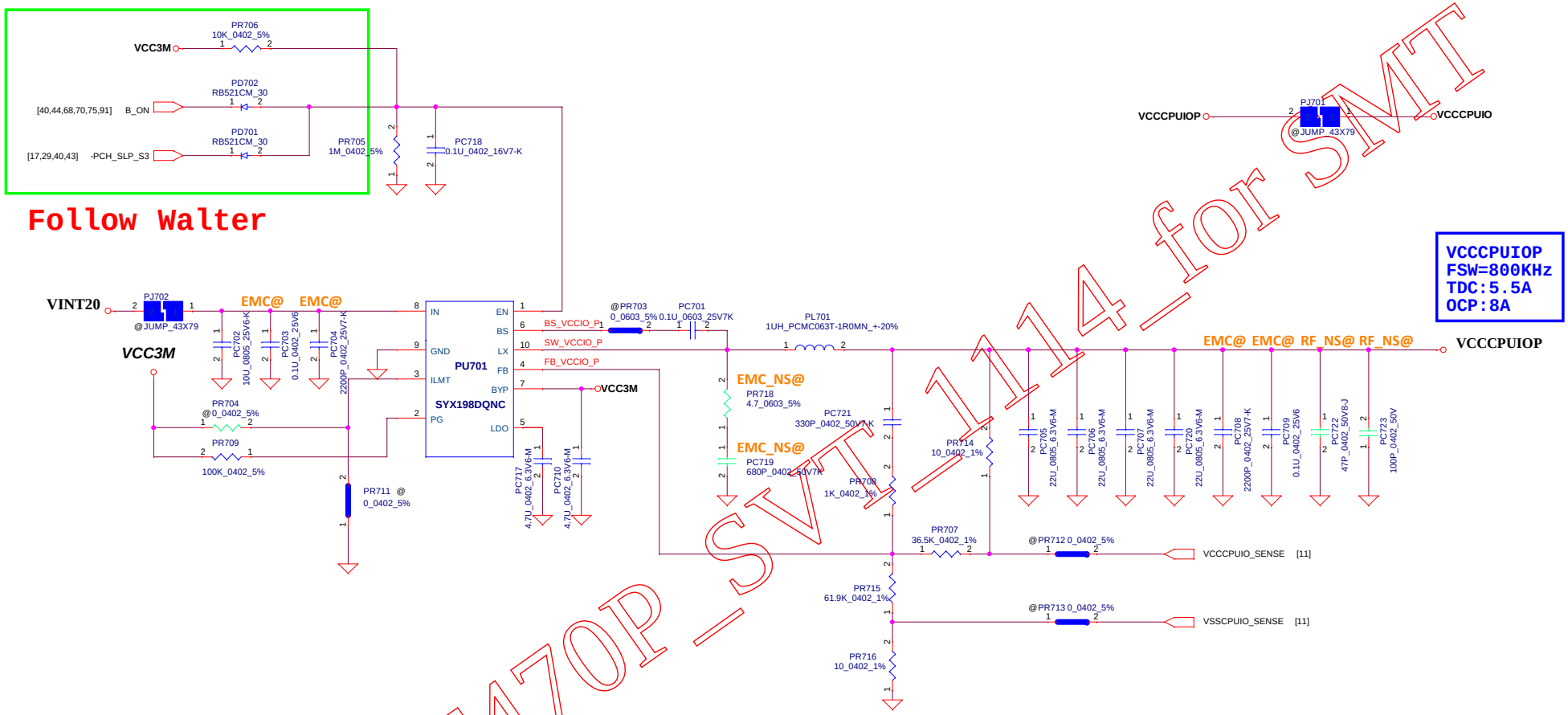
VCCSA



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

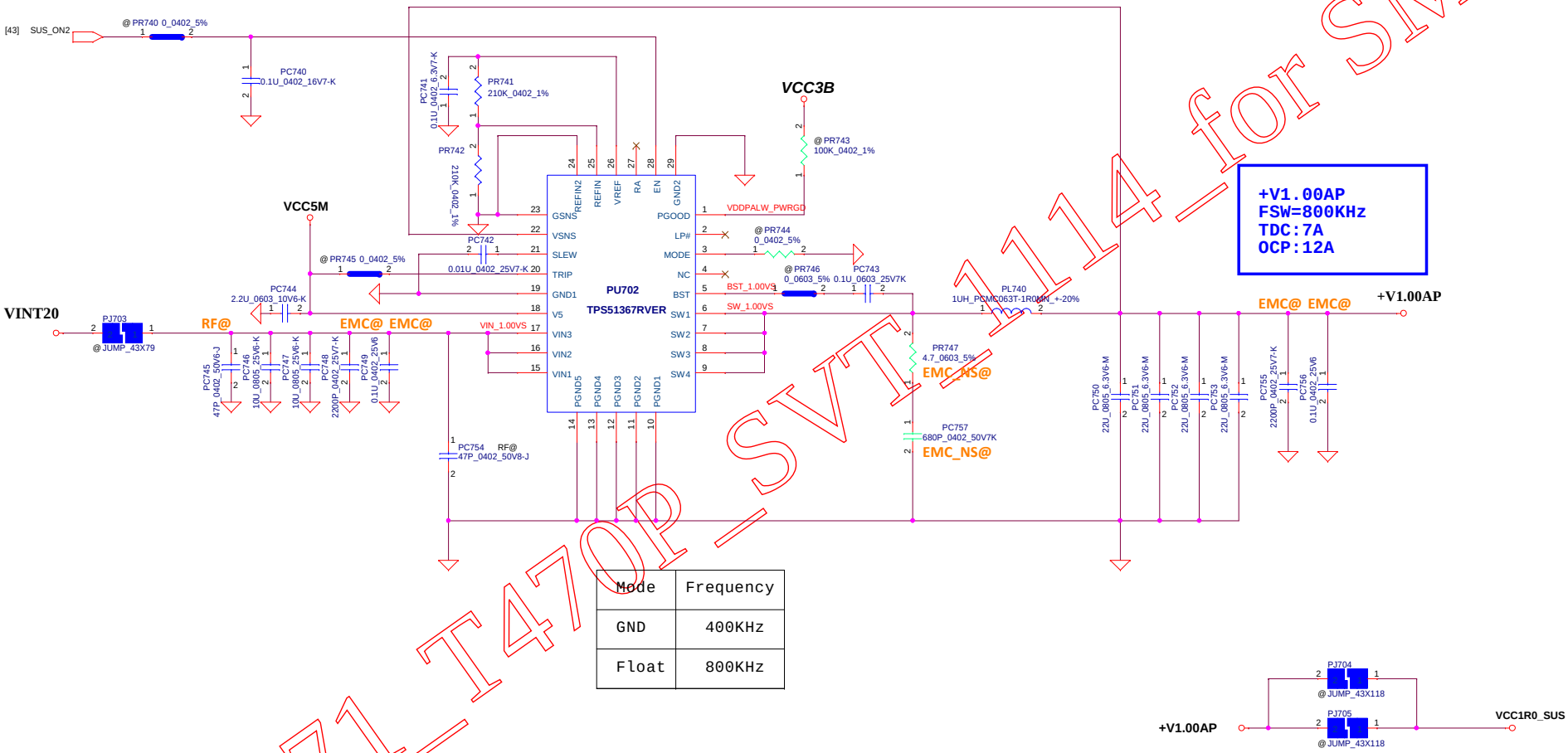
Size: B	Document Number: NM-A611	Rev: 0.1
Date: Monday, November 14, 2016	Sheet 88 of 99	



Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DC/DC VCCCPUIO

Size: Custom	Document Number: NM-A611	Rev: 0.1
Date: Monday, November 14, 2016	Sheet 89 of 99	



Mode	Frequency
GND	400KHz
Float	800KHz

Security Classification	LC Future Center Secret Data		
Issued Date	2014/07/01	Deciphered Date	2015/12/31

Title: DC/DC VCC1R0_SUS

Size	Document Number	Rev
Custom	NM-A611	0.1

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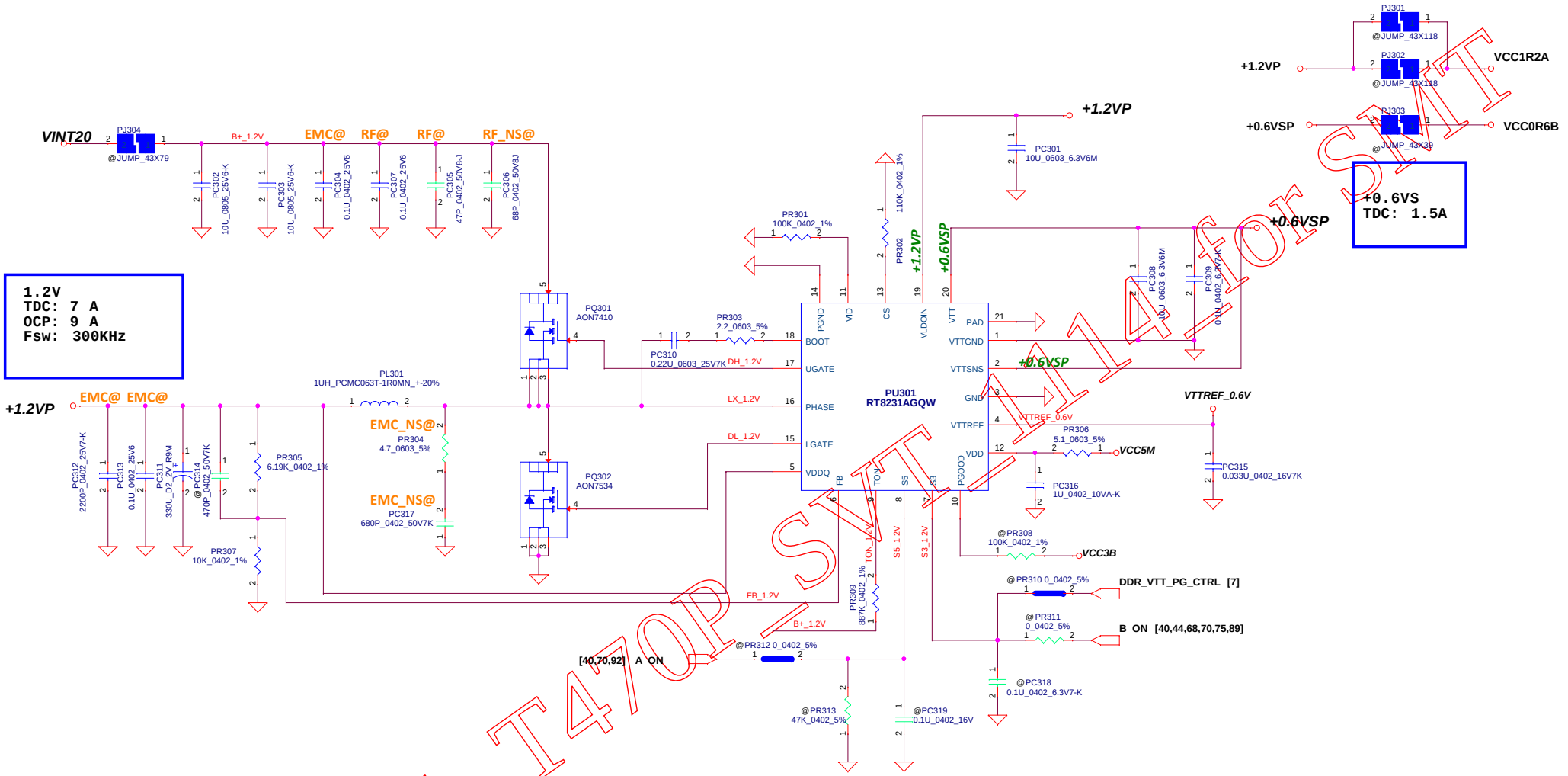

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.35V/+0.675VS		
Size	Document Number		Rev
Custom	NM-A611		0.1
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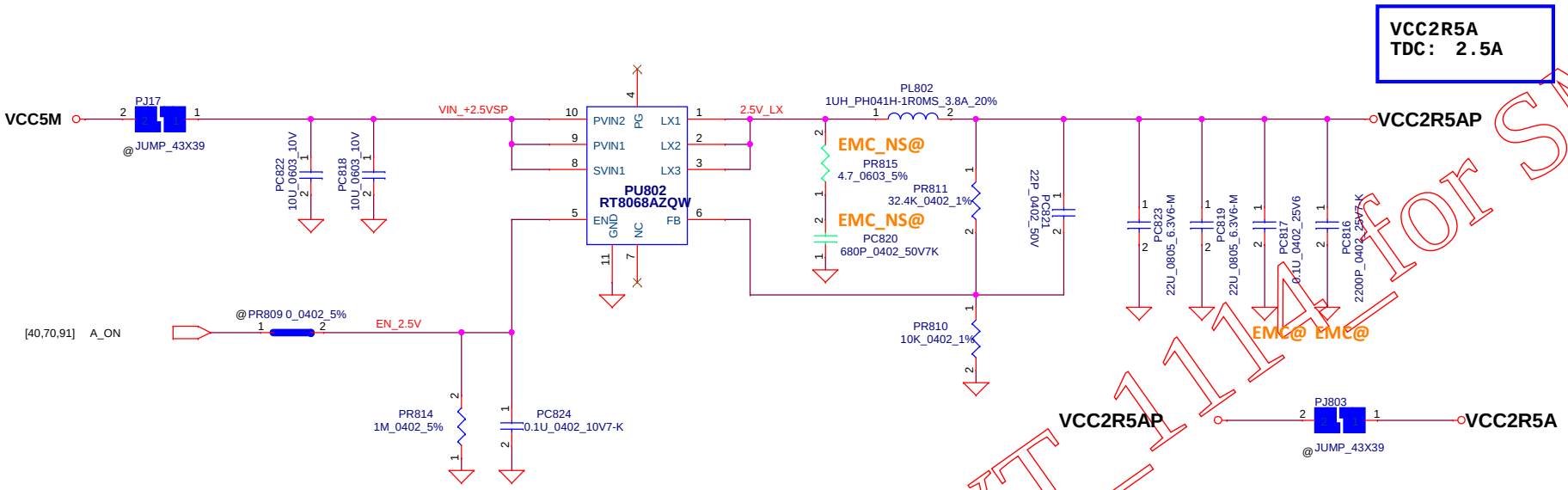
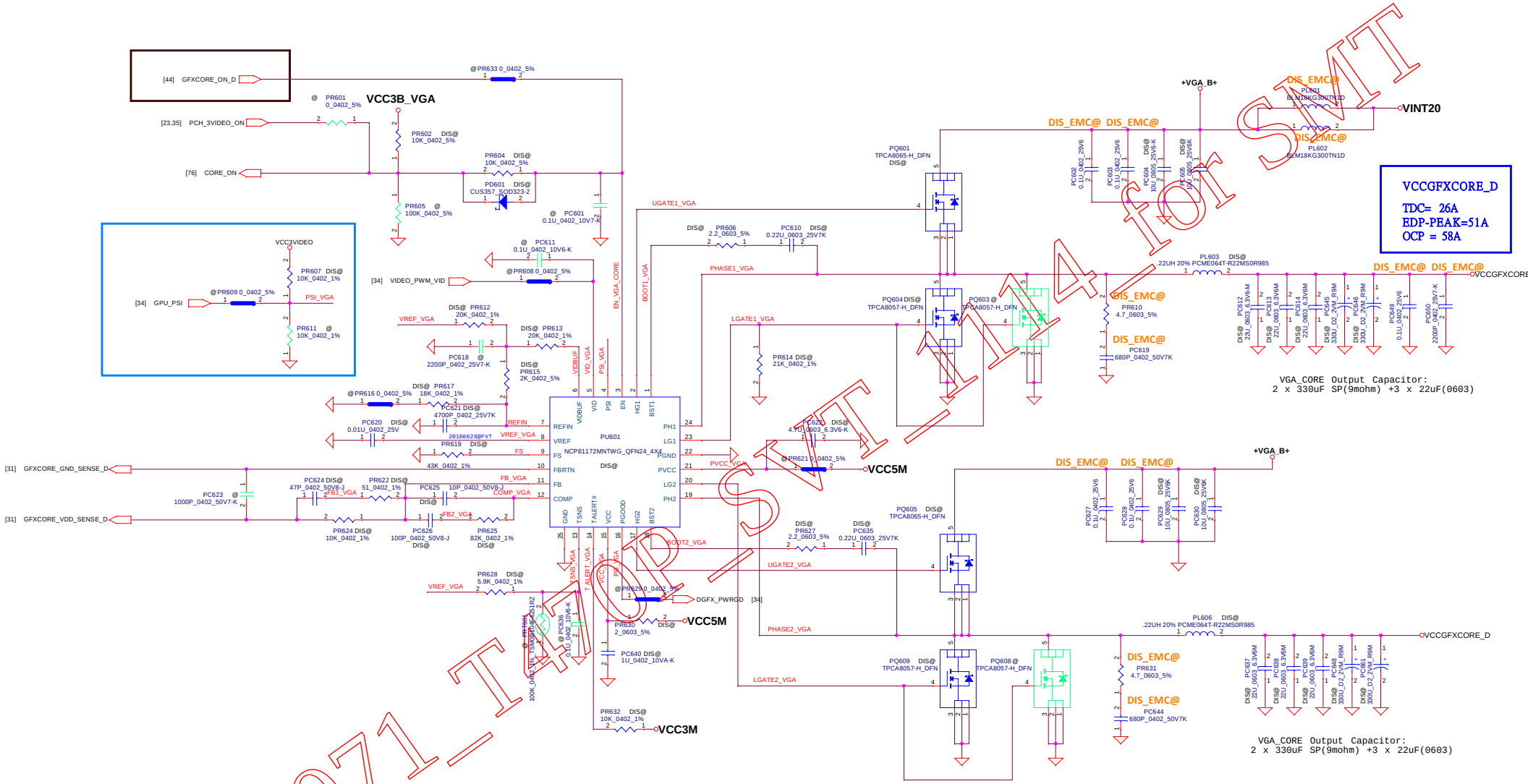


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	DC/DC VCC2R5A		
Size	Document Number		Rev
B	NM-A611		0.1
Date:	Monday, November 14, 2016	Sheet	92 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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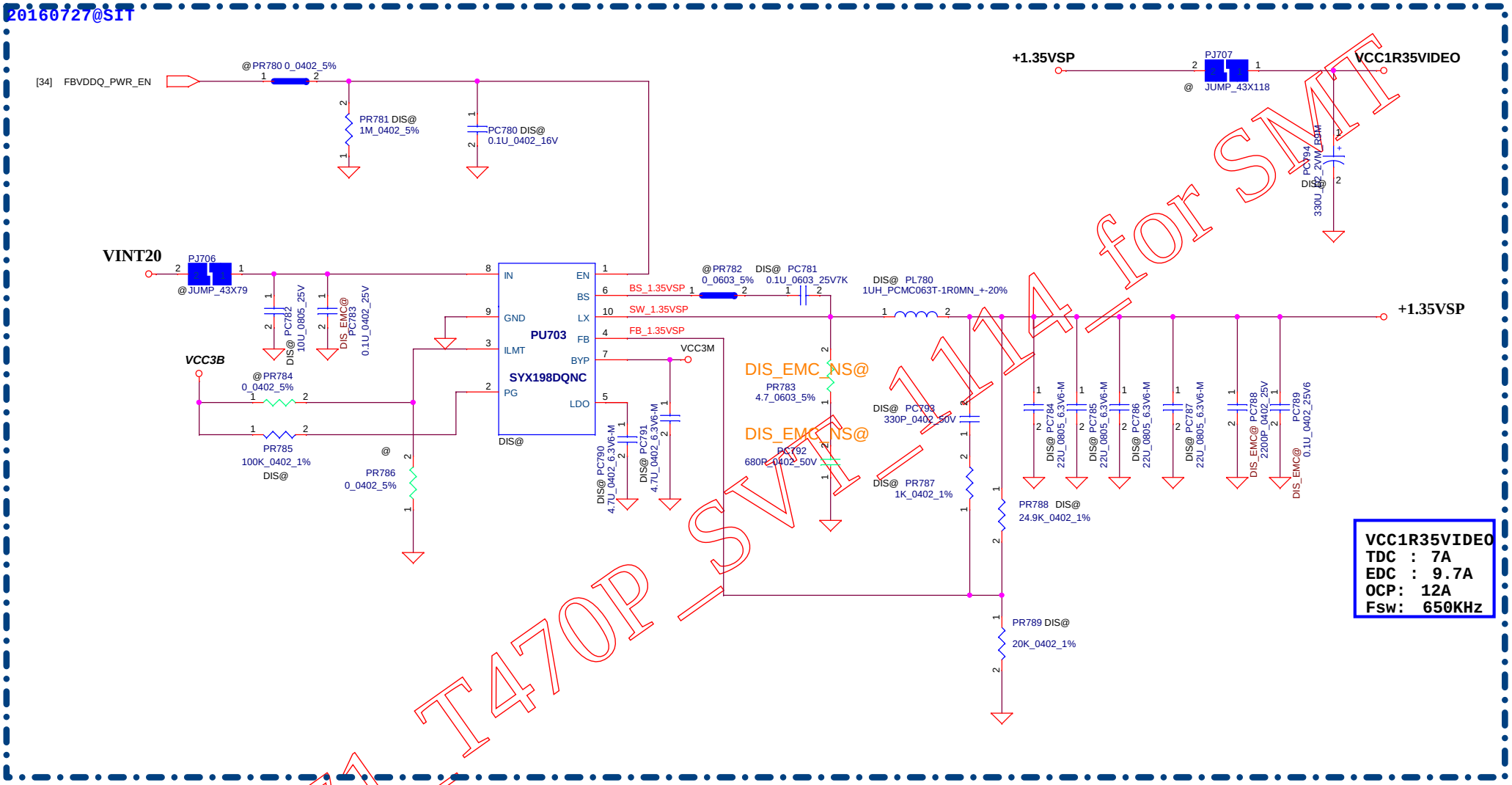
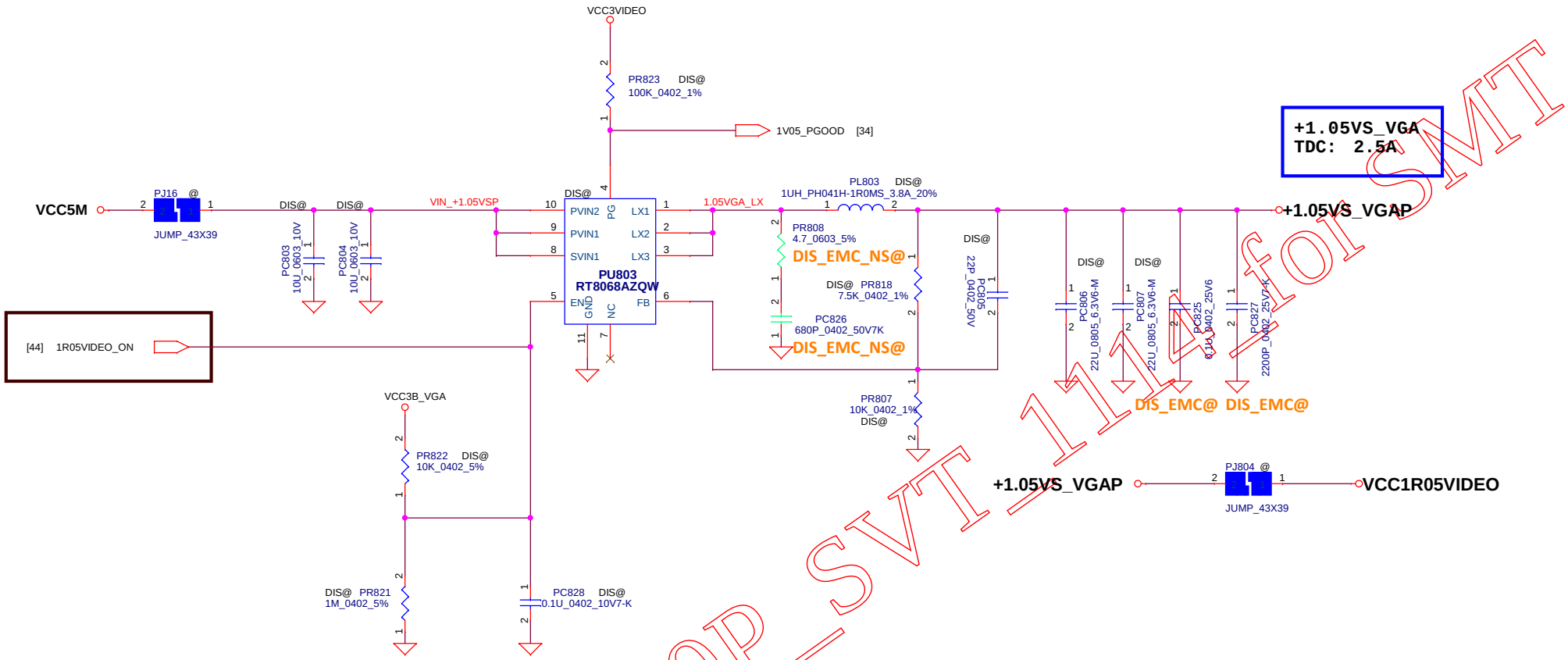
Title	PWR-VGA_CORE(NCP81174)		
Size	Document Number		Rev
Custom	NM-A611		0.1
Date:	Monday, November 14, 2016	Sheet	93 of 99

20160727@SIT



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+VCC1R35VIDEO		
Size	Document Number		Rev
B	NM-A611		0.1
Date:	Monday, November 14, 2016	Sheet	94 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **PWR-+1.05ALW**

Size	Document Number	Rev
B	NM-A611	0.1
Date: Monday, November 14, 2016	Sheet 95 of 99	

+0.6VSP +0.6VSP [91]
+1.05VS_VGAP +1.05VS_VGAP [95]
+1.2VP +1.2VP [91]
+1.35VSP +1.35VSP [94]
+V1.00AP +V1.00AP [90]
BAT-PWR12 BAT-PWR12 [81,82]
DCIN_PWR20_F DCIN_PWR20_F [80,81,82]
DOCK_DCIN20 DOCK_DCIN20 [60,81]
DOCK_DCIN20_F DOCK_DCIN20_F [81]
DOCK_PWR20 DOCK_PWR20 [60,80]
M-BAT-PWR M-BAT-PWR [81]
M-BAT-PWR_F M-BAT-PWR_F [81]
VCC2R5AP VCC2R5AP [92]
VCC3P VCC3P [56]
VTTREF_0.6V VTTREF_0.6V [91]

VINT20 VINT20 [41,56,80,81,82,83,84,85,86,87,89,90,91,93,94]
+3VL +3VL [45,47,57,67,83]
+5VL +5VL [40,83]
VCC3M VCC3M [7,14,17,21,29,40,41,42,43,44,51,55,56,57,62,66,68,70,71,72,73,74,76,80,81,82,83,89,93,94]
VCC3_SUS VCC3_SUS [7,14,15,16,17,18,21,23,24,26,29,42,43,45,62,71]
VCC3B VCC3B [7,16,17,18,19,20,21,23,24,27,28,35,40,41,42,43,44,45,47,49,54,55,56,57,58,59,60,61,62,67,68,71,73,74,75,81,84,90,91,94]
VCC5M VCC5M [35,41,63,64,73,83,84,85,86,87,90,91,92,93,95]
VCC5B VCC5B [41,45,57,59,61,65,66,67,71,73,75]
VCCCPUCORE VCCCPUCORE [9,85,88]
VCCGFXCORE_I VCCGFXCORE_I [10,86,88]
VCCSA VCCSA [11,87,88]
VCCST VCCST [7,11,16,24,43,70,84]
VCCSTG VCCSTG [7,11,43,70]
VCCCPUIO VCCCPUIO [5,6,11,89]
RTCVCC RTCVCC [14,21,25,45]
VCC0R6B VCC0R6B [27,28,91]
VCC3SW VCC3SW [25,40,41,42,43,44,45,47,60,62,82]
VCC1R2A VCC1R2A [7,11,17,27,28,91]
VCC1R35VIDEO VCC1R35VIDEO [33,34,35,37,76,94]
VCC2R5A VCC2R5A [27,28,75,92]
VCC1R0_SUS VCC1R0_SUS [7,20,21,24,70,90]
VDD10 VDD10 [41]

VCCGFXCORE_D VCCGFXCORE_D [31,35,76,93]
VCC3VIDEO VCC3VIDEO [31,34,35,93,95]
VCC3B_VGA VCC3B_VGA [34,35,76,93,95]
VCC1R05VIDEO VCC1R05VIDEO [31,33,34,76,95]
VCC1R5B_HDMI VCC1R5B_HDMI [57,75]
VCC1R5HDMI VCC1R5HDMI [75]
VCC1R8CODEC VCC1R8CODEC [75]
VCC1R8B_Codec VCC1R8B_Codec [45,75]

VCC3_SUS_SPI VCC3_SUS_SPI [19,26,55]
VCC5B_AVDD VCC5B_AVDD [45]
VCC5B_PVDD12 VCC5B_PVDD12 [45]
VCC3_SUS_DVDDIO VCC3_SUS_DVDDIO [45]
VCC3B_DVDD VCC3B_DVDD [45]
VCC3B_MINIDP VCC3B_MINIDP [59]
VCC3GBE VCC3GBE [51,52,53]
VCC3LAN VCC3LAN [51,72]
VCC3M_EC VCC3M_EC [43,44]
VCC3WWAN VCC3WWAN [62,74]
VCC3WLAN VCC3WLAN [62,74]
VCC5_TP VCC5_TP [66,71]
VCC3_MC VCC3_MC [54]
+UIM_PWR +UIM_PWR [62]
+USB_VCCA +USB_VCCA [63]

NOTE

1:NEED FIX SYMBOL
LV3301,LV3402,UL5201,U3401

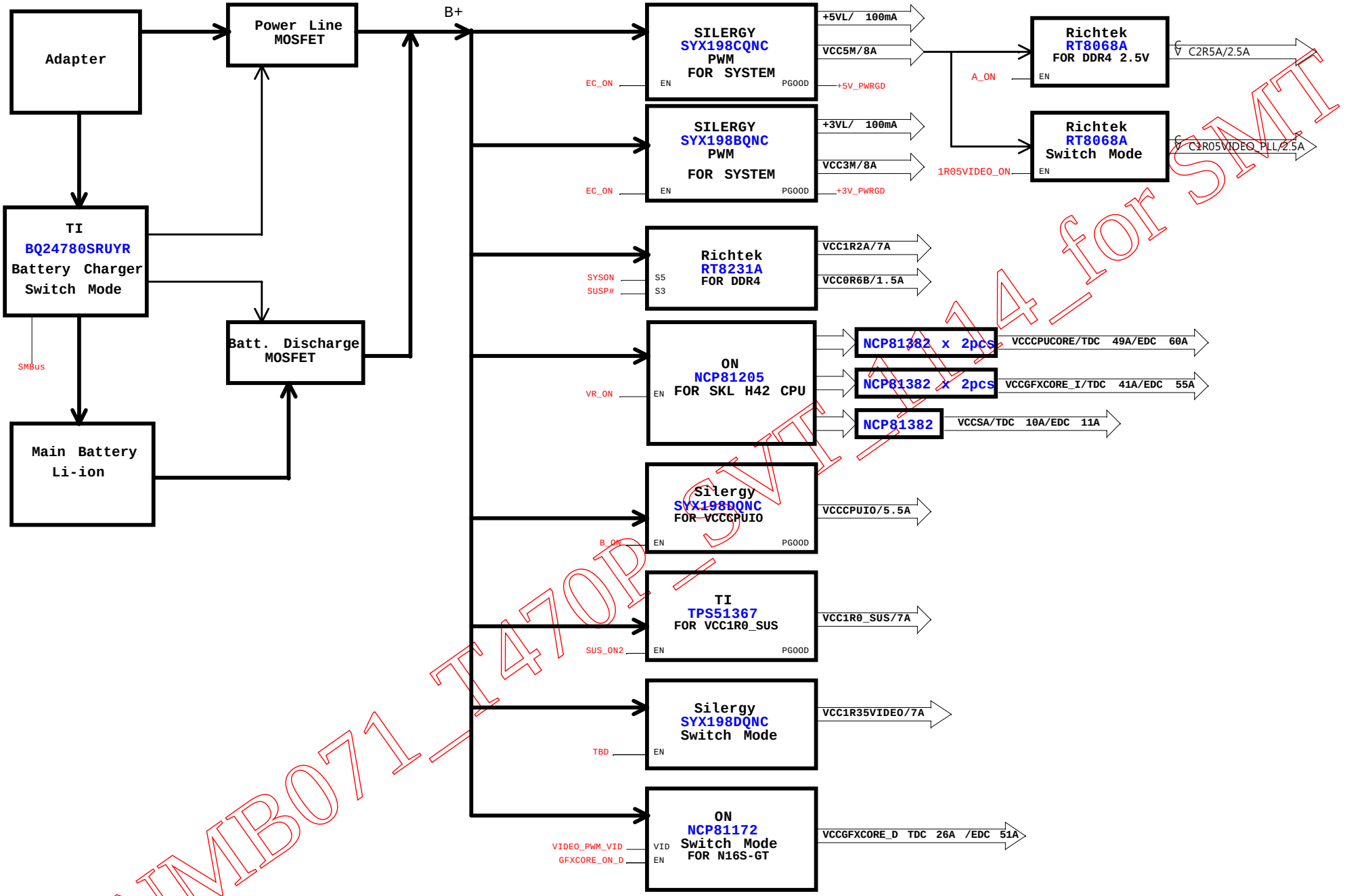
2:NEED APPLY PART NUMBER
LV3101==>FROM BLM18PG121SN1D TO BLM15PD121SN1

3:10 OHM ALREADY CHANGE 470 OHM
RV3465,R7604,R7608

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: POWER NET NAME

Size: Custom	Document Number: NM-A611	Rev: 0.1
Date: Wednesday, October 12, 2016	Sheet 96 of 99	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/01/12	Deciphered Date	2016/01/12

Title: PWR-PIR

Size	Document Number	Rev
Custom	AXXXX_NM-AXXX	0.1

Date: Wednesday, October 12, 2016 Sheet 97 of 99

LPX-Series

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/08	Deciphered Date	2013/11/08

Title: ***Load BOM Only(RTC BATTE***

Size	Document Number	Rev
B		0.2

Date: Wednesday, October 12, 2016 Sheet 98 of 98