SYSTEM PAGE REF.

X430 SCHEMATIC Revision

(FA : UMA)
(FN : DGPU = Nvidia N17S-G1, MX150)

BLOCK DIAGRAM

Non Connected Standby

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	057_DSG_Discharge
	058_PRO_Protect
	060_DC_DC & BAT IN
	064_
	065_ME_Conn & Skew Hole
	066_
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	068_B to B connector
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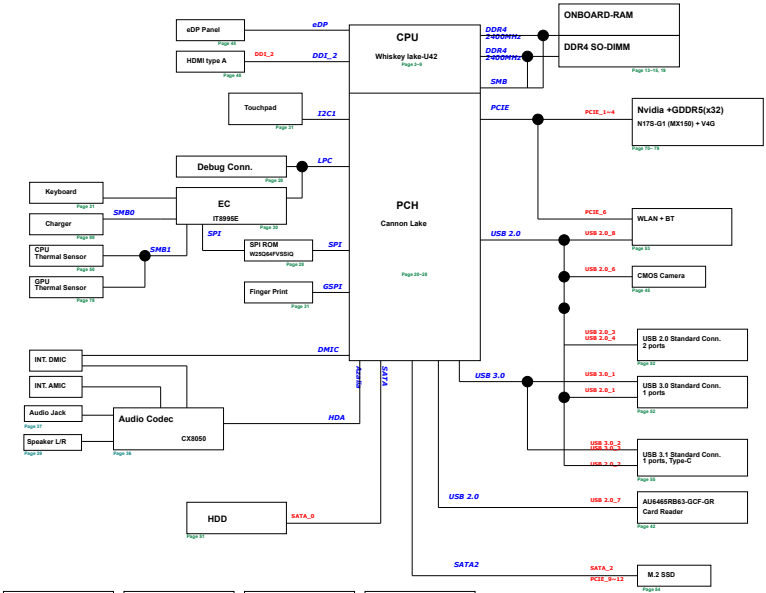
	071_VGA_nVIDIA_N16V/S_FB-IF
	072_VGA_nVIDIA_N16V/S_FB-DDR3
	073_VGA_nVIDIA_N16V/S_VDD
	074_VGA_nVIDIA_N16V/S_DISPLAY
	075_VGA_nVIDIA_N16V/S_ROM,XTAL
	076_VGA_nVIDIA_N16V/S_GPIO
	077_VGA_nVIDIA_N16V/S_POWER

080_PW_IMVP8 (1) (RT3601BCGQW)
081_PW_IMVP8 (2) (RT3601BCGQW)
083_PW_+1.0VSUS / +1.8VSUS
084_PW_+1.2VS
085_PW_1.35V/+0.675VS (UP9511Q)
087_PW_+3VADSW/+5VSUS (RT8249C)
088_PW_LOAD SWITCH
089.PW_CHARGER(BQ24780)
090_PW_PROTECTION
091_PW_DGPU_2PHASE(RT8815A)

Power

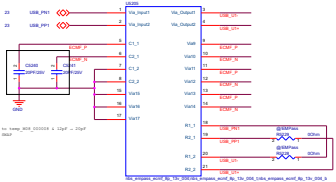
- +VCCGT +VCCCORE +VCCSA — Page 80 & 81
- +1.0VSUS / +1.8VSUS — Page 83
- +VCCPRIM_CORE — Page 84
- +1.35V / +0.675VS — Page 86
- +3VADSW/+5VSUS — Page 87
- Load Switch — Page 88
- Charger — Page 89
- +NVVDD — Page 91



Project Name	X430
Title :	Block Diagram
Dept.:	Engineer: EE
Date: Thursday, August 30, 2018	Sheet 1 of 106

0919-10 Daan

2014/05/15 G2320F_R1_0 #R1, C5205 modify to temp_MOS_000008 & 12pF -> 22pF
2014/05/15 G2320F_R1_0 #R4, C5203 100R/1% 0402F



0925-1 Daan

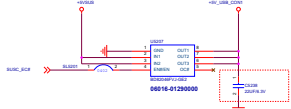
1003-6 Rick

1006-2 Rick
1027-2 Rick

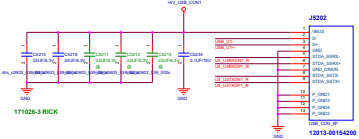
1108-1 Rick
1114-5 rick swap

2014/05/22 G2320F_R1_0 #R1, C5207 100R PWR EN2 enable modify to EC2C_EC4

USB3.0 port 0 Power SW for Power Protect

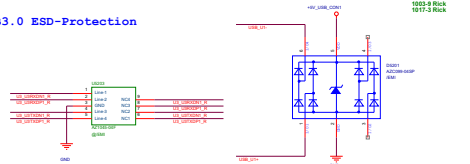


USB3.0_Port 0



USB3.0 ESD-Protection

1003-9 Rick
1017-3 Rick

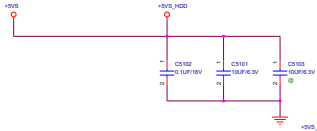


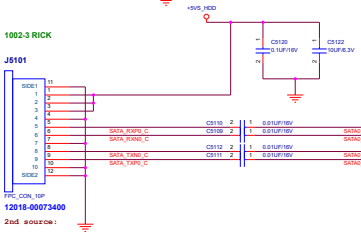
BOM

ASUS	Project Name: X430		Rev: R2.0
Title :	USB 3.0 + 2.0 CONN.		
Size:	Dept.: MSD(Mod. COMPUTER INC.	Engineer:	EE
Custom			
Date:	Thursday, August 20, 2015	Sheet: 32 of 56	

0919-5 Dean

1130-2 rick





s530 FFC PIN DEFINE

FFC	PIN DEFINE	SATA CONN
	GND	P11
	GND	P10
1	5V	P9
2	5V	P8
3	5V	P7
	GND	P6
	GND	P5
	GND	P4
4	GND	S7
5	RXP(B+)	S6
6	RXN(B-)	S5
7	GND	S4
8	TXN(A-)	S3
9	TXP(A+)	S2
10	GND	S1

.

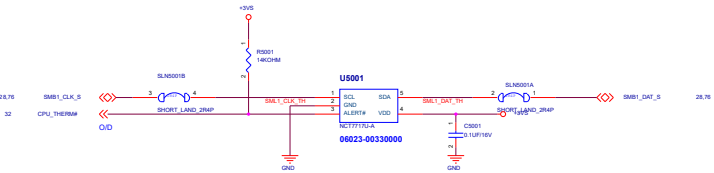
Reserve for EMI
170426 Shaun
change to 07G028076030 ESD
170427 Shaun
4-5 6-7 swaps
170428 Shaun

2018/05/10 X430FF_R1.0 #A5, Mount U5105 for ESD issue test

BOM

ASUS	Project Name: X430	Rev: R2.0
Title : SATA HDD & ODD		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Thursday, August 30, 2018	Sheet 51 of 104	

CPU Thermal Sensor



5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

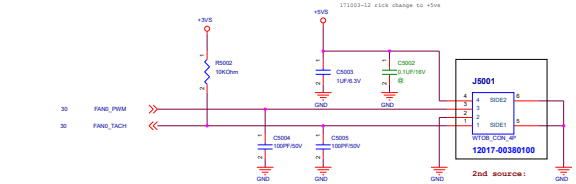
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS
Avoid FSB,Power

DC FAN Control

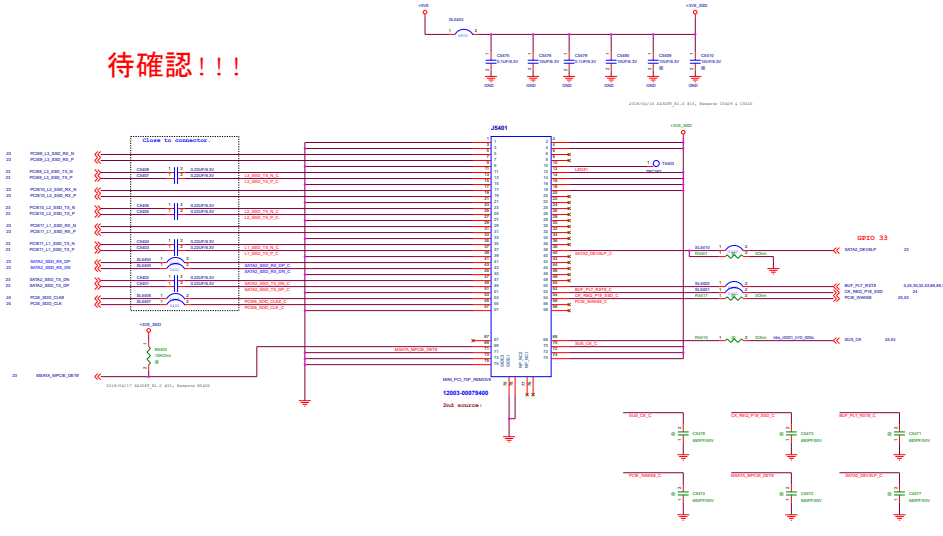


PCIe/SATA M.2 SSD

0915-1 Dean
0915-2 Dean
0922-6 Dean
1003-4 rick

待確認！！！

1109-4 rick



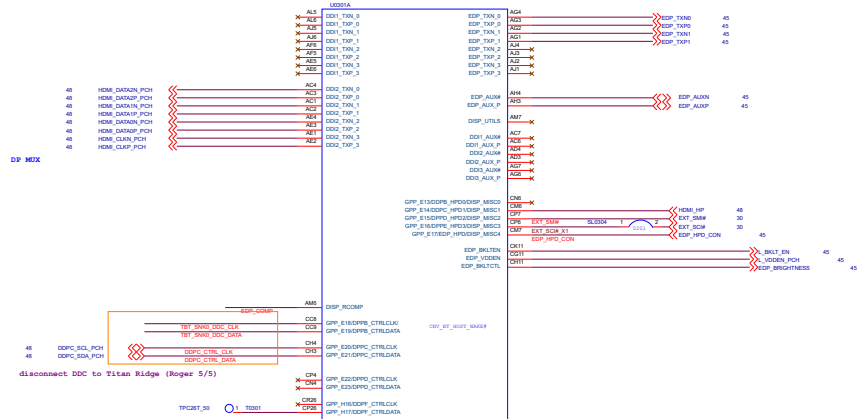
Title :	OTH_KB+TP+Camera		
Engineer:	EE		
Size	Project Name		Rev
Custom	X430		R2.0
Date: Thursday, August 30, 2018		Sheet 32 of 100	

WHL ES2 QS symbol ==> temp_T_002277 / nbs_bga_1528p_003

Display Port

A	EDP	
B	Type C(TBT1)	DP
C	Type C(TBT2 or Full function)	DP

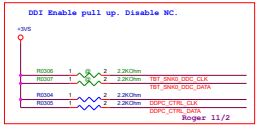
Intel Version	ASUS P/N



disconnect DDC to Titan Ridge (Roger 5/5)

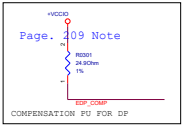
2018/04/26 1430DFP_R1.0 #79, Shamount #0304 & #0307

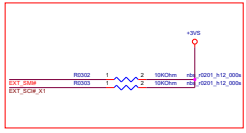
DDPC NC when no use KBL PDG R0.9 P.200



	HDMI
DDI_0	Lane2
DDI_1	Lane1
DDI_2	Lane0
DDI_3	CLK

PDG#543016 DDI1 mapping DDPB
DDI2 mapping DDPC





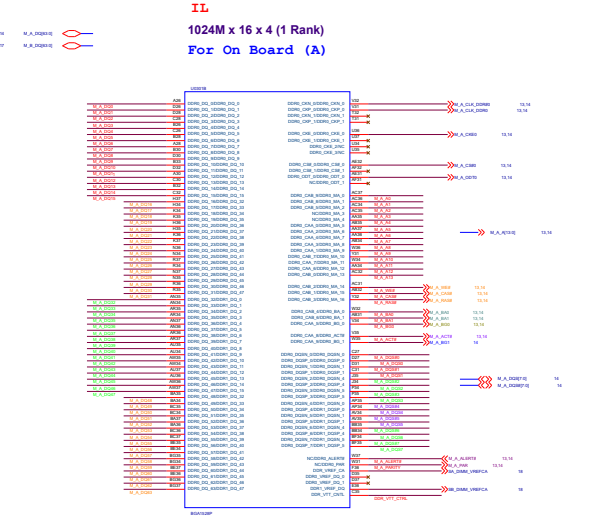
<Variant Name>

ASUS	Project Name: UX391RA		Rev: R2.0
Title : CPU_DISPLAY			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: Roger Liao	
Date: Thursday, August 30, 2018	Sheet 3 of 104		

IL

1024M x 16 x 4 (1 Rank)

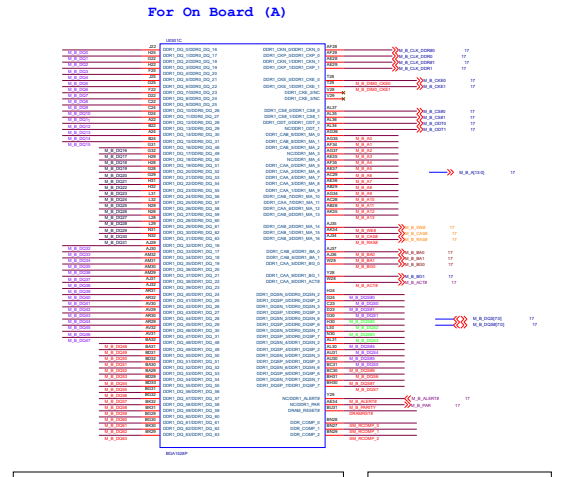
For On Board (A)



IL

1024M x 16 x 4 (1 Rank)

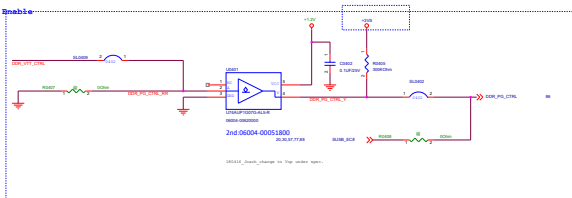
For On Board (A)



DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the Platform memory VTT regulator
in C8 and deeper and S3.
Ref:544024_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120

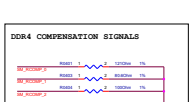
171107-5 RICK

VTT Enable



2nd:06004-00051800

DDR4 COMPENSATION SIGNALS



Notes:

1. Avoid any parallel routing for Memory down x16 Channel and SoDIMM Channel.
2. For CFL -U43e/WHL-U42 Rcomp[0] should be 121 Ohm.For CNL-U22 all RCOMP value 100 Ohm

Title :	CPU_DDR4		
Engineer:	Roger Liao		
Size: C	Project Name: UX391RA		Rev: R2.0
Date: Thursday, August 30, 2018	Sheet 1 of 100		

Notes:

1. R1 should be 50 Ohm for 3.3V and 33 Ohm for 1.8V. R1 is recommended to be placed 12.7mm (500 mils) from the PCH, but can be extended to 25.4 mm (1000 mils) maximum if required. The length of breakout section B0 is still 12.7mm (500 mils) maximum. R1 is not required for CS# signal.

2018/06/22 XX399F_R1_0 #62, R0511/23/16/39/60 change from 15 ohm to 49.9 ohm
2018/06/24 XX399F_R1_0 #66, R0511/23/16/39/60 change from 49.9 ohm to 0 ohm

U0301G

28	SPI_CLK_SPI_2	R0511	1	2	0Ohm	SPI_CLK_SPI_2_X1	CH37
28	SPI_SO_SPI_2	R0513	1	2	0Ohm	SPI_SO_SPI_2_X1	CF36
28	SPI_SI_SPI_2	R0539	1	2	0Ohm	SPI_SI_SPI_2_X1	CF34
28	PCH_SPI_IO2	R0540	1	2	0Ohm	PCH_SPI_IO2_X1	CG34
28	PCH_SPI_IO3	R0504	2	1	0Ohm	PCH_SPI_IO3_X1	CG36
28	SPI_CS#0_SPI_2					SPI_CS#0_SPI_2_X1	CH36

SPI_CLK
SPI_MISO
SPI_MOSI
SPI_IO2
SPI_IO3
SPI_CS#0
SPI_CS#1
SPI_CS#2

Series resistors move to P.28 0119

TBT

follow UX490

CLINK/FDO R1.2 P.834 If an AMT capable Intel WLAN device is not implemented, then this signal can be left as NO CONNECT (NC).

CF26 GPP_D1/SPI1_CLK/BK1/SBK1
CD22 GPP_D2/SPI1_MISO_IO1/BK2/SBK2
CF27 GPP_D3/SPI1_MOSI_IO0/BK3/SBK3
CD23 GPP_D4/SPI1_IO2
CH23 GPP_D5/SPI1_IO3
CG20 GPP_D6/SPI1_CS0#/BK0/SBK0

CH7 CL_CLK
CH8 CL_DATA
CL_RST#

BC328= Keyboard Controller Reset, Processor
30 RC_INI#
30 INT_SERIRQ
BV29 GPP_A0/RCINI#/TIME_SYNC1
BV28 GPP_A6/SERIRQ
INT_SERIRQ

BGA1528P

GPP_C0/SMBCLK
GPP_C1/SMBDATA
GPP_C2/SMBALERT#

GPP_C3/SML0CLK
GPP_C4/SML0DATA

GPP_C5/SML1CLK
GPP_C6/SML1DATA
GPP_C7/SML1ALERT#/CPUHOT#

GPP_A11/LAD0/ESPI_IO0
GPP_A10/LAD1/ESPI_IO1
GPP_A9/LAD2/ESPI_IO2
GPP_A8/LAD3/ESPI_IO3
GPP_A5/LFRAME#/ESPI_CS#
GPP_A14/SUS_STAT#/ESPI_RESET#

GPP_A0/CLKOUT_LPC0/ESPI_CLK
GPP_A13/CLKOUT_LPC1
GPP_A9/CLINK0/RM

CK14
CH15 SMB_CK
CJ15 SMB_DATA
TO XDP & DIM_SPD
TD501 1 2 TPC26T_S0
UX305UA no SODIMM only need to pull up

CH14
CF15 SML0_CK
CG15 SML0_DATA
GPP_A23
TO NFC

CN15
CM16 SML1_CK
CC34 SML1_DATA
SML1ALERT#
SMLink0 Advanced TCO Mode connect to EC monitor thermal sensor

CA29
BY29 PCH_LAD0
BY27 PCH_LAD1
BY23 PCH_LAD2
CA28 PCH_LAD3
CA27 LPC_FRAME#
BU28 SUS_STAT#
BV32 CLK_KBC/PCI_PCH
BV30 CLK_DEBUG
BY30 RM_CLKRUN#

2018/06/22 XX399F_R1_0 #53, Add R0533/20/21/23 For LPC & remove R0505/06/27/29
R0529 1 2 15Ohm LPC_AD0 29,30
R0521 1 2 15Ohm LPC_AD1 29,30
R0515 1 2 15Ohm LPC_AD2 29,30
R0523 1 2 15Ohm LPC_AD3 29,30
R0517 1 2 33Ohm ESPI_RST#
R0507 1 2 33Ohm ESPI_RST#
SLG5012 1 2 ESPI_RST#
Add ESPI_RST# connect to EC GPD2 for eSPI interface
26,30,32,53,54,68,69,70
2018/06/16 XX399F_R1_0 #62, Ref UX432 connect ESPI_RST# to BC_PLT_RST#
30
26
30

+3VS
R0522 1 2 8.2KOhm rtks_r5025_h12_000s PM_CLKRUN#
R0519 1 2 10KOhm rtks_r5025_h12_000s INT_SERIRQ

UX305UA CRB 1.1 P.20 150K PU ok 0318 change to 100K 0324

+3VSUS B1.1-5
R0508 1 2 100KOhm SML1ALERT#
R0503 1 2 2.2KOhm rtks_r5201_h12_000s SML1_CK
R0504 1 2 2.2KOhm rtks_r5201_h12_000s SML1_DATA
R0505 1 2 2.2KOhm rtks_r5201_h12_000s SML0_CK
R0506 1 2 2.2KOhm rtks_r5201_h12_000s SML0_DATA

+3VSUS
RN5505A 2.2KOhm
RN5505B 2.2KOhm
+12VS
Q0501A EMB41-G-T2R
Q0501B EMB41-G-T2R
SMB_CK
SMB_DATA
SMB_CK_S3
SMB_DATA_S3
+3VS
RN5506A 2.2KOhm
RN5506B 2.2KOhm
17
17
TO DIMM

TP for Boundary Scan Test
TD503
PCH_SPI_SO2
TPC26T_S0
SA

UX391RA add
+3VA_DSW
R0509 0Ohm
R0510 0Ohm
GPP_C3

GPP_C5: weak internal pull down

PU	SPI MOS
PD	LPC is selected for EC (Default)

GPP_C2: weak internal pull down

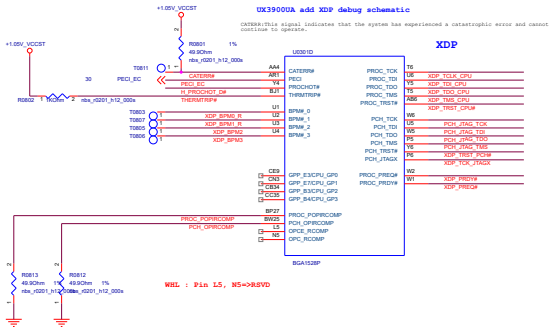
PU	Enable
PD	Disable Intel ME TLS cipher suite (no confidentiality) (Default)

Transport Layer Security (TLS) Confidentiality

UX305UA remove 0429

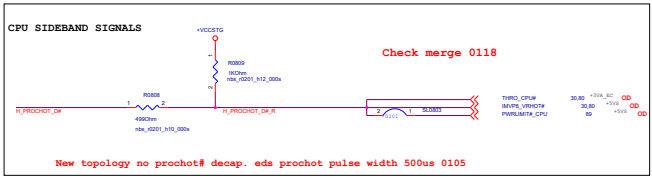
<Variant Name>

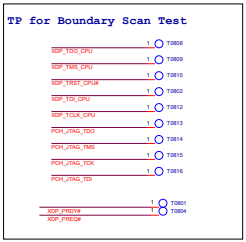
Project Name: UX391RA			Rev: R2.0
Title: CPU_LPC,SPI,SMB,CLINK			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Roger Liao	
Date: Thursday, August 30, 2018	Sheet: 5	of: 104	

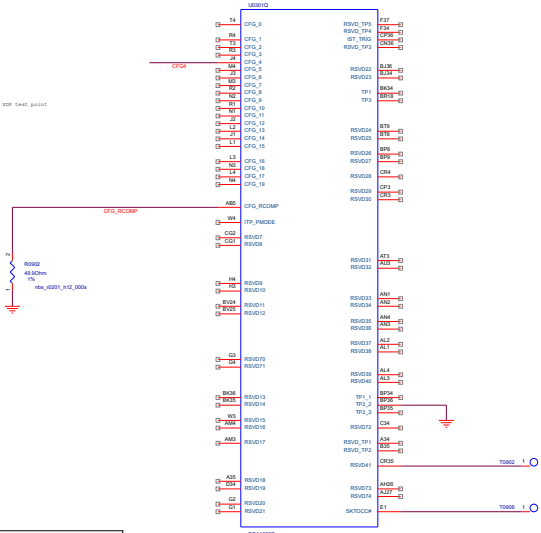


On Package Cache resistance Compensation
from processor: Refer to the appropriate platform
design guide for implementation details and values.
Unconnected for Processors without OPC.

No OPC Check remove 且R0811 R0810量測兩端為0V 0126

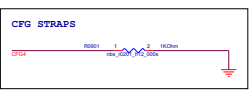






WHL : Pin C34, G1, G2, G3, G4, AM26, AJ27, B34, A35=>RSVD

CFG STRAPS



	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

<Variant Name>

ASUS Project Name: UX391RA — Rev: R2.0

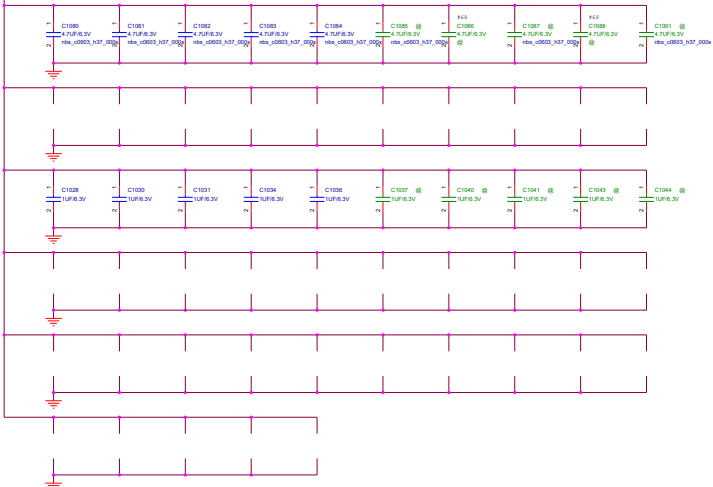
Title : CPU_CFG,RSVD

Size: Custom | Dept.: ASUSTeK COMPUTER INC. | Engineer: Roger Liao

Date: Thursday, August 30, 2018 | Sheet 9 of 104

VCCCORE

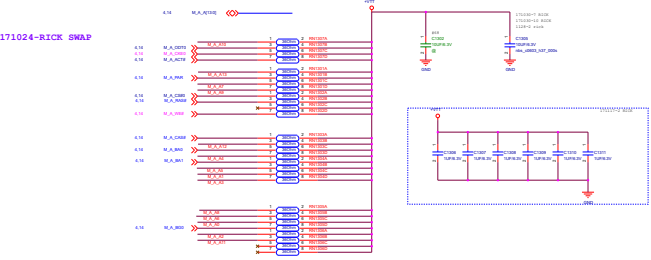
CPU - VCC DECAPS- Underneath the package

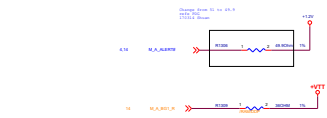


電容數需再評估!!!

ASUS	Project Name: UX391RA		Rev: R2.0
Title : CPU_POWER_CAP			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Roger Liao	
Date: Thursday, August 30, 2018	Sheet: 10	of: 104	

171024-RICK SWAP





BG1 Rtt for DDP.

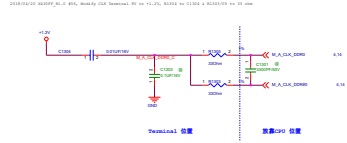
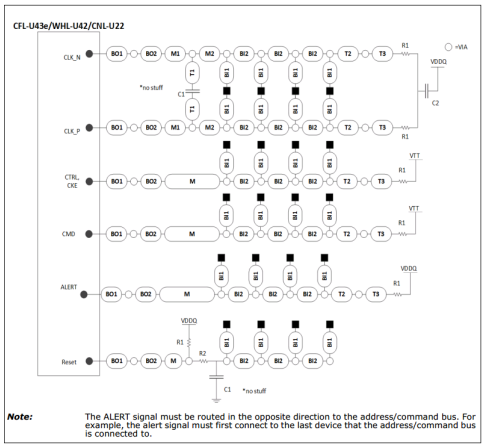
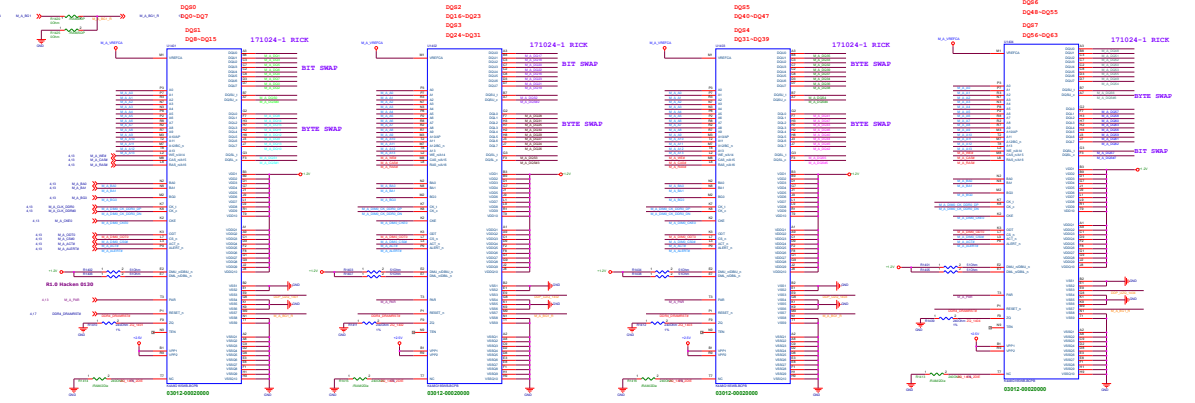


Figure 4-7. WHL U DDR4 x16 Memory Down CLK/CTRL/CKE/CMD/Reset Signal Topology



Note: The ALERT signal must be routed in the opposite direction to the address/command bus. For example, the alert signal must first connect to the last device that the address/command bus is connected to.



待確認...

Del DIM Thermal Sensor

Close U1401

Close U1402

Close U1403

Close U1404

Close U1401

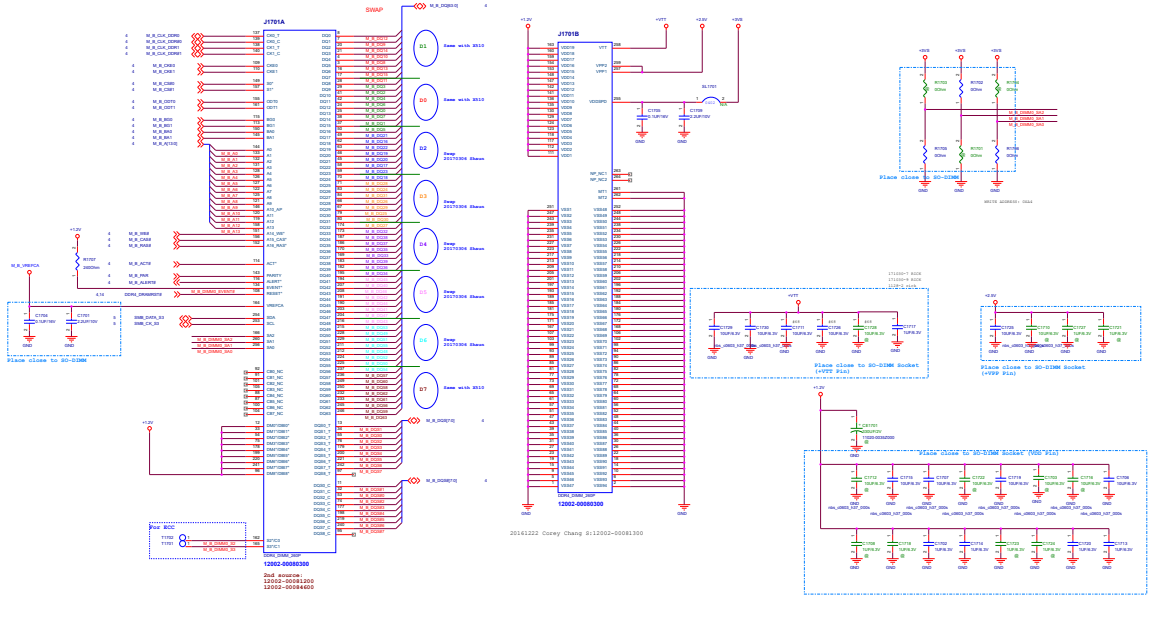
Close U1402

Close U1403

Close U1404

Title :	DDR4_ON-BOARD_A1
Engineer:	ME
Size	X430
Rev	
Sheet	

DDR4 4H SO-DIMM



'EVENT_N' : INDICATES THERMAL EVENT ON DIMM.
NON-ECC DIMM: NOT CONNECTED

EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH

Title :	DDR4_SO-DIMM_1		
Engineer:	NB EE2		
Size	Project Name		Rev
C	X430		R0.0
Date: Thursday, August 06, 2015		Sheet 17 of 56	

Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V_{REF-CA} Overview

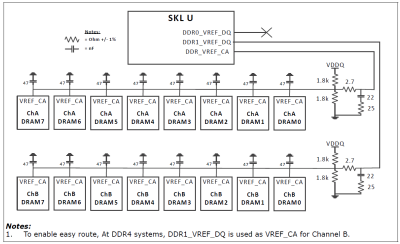
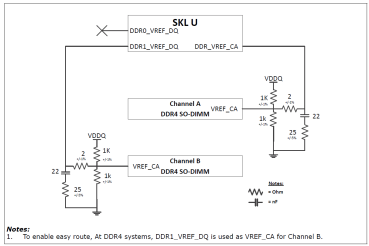
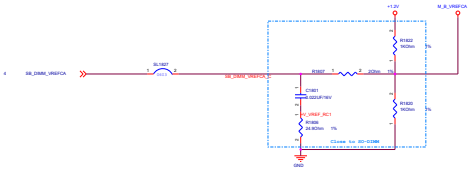
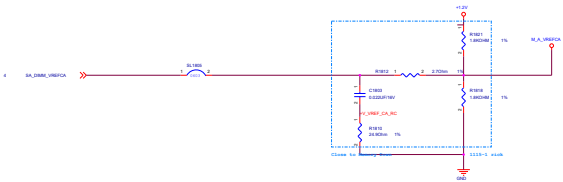


Figure 4-49. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



All Vref trace must be 20 mils width

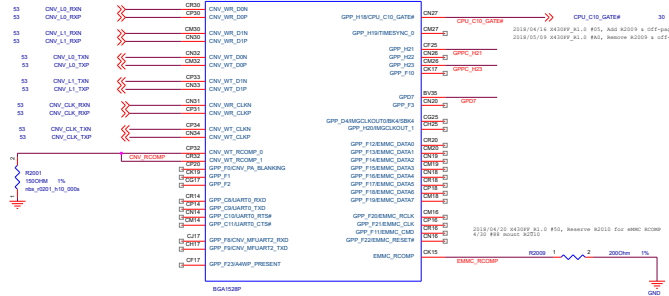




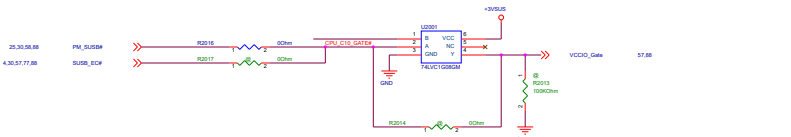
Title : DDR4 CA VOLTAGE			
Engineer: NB EE2			
Size: C	Project Name: X430		Rev: R2.0
Date: Thursday, August 30, 2018	Sheet	of	

CNVi Wlan module

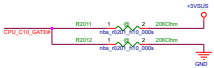
TBT



2018/05/09 X430FF_R1.0 #A1, Add U2001 current for VCCIO PWR gate

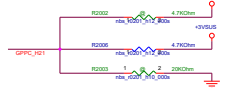


2018/05/09 X430FF_R1.0 #99, Reserve PU (R2011) & PD (R2012) for CPU_C10_GATE#

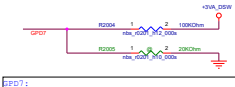


2018/04/26 X430FF_R1.0 #77, GPPC_H21 modify PU to +3VSUS (ROM option)

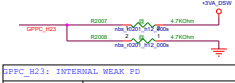
CFL CRB v0.8 page#44



GPPC_H21:	
PU	24Mhz
PD	38.4/19.2MHZ



GPD7:	
PU	XTAL INPUT IS SINGLE ENDED
PD	XTAL IS ATTACHED



GPPC_H23: INTERNAL WEAK PD	
PU	SAF
PD	MAF

<Variant Name>

Project Name: UX391RA			Rev: R2.0
Title : CPU_PCH_CSI2,EMMC			
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: Roger Liao	
Date: Thursday, August 30, 2018	Sheet 20 of 104		

Remove ISH ALS_INT# 0331

Delete ISH by Roger11/3

Change to +3V5 0506

6. The signal is high-Z output with
no glitch.Free pull-down resistor during the pin power sequencing

UX391 add PD_I2C_IRQ

For finger printer Reset use

EC Request

Touch pad

CNVi Wlan module

Onboard Memory PCB-ID:
GPC_12 => DIMM_SEL2
GPC_13 => DIMM_SEL1
GPC_14 => DIMM_SEL0

PCB-ID0 GPP_D9
PCB-ID1 GPP_D10

DRAM Part Number		DIMM_SEL2	DIMM_SEL1	DIMM_SEL0	
93012-60020500	SDR4 2400 512MF16 //MICRON/MT40A512M16LY-075:E	0	0	0	BOM
93012-60020300	SDR4 2400 512MF16 //SKHYNIX/H5AN8G8NAFR-UHC	0	0	1	BOM
93012-60020400	SDR4 2400 1G2MF16 //SAMSUNG/K4A8G165WC-BCRC	0	1	0	BOM
93012-60040100	SDR4 2400 1G2MF16 //SAMSUNG/K4AAG165WB-BCRC	0	1	1	BOM
93012-60040200	SDR4 2400 1G2MF16 //MICRON/MT40A1G16KNR-075:E	1	0	0	BOM
		1	0	1	
		1	1	0	
NO-DIMM only		1	1	1	

Add new KBOM No 93012-60030400
Roger 11/3
170810 Shawn

Refer helpertalk change these RAM note 170810

1211-5 vick

No Reboot

UX305UA remove 0429

NOTE: Enable No Reboot
EC will disable the TCO.
Then system will not reboot.
Note: System is valid when running SUS/S0X.

PCH_GPP018: weak internal pull down	
PU	Enable
PD	Disable

Boot BIOS Strap Bit BBS

PCH_GPP022: weak internal pull down	
PU	LPC
PD	SPI (Default)

UX391RA add 0504

PCH_GPP26: weak internal pull HIGH	
PU	INTEGRATED CNVI DISABLE
PD	INTEGRATED CNVI ENABLE

UX391RA add 0803

PCH_GPP012:
Internal pull-up is required
(CNL_PCH EDS 0.7 #56)

HD Audio

RN2201 near PCH

38	ACZ_BCLK_PCH	33Ohm	5%	1/16W	R2201	
38	ACZ_SYNC_PCH	33Ohm	5%	1/16W	R2202	ACZ_BCLK_AUD_R1
38	ACZ_RST#_PCH	33Ohm	5%	1/16W	R2203	ACZ_SYNC_AUD_R1
38	ACZ_SDOUT_PCH	33Ohm	5%	1/16W	R2204	ACZ_RST#_AUD_R1
						ACZ_SDOUT_AUD_R1

0402 change to 0201 0105

2016/04/14 SCHPT_R1.0 #01, Modify ACZ_RST#_PCH current. Remove Q2201B & Q2202A modify to 2N7002.

C2202,C2203,C2204, CFL PDG: 2PF

38 ACZ_SDIN0_PCH

ACZ_SYNC_AUD_R1
ACZ_BCLK_AUD_R1
ACZ_SDOUT_AUD_R1
ACZ_SDIN0_AUD

ACZ_RST#_AUD_R1

C2202 0.1UF/16V
C2203 0.1UF/16V
C2204 0.1UF/16V

53 RP_RESET#_B

53 CLKREQ2

45 DMIC_CLK_PCH
45 DMIC_DAT_PCH

R2207 1 2 22OHM
DMIC_CLK_PCH_R1

For EMI request

C2201 10PF/50V
@DMIC_PCH

TP2201_SD
TPC2201_SD

U2201G

B24	HDA_SYNC/I2S0_SFRM	GPP_D0/SD_CMD
B23	HDA_BCLK/I2S0_SCLK	GPP_D1/SD_DATA0
B20	HDA_SDO/I2S0_TXD	GPP_D2/SD_DATA1
B22	HDA_SDI0/I2S0_RXD	GPP_D3/SD_DATA2
B19	HDA_SDI1/I2S1_RXD/GENINT_DATA	GPP_D4/SD_DATA3
A24	HDA_RST#/I2S1_SCLK/GENINT_CLK	GPP_D5/SD_CD#
A23	GPP_D23/I2S_MCLK	GPP_D6/SD_CLK
		GPP_D7/SD_WP
BL37	DBI_SFR#/SNDW3_CLK	
BL31	DBI_TX/SNDW3_DATA	

C2302	GPP_H15/I2C_SFR#/	CMC_MB_I2C_SCL0/CMC_MP_SMBUS
C2303	GPP_H0/I2C0_SCLK/	CMC_MP_I2C_SCL0
C2304	GPP_H1/I2C0_TXD/	CMC_MP_I2C_SDA/MCHPE_CLKREQ
C2305	GPP_H2/I2C0_RXD/CNV_RF_I2S_SDO	
CP54	GPP_C7/I2C_C_CLK/GENI2C_CLK	GPP_A17/SD_VDD1_PWR_ENB/SIM_GPT
CN24	GPP_C6/I2C_C_DAT/GENI2C_DATA	GPP_A15/SD_1P8_SEL
C2025	GPP_D17/I2C_C_CLK1/GENI2C_CLK	SD_1P8_RCOMP
C2026	GPP_D18/I2C_DAT/1/GENI2C_DATA	SD_3P3_RCOMP
CP55	GPP_B14/SPKR	

BGA1528P

BA28	GPP_A0/ESPI_IO0	
BA27	GPP_A1/ESPI_IO1	
BA26	GPP_A2/ESPI_IO2	
BA25	GPP_A3/ESPI_IO3	
BA24	GPP_A4/ESPI_CS0#	
BA23	GPP_A5/ESPI_CLK	
BA22	GPP_A6/ESPI_RST#	
BA21	GPP_A7/ESPI_ALERT0#	
BA20	GPP_A8/ESPI_ALERT1#	

CK30	SD_1P8_RCOMP	
CK34	SD_3P3_RCOMP	

R2208 1 2 200Ohm 1%

GND

ST8962 BML_GPAL_REV 2DB TOE Backpl

2016/04/26 SCHPT_R1.0 #02, Remove R2205 & reconnect SD_1P8_RCOMP to SD_3P3_RCOMP &CN/ 2MM Rotary ALPS#

FLASH DESCRIPTOR STRAP

EDS 31.7.1.3

HDA_SDO
0=Enable
1=Disable Override

ACZ_SDOUT:(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65*3.3V (2) ALC269:VIL<0.35*3.3V, VIH>0.65*3.3V

VCCHDA=+1.8VS

+VCCHDA

R2222 2.2KOhm ohm_4\201_1/12_5\5%

ACZ_SDOUT_AUD_R1

R2223 33Ohm ohm_4\201_1/12_5\5%

Q2201_S

Q2201 2N7002K

30 PCH_SPI_CV

ACZ_SDOUT is a signal used for Flash Descriptor security Override?HE debug mode HIGH : get overridem, LOW : disable override

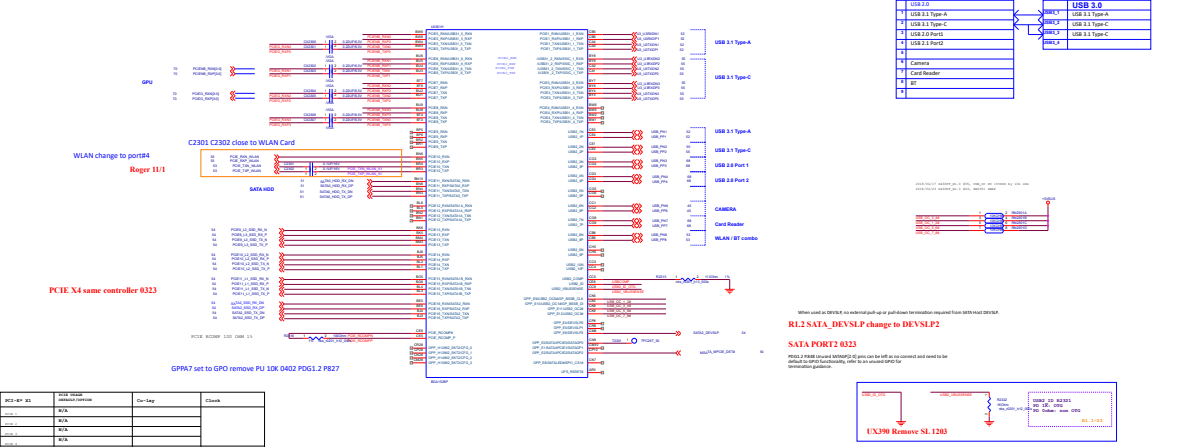
Intel: To enable Flash Descriptor Security Override, this signal should be pulled up to VCCHDA through a 1 KΩ to 2.2 KΩ ±5% resistor.

Top-Block Swap Override

Remove 0429 EDS 4.3.1

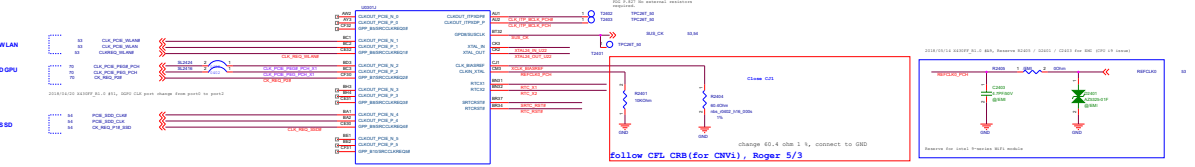
PCH_GPP_B14: weak internal pull down	
PU	Enable
PD	Disable (default)

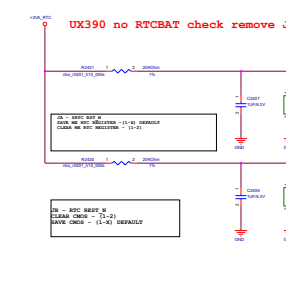
Title :	CPU_PCH_AUDIO,SDIO,SEMC		
Size: C	Project Name: UX391RA		Rev: R2.0
Date: Thursday, August 30, 2018	Dept.: ASUSTeK COMPUTER INC.	Engineer: Roger Liao	
	Sheet 22 of 104		

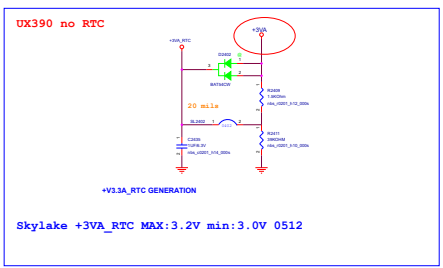


PCI-E* X1	PCIE USAGE DEFAULT CONFIG	Co-lay	Clock
PCIE_1	N/A		
PCIE_2	N/A		
PCIE_3	N/A		
PCIE_4	N/A		
PCIE_5	WLAN		Port5
PCIE_6 / SATA_0	SSD	SATA_SSD	Port0
PCIE_7/SATA_1	SSD		
PCIE_8	SSD		
PCIE_9	SSD		
PCIE_10/SATA_2	N/A		

Project Name	UX391UA
Rev	REV
Title	CPU_PCH_PCIE,SSD,SATA
Size	Document Number
Custom	Date: Thursday, August 06, 2015 Sheet of
Dept.	Engineer: Roger Lee







Project Name	UX391RA
Title	CPU_PCH_CLOCK SIGNALS,RTC
Size	C
Dept.	ASUSTeK COMPUTER INC.
Engineer	Roger Liao
Date	Thursday, August 30, 2018
Sheet	26 of 104

Main Board

UX391 add SLP_S5#, SLP_A# TP

UX305UA remove LAN_WAKE# 0506

UX390 remove WLAN_ON# option1203

UX390 remove PLTRST buffer 1203

UX390 remove PME option 1203

UX390 remove VRALERT# option 1203

UX305UA remove SLP_WLAN# SLP_LAN# SLP_A# 0429

PCH STRAPS

Roger 3/21

SPI: 3V SELECT STRAP	
LOW	3.3V +/-5%
HIGH	3.0V +/-5%

LAN_WAKE#=PCH_GPD2 PDG1.2 P.849Connect this signal on PCH to EC. 0319

R2559 change to 1K to reduce power consumption0330

ADD 0302 prevent PCH floating

TP for Boundary Scan Test

Remove +3VSUS route 0429

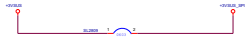
Power failure solution (S0-->G3,S5-->G3);

2014/04/09-1

Project Name	UX391RA
Title :	CPU_PCH_SYS_POWER
Size	
Dept.:	MB&ME&AE-CQ/PRJ/SW&C
Engineer:	Roger Liao
Date:	Thursday, August 29, 2013
Sheet	20 of 109

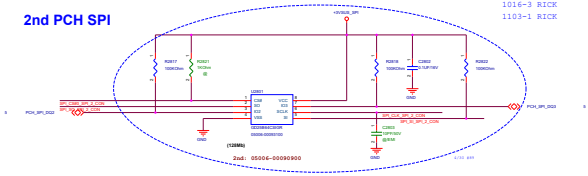
SPI PCH Power

1003-11 RICK

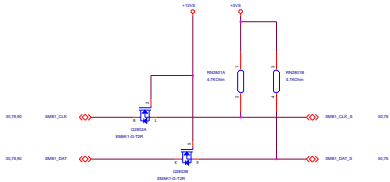


2nd PCH SPI

1016-3 RICK
1103-1 RICK

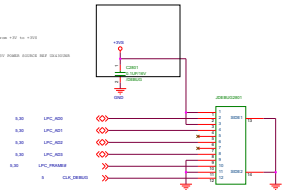


確認是否更換SPI ROM 用料



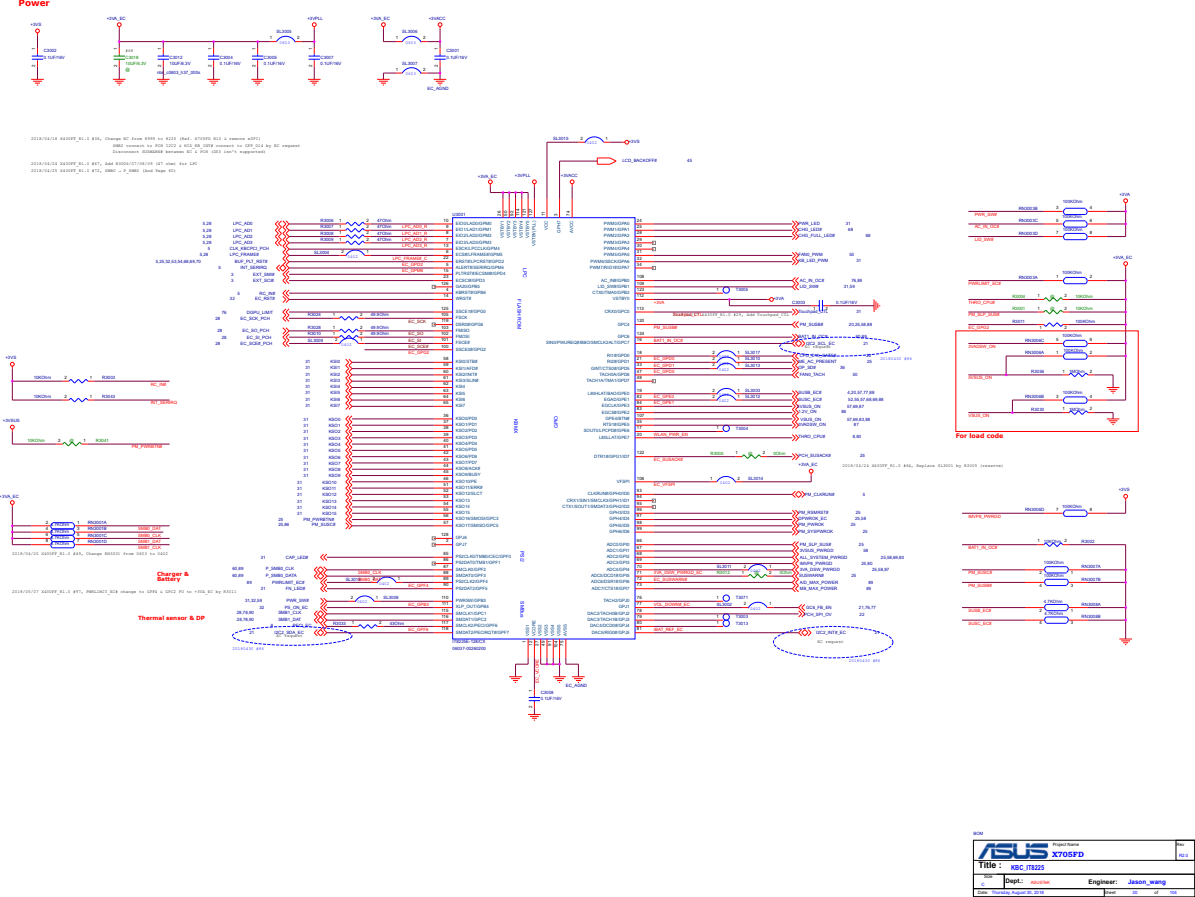
LPC Debug Port

同面CABLE



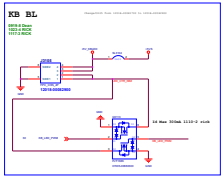
2nd source:

ASUSTeK COMPUTER INC.	Title :	2S_PCH-SPI ROM,GTH	
	Engineer:	EE	
Size	Project Name		Rev
C	X430		REV
Date: Thursday, August 30, 2018	Sheet	28	of 31


Power
+3VS
+3VA_EC
+3VPLL
+3VALW_EC
+3VACC
EC_AGND
LCD_BACKOFF#
+3VALW
+5VALW
+1.5VS
+1.5VALW
+VSB
+VSB_EC
Charger & Battery
Thermal sensor & DP
For load code
BOM
Project Name
X705FD
Title : KBC_IT8225
Engineer: Jason_wang
Date: Thursday, August 30, 2018
Sheet 35 of 104

Internal Keyboard

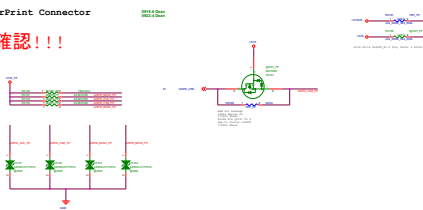
KB BL



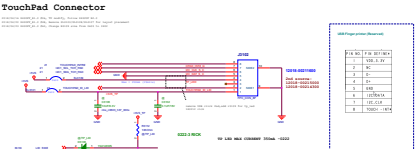
FingerPrint Connector

0910-2 Dunn
0922-2 Dunn

待確認！！！

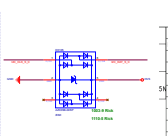


TouchPad Connector



USB Finger printer (Reserved)

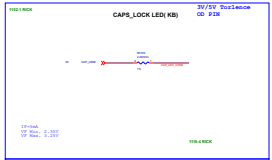
PIN NO.	PIN DEFINE*
1	VDD_3.3V
2	NC
3	D-
4	D+
5	GND
6	INTR/TX
7	I2C_CLK
8	TOUCH - RTX

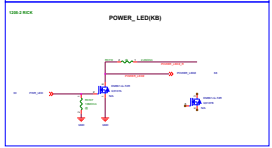


CN1		CN2	
PIN NO.	PIN DEFINE*	PIN NO.	PIN DEFINE*
1	VDD_3.3V_FP	1	VDD_3.3V_FP
2	GND	2	FP_RSTN
3	PS2_CLK	3	FP_MOSI
4	PS2_DATA	4	FP_INTN
5	GND	5	FP_MISO
6	SDA	6	FP_CSN
7	SCL	7	FP_SCK
8	INT	8	GND

KB Function LEDs

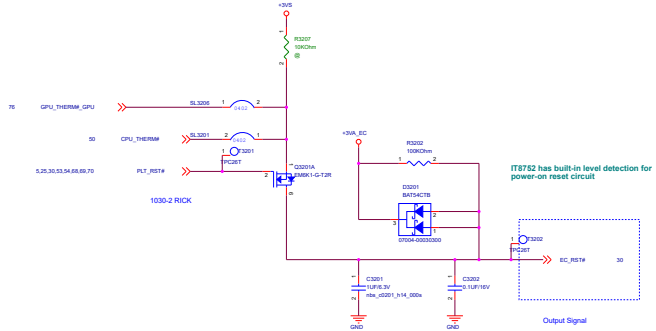
0910-7 Dunn
0928-13 Dunn
DEL KB PWR LED



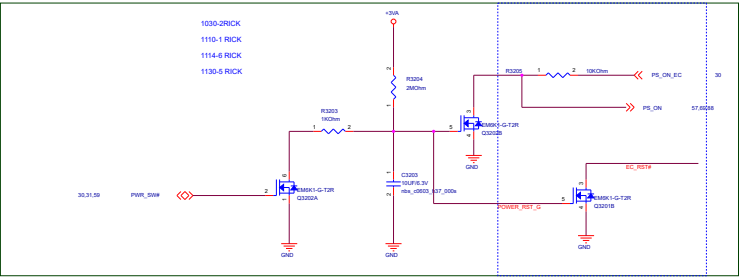


Project Name			Rev
ASUS	X543D		
Title :	ELUTIL-SLT		
Size	Doc#	Date: Monday, August 06, 2018	Sheet of
Engineer:	MB		

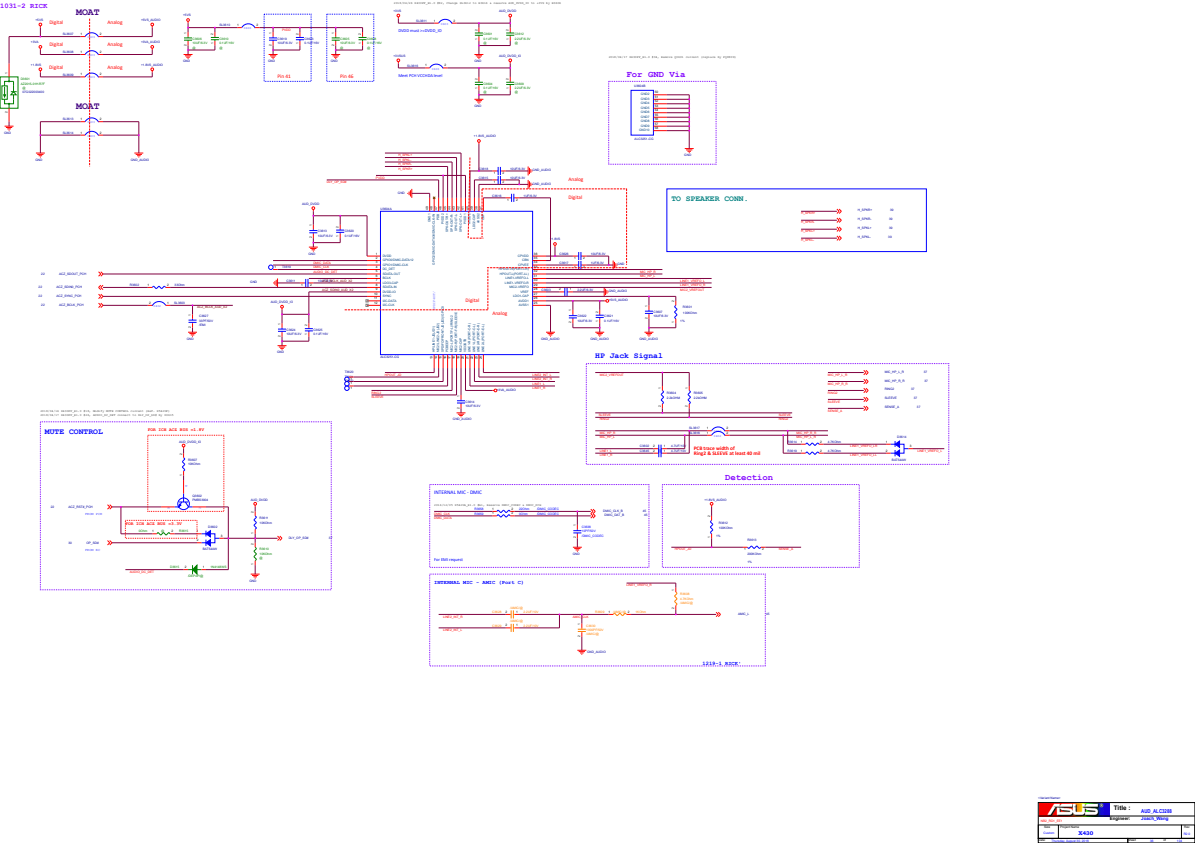
Thermal Policy



battery embedded (press pwr_sw 10sec, then reset ec)



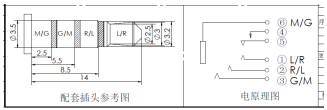
Audio Cdeco ALC3251



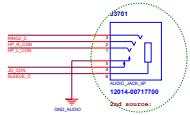
ASUS	Title :	ASS_ALC3288	
File Location:	Engineer:	Jason_Wang	
Size:	Project Name:		Rev:
Custom	X430		
Date: 2014/06/06 Wednesday 09:49:05	Sheet	of	1.00

Audio Jack

1031-2 RICK



JD pin = Normal open.



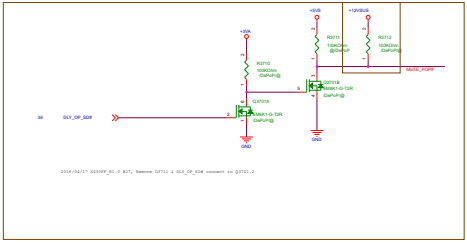
flow con. list chang J3701 form 12014-00710100 to 12014-00717700
1022-2 RICK

1030-1 RICK

PCB trace width of
Ring2 & SLEEVE at least 40 mil

1031-2 RICK
1101-1 RICK
1128-3 RICK

Headphone depop circuit

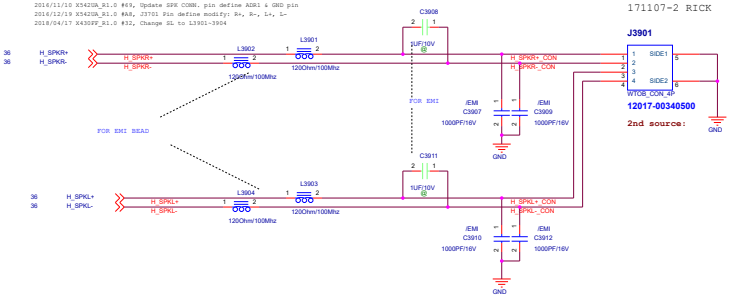


Max = 4W / Channel
I = 0.7 A (@Speaker : 8 Ohm)

SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 60mils

INTERNAL SPK Conn.

Check



<Variant Name>

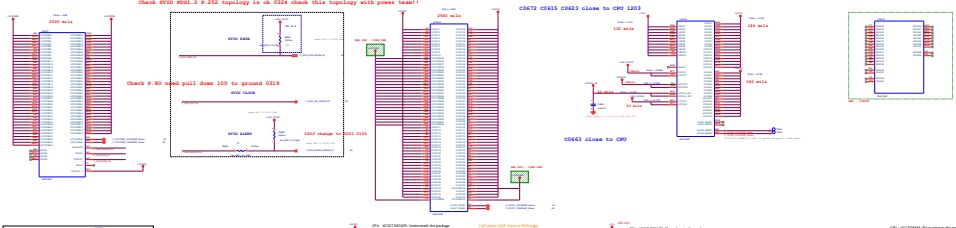
ASUSTeK COMPUTER INC. NB4

Title : AUD-SPEAKER CONN.

Engineer: EE

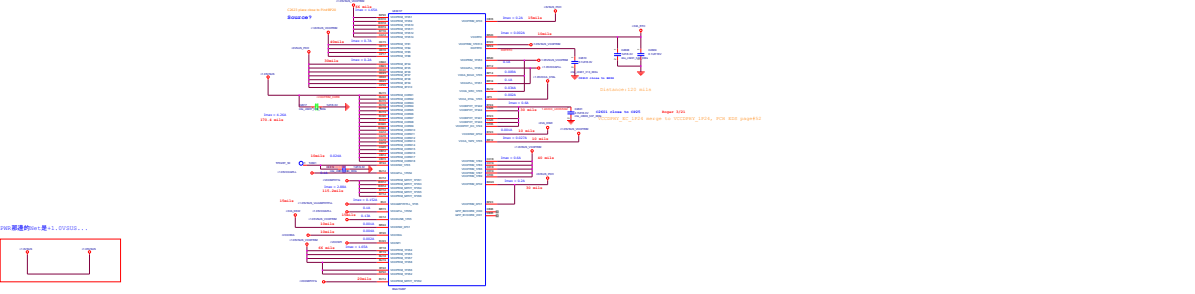
Size	Project Name	Rev
B	X430	R2.0

Date: Thursday, August 30, 2018 Sheet 39 of 104



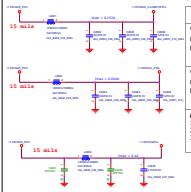
Power Plane:

+VCCCORE	
+VCCSA	System Agent power rail
+VCCGT	Silicon graphics power rail
+1.2V_VCCPLL=+VCCSE	CPU PLL power rails
+VCCIO_CPU=+VCCIO=+VCCSTG	IO power rail Gated version of VCCST
+VCCPLL_1V=+1.2V	CPU digital PLL power rails
+VDDQ_CPU=+1.2V	CPU Memory power rail, voltage dependent on memory technology
+VCCST	Sustain voltage for processor in Standby modes
+VCC_EDRAM_EGFIO	
+VCC_EDRAM_1.8S	



Filter requirement for +1.05VSUS

LC size 0603->0402 DCR MAX 0.3 ohm 0126



Filter Requirements for CFL U PCH

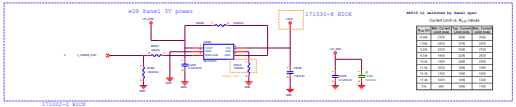
Supply	Value	Quantity	Type	Notes
VCCA_XTAL_1P05 (Pin F1) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47 uF	1	Filter Capacitor 0603	X5R rating capacitor recommended
VCCAMPHYPLL_1P05 (Pin B22) Note 1, 3	2.2 uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47 uF	1	Filter Capacitor 0603	X5R rating capacitor recommended

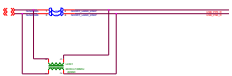
Notes:

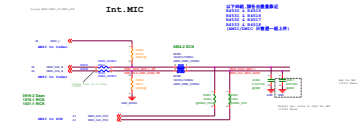
1. Placeholder is only. Does not need to be stuffed.
2. All capacitors are edge capacitors unless labeled otherwise.
3. 2x 22uF 0603 caps can optionally be used instead of 1x 47 uF 0603 caps. Caps should be with X5R temperature characteristics.

ASUS	UX391UA	Rev
Title :	ZIN_PCH_PWR.SCH	
Size :	Project :	Engineer : Roger Lee

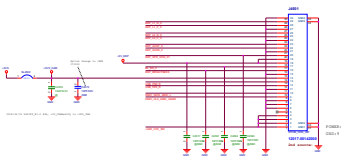
eDP (LVDS) Panel







171005-3 RICK 改30PIN



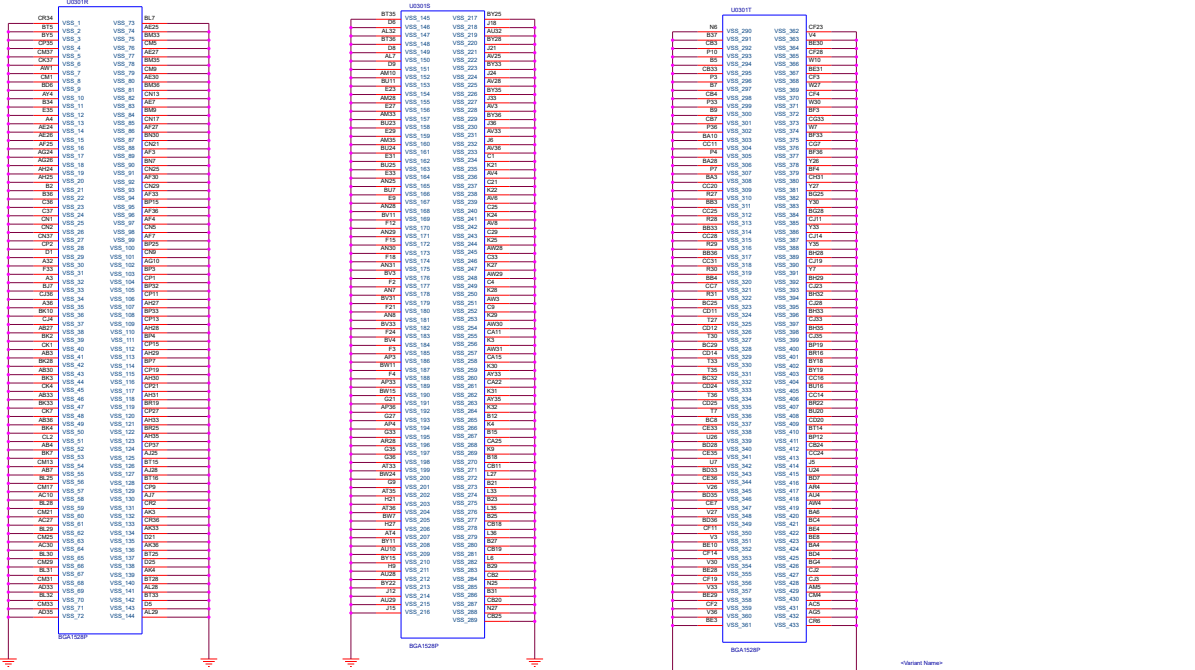
1005-3 RICK REF K401UA/C202SA Change J4501 from 40PIN 12017-00181600 to 30PIN 12017-00142000

1006-1 RICK Change J4501 back to 40PIN 12017-00181600

1016-1 RICK REF K401UA/C202SA Change J4501 from 40PIN 12017-00181600 to 30PIN 12017-00142000

1108-3 Rick modify J4501.15 NC to GND (page45)

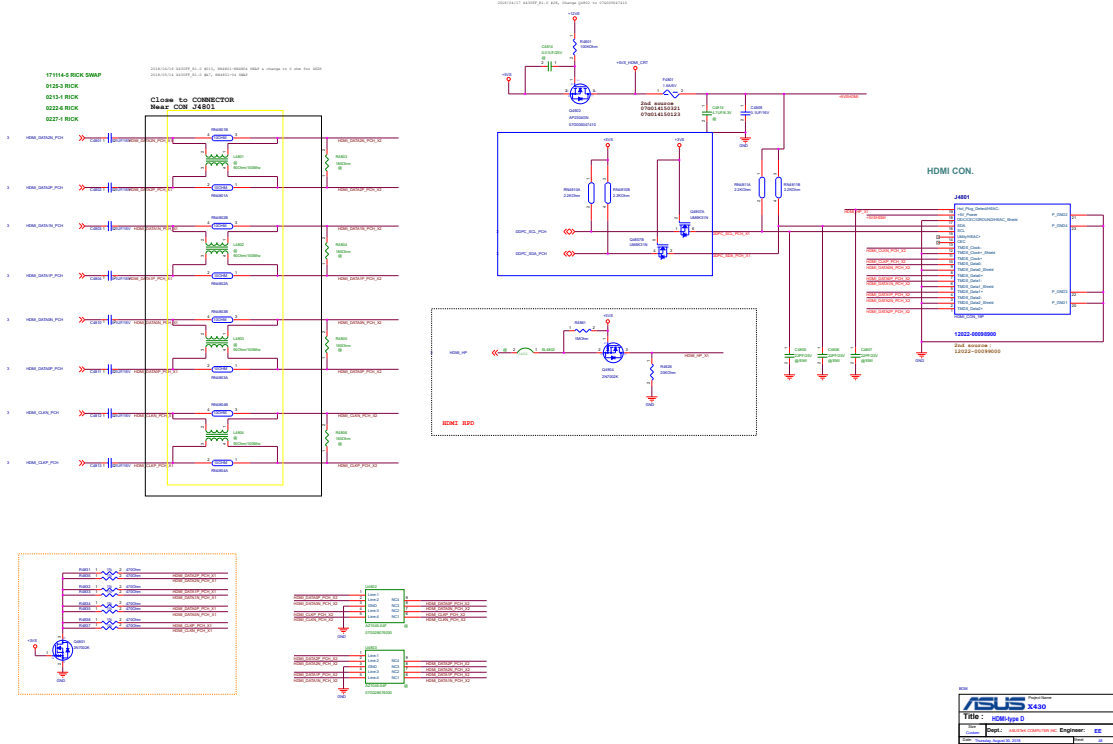
ASUS	Size: B4GD	Rev:	
Title:	LCD Panel CONN 30NC		
Date:	Sheet:	Engineer:	

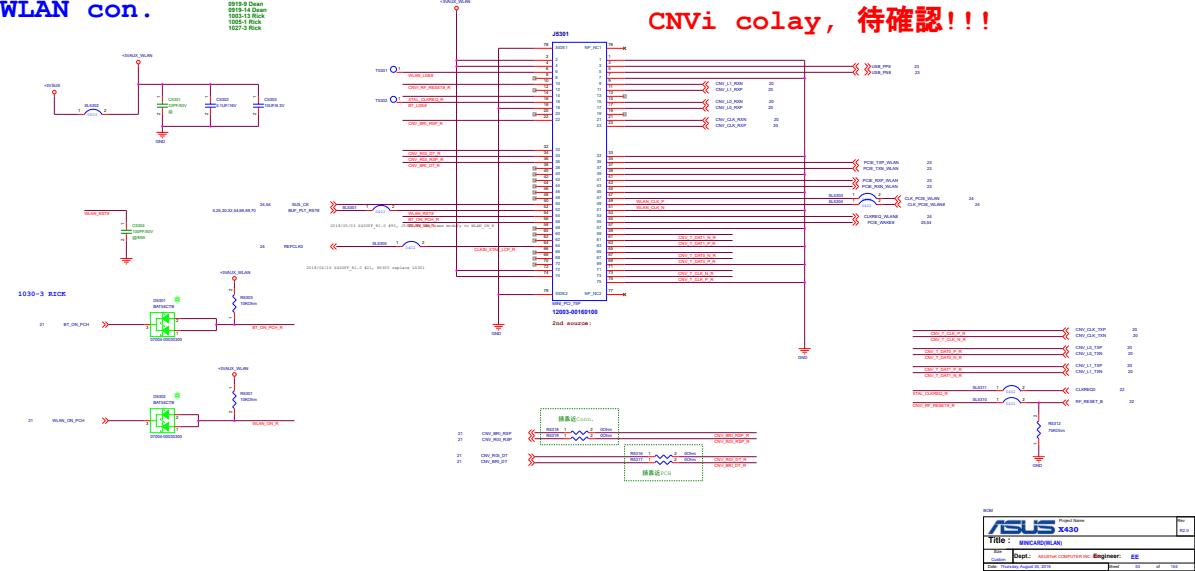


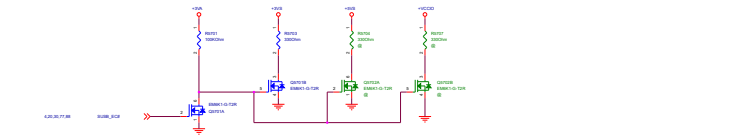
<Variant Name>

ASUS	Project Name: UX391RA		Rev: R2.0
Title : CPU_PCH_POEWR,GND			
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer: Roger Liao	
Date: Thursday, August 30, 2018	Sheet: 27	of: 104	

HDMI type-A

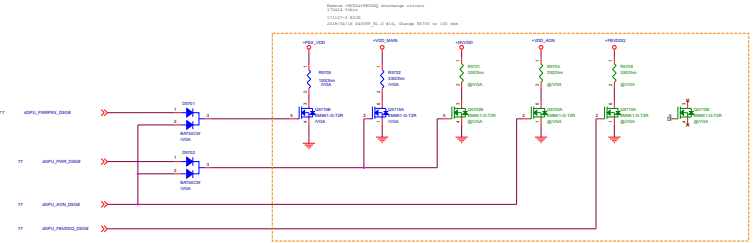

171114-5 RICK SWAP
0125-3 RICK
0213-1 RICK
0222-6 RICK
0227-1 RICK
Close to CONNECTOR
Near CON J4801
HDMI CON.
J4801
2nd source
0790014150321
0790014151223
HDMI HP
HDMI ESD


WLAN con.
0918-9 Dean
0918-14 Dean
1003-13 Rick
1005-1 Rick
1027-3 Rick
CNVi colay, 待確認!!!
J5301
12003-00160100
2nd source:
1030-3 RICK
X430
MINICARD(WLAN)
ASUSTeK COMPUTER INC.
Engineer:
EE

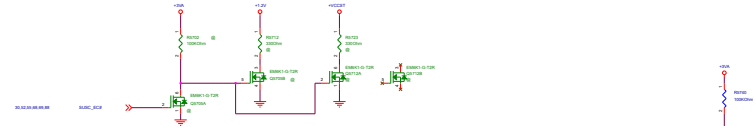


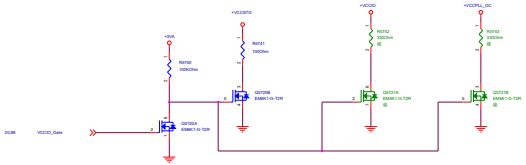
170927-rick
改用ux430un 相同設計
ADD +5VTOD4+FBVDDQ discharge circuit&VDD_AON

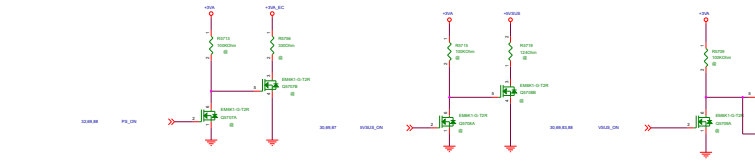
171103-2-rick



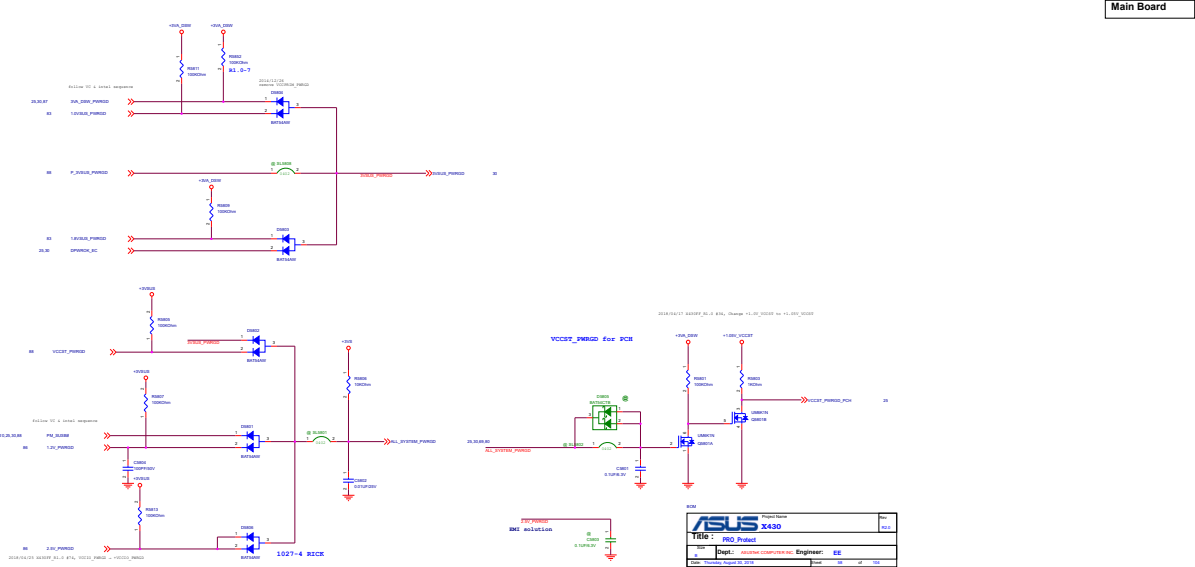
171114-7 -rick







Main Board


+3VA_DSW
+3VA_DSW
R9871
100KOhm
R9852
100KOhm
R1.0-7
2014/12/26
remove VCCRCOR_PWRGD
follow VC 1 intel sequence
29,30,87
3VA_DSW_PWRGD
83
1.0VSUS_PWRGD
D9858
BAT54AW
88
P_3VSUS_PWRGD
@ SLG659
R=0.1%
3VSUS_PWRGD
3VSUS_PWRGD
30
+3VA_DSW
R9859
100KOhm
83
1.0VSUS_PWRGD
D9857
BAT54AW
29,30
DPWROK_EC
2018/04/17 ADDOPT_R2.0 #34, Change +1.05V_VCCST to +1.05V_VCCST
+3VSUS
R9828
100KOhm
D9852
BAT54AW
88
VCCST_PWRGD
3VSUS_PWRGD
+3VS
R9836
10KOhm
C9862
0.01UF/25V
+3VSUS
R9857
100KOhm
follow VC 1 intel sequence
29,30,32,88
PM_SLEEP#
84
1.2V_PWRGD
D9867
BAT54AW
@ SLG601
R=0.1%
ALL_SYSTEM_PWRGD
C9863
1000PF/50V
+3VSUS
R9813
100KOhm
D9856
BAT54AW
88
2.5V_PWRGD
1027-4 RICK
2018/04/23 ADDOPT_R1.0 #74, VCCIO_PWRGD = +VCCIO_PWRGD
VCCST_PWRGD for PCH
+3VA_DSW
+1.05V_VCCST
R9821
100KOhm
R9822
1KOhm
VCCST_PWRGD_PCH
25
D9855
BAT54CTW
@
29,30,88,90
ALL_SYSTEM_PWRGD
@ SLG657
R=0.1%
C9851
0.1UF/6.3V
U9857A
U9857B
PCH_PWRGD
EM2 solution
C9853
0.1UF/6.3V
BOM
Project Name
X430
Rev
R2.0
Title :
PRO_Protect
Size
A
Dept.:
ASUSTeK COMPUTER INC.
Engineer:
EE
Date:
Thursday, August 30, 2018
Sheet
68
of
104

1121-3 RICK

1123-1 RICK

NUT

A-CPU

TOP置件!!

B-GPU

TOP置件!!

C-SSD

BOT

D-WLAN

BOT

HOLE

1211-1 RICK

0223-1 RICK

H1

H2

0223-1 RICK

H3

0223-1 RICK

H4,H6,H13

H7

H10,H12

H11

1211-1 RICK

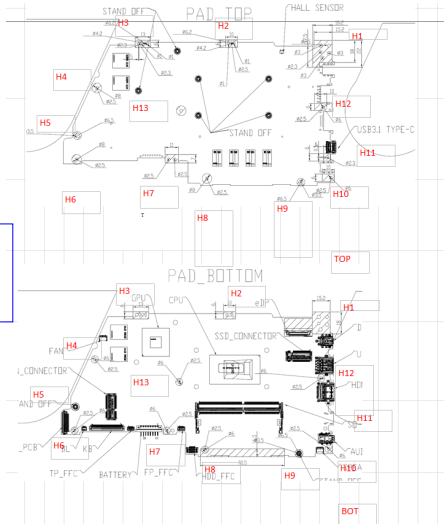
H8

1212-1

PAD

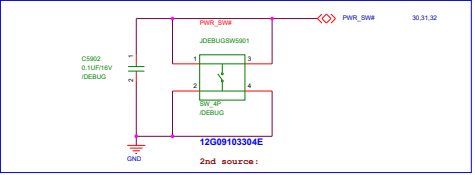
P1

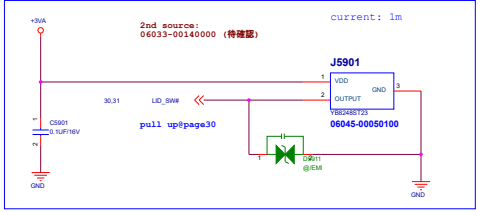
1215-1 RICK



DXF :s430_mb_pcb_dxf_3_20171120

ASUSTeK COMPUTER INC. taipei	Title :	05_MB_Conn & Show Hole	
	Engineer:	EE	
Size: C	Project Name: X430		Rev: REV:0
Date: Thursday, August 30, 2018	Sheet	50 of	50





1003- 8 RICK
MOVE TO IO BD

1027- 5 RICK
ADD LID CKT

待確認！！！

<Variant Name>

ASUSTeK COMPUTER INC. NB8	Title : 59_Power & WIFI & CAP LED	
	Engineer: EE	
Size: B	Project Name: X430	Rev: R2.0
Date: Thursday, August 30, 2018	Sheet 59 of 104	

Modify Common Chock
RF required
170503 Shaun

0925-1 Daan
1002-6 RICK
1006-2 RICK
1106-1 RICK

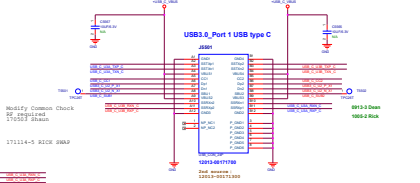
From PCH

USB3.0 Bus

USB3.0 Bus

Modify Common Chock
RF required
170503 Shaun

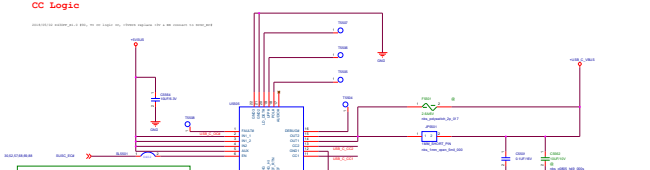
171114-5 RICK SWAP



6913-3 Daan
1005-2 Rick

RICK Change JT5501 from 12013-00119300 to 12013-00171700
171005-2 rick

CC Logic



CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

USB2.0 ESD-Protection

Modify ESD COMMON CHOCK circuit
170313 Shaun

1003-9 Rick

USB3.0 ESD-Protection

ASUS	Project Name: X430			Rev: REV.0
TITLE : USB 3.1 Gen 1 Type-C				
Size: Custom	Dept:	Engineer:	ED	
Date: Thursday, August 03, 2017		Sheet: 33	of: 106	

USB
Card Reader

AU6465

mode		Vin(V)	Iin (mA)	mW
AU6465 (Enable Power saving mode)	Suspend with card	3.3V	0.33	1.1
	Suspend without card	3.3V	0.14	0.46
	Idle with card	3.3V	32.8	108.24
	Idle without card	3.3V	0.14	0.46
	operating	3.3V	119	392.7

Use SanDisk SDHC 8G card (Extreme Pro)

Imax = 0.5A

40ai1

1123-2 Kappa

119mA

40ai1

0626-2 Dean

1022-8 Dean
1026-1 Dean
1030-1 Dean

0630-1 Dean

X'tal

AU6465 CLK source : External CLK or X'tal
XTALSEL : 0 = 12Mhz, 1 = 48Mhz(default)
AU6465K : Build in X'tal

1114-3 Dean

MICRO SD SOCKET

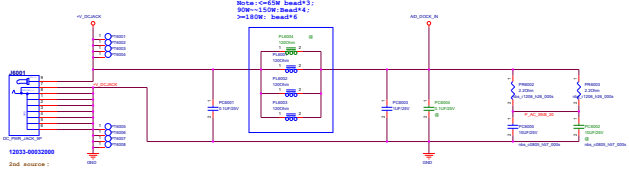
FOR EMI

0316-2 Kappa
0113-2 Kappa
1109-3 Kappa
0204-2 Kappa

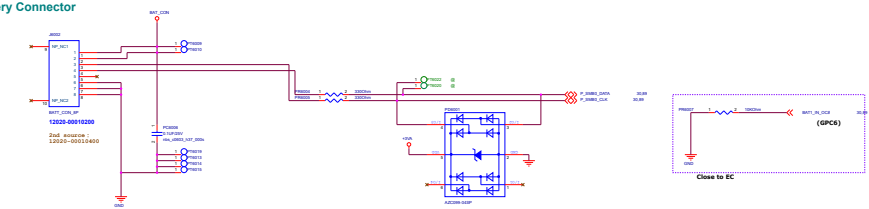
1123-2 Kappa
0311-1 Kappa
1030-2 Dean
1106-2 Dean

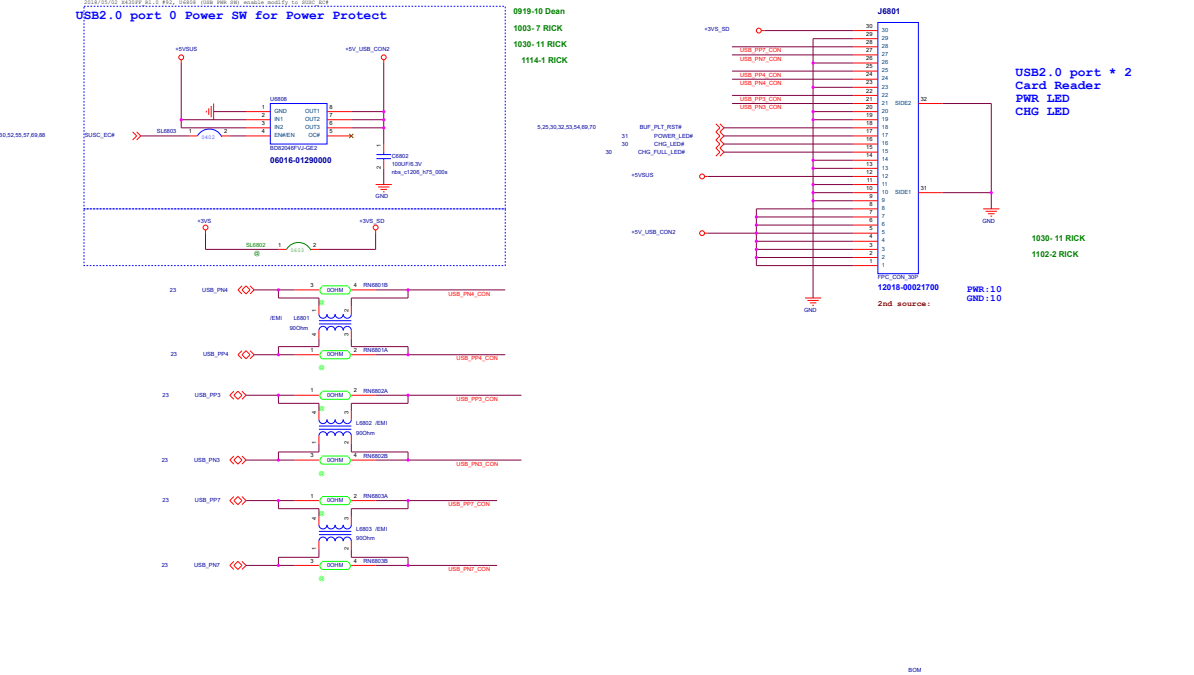
12023-00100100

Title :	IO_BD-2(AU6465RB63)		
Engineer:	EE		
Size	Project Name		Rev
Custom	X430		R2.0
Date: Thursday, August 05, 2010	Sheet 37 of 104		



Battery Connector





BOM

ASUS	Project Name: X430		Rev: R2.0
Title : B TO B CONNECTOR			
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Thursday, August 30, 2018	Sheet: 68	of: 104	

EMI

GASKET

1123-3
1220-1

1123-3

1116-3
rick
CLOSE
U7002

1123-4

(8637.00 3847.00)、(6033.00 4309.00)、
(4781.00 3811.00)、(1942.00 2601.00)、
(4091.00 1330.00)

(7307.00 1884.00)

Bot (7749.00 2054.00)
Bot (4963.00 3847.00)
Bot (1341.00 1064.00)

(4667.00 2511.00)、(3232.00 2663.00)、(5580.00 3595.00)

Bot (7573.00 2882.00)

Bot (7646.00 2012.00)

Top (1167.00 1759.00)

Top (1256.00 1847.00)

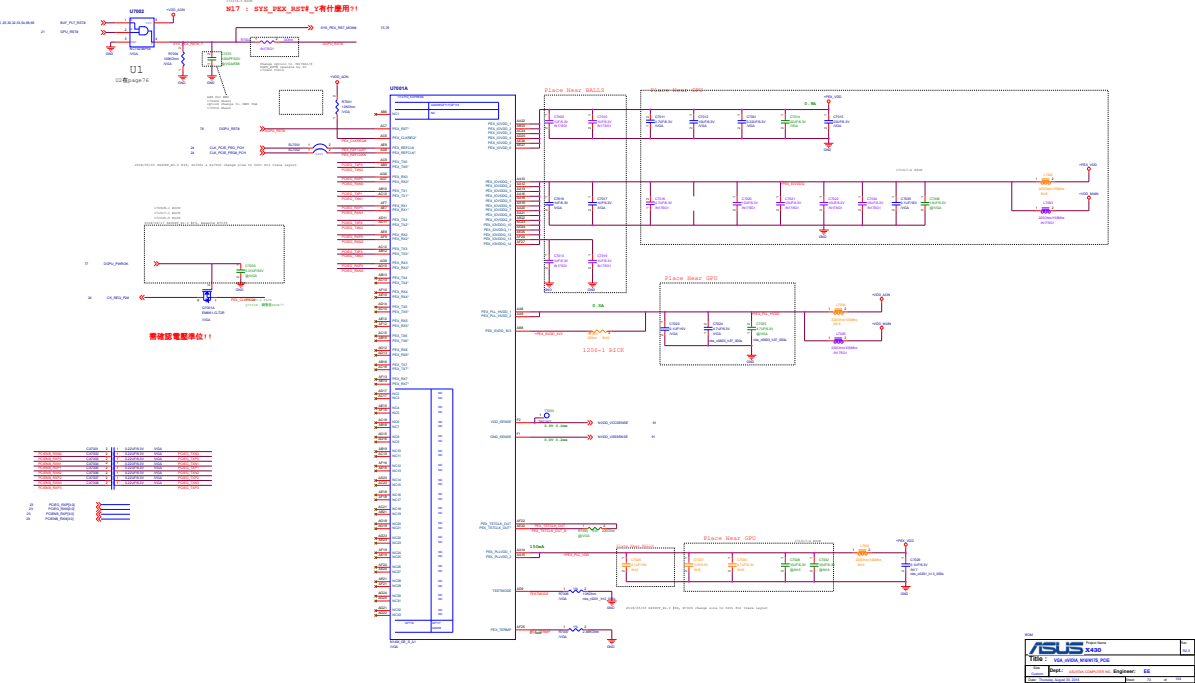
Top (1256.00 1847.00)

Top (1256.00 1847.00)

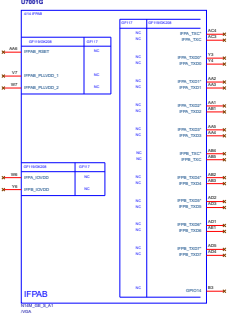
(BOT 5595.00 , 4157.50)

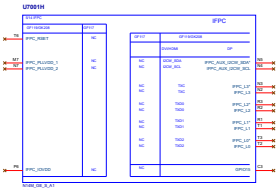
BOM

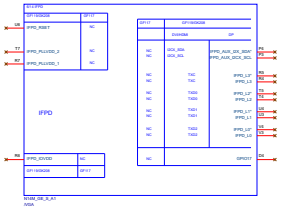
ASUS	Project Name: X430		Rev: R2.0
Title : EMI			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE	
Date: Thursday, August 30, 2018	Sheet: 69 of 104		


NI7 : SYS_PEX_RST#_Y有什麼用?!
Place Near BALLS
Place Near GPU
Place Near GPU
Place Near GPU
Place Near GPU
0.9A
0.3A
120H-1 RICK
電容認電壓準位!!
U7001A
U7002
U1
ASUSTeK
Title : VGA_nVIDIA_MAHAL5_PCIE
Project Name : X430
Engineer: EE

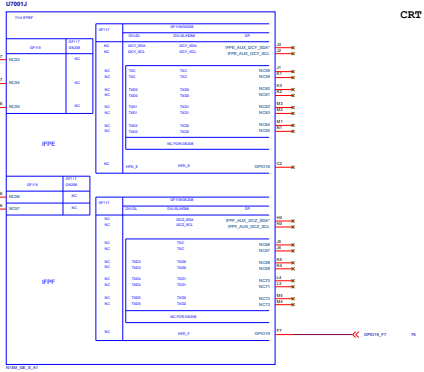
LVDS

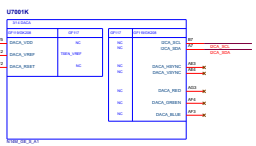


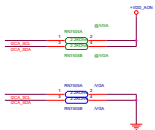




CRT







Title : VGA_nVIDIA_N16M11S_DISPLAY			
Size	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Thursday, August 20, 2015	Sheet 73 of 164		

Level shift
N17:1.8V
N16:3.3V

GPIO

U7001N

U2

VR Complex

GPU

ASUSTeK COMPUTER INC.

Project Name: X430

Title : VGA_nVIDIA_N16N17S_GPIO

Engineer: EE

Dept.:

Date: Thursday, August 30, 2018

Sheet 78 of 104

1. +VDD_AON
N17 : 1.8V
N16 : 3.3V

dGPU Power Sequence

170928-3 RICK DEL N17 GPAK ckt.

2. +VDD_MAIN

4. +PEX

MAIN_EN to PEX_VDD PG : Max 6ms

3. NVVDD_EN

5. +FBVDD_EN

6. GPU_POWER_GOOD

N17X-PWR SEQ

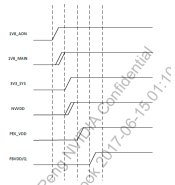


Figure 5. H17/G82C-64 GPU Power-Up Sequencing

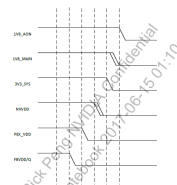


Figure 6. H17/G82C-64 GPU Power-Down Sequencing

N16X-PWR SEQ

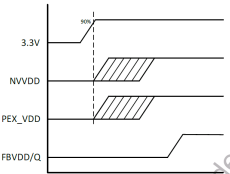
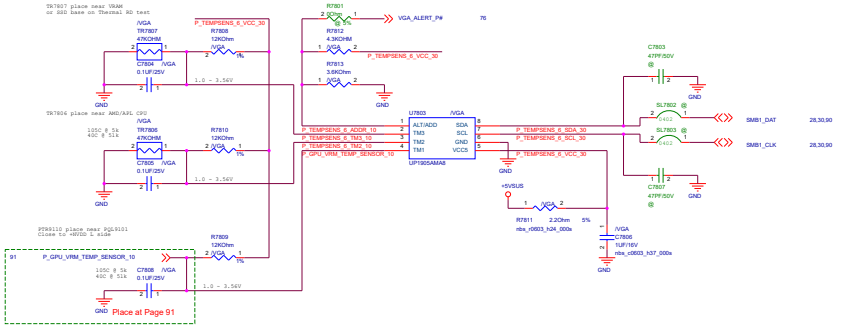


Figure 3-7. Example of Power-Up Sequencing Order

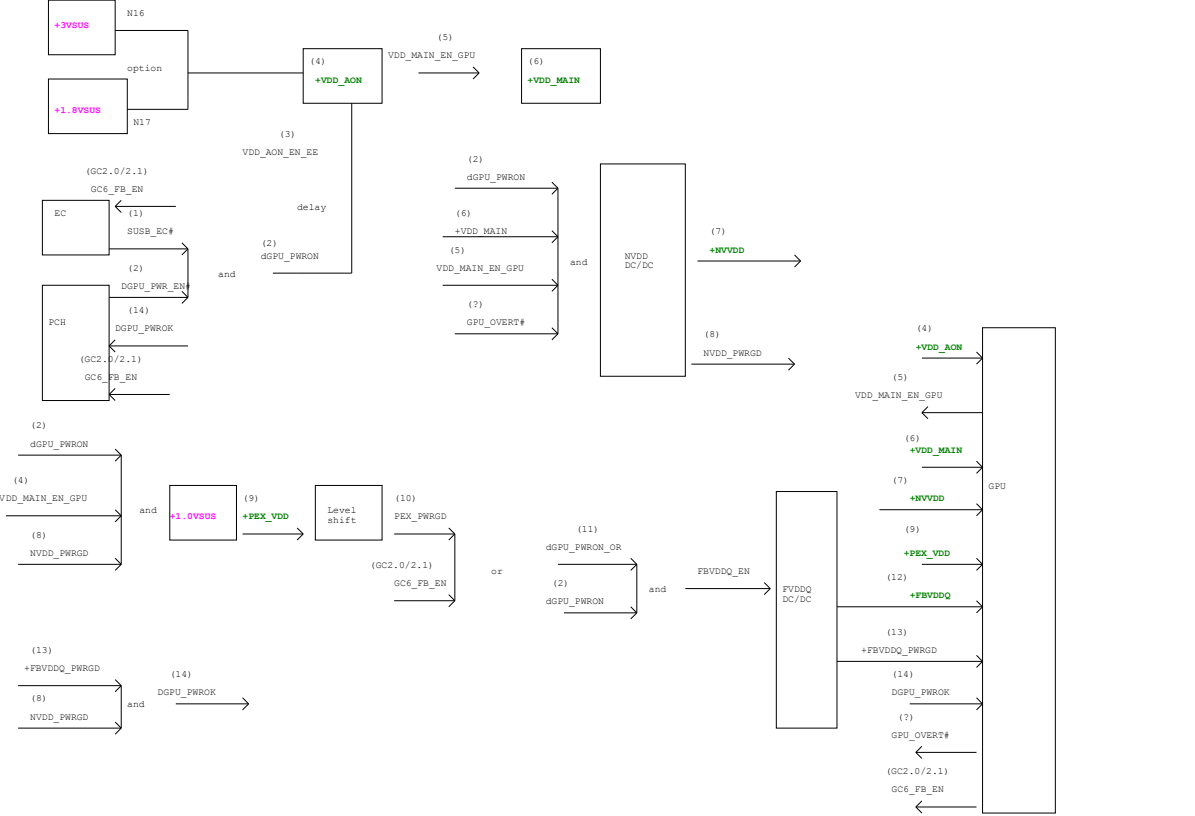
Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R7812	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R7813	Open	6.2k	6.2k	6.8k	6.7k	3.6k	2.7k	2k

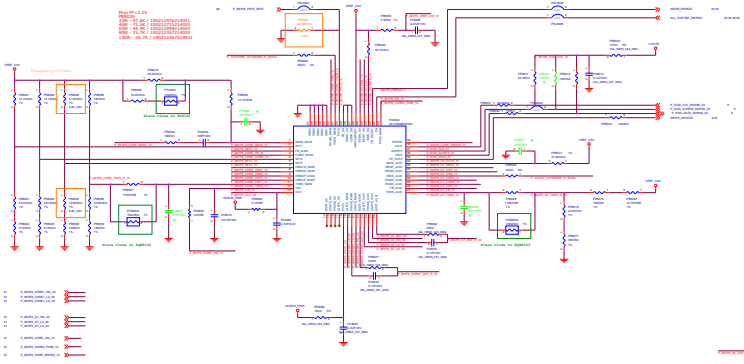


BOM

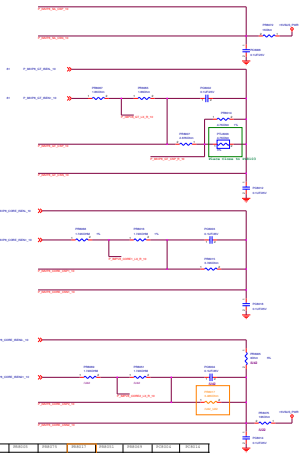
ASUS	Project Name: X430		Rev: R2.0
Title : VGA ****			
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Thursday, August 30, 2018	Sheet: 78	of: 104	



ASUS	Project Name: X430		Rev: REV
Title : VGA ****			
Size: A	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Thursday, August 30, 2018	Sheet 78 of 103		



	U42:	U22:
PR8005:	0 ohm-	@-
PR8075:	@-	10KOhm-
PR8017:	3.48KOHm-	0 ohm-
PR8051:	1.74KOHM-	@-
PR8069:	1.74KOHM-	@-
PC8004:	0.1UF/25V-	@-
PR8053:	32.4KOhm-	24.3KOhm-
PR8006:	31.6KOhm-	18.7KOhm-
PR8035:	19.6KOhm-	11.5kOhm-
PC8014:	N/A-	N/A-

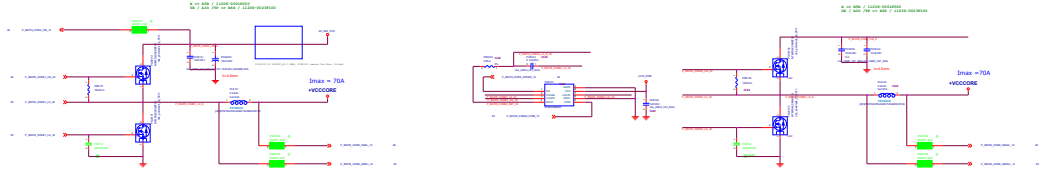


	PR8005	PR8017	PR8051	PR8069	PC8004	PC8014
U42:	Nodraw	0	1.74Kohm	1.74Kohm	0.1UF/25V	0.1UF
U22:	0	3.65Kohm	Nodraw	0	0	0

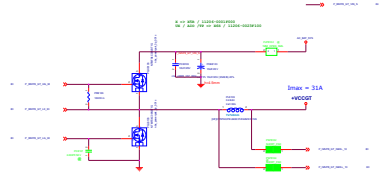
ASUS	Wave Driver		Rev
	X533FN		
Title:	PM_Whisky Lake IMVP8 (3)		
Size:	Document Number:	Rev:	
Date:	Sheet of	Engineer:	Andy

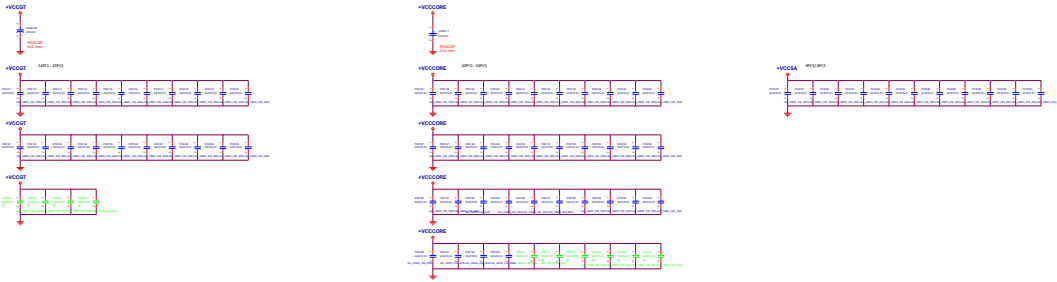
Wishky LAKE IMVP8 Power (2)[For CPU]

+VCCCORE

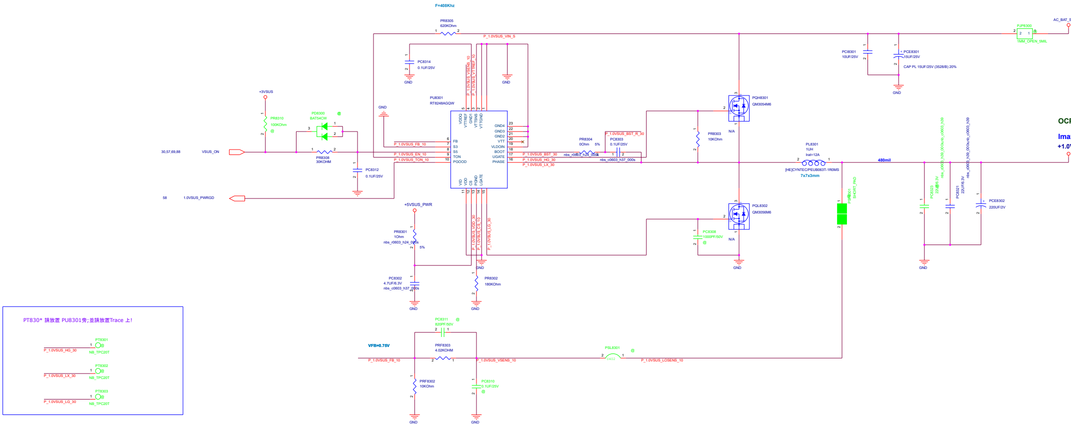


+VCCGT

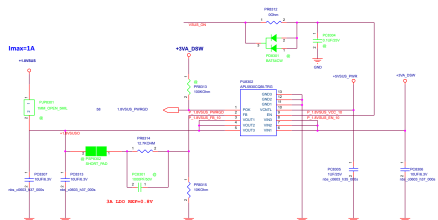




+1.0VSUS [For PCH]



+1.8VSUS [For PCH]



<Core Design>

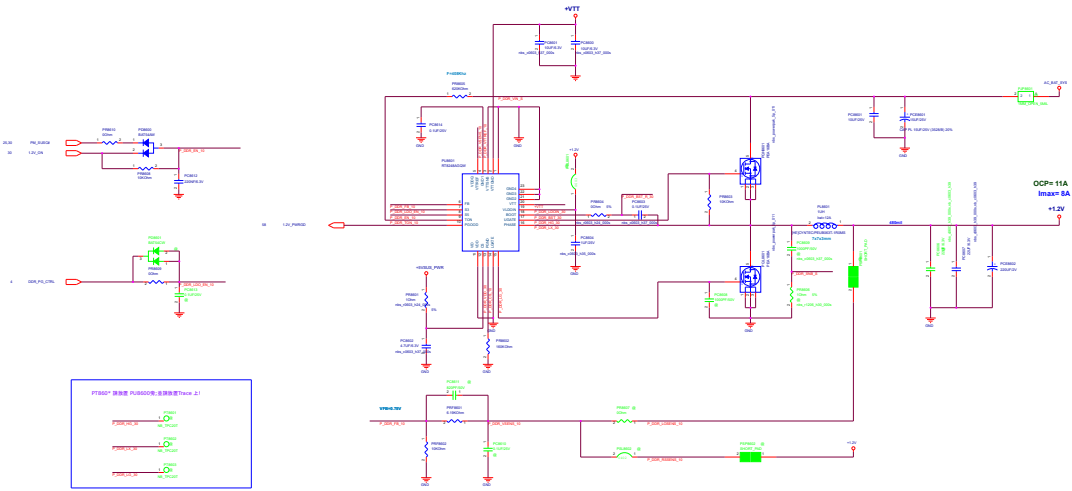
ASUS — Project Name: X530FN — Rev R2.0

Title : PW_+1.0VSUS/+1.8VSUS

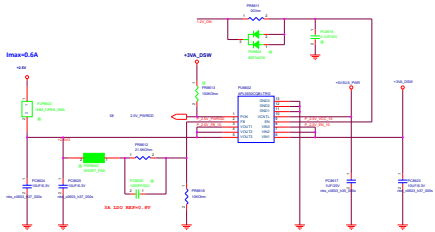
Size A2 — Dept.: Power team — Engineer: Andy

Date: Thursday, August 30, 2018 — Sheet 83 of 104

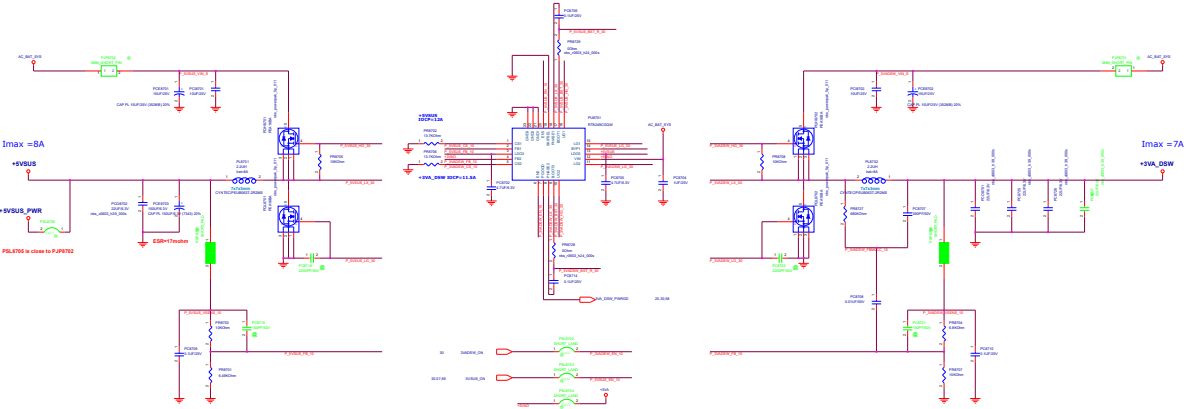
+1.2V / +VTT[For Memory]

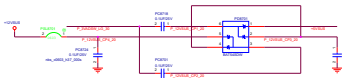


+2.5V[For Memory]



+3VA_DSW / +5VSUS [System Power]



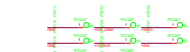


Adaptor Mode (MVP8)

	S0	C0	S3	DS3	S4	S5	S5 with USB Charger
PS_ON	1	-	1	-	1	-	1
5VDSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	0	-	0
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_SCH	1	-	1	-	0	-	0
SUSB_SCH	1	-	0	-	0	-	0

Battery Mode (MVP8)

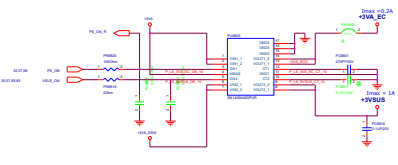
	S0	C0	S3	DS3	S4	S5	S5 with USB Charger
PS_ON	1	-	-	-	1	0	1
5VDSW_ON	1	-	-	-	1	0	0
3VSUS_ON	1	-	-	-	0	0	0
5VSUS_ON	1	-	-	-	1	0	1
1.35V_ON	1	-	-	-	1	0	0
SUSC_SCH	1	-	-	-	0	0	0
SUSB_SCH	1	-	-	-	0	0	0

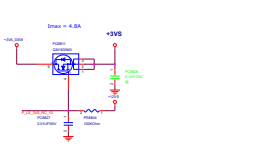


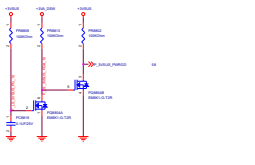
BOM

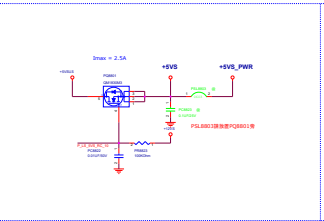
ASUS	Project Name: X530FN	Rev: REV
Title :	PW - +3VA_DSW/+5VSUS	
Size: A3	Dept.: Power team	Engineer: Andy
Date: Thursday, August 30, 2018	Sheet 67 of 103	

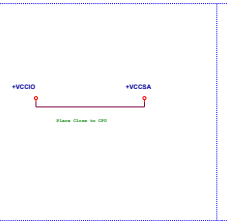
Load Switch

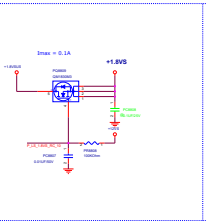


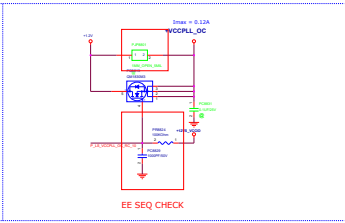


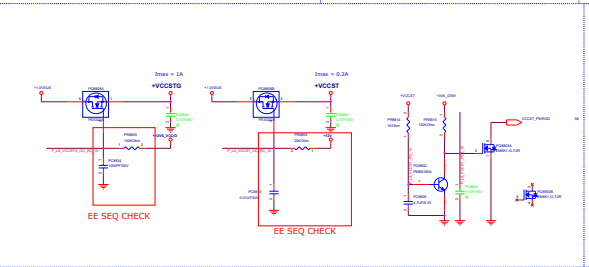


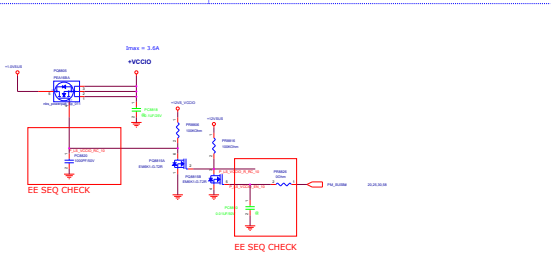


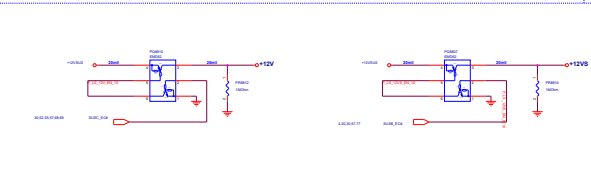


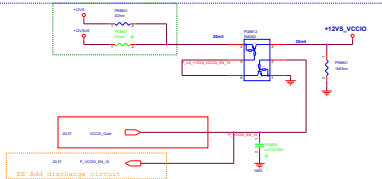




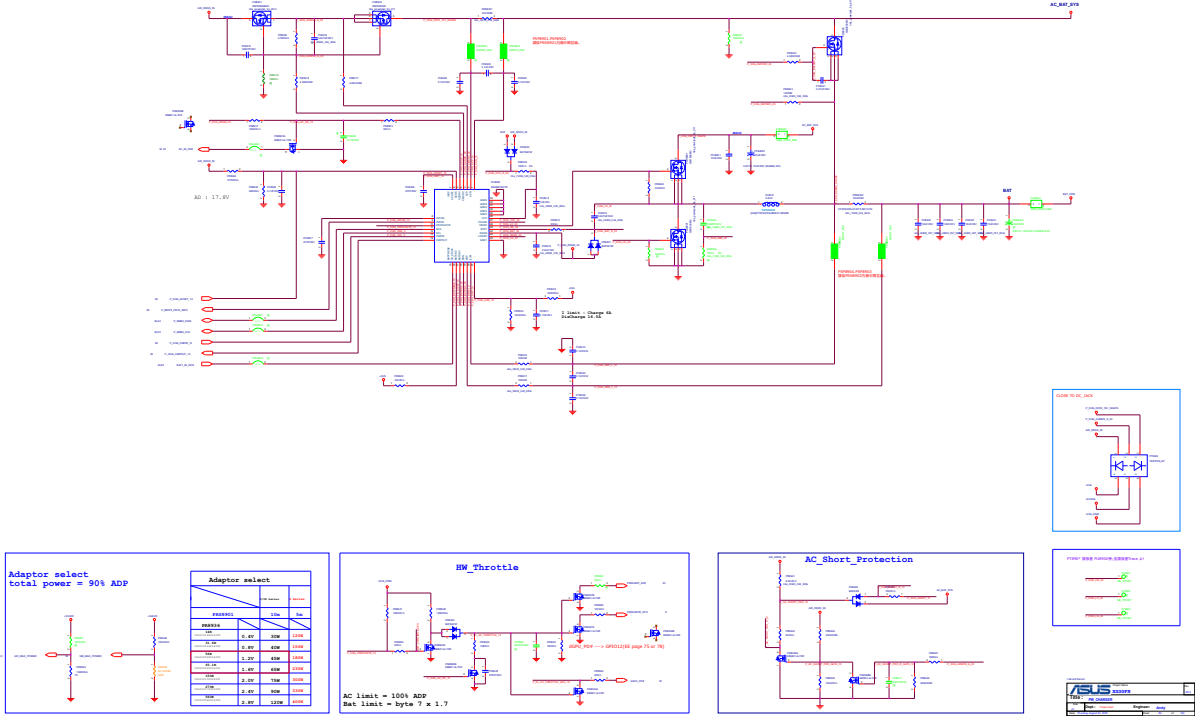








ASUS	Project Name: X530FN		Rev: 0.1
Title :	PW_LOAD_SWITCH		
Size:	Project:	Engineer: Andy	
Date: Thursday, August 08, 2013	Sheet 30 of 100		

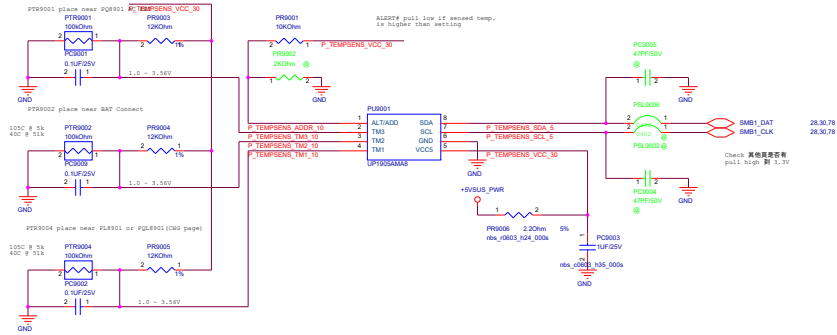

AC_BAT_SYS
AD : 17.6V
BAT
2 limit : Charge 6A
Discharge 15 6A
CLOSE TO DC_JACK
Adaptor select
total power = 90% ADP
Adaptor select
PD85921
15w
5w
PD85924
5W Series
5 Series
AD
0.4V
30W
120W
BI/SW
0.6V
45W
180W
BQ
1.2V
65W
260W
BI/SW
1.4V
85W
340W
PCH
2.4V
75W
300W
PCH
2.4V
90W
360W
BQ
2.9V
120W
480W
HW_Throttle
AC limit = 100% ADP
Bat limit = byte 7 x 1.7
AC_Short_Protection
ASUS
TITLE : MB_DIAGRAM
Size
Engineer
Rev
Date
Sheet
of

Address Selection Table

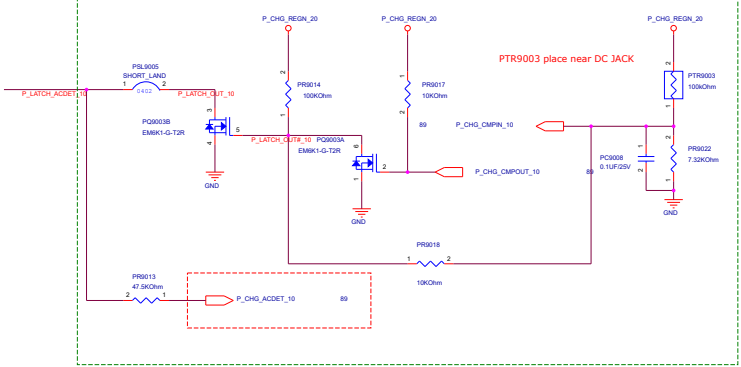
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



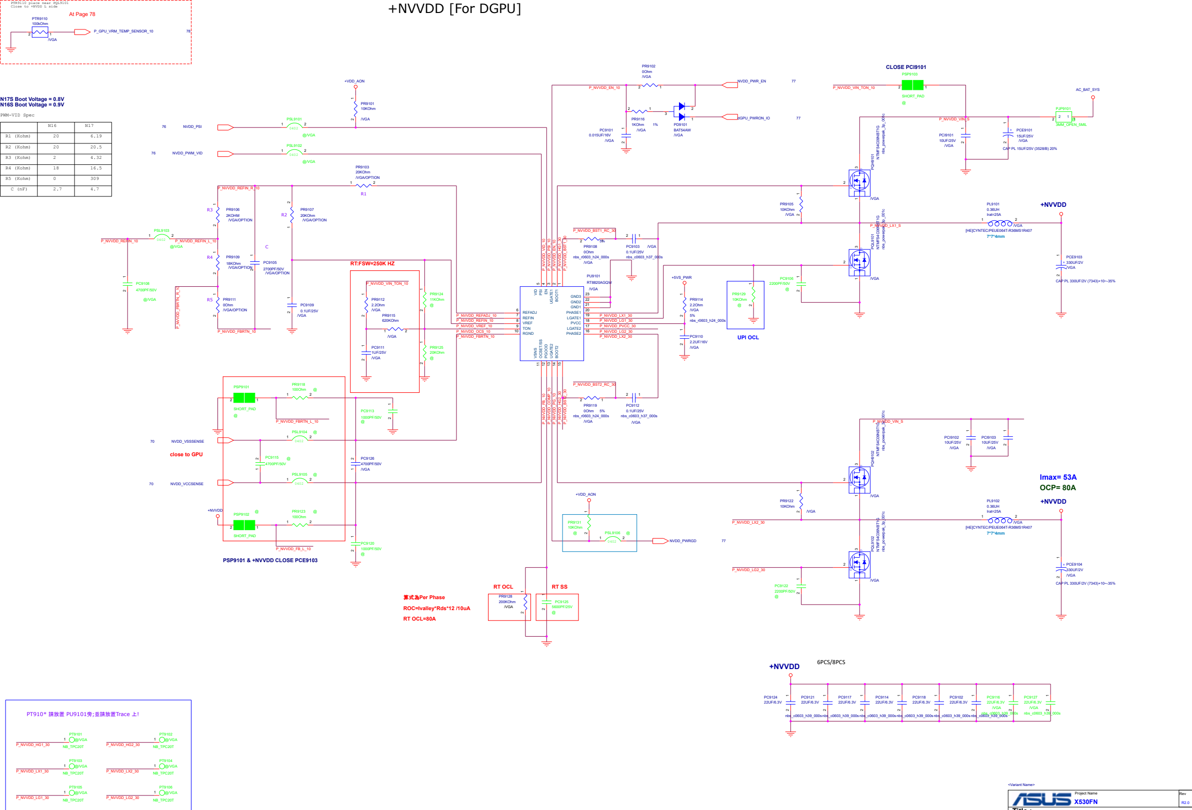
DC Jack Thermal Latch



<Variant Name>

ASUS	Project Name: X530FN		Rev: R2.0
Title : PW_PROTECTION			
Size: A3	Dept.: Power team	Engineer: Andy	
Date: Thursday, August 30, 2018	Sheet: 90 of 104		

+NVVDD [For DGPU]



N17S Boot Voltage = 0.8V
N16S Boot Voltage = 0.9V

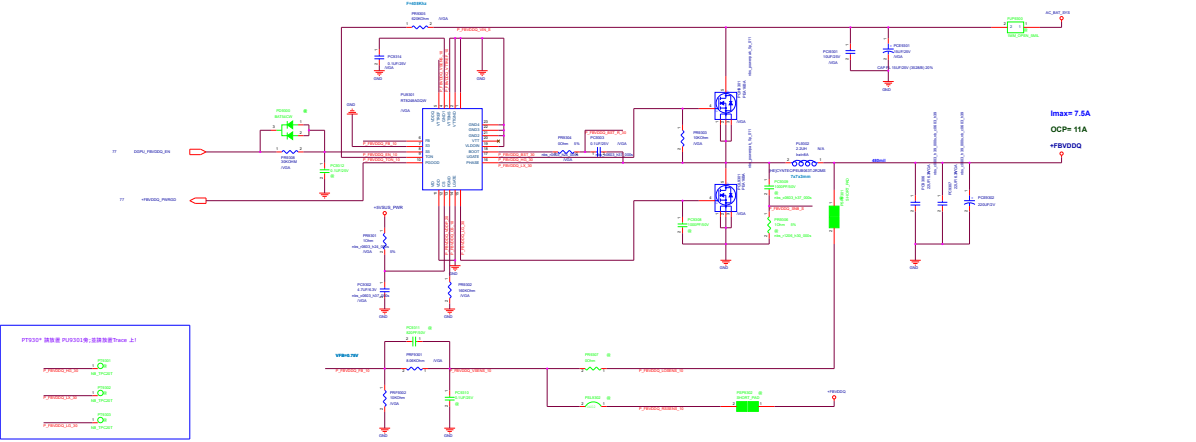
PWM-VID Spec

	N16	N17
R1 (Kohm)	20	6.19
R2 (Kohm)	20	20.5
R3 (Kohm)	2	4.32
R4 (Kohm)	18	16.5
R5 (Kohm)	0	309
C (nF)	2.7	4.7

<Variant Name>

ASUS	Project Name: X530FN	Rev: R2.0
Title : PW_+NVVDD		
Size: A2	Dept.: Power team	Engineer: Andy
Date: Thursday, August 30, 2018	Sheet 91 of 104	

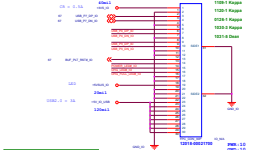
+FBVDDQ [For VRAM]



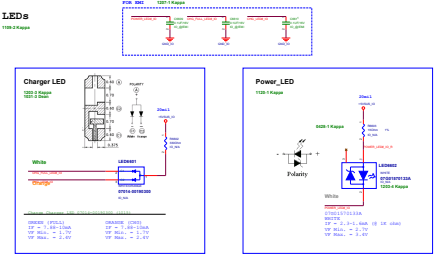
PT930* 調整器 PU9301會;並聯旁路Trace 上1

Project Name: X530FN			Rev: 0.0.0
Title : PW_+FBVDDQ			
Size: A3	Dept.: Power team	Engineer: Andy	
Date: Thursday, August 01, 2019	Sheet: 61	of: 105	

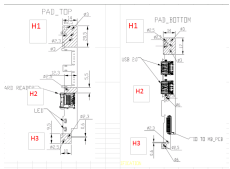
MB to IO CONN (cable同面)



LEDs

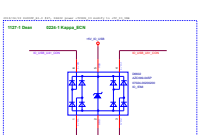


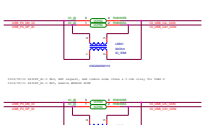
SCREW HOLE

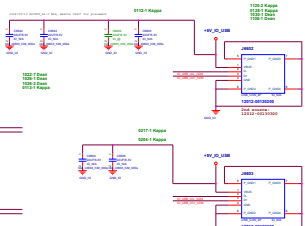


s430_io_pcb_dxf_3_20171120

USB 2.0 Port







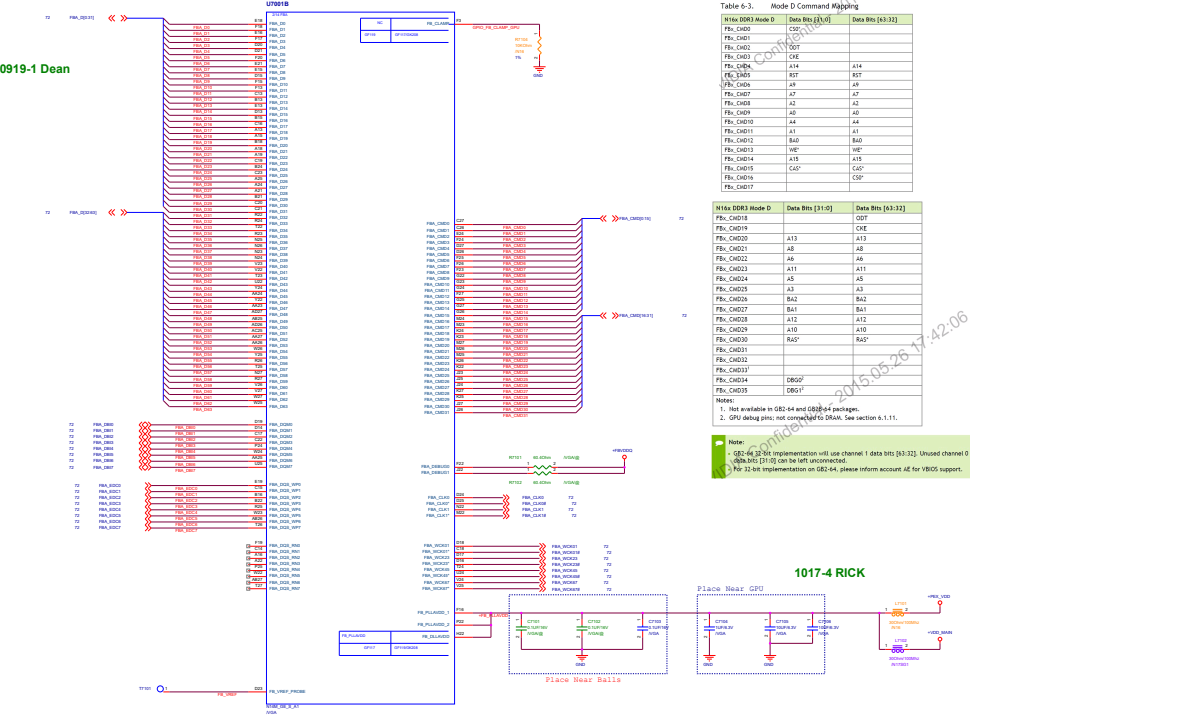


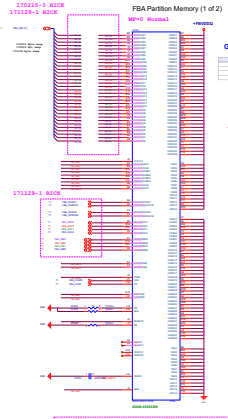
Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1	ODT	
FBx_CMD2	CKE	
FBx_CMD3	A14	A14
FBx_CMD4	RST	RST
FBx_CMD5	A9	A9
FBx_CMD6	A7	A7
FBx_CMD7	A2	A2
FBx_CMD8	A0	A0
FBx_CMD9	A4	A4
FBx_CMD10	A1	A1
FBx_CMD11	BA0	BA0
FBx_CMD12	WE*	WE*
FBx_CMD13	A15	A15
FBx_CMD14	CAS*	CAS*
FBx_CMD15	CS1*	CS0*
FBx_CMD16		CS1*
FBx_CMD17		

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBGO[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2-64 and GB2-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

Note:
- GB2-64 32-bit implementation will use channel 1 data bits [63:32]. Unused channel 0 data bits [31:0] can be left unconnected.
- For 32-bit implementation on GB2-64, please inform account AE for VBIOS support.



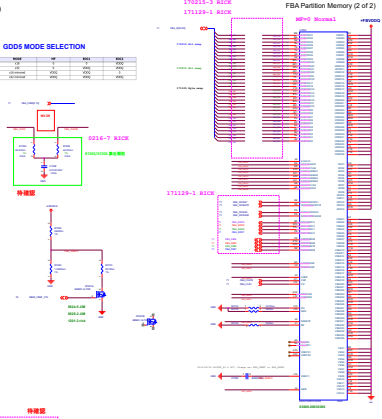


Table 9.8 GDDR5 x32 vs. x16 Dual Bus Connectivity

GPU Signal (for FB Partition n)	x32 Mode (Non-Clamshell)		x16 Mode (Clamshell)	
	GDDR5 SDRAM Device	Data Lines	GDDR5 SDRAM Device	Data Lines
FBn_A<x>, FBn_A<x>	Top Device (typically active-mirrored pinout, top of PCB)	DQ[7:0]A	Hi-Z (Non-Active Device, bottom of PCB)	DQ[7:0]Z
FBn_A<x>, FBn_A<x>		DQ[15:8]A	Hi-Z (Non-Active Device, bottom of PCB)	DQ[15:8]Z
FBn_A<x>, FBn_A<x>		DQ[23:16]A	Hi-Z (Non-Active Device, bottom of PCB)	DQ[23:16]Z
FBn_A<x>, FBn_A<x>		DQ[31:24]A	Hi-Z (Non-Active Device, bottom of PCB)	DQ[31:24]Z
FBn_EDC[3:0]		DQ[7:0]B	Hi-Z (Non-Active Device, top of PCB)	DQ[7:0]B
FBn_EDC[7:4]		DQ[15:8]B	Hi-Z (Non-Active Device, top of PCB)	DQ[15:8]B
FBn_EDC[11:8]		DQ[23:16]B	Hi-Z (Non-Active Device, top of PCB)	DQ[23:16]B
FBn_EDC[15:12]		DQ[31:24]B	Hi-Z (Non-Active Device, top of PCB)	DQ[31:24]B

Table 9.8 GDDR5 x32 vs. x16 Data Bus Connectivity (Continued)

GPU Signal (for FB Partition n)	x32 Mode (Non-Clamshell)		x16 Mode (Clamshell)	
	GDDR5 SDRAM Device	Data Lines	GDDR5 SDRAM Device	Data Lines
FBn_A<2>n, FBn_A<2>n	Low Device (typically active-mirrored pinout, top of PCB)	DQ[7:0]A	Low-Chicken Device (mirrored pinout, bottom of PCB)	DQ[7:0]A
FBn_A<2>n, FBn_A<2>n		DQ[15:8]A	Low-Chicken Device (mirrored pinout, top of PCB)	DQ[15:8]A
FBn_A<2>n, FBn_A<2>n		DQ[23:16]A	Low-Chicken Device (mirrored pinout, bottom of PCB)	DQ[23:16]A
FBn_A<2>n, FBn_A<2>n		DQ[31:24]A	Low-Chicken Device (mirrored pinout, top of PCB)	DQ[31:24]A
FBn_EDC[3:0]		DQ[7:0]B	Low-Chicken Device (mirrored pinout, top of PCB)	DQ[7:0]B
FBn_EDC[7:4]		DQ[15:8]B	Low-Chicken Device (mirrored pinout, bottom of PCB)	DQ[15:8]B
FBn_EDC[11:8]		DQ[23:16]B	Low-Chicken Device (mirrored pinout, top of PCB)	DQ[23:16]B
FBn_EDC[15:12]		DQ[31:24]B	Low-Chicken Device (mirrored pinout, bottom of PCB)	DQ[31:24]B

Table 9.18 GPU-Side FBVDDQ Decoupling Requirements

Decoupling Capacitor		Recommended Quantity and Placement (for all supported partitions combined)	
Capacitance	Type Size	Quantity	Placement
For H/Tx GPU Package: GB2C-64 (preliminary)			
1.0 uF	0402 [1005]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
10 uF	805 [2603]	1	Near GPU Device
10 uF	805 [2603]	1	Near GPU Device
22 uF	805 [2603]	1	

Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitor		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (to DRAM/Near Race Node)
Combined FBVDD/FBVDDQ Rail			
1.0 uF	X6S [0402]	8	For x32 DRAM, locate the DRAM FBVDD or FBVDDQ balls.
10 uF	X6S [0603]	4	For x16 DRAM in a "clamshell" mode configuration, locate the DRAM FBVDD or FBVDDQ balls.
			Group the two 2.2nF vias and 1 power via for each decoupling capacitor.
1.0 uF	X6S [0402]	4 additional	For x16 DRAM, choose one interface to achieve two PDR DRAM pads. Add these four additional capacitors to the existing FBVDD/Q rail; should share existing FBVDD/Q rail via if possible. See Figure 9.23 for an example.
			Near DRAM device, ensure at least 2 GHB vias and 2 power vias for each capacitor.
10 uF	X6S [0603]	2	For x16/x32 DRAM, locate the DRAM FBVDD or FBVDDQ balls.
			Near DRAM device, ensure at least 2 GHB vias and 2 power vias for each capacitor.
22 uF	X6S [0603]	1	

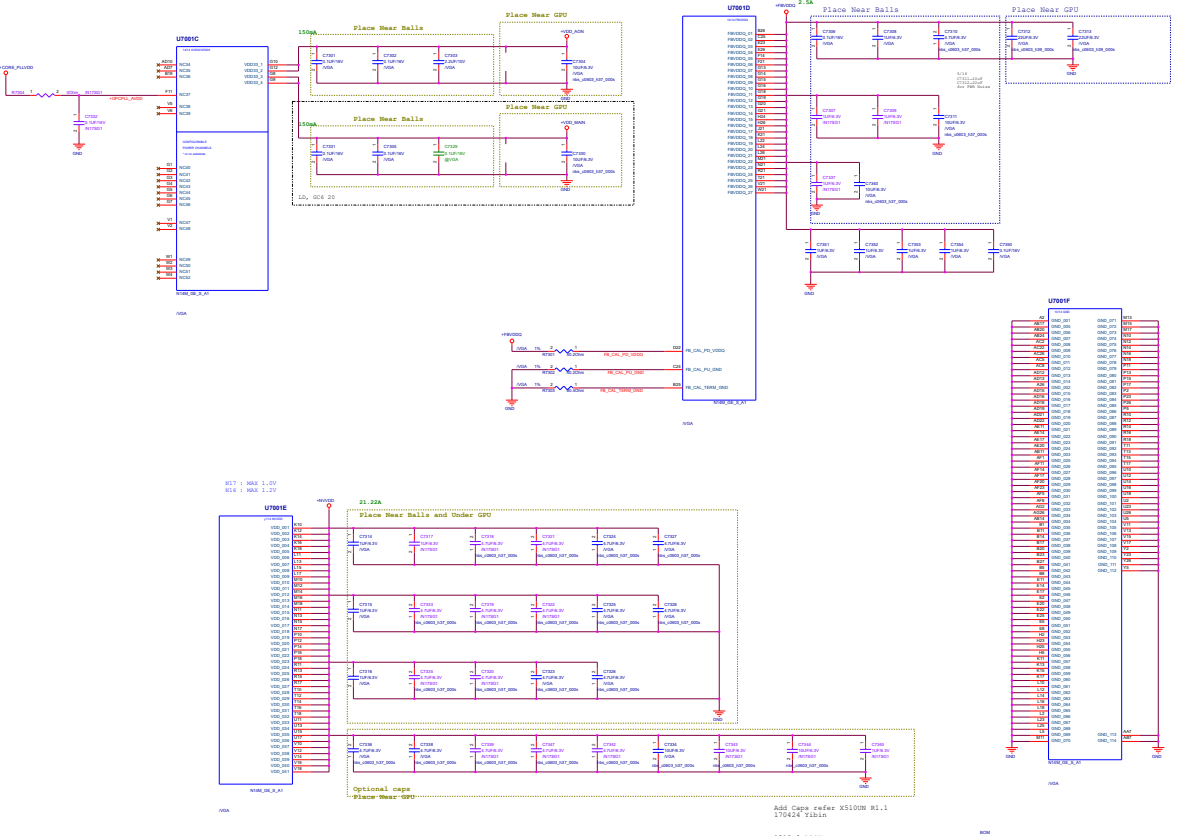

U7001C
U7001D
U7001F
U7001E
Place Near Balls
Place Near GPU
Place Near Balls and Under GPU
Optional caps
Place Near GPU
150uA
21.22A
2.5A
+VGPU_AON
+VGPU_MAIN
+VGPUSDQ
+VNVDD
+VFBVDDQ
+VGPU_PCI_VDDIO
+VGPU_FU_GND
+VGPU_TERM_GND
+CORE_FU_VDD
+GPCPLL_AVDD
LD, QC6 20
N17 : MAX 1.0V
N16 : MAX 1.2V
Add Caps refer X510UN R1.1
170424 Yibin
1219-2 Rick
ASUS
X430
VGA_nVIDIA_N16N17S_VDD
ASUSTeK COMPUTER INC.
Engineer:
EE
Thursday, August 20, 2015
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Table 4. N17S-G1 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production ready
			Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production ready
			Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production ready
			Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x4	7 Gbps	N/A	Full	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x4	8 Gbps	N/A	N/A	Substitution allowed with waiver[2]

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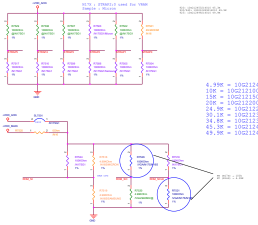
Table 11. N17/GB2C-64 Ternary Strapping

Strap Pin	N17S-G1, GDDR5 SAMSUNG(256Mx32) K4G80325FB-HC28 03008-00050000	MICRON(256Mx32) MT51J256M32HF-70:B 03008-00051700	HYMIX(256Mx32) H5GC8H24MJR-R0C	N16S-GTR, GDDR5
STRAP0	L: R7504 = 100Kohm	L: R7504 = 100Kohm	L: R7504 = 100Kohm	R7501 = 49.9Kohm, R7504=>@
STRAP1	L: R7505 = 100Kohm	L: R7505 = 100Kohm	H: R7502 = 100Kohm	Do not stuff
STRAP2	L: R7506 = 100Kohm	H: R7503 = 100Kohm	L: R7506 = 100Kohm	Do not stuff
STRAP3		L: R7509 = 100Kohm		Do not stuff
STRAP4		L: R7510 = 100Kohm		Do not stuff
STRAP5		L: R7517 = 100Kohm		Do not stuff
ROM_SCLK		M: R7521,R7518 = 100Kohm		R7521 = 4.99Kohm, R7518=>@
ROM_SI		H: R7524 = 100Kohm		see N16 VRAM table.
ROM_SO		H: R7526 = 100Kohm		R7520 = @, R7526=>4.99Kohm

2018/05/11 X430FF_R1.0 #A4, Update VRAM strap optional & remove R7530

N17S-G1

P/N	Type/Config	VRAM	RAM_CFG	Strap0	Strap1	Strap2
03008-00051700	GDDR5 256M*32 6.0 1.5V FBGA170	MICRON/MT51J256M32HF-70:B	0x4	L	L	H
03008-00050000		SAMSUNG/K4G80325FB-HC28	0x0	L	L	L



4.99K = 10G212499114010
10K = 10G212100214010
15K = 10G212150214030
20K = 10G212200214030
24.9K = 10G212249214010
30.1K = 10G212301214010
34.8K = 10G212348214010
45.3K = 10G212453214010
49.9K = 10G212499214010

GDDR5 VRAM (單位用量 *2pcs)			
2G(256*32)	03008-00050000	GDDR5 256M*32 7.0 1.5V FBGA170	//SAMSUNG/K4G80325FB-HC28
	~~03008-00050400~~	GDDR5 256M*32 7.0 1.5V FBGA170	~~//MICRON/MT51J256M32HF-70:A~~
	03008-00051700		MICRON/MT51J256M32HF-70:B

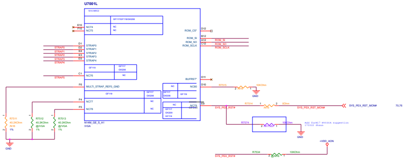
256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
	Samsung	K4G80325FB-HC28	B-die	0x0	3000	N/A	Substitution allowed with waiver[2]

N16S-GTR

P/N	Type/Config	VRAM	RAM_CFG	SI
03008-00051700	GDDR5 256M*32 6.0 1.5V FBGA170	MICRON/MT51J256M32HF-70:B	0x8	PU 4.99K
03008-00050000		SAMSUNG/K4G80325FB-HC28	0x0	PD 4.99K

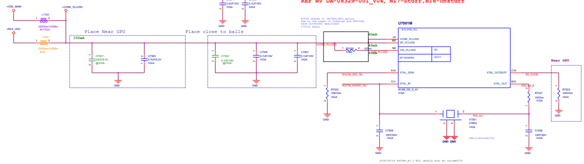
NVIDIA CONFIDENTIAL
N16x Memory RVL RVL-07229-001_v26 | 16

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
			Samsung	K4G80325FB-HC25	B-die	0x0	3250	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production ready
			Hynix	H5GC8H24MJR-R0C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Hynix	H5GQ8H24MJR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
			Micron	MT51J256M32HF-70:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-80:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x8	3000	N/A	Post production ready



Xtal

R7556 N17/N16都要上!!, 還需留0ohm ?!
REF NV DA-08329-001_V04, N17-Stuff,N16-Unstuff



Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_ EXPOSED	SOR2_ EXPOSED	SOR1_ EXPOSED	SOR0_ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

Project Name X430
Title : VGA_nVIDIA_N16/N17S_XTAL
Dept.: ASUSTeK COMPUTER INC. Engineer: EE
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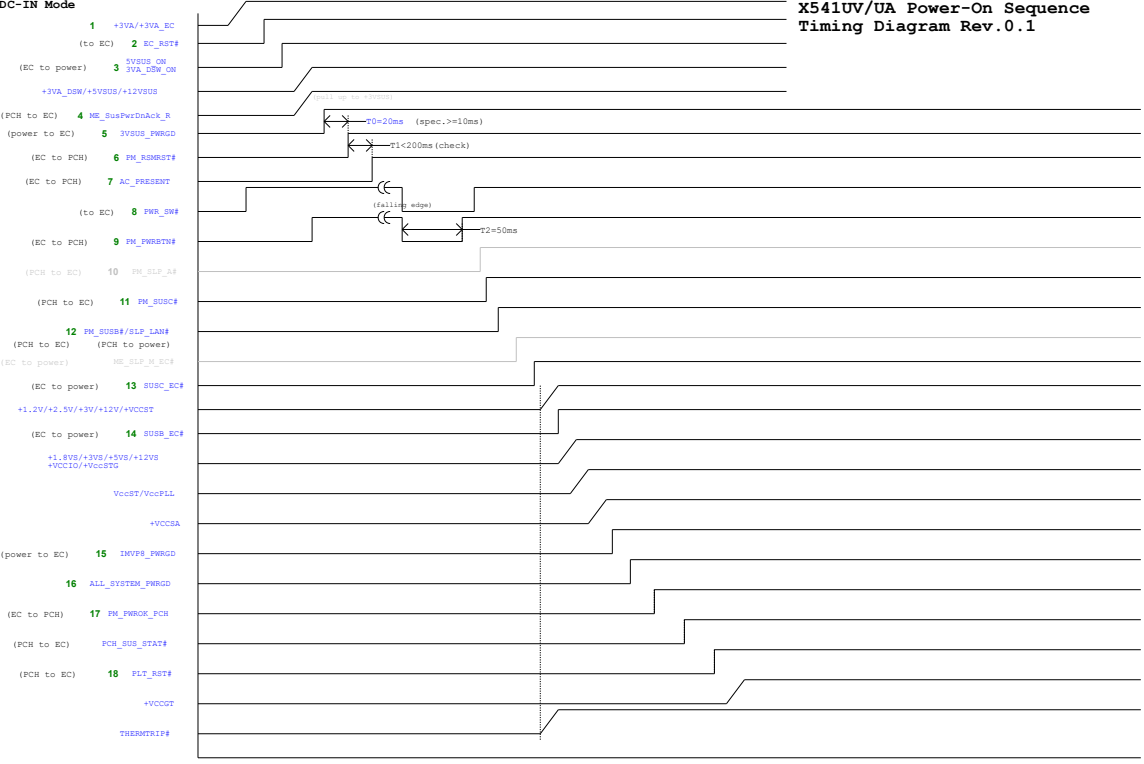
DC-IN Mode

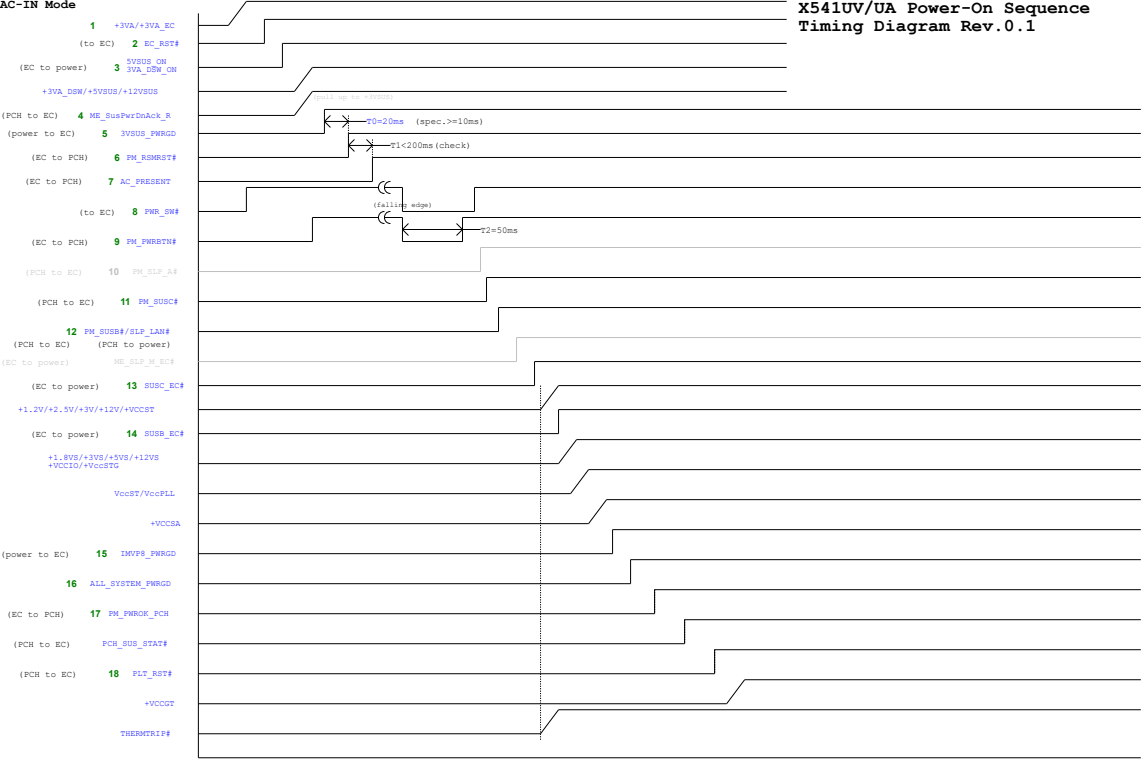
X541UV/UA Power-On Sequence Timing Diagram Rev.0.1



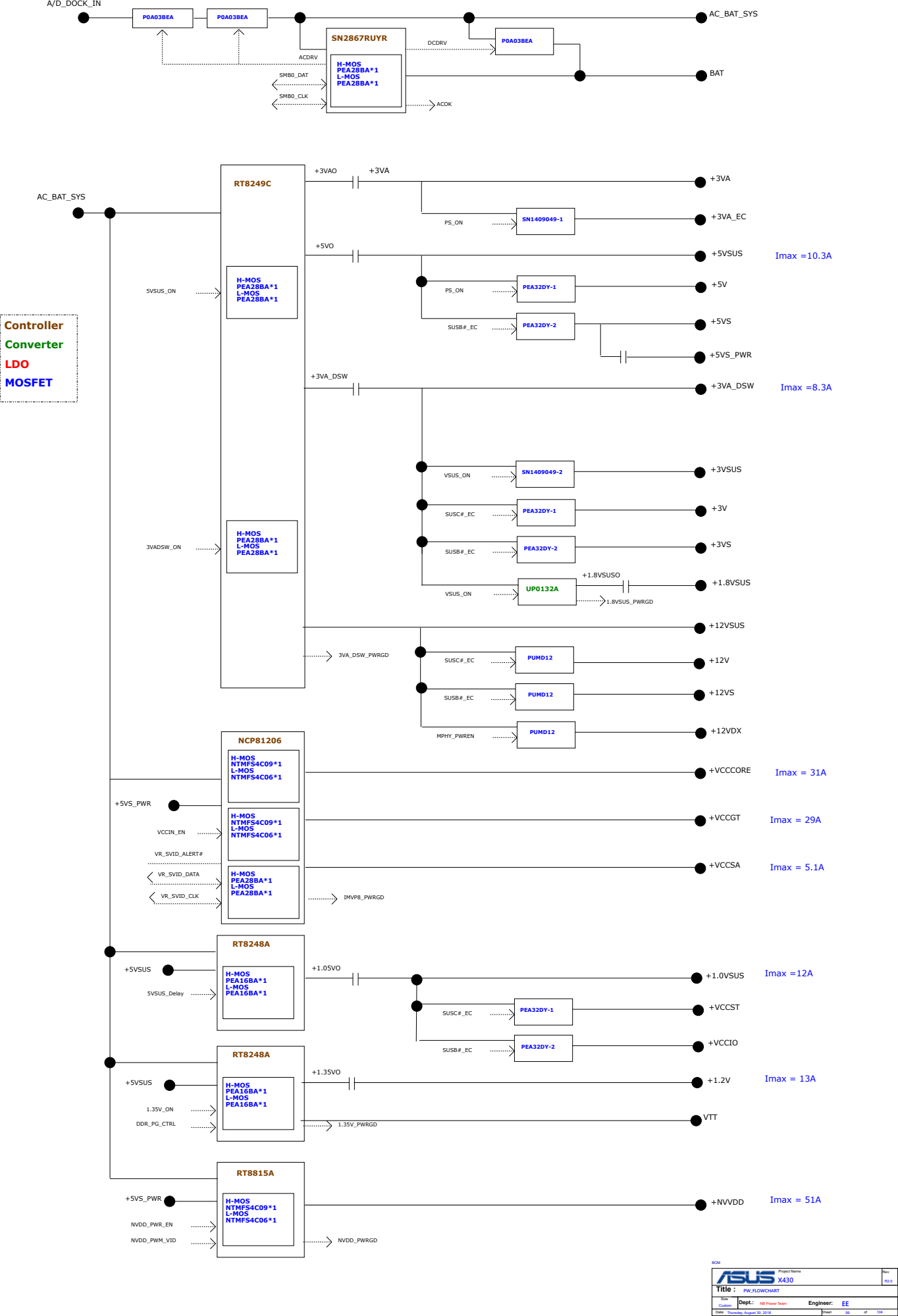
Project Name: X430			Rev: 90.0
Title: Power On Timing			
Size:	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Thursday, August 30, 2018	Sheet: 101	of: 104	

X541UV/UA Power-On Sequence Timing Diagram Rev.0.1

AC-IN Mode



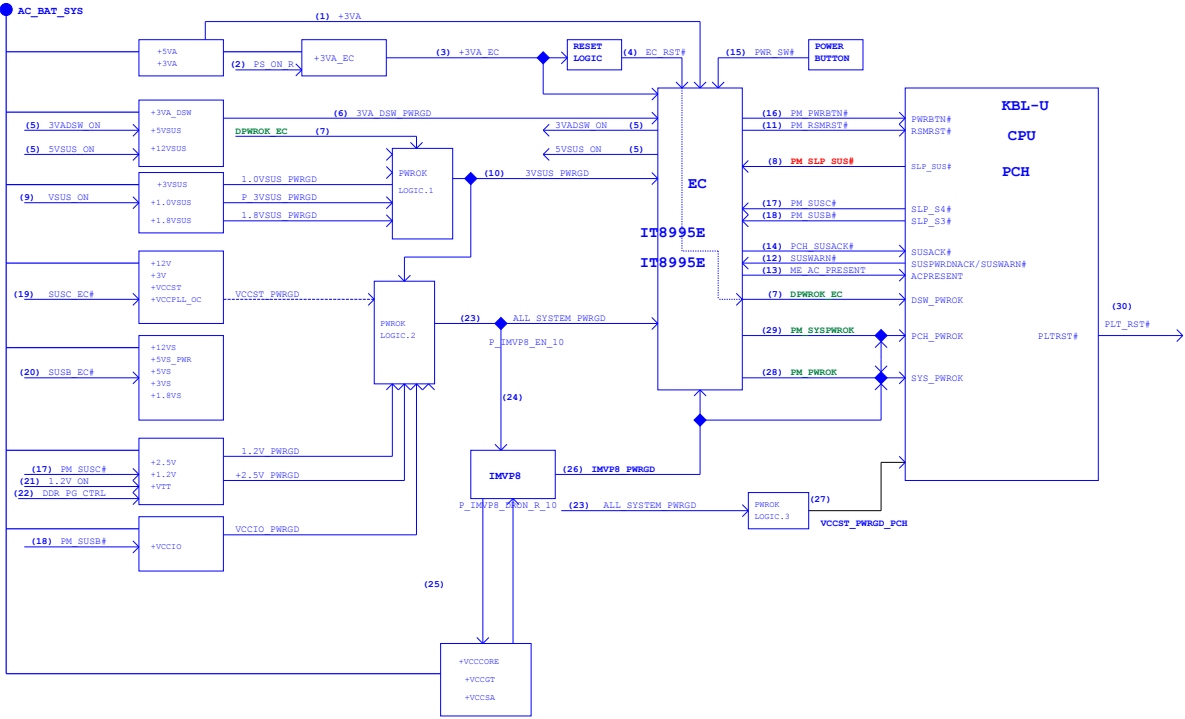
Project Name: X430			Rev: 82.0
Title: Power On Timing			
Size:	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Thursday, August 30, 2018	Sheet: 100 of 104		


A/D_DOCK_IN
P0A03BEA
P0A03BEA
AC_BAT_SYS
SN2867RUYR
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
ACDRV
DCDRV
P0A03BEA
BAT
SMB0_DAT
SMB0_CLK
ACOK
AC_BAT_SYS
RT8249C
+3VAO
+3VA
+3VA
+3VA_EC
PS_ON
SN1409049-1
+5VO
+5VSUS
Imax =10.3A
5VSUS_ON
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
PS_ON
PEA32DY-1
+5V
SUSB#_EC
PEA32DY-2
+5VS
+5VS_PWR
Controller
Converter
LDO
MOSFET
+3VA_DSW
+3VA_DSW
Imax =8.3A
VSUS_ON
SN1409049-2
+3VSUS
SUSC#_EC
PEA32DY-1
+3V
3VADSW_ON
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
SUSB#_EC
PEA32DY-2
+3VS
+1.8VSUSO
VSUS_ON
UP0132A
+1.8VSUS
1.8VSUS_PWRGD
+12VSUS
3VA_DSW_PWRGD
SUSC#_EC
PUMD12
+12V
SUSB#_EC
PUMD12
+12VS
MPHY_PWREN
PUMD12
+12VDX
NCP81206
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
+VCCCORE
Imax = 31A
+5VS_PWR
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
+VCCGT
Imax = 29A
VCCIN_EN
VR_SVID_ALERT#
H-MOS
PEA28BA*1
L-MOS
PEA28BA*1
+VCCSA
Imax = 5.1A
VR_SVID_DATA
VR_SVID_CLK
IMVP8_PWRGD
RT8248A
+5VSUS
H-MOS
PEA16BA*1
L-MOS
PEA16BA*1
+1.05VO
+1.0VSUS
Imax =12A
5VSUS_Delay
SUSC#_EC
PEA32DY-1
+VCCST
SUSB#_EC
PEA32DY-2
+VCCIO
RT8248A
+5VSUS
H-MOS
PEA16BA*1
L-MOS
PEA16BA*1
+1.35VO
+1.2V
Imax = 13A
1.35V_ON
DDR_PG_CTRL
1.35V_PWRGD
VTT
RT8815A
+5VS_PWR
H-MOS
NTMFS4C09*1
L-MOS
NTMFS4C06*1
+NVVDD
Imax = 51A
NVDD_PWR_EN
NVDD_PWM_VID
NVDD_PWRGD
BOM
Project Name
X430
Rev
R2.0
Title :
PW_FLOWCHART
Size
Custom
Dept.:
NB Power Team
Engineer:
EE
Date:
Thursday, August 30, 2018
Sheet
99
of
104

+RTCBAT->3.3V
RTCCLK->on
RTC_RST->High

AC-IN Mode
AC_IN_OC->Low

X550VD Power On Sequence Diagram Rev.1.0



Title :	POWER SEQUENCE
Engineer:	EE
Project Name	X430
Rev	REV
Date	Thursday, August 30, 2018
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PCH_CPT GPIO

SYS_PWROK GPIO	Use As	Signal Name	Powermap Control Options	3V/S Out Default Value	Power
GPP_A0	Native1	RCIN#		3V/S PP 20K	
GPP_A1	Native1	LAD_0#/FWH_0			+3VS
GPP_A2	Native1	LAD_1#/FWH_1			
GPP_A3	Native1	LAD_2#/FWH_2			
GPP_A4	Native1	LAD_3#/FWH_3			
GPP_A5	Native1	LFRAME#/FWH_4		3V/S PD 20K	
GPP_A6	Native1	SERIRQ		3V/S PU 8.2K	+3VS
GPP_A7	GPO	N/A			
GPP_A8	Native	PM_CLKRUN#		3V/S PU 8.2K	+3VS
GPP_A9	Native1	PLT_RST1#/I_RST#			
GPP_A10	Native1	CLK_PCI#/I_GPIO		3V/S PD 20K	+3VS
GPP_A11	GPO	N/A	無線藍芽開關 Enable 功能		
GPP_A12	GPO	N/A			
GPP_A13	Native1	SUSWARN#		3V/S PU 20K	+3VSUS
GPP_A14	Native1	SUS_STAT#/I_GPIO			
GPP_A15	Native1	PCH_SUSACK#			
GPP_A16	GPO	N/A, USB_OC6 (EC)			
GPP_A17	GPO	N/A, USB_OC5 (EC)			
GPP_A18	GPO	N/A			
GPP_A19	GPO	N/A			
GPP_A20	GPO	N/A			
GPP_A21	GPO	N/A			
GPP_A22	GPO	N/A			
GPP_A23	GPO	N/A			
GPP_B0	Native	N/A (VGCISCLK_C232)		3V/S PD 20K	+3VS
GPP_B1	Native	N/A (VGCISDLK_C232)		3V/S PD 20K	+3VS
GPP_B2	GPO	N/A			
GPP_B3	GPO	N/A			
GPP_B4	GPO	N/A			
GPP_B5	Native	CK_REQ_P1#	GLAN	3V/S PU 20K	+3VS
GPP_B6	Native	CK_REQ_P2#		3V/S PU 20K	+3VS
GPP_B7	Native	CK_REQ_P3#		3V/S PU 20K	+3VS
GPP_B8	Native	CK_REQ_P4#	CLAN1	3V/S PU 20K	+3VS
GPP_B9	Native	CK_REQ_P5#	WLAN	3V/S PU 20K	+3VS
GPP_B10	Native	WAKE_PEG#/I_GPIO		3V/S PU 20K	+3VS
GPP_B11	Native	PLT_RST2#			
GPP_B12	GPO	N/A (PWROK)			
GPP_B13	GPO	N/A (SUSPC_CK_PM)			
GPP_B14	GPO	N/A (SUSPC_CK_PM)			
GPP_B15	GPO	N/A (SUSPC_WLED_N)			
GPP_B16	Native	SPI_CLK#/I_GPIO			
GPP_B17	GPO	MC_CS1/SPI#			
GPP_B18	GPO	LPC_SERIRQ#		3V/S PU 20K	+3VS
GPP_B19	GPO	MC_CS0/SPI#			
GPP_B20	GPO	LPC_SERIRQ#		3V/S PU 20K	+3VS
GPP_B21	GPO	MISO/M_CK_CLAMP_GPIO			PU at SUSPC
GPP_B22	GPO	MOSI/SPI#			
GPP_B23	Native	SML1ALERT#		3V/S PU 100K	+3VSUS
GPP_C0	Native	SMB_CLK		3V/S PU 2.2K	+3VSUS
GPP_C1	Native	SMB_DATA		3V/S PU 2.2K	+3VSUS
GPP_C2	GPO	SMB_LK2			
GPP_C3	Native	SMB_DA2		3V/S PU 2.2K	+3VSUS
GPP_C4	Native	SMB_CLK2		3V/S PU 2.2K	+3VSUS
GPP_C5	Native	SMB_DATA2		3V/S PU 2.2K	+3VSUS
GPP_C6	GPO	N/A (PCH_OPI#)			
GPP_C7	GPO	N/A (PCH_OPI#)			
GPP_C8	GPO	N/A (PCH_OPI#)			
GPP_C9	GPO	N/A (PCH_OPI#)			
GPP_C10	SPI	SPI_CS1#		3V/S PU 20K	+3VS
GPP_C11	GPO	SPI_MISO		3V/S PU 20K	+3VS
GPP_C12	SPI	SPI_MOSI	SMB01_SMB	3V/S PU 20K	+3VS
GPP_C13	SPI	SPI_CLK	SMB01_CTRL	3V/S PU 20K	+3VS
GPP_C14	GPO	SMB_ALERT#/GPIO			
GPP_C15	GPO	N/A (SLP_SUS#)			
GPP_C16	Native	N/A			
GPP_C17	Native	N/A			
GPP_C18	GPO	LPC_AD0#		3V/S PU 20K	+3VS
GPP_C19	GPO	LPC_AD1#		3V/S PU 20K	+3VS
GPP_C20	GPO	LPC_AD2#		3V/S PU 20K	+3VS
GPP_C21	GPO	LPC_AD3#		3V/S PU 20K	+3VS
GPP_C22	GPO	LPC_CLK0			
GPP_C23	GPO	LPC_CLK1			

SYS_PWROK GPIO	Use As	Signal Name	Powermap Control Options	3V/S Out Default Value	Power
GPP_D23	GPO	N/A			
GPP_D0	GPO	N/A(SPI_PWROK_GPIO#)			
GPP_D1	GPO	SATA_DEVSLP_0#		3V/S PU 20K	
GPP_D2	GPO	SATA_DEVSLP_1#		3V/S PU 20K	
GPP_D3	GPO	N/A			
GPP_D4	GPO	SATA0_GP[0]#			
GPP_D5	GPO	SATA1_GP[0]#/SMB01			
GPP_D6	GPO	SATA2_GP[0]#			
GPP_D7	GPO	N/A			
GPP_D8	Native	LAN_WAKE#		3V/S PU 20K	+3VS
GPP_D9	Native	SLP_WLAN#		3V/S PU 20K	+3VS
GPP_D10	Native	SLP_S4#		3V/S PU 20K	+3VS
GPP_D11	Native	SLP_S3#		3V/S PU 20K	+3VS
GPP_D12	GPO	N/A			
GPP_D13	GPO	N/A			
GPP_D14	GPO	N/A			
GPP_D15	GPO	N/A			
GPP_D16	GPO	N/A			
GPP_D17	GPO	N/A			
GPP_D18	GPO	N/A			
GPP_D19	GPO	N/A			
GPP_D20	GPO	N/A			
GPP_D21	GPO	N/A			
GPP_D22	GPO	N/A			
GPP_E0	GPO	SATA_ACT#/GPIO			
GPP_E1	GPO	SATA_LED#/GPIO			
GPP_E2	GPO	N/A (GPIO)			
GPP_E3	GPO	N/A (GPIO)			
GPP_E4	GPO	N/A (GPIO)			
GPP_E5	GPO	N/A (GPIO)			
GPP_E6	GPO	N/A (GPIO)			
GPP_E7	GPO	N/A (GPIO)			
GPP_E8	Native	LAN_PHY_PWR_CTRL		3V/S PU 8.2K	+3VS, GLAN
GPP_E9	Native	USB_OC1#		3V/S PU 20K	+3VS, USB
GPP_E10	Native	USB_OC2#		3V/S PU 20K	+3VS, USB
GPP_E11	Native	USB_OC3#		3V/S PU 20K	+3VS, USB
GPP_E12	Native	USB_OC4#		3V/S PU 20K	+3VS, USB
GPP_E13	Native	USB_OC5#		3V/S PU 20K	+3VS, USB
GPP_E14	Native	USB_OC6#		3V/S PU 20K	+3VS, USB
GPP_E15	GPO	N/A			
GPP_E16	GPO	N/A			
GPP_E17	GPO	N/A			
GPP_E18	GPO	N/A			
GPP_E19	GPO	N/A			
GPP_E20	GPO	N/A			
GPP_E21	GPO	N/A			
GPP_E22	GPO	N/A			
GPP_E23	GPO	N/A (CPU_OPI#)			
GPP_F0	GPO	N/A (SATA3_GP[0]#)			
GPP_F1	GPO	N/A (SATA4_GP[0]#)			
GPP_F2	GPO	N/A (SATA5_GP[0]#)			
GPP_F3	GPO	N/A (SATA6_GP[0]#)			
GPP_F4	GPO	N/A (SATA7_GP[0]#)			
GPP_F5	GPO	N/A (SATA8_GP[0]#)			
GPP_F6	GPO	N/A (SATA9_GP[0]#)			
GPP_F7	GPO	N/A (SATA10_GP[0]#)			
GPP_F8	GPO	N/A (SATA11_GP[0]#)			
GPP_F9	GPO	N/A (SATA12_GP[0]#)			
GPP_F10	GPO	N/A (SATA13_GP[0]#)			
GPP_F11	GPO	N/A (SATA14_GP[0]#)			
GPP_F12	GPO	N/A (SATA15_GP[0]#)			
GPP_F13	GPO	N/A (SATA16_GP[0]#)			
GPP_F14	GPO	N/A (SATA17_GP[0]#)			
GPP_F15	GPO	N/A (SATA18_GP[0]#)			
GPP_F16	GPO	N/A (SATA19_GP[0]#)			
GPP_F17	GPO	N/A (SATA20_GP[0]#)			
GPP_F18	GPO	N/A (SATA21_GP[0]#)			
GPP_F19	GPO	N/A (SATA22_GP[0]#)			
GPP_F20	GPO	N/A (SATA23_GP[0]#)			
GPP_F21	GPO	N/A (SATA_LED_N#)			
GPP_F22	GPO	N/A (SATA_LED_N#)			
GPP_F23	GPO	N/A (SATA_LED_N#)			
GPP_G0	Native	SD_CMD		3V/S PU 20K	+3VS
GPP_G1	Native	SD_D0		3V/S PU 20K	+3VS
GPP_G2	Native	SD_D1		3V/S PU 20K	+3VS
GPP_G3	Native	SD_D2		3V/S PU 20K	+3VS
GPP_G4	Native	SD_D3		3V/S PU 20K	+3VS
GPP_G5	GPO	N/A (SD_CD#)			
GPP_G6	GPO	N/A (SD_CLK)			
GPP_G7	GPO	N/A (SD_WP)			
GPIO0	Native	SD_PWR_EN#/GPIO		3V/S PU 8.2K	+3VS
GPIO1	Native	SD_PWR_EN#/GPIO		3V/S PU 8.2K	+3VS
GPIO2	Native	SD_PWR_EN#/GPIO		3V/S PU 8.2K	+3VS
GPIO3	Native	SD_PWR_EN#/GPIO		3V/S PU 8.2K	+3VS
GPIO4	Native	SD_PWR_EN#/GPIO		3V/S PU 8.2K	+3VS
GPIO5	Native	SD_PWR_EN#/GPIO		3V/S PU 8.2K	+3VS
GPIO6	Native	SD_PWR_EN#/GPIO		3V/S PU 8.2K	+3VS
GPIO7	Native	SD_PWR_EN#/GPIO		3V/S PU 8.2K	+3VS

EC IT8995 GPIO

Pin Name	Config	Signal Name	Default status	Ext Pull up / down	Power
GPA0	IO	PWR_SW	I,DW		
GPA1	IO	LID_SW#	I,DW		
GPA2	OD	CPU_PROCHOT	I,DW		
GPA3	ALT	CPU_PECI	I,DW		
GPA4	O	CLOCK_SERIES(TALOS_MAINBOARD_ID_0/1/2)	I,DW		
GPA5	O	CLOCK_SERIES	I,DW		
GPA6	ALT		I,DW		
GPA7	ALT	EC_WAKE_UP#	I,DW		
GPB0	ALT	EC_SCI#	I,DW		
GPB1	ALT	EC_SMI#	I,DW		
GPB2	ALT	EC_RST#	I,DW		
GPB3	ALT	EC_SWI#	I,DW		
GPB4	O	SMB_EN#	I,DW		
GPB5	O	EC_ON	I,DW		
GPB6	O	SYSTEM_LED	I,DW		
GPB7	O		I,DW		
GPC0	O	CHARGE_LED	I,DW		
GPC1	ALT	SMB_CLK	I,DW		
GPC2	ALT	SMB_DAT	I,DW		
GPC3	O	EC_SMB_CK2	I,DW		
GPC4	O	EC_SMB_DA2	I,DW		
GPC5	ALT	KBPC_CK_PM	I,DW		
GPC6	ALT	KBPC_DA_PM	I,DW		
GPC7	O		I,DW		
GPD0	O	PCH_SPI_WP#	I,DW		
GPD1	ALT	PCH_SPI_HOLD#	I,DW		
GPD2	ALT	PCH_SPI_CS#	I,DW		
GPD3	OD	EC_SCI#	I,DW		
GPD4	OD	EC_SMI#	I,DW		
GPD5	O	EC_RST#	I,DW		
GPD6	ALT	PCH_SPI_CLK	I,DW		
GPD7	ALT	PCH_SPI_SI	I,DW		
GPE0	O	PCH_SPI_SO	I,DW		
GPE1	O	EC_SWI#	I,DW		
GPE2	O	PCH_SPI_IO2	I,DW		
GPE3	O	PCH_SPI_IO3	I,DW		
GPE4	ALT	SMB_CLK	I,DW		
GPE5	ALT	SMB_DAT	I,DW		
GPE6	O	CPUVR_EN	I,DW		
GPE7	ALT	KBPC_CK_PM	I,DW		
GPF0	ALT	KBPC_DA_PM	I,DW		
GPF1	O	CPU_VID_SELECT	I,DW		
GPF2	O	CHARGER_EN	I,DW		
GPF3	O		I,DW		
GPF4	O	CPU_VID_SELECT	I,DW		
GPF5	O	CPUVR_EN	I,DW		
GPF6	I	CPU_VGA_THERM	I,DW		
GPF7	I	PWR_SW_THERM#/ALERT#	I,DW		
GPG0	O	CPU_VID	I,DW		
GPG1	ALT	SMB_CLK	I,DW		
GPG2	ALT	SMB_DAT	I,DW		
GPG3	O	EC_SMB_CK1	I,DW		
GPG4	O	EC_SMB_DA1	I,DW		
GPG5	O		I,DW		
GPG6	O		I,DW		
GPG7	O		I,DW		
GPH0	O		I,DW		
GPH1	O		I,DW		
GPH2	O		I,DW		
GPH3	O		I,DW		
GPH4	O		I,DW		
GPH5	O		I,DW		
GPH6	O		I,DW		
GPH7	O		I,DW		
GPI0	O		I,DW		
GPI1	O		I,DW		
GPI2	O		I,DW		
GPI3	O		I,DW		
GPI4	O		I,DW		
GPI5	O		I,DW		
GPI6	O		I,DW		
GPI7	O		I,DW		
GPJ0	ALT		I,DW		
GPJ1	ALT		I,DW		
GPJ2	ALT		I,DW		
GPJ3	ALT		I,DW		
GPJ4	ALT		I,DW		
GPJ5	ALT		I,DW		
GPJ6	ALT		I,DW		
GPJ7	O		I,DW		

Design IP Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
EC Master (SMB1)	**SM-Bus Address**
SM-Bus Device	
Battery	0x16
CPU Thermal Sensor	0x98

USB3 Port

USB3_0	USB 3.1 Type-A
USB3_1	USB 3.1 Type-A
USB3_2	USB 3.1 Type-A
USB3_3	

PCI Express

PCIE 1	
PCIE 2	8GBPS
PCIE 3	
PCIE 4	
PCIE 5	WLAN
PCIE 6	WLAN

SATA Port

SATA3	7mm
SATA1	HDD / 2nd HDD

PCI CLK

CLK0	CPU/PCH
CLK1	
CLK2	
CLK3	
CLK4	LAN
CLK5	WLAN

USB Port

USB 0	USB 2.0 Back	USB 3.1 Type-A
USB 1	USB 2.0 Back	USB 3.1 Type-A
USB 2	USB 2.0 Front	USB 2.0
USB 3	BT	BT
USB 4	CAMERA	
USB 5		
USB 6	Touch_Panel	
USB 7		
USB 8		
USB 9		
USB 10		

Device Identification

CPU Thermal Sensor	
Top	1001h/1451h/1423h
Bottom	

Notes

- Use Switch MOS Function Support.

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Reference	Value
C0602	1UF/6.3V
C0603	1UF/6.3V
C0604	1UF/6.3V
C0605	1UF/6.3V
C0607	1UF/6.3V
C0608	1UF/6.3V
C0613	1UF/6.3V
C0619	1UF/6.3V
C0621	1UF/6.3V
C0622	1UF/6.3V
C0624	1UF/6.3V
C0628	1UF/6.3V
C0629	1UF/6.3V
C0630	1UF/6.3V
C0631	1UF/6.3V
C0632	1UF/6.3V
C0633	1UF/6.3V
C0634	1UF/6.3V
C0635	1UF/6.3V
C0636	1UF/6.3V
C0638	1UF/6.3V
C0640	1UF/6.3V
C0651	1UF/6.3V
C0652	1UF/6.3V
C0653	1UF/6.3V
C0654	1UF/6.3V
C0655	1UF/6.3V
C0661	1UF/6.3V
C0663	1UF/6.3V
C0665	1UF/6.3V
C0667	1UF/6.3V
C0669	1UF/6.3V
C0670	1UF/6.3V
C0684	1UF/6.3V
C0694	1UF/6.3V
C1028	1UF/6.3V
C1030	1UF/6.3V
C1031	1UF/6.3V
C1034	1UF/6.3V
C1036	1UF/6.3V
C1037	1UF/6.3V
C1040	1UF/6.3V

#44

C1040	1UF/6.3V
C1041	1UF/6.3V
C1043	1UF/6.3V
C1044	1UF/6.3V
C2406	1UF/6.3V
C2407	1UF/6.3V
C2435	1UF/6.3V
C2603	1UF/6.3V
C2605	1UF/6.3V
C2606	1UF/6.3V
C2608	1UF/6.3V
C2611	1UF/6.3V
C2614	1UF/6.3V
C2615	1UF/6.3V
C2617	1UF/6.3V
C2618	1UF/6.3V
C2619	1UF/6.3V
C2620	1UF/6.3V
C2622	1UF/6.3V
C2623	1UF/6.3V
C2626	1UF/6.3V
C2627	1UF/6.3V
C2628	1UF/6.3V
C2676	1UF/6.3V

Reference	Value
C1306	1UF/6.3V
C1307	1UF/6.3V
C1308	1UF/6.3V
C1309	1UF/6.3V
C1310	1UF/6.3V
C1311	1UF/6.3V
C1418	1UF/6.3V
C1419	1UF/6.3V
C1420	1UF/6.3V
C1421	1UF/6.3V
C1423	1UF/6.3V
C1424	1UF/6.3V
C1425	1UF/6.3V
C1426	1UF/6.3V
C1428	1UF/6.3V
C1429	1UF/6.3V
C1430	1UF/6.3V
C1431	1UF/6.3V
C1433	1UF/6.3V
C1434	1UF/6.3V
C1435	1UF/6.3V
C1436	1UF/6.3V
C1438	1UF/6.3V
C1439	1UF/6.3V
C1440	1UF/6.3V
C1441	1UF/6.3V
C1443	1UF/6.3V
C1444	1UF/6.3V
C1445	1UF/6.3V
C1446	1UF/6.3V
C1448	1UF/6.3V
C1449	1UF/6.3V
C1450	1UF/6.3V
C1451	1UF/6.3V
C1453	1UF/6.3V
C1454	1UF/6.3V
C1455	1UF/6.3V
C1456	1UF/6.3V
C1702	1UF/6.3V
C1708	1UF/6.3V
C1713	1UF/6.3V
C1714	1UF/6.3V

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C1714	1UF/6.3V
C1717	1UF/6.3V
C1718	1UF/6.3V
C1720	1UF/6.3V
C1721	1UF/6.3V
C1723	1UF/6.3V
C1724	1UF/6.3V
C1727	1UF/6.3V
C3616	1UF/6.3V
C3617	1UF/6.3V
C4550	1UF/6.3V
C4555	1UF/6.3V
C7009	1UF/6.3V
C7010	1UF/6.3V
C7013	1UF/6.3V
C7016	1UF/6.3V
C7017	1UF/6.3V
C7019	1UF/6.3V
C7314	1UF/6.3V
C7315	1UF/6.3V
C7316	1UF/6.3V
C7317	1UF/6.3V
C7345	1UF/6.3V

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Reference	Value
C7027	1UF/6.3V
C7029	1UF/6.3V
C7104	1UF/6.3V
C7307	1UF/6.3V
C7308	1UF/6.3V
C7309	1UF/6.3V
C7337	1UF/6.3V

C0615
C1086
C1088
C1302
C1406
C1416
C1422
C1427
C1432
C1437
C1442
C1447
C1452
C1457
C1711
C1726
C1728
C2602
C2613
C2625
C3012
以上，請幫忙評估換0402

C2602/13/25 can't change 0402
C3012 ~ C3018

#80
R761,4,R7701
C7910,C7555
C7911,C7556
C304,C2303
C306,C2304
C303,C2305
C307,C2306
C305,C2307

5.1. Power Management/Isolation

Table 1. Power Management/Isolation

Symbol	Type	Pin No	Description
LANWAKEB	O/D	33	Power Management Event. Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	32	Isolate Pin: Active low. Used to isolate the RTL8402 from the PCI Express bus. The RTL8402 will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2. PCI Express Interface

Table 2. PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK_P	I	21	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_N	I	22	
HSOP	O	25	PCI Express Transmit Differential Pair.
HSON	O	24	
HSIP	I	19	PCI Express Receive Differential Pair.
HSIN	I	20	
PERSTB	I	30	PCI Express Reset Signal: Active low. When the PERSTB is asserted or power-on state, the RTL8402 returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	29	Reference Clock Request Signal. This signal is used by the RTL8402 to request starting of the PCI Express reference clock.

5.3. EEPROM (TWSI)

Table 3. EEPROM (TWSI)

Symbol	Type	Pin No	Description
SCL/LED_CR	O	35	SCL: Clock interface for TWSI EEPROM.
SDA	IO	36	SDA: Data interface for TWSI EEPROM. Refer to the reference schematic for strapping pin information. All strapping pins are power-on latch pins.

5.4. Transceiver Interface

Table 4. Transceiver Interface

Symbol	Type	Pin No	Description
MDIP0	IO	2	In MDI mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN0	IO	3	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	IO	4	In MDI mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN1	IO	5	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.

5.5. Clock

Table 5. Clock

Symbol	Type	Pin No	Description
CKXTAL1	I	41	Input of 25MHz Clock Reference.
CKXTAL2	IO	46	Output of 25MHz Clock Reference. Input of External Clock Source.

5.6. Reference

Table 6. Reference

Symbol	Type	Pin No	Description
RSET	I	48	Reference. External resistor reference.

5.7. LEDs

Table 7. LEDs

Symbol	Type	Pin No	Description
SCL/LED_CR	O	35	See Section 6.2.5 Customizable LED Configuration, Page 11 for Details.
LED0	O	39	
LED1	O	37	

Note: During power down mode, the LED signals are logic high.

5.8. Card Reader

Table 8. Card Reader

Symbol	Type	Pin No	Description
SD_D0/MS_D7/xD_D5	IO	13	SD Data 0 (SD_DAT0), MS Data 7 (MS_D7), and xD Data 5 (xD_D5).
SD_D1/MS_CLK/xD_D4	IO	12	SD Data 1 (SD_DAT1), MS Clock (MS_CLK), and xD Data 4 (xD_D4)
SD_D2/xD_D7	IO	17	SD Data 2 (SD_DAT2) and xD Data 7 (xD_D7).
SD_D3/MS_D3/xD_D2	IO	18	SD Data 3 (SD_DAT3), MS Data 3 (MS_D3), and xD Data 2 (xD_D2)
SD_D4/xD_WE#/	IO	11	SD Data 4 (SD_DAT4) and xD Write Enable (xD_WE#)
SD_D5/xD_CE#	IO	10	SD Data 5 (SD_DAT5) and xD Chip Select (xD_CE#)
SD_D6/MS_D6/xD_RE#	IO	9	SD Data 6 (SD_DAT6), MS Card Detect (MS_D6#), and xD Read Enable (xD_RE#)
SD_D7/xD_RDY	IO	8	SD_D7/xD_RDY: SD Data7 and xD Ready Signal (xD_RDY).
SD_CLK/MS_D5/xD_D1	IO	14	SD Clock (SD_CLK), MS Data 5 (MS_D5), and xD Data 4 (xD_D4).
SD_CMD/MS_D4/xD_D3	IO	15	SD Serial Protocol Command, and Response Signal, MS_Data 4 (MS_D4), and xD Data 3 (xD_D3)
SD_WP/MS_D1/xD_WP#	IO	28	SD Write Protect (SD_WP), MS_Data 1 (MS_D1), and xD Write Protect (xD_WP#).
SD_CD/MS_D3/xD_ALE	IO	41	SD Card Detect (SD_CD#), MS_Data 3 (MS_D3), and xD Address Latch Enable (xD_ALE).
MS_BS/xD_CLE	IO	37	MS_BS and xD Command Latch Enable (xD_CLE)
MS_D4/xD_D0	IO	42	MS_Data 4 (MS_D4) and xD Data 0 (xD_D0)
MS_D0/xD_D1	IO	43	MS_Data 0 (MS_D0) and xD Data 1 (xD_D1)
xD_CD#	I	44	xD Card Detect (xD_CD).

5.9. GPO Pin

Table 9. GPO Pin

Symbol	Type	Pin No	Description
GPO	IO	38	General Purpose IO Pin (Used for Power Saving Feature).

5.10. Power and Ground

Table 10. Power and Ground

Symbol	Type	Pin No	Description
DVDD33	P	6, 31	Digital 3.3V Power Supply.
DVDD10	P	34	Digital 1.05V Power Supply.
EVDD10	P	18	LDO Regulator 1.05V Output.
Card_3V3	P	7	3.3V Power for All Cards.
VDD33/18	P	16, 40	SD UHS Mode Power Supply.
CTRL10	P	47	LDO Regulator 1.05V Output.
AVDD33	P	1	Analog 3.3V Power Supply.
GND	P	23	Ground.
GND	P	49	Ground (Exposed Pad).

8.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be effected. All voltages are specified reference to GND unless otherwise specified.

Table 18. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
AVDD33, CARD_3V3, DVDD33	Supply Voltage 3.3V	-0.3	3.6	V
DVDD10, EVDD10, CTRL10	Supply Voltage 1.05V	-0.3	1.32	V
3.3V DC Input	Input Voltage	-0.3	3.6	V
3.3V DC Output	Output Voltage			
1.05V DC Input	Input Voltage	-0.5	1.32	V
1.05V DC Output	Output Voltage			
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

8.2. Recommended Operating Conditions

Table 19. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	AVDD33, CARD_3V3, DVDD33 DVDD10, EVDD10, CTRL10	3.14 1.00	3.3 1.05	3.46 1.10	V V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

8.6. DC Characteristics

Table 23. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
AVDD33, CARD_3V3, DVDD33	3.3V Supply Mean Voltage	-	3.14	3.3	3.46	V
DVDD10, EVDD10, CTRL10	1.05V Supply Mean Voltage	-	1.00	1.05	1.10	V
Voh	Minimum High Level Output Voltage	Ioh = -4mA	0.9*VDD33	-	VDD33	V
Vol	Maximum Low Level Output Voltage	Iol = 4mA	0	-	0.1*VDD33	V
Vih	Minimum High Level Input Voltage	-	2.0	-	-	V
Vil	Maximum Low Level Input Voltage	-	-	-	0.8	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	µA
Icc33	Maximum Operating Supply Current from 3.3V	At 100Mbps with heavy network traffic and with Card Reader R/W operation	-	850	-	mA
Icc10	Maximum Operating Supply Current from 1.05V	At 100Mbps with heavy network traffic and with Card Reader R/W operation	-	150	-	mA

Note 1: Refer to the latest schematic circuit for correct configuration.
Note 2: All Supply Mean Voltage power noise <±5% of Mean Voltage.

8.8.4. Auxiliary Signal Timing Parameters

Table 29. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PVPGL}	Power Stable to PERSTB Inactive	100	-	ms
$T_{PERSTCLK}$	REFCLK Stable before PERSTB Inactive	100	-	µs
T_{PERST}	PERSTB Active Time	100	-	µs
$T_{FAIL/RTN}$	PERSTB Rising Time Duration	10	-	ms
T_{PVRL}	Power Down Low Time for PERSTB Inactive	500	-	ns
T_{PRVPG}	3.3 Main Power On Time	-	300	ms

Note: T_{PVPGL} must be met to guarantee the power rail going out of specification (exceeding the specified operating voltage by more than 500 mV). Refer to PCI Express Mini Card Electromechanical Specification Revision 1.0 for further information. T_{PVRL} can be disregarded when implementation and timing of T_{PVPGL} will not affect any L2/3 Ready.
Note 1: The ISOLATEB pin should follow the behavior of the 3.3V main power waveform.

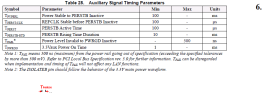

Figure 17. Auxiliary Signal Timing

6. Power Sequence

Figure 21. Power Sequence

Table 1. Power Sequence Parameter

Symbol	Description	Min	Typical	Max	Units
Ps1	1.1V Rise Time	0	-	100	ms
Ps2	3.3/1.5V Off Time	70	-	-	ms

Note 1: Ps1 must be met to guarantee don't A/V bug. Ps1 < 100ms, Ps1 must be controlled over 5ms.
Note 2: If there is any action that involves consecutive ON/OFF toggling of the LDO regulator source (1.1V), the designer must make sure the OFF time of both the LDO regulator source (1.1V) and output (1.05V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 70ms).

CPU XDP connector

eDP to LVDS

BOM

ASUS	Project Name: X430	Rev: REV.0
Title : LVDS CONNECTOR		
Size:	Dept.: Notebook COMPUTER Inc. Engineer: EE	
Date: Thursday, August 30, 2018	Sheet 46 of 158	

LPC DEBUG PORT

BOM

ASUS	Project Name: X430	Rev: R2.0
Title : DEBUG PORT		
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
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0915-4 Dean Del Green CLK ckt(page9,24,29,75)

ASUSTeK COMPUTER INC. NEI	Title : Green CLK Gen	
	Engineer: EE	
Size: Custom	Project Name: X430	Rev: REV
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RC04

ASUS	Project Name: X430	Rev: RC0.0
Title : CARD READER CONNECTOR		
Size: A3	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
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/ISUS	Project Name X430	Rev R2.0

Title : SDIO_CR

Size	Dept.:	Engineer:
A	ASUSTeK COMPUTER INC.	EE

ASUS	Project Name X430	Rev R2.0

Title : RTL8402_RJ45

Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
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/ISUS	Project Name **X430**	Rev R2.0

Title :

Size		
C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** EE

/ISUS	Project Name **X430**	Rev R2.0

Title : CB-****

Size C	**Dept.:** ASUSTeK COMPUTER INC. **Engineer:** EE	
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<Variant Name>

ASUS	Title : DDR4_ON-BOARD_A2	
	Engineer: EE	
Size: Custom	Project Name: X430	Rev: R2.0
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<Variant Name>

	Title : DDR4_SO-DIMM_1	
	Engineer: NB EE2	
Size: C	Project Name: X430	Rev: R2.0
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ASUS	Project Name X430	Rev R2.0

Title : CRT D-SUB

Size	Dept.:	Engineer:
D	ASUSTeK COMPUTER INC.	EE

/ISUS	Project Name X430	Rev R2.0

Title : DDR3_ON-BOARD_B_H32

Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB EE2
Date: Thursday, August 30, 2018	Sheet 19 of 104	

	Project Name **X430**	Rev R2.0

Title : HDD Board-Speaker

Size C	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** EE

Date: Thursday, August 30, 2018	Sheet	38	of	104

ASUS	Project Name X430	Rev R2.0

Title : small board_Screw_hole

Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer:
Date: Thursday, August 30, 2018	Sheet 12 of 104	

	Project Name **X430**	Rev R2.0

Title : small board_USB Port

Size D	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** EE
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<Variant Name>

Title <Title>		
Size A	Document Number X430	Rev R2.0
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<Variant Name>

Title <Title>		
Size A	Document Number X430	Rev R2.0
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<Variant Name>

Title <Title>		
Size A	Document Number X430	Rev R2.0
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	Project Name **X430**	Rev R2.0

Title : POWER_+VGFX_CORE

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** EE

/ISUS	Project Name **X530FN**	Rev R2.0

Title : POWER

Size Custom	**Dept.:** Power team	**Engineer:** Andy
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/ISUS	Project Name **X430**	Rev R2.0

Title : POWER_+VGFX_CORE

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** EE

/ISUS	Project Name X430	Rev R2.0

Title : IO_SATA HDD & SPEAKER

Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
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/ISUS	Project Name X430	Rev R2.0

Title : Sensors

Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
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<Variant Name>

	Project Name **X530FN**	Rev R2.0

Title : POWER

Size Custom	**Dept.:** Power team	**Engineer:** Andy

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	Project Name **X430**	Rev R2.0
Title : ****		
Size C	**Dept.:** ASUSTeK COMPUTER INC. **Engineer:** EE	
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<Variant Name>

Project Name X530FN		Rev R2.0
Title : PW_+VCCIO / +VCCPRIM_CORE		
Size A2	**Dept.:** Power team	**Engineer:** Andy
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<Variant Name>

	Project Name **X530FN**	Rev R2.0

Title : POWER

Size Custom	**Dept.:** Power team	**Engineer:** Andy

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	Project Name X430	Rev R2.0

Title : NFC

Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
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	Project Name **X430**	Rev R2.0

Title : POWER_+VGFX_CORE

Size Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
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/ISUS	Project Name **X430**	Rev R2.0

Title : POWER_+VGFX_CORE

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** EE

	Project Name **X430**	Rev R2.0

Title : POWER_+VGFX_CORE

Size Custom	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** EE

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