1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X2728 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6			2021-02-04

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PAGE	CSA	CONTENTS	SYNC	DATE
1	1	SCHEM, MLB, T728		
2	2	REFERENCE DESIGN TABLE		10/23/2019
3	4	PD PARTS	GAREN	03/09/2020
4	5	SOC: CONFIG STRAPS	T585_REF_SOC_H13S_0.0.44	
5	6	SOC: RESETS, CLOCKS, SWD	T585_REF_SOC_H13S_0.0.44	
6	8	SOC: GPIO, I2C, I2S, SPI, UART	T585_REF_SOC_H13S_0.0.44	
7	10	SOC: LPDP, ISP, MIPI	T585_REF_SOC_H13S_0.0.44	
8	12	SOC: PCIE	T585_REF_SOC_H13S_0.0.44	
9	14	SOC: CIO, USB	T585_REF_SOC_H13S_0.0.44	
10	16	SOC: AOP, SMC, NUB	T585_REF_SOC_H13S_0.0.44	
11	19	SOC: SHARED SUPPORT	BYRON	09/18/2020
12	20	SOC: SPI NOR & SEP ROM	T585_REF_SOC_H13S_0.0.44	
13	21	PROJECT SUPPORT (1/2)	GAREN	09/18/2020
14	22	PROJECT SUPPORT (2/2)	T724_TKIM3_MLB_S_0.46.0	03/19/2020
15	23	SOC: POWER (CPU, GPU)	T585_REF_SOC_H13S_0.0.44	
16	25	SOC: POWER (SRAM, DISP, DCS)	T585_REF_SOC_H13S_0.0.44	
17	27	SOC: POWER (VDD1, VDD2)	T585_REF_SOC_H13S_0.0.44	
18	29	SOC: POWER (VDDQ)	T585_REF_SOC_H13S_0.0.44	
19	31	SOC: POWER (AFR, ANE, CIO)	T585_REF_SOC_H13S_0.0.44	
20	33	SOC: POWER (FABRIC, FIXED)	T585_REF_SOC_H13S_0.0.44	
21	35	SOC: POWER (VDDIO)	T585_REF_SOC_H13S_0.0.44	
22	37	SOC: POWER (VDD2H0)	T585_REF_SOC_H13S_0.0.44	
23	39	SOC: POWER (VDD2H1)	T585_REF_SOC_H13S_0.0.44	
24	41	SOC: GND-1	T585_REF_SOC_H13S_0.0.44	
25	42	SOC: GND-2	T585_REF_SOC_H13S_0.0.44	
26	50	Secure Element	T585_REF_SE_CERES_0.13.0	
27	51	BATTERY CONN	AMIR_T724	03/25/2020
28	52	PBUS SUPPLY & BATTERY CHARGER	T585_REF_MAGSAFE_ACE2_0.68.0	
29	53	MAGSAFE: WHAMOLA SUPPORT	T585_REF_MAGSAFE_ACE2_0.68.0	
30	54	MAGSAFE: CONNECTOR	T585_REF_MAGSAFE_ACE2_0.68.0	
31	55	MAGSAFE: PORT CONTROLLER	T585_REF_MAGSAFE_ACE2_0.68.0	
32	56	MAGSAFE: CONTROLLER SUPPORT	T585_REF_MAGSAFE_ACE2_0.68.0	
33	57	POWER: 3V8 AON (1/2)	T585_REF_VR_ICEMAN_1.25.0	
34	58	POWER: 3V8 AON (2/2)	T585_REF_VR_ICEMAN_1.25.0	
35	60	POWER: 3V8 AON OUTPUT THROTTLE	T585_REF_VR_ICEMAN_HP_0.25.0	
36	76	PMU BUCK OUTPUT DESENSE CAPS	T724_DTUZMAN_MLB_S_1.05.0	05/20/2020
37	77	PMIC SLAVE VIN/LDO/SW	T585_REF_PMIC_MAVERICKS_0.89.0	
38	78	PMIC SLAVE BUCKS	T585_REF_PMIC_MAVERICKS_0.89.0	
39	79	PMIC SLAVE GPIO & GND	T585_REF_PMIC_MAVERICKS_0.89.0	
40	80	PMIC BUCK OUTPUT CAPS	T585_REF_PMIC_MAVERICKS_0.89.0	
41	81	PMIC MASTER VIN/LDO/SW	T585_REF_PMIC_MAVERICKS_0.89.0	
42	82	PMIC MASTER BUCKS	T585_REF_PMIC_MAVERICKS_0.89.0	
43	83	PMIC MASTER GPIO & GND	T585_REF_PMIC_MAVERICKS_0.89.0	
44	84	PMU PROJECT-SPECIFIC SUPPORT	T724_DTUZMAN_MLB_S_2.05.0	05/27/2020
45	85	PMU PROJECT SPECIFIC SUPPORT 2	T728_MLB_1.15.0	12/02/2020
46	92	VIPER SUPPORT	MLADEN	04/15/2020
47	93	VIPER CONTROLLER	T585_REF_VR_VIPER_0.61.0	
48	94	VIPER POWER STAGES 1	T585_REF_VR_VIPER_0.61.0	
49	95	VIPER POWER STAGES 2	T585_REF_VR_VIPER_0.61.0	
50	101	MONACO 0	T585_REF_CLVR_MONACO_0.74.0	
51	102	MONACO 1	T585_REF_CLVR_MONACO_0.74.0	
52	105	MONACO 4	T585_REF_CLVR_MONACO_0.74.0	
53	120	MONACO PROJECT SUPPORT	DTUZMAN	01/10/2020
54	122	POWER: 5V S2 TPS62130	T585_REF_VR_5V_TPS62130_0.11.0	
55	130	I2C Connections - AP	APADRON7	03/04/2020
56	131	I2C Connections - SMC	APADRON7	03/04/2020
57	132	I2C Connections - Other	APADRON7	03/04/2020
58	135	SENSORS: HIGH-SIDE (1/2)	HKUKRATI	05/15/2020
59	136	SENSORS: HIGH-SIDE (2/2)	HKUKRATI	03/02/2020
60	137	SENSORS: HIGH-SIDE	HKUKRATI	03/02/2020

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61	138	SENSORS: LOW-SIDE (1/3)	HKUKRATI	05/15/2020
62	139	SENSORS: LOW-SIDE (2/3)	HKUKRATI	03/02/2020
63	140	SENSORS: LOW-SIDE (3/3)	HKUKRATI	03/25/2020
64	141	SENSORS:THERMAL	T724_HKUKRATI_MLB_S_2.05.0	05/20/2020
65	144	SENSORS: MOTION	T585_REF_IMU_COBOL_0.0.6	
66	145	FANS		01/10/2020
67	150	USB-C: High Speed ATC0	T585_REF_USBC_ACE2_0.33.0	
68	151	USB-C: High Speed ATC1	T585_REF_USBC_ACE2_0.33.0	
69	152	USB-C: Support 1 ATC01	T585_REF_USBC_ACE2_0.33.0	
70	153	USB-C: Support 2 ATC01	T724_RUENJOU_MLB_S_0.53.0	05/26/2020
71	154	USB-C: Port Controller ATC0	T724_RUENJOU_MLB_S_0.53.0	05/26/2020
72	155	USB-C: Port Controller ATC1	T724_RUENJOU_MLB_S_0.53.0	05/26/2020
73	156	USB-C: Left Connectors	BYRON	04/01/2020
74	157	USB-C: HS Level Shifters	T585_REF_USBC_ACE2_0.40.0	
75	158	USB-C: 5V Regulator	T585_REF_USBC_VR_LT8642_0.8.5	
76	159	USB-C: CC Protection	T728_MLB_1.15.0	11/20/2020
77	160	USB-C: High Speed ATC2	T585_REF_USBC_ACE2_0.33.0	
78	162	USB-C: Support 1 ATC23	T724_RUENJOU_MLB_S_0.53.0	02/18/2020
79	163	USB-C: Support 2 ATC23	T724_RUENJOU_MLB_S_0.53.0	05/26/2020
80	164	USB-C: Port Controller ATC2	T724_RUENJOU_MLB_S_0.53.0	05/26/2020
81	166	USB-C: Right Connector	BYRON	04/01/2020
82	167	USB-C: HS Level Shifters	T585_REF_USBC_ACE2_0.40.0	
83	168	USB-C: 5V Regulator	T585_REF_USBC_VR_TPS62180_0.6.3	
84	169	USB-C: CIO Redrivers 2/3	T585_REF_CIO_RDVR_COLUMBUS_0.7.0	
85	170	USB-C: SUPPORT	T728_MLB_0.67.0	09/18/2020
86	175	HDMI: CONNECTOR	T585_REF_HDMI_MADEA_0.15.1	
87	176	HDMI: DESENSE FILTERS	T585_REF_HDMI_MADEA_0.15.1	
88	177	HDMI: MADEA	T585_REF_HDMI_MADEA_0.15.1	
89	178	HDMI: Project Support 1	T585_REF_HDMI_MADEA_0.15.1	
90	179	HDMI: Project Support 2	T585_REF_HDMI_MADEA_0.15.1	
91	195	SDCARD CONTROLLER	T585_REF_SDCARD_GL9755_0.17.0	
92	196	SDCARD CONNECTOR	T585_REF_SDCARD_GL9755_0.17.0	
93	197	SDCARD IO LS/BUF SUPPORT	T585_REF_SDCARD_GL9755_0.17.0	
94	198	SDCARD POWER SUPPORT	T585_REF_SDCARD_GL9755_0.17.0	
95	200	WIFI/BT: MODULE	T585_REF_WIRELESS_TYPHOON_0.28.0	
96	201	WIFI/BT: ANTENNA and GND	T585_REF_WIRELESS_TYPHOON_0.28.0	
97	220	STORAGE: SSD0 S5E <0>	T585_REF_STORAGE_S5E_0.36.0	
98	221	STORAGE: SSD0 S5E <1>	T585_REF_STORAGE_S5E_0.36.0	
99	222	STORAGE: SSD0 S5E <2>	T585_REF_STORAGE_S5E_0.36.0	
100	223	STORAGE: SSD0 S5E <3>	T585_REF_STORAGE_S5E_0.36.0	
101	224	STORAGE: SSD0 OCARINA & NAND VCC	T585_REF_STORAGE_S5E_0.36.0	
102	225	STORAGE: SSD1 S5E <0>	T585_REF_STORAGE_S5E_0.36.0	
103	226	STORAGE: SSD1 S5E <1>	T585_REF_STORAGE_S5E_0.36.0	
104	227	STORAGE: SSD1 S5E <2>	T585_REF_STORAGE_S5E_0.36.0	
105	228	STORAGE: SSD1 S5E <3>	T585_REF_STORAGE_S5E_0.36.0	
106	229	STORAGE: SSD1 OCARINA & NAND VCC	T585_REF_STORAGE_S5E_0.36.0	
107	230	STORAGE: SSD SUPPORT	WUDI_T668_MLB	09/18/2020
108	234	CAMERA: FLEX CONNECTOR	COLIN	09/10/2020
109	236	DISPLAY CONNECTOR	T728_YANIR_MLB_0.62.4	12/03/2020
110	237	DISPLAY POWER SEQUENCER	T585_REF_PANELPWR_2D_0.7.0	
111	238	LUXE LCD Backlight Driver	T585_REF_BLC_LUXE_0.28.0	
112	239	BCON CONNECTOR	T585_REF_BLC_LUXE_0.28.0	
113	242	SECDIS: LID ANGLE SENSOR	T585_REF_LAS_LID_0.6.0	09/18/2020
114	243	SECDIS: DMIC_LID_CONTROL	T585_REF_LAS_LID_0.6.0	
115	245	AUDIO JACK CODEC	T585_REF_CODEC_CARLOW_1.1.0	
116	246	AUDIO AMPLIFIERS (1/2)	T585_REF_SPKRAMP_SN012776_3.3.0	
117	247	AUDIO AMPLIFIERS (2/2)	T585_REF_SPKRAMP_SN012776_3.3.0	
118	248	AUDIO CONNECTORS: AMPS	RAYMOND	09/18/2020
119	249	Audio Flex Connectors	RAYMOND	09/18/2020
120	250	BEN: KEYBD BKLT	T585_REF_BLC_BEN_KBD_ONLY_0.4.0	

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122	252	KEYBOARD SIGNAL CONNECTOR, ESD	RAYMOND	09/18/2020
123	253	TRACKPAD SUPPORT	T724_HKUKRATI_MLB_S_0.94.0	04/17/2020
124	254	TRACKPAD CONNECTOR	HKUKRATI	01/18/2020
125	255	TOUCHID CONN	JSHAO	03/02/2020
126	256	TOUCHID SUPPORT	T585_REF_MESA_SUPPORT_0.14.0	
127	257	TOUCHID_BACKLIGHT	T585_REF_MESA_BACKLIGHT_0.1.0	
128	266	FCT 1	SELIM	01/06/2021
129	267	FCT 2	SELIM	12/10/2020
130	268	PMU TEST POINTS	SELIM	01/22/2021
131	271	Debug: LEDs, Koba	TAEWAN_T724	03/23/2020
132	272	Debug: Buttons	TAEWAN_T724	03/23/2020
133	282	DESENSE_1	MLADEN	04/27/2020
134	295	DEBUG: VITAMIN-C	T724_TKIM3_MLB_S_0.39.0	05/18/2020
135	401	POWER ALIASES 1	DTUZMAN	01/31/2020
136	402	POWER ALIASES 2	DTUZMAN	01/28/2020
137	403	POWER ALIASES CLVR	T585_REF_PMIC_MAVERICKS_0.86.0	05/07/2020
138	404	POWER ALIASES MPMU	T585_REF_PMIC_MAVERICKS_0.86.0	
139	405	POWER ALIASES SPMU	T585_REF_PMIC_MAVERICKS_0.86.0	
140	406	SIGNAL ALIASES - 1 (HIGH SPEED)	GAREN	06/23/2020
141	407	SIGNAL ALIASES 2		10/29/2019
142	408	SIGNAL ALIASES 3		06/24/2020
143	409	SIGNAL ALIASES - 4	GAREN	06/23/2020
144	411	SIGNAL ALIASES-T728		03/10/2020
145	501	17.2 RULES	CONSTRAINTS	01/08/2020
146	502	17.2 PHYSICAL CSETS	CONSTRAINTS	01/08/2020
147	503	17.2 SPACING CSETS, ISO	CONSTRAINTS	01/08/2020
148	504	17.2 SPACING CSETS, CLASS-CLASS	CONSTRAINTS	01/08/2020
149	601	BOM TABLES	T668_MLB	01/30/2020
150	602	BOM OPTION TABLES	T668_MLB_5.7.0	05/20/2020
151	603	BOM GROUPS	T668_MLB_5.7.0	05/20/2020
152	604	BOM VARIANT TABLES	T668_MLB_5.7.0	05/20/2020
153	611	BOM ALTERNATES	T668_MLB_5.7.0	05/01/2020
154	701	PACK OPTIONS		10/20/2019
155	999	TEMPORARY ALIASES	GAREN	06/23/2020

CHECKPLUS RULE CONFIGURATIONS	
CHECK VOLTAGE IC - LEVELS	?
PCB TESTPOINTS ALLOWED	YES
CHECK FATAL PACK_OPTION	YES

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-05641	1	SCHEM,MLB,X2728	SCH	CRITICAL	SCH
820-02100	1	PCBF,MLB,X2728	PCB	CRITICAL	PCB

SCHEM, MLB, T728

SYNC_DATE=10/04/2019

DRAWING TITLE: SCHEM,MLB-S,X2728

Apple Inc.

DRAWING NUMBER: 051-05641 SIZE: D

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SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
T585	REF_SOC_H13S	5,6,8,10,12,14,16,20,23,25,27,29,31,33,35,37,39,41,42	0.0.44	S	2020_08_25_19:51:48
T585	REF_SE_CERES	50	0.13.0	S	2020_02_27_16:33:46
T585	REF_MAGSAFE_ACE2	52-56	0.68.0	S	2021_01_29_16:52:02
T585	REF_VR_ICEMAN	57,58	1.25.0	S	2020_11_30_14:38:35
T585	REF_VR_ICEMAN_HP	60	0.25.0	S	2020_11_30_14:39:44
T585	REF_PMIC_MAVERICKS	77-83	0.89.0	S	2021_01_26_21:06:59
T585	REF_VR_VIPER	93,94,95	0.61.0	S	2021_01_27_13:09:56
T585	REF_CLVR_MONACO	101,102,105,106	0.74.0	S	2020_11_30_14:41:17
T585	REF_VR_5V_TPS62130	122	0.11.0	S	2020_12_01_11:36:35
T585	REF_IMU_COBOL	144	0.0.6	S	2020_12_01_11:35:58
T585	REF_USBC_ACE2	157,167	0.40.0	S	2021_01_11_12:16:11
T585	REF_CIO_RDVR_COLUMBUS	169	0.7.0	S	2021_01_14_12:53:02
T585	REF_USBC_VR_LT8642	158	0.8.5	S	2020_09_09_12:38:55
T585	REF_USBC_VR_TPS62180	168	0.6.3	S	2020_08_24_13:32:22
T585	REF_HDMI_MADEA	175-179	0.15.1	S	2020_12_01_17:03:28
T585	REF_SDCARD_GL9755	195-198	0.17.0	S	2021_01_19_14:27:56
T585	REF_WIRELESS_TYPHOON	200,201	0.28.0	S	2020_12_04_18:38:32
T585	REF_STORAGE_S5E	220-229	0.36.0	S	2020_05_01_14:39:35
T585	REF_PANELPWR_2D	237	0.7.0	S	2020_09_14_16:14:38
T585	REF_BLC_LUXE	238,239	0.28.0	S	2021_01_26_13:37:42
T585	REF_LAS_LID	242,243	0.6.0	S	2020_09_08_18:41:24
T585	REF_CODEC_CARLOW	245	1.1.0	S	2020_12_01_11:32:53
T585	REF_SPKRAMP_SN012776	246,247	3.3.0	S	2020_12_01_11:32:10
T585	REF_BLC_BEN_KBD_ONLY	250	0.4.0	S	2020_03_29_14:11:13
T585	REF_KBD_34PIN	251	0.2.0	S	2020_05_26_18:38:49
T585	REF_MESA_SUPPORT	256	0.14.0	H	2020_03_13_12:25:09
T585	REF_MESA_BACKLIGHT	257	0.1.0	S	2021_01_26_10:53:41
J316.SAKKOC	MLB_S	268	?	?	?

PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	PIN DELAY CSV FILE NAME
U0600	SGA_PINDELAY_2020_01_08.CSV

SYNC_DATE=10/23/2019

PAGE TITLE

REFERENCE DESIGN TABLE

Apple Inc.

DRAWING NUMBER 051-05641 | SIZE D

REVISION 6.33.0

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MAGSAFE BOSS

BS0450
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS0451
2.7X1.8R-1.4ID-1.7H-SM
860-01714

L USBC BOSS

BS04F0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04F1
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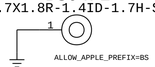
860-01714

BS04F2
2.7X1.8R-1.4ID-1.7H-SM
860-01714



R USBC BOSS

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860-01714

BS04G1
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860-01714

ANTENNA BOSS

BS04L0
2.7X1.8R-1.4ID-1.7H-SM
860-01714

BS04L1
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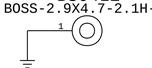
860-01714

BS04L2
BOSS-2.9X4.7-2.1H-SM
860-01841



DISP, CAM BOSS

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860-01714

BS04P1
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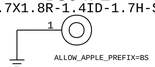
860-01714



BKLT BOSS

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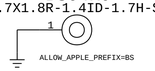
860-01714

BS04P3
2.7X1.8R-1.4ID-1.7H-SM
860-01714

LAS BOSS

BS04R0
2.7X1.8R-1.4ID-1.7H-SM
860-01714



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860-01714

L SPEAKER BOSS

BS04R2
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860-01714

R SPEAKER BOSS

BS04R3
2.7X1.8R-1.4ID-1.7H-SM
860-01714

AUDIO JACK BOSS

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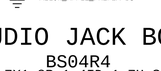
860-01714



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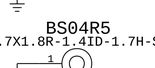
860-01714



TRACKPAD BOSS

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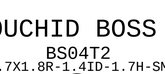
BOSS-3.4OD1.75ID-2.6H-SM
860-01717

BS04T1
BOSS-3.4OD1.75ID-2.6H-SM
860-01717

TOUCHID BOSS

BS04T2
2.7X1.8R-1.4ID-1.7H-SM
860-01714

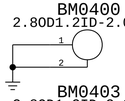


BS04T3
2.7X1.8R-1.4ID-1.7H-SM
860-01714

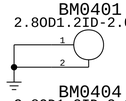
BUMPERS

860-01715

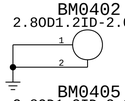
BM0400
2.8OD1.2ID-2.0H-SM



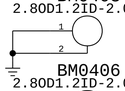
BM0401
2.8OD1.2ID-2.0H-SM



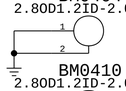
BM0402
2.8OD1.2ID-2.0H-SM



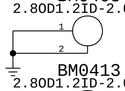
BM0403
2.8OD1.2ID-2.0H-SM



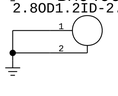
BM0404
2.8OD1.2ID-2.0H-SM



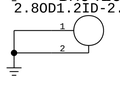
BM0405
2.8OD1.2ID-2.0H-SM



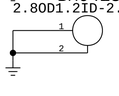
BM0406
2.8OD1.2ID-2.0H-SM



BM0410
2.8OD1.2ID-2.0H-SM



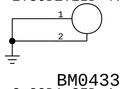
BM0413
2.8OD1.2ID-2.0H-SM



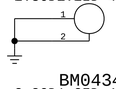
BUMPERS

860-01839

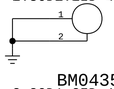
BM0430
2.8OD1.2ID-4.0H-SM



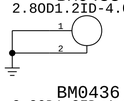
BM0431
2.8OD1.2ID-4.0H-SM



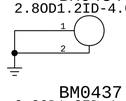
BM0432
2.8OD1.2ID-4.0H-SM



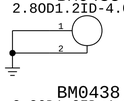
BM0433
2.8OD1.2ID-4.0H-SM



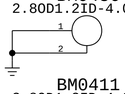
BM0434
2.8OD1.2ID-4.0H-SM



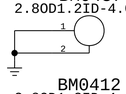
BM0435
2.8OD1.2ID-4.0H-SM



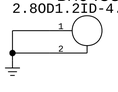
BM0436
2.8OD1.2ID-4.0H-SM



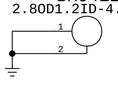
BM0437
2.8OD1.2ID-4.0H-SM



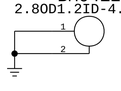
BM0438
2.8OD1.2ID-4.0H-SM



BM0411
2.8OD1.2ID-4.0H-SM



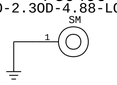
BM0412
2.8OD1.2ID-4.0H-SM



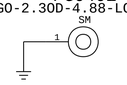
POGO PINS

870-08821

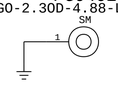
PG0400
POGO-2.3OD-4.88-LOW FORCE



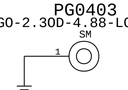
PG0401
POGO-2.3OD-4.88-LOW FORCE



PG0402
POGO-2.3OD-4.88-LOW FORCE

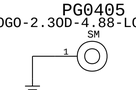


PG0403
POGO-2.3OD-4.88-LOW FORCE

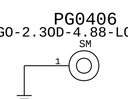


PG0404
POGO-2.3OD-4.88-LOW FORCE

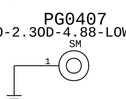
PG0405
POGO-2.3OD-4.88-LOW FORCE



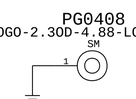
PG0406
POGO-2.3OD-4.88-LOW FORCE



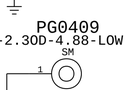
PG0407
POGO-2.3OD-4.88-LOW FORCE



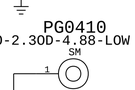
PG0408
POGO-2.3OD-4.88-LOW FORCE



PG0409
POGO-2.3OD-4.88-LOW FORCE



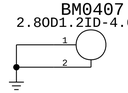
PG0410
POGO-2.3OD-4.88-LOW FORCE



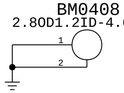
BUMPERS

860-01722

BM0407
2.8OD1.2ID-4.6H-SM



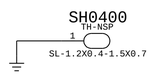
BM0408
2.8OD1.2ID-4.6H-SM



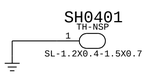
SHIELD CAN SLOTS

998-04440

SH0400
TH-NSP
SL-1.2X0.4-1.5X0.7

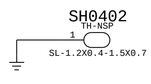


SH0401
TH-NSP
SL-1.2X0.4-1.5X0.7

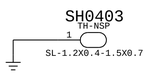


ATC01 BBR Shield Can APN: 806-27113

SH0402
TH-NSP
SL-1.2X0.4-1.5X0.7

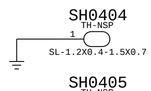


SH0403
TH-NSP
SL-1.2X0.4-1.5X0.7

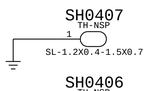


Left Viper Shield Can APN: 806-27111

SH0404
TH-NSP
SL-1.2X0.4-1.5X0.7

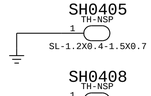


SH0407
TH-NSP
SL-1.2X0.4-1.5X0.7



Right Viper Shield Can APN: 806-27112

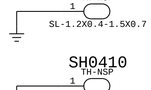
SH0405
TH-NSP
SL-1.2X0.4-1.5X0.7



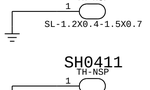
SH0406
TH-NSP
SL-1.2X0.4-1.5X0.7

Columbus Redriver Shield Can APN: 806-27436

SH0408
TH-NSP
SL-1.2X0.4-1.5X0.7

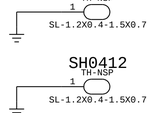


SH0409
TH-NSP
SL-1.2X0.4-1.5X0.7

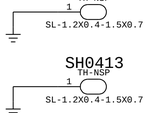


SD Card Shield Can APN: 806-28825

SH0410
TH-NSP
SL-1.2X0.4-1.5X0.7

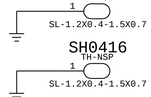


SH0411
TH-NSP
SL-1.2X0.4-1.5X0.7

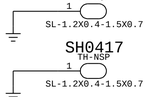


ATC2 BBR Shield Can APN: 806-27115

SH0412
TH-NSP
SL-1.2X0.4-1.5X0.7

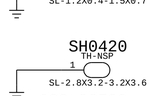


SH0413
TH-NSP
SL-1.2X0.4-1.5X0.7

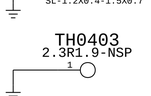


HDMI Madea Shield Can APN: 806-27117

SH0414
TH-NSP
SL-1.2X0.4-1.5X0.7



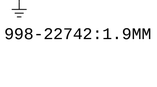
SH0415
TH-NSP
SL-1.2X0.4-1.5X0.7



Slave Maverick Shield Can APN: 806-27114

SH0416
TH-NSP
SL-1.2X0.4-1.5X0.7

SH0417
TH-NSP
SL-1.2X0.4-1.5X0.7

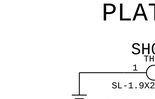


Iceman Shield Can APN: 806-29632

SH0420
TH-NSP
SL-2.8X3.2-3.2X3.6

998-22739

TH0403
2.3R1.9-NSP

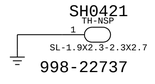


SoC Stiffener Charlie APN:806-29037

998-22742:1.9MM HOLE

PLATED SLOTS NEAR SOC

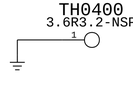
SH0421
TH-NSP
SL-1.9X2.3-2.3X2.7



998-22737

PLATED HOLES NEAR SOC

TH0400
3.6R3.2-NSP



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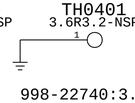
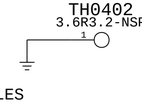
3.6R3.2-NSP



TH0402
3.6R3.2-NSP



998-22740:3.2MM HOLES

SYNC_MASTER=GAREN
SYNC_DATE=03/09/2020

PAGE TITLE
PD PARTS

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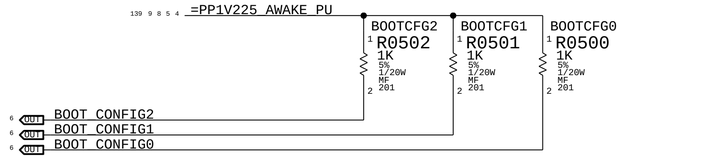
BOOT CONFIG

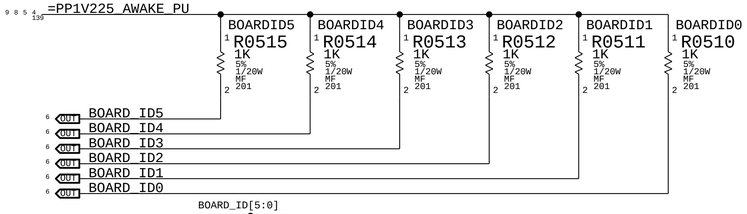


BOOT_CONFIGFG[2:0]	MODE
POR ---> 000	SPI1 NOR (12MHZ)
CURRENT SETTING (DEV) ---> 001	SPI1 NOR (12MHZ) TEST
010	SPI0 NAND (12MHZ)
011	SPI0 NAND (12MHZ) TEST
POR INVESTIGATION ---> 100	SPI1 NOR (40MHZ)
101	SPI1 NOR (40MHZ) TEST
110	SPI1 NOR (6MHZ)
111	SPI1 NOR (6MHZ) TEST

SW READ FLOW

1. SET GPIO AS INPUT
2. ENABLE IPD
3. WAIT 100 MILLISECONDS
4. READ VALUES
5. DISABLE GPIOS

BOARD ID

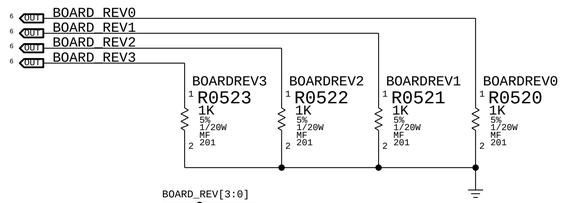


BOARD_ID[5:0]
000000 TEMP
000001 TEMP
000010 TEMP
000011 TEMP
000100 TEMP
000101 TEMP
000110 TEMP
000111 TEMP
001000 TEMP
001001 TEMP
001010 TEMP
001011 TEMP
001100 TEMP
001101 TEMP
001110 TEMP
001111 TEMP

HW READ FLOW

- HARDWARE SAMPLED BEFORE AP TAKEN OUT OF RESET
- SEE CHIPPADS INTEGRATION SPEC, SECTION 2.4.7

BOARD REV



BOARD_REV[3:0]
0000 TEMP
0001 TEMP
0010 TEMP
0011 TEMP
0100 TEMP
0101 TEMP
0110 TEMP
0111 TEMP
1000 TEMP
1001 TEMP
1010 TEMP
1011 TEMP
1100 TEMP
1101 TEMP
1110 TEMP
1111 TEMP

SW READ FLOW

- SAMPLED IN IBOOT ONCE AP IS RUNNING

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: CONFIG STRAPS

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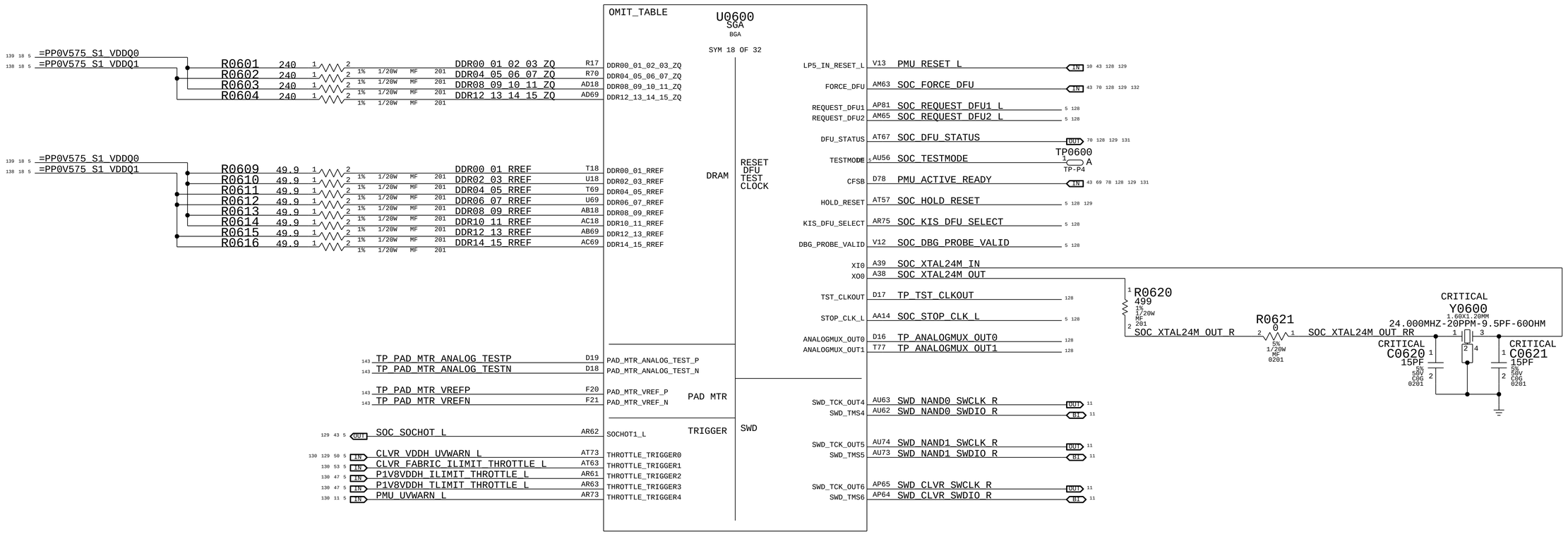

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: RESETS, CLOCKS, SWD

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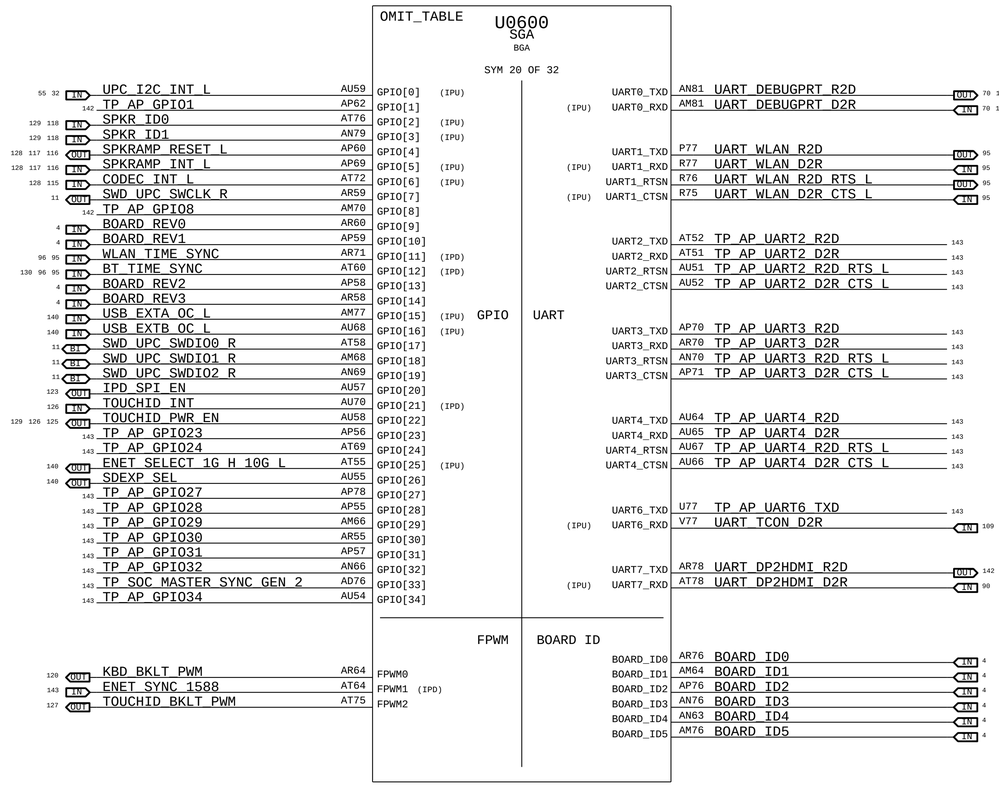

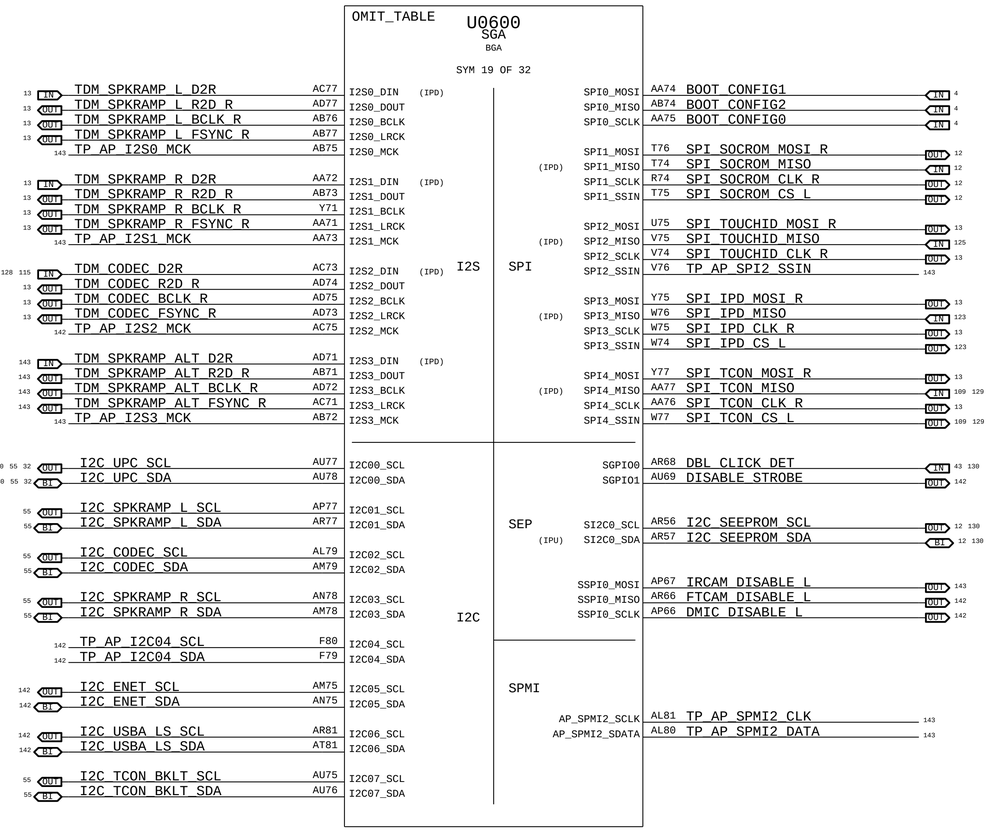

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GPIO, I2C, I2S, SPI, UART

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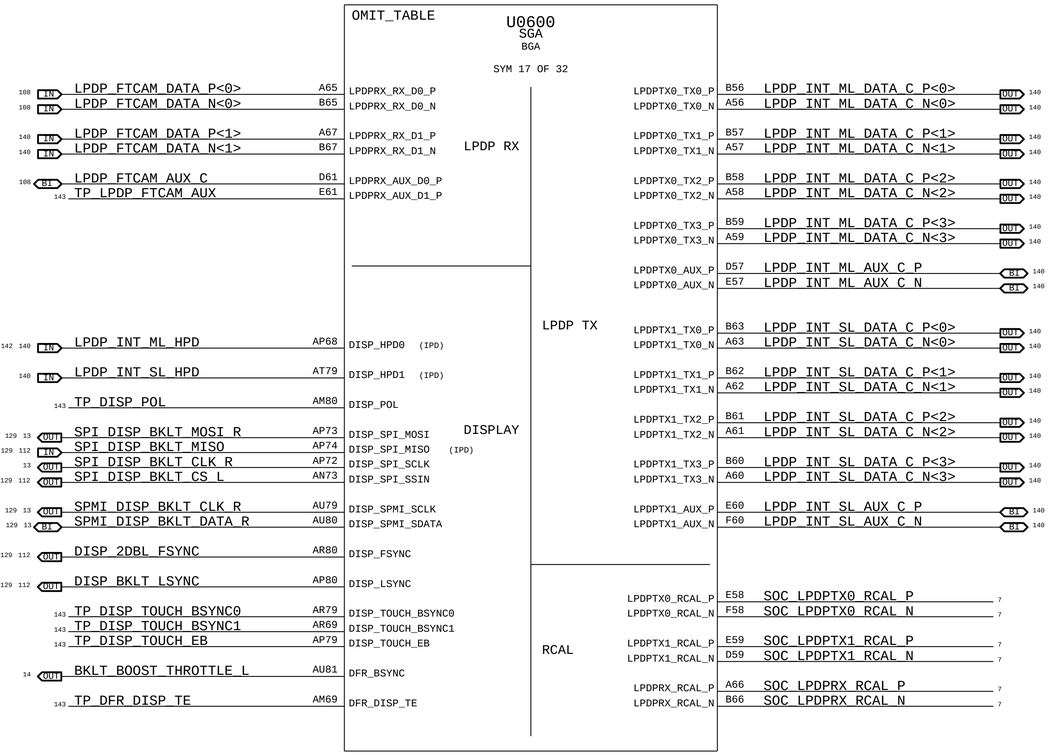

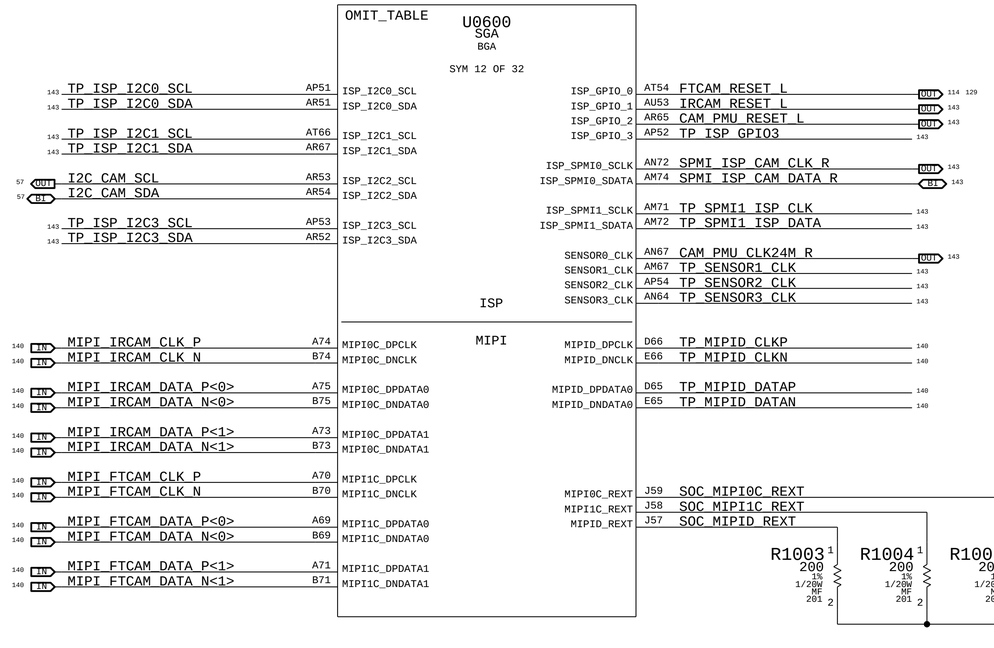

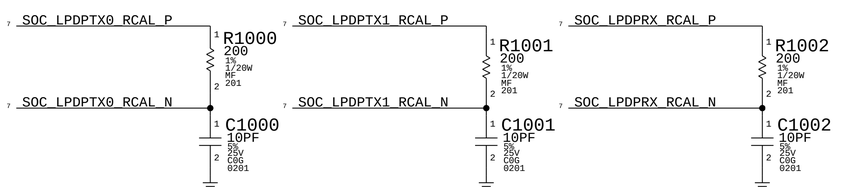

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PAGE TITLE: SOC: LPDP, ISP, MIPI

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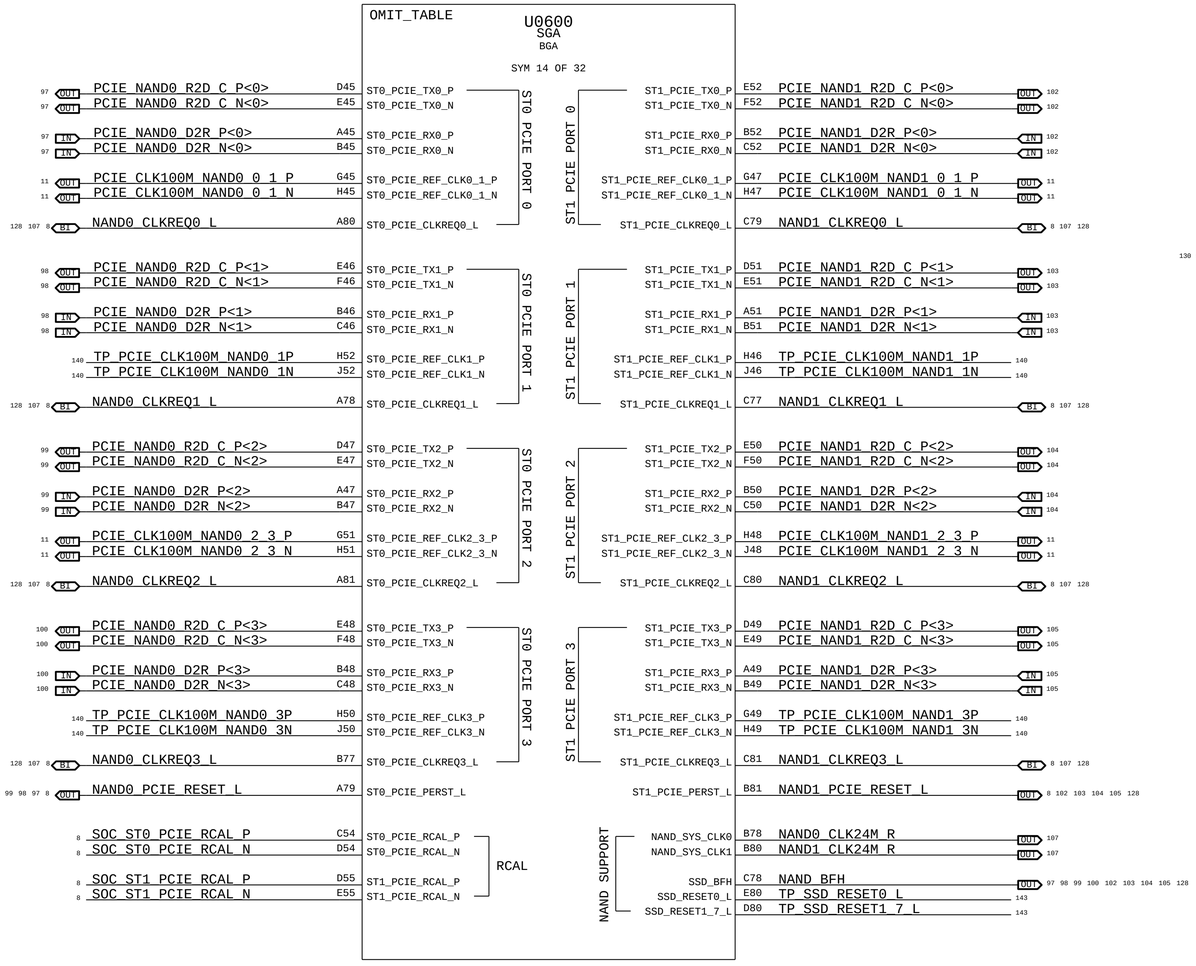

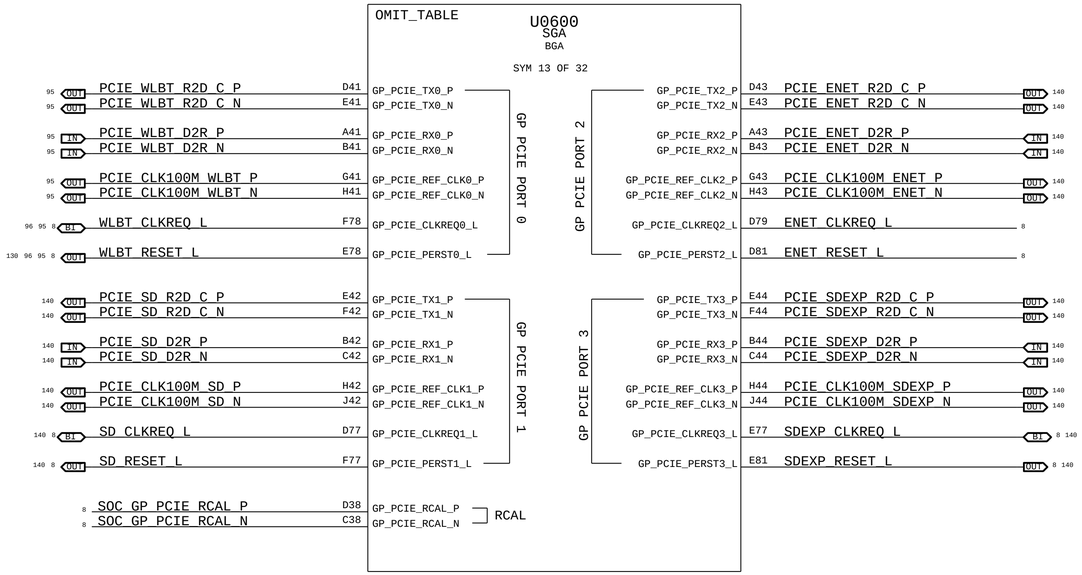

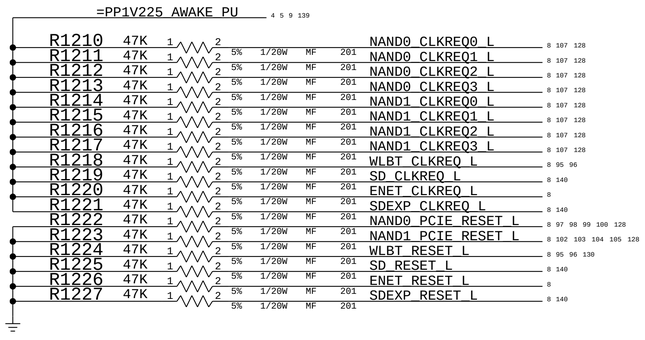

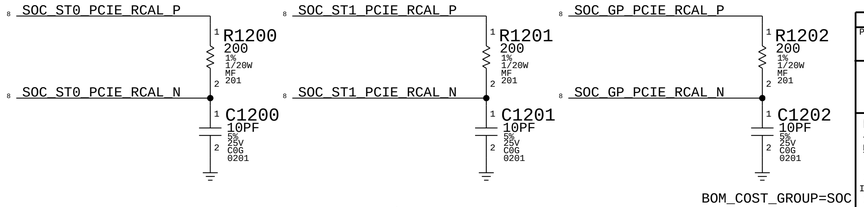

PAGE TITLE
SOC: PCIE

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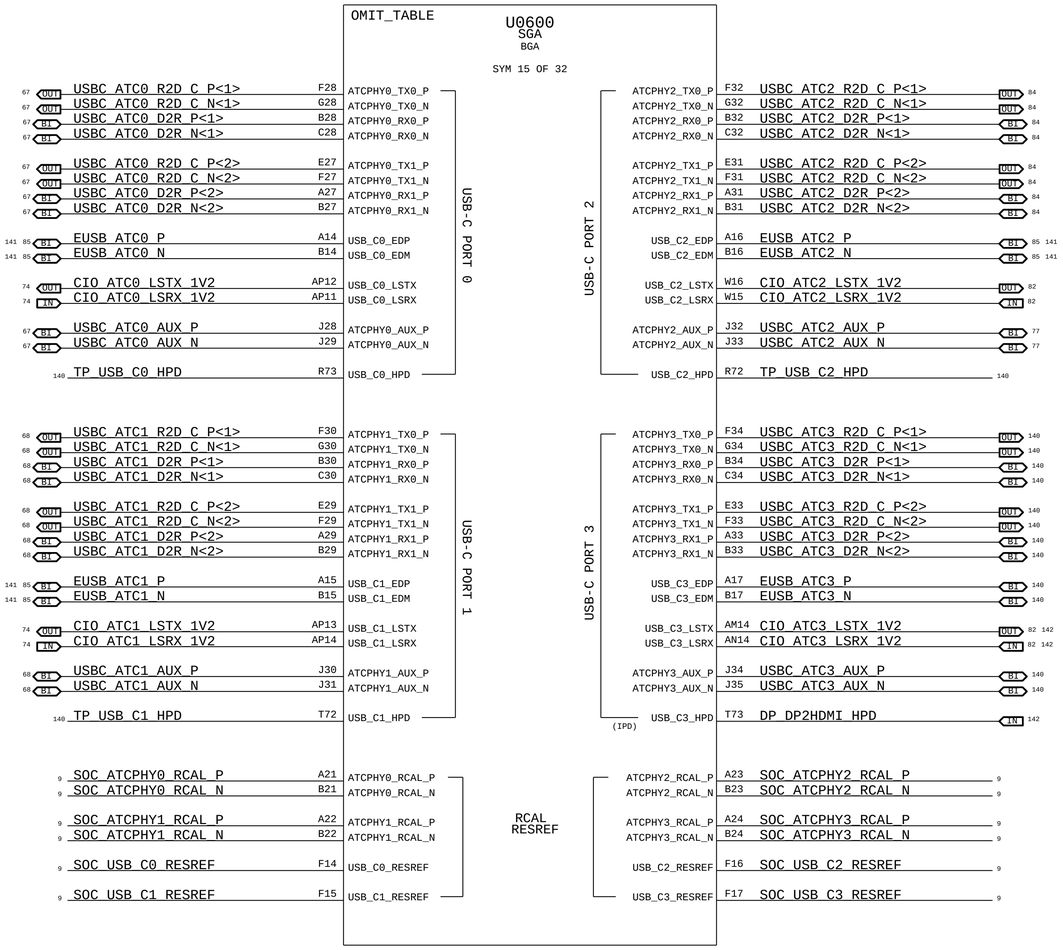

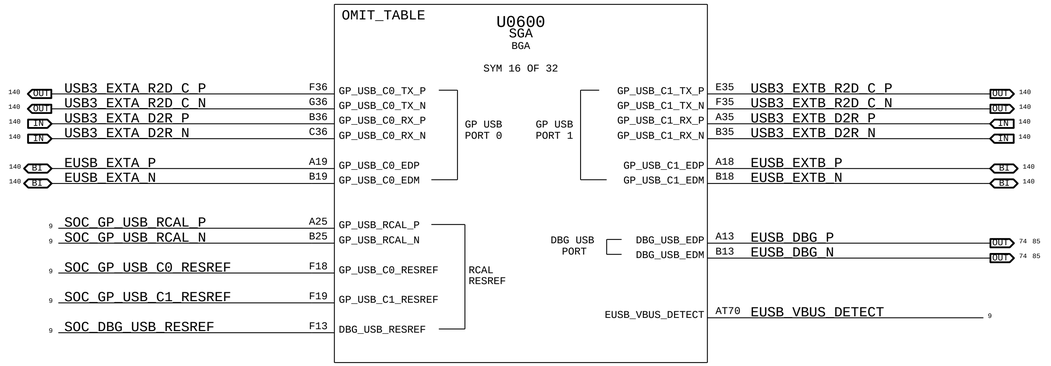

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R1412	0	5%	1/20W	MF	0201	EUSB_VBUS_DETECT	
R1400	200	1%	1/20W	MF	201	SOC_DBG_USB_RESREF	
R1401	200	1%	1/20W	MF	201	SOC_GP_USB_C1_RESREF	
R1402	200	1%	1/20W	MF	201	SOC_GP_USB_C0_RESREF	
R1403	200	1%	1/20W	MF	201	SOC_USB_C3_RESREF	
R1404	200	1%	1/20W	MF	201	SOC_USB_C2_RESREF	
R1405	200	1%	1/20W	MF	201	SOC_USB_C1_RESREF	
R1406	200	1%	1/20W	MF	201	SOC_USB_C0_RESREF	

SOC_ATCPHY0_RCAL_P	R1407	200	1%	1/20W	MF	201
SOC_ATCPHY0_RCAL_N	C1407	10PF	5%	25V	C0G	0201
SOC_ATCPHY1_RCAL_P	R1408	200	1%	1/20W	MF	201
SOC_ATCPHY1_RCAL_N	C1408	10PF	5%	25V	C0G	0201
SOC_ATCPHY2_RCAL_P	R1409	200	1%	1/20W	MF	201
SOC_ATCPHY2_RCAL_N	C1409	10PF	5%	25V	C0G	0201
SOC_ATCPHY3_RCAL_P	R1410	200	1%	1/20W	MF	201
SOC_ATCPHY3_RCAL_N	C1410	10PF	5%	25V	C0G	0201
SOC_GP_USB_RCAL_P	R1411	200	1%	1/20W	MF	201
SOC_GP_USB_RCAL_N	C1411	10PF	5%	25V	C0G	0201

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: CIO, USB

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OMIT_TABLE

U0600
SGA
BGA

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AOP GPIO

143	TP_AOP_GPIO0	AT8	AOP_FUNC[0]
143	TP_AOP_GPIO1	AT9	AOP_FUNC[1]
143	TP_AOP_GPIO2	AD14	AOP_FUNC[2]
143	TP_AOP_GPIO3	AR8	AOP_FUNC[3]
143	TP_AOP_GPIO4	AM7	AOP_FUNC[4]
143	TP_AOP_GPIO5	AR9	AOP_FUNC[5]
65 OUT	SPI_GYRO_CS_L	AA10	AOP_FUNC[6]
65 IN	GYRO_INT	AA11	AOP_FUNC[7]
65 IN	GYRO_MOTION_INT	AR10	AOP_FUNC[8]
114 IN	LID_OPEN	AA13	AOP_FUNC[9] (IPD)
113 OUT	SPI_LAS_CS_L	AB11	AOP_FUNC[10]
143 OUT	WLAN_CONTEXT_A	AT6	AOP_FUNC[11]
143 OUT	WLAN_CONTEXT_B	AD15	AOP_FUNC[12]
143 IN	IRCAM_PROX_INT_L	AM13	AOP_FUNC[13] (IPU)
128 114 IN	PDM_DMIC_DATA3	AD13	AOP_FUNC[14] (IPD)

AOP I2C

57 OUT	I2C_AOP_CAM_SCL	AU12	AOP_I2CM0_SCL
57 BI	I2C_AOP_CAM_SDA	AU11	AOP_I2CM0_SDA
143	TP_AOP_I2CM1_SCL	AU6	AOP_I2CM1_SCL
143	TP_AOP_I2CM1_SDA	AU7	AOP_I2CM1_SDA

AOP PDM

143	TP_PDM_DMIC_CLK1	AD10	AOP_PDM_IN_CLK1
143	TP_AOP_I2S0_MCK	AR12	AOP_PDM_IN_CLK2
143	TP_AOP_I2S0_LRCK	AT14	AOP_PDM_IN_CLK3
143	TP_AOP_I2S0_DOUT	AT12	AOP_PDM_IN_CLK4
143	TP_AOP_I2S0_DIN	AR13	AOP_PDM_IN_CLK5
143	TP_AOP_I2S0_BCLK	AR14	AOP_PDM_IN_CLK6
128 114 OUT	PDM_DMIC_CLK3	AD11	AOP_PDM_IN_CLK7
128 114 OUT	PDM_DMIC_CLK4	AB10	AOP_PDM_IN_CLK8
143	TP_PDM_DMIC_DATA1	AC10	AOP_PDM_IN_DATA1
128 114 IN	PDM_DMIC_DATA4	AB13	AOP_PDM_IN_DATA4 (IPD)

AOP SPI

13 OUT	SPI_AOP_SENSOR_MOSI_R	AU10	AOP_SPI0_MOSI
13 IN	SPI_AOP_SENSOR_MISO	AU9	AOP_SPI0_MISO (IPD)
13 OUT	SPI_AOP_SENSOR_SCLK_R	AU8	AOP_SPI0_SCLK

AOP SPMI

13 OUT	SPMI_WLBT_CLK_R	AA16	AOP_SPMI0_SCLK
13 BI	SPMI_WLBT_DATA_R	AB16	AOP_SPMI0_SDATA
13 OUT	SPMI_SE_CLK_R	AB14	AOP_SPMI1_SCLK
13 BI	SPMI_SE_DATA_R	AB15	AOP_SPMI1_SDATA

AOP UART

143	TP_AOP_UART2_R2D	AC12	AOP_UART2_TXD
143	TP_AOP_UART2_D2R	AD12	AOP_UART2_RXD

AON CLOCK RESETS WDOG

128 44 IN	PMU_CLK32K_SOC	AM8	RT_CLK32768
		T12	CFSB_AON
129 128 43 5 IN	PMU_RESET_L	T13	COLD_RESETN
130	TP_AON_SLEEP1_RESET_L	AU50	AON_SLEEP1_RESETN
43 10 OUT	SOC_WDOG_L	T11	WDOG_L

SMC GPIO

130 56 IN	UPC_SMC_I2C_INT_L	E7	SMC_GPIO0 (IPU)
143	TP_SMC_GPIO1	C6	SMC_GPIO1
143	TP_SMC_GPIO2	AB12	SMC_GPIO2
143	TP_SMC_GPIO3	D6	SMC_GPIO3
143	TP_SMC_GPIO4	C7	SMC_GPIO4
143	TP_SMC_GPIO5	V10	SMC_GPIO5
143 OUT	ACDC_BURST_EN_L	D8	SMC_GPIO6
143 IN	ACDC_ID	AA12	SMC_GPIO7
143	PSU_TBD3	Y12	SMC_GPIO8
142 IN	CHGR_INT_L_PSU_TBD4	A7	SMC_GPIO9

SMC UART

129 70 OUT	UART_SMC_DEBUGPRT_R2D	AA15	SMC_UART0_TXD
129 70 IN	UART_SMC_DEBUGPRT_D2R	Y14	SMC_UART0_RXD (IPD)

NUB GPIO

V16	TP_NUB_CLK_OUT0	143	NUB_CLK_OUT0
U16	TP_SOC_DOCK_ATTENTION	128	NUB_DOCK_ATTENTION
W11	SOC_DOCK_CONNECT	IN 10 128 134	NUB_DOCK_CONNECT
B7	TP_NUB_CLK_OUT1	143	NUB_GPIO[0]
R10	CODEC_RESET_L	OUT 115 128	NUB_GPIO[1]
W13	SOC_SW_DBG	OUT 131	NUB_GPIO[2]
E6	IPD_SPI_INT_L_ENET_LOW_PWR	IN 142	NUB_GPIO[3] (IPU)
E9	SMC_FIXTURE_MODE_L	IN 128 129	NUB_GPIO[4] (IPU)
Y16	PARROT_RESET_L	OUT 140 142	NUB_GPIO[5]
AC14	PARROT_INT_L	IN 140	NUB_GPIO[6] (IPU)
P16	TITUS_B2B_DETECT_L	IN 143	NUB_GPIO[7] (IPU)
U10	ALS_INT_L	IN 108 129	NUB_GPIO[8] (IPU)
D7	SPI_DP2HDMI_HOLD_L	OUT 89	NUB_GPIO[9]
T10	HDMI_CEC_AOP_TX	OUT 89 129	NUB_GPIO[10]
A8	HDMI_CEC_AOP_RX	IN 89 129	NUB_GPIO[11]
V11	HDMI_HPD_AOP	IN 89 130	NUB_GPIO[12] (IPU)

NUB SPMI

E10	SPMI_NUB_MPMU_CLK_R	OUT 11 13	NUB_SPMI0_SCLK
D10	SPMI_NUB_MPMU_DATA_R	BI 11 13	NUB_SPMI0_SDATA
D9	SPMI_NUB_SPMU_P1V8VDDH_CLK_R	OUT 11 13	NUB_SPMI1_SCLK
C10	SPMI_NUB_SPMU_P1V8VDDH_DATA_R	BI 11 13	NUB_SPMI1_SDATA

NUB SWD

A10	SWD_NUB_PMU_SWCLK_R	OUT 11	NUB_SWD_TCK_OUT0
A11	SWD_NUB_PMU_SWDIO_R	BI 11	NUB_SWD_TMS0
C8	SWD_NUB_CLVR_SWCLK_R	OUT 11	NUB_SWD_TCK_OUT1
C9	SWD_NUB_CLVR_SWDIO_R	BI 11	NUB_SWD_TMS1
B9	TP_NUB_SWD_TCK_OUT2	143	NUB_SWD_TCK_OUT2
B10	TP_NUB_SWD_TMS2	143	NUB_SWD_TMS2
A9	TP_NUB_SWD_TMS3	143	NUB_SWD_TMS3

NUB JTAG

AM12	SWD_SOC_SWCLK_R	IN 11	JTAG_TCK
AM9	SWD_SOC_SWDIO_R	BI 11	JTAG_TMS
AM10	TP_JTAG_SOC_TDI	128 144	JTAG_TDI
AN12	TP_JTAG_SOC_TDO	128 144	JTAG_TDO
AM11	TP_JTAG_SOC_TRST_L	128	JTAG_TRSTN
AP8	SOC_JTAG_SEL (DAP=0, TAP=1)	IN 10 128	JTAG_SEL
Y10	TP_NUB_JTAG_SLV_TCK	143	JTAG_SLV_TCK
W14	TP_NUB_JTAG_SLV_TMS	143	JTAG_SLV_TMS
U12	TP_NUB_JTAG_SLV_TDI	143	JTAG_SLV_TDI
AR11	TP_NUB_JTAG_SLV_TDO	143	JTAG_SLV_TDO
AN8	TP_NUB_JTAG_SLV_TRSTN	143	JTAG_SLV_TRSTN

SMC I2C

T14	I2C_SMC_PWR_SCL	OUT 56 129	SMC_I2CM0_SCL
U14	I2C_SMC_PWR_SDA	BI 56 129	SMC_I2CM0_SDA
T16	I2C_SMC_UPC_SCL	OUT 32 56 129 130	SMC_I2CM1_SCL
T15	I2C_SMC_UPC_SDA	BI 32 56 129 130	SMC_I2CM1_SDA
R12	I2C_SMC_NAND_SCL	OUT 56 130	SMC_I2CM2_SCL
R11	I2C_SMC_NAND_SDA	BI 56 130	SMC_I2CM2_SDA
R13	I2C_SMC_IPD_SCL	OUT 57 129	SMC_I2CM3_SCL
R14	I2C_SMC_IPD_SDA	BI 57 129	SMC_I2CM3_SDA
R16	I2C_SMC_SNS0_SCL	OUT 57	SMC_I2CM4_SCL
R15	I2C_SMC_SNS0_SDA	BI 57	SMC_I2CM4_SDA
AC16	I2C_SMC_SNS1_SCL	OUT 142	SMC_I2CM5_SCL
AD16	I2C_SMC_SNS1_SDA	BI 142	SMC_I2CM5_SDA
A6	TP_SMC_I2CM6_SCL	143	SMC_I2CM6_SCL
B6	TP_SMC_I2CM6_SDA	143	SMC_I2CM6_SDA

SMC FPWM

AN11	SMC_FAN_0_PWM	OUT 66	SMC_FPWM0
AP10	SMC_FAN_0_TACH	IN 66	SMC_FPWM1
AP9	SMC_FAN_1_PWM	OUT 66	SMC_FPWM2
AN9	SMC_FAN_1_TACH	IN 66	SMC_FPWM3

=PP1V2_S2_PU 5 138

R1600	10K	5%	1/20W	MF	201	SOC_WDOG_L	10 43
R1601	47K	5%	1/20W	MF	201	SOC_DOCK_CONNECT	10 128 134
R1602	10K	5%	1/20W	MF	201	SOC_JTAG_SEL	10 128

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: AOP, SMC, NUB

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IN PROGRESS

SPMI SOURCE TERMINATION

5 IN	SPMI_CLVR0_CLK_R	PLACE_NEAR=U0600.Y73:16MM	R1914	33	1	2	5% 1/20W MF 201	SPMI_CLVR0_CLK	OUT	50
5 BI	SPMI_CLVR0_DATA_R	PLACE_NEAR=U0600.W73:16MM	R1915	33	1	2	5% 1/20W MF 201	SPMI_CLVR0_DATA	BI	50
5 IN	SPMI_CLVR1_CLK_R	PLACE_NEAR=U0600.V73:16MM	R1916	33	1	2	5% 1/20W MF 201	SPMI_CLVR1_CLK	OUT	51
5 BI	SPMI_CLVR1_DATA_R	PLACE_NEAR=U0600.U71:18MM	R1917	33	1	2	5% 1/20W MF 201	SPMI_CLVR1_DATA	BI	51
5 IN	SPMI_CLVR2_CLK_R	PLACE_NEAR=U0600.U71:18MM	R1918	33	1	2	5% 1/20W MF 201	SPMI_CLVR4_CLK	OUT	52
5 BI	SPMI_CLVR2_DATA_R	PLACE_NEAR=U0600.T71:18.1MM	R1919	33	1	2	5% 1/20W MF 201	SPMI_CLVR4_DATA	BI	52

NAND PCIE CLK BRANCH RESISTORS

8 IN	PCIE_CLK100M_NAND0_0_1_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_0_P	OUT	97 107
			PCIE_CLK100M_NAND0_1_P	OUT	98
8 IN	PCIE_CLK100M_NAND0_0_1_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_0_N	OUT	97 107
			PCIE_CLK100M_NAND0_1_N	OUT	98
8 IN	PCIE_CLK100M_NAND0_2_3_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_2_P	OUT	99 107
			PCIE_CLK100M_NAND0_3_P	OUT	100
8 IN	PCIE_CLK100M_NAND0_2_3_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND0_2_N	OUT	99 107
			PCIE_CLK100M_NAND0_3_N	OUT	100
8 IN	PCIE_CLK100M_NAND1_0_1_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_0_P	OUT	102 107
			PCIE_CLK100M_NAND1_1_P	OUT	103
8 IN	PCIE_CLK100M_NAND1_0_1_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_0_N	OUT	102 107
			PCIE_CLK100M_NAND1_1_N	OUT	103
8 IN	PCIE_CLK100M_NAND1_2_3_P	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_2_P	OUT	104 107
			PCIE_CLK100M_NAND1_3_P	OUT	105
8 IN	PCIE_CLK100M_NAND1_2_3_N	MAKE_BASE=TRUE	PCIE_CLK100M_NAND1_2_N	OUT	104 107
			PCIE_CLK100M_NAND1_3_N	OUT	105

SWD SERIES RESISTORS

5 IN	SWD_CLVR_SWCLK_R	R1936	PLACE_NEAR=U0600.AP65:11MM	15	SWD_CLVR_SWCLK	R1920	49.9	1% 1/20W MF 201	SWD_CLVR0_SWCLK	OUT	50
						R1921	49.9	1% 1/20W MF 201	SWD_CLVR1_SWCLK	OUT	51
5 BI	SWD_CLVR_SWDIO_R	R1937	PLACE_NEAR=U0600.AP64:10MM	15	SWD_CLVR_SWDIO	R1922	49.9	1% 1/20W MF 201	SWD_CLVR0_SWDIO	BI	50
						R1923	49.9	1% 1/20W MF 201	SWD_CLVR1_SWDIO	BI	51
5 IN	SWD_NAND0_SWCLK_R	R1932	PLACE_NEAR=U0600.AU63:10MM	15 128	SWD_NAND0_SWCLK	R1985	49.9	1% 1/20W MF 201	SWD_NAND0_S5E0_S5E1_SWCLK	OUT	140
						R1986	49.9	1% 1/20W MF 201	SWD_NAND0_S5E2_S5E3_SWCLK	OUT	140
5 BI	SWD_NAND0_SWDIO_R	R1933	PLACE_NEAR=U0600.AU62:10MM	15 128	SWD_NAND0_SWDIO	R1987	15	5% 1/20W MF 201	SWD_NAND0_S5E0_S5E1_SWDIO	BI	140
						R1988	15	5% 1/20W MF 201	SWD_NAND0_S5E2_S5E3_SWDIO	BI	140
5 IN	SWD_NAND1_SWCLK_R	R1934	PLACE_NEAR=U0600.AU74:10MM	15 128	SWD_NAND1_SWCLK	R1989	49.9	1% 1/20W MF 201	SWD_NAND1_S5E0_S5E1_SWCLK	OUT	140
						R1990	49.9	1% 1/20W MF 201	SWD_NAND1_S5E2_S5E3_SWCLK	OUT	140
5 BI	SWD_NAND1_SWDIO_R	R1935	PLACE_NEAR=U0600.AU73:10MM	15 128	SWD_NAND1_SWDIO	R1991	15	5% 1/20W MF 201	SWD_NAND1_S5E0_S5E1_SWDIO	BI	140
						R1992	15	5% 1/20W MF 201	SWD_NAND1_S5E2_S5E3_SWDIO	BI	140

10 OUT	SWD_SOC_SWCLK_R	PLACE_NEAR=U0600.AM12:10MM	R1938	0	5% 1/20W MF 0201	SWD_SOC_SWCLK	IN	70 128 129
10 BI	SWD_SOC_SWDIO_R	PLACE_NEAR=U0600.AM9:10MM	R1939	0	5% 1/20W MF 0201	SWD_SOC_SWDIO	BI	70 128 129
10 IN	SWD_NUB_PMU_SWCLK_R	PLACE_NEAR=U0600.A10:10MM	R1942	15	5% 1/20W MF 201	SWD_NUB_PMU_SWCLK	OUT	13 130
10 BI	SWD_NUB_PMU_SWDIO_R	PLACE_NEAR=U0600.A11:10MM	R1943	15	5% 1/20W MF 201	SWD_NUB_PMU_SWDIO	BI	13 130
6 IN	SWD_UPC_SWCLK_R		R1946	49.9	1% 1/20W MF 201	SWD_UPC_SWCLK0	OUT	78
			R1993	49.9	1% 1/20W MF 201	SWD_UPC_SWCLK1	OUT	32 69 130
6 BI	SWD_UPC_SWDIO0_R	PLACE_NEAR=U0600.AT58:15MM	R1947	0	5% 1/20W MF 0201	SWD_UPC_SWDIO0	BI	69
6 BI	SWD_UPC_SWDIO1_R	PLACE_NEAR=U0600.AM68:15MM	R1948	0	5% 1/20W MF 0201	SWD_UPC_SWDIO1	BI	78
6 BI	SWD_UPC_SWDIO2_R	PLACE_NEAR=U0600.AN69:15MM	R1949	0	5% 1/20W MF 0201	SWD_UPC_SWDIO2	BI	32
140 BI	SWD_UPC_SWDIO3_R	PLACE_NEAR=U0600.AU68:15MM	R1950	0	5% 1/20W MF 0201	SWD_UPC_SWDIO3	BI	69 130

10 IN	SWD_NUB_CLVR_SWCLK_R	PLACE_NEAR=U0600.C8:10MM	R1982	33	5% 1/20W MF 201	SWD_CLVR4_SWCLK	OUT	52
10 BI	SWD_NUB_CLVR_SWDIO_R	PLACE_NEAR=U0600.C9:10MM	R1983	33	5% 1/20W MF 201	SWD_CLVR4_SWDIO	BI	52

VDD/VSS SENSE BREAKOUT PADS

15 IN	VSNS_PVDDGPU0AWAKESW_SENSE	PLACE_NEAR=U0600.AG28:25.4MM FUNC_TEST=TRUE	TP1900	1 A	TP-P4	16 IN	VSNS_PVDDDISP_SENSE	PLACE_NEAR=U0600.N57:25.4MM FUNC_TEST=TRUE	TP1906	1 A	TP-P4
25 IN	VSNS_PVSSGPU0AWAKESW_SENSE	PLACE_NEAR=TP1900.1:1MM	TP1901	1 A	TP-P4	25 IN	VSNS_PVSSDISP_SENSE	PLACE_NEAR=TP1906.1:1MM	TP1907	1 A	TP-P4
15 IN	VSNS_PVDDPCPU0AWAKESW_SENSE	PLACE_NEAR=U0600.T26:25.4MM FUNC_TEST=TRUE	TP1902	1 A	TP-P4	22 IN	VSNS_PVDD2H0S2SW_SENSE1	PLACE_NEAR=U0600.H14:25.4MM FUNC_TEST=TRUE	TP1908	1 A	TP-P4
25 IN	VSNS_PVSSPCPU0AWAKESW_SENSE	PLACE_NEAR=TP1902.1:1MM	TP1903	1 A	TP-P4	25 IN	VSNS_PVSS2H0S2SW_SENSE1	PLACE_NEAR=TP1908.1:1MM	TP1909	1 A	TP-P4
18 IN	VSNS_P0V575VDDQ0_SENSE	PLACE_NEAR=U0600.AA29:25.4MM FUNC_TEST=TRUE	TP1904	1 A	TP-P4	23 IN	VSNS_PVDD2H1S2SW_SENSE2	PLACE_NEAR=U0600.H73:25.4MM FUNC_TEST=TRUE	TP1910	1 A	TP-P4
25 IN	VSNS_P0V575VSSQ0_SENSE	PLACE_NEAR=TP1904.1:1MM	TP1905	1 A	TP-P4	25 IN	VSNS_PVSS2H1S2SW_SENSE2	PLACE_NEAR=TP1910.1:1MM	TP1911	1 A	TP-P4

SPMI_NUB DAMPING FILTERS

13 10 SPMI_NUB_MPMU_CLK_R
13 10 SPMI_NUB_MPMU_DATA_R
13 10 SPMI_NUB_SPMU_P1V8VDDH_CLK_R
13 10 SPMI_NUB_SPMU_P1V8VDDH_DATA_R

NOSTUFF	C1900	10PF	5% 25V C0G 0201	1 2	
NOSTUFF	C1901	10PF	5% 25V C0G 0201	1 2	
NOSTUFF	C1902	10PF	5% 25V C0G 0201	1 2	
NOSTUFF	C1903	10PF	5% 25V C0G 0201	1 2	

130 5 OUT	PMU_UVWARN_L	R198B	909	1% 1/20W MF 201	P3V8AON_ILIMIT_L	IN	35
		R1980	430	1% 1/20W MF 201	PMU_VDDMAIN_UVWARN_L	IN	43 130
		R1981	0	5% 1/20W MF 201	PMU_VDDHI_UVWARN_L	IN	43 130
		R198A	220	5% 1/20W MF 0201	=PVBAT_ILIMIT_L_P12VAON_PLIMIT_L	IN	43 44

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SYNC_MASTER=BH00K SYNC_DATE=09/18/2020

PAGE TITLE

SOC: SHARED SUPPORT

Apple Inc.

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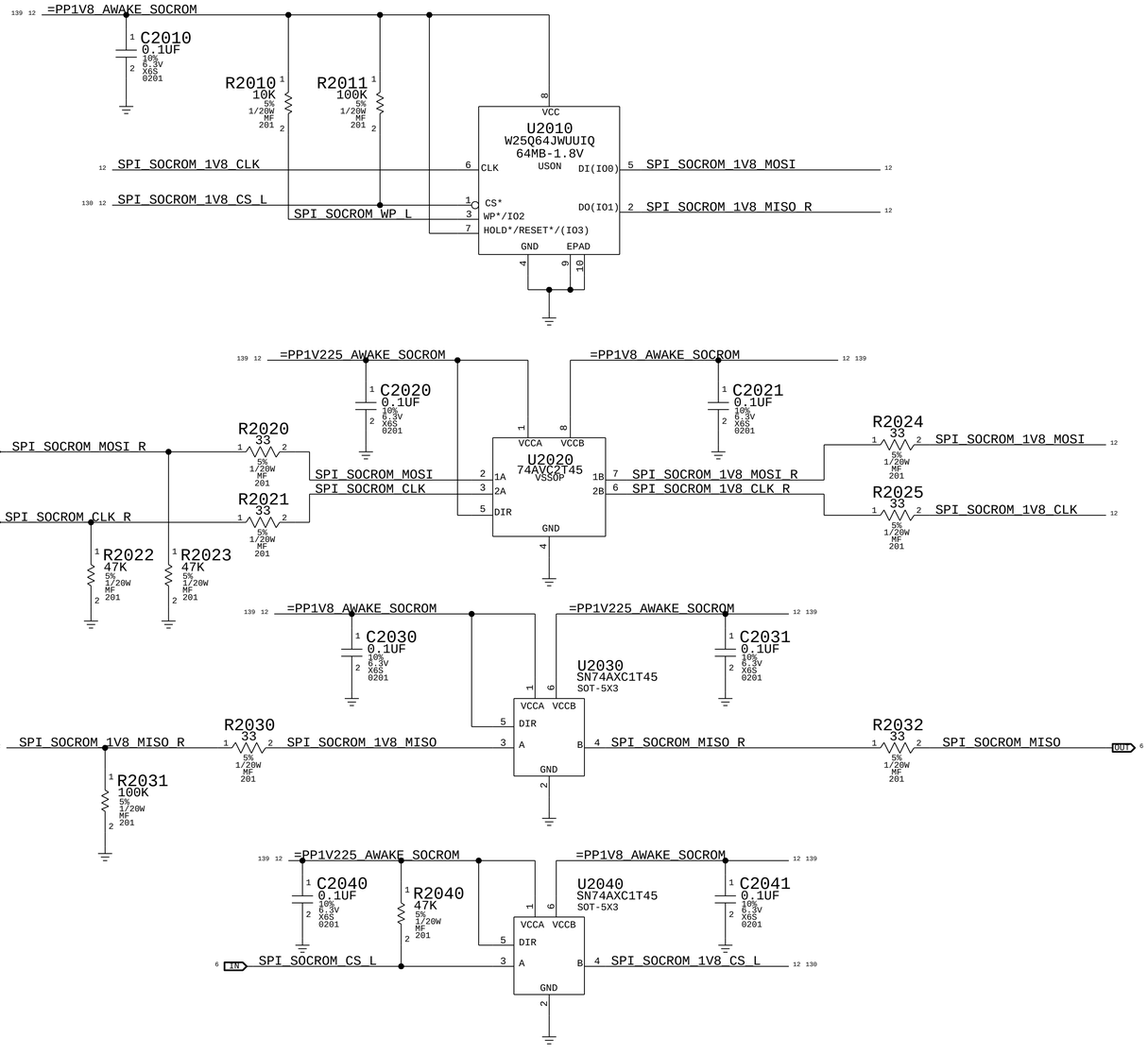
SPI NOR (1.8V 64MBIT)

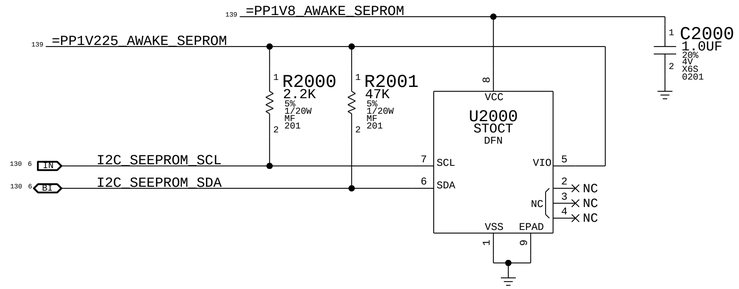
APN:335S00494



SEP EEPROM (16KBIT)

(Write: 0xA2, Read 0xA3)

APN:335S00488



BOM_COST_GROUP=SOC

PAGE TITLE: SOC: SPI NOR & SEP ROM

Apple Inc.

DRAWING NUMBER: 051-05641 SIZE: D

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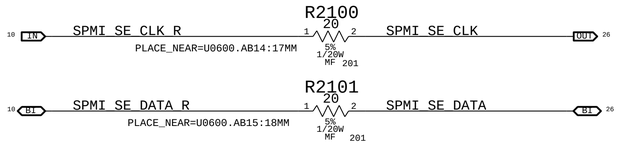
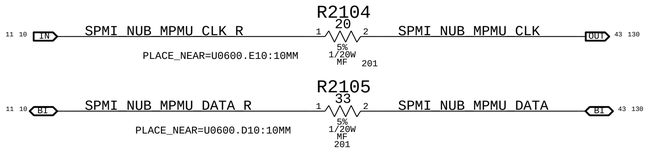
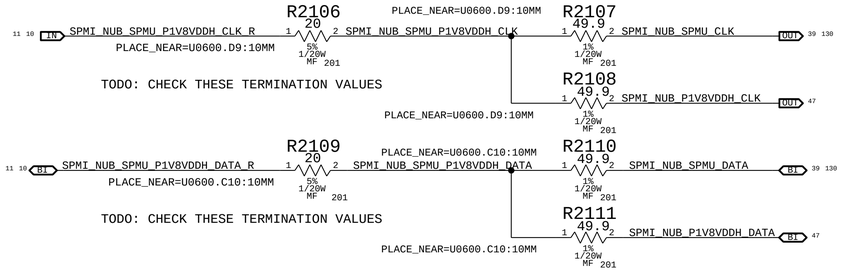
SGA SPMI SE SOURCE TERMINATIONS



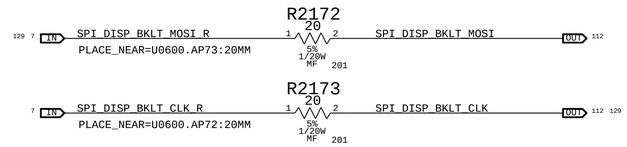
SGA SPMI MPMU SOURCE TERMINATIONS



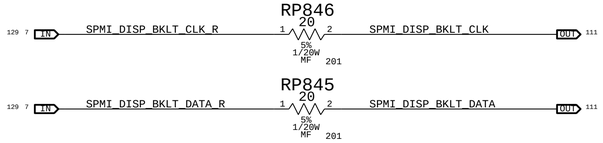
SGA SPMI SPMU SOURCE TERMINATIONS



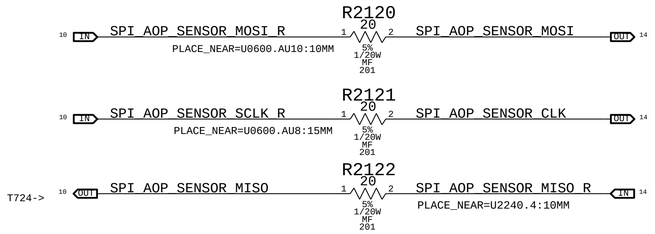
SGA SPI BKLT SOURCE TERMINATIONS



LUXE SPMI SOURCE TERMINATIONS



SGA SPI SENSOR SOURCE TERMINATIONS



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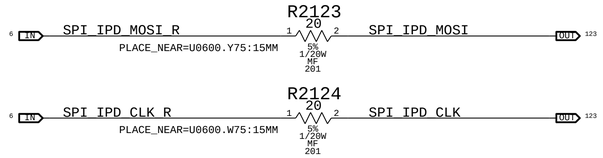

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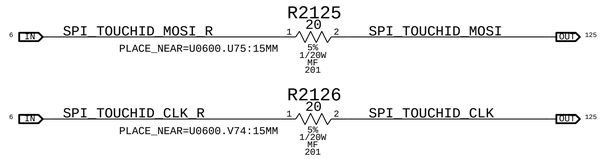

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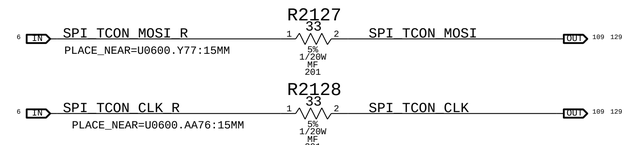
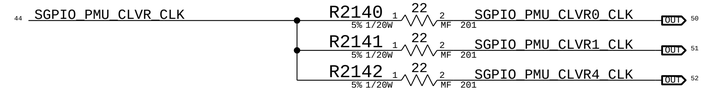
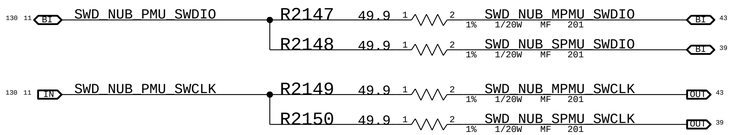
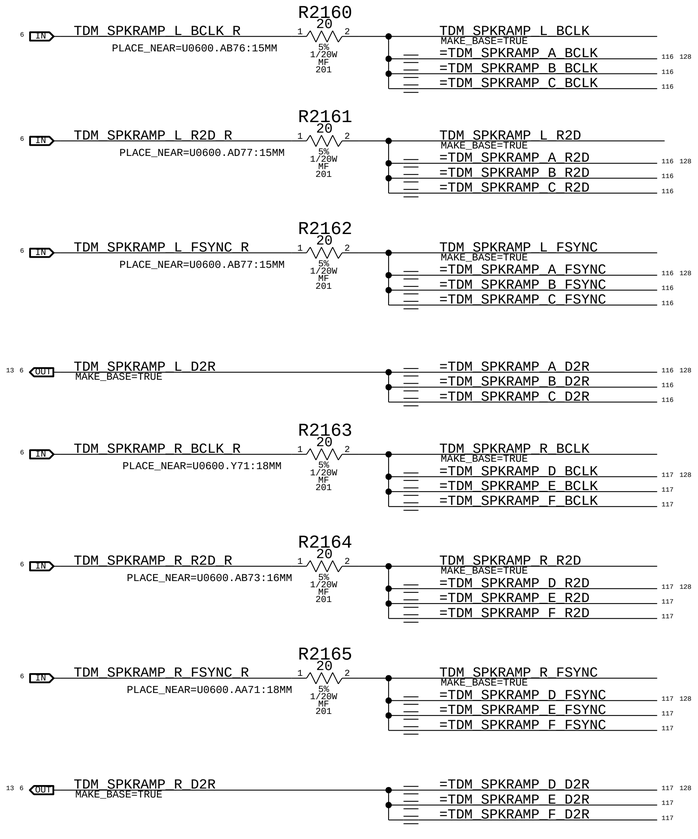
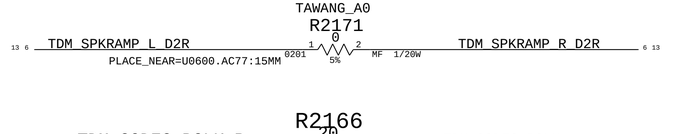






SGA TDM SOURCE TERMINATIONS





BOM_COST_GROUP=SOC

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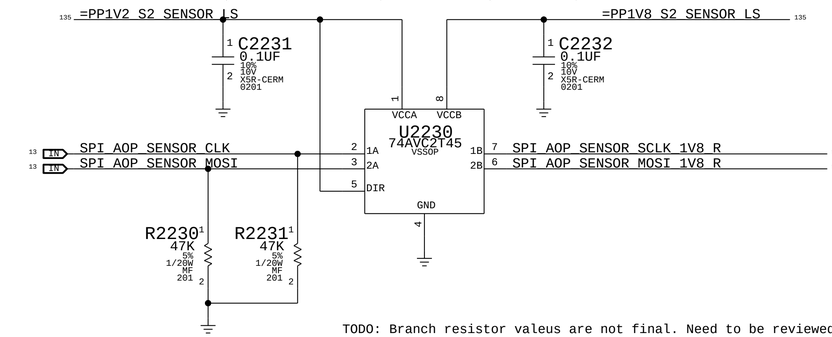
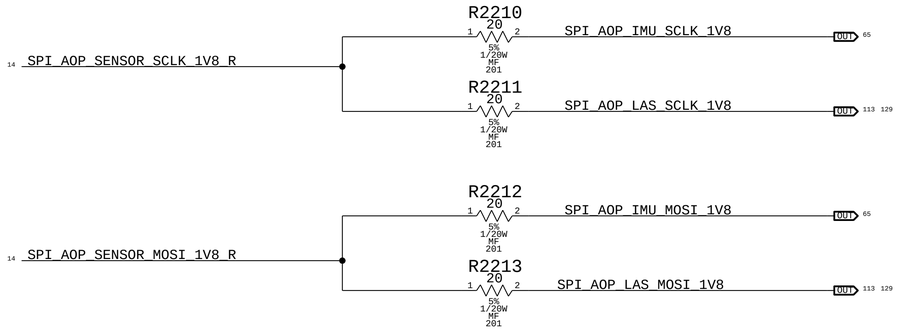
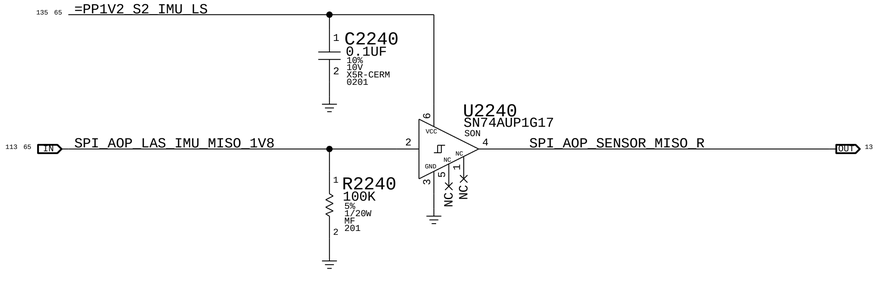
SPI AOP Sensor LS and Branch Resistors

TODO: Reference designators need to be updated once layout has imported latest netlist

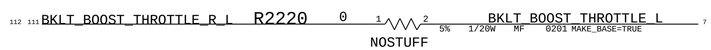


TODO: Branch resistor valeus are not final. Need to be reviewed by SI once routed

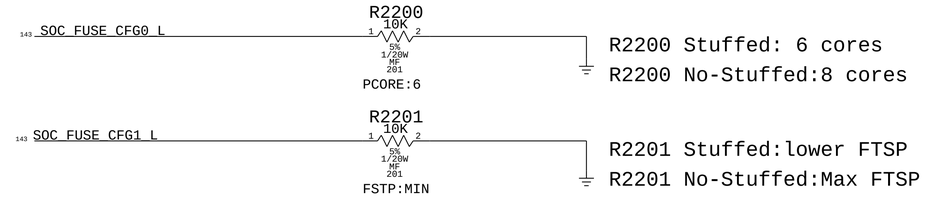




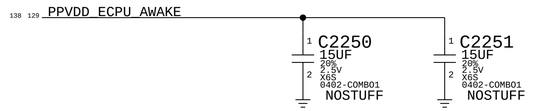
DISPLAY BACKLIGHT



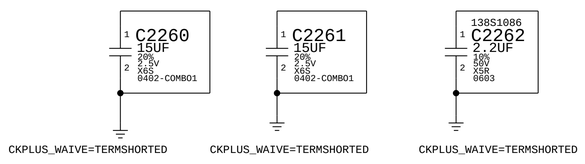
SoC POWER BINNING RESISTORS



rdar//73623710 Marginal PM on PPVDD_ECPU_AWAKE



rdar//73770219 Add Dummy Caps for DFM



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Apple Inc.	DRAWING NUMBER 051-05641 · SIZE D
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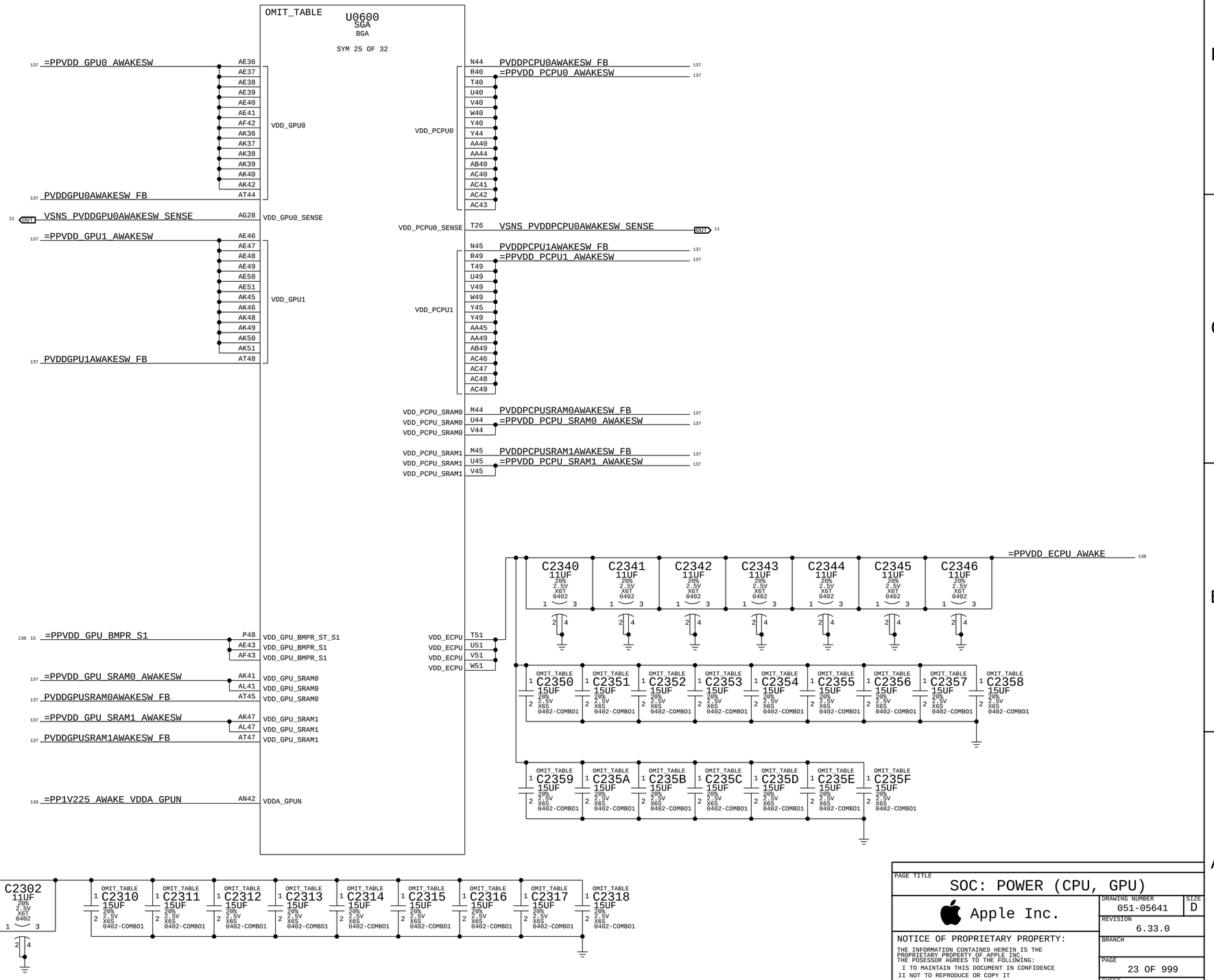

PAGE TITLE
SOC: POWER (CPU, GPU)

Apple Inc.

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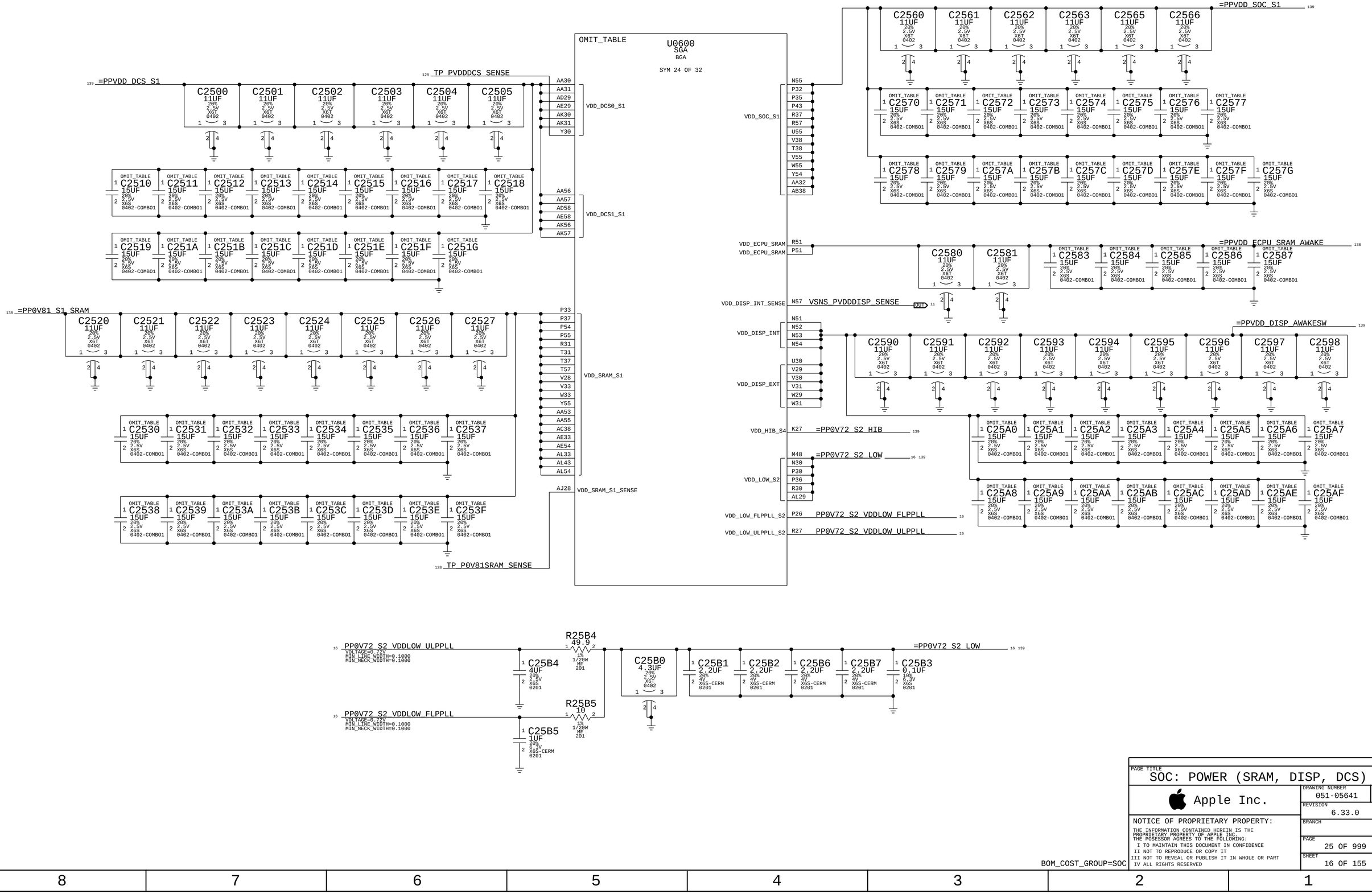

PAGE TITLE
SOC: POWER (SRAM, DISP, DCS)

Apple Inc.

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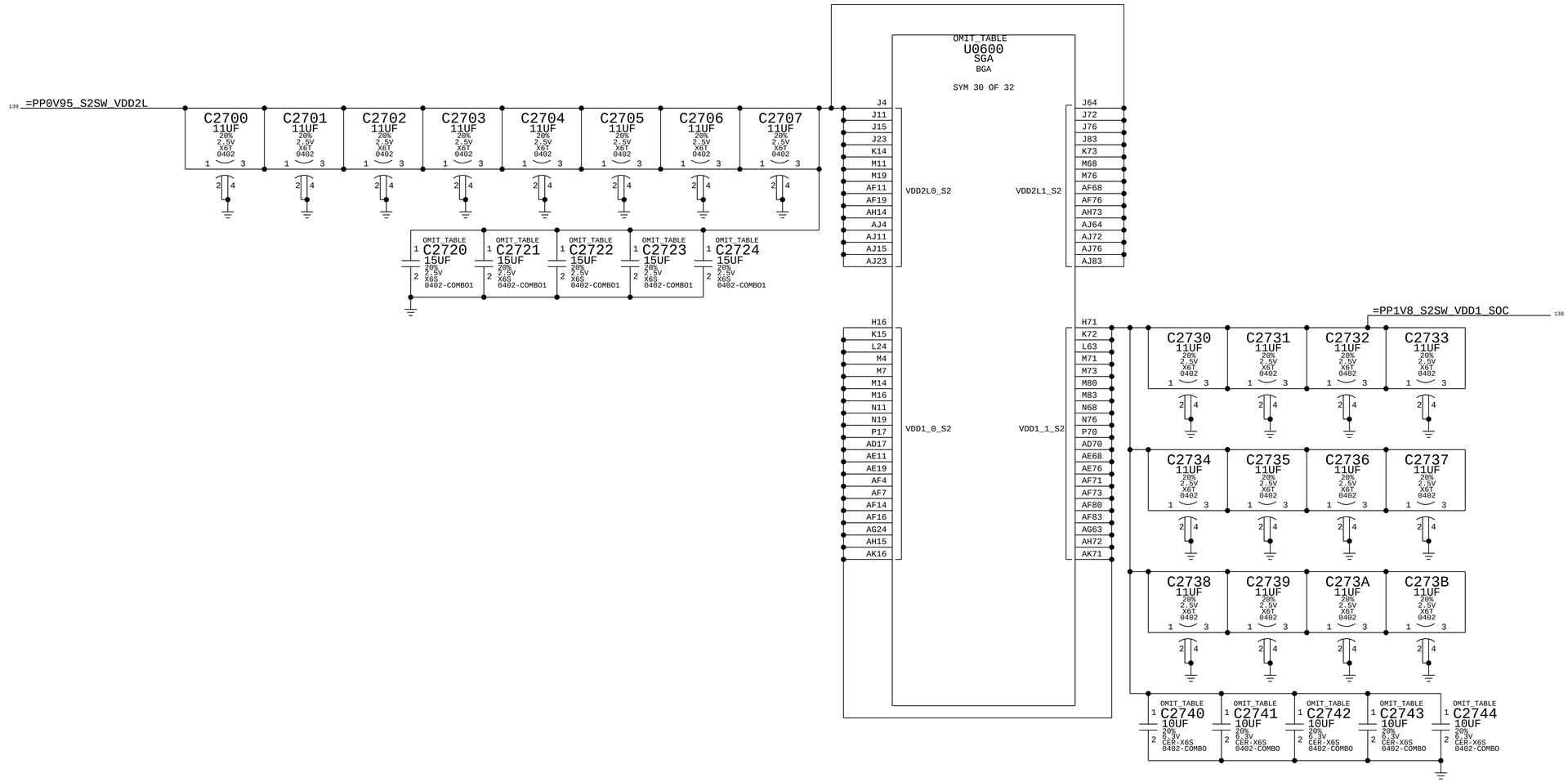
BOM_COST_GROUP=SOC



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PAGE TITLE
SOC: POWER (VDD1, VDD2)

Apple Inc.

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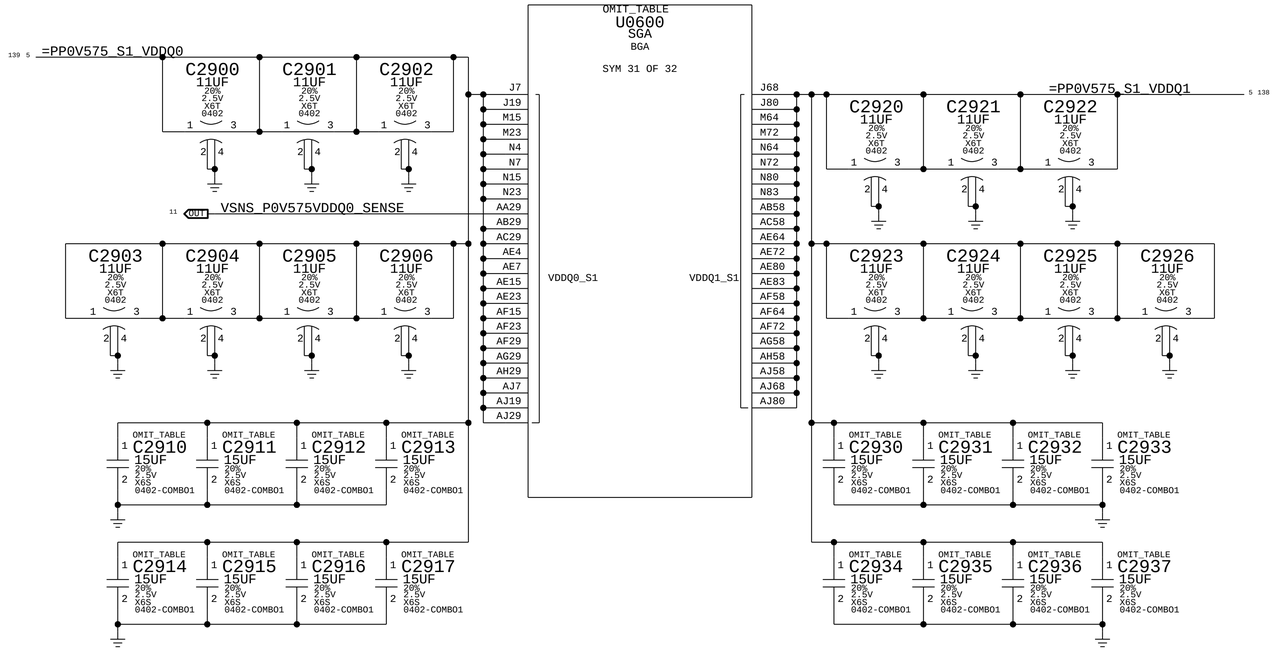

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDDQ)

Apple Inc.

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BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (AFR, ANE, CIO)

Apple Inc.

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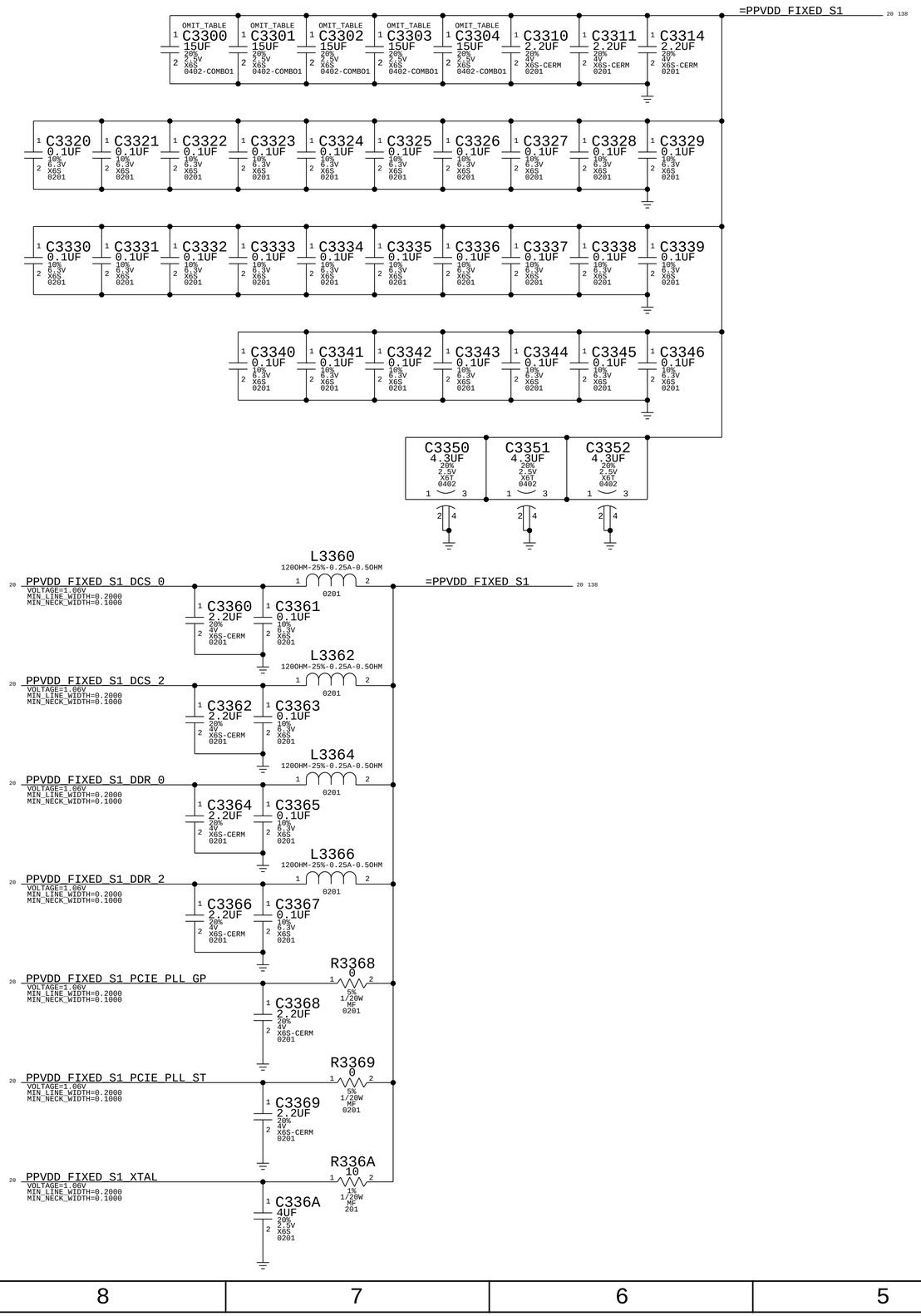

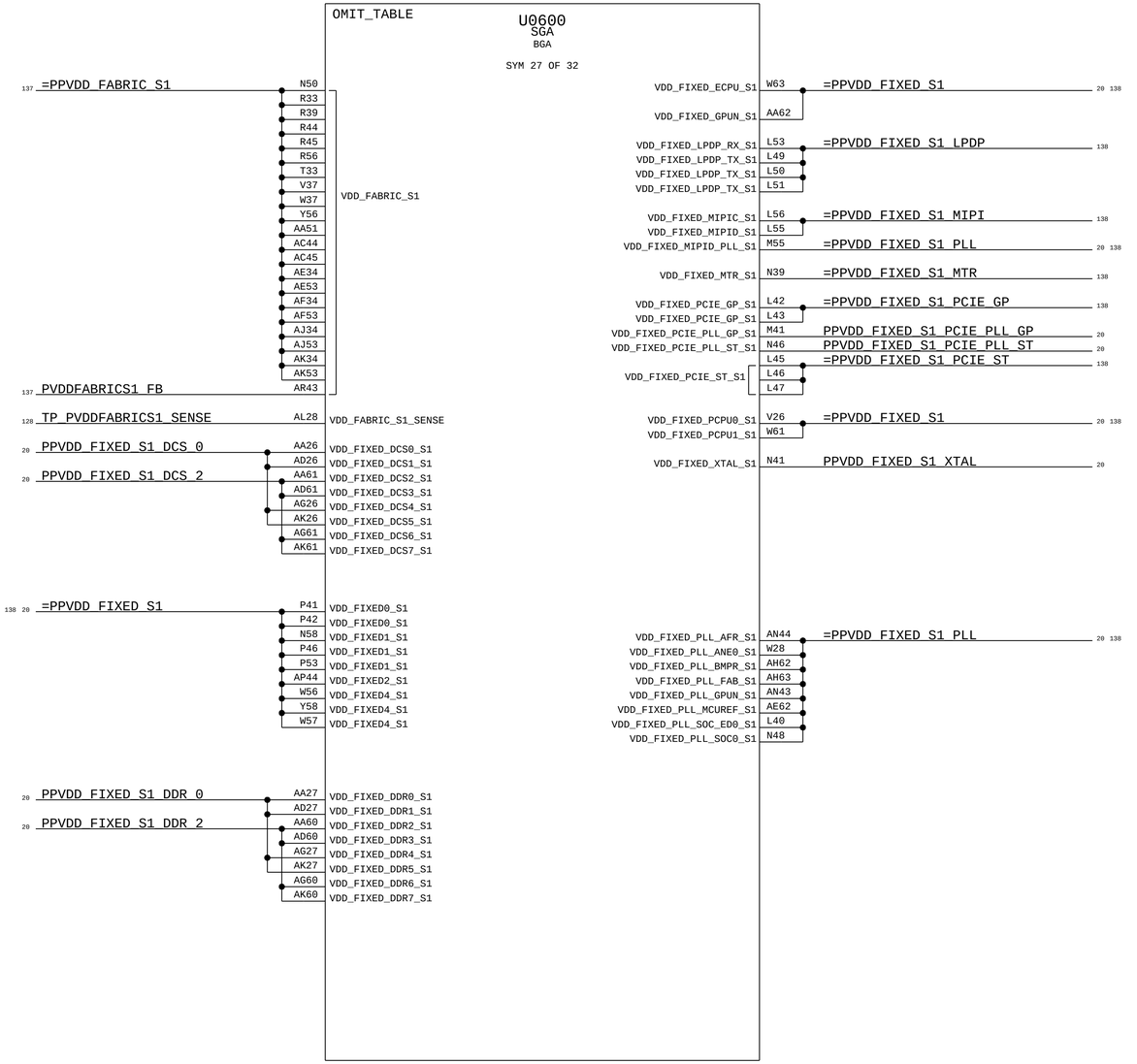

BOM_COST_GROUP=SOC

PAGE TITLE	SOC: POWER (FABRIC, FIXED)
	Apple Inc.
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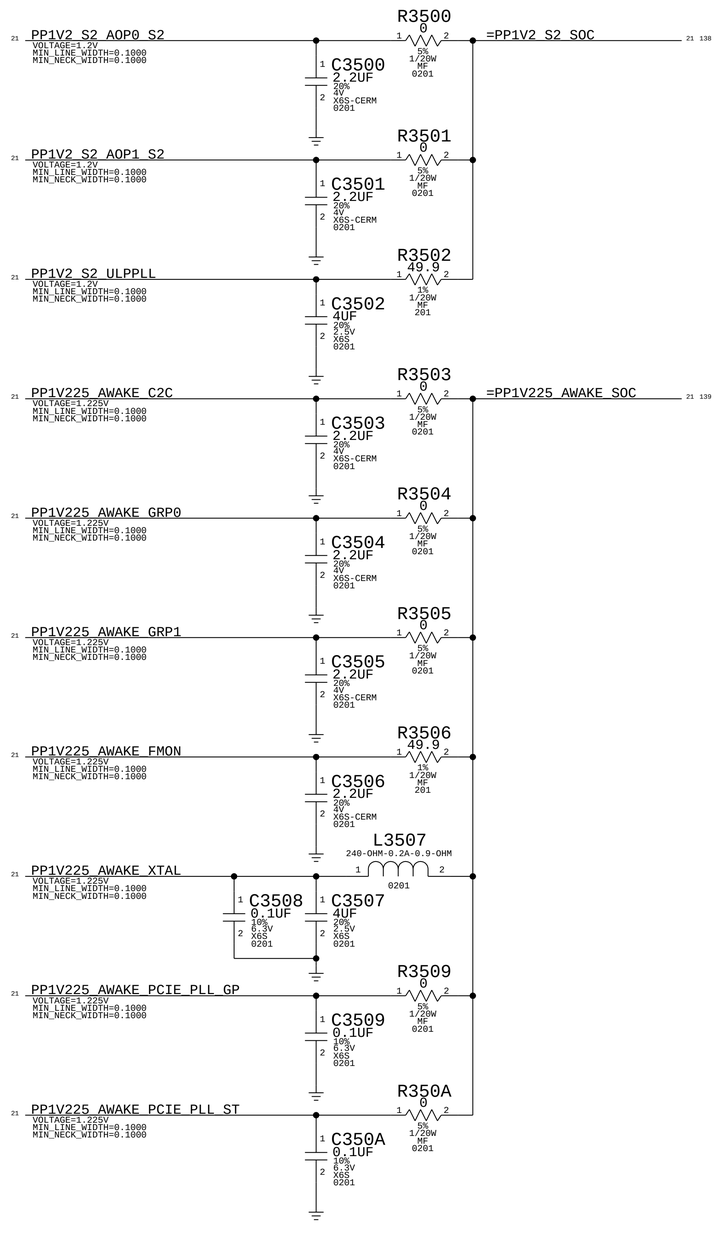

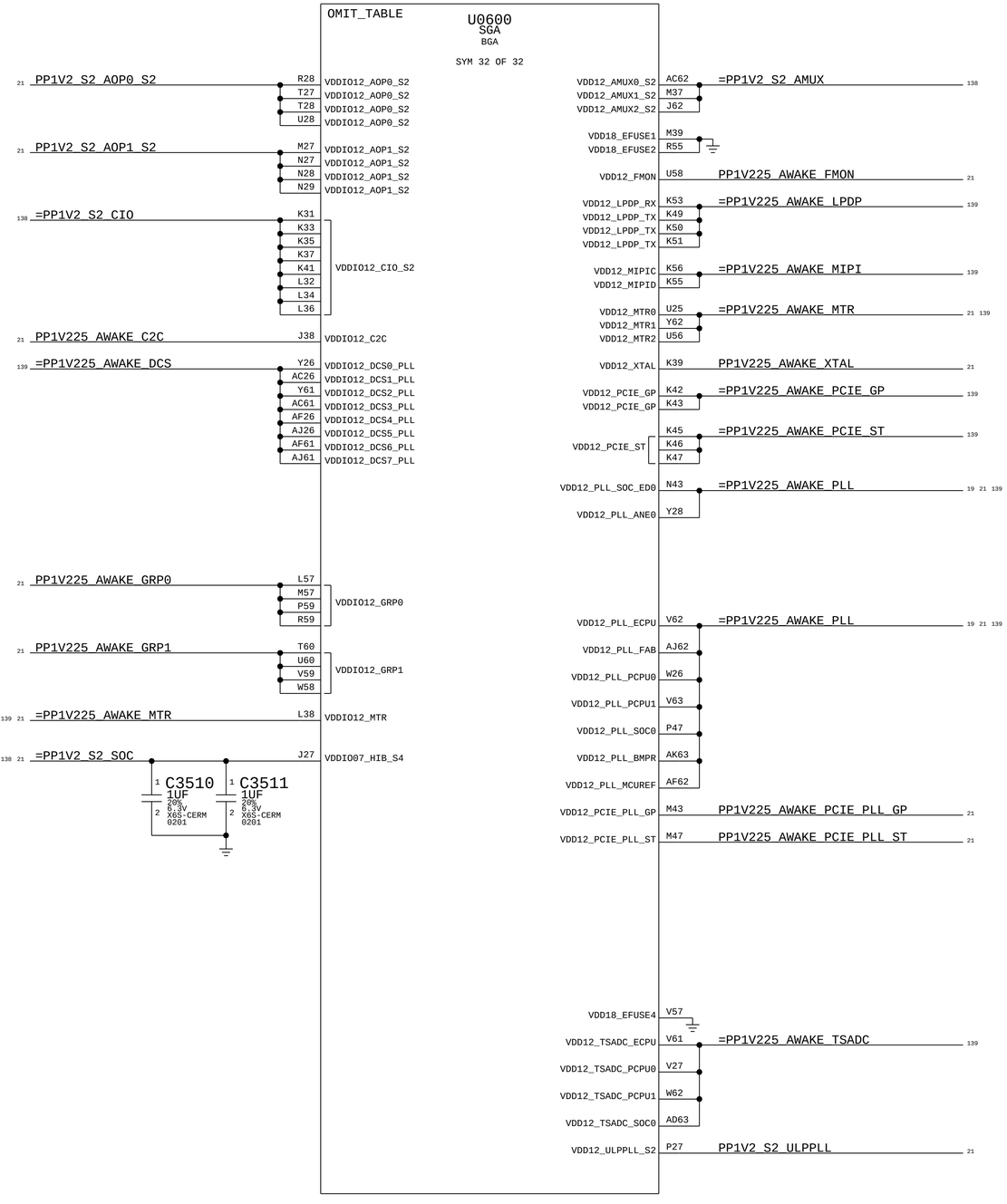

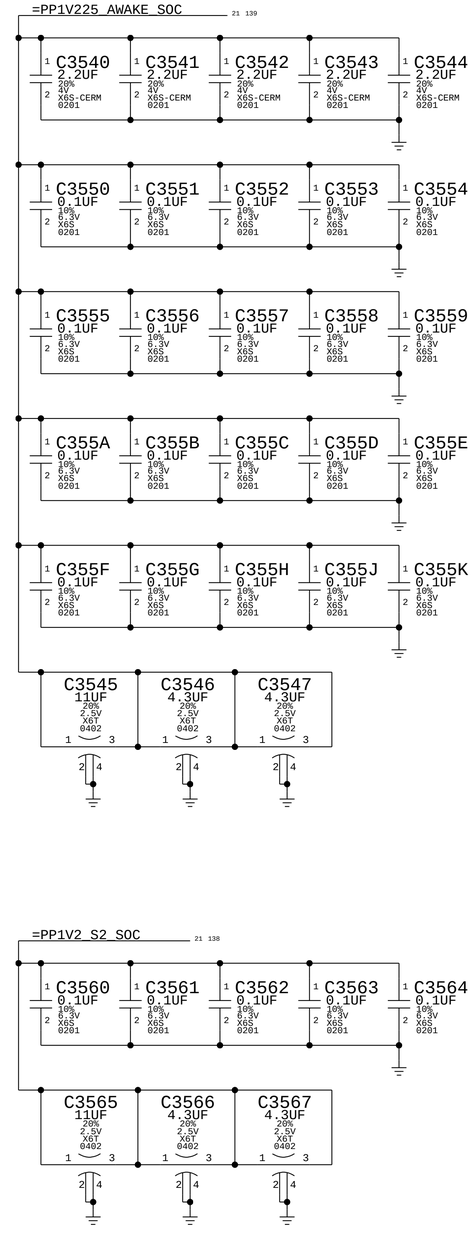

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PAGE TITLE
SOC: POWER (VDDIO)

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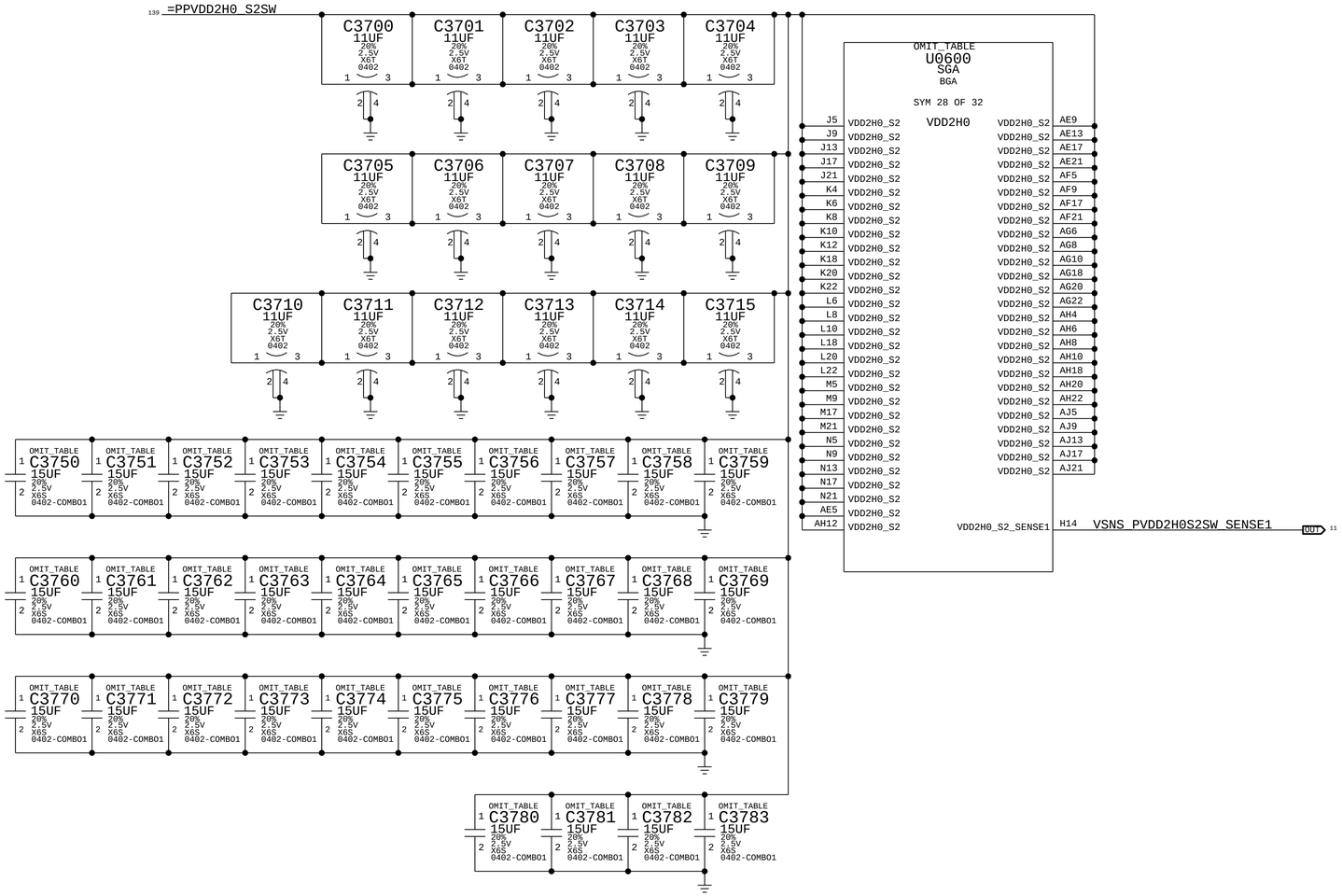

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD2H0)

Apple Inc.

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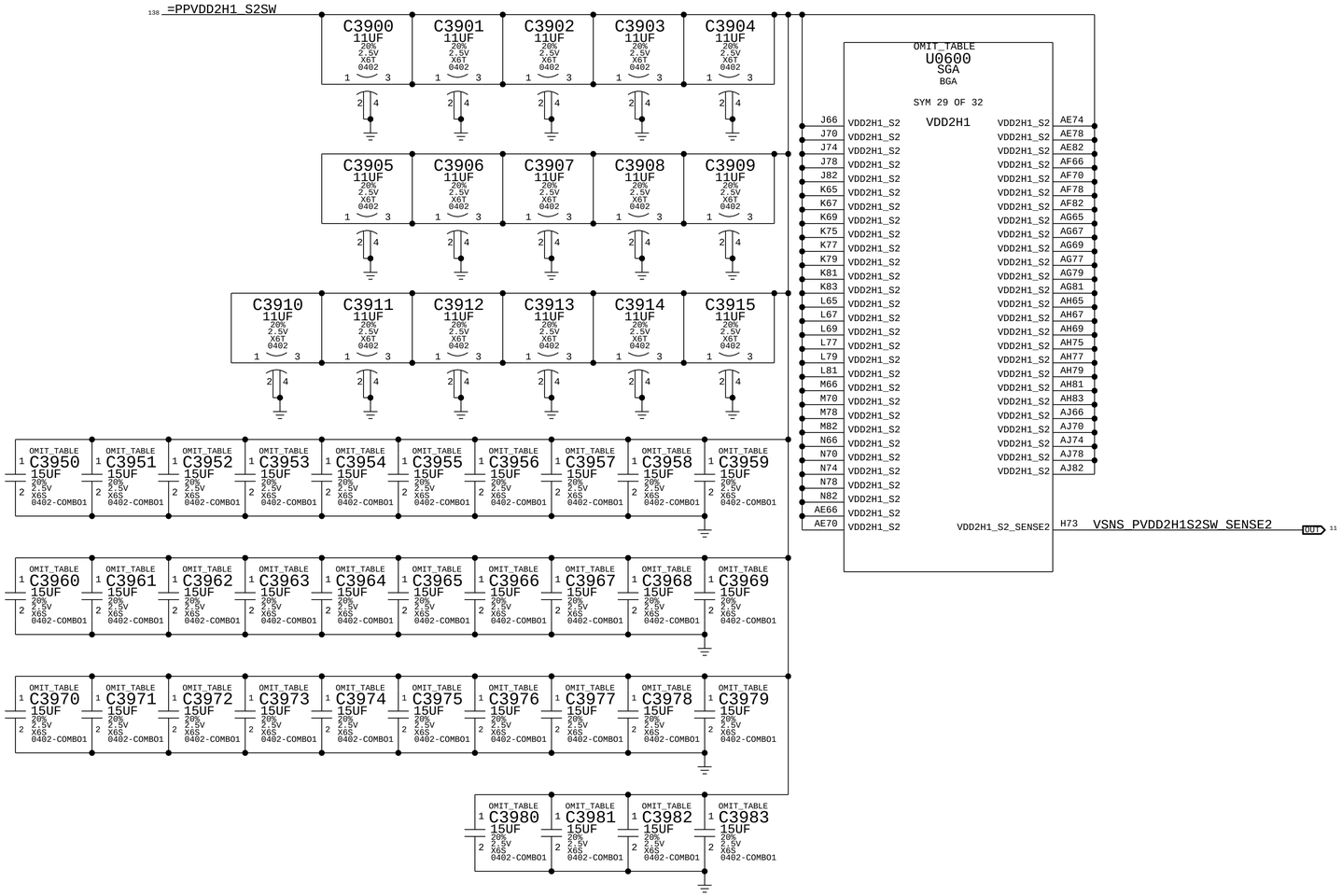

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER (VDD2H1)

Apple Inc.

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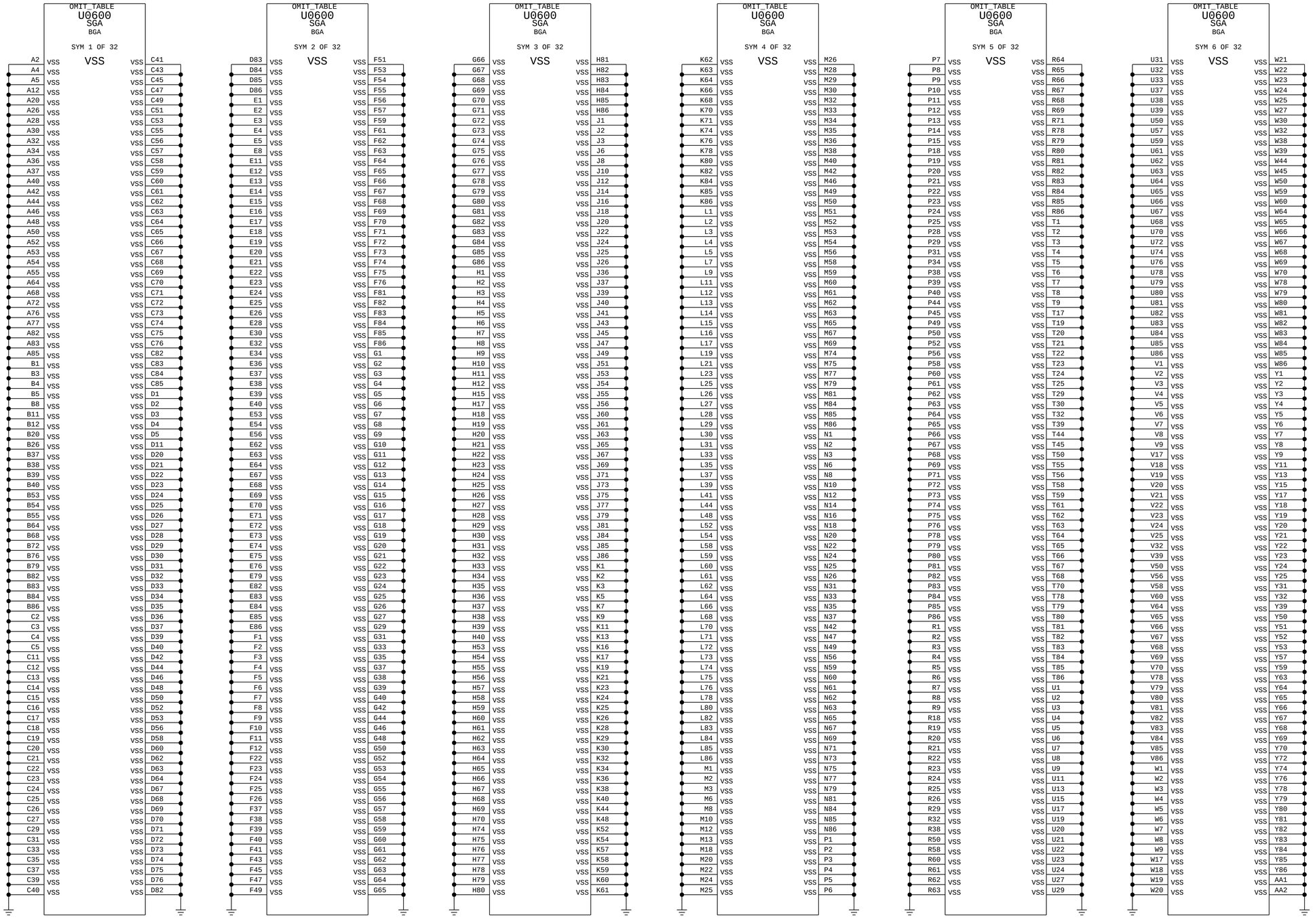

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GND-1

Apple Inc.

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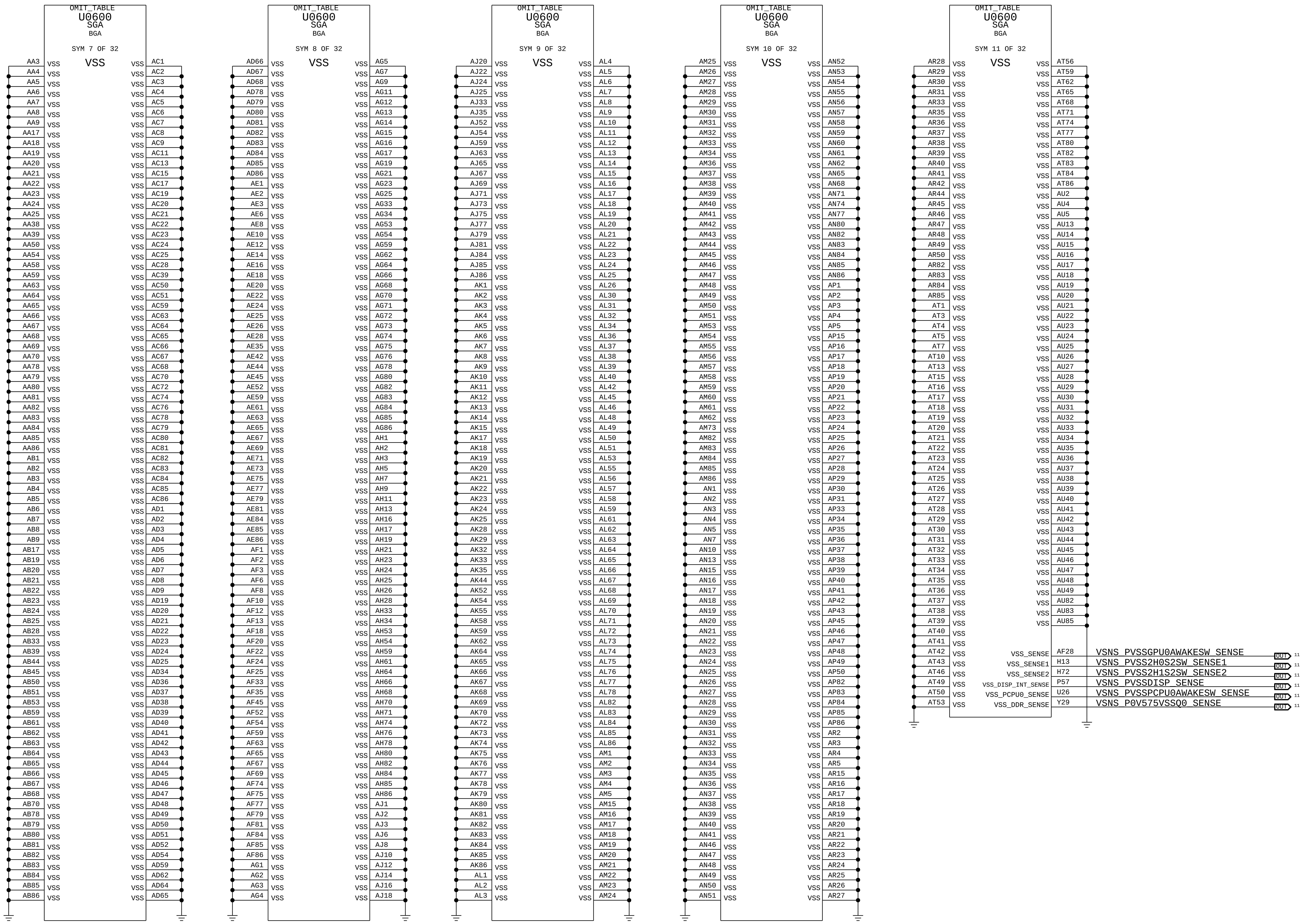

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: GND-2

Apple Inc.

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Timing Requirements:
- VBAT supply ramp time: 20ms

Ceres - Secure Element

*** OK2INTEGRATE ***

Per TGA Power Block Diagram v0.3

=PP1V8_S2_SE 135
IccMax SE only: 125mA
C5014 1.0UF 20% 6.3V X5R 0201-1 (U5000.F9:3mm)

C5002 0.22UF 20% 6.3V X5R 0201 (U5000.F8:3mm)
C5003 0.22UF 20% 6.3V X5R 0201 (U5000.E7:3mm)

=PP1V25_S2_SE 135
IccMax SE only: 10mA
Based on SPMI only use case

VDDBOOST_SE
R5030 0 1/20W MF 0201 5% 1 2 VUP_SE

VDDPLL_SE
VDDNV_SE
VDDC_SE

C5008 0.22UF 20% 6.3V X5R 0201 (U5000.B5:3mm)
C5009 0.22UF 20% 6.3V X5R 0201 (U5000.E8:3mm)
C5010 0.22UF 20% 6.3V X5R 0201 (U5000.E9:3mm)

=PP3V8_AON_SE 26 135
IccMax: 100mA
As per NXP preliminary estimate, final pending
C5051 2.2UF 20% 10V X5R 0201

U5000
SN210VUK/B101V7
WLCSP
OMIT_TABLE

H9	PMUVCC1		
J9	PMUVCC2		
G8	SIMVCC1	NC	
H8	SIMVCC2	NC	
A8	VDDBOOST		
A9	VDDBOOST		
B4	VDDA	NC	
E9	VDDC		
F9	VDDCIN		
F8	VDDIO		
E7	VDDIO_I2C		
J1	VDDIO_SE		
A5	VDDMIX	NC	
E8	VDDNV		
B2	VDDPA	NC	
B5	VDDPLL		
A2	VUP		
A7	VBAT		
D9	VBATPWR		

D4	NFC_CLK_32K		
H6	NFC_CLK_REQ	NC	
A6	NFC_CLK_XTAL1		
G4	NFC_DWL_REQ	26 SE_CTLR_FW_DWLD	
F6	NFC_GPIO0	142 TP_SE_GPIO0	
J7	NFC_GPIO1	NC	
J5	NFC_GPIO2_AO	NC	
H4	NFC_GPIO3_AO	NC	
E6	NFC_HSU_CTS	R5042 47K 1/20W MF 201 5% (NO_TEST) UART_SE_R2D_RTS_L	
F5	NFC_HSU_RTS	NC_UART_SE_D2R_CTS_L	
G5	NFC_HSU_RX	R5041 47K 1/20W MF 201 5% UART_SE_R2D	
E5	NFC_HSU_TX	NC_UART_SE_D2R (NO_TEST)	
E4	NFC_I2C_SCL	NC	
F4	NFC_I2C_SDA	NC	
J6	NFC_IRQ	NC	
G9	NFC_SIM_SWIO1	NC	
J8	NFC_SIM_SWIO2	NC	
H7	NFC_SPMI_SCLK	13 IN SPMI_SE_CLK	
G7	NFC_SPMI_SDATA	13 BI SPMI_SE_DATA	
H5	NFC_WKUP_REQ	26 SE_DEV_WAKE	
B6	NFC_XTAL2	NC	
G6	TM		
A3	RXP		
A4	RXN		

50K internal pull-down

R5050 1M 5% 1/20W MF 201
R5051 1M 5% 1/20W MF 201

H3	SE_GPIO0	NC	
F3	SE_GPIO1	NC	
G1	SE_I2C_SCL	=I2C_SE_SCL	IN 143
H1	SE_I2C_SDA	=I2C_SE_SDA	BI 143
F2	SE_ISO_CLK	NC	
F1	SE_ISO_IO	NC	
G3	SE_ISO_RST	NC	
G2	SE_SPI_CLK	NC	
J2	SE_SPI_CS	NC	
H2	SE_SPI_MISO	NC	
E2	SE_SPI_MOSI	NC	
D2	TXVCASCP	NC	
D1	TXVCASCN	NC	
B3	RXVCM	NC	
C2	TXVCM	NC	
A1	TX1	NC	
C1	TX2	NC	
D7	VCASCHI	NC	
C7	VCASCLO	NC	
B8	BOOST_LX	=PP3V8_AON_SE 26 135	
B9	BOOST_LX		
B7	VHV	VHV_SE	
D3	VTUNE	NC	
D5	VEN	SE_PWR_EN IN 43,44,129	
C5	VREF	VREF_SE	

Pulls to be added in system, can be NC'd if unused

F7	VSS_DIG		
J3	VSS_DIG		
E1	VSS_DIG_2		
J4	VSS_DIG_LN		
C3	VSS_NFC		
B1	VSS_PA		
C4	VSS_PLL		
D6	VSS_PMU		
C8	VSS_PWR		
C9	VSS_PWR		
C6	VSS_REF		
D8	VSS_SUB		
E3	VSS_SUB		

C5004 0.1UF 10% 6.3V CERM-X5R 0201
C5017 0.22UF 20% 6.3V X5R 0201

R5000 47K 1/20W MF 201 5% SE_CTLR_FW_DWLD 26
R5006 47K 1/20W MF 201 5% SE_DEV_WAKE 26

<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

PAGE TITLE: Secure Element
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Battery Sub-System Debug Connector

AARDVARKANOID CONN

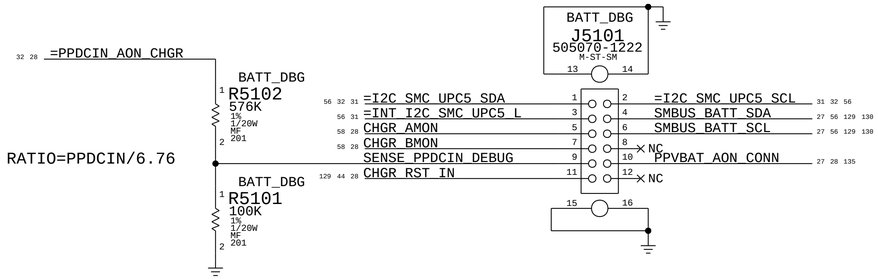
ARKANOID	MLB Connector / Signals		Saleae
J0301 - 1	6	SMBUS_BATT_SCL (= I2C_SMC_PWR_SCL)	0
J0301 - 3	4	SMBUS_BATT_SDA (= I2C_SMC_PWR_SDA)	1
J0301 - 5	2	I2C_SMC_UPC_SCL	2
J0301 - 7	1	I2C_SMC_UPC_SDA	3
J0302 - 1	3	UPC_SMC_I2C_INT_L	4
J0302 - 3	5	CHGR_AMON	5
J0302 - 5	7	CHGR_BMON	6
J0302 - 7	9	1 / 6.76 * PPDCIN_AON	7
J0303 - 1	11	CHGR_RST_IN	8
J0303 - 3	12	—	9
J0303 - 5	10	PPVBAT_AON	10
J0303 - 7	8	—	11

BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-04146	1	PCBA,FLEX,FLEX,BMU-POWER,X1704	J5150	CRITICAL	BATT:POR

Flex Pad TO MLB 998-03780.

J80 Battery Hotbar Flex Pads 998-03902



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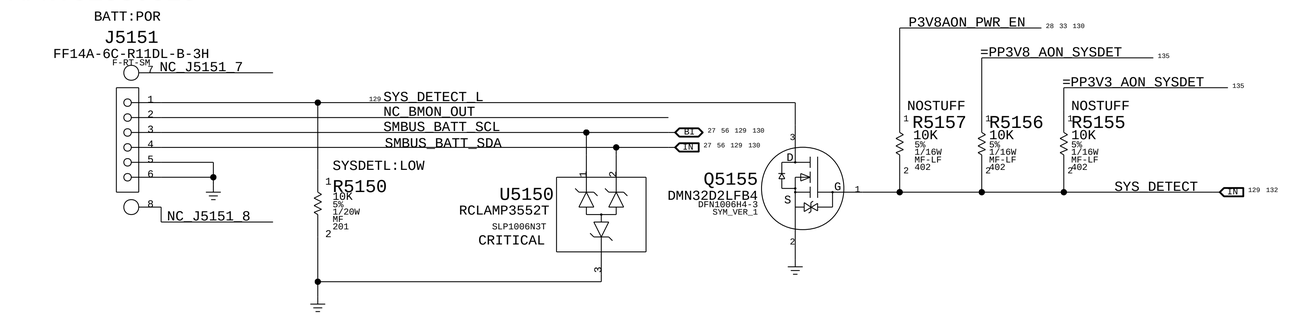

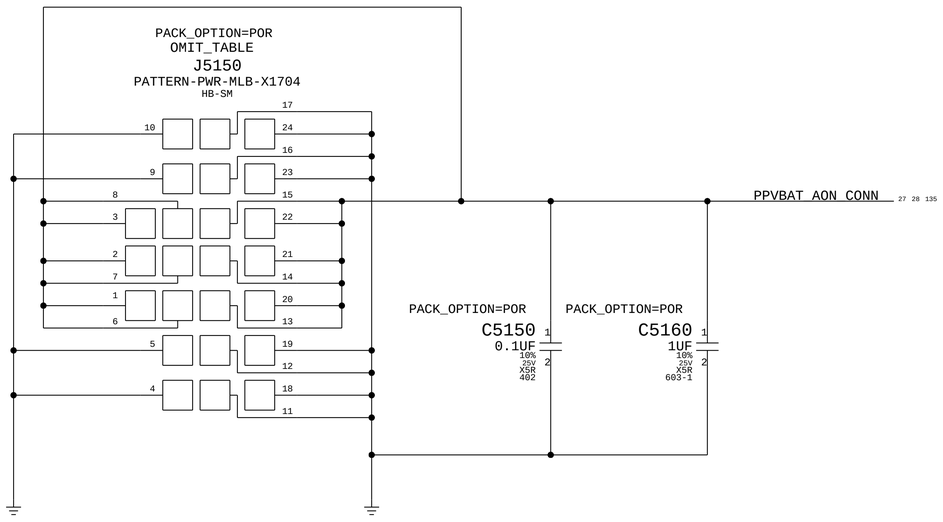

BOM_COST_GROUP=BATTERY

PAGE TITLE: BATTERY CONN

Apple Inc.

DRAWING NUMBER: 051-05641

SIZE: D

REVISION: 6.33.0

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*** OK2PLACE ***

PPDCIN_AON_CHGR_R

CRITICAL C5201 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
CRITICAL C5202 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
CRITICAL C5203 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
C520A 0.1UF 10% 50V CERM-X7R 0402
C520B 0.1UF 10% 50V CERM-X7R 0402
C520C 0.1UF 10% 50V CERM-X7R 0402
C520D 0.1UF 10% 50V CERM-X7R 0402
C520E 0.1UF 10% 50V CERM-X7R 0402
MIN_NECK_WIDTH=0.1800
MIN_LINE_WIDTH=0.6000
VOLTAGE=28V

CRITICAL C5204 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
CRITICAL C5205 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
C520F 0.1UF 10% 50V CERM-X7R 0402
C520G 0.1UF 10% 50V CERM-X7R 0402
C520H 0.1UF 10% 50V CERM-X7R 0402

L5230 1UH-20%-23A-0.0029OHM PIMB103E-SM CRITICAL
CHGR_LL
L5231 1UH-20%-23A-0.0029OHM PIMB103E-SM CRITICAL

CKPLUS_WAIVE=CAPDERATE
CRITICAL C5250 33UF 20% 16V TANT CASED12-SM
CRITICAL C5251 33UF 20% 16V TANT CASED12-SM
CRITICAL C5252 33UF 20% 16V TANT CASED12-SM
CRITICAL C5253 33UF 20% 16V TANT CASED12-SM
CRITICAL C5254 33UF 20% 16V TANT CASED12-SM
CRITICAL C5255 33UF 20% 16V TANT CASED12-SM
CRITICAL C5256 33UF 20% 16V TANT CASED12-SM
CRITICAL C5257 33UF 20% 16V TANT CASED12-SM

CRITICAL C5290 2.2UF 20% 25V X5R 0402-1
CRITICAL C5291 2.2UF 20% 25V X5R 0402-1
C5292 1000PF 10% 25V X7R 0201

107S00044
NO_XNET_CONNECTION=1
CRITICAL R5220 0.01 (AMON) 0.5% 1W MF 0612-1-COMBO
1-CELL: 0.02 OHM
3-CELL: 0.01 OHM

FROM USB-C SOURCE
=PPDCIN_AON_CHGR

CRITICAL C5206 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT
CRITICAL C5207 10UF 20% 50V TANT-POLY 7343-31 CAPMAT=POLY-TANT

CHGR_PHASE1 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_PHASE2 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_GATE_Q1 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q2 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q3 DIDT=TRUE GATE_NODE=TRUE
CHGR_GATE_Q4 DIDT=TRUE SWITCH_NODE=TRUE

ALLOW_APPLE_PREFIX=Q
CRITICAL Q5232 DMTH6004LPDW-13 DFN5060H4-1NL
CRITICAL Q5233 DMTH6004LPDW-13 DFN5060H4-1NL
CRITICAL Q5230 DMTH6004LPDW-13 DFN5060H4-1NL
CRITICAL Q5231 DMTH6004LPDW-13 DFN5060H4-1NL
DOUBLED_FET
CRITICAL Q5240 FDMD8800 DFN
ALLOW_APPLE_PREFIX=Q

CRITICAL F5200 12A-32V-0.0045OHM 1206
CRITICAL F5201 12A-32V-0.0045OHM 1206
TO SYSTEM
=PPBUS_AON_REG
PPVBAT_AON_CHGR_REG
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.05V

PPVBAT_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
CRITICAL C5265 2.2UF 20% 25V X5R 0402-1
CRITICAL C5266 2.2UF 20% 25V X5R 0402-1
CRITICAL C5267 0.1UF 10% 25V X5R 0201
CRITICAL C5268 0.01UF 10% 25V X5R-CERM 0201

Consult DCDC DRI before removing PP

PP5201 P2MM SM CHGR_GATE_Q1 PLACE_SIDE=TOP
PP5211 P2MM SM PLACE_SIDE=BOTTOM
PP5202 P2MM SM CHGR_GATE_Q2 PLACE_SIDE=TOP
PP5212 P2MM SM PLACE_SIDE=BOTTOM
PP5203 P2MM SM CHGR_GATE_Q3 PLACE_SIDE=TOP
PP5213 P2MM SM PLACE_SIDE=BOTTOM
PP5204 P2MM SM CHGR_GATE_Q4 PLACE_SIDE=TOP
PP5214 P2MM SM PLACE_SIDE=BOTTOM
PP5205 P2MM SM CHGR_PHASE1 PLACE_SIDE=TOP
PP5215 P2MM SM PLACE_SIDE=BOTTOM
PP5206 P2MM SM CHGR_PHASE2 PLACE_SIDE=TOP
PP5216 P2MM SM PLACE_SIDE=BOTTOM
PP5207 P2MM SM P3V8AON_PWR_EN
PP5208 P2MM SM CHGR_INT_1V8_L

CHGR_CSI_P PLACE_NEAR=U5200.D5:2MM
R5221 1.00 1% 1/20W MF-LF 0201
CHGR_CSI_N PLACE_NEAR=U5200.C5:2MM
R5222 1.00 1% 1/20W MF-LF 0201
CHGR_CSI_FILT_P
CRITICAL C5221 0.1UF 10% 10V CERM-X7R 0402
CHGR_CSI_FILT_N
CRITICAL C5222 0.047UF 10% 10V CER-X7R 0402

CRITICAL C5220 0.47UF 20% 4V CERM-X5R-1 201
NO_XNET_CONNECTION=1

CRITICAL C5230 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT1_RC DIDT=TRUE SWITCH_NODE=TRUE
R5230 0 5% 1/16W MF-LF 402
CHGR_BOOT1 DIDT=TRUE SWITCH_NODE=TRUE

CHGR_LX2 DIDT=TRUE SWITCH_NODE=TRUE
CRITICAL C5240 0.1UF 10% 25V X7R-CERM-1 0402
CHGR_BOOT2_RC DIDT=TRUE SWITCH_NODE=TRUE
R5240 0 5% 1/16W MF-LF 402
CHGR_BOOT2 DIDT=TRUE SWITCH_NODE=TRUE

(BMON) 2-CELL: 0.010 OHM 3-CELL: 0.005 OHM
NO_XNET_CONNECTION=1
CRITICAL 107S00032 R5265 .01 1% 1W MF 0612
CHGR_CSO1_P
CHGR_CSO1_N
NO_XNET_CONNECTION=1
CRITICAL R5260 .01 1% 1W MF 0612

376S0761
CRITICAL Q5265 SI7137DP SO-8 SYM-VER-2
TO/FROM BATTERY
PPVBAT_AON_CONN
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.05V
VOLTAGE=13.05V
C5264 1000PF 10% 25V X7R 0201
CRITICAL C5263 4700PF 10% 25V CER-X5R 0201
C5269 0.1UF 10% 25V X5R 0201
R5272 0 5% 1/16W MF-LF 402
Place near battery conn.
SAVE_BAT_D
<rdar://37259372&39763505>
CRITICAL Q5270 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2
=PPDCIN_AON_CHGR
R5271 200K 1% 1/20W MF 201
SAVE_BAT_S
SAVE_BAT_G
CRITICAL D5270 DZD5V6LP3-55 DFN0201 ALLOW_APPLE_PREFIX=D
R5263 1K 5% 1/20W MF 201
R5270 24K 5% 1/20W MF 201

XW5260 SM PLACE_NEAR=Q5240.1:2MM
CHGR_CSO_P
CHGR_CSO_N
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
R5261 2 1% 1/20W MF 0201
PLACE_NEAR=U5200.A4:2MM
R5262 2 1% 1/20W MF 0201
PLACE_NEAR=U5200.B4:2MM
CHGR_CSO_FILT_P
CRITICAL C5261 0.047UF 10% 10V CER-X7R 0402
CHGR_CSO_FILT_N
CRITICAL C5262 0.047UF 10% 10V CER-X7R 0402
R5266 2 1% 1/20W MF 0201
CHGR_CSO1_P
R5267 2 1% 1/20W MF 0201
CHGR_CSO1_N
CRITICAL C5260 0.47UF 20% 4V CERM-X5R-1 201
NO_XNET_CONNECTION=1

XW5263 SM PLACE_NEAR=J5150.15:5MM
CHGR_VBAT_XW

PPVBAT_AON_CHGR_REG
C5278 2.2UF 20% 35V X5R-CERM 0402
=PPDCIN_AON_CHGR
OMIT_TABLE
R5215 750K 1% 1/20W MF 201
CHGR_AUX_DET
NOSTUFF C5216 0.01UF 10% 25V X5R-CERM 0201
OMIT_TABLE
R5216 255K 1% 1/20W MF 201
=PP1V8_S2_CHGR
C5280 1.0UF 20% 6.3V X5R 0201-1

PPV5_CHGR_SW
R5275 4.7 MF 5% 1/20W VOLTAGE=5V
R5276 1 MF 5% 1/20W VOLTAGE=5V
PPCHGR_VDDA
CRITICAL C5275 2.2UF 20% 25V X5R-CERM 0402-1
PPCHGR_VDDP
CRITICAL C5277 10UF 20% 25V X5R-CERM 0603
C5223 1.0UF 10% 50V CERM-X7R 0603
PLACE_NEAR=U5200.B5:5MM

U5200 RAA489900 WLCSP CRITICAL 353S02432

B5	P_IN	GATE_Q1	H1
C5	CSIN	BOOT1	F1
D5	CSIP	LX1	G1
A5	PBUS_PWR	GATE_Q2	E1
D3	AUX_DET	GATE_Q3	D1
		LX2	B1
		BOOT2	C1
		GATE_Q4	A1
		PBUS_Q4SNS	A3
		CSOP	A4
		CSON	B4
F5	VDDIO1P8	BGATE	B3
G5	SDA	VBAT	C3
H5	SCL	EN_VR1	F2
G2	SMC_RST_IN	SMC_RST*	H4
G3	HPWR_EN*	IRQ_L	H3
E5	COMP	CBC_ON	H2
G4	CELL	(5V) EN_MVR	F4
B2	NC0	(OD) AUX_OK	F3
C2	NC1	AMON	D4
E4	NC2	BMON	C4
		AGND	E3
		PGND	E2

SMBUS_CHGR_1V8_SDA
SMBUS_CHGR_1V8_SCL
CHGR_RST_IN
CHGR_COMP
H:3-CELL L:2-CELL

CHGR_PBUS_SNS MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
CHGR_BGATE
CHGR_VBAT
TP_CHGR_EN_VR1
TP_CHGR_SMC_RST_L
CHGR_INT_1V8_L
TP_CHGR_CBC_ON
P3V8AON_PWR_EN
CHGR_AUX_OK_1V8
CHGR_AMON
CHGR_BMON

AUX_DET_SHORT
Q5216 DMN5L06TK SOT523 SYM_VER_1
R5217 10K 1% 1/20W MF 201

CRITICAL C5270 0.12UF 10% 10V X5R 0402
CRITICAL C5271 0.12UF 10% 10V X5R 0402

ID Register 0xFF => 0x001C
ID Register 0xFF => 0x000D

BOM_COST_GROUP=BATTERY

PAGE TITLE
PBUS SUPPLY & BATTERY CHARGER

Apple Inc.

DRAWING NUMBER 051-05641
SIZE D
REVISION 6.33.0
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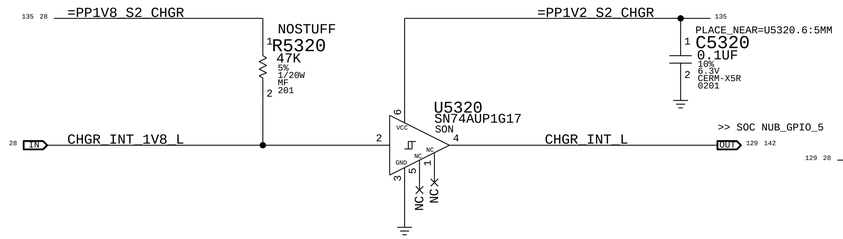
*** OK2PLACE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

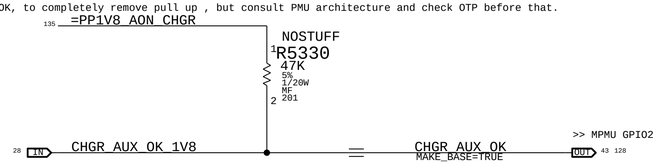
CHGR_INT_L Level Translation

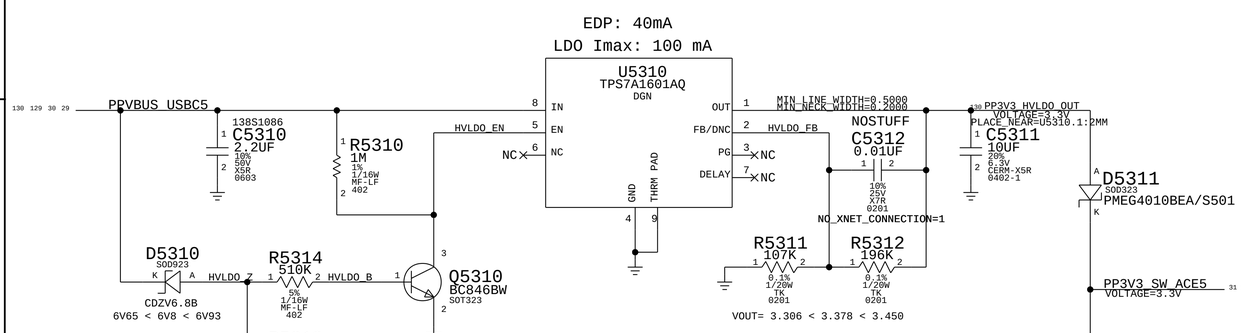
Stuff R5320 in case, glitch during power sequencing is a concern.

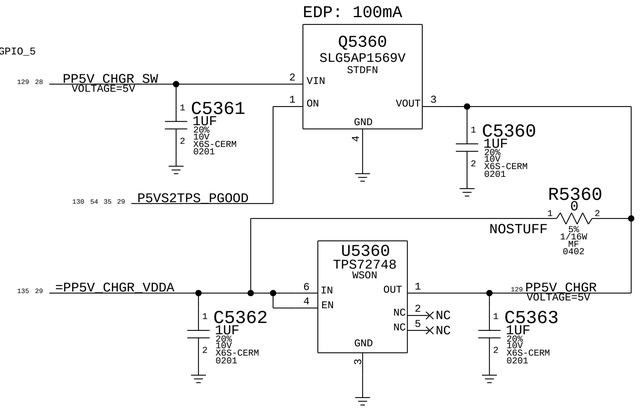


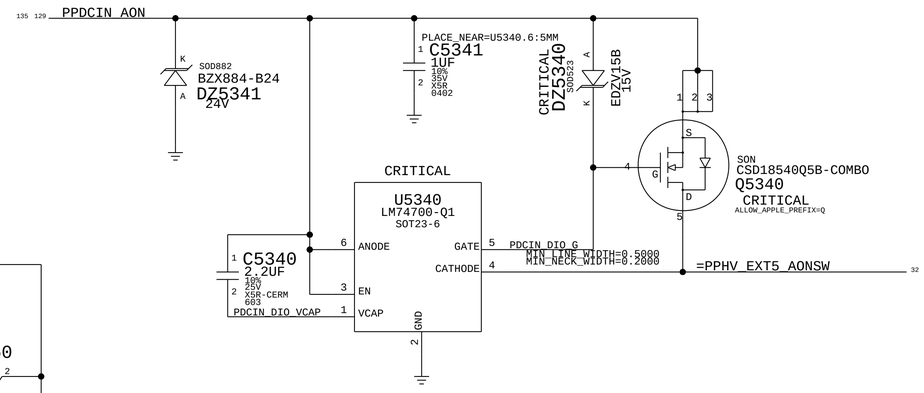
CHGR_AUX_OK Pull Up

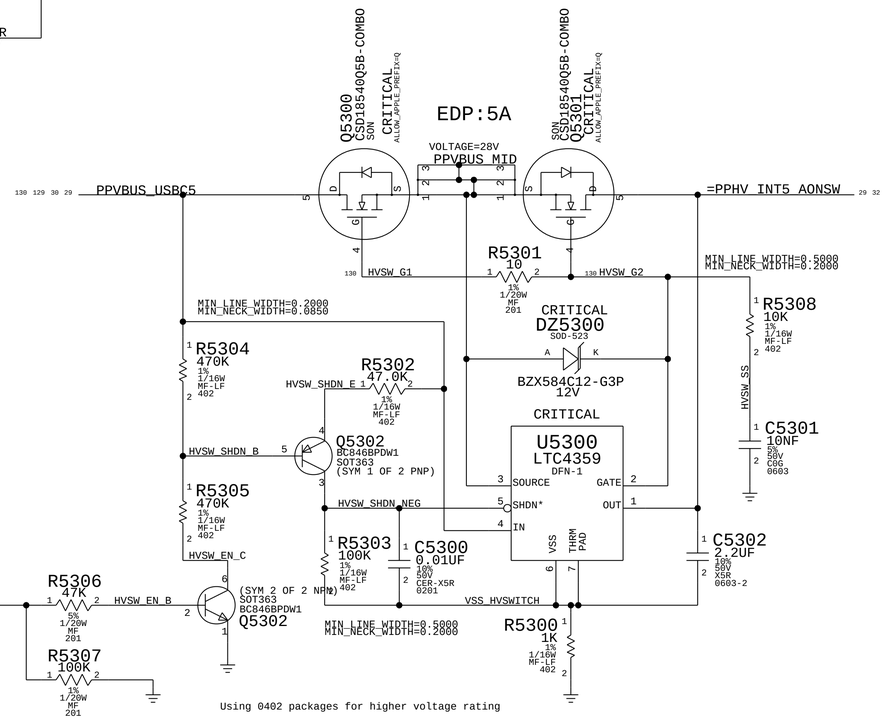
Pull up to MPMU LDO9, or rely on MPMU internal pull up.
OK, to completely remove pull up , but consult PMU architecture and check OTP before that.

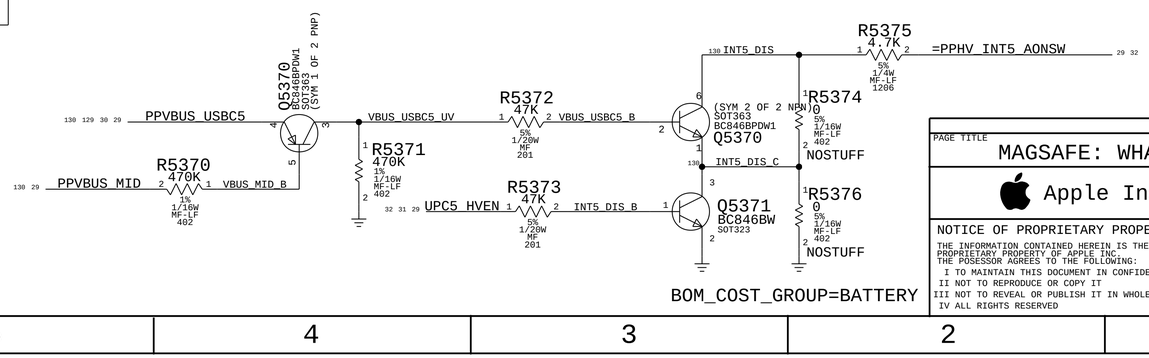








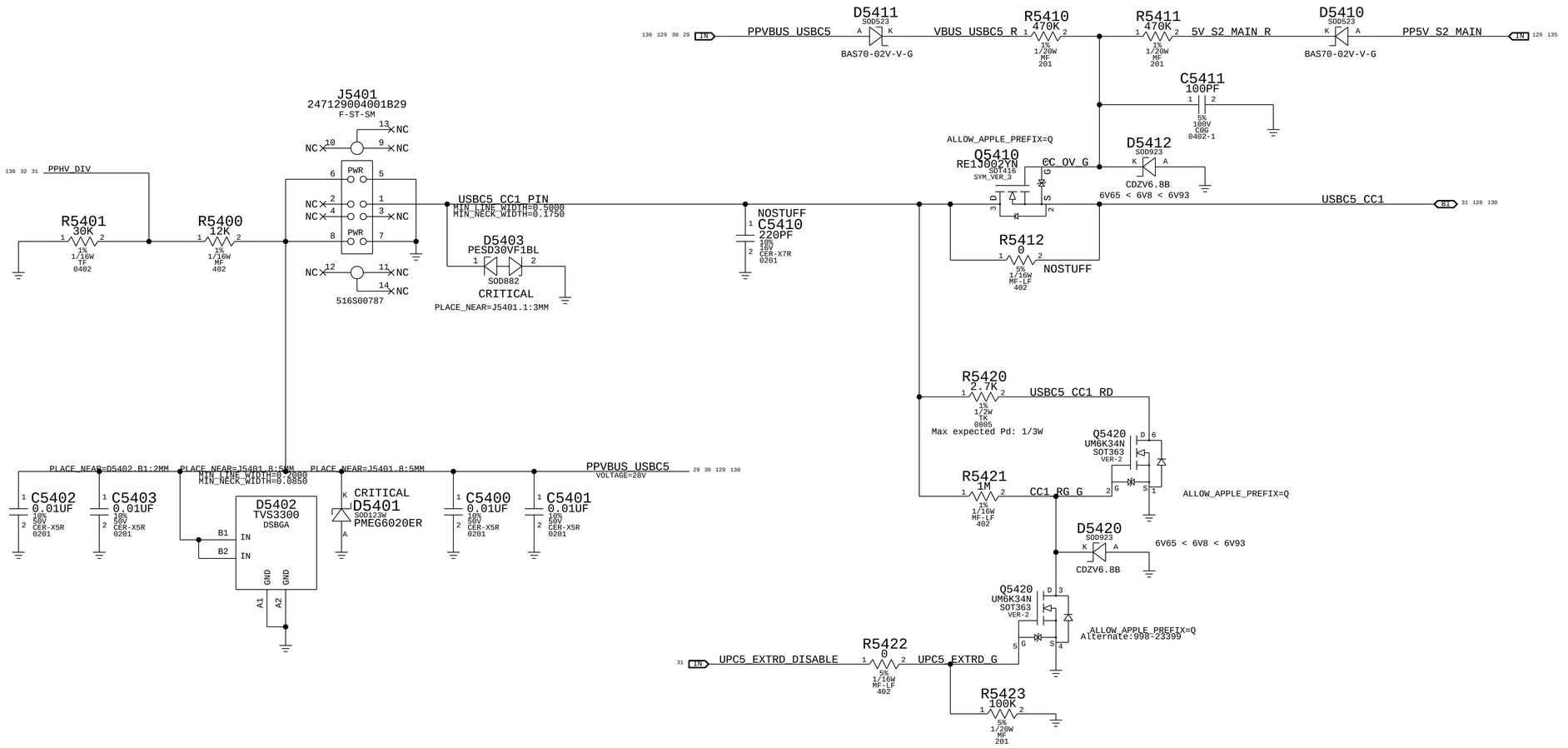




PAGE TITLE	MAGSAFE: WHAMOLA SUPPORT	
Apple Inc.	DRAWING NUMBER 051-05641	SIZE D
	REVISION 6.33.0	
	BRANCH	
	PAGE 53 OF 999	
	SHEET 29 OF 155	

** OK2PLACE **

MAGSAFE MLB connector, CC OV and External RD



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0516	1	UVLO set RH=750K	R5215	CRITICAL	SUONA_UVLO
118S0236	1	UVLO set RL=255K	R5216	CRITICAL	SUONA_UVLO
118S0526	1	UVLO set RH=787K	R5215	CRITICAL	WHAMOLA_UVLO
118S0116	1	UVLO set RL=158K	R5216	CRITICAL	WHAMOLA_UVLO
353S02781	1	IC,RAA489900,PMIC,WHAMOLA,OTP-4,WCSP40	U5200	CRITICAL	WHAMOLA:1A

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-05641 SIZE: D
REVISION: 6.33.0
BRANCH:
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** 0K2PLACE **

Configured as UPC5 (the 6th slot)

PP3V3_UPC5_LDO 31 32

- 1M R5509 5% 1/20W MF 201 — I2C_UPC5_SCL — 31 130 — CKPLUS_WAIVE=I2C_PULLUP
- 1M R5508 5% 1/20W MF 201 — I2C_UPC5_SDA — 31 130 — CKPLUS_WAIVE=I2C_PULLUP
- 10K R5507 5% 1/20W MF 201 — UPC5_GPIO2 — 31
- 1M R5505 5% 1/20W MF 201 — UART_UPC5 — 32
- 100K R5506 5% 1/20W MF 201 — PD_UPC5_MRESET — 31

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

GND_I2C_ADDR PRIMARY ONLY

CRITICAL R5503 15K 0.1% 1/20W TF-LF 0201

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

130 32 30 PPHV_DIV — NOSTUFF C5504 1UF 10% 35V X5R 0402

32 =PP5V_S2_ACE5_VCONN
32 =PP5V_S2_ACE5
CAP FOR PP_5V0 ON VR PAGE

PP_5V0: K9 L10 M9 M10 K11 L12 M11 N12
PP_CABLE: N14 M13
PP_HV: G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 N2 N4
VBUS: G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8

U5500
CD3218B12ACE2
FCBGA

OMIT_TABLE
CRITICAL

DIGITAL CORE I/O & CONTROL

	B13	HRESET	
31 PD_UPC5_MRESET	A14	MRESET	
32 OUT UPC5_RESET_L	B17	RESET*	
129 32 UPC5_GPIO0	A2	GPIO0	
	B1		
29 PMUX_STAT	D1	GPIO1	
31 UPC5_GPIO2	F1	GPIO2	
30 OUT UPC5_EXTRD_DISABLE	C2	GPIO3	
32 OUT UPC5_GPIO4	E2	GPIO4	
32 29 OUT UPC5_HVEN	B3	GPIO5	
85 32 OUT UPC5_GPIO6	C4	GPIO6	
32 OUT UPC5_GPIO7	D3	GPIO7	
32 OUT UPC5_GPIO8	E4	GPIO8	
32 IN UPC5_GPIO9	F3	GPIO9	
32 OUT UPC5_GPIO10	F7	GPIO10	
32 UPC5_BUSPOWER	A18	BUSPOWER	
32 UPC5_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
UPC5_R_OSC	M21	R_OSC	
130 31 I2C_UPC5_SDA	A16	I2CM_SDA_CNFG	
130 31 I2C_UPC5_SCL	B15	I2CM_SCL_CNFG	
55 32 BI =I2C_UPC5_SDA	B5	I2C_SDA1	
55 32 BI =I2C_UPC5_SCL	A4	I2C_SCL1	
55 32 OUT =INT_I2C_UPC5_L	D7	I2C_IRQ1*	
56 32 27 BI =I2C_SMC_UPC5_SDA	B7	I2C_SDA2	
56 32 27 BI =I2C_SMC_UPC5_SCL	A6	I2C_SCL2	
56 27 OUT =INT_I2C_SMC_UPC5_L	C8	I2C_IRQ2*	
32 OUT SPI_UPC5_R_CLK	B9	SPI_CLK	
32 OUT SPI_UPC5_R_MOSI	B11	SPI_MOSI	
32 IN SPI_UPC5_R_MISO	A10	SPI_MISO	
32 OUT SPI_UPC5_R_CS_L	A8	SPI_SSZ	
32 BI SWD_UPC5_DATA	E20	SWD_DATA	IPU
32 BI SWD_UPC5_CLK	E16	SWD_CLK	IPU
32 IN =UART_UPC5_RX	B19	UART_RX	
32 OUT =UART_UPC5_TX	A20	UART_TX	
32 BI USB2_ATC5_LS_P	H19	USB_RP1_P	
32 BI USB2_ATC5_LS_N	H21	USB_RP1_N	
32 BI USB2_UPC5_P2_P	G20	USB_RP2_P	
32 BI USB2_UPC5_P2_N	G22	USB_RP2_N	
32 BI USB2_UPC5_P3_P	F19	USB_RP3_P	
32 BI USB2_UPC5_P3_N	F21	USB_RP3_N	
32 BI USBC5_AUXLSX_P	J12	AUX_P	
32 BI USBC5_AUXLSX_N	H11	AUX_N	
32 PD_UPC5_HPD	C12	HPD	
32 BI UPC5_DBG0	G12	DEBUG0	
32 BI UPC5_DBG1	F11	DEBUG1	
32 BI UPC5_DBG2	E8	DEBUG2	
32 BI UPC5_DBG3	E12	DEBUG3	
32 OUT UPC5_DBG4	G16	DEBUG4	
32 BI UPC5_DBG5	F15	DEBUG5	
32 IN UPC5_DBG6	D15	DEBUG6	
32 OUT UPC5_DBG7	D19	DEBUG7	

PORT_MUX

POWER

TP_PPVBUS_USBC5
R5500 1K 1% 1/16W MF-LF 402
NOSTUFF C5501 1UF 10% 35V X5R 0402

PP3V3_SW_ACE5 29 129 130
C5500 10UF 20% 6.3V CERM 0402

=PP1V225_S2_ACE5 32 135
C5502 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0850
VOLTAGE=3.3V
PP3V3_UPC5_LDO 31 32
C5508 10UF 20% 6.3V CERM 0402

R5501 1K 1% 1/16W MF-LF 402

VIN_3V3	C20	
VDDIO	A12	
VDDIO_CFG	D11	UPC5_VDDIO_CFG 32
LDO_3V3	C22	
	D21	
VIN_LV	L20	UPC5_LV
VOUT_LV	L18	
VRET	C16	
SS	L22	UPC5_SS
LDO_CORE	E22	PP1V5_UPC5_LDO_CORE
VBUS_OPT	D5	=PPVBUS_USBC5_OPT 32 FLOATING?
PP_HV_OPT	F5	=PPHV_INT5_AONSW_OPT HOOKED TO PPHV_DIV

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0850
C5505 10UF 20% 6.3V CERM 0402
R5512 0 5% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
BI 30 128 130

C_CC1	M15	USBC5_CC1
	N16	
C_CC2	M17	USBC5_CC2
	N18	
RPD_G1	L14	USBC5_RPD_G1 BI 32
RPD_G2	L16	USBC5_RPD_G2 BI 32
C_USB_TP	K19	USBC5_USB_TOP_P 31
C_USB_TN	K21	USBC5_USB_TOP_N 31
C_USB_BP	J20	USBC5_USB_BOT_P 31
C_USB_BN	J22	USBC5_USB_BOT_N 31
C_SBU1	J16	USBC5_SBU1 31
C_SBU2	H15	USBC5_SBU2 31

NOSTUFF C5514 220PF 5% 50V C0G 0201-1
C5513 220PF 5% 50V C0G 0201-1

TYPE-C

GND_OPT	C18	
GND_OPT	E18	
GND_OPT	D17	
GND_OPT	G18	

GND

GND: A22 H9 N20 B21 K15 N22

USBC5_USB_BOT_N 31
USBC5_USB_BOT_P 31
USBC5_USB_TOP_N 31
USBC5_USB_TOP_P 31
USBC5_SBU1 31
USBC5_SBU2 31
USBC5_WPD MAKE_BASE=TRUE
R5511 10K 1% 1/10W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02166	1	IC,CD3218,ACE2,B2,USB PWR SW,BGA123	U5500	CRITICAL	

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: PORT CONTROLLER

Apple Inc.

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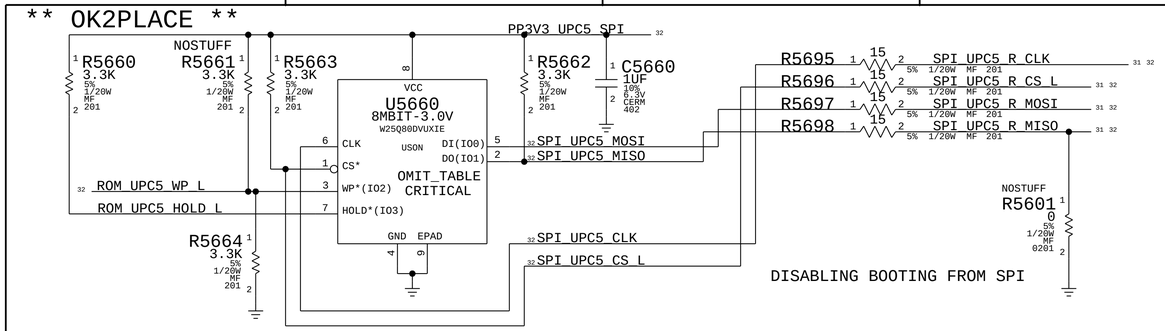
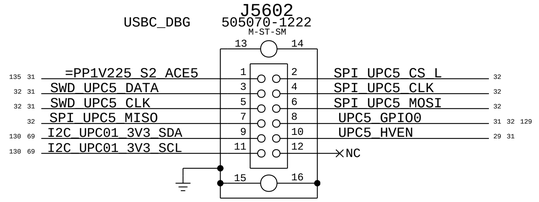
** OK2PLACE **



DISABLING BOOTING FROM SPI

AARDVARKANOID CONN

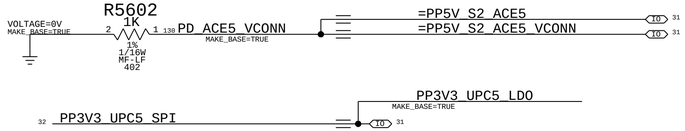


UPC5: I2C_ADDR=Float, I2CM_SCL_CNFG=HIGH, SDA=LOW

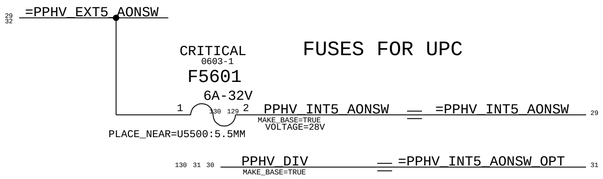
UPC5_I2C_ADDR = NC_UPC5_I2C_ADDR (MAKE_BASE=TRUE; NO_TEST=1)

POWER ALIASES

=PPVBUS_USBC5_OPT = NC_PPVBUS_USBC5_OPT (MAKE_BASE=TRUE)

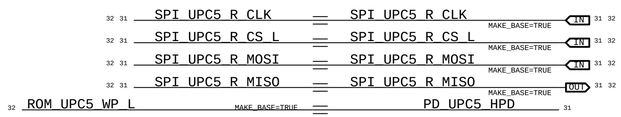


WE DO NOT NEED HIGHER VOLTAGE RATING FOR THIS FUSE CHECKED WITH MFGR

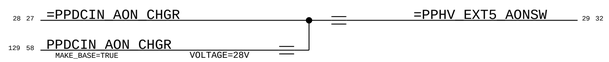


FUSES FOR UPC

ACE5 IS SPI ROM ONLY

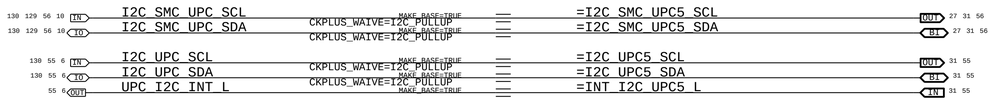


CONNECTION TO CHARGER

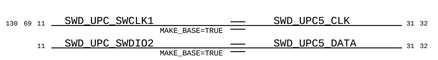


UPC5_RESET_L = NC_UPC5_RESET_L (MAKE_BASE=TRUE; NO_TEST=1)

CCONNECTION TO SoC



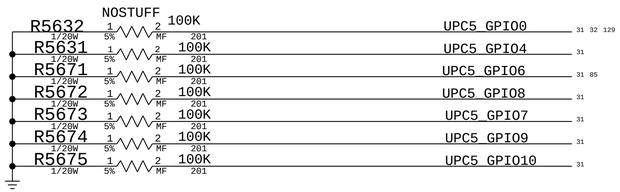
SWD TO SoC

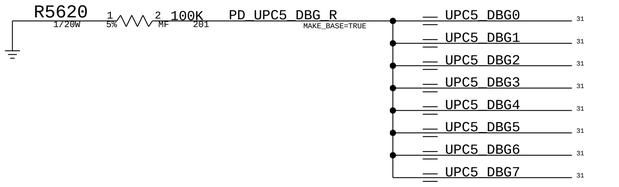


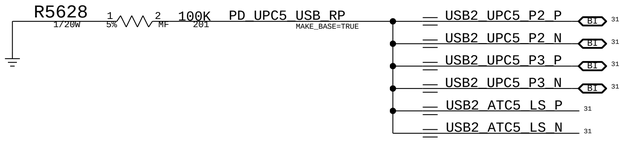
UPC5_VDDIO_CFG

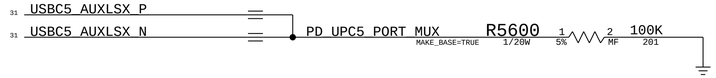
UPC5_BUSPOWER

Unused ports and GPIOs

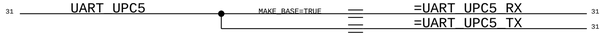








UART



ACE RPD STRAPPING

USBC5_RPD_G1

USBC5_RPD_G2

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: MAGSAFE: CONTROLLER SUPPORT

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*** OK2RELEASE ***

3V8 AON CONTROLLER
30A ICC MAX

=PPVIN_P3V8AON
5.5 < VIN < 13.5 V
C5704 2.2UF 20% 25V X6S-CERM 0402 138S00042 BYPASS=U5700.8::15MM

=PP5V_P3V8AON_VDRV
4.75 < VDRV < 5.5 V
VDRV IS EXTERNAL OPTION TO POWER IC INSTEAD OF VIN TO SAVE POWER
C5700 10UF 20% 10V X6S 0603-1 138S00248 BYPASS=U5700.6::15MM 0603 SIZE REQUESTED BY DCDC

=PP5V_AON_LDO5_REG
4.75 < LDO5 < 5.25 V
MAX I_OUT TYP 160 MA
LDO5 NOT TO BE USED BY SYSTEM IN 30A DESIGNS
C5702 10UF 20% 10V X6S 0603-1 138S00248 BYPASS=U5700.7::15MM 0603 SIZE REQUESTED BY DCDC

P3V8AON_PVCC
ONLY FOR USE BY GATE DRIVE CIRCUITRY
C5701 10UF 20% 10V X6S 0603-1 138S00248 BYPASS=U5700.5::15MM 0603 SIZE REQUESTED BY DCDC

P3V8AON_PWR_EN → R5710 0 5% 1/20W MF 0201 → P3V8AON_PWR_EN_R → ENABLE (9M PD)
VIH_MIN 1.07 V
VIL_MAX 0.63 V

P3V8AON_LPM → R5711 0 5% 1/20W MF 0201 → P3V8AON_LPM_R → LPM (9M PD)
VIH_MIN 1.1 V
VIL_MAX 0.5 V

=PPVDD_3V8AONFAULTPU → R5712 47K 5% 1/20W MF 201
PU TO INT LDO5 OR OTHER RAIL
P3V8AON_FAULT_L → FAULT* (OD)
FAULT PULL DOWN CURRENT 1-2 MA TYPICAL

I2C_P3V8AON_SCL → SCL
I2C_P3V8AON_SDA → SDA
VIH_MIN 1.1 V
VIL_MAX 0.5 V
GND'ED FOR POR (DATASHEET TABLE 1.5)

P3V8AON_IMON
IMON NOT TO BE USED SYSTEM SIDE
<RDAR://58648650>
IMON IS 2.52 V @ 30 A
VENDOR REQUIRES R > 1M, C < 50 PF
R5750 1M 1% 1/20W MF 201 117S0009 → P3V8AON_IMON_P3V8AON → IMON (0-4.5V)
C5751 10PF 5% 25V C0G 0201 131S00003
NOSTUFF R5751 2.21K 1% 1/20W MF 201 118S0199

P3V8AON_GPIO → GPIO
OPEN FOR PRODUCTION APPLICATION PER DATASHEET REV 1.0

P3V8AON_SS → SOFTSTART
LONG STARTUP TIME SO INRUSH BELOW 0.5A USB LIMIT
C5703 0.22UF 10% 25V X5R 0201-1 132S00202
NOSTUFF R5700 100K 5% 1/20W MF 201

EPAD → 33

U5700
RAA225501A-BOM1
QFN
OMIT_TABLE

"BOM1" SCH SYMBOL FOR 30A OTP

APN OF SYMBOL 353S02326

F_SW IS REGISTER CONTROLLED
ICC MAX 30A DESIGN: 1 MHZ

BOOT1	4	P3V8AON_BST1	IN
UGATE1	3	P3V8AON_DRVH1	OUT
PHASE1	2	P3V8AON_SW1	IN
LGATE1	1	P3V8AON_DRVL1	OUT
BOOT2	29	P3V8AON_BST2	IN
UGATE2	30	P3V8AON_DRVH2	OUT
PHASE2	31	P3V8AON_SW2	IN
LGATE2	32	P3V8AON_DRVL2	OUT
BOOT3	28	P3V8AON_BST3	IN
UGATE3	27	P3V8AON_DRVH3	OUT
PHASE3	26	P3V8AON_SW3	IN
LGATE3	25	P3V8AON_DRVL3	OUT
VSEN	15	P3V8AON_VSENSE	IN
VRTN	16	P3V8AON_VRTN	IN
CSP1	19	P3V8AON_ISEN1_P	IN
CSN1	20	P3V8AON_ISEN1_N	IN
CSP2	21	P3V8AON_ISEN2_P	IN
CSN2	22	P3V8AON_ISEN2_N	IN
CSP3	23	P3V8AON_ISEN3_P	IN
CSN3	24	P3V8AON_ISEN3_N	IN

TPT_P3V8AON_PU_RAIL → TP5700 TP-P5 3V8_AON_I2C-DEV
NOSTUFF R5760 1K 5% 1/20W MF 201
NOSTUFF R5761 1K 5% 1/20W MF 201
CKPLUS_WAIVE=I2C_PULLUP I2C_P3V8AON_SCL
CKPLUS_WAIVE=I2C_PULLUP I2C_P3V8AON_SDA
R5762 0 5% 1/20W MF 0201
R5763 0 5% 1/20W MF 0201
3V8_AON_I2C-POR → GND MAKE_BASE=TRUE

30A OTP CHANGES DOCUMENTED IN <RDAR://61519509>
BOM5 IS A CONTINUATION OF BOM1 SINCE BOM1 IS FROZEN FOR TGA PROGRAMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
353S02326	1	IC,RAA225501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC:A0	
353S02472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B0	
353S02544	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B1,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B1	
353S02560	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B2,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B2	
353S02576	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B3,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B3	
353S02592	1	IC,RAA225501B,ICE,BOM1,A2,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R0B0	<- 30A BOM1 OTP TGA PROGRAMS ARE GOING TO RAMP WITH
353S02645	1	IC,RAA225501C,ICE,BOM5,A2,OTP-R170,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R170	<- NEW BOM5 OTP FOR FUTURE PROGRAMS

BOM_COST_GROUP=SOC POWER

PAGE TITLE: POWER: 3V8 AON (1/2)

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*** OK2RELEASE ***

ICCMAX = 30 A

=PPVIN_P3V8AON

P3V8AON_DRVH1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5804 2.2 5% 1/20W MF 201 117S0056 <RDAR://59524111>

P3V8AON_DRVH1_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

CRITICAL Q5800 CSD58889Q3D Q3D 376S00012

P3V8AON_BST1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

R5803 0 5% 1/20W MF 0201 117S0201

P3V8AON_BST1_RC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

C5811 0.1UF 10% 25V CERM-X7R 0402 132S0578

P3V8AON_SW1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

NOSTUFF D5800 SBR1A30T5 SOD523 371S00245 3V8_EXT_DIODE

P3V8AON_PVCC

P3V8AON_DRVL1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5805 1 5% 1/10W MF-LF 402 116S0006

P3V8AON_DRVL1_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

CRITICAL C5800 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5801 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5800 33UF 20% 16V TANT CASED12-SM 128S0436 — CRITICAL C5801 33UF 20% 16V TANT CASED12-SM 128S0436 — CRITICAL C5800 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264 — CRITICAL C5801 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264 — C5804 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5805 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5804)

P3V8AON_VSW1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

CRITICAL L5800 PIBR061E-SM 1UH-20%-11A-0.01150HM 152S01458 — L5800 PIHA052D-SM 1UH-20%-14A-0.0127OHM 152S00765 (3V8_INDUCTOR:2P4MM, PACK_IGNORE=TRUE, 3V8_INDUCTOR:1P5MM)

PP3V8AON_PH1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V

107S00373 R5800 0.004 1% 1/3W LF 0306 (NO_XNET_CONNECTION=1)

=PP3V8_AON_REG

CRITICAL C5890 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5891 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5892 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5893 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5894 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067 — CRITICAL C5895 150UF 20% 6.3V TANT-POLY CASE-B1S-1 128S00067

C5886 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5887) — C5887 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5888 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5889) — C5889 2.2UF 20% 25V X6S-CERM 0402 138S00042

116S0007 R5809 1.5 5% 1/16W MF-LF 402 — P3V8AON_SNUB1 (SWITCH_NODE=TRUE, DIDT=TRUE) — 131S0514 C5809 150PF 5% 50V C0G-CERM 0402 <RDAR://59524111>

NOSTUFF C5814 220PF 5% 50V C0G 0201-1 — C5810 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1) — NOSTUFF C5815 220PF 5% 50V C0G 0201-1

R5801 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS1_P

R5802 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS1_N

P3V8AON_ISEN1_P

P3V8AON_ISEN1_N

=PPVIN_P3V8AON

P3V8AON_DRVH2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5824 1.5 5% 1/8W TK 0402 107S00371

P3V8AON_DRVH2_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

CRITICAL Q5820 AONE36196 376S00281 (ALLOW_APPLE_PREFIX=Q)

P3V8AON_BST2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

R5823 0 NA 0.09W TK 0402 116S00015

P3V8AON_BST2_RC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

C5831 0.1UF 10% 25V CERM-X7R 0402 132S0578

P3V8AON_SW2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

NOSTUFF D5820 SBR1A30T5 SOD523 371S00245 3V8_EXT_DIODE

P3V8AON_PVCC

P3V8AON_DRVL2 — MIN_NECK_WIDTH=0.2000, MIN_LINE_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5825 0.100 1% 1/4W MF 0402 104S0050

P3V8AON_DRVL2_R — MIN_NECK_WIDTH=0.2000, MIN_LINE_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5826 0.100 1% 1/4W MF 0402 104S0050

P3V8AON_DRVL2_RR — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

CRITICAL C5820 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5821 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5820 33UF 20% 16V TANT CASED12-SM 128S0436 — CRITICAL C5820 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264 — C5824 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5825 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5824)

P3V8AON_SW2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE (SAME SW NET ON BOTH SIDES)

R5829 2.2 5% 1/16W MF-LF 402 (DIDT=TRUE, SWITCH_NODE=TRUE) — P3V8AON_SNUB2 — C5829 100PF 5% 50V C0G 0402

L5820 PILA062D-SM-COMBO 0.56UH-20%-22.8A-0.0067OHM 152S01249 CRITICAL (3V8_INDUCTOR:2P4MM)

PP3V8AON_PH2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V

107S00090 R5820 0.001 1% 1/3W MF 0306 (NO_XNET_CONNECTION=1)

NOSTUFF C5834 220PF 5% 50V C0G 0201-1 — C5830 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1) — NOSTUFF C5835 220PF 5% 50V C0G 0201-1

R5821 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS2_P

R5822 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS2_N

P3V8AON_ISEN2_P

P3V8AON_ISEN2_N

=PPVIN_P3V8AON

P3V8AON_DRVH3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5844 1.5 5% 1/8W TK 0402 107S00371

P3V8AON_DRVH3_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

CRITICAL Q5840 AONE36196 376S00281 (ALLOW_APPLE_PREFIX=Q)

P3V8AON_BST3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

R5843 0 NA 0.09W TK 0402 116S00015

P3V8AON_BST3_RC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE

C5851 0.1UF 10% 25V CERM-X7R 0402 132S0578

P3V8AON_SW3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE

NOSTUFF D5840 SBR1A30T5 SOD523 371S00245 3V8_EXT_DIODE

P3V8AON_PVCC

P3V8AON_DRVL3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5845 0.100 1% 1/4W MF 0402 104S0050

P3V8AON_DRVL3_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

R5846 0.100 1% 1/4W MF 0402 104S0050

P3V8AON_DRVL3_RR — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, GATE_NODE=TRUE, DIDT=TRUE

CRITICAL C5840 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5841 33UF 20% 16V TANT CASE-T 128S00009 — CRITICAL C5840 33UF 20% 16V TANT CASED12-SM 128S0436 — CRITICAL C5840 68UF 20% 16V POLY-TANT CASE-D2E-SM 128S0264 — C5844 2.2UF 20% 25V X6S-CERM 0402 138S00042 — C5845 2.2UF 20% 25V X6S-CERM 0402 138S00042 (MIRROR_WITH=C5844)

P3V8AON_SW3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE, DIDT=TRUE (SAME SW NET ON BOTH SIDES)

R5849 2.2 5% 1/16W MF-LF 402 (DIDT=TRUE, SWITCH_NODE=TRUE) — P3V8AON_SNUB3 — C5849 100PF 5% 50V C0G 0402

L5840 PILA062D-SM-COMBO 0.56UH-20%-22.8A-0.0067OHM 152S01249 CRITICAL

PP3V8AON_PH3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=5V

107S00090 R5840 0.001 1% 1/3W MF 0306 (NO_XNET_CONNECTION=1)

NOSTUFF C5854 220PF 5% 50V C0G 0201-1 — C5850 5600PF 10% 10V CERM-X7R 0201 132S0370 (NO_XNET_CONNECTION=1) — NOSTUFF C5855 220PF 5% 50V C0G 0201-1

R5841 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS3_P

R5842 1.00 1% 1/20W MF-LF 0201 118S0744 — P3V8AON_ISNS3_N

P3V8AON_ISEN3_P

P3V8AON_ISEN3_N

XW5870 (NO_XNET_CONNECTION=1) P3V8AON_VSNS_XW_P — R5870 0 5% 1/20W MF 0201 117S0201 (NO_XNET_CONNECTION=1) — P3V8AON_VSENSE

NOSTUFF C5870 1UF 20% 10V X6S-CERM 0201 138S00044

XW5871 (NO_XNET_CONNECTION=1) P3V8AON_VSNS_XW_N — R5871 0 5% 1/20W MF 0201 117S0201 (NO_XNET_CONNECTION=1) — P3V8AON_VRTN

BOM_COST_GROUP=SOC POWER

PAGE TITLE: POWER: 3V8 AON (2/2)

Apple Inc.

DRAWING NUMBER: 051-05641 | SIZE: D

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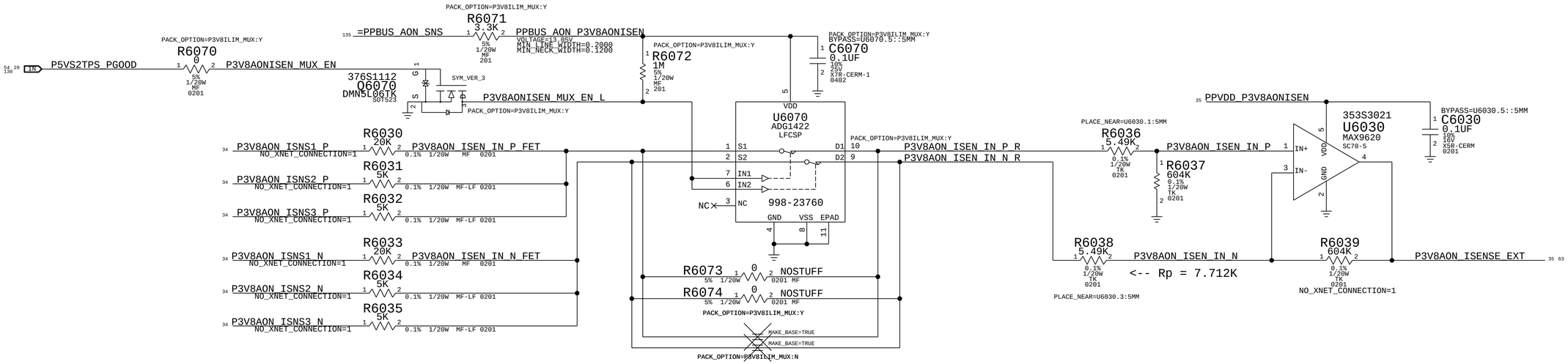
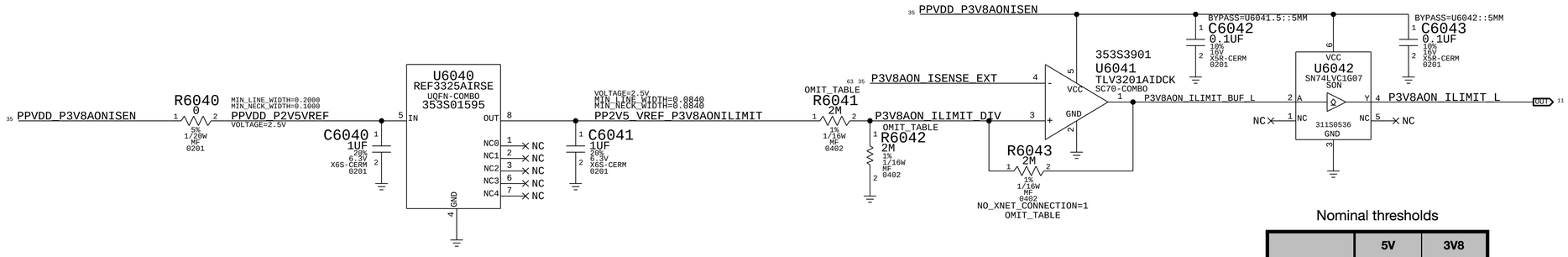
P3V8 LOW SIDE ISENSE AND ILIMIT (SUMMING AMP FOR 3 PHASES)

rdar://problem/69466996 Iceman Throttle Design Data

10A MAX ON PHASE 1, MAX TOTAL CURRENT SENSE @ PMU= 43.11A



PHASE 1 VSENSE GAIN: 8.75
PHASE 2/3 VSENSE GAIN: 35
4:1 WEIGHT FOR PHASE 1 RTREE



Nominal thresholds

		5V		3V8	
		A	V	A	V
BOM1	th_rise	34.6	1.20	32.7	1.20
	th_fall	32.9	1.14	34.4	1.14
BOM2	th_rise	49.7	1.30	47.1	1.29
	th_fall	47.3	1.24	49.5	1.23

Call one of these BOM GROUPs in the main BOM:

BOM GROUP	BOM OPTIONS
P3V8ILIM:BOM1_5V	P3V8ILIM_RT:23K2,P3V8ILIM_RB:20K,P3V8ILIM_RF:909K,P3V8ILIM_VCC:5V
P3V8ILIM:BOM2_5V	P3V8ILIM_RT:22K,P3V8ILIM_RB:22K,P3V8ILIM_RF:887K,P3V8ILIM_VCC:5V
P3V8ILIM:BOM1_3V8	P3V8ILIM_RT:23K2,P3V8ILIM_RB:20K,P3V8ILIM_RF:680K,P3V8ILIM_VCC:3V8
P3V8ILIM:BOM2_3V8	P3V8ILIM_RT:22K,P3V8ILIM_RB:22K,P3V8ILIM_RF:649K,P3V8ILIM_VCC:3V8

Don't Call these OPTIONs directly:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0349	1	RES,0402,1%,1/16W,23.2K	R6041	P3V8ILIM_RT:23K2
114S00141	1	RES,0402,1%,1/16W,22K	R6041	P3V8ILIM_RT:22K
114S0343	1	RES,0402,1%,1/16W,20K	R6042	P3V8ILIM_RB:20K
114S00141	1	RES,0402,1%,1/16W,22K	R6042	P3V8ILIM_RB:22K
114S0491	1	RES,0402,1%,1/16W,649K	R6043	P3V8ILIM_RF:649K
114S00146	1	RES,0402,1%,1/16W,680K	R6043	P3V8ILIM_RF:680K
114S0504	1	RES,0402,1%,1/16W,887K	R6043	P3V8ILIM_RF:887K
114S0505	1	RES,0402,1%,1/16W,909K	R6043	P3V8ILIM_RF:909K

BOM_COST_GROUP=SOC POWER

PAGE TITLE: POWER: 3V8 AON OUTPUT THROTTLE

Apple Inc.

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Desense Caps for every rail

1 pair for 1- and 2- phase BUCKs
2 pairs for 3- and 4- phase BUCKs

138 42 40 =PPVDD_ECPU_AWAKE_REG
- C7600 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7601 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- C7602 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7603 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PPVDD_GPU_BMPR_S1_REG
- C7610 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7611 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PPVDD_ECPU_SRAM_AWAKE_REG
- C7620 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7621 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PP1V8_S2SW_REG
- C7630 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7631 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PPVDD2H1_S2SW_REG
- C7640 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7641 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- C7642 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7643 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PPVDD_AVEMSR_AWAKESW_REG
- C7650 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7651 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- C7652 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7653 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PPVDD_AMPH1_S2SW_REG
- C7660 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7661 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PP0V81_S1_SRAM_REG
- C7670 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7671 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- C7672 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7673 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 135 42 40 =PP1V2_S2_REG
- C7680 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7681 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PPVDD_FIXED_S1_REG
- C7690 1 | 2 12PF 25V NP0-C0G 5% 0201
- C7691 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

138 42 40 =PP0V575_S1_VDDQ1_REG
- C76A0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76A1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 40 38 =PPVDD_DCS_S1_REG
- C76B0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76B1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- C76B2 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76B3 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 40 38 =PP0V575_S1_VDDQ0_REG
- C76C0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76C1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 40 38 =PP0V95_S2SW_VDD2L_REG
- C76D0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76D1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 135 40 38 =PP1V8_S2_REG
- C76E0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76E1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 40 38 =PPVDD2H0_S2SW_REG
- C76F0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76F1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- C76F2 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76F3 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 40 38 =PPVDD_SOC_S1_REG
- C76G0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76G1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- C76G2 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76G3 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 40 38 =PP0V855_S2_VDDCIO_REG
- C76H0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76H1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 135 40 38 =PP1V225_AWAKE_REG
- C76J0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76J1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 40 38 =PPVDD_AMPH0_S2SW_REG
- C76K0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76K1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

139 40 38 =PPVDD_DISP_AWAKESW_REG
- C76L0 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76L1 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201
- C76L2 1 | 2 12PF 25V NP0-C0G 5% 0201
- C76L3 1 | 2 3.0PF 25V NP0-C0G +/-0.1PF 0201

BOM_COST_GROUP=WIRELESS

PAGE TITLE
PMU BUCK OUTPUT DESENSE CAPS

Apple Inc.

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*** OK2INTEGRATE ***

Place these caps on opposite side of PMU
Placement strategy varies by program

Place these caps on PMU side as drawn here

Pin A1
Bottom View

All VIN_LDOx and VBUCK_SWx pins must be powered or GND'd. Do not float!

BOM_COST_GROUP=SOC POWER

VDDLOW
Vboot = 0.8V (based on AM/BM OTP)

PAGE TITLE	PMIC SLAVE VIN/LDO/SW
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*** OK2INTEGRATE ***

SLAVE BUCKS

TODO: XW's are only for 16L boards. TBD how to manage this in a ref-schematic

U7700
MVK-PLUS
BGA
SYM 2 OF 4
OMIT_TABLE

System BUCK11
Vboot = 0.696875V
IOUT_MAX = 19.2A

=PPVDD_SOC_S1_REG (139 40 36)

L7850 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
L7851 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887
L7852 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887
L7853 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887

SPMU_BUCK5_LX0	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	Y9 / AA9 / AB9	BUCK5_LX0
SPMU_BUCK5_LX1	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	Y11 / AA11 / AB11	BUCK5_LX1
SPMU_BUCK5_LX2	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	Y13 / AA13 / AB13	BUCK5_LX2
SPMU_BUCK5_LX3	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	Y15 / AA15 / AB15	BUCK5_LX3

=PPVDD_SOC_S1_FB (139) — XW7850 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, NO_XNET_CONNECTION=1 — SPMU_BUCK5_FB_R

R7850 0 1/20W MF 0201 5% (64 44 39 38 37) — SPMU_BUCK5_FB (130) — V10 — BUCK5_FB
VSS_ANA_SPMU — W14 — VSS_A_BUCK5

System BUCK16
Vboot = 0.85625V
IOUT_MAX = 2.1A
OFF in SLP_SMC, and S2 if CIO is unplugged

=PP0V855_S2_VDDCIO_REG (139 40 36)

L7860 0.47UH-20%-4A-0.027OHM — 2012 152S00885

SPMU_BUCK6_LX0	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	Y7 / AA7 / AB7	BUCK6_LX0

=PP0V855_S2_VDDCIO_FB (139) — XW7860 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, NO_XNET_CONNECTION=1 — SPMU_BUCK6_FB_R

R7860 0 1/20W MF 0201 5% (64 44 39 38 37) — SPMU_BUCK6_FB (130) — V6 — BUCK6_FB
VSS_ANA_SPMU — W6 — VSS_A_BUCK6

System BUCK15
Vboot = 0.715625V
IOUT_MAX = 9A

Not used on sC designs

=PPVDD_DISP2_AWAKESW_REG (139 40)

L7870 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883 — BOMOPTION=PMU_DISP2:Y — PACK_OPTION=PMU_DISP2:Y, PACK_IGNORE=TRUE
L7871 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887 — BOMOPTION=PMU_DISP2:Y — PACK_OPTION=PMU_DISP2:Y, PACK_IGNORE=TRUE
L7872 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887 — BOMOPTION=PMU_DISP2:Y — PACK_OPTION=PMU_DISP2:Y, PACK_IGNORE=TRUE

SPMU_BUCK7_LX0	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A6 / B6 / C6	BUCK7_LX0
SPMU_BUCK7_LX1	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A8 / B8 / C8	BUCK7_LX1
SPMU_BUCK7_LX2	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A10 / B10 / C10	BUCK7_LX2

=PPVDD_DISP2_AWAKESW_FB (139) — XW7870 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, PACK_OPTION=PMU_DISP2:Y, PACK_IGNORE=TRUE, NO_XNET_CONNECTION=1 — SPMU_BUCK7_FB_R

R7870 0 1/20W MF 0201 5% (PACK_OPTION=PMU_DISP2:Y, PACK_IGNORE=TRUE) — SPMU_BUCK7_FB (130) — F7 — BUCK7_FB
VSS_ANA_SPMU (64 44 39 38 37) — MAKE_BASE=TRUE — D7 — VSS_A_BUCK7
SPMU_BUCK7_FB — PACK_OPTION=PMU_DISP2:N

System BUCK12
Vboot = 1.225V
IOUT_MAX = 3.2A

=PP1V225_AWAKE_REG (139 135 40 36)

L7880 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883

SPMU_BUCK8_LX0	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	L20 / L19	BUCK8_LX0

=PP1V225_AWAKE_FB (139) — XW7880 SHORT-16L-0.1MM-SM — NO_XNET_CONNECTION=1 — SPMU_BUCK8_FB_R

R7880 0 1/20W MF 0201 5% (64 44 39 38 37) — SPMU_BUCK8_FB (130) — M17 — BUCK8_FB
VSS_ANA_SPMU — L17 — VSS_A_BUCK8

System BUCK21
Vboot = 1.121875V
IOUT_MAX = 2.1A
OFF in SLP_SMC

=PPVDD_AMPH0_S2SW_REG (139 40 36)

L7890 0.47UH-20%-4A-0.027OHM — 2012 152S00885

SPMU_BUCK9_LX0	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	N20 / N19	BUCK9_LX0

=PPVDD_AMPH0_S2SW_FB (139) — XW7890 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, NO_XNET_CONNECTION=1 — SPMU_BUCK9_FB_R

R7890 0 1/20W MF 0201 5% (64 44 39 38 37) — SPMU_BUCK9_FB (130) — P17 — BUCK9_FB
VSS_ANA_SPMU — N17 — VSS_A_BUCK9

System BUCK20
Vboot = 0.715625V
Iout_Max = 13.2A/14.3A

=PPVDD_DISP_AWAKESW_REG (139 40 36)

L78A0 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
L78A1 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887
L78A2 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887

SPMU_BUCK10_LX0	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	R3 / R2 / R1	BUCK10_LX0
SPMU_BUCK10_LX1	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	U3 / U2 / U1	BUCK10_LX1
SPMU_BUCK10_LX2	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	W3 / W2 / W1	BUCK10_LX2

=PPVDD_DISP_AWAKESW_FB (139) — XW78A0 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, NO_XNET_CONNECTION=1 — SPMU_BUCK10_FB_R

R78A0 0 1/20W MF 0201 5% (64 44 39 38 37) — SPMU_BUCK10_FB (130) — T5 — BUCK10_FB
VSS_ANA_SPMU — T4 — VSS_A_BUCK10

System BUCK17
Vboot = 0.696875V
IOUT_MAX = 19.2A

=PPVDD_DCS_S1_REG (36 40 139)

L7800 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
L7801 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887
L7802 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887
L7803 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887

SPMU_BUCK0_LX0	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A19 / B19 / C19	BUCK0_LX0
SPMU_BUCK0_LX1	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A17 / B17 / C17	BUCK0_LX1
SPMU_BUCK0_LX2	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A15 / B15 / C15	BUCK0_LX2
SPMU_BUCK0_LX3	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A13 / B13 / C13	BUCK0_LX3

R7800 0 1/20W MF 0201 5% (37 38 39 44 64) — SPMU_BUCK0_FB (130) — F17 — BUCK0_FB
VSS_ANA_SPMU — D18 — VSS_A_BUCK0
SPMU_BUCK0_FB_R — XW7800 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, NO_XNET_CONNECTION=1 — =PPVDD_DCS_S1_FB (139)

System BUCK13
Vboot = 0.575V
IOUT_MAX = 5.4A

=PP0V575_S1_VDDQ0_REG (36 40 139)

L7810 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
L7811 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887

SPMU_BUCK1_LX0	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A4 / B4 / C4	BUCK1_LX0
SPMU_BUCK1_LX1	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	A2 / B2 / C2	BUCK1_LX1

R7810 0 1/20W MF 0201 5% (37 38 39 44 64) — SPMU_BUCK1_FB (130) — F6 — BUCK1_FB
VSS_ANA_SPMU — E4 — VSS_A_BUCK1
SPMU_BUCK1_FB_R — XW7810 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, NO_XNET_CONNECTION=1 — =PP0V575_S1_VDDQ0_FB (139)

System BUCK18
Vboot = 0.9V
IOUT_MAX = 3.2A
OFF in SLP_SMC

L7820 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883

SPMU_BUCK2_LX0	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	F20 / F19	BUCK2_LX0

=PP0V95_S2SW_VDD2L_REG (36 40 139)

R7820 0 1/20W MF 0201 5% (37 38 39 44 64) — SPMU_BUCK2_FB (130) — H17 — BUCK2_FB
VSS_ANA_SPMU — G17 — VSS_A_BUCK2
SPMU_BUCK2_FB_R — XW7820 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, NO_XNET_CONNECTION=1 — =PP0V95_S2SW_VDD2L_FB (139) OFF in SLP_SMC

System BUCK19
Vboot = 1.8V
IOUT_MAX = 3.4A

L7830 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883

SPMU_BUCK3_LX0	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 DIDT=TRUE SWITCH_NODE=TRUE	H20 / H19	BUCK3_LX0

=PP1V8_S2_REG (36 40 135 139)

R7830 0 1/20W MF 0201 5% (37 38 39 44 64) — SPMU_BUCK3_FB (130) — K17 — BUCK3_FB
VSS_ANA_SPMU — J17 — VSS_A_BUCK3
SPMU_BUCK3_FB_R — XW7830 SHORT-16L-0.1MM-SM — NO_XNET_CONNECTION=1 — =PP1V8_S2_FB (139)

System BUCK14
Vboot = 1.05V
IOUT_MAX = 15A
OFF in SLP_SMC

L7840 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
L7841 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887
L7842 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887
L7843 0.15UH-20%-8.8A-0.015OHM — PIA20161B 152S00887

SPMU_BUCK4_LX0	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	N3 / N2 / N1	BUCK4_LX0
SPMU_BUCK4_LX1	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	L3 / L2 / L1	BUCK4_LX1
SPMU_BUCK4_LX2	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	J3 / J2 / J1	BUCK4_LX2
SPMU_BUCK4_LX3	SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 DIDT=TRUE	G3 / G2 / G1	BUCK4_LX3

=PPVDD2H0_S2SW_REG (36 40 139)

R7840 0 1/20W MF 0201 5% (37 38 39 44 64) — SPMU_BUCK4_FB (130) — M5 — BUCK4_FB
VSS_ANA_SPMU — H5 — VSS_A_BUCK4
SPMU_BUCK4_FB_R — XW7840 SHORT-16L-0.1MM-SM — PLACE_NEAR=U6600:10MM, NO_XNET_CONNECTION=1 — =PPVDD2H0_S2SW_FB (139)

Iout-max is based on PMIC datasheet 1v3
Vboot is based on AM OTP (* indicates 0V initial boot)
<<< Many Vboot are not updated in BM3, due to SOC bincut alignment >>>
<<< Refer to OTP source for details >>>

BOM_COST_GROUP=SOC POWER

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Apple Inc.

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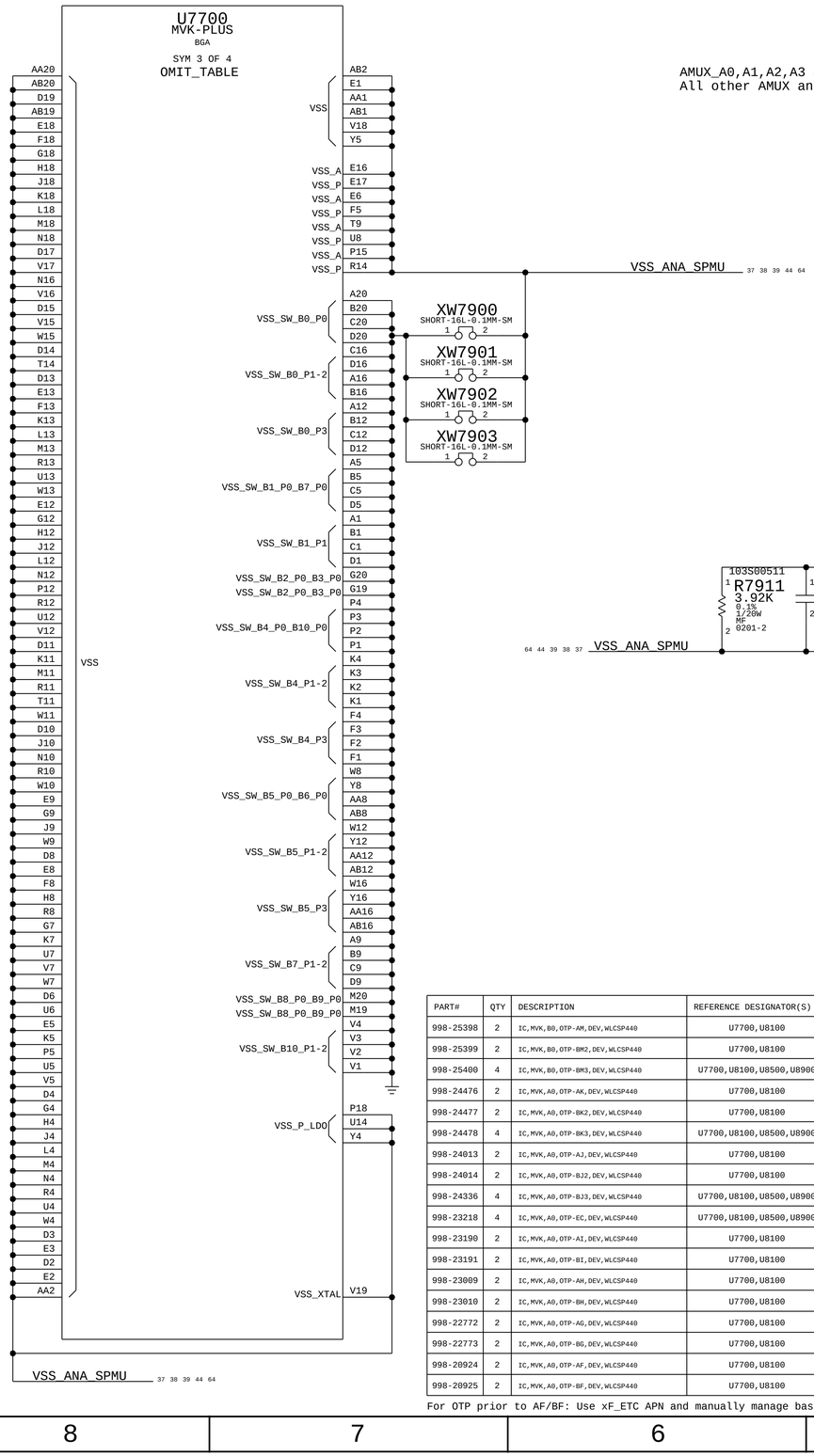
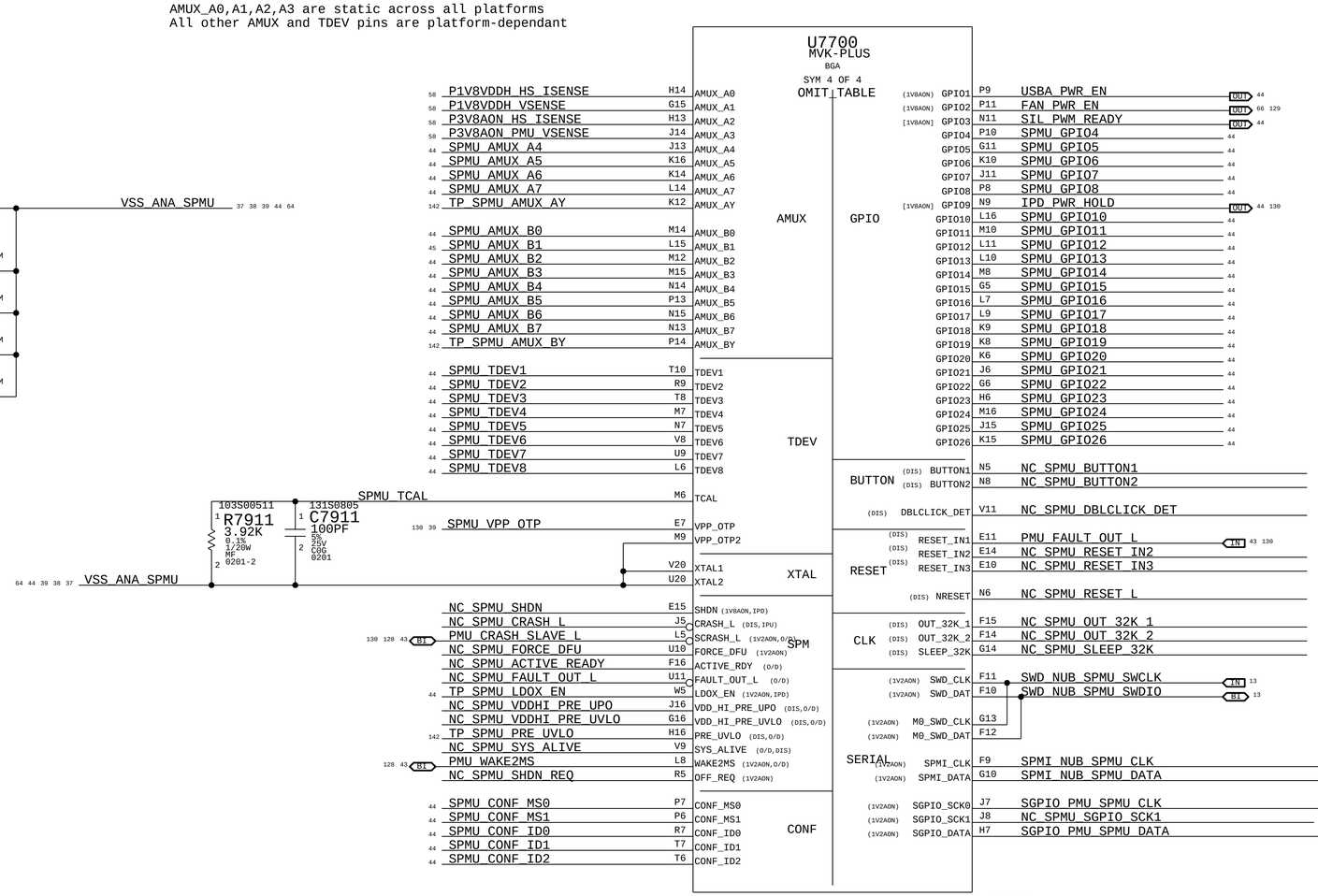
*** OK2INTEGRATE ***

TODO: XW's are only for 16L boards. TBD how to manage this in a ref-schematic



AMUX_A0,A1,A2,A3 are static across all platforms
All other AMUX and TDEV pins are platform-dependant



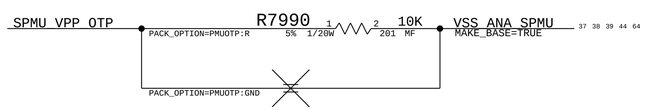
(Pin notes) are based on OTP version AM/BM
https://seg-docs.csg.apple.com/projects/maverick/release/OTP/

[Pin notes] are based on SW Overrides
J314: rdar://problem/58535481
J316: rdar://problem/61525321
J375: rdar://problem/69103874
J374: rdar://problem/59234559

GPIO without (OTP notes) are Input/IPD/1V8AON
GPIO without [SW notes] are left in their OTP state
GPIO that are unused per project are left in their OTP state

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-25398	2	IC,MVK,B0,OTP-AM,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AM
998-25399	2	IC,MVK,B0,OTP-BM2,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BM2
998-25400	4	IC,MVK,B0,OTP-BM3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:BM3
998-24476	2	IC,MVK,A0,OTP-AK,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AK
998-24477	2	IC,MVK,A0,OTP-BK2,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BK2
998-24478	4	IC,MVK,A0,OTP-BK3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:BK3
998-24013	2	IC,MVK,A0,OTP-AJ,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AJ
998-24014	2	IC,MVK,A0,OTP-BJ2,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BJ2
998-24336	4	IC,MVK,A0,OTP-BJ3,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:BJ3
998-23218	4	IC,MVK,A0,OTP-EC,DEV,WLCSP440	U7700,U8100,U8500,U8900	CRITICAL	MVK_OTP:EC
998-23190	2	IC,MVK,A0,OTP-AI,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AI
998-23191	2	IC,MVK,A0,OTP-BI,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BI
998-23009	2	IC,MVK,A0,OTP-AH,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AH
998-23010	2	IC,MVK,A0,OTP-BH,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BH
998-22772	2	IC,MVK,A0,OTP-AG,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AG
998-22773	2	IC,MVK,A0,OTP-BG,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BG
998-20924	2	IC,MVK,A0,OTP-AF,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:AF_ETC
998-20925	2	IC,MVK,A0,OTP-BF,DEV,WLCSP440	U7700,U8100	CRITICAL	MVK_OTP:BF_ETC

For OTP prior to AF/BF: Use xF_ETC APN and manually manage based on MPN



BOM_COST_GROUP=SOC POWER

PAGE TITLE: PMIC SLAVE GPIO & GND

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*** OK2INTEGRATE ***

MASTER

138 42 36 =PPVDD_ECPU_AWAKE_REG
C8003 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8002 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8001 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8000 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 0

138 42 36 =PPVDD_GPU_BMPR_S1_REG
C8013 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8012 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8011 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8010 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 1

138 42 36 =PPVDD_ECPU_SRAM_AWAKE_REG
C8023 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8022 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8021 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8020 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 2

138 42 36 =PP1V8_S2SW_REG
C8033 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8032 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8031 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8030 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 3

138 42 36 =PPVDD2H1_S2SW_REG
C8043 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8042 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8041 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8040 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 4

138 42 36 =PPVDD_AVEMSR_AWAKESW_REG
C8053 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8052 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8051 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8050 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 5

138 42 36 =PPVDD_AMPH1_S2SW_REG
C8063 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8062 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8061 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8060 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 6

138 42 36 =PP0V81_S1_SRAM_REG
C8073 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8072 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8071 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8070 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 7

138 135 42 36 =PP1V2_S2_REG
C8088 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C8087 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C8086 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C8085 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C8084 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C8083 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8082 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8081 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8080 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 8
(C8088–C8084: OMIT_TABLE)

138 42 36 =PPVDD_FIXED_S1_REG
C8093 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8092 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8091 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C8090 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 9

138 42 36 =PP0V575_S1_VDDQ1_REG
C80A3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80A2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80A1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80A0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 10

SLAVE

139 38 36 =PPVDD_DCS_S1_REG
C80B3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80B2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80B1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80B0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 0

139 38 36 =PP0V575_S1_VDDQ0_REG
C80C3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80C2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80C1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80C0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 1

139 38 36 =PP0V95_S2SW_VDD2L_REG
C80D3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80D2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80D1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80D0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 2

139 135 38 36 =PP1V8_S2_REG
C80E9 20UF 20% 2.5V X6S-CERM 0402-COMBO 138S00035 | C80E8 20UF 20% 2.5V X6S-CERM 0402-COMBO 138S00035 | C80E7 20UF 20% 2.5V X6S-CERM 0402-COMBO 138S00035 | C80E6 20UF 20% 2.5V X6S-CERM 0402-COMBO 138S00035 | C80E5 20UF 20% 2.5V X6S-CERM 0402-COMBO 138S00035 | C80E4 20UF 20% 2.5V X6S-CERM 0402-COMBO 138S00035 (NOSTUFF) | C80E3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80E2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80E1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80E0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 3
(C80E9–C80E5: OMIT_TABLE)

139 38 36 =PPVDD2H0_S2SW_REG
C80F3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80F2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80F1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80F0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 4

139 38 36 =PPVDD_SOC_S1_REG
C80G3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80G2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80G1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80G0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 5

139 38 36 =PP0V855_S2_VDDCIO_REG
C80H3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80H2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80H1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80H0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 6

139 38 =PPVDD_DISP2_AWAKESW_REG
C80I3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80I2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80I1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80I0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 7
BOMOPTION=PMU_DISP2:Y
PACK_OPTION=PMU_DISP2:Y
PACK_IGNORE=TRUE

139 135 38 36 =PP1V225_AWAKE_REG
C80J8 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C80J7 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C80J6 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C80J5 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C80J4 15UF 20% 2.5V X6S 0402-COMBO1 998-22969 | C80J3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80J2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80J1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80J0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 8
(C80J8–C80J4: OMIT_TABLE)

139 38 36 =PPVDD_AMPH0_S2SW_REG
C80K3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80K2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80K1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80K0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 9

139 38 36 =PPVDD_DISP_AWAKESW_REG
C80L3 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80L2 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80L1 2.2UF 10% 10V X6S-CERM 0402 138S00041 | C80L0 2.2UF 10% 10V X6S-CERM 0402 138S00041 — 10

Output Desense Caps to be drawn on project-specific page(s):
1x each 3pF+12pF for 1/2phase Buck: 1/2/3/6/8/9/10_M
2x each 3pF+12pF for 3/4-phase Buck: 0/4/5/7/10_S

BOM_COST_GROUP=SOC POWER

PAGE TITLE: PMIC BUCK OUTPUT CAPS

Apple Inc.

DRAWING NUMBER: 051-05641 | SIZE: D
REVISION: 6.33.0
BRANCH:
PAGE: 80 OF 999
SHEET: 40 OF 155

*** OK2INTEGRATE ***

Place these caps on opposite side of PMU
Placement strategy varies by program

C812A 2.2UF 20% 6.3V X6S 0201
C812B 2.2UF 20% 6.3V X6S 0201
C812C 2.2UF 20% 6.3V X6S 0201
C812D 2.2UF 20% 6.3V X6S 0201
C812E 2.2UF 20% 6.3V X6S 0201
C812F 2.2UF 20% 6.3V X6S 0201
C812G 2.2UF 20% 6.3V X6S 0201
C812H 2.2UF 20% 6.3V X6S 0201
C812I 2.2UF 20% 6.3V X6S 0201

C8120 1UF 20% 6.3V X6S-CERM 0201
C8121 1UF 20% 6.3V X6S-CERM 0201
C8122 1UF 20% 6.3V X6S-CERM 0201
C8123 1UF 20% 6.3V X6S-CERM 0201
C8124 1UF 20% 6.3V X6S-CERM 0201
C8125 1UF 20% 6.3V X6S-CERM 0201
C8126 1UF 20% 6.3V X6S-CERM 0201
C8127 1UF 20% 6.3V X6S-CERM 0201
C8128 1UF 20% 6.3V X6S-CERM 0201

BUCK0,PH0 D20,C20,B20,A20
BUCK0,PH0/1 C18,B18,A18
BUCK1,PH0/1/2 B16,C16,B15,A16
BUCK0,PH2/3 C14,B14,A14
BUCK0,PH3 B13,C13,A13
BUCK1,PH2/3 C12,B12,A12
BUCK1,PH1 C11,B11,A11
BUCK7,PH1/0 C9,B9,A9
BUCK7,PH2/3 D9,C9,B9,A9
BUCK7,PH3/0 C7,B7,A7
BUCK7,PH0 & BUCK1,PH0 B5,C5,B5,A5
BUCK1,PH0/1 C3,B3,A3
BUCK1,PH1 B1,C1,B1,A1

Pin A1
Bottom View

136 44 41 =PP3V8_AON_MPMU

C8130 2.2UF 20% 6.3V X6S 0201
C8131 2.2UF 20% 6.3V X6S 0201
C8132 2.2UF 20% 6.3V X6S 0201
C8133 2.2UF 20% 6.3V X6S 0201
C8134 1UF 20% 6.3V X6S-CERM 0201
C8135 1UF 20% 6.3V X6S-CERM 0201
C8136 1UF 20% 6.3V X6S-CERM 0201
C813A 2.2UF 20% 6.3V X6S 0201
C813B 2.2UF 20% 6.3V X6S 0201
C813C 2.2UF 20% 6.3V X6S 0201
C813D 2.2UF 20% 6.3V X6S 0201
C813E 2.2UF 20% 6.3V X6S 0201
C813F 2.2UF 20% 6.3V X6S 0201
C813G 2.2UF 20% 6.3V X6S 0201

BUCK4,PH3 F4,F3,F2,F1
BUCK4,PH3/2 H3,H2,H1
BUCK4,PH2/1 K4,K3,K2,K1
BUCK4,PH1/0 M3,M2,M1
BUCK4,PH0 & BUCK10,PH0 P4,P3,P2,P1
BUCK10,PH0/1 T3,T2,T1
BUCK10,PH1/2 V4,V3,V2,V1
BUCK10,PH2 Y3,Y2,Y1

C81AA 12PF 5% 25V NP0-C0G 0201
C81AB 2.2UF 20% 6.3V X6S 0201
C81AC 2.2UF 20% 6.3V X6S 0201
C81AD 2.2UF 20% 6.3V X6S 0201
C81AE 2.2UF 20% 6.3V X6S 0201
C81AF 12PF 5% 25V NP0-C0G 0201
C81A0 12PF 5% 25V NP0-C0G 0201
C81A1 1UF 20% 6.3V X6S-CERM 0201
C81A2 1UF 20% 6.3V X6S-CERM 0201
C81A3 1UF 20% 6.3V X6S-CERM 0201
C81A4 1UF 20% 6.3V X6S-CERM 0201
C81A5 12PF 5% 25V NP0-C0G 0201

BUCK2 E20,E19
BUCK2 & BUCK3 G20,G19
BUCK3 J20,J19
BUCK8 K20,K19
BUCK8 & BUCK9 M20,M19
BUCK9 P20,P19

136 44 41 =PP3V8_AON_MPMU

C8140 1UF 20% 6.3V X6S-CERM 0201
C8141 1UF 20% 6.3V X6S-CERM 0201
C8142 1UF 20% 6.3V X6S-CERM 0201
C8143 1UF 20% 6.3V X6S-CERM 0201
C8144 1UF 20% 6.3V X6S-CERM 0201
C814A 2.2UF 20% 6.3V X6S 0201
C814B 2.2UF 20% 6.3V X6S 0201
C814C 2.2UF 20% 6.3V X6S 0201
C814D 2.2UF 20% 6.3V X6S 0201
C814E 2.2UF 20% 6.3V X6S 0201

BUCK5,PH3 AB15,AA15,Y15,W16
BUCK5,PH2/2 AB14,AA14,Y14
BUCK5,PH2/1 AB12,AA12,Y12,W12
BUCK5,PH1/0 AB10,AA10,Y10
BUCK5,PH0 & BUCK6 AB9,AA9,Y9,W8
BUCK6 AB6,AA6,Y6

Place these caps on PMU side as drawn here

U8100
MVK-PLUS
BGA
SYM 1 OF 4
OMIT_TABLE

BUCK INPUT POWER

A18 B18 C18 VDD_BUCK0_01
A14 B14 C14 VDD_BUCK0_23
A3 B3 C3 VDD_BUCK1
E20 E19 VDD_BUCK2
J20 J19 VDD_BUCK3
M3 M2 M1 VDD_BUCK4_01
H3 H2 H1 VDD_BUCK4_23
Y10 AA10 AB10 VDD_BUCK5_01
Y14 AA14 AB14 VDD_BUCK5_23
Y6 AA6 AB6 VDD_BUCK6
A7 B7 C7 VDD_BUCK7_01
A11 B11 C11 VDD_BUCK7_2
K20 K19 VDD_BUCK8
P20 P19 VDD_BUCK9
T3 T2 T1 VDD_BUCK10_01
Y3 Y2 Y1 VDD_BUCK10_2

H15 G8 R6 R17 VDD_MAIN
(PRE_UVLO@3.35V) (CRASH@3.05V)
P16 VDD_MAIN_SNS =VDD_MAIN_SNS_MPMU 44
(VDDHI_PRE_UVLO@1.6V) (CRASH@1.5V)
V14 VDDHI PMU VDDHI
V13 VDD3V3 =PP3V3_S2_UPC_MPMU 138
H9 VDD1V8 =PP1V8_S2_MPMU 43 139
H11 VDD1V2_0 =PP1V2_AON_MPMU 43 44 138
H10 VDD1V2_1 =PP1V2_S2_MPMU 41 43 44 138

C8100 10UF 20% 6.3V CERM-X6S 0402
C8101 10UF 20% 6.3V CERM-X6S 0402
C8102 10UF 20% 6.3V CERM-X6S 0402
C8103 10UF 20% 6.3V CERM-X6S 0402
C8104 10UF 20% 6.3V CERM-X6S 0402
C8105 10UF 20% 6.3V CERM-X6S 0402
C8106 10UF 20% 6.3V CERM-X6S 0402
C8107 10UF 20% 6.3V CERM-X6S 0402
C8108 10UF 20% 6.3V CERM-X6S 0402
C8109 10UF 20% 6.3V CERM-X6S 0402
C8110 10UF 20% 6.3V CERM-X6S 0402
C8111 10UF 20% 6.3V CERM-X6S 0402
C8112 10UF 20% 6.3V CERM-X6S 0402
C8113 10UF 20% 6.3V CERM-X6S 0402
C8114 10UF 20% 6.3V CERM-X6S 0402
C8115 10UF 20% 6.3V CERM-X6S 0402
C8116 10UF 20% 6.3V CERM-X6S 0402
C8117 10UF 20% 6.3V CERM-X6S 0402

136 44 41 =PP3V8_AON_MPMU
C811A 12PF 5% 25V NP0-C0G 0201
C811B 12PF 5% 25V NP0-C0G 0201

XW8170
SHORT-18L-0.1MM-SM
PPBUS_AON_MPMU =PPBUS_AON_MPMU 135
VOLTAGE=13.05V
MIN_LINE_WIDTH=0.0000
MIN_NECK_WIDTH=0.0000

OMIT_TABLE
R8170 200K 1% 1/20W MF 201
OMIT_TABLE
R8171 200K 1% 1/20W MF 201
NOSTUFF
C8170 0.1UF 20% 16V X6S 0201

PP1V5_AON_VRTC_MPMU
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
T17 VRTC
U17 VIN_BBAT
AA19 VPUMP
W19 Y19 VBUCK_SW0
AA18 AB18 VBUCK_SW1
W18 Y18 VBUCK_SW2

OTHER POWER
SWITCHES
LDOS

VREF_1V2 T13 MPMU_VREF1V2
IREF T12 MPMU_IREF
118S0176 R8101 200K 1% 1/20W MF 201
132S0395 C8151 0.1UF 10% 6.3V X6S 0201
VSS_ANA_MPMU 41 42 43 44 64

W20 Y20 BUCK_SW0 (500mA-max) (23mR-max) =PP1V2_S2_CLVR_VDDIO_FET 41 138
AA17 AB17 BUCK_SW1 (500mA-max) (23mR-max) =PPVOUT_SW1_MPMU_FET 41 44
W17 Y17 BUCK_SW2 (500mA-max) (23mR-max) =PPVOUT_SW2_MPMU_FET 41 44

AB3 VIN_LDO0 VLDO0 (400mA-max) =PPVOUT_LDO0_MPMU_REG 41 44
R20 VIN_LDO1 VLDO1 (300mA-max) =PP3V3_S2_UPC_REG 41 135 138
R19 VIN_LDO2 VLDO2 (300mA-max) =PP1V8_S2SW_CLVR_VDDC1_MPMU_REG 41 138
R18 VIN_LDO3 VLDO3 (300mA-max) =PP1V8_AWAKE_PCC_REG 41 44
AB5 VIN_LDO4 VLDO4 (300mA-max) =PP3V3_AON_REG 41 135
AB4 VIN_LDO5 VLDO5 (400mA-max) =PP0V8_S2_CLVR_VDDDIG_REG 41 138
U18 VIN_LDO6 VLDO6 (10mA-max) =PPVOUT_LDO6_MPMU_REG 41 44
U16 VIN_LDO1V8 VLDO1V8 (50mA-max) =PP1V8_AON_REG 41 135 138
T16 VIN_LDO1V2 VLDO1V2 (50mA-max) =PP1V2_AON_REG 41 138
R16 VIN_VCORE VCORE PP1V5_AON_VCORE_MPMU 132S0395 C8180 0.1UF 10% 6.3V X6S 0201
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

All VIN_LDOx and VBUCK_SWx pins must be powered or GND'd. Do not float!

64 44 43 42 41 VSS_ANA_MPMU
MAKE_BASE=TRUE

132S0395 C8150 0.1UF 10% 6.3V X6S 0201
MPMU_VIN_BBAT
132S0395 C8153 0.1UF 10% 6.3V X6S 0201
PACK_IGNORE=TRUE
PACK_OPTION=PMU_BBAT:Y
PACK_OPTION=PMU_BBAT:N

132S00070 C8152 0.01UF 10% 25V X7R 0201
VOLTAGE=4.9V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
Must be ON to use any BUCK_SW

138 44 43 41 =PP1V2_S2_MPMU
44 =PPVIN_SW1_MPMU
44 =PPVIN_SW2_MPMU
44 =PPVIN_LDO0_MPMU
136 44 41 =PP3V8_AON_MPMU
136 44 41 =PP3V8_AON_MPMU
44 =PP3V8_AON_MPMU_LDO3
136 =PP3V8_AON_MPMU_LDO4
138 44 43 41 =PP1V2_S2_MPMU
44 =PPVIN_LDO6_MPMU
136 44 41 =PP3V8_AON_MPMU
136 44 41 =PP3V8_AON_MPMU
136 44 41 =PP3V8_AON_MPMU

=PP1V2_S2_CLVR_VDDIO_FET 41 138
=PPVOUT_SW1_MPMU_FET 41 44
=PPVOUT_SW2_MPMU_FET 41 44
=PPVOUT_LDO0_MPMU_REG 41 44

138S00040 C8190 1UF 20% 6.3V X6S-CERM 0201
138S00040 C8191 1UF 20% 6.3V X6S-CERM 0201
PACK_IGNORE=TRUE
PACK_OPTION=MPMU_SW1
138S00040 C8192 1UF 20% 6.3V X6S-CERM 0201
PACK_OPTION=MPMU_SW2
PACK_IGNORE=TRUE
138S00073 C8160 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=MPMU_LDO0
PACK_IGNORE=TRUE

=PP3V3_S2_UPC_REG 41 135 138
=PP1V8_S2SW_CLVR_VDDC1_MPMU_REG 41 138
=PP1V8_AWAKE_PCC_REG 41 44
=PP3V3_AON_REG 41 135

138S00073 C8161 10UF 20% 6.3V CER-X6S 0402
138S00073 C8162 10UF 20% 6.3V CER-X6S 0402
138S00073 C8163 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=MPMU_LDO3
PACK_IGNORE=TRUE
138S00073 C8164 10UF 20% 6.3V CER-X6S 0402
PACK_OPTION=MPMU_LDO4

=PP0V8_S2_CLVR_VDDDIG_REG 41 138
=PPVOUT_LDO6_MPMU_REG 41 44
=PP1V8_AON_REG 41 135 138
=PP1V2_AON_REG 41 138

138S00329 C8165 4UF 20% 2.5V X6S 0201
138S00102 C8166 1UF 10% 16V CER-X6S 0402
138S00102 C8169 1UF 10% 16V CER-X6S 0402
PACK_OPTION=MPMU_LDO6
PACK_IGNORE=TRUE
138S00044 C8167 1UF 20% 10V X6S-CERM 0201
138S00044 C8168 1UF 20% 10V X6S-CERM 0201

Buck Numbering

System Virtual #	Physical # 0	1	2	3	4	5	6	7	8	9	10	System Virtual #
0	M											0
1		M										1
2			M									2
3				M								3
4					M							4
5						M						5
6							M					6
7								M				7
8									M			8
9										M		9
10											M	10
11						5						11
12								5				12
13		5										13
14				5								14
15							5					15
16						5						16
17	5											17
18			5									18
19				5								19
20											5	20
21											5	21

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
103S00496	1	RES,TK,1.07MOHM,0.1%,1/20W,0201	R8170	CRITICAL	PBUS:3S
103S00497	1	RES,TK,291KOHM,0.1%,1/20W,0201	R8171	CRITICAL	PBUS:3S
103S00498	1	RES,TK,1.1MOHM,0.1%,1/20W,0201	R8170	CRITICAL	PBUS:12VDCIN
103S00499	1	RES,TK,237KOHM,0.1%,1/20W,0201	R8171	CRITICAL	PBUS:12VDCIN

<== For 3S BATTERY (7V UVLO)
VDDHI = 1.49669V @ 7V-PBUS
VDDHI = 1.5V @ 7.0155V-PBUS

<== For 12V DCIN (8.46V UVLO)
VDDHI = 1.49964V @ 8.46V-PBUS
VDDHI = 1.5V @ 8.46203V-PBUS

BOM_COST_GROUP=SOC POWER

PAGE TITLE
PMIC MASTER VIN/LDO/SW

Apple Inc.

DRAWING NUMBER 051-05641
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REVISION 6.33.0
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*** OK2INTEGRATE ***

U8100
MVK-PLUS
BGA
SYM 2 OF 4
OMIT_TABLE

System BUCK5
Vboot = *
Iout_Max = 19.2A

=PPVDD_AVEMSR_AWAKESW_REG

L8250 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
MPMU_BUCK5_LX0 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
Y9, AA9, AB9 → BUCK5_LX0

L8251 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK5_LX1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
Y11, AA11, AB11 → BUCK5_LX1

L8252 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK5_LX2 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
Y13, AA13, AB13 → BUCK5_LX2

L8253 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK5_LX3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
Y15, AA15, AB15 → BUCK5_LX3

XW8250 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
=PPVDD_AVEMSR_AWAKESW_FB — MPMU_BUCK5_FB_R
R8250 0 1/20W MF 0201 5%
MPMU_BUCK5_FB — V10 → BUCK5_FB
VSS_ANA_MPMU — W14 → VSS_A_BUCK5

System BUCK6
Vboot = 1.121875V
Iout_Max = 2.1A
OFF in SLP_SMC

=PPVDD_AMPH1_S2SW_REG

L8260 0.47UH-20%-4A-0.027OHM — 2012 152S00885
MPMU_BUCK6_LX0 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
Y7, AA7, AB7 → BUCK6_LX0

XW8260 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
=PPVDD_AMPH1_S2SW_FB — MPMU_BUCK6_FB_R
R8260 0 1/20W MF 0201 5%
MPMU_BUCK6_FB — V6 → BUCK6_FB
VSS_ANA_MPMU — W6 → VSS_A_BUCK6

System BUCK7
Vboot = 0.815625V
Iout_Max = 9A

=PP0V81_S1_SRAM_REG

L8270 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
MPMU_BUCK7_LX0 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A6, B6, C6 → BUCK7_LX0

L8271 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK7_LX1 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A8, B8, C8 → BUCK7_LX1

L8272 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK7_LX2 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A10, B10, C10 → BUCK7_LX2

XW8270 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
=PP0V81_S1_SRAM_FB — MPMU_BUCK7_FB_R
R8270 0 1/20W MF 0201 5%
MPMU_BUCK7_FB — F7 → BUCK7_FB
VSS_ANA_MPMU — D7 → VSS_A_BUCK7

System BUCK8
Vboot = 1.225V
Iout_Max = 3.2A

=PP1V2_S2_REG

L8280 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
MPMU_BUCK8_LX0 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
L20, L19 → BUCK8_LX0

XW8280 SHORT-16L-0.1MM-SM — NO_XNET_CONNECTION=1
=PP1V2_S2_FB — MPMU_BUCK8_FB_R
R8280 0 1/20W MF 0201 5%
MPMU_BUCK8_FB — M17 → BUCK8_FB
VSS_ANA_MPMU — L17 → VSS_A_BUCK8

System BUCK9
Vboot = 0.840625V
Iout_Max = 2.1A

=PPVDD_FIXED_S1_REG

L8290 0.47UH-20%-4A-0.027OHM — 2012 152S00885
MPMU_BUCK9_LX0 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
N20, N19 → BUCK9_LX0

XW8290 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
=PPVDD_FIXED_S1_FB — MPMU_BUCK9_FB_R
R8290 0 1/20W MF 0201 5%
MPMU_BUCK9_FB — P17 → BUCK9_FB
VSS_ANA_MPMU — N17 → VSS_A_BUCK9

System BUCK10
Vboot = 0.575V
Iout_Max = 5A

=PP0V575_S1_VDDQ1_REG

L82A0 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
MPMU_BUCK10_LX0 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
R3, R2, R1 → BUCK10_LX0

L82A1 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK10_LX1 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
U3, U2, U1 → BUCK10_LX1

NC W3, NC W2, NC W1 → BUCK10_LX2

XW82A0 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
=PP0V575_S1_VDDQ1_FB — MPMU_BUCK10_FB_R
R82A0 0 1/20W MF 0201 5%
MPMU_BUCK10_FB — T5 → BUCK10_FB
VSS_ANA_MPMU — T4 → VSS_A_BUCK10

System BUCK0
Vboot = 0.63125V
Iout_Max = 19.2A

=PPVDD_ECPU_AWAKE_REG

L8200 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
MPMU_BUCK0_LX0 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A19, B19, C19 ← BUCK0_LX0

L8201 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK0_LX1 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A17, B17, C17 ← BUCK0_LX1

L8202 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK0_LX2 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A15, B15, C15 ← BUCK0_LX2

L8203 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK0_LX3 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A13, B13, C13 ← BUCK0_LX3

R8200 0 1/20W MF 0201 5%
MPMU_BUCK0_FB — F17 ← BUCK0_FB
VSS_ANA_MPMU — D18 ← VSS_A_BUCK0
XW8200 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
MPMU_BUCK0_FB_R — =PPVDD_ECPU_AWAKE_FB

System BUCK1
Vboot = 0.91875V
Iout_Max = 5.4A

=PPVDD_GPU_BMPR_S1_REG

L8210 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
MPMU_BUCK1_LX0 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A4, B4, C4 ← BUCK1_LX0

L8211 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK1_LX1 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
A2, B2, C2 ← BUCK1_LX1

R8210 0 1/20W MF 0201 5%
MPMU_BUCK1_FB — F6 ← BUCK1_FB
VSS_ANA_MPMU — E4 ← VSS_A_BUCK1
XW8210 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
MPMU_BUCK1_FB_R — =PPVDD_GPU_BMPR_S1_FB

System BUCK2
Vboot = 0.765625V
Iout_Max = 2.1A

=PPVDD_ECPU_SRAM_AWAKE_REG

L8220 0.47UH-20%-4A-0.027OHM — 2012 152S00885
MPMU_BUCK2_LX0 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, DIDT=TRUE, SWITCH_NODE=TRUE
F20, F19 ← BUCK2_LX0

R8220 0 1/20W MF 0201 5%
MPMU_BUCK2_FB — H17 ← BUCK2_FB
VSS_ANA_MPMU — G17 ← VSS_A_BUCK2
XW8220 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
MPMU_BUCK2_FB_R — =PPVDD_ECPU_SRAM_AWAKE_FB

System BUCK3
Vboot = 1.8V
Iout_Max = 3.4A
OFF in SLP_SMC

=PP1V8_S2SW_REG

L8230 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
MPMU_BUCK3_LX0 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
H20, H19 ← BUCK3_LX0

R8230 0 1/20W MF 0201 5%
MPMU_BUCK3_FB — K17 ← BUCK3_FB
VSS_ANA_MPMU — J17 ← VSS_A_BUCK3
XW8230 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
MPMU_BUCK3_FB_R — =PP1V8_S2SW_FB

System BUCK4
Vboot = 1.05V
Iout_Max = 15A
OFF in SLP_SMC

=PPVDD2H1_S2SW_REG

L8240 1.0UH-20%-4A-0.038OHM — PIKA20161B-COMBO 152S00883
MPMU_BUCK4_LX0 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
N3, N2, N1 ← BUCK4_LX0

L8241 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK4_LX1 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
L3, L2, L1 ← BUCK4_LX1

L8242 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK4_LX2 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
J3, J2, J1 ← BUCK4_LX2

L8243 0.15UH-20%-8.8A-0.015OHM — PIIA20161B 152S00887
MPMU_BUCK4_LX3 — SWITCH_NODE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, DIDT=TRUE
G3, G2, G1 ← BUCK4_LX3

R8240 0 1/20W MF 0201 5%
MPMU_BUCK4_FB — M5 ← BUCK4_FB
VSS_ANA_MPMU — H5 ← VSS_A_BUCK4
XW8240 SHORT-16L-0.1MM-SM — PLACE_NEAR=U0600:10MM, NO_XNET_CONNECTION=1
MPMU_BUCK4_FB_R — =PPVDD2H1_S2SW_FB

Iout-max is based on PMIC datasheet 1v3
Vboot is based on AM OTP (* indicates 0V initial boot)
<<< Many Vboot are not updated in BM3, due to SOC bincut alignment >>>
<<< Refer to OTP source for details >>>

BOM_COST_GROUP=SOC POWER

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*** OK2INTEGRATE ***

TODO: XW's are only for 16L boards. TBD how to manage this in a ref-schematic

AMUX_A0,A1 are static across all platforms
All other AMUX and TDEV pins are platform-dependant

U8100
MVK-PLUS
BGA
SYM 3 OF 4
OMIT_TABLE

VSS: AA20, AB20, D19, AB19, E18, F18, G18, H18, J18, K18, L18, M18, N18, D17, V17, N16, D16, V15, W15, D14, T14, D13, E13, F13, K13, L13, M13, R13, U13, W13, E12, G12, H12, J12, L12, N12, P12, R12, U12, V12, D11, K11, M11, R11, T11, W11, D10, J10, N10, R10, W10, E9, G9, J9, W9, D8, E8, F8, H8, R8, G7, K7, U7, V7, W7, D6, U6, E5, K5, P5, U5, V5, D4, G4, H4, J4, L4, M4, N4, R4, U4, W4, D3, E3, D2, E2, AA2

VSS_A: AB2, E1, AA1, V18, Y5
VSS_P: E16, E17
VSS_A: E6, F5, T9, U8, P15
VSS_P: R14
VSS_SW_B0_P0: A20, B20, C20, D20
VSS_SW_B0_P1-2: C16, D16, A16, B16
VSS_SW_B0_P3: A12, B12, C12, D12
VSS_SW_B1_P0_B7_P0: A5, B5, C5, D5
VSS_SW_B1_P1: A1, B1, C1, D1
VSS_SW_B2_P0_B3_P0: G20, G19
VSS_SW_B4_P0_B10_P0: P4, P3, P2, P1
VSS_SW_B4_P1-2: K4, K3, K2, K1
VSS_SW_B4_P3: F4, F3, F2, F1
VSS_SW_B5_P0_B6_P0: W8, Y8, AA8, AB8
VSS_SW_B5_P1-2: W12, Y12, AA12, AB12
VSS_SW_B5_P3: W16, Y16, AA16, AB16
VSS_SW_B7_P1-2: A9, B9, C9, D9
VSS_SW_B8_P0_B9_P0: M20, M19
VSS_SW_B8_P0_B9_P0: V4, V3
VSS_SW_B10_P1-2: V2, V1
VSS_P_LDO: P18, U14, Y4
VSS_XTAL: V19

VSS_ANA_MPMU 41 42 43 44 64

VSS_ANA_MPMU 41 42 43 44 64

XW8300 SHORT-16L-0.1MM-SM
XW8301 SHORT-16L-0.1MM-SM
XW8302 SHORT-16L-0.1MM-SM
XW8303 SHORT-16L-0.1MM-SM

64 44 43 42 41 VSS_ANA_MPMU — 103S00511 R8311 3.92K 0.1% 1/20W MF 0201-2 — 131S0805 C8311 100PF 5% 25V C0G 0201 — MPMU_VPP_OTP 130 43

U8100
MVK-PLUS
BGA
SYM 4 OF 4
OMIT_TABLE

AMUX
58 DCIN_ISENSE H14 AMUX_A0
130 58 DCIN_VSENSE G15 AMUX_A1
44 MPMU_AMUX_A2 H13 AMUX_A2
44 MPMU_AMUX_A3 J14 AMUX_A3
44 MPMU_AMUX_A4 J13 AMUX_A4
44 MPMU_AMUX_A5 K16 AMUX_A5
44 MPMU_AMUX_A6 K14 AMUX_A6
45 MPMU_AMUX_A7 L14 AMUX_A7
142 TP_MPMU_AMUX_AY K12 AMUX_AY
44 MPMU_AMUX_B0 M14 AMUX_B0
44 MPMU_AMUX_B1 L15 AMUX_B1
44 MPMU_AMUX_B2 M12 AMUX_B2
44 MPMU_AMUX_B3 M15 AMUX_B3
44 MPMU_AMUX_B4 N14 AMUX_B4
44 MPMU_AMUX_B5 P13 AMUX_B5
44 MPMU_AMUX_B6 N15 AMUX_B6
44 MPMU_AMUX_B7 N13 AMUX_B7
142 TP_MPMU_AMUX_BY P14 AMUX_BY

TDEV
44 MPMU_TDEV1 T10 TDEV1
44 MPMU_TDEV2 R9 TDEV2
44 MPMU_TDEV3 T8 TDEV3
44 MPMU_TDEV4 M7 TDEV4
44 MPMU_TDEV5 N7 TDEV5
44 MPMU_TDEV6 V8 TDEV6
44 MPMU_TDEV7 U9 TDEV7
44 MPMU_TDEV8 L6 TDEV8

XTAL
MPMU_TCAL M6 TCAL
130 43 MPMU_VPP_OTP E7 VPP_OTP
64 44 43 42 41 VSS_ANA_MPMU M9 VPP_OTP2
43 MPMU_XTAL1 V20 XTAL1
43 MPMU_XTAL2 U20 XTAL2

SPM
Debug Only
132 129 IN PMU_SHDN E15 SHDN (1V8AON,IPD)
130 52 51 50 43 BI PMU_CRASH_L J5 CRASH_L (1V2AON,O/D)
130 128 43 39 BI PMU_CRASH_SLAVE_L L5 SCRASH_L (1V2AON,O/D)
43 PMU_FORCE_DFU U10 FORCE_DFU (1V2AON)
131 129 128 78 69 43 5 OUT PMU_ACTIVE_READY F16 ACTIVE_RDY (O/D)
43 PMU_FAULT_OUT_R_L U11 FAULT_OUT_L (O/D)
142 TP_MPMU_LDOX_EN W5 LDOX_EN (1V2AON,IPD)
142 TP_MPMU_VDDHI_PRE_UPO J16 VDD_HI_PRE_UPO (DIS,O/D)
130 11 OUT PMU_VDDHI_UVWARN_L G16 VDD_HI_PRE_UVLO (O/D)
130 11 OUT PMU_VDDMAIN_UVWARN_L H16 PRE_UVLO (O/D)
129 110 106 101 90 83 75 43 OUT PMU_SYS_ALIVE V9 SYS_ALIVE (O/D)
128 43 39 BI PMU_WAKE2MS L8 WAKE2MS (1V2AON,O/D)
44 OUT PMU_SHDN_REQ R5 OFF_REQ (1V2AON)
To M2 SHDN (2C only)

CONF
44 MPMU_CONF_MS0 P7 CONF_MS0 (3V8AON)
44 MPMU_CONF_MS1 P6 CONF_MS1 (3V8AON)
44 MPMU_CONF_ID0 R7 CONF_ID0 (3V8AON)
44 MPMU_CONF_ID1 T7 CONF_ID1 (3V8AON)
44 MPMU_CONF_ID2 T6 CONF_ID2 (3V8AON)

GPIO
(1V8AON) GPIO1 P9 =IPD_LID_OPEN_1V8_POWER_IN_WAKE IN 44
(1V8AON,IPU)* GPIO2 P11 CHGR_AUX_OK IN 29 128 *Portables Only
[1V2S2,IPU] GPIO3 N11 CODEC_WAKE_L IN 115 128
[1V2S2,IPD] GPIO4 P10 WLBT_WAKE IN 95 96
(1V8S2)/[1V8AON,IPU]* GPIO5 G11 =IPD_WAKE_L_ENET_WAKE_L IN 44 *Portables/Desktop
(1V8S2,IPD)[1V8S2/1V8AON*] GPIO6 K10 =DP2HDMI_PWR_EN_HDMI_CEC_IRQ BI 44 *Portables/Desktop
[1V8AON,IPU] GPIO7 J11 SDCONN_STATE_CHANGE_L IN 93
[1V8AON,O/D] GPIO8 P8 HDMI_RESET_L OUT 89 129
(1V8AON) GPIO9 N9 P3V8AON_LPM OUT 33 44 130
(1V2AON) GPIO10 L16 CLVR_RESET_L OUT 50 51 52 130
(1V2AON) GPIO11 M10 P1V8VDDH_PWR_EN OUT 44 47 130
(1V2AON) GPIO12 L11 P1V8VDDH_SLP_L OUT 47 130 131
[1V8AON] GPIO13 L10 WLBT_PWR_EN OUT 44 95 96 130
[1V8AON] GPIO14 M8 =IPD_PWR_EN_ENET_PWR_EN OUT 44
[1V2S2] GPIO15 G5 SE_PWR_EN OUT 26 44 129
(1V8AON) GPIO16 L7 P3V3S2_PWR_EN OUT 44
(1V8AON) GPIO17 L9 P5VS2_PWR_EN OUT 44 130
[1V8AON] GPIO18 K9 HDMI_CECFET_EN OUT 86 129
[1V2S2] GPIO19 K8 BL_PWR_EN OUT 111 129
[1V8AON] GPIO20 K6 LCD_PWR_EN OUT 110
(1V8AON)[1V2AON,O/D] GPIO21 J6 =PVBAT_ILIMIT_L_P12VAON_PLIMIT_L OUT 11 44
[1V2S2] GPIO22 G6 BL_PMIC_PWR_EN OUT 112 129
[1V8AON] GPIO23 H6 HDMI_PWR_EN OUT 86 129
(1V8AON) GPIO24 M16 P1V8S2_PWR_EN OUT 44
(3V8AON) GPIO25 J15 P5VUSB_PWR_EN OUT 44
[1V8AON] GPIO26 K15 SD_PWR_EN OUT 94

BUTTON
(1V8AON,L) BUTTON1 N5 PMU_ONOFF_L IN 43 44 125 129 132
(1V8AON,L) BUTTON2 N8 PMU_RSLOC_RST_L IN 43 44 121 129 132
(1V2S2) DBLCLICK_DET V11 DBL_CLICK_DET OUT 6 130

RESET
(1V2S2,L) RESET_IN1 E11 SOC_WDOG_L IN 10
(1V2S2,H,IPD) RESET_IN2 E14 UPC_PMU_RESET_1V2 IN 44 130
(1V2S2,L) RESET_IN3 E10 SOC_SOCHOT_L IN 5 129
(O/D) NRESET N6 PMU_RESET_L OUT 5 10 43 128 129

CLK
(1V2AON) OUT_32K_1 F15 PMU_CLK32K_CLVR_R OUT 44
(1V2S2) OUT_32K_2 F14 PMU_CLK32K_WLBT_R OUT 44
(1V2AON) SLEEP_32K G14 PMU_CLK32K_SOC_R OUT 44

(1V2AON) SWD_CLK F11 SWD_NUB_MPMU_SWCLK IN 13
(1V2AON) SWD_DAT F10 SWD_NUB_MPMU_SWDIO BI 13
(1V2AON) M0_SWD_CLK G13
(1V2AON) M0_SWD_DAT F12

SERIAL
(1V2AON) SPMI_CLK F9 SPMI_NUB_MPMU_CLK IN 13 130
(1V2AON) SPMI_DATA G10 SPMI_NUB_MPMU_DATA BI 13 130
(1V2AON) SGPIO_SCK0 J7 SGPIO_PMU_SPMU_CLK_R OUT 44
(1V2AON) SGPIO_SCK1 J8 SGPIO_PMU_CLVR_CLK_R OUT 44
(1V2AON) SGPIO_DATA H7 SGPIO_PMU_DATA_R BI 44

=PP1V8_S2_MPMU 139 41
=PP1V8_AON_MPMU 138 44
=PP1V2_S2_MPMU 138 44 41
=PP1V225_AWAKE_MPMU 139
=PP1V2_AON_MPMU 138 44 41

PMU_CRASH_L 130 52 51 50 43 — R8312 1K 5% 1/20W MF 201
PMU_CRASH_SLAVE_L 130 128 43 39 — R8313 47K 5% 1/20W MF 201
PMU_WAKE2MS 128 43 39 — R8314 47K 5% 1/20W MF 201
PMU_ACTIVE_READY 128 78 69 43 5 131 129 — R8320 10K 5% 1/20W MF 201
PMU_RESET_L 129 128 43 10 5 — R8321 10K 5% 1/20W MF 201
PMU_ONOFF_L 129 125 44 43 132 — R8317 1K 5% 1/20W MF 201
PMU_RSLOC_RST_L 129 121 44 43 132 — R8318 10K 5% 1/20W MF 201
PMU_SYS_ALIVE 101 90 83 75 43 129 110 106 — R8319 10K 5% 1/20W MF 201

43 PMU_FAULT_OUT_R_L — R8316 0 5% 1/20W 0201 MF — NOSTUFF_PMU_FAULT_OUT_L OUT 39 130

43 PMU_FORCE_DFU — R8330 2.2K 5% 1/20W 201 MF — SOC_FORCE_DFU OUT 5 70 128 129 132

130 43 MPMU_VPP_OTP — R8390 10K 5% 1/20W 201 MF — VSS_ANA_MPMU 41 42 43 44 64
PACK_OPTION=PMUOTP:R
PACK_OPTION=PMUOTP:GND
MAKE_BASE=TRUE

(Pin notes) are based on OTP version AM/BM
https://seg-docs.csg.apple.com/projects/maverick/release/OTP/

[Pin notes] are based on SW Overrides
J314: rdar://problem/58535481
J316: rdar://problem/61525321
J375: rdar://problem/69103874
J374: rdar://problem/59234559

GPIO without (OTP notes) are Input/IPD/1V8AON
GPIO without [SW notes] are left in their OTP state
GPIO that are unused per project are left in their OTP state

64 44 43 42 41 VSS_ANA_MPMU — U8355 CRITICAL — 197S00323 32.768KHZ-20PPM-1.8V 2.5X2.0-SM
PACK_OPTION=PMU32K:OSC_QRTZ
VCC 4, OUT 3, EN/DIS 1, GND 2
132S0403 C8355 0.1UF 10% 6.3V X7R 0201
PACK_OPTION=PMU32K:OSC_QRTZ
PMUOSC_PIN1
=PP1V8_PMUOSC 135 — R8355 1K 5% 1/20W MF 201
PACK_OPTION=PMU32K:OSC_QRTZ

MPMU_XTAL_R — R8351 0 1/20W 5% MF 0201 — MPMU_XTAL2 43
Inverter Output<-> (RTC bypass)
R8350 0 1/20W 5% MF 0201 NOSTUFF NO_XNET_CONNECTION=1 — MPMU_XTAL1 43
Inverter Input->
R8352 0 5% 1/20W MF 0201 — VSS_ANA_MPMU 41 42 43 44 64

BOM_COST_GROUP=SOC POWER

PAGE TITLE
PMIC MASTER GPIO & GND

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PMU_CLK32K_WLBT_R R8410 22 PMU_CLK32K_WLBT
PMU_CLK32K_CLVR_R R8411 22 PMU_CLK32K_CLVR
PMU_CLK32K_SOC_R R8412 22 PMU_CLK32K_SOC
Termination should be resimulated per project
SGPIO_PMU_SPMU_CLK_R R8400 22 SGPIO_PMU_SPMU_CLK
SGPIO_PMU_CLVR_CLK_R R8401 22 SGPIO_PMU_CLVR_CLK
SGPIO_PMU_DATA_R R8402 22 SGPIO_PMU_DATA
C8400 56PF
C8401 56PF
C8402 56PF
=PP3V3_AON_CHGRRST R8444 0 NOSTUFF
=PP1V8_AON_CHGRRST R8445 0
PPVDD_CHGRRST
PLACE_NEAR=U8440.1:5MM
C8440 0.1UF
U8440 SLG4AP43601 STQFN
CRITICAL 343S00387
PMU_ONOFF_L
PMU_RSLOC_RST_L
CHGR_RST_IN
=PP1V2_S2_MPMU R8441 0
=PP1V2_AON_MPMU R8442 0 NOSTUFF
PP1V2_UPCPMURESET
PLACE_NEAR=U8441.1:5MM
C8441 0.1UF
UPC_PMU_RESET_3V3
R8440 10K
U8441 SN74AUP1G32 SOT553 311S00301
UPC_PMU_RESET_1V2_R R8443 0 UPC_PMU_RESET_1V2
SPMU_GPIO4 MAKE_BASE=TRUE NC_SPMU_GPIO4
SPMU_GPIO5 NC_SPMU_GPIO5
SPMU_GPIO6 NC_SPMU_GPIO6
SPMU_GPIO7 NC_SPMU_GPIO7
SPMU_GPIO8 NC_SPMU_GPIO8
SPMU_GPIO10 NC_SPMU_GPIO10
SPMU_GPIO11 NC_SPMU_GPIO11
SPMU_GPIO12 NC_SPMU_GPIO12
SPMU_GPIO13 NC_SPMU_GPIO13
SPMU_GPIO14 NC_SPMU_GPIO14
SPMU_GPIO15 NC_SPMU_GPIO15
SPMU_GPIO17 NC_SPMU_GPIO17
SPMU_GPIO18 NC_SPMU_GPIO18
SPMU_GPIO19 NC_SPMU_GPIO19
SPMU_GPIO20 NC_SPMU_GPIO20
SPMU_GPIO21 NC_SPMU_GPIO21
SPMU_GPIO22 NC_SPMU_GPIO22
SPMU_GPIO23 NC_SPMU_GPIO23
SPMU_GPIO24 NC_SPMU_GPIO24
SPMU_GPIO25 NC_SPMU_GPIO25
=PPVOUT_SW1_MPMU_FET NC_PPVOUT_SW1_MPMU
=PPVOUT_SW2_MPMU_FET NC_PPVOUT_SW2_MPMU
=PPVOUT_LDO0_MPMU_REG NC_PPVOUT_LDO0_MPMU
=PP1V8_AWAKE_PCC_REG NC_PPVOUT_LDO3_MPMU
=PPVOUT_LDO6_MPMU_REG NC_PPVOUT_LDO6_MPMU
=PPVOUT_SW2_SPMU_FET NC_PPVOUT_SW2_SPMU
=PP3V3_S2_ENET_1G_REG NC_PPVOUT_LDO1_SPMU
=PPVOUT_LDO2_SPMU_REG NC_PPVOUT_LDO2_SPMU
=PPVOUT_LDO4_SPMU_REG NC_PPVOUT_LDO4_SPMU
=PPVOUT_LDO5_SPMU_REG NC_PPVOUT_LDO5_SPMU
=PPVOUT_LDO6_SPMU_REG NC_PPVOUT_LDO6_SPMU
TODO: SCRUB PULL DOWN VALUES and necessity
for ICs powered by 3V8 or PBUS (** items are known necessary)
P3V8AON_LPM R8485 100K
SE_PWR_EN R8480 47K
WLBT_PWR_EN R8486 100K
P5VS2TPS_PWR_EN NOSTUFF R8483 100K
P1V8VDDH_PWR_EN ** R8484 100K
=PPVIN_SW1_MPMU
=PPVIN_SW2_MPMU
=PPVIN_LDO0_MPMU
=PP3V8_AON_MPMU_LDO3
=PPVIN_LDO6_MPMU
=PPVIN_SW2_SPMU
=PP3V8_AON_SPMU_LDO1
=PPVIN_LDO2_SPMU
=PPVIN_LDO4_SPMU
=PPVIN_LDO5_SPMU
=PPVIN_LDO6_SPMU
PMU_SHDN_REQ MAKE_BASE=TRUE NC_PMU_SHDN_REQ
USBA_PWR_EN NC_USBA_PWR_EN
SIL_PWM_READY NC_SIL_PWM_READY
P1V8S2_PWR_EN NC_P1V8S2_PWR_EN
P3V3S2_PWR_EN NC_P3V3S2_PWR_EN
P5VUSB_PWR_EN NC_P5VUSB_PWR_EN
=PP1V8_AON_MPMU
C8430 0.1UF
IPD_PWR_EN_PMU R8435 0 NOSTUFF
U8432 74LVC2G32GT SOT833
IPD_PWR_HOLD
IPD_PWR_EN_PMU
IPD_PWR_EN
P5VS2_PWR_EN
MAKE_BASE=TRUE P5VS2TPS_PWR_EN
=PP5V_S2_TPS_PU
P5VS2_PWR_EN R8430 0 NOSTUFF
R8432 100K
R8431 100K
R8436 100K
AMUXA0-A1 are the same across all programs
MPMU_AMUX_A2 BMON_ISENSE
MPMU_AMUX_A3 PBUS_VSENSE
MPMU_AMUX_A4 P5VUSB23_HS_ISENSE
MPMU_AMUX_A5 P5VS2_HS_ISENSE
MPMU_AMUX_A6 WLBT_3V8_ISENSE
MPMU_AMUX_A7 usage is unique per project, see CSA85
MPMU_AMUX_B0 IPD_3V8_ISENSE
MPMU_AMUX_B1 MPMU_3V8_ISENSE
MPMU_AMUX_B2 VCCNAND0_HS_ISENSE
MPMU_AMUX_B3 VCCNAND1_HS_ISENSE
MPMU_AMUX_B4 P3V8AON_ISENSE
MPMU_AMUX_B5 USB23_3V8_ISENSE
MPMU_AMUX_B6 SSD0_3V8_ISENSE
MPMU_AMUX_B7 SSD1_3V8_ISENSE
AMUXA0-A3 are the same across all programs
SPMU_AMUX_A4 SPKRAMP_ABC_ISENSE
SPMU_AMUX_A5 SPMU_3V8_ISENSE
SPMU_AMUX_A6 KBD_BKLT_5V_ISENSE
SPMU_AMUX_A7 P1V8VDDH_ISENSE
SPMU_AMUX_B0 USB01_3V8_ISENSE
SPMU_AMUX_B1 usage is unique per project, see CSA85
SPMU_AMUX_B2 P5VUSB01_HS_ISENSE
SPMU_AMUX_B3 TCON_3V8_ISENSE
SPMU_AMUX_B4 BKLT_HS_ISENSE
SPMU_AMUX_B5 SD_HS_ISENSE
SPMU_AMUX_B6 ALSCAM_5V_ISENSE
SPMU_AMUX_B7 BKLTCONN_3V8_ISENSE
MPMU_TDEV1 P3V8AON_THMSNS
MPMU_TDEV2 MPMU_THMSNS
MPMU_TDEV3 P1V8VDDH_THMSNS_1
MPMU_TDEV4 AIRFLOW_R_THMSNS
MPMU_TDEV5 WING_R_THMSNS
MPMU_TDEV6 CHGR_THMSNS
MPMU_TDEV7 SOC_THMSNS_1
MPMU_TDEV8 P1V8VDDH_THMSNS_2
SPMU_TDEV1 P1V8VDDH_THMSNS_3
SPMU_TDEV2 AIRFLOW_C_THMSNS
SPMU_TDEV3 FINSTACK_R_THMSNS
SPMU_TDEV4 FINSTACK_L_THMSNS
SPMU_TDEV5 AIRFLOW_L_THMSNS
SPMU_TDEV6 WING_L_THMSNS
SPMU_TDEV7 SPMU_THMSNS
SPMU_TDEV8 WLBT_THMSNS
-MPMU-
-SPMU-
=PP3V8_AON_MPMU
MPMU_CONF_MS0 <-MS0
MPMU_CONF_MS1 <-MS1
SPMU_CONF_MS0 <-MS0
SPMU_CONF_MS1 <-MS1
VSS_ANA_SPMU MAKE_BASE=TRUE
CONF_MS[0]: 0=Slave, 1=Master
CONF_MS[1]: XTAL: 0=disable, 1=enable
=VDD_MAIN_SNS_MPMU =PP3V8_AON_MPMU
=VDD_MAIN_SNS_SPMU =PP3V8_AON_SPMU
TP_SPMU_LDOX_EN MAKE_BASE=TRUE EDP_BKLT_1V29_EN
=IPD_LID_OPEN_1V8_POWER_IN_WAKE IPD_LID_OPEN_1V8
=IPD_WAKE_L_ENET_WAKE_L IPD_WAKE_L
=IPD_PWR_EN_ENET_PWR_EN IPD_PWR_EN_PMU
=DP2HDMI_PWR_EN_HDMI_CEC_IRQ DP2HDMI_PWR_EN_PMU
=PVBAT_ILIMIT_L_P12VAON_PLIMIT_L PVBAT_ILIMIT_L
SPMU_GPIO16 DEBUG_SPMU_GPIO16 TP8400 TP-P4
SPMU_GPIO26 PMU_DBGLED_ENABLE
=PP3V8_AON_SPMU
MPMU_CONF_ID0 <-ID0
MPMU_CONF_ID1 <-ID1
MPMU_CONF_ID2 <-ID2
SPMU_CONF_ID0 <-ID0
SPMU_CONF_ID1 <-ID1
SPMU_CONF_ID2 <-ID2
VSS_ANA_MPMU MAKE_BASE=TRUE
VSS_ANA_SPMU MAKE_BASE=TRUE
CONF_ID[0]: SGPIO SLAVE_ID[0] and SWD TINSTANCE[0]
CONF_ID[1]: SGPIO SLAVE_ID[1] and SWD TINSTANCE[1]
CONF_ID[2]: SGPIO SLAVE_ID[2]
BOM_COST_GROUP=SOC POWER

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0 Ohm resistor bom option to have Viper Tsense connect to AMUX_A7 by default
Adding NOSTUFF to HDMI_1V8 sensor to keep circuitry in case its needed again

43 MPMU_AMUX_A7 — R8500 1 0 2 5% 1/20W 0201 MF — P1V8VDDH_TSENSE 64

R8501 1 0 2 NOSTUFF 5% 1/20W 0201 MF — HDMI_1V8_ISENSE 62

39 SPMU_AMUX_B1 — MAKE_BASE=TRUE — FAN_PBUS_ISENSE 61

Dummy Cap, North

C8500	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8501	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8502	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8503	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8504	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8505	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8506	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8507	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201

Dummy Cap, South

C8508	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8509	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8510	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8511	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8512	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8513	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8514	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201
C8515	CKPLUS_WAIVE=TERMSHORTED	12PF	25V	NP0-C0G	5% 0201

BOM_COST_GROUP=PLATFORM POWER

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PMU PROJECT SPECIFIC SUPPORT 2

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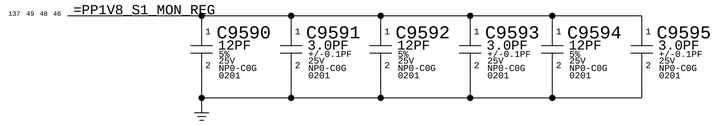
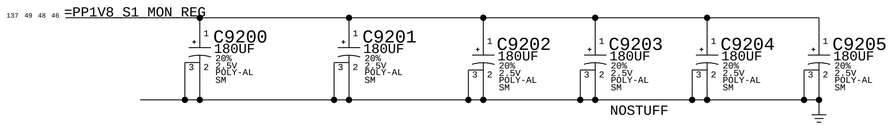
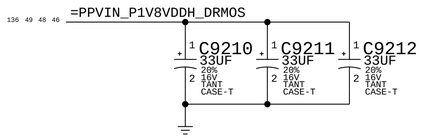
ADDITIONAL VIPER DESENSE CAPS REQUIRED FOR T728 IN ADDITION TO DESENSE CAPS IN REF DESIGN



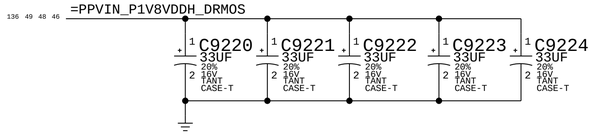
ADDITIONAL VIPER BULK CAPS REQUIRED FOR T728 IN ADDITION TO BULK CAPS IN REF DESIGN



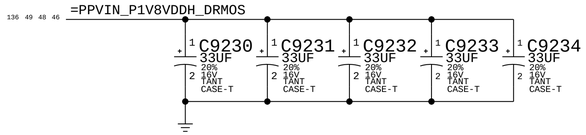
<rdar://problem/61127187> (P2_ J316 P1s MLB Add PBUS caps on Viper input



PH1



PH2



PH3

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=MLADEN SYNC_DATE=04/15/2020

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OK2INTEGRATE

VIPER CONTROLLER

ROUTE VIPER_BOOT_1, VIPER_GSW1, VIPER_GSENSE1 TOGETHER IN DIFFENTIAL-TRIPLET FASHION, WITH VIPER_GSW1 IN THE MIDDLE

130 44 43 IN P1V8VDDH_PWR_EN
R9330 0 5% 1/20W MF 0201
P1V8VDDH_PWR_EN_R 47

131 130 43 IN P1V8VDDH_SLP_L
R9331 0 5% 1/20W MF 0201
P1V8VDDH_SLP_R_L 47

136 =PPVIN_P1V8VDDH_CTRL
R9310 1 5% 1/20W MF 201
PLACE_NEAR=U9300.34:10MM
C9310 2.2UF 20% 25V X6S-CERM 0402

135 47 =PP5V_P1V8VDDH_CTRL
R9315 1 5% 1/20W MF 201
PLACE_NEAR=U9300.39:10MM
C9315 2.2UF 20% 25V X6S-CERM 0402

135 47 =PP1V2_P1V8VDDH_CTR
PLACE_NEAR=U9300.40:10MM
C9320 2.2UF 20% 25V X6S-CERM 0402

47 PP1V5_P1V8VDDH_LDO15
PLACE_NEAR=U9300.38:10MM VOLTAGE=1.5V
C9321 2.2UF 20% 25V X6S-CERM 0402

63 47 OUT P1V8VDDH_IMON

137 =PP1V8_S1_MON_VDDH_FB
XW9300 SHORT-16L-0.1MM-SM
PLACE_NEAR=UA100:10MM
R9305 0 5% 1/20W MF 0201
P1V8S1MONVDDH_SENSE_R_P
C9307 330PF 10% 16V X7R 0201
PLACE_NEAR=U9300:10MM

XW9301 SHORT-16L-0.1MM-SM
P1V8S1MONVDDH_SENSE_R_N
PLACE_NEAR=XW9300:5MM
R9306 0 5% 1/20W MF 0201
C9305 100PF 5% 50V C0G 0201
C9306 330PF 10% 16V X7R 0201
PLACE_NEAR=U9300:10MM

49 48 OUT P1V8VDDH_IREF_R
R9325 0 5% 1/20W MF 0201
PLACE_NEAR=U9300.12:10MM
C9325 1UF 20% 10V X6S-CERM 0201

353S02508
U9300
RAA225502A-3PH-R0E8
TQFN
OMIT_TABLE

PPVIN_P1V8VDDH_CTRL_VIN VOLTAGE=12V	34	VIN	BOOT1	33	P1V8VDDH_BOOT1_R
PP5V_P1V8VDDH_CTRL_VCC VOLTAGE=5V	39	VCC	GSW1	32	P1V8VDDH_GSW1_R
47 P1V8VDDH_VPP	36	VPP	GSENSE1	31	P1V8VDDH_GSENSE1_R
	40	VIN1V2	PWM1	23	P1V8VDDH_DRMOS_PWM1 OUT 48 130
47 PP1V5_P1V8VDDH_LDO15	38	LDO15	PWM2	24	P1V8VDDH_DRMOS_PWM2 OUT 48 130
63 47 OUT P1V8VDDH_IMON	11	IMON	PWM3	25	P1V8VDDH_DRMOS_PWM3 OUT 49 130
			PWM4	26	P1V8VDDH_DRMOS_PWM4 OUT 143
			PWM5	27	P1V8VDDH_DRMOS_PWM5 OUT 143
			PWM6	28	P1V8VDDH_DRMOS_PWM6 OUT 143
			PWM7	29	P1V8VDDH_DRMOS_PWM7 OUT 143
			PWM8	30	P1V8VDDH_DRMOS_PWM8 OUT 143
47 P1V8VDDH_IMON_FILT	10	IMON_FILT	ISENSE1	13	P1V8VDDH_ISENSE1 IN 48
47 P1V8VDDH_PWR_EN_R	3	ENABLE	ISENSE2	14	P1V8VDDH_ISENSE2 IN 48
47 P1V8VDDH_SLP_R_L	6	SLP*	ISENSE3	15	P1V8VDDH_ISENSE3 IN 49
47 P1V8VDDH_FAULT_L	37	FAULT*	ISENSE4	16	P1V8VDDH_ISENSE4
P1V8S1MONVDDH_SENSE_P	8	VSENSE	ISENSE5	17	P1V8VDDH_ISENSE5
P1V8S1MONVDDH_SENSE_N	9	VRTN	ISENSE6	18	
P1V8VDDH_IREF	12	IREF	ISENSE7	19	
47 P1V8VDDH_OTP_SEL	35	CONFIG	ISENSE8	20	
			TSENSE	7	P1V8VDDH_DRMOS_TSENSE_R
			SPS_EN	22	P1V8VDDH_DRMOS_EN OUT 48 49
			FET_FAULT*	21	P1V8VDDH_DRMOS_FAULT_L IN 47 48 49
			TRIGGER0*	4	P1V8VDDH_ILIMIT_THROTTLE_L OUT 5 130
			TRIGGER1*	5	P1V8VDDH_TLIMIT_THROTTLE_L OUT 5 130
			SCLK	2	SPMI_NUB_P1V8VDDH_CLK IN 13
			SDATA	1	SPMI_NUB_P1V8VDDH_DATA BI 13
	41	EPAD			

R9300 49.9 1% 1/20W MF 201
SWITCH_NODE=TRUE DIDT=TRUE
P1V8VDDH_BOOT1 IN 48
PLACE_NEAR=R9301:5MM
PLACE_NEAR=U9300.32:10MM
C9300 100PF 5% 50V C0G 0201

R9301 1.00 1% 1/20W MF-LF 0201
P1V8VDDH_GSW1 IN 48
PLACE_NEAR=C9301:5MM
NO_XNET_CONNECTION=1
PLACE_NEAR=U9300.32:10MM
C9301 100PF 5% 50V C0G 0201
NOSTUFF

R9302 49.9 1% 1/20W MF 201
P1V8VDDH_GSENSE1 IN 48
PLACE_NEAR=R9301:5MM
NO_XNET_CONNECTION=1
PLACE_NEAR=U9300.31:10MM
C9302 100PF 5% 50V C0G 0201

PACK_OPTION=VIPER:3PH
PP5V_P1V8VDDH_CTRL_VCC 47
MAKE_BASE=TRUE

R9303 10K 1% 1/20W MF 201
P1V8VDDH_DRMOS_TSENSE IN 48 49 64
C9303 470PF 10% 16V X5R-X7R-CERM 0201
PLACE_NEAR=U9300.7:10MM

P1V8VDDH_IMON 47 63
R9323 200K 1% 1/20W MF 201
PLACE_NEAR=U9300.10:10MM
P1V8VDDH_IMON_FILT 47
NOSTUFF
PLACE_NEAR=U9300.10:10MM PLACE_NEAR=U9300.10:10MM
R9322 100K 1% 1/20W MF 201
C9322 0.1UF 10% 25V X6S-CERM 0201

47 P1V8VDDH_OTP_SEL
PP1V5_P1V8VDDH_LDO15 47
NOSTUFF
R9340 1K 1% 1/20W MF 201
R9341 1K 1% 1/20W MF 201

49 48 47 P1V8VDDH_DRMOS_FAULT_L
=PP5V_P1V8VDDH_CTRL 47 135
R9342 1K 1% 1/20W MF 201

PP5V_P1V8VDDH_CTRL_VCC 47
R9344 1K 1% 1/20W MF 201
47 P1V8VDDH_VPP

=PP1V2_P1V8VDDH_CTR 47 135
R9343 100K 1% 1/20W MF 201
47 P1V8VDDH_FAULT_L

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02759	1	IC,RAA225502C,VPR,A2,3PH,OTP-R0E0,TQFN40	U9300	CRITICAL	VIPER:3PH
353S02760	1	IC,RAA225502C,VPR,A2,5PH,OTP-R0F0,TQFN40	U9300	CRITICAL	VIPER:5PH

BOM_COST_GROUP=SOC POWER

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VIPER POWER STAGES 1

=PPVIN_P1V8VDDH_DRMOS

C9407 33UF 20% 16V TANT CASE-T
C9400 33UF 20% 16V TANT CASE-T
C9401 33UF 20% 16V TANT CASE-T
C9402 33UF 20% 16V TANT CASE-T
C9403 33UF 20% 16V TANT CASE-T
C9404 33UF 20% 16V TANT CASE-T
C9405 2.2UF 20% 25V X6S-CERM 0402
C9406 2.2UF 20% 25V X6S-CERM 0402 MIRROR_WITH=C9405
C9408 0.1UF 10% 25V X6S-CERM 0201

MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
PP5V_P1V8VDDH_DRMOS_VCC1

D9400 SOD523 SBR1A30T5

PLACE_NEAR=U9400:5MM
R9410 0.1 1% 1/2W MF 0603
=PP5V_P1V8VDDH_DRMOS

C9410 2.2UF 20% 25V X6S-CERM 0402
C9411 2.2UF 20% 25V X6S-CERM 0402

OMIT_TABLE

353S02574
U9400
RAA225701B
PQFN

VIN, VCC, PVCC, PWM, EN, FAULT_L, TSENSE, ISENSE, IREF, SGND, PGND, GSW, BOOT, SW, VOS, GL

P1V8VDDH_DRMOS_PWM1
P1V8VDDH_DRMOS_EN
P1V8VDDH_DRMOS_FAULT_L1
P1V8VDDH_DRMOS_TSENSE
P1V8VDDH_DRMOS_GSW1
P1V8VDDH_DRMOS_BOOT1_R
P1V8VDDH_SW1
TP_P1V8VDDH_DRMOS1_GL1

MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.2000
SWITCH_NODE=TRUE
DIDT=TRUE

R9412 0 5% 1/16W MF-LF 402
P1V8VDDH_DRMOS_BOOT1

C9412 0.1UF 10% 25V X7R-CERM-1 0402

R9417 0 5% 1/20W MF 0201 PLACE_NEAR=C9412.1:5MM
P1V8VDDH_GSW1

R9418 49.9 1% 1/20W MF 201 PLACE_NEAR=C9412.2:5MM
P1V8VDDH_BOOT1

L9400 0.22UH-20%-55A-0.0013OHM PILS083T-SM PACK_OPTION=VIPER_L3MM NO_XNET_CONNECTION=1
L9400 0.22UH-20%-44A-0.0019OHM PILA082O-SM NO_XNET_CONNECTION=1 PACK_OPTION=VIPER_L2M4M PACK_IGNORE=TRUE
P1V8VDDH_SW1_L

P1V8VDDH_RISNS1_P
P1V8VDDH_RISNS1_N
0612-2 MF 1W 1%
R9450 0.0005 PACK_OPTION=VIPER_DBG
PACK_OPTION=VIPER_PRF

=PP1V8_S1_MON_REG

NOSTUFF R9413 2.2 5% 1/10W MF-LF 603
P1V8VDDH_SNUB1 DIDT=TRUE SWITCH_NODE=TRUE
NOSTUFF C9413 0.001UF 10% 50V X7R-CERM 0402
NOSTUFF
P1V8VDDH_VOS1

XW9400 SM PLACE_NEAR=L9400.2:6MM

P1V8VDDH_ISENSE1
NO_XNET_CONNECTION=1 PLACE_NEAR=C9414:5MM
R9414 100 1% 1/20W MF 201
P1V8VDDH_DRMOS_ISENSE1_P

NOSTUFF R9415 100 1% 1/20W MF 201
C9414 47PF 5% 25V C0G 0201 PLACE_NEAR=U9300:10MM
XW9402 SM PLACE_NEAR=C9414:5MM
P1V8VDDH_IREF_R
PLACE_NEAR=R9325:10MM NO_XNET_CONNECTION=1
P1V8VDDH_DRMOS_ISENSE1_N

P1V8VDDH_DRMOS_IREF1
R9416 0 5% 1/20W MF 0201 PLACE_NEAR=C9416:5MM
C9416 0.1UF 10% 25V X6S-CERM 0201 PLACE_NEAR=U9400.29:5MM

PLACE_NEAR=U9400:5MM
R9419 49.9 1% 1/20W MF 201
P1V8VDDH_GSENSE1

R9415, C9414, R9416 VALUES ARE TBD

P1V8VDDH_SW1
C9418 12PF 5% 25V NP0-C0G 0201
C9419 3.0PF +/-0.1PF 25V NP0-C0G 0201

R9401 0 5% 1/20W MF 0201
P1V8VDDH_DRMOS_FAULT_L
P1V8VDDH_DRMOS_FAULT_L1

R9402 0 5% 1/20W MF 0201
P1V8VDDH_DRMOS_FAULT_L
P1V8VDDH_DRMOS_FAULT_L2

=PPVIN_P1V8VDDH_DRMOS

C9420 33UF 20% 16V TANT CASE-T
C9421 33UF 20% 16V TANT CASE-T
C9422 33UF 20% 16V TANT CASE-T
C9423 33UF 20% 16V TANT CASE-T
C9425 2.2UF 20% 25V X6S-CERM 0402
C9426 2.2UF 20% 25V X6S-CERM 0402 MIRROR_WITH=C9425
C9428 0.1UF 10% 25V X6S-CERM 0201

MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
PP5V_P1V8VDDH_DRMOS_VCC2

PLACE_NEAR=U9420:5MM
R9430 0.1 1% 1/2W MF 0603
=PP5V_P1V8VDDH_DRMOS

C9430 2.2UF 20% 25V X6S-CERM 0402
C9431 2.2UF 20% 25V X6S-CERM 0402

OMIT_TABLE

353S02574
U9420
RAA225701B
PQFN

P1V8VDDH_DRMOS_PWM2
P1V8VDDH_DRMOS_EN
P1V8VDDH_DRMOS_FAULT_L2
P1V8VDDH_DRMOS_TSENSE
P1V8VDDH_DRMOS_GSW2
P1V8VDDH_DRMOS_BOOT2_R
P1V8VDDH_SW2
TP_P1V8VDDH_DRMOS2_GL1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
SWITCH_NODE=TRUE
DIDT=TRUE

R9432 0 5% 1/16W MF-LF 402
P1V8VDDH_DRMOS_BOOT2

C9432 0.1UF 10% 25V X7R-CERM-1 0402

P1V8VDDH_RISNS2_P
P1V8VDDH_RISNS2_N
0612-2 MF 1W 1%
R9451 0.0005 PACK_OPTION=VIPER_DBG
PACK_OPTION=VIPER_PRF

L9420 0.22UH-20%-55A-0.0013OHM PILS083T-SM PACK_OPTION=VIPER_L3MM NO_XNET_CONNECTION=1
L9420 0.22UH-20%-44A-0.0019OHM PILA082O-SM PACK_OPTION=VIPER_L2M4M PACK_IGNORE=TRUE
P1V8VDDH_SW2_L

NOSTUFF R9433 2.2 5% 1/10W MF-LF 603
P1V8VDDH_SNUB2 DIDT=TRUE SWITCH_NODE=TRUE
NOSTUFF C9433 0.001UF 10% 50V X7R-CERM 0402
NOSTUFF
P1V8VDDH_VOS2

XW9420 SM PLACE_NEAR=L9420.2:5MM

P1V8VDDH_ISENSE2
NO_XNET_CONNECTION=1 PLACE_NEAR=C9434:5MM
R9434 100 1% 1/20W MF 201
P1V8VDDH_DRMOS_ISENSE2_P

NOSTUFF R9435 100 1% 1/20W MF 201
C9434 47PF 5% 25V C0G 0201 PLACE_NEAR=U9300:10MM
XW9422 SM PLACE_NEAR=C9434:5MM
P1V8VDDH_IREF_R
PLACE_NEAR=R9325:10MM NO_XNET_CONNECTION=1
P1V8VDDH_DRMOS_ISENSE2_N

P1V8VDDH_DRMOS_IREF2
R9436 0 5% 1/20W MF 0201 PLACE_NEAR=C9436:5MM
C9436 0.1UF 10% 25V X6S-CERM 0201 PLACE_NEAR=U9420.29:5MM

R9435, C9434, R9436 VALUES ARE TBD

P1V8VDDH_SW2
C9440 12PF 5% 25V NP0-C0G 0201
C9441 3.0PF +/-0.1PF 25V NP0-C0G 0201

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02708	2	IC,RAA225701C,SKY,DR MOS,A2,OTP-0,PQFN32	U9400,U9420	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE: VIPER POWER STAGES 1

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OK2INTEGRATE

VIPER POWER STAGES 2

=PPVIN_P1V8VDDH_DRMOS

C9500 33UF 20% 16V TANT CASE-T
C9501 33UF 20% 16V TANT CASE-T
C9502 33UF 20% 16V TANT CASE-T
C9503 33UF 20% 16V TANT CASE-T
C9505 2.2UF 20% 25V X6S-CERM 0402
C9506 2.2UF 20% 25V X6S-CERM 0402 MIRROR_WITH=C9505
C9508 0.1UF 10% 25V X6S-CERM 0201

MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
PP5V_P1V8VDDH_DRMOS_VCC3

C9510 2.2UF 20% 25V X6S-CERM 0402
C9511 2.2UF 20% 25V X6S-CERM 0402

PLACE_NEAR=U9500:5MM
R9510 0.1 1% 1/2W MF 0603
=PP5V_P1V8VDDH_DRMOS

OMIT_TABLE

353S02574
U9500
RAA225701B
PQFN

VIN VIN VCC PVCC

P1V8VDDH_DRMOS_PWM3 → PWM
P1V8VDDH_DRMOS_EN → EN
P1V8VDDH_DRMOS_FAULT_L3 → FAULT_L
P1V8VDDH_DRMOS_TSENSE ← TSENSE
P1V8VDDH_DRMOS_ISENSE3_P → ISENSE
P1V8VDDH_DRMOS_IREF3 → IREF
SGND PGND PGND PGND

GSW → P1V8VDDH_DRMOS_GSW3
BOOT → P1V8VDDH_DRMOS_BOOT3_R
SW → P1V8VDDH_SW3
VOS → P1V8VDDH_VOS3
GL → TP_P1V8VDDH_DRMOS3_GL1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
SWITCH_NODE=TRUE
DIDT=TRUE

R9512 0 5% 1/10W MF-LF 402
P1V8VDDH_DRMOS_BOOT3

MIN_LINE_WIDTH=0.2500
MIN_NECK_WIDTH=0.2000
SWITCH_NODE=TRUE
DIDT=TRUE

C9512 0.1UF 10% 25V X7R-CERM-1 0402

MIN_LINE_WIDTH=0.0890
MIN_NECK_WIDTH=0.1000
SWITCH_NODE=TRUE
DIDT=TRUE

NOSTUFF
R9513 2.2 5% 1/10W MF-LF 603
P1V8VDDH_SNUB3
DIDT=TRUE
SWITCH_NODE=TRUE

C9513 0.001UF 10% 50V X7R-CERM 0402
NOSTUFF
P1V8VDDH_VOS3

L9500 0.22UH-20%-55A-0.0013OHM PILS083T-SM
PACK_OPTION=VIPER_L3MM
NO_XNET_CONNECTION=1

L9500 0.22UH-20%-44A-0.0019OHM PILA062Q-SM
PACK_OPTION=VIPER_L2M4M
PACK_IGNORE=TRUE

P1V8VDDH_SW3
XW9500 SM
PLACE_NEAR=L9500.2:5MM

P1V8VDDH_RISNS3_P
P1V8VDDH_RISNS3_N
0612-2 MF 1W 1% 0.0005 R9550
PACK_OPTION=VIPER_DBG
NO_XNET_CONNECTION=1
PACK_OPTION=VIPER_PRF

P1V8VDDH_ISENSE3
NO_XNET_CONNECTION=1
PLACE_NEAR=C9514:5MM
R9514 100 1% 1/20W MF 201
P1V8VDDH_DRMOS_ISENSE3_P

NOSTUFF
R9515 100 1% 1/20W MF 201
PLACE_NEAR=C9514:5MM

C9514 47PF 5% 25V C0G 0201
PLACE_NEAR=U9300:10MM

XW9502 SM
P1V8VDDH_IREF_R
PLACE_NEAR=R9325:10MM
NO_XNET_CONNECTION=1
P1V8VDDH_DRMOS_ISENSE3_N

R9516 0 5% 1/20W MF 0201
PLACE_NEAR=C9516:5MM

C9516 0.1UF 10% 25V X5S-CERM 0201
PLACE_NEAR=U9500.29:5MM

R9515, C9514, R9516 VALUES ARE TBD

P1V8VDDH_DRMOS_FAULT_L
R9503 0 5% 1/20W MF 0201
P1V8VDDH_DRMOS_FAULT_L3

P1V8VDDH_SW3
C9518 12PF 5% 25V NP0-C0G 0201
C9519 3.0PF +/-0.1PF 25V NP0-C0G 0201

OMIT_TABLE IS FOR N&V BOM OPTIONS
MASTER TABLE IS ON SOC PAGES

C9560 C9561 C9562 C9563 C9564 C9565 C9566 C9567 C9568 C9569
20UF 20% 2.5V X6S-CERM 0402-COMBO

C9570 C9571 C9572 C9573 C9574 C9575 C9576 C9577 C9578 C9579
20UF 20% 2.5V X6S-CERM 0402-COMBO

C9580 C9581 C9582 C9583 C9584 C9585 C9586 C9587 C9588 C9589
20UF 20% 2.5V X6S-CERM 0402-COMBO

PACK_IGNORE=TRUE
PACK_OPTION=VIPER_C9544
BOMOPTION=VIPER_C9544

C9540 C9541 C9542 C9543 C9544
470UF 20% 2.5V POLY-AL D-SM

PACK_OPTION=VIPER_C9543
BOMOPTION=VIPER_C9543

C9546 C9547 C9548 C9549 C9550
180UF 20% 2.5V POLY-AL SM

=PP1V8_S1_MON_REG

C9520 C9521 C9522 C9523 C9524 C9525 C9526 C9527 C9528 C9529
12PF 5% 25V NP0-C0G 0201
3.0PF +/-0.1PF 25V NP0-C0G 0201

C9530 C9531 C9532 C9533 C9534 C9535 C9536 C9537 C9538 C9539
12PF 5% 25V NP0-C0G 0201
3.0PF +/-0.1PF 25V NP0-C0G 0201

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02708	1	IC,RAA225701C,SKY,DR MOS,A2,OTP-0,PQFN32	U9500	CRITICAL	

BOM_COST_GROUP=SOC POWER

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OK2INTEGRATE

MONACO_0

INSTANCE = C0
SILICON:CFG = A0:A0, B0:D0
SILICON:OTP = A0:ZP_, B0:YP_

CA160 12PF 5% 25V NP0-C0G 0201
CA161 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA162 12PF 5% 25V NP0-C0G 0201
CA163 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA164 12PF 5% 25V NP0-C0G 0201
CA165 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA166 12PF 5% 25V NP0-C0G 0201
CA167 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA168 12PF 5% 25V NP0-C0G 0201
CA169 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA170 12PF 5% 25V NP0-C0G 0201
CA171 3.0PF +/-0.1PF 25V NP0-C0G 0201

PACK_OPTION=CLVR_2C_SC
PACK_OPTION=CLVR_2C_SC
PACK_OPTION=CLVR_2C_SC

11UF APN: 138S00328

137 53 52 51 50 =PP1V8_S1_CLVR_VDDH

CA100 11UF 20% 2.5V X6T 0402
CA101 11UF 20% 2.5V X6T 0402
CA102 11UF 20% 2.5V X6T 0402
CA103 11UF 20% 2.5V X6T 0402
CA104 11UF 20% 2.5V X6T 0402
CA105 11UF 20% 2.5V X6T 0402
CA106 11UF 20% 2.5V X6T 0402
CA107 11UF 20% 2.5V X6T 0402
CA108 11UF 20% 2.5V X6T 0402
CA109 11UF 20% 2.5V X6T 0402
CA117 11UF 20% 2.5V X6T 0402
CA118 11UF 20% 2.5V X6T 0402

CA130 10UF 20% 6.3V CER-X6S 0402

138 52 51 =PP0V8_S2_CLVR_VDDDIG
138 53 52 51 50 =PP1V2_S2_CLVR_VDDIO

CA131 10UF 20% 6.3V CER-X6S 0402

52 51 138 =PP1V8_S2_CLVR_VDDC
52 51 50 PP1V8_CLVR_VDDC1

XWA100 SHORT-16L-0.1MM-SM
137 IN =M0_BUCK0_FB
M0_BUCK0_1_SVSS

XWA101 SHORT-16L-0.1MM-SM
137 IN =M0_BUCK2_FB
M0_BUCK2_3_SVSS

PLACE_NEAR=XW9300:8MM
137 IN =M0_BUCK1_FB
137 IN =M0_BUCK3_FB

RA150 22 1% 1/20W MF 201
137 53 52 51 50 =PP1V8_S1_CLVR_VDDH
P1V8S1CLVR0VDDH_SENSE

KEEP BELOW 25 OHM FOR ONE SVDDH

PLACE_NEAR=UA100.M7:5MM
CA150 470PF 5% 25V C0G 0201
FILTER CUTOFF: 15MHZ

OMIT_TABLE

UA100 MON BGA SYM 1 OF 2

B4	VDDH	VOUT0_A	L10
B11		VOUT0_B	L13
C3		VOUT1_A	K10
C4		VOUT1_B	K13
C7		VOUT2_A	J10
C8		VOUT2_B	J13
C11		VOUT3_A	H10
C12		VOUT3_B	H13
D1		VOUT4_A	G10
D7		VOUT4_B	G13
D8		VOUT5_A	F10
D14		VOUT5_B	F13
E3		VOUT6_A	E10
E4		VOUT6_B	E13
E11		VOUT7_A	D10
E12		VOUT7_B	D13
F1		VOUT8_A	C10
F14		VOUT8_B	C13
G3		VOUT9_A	B10
G4		VOUT9_B	B13
G7		VOUT10_A	J9
G8		VOUT10_B	J6
G11		VOUT11_A	H9
G12		VOUT11_B	H6
H1		VOUT12_A	G9
H7		VOUT12_B	G6
H8		VOUT13_A	F9
H14		VOUT13_B	F6
J3		VOUT14_A	E9
J4		VOUT14_B	E6
J11		VOUT15_A	D9
J12		VOUT15_B	D6
K4		VOUT16_A	C9
K11		VOUT16_B	C6
M6	VDD_DIG	VOUT17_A	B9
M4	VDDIO	VOUT17_B	B6
M9	VDDC	VOUT18_A	L2
M10	VDDC1	VOUT18_B	L5
L9	SVDD_HP0	VOUT19_A	K2
K8	SVSS_0	VOUT19_B	K5
L6	SVDD_HP1	VOUT20_A	J2
K7	SVSS_1	VOUT20_B	J5
L8	SVDD_LP0	VOUT21_A	H2
L7	SVDD_LP1	VOUT21_B	H5
M7	SVDDH	VOUT22_A	G2
		VOUT22_B	G5
		VOUT23_A	F2
		VOUT23_B	F5
		VOUT24_A	E2
		VOUT24_B	E5
		VOUT25_A	D2
		VOUT25_B	D5
		VOUT26_A	C2
		VOUT26_B	C5
		VOUT27_A	B2
		VOUT27_B	B5

HP0 =M0_BUCK0 50 137
LP0 =M0_BUCK1 137
HP0 =M0_BUCK0 50 137
HP1 =M0_BUCK2 50 137
LP1 =M0_BUCK3 137
HP1 =M0_BUCK2 50 137

OMIT_TABLE

UA100 MON BGA SYM 2 OF 2

A1	VSS	GPIO0	A10	CLVR0_GPIO0	BI 53
A2		GPIO1	B1	CLVR0_GPIO1	BI 53
A4		GPIO2	C1	CLVR0_GPIO2	BI 53
A6		GPIO3	A13	CLVR0_GPIO3	BI 53
A9		GPIO4	A12	CLVR0_GPIO4	BI 53
A11		GPIO5	B14	CLVR0_GPIO5	BI 53
A14		JTAG_TCK/SWD_CLK	L1	SWD_CLVR0_SWCLK	IN 11
B3		JTAG_TMS/SWD_DAT	K1	SWD_CLVR0_SWDIO	BI 11
B7		JTAG_TDI	G1		
B8		JTAG_TDO	C14	NC_TDO0	
B12		JTAG_TRSTN	G14		
D3		ATB0	A3	NC_ATB00	
D4		ATB1	A8	NC_ATB01	
D11		ATB2	A5	NC_ATB02	
D12		ATB3	A7	NC_ATB03	
E1		SGPIO_CLK	M12	SGPIO_PMU_CLVR0_CLK	IN 13
E7		SGPIO_D	L12	SGPIO_PMU_CLVR0_DATA	BI 13
E8		ADDR0	M5	CLVR0_SGPIO_ADDR0	50
E14		ADDR1	M3	CLVR0_SGPIO_ADDR1	50
F3		SPMI_SCLK	K14	SPMI_CLVR0_CLK	IN 11
F4		SPMI_SDATA	L14	SPMI_CLVR0_DATA	BI 11
F7		CRASH*	M13	PMU_CRASH_L	BI 43 51 52 130
F8		UT*	M2	CLVR_VDDH_UVWARN_L	OUT 5 129 130
F11		CLK32K	M11	PMU_CLK32K_CLVR	IN 44 51 52 130
F12		RESET*	L3	CLVR_RESET_L	IN 43 51 52 130
H3					
H4					
H11					
H12					
J1					
J7					
J8					
J14					
K3					
K6					
K9					
K12					
L4					
L11					
M1					
M14					

XWA102 SHORT-16L-0.1MM-SM
1 2 CLVR0_VSSC M8 VSSC

50 CLVR0_SGPIO_ADDR0 =PP1V2_S2_CLVR_VDDIO 50 51 52 53 138
50 CLVR0_SGPIO_ADDR1 MAKE_BASE=TRUE

VOLTAGE=1.8V
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.1000
130 =PP1V8_CLVR_VDDC1 PP1V8_CLVR_VDDC1 50 51 52
MAKE_BASE=TRUE

138S0858
CA121 10UF 20% 6.3V CERM-X6S 0402

137 50 =M0_BUCK0
CA140 12PF 5% 25V NP0-C0G 0201
CA141 3.0PF +/-0.1PF 25V NP0-C0G 0201

137 50 =M0_BUCK2
CA142 12PF 5% 25V NP0-C0G 0201
CA143 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=SOC POWER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-24561	1	IC,MON,B0,OTP-YPJ,DEV,FCCSP168	UA100	CRITICAL	

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OK2INTEGRATE

MONACO_1

INSTANCE = C1
CFG = A1
OTP = BP_

PACK_OPTION=CLVR_2C_SC

CA260 12PF 5% 25V NP0-C0G 0201
CA261 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA262 12PF 5% 25V NP0-C0G 0201
CA263 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA264 12PF 5% 25V NP0-C0G 0201
CA265 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA266 12PF 5% 25V NP0-C0G 0201
CA267 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA268 12PF 5% 25V NP0-C0G 0201
CA269 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA270 12PF 5% 25V NP0-C0G 0201
CA271 3.0PF +/-0.1PF 25V NP0-C0G 0201

137 53 52 51 50 =PP1V8_S1_CLVR_VDDH

11UF APN: 138S00328

CA200 11UF 20% 2.5V X6T 0402
CA201 11UF 20% 2.5V X6T 0402
CA202 11UF 20% 2.5V X6T 0402
CA203 11UF 20% 2.5V X6T 0402
CA204 11UF 20% 2.5V X6T 0402
CA205 11UF 20% 2.5V X6T 0402
CA206 11UF 20% 2.5V X6T 0402
CA207 11UF 20% 2.5V X6T 0402
CA208 11UF 20% 2.5V X6T 0402

OMIT_TABLE

UA200
MON
BGA
SYM 1 OF 2

	B4	VOUT0_A	L10
	B11	VOUT0_B	L13
	C3	VOUT1_A	K10
	C4	VOUT1_B	K13
	C7	VOUT2_A	J10
	C8	VOUT2_B	J13
	C11	VOUT3_A	H10
	C12	VOUT3_B	H13
	D1	VOUT4_A	G10
	D7	VOUT4_B	G13
	D8	VOUT5_A	F10
	D14	VOUT5_B	F13
	E3	VOUT6_A	E10
	E4	VOUT6_B	E13
	E11	VOUT7_A	D10
	E12	VOUT7_B	D13
	F1	VOUT8_A	C10
	F14	VOUT8_B	C13
	G3	VOUT9_A	B10
VDDH	G4	VOUT9_B	B13
	G7	VOUT10_A	J9
	G8	VOUT10_B	J6
	G11	VOUT11_A	H9
	G12	VOUT11_B	H6
	H1	VOUT12_A	G9
	H7	VOUT12_B	G6
	H8	VOUT13_A	F9
	H14	VOUT13_B	F6
	J3	VOUT14_A	E9
	J4	VOUT14_B	E6
	J11	VOUT15_A	D9
	J12	VOUT15_B	D6
	K4	VOUT16_A	C9
	K11	VOUT16_B	C6
		VOUT17_A	B9
		VOUT17_B	B6
		VOUT18_A	L2
		VOUT18_B	L5
		VOUT19_A	K2
		VOUT19_B	K5
		VOUT20_A	J2
		VOUT20_B	J5
		VOUT21_A	H2
		VOUT21_B	H5
		VOUT22_A	G2
		VOUT22_B	G5
		VOUT23_A	F2
		VOUT23_B	F5
		VOUT24_A	E2
		VOUT24_B	E5
		VOUT25_A	D2
		VOUT25_B	D5
		VOUT26_A	C2
		VOUT26_B	C5
		VOUT27_A	B2
		VOUT27_B	B5

HP0 → =M1_BUCK0 51 137
LP0 → =M1_BUCK1 137
HP0 → =M1_BUCK0 51 137
HP1 → =M1_BUCK2 51 137
LP1 → =M1_BUCK3 137
HP1 → =M1_BUCK2 51 137

138 52 50 =PP0V8_S2_CLVR_VDDDIG → M6 VDD_DIG
138 53 52 51 50 =PP1V2_S2_CLVR_VDDIO → M4 VDDIO
138 52 50 =PP1V8_S2_CLVR_VDDC → M9 VDDC
52 50 PP1V8_CLVR_VDDC1 → M10 VDDC1

XWA200 SHORT-16L-0.1MM-SM
137 IN =M1_BUCK0_FB → L9 SVDD_HP0
M1_BUCK0_1_SVSS → K8 SVSS_0

XWA201 SHORT-16L-0.1MM-SM
137 IN =M1_BUCK2_FB → L6 SVDD_HP1
M1_BUCK2_3_SVSS → K7 SVSS_1
137 IN =M1_BUCK1_FB → L8 SVDD_LP0
137 IN =M1_BUCK3_FB → L7 SVDD_LP1
137 53 52 51 50 =PP1V8_S1_CLVR_VDDH → M7 SVDDH

OMIT_TABLE

UA200
MON
BGA
SYM 2 OF 2

	A1	GPIO0	A10
	A2	GPIO1	B1
	A4	GPIO2	C1
	A6	GPIO3	A13
	A9	GPIO4	A12
	A11	GPIO5	B14
	A14		
	B3	JTAG_TCK/SWD_CLK	L1
	B7	JTAG_TMS/SWD_DAT	K1
	B8	JTAG_TDI	G1
	B12	JTAG_TDO	C14
	D3	JTAG_TRSTN	G14
	D4		
	D11	ATB0	A3
	D12	ATB1	A8
	E1	ATB2	A5
	E7	ATB3	A7
	E8		
	E14	SGPIO_CLK	M12
	F3	SGPIO_D	L12
VSS	F4	ADDR0	M5
	F7	ADDR1	M3
	F8		
	F11	SPMI_SCLK	K14
	F12	SPMI_SDATA	L14
	H3		
	H4	CRASH*	M13
	H11		
	H12	UT*	M2
	J1		
	J7	CLK32K	M11
	J8	RESET*	L3
	J14		
	K3		
	K6		
	K9		
	K12		
	L4		
	L11		
	M1		
	M14		

GPIO0 A10 CLVR1_GPIO0 B1 53
GPIO1 B1 CLVR1_GPIO1 B1 53
GPIO2 C1 CLVR1_GPIO2 B1 53
GPIO3 A13 CLVR1_GPIO3 B1 53
GPIO4 A12 CLVR1_GPIO4 B1 53
GPIO5 B14 CLVR1_GPIO5 B1 53

JTAG_TCK/SWD_CLK L1 SWD_CLVR1_SWCLK IN 11
JTAG_TMS/SWD_DAT K1 SWD_CLVR1_SWDIO B1 11
JTAG_TDO C14 NC_TDO1
JTAG_TRSTN G14

ATB0 A3 NC_ATB10
ATB1 A8 NC_ATB11
ATB2 A5 NC_ATB12
ATB3 A7 NC_ATB13

SGPIO_CLK M12 SGPIO_PMU_CLVR1_CLK IN 13
SGPIO_D L12 SGPIO_PMU_CLVR1_DATA B1 13
ADDR0 M5 CLVR1_SGPIO_ADDR0 51
ADDR1 M3 CLVR1_SGPIO_ADDR1 51

SPMI_SCLK K14 SPMI_CLVR1_CLK IN 11
SPMI_SDATA L14 SPMI_CLVR1_DATA B1 11

CRASH* M13 PMU_CRASH_L B1 43 50 52 130

UT* M2 TP_CLVR1_UT_L 129

CLK32K M11 PMU_CLK32K_CLVR IN 44 50 52 130
RESET* L3 CLVR_RESET_L IN 43 50 52 130

XWA202 SHORT-16L-0.1MM-SM
1 2 CLVR1_VSSC M8 VSSC

51 CLVR1_SGPIO_ADDR0 — MAKE_BASE=TRUE
51 CLVR1_SGPIO_ADDR1 — =PP1V2_S2_CLVR_VDDIO 50 51 52 53 138

137 53 =M1_BUCK0
CA240 12PF 5% 25V NP0-C0G 0201
CA241 3.0PF +/-0.1PF 25V NP0-C0G 0201

137 53 =M1_BUCK2
CA242 12PF 5% 25V NP0-C0G 0201
CA243 3.0PF +/-0.1PF 25V NP0-C0G 0201

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-24556	1	IC,MON,B0,OTP-BPJ,DEV,FCCSP168	UA200	CRITICAL	

BOM_COST_GROUP=SOC POWER

PAGE TITLE: MONACO 1

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OK2INTEGRATE

MONACO_4

SC
INSTANCE = C2
CFG = C0
OTP = QP_

1C
INSTANCE = C4
CFG = C1
OTP = RP_

2C
INSTANCE = C4
CFG = C2
OTP = SP_

PACK_OPTION=CLVR_2C_SC PACK_OPTION=CLVR_2C_SC

CA560 12PF 5% 25V NP0-C0G 0201 | CA561 3.0PF +/-0.1PF 25V NP0-C0G 0201 | CA562 12PF 5% 25V NP0-C0G 0201 | CA563 3.0PF +/-0.1PF 25V NP0-C0G 0201 | CA564 12PF 5% 25V NP0-C0G 0201 | CA565 3.0PF +/-0.1PF 25V NP0-C0G 0201

CA566 12PF 5% 25V NP0-C0G 0201 | CA567 3.0PF +/-0.1PF 25V NP0-C0G 0201 | CA568 12PF 5% 25V NP0-C0G 0201 | CA569 3.0PF +/-0.1PF 25V NP0-C0G 0201 | CA570 12PF 5% 25V NP0-C0G 0201 | CA571 3.0PF +/-0.1PF 25V NP0-C0G 0201

PACK_OPTION=CLVR_2C_SC PACK_OPTION=CLVR_2C_SC

11UF APN: 138S00328

CA500 11UF 20% 2.5V X6T 0402 | CA501 11UF 20% 2.5V X6T 0402 | CA502 11UF 20% 2.5V X6T 0402 | CA503 11UF 20% 2.5V X6T 0402 | CA504 11UF 20% 2.5V X6T 0402

137 53 52 51 50 =PP1V8_S1_CLVR_VDDH

OMIT_TABLE

UA500 MON BGA SYM 1 OF 2

B4	VOUT0_A	L10	HP1	=M4_BUCK2 52 137
B11	VOUT0_B	L13		
C3	VOUT1_A	K10	HP0	=M4_BUCK0 52 137
C4	VOUT1_B	K13		
C7	VOUT2_A	J10		
C8	VOUT2_B	J13		
C11	VOUT3_A	H10		
C12	VOUT3_B	H13		
D1	VOUT4_A	G10		
D7	VOUT4_B	G13		
D8	VOUT5_A	F10	LP0	=M4_BUCK1 137
D14	VOUT5_B	F13		
E3	VOUT6_A	E10	HP0	=M4_BUCK0 52 137
E4	VOUT6_B	E13		
E11	VOUT7_A	D10		
E12	VOUT7_B	D13		
F1	VOUT8_A	C10		
F14	VOUT8_B	C13		
G3	VOUT9_A	B10		
G4	VOUT9_B	B13		
G7	VOUT10_A	J9	HP1	=M4_BUCK2 52 137
G8	VOUT10_B	J6		
G11	VOUT11_A	H9		
G12	VOUT11_B	H6		
H1	VOUT12_A	G9		
H7	VOUT12_B	G6		
H8	VOUT13_A	F9		
H14	VOUT13_B	F6		
J3	VOUT14_A	E9		
J4	VOUT14_B	E6		
J11	VOUT15_A	D9		
J12	VOUT15_B	D6		
K4	VOUT16_A	C9		
K11	VOUT16_B	C6		
	VOUT17_A	B9		
	VOUT17_B	B6		
	VOUT18_A	L2	PACK_OPTION=CLVR_2C_SC	
	VOUT18_B	L5	UA500_L5	=M4_BUCK3 52 137
	VOUT19_A	K2	UA500_K2	LP1
	VOUT19_B	K5	UA500_K5	
	VOUT20_A	J2	UA500_J2	
	VOUT20_B	J5	UA500_J5	
	VOUT21_A	H2	UA500_H2	
	VOUT21_B	H5	UA500_H5	
	VOUT22_A	G2	UA500_G2	
	VOUT22_B	G5	UA500_G5	
	VOUT23_A	F2	UA500_F2	
	VOUT23_B	F5	UA500_F5	
	VOUT24_A	E2		
	VOUT24_B	E5		
	VOUT25_A	D2		
	VOUT25_B	D5		
	VOUT26_A	C2		
	VOUT26_B	C5		
	VOUT27_A	B2		
	VOUT27_B	B5	HP1	=M4_BUCK2 52 137

VDDH

138 51 50 =PP0V8_S2_CLVR_VDDDIG M6 VDD_DIG

138 53 52 51 50 =PP1V2_S2_CLVR_VDDIO M4 VDDIO

138 51 50 =PP1V8_S2_CLVR_VDDC M9 VDDC

51 50 PP1V8_CLVR_VDDC1 M10 VDDC1

XWA500 SHORT-16L-0.1MM-SM 1 2

137 IN =M4_BUCK0_FB L9 SVDD_HP0

M4_BUCK0_1_SVSS K8 SVSS_0

XWA501 SHORT-16L-0.1MM-SM 1 2

137 IN =M4_BUCK2_FB L6 SVDD_HP1

M4_BUCK2_3_SVSS K7 SVSS_1

137 IN =M4_BUCK1_FB L8 SVDD_LP0

137 IN =M4_BUCK3_FB L7 SVDD_LP1

137 53 52 51 50 =PP1V8_S1_CLVR_VDDH M7 SVDDH

OMIT_TABLE

UA500 MON BGA SYM 2 OF 2

A1	GPIO0	A10	CLVR4_GPIO0	B1 53
A2	GPIO1	B1	CLVR4_GPIO1	B1 53
A4	GPIO2	C1	CLVR4_GPIO2	PACK_OPTION=CLVR_C-CHOP / CLVR_FABRIC_ILIMIT_THROTTLE MAKE_BASE=TRUE OUT 53
A6	GPIO3	A13	CLVR4_GPIO3	B1 53
A9	GPIO4	A12	CLVR4_GPIO4	B1 53
A11	GPIO5	B14	CLVR4_GPIO5	B1 53
A14	JTAG_TCK/SWD_CLK	L1	SWD_CLVR4_SWCLK	IN 11
B3	JTAG_TMS/SWD_DAT	K1	SWD_CLVR4_SWDIO	B1 11
B7	JTAG_TDI	G1		
B8	JTAG_TDO	C14	NC_TDO4	
B12	JTAG_TRSTN	G14		
D3	ATB0	A3	NC_ATB40	
D4	ATB1	A8	NC_ATB41	
D11	ATB2	A5	NC_ATB42	
D12	ATB3	A7	NC_ATB43	
E1	SGPIO_CLK	M12	SGPIO_PMU_CLVR4_CLK	IN 13
E7	SGPIO_D	L12	SGPIO_PMU_CLVR4_DATA	B1 13
E8	ADDR0	M5	CLVR4_SGPIO_ADDR0	52
E14	ADDR1	M3	CLVR4_SGPIO_ADDR1	52
F3	SPMI_SCLK	K14	SPMI_CLVR4_CLK	IN 11
F4	SPMI_SDATA	L14	SPMI_CLVR4_DATA	B1 11
F7	CRASH*	M13	PMU_CRASH_L	B1 43 50 51 130
F8	UT*	M2	TP_CLVR4_UT_L	
F11	CLK32K	M11	PMU_CLK32K_CLVR	IN 44 50 51 130
F12	RESET*	L3	CLVR_RESET_L	IN 43 50 51 130
H3				
H4				
H11				
H12				
J1				
J7				
J8				
J14				
K3				
K6				
K9				
K12				
L4				
L11				
M1				
M14				

VSS

XWA502 SHORT-16L-0.1MM-SM 1 2 CLVR4_VSSC M8 VSSC

PACK_OPTION=CLVR_C-CHOP
=PP1V2_S2_CLVR_VDDIO IN 50 51 52 53 138
52 CLVR4_SGPIO_ADDR0
PACK_OPTION=CLVR_1C_2C
GND
MAKE_BASE=TRUE
52 CLVR4_SGPIO_ADDR1
MAKE_BASE=TRUE

137 52 =M4_BUCK3
CA544 12PF 5% 25V NP0-C0G 0201 | CA545 3.0PF +/-0.1PF 25V NP0-C0G 0201
PACK_OPTION=CLVR_2C_SC

137 52 =M4_BUCK0
CA540 12PF 5% 25V NP0-C0G 0201 | CA541 3.0PF +/-0.1PF 25V NP0-C0G 0201

137 52 =M4_BUCK2
CA542 12PF 5% 25V NP0-C0G 0201 | CA543 3.0PF +/-0.1PF 25V NP0-C0G 0201

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-24558	1	IC,MON,B0,OTP-QPJ,DEV,FCCSP168	UA500	CRITICAL	MONACO_SC
998-24559	1	IC,MON,B0,OTP-RPJ,DEV,FCCSP168	UA500	CRITICAL	MONACO_1C

BOM_COST_GROUP=SOC POWER

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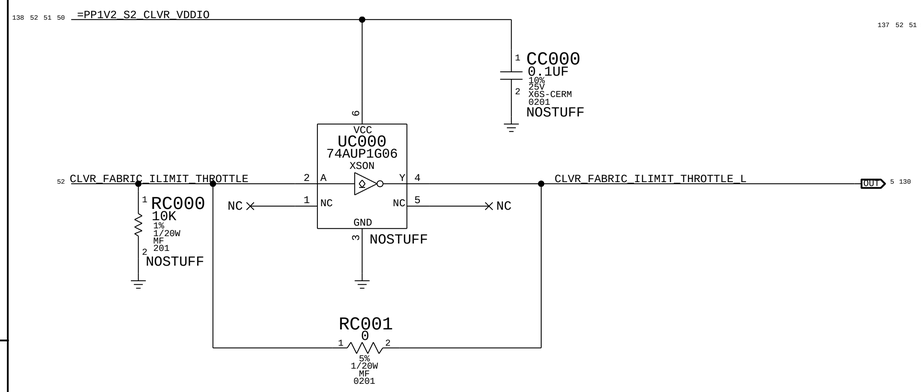
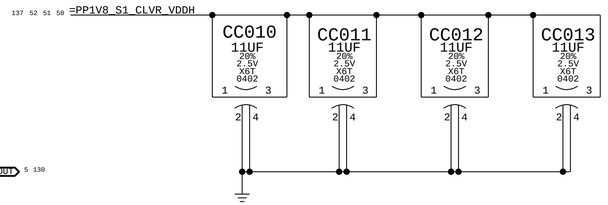


BYPASS ADDED FOR MONACO B0 - INTERCEPTING P2s



MONACO UNUSED GPIO's

MAKE_BASE=TRUE

50	CLVR0_GPIO0	NC_CLVR0_GPIO0
50	CLVR0_GPIO1	NC_CLVR0_GPIO1
50	CLVR0_GPIO2	NC_CLVR0_GPIO2
50	CLVR0_GPIO3	NC_CLVR0_GPIO3
50	CLVR0_GPIO4	NC_CLVR0_GPIO4
50	CLVR0_GPIO5	NC_CLVR0_GPIO5

MAKE_BASE=TRUE

51	CLVR1_GPIO0	NC_CLVR1_GPIO0
51	CLVR1_GPIO1	NC_CLVR1_GPIO1
51	CLVR1_GPIO2	NC_CLVR1_GPIO2
51	CLVR1_GPIO3	NC_CLVR1_GPIO3
51	CLVR1_GPIO4	NC_CLVR1_GPIO4
51	CLVR1_GPIO5	NC_CLVR1_GPIO5

MAKE_BASE=TRUE

52	CLVR4_GPIO0	NC_CLVR4_GPIO0
52	CLVR4_GPIO1	NC_CLVR4_GPIO1
52	CLVR4_GPIO3	NC_CLVR4_GPIO3
52	CLVR4_GPIO4	NC_CLVR4_GPIO4
52	CLVR4_GPIO5	NC_CLVR4_GPIO5

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=STUZMAN SYNC_DATE=01/16/2020

PAGE TITLE

MONACO PROJECT SUPPORT

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* OK2INTEGRATE *

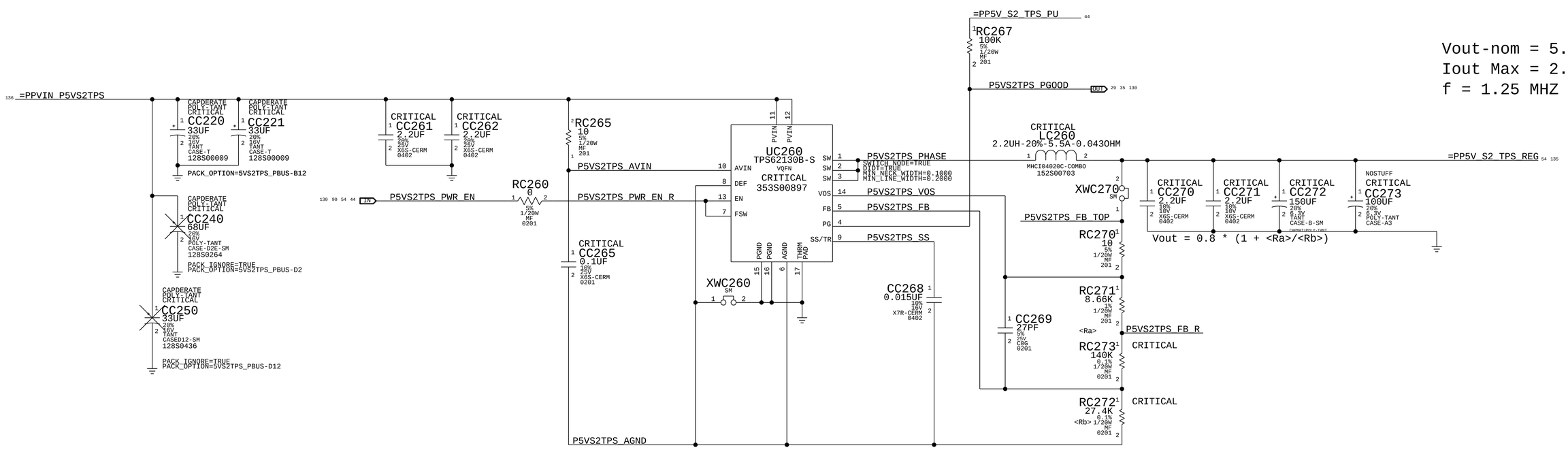
5V_S2 Voltage Regulator (low power option)

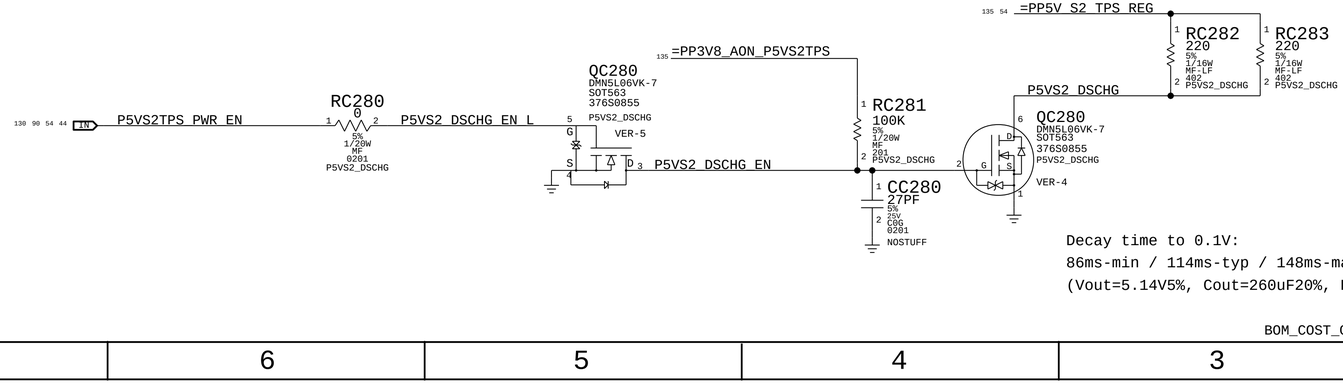
SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=5VS2TPS_PBUS-B12
PACK_OPTION=5VS2TPS_PBUS-D2
PACK_OPTION=5VS2TPS_PBUS-D12

START UP TIME = 4.7/7.5/10.5 MS
(min/typ/max)

Vout-nom = 5.14V
Iout Max = 2.1A
f = 1.25 MHZ





Decay time to 0.1V:
86ms-min / 114ms-typ / 148ms-max
(Vout=5.14V5%, Cout=260uF20%, R=2x220R5%)

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
POWER: 5V S2 TPS62130

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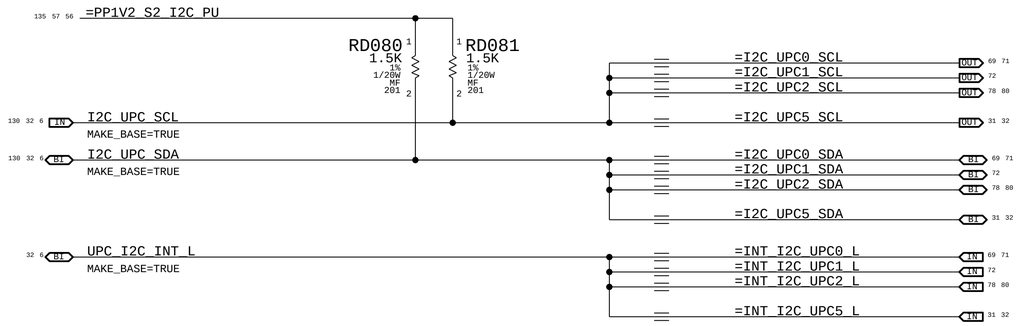
AP_I2C0

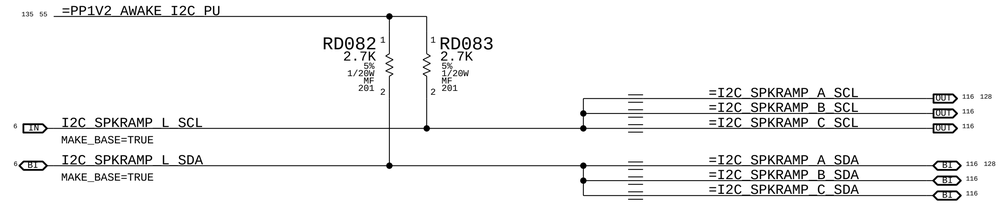
DEVICE	CARD/REFDES	7-BIT	8-BIT
ACE2 - 0 (DEBUG)	USB-C 0	0X38	0X70
ACE2 - 1 (DEBUG)	USB-C 0	0X3F	0X7E
ACE2 - 2 (DEBUG)	USB-C 1	0X3B	0X76
ACE2 - 5 (DEBUG)	USB-C 1	0X3A	0X74
BANK ALL CALL		0X6B	0XD6

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
?	?	?	?	?	?
?	?	?	?	?	?
?	?	?	?	?	?



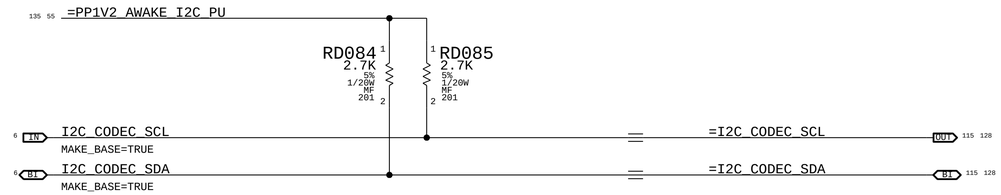
AP_I2C1

DEVICE	CARD/REFDES	7-BIT	8-BIT
SPKRAMP TAWANG A	SPKRAMP	0X38	0X70
SPKRAMP TAWANG B	SPKRAMP	0X39	0X72
SPKRAMP TAWANG C	SPKRAMP	0X3A	0X74



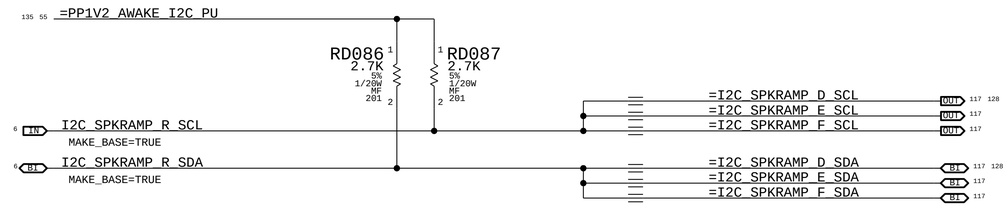
AP_I2C2

DEVICE	CARD/REFDES	7-BIT	8-BIT
CODEC - CLIFDEN	DMIC & CODEC	0X48	0X90
CODEC - CARLOW POR	DMIC & CODEC	0X4B	0X95



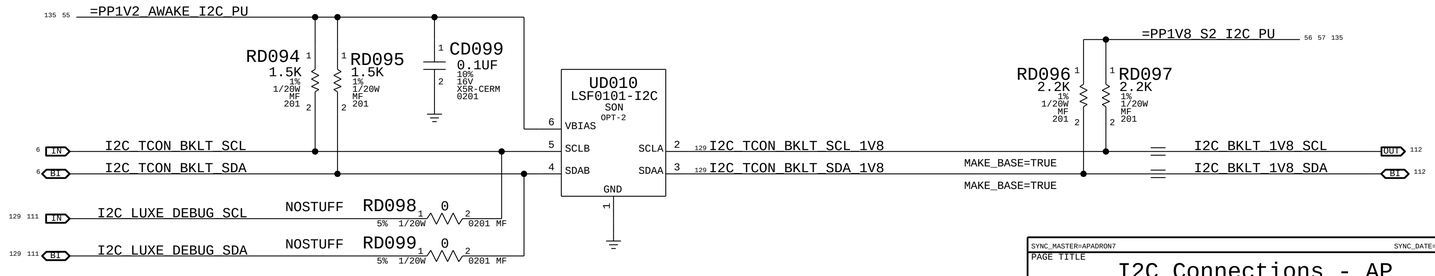
AP_I2C3

DEVICE	CARD/REFDES	7-BIT	8-BIT
SPKRAMP TAWANG D	SPKRAMP	0X3B	0X76
SPKRAMP TAWANG E	SPKRAMP	0X3C	0X78
SPKRAMP TAWANG F	SPKRAMP	0X3D	0X7A



AP_I2C7

DEVICE	CARD/REFDES	7-BIT	8-BIT
Avellino PMIC	Display	0XXX	0XX



UNUSED:

AOP_I2C1
ISP_I2C0
ISP_I2C1
ISP_I2C3

BOM_COST_GROUP=SOC

SYNC_MASTER=APADRON7 SYNC_DATE=03/04/2020

PAGE TITLE

I2C Connections - AP

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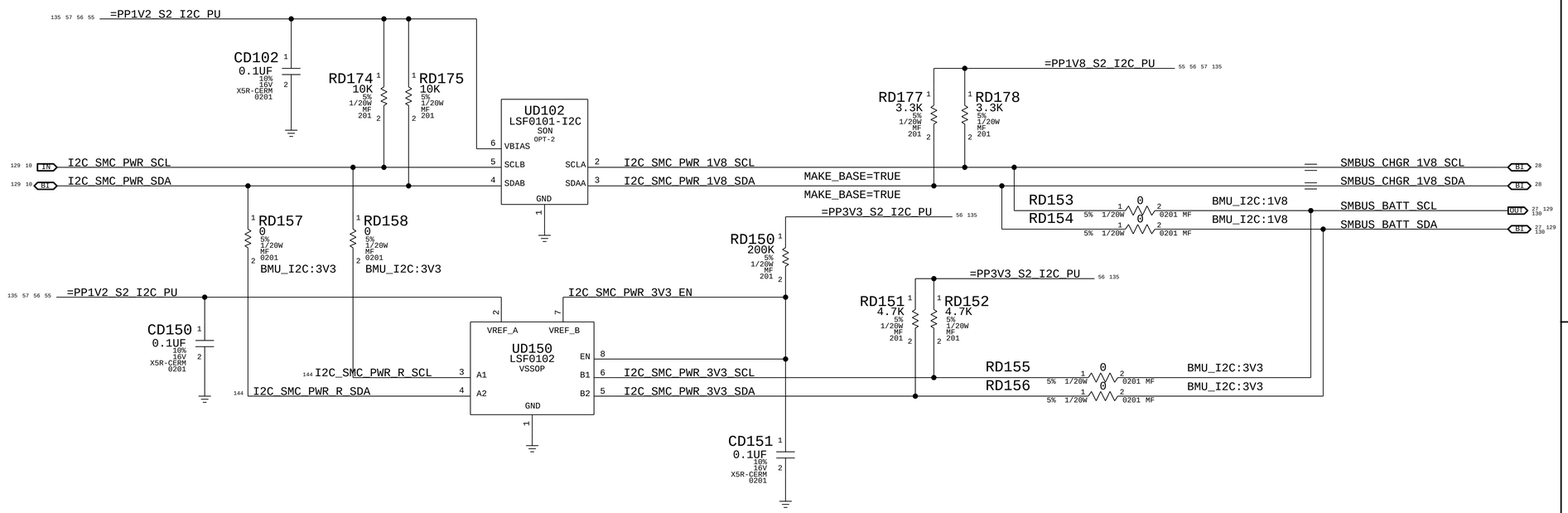
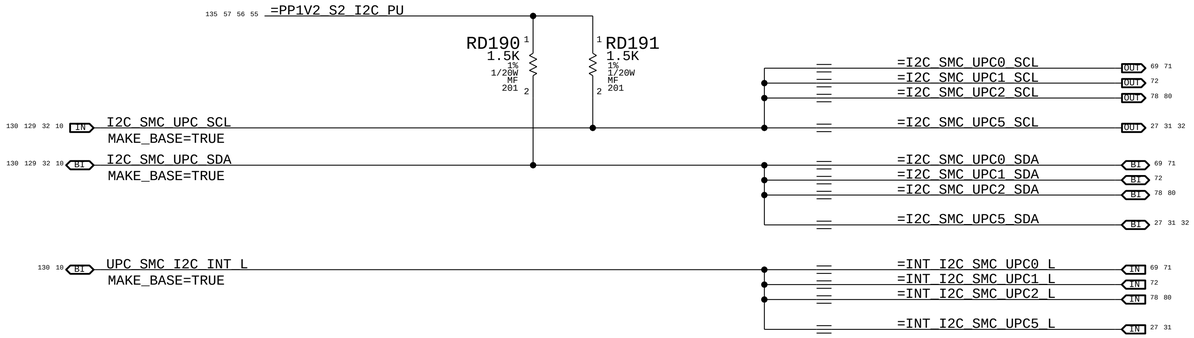
SMC_I2C0

DEVICE	CARD/REFDES	7-BIT	8-BIT
CHARGER - SUONA	BATT/CHARGER	0X09	0X12
CHARGER - WHAMOLA	BATT/CHARGER	0X??	??
ICEMAN	U5700	0XXX	0XX
BMU	BMU	0X0B	0X16



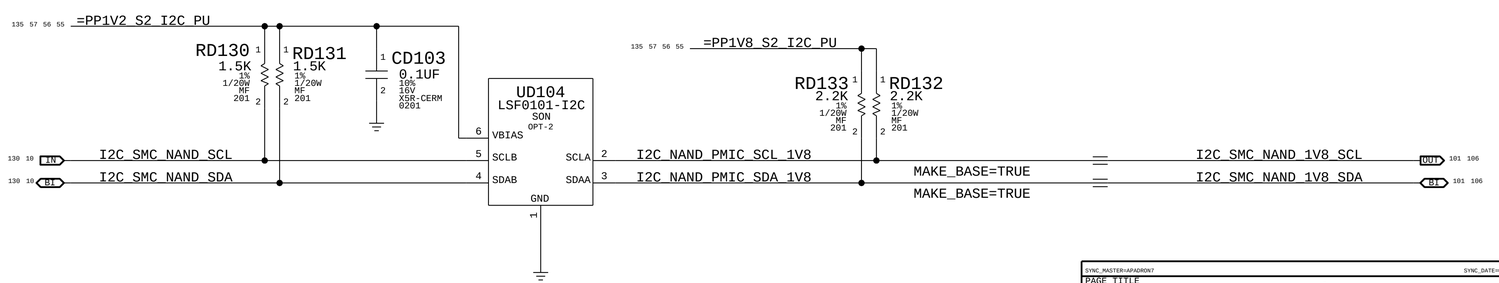
SMC_I2C1

DEVICE	CARD/REFDES	7-BIT	8-BIT
ACE2 - 0 (DEBUG)	USB-C 0	0X38	0X70
ACE2 - 1 (DEBUG)	USB-C 0	0X3F	0X7E
ACE2 - 2 (DEBUG)	USB-C 1	0X3B	0X76
ACE2 - 5 (DEBUG)	USB-C 1	0X3A	0X74
BANK1 ALL CALL		0X6B	0XD6



SMC_I2C2

DEVICE	CARD/REFDES	7-BIT	8-BIT
NAND PMIC 0	NAND 0	0X79	0XF2
NAND PMIC 1	NAND 1	0X78	0XF0



BOM_COST_GROUP=SOC

SYNC_MASTER=APADRIN7 SYNC_DATE=03/04/2020

PAGE TITLE

I2C Connections - SMC

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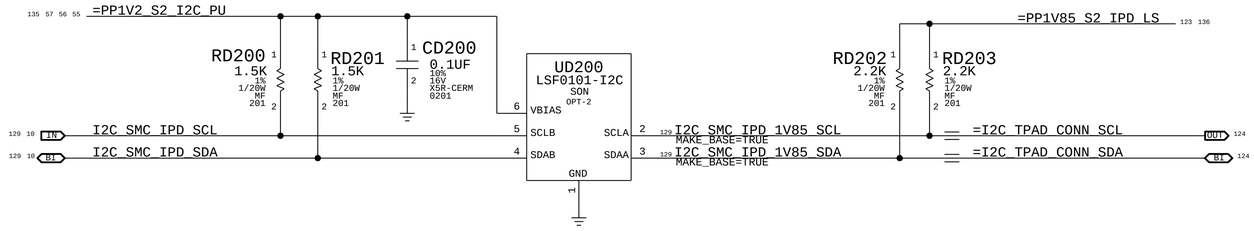
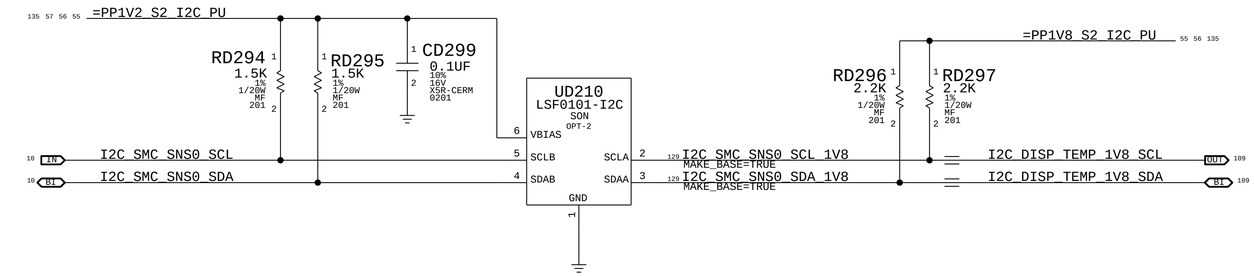
SMC_I2C3

DEVICE	CARD/REFDES	7-BIT	8-BIT
Palm Rest Temp	IPD	0X4C	0X98



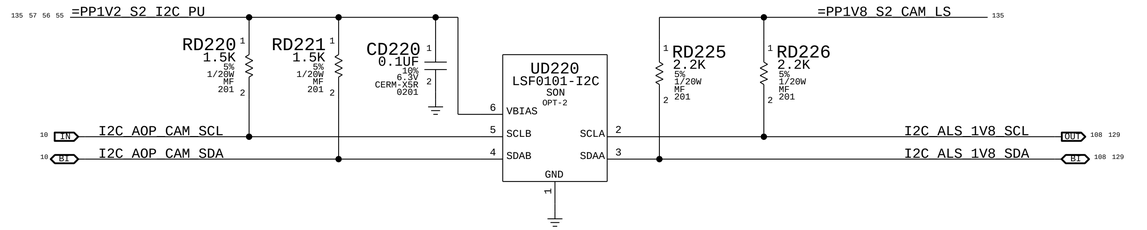
SMC_I2C4

DEVICE	CARD/REFDES	7-BIT	8-BIT
Temp Sensors	DISPLAY TEMP SNS	0X48	0X90



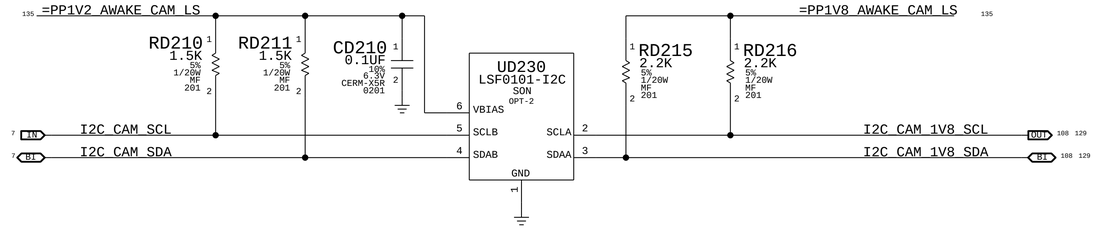
AOP_I2C0

DEVICE	CARD/REFDES	7-BIT	8-BIT
ALS	Camera	0X29	0X52
ALS Temp	Camera	0X24	0X48



ISP_I2C2

DEVICE	CARD/REFDES	7-BIT	8-BIT
FHSi+	Camera	0X10	0X20
Camera Sensor	Camera	0X6C	0XD8



UNUSED and already aliased
ISP_I2C0 SMC_I2C6
ISP_I2C1
ISP_I2C3
AOP_I2C1

SI2C

DEVICE	CARD/REFDES	7-BIT	8-BIT
SEP EEPROM	U0500	0XXX	0XX

Need to confirm if this needs/has pull-ups

MISSING WLAN/BT, R1, CELL - VENDOR CARDS

BOM_COST_GROUP=SOC

SYNC_MASTER=APADRON7 SYNC_DATE=03/04/2020

PAGE TITLE: I2C Connections - Other

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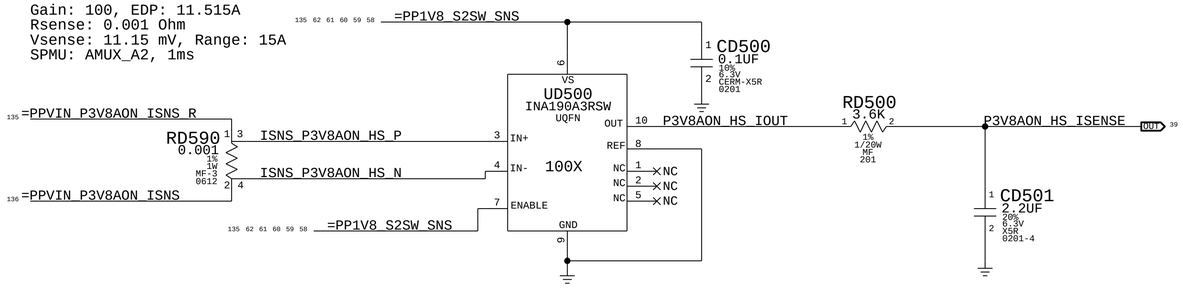
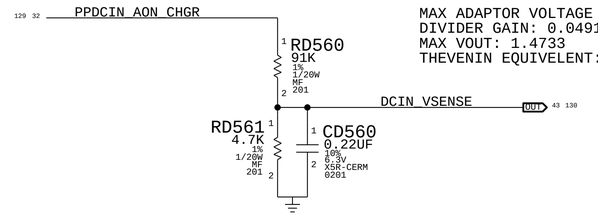
P3V8 AON HIGH SIDE ISENSE

Gain: 100, EDP: 11.515A
Rsense: 0.001 Ohm
Vsense: 11.15 mV, Range: 15A
SPMU: AMUX_A2, 1ms



DCIN VOLTAGE SENSE

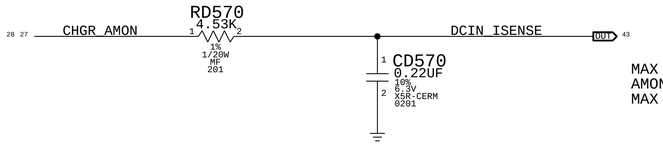
MPMU: AMUX_A0, 1ms



MAX ADAPTOR VOLTAGE = 28V + 5% -> 30V
DIVIDER GAIN: 0.0491
MAX VOUT: 1.4733
THEVENIN EQUIVELENT: 4.47K

DCIN ISENSE AMON

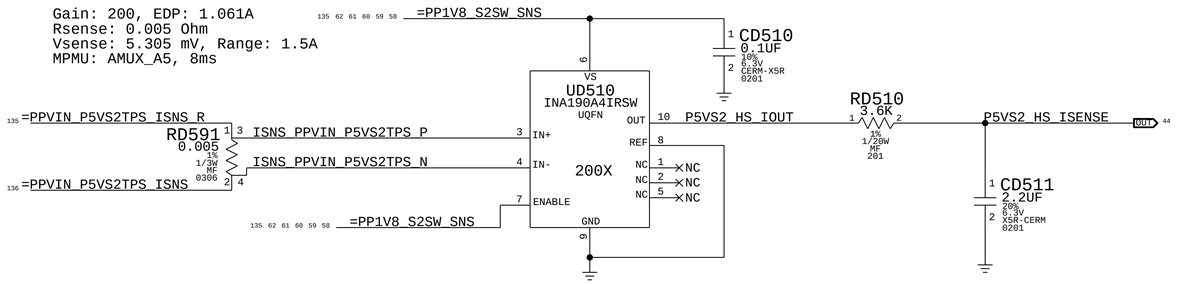
MPMU: AMUX_A1, 1ms



MAX ADAPTOR CURRENT: 5A
AMON GAIN, RSENSE: 20X, 10m
MAX AMON OUTPUT VOLTAGE: 1V

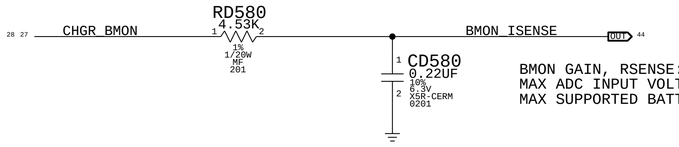
5V S2 VR HIGH SIDE ISENSE

Gain: 200, EDP: 1.061A
Rsense: 0.005 Ohm
Vsense: 5.305 mV, Range: 1.5A
MPMU: AMUX_A5, 8ms



BATTERY ISENSE BMON

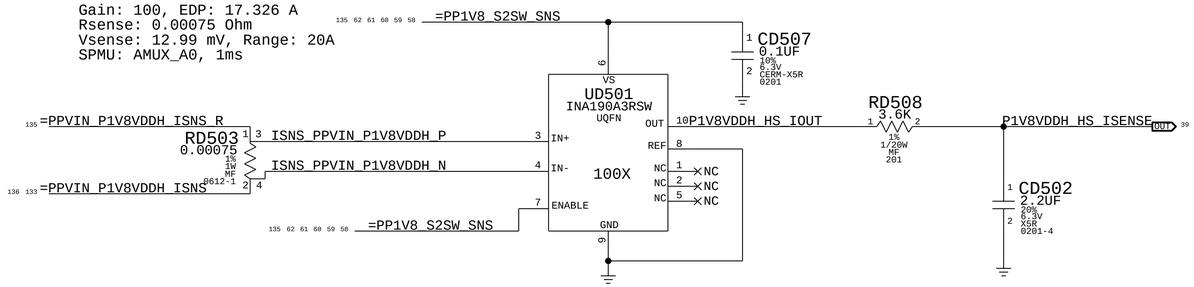
MPMU: AMUX_A2, 1ms



BMON GAIN, RSENSE: 7.9X, 5m
MAX ADC INPUT VOLTAGE: 1.5V (G=1)
MAX SUPPORTED BATTERY CURRENT SENSE: 37.97A

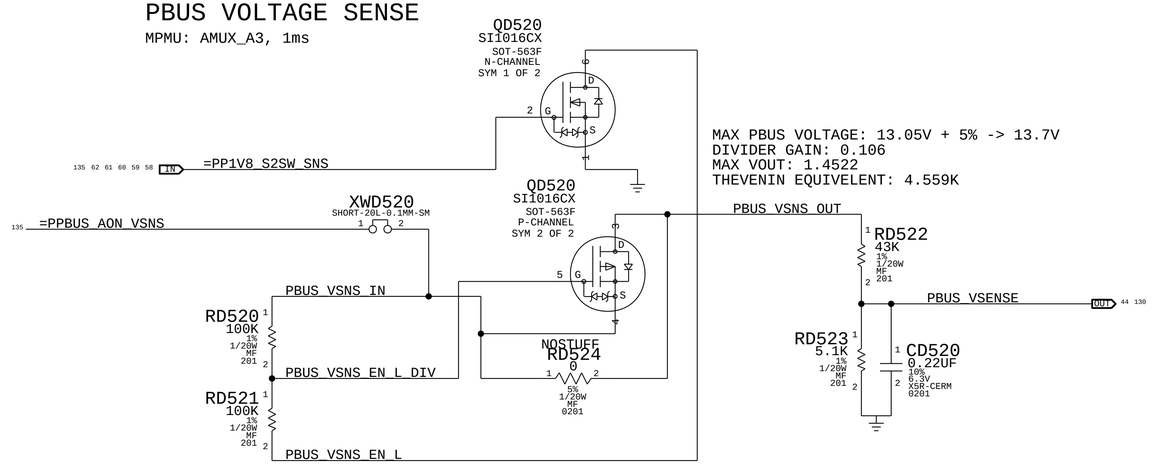
P1V8VDDH HIGH SIDE ISENSE

Gain: 100, EDP: 17.326 A
Rsense: 0.00075 Ohm
Vsense: 12.99 mV, Range: 20A
SPMU: AMUX_A0, 1ms



PBUS VOLTAGE SENSE

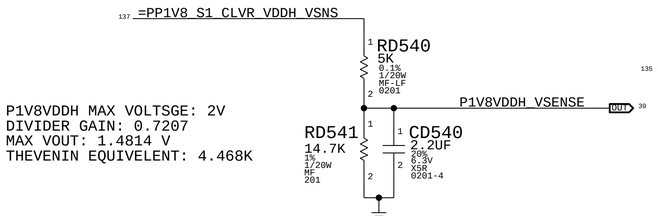
MPMU: AMUX_A3, 1ms



MAX PBUS VOLTAGE: 13.05V + 5% -> 13.7V
DIVIDER GAIN: 0.106
MAX VOUT: 1.4522
THEVENIN EQUIVELENT: 4.559K

P1V8VDDH VSENSE

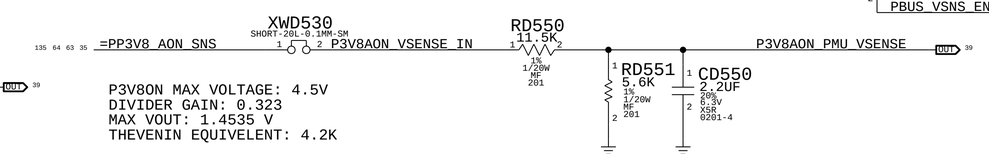
SPMU: AMUX_A1, 1ms



P1V8VDDH MAX VOLTSGE: 2V
DIVIDER GAIN: 0.7207
MAX VOUT: 1.4814 V
THEVENIN EQUIVELENT: 4.468K

P3V8AON VSENSE

SPMU: AMUX_A2, 1ms



P3V8ON MAX VOLTAGE: 4.5V
DIVIDER GAIN: 0.323
MAX VOUT: 1.4535 V
THEVENIN EQUIVELENT: 4.2K

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: HIGH-SIDE (1/2)

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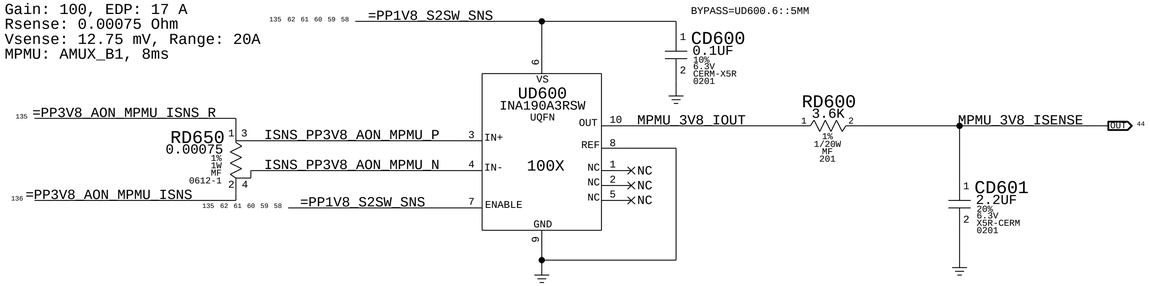
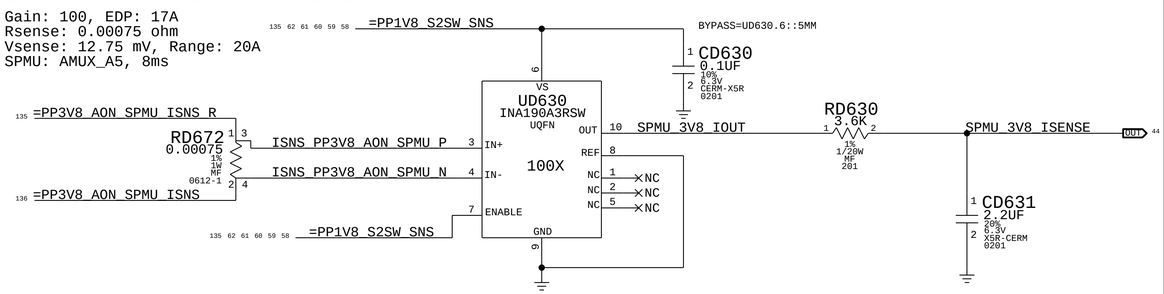
MASTER PMU HIGH SIDE 3V8 ISENSE

Gain: 100, EDP: 17 A
Rsense: 0.00075 Ohm
Vsense: 12.75 mV, Range: 20A
MPMU: AMUX_B1, 8ms



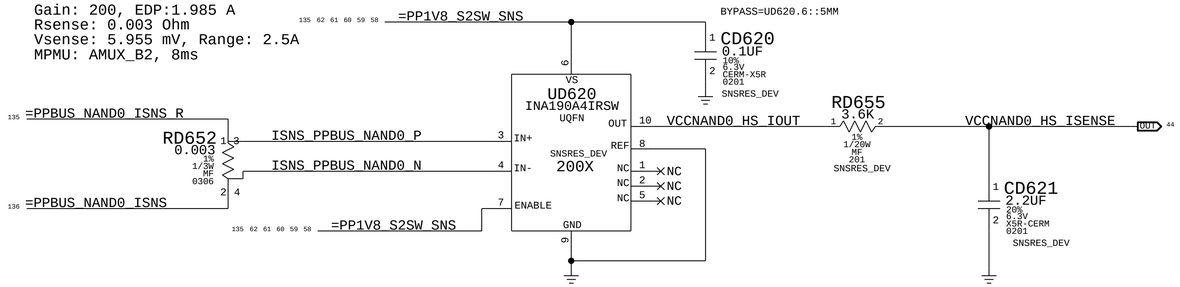
SLAVE PMU HIGH SIDE 3V8 ISENSE

Gain: 100, EDP: 17A
Rsense: 0.00075 ohm
Vsense: 12.75 mV, Range: 20A
SPMU: AMUX_A5, 8ms



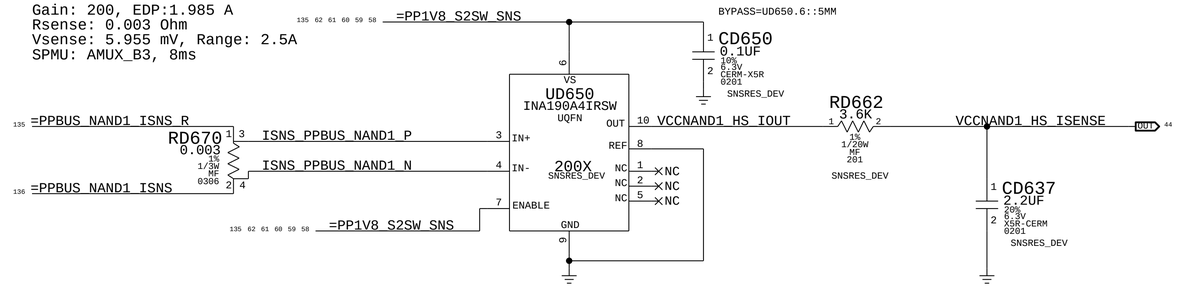
NAND 0 PBUS ISENSE

Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
MPMU: AMUX_B2, 8ms



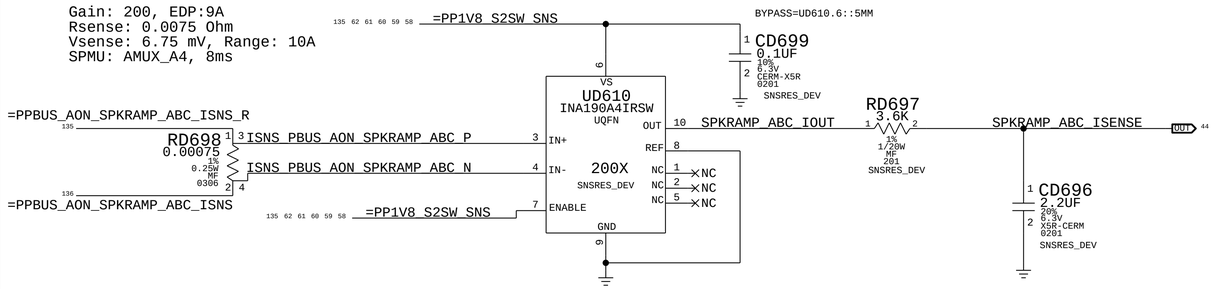
NAND 1 PBUS ISENSE

Gain: 200, EDP:1.985 A
Rsense: 0.003 Ohm
Vsense: 5.955 mV, Range: 2.5A
SPMU: AMUX_B3, 8ms



LEFT SPKRAMP PBUS ISENSE

Gain: 200, EDP:9A
Rsense: 0.0075 Ohm
Vsense: 6.75 mV, Range: 10A
SPMU: AMUX_A4, 8ms



BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: HIGH-SIDE (2/2)

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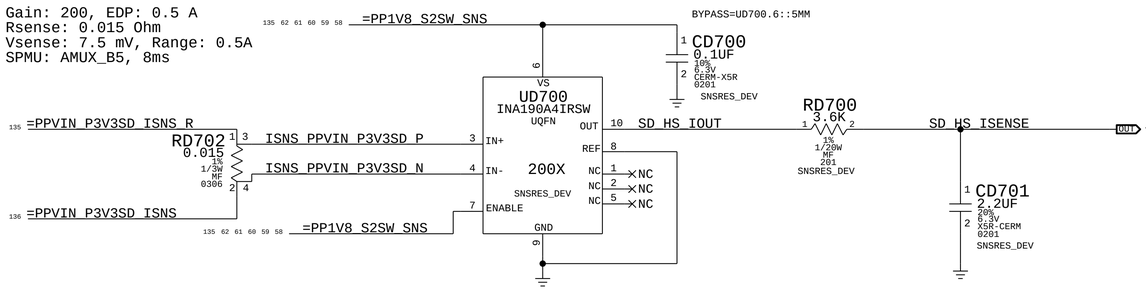
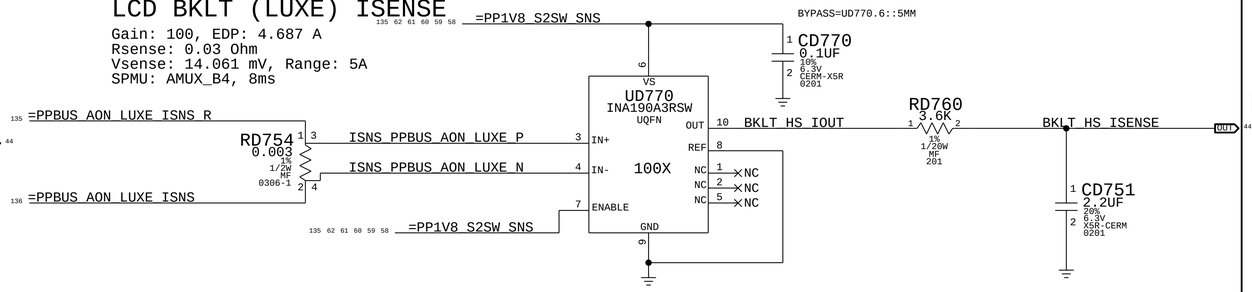
SD PBUS ISENSE

Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
SPMU: AMUX_B5, 8ms



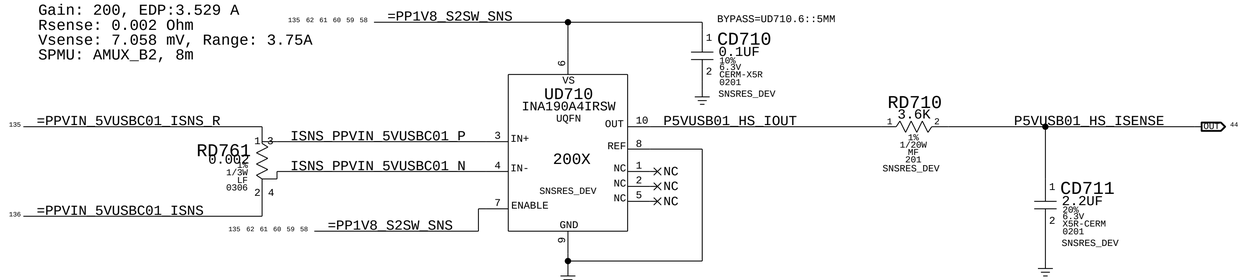
LCD BKLT (LUXE) ISENSE

Gain: 100, EDP: 4.687 A
Rsense: 0.03 Ohm
Vsense: 14.061 mV, Range: 5A
SPMU: AMUX_B4, 8ms



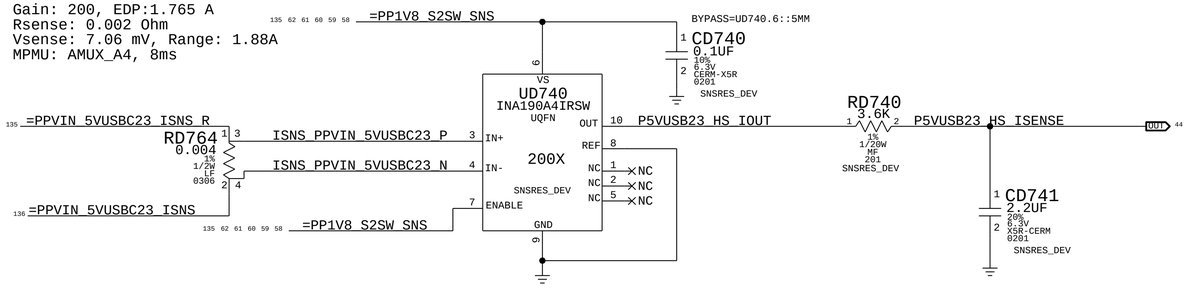
USB 5V OUT LEFT ISENSE

Gain: 200, EDP:3.529 A
Rsense: 0.002 Ohm
Vsense: 7.058 mV, Range: 3.75A
SPMU: AMUX_B2, 8m



USB 5V OUT RIGHT ISENSE

Gain: 200, EDP:1.765 A
Rsense: 0.002 Ohm
Vsense: 7.06 mV, Range: 1.88A
MPMU: AMUX_A4, 8ms



SYNC_MASTER=HKUKRATI SYNC_DATE=03/02/2020

PAGE TITLE
SENSORS: HIGH-SIDE

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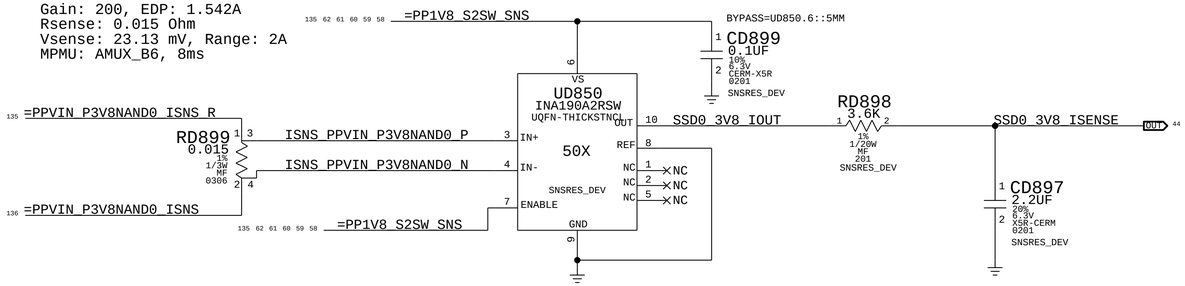
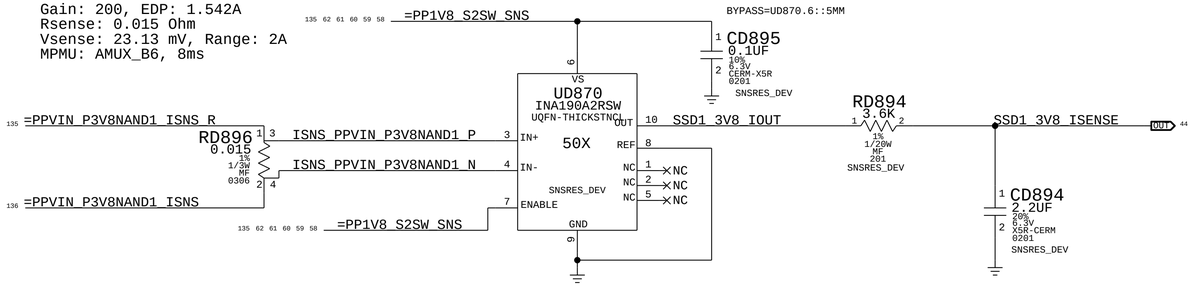
OCARINA 0 ISENSE

Gain: 200, EDP: 1.542A
Rsense: 0.015 Ohm
Vsense: 23.13 mV, Range: 2A
MPMU: AMUX_B6, 8ms



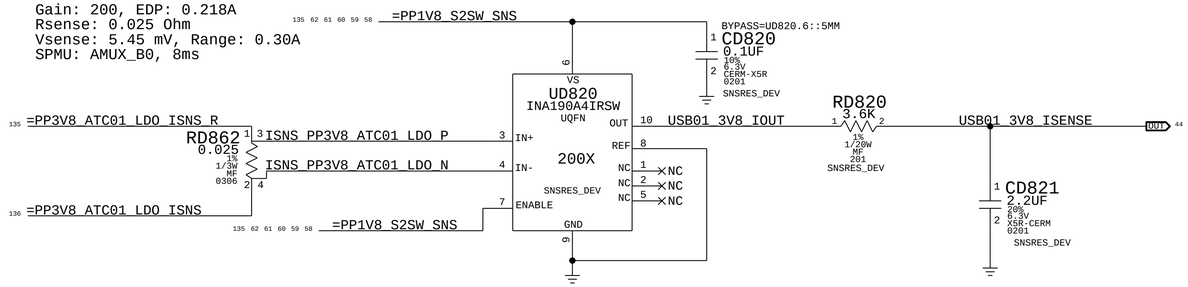
OCARINA 1 ISENSE

Gain: 200, EDP: 1.542A
Rsense: 0.015 Ohm
Vsense: 23.13 mV, Range: 2A
MPMU: AMUX_B6, 8ms



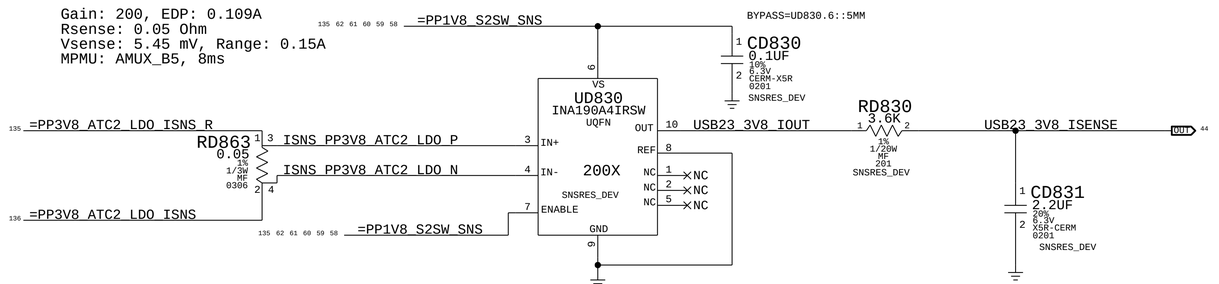
USB 3V8 LEFT ISENSE

Gain: 200, EDP: 0.218A
Rsense: 0.025 Ohm
Vsense: 5.45 mV, Range: 0.30A
SPMU: AMUX_B0, 8ms



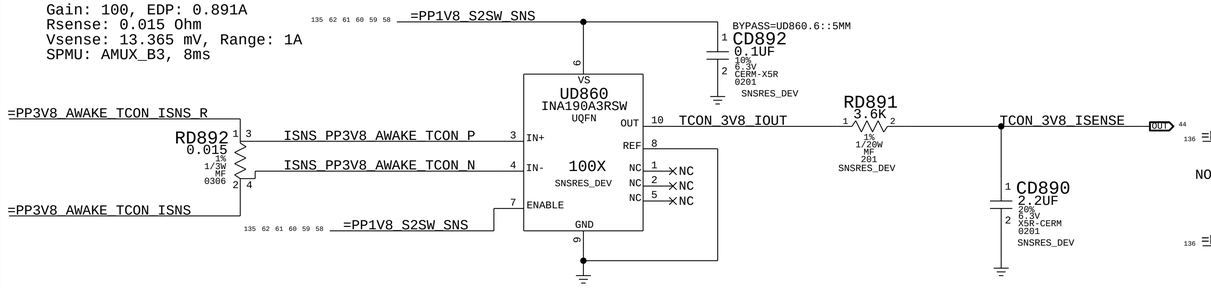
USB 3V8 RIGHT ISENSE

Gain: 200, EDP: 0.109A
Rsense: 0.05 Ohm
Vsense: 5.45 mV, Range: 0.15A
MPMU: AMUX_B5, 8ms



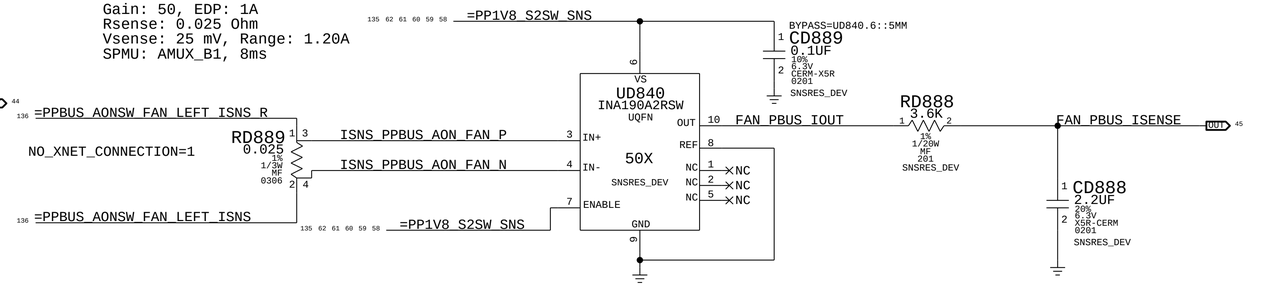
DISPLAY (TCON) 3V8 ISENSE

Gain: 100, EDP: 0.891A
Rsense: 0.015 Ohm
Vsense: 13.365 mV, Range: 1A
SPMU: AMUX_B3, 8ms



LEFT FAN PBUS ISENSE

Gain: 50, EDP: 1A
Rsense: 0.025 Ohm
Vsense: 25 mV, Range: 1.20A
SPMU: AMUX_B1, 8ms



BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: LOW-SIDE (1/3)

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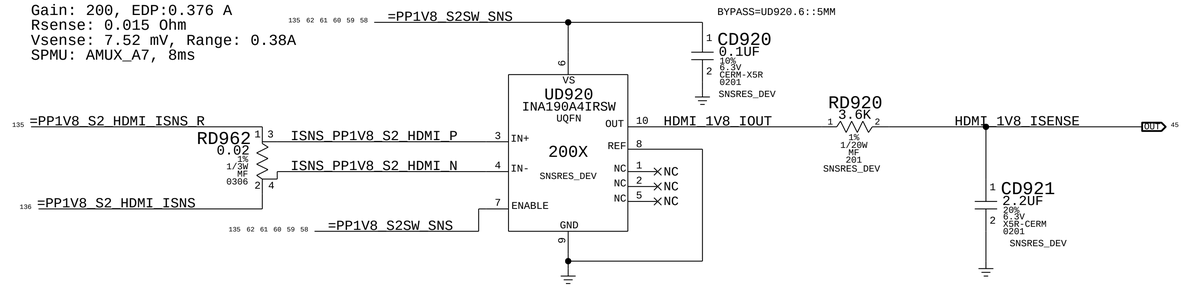
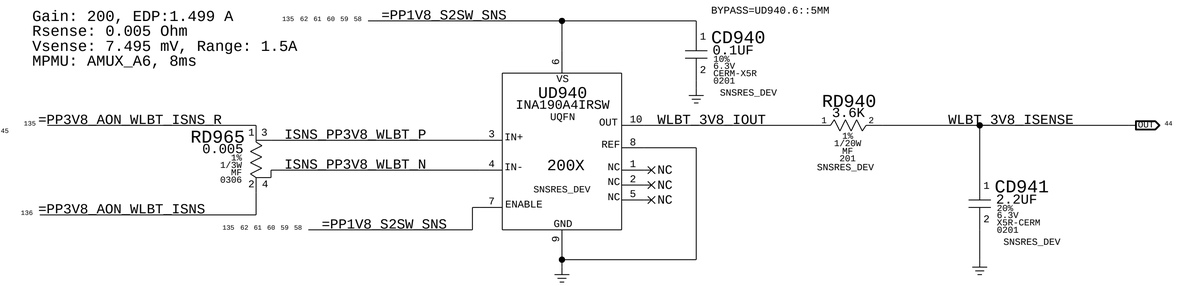
HDMI 1V8 ISENSE

Gain: 200, EDP:0.376 A
Rsense: 0.015 Ohm
Vsense: 7.52 mV, Range: 0.38A
SPMU: AMUX_A7, 8ms



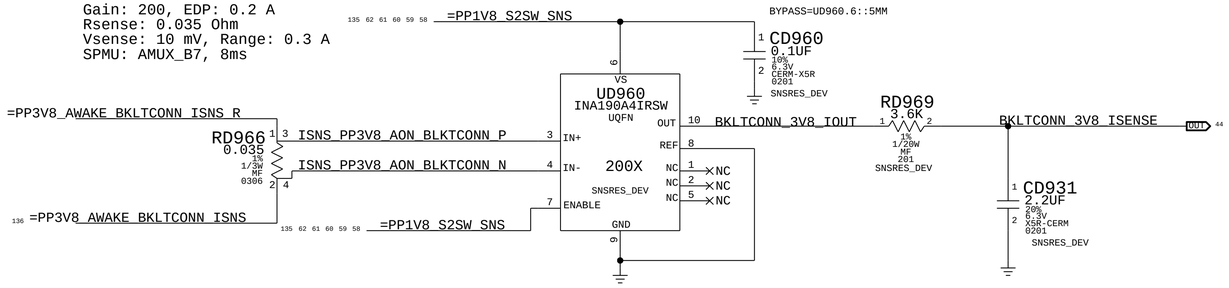
WLAN BT 3V8 ISENSE

Gain: 200, EDP:1.499 A
Rsense: 0.005 Ohm
Vsense: 7.495 mV, Range: 1.5A
MPMU: AMUX_A6, 8ms



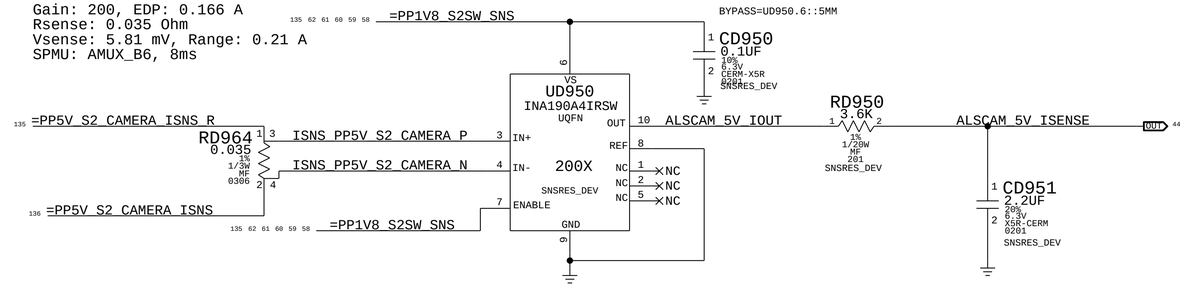
DISPLAY BACKLIGHT 3V8 ISENSE

Gain: 200, EDP: 0.2 A
Rsense: 0.035 Ohm
Vsense: 10 mV, Range: 0.3 A
SPMU: AMUX_B7, 8ms



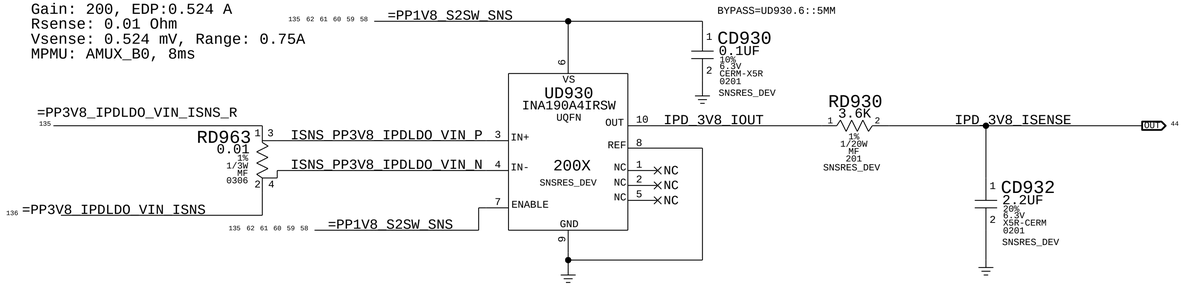
CAMERA 5V ISENSE

Gain: 200, EDP: 0.166 A
Rsense: 0.035 Ohm
Vsense: 5.81 mV, Range: 0.21 A
SPMU: AMUX_B6, 8ms



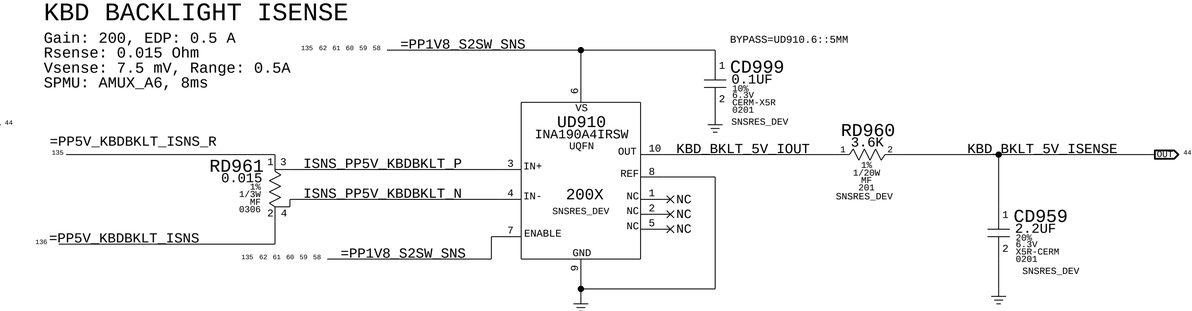
IPD 3V8 ISENSE

Gain: 200, EDP:0.524 A
Rsense: 0.01 Ohm
Vsense: 0.524 mV, Range: 0.75A
MPMU: AMUX_B0, 8ms



KBD BACKLIGHT ISENSE

Gain: 200, EDP: 0.5 A
Rsense: 0.015 Ohm
Vsense: 7.5 mV, Range: 0.5A
SPMU: AMUX_A6, 8ms



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: LOW-SIDE (2/3)

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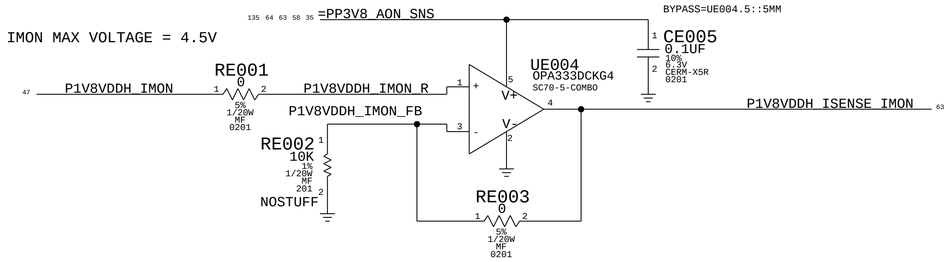
P1V8VDDH LOW SIDE ISENSE (IMON)

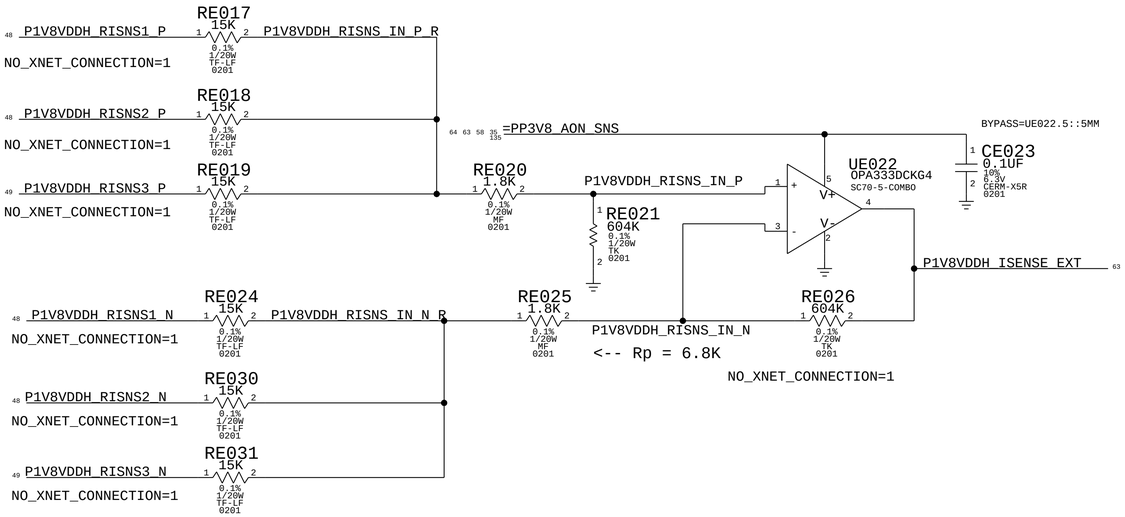
MPMU AMUX_B4, 8ms, VMAX AFTER DIVIDER = 1.51V



P1V8VDDH LOW SIDE ISENSE (SUMMING AMP FOR 3 PHASES)

EDP: 90A, 30A/PHASE, G=88.82, MAX CURRENT SENSE = 100A

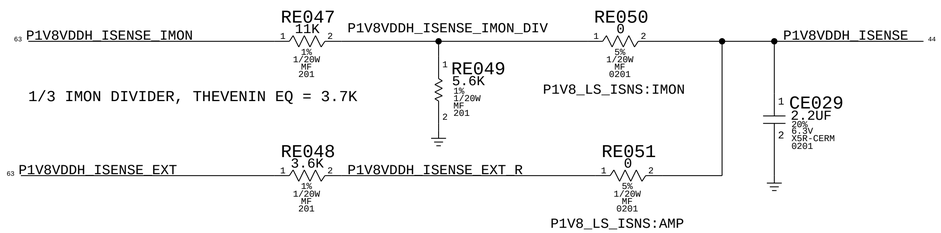
SPMU AMUX_A7, 8ms

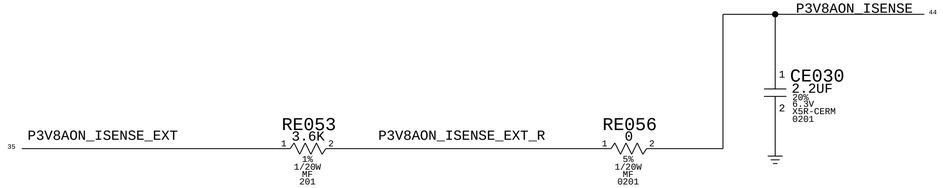


P3V8 LOW SIDE ISENSE (SUMMING AMP FOR 3 PHASES)

Moved to CSA 60

RESISTOR STUFFING OPTION FOR IMON OR SUMMING AMP





BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: LOW-SIDE (3/3)

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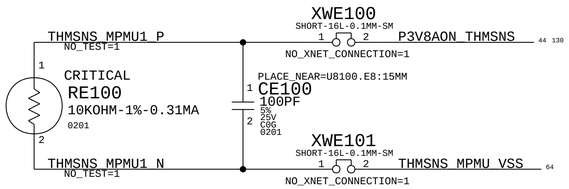
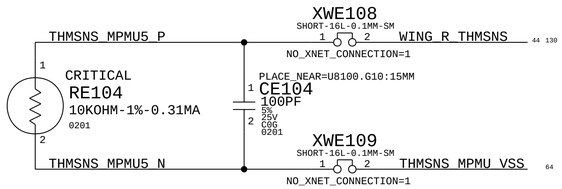
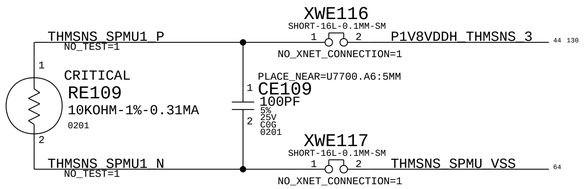
MASTER PMU TDEV1



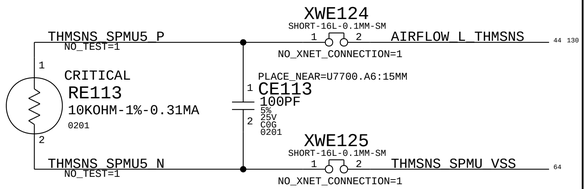
MASTER PMU TDEV5



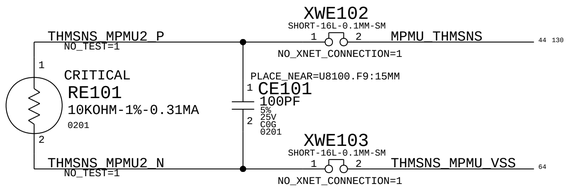
SLAVE PMU TDEV1



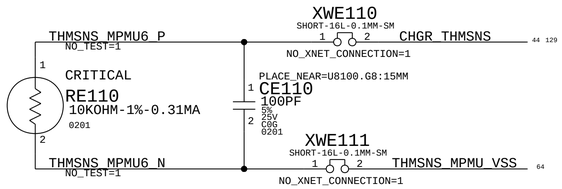
SLAVE PMU TDEV5



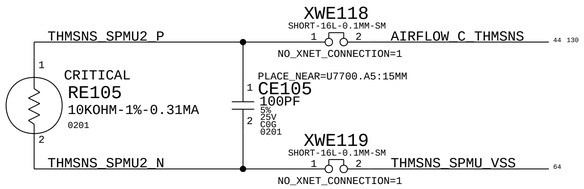
MASTER PMU TDEV2



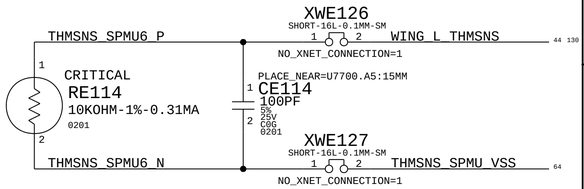
MASTER PMU TDEV6



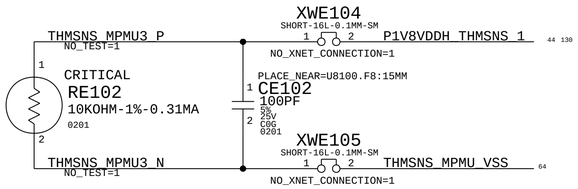
SLAVE PMU TDEV2



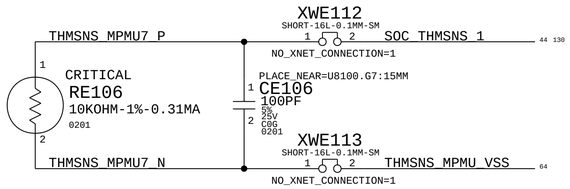
SLAVE PMU TDEV6



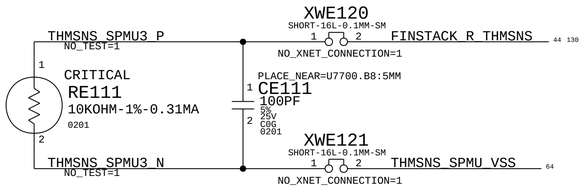
MASTER PMU TDEV3



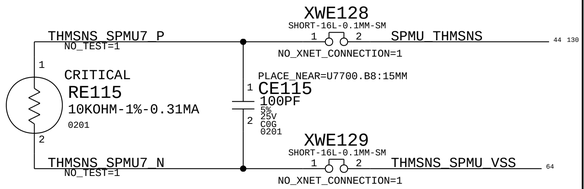
MASTER PMU TDEV7



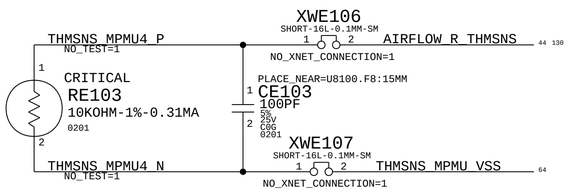
SLAVE PMU TDEV3



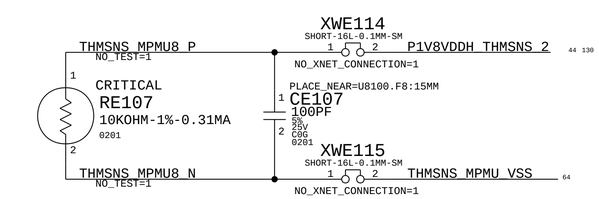
SLAVE PMU TDEV7



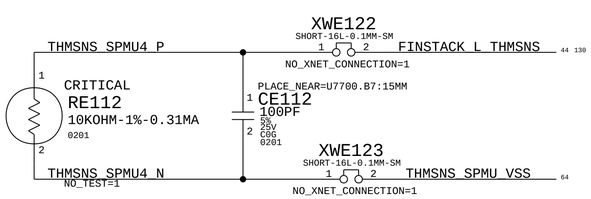
MASTER PMU TDEV4



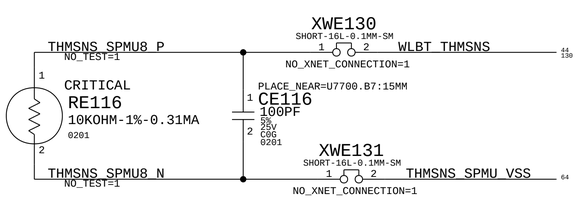
MASTER PMU TDEV8



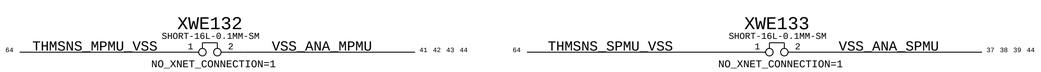
SLAVE PMU TDEV4



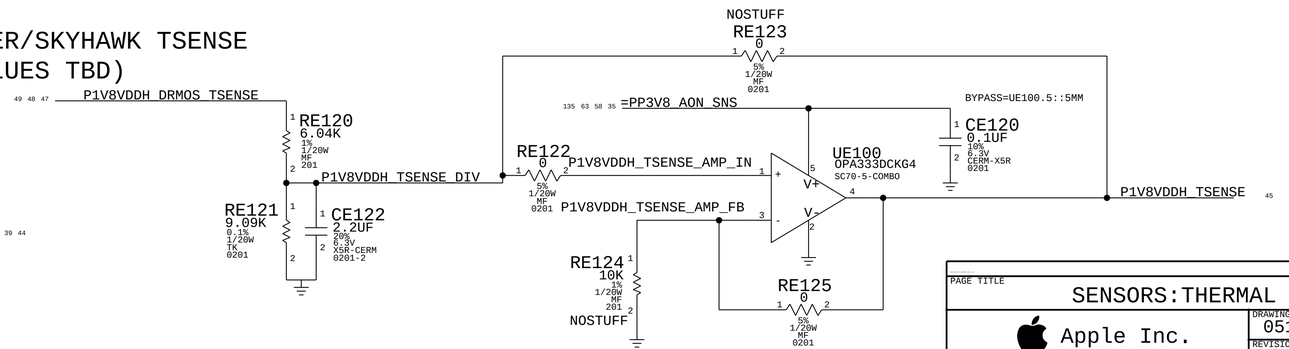
SLAVE PMU TDEV8



MPMU AND SPMU ANALOG GROUND CONNECTION



VIPER/SKYHAWK TSENSE (VALUES TBD)



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS:THERMAL

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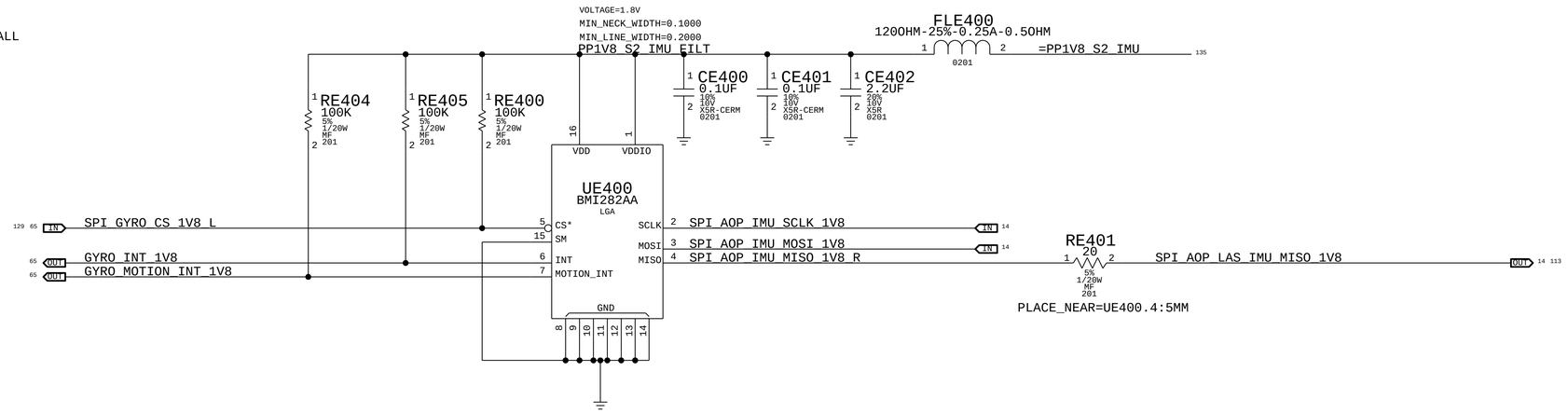
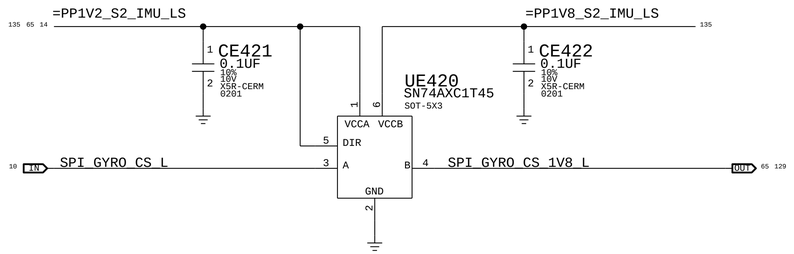
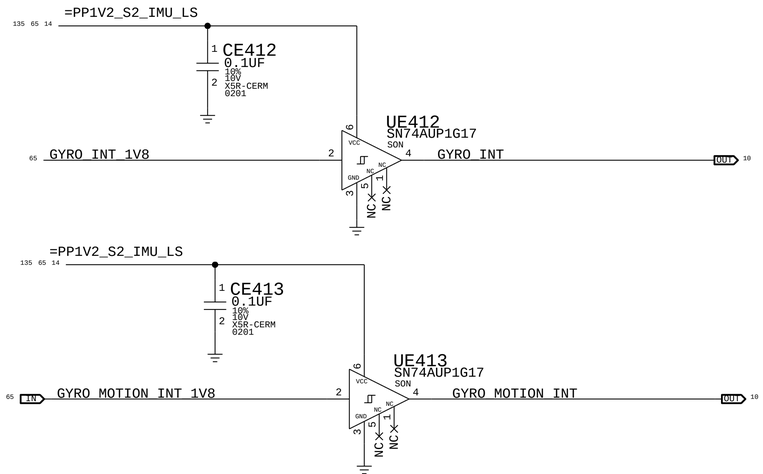
KOBOL: ACCEL & GYRO

FERRITE IS PLACEHOLDER ONLY
J417 USES 1555S0686 (01005)
MUST FIND PROPER PART, IF ONE IS NEEDED AT ALL



SPI LEVEL TRANSLATION





BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: MOTION

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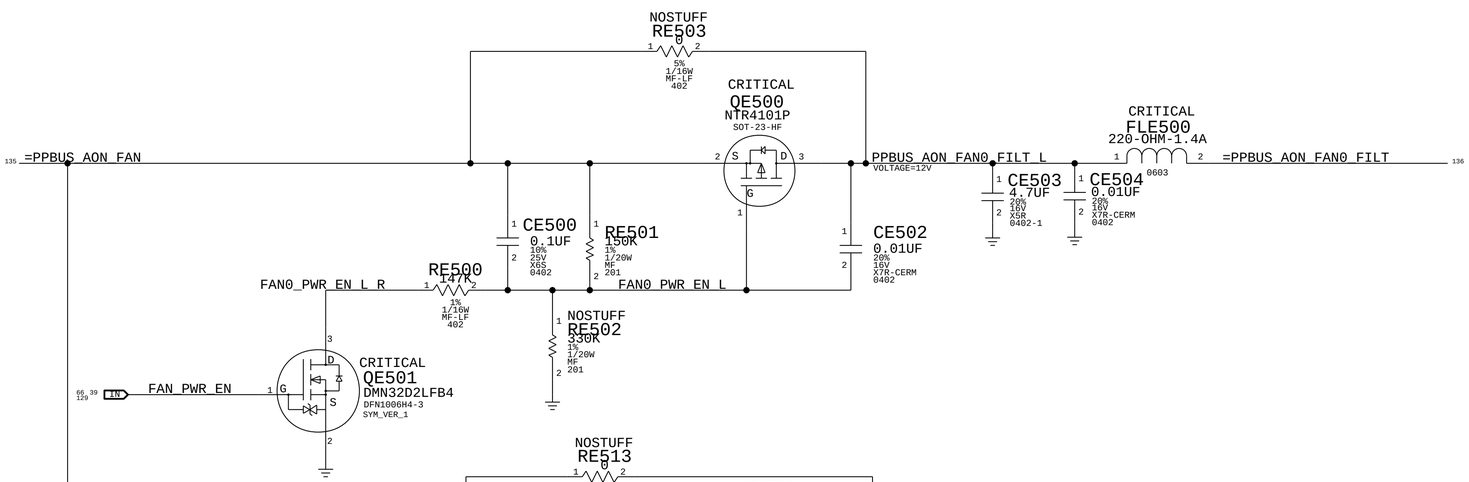
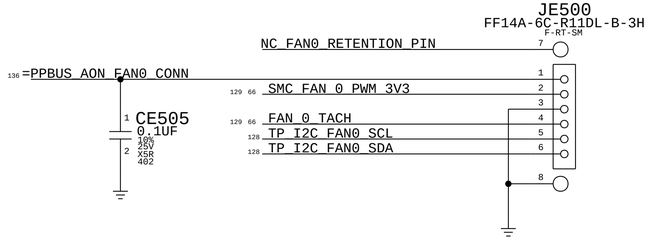
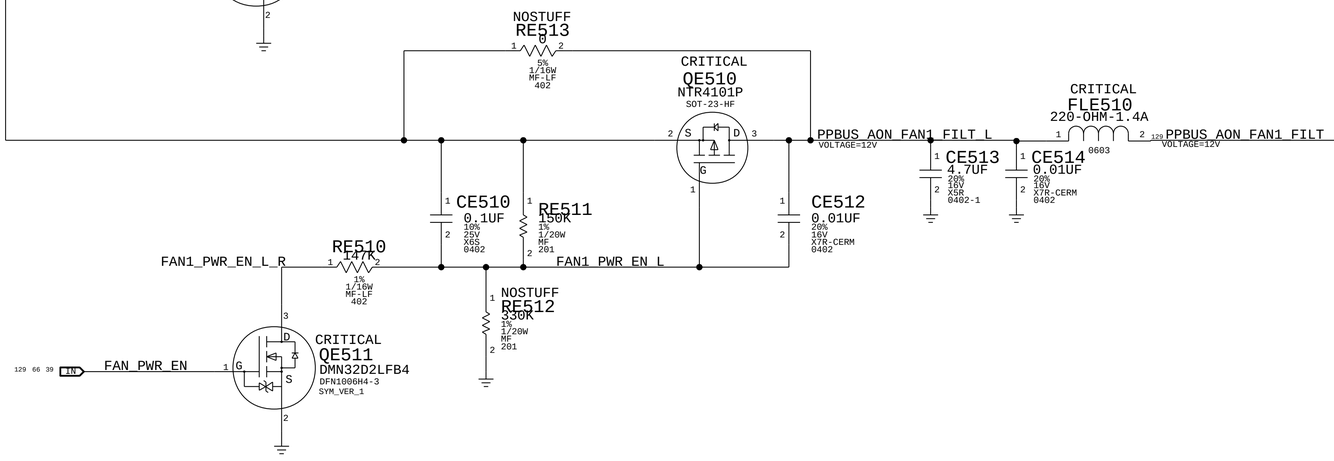
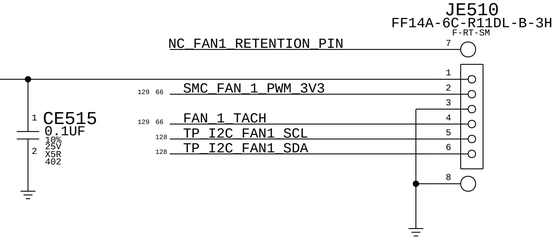
FAN0 (LEFT) CONNECTOR





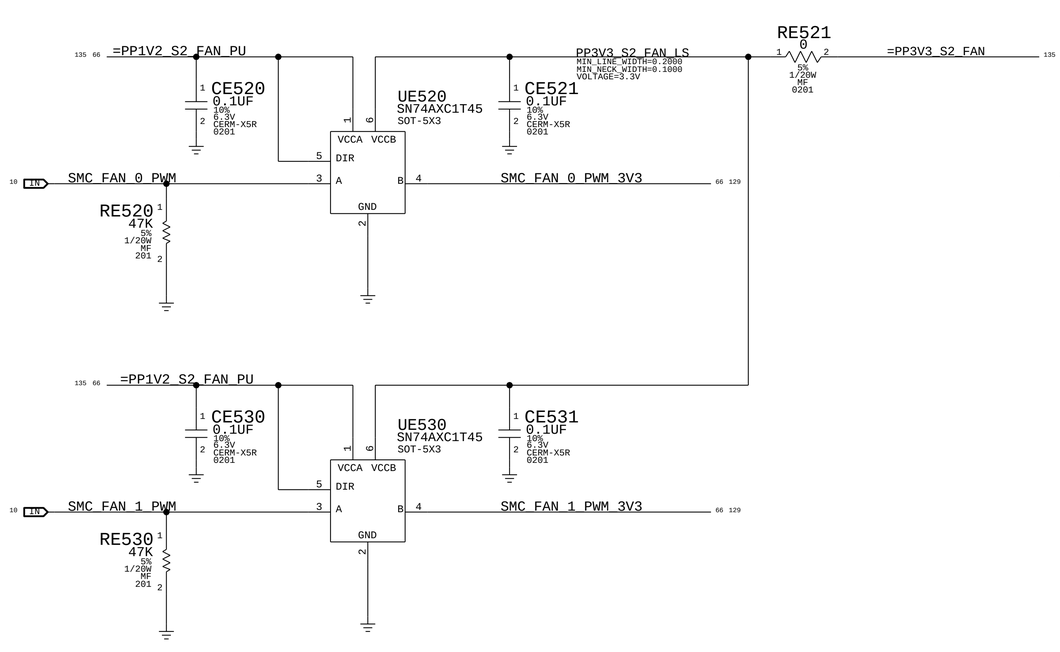
FAN1 (RIGHT) CONNECTOR

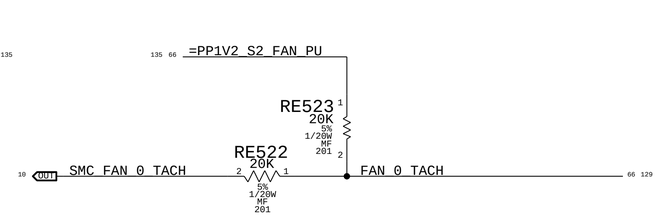


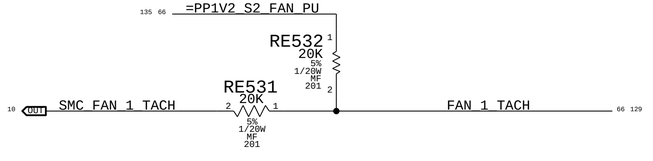


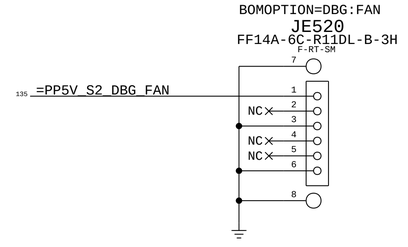
DUMMY COOLER CONNECTOR

IN PROGRESS









PAGE TITLE

FANS

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** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

USBC HIGH-SPEED AC COUPLING

GND_VOID=TRUE

IN	USBC_ATC0_R2D_C_P<1>	CF020	0.22UF	USBC_ATC0_R2D_P<1>	141
IN	USBC_ATC0_R2D_C_N<1>	CF021	0.22UF	USBC_ATC0_R2D_N<1>	141
IN	USBC_ATC0_R2D_C_P<2>	CF024	0.22UF	USBC_ATC0_R2D_P<2>	141
IN	USBC_ATC0_R2D_C_N<2>	CF025	0.22UF	USBC_ATC0_R2D_N<2>	141
BI	USBC_ATC0_D2R_P<1>	CF022	0.22UF	USBC_ATC0_D2R_C_P<1>	141
BI	USBC_ATC0_D2R_N<1>	CF023	0.22UF	USBC_ATC0_D2R_C_N<1>	141
BI	USBC_ATC0_D2R_P<2>	CF026	0.22UF	USBC_ATC0_D2R_C_P<2>	141
BI	USBC_ATC0_D2R_N<2>	CF027	0.22UF	USBC_ATC0_D2R_C_N<2>	141

All 0.22UF: 20% 6.3V 0201 X5R

BI	USBC_ATC0_AUX_P	CF028	0.1UF	USBC_ATC0_AUX_C_P
BI	USBC_ATC0_AUX_N	CF029	0.1UF	USBC_ATC0_AUX_C_N

CF028, CF029: 10% 6.3V 0201 CERM-X5R

RF028 33K 5% 1/20W MF 201
RF029 33K 5% 1/20W MF 201

IN	CIO_ATC0_LSTX_3V3		M7
OUT	CIO_ATC0_LSRX_3V3		L7

NOSTUFF
RF008 100K 5% 1/20W MF 201
RF009 100K 5% 1/20W MF 201

OUT	INT_I2C_ATCRTMR0_L	A10
BI	I2C_UPC0_ATCRTMR0_SCL	C9
BI	I2C_UPC0_ATCRTMR0_SDA	E7
	ATCRTMR0_GPIO_5	B9
	ATCRTMR0_GPIO_6	A8
	ATCRTMR0_FLASH_SHARE_EN	A4
IN	ATCRTMR0_FLASH_MSTR_H_SLV_L	A5
	ATCRTMR0_GPIO_12	A6
OUT	ATCRTMR0_THERM_D_P	M11
	ATCRTMR0_XTAL25M_IN	L9
	ATCRTMR0_XTAL25M_OUT	M9

338S00561
UF000
9999HH
BGA
SYM 1 OF 2

CRITICAL
OMIT_TABLE

=USBC_ATC0_R2D_P<1>	ASSRXP1	J1	GND_VOID=TRUE
=USBC_ATC0_R2D_N<1>	ASSRXN1	J2	GND_VOID=TRUE
=USBC_ATC0_R2D_P<2>	ASSRXP2	C1	GND_VOID=TRUE
=USBC_ATC0_R2D_N<2>	ASSRXN2	C2	GND_VOID=TRUE
=USBC_ATC0_D2R_C_P<1>	ASSTXP1	G1	GND_VOID=TRUE
=USBC_ATC0_D2R_C_N<1>	ASSTXN1	G2	GND_VOID=TRUE
=USBC_ATC0_D2R_C_P<2>	ASSTXP2	E1	GND_VOID=TRUE
=USBC_ATC0_D2R_C_N<2>	ASSTXN2	E2	GND_VOID=TRUE
USBC_ATC0_AUX_C_P	PA_AUX_P	L8	INTERNAL CAPS, PU, PD
USBC_ATC0_AUX_C_N	PA_AUX_N	M8	INTERNAL CAPS, PU, PD
	PA_LSTX_SBU1	M7	
	PA_LSRX_SBU2	L7	
	I2C_INT	A10	
	I2C_SCL	C9	
	I2C_SDA	E7	
	POC_GPIO_5	B9	
	POC_GPIO_6	A8	To SPI Flash
	POC_GPIO_10	A4	IPU ~ 65K
	POC_GPIO_11	A5	IPU ~ 65K
	POC_GPIO_12	A6	IPU ~ 65K
	THERMDA	M11	
	XTAL_25_IN	L9	
	XTAL_25_OUT	M9	
	MONDC_SVR	L12	
	MONDC	A11	
	TEST_EDM	M12	
NC	NC_A12	A12	
NC	NC_J6	J6	
NC	NC_L3	L3	
NC	NC_J5	J5	

BSSRXP1	J12	=USBC0_D2R_P<1>	BI
BSSRXN1	J11	=USBC0_D2R_N<1>	BI
BSSRXP2	C12	=USBC0_D2R_P<2>	BI
BSSRXN2	C11	=USBC0_D2R_N<2>	BI
BSSTXP1	G12	=USBC0_R2D_CR_P<1>	OUT
BSSTXN1	G11	=USBC0_R2D_CR_N<1>	OUT
BSSTXP2	E12	=USBC0_R2D_CR_P<2>	OUT
BSSTXN2	E11	=USBC0_R2D_CR_N<2>	OUT
BSBU1	M10	USBC0_AUXLSX_P	BI
BSBU2	L10	USBC0_AUXLSX_N	BI
PERST*	B8	ATCRTMR01_ACTIVE_READY_3V3	IN
RESET*	L11	ATCRTMR0_RESET_L	IN
TDI	A3	=JTAG_ATCRTMR0_TDI	IN
TMS	C3	=JTAG_ATCRTMR0_TMS	IN
TCK	B5	=JTAG_ATCRTMR0_TCK	IN
TDO	C5	=JTAG_ATCRTMR0_TDO	OUT
EE_DI	C6	SPI_ATCRTMR0_R_MOSI	OUT
EE_DO	B4	SPI_ATCRTMR0_R_MISO	IN
EE_CS*	B6	SPI_ATCRTMR0_R_CS_L	OUT
EE_CLK	C7	SPI_ATCRTMR0_R_CLK	OUT
TEST_EN	B11		
TEST_PWR_GOOD	B3	ATCRTMR0_TEST_PWR_GOOD	
RBIAS	L4	ATCRTMR0_RBIAS	
RSENSE	L5	ATCRTMR0_RSENSE	
ATEST_P	A1	NC	
ATEST_N	A2	NC	
FORCE_PWR	B10	ATCRTMR0_FORCE_PWR	IN
FLASH_BUSY*	A9	FLASH_BUSY_USBC01_L	BI
FUSE_VQPS_64	B2		
SMBUS_SCL	A7	TP_SMBUS_ATCRTMR0_SCL	
SMBUS_SDA	B7	TP_SMBUS_ATCRTMR0_SDA	

RF006 100 5% 1/20W MF 201
RF007 4.75K 0.5% 1/20W TF 0201
PLACE_NEAR=UF000.L5:2MM
PLACE_NEAR=UF000.L4:2MM

=PP3V3_ATCRTMR0_SX
=PP3V3_ATCRTMR0

RF050	100K		ATCRTMR0_GPIO_5
NOSTUFF RF041	100K		ATCRTMR0_GPIO_6
ATCRTMR01_ACTIVE_READY_3V3	0	RF040	
NOSTUFF RF051	100K		
NOSTUFF RF043	100K		ATCRTMR0_FLASH_SHARE_EN
NOSTUFF RF045	100K		ATCRTMR0_GPIO_12

All: 5% 1/20W MF 201

ATCRTMR0_XTAL25M_OUT_R — RF002 0 0201 5% MF 1/20W — ATCRTMR0_XTAL25M_OUT
CF002 20PF 5% 25V C0G 0201
CF003 20PF 5% 25V C0G 0201
CRITICAL
YF000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
ATCRTMR0_XTAL25M_IN_R — RF003 0 0201 5% MF 1/20W — ATCRTMR0_XTAL25M_IN

3.3V LDO

PACK_IGNORE=TRUE
PACK_OPTION=PKGS:SMALL_PITCH
AVOW_APPLE_PREFIX=U

UF015 TLV75533 X2SON
=PP3V8_ATC0_LDO
=USBC0_3V3LDO_EN
IN, EN, GND, THRM PAD, OUT
=PP3V3_S2_USB0_REG
RF012 100K 5% 1/20W MF 201
CF010 1.0UF 20% 6.3V X5R 0201-1
CF015 1.0UF 20% 6.3V X5R 0201-1

PACK_OPTION=PKGS:LARGER_PITCH
UF015 TLV75533 WSON
IN, EN, GND, EPAD, OUT, NC, NC

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

PP0V9_ATCRTMR0_SVR	CF065	20UF	CRITICAL
	CF064	20UF	CRITICAL
	CF063	20UF	CRITICAL
	CF062	20UF	CRITICAL
	CF061	4UF	CRITICAL
	CF060	4UF	CRITICAL
	CF050	4UF	CRITICAL
	CF051	4UF	CRITICAL
	CF052	4UF	CRITICAL
	CF053	4UF	CRITICAL

20% 2.5V X6S-CERM 0402 (20UF) / 20% 6.3V CER-X5R 0201 (4UF)

	VCC0P9_SVR_ANA	F6	
	VCC0P9_SVR_PB_ANA	G6	
		E9	
		G9	
	VCC0P9_LVR	L6	
	VCC0P9_LVR_SENSE	M6	
	VCC3P3_LC	E5	
	VCC3P3_ANA	L2	
	VCC0P9_LC	J3	
	VSS	F3	
		F5	
		G5	
	VSS_ANA	B1	
		B12	
		D1	
		D11	
		D12	
		D2	
		F1	
		F11	
		F12	
		F2	
	VCC3P3_SX	E6	
	VCC3P3A	J7	
	VCC3P3_SVR	M4	
		M5	
	VCC0P9_SVR	E3	
		G3	
	SVR_IND	L1	
		M1	
	SVR_VSS	M2	
		M3	
		F7	
		F9	
		G7	
		H1	
		H11	
		H12	
		H2	
	VSS_ANA	J9	
		K1	
		K11	
		K12	
		K2	

PP0V9_ATCRTMR0_LVR — VOLTAGE=0.9V
CF054 10UF 20% 6.3V CERM 0402
CF055 2.2UF 20% 6.3V X5R-CERM 0201

PP3V3_ATCRTMR0_ANA — VOLTAGE=3.3V
PP0V9_ATCRTMR0_LC — VOLTAGE=0.9V
PP3V3_ATCRTMR0_LC — VOLTAGE=3.3V
CF056 2.2UF 20% 6.3V X5R-CERM 0201
CF057 2.2UF 20% 6.3V X5R-CERM 0201
CF058 2.2UF 20% 6.3V X5R-CERM 0201

FROM USB-C PORT CONTROLLER (UPC)
=PP3V3_ATCRTMR0_SX
NOSTUFF CF042 47UF 20% 6.3V X5R-CERM 0603
CF036 2.2UF 20% 6.3V X5R-CERM 0201
CF037 2.2UF 20% 6.3V X5R-CERM 0201
RF000 0 5% 1/16W MF-LF 402
RF001 0 5% 1/16W MF-LF 402
XWF001 SM NO_XNET_CONNECTION=1

PP3V3_ATCRTMR0_VCCA — VOLTAGE=3.3V
CF043 12PF 5% 25V NP0-C0G 0201
CF030 2.2UF 20% 6.3V X5R-CERM 0201
CF031 10UF 20% 6.3V CERM 0402

PP3V3_ATCRTMR0_SVR — VOLTAGE=3.3V
CF032 10UF 20% 6.3V CERM 0402
CF033 10UF 20% 6.3V CERM 0402
CF034 10UF 20% 6.3V CERM 0402
CF035 10UF 20% 6.3V CERM 0402
BYPASS=UF000.M4:M3:3MM

P0V9_ATCRTMR0_SVR_PGND — VOLTAGE=0V
XWF000 SM
PLACE_NEAR=CF032.2:2MM
NO_XNET_CONNECTION=1

PP0V9_ATCRTMR0_SVR — VOLTAGE=0.9V
CF038 12PF 5% 25V NP0-C0G 0201
CF039 4UF 20% 6.3V CER-X5R 0201
CF041 4UF 20% 6.3V CER-X5R 0201
CF040 47UF 20% 6.3V CER-X5R 0603

CRITICAL
LF000 0.68UH-20%-4.3A-0.043OHM 0805
PP0V9_ATCRTMR0_SVR_IND — VOLTAGE=0.9V — DIDT=TRUE

XWF030 SM — ATCRTMR0_THERM_D_N
PLACE_NEAR=UF000.K11:2MM
NO_XNET_CONNECTION=1
CONNECT TO GND PIN CLOSEST TO THERMDA PIN

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC0

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** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
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USBC_ATC1_R2D_C_P<1>	CF120	0.22UF	20% X5R 6.3V 0201	USBC_ATC1_R2D_P<1>	
USBC_ATC1_R2D_C_N<1>	CF121	0.22UF	20% X5R 6.3V 0201	USBC_ATC1_R2D_N<1>	
USBC_ATC1_R2D_C_P<2>	CF124	0.22UF	20% X5R 6.3V 0201	USBC_ATC1_R2D_P<2>	
USBC_ATC1_R2D_C_N<2>	CF125	0.22UF	20% X5R 6.3V 0201	USBC_ATC1_R2D_N<2>	
USBC_ATC1_D2R_P<1>	CF122	0.22UF	20% X5R 6.3V 0201	USBC_ATC1_D2R_C_P<1>	
USBC_ATC1_D2R_N<1>	CF123	0.22UF	20% X5R 6.3V 0201	USBC_ATC1_D2R_C_N<1>	
USBC_ATC1_D2R_P<2>	CF126	0.22UF	20% X5R 6.3V 0201	USBC_ATC1_D2R_C_P<2>	
USBC_ATC1_D2R_N<2>	CF127	0.22UF	20% X5R 6.3V 0201	USBC_ATC1_D2R_C_N<2>	
USBC_ATC1_AUX_P	CF128	0.1UF	10% CERM-X5R 6.3V 0201	USBC_ATC1_AUX_C_P	
USBC_ATC1_AUX_N	CF129	0.1UF	10% CERM-X5R 6.3V 0201	USBC_ATC1_AUX_C_N	

RF128 33K 5% 1/20W MF 201
RF129 33K 5% 1/20W MF 201

CIO_ATC1_LSTX_3V3
CIO_ATC1_LSRX_3V3
NOSTUFF
RF108 100K 5% 1/20W MF 201
RF109 100K 5% 1/20W MF 201

UF100 9999HH BGA SYM 2 OF 2

338S00561

CRITICAL
OMIT_TABLE

=USBC_ATC1_R2D_P<1>	J1	ASSRXP1	J12	BSSRXP1	=USBC1_D2R_P<1>
=USBC_ATC1_R2D_N<1>	J2	ASSRXN1	J11	BSSRXN1	=USBC1_D2R_N<1>
=USBC_ATC1_R2D_P<2>	C1	ASSRXP2	C12	BSSRXP2	=USBC1_D2R_P<2>
=USBC_ATC1_R2D_N<2>	C2	ASSRXN2	C11	BSSRXN2	=USBC1_D2R_N<2>
=USBC_ATC1_D2R_C_P<1>	G1	ASSTXP1	G12	BSSTXP1	=USBC1_R2D_CR_P<1>
=USBC_ATC1_D2R_C_N<1>	G2	ASSTXN1	G11	BSSTXN1	=USBC1_R2D_CR_N<1>
=USBC_ATC1_D2R_C_P<2>	E1	ASSTXP2	E12	BSSTXP2	=USBC1_R2D_CR_P<2>
=USBC_ATC1_D2R_C_N<2>	E2	ASSTXN2	E11	BSSTXN2	=USBC1_R2D_CR_N<1>
USBC_ATC1_AUX_C_P	L8	PA_AUX_P	M10	BSBU1	USBC1_AUXLSX_P
USBC_ATC1_AUX_C_N	M8	PA_AUX_N	L10	BSBU2	USBC1_AUXLSX_N
	M7	PA_LSTX_SBU1	B8	PERST*	ATCRTMR01_ACTIVE_READY_3V3
	L7	PA_LSRX_SBU2	L11	RESET*	ATCRTMR1_RESET_L
INT_I2C_ATCRTMR1_L	A10	I2C_INT	A3	TDI	=JTAG_ATCRTMR1_TDI
I2C_UPC1_ATCRTMR1_SCL	C9	I2C_SCL	C3	TMS	=JTAG_ATCRTMR1_TMS
I2C_UPC1_ATCRTMR1_SDA	E7	I2C_SDA	B5	TCK	=JTAG_ATCRTMR1_TCK
			C5	TDO	=JTAG_ATCRTMR1_TDO
ATCRTMR1_GPIO_5	B9	POC_GPIO_5			
ATCRTMR1_GPIO_6	A8	POC_GPIO_6		To SPI Flash	
ATCRTMR1_FLASH_SHARE_EN	A4	POC_GPIO_10 IPU ~ 65K	C6	EE_DI	SPI_ATCRTMR1_R_MOSI
ATCRTMR1_FLASH_MSTR_H_SLV_L	A5	POC_GPIO_11 IPU ~ 65K	B4	EE_DO	SPI_ATCRTMR1_R_MISO
ATCRTMR1_GPIO_12	A6	POC_GPIO_12 IPU ~ 65K	B6	EE_CS*	SPI_ATCRTMR1_R_CS_L
			C7	EE_CLK	SPI_ATCRTMR1_R_CLK
ATCRTMR1_THERM_D_P	M11	THERMDA			
ATCRTMR1_XTAL25M_IN	L9	XTAL_25_IN			
ATCRTMR1_XTAL25M_OUT	M9	XTAL_25_OUT			
	L12	MONDC_SVR	B11	TEST_EN	
	A11	MONDC	B3	TEST_PWR_GOOD	ATCRTMR1_TEST_PWR_GOOD
	M12	TEST_EDM	L4	RBIAS	ATCRTMR1_RBIAS
	A12	NC_A12	L5	RSENSE	ATCRTMR1_RSENSE
	J6	NC_J6	A1	ATEST_P	NC
	L3	NC_L3	A2	ATEST_N	NC
	J5	NC_J5	B10	FORCE_PWR	ATCRTMR1_FORCE_PWR
			A9	FLASH_BUSY*	FLASH_BUSY_USBC01_L
			B2	FUSE_VQPS_64	
			A7	SMBUS_SCL	TP_SMBUS_ATCRTMR1_SCL
			B7	SMBUS_SDA	TP_SMBUS_ATCRTMR1_SDA

RF106 100 5% 1/20W MF 201
RF107 4.75K 0.5% 1/20W TF 0201
PLACE_NEAR=UF100.L5:3MM
PLACE_NEAR=UF100.L4:3MM

=PP3V3_ATCRTMR1_SX
=PP3V3_ATCRTMR1
ATCRTMR1_RSENSE

RF150 100K 5% 1/20W MF 201 — ATCRTMR1_GPIO_5
RF141 100K 5% 1/20W MF 201 — ATCRTMR1_GPIO_6
ATCRTMR01_ACTIVE_READY_3V3 — RF140 0 5% 1/20W MF 0201
RF151 100K 5% 1/20W MF 201
RF143 100K 5% 1/20W MF 201 — ATCRTMR1_FLASH_SHARE_EN
RF145 100K 5% 1/20W MF 201 — ATCRTMR1_GPIO_12

ATCRTMR1_XTAL25M_OUT_R — RF102 0 5% 1/20W — ATCRTMR1_XTAL25M_OUT
CF102 20PF 5% 25V C0G 0201
CF103 20PF 5% 25V C0G 0201
CRITICAL
YF100 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
ATCRTMR1_XTAL25M_IN_R — RF103 0 5% 1/20W — ATCRTMR1_XTAL25M_IN

UF100 9999HH BGA SYM 2 OF 2

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CRITICAL
OMIT_TABLE

PP0V9_ATCRTMR1_SVR		VCC0P9_SVR_ANA	F6	VCC3P3_SX	E6
		VCC0P9_SVR_PB_ANA	G6	VCC3P3A	J7
			E9		
			G9		
PP0V9_ATCRTMR1_LVR	L6	VCC0P9_LVR		VCC3P3_SVR	M4
VOLTAGE=0.9V	M6	VCC0P9_LVR_SENSE			M5
	E5	VCC3P3_LC		VCC0P9_SVR	E3
PP3V3_ATCRTMR1_ANA	L2	VCC3P3_ANA			G3
PP0V9_ATCRTMR1_LC	J3	VCC0P9_LC		SVR_IND	L1
VOLTAGE=0.9V					M1
	F3	VSS		SVR_VSS	M2
	F5				M3
	G5		F7	VSS_ANA	
	B1	VSS_ANA	F9		
	B12		G7		
	D1		H1		
	D11		H11		
	D12		H12		
	D2		H2		
	F1		J9		
	F11		K1		
	F12		K11		
	F2		K12		
			K2		

FROM USB-C PORT CONTROLLER (UPC)
=PP3V3_ATCRTMR1_SX
NOSTUFF CF142 47UF 20% 6.3V CER-X5R 0603
CF136 2.2UF 20% 6.3V X5R-CERM 0201
CF137 2.2UF 20% 6.3V X5R-CERM 0201
RF100 0 5% 1/16W MF-LF 402
RF101 0 5% 1/16W MF-LF 402
XWF101 SM NO_XNET_CONNECTION=1 — =PP3V3_ATCRTMR1

VOLTAGE=3.3V
PP3V3_ATCRTMR1_VCCA
CF143 12PF 5% 25V NP0-C0G 0201
CF130 2.2UF 20% 6.3V X5R-CERM 0201
CF131 10UF 20% 6.3V CERM 0402

VOLTAGE=3.3V
PP3V3_ATCRTMR1_SVR
CF132 10UF 20% 6.3V CERM 0402
CF133 10UF 20% 6.3V CERM 0402
CF134 10UF 20% 6.3V CERM 0402
CF135 10UF 20% 6.3V CERM 0402
BYPASS=UF100.M4:M3:3MM
XWF100 SM
P0V9_ATCRTMR1_SVR_PGND VOLTAGE=0V
PLACE_NEAR=CF132.2:2MM
NO_XNET_CONNECTION=1
PP0V9_ATCRTMR1_SVR VOLTAGE=0.9V

CF138 12PF 5% 25V NP0-C0G 0201
CF139 4UF 20% 6.3V CER-X5R 0201
CF141 4UF 20% 6.3V CER-X5R 0201
CF140 47UF 20% 6.3V CER-X5R 0603

CRITICAL
LF100 0.68UH-20%-4.3A-0.043OHM 0805
PP0V9_ATCRTMR1_SVR_IND VOLTAGE=0.9V DIDT=TRUE

CF154 10UF 20% 6.3V CERM 0402
CF155 2.2UF 20% 6.3V X5R-CERM 0201
CF156 2.2UF 20% 6.3V X5R-CERM 0201
CF157 2.2UF 20% 6.3V X5R-CERM 0201
CF158 2.2UF 20% 6.3V X5R-CERM 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

3.3V LDO

PACK_IGNORE=TRUE
PACK_OPTION=PKGS:SMALL_PITCH
AVOW_APPLE_PREFIX=U

UF115 TLV75533 X2SON
=PP3V8_ATC1_LDO
=USBC1_3V3LDO_EN
RF112 100K 5% 1/20W MF 201
CF110 1.0UF 20% 6.3V X5R 0201-1
CF115 1.0UF 20% 6.3V X5R 0201-1
=PP3V3_S2_USB1_REG

PACK_OPTION=PKGS:LARGER_PITCH
UF115 TLV75533 WSON
NC
NC

CONNECT TO GND PIN CLOSEST TO THERMDA PIN
XWF130 SM — ATCRTMR1_THERM_D_N

PLACE_NEAR=UF100.K11:2MM
NO_XNET_CONNECTION=1

BOM_COST_GROUP=TBT

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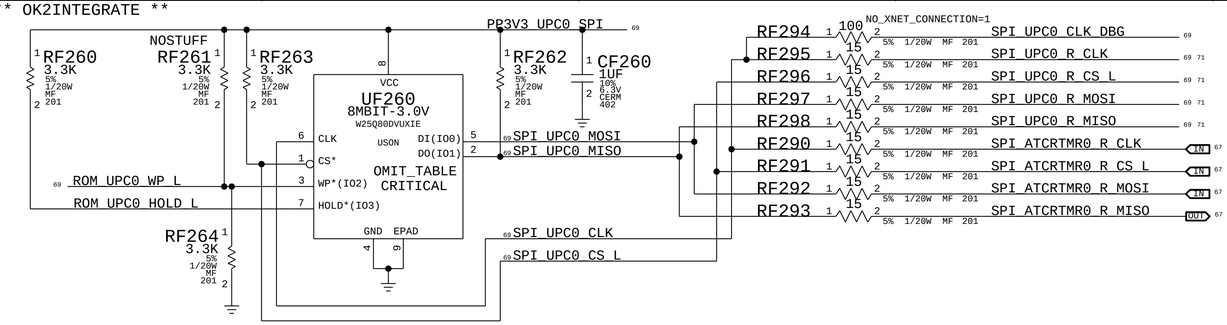
** OK2INTEGRATE **



Ace 0 is SPI Ace?

PACK_OPTION=USBC_SPI_UPC0

Ace 1 is SPI Ace?

PACK_IGNORE=TRUE
PACK_OPTION=USBC_SPI_UPC1

PP3V3_UPC1_SPI — MAKE_BASE=TRUE — PP3V3_UPC1_LDO
ROM_UPC1_WP_L — MAKE_BASE=TRUE — PD_UPC1_HPD

ROM_UPC0_WP_L — MAKE_BASE=TRUE — PD_UPC0_HPD
SWD_UPC_SWCLK1 — MAKE_BASE=TRUE — SWD_UPC0_CLK, SWD_UPC1_CLK
SWD_UPC_SWDIO0 — MAKE_BASE=TRUE — SWD_UPC0_DATA
SWD_UPC_SWDIO3 — MAKE_BASE=TRUE — SWD_UPC1_DATA
PP3V3_UPC0_SPI — MAKE_BASE=TRUE — PP3V3_UPC0_LDO

=PP3V3_ATCRTMR0_SX — (Internal pull-up) NOSTUFF 100K — RF244 ATCRTMR0_FLASH_MSTR_H_SLV_L — Master should be on SPI Ace2.
FLASH_BUSY_USBC01_L — MAKE_BASE=TRUE — PD_UPC0_GPIO1

Ace 1 is UART Ace?

PACK_OPTION=USBC_SPI_UPC0

=PP3V3_ATCRTMR1_SX — (Internal pull-up) NOSTUFF 100K — RF244 ATCRTMR1_FLASH_MSTR_H_SLV_L — Master should be on SPI Ace2.
ATCRTMR0_FLASH_MSTR — MAKE_BASE=TRUE — PD_UPC1_GPIO1

Ace 0 is UART Ace?

PACK_IGNORE=TRUE
PACK_OPTION=USBC_SPI_UPC1

SPI_UPC0_R_CLK
SPI_UPC0_R_CS_L
SPI_UPC0_R_MOSI
SPI_UPC0_R_MISO
SWD_UPC0_CLK
SWD_UPC0_DATA
MAKE_BASE=TRUE

SWD_UPC01_UART_CLK — MAKE_BASE=TRUE — SWD_UPC1_CLK
SWD_UPC01_UART_DATA — MAKE_BASE=TRUE — SWD_UPC1_DATA

ATCRTMR1_FLASH_SLV_L — MAKE_BASE=TRUE
RF247 2.2K — ATCRTMR1_FLASH_MSTR_H_SLV_L
RF272 100K — PD_UPC1_GPIO1
RF273 100K — PD_UPC1_HPD

RF247 2.2K — ATCRTMR0_FLASH_MSTR_H_SLV_L
RF272 100K — PD_UPC0_GPIO1
RF273 100K — PD_UPC0_HPD

=UART_UPC0_TX — UART_UPC0_TX — MAKE_BASE=TRUE — =UART_UPC0_RX
=UART_UPC1_TX — UART_UPC1_TX — MAKE_BASE=TRUE — =UART_UPC1_RX

ACE ARKANOID CONN

JF200 M-ST-SM — USBC_DBG 505070-1222

SMC		SOC
ATCRTMR0_RESET_L	1 2	=INT_I2C_UPC0_L
=I2C_SMC_UPC0_SCL	3 4	=I2C_UPC0_SDA
=I2C_SMC_UPC0_SDA	5 6	=I2C_UPC0_SCL
=INT_I2C_SMC_UPC0_L	7 8	UPC0_SER_DBG
SPI_UPC0_CLK_DBG	9 10	UPC1_SER_DBG
SPI_UPC1_CLK_DBG	11 12	SPI_UPC1_CS_L
	13 14	
	15 16	

BRIDGE ARKANOID CONN

JF201 M-ST-SM — USBC_DBG 505070-1222

ATCRTMR0_FORCE_PWR	1 2	INT_I2C_UPC0_ATCRTMR0_L
=PP3V3_ATCRTMR0	3 4	I2C_UPC0_ATCRTMR0_SCL
PP0V9_ATCRTMR0_LC	5 6	I2C_UPC0_ATCRTMR0_SDA
ATCRTMR01_ACTIVE_READY_3V3	7 8	ATCRTMR1_FORCE_PWR
=PP3V3_ATCRTMR1	9 10	INT_I2C_UPC1_ATCRTMR1_L
I2C_UPC1_ATCRTMR1_SDA	11 12	I2C_UPC1_ATCRTMR1_SCL
	13 14	
	15 16	

USBC_DBG RF280 200K

VREFB_ARDV01 — =PP3V3_S2_ACE01

=PP1V25_S2_ACE01 — CF281 0.1UF — CF280 0.1UF — RF282 5.1K — RF283 5.1K

PACK_IGNORE=TRUE
PACK_OPTION=PKGS:SMALL_PITCH

UF280 LSF0102 X2SON 311S00234
VREF_A VREF_B A1 A2 B1 B2 EN GND

=I2C_UPC0_SCL — I2C_UPC01_3V3_SCL
=I2C_UPC0_SDA — I2C_UPC01_3V3_SDA

PACK_OPTION=PKGS:LARGER_PITCH

UF280 LSF0102 VSSOP 311S00257

AARDVARKANOID CONN

JF202 M-ST-SM — USBC_DBG 505070-1222

SPI ACE		
=PP1V25_S2_ACE01	1 2	SPI_UPC0_CS_L
SWD_UPC_SWDIO0	3 4	SPI_UPC0_CLK
SWD_UPC_SWCLK1	5 6	SPI_UPC0_MOSI
SPI_UPC0_MISO	7 8	SWD_UPC01_UART_CLK
I2C_UPC01_3V3_SDA	9 10	SWD_UPC01_UART_DATA
I2C_UPC01_3V3_SCL	11 12	=PP1V25_S2_ACE01
	13 14	
	15 16	

UART ACE

BOM_COST_GROUP=USB-C

ATC0: I2C_ADDR=GND, I2C_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, I2C_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, I2C_*_CNFG=1M\u03a9 pull-downs
ATC3: I2C_ADDR=Float, I2C_*_CNFG=1M\u03a9 pull-downs

UPC0_I2C_ADDR — UPC1_I2C_ADDR — MAKE_BASE=TRUE — NC_UPC1_I2C_ADDR — NO_TEST=1

Configure to enable VDDIO and use it for SWD.
UPC0_VDDIO_CFG — UPC1_VDDIO_CFG — MAKE_BASE=TRUE

PP3V3_UPC0_SPI — RF242 10K — FLASH_BUSY_USBC01_L — MAKE_BASE=TRUE

INT_I2C_ATCRTMR0_L — UPC_ATCRTMR_INT RF210 0 — INT_I2C_UPC0_ATCRTMR0_L
INT_I2C_EUSBLS0_L — UPC_EUSBLS_INT RF211 0 — INT_I2C_UPC0_ATCRTMR0_L
INT_I2C_ATCRTMR1_L — UPC_ATCRTMR_INT RF215 0 — INT_I2C_UPC1_ATCRTMR1_L
INT_I2C_EUSBLS1_L — UPC_EUSBLS_INT RF216 0 — INT_I2C_UPC1_ATCRTMR1_L

Is UPCx_5V_EN being used?

UPC0_5V_EN — RF234 100K
UPC1_5V_EN — RF235 100K

PACK_IGNORE=TRUE
PACK_OPTION=USBC01_VR5V_LOCAL_NO

=PP3V3_S2_ACE01
RF220 10K — JTAG_ATCRTMR01_TCK — =JTAG_ATCRTMR0_TCK
RF221 10K — JTAG_ATCRTMR0_TMS — =JTAG_ATCRTMR0_TMS
RF222 10K — JTAG_ATCRTMR0_TDI — =JTAG_ATCRTMR0_TDI
RF223 100K — JTAG_ATCRTMR1_TMS — =JTAG_ATCRTMR0_TDO
RF224 100K — JTAG_ATCRTMR1_TDI — =JTAG_ATCRTMR1_TCK
JTAG_ATCRTMR01_TDO — =JTAG_ATCRTMR1_TMS
=JTAG_ATCRTMR1_TDI
=JTAG_ATCRTMR1_TDO

=PP1V25_S2_ACE01 — CF230 0.1UF — UF230 SN74AXC1T45 SOT-5X3 — CF231 0.1UF — =PP3V3_S2_ACE01
VCCA VCCB DIR A B GND
PMU_ACTIVE_READY — ATCRTMR01_ACTIVE_READY_3V3

HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

CRITICAL FF200 6A-32V — =PPHV_EXT01_AONSW — PPHV_INT0_AONSW — =PPHV_INT0_AONSW
PLACE_NEAR=UF400:5MM — MAKE_BASE=TRUE VOLTAGE=20V
RF200 0 — =PPHV_INT0_AONSW_OPT

CRITICAL FF201 6A-32V — PPHV_INT1_AONSW — =PPHV_INT1_AONSW
PLACE_NEAR=UF500:5MM — MAKE_BASE=TRUE VOLTAGE=20V
RF201 0 — =PPHV_INT1_AONSW_OPT

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DESKTOP

Desktops only need connection for programming OTP.

=PPVBUS_USBC0_OPT — MAKE_BASE=TRUE — PPVBUS_USBC0
=PPVBUS_USBC1_OPT — MAKE_BASE=TRUE — PPVBUS_USBC1

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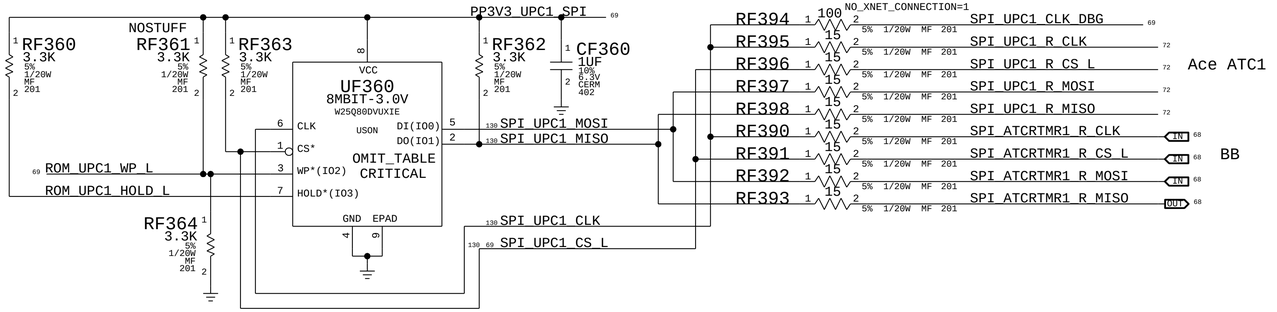
** OK2INTEGRATE **

Ace 0 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC0

ATC0 / UPC0 / RTMR0

UART_DEBUGPRT_R2D	IN	MAKE_BASE=TRUE	=	UPC0_DBG0	IN
UART_DEBUGPRT_D2R	OUT	MAKE_BASE=TRUE	=	UPC0_DBG1	IN
SWD_SOC_SWCLK	BI	MAKE_BASE=TRUE	=	UPC0_DBG2	OUT
SWD_SOC_SWDIO	BI	MAKE_BASE=TRUE	=	UPC0_DBG3	OUT
UART_SMC_DEBUGPRT_R2D	IN	MAKE_BASE=TRUE	=	UPC0_DBG4	OUT
UART_SMC_DEBUGPRT_D2R	OUT	MAKE_BASE=TRUE	=	UPC0_DBG5	IN
USB_DBG_LS_P	BI	MAKE_BASE=TRUE	=	USB2_UPC0_P2_P	BI
USB_DBG_LS_N	BI	MAKE_BASE=TRUE	=	USB2_UPC0_P2_N	BI
=PP1V8_S2_DBGUPC			=	=PP1V8_S2_UPC0	BI
=PP1V8_S2_DBGUSBLS			=	=PP1V8_S2_EUSBLS0	BI
SOC_DFU_STATUS	IN	MAKE_BASE=TRUE	=	UPC0_GPIO9	OUT
SOC_FORCE_DFU	OUT	MAKE_BASE=TRUE	=	UPC0_GPIO10	IN



Ace 1 is non-debug Port?

PACK_OPTION=USBC_DEBUG_UPC0

ATC1 / UPC1 / RTMR1

=PP1V8_S2_UPC01	PACK_OPTION=USBC_DEBUG_UPC0		=	=PP1V8_S2_UPC1	BI
=PP1V8_S2_USBLS01	PACK_OPTION=USBC_DEBUG_UPC0		=	=PP1V8_S2_EUSBLS1	BI
RF320 1/20W 5% MF 201 100K	PD_UPC1_DBG0_R	MAKE_BASE=TRUE	=	UPC1_DBG0	BI
RF321 1/20W 5% MF 201 100K	PD_UPC1_DBG1_R	MAKE_BASE=TRUE	=	UPC1_DBG1	BI
RF322 1/20W 5% MF 201 100K	PD_UPC1_DBG2_R	MAKE_BASE=TRUE	=	UPC1_DBG2	BI
RF323 1/20W 5% MF 201 100K	PD_UPC1_DBG3_R	MAKE_BASE=TRUE	=	UPC1_DBG3	BI
RF324 1/20W 5% MF 201 100K	PD_UPC1_DBG4_R	MAKE_BASE=TRUE	=	UPC1_DBG4	BI
RF325 1/20W 5% MF 201 100K	PD_UPC1_DBG5_R	MAKE_BASE=TRUE	=	UPC1_DBG5	BI
RF328 1/20W 5% MF 201 100K	PD_UPC1_USBP2_RP	MAKE_BASE=TRUE	=	USB2_UPC1_P2_P	BI
RF329 1/20W 5% MF 201 100K	PD_UPC1_USBP2_RN	MAKE_BASE=TRUE	=	USB2_UPC1_P2_N	BI

Ace2 GPIOs

RF373 1/20W 5% MF 201 100K	PD_UPC1_GPIO7	MAKE_BASE=TRUE	=	UPC1_GPIO7	OUT
RF374 1/20W 5% MF 201 100K	PD_UPC1_GPIO9	MAKE_BASE=TRUE	=	UPC1_GPIO9	OUT
RF375 1/20W 5% MF 201 100K	PD_UPC1_GPIO10	MAKE_BASE=TRUE	=	UPC1_GPIO10	OUT

CKPLUS_WAIVE=SINGLE_NODENET
on all nets above.

RF300 1/20W 5% MF 201 100K	PD_UPC0_FORCE_PWR				71
RF301 1/20W 5% MF 201 100K	PD_UPC1_FORCE_PWR				72

Unused ports

RF316 1/20W 5% MF 201 100K	PD_UPC0_DBG6_R	MAKE_BASE=TRUE	=	UPC0_DBG6	BI
RF317 1/20W 5% MF 201 100K	PD_UPC0_DBG7_R	MAKE_BASE=TRUE	=	UPC0_DBG7	BI
RF31A 1/20W 5% MF 201 100K	PD_UPC0_USBP3_RP	MAKE_BASE=TRUE	=	USB2_UPC0_P3_P	BI
RF31B 1/20W 5% MF 201 100K	PD_UPC0_USBP3_RN	MAKE_BASE=TRUE	=	USB2_UPC0_P3_N	BI
RF326 1/20W 5% MF 201 100K	PD_UPC1_DBG6_R	MAKE_BASE=TRUE	=	UPC1_DBG6	BI
RF327 1/20W 5% MF 201 100K	PD_UPC1_DBG7_R	MAKE_BASE=TRUE	=	UPC1_DBG7	BI
RF32A 1/20W 5% MF 201 100K	PD_UPC1_USBP3_RP	MAKE_BASE=TRUE	=	USB2_UPC1_P3_P	BI
RF32B 1/20W 5% MF 201 100K	PD_UPC1_USBP3_RN	MAKE_BASE=TRUE	=	USB2_UPC1_P3_N	BI

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP

UPC0_BUSPOWER	OUT	PACK_OPTION=BUSPOWER_2_LDO MAKE_BASE=TRUE		PP3V3_UPC0_LDO	IN
USBC0_RPD_G1	BI	MAKE_BASE=TRUE	=	USBC0_CC1	BI
USBC0_RPD_G2	BI	MAKE_BASE=TRUE	=	USBC0_CC2	BI
UPC1_BUSPOWER	OUT	PACK_OPTION=BUSPOWER_2_LDO MAKE_BASE=TRUE		PP3V3_UPC1_LDO	IN
USBC1_RPD_G1	BI	MAKE_BASE=TRUE	=	USBC1_CC1	BI
USBC1_RPD_G2	BI	MAKE_BASE=TRUE	=	USBC1_CC2	BI

BOM_COST_GROUP=USB-C

SYNC_MASTER=T724_RUENJOU_MLB_S_0.55.1 SYNC_DATE=03/26/2020

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** OK2INTEGRATE **

PP3V3_UPC0_LDO 69 70 71 76 129

Internal Pull-ups
Enabled after reading straps

RF409 1M 5% 1/20W MF 201 — I2C_UPC0_ATCRTMR0_SCL — CKPLUS_WAIVE=I2C_PULLUP — 67 69 71 74 129 130

RF408 1M 5% 1/20W MF 201 — I2C_UPC0_ATCRTMR0_SDA — CKPLUS_WAIVE=I2C_PULLUP — 67 69 71 74 129 130

RF407 10K 5% 1/20W MF 201 — INT_I2C_UPC0_ATCRTMR0_L — 69 71

RF405 1M 5% 1/20W MF 201 — =UART_UPC0_RX — 69 71

RF406 100K 5% 1/20W MF 201 — PD_UPC0_MRESET — 71

RF402 100K 5% 1/20W MF 201 — PD_UPC0_GPIO5 — 71 85

NOSTUFF

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

PP3V3_UPC0_LDO 69 70 71 76 129

NOSTUFF

RF410 0 5% 1/20W MF 0201

RF411 0 5% 1/20W MF 0201 — UPC0_BUSPOWER — 70 71

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

CRITICAL
RF403 15K 0.1% 1/20W TF-LF 0201

GND_I2C_ADDR
PRIMARY ONLY

69 =PPHV_INT0_AONSW

MAX 100uF TOTAL ON RAIL

136 72 =PP5V_S2_ACE01_VCONN

136 72 =PP5V_S2_ACE01

CAP FOR PP_5V0 ON VR PAGE

PP_5V0: K9 L10 M9 K10 K11 L12 M11 N12 M14 M13
PP_CABLE: G2
PP_HV: G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 N2 N4
VBUS: G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8

UF400
CD3217B12BCE
FCBGA

353S02158
CRITICAL
OMIT_TABLE

		B13	HRESET	
71	PD_UPC0_MRESET	A14	MRESET	
129 74 69 67	ATCRTMR0_RESET_L	B17	RESET*	
69	UPC0_SER_DBG	A2	GPIO0	
		B1		
69	PD_UPC0_GPIO1	D1	GPIO1	
71 69	INT_I2C_UPC0_ATCRTMR0_L	F1	GPIO2	
75 69	UPC0_5V_EN	C2	GPIO3	
69 67	ATCRTMR0_FORCE_PWR	E2	GPIO4	
85 71	PD_UPC0_GPIO5	B3	GPIO5	
70	PD_UPC0_FORCE_PWR	C4	GPIO6	DIGITAL CORE I/O & CONTROL
134	UPC0_GPIO7	D3	GPIO7	
134 132 130 80 72 44	UPC_PMU_RESET_3V3	E4	GPIO8	
70	UPC0_GPIO9	F3	GPIO9	
70	UPC0_GPIO10	F7	GPIO10	
71 70	UPC0_BUSPOWER	A18	BUSPOWER	
69	UPC0_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
	UPC0_R_OSC	M21	R_OSC	
130 129 74 71 69 67 BI	I2C_UPC0_ATCRTMR0_SDA	A16	I2CM_SDA_CNFG	
130 129 74 71 69 67 BI	I2C_UPC0_ATCRTMR0_SCL	B15	I2CM_SCL_CNFG	
69 55 BI	=I2C_UPC0_SDA	B5	I2C_SDA1	
69 55 BI	=I2C_UPC0_SCL	A4	I2C_SCL1	
69 55 OUT	=INT_I2C_UPC0_L	D7	I2C_IRQ1*	
69 56 BI	=I2C_SMC_UPC0_SDA	B7	I2C_SDA2	
69 56 BI	=I2C_SMC_UPC0_SCL	A6	I2C_SCL2	
69 56 OUT	=INT_I2C_SMC_UPC0_L	C8	I2C_IRQ2*	
69 OUT	SPI_UPC0_R_CLK	B9	SPI_CLK	
69 OUT	SPI_UPC0_R_MOSI	B11	SPI_MOSI	
69 IN	SPI_UPC0_R_MISO	A10	SPI_MISO	
69 OUT	SPI_UPC0_R_CS_L	A8	SPI_SSZ	
69 BI	SWD_UPC0_DATA	E20	SWD_DATA	IPU
69 BI	SWD_UPC0_CLK	E16	SWD_CLK	IPU
71 69 IN	=UART_UPC0_RX	B19	UART_RX	
69 OUT	=UART_UPC0_TX	A20	UART_TX	
85 BI	USB2_UPC0_P1_P	H19	USB_RP1_P	
85 BI	USB2_UPC0_P1_N	H21	USB_RP1_N	
70 BI	USB2_UPC0_P2_P	G20	USB_RP2_P	PORT_MUX
70 BI	USB2_UPC0_P2_N	G22	USB_RP2_N	
70 BI	USB2_UPC0_P3_P	F19	USB_RP3_P	
70 BI	USB2_UPC0_P3_N	F21	USB_RP3_N	
67 BI	USBC0_AUXLSX_P	J12	AUX_P	
67 BI	USBC0_AUXLSX_N	H11	AUX_N	
69 OUT	PD_UPC0_HPD	C12	HPD	
134 70 BI	UPC0_DBG0	G12	DEBUG0	
134 70 BI	UPC0_DBG1	F11	DEBUG1	
134 70 BI	UPC0_DBG2	E8	DEBUG2	
134 70 BI	UPC0_DBG3	E12	DEBUG3	
134 70 OUT	UPC0_DBG4	G16	DEBUG4	
134 70 BI	UPC0_DBG5	F15	DEBUG5	
70 IN	UPC0_DBG6	D15	DEBUG6	
70 OUT	UPC0_DBG7	D19	DEBUG7	

VIN_3V3	C20	PPVBUS_USBC0 69 73 129 130	CF401 1UF 10% 25V X5R 0402
VDDIO	A12	=PP3V3_S2_ACE01 69 72 135	CF400 10UF 20% 6.3V CERM 0402
VDDIO_CFG	D11	UPC0_VDDIO_CFG 69	
LDO_3V3	C22	=PP1V25_S2_ACE01 69 72 130 135	CF402 1.0UF 20% 6.3V X5R 0201-1
	D21		
VIN_LV	L20	PP3V3_UPC0_LDO 69 70 71 76 129	CF408 10UF 20% 6.3V CERM 0402
VOUT_LV	L18	=PP1V8_S2_UPC0 70 74	CF403 0.1UF 10% 6.3V CERM-X5R 0201
		USBC0_3V3LDO_EN 130 134 (cap needed when used as power source)	
VRET	C16		
SS	L22	UPC0_SS	
LDO_CORE	E22	PP1V5_UPC0_LDO_CORE	CF409 0.68UF 20% 6.3V X6S 0402
VBUS_OPT	D5	=PPVBUS_USBC0_OPT 69	CF405 10UF 20% 6.3V CERM 0402
PP_HV_OPT	F5	=PPHV_INT0_AONSW_OPT 69	
C_CC1	M15 N16	USBC0_CC1	CF414 220PF 5% 50V C0G 0201-1
C_CC2	M17 N18	USBC0_CC2	CF413 220PF 5% 50V C0G 0201-1
RPD_G1	L14	USBC0_RPD_G1 BI 70	
RPD_G2	L16	USBC0_RPD_G2 BI 70	
C_USB_TP	K19	USBC0_USB_TOP_P BI 73 129	
C_USB_TN	K21	USBC0_USB_TOP_N BI 73 129	
C_USB_BP	J20	USBC0_USB_BOT_P BI 73	
C_USB_BN	J22	USBC0_USB_BOT_N BI 73	
C_SBU1	J16	USBC0_SBU1 BI 73 129	
C_SBU2	H15	USBC0_SBU2 BI 73 129	

MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.1000

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

POWER

TYPE-C

GND_OPT	C18	
GND_OPT	E18	
GND_OPT	D17	
GND_OPT	G18	

GND

GND: A22 H9 N20 B21 K15 N22

BOM_COST_GROUP=USB-C

SYNC_MASTER=T724_RUENJOU_MLB_S_0.55.1 SYNC_DATE=03/26/2020

PAGE TITLE
USB-C: Port Controller ATC0

Apple Inc.

DRAWING NUMBER 051-05641
SIZE D
REVISION 6.33.0
BRANCH
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SHEET 71 OF 155

** OK2INTEGRATE **

PP3V3_UPC1_LDO 69 70 72 76

1 1M 2 RF509 5% 1/20W MF 201 I2C_UPC1_ATCRTMR1_SCL CKPLUS_WAIVE=I2C_PULLUP 68 69 72 74 129

1 1M 2 RF508 5% 1/20W MF 201 I2C_UPC1_ATCRTMR1_SDA CKPLUS_WAIVE=I2C_PULLUP 68 69 72 74 129

1 10K 2 RF507 5% 1/20W MF 201 INT_I2C_UPC1_ATCRTMR1_L 69 72

1 1M 2 RF505 5% 1/20W MF 201 =UART_UPC1_RX 69 72

1 100K 2 RF506 5% 1/20W MF 201 PD_UPC1_MRESET 72

1 100K 2 RF502 5% 1/20W MF 201 PD_UPC1_GPIO5 72 85

NOSTUFF

Either a Testpoint or Arkanoid connector must be present for GPIO0 (EVEN IN PRODUCTION)

PP3V3_UPC1_LDO 69 70 72 76

NOSTUFF

1 0 2 RF510 5% 1/20W MF 0201

1 0 2 RF511 5% 1/20W MF 0201 UPC1_BUSPOWER 70 72

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

CRITICAL
RF503 1 15K 0.1% 1/20W TF 0201 2

GND_I2C_ADDR PRIMARY ONLY

69 =PPHV_INT1_AONSW

MAX 100uF TOTAL ON RAIL

136 71 =PP5V_S2_ACE01_VCONN

136 71 =PP5V_S2_ACE01

CAP FOR PP_5V0 ON VR PAGE

K9 L10 M9 N10 K11 L12 M11 N12 — PP_5V0
N14 M13 — PP_CABLE
G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 N2 N4 — PP_HV
G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8 — VBUS

UF500
CD3217B12BCE
FCBGA

353S02158
CRITICAL
OMIT_TABLE

		B13	HRESET	
72	PD_UPC1_MRESET	A14	MRESET	
129 74 68	OUT ATCRTMR1_RESET_L	B17	RESET*	
69	OUT UPC1_SER_DBG	A2		
		B1	GPIO0	
69	OUT PD_UPC1_GPIO1	D1	GPIO1	
	OUT INT_I2C_UPC1_ATCRTMR1_L	F1	GPIO2	
72 69	IN UPC1_5V_EN	C2	GPIO3	
75 69	OUT ATCRTMR1_FORCE_PWR	E2	GPIO4	
69 68	OUT PD_UPC1_GPIO5	B3	GPIO5	
85 72	PD_UPC1_FORCE_PWR	C4	GPIO6	DIGITAL CORE I/O & CONTROL
70	OUT UPC1_GPIO7	D3	GPIO7	
70	OUT UPC_PMU_RESET_3V3	E4	GPIO8	
134 132 130 80 71 44	IN UPC1_GPIO9	F3	GPIO9	
70	OUT UPC1_GPIO10	F7	GPIO10	
72 70	UPC1_BUSPOWER	A18	BUSPOWER	
69	UPC1_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
	UPC1_R_OSC	M21	R_OSC	
129 74 72 69 68	BI I2C_UPC1_ATCRTMR1_SDA	A16	I2CM_SDA_CNFG	
129 74 72 69 68	BI I2C_UPC1_ATCRTMR1_SCL	B15	I2CM_SCL_CNFG	
55	BI =I2C_UPC1_SDA	B5	I2C_SDA1	
55	BI =I2C_UPC1_SCL	A4	I2C_SCL1	
55	OUT =INT_I2C_UPC1_L	D7	I2C_IRQ1*	
56	BI =I2C_SMC_UPC1_SDA	B7	I2C_SDA2	
56	BI =I2C_SMC_UPC1_SCL	A6	I2C_SCL2	
56	OUT =INT_I2C_SMC_UPC1_L	C8	I2C_IRQ2*	
70	OUT SPI_UPC1_R_CLK	B9	SPI_CLK	
70	OUT SPI_UPC1_R_MOSI	B11	SPI_MOSI	
70	IN SPI_UPC1_R_MISO	A10	SPI_MISO	
70	OUT SPI_UPC1_R_CS_L	A8	SPI_SSZ	
69	BI SWD_UPC1_DATA	E20	SWD_DATA	IPU
69	BI SWD_UPC1_CLK	E16	SWD_CLK	IPU
72 69	IN =UART_UPC1_RX	B19	UART_RX	
69	OUT =UART_UPC1_TX	A20	UART_TX	
85	BI USB2_UPC1_P1_P	H19	USB_RP1_P	
85	BI USB2_UPC1_P1_N	H21	USB_RP1_N	
70	BI USB2_UPC1_P2_P	G20	USB_RP2_P	
70	BI USB2_UPC1_P2_N	G22	USB_RP2_N	PORT_MUX
70	BI USB2_UPC1_P3_P	F19	USB_RP3_P	
70	BI USB2_UPC1_P3_N	F21	USB_RP3_N	
68	BI USBC1_AUXLSX_P	J12	AUX_P	
68	BI USBC1_AUXLSX_N	H11	AUX_N	
69	OUT PD_UPC1_HPD	C12	HPD	
70	BI UPC1_DBG0	G12	DEBUG0	
70	BI UPC1_DBG1	F11	DEBUG1	
70	BI UPC1_DBG2	E8	DEBUG2	
70	BI UPC1_DBG3	E12	DEBUG3	
70	OUT UPC1_DBG4	G16	DEBUG4	
70	BI UPC1_DBG5	F15	DEBUG5	
70	IN UPC1_DBG6	D15	DEBUG6	
70	OUT UPC1_DBG7	D19	DEBUG7	

POWER

TYPE-C

GND

GND
A22 H9 N20 B21 K15 N22

PPVBUS_USBC1 69 73 129 130

CF501 1 1UF 10% 35V X5R 0402 2

=PP3V3_S2_ACE01 69 71 135

CF500 1 10UF 20% 6.3V CERM 0402 2

=PP1V25_S2_ACE01 69 71 130 135

CF502 1 1.0UF 20% 6.3V X5R 0201-1 2

MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
PP3V3_UPC1_LDO 69 70 72 76

CF508 1 10UF 20% 6.3V CERM 0402 2

=PP1V8_S2_UPC1 70 74

CF503 1 0.1UF 10% 6.3V CERM-X5R 0201 2

USBC1_3V3LDO_EN 130 141
(cap needed when used as power source)

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	UPC1_VDDIO_CFG	69
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18		
VRET	C16		
SS	L22	UPC1_SS	
LDO_CORE	E22	PP1V5_UPC1_LDO_CORE	
VBUS_OPT	D5	=PPVBUS_USBC1_OPT	69
PP_HV_OPT	F5	=PPHV_INT1_AONSW_OPT	69
C_CC1	M15	USBC1_CC1	
	N16		
C_CC2	M17	USBC1_CC2	
	N18		
RPD_G1	L14	USBC1_RPD_G1	BI 70
RPD_G2	L16	USBC1_RPD_G2	BI 70
C_USB_TP	K19	USBC1_USB_TOP_P	BI 73
C_USB_TN	K21	USBC1_USB_TOP_N	BI 73
C_USB_BP	J20	USBC1_USB_BOT_P	BI 73
C_USB_BN	J22	USBC1_USB_BOT_N	BI 73
C_SBU1	J16	USBC1_SBU1	BI 73 129
C_SBU2	H15	USBC1_SBU2	BI 73 129

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.1000
CF505 1 10UF 20% 6.3V CERM 0402 2

CF509 1 0.68UF 5% 6.3V X6S 0402 2

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
70 76 129

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
70 76 129

CF514 1 220PF 5% 50V C0G 0201-1 2

CF513 1 220PF 5% 50V C0G 0201-1 2

GND_OPT	C18	
GND_OPT	E18	
GND_OPT	D17	
GND_OPT	G18	

BOM_COST_GROUP=USB-C

SYNC_MASTER=T724_RUENJOU_MLB_S_0.55.1 SYNC_DATE=03/26/2020

PAGE TITLE
USB-C: Port Controller ATC1

Apple Inc.

DRAWING NUMBER 051-05641 SIZE D
REVISION 6.33.0
BRANCH
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Left Side Port

PPVBUS_USBC0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

PLACE_NEAR=JF600.30:5MM
ALLOW_APPLE_PREFIX=D

DF622
TVS2200
WSON
4 IN
5 IN
6 IN
GND 1
GND 2
GND 3
EPAD 7

CRITICAL
DZF620
X3-WLB1608-1
SDM2U40CSP

516S00686
PACK_OPTION=POR
JF600
20875-028E-01
F-ST-SMM

PLACE VBUS CAP NEAR EACH VBUS PIN

CRITICAL CF620 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF621 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF622 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF623 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF626 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF627 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF628 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF625 0.01UF 10% 25V X5R-CERM 0201

USBC0_D2R_CR_N<1>
USBC0_D2R_CR_P<1>
USBC0_R2D_N<1>
USBC0_R2D_P<1>
USBC0_USB_TOP_P
USBC0_USB_TOP_N
USBC0_D2R_CR_N<2>
USBC0_D2R_CR_P<2>
TP_USBC0_PP20V
USBC0_SBU2
USBC0_CC1_CONN
USBC0_USB_BOT_N
USBC0_USB_BOT_P
USBC0_SBU1
USBC0_CC2_CONN
USBC0_R2D_N<2>
USBC0_R2D_P<2>

USBC0_CC1_CONN
USBC0_R2D_CR_N<1>
USBC0_R2D_CR_P<1>
USBC0_D2R_N<1>
USBC0_D2R_P<1>
USBC0_SBU2
USBC0_USB_BOT_N
USBC0_USB_BOT_P

RF661 5% 1/20W MF 201 USBC0_R2D_C_N<1>
RF660 5% 1/20W MF 201 USBC0_R2D_C_P<1>
RF663 5% 1/20W MF 201 USBC0_D2R_R_N<1>
RF662 5% 1/20W MF 201 USBC0_D2R_R_P<1>
GND_VOID=TRUE

CF661 X5R 10% 0.22UF 25V 0201 USBC0_R2D_N<1>
CF660 X5R 10% 0.22UF 25V 0201 USBC0_R2D_P<1>
CF663 CER-X5R 10% 0.33UF 25V 0201 USBC0_D2R_CR_N<1>
CF662 CER-X5R 10% 0.33UF 25V 0201 USBC0_D2R_CR_P<1>
GND_VOID=TRUE

DZF662 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF663 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF660 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF661 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF664 CRITICAL 5.5V-0.28PF 0201-1TH1CKSTNCL
DZF665 CRITICAL 5.5V-0.28PF 0201-1TH1CKSTNCL
DZF667 CRITICAL ESDL20-1BF4 0201-1TH1CKSTNCL
DZF666 CRITICAL ESDL20-1BF4 0201-1TH1CKSTNCL

RF665 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF664 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF667 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF666 220K 5% 1/20W MF 201 GND_VOID=TRUE

USBC1_USB_BOT_N
USBC1_USB_BOT_P
USBC1_SBU1
USBC1_R2D_CR_P<2>
USBC1_R2D_CR_N<2>
USBC1_D2R_P<2>
USBC1_D2R_N<2>
USBC1_CC2_CONN

RF680 5% 1/20W MF 201 USBC1_R2D_C_P<2>
RF681 5% 1/20W MF 201 USBC1_R2D_C_N<2>
RF682 5% 1/20W MF 201 USBC1_D2R_R_P<2>
RF683 5% 1/20W MF 201 USBC1_D2R_R_N<2>
GND_VOID=TRUE

CF680 X5R 10% 0.22UF 25V 0201 USBC1_R2D_P<2>
CF681 X5R 10% 0.22UF 25V 0201 USBC1_R2D_N<2>
CF682 CER-X5R 10% 0.33UF 25V 0201 USBC1_D2R_CR_P<2>
CF683 CER-X5R 10% 0.33UF 25V 0201 USBC1_D2R_CR_N<2>
GND_VOID=TRUE

DZF682 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF683 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF680 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF681 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF686 CRITICAL ESDL20-1BF4 0201-1TH1CKSTNCL
DZF687 CRITICAL ESDL20-1BF4 0201-1TH1CKSTNCL
DZF684 CRITICAL 5.5V-0.28PF 0201-1TH1CKSTNCL
DZF685 CRITICAL 5.5V-0.28PF 0201-1TH1CKSTNCL

RF684 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF685 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF686 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF687 220K 5% 1/20W MF 201 GND_VOID=TRUE

USBC0_CC2_CONN
USBC0_R2D_N<2>
USBC0_R2D_P<2>
USBC0_R2D_CR_N<2>
USBC0_R2D_CR_P<2>
USBC0_USB_TOP_P
USBC0_USB_TOP_N
USBC0_D2R_N<2>
USBC0_D2R_P<2>
USBC0_SBU1

RF691 5% 1/20W MF 201 USBC0_R2D_CR_N<2>
RF690 5% 1/20W MF 201 USBC0_R2D_CR_P<2>
RF693 5% 1/20W MF 201 USBC0_D2R_N<2>
RF692 5% 1/20W MF 201 USBC0_D2R_P<2>
GND_VOID=TRUE

CF691 X5R 10% 0.22UF 25V 0201 USBC0_R2D_C_N<2>
CF690 X5R 10% 0.22UF 25V 0201 USBC0_R2D_C_P<2>
CF693 CER-X5R 10% 0.33UF 25V 0201 USBC0_D2R_R_N<2>
CF692 CER-X5R 10% 0.33UF 25V 0201 USBC0_D2R_R_P<2>
GND_VOID=TRUE

DZF690 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF691 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF694 CRITICAL 5.5V-0.28PF 0201-1TH1CKSTNCL
DZF695 CRITICAL 5.5V-0.28PF 0201-1TH1CKSTNCL
DZF696 CRITICAL ESDL20-1BF4 0201-1TH1CKSTNCL
DZF697 CRITICAL ESDL20-1BF4 0201-1TH1CKSTNCL

RF696 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF697 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF694 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF695 220K 5% 1/20W MF 201 GND_VOID=TRUE

USBC1_SBU2
USBC1_R2D_P<1>
USBC1_R2D_N<1>
USBC1_R2D_CR_P<1>
USBC1_R2D_CR_N<1>
USBC1_USB_TOP_P
USBC1_USB_TOP_N
USBC1_D2R_CR_P<1>
USBC1_D2R_CR_N<1>
USBC1_CC1_CONN

RF670 5% 1/20W MF 201 USBC1_R2D_CR_P<1>
RF671 5% 1/20W MF 201 USBC1_R2D_CR_N<1>
RF672 5% 1/20W MF 201 USBC1_D2R_P<1>
RF673 5% 1/20W MF 201 USBC1_D2R_N<1>
GND_VOID=TRUE

CF670 X5R 10% 0.22UF 25V 0201 USBC1_R2D_C_P<1>
CF671 X5R 10% 0.22UF 25V 0201 USBC1_R2D_C_N<1>
CF672 CER-X5R 10% 0.33UF 25V 0201 USBC1_D2R_R_P<1>
CF673 CER-X5R 10% 0.33UF 25V 0201 USBC1_D2R_R_N<1>
GND_VOID=TRUE

DZF670 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF671 CRITICAL SESDL2012 X4DFN2-3Y1CKSTNCL
DZF674 CRITICAL 5.5V-0.28PF 0201-1TH1CKSTNCL
DZF675 CRITICAL 5.5V-0.28PF 0201-1TH1CKSTNCL
DZF676 CRITICAL ESDL20-1BF4 0201-1TH1CKSTNCL
DZF677 CRITICAL ESDL20-1BF4 0201-1TH1CKSTNCL

RF677 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF676 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF675 220K 5% 1/20W MF 201 GND_VOID=TRUE
RF674 220K 5% 1/20W MF 201 GND_VOID=TRUE

PLACE VBUS CAP NEAR EACH VBUS PIN

PPVBUS_USBC1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=20V

PLACE_NEAR=JF601.30:5MM
ALLOW_APPLE_PREFIX=D

DF602
TVS2200
WSON
4 IN
5 IN
6 IN
GND 1
GND 2
GND 3
EPAD 7

CRITICAL
DZF600
X3-WLB1608-1
SDM2U40CSP

516S00686
PACK_OPTION=POR
JF601
20875-028E-01
F-ST-SMM

CRITICAL CF600 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF601 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF602 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF603 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF606 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF607 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF608 0.01UF 10% 25V X5R-CERM 0201
CRITICAL CF605 0.01UF 10% 25V X5R-CERM 0201

USBC1_D2R_CR_N<1>
USBC1_D2R_CR_P<1>
USBC1_R2D_N<1>
USBC1_R2D_P<1>
USBC1_USB_TOP_P
USBC1_USB_TOP_N
USBC1_D2R_CR_N<2>
USBC1_D2R_CR_P<2>
TP_USBC1_PP20V
USBC1_SBU2
USBC1_CC1_CONN
USBC1_USB_BOT_N
USBC1_USB_BOT_P
USBC1_SBU1
USBC1_CC2_CONN
USBC1_R2D_N<2>
USBC1_R2D_P<2>

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: Left Connectors

Apple Inc.

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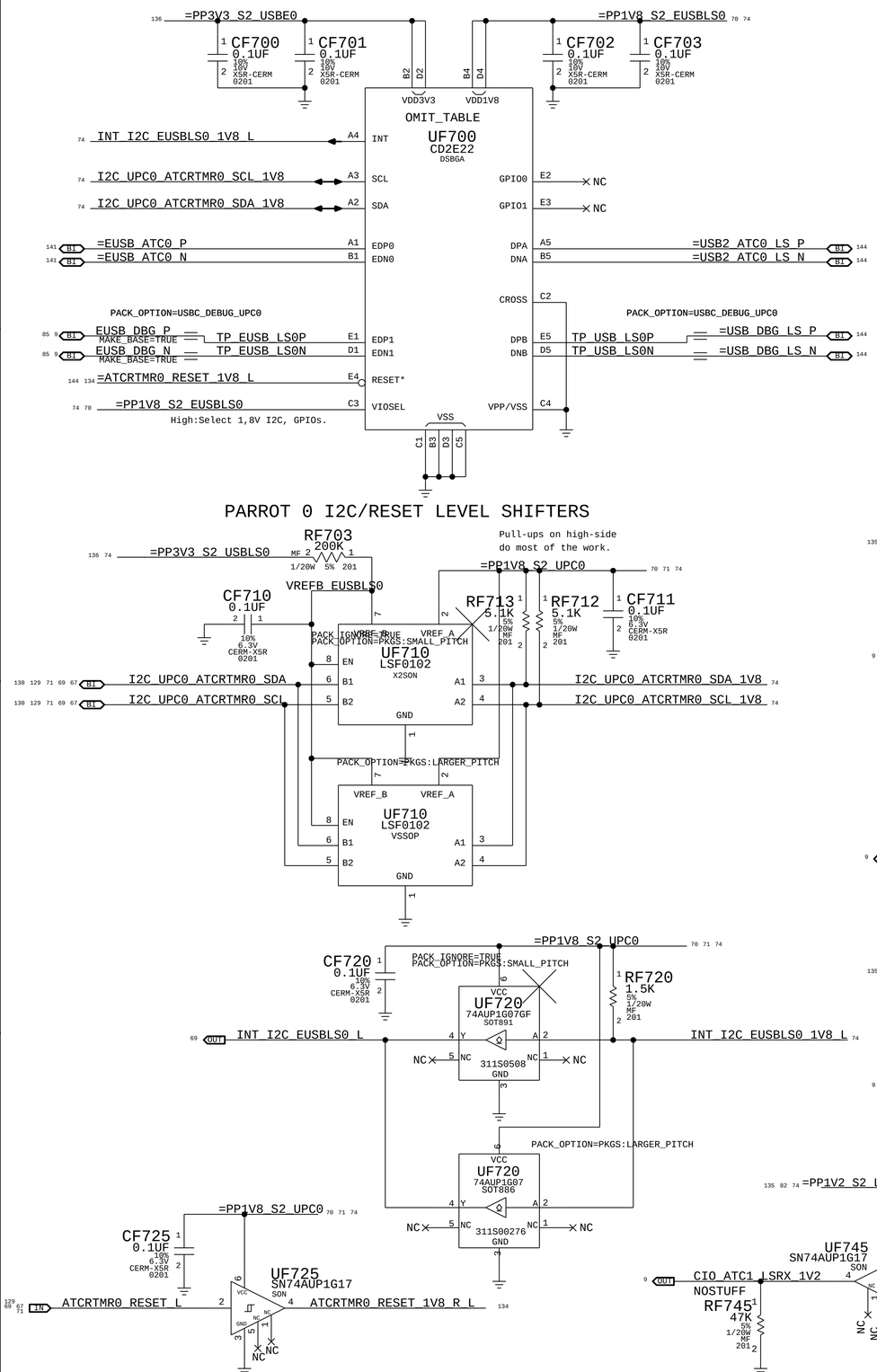
** OK2INTEGRATE **

PARROT 0 I2C/RESET LEVEL SHIFTERS



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: HS Level Shifters

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*** OK2INTEGRATE ***

=PPVIN_5VUSBC01

CF800 33UF 20% 16V TANT CASE-T 128S00009 (CAPDERATE POLY-TANT CRITICAL)
CF801 33UF 20% 16V TANT CASE-T 128S00009 (CAPDERATE POLY-TANT CRITICAL)
CF806 33UF 20% 16V TANT CASE-T 128S00009 (CAPDERATE POLY-TANT CRITICAL)
CF802 2.2UF 20% 25V X6S-CERM 0402 138S00042
CF803 2.2UF 20% 25V X6S-CERM 0402 138S00042
CF804 2.2UF 20% 25V X6S-CERM 0402 138S00042
CF805 2.2UF 20% 25V X6S-CERM 0402 138S00042

=PP1V8_S2_UPC01

CF840 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

UF840 SN74AUP1G08 USON

PMU_SYS_ALIVE (IN)
UPC0_5V_EN (IN)
UPC1_5V_EN (IN)
UPC01_5V_EN MAKE_BASE=TRUE
NC

RF840 0 5% 1/20W MF 0201 117S0201 NOSTUFF

RF830 0 5% 1/20W MF 0201 117S0201

RF834 360K 5% 1/20W MF 0201 117S0089

P5VUSBC01_EN_R

UF800 LT8642EV-2#PBF LQFN-THICKSTNCL CRITICAL

VIN	4	
VIN	5	
VIN	6	
VIN	13	
VIN	14	
VIN	15	
EN/UV	17	P5VUSBC01_EN
VC	22	P5VUSBC01_VC
PG	23	P5VUSBC01_PGOOD
FB	24	P5VUSBC01_FB
SS	21	P5VUSBC01_SS
RT	18	P5VUSBC01_RT
SYNC/MODE	20	
BIAS	1	P5VUSBC01_BIAS
INTVCC	2	P5VUSBC01_INTVCC
BST	7	P5VUSBC01_BST (SWITCH_NODE=TRUE DIDT=TRUE)
SW	8,9,10,11,12	P5VUSBC01_SW (SWITCH_NODE=TRUE DIDT=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000)
CLKOUT	19	NC
GND	3,16,25,26,27,28	
NC	29,30,31,32	

CF830 2.2UF 20% 25V X6S-CERM 0402 138S00042
CF831 2.2UF 20% 25V X6S-CERM 0402 138S00042

RF828 1.5 5% 1/20W MF 201 117S0029

CF832 47NF 10% 10V X6S-CERM 0201 132S00028

RF827 0 5% 1/20W MF 0201 117S0201

CRITICAL LF800 1UH-20%-11A-0.0127OHM PIHA052D-SM 152S00265

XWF820 SM

P5VUSBC01_FB_XW

RF822 10 5% 1/20W MF 0201 117S0004

P5VUSBC01_FB_RC

RF823 12.7K 1% 1/20W MF 0201 118S0070

RF826 47K 1% 1/20W MF 0201 118S0395

P5VUSBC01_FB_C

P5VUSBC01_FB_RC2

CF820 470PF 10% 16V X5R-X7R-CERM 0201 132S0361

CRITICAL RF824 200K 0.1% 1/20W TF 0201 118S0738

P5VUSBC01_FB

CRITICAL RF825 27.4K 0.1% 1/20W MF 0201 103S00009

RF833 20.5K 1% 1/20W MF 0201 118S0180

P5VUSBC01_VC_R

CF833 1000PF 10% 16V X7R-1 0201 132S0651
CF834 100PF 5% 25V C0G 0201 131S0805
CF835 0.01UF 10% 16V X7R-CERM 0402 132S0374

RF832 25.5K 1% 1/20W MF 0201 118S0235

XWF800 SM

P5VUSBC01_AGND

Vout=5.23V
EDC=6.6A
F=1.5MHz
START UP TIME < 15 MS

CF810 150UF 20% 6.3V TANT CASE-B-SM 128S00038 (CAPDERATE POLY-TANT CRITICAL)
CF811 150UF 20% 6.3V TANT CASE-B-SM 128S00038 (CAPDERATE POLY-TANT CRITICAL)
CF812 2.2UF 20% 25V X6S-CERM 0402 138S00042 (CRITICAL)
CF813 2.2UF 20% 25V X6S-CERM 0402 138S00042 (CRITICAL)

RF831 100K 5% 1/20W MF 201 117S0008

=PP5V_USBC01_REG

P5VUSBC01_PGOOD

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: 5V Regulator

Apple Inc.

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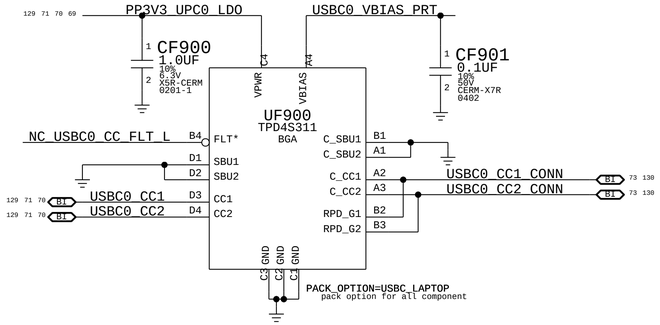
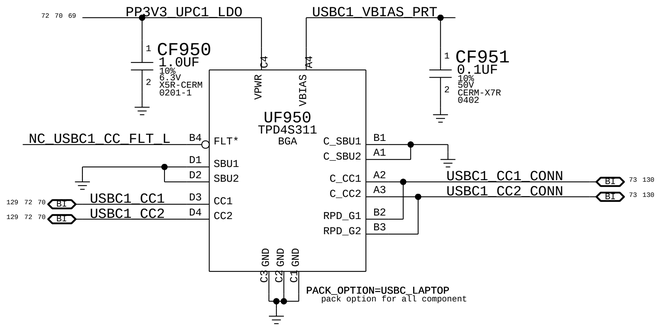
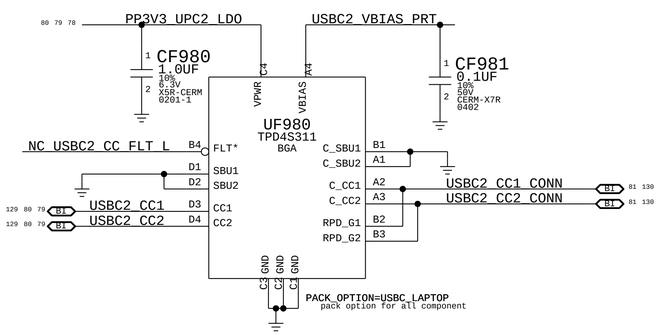
USBC0 CC Protection



USBC1 CC Protection



USBC2 CC Protection



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S00753	338S00740	ANY	ALL	<RDAR://73369307>

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: CC Protection

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** OK2INTEGRATE **

Caps and connector must be aliased to BBR signals.
Lanes 1 and 2 can be swapped, both pairs, both sides; all or nothing.
Inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

USBC HIGH-SPEED AC COUPLING

GND_VOID=TRUE

84 IN	USBC_ATC2_R2D_LS_C_P<1>	CG020	0.22UF	USBC_ATC2_R2D_LS_P<1>	141
84 IN	USBC_ATC2_R2D_LS_C_N<1>	CG021	0.22UF	USBC_ATC2_R2D_LS_N<1>	141
84 IN	USBC_ATC2_R2D_LS_C_P<2>	CG024	0.22UF	USBC_ATC2_R2D_LS_P<2>	141
84 IN	USBC_ATC2_R2D_LS_C_N<2>	CG025	0.22UF	USBC_ATC2_R2D_LS_N<2>	141
84 BI	USBC_ATC2_D2R_LS_P<1>	CG022	0.22UF	USBC_ATC2_D2R_LS_C_P<1>	141
84 BI	USBC_ATC2_D2R_LS_N<1>	CG023	0.22UF	USBC_ATC2_D2R_LS_C_N<1>	141
84 BI	USBC_ATC2_D2R_LS_P<2>	CG026	0.22UF	USBC_ATC2_D2R_LS_C_P<2>	141
84 BI	USBC_ATC2_D2R_LS_N<2>	CG027	0.22UF	USBC_ATC2_D2R_LS_C_N<2>	141

All: 2 — 20% 6.3V X5R 0201

9 BI	USBC_ATC2_AUX_P	CG028	0.1UF	10% 6.3V 0201 CERM-X5R
9 BI	USBC_ATC2_AUX_N	CG029	0.1UF	10% 6.3V 0201 CERM-X5R

RG028 33K 5% 1/20W MF 201 — RG029 33K 5% 1/20W MF 201

84 82 IN CIO_ATC2_LSTX_3V3
84 82 OUT CIO_ATC2_LSRX_3V3
NOSTUFF
RG008 100K 5% 1/20W MF 201 — RG009 100K 5% 1/20W MF 201

UG000 9999HH BGA SYM 2 OF 2 — 338S00561

CRITICAL OMIT_TABLE

141	=USBC_ATC2_R2D_LS_P<1>	GND_VOID=TRUE	J1	ASSRXP1	
141	=USBC_ATC2_R2D_LS_N<1>		J2	ASSRXN1	
141	=USBC_ATC2_R2D_LS_P<2>	GND_VOID=TRUE	C1	ASSRXP2	
141	=USBC_ATC2_R2D_LS_N<2>		C2	ASSRXN2	
141	=USBC_ATC2_D2R_LS_C_P<1>	GND_VOID=TRUE	G1	ASSTXP1	
141	=USBC_ATC2_D2R_LS_C_N<1>		G2	ASSTXN1	
141	=USBC_ATC2_D2R_LS_C_P<2>	GND_VOID=TRUE	E1	ASSTXP2	
141	=USBC_ATC2_D2R_LS_C_N<2>		E2	ASSTXN2	
84	USBC_ATC2_AUX_C_P		L8	PA_AUX_P	INTERNAL CAPS, PU, PD
84	USBC_ATC2_AUX_C_N		M8	PA_AUX_N	
84 82	CIO_ATC2_LSTX_3V3		M7	PA_LSTX_SBU1	
84 82	CIO_ATC2_LSRX_3V3		L7	PA_LSRX_SBU2	
78	INT_I2C_ATCRTMR2_L		A10	I2C_INT	
129 82 80 78	I2C_UPC2_ATCRTMR2_SCL		C9	I2C_SCL	
129 82 80 78	I2C_UPC2_ATCRTMR2_SDA		E7	I2C_SDA	
77	ATCRTMR2_GPIO_5		B9	POC_GPIO_5	
77	ATCRTMR2_GPIO_6		A8	POC_GPIO_6	To SPI Flash
77	ATCRTMR2_FLASH_SHARE_EN		A4	POC_GPIO_10	IPU ~ 65K
78 IN	ATCRTMR2_FLASH_MSTR_H_SLV_L		A5	POC_GPIO_11	IPU ~ 65K
77	ATCRTMR2_GPIO_12		A6	POC_GPIO_12	IPU ~ 65K
128 OUT	ATCRTMR2_THERM_D_P		M11	THERMDA	
77	ATCRTMR2_XTAL25M_IN		L9	XTAL_25_IN	
77	ATCRTMR2_XTAL25M_OUT		M9	XTAL_25_OUT	
			L12	MONDC_SVR	
			A11	MONDC	
			M12	TEST_EDM	
			A12	NC_A12	NC
			J6	NC_J6	NC
			L3	NC_L3	NC
			J5	NC_J5	NC

		GND_VOID=TRUE	J12	BSSRXP1	=USBC2_D2R_P<1> 141 BI
			J11	BSSRXN1	=USBC2_D2R_N<1> 141 BI
		GND_VOID=TRUE	C12	BSSRXP2	=USBC2_D2R_P<2> 141 BI
			C11	BSSRXN2	=USBC2_D2R_N<2> 141 BI
		GND_VOID=TRUE	G12	BSSTXP1	=USBC2_R2D_CR_P<1> 141 OUT
			G11	BSSTXN1	=USBC2_R2D_CR_N<1> 141 OUT
		GND_VOID=TRUE	E12	BSSTXP2	=USBC2_R2D_CR_P<2> 141 OUT
			E11	BSSTXN2	=USBC2_R2D_CR_N<2> 141 OUT
			M10	BSBU1	USBC2_AUXLSX_P 80 BI
			L10	BSBU2	USBC2_AUXLSX_N 80 BI
			B8	PERST*	ATCRTMR23_ACTIVE_READY_3V3 77 78 IN
			L11	RESET*	ATCRTMR2_RESET_L 80 82 129 IN
			A3	TDI	=JTAG_ATCRTMR2_TDI 78 IN
			C3	TMS	=JTAG_ATCRTMR2_TMS 78 IN
			B5	TCK	=JTAG_ATCRTMR2_TCK 78 IN
			C5	TDO	=JTAG_ATCRTMR2_TDO 78 OUT
			C6	EE_DI	SPI_ATCRTMR2_R_MOSI 78 OUT
			B4	EE_DO	SPI_ATCRTMR2_R_MISO 78 IN
			B6	EE_CS*	SPI_ATCRTMR2_R_CS_L 78 OUT
			C7	EE_CLK	SPI_ATCRTMR2_R_CLK 78 OUT
			B11	TEST_EN	
			B3	TEST_PWR_GOOD	ATCRTMR2_TEST_PWR_GOOD
			L4	RBIAS	ATCRTMR2_RBIAS
			L5	RSENSE	ATCRTMR2_RSENSE
			A1	ATEST_P	NC
			A2	ATEST_N	NC
			B10	FORCE_PWR	ATCRTMR2_FORCE_PWR 78 80 IN
			A9	FLASH_BUSY*	FLASH_BUSY_USBC23_L 78 129 BI
			B2	FUSE_VQPS_64	
			A7	SMBUS_SCL	TP_SMBUS_ATCRTMR2_SCL 142
			B7	SMBUS_SDA	TP_SMBUS_ATCRTMR2_SDA 142

RG006 100 5% 1/20W MF 201
RG007 4.75K 0.5% 1/20W TF 0201
PLACE_NEAR=UG000.L5:2MM
PLACE_NEAR=UG000.L4:2MM

=PP3V3_ATCRTMR2_SX 77 78 136
=PP3V3_ATCRTMR2 77 78 136
=PP3V3_ATCRTMR2_SVR 77 78 136
=PP3V8_ATC2_LDO 136
=USBC2_3V3LDO_EN 141 IN
ATCRTMR23_ACTIVE_READY_3V3 78 77 IN

RG050 100K 5% 1/20W MF 201 — ATCRTMR2_GPIO_5 77
NOSTUFF RG041 100K 5% 1/20W MF 201 — ATCRTMR2_GPIO_6 77
RG040 0 5% 1/20W MF 0201
NOSTUFF RG051 100K 5% 1/20W MF 201
NOSTUFF RG043 100K 5% 1/20W MF 201 — ATCRTMR2_FLASH_SHARE_EN 77
NOSTUFF RG045 100K 5% 1/20W MF 201 — ATCRTMR2_GPIO_12 77

ATCRTMR2_XTAL25M_OUT_R — RG002 0 0201 5% MF 1/20W — ATCRTMR2_XTAL25M_OUT 77
CG002 20PF 5% 25V C0G 0201
CG003 20PF 5% 25V C0G 0201
CRITICAL YG000 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
RG003 0 0201 5% MF 1/20W — ATCRTMR2_XTAL25M_IN 77
ATCRTMR2_XTAL25M_IN_R

UG000 9999HH BGA SYM 2 OF 2 — 338S00561

CRITICAL OMIT_TABLE

77	PP0V9_ATCRTMR2_SVR		F6	VCC0P9_SVR_ANA	
			G6		
			E9	VCC0P9_SVR_PB_ANA	
			G9		
	PP0V9_ATCRTMR2_LVR	VOLTAGE=0.9V	L6	VCC0P9_LVR	
			M6	VCC0P9_LVR_SENSE	
	PP3V3_ATCRTMR2_ANA	VOLTAGE=3.3V	E5	VCC3P3_LC	
			L2	VCC3P3_ANA	
78	PP0V9_ATCRTMR2_LC	VOLTAGE=0.9V	J3	VCC0P9_LC	
	PP3V3_ATCRTMR2_LC	VOLTAGE=3.3V	F3		
			F5	VSS	
			G5		
			B1		
			B12		
			D1		
			D11		
			D12	VSS_ANA	
			D2		
			F1		
			F11		
			F12		
			F2		

			E6	VCC3P3_SX	
			J7	VCC3P3A	
			M4	VCC3P3_SVR	
			M5		
			E3	VCC0P9_SVR	
			G3		
			L1	SVR_IND	
			M1		
			M2	SVR_VSS	
			M3		
			F7		
			F9		
			G7		
			H1		
			H11		
			H12	VSS_ANA	
			H2		
			J9		
			K1		
			K11		
			K12		
			K2		

CG065 20UF 20% 2.5V X6S-CERM 0402
CG064 20UF 20% 2.5V X6S-CERM 0402
CG063 20UF 20% 2.5V X6S-CERM 0402
CG062 20UF 20% 2.5V X6S-CERM 0402
CG061 4UF 20% 6.3V CER-X5R 0201
CG060 4UF 20% 6.3V CER-X5R 0201
CG050 4UF 20% 6.3V CER-X5R 0201
CG051 4UF 20% 6.3V CER-X5R 0201
CG052 4UF 20% 6.3V CER-X5R 0201
CG053 4UF 20% 6.3V CER-X5R 0201

CG054 10UF 20% 6.3V CERM 0402
CG055 2.2UF 20% 6.3V X5R-CERM 0201
CG056 2.2UF 20% 6.3V X5R-CERM 0201
CG057 2.2UF 20% 6.3V X5R-CERM 0201
CG058 2.2UF 20% 6.3V X5R-CERM 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

VOLTAGE=3.3V PP3V3_ATCRTMR2_VCCA
CG043 12PF 5% 25V NP0-C0G 0201
CG030 2.2UF 20% 6.3V X5R-CERM 0201
CG031 10UF 20% 6.3V CERM 0402
RG000 0 5% 1/16W MF-LF 402
RG001 0 5% 1/16W MF-LF 402
CG036 2.2UF 20% 6.3V X5R-CERM 0201
CG037 2.2UF 20% 6.3V X5R-CERM 0201
NOSTUFF CG042 47UF 20% 6.3V CER-X5R 0603
FROM USB-C PORT CONTROLLER (UPC)

VOLTAGE=3.3V PP3V3_ATCRTMR2_SVR
CG032 10UF 20% 6.3V CERM 0402
CG033 10UF 20% 6.3V CERM 0402
CG034 10UF 20% 6.3V CERM 0402
CG035 10UF 20% 6.3V CERM 0402
BYPASS=UG000.M4:M3:3MM
XWG001 SM — NO_XNET_CONNECTION=1

VOLTAGE=0V P0V9_ATCRTMR2_SVR_PGND
XWG000 SM — NO_XNET_CONNECTION=1
PLACE_NEAR=CG032.2:2MM

CG038 12PF 5% 25V NP0-C0G 0201
CG039 4UF 20% 6.3V CER-X5R 0201
CG041 4UF 20% 6.3V CER-X5R 0201
CG040 47UF 20% 6.3V CER-X5R 0603
PP0V9_ATCRTMR2_SVR 77 VOLTAGE=0.9V

CRITICAL LG000 0.68UH-20%-4.3A-0.043OHM 0805
PP0V9_ATCRTMR2_SVR_IND VOLTAGE=0.9V DIDT=TRUE

XWG030 SM — ATCRTMR2_THERM_D_N 128 OUT
PLACE_NEAR=UG000.K11:2MM
NO_XNET_CONNECTION=1
CONNECT TO GND PIN CLOSEST TO THERMDA PIN

3.3V LDO

PACK_IGNORE=TRUE
PACK_OPTION=PKGS:SMALL_PITCH
AVOW_APPLE_PREFIX=U

UG015 TLV75533 X2SON: IN 4, EN 3, GND 2, THRM PAD 5, OUT 1
RG012 100K 5% 1/20W MF 201
CG010 1.0UF 20% 6.3V X5R 0201-1
CG015 1.0UF 20% 6.3V X5R 0201-1
PACK_OPTION=PKGS:LARGER_PITCH
UG015 TLV75533 WSON: IN 6, EN 4, OUT 1, NC 2, NC 5, GND, EPAD 3 7

BOM_COST_GROUP=TBT

PAGE TITLE	USB-C: High Speed ATC2
	Apple Inc.
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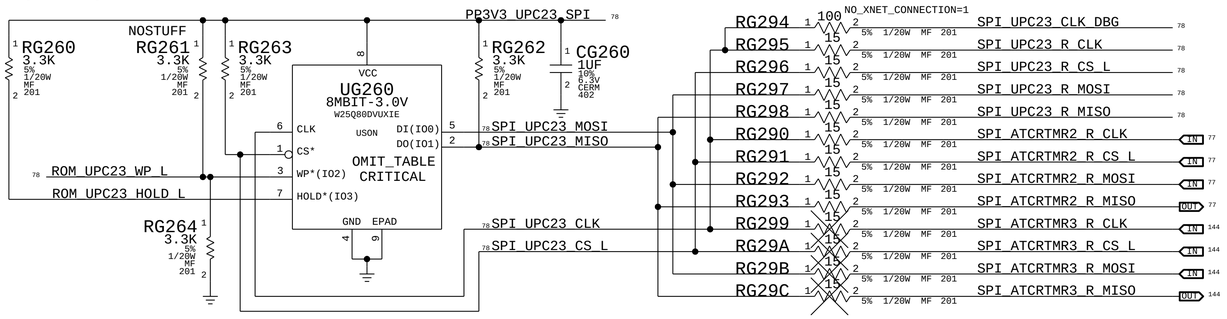
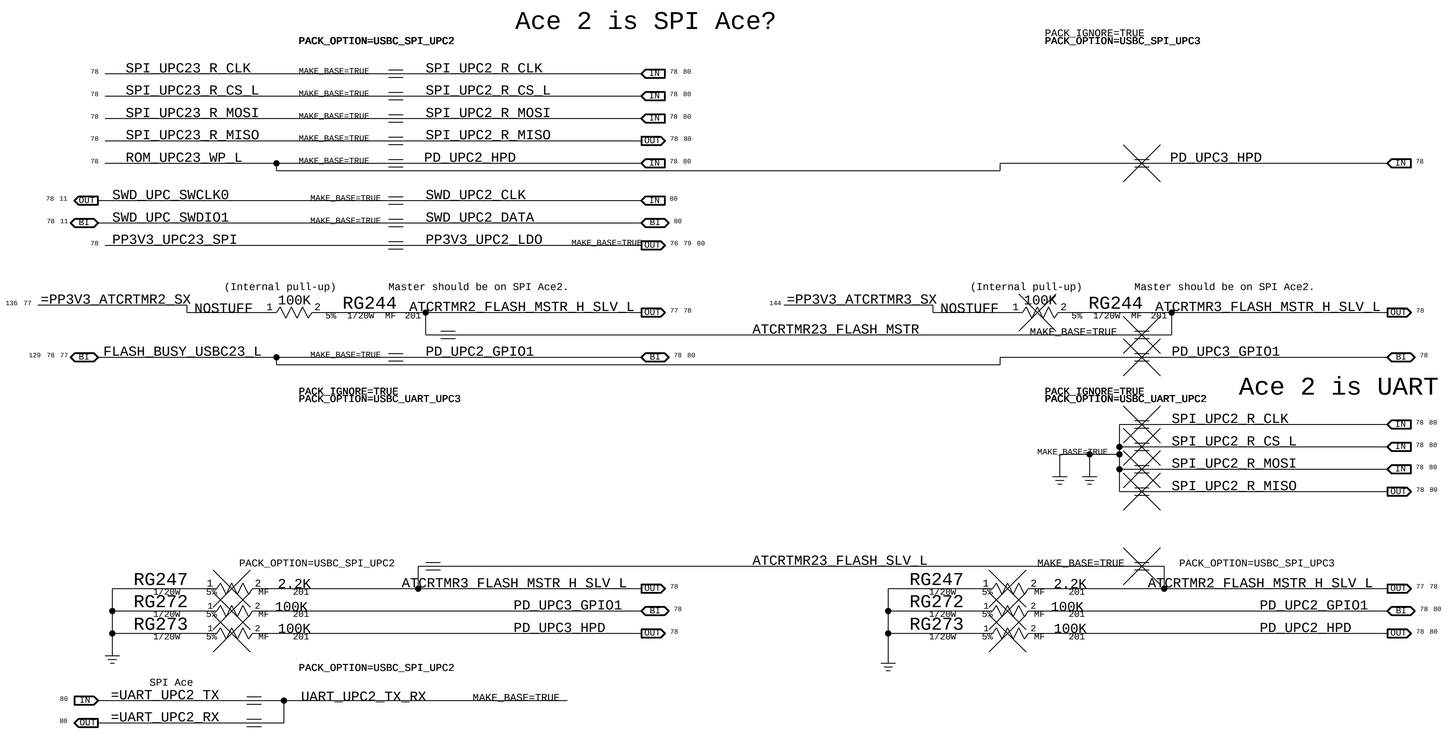
** OK2INTEGRATE **

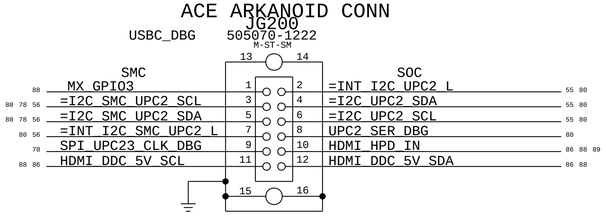


Ace 2 is SPI Ace?

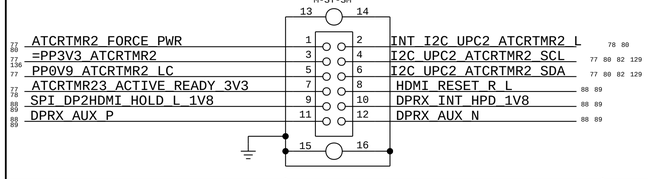


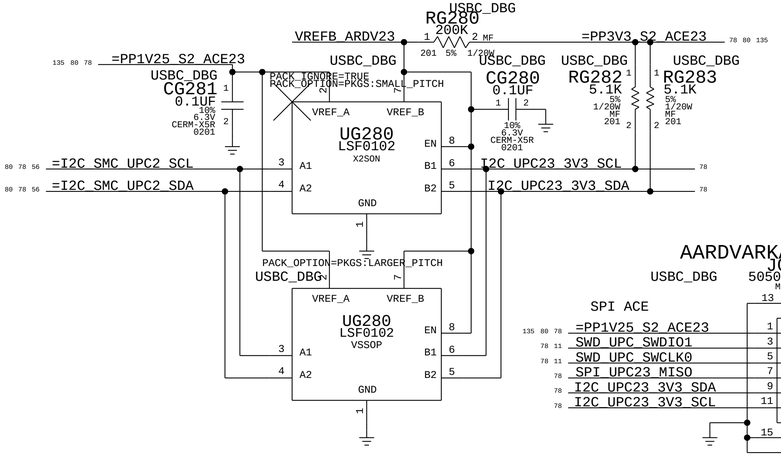
Ace 2 is UART Ace?

ACE ARKANOID CONN

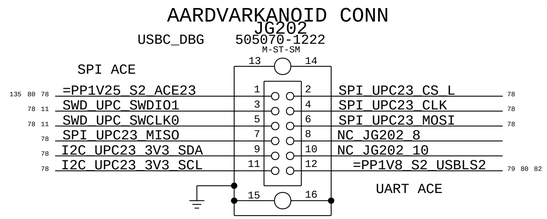


BRIDGE ARKANOID CONN

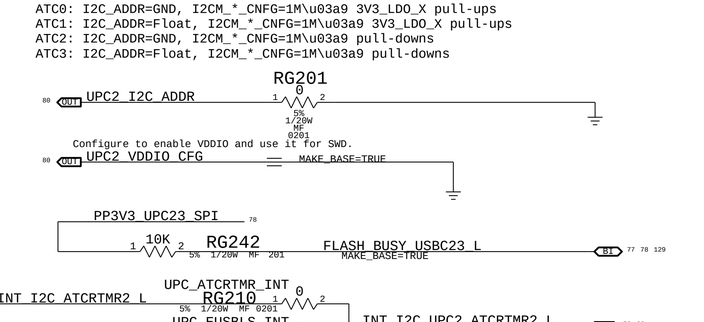




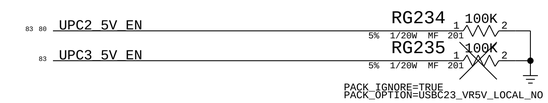
AARDVARKANOID CONN

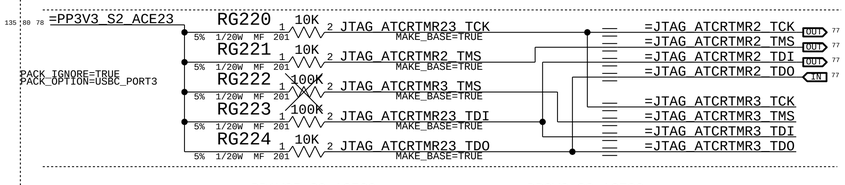


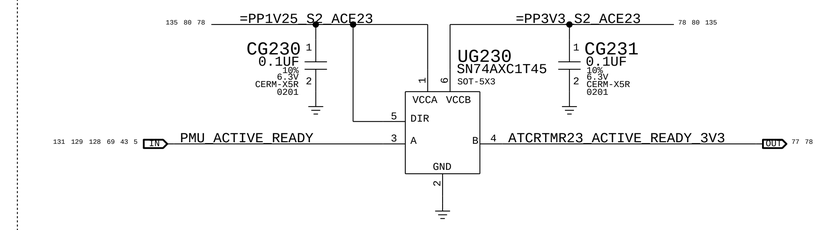
BOM_COST_GROUP=USB-C



Is UPCx_5V_EN being used?



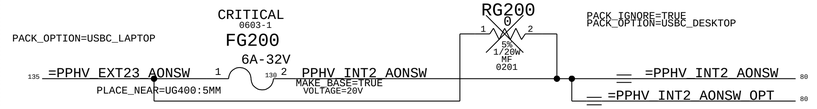


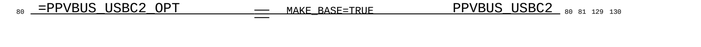


HV POWER ALIASES

Fuses for laptop charging.

Desktops only need connection for programming OTP.





PAGE TITLE	USB-C: Support 1 ATC23
	Apple Inc.
DRAWING NUMBER	051-05641
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SYNC_DATE=02/18/2020

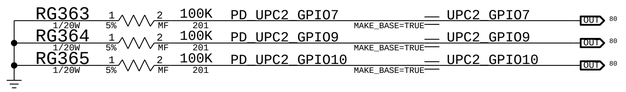
** OK2INTEGRATE **

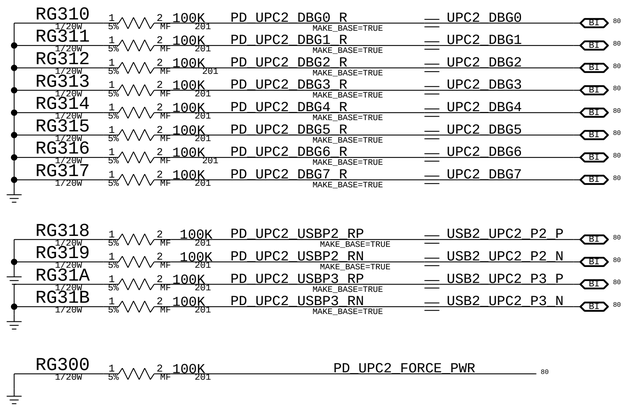
USB-C Port assignments

This schematic not currently set up to allow ATC channels 2 or 3 be the debug port.
These options can be added if needed.

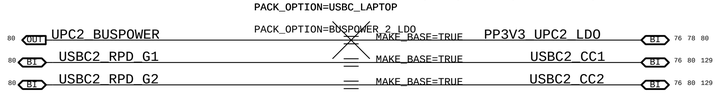
Unused ports

Ace2 GPIOs





Connections for Laptops (USBC power in)



Connections for Desktops (No USBC power in)

BOM_COST_GROUP=USB-C

SYNC_MASTER=T724_RUEN3OU_MLB_S_0-55_1 SYNC_DATE=03/26/2020

PAGE TITLE
USB-C: Support 2 ATC23

Apple Inc.

DRAWING NUMBER 051-05641 SIZE D
REVISION 6.33.0
BRANCH
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** OK2INTEGRATE **

PP3V3_UPC2_LDO 76 78 79 80

Note: I2CM pins pulled to 3.3V for P0 only
Pull to GND for P1 and forward

1M RG409 I2C_UPC2_ATCRTMR2_SCL 77 78 80 82 129
5% 1/20W MF 201 CKPLUS_WAIVE=I2C_PULLUP

1M RG408 I2C_UPC2_ATCRTMR2_SDA 77 78 80 82 129
5% 1/20W MF 201 CKPLUS_WAIVE=I2C_PULLUP

10K RG407 INT_I2C_UPC2_ATCRTMR2_L 78 80
5% 1/20W MF 201

1M RG405 =UART_UPC2_RX 78 80
5% 1/20W MF 201

100K RG406 PD_UPC2_MRESET 80
5% 1/20W MF 201

100K RG402 PD_UPC2_GPIO5 80 85
5% 1/20W MF 201

NOSTUFF

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

PP3V3_UPC2_LDO 76 78 79 80

NOSTUFF
0 RG420
5% 1/20W MF 0201

0 RG421 UPC2_BUSPOWER 79 80
5% 1/20W MF 0201

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

78 =PPHV_INT2_AONSW

MAX 100uF TOTAL ON RAIL

136 =PP5V_S2_ACE23_VCONN

136 =PP5V_S2_ACE23
CAP FOR PP_5V0 ON VR PAGE

K9 L10 M9 M10 K11 L12 M11 N12 — PP_5V0
M14 M13 — PP_CABLE
G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 M2 N4 — PP_HV
G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8 — VBUS

UG400
CD3217B12BCE
FCBGA
353S02158
CRITICAL
OMIT_TABLE

CRITICAL
RG403 15K 0.1% 1/20W TF-1F 0201

GND_I2C_ADDR
PRIMARY ONLY

		B13	HRESET	
80	PD_UPC2_MRESET	A14	MRESET	
129 82 77 OUT	ATCRTMR2_RESET_L	B17	RESET*	
78 OUT	UPC2_SER_DBG	A2	GPIO0	
		B1		
78 OUT	PD_UPC2_GPIO1	D1	GPIO1	
80 78 IN	INT_I2C_UPC2_ATCRTMR2_L	F1	GPIO2	
83 78 OUT	UPC2_5V_EN	C2	GPIO3	
78 77 OUT	ATCRTMR2_FORCE_PWR	E2	GPIO4	
85 80	PD_UPC2_GPIO5	B3	GPIO5	
79	PD_UPC2_FORCE_PWR	C4	GPIO6	DIGITAL CORE I/O & CONTROL
79 OUT	UPC2_GPIO7	D3	GPIO7	
134 132 130 72 71 44 OUT	UPC_PMU_RESET_3V3	E4	GPIO8	
79 IN	UPC2_GPIO9	F3	GPIO9	
79 OUT	UPC2_GPIO10	F7	GPIO10	
80 79	UPC2_BUSPOWER	A18	BUSPOWER	
78	UPC2_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
	UPC2_R_OSC	M21	R_OSC	
129 82 80 78 77 BI	I2C_UPC2_ATCRTMR2_SDA	A16	I2CM_SDA_CNFG	
129 82 80 78 77 BI	I2C_UPC2_ATCRTMR2_SCL	B15	I2CM_SCL_CNFG	
78 55 BI	=I2C_UPC2_SDA	B5	I2C_SDA1	
78 55 BI	=I2C_UPC2_SCL	A4	I2C_SCL1	
78 55 OUT	=INT_I2C_UPC2_L	D7	I2C_IRQ1*	
78 56 BI	=I2C_SMC_UPC2_SDA	B7	I2C_SDA2	
78 56 BI	=I2C_SMC_UPC2_SCL	A6	I2C_SCL2	
78 56 OUT	=INT_I2C_SMC_UPC2_L	C8	I2C_IRQ2*	
78 OUT	SPI_UPC2_R_CLK	B9	SPI_CLK	
78 OUT	SPI_UPC2_R_MOSI	B11	SPI_MOSI	
78 IN	SPI_UPC2_R_MISO	A10	SPI_MISO	
78 OUT	SPI_UPC2_R_CS_L	A8	SPI_SSZ	
78 BI	SWD_UPC2_DATA	E20	SWD_DATA	IPU
78 BI	SWD_UPC2_CLK	E16	SWD_CLK	IPU
80 78 IN	=UART_UPC2_RX	B19	UART_RX	
78 OUT	=UART_UPC2_TX	A20	UART_TX	
85 BI	USB2_UPC2_P1_P	H19	USB_RP1_P	
85 BI	USB2_UPC2_P1_N	H21	USB_RP1_N	
79 BI	USB2_UPC2_P2_P	G20	USB_RP2_P	
79 BI	USB2_UPC2_P2_N	G22	USB_RP2_N	
79 BI	USB2_UPC2_P3_P	F19	USB_RP3_P	
79 BI	USB2_UPC2_P3_N	F21	USB_RP3_N	
72 BI	USBC2_AUXLSX_P	J12	AUX_P	
72 BI	USBC2_AUXLSX_N	H11	AUX_N	
78 OUT	PD_UPC2_HPD	C12	HPD	
79 BI	UPC2_DBG0	G12	DEBUG0	
79 BI	UPC2_DBG1	F11	DEBUG1	
79 BI	UPC2_DBG2	E8	DEBUG2	
79 BI	UPC2_DBG3	E12	DEBUG3	
79 OUT	UPC2_DBG4	G16	DEBUG4	
79 BI	UPC2_DBG5	F15	DEBUG5	
79 IN	UPC2_DBG6	D15	DEBUG6	
79 OUT	UPC2_DBG7	D19	DEBUG7	

PORT_MUX

PPVBUS_USBC2 78 81 129 130

CG401 1UF 10% 25V X5R 0402

=PP3V3_S2_ACE23 78 135

CG400 10UF 20% 6.3V CERM 0402

=PP1V25_S2_ACE23 78 135

CG402 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
PP3V3_UPC2_LDO 76 78 79 80

CG408 10UF 20% 6.3V CERM 0402

=PP1V8_S2_USBLS2 78 79 82

CG403 0.1UF 10% 6.3V CERM-X5R 0201

USBC2_3V3LDO_EN 130 141
(cap needed when used as power source)

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	UPC2_VDDIO_CFG	78
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18		
VRET	C16		
SS	L22	UPC2_SS	
LDO_CORE	E22	PP1V5_UPC2_LDO_CORE	
VBUS_OPT	D5	=PPVBUS_USBC2_OPT	78
PP_HV_OPT	F5	=PPHV_INT2_AONSW_OPT	78

POWER

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
CG405 10UF 20% 6.3V CERM 0402

CG409 0.68UF 20% 6.3V X6S 0402

TYPE-C

C_CC1	M15	USBC2_CC1	
	N16		
C_CC2	M17	USBC2_CC2	
	N18		
RPD_G1	L14	USBC2_RPD_G1	BI 79
RPD_G2	L16	USBC2_RPD_G2	BI 79
C_USB_TP	K19	USBC2_USB_TOP_P	BI 81
C_USB_TN	K21	USBC2_USB_TOP_N	BI 81
C_USB_BP	J20	USBC2_USB_BOT_P	BI 81
C_USB_BN	J22	USBC2_USB_BOT_N	BI 81
C_SBU1	J16	USBC2_SBU1	BI 81 129
C_SBU2	H15	USBC2_SBU2	BI 81 129

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
BI 76 79 129

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
BI 76 79 129

CG414 220PF 5% 50V C0G 0201-1

CG413 220PF 5% 50V C0G 0201-1

GND_OPT	C18	
GND_OPT	E18	
GND_OPT	D17	
GND_OPT	G18	

GND

GND
A22 H9 N20 B21 K15 N22

BOM_COST_GROUP=USB-C

SYNC_MASTER=T724_RUENJOU_MLB_S_0.55.1 SYNC_DATE=03/26/2020

PAGE TITLE
USB-C: Port Controller ATC2

Apple Inc.

DRAWING NUMBER 051-05641
SIZE D
REVISION 6.33.0
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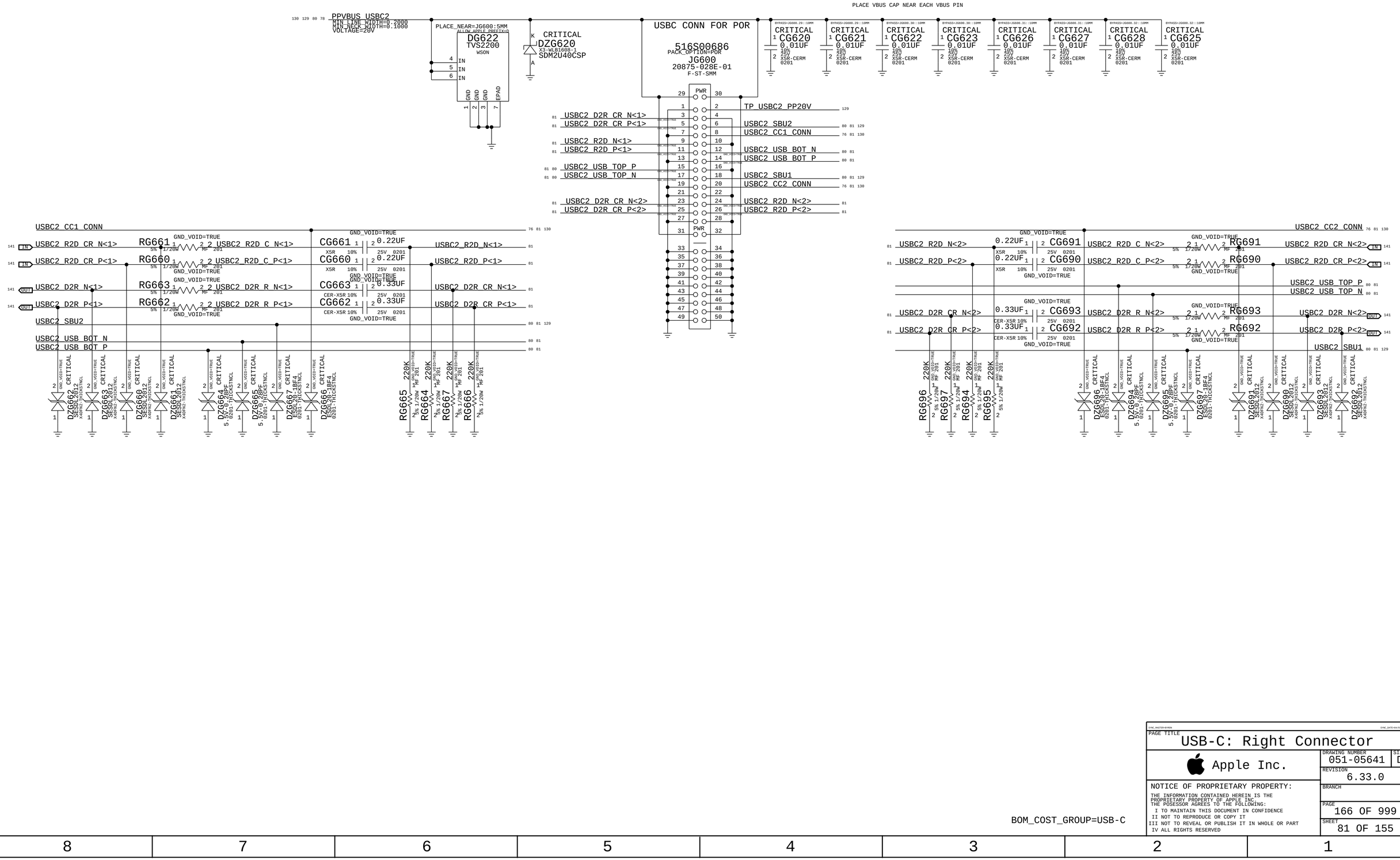
Right Side Port



BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: Right Connector
	Apple Inc.
DRAWING NUMBER	051-05641
SIZE	D
REVISION	6.33.0
BRANCH	
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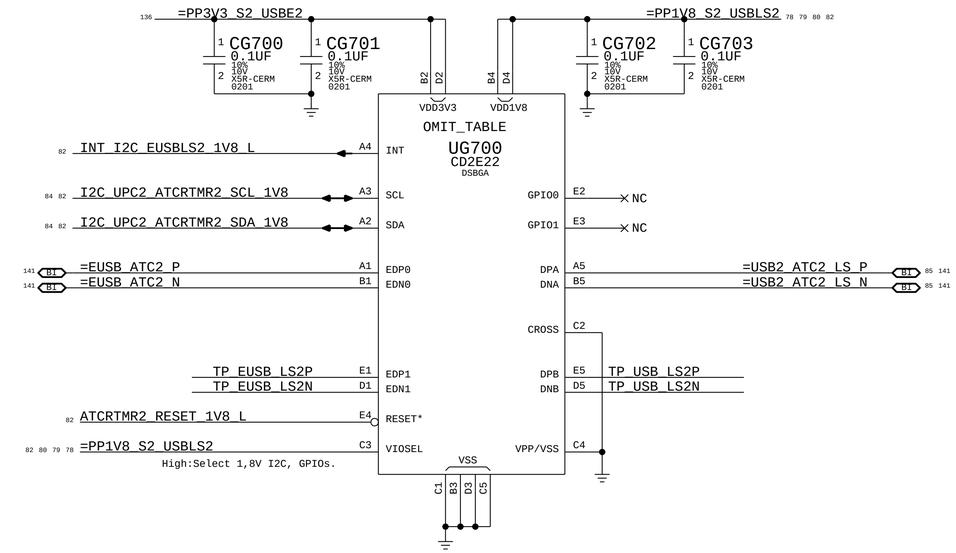
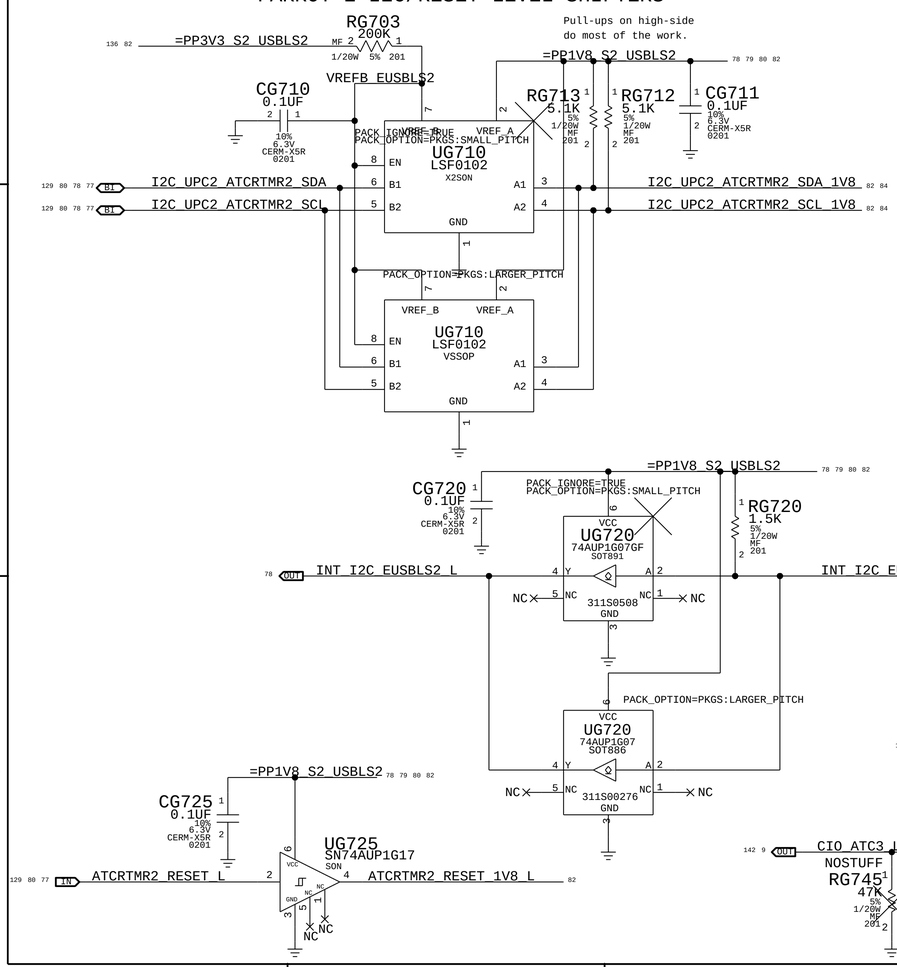
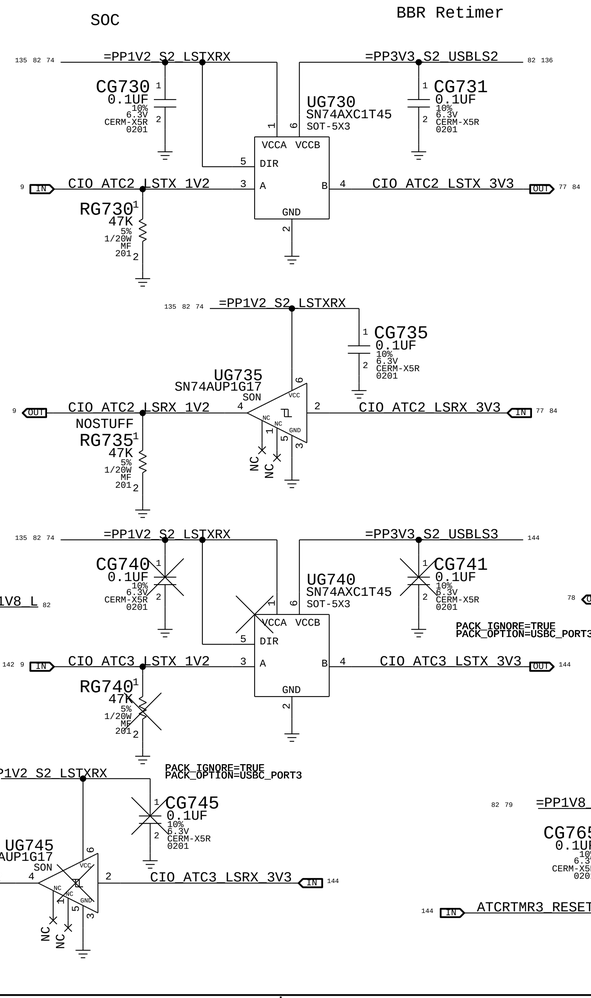
** OK2INTEGRATE **

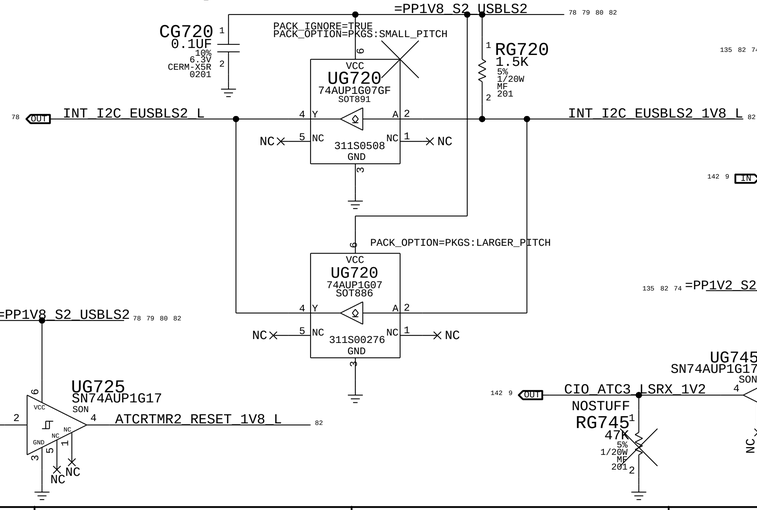


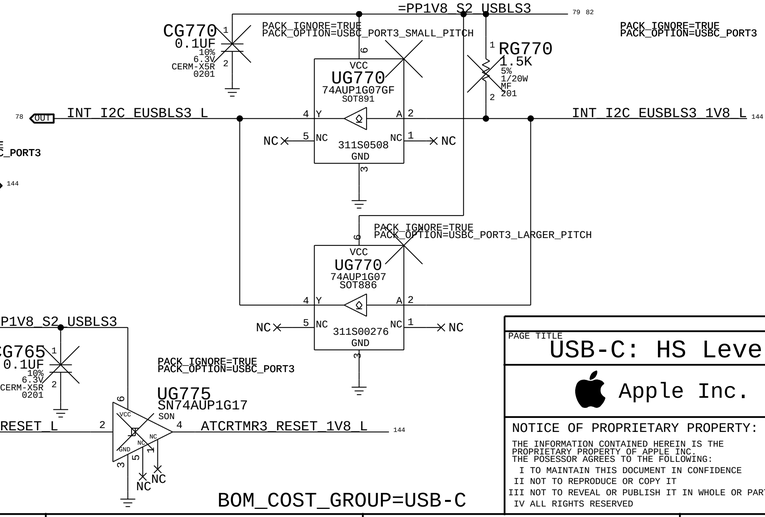
PARROT 2 I2C/RESET LEVEL SHIFTERS



TBT LS RX/TX LEVEL SHIFTERS







BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: HS Level Shifters

Apple Inc.

DRAWING NUMBER 051-05641
SIZE D
REVISION 6.33.0
BRANCH
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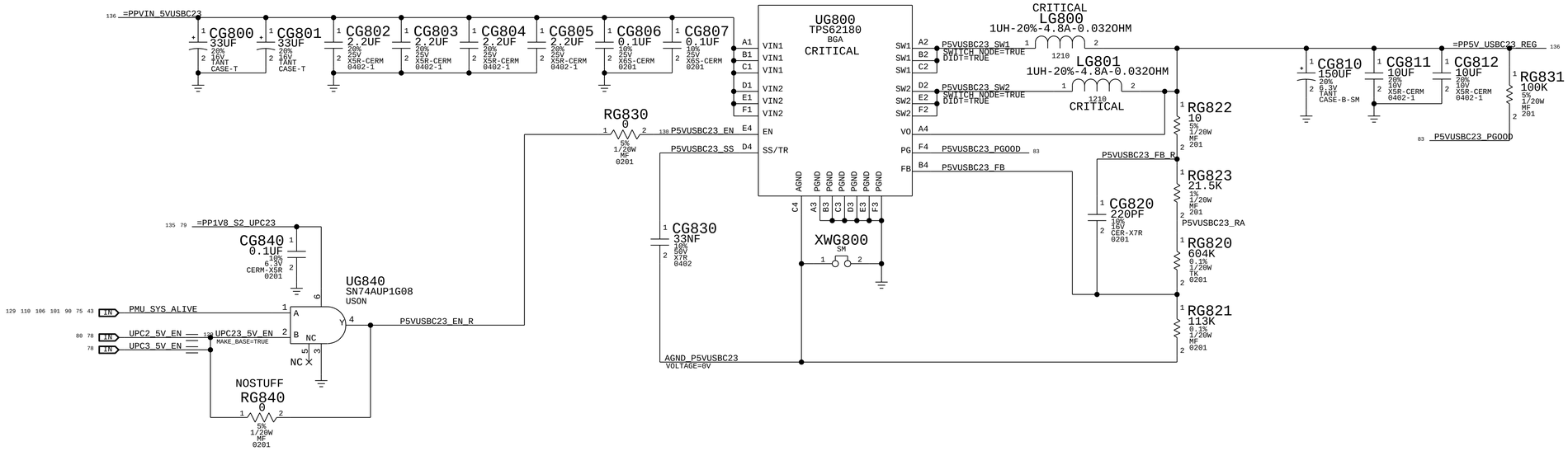
*** OK2INTEGRATE ***

Vout = 5.23V
Freq = 1.9-2.0MHz
OCP Max = 9A
OCP Nom = 7A
OCP Min = 4A
Icc Max = 3.3A



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: 5V Regulator

Apple Inc.

DRAWING NUMBER 051-05641
SIZE D
REVISION 6.33.0
BRANCH
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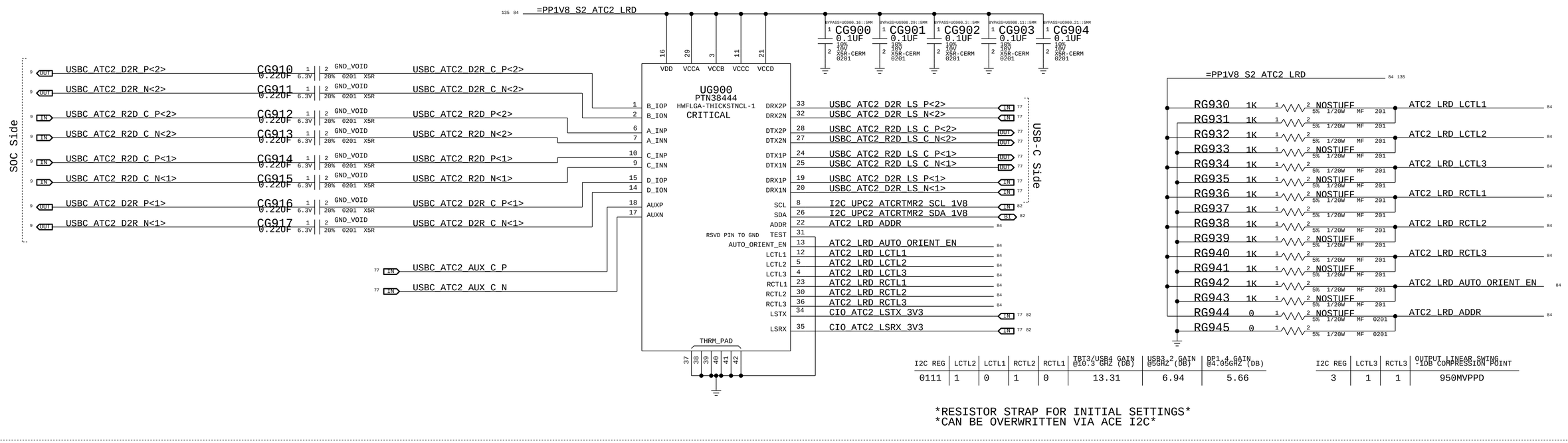
*** In Progress ***



I2C REG	LCTL2	LCTL1	RCTL2	RCTL1	TBT3/USB4 GAIN @10.3 GHZ (DB)	USB3.2 GAIN @5GHZ (DB)	DP1.4 GAIN @4.05GHZ (DB)
0111	1	0	1	0	13.31	6.94	5.66

I2C REG	LCTL3	RCTL3	OUTPUT LINEAR SWING -1DB COMPRESSION POINT
3	1	1	950MVPPD

RESISTOR STRAP FOR INITIAL SETTINGS
CAN BE OVERWRITTEN VIA ACE I2C

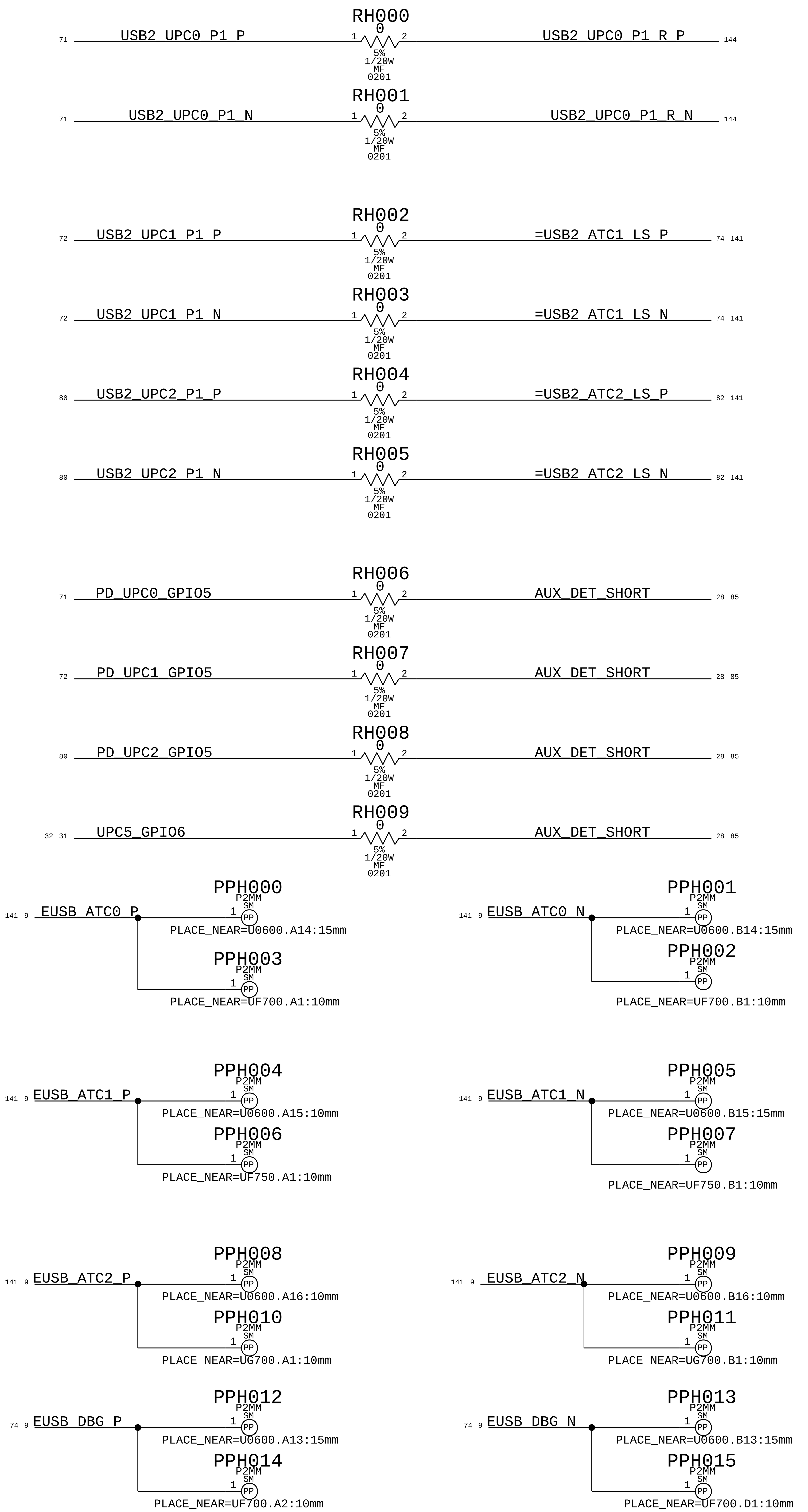
ATC3 Redriver still in progress
Circuit will be identical to that of ATC2

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: CIO Redrivers 2/3

Apple Inc.

DRAWING NUMBER: 051-05641 SIZE: D
REVISION: 6.33.0
BRANCH:
PAGE: 169 OF 999
SHEET: 84 OF 155



BOM_COST_GROUP=USB-C

PAGE TITLE

USB-C: SUPPORT

Apple Inc.

DRAWING NUMBER 051-05641 SIZE D

REVISION 6.33.0

BRANCH

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*** OK2INTEGRATE***

HDMI CONNECTOR
THRU-HOLE

(PER HDMI SPEC, SOURCE MUST SUPPLY MINIMUM 55 MA TO SINK)

(0.5A OVER-CURRENT LIMIT IMPLEMENTED)

HDMI SPEC 1.4B (SEC 4.2.7):
+5.0V M: 5.3V [SOURCE REQ]
+5.0V L: 4.8V [SOURCE REQ]
*ELEC SPECS NOT IN 2.0 SPEC YET

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0077	377S0183		DZH505	

JH500
RCPT-HDMI-X2094
F-RT-TH

129 87 IN HDMI_DATA_CONN_P<2> GND_VOID=TRUE — 1 TMDS_DATA2+ | 2 TMDS_DATA2_SHLD
129 87 IN HDMI_DATA_CONN_N<2> GND_VOID=TRUE — 3 TMDS_DATA2- | 4 TMDS_DATA1+ — HDMI_DATA_CONN_P<1> GND_VOID=TRUE — IN 87 129
5 TMDS_DATA1_SHLD | 6 TMDS_DATA1- — HDMI_DATA_CONN_N<1> GND_VOID=TRUE — IN 87 129
129 87 IN HDMI_DATA_CONN_P<0> GND_VOID=TRUE — 7 TMDS_DATA0+ | 8 TMDS_DATA0_SHLD
129 87 IN HDMI_DATA_CONN_N<0> GND_VOID=TRUE — 9 TMDS_DATA0- | 10 TMDS_CLK+ — HDMI_CLK_CONN_P GND_VOID=TRUE — IN 87 129
11 TMDS_CLK_SHLD | 12 TMDS_CLK- — HDMI_CLK_CONN_N GND_VOID=TRUE — IN 87 129
129 86 HDMI_CEC_CONN — 13 CEC | 14 RSRVD — HDMI_RSVD
129 86 HDMI_DDC_5V_CONN_SCL — 15 SCL | 16 SDA — HDMI_DDC_5V_CONN_SDA — 86 129
17 DDC/CEC/HEC GND | 18 +5V_PWR — PP5V0_HDMI_DDC_CONN VOLTAGE=5V
129 86 HDMI_HPD_IN_CONN — 19 HOT_PLUG_DETECT

514S00354
SHLD PINS
OMIT_TABLE

20 IO20 | 21 IO21
22 IO22 | 23 IO23
24 IO24 | 25 IO25
26 IO26 | 27 IO27
28 IO28 | 29 IO29
30 IO30 | 31 IO31
32 IO32 | 33 IO33

RH525 0 5% 1/20W MF 0201

HDMI SPEC 1.4B (SEC 4.2.9):
HPD H:2.0 - 3.3V [SOURCE REQ]
HPD L:0.0 - 0.8V [SOURCE REQ]
HDMI SPEC 1.4B (SEC 4.2.10):
CEC H:2.50 - 3.63V
CEC L:0.00 - 0.60V
*ELEC SPECS NOT IN 2.0 SPEC YET

INTEGRATORS, PLEASE HAVE SEPARATE BOM TABLE FOR JH500

FLH500 600-OHM-25%-1.3A-0.15OHM 0603
DZH505 5.5V-6.2PF 0201-THICKSTNCL
CH512 1UF 10% 25V X5R 402
CH511 0.1UF 10% 10V X5R-CERM 0201
CH515 0.1UF 10% 10V X5R-CERM 0201
PP5V0_HDMI_DDC_LDSW VOLTAGE=5V

QH502 DMG1016V SOT-563
=PP5V_S2_HDMI 86 90
SYS_ALIVE_BUFF
RH524 100K 5% 1/20W MF 201
RH523 10K 5% 1/20W MF 201
P-CHN
HDMI_CECFET_EN_Q
RH508 560 5% 1/20W MF 201
N-CHN
QH502 DMG1016V SOT-563
HDMI_CECFET_EN — IN 43 129
CEC_PFET_GATE_R
CH513 2.2UF 20% 10V X5R-CERM 402

=PP5V_S2_HDMI 86 90
NOSTUFF CH514 0.1UF 10% 10V X5R-CERM 0201
CH516 12PF 5% 25V NP0-C0G 0201
DH507 NSR0620P2XXG SOD-923-HF
RH528 0 5% 1/20W MF 0201
HDMI_PWR_EN — VTH(MAX) = 1.15V

90 86 =PP5V_S2_HDMI
RH527 4.7K 5% 1/20W MF 201
TPH501 A TP-P4
HDMI_5V_FAULT

UH502 FPF2495C CSP
VIN B1 A1
CRITICAL ON C3
VOUT A3 B3
ISET C2
OCFLAGB C1
GND B2 A2
HDMI_5V_ON
HDMI_5V_ISET
RH526 7.32K 1% 1/20W MF 201
OVERCURRENT PROTECTION

CRITICAL QH500 NTNS4CS69N XDFN
VTH=0.6-1.2V
376S1128 CHANGES TO 376S00282
PER <RDAR://59164333>
CEC_FLT — 89 86 B1
VOLTAGE=5V PP5V0_S2SW_HDMI_D
RH506 2.2K 5% 1/20W MF 201
RH505 2.2K 5% 1/20W MF 201
S/M_VER_1
RH507 0 5% 1/20W 0201 MF NOSTUFF
HDMI_CEC — B1 86 88

CAPACITANCE = 0.4PF
CLAMPING VOLTAGE = 7.0V
IEC 61000-4-2 ESD: +/-30KV (AIR), +/-25KV (CONTACT)
IEC 61000-4-4 EFT: 40A (5/50NS)
IEC 61000-4-5 SURGE: 5A (8/20US)

129 86 HDMI_CEC_CONN
CRITICAL LH504 FERR-470-OHM-215MA-1.5OHM 0201
CH504 22PF 5% 25V C0G 0201 NOSTUFF
RH509 33 5% 1/20W MF 201
HDMI_DDC_5V_FLT_SCL — HDMI_DDC_5V_SCL — IN 78 88

129 86 HDMI_DDC_5V_CONN_SCL
LH501 FERR-470-OHM-215MA-1.5OHM 0201 CRITICAL
CH505 18PF 5% 25V C0G 0201 NOSTUFF

129 86 HDMI_DDC_5V_CONN_SDA
LH502 FERR-470-OHM-215MA-1.5OHM 0201 CRITICAL
CH506 18PF 5% 25V C0G 0201 NOSTUFF
RH510 33 5% 1/20W MF 201
HDMI_DDC_5V_FLT_SDA — HDMI_DDC_5V_SDA — B1 78 88

129 86 HDMI_HPD_IN_CONN
LH503 FERR-470-OHM-215MA-1.5OHM 0201 CRITICAL
CH507 220PF 10% 25V X7R-CERM 201
RH511 0 5% 1/20W MF 0201
HDMI_HPD_IN_FLT — HDMI_HPD_IN — OUT 78 88 89

DZH503 ESD8011 X3DFN2-THICKSTNCL CRITICAL
DZH502 ESD8011 X3DFN2-THICKSTNCL CRITICAL
DZH501 ESD8011 X3DFN2-THICKSTNCL CRITICAL
DZH500 ESD8011 X3DFN2-THICKSTNCL CRITICAL

90 88 86 =PP3V3_S2SW_DP2HDMI
CH508 0.1UF 10% 6.3V CERM-X5R 0201
DATA_FILT
RH512 100K 5% 1/20W MF 201
PIND_PFET_EN
QH501 DMG1016V SOT-563 P-CHN CRITICAL
HDMI_PIND_VBIAS — OUT 87
RH513 10K 5% 1/20W MF 201
CH509 0.1UF 10% 6.3V CERM-X5R 0201
PIN DIODE VOLTAGE DROP = 0.8V
CURRENT PER DIODE:
(3.3V - 0.8V) / 1K = 2.5MA
CURRENT THROUGH 16 DIODES = 40MA
TIME FOR VOLTAGE TO DISCHARGE FROM 3.3V TO 0.8V USING 0.1UF AND 10K = 1.4MS

DP2HDMI_1.5G_FILT_EN	PIN DIODE	FILTER
LOW	UNBIASED	6GBPS
HI	BIASED	1.5GBPS

88 IN DP2HDMI_1.5G_FILT_EN
RH514 100K 5% 1/20W MF 201
N-CHN
QH501 DMG1016V SOT-563
VTH = 0.5V - 1V MAX
CRITICAL

=PP3V3_S2SW_DP2HDMI 86 88 90
DH504 X3DFN2-THICKSTNCL NSR01L30MXT5G
CEC_FLT_PULL
RH515 27K 5% 1/20W MF 201
CEC_FLT 86 89 129
NOSTUFF RH516 10M 5% 1/20W MF 201

=PP3V3_S2SW_DP2HDMI 86 88 90
DH505 NSR0620P2XXG SOD-923-HF
HDMI_CEC_PULL
RH517 3.0M 1% 1/20W MF 0201
HDMI_CEC 86 88
NOSTUFF RH518 10M 5% 1/20W MF 201

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: CONNECTOR

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*** OK2INTEGRATE***

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

NOTE:
TERMINATION R INTEGRATED IN PCON.
NO EXT. TERMINATION NEEDED.

0.5PF CAP AND 8.2OHM RESISTORS ARE BASED ON EMPIRICAL TESTING WITH MEGACHIPS TO IMPROVE INTEROPERABILITY

ESD DIODE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377S00185	4	TVS,DIODE,BIDIR,5.5V,0.2PF,0201	DZH600,DZH601,DZH604,DZH607	
377S00185	4	TVS,DIODE,BIDIR,5.5V,0.2PF,0201	DZH608,DZH611,DZH612,DZH615	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S0724	2	0.00 OHM 0201 RES	LH600,LH601	NO_CFILT
152S1073	2	8.2UH 0201 IND	LH600,LH601	CLK_FILT
118S0724	4	0.00 OHM 0201 RES	LH603,LH604,LH606,LH607	NO_DFILT
118S0724	2	0.00 OHM 0201 RES	LH609,LH610	NO_DFILT
152S2036	4	2.5UH 0201 IND	LH603,LH604,LH606,LH607	DATA_FILT
152S2036	2	2.5UH 0201 IND	LH609,LH610	DATA_FILT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S00196	377S00185		ALL	
371S00047	371S00322		ALL	

FILTER APN NUMBERS
0.2PF: 131S0431
3.0PF: 131S0439
4.0PF: 131S0597
3.0NH: 152S2045
CMCC: 155S0897
PIN DIODE: 271S0047
ESD DIODE: 377S0178

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: DESENSE FILTERS

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*** OK2INTEGRATE***
=PP3V3_S2SW_DP2HDMI
PP3V3_DP2HDMI_AUX_IO
VOLTAGE=3.3V (TBD MA)
PP3V3_DP2HDMI_RX_TX
PP1V8_MIXEDIO_VDD
PP1V2_DP2HDMI_TX_RX_PLL_OSC
VOLTAGE=1.2V (TBD MA)
=PP1V2_S2_DP2HDMI
=PP1V8_S2SW_DP2HDMI
FOR 1.8V I/O:
MIXEDIO_VDD = 1.8V
MIXEDIO_CONFIG = 3.3V
FOR 3.3V I/O:
MIXEDIO_VDD = 3.3V
MIXEDIO_CONFIG = GND
CRITICAL
OMIT_TABLE
UH700
MCDP2920A4
BGA
PU SETS ADDR TO C0H/C1H
JX74:CONNECTED TO PMU GPIO
J31X:NOT CONNECTED
CA881/2 per desense team request
(SPDIF_GPIO PU: DP_HPD FOLLOWS HDMI_HPD)
(SPDIF_GPIO PD: DP_HPD ALLOWS ASSERTED)
(27K PU AT CONNECTOR)
(1.8V LEVEL)
NET/TP NOT USED ON POR PROGRAMS
MUST ONLY BE OPEN-DRAIN!
Make sure no SOC backpower
(SPI_WP PU FOR 27MHZ OSC)
(SPI_WP PD FOR 24MHZ OSC)
UH701
8MBIT-1.8V
W25Q80EWUXIE
USON
OMIT_TABLE
CRITICAL
197S00109
CRITICAL
YH700
2.50X2.00MM-SM
27MHZ-10PPM-18PF
NOTE:
REQUIREMENTS FOR SPI FLASH
-SUPPORTS FAST READ WITH CMD 08H.
-ERASABLE IN 64K BYTE BLOCKS.

NOTE: MAIN LINK RX IS INTERNALLY TERMINATED TO 1.2V RAIL VIA 50 OHM.
* IN NORMAL MODE, OCM BOOTS FROM INTERNAL ROM.
* PCON COVERS CHAR CLOCK RANGES FROM 25MHZ TO 600MHZ.
* VDD12_ON IS ASSERTED UPON DETECTING AUX FROM A DP SOURCE OR HPD FROM AN HDMI SINK.

CONVERTER MODE:	600MW
SLEEP STATE:	15MW
CS POWER STATE: (TCLK_OFF)	5MW
CS POWER STATE: (VDD12_OFF)	0.1MW

UART (MAX) = 115.2KBPS
I2C (MAX) = 1MBPS (50KBPS)
SPI (MAX) = 75MHZ
INTERNAL OCM CK = 150MHZ
HDMI OUTPUT: 0.25 - 6.0 GBPS

HDMI_TX:
VSWING: 0 - 1200MV
PEMP: 0 - 5DB
DDC = 1 - 100KBPS

1V2	350MA TYPICAL
1V8	5MA TYPICAL
3V3	50MA TYPICAL

BOM_COST_GROUP=HDMI

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
197S00113	197S00109	YH700	CRYSTAL	

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HDMI: MADEA

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*** IN PROGRESS ***

From SOC

LPDP AC Caps

To HDMI

140	IN	DPRX_INT_DATA_C_N<0>	CH820 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<0>	OUT	88
140	IN	DPRX_INT_DATA_C_P<0>	CH821 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<0>	OUT	88
140	IN	DPRX_INT_DATA_C_N<1>	CH822 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<1>	OUT	88
140	IN	DPRX_INT_DATA_C_P<1>	CH823 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<1>	OUT	88
140	IN	DPRX_INT_DATA_C_N<2>	CH824 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<2>	OUT	88
140	IN	DPRX_INT_DATA_C_P<2>	CH825 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<2>	OUT	88
140	IN	DPRX_INT_DATA_C_N<3>	CH826 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<3>	OUT	88
140	IN	DPRX_INT_DATA_C_P<3>	CH827 0.1UF	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<3>	OUT	88
140	BI	DPRX_INT_AUX_C_N	CH828 0.1UF	10% 6.3V CERM-X5R 0201	DPRX_AUX_N	BI	78 88
140	BI	DPRX_INT_AUX_C_P	CH829 0.1UF	10% 6.3V CERM-X5R 0201	DPRX_AUX_P	BI	78 88

129 43 IN HDMI_RESET_L — RH801 0 5% 1/20W MF 0201 — HDMI_RESET_R_L OUT 78 88

HDMI ROM BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S00049	1	MADEA SPI FLASH,8MB,1.8V,8P,USON	UH701	HDMI_ROM:BLANK
341S01592	1	IC,HDMI ROM,FW V1.130,X1814	UH701	HDMI_ROM:FW_V1P130
341S01701	1	ROM,HDMI (VKXX),PROTO-0,X2737	UH701	HDMI_ROM:PROTO0

HDMI 1V2 VR

1V2 S2 @ 0.4A

VR:0.5A CONTINUOUS, 0.8A PEAK

LEVEL SHIFTERS

90 89 88 =PP1V2_S2_DP2HDMI — CH842 0.1UF 10% 6.3V CERM-X5R 0201 — RH822 47K 1% 1/20W MF 201

88 90 =PP1V8_S2SW_DP2HDMI — CH841 0.1UF 10% 6.3V CERM-X5R 0201

UH840 SN74AXC1T45 SOT-5X3 (VCCA, VCCB, DIR, A, B, GND)

10 IN SPI_DP2HDMI_HOLD_L — SPI_DP2HDMI_HOLD_L_1V8 OUT 78 88

78 88 IN DPRX_INT_HPD_1V8 — RH811 100K 5% 1/20W MF 201

1.8V => 1.2V LS

90 89 88 =PP1V2_S2_DP2HDMI — CH840 0.1UF 10% 6.3V CERM-X5R 0201

UH800 SN74AUP1G17 SON (VCC, GND, NC, NC) — NC NC

DPRX_INT_HPD — RH812 10K 5% 1/20W MF 201 — DPRX_INT_HPD OUT 142

135 =PP3V3_S2_HDMI_HPD — CH802 0.1UF 10% 10V X5R-CERM 0201

UH802 74LVC1G07 SOT886 (VCC, GND)

88 86 78 IN HDMI_HPD_IN — NC NC NC NC

135 89 =PP1V2_S2_HDMI_HPD — NOSTUFF RH803 47K 1% 1/20W MF 201

RH804 100 1% 1/20W MF 201 — HDMI_HPD_AOP OUT 10 130

135 89 =PP1V2_S2_HDMI_HPD — CH801 0.1UF 10% 10V X5R-CERM 0201

RH815 47K 1% 1/20W MF 201

129 10 IN HDMI_CEC_AOP_TX — RH806 0 5% 1/20W MF 0201 — AOP_HDMI_CEC_R

UH801 74AUP2G07GM SOT886 (VCC, GND, 1A, 1Y, 2A, 2Y)

CEC_FLT_R — RH810 187 1% 1/20W MF 201 — CEC_FLT BI 86 129

RH816 27K 5% 1/20W MF 201

HDMI_AOP_CEC_R — 100 1% 1/20W MF 201 — HDMI_CEC_AOP_RX OUT 10 129

RH805

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0341	311S0536		UH802	RDAR://64195790

UH801 IS UPDATED TO 311S00279 PER RDAR://63399828
J31X HAS ADOPTED THIS NEW PART

1V2 S2 @ 350MA LOAD

ALTERNATE PART FOR UH850 IS 353S02127
PLEASE ADD TO ALT PARTS LIST

99 =PP1V8_S2_P1V2_IN — PACK_OPTION=HDMI_LDO:ON-SEMI

PACK_OPTION=HDMI_LDO:ON-SEMI — RH851 0 5% 1/20W MF 0201

135 =PP5V_S2_BIAS — RH852 510 5% 1/20W MF 201

PACK_OPTION=HDMI_LDO:ON-SEMI — UH850_BIAS

CH853 1UF 10% 10V X5R 402-1 — CH851 0.1UF 10% 10V X6S-CERM 0201 — CH852 4.7UF 20% 10V X5R-CERM 0402

PACK_OPTION=HDMI_LDO:ON-SEMI

UH850 SCY99247CFCS120 WLCSP-COMBO VER-1 CRITICAL (VIN, VOUT, EN, VBIAS, SNS, GND, A2, B2, C2, A1, B1, C1)

UH850_EN

UH850_FB

PACK_OPTION=HDMI_LDO:ON-SEMI — =PP1V2_S2_DP2HDMI_REG

RH853 0 5% 1/20W MF 0201 — CH854 120PF 10% 25V X7R 0201 NOSTUFF — CH850 10UF 20% 10V X5R-CERM 0402-7

PACK_OPTION=HDMI_LDO:ON-SEMI — NOSTUFF RH854 0 5% 1/20W MF 0201 — PACK_OPTION=HDMI_LDO:ON-SEMI

PACK_OPTION=HDMI_LDO:ON-SEMI

LDO: 0.7A MAX

THE LDO IS A CHEAPER PART COMPARED TO TI PART

BOM_COST_GROUP=HDMI

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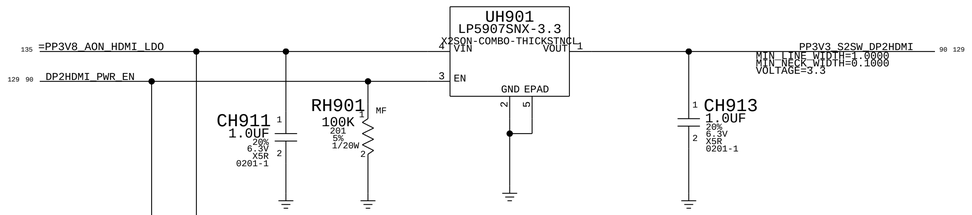
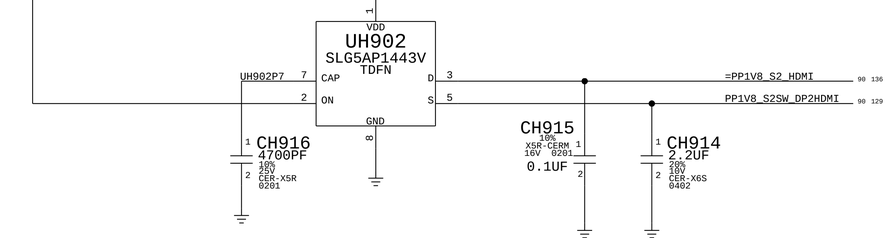
3.3V LDO



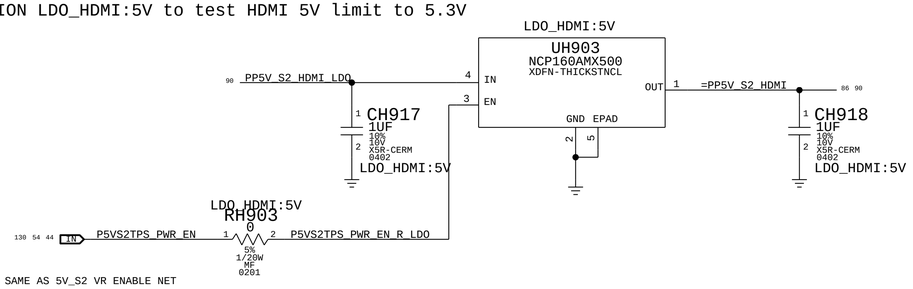
1.8V LOAD SW



THIS IS USED FOR LONGER 5V POWER PATHS TO ENSURE GOOD 5V REGULATION

Enable BOMOPTION LDO_HDMI:NONE to disable the LDO use

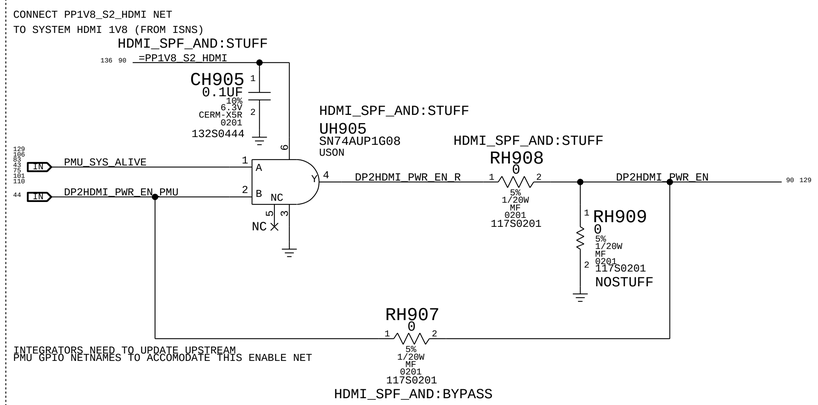
Enable BOMOPTION LDO_HDMI:5V to test HDMI 5V limit to 5.3V



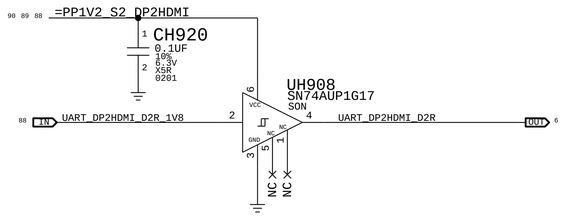
PWR_EN SHOULD BE SAME AS 5V_S2 VR ENABLE NET

THIS IS USED FOR CONTROLLING HDMI PORT POWER VIA THE PMU SYS ALIVE NET

USE THE BYPASS BOMOPTION TO NOT STUFF THESE
OR NO STUFF ALL OF THESE FOR DESKTOPS

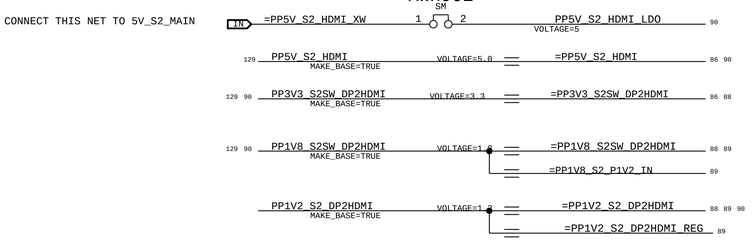


RH908/RH909 intended for potential
resistor divider need after AND gate



PLACE_NEAR=UH903:10mm

CONNECT THIS NET TO 5V_S2_MAIN



PAGE TITLE
HDMI: Project Support 2

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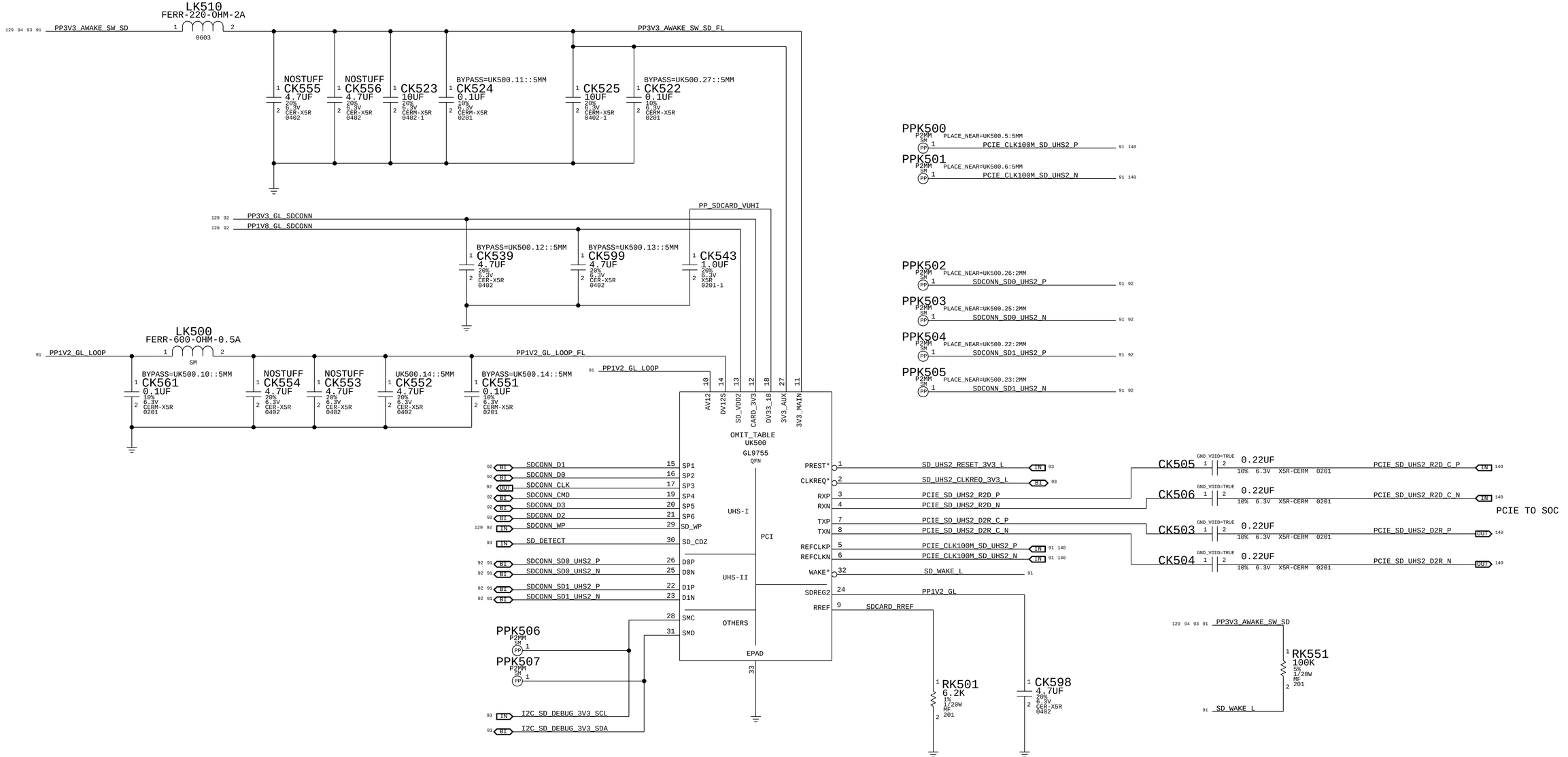

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00729	1	IC,GL9755A,REV5A,SCREENED	UK500	CRITICAL	SD:REV5
338S00755	1	IC,GL9755A,REV6	UK500	CRITICAL	SD:REV6

REV6 TO BE USED WHEN AVAILABLE, FIXES PCIE INSTABILITY

BOM_COST_GROUP=SDCARD

PAGE TITLE: SDCARD CONTROLLER

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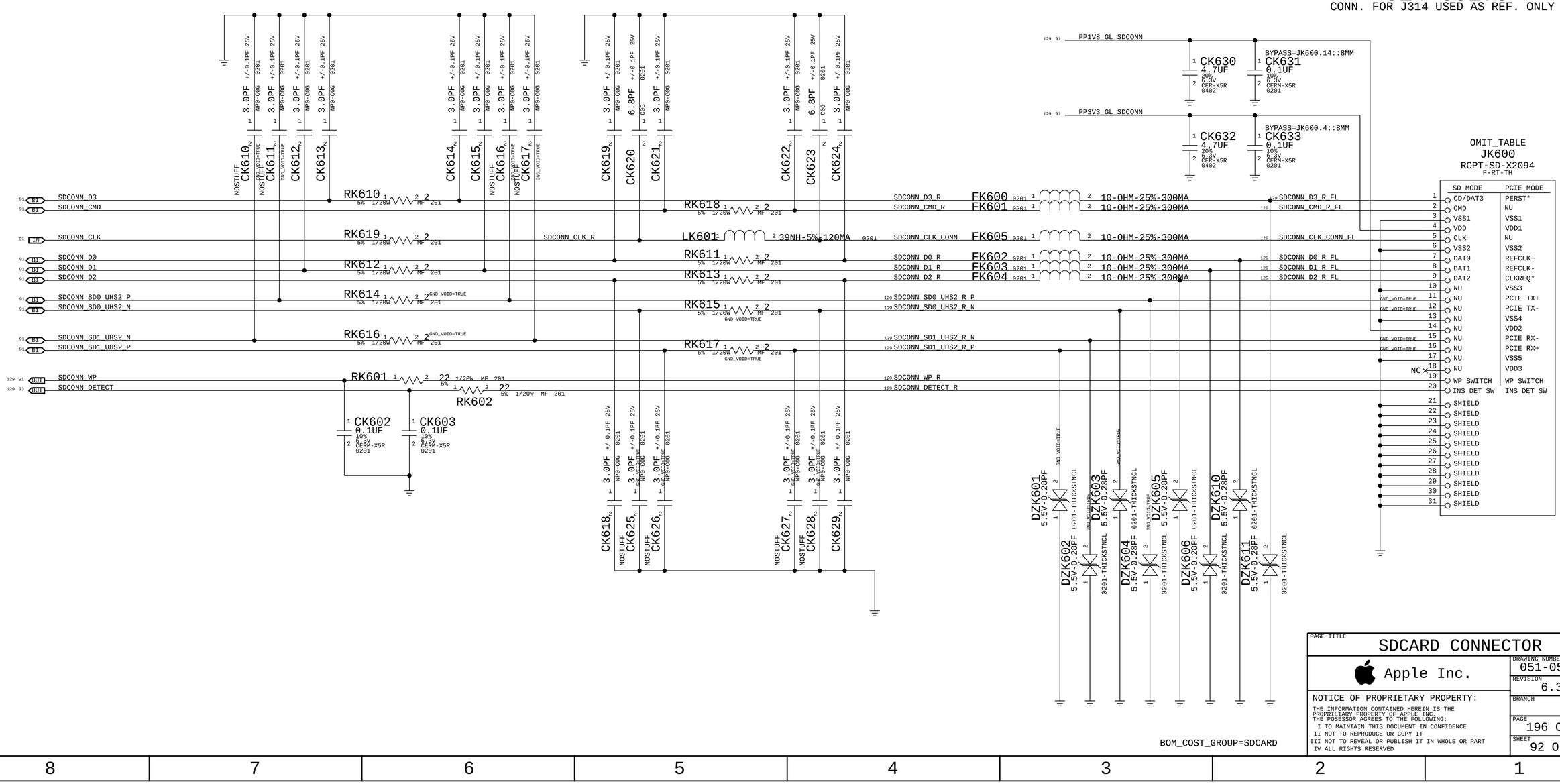
SD CARD CONNECTOR
514-00175
CONN. FOR J314 USED AS REF. ONLY



PAGE TITLE
SDCARD CONNECTOR

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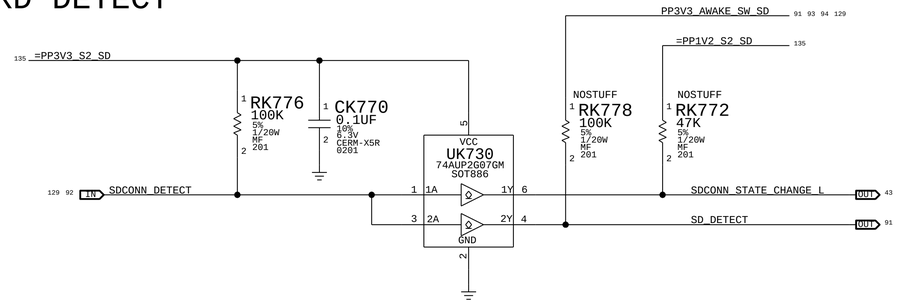
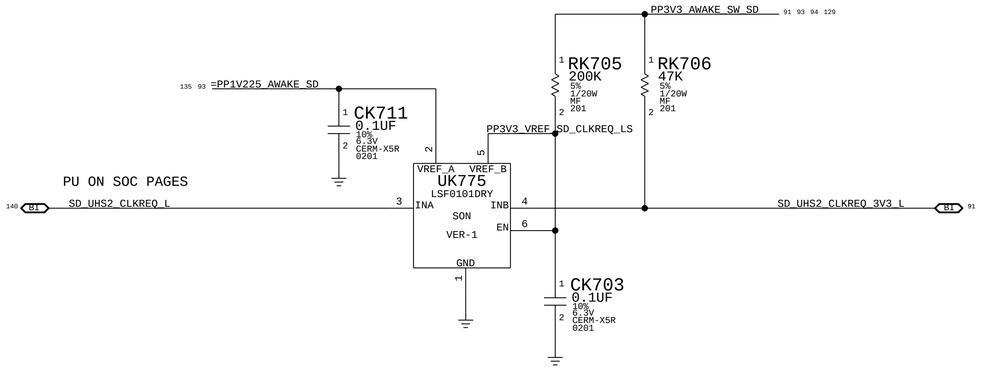
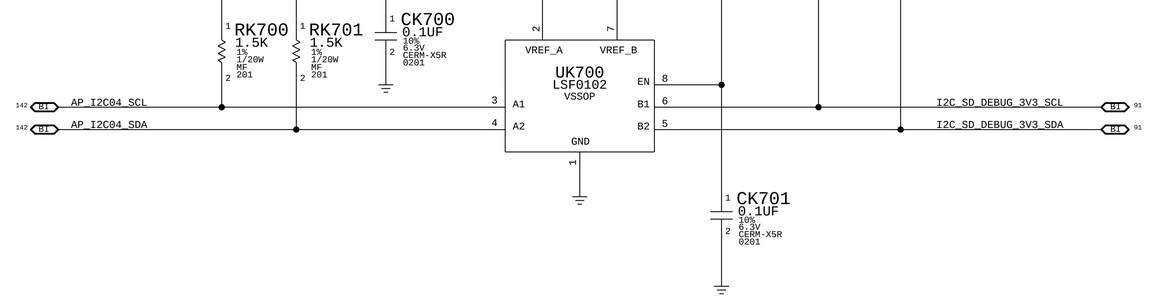
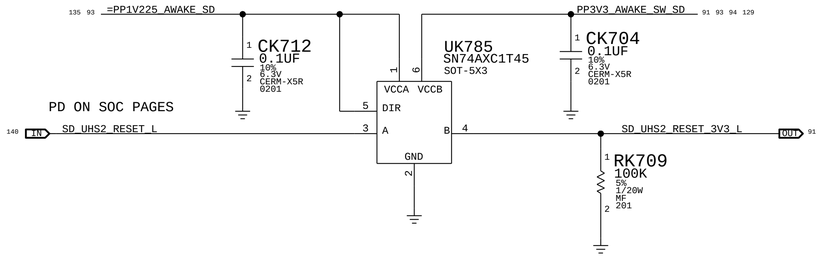
CARD DETECT



CONTROLLER IO







BOM_COST_GROUP=SDCARD

PAGE TITLE: SDCARD IO LS/BUF SUPPORT

Apple Inc.

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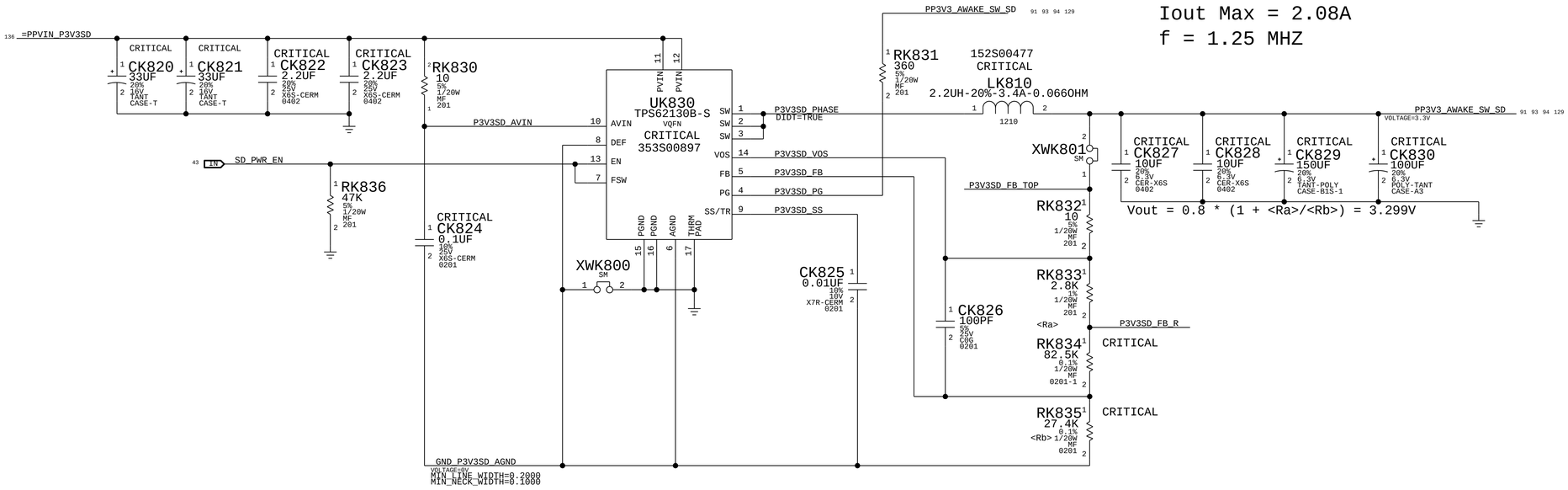

BOM_COST_GROUP=SDCARD

PAGE TITLE
SDCARD POWER SUPPORT

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*** IN PROGRESS ***

FOR SYSTEM INTEGRATION INFORMATION REFER TO
RDAR://PROBLEM/59047597

TYPHOON WIFI/BT MODULE

PLACE_NEAR=UL000.48:4MM
PLACE_NEAR=UL000.48:3MM
PLACE_NEAR=UL000.48:3MM =PP3V8_AON_WLBT 95 136
CL005 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL030 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CL020 12PF 5% 25V NP0-C0G 0201
VBAT

PLACE_NEAR=UL000.14:4MM
PLACE_NEAR=UL000.14:3MM
PLACE_NEAR=UL000.14:3MM =PP3V8_AON_WLBT 95 136
CL006 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL031 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CL021 12PF 5% 25V NP0-C0G 0201
2GFEM

PLACE_NEAR=UL000.38:4MM
PLACE_NEAR=UL000.38:3MM
PLACE_NEAR=UL000.38:3MM =PP3V8_AON_WLBT 95 136
CL007 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL032 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CL022 12PF 5% 25V NP0-C0G 0201
5GFEM_C0

PLACE_NEAR=UL000.76:4MM
PLACE_NEAR=UL000.76:3MM
PLACE_NEAR=UL000.76:3MM =PP3V8_AON_WLBT 95 136
CL008 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL033 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL CL023 12PF 5% 25V NP0-C0G 0201
5GFEM_C1

PLACE_NEAR=UL000.23:4MM
PLACE_NEAR=UL000.23:3MM =PP1V8_S2_WLBT 95 135
CL010 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL CL024 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.4:4MM
PLACE_NEAR=UL000.4:3MM =PP1V8_S2_WLBT 95 135
CL011 10UF 20% 10V X5R-CERM 0402-8
CRITICAL CL025 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.33:4MM
PLACE_NEAR=UL000.33:3MM =PP1V8_S2_WLBT 95 135
CL012 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL CL034 3.0PF +/-0.1PF 25V NP0-C0G 0201
5GFEM_C0

PLACE_NEAR=UL000.82:4MM
PLACE_NEAR=UL000.82:3MM =PP1V8_S2_WLBT 95 135
CL013 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL CL035 3.0PF +/-0.1PF 25V NP0-C0G 0201
5GFEM_C1

=PP1V8_S2_WLBT 135 95
=PP3V8_AON_WLBT 136 95
=PP1V2_S2_WLBT_IO 136
PLACE_NEAR=UL000.51:4MM
CL014 0.1UF 10% 6.3V CERM-X5R 0201

UL000
2103-601908-80
LGA
SYM 1 OF 4
OMIT_TABLE

96	BI	RF_ANT_0	NO_TEST=1	28	ANT_X
96	BI	RF_ANT_1	NO_TEST=1	87	ANT_Y
96	BI	RF_BT_DED	NO_TEST=1	72	BT_DEDICATED
		NC_BT_GPIO_2	NO_TEST=1	431	BT_GPIO_2
130 96 95 6	OUT	BT_TIME_SYNC		36	BT_GPIO_3
		NC_BT_GPIO_4	NO_TEST=1	43	BT_GPIO_4
		NC_BT_GPIO_5	NO_TEST=1	128	BT_GPIO_5
95 13	IN	SPMI_WLBT_CLK		119	SPMI_HEB_CLK
95 13	BI	SPMI_WLBT_DATA		321	SPMI_HEB_DAT
95		BT_LHL_GPIO2		136	LHL_GPIO2
		NC_SPMI_IDC_CLK		120	SPMI_IDC_CLK
		NC_SPMI_IDC_DATA		343	SPMI_IDC_DAT
130 96 95 44 43	IN	WLBT_PWR_EN		41	WLBT_REG_ON
130 96 95 44	IN	PMU_CLK32K_WLBT		515	WLBT_CLK_32K
95		WLAN_JTAG_SEL		54	JTAG_SEL
		RL002 10K 5% 1/20W MF 201		497	SFLASH_OPTION_2

TYPHOON ES2.X

		WL_GPIO_0		126	WLBT_WAKE
		WL_GPIO_2		388	TPT_WLAN_JTAG_TCK
		WL_GPIO_3		410	TPT_WLAN_JTAG_TMS
		WL_GPIO_4		500	TPT_WLAN_JTAG_TDI
		WL_GPIO_5		501	WLAN_TIME_SYNC
		WL_GPIO_6		366	TPT_WLAN_JTAG_TRSTN
		WL_GPIO_7		137	WL_GPIO_7
		WL_GPIO_8		151	UART_WLAN_R2D_R
		WL_GPIO_9		150	UART_WLAN_D2R_R
		WL_GPIO_10		498	UART_WLAN_R2D_RTS_L_R
		WL_GPIO_11		499	UART_WLAN_D2R_CTS_L_R
		WL_GPIO_12	NO_TEST=1	453	NC_WL_GPIO_12
		WL_GPIO_13	NO_TEST=1	160	NC_WL_GPIO_13
		WL_GPIO_14	NO_TEST=1	159	NC_WL_GPIO_14
		WL_GPIO_15	NO_TEST=1	475	NC_WL_GPIO_15
		WL_GPIO_16	NO_TEST=1	513	NC_WL_GPIO_16
		WL_GPIO_18	NO_TEST=1	512	NC_WL_GPIO_18
		WL_GPIO_19	NO_TEST=1	476	NC_WL_GPIO_19
		WLBT_PCIE_PERST_L		505	WLBT_RESET_L
		WLBT_PCIE_CLKREQ_L		508	WLBT_CLKREQ_R_L
		WLBT_PCIE_RXD_P		145	PCIE_WLBT_R2D_P
		WLBT_PCIE_RXD_N		146	PCIE_WLBT_R2D_N
		WLBT_PCIE_TXD_P		142	PCIE_WLBT_D2R_C_P
		WLBT_PCIE_TXD_N		143	PCIE_WLBT_D2R_C_N
		WLBT_PCIE_REFCLK_P		139	PCIE_CLK100M_WLBT_P
		WLBT_PCIE_REFCLK_N		140	PCIE_CLK100M_WLBT_N

0201 ME 1/10W 2 5% 0.00 RL005 UART_WLAN_R2D IN 6
0201 ME 1/10W 2 5% 0.00 RL006 UART_WLAN_D2R OUT 6
0201 ME 1/10W 2 5% 0.00 RL007 UART_WLAN_R2D_RTS_L IN 6
0201 ME 1/10W 2 5% 0.00 RL008 UART_WLAN_D2R_CTS_L OUT 6

TPL001 A 1 TP-P5 PMU_CLK32K_WLBT 44 95 96 130
TPL002 A 1 TP-P5 WLBT_PWR_EN 43 44 95 96 130
TPL003 A 1 TP-P5 WLBT_WAKE 43 95 96
TPL004 A 1 TP-P5 TPT_WLAN_JTAG_TCK 95 96 130
TPL005 A 1 TP-P5 TPT_WLAN_JTAG_TMS 95 96 130
TPL006 A 1 TP-P5 TPT_WLAN_JTAG_TDI 95 130
TPL007 A 1 TP-P5 WLAN_TIME_SYNC 6 95 96
WLAN_JTAG_TDO
TPL008 A 1 TP-P5 TPT_WLAN_JTAG_TRSTN 95 130
TPL009 A 1 TP-P5 WLAN_JTAG_SEL 95
TPL010 A 1 TP-P5 BT_TIME_SYNC 6 95 96 130
TPL011 A 1 TP-P5 UART_WLAN_R2D_R 95
TPL012 A 1 TP-P5 UART_WLAN_D2R_R 95
TPL013 A 1 TP-P5 UART_WLAN_R2D_RTS_L_R 95
TPL014 A 1 TP-P5 UART_WLAN_D2R_CTS_L_R 95

TPL018 A 1 TP-P5 SPMI_WLBT_CLK 13 95
TPL019 A 1 TP-P5 SPMI_WLBT_DATA 13 95
TPL020 A 1 TP-P5 BT_LHL_GPIO2 95
PPL021 P2MM SM PP 1 PCIE_CLK100M_WLBT_P 8 95
PLACE_SIDE=BOTTOM
PPL022 P2MM SM PP 1 PCIE_CLK100M_WLBT_N 8 95
PLACE_SIDE=BOTTOM
TPL023 A 1 TP-P5 WLBT_RESET_L 8 95 96 130
PLACE_SIDE=BOTTOM
TPL024 A 1 TP-P5 WLBT_CLKREQ_L 8 95 96
PLACE_SIDE=BOTTOM
TPL025 A 1 TP-P5 WL_GPIO_7 95
PACK_OPTION=WLBT_D2R_TP_JADE
PLACE_NEAR=U0600.A41:10MM
PPL026 P2MM SM PP 1 PCIE_WLBT_D2R_P 8 95
PLACE_SIDE=BOTTOM
PACK_OPTION=WLBT_D2R_TP_JADE
PLACE_NEAR=U0600.B41:10MM
PPL027 P2MM SM PP 1 PCIE_WLBT_D2R_N 8 95
PLACE_SIDE=BOTTOM

GND_VOID=TRUE
PLACE_NEAR=UL000.145:4MM
PCIE_WLBT_R2D_C_P 8 IN — CL001 0.1UF 10% 6.3V CERM-X5R 0201 — PCIE_WLBT_R2D_P 95
PCIE_WLBT_R2D_C_N 8 IN — CL002 0.1UF 10% 6.3V CERM-X5R 0201 — PCIE_WLBT_R2D_N 95
PLACE_NEAR=UL000.146:4MM
GND_VOID=TRUE

SPMI_WLBT_CLK 95 13 — RL003 51K 1/20W 5% MF 201
SPMI_WLBT_DATA 95 13 — RL004 51K 1/20W 5% MF 201

PACK_OPTION=WLBT_D2R_TP_JADE
PLACE_NEAR=UL000.142:4MM
GND_VOID=TRUE
PCIE_WLBT_D2R_C_P 95 — CL003 0.1UF 10% 6.3V CERM-X5R 0201 — PCIE_WLBT_D2R_P OUT 8 95
PCIE_WLBT_D2R_C_N 95 — CL004 0.1UF 10% 6.3V CERM-X5R 0201 — PCIE_WLBT_D2R_N OUT 8 95
PLACE_NEAR=UL000.143:4MM
PACK_OPTION=WLBT_D2R_TP_JADE
GND_VOID=TRUE

PACK_IGNORE=TRUE
PACK_OPTION=WLBT_D2R_TP_STATEN
PLACE_NEAR=U0600.BF29:10MM
GND_VOID=TRUE
PCIE_WLBT_D2R_C_P 95 — CL043 0.1UF 10% 6.3V CERM-X5R 0201 — PCIE_WLBT_D2R_P 8 95
PCIE_WLBT_D2R_C_N 95 — CL044 0.1UF 10% 6.3V CERM-X5R 0201 — PCIE_WLBT_D2R_N 8 95
GND_VOID=TRUE
PLACE_NEAR=U0600.BG29:10MM
PACK_IGNORE=TRUE
PACK_OPTION=WLBT_D2R_TP_STATEN

WLBT_CLKREQ_R_L 95 — RL001 1K 1/20W 5% MF 201 — WLBT_CLKREQ_L BI 8 95 96

BOM_COST_GROUP=WIRELESS

TYPHOON BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00813	1	MODULE,WLAN/BT,TYPHOON, ES2.5	UL000	CRITICAL	

TYPHOON ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00858	339S00813	ANY	UL000	TYPHOON ES2.7
339S00859	339S00813	ANY	UL000	TYPHOON ES2.9
339S00863	339S00813	ANY	UL000	TYPHOON ES4.1

PAGE TITLE: WIFI/BT: MODULE

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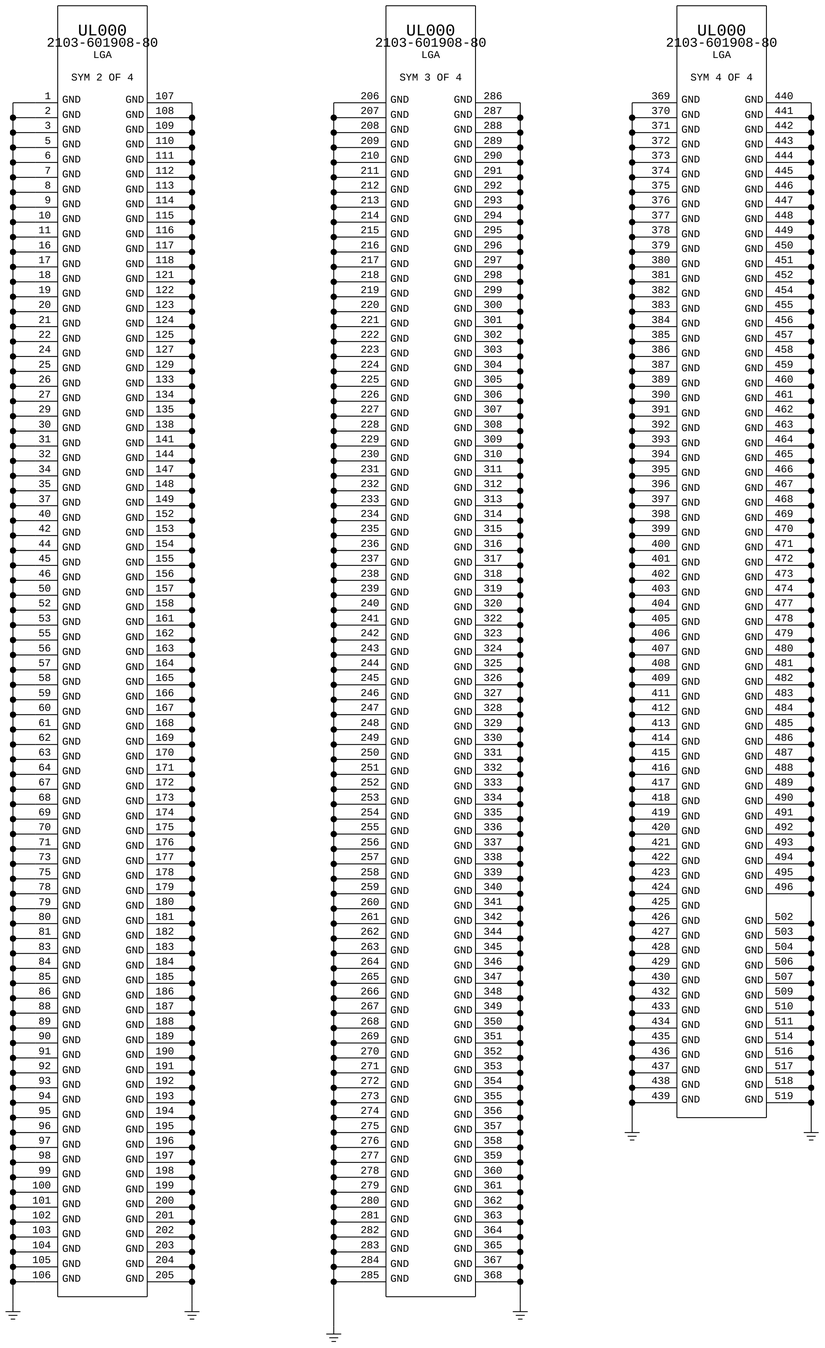
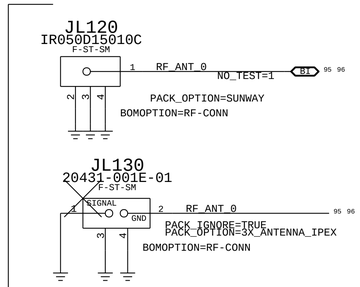
*** IN PROGRESS ***

TYPHOON WIFI/BT MODULE GND

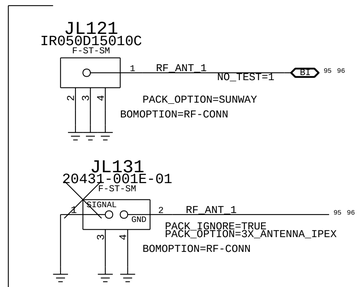


ANTENNA CONNECTORS

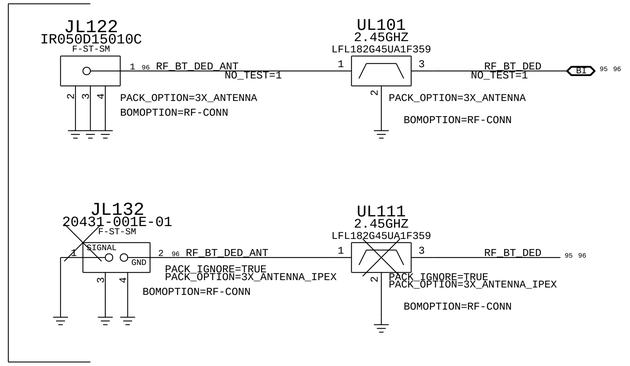
2G_C0
5G_C0
BT_C0



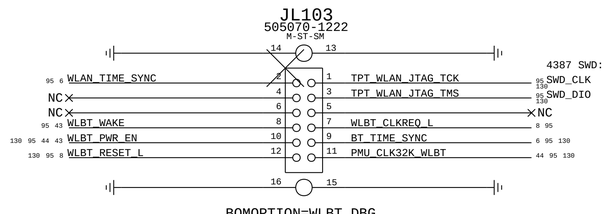
2G_C1
5G_C1
BT_C1



BT_C1_DED



WLBT DEBUG CONNECTOR



BOM_COST_GROUP=WIRELESS

PAGE TITLE: WIFI/BT: ANTENNA and GND

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*** OK2INTEGRATE ***

NAND0 S5E0

=PP0V9_NAND0_S5E0 — CN010 20UF 20% 10V X5R 0402; CN011 20UF 20% 10V X5R 0402; CN012 2.2UF 20% 10V X5R 0201; CN013 2.2UF 20% 10V X5R 0201; CN014 2.2UF 20% 10V X5R 0201; CN015 0.1UF 10% 6.3V CERM-X5R 0201; CN016 0.1UF 10% 6.3V CERM-X5R 0201; CN017 0.1UF 10% 6.3V CERM-X5R 0201

=PP1V2_NAND0 — CN032 20UF 20% 10V X5R 0402; CN030 4.3UF 20% 4V CERM 0402-THICKSTNCL; CN034 2.2UF 20% 10V X5R 0201; CN035 2.2UF 20% 10V X5R 0201; CN036 2.2UF 20% 10V X5R 0201; CN037 2.2UF 20% 10V X5R 0201; CN038 2.2UF 20% 10V X5R 0201; CN039 2.2UF 20% 10V X5R 0201; CN03A 2.2UF 20% 10V X5R 0201

=PP2V5_NAND0 — CN020 20UF 20% 10V X5R 0402; CN022 2.2UF 20% 10V X5R 0201; CN023 2.2UF 20% 10V X5R 0201; CN024 2.2UF 20% 10V X5R 0201; CN025 2.2UF 20% 10V X5R 0201

TP_NAND0_S5E0_ANI1_VREF

TP_NAND0_S5E0_ANI0_VREF

=PP1V2_NAND0 — RN010 2 1% 1/20W MF 0201 PLACE_NEAR=UN000.L2:10MM

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V

PP1V2_NAND0_S5E0_AVDD1X_PLL — CN047 2.2UF 20% 10V X5R 0201; CN046 0.1UF 10% 6.3V CERM-X5R 0201

FLN000 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN000.J6:20MM

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V

PP1V2_NAND0_S5E0_PCI_AVDD_H — CN045 4.7UF 20% 4V CER-X5R 0201; CN044 0.1UF 10% 6.3V CERM-X5R 0201

The inductance from CN047, CN046, CN045, CN044 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V

PP0V9_NAND0_S5E0_VDD_PLL

FLN001 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN000.R4:20MM

=PP0V9_NAND0_S5E0 — CN083 4.7UF 20% 4V CER-X5R 0201 PLACE_NEAR=FLN001.2:5MM

TP_NAND0_S5E0_VPP

Ball	Net
J6	PCIE_AVDD_H
J8	PCIE_VDD
M9	PCIE_VDD
N6	PCIE_VDD
N8	PCIE_VDD
L2	AVDDIX_PLL
G12	ANI0_VREF
J4	ANI1_VREF
G6	VDD
G8	VDD
L6	VDD
L8	VDD
R6	VDD
R8	VDD
J2	VDDIO_1
K9	VDDIO_1
T5	VDDIO_1
E10	VDDIO_2
E2	VDDIO_2
N2	VDDIO_2
P9	VDDIO_2
D3	VCC
E12	VCC
G4	VCC
L12	VCC
R2	VCC
R4	VDD_PLL
F3	VPP
F5	VQPS

OMIT_TABLE

UN000 S5E-MCP-STUDY-2TB LGA

CN085 10PF 5% 25V C0G 0201; RN004 200 0.1% 1/20W TF 0201-1

NAND0_CLK24M_0	M3	CLK_IN	
PCIE_CLK100M_NAND0_0_P	K11	PCIE_REFCLK_P	
PCIE_CLK100M_NAND0_0_N	J12	PCIE_REFCLK_N	
NAND0_CLKREQ0_R_L	P5	PCIE_CLKREQ*	
NAND0_S5E0_PCIE_RESREF	H7	PCIE_RESREF	
PCIE_NAND0_R2D_C_P<0> — CN003 0.22UF	M11	PCIE_RX0_P	
PCIE_NAND0_R2D_C_N<0> — CN004 0.22UF	N12	PCIE_RX0_N	
PCIE_NAND0_D2R_P<0> — CN001 0.22UF	R12	PCIE_TX0_P	
PCIE_NAND0_D2R_C_N<0> — CN002 0.22UF	T11	PCIE_TX0_N	
NAND0_RESET_L	L4	RESET*	
NAND0_JTAG_TRST_L	G10	TRST*	
NAND0_S5E0_ZQ_0	C10	ZQ_0	
NAND0_S5E0_ZQ_1	K3	ZQ_1	

PLACE_NEAR=UN000.C10:15MM RN006 300 1% 1/20W MF 201

PLACE_NEAR=UN000.K3:15MM RN005 300 1% 1/20W MF 201

Ball	Net
A12	VSS
A2	VSS
B13	VSS
C12	VSS
C2	VSS
D1	VSS
D13	VSS
F1	VSS
F11	VSS
F13	VSS
F7	VSS
F9	VSS
H1	VSS
H11	VSS
H13	VSS
H3	VSS
H5	VSS
H9	VSS
J10	VSS
K1	VSS
K13	VSS
K5	VSS
K7	VSS
L10	VSS
M1	VSS
M13	VSS
M5	VSS
M7	VSS
N10	VSS
N4	VSS
P1	VSS
P11	VSS
P13	VSS
P3	VSS
P7	VSS
R10	VSS
T1	VSS
T13	VSS
T7	VSS
T9	VSS
U12	VSS
U2	VSS
A10	VSS_R
A4	VSS_R
A6	VSS_R
A8	VSS_R
U10	VSS_R
U4	VSS_R
U6	VSS_R
U8	VSS_R

Ball	Net
B3	EXT_D0/BOOT0 — NAND0_LPB_L
C4	EXT_D1/BOOT1 — NAND_BFH
B5	EXT_D2/BOOT2/SPINAND_SCLK — NAND0_BOOT2
C6	EXT_D3/SWD_UID0/SPINAND_MISO — NAND0_S5E0_SWD_UID0
B7	EXT_D4/SPI_CS
C8	EXT_D5/SWD_UID1/SPINAND_MOSI — NAND0_S5E0_SWD_UID1
B9	EXT_D6/BOOT3
B11	EXT_D7/SPF — NAND0_PFN_L
D11	EXT_DQS/BCM* — NAND0_BCM_L
E8	EXT_NCE/PERST* — NAND0_PCIE_RESET_L
D7	EXT_NRE/JTAG_TMS — SWD_NAND0_S5E0_SWDIO
E6	EXT_NWE/JTAG_TCK — SWD_NAND0_S5E0_SWCLK
E4	EXT_RNB/JTAG_TDO — NAND0_S5E0_JTAG_TDO
D5	EXT_CLE/JTAG_TDI — TP_NAND0_S5E0_JTAG_TDI
D9	EXT_ALE/JTAG_SEL — NAND0_JTAG_SEL
T3	DROOP* — TP_NAND0_S5E0_DROOP_L
G2	WP* — NAND0_WP_L

NAND0_BOOT2

NAND0_JTAG_SEL

NAND0_JTAG_TRST_L

RN000 47K 1% 1/20W MF 201; RN002 47K 1% 1/20W MF 201; RN021 0 5% 1/20W MF 0201

Spec recommends to tie Boot2 directly to Gnd

=PP1V2_NAND0 — RN001 0 5% 1/20W MF 0201; RN007 0 5% 1/20W MF 0201

NAND0_BCM_L

NAND0_WP_L

Spec recommends to tie BCM, WP directly to 1.2V rail

NAND0_S5E0_SWD_UID0

NAND0_S5E0_SWD_UID1

RN009 47K 1% 1/20W MF 201; RN008 47K 1% 1/20W MF 201

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD0 S5E <0>

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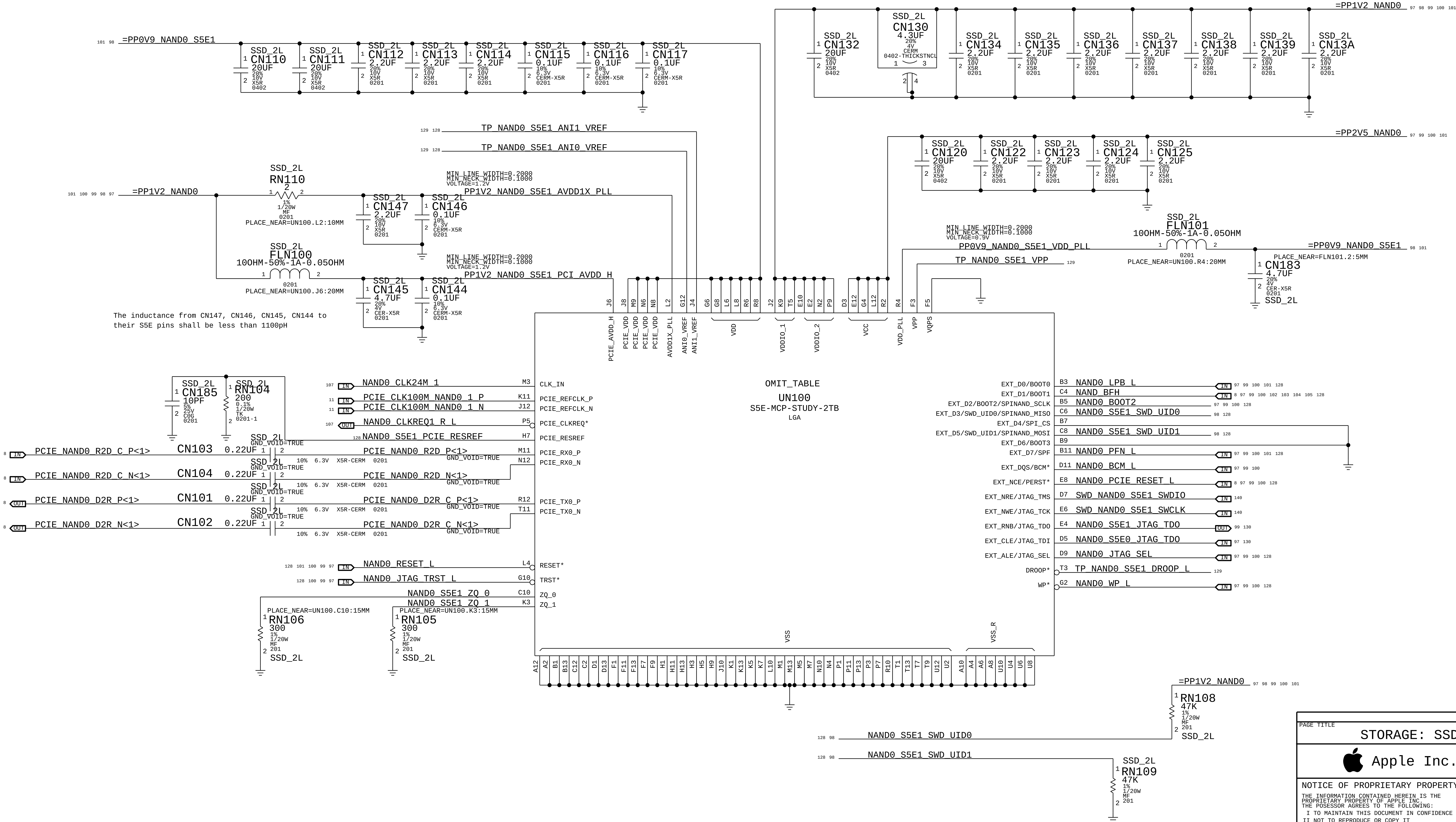
*** OK2INTEGRATE ***

NAND0 S5E1



BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD0 S5E <1>

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*** OK2INTEGRTE ***

NAND0 S5E2

=PP0V9_NAND0_S5E2

SSD_4L CN210 20UF 20% 10V X5R 0402
SSD_4L CN211 20UF 20% 10V X5R 0402
SSD_4L CN212 2.2UF 20% 10V X5R 0201
SSD_4L CN213 2.2UF 20% 10V X5R 0201
SSD_4L CN214 2.2UF 20% 10V X5R 0201
SSD_4L CN215 0.1UF 10% 6.3V CERM-X5R 0201
SSD_4L CN216 0.1UF 10% 6.3V CERM-X5R 0201
SSD_4L CN217 0.1UF 10% 6.3V CERM-X5R 0201

=PP1V2_NAND0

SSD_4L CN232 20UF 20% 10V X5R 0402
SSD_4L CN230 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_4L CN234 2.2UF 20% 10V X5R 0201
SSD_4L CN235 2.2UF 20% 10V X5R 0201
SSD_4L CN236 2.2UF 20% 10V X5R 0201
SSD_4L CN237 2.2UF 20% 10V X5R 0201
SSD_4L CN238 2.2UF 20% 10V X5R 0201
SSD_4L CN239 2.2UF 20% 10V X5R 0201
SSD_4L CN23A 2.2UF 20% 10V X5R 0201

=PP2V5_NAND0

SSD_4L CN220 20UF 20% 10V X5R 0402
SSD_4L CN222 2.2UF 20% 10V X5R 0201
SSD_4L CN223 2.2UF 20% 10V X5R 0201
SSD_4L CN224 2.2UF 20% 10V X5R 0201
SSD_4L CN225 2.2UF 20% 10V X5R 0201

TP_NAND0_S5E2_ANI1_VREF
TP_NAND0_S5E2_ANI0_VREF

SSD_4L RN210 2 1% 1/20W MF 0201 PLACE_NEAR=UN200.L2:10MM

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
PP1V2_NAND0_S5E2_AVDD1X_PLL

SSD_4L CN247 2.2UF 20% 10V X5R 0201
SSD_4L CN246 0.1UF 10% 6.3V CERM-X5R 0201

SSD_4L FLN200 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN200.J6:20MM

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
PP1V2_NAND0_S5E2_PCI_AVDD_H

SSD_4L CN245 4.7UF 20% 4V CER-X5R 0201
SSD_4L CN244 0.1UF 10% 6.3V CERM-X5R 0201

The inductance from CN247, CN246, CN245, CN244 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V
PP0V9_NAND0_S5E2_VDD_PLL

SSD_4L FLN201 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN200.R4:20MM

=PP0V9_NAND0_S5E2

PLACE_NEAR=FLN201.2:5MM
SSD_4L CN283 4.7UF 20% 4V CER-X5R 0201

TP_NAND0_S5E2_VPP

Pin	Net
J6	PCIE_AVDD_H
J8	PCIE_VDD
M9	PCIE_VDD
N6	PCIE_VDD
N8	PCIE_VDD
L2	AVDDIX_PLL
G12	ANI0_VREF
J4	ANI1_VREF
G6	VDD
G8	VDD
L6	VDD
L8	VDD
R6	VDD
R8	VDD
J2	VDDIO_1
K9	VDDIO_1
T5	VDDIO_1
E10	VDDIO_1
E2	VDDIO_2
N2	VDDIO_2
P9	VDDIO_2
D3	VCC
E12	VCC
G4	VCC
L12	VCC
R2	VCC
R4	VDD_PLL
F3	VPP
F5	VQPS

SSD_4L CN285 10PF 5% 25V C0G 0201
SSD_4L RN204 200 0.1% 1/20W TF 0201-1

PCIE_NAND0_R2D_C_P<2>	CN203 0.22UF	PCIE_NAND0_R2D_P<2>	M11 PCIE_RX0_P
PCIE_NAND0_R2D_C_N<2>	CN204 0.22UF	PCIE_NAND0_R2D_N<2>	N12 PCIE_RX0_N
PCIE_NAND0_D2R_P<2>	CN201 0.22UF	PCIE_NAND0_D2R_C_P<2>	R12 PCIE_TX0_P
PCIE_NAND0_D2R_N<2>	CN202 0.22UF	PCIE_NAND0_D2R_C_N<2>	T11 PCIE_TX0_N

SSD_4L GND_VOID=TRUE 10% 6.3V X5R-CERM 0201

NAND0_CLK24M_2	M3	CLK_IN
PCIE_CLK100M_NAND0_2_P	K11	PCIE_REFCLK_P
PCIE_CLKREQ2_N	J12	PCIE_REFCLK_N
NAND0_CLKREQ2_R_L	P5	PCIE_CLKREQ*
NAND0_S5E2_PCIE_RESREF	H7	PCIE_RESREF
NAND0_RESET_L	L4	RESET*
NAND0_JTAG_TRST_L	G10	TRST*
NAND0_S5E2_ZQ_0	C10	ZQ_0
NAND0_S5E2_ZQ_1	K3	ZQ_1

OMIT_TABLE

UN200
S5E-MCP-STUDY-2TB
LGA

EXT_D0/BOOT0	B3	NAND0_LPB_L
EXT_D1/BOOT1	C4	NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK	B5	NAND0_BOOT2
EXT_D3/SWD_UID0/SPINAND_MISO	C6	NAND0_S5E2_SWD_UID0
EXT_D4/SPI_CS	B7	
EXT_D5/SWD_UID1/SPINAND_MOSI	C8	NAND0_S5E2_SWD_UID1
EXT_D6/BOOT3	B9	
EXT_D7/SPF	B11	NAND0_PFN_L
EXT_DQS/BCM*	D11	NAND0_BCM_L
EXT_NCE/PERST*	E8	NAND0_PCIE_RESET_L
EXT_NRE/JTAG_TMS	D7	SWD_NAND0_S5E2_SWDIO
EXT_NWE/JTAG_TCK	E6	SWD_NAND0_S5E2_SWCLK
EXT_RNB/JTAG_TDO	E4	NAND0_S5E2_JTAG_TDO
EXT_CLE/JTAG_TDI	D5	NAND0_S5E1_JTAG_TDO
EXT_ALE/JTAG_SEL	D9	NAND0_JTAG_SEL
DROOP*	T3	TP_NAND0_S5E2_DROOP_L
WP*	G2	NAND0_WP_L

SSD_4L RN206 300 1% 1/20W MF 201 PLACE_NEAR=UN200.C10:15MM
SSD_4L RN205 300 1% 1/20W MF 201 PLACE_NEAR=UN200.K3:15MM

VSS
VSS_R

A12 A2 B1 B13 C12 C2 D1 D13 F1 F11 F13 F7 F9 H1 H11 H13 H3 H5 H9 J10 K1 K13 K5 K7 L10 M1 M13 M5 M7 N10 N4 P1 P11 P13 P3 P7 R10 T1 T13 T7 T9 U12 U2 A10 A4 A6 A8 U10 U4 U6 U8

=PP1V2_NAND0

SSD_4L RN209 47K 1% 1/20W MF 201
SSD_4L RN208 47K 1% 1/20W MF 201

NAND0_S5E2_SWD_UID0
NAND0_S5E2_SWD_UID1

BOM_COST_GROUP=SSD

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*** OK2INTEGRATE ***

NAND0 S5E3

=PP0V9_NAND0_S5E3

CN310 20UF 20% 10V X5R 0402
CN311 20UF 20% 10V X5R 0402
CN312 2.2UF 20% 10V X5R 0201
CN313 2.2UF 20% 10V X5R 0201
CN314 2.2UF 20% 10V X5R 0201
CN315 0.1UF 10% 6.3V CERM-X5R 0201
CN316 0.1UF 10% 6.3V CERM-X5R 0201
CN317 0.1UF 10% 6.3V CERM-X5R 0201

=PP1V2_NAND0

CN332 20UF 20% 10V X5R 0402
CN330 4.3UF 20% 4V CERM 0402-THICKSTNCL
CN334 2.2UF 20% 10V X5R 0201
CN335 2.2UF 20% 10V X5R 0201
CN336 2.2UF 20% 10V X5R 0201
CN337 2.2UF 20% 10V X5R 0201
CN338 2.2UF 20% 10V X5R 0201
CN339 2.2UF 20% 10V X5R 0201
CN33A 2.2UF 20% 10V X5R 0201

TP_NAND0_S5E3_ANI1_VREF
TP_NAND0_S5E3_ANI0_VREF

=PP2V5_NAND0

CN320 20UF 20% 10V X5R 0402
CN322 2.2UF 20% 10V X5R 0201
CN323 2.2UF 20% 10V X5R 0201
CN324 2.2UF 20% 10V X5R 0201
CN325 2.2UF 20% 10V X5R 0201

=PP1V2_NAND0

RN310 2 1% 1/20W MF 0201 PLACE_NEAR=UN300.L2:10MM

CN347 2.2UF 20% 10V X5R 0201
CN346 0.1UF 10% 6.3V CERM-X5R 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V
PP1V2_NAND0_S5E3_AVDD1X_PLL

FLN300 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN300.J6:20MM

CN345 4.7UF 20% 4V CER-X5R 0201
CN344 0.1UF 10% 6.3V CERM-X5R 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V
PP1V2_NAND0_S5E3_PCI_AVDD_H

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=0.9V
PP0V9_NAND0_S5E3_VDD_PLL

FLN301 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN300.R4:20MM

=PP0V9_NAND0_S5E3

PLACE_NEAR=FLN301.2:5MM
CN383 4.7UF 20% 4V CER-X5R 0201

TP_NAND0_S5E3_VPP

The inductance from CN347, CN346, CN345, CN344 to their S5E pins shall be less than 1100pH

J6 PCIE_AVDD_H
J8 M9 N6 N8 PCIE_VDD
L2 AVDDIX_PLL
G12 ANI0_VREF
J4 ANI1_VREF
G6 G8 L6 L8 R6 R8 VDD
J2 K9 T5 E10 E2 N2 P9 VDDIO_1 VDDIO_2
D3 E12 G4 L12 R2 VCC
R4 VDD_PLL
F3 VPP
F5 VQPS

CN385 10PF 5% 25V C0G 0201
RN304 200 0.1% 1/20W TF 0201-1

SSD_4L GND_VOID=TRUE

PCIE_NAND0_R2D_C_P<3>	CN303	0.22UF	PCIE_NAND0_R2D_P<3>	M11	PCIE_RX0_P
PCIE_NAND0_R2D_C_N<3>	CN304	0.22UF	PCIE_NAND0_R2D_N<3>	N12	PCIE_RX0_N
PCIE_NAND0_D2R_P<3>	CN301	0.22UF	PCIE_NAND0_D2R_C_P<3>	R12	PCIE_TX0_P
PCIE_NAND0_D2R_N<3>	CN302	0.22UF	PCIE_NAND0_D2R_C_N<3>	T11	PCIE_TX0_N

10% 6.3V X5R-CERM 0201

NAND0_CLK24M_3 M3 CLK_IN
PCIE_CLK100M_NAND0_3_P K11 PCIE_REFCLK_P
PCIE_CLK100M_NAND0_3_N J12 PCIE_REFCLK_N
NAND0_CLKREQ3_R_L P5 PCIE_CLKREQ*
NAND0_S5E3_PCIE_RESREF H7 PCIE_RESREF

OMIT_TABLE
UN300
S5E-MCP-STUDY-2TB
LGA

EXT_D0/BOOT0	B3	NAND0_LPB_L
EXT_D1/BOOT1	C4	NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK	B5	NAND0_BOOT2
EXT_D3/SWD_UID0/SPINAND_MISO	C6	NAND0_S5E3_SWD_UID0
EXT_D4/SPI_CS	B7	
EXT_D5/SWD_UID1/SPINAND_MOSI	C8	NAND0_S5E3_SWD_UID1
EXT_D6/BOOT3	B9	
EXT_D7/SPF	B11	NAND0_PFN_L
EXT_DQS/BCM*	D11	NAND0_BCM_L
EXT_NCE/PERST*	E8	NAND0_PCIE_RESET_L
EXT_NRE/JTAG_TMS	D7	SWD_NAND0_S5E3_SWDIO
EXT_NWE/JTAG_TCK	E6	SWD_NAND0_S5E3_SWCLK
EXT_RNB/JTAG_TDO	E4	TP_NAND0_S5E3_JTAG_TDO
EXT_CLE/JTAG_TDI	D5	NAND0_S5E2_JTAG_TDO
EXT_ALE/JTAG_SEL	D9	NAND0_JTAG_SEL
DROOP*	T3	TP_NAND0_S5E3_DROOP_L
WP*	G2	NAND0_WP_L

NAND0_RESET_L L4 RESET*
NAND0_JTAG_TRST_L G10 TRST*
NAND0_S5E3_ZQ_0 C10 ZQ_0
NAND0_S5E3_ZQ_1 K3 ZQ_1

RN306 300 1% 1/20W MF 201 SSD_4L PLACE_NEAR=UN300.C10:15MM
RN305 300 1% 1/20W MF 201 SSD_4L PLACE_NEAR=UN300.K3:15MM

VSS: A12 A2 B1 B13 C12 C2 D1 D13 F1 F11 F13 F7 F9 H1 H11 H13 H3 H5 H9 J10 K1 K13 K5 K7 L10 M1 M13 M5 M7 N10 N4 P1 P11 P13 P3 P7 R10 T1 T13 T7 T9 U12 U2
VSS_R: A10 A4 A6 A8 U10 U4 U6 U8

RN308 47K 1% 1/20W MF 201 SSD_4L
RN309 47K 1% 1/20W MF 201 SSD_4L

=PP1V2_NAND0

NAND0_S5E3_SWD_UID0
NAND0_S5E3_SWD_UID1

BOM_COST_GROUP=SSD

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*** OK2INTEGRATE***

=PPBUS_NAND0

CN479 33UF 20% 6.3V CERM-X6S 0402
CN480 33UF 20% 16V TANT CASE-T
CN481 33UF 20% 16V TANT CASE-T
CN482 33UF 20% 16V TANT CASE-T
128S00009

PACK_OPTION=2V5_NAND_PBUS-B12
PACK_OPTION=2V5_NAND_PBUS-B12
PACK_OPTION=2V5_NAND_PBUS-B12
PACK_OPTION=2V5_NAND_PBUS-B12

CN480 33UF 20% 16V TANT CASED12-SM
CN481 33UF 20% 16V TANT CASED12-SM

PACK_OPTION=2V5_NAND_PBUS-D12
PACK_OPTION=2V5_NAND_PBUS-D12
PACK_IGNORE=TRUE
PACK_IGNORE=TRUE

CN480 68UF 20% 16V POLY-TANT CASE-D2E-SM
CN481 68UF 20% 16V POLY-TANT CASE-D2E-SM

PACK_OPTION=2V5_NAND_PBUS-D2E
PACK_OPTION=2V5_NAND_PBUS-D2E
PACK_IGNORE=TRUE
PACK_IGNORE=TRUE

CN483 2.2UF 20% 25V X6S-CERM 0402
CN484 2.2UF 20% 25V X6S-CERM 0402
CN485 2.2UF 20% 25V X6S-CERM 0402
CN486 2.2UF 20% 25V X6S-CERM 0402

UN480
LT8642EV-2#PBF
LQFN-THICKSTNCL
CRITICAL

VIN (4,5,6,13,14,15)
EN/UV (17)
VC (22)
PG (23)
FB (24)
SS (21)
RT (18)
SYNC/MODE (20)
BIAS (1)
INTVCC (2)
BST (7)
SW (8,9,10,11,12)
CLKOUT (19)
GND (3,16,25,26,27,28)
NC (29,30,31,32)

P2V5_NAND0_BIAS
PP2V5_NAND0_INTVCC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=2.5V

CN490 2.2UF 20% 25V X6S-CERM 0402

P2V5_NAND0_BST
SWITCH_NODE=TRUE
DIDT=TRUE

RN492 1.5 5% 1/20W MF 201

P2V5_NAND0_BST_R
SWITCH_NODE=TRUE
DIDT=TRUE

CN492 47NF 10% 10V X6S-CERM 0201

P2V5_NAND0_SW
SWITCH_NODE=TRUE
DIDT=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

RN487 0 5% 1/20W MF 0201 =PPVIN_P3V8NAND0
CN491 2.2UF 20% 25V X6S-CERM 0402

P2V5_NAND0_PGOOD
RN412 100K 1% 1/20W MF 201

LN480 0.56UH-20%-16A-0.0072OHM PILA052D-SM

=PP2V5_NAND0_REG
CN494 150UF 20% 6.3V TANT CASE-B-SM
CN495 150UF 20% 6.3V TANT CASE-B-SM
CN496 150UF 20% 6.3V TANT CASE-B-SM
CN498 10UF 20% 6.3V CER-X6S 0402
CN499 10UF 20% 6.3V CER-X6S 0402

XWN481 SM
P2V5_NAND0_FB_XW
RN482 10 5% 1/20W MF 201

RN488 0 0201 1/20W MF 5%
P2V5_NAND0_EN
P2V5_NAND0_EN_R
P2V5_NAND0_VC
P2V5_NAND0_PGOOD
P2V5_NAND0_FB
P2V5_NAND0_SS
P2V5_NAND0_RT

RN481 18K 1% 1/20W MF 201
CN488 1000PF 10% 16V X7R-1 0201
CN489 56PF 5% 25V NP0-C0G 0201
CN487 1.2NF +/-10% 10V CERM 0201-1
SOFT START TIME SET TO: 9.42/0.63/1.1 ms min / typ / max
RN480 25.5K 1% 1/20W MF 201
FREQUENCY SET TO: 1.5MHz
XWN480 SM

P2V5_NAND0_VC_R
AGND_P2V5_NAND0
Note: Need to verify 1.1ms is fine for Pwr Up seq

RN485 27.4K 0.1% 1/20W MF 0201

RN486 10K 1% 1/20W MF 201
P2V5_NAND0_FB_C
CN493 1000PF 10% 16V X7R-1 0201

P2V5_NAND0_FB_RC
RN483 6.98K 1% 1/20W MF 201
P2V5_NAND0_FB_RC2
RN484 82.5K 0.1% 1/20W MF 201-1
P2V5_NAND0_FB

OCARINA I2C BASE ADDRESS
STG0: F2
STG1: F0

=PPVIN_P3V8NAND0
CN400 10UF 20% 6.3V CERM-X6S 0402
CN401 10UF 20% 6.3V CERM-X6S 0402
CN402 0.1UF 20% 16V X6S-CERM 0201
CN403 4.7UF 20% 6.3V X6S 0402
CN404 4.7UF 20% 6.3V X6S 0402
CN405 0.1UF 20% 16V X6S-CERM 0201
CRITICAL CN406 150UF 20% 6.3V TANT-POLY CASE-B1S-1

PLACE CN400-CN402 NEAR OCARINA PINS E7/E8
PLACE CN403-CN405 NEAR OCARINA PINS A7/A8
PLACE CN406 NEAR OCARINA PIN B4

PPVDD_LDO_NAND0_OCARINA
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=2.5V
CN407 0.22UF 20% 6.3V X6S-CERM 0201

TP_NAND0_OCARINA_VCC_DET
=PP1V8_S2_NAND0
CN409 0.1UF 10% 6.3V CERM-X5R 0201

VDD_BUCK0 (E8,E7)
VDD_BUCK1 (A8,A7)
VDD_MAIN (B4)
VDD_LDO (B5)
VCC_DET (G1)
V_BUF_1.8V (C1)

=PPVIN_P3V8NAND0
RN406 10K 5% 1/20W MF 201
RN410 100K 1% 1/20W MF 201
RN411 100K 1% 1/20W MF 201

UN400
D2499A0P0VLAVBC2
WLCSP

338S00600
CRITICAL
OMIT_TABLE

ATM (F3)
ADDR (D2) NAND0_STG01_ADDR
FORCE_EN (E1) NAND0_FORCE_EN
I2C_SCL (G2) I2C_SMC_NAND_1V8_SCL
I2C_SDA (G3) I2C_SMC_NAND_1V8_SDA
LPBN (F4) NAND0_LPB_L
PFN* (G5) NAND0_PFN_L
PGOOD (G6) NAND0_OCARINA_PGOOD
PMIC_RESET* (D1)
POK1 (D3) P2V5_NAND0_PGOOD
POK2 (F1)
RESET* (E5) NAND0_RESET_L
SYS_ALIVE (F2) PMU_SYS_ALIVE
VEN1 (F5) P2V5_NAND0_EN
VEN2/PMIC_CTRL (E4) TP_NAND0_OCARINA_VEN2
WP* (G4) TP_NAND0_OCARINA_WP_L

TCAL (A4) NAND0_OCARINA_TCAL
VREF (B3) NAND0_OCARINA_VREF
IREF (B2) NAND0_OCARINA_IREF
TDEV1 (B1) NAND0_OCARINA_TDEV1
TDEV2 (C2) NAND0_OCARINA_TDEV2
VR1_DISCHG (A3) =PP2V5_NAND0
VR2_DISCHG (A1)
BUCK0_FB_DIS (D5) PP0V9_NAND0_FB_DIS
BUCK1_FB_DIS (C5) PP1V2_NAND0_FB_DIS
BUCK0_LX0 (F8,F7)
BUCK0_LX1 (D8,D7)
BUCK1_LX0 (B8,B7)
VSS (A6,A5,B6,A2,C3,C4,D5,D4,E6,E2,F6,E3,G8,G7,C8,C7,C6)
VSS(VSS_BUCK0) (G8,G7)
VSS(VSS_BUCK01) (C8,C7,C6)

RN405 200K 0.1% 1/20W TF 0201
CN408 0.1UF 10% 6.3V CERM-X5R 0201
RN400 8.06K 0.1% 1/20W TF 0201

PP0V9_NAND0
RN420 0 5% 1/20W MF 0201
=PP1V2_NAND0
RN430 0 5% 1/20W MF 0201

CN428 20UF 20% 10V X5R 0402
CN429 20UF 20% 10V X5R 0402
CN42A 20UF 20% 10V X5R 0402
CN42B 20UF 20% 10V X5R 0402

P0V9_LX0_NAND0
DIDT=TRUE
SWITCH_NODE=TRUE
LN421 1UH-20%-4.8A-0.032OHM 1210

P0V9_LX1_NAND0
DIDT=TRUE
SWITCH_NODE=TRUE
LN420 0.47UH-20%-6.7A-0.023OHM 1210

P1V2_LX0_NAND0
DIDT=TRUE
SWITCH_NODE=TRUE
LN430 0.47UH-20%-6.7A-0.023OHM 1210

=PP0V9_NAND0_REG
CN420 20UF 20% 10V X5R 0402
CN421 20UF 20% 10V X5R 0402
CN422 20UF 20% 10V X5R 0402
CN423 20UF 20% 10V X5R 0402
CN424 20UF 20% 10V X5R 0402
CN425 20UF 20% 10V X5R 0402
CN426 20UF 20% 10V X5R 0402
CN427 20UF 20% 10V X5R 0402

=PP1V2_NAND0_REG
CN430 20UF 20% 10V X5R 0402
CN431 20UF 20% 10V X5R 0402
CN432 20UF 20% 10V X5R 0402
CN433 20UF 20% 10V X5R 0402
CN434 20UF 20% 10V X5R 0402
CN435 20UF 20% 10V X5R 0402
CN436 20UF 20% 10V X5R 0402
CN437 20UF 20% 10V X5R 0402
CN438 20UF 20% 10V X5R 0402
CN439 20UF 20% 10V X5R 0402

NAND0_OCARINA_TDEV1
RN402 100K-1%-0.001A 0201
RN401 18.2K 0.1% 1/20W TK 0201

NAND0_OCARINA_TDEV2
RN404 100K-1%-0.001A 0201
RN403 18.2K 0.1% 1/20W TK 0201

=PP2V5_NAND0_REG
PP2V5_NAND0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=2.5V
MAKE_BASE=TRUE
=PP2V5_NAND0

=PP1V2_NAND0_REG
PP1V2_NAND0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PP1V2_NAND0

=PP0V9_NAND0_REG
PP0V9_NAND0
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PP0V9_NAND0_S5E0
=PP0V9_NAND0_S5E1
=PP0V9_NAND0_S5E2
=PP0V9_NAND0_S5E3

RN418 47K 1% 1/20W MF 201
RN419 47K 1% 1/20W MF 201
RN417 47K 1% 1/20W MF 201
=PP1V2_NAND0

NAND0_RESET_L
NAND0_LPB_L
NAND0_PFN_L

BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD0 OCARINA & NAND VCC

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*** OK2INTEGRATE ***

NAND1 S5E0

The inductance from CN547, CN546, CN545, CN544 to their S5E pins shall be less than 1100pH

Spec recommends to tie Boot2 directly to Gnd

Spec recommends to tie BCM, WP directly to 1.2V rail

BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD1 S5E <0>

Apple Inc.

DRAWING NUMBER 051-05641 SIZE D

REVISION 6.33.0

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*** OK2INTEGRATE ***

NAND1 S5E1

=PP0V9_NAND1_S5E1

SSD_8L CN610 20UF 20% 10V X5R 0402
SSD_8L CN611 20UF 20% 10V X5R 0402
SSD_8L CN612 2.2UF 20% 10V X5R 0201
SSD_8L CN613 2.2UF 20% 10V X5R 0201
SSD_8L CN614 2.2UF 20% 10V X5R 0201
SSD_8L CN615 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN616 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN617 0.1UF 10% 6.3V CERM-X5R 0201

=PP1V2_NAND1

SSD_8L CN632 20UF 20% 10V X5R 0402
SSD_8L CN630 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_8L CN634 2.2UF 20% 10V X5R 0201
SSD_8L CN635 2.2UF 20% 10V X5R 0201
SSD_8L CN636 2.2UF 20% 10V X5R 0201
SSD_8L CN637 2.2UF 20% 10V X5R 0201
SSD_8L CN638 2.2UF 20% 10V X5R 0201
SSD_8L CN639 2.2UF 20% 10V X5R 0201
SSD_8L CN63A 2.2UF 20% 10V X5R 0201

=PP2V5_NAND1

SSD_8L CN620 20UF 20% 10V X5R 0402
SSD_8L CN622 2.2UF 20% 10V X5R 0201
SSD_8L CN623 2.2UF 20% 10V X5R 0201
SSD_8L CN624 2.2UF 20% 10V X5R 0201
SSD_8L CN625 2.2UF 20% 10V X5R 0201

TP_NAND1_S5E1_ANI1_VREF
TP_NAND1_S5E1_ANI0_VREF

=PP1V2_NAND1 — SSD_8L RN610 2 1% 1/20W MF 0201 — PLACE_NEAR=UN600.L2:10MM

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
PP1V2_NAND1_S5E1_AVDD1X_PLL

SSD_8L CN647 2.2UF 20% 10V X5R 0201
SSD_8L CN646 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L FLN600 10OHM-50%-1A-0.05OHM 0201 — PLACE_NEAR=UN600.J6:20MM

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
PP1V2_NAND1_S5E1_PCI_AVDD_H

SSD_8L CN645 4.7UF 20% 6.3V CER-X5R 0201
SSD_8L CN644 0.1UF 10% 6.3V CERM-X5R 0201

The inductance from CN647, CN646, CN645, CN644 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V
PP0V9_NAND1_S5E1_VDD_PLL

SSD_8L FLN601 10OHM-50%-1A-0.05OHM 0201 — PLACE_NEAR=UN600.R4:20MM

=PP0V9_NAND1_S5E1 — PLACE_NEAR=FLN601.2:5MM
SSD_8L CN683 4.7UF 20% 4V CER-X5R 0201

TP_NAND1_S5E1_VPP

J6 PCIE_AVDD_H; J8 M9 N6 N8 PCIE_VDD; L2 AVDDIX_PLL; G12 ANI0_VREF; J4 ANI1_VREF; G6 G8 L6 L8 R6 R8 VDD; J2 K9 T5 E10 E2 N2 P9 VDDIO_1 VDDIO_2; D3 E12 G4 L12 R2 VCC; R4 VDD_PLL; F3 VPP; F5 VQPS

OMIT_TABLE
UN600
S5E-MCP-STUDY-2TB
LGA

SSD_8L CN685 10PF 5% 25V C0G 0201
SSD_8L RN604 200 0.1% 1/20W TF 0201-1

NAND1_CLK24M_1 — M3 CLK_IN
PCIE_CLK100M_NAND1_1_P — K11 PCIE_REFCLK_P
PCIE_CLK100M_NAND1_1_N — J12 PCIE_REFCLK_N
NAND1_CLKREQ1_R_L — P5 PCIE_CLKREQ*
NAND1_S5E1_PCIE_RESREF — H7 PCIE_RESREF

PCIE_NAND1_R2D_C_P<1> — CN603 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND1_R2D_P<1> — M11 PCIE_RX0_P
PCIE_NAND1_R2D_C_N<1> — CN604 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND1_R2D_N<1> — N12 PCIE_RX0_N
PCIE_NAND1_D2R_P<1> — CN601 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND1_D2R_C_P<1> — R12 PCIE_TX0_P
PCIE_NAND1_D2R_N<1> — CN602 0.22UF 10% 6.3V X5R-CERM 0201 — PCIE_NAND1_D2R_C_N<1> — T11 PCIE_TX0_N

NAND1_RESET_L — L4 RESET*
NAND1_JTAG_TRST_L — G10 TRST*
NAND1_S5E1_ZQ_0 — C10 ZQ_0
NAND1_S5E1_ZQ_1 — K3 ZQ_1

PLACE_NEAR=UN600.C10:15MM — SSD_8L RN606 300 1% 1/20W MF 201 — SSD_8L
PLACE_NEAR=UN600.K3:15MM — SSD_8L RN605 300 1% 1/20W MF 201 — SSD_8L

EXT_D0/BOOT0 — B3 NAND1_LPB_L
EXT_D1/BOOT1 — C4 NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK — B5 NAND1_BOOT2
EXT_D3/SWD_UID0/SPINAND_MISO — C6 NAND1_S5E1_SWD_UID0
EXT_D4/SPI_CS — B7
EXT_D5/SWD_UID1/SPINAND_MOSI — C8 NAND1_S5E1_SWD_UID1
EXT_D6/BOOT3 — B9
EXT_D7/SPF — B11 NAND1_PFN_L
EXT_DQS/BCM* — D11 NAND1_BCM_L
EXT_NCE/PERST* — E8 NAND1_PCIE_RESET_L
EXT_NRE/JTAG_TMS — D7 SWD_NAND1_S5E1_SWDIO
EXT_NWE/JTAG_TCK — E6 SWD_NAND1_S5E1_SWCLK
EXT_RNB/JTAG_TDO — E4 NAND1_S5E1_JTAG_TDO
EXT_CLE/JTAG_TDI — D5 NAND1_S5E0_JTAG_TDO
EXT_ALE/JTAG_SEL — D9 NAND1_JTAG_SEL
DROOP* — T3 TP_NAND1_S5E1_DROOP_L
WP* — G2 NAND1_WP_L

VSS: A12 A2 B1 B13 C12 C2 D1 D13 F1 F11 F13 F7 F9 H1 H11 H13 H3 H5 H9 J10 K1 K13 K5 K7 L10 M1 M13 M5 M7 N10 N4 P1 P11 P13 P3 P7 R10 T1 T13 T7 T9 U12 U2
VSS_R: A10 A4 A6 A8 U10 U4 U6 U8

=PP1V2_NAND1
SSD_8L RN608 47K 1% 1/20W MF 201
NAND1_S5E1_SWD_UID0
SSD_8L RN609 47K 1% 1/20W MF 201
NAND1_S5E1_SWD_UID1

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 S5E <1>

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*** OK2INTEGRTE ***

NAND1 S5E2

=PP0V9_NAND1_S5E2

SSD_8L CN710 20UF 20% 10V X5R 0402
SSD_8L CN711 20UF 20% 10V X5R 0402
SSD_8L CN712 2.2UF 20% 10V X5R 0201
SSD_8L CN713 2.2UF 20% 10V X5R 0201
SSD_8L CN714 2.2UF 20% 10V X5R 0201
SSD_8L CN715 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN716 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN717 0.1UF 10% 6.3V CERM-X5R 0201

=PP1V2_NAND1

SSD_8L CN732 20UF 20% 10V X5R 0402
SSD_8L CN730 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_8L CN734 2.2UF 20% 10V X5R 0201
SSD_8L CN735 2.2UF 20% 10V X5R 0201
SSD_8L CN736 2.2UF 20% 10V X5R 0201
SSD_8L CN737 2.2UF 20% 10V X5R 0201
SSD_8L CN738 2.2UF 20% 10V X5R 0201
SSD_8L CN739 2.2UF 20% 10V X5R 0201
SSD_8L CN73A 2.2UF 20% 10V X5R 0201

=PP2V5_NAND1

SSD_8L CN720 20UF 20% 10V X5R 0402
SSD_8L CN722 2.2UF 20% 10V X5R 0201
SSD_8L CN723 2.2UF 20% 10V X5R 0201
SSD_8L CN724 2.2UF 20% 10V X5R 0201
SSD_8L CN725 2.2UF 20% 10V X5R 0201

TP_NAND1_S5E2_ANI1_VREF
TP_NAND1_S5E2_ANI0_VREF

=PP1V2_NAND1

SSD_8L RN710 2 1% 1/20W MF 0201
PLACE_NEAR=UN700.L2:10MM

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V

PP1V2_NAND1_S5E2_AVDD1X_PLL

SSD_8L CN747 2.2UF 20% 10V X5R 0201
SSD_8L CN746 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L FLN700 10OHM-50%-1A-0.05OHM 0201
PLACE_NEAR=UN700.J6:20MM

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=1.2V

PP1V2_NAND1_S5E2_PCI_AVDD_H

SSD_8L CN745 4.7UF 20% 4V CER-X5R 0201
SSD_8L CN744 0.1UF 10% 6.3V CERM-X5R 0201

The inductance from CN747, CN746, CN745, CN744 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=0.9V

PP0V9_NAND1_S5E2_VDD_PLL

SSD_8L FLN701 10OHM-50%-1A-0.05OHM 0201
PLACE_NEAR=UN700.R4:20MM

=PP0V9_NAND1_S5E2

PLACE_NEAR=FLN701.2:5MM
SSD_8L CN783 4.7UF 20% 4V CER-X5R 0201

TP_NAND1_S5E2_VPP

Pin	Net
J6	PCIE_AVDD_H
J8	PCIE_VDD
M9	PCIE_VDD
N6	PCIE_VDD
N8	PCIE_VDD
L2	AVDDIX_PLL
G12	ANI0_VREF
J4	ANI1_VREF
G6	VDD
G8	VDD
L6	VDD
L8	VDD
R6	VDD
R8	VDD
J2	VDDIO_1
K9	VDDIO_1
T5	VDDIO_1
E10	VDDIO_1
E2	VDDIO_2
N2	VDDIO_2
P9	VDDIO_2
D3	VCC
E12	VCC
G4	VCC
L12	VCC
R2	VCC
R4	VDD_PLL
F3	VPP
F5	VQPS

SSD_8L CN785 10PF 5% 25V C0G 0201
SSD_8L RN704 200 0.1% 1/20W TF 0201-1

PCIE_NAND1_R2D_C_P<2>	CN703 0.22UF	PCIE_NAND1_R2D_P<2>	M11
PCIE_NAND1_R2D_C_N<2>	CN704 0.22UF	PCIE_NAND1_R2D_N<2>	N12
PCIE_NAND1_D2R_P<2>	CN701 0.22UF	PCIE_NAND1_D2R_C_P<2>	R12
PCIE_NAND1_D2R_N<2>	CN702 0.22UF	PCIE_NAND1_D2R_C_N<2>	T11

SSD_8L 10% 6.3V X5R-CERM 0201 GND_VOID=TRUE

NAND1_CLK24M_2	M3	CLK_IN
PCIE_CLK100M_NAND1_2_P	K11	PCIE_REFCLK_P
PCIE_CLK100M_NAND1_2_N	J12	PCIE_REFCLK_N
NAND1_CLKREQ2_R_L	P5	PCIE_CLKREQ*
NAND1_S5E2_PCIE_RESREF	H7	PCIE_RESREF
	M11	PCIE_RX0_P
	N12	PCIE_RX0_N
	R12	PCIE_TX0_P
	T11	PCIE_TX0_N

OMIT_TABLE
UN700
S5E-MCP-STUDY-2TB
LGA

NAND1_RESET_L	L4	RESET*
NAND1_JTAG_TRST_L	G10	TRST*
NAND1_S5E2_ZQ_0	C10	ZQ_0
NAND1_S5E2_ZQ_1	K3	ZQ_1

SSD_8L RN706 300 1% 1/20W MF 201
PLACE_NEAR=UN700.C10:15MM

SSD_8L RN705 300 1% 1/20W MF 201
PLACE_NEAR=UN700.K3:15MM

VSS: A12 A2 B1 B13 C12 C2 D1 D13 F1 F11 F13 F7 F9 H1 H11 H13 H3 H5 H9 J10 K1 K13 K5 K7 L10 M1 M13 M5 M7 N10 N4 P1 P11 P13 P3 P7 R10 T1 T13 T7 T9 U12 U2

VSS_R: A10 A4 A6 A8 U10 U4 U6 U8

EXT_D0/BOOT0	B3	NAND1_LPB_L
EXT_D1/BOOT1	C4	NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK	B5	NAND1_BOOT2
EXT_D3/SWD_UID0/SPINAND_MISO	C6	NAND1_S5E2_SWD_UID0
EXT_D4/SPI_CS	B7	
EXT_D5/SWD_UID1/SPINAND_MOSI	C8	NAND1_S5E2_SWD_UID1
EXT_D6/BOOT3	B9	
EXT_D7/SPF	B11	NAND1_PFN_L
EXT_DQS/BCM*	D11	NAND1_BCM_L
EXT_NCE/PERST*	E8	NAND1_PCIE_RESET_L
EXT_NRE/JTAG_TMS	D7	SWD_NAND1_S5E2_SWDIO
EXT_NWE/JTAG_TCK	E6	SWD_NAND1_S5E2_SWCLK
EXT_RNB/JTAG_TDO	E4	NAND1_S5E2_JTAG_TDO
EXT_CLE/JTAG_TDI	D5	NAND1_S5E1_JTAG_TDO
EXT_ALE/JTAG_SEL	D9	NAND1_JTAG_SEL
DROOP*	T3	TP_NAND1_S5E2_DROOP_L
WP*	G2	NAND1_WP_L

=PP1V2_NAND1

SSD_8L RN709 47K 1% 1/20W MF 201
SSD_8L RN708 47K 1% 1/20W MF 201

NAND1_S5E2_SWD_UID0
NAND1_S5E2_SWD_UID1

BOM_COST_GROUP=SSD

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*** OK2INTEGRATE ***

NAND1 S5E3

=PP0V9_NAND1_S5E3

SSD_8L CN810 20UF 20% 10V X5R 0402
SSD_8L CN811 20UF 20% 10V X5R 0402
SSD_8L CN812 2.2UF 20% 10V X5R 0201
SSD_8L CN813 2.2UF 20% 10V X5R 0201
SSD_8L CN814 2.2UF 20% 10V X5R 0201
SSD_8L CN815 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN816 0.1UF 10% 6.3V CERM-X5R 0201
SSD_8L CN817 0.1UF 10% 6.3V CERM-X5R 0201

=PP1V2_NAND1

SSD_8L CN832 20UF 20% 10V X5R 0402
SSD_8L CN830 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_8L CN834 2.2UF 20% 10V X5R 0201
SSD_8L CN835 2.2UF 20% 10V X5R 0201
SSD_8L CN836 2.2UF 20% 10V X5R 0201
SSD_8L CN837 2.2UF 20% 10V X5R 0201
SSD_8L CN838 2.2UF 20% 10V X5R 0201
SSD_8L CN839 2.2UF 20% 10V X5R 0201
SSD_8L CN83A 2.2UF 20% 10V X5R 0201

=PP2V5_NAND1

SSD_8L CN820 20UF 20% 10V X5R 0402
SSD_8L CN822 2.2UF 20% 10V X5R 0201
SSD_8L CN823 2.2UF 20% 10V X5R 0201
SSD_8L CN824 2.2UF 20% 10V X5R 0201
SSD_8L CN825 2.2UF 20% 10V X5R 0201

TP_NAND1_S5E3_ANI1_VREF
TP_NAND1_S5E3_ANI0_VREF

=PP1V2_NAND1 → SSD_8L RN810 2 1% 1/20W MF 0201 → PLACE_NEAR=UN800.L2:10MM

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
PP1V2_NAND1_S5E3_AVDD1X_PLL

SSD_8L CN847 2.2UF 20% 10V X5R 0201
SSD_8L CN846 0.1UF 10% 6.3V CERM-X5R 0201

SSD_8L FLN800 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN800.J6:20MM

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
PP1V2_NAND1_S5E3_PCI_AVDD_H

SSD_8L CN845 4.7UF 20% 4V CER-X5R 0201
SSD_8L CN844 0.1UF 10% 6.3V CERM-X5R 0201

The inductance from CN847, CN846, CN845, CN844 to their S5E pins shall be less than 1100pH

MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V
PP0V9_NAND1_S5E3_VDD_PLL

SSD_8L FLN801 10OHM-50%-1A-0.05OHM 0201 PLACE_NEAR=UN800.R4:20MM

=PP0V9_NAND1_S5E3 → PLACE_NEAR=FLN801.2:5MM → SSD_8L CN883 4.7UF 20% 4V CER-X5R 0201

TP_NAND1_S5E3_VPP

SSD_8L CN885 10PF 5% 25V C0G 0201
SSD_8L RN804 200 0.1% 1/20W TF 0201-1

PCIE_NAND1_R2D_C_P<3>	CN803	0.22UF	PCIE_NAND1_R2D_P<3>	GND_VOID=TRUE
PCIE_NAND1_R2D_C_N<3>	CN804	0.22UF	PCIE_NAND1_R2D_N<3>	GND_VOID=TRUE
PCIE_NAND1_D2R_P<3>	CN801	0.22UF	PCIE_NAND1_D2R_C_P<3>	GND_VOID=TRUE
PCIE_NAND1_D2R_N<3>	CN802	0.22UF	PCIE_NAND1_D2R_C_N<3>	GND_VOID=TRUE

10% 6.3V X5R-CERM 0201

NAND1_CLK24M_3 → CLK_IN (M3)
PCIE_CLK100M_NAND1_3_P → PCIE_REFCLK_P (K11)
PCIE_CLK100M_NAND1_3_N → PCIE_REFCLK_N (J12)
NAND1_CLKREQ3_R_L → PCIE_CLKREQ* (P5)
NAND1_S5E3_PCIE_RESREF → PCIE_RESREF (H7)
PCIE_RX0_P (M11)
PCIE_RX0_N (N12)
PCIE_TX0_P (R12)
PCIE_TX0_N (T11)
NAND1_RESET_L → RESET* (L4)
NAND1_JTAG_TRST_L → TRST* (G10)
NAND1_S5E3_ZQ_0 → ZQ_0 (C10)
NAND1_S5E3_ZQ_1 → ZQ_1 (K3)

PLACE_NEAR=UN800.C10:15MM
SSD_8L RN806 300 1% 1/20W MF 201 SSD_8L

PLACE_NEAR=UN800.K3:15MM
SSD_8L RN805 300 1% 1/20W MF 201 SSD_8L

OMIT_TABLE
UN800
S5E-MCP-STUDY-2TB
LGA

PCIE_AVDD_H: J6
PCIE_VDD: J8, M9, N6, N8
AVDDIX_PLL: L2
ANI0_VREF: G12
ANI1_VREF: J4
VDD: G6, G8, L6, L8, R6, R8
VDDIO_1: J2, K9, T5
VDDIO_2: E10, E2, N2, P9
VCC: D3, E12, G4, L12, R2
VDD_PLL: R4
VPP: F3
VQPS: F5
VSS: A12, A2, B1, B13, C12, C2, D1, D13, F1, F11, F13, F7, F9, H1, H11, H13, H3, H5, H9, J10, K1, K13, K5, K7, L10, M1, M13, M5, M7, N10, N4, P1, P11, P13, P3, P7, R10, T1, T13, T7, T9, U12, U2
VSS_R: A10, A4, A6, A8, U10, U4, U6, U8

EXT_D0/BOOT0	B3	NAND1_LPB_L
EXT_D1/BOOT1	C4	NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK	B5	NAND1_BOOT2
EXT_D3/SWD_UID0/SPINAND_MISO	C6	NAND1_S5E3_SWD_UID0
EXT_D4/SPI_CS	B7	
EXT_D5/SWD_UID1/SPINAND_MOSI	C8	NAND1_S5E3_SWD_UID1
EXT_D6/BOOT3	B9	
EXT_D7/SPF	B11	NAND1_PFN_L
EXT_DQS/BCM*	D11	NAND1_BCM_L
EXT_NCE/PERST*	E8	NAND1_PCIE_RESET_L
EXT_NRE/JTAG_TMS	D7	SWD_NAND1_S5E3_SWDIO
EXT_NWE/JTAG_TCK	E6	SWD_NAND1_S5E3_SWCLK
EXT_RNB/JTAG_TDO	E4	TP_NAND1_S5E3_JTAG_TDO
EXT_CLE/JTAG_TDI	D5	NAND1_S5E2_JTAG_TDO
EXT_ALE/JTAG_SEL	D9	NAND1_JTAG_SEL
DROOP*	T3	TP_NAND1_S5E3_DROOP_L
WP*	G2	NAND1_WP_L

=PP1V2_NAND1 → SSD_8L RN808 47K 1% 1/20W MF 201
=PP1V2_NAND1 → SSD_8L RN809 47K 1% 1/20W MF 201

NAND1_S5E3_SWD_UID0
NAND1_S5E3_SWD_UID1

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD1 S5E <3>

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*** OK2INTEGRATE***

=PPBUS_NAND1

SSD_OC1VR1 CN979 33UF 20% 16V TANT CASE-T 128S00009
SSD_OC1VR1 CN980 33UF 20% 16V TANT CASE-T 128S00009
SSD_OC1VR1 CN981 33UF 20% 16V TANT CASE-T 128S00009
SSD_OC1VR1 CN982 33UF 20% 16V TANT CASE-T 128S00009

PACK_OPTION=2V5_NAND_PBUS-B12
PACK_OPTION=2V5_NAND_PBUS-B12
PACK_OPTION=2V5_NAND_PBUS-B12
PACK_OPTION=2V5_NAND_PBUS-B12

SSD_OC1VR1 CN980 33UF 20% 16V TANT CASED12-SM
SSD_OC1VR1 CN981 33UF 20% 16V TANT CASED12-SM

PACK_OPTION=2V5_NAND_PBUS-D12
PACK_OPTION=2V5_NAND_PBUS-D12
PACK_IGNORE=TRUE
PACK_IGNORE=TRUE

SSD_OC1VR1 CN980 68UF 20% 16V POLY-TANT CASE-D2E-SM
SSD_OC1VR1 CN981 68UF 20% 16V POLY-TANT CASE-D2E-SM

PACK_OPTION=2V5_NAND_PBUS-D2E
PACK_OPTION=2V5_NAND_PBUS-D2E
PACK_IGNORE=TRUE
PACK_IGNORE=TRUE

SSD_OC1VR1 CN983 2.2UF 20% 25V X6S-CERM 0402
SSD_OC1VR1 CN984 2.2UF 20% 25V X6S-CERM 0402
SSD_OC1VR1 CN985 2.2UF 20% 25V X6S-CERM 0402
SSD_OC1VR1 CN986 2.2UF 20% 25V X6S-CERM 0402

UN980
LT8642EV-2#PBF
LQFN-THICKSTNCL
CRITICAL
SSD_OC1VR1

VIN	4	
VIN	5	
VIN	6	
VIN	13	
VIN	14	
VIN	15	
BIAS	1	P2V5_NAND1_BIAS
INTVCC	2	PP2V5_NAND1_INTVCC MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=2.5V
BST	7	P2V5_NAND1_BST SWITCH_NODE=TRUE DIDT=TRUE
SW	8	
SW	9	
SW	10	
SW	11	
SW	12	P2V5_NAND1_SW SWITCH_NODE=TRUE DIDT=TRUE MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000
CLKOUT	19	NC
EN/UV	17	P2V5_NAND1_EN_R
VC	22	P2V5_NAND1_VC
PG	23	P2V5_NAND1_PGOOD
FB	24	P2V5_NAND1_FB
SS	21	P2V5_NAND1_SS
RT	18	P2V5_NAND1_RT
SYNC/MODE	20	
GND	3 16 25 26 27 28	
NC	29 30 31 32	

SSD_OC1VR1 RN988 0 1/20W MF 0201 5%
P2V5_NAND1_EN
P2V5_NAND1_EN_R

SSD_OC1VR1 RN981 18K 1% 1/20W MF 201
SSD_OC1VR1 CN988 1000PF 10% 16V X7R-1 0201
SSD_OC1VR1 CN989 56PF 5% 25V NP0-C0G 0201
SSD_OC1VR1 CN987 1.2NF +/-10% 10V CERM 0201-1
SOFT START TIME SET TO: 9.42/0.63/1.1 ms min / typ / max
SSD_OC1VR1 RN980 25.5K 1% 1/20W MF 201
FREQUENCY SET TO: 1.5MHz
XWN980 SM

P2V5_NAND1_VC_R
AGND_P2V5_NAND1
Note: Need to verify 1.1ms is fine for Pwr Up seq

SSD_OC1VR1 RN985 27.4K 0.1% 1/20W MF 0201

SSD_OC1VR1 RN987 0 5% 1/20W MF 0201 =PPVIN_P3V8NAND1
SSD_OC1VR1 CN991 2.2UF 20% 25V X6S-CERM 0402
SSD_OC1VR1 CN990 2.2UF 20% 25V X6S-CERM 0402
SSD_OC1VR1 RN992 1.5 5% 1/20W MF 201
SSD_OC1VR1 CN992 47NF 10% 10V X6S-CERM 0201

SSD_OC1VR1 LN980 0.56UH-20%-16A-0.0072OHM PILA052D-SM

SSD_OC1VR1 RN912 100K 1% 1/20W MF 201
P2V5_NAND1_PGOOD

SSD_OC1VR1 XWN981 SM
SSD_OC1VR1 CN994 150UF 20% 6.3V TANT CASE-B-SM
SSD_OC1VR1 CN995 150UF 20% 6.3V TANT CASE-B-SM
SSD_OC1VR1 CN996 150UF 20% 6.3V TANT CASE-B-SM
=PP2V5_NAND1_REG

P2V5_NAND1_FB_XW
SSD_OC1VR1 RN982 10 5% 1/20W MF 201

SSD_OC1VR1 RN986 10K 1% 1/20W MF 201
P2V5_NAND1_FB_C
SSD_OC1VR1 CN993 1000PF 10% 16V X7R-1 0201

P2V5_NAND1_FB_RC
SSD_OC1VR1 RN983 6.98K 1% 1/20W MF 201
P2V5_NAND1_FB_RC2
SSD_OC1VR1 RN984 82.5K 0.1% 1/20W MF 0201-1
P2V5_NAND1_FB

SSD_OC1VR1 CN998 10UF 20% 6.3V CER-X6S 0402
SSD_OC1VR1 CN999 10UF 20% 6.3V CER-X6S 0402

=PPVIN_P3V8NAND1
SSD_OC1VR1 CN900 10UF 20% 6.3V CERM-X6S 0402
SSD_OC1VR1 CN901 10UF 20% 6.3V CERM-X6S 0402
SSD_OC1VR1 CN902 0.1UF 20% 16V X6S-CERM 0201
SSD_OC1VR1 CN903 4.7UF 20% 6.3V X6S 0402
SSD_OC1VR1 CN904 4.7UF 20% 6.3V X6S 0402
SSD_OC1VR1 CN905 0.1UF 20% 16V X6S-CERM 0201
SSD_OC1VR1 CRITICAL CN906 150UF 20% 6.3V TANT-POLY CASE-B1S-1

PLACE CN900-CN902 NEAR OCARINA PINS E7/E8
PLACE CN903-CN905 NEAR OCARINA PINS A7/A8
PLACE CN906 NEAR OCARINA PIN B4

OCARINA I2C BASE ADDRESS
STG0: F2
STG1: F0

PPVDD_LDO_NAND1_OCARINA MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=2.5V
SSD_OC1VR1 CN907 0.22UF 20% 6.3V X6S-CERM 0201
TP_NAND1_OCARINA_VCC_DET
=PP1V8_S2_NAND1
SSD_OC1VR1 CN909 0.1UF 10% 6.3V CERM-X5R 0201

NAND1_OCARINA_TDEV1
SSD_OC1VR1 RN902 100K-1%-0.001A 0201
SSD_OC1VR1 RN901 18.2K 0.1% 1/20W TK 0201

NAND1_OCARINA_TDEV2
SSD_OC1VR1 RN904 100K-1%-0.001A 0201
SSD_OC1VR1 RN903 18.2K 0.1% 1/20W TK 0201

UN900
D2499A0P0VLAVBC2
WLCSP
338S00600
CRITICAL
OMIT_TABLE

ATM	F3	
ADDR	D2	NAND1_STG01_ADDR
FORCE_EN	E1	NAND1_FORCE_EN
I2C_SCL	G2	I2C_SMC_NAND_1V8_SCL
I2C_SDA	G3	I2C_SMC_NAND_1V8_SDA
LPBN	F4	NAND1_LPB_L
PFN*	G5	NAND1_PFN_L
PGOOD	G6	NAND1_OCARINA_PGOOD
PMIC_RESET*	D1	
POK1	D3	P2V5_NAND1_PGOOD
POK2	F1	
RESET*	E5	NAND1_RESET_L
SYS_ALIVE	F2	PMU_SYS_ALIVE
VEN1	F5	P2V5_NAND1_EN
VEN2/PMIC_CTRL	E4	TP_NAND1_OCARINA_VEN2
WP*	G4	TP_NAND1_OCARINA_WP_L
TCAL	A4	NAND1_OCARINA_TCAL
VREF	B3	NAND1_OCARINA_VREF
IREF	B2	NAND1_OCARINA_IREF
TDEV1	B1	NAND1_OCARINA_TDEV1
TDEV2	C2	NAND1_OCARINA_TDEV2
VR1_DISCHG	A3	=PP2V5_NAND1
VR2_DISCHG	A1	
BUCK0_FB_DIS	D5	PP0V9_NAND1_FB_DIS
BUCK1_FB_DIS	C5	PP1V2_NAND1_FB_DIS MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V
BUCK0_LX0	F8	
BUCK0_LX0	F7	P0V9_LX0_NAND1 DIDT=TRUE SWITCH_NODE=TRUE
BUCK0_LX1	D8	
BUCK0_LX1	D7	P0V9_LX1_NAND1 DIDT=TRUE SWITCH_NODE=TRUE
BUCK1_LX0	B8	
BUCK1_LX0	B7	P1V2_LX0_NAND1 DIDT=TRUE SWITCH_NODE=TRUE
VSS	A5 B6 A2 C3 C4 D6 D4 E6 E2 F6 E3	
VSS(VSS_BUCK0)	G8 G7	
VSS(VSS_BUCK01)	C8 C7 C6	

SSD_OC1VR1 RN905 200K 0.1% 1/20W TF 0201
SSD_OC1VR1 CN908 0.1UF 10% 6.3V CERM-X5R 0201
SSD_OC1VR1 RN900 8.06K 0.1% 1/20W TK 0201

PP0V9_NAND1 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V
SSD_OC1VR1 RN920 0 5% 1/20W MF 0201

=PP1V2_NAND1
SSD_OC1VR1 RN930 0 5% 1/20W MF 0201
SSD_OC1VR1 CN928 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN929 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN92A 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN92B 20UF 20% 10V X5R 0402

LN921 1UH-20%-4.8A-0.032OHM 1210
LN920 0.47UH-20%-6.7A-0.023OHM 1210
LN930 0.47UH-20%-6.7A-0.023OHM 1210

SSD_OC1VR1 CN920 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN921 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN922 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN923 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN924 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN925 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN926 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN927 20UF 20% 10V X5R 0402
=PP0V9_NAND1_REG

SSD_OC1VR1 CN930 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN931 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN932 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN933 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN934 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN935 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN936 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN937 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN938 20UF 20% 10V X5R 0402
SSD_OC1VR1 CN939 20UF 20% 10V X5R 0402
=PP1V2_NAND1_REG
BOM_COST_GROUP=SSD

=PP1V2_NAND1
SSD_OC1VR1 RN918 47K 1% 1/20W MF 201
SSD_OC1VR1 RN919 47K 1% 1/20W MF 201
SSD_OC1VR1 RN917 47K 1% 1/20W MF 201
NAND1_RESET_L
NAND1_LPB_L
NAND1_PFN_L

=PP0V9_NAND1_REG
PP0V9_NAND1 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=0.9V MAKE_BASE=TRUE
=PP0V9_NAND1_S5E0
=PP0V9_NAND1_S5E1
=PP0V9_NAND1_S5E2
=PP0V9_NAND1_S5E3

=PP2V5_NAND1_REG
PP2V5_NAND1 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=2.5V MAKE_BASE=TRUE
=PP2V5_NAND1

=PP1V2_NAND1_REG
PP1V2_NAND1 MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 VOLTAGE=1.2V MAKE_BASE=TRUE
=PP1V2_NAND1

PAGE TITLE
STORAGE: SSD1 OCARINA & NAND VCC

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PPP000
P4MM
SM
PP
107 97 NAND0_CLK24M_0 1
PLACE_NEAR=UN000.M3:10MM

PPP005
P4MM
SM
PP
107 102 NAND1_CLK24M_0 1
PLACE_NEAR=UN500.M3:15MM

PPP009
P4MM
SM
PP
97 11 PCIE_CLK100M_NAND0_0_N 1

PPP010
P4MM
SM
PP
97 11 PCIE_CLK100M_NAND0_0_P 1

PPP013
P4MM
SM
PP
99 11 PCIE_CLK100M_NAND0_2_N 1

PPP014
P4MM
SM
PP
99 11 PCIE_CLK100M_NAND0_2_P 1

PPP017
P4MM
SM
PP
102 11 PCIE_CLK100M_NAND1_0_N 1

PPP018
P4MM
SM
PP
102 11 PCIE_CLK100M_NAND1_0_P 1

PPP021
P4MM
SM
PP
104 11 PCIE_CLK100M_NAND1_2_N 1

PPP022
P4MM
SM
PP
104 11 PCIE_CLK100M_NAND1_2_P 1

SSD 24M CLOCK TERMINATIONS

8 IN NAND0_CLK24M_R
RP000
15
1 2
5%
1/20W
MF
201
PLACE_NEAR=U0600.B78:10MM

NAND0_CLK24M_0123_R
RP001
49.9
1 2
1%
1/20W
MF
201
NAND0_CLK24M_01
MAKE_BASE=TRUE
NAND0_CLK24M_0
NAND0_CLK24M_1
97 107
98

RP002
49.9
1 2
1%
1/20W
MF
201
NAND0_CLK24M_23
MAKE_BASE=TRUE
NAND0_CLK24M_2
NAND0_CLK24M_3
99
100

8 IN NAND1_CLK24M_R
RP003
15
1 2
5%
1/20W
MF
201
PLACE_NEAR=U0600.B80:10MM

NAND1_CLK24M_0123_R
RP004
49.9
1 2
1%
1/20W
MF
201
NAND1_CLK24M_01
MAKE_BASE=TRUE
NAND1_CLK24M_0
NAND1_CLK24M_1
102 107
103

RP005
49.9
1 2
1%
1/20W
MF
201
NAND1_CLK24M_23
MAKE_BASE=TRUE
NAND1_CLK24M_2
NAND1_CLK24M_3
104
105

NAND CLKREQ SERIES RESISTORS

TODO: RES VALUES NOT FINAL

RP006
0
1 2
5%
1/20W
MF
0201
128 8 IN NAND0_CLKREQ0_L
NAND0_CLKREQ0_R_L OUT 97

RP007
0
1 2
5%
1/20W
MF
0201
128 8 IN NAND0_CLKREQ1_L
NAND0_CLKREQ1_R_L OUT 98

RP008
0
1 2
5%
1/20W
MF
0201
128 8 IN NAND0_CLKREQ2_L
NAND0_CLKREQ2_R_L OUT 99

RP009
0
1 2
5%
1/20W
MF
0201
128 8 IN NAND0_CLKREQ3_L
NAND0_CLKREQ3_R_L OUT 100

RP010
0
1 2
5%
1/20W
MF
0201
128 8 IN NAND1_CLKREQ0_L
NAND1_CLKREQ0_R_L OUT 102

RP011
0
1 2
5%
1/20W
MF
0201
128 8 IN NAND1_CLKREQ1_L
NAND1_CLKREQ1_R_L OUT 103

RP012
0
1 2
5%
1/20W
MF
0201
128 8 IN NAND1_CLKREQ2_L
NAND1_CLKREQ2_R_L OUT 104

RP013
0
1 2
5%
1/20W
MF
0201
128 8 IN NAND1_CLKREQ3_L
NAND1_CLKREQ3_R_L OUT 105

BOM_COST_GROUP=SSD

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STORAGE: SSD SUPPORT

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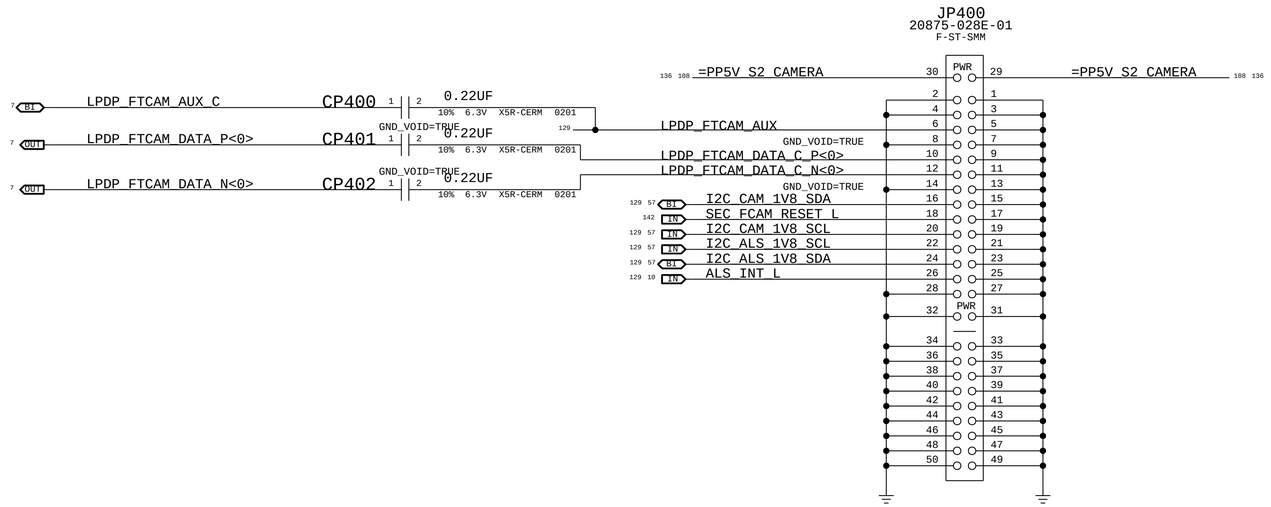

BOM_COST_GROUP=CAMERA

SYNC_MASTER=COLIN SYNC_DATE=09/10/2020

PAGE TITLE
CAMERA: FLEX CONNECTOR

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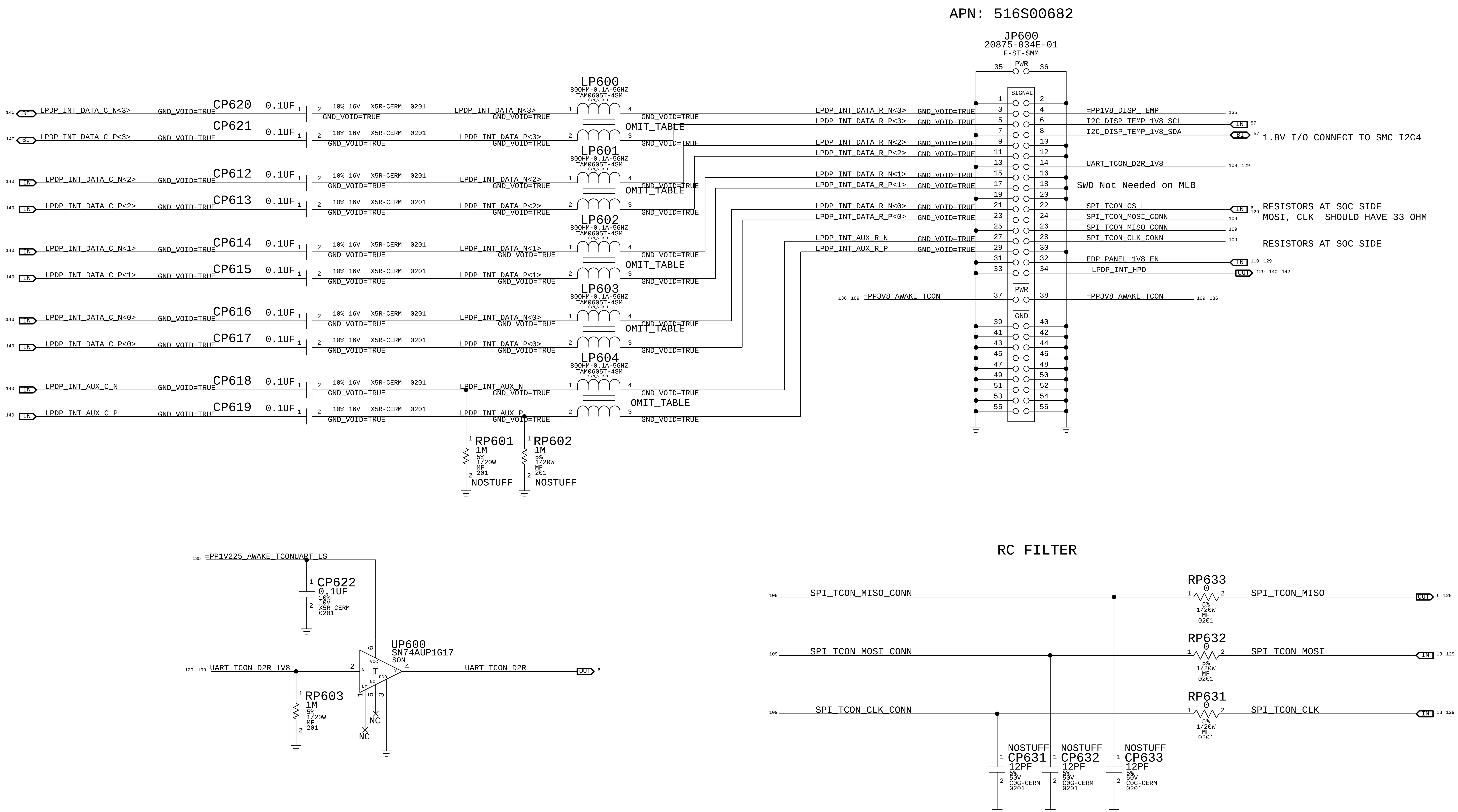

CMC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0943	5	FLTR,NOISE,8 OHMZ,2.6 OHM,100MA,0605	LP600-LP604	CRITICAL	

BOM_COST_GROUP=DISPLAY

PAGE TITLE
DISPLAY CONNECTOR

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*** OK2INTEGRATE ***

135 =PP3V8_AON_LCD_SW_VIN

CP730 1.0UF 20% 6.3V X5R 0201-1

CRITICAL

UP730 TLV758P WSON-THICKSTNCL

IN, OUT, EN, FB, DNC, GND, EPAD

NC

FB_BLKT_2D

RP732 49.9K 1% 1/20W MF 201

RP731 10K 1% 1/20W MF 201

VOUT = VFB * (1 + R1/R2)
VOUT = 0.55 * (1 + 49.9/10)
VOUT = 3.2945

3V29 FEED TO BACKLIGHT

=PPBCON_SW_REG 135

CP731 0.1UF 10% 16V X5R-CERM 0201

CP732 10UF 20% 16V X5R-CERM 0402-7

NOSTUFF
RP730 0 5% 1/16W MF-LF 402

CP710 1.0UF 20% 6.3V X5R 0201-1

CRITICAL

UP701 SLG5AP1564V STDFN

VDD, ON, D, S, PG, GND

NC

3V8 FEED TO MDB

=PPMDB_SW_FET 135

CP718 0.1UF 10% 16V X5R-CERM 0201

CP719 10UF 20% 16V X5R-CERM 0402-7

135 =PP1V8_AON_LCD_SW_VIN

BYPASS=UP710::4MM
CP770 0.1UF 10% 10V X5R-CERM 0201

UP710 SLG4AP44015 STQFN

VDD, GND

43 IN LCD_PWR_EN → LCD_EN_IN

129 106 101 90 83 75 43 IN PMU_SYS_ALIVE → SYS_ALIVE

NC NC NC NC NC NC NC NC NC NC NC NC

LCD_EN_OUT → EDP_PANEL_1V8_EN OUT 109 129

PANEL_3V8_EN → EDP_PANEL_PWR_EN

BLC_1V29_EN → EDP_BKLT_1V29_EN OUT 44 130

CONTROLS 1.29V LDO IN PMIC

PANEL_DISCHARGE → EDP_PANEL_DISCHARGE

RP700 300 5% 1/16W MF-LF 402

PPPANEL_PANEL_DISCHARGE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=4V

QP700 DMN2300UFB4
X2-DFN1006-3-COMBO
SYM_VER_1

RP701 100K 5% 1/20W MF 201

BOM_COST_GROUP=DISPLAY

PAGE TITLE
DISPLAY POWER SEQUENCER

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*** OK2INTEGRATE***

CP800 AND CP801 MUST BE MIRRORED

CP834 AND CP835 MUST BE MIRRORED

=PPBUS_AON_LUXE

NOSTUFF CP800 10UF 20% 16V CER-X6S 0603

NOSTUFF CP801 10UF 20% 16V CER-X6S 0603

CP802 33UF 20% 16V TANT CASE-T POLY-TANT

CP803 33UF 20% 16V TANT CASE-T POLY-TANT

RP850 0.01 MF 1W 0.5% 0612-1-COMBO VOLTAGE=13.1V

PPLUXE_INPUT_R_V

LUXE_ISH_P — RP801 0 5% 1/20W MF 0201 — LUXE_ISH_N

LUXE_ISH_R_P — RP802 0 5% 1/20W MF 0201 — LUXE_ISH_R_N

QP800 BSZ099N06LS5 PG-TSDSON-COMBO

VOLTAGE=10V DIDT=TRUE SWITCH_NODE=TRUE GATE_NODE=TRUE

4LUXE_UG1 — RP832 0 5% 1/10W MF-LF 402

QP801 BSZ099N06LS5 PG-TSDSON-COMBO

RP833 0 5% 1/10W MF-LF 402 — LUXE_UG2 4

PPVOUT_LUXE_XW VOLTAGE=15V

XWP801 SM — PPVOUT_LUXE VOLTAGE=15V

CP830 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP831 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP832 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP833 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP834 0.1UF 20% 50V C0G 1206

CP835 0.1UF 20% 50V C0G 1206

LP800 2.2UH-20%-8.0A-0.0501OHM PIMS052T-SM

PPLUXE_LX1 VOLTAGE=10V SWITCH_NODE=TRUE GATE_NODE=TRUE DIDT=TRUE

PPLUXE_LX2 VOLTAGE=10V SWITCH_NODE=TRUE GATE_NODE=TRUE DIDT=TRUE

QP802 BSZ099N06LS5 PG-TSDSON-COMBO

4LUXE_LG1 — RP831 0 5% 1/10W MF-LF 402 — LUXE_LG1_R

QP803 BSZ099N06LS5 PG-TSDSON-COMBO

RP830 0 5% 1/10W MF-LF 402 — LUXE_LG2 4 — LUXE_LG2_R

DIDT=TRUE SWITCH_NODE=TRUE GATE_NODE=TRUE VOLTAGE=10V

PPLUXE_LG1_S VOLTAGE=1V

RP803 0 5% 1/20W MF 0201 — LUXE_ISL_R_P

RP804 0 5% 1/20W MF 0201 — LUXE_ISL_R_N

RP809 0.01 0.5% 1W MF 0612-1-COMBO — LUXE_ISL_P — LUXE_ISL_N

CP823 0.1UF 10% 25V X5R 402 — LUXE_BT_C1

CP822 0.1UF 10% 25V X5R 402 — LUXE_BT_C2

RP820 4.32K 1% 1/10W MF-LF 402 — LUXE_COMP_R

CP820 0.022UF 20% 16V X7R-CERM 0402

CP821 56PF 5% 50V CERM 0402 — LUXE_AGND

LUXE_COMP

=PP1V2_AWAKE_LUXE

RP860 100K 5% 1/20W MF 201 — LUXE_FAULT

BKLT_BOOST_THROTTLE_LUXE_L

PVOUT_LUXE_R

RP881 0 5% 1/20W MF 0201 — BKLT_BOOST_THROTTLE_R_L (OUT)

OD SIGNAL.
47K PU IS ON THE BCON CONNECTOR PAGE

RP880 0 5% 1/20W MF 0201

CP880 12PF 5% 50V C0G-CERM 0201 NOSTUFF — LUXE_AGND

=PP5V_S2_LUXE

PLACE_NEAR=UP800.C2:5MM

RP805 10 5% 1/16W MF-LF 402

CP870 2.2UF 20% 25V X5R-CERM 0402-1

UP800 RAA209100B WLCSP

C5	VGD	D2	FAULT
C2	VGD	B2	BT_C1
F2	C_VDD	A1	UG1
F3	VDDA	A2	LX1
E2	VIN	A3	LG1
F6	VDDIO	A4	LG2
		A5	LX2
		A6	UG2
		B5	BT_C2
		E6	COMP
		C6	THROTTLE
		D6	FB
D5	VPROG_TEST		
E5	SCL		
E4	SDA		
F5	SCLK		
F4	SDATA		
D3	EN		
C3	BYP		
C4	TEST		
E1	ISH_P		
F1	ISH_N		
C1	ISL_P		
D1	ISL_N		

LUXE_C_VDD VOLTAGE=2.5V

PP5V_S2_LUXE_VDDA VOLTAGE=5V

=PPBUS_AON_LUXE_VIN

=PP1V2_AWAKE_LUXE

CP810 2.2UF 20% 25V X5R-CERM 0402-1

CP811 2.2UF 20% 25V X5R-CERM 0402-1

CP812 2.2UF 20% 25V X5R-CERM 0402-1

LUXE_AGND

XWP800 SM

B4	PGND
B3	PGND
D4	DGND
E3	AGND
B6	AGND
B1	AGND

LUXE_AGND VOLTAGE=0V

=PP5V_S2_LUXE — RP840 100K 5% 1/20W MF 201 NOSTUFF — LUXE_VPROG_TEST

=PP1V2_AWAKE_LUXE

RP842 100K 1/20W 5% MF 201

RP841 100K 1/20W 5% MF 201

RP870 10K 5% 1/20W MF 201 — LUXE_AGND

RP871 10K 5% 1/20W MF 201 — LUXE_BYP

RP872 10K 5% 1/20W MF 201 — LUXE_TEST

I2C_LUXE_DEBUG_SCL (IN)

I2C_LUXE_DEBUG_SDA (BI)

SPMI_DISP_BKLT_CLK (IN)

SPMI_DISP_BKLT_DATA (BI)

BL_PWR_EN (IN) — RP873 0 1/20W 5% MF 0201 — BL_PWR_EN_R

LUXE_AGND

NOSTUFF CP813 33PF 5% 25V NP0-C0G 0201

NOSTUFF CP814 33PF 5% 25V NP0-C0G 0201

NOSTUFF CP815 100PF 5% 50V C0G 0402

NOSTUFF CP816 100PF 5% 50V C0G 0402

CP817 100PF 5% 50V C0G 0402

CP818 100PF 5% 50V C0G 0402

LUXE_AGND

BOM_COST_GROUP=DISPLAY

PAGE TITLE: LUXE LCD Backlight Driver

Apple Inc.

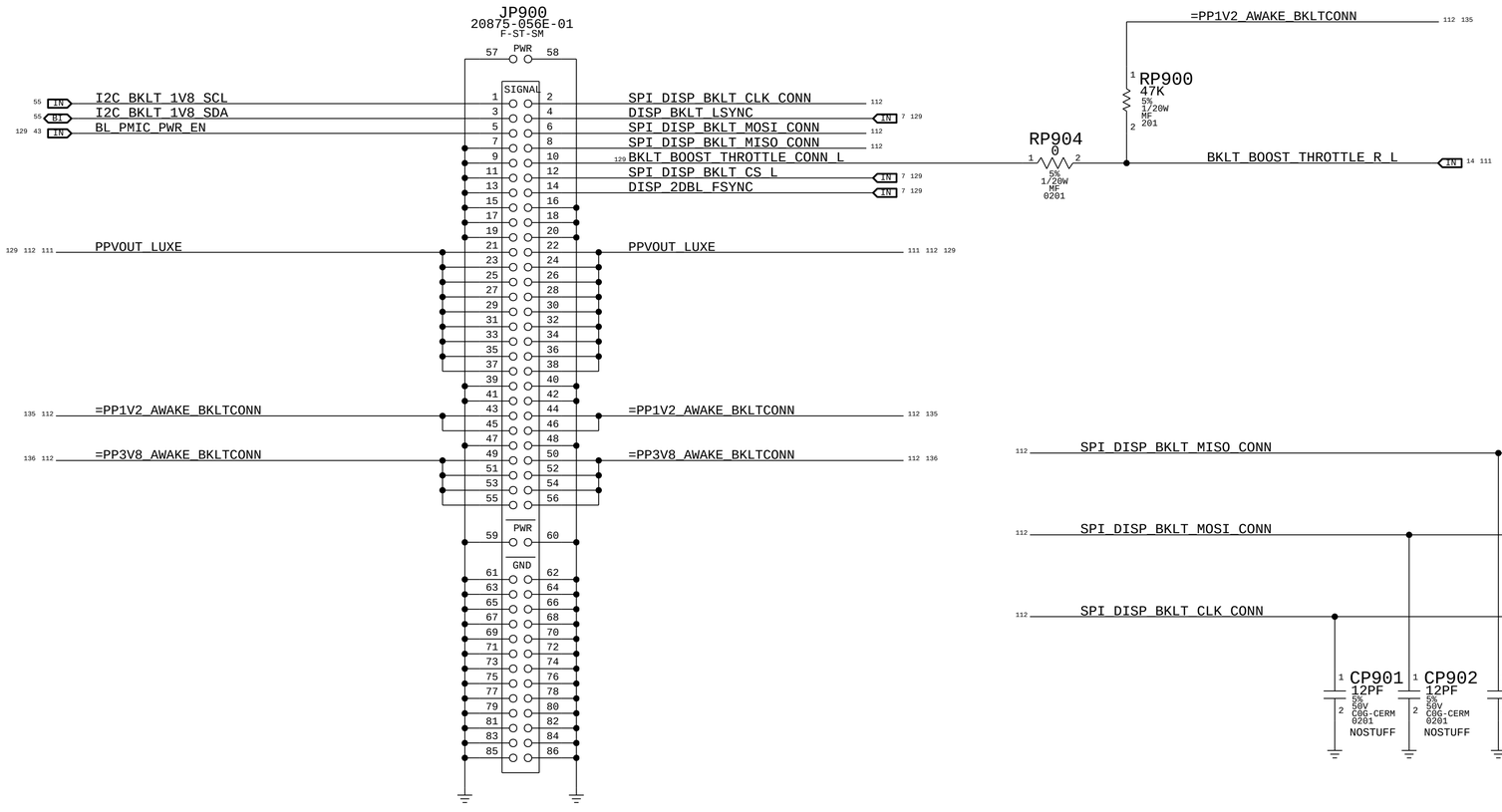
DRAWING NUMBER: 051-05641 SIZE: D

REVISION: 6.33.0

BRANCH:

PAGE: 238 OF 999

SHEET: 111 OF 155



BOM_COST_GROUP=DISPLAY

PAGE TITLE

BCON CONNECTOR

Apple Inc.

DRAWING NUMBER 051-05641 | SIZE D

REVISION 6.33.0

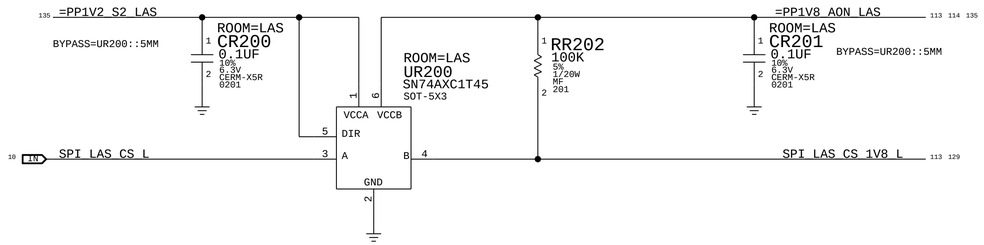
BRANCH

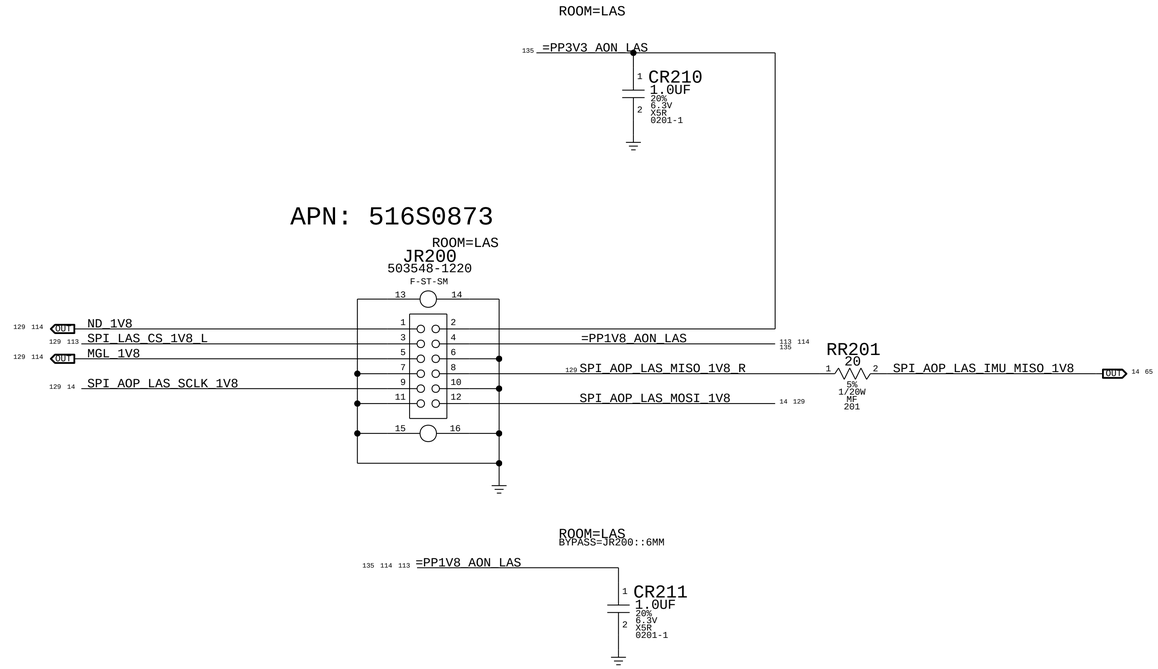
PAGE 239 OF 999

SHEET 112 OF 155

*** OK2INTEGRATE ***

LEVEL TRANSLATION





CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	22UA	1.2MA
1.8 AON	30UA	8 MA
3.3 AON	1UA	10 MA

BOM_COST_GROUP=SOC

SYNC_MASTER=T58S_REF_LAS_LID_0.6.0 SYNC_DATE=09/18/2020

PAGE TITLE
SECDIS: LID ANGLE SENSOR

Apple Inc.

DRAWING NUMBER 051-05641 SIZE D
REVISION 6.33.0
BRANCH
PAGE 242 OF 999
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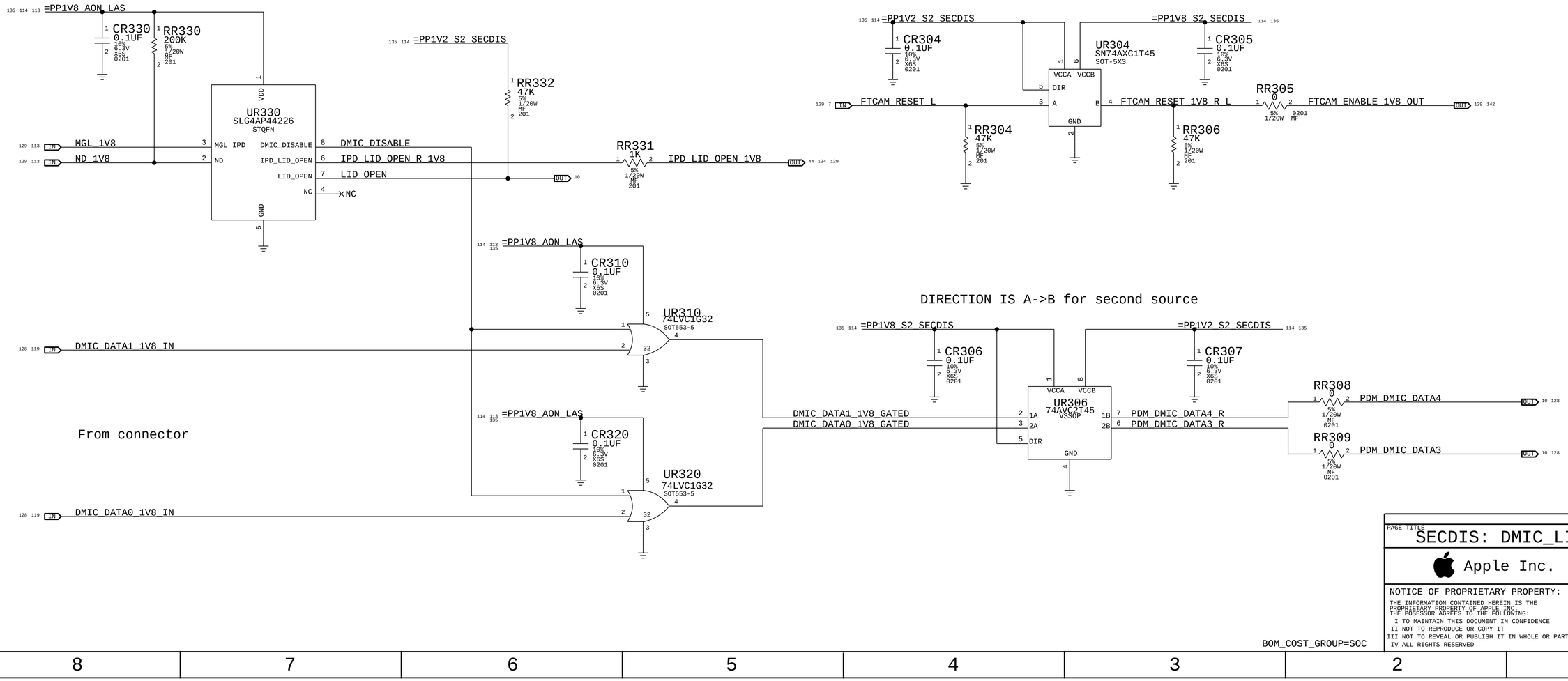
*** OK2INTEGRATE ***

Level Shifter - DMIC & FTCAM



BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: DMIC_LID_CONTROL

Apple Inc.

DRAWING NUMBER 051-05641 | SIZE D
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BRANCH
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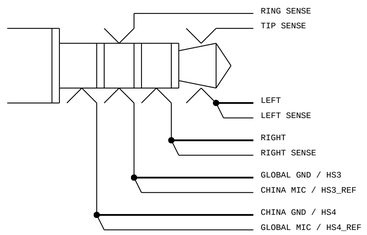
*** OK2INTEGRATE ***

CARLOW CODEC I2C ADDRESS	
ADDR PIN	ADDRESS
0R TO GND	0X48
100K TO GND	0X49
100K TO VDDIO	0X4A
0R TO VDDIO	0X4B <--

AUDIO JACK PINOUT



TO / FROM
AUDIO JACK
CONNECTOR

NOTES:

- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1

- THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
  - VP SUPPLY
  - VCP SUPPLY
  - AUDIO_JACK_LEFT/RIGHT_OUT
  - AUDIO_JACK_GB/CH_GND

- GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR.
  CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.

- VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO
  COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP
  WHEN THE OTHER RAILS GO DOWN)
  VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
  3.1UA (1V8 OFF, RST# LOW)
  TBD (1V8 ON, RST# LOW)
  37UA (1V8 OFF, RST# HIGH)

CARLOW B0 SILICON

BOM_COST_GROUP=AUDIO

PAGE TITLE	AUDIO JACK CODEC
Apple Inc.	DRAWING NUMBER 051-05641 · SIZE D
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*** OK2INTEGRATE ***

AMP A

=PP1V8_AWAKE_SPKRAMP
=PP1V2_AWAKE_SPKRAMP
=PP3V8_AON_A_SPKRAMP (MAX CURRENT EDC = 1A (PER AMP))
=PPBUS_AON_A_SPKRAMP (MAX CURRENT EDC = 4A (PER AMP))

SPKRAMP_A_DREG
CR600 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.E5:5MM)
CR601 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.F3:5MM)
CR602 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.C2:5MM)

CR603 0.1UF 10% 25V X5R 0201 (SPKRAMP_A PLACE_NEAR=UR600.C5:5MM)
CR604 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_A PLACE_NEAR=UR600.C5:10MM)
CR605 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_A PLACE_NEAR=UR600.C5:10MM)
CR606 0.1UF 10% 25V X5R 0201 (SPKRAMP_A PLACE_NEAR=UR600.D5:5MM)
CR607 10UF 20% 10V X5R-CERM 0402-7 (SPKRAMP_A PLACE_NEAR=UR600.D5:10MM)

XWR600 SM (* SEE NOTE)
SPKRAMP_A_PVDD_SNS

SPKRAMP_A_VSENSEP (* SEE NOTE) → SPKRAMP_A IN 118
SPKRAMP_A_VSENSEN → SPKRAMP_A IN 118

UR600 SN012776B0YBH DSBGA — TAWANG B0 — SPKRAMP_A

DREG	C2	
SCL	F2	=I2C_SPKRAMP_A_SCL
SDA	F1	=I2C_SPKRAMP_A_SDA
ADDR	D4	SPKRAMP_A_ADDR
SBCLK	E1	=TDM_SPKRAMP_A_BCLK
FSYNC	D2	=TDM_SPKRAMP_A_FSYNC
SDIN	E2	=TDM_SPKRAMP_A_R2D
SDOUT	D1	=TDM_SPKRAMP_A_D2R
ICC	F5	SPKRAMP_ABC_ICC
BYP_EN	D3	TP_SPKRAMP_A_LV_EN
IRQ*	E3	SPKRAMP_INT_L
SD*	F4	SPKRAMP_RESET_L
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	
PVDD_SNS	C3	
VSNS_P	B1	
VSNS_N	A1	
BST_P	B2	
OUT_P	B3	
OUT_P	A3	
OUT_N	B5	
OUT_N	A5	
BST_N	A2	

(* SEE NOTE)

SPKRAMP_A_TDM_SPKRAMP_A_D2R_R: RR600 33 5% 1/20W MF 201 (PLACE_NEAR=UR600.D1:10MM)
SPKRAMP_A_ICC_R: RR601 33 5% 1/20W MF 201 (PLACE_NEAR=UR600.F5:10MM)

SPKRAMP_A_BOOTP: MIN_LINE_WIDTH=0.1000 → CR608 0.1UF 10% 25V X5R 0201 → SPKRAMP_A_BYPASS=UR600.B2:B3:10MM NO_XNET_CONNECTION=1
SPKRAMP_A_BOOTN: MIN_LINE_WIDTH=0.1000 → CR609 0.1UF 10% 25V X5R 0201 → SPKRAMP_A_BYPASS=UR600.A2:A5:10MM NO_XNET_CONNECTION=1

SPKRAMP_A_OUTP_R: MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE → RR602 0 0% MF 0603 1/4W → MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE → SPKRAMP_A_OUTP (* SEE NOTE) OUT 118 129
SPKRAMP_A_OUTN_R: MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE → RR603 0 0% MF 0603 1/4W → MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE → SPKRAMP_A_OUTN (* SEE NOTE) OUT 118 129

CR610 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR611 220PF 10% 25V X7R-CERM 201 NOSTUFF

RR605 0 5% 1/20W MF 0201 — SPKRAMP_A_ADDR 0x70
RR635 470 5% 1/20W MF 201 — SPKRAMP_B_ADDR 0x72
RR664 470 5% 1/20W MF 201 — SPKRAMP_C_ADDR 0x74

AMP B

=PP1V8_AWAKE_SPKRAMP
=PP1V2_AWAKE_SPKRAMP
=PP3V8_AON_B_SPKRAMP
=PPBUS_AON_B_SPKRAMP

SPKRAMP_B_DREG
CR630 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR630.E5:5MM)
CR631 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR630.F3:5MM)
CR632 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR630.C2:5MM)

CR633 0.1UF 10% 25V X5R 0201 (SPKRAMP_B PLACE_NEAR=UR630.C5:5MM)
CR634 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_B PLACE_NEAR=UR630.C5:10MM)
CR635 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_B PLACE_NEAR=UR630.C5:10MM)
CR636 0.1UF 10% 25V X5R 0201 (SPKRAMP_B PLACE_NEAR=UR630.D5:5MM)
CR637 10UF 20% 10V X5R-CERM 0402-7 (SPKRAMP_B PLACE_NEAR=UR630.D5:10MM)

XWR601 SM (* SEE NOTE)
SPKRAMP_B_PVDD_SNS

SPKRAMP_B_VSENSEP (* SEE NOTE) → SPKRAMP_B IN 118
SPKRAMP_B_VSENSEN → SPKRAMP_B IN 118

UR630 SN012776B0YBH DSBGA — TAWANG B0 — SPKRAMP_B

DREG	C2	
SCL	F2	=I2C_SPKRAMP_B_SCL
SDA	F1	=I2C_SPKRAMP_B_SDA
ADDR	D4	SPKRAMP_B_ADDR
SBCLK	E1	=TDM_SPKRAMP_B_BCLK
FSYNC	D2	=TDM_SPKRAMP_B_FSYNC
SDIN	E2	=TDM_SPKRAMP_B_R2D
SDOUT	D1	=TDM_SPKRAMP_B_D2R
ICC	F5	SPKRAMP_ABC_ICC
BYP_EN	D3	TP_SPKRAMP_B_LV_EN
IRQ*	E3	SPKRAMP_INT_L
SD*	F4	SPKRAMP_RESET_L
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	
PVDD_SNS	C3	
VSNS_P	B1	
VSNS_N	A1	
BST_P	B2	
OUT_P	B3	
OUT_P	A3	
OUT_N	B5	
OUT_N	A5	
BST_N	A2	

(* SEE NOTE)

SPKRAMP_B_TDM_SPKRAMP_B_D2R_R: RR630 33 5% 1/20W MF 201 (PLACE_NEAR=UR630.D1:10MM)
SPKRAMP_B_ICC_R: RR631 33 5% 1/20W MF 201 (PLACE_NEAR=UR630.F5:10MM)

SPKRAMP_B_BOOTP: MIN_LINE_WIDTH=0.1000 → CR638 0.1UF 10% 25V X5R 0201 → SPKRAMP_B_BYPASS=UR630.B2:B3:10MM NO_XNET_CONNECTION=1
SPKRAMP_B_BOOTN: MIN_LINE_WIDTH=0.1000 → CR639 0.1UF 10% 25V X5R 0201 → SPKRAMP_B_BYPASS=UR630.A2:A5:10MM NO_XNET_CONNECTION=1

SPKRAMP_B_OUTP_R: MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE → RR632 0 0% MF 0603 1/4W → MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE → SPKRAMP_B_OUTP (* SEE NOTE) OUT 118 129
SPKRAMP_B_OUTN_R: MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE → RR633 0 0% MF 0603 1/4W → MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE → SPKRAMP_B_OUTN (* SEE NOTE) OUT 118 129

CR640 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR641 220PF 10% 25V X7R-CERM 201 NOSTUFF

=PP1V2_AWAKE_IO
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR691 47K 5% 1/20W MF 201 (NOSTUFF)
RR692 47K 5% 1/20W MF 201

THIS RESISTOR TIES ICC SIGNAL BETWEEN AMPS A,B,C AND AMPS D,E,F:
0R --> GLOBAL ICC (ABCDEF)
DNE --> LOCAL ICC (ABC, DEF)

SPKRAMP_ICC_GB
RR693 0 5% 1/20W MF 0201
SPKRAMP_ABC_ICC ↔ SPKRAMP_DEF_ICC (BI 117 128)
SPKRAMP_ICC_GB

AMP C

=PP1V8_AWAKE_SPKRAMP
=PP1V2_AWAKE_SPKRAMP
=PP3V8_AON_C_SPKRAMP
=PPBUS_AON_C_SPKRAMP

SPKRAMP_C_DREG
CR660 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR660.E5:5MM)
CR661 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR660.F3:5MM)
CR662 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR660.C2:5MM)

CR663 0.1UF 10% 25V X5R 0201 (SPKRAMP_C PLACE_NEAR=UR660.C5:5MM)
CR664 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_C PLACE_NEAR=UR660.C5:10MM)
CR665 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_C PLACE_NEAR=UR660.C5:10MM)
CR666 0.1UF 10% 25V X5R 0201 (SPKRAMP_C PLACE_NEAR=UR660.D5:5MM)
CR667 10UF 20% 10V X5R-CERM 0402-7 (SPKRAMP_C PLACE_NEAR=UR660.D5:10MM)

XWR602 SM (* SEE NOTE)
SPKRAMP_C_PVDD_SNS

SPKRAMP_C_VSENSEP (* SEE NOTE) → SPKRAMP_C IN 118
SPKRAMP_C_VSENSEN → SPKRAMP_C IN 118

UR660 SN012776B0YBH DSBGA — TAWANG B0 — SPKRAMP_C

DREG	C2	
SCL	F2	=I2C_SPKRAMP_C_SCL
SDA	F1	=I2C_SPKRAMP_C_SDA
ADDR	D4	SPKRAMP_C_ADDR
SBCLK	E1	=TDM_SPKRAMP_C_BCLK
FSYNC	D2	=TDM_SPKRAMP_C_FSYNC
SDIN	E2	=TDM_SPKRAMP_C_R2D
SDOUT	D1	=TDM_SPKRAMP_C_D2R
ICC	F5	SPKRAMP_ABC_ICC
BYP_EN	D3	TP_SPKRAMP_C_LV_EN
IRQ*	E3	SPKRAMP_INT_L
SD*	F4	SPKRAMP_RESET_L
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	
PVDD_SNS	C3	
VSNS_P	B1	
VSNS_N	A1	
BST_P	B2	
OUT_P	B3	
OUT_P	A3	
OUT_N	B5	
OUT_N	A5	
BST_N	A2	

(* SEE NOTE)

SPKRAMP_C_TDM_SPKRAMP_C_D2R_R: RR660 33 5% 1/20W MF 201 (PLACE_NEAR=UR660.D1:10MM)
SPKRAMP_C_ICC_R: RR661 33 5% 1/20W MF 201 (PLACE_NEAR=UR660.F5:10MM)

SPKRAMP_C_BOOTP: MIN_LINE_WIDTH=0.1000 → CR668 0.1UF 10% 25V X5R 0201 → SPKRAMP_C_BYPASS=UR660.B2:B3:10MM NO_XNET_CONNECTION=1
SPKRAMP_C_BOOTN: MIN_LINE_WIDTH=0.1000 → CR669 0.1UF 10% 25V X5R 0201 → SPKRAMP_C_BYPASS=UR660.A2:A5:10MM NO_XNET_CONNECTION=1

SPKRAMP_C_OUTP_R: MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE → RR662 0 0% MF 0603 1/4W → MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE → SPKRAMP_C_OUTP (* SEE NOTE) OUT 118 129
SPKRAMP_C_OUTN_R: MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE → RR663 0 0% MF 0603 1/4W → MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE → SPKRAMP_C_OUTN (* SEE NOTE) OUT 118 129

CR670 220PF 10% 25V X7R-CERM 201 NOSTUFF
CR671 220PF 10% 25V X7R-CERM 201 NOSTUFF

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (1/2)

Apple Inc.

DRAWING NUMBER: 051-05641 SIZE: D
REVISION: 6.33.0
BRANCH:
PAGE: 246 OF 999
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*** OK2INTEGRATE ***

AMP D

=PP1V8_AWAKE_SPKRAMP
=PP1V2_AWAKE_SPKRAMP
=PP3V8_AON_D_SPKRAMP (MAX CURRENT EDC = 1A (PER AMP))
=PPBUS_AON_D_SPKRAMP (MAX CURRENT EDC = 4A (PER AMP))

CR700 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.E5:5MM
CR701 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.F3:5MM
CR702 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.C2:5MM
SPKRAMP_D_DREG

CR703 0.1UF 10% 25V X5R 0201 — SPKRAMP_D PLACE_NEAR=UR700.C5:5MM
CR704 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_D PLACE_NEAR=UR700.C5:10MM
CR705 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_D PLACE_NEAR=UR700.C5:10MM
CR706 0.1UF 10% 25V X5R 0201 — SPKRAMP_D PLACE_NEAR=UR700.D5:5MM
CR707 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_D PLACE_NEAR=UR700.D5:10MM

XWR700 SM — SPKRAMP_D — * SEE NOTE

SPKRAMP_D_PVDD_SNS

SPKRAMP_D_VSENSEP — * SEE NOTE — SPKRAMP_D IN 118
SPKRAMP_D_VSENSEN — SPKRAMP_D IN 118

UR700 SN012776B0YBH DSBGA — SPKRAMP_D — TAWANG B0

DREG	C2	
PVDD_SNS	C3	
VSNS_P	B1	
VSNS_N	A1	
BST_P	B2	
OUT_P	B3	
OUT_P	A3	
OUT_N	B5	
OUT_N	A5	
BST_N	A2	
SCL	F2	
SDA	F1	
ADDR	D4	
SBCLK	E1	
FSYNC	D2	
SDIN	E2	
SDOUT	D1	
ICC	F5	
BYP_EN	D3	
IRQ*	E3	
SD*	F4	
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	

* SEE NOTE

SPKRAMP_D_BOOTP — MIN_LINE_WIDTH=0.1000 — CR708 0.1UF 10% 25V X5R 0201
SPKRAMP_D_OUTP_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_D_OUTN_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — CR709 0.1UF 10% 25V X5R 0201
SPKRAMP_D_BOOTN — MIN_LINE_WIDTH=0.1000
SPKRAMP_D BYPASS=UR700.B2:B3:10MM NO_XNET_CONNECTION=1

RR702 0 0% MF 1/4W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE
RR703 0 0% MF 1/4W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE

SPKRAMP_D_OUTP — * SEE NOTE — SPKRAMP_D OUT 118 129
SPKRAMP_D_OUTN — * SEE NOTE — SPKRAMP_D OUT 118 129

CR710 220PF 10% 25V X7R-CERM 201 — NOSTUFF
CR711 220PF 10% 25V X7R-CERM 201 — NOSTUFF

=I2C_SPKRAMP_D_SCL — SPKRAMP_D IN
=I2C_SPKRAMP_D_SDA — SPKRAMP_D BI
SPKRAMP_D_ADDR
=TDM_SPKRAMP_D_BCLK — SPKRAMP_D IN
=TDM_SPKRAMP_D_FSYNC — SPKRAMP_D IN
=TDM_SPKRAMP_D_R2D — SPKRAMP_D IN
=TDM_SPKRAMP_D_D2R — SPKRAMP_D OUT
SPKRAMP_DEF_ICC_R — SPKRAMP_D RR700 33 5% 1/20W MF 201 — TDM_SPKRAMP_D_D2R_R
SPKRAMP_D_ICC_R — SPKRAMP_D RR701 33 5% 1/20W MF 201 — PLACE_NEAR=UR700.D1:10MM
TP_SPKRAMP_D_LV_EN — PLACE_NEAR=UR700.F5:10MM
SPKRAMP_INT_L — SPKRAMP_D OUT
SPKRAMP_RESET_L — SPKRAMP_D IN

=PP1V8_AWAKE_SPKRAMP
RR705 2.2K 5% 1/20W MF 201 — SPKRAMP_D_ADDR 0X76
RR734 2.2K 5% 1/20W MF 201 — SPKRAMP_E_ADDR 0X78
RR765 10K 5% 1/20W MF 201 — SPKRAMP_F_ADDR 0X7A

=PP1V8_AWAKE_SPKRAMP
SPKRAMP_DEF_ICC
RR706 0 5% 1/20W MF 0201 — SPKRAMP_DEF_ICC_R
RR707 0 5% 1/20W MF 0201 — NOSTUFF

RR706 TO REDUCE STUB LENGTH FOR LOCAL ICC OPERATION. RR707 PROVIDES THE OPTION TO GND FLOATING SPKRAMP_DEF_ICC TRACE

AMP E

=PP1V8_AWAKE_SPKRAMP
=PP1V2_AWAKE_SPKRAMP
=PP3V8_AON_E_SPKRAMP
=PPBUS_AON_E_SPKRAMP

CR730 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.E5:5MM
CR731 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.F3:5MM
CR732 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.C2:5MM
SPKRAMP_E_DREG

CR733 0.1UF 10% 25V X5R 0201 — SPKRAMP_E PLACE_NEAR=UR730.C5:5MM
CR734 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_E PLACE_NEAR=UR730.C5:10MM
CR735 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_E PLACE_NEAR=UR730.C5:10MM
CR736 0.1UF 10% 25V X5R 0201 — SPKRAMP_E PLACE_NEAR=UR730.D5:5MM
CR737 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_E PLACE_NEAR=UR730.D5:10MM

XWR701 SM — SPKRAMP_E — * SEE NOTE

SPKRAMP_E_PVDD_SNS

SPKRAMP_E_VSENSEP — * SEE NOTE — SPKRAMP_E IN 118
SPKRAMP_E_VSENSEN — SPKRAMP_E IN 118

UR730 SN012776B0YBH DSBGA — SPKRAMP_E — TAWANG B0

DREG	C2	
PVDD_SNS	C3	
VSNS_P	B1	
VSNS_N	A1	
BST_P	B2	
OUT_P	B3	
OUT_P	A3	
OUT_N	B5	
OUT_N	A5	
BST_N	A2	
SCL	F2	
SDA	F1	
ADDR	D4	
SBCLK	E1	
FSYNC	D2	
SDIN	E2	
SDOUT	D1	
ICC	F5	
BYP_EN	D3	
IRQ*	E3	
SD*	F4	
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	

* SEE NOTE

SPKRAMP_E_BOOTP — MIN_LINE_WIDTH=0.1000 — CR738 0.1UF 10% 25V X5R 0201
SPKRAMP_E_OUTP_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_E_OUTN_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — CR739 0.1UF 10% 25V X5R 0201
SPKRAMP_E_BOOTN — MIN_LINE_WIDTH=0.1000
SPKRAMP_E BYPASS=UR730.B2:B3:10MM NO_XNET_CONNECTION=1

RR732 0 0% MF 1/4W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE
RR733 0 0% MF 1/4W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE

SPKRAMP_E_OUTP — * SEE NOTE — SPKRAMP_E OUT 118 129
SPKRAMP_E_OUTN — * SEE NOTE — SPKRAMP_E OUT 118 129

CR740 220PF 10% 25V X7R-CERM 201 — NOSTUFF
CR741 220PF 10% 25V X7R-CERM 201 — NOSTUFF

=I2C_SPKRAMP_E_SCL — SPKRAMP_E IN
=I2C_SPKRAMP_E_SDA — SPKRAMP_E BI
SPKRAMP_E_ADDR
=TDM_SPKRAMP_E_BCLK — SPKRAMP_E IN
=TDM_SPKRAMP_E_FSYNC — SPKRAMP_E IN
=TDM_SPKRAMP_E_R2D — SPKRAMP_E IN
=TDM_SPKRAMP_E_D2R — SPKRAMP_E OUT
SPKRAMP_DEF_ICC_R — SPKRAMP_E RR730 33 5% 1/20W MF 201 — TDM_SPKRAMP_E_D2R_R
SPKRAMP_E_ICC_R — SPKRAMP_E RR731 33 5% 1/20W MF 201 — PLACE_NEAR=UR730.D1:10MM
TP_SPKRAMP_E_LV_EN — PLACE_NEAR=UR730.F5:10MM
SPKRAMP_INT_L — SPKRAMP_E OUT
SPKRAMP_RESET_L — SPKRAMP_E IN

AMP F

=PP1V8_AWAKE_SPKRAMP
=PP1V2_AWAKE_SPKRAMP
=PP3V8_AON_F_SPKRAMP
=PPBUS_AON_F_SPKRAMP

CR760 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.E5:5MM
CR761 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.F3:5MM
CR762 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.C2:5MM
SPKRAMP_F_DREG

CR763 0.1UF 10% 25V X5R 0201 — SPKRAMP_F PLACE_NEAR=UR760.C5:5MM
CR764 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_F PLACE_NEAR=UR760.C5:10MM
CR765 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_F PLACE_NEAR=UR760.C5:10MM
CR766 0.1UF 10% 25V X5R 0201 — SPKRAMP_F PLACE_NEAR=UR760.D5:5MM
CR767 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_F PLACE_NEAR=UR760.D5:10MM

XWR702 SM — SPKRAMP_F — * SEE NOTE

SPKRAMP_F_PVDD_SNS

SPKRAMP_F_VSENSEP — * SEE NOTE — SPKRAMP_F IN 118
SPKRAMP_F_VSENSEN — SPKRAMP_F IN 118

UR760 SN012776B0YBH DSBGA — SPKRAMP_F — TAWANG B0

DREG	C2	
PVDD_SNS	C3	
VSNS_P	B1	
VSNS_N	A1	
BST_P	B2	
OUT_P	B3	
OUT_P	A3	
OUT_N	B5	
OUT_N	A5	
BST_N	A2	
SCL	F2	
SDA	F1	
ADDR	D4	
SBCLK	E1	
FSYNC	D2	
SDIN	E2	
SDOUT	D1	
ICC	F5	
BYP_EN	D3	
IRQ*	E3	
SD*	F4	
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	

* SEE NOTE

SPKRAMP_F_BOOTP — MIN_LINE_WIDTH=0.1000 — CR768 0.1UF 10% 25V X5R 0201
SPKRAMP_F_OUTP_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE
SPKRAMP_F_OUTN_R — MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE — CR769 0.1UF 10% 25V X5R 0201
SPKRAMP_F_BOOTN — MIN_LINE_WIDTH=0.1000
SPKRAMP_F BYPASS=UR760.B2:B3:10MM NO_XNET_CONNECTION=1

RR762 0 0% MF 1/4W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE
RR763 0 0% MF 1/4W 0603 — MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000 SWITCH_NODE=TRUE

SPKRAMP_F_OUTP — * SEE NOTE — SPKRAMP_F OUT 118 129
SPKRAMP_F_OUTN — * SEE NOTE — SPKRAMP_F OUT 118 129

CR770 220PF 10% 25V X7R-CERM 201 — NOSTUFF
CR771 220PF 10% 25V X7R-CERM 201 — NOSTUFF

=I2C_SPKRAMP_F_SCL — SPKRAMP_F IN
=I2C_SPKRAMP_F_SDA — SPKRAMP_F BI
SPKRAMP_F_ADDR
=TDM_SPKRAMP_F_BCLK — SPKRAMP_F IN
=TDM_SPKRAMP_F_FSYNC — SPKRAMP_F IN
=TDM_SPKRAMP_F_R2D — SPKRAMP_F IN
=TDM_SPKRAMP_F_D2R — SPKRAMP_F OUT
SPKRAMP_DEF_ICC_R — SPKRAMP_F RR760 33 5% 1/20W MF 201 — TDM_SPKRAMP_F_D2R_R
SPKRAMP_F_ICC_R — SPKRAMP_F RR761 33 5% 1/20W MF 201 — PLACE_NEAR=UR760.D1:10MM
TP_SPKRAMP_F_LV_EN — PLACE_NEAR=UR760.F5:10MM
SPKRAMP_INT_L — SPKRAMP_F OUT
SPKRAMP_RESET_L — SPKRAMP_F IN

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (2/2)

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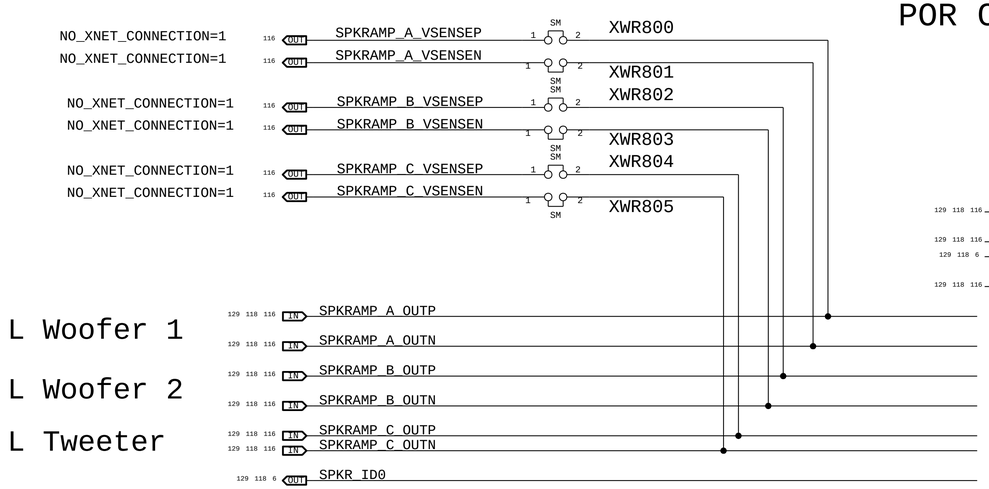
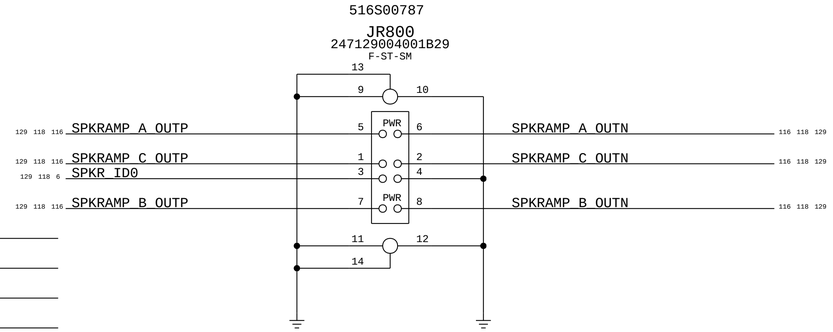
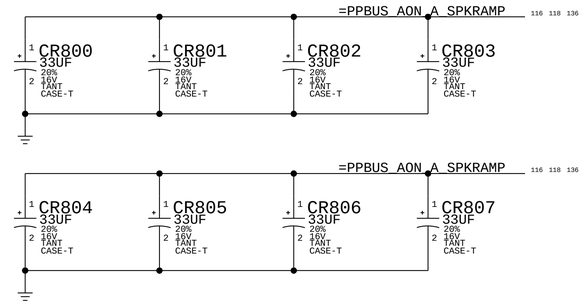
LEFT AUDIO SPEAKER CONNECTOR



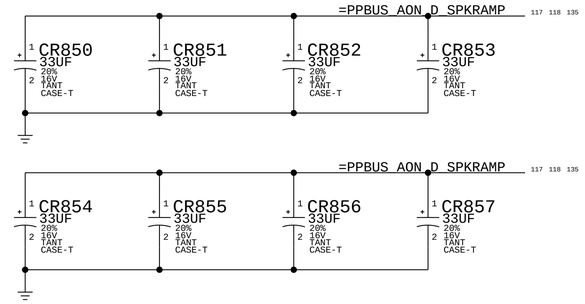
J152 CONN APN:518S00818 FOR P0.
J316 CONN APN:516S00690 FOR P1.
POR COST CONN APN:516S00787 FOR P1C.P2S



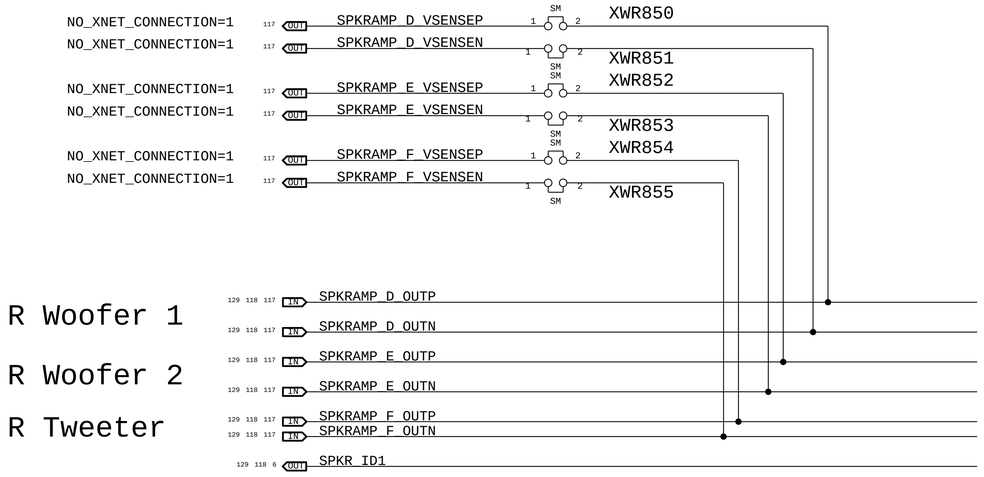
LEFT AMPLIFIERS BULK CAPACITANCE

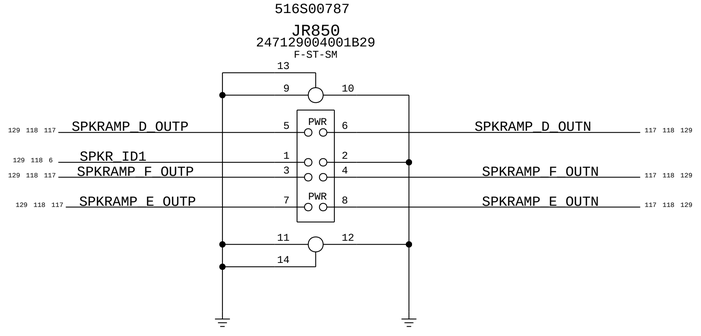


RIGHT AMPLIFIERS BULK CAPACITANCE

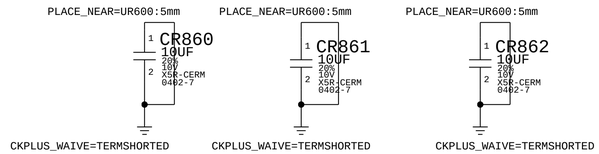


RIGHT AUDIO SPEAKER CONNECTOR





DUMMY 0201 CAPS



BOM_COST_GROUP=AUDIO

SYNC_MASTER=RAYMOND

PAGE TITLE: AUDIO CONNECTORS: AMPS

Apple Inc.

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Digital Mic Flex Connector

APN: 518S0818

JR940
FF14A-6C-R11DL-B-3H
F-RT-SM

- 1 AUD_DMIC0_CLK_CONN (119 129)
- 2 AUD_DMIC0_DATA_CONN (119 129)
- 3 PP1V8_DMIC
- 4 AUD_DMIC1_CLK_CONN (119 129)
- 5 AUD_DMIC1_DATA_CONN (119 129)
- 6
- 7
- 8

LR940
FERR-470-OHM
0201
1 → 2 =PP1V8_S2_DMIC (135)

CR940
1UF
20%
16V
CER-X5R
0201

TODO: Check if zero ohms between connector an SECDIS are required

129 119	AUD_DMIC0_CLK_CONN	MAKE_BASE=TRUE	=	DMIC_CLK0_1V8_OUT	114
129 119	AUD_DMIC0_DATA_CONN	MAKE_BASE=TRUE	=	DMIC_DATA0_1V8_IN	114 128
129 119	AUD_DMIC1_CLK_CONN	MAKE_BASE=TRUE	=	DMIC_CLK1_1V8_OUT	114
129 119	AUD_DMIC1_DATA_CONN	MAKE_BASE=TRUE	=	DMIC_DATA1_1V8_IN	114 128

Audio Jack Flex Connector

115	IN	AUDIO_JACK_LEFT_OUT	CRITICAL FLR901 1500OHM-0.4A-0.8OHM 0402	AUD_CONN_HP_LEFT MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1000
115	IN	AUDIO_JACK_RIGHT_OUT	CRITICAL FLR900 1500OHM-0.4A-0.8OHM 0402	AUD_CONN_HP_RIGHT MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1000
115	OUT	AUDIO_JACK_GB_GND	CRITICAL FLR903 1500OHM-0.4A-0.8OHM 0402	AUD_CONN_RING2 MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.1000
115	OUT	AUDIO_JACK_CH_GND	CRITICAL FLR905 1500OHM-0.4A-0.8OHM 0402	129 119 AUD_CONN_SLEEVE MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.1000
115	OUT	AUDIO_JACK_LEFT_SNS	CRITICAL FLR906 1500OHM-0.4A-0.8OHM 0402	AUD_CONN_HP_SENSE_L
115	OUT	AUDIO_JACK_RIGHT_SNS	CRITICAL FLR907 1500OHM-0.4A-0.8OHM 0402	AUD_CONN_HP_SENSE_R
115	OUT	AUDIO_JACK_TIP_SNS	RR900 2.0K 5% 1/20W MF 201	AUD_CONN_TIP_SENSE
115	OUT	AUDIO_JACK_RING_SNS	RR901 2.0K 5% 1/20W MF 201	AUD_CONN_RING_SENSE
115	OUT	AUDIO_JACK_GB_MIC	CRITICAL FLR902 1500OHM-0.4A-0.8OHM 0402	AUD_CONN_SLEEVE_XW MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
115	OUT	AUDIO_JACK_CH_MIC	CRITICAL FLR904 1500OHM-0.4A-0.8OHM 0402	129 AUD_CONN_RING2_XW MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

PART_NUMBER=516S1181

JR900
AA25D-S016VA1
F-ST-SM

- 18
- 17
- 1 AUD_CONN_HP_LEFT (119 129)
- 2
- 3 AUD_CONN_HP_RIGHT (119 129)
- 4
- 5 AUD_CONN_RING2 (119 129)
- 6
- 7
- 8
- 9 AUD_CONN_SLEEVE (119 129)
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 19
- 20

APN: 516S1181 ,MATINGM PLUG APN:516S1180
SAME AS J214

BOM_COST_GROUP=AUDIO

LAST CHANGE: Wed Feb 18 17:12:24 2015

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Audio Flex Connectors

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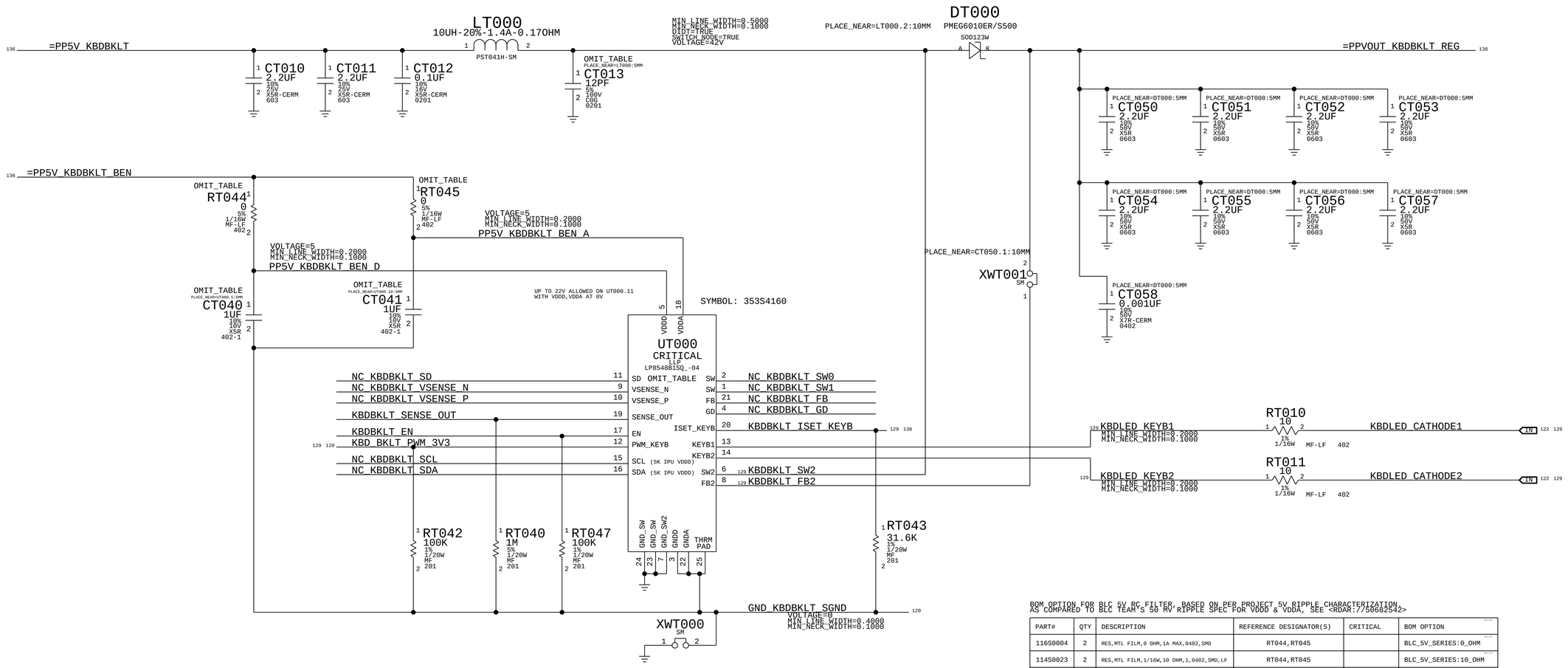
*** OK2INTEGRATE ***

BEN IC: KEYBOARD LED DRIVER

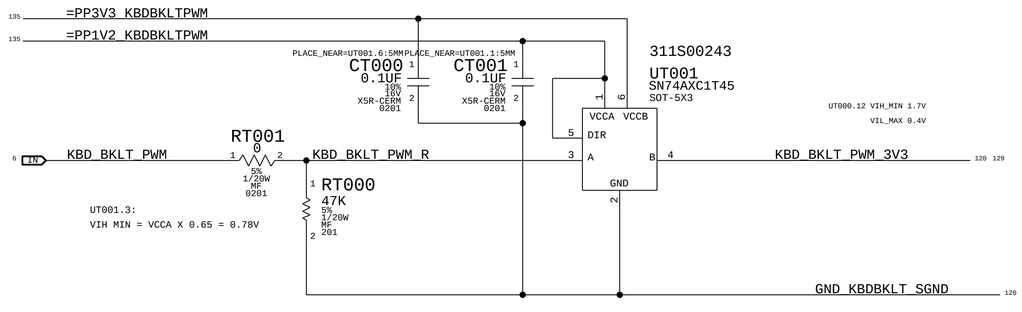


BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION, AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR:/750682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	RT044,RT045		BLC_5V_SERIES:0_OHM
114S0023	2	RES,MTL FILM,1/16W,10 OHM,1,0402,SMD,LF	RT044,RT045		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CT040,CT041		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CT040,CT041		BLC_5V_CAP:4P7_UF

KEYBOARD BKLT PWM LEVEL-SHIFTER

UT001.4: VOH_MIN = 2.3V
VOL_MAX = 0.1V @ PWM_KEYB I_MAX OF 1UA



BEN IC VERSION 4 VS 6 DEPENDS ON WHICH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01615	1	IC,LP8548B1-04,DC/DC CVTR,BST,AIDU,QFN-24	UT000		BLC_BEN_IC:V4
353S01685	1	IC,LP8548B1-06,DC/DC CVTR,BST,QFN24	UT000		BLC_BEN_IC:V6

ALTERNATE PART FOR BEN IC VERSION 4

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S4160	353S01615	BLC_BEN_IC:V4	ANY	RECOMMENDED BY LOUISA

KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CT013		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

PAGE TITLE: BEN: KEYBD BKLT

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*** OK2PLACE ***

TO/FROM TRACKPAD

I2C_KBD_SCL — PLACE_NEAR=JT400.8:10MM — RT110 33 1% 1/20W MF 201 — DZT110 5.5V-0.28PF 0201-THICKSTNCL — CKPLUS_WAIVE=I2C_PULLUP — IOXP_I2C_SCL

I2C_KBD_SDA — PLACE_NEAR=JT400.9:10MM — RT111 33 1% 1/20W MF 201 — DZT111 5.5V-0.28PF 0201-THICKSTNCL — CKPLUS_WAIVE=I2C_PULLUP — IOXP_I2C_SDA

KBD_INT_L — PLACE_NEAR=JT400.9:10MM — RT112 33 1% 1/20W MF 201 — DZT112 5.5V-0.28PF 0201-THICKSTNCL — IOXP2_INT_L

KEYBAORD IOX1

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3

=PP1V83V3_S2_KBDIOXI2C — CT110 1.0UF 20% 6.3V X5R 0201-1 138S0692 — CT112 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8

=PP1V8_S2_KBD — CT113 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 — CT114 10UF 20% 10V X5R-CERM 0402-7

IOX1 DOESN'T SEND THE INTERRUPT INSTEAD, IOX2 SENDS INT WHEN A KEY IS PRESSED

IOXP1_INT_L → INT*

IOXP1_RESET_L → RESET* — CT111 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

UT101 PCAL6416A HWQFN

ADDR, SCL, SDA, VDD/I2C-BUS, VDD/P, VSS, THRM PAD

311S0665
WRITE: 0X40
READ: 0X41

P0_0	KBD_DRIVE_Y0
P0_1	KBD_DRIVE_Y1
P0_2	KBD_DRIVE_Y2
P0_3	KBD_DRIVE_Y3
P0_4	KBD_DRIVE_Y4
P0_5	KBD_DRIVE_Y5
P0_6	KBD_DRIVE_Y6
P0_7	KBD_DRIVE_Y7
P1_0	KBD_DRIVE_Y8
P1_1	KBD_DRIVE_Y9
P1_2	KBD_DRIVE_Y10
P1_3	KBD_DRIVE_Y11
P1_4	NC
P1_5	KBD_ID_DETECT2
P1_6	KBD_ID_DETECT1
P1_7	CAPSLOCK_LED_EN

ADD 4X NEW IO_Y8,Y9,Y10,Y11 FOR 3314/316 AND 34-PIN KBD
CONNECT THE NEW IO FROM KBD ZIF CONN TO NEARBY ESD DIODES

KEYBAORD IOX2

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3

=PP1V83V3_S2_KBDIOXI2C — RT121 100K 5% 1/20W MF 201 — CT120 1.0UF 20% 6.3V X5R 0201-1 138S0692 — CT121 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8

=PP1V8_S2_KBD — CT122 0.1UF 10% 10V X5R-CERM 0201

IOXP2_ADDR → ADDR

IOXP2_RESET_L → RESET* — CT123 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

UT102 PCAL6416A HWQFN

ADDR, SCL, SDA, VDD/I2C-BUS, VDD/P, VSS, THRM PAD

311S0665
WRITE: 0X42
READ: 0X43

P0_0	KBD_SENSE_X0
P0_1	KBD_SENSE_X1
P0_2	KBD_SENSE_X2
P0_3	KBD_SENSE_X3
P0_4	KBD_SENSE_X4
P0_5	KBD_SENSE_X5
P0_6	KBD_SENSE_X6
P0_7	KBD_SENSE_X7
P1_0	KBD_SENSE_X8
P1_1	KBD_SENSE_X9
P1_2	KBD_SENSE_X10
P1_3	KBD_SENSE_X11
P1_4	KBD_SENSE_X12
P1_5	KBD_CONTROL_L
P1_6	KBD_LEFT_OPTION_L
P1_7	KBD_RIGHT_SHIFT_L

3.3V RSLOC ISOLATION KEYS/ASIC RESET

=PP3V3_AON_KBD — CT150 1.0UF 20% 6.3V X5R 0201-1 138S0692 (PLACE_NEAR=UT103.10:5MM) — CT151 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 (PLACE_NEAR=UT103.10:2MM)

=PP1V8_S2_KBD → RT190 0 5% 1/20W MF 0201 → VDD

UT103 SLG4AP4815V TQFN 343S00073 (2.97 < VDD < 3.63)

IN_X: VIH_MIN 2.0V, VIL_MAX 0.8V, 100K IPD
OUT_X: VOH_MIN 2.4V, VOL_MAX 0.4V, 12.5K IPU OE

OUT123_EN → OE

KBD_RIGHT_SHIFT_KEY	IN_1	OUT_1 → KBD_RIGHT_SHIFT_L
KBD_LEFT_OPTION_KEY	IN_2	OUT_2 → KBD_LEFT_OPTION_L
KBD_CONTROL_KEY	IN_3	OUT_3 → KBD_CONTROL_L
		OUT_ALL# → RSLOC_RST_L

GND, EPAD

RT152 33 1% 1/20W MF 201 — RSLOC_RST_L → PMU_RSLOC_RST_L

CAPSLOCK LED DRIVER

CURRENT CONTROLLED LED DRIVING FROM J214/J223/J230
DIFFERENT FROM RESISTANCE CONTROL LED DRIVING FROM J152

NOSTUFF RT164 0 5% 1/20W MF 0201 — =PP3V3_AON_KBD_LEDDRIVER_R

RT163 0 5% 1/20W MF 0201 — =PP3V3_S2_KBD_LEDDRIVER_R

NOTE: THIS CAN BE THE SAME RAIL AS THE CAPSLOCK LED, OR IT CAN BE A RAIL THAT COMES UP AFTER

PP3V3_KBD_LEDDRIVER — CT105 1.0UF 20% 6.3V X5R 0201-1 138S0692

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

UT105 FAN5622 SSOT23

CAPSLOCK_LED_EN → RT161 1K 5% 1/20W MF 201 → LED_CTRL

LED_ISET — RT162 200K 5% 1/20W MF 201 — RT160 19.1K 1% 1/20W MF 201 <R_SET>

VIN_MIN 1.2V, VIL_MAX 0.4V

CTRL, ISET, LED1, LED2, GND

R_SET 19.1K 15 MA SINK

LED1 → KBD_LED1 → RT118 1.00 1% 1/20W MF-LF 0201 → KBD_CAP_CATHODE

3V3 KBD CONN SERIES R

KBD DRI REQUEST, TO MEASURE CAPSLOCK LED CURRENT

=PP3V3_AON_KBD — RT103 0 5% 1/20W MF 0201 — PP3V3_AON_KBD_CONN

TO KBD CONN AND ESD
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3V

ID_DETECT SERIES R

KBD_ID_DETECT1 — RT117 1K 5% 1/20W MF 201 — KBD_ID1

KBD_ID_1 PIN ON KBD CONNECTOR
ANSI: NO CONNECT
ISO: TIED HIGH TO PP1V8
JIS: TIED LOW TO GND

KBD_ID_DETECT2 — RT119 1K 5% 1/20W MF 201 — KBD_ID2

KBD_ID_2 PIN ON KBD CONNECTOR
TIED LOW TO GND FOR 34-PIN NEW KBD

=PP1V8_S2_KBD

RT130	10K	KBD_SENSE_X0
RT131	10K	KBD_SENSE_X1
RT132	10K	KBD_SENSE_X2
RT133	10K	KBD_SENSE_X3
RT134	10K	KBD_SENSE_X4
RT135	10K	KBD_SENSE_X5
RT136	10K	KBD_SENSE_X6
RT137	10K	KBD_SENSE_X7
RT138	10K	KBD_SENSE_X8
RT139	10K	KBD_SENSE_X9
RT140	10K	KBD_SENSE_X10
RT141	10K	KBD_SENSE_X11
RT142	10K	KBD_SENSE_X12
RT143	1K	IOXP2_ADDR

5% 1/20W MF 201

=PP1V83V3_S2_KBDIOXI2C

RT120	10K	IOXP2_RESET_L
RT122	10K	IOXP1_RESET_L
RT123	1.3K	I2C_KBD_SCL
RT124	1.3K	I2C_KBD_SDA
RT125	100K	IOXP1_INT_L

5% 1/20W MF 201

BOM_COST_GROUP=KEYBOARD

PAGE TITLE	KEYBOARD IOX, SUPPORT
	Apple Inc.
DRAWING NUMBER	051-05641
SIZE	D
REVISION	6.33.0
BRANCH	
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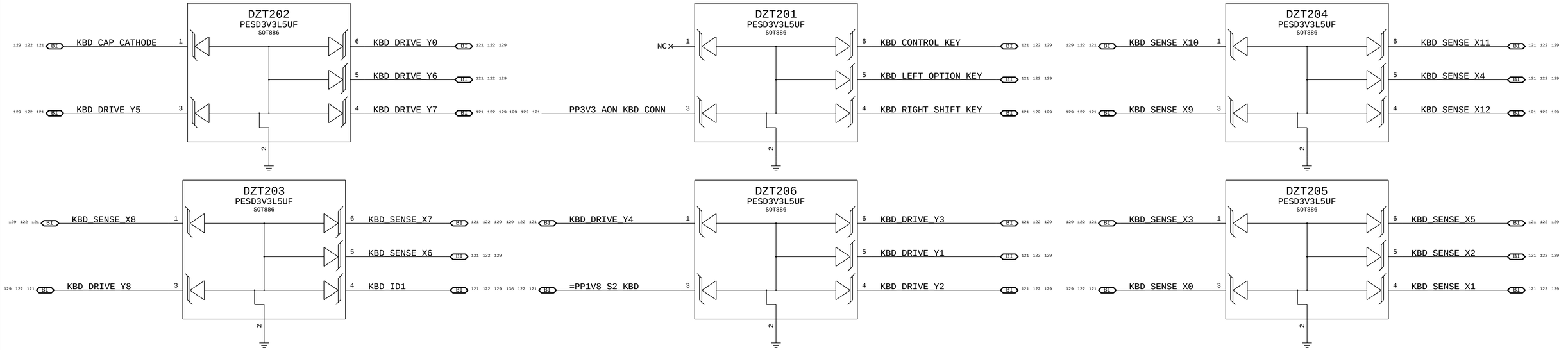
KEYBOARD ESD



MEMBRANE POR 34 PIN ZIF CONNECTOR

518S00231
CRITICAL
JT200
FF14A-34C-R11DL-B-3H
F-RT-SM

KBD_RIGHT_SHIFT_KEY	1	35	
=PP1V8_S2_KBD	2		
KBD_ID1	3		
	4		
KBD_ID2	5		
KBD_SENSE_X7	6		
KBD_SENSE_X11	7		
KBD_SENSE_X6	8		
KBD_SENSE_X9	9		
KBD_DRIVE_Y0	10		
KBD_DRIVE_Y10	11		
KBD_DRIVE_Y2	12		
KBD_DRIVE_Y8	13		
KBD_DRIVE_Y1	14		
KBD_SENSE_X8	15		
KBD_SENSE_X12	16		
KBD_SENSE_X10	17		
KBD_SENSE_X5	18		
KBD_SENSE_X4	19		
KBD_SENSE_X3	20		
KBD_SENSE_X1	21		
KBD_SENSE_X2	22		
KBD_SENSE_X0	23		
KBD_DRIVE_Y11	24		
KBD_DRIVE_Y9	25		
KBD_DRIVE_Y3	26		
KBD_DRIVE_Y4	27		
KBD_DRIVE_Y5	28		
KBD_DRIVE_Y7	29		
KBD_DRIVE_Y6	30		
KBD_CAP_CATHODE	31		
PP3V3_AON_KBD_CONN	32		
KBD_LEFT_OPTION_KEY	33		
KBD_CONTROL_KEY	34		
		36	

KEYBOARD BACKLIGHT CONNECTOR P0

CRITICAL
518S0818
PACK_IGNORE=TRUE
PACK_OPTION=P0
JT220
FF14A-6C-R11DL-B-3H
F-RT-SM

KBDLED_CATHODE1	1	7
	2	
NC	3	
=PPVOUT_KBDLED_CONN	4	
	5	
NC	6	
KBDLED_CATHODE2		8

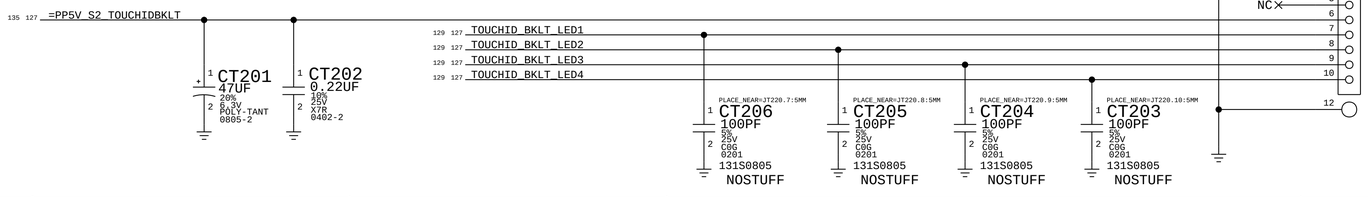
Placeholder for P0,J230 Backlight Flex

KEYBOARD BACKLIGHT CONNECTOR P1

CRITICAL
518S00116
PACK_OPTION=POR
JT220
FF14A-10C-R11DL-B-3H
F-RT-SM1

KBDLED_CATHODE2	1	11
KBDLED_CATHODE1	2	
NC	3	
=PPVOUT_KBDLED_CONN	4	
NC	5	
	6	
	7	
	8	
	9	
	10	
	12	

Add 4X caps Nostuff in case MESA LED ESD issue
Place 4x CAPS as close as possible to JT220



BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=RAYMOND SYNC_DATE=09/19/2020

PAGE TITLE
KEYBOARD SIGNAL CONNECTOR, ESD

Apple Inc.

DRAWING NUMBER 051-05641
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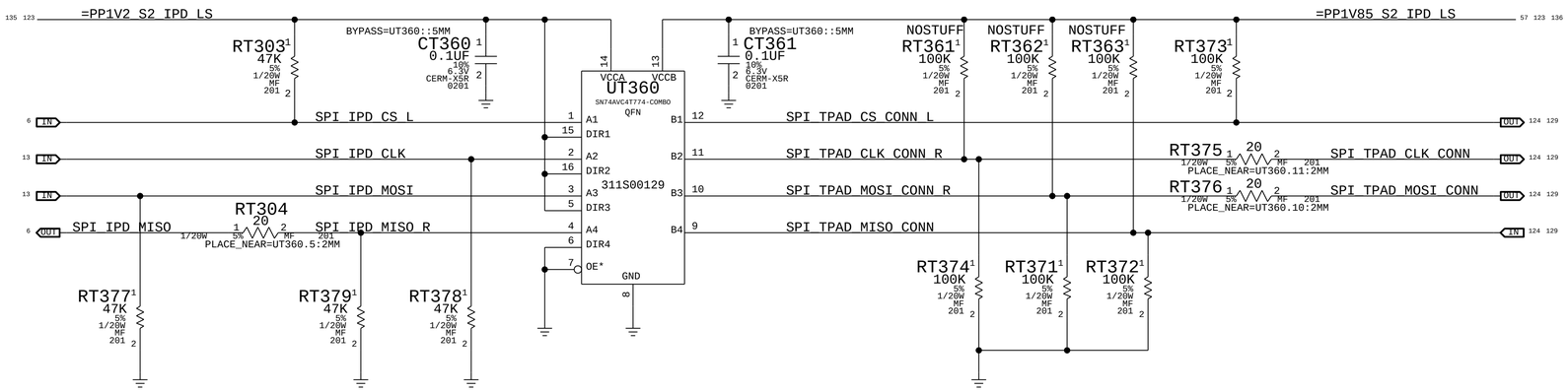
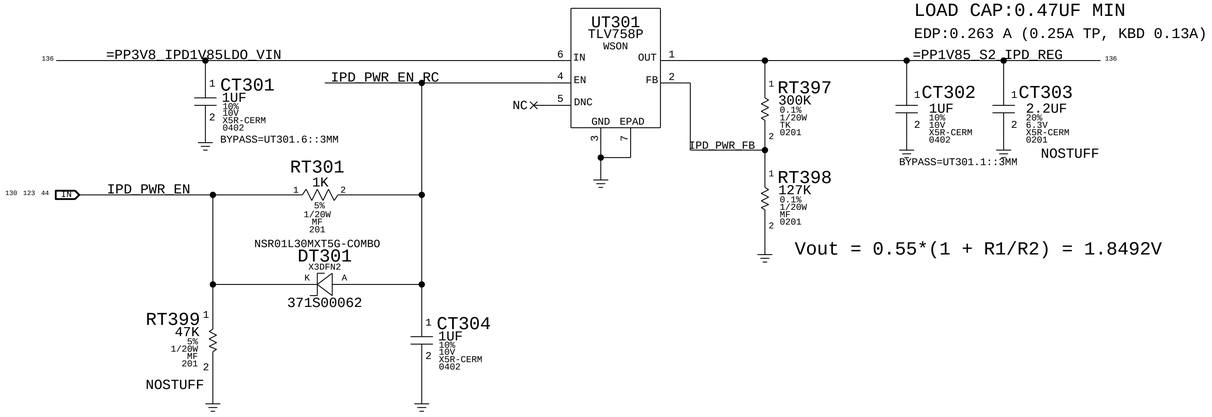
TRACKPAD SPI BUS LEVEL SHIFTER (+1.2V TO +1.8V)



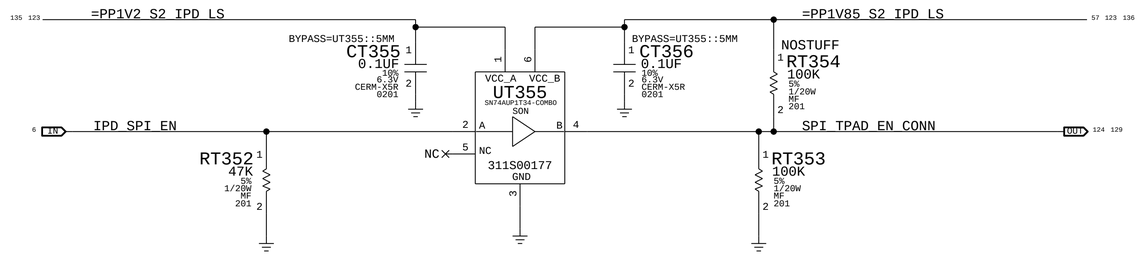
SN74AVC4T774 Truth Table

CTRL INPUTS		OUTPUT CIRCUITS		OPERATION
/OE	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

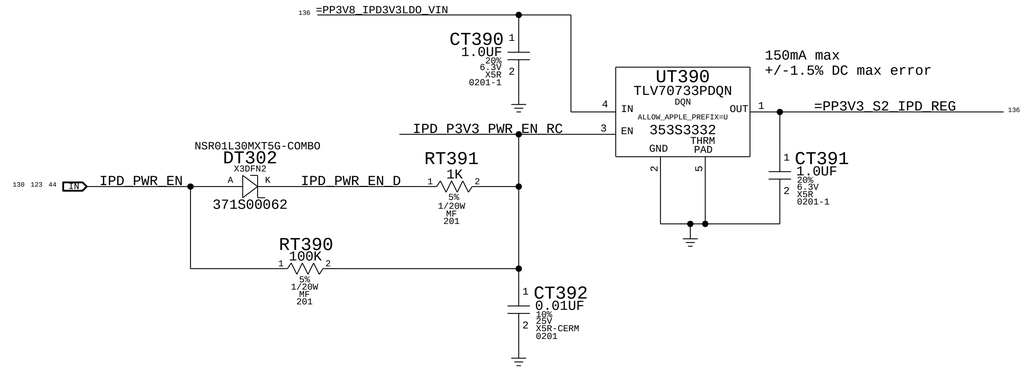
IPD LDO
1.85 V FOR TRACKPAD AND KEYBOARD IOX



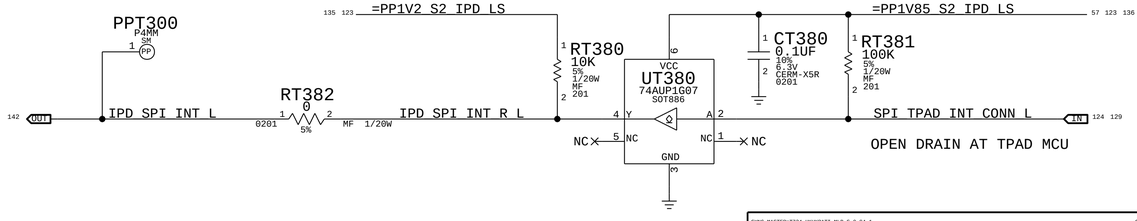
TRACKPAD SPI ENABLE LEVEL SHIFTER



3.3V S2 LDO FOR TPAD



IPD SPI INTERRUPT LEVEL SHIFTER



BOM_COST_GROUP=TRACKPAD

PAGE TITLE: TRACKPAD SUPPORT

Apple Inc.

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SIZE: D
REVISION: 6.33.0
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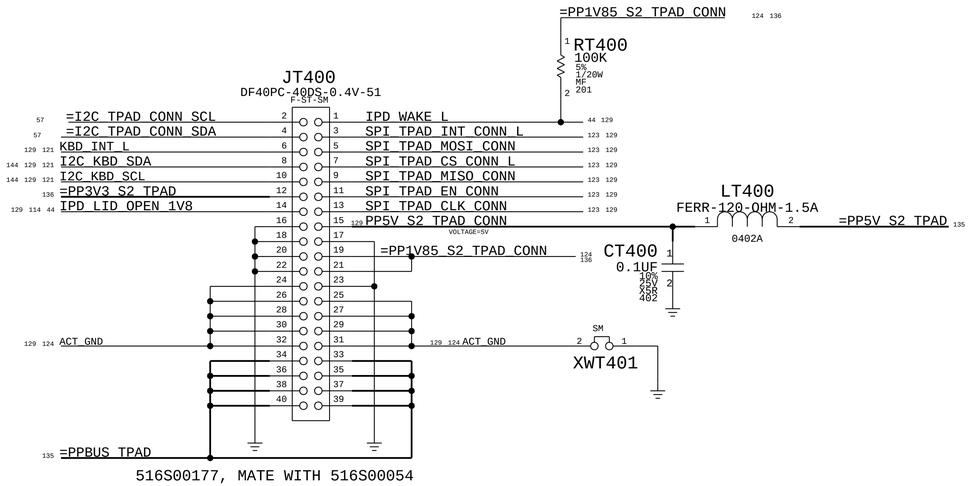
TPAD CONNECTOR



516S00177, MATE WITH 516S00054

BOM_COST_GROUP=TRACKPAD

SYNC_MASTER=MHARRAY1 SYNC_DATE=01/16/2020

PAGE TITLE

TRACKPAD CONNECTOR

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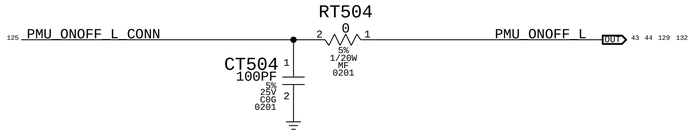

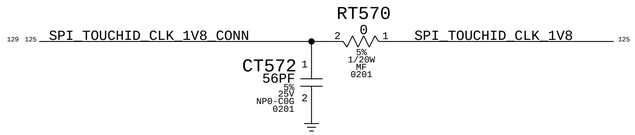

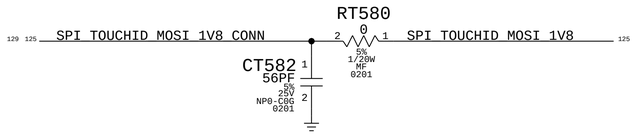

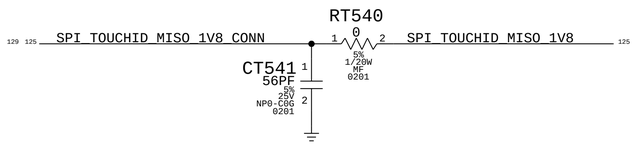

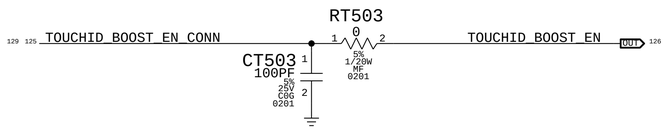

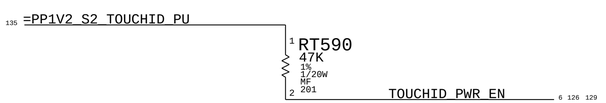

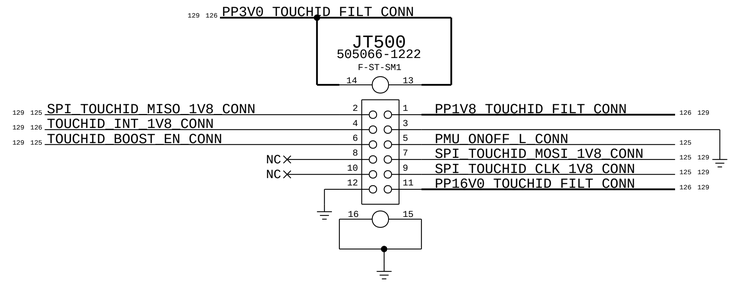

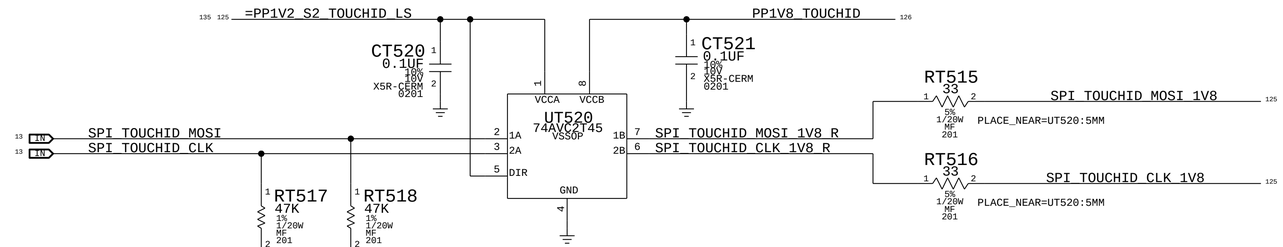

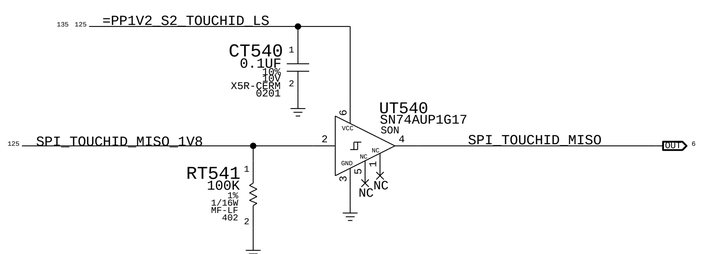

BOM_COST_GROUP=TOUCHID

SYNC_MASTER=JSHAO

PAGE TITLE

TOUCHID CONN

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SIZE D

REVISION 6.33.0

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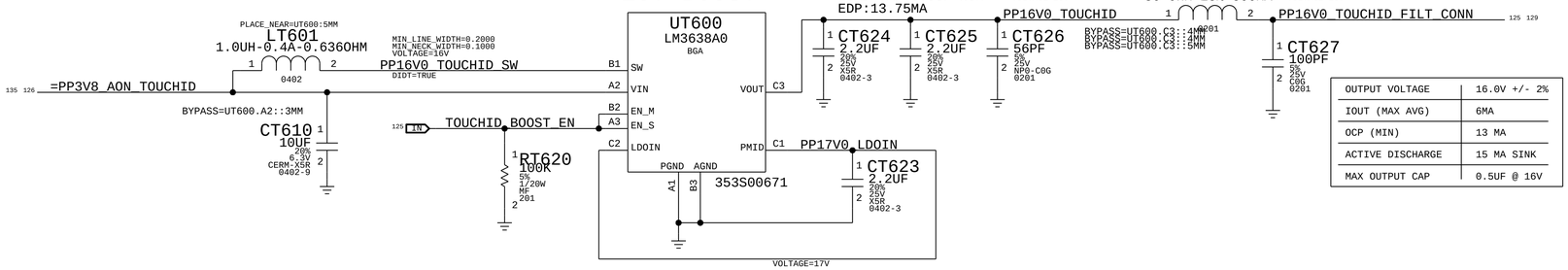
*** OK2INTEGRATE ***

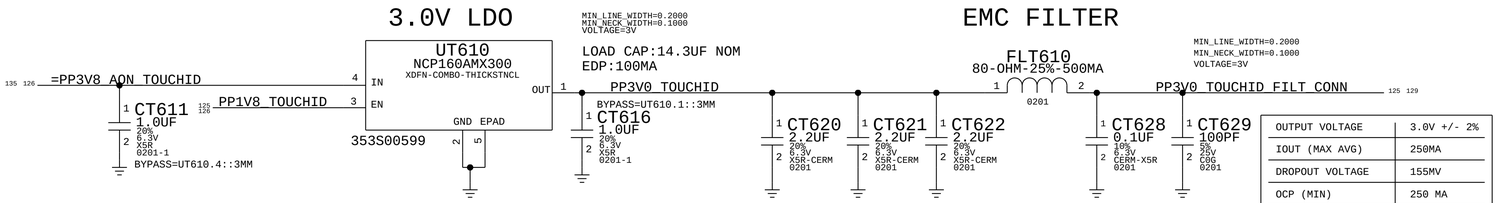
TOUCHID POWER SEQUENCING REQUIREMENTS
POWER ON: 1V8 -> 3V3 -> 16V0

16V BOOST



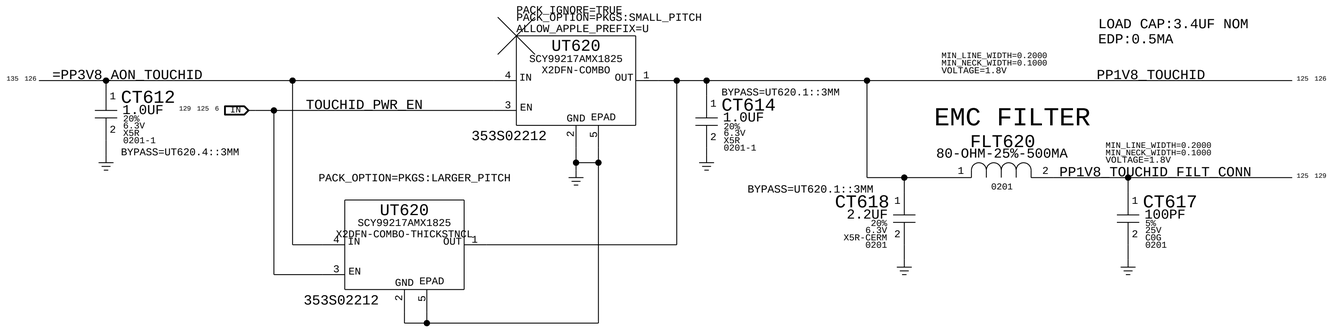
OUTPUT VOLTAGE	16.0V +/- 2%
IOUT (MAX AVG)	6MA
OCP (MIN)	13 MA
ACTIVE DISCHARGE	15 MA SINK
MAX OUTPUT CAP	0.5UF @ 16V

3.0V LDO



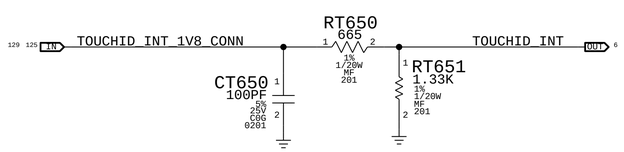
OUTPUT VOLTAGE	3.0V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	155MV
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP

1.8V LDO



OUTPUT VOLTAGE	1.825 V +/- 2%
IOUT (MAX AVG)	250 MA
DROPOUT VOLTAGE	75MV TYP @ 100MA
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MIN OUTPUT CAP	1.0 UF

UT620 CHANGED FROM 353S00754 TO 353S02212 FOR 1.2V EN SIGNAL SUPPORT.
N.B.: TOUCHID_PWR_EN REQUIRES 47K PULL-UP TO PP1V25_S2 AT THE SOC



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PAGE TITLE: TOUCHID SUPPORT

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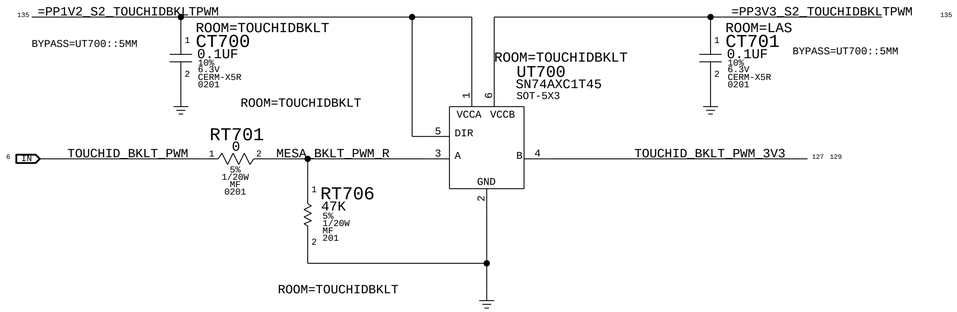
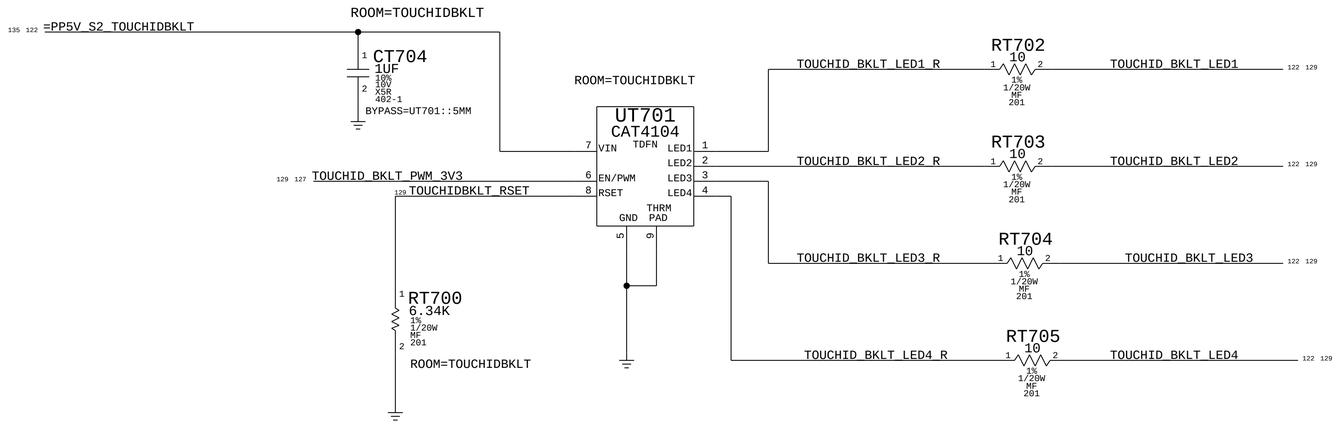
TOUCHID BKLT PWM LEVEL SHIFTER



TOUCHID BKLT LED DRIVER



CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	10UA	1.2MA
3 AON	10UA	8 MA
5V S2	80MA	80 MA

4X LEDS, 20MA EACH LED

BOM_COST_GROUP=TOUCHID

PAGE TITLE: TOUCHID_BACKLIGHT

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NAND0 TEST POINTS

101 100 99 98 97	IN	NAND0_LPB_L	TOP 1 TP	TPU603 TP-P4
105 104 103 102 100 99 98 97 8	IN	NAND_BFH	TOP 1 TP	TPU604 TP-P4
100 99 98 97	IN	NAND0_BOOT2	TOP 1 TP	TPU605 TP-P4
97	IN	NAND0_S5E0_SWD_UID0	TOP 1 TP	TPU606 TP-P4
98	IN	NAND0_S5E1_SWD_UID0	TOP 1 TP	TPU607 TP-P4
99	IN	NAND0_S5E2_SWD_UID0	TOP 1 TP	TPU608 TP-P4
100	IN	NAND0_S5E3_SWD_UID0	TOP 1 TP	TPU609 TP-P4
97	IN	NAND0_S5E0_SWD_UID1	TOP 1 TP	TPU610 TP-P4
98	IN	NAND0_S5E1_SWD_UID1	TOP 1 TP	TPU611 TP-P4
99	IN	NAND0_S5E2_SWD_UID1	TOP 1 TP	TPU612 TP-P4
100	IN	NAND0_S5E3_SWD_UID1	TOP 1 TP	TPU613 TP-P4
101 100 99 98 97	IN	NAND0_PFN_L	TOP 1 TP	TPU614 TP-P4
100 99 98 97 8	IN	NAND0_PCIE_RESET_L	TOP 1 TP	TPU615 TP-P4
11	IN	SWD_NAND0_SWDIO	TOP 1 TP	TPU616 TP-P4
11	IN	SWD_NAND0_SWCLK	TOP 1 TP	TPU617 TP-P4
100 99 98 97	IN	NAND0_WP_L	TOP 1 TP	TPU618 TP-P4
107 8	IN	NAND0_CLKREQ0_L	TOP 1 TP	TPU619 TP-P4
107 8	IN	NAND0_CLKREQ1_L	TOP 1 TP	TPU620 TP-P4
107 8	IN	NAND0_CLKREQ2_L	TOP 1 TP	TPU621 TP-P4
107 8	IN	NAND0_CLKREQ3_L	TOP 1 TP	TPU622 TP-P4
97	IN	NAND0_S5E0_PCIE_RESREF	TOP 1 TP	TPU623 TP-P4
98	IN	NAND0_S5E1_PCIE_RESREF	TOP 1 TP	TPU624 TP-P4
99	IN	NAND0_S5E2_PCIE_RESREF	TOP 1 TP	TPU625 TP-P4
100	IN	NAND0_S5E3_PCIE_RESREF	TOP 1 TP	TPU626 TP-P4
101 100 99 98 97	IN	NAND0_RESET_L	TOP 1 TP	TPU627 TP-P4
97	IN	NAND0_S5E0_ZQ_0	TOP 1 TP	TPU628 TP-P4
97	IN	NAND0_S5E0_ZQ_1	TOP 1 TP	TPU629 TP-P4
98	IN	NAND0_S5E1_ZQ_1	TOP 1 TP	TPU630 TP-P4
98	IN	NAND0_S5E1_ZQ_0	TOP 1 TP	TPU631 TP-P4
99	IN	NAND0_S5E2_ZQ_0	TOP 1 TP	TPU632 TP-P4
99	IN	NAND0_S5E2_ZQ_1	TOP 1 TP	TPU633 TP-P4
100	IN	NAND0_S5E3_ZQ_1	TOP 1 TP	TPU634 TP-P4
100	IN	NAND0_S5E3_ZQ_0	TOP 1 TP	TPU635 TP-P4
97	IN	TP_NAND0_S5E0_JTAG_TDI	TOP 1 TP	TPU668 TP-P4
100	IN	TP_NAND0_S5E3_JTAG_TDO	TOP 1 TP	TPU669 TP-P4
100 99 98 97	IN	NAND0_JTAG_SEL	TOP 1 TP	TPU670 TP-P4
100 99 98 97	IN	NAND0_JTAG_TRST_L	TOP 1 TP	TPU671 TP-P4
129 97	IN	TP_NAND0_S5E0_ANI1_VREF	TOP 1 TP	TPU672 TP-P4
129 97	IN	TP_NAND0_S5E0_ANI0_VREF	TOP 1 TP	TPU673 TP-P4
129 98	IN	TP_NAND0_S5E1_ANI1_VREF	TOP 1 TP	TPU674 TP-P4
129 98	IN	TP_NAND0_S5E1_ANI0_VREF	TOP 1 TP	TPU675 TP-P4
99	IN	TP_NAND0_S5E2_ANI1_VREF	TOP 1 TP	TPU676 TP-P4
99	IN	TP_NAND0_S5E2_ANI0_VREF	TOP 1 TP	TPU677 TP-P4
100	IN	TP_NAND0_S5E3_ANI1_VREF	TOP 1 TP	TPU678 TP-P4
100	IN	TP_NAND0_S5E3_ANI0_VREF	TOP 1 TP	TPU679 TP-P4
101	IN	TP_NAND0_OCARINA_VEN2	TOP 1 TP	TPU600 TP-P4

NAND1 TEST POINTS

106 105 104 103 102	IN	NAND1_LPB_L	TOP 1 TP	TPU636 TP-P4
105 104 103 102	IN	NAND1_BOOT2	TOP 1 TP	TPU637 TP-P4
102	IN	NAND1_S5E0_SWD_UID0	TOP 1 TP	TPU638 TP-P4
103	IN	NAND1_S5E1_SWD_UID0	TOP 1 TP	TPU639 TP-P4
104	IN	NAND1_S5E2_SWD_UID0	TOP 1 TP	TPU640 TP-P4
105	IN	NAND1_S5E3_SWD_UID0	TOP 1 TP	TPU641 TP-P4
102	IN	NAND1_S5E0_SWD_UID1	TOP 1 TP	TPU642 TP-P4
103	IN	NAND1_S5E1_SWD_UID1	TOP 1 TP	TPU643 TP-P4
104	IN	NAND1_S5E2_SWD_UID1	TOP 1 TP	TPU644 TP-P4
105	IN	NAND1_S5E3_SWD_UID1	TOP 1 TP	TPU645 TP-P4
106 105 104 103 102	IN	NAND1_PFN_L	TOP 1 TP	TPU646 TP-P4
105 104 103 102 8	IN	NAND1_PCIE_RESET_L	TOP 1 TP	TPU647 TP-P4
11	IN	SWD_NAND1_SWDIO	TOP 1 TP	TPU648 TP-P4
11	IN	SWD_NAND1_SWCLK	TOP 1 TP	TPU649 TP-P4
105 104 103 102	IN	NAND1_WP_L	TOP 1 TP	TPU650 TP-P4
107 8	IN	NAND1_CLKREQ0_L	TOP 1 TP	TPU651 TP-P4
107 8	IN	NAND1_CLKREQ1_L	TOP 1 TP	TPU652 TP-P4
107 8	IN	NAND1_CLKREQ2_L	TOP 1 TP	TPU653 TP-P4
107 8	IN	NAND1_CLKREQ3_L	TOP 1 TP	TPU654 TP-P4
102	IN	NAND1_S5E0_PCIE_RESREF	TOP 1 TP	TPU655 TP-P4
103	IN	NAND1_S5E1_PCIE_RESREF	TOP 1 TP	TPU656 TP-P4
104	IN	NAND1_S5E2_PCIE_RESREF	TOP 1 TP	TPU657 TP-P4
105	IN	NAND1_S5E3_PCIE_RESREF	TOP 1 TP	TPU658 TP-P4
106 105 104 103 102	IN	NAND1_RESET_L	TOP 1 TP	TPU659 TP-P4
102	IN	NAND1_S5E0_ZQ_0	TOP 1 TP	TPU660 TP-P4
102	IN	NAND1_S5E0_ZQ_1	TOP 1 TP	TPU661 TP-P4
103	IN	NAND1_S5E1_ZQ_1	TOP 1 TP	TPU662 TP-P4
103	IN	NAND1_S5E1_ZQ_0	TOP 1 TP	TPU663 TP-P4
104	IN	NAND1_S5E2_ZQ_0	TOP 1 TP	TPU664 TP-P4
104	IN	NAND1_S5E2_ZQ_1	TOP 1 TP	TPU665 TP-P4
105	IN	NAND1_S5E3_ZQ_1	TOP 1 TP	TPU666 TP-P4
105	IN	NAND1_S5E3_ZQ_0	TOP 1 TP	TPU667 TP-P4
104 103	IN	NAND1_S5E1_JTAG_TDO	TOP 1 TP	TPU680 TP-P4
105 104	IN	NAND1_S5E2_JTAG_TDO	TOP 1 TP	TPU681 TP-P4
102	IN	TP_NAND1_S5E0_JTAG_TDI	TOP 1 TP	TPU682 TP-P4
105	IN	TP_NAND1_S5E3_JTAG_TDO	TOP 1 TP	TPU683 TP-P4
105 104 103 102	IN	NAND1_JTAG_SEL	TOP 1 TP	TPU684 TP-P4
105 104 103 102	IN	NAND1_JTAG_TRST_L	TOP 1 TP	TPU685 TP-P4
129 102	IN	TP_NAND1_S5E0_ANI1_VREF	TOP 1 TP	TPU686 TP-P4
129 102	IN	TP_NAND1_S5E0_ANI0_VREF	TOP 1 TP	TPU687 TP-P4
129 103	IN	TP_NAND1_S5E1_ANI1_VREF	TOP 1 TP	TPU688 TP-P4
129 103	IN	TP_NAND1_S5E1_ANI0_VREF	TOP 1 TP	TPU689 TP-P4
104	IN	TP_NAND1_S5E2_ANI1_VREF	TOP 1 TP	TPU690 TP-P4
104	IN	TP_NAND1_S5E2_ANI0_VREF	TOP 1 TP	TPU691 TP-P4
105	IN	TP_NAND1_S5E3_ANI1_VREF	TOP 1 TP	TPU692 TP-P4
105	IN	TP_NAND1_S5E3_ANI0_VREF	TOP 1 TP	TPU693 TP-P4
106	IN	TP_NAND1_OCARINA_VEN2	TOP 1 TP	TPU601 TP-P4

SOC MISC DEBUG TEST-POINTS

44 10	PMU_CLK32K_SOC	1 A TP-P5	TPU6600	PLACE_SIDE=BOTTOM
TPT_SOC_DOCK_ATTENTION MAKE_BASE=TRUE	10 TP_SOC_DOCK_ATTENTION	1 A TP-P5	TPU6601	PLACE_SIDE=TOP
129 10	SMC_FIXTURE_MODE_L	1 A TP-P5	TPU6603	PLACE_SIDE=TOP

SOC JTAG TEST-POINTS

10	SOC_JTAG_SEL	1 A TP-P5	TPU6604	
129 70 11	SWD_SOC_SWCLK	1 A TP-P5	TPU6605	
TPT_JTAG_SOC_TDI MAKE_BASE=TRUE	144 10 TP_JTAG_SOC_TDI	1 A TP-P5	TPU6606	
TPT_JTAG_SOC_TDO MAKE_BASE=TRUE	144 10 TP_JTAG_SOC_TDO	1 A TP-P5	TPU6607	
129 70 11	SWD_SOC_SWDIO	1 A TP-P5	TPU6608	
TPT_JTAG_SOC_TRST_L MAKE_BASE=TRUE	10 TP_JTAG_SOC_TRST_L	1 A TP-P5	TPU6609	

SOC DEBUG TEST-POINTS

TPT_TST_CLKOUT MAKE_BASE=TRUE	TP_TST_CLKOUT	TRUE 5	PPU1 1 PP P3MM	PLACE_SIDE=BOTTOM
5	TP_ANALOGMUX_OUT0	1 A TP-P5	TPU6612	PLACE_SIDE=TOP
5	TP_ANALOGMUX_OUT1	1 A TP-P5	TPU6613	PLACE_SIDE=TOP
129 70 6	UART_DEBUGPRT_D2R	1 A TP-P5	TPU6614	PLACE_SIDE=BOTTOM
129 70 6	UART_DEBUGPRT_R2D	1 A TP-P5	TPU6615	PLACE_SIDE=BOTTOM
129 43 10 5	PMU_RESET_L	1 A TP-P5	TPU6616	PLACE_SIDE=BOTTOM
132 129 70 43 5	SOC_FORCE_DFU	1 A TP-P5	TPU6617	PLACE_SIDE=BOTTOM
5	SOC_REQUEST_DFU1_L	1 A TP-P5	TPU6618	PLACE_SIDE=BOTTOM
5	SOC_REQUEST_DFU2_L	1 A TP-P5	TPU6619	PLACE_SIDE=BOTTOM
131 129 70 5	SOC_DFU_STATUS	1 A TP-P5	TPU6620	PLACE_SIDE=BOTTOM
131 129 78 69 43 5	PMU_ACTIVE_READY	1 A TP-P5	TPU6621	PLACE_SIDE=BOTTOM
129 5	SOC_HOLD_RESET	1 A TP-P5	TPU6622	PLACE_SIDE=BOTTOM
5	SOC_KIS_DFU_SELECT	1 A TP-P5	TPU6623	PLACE_SIDE=BOTTOM
5	SOC_DBG_PROBE_VALID	1 A TP-P5	TPU6624	PLACE_SIDE=BOTTOM
5	SOC_STOP_CLK_L	1 A TP-P5	TPU6625	PLACE_SIDE=BOTTOM

TEST POINTS REQUESTED BY BY AUDIO TEAM

115	PP3V8_CODEC_VP	1 TP	TPU6626
115	PP1V8_CODEC_VCP	1 TP-P5	TPU6627
115 10	CODEC_RESET_L	1 TP-P5	TPU6628
115 6	CODEC_INT_L	1 TP-P5	TPU6629
115 13	TDM_CODEC_FSYNC PLACE_NEAR=UR500.B2:20MM	1 TP-P5	TPU6630
115 13	TDM_CODEC_R2D PLACE_NEAR=UR500.B3:20MM	1 TP-P5	TPU6631
115 6	TDM_CODEC_D2R PLACE_NEAR=U0600.AC73:20MM	1 TP-P5	TPU6632
115 13	TDM_CODEC_BCLK PLACE_NEAR=UR500.A3:20MM	1 TP-P5	TPU6633
115 55	=I2C_CODEC_SDA	1 TP-P5	TPU6634
115 55	=I2C_CODEC_SCL	1 TP-P5	TPU6635
117 116 6	SPKRAMP_RESET_L	1 TP-P5	TPU6636
117 116 6	SPKRAMP_INT_L	1 TP-P5	TPU6637
116 13	=TDM_SPKRAMP_A_BCLK PLACE_NEAR=UR600.E1:20MM	1 TP-P5	TPU6638
116 13	=TDM_SPKRAMP_A_FSYNC PLACE_NEAR=UR600.D2:20MM	1 TP-P5	TPU6639
116 13	=TDM_SPKRAMP_A_R2D PLACE_NEAR=UR600.E2:20MM	1 TP-P5	TPU6640
116 13	=TDM_SPKRAMP_A_D2R PLACE_NEAR=U0600.AC77:20MM	1 TP-P5	TPU6641
116	SPKRAMP_ABC_ICC	1 TP-P5	TPU6642
117 116	SPKRAMP_DEF_ICC	1 TP-P5	TPU6672
116 55	=I2C_SPKRAMP_A_SCL	1 TP-P5	TPU6643
116 55	=I2C_SPKRAMP_A_SDA	1 TP-P5	TPU6644
116	TP_SPKRAMP_A_LV_EN	1 TP-P5	TPU6645
116	TP_SPKRAMP_B_LV_EN	1 TP-P5	TPU6646
116	TP_SPKRAMP_C_LV_EN	1 TP-P5	TPU6647
117 13	=TDM_SPKRAMP_D_BCLK PLACE_NEAR=UR700.E1:20MM	1 TP-P5	TPU6648
117 13	=TDM_SPKRAMP_D_FSYNC PLACE_NEAR=UR700.D2:20MM	1 TP-P5	TPU6649
117 13	=TDM_SPKRAMP_D_R2D PLACE_NEAR=UR700.E2:20MM	1 TP-P5	TPU6650
117 13	=TDM_SPKRAMP_D_D2R PLACE_NEAR=U0600.AA72:20MM	1 TP-P5	TPU6651
117 55	=I2C_SPKRAMP_D_SCL	1 TP-P5	TPU6652
117 55	=I2C_SPKRAMP_D_SDA	1 TP-P5	TPU6653
117	TP_SPKRAMP_D_LV_EN	1 TP-P5	TPU6654
117	TP_SPKRAMP_E_LV_EN	1 TP-P5	TPU6655
117	TP_SPKRAMP_F_LV_EN	1 TP-P5	TPU6656
114 10	PDM_DMIC_DATA3 PLACE_NEAR=U0600.AD13:20MM	TOP 1 TP TP-P4	TPU6657
114 10	PDM_DMIC_DATA4 PLACE_NEAR=U0600.AB13:20MM	TOP 1 TP TP-P4	TPU6658
114 10	PDM_DMIC_CLK3 PLACE_NEAR=UR300.3:20MM	TOP 1 TP TP-P4	TPU6659
114 10	PDM_DMIC_CLK4 PLACE_NEAR=UR302.3:20MM	TOP 1 TP TP-P4	TPU6660
119 114	DMIC_DATA0_1V8_IN PLACE_NEAR=UR320.2:20MM	TOP 1 TP TP-P4	TPU6661
119 114	DMIC_DATA1_1V8_IN PLACE_NEAR=UR310.2:20MM	TOP 1 TP TP-P4	TPU6662
I115	TP_P0V81SRAM_SENSE	TRUE 16		
I115	TP_PVDDAFRAWAKESW_SENSE	TRUE 19		
I115	TP_PVDDAMPH0S2SW_SENSE	TRUE 19		
I115	TP_PVDDANE0AWAKESW_SENSE	TRUE 19		
I115	TP_PVDDDCS_SENSE	TRUE 16		
I115	TP_PVDDFABRICS1_SENSE	TRUE 20		
130 31 30	USBC5_CC1	TOP 1 TP TP-P4	TPU6663	
43 29	CHGR_AUX_OK	TOP 1 TP TP-P4	TPU6664	
137	PP1V8_S1_CLVR_VDDH	TOP 1 TP TP-P4	TPU6665	
121	KBD_RIGHT_SHIFT_L PLACE_NEAR=UI103.9:20MM	TOP 1 TP TP-P4	TPU6666	
121	KBD_LEFT_OPTION_L PLACE_NEAR=UI103.8:20MM	TOP 1 TP TP-P4	TPU6667	
121	KBD_CONTROL_L PLACE_NEAR=UI103.7:20MM	TOP 1 TP TP-P4	TPU6668	
130 128 43 39	PMU_CRASH_SLAVE_L	TOP 1 TP TP-P4	TPU6669	
128 43 39	PMU_WAKE2MS	TOP 1 TP TP-P4	TPU6670	
I110	KBD_ID2	TRUE 121 122		
I110	KBD_DRIVE_Y9	TRUE 121 122		
I110	KBD_DRIVE_Y10	TRUE 121 122		
I110	KBD_DRIVE_Y11	TRUE 121 122		
I110	PPVDD_GPU0_AWAKESW	TRUE 137		
I110	PMU_CRASH_SLAVE_L	TRUE 39 43 128 130		
I117	PMU_WAKE2MS	TRUE 39 43 128		
I110	ATCRTMR01_ACTIVE_READY_3V3	TRUE 67 68 69		

FAN TEST POINTS

66	TP_I2C_FAN0_SCL	BOTTOM 1 TP	TPU6200	TP-P4
66	TP_I2C_FAN0_SDA	BOTTOM 1 TP	TPU6201	TP-P4
66	TP_I2C_FAN1_SCL	BOTTOM 1 TP	TPU6202	TP-P4
66	TP_I2C_FAN1_SDA	BOTTOM 1 TP	TPU203	TP-P4

BSB THERMAL TESTPOINTS

67	ATCRTMR0_THERM_D_P	1 TP	TP-P4	TPU6300
67	ATCRTMR0_THERM_D_N	1 TP	TP-P4	TPU6301
68	ATCRTMR1_THERM_D_P	1 TP	TP-P4	TPU6302
68	ATCRTMR1_THERM_D_N	1 TP	TP-P4	TPU6303
77	ATCRTMR2_THERM_D_P	1 TP	TP-P4	TPU6304
77	ATCRTMR2_THERM_D_N	1 TP	TP-P4	TPU6305

33	I2C_P3V8AON_SCL	1 TP	TP-P5	TPV001
33	I2C_P3V8AON_SDA	1 TP	TP-P5	TPV002

134 10	SOC_DOCK_CONNECT	TOP 1 TP TP-P4	TPU6671
I114	CODEC_WAKE_L	TRUE 43 115	

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SPMU PPs

PPU800
P3MM_SM (PP 1) SPMU_BUCK5_LX0 38
PPU801
P3MM_SM (PP 1) SPMU_BUCK5_LX1 38
PPU802
P3MM_SM (PP 1) SPMU_BUCK5_LX2 38
PPU803
P3MM_SM (PP 1) SPMU_BUCK5_LX3 38
PPU804
P3MM_SM (PP 1) SPMU_BUCK5_FB_R 38
PPU805
P3MM_SM (PP 1) SPMU_BUCK5_FB 38
PPU806
P3MM_SM (PP 1) SPMU_BUCK6_LX0 38
PPU807
P3MM_SM (PP 1) SPMU_BUCK6_FB_R 38
PPU808
P3MM_SM (PP 1) SPMU_BUCK6_FB 38
PPU809
P3MM_SM (PP 1) SPMU_BUCK7_LX0 38
PPU810
P3MM_SM (PP 1) SPMU_BUCK7_LX1 38
PPU811
P3MM_SM (PP 1) SPMU_BUCK7_LX2 38
PPU812
P3MM_SM (PP 1) SPMU_BUCK8_LX0 38
PPU813
P3MM_SM (PP 1) SPMU_BUCK8_FB_R 38
PPU814
P3MM_SM (PP 1) SPMU_BUCK8_FB 38
PPU815
P3MM_SM (PP 1) SPMU_BUCK9_LX0 38
PPU816
P3MM_SM (PP 1) SPMU_BUCK9_FB_R 38
PPU817
P3MM_SM (PP 1) SPMU_BUCK9_FB 38
PPU818
P3MM_SM (PP 1) SPMU_BUCK10_LX0 38
PPU819
P3MM_SM (PP 1) SPMU_BUCK10_LX1 38
PPU820
P3MM_SM (PP 1) SPMU_BUCK10_LX2 38
PPU821
P3MM_SM (PP 1) SPMU_BUCK10_FB_R 38
PPU822
P3MM_SM (PP 1) SPMU_BUCK10_FB 38
PPU823
P3MM_SM (PP 1) SPMU_BUCK0_LX0 38
PPU824
P3MM_SM (PP 1) SPMU_BUCK0_LX1 38
PPU825
P3MM_SM (PP 1) SPMU_BUCK0_LX2 38
PPU826
P3MM_SM (PP 1) SPMU_BUCK0_LX3 38
PPU827
P3MM_SM (PP 1) SPMU_BUCK0_FB 38
PPU828
P3MM_SM (PP 1) SPMU_BUCK0_FB_R 38
PPU829
P3MM_SM (PP 1) SPMU_BUCK1_LX0 38
PPU830
P3MM_SM (PP 1) SPMU_BUCK1_LX1 38
PPU8031
P3MM_SM (PP 1) SPMU_BUCK1_FB 38
PPU832
P3MM_SM (PP 1) SPMU_BUCK1_FB_R 38
PPU833
P3MM_SM (PP 1) SPMU_BUCK2_LX0 38
PPU834
P3MM_SM (PP 1) SPMU_BUCK2_FB 38
PPU835
P3MM_SM (PP 1) SPMU_BUCK2_FB_R 38
PPU836
P3MM_SM (PP 1) SPMU_BUCK3_LX0 38
PPU837
P3MM_SM (PP 1) SPMU_BUCK3_FB 38
PPU838
P3MM_SM (PP 1) SPMU_BUCK3_FB_R 38
PPU839
P3MM_SM (PP 1) SPMU_BUCK4_LX0 38

PPU840
P3MM_SM (PP 1) SPMU_BUCK4_LX1 38
PP1
P3MM_SM (PP 1) SPMU_BUCK4_LX2 38
PPU842
P3MM_SM (PP 1) SPMU_BUCK4_LX3 38
PP2
P3MM_SM (PP 1) SPMU_BUCK4_FB 38
PPU844
P3MM_SM (PP 1) SPMU_BUCK4_FB_R 38

MPMU PPs

PP3
P3MM_SM (PP 1) MPMU_BUCK5_LX0 42
PPU846
P3MM_SM (PP 1) MPMU_BUCK5_LX1 42
PP4
P3MM_SM (PP 1) MPMU_BUCK5_LX2 42
PPU848
P3MM_SM (PP 1) MPMU_BUCK5_LX3 42
PPU849
P3MM_SM (PP 1) MPMU_BUCK5_FB_R 42
PPU850
P3MM_SM (PP 1) MPMU_BUCK5_FB 42
PP5
P3MM_SM (PP 1) MPMU_BUCK6_LX0 42
PPU852
P3MM_SM (PP 1) MPMU_BUCK6_FB_R 42
PP6
P3MM_SM (PP 1) MPMU_BUCK6_FB 42
PPU854
P3MM_SM (PP 1) MPMU_BUCK7_LX0 42
PPU855
P3MM_SM (PP 1) MPMU_BUCK7_LX1 42
PPU856
P3MM_SM (PP 1) MPMU_BUCK7_LX2 42
PPU857
P3MM_SM (PP 1) MPMU_BUCK8_LX0 42
PPU858
P3MM_SM (PP 1) MPMU_BUCK8_FB_R 42
PPU859
P3MM_SM (PP 1) MPMU_BUCK8_FB 42
PPU860
P3MM_SM (PP 1) MPMU_BUCK9_LX0 42
PPU861
P3MM_SM (PP 1) MPMU_BUCK9_FB_R 42
PPU862
P3MM_SM (PP 1) MPMU_BUCK9_FB 42
PPU863
P3MM_SM (PP 1) MPMU_BUCK10_LX0 42
PPU864
P3MM_SM (PP 1) MPMU_BUCK10_LX1 42

PPU866
P3MM_SM (PP 1) MPMU_BUCK10_FB_R 42
PPU867
P3MM_SM (PP 1) MPMU_BUCK10_FB 42
PPU868
P3MM_SM (PP 1) MPMU_BUCK0_LX0 42
PPU869
P3MM_SM (PP 1) MPMU_BUCK0_LX1 42

PPU870
P3MM_SM (PP 1) MPMU_BUCK0_LX2 42
PPU871
P3MM_SM (PP 1) MPMU_BUCK0_LX3 42
PPU872
P3MM_SM (PP 1) MPMU_BUCK0_FB 42
PPU873
P3MM_SM (PP 1) MPMU_BUCK0_FB_R 42
PPU874
P3MM_SM (PP 1) MPMU_BUCK1_LX0 42
PPU875
P3MM_SM (PP 1) MPMU_BUCK1_LX1 42
PPU876
P3MM_SM (PP 1) MPMU_BUCK1_FB 42
PPU877
P3MM_SM (PP 1) MPMU_BUCK1_FB_R 42
PPU878
P3MM_SM (PP 1) MPMU_BUCK2_LX0 42
PPU879
P3MM_SM (PP 1) MPMU_BUCK2_FB 42
PPU880
P3MM_SM (PP 1) MPMU_BUCK2_FB_R 42
PPU881
P3MM_SM (PP 1) MPMU_BUCK3_LX0 42
PPU882
P3MM_SM (PP 1) MPMU_BUCK3_FB 42
PP8
P3MM_SM (PP 1) MPMU_BUCK3_FB_R 42
PPU884
P3MM_SM (PP 1) MPMU_BUCK4_LX0 42
PPU885
P3MM_SM (PP 1) MPMU_BUCK4_LX1 42
PPU886
P3MM_SM (PP 1) MPMU_BUCK4_LX2 42
PPU887
P3MM_SM (PP 1) MPMU_BUCK4_LX3 42
PPU888
P3MM_SM (PP 1) MPMU_BUCK4_FB 42
PPU889
P3MM_SM (PP 1) MPMU_BUCK4_FB_R 42

UPC_PMU_RESET_1V2 TRUE 43 44
134 132 80 72 71 44 UPC_PMU_RESET_3V3 TPU6800 1 A TP-P5
PLACE_SIDE=BOTTOM
EDP_BKLT_1V29_EN TRUE 44 110
IPD_PWR_EN TRUE 44 123
IPD_PWR_EN_PMU TRUE 44

PPU8A0
P3MM_SM (PP 1) MPMU_VPP_OTP 43
PPU8A3
P3MM_SM (PP 1) SPMU_BUCK7_FB 38
PPU8A5
P3MM_SM (PP 1) SPMU_VPP_OTP 39
PPU8A8
P3MM_SM (PP 1) CLVR_VDDH_UVWARN_L 5 50 129
PPU8A9
P3MM_SM (PP 1) P1V8VDDH_ILIMIT_THROTTLE_L 5 47
PPU8B0
P3MM_SM (PP 1) P1V8VDDH_PWR_EN 43 44 47
PPU8B1
P3MM_SM (PP 1) P1V8VDDH_SLP_L 43 47 131
PPU8B2
P3MM_SM (PP 1) P3V8AON_LPM 33 43 44
PPU8B7
P3MM_SM (PP 1) PMU_UVWARN_L 5 11

MAGSAFE PPs
29 PP3V3_HVLDO_OUT BOTTOM 1 PPU2
129 31 29 PP3V3_SW_ACE5 BOTTOM 1 PPU3
130 29 HVSW_G2 BOTTOM 1 PPU4
128 31 30 USBC5_CC1 BOTTOM 1 PPU5
129 56 32 10 I2C_SMC_UPC_SCL BOTTOM 1 PPU6
129 56 32 10 I2C_SMC_UPC_SDA BOTTOM 1 PPU7
29 VBUS_USBC5_UV BOTTOM 1 PPU7A
29 INT5_DIS BOTTOM 1 PPU7B
29 INT5_DIS_C BOTTOM 1 PPU7C
130 29 PPVBUS_MID BOTTOM 1 PPU7D

USB-C ATC1 Aardvarkanoid PPs
69 11 SWD_UPC_SWDIO3 BOTTOM 1 PPU8
69 32 11 SWD_UPC_SWCLK1 BOTTOM 1 PPU9
70 SPI_UPC1_MISO BOTTOM 1 PPU10
70 SPI_UPC1_MOSI BOTTOM 1 PPU11
70 SPI_UPC1_CLK BOTTOM 1 PPU12
70 69 SPI_UPC1_CS_L BOTTOM 1 PPU13
69 32 I2C_UPC01_3V3_SDA BOTTOM 1 PPU14
69 32 I2C_UPC01_3V3_SCL BOTTOM 1 PPU15
135 72 71 69 =PP1V25_S2_ACE01 BOTTOM 1 PPU16

USBC Debug 3mm PP PLACE_SIDE=BOTTOM
129 73 71 69 PPVBUS_USBC0 1 PPU8C0
69 PPHV_INT0_AONSW 1 PPU8C1
136 129 PP5V_S2SW_USBC01 1 PPU8C2
129 73 72 69 PPVBUS_USBC1 1 PPU8C3
69 PPHV_INT1_AONSW 1 PPU8C4
129 81 80 78 PPVBUS_USBC2 1 PPU8C5
78 PPHV_INT2_AONSW 1 PPU8C6
136 129 PP5V_S2SW_USBC23 1 PPU8C7
129 30 29 PPVBUS_USBC5 1 PPU8C8
129 32 PPHV_INT5_AONSW 1 PPU8C9
32 31 30 PPHV_DIV 1 PPU8D0
32 PD_ACE5_VCONN 1 PPU8D1

DCDC Debug 3mm PP
129 56 27 SMBUS_BATT_SCL BOTTOM 1 PPU8D2
129 56 27 SMBUS_BATT_SDA BOTTOM 1 PPU8D3

28 CHGR_COMP TOP 1 PPU8D4
28 CHGR_BGATE TOP 1 PPU8D5
48 47 P1V8VDDH_DRMOS_PWM1 TOP 1 PPU8D6
48 47 P1V8VDDH_DRMOS_PWM2 TOP 1 PPU8D7
49 47 P1V8VDDH_DRMOS_PWM3 TOP 1 PPU8D8

SPI_DISP_BKLT_MISO BOTTOM 1 PPU8D9
PLACE_NEAR=U0600.AP74:17MM

PPVDD_ANE0_SRAM_AWAKESW TRUE 137
PPVDD_GPU_SRAM0_AWAKESW TRUE 137
I2C_UPC0_ATCRTMR0_SCL TRUE 67 69 71 74 129
I2C_UPC0_ATCRTMR0_SDA TRUE 67 69 71 74 129

USBC0_CC1_CONN TRUE 73 76
USBC0_CC2_CONN TRUE 73 76
USBC1_CC1_CONN TRUE 73 76
USBC1_CC2_CONN TRUE 73 76
USBC2_CC1_CONN TRUE 76 81
USBC2_CC2_CONN TRUE 76 81

P5VS2TPS_PGOOD TRUE 29 35 54
HDMI_HPD_AOP TRUE 10 89
PMU_VDDHI_UVWARN_L TRUE 11 43
PMU_VDDMAIN_UVWARN_L TRUE 11 43
DBL_CLICK_DET TRUE 6 43
UPC_SMC_I2C_INT_L TRUE 10 56
P1V8VDDH_TLIMIT_THROTTLE_L TRUE 5 47
TP_AON_SLEEP1_RESET_L TRUE 10

PPVBUS_MID TRUE 29 130
HVSW_G1 TRUE 29
HVSW_G2 TRUE 29 130

USB-C (cont.) FUNC_TEST
I2C_UPC_SCL TRUE 6 32 55
I2C_UPC_SDA TRUE 6 32 55
I2C_UPC5_SCL TRUE 31
I2C_UPC5_SDA TRUE 31
P5VUSBC01_EN TRUE 75
P5VUSBC23_EN TRUE 83
USBC0_3V3LDO_EN TRUE 71 134
USBC1_3V3LDO_EN TRUE 72 141
USBC2_3V3LDO_EN TRUE 80 141

PMU_CRASH_L TRUE
USBC Debug 3mm PP PLACE_SIDE=BOTTOM
PMU_CRASH_SLAVE_L TRUE 39 43 128
CLVR_FABRIC_ILIMIT_THROTTLE_L TRUE 5 53
CLVR_RESET_L TRUE 43 50 51 52
P3V8AON_PWR_EN TRUE 27 28 33
P5VS2_PWR_EN TRUE 43 44
P5VS2TPS_PWR_EN TRUE 44 54 90
IPD_PWR_HOLD TRUE 39 44

NAND (cont.) FUNC_TEST
I2C_SMC_NAND_SCL TRUE 10 56
I2C_SMC_NAND_SDA TRUE 10 56
NAND0_OCARINA_VREF TRUE 101
NAND1_OCARINA_VREF TRUE 106
NAND1_S5E0_JTAG_TDO TRUE 102 103
P2V5_NAND0_PGOOD TRUE 101
P2V5_NAND1_PGOOD TRUE 106
PPVDD_LDO_NAND0_OCARINA TRUE 101
PPVDD_LDO_NAND1_OCARINA TRUE 106

SoC FUNC_TEST
SPI_SOCROM_1V8_CS_L TRUE 12
I2C_SEEPROM_SCL TRUE 6 12
I2C_SEEPROM_SDA TRUE 6 12

NAND (cont.) FUNC_TEST
NAND0_OCARINA_TDEV1 TRUE 101
NAND1_OCARINA_TDEV2 TRUE 106 130
NAND0_S5E0_JTAG_TDO TRUE 97 98
NAND0_S5E1_JTAG_TDO TRUE 98 99
NAND0_S5E2_JTAG_TDO TRUE 99 100
NAND1_OCARINA_TDEV1 TRUE 106
NAND1_OCARINA_TDEV2 TRUE 106 130
P2V5_NAND0_EN_R TRUE 101
P2V5_NAND1_EN_R TRUE 106

PMICs FUNC_TEST
PMU_CLK32K_CLVR TRUE 44 50 51 52
PMU_VDDHI TRUE 41
SPMI_NUB_MPMU_CLK TRUE 13 43
SPMI_NUB_MPMU_DATA TRUE 13 43
SPMI_NUB_SPMU_CLK TRUE 13 39
SPMI_NUB_SPMU_DATA TRUE 13 39
SWD_NUB_PMU_SWCLK TRUE 11 13
SWD_NUB_PMU_SWDIO TRUE 11 13
PMU_FAULT_OUT_L TRUE 39 43
DEBUG_SPMU_GPIO16 TRUE 44

WLBT FUNC_TEST
PMU_CLK32K_WLBT TRUE 44 95 96
TPT_WLAN_JTAG_TCK TRUE 95 96
TPT_WLAN_JTAG_TDI TRUE 95
TPT_WLAN_JTAG_TMS TRUE 95 96
TPT_WLAN_JTAG_TRSTN TRUE 95
WLBT_RESET_L 8 95 96 TP TPU867 TP-P4 TOP
BT_TIME_SYNC TRUE 6 95 96
WLBT_PWR_EN TRUE 43 44 95 96

IPD FUNC_TEST
CAPSLOCK_LED_EN TRUE 121
IOXP1_RESET_L TRUE 121
IOXP2_RESET_L TRUE 121
KBDBKLT_ISET_KEYB TRUE 120 129

Sensor FUNC_TEST
AIRFLOW_C_THMSNS TRUE 44 64
AIRFLOW_L_THMSNS TRUE 44 64
AIRFLOW_R_THMSNS TRUE 44 64
DCIN_VSENSE TRUE 43 58
FINSTACK_L_THMSNS TRUE 44 64
FINSTACK_R_THMSNS TRUE 44 64
MPMU_THMSNS TRUE 44 64
P1V8VDDH_THMSNS_1 TRUE 44 64
P1V8VDDH_THMSNS_2 TRUE 44 64
P1V8VDDH_THMSNS_3 TRUE 44 64
P3V8AON_THMSNS TRUE 44 64
PBUS_VSENSE TRUE 44 58
SOC_THMSNS_1 TRUE 44 64
SPMU_THMSNS TRUE 44 64
WING_L_THMSNS TRUE 44 64
WING_R_THMSNS TRUE 44 64
WLBT_THMSNS TRUE 44 64

SYNC_MASTER=SELIM SYNC_DATE=05/22/2023
PAGE TITLE
PMU TEST POINTS

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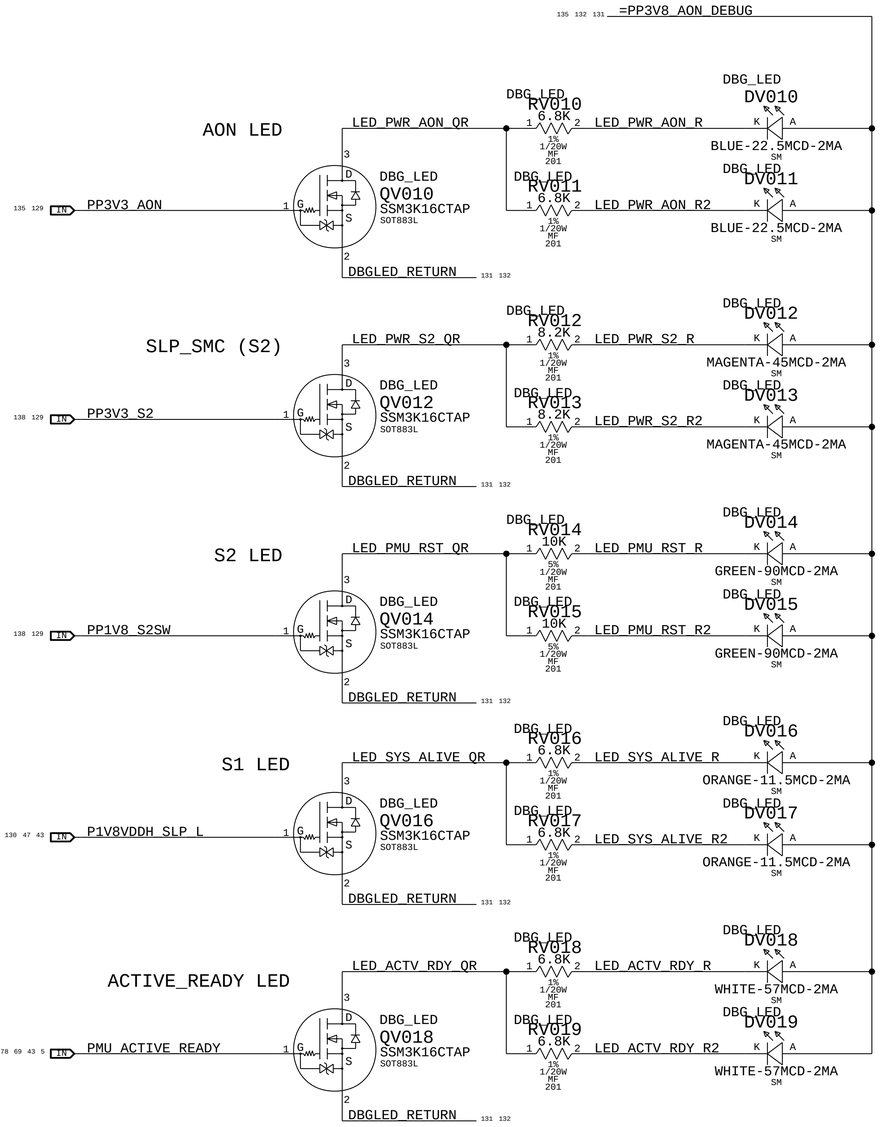
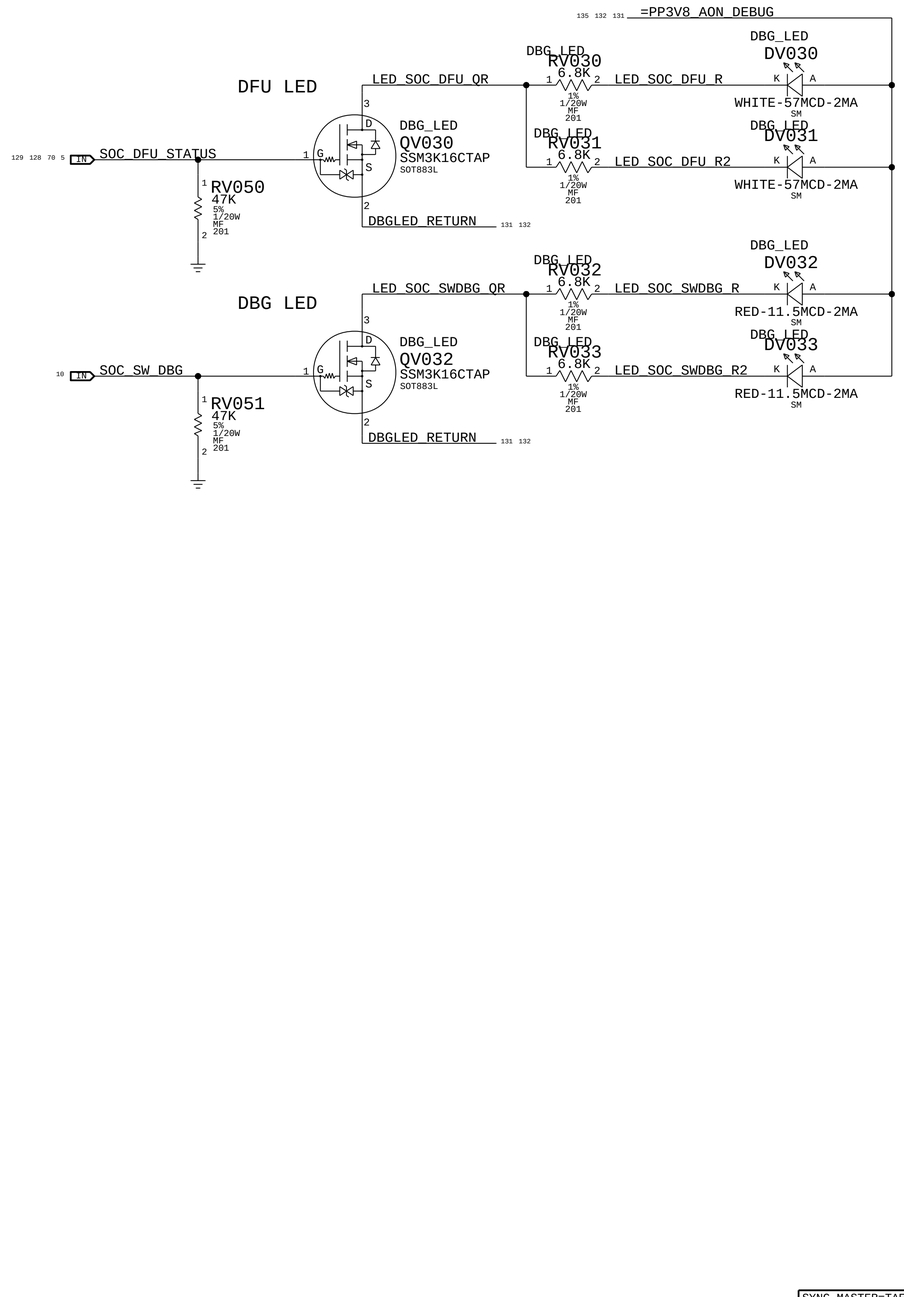
Debug LEDs





BOM_COST_GROUP=DEBUG

SYNC_MASTER=TAEWAN_T724 SYNC_DATE=03/23/2020

PAGE TITLE: Debug: LEDs, Koba

Apple Inc.

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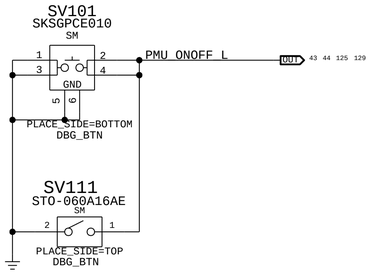
POWER BUTTON

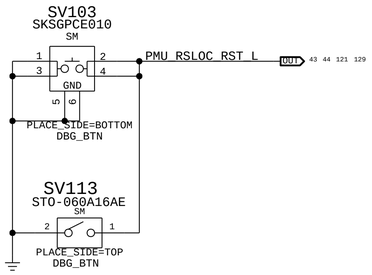
Imitate a user-facing Power Button press, many functions:
- Press to Wake from any state
- Combine with RSLOC (see RSLOC)
- Hold for 8sec to trigger "one-finger reset"
- - Similar to PMU RESET, except SW gets a warning to initiate panic-flow



RSLOC BUTTON

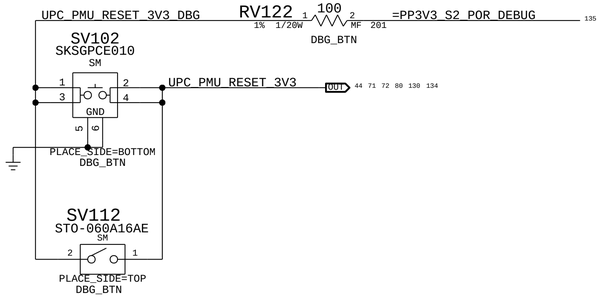
Imitate a user-facing key combo Right-Shift + Left-Option + Control:
- Hold RSLOC 4sec, then press Power Button to initiate PMU RESET
- Hold RSLOC 4sec, then hold Power Button 4sec to power-cycle P3V8AON VR
- Hold Power Button 1sec, then hold RSLOC 10sec to trigger PMU RESET into DFU

(continue holding first button when second button is added)



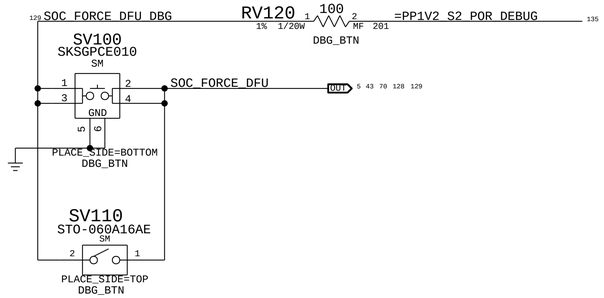
PMU RESET

PMU transitions to OFF and automatically proceeds up to AWAKE



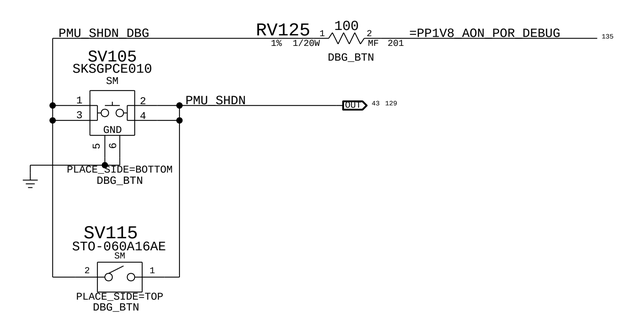
FORCE DFU

Hold during OFF->AWAKE transition to enter SOC's "Debug Firmware Update" mode



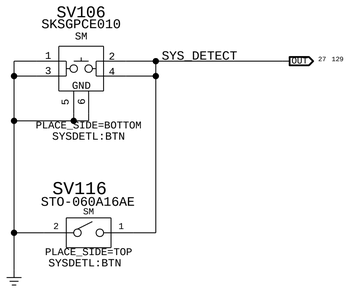
PMU SHUTDOWN

PMU transitions to OFF state and waits for a WAKE source*



SYS_DETECT (Battery Disconnect)

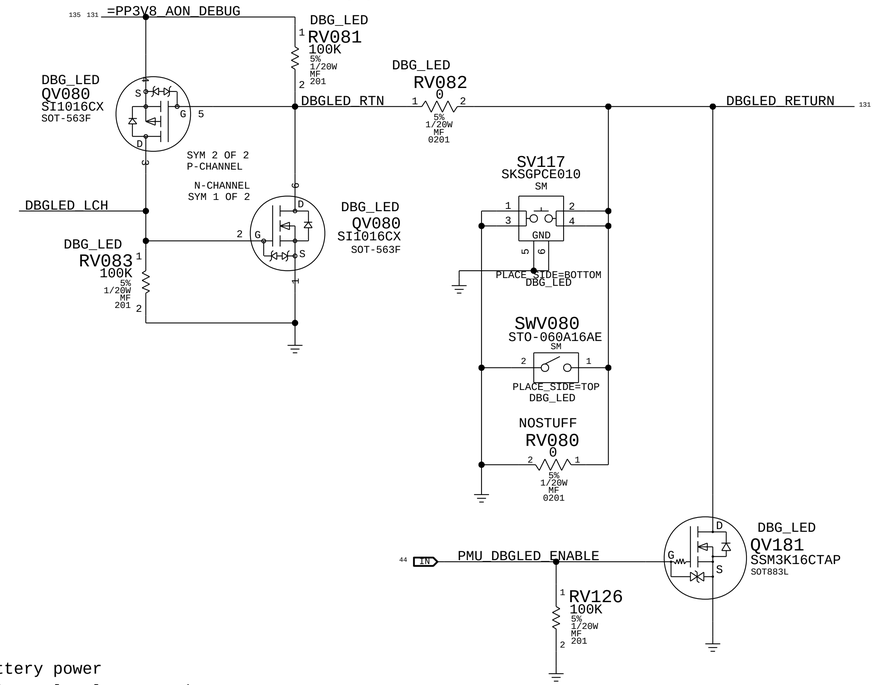
Imitate unplugging the battery signal flex, to disconnect MLB from Battery power
- Disconnect all DCIN sources, then hold SYS_DETECT for 2sec. MLB will completely power down



Debug LED Latch

Press button once to engage.
Remove power to disengage.

Debug LED Enable



*WAKE sources in OFF:
CHGR_AUX_OK (DCIN present)
IPD_LID_OPEN_1V8 (Lid is open)
PMU_ONOFF_L (User Power Button)

BOM_COST_GROUP=DEBUG

PAGE TITLE: Debug: Buttons

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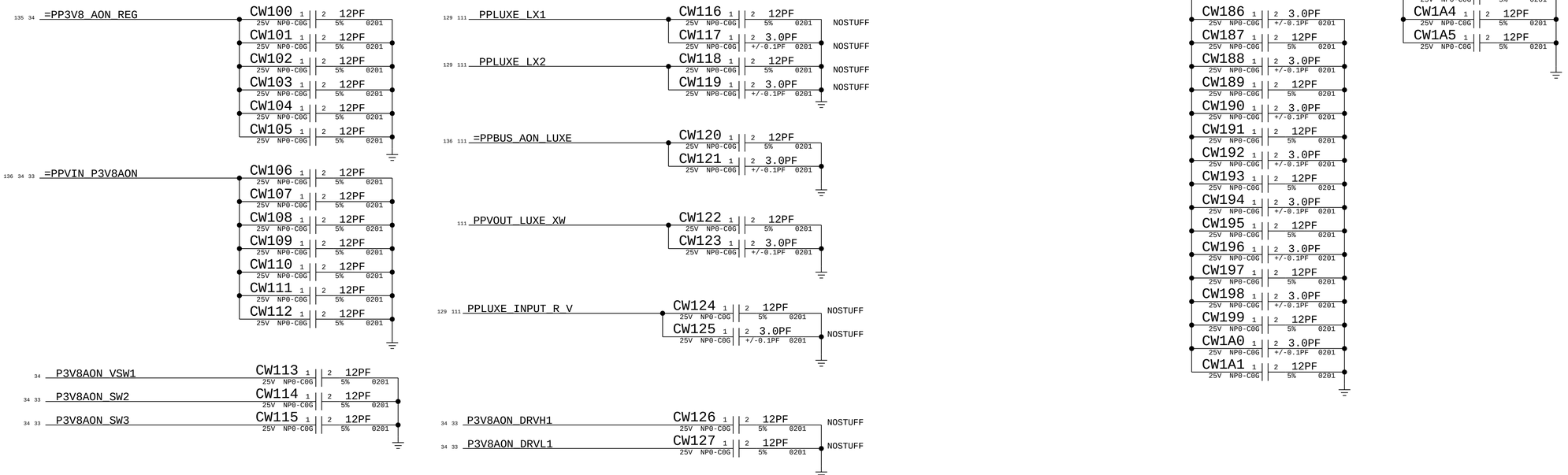
Desense Caps for every rail

1 pair for 1- and 2- phase BUCKs
2 pairs for 3- and 4- phase BUCKs



BOM_COST_GROUP=WIRELESS

PAGE TITLE: DESENSE_1

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SOC USB DFU MUX
=PP3V3_AON_DFUMUX_VC
PACK_OPTION=VITAMINC
VITAMIN-C:YES
RX412
20K
20K LIMITS USB MINI-B
FROM BACK POWERING MLB
CX410
0.1UF
PP3V3_AON_DFUMUX
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
2UA MAX IDD
LVL SHFTR
RX410
100K
VIT-C CONN
USB2_ATC0_VITC_CONN_P
USB2_ATC0_VITC_CONN_N
=USB2_ATC0_VITC_UPC_P
=USB2_ATC0_VITC_UPC_N
UX410
PI3USB102EZLE
TQFN-THICKSTNCL
CRITICAL
=USB2_ATC0_VITC_LS_P
=USB2_ATC0_VITC_LS_N
DFUMUX_SEL
DEBUG SPI ACE
SEL OUTPUT
L VIT-C (M)
H TYPE-C (D)
RX414
RX416
NO_XNET_CONNECTION=1
SOC DBG MUX
=PP3V3_AON_DBGMUX_VC
RX413
CX411
PP3V3_AON_DBGMUX_VC
RX411
UX411
USB_DBG_VITC_CONN_P
USB_DBG_VITC_CONN_N
=USB_DBG_VITC_UPC_P
=USB_DBG_VITC_UPC_N
=USB_DBG_VITC_LS_P
=USB_DBG_VITC_LS_N
KISMUX_SEL
RX415
RX417
PARROT DBG MUX
RX418
CX415
PP3V3_AON_DBGMUX
UX412
VITC_RTMR_RESET_L
VITC_RTMR_PWR_EN
ATCRTMR0_RESET_1V8_R_L
USBC0_3V3LDO_EN
=ATCRTMR0_RESET_1V8_L
=USB0_3V3_LDO_EN_VITC
RTMRMUX_OE_L
RX422
RX420
RX421
VITAMIC-C MK2 CONNECTOR
516S1074
SILK_PART=VITAMIN-C
JX401
AA25D-S038VA1
F-ST-SM
SOC ATC0 DFU
SOC KIS DBG
RFU
VITC_RESET_L
DFUMUX_SEL
KISMUX_SEL
SOC_DOCK_CONNECT_VITAMINC
TP_DC_MUX_SEL
UPC0_DBG3
UPC0_DBG2
DEBUG_JTAG_SOC_TDO
DEBUG_JTAG_SOC_TDI
UPC0_DBG0
UPC0_DBG1
UPC0_DBG4
UPC0_DBG5
VITC_RTMR_RESET_L
VITC_RTMR_PWR_EN
=PP1V8_S2_VITAMINC
=PP1V2_S2_VITAMINC
=PP3V8_AON_VITAMINC
=PP5V_S2_VITAMINC
KOBA
SOC UART
SMC UART
SWD_SOC_SWDIO
SWD_SOC_SWCLK
JTAG_SOC_TDO
JTAG_SOC_TDI
=PP3V3_S2_VITAMINC
RX430
100K
QX400
DMP2160UWQ
SOT323
UPC_PMU_RESET_3V3
CX405
CX406
CX404
2.2UF
CX401
CX402
CX403
TO SOC
1V2 NUB AOP, S2
47K PD ON SOC PAGE
SOC_DOCK_CONNECT
RX491
100
FROM ACE GPIO 7, PMOS OPEN DRAIN
1V2 S2
UPC0_GPIO7
RX492
10
FROM VITAMIN C
GPIO 7, 1V2 S2
SOC_DOCK_CONNECT_VITAMINC
BOM_COST_GROUP=DEBUG

SYNC_MASTER=T724_TKIM3_MLB_S_0.39.5 SYNC_DATE=09/18/2020

PAGE TITLE

DEBUG: VITAMIN-C

Apple Inc.

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BRANCH

VBAT

PPVBAT_G3H_CONN
- PPVBAT_AON (129)
  - MAKE_BASE=TRUE
  - MIN_LINE_WIDTH=0.6000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=13.05V
- PPVBAT_AON_CONN (27 28)

DCIN

69 =PPHV_EXT01_AONSW
- PPDCIN_AON (29 129)
  - MAKE_BASE=TRUE
  - MIN_LINE_WIDTH=0.6000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=20V
- =PPHV_EXT23_AONSW (78)
- =PPDCIN_AON_VSNS

PBUS

135 28 =PPBUS_AON_REG
- PPBUS_AON (129)
  - MAKE_BASE=TRUE
  - MIN_LINE_WIDTH=0.6000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=13.05V
- =PPBUS_AON_REG (28 135)
- =PPBUS_AON_MPMU (41)
- =PPVIN_P5VS2TPS_ISNS_R (58)
- =PPBUS_NAND0_ISNS_R (59)
- =PPBUS_NAND1_ISNS_R (59)
- =PPBUS_AON_SPKRAMP_ABC_ISNS_R (59)
- =PPBUS_AON_D_SPKRAMP (117 118)
- =PPBUS_AON_E_SPKRAMP (117)
- =PPBUS_AON_F_SPKRAMP (117)
- =PPVIN_5VUSBC01_ISNS_R (60)
- =PPVIN_5VUSBC23_ISNS_R (60)
- =PPVIN_P3V8AON_ISNS_R (58)
- =PPVIN_P1V8VDDH_ISNS_R (58)
- =PPBUS_AON_VSNS (58)
- =PPVIN_P3V3SD_ISNS_R (60)
- =PPBUS_AON_LUXE_ISNS_R (60)
- =PPBUS_TPAD (124)
- =PPBUS_AON_FAN (66)
- =PPBUS_AON_SNS (35)

ICEMAN VMAIN

133 34 =PP3V8_AON_REG
- PP3V8_AON (129)
  - MAKE_BASE=TRUE
  - MIN_LINE_WIDTH=0.6000
  - MIN_NECK_WIDTH=0.1000
  - VOLTAGE=3.8V
- =PP3V8_AON_SE (26)
- =PP3V8_AON_MPMU_ISNS_R (59)
- =PP3V8_AON_SPMU_ISNS_R (59)
- =PP3V8_ATC01_LDO_ISNS_R (61)
- =PP3V8_ATC2_LDO_ISNS_R (61)
- =PPVIN_P3V8NAND0_ISNS_R (61)
- =PPVIN_P3V8NAND1_ISNS_R (61)
- =PP3V8_AON_CODEC (115)
- =PP3V8_AON_A_SPKRAMP (116)
- =PP3V8_AON_B_SPKRAMP (116)
- =PP3V8_AON_C_SPKRAMP (116)
- =PP3V8_AON_D_SPKRAMP (117)
- =PP3V8_AON_E_SPKRAMP (117)
- =PP3V8_AON_F_SPKRAMP (117)
- =PP3V8_AON_TOUCHID (126)
- =PP3V8_AON_LCD
- =PP3V8_IPDLDO_VIN_ISNS_R (62)
- =PP3V8_AON_HDMI_LDO (90)
- =PPPANEL_LCD_SW_VIN
- =PP3V8_AON_BKLTCONN_ISNS_R
- =PP3V8_AON_LCD_SW_VIN (110)
- =PP3V8_AON_WLBT_ISNS_R (62)
- =PP3V8_AON_SYSDET (27)
- =PP3V8_AON_DEBUG (131 132)
- =PP3V8_AON_VITAMINC (134)
- =PP3V8_AON_SNS (35 58 63 64)
- =PP3V8_AON_P5VS2TPS (54)

PP5V_S2

54 =PP5V_S2_TPS_REG
- PP5V_S2_MAIN (30 129)
  - MAKE_BASE=TRUE
  - VOLTAGE=5.0V
- =PP5V_P3V8AON_VDRV (33)
- =PP5V_P1V8VDDH_CTRL (47)
- =PP5V_P1V8VDDH_DRMOS (48 49)
- =PP5V_S2_HDMI_XW (90)
- =PP5V_S2_LUXE (111)
- =PP5V_KBDBKLT_ISNS_R (62)
- =PP5V_S2_TPAD (124)
- =PP5V_S2_CAMERA_ISNS_R (62)
- =PP5V_S2_BIAS (89)
- =PP5V_S2_TOUCHIDBKLT (122 127)
- =PP5V_CHGR_VDDA (29)
- =PP5V_S2_SNS (35)
- =PP5V_S2_VITAMINC (134)
- =PP5V_S2_DBG_FAN (66)

PP1V2 AWAKE SYSTEM LOADS

139 40 38 36 =PP1V225_AWAKE_REG

SPMU Buck12(8)
- =PP1V225_AWAKE_SD (93)
- =PP1V2_AWAKE_LUXE (111)
- =PP1V2_AWAKE_CODEC (115)
- =PP1V2_AWAKE_IO (115 116)
- =PP1V2_AWAKE_SPKRAMP (116 117)
- =PP1V2_AWAKE_I2C_PU (55)
- =PP1V2_AWAKE_CAM_LS (57)
- =PP1V225_AWAKE_TCONUART_LS (109)
- =PPVDD_AWAKE_SD_I2C_PU (93)

PP1V2 S2 SYSTEM LOADS

138 42 40 36 =PP1V2_S2_REG

MPMU Buck8(8)
- =PP1V25_S2_SE (26)
- =PP1V2_S2_CHGR (29)
- =PP1V225_S2_ACE5 (31 32)
- =PP1V2_P1V8VDDH_CTR (47)
- =PP1V2_S2_I2C_PU (55 56 57)
- =PP1V25_S2_ACE01 (69 71 72 130)
- =PP1V2_S2_LSTXRX (74 82)
- =PP1V25_S2_ACE23 (78 80)
- =PP1V2_S2_SD (93)
- =PP1V2_S2_WLBT_IO (95)
- =PP1V2_S2_LAS (113)
- =PP1V2_S2_SECDIS (114)
- =PP1V2_KBDBKLTPWM (120)
- =PP1V2_S2_IMU_LS (14 65)
- =PP1V2_S2_IPD_LS (123)
- =PP1V2_S2_HDMI_HPD (89)
- =PP1V2_S2_POR_DEBUG (132)
- =PP1V2_S2_TOUCHIDBKLTPWM (127)
- =PP1V2_S2_CODEC (115)
- =PP1V2_S2_FAN_PU (66)
- =PP1V2_S2_SENSOR_LS (14)
- =PP1V2_S2_MISC
- =PP1V2_S2_TOUCHID_LS (125)
- =PP1V2_S2_TOUCHID_PU (125)
- =PP1V2_S2_VITAMINC (134)
- =PP1V2_S2_MACAW_RESET

SPMU 1V8 S2 SYSTEM LOADS

139 40 38 36 =PP1V8_S2_REG

SPMU Buck19(3)
- =PP1V8_S2_SPMU_SW1 (37)
- =PP1V8_S2_SE (26)
- =PP1V8_S2_CHGR (28 29)
- =PP1V8_S2_DBGUPC (70)
- =PP1V8_S2_DBGUSBLS (70)
- =PP1V8_S2_UPC01 (70 75)
- =PP1V8_S2_EUSBLS1 (70 74)
- =PP1V8_S2_WLBT (95)
- =PP1V8_S2_NAND0 (101)
- =PP1V8_S2_NAND1 (106)
- =PP1V8_DISP_TEMP (109)
- =PP1V8_S2_SECDIS (114)
- =PP1V8_S2_DMIC (119)
- =PP1V8_S2_SENSOR_LS (14)
- =PP1V8_S2_IMU (65)
- =PP1V8_S2_IMU_LS (65)
- =PP1V8_S2_I2C_PU (55 56 57)
- =PP1V8_S2_HDMI_ISNS_R (62)
- =PP1V8_S2_UPC23 (79 83)
- =PP1V8_S2_SPMU_LDO3 (37)
- =PP1V8_S2_ATC2_LRD (84)
- =PP1V8_S2_SD
- =PP1V8_S2_VITAMINC (134)
- =PP1V8_S2_CAM_LS (57)
- =PP1V8_S2_MACAW_RESET

MPMU LDO1 S2 SYSTEM LOADS

138 41 =PP3V3_S2_UPC_REG

MPMU LDO1
- =PP3V3_S2_FAN (66)
- =PP3V3_S2_ACE01 (69 71 72)
- =PP3V3_S2_ACE23 (78 80)
- =PP3V3_S2_SD (93)
- =PP3V3_KBDBKLTPWM (120)
- =PP3V3_S2_HDMI_HPD (89)
- =PP3V3_S2_POR_DEBUG (132)
- =PP3V3_S2_I2C_PU (56)
- =PP3V3_S2_TOUCHIDBKLTPWM (127)
- =PP3V3_S2_ACE5 (29)
- =PP3V3_S2_5VEN_UPC01
- =PP3V3_S2_5VEN_UPC23
- =PP3V3_S2_VITAMINC (134)

MPMU 3V3 AON SYSTEM LOADS

41 =PP3V3_AON_REG

MPMU LDO4

Portable Only
- PP3V3_AON (129 131)
  - MAKE_BASE=TRUE
  - VOLTAGE=3.3V
- =PP3V3_AON_KBD (121)
- =PP3V3_AON_CHGRRST (44)
- =PP3V3_AON_LAS (113)
- =PP3V3_AON_SYSDET (27)
- =PP3V3_AON_DBGMUX_VC (134)
- =PP3V3_AON_DFUMUX_VC (134)
- =PP3V3_AON_KBD_LEDDRIVER_R (121)

PP1V8_AON SYSTEM LOADS

138 41 =PP1V8_AON_REG

MPMU LDO1V8
- =PP1V8_AON_LAS (113 114)
- =PP1V8_AON_POR_DEBUG (132)
- =PP1V8_AON_CHGR (29)
- =PP1V8_AON_CHGRRST (44)
- =PP1V8_AON_LCD_SW_VIN (110)
- =PP1V8_PMUOSC (43)

PP1V8 AWAKE SYSTEM LOADS

139 37 =PP1V8_AWAKE_SPMU_FET

SPMU SW0
- =PP1V8_AWAKE_CODEC (115)
- =PP1V8_AWAKE_SPKRAMP (116 117)
- =PP1V8_AWAKE_CAM_LS (57)

PP1V2 SPMU LDO3 AWAKE SYSTEM LOADS

37 =PP1V2_AWAKESW_BLC_REG

SPMU_LDO3
- PP1V2_AWAKESW_BLC (129)
  - MAKE_BASE=TRUE
  - VOLTAGE=1.2V
  - MIN_LINE_WIDTH=0.2000
  - MIN_NECK_WIDTH=0.1000
- =PP1V2_AWAKE_BKLTCONN (112)

PP1V8 SPMU SW1 S2 SYSTEM LOADS

37 =PP1V8_S2SW_SNS_FET

SPMU_SW1
- PP1V8_S2SW_SNS (129)
  - MAKE_BASE=TRUE
  - VOLTAGE=1.8V
  - MIN_LINE_WIDTH=0.2000
  - MIN_NECK_WIDTH=0.1000
- =PP1V8_S2SW_SNS (58 59 60 61 62)

DISPLAY POWER SEQUENCER OUTPUT

110 =PPBCON_SW_REG
- PPBCON_AWAKESW_BKLTCONN
  - MAKE_BASE=TRUE
  - VOLTAGE=3.8V
  - MIN_LINE_WIDTH=0.6000
  - MIN_NECK_WIDTH=0.1000
- =PP3V8_AWAKE_BKLTCONN_ISNS_R (62)

110 =PPMDB_SW_FET
- PPPANEL_SW_LCD_REG (129)
  - MAKE_BASE=TRUE
  - VOLTAGE=3.8V
  - MIN_LINE_WIDTH=0.6000
  - MIN_NECK_WIDTH=0.1000
- =PP3V8_AWAKE_TCON_ISNS_R (61)

ICEMAN LDO5 OUTPUT

33 =PP5V_AON_LDO5_REG
- PP5V_AON_P3V8AON
  - MAKE_BASE=TRUE
  - VOLTAGE=5.0V
  - MIN_LINE_WIDTH=0.2000
  - MIN_NECK_WIDTH=0.1000
- =PPVDD_3V8AONFAULTPU (33)

SYNC_MASTER=DTUZMAN SYNC_DATE=01/31/2020

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USBC REQUIRED POWER ALIASES

PP3V3_S2SW_USBC0 (129) — MAKE_BASE=TRUE — VOLTAGE=3.3V
- =PP3V3_S2_USB0_REG (67)
- =PP3V3_ATCRTMR0_SX (67 69)
- =PP3V3_ATCRTMR0 (67 69)
- =PP3V3_S2_USBLS0 (74)
- =PP3V3_S2_USBE0 (74)

PP3V3_S2SW_USBC1 (129) — MAKE_BASE=TRUE — VOLTAGE=3.3V
- =PP3V3_S2_USB1_REG (68)
- =PP3V3_ATCRTMR1_SX (68 69)
- =PP3V3_ATCRTMR1 (68 69)
- =PP3V3_S2_USBLS1 (74)
- =PP3V3_S2_USBE1 (74)

PP3V3_S2SW_USBC2 (129) — MAKE_BASE=TRUE — VOLTAGE=3.3V
- =PP3V3_S2_USB2_REG (77)
- =PP3V3_ATCRTMR2_SX (77 78)
- =PP3V3_ATCRTMR2 (77 78)
- =PP3V3_S2_USBLS2 (82)
- =PP3V3_S2_USBE2 (82)

(75) =PP5V_USBC01_REG
POWER FROM LOCAL USBC 5V VRS TO ACE01.
→ VOLTAGE=5V, MAKE_BASE=TRUE: PP5V_S2SW_USBC01 (129 130)
- =PP5V_S2_ACE01 (OUT 71 72)
- =PP5V_S2_ACE01_VCONN (OUT 71 72)

(83) =PP5V_USBC23_REG
POWER FROM LOCAL USBC 5V VRS TO ACE23.
Power rail for ports 2,3 only
→ VOLTAGE=5V, MAKE_BASE=TRUE: PP5V_S2SW_USBC23 (129 130)
- =PP5V_S2_ACE23 (OUT 80)
- =PP5V_S2_ACE23_VCONN (OUT 80)

KEYBOARD BACKLIGHT

(120) =PPVOUT_KBDBKLT_REG
→ VOLTAGE=41.4V, MAKE_BASE=TRUE: PPVOUT_KBDLED_CONN (129)
- =PPVOUT_KBDLED_CONN (OUT 122)

PBUS FAN SWITCH ALIAS

(66) =PPBUS_AON_FAN0_FILT
→ VOLTAGE=13.05V, MAKE_BASE=TRUE: PPBUS_AONSW_FAN_LEFT (129)
- =PPBUS_AONSW_FAN_LEFT_ISNS_R (OUT 61)

IPD: KEYBOARD / TRACKPAD

PP3V3_S2_IPD (LDO) ALIASES

(123) =PP3V3_S2_IPD_REG
→ PP3V3_S2_IPD (129) — MAKE_BASE=TRUE — VOLTAGE=3.3V
- =PP3V3_S2_TPAD (124)
- =PP3V3_S2_KBD_LEDDRIVER_R (121)

PP1V85_S2_IPD (LDO) ALIASES

(123) =PP1V85_S2_IPD_REG
→ PP1V85_S2_IPD (129) — MAKE_BASE=TRUE — VOLTAGE=1.85
- =PP1V85_S2_IPD_LS (57 123)
- =PP1V83V3_S2_KBDIOXI2C (121)
- =PP1V8_S2_KBD (121 122)
- =PP1V85_S2_TPAD_CONN (124)

OUTPUT SENSOR ALIASES

(133 58) =PPVIN_P1V8VDDH_ISNS
→ PPVIN_P1V8VDDH — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPVIN_P1V8VDDH_CTRL (47)
- =PPVIN_P1V8VDDH_DRMOS (46 48 49)

(58) =PPVIN_P3V8AON_ISNS
→ PPVIN_P3V8AON — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPVIN_P3V8AON (33 34 133)

(58) =PPVIN_P5VS2TPS_ISNS
→ PPVIN_P5VS2 — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPVIN_P5VS2TPS (54)

(59) =PP3V8_AON_MPMU_ISNS
→ PP3V8_AON_MPMU — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
- =PP3V8_AON_MPMU (41 44)
- =PP3V8_AON_MPMU_LDO4 (41)

(59) =PP3V8_AON_SPMU_ISNS
→ PP3V8_AON_SPMU — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
- =PP3V8_AON_SPMU (37 44)

(61) =PPVIN_P3V8NAND0_ISNS
→ PPVIN_P3V8NAND0 — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
- =PPVIN_P3V8NAND0 (101)

(61) =PPVIN_P3V8NAND1_ISNS
→ PPVIN_P3V8NAND1 — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
- =PPVIN_P3V8NAND1 (106)

(61) =PP3V8_ATC01_LDO_ISNS
→ PP3V8_ATC01_LDO — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
- =PP3V8_ATC0_LDO (67)
- =PP3V8_ATC1_LDO (68)

(60) =PPBUS_AON_LUXE_ISNS
→ PPBUS_AON_LUXE — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPBUS_AON_LUXE (111 133)
- =PPBUS_AON_LUXE_VIN (111)

(59) =PPBUS_NAND0_ISNS
→ PPBUS_NAND0 — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPBUS_NAND0 (101)

(59) =PPBUS_NAND1_ISNS
→ PPBUS_NAND1 — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPBUS_NAND1 (106)

(59) =PPBUS_AON_SPKRAMP_ABC_ISNS
→ PPBUS_AON_SPKRAMP_ABC — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPBUS_AON_A_SPKRAMP (116 118)
- =PPBUS_AON_B_SPKRAMP (116)
- =PPBUS_AON_C_SPKRAMP (116)

(60) =PPVIN_P3V3SD_ISNS
→ PPVIN_P3V3SD — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPVIN_P3V3SD (94)

(60) =PPVIN_5VUSBC01_ISNS
→ PPVIN_5VUSBC01 — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPVIN_5VUSBC01 (75)

(60) =PPVIN_5VUSBC23_ISNS
→ PPVIN_5VUSBC23 — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPVIN_5VUSBC23 (83)

(61) =PP3V3_ATC2_LDO_ISNS
→ PP3V3_ATC2_LDO — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
- =PP3V3_ATC2_LDO (77)

(61) =PP3V3_AWAKE_TCON_ISNS
→ PP3V3_AWAKE_TCON — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.3V
- =PP3V3_AWAKE_TCON (109)

(62) =PP3V3_AWAKE_BKLTCONN_ISNS
→ PP3V3_AWAKE_BKLTCONN — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.3V
- =PP3V3_AWAKE_BKLTCONN (112)

(62) =PP1V8_S2_HDMI_ISNS
→ PP1V8_S2_HDMI — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=1.8V
- =PP1V8_S2_HDMI (90)

(62) =PP3V8_AON_WLBT_ISNS
→ PP3V8_AON_WLBT — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
- =PP3V8_AON_WLBT (95)

(62) =PP5V_S2_CAMERA_ISNS
→ PP5V_S2_CAMERA — MAKE_BASE=TRUE, VOLTAGE=5.0V
- =PP5V_S2_CAMERA (108)

(62) =PP3V8_IPDLDO_VIN_ISNS
→ PP3V8_IPDLDO_VIN — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1000, VOLTAGE=3.8V
- =PP3V8_IPD1V85LDO_VIN (123)
- =PP3V8_IPD3V3LDO_VIN (123)

(62) =PP5V_KBDBKLT_ISNS
→ PP5V_KBDBKLT — MAKE_BASE=TRUE, VOLTAGE=5.0V
- =PP5V_KBDBKLT (120)
- =PP5V_KBDBKLT_BEN (120)

(61) =PPBUS_AONSW_FAN_LEFT_ISNS
→ PPBUS_AON_FAN0_CONN — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, VOLTAGE=13.05V
- =PPBUS_AON_FAN0_CONN (66)

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=M0_BUCK0
Monaco0 Buck 0
PPVDD_PCPU1_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_PCPU1_AWAKESW

=M0_BUCK1
Monaco0 Buck 1
PPVDD_PCPU_SRAM1_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_PCPU_SRAM1_AWAKESW

=M0_BUCK2
Monaco0 Buck 2
PPVDD_PCPU0_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_PCPU0_AWAKESW

=M0_BUCK3
Monaco0 Buck 3
PPVDD_PCPU_SRAM0_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_PCPU_SRAM0_AWAKESW

=M1_BUCK0
Monaco1 Buck 0
PPVDD_GPU1_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_GPU1_AWAKESW

=M1_BUCK1
Monaco1 Buck 1
PPVDD_GPU_SRAM1_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_GPU_SRAM1_AWAKESW

=M1_BUCK2
Monaco1 Buck 2
PPVDD_GPU0_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_GPU0_AWAKESW

=M1_BUCK3
Monaco1 Buck 3
PPVDD_GPU_SRAM0_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_GPU_SRAM0_AWAKESW

=M4_BUCK0
Monaco4 Buck 0
PPVDD_ANE0_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_ANE0_AWAKESW

=M4_BUCK1
Monaco4 Buck 1
PPVDD_ANE0_SRAM_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_ANE0_SRAM_AWAKESW

=M4_BUCK2
Monaco4 Buck 2
PPVDD_FABRIC_S1
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_FABRIC_S1

=M4_BUCK3
Monaco4 Buck 3
PPVDD_AFR_AWAKESW
MAKE_BASE=TRUE
VOLTAGE=1.11V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_AFR_AWAKESW

=PP1V8_S1_MON_REG
Viper -> Monaco VDDH
PP1V8_S1_CLVR_VDDH
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V8_S1_CLVR_VDDH
=PP1V8_S1_MON_VDDH_FB
=PP1V8_S1_CLVR_VDDH_VSNS

Monaco0

=M0_BUCK0_FB
PVDDPCPU1AWAKESW_FB
MAKE_BASE=TRUE

=M0_BUCK1_FB
PVDDPCPUSRAM1AWAKESW_FB
MAKE_BASE=TRUE

=M0_BUCK2_FB
PVDDPCPU0AWAKESW_FB
MAKE_BASE=TRUE

=M0_BUCK3_FB
PVDDPCPUSRAM0AWAKESW_FB
MAKE_BASE=TRUE

Monaco1

=M1_BUCK0_FB
PVDDGPU1AWAKESW_FB
MAKE_BASE=TRUE

=M1_BUCK1_FB
PVDDGPUSRAM1AWAKESW_FB
MAKE_BASE=TRUE

=M1_BUCK2_FB
PVDDGPU0AWAKESW_FB
MAKE_BASE=TRUE

=M1_BUCK3_FB
PVDDGPUSRAM0AWAKESW_FB
MAKE_BASE=TRUE

Monaco4

=M4_BUCK0_FB
PVDDANE0AWAKESW_FB
MAKE_BASE=TRUE

=M4_BUCK1_FB
PVDDANE0SRAMAWAKESW_FB
MAKE_BASE=TRUE

=M4_BUCK2_FB
PVDDFABRICS1_FB
MAKE_BASE=TRUE

=M4_BUCK3_FB
PVDDAFRAWAKESW_FB
MAKE_BASE=TRUE

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42 40 36 =PPVDD_ECPU_AWAKE_REG
MPMU Buck0(0)
PPVDD_ECPU_AWAKE 14 129
VOLTAGE=1.11V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_ECPU_AWAKE 15
=PPVDD_ECPU_AWAKE_FB 42

42 40 36 =PPVDD_GPU_BMPR_S1_REG
MPMU Buck1(1)
PPVDD_GPU_BMPR_S1 129
VOLTAGE=0.9V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_GPU_BMPR_S1 15
=PPVDD_GPU_BMPR_S1_FB 42

42 40 36 =PPVDD_ECPU_SRAM_AWAKE_REG
MPMU Buck2(2)
PPVDD_ECPU_SRAM_AWAKE
VOLTAGE=1.11V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_ECPU_SRAM_AWAKE 16
=PPVDD_ECPU_SRAM_AWAKE_FB 42

42 40 36 =PP1V8_S2SW_REG
MPMU Buck3(3)
PP1V8_S2SW 129 131
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V8_S2SW_VDD1_SOC 17
=PP1V8_S2_CLVR_VDDC 50 51 52
=PP1V8_S2SW_FB 42

42 40 36 =PPVDD2H1_S2SW_REG
MPMU Buck4(4)
PPVDD2H1_S2SW 129
VOLTAGE=1.15V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD2H1_S2SW 23
=PPVDD2H1_S2SW_FB 42

42 40 36 =PPVDD_AVEMSR_AWAKESW_REG
MPMU Buck5(5)
PPVDD_AVEMSR_AWAKESW 129
VOLTAGE=0.945V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_AVEMSR_AWAKESW 19
=PPVDD_AVEMSR_AWAKESW_FB 42

42 40 36 =PPVDD_AMPH1_S2SW_REG
MPMU Buck6(6)
PPVDD_AMPH1_S2SW 129
VOLTAGE=1.15V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_AMPH1_S2SW 19
=PPVDD_AMPH1_S2SW_FB 42

42 40 36 =PP0V81_S1_SRAM_REG
MPMU Buck7(7)
PP0V81_S1_SRAM 129
VOLTAGE=0.81V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP0V81_S1_SRAM 16
=PP0V81_S1_SRAM_FB 42

135 42 40 36 =PP1V2_S2_REG
MPMU Buck8(8)
PP1V2_S2 129
VOLTAGE=1.225V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V2_S2_SOC 21
=PP1V2_S2_CIO 21
=PP1V2_S2_AMUX 21
=PP1V2_S2_PU 5 10
=PP1V2_S2_MPMU 41 43 44
=PP1V2_S2_SPMU 37
=PP1V2_S2_FB 42

42 40 36 =PPVDD_FIXED_S1_REG
MPMU Buck9(9)
PPVDD_FIXED_S1 129
VOLTAGE=0.84V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_FIXED_S1 20
=PPVDD_FIXED_S1_PCIE_ST 20
=PPVDD_FIXED_S1_PCIE_GP 20
=PPVDD_FIXED_S1_MTR 20
=PPVDD_FIXED_S1_MIPI 20
=PPVDD_FIXED_S1_LPDP 20
=PPVDD_FIXED_S1_PLL 20
=PPVDD_FIXED_S1_FB 42

42 40 36 =PP0V575_S1_VDDQ1_REG
MPMU Buck10(10)
PP0V575_S1_VDDQ1 129
VOLTAGE=0.575V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP0V575_S1_VDDQ1 5 18
=PP0V575_S1_VDDQ1_FB 42

MPMU LDO0

135 41 =PP3V3_S2_UPC_REG
MPMU LDO1
PP3V3_S2 129 131
VOLTAGE=3.3V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1000
=PP3V3_S2_UPC_MPMU 41
=PP3V3_S2_UPC_SPMU 37

41 =PP1V8_S2SW_CLVR_VDDC1_MPMU_REG
MPMU LDO2
PP1V8_S2SW_CLVR_VDDC1_LDO 129
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.1000
=PP1V8_CLVR_VDDC1 50

MPMU LDO3

MPMU LDO4

41 =PP0V8_S2_CLVR_VDDDIG_REG
MPMU LDO5
PP0V8_S2_CLVR_VDDDIG 129
VOLTAGE=0.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP0V8_S2_CLVR_VDDDIG 50 51 52

MPMU LDO6

135 41 =PP1V8_AON_REG
MPMU LDO1V8
PP1V8_AON 129
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V8_AON_MPMU 43 44

41 =PP1V2_AON_REG
MPMU LDO1V2
PP1V2_AON 129
VOLTAGE=1.2V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V2_AON_MPMU 41 43 44

41 =PP1V2_S2_CLVR_VDDIO_FET
MPMU SW0
PP1V2_S2_CLVR_VDDIO 129
VOLTAGE=1.2V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V2_S2_CLVR_VDDIO 50 51 52 53

MPMU SW1

MPMU SW2

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=PPVDD_DCS_S1_REG
SPMU Buck17(0)
PPVDD_DCS_S1
VOLTAGE=1.05V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_DCS_S1
=PPVDD_DCS_S1_FB

=PP0V575_S1_VDDQ0_REG
SPMU Buck13(1)
PP0V575_S1_VDDQ0
VOLTAGE=0.575V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP0V575_S1_VDDQ0
=PP0V575_S1_VDDQ0_FB

=PP0V95_S2SW_VDD2L_REG
SPMU Buck18(2)
PP0V95_S2SW_VDD2L
VOLTAGE=0.95V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP0V95_S2SW_VDD2L
=PP0V95_S2SW_VDD2L_FB

=PP1V8_S2_REG
SPMU Buck19(3)
PP1V8_S2
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V8_S2_MPMU
=PP1V8_S2_SPMU
=PP1V8_S2_FB

=PPVDD2H0_S2SW_REG
SPMU Buck14(4)
PPVDD2H0_S2SW
VOLTAGE=1.15V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD2H0_S2SW
=PPVDD2H0_S2SW_FB

=PPVDD_SOC_S1_REG
SPMU Buck11(5)
PPVDD_SOC_S1
VOLTAGE=0.84V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_SOC_S1
=PPVDD_SOC_S1_FB

=PP0V855_S2_VDDCIO_REG
SPMU Buck16(6)
PP0V855_S2SW_VDDCIO
VOLTAGE=0.89V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP0V855_S2_VDDCIO
=PP0V855_S2_VDDCIO_FB

=PPVDD_DISP2_AWAKESW_REG
SPMU Buck15(7)
Not used on sC designs
PPVDD_DISP2_AWAKESW
VOLTAGE=1.11V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0840
MIN_NECK_WIDTH=0.0840
=PPVDD_DISP2_AWAKESW
=PPVDD_DISP2_AWAKESW_FB

=PP1V225_AWAKE_REG
SPMU Buck12(8)
* Base Net Voltage truncated
PP1V2_AWAKE
VOLTAGE=1.225V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V225_AWAKE_DCS
=PP1V225_AWAKE_LPDP
=PP1V225_AWAKE_MIPI
=PP1V225_AWAKE_MTR
=PP1V225_AWAKE_PCIE_GP
=PP1V225_AWAKE_PCIE_ST
=PP1V225_AWAKE_PLL
=PP1V225_AWAKE_PU
=PP1V225_AWAKE_SEPROM
=PP1V225_AWAKE_SOC
=PP1V225_AWAKE_SOCROM
=PP1V225_AWAKE_TSADC
=PP1V225_AWAKE_VDDA_AFR
=PP1V225_AWAKE_VDDA_GPUN
=PP1V225_AWAKE_SPMU
=PP1V225_AWAKE_MPMU
=PP1V225_AWAKE_FB

=PPVDD_AMPH0_S2SW_REG
SPMU Buck21(9)
PPVDD_AMPH0_S2SW
VOLTAGE=1.15V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_AMPH0_S2SW
=PPVDD_AMPH0_S2SW_FB

=PPVDD_DISP_AWAKESW_REG
SPMU Buck20(10)
PPVDD_DISP_AWAKESW
VOLTAGE=1.11V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PPVDD_DISP_AWAKESW
=PPVDD_DISP_AWAKESW_FB

=PP0V72_S2_VDDLOW_REG
SPMU LDO0
PP0V72_S2_VDDLOW
VOLTAGE=0.72V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP0V72_S2_HIB
=PP0V72_S2_CIO_KIS
=PP0V72_S2_LOW

SPMU LDO1

SPMU LDO2

SPMU LDO3

SPMU LDO4

SPMU LDO5

SPMU LDO6

SPMU LDO1V8
-Internal Only-

SPMU LDO1V2
-Internal Only-

=PP1V8_AWAKE_SPMU_FET
SPMU SW0
PP1V8_AWAKE
VOLTAGE=1.8V
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
=PP1V8_AWAKE_SOCROM
=PP1V8_AWAKE_SEPROM

SPMU SW1

SPMU SW2

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LPDPTX

7	LPDP_INT_ML_DATA_C_P<0>		LPDP_INT_DATA_C_P<0>	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_DATA_C_N<0>		LPDP_INT_DATA_C_N<0>	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_DATA_C_P<1>		LPDP_INT_DATA_C_P<1>	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_DATA_C_N<1>		LPDP_INT_DATA_C_N<1>	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_DATA_C_P<2>		LPDP_INT_DATA_C_P<2>	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_DATA_C_N<2>		LPDP_INT_DATA_C_N<2>	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_DATA_C_P<3>		LPDP_INT_DATA_C_P<3>	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_DATA_C_N<3>		LPDP_INT_DATA_C_N<3>	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_AUX_C_P		LPDP_INT_AUX_C_P	109	MAKE_BASE=TRUE
7	LPDP_INT_ML_AUX_C_N		LPDP_INT_AUX_C_N	109	MAKE_BASE=TRUE
142 7	LPDP_INT_ML_HPD		LPDP_INT_HPD	109 129 142	MAKE_BASE=TRUE
7	LPDP_INT_SL_DATA_C_P<0>		NC_LPDPTX1_DATAP0		MAKE_BASE=TRUE
7	LPDP_INT_SL_DATA_C_N<0>		NC_LPDPTX1_DATAN0		MAKE_BASE=TRUE
7	LPDP_INT_SL_DATA_C_P<1>		NC_LPDPTX1_DATAP1		MAKE_BASE=TRUE
7	LPDP_INT_SL_DATA_C_N<1>		NC_LPDPTX1_DATAN1		MAKE_BASE=TRUE
7	LPDP_INT_SL_DATA_C_P<2>		NC_LPDPTX1_DATAP2		MAKE_BASE=TRUE
7	LPDP_INT_SL_DATA_C_N<2>		NC_LPDPTX1_DATAN2		MAKE_BASE=TRUE
7	LPDP_INT_SL_DATA_C_P<3>		NC_LPDPTX1_DATAP3		MAKE_BASE=TRUE
7	LPDP_INT_SL_DATA_C_N<3>		NC_LPDPTX1_DATAN3		MAKE_BASE=TRUE
7	LPDP_INT_SL_AUX_C_P		NC_LPDPTX1_AUXP		MAKE_BASE=TRUE
7	LPDP_INT_SL_AUX_C_N		NC_LPDPTX1_AUXN		MAKE_BASE=TRUE
7	LPDP_INT_SL_HPD		NC_LPDP_INT_SL_HPD		MAKE_BASE=TRUE

LPDPRX

7	LPDP_FTCAM_DATA_P<1>		NC_LPDPRX_DATAP1	MAKE_BASE=TRUE
7	LPDP_FTCAM_DATA_N<1>		NC_LPDPRX_DATAN1	MAKE_BASE=TRUE

NAND

8	TP_PCIE_CLK100M_NAND0_1P		NC_PCIE_CLK100M_NAND0_1P	MAKE_BASE=TRUE
8	TP_PCIE_CLK100M_NAND0_1N		NC_PCIE_CLK100M_NAND0_1N	MAKE_BASE=TRUE
8	TP_PCIE_CLK100M_NAND0_3P		NC_PCIE_CLK100M_NAND0_3P	MAKE_BASE=TRUE
8	TP_PCIE_CLK100M_NAND0_3N		NC_PCIE_CLK100M_NAND0_3N	MAKE_BASE=TRUE
8	TP_PCIE_CLK100M_NAND1_1P		NC_PCIE_CLK100M_NAND1_1P	MAKE_BASE=TRUE
8	TP_PCIE_CLK100M_NAND1_1N		NC_PCIE_CLK100M_NAND1_1N	MAKE_BASE=TRUE
8	TP_PCIE_CLK100M_NAND1_3P		NC_PCIE_CLK100M_NAND1_3P	MAKE_BASE=TRUE
8	TP_PCIE_CLK100M_NAND1_3N		NC_PCIE_CLK100M_NAND1_3N	MAKE_BASE=TRUE
97	SWD_NAND0_S5E0_SWCLK		SWD_NAND0_S5E0_S5E1_SWCLK	MAKE_BASE=TRUE
98	SWD_NAND0_S5E1_SWCLK			
99	SWD_NAND0_S5E2_SWCLK		SWD_NAND0_S5E2_S5E3_SWCLK	MAKE_BASE=TRUE
100	SWD_NAND0_S5E3_SWCLK			
97	SWD_NAND0_S5E0_SWDIO		SWD_NAND0_S5E0_S5E1_SWDIO	MAKE_BASE=TRUE
98	SWD_NAND0_S5E1_SWDIO			
99	SWD_NAND0_S5E2_SWDIO		SWD_NAND0_S5E2_S5E3_SWDIO	MAKE_BASE=TRUE
100	SWD_NAND0_S5E3_SWDIO			
102	SWD_NAND1_S5E0_SWCLK		SWD_NAND1_S5E0_S5E1_SWCLK	MAKE_BASE=TRUE
103	SWD_NAND1_S5E1_SWCLK			
104	SWD_NAND1_S5E2_SWCLK		SWD_NAND1_S5E2_S5E3_SWCLK	MAKE_BASE=TRUE
105	SWD_NAND1_S5E3_SWCLK			
102	SWD_NAND1_S5E0_SWDIO		SWD_NAND1_S5E0_S5E1_SWDIO	MAKE_BASE=TRUE
103	SWD_NAND1_S5E1_SWDIO			
104	SWD_NAND1_S5E2_SWDIO		SWD_NAND1_S5E2_S5E3_SWDIO	MAKE_BASE=TRUE
105	SWD_NAND1_S5E3_SWDIO			

MIPI

7	TP_MIPID_DATAP		NC_MIPID_DATAP	MAKE_BASE=TRUE
7	TP_MIPID_DATAN		NC_MIPID_DATAN	MAKE_BASE=TRUE
7	TP_MIPID_CLKP		NC_MIPID_CLKP	MAKE_BASE=TRUE
7	TP_MIPID_CLKN		NC_MIPID_CLKN	MAKE_BASE=TRUE
7	MIPI_FTCAM_DATA_P<0>		NC_MIPI_FTCAM_DATAP0	MAKE_BASE=TRUE
7	MIPI_FTCAM_DATA_N<0>		NC_MIPI_FTCAM_DATAN0	MAKE_BASE=TRUE
7	MIPI_FTCAM_DATA_P<1>		NC_MIPI_FTCAM_DATAP1	MAKE_BASE=TRUE
7	MIPI_FTCAM_DATA_N<1>		NC_MIPI_FTCAM_DATAN1	MAKE_BASE=TRUE
7	MIPI_FTCAM_CLK_P		NC_MIPI_FTCAM_CLKP	MAKE_BASE=TRUE
7	MIPI_FTCAM_CLK_N		NC_MIPI_FTCAM_CLKN	MAKE_BASE=TRUE
7	MIPI_IRCAM_DATA_P<0>		NC_MIPI_IRCAM_DATAP0	MAKE_BASE=TRUE
7	MIPI_IRCAM_DATA_N<0>		NC_MIPI_IRCAM_DATAN0	MAKE_BASE=TRUE
7	MIPI_IRCAM_DATA_P<1>		NC_MIPI_IRCAM_DATAP1	MAKE_BASE=TRUE
7	MIPI_IRCAM_DATA_N<1>		NC_MIPI_IRCAM_DATAN1	MAKE_BASE=TRUE
7	MIPI_IRCAM_CLK_P		NC_MIPI_IRCAM_CLKP	MAKE_BASE=TRUE
7	MIPI_IRCAM_CLK_N		NC_MIPI_IRCAM_CLKN	MAKE_BASE=TRUE

USB3

9	USB3_EXTA_R2D_C_P		NC_USB3_EXTA_R2DP	MAKE_BASE=TRUE
9	USB3_EXTA_R2D_C_N		NC_USB3_EXTA_R2DN	MAKE_BASE=TRUE
9	USB3_EXTA_D2R_P		NC_USB3_EXTA_D2RP	MAKE_BASE=TRUE
9	USB3_EXTA_D2R_N		NC_USB3_EXTA_D2RN	MAKE_BASE=TRUE
9	EUSB_EXTA_P		NC_EUSB_EXTAP	MAKE_BASE=TRUE
9	EUSB_EXTA_N		NC_EUSB_EXTAN	MAKE_BASE=TRUE
9	USB3_EXTB_R2D_C_P		NC_USB3_EXTB_R2DP	MAKE_BASE=TRUE
9	USB3_EXTB_R2D_C_N		NC_USB3_EXTB_R2DN	MAKE_BASE=TRUE
9	USB3_EXTB_D2R_P		NC_USB3_EXTB_D2RP	MAKE_BASE=TRUE
9	USB3_EXTB_D2R_N		NC_USB3_EXTB_D2RN	MAKE_BASE=TRUE
9	EUSB_EXTB_P		NC_EUSB_EXTBP	MAKE_BASE=TRUE
9	EUSB_EXTB_N		NC_EUSB_EXTBN	MAKE_BASE=TRUE
142 10	PARROT_RESET_L		NC_PARROT_RESET_L	MAKE_BASE=TRUE
10	PARROT_INT_L		NC_PARROT_INT_L	MAKE_BASE=TRUE
6	USB_EXTA_OC_L		NC_USB_EXTA_OC_L	MAKE_BASE=TRUE
6	USB_EXTB_OC_L		SWD_UPC_SWDIO3_R	MAKE_BASE=TRUE

ATC3 - HDMI

9	USBC_ATC3_R2D_C_P<1>		DP_DP2HDMI_DATA_P<2>	
89	DPRX_INT_DATA_C_P<2>		MAKE_BASE=TRUE	
9	USBC_ATC3_R2D_C_N<1>		DP_DP2HDMI_DATA_N<2>	
89	DPRX_INT_DATA_C_N<2>		MAKE_BASE=TRUE	
9	USBC_ATC3_D2R_P<1>		DP_DP2HDMI_DATA_P<3>	
89	DPRX_INT_DATA_C_P<3>		MAKE_BASE=TRUE	
9	USBC_ATC3_D2R_N<1>		DP_DP2HDMI_DATA_N<3>	
89	DPRX_INT_DATA_C_N<3>		MAKE_BASE=TRUE	
9	USBC_ATC3_R2D_C_P<2>		DP_DP2HDMI_DATA_P<1>	
89	DPRX_INT_DATA_C_P<1>		MAKE_BASE=TRUE	
9	USBC_ATC3_R2D_C_N<2>		DP_DP2HDMI_DATA_N<1>	
89	DPRX_INT_DATA_C_N<1>		MAKE_BASE=TRUE	
9	USBC_ATC3_D2R_P<2>		DP_DP2HDMI_DATA_P<0>	
89	DPRX_INT_DATA_C_P<0>		MAKE_BASE=TRUE	
9	USBC_ATC3_D2R_N<2>		DP_DP2HDMI_DATA_N<0>	
89	DPRX_INT_DATA_C_N<0>		MAKE_BASE=TRUE	
9	USBC_ATC3_AUX_P		DP_DP2HDMI_AUX_P	
89	DPRX_INT_AUX_C_P		MAKE_BASE=TRUE	
9	USBC_ATC3_AUX_N		DP_DP2HDMI_AUX_N	
89	DPRX_INT_AUX_C_N		MAKE_BASE=TRUE	

USBC

9	TP_USB_C0_HPD		NC_USB_C0_HPD	MAKE_BASE=TRUE
9	TP_USB_C1_HPD		NC_USB_C1_HPD	MAKE_BASE=TRUE
9	TP_USB_C2_HPD		NC_USB_C2_HPD	MAKE_BASE=TRUE

ENET

8	PCIE_ENET_R2D_C_P		NC_PCIE_ENET_R2DP	MAKE_BASE=TRUE
8	PCIE_ENET_R2D_C_N		NC_PCIE_ENET_R2DN	MAKE_BASE=TRUE
8	PCIE_ENET_D2R_P		NC_PCIE_ENET_D2RP	MAKE_BASE=TRUE
8	PCIE_ENET_D2R_N		NC_PCIE_ENET_D2RN	MAKE_BASE=TRUE
8	PCIE_CLK100M_ENET_P		NC_PCIE_CLK100M_SDP	MAKE_BASE=TRUE
8	PCIE_CLK100M_ENET_N		NC_PCIE_CLK100M_SDN	MAKE_BASE=TRUE
6	ENET_SELECT_1G_H_10G_L		NC_ENET_SELECT_1G_H_10G_L	MAKE_BASE=TRUE

SD

8	PCIE_SD_R2D_C_P		PCIE_SD_UHS2_R2D_C_P	91 MAKE_BASE=TRUE
8	PCIE_SD_R2D_C_N		PCIE_SD_UHS2_R2D_C_N	91 MAKE_BASE=TRUE
8	PCIE_SD_D2R_P		PCIE_SD_UHS2_D2R_P	91 MAKE_BASE=TRUE
8	PCIE_SD_D2R_N		PCIE_SD_UHS2_D2R_N	91 MAKE_BASE=TRUE
8	PCIE_CLK100M_SD_P		PCIE_CLK100M_SD_UHS2_P	91 MAKE_BASE=TRUE
8	PCIE_CLK100M_SD_N		PCIE_CLK100M_SD_UHS2_N	91 MAKE_BASE=TRUE
8	SD_RESET_L		SD_UHS2_RESET_L	93 MAKE_BASE=TRUE
8	SD_CLKREQ_L		SD_UHS2_CLKREQ_L	93 MAKE_BASE=TRUE
8	PCIE_SDEXP_R2D_C_P		NC_PCIE_SD_EXP_R2D_C_P	MAKE_BASE=TRUE
8	PCIE_SDEXP_R2D_C_N		NC_PCIE_SD_EXP_R2D_C_N	MAKE_BASE=TRUE
8	PCIE_SDEXP_D2R_P		NC_PCIE_SD_EXP_D2R_P	MAKE_BASE=TRUE
8	PCIE_SDEXP_D2R_N		NC_PCIE_SD_EXP_D2R_N	MAKE_BASE=TRUE
8	PCIE_CLK100M_SDEXP_P		NC_PCIE_CLK100M_SD_EXP_P	MAKE_BASE=TRUE
8	PCIE_CLK100M_SDEXP_N		NC_PCIE_CLK100M_SD_EXP_N	MAKE_BASE=TRUE
8	SDEXP_RESET_L		SD_EXP_RESET_L	MAKE_BASE=TRUE
8	SDEXP_CLKREQ_L		SD_EXP_CLKREQ_L	MAKE_BASE=TRUE
6	SDEXP_SEL		NC_SDEXP_SEL	MAKE_BASE=TRUE

				MAKE_BASE=TRUE
9	EUSB_ATC3_P		NC_EUSB_ATC3P	
9	EUSB_ATC3_N		NC_EUSB_ATC3N	

SYNC_MASTER=GAREN SYNC_DATE=06/23/2020

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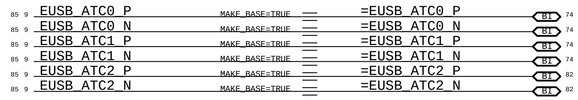
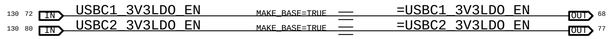
Internal signal aliases - Must be configured on project pages per notes below.

SOC, series caps | BBR A side | BBR B side | Connector

Caps and connector must be aliased to BBR signals.
BBR lanes 1 and 2 can be swapped, both pairs, both sides - all or nothing.
BBR inputs can be polarity inverted independently per pair.
All swaps and inversions must be communicated to TBT Firmware team.

Internal signal aliases - Copied or debug circuitry added between.





SYNC_DATE=10/29/2019

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REF_SECDIS_SAK

108 SEC_FCAM_RESET_L —— FTCAM_ENABLE_1V8_OUT (MAKE_BASE=TRUE) 114 129

6 DISABLE_STROBE —— NC_DISABLE_STROBE (MAKE_BASE=TRUE)

6 FTCAM_DISABLE_L —— NC_FTCAM_DISABLE_L (MAKE_BASE=TRUE)

6 DMIC_DISABLE_L —— NC_DMIC_DISABLE_L (MAKE_BASE=TRUE)

CHARGER

10 CHGR_INT_L_PSU_TBD4 —— CHGR_INT_L (MAKE_BASE=TRUE) 29 129

HDMI

9 DP_DP2HDMI_HPD (MAKE_BASE=TRUE) —— DPRX_INT_HPD (MAKE_BASE=TRUE) 89

6 UART_DP2HDMI_R2D —— NC_UART_DP2HDMI_R2D (MAKE_BASE=TRUE)

LPDPTX

140 139 LPDP_INT_HPD (MAKE_BASE=TRUE) —— LPDP_INT_ML_HPD 7 140

MACAW

140 10 PARROT_RESET_L —— SOC_RECOVERY_STATUS (MAKE_BASE=TRUE)

IPD

10 IPD_SPI_INT_L_ENET_LOW_PWR —— IPD_SPI_INT_L (MAKE_BASE=TRUE) 123

SMC_I2C5

10 IN I2C_SMC_SNS1_SCL —— NC_I2C_SMC_SNS1_SCL (MAKE_BASE=TRUE)

10 BI I2C_SMC_SNS1_SDA —— NC_I2C_SMC_SNS1_SDA (MAKE_BASE=TRUE)

AP_I2C4

93 IN AP_I2C04_SCL —— TP_AP_I2C04_SCL (MAKE_BASE=TRUE) 6

93 BI AP_I2C04_SDA —— TP_AP_I2C04_SDA (MAKE_BASE=TRUE) 6

AP_I2C5

6 IN I2C_ENET_SCL —— NC_I2C_ENET_SCL (MAKE_BASE=TRUE)

6 BI I2C_ENET_SDA —— NC_I2C_ENET_SDA (MAKE_BASE=TRUE)

AP_I2C6

6 IN I2C_USBA_LS_SCL —— NC_I2C_USBA_LS_SCL (MAKE_BASE=TRUE)

6 BI I2C_USBA_LS_SDA —— NC_I2C_USBA_LS_SDA (MAKE_BASE=TRUE)

NC SPN'S

28 TP_CHGR_EN_VR1 —— NC_CHGR_EN_VR1 (MAKE_BASE=TRUE)

67 TP_SMBUS_ATCRTMR0_SCL —— NC_SMBUS_ATCRTMR0_SCL (MAKE_BASE=TRUE)

67 TP_SMBUS_ATCRTMR0_SDA —— NC_SMBUS_ATCRTMR0_SDA (MAKE_BASE=TRUE)

68 TP_SMBUS_ATCRTMR1_SCL —— NC_SMBUS_ATCRTMR1_SCL (MAKE_BASE=TRUE)

68 TP_SMBUS_ATCRTMR1_SDA —— NC_SMBUS_ATCRTMR1_SDA (MAKE_BASE=TRUE)

77 TP_SMBUS_ATCRTMR2_SCL —— NC_SMBUS_ATCRTMR2_SCL (MAKE_BASE=TRUE)

77 TP_SMBUS_ATCRTMR2_SDA —— NC_SMBUS_ATCRTMR2_SDA (MAKE_BASE=TRUE)

28 TP_CHGR_SMC_RST_L —— NC_CHGR_SMC_RST_L (MAKE_BASE=TRUE)

28 TP_CHGR_CBC_ON —— NC_CHGR_CBC_ON (MAKE_BASE=TRUE)

43 TP_MPMU_AMUX_AY —— NC_MPMU_AMUX_AY (MAKE_BASE=TRUE)

39 TP_SPMU_AMUX_BY —— NC_SPMU_AMUX_BY (MAKE_BASE=TRUE)

39 TP_SPMU_PRE_UVLO —— NC_SPMU_PRE_UVLO (MAKE_BASE=TRUE)

43 TP_MPMU_AMUX_BY —— NC_MPMU_AMUX_BY (MAKE_BASE=TRUE)

39 TP_SPMU_AMUX_AY —— NC_SPMU_AMUX_AY (MAKE_BASE=TRUE)

43 TP_MPMU_LDOX_EN —— NC_MPMU_LDOX_EN (MAKE_BASE=TRUE)

88 TP_HDMI_I2C_SCL —— NC_HDMI_I2C_SCL (MAKE_BASE=TRUE)

88 TP_HDMI_I2C_SDA —— NC_HDMI_I2C_SDA (MAKE_BASE=TRUE)

101 TP_NAND0_OCARINA_WP_L —— NC_NAND0_OCARINA_WP_L (MAKE_BASE=TRUE)

26 TP_SE_GPIO0 —— NC_SE_GPIO0 (MAKE_BASE=TRUE)

106 TP_NAND1_OCARINA_WP_L —— NC_NAND1_OCARINA_WP_L (MAKE_BASE=TRUE)

82 9 CIO_ATC3_LSRX_1V2 —— NC_CIO_ATC3_LSRX_1V2 (MAKE_BASE=TRUE)

82 9 CIO_ATC3_LSTX_1V2 —— NC_CIO_ATC3_LSTX_1V2 (MAKE_BASE=TRUE)

6 TP_AP_GPIO1 —— NC_AP_GPIO1 (MAKE_BASE=TRUE)

6 TP_AP_GPIO8 —— NC_AP_GPIO8 (MAKE_BASE=TRUE)

5 TP_CLVR_GPIO0 —— NC_CLVR_GPIO0 (MAKE_BASE=TRUE)

43 TP_MPMU_VDDHI_PRE_UPO —— NC_MPMU_VDDHI_PRE_UPO (MAKE_BASE=TRUE)

6 TP_AP_I2S2_MCK —— NC_AP_I2S2_MCK (MAKE_BASE=TRUE)

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ISP GPIO

		MAKE_BASE=TRUE	
7	IRCAM_RESET_L	NC_IRCAM_RESET_L	
7	CAM_PMU_RESET_L	NC_CAM_PMU_RESET_L	

AOP IO

10	IRCAM_PROX_INT_L	NC_IRCAM_PROX_INT_L	MAKE_BASE=TRUE
10	TP_AOP_GPIO1	NC_AOP_GPIO1	MAKE_BASE=TRUE
10	TP_AOP_GPIO5	NC_AOP_GPIO5	MAKE_BASE=TRUE
10	TP_AOP_I2CM1_SCL	NC_AOP_I2CM1_SCL	MAKE_BASE=TRUE
10	TP_AOP_I2CM1_SDA	NC_AOP_I2CM1_SDA	MAKE_BASE=TRUE
10	TP_PDM_DMIC_CLK1	NC_PDM_DMIC_CLK1	MAKE_BASE=TRUE
10	TP_AOP_I2S0_MCK	NC_AOP_I2S0_MCK	MAKE_BASE=TRUE
10	TP_AOP_I2S0_LRCK	NC_AOP_I2S0_LRCK	MAKE_BASE=TRUE
10	TP_AOP_I2S0_DOUT	NC_AOP_I2S0_DOUT	MAKE_BASE=TRUE
10	TP_AOP_I2S0_DIN	NC_AOP_I2S0_DIN	MAKE_BASE=TRUE
10	TP_AOP_I2S0_BCLK	NC_AOP_I2S0_BCLK	MAKE_BASE=TRUE
10	TP_PDM_DMIC_DATA1	NC_PDM_DMIC_DATA1	MAKE_BASE=TRUE
10	TP_AOP_UART2_R2D	NC_AOP_UART2_R2D	MAKE_BASE=TRUE
10	TP_AOP_UART2_D2R	NC_AOP_UART2_D2R	MAKE_BASE=TRUE
10	TP_AOP_GPIO0	SOC_DOMAIN_AGPIO_AOP0	MAKE_BASE=TRUE 143
10	TP_AOP_GPIO2	NC_AOP_GPIO2	MAKE_BASE=TRUE
10	TP_AOP_GPIO3	NC_AOP_GPIO3	MAKE_BASE=TRUE
10	TP_AOP_GPIO4	NC_AOP_GPIO4	MAKE_BASE=TRUE

CLVR GPIO

5	TP_CLVR_GPIO1	NC_CLVR_GPIO1	MAKE_BASE=TRUE
5	TP_CLVR_GPIO2	NC_CLVR_GPIO2	MAKE_BASE=TRUE
5	TP_CLVR_GPIO3	NC_CLVR_GPIO3	MAKE_BASE=TRUE
5	TP_CLVR_GPIO4	NC_CLVR_GPIO4	MAKE_BASE=TRUE
5	TP_CLVR_GPIO5	NC_CLVR_GPIO5	MAKE_BASE=TRUE
5	TP_CLVR_GPIO6	NC_CLVR_GPIO6	MAKE_BASE=TRUE
5	TP_CLVR_GPIO7	SOC_DOMAIN_GPIO_GRP1_0	MAKE_BASE=TRUE 143
5	TP_CLVR_GPIO8	NC_CLVR_GPIO8	MAKE_BASE=TRUE
5	TP_CLVR_GPIO9	NC_CLVR_GPIO9	MAKE_BASE=TRUE

SMC GPIO

		MAKE_BASE=TRUE	
10	TP_SMC_GPIO5	NC_BKLT_PWR_ON_SMC_LED_SEL	
10	ACDC_BURST_EN_L	NC_ACDC_BURST_EN_L	
10	ACDC_ID	NC_ACDC_ID	
10	PSU_TBD3	NC_PSU_TBD3	
10	TP_SMC_GPIO1	SOC_DOMAIN_MGPIO_AOP1	143
10	TP_SMC_GPIO2	NC_SMC_GPIO2	
10	TP_SMC_GPIO3	NC_SMC_GPIO3	
10	TP_SMC_GPIO4	NC_SMC_GPIO4	
10	TP_SMC_I2CM6_SCL	NC_SMC_I2CM6_SCL	
10	TP_SMC_I2CM6_SDA	NC_SMC_I2CM6_SDA	

NUB GPIO

		MAKE_BASE=TRUE	
10	TITUS_B2B_DETECT_L	SOC_DOMAIN_NGPIO_AOP1_2	143
10	TP_NUB_CLK_OUT0	SOC_DOMAIN_NGPIO_AOP1_0	143
10	TP_NUB_CLK_OUT1	SOC_DOMAIN_NGPIO_AOP1_1	143
10	TP_NUB_SWD_TMS3	NC_NUB_SWD_TMS3	
10	TP_NUB_JTAG_SLV_TCK	NC_NUB_JTAG_SLV_TCK	
10	TP_NUB_JTAG_SLV_TMS	NC_NUB_JTAG_SLV_TMS	
10	TP_NUB_JTAG_SLV_TDI	NC_NUB_JTAG_SLV_TDI	
10	TP_NUB_JTAG_SLV_TDO	NC_NUB_JTAG_SLV_TDO	
10	TP_NUB_JTAG_SLV_TRSTN	NC_NUB_JTAG_SLV_TRSTN	

SEP

		MAKE_BASE=TRUE	
6	IRCAM_DISABLE_L	SOC_DOMAIN_SGPIO_GRP1	143

ENET GPIO

		MAKE_BASE=TRUE	
6	ENET_SYNC_1588	NC_ENET_SYNC_1588	

D2D IO

5	TP_A2A_SYNC_ACK	NC_A2A_SYNC_ACK	MAKE_BASE=TRUE
5	TP_A2A_SYNC_REQ	NC_A2A_SYNC_REQ	MAKE_BASE=TRUE
5	TP_A2A_WAKEUP	NC_A2A_WAKEUP	MAKE_BASE=TRUE
5	TP_C2C_CLK_24_IN	NC_C2C_CLK_24_IN	MAKE_BASE=TRUE
5	TP_C2C_CLK_24_OUT	NC_C2C_CLK_24_OUT	MAKE_BASE=TRUE
5	TP_C2C_TIME_SYNC_IN	NC_C2C_TIME_SYNC_IN	MAKE_BASE=TRUE
5	TP_C2C_TIME_SYNC_OUT	NC_C2C_TIME_SYNC_OUT	MAKE_BASE=TRUE
5	TP_GTRIG_TX_REQ	NC_GTRIG_TX_REQ	MAKE_BASE=TRUE
5	TP_GTRIG_TX_ACK	NC_GTRIG_TX_ACK	MAKE_BASE=TRUE
5	TP_GTRIG_TX_LN0	NC_GTRIG_TX_LN0	MAKE_BASE=TRUE
5	TP_GTRIG_TX_LN1	NC_GTRIG_TX_LN1	MAKE_BASE=TRUE
5	TP_GTRIG_RX_REQ	NC_GTRIG_RX_REQ	MAKE_BASE=TRUE
5	TP_GTRIG_RX_ACK	NC_GTRIG_RX_ACK	MAKE_BASE=TRUE
5	TP_GTRIG_RX_LN0	NC_GTRIG_RX_LN0	MAKE_BASE=TRUE
5	TP_GTRIG_RX_LN1	NC_GTRIG_RX_LN1	MAKE_BASE=TRUE

NAND

8	TP_SSD_RESET0_L	SOC_DOMAIN_HGPIO_GRP0_0	MAKE_BASE=TRUE
8	TP_SSD_RESET1_7_L	SOC_DOMAIN_HGPIO_GRP0_1	MAKE_BASE=TRUE

CLVR SPMI

5	SPMI_CLVR3_CLK_R	NC_SPMI_CLVR3_CLK_R	MAKE_BASE=TRUE
5	SPMI_CLVR3_DATA_R	NC_SPMI_CLVR3_DATA_R	MAKE_BASE=TRUE
5	SPMI_CLVR4_CLK_R	NC_SPMI_CLVR4_CLK_R	MAKE_BASE=TRUE
5	SPMI_CLVR4_DATA_R	NC_SPMI_CLVR4_DATA_R	MAKE_BASE=TRUE

ISP SPMI

7	SPMI_ISP_CAM_CLK_R	NC_SPMI_ISP_CAM_CLK_R	MAKE_BASE=TRUE
7	SPMI_ISP_CAM_DATA_R	NC_SPMI_ISP_CAM_DATA_R	MAKE_BASE=TRUE
7	TP_ISP_I2C0_SCL	NC_ISP_I2C0_SCL	MAKE_BASE=TRUE
7	TP_ISP_I2C0_SDA	NC_ISP_I2C0_SDA	MAKE_BASE=TRUE
7	TP_ISP_I2C1_SCL	NC_ISP_I2C1_SCL	MAKE_BASE=TRUE
7	TP_ISP_I2C1_SDA	NC_ISP_I2C1_SDA	MAKE_BASE=TRUE
7	TP_ISP_I2C3_SCL	NC_ISP_I2C3_SCL	MAKE_BASE=TRUE
7	TP_ISP_I2C3_SDA	NC_ISP_I2C3_SDA	MAKE_BASE=TRUE
7	TP_ISP_GPIO3	SOC_DOMAIN_GPIO_GRP1_2	MAKE_BASE=TRUE
7	TP_SPMI1_ISP_CLK	NC_SPMI1_ISP_CLK	MAKE_BASE=TRUE
7	TP_SPMI1_ISP_DATA	NC_SPMI1_ISP_DATA	MAKE_BASE=TRUE

VIPER PWM

47	P1V8VDDH_DRMOS_PWM4	NC_P1V8VDDH_DRMOS_PWM4	MAKE_BASE=TRUE
47	P1V8VDDH_DRMOS_PWM5	NC_P1V8VDDH_DRMOS_PWM5	MAKE_BASE=TRUE
47	P1V8VDDH_DRMOS_PWM6	NC_P1V8VDDH_DRMOS_PWM6	MAKE_BASE=TRUE
47	P1V8VDDH_DRMOS_PWM7	NC_P1V8VDDH_DRMOS_PWM7	MAKE_BASE=TRUE
47	P1V8VDDH_DRMOS_PWM8	NC_P1V8VDDH_DRMOS_PWM8	MAKE_BASE=TRUE

NC SPN's

5	TP_PAD_MTR_ANALOG_TESTP	NC_PAD_MTR_ANALOG_TESTP	MAKE_BASE=TRUE
5	TP_PAD_MTR_ANALOG_TESTN	NC_PAD_MTR_ANALOG_TESTN	MAKE_BASE=TRUE
5	TP_PAD_MTR_VREFP	NC_PAD_MTR_VREFP	MAKE_BASE=TRUE
5	TP_PAD_MTR_VREFN	NC_PAD_MTR_VREFN	MAKE_BASE=TRUE

6	TDM_SPKRAMP_ALT_BCLK_R	NC_TDM_SPKRAMP_ALT_BCLK_R	MAKE_BASE=TRUE
6	TDM_SPKRAMP_ALT_D2R	NC_TDM_SPKRAMP_ALT_D2R	MAKE_BASE=TRUE
6	TDM_SPKRAMP_ALT_FSYNC_R	NC_TDM_SPKRAMP_ALT_FSYNC_R	MAKE_BASE=TRUE
6	TDM_SPKRAMP_ALT_R2D_R	NC_TDM_SPKRAMP_ALT_R2D_R	MAKE_BASE=TRUE
6	TP_AP_I2S3_MCK	NC_AP_I2S3_MCK	MAKE_BASE=TRUE
6	TP_AP_I2S0_MCK	NC_AP_I2S0_MCK	MAKE_BASE=TRUE
6	TP_AP_I2S1_MCK	NC_AP_I2S1_MCK	MAKE_BASE=TRUE
6	TP_AP_GPIO23	NC_AP_GPIO23	MAKE_BASE=TRUE
6	TP_AP_GPIO24	NC_AP_GPIO24	MAKE_BASE=TRUE
6	TP_AP_GPIO27	SD_CONTROLLER_GPIO	MAKE_BASE=TRUE
6	TP_AP_GPIO28	NC_AP_GPIO28	MAKE_BASE=TRUE
6	TP_AP_GPIO29	NC_AP_GPIO29	MAKE_BASE=TRUE
6	TP_AP_GPIO30	NC_AP_GPIO30	MAKE_BASE=TRUE
6	TP_AP_GPIO31	NC_AP_GPIO31	MAKE_BASE=TRUE
6	TP_AP_GPIO32	NC_AP_GPIO32	MAKE_BASE=TRUE
6	TP_SOC_MASTER_SYNC_GEN_2	SOC_FUSE_CFG0_L	14 143 MAKE_BASE=TRUE
6	TP_AP_GPIO34	SOC_FUSE_CFG1_L	14 143 MAKE_BASE=TRUE
10	WLAN_CONTEXT_A	NC_WLAN_CONTEXT_A	MAKE_BASE=TRUE
10	WLAN_CONTEXT_B	NC_WLAN_CONTEXT_B	MAKE_BASE=TRUE

NC SPN's

		MAKE_BASE=TRUE	
7	TP_DISP_TOUCH_BSYNC0	NC_DISP_TOUCH_BSYNC0	
7	TP_DISP_TOUCH_BSYNC1	NC_DISP_TOUCH_BSYNC1	
7	TP_DISP_TOUCH_EB	NC_DISP_TOUCH_EB	
7	TP_DFR_DISP_TE	NC_DFR_DISP_TE	

		MAKE_BASE=TRUE	
7	CAM_PMU_CLK24M_R	NC_CAM_PMU_CLK24M_R	
7	TP_SENSOR1_CLK	NC_SENSOR1_CLK	
7	TP_SENSOR2_CLK	NC_SENSOR2_CLK	
7	TP_SENSOR3_CLK	NC_SENSOR3_CLK	

		MAKE_BASE=TRUE	
26	=I2C_SE_SCL	NC_I2C_SE_SCL	
26	=I2C_SE_SDA	NC_I2C_SE_SDA	

6	TP_AP_UART2_R2D	NC_AP_UART2_R2D	MAKE_BASE=TRUE
6	TP_AP_UART2_D2R	NC_AP_UART2_D2R	MAKE_BASE=TRUE
6	TP_AP_UART2_R2D_RTS_L	NC_AP_UART2_R2D_RTS_L	MAKE_BASE=TRUE
6	TP_AP_UART2_D2R_CTS_L	NC_AP_UART2_D2R_CTS_L	MAKE_BASE=TRUE
6	TP_AP_UART3_R2D	NC_AP_UART3_R2D	MAKE_BASE=TRUE
6	TP_AP_UART3_D2R	NC_AP_UART3_D2R	MAKE_BASE=TRUE
6	TP_AP_UART3_R2D_RTS_L	NC_AP_UART3_R2D_RTS_L	MAKE_BASE=TRUE
6	TP_AP_UART3_D2R_CTS_L	NC_AP_UART3_D2R_CTS_L	MAKE_BASE=TRUE
6	TP_AP_UART4_D2R	NC_AP_UART4_D2R NO_TEST=1	MAKE_BASE=TRUE
6	TP_AP_UART4_R2D	NC_AP_UART4_R2D NO_TEST=1	MAKE_BASE=TRUE
6	TP_AP_UART4_R2D_RTS_L	NC_AP_UART4_R2D_RTS_L	MAKE_BASE=TRUE
6	TP_AP_UART4_D2R_CTS_L	NC_AP_UART4_D2R_CTS_L	MAKE_BASE=TRUE
6	TP_AP_UART6_TXD	NC_AP_UART6_TXD	MAKE_BASE=TRUE
6	TP_AP_SPI2_SSIN	NC_AP_SPI2_SSIN	MAKE_BASE=TRUE
6	TP_AP_SPMI2_DATA	NC_AP_SPMI2_DATA	MAKE_BASE=TRUE
6	TP_AP_SPMI2_CLK	NC_AP_SPMI2_CLK	MAKE_BASE=TRUE
7	TP_LPDP_FTCAM_AUX	NC_LPDP_FTCAM_AUX	MAKE_BASE=TRUE
7	TP_DISP_POL	NC_DISP_POL	MAKE_BASE=TRUE

NUB_SWD

10	TP_NUB_SWD_TCK_OUT2	NC_NUB_SWD_TCK_OUT2	MAKE_BASE=TRUE
10	TP_NUB_SWD_TMS2	NC_NUB_SWD_TMS2	MAKE_BASE=TRUE

SOC GPIO TPs BY DOMAIN

Nonused SOC pins pulled out by functional/power domains

143 14	SOC_FUSE_CFG0_L	P2MM SM 1 PP	PPZZ01	143	SOC_DOMAIN_NGPIO_AOP1_0	P2MM SM 1 PP	PPZZ02
	PLACE_SIDE=TOP				PLACE_SIDE=TOP		
143	SOC_DOMAIN_GPIO_GRP1_0	P2MM SM 1 PP	PPZZ03	143	SOC_DOMAIN_NGPIO_AOP1_1	P2MM SM 1 PP	PPZZ04
	PLACE_SIDE=TOP				PLACE_SIDE=TOP		
143 14	SOC_FUSE_CFG1_L	P2MM SM 1 PP	PPZZ05	143	SOC_DOMAIN_NGPIO_AOP1_2	P2MM SM 1 PP	PPZZ06
	PLACE_SIDE=TOP				PLACE_SIDE=TOP		
143	SOC_DOMAIN_GPIO_GRP1_2	P2MM SM 1 PP	PPZZ07	143	SOC_DOMAIN_HGPIO_GRP0_0	P2MM SM 1 PP	PPZZ08
	PLACE_SIDE=TOP				PLACE_SIDE=TOP		
143	SOC_DOMAIN_AGPIO_AOP0	P2MM SM 1 PP	PPZZ09	143	SOC_DOMAIN_HGPIO_GRP0_1	P2MM SM 1 PP	PPZZ10
	PLACE_SIDE=TOP				PLACE_SIDE=TOP		
143	SOC_DOMAIN_MGPIO_AOP1	P2MM SM 1 PP	PPZZ11	143	SOC_DOMAIN_SGPIO_GRP1	P2MM SM 1 PP	PPZZ12
	PLACE_SIDE=TOP				PLACE_SIDE=TOP		

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USBC ATC3 NC

82 CIO_ATC3_LSRX_3V3 = NC_CIO_ATC3_LSRX_3V3 MAKE_BASE=TRUE
82 CIO_ATC3_LSTX_3V3 = NC_CIO_ATC3_LSTX_3V3 MAKE_BASE=TRUE
82 ATCRTMR3_RESET_L = NC_ATCRTMR3_RESET_L MAKE_BASE=TRUE
78 INT_I2C_UPC3_ATCRTMR3_L = NC_INT_I2C_UPC3_ATCRTMR3_L MAKE_BASE=TRUE
78 SPI_ATCRTMR3_R_MISO = NC_SPI_ATCRTMR3_R_MISO MAKE_BASE=TRUE
78 SPI_ATCRTMR3_R_CLK = NC_SPI_ATCRTMR3_R_CLK MAKE_BASE=TRUE
78 SPI_ATCRTMR3_R_CS_L = NC_SPI_ATCRTMR3_R_CS_L MAKE_BASE=TRUE
78 SPI_ATCRTMR3_R_MOSI = NC_SPI_ATCRTMR3_R_MOSI MAKE_BASE=TRUE
82 ATCRTMR3_RESET_1V8_L = NC_ATCRTMR3_RESET_1V8_L MAKE_BASE=TRUE
82 INT_I2C_EUSBLS3_1V8_L = NC_INT_I2C_EUSBLS3_1V8_L MAKE_BASE=TRUE
82 =PP3V3_S2_USBLS3 = NC_PP3V3_S2_USBLS3 MAKE_BASE=TRUE
78 INT_I2C_ATCRTMR3_L = NC_INT_I2C_ATCRTMR3_L MAKE_BASE=TRUE
78 =PP3V3_ATCRTMR3_SX = NC_PP3V3_ATCRTMR3_SX MAKE_BASE=TRUE

VITAMIN C

134 DEBUG_JTAG_SOC_TDO
128 10 TP_JTAG_SOC_TDO
= SOC_JTAG_TDO MAKE_BASE=TRUE

134 DEBUG_JTAG_SOC_TDI
128 10 TP_JTAG_SOC_TDI
= SOC_JTAG_TDI MAKE_BASE=TRUE

134 TP_DC_MUX_SEL = NC_DC_MUX_SEL MAKE_BASE=TRUE
NO_TEST=1
134 74 =ATCRTMR0_RESET_1V8_L = ATCRTMR0_RESET_MUX_1V8_L MAKE_BASE=TRUE

67 =USBC0_3V3LDO_EN
134 =USB0_3V3_LDO_EN_VITC
= USB0_3V3_LDO_EN_VITC 129 MAKE_BASE=TRUE

I2C CKPLUS WAIVER

56 B1 I2C_SMC_PWR_R_SDA
CKPLUS_WAIVE=I2C_PULLUP

56 B1 I2C_SMC_PWR_R_SCL
CKPLUS_WAIVE=I2C_PULLUP

129 124 121 B1 I2C_KBD_SCL
CKPLUS_WAIVE=I2C_PULLUP

129 124 121 B1 I2C_KBD_SDA
CKPLUS_WAIVE=I2C_PULLUP

134 =USB_DBG_VITC_UPC_P = USB_DBG_LS_P 70 129
MAKE_BASE=TRUE
134 =USB_DBG_VITC_UPC_N = USB_DBG_LS_N 70 129
MAKE_BASE=TRUE

134 =USB_DBG_VITC_LS_P
74 =USB_DBG_LS_P
= USB_DBG_LS_MUX_P
MAKE_BASE=TRUE

134 =USB_DBG_VITC_LS_N
74 =USB_DBG_LS_N
= USB_DBG_LS_MUX_N
MAKE_BASE=TRUE

74 =USB2_ATC0_LS_P
134 =USB2_ATC0_VITC_LS_P
= USB2_ATC0_LS_MUX_P
MAKE_BASE=TRUE

74 =USB2_ATC0_LS_N
134 =USB2_ATC0_VITC_LS_N
= USB2_ATC0_LS_MUX_N
MAKE_BASE=TRUE

85 USB2_UPC0_P1_R_P
134 =USB2_ATC0_VITC_UPC_P
= USB2_ATC0_LS_P 129
MAKE_BASE=TRUE

85 USB2_UPC0_P1_R_N
134 =USB2_ATC0_VITC_UPC_N
= USB2_ATC0_LS_N 129
MAKE_BASE=TRUE

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from stackup, shortest distance is used unless 'L'is defined	EXAMPLE: 1,3-5,7L,8L-10L 2-10
A_DIELECTRIC_(N)XD XV,XVL,X Calculates dielectric distance from Hybrid Table and stackup, shortest distance is used unless 'L' defined	EXAMPLE: 2,1DL,3D-5D,7V,8VL-10VL PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from stackup, shortest distance is used unless 'L' is defined	EXAMPLE: 2_4,3L_5L

PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR DOWNSTREAM
CLASS NAME	NONE A-A	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
SPI	P	A_45_OHM_SE	*SPI*MISO*,*SPI*MOSI*,*SPI*CLK*,*SPI*CS*	Y
SPMI	P	A_45_OHM_SE	*SPMI*	Y
SWD	P	A_45_OHM_SE	SWD_NAND*,SWD_NUB*	Y
JTAG	P	A_45_OHM_SE	*JTAG*SEL,*JTAG*TCK,*JTAG*TDI,*JTAG*TDO,*JTAG*TMS	Y
CLOCK_24M	P	A_45_OHM_SE	SOC_24M_O_R,NAND0_CLK24M*	Y
SOC_XTAL_24M_IN	P	A_45_OHM_SE	SOC_XTAL24M_IN	Y
SOC_XTAL_24M_OUT	P	A_45_OHM_SE	SOC_XTAL24M_OUT	Y
CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
TDM_LEFT	P	A_45_OHM_SE	TDM_SPKRAMP_L*.TDM_SPKRAMP_A*,TDM_SPKRAMP_B*	Y
TDM_RIGHT	P	A_45_OHM_SE	TDM_SPKRAMP_R*,TDM_SPKRAMP_D*,TDM_SPKRAMP_E*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
SPKR_ICC	P	A_45_OHM_SE	SPKRAMP_ICC,SPKRAMP_*_ICC_R	Y
UART	P	A_45_OHM_SE	UART_*	Y
RESETS	P	A_45_OHM_SE	*RST*,*RESET*,*PERST*	Y
WDOG	P	A_45_OHM_SE	SOC_WDOG	Y
SOCHOT	P	A_45_OHM_SE	SOC_SOCHOT_L	Y
POWER_BUTTON	P	A_45_OHM_SE	*PMU_ONOFF*	Y
FAULT	P	A_45_OHM_SE	*FAULT*	Y
DMIC_PDM	P	A_45_OHM_SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
FAN_CTRL	P	A_45_OHM_SE	SMC_FAN_*	Y
USBC_SOC_BSB0_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_D2R_C_1	Y
USBC_SOC_BSB0_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_D2R_C_2	Y
USBC_SOC_BSB0_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_R2D_1	Y
USBC_SOC_BSB0_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_R2D_2	Y
USBC_SOC_BSB0_AUX	P	A_85_OHM_DIFF	DP:DP_USBC_ATC0_AUX	Y
USBC_SOC_BSB0_LSX	P	A_45_OHM_SE	CIO_ATC0_LS*	Y
USBC_BSB0_CONN_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC0_D2R_CR_1	Y
USBC_BSB0_CONN_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC0_D2R_CR_2	Y
USBC_BSB0_CONN_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC0_R2D_C_1	Y
USBC_BSB0_CONN_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC0_R2D_C_2	Y
USBC_BSB0_CONN_AUXLSX	P	A_85_OHM_DIFF	DP:DP_USBC0_AUXLSX	Y
USBC_UPC0_CONN_TOP	P	A_85_OHM_DIFF	DP:DP_USBC0_USB_TOP	Y
USBC_UPC0_CONN_BOT	P	A_85_OHM_DIFF	DP:DP_USBC0_USB_BOT	Y
USBC_UPC0_CONN_CC	P	WIDTH_0P400	USBC0_CC*	Y
USBC_UPC0_CONN_SBU	P	A_45_OHM_SE	USBC0_SBU*	Y
USBC_SOC_RTMR0_USB2	P	A_85_OHM_DIFF	DP:DP_EUSB_ATC0	Y
USBC_RTMR0_MUX_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC0_LS_MUX	Y
USBC_MUX_UPC0_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC0_LS	Y
USBC_MUX_VITC_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC0_LS_VITAMINC	Y
USBC_SOC_BSB1_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_D2R_C_1	Y
USBC_SOC_BSB1_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_D2R_C_2	Y
USBC_SOC_BSB1_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_R2D_1	Y
USBC_SOC_BSB1_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_R2D_2	Y
USBC_SOC_BSB1_AUX	P	A_85_OHM_DIFF	DP:DP_USBC_ATC1_AUX	Y
USBC_SOC_BSB1_LSX	P	A_45_OHM_SE	CIO_ATC1_LS*	Y
USBC_BSB1_CONN_D2R_1	P	A_85_OHM_DIFF	DP:DP_USBC1_D2R_CR_1	Y
USBC_BSB1_CONN_D2R_2	P	A_85_OHM_DIFF	DP:DP_USBC1_D2R_CR_2	Y
USBC_BSB1_CONN_R2D_1	P	A_85_OHM_DIFF	DP:DP_USBC1_R2D_C_1	Y
USBC_BSB1_CONN_R2D_2	P	A_85_OHM_DIFF	DP:DP_USBC1_R2D_C_2	Y
USBC_BSB1_CONN_AUXLSX	P	A_85_OHM_DIFF	DP:DP_USBC1_AUXLSX	Y
USBC_UPC1_CONN_TOP	P	A_85_OHM_DIFF	DP:DP_USBC1_USB_TOP	Y
USBC_UPC1_CONN_BOT	P	A_85_OHM_DIFF	DP:DP_USBC1_USB_BOT	Y
USBC_UPC1_CONN_CC	P	WIDTH_0P400	USBC1_CC*	Y
USBC_UPC1_CONN_SBU	P	A_45_OHM_SE	USBC1_SBU*	Y
USBC_SOC_RTMR1_USB2	P	A_85_OHM_DIFF	DP:DP_EUSB_ATC1	Y
USBC_RTMR1_UPC1_USB2	P	A_85_OHM_DIFF	DP:DP_USB2_ATC1_LS	Y
USBC_SOC_RTMR_USB2_DBG	P	A_85_OHM_DIFF	DP:DP_EUSB_DBG	Y
USBC_RTMR_MUX_USB2_DBG	P	A_85_OHM_DIFF	DP:DP_USB_DBG_LS_MUX	Y
USBC_MUX_UPC_USB2_DBG	P	A_85_OHM_DIFF	DP:DP_USB_DBG_LS	Y
USBC_MUX_VITC_USB2_DBG	P	A_85_OHM_DIFF	DP:DP_USB_DBG_LS_VITAMINC	Y
USBC_LSX	P	A_45_OHM_SE	*ATC*LS*X	Y
MIPI_FTCAM_CLK	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_CLK,DP_MIPI_CLOCK_CONN	Y
MIPI_FTCAM_DATA	P	A_85_OHM_DIFF	DP:DP_MIPI_FTCAM_DATA_0,DP_MIPI_DATA_CONN	Y
MIPI_DFR_CLK	P	A_85_OHM_DIFF	DP:DP_MIPI_DFR_CLK_CONN_FILT	Y
MIPI_DFR_DATA	P	A_85_OHM_DIFF	DP:DP_MIPI_DFR_DATA_CONN_FILT	Y
PCIE_WIFI_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT_D2R_C	Y
PCIE_WIFI_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT_R2D_C	Y
PCIE_WIFI_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M_WLBT	Y
PCIE_NAND0_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND0_D2R_C_0	Y
PCIE_NAND0_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND0_R2D_C_0	Y
PCIE_NAND0_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M_NAND0_0	Y
PCIE_NAND1_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND0_D2R_C_1	Y
PCIE_NAND1_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND0_R2D_C_1	Y
PCIE_NAND1_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M_NAND0_1	Y
PCIE_CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
PANEL_LPDP_DATA	P	A_85_OHM_DIFF	DP:DP_DP0,DP_DP1,DP_DP2,DP_DP3	Y
PANEL_LPDP_AUX	P	A_85_OHM_DIFF	DP:DP_AUX	Y
RCAL_PCIE	P	WIDTH_0P100	SOC_ST_PCIE_RCAL*,SOC_GP_PCIE_RCAL*	Y
RCAL_CIO	P	WIDTH_0P100	SOC_ATCPHY0_RCAL*,SOC_ATCPHY1_RCAL*	Y
RCAL_MIPI	P	WIDTH_0P100	*MIPI*REXT	Y
RCAL_EUSB	P	WIDTH_0P100	SOC_ATC*_USB_RESREF,SOC_USBDBG_RESREF	Y
BOARD_ID	P	A_45_OHM_SE	BOARD_ID*	Y
BOARD_REV	P	A_45_OHM_SE	BOARD_REV*	Y
WIRELESS_TIME_SYNC	P	A_45_OHM_SE	*TIME_SYNC*	Y
KBD_PWM	P	A_45_OHM_SE	*KBD_BKLT_PWM*,BKLT_PWM_KEYB_3V3	Y

PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR DOWNSTREAM
CLASS NAME	NONE A-A	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GROUND	P	DEFAULT	GND	Y
ANALOG_GROUND	P	DEFAULT	*AGND*,GND_*	Y
AUDIO_CONN_HEADPHONE_OUT	P	WIDTH_0P400	AUDIO_JACK_LEFT_OUT,AUDIO_JACK_RIGHT_OUT	Y
AUDIO_CONN_HEADPHONE_OUT	P	WIDTH_0P400	AUD_CONN_LEFT_OUT,AUD_CONN_RIGHT_OUT	Y
AUDIO_CONN_RETURN	P	WIDTH_0P500	AUDIO_JACK_GB_GND,AUDIO_JACK_CH_GND	Y
AUDIO_CONN_RETURN	P	WIDTH_0P500	AUD_CONN_RING2,AUD_CONN_SLEEVE	Y
AUDIO_CONN_SENSE	P	WIDTH_0P100	AUDIO_JACK_LEFT_SNS,AUDIO_JACK_RIGHT_SNS	Y
AUDIO_CONN_SENSE	P	WIDTH_0P100	AUDIO_JACK_TIP_SNS,AUDIO_JACK_RING_SNS	Y
AUDIO_CONN_SENSE	P	WIDTH_0P100	AUD_CONN_LEFT_SNS,AUD_CONN_RIGHT_SNS	Y
AUDIO_CONN_SENSE	P	WIDTH_0P100	AUD_CONN_TIP_SENSE,AUD_CONN_RING_SENSE	Y
SPEAKERAMP_OUTPUT	P	SPKRAMP_OUT_DIFF	DP:DP_SPKRAMP_*_OUT	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_CHGR_CS*,DP_ISNS_*,DP_*VSNS_XW,DP_*_VSEN_XW	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_SPMU_TDEV,DP_SPKRAMP_*_VSENSE	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_P3V8AON_ISEN*,DP_THMSNS*,DP_ISNS_*LCD	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_SOC_*_RCAL,DP_P3V8IDIF2_FB	Y
SENSE_DIFF	P	SENSE_DIFF	DP:DP_P3V8AON_VSNS,DP_ATCRTMR*_THERM_D	Y
RF_ANTENNA	P	WIDTH_0P100	RF_ANT_0,RF_ANT_1	Y
PMU_BUCK_FB	P	VR_FEEDBACK	BUCK*_FB*	Y
POWER	P	POWER	PP*	Y

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SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DOMAIN E,P,S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	S	A_DIELECTRIC_3X	=	Y
SPI	S	A_DIELECTRIC_3X	=	Y
SPMI	S	A_DIELECTRIC_3X	=	Y
SWD	S	A_DIELECTRIC_3X	=	Y
JTAG	S	A_DIELECTRIC_2X	=	Y
CLOCK_24M	S	A_DIELECTRIC_8X	=	Y
SOC_XTAL_24M_IN	S	A_DIELECTRIC_8X	=	Y
SOC_XTAL_24M_OUT	S	A_DIELECTRIC_8X	=	Y
CLOCK_32K	S	A_DIELECTRIC_8X	=	Y
TDM_LEFT	S	A_DIELECTRIC_3X	=	Y
TDM_RIGHT	S	A_DIELECTRIC_3X	=	Y
TDM_CODEC	S	A_DIELECTRIC_3X	=	Y
SPKR_ICC	S	A_DIELECTRIC_3X	=	Y
UART	S	A_DIELECTRIC_2X	=	Y
RESETS	S	A_DIELECTRIC_3X	=	Y
WDOG	S	A_DIELECTRIC_3X	=	Y
SOCHOT	S	A_DIELECTRIC_3X	=	Y
POWER_BUTTON	S	A_DIELECTRIC_3X	=	Y
FAULT	S	A_DIELECTRIC_3X	=	Y
DMIC_PDM	S	A_DIELECTRIC_3X	=	Y
FAN_CTRL	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_BSB0_D2R_1	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_D2R_2	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_R2D_1	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_R2D_2	S	A_DIELECTRIC_9X	=	Y
USBC_SOC_BSB0_AUX	S	A_DIELECTRIC_7X	=	Y
USBC_SOC_BSB0_LSX	S	A_DIELECTRIC_7X	=	Y
USBC_BSB0_CONN_D2R_1	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_D2R_2	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_R2D_1	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_R2D_2	S	A_DIELECTRIC_9X	=	Y
USBC_BSB0_CONN_AUXLSX	S	A_DIELECTRIC_7X	=	Y
USBC_UPC0_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
USBC_UPC0_CONN_BOT	S	A_DIELECTRIC_5X	=	Y
USBC_UPC0_CONN_CC	S	A_DIELECTRIC_2X	=	Y
USBC_UPC0_CONN_SBU	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_RTMR0_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR0_MUX_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_UPC0_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_VITC_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_SOC_BSB1_D2R_1	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_D2R_2	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_R2D_1	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_R2D_2	S	A_DIELECTRIC_10X	=	Y
USBC_SOC_BSB1_AUX	S	A_DIELECTRIC_7X	=	Y
USBC_SOC_BSB1_LSX	S	A_DIELECTRIC_7X	=	Y
USBC_BSB1_CONN_D2R_1	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_D2R_2	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_R2D_1	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_R2D_2	S	A_DIELECTRIC_10X	=	Y
USBC_BSB1_CONN_AUXLSX	S	A_DIELECTRIC_7X	=	Y
USBC_UPC1_CONN_TOP	S	A_DIELECTRIC_5X	=	Y
USBC_UPC1_CONN_BOT	S	A_DIELECTRIC_5X	=	Y
USBC_UPC1_CONN_CC	S	A_DIELECTRIC_2X	=	Y
USBC_UPC1_CONN_SBU	S	A_DIELECTRIC_2X	=	Y
USBC_SOC_RTMR1_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR1_UPC1_USB2	S	A_DIELECTRIC_6X	=	Y
USBC_SOC_RTMR_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_RTMR_MUX_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_UPC_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_MUX_VITC_USB2_DBG	S	A_DIELECTRIC_6X	=	Y
USBC_LSX	S	A_DIELECTRIC_6X	=	Y
MIPI_FTCAM_CLK	S	A_DIELECTRIC_6X	=	Y
MIPI_FTCAM_DATA	S	A_DIELECTRIC_6X	=	Y
MIPI_DFR_CLK	S	A_DIELECTRIC_6X	=	Y
MIPI_DFR_DATA	S	A_DIELECTRIC_6X	=	Y
PCIE_WIFI_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_WIFI_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_WIFI_CLK	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND0_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND0_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND0_CLK	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND1_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND1_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_NAND1_CLK	S	A_DIELECTRIC_7X	=	Y
PCIE_CLKREQ	S	A_DIELECTRIC_2X	=	Y
PANEL_LPDP_DATA	S	A_DIELECTRIC_6X	=	Y
PANEL_LPDP_AUX	S	A_DIELECTRIC_6X	=	Y
RCAL_PCIE	S	A_DIELECTRIC_2X	=	Y
RCAL_CIO	S	A_DIELECTRIC_2X	=	Y
RCAL_MIPI	S	A_DIELECTRIC_2X	=	Y
RCAL_EUSB	S	A_DIELECTRIC_2X	=	Y
BOARD_ID	S	A_DIELECTRIC_2X	=	Y
BOARD_REV	S	A_DIELECTRIC_2X	=	Y
WIRELESS_TIME_SYNC	S	A_DIELECTRIC_2X	=	Y
KBD_PWM	S	A_DIELECTRIC_2X	=	Y
GROUND	S	DEFAULT	=	Y
ANALOG_GROUND	S	DEFAULT	=	Y
AUDIO_CONN_HEADPHONE_OUT	S	A_DIELECTRIC_3X	=	Y
AUDIO_CONN_RETURN	S	A_DIELECTRIC_2X	=	Y
AUDIO_CONN_SENSE	S	A_DIELECTRIC_2X	=	Y
SPEAKERAMP_OUTPUT	S	A_DIELECTRIC_2X	=	Y
SENSE_DIFF	S	A_DIELECTRIC_2X	=	Y
RF_ANTENNA	S	RF_ANTENNA	=	Y
PMU_BUCK_FB	S	DEFAULT	=	Y
POWER	S	DEFAULT	=	Y

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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	GROUND	DEFAULT
SPI	GROUND	DEFAULT
SPMI	GROUND	DEFAULT
SWD	GROUND	DEFAULT
JTAG	GROUND	DEFAULT
CLOCK_24M	GROUND	DEFAULT
CLOCK_32K	GROUND	DEFAULT
TDM_LEFT	GROUND	DEFAULT
TDM_RIGHT	GROUND	DEFAULT
TDM_CODEC	GROUND	DEFAULT
SPKR_ICC	GROUND	DEFAULT
UART	GROUND	DEFAULT
RESETS	GROUND	DEFAULT
WDOG	GROUND	DEFAULT
SOCHOT	GROUND	DEFAULT
POWER_BUTTON	GROUND	DEFAULT
FAULT	GROUND	DEFAULT
DMIC_PDM	GROUND	DEFAULT
FAN_CTRL	GROUND	DEFAULT
USBC_SOC_BSB0_D2R_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_D2R_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_R2D_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_R2D_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_AUX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_LSX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_D2R_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_D2R_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_R2D_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_R2D_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_AUXLSX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_TOP	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_BOT	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_CC	GROUND	DEFAULT
USBC_UPC0_CONN_SBU	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR0_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR0_MUX_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_UPC0_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_VITC_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_D2R_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_D2R_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_R2D_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_R2D_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_AUX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_LSX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_D2R_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_D2R_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_R2D_1	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_R2D_2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_AUXLSX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_TOP	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_BOT	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_CC	GROUND	DEFAULT
USBC_UPC1_CONN_SBU	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR1_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR1_UPC1_USB2	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR_USB2_DBG	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR_MUX_USB2_DBG	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_UPC_USB2_DBG	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_VITC_USB2_DBG	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_FTCAM_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_FTCAM_DATA	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_DFR_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_DFR_DATA	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_D2R	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_R2D	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_D2R	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_R2D	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_D2R	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_R2D	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_CLK	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_CLKREQ	GROUND	DEFAULT
PANEL_LPDP_DATA	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
PANEL_LPDP_AUX	GROUND	DEFAULT_WITH_5X_LINE2SHAPE
RCAL_PCIE	GROUND	DEFAULT
RCAL_CIO	GROUND	DEFAULT
RCAL_MIPI	GROUND	DEFAULT
BOARD_ID	GROUND	DEFAULT
BOARD_REV	GROUND	DEFAULT
WIRELESS_TIME_SYNC	GROUND	DEFAULT
KBD_PWM	GROUND	DEFAULT
AUDIO_CONN_HEADPHONE_OUT	GROUND	DEFAULT
AUDIO_CONN_RETURN	GROUND	DEFAULT
AUDIO_CONN_SENSE	GROUND	DEFAULT
SPEAKERAMP_OUTPUT	GROUND	DEFAULT
SENSE_DIFF	GROUND	DEFAULT
SOC_XTAL_24M_IN	GROUND	DEFAULT
SOC_XTAL_24M_OUT	GROUND	DEFAULT
POWER	GROUND	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
I2C	POWER	DEFAULT
SPI	POWER	DEFAULT
SPMI	POWER	DEFAULT
SWD	POWER	DEFAULT
JTAG	POWER	DEFAULT
CLOCK_24M	POWER	DEFAULT
CLOCK_32K	POWER	DEFAULT
TDM_LEFT	POWER	DEFAULT
TDM_RIGHT	POWER	DEFAULT
TDM_CODEC	POWER	DEFAULT
SPKR_ICC	POWER	DEFAULT
UART	POWER	DEFAULT
RESETS	POWER	DEFAULT
WDOG	POWER	DEFAULT
SOCHOT	POWER	DEFAULT
POWER_BUTTON	POWER	DEFAULT
FAULT	POWER	DEFAULT
DMIC_PDM	POWER	DEFAULT
FAN_CTRL	POWER	DEFAULT
USBC_SOC_BSB0_D2R_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_D2R_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_R2D_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_R2D_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_AUX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB0_LSX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_D2R_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_D2R_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_R2D_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_R2D_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB0_CONN_AUXLSX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_TOP	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_BOT	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC0_CONN_CC	POWER	DEFAULT
USBC_UPC0_CONN_SBU	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR0_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR0_MUX_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_UPC0_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_VITC_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_D2R_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_D2R_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_R2D_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_R2D_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_AUX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_BSB1_LSX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_D2R_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_D2R_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_R2D_1	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_R2D_2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_BSB1_CONN_AUXLSX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_TOP	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_BOT	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_UPC1_CONN_CC	POWER	DEFAULT
USBC_UPC1_CONN_SBU	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR1_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR1_UPC1_USB2	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_SOC_RTMR_USB2_DBG	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_RTMR_MUX_USB2_DBG	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_UPC_USB2_DBG	POWER	DEFAULT_WITH_5X_LINE2SHAPE
USBC_MUX_VITC_USB2_DBG	POWER	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_FTCAM_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_FTCAM_DATA	POWER	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_DFR_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
MIPI_DFR_DATA	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_D2R	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_R2D	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_WIFI_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_D2R	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_R2D	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND0_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_D2R	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_R2D	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_NAND1_CLK	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PCIE_CLKREQ	POWER	DEFAULT
PANEL_LPDP_DATA	POWER	DEFAULT_WITH_5X_LINE2SHAPE
PANEL_LPDP_AUX	POWER	DEFAULT_WITH_5X_LINE2SHAPE
RCAL_PCIE	POWER	DEFAULT
RCAL_CIO	POWER	DEFAULT
RCAL_MIPI	POWER	DEFAULT
BOARD_ID	POWER	DEFAULT
BOARD_REV	POWER	DEFAULT
WIRELESS_TIME_SYNC	POWER	DEFAULT
KBD_PWM	POWER	DEFAULT
AUDIO_CONN_HEADPHONE_OUT	POWER	DEFAULT
AUDIO_CONN_RETURN	POWER	DEFAULT
AUDIO_CONN_SENSE	POWER	DEFAULT
SPEAKERAMP_OUTPUT	POWER	DEFAULT
SENSE_DIFF	POWER	DEFAULT
SOC_XTAL_24M_IN	POWER	DEFAULT
SOC_XTAL_24M_OUT	POWER	DEFAULT
POWER	POWER	DEFAULT

SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
USBC_SOC_BSB0_D2R_1	USBC_SOC_BSB0_D2R_2	A_DIELECTRIC_6X
USBC_SOC_BSB0_R2D_1	USBC_SOC_BSB0_R2D_2	A_DIELECTRIC_6X
USBC_BSB0_CONN_D2R_1	USBC_BSB0_CONN_D2R_2	A_DIELECTRIC_6X
USBC_BSB0_CONN_R2D_1	USBC_BSB0_CONN_R2D_2	A_DIELECTRIC_6X
USBC_SOC_BSB1_D2R_1	USBC_SOC_BSB1_D2R_2	A_DIELECTRIC_6X
USBC_SOC_BSB1_R2D_1	USBC_SOC_BSB1_R2D_2	A_DIELECTRIC_6X
USBC_BSB1_CONN_D2R_1	USBC_BSB1_CONN_D2R_2	A_DIELECTRIC_6X
USBC_BSB1_CONN_R2D_1	USBC_BSB1_CONN_R2D_2	A_DIELECTRIC_6X
PANEL_LPDP_DATA	PANEL_LPDP_DATA	A_DIELECTRIC_5X
SOC_XTAL_24M_IN	SOC_XTAL_24M_OUT	A_DIELECTRIC_2X

SYNC_MASTER=CONSTRAINTS SYNC_DATE=01/08/2020

PAGE TITLE

17.2 SPACING CSETS, CLASS-CLASS

Apple Inc.

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SYNC_MASTER=T668_MLB SYNC_DATE=01/30/2020

PAGE TITLE

BOM TABLES

Apple Inc.

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SOC/CPU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-16917	1	IC,SGA,BGA2971	U0600	CRITICAL	SOC:DEV
998-21824	1	IC,SGA,A0+16G,1Y,15C,DEV,AX,M,ATK,B2971	U0600	CRITICAL	SOC:A0_16G
998-21826	1	IC,SGA,A0+32G,1Y,15C,DEV,AX,M,ATK,B2971	U0600	CRITICAL	SOC:A0_32G
939-09653	1	PCBF,NANJING,X2737	U0600	CRITICAL	SOC:SOCKET
998-23472	1	IC,SGA,B0+16G,1Y,8C,DEV,AXX,H,SCK,B2971	U0600	CRITICAL	SOC:B0_16G
998-23474	1	IC,SGA,B0+32G,1Y,8C,DEV,AXX,H,SCK,B2971	U0600	CRITICAL	SOC:B0_32G

SPACE LEFT FOR ADDITIONAL SOC APNs

BBR IC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-13316	3	IC,BURNSIDE BRIDGE,USB/TB RETIMER,BGA105	UF000,UF100,UG000	CRITICAL	ATCRTMR:DEV
338S00561	3	IC,TBT,BBR,SLMN7,PRQ,A1,BGA105	UF000,UF100,UG000	CRITICAL	BBR:A1_PRQ

ACE/UPC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S02158	3	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500,UG400	CRITICAL	ACE2:B2

BBR ROMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
341S01829	1	ROM,ACE/BBR-P01 (VXXX) P-2,X2728	UF260	CRITICAL	BBR_L_ROM:POC-2	<-LEFT
341S01831	1	ROM,ACE/BBR-P23 (VXXX) P-2,X2728	UG260	CRITICAL	BBR_R_ROM:POC-2	<-RIGHT

Magsafe Ace ROM APN -> CSA 55

BBR BOM ALT parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00537	335S00133		ALL	

EUSB LEVEL SHIFTER

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-23161	3	IC,MACAW,CYUSB2402A0,A0,VER 2,CSP24	UF700,UF750,UG700	CRITICAL	EUSB_LS:MACAW

OCARINA0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00600	1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56	UN400	CRITICAL	OCARINA0:A0_OTPBC

OCARINA1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00600	1	IC,PMU,OCARINA,D2499A0,OPT-BC,WLCSP56	UN900	CRITICAL	OCARINA1:A0_OTPBC

SECURE ELEMENT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00630	1	IC,SN210V,B1,CERES,PROD,VER=MU,WLCSP81	U5000	CRITICAL	SE:PROD_SW_MU
998-21255	1	IC,SN210V,B1,CERES,SW-H3,WLCSP81	U5000	CRITICAL	SE:DEV_SW_H3
338S00629	1	IC,SN210V,B1,CERES,DEV,VER=LN,WLCSP81	U5000	CRITICAL	SE:DEV_SW_LN

HDMI MADEA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00347	1	IC,HDMI,PUMA81,MCDP2920,A4,BGA117	UH700	CRITICAL	

HDMI CONNECTOR BOM OPTIONS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
514S00354	1	CONN,RCPT,HDMI,X2094	JH500	CRITICAL		HDMI CONN

SD CONNECTOR BOM OPTIONS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
514-00180	1	CONN,RCPT,SD,X2094	JK600	CRITICAL		SD CONN

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
514S00359	514S00354		ALL	
514-00204	514-00180		ALL	
514S00373	514S00354		ALL	
514-00214	514-00180		ALL	

NAND

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00480	1	NAND,3DV4,160GBT,XXX,S5E,256G,K,SLGA110	UN000	CRITICAL	NAND:512GB_TS
335S00462	3	NAND,3DV4,128GBT,XXX,S5E,256G,T,SLGA110	UN100,UN200,UN300	CRITICAL	NAND:512GB_TS
335S00437	4	NAND,3DV5,128GB,S5E,512G,H,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:512GB_HY
335S00436	1	NAND,3DV5,64GB,S5E,512G,H,SLGA110	UN500	CRITICAL	NAND:512GB_HY
335S00464	4	NAND,3DV4,256GBT,XXX,S5E,256G,T,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:1TB_TS
335S00472	4	NAND,3DV4,256GBT,XXX,S5E,256G,SD,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:1TB_WD
335S00438	4	NAND,3DV5,256GB,S5E,512G,H,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:1TB_HY
335S00436	1	NAND,3DV5,64GB,S5E,512G,H,SLGA110	UN500	CRITICAL	NAND:1TB_HY
335S00466	4	NAND,3DV4,512GBT,XXX,S5E,256G,T,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:2TB_TS
335S00474	4	NAND,3DV4,512GBT,XXX,S5E,256G,SD,SLGA110	UN000,UN100,UN200,UN300	CRITICAL	NAND:2TB_WD
335S00466	8	NAND,3DV4,512GBT,XXX,S5E,256G,T,SLGA110	UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800	CRITICAL	NAND:4TB_TS
335S00439	8	NAND,3DV5,512GB,S5E,512G,H,SLGA110	UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800	CRITICAL	NAND:4TB_HY
335S00468	8	NAND,3DV4,1TBT,XXX,S5E,512G,T,SLGA110	UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800	CRITICAL	NAND:8TB_TS
335S00458	8	NAND,3DV5,1024GBT,S5E,512G,H,SLGA110	UN000,UN100,UN200,UN300,UN500,UN600,UN700,UN800	CRITICAL	NAND:8TB_HY

NAND SOCKET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-08815	1	PCBF,BANDIPUR,X1711	UN000,UN500	CRITICAL	NAND:SOCKET

ENOISE CAP SELECTION

1V8 CAPS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S00037	5	CAP,CER,X6S,10UF,20%,4V,0402,LOW NOISE	C2740-C2744	CRITICAL	ENOISE_1V8_10UF:ZRB
138S00073	5	CAP,X6S,10UF,20%,6.3V,HZTL,MUR,0402	C2740-C2744	CRITICAL	ENOISE_1V8_10UF:HZTL
138S00036	5	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C80E5-C80E9	CRITICAL	ENOISE_1V8_20UF:ZRB
138S00035	5	CAP,CER,20UF,20%,2.5V,X6S,HRZTL,0402	C80E5-C80E9	CRITICAL	ENOISE_1V8_20UF:HZTL
998-22077	5	CAP,X6S,20UF,20%,2.5V,LOW NOISE,MS,0402	C80E5-C80E9	CRITICAL	ENOISE_1V8_20UF:ZRX

VDDH CAPS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S00036	30	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C9560-C9569,C9570-C9579,C9580-C9589	CRITICAL	ENOISE_VDDH_20UF:ZRB
138S00035	30	CAP,CER,20UF,20%,2.5V,X6S,HRZTL,0402	C9560-C9569,C9570-C9579,C9580-C9589	CRITICAL	ENOISE_VDDH_20UF:HZTL
998-22077	30	CAP,X6S,20UF,20%,2.5V,LOW NOISE,MS,0402	C9560-C9569,C9570-C9579,C9580-C9589	CRITICAL	ENOISE_VDDH_20UF:ZRX

20UF ZRB SOC CAPS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S00036	27	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C2350-C2353,C2355,C2356,C2358,C2359,C235D,C235E,C2510-C2519,C251A,C251B,C251C,C251D,C251E,C251F,C251G	CRITICAL	ENOISE_GRP1:20UF_ZRB
138S00036	22	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C2570-C2579,C257A,C257B,C257C,C257D,C257E,C257F,C257G,C2583-C2587	CRITICAL	ENOISE_GRP1:20UF_ZRB
138S00036	33	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C25A0-C25A9,C25AA,C25AB,C25AC,C25AD,C25AE,C25AF,C3150-C3159,C315A,C315B,C315C,C315D,C315E,C315F,C315G	CRITICAL	ENOISE_GRP1:20UF_ZRB
138S00036	25	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C2310-C2318,C2530-C2539,C253A,C253B,C253C,C253D,C253E,C253F	CRITICAL	ENOISE_GRP2:20UF_ZRB
138S00036	84	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C2910-C2917,C2930-C2937,C3750-C3783,C3950-C3983	CRITICAL	ENOISE_GRP2:20UF_ZRB
138S00036	22	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C2720-C2724,C3110-C3115,C3130-C3135,C3160-C3164	CRITICAL	ENOISE_GRP3:20UF_ZRB
138S00036	15	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C3300-C3304,C8084-C8088,C80J4-C80J8	CRITICAL	ENOISE_GRP3:20UF_ZRB

15UF ZRX SOC CAPS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-22815	27	CAP,X6S,15UF,20%,2.5V,LOW NOISE,MS,0402	C2350-C2353,C2355,C2356,C2358,C2359,C235D,C235E,C2510-C2519,C251A,C251B,C251C,C251D,C251E,C251F,C251G	CRITICAL	ENOISE_GRP1:15UF_ZRX
998-22815	22	CAP,X6S,15UF,20%,2.5V,LOW NOISE,MS,0402	C2570-C2579,C257A,C257B,C257C,C257D,C257E,C257F,C257G,C2583-C2587	CRITICAL	ENOISE_GRP1:15UF_ZRX
998-22815	33	CAP,X6S,15UF,20%,2.5V,LOW NOISE,MS,0402	C25A0-C25A9,C25AA,C25AB,C25AC,C25AD,C25AE,C25AF,C3150-C3159,C315A,C315B,C315C,C315D,C315E,C315F,C315G	CRITICAL	ENOISE_GRP1:15UF_ZRX
998-22815	25	CAP,X6S,15UF,20%,2.5V,LOW NOISE,MS,0402	C2310-C2318,C2530-C2539,C253A,C253B,C253C,C253D,C253E,C253F	CRITICAL	ENOISE_GRP2:15UF_ZRX
998-22815	84	CAP,X6S,15UF,20%,2.5V,LOW NOISE,MS,0402	C2910-C2917,C2930-C2937,C3750-C3783,C3950-C3983	CRITICAL	ENOISE_GRP2:15UF_ZRX
998-22815	22	CAP,X6S,15UF,20%,2.5V,LOW NOISE,MS,0402	C2720-C2724,C3110-C3115,C3130-C3135,C3160-C3164	CRITICAL	ENOISE_GRP3:15UF_ZRX
998-22815	15	CAP,X6S,15UF,20%,2.5V,LOW NOISE,MS,0402	C3300-C3304,C8084-C8088,C80J4-C80J8	CRITICAL	ENOISE_GRP3:15UF_ZRX

15UF HZTL SOC CAPS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S00392	27	CAP,X6S,15UF,20%,2.5V,HZTL,M,0402	C2350-C2353,C2355,C2356,C2358,C2359,C235D,C235E,C2510-C2519,C251A,C251B,C251C,C251D,C251E,C251F,C251G	CRITICAL	ENOISE_GRP1:15UF_HZTL
138S00392	22	CAP,X6S,15UF,20%,2.5V,HZTL,M,0402	C2570-C2579,C257A,C257B,C257C,C257D,C257E,C257F,C257G,C2583-C2587	CRITICAL	ENOISE_GRP1:15UF_HZTL
138S00392	33	CAP,X6S,15UF,20%,2.5V,HZTL,M,0402	C25A0-C25A9,C25AA,C25AB,C25AC,C25AD,C25AE,C25AF,C3150-C3159,C315A,C315B,C315C,C315D,C315E,C315F,C315G	CRITICAL	ENOISE_GRP1:15UF_HZTL
138S00392	25	CAP,X6S,15UF,20%,2.5V,HZTL,M,0402	C2310-C2318,C2530-C2539,C253A,C253B,C253C,C253D,C253E,C253F	CRITICAL	ENOISE_GRP2:15UF_HZTL
138S00392	84	CAP,X6S,15UF,20%,2.5V,HZTL,M,0402	C2910-C2917,C2930-C2937,C3750-C3783,C3950-C3983	CRITICAL	ENOISE_GRP2:15UF_HZTL
138S00392	22	CAP,X6S,15UF,20%,2.5V,HZTL,M,0402	C2720-C2724,C3110-C3115,C3130-C3135,C3160-C3164	CRITICAL	ENOISE_GRP3:15UF_HZTL
138S00392	15	CAP,X6S,15UF,20%,2.5V,HZTL,M,0402	C3300-C3304,C8084-C8088,C80J4-C80J8	CRITICAL	ENOISE_GRP3:15UF_HZTL

ACE/UPC OTP
---> CSA 162

ICEMAN
---> CSA 57

VIPER
---> CSA 93

MONACO
---> CSA 101,102,105

HDMI ROM
---> CSA 178

SYNC_MASTER=T668_MLB_5.7.0 SYNC_DATE=05/20/2020

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BOM OPTION TABLES

Apple Inc.

DRAWING NUMBER 051-05641 SIZE D
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Variable BOM Groups/Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00371	1	COMMON PARTS,MLB,X2728	BASE	CRITICAL	BASE_BOM
985-01342	1	DEV-PARTS,MLB,X2728	DEVEL	CRITICAL	DEVEL_BOM

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00371	COMMON PARTS,MLB,X2728	X2728_COMMON
985-01342	DEV-PARTS,MLB,X2728	X2728_DEVEL:ENG

X2728 BOM GROUPS

BOM GROUP	BOM OPTIONS
X2728_COMMON	SCH,PCB,COMMON,ALTERNATE,X2728_COMMON1,X2728_COMMON2,X2728_PROGPARTS,X2728_USBC,X2728_HDMI,X2728_PWR,X2728_BLC,SSD_SUPPORT:L1-L4,X2728_ENOISE
X2728_COMMON1	BOARD_ID,BOARD_REV:0101,BOOTCFG2,PCORE:6,FSTP:MIN,SD:REV6
X2728_COMMON2	SECDIS_EXT_CLK,DMIC_CLK_10OHM,SE:DEV_SW_LN,RF-CONN,BMU_I2C:1V8,KBD_NEW,P1V8_LS_ISNS:AMP
X2728_PROGPARTS	BBR_L_ROM:POC-2,BBR_R_ROM:POC-2,ACE5_ROM:T818,HDMI_ROM:FW_V1P130
X2728_USBC	BBR:A1_PRQ,ACE2:B2,EUSB_LS:MACAW,UPC_ATCRTMR_INT,UPC_EUSBLS_INT
X2728_HDMI	DATA_FILT,CLK_FILT,HDMI_SPF_AND:STUFF
X2728_BLC	BLC_BEN_IC:V4,BLC_5V_SERIES:10_OHM,BLC_5V_CAP:4P7_UF
X2728_PWR	X2728_PWR2,P3V8AON_IC:A2_R170,PBUS:3S,P3V8AON_LPM,MONACO,MONACO_SC,VIPER:3PH,BATT:POR,SYSDETL:BTN,MVK_OTP:AM,P5VS2_DSCHG,LDO_HDMI:5V
X2728_PWR2	WHAMOLA:1A,WHAMOLA_UVLO,DOUBLED_FET,VDDH_DISCHARGE,P3V8ILIM:BOM1_5V
X2728_ENOISE	ENOISE_VDDH_20UF:HZTL,ENOISE_GRP1:15UF_HZTL,ENOISE_GRP2:15UF_HZTL,ENOISE_GRP3:15UF_HZTL,ENOISE_1V8_10UF:HZTL,ENOISE_1V8_20UF:HZTL,ENOISE_ECPU_20UF:HZTL

DEV BOM GROUPS

BOM GROUP	BOM OPTIONS
X2728_DEVEL:ENG	ALTERNATE,USBC_DBG,DBG_BTN,SYSDETL:BTN,DBG_LED,VITAMIN-C:YES,DBG:FAN,SNSRES_DEV,BATT_DBG

NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
NANDCFG:STUDY	NAND_L_NMBR:6,NAND:S5E_STUDY
NANDCFG:INTERPOSER	NAND_L_NMBR,NAND:INTERPOSER

BOARD REV BOM

BOM GROUP	BOM OPTIONS
BOARD_REV:0000	BOARDREV3,BOARDREV2,BOARDREV1,BOARDREV0
BOARD_REV:0001	BOARDREV3,BOARDREV2,BOARDREV1
BOARD_REV:0010	BOARDREV3,BOARDREV2,BOARDREV0
BOARD_REV:0011	BOARDREV3,BOARDREV2
BOARD_REV:0111	BOARDREV3
BOARD_REV:0111	BOARDREV3
BOARD_REV:0100	BOARDREV3,BOARDREV1,BOARDREV0
BOARD_REV:0101	BOARDREV3,BOARDREV1

BOARD ID

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARDID3,BOARDID1

radar 57499790: T728 board ID number 0000101x

SSD Config Table

Controls NAND ICs and SSD support BOMs

BOM GROUP	Landings	BOM OPTIONS
SSD:TS-512	4	NAND:512GB_TS,OCARINA0:A0_OTPBC
SSD:HY-512	5	NAND:512GB_HY,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:5L
SSD:TS-1TB	4	NAND:1TB_TS,OCARINA0:A0_OTPBC
SSD:WD-1TB	4	NAND:1TB_WD,OCARINA0:A0_OTPBC
SSD:HY-1TB	5	NAND:1TB_HY,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:5L
SSD:TS-2TB	4	NAND:2TB_TS,OCARINA0:A0_OTPBC
SSD:WD-2TB	4	NAND:2TB_WD,OCARINA0:A0_OTPBC
SSD:TS-4TB	8	NAND:4TB_TS,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:HY-4TB	8	NAND:4TB_HY,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:TS-8TB	8	NAND:8TB_TS,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:HY-8TB	8	NAND:8TB_HY,OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L
SSD:NOS5E	0	OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC
SSD:8L-DCDC	8	OCARINA0:A0_OTPBC,OCARINA1:A0_OTPBC,BOM_SSD:8L

SSD Support BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00402	1	SSD PARTS,L5,MLB,X2728	SSD	CRITICAL	BOM_SSD:5L
685-00403	1	SSD PARTS,L5-L8,MLB,X2728	SSD	CRITICAL	BOM_SSD:8L

Adds to support Landings on common BOM

SSD Support BOM Definitions

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00402	SSD PARTS,L5,MLB,X2728	ALTERNATE,SSD_SUPPORT:L5
685-00403	SSD PARTS,L5-L8,MLB,X2728	ALTERNATE,SSD_SUPPORT:L5-L8

Host BOM
Common BOM
5L Support BOM
8L Support BOM

SSD Support BOM Groups

BOM GROUP	BOM OPTIONS
SSD_SUPPORT:L1-L4	SSD_2L,SSD_4L
SSD_SUPPORT:L5	SSD_OC1VR1,SSD_5L
SSD_SUPPORT:L5-L8	SSD_OC1VR1,SSD_5L,SSD_8L

20U SOC ECPU CAPS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S00036	6	CAP,CER,20UF,20%,2.5V,X6S,LOW NOISE,0402	C2354,C2357,C235A,C2358,C235C,C235F	CRITICAL	ENOISE_ECPU_20UF:ZRB
138S00035	6	CAP,CER,20UF,20%,2.5V,X6S,HRZTL,0402	C2354,C2357,C235A,C2358,C235C,C235F	CRITICAL	ENOISE_ECPU_20UF:HZTL
998-22077	6	CAP,X6S,20UF,20%,2.5V,LOW NOISE,0402	C2354,C2357,C235A,C2358,C235C,C235F	CRITICAL	ENOISE_ECPU_20UF:ZRX

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BOM GROUPS

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BOM VARIANT TABLES

BOM NUMBER	BOM NAME	BOM OPTIONS
639-12852	PCBA,MLB-S,16GB,TS-512,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:TS-512
639-13090	PCBA,MLB-S,16GB,HY-512,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:HY-512
639-14421	PCBA,MLB-S,16GB,TS-1TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:TS-1TB
639-14434	PCBA,MLB-S,16GB,HY-1TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:HY-1TB
639-14422	PCBA,MLB-S,16GB,TS-2TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:TS-2TB
639-15061	PCBA,MLB-S,16GB,WD-1TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:WD-1TB
639-14423	PCBA,MLB-S,16GB,WD-2TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:WD-2TB
639-14424	PCBA,MLB-S,16GB,TS-4TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:TS-4TB
639-14425	PCBA,MLB-S,16GB,HY-4TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:HY-4TB
639-12853	PCBA,MLB-S,16GB,TS-8TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:TS-8TB
639-14426	PCBA,MLB-S,16GB,HY-8TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_16G,SSD:HY-8TB
639-14427	PCBA,MLB-S,32GB,HY-512,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:HY-512
639-12946	PCBA,MLB-S,32GB,TS-512,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:TS-512
639-13091	PCBA,MLB-S,32GB,HY-1TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:HY-1TB
639-14428	PCBA,MLB-S,32GB,WD-1TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:WD-1TB
639-14429	PCBA,MLB-S,32GB,TS-1TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:TS-1TB
639-14430	PCBA,MLB-S,32GB,WD-2TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:WD-2TB
639-15262	PCBA,MLB-S,32GB,TS-2TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:TS-2TB
639-14431	PCBA,MLB-S,32GB,TS-4TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:TS-4TB
639-14940	PCBA,MLB-S,32GB,HY-4TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:HY-4TB
639-12947	PCBA,MLB-S,32GB,TS-8TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:TS-8TB
639-14432	PCBA,MLB-S,32GB,HY-8TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:HY-8TB
939-10452	PCBA,MLB-S,SOCKET,SOC,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:SOCKET,SSD:NOS5E
939-10453	PCBA,MLB-S,NO SOC,X2728	BASE_BOM,DEVEL_BOM,NAND:SOCKET
939-11387	PCBA,MLB-S,SOCKET-SOC,8L-DCDC,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:SOCKET,SSD:8L-DCDC
939-11388	PCBA,MLB-S,SPF-VAL,32GB,8TB,X2728	BASE_BOM,DEVEL_BOM,ALTERNATE,SOC:B0_32G,SSD:TS-8TB

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BOM VARIANT TABLES

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01346	353S01320	ANY	ALL	<RDAR://56390543>
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107S0276	107S00020	ANY	ALL	<RDAR://57126636>
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353S02030	353S01993	ANY	ALL	<RDAR://57133661>
138S00284	138S00136	ANY	ALL	<RDAR://57134599>
132S00229	132S00010	ANY	ALL	<RDAR://57135129>
107S00346	107S00116	ANY	ALL	<RDAR://57135567>
138S0852	138S0818	ANY	ALL	<RDAR://57137990>
138S0750	138S00097	ANY	ALL	<RDAR://57138474>
152S00864	152S00851	ANY	ALL	<RDAR://57159654>
138S00181	138S0835	ANY	ALL	<RDAR://57161300>
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353S00878	353S00599	ANY	ALL	<RDAR://57173083>
371S00220	371S00181	ANY	ALL	<RDAR://57196734>
376S00146	376S1061	ANY	ALL	<RDAR://57198167>
311S00013	311S0508	ANY	ALL	<RDAR://57211339>
197S00046	197S00036	ANY	ALL	<RDAR://57229594>
197S00047	197S00036	ANY	ALL	<RDAR://57229594>
197S00048	197S00036	ANY	ALL	<RDAR://57229594>
377S0155	377S0184	ANY	ALL	<RDAR://57230484>
371S0718	371S0531	ANY	ALL	<RDAR://57233043>
353S00852	353S4262	ANY	ALL	<RDAR://57244062>
138S00229	138S00107	ANY	ALL	<RDAR://64381231>
107S00056	107S00086	ANY	ALL	<RDAR://64241290>
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107S00104	107S00061	ANY	ALL	<RDAR://64241122>
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155S00155	155S0441	ANY	ALL	<RDAR://65043740>
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155S0660	155S0513	ANY	ALL	<RDAR://65045000>
155S0694	155S0387	ANY	ALL	<RDAR://65044861>
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376S00488	376S00455	ANY	ALL	<RDAR://73219378>
152S01037	152S00887	ANY	ALL	<RDAR://65152741>
152S01070	152S00887	ANY	ALL	<RDAR://65152741>
152S00182	152S00703	ANY	ALL	<RDAR://64435747>
152S01415	152S01280	ANY	ALL	<RDAR://64722980>
152S01344	152S00883	ANY	ALL	<RDAR://64434865>
152S01451	152S00883	ANY	ALL	<RDAR://64434865>

152S01023	152S00384	ANY	ALL	<RDAR://64458983>
152S00841	152S00238	ANY	ALL	<RDAR://64476987>
152S00801	152S00695	ANY	ALL	<RDAR://64386631>
152S00367	152S01248	ANY	ALL	<RDAR://67823644>
152S01452	152S01248	ANY	ALL	<RDAR://67823644>
152S00785	152S00477	ANY	ALL	<RDAR://69846739>
107S0150	107S0208	ANY	ALL	<RDAR://64240857>
107S00298	107S0208	ANY	ALL	<RDAR://64240857>
107S00101	107S00005	ANY	ALL	<RDAR://64239203>
107S00392	107S00391	ANY	ALL	
376S00086	376S0761	ANY	ALL	
376S1147	376S00281	ANY	ALL	
128S00058	128S00098	ANY	ALL	
128S00105	128S00098	ANY	ALL	
152S01024	152S00386	ANY	ALL	

SOC & Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
998-21821	998-21824	ANY	ALL	SOC:A0_16G_S	
998-21818	998-21824	ANY	ALL	SOC_A0_16G_H	
998-21820	998-21826	ANY	ALL	SOC_A0_32G_H	
998-23473	998-23472	ANY	ALL	SOC_B0_16G_H	16GB HY ATK
998-23478	998-23472	ANY	ALL	SOC_B0_16G_M	16GB MC SCK
998-23479	998-23472	ANY	ALL	SOC_B0_16G_M	16GB MC ATK
998-23476	998-23472	ANY	ALL	SOC_B0_16G_S	16GB SS SCK
998-23477	998-23472	ANY	ALL	SOC_B0_16G_S	16GB SS ATK
998-23475	998-23474	ANY	ALL	SOC_B0_32G_H	32GB HY ATK
998-23480	998-23474	ANY	ALL	SOC_B0_32G_M	32GB MC SCK
998-23481	998-23474	ANY	ALL	SOC_B0_32G_M	32GB MC ATK
998-23481	998-23474	ANY	ALL	SOC_B0_32G_M	32GB MC ATK

WIFI MODULE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-20460	998-20465	ANY	ALL	<RDAR://56163271>

BLC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0738	138S1101	ANY	ALL	<RDAR://55465318>
138S0846	138S0811	ANY	ALL	<RDAR://55465318>
376S1053	376S0604	ANY	ALL	<RDAR://55465318>
152S00359	152S00253	ANY	ALL	<RDAR://55465318>
740S00041	740S0159	ANY	ALL	<RDAR://55465318>
371S00077	371S00180	ANY	ALL	<RDAR://55465318>
376S1106	376S0678	ANY	ALL	<RDAR://55465318>
107S00033	107S00034	ANY	ALL	<RDAR://55465318>
138S00087	138S1086	ANY	ALL	<RDAR://55465318>
152S00812	152S1701	ANY	ALL	<RDAR://55465318>
371S00217	371S00079	ANY	ALL	<RDAR://55465318>
152S00700	152S00285	ANY	ALL	<RDAR://64470558>
152S00017	152S00016	ANY	ALL	<RDAR://68780391>
152S00119	152S00016	ANY	ALL	<RDAR://68780391>
376S00021	376S00263	ANY	ALL	<RDAR://72834033>
376S0927	376S00263	ANY	ALL	<RDAR://73477267>
128S00017	128S00016	ANY	ALL	<RDAR://73477267>
128S0487	128S00012	ANY	ALL	<RDAR://73477267>

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BOM ALTERNATES

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REF_CLVR_MONACO

PACK_OPTIONS TO INCLUDE IN NETLIST
CLVR_C-CHOP
CLVR_2C_SC

REF_VR_ICEMAN

PACK_OPTIONS TO INCLUDE IN NETLIST
3V8_AON_PBUS-B12
3V8_AON_I2C-DEV
3V8_EXT_DIODE
3V8_INDUCTOR:2P4MM

REF_VR_ICEMAN_HP

PACK_OPTIONS TO INCLUDE IN NETLIST
P3V8ILIM_MUX:Y

REF_VR_VIPER

PACK_OPTIONS TO INCLUDE IN NETLIST
VIPER:3PH
VIPER_DBG
VIPER_L3MM
VIPER_C9543

REF_VR_5V_TPS62130

PACK_OPTIONS TO INCLUDE IN NETLIST
5VS2TPS_PBUS-B12

REF_VR_3V3_TPS62135

PACK_OPTIONS TO INCLUDE IN NETLIST
3V3_S2_PBUS-B12

REF_USBC_ACE2

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_LAPTOP
USBC_SPI_UPC0
USBC_SPI_UPC2
USBC_DEBUG_UPC0
PKGS:LARGER_PITCH

REF_STORAGE_S5E

PACK_OPTIONS TO INCLUDE IN NETLIST
2V5_NAND_PBUS-B12

REF_SECDIS_SAK

PACK_OPTIONS TO INCLUDE IN NETLIST
PROD_SECDIS
JTAG_SECDIS:YES
PROD_SECDIS_NOTMIPI
PROTO_PULLDOWN_SECDIS

REF_SPKRAMP_SN012776

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A
SPKRAMP_B
SPKRAMP_C
SPKRAMP_D
SPKRAMP_E
SPKRAMP_F
SPKRAMP_ICC_GB

REF_WIRELESS_TYPHOON

PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
3X_ANTENNA
WLBT_D2R_TP_JADE

REF_PMIC_MAVERICKS

PACK_OPTIONS TO INCLUDE IN NETLIST
PMU_IPD
SPMU_LDO3
MPMU_LDO4
SPMU_SW1
SPMU_LDO3
PMUOTP:R
PMU_DISP2:N
PMU32K:OSC_QRTZ
PMU_BBAT:N
SPMU_0201:DS

REF_HDMI_MADEA

PACK_OPTIONS TO INCLUDE IN NETLIST
HDMI_LDO:ON-SEMI
HDMI_CMC:YES
HDMI2SOC:ATC3

REF_SOC_H13S

PACK_OPTIONS TO INCLUDE IN NETLIST
SEEPROM_DEV
LPDPTX_X4
LPDPRX_X1
MIPID_DEV
MIPID_NC
ENET_NC
ATC3_HDMI
NAND_8X
SDCARD
SPMI_R
GPPCIE3_DEV

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PACK_OPTIONS TO INCLUDE IN NETLIST
P1
POR
VITAMINC

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PACK OPTIONS

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