Cottonwood Schematics
Skylake-U

2015-07-08

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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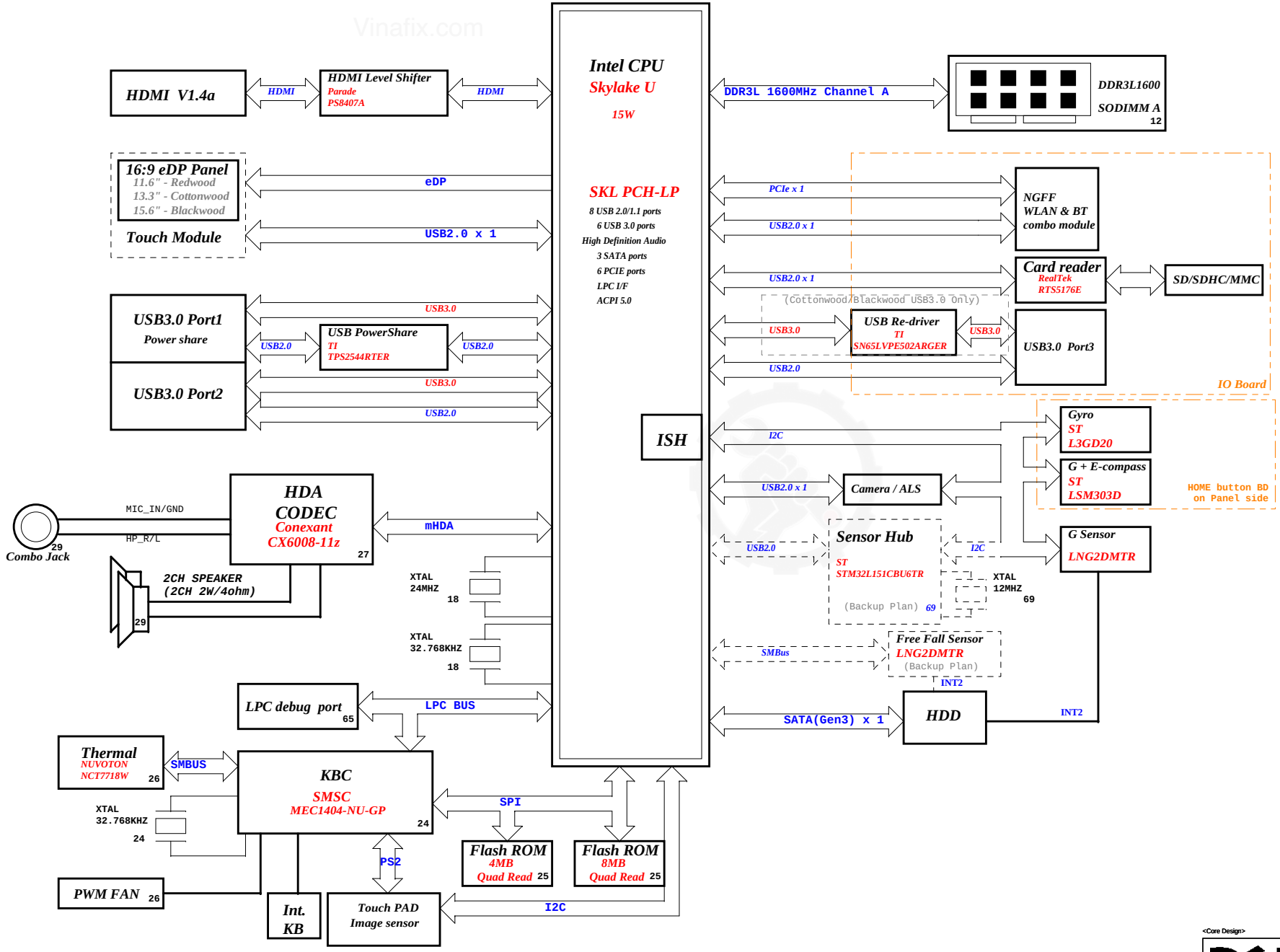
Title: *Cover Page*		
Size: A3	Document Number: Cottonwood SKL-U	Rev: A00
Date: Thursday, July 09, 2015	Sheet 1 of 105	

Project code: 4PD05M010001
PCB P/N: 14275
Revision: A00

Cottonwood SKL-U Block Diagram



CHARGER		
BQ24770RUYR-GP		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC		
TPS51225RUKR-GP		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_PWR_2 5V_S5 3D3V_S5	

CPU Core Power		
NCP81208MNTXG-GP NCP81382MNTXG-1-GP NCP81382MNTXG-1-GP NCP81253MNTBG-GP		46~50
INPUTS	OUTPUTS	
DCBATOUT DCBATOUT DCBATOUT	VCC_CORE +VCCGT +VCCSA_VR	

DDR3L SUS		
SY8206DQNC-GP-U APL5338XAI-TRG-GP		51
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D675V_S0	

CPU DCDC-V1D00A		
SY8208DQNC-GP-U		52
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	

LDO-V1D5V		
S-1339D15-M5001-GP		54
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	

LDO-V1D8V		
APL5930KAI-TRG		54
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	

5V/3V S0		
G5016KD1U		40
INPUTS	OUTPUTS	
5V_S5 3D3V_S5	5V_S0 3D3V_S0	

VCCSTG		
SLG59M1470VTR		40
INPUTS	OUTPUTS	
1D0V_S5	+VCCSTG	

VCCST		
SLG59M1470VTR		40
INPUTS	OUTPUTS	
1D0V_S5	+V1.00U_CPU	

<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
C	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 2 of 105

Main Func = CPU

(Blanking)

<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *Cottonwood SKL-U* | Rev: *A00*

Date: Wednesday, July 08, 2015 | Sheet 3 of 105

Main Func = CPU

#544669 CRB Rev0.52

+VCCSTG = 1.0 V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

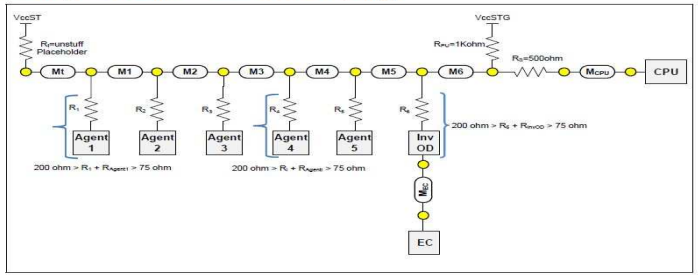
#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm

071.SKYLA.000U

Add resistor by NON DS3 function

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

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Title: CPU_(JTAG/CPU SIDE BAND)

Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

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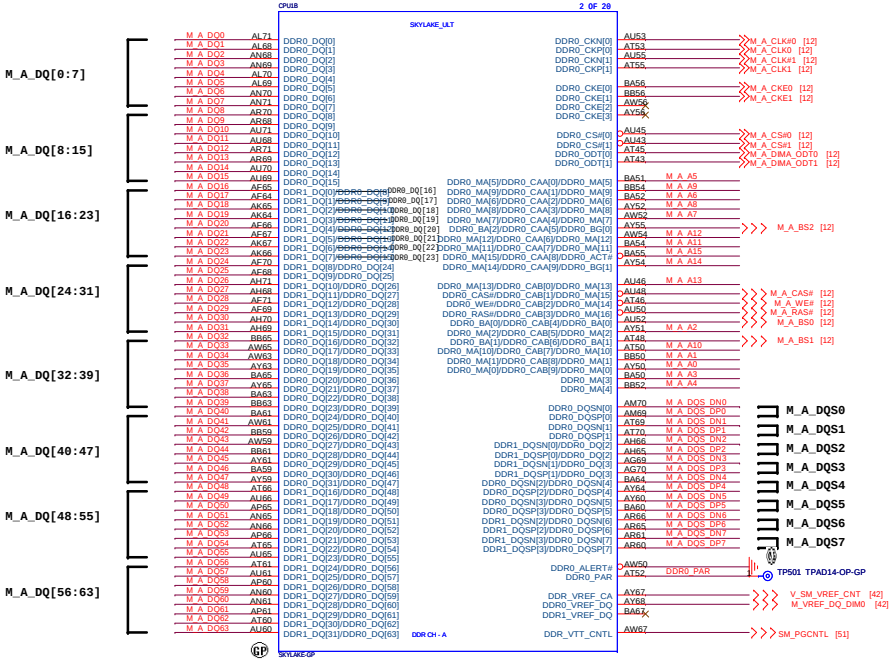
Main Func = CPU

DDR3L ball type:Non Interleaved Type

[12] M_A_DQ[63:0]



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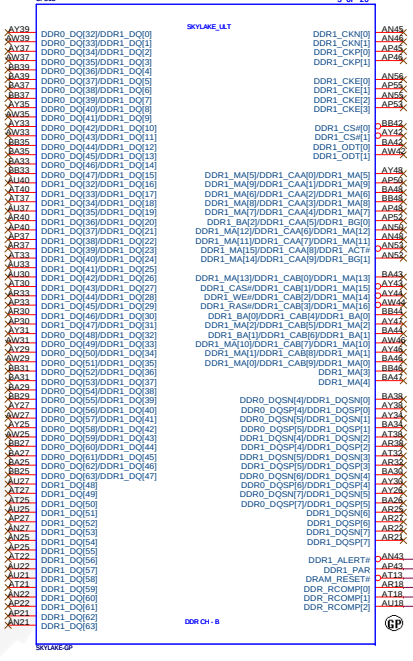

071.SKYLA.000U

M_A_DQS0
M_A_DQS1
M_A_DQS2
M_A_DQS3
M_A_DQS4
M_A_DQS5
M_A_DQS6
M_A_DQS7

TP501 TPAD14-OP-GP

M_A_CLK#0 [12]
M_A_CLK0 [12]
M_A_CLK#1 [12]
M_A_CLK1 [12]
M_A_CKE0 [12]
M_A_CKE1 [12]
M_A_CS#0 [12]
M_A_CS#1 [12]
M_A_DIMA_ODT0 [12]
M_A_DIMA_ODT1 [12]
M_A_BS2 [12]
M_A_CAS# [12]
M_A_WE# [12]
M_A_RAS# [12]
M_A_BS0 [12]
M_A_BS1 [12]
V_SM_VREF_CNT [42]
M_VREF_DQ_DIM0 [42]
SM_PGCNTL [51]

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

M_A_A[15:0] [12]

M_A_DQS_DN[7:0] [12]

M_A_DQS_DP[7:0] [12]

TP502 TPAD14-OP-GP
R501 121R2F-GP
R502 80D6R2F-L-GP
R503 100R2F-L1-GP-U
#543016
SM_DRAMRST# [12]
ED501 AZ5725-01FDR7G-GP
EMI DVT1 0210

Layout Note:
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

<Core Design>

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Title: CPU (DDR)
Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00
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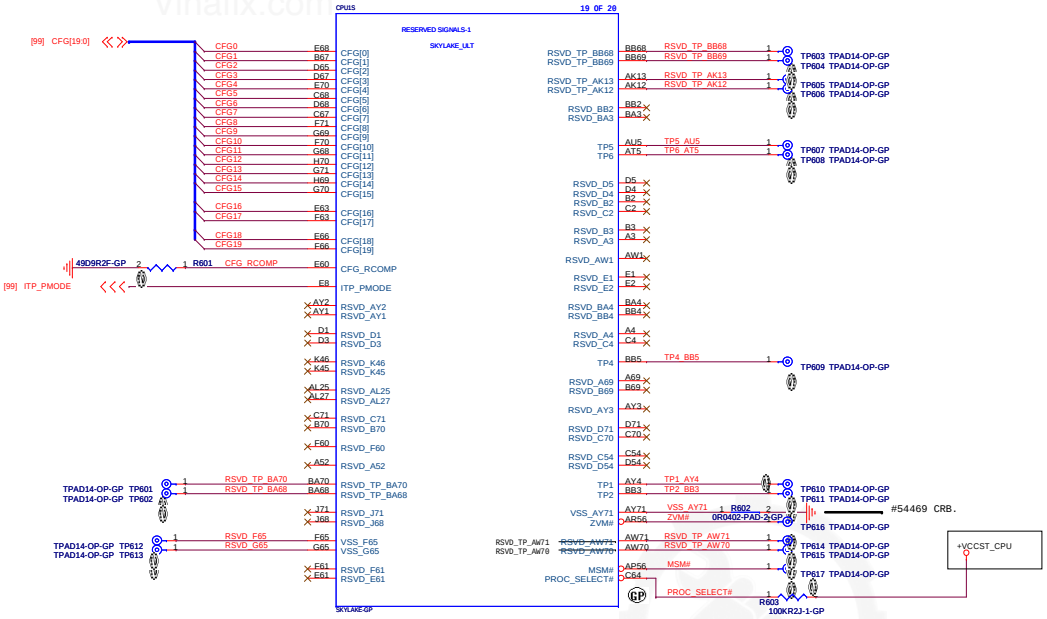
Main Func = CPU



PCH strap pin:

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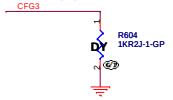
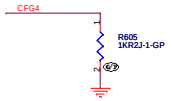


[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

(#543016)



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Design>

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Title: CPU (RESERVED)

Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

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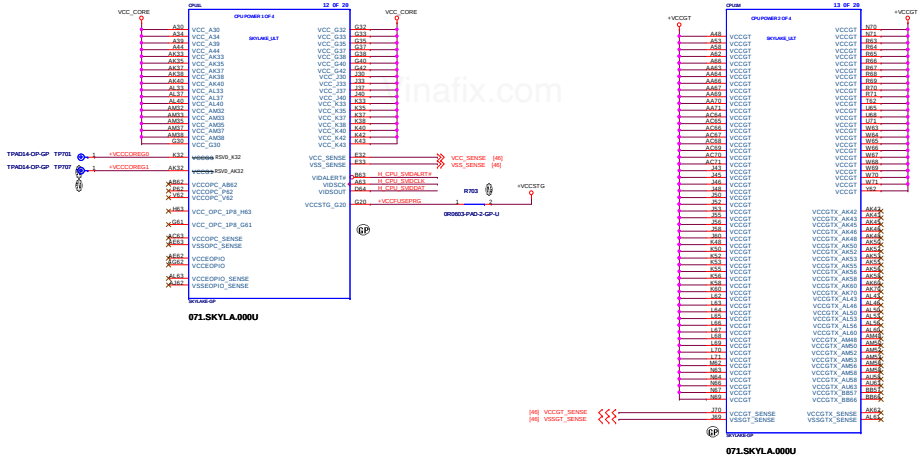
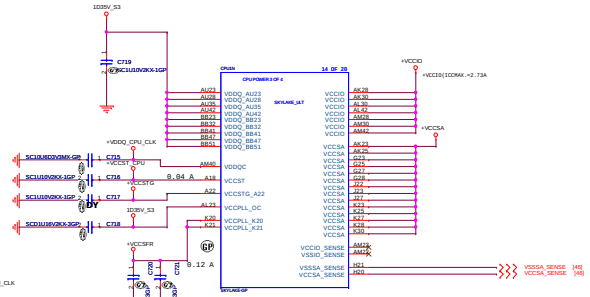
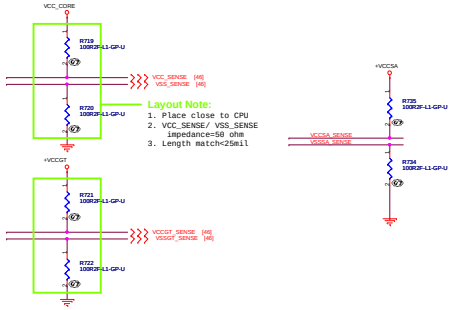
Main Func = CPU

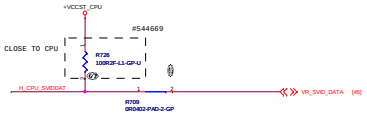




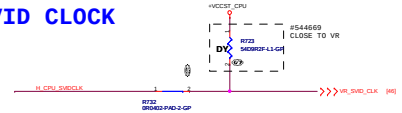


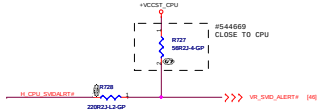
SVID DATA

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID CLOCK





SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

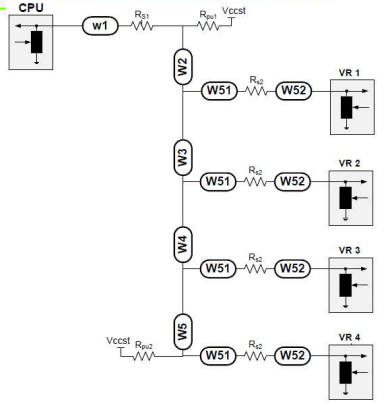
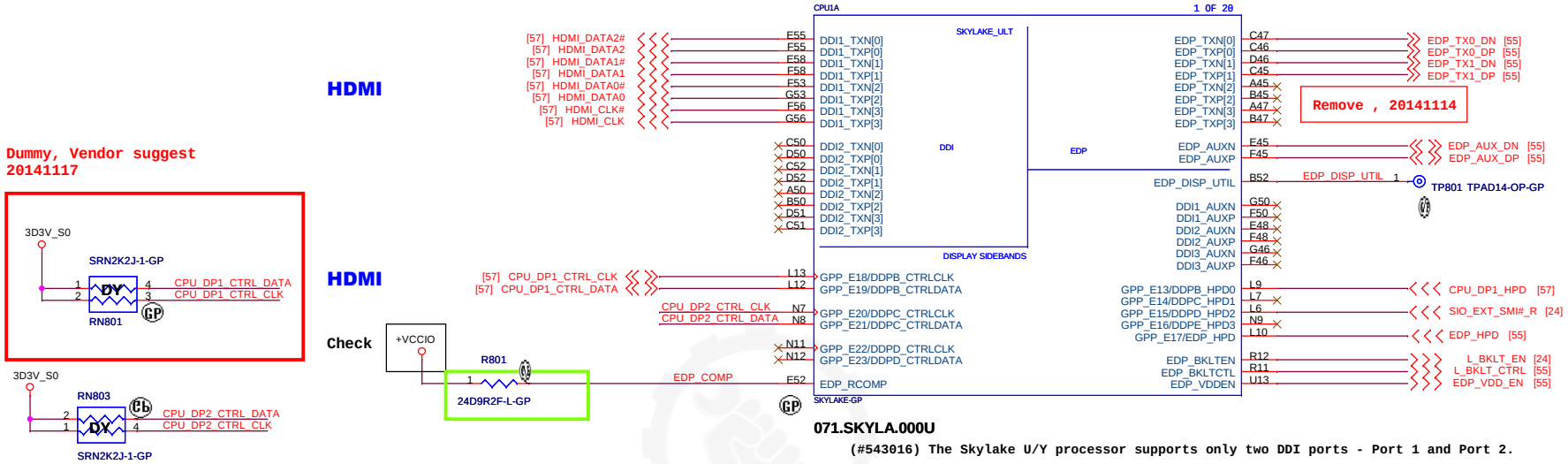


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{pu1} [Ω]	R_{pu2} [Ω]	R_{s1} [Ω]	R_{s2} [Ω]	VCCprr [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

Main Func = CPU



071.SKYLA.000U

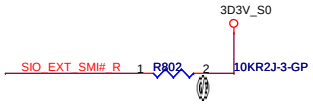
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC



Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

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Title: CPU (DISPLAY)

Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

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Main Func = CPU

(Blanking)

<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *Cottonwood SKL-U* | Rev: *A00*

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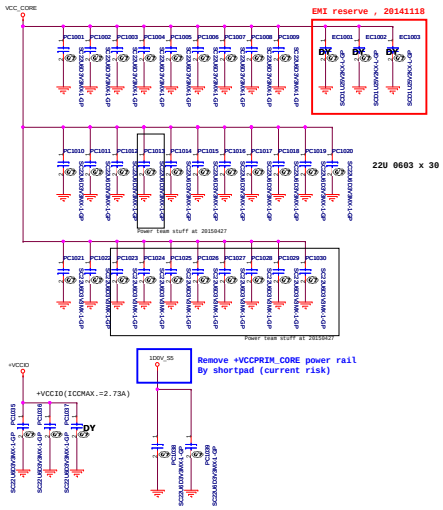
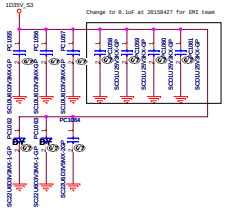
Main Func = CPU

20140814 DAVID

CORE

U-line 23e 28W
IccMax current-10ms max = 34 A

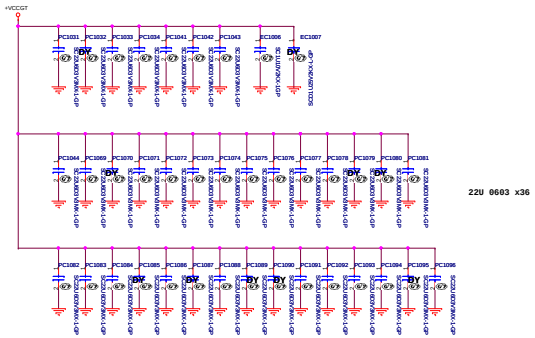




VCCSA

SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A



(#543016 PDG)

Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

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File: CPU (Power CAP1)

Size	Document Number	Rev
A1	Cottonwood SKL-U	A00

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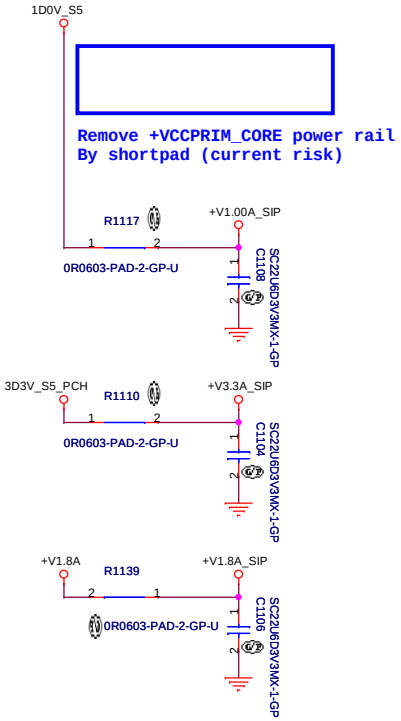
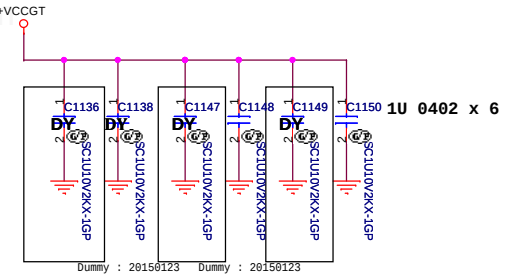
Main Func = CPU

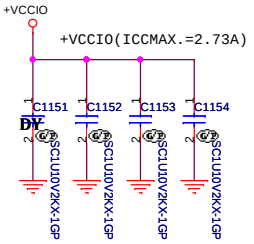
PCH DERIVED RAILS

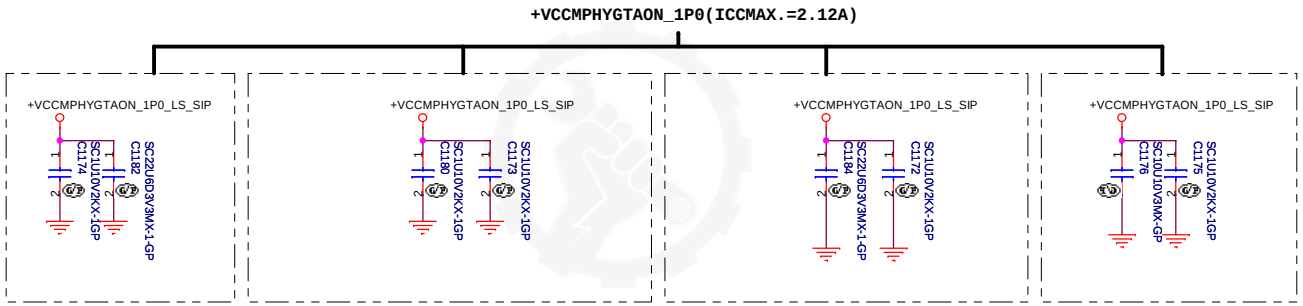


UNSLICED GT



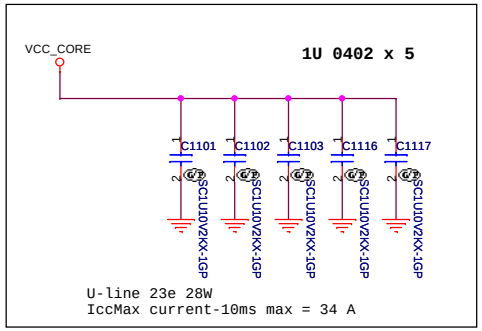
VCCIO

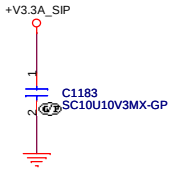




Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15





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Title	CPU (Power CAP2)	
Size: A3	Document Number: Cottonwood SKL-U	Rev: A00
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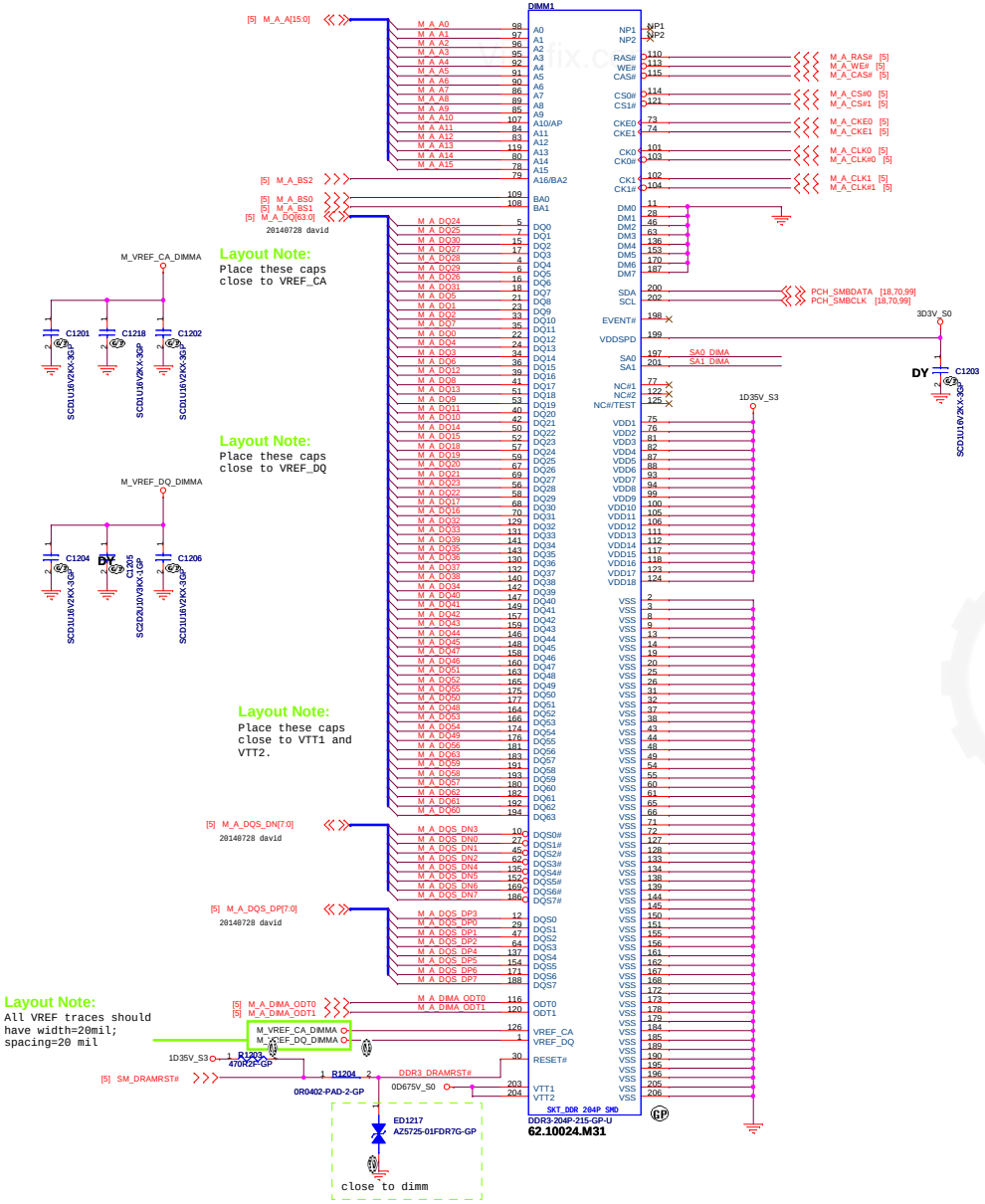
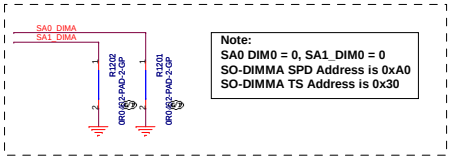
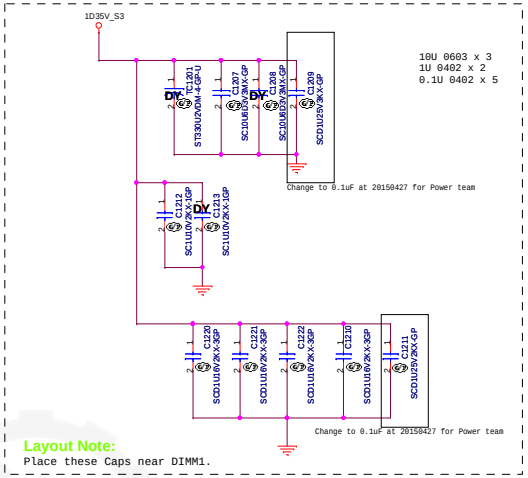
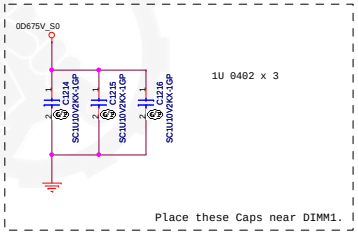
Main Func = DDR SODIMM









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Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 12 of 105

Main Func = DDR SODIMM

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Wednesday, July 08, 2015 | Sheet 13 of 105

(Blanking)

<Core Design>

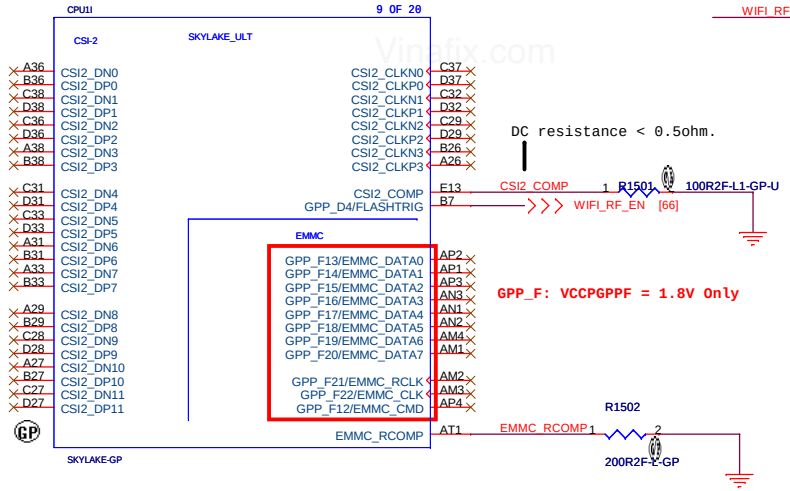
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
A4	*Cottonwood SKL-U*	*A00*

Date: Wednesday, July 08, 2015 Sheet 14 of 105

Main Func = PCH



071.SKYLA.000U

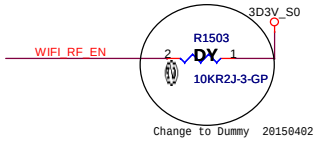


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

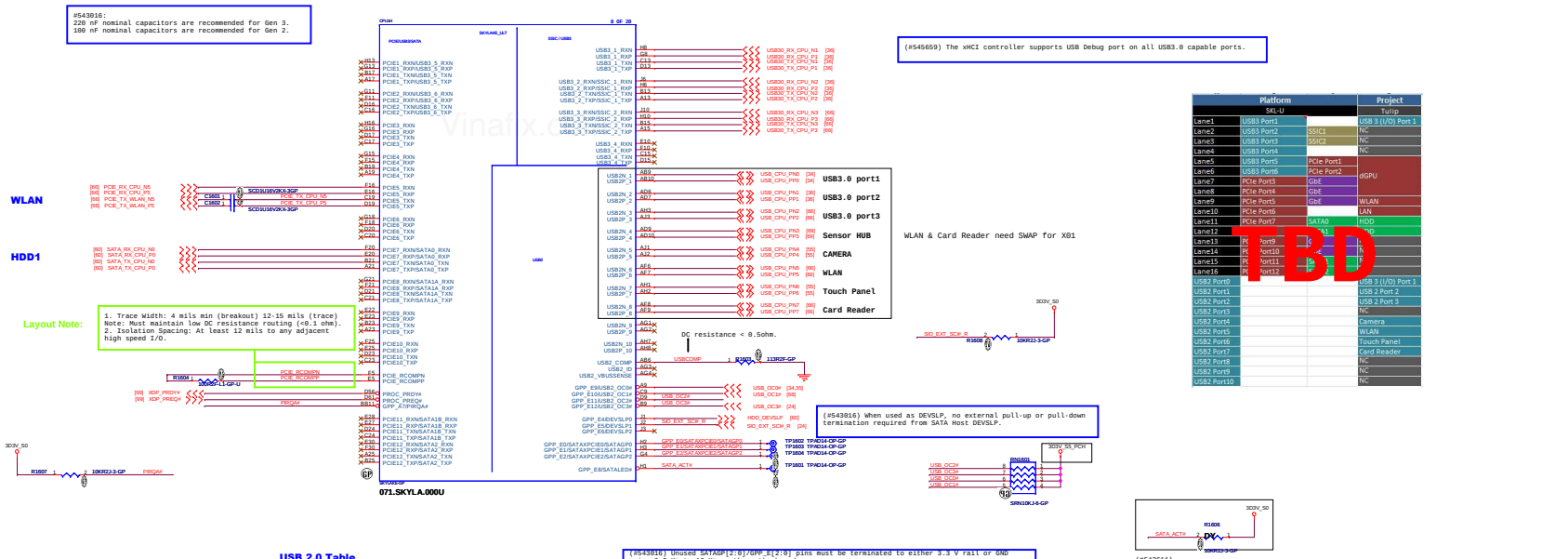
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CS-2/EMMC)

Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Wednesday, July 08, 2015 | Sheet 15 of 105

Main Func = PCH



(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

WLAN & Card Reader need SWAP for X01

Platform			Project
SKL-U			Tulip
Lane1	USB3 Port1		USB 3 (I/O) Port 1
Lane2	USB3 Port2	SSIC1	NC
Lane3	USB3 Port3	SSIC2	NC
Lane4	USB3 Port4		NC
Lane5	USB3 Port5	PCIe Port1	dGPU
Lane6	USB3 Port6	PCIe Port2	
Lane7	PCIe Port3	GbE	
Lane8	PCIe Port4	GbE	
Lane9	PCIe Port5	GbE	WLAN
Lane10	PCIe Port6		LAN
Lane11	PCIe Port7	SATA0	HDD
Lane12	[illegible]	A1	[illegible]
Lane13	PC	Port9	[illegible]
Lane14	PC	Port10	[illegible]
Lane15	PC	Port11	[illegible]
Lane16	PC	Port12	[illegible]
USB2 Port0			USB 3 (I/O) Port 1
USB2 Port1			USB 2 Port 2
USB2 Port2			USB 2 Port 3
USB2 Port3			NC
USB2 Port4			Camera
USB2 Port5			WLAN
USB2 Port6			Touch Panel
USB2 Port7			Card Reader
USB2 Port8			NC
USB2 Port9			NC
USB2 Port10			NC

(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

(#543016) Unused SATA6P[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2 (Debug Port/IOBD)
2	USB3.0 Port3 (IOBD)
3	Sensor HUB
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

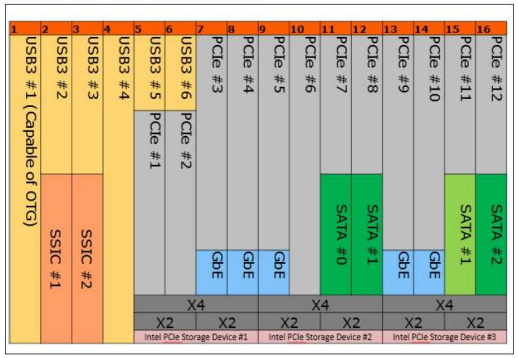


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

File: CPU (PCIE/SATA/USB)

Size: A1 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Wednesday, July 08, 2015 | Sheet 16 of 106

Main Func = PCH

Remove Power rail +V3.3A_SIP and R1712(DY), 20141118

Layout note: 3 PAD SHARING

#544669 (CRB): 330k.

[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

GPD11 pull high by Intel PDG1.3 request

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

NON DS3

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

071.SKYLA.000U

Remove SIO_SLP_S0#

BATLOW#:
Pull-up required even if not implemented.

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

Modify HSIO power switch IC and relate schematic ,DVT1 20150204

+VCCMPHYGTAON_1P0
SKL: 1.0V
+VCCMPHYGTAON_1P0(ICCMAX.=3.5A)

Dis-wire with XDP_PM_RSMRST_PWRGD_XDP

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

DS3 BOM Option

Change dummy property from DS3 to DY

Change location to net PCH_DPWROK

Dummy C1710 by it's useless

EC1711 modify to 100k and 0.01uF at DVT1 20150203

4th = 84.DMN66.03F
3rd = 75.00601.07C
2nd = 84.2N702.E3F
84.2N702.A3F

83.R2004.G8F

Reserve by NON DS3 function 20150413

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C
4th = 84.DMN66.03F

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00
Date: Thursday, July 23, 2015 | Sheet 17 of 105

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

PLACE WITHIN 1.1 INCH OF PCH

(#543016)Optional, can be left as OPEN/No-Connect.

RCIN#:
Frequency to Avoid: 33 MHz

SERIRQ PH:
PDG: 8.2k
CRB: 10k

WLAN

071.SKYLA.000U

20140820 DAIVD

Layout: Place at the open door area.

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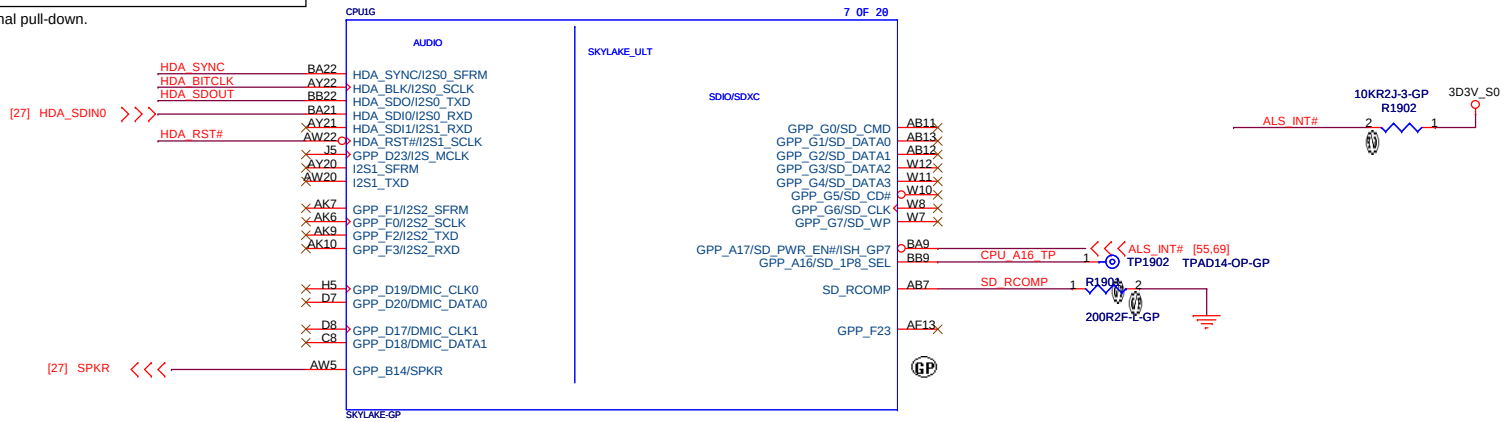
Title: CPU_(LPC/SPI/SMBUS/CL/CLK)
Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00
Date: Thursday, July 23, 2015 | Sheet 18 of 105

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

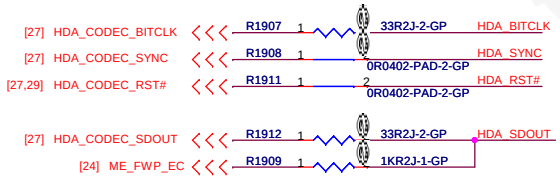
The internal pull-down is disabled after PLTRST# deasserts

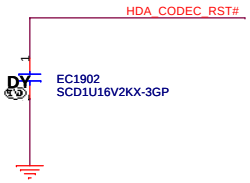
PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

071.SKYLA.000U





<Core Design>

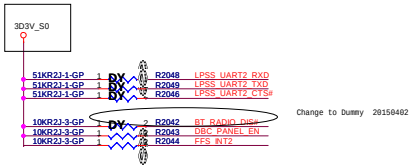
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (AUDIO/SDIO/SDXC)

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 19 of 105

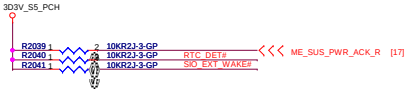
Main Func = PCH

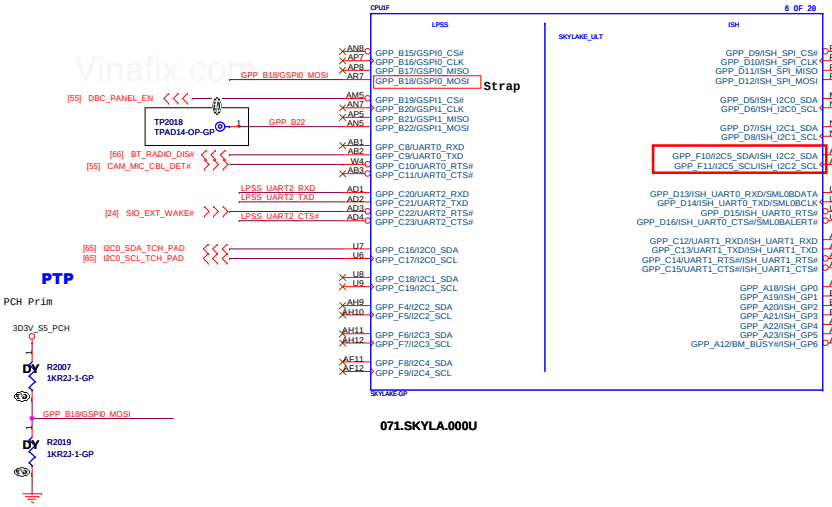


PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

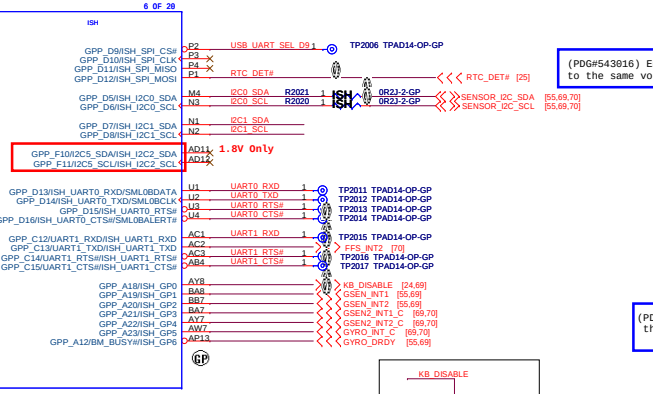


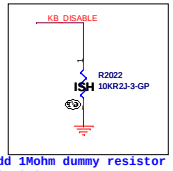


PTP

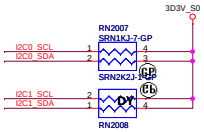
PCH Prim

071.SKYLA.000U





Add 1Mohm dummy resistor to KB_Disable 20150707



(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.

(PDG#543016) If the UART/GPIO functionality is also not used, the signals can be left as no-connect.

<Core Design>

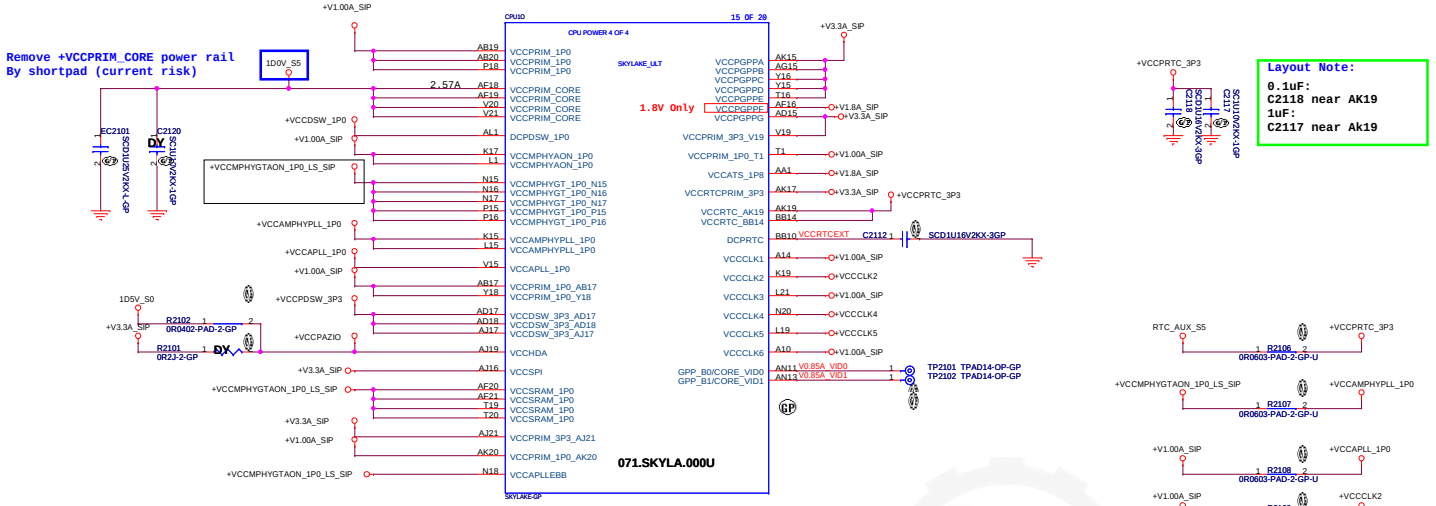
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (LPSS/ISH)

Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

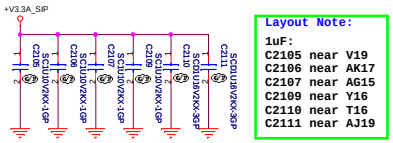
Date: Tuesday, July 21, 2015 | Sheet 20 of 105

Main Func = PCH



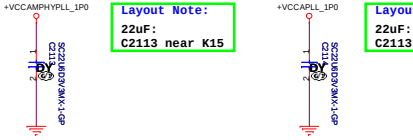
Layout Note:
0.1uF:
C2118 near AK19
1uF:
C2117 near Ak19

Remove +VCCPRIM_CORE power rail
By shortpad (current risk)



Layout Note:
1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

Layout Note:
1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1



Layout Note:
22uF:
C2113 near K15

Layout Note:
22uF:
C2113 near K15

Layout Note:
1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

<Core Design>

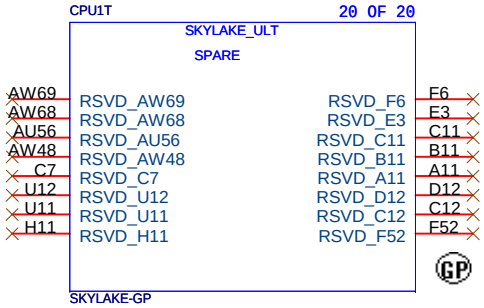
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Thursday, July 23, 2015 | Sheet 21 of 105

Main Func = PCH



071.SKYLA.000U

<Core Design>

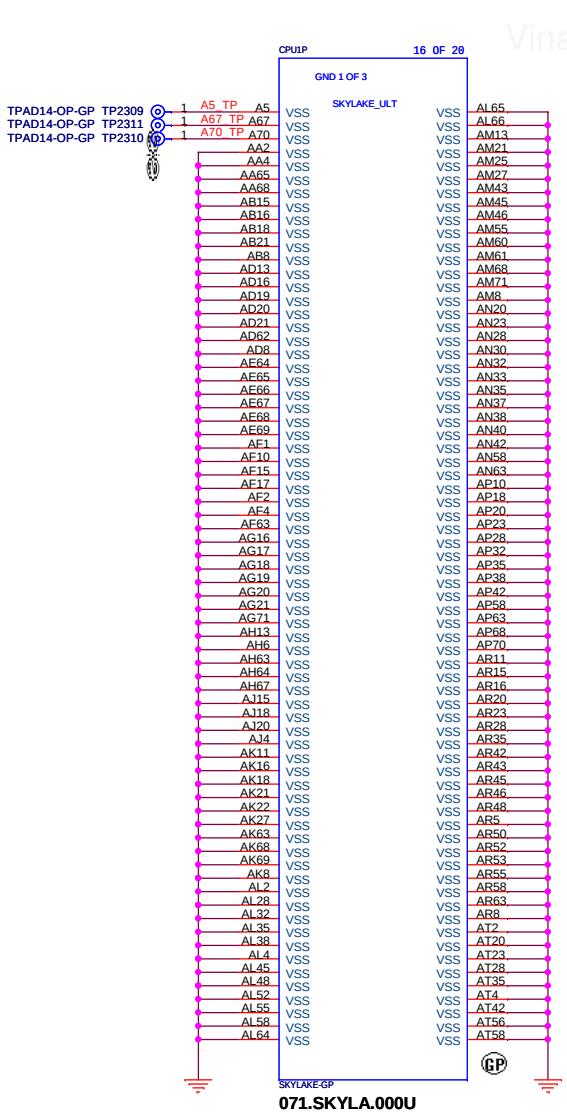
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

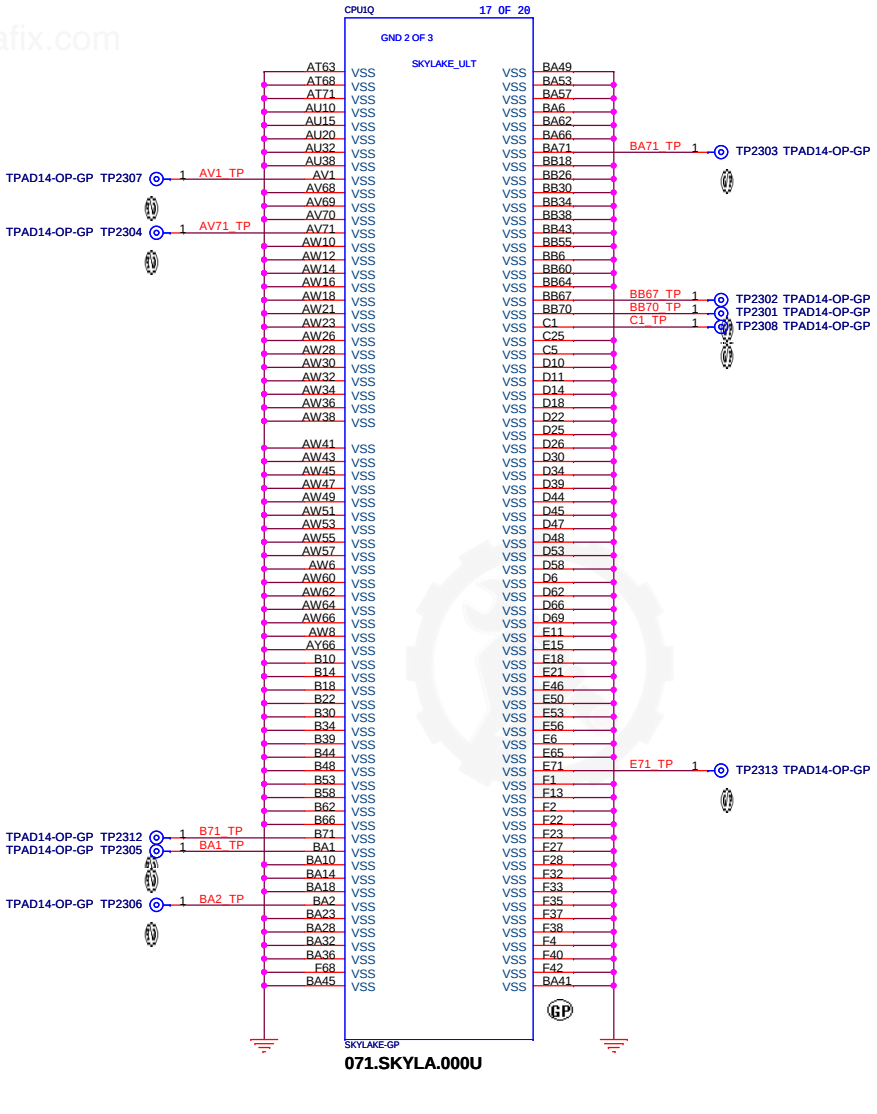
Title: ***CPU_(RSVD)***

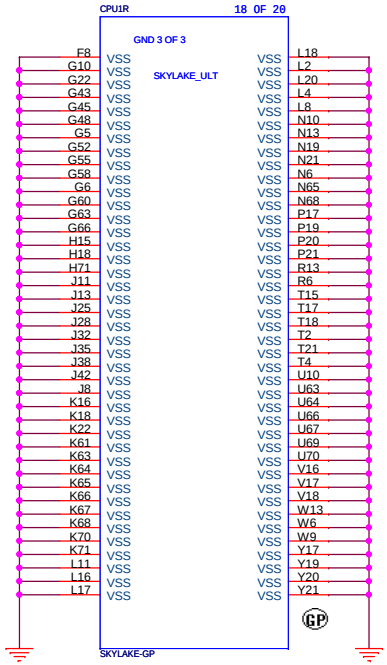
Size	Document Number	Rev
A4	***Cottonwood SKL-U***	***A00***

Date: Wednesday, July 08, 2015 Sheet 22 of 105

Main Func = PCH







Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Wednesday, July 08, 2015 | Sheet 23 of 105

Main Func = KBC

20140814 DAVID

BOARD_ID VERSION A/D	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
EVT (SA)	100.0K	10.0K	3.0V
DVT1 (SB)	100.0K	20.0K	2.75V
DVT2 (SC)	100.0K	33.0K	2.48V
DVT2 ST sensor	100.0K	47.0K	2.24V
Pilot (For ST)	100.0K	64.9K	2.0V
Pilot (For ISH)	100.0K	76.8K	1.87V
Pilot (For UHD ST)	100.0K	100.0K	1.65V
Pilot (For UHD ISH)	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

Layout Note:
Need very close to EC

Remove R2473 , 20141118

Layout Note:
Need very close to EC

Need very close to EC, PDG: <0.5 inches.

Reserve resistor, 20141118

Add Dummy resistor by work around 20150414
Change Dummy property from DY to DS3 20150416

Dummy R2422 & C2427
by EC control PCH_DPWROK
20150416

Move schematic, 20141118

Layout Note:
Need very close to EC
Need very close to EC

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

Change symbol part number, because origin symbol is DELL OBS part

Reserve VOL up/down 3D3V_S5 & 3D3V_S0 path
20150423

Reserve NON DS3 function 20150413

Change symbol part number, because origin symbol is DELL OBS part 20150116 2040

Power Switch Logic(PSL)

X00_0804

ALL_SYS_PWRGD assert,
delay 10ms; PCH_PWROK assert.

MEC1404	071.01404.000E
82.30003.0131	20.K0691.006
83.R2004.G8F	84.2N702.I31
84.2N702.A3F	84.DMN56.03F

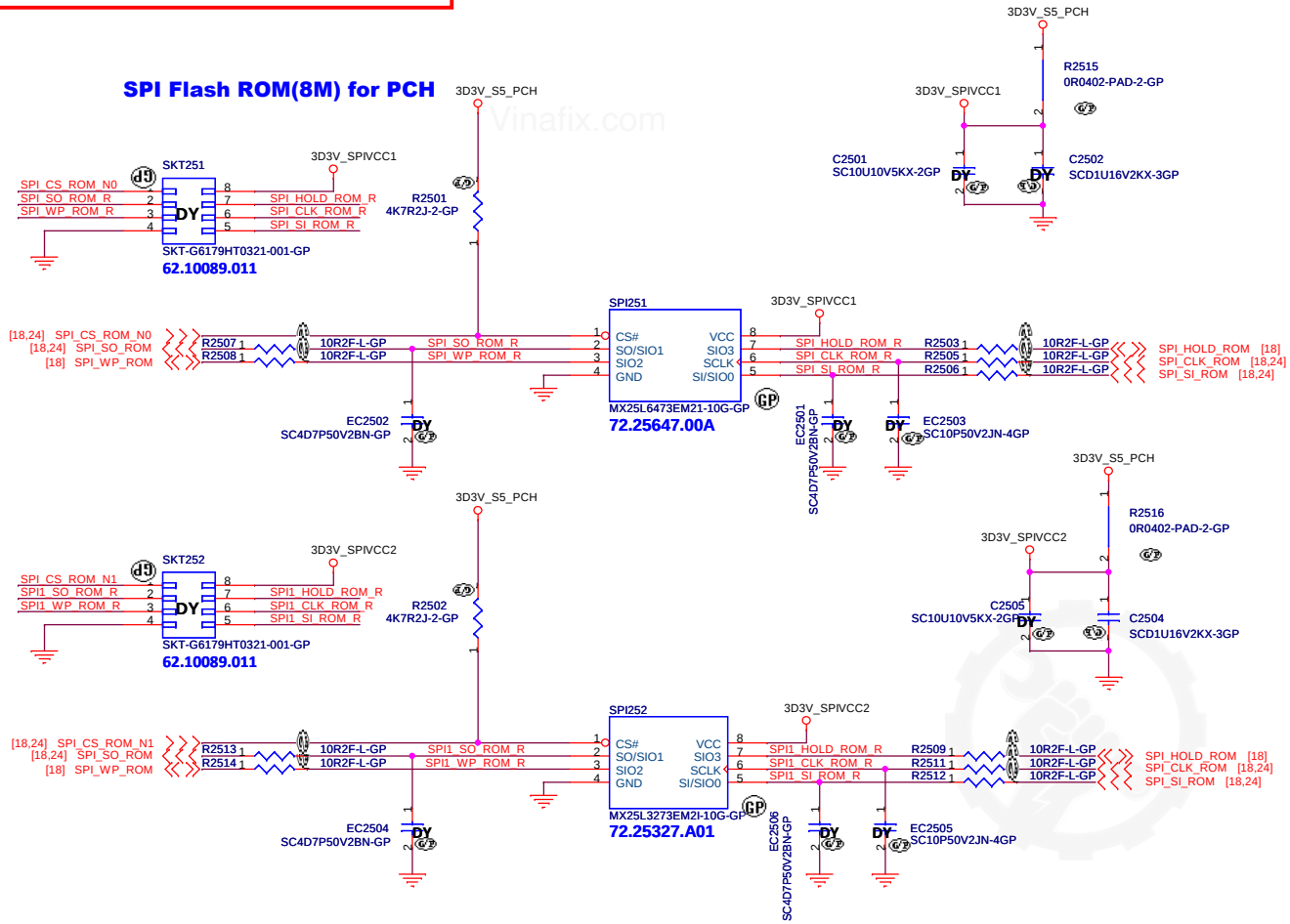
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

KBC Nuvoton NPCE285PA0DX

Size: A1 | Document Number: Cottonwood SKL-U | Rev: A00

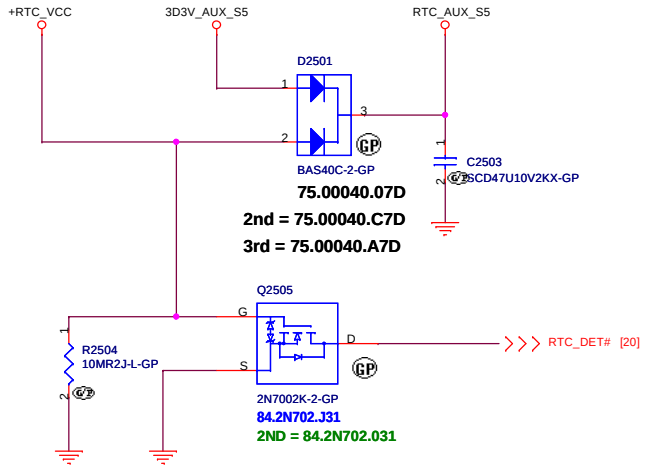
Date: Thursday, July 23, 2015 | Sheet 24 of 105

Main Func = SPI Flash



Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25Q64.K01	O	O	O
72.25647.00A	O	O	O
072.25B64.0001	O	O	O

Main Func = RTC



<Core Design>

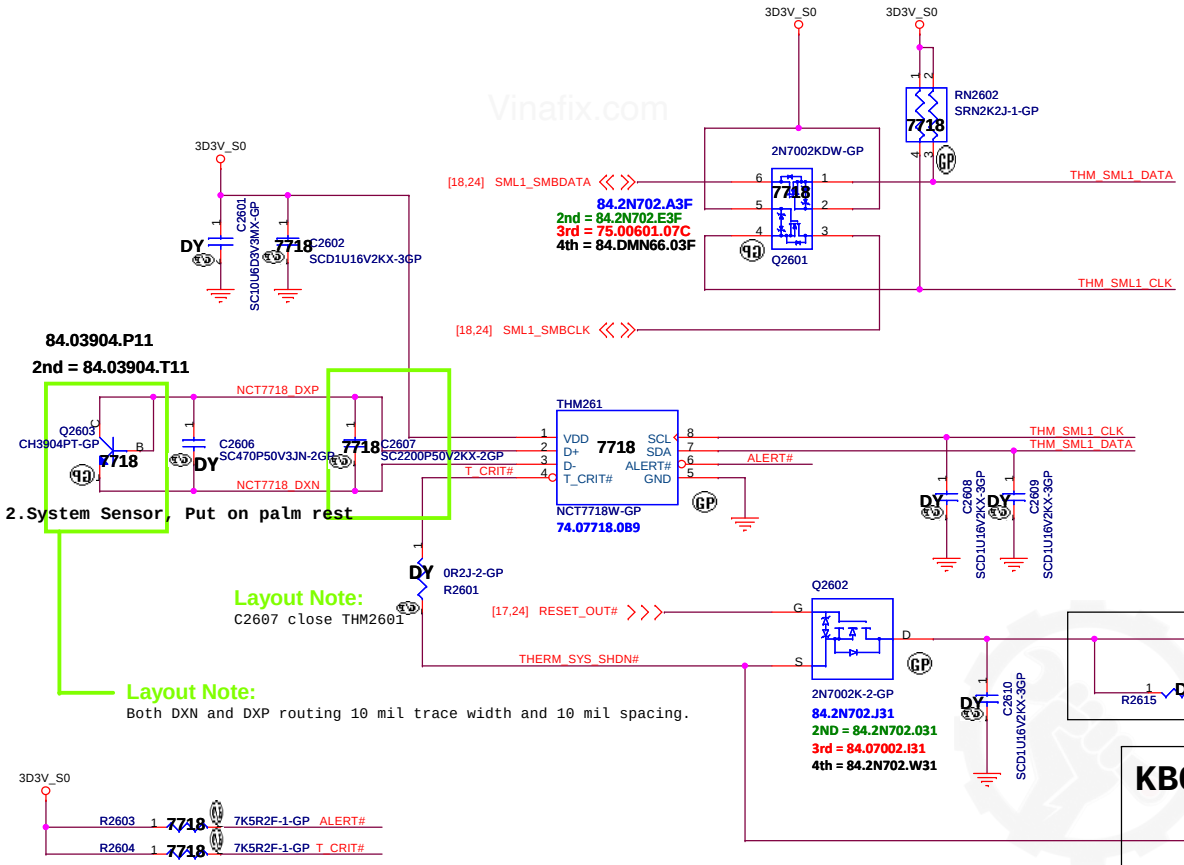
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC

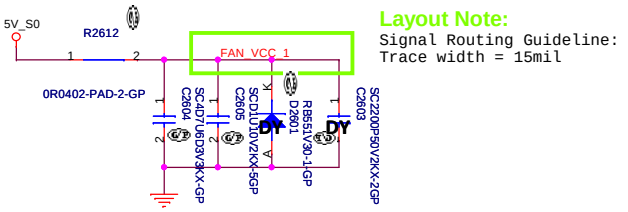
Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

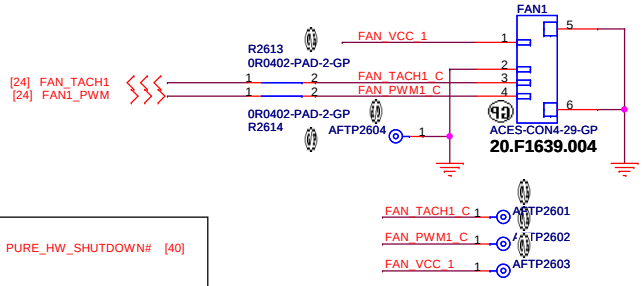
Date: Tuesday, July 21, 2015 | Sheet 25 of 105

Main Func = Thermal Sensor

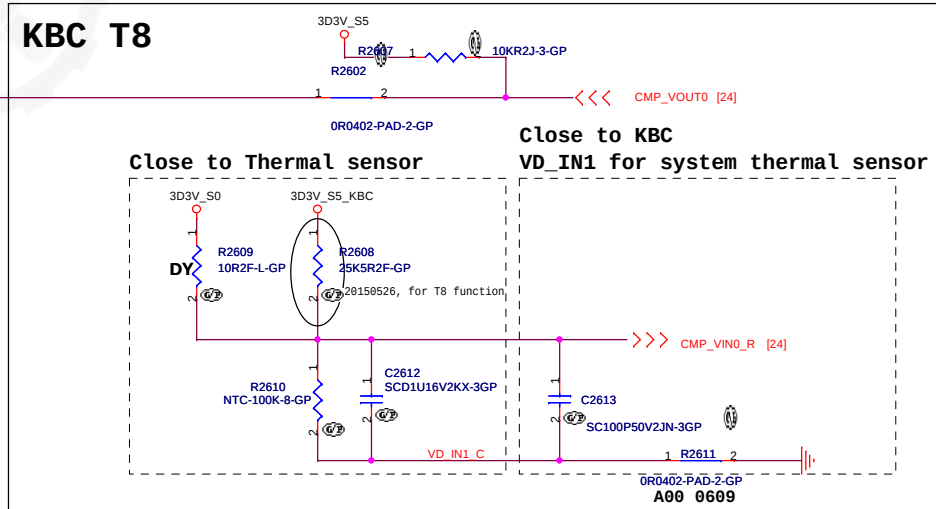


PWM FAN1





KBC T8



TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

<Core Design>

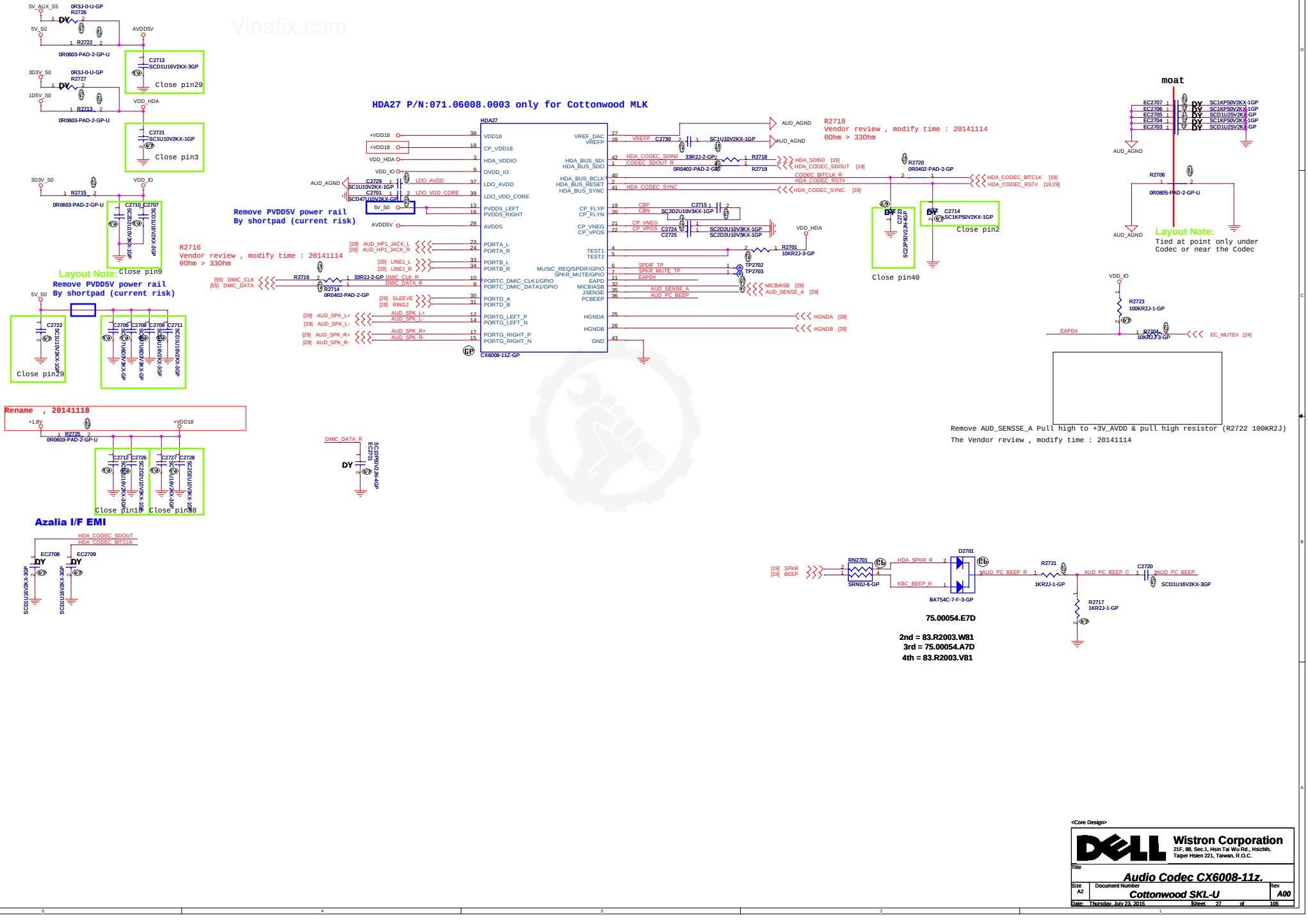
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Thursday, July 09, 2015 | Sheet 26 of 105

Main Func = Audio



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec CX6008-11z.

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Thursday, July 23, 2015 Sheet 27 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

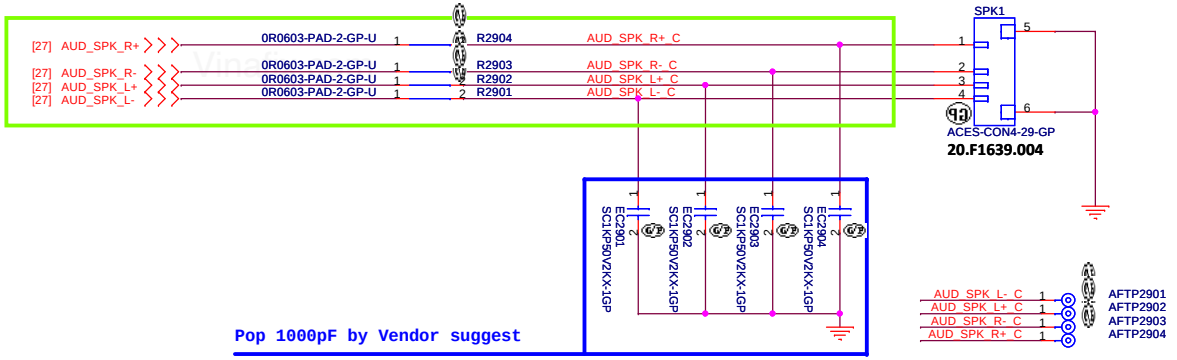
Size	Document Number	Rev
A1	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 28 of 105

Main Func = Audio

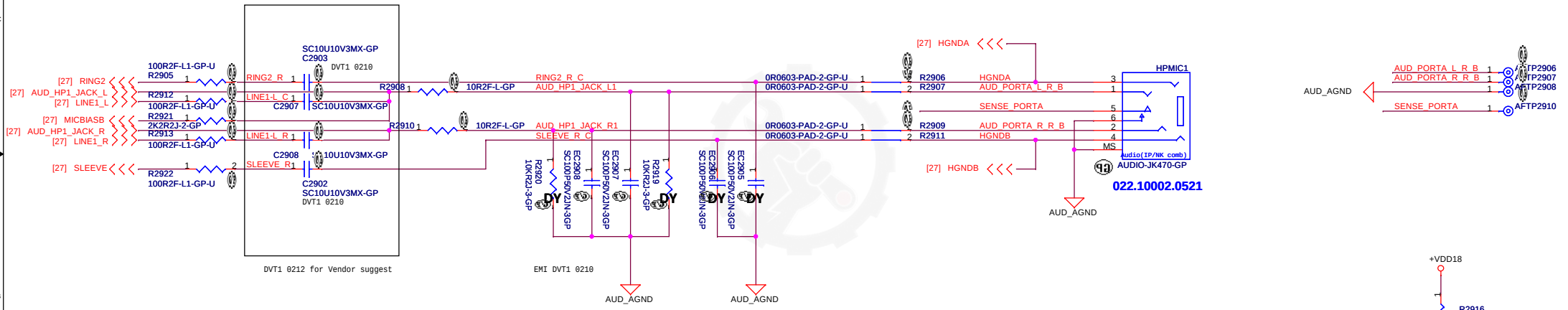
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

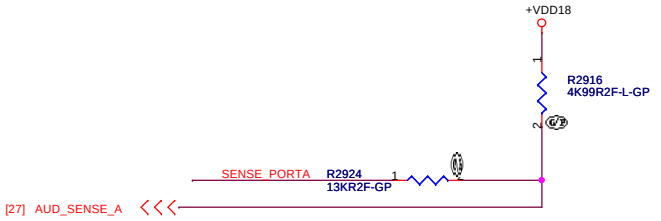
Speaker

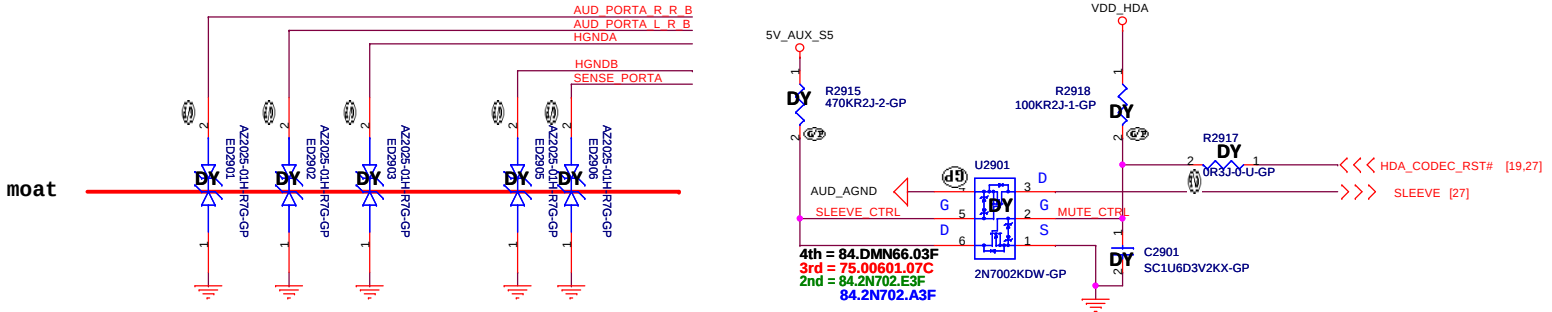


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

Combo Jack







<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio IO**

Size: A3 | Document Number: **Cottonwood SKL-U** | Rev: **A00**

Date: Wednesday, July 08, 2015 | Sheet 29 of 105

Main Func = Audio

(Blanking)

<Core Design>

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Title

(Reserved)

Size	Document Number	Rev
A4	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 30 of 105

Main Func = LAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8106

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 31 of 105

Main Func = LAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *XFOM&RJ45*

Size	Document Number	Rev
A3	*Cottonwood SKL-U*	*A00*

Date: Wednesday, July 08, 2015 Sheet 32 of 105

Main Func = Card Reader

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

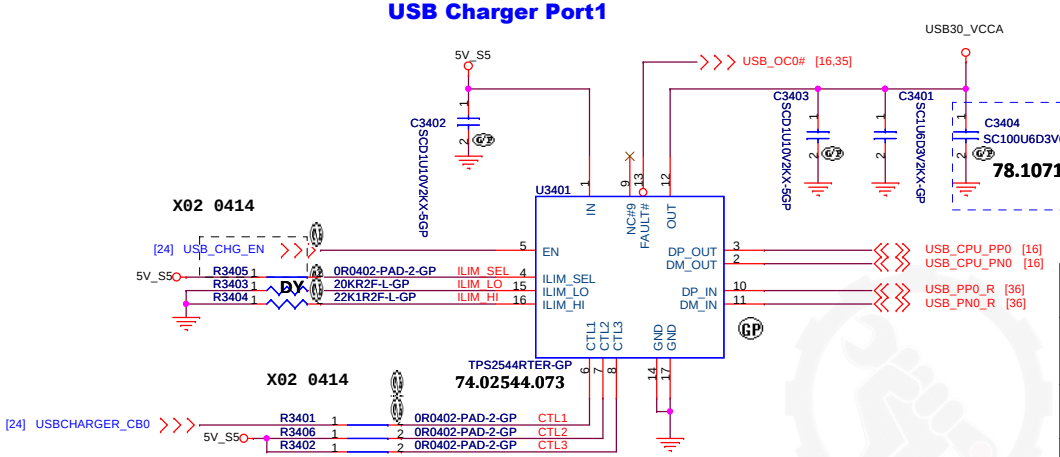
Title: Card Reader-RTS5170

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 33 of 105

Main Func = USB3.0 Port1

USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

<Core Design>

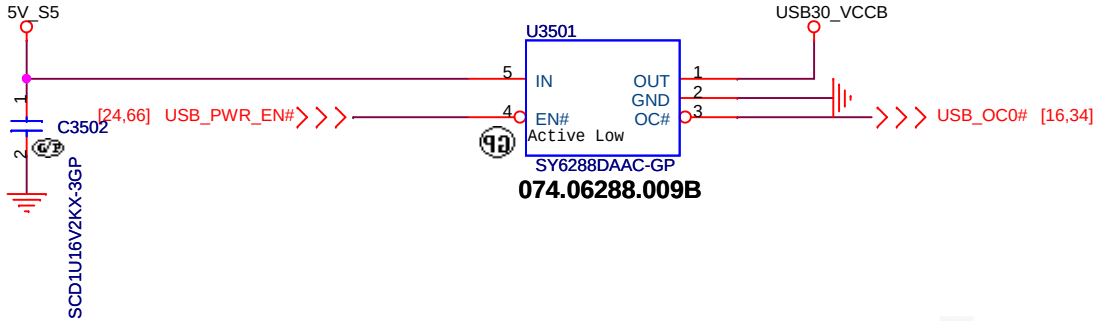
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

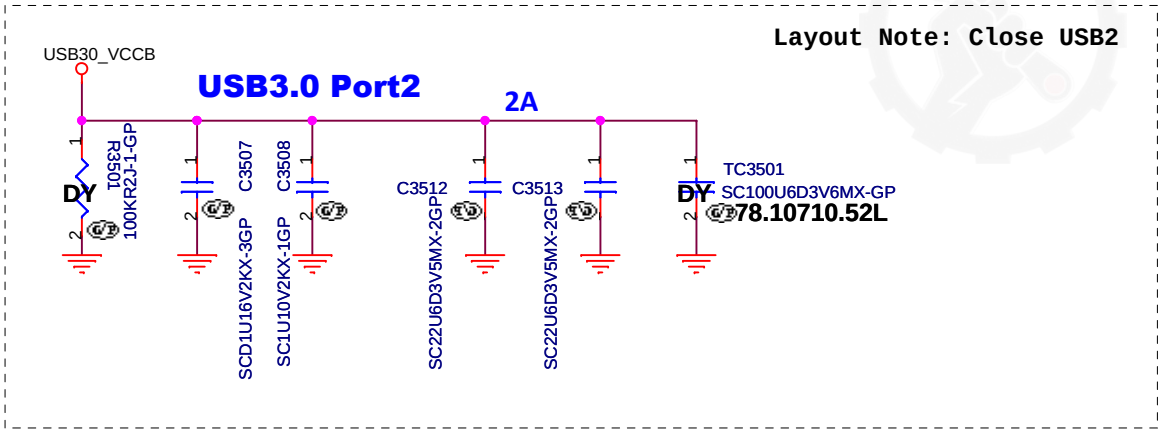
Title: (Reserved)

Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Wednesday, July 08, 2015 | Sheet 34 of 105

Main Func = USB3.0 Port1





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB switch

Size	Document Number	Rev
	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 35 of 105

Main Func = USB3.0 Port1

USB3.0 Port1

[16] USB30_TX_CPU_N1 → C3601 SCD1U10V2KX-5GP → USB30_TXDN1_R → R3605 0R0402-PAD-2-GP → USB30_TXDN1_C

Remove CMC TR3601 by A00 version

[16] USB30_TX_CPU_P1 → C3602 SCD1U10V2KX-5GP → USB30_TXDP1_R → R3606 0R0402-PAD-2-GP → USB30_TXDP1_C

[16] USB30_RX_CPU_N1 → R3609 0R0402-PAD-2-GP → USB30_RXDN1_C

Remove CMC TR3605 by A00 version

[16] USB30_RX_CPU_P1 → R3610 0R0402-PAD-2-GP → USB30_RXDP1_C

[34] USB_PP0_R / [34] USB_PN0_R → DLP11SN900HL2L-GP TR3602 → USB20_DP0_C / USB20_DN0_C

Remove 0Ohm pad R3607,R3608 by A00 version

USB2.0 Port2 and USB2.0 Port3 are on IOBD

EU3601 ESD3V3U4ULC-GP
USB30_RXDN1_C / USB30_RXDP1_C / USB30_TXDN1_C / USB30_TXDP1_C
83.3V3U4.0A0

EU3602 AZC099-04S-1-GP
USB20_DN0_C / USB20_DP0_C
USB30_VCCA
75.09904.07C
2nd = 75.02304.07C

EMI for DVT1 0212

USB30_VCCA

USB1 SKT-USB14-5-GP-U
VBUS, D-, D+, SSRX-, SSRX+, SSTX-, SSTX+, GND_DRAIN, DET#, GND, CHASSIS#11–14
USB20_DN0_C / USB20_DP0_C / USB30_RXDN1_C / USB30_RXDP1_C / USB30_TXDN1_C / USB30_TXDP1_C
USBDET_CON# [24]
022.10005.0441

USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB3.0 Port2

[16] USB30_TX_CPU_N2 → C3603 SCD1U10V2KX-5GP → USB30_TXDN2_R → R3611 0R0402-PAD-2-GP → USB30_TXDN2_C

Remove CMC TR3604 by A00 version

[16] USB30_TX_CPU_P2 → C3604 SCD1U10V2KX-5GP → USB30_TXDP2_R → R3614 0R0402-PAD-2-GP → USB30_TXDP2_C

[16] USB30_RX_CPU_N2 → R3612 0R0402-PAD-2-GP → USB30_RXDN2_C

Remove CMC TR3606 by A00 version

[16] USB30_RX_CPU_P2 → R3613 0R0402-PAD-2-GP → USB30_RXDP2_C

[16] USB_CPU_PP1 / [16] USB_CPU_PN1 → DLP11SN900HL2L-GP TR3603 → USB20_DP1_C / USB20_DN1_C

Remove 0Ohm pad R3615,R3616 by A00 version

EU3603 ESD3V3U4ULC-GP
USB30_RXDN2_C / USB30_RXDP2_C / USB30_TXDN2_C / USB30_TXDP2_C
83.3V3U4.0A0

EU3604 AZC099-04S-1-GP
USB20_DN1_C / USB20_DP1_C
USB30_VCCB
75.09904.07C
2nd = 75.02304.07C

EMI for DVT1 0212

USB30_VCCB

USB2 SKT-USB13-90-GP-U
USB30_TXDP2_C / USB30_TXDN2_C / USB20_DN1_C / USB20_DP1_C / USB30_RXDP2_C / USB30_RXDN2_C

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30
Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00
Date: Thursday, July 09, 2015 | Sheet 36 of 105

Main Func = USB2.0

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB20*

Size: A3 | Document Number: *Cottonwood SKL-U* | Rev: *A00*

Date: Wednesday, July 08, 2015 | Sheet 37 of 105

Main Func = USB3.0 Port1

(Blanking)

<Core Design>

Wistron Corporation
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Title

(Reserved)

Size	Document Number	Rev
A4	*Cottonwood SKL-U*	*A00*

Date: Wednesday, July 08, 2015 Sheet 38 of 105

Main Func = USB3.0 Port1

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

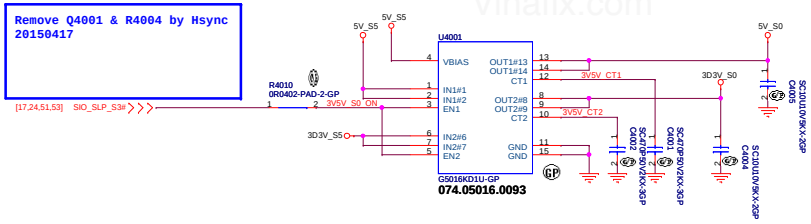
Size	Document Number	Rev
A4	*Cottonwood SKL-U*	*A00*

Date: Wednesday, July 08, 2015 Sheet 39 of 105

Main Func = Power Plane & Sequence

ROSA Run Power

Remove Q4001 & R4004 by Hsync
20150417



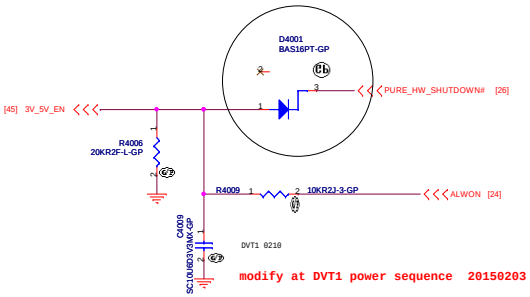
5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

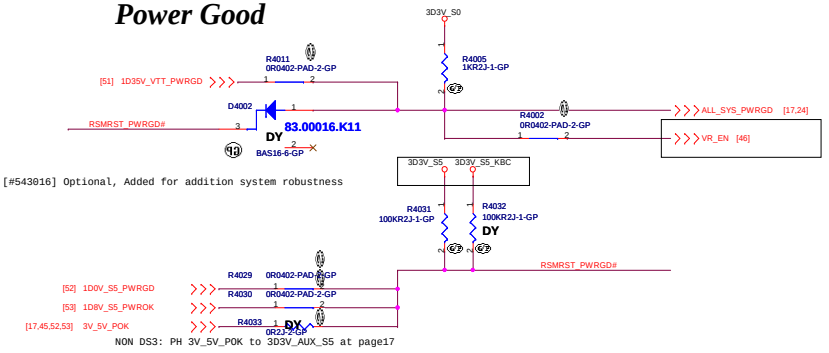
Change to Diode 20150402



modify at DVT1 power sequence 20150203

20150116 2032

Power Good

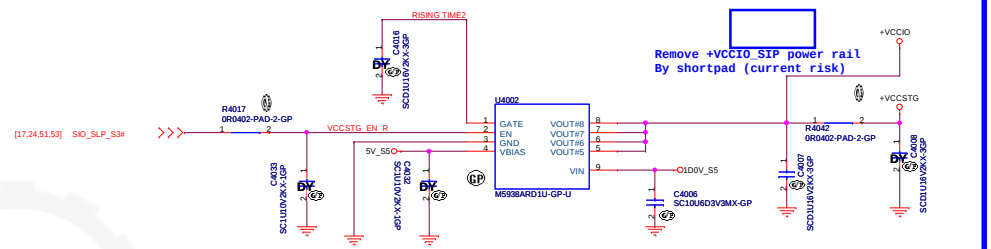


[#543016] Optional, Added for addition system robustness

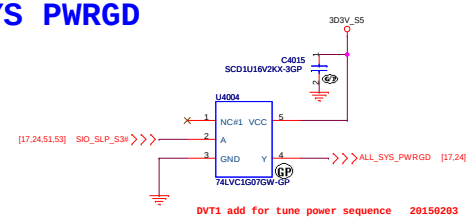
NON DS3: PH 3V_5V_POK to 3D3V_AUX_S5 at page17

VCCIO and VCCSTG

Modify power switch IC and relate schematic ,DVT2 20150407



ALL SYS PWRGD

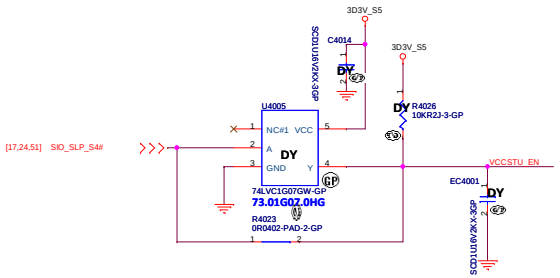


DVT1 add for tune power sequence 20150203

V1.8A

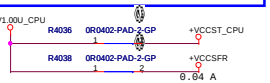
+VCCIO(ICCMAX = 2.73A)

MANAGEMENT RAIL POWER GENERATION

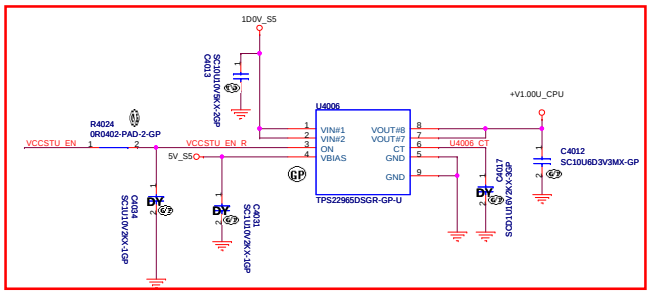


VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

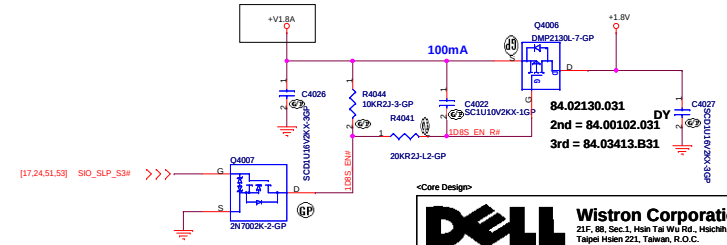
VCCST



Modify power switch IC and relate schematic ,DVT1 20150204



+1.8V for codec



<Core Design>

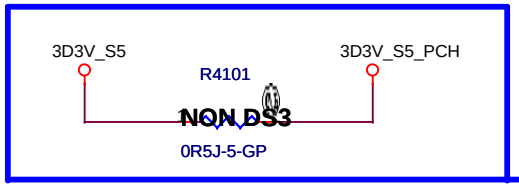
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

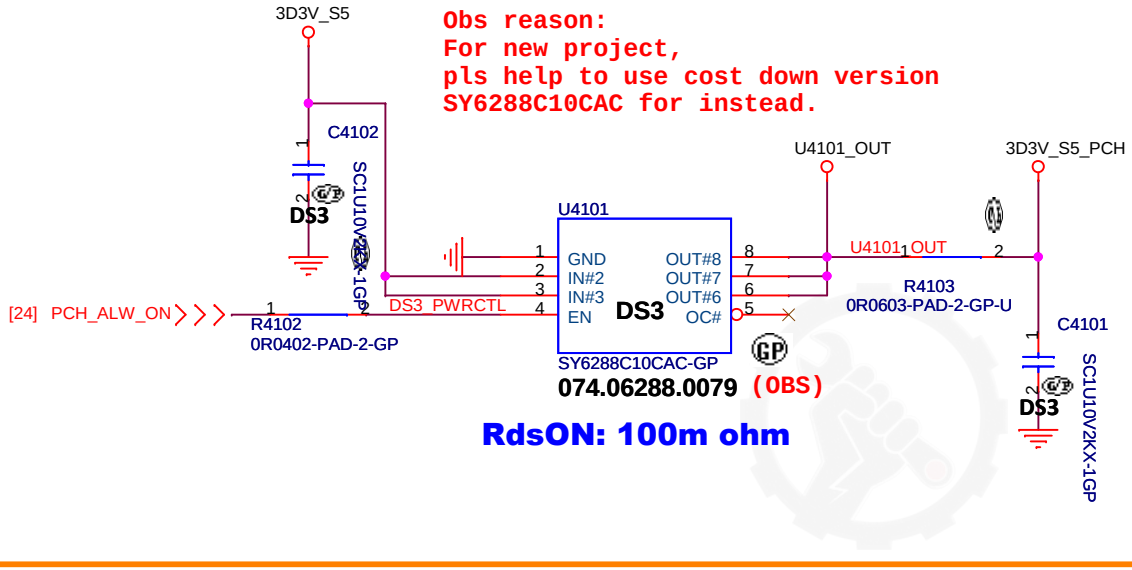
Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Thursday, July 23, 2015 | Sheet 40 of 105

Main Func = Power Plane & Sequence



Reserve by NON DS3 function 20150413



DS3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Connected_Standby(1/2)+DS3	
Size A4	Document Number Cottonwood SKL-U	Rev A00
Date: Thursday, July 09, 2015	Sheet 41 of 105	

Main Func = DIMM1
Main Func = DIMM2

VREF CIRCUITRY

SA_DIMM_VREFDQ

DIMM1

M_VREF_CA_DIMMA

DDR_VREF_S3

R4204
0R2J-2-GP
DY

Layout Note:
Place Close DIMMs

1D35V_S3

R4206
1K8R2F-GP

2R2F-GP
R4208

V_SM_VREF_CNT [5]

C4201
SCD022U16V2KX-3GP

+V_VREF_PATH3

R4207
24D9R2F-L-GP

R4203
1K8R2F-GP

[5] M_VREF_DQ_DIM0

Layout Note:
Place Close DIMM1

DDR_VREF_S3

R4210
0R2J-2-GP
DY

1D35V_S3

R4201
1K8R2F-GP

R4202
2R2F-GP

M_VREF_DQ_DIMMA

C420
SCD022U16V2KX-3GP

+V_VREF_PATH1

R4211
24D9R2F-L-GP

R4209
1K8R2F-GP

<Core Design>

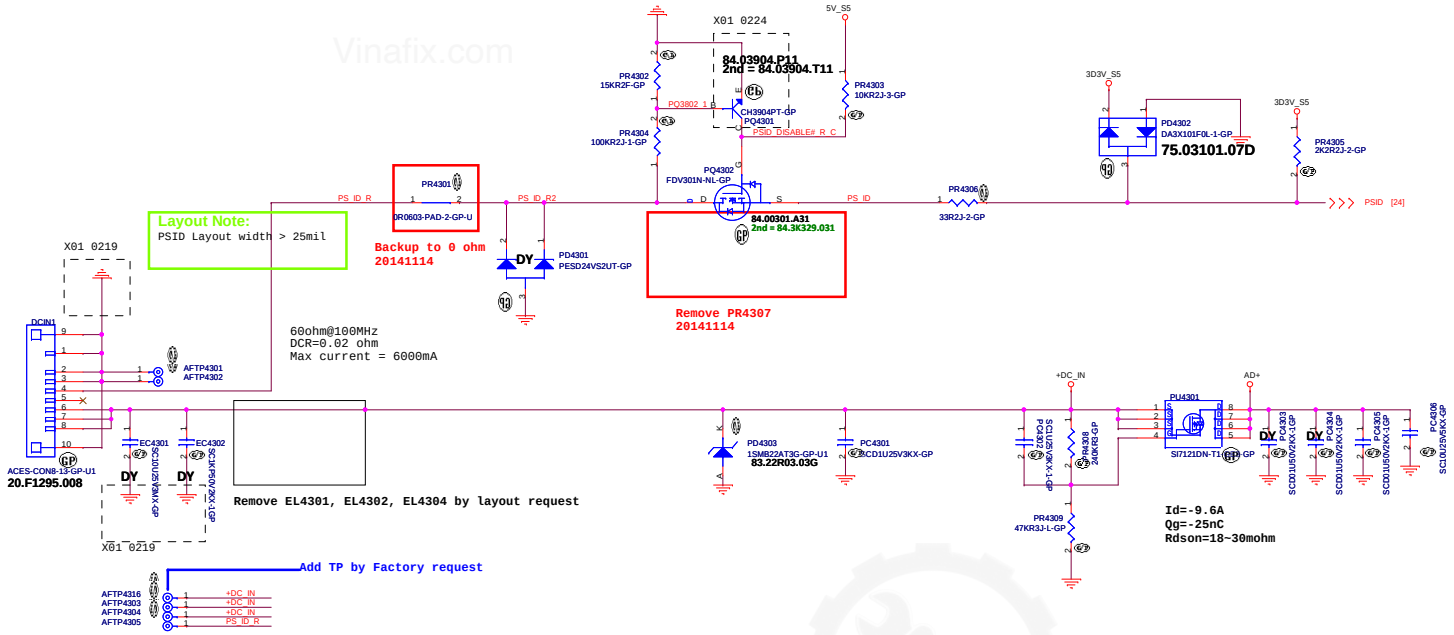
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Connected_Standby(2/2)

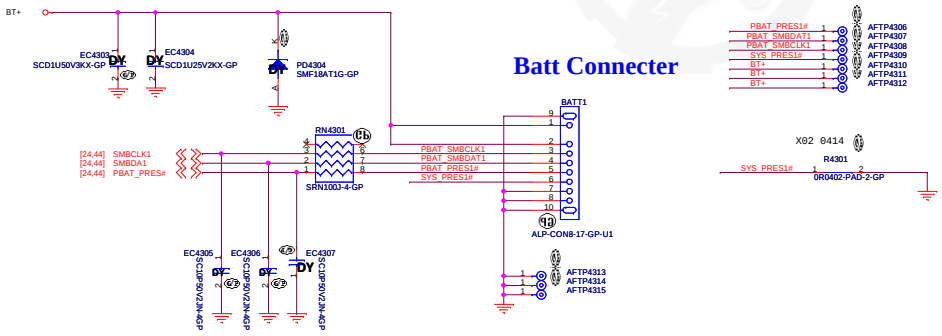
Size: A3
Document Number: Cottonwood SKL-U
Rev: A00

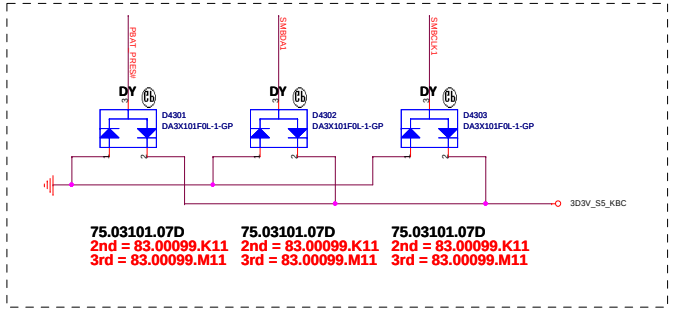
Date: Wednesday, July 08, 2015
Sheet 42 of 105

Main Func = ADT Input



Main Func = BAT Input





75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

75.03101.07D
2nd = 83.00099.K11
3rd = 83.00099.M11

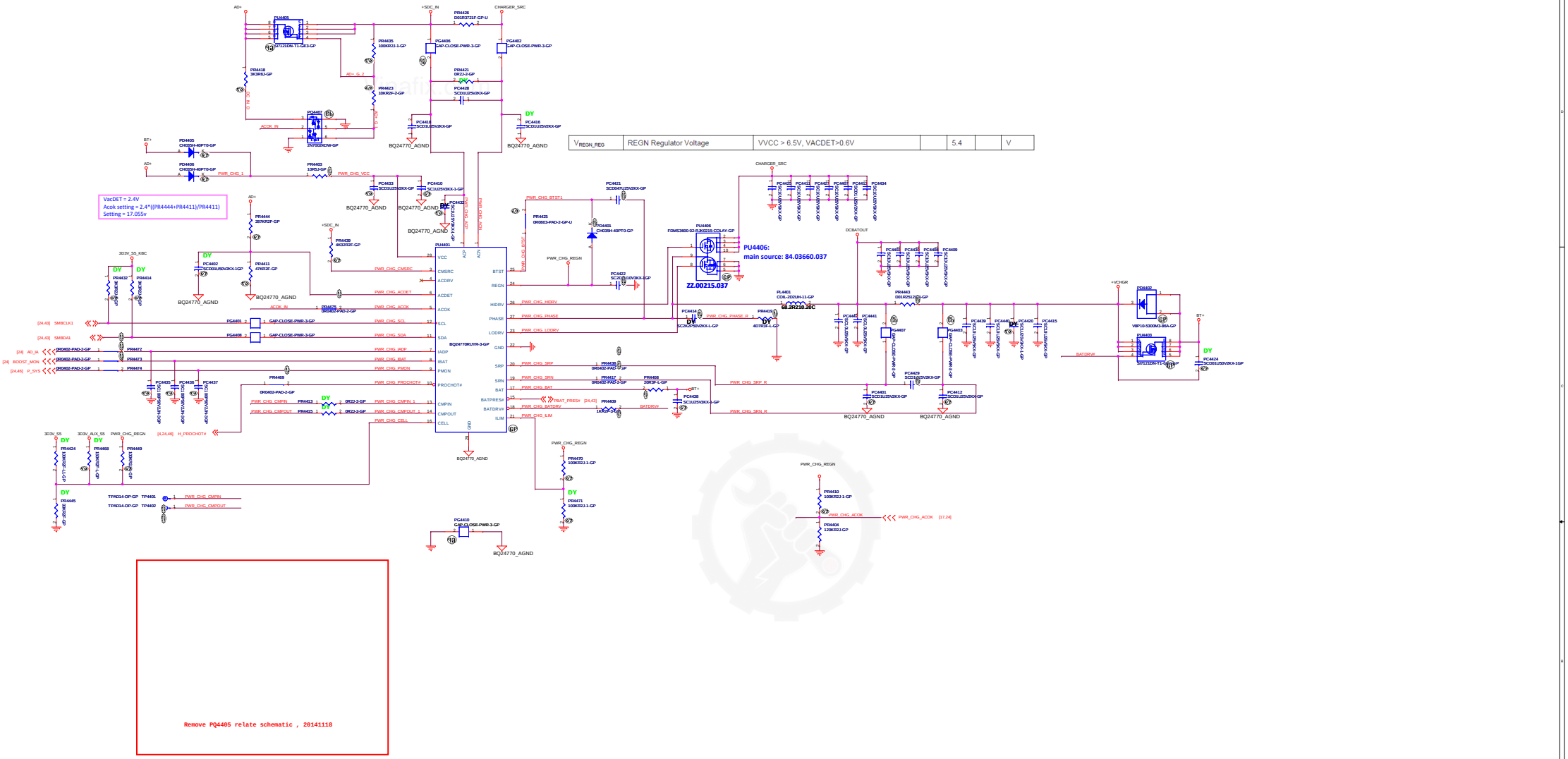
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 43 of 105



V_{REGN_REG}	REGN Regulator Voltage	VVCC > 6.5V, VACDET>0.6V		5.4		V

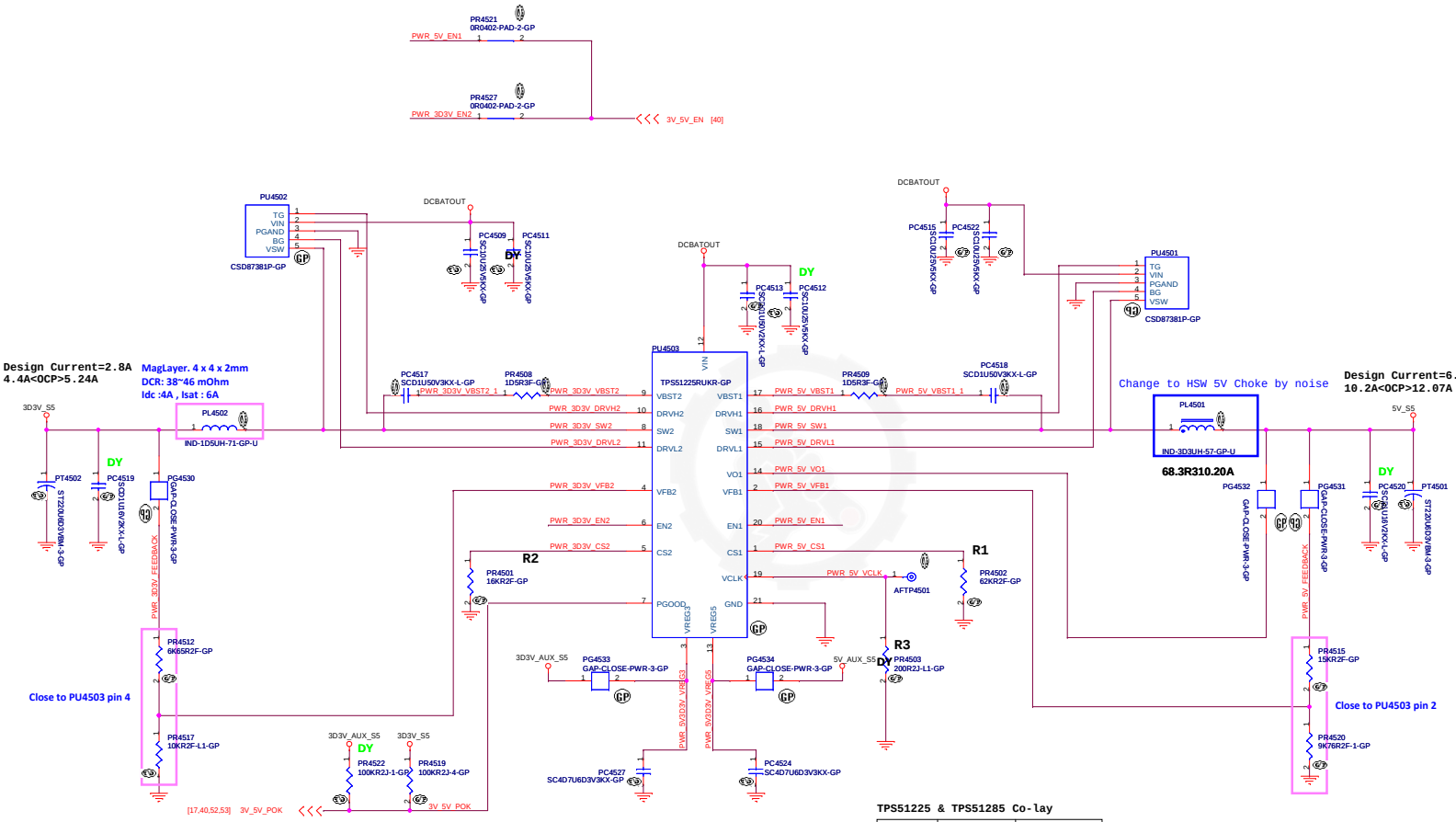
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

File: CHARGER

Size	Document Number	Rev
A1	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 44 of 105



TPS51225 & TPS51285 Co-lay

	TPS51225	TPS51285
R1	100K	20K
R2	64.9K	13K
R3	DY	200

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC-3D3V&5V

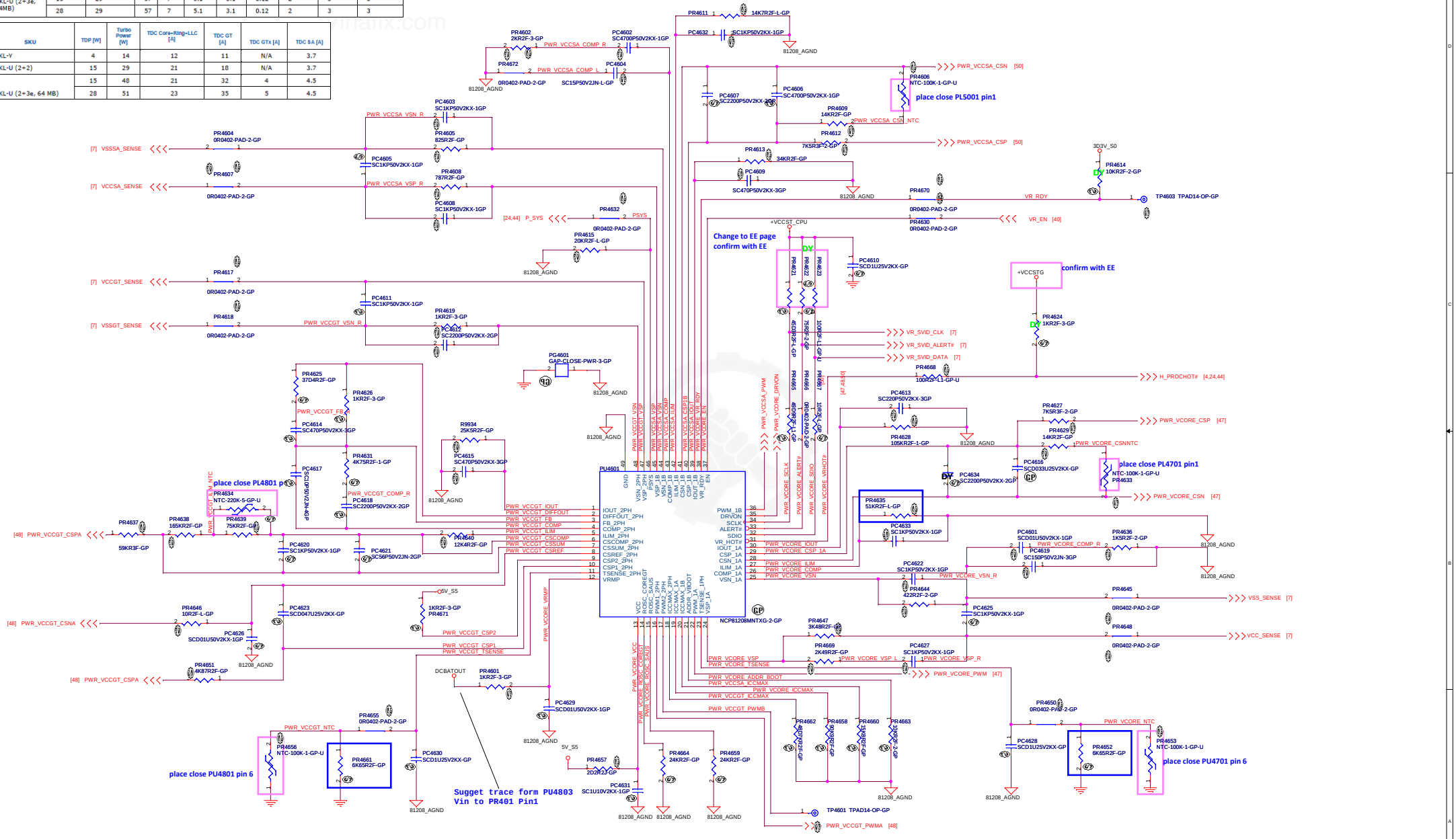
Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Thursday, July 23, 2015 Sheet 45 of 105

Main Func = CPU_CORE

SKU	TDP[W]	Core+Ring +LLC	GT	GTx	SA	VCCIO	VCCST	VCCDDQ	VCCOPC	VCCEOPIO
SKL-Y(2+2)	4	16	20	N/A	4.1	3	0.1	2	N/A	N/A
SKL-U (2+2)	15	28	31	N/A	4.5	3	0.075	2	NA	N/A
SKL-U (2+3e, 64MB)	15	29	57	7	5.1	3.1	0.12	2	3	3
	28	29	57	7	5.1	3.1	0.12	2	3	3

SKU	TDP [W]	Turbo Power [W]	TDC Core+Ring+LLC [A]	TDC GT [A]	TDC GTx [A]	TDC SA [A]
SKL-Y	4	14	12	11	N/A	3.7
SKL-U (2+2)	15	29	21	18	N/A	3.7
	15	48	21	32	4	4.5
SKL-U (2+3e, 64 MB)	28	51	23	35	5	4.5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81208MN_CPU_VCORE(1/3)

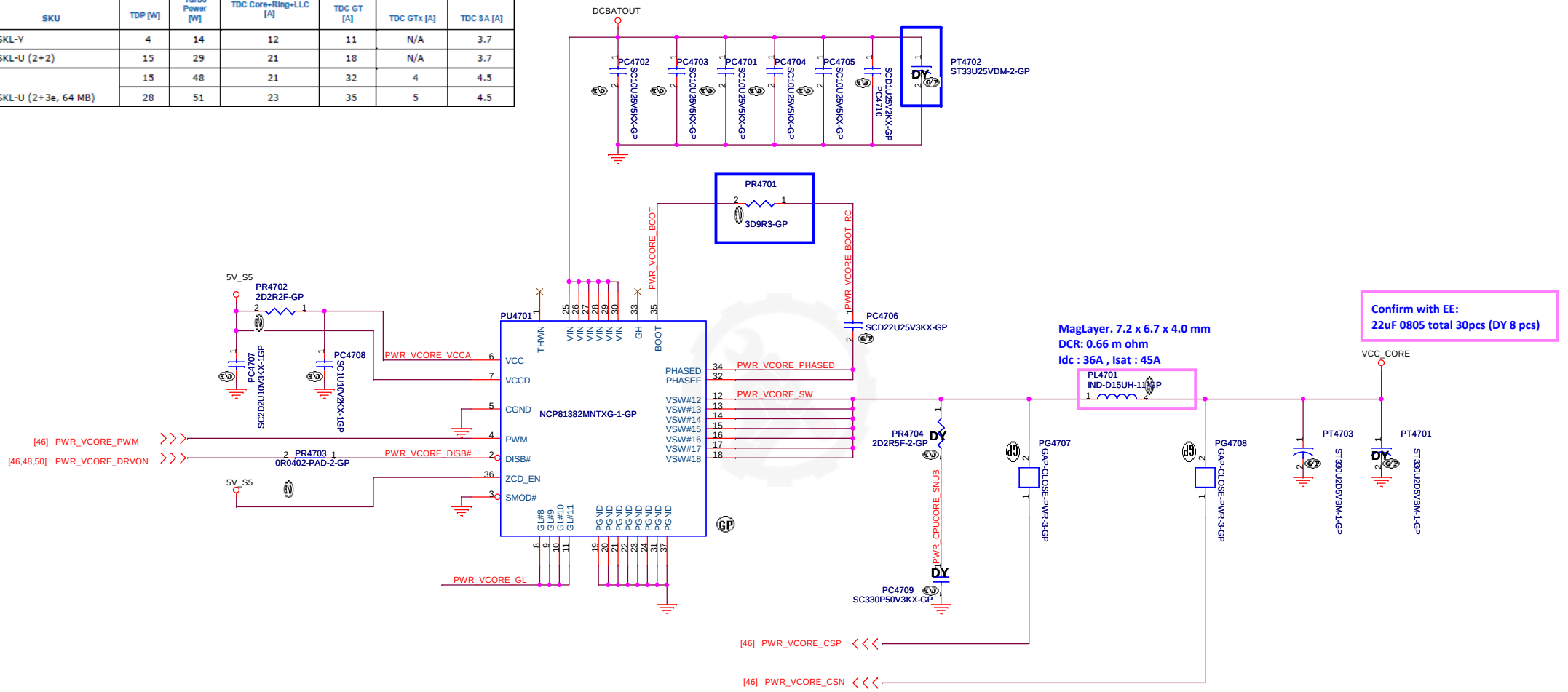
Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Thursday, July 23, 2015 | Sheet 46 of 105

Main Func = CPU_CORE

SKU	TDP[W]	Core+Ring +LLC	GT	GTx	SA	VCCIO	VCCST	VCCDDQ	VCCOPC	VCCEOPIO
SKL-Y(2+2)	4	16	20	N/A	4.1	3	0.1	2	N/A	N/A
SKL-U (2+2)	15	28	31	N/A	4.5	3	0.075	2	NA	N/A
SKL-U (2+3e, 64MB)	15	29	57	7	5.1	3.1	0.12	2	3	3
	28	29	57	7	5.1	3.1	0.12	2	3	3

SKU	TDP [W]	Turbo Power [W]	TDC Core+Ring+LLC [A]	TDC GT [A]	TDC GTx [A]	TDC SA [A]
SKL-Y	4	14	12	11	N/A	3.7
SKL-U (2+2)	15	29	21	18	N/A	3.7
SKL-U (2+3e, 64 MB)	15	48	21	32	4	4.5
	28	51	23	35	5	4.5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCORE(2/3)

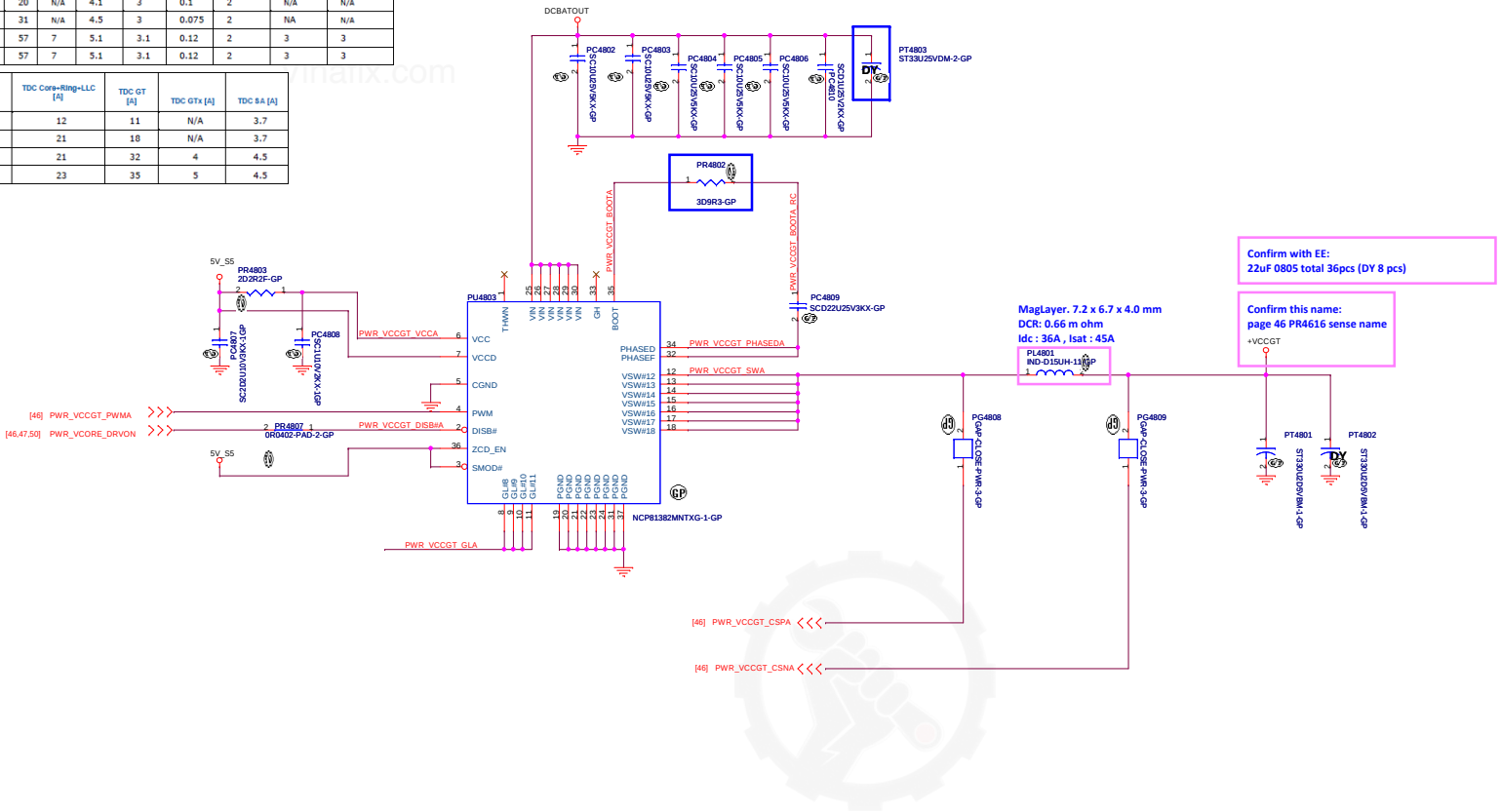
Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Thursday, July 23, 2015 | Sheet 47 of 105

Main Func = CPU_CORE

SKU	TDP[W]	Core+Ring +LLC	GT	GTx	SA	VCCIO	VCCST	VCCDDQ	VCCOPC	VCCEOPIO
SKL-Y(2+2)	4	16	20	N/A	4.1	3	0.1	2	N/A	N/A
SKL-U (2+2)	15	28	31	N/A	4.5	3	0.075	2	NA	N/A
SKL-U (2+3e, 64MB)	15	29	57	7	5.1	3.1	0.12	2	3	3
	28	29	57	7	5.1	3.1	0.12	2	3	3

SKU	TDP [W]	Turbo Power [W]	TDC Core+Ring+LLC [A]	TDC GT [A]	TDC GTx [A]	TDC SA [A]
SKL-Y	4	14	12	11	N/A	3.7
SKL-U (2+2)	15	29	21	18	N/A	3.7
	15	48	21	32	4	4.5
SKL-U (2+3e, 64 MB)	28	51	23	35	5	4.5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)

Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Thursday, July 23, 2015 | Sheet 48 of 105

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81210MN_CPU_VCCGTUS

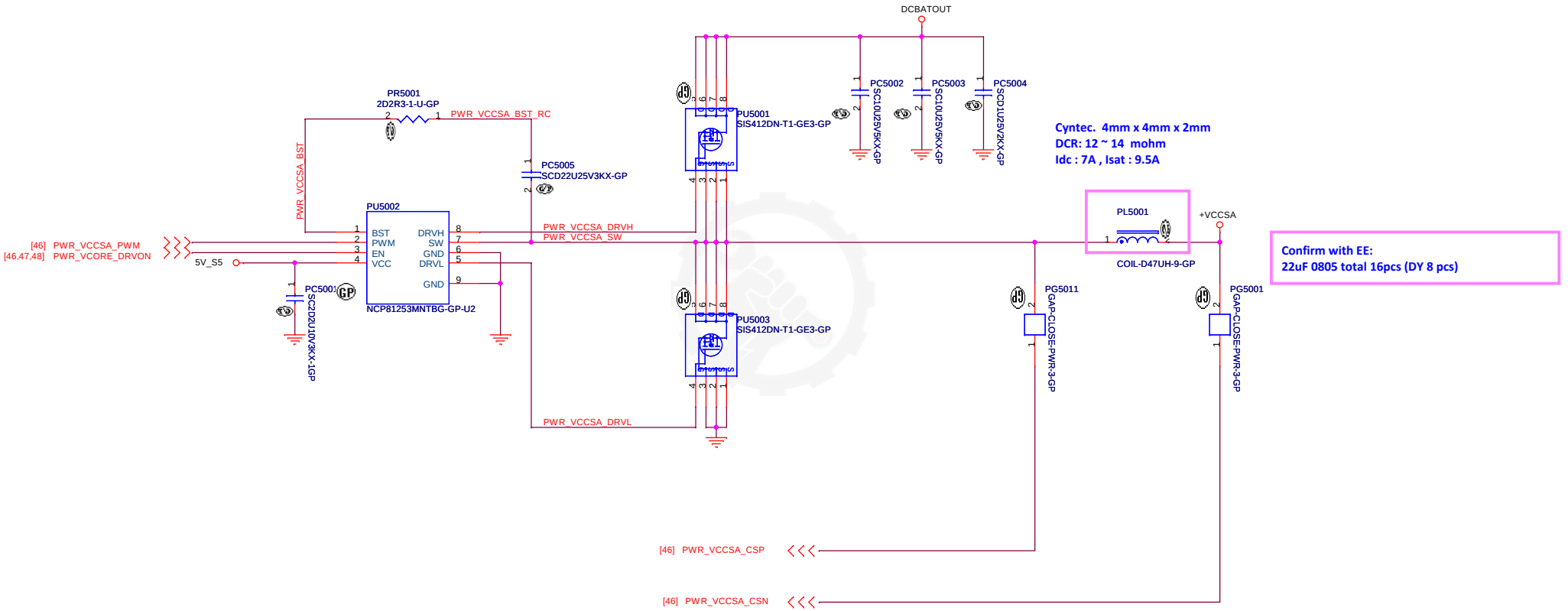
Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Wednesday, July 08, 2015 | Sheet 49 of 105

Main Func = CPU_CORE

SKU	TDP[W]	Core+Ring +LLC	GT	GTx	SA	VCCIO	VCCST	VCCDDQ	VCCOPC	VCCEOPIO
SKL-Y(2+2)	4	16	20	N/A	4.1	3	0.1	2	N/A	N/A
SKL-U (2+2)	15	28	31	N/A	4.5	3	0.075	2	NA	N/A
SKL-U (2+3e, 64MB)	15	29	57	7	5.1	3.1	0.12	2	3	3
	28	29	57	7	5.1	3.1	0.12	2	3	3

SKU	TDP [W]	Turbo Power [W]	TDC Core+Ring+LLC [A]	TDC GT [A]	TDC GTx [A]	TDC SA [A]
SKL-Y	4	14	12	11	N/A	3.7
SKL-U (2+2)	15	29	21	18	N/A	3.7
SKL-U (2+3e, 64 MB)	15	48	21	32	4	4.5
	28	51	23	35	5	4.5

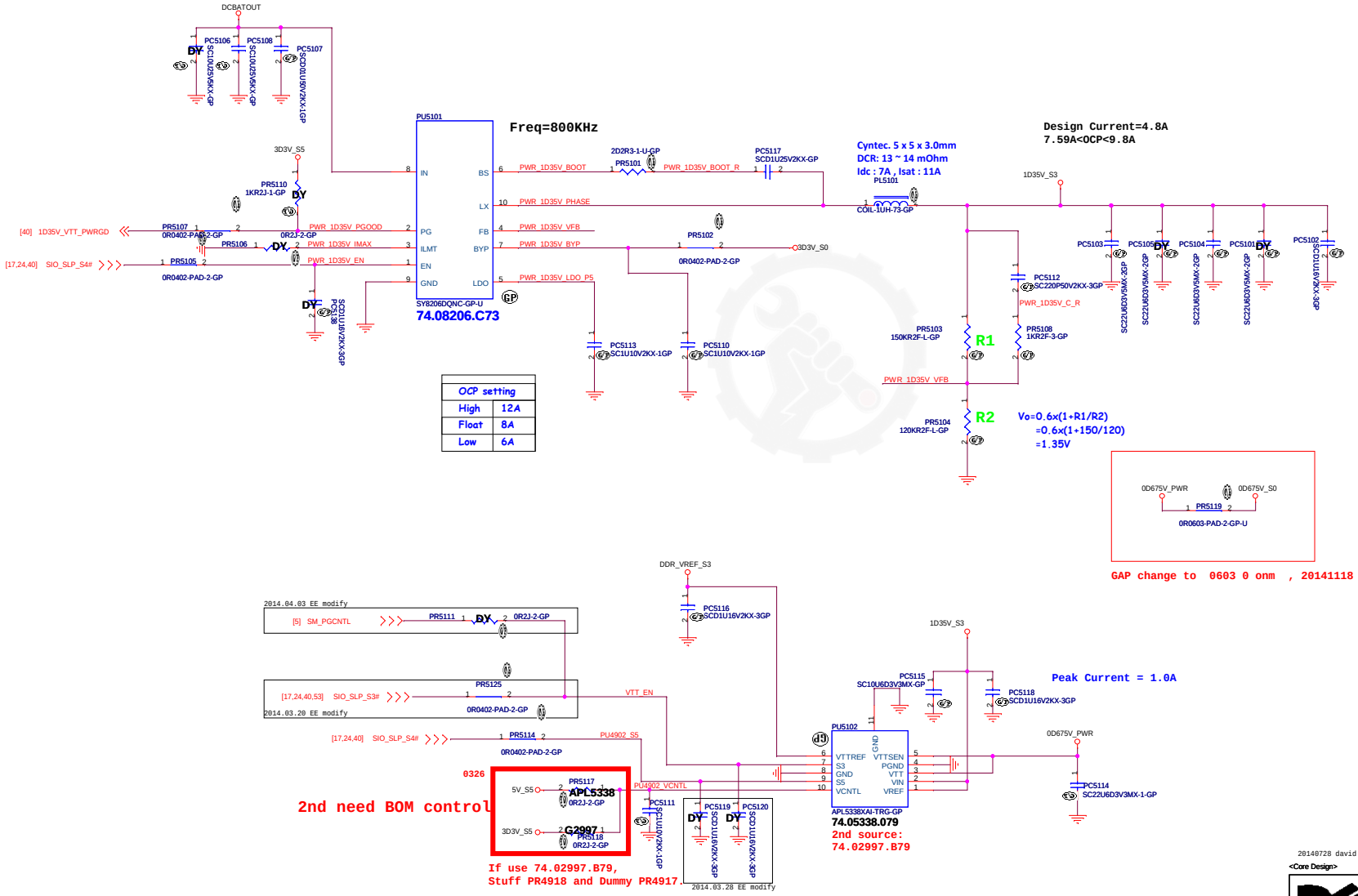


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
NCP81253MN_CPU_VCCSA		
Size: A3	Document Number: Cottonwood SKL-U	Rev: A00
Date: Tuesday, July 21, 2015	Sheet 50 of 105	

SY8206D for 1D35V



20140728 david

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEM&MEMVTT

Size: C | Document Number: Cottonwood SKL-U | Rev: A00

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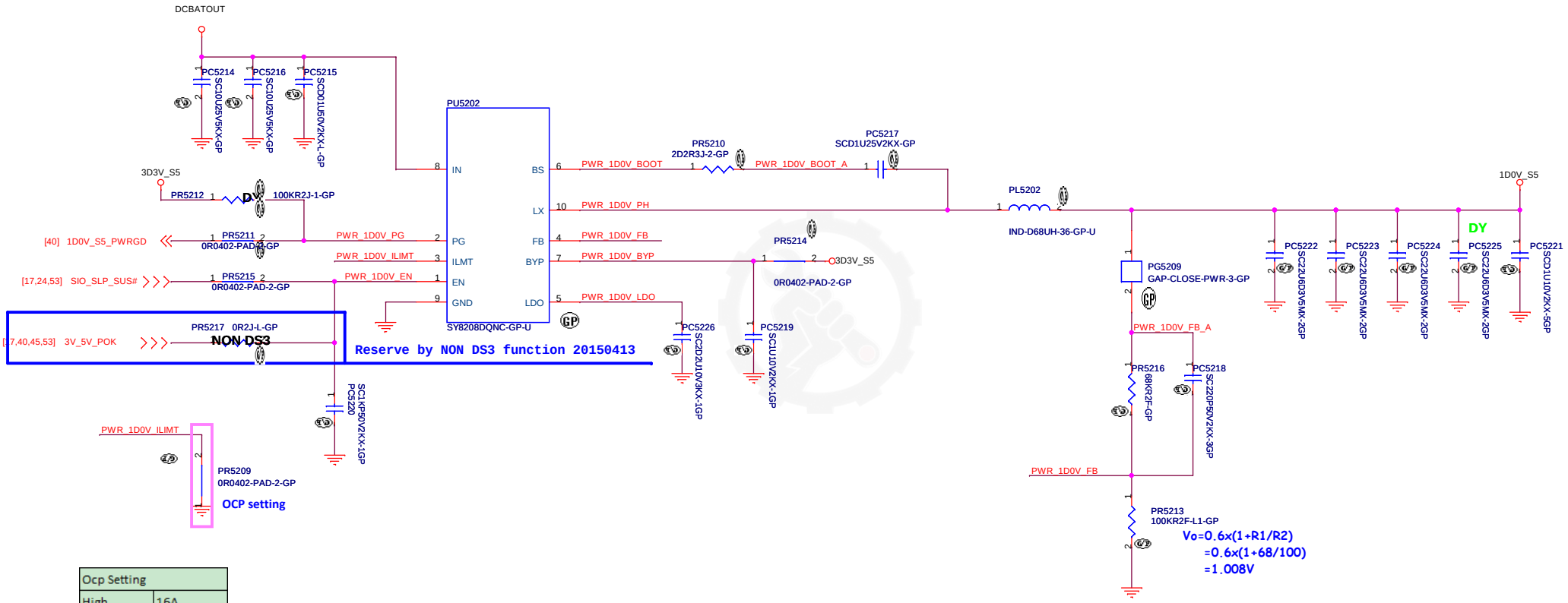
Main Func = 1D0V



Ocp Setting	
High	16A
Floating	12A
Low	8A

<Core Design>

Wistron Corporation
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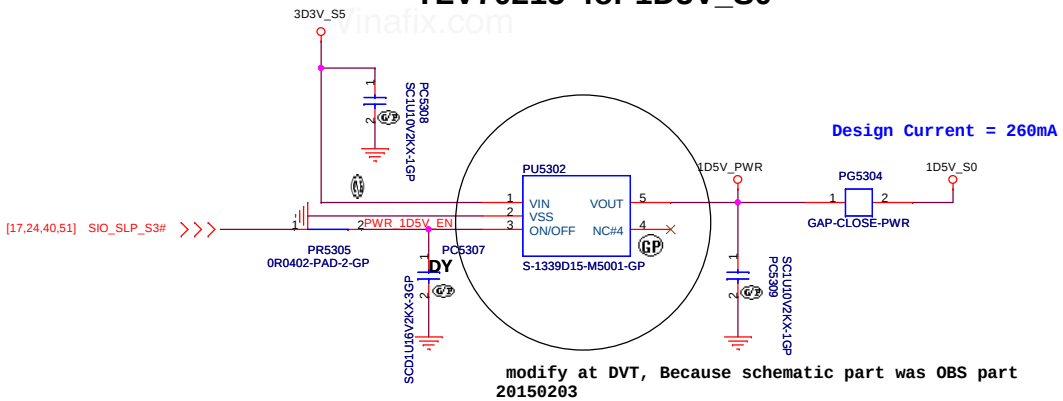
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC-V1D00A		
Size: A3	Document Number: Cottonwood SKL-U	Rev: A00
Date: Wednesday, July 08, 2015	Sheet 52 of 105	

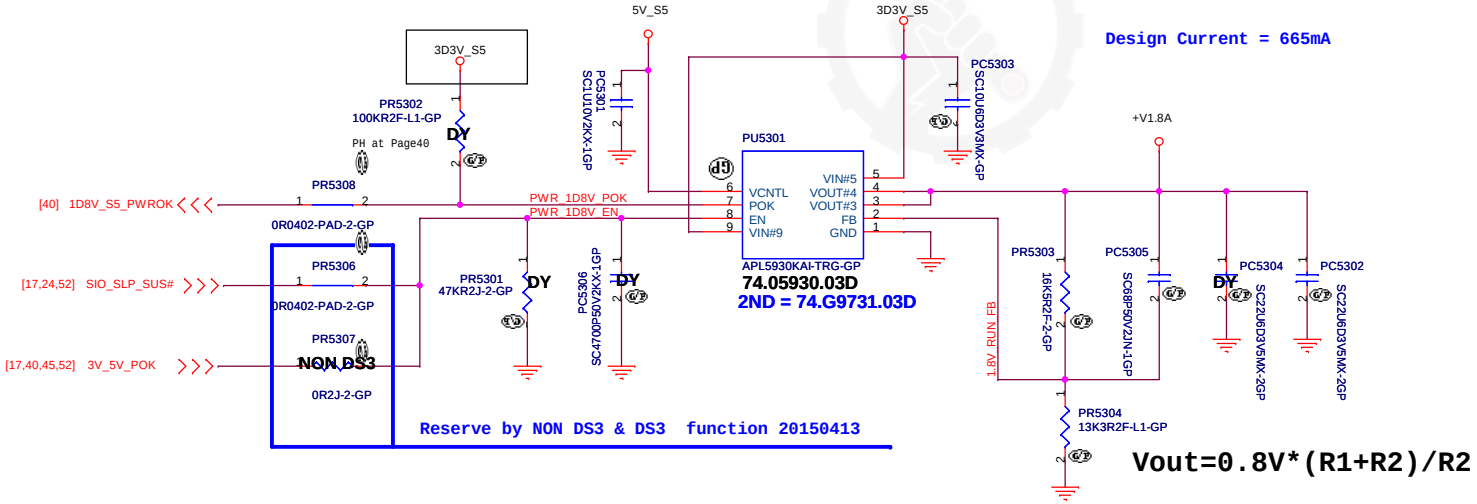
Main Func = 1D5V

TLV70215 for 1D5V_S0



modify at DVT, Because schematic part was OBS part
20150203

APL5930 for 1D8V_S5



Vout=0.8V*(R1+R2)/R2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO-V1D5V&V1D8V

Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

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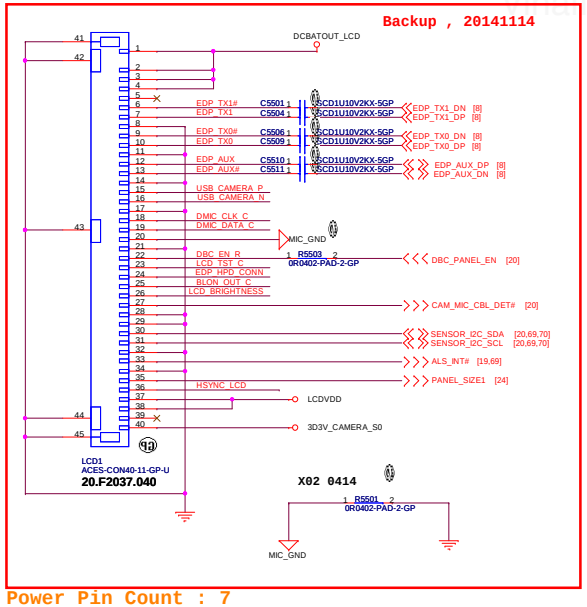
<Variant Name>

Title <Title>		
Size A	Document Number <Doc>	Rev A00
Date: Wednesday, July 08, 2015	Sheet 54 of 105	

Main Func = LCD

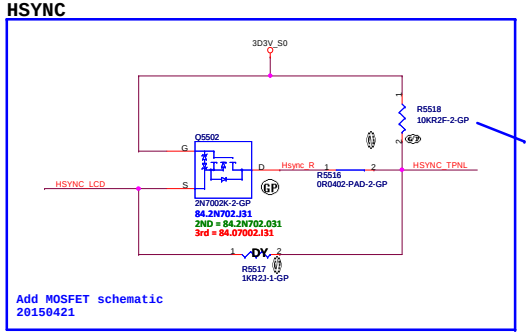
Panel Conn.

Backup , 20141114

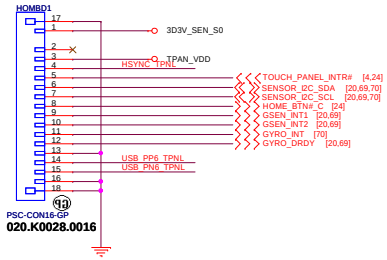


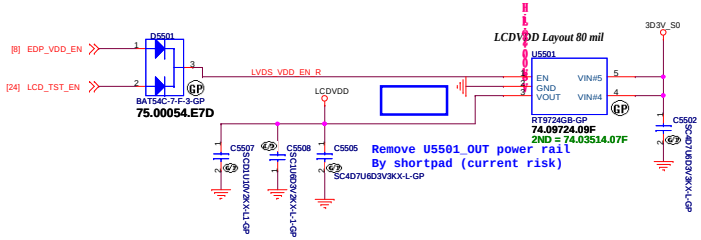
Power Pin Count : 7
GND Pin Count : 9

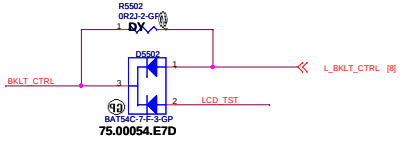
HSYNC

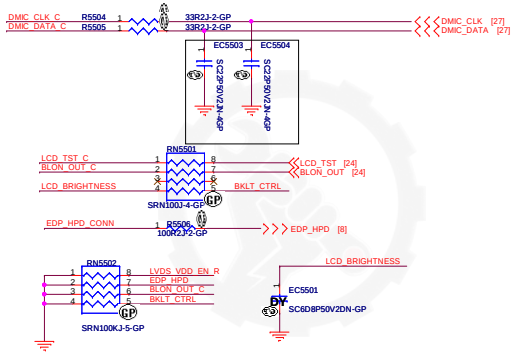


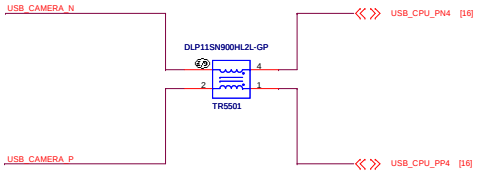
Change from 10k ohm (J) to 10k ohm (F)
20150423



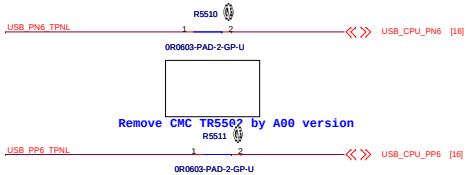




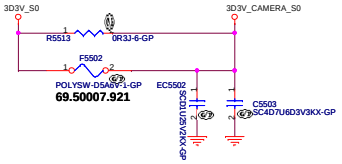




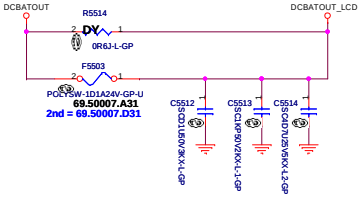
Remove 0Ohm pad R5508,R5509 by A00 version



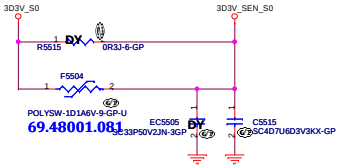
CAMERA POWER



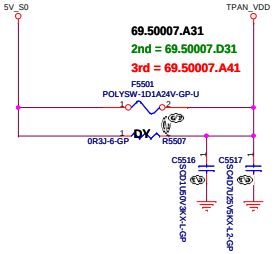
INVERTER POWER



SENSOR POWER



TOUCH PANEL POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch

Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

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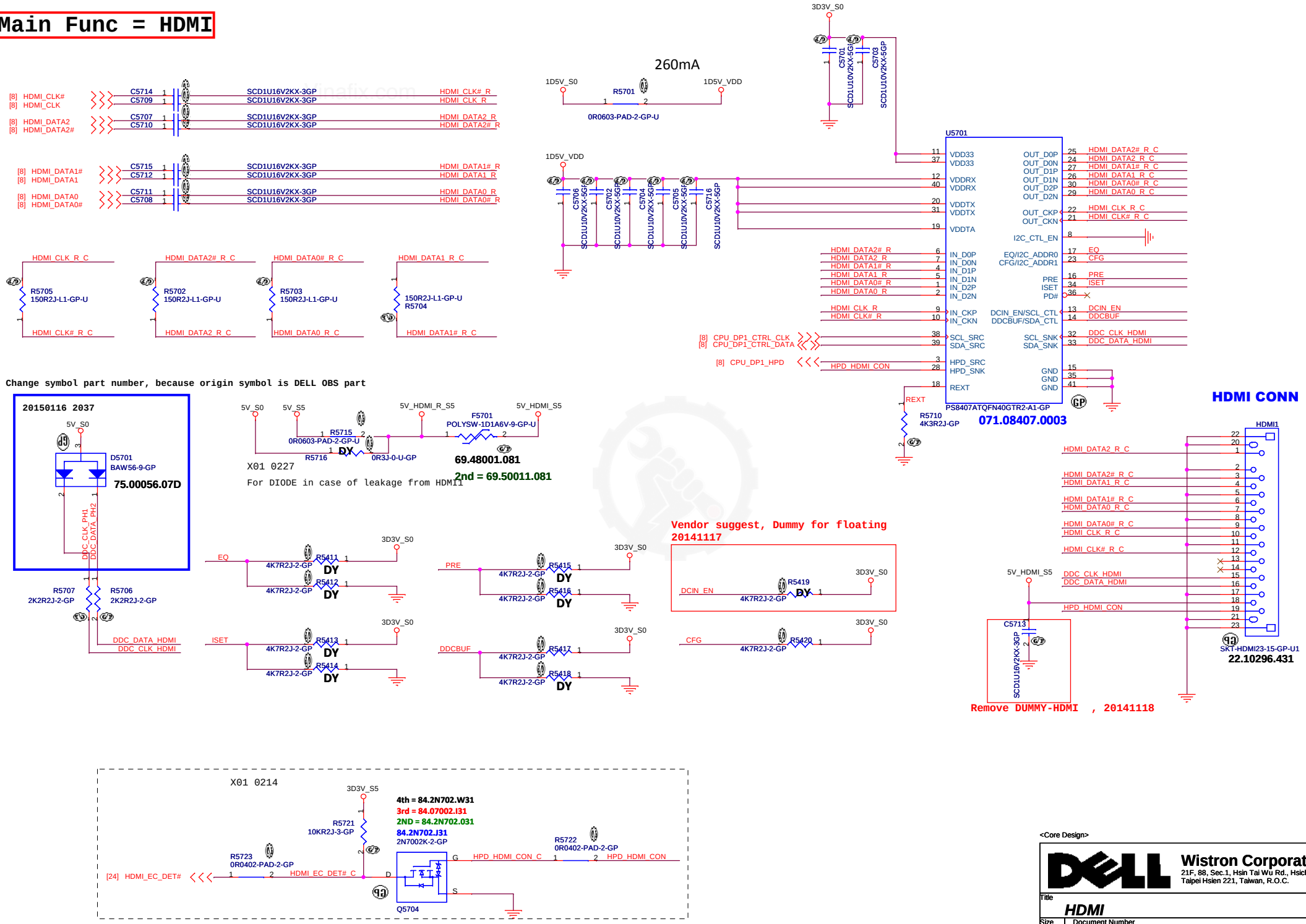
Main Func = HDMI



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI		
Size: A3	Document Number: Cottonwood SKL-U	Rev: A00
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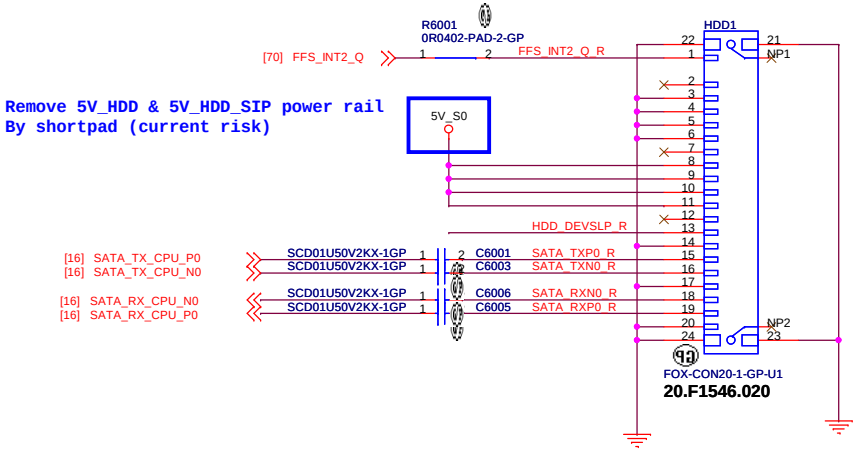
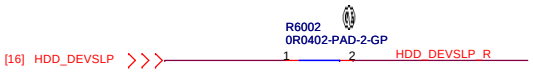
Main Func = HDD

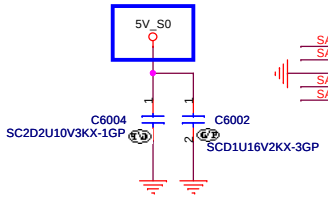
SATA HDD Connector



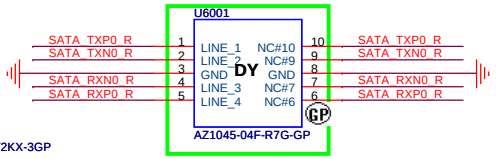
Remove 5V_HDD & 5V_HDD_SIP power rail
By shortpad (current risk)



Remove 5V_HDD & 5V_HDD_SIP power rail
By shortpad (current risk)



Layout Note:
Place near HDD1



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SATA IF_HDD/ODD

Size: A3 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Thursday, July 23, 2015 | Sheet 60 of 105

Main Func = WLAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF WLAN CONN

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 61 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	***Cottonwood SKL-U***	***A00***

Date: Wednesday, July 08, 2015 Sheet 62 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	*Cottonwood SKL-U*	*A00*

Date: Wednesday, July 08, 2015 Sheet 63 of 105

Main Func = Power BTN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

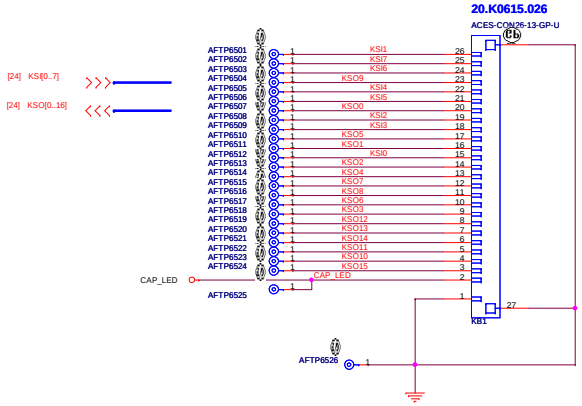
Title: *LED Board&Power Button*

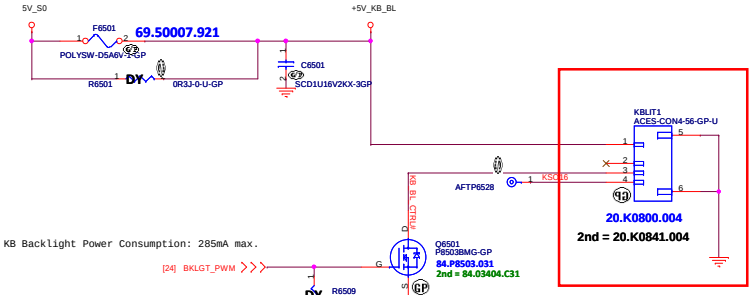
Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Wednesday, July 08, 2015 Sheet 64 of 105

Main Func = KB

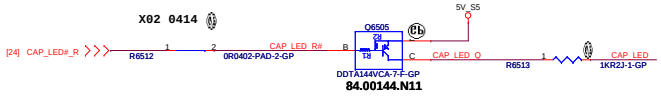
Keyboard



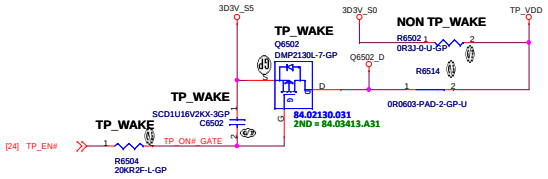


Modify at DVT1 20150127
Change component by Lock function

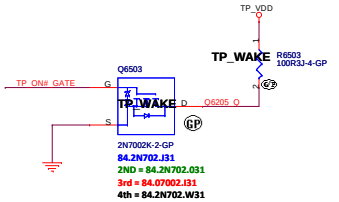
CAP LED Control
LOW actived from KBC GPIO

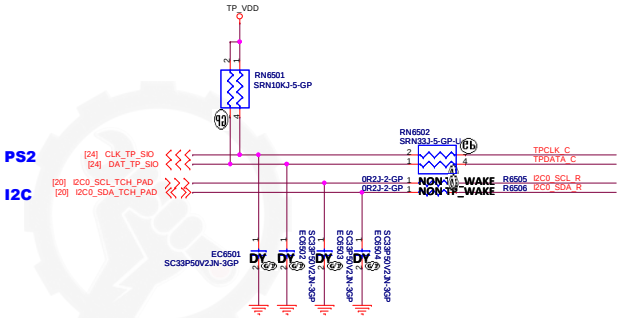


Main Func = TPAD



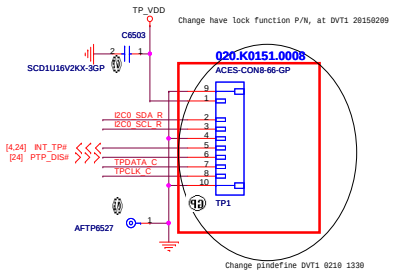
TP_VDD Discharge Circuit

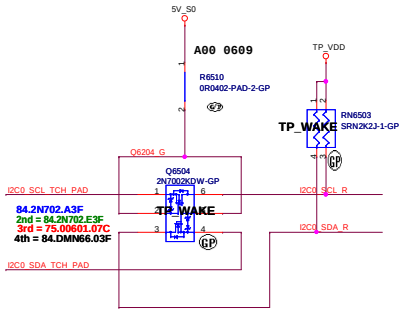




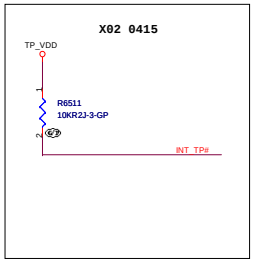
GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

Touch Pad Connector

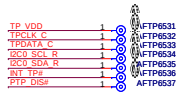




Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

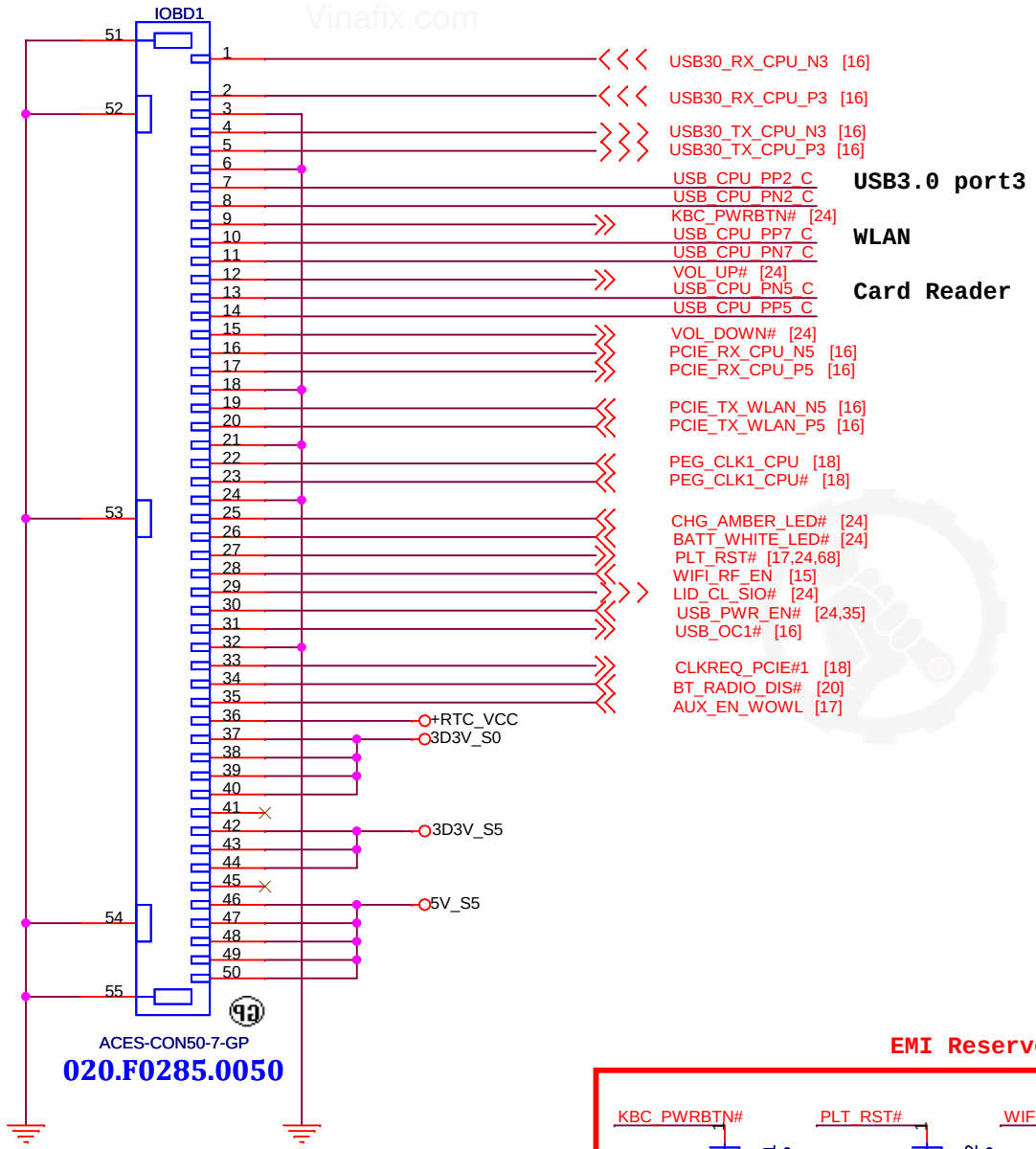


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

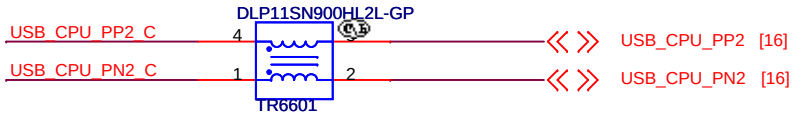
Title: Key Board&Touch Pad
Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00
Date: Wednesday, July 08, 2015 | Sheet 65 of 105

Main Func = IO Connector

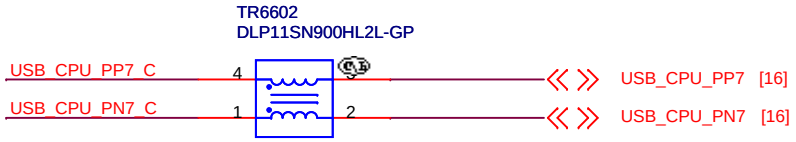


Power Pin Count : 10
GND Pin Count :5

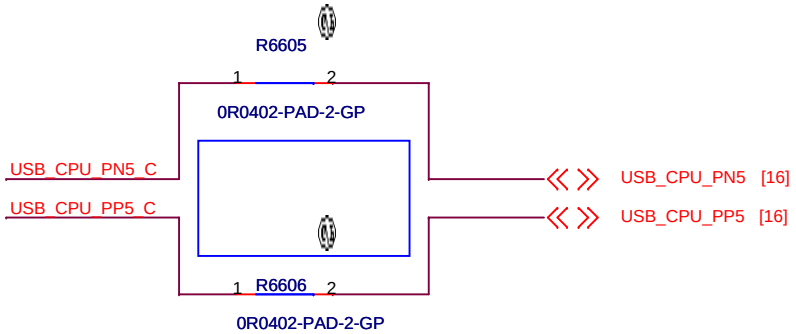
EMI Reserve , 20141118



Remove 0Ohm pad R6601,R6602 by A00 version

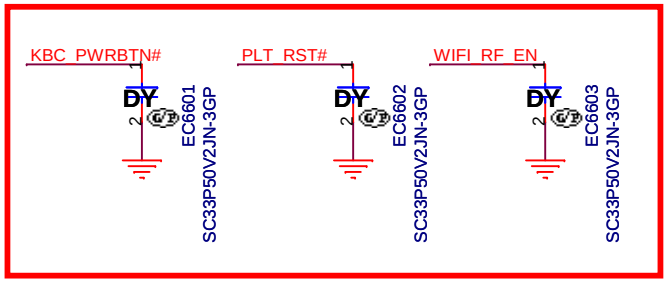


Remove 0Ohm pad R6603,R6604 by A00 version



Remove CMC TR6603 by A00 version

EMI Reserve , 20141118



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

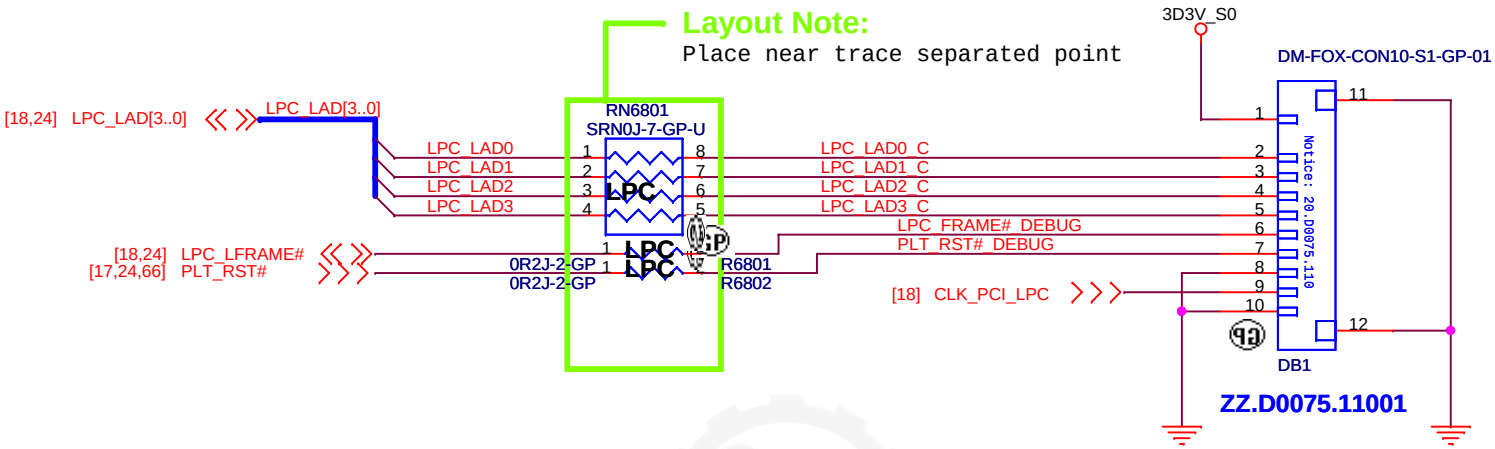
Title: *IO Board Connector*

Size	Document Number	Rev
A4	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 66 of 105

Main Func = Debug

Debug Connector



20.D0075.110: Dummy Pad with solder mask is ZZ.D0075.11001
DB1 Optional: New one smaller LPC connector is 20.F1180.010.

<Core Design>

Wistron Corporation
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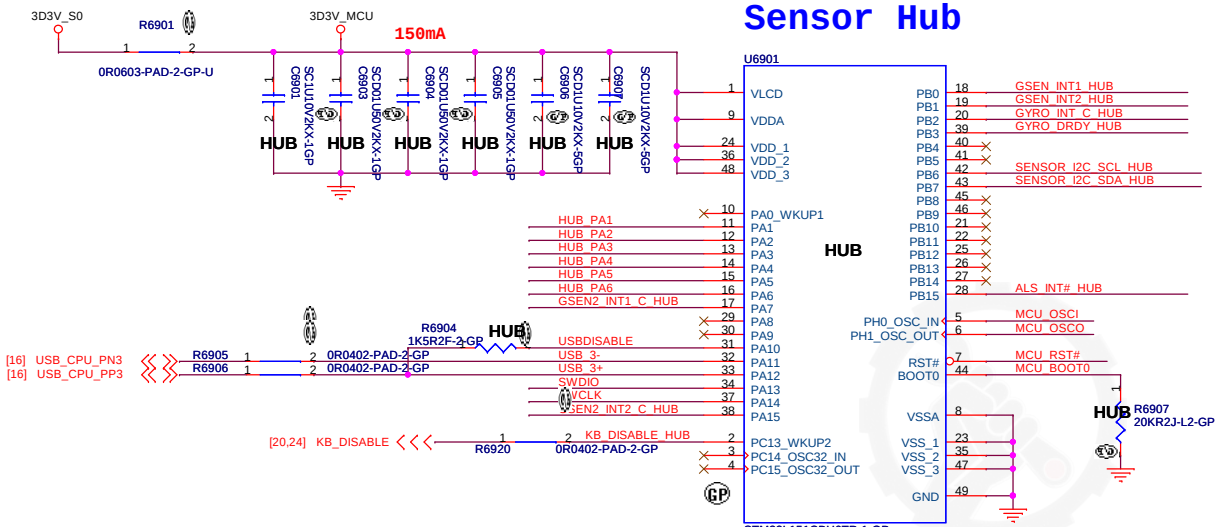
Taipei Hsien 221, Taiwan, R.O.C.

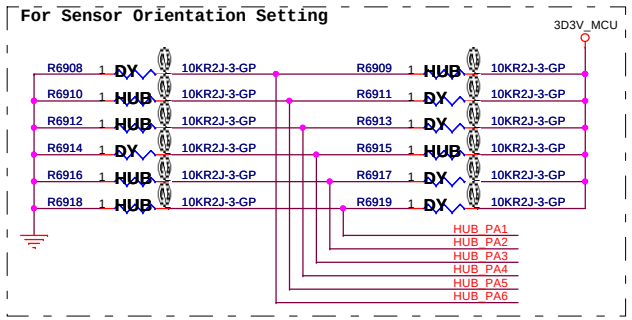
Title	*Dubug connector*	
Size A4	Document Number *Cottonwood SKL-U*	Rev *A00*
Date: Thursday, July 23, 2015	Sheet 67 of 105	

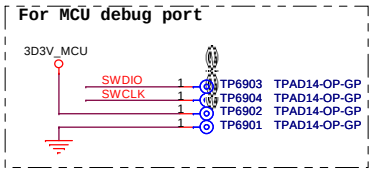
Sensor Hub

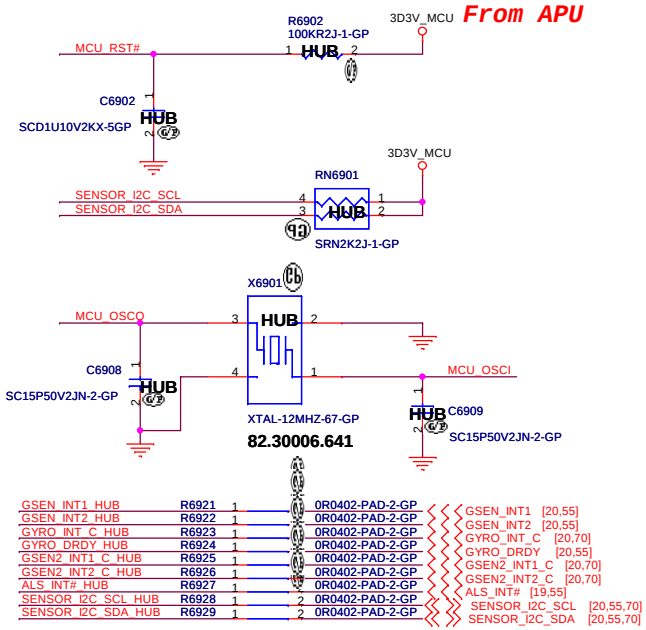


071.32151.0B0U

Sensor HUB FW version : V37







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

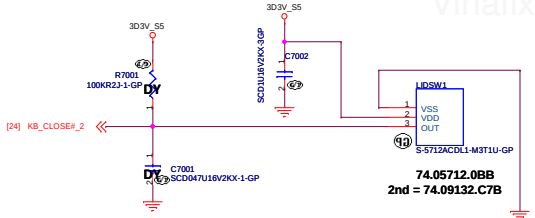
Title: **Reserved**

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

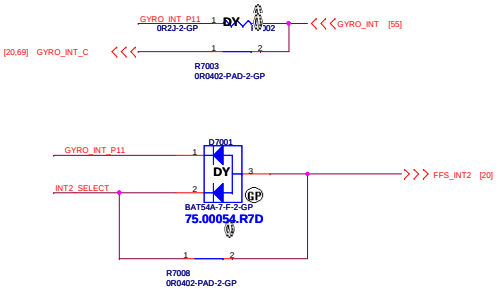
Date: Thursday, July 23, 2015 Sheet 68 of 105

Main Func = Hall Sensor

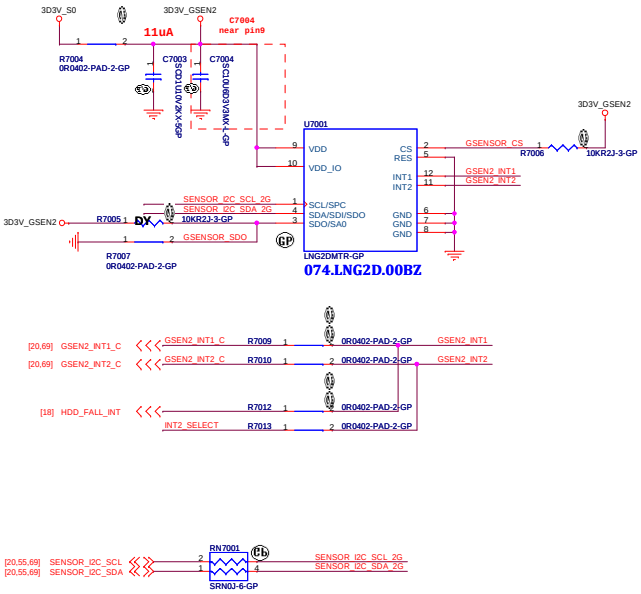
LID sensoe



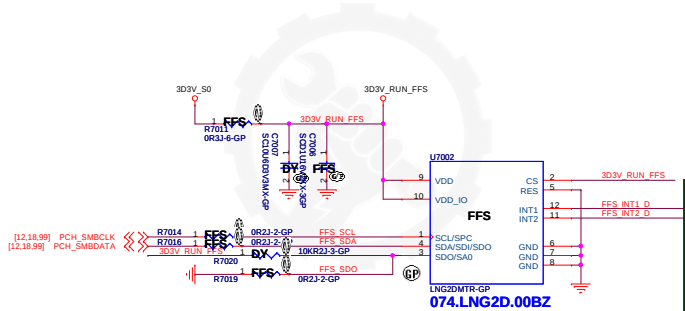
combine G



G sensor

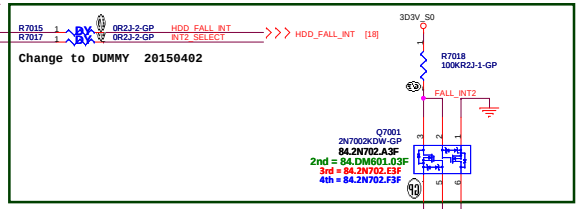


Free Fall Sensor



Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
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Title: (Reserved)

Size: A2 | Document Number: Cottonwood SKL-U | Rev: A00

Date: Tuesday, July 21, 2015 | Sheet 69 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB3.0 PORT***

Size	Document Number	Rev
A3	***Cottonwood SKL-U***	***A00***

Date: Tuesday, July 21, 2015 Sheet 71 of 105

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Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(1/5)PEG

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 75 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 76 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(3/5)VRAM/F

Size	Document Number	Rev
A1	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 77 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(4/5)GPIO/STRAP

Size	Document Number	Rev
Custom	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 78 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU(5/5)PWR/GND

Size: Custom | Document Number: Cottonwood SKL-U | Rev: A00

Date: Tuesday, July 21, 2015 | Sheet 79 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM1,2 (1/4)*

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 80 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM3,4 (2/4)*

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 81 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM5,6 (3/4)*

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 82 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU-VRAM7,8 (4/4)*

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 83 of 105

Main Func = dGFX_CORE

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU CORE

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 84 of 105

Main Func = dGPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Discrete Power

Size	Document Number	Rev
A2	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 85 of 105

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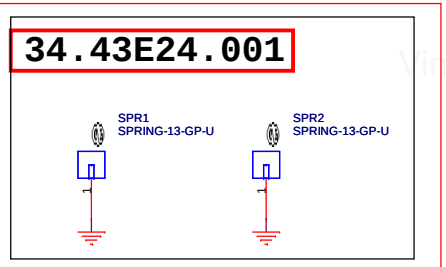
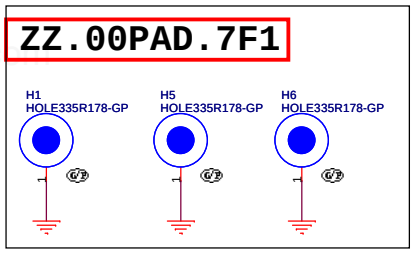
Main Func = UnusedParts

34.43E24.001

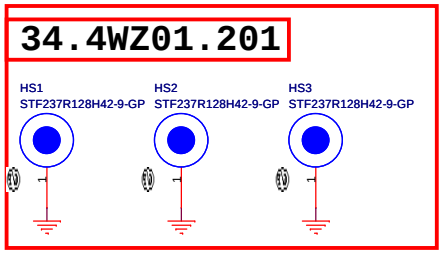


DVT1 0212 for ME

ZZ.00PAD.7F1

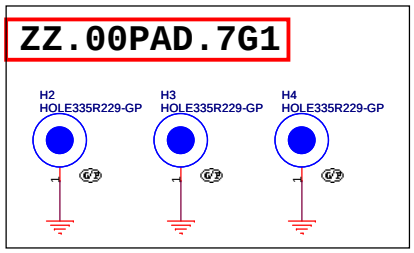


34.4WZ01.201



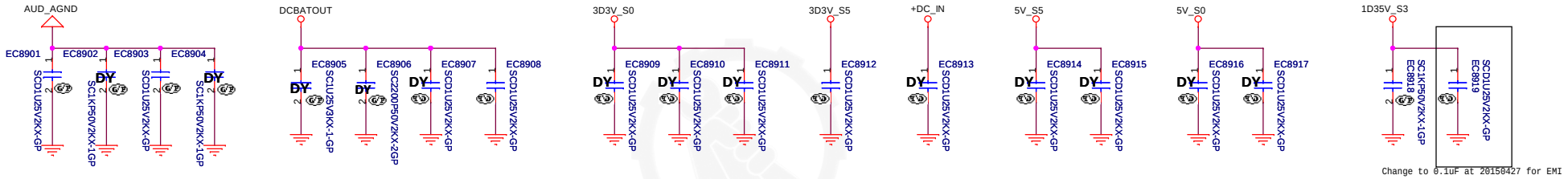
Modify at DVT1 20150204

ZZ.00PAD.7G1



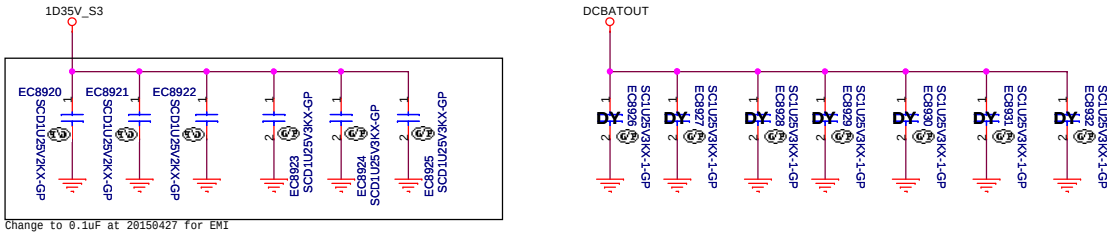
SSID = EMI

Mind the voltage rating of the caps.

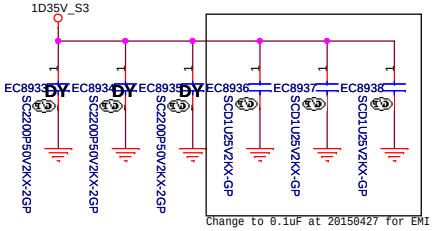


Change to 0.1uF at 20150427 for EMI

SSID = RF



Change to 0.1uF at 20150427 for EMI



Change to 0.1uF at 20150427 for EMI

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 88 of 105

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: *Cottonwood SKL-U* | Rev: *A00*

Date: Tuesday, July 21, 2015 | Sheet 93 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size: A3 | Document Number: *Cottonwood SKL-U* | Rev: *A00*

Date: Tuesday, July 21, 2015 | Sheet 94 of 105

(Blanking)

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LVDS_Switch*

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 96 of 105

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CRT_Switch*

Size	Document Number	Rev
A3	Cottonwood SKL-U	A00

Date: Tuesday, July 21, 2015 Sheet 97 of 105

Main Func = Debug

CPU XDP

Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<0>

CFG0 — R9908 1KR2J-1-GP — FIVR_EN_R

Layout Note:
ROUTE WITH MINIMAL STUB WITH RESPECT TO CFG<3>

CFG3 — R9902 1KR2J-1-GP — XDP_PRSNT_PIN1

[17] PM_RSMRST# — R9904 1KR2J-1-GP — PM_RSMRST_PWRGD_XDP

[17,24] SIO_PWRBTN# — R9926 0R0402-PAD-2-GP — BP_PWRGD_RST#

C9901 SCD1U16V2KK-3GP

C9903 SCD1U16V2KK-3GP

3D3V_S5 — R9909 3KR2J-2-GP

[18] SPI0_MOSI_XDP

[12,18,70] PCH_SMBDATA — 0R0402-PAD-2-GP — R9911 — XDP_SMBDAT
[12,18,70] PCH_SMBCLK — 0R0402-PAD-2-GP — R9912 — XDP_SMBCLK

[18] PCIE_CLK_XDP_P — R9913 0R0402-PAD-2-GP — PCIE_CLK_XDP_R_P
[18] PCIE_CLK_XDP_N — R9923 0R0402-PAD-2-GP — PCIE_CLK_XDP_R_N

[6] CFG[19:0] — CFG[19:0]
[4] XDP_BPM[3:0] — XDP_BPM[3:0]

XDP_BPM2 — TP9901 TPAD14-OP-GP
XDP_BPM3 — TP9902 TPAD14-OP-GP

+VCCIO — R9906 150R2J-L1-GP-U — FIVR_EN_R

XDP_PRSNT_PIN1

[16] XDP_PREQ#
[16] XDP_PRDY# — XDP_PRDY#

XDP1 — PAD-60P-GP — ZZ.00PAD.Q81

CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7
CFG8 CFG9 CFG10 CFG11 CFG12 CFG13 CFG14 CFG15
CFG16 CFG17 CFG18 CFG19

XDP_BPM0 XDP_BPM1

PM_RSMRST_PWRGD_XDP
BP_PWRGD_RST#
FIVR_EN_R
SPI0_MOSI_XDP
XDP_SMBDAT
XDP_SMBCLK
XDP_TCLK1

PCIE_CLK_XDP_R_P
PCIE_CLK_XDP_R_N
TP_PMODE_XDP_RST_R_N
XDP_DBRESET#_XDP#
PCH_JTAG_TDO

[4] XDP_TCLK
XDP_TRST# [4]
XDP_TDI [4]
XDP_TMS [4]
XDP_SPI0_IO2 [18]

(#543016)Routing of this signal to CFG[0] is OPTIONAL.

1D0V_S5

PLACE THIS NEAR CPU XDP CONNECTOR

C9905 SCD1U16V2KK-3GP

R9925 0R0402-PAD-2-GP — XDP_DBRESET# [17]

EE Note:
Use ZZ.00PAD.Q81 DUMMY PAD for MP.

1D0V_S5 — R9927 0R0402-PAD-2-GP — +V1.00A_XDP

C9902 SCD1U16V2KK-3GP

C9904 SCD1U16V2KK-3GP

3D3V_S5 — R9929 100KR2J-1-GP — XDP_SPI0_IO2 — R9931 0R2J-2-GP

+V1.00A_XDP — R9932 1K5R2J-3-GP — [6] ITP_PMODE

(#544669 Rev0.52) NC.
R9933 0R0402-PAD-2-GP — TP_PMODE_XDP_RST_R_N

(#544669)

XDP_TCLK1 — R9914 0R0402-PAD-2-GP — PCH_JTAG_TCK [4]
XDP_TCLK — R9915 0R0402-PAD-2-GP — XDP_TCK_JTAGX [4]
[4] XDP_TDO_CPU — R9919 0R0402-PAD-2-GP — PCH_JTAG_TDO [4]
XDP_TDI — R9916 0R0402-PAD-2-GP — PCH_JTAG_TDI [4]
XDP_TMS — R9917 0R0402-PAD-2-GP — PCH_JTAG_TMS [4]

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_XDP;PCH_XDP
Size: A2
Document Number: Cottonwood SKL-U
Rev: A00
Date: Tuesday, July 21, 2015
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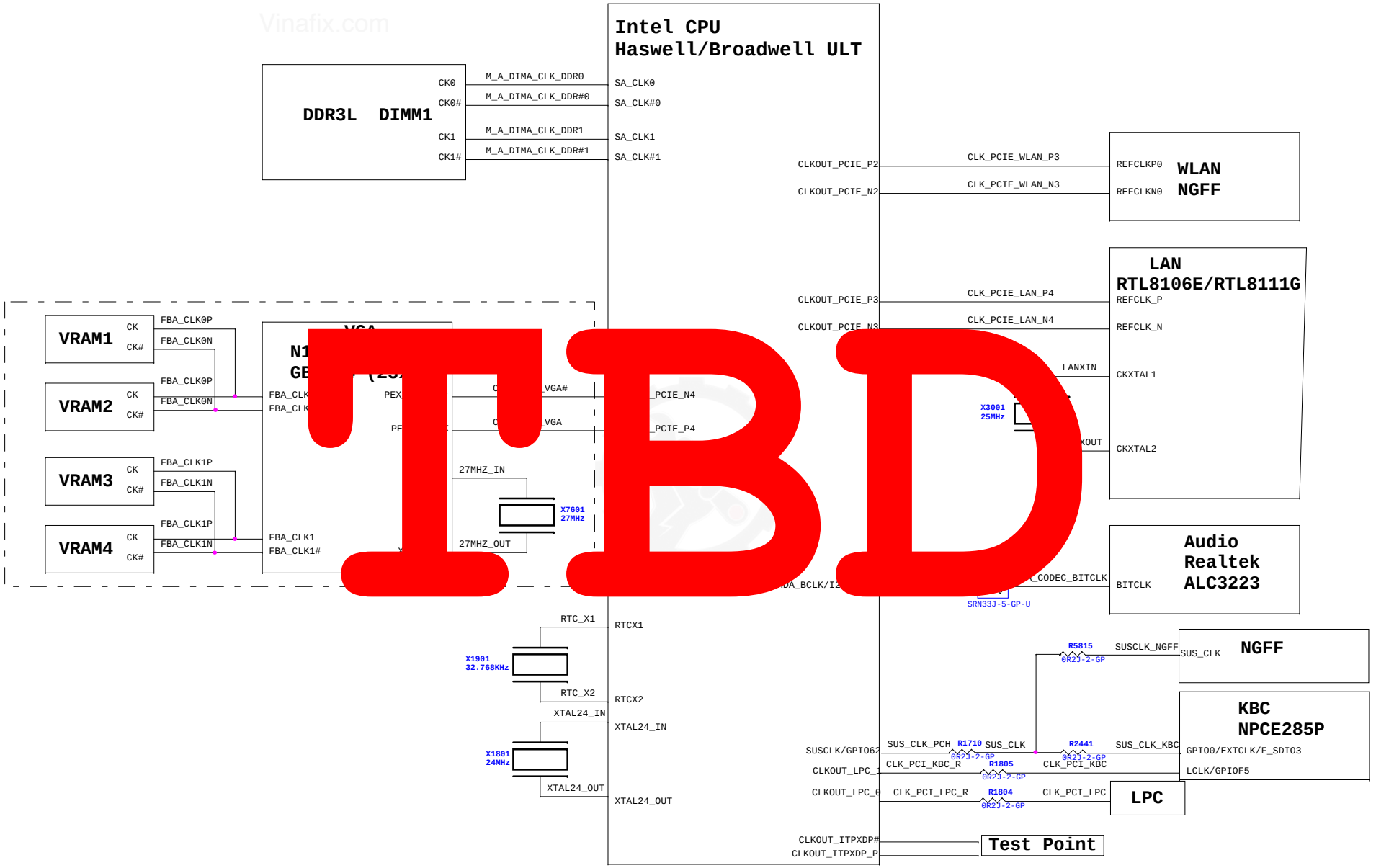
CLK Block Diagram



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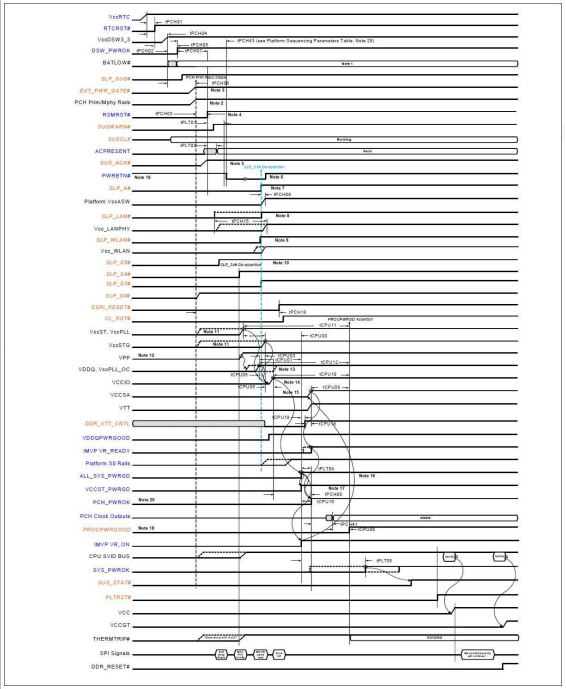
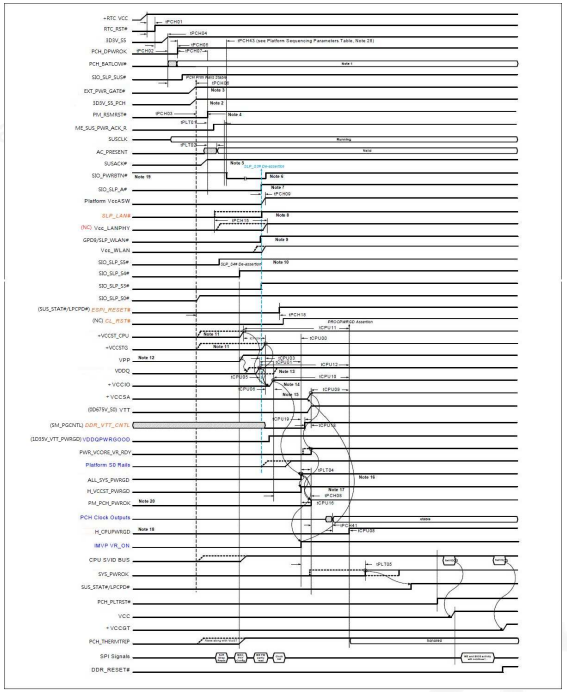
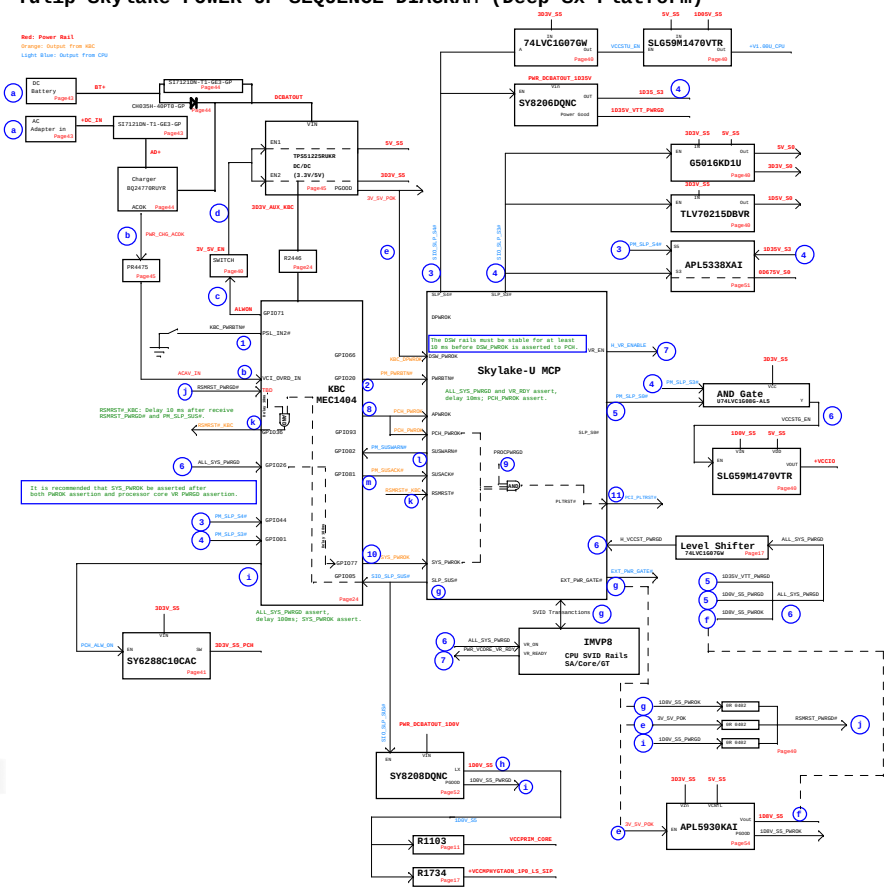
SKL-U/Y Timing Diagram for G3 to S0/M0 [Deep Sx Platform]



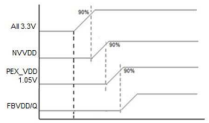
SKL-U/Y Timing Diagram for G3 to S0/M0 [Deep Sx Platform]



Tulip Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)



[dGPU] N16x Power-Up/Down Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

Note:
- The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- The previous power rail must ramp up to 90% before the next power rail can start ramping up.
- No signal should be applied to the GPU before the power rails are fully ramped
- Refer to the JEDEC Memory Specification for memory related power sequencing.
- The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 en and exit sequence and timing requirements.

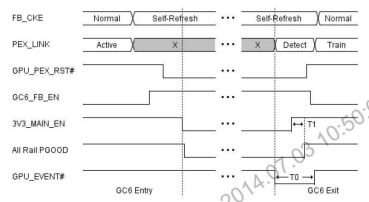
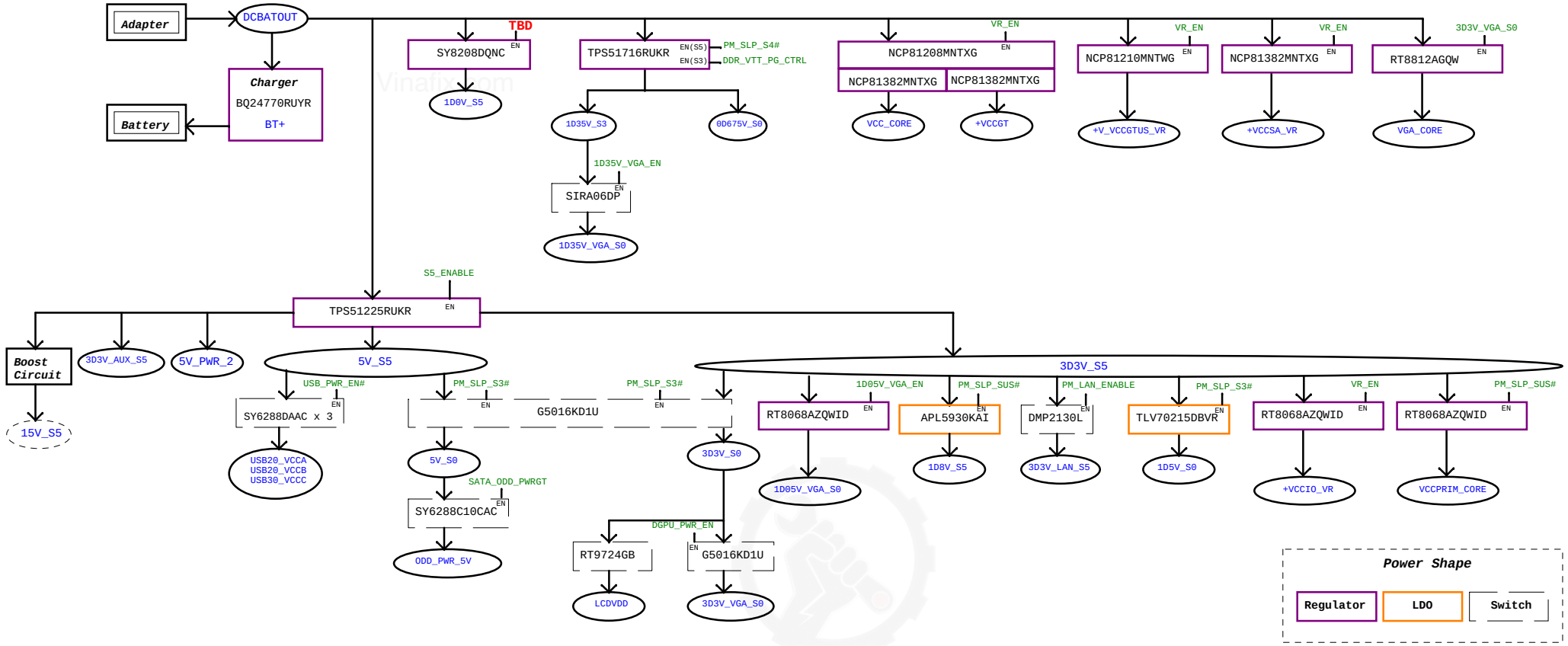


Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.



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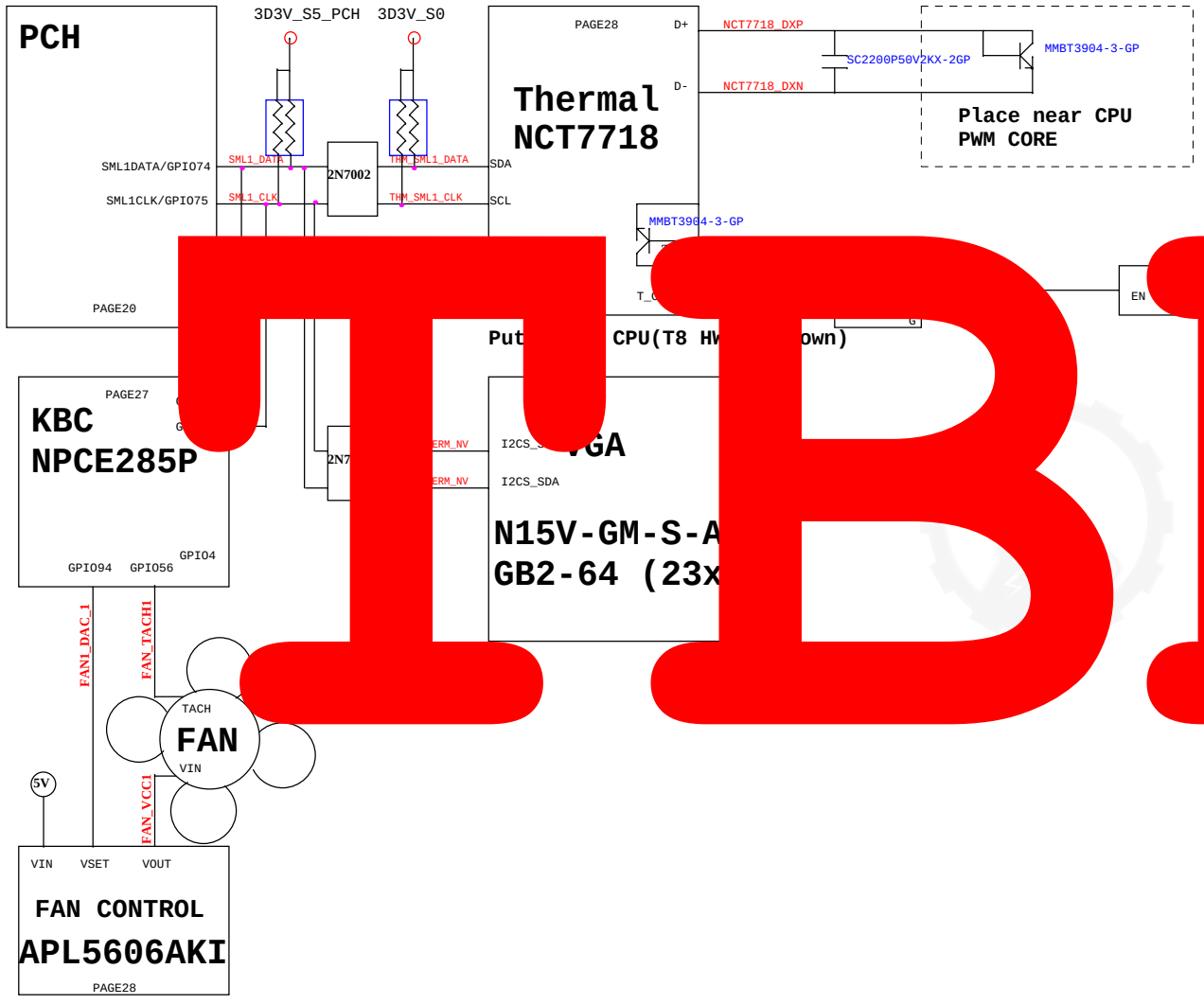
Thermal Block Diagram



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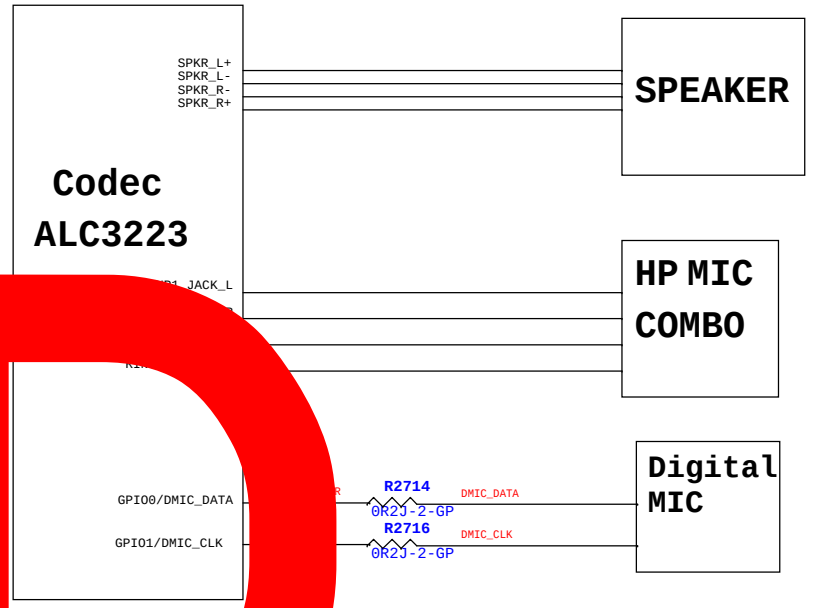
Audio Block Diagram



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