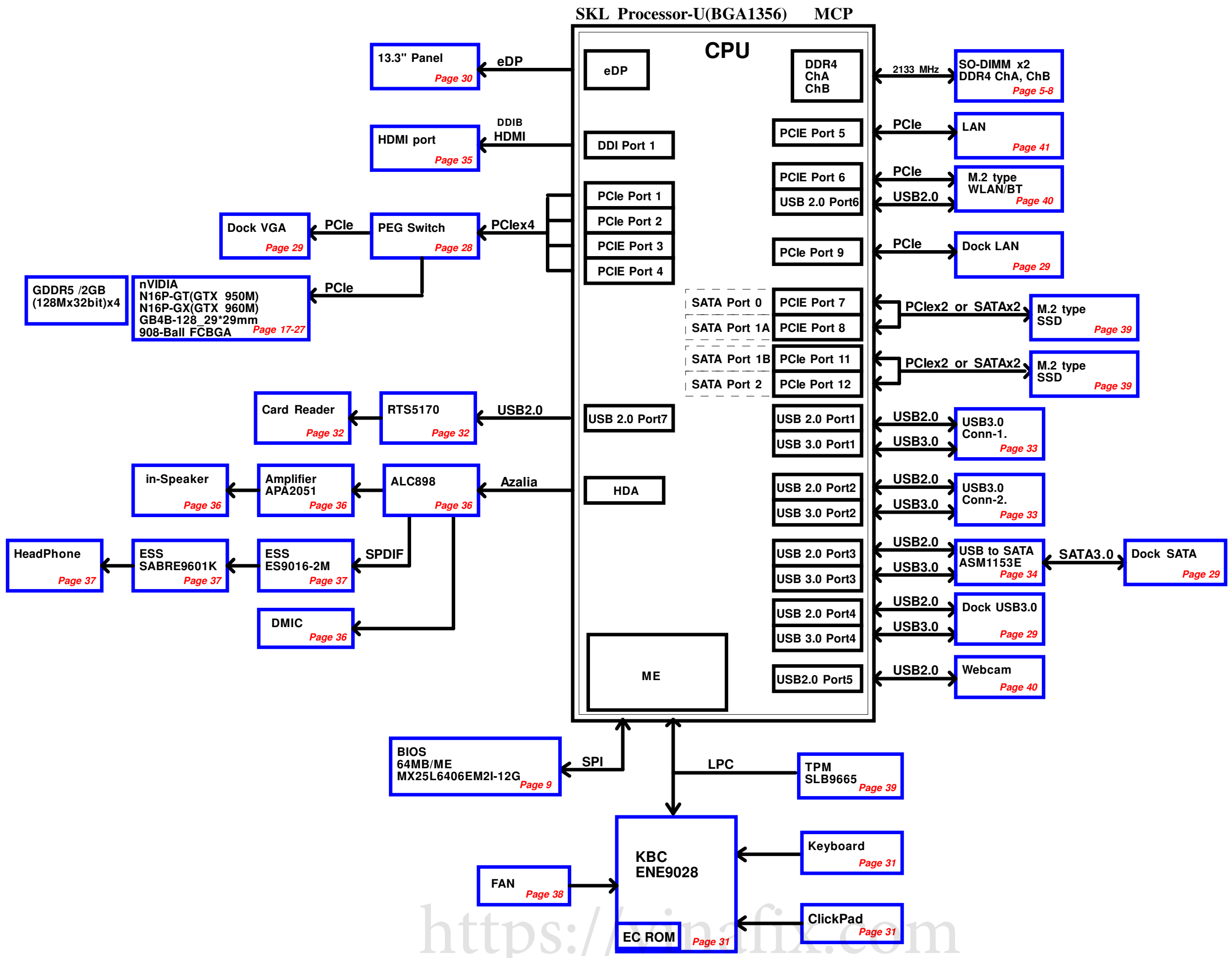
SkyLake Processor-U Platform

MS-13F2 Ver:10



MICRO-STAR INT'L CO.,LTD.		
Title: Block Diagram		
Size	Document Number: MS-13F2	Rev: 10
Date:	Sheet 1 of 60	

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1.2VDIMM	1.2V DDR4 power rail (off in S4-S5)	DIMM_ON_1V2
+0_6VRUN	0.6V DDR4 Termination voltage (off in S3-S5)	DDR_PG_CTRL
+5VRUN	5.0V switched power rail (off in S3-S5)	RUN_ON
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	RUN_ON
+1.0VSUS	1.0V switched power rail (off in S3-S5)	3V5VSUSPWROK
+1.8V_SUS	1.8V power rail	SUS_ON
+VCC_CORE	Core Voltage for Processor	EC_ALLSYSPG
+VCCSA	VCCSA Voltage for Processor	EC_ALLSYSPG
+VCC_GT	VCC_GT Voltage for Processor	EC_ALLSYSPG
+1_05VRUN	1.05V rail for Processor	RUN_ON
NVVDD	NVVDD Voltage for GPU	NVVDD_EN
FBVDDQ	1.35 Voltage for GPU Memory	FBVDDQ_ON
+3V_LCD	3.3V power rail for Panel	EDP_VDDEN
CARD_3V3	3.3V power rail for Cardreader	SD_PWR_EN_Q
USB5V_PT1	5V power rail for USB	USB_ENABLE
USB5V_PT2	5V power rail for USB	USB_ENABLE
+5V_SATA	5V power rail for SATA	EC_ALLSYSPG SD_PWR_EN_Q
+1.05V_SATA	+1.05V power rail for SATA	+3.3V_SATA
+5VRUN_HDMI	5V power rail for HDMI	+3VRUN

POWER STATES

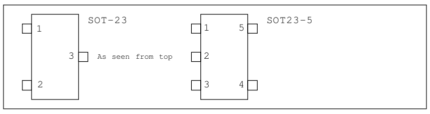
SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0(Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on and +V*SUS always keep high

Net Naming Conventions

Suffix
```
#  =  Active Low Signal
```
Prefix
```
H  =  Host
M  =  DDR Memory
TP =  Test Point (does not connect anywhere else)
FB = DGPU VRAM
VIAxxx =  Like Test Point, but using VIA.
```

PCB Footprints



MICRO-STAR INT'L CO.,LTD.

Title	Platform
Size	Document Number: MS-13F2
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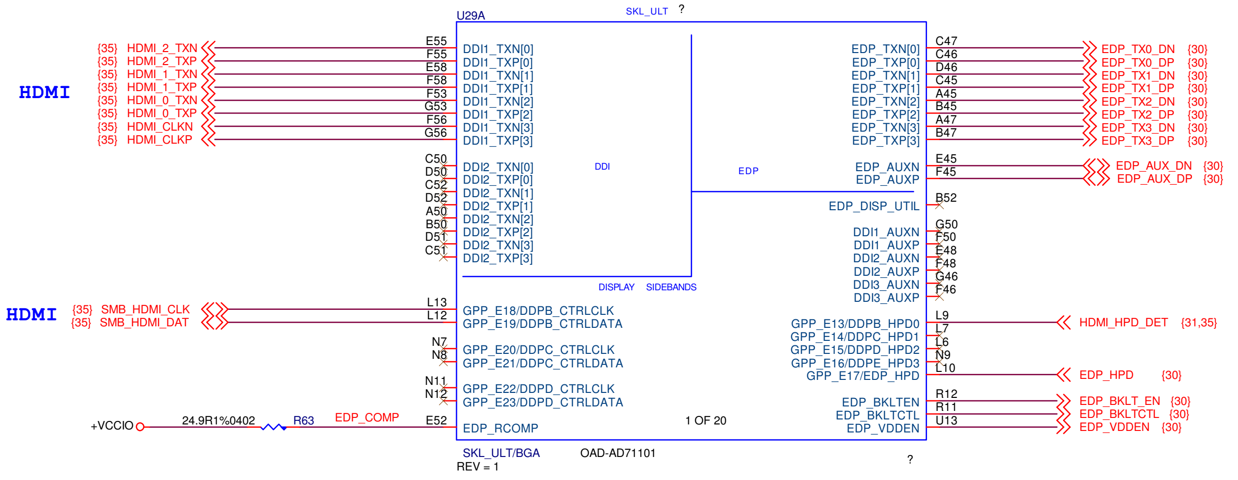
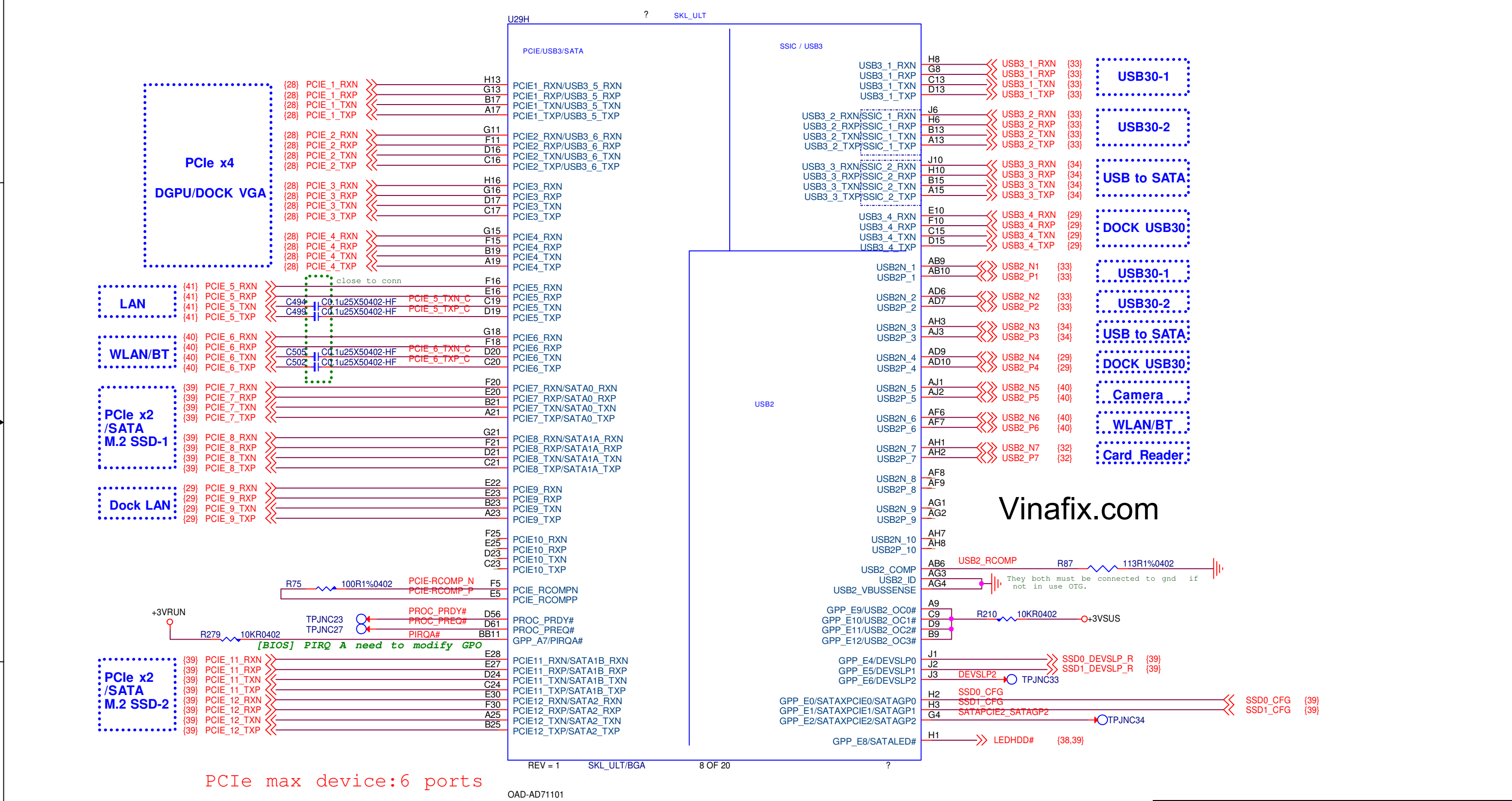
OA9-13G1001



MSI
Link to the Future

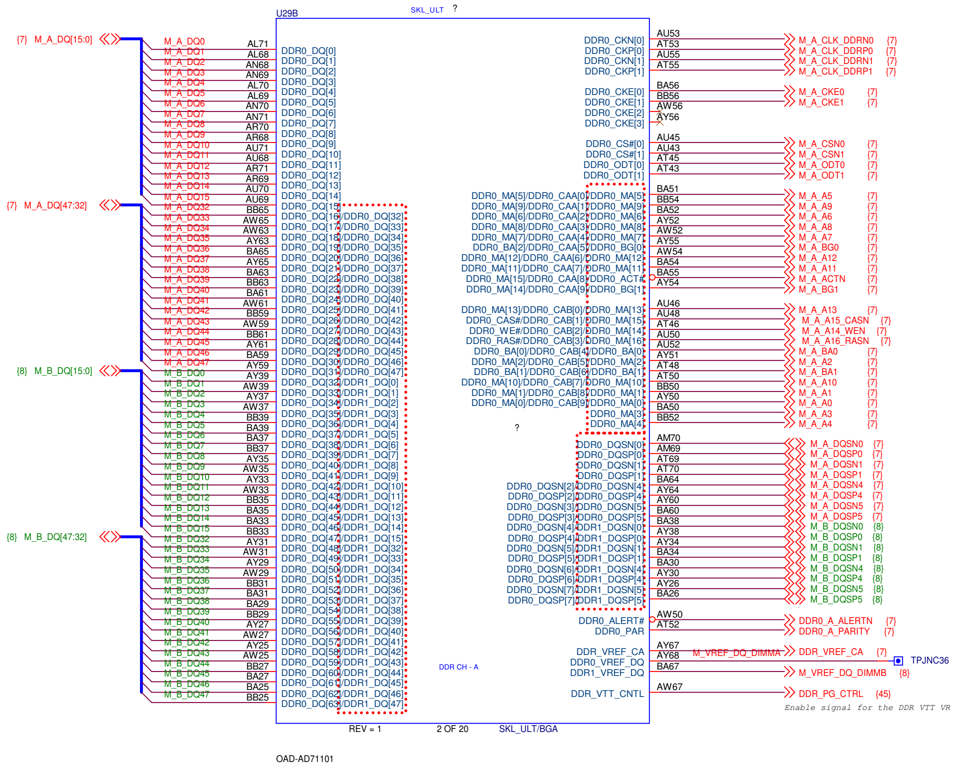
MICRO-STAR INT'L CO.,LTD.

Title	Skylake-U (eDP,DDI)		
Size Custom	Document Number MS-13F2		Rev 10
Date:	Tuesday, February 23, 2016	Sheet 3 of 60	

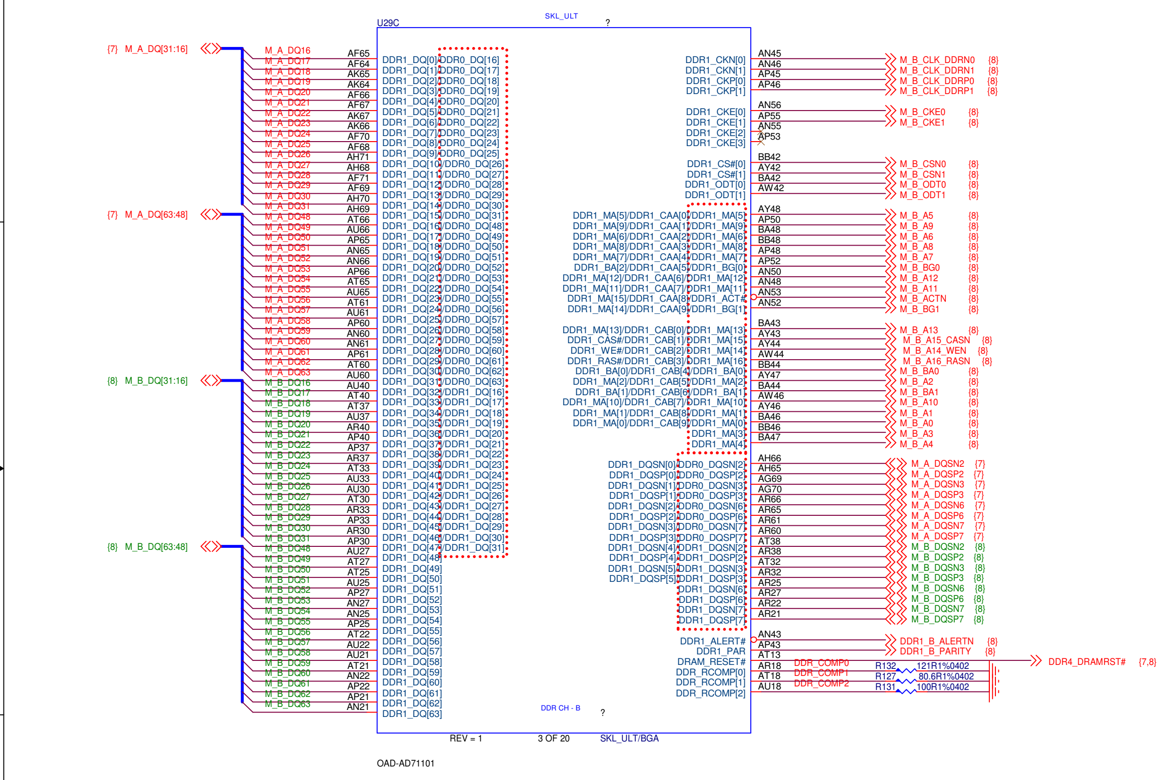


MICRO-STAR INT'L CO.,LTD.

Title	Skylake-U (PCIE,SATA,USB)	
Size B	Document Number MS-13F2	Rev 10
Date: Tuesday, February 23, 2016	Sheet 4 of 60	

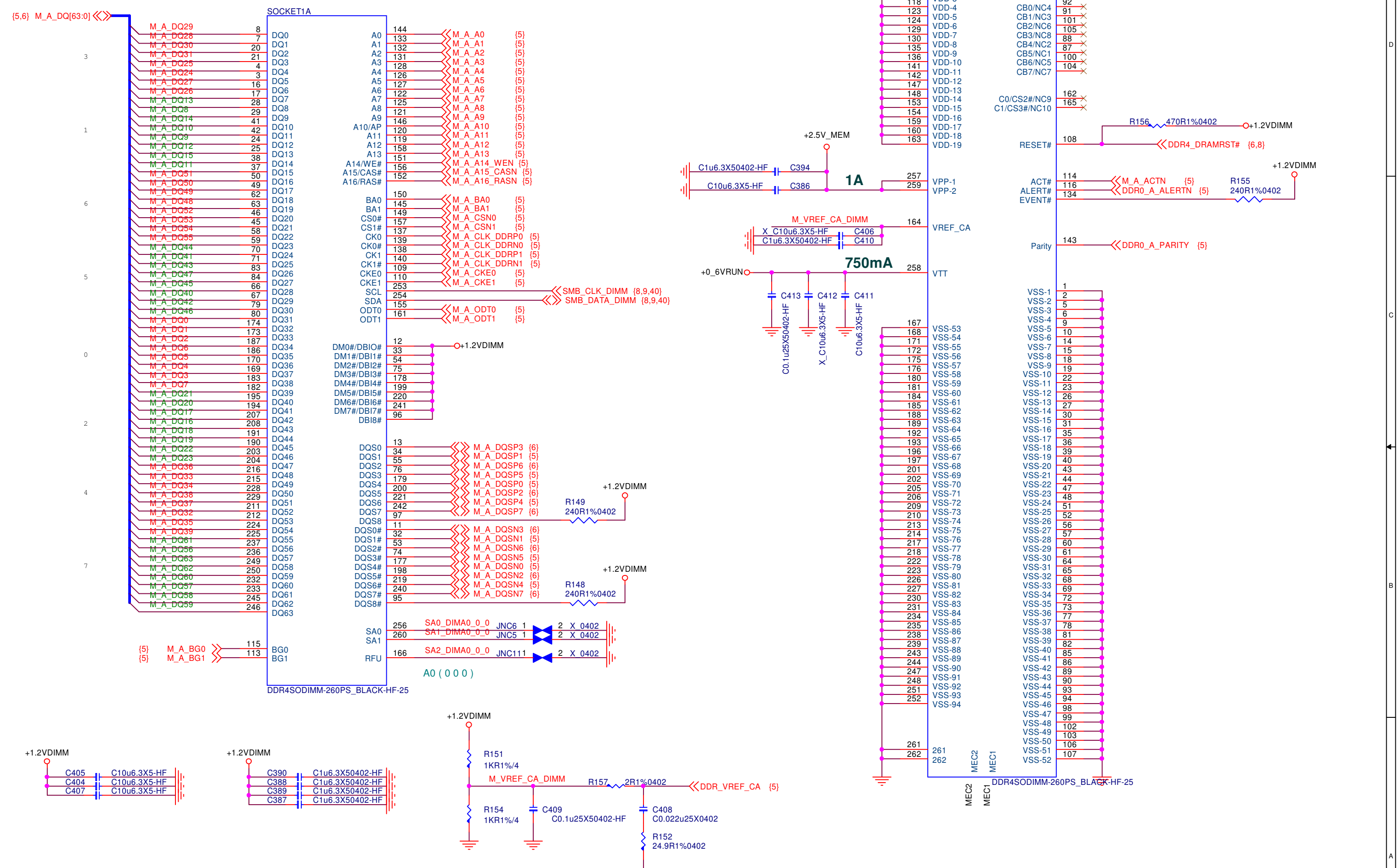


MSI	MICRO-STAR INT'L CO.,LTD.		
Title	Skylake-U (DDR4)CHA		
Size B	Document Number MS-13F2		Rev 10
Date: Tuesday, February 23, 2016	Sheet 5 of 60		



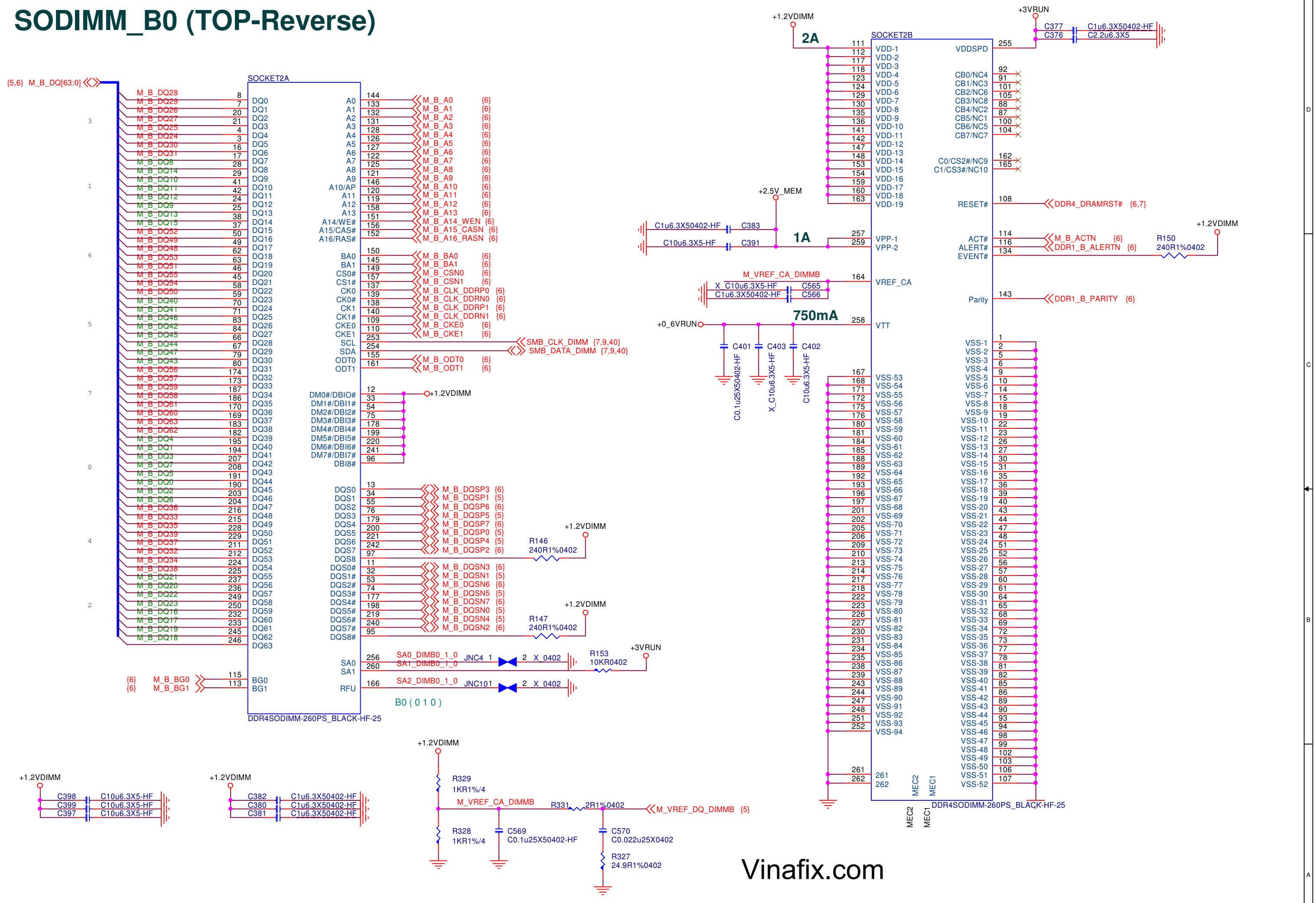
MICRO-STAR INT'L CO.,LTD.		
Title: Skylake-U (DDR4)CHB		
Size: B	Document Number: MS-13F2	Rev: 10
Date: Tuesday, February 23, 2016	Sheet 6 of 60	

SODIMM_A0 (TOP-Reverse)



MSI	MICRO-STAR INT'L CO.,LTD.	
Title	DDR4 SODIMM A0	
Size: Custom	Document Number: MS-13F2	Rev: 10
Date: Tuesday, February 23, 2016	Sheet 7 of 60	

SODIMM_B0 (TOP-Reverse)



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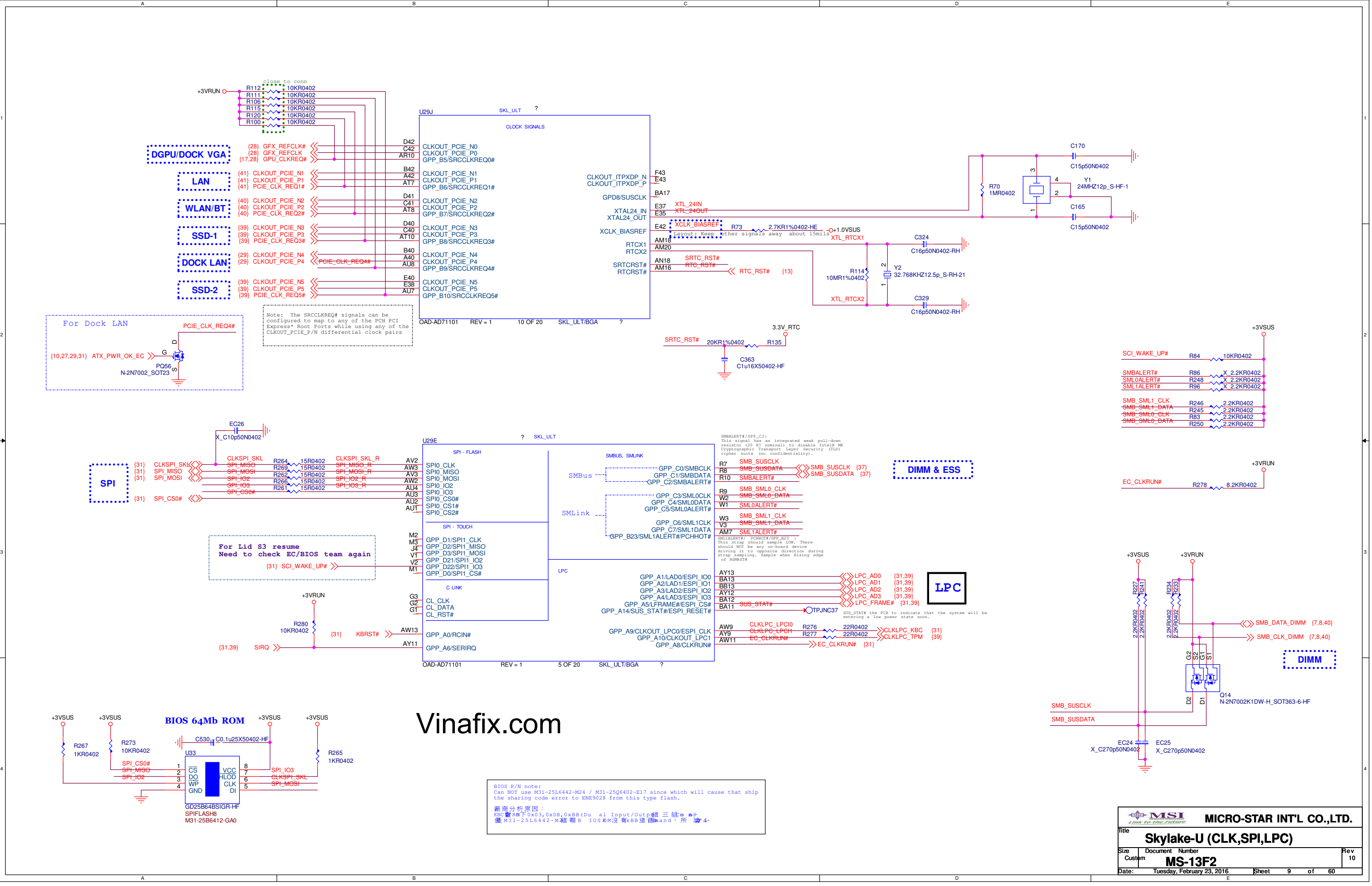
MSI Link to the Future

MICRO-STAR INT'L CO.,LTD.

Title	DDR4 SODIMM B0	
Size: Custom	Document Number: MS-13F2	Rev: 10
Date: Tuesday, February 23, 2016	Sheet 8 of 60	



MICRO-STAR INT'L CO.,LTD.

Title: Skylake-U (CLK,SPI,LPC)

Size	Document Number	Rev
Custom	MS-13F2	10

Date: Tuesday, February 23, 2016 Sheet 9 of 60

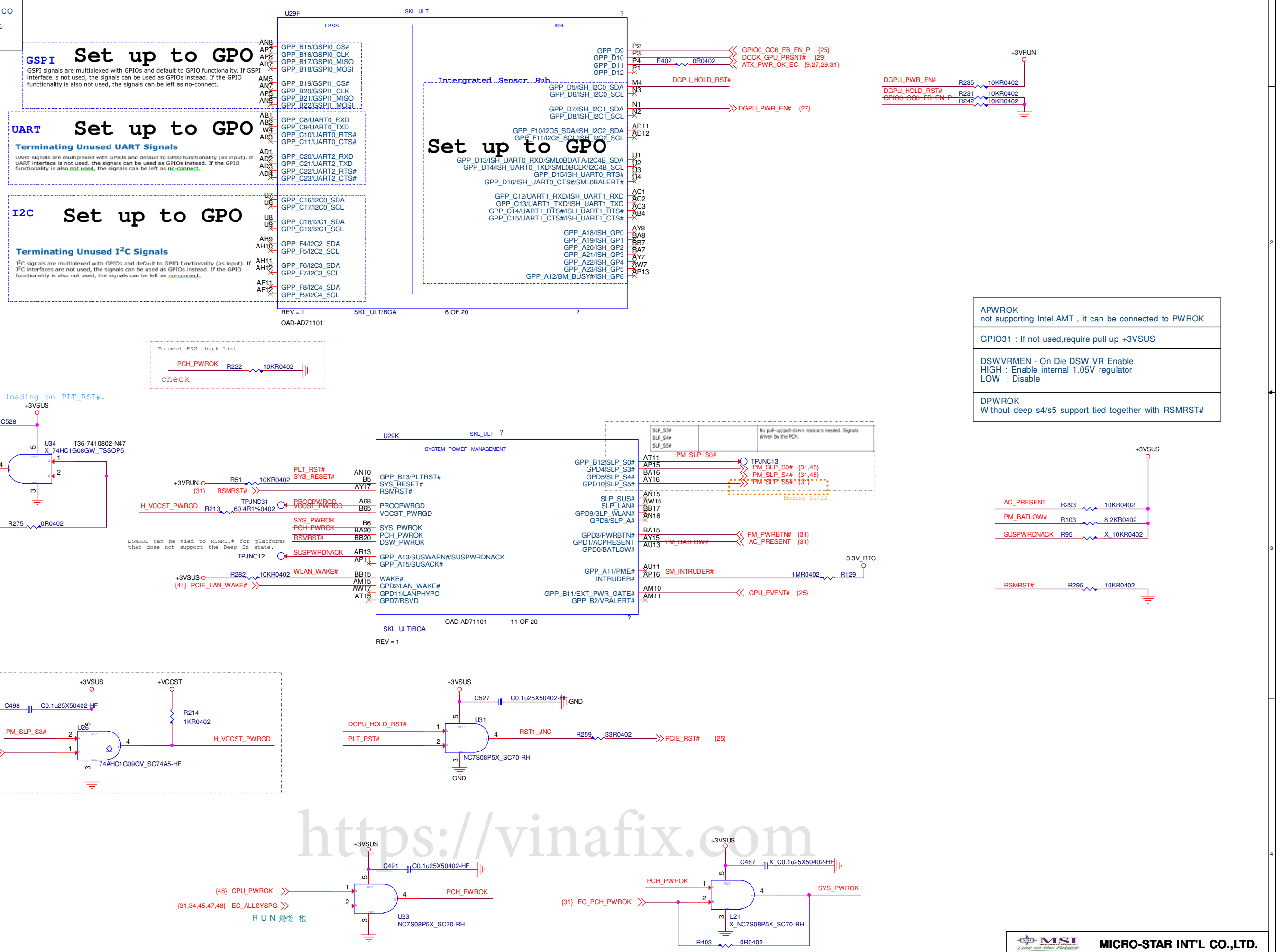
GPIO27
Connect this signal on PCH to EC. This signal resides in the DSW rail and can be used to wake the system from Deep Sx.

GPIO12
This signal may optionally be connected to a switch to turn 3.3-V PHY power off when LAN is disabled for additional power savings.

GPIO15:
This signal has an integrated weak pull-down (20KΩ nominal) resistor to enable the ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

GPIO71: This power can be shut off when PCH drives HSIOPC low during S0 idle condition. external resistor is required for out put de -glitch during power sequencing.

GPIO81:This signal has an integrated weak pull-down (20KΩ nominal) to enable reboot on TCO Timer expiration.
Pull up to VCC3_3 through a 1K to 8.2KΩ ± 5% resistor to disable this capability.



APWROK
not supporting Intel AMT , it can be connected to PWROK

GPIO31 : If not used,require pull up +3VSUS

DSWVRMEN - On Die DSW VR Enable
HIGH : Enable internal 1.05V regulator
LOW : Disable

DPWROK
Without deep s4/s5 support tied together with RSMRST#

MSI	MICRO-STAR INT'L CO.,LTD.
Title	Skylake-U (GPIO, SYSPWR, I2C)
Size: Custom	Document Number: MS-13F2
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Date:	Tuesday, February 23, 2016
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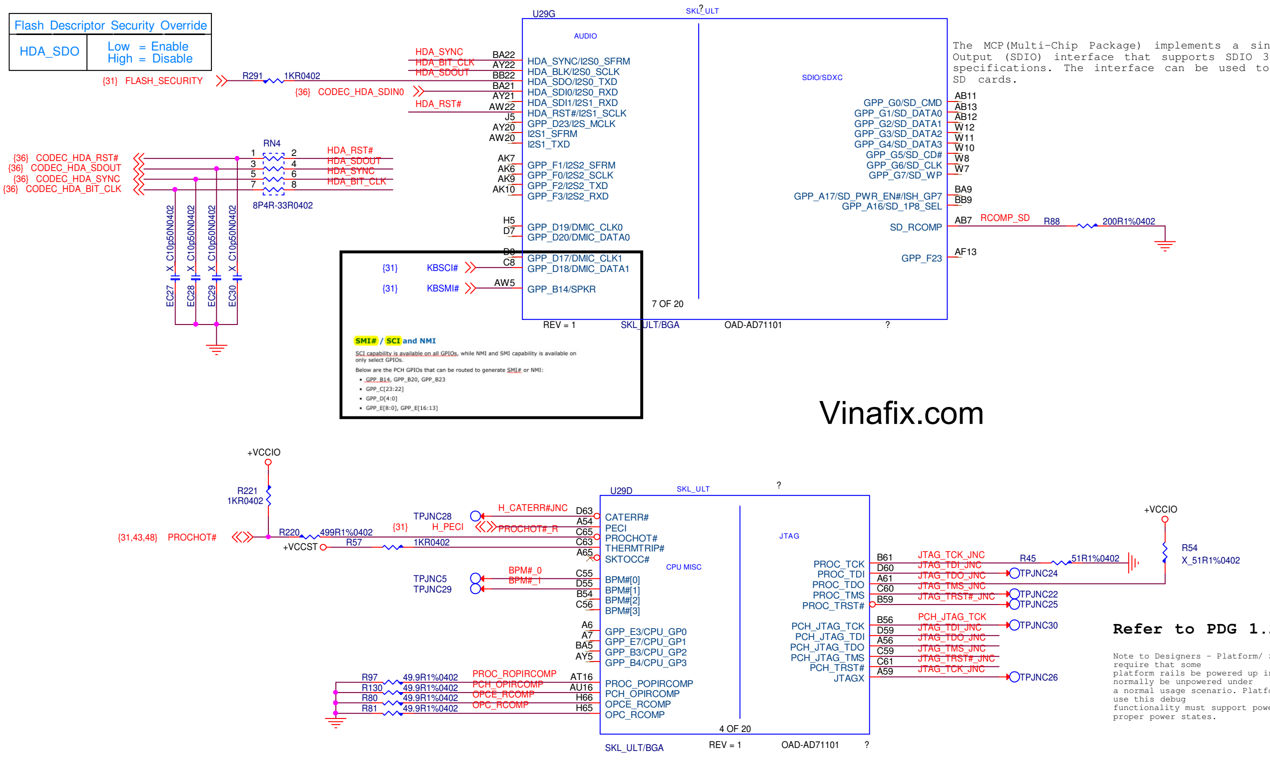

The MCP(Multi-Chip Package) implements a single Secure Digital Input Output (SDIO) interface that supports SDIO 3.01 and SDXC 3.01 specifications. The interface can be used to support either Wi-Fi or SD cards.

Refer to PDG 1.2 (page 625)

Note to Designers - Platform/ Silicon debug functionality may require that some platform rails be powered up in states where they would normally be unpowered under a normal usage scenario. Platforms that require the ability to use this debug functionality must support powering the proper rails in the proper power states.

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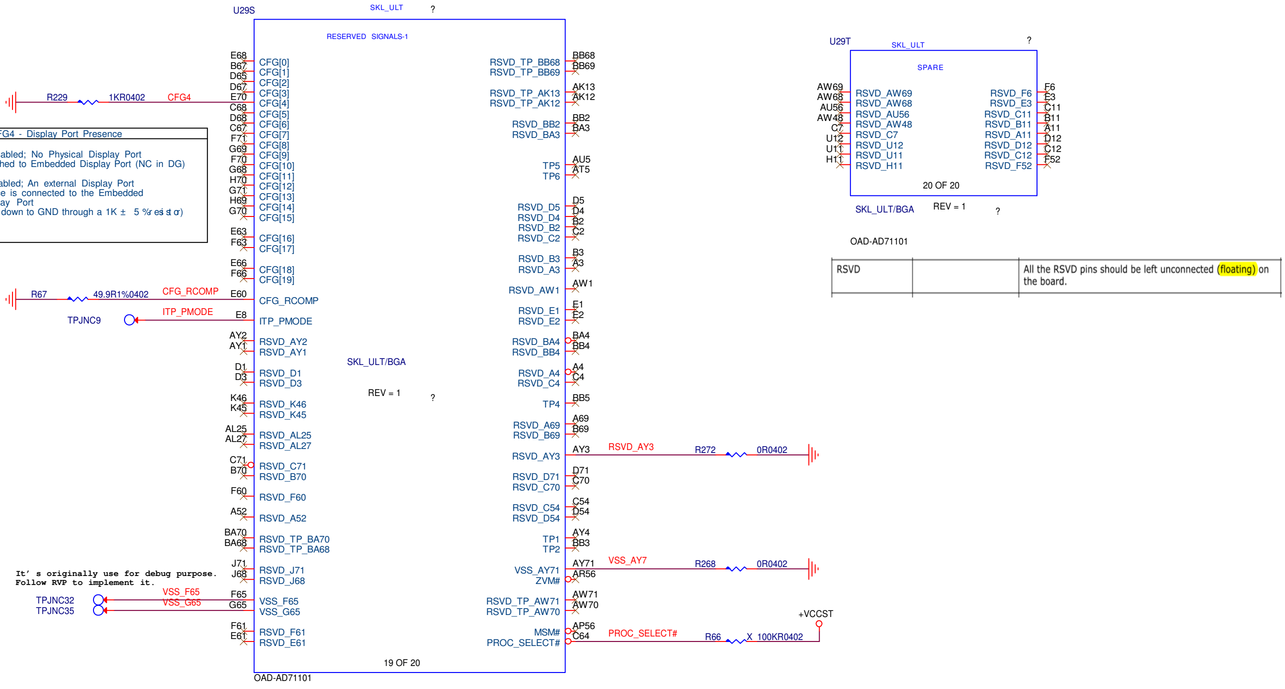
MSI Link to the Future	MICRO-STAR INT'L CO.,LTD.	
Title	Skylake-U (HDA, MISC, JTAG)	
Size B	Document Number MS-13F2	Rev 10
Date: Tuesday, February 23, 2016	Sheet 11 of 60	



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (NC in DG) 0:Enabled; An external Display Port device is connected to the Embedded Display Port (Pull down to GND through a 1K ± 5 %resistor)

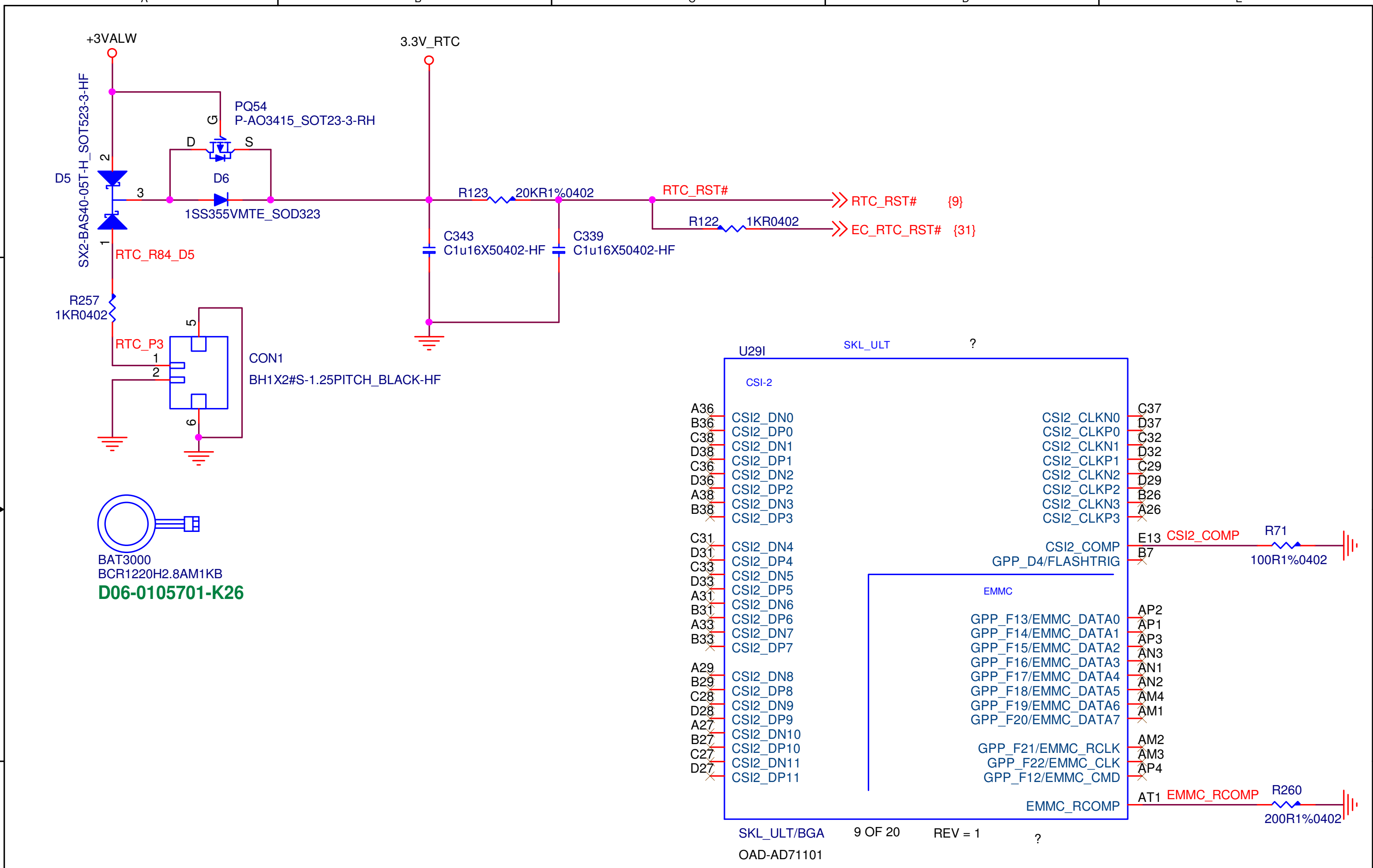
RSVD		All the RSVD pins should be left unconnected (floating) on the board.

MICRO-STAR INT'L CO.,LTD.

Title: **Skylake-U (CFG / RVSD)**

Size: B | Document Number: **MS-13F2** | Rev: 10

Date: Tuesday, February 23, 2016 | Sheet 12 of 60



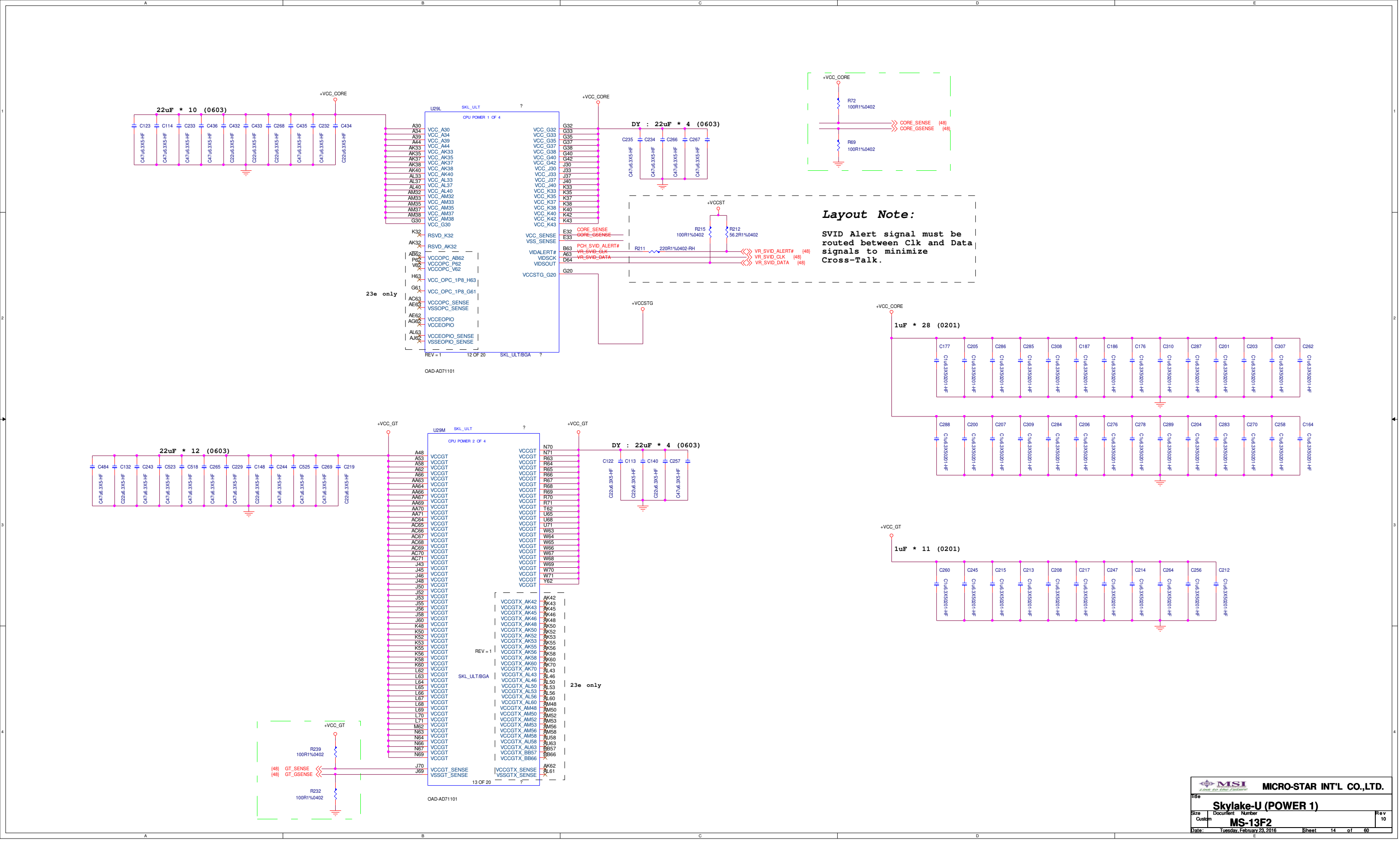
MICRO-STAR INT'L CO.,LTD.

Title

Skylake-U (RTC, CSI, EMMC)

Size	Document Number	Rev
A	MS-13F2	10

Date: Tuesday, February 23, 2016 Sheet 13 of 60


22uF * 10 (0603)
+VCC_CORE
CPU POWER 1 OF 4
DY : 22uF * 4 (0603)
23e only
Layout Note:
SVID Alert signal must be routed between Clk and Data signals to minimize Cross-Talk.
CORE_SENSE
CORE_GSENSE
VR_SVID_ALERT#
VR_SVID_CLK
VR_SVID_DATA
+VCCST
+VCCSTG
1uF * 28 (0201)
+VCC_GT
22uF * 12 (0603)
CPU POWER 2 OF 4
DY : 22uF * 4 (0603)
1uF * 11 (0201)
GT_SENSE
GT_GSENSE
MICRO-STAR INT'L CO.,LTD.
Skylake-U (POWER 1)
MS-13F2
Tuesday, February 23, 2016
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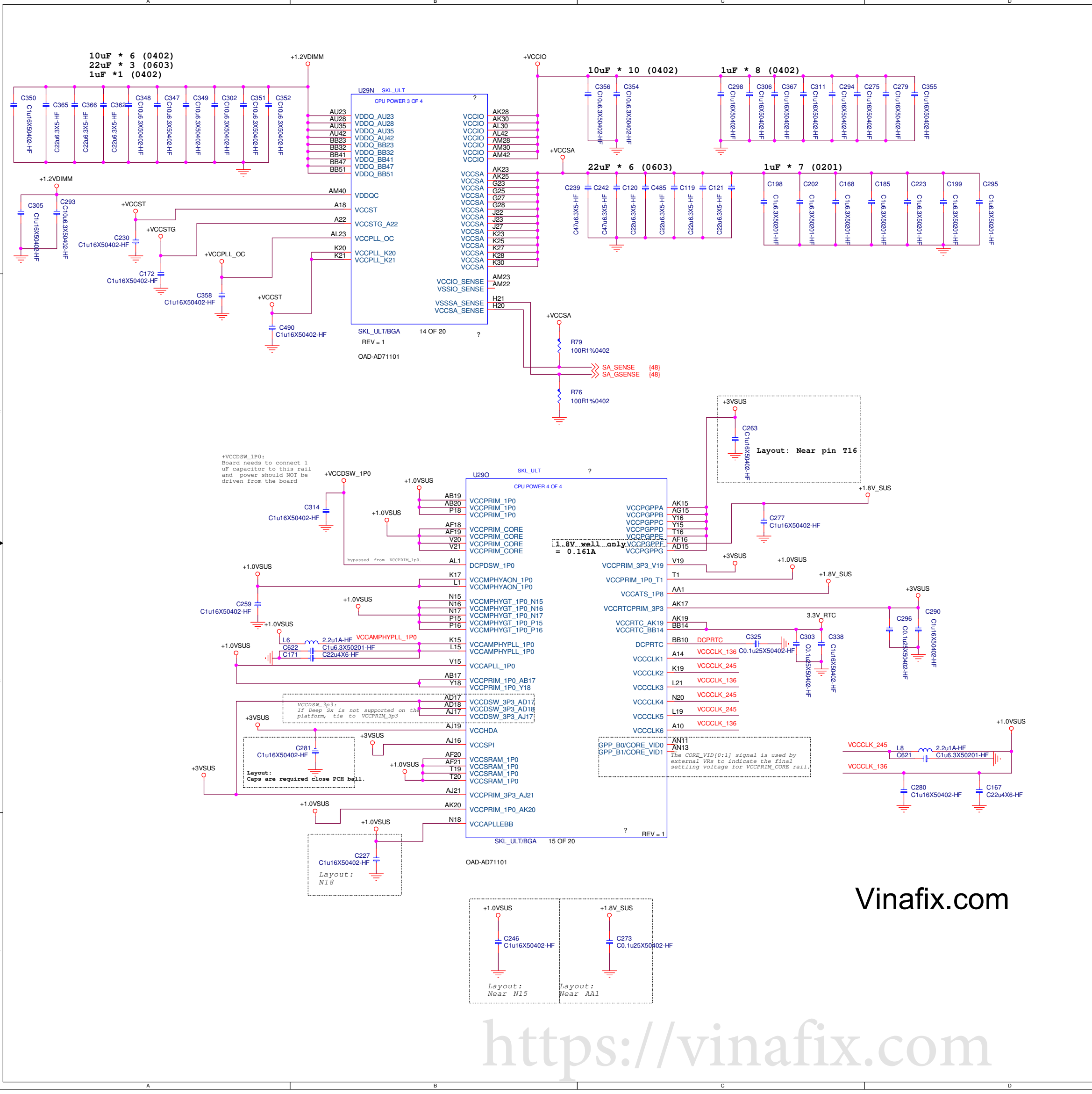
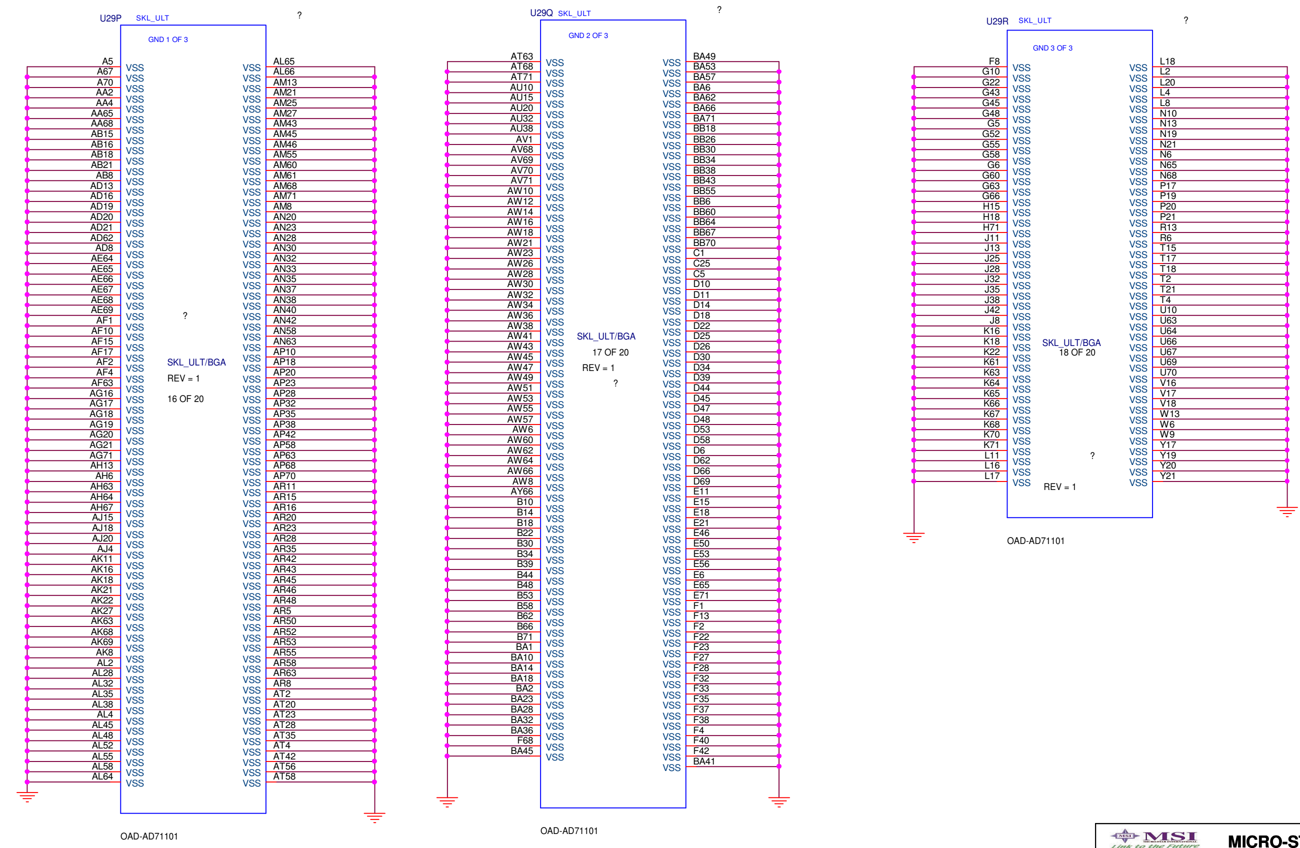


Name	Description
VCCPRIM_CORE	**Core Logic Primary Well:** This rail scales from 0.85V to 1.0V.
VCCPRIM_1p0	**Primary Well 1.0V:** For I/O blocks, ungated ISH SRAM power, USB AFE Digital Logic, JTAG, Thermal Sensor and MIPI DPHY.
VCCSRAM_1p0	**SRAM Primary Well 1.0V:** Dedicated SRAM rail and can have on board power down gate control.
VCCMPHYAON_1p0	**Mod PHY Always On Primary 1.0V**: Always on primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic
VCCMPHYGT_1p0	**Mod PHY Externally Gated Primary 1.0V**: Externally gated primary supply for PCIe/DMI/USB3/SATA/MIPI MPHY logic.
VCCAMPHYPLL_1p0	**Analog supply for USB3, PCIe Gen 2/Gen 3, SATA3 and MIPI PLL 1.0V:** This rail is from externally gated domain. Filtering required.
VCCAPLLEBB_1p0	**PCIe* PLL EBB Primary 1.0:** EBB contains primary supply for PCIe PLL dividers and lane drivers.
VCCAPLL_1p0	**Analog supply for OPI, USB2 and Audio PLL Primary 1.0V:** Filtering required.
VCCCLK1, VCCCLK2, VCCCLK3, VCCCLK4, VCCCLK5, VCCCLK6	**Clock Buffers Primary 1.0V**
VCCPGPPA	**Group A Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPB	**Group B Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPC	**Group C Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPD	**Group D Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPE	**Group E Primary Well GPIOs 3.3V or 1.8V**
VCCPGPPF	**Group F Primary Well GPIOs 1.8V only**
VCCPGPPG	**Group G Primary Well GPIOs 3.3V or 1.8V**
VCCATS	**Thermal Sensor Primary Well 1.8V**
VCCHDA	**HD Audio Power 3.3V, 1.8V, 1.5V.** For Intel High Definition Audio.
VCCSPI	**SPI Primary Well 3.3V or 1.8V**
VCCPRIM_3p3	**Primary Well 3.3V**
VCCRTCPRIM_3p3	**RTC Logic Primary Well 3.3V.** This power supplies the RTC internal VRM. It will be off during Deep Sx mode.
DCPDSW_1p0	**Deep Sx Well 1.0V:** This rail is generated by on die DSW low dropout (LDO) linear voltage regulator to supply DSW GPIOs, DSW core logic and DSW USB2 logic. Board needs to connect 1 uF capacitor to this rail and power should NOT be driven from the board. When primary well power is up, this rail is bypassed from VCCPRIM_1p0.
VCCDSW_3p3	**Deep Sx Well for GPD GPIOs and USB2**
DCPRTC	**RTC de-coupling capacitor only.** This rail should NOT be driven.

Name	Description
VCCRTC	**RTC Well Supply.** This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained. ***Note:*** VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-coin battery designs. ***Note:*** Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTCRST# or GPI.
VSS	**Ground**

MICRO-STAR INT'L CO.,LTD.

Title	Skylake-U (POWER 2)	
Size C	Document Number MS-13F2	Rev 10
Date: Tuesday, February 23, 2016	Sheet 15 of 60	



MSI
MICRO-STAR INT'L CO.,LTD.

Title	Skylake-U (GND)	
Size B	Document Number MS-13F2	Rev 10
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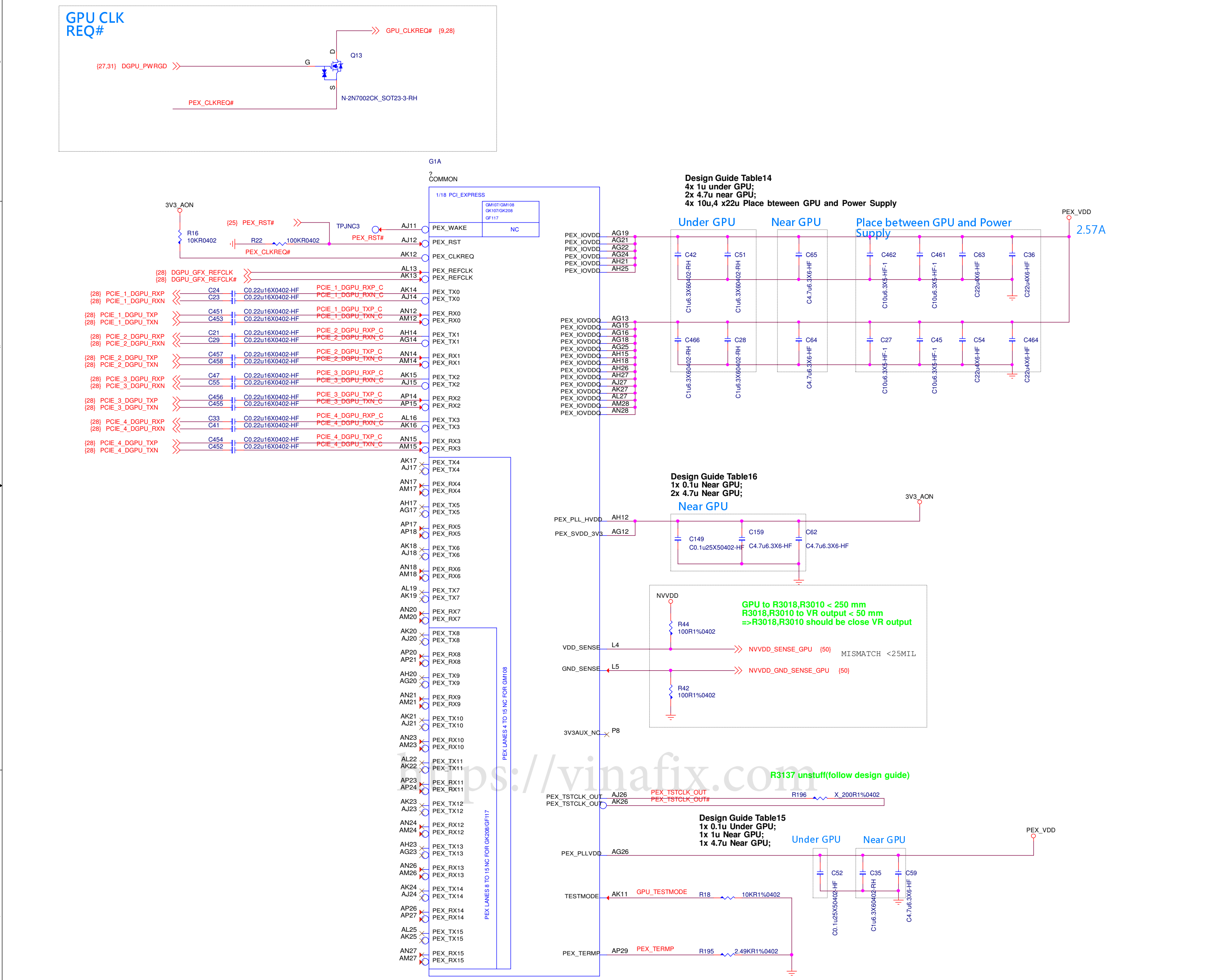
N16P-GX(PCI-Express Gen3 x16 Interface)



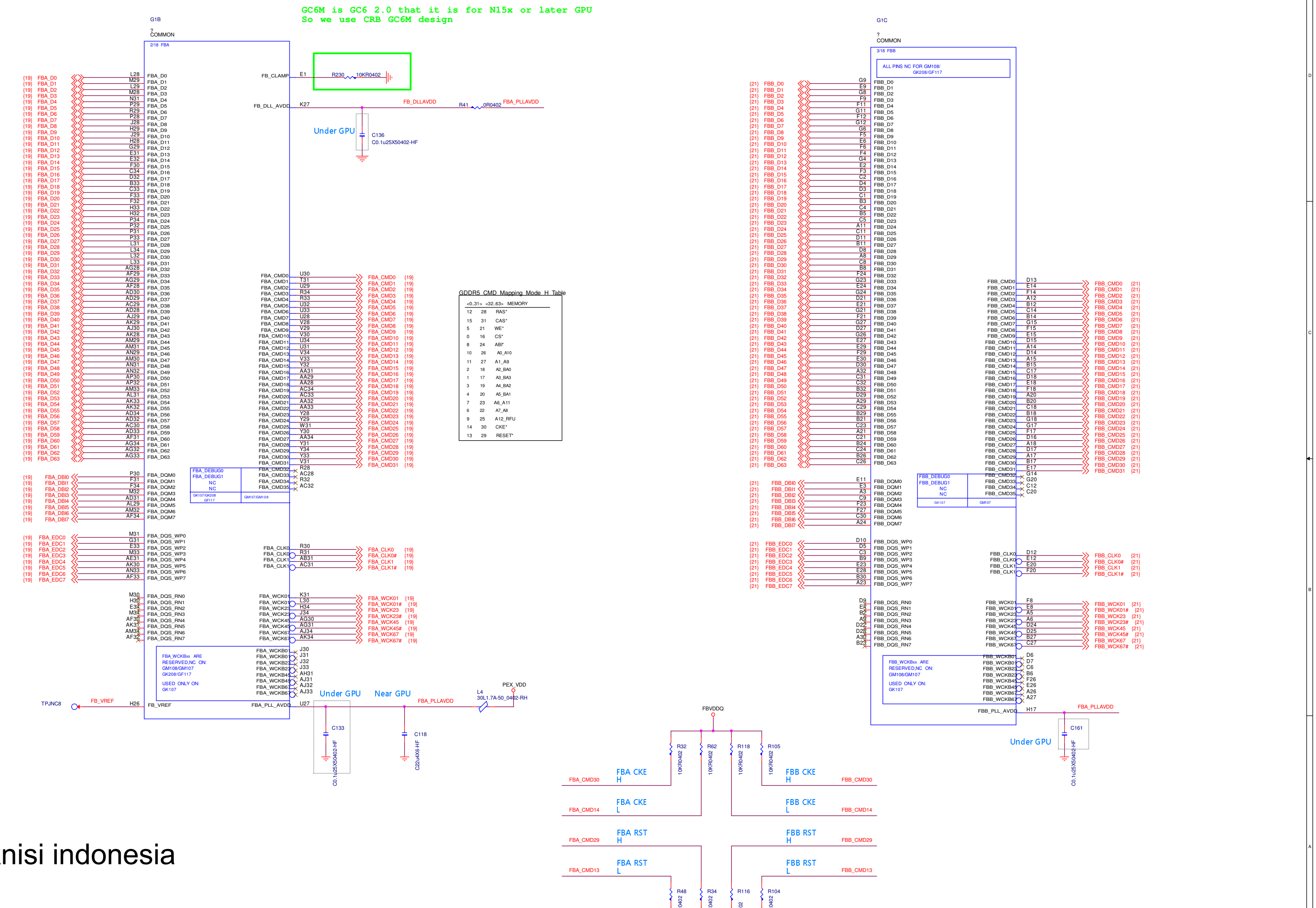
msi MICRO-STAR INT'L CO.,LTD.

Title: N16P-GX PCI-E Host

Size: Custom | Document Number: MS-13F2 | Rev: 10

Date: Tuesday, February 23, 2016 | Sheet 17 of 60

N16P-GX(Frame Buffer Interface)



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MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX MEM IF A/B	
Size Custom	Document Number MS-13F2	Rev 10
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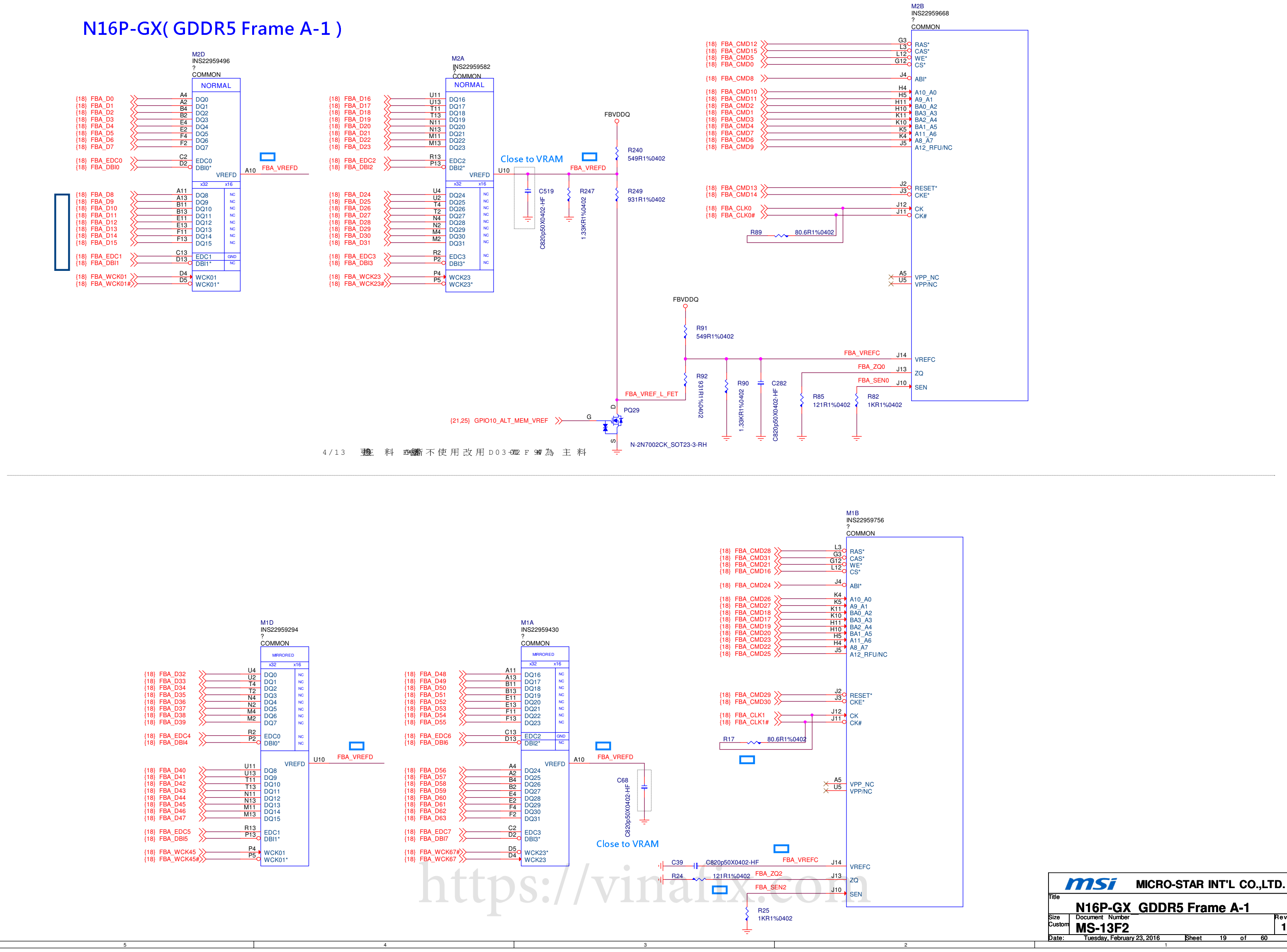
N16P-GX(GDDR5 Frame A-1)



MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_GDDR5 Frame A-1
Size Custom	Document Number MS-13F2
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Date:	Tuesday, February 23, 2016
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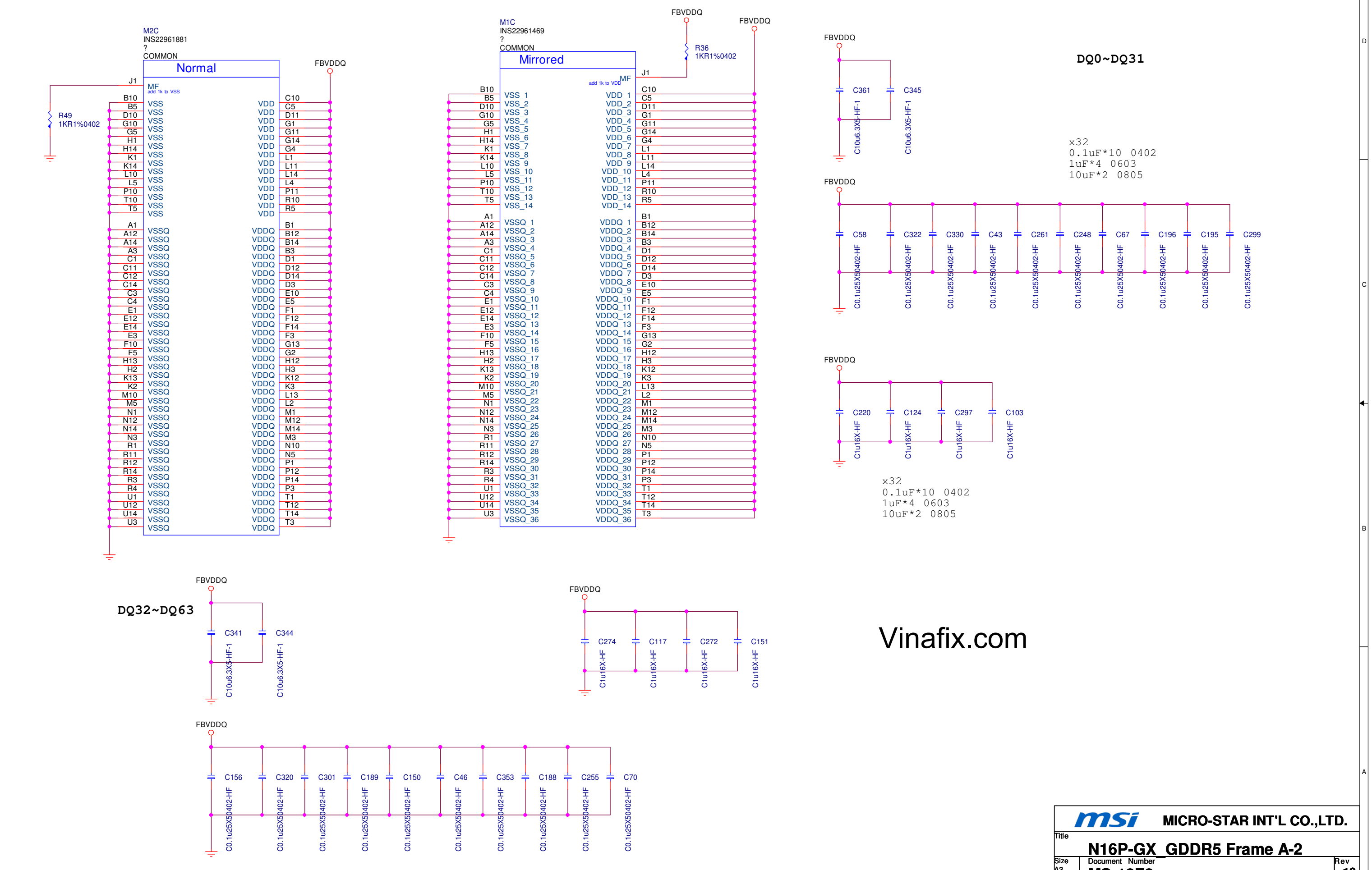
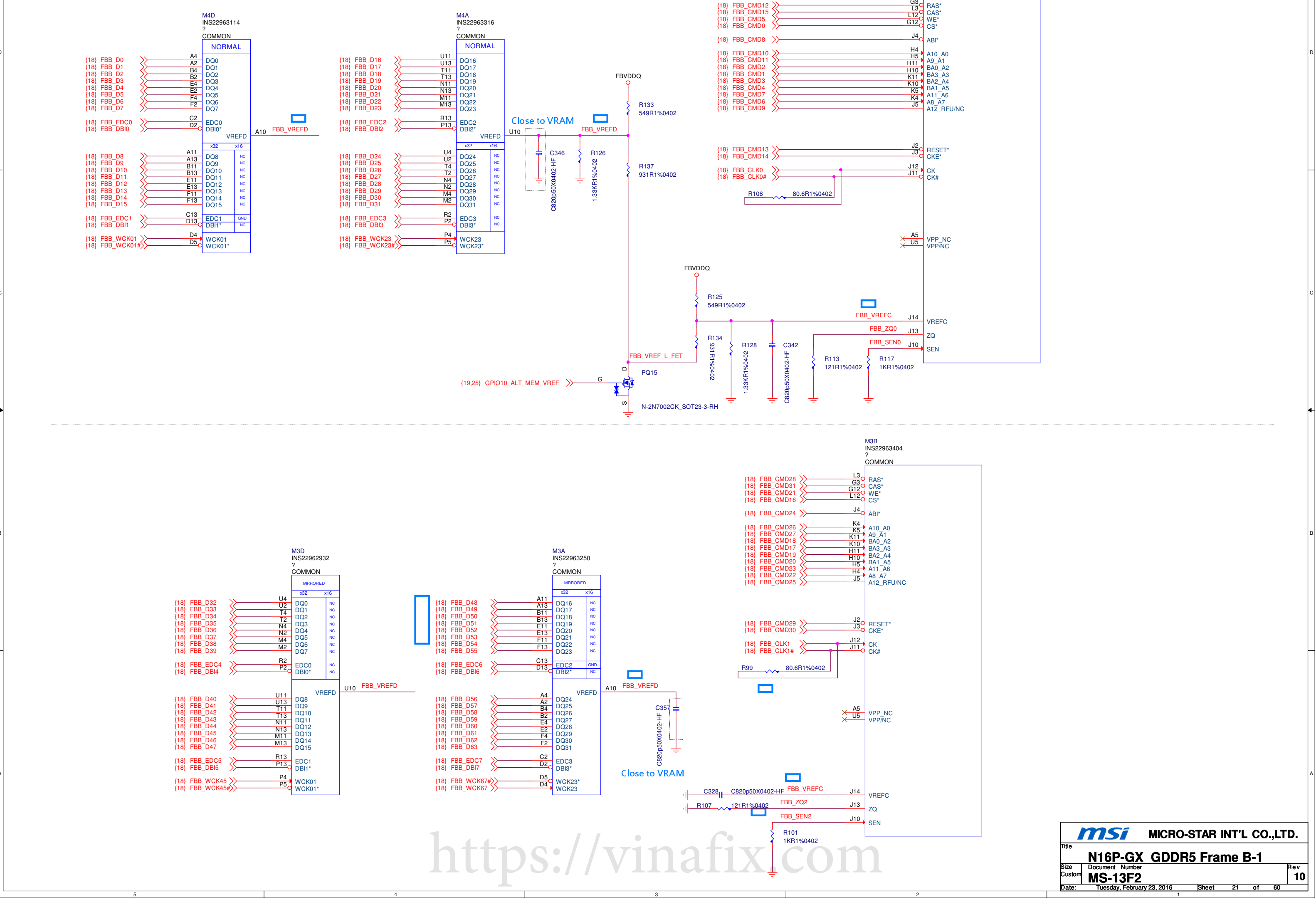
N16P-GX(GDDR5 Frame A-2)

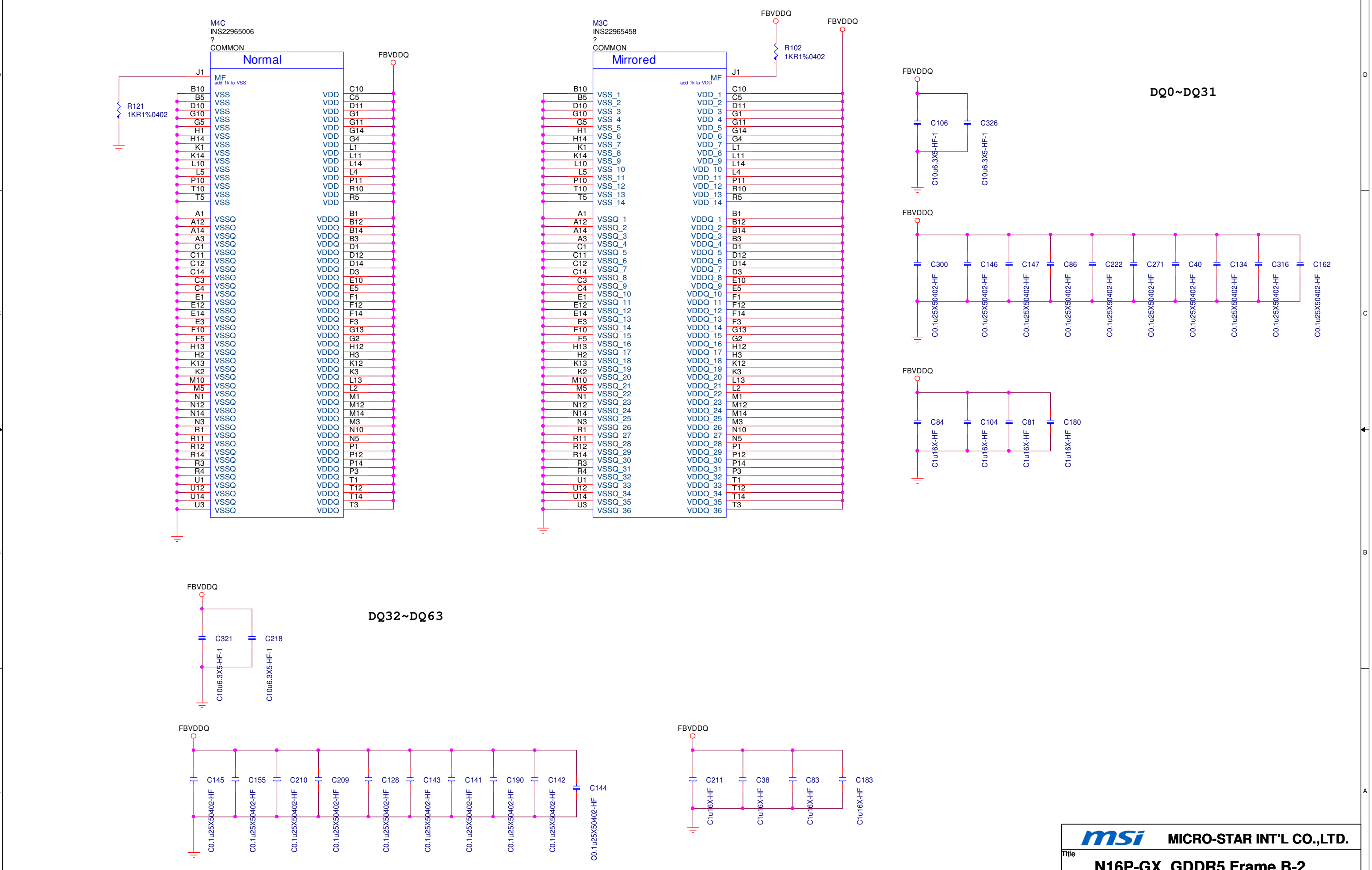


msi	MICRO-STAR INT'L CO.,LTD.	
Title	N16P-GX_GDDR5 Frame A-2	
Size A3	Document Number MS-13F2	Rev 10
Date: Tuesday, February 23, 2016	Sheet 20 of 60	

N16P-GX(GDDR5 Frame B-1)



N16P-GX(GDDR5 Frame B-2)



MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_GDDR5 Frame B-2	
Size A3	Document Number MS-13F2	Rev 10
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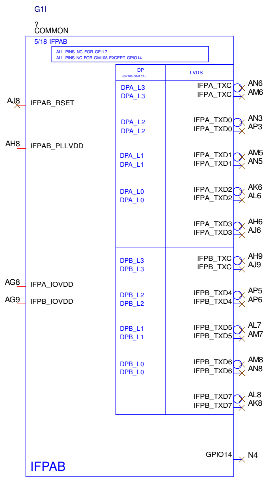
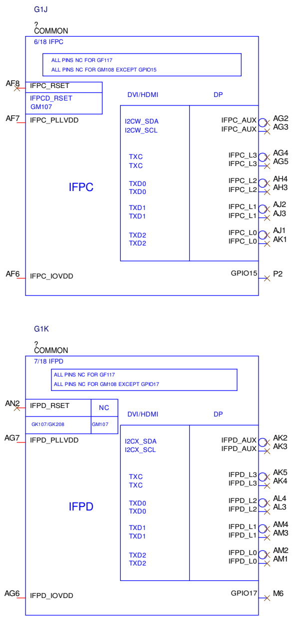
N16P-GX(Display IF)

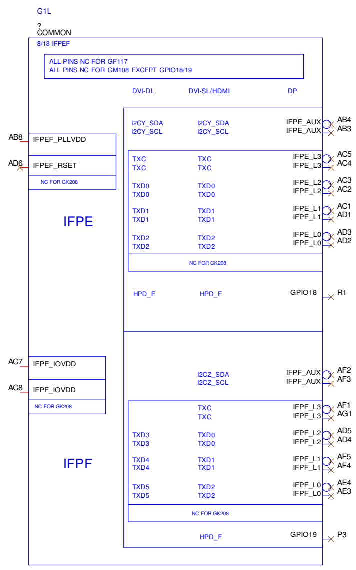
IFP A/B LVDSDual Link



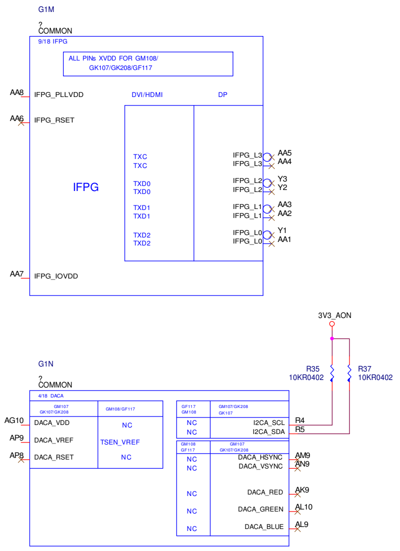
IFP C Native HDMI OR DP



IFP E/F Dual Link TMDS DVI-I



DAC A VGA



msi	MICRO-STAR INT'L CO.,LTD.
Title	N16P-GX_Display IF
Size Custom	Document Number MS-13F2	Rev 10
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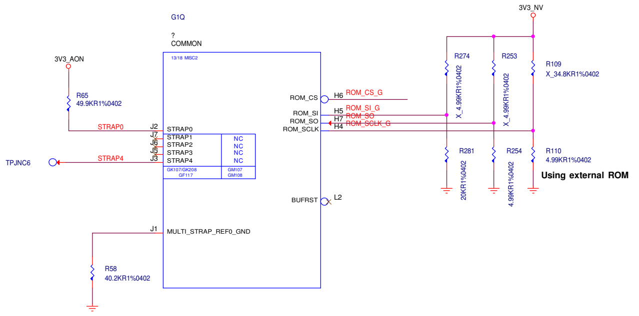
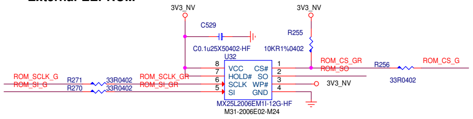
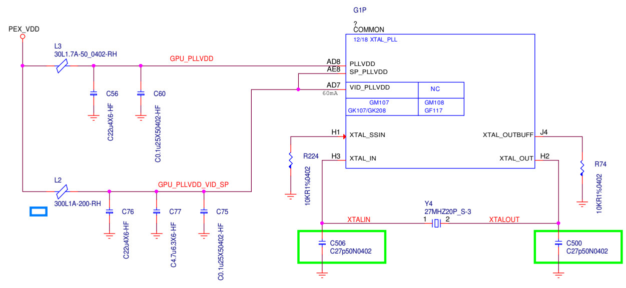
ROM, MULTI-LEVEL STRAPS



External EEPROM



M31-2006E02-M24



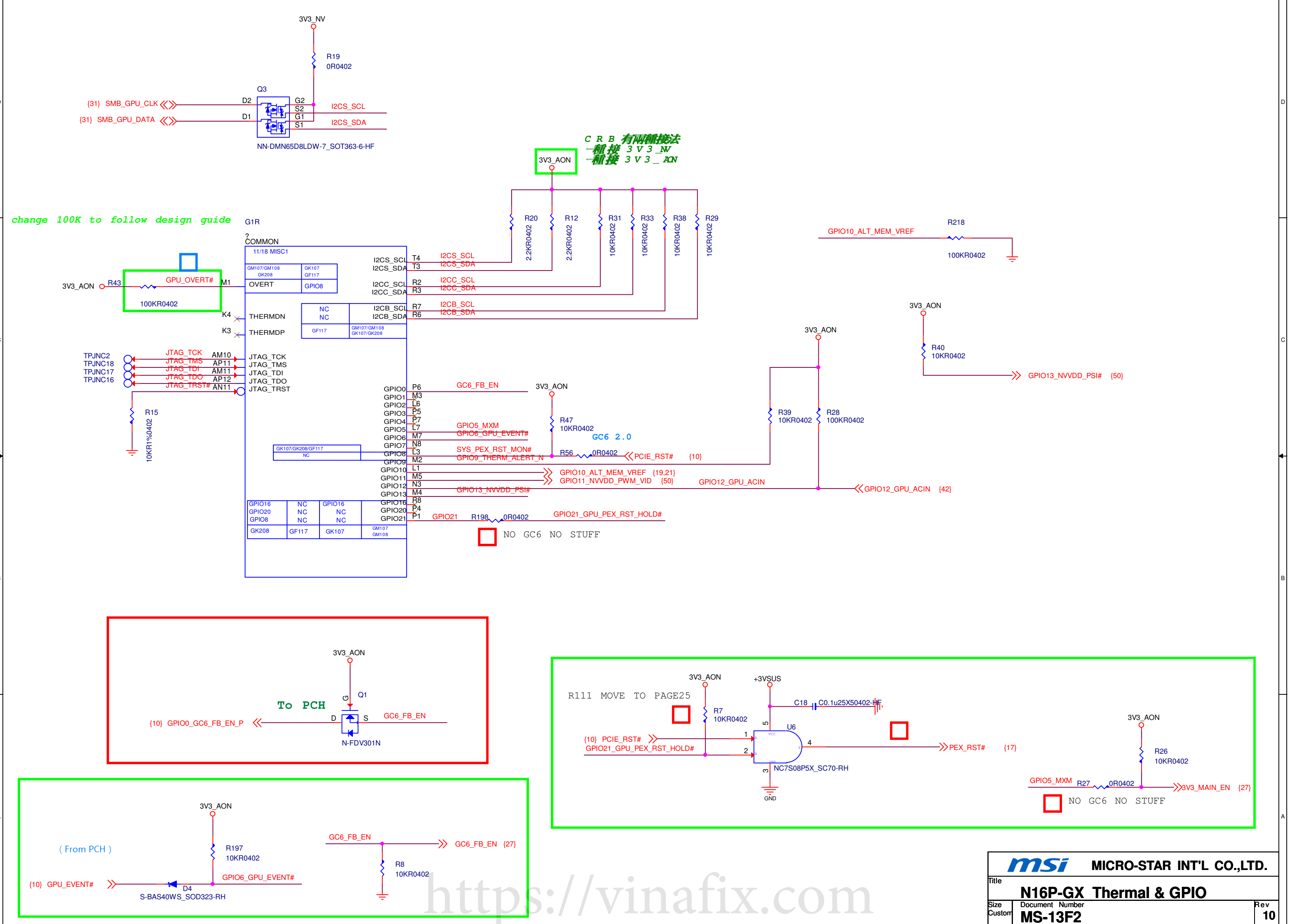
C3438 and C3439 change to 27pF for SA

ROM_SI	RAM_CFG[3:0]		
128Mx32bit (16S-GTR/16P-GT) **Samsung GDDR5 : M12-4132525-S02** **Hynix GDDR5 : M12-5GC4H65-H23**		0x4 24.9K PD 0x3 20K PD 0x6 35K PD	Micron 128Mx32bit Samsung 128Mx32bit Hynix 128Mx32bit
ROM_SO	DEVID_SEL PCIE_CFG SMB_ALT_ADDR VGADEVICE	5K PD	
ROM_SCLK	SOR_EXposed[3:0]	5K PD	
STRAP0		50K PU 3V3_AON	
STRAP1		Reserved	
STRAP2		Reserved	
STRAP3		Reserved	
STRAP4		Reserved	

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX ROM & HW Straps	
Size Custom	Document Number MS-13F2	Rev 10
Date: Tuesday, February 23, 2016	Sheet 24 of 60	



MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX Thermal & GPIO
Size	Custom
Document Number	MS-13F2
Rev	10
Date:	Tuesday, February 23, 2016
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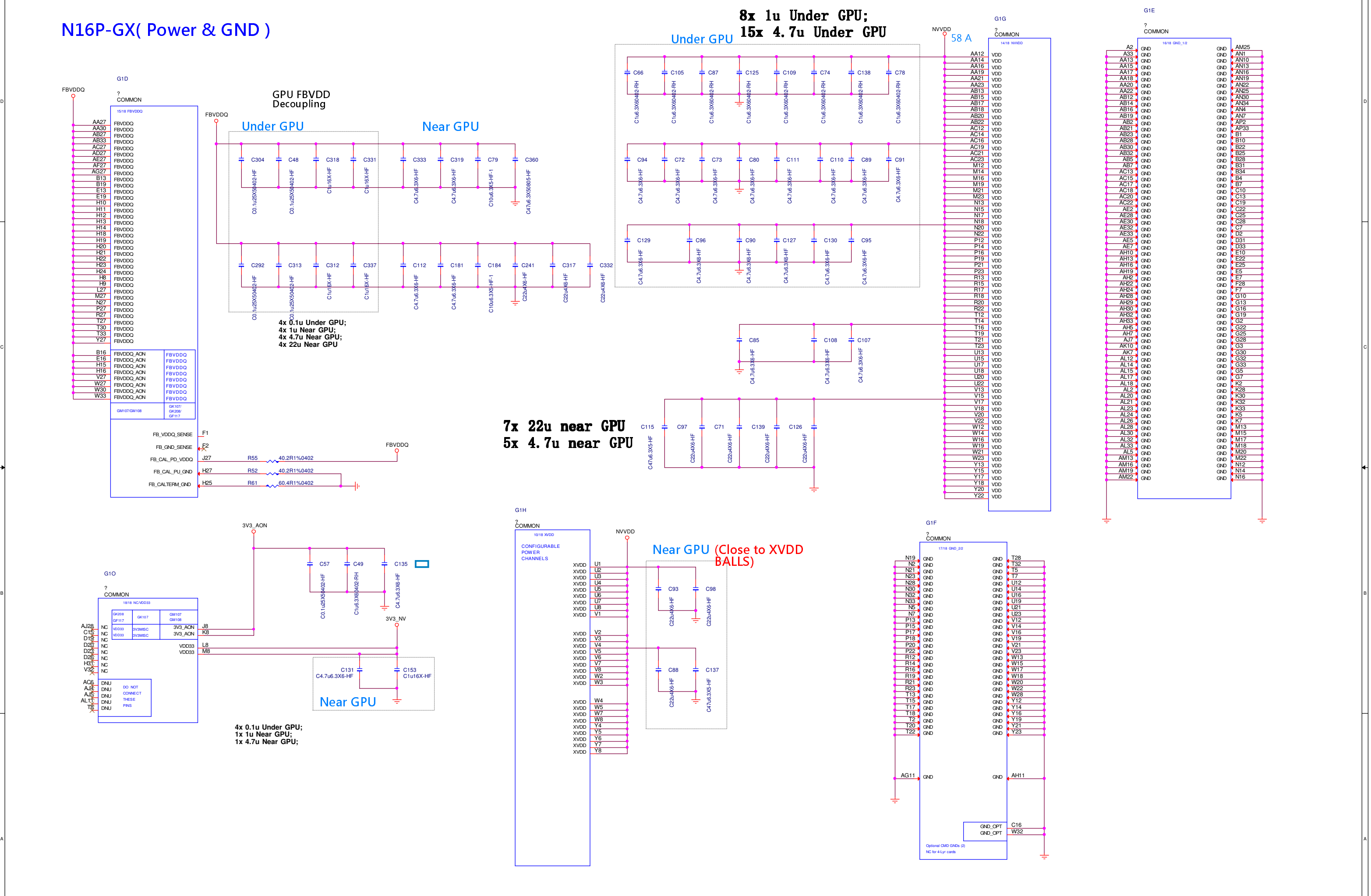
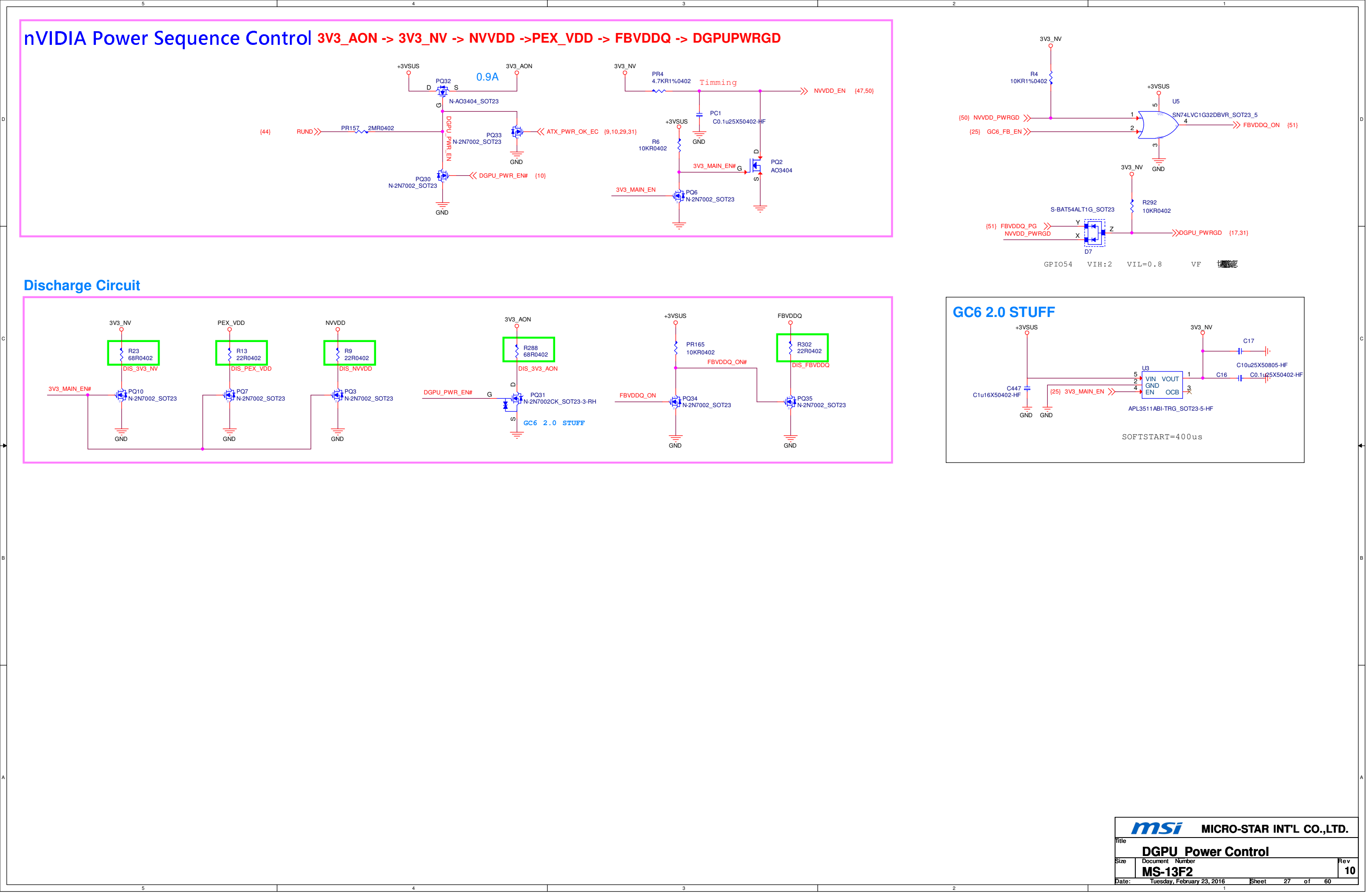


MICRO-STAR INT'L CO.,LTD.

Title: N16P-GX Power & GND

Size: Custom | Document Number: MS-13F2 | Rev: 10

Date: Tuesday, February 23, 2016 | Sheet 26 of 60


nVIDIA Power Sequence Control 3V3_AON -> 3V3_NV -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD
+3VSUS
3V3_AON
PQ32
0.9A
N-AO3404_SOT23
RUNO
PR157 2MR0402
DGPU_PWR_EN
PQ33
N-2N7002_SOT23
ATX_PWR_OK_EC (9,10,29,31)
PQ30
N-2N7002_SOT23
DGPU_PWR_EN# (10)
GND
3V3_NV
PR4
4.7KR1%0402
Timming
NVVDD_EN (47,50)
PC1
C0.1u25X50402-HF
R6
10KR0402
3V3_MAIN_EN#
PQ2
AO3404
3V3_MAIN_EN
PQ6
N-2N7002_SOT23
R4
10KR1%0402
U5
SN74LVC1G32DBVR_SOT23_5
(50) NVVDD_PWRGD
(25) GC6_FB_EN
FBVDDQ_ON (51)
R292
10KR0402
S-BAT54ALT1G_SOT23
(51) FBVDDQ_PG
NVVDD_PWRGD
D7
DGPU_PWRGD (17,31)
GPIO54 VIH:2 VIL=0.8 VF
Discharge Circuit
3V3_NV
R23
68R0402
DIS_3V3_NV
3V3_MAIN_EN#
PQ10
N-2N7002_SOT23
PEX_VDD
R13
22R0402
DIS_PEX_VDD
PQ7
N-2N7002_SOT23
NVVDD
R9
22R0402
DIS_NVVDD
PQ3
N-2N7002_SOT23
R288
68R0402
DIS_3V3_AON
DGPU_PWR_EN#
PQ31
N-2N7002CK_SOT23-3-RH
GC6 2.0 STUFF
PR165
10KR0402
FBVDDQ_ON#
FBVDDQ_ON
PQ34
N-2N7002_SOT23
FBVDDQ
R302
22R0402
DIS_FBVDDQ
PQ35
N-2N7002_SOT23
GC6 2.0 STUFF
C447
C1u16X50402-HF
U3
VIN VOUT
GND
EN OCB
(25) 3V3_MAIN_EN
C17
C10u25X50805-HF
C16
C0.1u25X50402-HF
APL3511ABI-TRG_SOT23-5-HF
SOFTSTART=400us
msi MICRO-STAR INT'L CO.,LTD.
Title
DGPU_Power Control
Size Document Number Rev
MS-13F2 10
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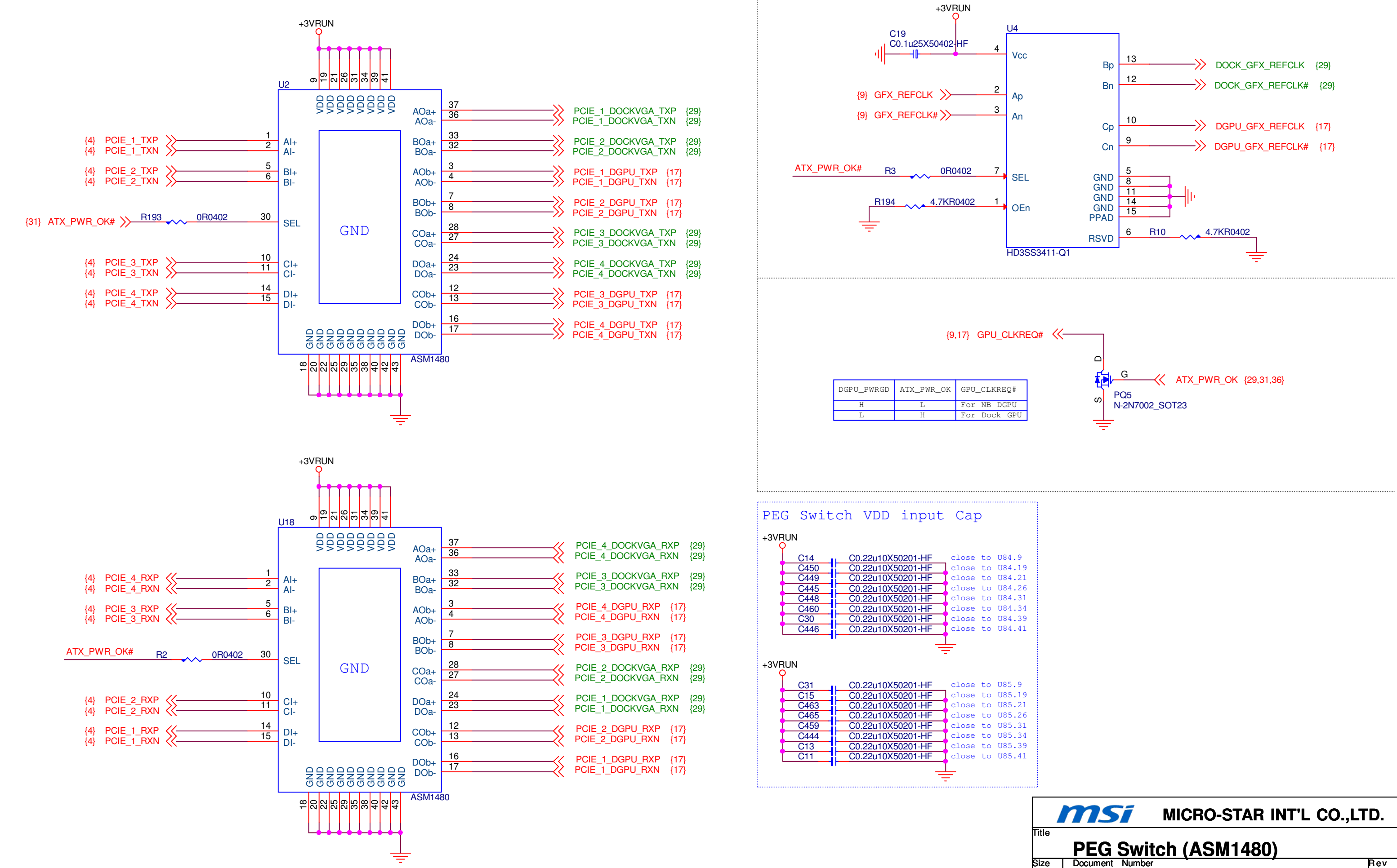
PCIE TX&RX SEL

SEL=0	Output = a	For Docking
SEL=1 (Default)	Output = b (Default)	For GTX950M

PCIE CLK SEL

SEL=0	Output = B	For Docking
SEL=1	Output = C	For GTX950M

OE#, RSVD operation: pull 4.7K to GND.
SEL, OE# pin:
VIH:2V~Vcc
VIL:-0.1V~0.8V



DGPU_PWRGD	ATX_PWR_OK	GPU_CLKREQ#
H	L	For NB DGPU
L	H	For Dock GPU

MICRO-STAR INT'L CO.,LTD.

Title	PEG Switch (ASM1480)
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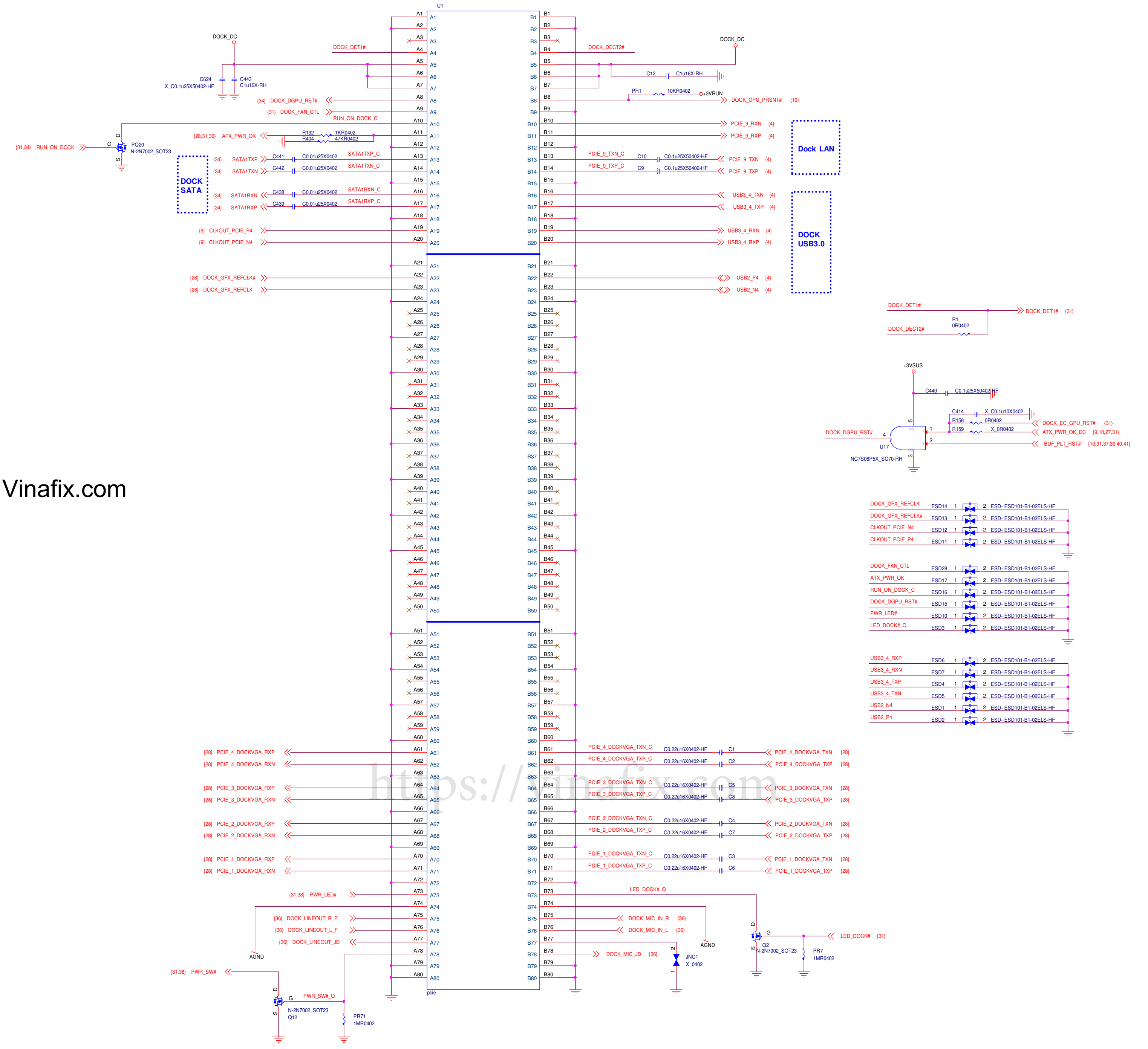
PCI-Express Gen3 x4 Interface



Title	Dock PCI-E Interface
Size: Custom	Document Number: MS-13F2
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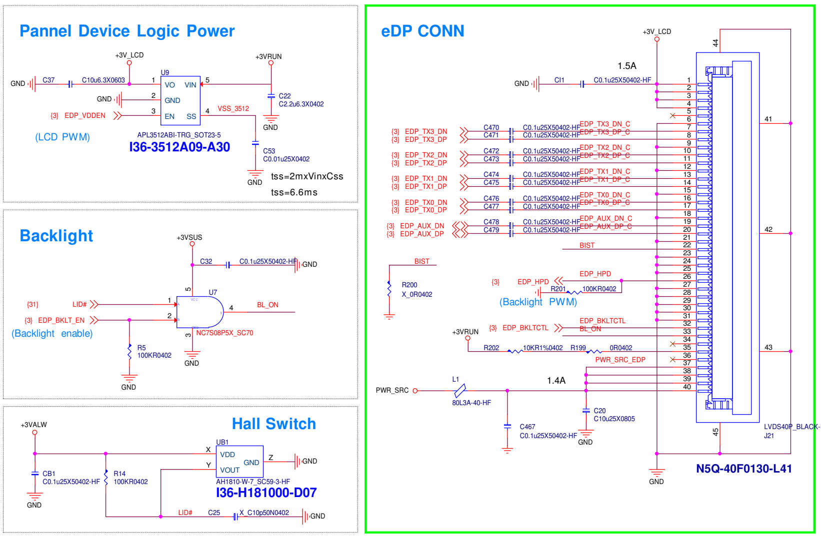
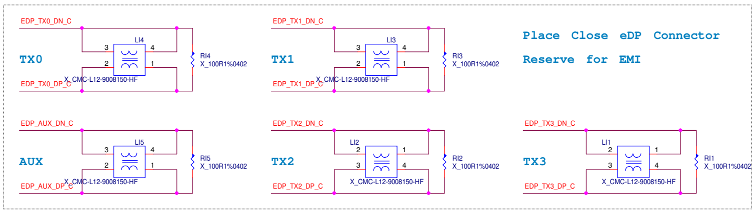
eDP Connector





LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	NC	No Connection (Reserved)

LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufactureer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/0ff
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer’ s use
35	NC	Reserved for LCD manufacturer’ s use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	NC	No Connection (Reserved)

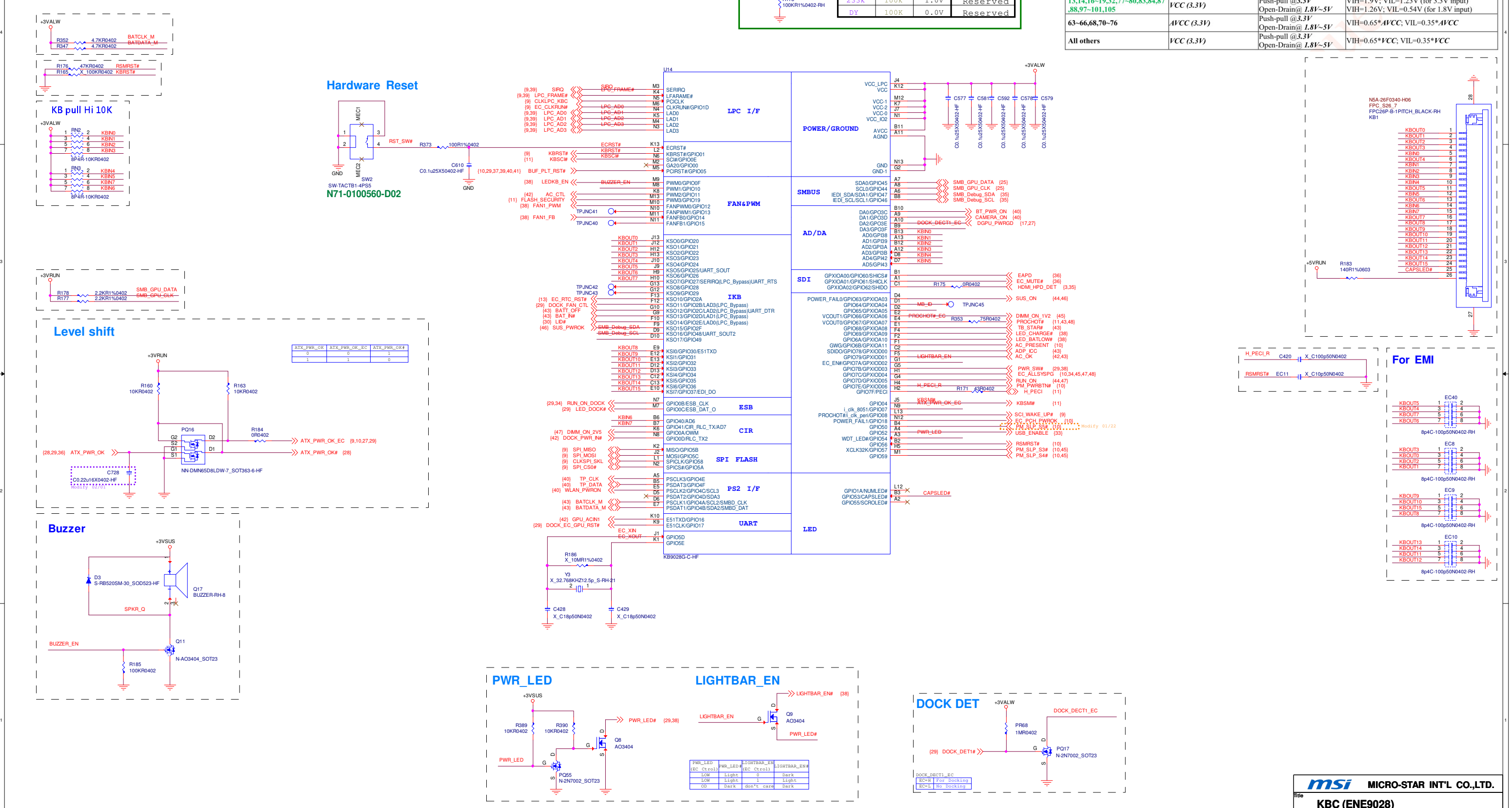
KBC/EC/uP (ENE9028)

PCB Ver. ID

Pull-up	Pull-low	MB_ID	Version
100k	DY	3.3V	0A
64.9k	100k	2.0V	Reserved
233k	100k	1.0V	Reserved
DY	100K	0.0V	Reserved

IO pin groups v.s Power planes:

Pin#	Power plane	Output Mode	Input Mode
3~8,10, 12	*VCC_LPC(1.8V or 3.3V)*	Push-pull @*1.8V or 3.3V* Open-Drain@ *1.8V~5V*	VIH=0.65**VCC_LPC*; VIL=0.35**VCC_LPC*
1,2,117,119~123, 126~128	*VCC_IO2 (1.8V or 3.3V)*	Push-pull @*1.8 or 3.3V* Open-Drain@ *1.8V~5V*	VIH=0.65**VCC_IO2*; VIL=0.35**VCC_IO2*
110,112,114,115,116	*VCC0 (3.3V)*	Push-pull @*3.3V* Open-Drain@ *1.8V~5V*	VIH=0.65**VCC0*; VIL=0.35 **VCC0*
13,14,16~19,32,77~80,83,84,87,88,97~101,105	*VCC (3.3V)*	Push-pull @*3.3V* Open-Drain@ *1.8V~5V*	VIH=1.9V; VIL=1.23V (for 3.3V input) VIH=1.26V; VIL=0.54V (for 1.8V input)
63~66,68,70~76	*AVCC (3.3V)*	Push-pull @*3.3V* Open-Drain@ *1.8V~5V*	VIH=0.65**AVCC*; VIL=0.35**AVCC*
All others	*VCC (3.3V)*	Push-pull @*3.3V* Open-Drain@ *1.8V~5V*	VIH=0.65**VCC*; VIL=0.35**VCC*



MICRO-STAR INT'L CO.,LTD.

Title	KBC (ENE9028)
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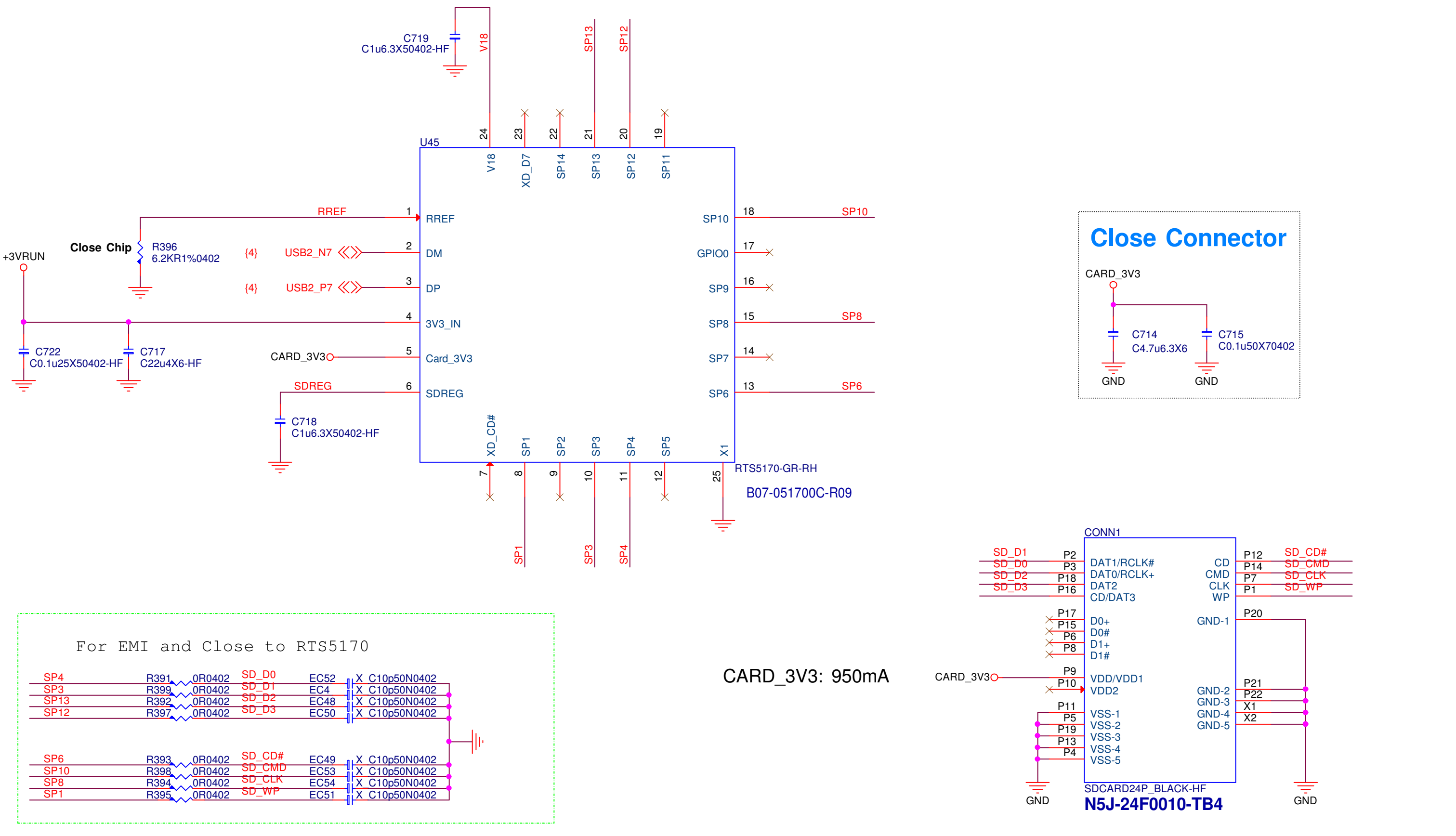
CardReader (RTS5170)



msi	MICRO-STAR INT'L CO.,LTD.
Title	Card Reader
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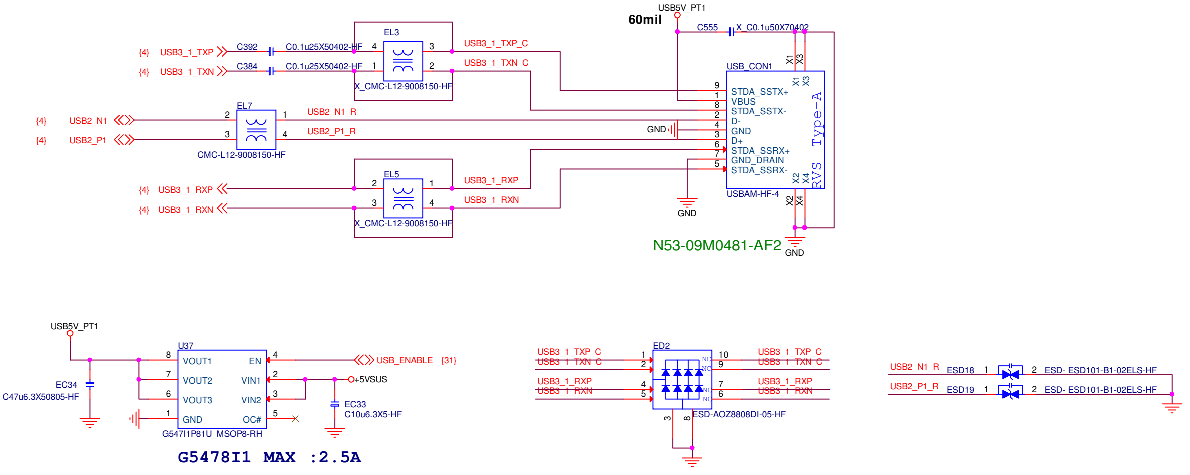
USB3.0 CNT-1



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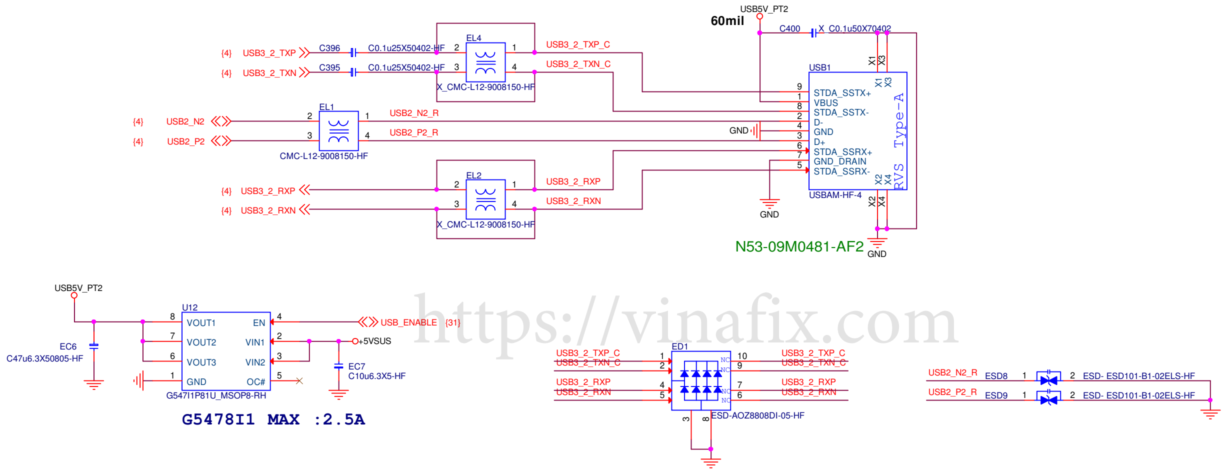
USB3.0 CNT-2



MICRO-STAR INT'L CO.,LTD.

Title	USB 3.0 connector
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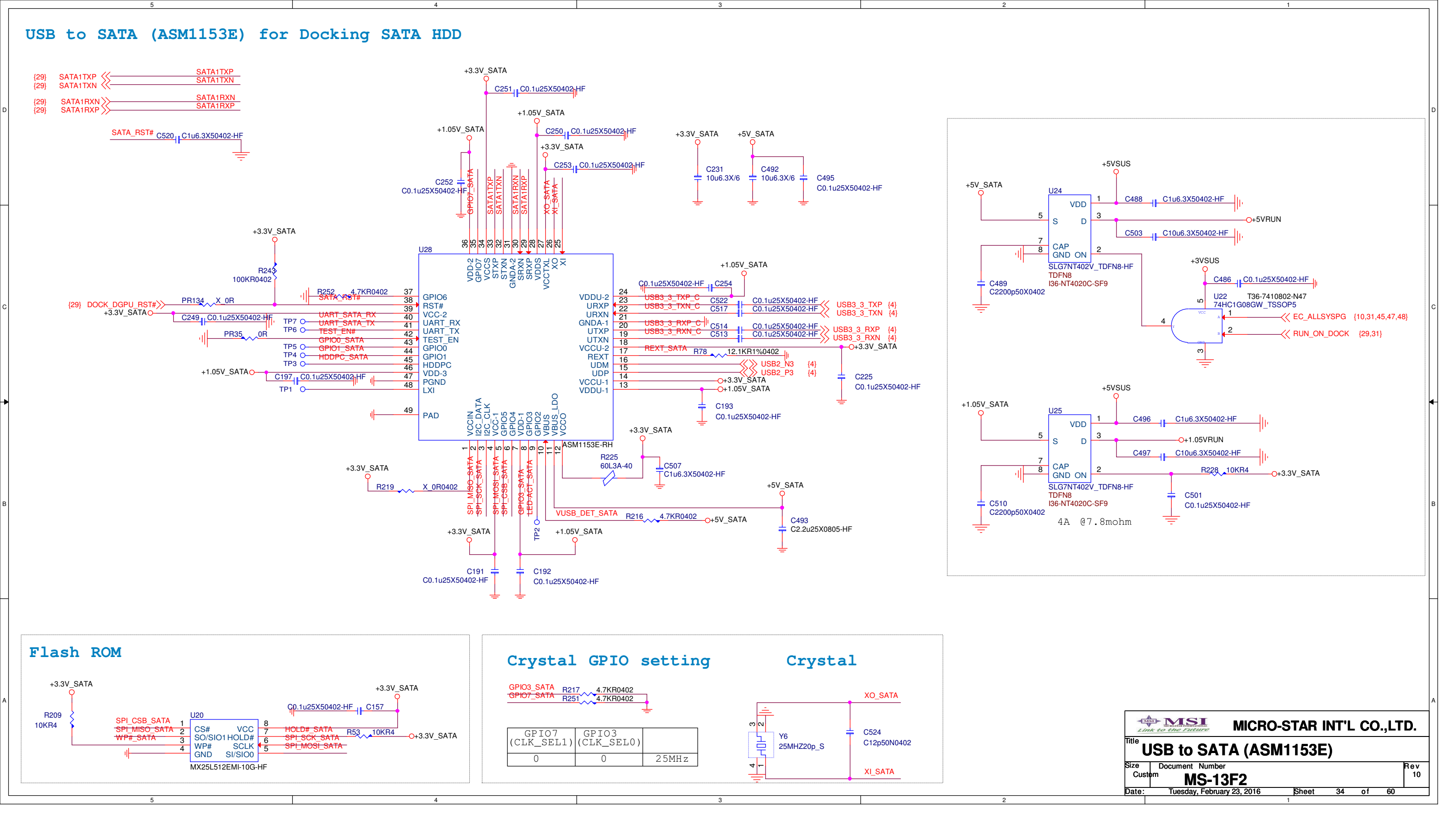
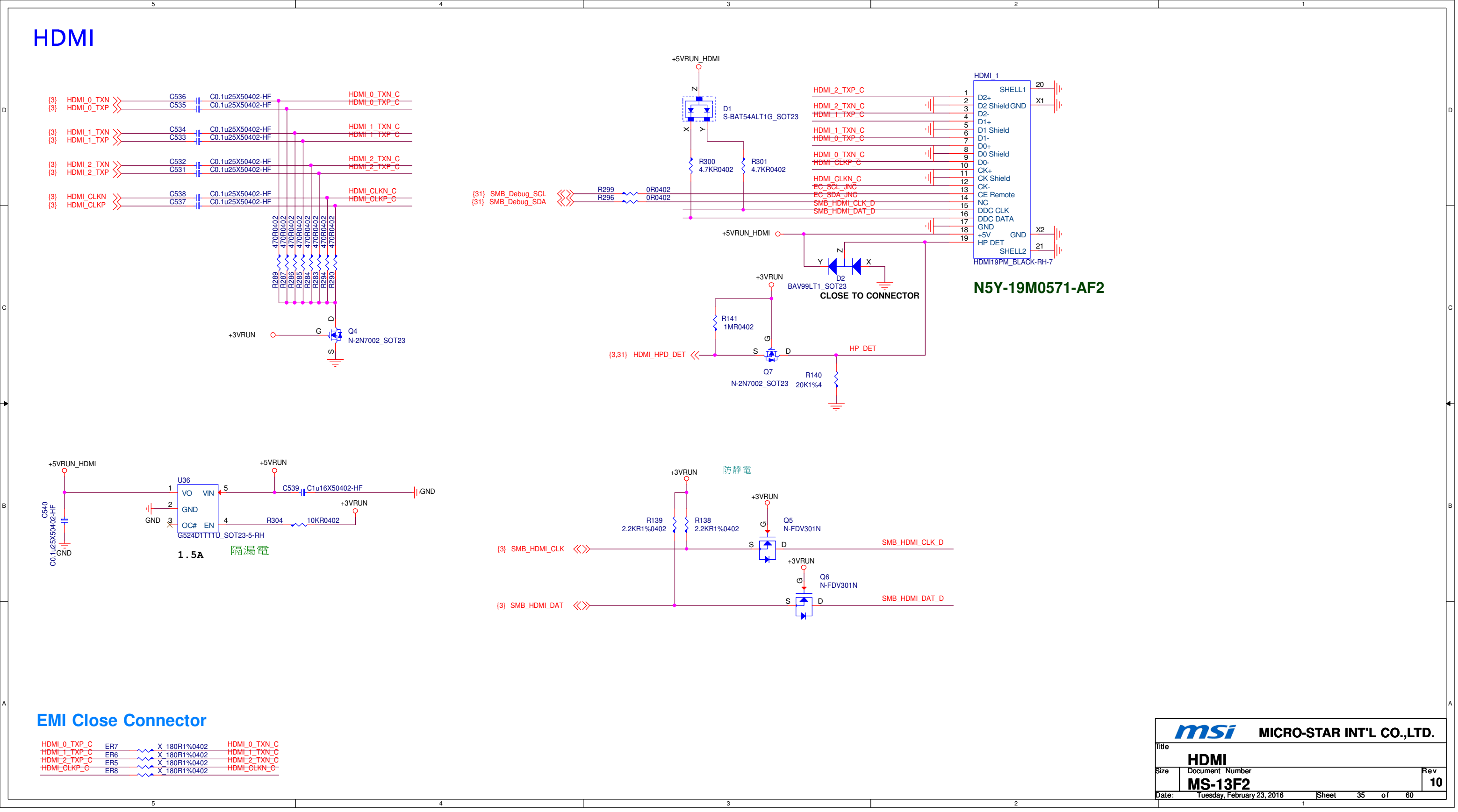


GPIO7 (CLK_SEL1)	GPIO3 (CLK_SEL0)	
0	0	25MHz


HDMI
HDMI_0_TXN
HDMI_0_TXP
HDMI_1_TXN
HDMI_1_TXP
HDMI_2_TXN
HDMI_2_TXP
HDMI_CLKN
HDMI_CLKP
C536
C535
C534
C533
C532
C531
C538
C537
C0.1u25X50402-HF
HDMI_0_TXN_C
HDMI_0_TXP_C
HDMI_1_TXN_C
HDMI_1_TXP_C
HDMI_2_TXN_C
HDMI_2_TXP_C
HDMI_CLKN_C
HDMI_CLKP_C
470R0402
R289
R287
R286
R285
R284
R283
R294
R290
+3VRUN
Q4
N-2N7002_SOT23
+5VRUN_HDMI
D1
S-BAT54ALT1G_SOT23
R300
4.7KR0402
R301
4.7KR0402
SMB_Debug_SCL
SMB_Debug_SDA
R299
R296
0R0402
EC_SCL_JNC
EC_SDA_JNC
SMB_HDMI_CLK_D
SMB_HDMI_DAT_D
HDMI_1
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL2
HDMI19PM_BLACK-RH-7
N5Y-19M0571-AF2
D2
BAV99LT1_SOT23
CLOSE TO CONNECTOR
R141
1MR0402
Q7
N-2N7002_SOT23
HDMI_HPD_DET
HP_DET
R140
20K1%4
U36
VO
VIN
GND
OC#
EN
G524D1T11U_SOT23-5-RH
1.5A
隔漏電
+5VRUN
C539
C1u16X50402-HF
R304
10KR0402
C540
C0.1u25X50402-HF
防靜電
R139
2.2KR1%0402
R138
2.2KR1%0402
Q5
N-FDV301N
Q6
N-FDV301N
SMB_HDMI_CLK
SMB_HDMI_DAT
EMI Close Connector
ER7
ER6
ER5
ER8
X_180R1%0402
msi
MICRO-STAR INT'L CO.,LTD.
Title
HDMI
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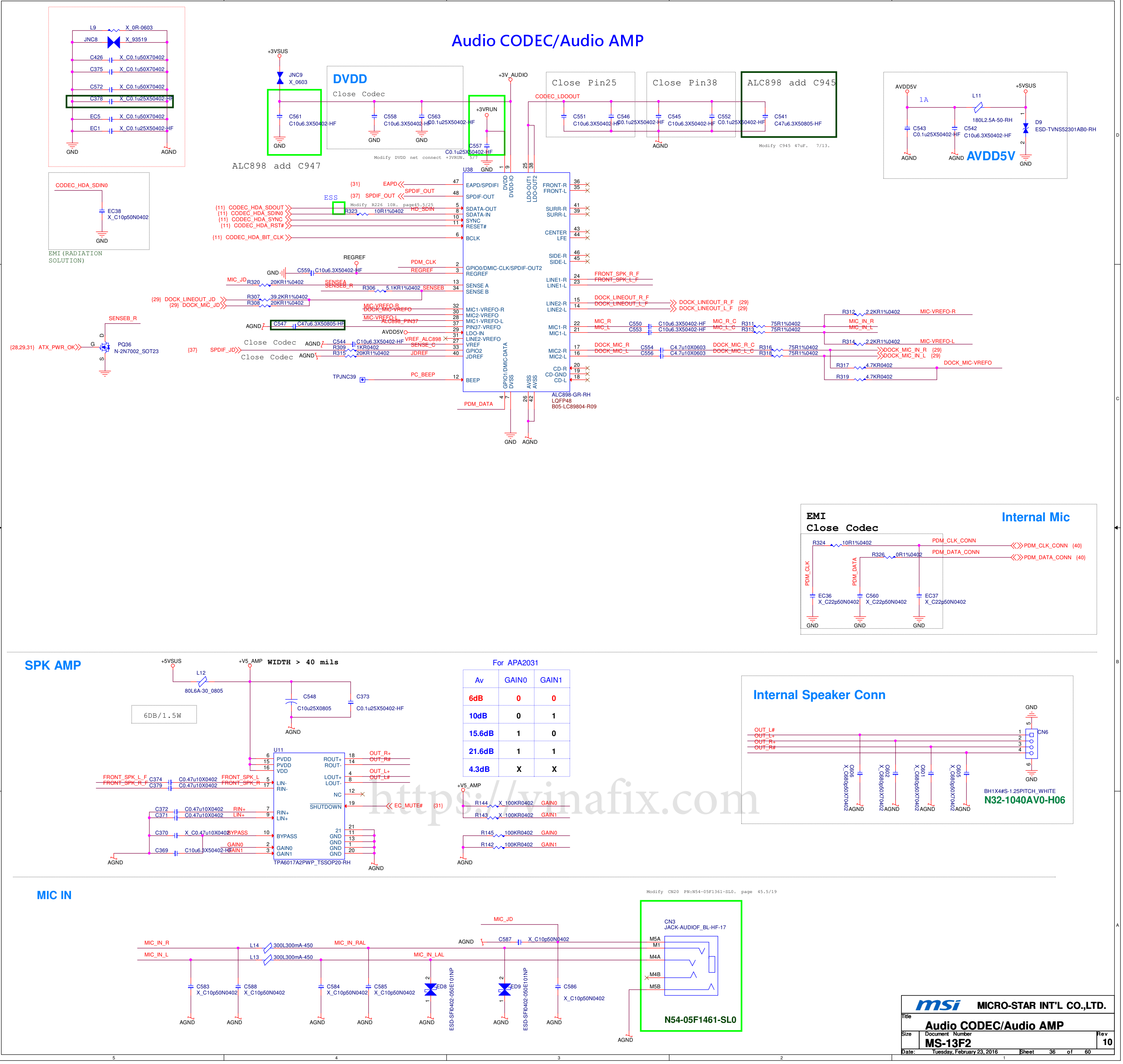
Audio CODEC/Audio AMP



For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

MICRO-STAR INT'L CO.,LTD.

Title: Audio CODEC/Audio AMP

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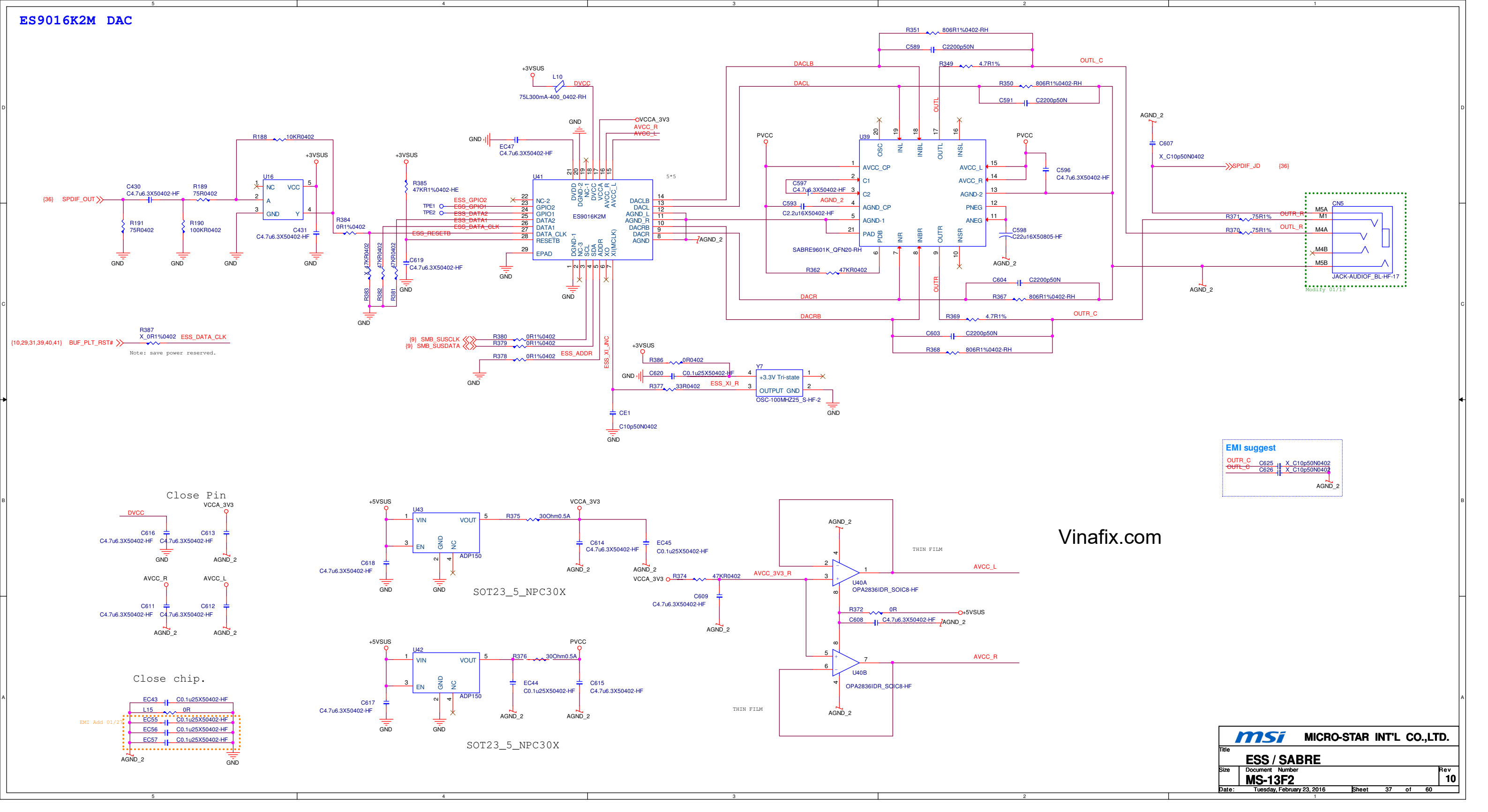

ES9016K2M DAC
SPDIF_OUT
BUF_PLT_RST#
ESS_DATA_CLK
Note: save power reserved.
U16
U41
ES9016K2M
U39
SABRE9601K_QFN20-RH
CN5
JACK-AUDIOF_BL-HF-17
SPDIF_JD
OUTR_R
OUTL_R
OUTL_C
OUTR_C
DACLB
DACL
DACR
DACRB
SMB_SUSCLK
SMB_SUSDATA
ESS_ADDR
ESS_XI_R
Y7
OSC-100MHZ25_S-HF-2
+3.3V Tri-state
EMI suggest
Close Pin
Close chip.
U43
U42
ADP150
SOT23_5_NPC30X
U40A
U40B
OPA2836IDR_SOIC8-HF
THIN FILM
AVCC_L
AVCC_R
AVCC_3V3_R
VCCA_3V3
DVCC
PVCC
+3VSUS
+5VSUS
AGND_2
GND
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MICRO-STAR INT'L CO.,LTD.
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ESS / SABRE
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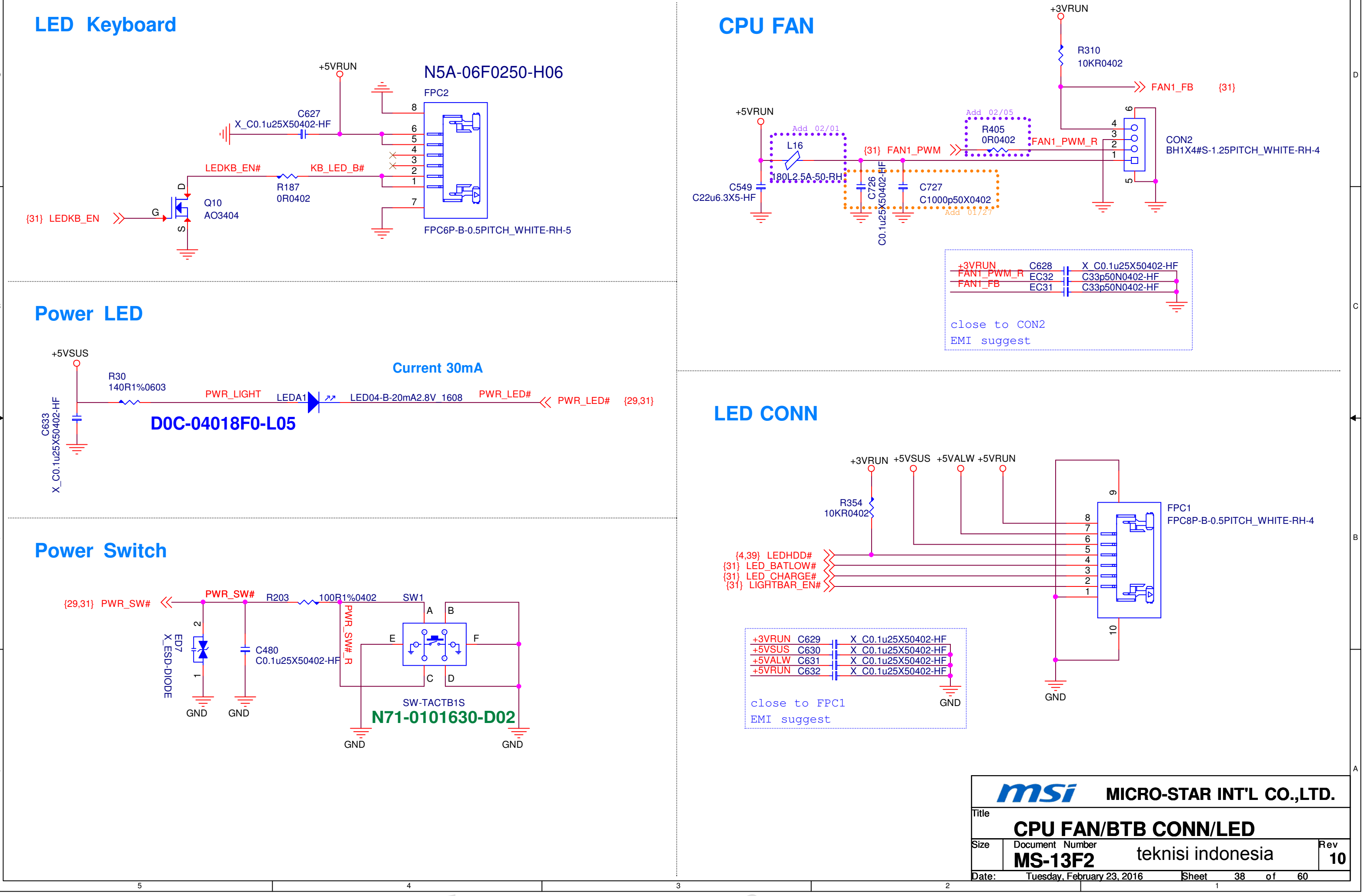
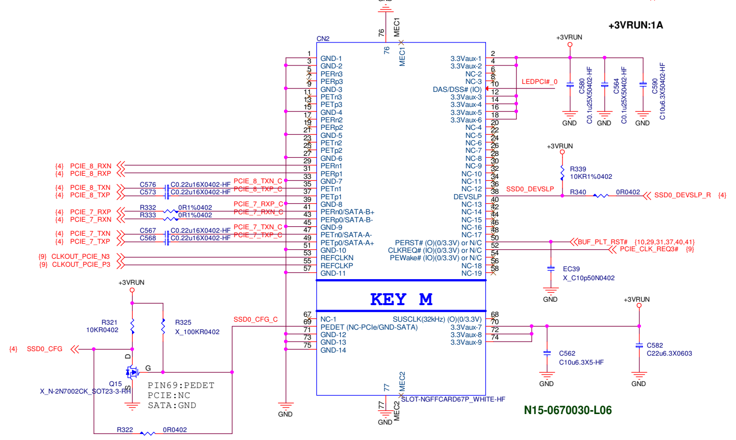
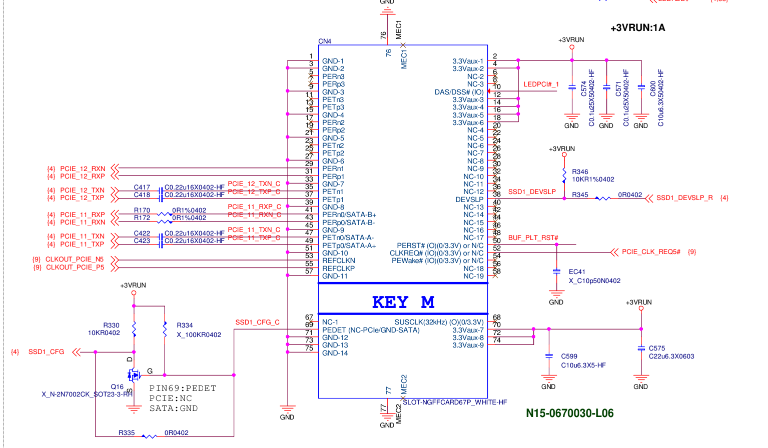
PWR SW/CPU FAN/BTB CONN/ LED CONN



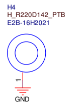
M2 SSD-1



M2 SSD-2

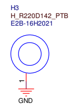


SSD Stand off

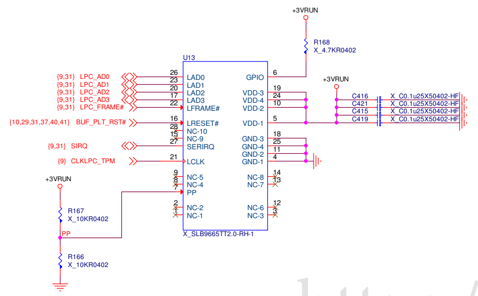


40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair

SSD Stand off



TPM



Physical Presence(PP)
The standard position of the jumper should connect the pin to GND. If the pin is connected to VDD, some special commands are enabled .

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Title	M2 SSD/TPM
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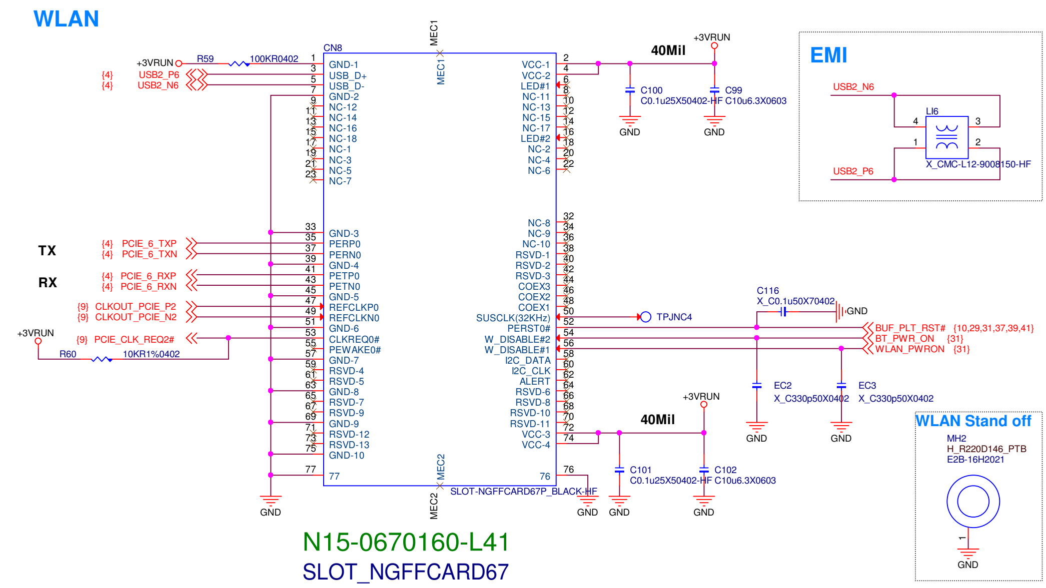
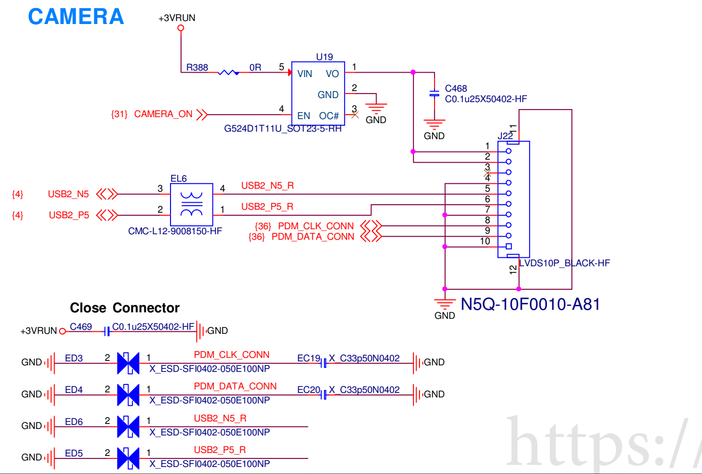
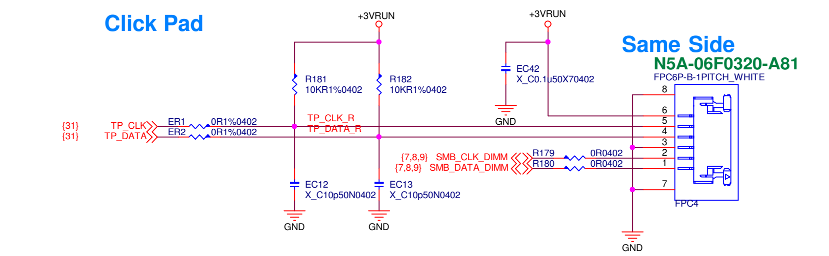
WLAN /Camera/ClickPad/FP



Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V





MICRO-STAR INT'L CO.,LTD.

Title		
WLAN /Camera/ClickPad		
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GIGA LAN(BFN2400/AR8171)

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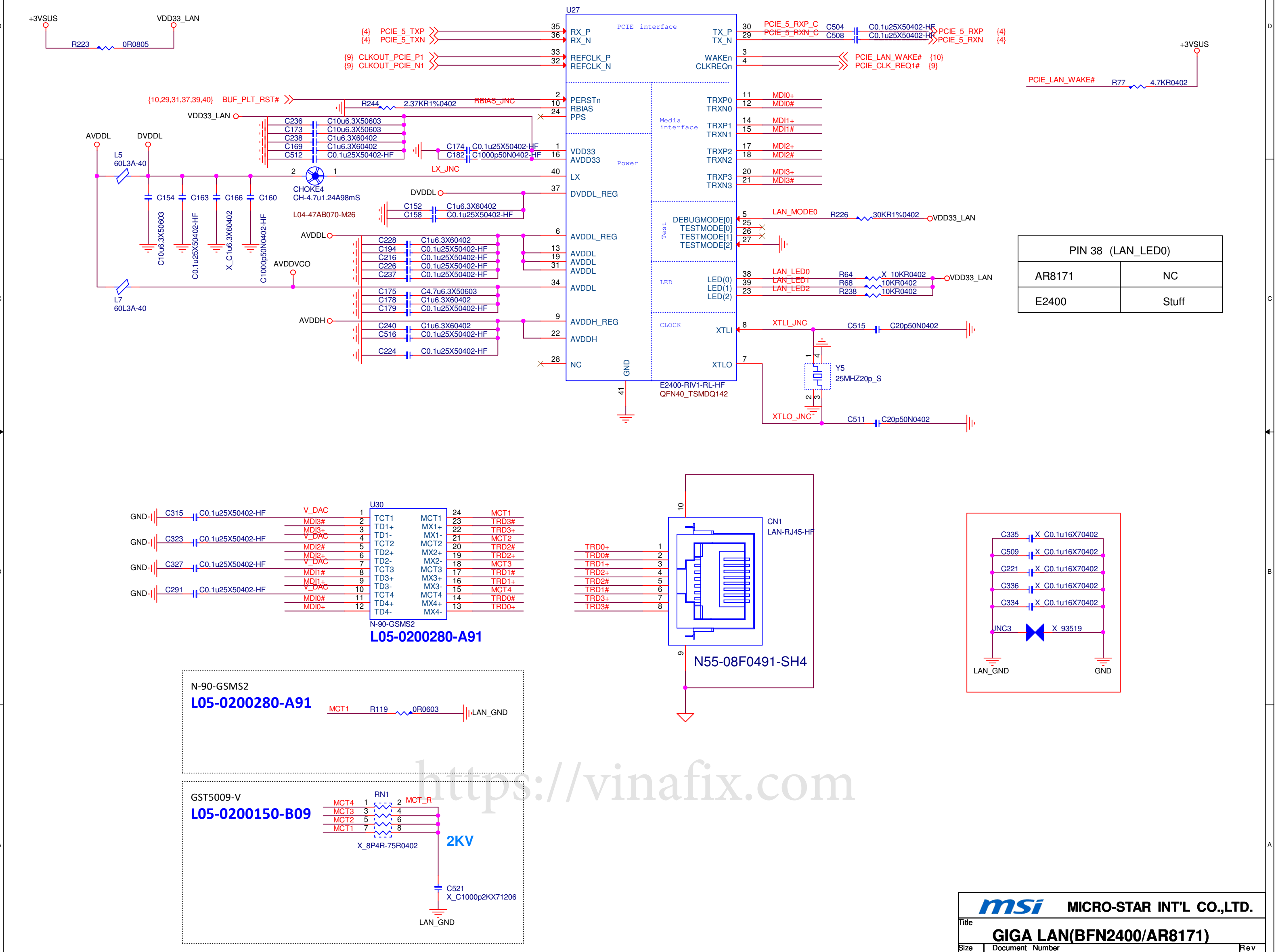

PIN 38 (LAN_LED0)	
AR8171	NC
E2400	Stuff

MICRO-STAR INT'L CO.,LTD.

Title: GIGA LAN(BFN2400/AR8171)

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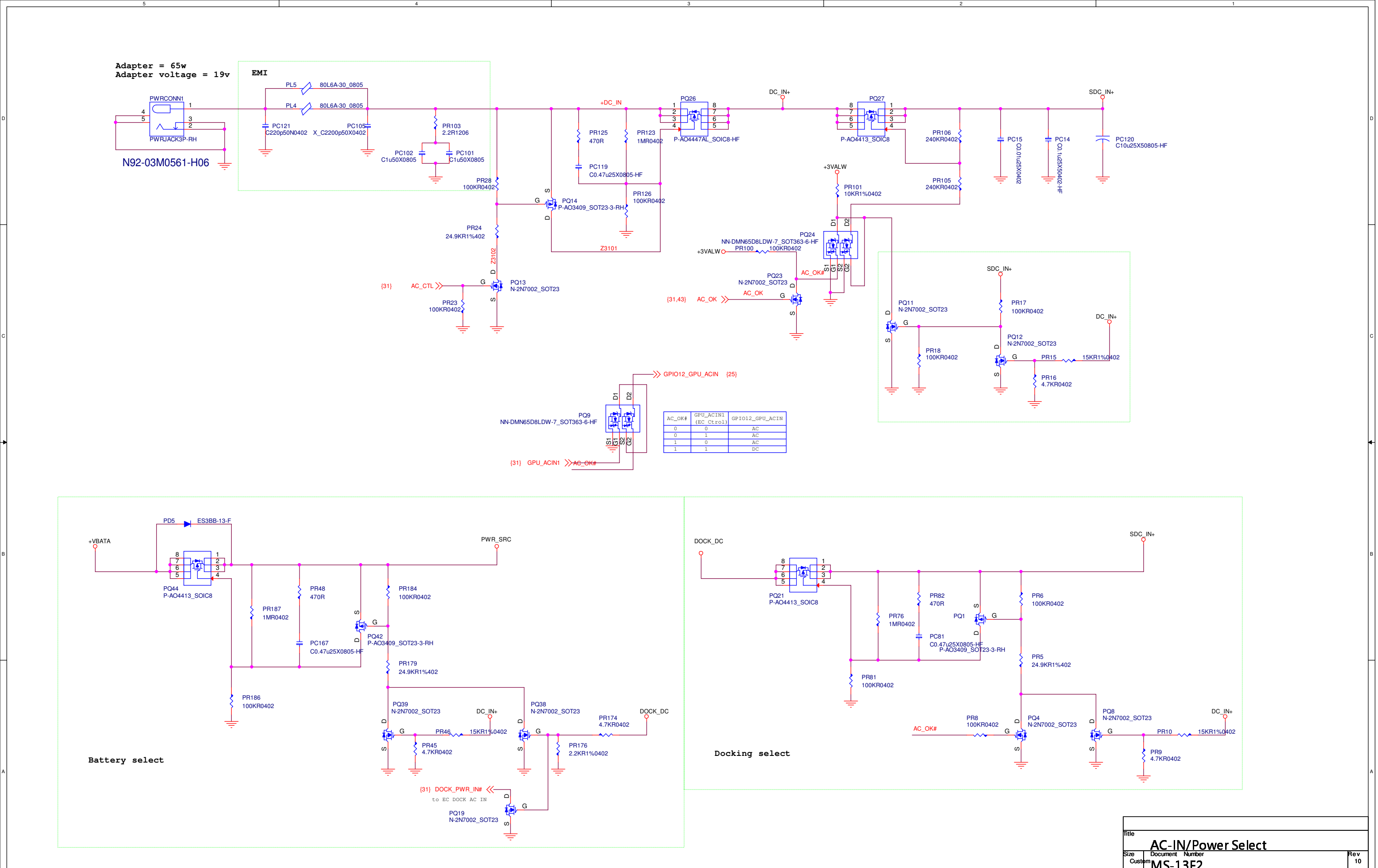

AC_OK#	GPU_ACIN1 (EC Ctrol)	GPIO12_GPU_ACIN
0	0	AC
0	1	AC
1	0	AC
1	1	DC

Title: AC-IN/Power Select
Size: Custom | Document Number: MS-13F2 | Rev: 10
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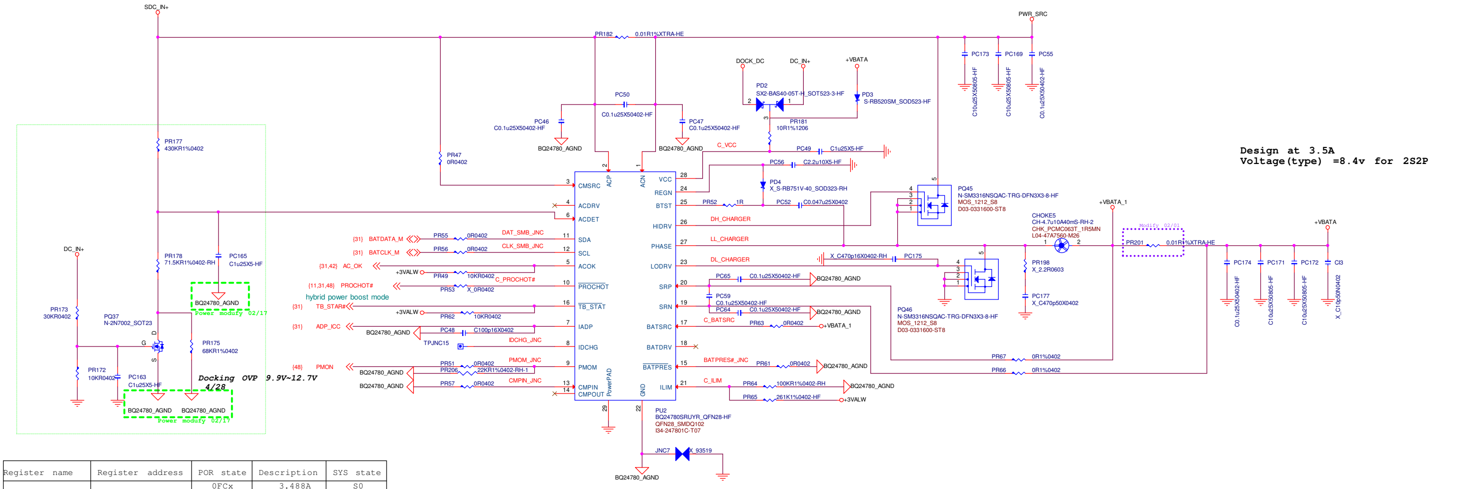
Battery Charger

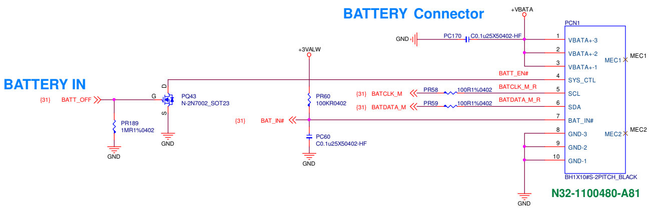
Design at 3.5A
Voltage(type) =8.4v for 2S2P

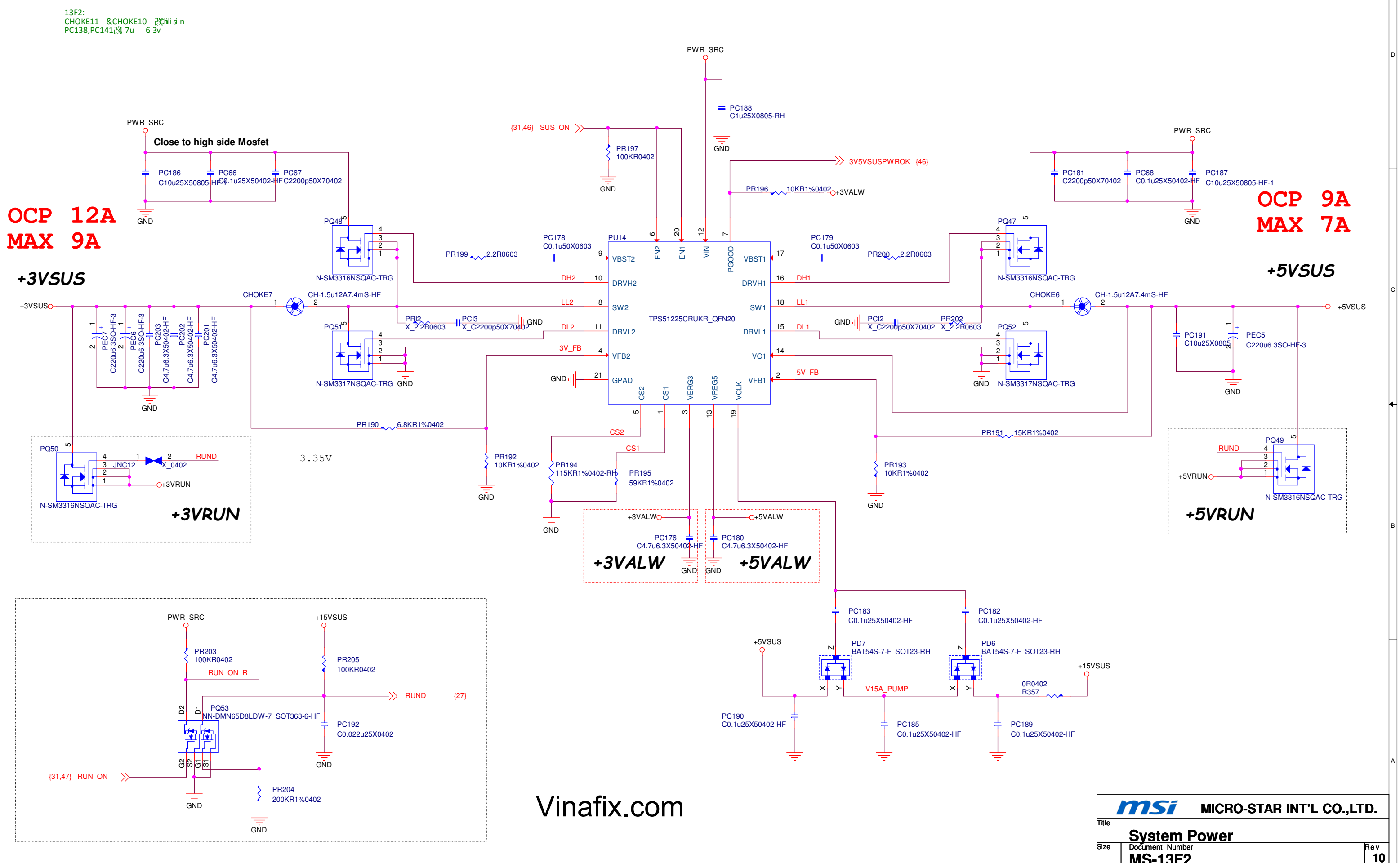


Register name	Register address	POR state		Description	SYS state
Charge current	0x14H	0FCx		3.488A	S0
		05Cx		0.736A	S3/S4/S5
Prepare charge	0x14H	018x		0.192A	
Total Power	0x3FH	19V	0C0x	3.072A	
		12V	130x	4.864A	
Charge voltage	0x15H	20Dx		8.4V	

BATTERY Connector

BATTERY IN





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MICRO-STAR INT'L CO.,LTD.

Title	System Power	
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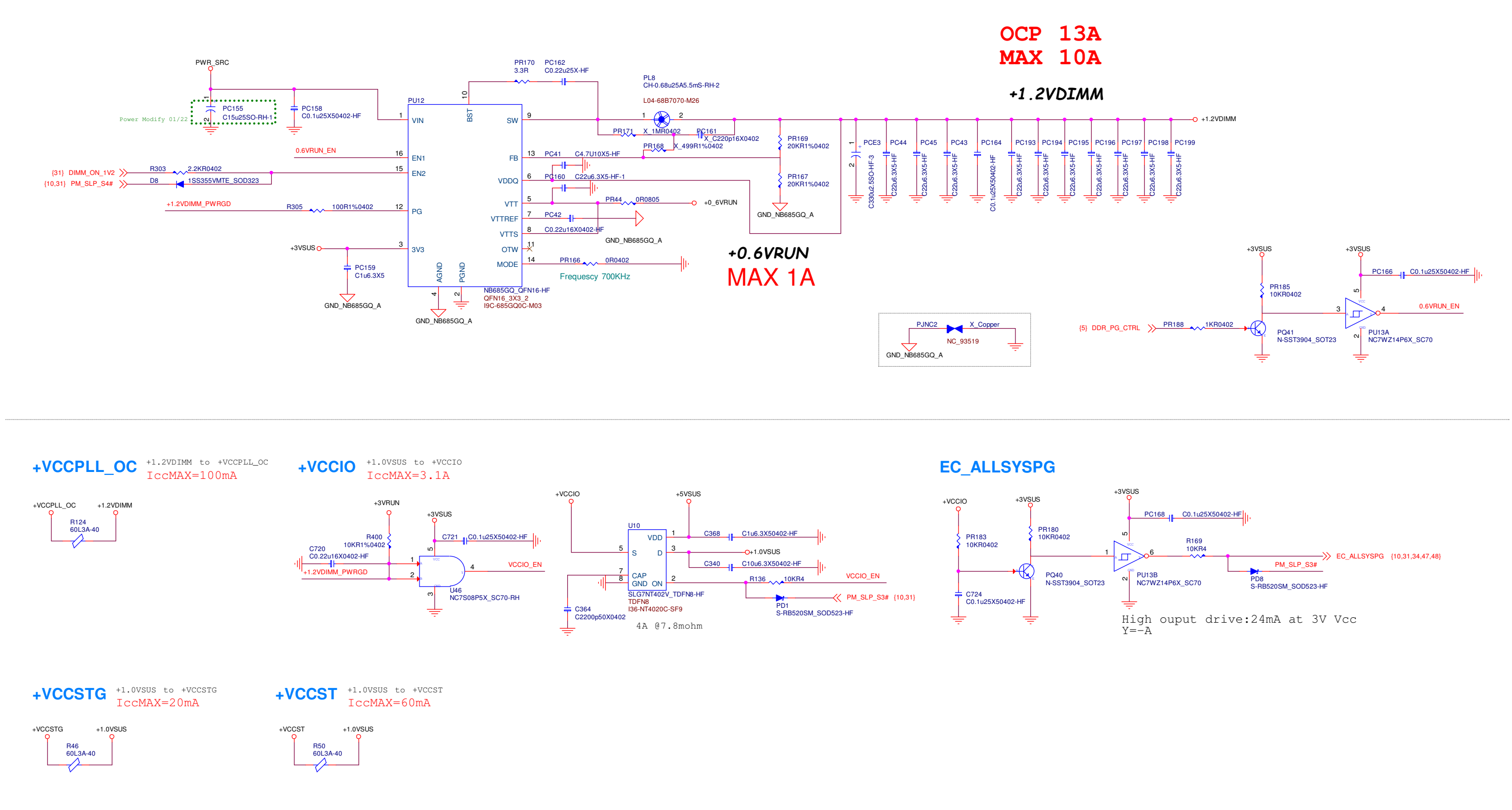
Date: Tuesday, February 23, 2016	Sheet 44 of 60	



MICRO-STAR INT'L CO.,LTD.

Title	+1.2VDIMM/+0.6VRUN	
Size	Document Number MS-13F2	Rev 10
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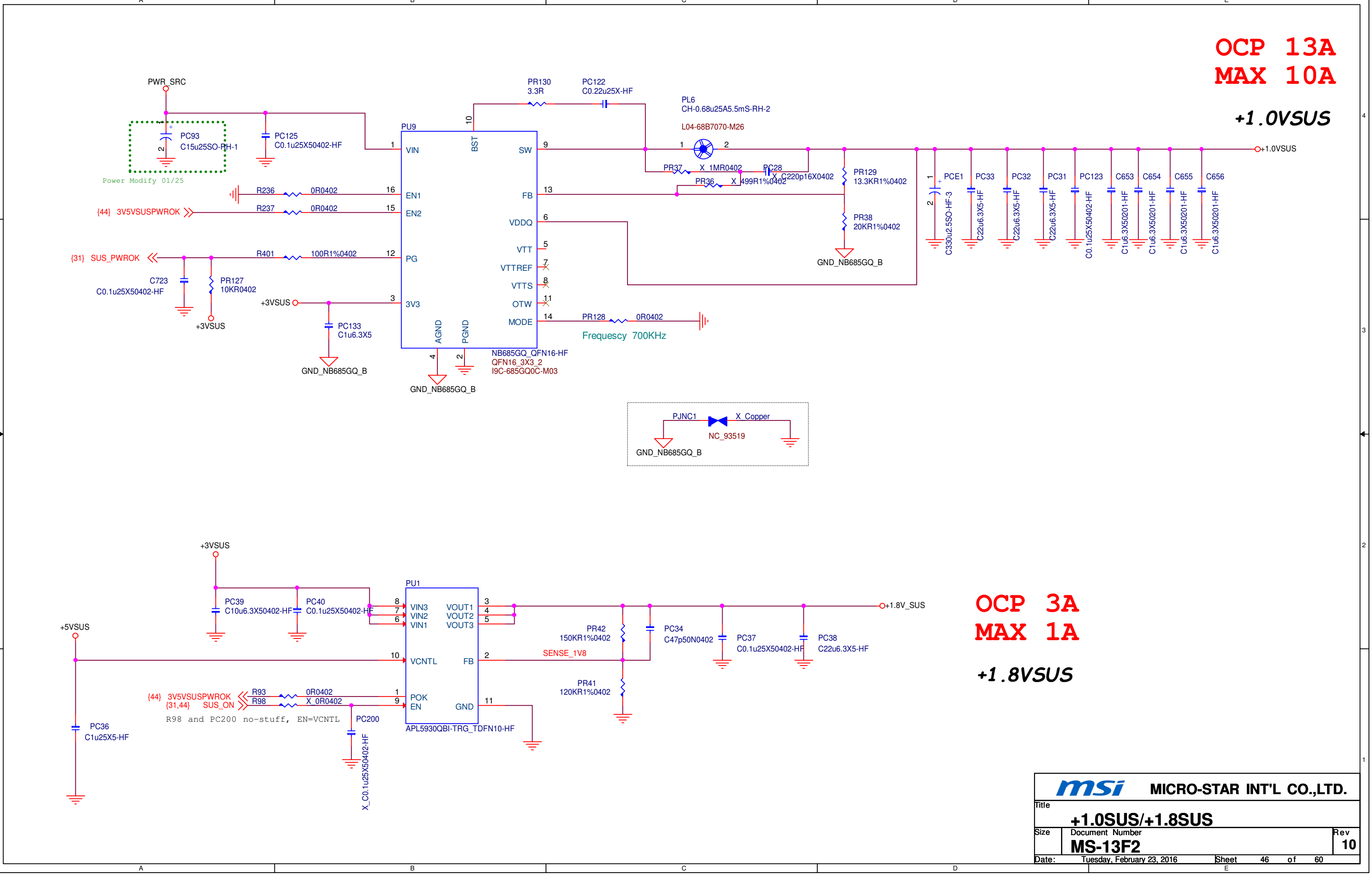

msi MICRO-STAR INT'L CO.,LTD.

Title: +1.0SUS/+1.8SUS

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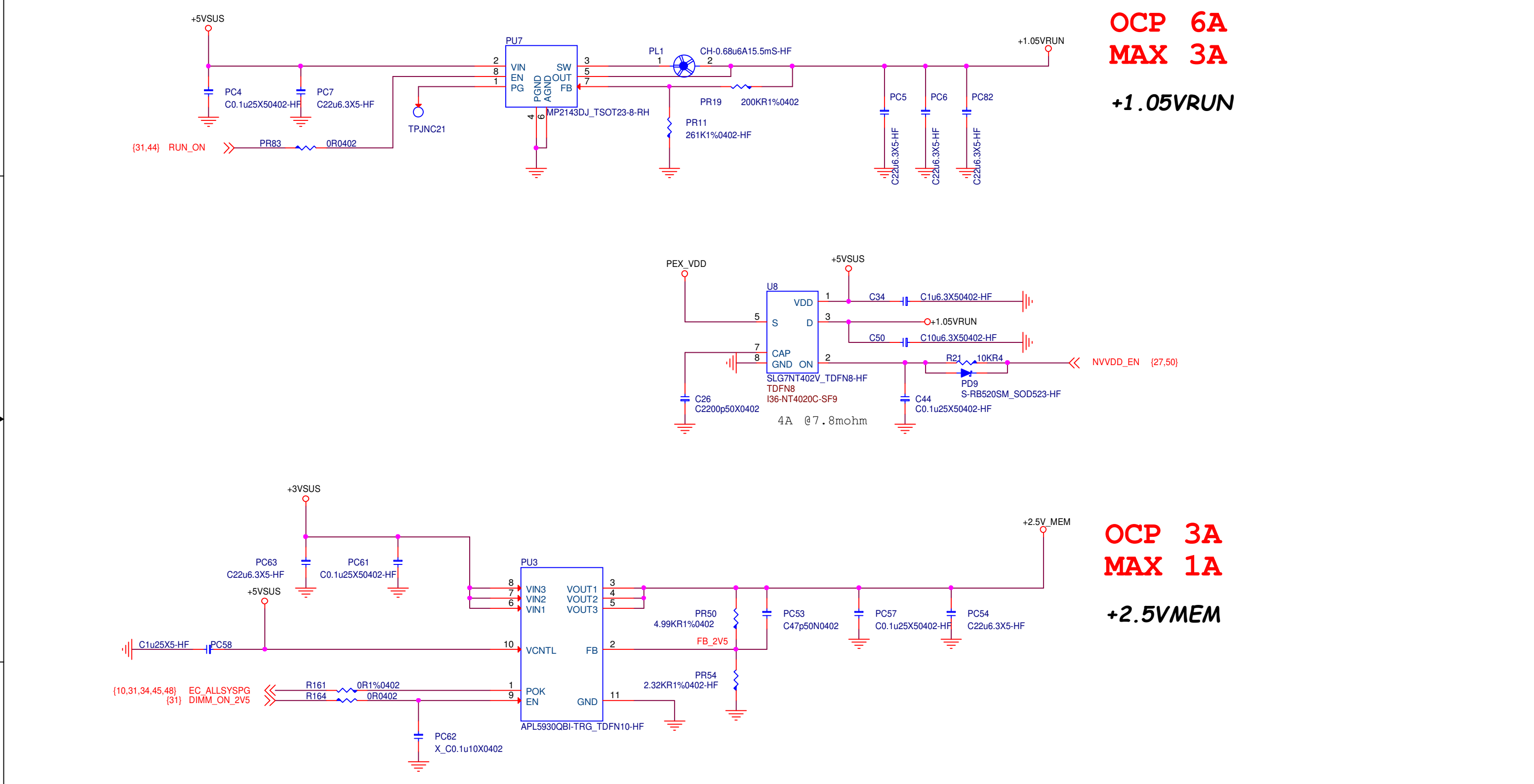
Date: Tuesday, February 23, 2016 | Sheet 46 of 60



MICRO-STAR INT'L CO.,LTD.

Title: +1.05VRUN/2.5VMEM

Size	Document Number	Rev
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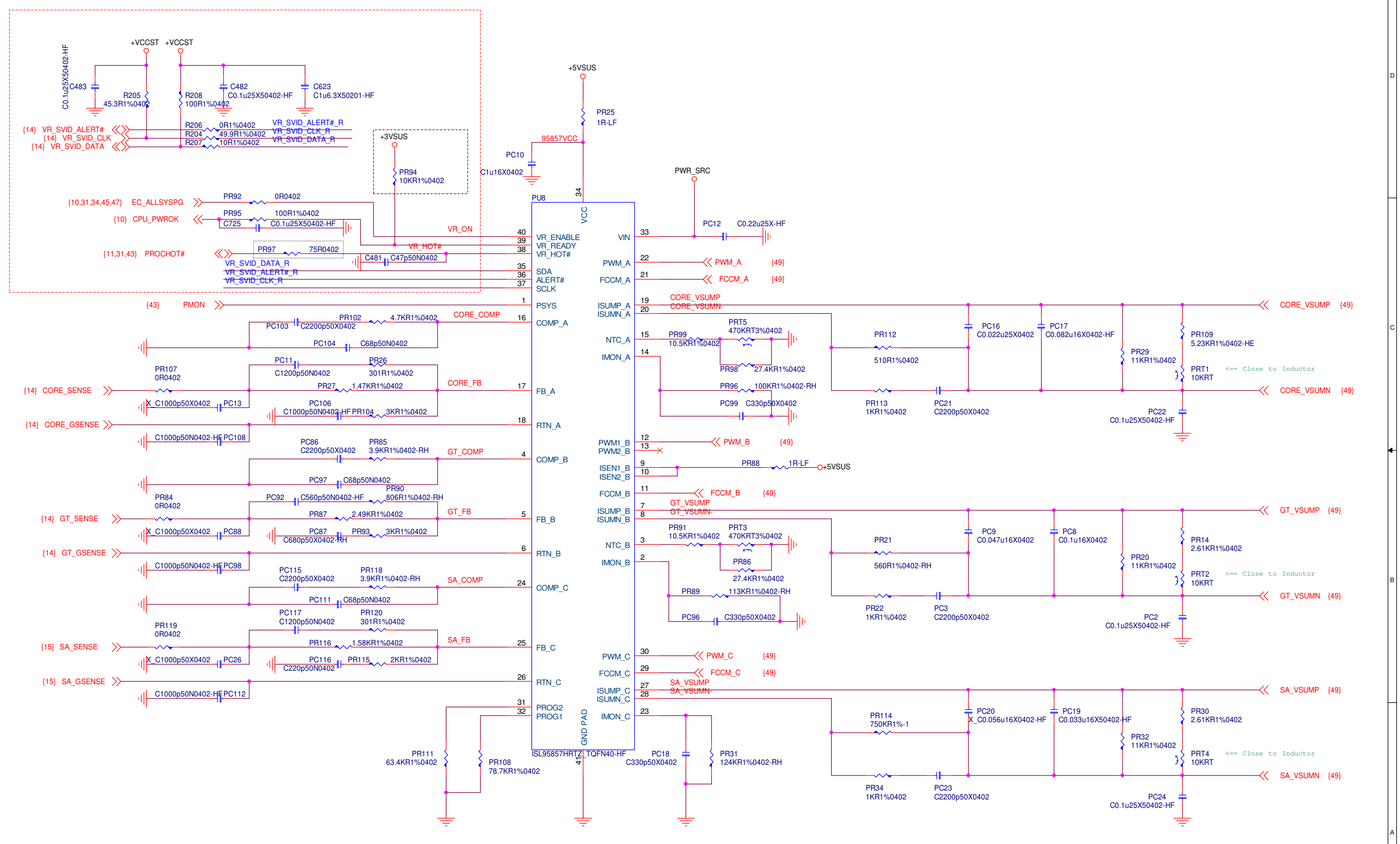
Skylake U-line

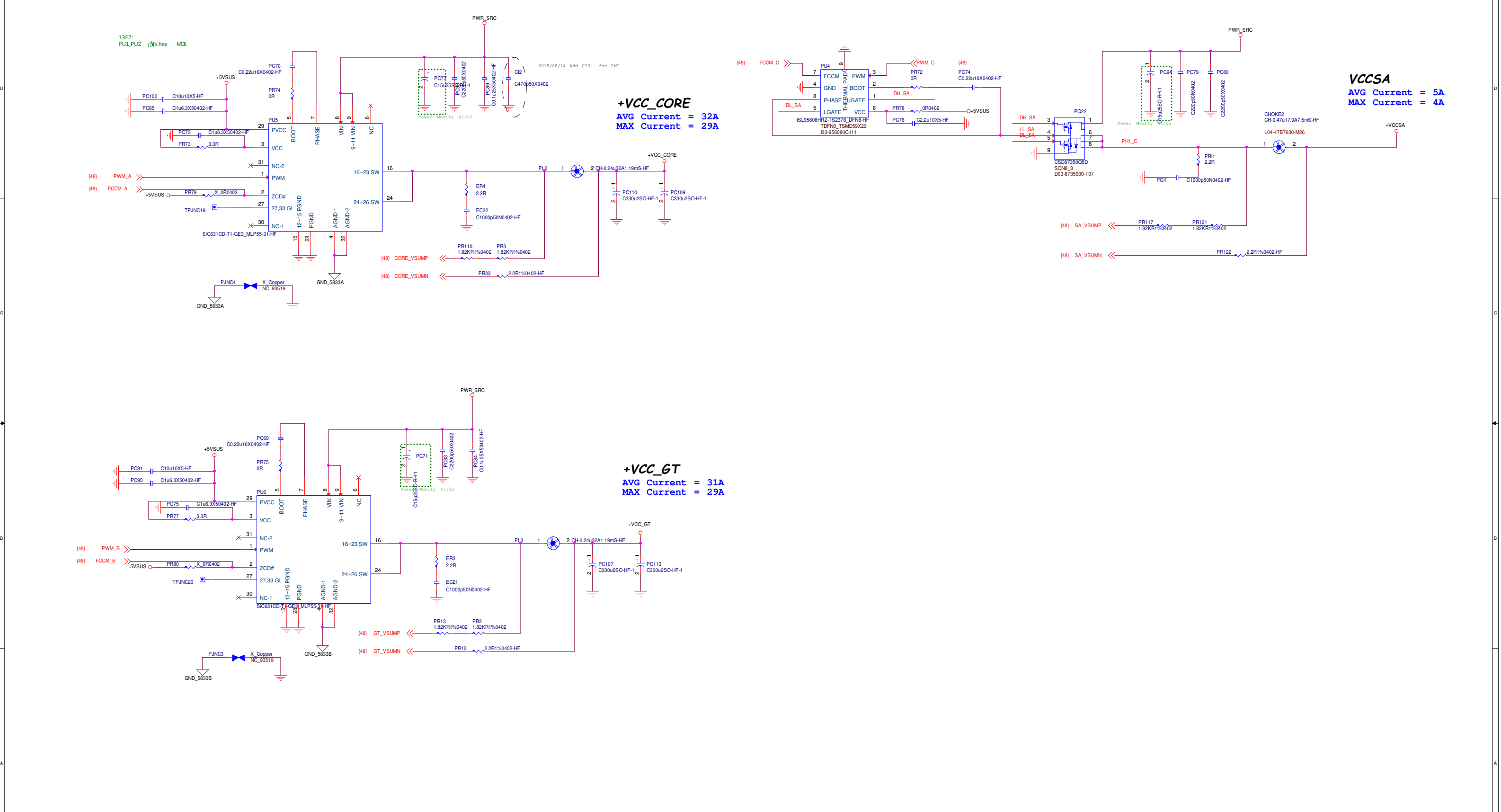


msi MICRO-STAR INT'L CO.,LTD.

Title: CPU Power (ISL95857)

Size | Document Number: MS-13F2 | Rev: 10

Date: Tuesday, February 23, 2016 | Sheet 48 of 60



MICRO-STAR INT'L CO.,LTD.

Title: +VCC_CORE/+VCC_GT/+VCCSA		
Size: Custom	Document Number: MS-13F2	Rev: 10
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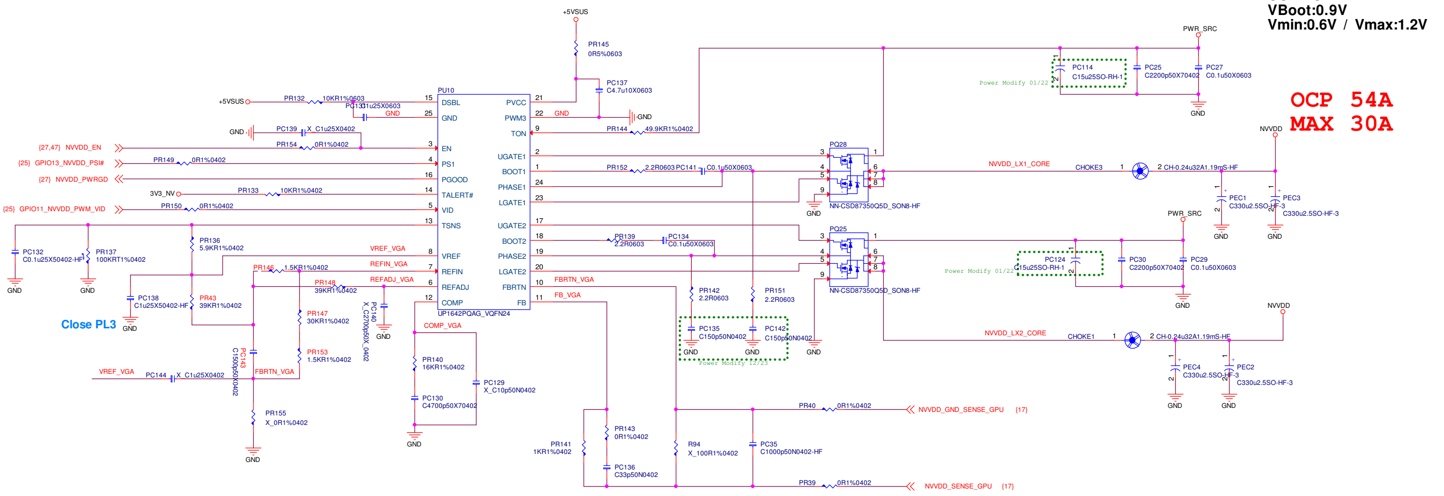
DGPU NVVDD POWER

CONFIG B
VBoot:0.9V
Vmin:0.6V / Vmax:1.2V

OCP 54A
MAX 30A



Close PL3

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MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER NVVDD

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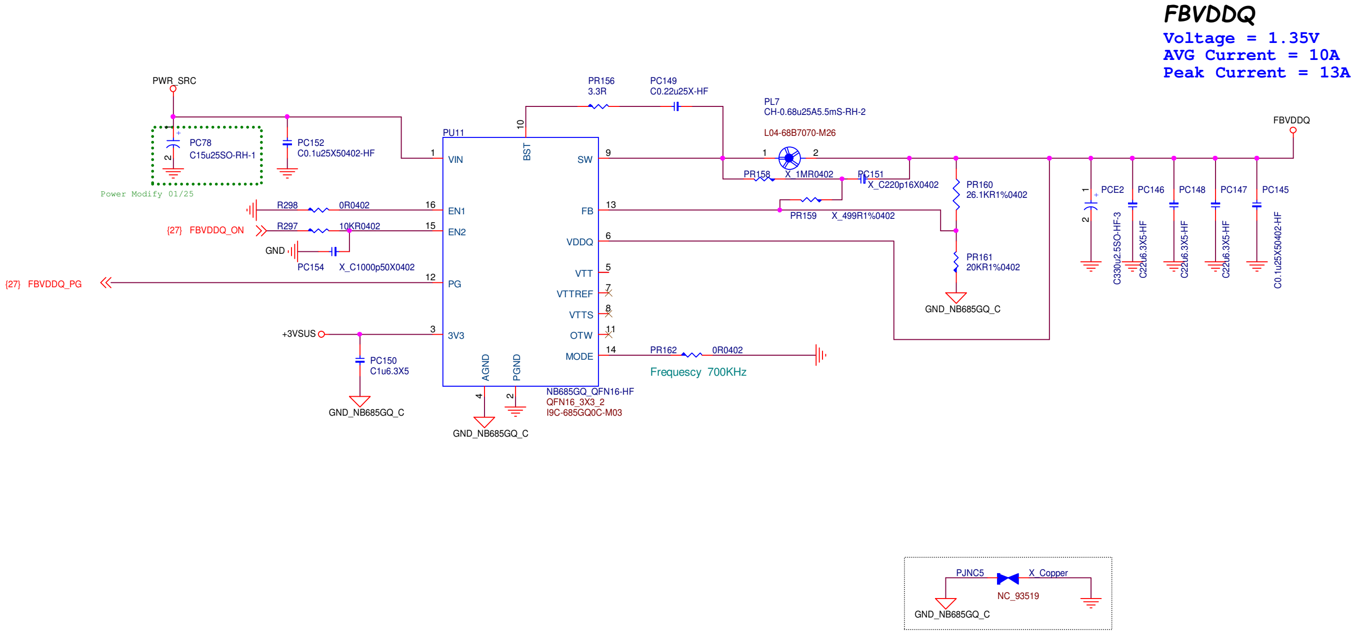
FBVDDQ POWER



msi	MICRO-STAR INT'L CO.,LTD.	
Title	DGPU POWER FBVDDQ	
Size B	Document Number MS-13F2	Rev 10
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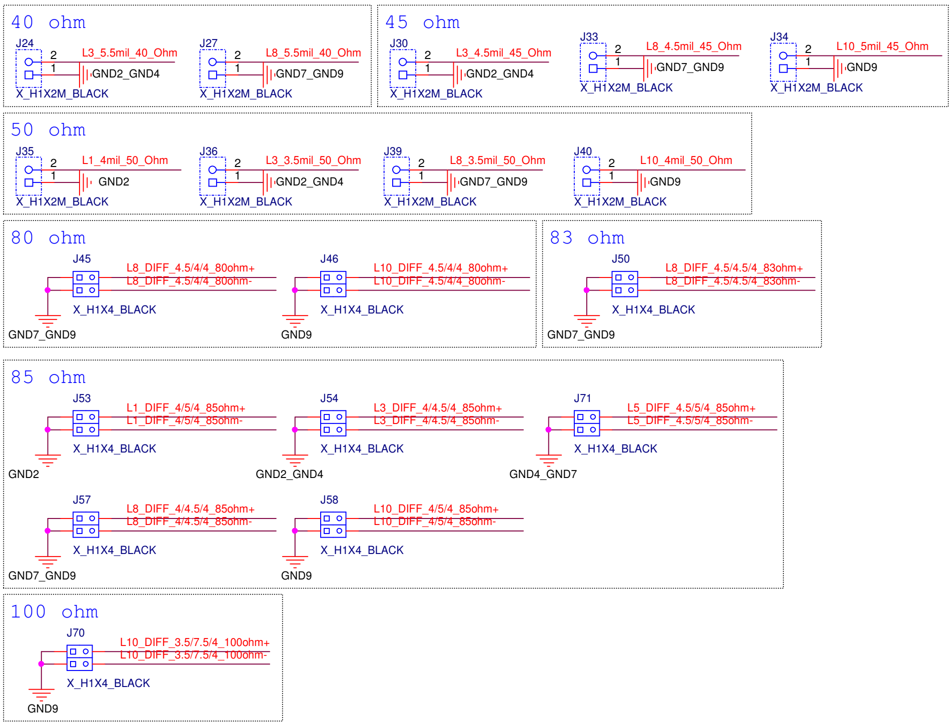
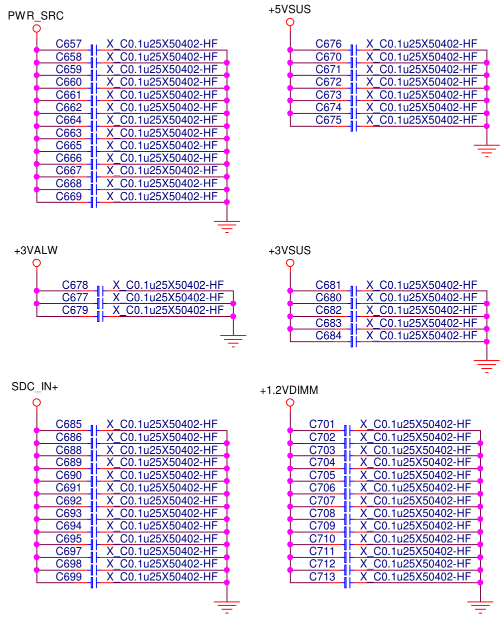
Impedence Connector No PN



EMI suggestion



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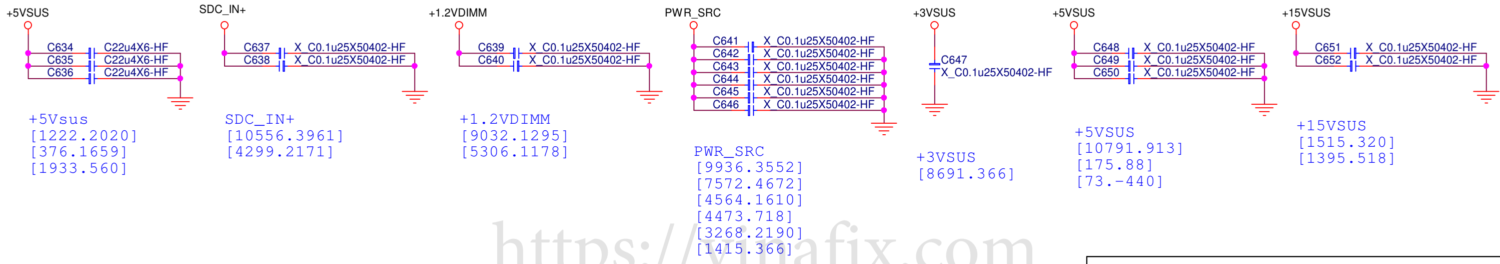
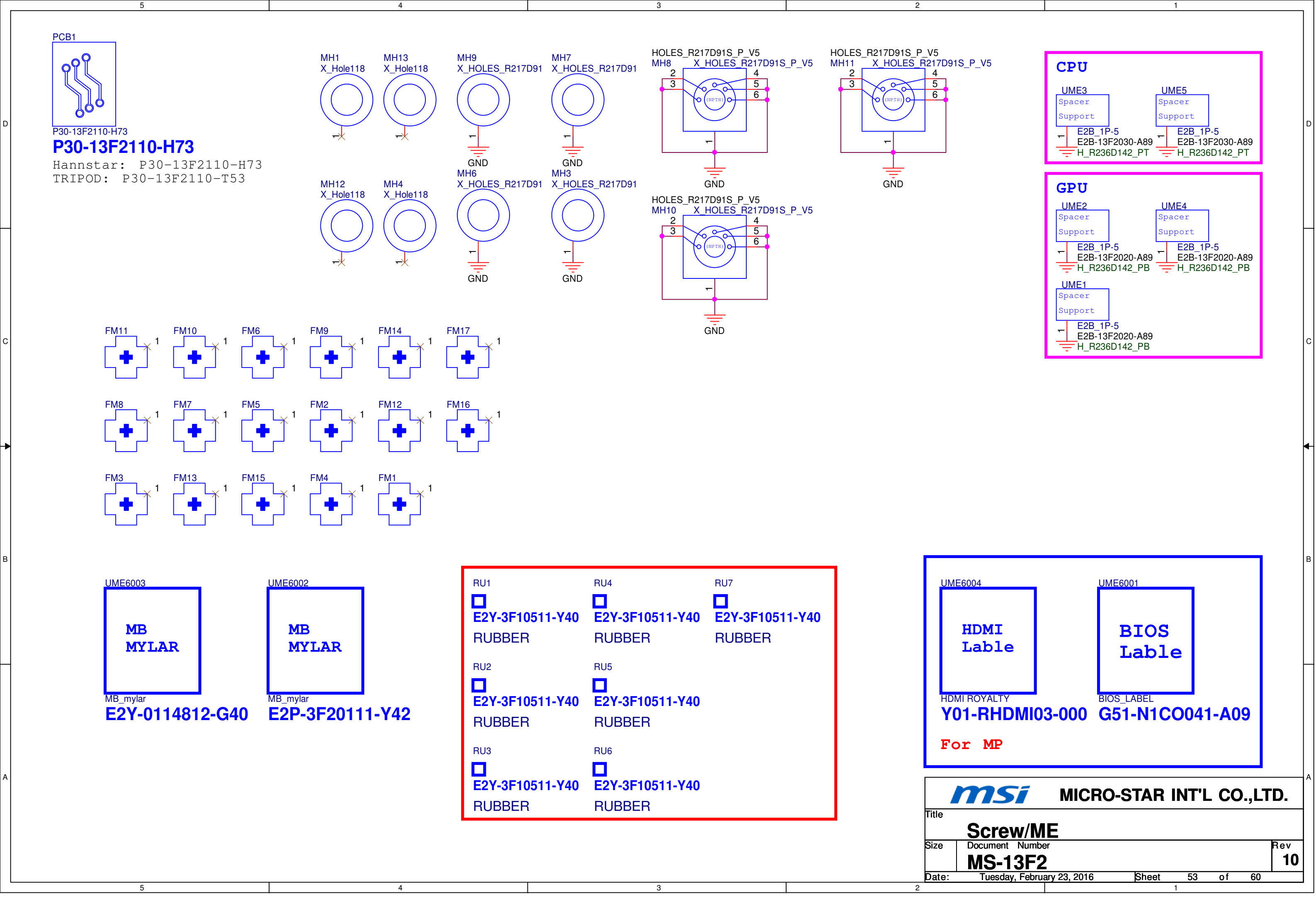
RFI suggestion



MICRO-STAR INT'L CO.,LTD.

Title	EMI/ Impedence	
Size	Document Number: MS-13F2	Rev: 10
Date: Tuesday, February 23, 2016	Sheet 52 of 60	


PCB1
P30-13F2110-H73
P30-13F2110-H73
Hannstar: P30-13F2110-H73
TRIPOD: P30-13F2110-T53
MH1 X_Hole118
MH13 X_Hole118
MH9 X_HOLES_R217D91
MH7 X_HOLES_R217D91
MH12 X_Hole118
MH4 X_Hole118
MH6 X_HOLES_R217D91
MH3 X_HOLES_R217D91
GND
HOLES_R217D91S_P_V5
MH8 X_HOLES_R217D91S_P_V5
MH11 X_HOLES_R217D91S_P_V5
MH10 X_HOLES_R217D91S_P_V5
CPU
UME3 Spacer Support E2B_1P-5 E2B-13F2030-A89 H_R236D142_PT
UME5 Spacer Support E2B_1P-5 E2B-13F2030-A89 H_R236D142_PT
GPU
UME2 Spacer Support E2B_1P-5 E2B-13F2020-A89 H_R236D142_PB
UME4 Spacer Support E2B_1P-5 E2B-13F2020-A89 H_R236D142_PB
UME1 Spacer Support E2B_1P-5 E2B-13F2020-A89 H_R236D142_PB
FM11 FM10 FM6 FM9 FM14 FM17
FM8 FM7 FM5 FM2 FM12 FM16
FM3 FM13 FM15 FM4 FM1
UME6003 MB MYLAR MB_mylar E2Y-0114812-G40
UME6002 MB MYLAR MB_mylar E2P-3F20111-Y42
RU1 E2Y-3F10511-Y40 RUBBER
RU4 E2Y-3F10511-Y40 RUBBER
RU7 E2Y-3F10511-Y40 RUBBER
RU2 E2Y-3F10511-Y40 RUBBER
RU5 E2Y-3F10511-Y40 RUBBER
RU3 E2Y-3F10511-Y40 RUBBER
RU6 E2Y-3F10511-Y40 RUBBER
UME6004 HDMI Lable HDMI ROYALTY Y01-RHDMI03-000
UME6001 BIOS Lable BIOS_LABEL G51-N1CO041-A09
For MP
msi MICRO-STAR INT'L CO.,LTD.
Title Screw/ME
Size Document Number MS-13F2 Rev 10
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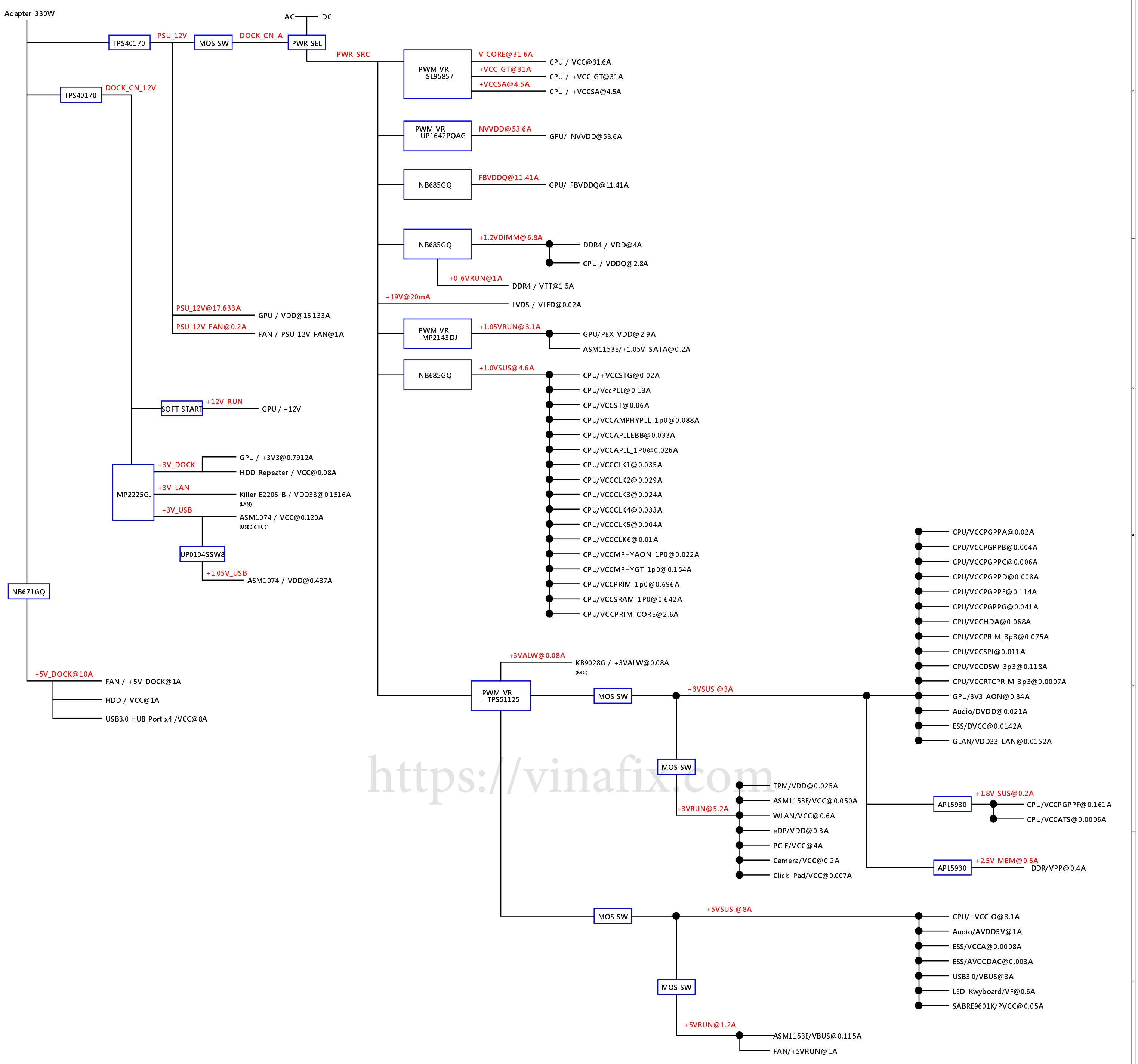
MS-13F2 Power Delivery Chart



msi	MICRO-STAR INT'L CO.,LTD.	
Title: Power Delivery Map		
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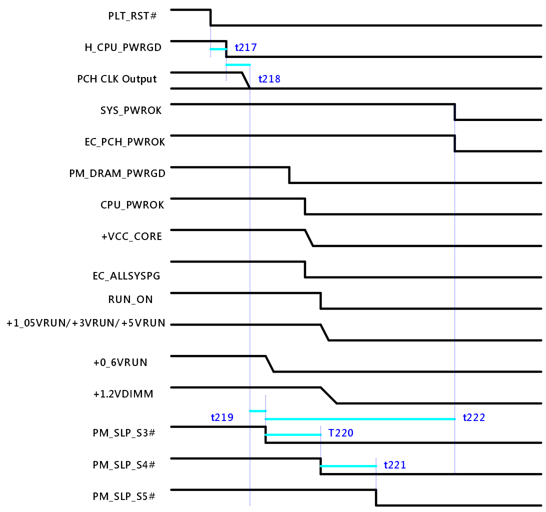
Power down Sequence

S0 -> S5



	MIN	MAX	Units	Description
t217	30		us	PLTRST# active to PWROK de-asserted
t218	30		us	PROCPWRGD inactive to clocks inactive
t219	1		ns	Clock invalid to SLP_S3# asserted
t220		500	ms	SLP_S3# low to SLP_S4# low
t221	40		ns	SLP_S4# low to SLP_S5# low
t222	5		us	SLP_S3# active to PWROK de-asserted

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Title: Power down Sequence

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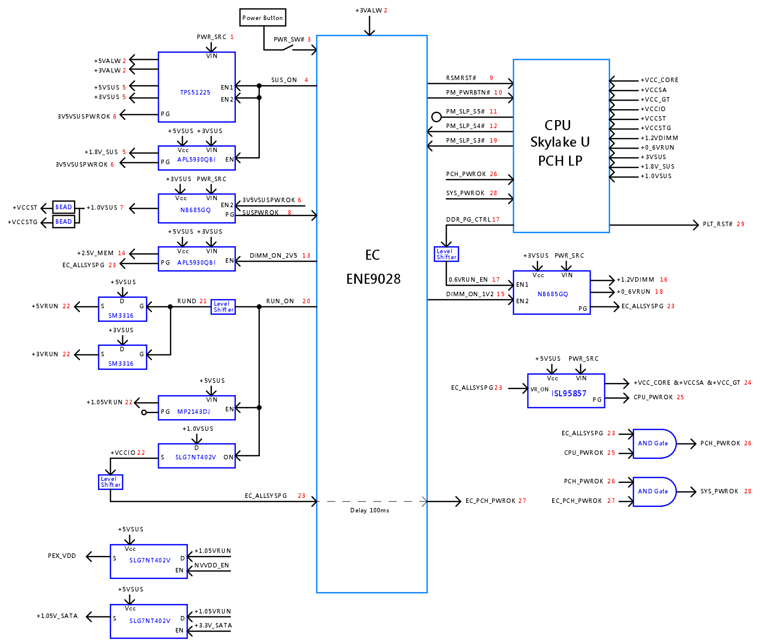
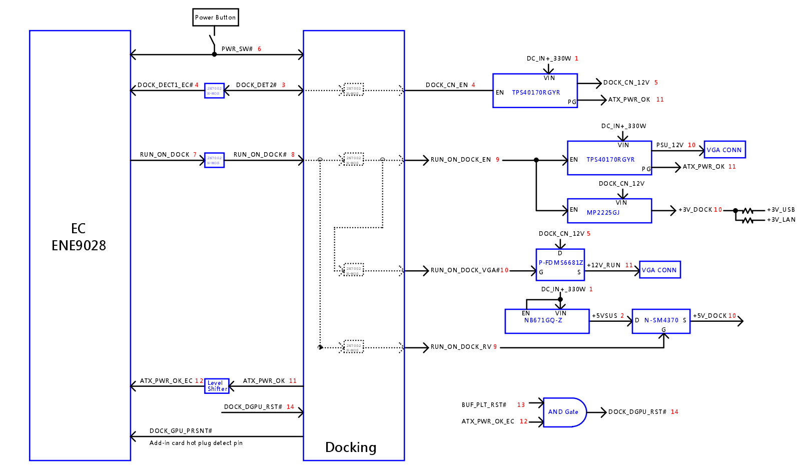
MS-13F2 Power on Block Diagram



Dock Power on Block Diagram

NB insert to Docking



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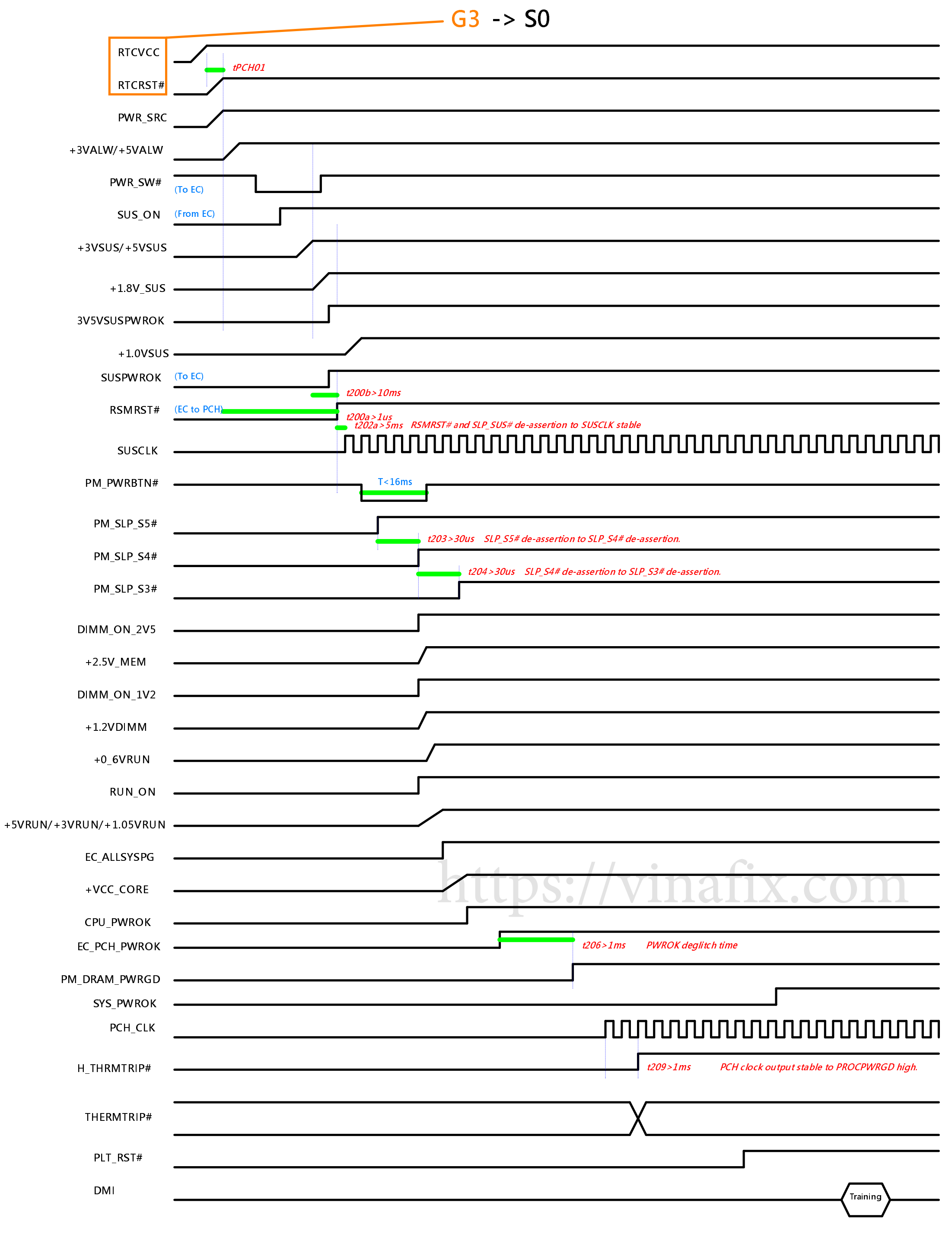
Power on Block Diagram

MS-13F2

10

Power on Sequence



0C History

2016/01/19:

1. Power Modify as below :
   PC77,PC78,PC71,PC72,PC94,PC93,PC118,PC114,PC124,PC128 change to C11-1067610-M09.
2. CN3, CN5 change to N54-05F1461-SL0 on page36,37.
3. Add PD9 for power down on page47.

2016/01/20:

1. D6 BOM stuff on page13.

2016/01/22:

1. Add PM_SLP_S5# to EC on page31.
2. Modify BOM for MB ID: R173 stuff, R174 no stuff on page31.
3. Power Modify as below:
   PC77,PC94,PC71,PC114,PC124,PC155 change to C71-150251G-S03,
   Remove: PC78,PC93,PC72,PC118,PC128,PC157.

2016/01/27:

1. EMI add cap. EC55,EC56,EC57 on page37.
2. Add C726, C727 on page38.

2016/02/01:

1. Add L16 on page38.
2. Change C728 to correct part reference on page31.
3. Power PR201 change to R11-001BT40-Y01 on page43.

2016/02/02:

1. R404 change to correct part reference on page29.

2016/02/04:

1. Power modify PQ25,PQ28 change to D03-8735000-T07 on page50.

2016/02/05:

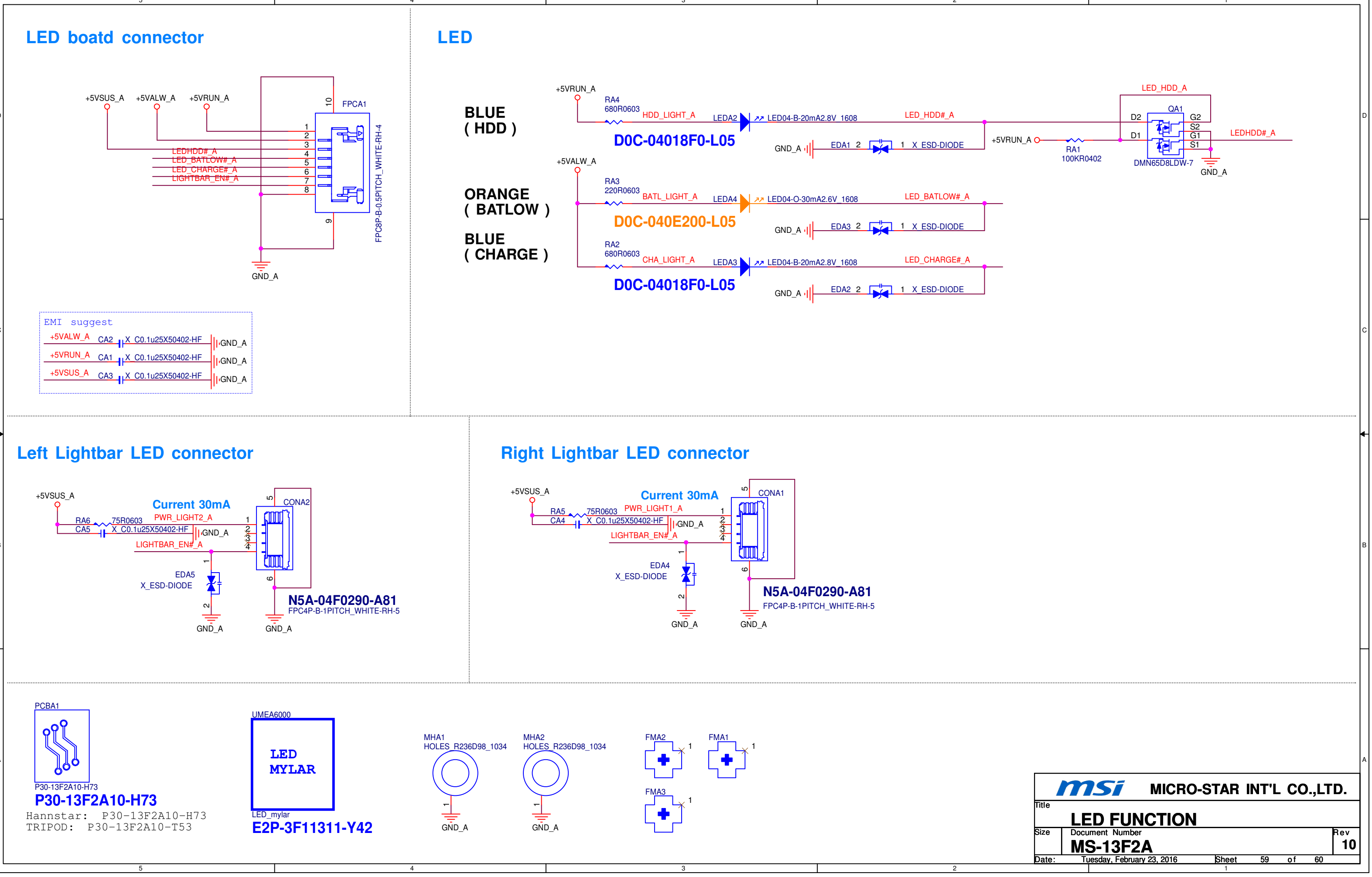
1. Add R405 0 ohm on page38.

2016/02/15:

1. H3, H4 footprint change to H_R220D142_PTB on page39.

2016/02/17:

1. Power modify power gnd name to BQ24780_AGND on page43.
2. TPM BOM no stuff on page39.



LED boatd connector
+5VSUS_A
+5VALW_A
+5VRUN_A
FPCA1
LEDHDD#_A
LED_BATLOW#_A
LED_CHARGE#_A
LIGHTBAR_EN#_A
FPC8P-B-0.5PITCH_WHITE-RH-4
GND_A
EMI suggest
+5VALW_A CA2 X_C0.1u25X50402-HF GND_A
+5VRUN_A CA1 X_C0.1u25X50402-HF GND_A
+5VSUS_A CA3 X_C0.1u25X50402-HF GND_A
LED
BLUE
(HDD)
+5VRUN_A
RA4
680R0603
HDD_LIGHT_A
LEDA2
LED04-B-20mA2.8V_1608
LED_HDD#_A
D0C-04018F0-L05
GND_A
EDA1
X_ESD-DIODE
LED_HDD_A
QA1
D2
D1
G2
S2
G1
S1
+5VRUN_A
RA1
100KR0402
DMN65D8LDW-7
LEDHDD#_A
GND_A
ORANGE
(BATLOW)
+5VALW_A
RA3
220R0603
BATL_LIGHT_A
LEDA4
LED04-O-30mA2.6V_1608
LED_BATLOW#_A
D0C-040E200-L05
GND_A
EDA3
X_ESD-DIODE
BLUE
(CHARGE)
RA2
680R0603
CHA_LIGHT_A
LEDA3
LED04-B-20mA2.8V_1608
LED_CHARGE#_A
D0C-04018F0-L05
GND_A
EDA2
X_ESD-DIODE
Left Lightbar LED connector
+5VSUS_A
Current 30mA
CONA2
RA6
75R0603
PWR_LIGHT2_A
CA5
X_C0.1u25X50402-HF
GND_A
LIGHTBAR_EN#_A
EDA5
X_ESD-DIODE
GND_A
GND_A
N5A-04F0290-A81
FPC4P-B-1PITCH_WHITE-RH-5
Right Lightbar LED connector
+5VSUS_A
Current 30mA
CONA1
RA5
75R0603
PWR_LIGHT1_A
CA4
X_C0.1u25X50402-HF
GND_A
LIGHTBAR_EN#_A
EDA4
X_ESD-DIODE
GND_A
GND_A
N5A-04F0290-A81
FPC4P-B-1PITCH_WHITE-RH-5
PCBA1
P30-13F2A10-H73
P30-13F2A10-H73
Hannstar: P30-13F2A10-H73
TRIPOD: P30-13F2A10-T53
UMEA6000
LED
MYLAR
LED_mylar
E2P-3F11311-Y42
MHA1
HOLES_R236D98_1034
GND_A
MHA2
HOLES_R236D98_1034
GND_A
FMA2
FMA1
FMA3
MICRO-STAR INT'L CO.,LTD.
Title
LED FUNCTION
Size
Document Number
MS-13F2A
Rev
10
Date: Tuesday, February 23, 2016
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History

0B: