LCFC Confidential

Y530 M/B Schematics Document

Coffee Lake H-Processor with DDR4 + NV N17E-G1 GPU

FY510

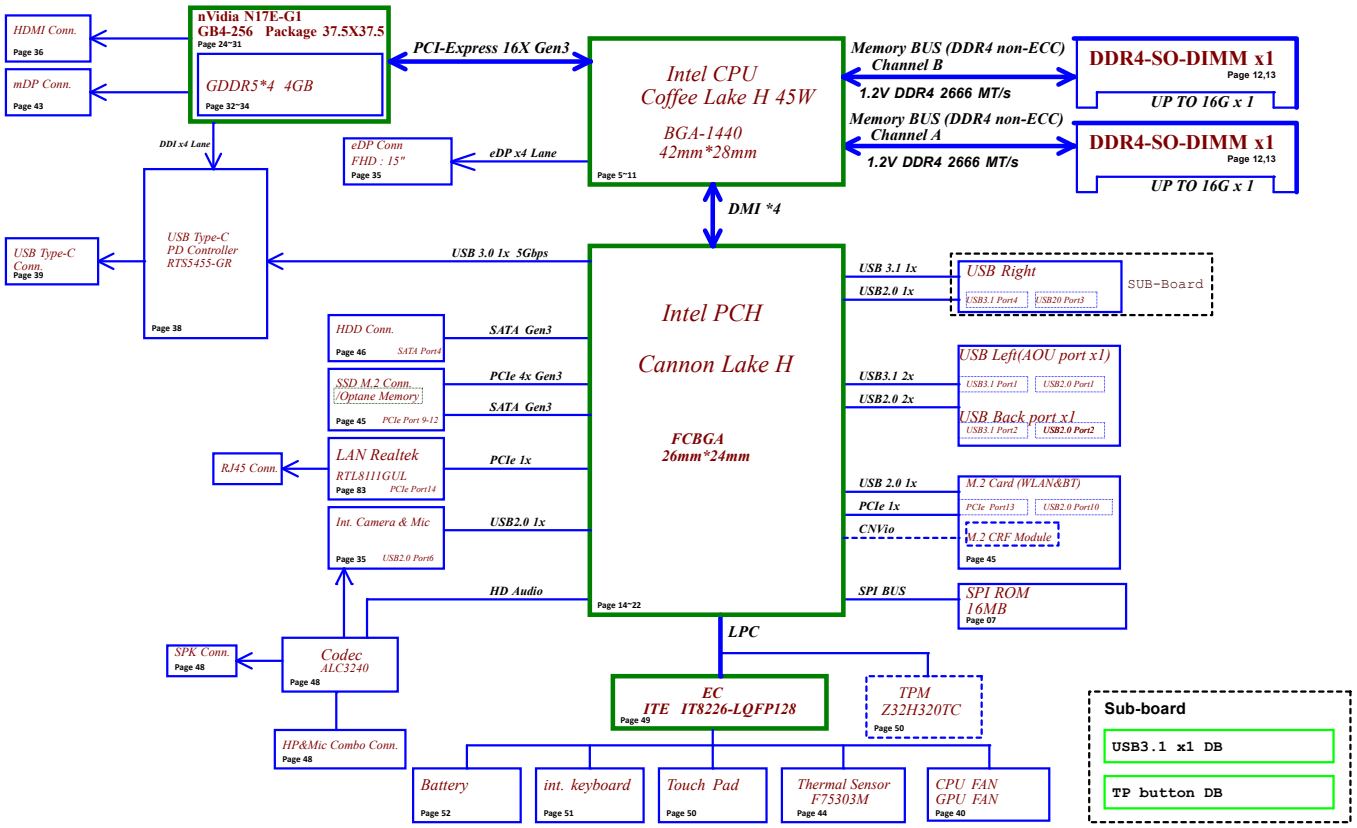
2018-06-27

REV:1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: Cover Page			
Size: Custom	Document Number: FY510		Rev: 1.0
Date: Monday, July 02, 2018	Sheet 1 of 75		

LCFC confidential



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	Block Diagram		
Size C	Document Number FY510		Rev 1.0
Date: Monday, July 02, 2018	Sheet 2 of 75		

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGPXCORE +1.8VS_AON +1.8VGS NVVDD NVVDDS +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
AOAC@	AOAC support part
CNVI@	CNVi support part
ME@	ME part(connector, hole)
OPT@	For NV GPU part
OPTANE@	Optane memory support part
TPM@	For support TPM sku part
CD@	Cost down part

USB2.0 Port table	
Port	Function
1	Back USB3.0
2	Left USB3.0
3	Right USB3.0
4	Type-C Port
5	NA
6	Camera
7:13	NA
14	BT

USB3.0 Port table	
Port	Function
1	Back USB3.0
2	Type-C Port
3	Left USB3.0
4	Right USB3.0
5	NA
6	NA

SATA Port table	
Port	Function
0A	NA
0B	NA
1A	M.2 SSD Gen3
1B	NA
2	HDD Gen3
3	NA
4	NA
5	NA

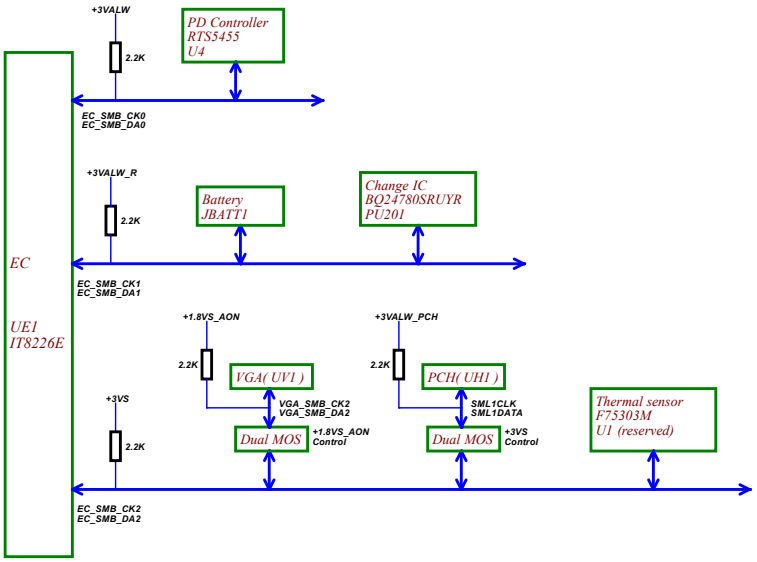
PCIE Port table	
Port	Function
1:8	NA
9	M.2 SSD/Optane
10	M.2 SSD/Optane
11	M.2 SSD/Optane
12	M.2 SSD/Optane
13	WLAN Gen1
14	LAN Gen1
15:24	NA

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **Notes List**

Size	Document Number	Rev
Custom	FY510	1.0

Date: Monday, July 02, 2018 Sheet 3 of 75



SMBUS Control Table

	SOURCE	VGA	BATT	IT8226E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	Charger	RGB KB Backlight	USB-C PD	Hi-Fi Audio
EC_SMB_CK1 EC_SMB_DA1	IT8226E +3VALW_R	X	V +3VALW_R	V +3VALW_R	X	X	X	X	X	V +3VALW_R	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8226E +3VS	V +1.8VS_AON	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X	X	X	X
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS Reserve	X	V +3VALW_PCH	V +3VS	X	X	X	X
PCH_RGBKB_SCL PCH_RGBKB_SDA	X	X	X	X	X	X	X	X	X	X	X	X	X
EC_SMB_CK0 EC_SMB_DA0	IT8226E +3VALW	X	X	X	X	X	X	X	X	X	X	V +LDO_3V3	X

EC SM Bus1 address

Device	Address
Smart Battery	0x16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
Thermal Sensor F75303M	1001_100x b
VGA	0x9E (default)
PCH	Need to update

PCH SM Bus address

Device	Address
DDR DIMMA	1010 000X b
DDR DIMMB	1010 010X b
TP Module	Need to update
Wlan	Reserved

PCH I2C 2 Bus address

Device	Address
RGB Backlight	Need to update

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: Blank4

Size	Document Number	Rev
D	FX510	1.0

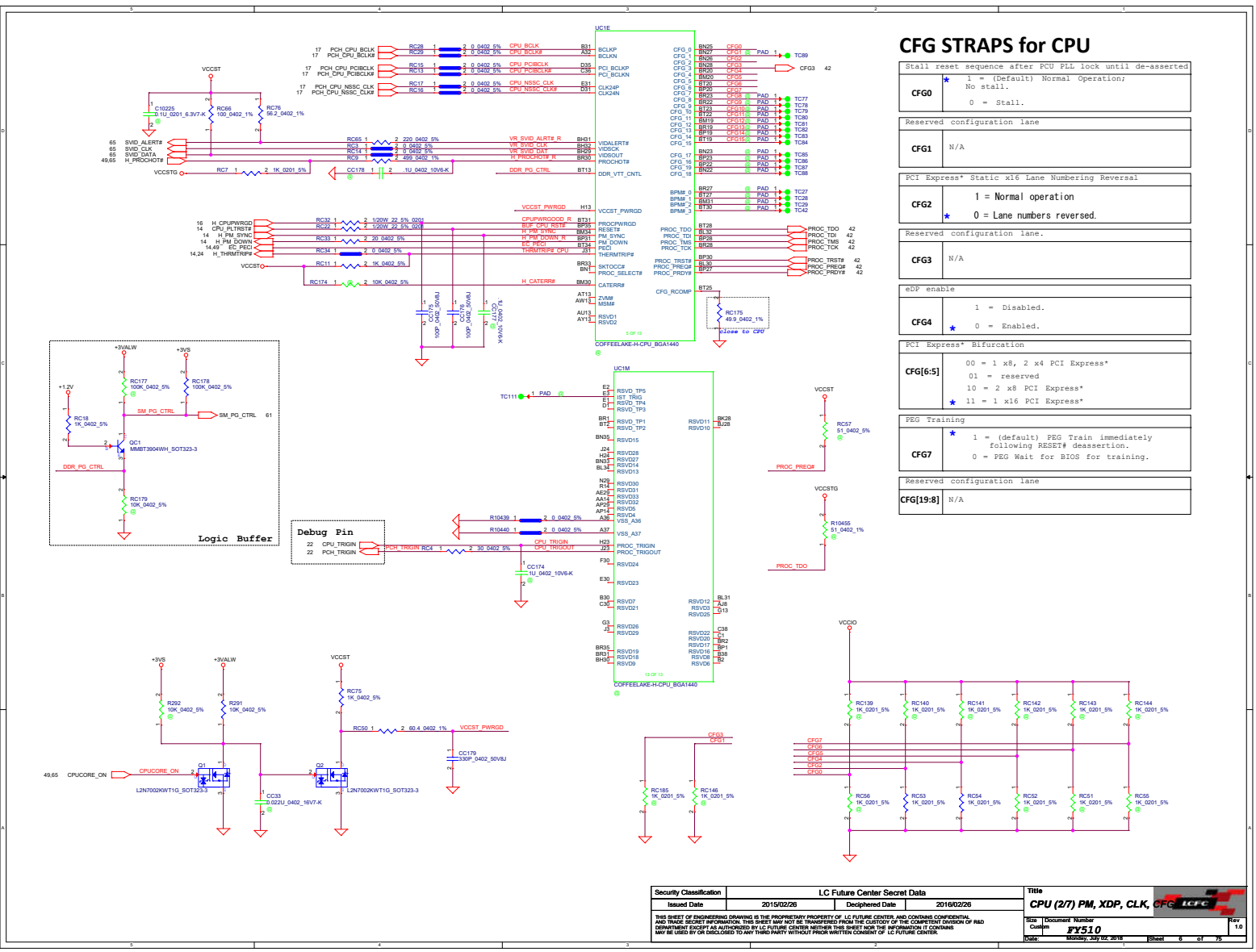
Date: Sunday, July 29, 2018 Sheet 1 of 46

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **CPU (1/7) DMI,PEG**

Size	Document Number	Rev
Custom	FY510	1.0

Date: Monday, July 02, 2018 Sheet 5 of 75



CFG STRAPS for CPU

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	★ 1 = (Default) Normal Operation; No stall. 0 = Stall.

Reserved configuration lane	
CFG1	N/A

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation ★ 0 = Lane numbers reversed.

Reserved configuration lane.	
CFG3	N/A

eDP enable	
CFG4	1 = Disabled. ★ 0 = Enabled.

PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* ★ 11 = 1 x16 PCI Express*

PEG Training	
CFG7	★ 1 = (default) PEG Train immediately following RESET# deassertion. 0 = PEG Wait for BIOS for training.

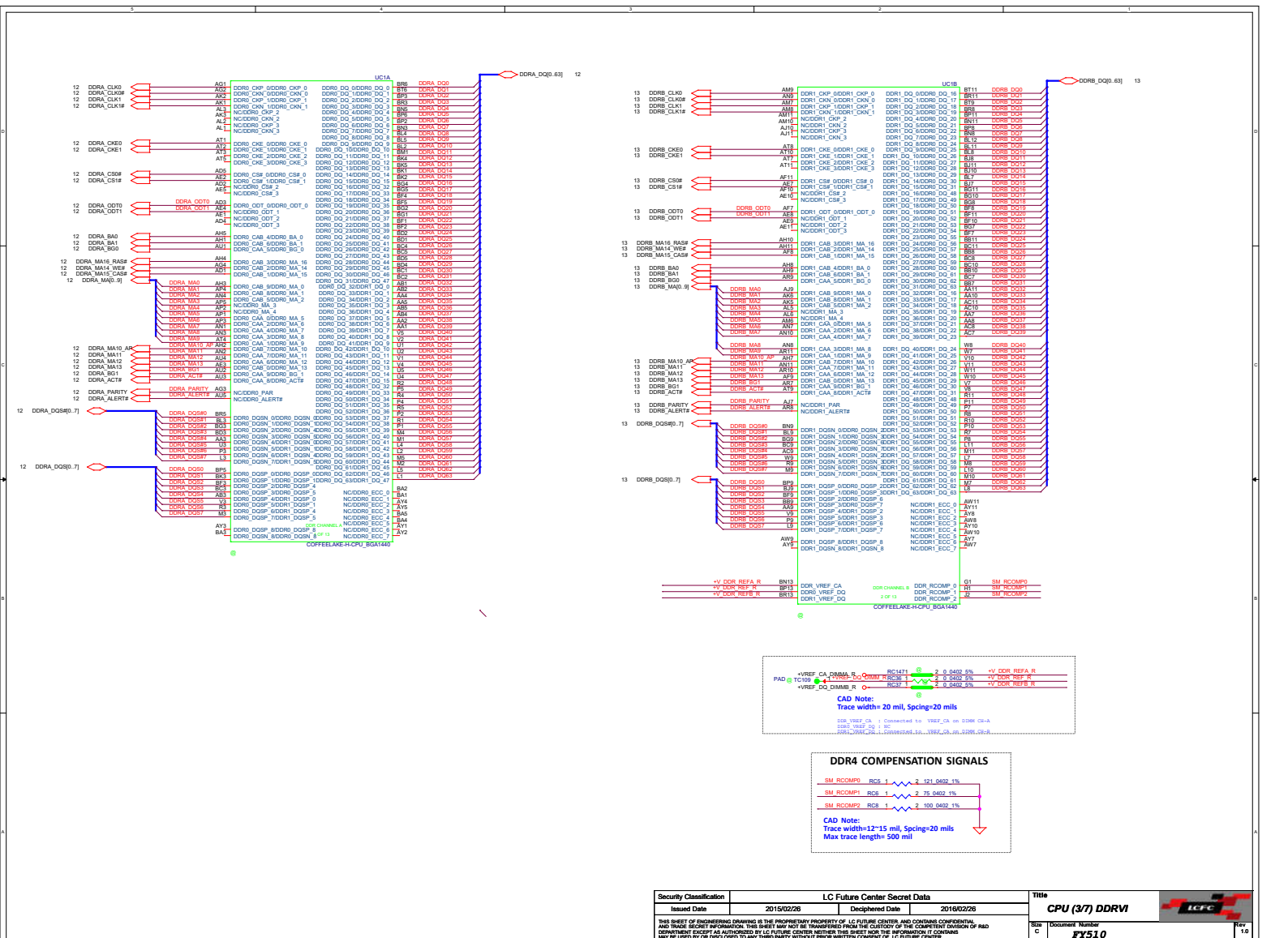
Reserved configuration lane	
CFG[19:8]	N/A

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (2/7) PM, XDP, CLK, CFG

Size: Custom | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018 | Sheet 8 of 75



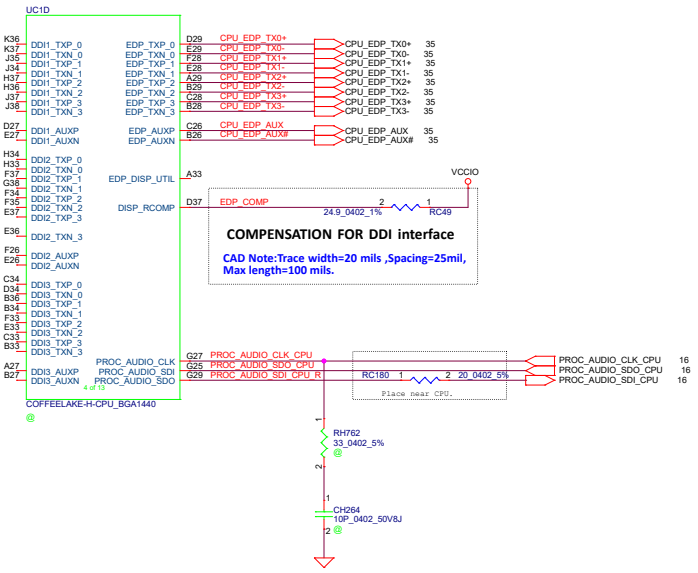
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: CPU (3/7) DDRVI

Size: C | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018 | Sheet 7 of 75

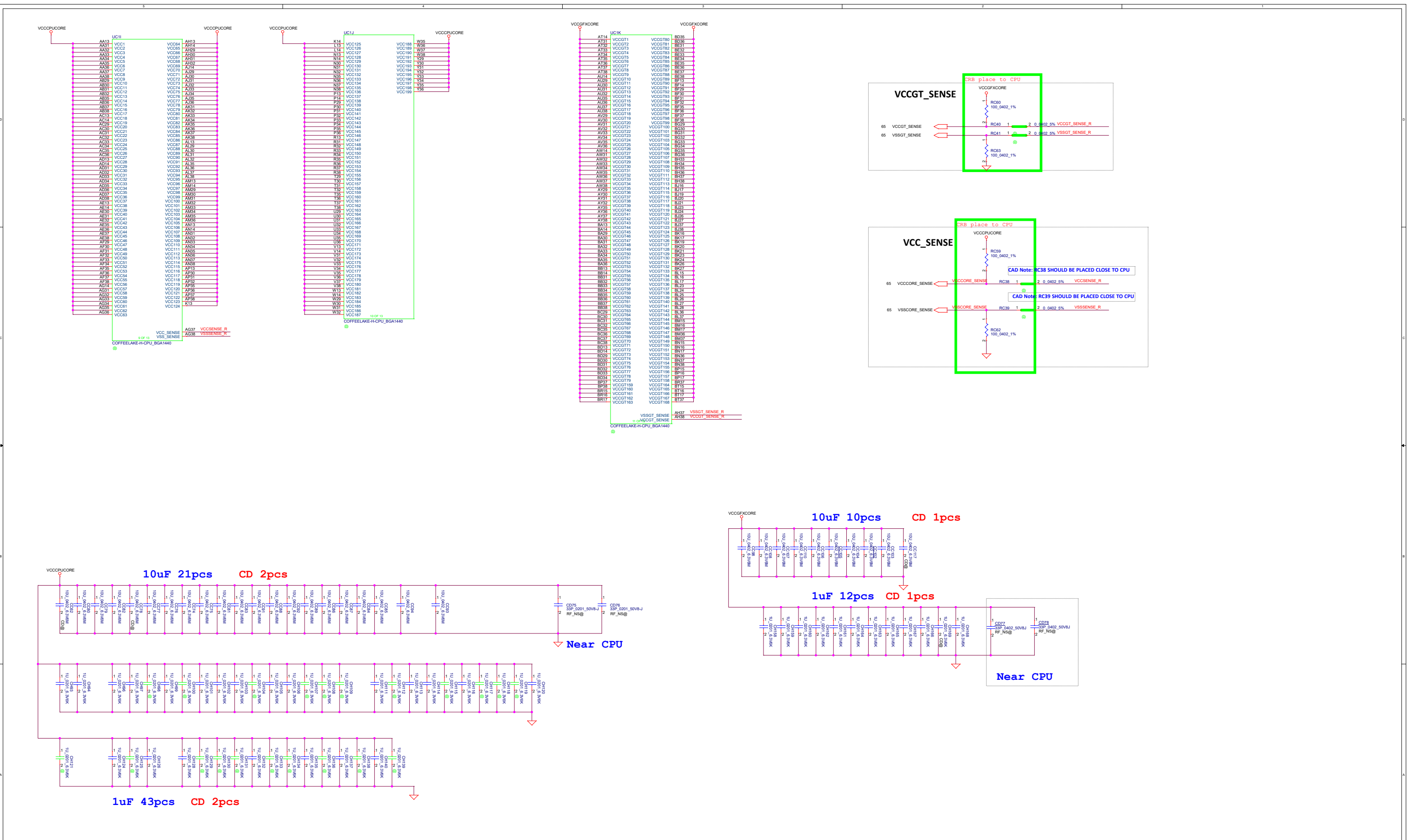


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (4/7) eDP, DDI

Size	Document Number	Rev
A3	FY510	1.0

Date: Monday, July 02, 2018 Sheet 8 of 75

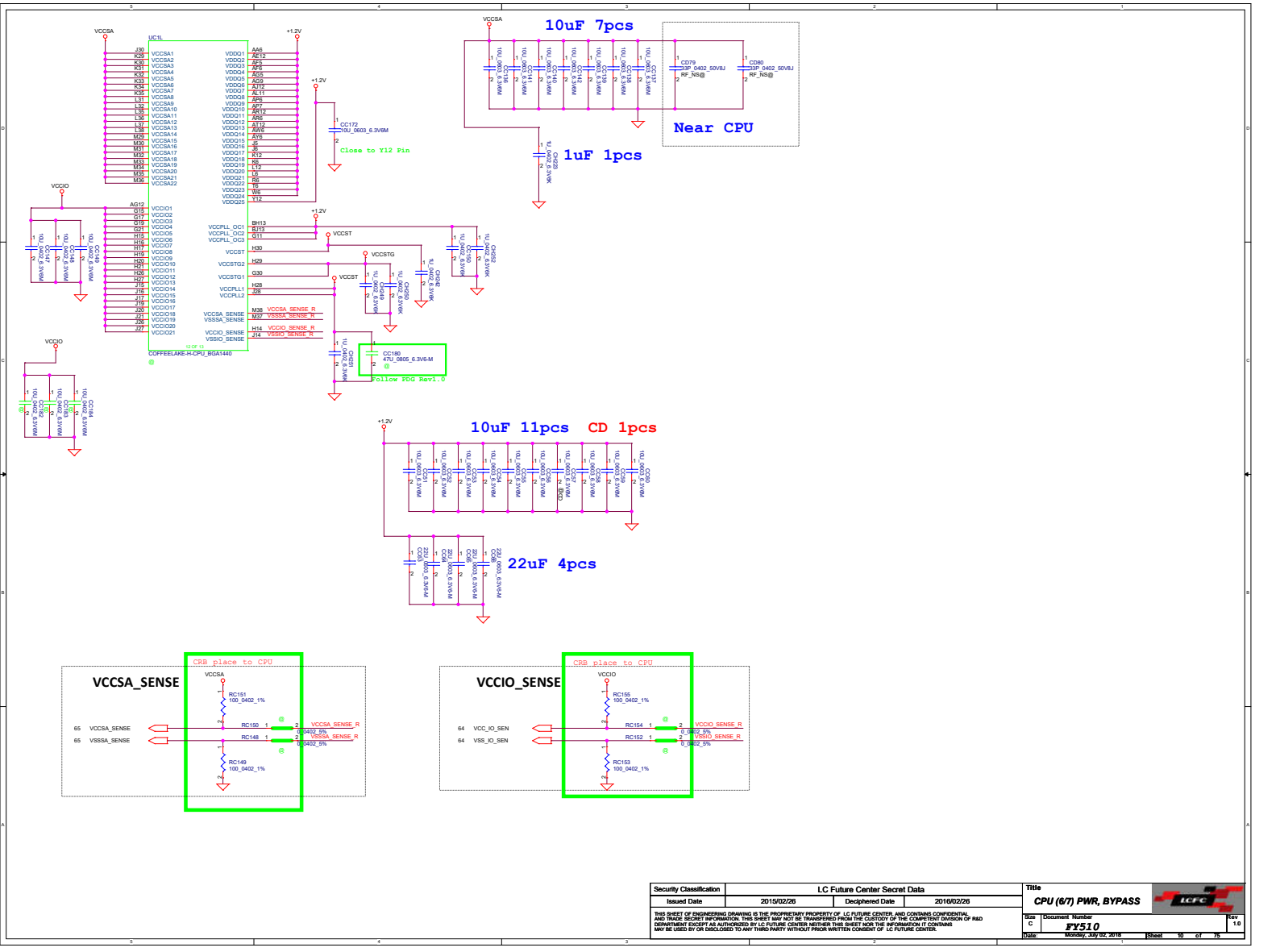


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **CPU (5/7) PWR, BYPASS**

Size	Document Number	Rev
D	FY510	1.0

Date: Monday, July 02, 2018 | Sheet 9 of 75

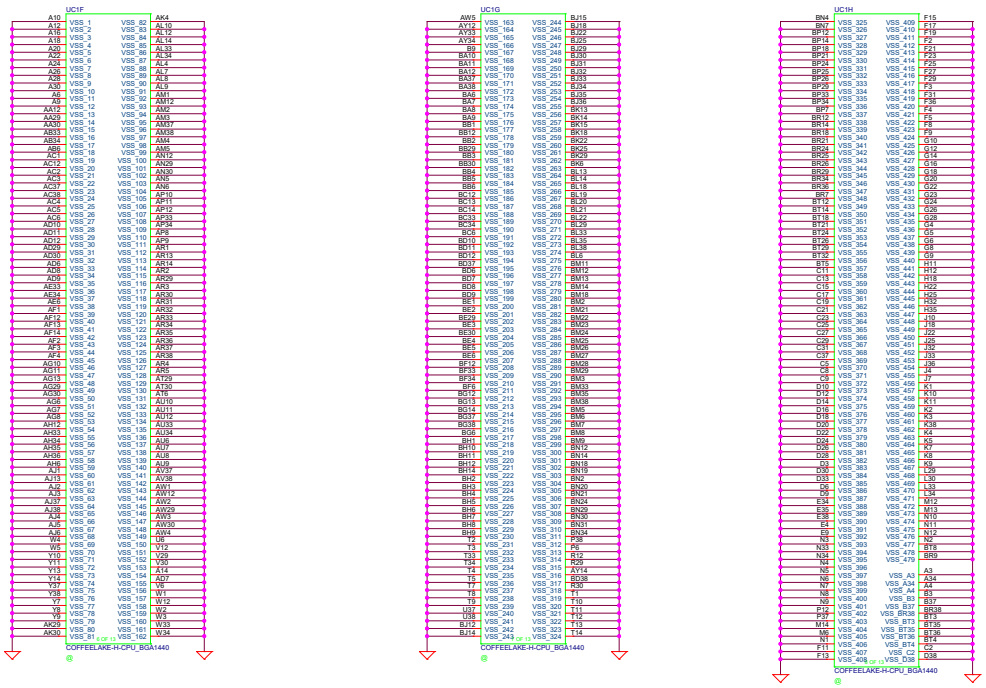


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: CPU (6/7) PWR, BYPASS

Size: C | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018 | Sheet 10 of 75

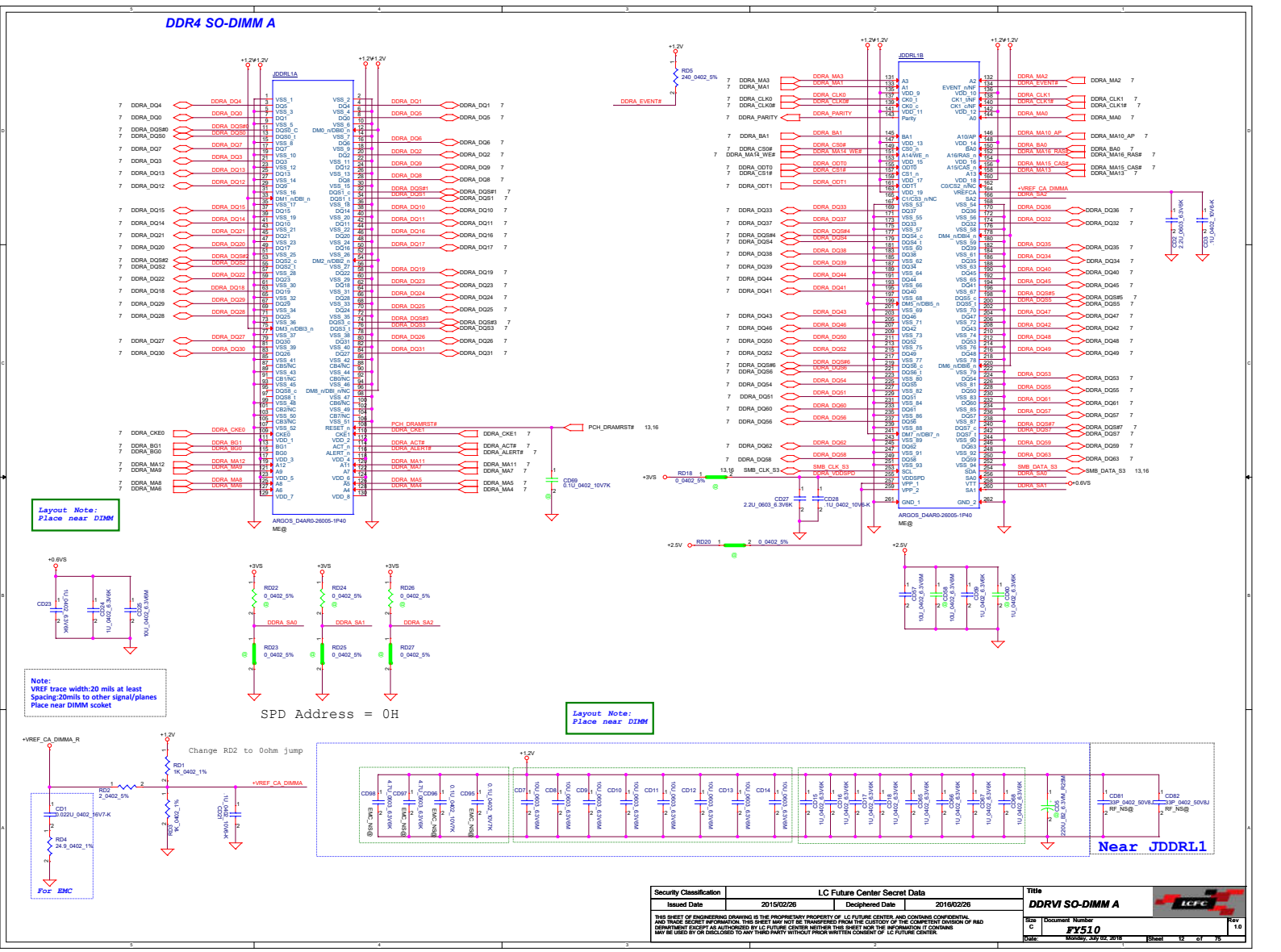


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **CPU (6/7) PWR, VSS**

Size	Document Number	Rev
C	FY510	1.0

Date: Monday, July 02, 2018 Sheet 11 of 75



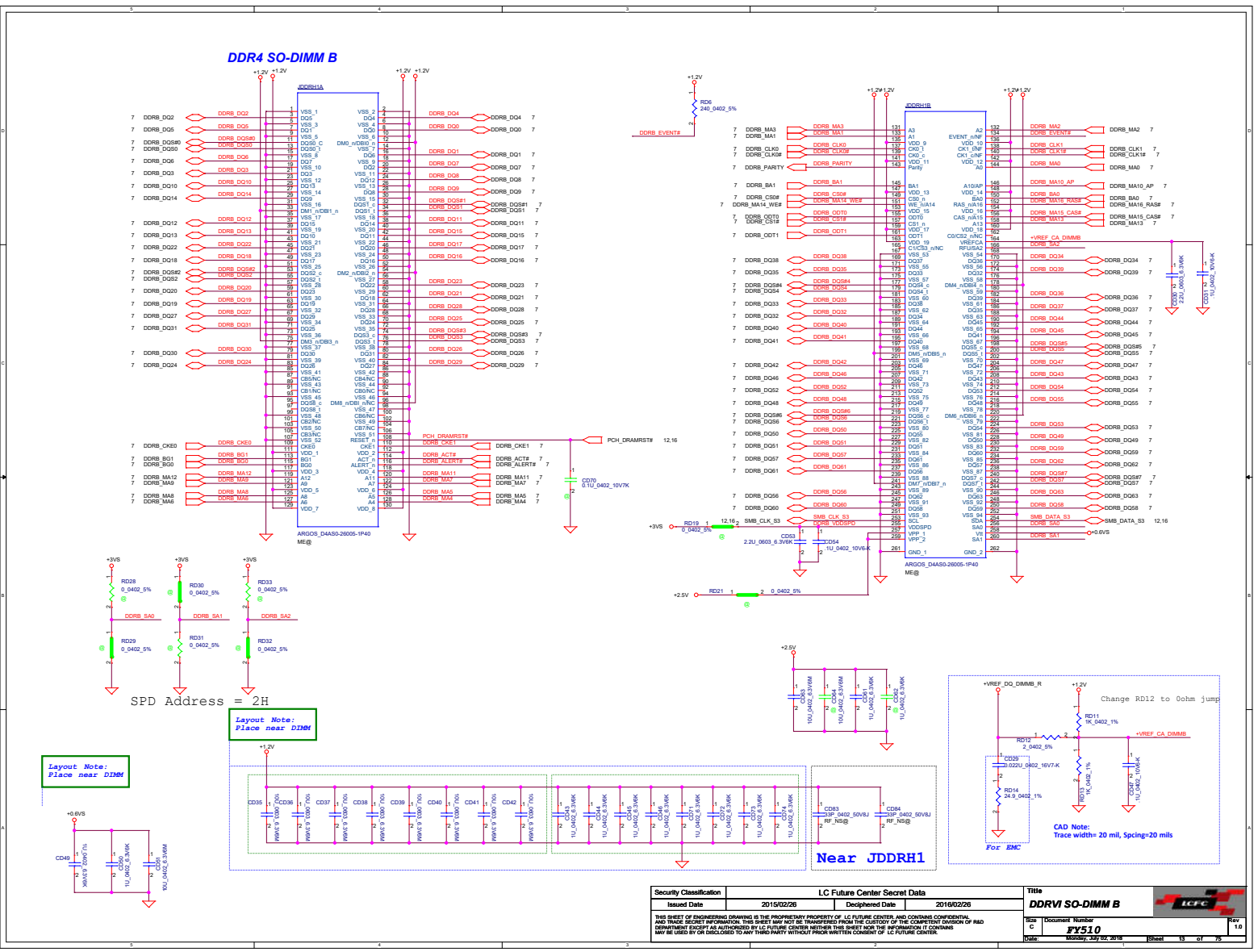
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: DDRVI SO-DIMM A

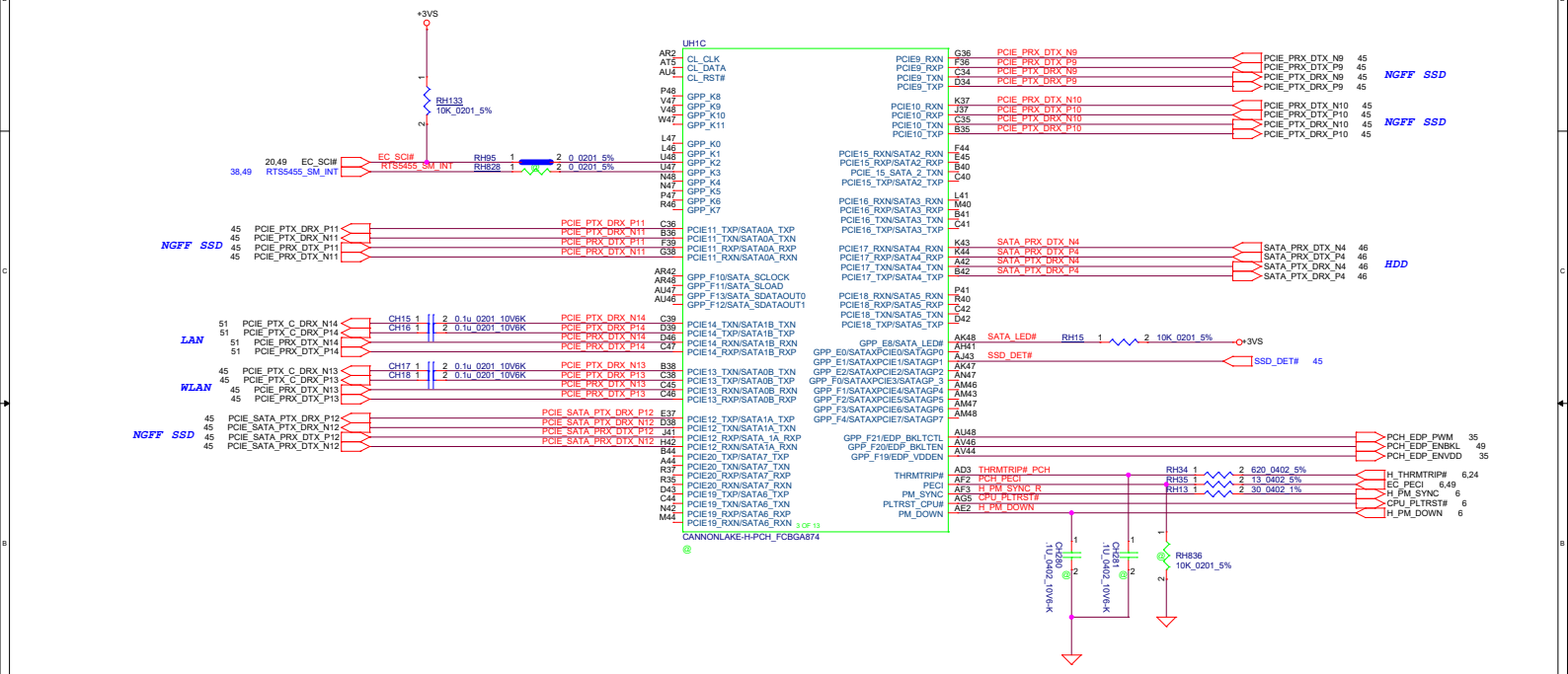
Size: C | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018 | Sheet 12 of 75



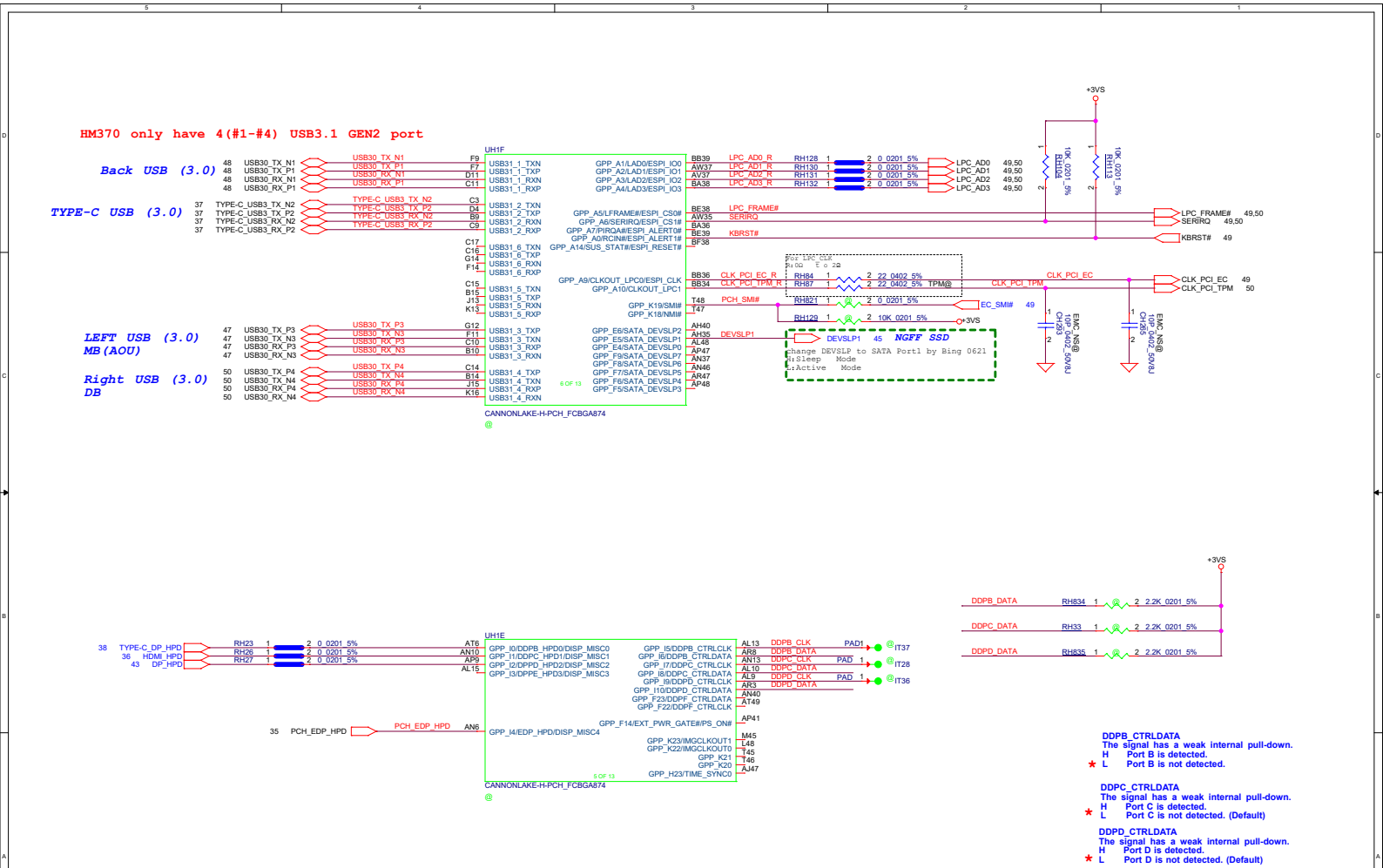
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	Size	Document Number	Rev
DDRVI SO-DIMM B	C	FY510	1.0
	Date: Monday, July 02, 2018	Sheet 13 of 75	



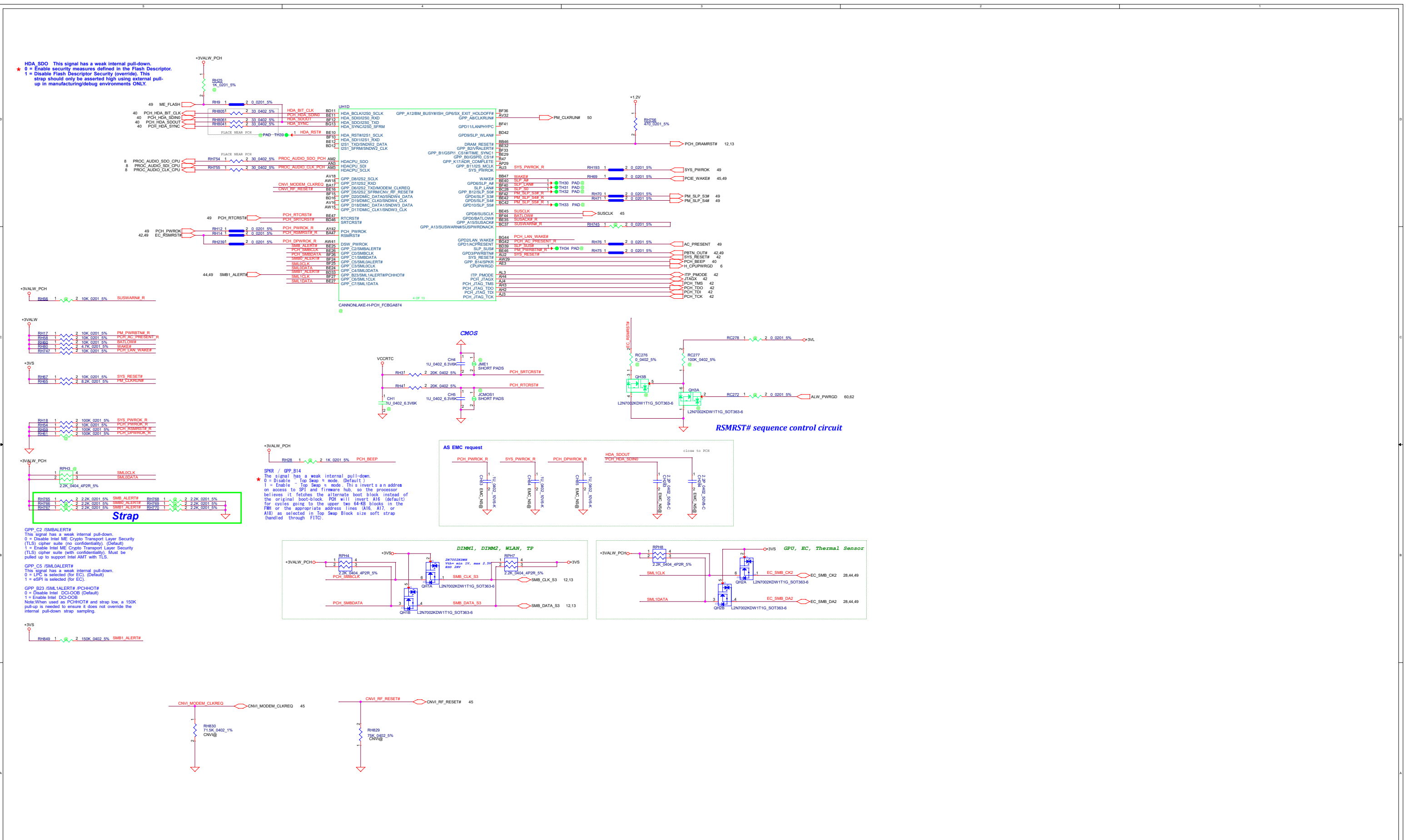
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	PCH (1/9) PCIe/SATA/GPPFG		
Size A3	Document Number FY510		Rev 1.0
Date: Monday, July 02, 2018	Sheet 14 of 75		



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	PCH (2/9) USB3/GPPAEFGHI		
Size	Document Number		Rev
A3	FY510		1.0
Date:	Monday, July 02, 2018	Sheet	15 of 75



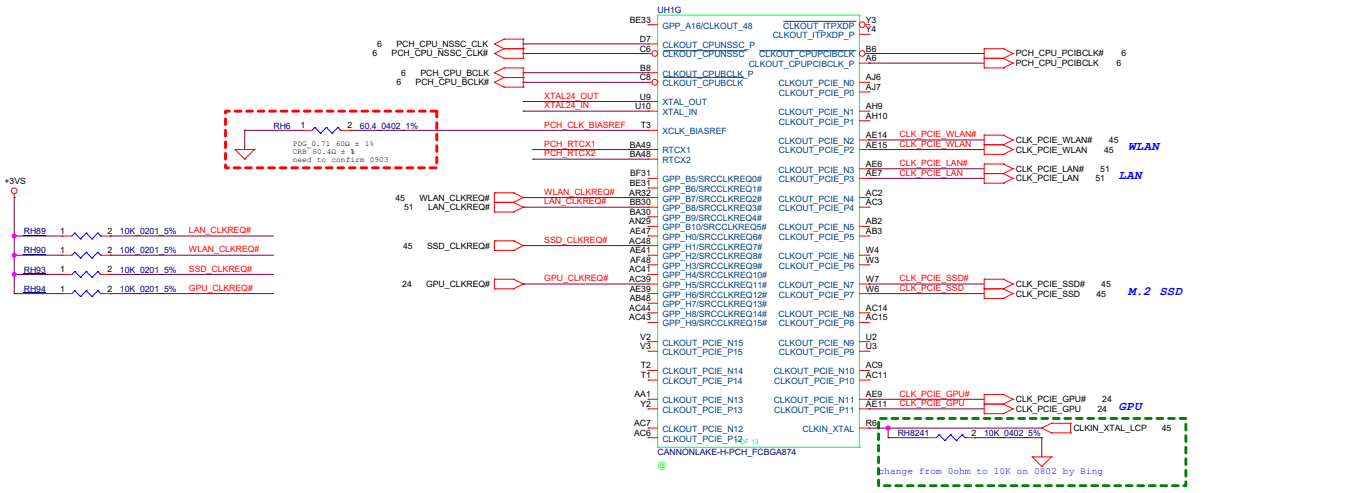
HDA_SDO This signal has a weak internal pull-down.
★ 0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
PLACE NEAR PCH
CANNONLAKE-H-PCH_FCBGA874
CMOS
RSMRST# sequence control circuit
AS EMC request
Strap
SPKR / GPP_B14
The signal has a weak internal pull-down.
★ 0 = Disable " Top Swap " mode. (Default)
1 = Enable " Top Swap " mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (handled through FITC).
GPP_C2 /SMBALERT#
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
GPP_C5 /SML0ALERT#
This signal has a weak internal pull-down.
0 = LPC is selected (for EC). (Default)
1 = eSPI is selected (for EC).
GPP_B23 /SML1ALERT# /PCHHOT#
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
Note:When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
DIMM1, DIMM2, WLAN, TP
GPU, EC, Thermal Sensor

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (3/9) HDA,RTC,SMBUS,PM

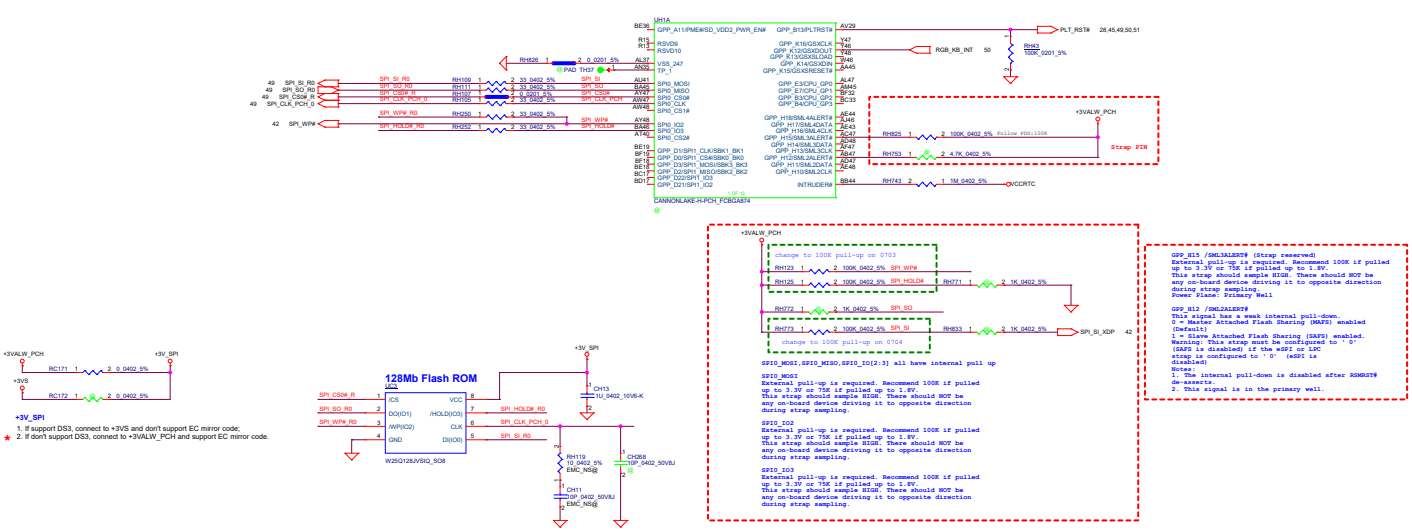
Size	Document Number	Rev
D	FY510	1.0

Date: Monday, July 02, 2018



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	PCH (3/9) CLOCK,GPPBH		
Size A3	Document Number FY510		Rev 1.0
Date: Monday, July 02, 2018	Sheet 17 of 75		



GPP_H15 /SML3ALERT# (Strap reserved)
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
Power Plane: Primary Well

GPP_H12 /SML2ALERT#
This signal has a weak internal pull-down.
0=Disable Attached Flash Sharing (SAFS) enabled.
Default
1= Slave Attached Flash Sharing (SAFS) enabled.
Warning: This strap must be configured to ' 0' (SAFS is disabled) if the eSPI or LPC strap is configured to ' 0' (eSPI is disabled)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+3V_SPI

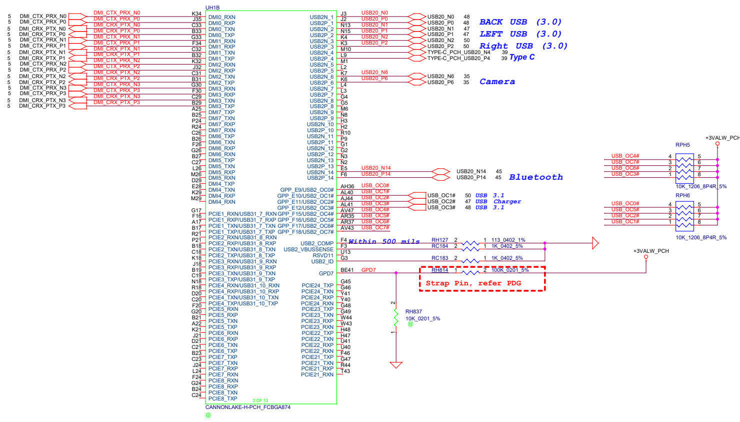
1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

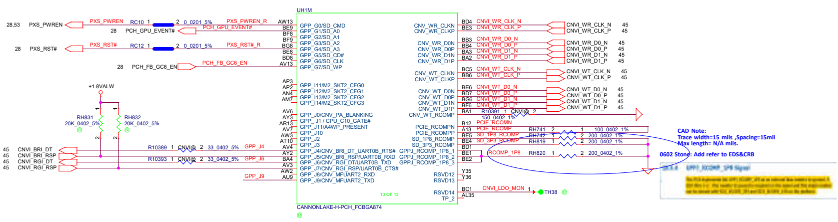
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

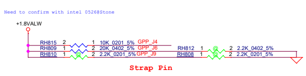
Title: PCH (5/9) SPI,SMBUS,GPPBEGH

Size	Document Number	Rev
A2	FY510	1.0

Date: Monday, July 02, 2018 Sheet 18 of 75







Primary Well Group J (1.8 V Only)

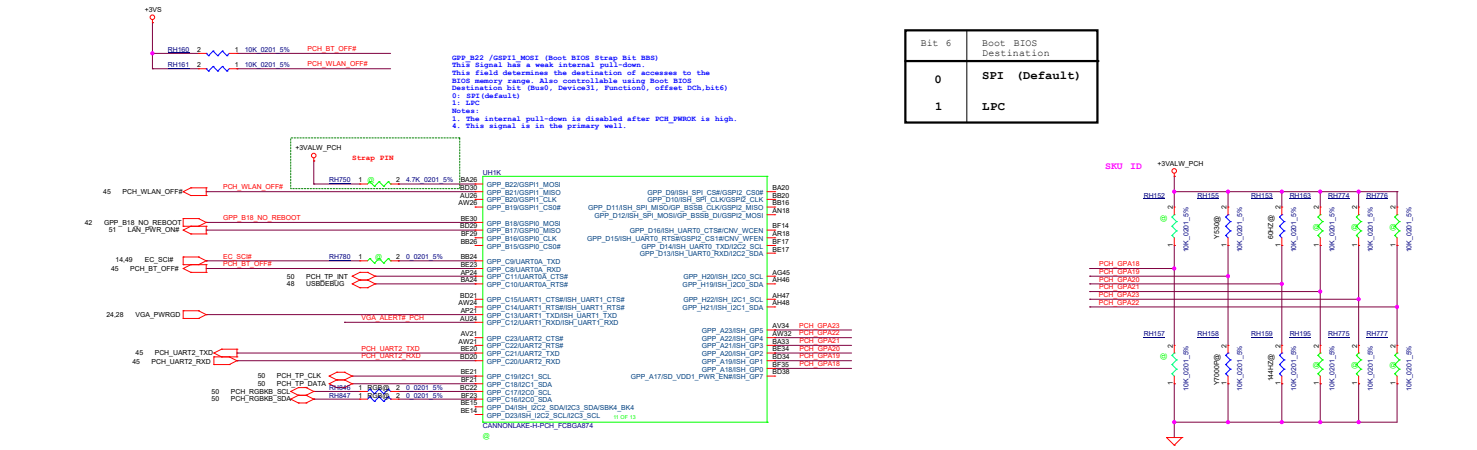
Signal	Usage	When Sampled	Comment
GPP_J4 / CNV_BRI_DT / UART0_RTS#	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. **Notes:** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_J6 / CNV_RGI_DT / UART0_TXD	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.
GPP_J9	1.8V VCCPSPI	Rising edge of RSMRST#	The signal has a weak internal pull-down 0 = VCCSPI is connected to 3.3V rail 1 = VCCSPI is connected to 1.8V rail **Note:** If VCCSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

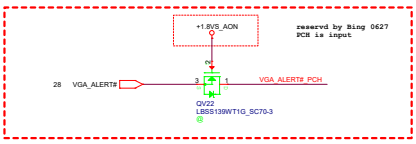
Title: **Blank**

Size: Custom | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018



Bit 6	Boot BIOS Destination
0	SPI (Default)
1	LPC



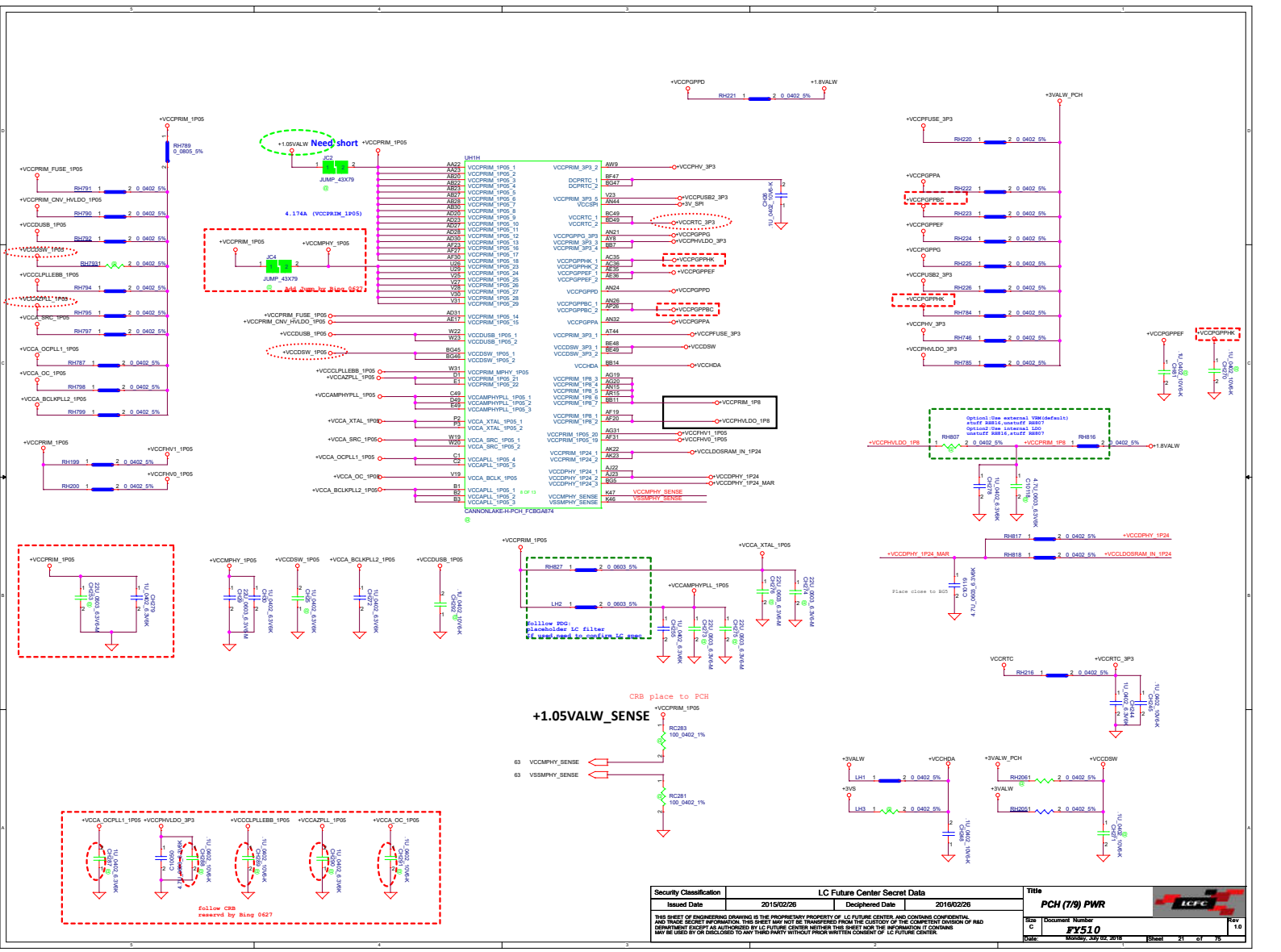
Function	PCH_GPA18	PCH_GPA19	PCH_GPA20	PCH_GPA21	PCH_GPA22	PCH_GPA23
1050	0	0	X	X	X	X
1050Ti	1	0	X	X	X	X
1060	X	1	X	X	X	X
Y530	X	X	1	X	X	X
Y7000P	X	X	0	X	X	X
PCIE SSD	X	X	X	X	X	X
Optane memory	X	X	X	X	X	X

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: PCH (6/9) GPPPABCD, I2C

Size	Document Number	Rev
C	FY510	1.0

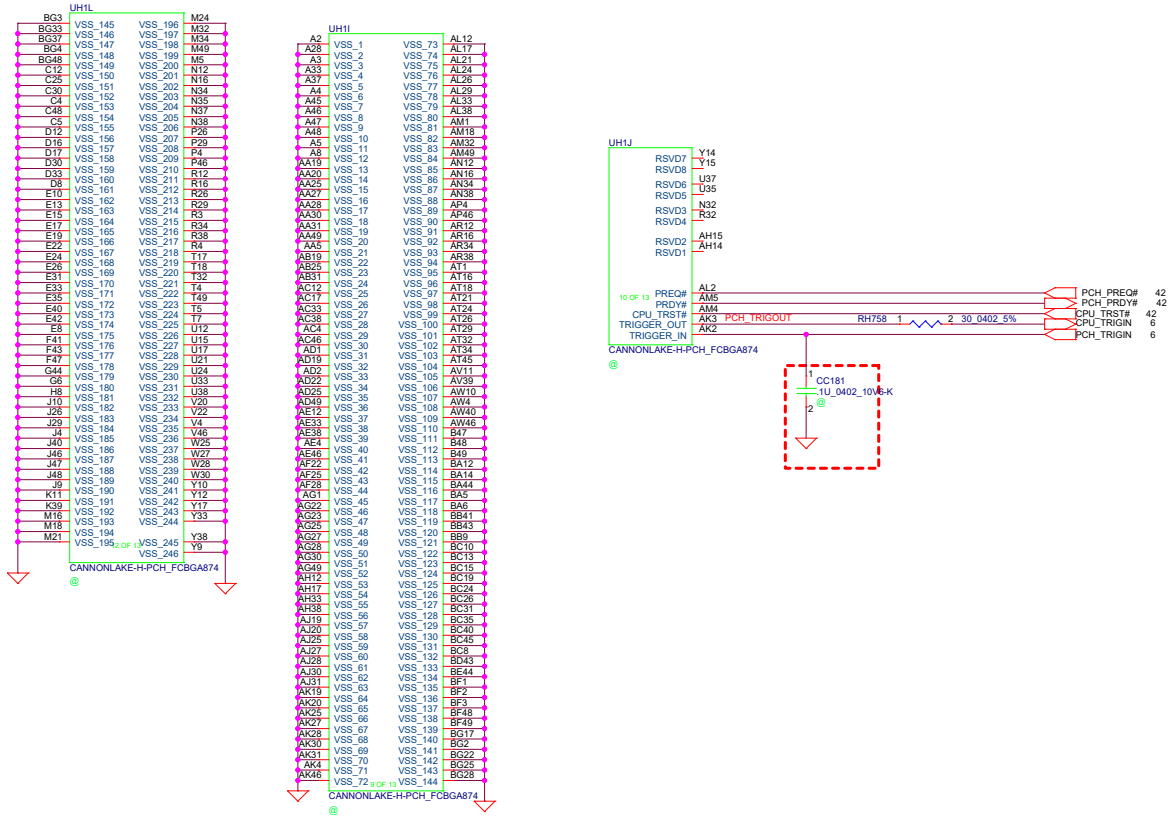
Date: Monday, July 02, 2018 Sheet 20 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	PCH (7/9) PWR		
Size	Document Number		Rev
C	FY510		1.0
Date:	Monday, July 02, 2018	Sheet	21 of 75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *PCH (9/9) VSS*

Size	Document Number	Rev
B	*FY510*	1.0

Date: Monday, July 02, 2018 Sheet 22 of 75

N17E-G1 GPIO

GPIO	I/O	ACTIVE	Function Description	I/O Termination
GPIO0	OUT	-	PWM Output to control NVVDD	
GPIO1	OUT	-	FB Enable for GC6 2.1	
GPIO2	IN	-	GPU wake signal for GC6 2.1	
GPIO3	OUT	-	PWM Output to control the SRAM power supply	
GPIO4	OUT	-	GPU power sequencing for GC6 2.1 --- 1V8_MAIN_EN	
GPIO5	IN	N/A	Active low Frame Lock	
GPIO6	OUT	-	Phase Shedding, NVVDD_PSI	
GPIO7	OUT	N/A	Panel Backlight enable	
GPIO8	OUT	-	Memory voltage Control	
GPIO9	I/O	-	Active Low Thermal Alert	
GPIO10	OUT	-	Memory VREF Control	(100K pull Down)
GPIO11	OUT	-	Panel Power enable	
GPIO12	IN	-	AC power detect or power supply overdraw input	(10K pull High)
GPIO13	OUT	N/A	LCD Panel Backlight Enable	
GPIO14	IN	N/A	Hot Plug Detect for IFPA	
GPIO15	IN	N/A	Hot Plug Detect for IFPB	
GPIO16	OUT	-	System side PCIe reset monitor	
GPIO17	IN	N/A	Hot Plug Detect for IFPD	
GPIO18	IN	N/A	Hot Plug Detect for IFPE	
GPIO19	OUT	N/A	3D Vision L/R Signal	
GPIO20		N/A	GC5_MODE	
GPIO21	I/O	N/A	UNUSED	
GPIO22	I/O	N/A	UNUSED	
GPIO23	OUT	-	GPU PCIe self-reset control	
GPIO24	IN	N/A	Hot Plug Detect for IFPF	
GPIO25		N/A	UNUSED	
GPIO26		N/A	UNUSED	
GPIO27	IN	N/A	Hot Plug Detect for IFPC	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
L	L	L	1111 DEFAULT
L	L	H	1110
L	H	L	1101
L	H	H	1100
H	L	L	1011
H	L	H	1010
H	H	L	1001
H	H	H	1000
L	L	M	0111
L	M	L	0110
L	M	H	0101
L	H	M	0100
H	L	M	0011
H	M	L	0010
H	M	H	0001
H	H	M	0000

1:ENABLE 0:DISABLE
SOR0/1/2/3 ENABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

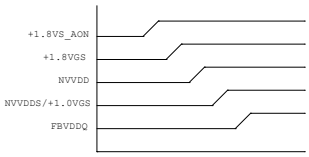
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

N17E-G1 Power Sequence

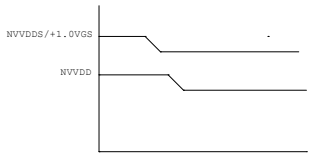


1. All power rail ramp up time should be larger than 40us and is recommended to be less than 2ms.

2. T (from 1V8_MAIN_EN to PEX_DVDD/NVVDD_Pgood) must NOT exceed 4ms.

3. All 3.3V devices that connect to the GPU must be powered after 1V8_AON; GPU can NOT have any 3.3V leakage path before 1V8_AON present.

4. The previous power rail must ramp up to 90% before the next power rail can start ramping up.



1. NVVDDS/PEX_DVDD must ramp down before NVVDD, all other power rails can ramp down together with NVVDD.

2. All 3.3V devices that connect to the GPU must be ramp down before 1V8_AON; GPU can NOT have any 3.3V leakage path after 1V8_AON and 1.8V_MAIN power down.

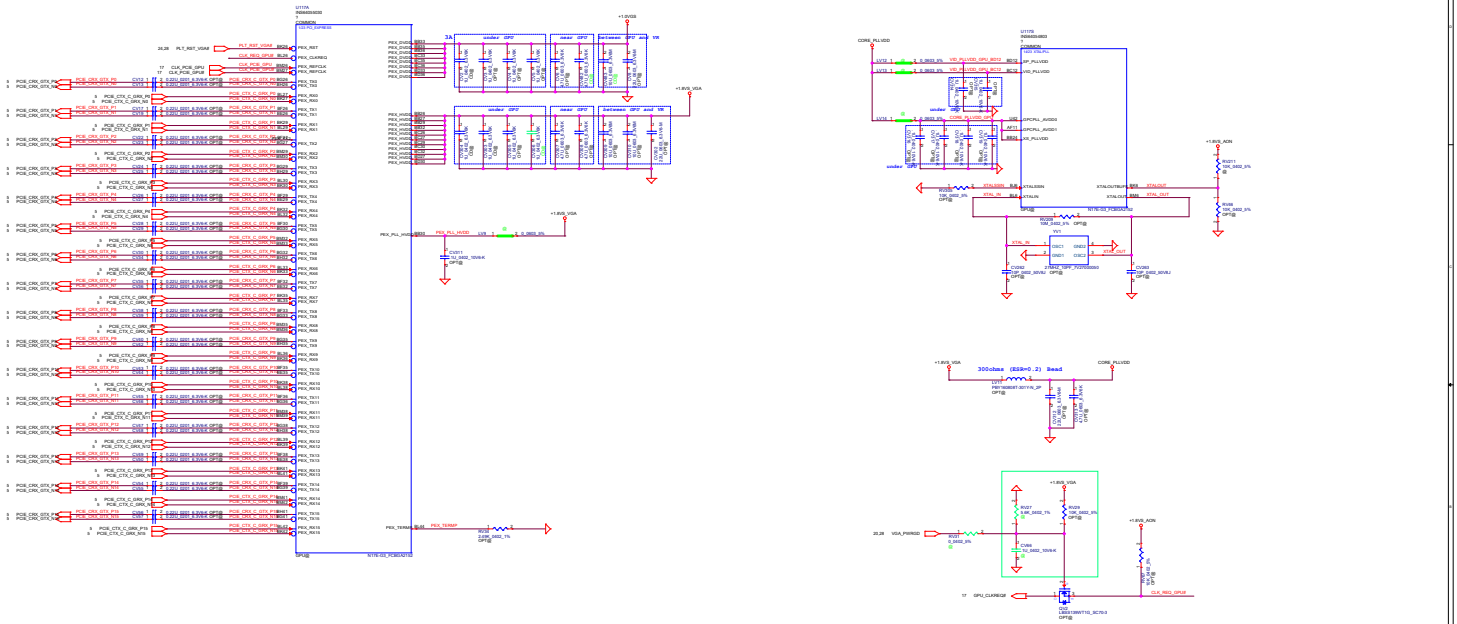
3. The previous power rail must ramp down to 10% before the next power rail can start ramping down.

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: VGA Notes List

Size	Document Number	Rev
C	FY510	1.0

Date: Monday, July 02, 2018 Sheet 23 of 75



choose one

For SWG mode

For UMA mode

updated by bing.gu 20180308

+1.8VGS Discharge

Vga(th)≤ 1.5V

Vga(th)≤ 1.5V

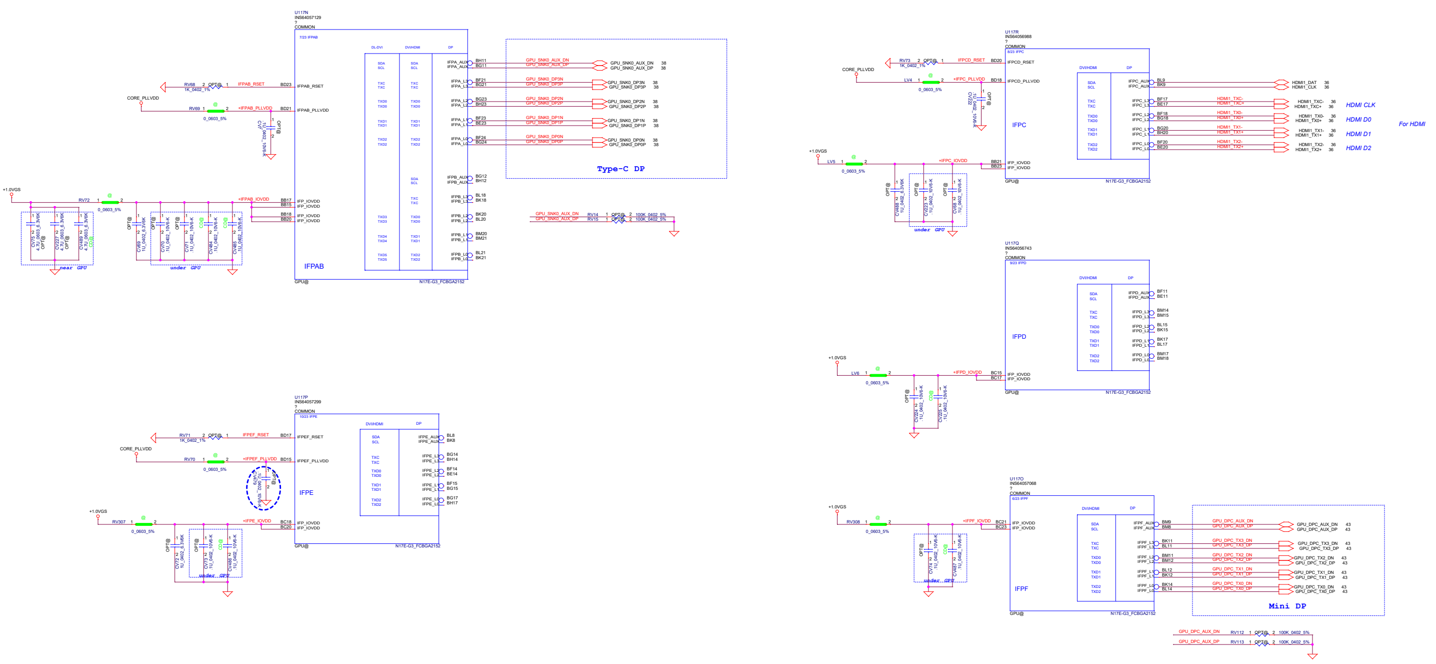
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. RECIPIENT AGREES NOT TO COPY, REPRODUCE, OR TRANSMIT THIS SHEET, OR ANY PORTION OF IT, WITHOUT THE WRITTEN PERMISSION OF LC FUTURE CENTER, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: N16P-GX_PEG 8F

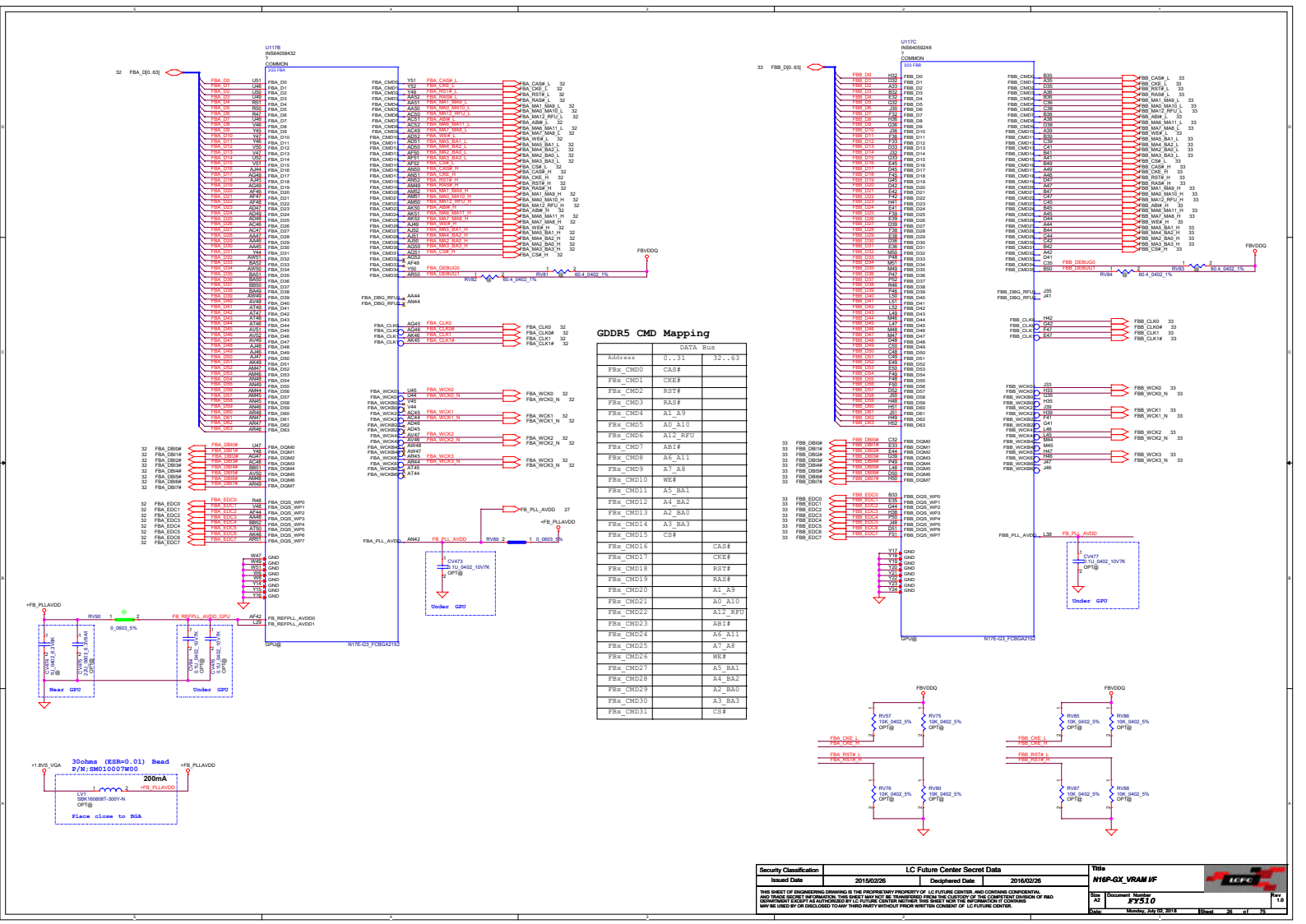
Size: B | Document Number: FY510 | Rev: 1.0

Date: Monday, July 09, 2018 | Sheet 38 of 46



Security Classification	LC Future Center Secret Data			Title
Issued Date	2015/02/26	Deciphered Date	2016/02/26	N16P-GX_DIGITAL OUT I/F

Size	Document Number	Rev
D	FY510	1.0



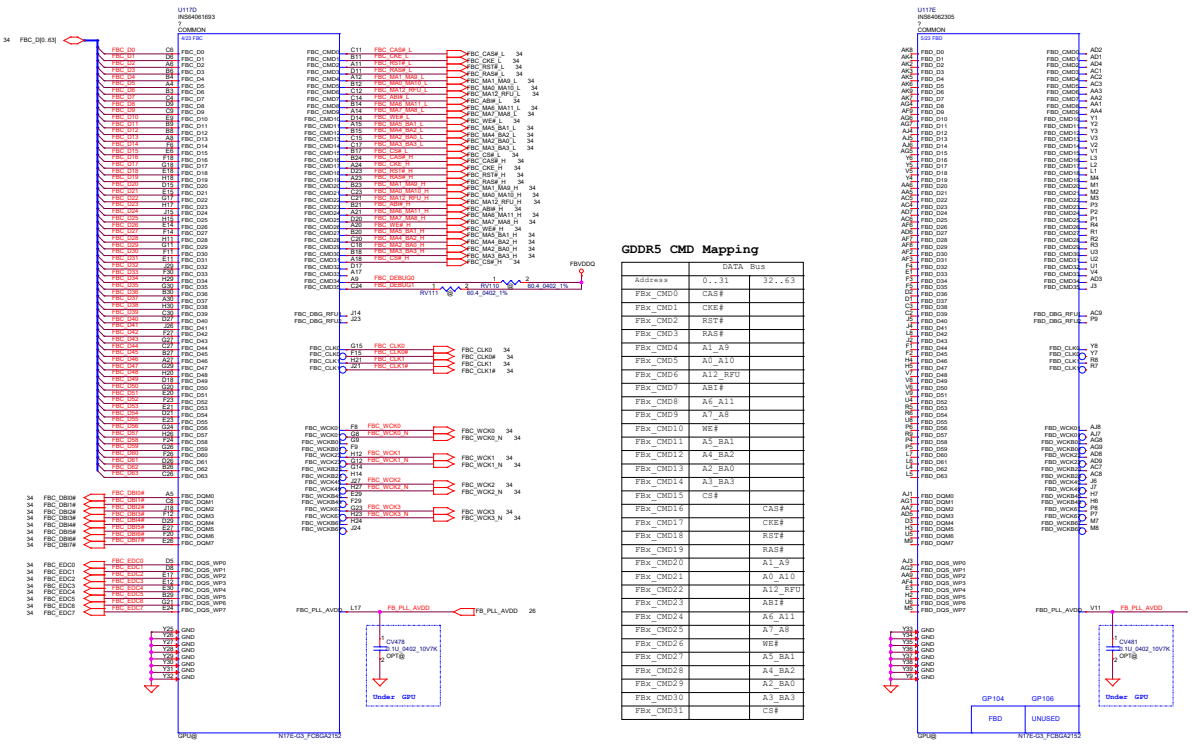
GDDR5 CMD Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CAS#	
FBx_CMD1	CKE#	
FBx_CMD2	RST#	
FBx_CMD3	RAS#	
FBx_CMD4	A1_A9	
FBx_CMD5	A0_A10	
FBx_CMD6	A12_RFU	
FBx_CMD7	ABI#	
FBx_CMD8	A6_A11	
FBx_CMD9	A7_A8	
FBx_CMD10	WE#	
FBx_CMD11	A5_BA1	
FBx_CMD12	A4_BA2	
FBx_CMD13	A2_BA0	
FBx_CMD14	A3_BA3	
FBx_CMD15	CS#	
FBx_CMD16		CAS#
FBx_CMD17		CKE#
FBx_CMD18		RST#
FBx_CMD19		RAS#
FBx_CMD20		A1_A9
FBx_CMD21		A0_A10
FBx_CMD22		A12_RFU
FBx_CMD23		ABI#
FBx_CMD24		A6_A11
FBx_CMD25		A7_A8
FBx_CMD26		WE#
FBx_CMD27		A5_BA1
FBx_CMD28		A4_BA2
FBx_CMD29		A2_BA0
FBx_CMD30		A3_BA3
FBx_CMD31		CS#

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. IT MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETITION DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	N16P-GX_VRAM I/F		
Size: A2	Document Number: P7510		Rev: 1.0
Date: Monday, July 02, 2018	Sheet 26 of 75		



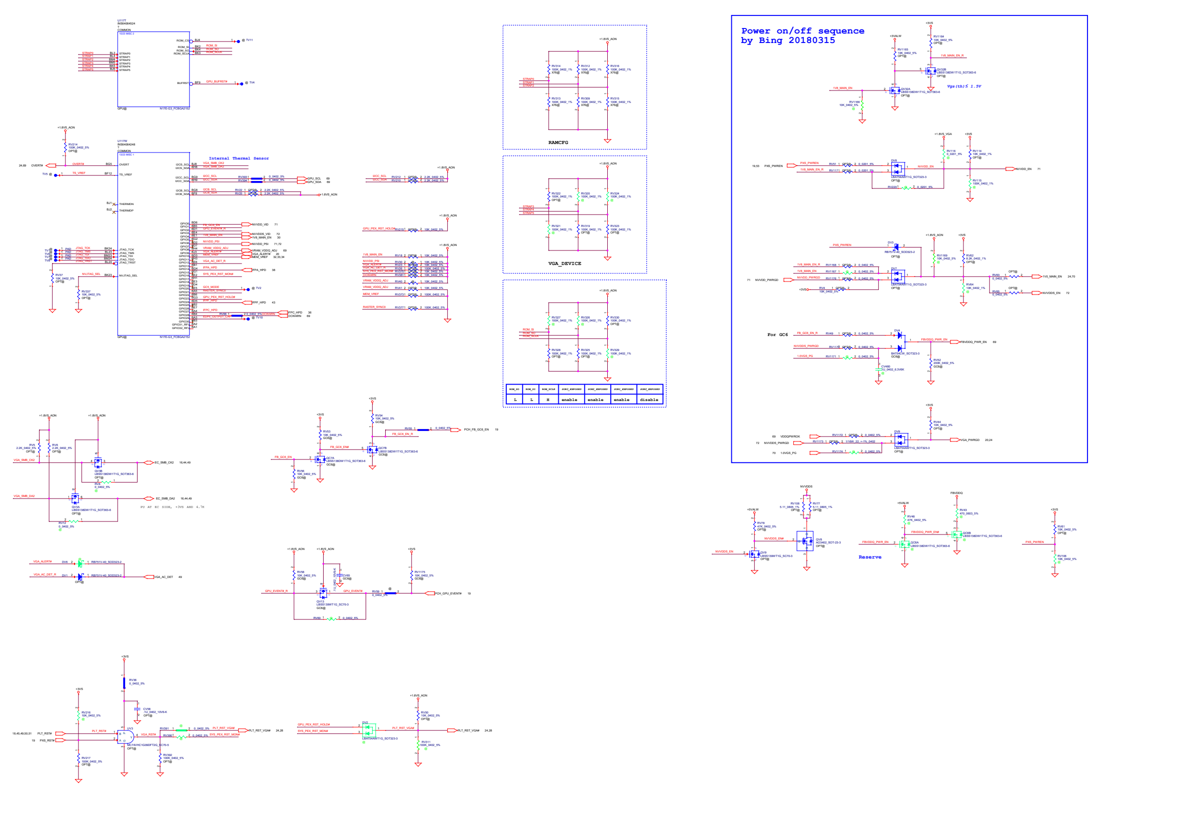
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: N17E-G1_VRAM C/D

Size	Document Number	Rev
A2	FX510	1.0

Date: Monday, July 02, 2018 Sheet 27 of 75



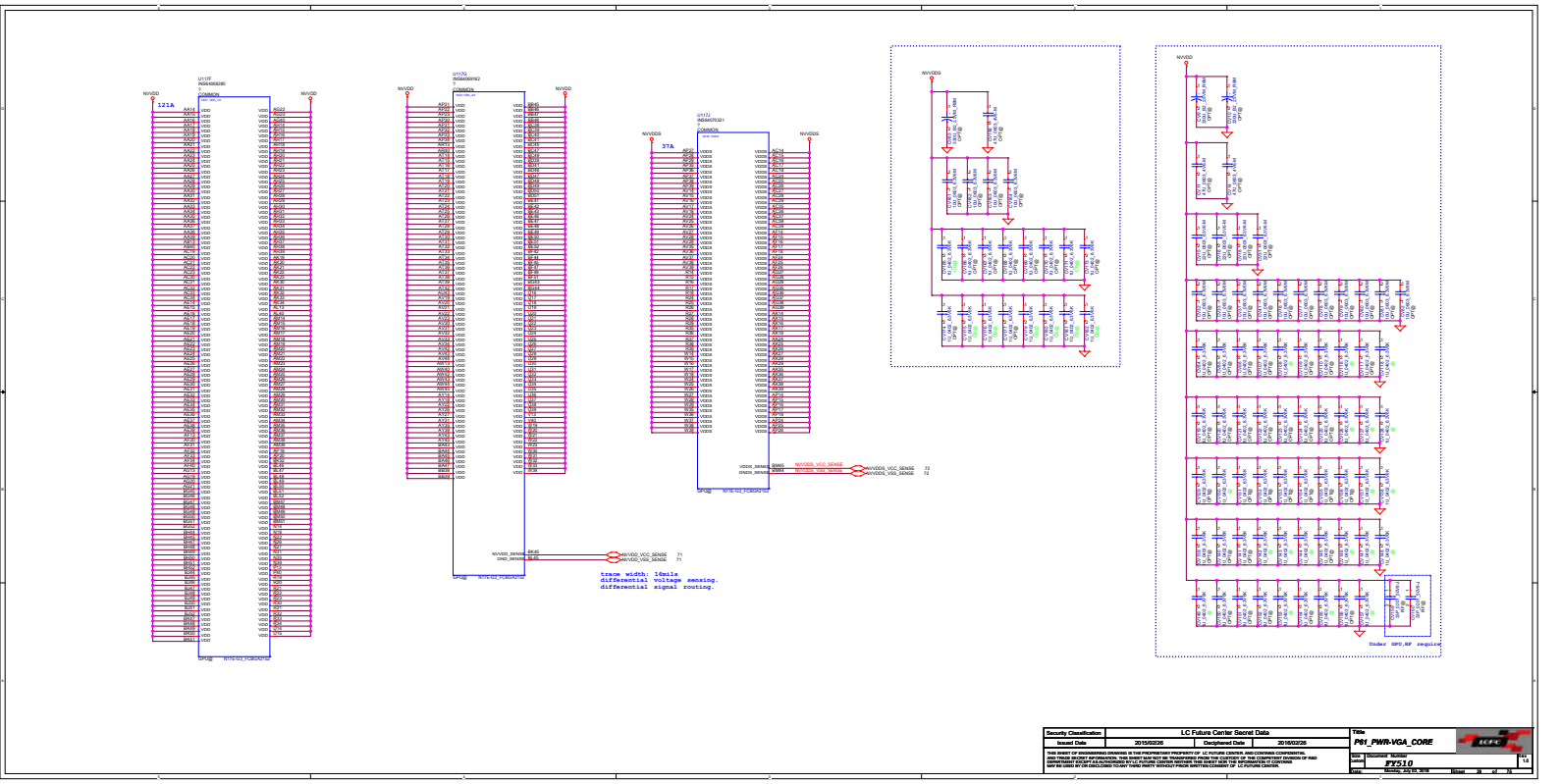
ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
L	L	H	enable	enable	enable	disable

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: N16P-GX_PEG I/F

Size: A0 | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018 |



Security Classification	LC Future Center Secret Data		
Issued Date	2015/03/26	Deciphered Date	2015/03/26

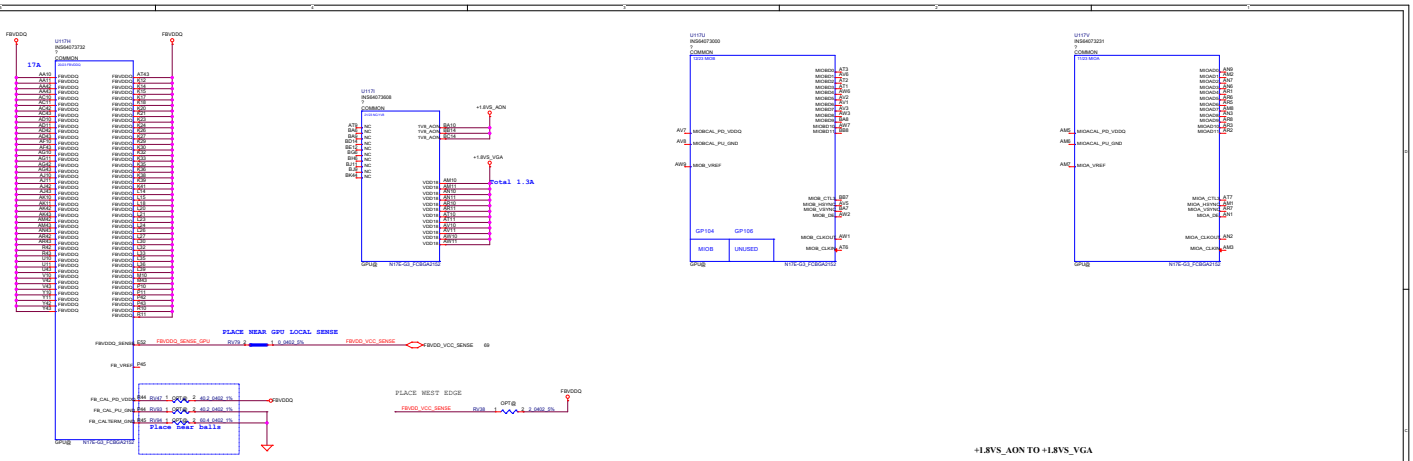
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. IT MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE ENGINEERING DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: P81_PWR-VGA_CORE

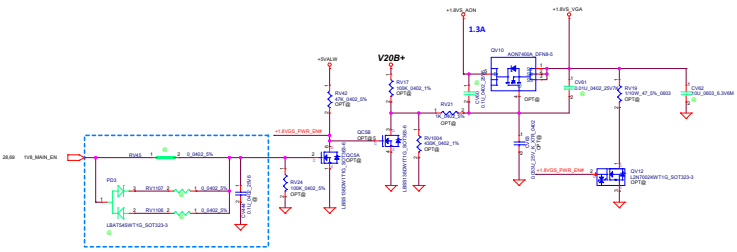
LCFC

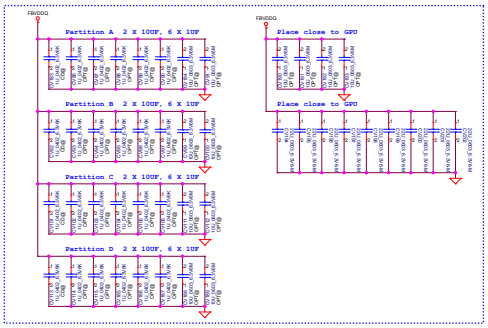
Size: A3 | Document Number: P7510 | Rev: 1.0

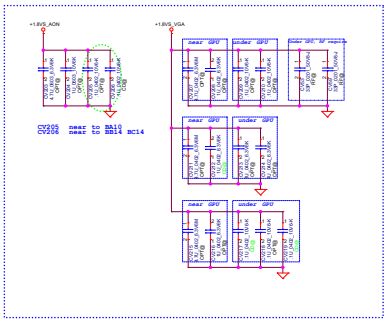
Date: Monday, July 06, 2015 | Sheet 26 of 73



+1.8VS_AON TO +1.8VS_VGA

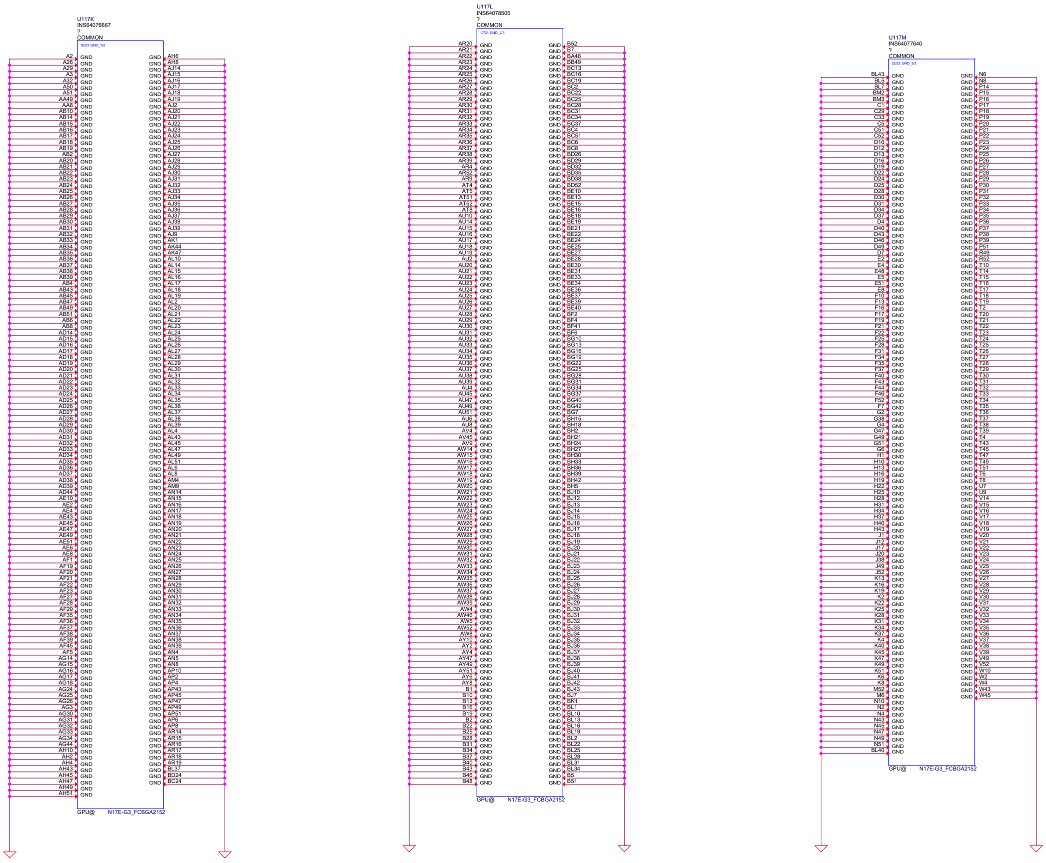






Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/02/26	Deciphered Date	2016/02/26
			POWER

Size	Document Number	Rev
C	FX510	1.0
Date:	Monday, July 04, 2016	Sheet 30 of 39

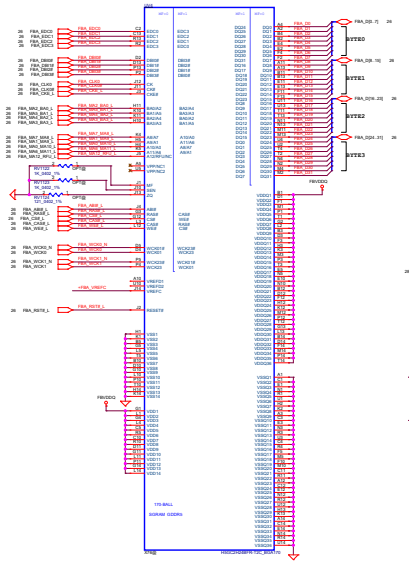


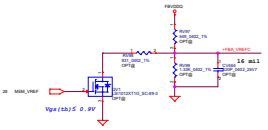
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

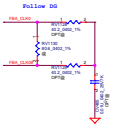
Title: **GND**

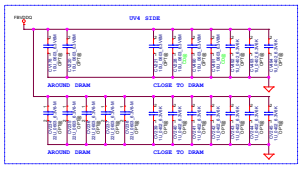
Size	Document Number	Rev
Custom	FY510	1.0

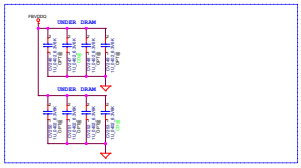
Memory - Lower 32 bits



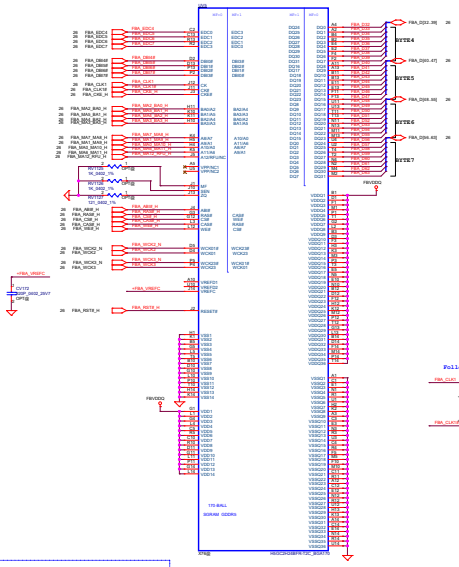


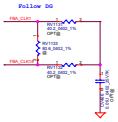


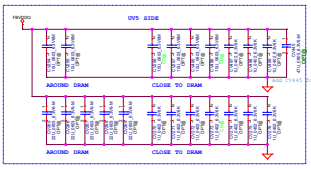


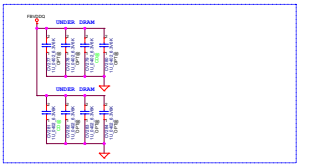


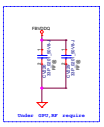
Memory - Upper 32 bits









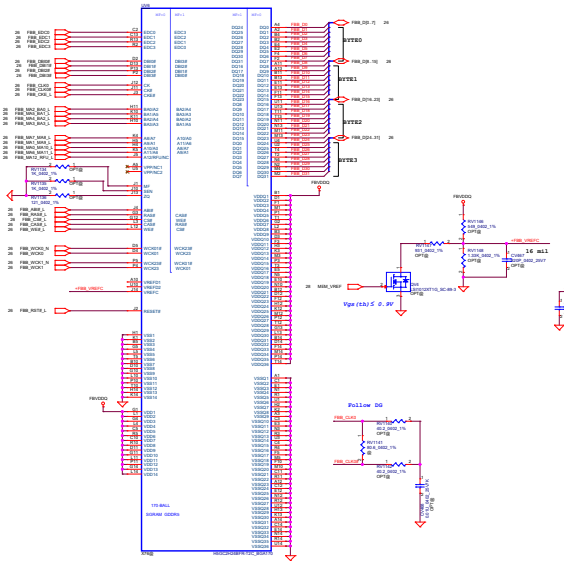


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

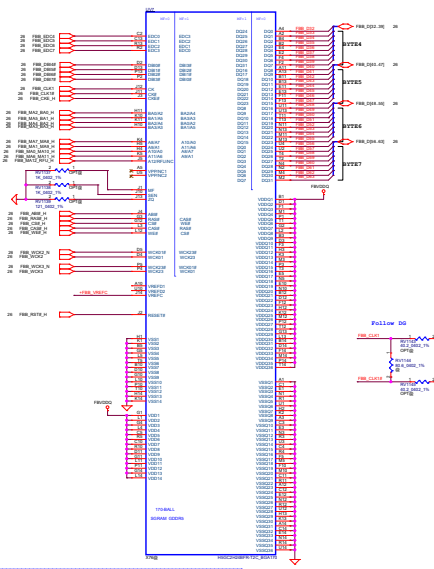
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPANY OR REVISED BY ANY DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

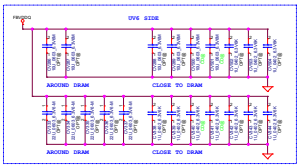
Title	
	N16P-GX_VRAM A Lower
Size: B	Document Number: PX510
Date: Monday, July 06, 2015	Sheet 38 of 46

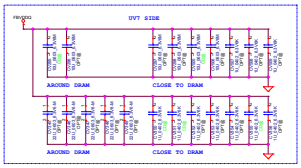
Memory - Lower 32 bits

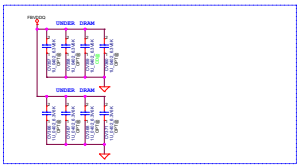


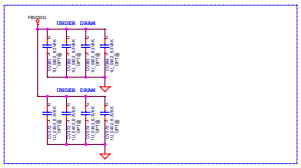
Memory - Upper 32 bits









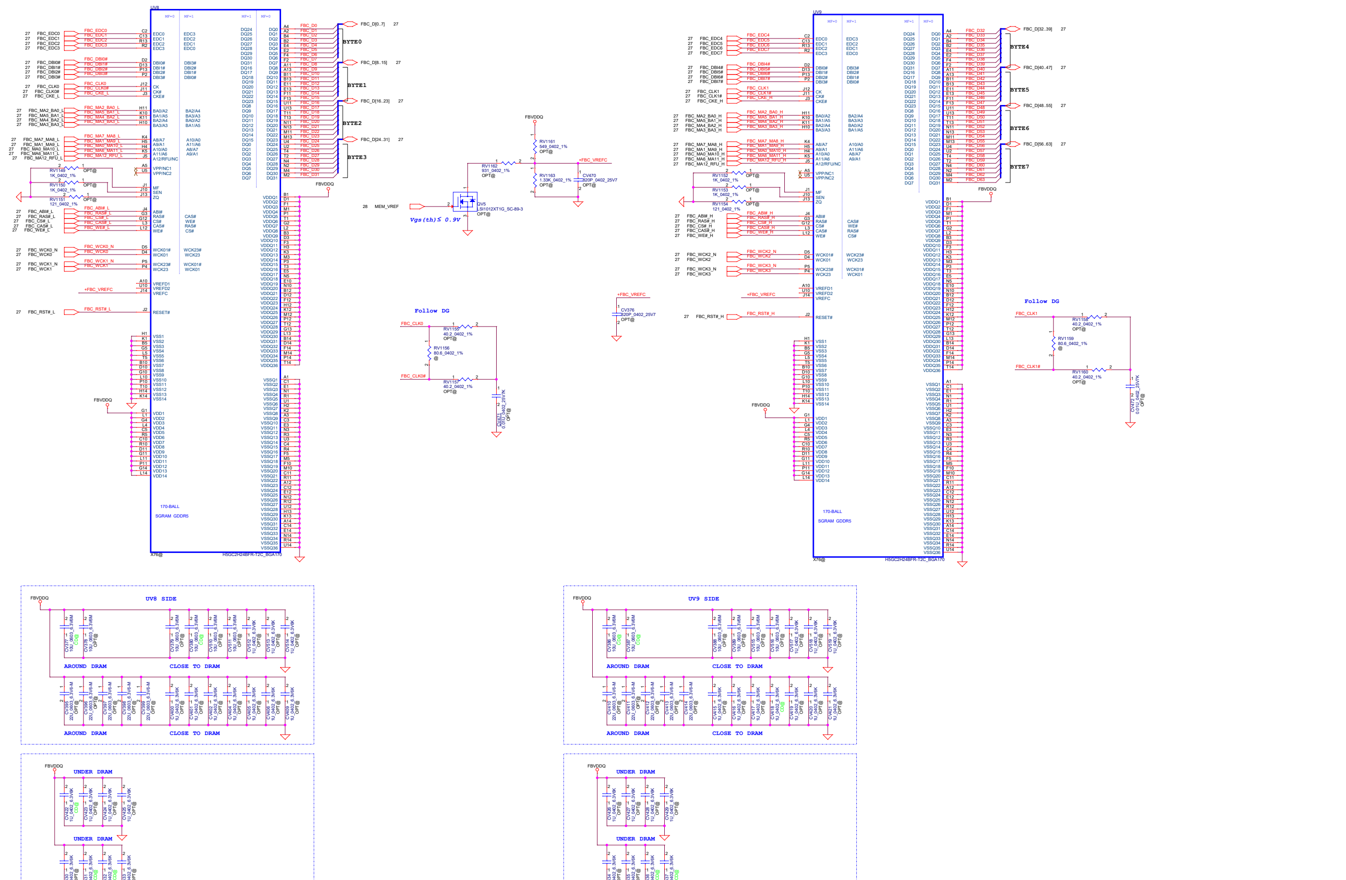


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	
	N16P-GX_VRAM A Lower
Size: B	Document Number: FX510
Date: Monday, July 06, 2015	Sheet 18 of 36

Memory Partition C - Lower 32 bits

Memory Partition C - Upper 32 bits



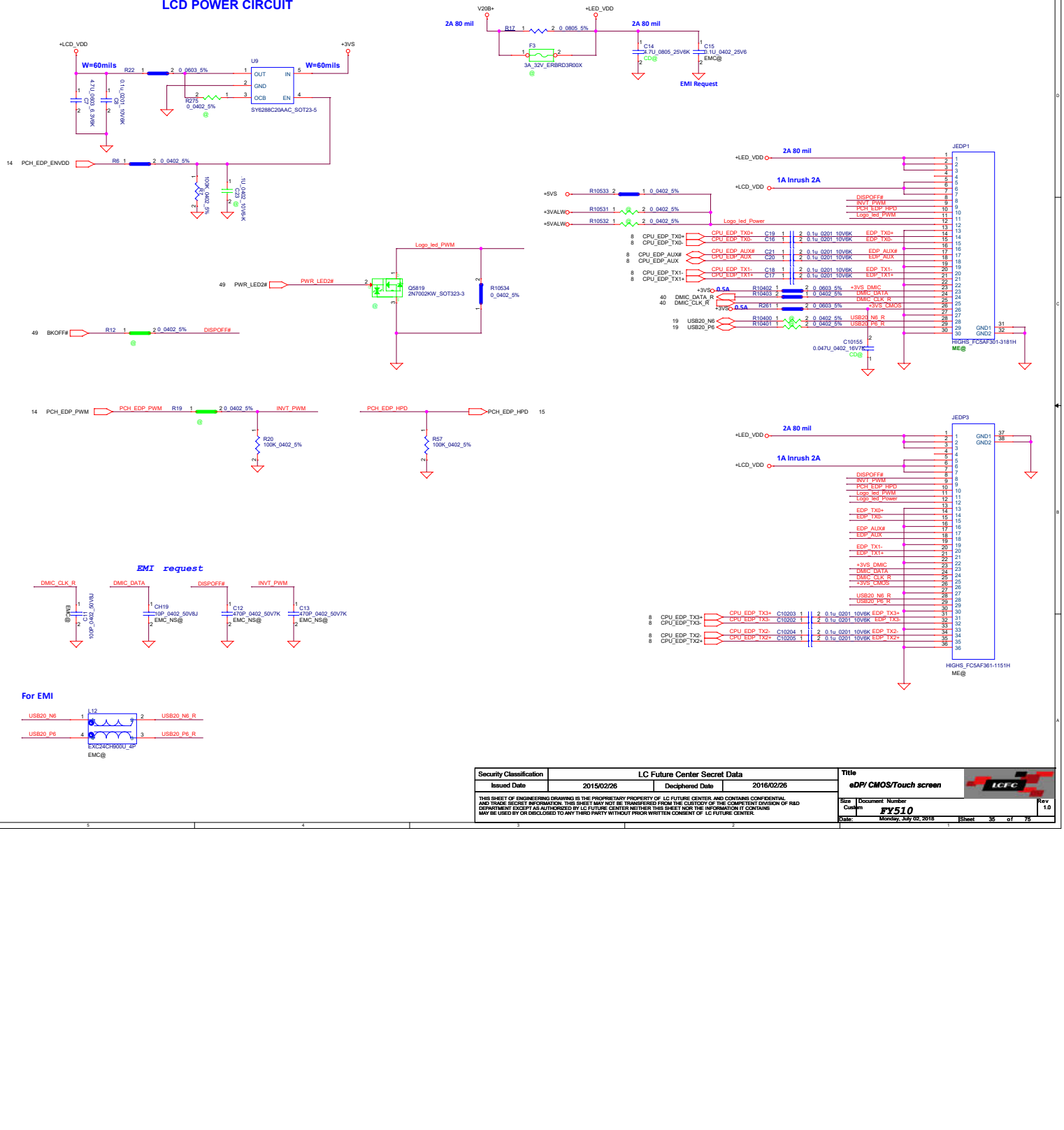
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: N16P-GX_VRAM C Lower

Size: D | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018

LCD POWER CIRCUIT

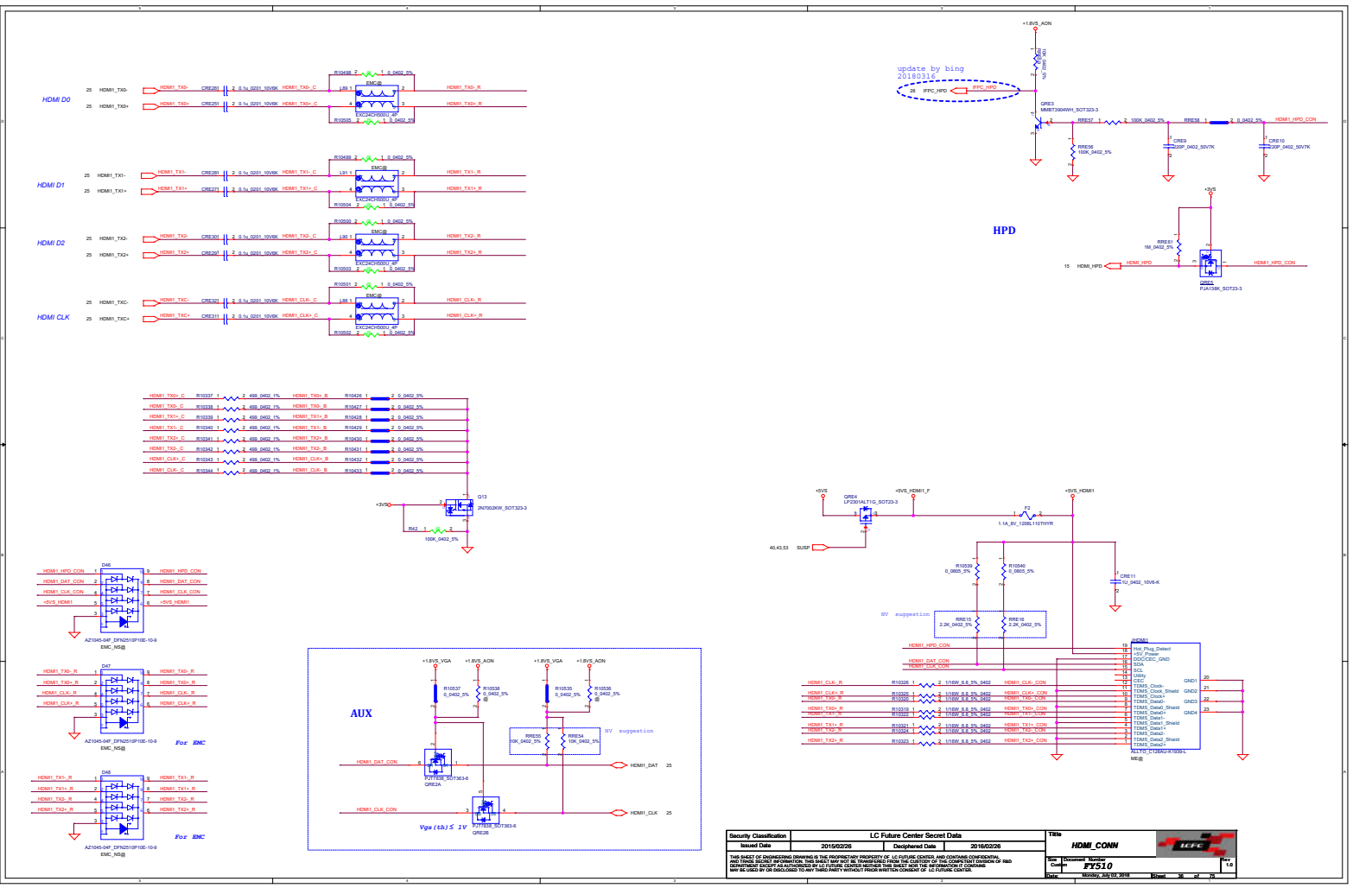


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: eDP/ CMOS/Touch screen

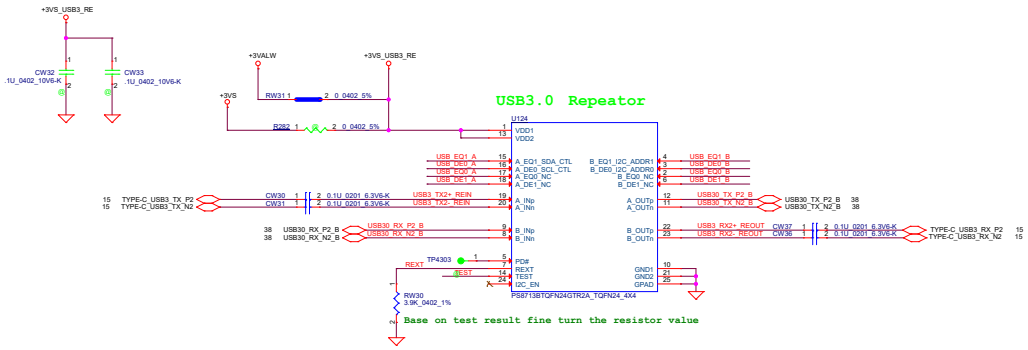
Size: Custom | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018 | Sheet 35 of 75



Security Classification	LC Future Center Secret Data		Title: HDMI_CONN
Issued Date: 2015/02/26	Deciphered Date: 2016/02/26		Size: Custom
			Document Number: FY510
			Rev: 1.0
			Date: Monday, July 02, 2018
			Sheet: 36 of 75

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL THE TRADE SECRET INFORMATION. THIS SHEET CAN NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

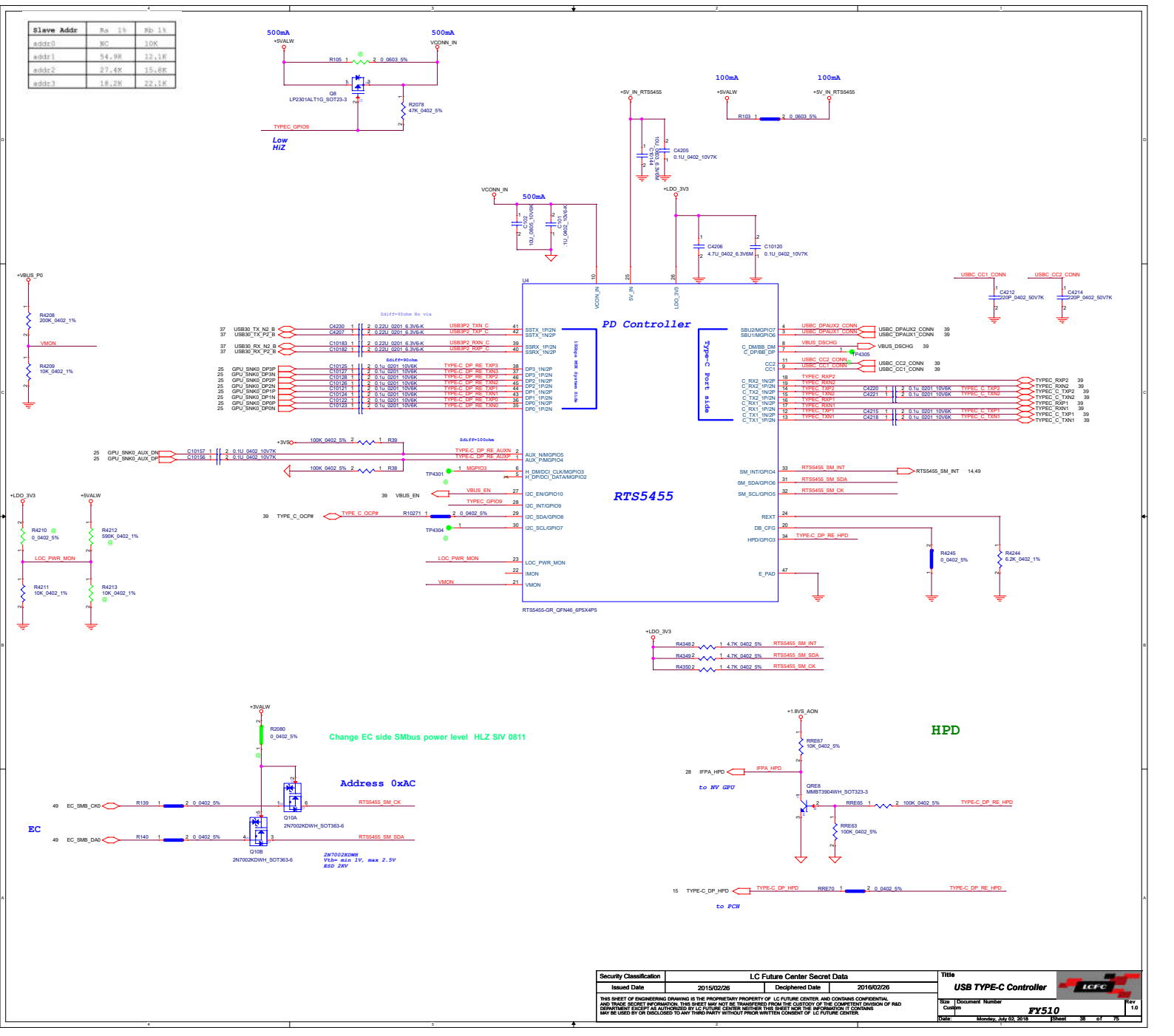


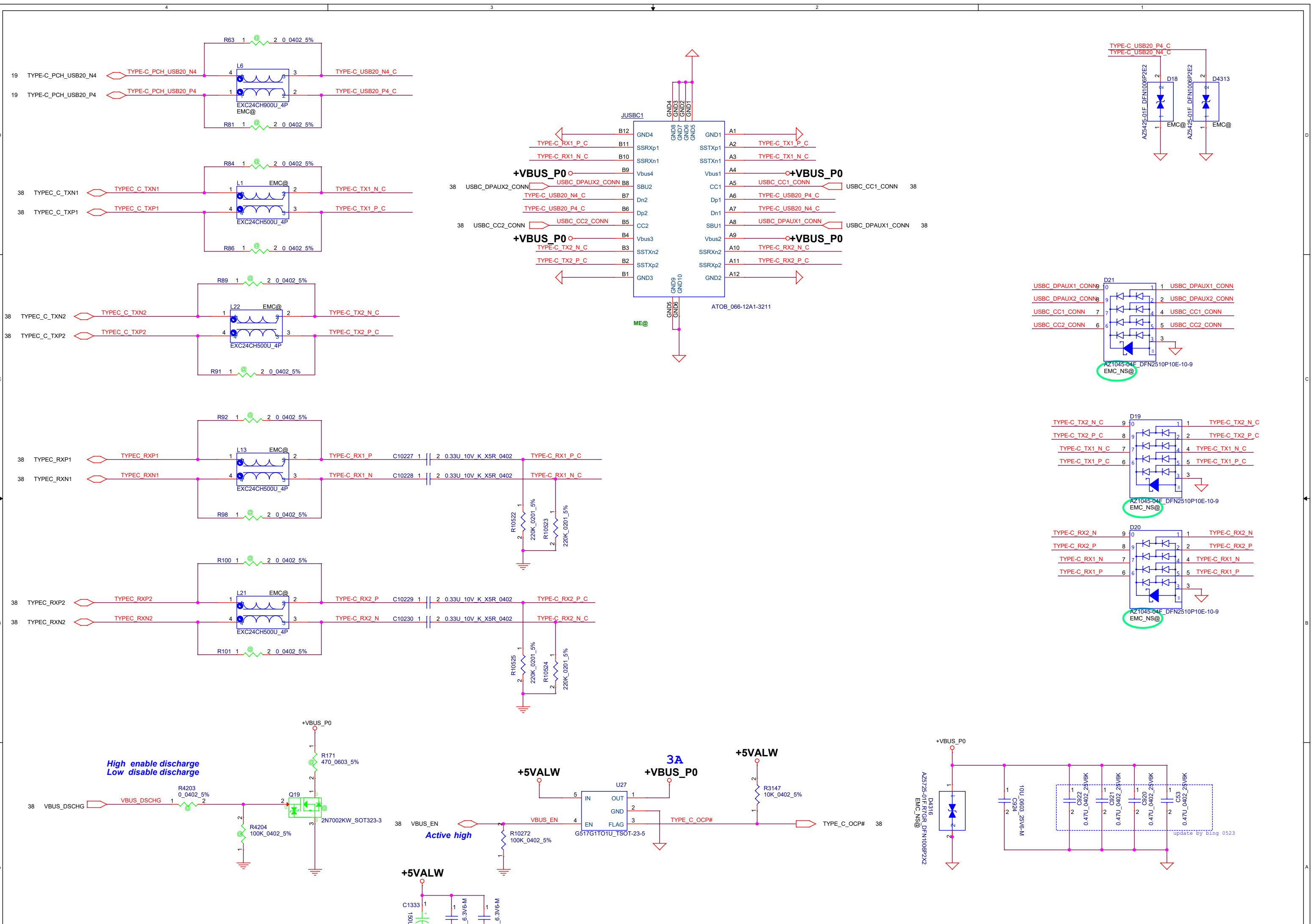
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: DDI Redriver PS8330

Size	Document Number	Rev
C	FY510	1.0

Date: Monday, July 02, 2018 Sheet 37 of 75

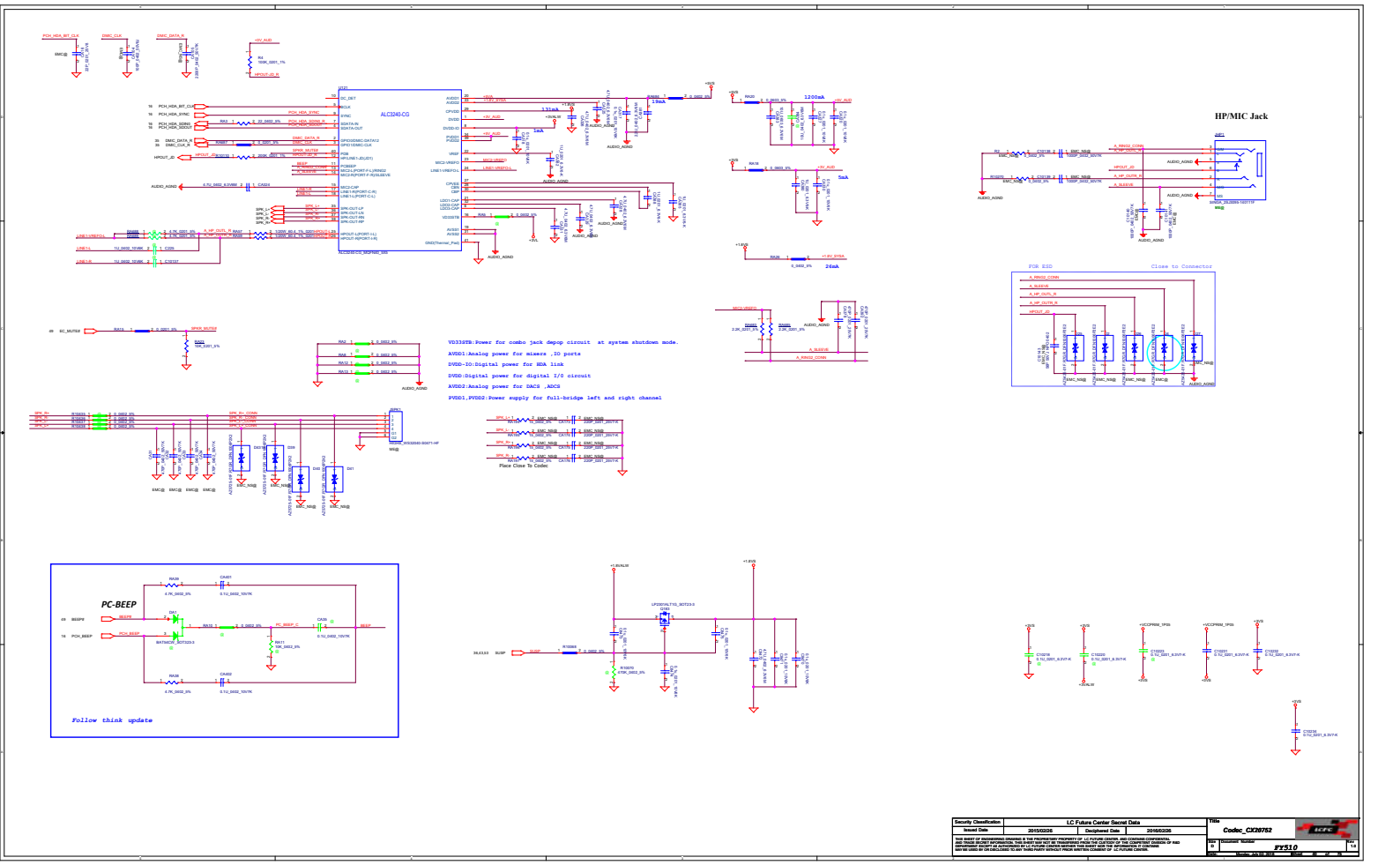

Slave Addr | Rs 1% | Rb 1%
addr0 | NC | 10K
addr1 | 54.9K | 12.1K
addr2 | 27.4K | 15.8K
addr3 | 18.2K | 22.1K
500mA
+5VALW
VCONN_IN
R105 0 0603 5%
Q8
LP2301ALT1G_SOT23-3
R2078
47K_0402_5%
TYPEC_GPIO9
Low
HiZ
+5V_IN_RTS5455
100mA
R103 0 0603 5%
C4205
0.1U_0402_10V7K
+LDO_3V3
C4206
4.7U_0402_6.3V6M
C10120
0.1U_0402_10V7K
C4102
10U_0805_10V6K
C4101
1U_0402_10V6K
+VBUS_P0
R4208
200K_0402_1%
VMON
R4209
10K_0402_1%
U4
PD Controller
RTS5455
RTS5455-GR_QFN46_6P5X4P5
Type-C Port side
USBC_CC1_CONN
USBC_CC2_CONN
C4212
220P_0402_50V7K
C4214
220P_0402_50V7K
USB30_TX_N2_B
USB30_TX_P2_B
USB30_RX_N2_B
USB30_RX_P2_B
C4230
C4207
C10183
C10182
USB3P2_TXN_C
USB3P2_TXP_C
USB3P2_RXN_C
USB3P2_RXP_C
SSTX_1P/2N
SSTX_1N/2P
SSRX_1P/2N
SSRX_1N/2P
SBU2/MGPIO7
SBU1/MGPIO6
USBC_DPAUX2_CONN
USBC_DPAUX1_CONN
VBUS_DSCHG
C_DM/BB_DM
C_DP/BB_DP
TP4305
CC2
CC1
USBC_CC2_CONN
USBC_CC1_CONN
GPU_SNK0_DP3P
GPU_SNK0_DP3N
GPU_SNK0_DP2P
GPU_SNK0_DP2N
GPU_SNK0_DP1P
GPU_SNK0_DP1N
GPU_SNK0_DP0P
GPU_SNK0_DP0N
C10125
C10127
C10128
C10126
C10121
C10124
C10122
C10123
TYPEC_DP_RE_TXP3
TYPEC_DP_RE_TXN3
TYPEC_DP_RE_TXP2
TYPEC_DP_RE_TXN2
TYPEC_DP_RE_TXP1
TYPEC_DP_RE_TXN1
TYPEC_DP_RE_TXP0
TYPEC_DP_RE_TXN0
DP3_1N/2P
DP3_1P/2N
DP2_1N/2P
DP2_1P/2N
DP1_1N/2P
DP1_1P/2N
DP0_1N/2P
DP0_1P/2N
C_RX2_1N/2P
C_RX2_1P/2N
C_TX2_1N/2P
C_TX2_1P/2N
C_RX1_1N/2P
C_RX1_1P/2N
C_TX1_1N/2P
C_TX1_1P/2N
TYPEC_RXP2
TYPEC_RXN2
TYPEC_TXP2
TYPEC_TXN2
TYPEC_RXP1
TYPEC_RXN1
TYPEC_TXP1
TYPEC_TXN1
C4220
C4221
C4215
C4218
TYPEC_C_RXP2
TYPEC_C_RXN2
TYPEC_C_TXP2
TYPEC_C_TXN2
TYPEC_C_RXP1
TYPEC_C_RXN1
TYPEC_C_TXP1
TYPEC_C_TXN1
GPU_SNK0_AUX_DN
GPU_SNK0_AUX_DP
C10157
C10156
TYPEC_DP_RE_AUXN
TYPEC_DP_RE_AUXP
AUX_N/MGPIO5
AUX_P/MGPIO4
+3VS
R39
R38
TP4301
MGPIO3
H_DM/DCI_CLK/MGPIO3
H_DP/DCI_DATA/MGPIO2
VBUS_EN
I2C_EN/GPIO10
TYPEC_GPIO9
I2C_INT/GPIO9
I2C_SDA/GPIO8
I2C_SCL/GPIO7
TYPE_C_OCP#
R10271
TP4304
LOC_PWR_MON
IMON
VMON
SM_INT/GPIO4
SM_SDA/GPIO6
SM_SCL/GPIO5
RTS5455_SM_INT
RTS5455_SM_SDA
RTS5455_SM_CK
14,49
REXT
DB_CFG
HPD/GPIO3
TYPE-C_DP_RE_HPD
E_PAD
R4245
0_0402_5%
R4244
6.2K_0402_1%
+LDO_3V3
+5VALW
R4210
0_0402_5%
R4212
590K_0402_1%
R4211
10K_0402_1%
R4213
10K_0402_1%
R43482
R43492
R43502
4.7K_0402_5%
+3VALW
R2080
0_0402_5%
Change EC side SMbus power level HLZ SIV 0811
Address 0xAC
EC
EC_SMB_CK0
EC_SMB_DA0
R139
R140
Q10A
Q10B
2N7002KDWH_SOT363-6
2N7002KDWH
Vth= min 1V, max 2.5V
ESD 2KV
+1.8VS_AON
RRE67
10K_0402_5%
IFPA_HPD
to NV GPU
QRE8
MMBT3904WH_SOT323-3
RRE65
100K_0402_5%
RRE63
100K_0402_5%
HPD
TYPE-C_DP_HPD
RRE70
to PCH
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
USB TYPE-C Controller
Size
Custom
Document Number
FY510
Rev
1.0
Date:
Monday, July 02, 2018
Sheet
38
of
75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **USB TYPE-C Port**

Size	Document Number	Rev
C	FY510	1.0



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	Codec_CX20752		
Size	Document Number		Rev
B	FY510		1.0
Date:	Thursday, July 09, 2015	Sheet	46 of 46

Security Classification	LC Future Center Secret Data		
Issued Date	2015/6/23	Deciphered Date	2015/6/23

Title

Audio Jack

Size	Document Number	Rev
C	FY510	1.0

Date: Monday, July 02, 2018 Sheet 41 of 75

TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

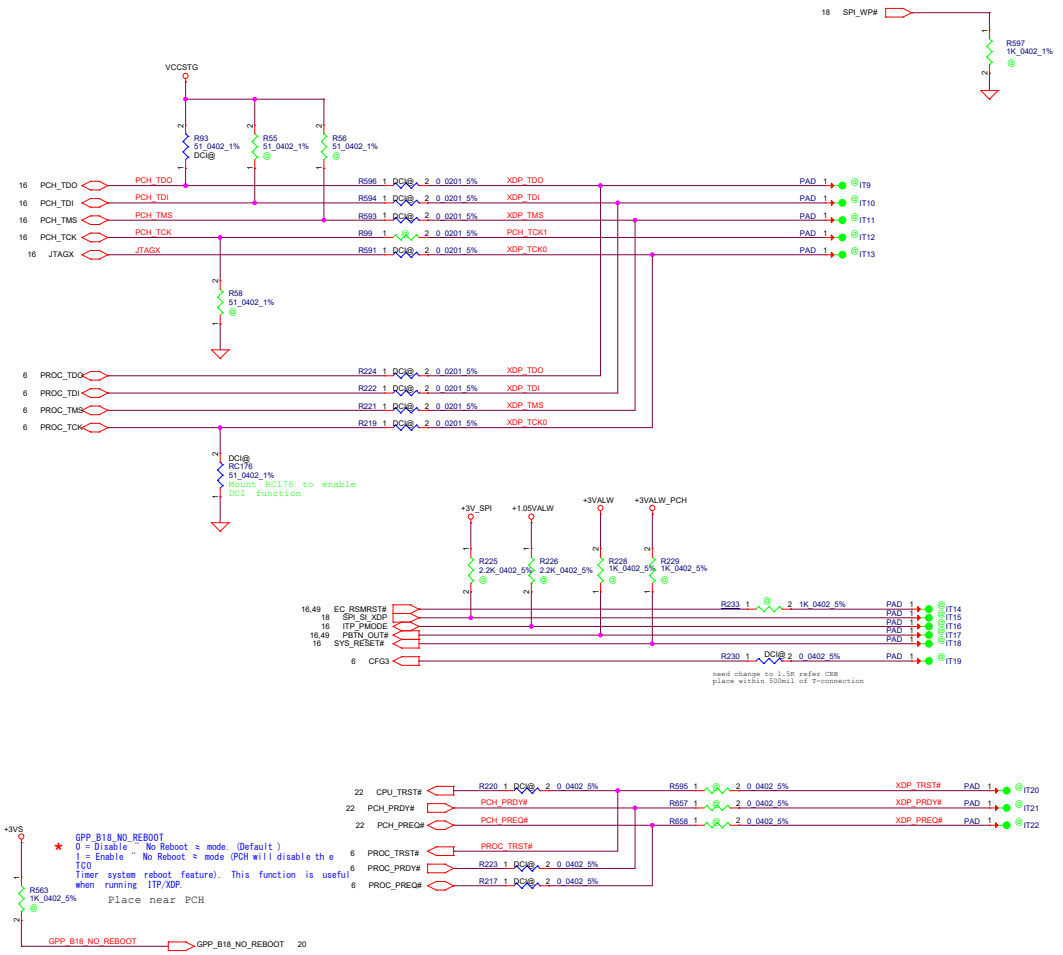
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

LOGIC

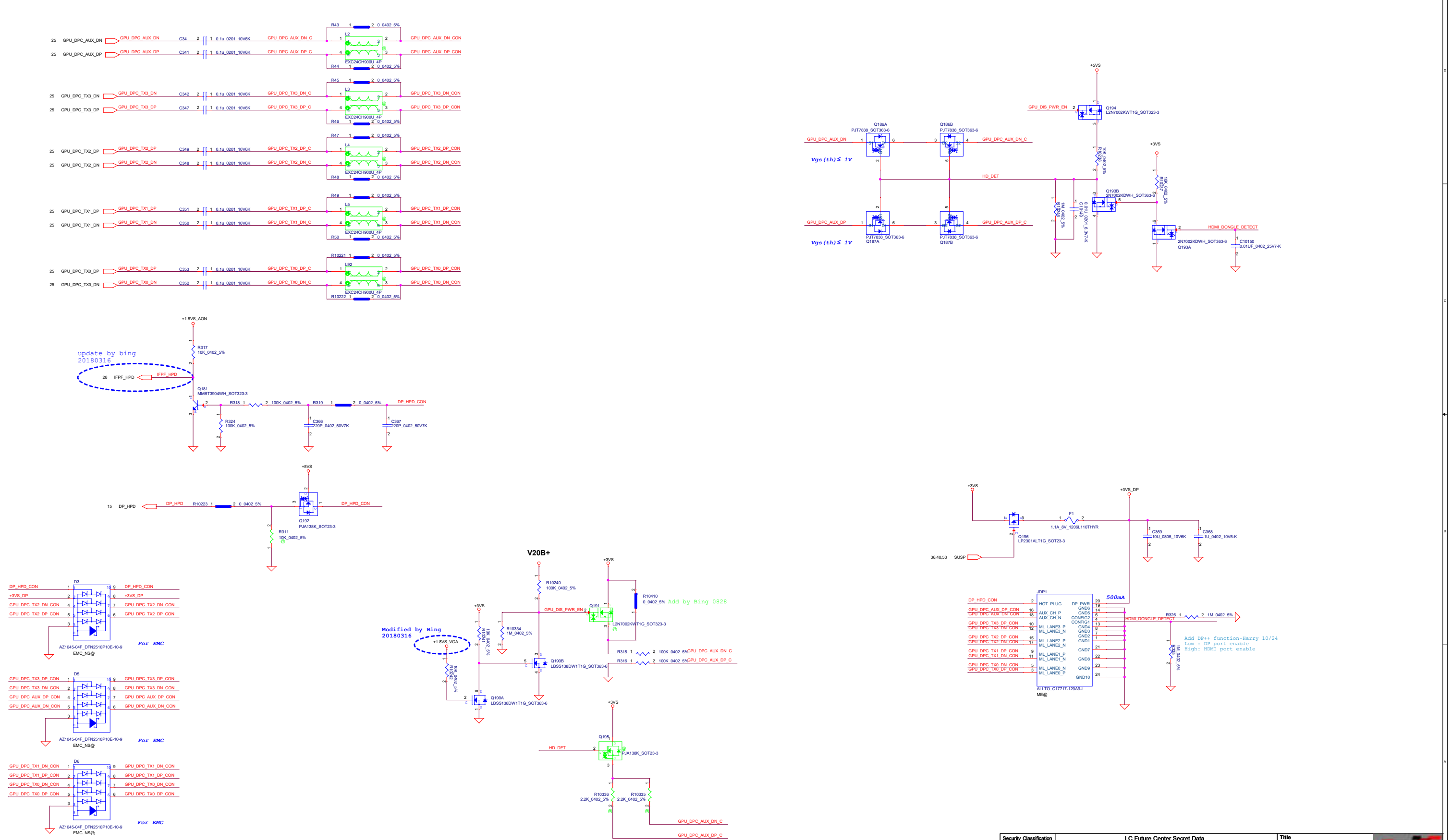


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: XDP

Size: Custom | Document Number: FY510 | Rev: 1.0

Date: Monday, July 02, 2018 | Sheet 42 of 75

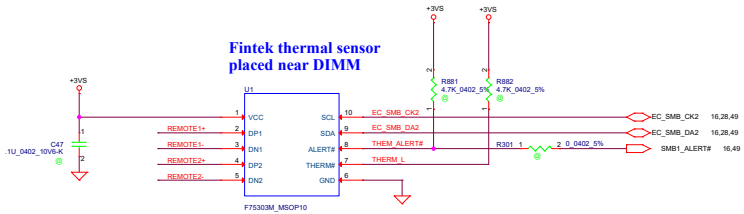


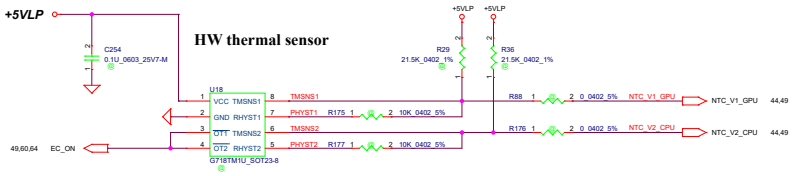
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2016/02/26

Title: DP

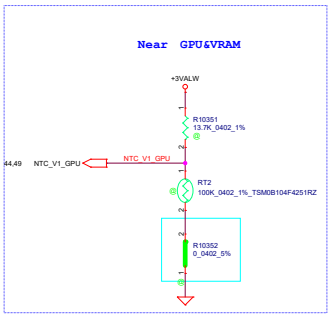
Size: D | Document Number: FY510 | Rev: 1.0

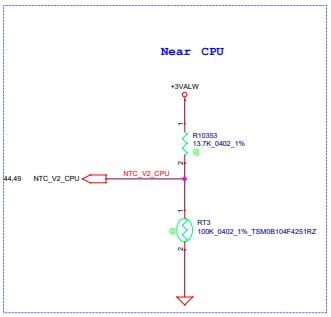
Date: Monday, July 02, 2018 |



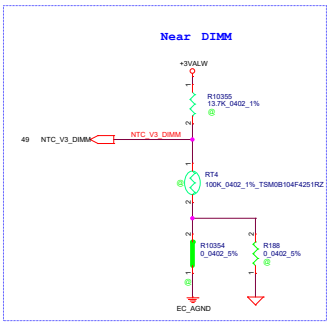


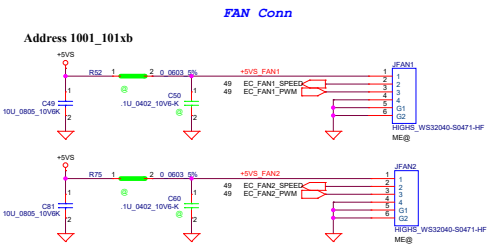
over temperature threshold:
RSET=3*RTMH
92+/-30C
Hysteresis temperature threshold.
RHYST=(RSET*RTML)/(3*RTML-RSET)
56+/-30C





for layout optimized, change the EC_AGND to GND



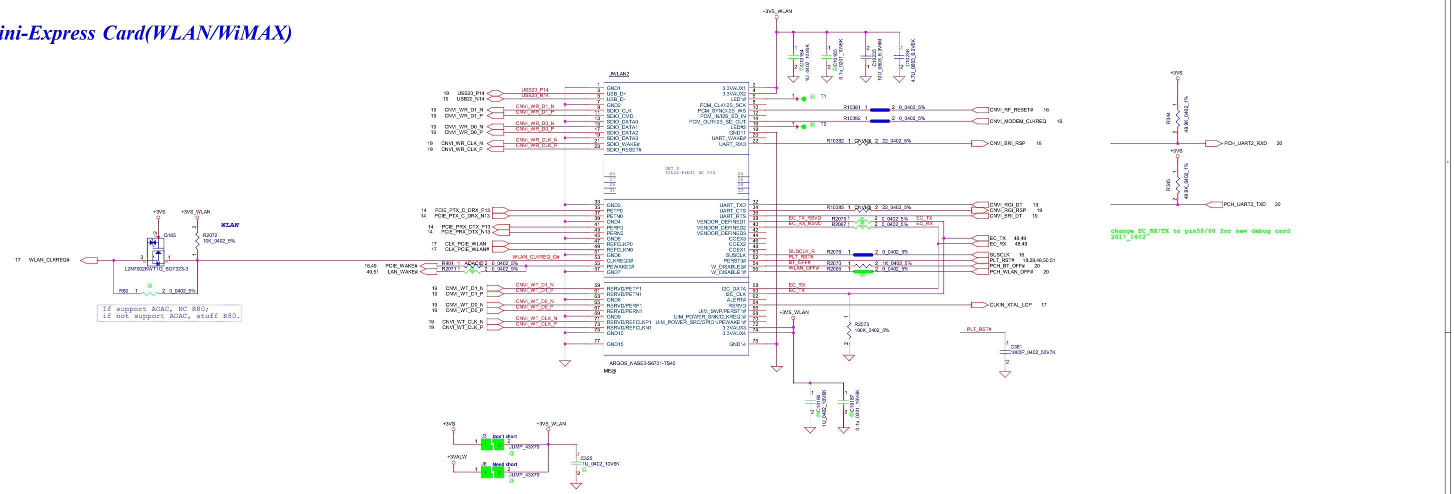


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

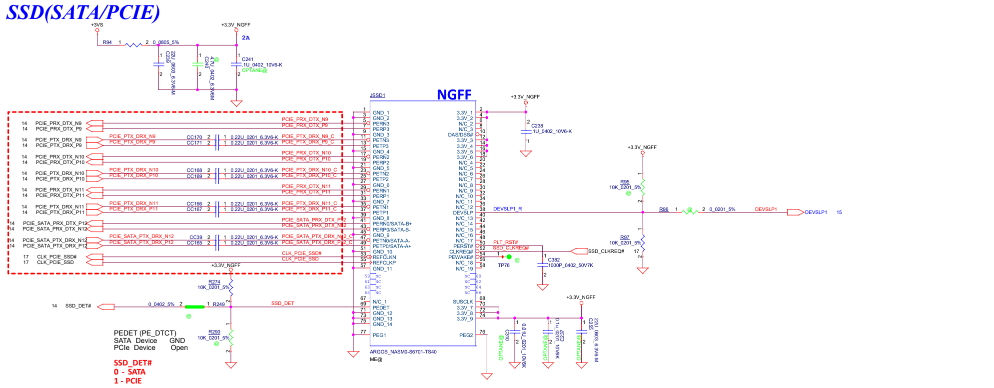
Title	Thermal sensor/FAN CONN		
Size	Document Number		Rev
Custom	FY510		1.0
Date:	Monday, July 02, 2018	Sheet	44 of 75

AMP/Volume Control

Mini-Express Card(WLAN/WiMAX)

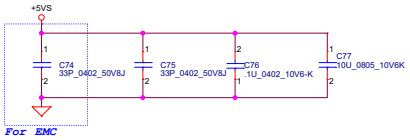


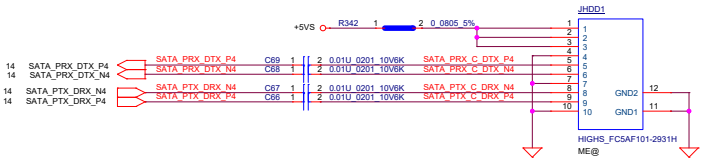
M.2 SSD(SATA/PCIE)



Security Classification	LC Future Center Secret Data			Title
Issued Date	2015/02/26	Deciphered Date	2016/02/26	NGFF WLAN
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size: Custom; Document Number: FY510; Rev: 1.0; Date: Monday, July 02, 2018; Sheet 45 of 75

SATA HDD Conn.



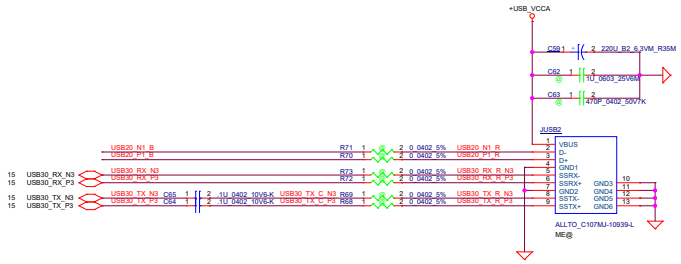


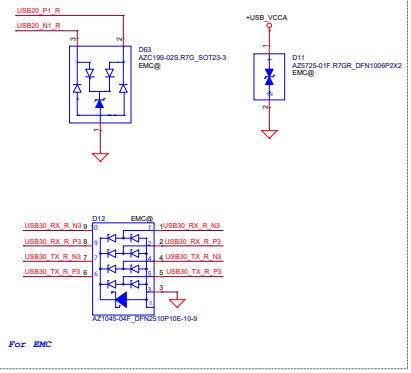
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

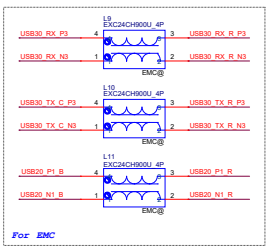
Title: **HDD/XBOX CONN**

Size	Document Number	Rev
Custom	FY510	1.0

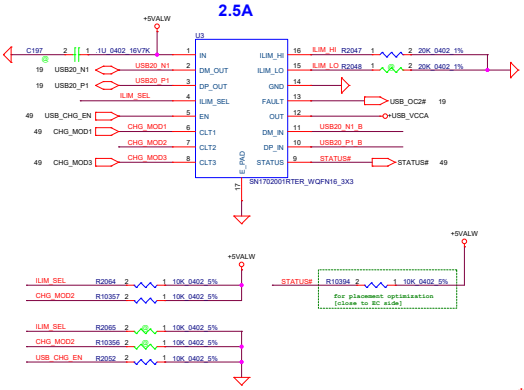
Date: Monday, July 02, 2018 Sheet 46 of 75







USB charger
2.5A



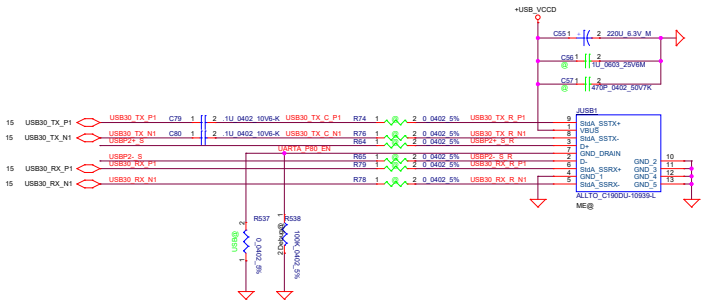
CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT hold low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: USB2.0/USB3.0 PORT (LEFT)

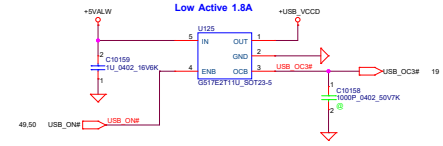
Size	Document Number	Rev
C	FY510	1.0

Date: Monday, July 02, 2018 Sheet 47 of 75

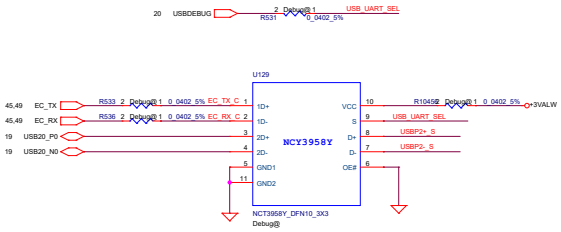


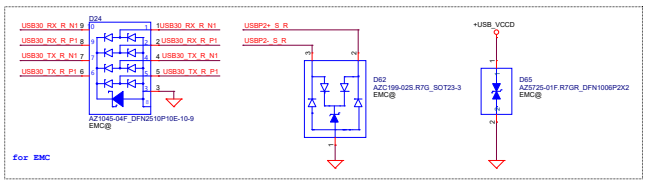
USB3.1 PORT x1

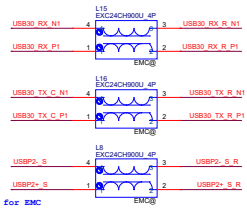
Low Active 1.8A



For USB Debug Function



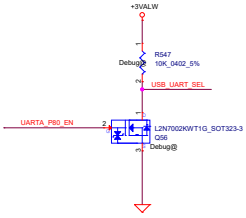




USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

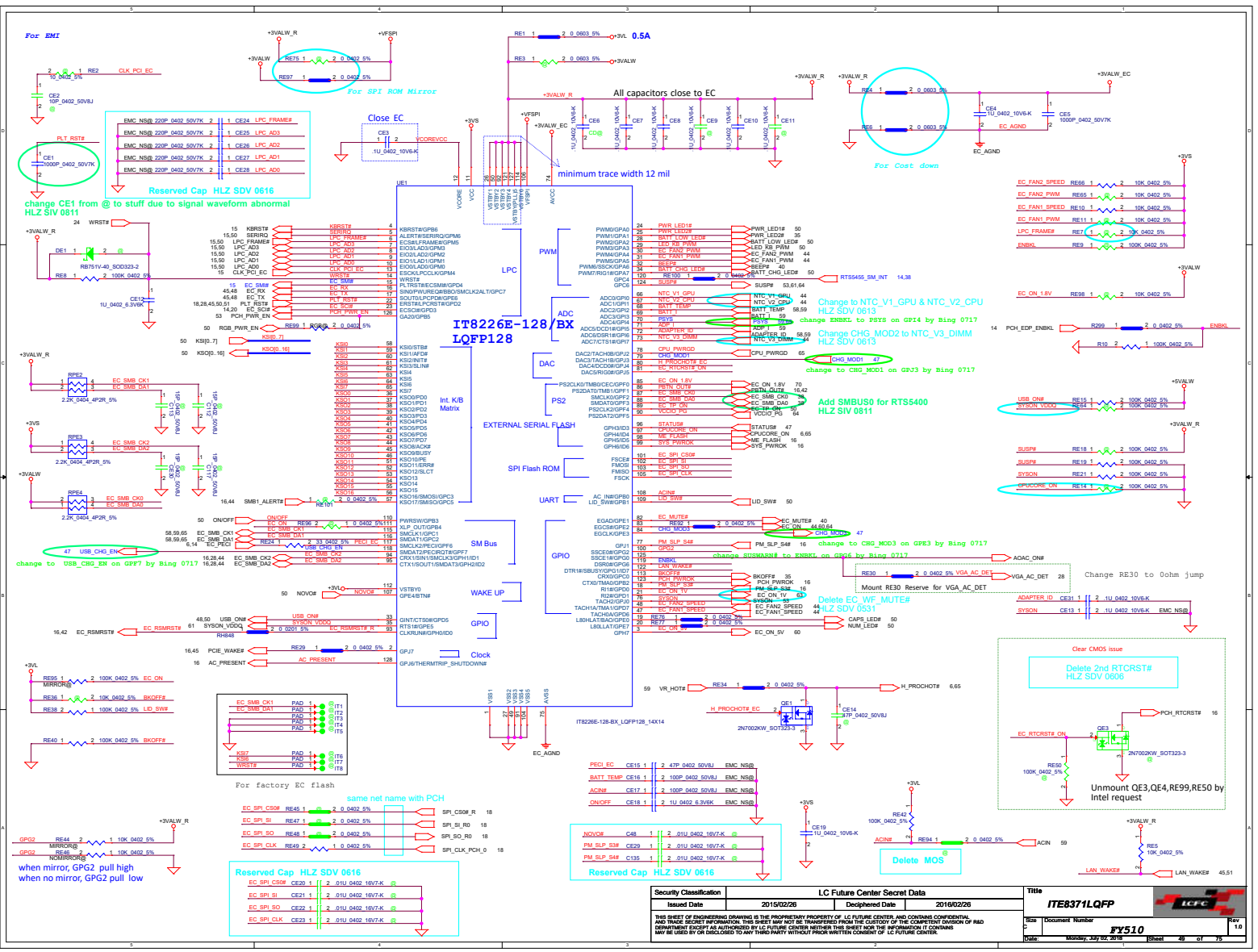


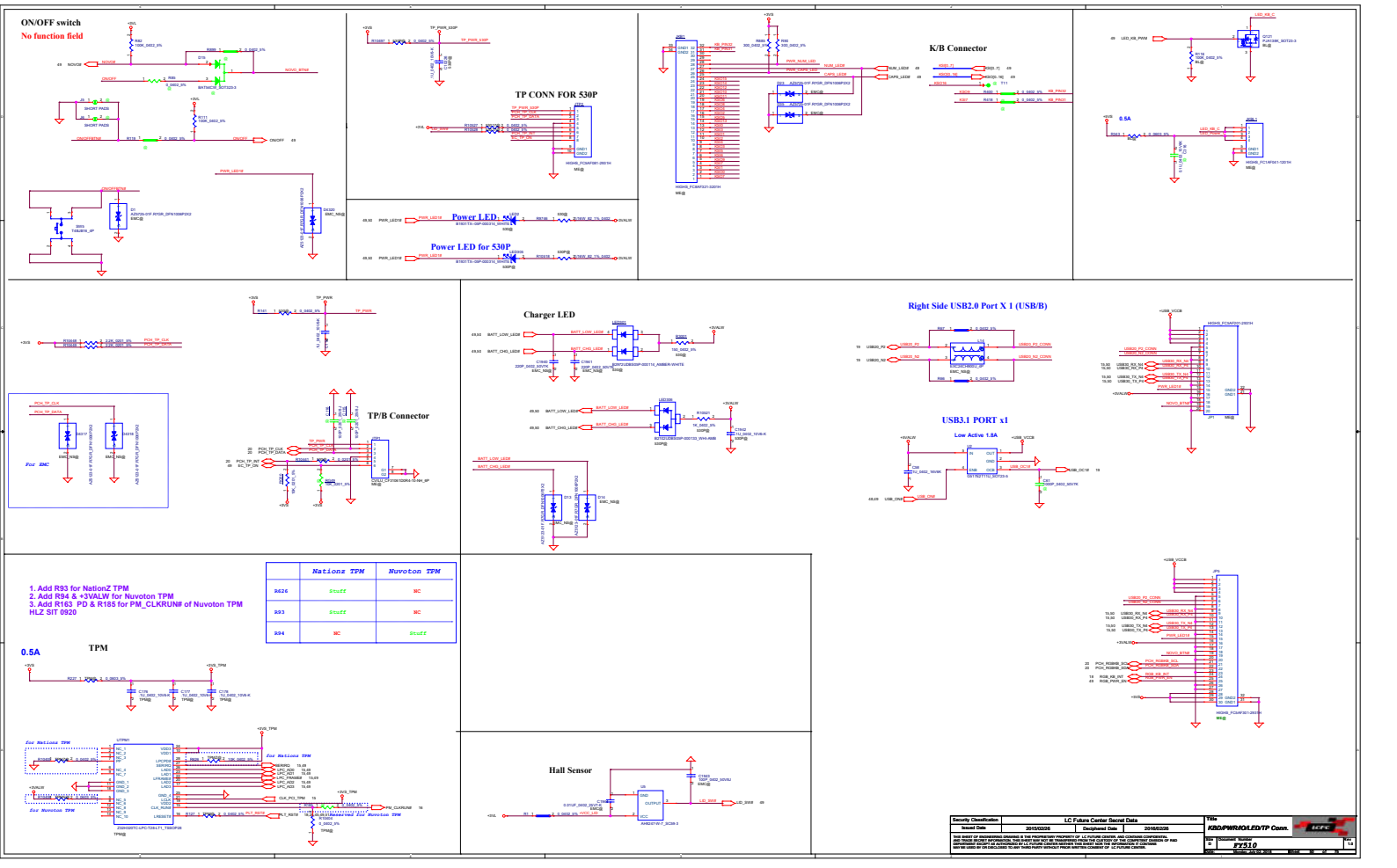
Security Classification	LC Future Center Secret Data		
Issued Date	2015/6/23	Deciphered Date	2015/6/23

Title: **USB2.0**

Size	Document Number	Rev
C	FY510	1.0

Date: Monday, July 02, 2018 Sheet 48 of 75

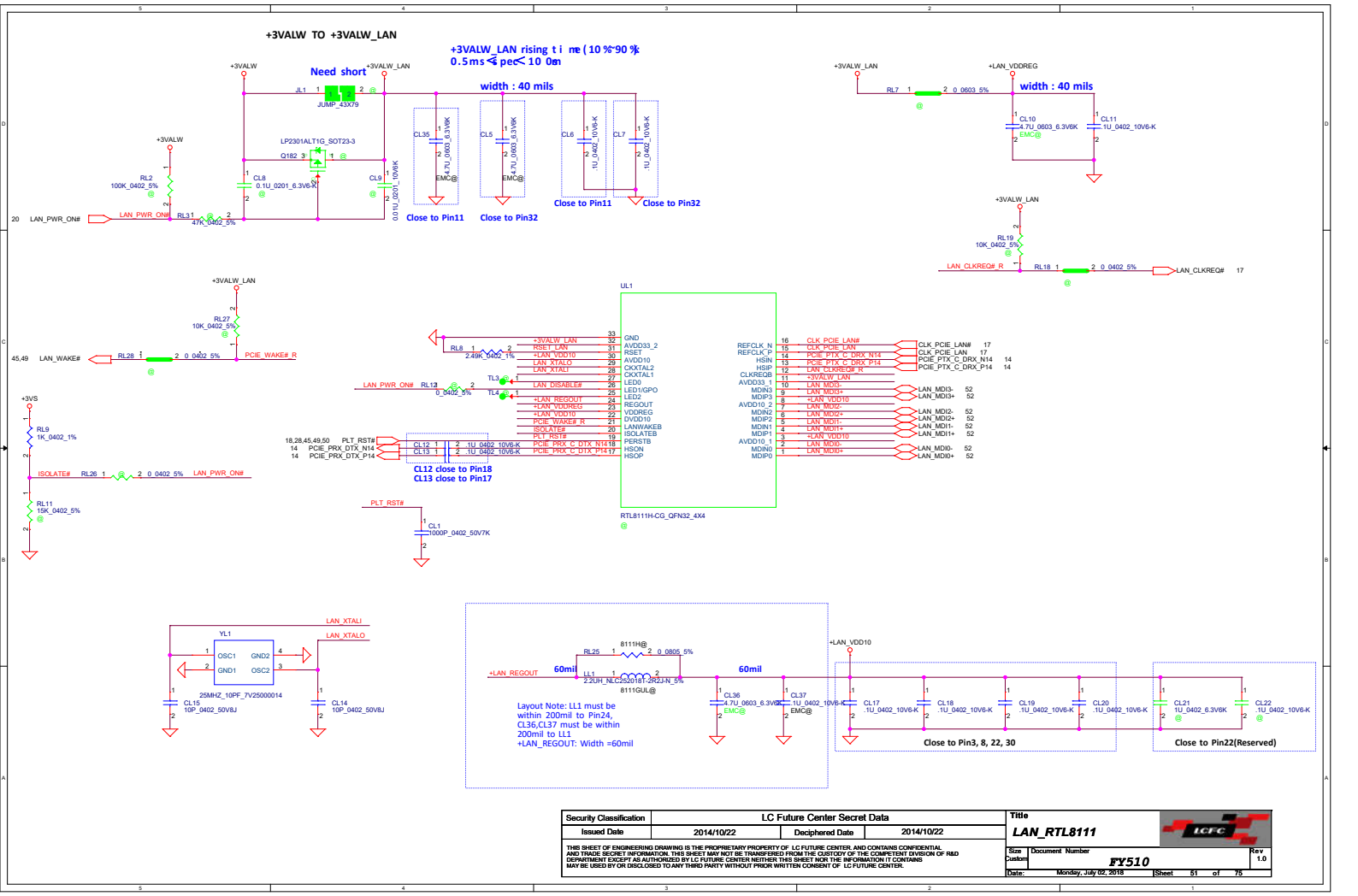

For EMI
IT8226E-128/BX
LQFP128
LPC
PWM
ADC
DAC
PS2
Int. K/B Matrix
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
GPIO
WAKE UP
Clock
Close EC
minimum trace width 12 mil
All capacitors close to EC
For SPI ROM Mirror
For Cost down
Reserved Cap HLZ SDV 0616
change CE1 from @ to stuff due to signal waveform abnormal
HLZ SIV 0811
Change to NTC_V1_GPU & NTC_V2_CPU
HLZ SDV 0613
change ENBKL to PSYS on GPI4 by Bing 0717
Change CHG_MOD2 to NTC_V3_DIMM
HLZ SDV 0613
change to CHG_MOD1 on GPJ3 by Bing 0717
Add SMBUS0 for RTS5400
HLZ SIV 0811
change to CHG_MOD3 on GPE3 by Bing 0717
change SUSWARN# to ENBKL on GPC6 by Bing 0717
change to USB_CHG_EN on GPF7 by Bing 0717
Change RE30 to 0ohm jump
Mount RE30 Reserve for VGA_AC_DET
Delete EC_WF_MUTE#
HLZ SDV 0531
Delete MOS
Clear CMOS issue
Delete 2nd RTCRST#
HLZ SDV 0606
Unmount QE3,QE4,RE99,RE50 by Intel request
same net name with PCH
For factory EC flash
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Reserved Cap HLZ SDV 0616
Reserved Cap HLZ SDV 0616
IT8226E-128-BX_LQFP128_14X14
Security Classification
LC Future Center Secret Data
Issued Date
2015/02/26
Deciphered Date
2016/02/26
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
ITE8371LQFP
Size
C
Document Number
FY510
Rev
1.0
Date:
Monday, July 02, 2018
Sheet
49
of
75



Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	KB/D/PWR/O/LED/TP Conn.	
Size	Document Number	Rev
B	FX510	1.0
Date: Sunday, July 26, 2015	Sheet 38 of 46	



Security Classification	LC Future Center Secret Data		
Issued Date	2014/10/22	Deciphered Date	2014/10/22

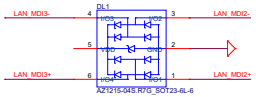
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

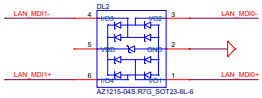
Title: LAN_RTL8111

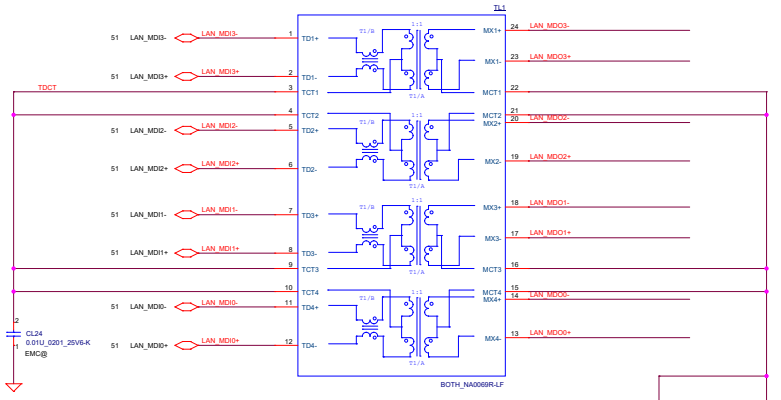
Size	Document Number	Rev
Custom	FY510	1.0

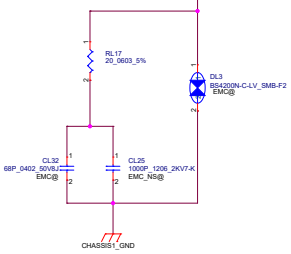
Date: Monday, July 02, 2018 Sheet 51 of 75

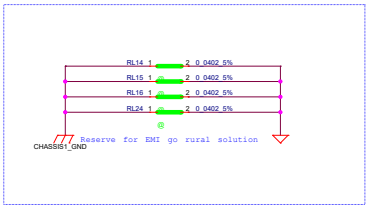
DL1/DL2
1'S PN:SC300005900
Place Close to TL1

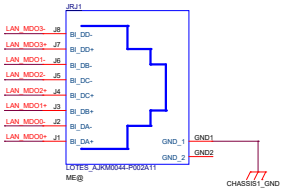










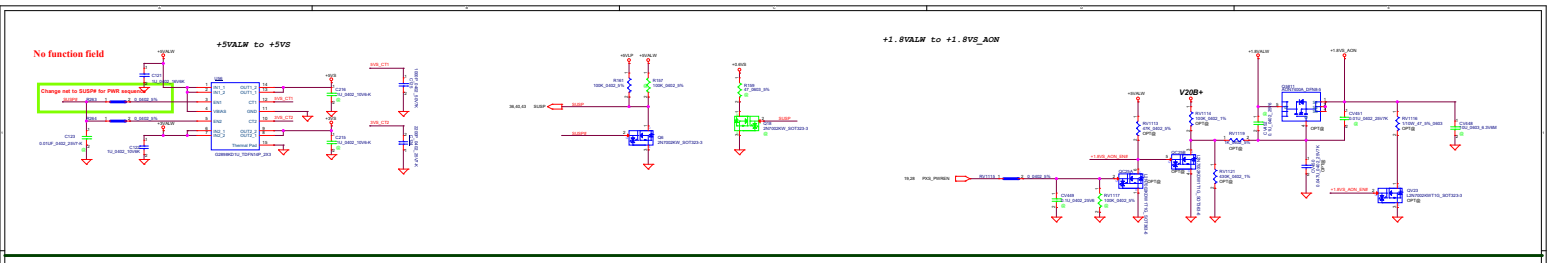


Security Classification	LC Future Center Secret Data		
Issued Date	2014/10/22	Deciphered Date	2014/10/22

Title: **LAN_Transformer**

Size	Document Number	Rev
C	FY510	1.0

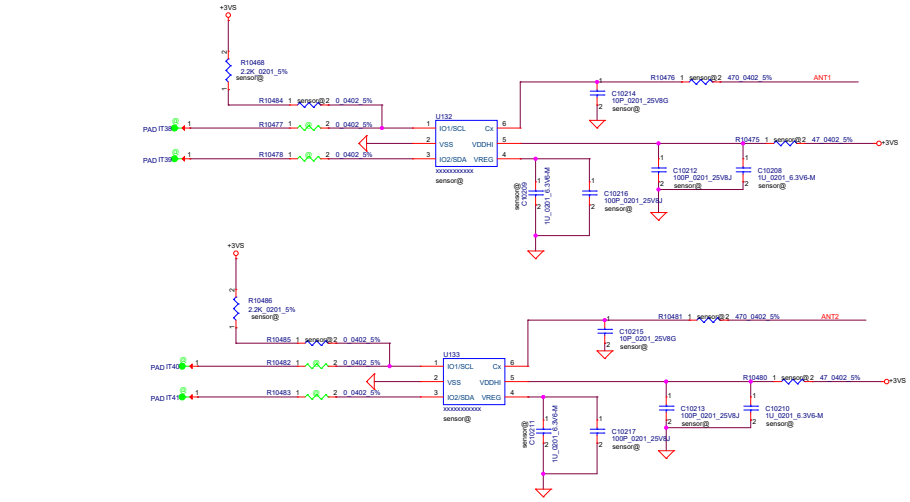
Date: Monday, July 02, 2018 Sheet 52 of 75

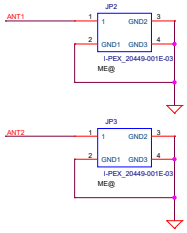


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPANY OR REVISED BY ANY DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	DC V TO VS INTERFACE		
Size	Document Number		Rev
B	FX510		1.0
Date:	Sunday, July 19, 2015	Sheet	38 of 46





Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *Virtual symbol*

Size	Document Number	Rev
C	FY510	1.0

Date: Monday, July 02, 2018 Sheet 54 of 75

PCB MB

ZZZ2 60HZ@

PCB FY510 NM-B961 NS-B961/B962/B963
DAZ1AM00100

HDMI Logo

ZZZ1 HDMI@

HDMI Logo
RC000000H0J

PCB MB

ZZZ10 144HZ@

PCB FY510 NM-B962 NS-B961/B962/B963
DAZ1AM00200

CPU

UC1 i5@

S IC CL80684033735 22 SR3ZD U0 2.3G 12
SA000093110

UC1 i7@

S IC CL80684033595 24 SR3YY U0 2.2G 12
SA000093010

PCH

UH1

S IC FH82HM370 SR40B B0 BGA 874P PCH 12
SA00009AG00

LAN

UL1 8111H@

S IC RTL8111H-CG QFN 32P CONTROLLER
SA000074W00

strap2	strap1	strap0

Hynix 6GB VRAM

ZZZ3 H6GX6@

HYNIX_6GB_VRAM
X7645M12008

UV4 H6G@	UV5 H6G@	UV6 H6G@	UV7 H6G@	UV8 H6G@	UV9 H6G@
H5GQ8H24MJR-R4C 8Gb SA00007ZQ00	H5GQ8H24MJR-R4C 8Gb SA00007ZQ00	H5GQ8H24MJR-R4C 8Gb SA00007ZQ00	H5GQ8H24MJR-R4C 8Gb SA00007ZQ00	H5GQ8H24MJR-R4C 8Gb SA00007ZQ00	H5GQ8H24MJR-R4C 8Gb SA00007ZQ00

256Mx32

RV315 H6G@	RV312 H6G@	RV313 H6G@	PR1812 H6G@
100K 0402 1% SD034100380	100K 0402 1% SD034100380	100K 0402 1% SD034100380	66.5K +-1% 0402 SD03466528J

010

Samsung 6GB VRAM

ZZZ4 S6GX6@

SAMSUNG_6GB_VRAM
X7645M12009

UV4 S6G@	UV5 S6G@	UV6 S6G@	UV7 S6G@	UV8 S6G@	UV9 S6G@
K4G80325FB-HC25 8Gb SA00007Z700	K4G80325FB-HC25 8Gb SA00007Z700	K4G80325FB-HC25 8Gb SA00007Z700	K4G80325FB-HC25 8Gb SA00007Z700	K4G80325FB-HC25 8Gb SA00007Z700	K4G80325FB-HC25 8Gb SA00007Z700

256Mx32

RV315 S6G@	RV309 S6G@	RV313 S6G@	PR1812 S6G@
100K 0402 1% SD034100380	100K 0402 1% SD034100380	100K 0402 1% SD034100380	66.5K +-1% 0402 SD03466528J

000

Micron 6GB VRAM

ZZZ5 M6GX6@

MICRON_6GB_VRAM
X7645M1200A

UV4 M6G@	UV5 M6G@	UV6 M6G@	UV7 M6G@	UV8 M6G@	UV9 M6G@
MT51J256M32HF-80:A 8Gb SA00007Z900	MT51J256M32HF-80:A 8Gb SA00007Z900	MT51J256M32HF-80:A 8Gb SA00007Z900	MT51J256M32HF-80:A 8Gb SA00007Z900	MT51J256M32HF-80:A 8Gb SA00007Z900	MT51J256M32HF-80:A 8Gb SA00007Z900

256Mx32

RV315 M6G@	RV309 M6G@	RV314 M6G@	PR1812 M6G@
100K 0402 1% SD034100380	100K 0402 1% SD034100380	100K 0402 1% SD034100380	82.5K +-1% 0402 SD00002078J

001

Micron 6GB VRAM (NEW)

ZZZ6 M6GX6N@

MICRON_6GB_VRAM
X7645M1200C

UV4 M6G@	UV5 M6G@	UV6 M6G@	UV7 M6G@	UV8 M6G@	UV9 M6G@
MT51J256M32HF-80:B 8Gb SA00007Z930	MT51J256M32HF-80:B 8Gb SA00007Z930	MT51J256M32HF-80:B 8Gb SA00007Z930	MT51J256M32HF-80:B 8Gb SA00007Z930	MT51J256M32HF-80:B 8Gb SA00007Z930	MT51J256M32HF-80:B 8Gb SA00007Z930

128Mx32

RV316 M6G@	RV309 M6G@	RV313 M6G@	PR1812 M6G@
100K 0402 1% SD034100380	100K 0402 1% SD034100380	100K 0402 1% SD034100380	82.5K +-1% 0402 SD00002078J

100

Hynix 6GB VRAM (NEW)

ZZZ7 H6GX6N@

HYNIX_6GB_VRAM
X7645M1200B

UV4 H6G@	UV5 H6G@	UV6 H6G@	UV7 H6G@	UV8 H6G@	UV9 H6G@
H5GC8H24AJR-R2C 8Gb SA00009FV00	H5GC8H24AJR-R2C 8Gb SA00009FV00	H5GC8H24AJR-R2C 8Gb SA00009FV00	H5GC8H24AJR-R2C 8Gb SA00009FV00	H5GC8H24AJR-R2C 8Gb SA00009FV00	H5GC8H24AJR-R2C 8Gb SA00009FV00

128Mx32

RV316 H6G@	RV309 H6G@	RV314 H6G@	PR1812 H6G@
100K 0402 1% SD034100380	100K 0402 1% SD034100380	100K 0402 1% SD034100380	82.5K +-1% 0402 SD00002078J

101

GPU

U117

S IC N17E-G1-A1 BGA 2152 GPU
SA000084900

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: *Virtual symbol*

Size	Document Number	Rev
C	FY510	0.1

Date: Monday, July 02, 2018 Sheet 55 of 74

PU2901

MP2949AGQKT-014D-Z
I7@
SA00008XG00

PU2901

MP2949AGQKT-014F-Z
I5@
SA00009810O

MPS2949 I5&I7

PR2944

S RES 1/16W 28.7K +-1% 0402
I7@
SD00001MM00

PR2944

S RES 1/16W 43.2K +-1% 0402
I5@
SD00001KR00

CPU I5&I7

PR2949

S RES 1/16W 392 +-1% 0402
I7@
SD00001KE00

PR2949

S RES 1/16W 100 +-1% 0402
I5@
SD03410008J

CPU I5&I7

Power MOS

ZZZ8

1060 CPU MOS
X7645M12001

Power MOS

ZZZ9

1060 MOS
X7645M12003

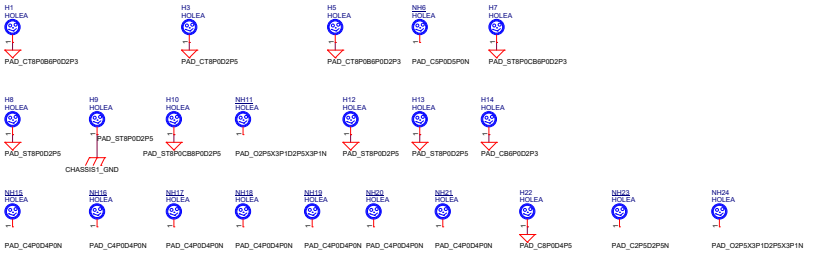
Check MP2949 LCFC PN
SA00008XG00 is Y530 (014D) for H62(I7)
SA00009810O (014F) for H42 (I5)

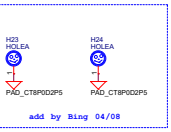
Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

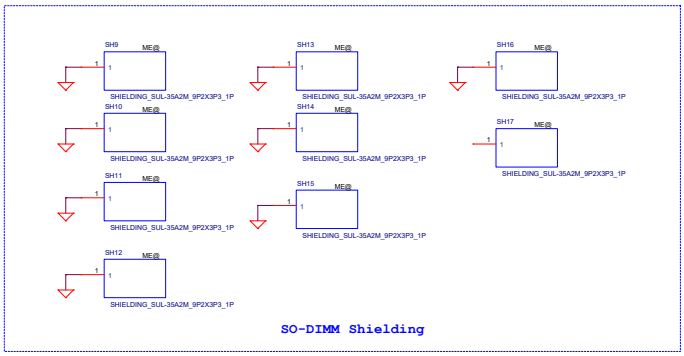
Title: *Virtual symbol*

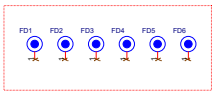
Size	Document Number	Rev
C	*FY510*	1.0

Date: Monday, July 02, 2018 Sheet 55 of 74



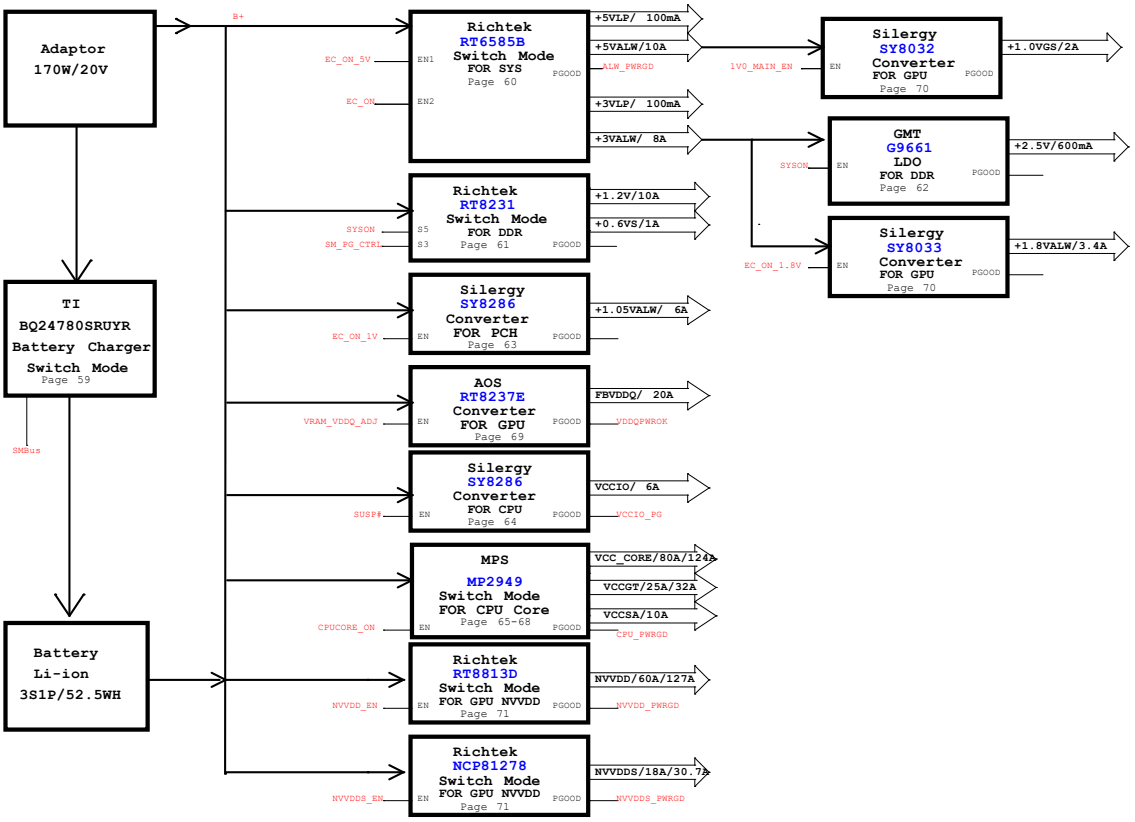






Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title	Blank		
Size	Document Number		Rev
C	FY510		1.0
Date:	Monday, July 02, 2018	Sheet	56 of 75

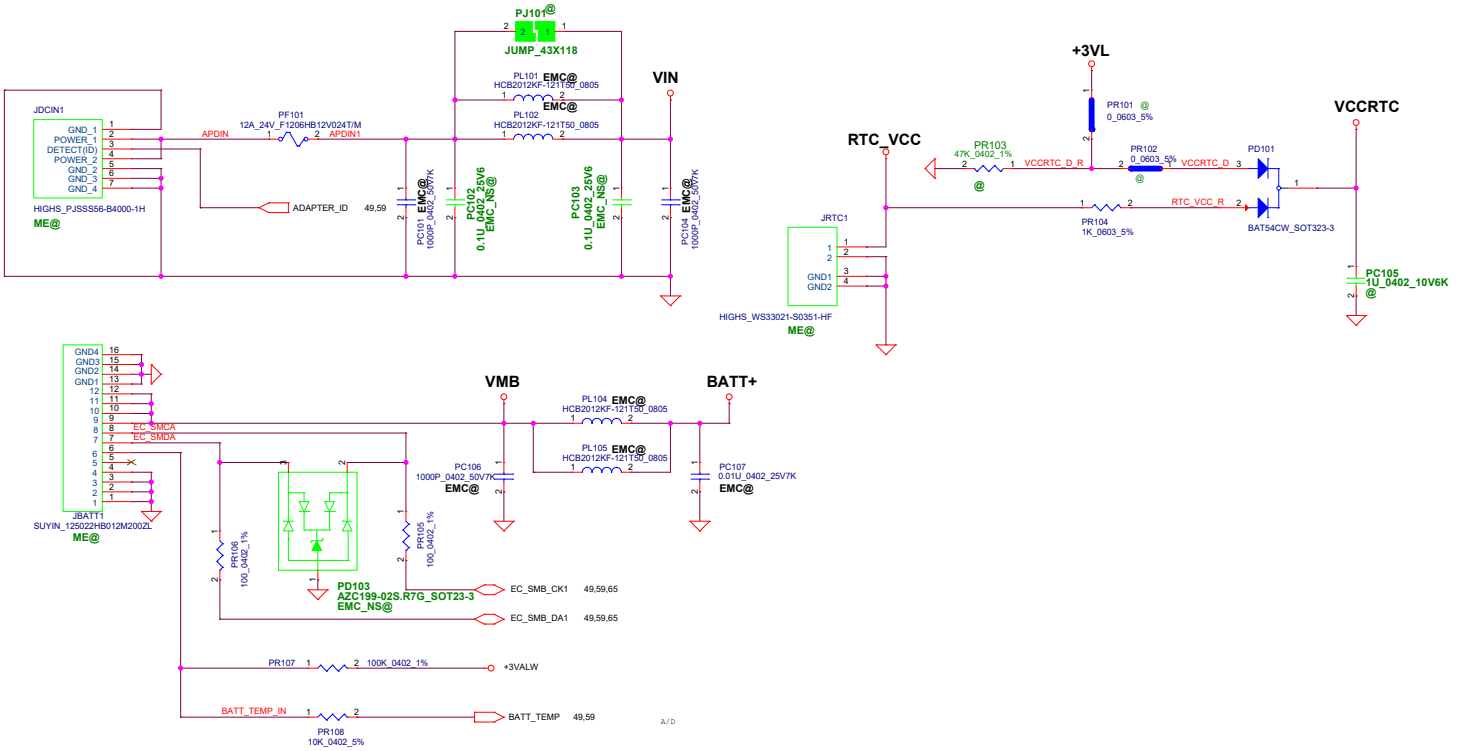


Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2016/02/26

Title: **Power Diagram**

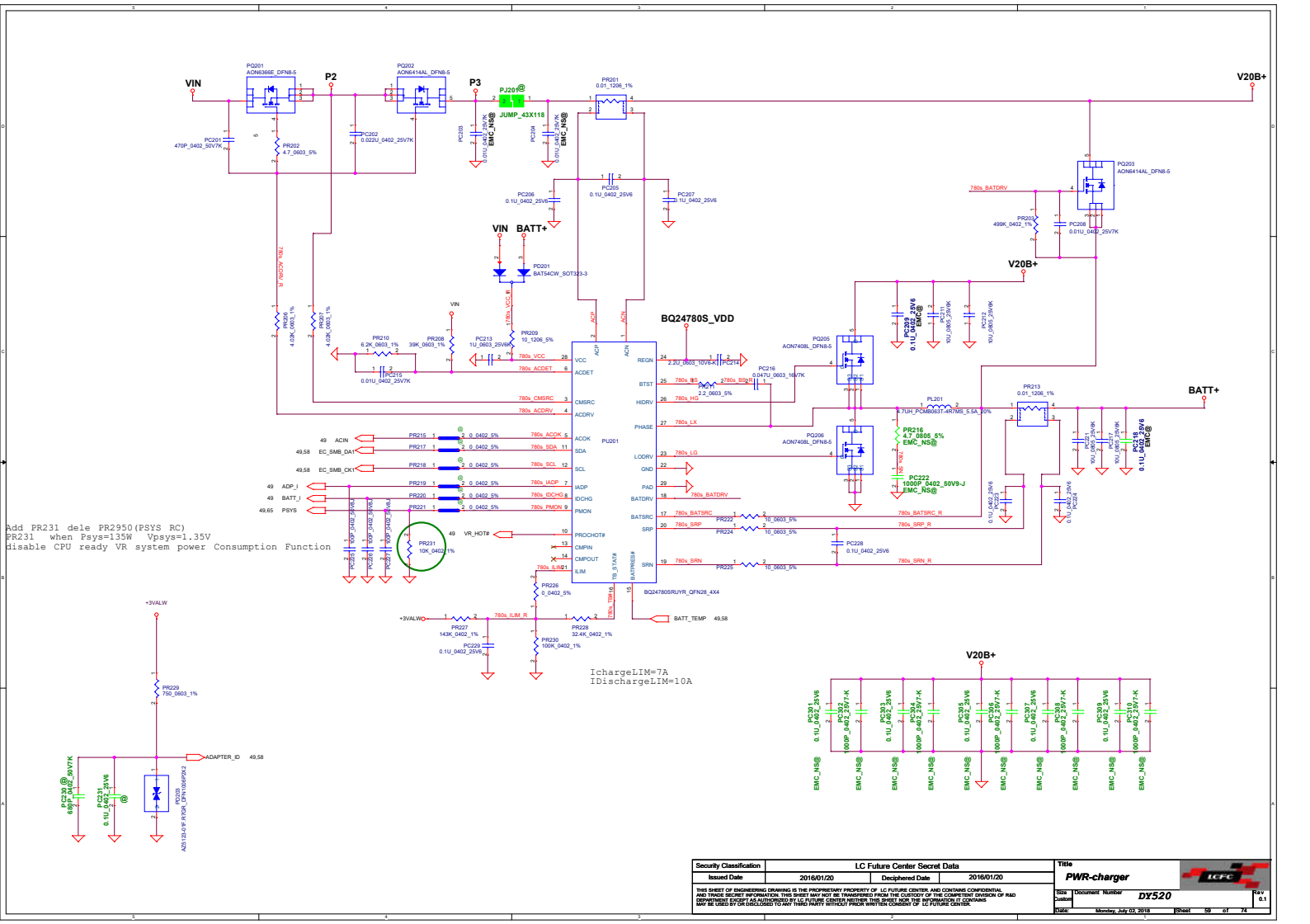
Size	Document Number	Rev
Custom	DZ510/DY512	1.0

Date: Monday, July 04, 2016 Sheet 57 of 74



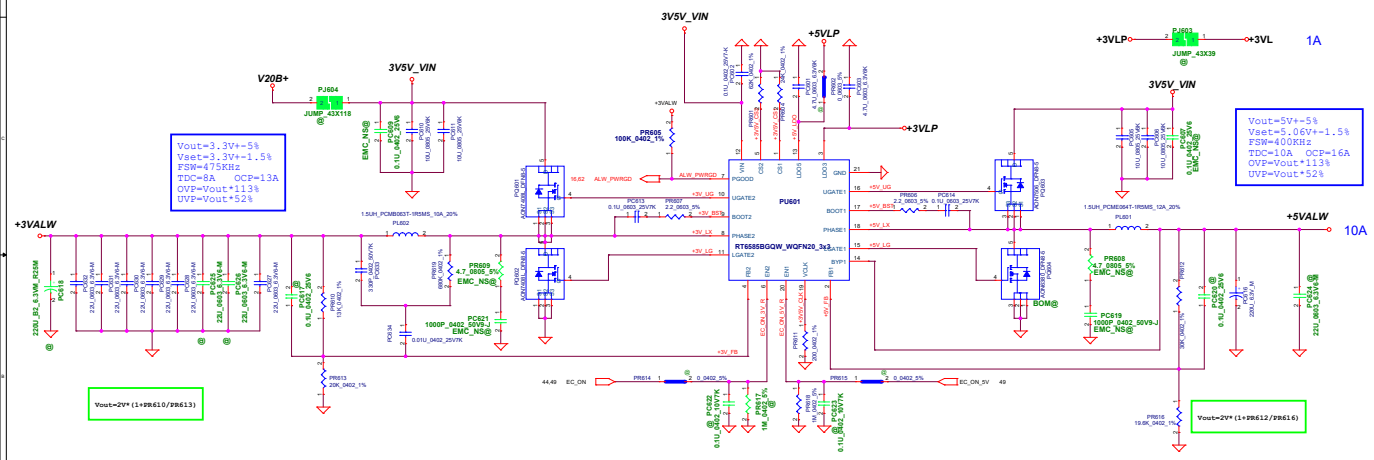
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title			
PWR-DCIN/BATT/RTC			
Size: Custom	Document Number: DZ510/DY512		Rev: 1.0
Date: Monday, July 02, 2018	Sheet 58 of 74		



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-charger		
Size	Document Number	DY520	Rev 0.1
Date: Monday, July 02, 2018	Sheet 59 of 74		



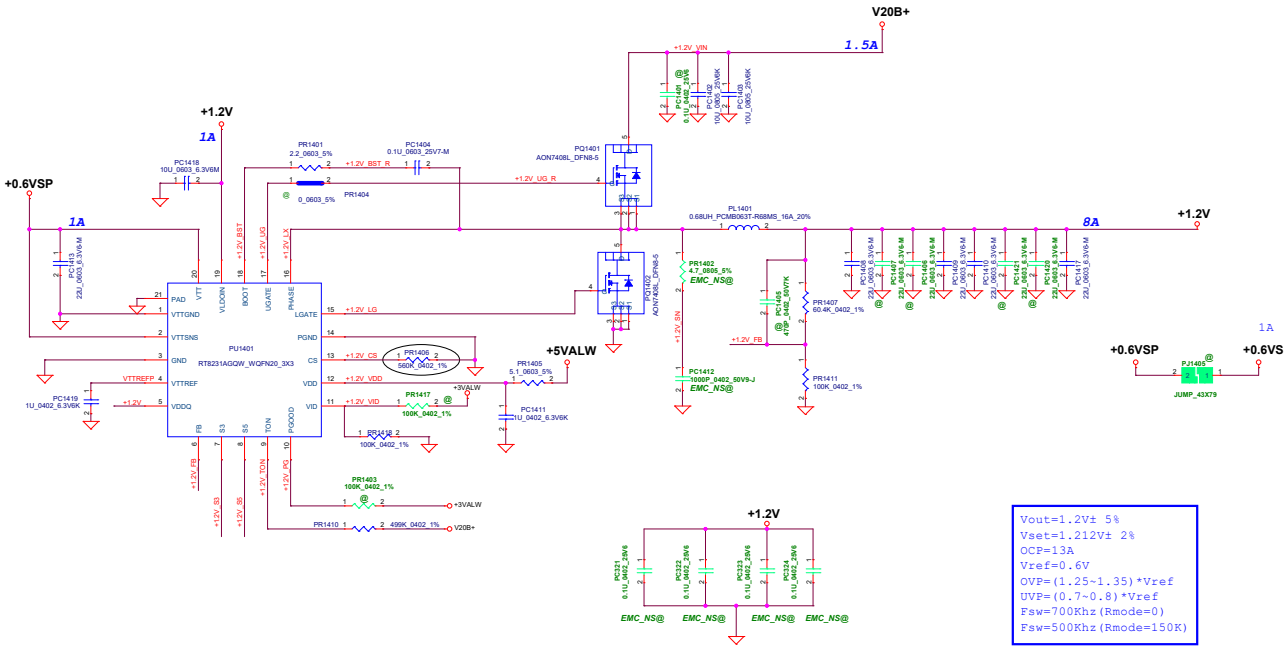
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

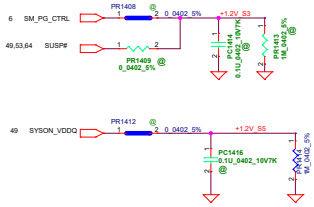
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D EXCEPT AS AUTHORIZED BY LC FUTURE CENTER CORPORATION OR ITS AUTHORIZED AGENT. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title: PWR-3/5VALW

Size: Custom | Document Number: DE510/DY512 | Rev: 1.0

Date: Monday, July 02, 2018 | Sheet 60 of 75





Vout=1.2V± 5%
Vset=1.212V± 2%
OCP=13A
Vref=0.6V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz(Rmode=0)
Fsw=500Khz(Rmode=150K)

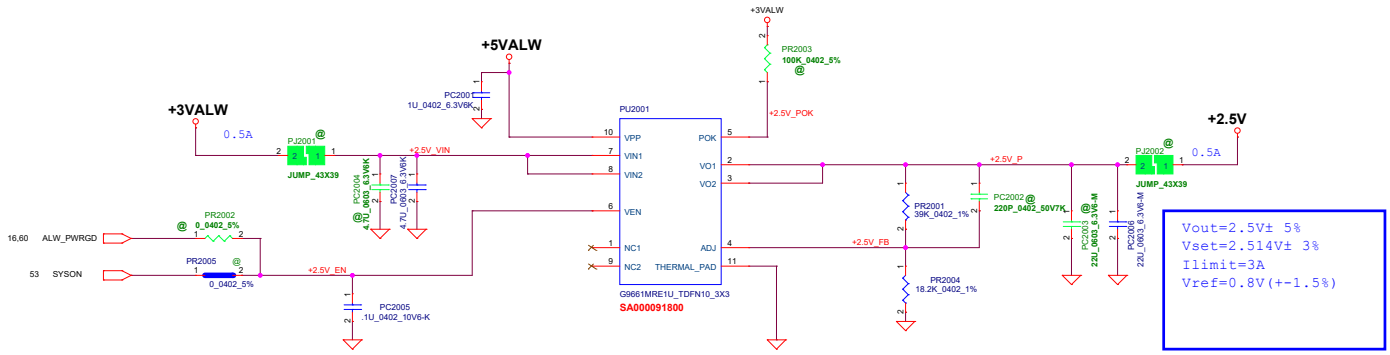
Vout=0.6V± 5%
OCP=1.5A
VTT=1/2VDDQ

STATE	EN1	EN2	VDDQ	VTT_REFP	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Note: S3 - sleep ; S5 - power off

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-VDDQ/VTT		
Size C	Document Number	DY520	Rev 0.1
Date:	Monday, July 02, 2018	Sheet	61 of 74

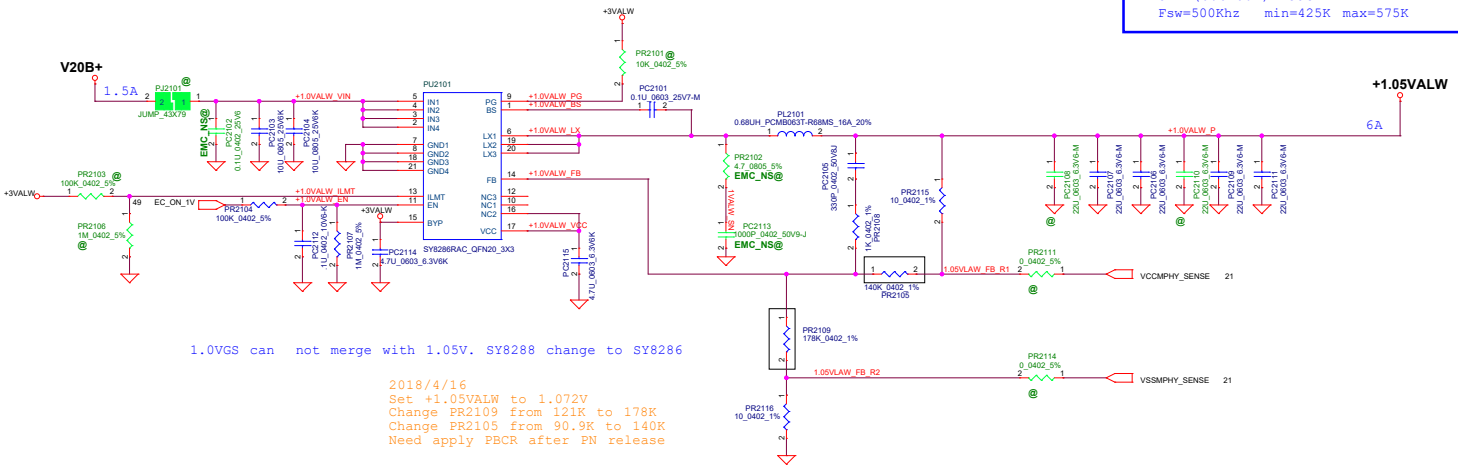


Need again link cis ,only change PN

Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-2.5V		
Size: Custom	Document Number: DY520		Rev: 0.1
Date: Monday, July 02, 2018	Sheet 62 of 74		

Vout=1.05V± 5%
Vset=1.051V± 1.81%
Vref=0.6V(+-1%)
TDC=8A
OCP=12A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K



1.0VGS can not merge with 1.05V. SY8288 change to SY8286

2018/4/16
Set +1.05VALW to 1.072V
Change PR2109 from 121K to 178K
Change PR2105 from 90.9K to 140K
Need apply PBCR after PN release

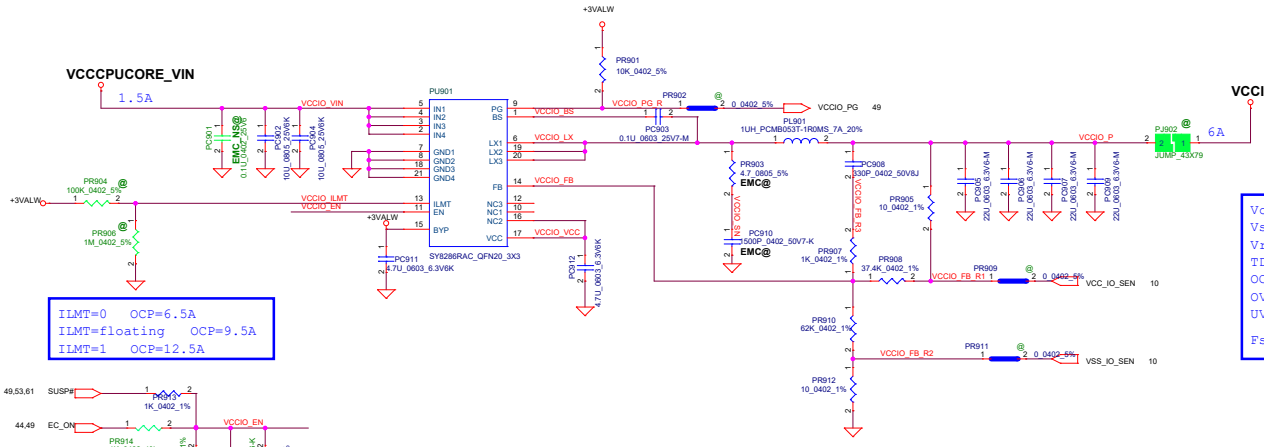
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-1.0VALW

Size	Document Number	Rev
Custom	DY510/DY511	1.0

Date: Monday, July 02, 2018 Sheet 63 of 74

VCCIO 20VB+ change to Core VIN for layout

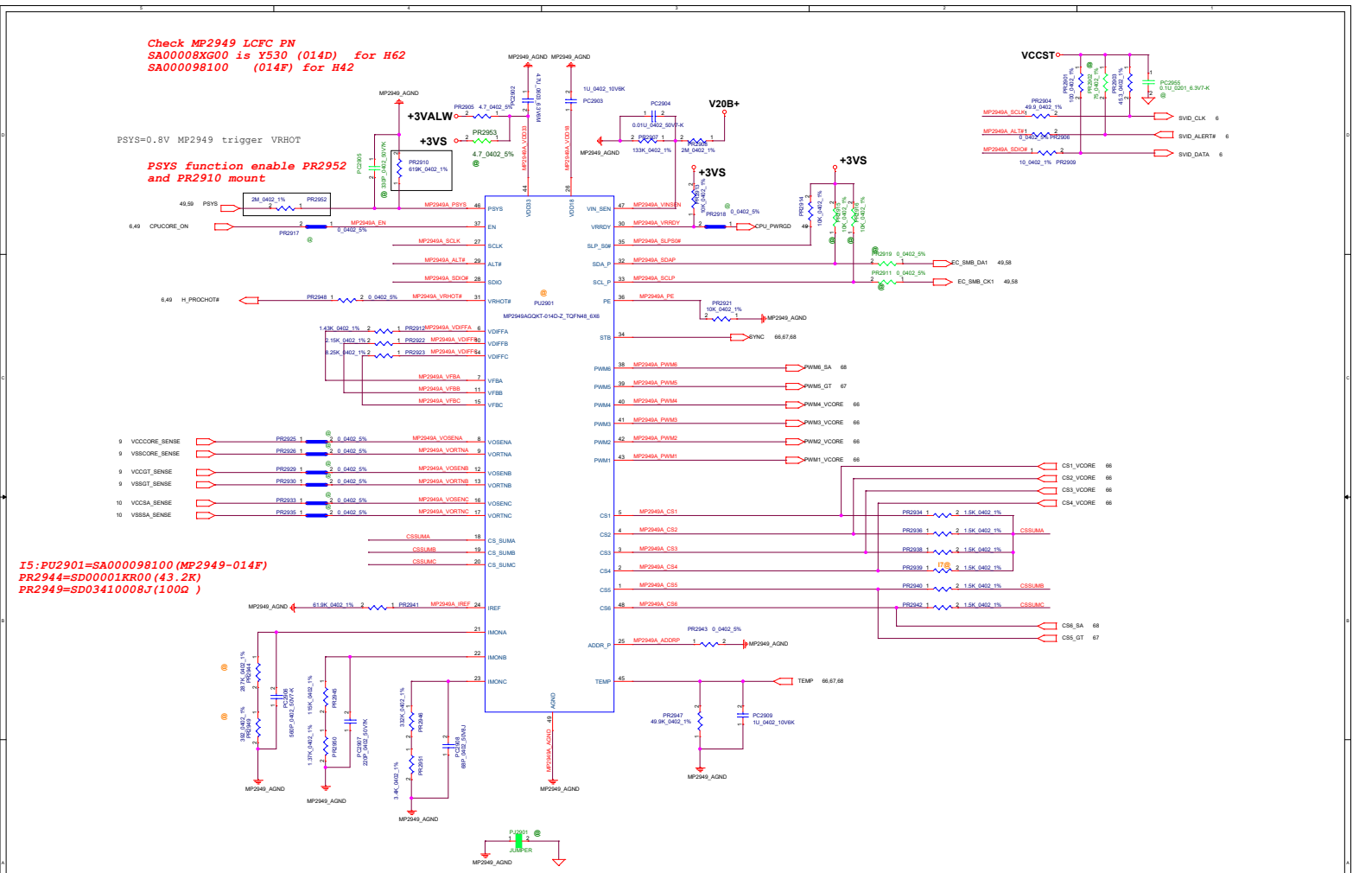


Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-VCCIO

Size	Document Number	Rev
Custom	DY510/DY511	1.0

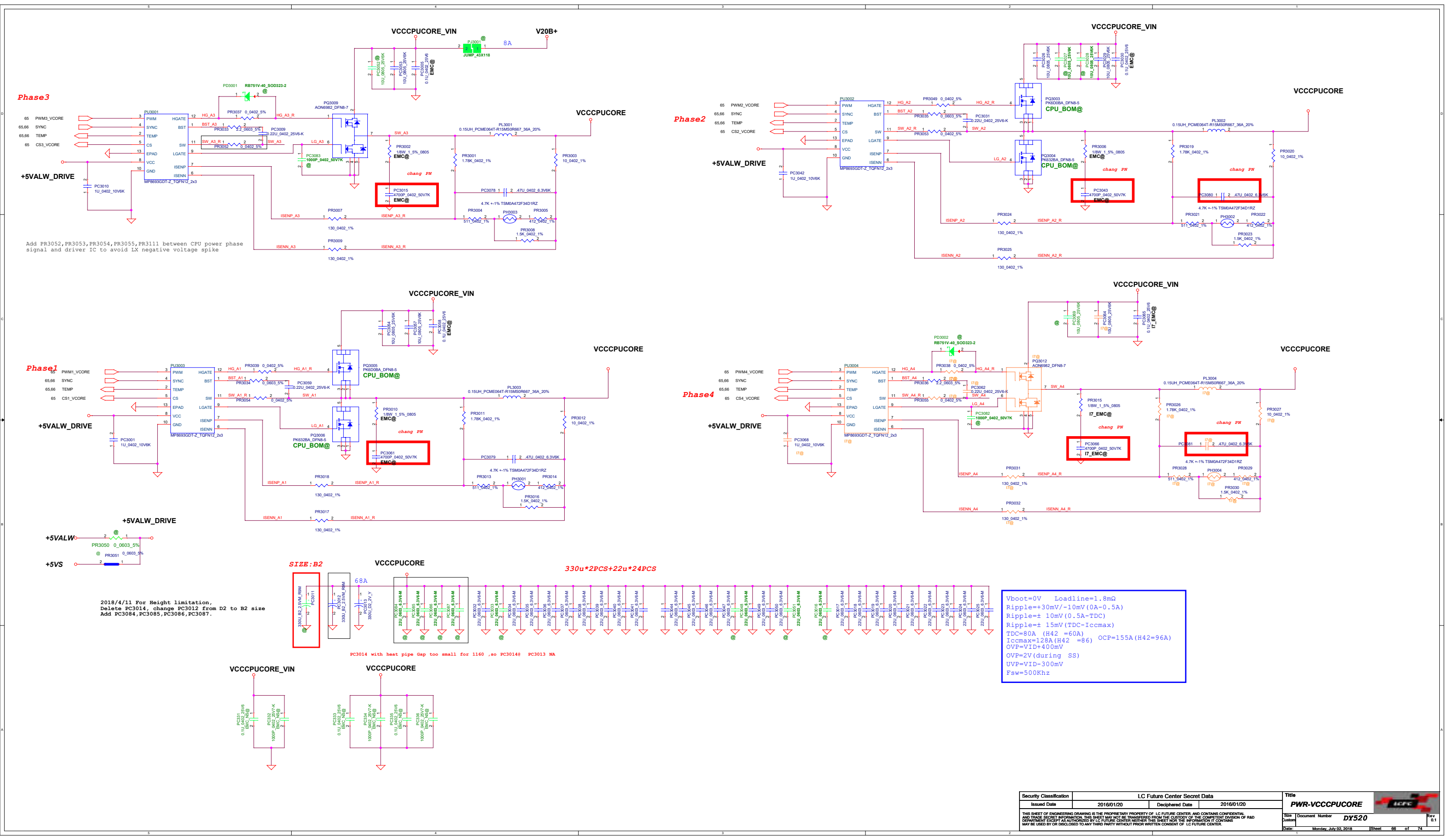
Date: Monday, July 02, 2018 Sheet 64 of 74



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

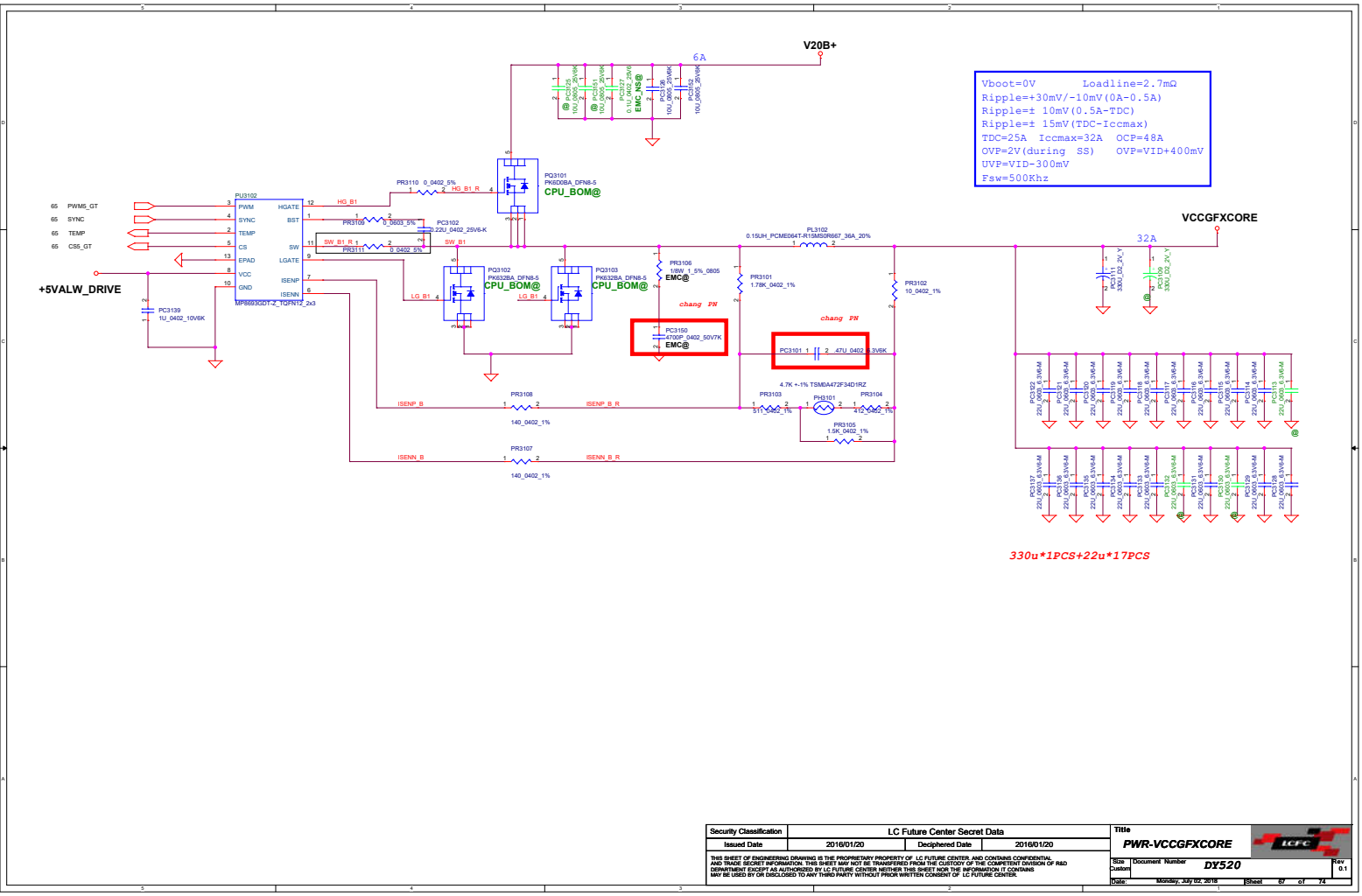
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D AND DISTRIBUTED EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.

Title	PWR-IMVP8_MP2949		
Size: Custom	Document Number: DY530		Rev: 0.1
Date: Monday, July 02, 2018	Sheet 65 of 74		



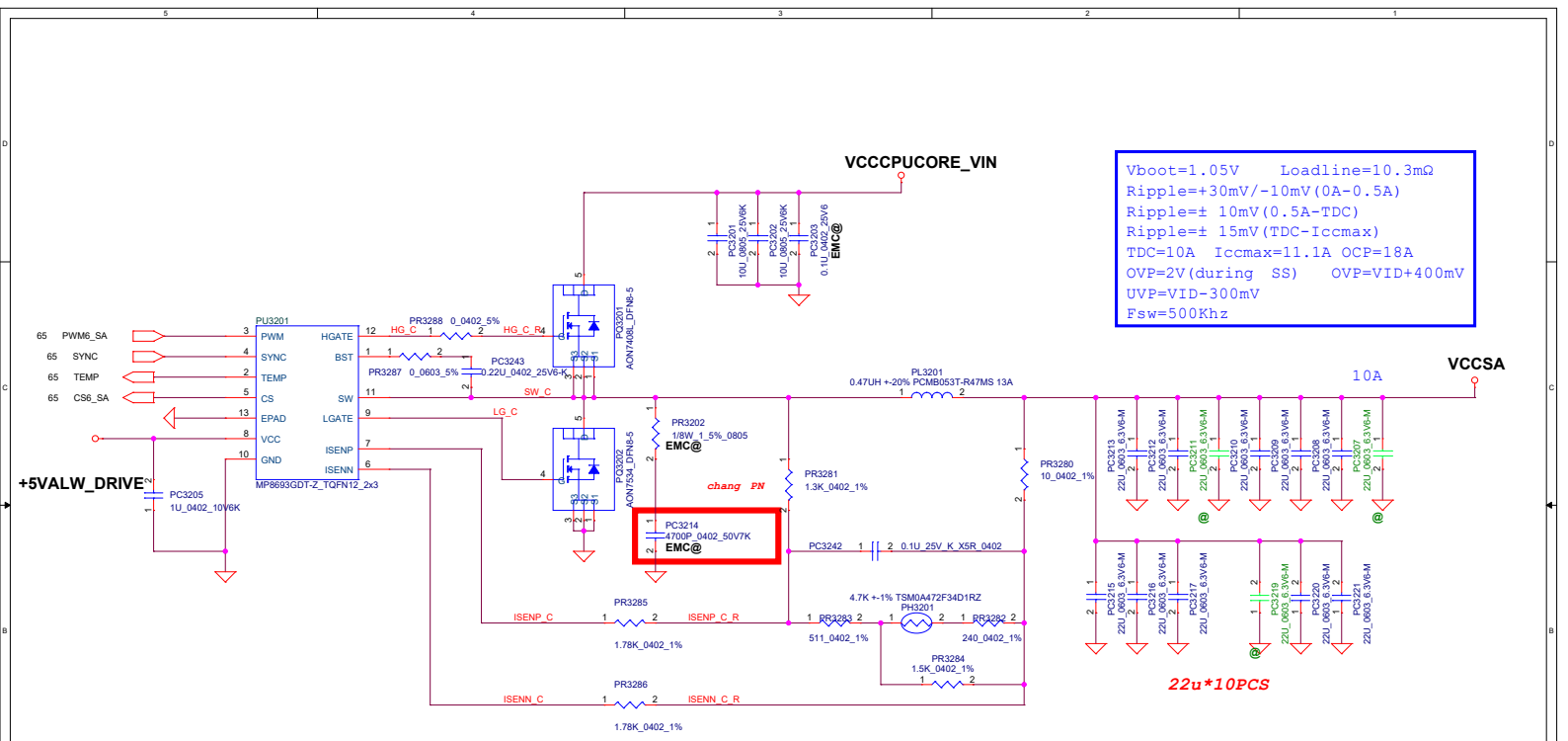
Phase3
Phase2
Phase1
Phase4
VCCCPUCORE_VIN
V20B+
8A
VCCCPUCORE
+5VALW_DRIVE
+5VALW
+5VS
MP8693GDT-Z_TQFN12_2x3
CPU_BOM@
EMC@
I7_EMC@
chang FW
Add PR3052,PR3053,PR3054,PR3055,PR3111 between CPU power phase signal and driver IC to avoid LX negative voltage spike
2018/4/11 For Height limitation,
Delete PC3014, change PC3012 from D2 to B2 size
Add PC3084,PC3085,PC3086,PC3087.
SIZE:B2
68A
330u*2PCS+22u*24PCS
PC3014 with heat pipe Gap too small for 1160 ,so PC3014@ PC3013 NA
Vboot=0V Loadline=1.8mΩ
Ripple=+30mV/-10mV(0A-0.5A)
Ripple=± 10mV(0.5A-TDC)
Ripple=± 15mV(TDC-Iccmax)
TDC=80A (H42 =60A)
Iccmax=128A(H42 =86)
OCP=155A(H42=96A)
OVP=VID+400mV
OVP=2V(during SS)
UVP=VID-300mV
Fsw=500Khz
Security Classification
LC Future Center Secret Data
Issued Date
2016/01/20
Deciphered Date
2016/01/20
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
PWR-VCCCPUCORE
Size Custom
Document Number
DY520
Rev 0.1
Date: Monday, July 02, 2018
Sheet 66 of 74

LG_A4



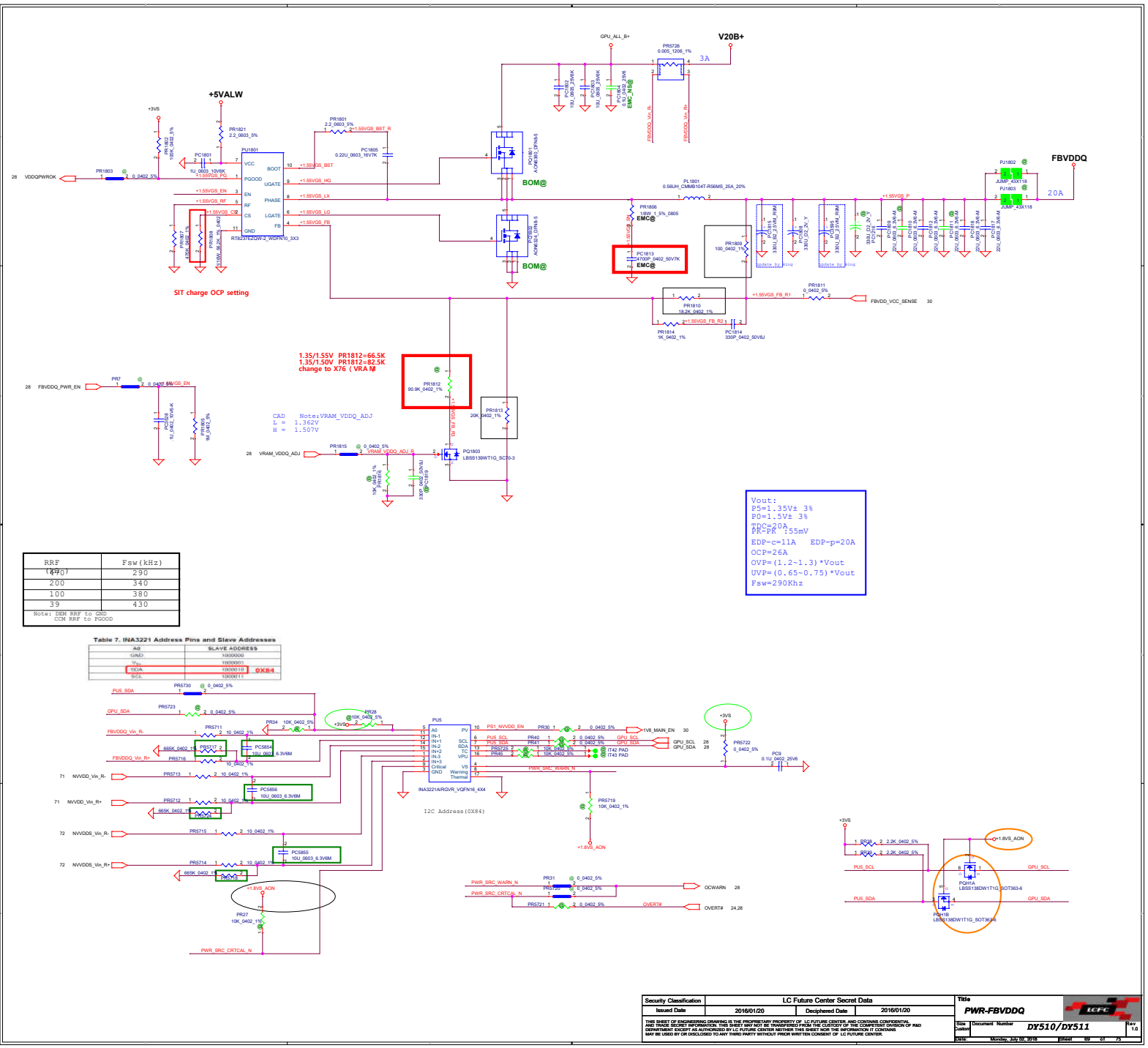
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-VCCGFXCORE		
Size: Custom	Document Number: DY520		Rev: 0.1
Date: Monday, July 02, 2018	Sheet 67 of 74		



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-VCCSA		
Size	Document Number	DY520	Rev 0.1
B			
Date:	Monday, July 02, 2018	Sheet	68 of 74



RRF (kΩ)	Fsw(kHz)
470	290
200	340
100	380
39	430

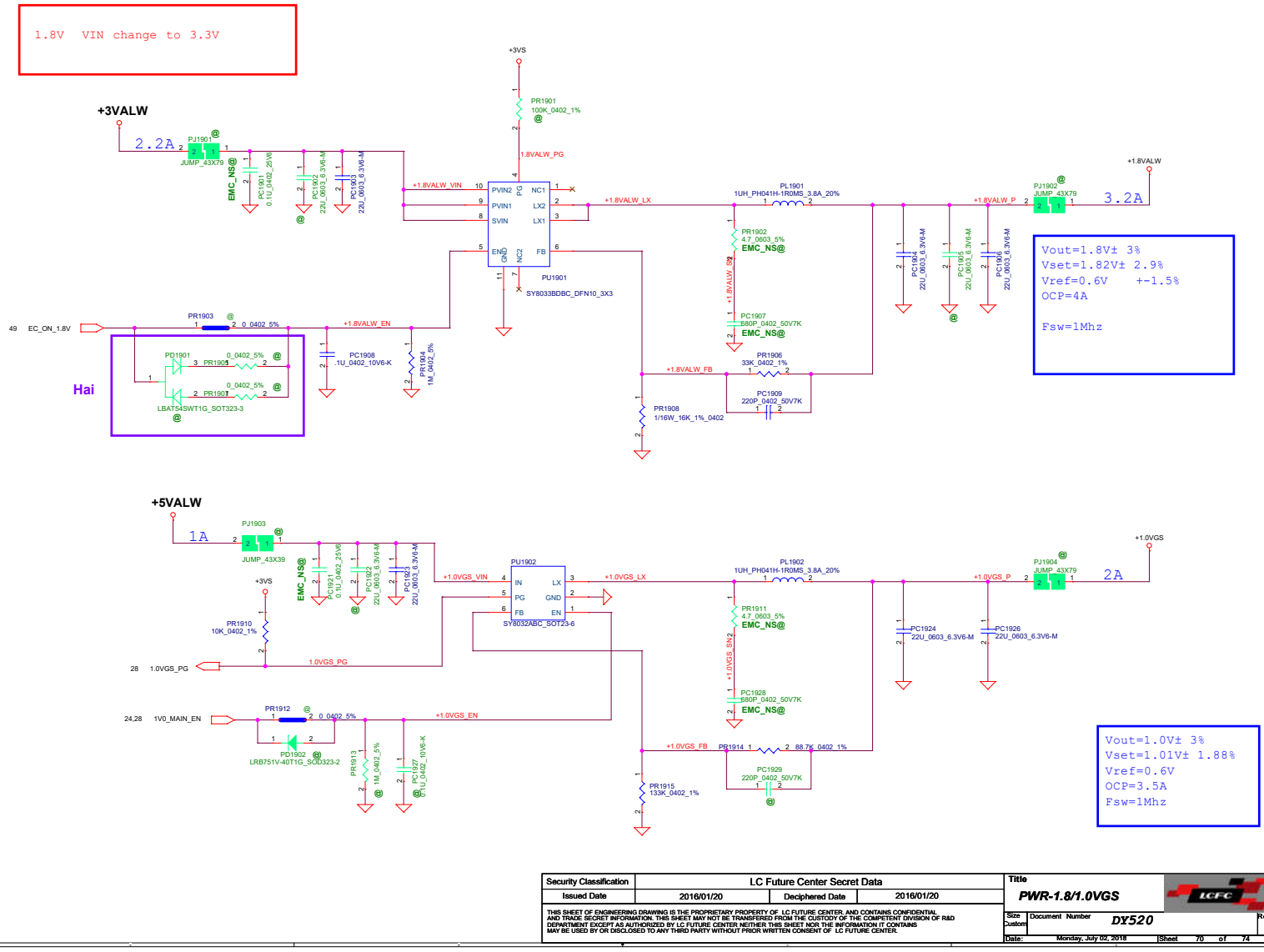
Note: DEM RRF to GND
COM RRF to PGOOD

Table 7. INA3221 Address Pins and Slave Addresses

A0	SLAVE ADDRESS
GND	1000000
V_{PU}	1000001
SDA	1000010 0X84
SCL	1000011

Security Classification	LC Futures Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-FBVDDQ		
Size: Custom	Document Number: DY510/DY511		Rev: 1.0
Date: Monday, July 02, 2018	Sheet 69 of 75		


1.8V VIN change to 3.3V
+3VALW
2.2A
PJ1901
JUMP_43X79
EMC_NS@
PC1901
0.1U_0402_25V6
PC1902
22U_0603_6.3V6-M
PC1903
22U_0603_6.3V6-M
+3VS
PR1901
100K_0402_1%
1.8VALW_PG
+1.8VALW_VIN
PVIN2
PVIN1
SVIN
EN
GND
PG
NC2
NC1
LX2
LX1
FB
PU1901
SY8033BDBC_DFN10_3X3
+1.8VALW_LX
PL1901
1UH_PH041H-1R0MS_3.8A_20%
+1.8VALW_P
PJ1902
JUMP_43X79
3.2A
+1.8VALW
PC1904
22U_0603_6.3V6-M
PC1905
22U_0603_6.3V6-M
PC1906
22U_0603_6.3V6-M
PR1902
4.7_0603_5%
EMC_NS@
+1.8VALW_SW
PC1907
680P_0402_50V7K
EMC_NS@
PR1906
33K_0402_1%
PC1909
220P_0402_50V7K
+1.8VALW_FB
PR1908
1/16W_16K_1%_0402
Vout=1.8V± 3%
Vset=1.82V± 2.9%
Vref=0.6V +-1.5%
OCP=4A
Fsw=1Mhz
49 EC_ON_1.8V
PR1903
0_0402_5%
+1.8VALW_EN
PC1908
.1U_0402_10V6-K
PR1904
1M_0402_5%
PD1901
PR1905
0_0402_5%
PR1907
0_0402_5%
LBAT54SWT1G_SOT323-3
Hai
+5VALW
1A
PJ1903
JUMP_43X39
EMC_NS@
PC1921
0.1U_0402_25V6
PC1922
22U_0603_6.3V6-M
PC1923
22U_0603_6.3V6-M
+3VS
PR1910
10K_0402_1%
28 1.0VGS_PG
1.0VGS_PG
PU1902
SY8032ABC_SOT23-6
+1.0VGS_VIN
IN
PG
FB
LX
GND
EN
+1.0VGS_LX
PL1902
1UH_PH041H-1R0MS_3.8A_20%
+1.0VGS_P
PJ1904
JUMP_43X79
2A
+1.0VGS
PC1924
22U_0603_6.3V6-M
PC1926
22U_0603_6.3V6-M
PR1911
4.7_0603_5%
EMC_NS@
+1.0VGS_SW
PC1928
680P_0402_50V7K
EMC_NS@
PR1914
88.7K_0402_1%
PC1929
220P_0402_50V7K
+1.0VGS_FB
PR1915
133K_0402_1%
Vout=1.0V± 3%
Vset=1.01V± 1.88%
Vref=0.6V
OCP=3.5A
Fsw=1Mhz
24,28 1V0_MAIN_EN
PR1912
0_0402_5%
+1.0VGS_EN
PD1902
LRB751V-40T1G_SOD323-2
PR1913
1M_0402_5%
PC1927
.1U_0402_10V6-K
Security Classification
LC Future Center Secret Data
Issued Date
2016/01/20
Deciphered Date
2016/01/20
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.
Title
PWR-1.8/1.0VGS
Size
Custom
Document Number
DY520
Rev
0.1
Date:
Monday, July 02, 2018
Sheet
70
of
74

PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
Nt(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component Value		
R1(KΩ)	PRS816	6.19
R2(KΩ)	PRS811	20.5
R3(KΩ)	PRS815	4.32
R4(KΩ)	PRS813	16.5
R5(KΩ)	PRS818	0.309
C(nF)	PCS838	4.7

PSI Level	Power Mode	Phase Configuration
PSI<0.4V	PS4	1Phase DEM
0.8V<PSI<1V	PS3	1Phase PCCM
1.4V<PSI<5.5V	PS1	3Phase PCCM

Vboot=0.8V
Ripple=± 20mV
IDC=60A Iccmax=127A OCP= 154A
Vref=2V
SUVP:VFb=0.2V
SOVP:Vcomp=3V
OVP:VFb=2V
Fsw=345KHz

VR Remote Sense - Tie to GPU sense points

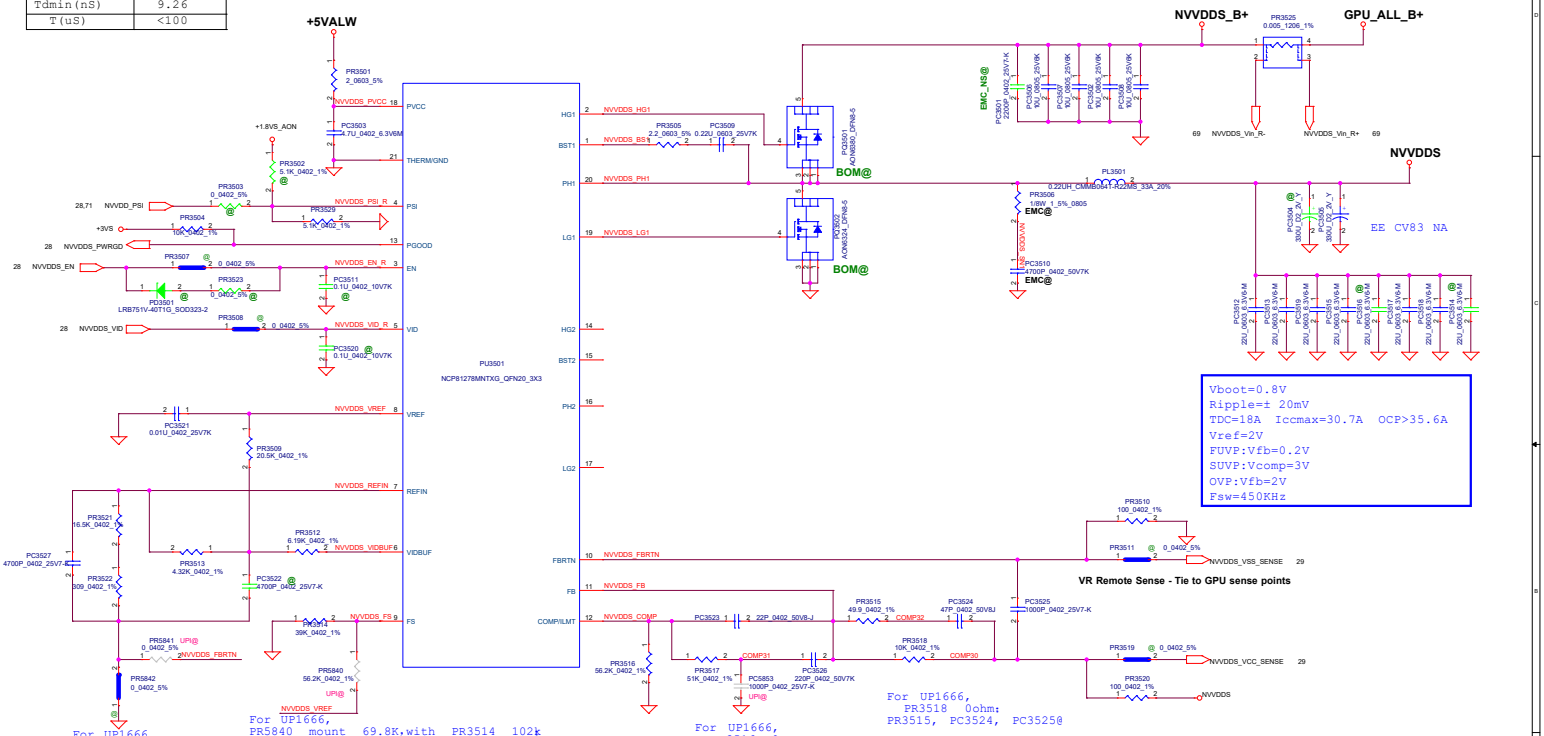
Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-NVVDD	
Size	Document Number	Rev
A	DB510/DY512	1.0
Date: Monday, July 04, 2016	Sheet 21 of 41	

PWM-VID Specification	
	Config
Vmin(V)	0.3
Vmax(V)	1.3
Vboot(V)	0.8
Vstep(mV)	6.25
N(level)	160
Fpwm(KHz)	675
Tdmin(nS)	9.26
T(uS)	<100

Component	Value	
R1(KΩ)	PR9440	6.19
R2(KΩ)	PR9434	20.5
R3(KΩ)	PR9436	4.32
R4(KΩ)	PR9437	16.5
R5(KΩ)	PR9431	0.309
C(nF)	PC1277	4.7

PSI Level	Power Mode	Phase Configuration
Connected to PVCC	PSH	2Phase Auto CCM/DCM
High	PS0	2Phase FCCM
Intermediate	PS1	2Phase Auto CCM
Low	PS2	1Phase Auto CCM/DCM



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title: PWR-NVVDDS

Size	Document Number	Rev
C	DY510/DY511	1.0

Date: Monday, July 02, 2018 Sheet 72 of 75

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2015/02/26

Title

Blank

Size	Document Number	Rev
D	DE510/DY512	1.0

Date: Thursday, July 09, 2015 Sheet 79 of 80

Security Classification	LC Future Center Secret Data		
Issued Date	2015/02/26	Deciphered Date	2015/02/26

Title: *Blank*

Size: D | Document Number: *DE510/DY512* | Rev: 1.0

Date: Thursday, July 09, 2015 | Sheet 19 of 19