MS-A953 Ver: 1.0

Title	Page
Cover Sheet	1
Block Diagram	2
PROCESSOR-1 (HOST BUS)	3
PROCESSOR-2 (DDR3)	4
PROCESSOR-3 (POWER)	5
PROCESSOR-4 GRAPHICS POWER	6
PROCESSOR-5 (GND)	7
PROCESSOR-6 (RESERVE)	8
DDR III SODIMM1	9
PCH-1 (HDA/JTAG/SATA)	11
PCH-2 (PCI-E/SMBUS/CLK)	12
PCH-3 (DMI/FDI/GPIO)	13
PCH-4 (LVDS/DDI/VGA)	14
PCH-5 (PCI/USB/NVRAM)	15
PCH-6 (GPIO/NCTF/RSVD)	16
PCH-7 (POWER)	17
PCH-8 (POWER)	18
PCH-9 (GND)	19
PCH-10 (STRAPS)	20
SIO-Fintek F71878AD	21
HDMI	22
VGA / LVDS	23
LAN-RTL8111E-VB-GR	24
Audio Codec ALC887	25
USB / IR / TOUCH / WEBCAM	26
SATA / FAN Control/COM	27
DDR Power -NCP5217- 1-Phase	28
CP / CPU_SA Power	29
CPU VCOER VCCP	31
CPU_VTT -NCP5217- 1-Phase	32
ATX/EMI/12V_REG/VCC1_8	33
3V/5V (TPS51125RGER)	34
CARD READER_RTS5139	35
Mini-PCIE Slot	36
Single Touch ETP-CP-ETR4000	37
HOTKEY/LED/Edi-Tensor	38
Manual Parts	39
S I/O BLOCK DIAGRAM	40
Power Delivery	41
HISTORY	42
External Converter	43
Power Sequencing	44
ASmedia USB3.0 (ASM1042)	45

CPU:

INTEL-Celeron B847

System Chipset:

INTEL-NM70

OnBoard Chipset:

HD Audio Codec:ALC887 CG

LAN:Realtek RTL8111E CG

SIO:Fintek F71878AD

Main Memory:

DDRIII (1333MHz) * 1

Expansion Slots:

MINIPCI Express (X1) Slot * 2

PWM:

Controller:ISL95837HRZ 1+1Phase (10W)

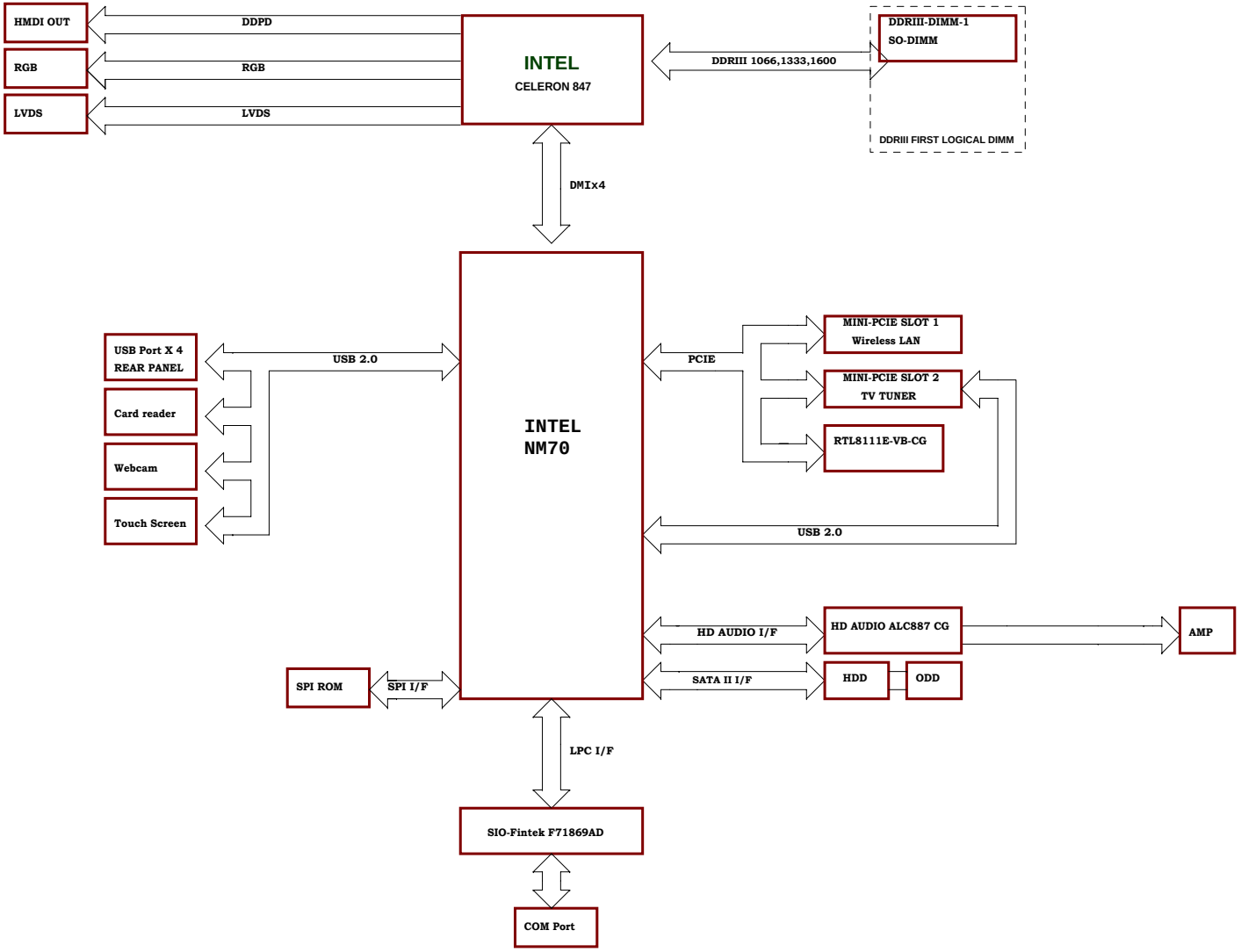
Other:

SATA(SATA2-300MB/s) *2

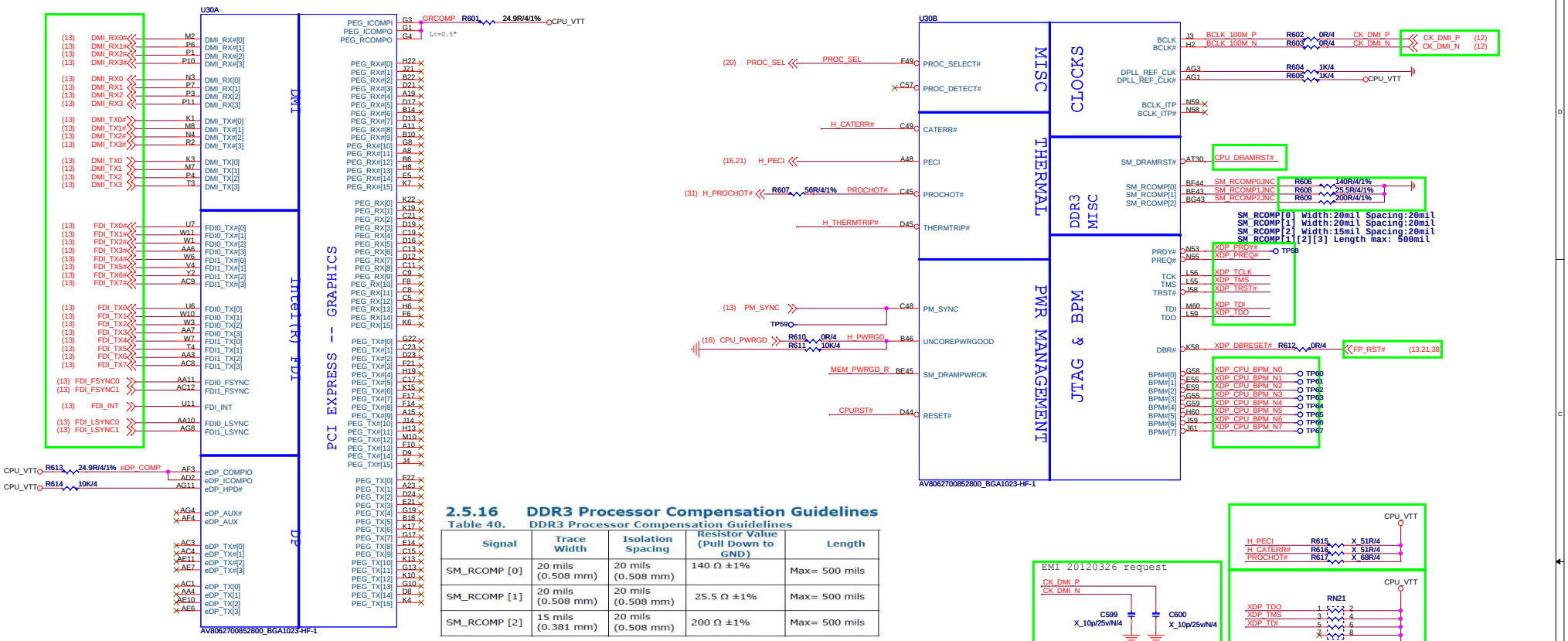
USB2.0 *2
USB3.0 *2 (USB2.0 option)
HDMI OUT *1
Card reader*1
COM Port*2

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A953	
Size: Custom	Document Description: Cover Sheet	Rev: 1.0
Date: Wednesday, October 24, 2012	Sheet 1 of 45	

MS-A953



MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: C	Document Description: Block Diagram	Rev: 1.0
Date: Tuesday, October 02, 2012	Sheet 2 of 45	

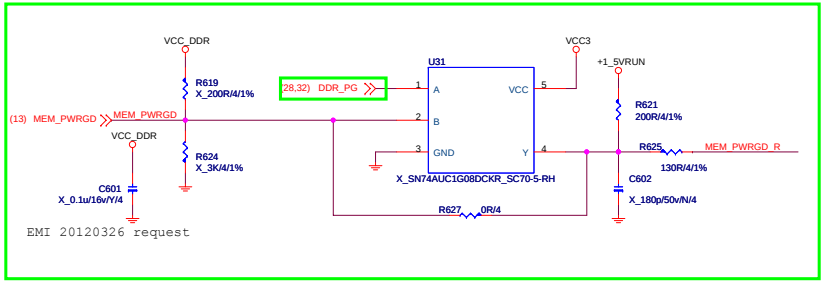


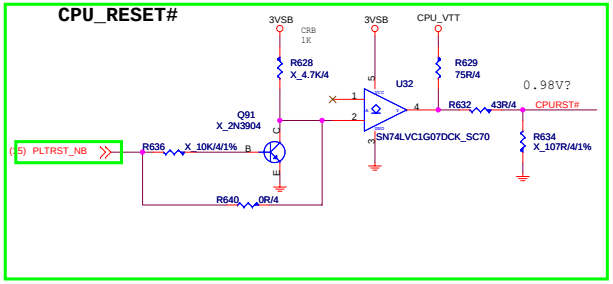
2.5.16 DDR3 Processor Compensation Guidelines

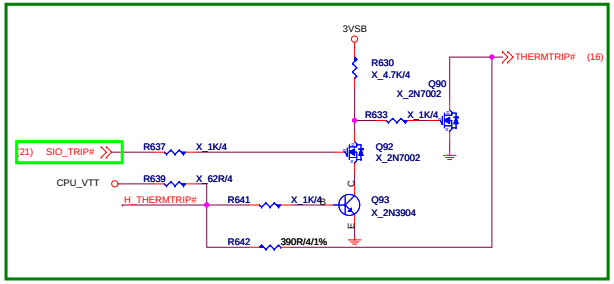
Table 40. DDR3 Processor Compensation Guidelines

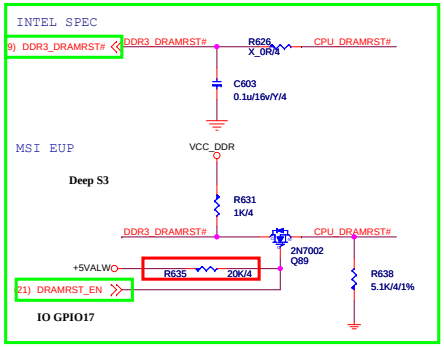
Signal	Trace Width	Isolation Spacing	Resistor Value (Pull Down to GND)	Length
SM_RCOMP [0]	20 mils (0.508 mm)	20 mils (0.508 mm)	140 Ω ±1%	Max= 500 mils
SM_RCOMP [1]	20 mils (0.508 mm)	20 mils (0.508 mm)	25.5 Ω ±1%	Max= 500 mils
SM_RCOMP [2]	15 mils (0.381 mm)	20 mils (0.508 mm)	200 Ω ±1%	Max= 500 mils

Intel Comments:
eDP COMP signals are required
if integrated gfx is enabled even
if eDP interface is disabled.

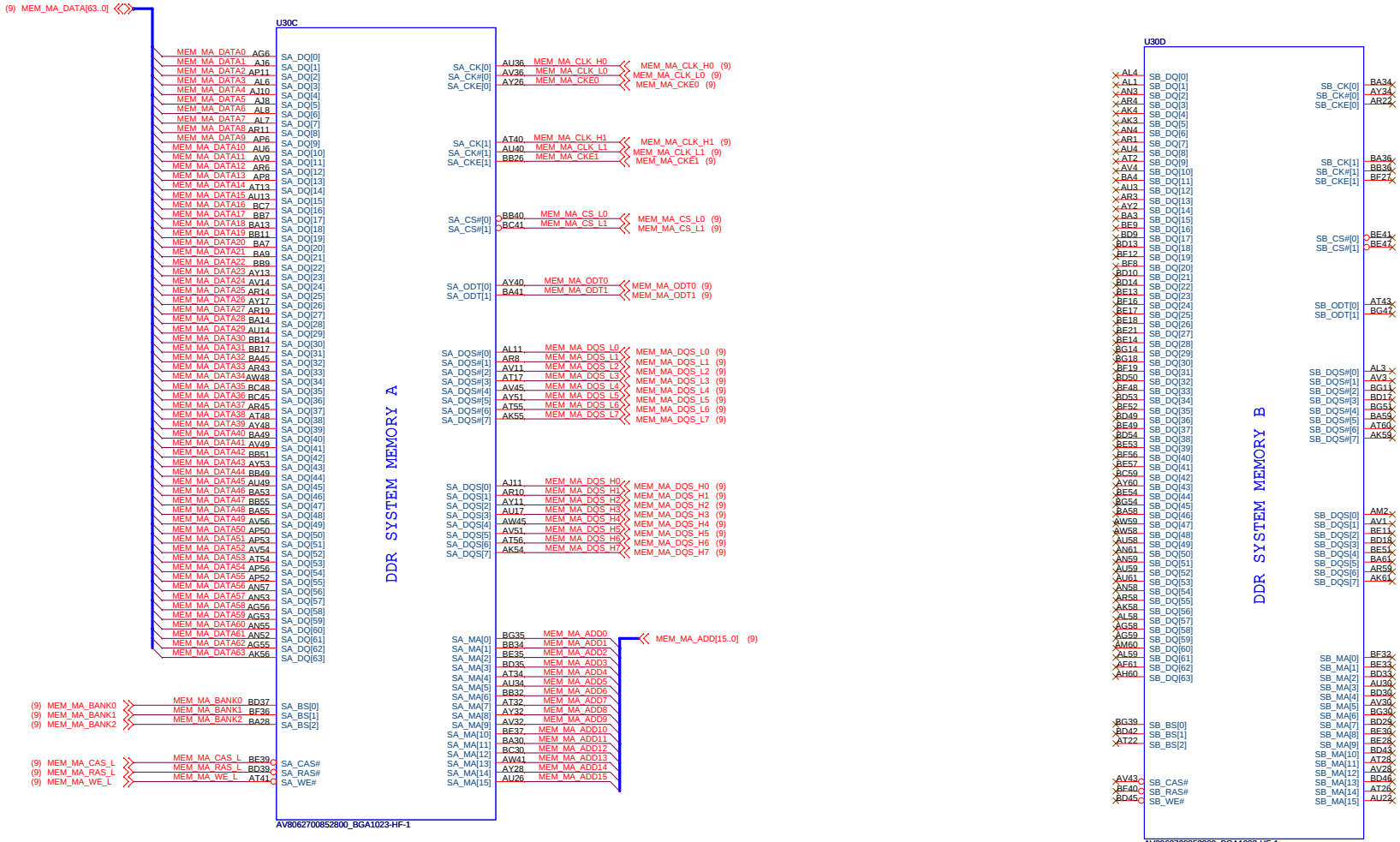








MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: PROCESSOR-1 (HOST BUS)	Rev: 1.0
Date: Monday, October 22, 2012	Sheet 3 of 45	

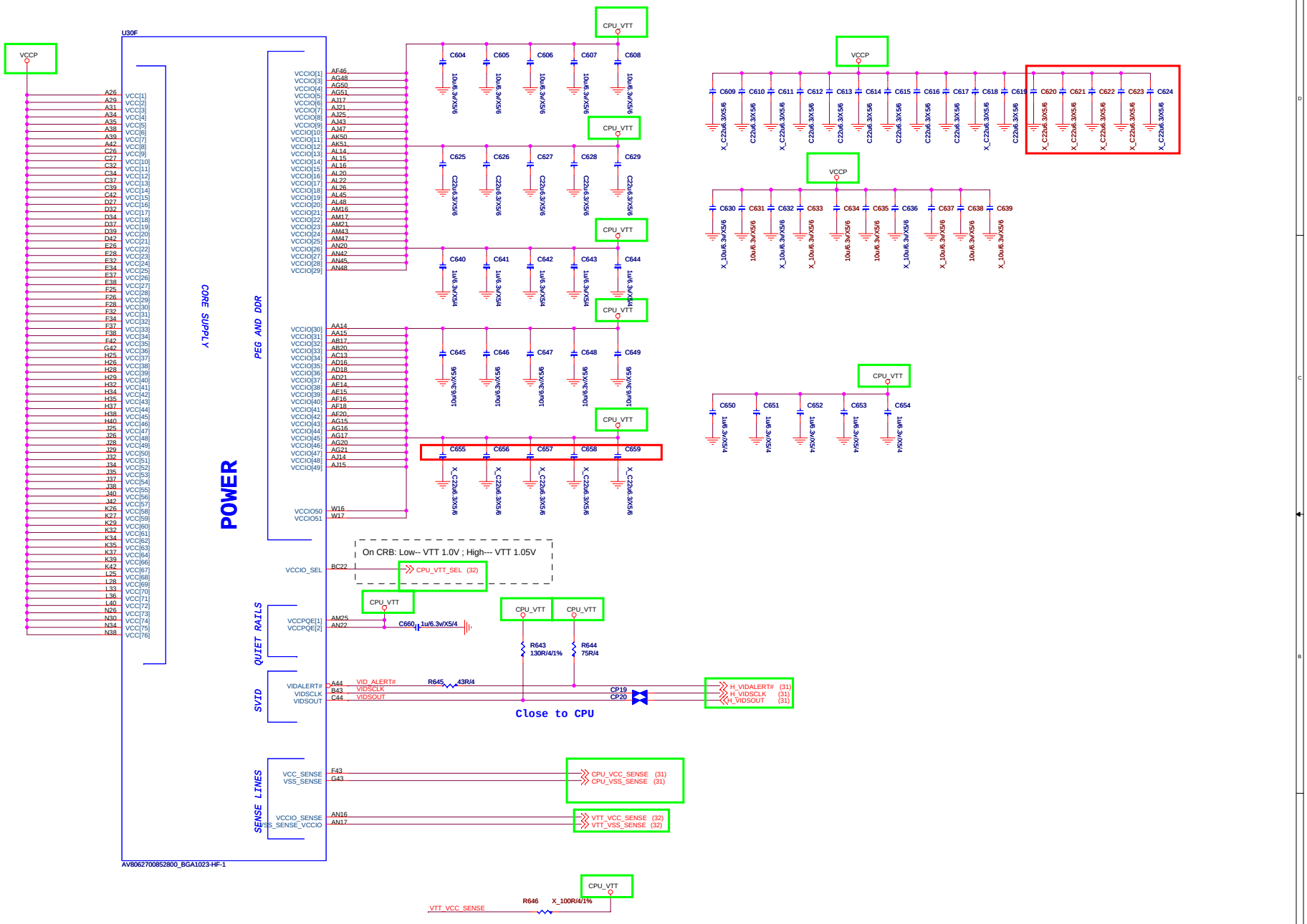


MICRO-STAR INT'L CO.,LTD

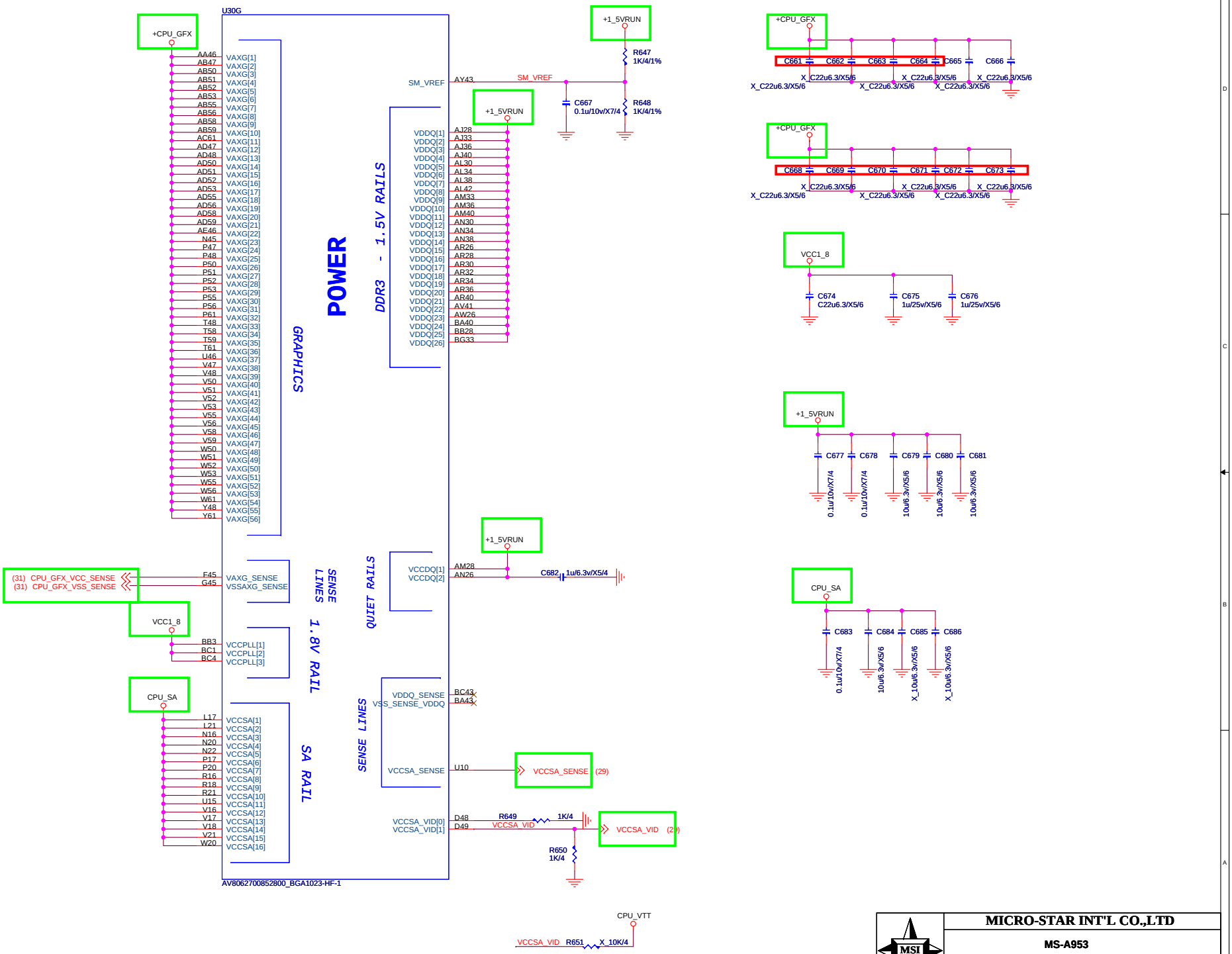
MS-A953

Size	Document Description	Rev
Custom	PROCESSOR-2 (DDR3)	1.0

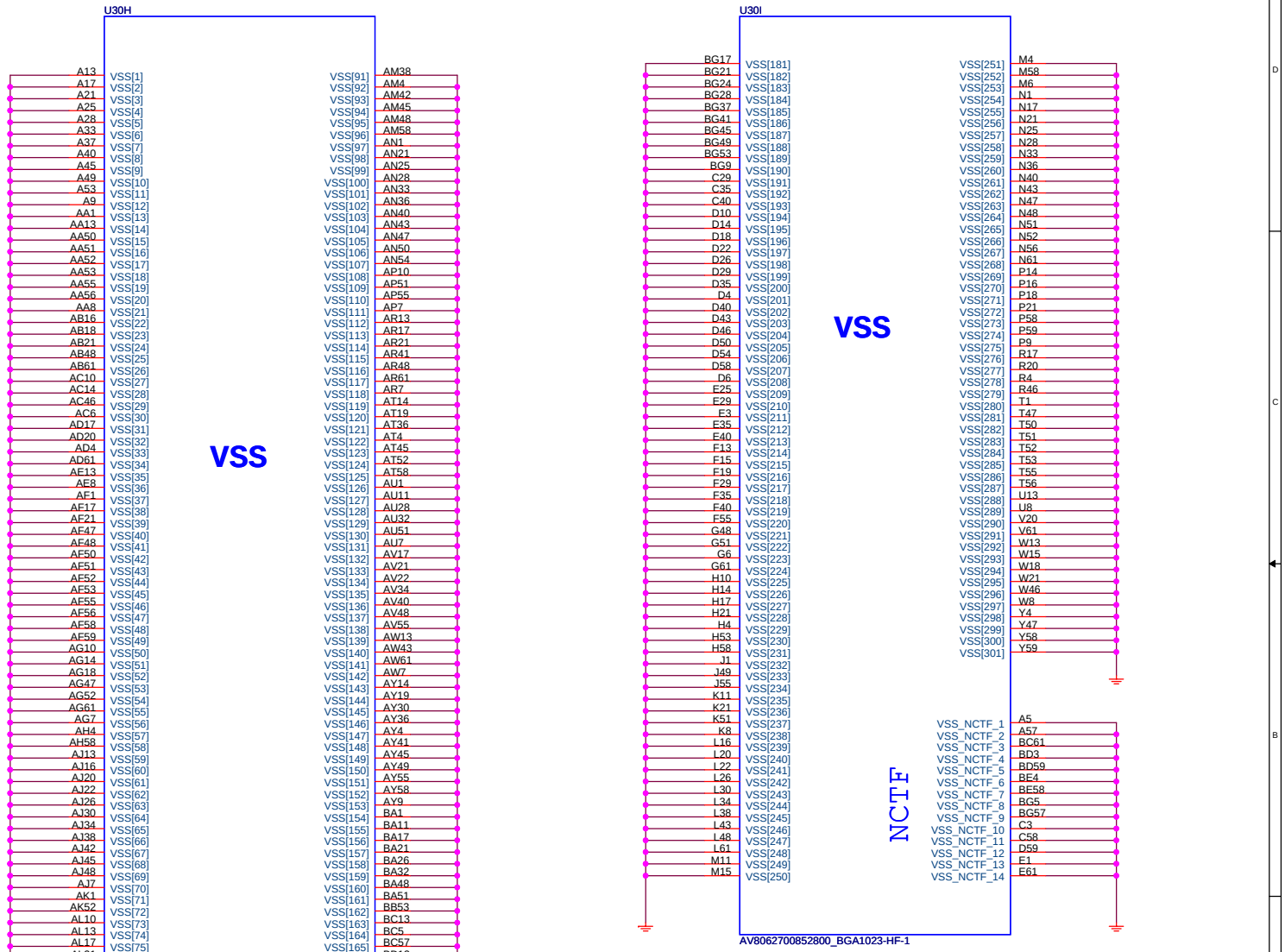
Date: Monday, October 22, 2012 Sheet 4 of 45



MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: PROCESSOR-3 (POWER)	Rev: 1.0
Date: Thursday, November 01, 2012	Sheet 5 of 45	

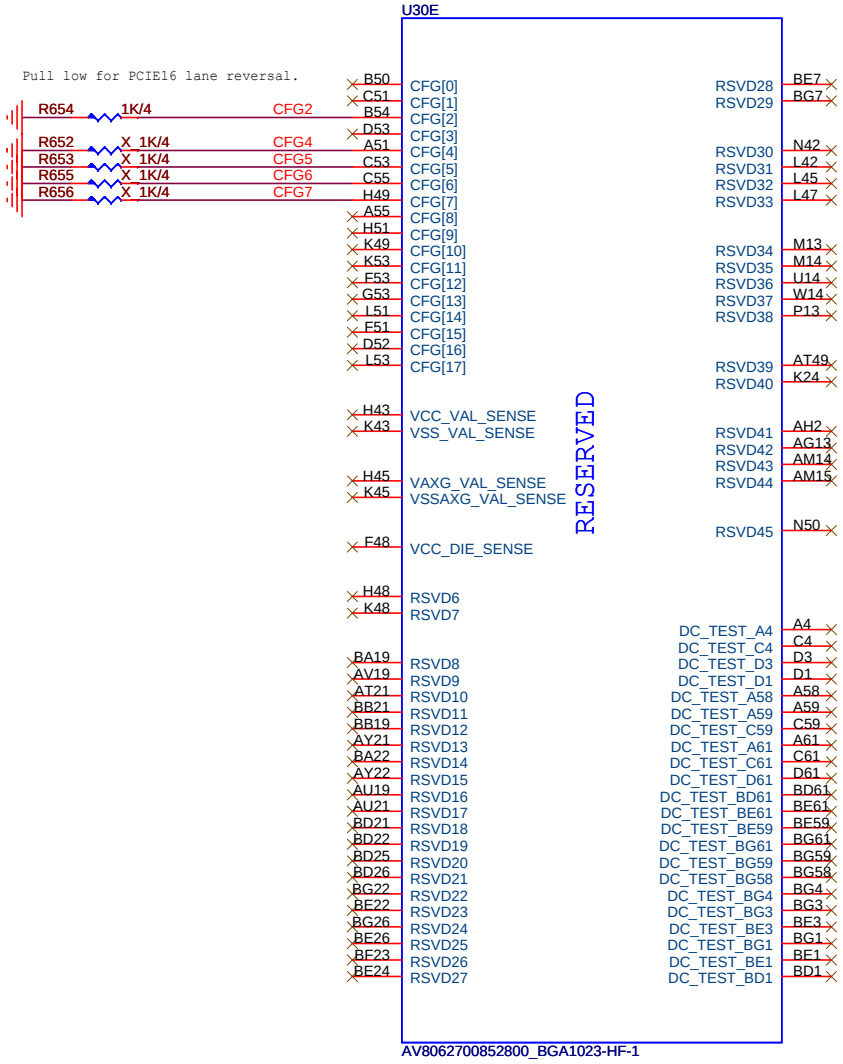


MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: PROCESSOR-4 GRAPHICS POWER	Rev: 1.0
Date: Thursday, November 01, 2012	Sheet 6 of 45	



MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: PROCESSOR-5 (GND)	Rev: 1.0
Date: Tuesday, October 02, 2012	Sheet 7 of 45	

SANDYBRIDGE PROCESSOR (RESERVED)



CFG2 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

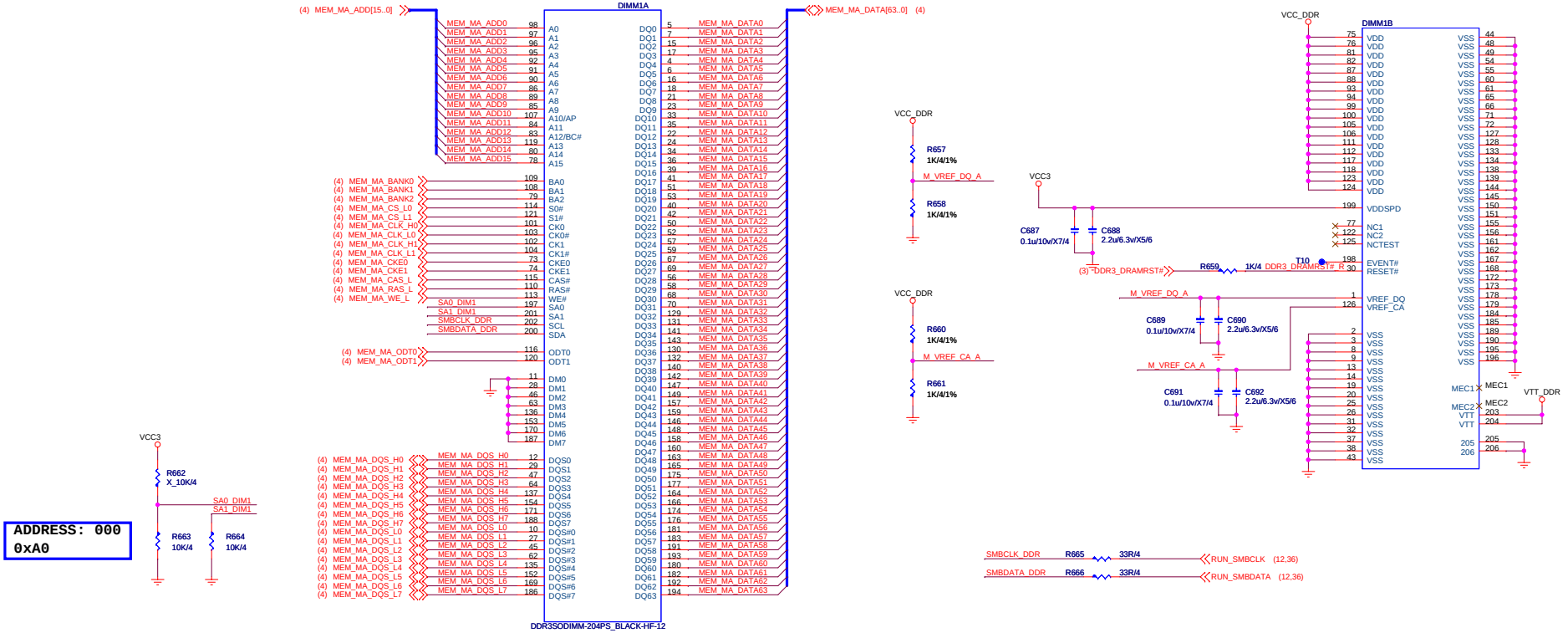
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

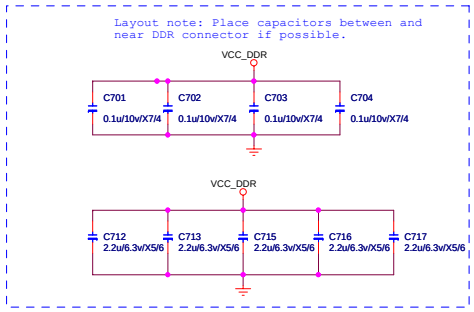
PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

PEG DEFER TRAINING	
CFG7	1 :(Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

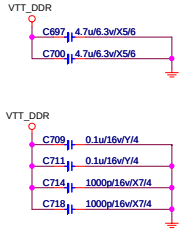
MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: PROCESSOR-6 (RESERVE)	Rev: 1.0
Date: Tuesday, October 02, 2012	Sheet 8 of 45	

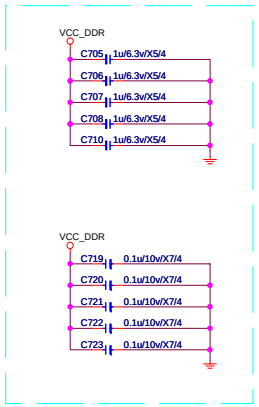
SODIMM#A

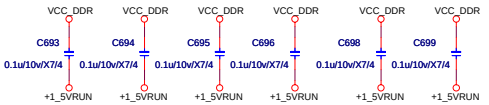




CHANNEL A V_SM_VTT DECOUPLING CAPS







MICRO-STAR INT'L CO.,LTD	
MS-A953	
Size: Custom	Document Description: DDR III SODIMM1 — Rev: 1.0
Date: Wednesday, October 24, 2012	Sheet 9 of 45

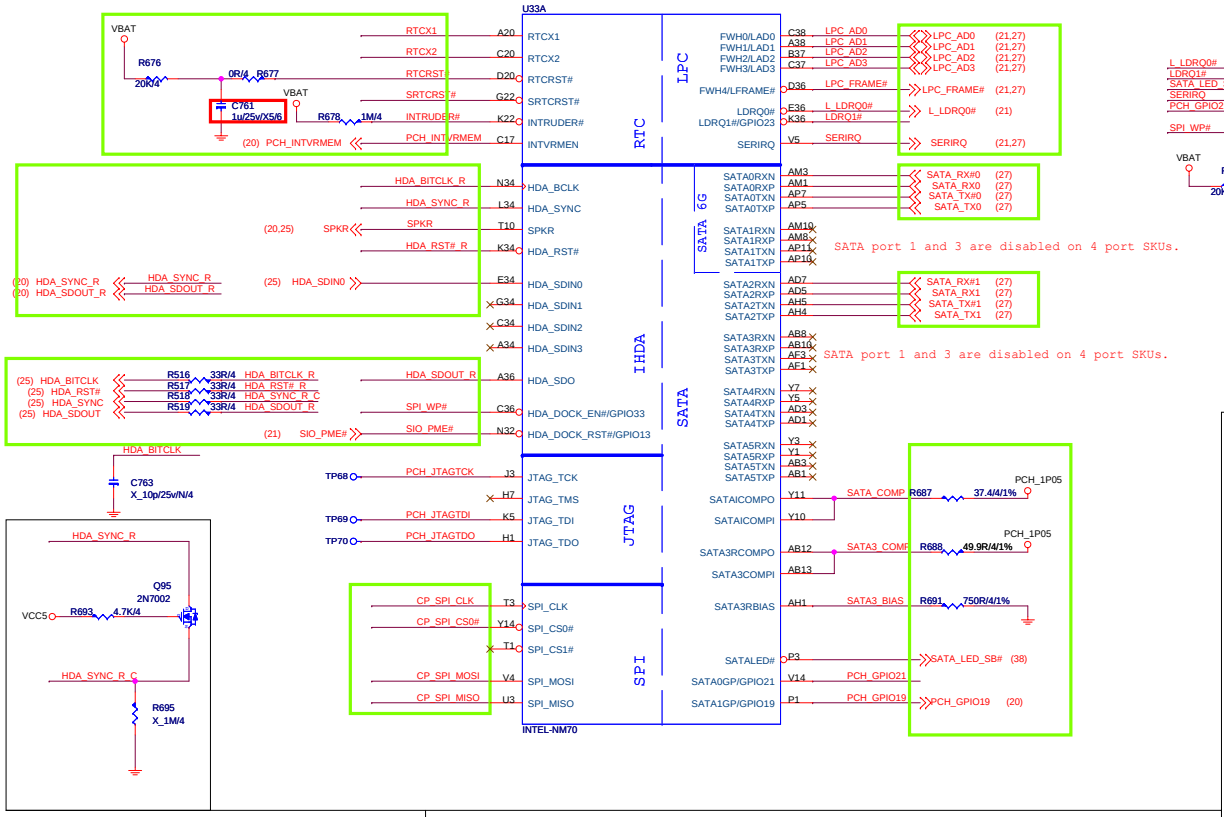
SODIMM#B

MICRO-STAR INT'L CO.,LTD

MS-A953

Size	Document Description	Rev
Custom	DDR III SODIMM 2	1.0

Date: Tuesday, October 02, 2012 | Sheet 10 of 45



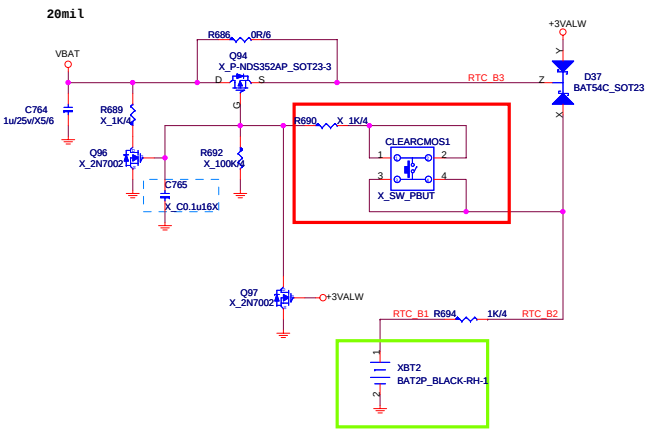
Serial ATA (SATA) Controller

The PCH has two integrated SATA host controllers that support independent DMA operation on up to six ports and supports data transfer rates of up to 6.0 Gb/s (600 MB/s) on up to two ports while all ports support rates up to 3.0 Gb/s (300 MB/s) and up to 1.5 Gb/s (150 MB/s). The SATA controller contains two modes of operation—a legacy mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities.

The PCH supports the Serial ATA Specification, Revision 3.0. The PCH also supports several optional sections of the Serial ATA II: Extensions to Serial ATA 1.0 Specification, Revision 1.0 (AHCI support is required for some elements). Please see Section 1.3 for details on SKU feature availability.

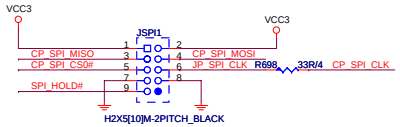
CDI / IBP #: 443554 55

RTC and CLR_CMOS



SPI DEBUG PORT

Close to SPI ROM

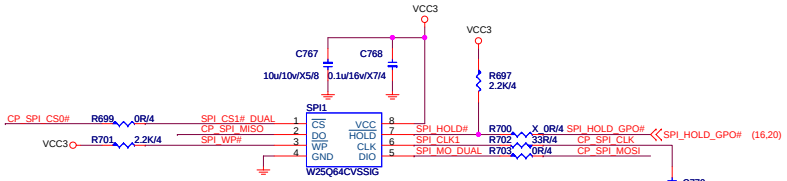


Part Number:N31-2051451-H06

SPI_FLASH_ROM

Place close to SB.

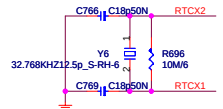
*SPI_CLK & SPI_MOSI must be length matched to within 500mils.
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.



M31-25Q6433-W03

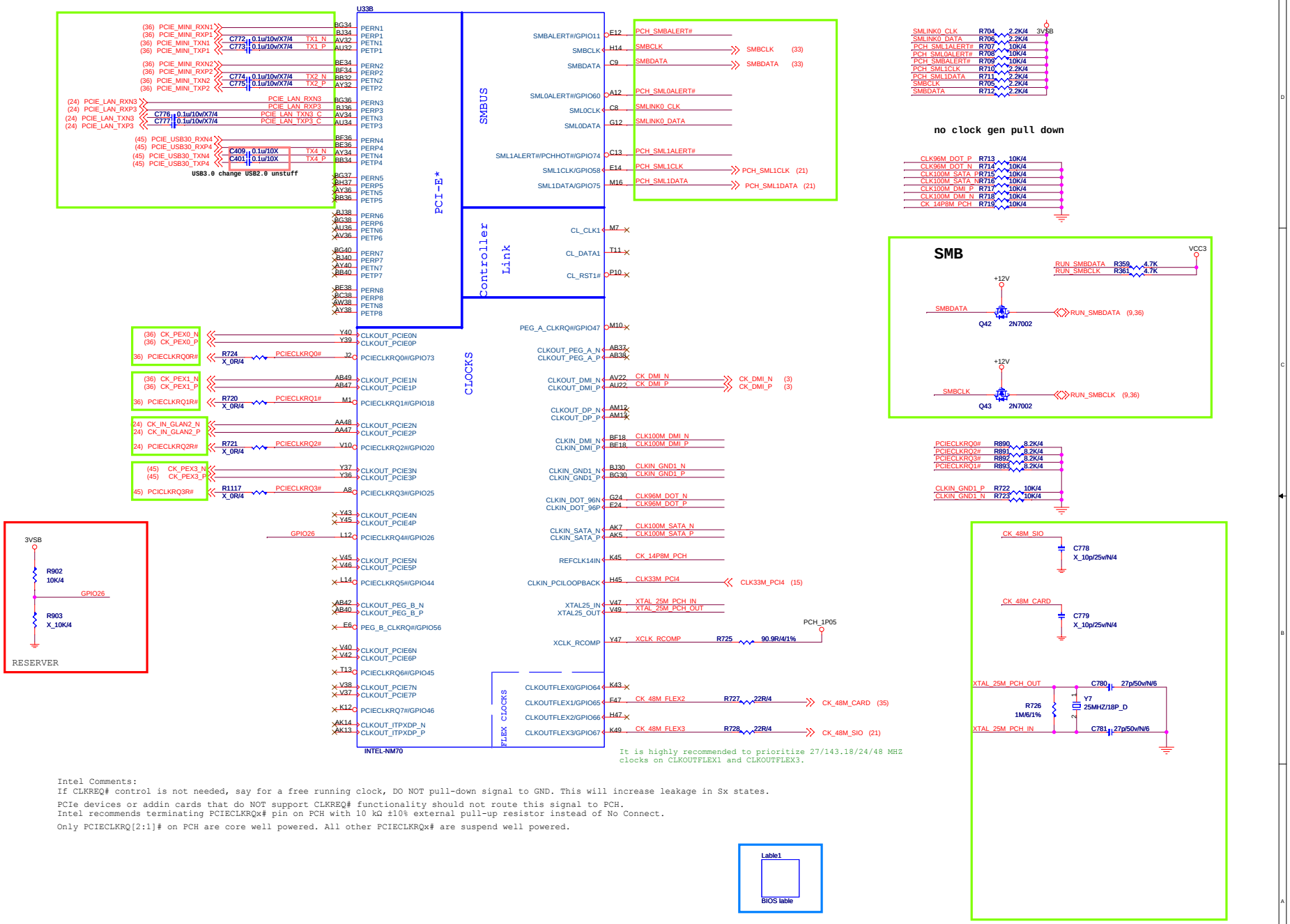
RTC Block

Close to PCH



law fix 0A Y6 DIP chage SMT

MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: PCH-1 (HDA/JTAG/SATA)	Rev: 1.0
Date: Monday, October 22, 2012	Sheet 11 of 45	

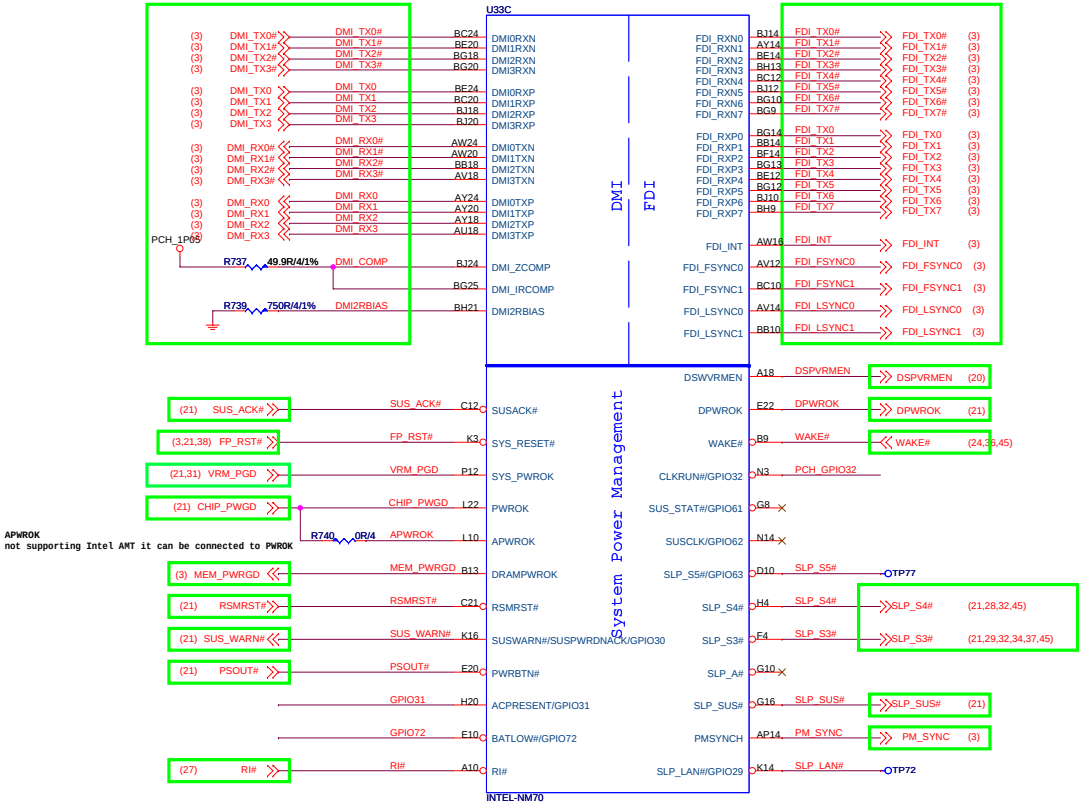


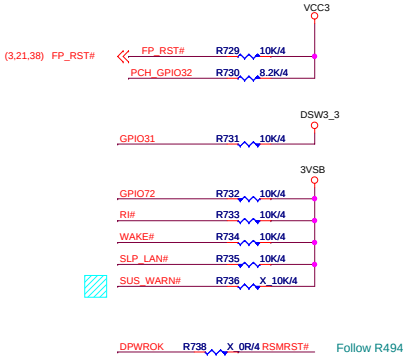
Intel Comments:
If CLKREQ# control is not needed, say for a free running clock, DO NOT pull-down signal to GND. This will increase leakage in Sx states.

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.

Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

MICRO-STAR INT'L CO.,LTD	
MS-A953	
Size: Custom	Document Description: PCH-2 (PCI-E/SMBUS/CLK)
Rev: 1.0	
Date: Thursday, November 01, 2012	Sheet 12 of 45





DPWROK	I	**DPWROK:** Power OK Indication for the VccDSW3_3 voltage rail. This input is tied together with RSMRST# on platforms that do not support Deep S4/S5. This signal is in the RTC well.

Name	Description
VccDSW3_3	3.3 V supply for Deep S4/S5 wells. If platform does not support Deep S4/S5 then tie to VccSus3_3.

Table 1-4. Mobile Intel® 6 Series Chipset SKUs

Feature Set		SKU Name				
		QM67	UM67	HM67	HM65	QS67
PCI Express* 2.0 Ports		8	8	8	8	8
PCI Interface		No	No	No	No	No
USB* 2.0 Ports		14	14	14	12[5]	14
Total number of SATA ports		6	6	6	6	6
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)		2[4]	2[4]	2[4]	2[4]	2[4]
• SATA Ports (3 Gb/s and 1.5 Gb/s only)		4	4	4	4	4
HDMI/DVI/VGA/SDVO/DisplayPort*/eDP*/LVDS		Yes	Yes	Yes	Yes	Yes
Integrated Graphics Support with PAVP 2.0		Yes	Yes	Yes	Yes	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes
	RAID 0/1/5/10 Support	Yes	No	Yes	No	Yes
Intel® Anti-Theft		Yes	Yes	Yes	Yes	Yes
Intel® AMT 7.0		Yes	No	No	No	Yes
Intel® Remote PC Assist Technology - Proactive		Yes	Yes	Yes	No	Yes
Intel® Remote PC Assist Technology- Reactive		Yes	Yes	Yes	Yes	Yes

MICRO-STAR INT'L CO.,LTD

MS-A953

Size: Custom | Document Description: PCH-3 (DMI/FDI/GPIO) | Rev: 1.0

Date: Monday, November 05, 2012 | Sheet 13 of 45

5.26.2.1.3 Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. To meet the panel power timing specification requirements two signals, LFP_VDD_EN and LFP_BKLT_EN, are provided to control the timing sequencing function of the panel and the backlight power supplies.

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

Table 5-61. Display Co-Existence Table

Display	Not Attached	DAC / VGA	Integrated LVDS	Integrated DisplayPort *	HDMI*/ DVI	eDP*
Not Attached	X	S	S	S	S	S
DAC VGA	S	X	S[1], C, E	A	A	S[1], C, E
Integrated LVDS	S	S[1], C, E	X	S[1], C, E	S[1], C, E	X
Integrated DisplayPort	S	A	S[1], C, E	A	A	S[1], C, E
HDMI/DVI	S	A	S[1], C, E	A	X	S[1], C, E
SDVO LVDS	S	S[1], C, E	X	S[1], C, E	S[1], C, E	X
eDP	S	S[1], C, E	X	S[1], C, E	S[1], C, E	X

- A = Single Pipe Single Display, Intel® Dual Display Clone (Only 24-bpp), or Extended Desktop Mode
- C = Clone Mode
- E = Extended Desktop Mode
- S = Single Pipe Single Display
- S[1] = Single Pipe Single Display With One Display Device Disabled
- X = Unsupported/Not Applicable

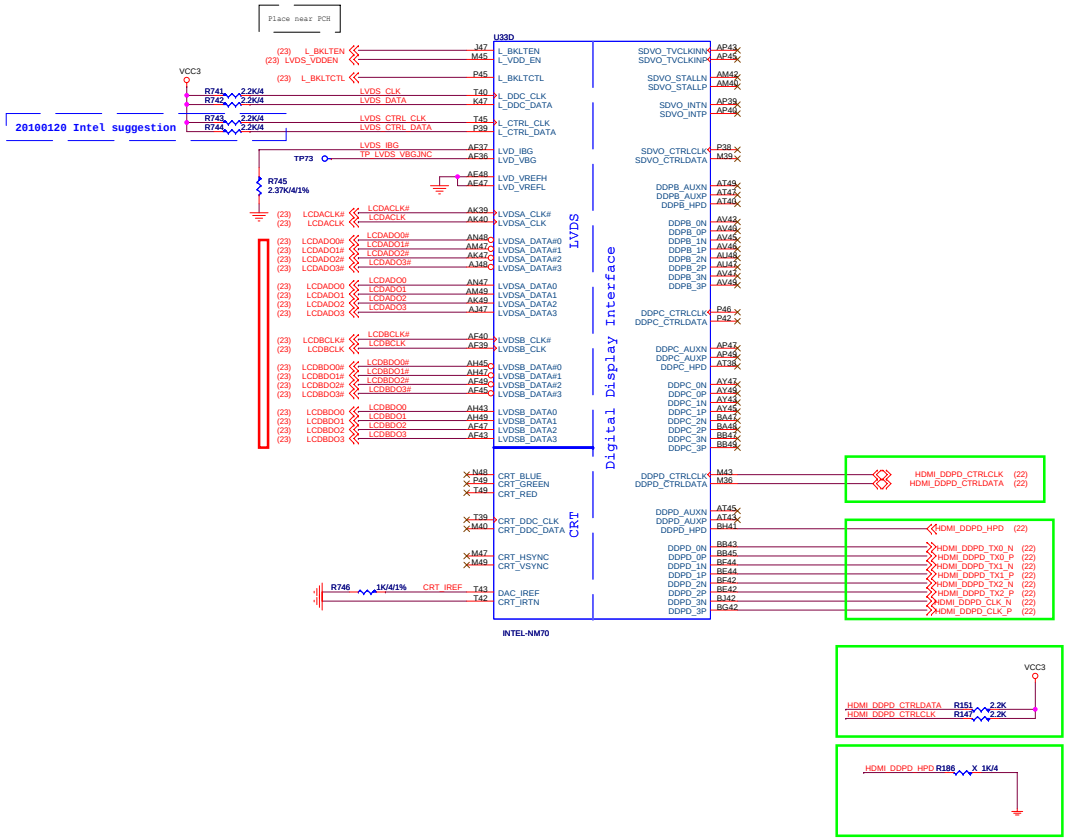


Table 2-20. LVDS Interface Signals (Sheet 1 of 2)

Name	Type	Description
LVDSA_DATA[3:0]	O	LVDS Channel A differential data output - positive
LVDSA_DATA#[3:0]	O	LVDS Channel A differential data output - negative
LVDSA_CLK	O	LVDS Channel A differential clock output - positive
LVDSA_CLK#	O	LVDS Channel A differential clock output - negative
L_DDC_CLK	I/O	EDID support for flat panel display
L_DDC_DATA	I/O	EDID support for flat panel display
L_CTRL_CLK	I/O	Control signal (clock) for external SSC clock chip control – optional
L_CTRL_DATA	I/O	Control signal (data) for external SSC clock chip control – optional

5.26.2.1.2 Single Channel versus Dual Channel Mode

In the single channel mode, only Channel-A is used. Channel-B cannot be used for single channel mode. In the dual channel mode, both Channel-A and Channel-B pins are used concurrently to drive one LVDS display.

In Single Channel mode, Channel A can take 18 bits of RGB pixel data, plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on three differential data pair outputs; or 24 bits of RGB (plus 4 bits of timing control) output on four differential data pair outputs. A dual channel interface converts 36 or 48 bits of color information plus the 3 or 4 bits of timing control respectively and outputs it on six or eight sets of differential data outputs respectively.

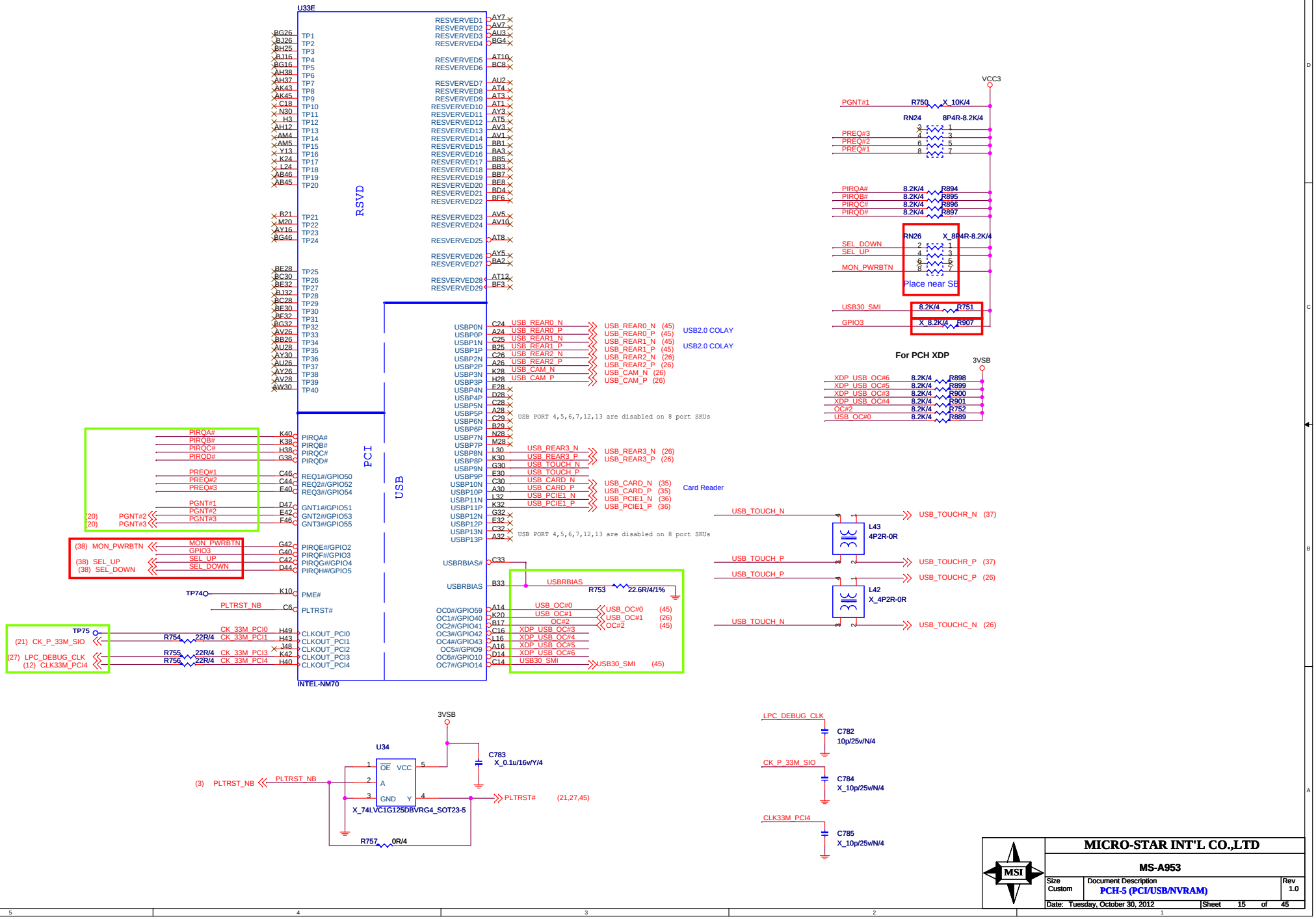
Dual Channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single channel. In general, one channel will be used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel will be sent out Channel-A. All horizontal timings for active, sync, and blank will be limited to be on two pixel boundaries in the two channel modes.

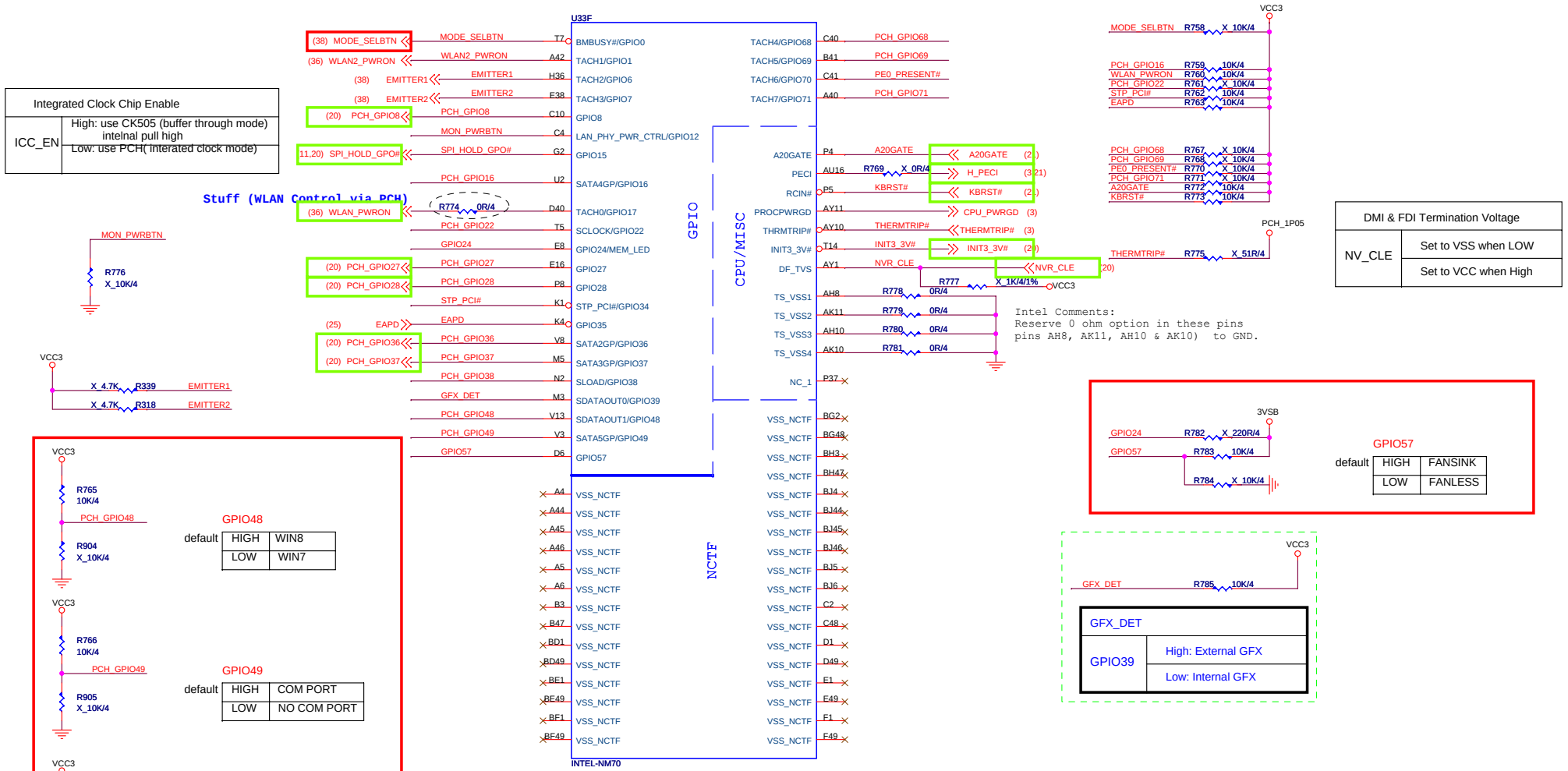
Note:
Platforms using the PCH for integrated graphics support 24-bpp display panels of Type 1 only (compatible with VESA LVDS color mapping).

1.if use MXM only LVD_IBG, LVD_VREFH and LVD_VREFL floating. VCCA_LCD and VCCTX_LVD can be connected to GND.

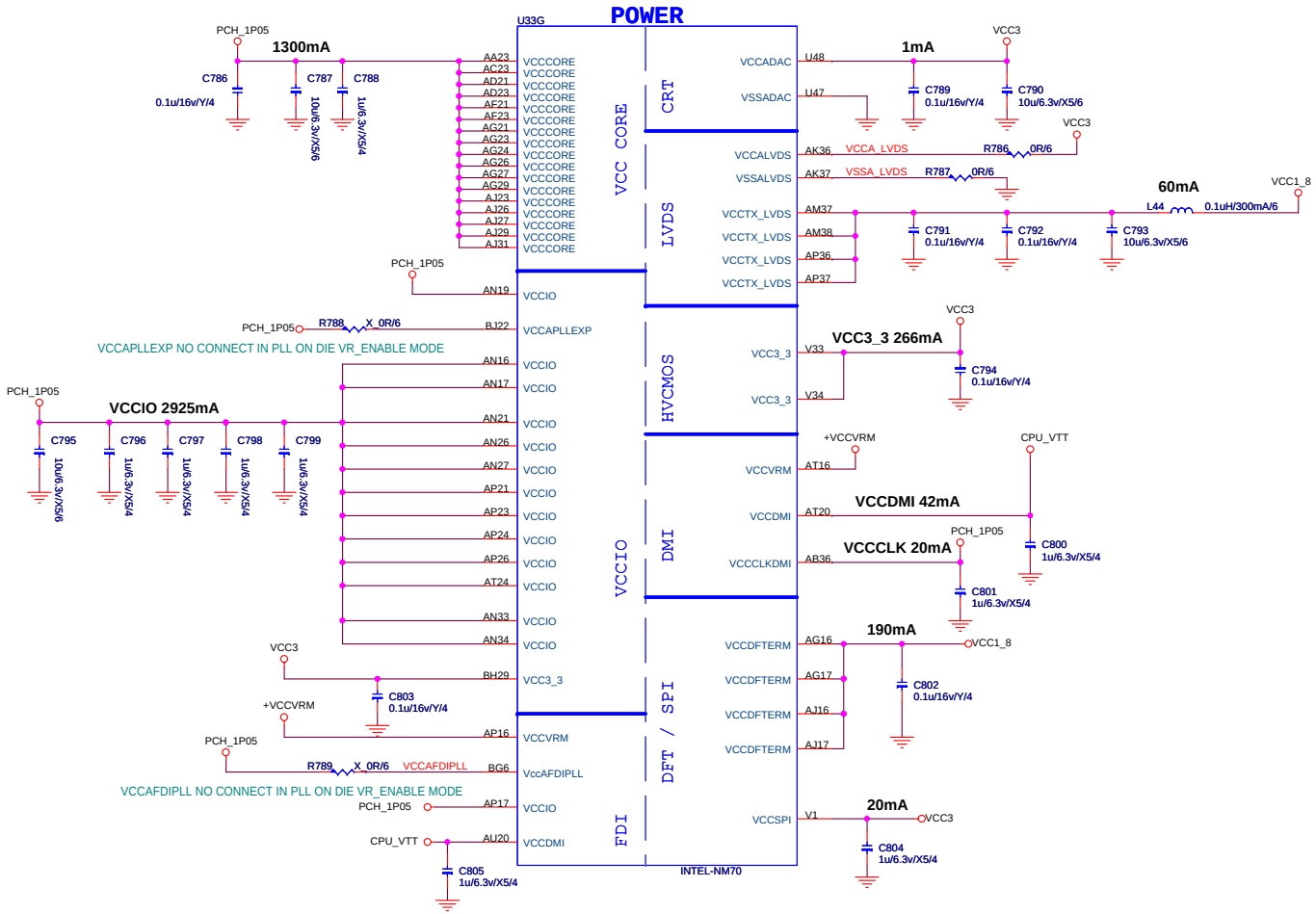
2.If use intel LVDS, LVD_IBG connect 2.37k to GND. LVD_VREFH and LVD_VREFL connect to GND. VCCA_LCD and VCCTX_LVD connect to power.

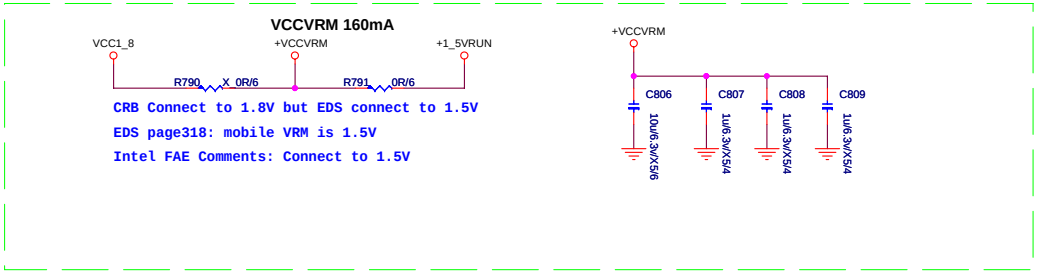
MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: PCH-4 (LVDS/DDI/VGA)	Rev: 1.0
Date: Thursday, November 01, 2012	Sheet 14 of 45	



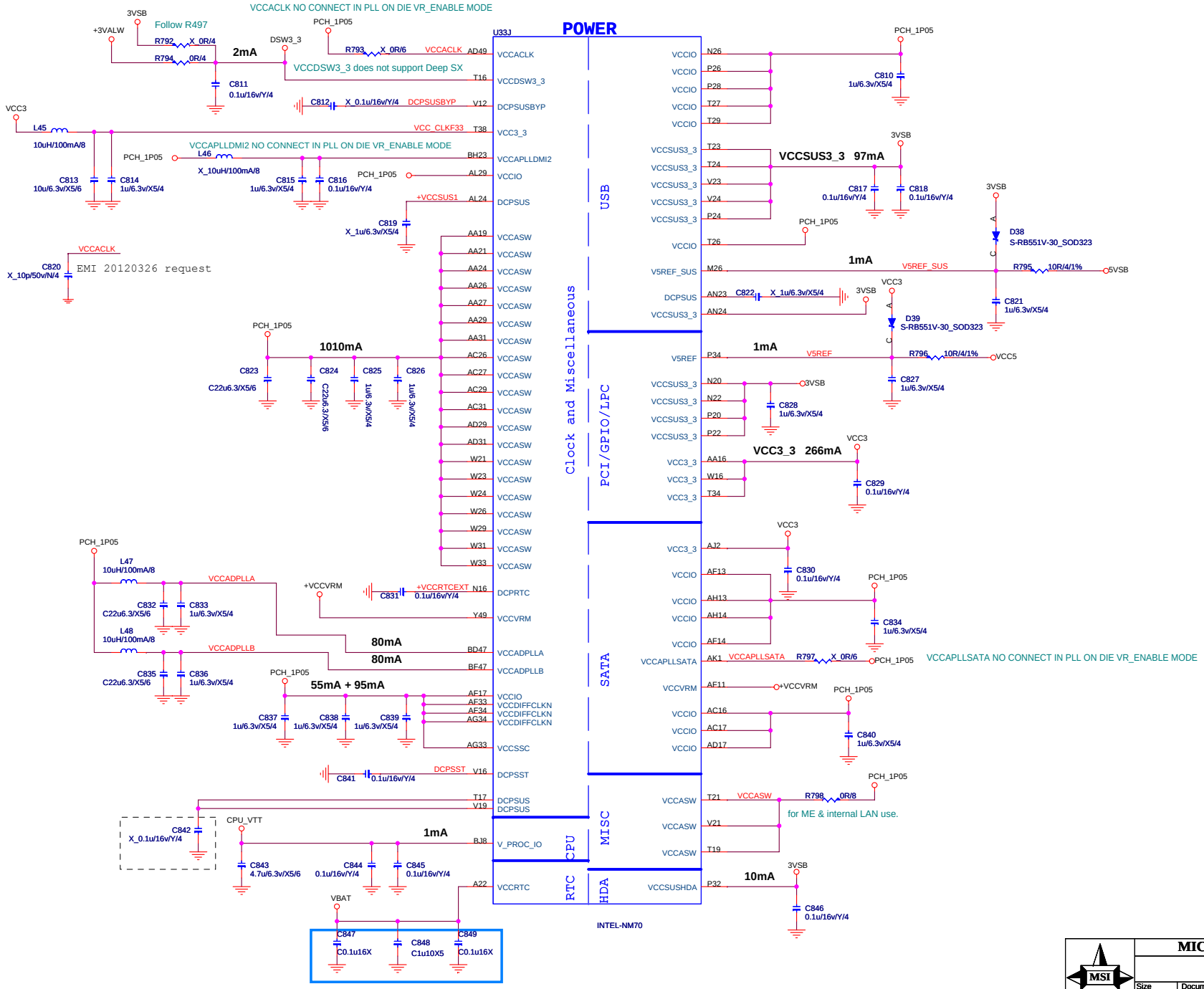


COUGAR POINT (POWER)

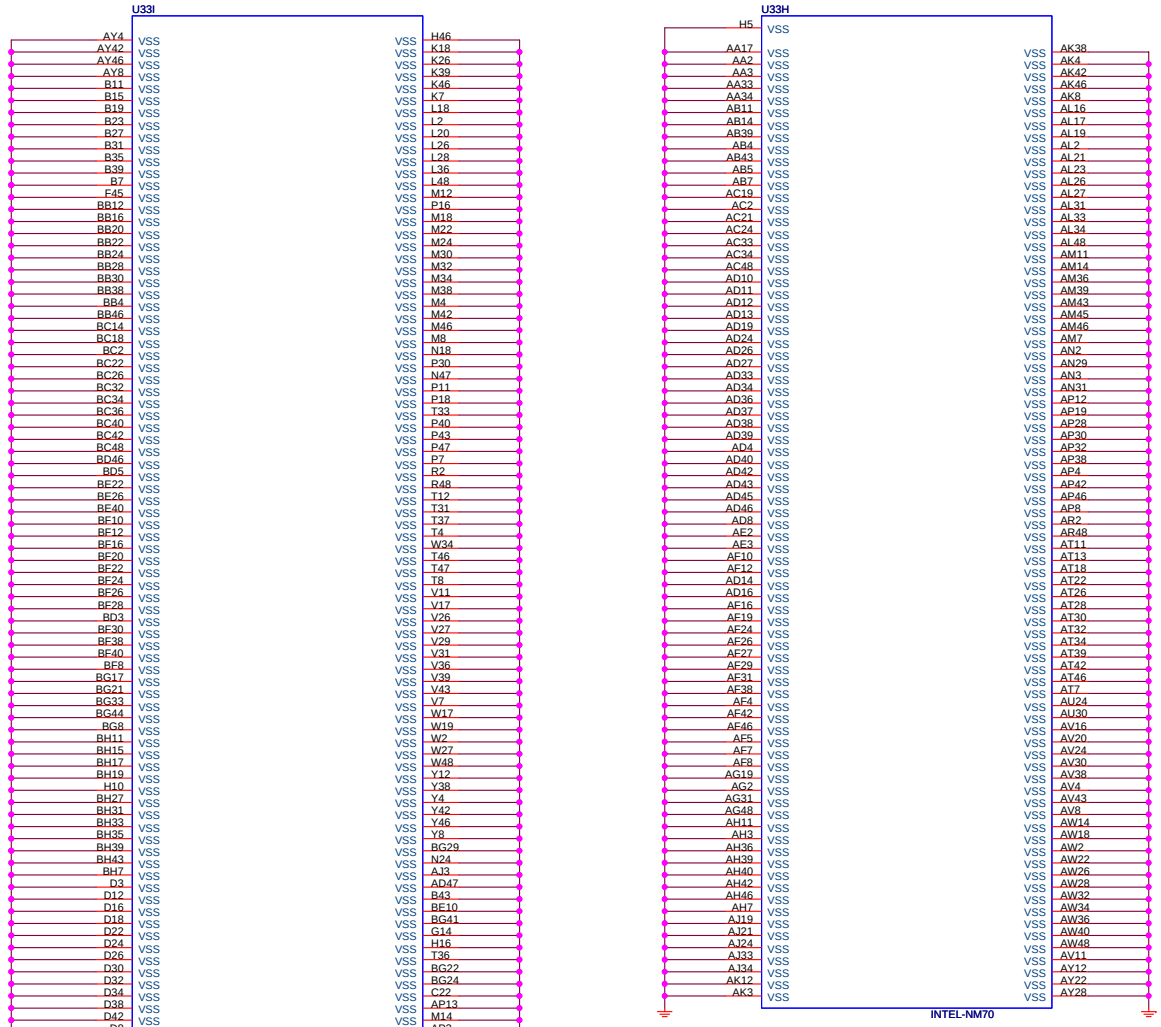




MICRO-STAR INT'L CO.,LTD	
MS-A953	
Size: Custom	Document Description: PCH-7 (POWER) — Rev: 1.0
Date: Thursday, November 01, 2012	Sheet 17 of 45



MICRO-STAR INT'L CO.,LTD	
MS-A953	
Size: Custom	Document Description: PCH-8 (POWER)
Rev: 1.0	
Date: Tuesday, October 02, 2012	Sheet 18 of 45



MICRO-STAR INT'L CO.,LTD

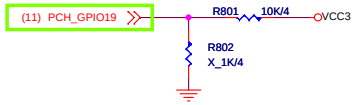
MS-A953

Size	Document Description	Rev
Custom	PCH-9 (GND)	1.0

Date: Tuesday, October 02, 2012 Sheet 19 of 45

CP REQUIRED STRAPS

BOOT DEVICE	GNT0	SATA1GP/GPIO19
LPC	0	0
PCI	0	Floating
SPI	Floating	Floating



DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

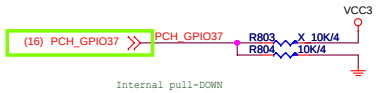
GPIO36 --CRB connector to 3V

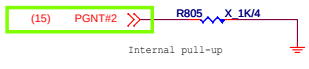
Cougar point EDS PAGE:93 This signal should not be pull high

PCH EDS1.0:GPl036&37 should not be pulled high when strap is sampled.
PCH EDS1.1:GPl036&37 when pins are unused as SATAGP or GPIO, terminate them to VSS via 8.2k-10k resistor.

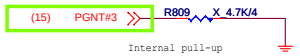
FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

Cougar point EDS PAGE:93 This signal should not be pull high

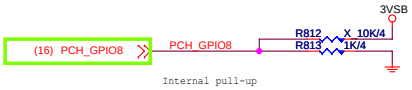




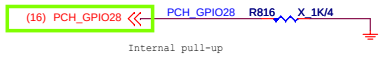
DMI AC/DC MODE
0 : AC
1 : DC *



Topblock swap override when pull-low
Signal has a weak internal pull-up

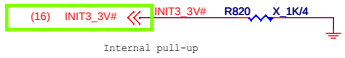


GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



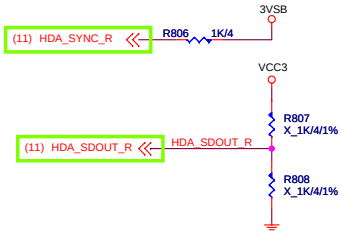
GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



INT3_3V#
0 : ????????????????
1 : ???????????????? *

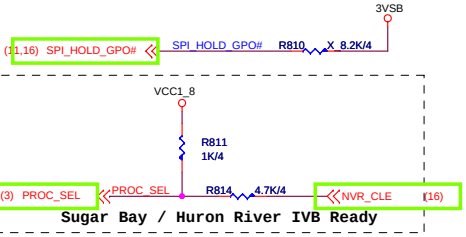
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

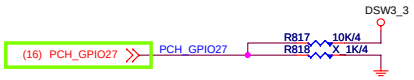


GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

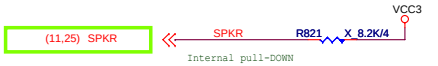


In Deep Sleep Power Well.

If not used,require a weak pull-up(8.2k~10k) to VccDSW3_3

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

MICRO-STAR INT'L CO.,LTD

MS-A953

Size	Document Description	Rev
Custom	PCH-10 (STRAPS)	1.0
Date: Monday, October 22, 2012	Sheet 20 of 45	

COLAY F71869 F71878

B02-7187804-F34 F71878AD

OPT PANEL

J9 OPT PANEL	
1 - 2	Samsung *
2 - 3	CHI MEI

X_N31-1030171+N33-1020301-RH

ATXPG is better to reflect the fastest falling power source (eg: 12V/5VSB/5VCC…) in adapter application under AC lose situation.

HW Monitor - Thermal

CPU Socket — S/IO — MOS Q4

Q26 P-PMBS3906_SOT23-RH

Q25 P-PMBS3906_SOT23-RH

Voltage Sensing

F71869AD

F71878AD-RH

LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT	Enable 80 Port	Disable 80 Port
RTSA#		

Reserver for leak current issue.

COLAY F71878AD.

F71878AD stuff.

AA5F	F71869AD	CFG-A953_U3
AA73	F71878AD	CFG-A953_U2

SIO7

F71869AD-LAD

B02-7186924-F34

F71869AD-LAD

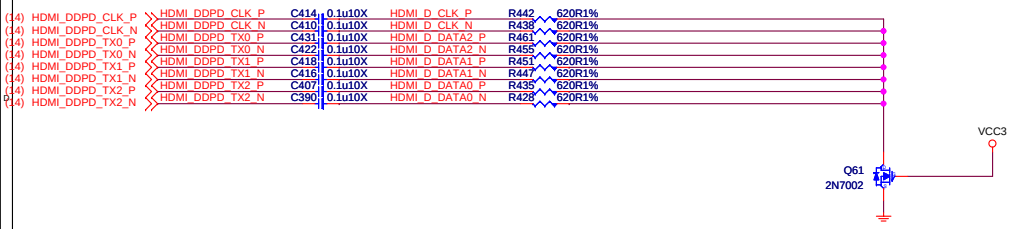
MICRO-STAR INT'L CO.,LTD

MS-A953

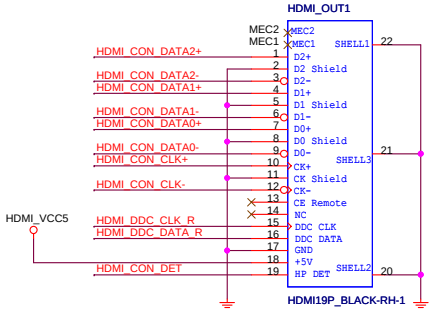
SIO-Fintek F71868AD

Size: Custom | Rev: 1.0 | Date: Monday, November 05, 2012 | Sheet 21 of 45

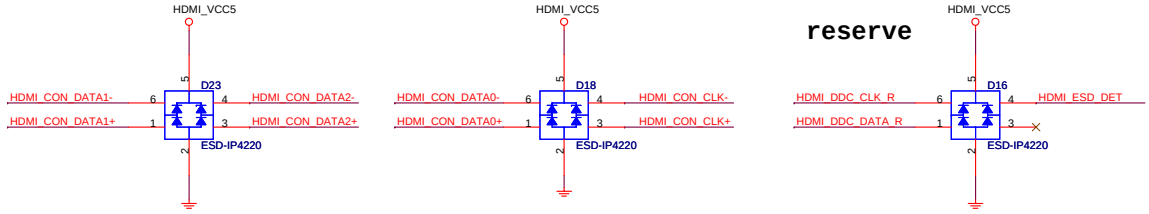
HDMI



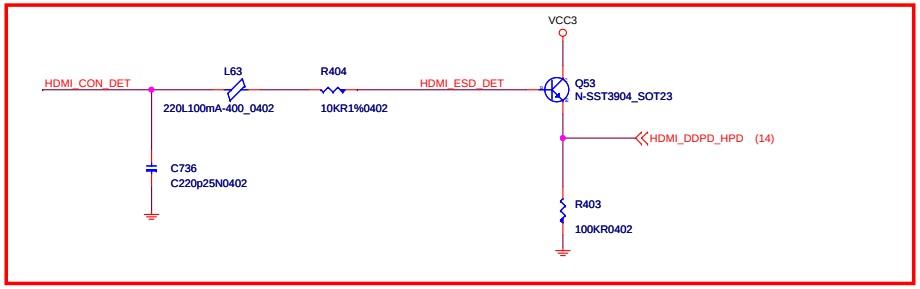
Signal Name	Description	Direction	Type
DDI0_TXP[3:0], DDI0_TXN[3:0]	PORT0: Capable of HDMI/DVI/DP HDMI/DVI: _TX[0]: TMDSB_DATA2 _TX[1]: TMDSB_DATA1 _TX[2]: TMDSB_DATA0 _TX[3]: TMDSB_BLK DP: _TX[0]: DPort Lane 0 (BLUE, HSYNC, VSYNC) _TX[1]: DPort Lane 1 (GRN, CTL0, CTL1) _TX[2]: DPort Lane 2 (RED, CTL2, CTL3) _TX[3]: DPort Lane 3	O	Diff

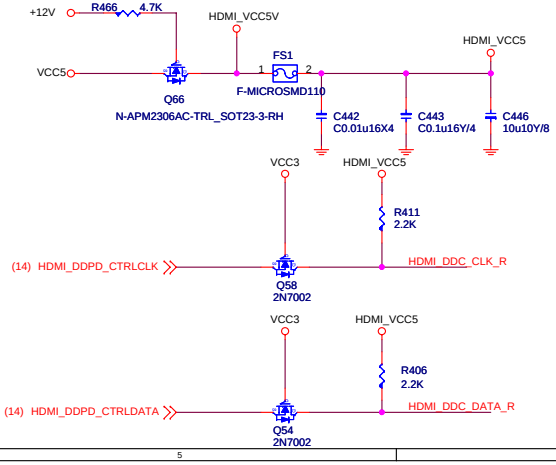


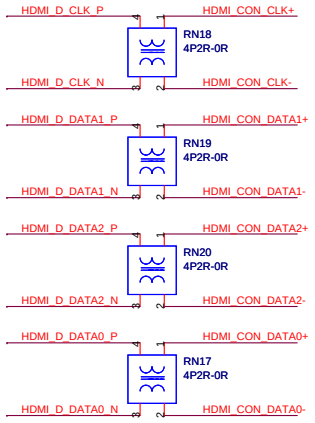
N5Y-19M0221-H06

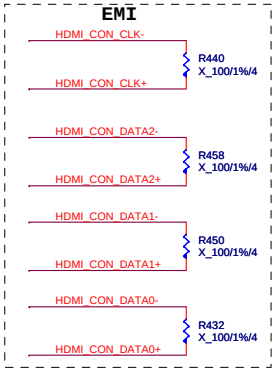


reserve









MICRO-STAR INT'L CO.,LTD

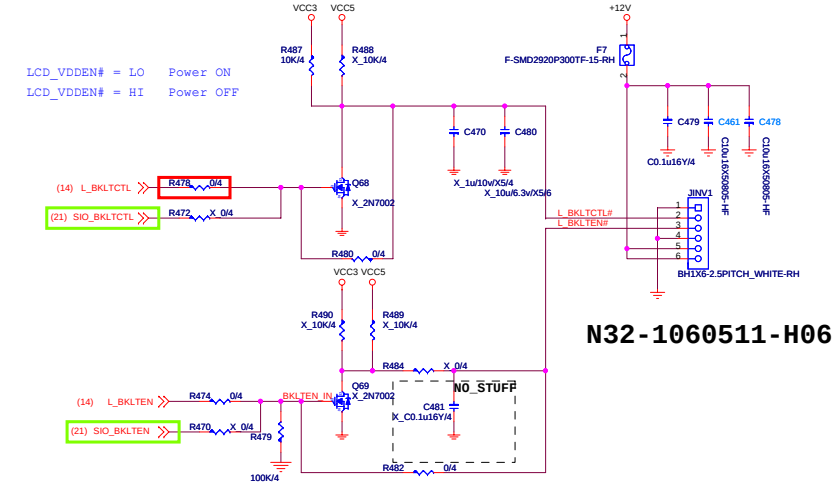
MS-A953

Size	Document Description	Rev
Custom	HDMI	1.0

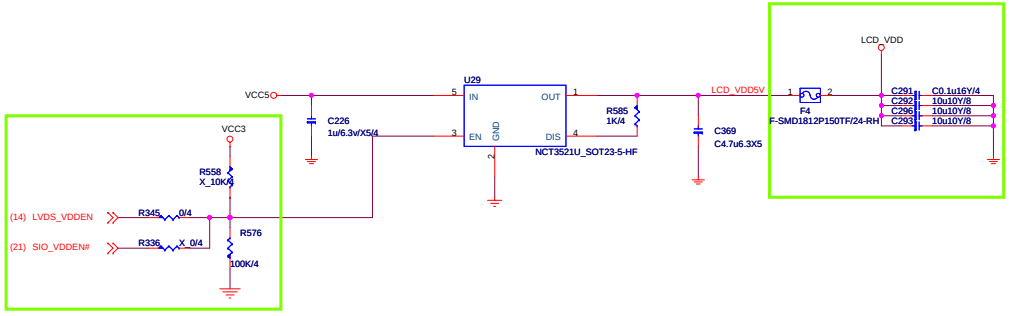
Date: Monday, November 05, 2012 Sheet 22 of 45

VGA

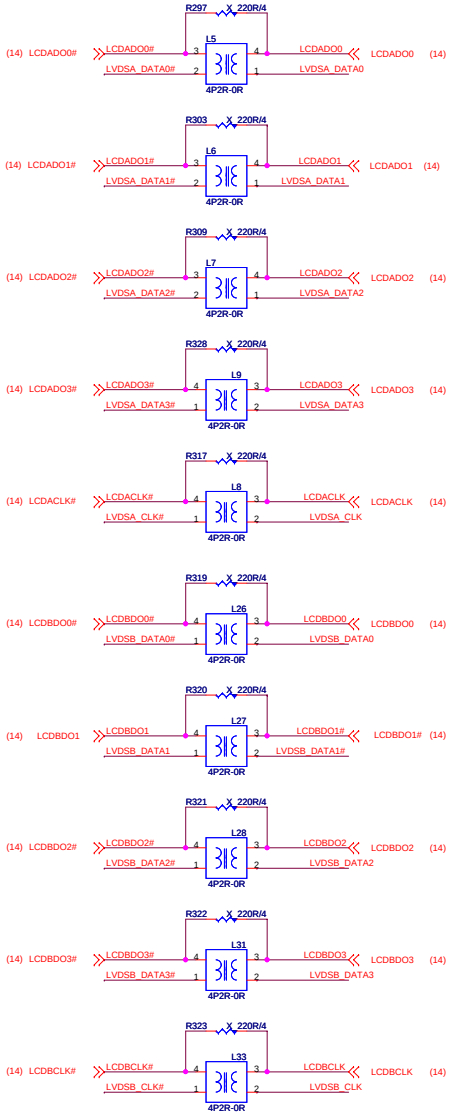
LVDS

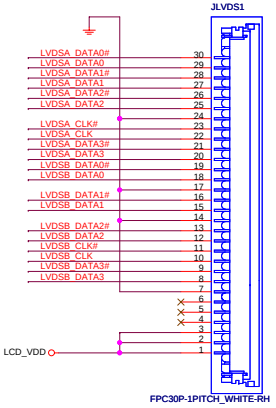


N32-1060511-H06



N5A-30F0120-H06

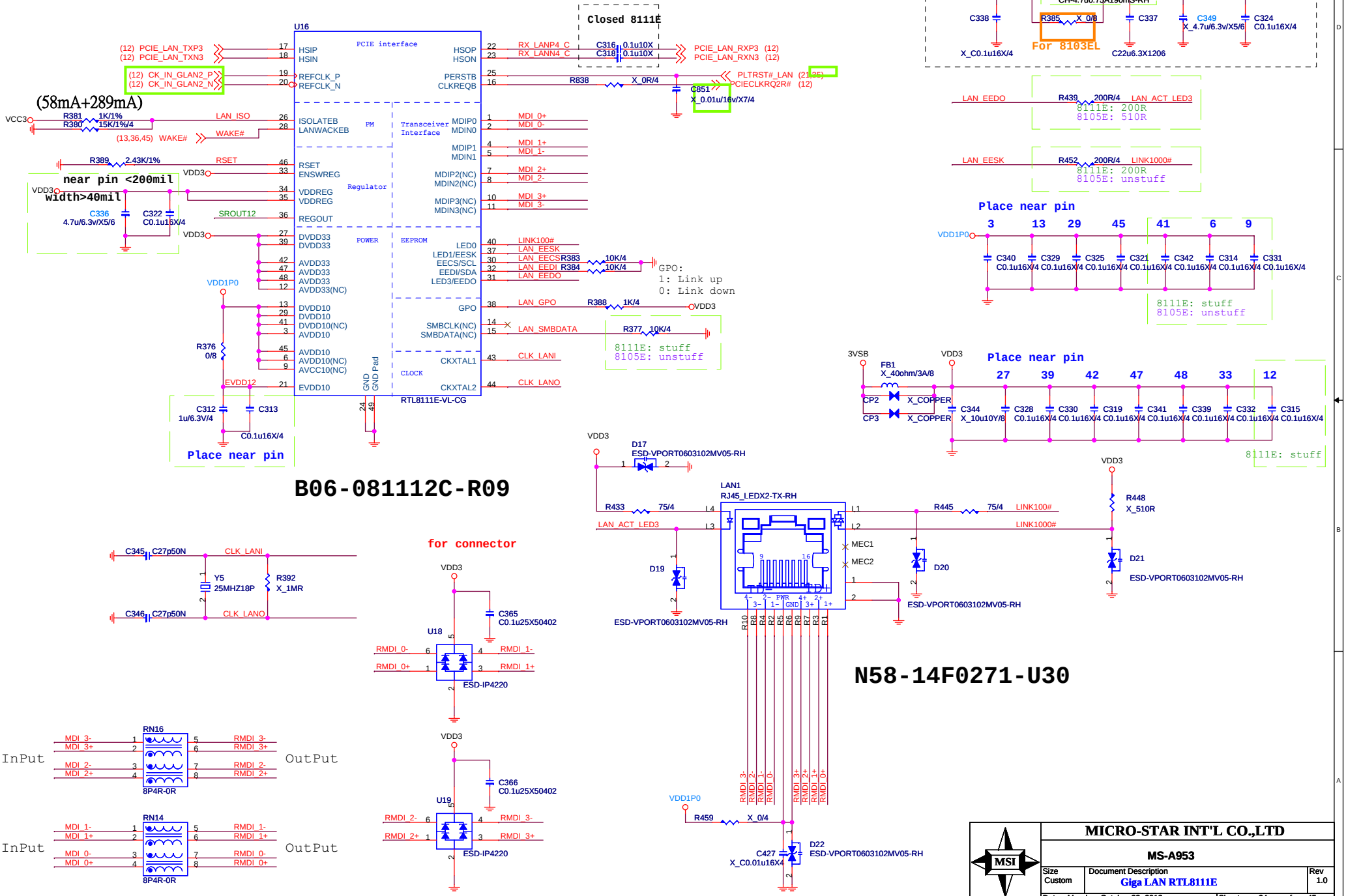


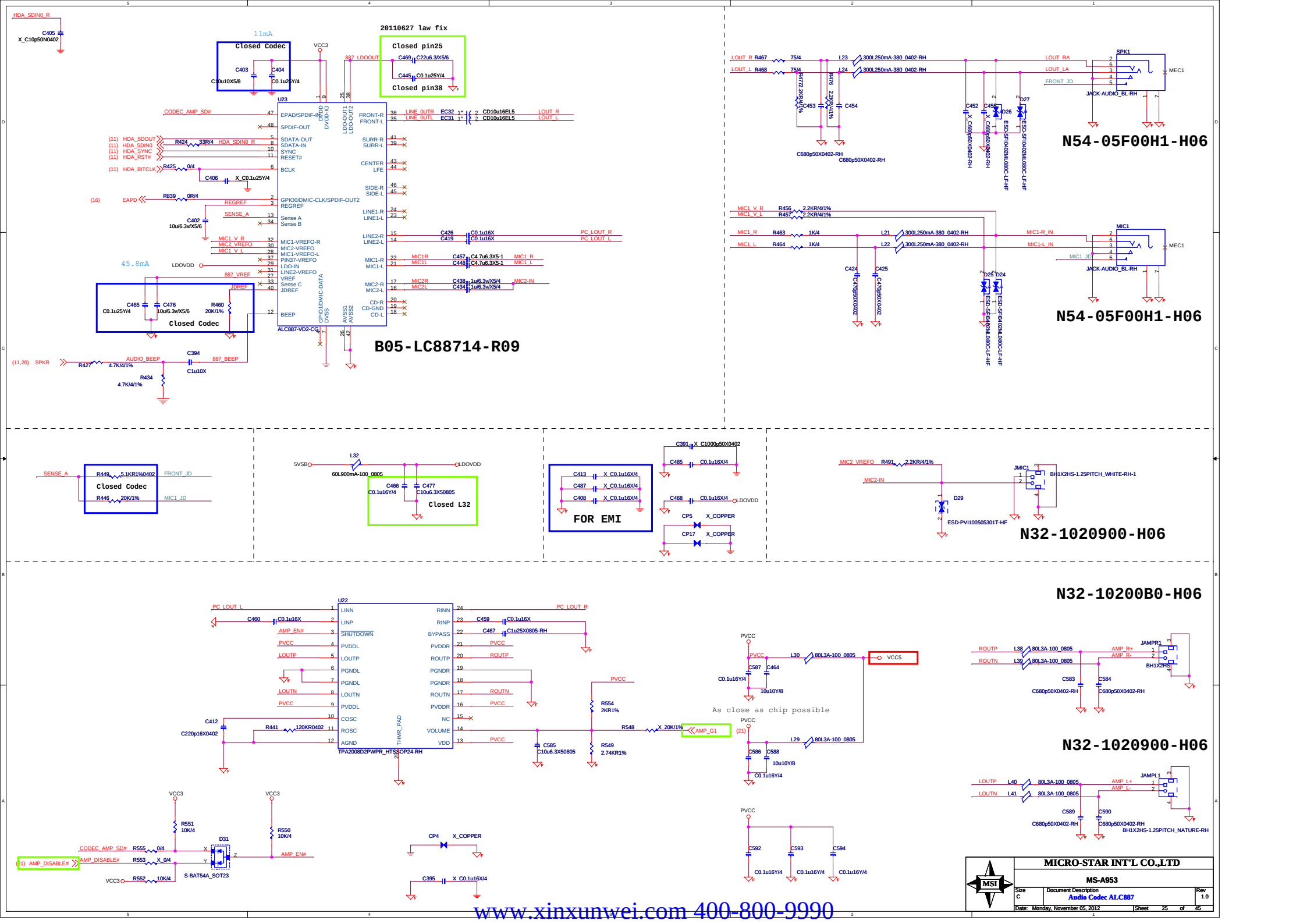


MICRO-STAR INT'L CO.,LTD	
MS-A953	
Size: Custom	Document Description: VGA / LVDS
Rev: 1.0	
Date: Friday, October 26, 2012	Sheet 23 of 45

RTL8111E Giga LAN

RTL8105E 10/100M LAN

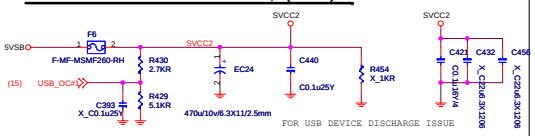




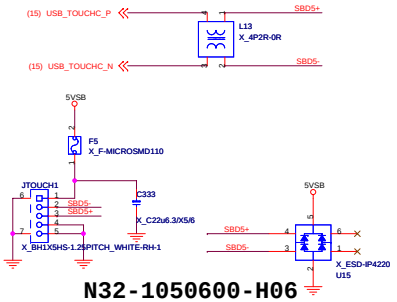
POWER CIRCUIT FOR USB PORT 0,1 (REAR)

DEL USB2.0 POWER

POWER CIRCUIT FOR USB PORT 2,3 (REAR)

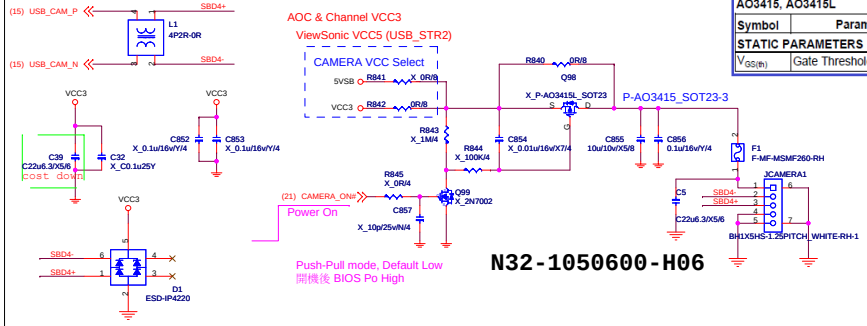


Multi Touch



N32-1050600-H06

Webcam



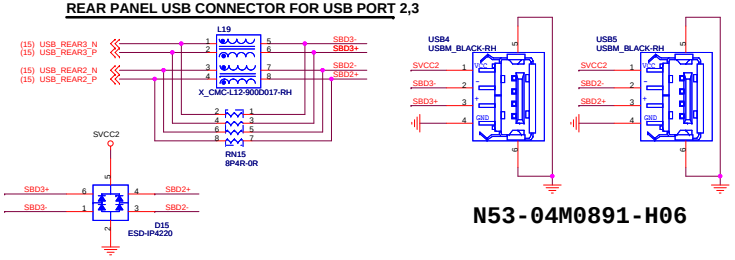
N32-1050600-H06

AO3415, AO3415L						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=-250µA	-0.3	-0.55	-1	

REAR PANEL USB CONNECTOR FOR USB PORT 0,1

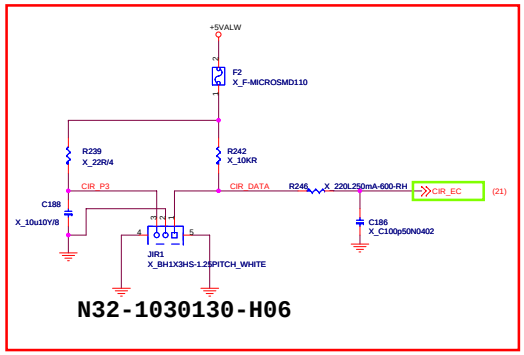
creative USB3.0 COLAY 2.0(P45) , DEL USB2.0

REAR PANEL USB CONNECTOR FOR USB PORT 2,3



N53-04M0891-H06

IR



N32-1030130-H06

AA5F	stuff	CFG-A953_U3
AA73	unstuff	CFG-A953_U2

F71878 NO IR

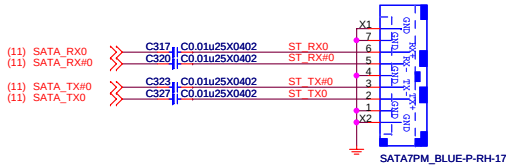
MICRO-STAR INT'L CO.,LTD

MS-A953

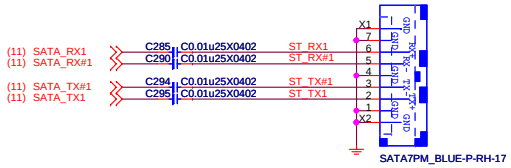
Size: Custom | Document Description: USB / IR / TOUCH / WEBCAM | Rev: 1.0

Date: Monday, November 05, 2012 | Sheet 26 of 45

SATA HDD

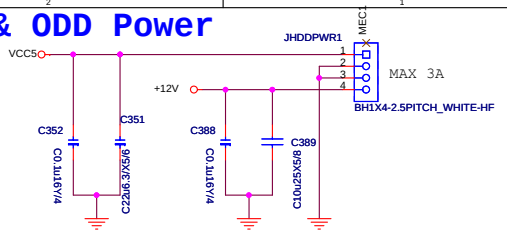


SATA 0DD



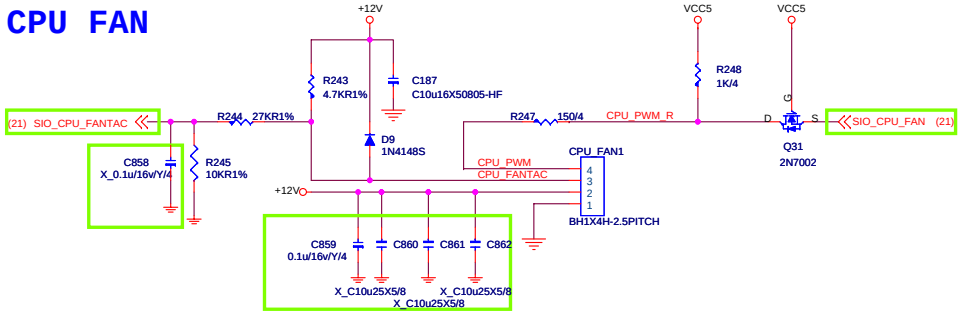
N5N-07M2101-H06 blue

HDD & ODD Power

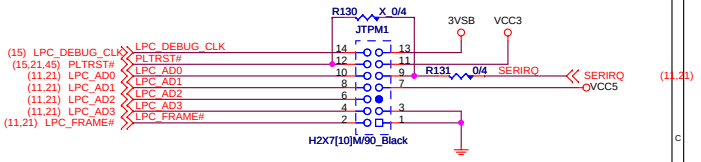


N32-1040901-H06

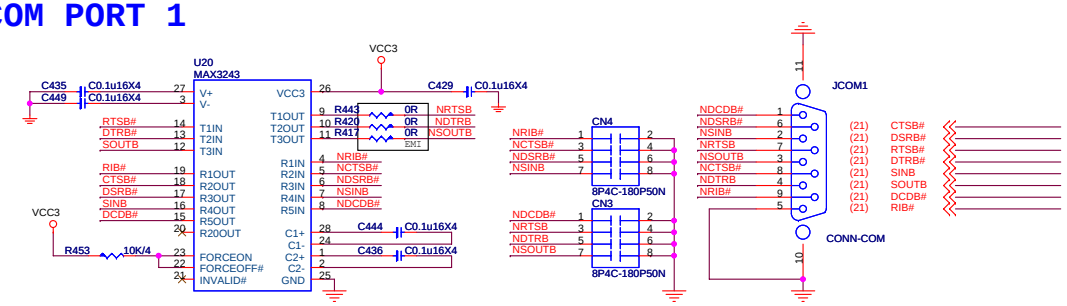
CPU FAN



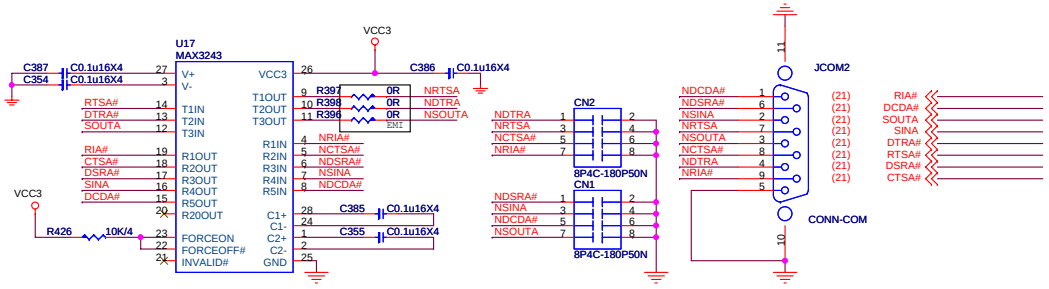
TPM HEADER



COM PORT 1

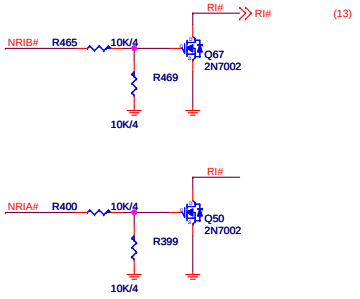


COM PORT 2



AA5F	unstuff	CFG-A953_U3
AA73	stuff	CFG-A953_U2

WAKE ON RING



AA5F	unstuff	CFG-A953_U3
AA73	stuff	CFG-A953_U2

MICRO-STAR INT'L CO.,LTD

MS-A953

Size	Document Description	Rev
Custom	SATA /FAN Control	1.0

Date: Monday, November 05, 2012 Sheet 27 of 45

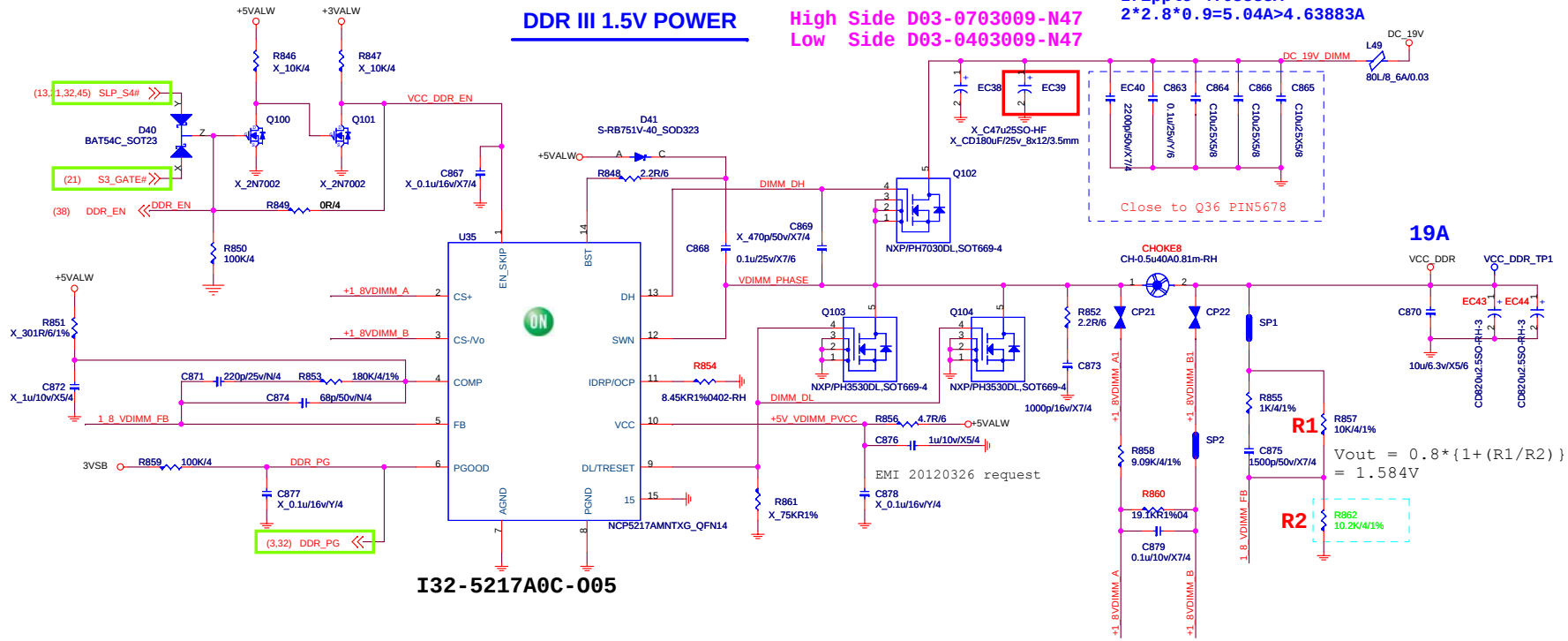
VCC_DDR

VCC_DDR
Current Max at 20A
DDR_VTT: 1.2A
+1.5VRUN: 6A
DDR3 x1 : 4A
PCH_1P05: 8.16A

DDR III 1.5V POWER

High Side D03-0703009-N47
Low Side D03-0403009-N47

Iripple=4.63883A
2*2.8*0.9=5.04A>4.63883A

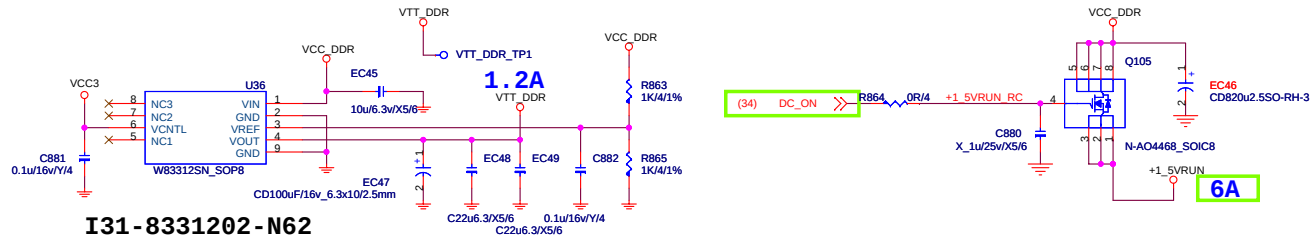


I32-5217A0C-005

Close to PWM(NCP5217A)

VTT_DDR

VTT_DDR
Current Max at 1.2A



I31-8331202-N62

MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: Memory Power(NCP5217)	Rev: 1.0
Date: Thursday, November 01, 2012	Sheet 28 of 45	

CPU_SA Power

VTT-->CPU_SA

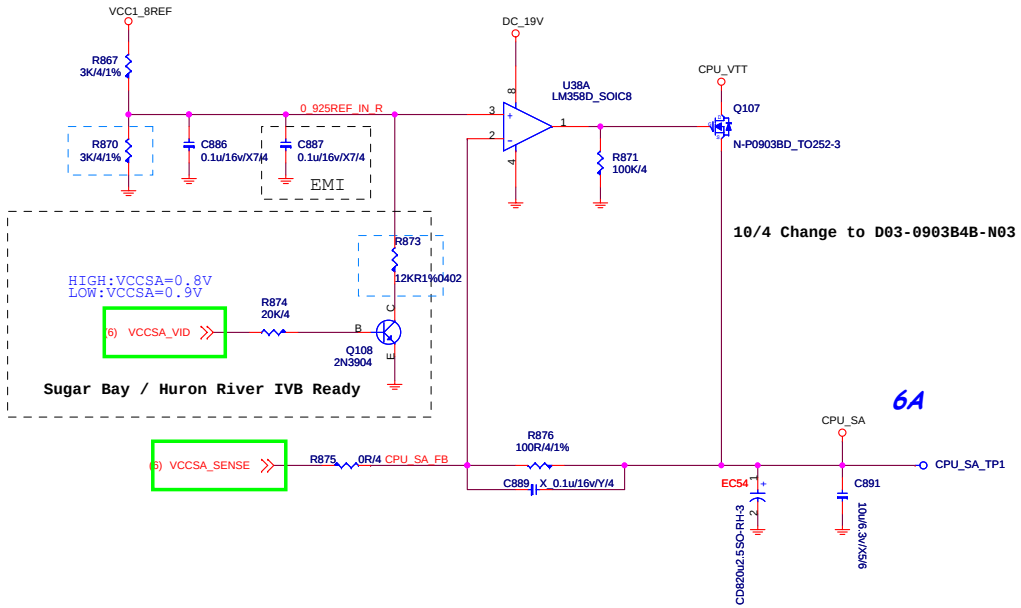
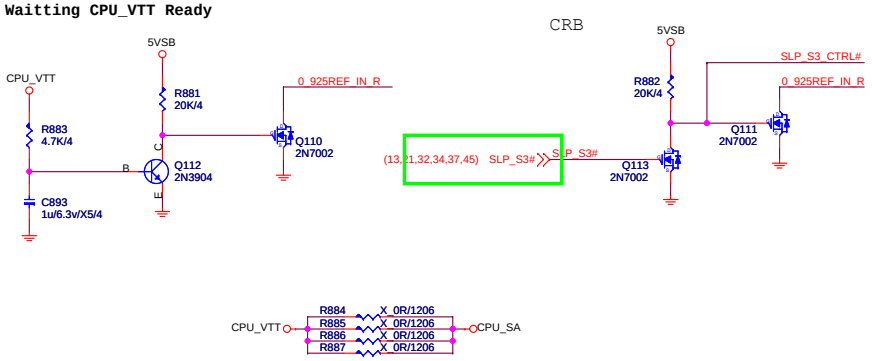


Table 3-10. VCCSA Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	1	7mΩ	1.4nH	Output	As close to RM keep-out as possible	1
10µF 0805 X5R	2	3mΩ	0.51nH	Output	Inside processor socket cavity	1,2,3

Waitting CPU_VTT Ready



CP Power

DDR-->PCH

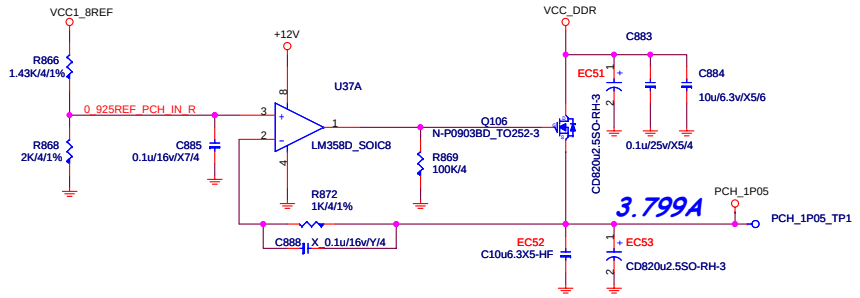
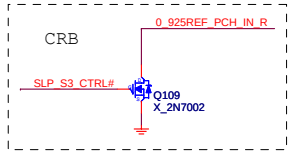
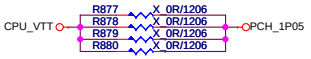


Table 4-1. V1.05A_PCH Plane Decoupling Recommendations

Bulk Decoupling Location	Qty x µF (size)	ESR, m
1.05S rail for VccCore & VccIO (dedicated)(AMT sku)	1x820uF	21mohm (bulk)
1.05A rail for VccASW (dedicated)(AMT sku)	2x22uF MLCC	
1.05S rail merge with 1.05A rail (non- AMT sku)	1x560uF 2x 22uF MLCC	7mohm (bulk)

Note: Bulk electrolytic capacitors (tantalum or aluminum based) render an aggregate ESR that matches the motherboard impedance budget. Other electrolytic capacitors that render motherboard impedance match can be deemed suitable as long as ripple current ratings and attach rate renders Bulk ESR not significantly different that those shown.





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-A953	
Size: Custom	Document Description: CP /CPU_SA POWER	Rev: 1.0
Date: Thursday, November 01, 2012	Sheet 29 of 45	

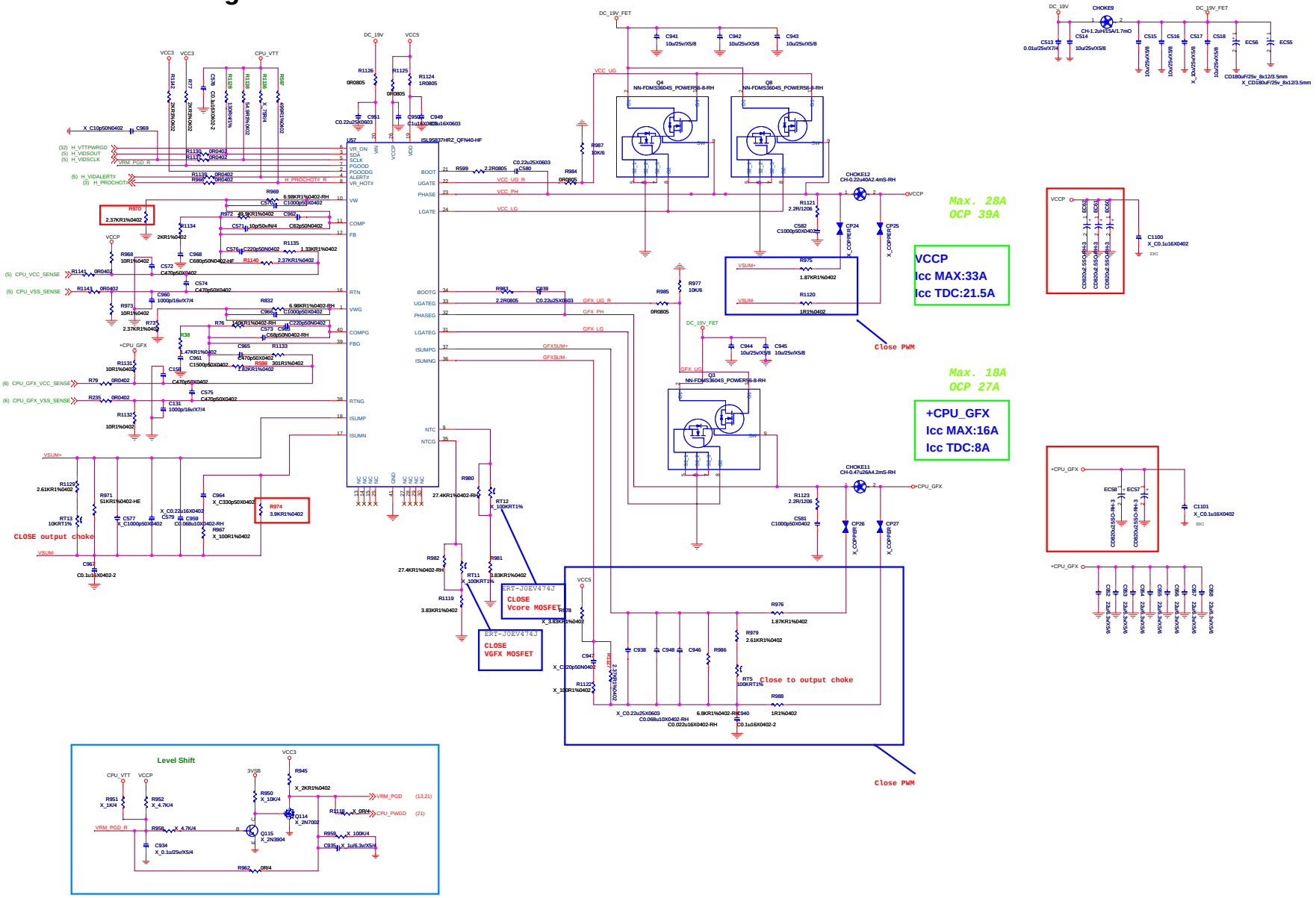
MICRO-STAR INT'L CO.,LTD

MS-A953

Size	Document Description	Rev
Custom	CPU CORE-1(NCP6151)	1.0

Date: Tuesday, October 02, 2012 | Sheet 30 of 45

ISL95837 Single Phase For VR12 solution

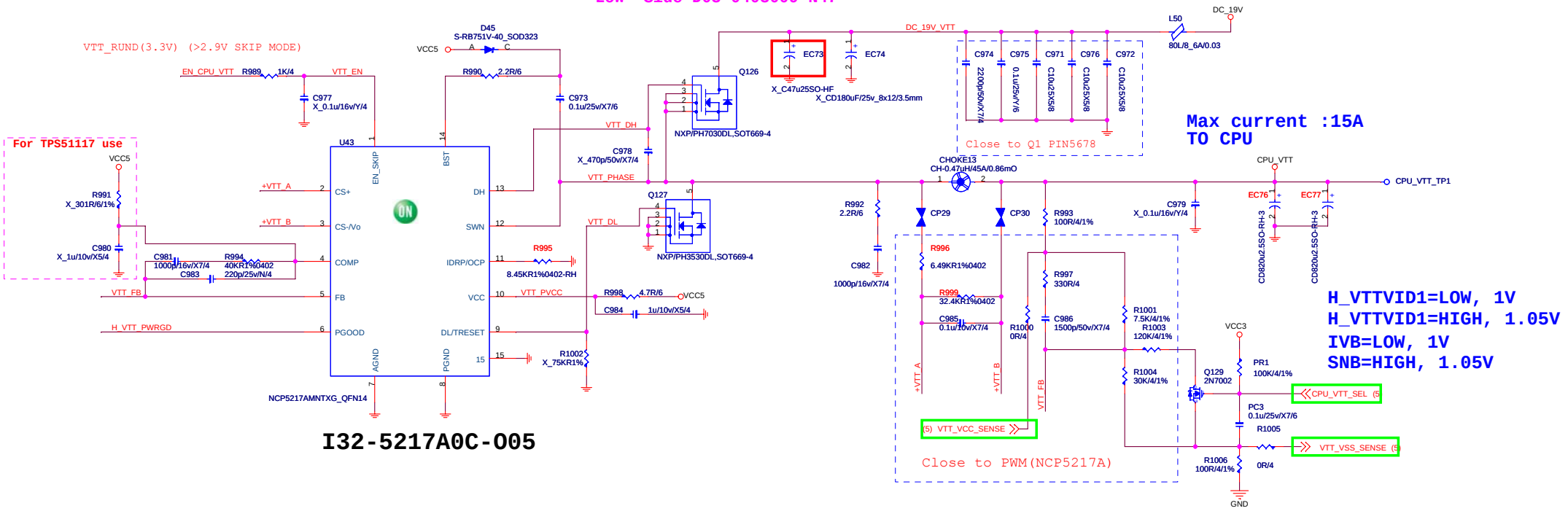


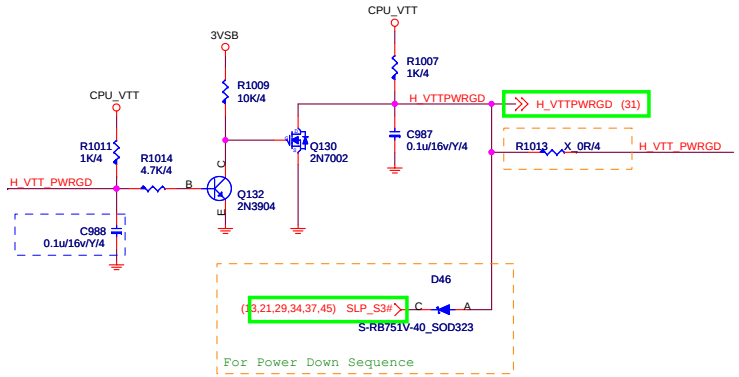
CPU_VTT

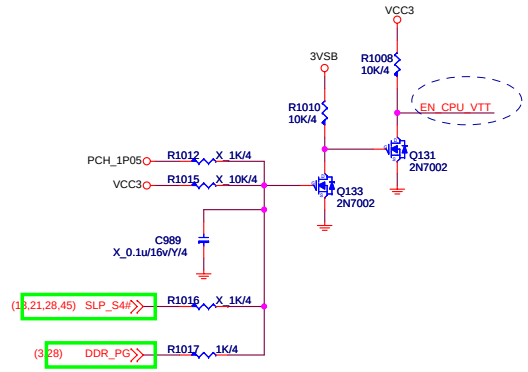
Current Max at 15A
VCCIO: 8.5A
CPU_SA : 6A

High Side D03-0703009-N47
Low Side D03-0403009-N47

Iripple=4.38707A
2*2.8*0.9=5.04A>4.38707A







1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA

If DCR = 1m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K

2. Csen = L/Rocset*DCR

If DCR = 1m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

Table 3-6. VCCIO Decoupling Requirements

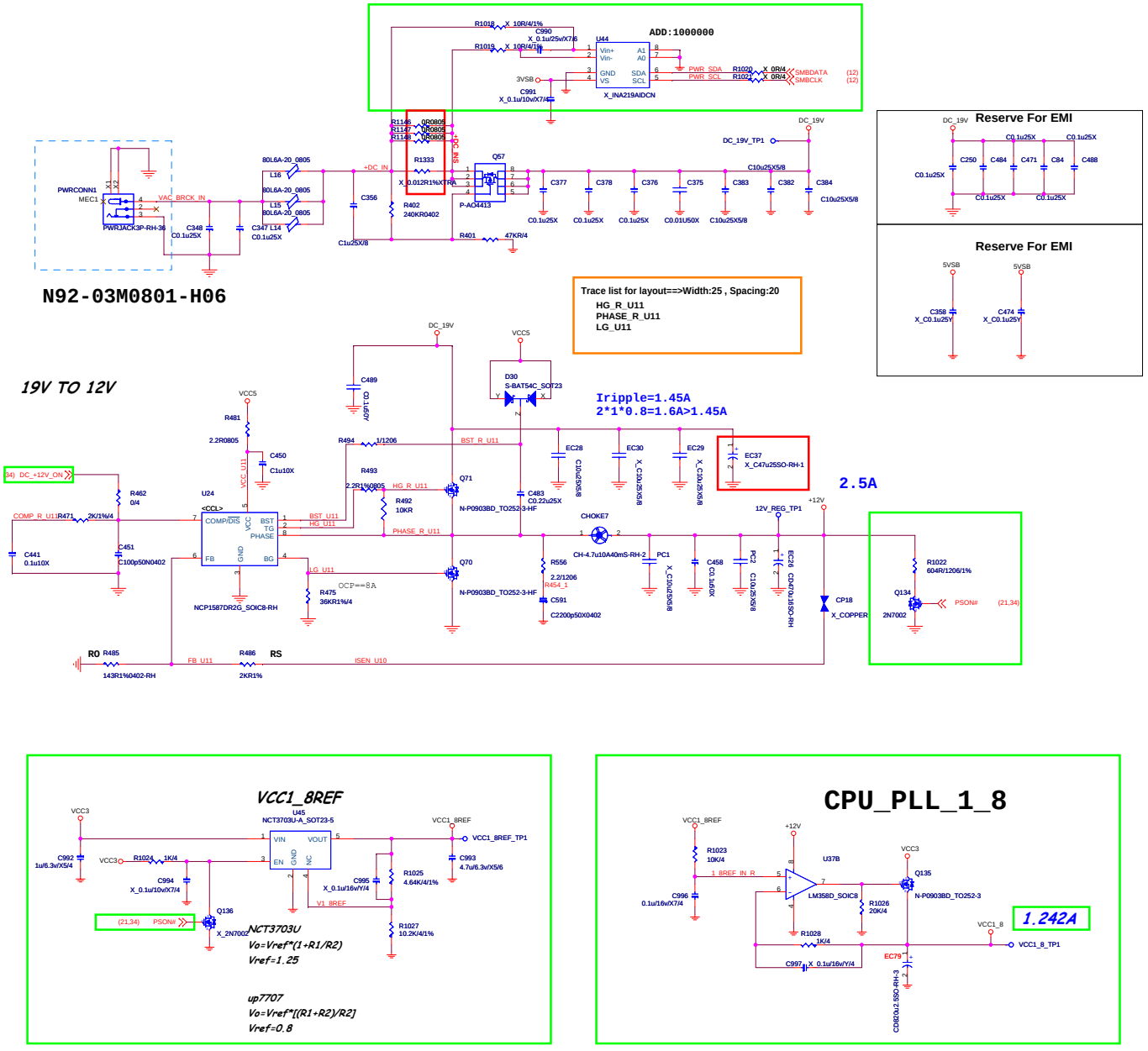
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	

MICRO-STAR INT'L CO.,LTD

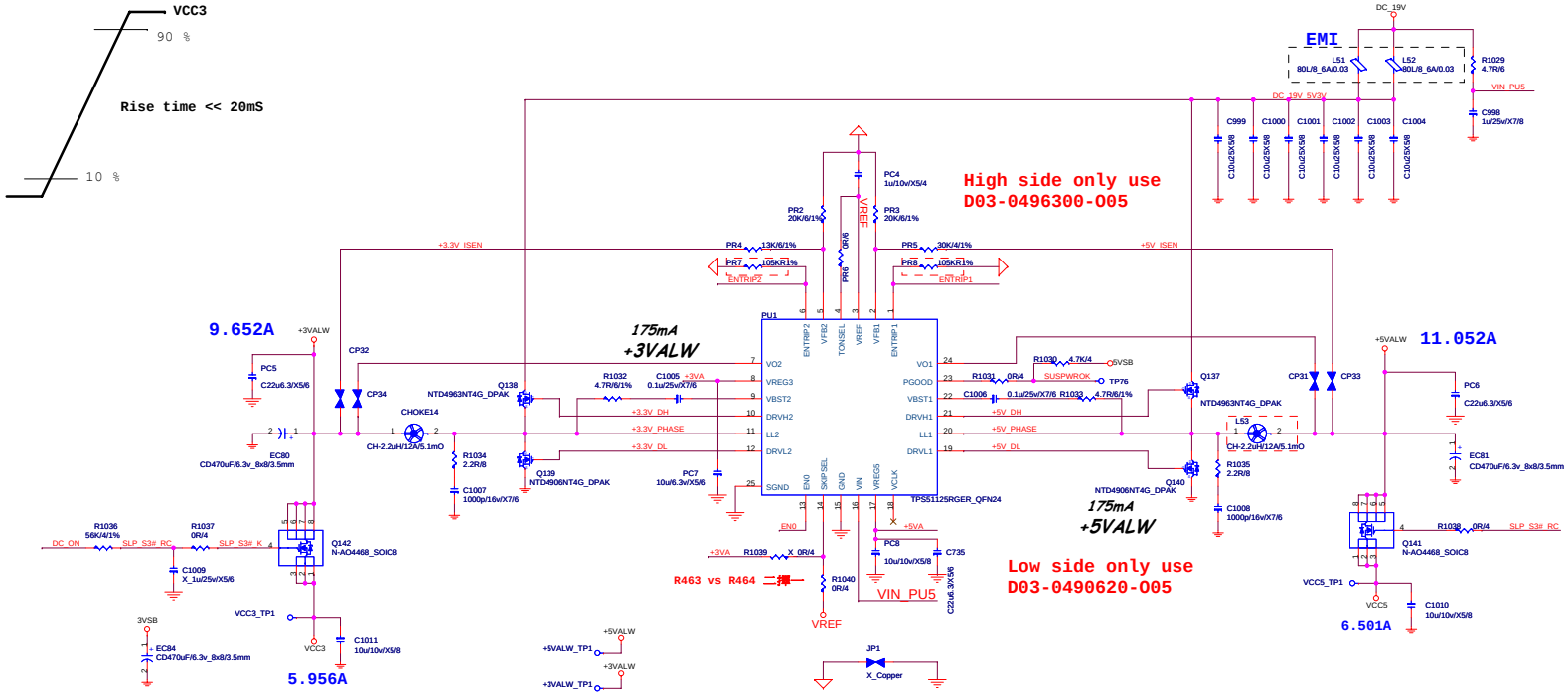
MS-A953

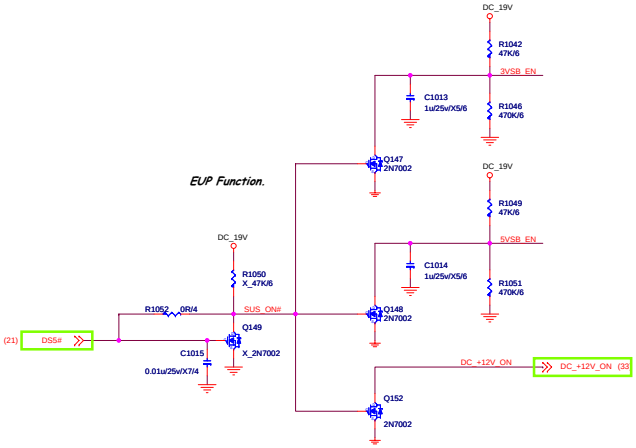
Size: Custom | Document Description: CPU_VTT - NCP5217AMNTXG- 1-Phase | Rev: 1.0

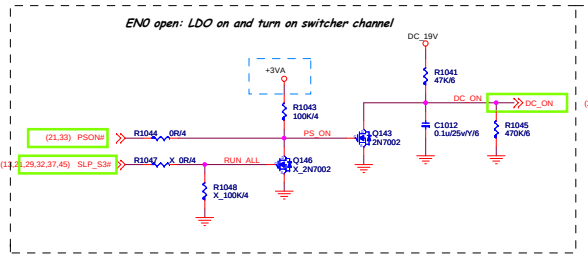
Date: Thursday, November 01, 2012 | Sheet 32 of 45

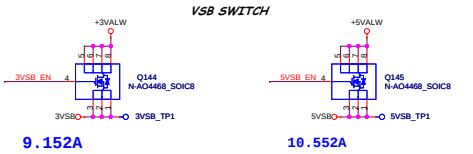


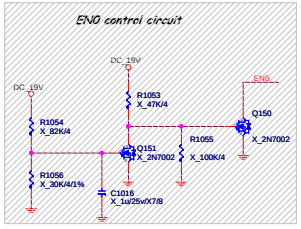
MSI	MICRO-STAR INT'L CO.,LTD		
	MS-A953		
Size: Custom	Document Description: ATX/EMI/12V_REG/VCC1_8		Rev: 1.0
Date: Monday, November 05, 2012	Sheet 33 of 45		











TPS51125

SLUS785A–OCTOBER 2007–REVISED NOVEMBER 2007

Texas Instruments
www.ti.com

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Softstart						
t_{SS}	Internal SS time	Internal soft start	1.1	1.6	2.1	ms

MSI	MICRO-STAR INT'L CO.,LTD			
	MS-A953			
Size: Custom	Document Description: 3V/5V (TPS51125RGER)			Rev: 1.0
Date: Wednesday, October 31, 2012		Sheet 34 of 45		

CLK	MODE1 Pin 27 R242	MODE0 Pin 42 R236
48MHz	X	X
24MHz	X	1
12MHz (XTAL)	1	1

SBD6 + (USB_CARD_P) / SBD6 - (USB_CARD_N) (Zdiff) is 90Ω±10%
Maintain at least 20 mils air gap to the edge of the reference plane

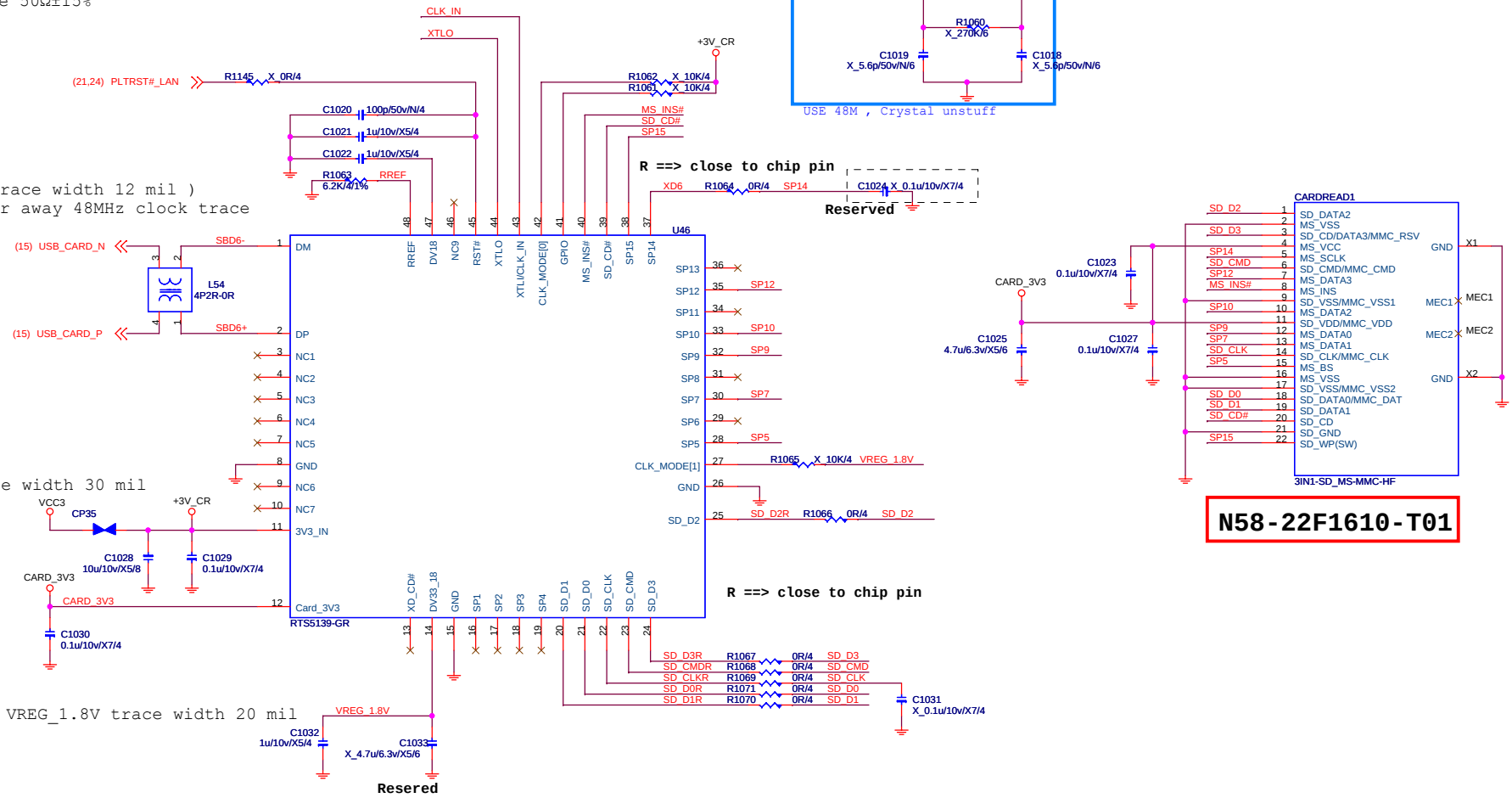
| CLK - DATA | trace length ≦ 100 mils
| DATA - DATA | trace length ≦ 100 mils
no more 2 via ; 2 inch (maximum)

MS_SCLK (Pin 37 SP14) & SD_CLK (Pin 22 SD_CLK)
are impedance are 50Ω±15%

Pin 48(RREF trace width 12 mil)
trace must far away 48MHz clock trace

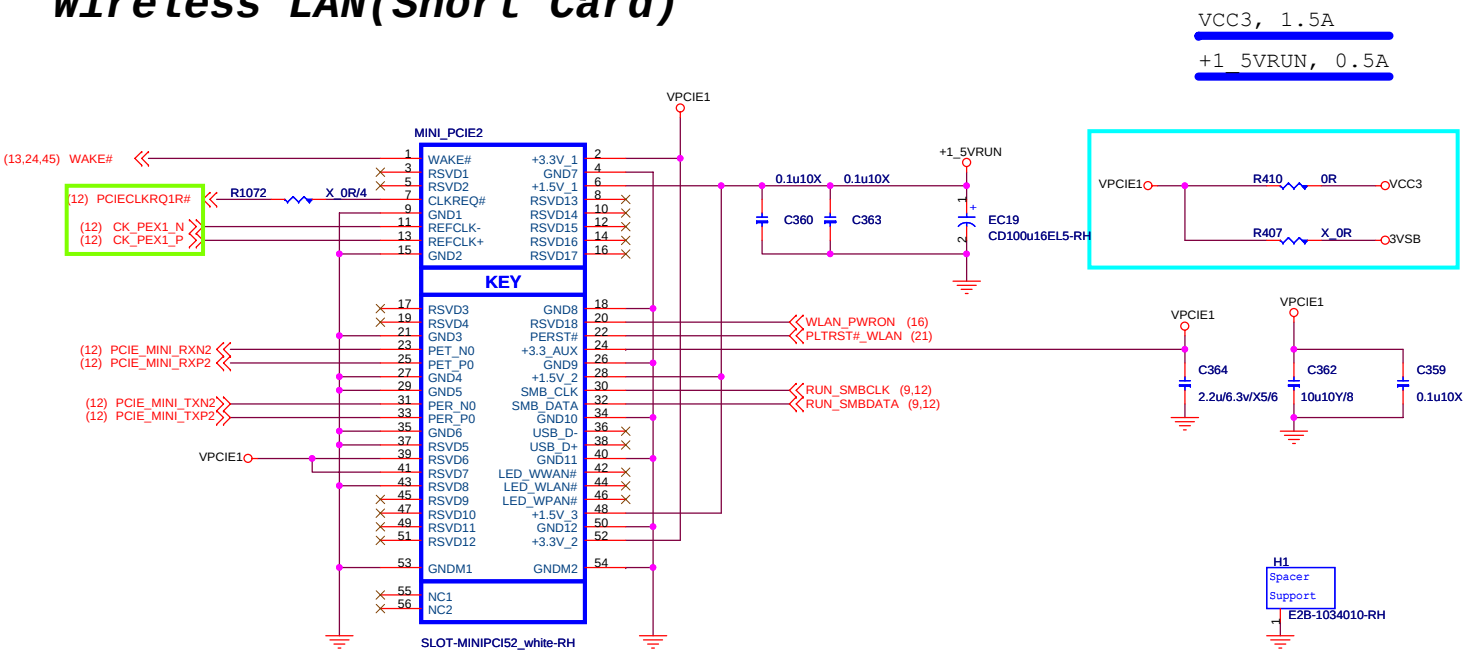
+3V_CR trace width 30 mil

VREG_1.8V trace width 20 mil

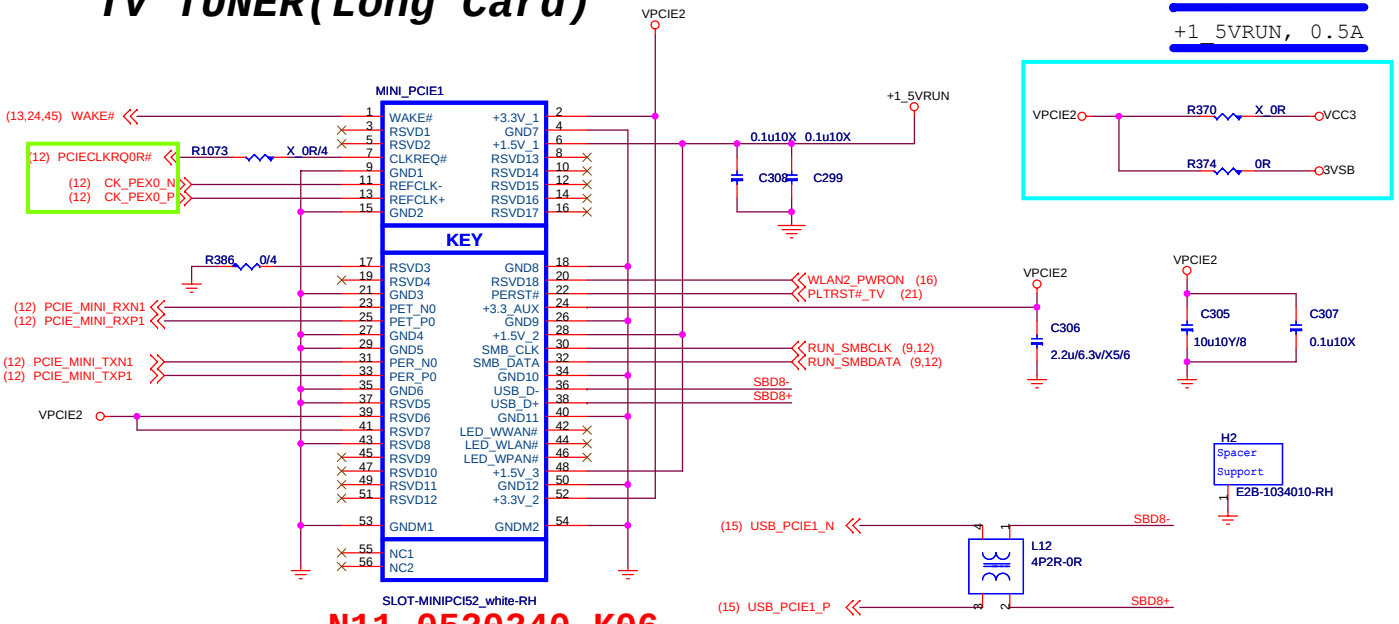


MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: CARD READER_RTS5139	Rev: 1.0
Date: Monday, October 22, 2012	Sheet 35 of 45	

Wireless LAN(Short Card)



TV TUNER(Long Card)

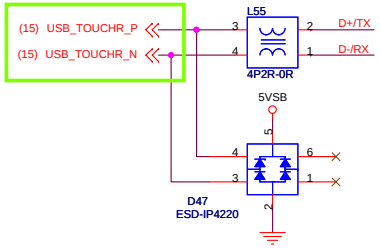


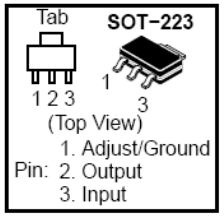
N11-0520240-K06

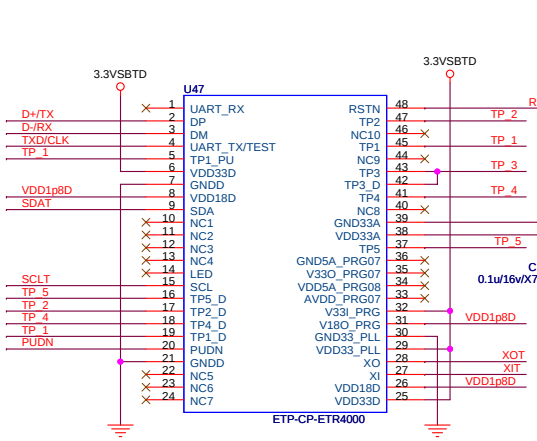
PCI ExpressR
Mini Card Electromechanical
Specification
Revision 1.2

MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: MINI-PCIE Slot	Rev: 1.0
Date: Wednesday, October 24, 2012	Sheet 36 of 45	

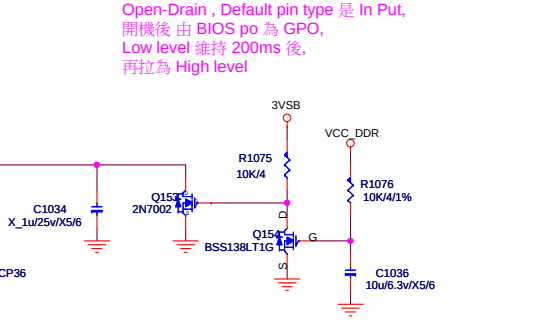
Low Speed USB D+/D-



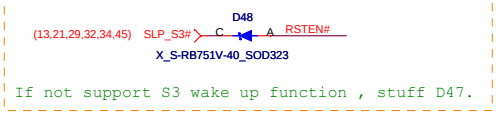




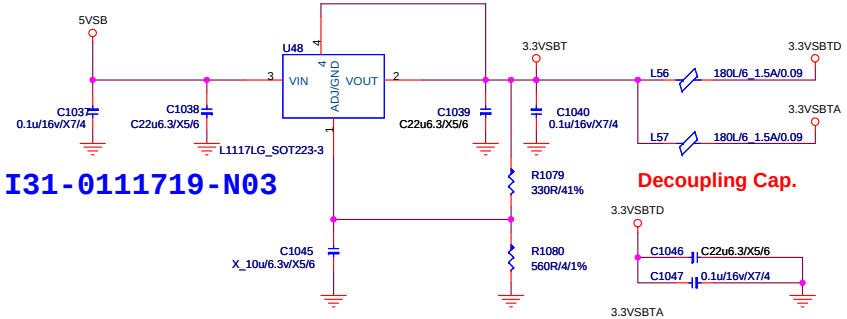
B07-ETPCP04-E79



Open-Drain , Default pin type 是 In Put,
開機後 由 BIOS po 為 GPO,
Low level 維持 200ms 後,
再拉為 High level

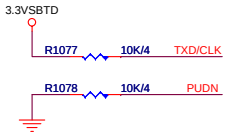


If not support S3 wake up function , stuff D47.

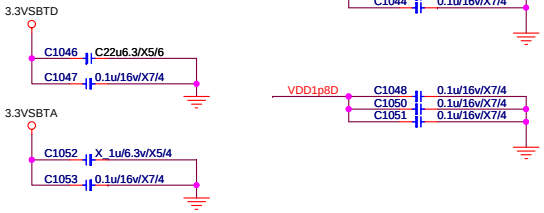


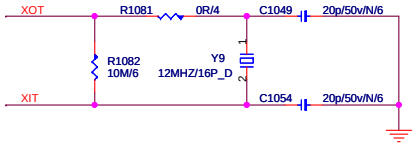
I31-0111719-N03

Vout=1.25*[1+(R732/R730)]

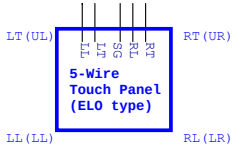


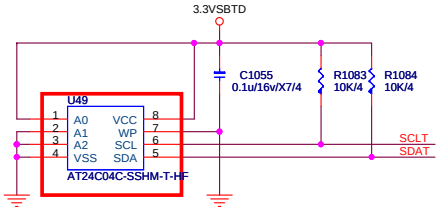
Decoupling Cap.



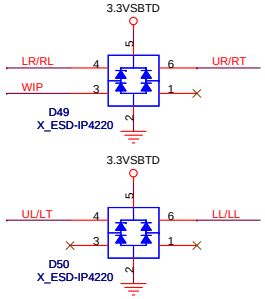


(Option 1) 5-Wire Resistive Touch Panel for ELO_type

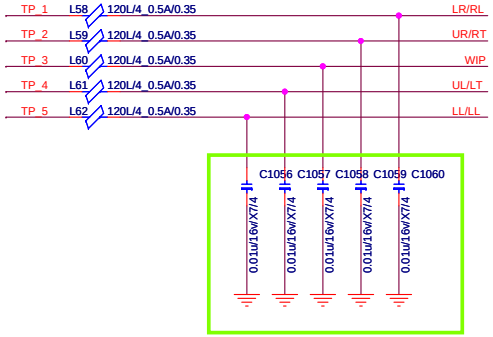


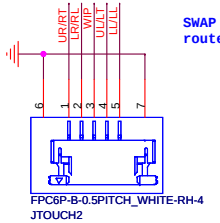


M33-24C0463-A26



EMI Suppressor

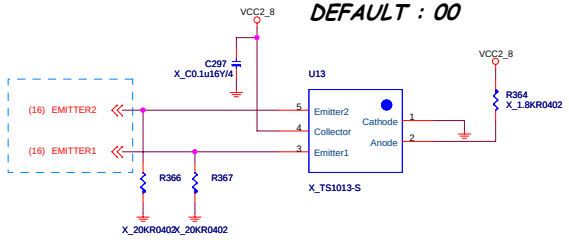




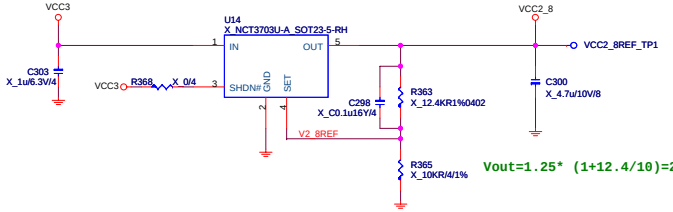
SWAP for cable route..

MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: Single Touch ETP-CP-ETR4000	Rev: 1.0
Date: Monday, November 05, 2012	Sheet 37 of 45	

DEFAULT : 00



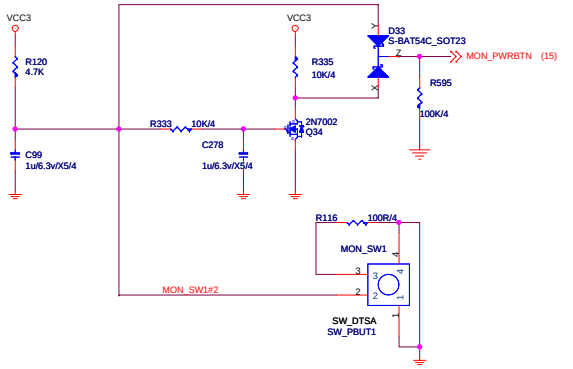
VCC2_8



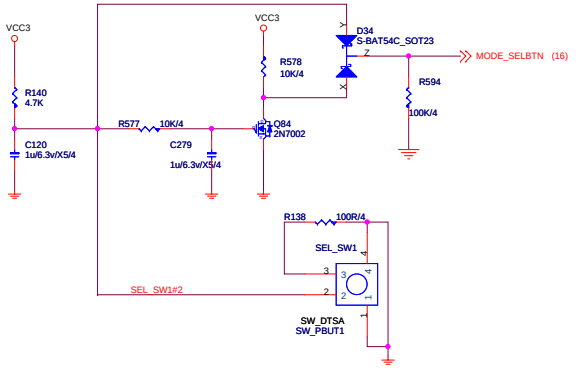
Detecting Rotation Characteristics

	E1	E2
E2 / LED / E1	0	1
E1 / E2 / LED	0	0
E1 / LED / E2	1	0
LED / E2 / E1	1	1

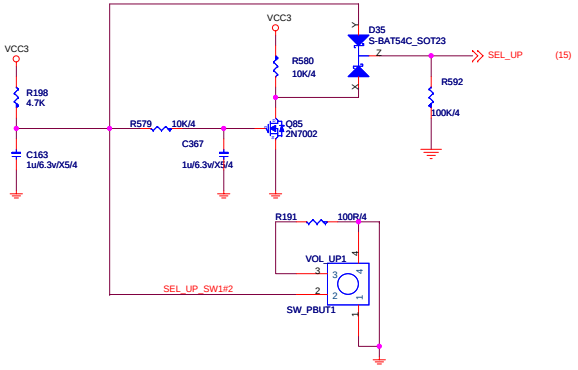
MONITOR ON/OFF BUTTON

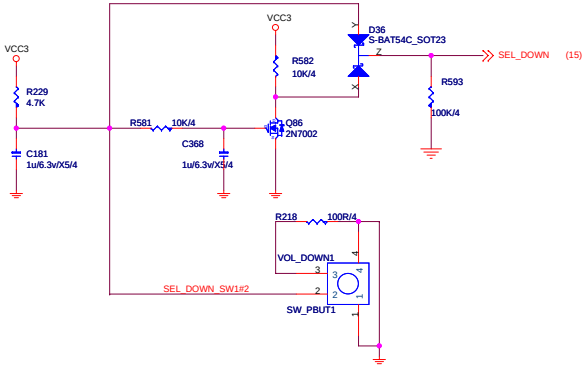


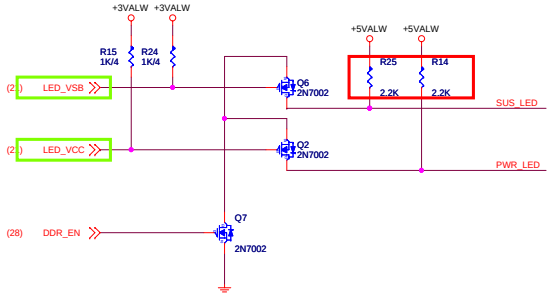
MODE SELECT BUTTON



MODE SELECT CONTROL

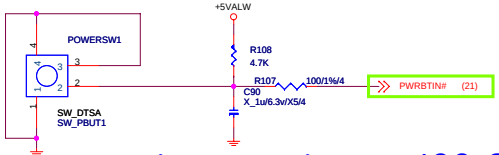






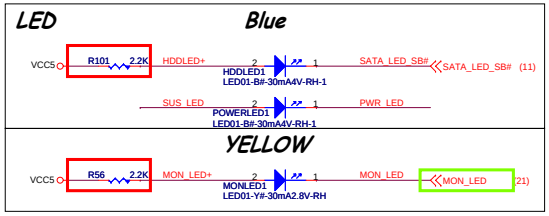
SYSTEM RESET

POWER ON/OFF BUTTON



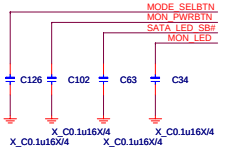
LED

Blue



YELLOW

FOR EMI



MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: C	Document Description: HOTKEY/LED/Edi-Tensor	Rev: 1.0
Date: Monday, November 05, 2012	Sheet 38 of 45	

Mounting Holes

Org.

M2 M4 M5 M7 M3 M6 M1 M10

BAT2
BAT-BCR2032P-RH

PCB1
MS-A9531-1.0

Single End 50ohm

J2 — L1_4mil_50_Ohm — VCC3 — J3 — L4_4mil_50_Ohm
X_H1X2_black-RH
X_H1X2_black-RH

J4 — L1_TOP_DIFF90+ / L1_TOP_DIFF90-
X_impedence

90 Ohm±10% 4/7/20(mil) put in Top layout

VCC3 — J5 — VCC3
L4_TOP_DIFF90+ / L4_TOP_DIFF90-
X_impedence

90 Ohm±10% 4/7/20(mil) put in bottom layout

E23-5566060-CA7

T4 X_E23-5566060-RH
T1 X_E23-5566060-RH
T3 X_E23-5566060-RH
T2 X_E23-5566060-RH

Optical Fiducial Marks-120

FM2 FM1 FM3 FM4 FM6 FM5 FM7 FM8
X_FM

U26 — MEC1 MEC2 MEC3 MEC4 — HS-0803120-RH
CPU FANSINK

U56 — HS-0800770
PCH HEATSINK

+5VALW: C334 C0.1u16Y/4, C23 C0.1u16Y/4, C183 C0.1u16Y/4
VCC5: C309 C0.1u16Y/4, C353 C0.1u16Y/4, C326 C0.1u16Y/4
DC_19V: C173 C0.1u25Y, C159 C0.1u25Y
DC_19V: C79 C0.1u25Y, C33 C0.1u25Y
VCC5: C196 C0.1u16Y/4
DC_19V: C205 C0.1u25Y
VCC3: C283 C0.1u16Y/4
VCC5: C350 C0.1u16Y/4
VCC_DDR: C361 C0.1u16Y/4
DC_19V: C68 C0.1u25Y, C3 C0.1u25Y
VCC3: C86 C0.1u25Y
DC_19V: C206 C0.1u25Y
VCC3: C595 C0.1u16Y/4
DC_19V: C596 C0.1u25Y
+CPU_GFX: C597 C0.1u16Y/4
DC_19V: C598 C0.1u25Y

VCC5: C371 C0.1u25X, C94 C0.1u25X, C88 C0.1u25X
5VSB: C437 C0.1u25X, C301 C0.1u25X
+3VALW: C311 C0.1u25X
DC_19V: C473 C0.1u25X
VCC3: C310 C0.1u25X, C392 C0.1u25X
VCC_DDR: C121 C0.1u25X, C106 C0.1u25X, C372 C0.1u25X

DC_19V — EMI: C490 X_C0.1u25Y, C343 X_C0.1u25Y, C482 X_C0.1u25Y

VCC_DDR: C373 C0.1u25X, C374 C0.1u25X, C532 C0.1u25X, C533 C0.1u25X

EMI

CPU_VTT: C894 X_0.1u/25w/X5/4, C895 X_0.1u/25w/X5/4
VCC_DDR: C896 X_0.1u/25w/X5/4, C897 X_0.1u/25w/X5/4, C898 X_0.1u/25w/X5/4, C899 X_0.1u/25w/X5/4

5VSB: C420 X_0.1u/25w/X5/4, C417 X_0.1u/25w/X5/4, C411 X_0.1u/25w/X5/4

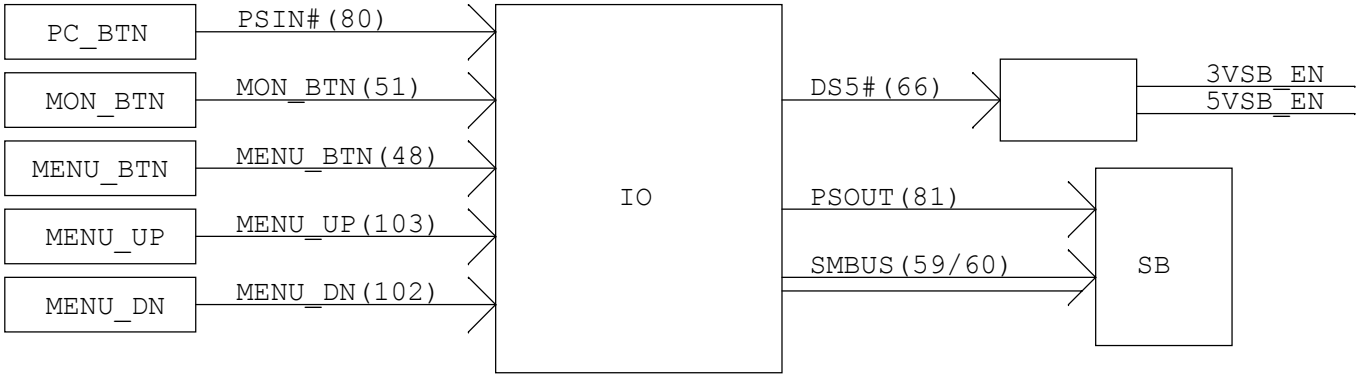
VCC3: C733 X_0.1u/25w/X5/4, C734 X_0.1u/25w/X5/4, C724 X_0.1u/25w/X5/4, C725 X_0.1u/25w/X5/4, C726 X_0.1u/25w/X5/4, C727 X_0.1u/25w/X5/4, C728 X_0.1u/25w/X5/4, C729 X_0.1u/25w/X5/4, C730 X_0.1u/25w/X5/4, C731 X_0.1u/25w/X5/4, C732 X_0.1u/25w/X5/4

VCC5: C472 C0.1u16Y/4, C182 C0.1u16Y/4
VCC3: C280 C0.1u16Y/4, C115 C0.1u16Y/4

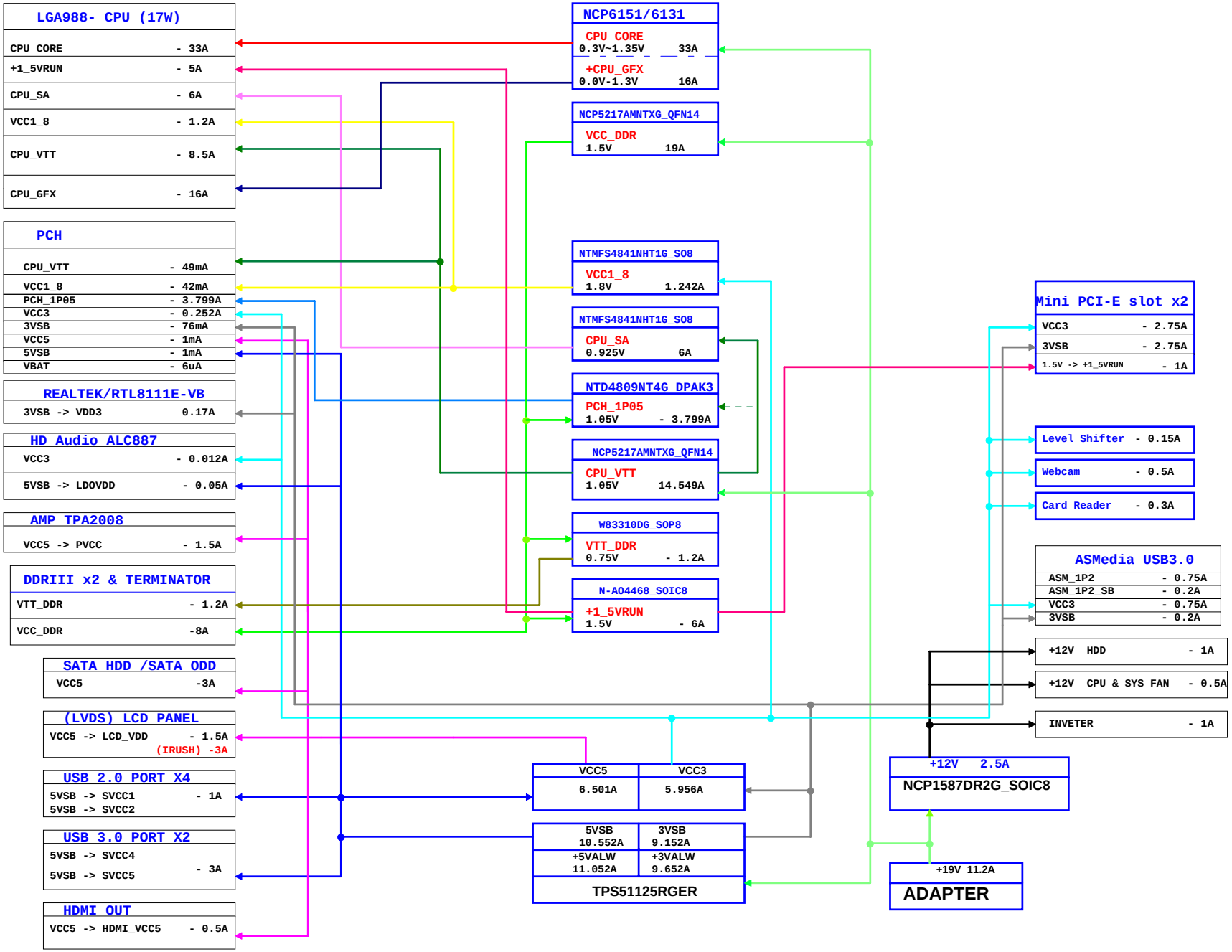
VCC5: C428 X_0.1u/25w/X5/4, C430 X_0.1u/25w/X5/4

DC_19V: C900 X_0.1u/25w/X5/4, C901 X_0.1u/25w/X5/4, C902 X_0.1u/25w/X5/4, C903 X_0.1u/25w/X5/4, C904 X_0.1u/25w/X5/4

MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: Manual parts	Rev: 1.0
Date: Thursday, November 01, 2012	Sheet 39 of 45	



MICRO-STAR INT'L CO.,LTD		
MS-A953		
Size: Custom	Document Description: S I/O BLOCK DIAGRAM	Rev: 1.0
Date: Tuesday, October 02, 2012	Sheet 40 of 45	



MICRO-STAR INT'L CO.,LTD

MS-A953

Size: Custom | Document Description: Power Delivery | Rev: 1.0

Date: Tuesday, October 02, 2012 | Sheet 41 of 45

A9531-0A change 1.0

page 22 HDMI_CON_DET fix circuit

page 31 EC57,EC58,EC60,EC61,EC62 change C71-8210271-N07

page 35 cardreader N58-22F1600-T01 change N58-22F1610-T01

page 28 ,23 ,33   EC37,EC39 ,EC73 C71-470530-S03 chagne C71-4702540-N07

page 25 PVCC source power 5VSB change VCC5.

page 33 ATX DC power jack , add voltage detect resistance R1333 (R11-012CT10-C36)
when R1333 unstuff , 0 ohm *3 stuff

10u C11-1067614-M09 change C11-1067614-T04

page 11 CLEARCMOS1 circuit fix

POWER TEAM FIX
C624,C623,C622,C621,C620,C655,C656,C657,C658,C659,C668,C669,C670,C671,C672,C673,C661,C662,C663,C664 NC
EC43,EC44,EC46,EC51,EC54,EC76,EC77,EC79,EC53,EC62,EC61,EC60,EC57,EC58 change C71-8210271-N07
EC41,EC42,EC50,EC78,EC83,EC82,EC75,EC59,C890,C892,Q128 REMOVE
EC52 change C11-1067313-S02
CHOKE8 change L04-05A7211-L65
R974 change 3.9 k ohm
R1140 change 2.37 k ohm
R1127 change 2.37 k ohm
R598 change 1.82 k ohm
R860 change 19.1 k ohm

page15 16 MON_PWRBTN GPIO3 change GPIO0

page21 VTIN1 FIX PWM circuit

page16 ADD GPIO57 set pull high FANSINK , pull low FANLESS

page38 R101 R56 R25 R14 LED set 2.2k

page15 RN26 unstuff for button .

power team fix
R854 change 8.45k ohm 1%
R995 change 8.45k ohm 1%
R996 change 6.49k ohm 1%
R999 change 32.4k ohm 1%

page 31 R970 change 2.37K VRM_PGD for sequence back.

page21 3VSB 5VSB in deep S5 leakage.

CHARGER_EN	3VSB	--> +3VALW
CHARGER_CB	3VSB	--> +3VALW
SIO_PME#	+3VALW	--> 3VSB
PSOUT#	3VSB	--> UNSTUFF

page 21 ADD VCC3 VCC5 LEAK current issue.

page 23 14 LVDS panel 18.5 "change 19.5" fix daul channel

page 23 C11-1063027-*** change C11-1067514-*** C461,C478

page 24 C11-4757014-*** change C11-4757313-*** C336,C349

page 23 backlight SIO control change SCH control R472 unstuff R478 stuff.

page 21 SIO change FINTEK F71878 COLAY

page 12 GPIO 26 reserver

page 16 GPIO38 set USB3.0 2.0 , GPIO48 set WIN7 WIN8, GPIO49 set COM PORT

page 15 USB30_SMI pull high 3VSB change VCC3, R751

page 45 USB3.0 Sequence fix , Q156 unstuff ,R509 change 100k , C1089 change 1u.

page 39 CPU HEATSINK change FANSINK

page 9 DIMM N13-2040680-F02 change N13-2040790-CK3 FOR COST DOWN

page 36 mini pcie N11-0520040-A81 change N11-0520240-K06 FOR COST DOWN

page 23 REMOVE VGA circuit

page 23 swap L6, L27

MICRO-STAR INT'L CO.,LTD

MS-A953

Size: Custom | Document Description: HISTORY | Rev: 1.0

Date: Friday, October 26, 2012 | Sheet 42 of 45

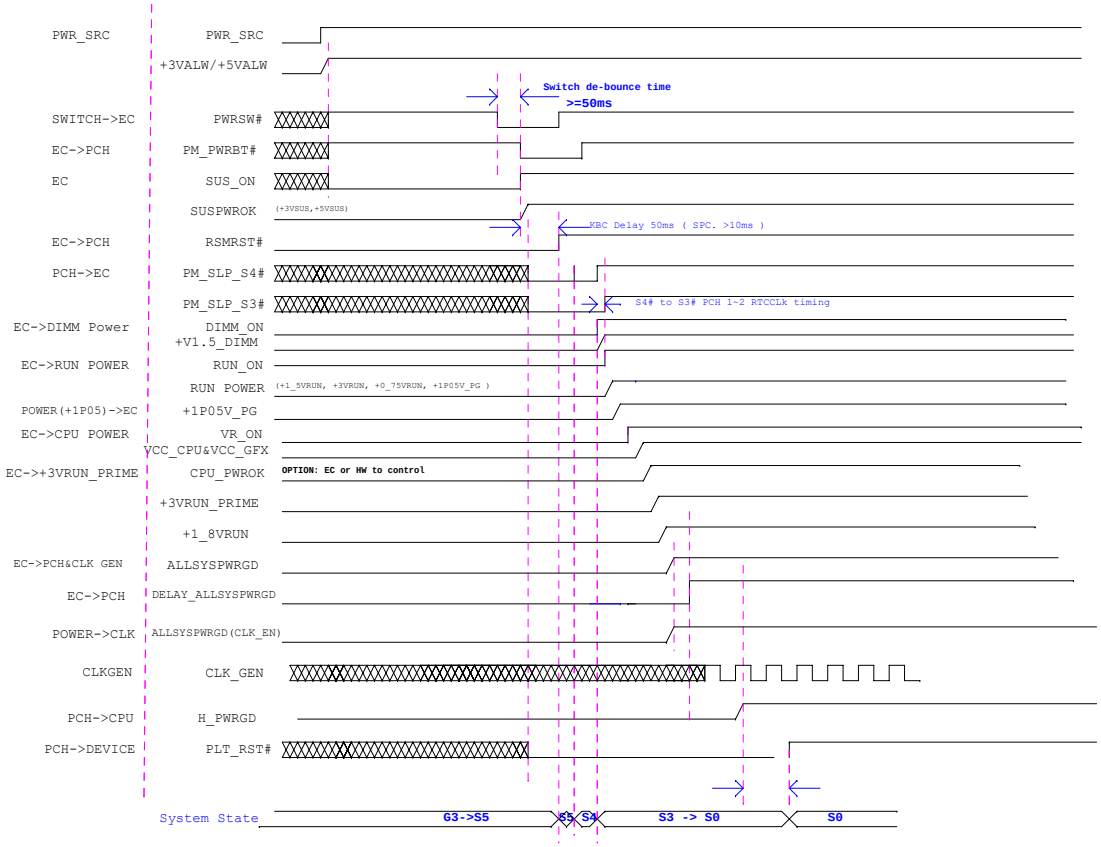
MICRO-STAR INT'L CO.,LTD

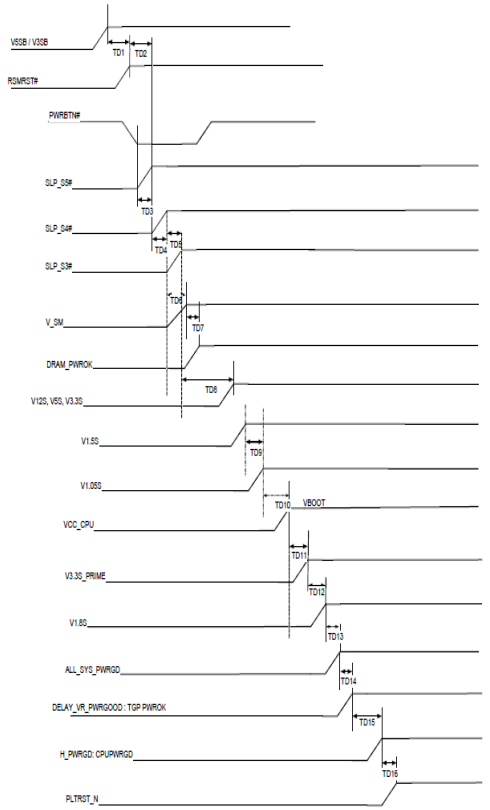
MS-A953

Size	Document Description	Rev
C	External Converter	1.0

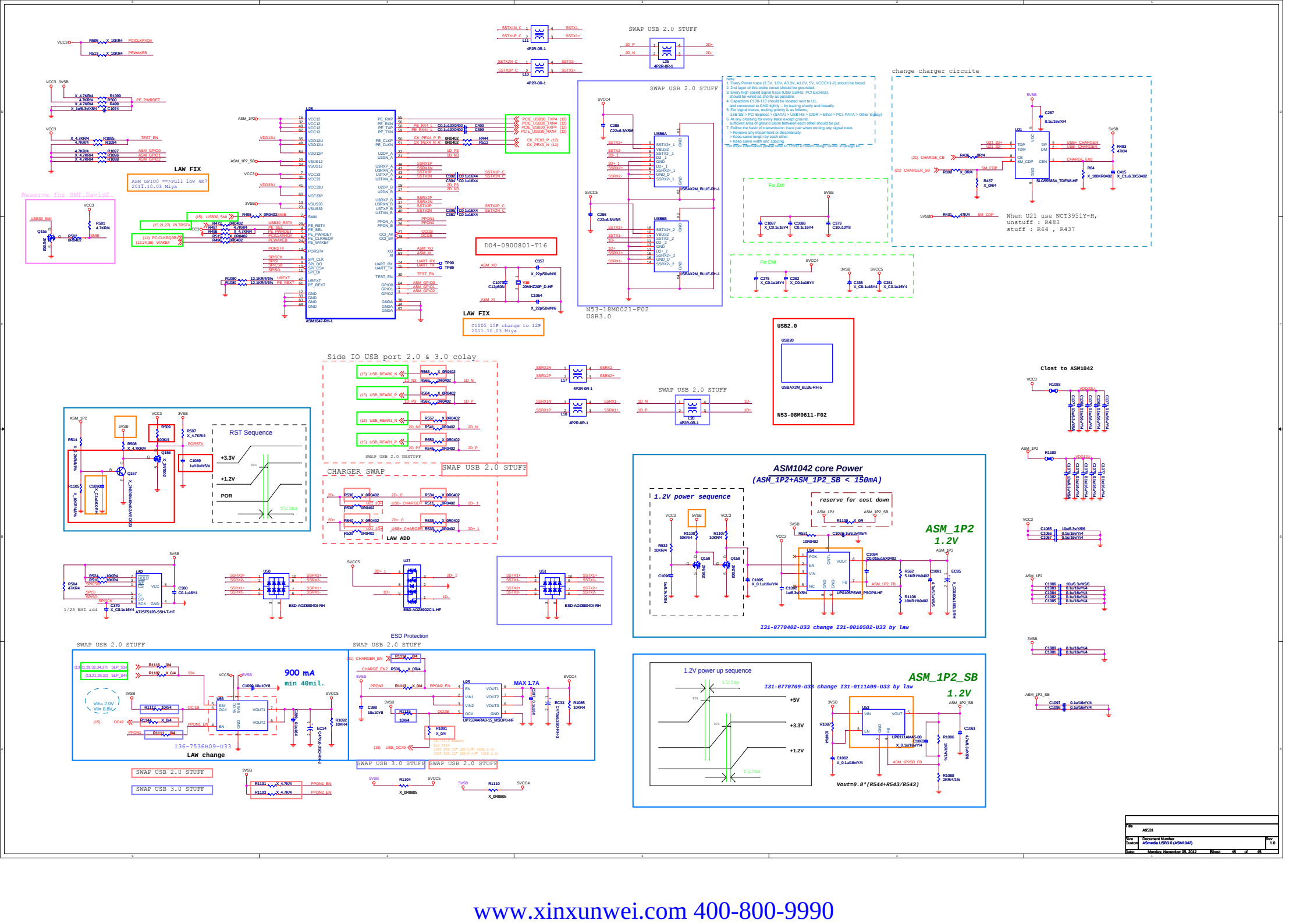
Date: Tuesday, October 02, 2012 | Sheet 43 of 45

Cedar Trail Power on Sequence DC mode





MICRO-STAR INT'L CO.,LTD			
MS-A953			
Size: Custom	Document Description: Power Sequencing		Rev: 1.0
Date: Tuesday, October 02, 2012	Sheet 44 of 45		


SWAP USB 2.0 STUFF
LAW FIX
ASM_GPIO0 ==>Pull low 4K7
2011.10.03 Miya
Reserve for SMI.David2.
SWAP USB 2.0 STUFF
N53-18M0021-F02
USB3.0
change charger circuite
When U21 use NCT3951Y-H,
unstuff : R483
stuff : R64 , R437
D04-0900801-T16
LAW FIX
C1005 15P change to 12P
2011.10.03 Miya
Side IO USB port 2.0 & 3.0 colay
CHARGER SWAP
SWAP USB 2.0 STUFF
LAW ADD
SWAP USB 2.0 UNSTUFF
USB2.0
USB20
USBAX2M_BLUE-RH-5
N53-08M0611-F02
Clost to ASM1042
RST Sequence
+3.3V
+1.2V
POR
ASM1042 core Power
(ASM_1P2+ASM_1P2_SB < 150mA)
1.2V power sequence
reserve for cost down
ASM_1P2
1.2V
I31-0770402-U33 change I31-0010502-U33 by law
ESD Protection
SWAP USB 2.0 STUFF
SWAP USB 3.0 STUFF
900 mA
min 40mil.
I36-7536B09-U33
LAW change
MAX 1.7A
1.2V power up sequence
I31-0770709-U33 change I31-0111A09-U33 by law
ASM_1P2_SB
1.2V
Vout=0.8*(R544+R543/R543)
www.xinxunwei.com 400-800-9990