MS-7A94

ATX

Ver: 10

Basinfall Platform

CPU:

Skylake X/Kabylake X

System Chipset:

Kaby Lake PCH-X

Onboard Chip:

HD Audio Codec:ALC1220

LAN-Intel i219

SIO:NTC6795D

Dual Flash ROM: SPI 64 MB X2

Main Memory:

*DDRIV (UP to 2677MHz) * 8DIMM (4 Channel)*

ACPI:

MPS

PWM:

VR13 -IR35201

Expansion Slots:

*PCI Express (X16) Slot * 2*
*PCI Express (X8) Slot * 1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 1*

Other:

*SATA3.0 *8*
*USB2.0 *6 Ports (4R/4F)*
*REAR USB30*4 + USB3.1*1 & TYPEC*1*
*FRONT USB3.0 *4+TYPEC*1*

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MA-7A94..

Size	Document Description	Rev
Custom	Cover Sheet	1.0

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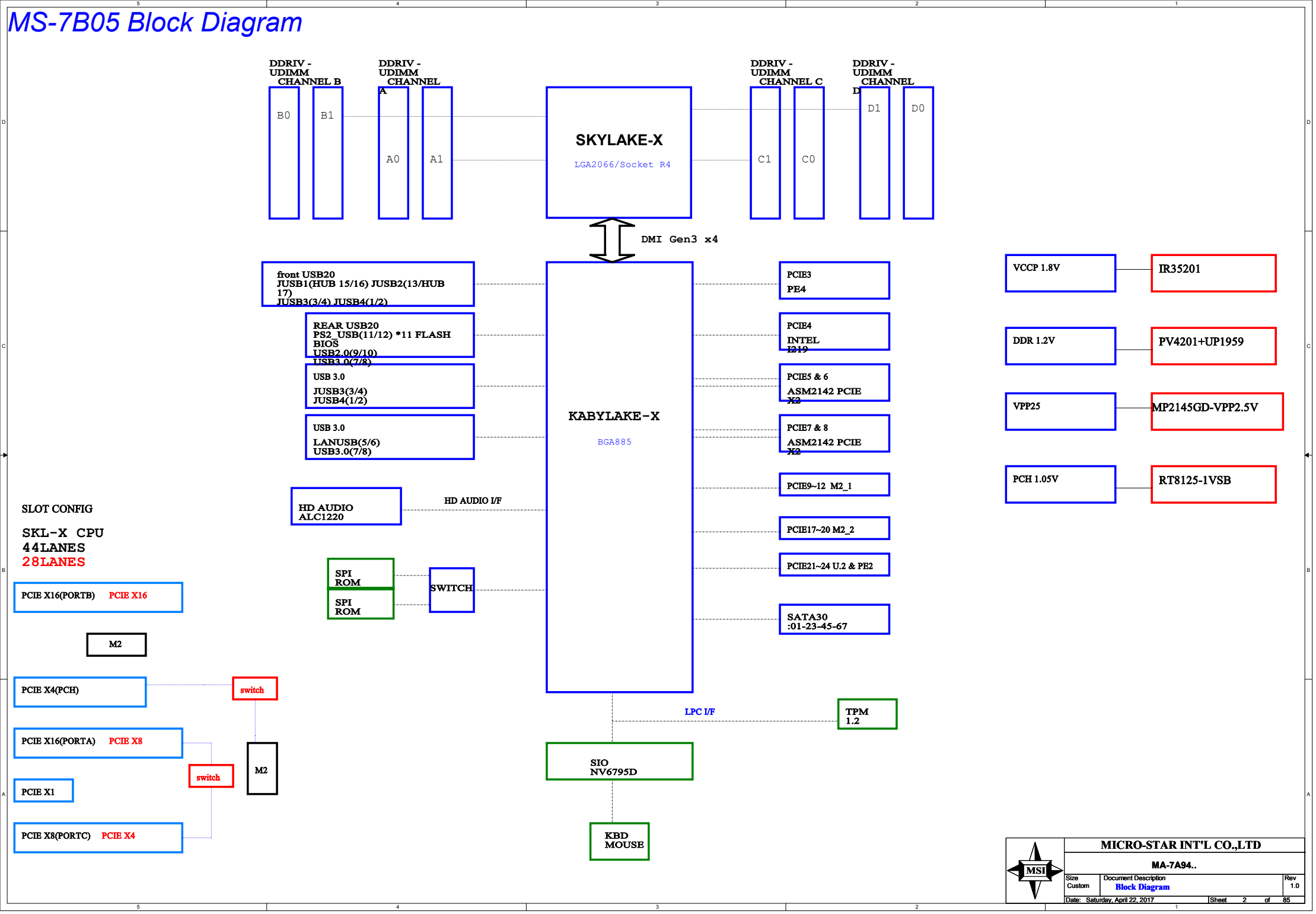
MS-7B05 Block Diagram



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Size: Custom	Document Description: Block Diagram
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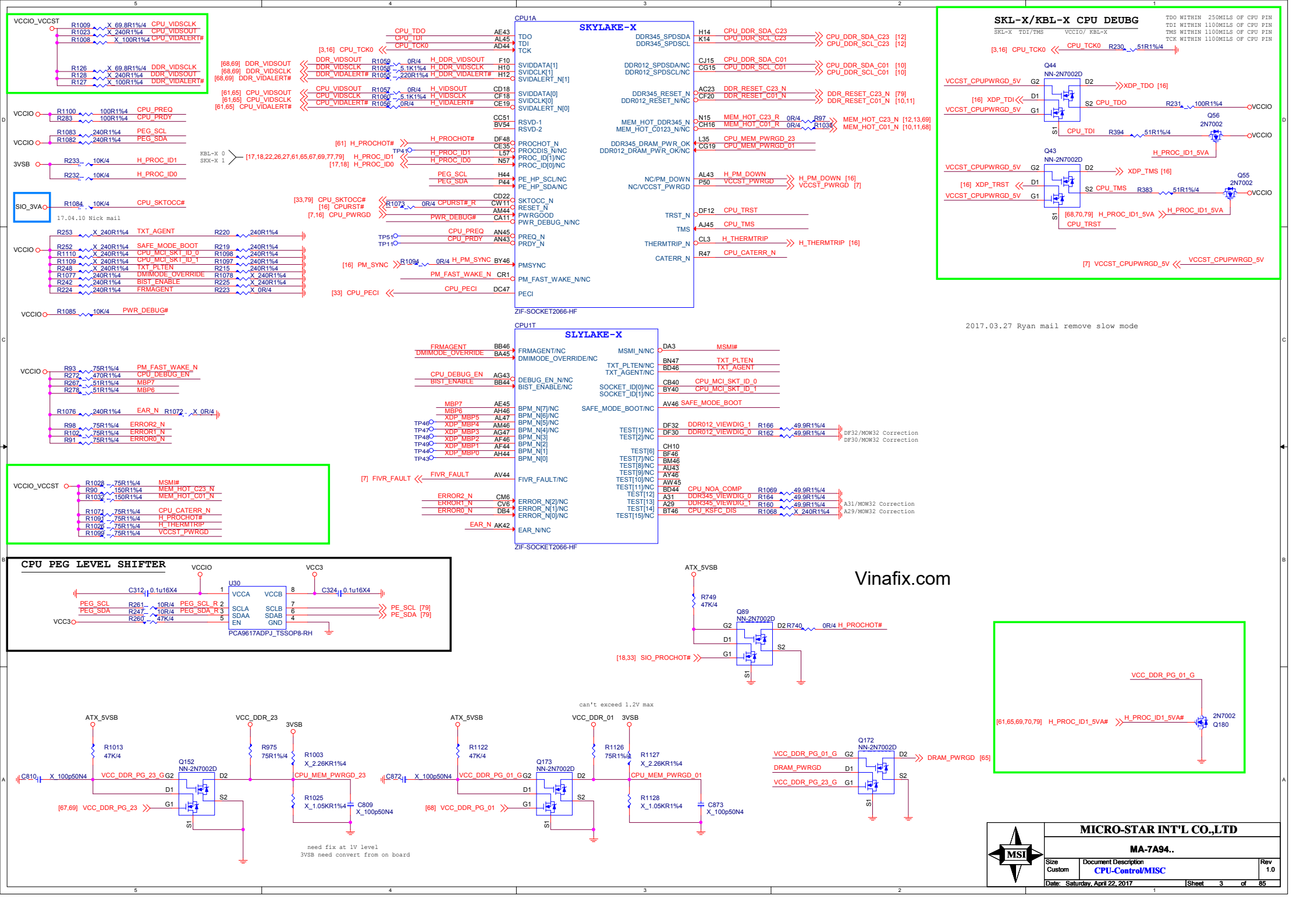
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CPU1T
ZIF-SOCKET2066-HF
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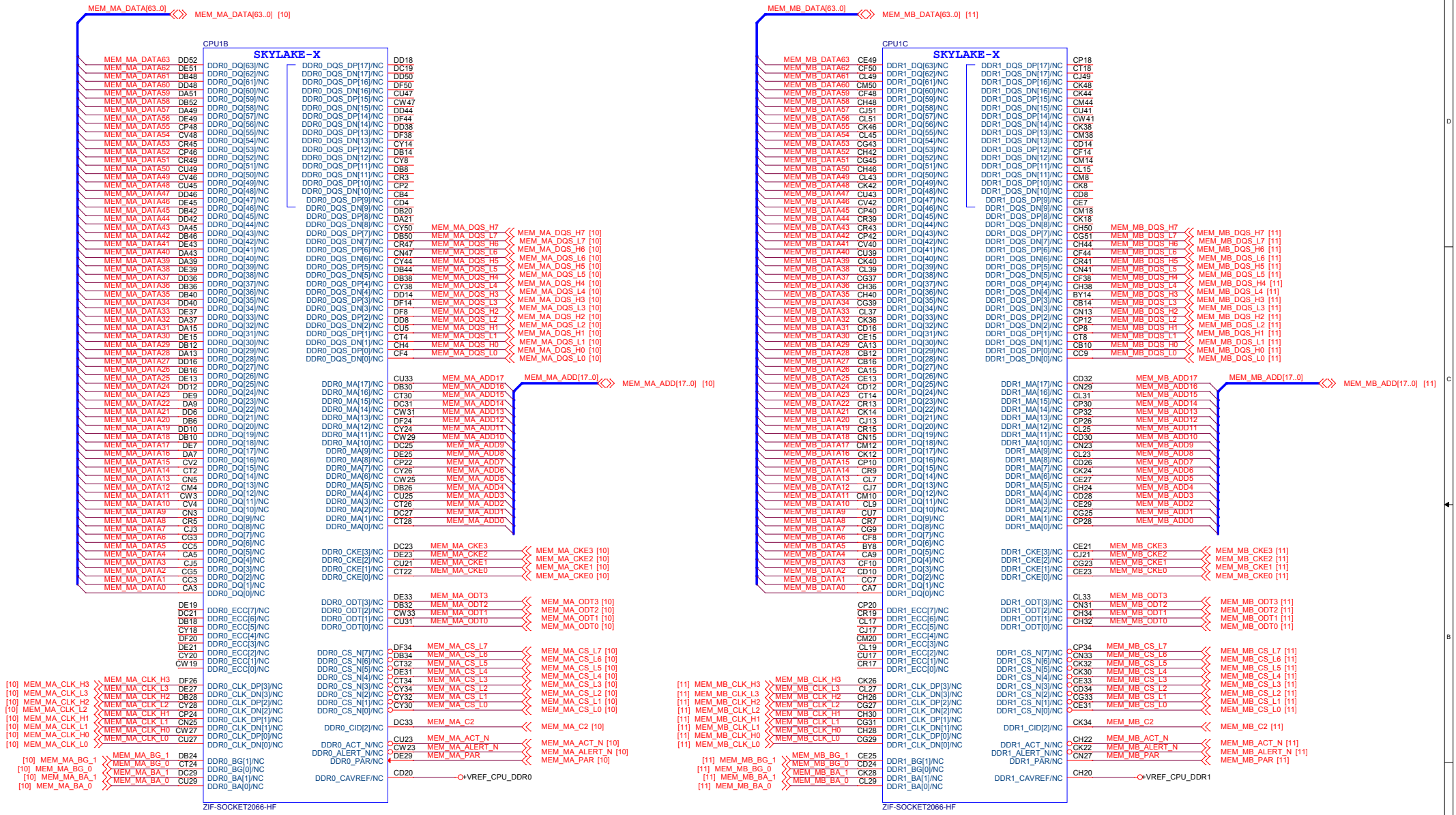
17.04.10 Nick mail
2017.03.27 Ryan mail remove slow mode
CPU PEG LEVEL SHIFTER
PCA9617ADPJ_TSSOP8-RH
Vinafix.com
need fix at 1V level
3VSB need convert from on board
MICRO-STAR INT'L CO.,LTD
MA-7A94..
CPU-Control/MISC
Date: Saturday, April 22, 2017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Document Description
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Rev
1.0
Date: Saturday, April 22, 2017
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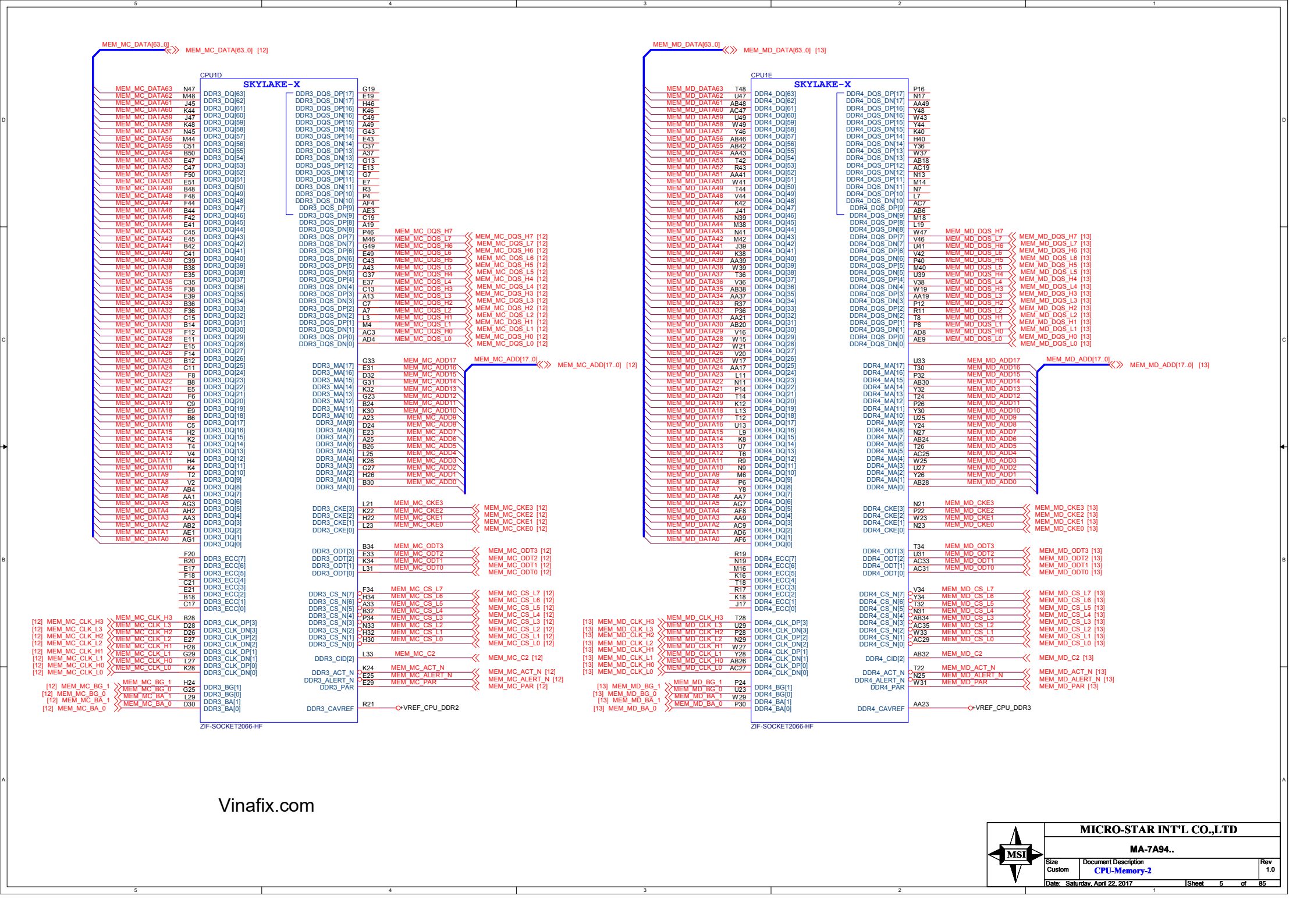
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DDR3_MA[8]
DDR3_MA[7]
DDR3_MA[6]
DDR3_MA[5]
DDR3_MA[4]
DDR3_MA[3]
DDR3_MA[2]
DDR3_MA[1]
DDR3_MA[0]
MEM_MC_CKE3
MEM_MC_CKE2
MEM_MC_CKE1
MEM_MC_CKE0
DDR3_CKE[3]
DDR3_CKE[2]
DDR3_CKE[1]
DDR3_CKE[0]
MEM_MC_ODT3
MEM_MC_ODT2
MEM_MC_ODT1
MEM_MC_ODT0
DDR3_ODT[3]
DDR3_ODT[2]
DDR3_ODT[1]
DDR3_ODT[0]
MEM_MC_CS_L7
MEM_MC_CS_L6
MEM_MC_CS_L5
MEM_MC_CS_L4
MEM_MC_CS_L3
MEM_MC_CS_L2
MEM_MC_CS_L1
MEM_MC_CS_L0
DDR3_CS_N[7]
DDR3_CS_N[6]
DDR3_CS_N[5]
DDR3_CS_N[4]
DDR3_CS_N[3]
DDR3_CS_N[2]
DDR3_CS_N[1]
DDR3_CS_N[0]
MEM_MC_CLK_H3
MEM_MC_CLK_L3
MEM_MC_CLK_H2
MEM_MC_CLK_L2
MEM_MC_CLK_H1
MEM_MC_CLK_L1
MEM_MC_CLK_H0
MEM_MC_CLK_L0
[12] MEM_MC_CLK_H3
[12] MEM_MC_CLK_L3
[12] MEM_MC_CLK_H2
[12] MEM_MC_CLK_L2
[12] MEM_MC_CLK_H1
[12] MEM_MC_CLK_L1
[12] MEM_MC_CLK_H0
[12] MEM_MC_CLK_L0
MEM_MC_C2
DDR3_CID[2]
MEM_MC_ACT_N
MEM_MC_ALERT_N
MEM_MC_PAR
DDR3_ACT_N
DDR3_ALERT_N
DDR3_PAR
MEM_MC_BG_1
MEM_MC_BG_0
MEM_MC_BA_1
MEM_MC_BA_0
[12] MEM_MC_BG_1
[12] MEM_MC_BG_0
[12] MEM_MC_BA_1
[12] MEM_MC_BA_0
DDR3_CAVREF
VREF_CPU_DDR2
ZIF-SOCKET2066-HF
MEM_MD_DATA[63..0]
MEM_MD_DATA[63..0] [13]
CPU1E
SKYLAKE-X
DDR4_DQ[63]
DDR4_DQ[62]
DDR4_DQ[61]
DDR4_DQ[60]
DDR4_DQ[59]
DDR4_DQ[58]
DDR4_DQ[57]
DDR4_DQ[56]
DDR4_DQ[55]
DDR4_DQ[54]
DDR4_DQ[53]
DDR4_DQ[52]
DDR4_DQ[51]
DDR4_DQ[50]
DDR4_DQ[49]
DDR4_DQ[48]
DDR4_DQ[47]
DDR4_DQ[46]
DDR4_DQ[45]
DDR4_DQ[44]
DDR4_DQ[43]
DDR4_DQ[42]
DDR4_DQ[41]
DDR4_DQ[40]
DDR4_DQ[39]
DDR4_DQ[38]
DDR4_DQ[37]
DDR4_DQ[36]
DDR4_DQ[35]
DDR4_DQ[34]
DDR4_DQ[33]
DDR4_DQ[32]
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DDR4_DQ[30]
DDR4_DQ[29]
DDR4_DQ[28]
DDR4_DQ[27]
DDR4_DQ[26]
DDR4_DQ[25]
DDR4_DQ[24]
DDR4_DQ[23]
DDR4_DQ[22]
DDR4_DQ[21]
DDR4_DQ[20]
DDR4_DQ[19]
DDR4_DQ[18]
DDR4_DQ[17]
DDR4_DQ[16]
DDR4_DQ[15]
DDR4_DQ[14]
DDR4_DQ[13]
DDR4_DQ[12]
DDR4_DQ[11]
DDR4_DQ[10]
DDR4_DQ[9]
DDR4_DQ[8]
DDR4_DQ[7]
DDR4_DQ[6]
DDR4_DQ[5]
DDR4_DQ[4]
DDR4_DQ[3]
DDR4_DQ[2]
DDR4_DQ[1]
DDR4_DQ[0]
DDR4_ECC[7]
DDR4_ECC[6]
DDR4_ECC[5]
DDR4_ECC[4]
DDR4_ECC[3]
DDR4_ECC[2]
DDR4_ECC[1]
DDR4_ECC[0]
DDR4_CLK_DP[3]
DDR4_CLK_DN[3]
DDR4_CLK_DP[2]
DDR4_CLK_DN[2]
DDR4_CLK_DP[1]
DDR4_CLK_DN[1]
DDR4_CLK_DP[0]
DDR4_CLK_DN[0]
DDR4_BG[1]
DDR4_BG[0]
DDR4_BA[1]
DDR4_BA[0]
DDR4_DQS_DP[17]
DDR4_DQS_DN[17]
DDR4_DQS_DP[16]
DDR4_DQS_DN[16]
DDR4_DQS_DP[15]
DDR4_DQS_DN[15]
DDR4_DQS_DP[14]
DDR4_DQS_DN[14]
DDR4_DQS_DP[13]
DDR4_DQS_DN[13]
DDR4_DQS_DP[12]
DDR4_DQS_DN[12]
DDR4_DQS_DP[11]
DDR4_DQS_DN[11]
DDR4_DQS_DP[10]
DDR4_DQS_DN[10]
DDR4_DQS_DP[9]
DDR4_DQS_DN[9]
DDR4_DQS_DP[8]
DDR4_DQS_DN[8]
DDR4_DQS_DP[7]
DDR4_DQS_DN[7]
DDR4_DQS_DP[6]
DDR4_DQS_DN[6]
DDR4_DQS_DP[5]
DDR4_DQS_DN[5]
DDR4_DQS_DP[4]
DDR4_DQS_DN[4]
DDR4_DQS_DP[3]
DDR4_DQS_DN[3]
DDR4_DQS_DP[2]
DDR4_DQS_DN[2]
DDR4_DQS_DP[1]
DDR4_DQS_DN[1]
DDR4_DQS_DP[0]
DDR4_DQS_DN[0]
MEM_MD_DQS_H7
MEM_MD_DQS_L7
MEM_MD_DQS_H6
MEM_MD_DQS_L6
MEM_MD_DQS_H5
MEM_MD_DQS_L5
MEM_MD_DQS_H4
MEM_MD_DQS_L4
MEM_MD_DQS_H3
MEM_MD_DQS_L3
MEM_MD_DQS_H2
MEM_MD_DQS_L2
MEM_MD_DQS_H1
MEM_MD_DQS_L1
MEM_MD_DQS_H0
MEM_MD_DQS_L0
MEM_MD_ADD17
MEM_MD_ADD16
MEM_MD_ADD15
MEM_MD_ADD14
MEM_MD_ADD13
MEM_MD_ADD12
MEM_MD_ADD11
MEM_MD_ADD10
MEM_MD_ADD9
MEM_MD_ADD8
MEM_MD_ADD7
MEM_MD_ADD6
MEM_MD_ADD5
MEM_MD_ADD4
MEM_MD_ADD3
MEM_MD_ADD2
MEM_MD_ADD1
MEM_MD_ADD0
MEM_MD_ADD[17..0]
MEM_MD_ADD[17..0] [13]
DDR4_MA[17]
DDR4_MA[16]
DDR4_MA[15]
DDR4_MA[14]
DDR4_MA[13]
DDR4_MA[12]
DDR4_MA[11]
DDR4_MA[10]
DDR4_MA[9]
DDR4_MA[8]
DDR4_MA[7]
DDR4_MA[6]
DDR4_MA[5]
DDR4_MA[4]
DDR4_MA[3]
DDR4_MA[2]
DDR4_MA[1]
DDR4_MA[0]
MEM_MD_CKE3
MEM_MD_CKE2
MEM_MD_CKE1
MEM_MD_CKE0
DDR4_CKE[3]
DDR4_CKE[2]
DDR4_CKE[1]
DDR4_CKE[0]
MEM_MD_ODT3
MEM_MD_ODT2
MEM_MD_ODT1
MEM_MD_ODT0
DDR4_ODT[3]
DDR4_ODT[2]
DDR4_ODT[1]
DDR4_ODT[0]
MEM_MD_CS_L7
MEM_MD_CS_L6
MEM_MD_CS_L5
MEM_MD_CS_L4
MEM_MD_CS_L3
MEM_MD_CS_L2
MEM_MD_CS_L1
MEM_MD_CS_L0
DDR4_CS_N[7]
DDR4_CS_N[6]
DDR4_CS_N[5]
DDR4_CS_N[4]
DDR4_CS_N[3]
DDR4_CS_N[2]
DDR4_CS_N[1]
DDR4_CS_N[0]
MEM_MD_CLK_H3
MEM_MD_CLK_L3
MEM_MD_CLK_H2
MEM_MD_CLK_L2
MEM_MD_CLK_H1
MEM_MD_CLK_L1
MEM_MD_CLK_H0
MEM_MD_CLK_L0
[13] MEM_MD_CLK_H3
[13] MEM_MD_CLK_L3
[13] MEM_MD_CLK_H2
[13] MEM_MD_CLK_L2
[13] MEM_MD_CLK_H1
[13] MEM_MD_CLK_L1
[13] MEM_MD_CLK_H0
[13] MEM_MD_CLK_L0
MEM_MD_C2
DDR4_CID[2]
MEM_MD_ACT_N
MEM_MD_ALERT_N
MEM_MD_PAR
DDR4_ACT_N
DDR4_ALERT_N
DDR4_PAR
MEM_MD_BG_1
MEM_MD_BG_0
MEM_MD_BA_1
MEM_MD_BA_0
[13] MEM_MD_BG_1
[13] MEM_MD_BG_0
[13] MEM_MD_BA_1
[13] MEM_MD_BA_0
DDR4_CAVREF
VREF_CPU_DDR3
ZIF-SOCKET2066-HF
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MICRO-STAR INT'L CO.,LTD
MA-7A94..
Size
Custom
Document Description
CPU-Memory-2
Rev
1.0
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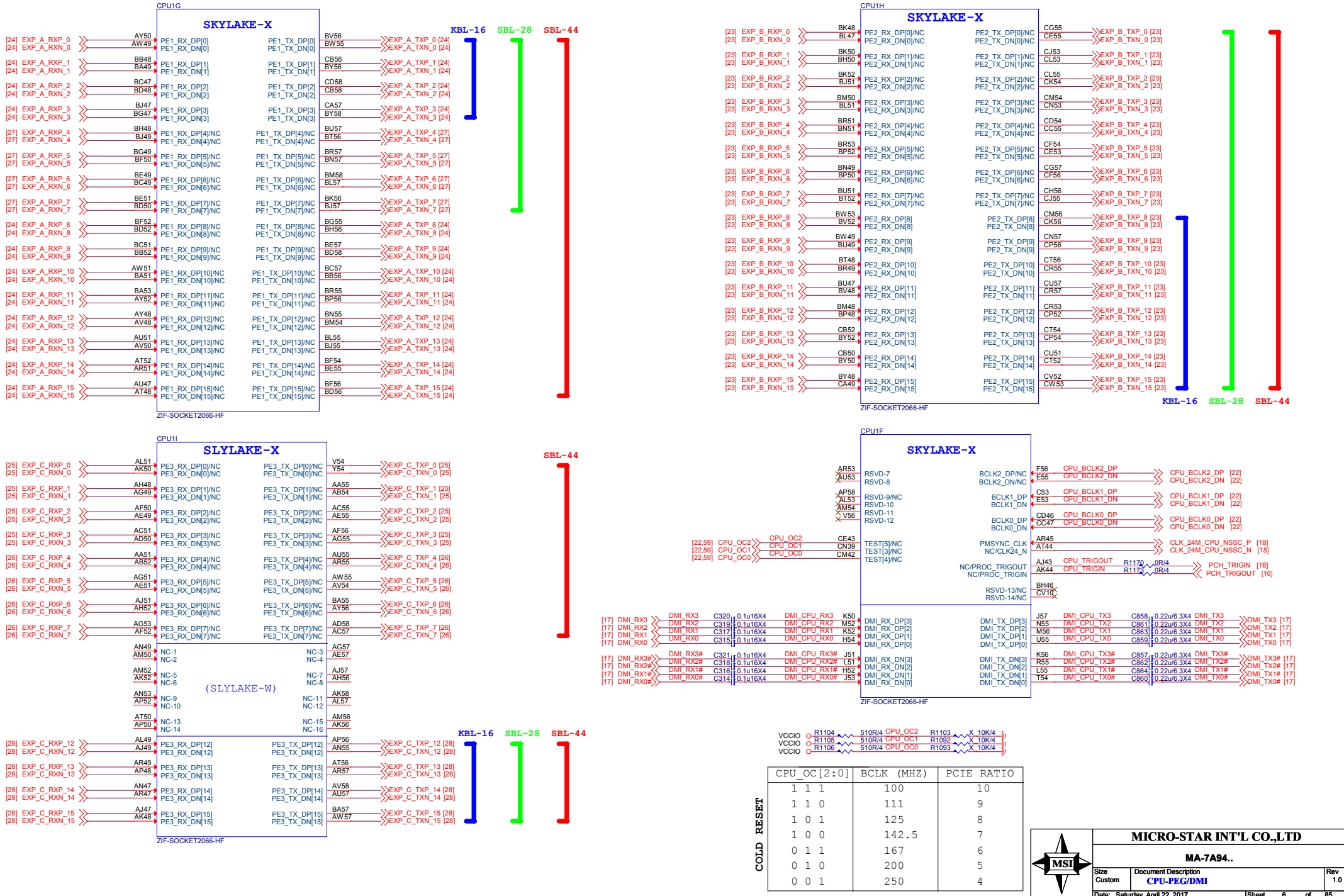
CPU1G
SKYLAKE-X
ZIF-SOCKET2066-HF
KBL-16
SBL-28
SBL-44
CPU1H
SKYLAKE-X
ZIF-SOCKET2066-HF
KBL-16
SBL-28
SBL-44
CPU1I
SLYLAKE-X
(SLYLAKE-W)
ZIF-SOCKET2066-HF
SBL-44
KBL-16
SBL-28
SBL-44
CPU1F
SKYLAKE-X
ZIF-SOCKET2066-HF
VCCIO
VCCIO
VCCIO
COLD RESET
CPU_OC[2:0] | BCLK (MHZ) | PCIE RATIO
1 1 1 | 100 | 10
1 1 0 | 111 | 9
1 0 1 | 125 | 8
1 0 0 | 142.5 | 7
0 1 1 | 167 | 6
0 1 0 | 200 | 5
0 0 1 | 250 | 4
MICRO-STAR INT'L CO.,LTD
MA-7A94..
Size Custom
Document Description CPU-PEG/DMI
Rev 1.0
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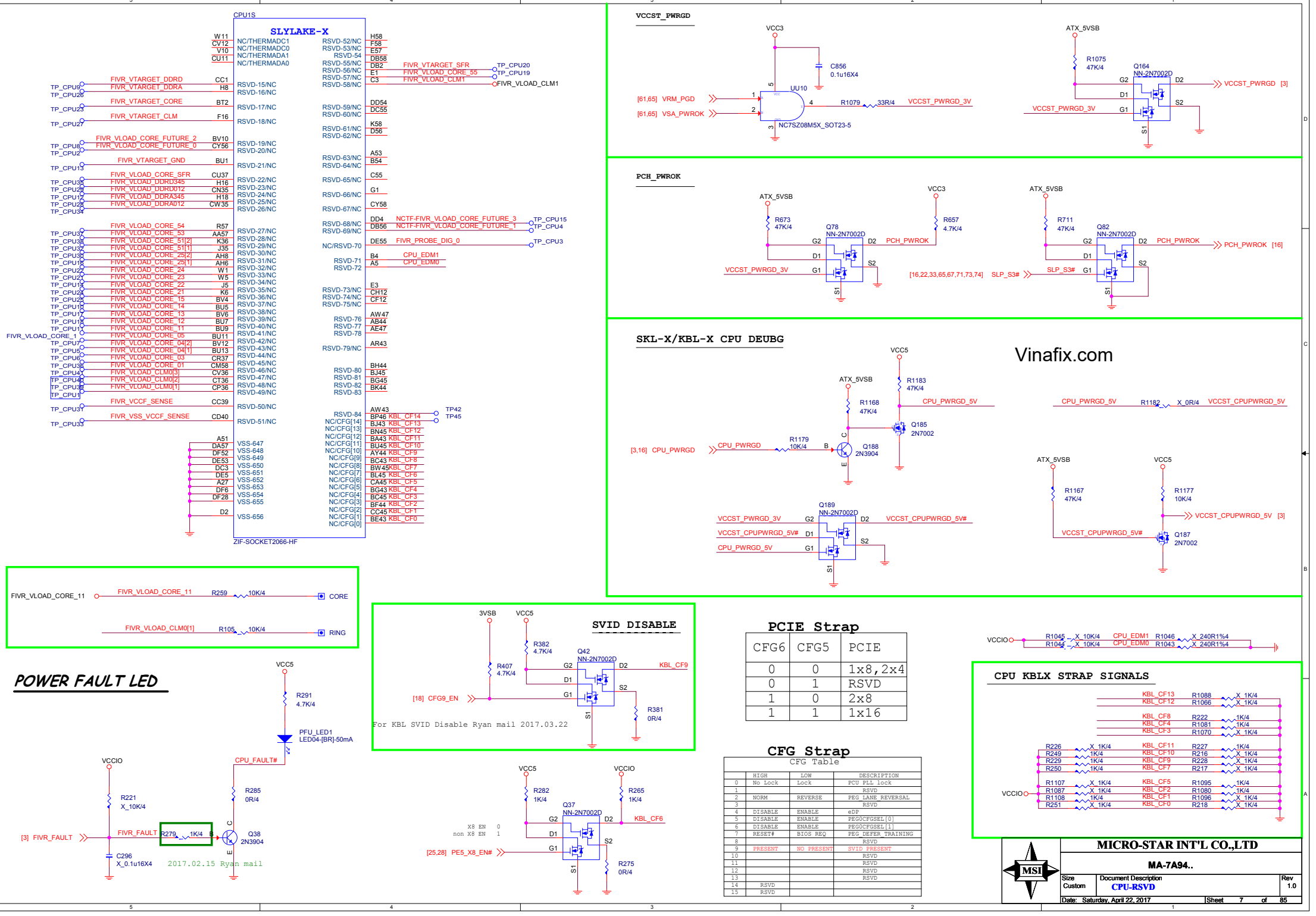
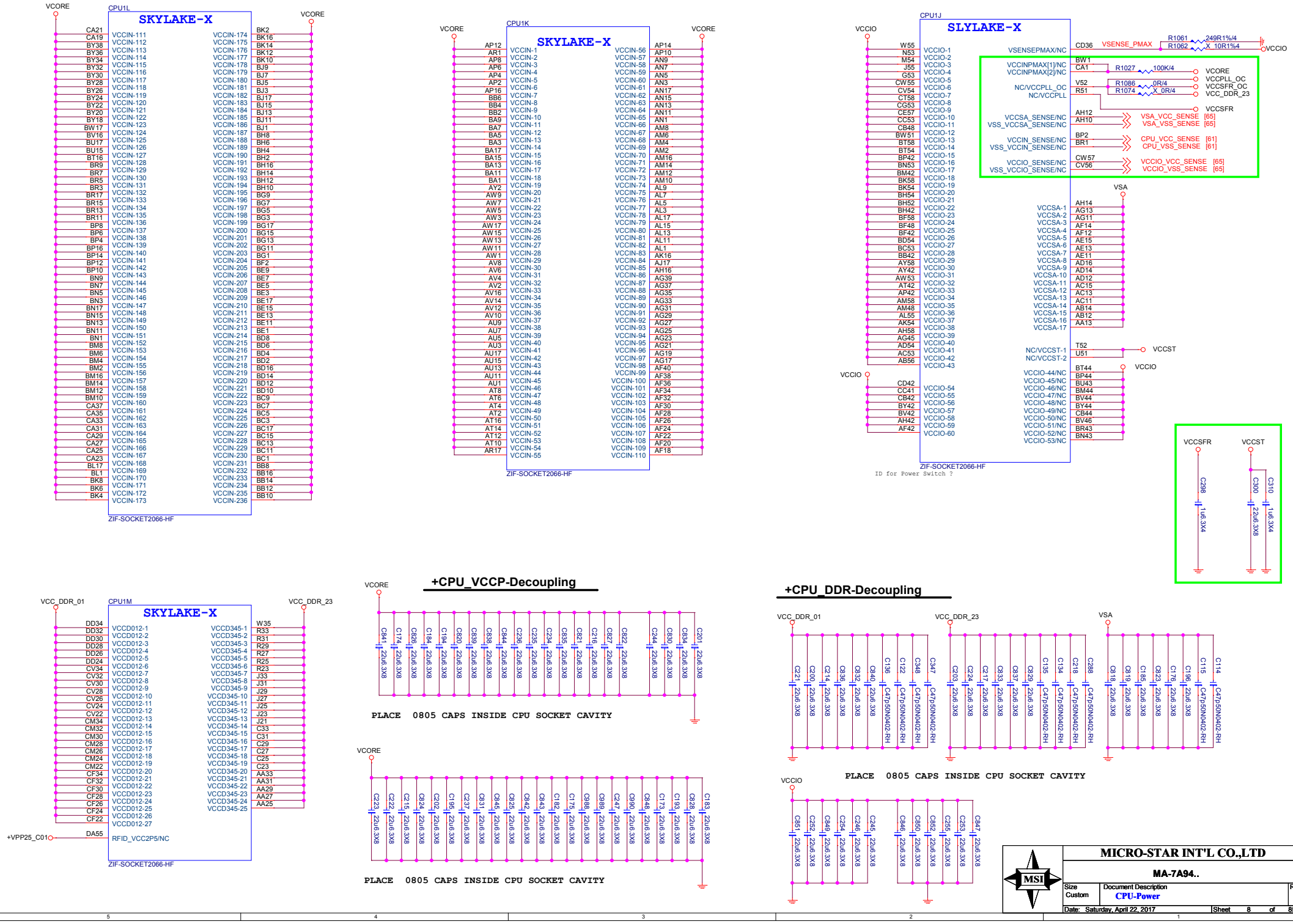


CFG6	CFG5	PCIE
0	0	1x8,2x4
0	1	RSVD
1	0	2x8
1	1	1x16

	HIGH	LOW	DESCRIPTION
0	No Lock	Lock	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG LANE REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET#	BIOS REQ	PEG DEFER TRAINING
8			RSVD
9	PRESENT	NO PRESENT	SVID PRESENT
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14	RSVD		
15	RSVD		


CPU1L
SKYLAKE-X
ZIF-SOCKET2066-HF
CPU1K
SKYLAKE-X
ZIF-SOCKET2066-HF
CPU1J
SLYLAKE-X
ZIF-SOCKET2066-HF
ID for Power Switch ?
CPU1M
SKYLAKE-X
ZIF-SOCKET2066-HF
+CPU_VCCP-Decoupling
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY
+CPU_DDR-Decoupling
PLACE 0805 CAPS INSIDE CPU SOCKET CAVITY
MICRO-STAR INT'L CO.,LTD
MA-7A94..
CPU-Power
Rev 1.0
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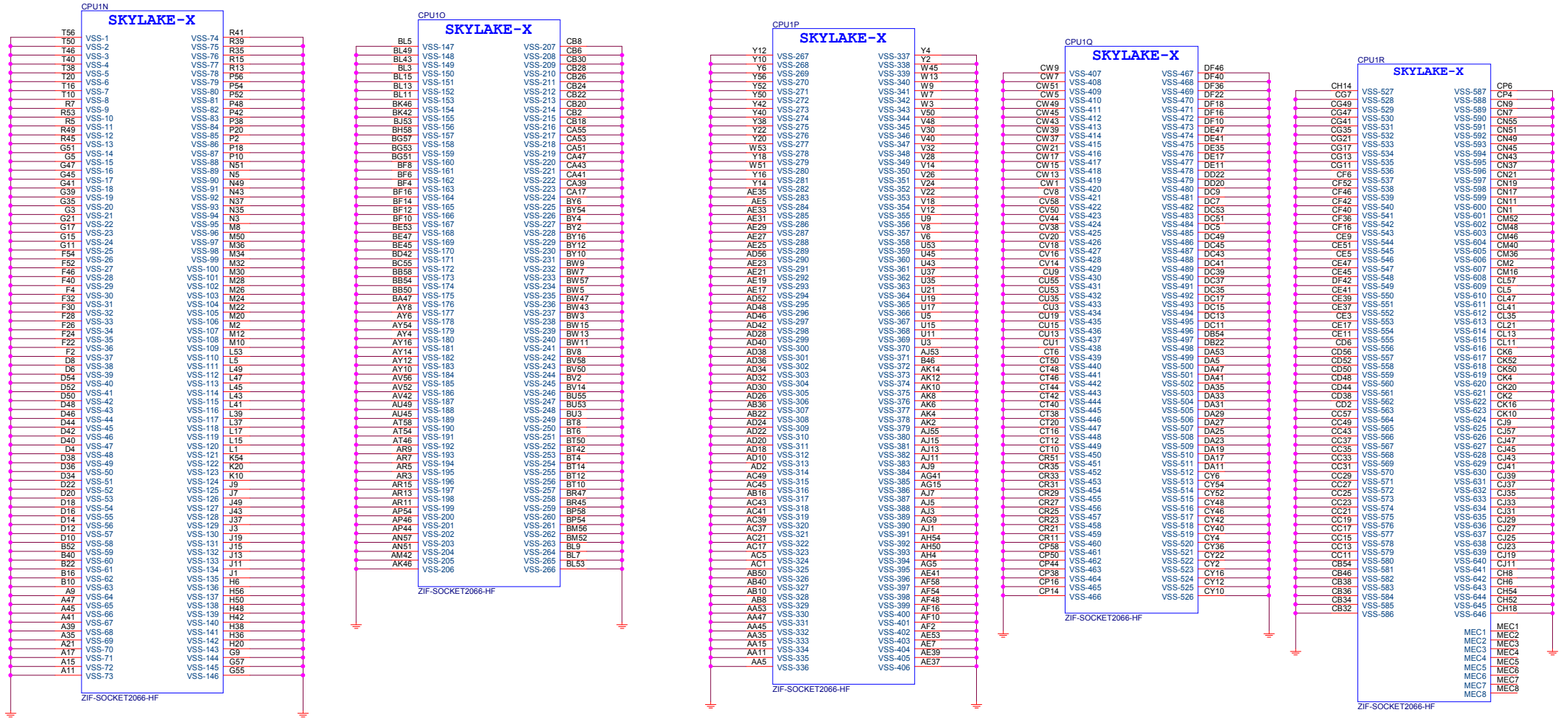

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MSI	MICRO-STAR INT'L CO.,LTD	
	MA-7A94..	
Size: Custom	Document Description: CPU-GND	Rev: 1.0
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DDR IV DIMM1/2

2017.02.13 Ryan mail
DQS9~17P PU to VCC_DDR

DIMMA1

DIMM1(CHANNEL-A0)
ADDRESS = 0:0:0 [SA2:SA1:SA0]

DIMM1 CH0 ADDRESS HEX:0

DIMMA2

DIMM2(CHANNEL-A1)
ADDRESS = 0:0:1 [SA2:SA1:SA0]

DIMM1 CH0 ADDRESS HEX:2

DDRIV-288P_BLACK-RH-33

PCA9617ADPJ_TSSOP8-RH

F-SPR-P260T-2.6A

MICRO-STAR INT'L CO.,LTD

MA-7A94..

Size	Document Description	Rev
Custom	DDR IV DIMM1/2	1.0

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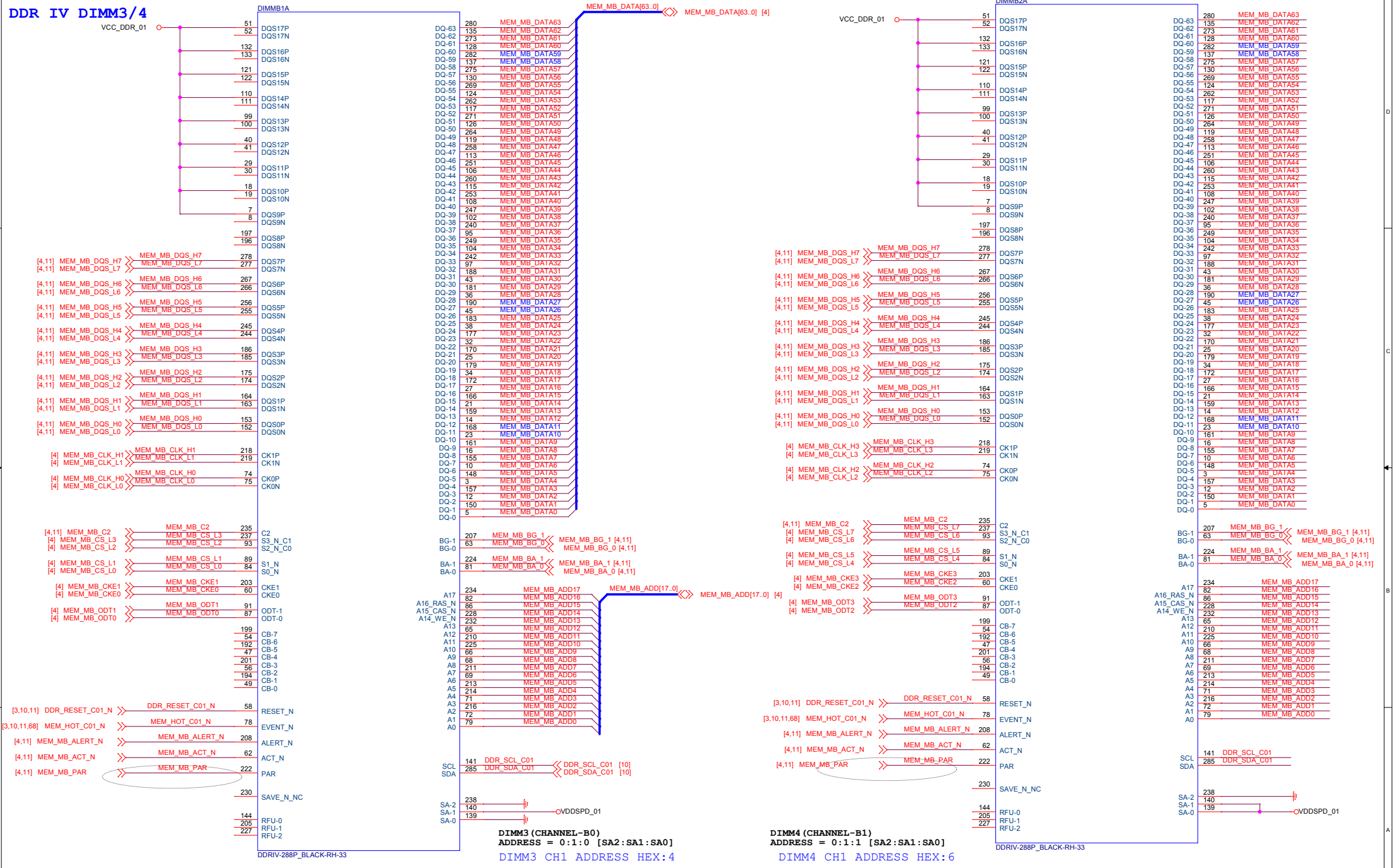
DDR IV DIMM3/4



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MA-7A94..		
Size: Custom	Document Description: DDR IV DIMM3/4	Rev: 1.0
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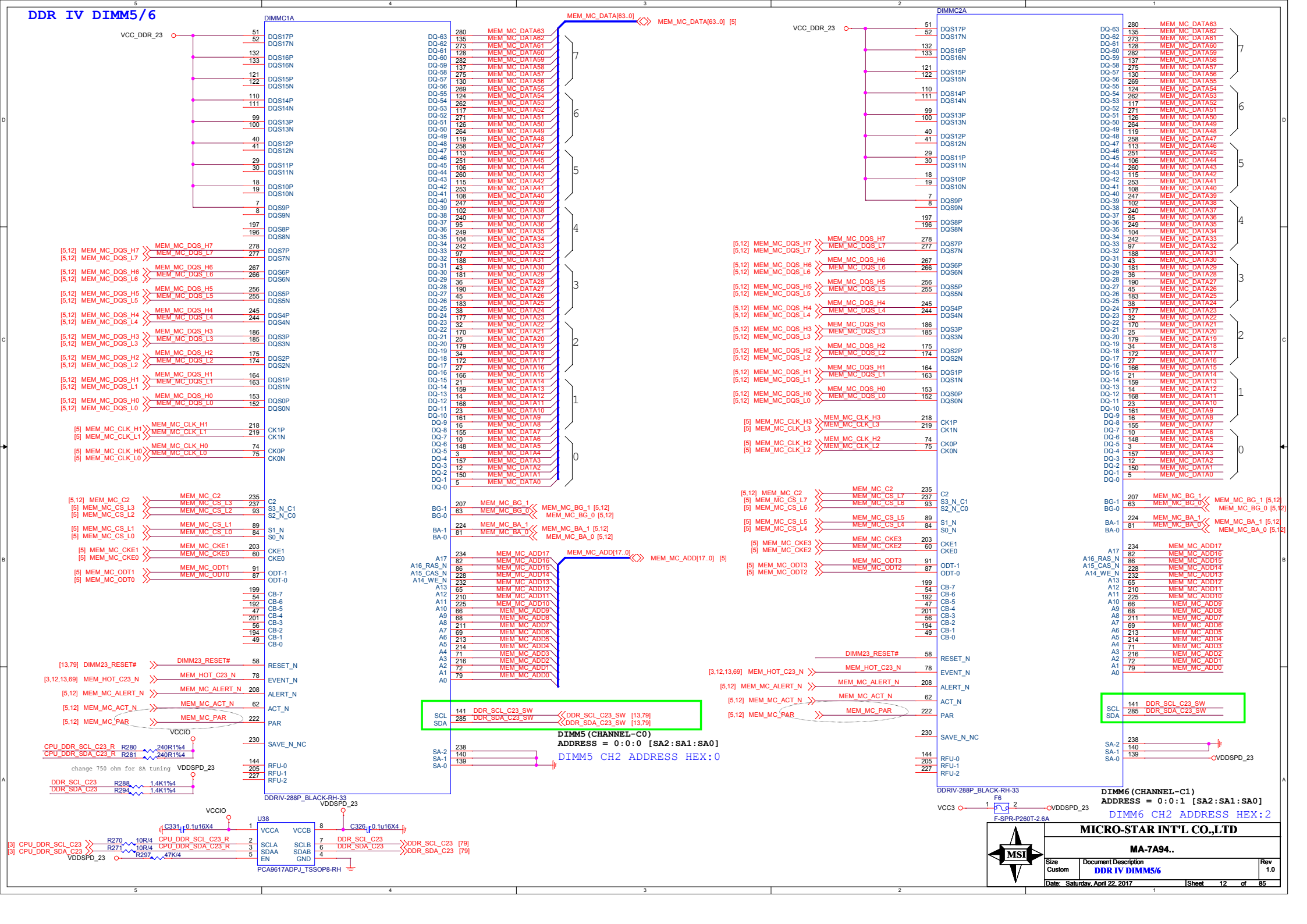
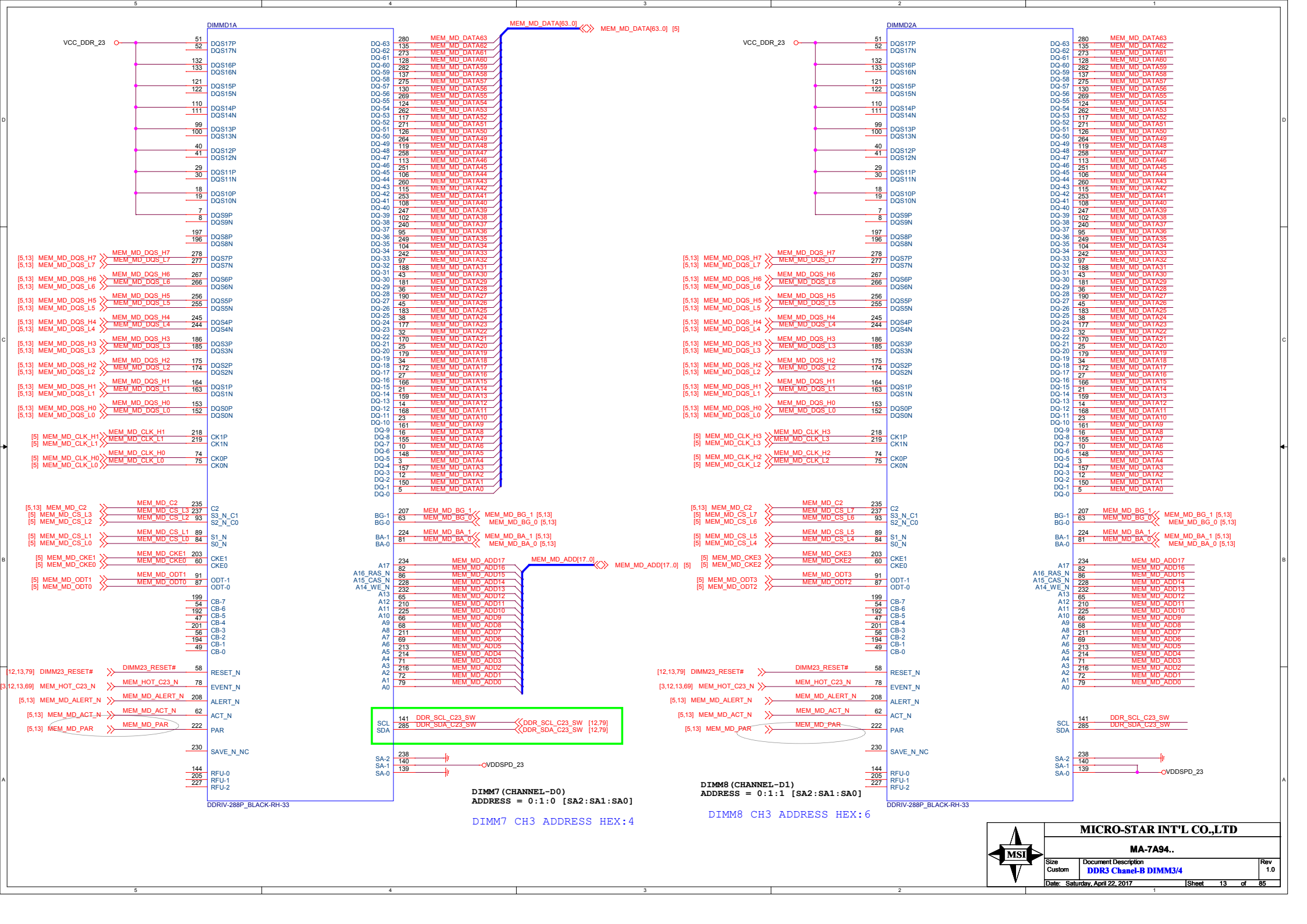
DDR IV DIMM5/6




DIMMD1A
DDRIV-288P_BLACK-RH-33
DIMMD2A
DDRIV-288P_BLACK-RH-33
MEM_MD_DATA[63..0]
MEM_MD_DATA[63..0] [5]
MEM_MD_ADD[17..0]
MEM_MD_ADD[17..0] [5]
VCC_DDR_23
VDDSPD_23
DIMM7(CHANNEL-D0)
ADDRESS = 0:1:0 [SA2:SA1:SA0]
DIMM7 CH3 ADDRESS HEX:4
DIMM8(CHANNEL-D1)
ADDRESS = 0:1:1 [SA2:SA1:SA0]
DIMM8 CH3 ADDRESS HEX:6
MICRO-STAR INT'L CO.,LTD
MA-7A94..
Size
Custom
Document Description
DDR3 Chanel-B DIMM3/4
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1.0
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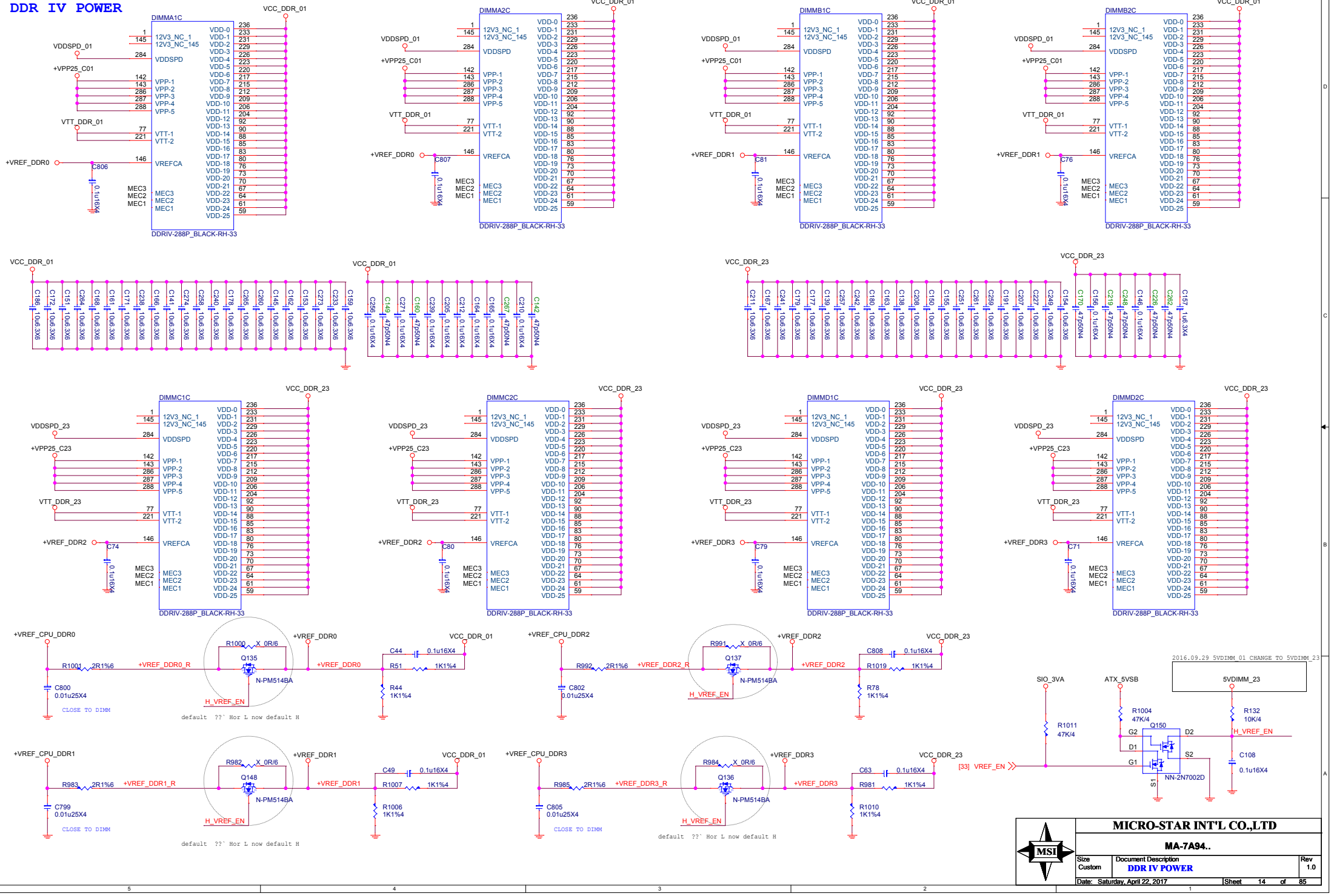
DDR IV POWER



MICRO-STAR INT'L CO.,LTD		
MA-7A94..		
Size: Custom	Document Description: DDR IV POWER	Rev: 1.0
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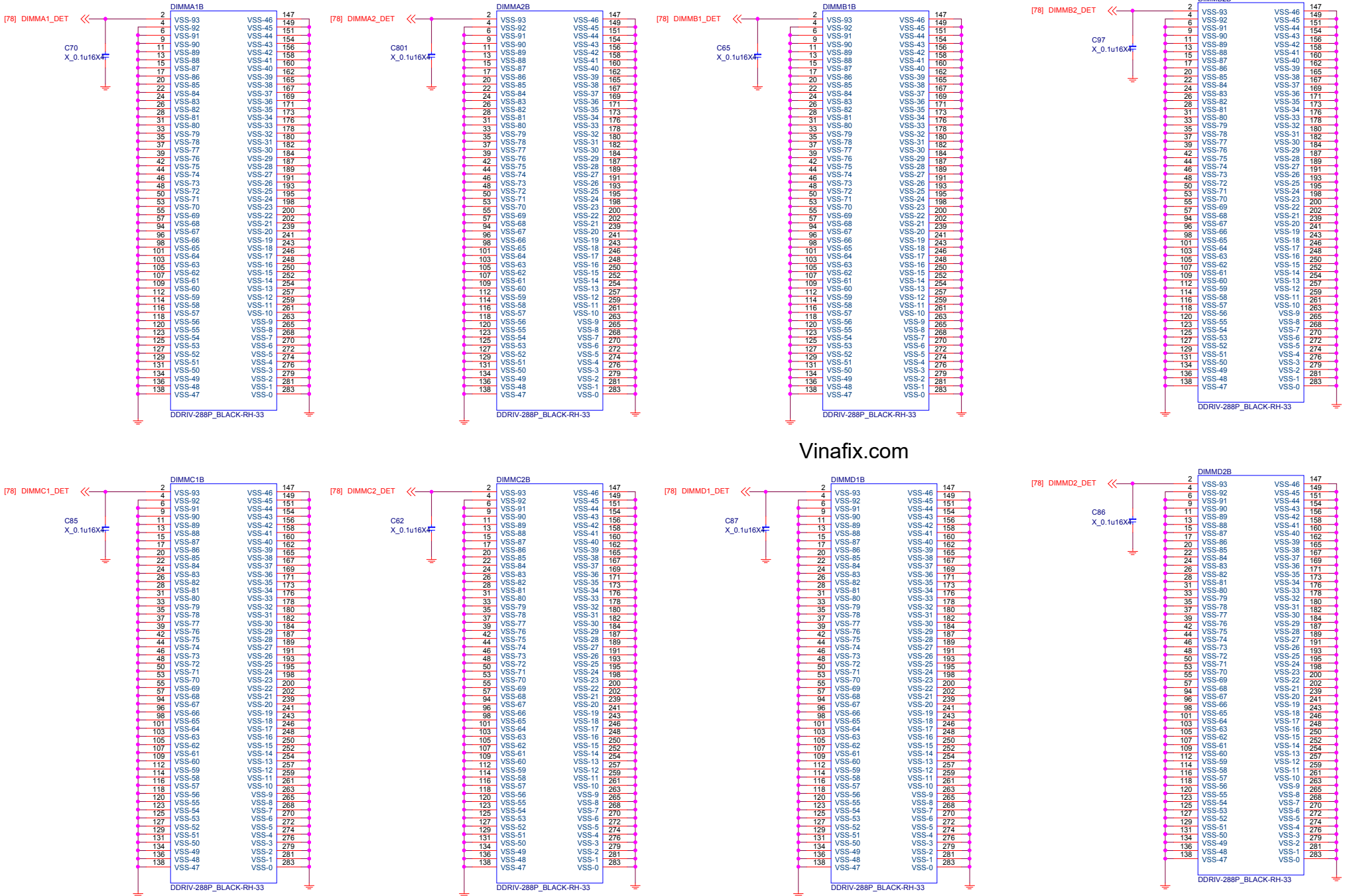
DDR IV GND



MICRO-STAR INT'L CO.,LTD	
MA-7A94..	
Size: Custom	Document Description: DDR IV GND
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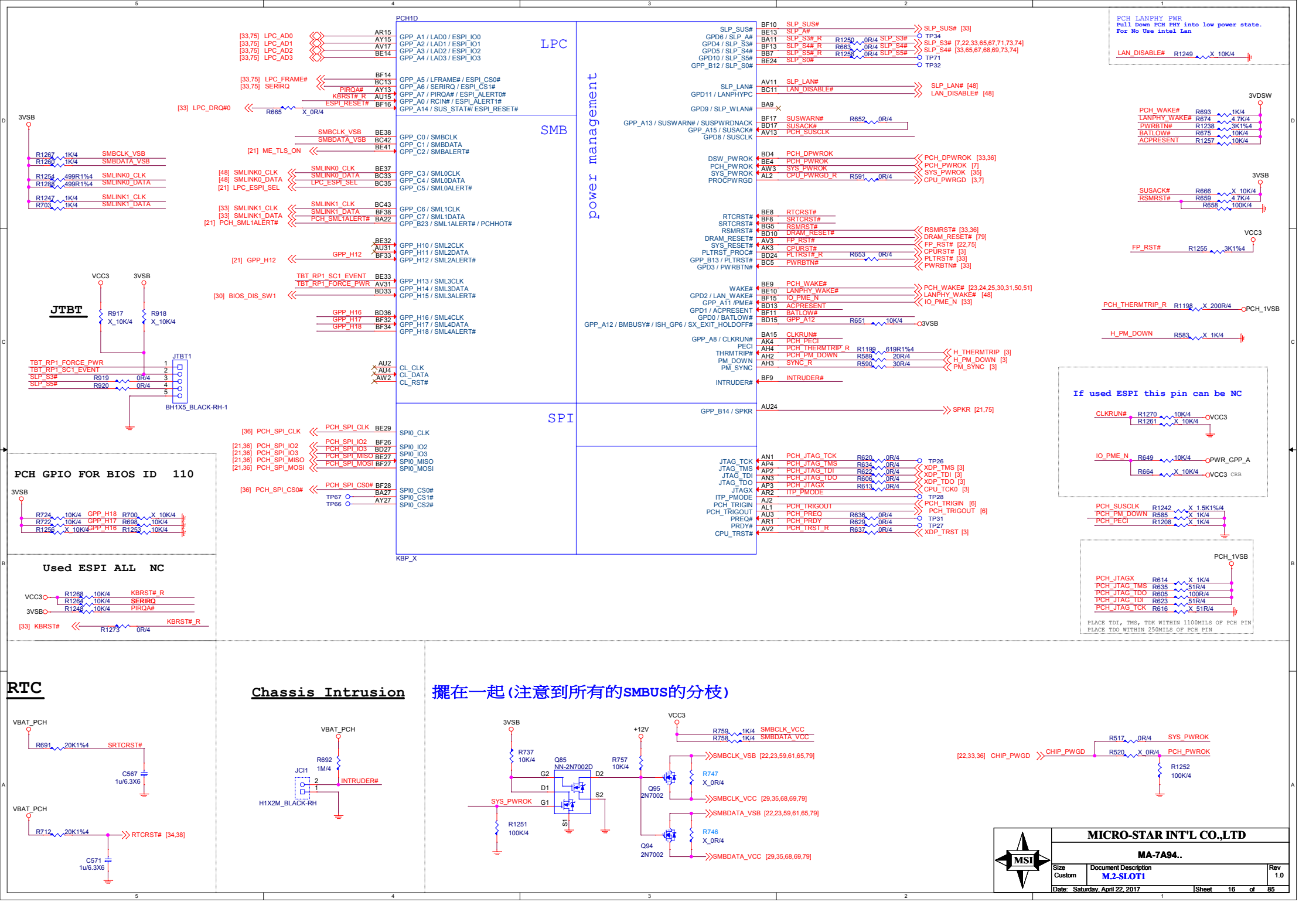
PCH1D
LPC
SMB
SPI
power management
GPP_A1 / LAD0 / ESPI_IO0
GPP_A2 / LAD1 / ESPI_IO1
GPP_A3 / LAD2 / ESPI_IO2
GPP_A4 / LAD3 / ESPI_IO3
GPP_A5 / LFRAME# / ESPI_CS0#
GPP_A6 / SERIRQ / ESPI_CS1#
GPP_A7 / PIRQA# / ESPI_ALERT0#
GPP_A0 / RCIN# / ESPI_ALERT1#
GPP_A14 / SUS_STAT# / ESPI_RESET#
GPP_C0 / SMBCLK
GPP_C1 / SMBDATA
GPP_C2 / SMBALERT#
GPP_C3 / SML0CLK
GPP_C4 / SML0DATA
GPP_C5 / SML0ALERT#
GPP_C6 / SML1CLK
GPP_C7 / SML1DATA
GPP_B23 / SML1ALERT# / PCHHOT#
GPP_H10 / SML2CLK
GPP_H11 / SML2DATA
GPP_H12 / SML2ALERT#
GPP_H13 / SML3CLK
GPP_H14 / SML3DATA
GPP_H15 / SML3ALERT#
GPP_H16 / SML4CLK
GPP_H17 / SML4DATA
GPP_H18 / SML4ALERT#
SPI0_CLK
SPI0_IO2
SPI0_IO3
SPI0_MISO
SPI0_MOSI
SPI0_CS0#
SPI0_CS1#
SPI0_CS2#
KBP_X
SLP_SUS#
GPD6 / SLP_A#
GPD4 / SLP_S3#
GPD5 / SLP_S4#
GPD10 / SLP_S5#
GPP_B12 / SLP_S0#
SLP_LAN#
GPD11 / LANPHYPC
GPD9 / SLP_WLAN#
GPP_A13 / SUSWARN# / SUSPWRDNACK
GPP_A15 / SUSACK#
GPD8 / SUSCLK
DSW_PWROK
PCH_PWROK
SYS_PWROK
PROCPWRGD
RTCRST#
SRTCRST#
RSMRST#
DRAM_RESET#
SYS_RESET#
PLTRST_PROC#
GPP_B13 / PLTRST#
GPD3 / PWRBTN#
WAKE#
GPD2 / LAN_WAKE#
GPP_A11 /PME#
GPD1 / ACPRESENT
GPD0 / BATLOW#
GPP_A12 / BMBUSY# / ISH_GP6 / SX_EXIT_HOLDOFF#
GPP_A8 / CLKRUN#
PECI
THRMTRIP#
PM_DOWN
PM_SYNC
INTRUDER#
GPP_B14 / SPKR
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAGX
ITP_PMODE
PCH_TRIGIN
PCH_TRIGOUT
PREQ#
PRDY#
CPU_TRST#
PCH_LANPHY_PWR
Pull Down PCH PHY into low power state.
For No Use intel Lan
LAN_DISABLE# R1249 X_10K/4
3VDSW
PCH_WAKE# R693 1K/4
LANPHY_WAKE# R674 4.7K/4
PWRBTN# R1238 3K1%4
BATLOW# R675 10K/4
ACPRESENT R1257 10K/4
3VSB
SUSACK# R666 X_10K/4
RSMRST# R659 4.7K/4
R658 100K/4
VCC3
FP_RST# R1255 3K1%4
PCH_THERMTRIP_R R1198 X_200R/4 PCH_1VSB
H_PM_DOWN R583 X_1K/4
If used ESPI this pin can be NC
CLKRUN# R1270 10K/4 VCC3
R1261 X_10K/4
IO_PME_N R649 10K/4 PWR_GPP_A
R664 X_10K/4 VCC3 CRB
PCH_SUSCLK R1242 X_1.5K1%/4
PCH_PM_DOWN R585 X_1K/4
PCH_PECI R1208 X_1K/4
PCH_1VSB
PCH_JTAGX R614 X_1K/4
PCH_JTAG_TMS R635 51R/4
PCH_JTAG_TDO R605 100R/4
PCH_JTAG_TDI R623 51R/4
PCH_JTAG_TCK R616 X_51R/4
PLACE TDI, TMS, TDK WITHIN 1100MILS OF PCH PIN
PLACE TDO WITHIN 250MILS OF PCH PIN
JTBT
JTBT1
BH1X5_BLACK-RH-1
PCH GPIO FOR BIOS ID 110
Used ESPI ALL NC
RTC
VBAT_PCH
SRTCRST#
RTCRST# [34,38]
Chassis Intrusion
H1X2M_BLACK-RH
INTRUDER#
擺在一起(注意到所有的SMBUS的分枝)
SMBCLK_VSB [22,23,59,61,65,79]
SMBDATA_VSB [22,23,59,61,65,79]
SMBCLK_VCC [29,35,68,69,79]
SMBDATA_VCC [29,35,68,69,79]
Q85 NN-2N7002D
Q95 2N7002
Q94 2N7002
SYS_PWROK
CHIP_PWGD
PCH_PWROK
MICRO-STAR INT'L CO.,LTD
MA-7A94..
Size Custom
Document Description M.2-SLOT1
Rev 1.0
Date: Saturday, April 22, 2017
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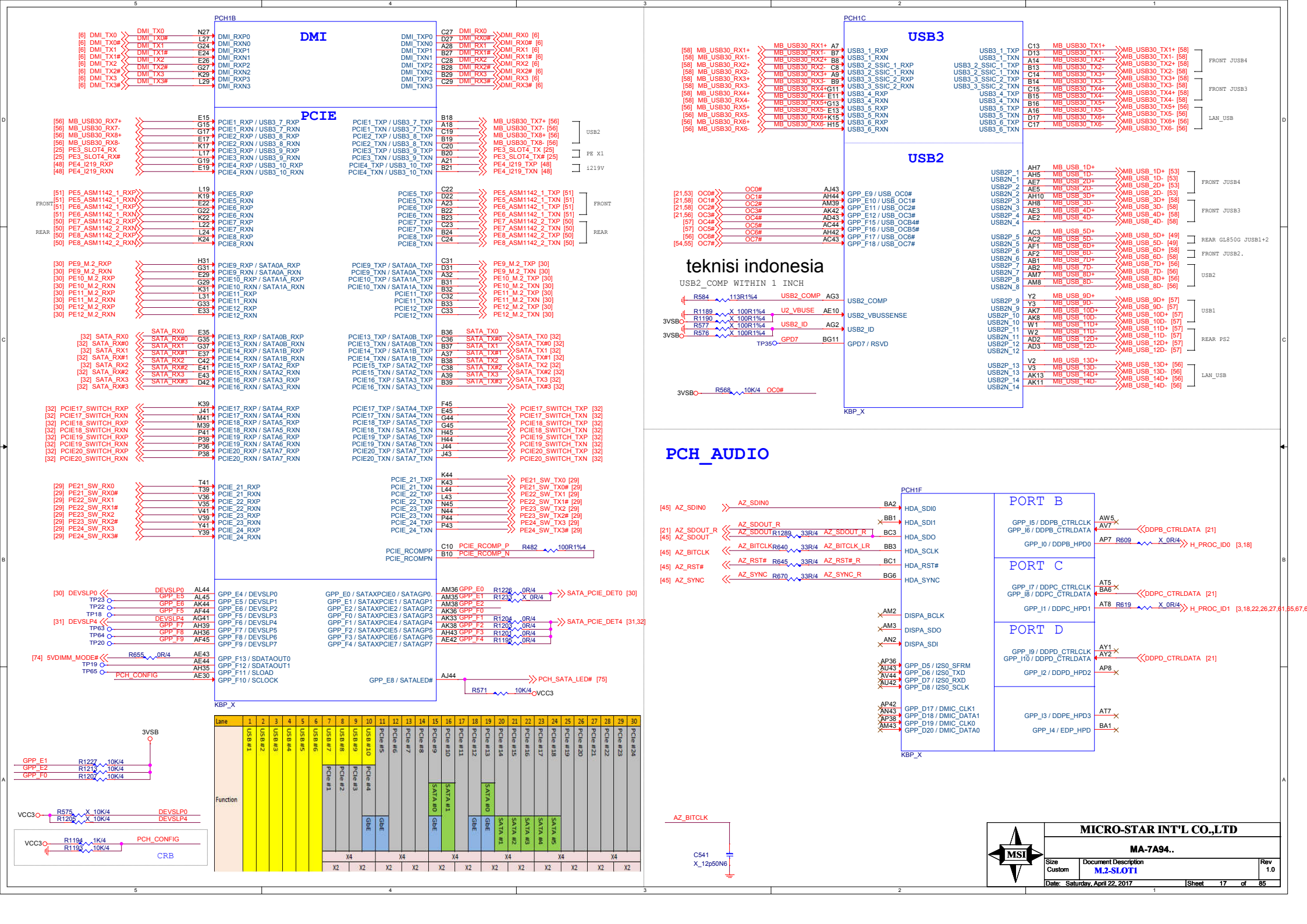
PCH1B
DMI
PCIE
KBP_X
PCH1C
USB3
USB2
KBP_X
teknisi indonesia
USB2_COMP WITHIN 1 INCH
PCH_AUDIO
PCH1F
PORT B
PORT C
PORT D
KBP_X
Lane
Function
USB #1
USB #2
USB #3
USB #4
USB #5
USB #6
USB #7
USB #8
USB #9
USB #10
PCIe #1
PCIe #2
PCIe #3
PCIe #4
PCIe #5
PCIe #6
PCIe #7
PCIe #8
PCIe #9
PCIe #10
PCIe #11
PCIe #12
PCIe #13
PCIe #14
PCIe #15
PCIe #16
PCIe #17
PCIe #18
PCIe #19
PCIe #20
PCIe #21
PCIe #22
PCIe #23
PCIe #24
SATA #0
SATA #1
SATA #2
SATA #3
SATA #4
SATA #5
GbE
X4
X2
CRB
MICRO-STAR INT'L CO.,LTD
MA-7A94..
Size
Custom
Document Description
M.2-SLOT1
Rev
1.0
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PCH_CLK

Used ESPI(GPPA) GPIO Group A will be come 1.8V leve)

2017.03.24 Ryan mail

PCH1E

PCH1A

GPIO

LPC

RTC

24MHz

XCLK_BIASREF < 500 mil

2017.02.22 Rex mail change

teknisi indonesia

2017.02.21 For GL850G

KBP_X

Close to PCH

W/ SMI/NMI Funtion
GPP_B[23,20,14]
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]

BOM ID

CLK GEN	R220 unstuff	R227 unstuff
HOTKEY	Stuff	Stuff

0716

GPI GPP_D21
HIGH : A0,A1 Version FOR ASM2142
LOW : Furture Version FOR ASM2142

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Size: Custom | Document Description: M.2-SLOT1 | Rev: 1.0

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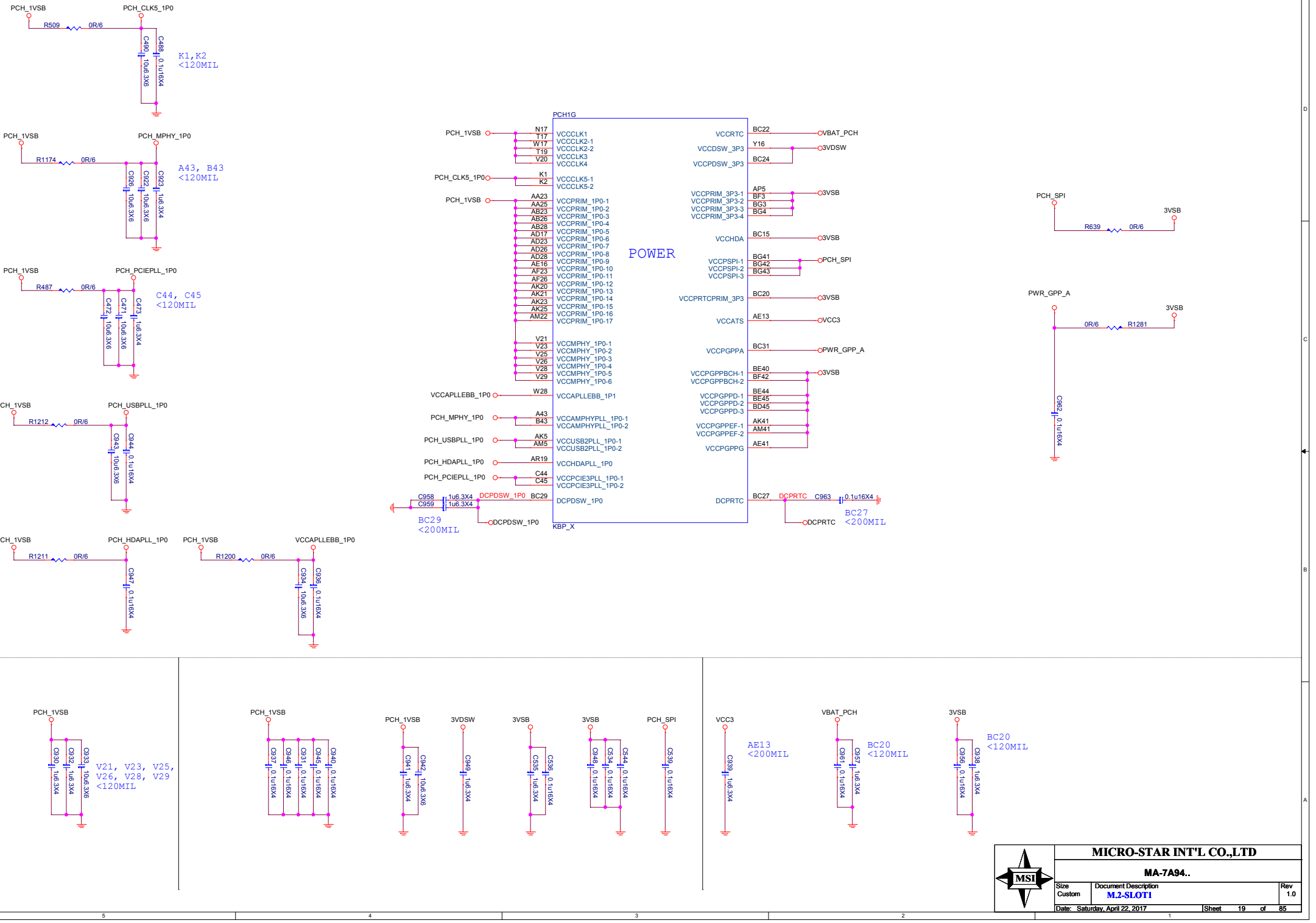

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MA-7A94..

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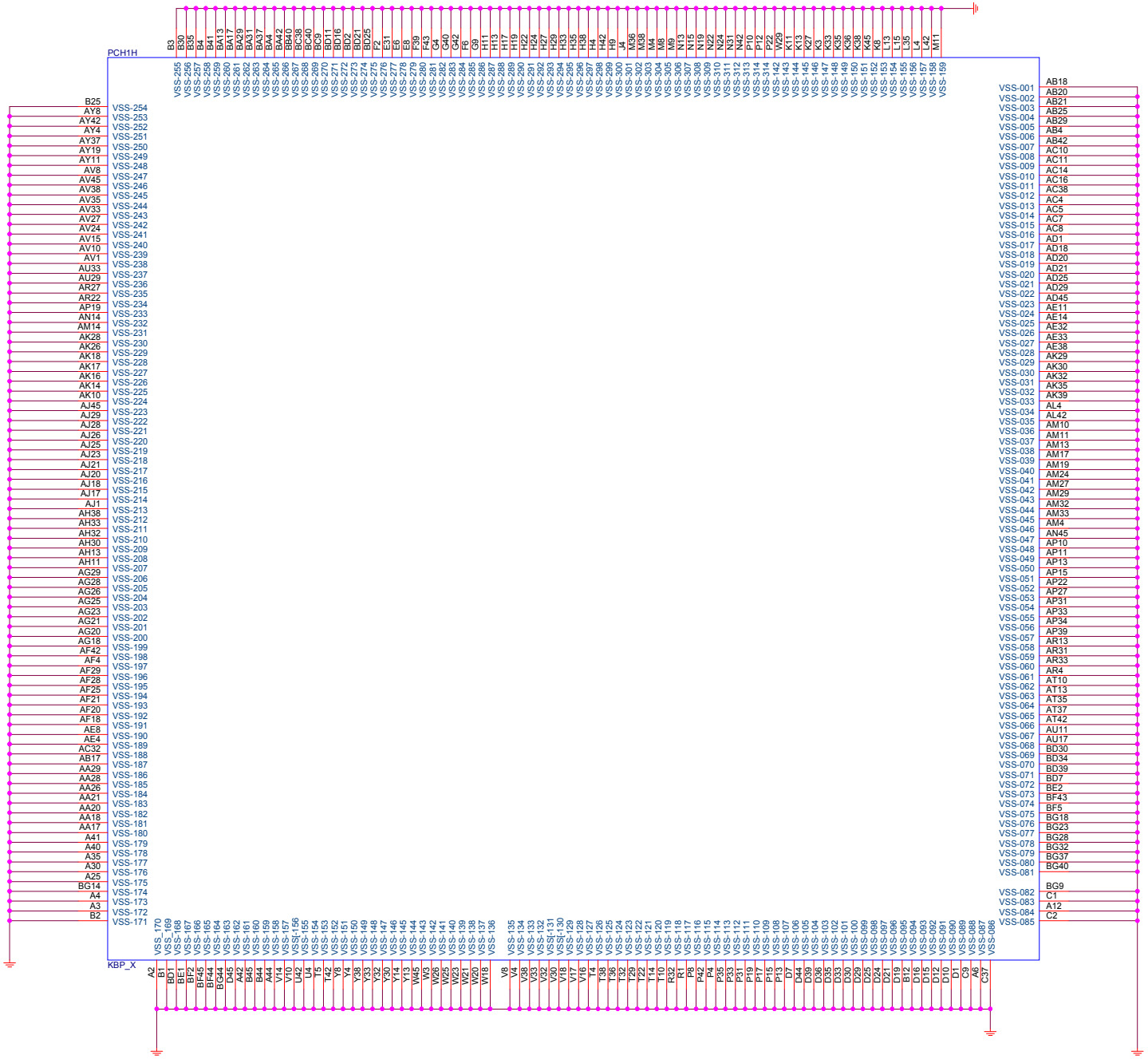
Vinafix.com



MICRO-STAR INT'L CO.,LTD			
MA-7A94..			
Size: Custom	Document Description: M.2-SLOT1		Rev: 1.0
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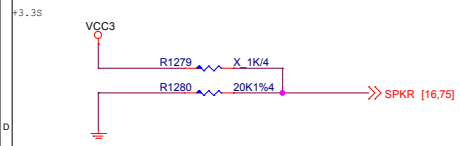
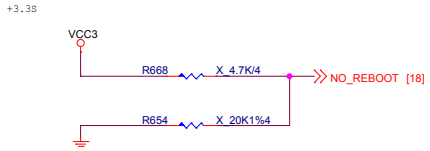
TOP SWAP OVERRIDE STRAP



HIGH: TOP_SWAP ENABLED
LOW : TOP_SWAP DISABLED

PCH HAS INTERNAL WEAK PD

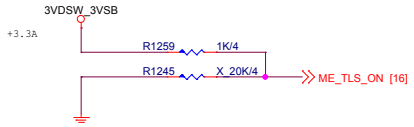
No Reboot OPTION



0 : NO-REBOOT (Default)
1 : REBOOT

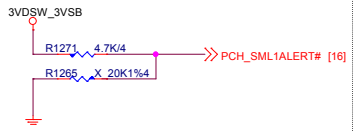
PCH HAS INTERNAL WEAK PD

AMT and SBA with confidentiality



0 : DISABLE
1 : ENABLE (Default)

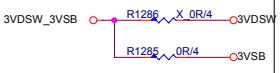
DCI ENABLE



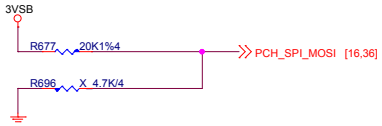
0 : DCI DISABLE
1 : DCI ENABLE (Default)

PCH HAS INTERNAL WEAK PD

CRB

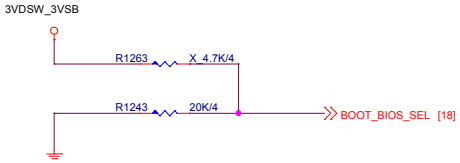


Booot-HALT SEL STRAP



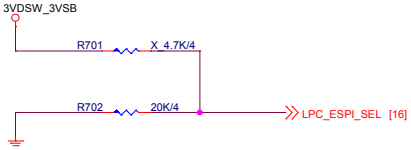
PCH HAS INTERNAL WEAK PU

Boot BIOS



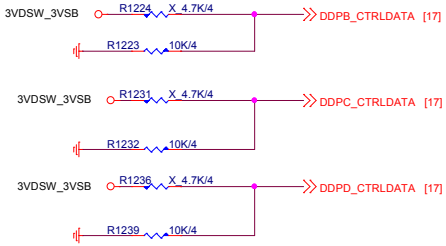
0 : SPI
1 : LPC

LPC eSPI Mode



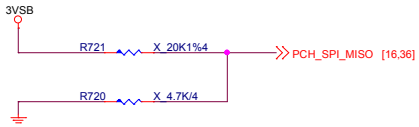
0 : LPC
1 : eSPI

DISPLAY PORT



0 : DISPLAY NOT DETECTED (Default)
1 : DISPLAY DETECTED

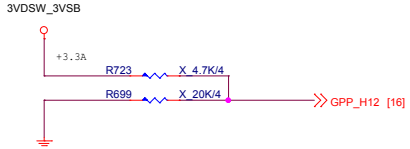
JTAG ODT SEL



HIGH: JTAG ODT ENABLED
LOW : JTAG ODT DISABLED

PCH HAS INTERNAL WEAK PU

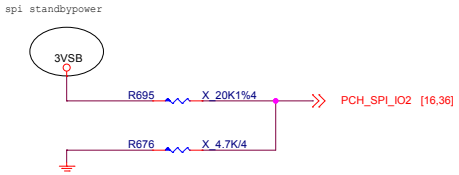
ESPI FLASH SHARING MODE



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

PCH HAS INTERNAL WEAK PD

CONSENT



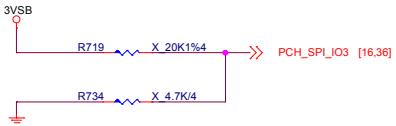
0 : CONSENT STRAP ENABLE
1 : CONSENT STRAP ENABLE

PCH HAS INTERNAL WEAK PU

DFX TEST MODE

UNSRTUFF: NORMAL
STUFF: TEST MODE

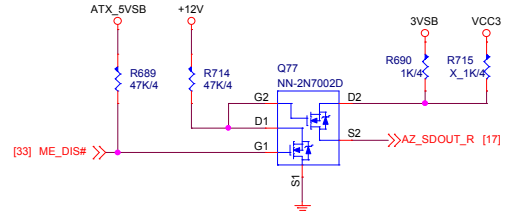
PERSONALITY



HIGH: PERSONALITY ENABLED
LOW : PERSONALITY DISABLED

PCH HAS INTERNAL WEAK PU

HDA_SDO

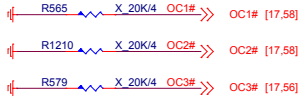


0 : SECURITY MEASURES OVERRIDEN
1 : SECURITY PER FLASH DESCRIPTOR

RING OSCILLATOR BYPASS (DFX)

0 : Ring Oscillator bypass
1 : Normal Mode

XTAL INPUT FREQUENCY [HVM MODE]



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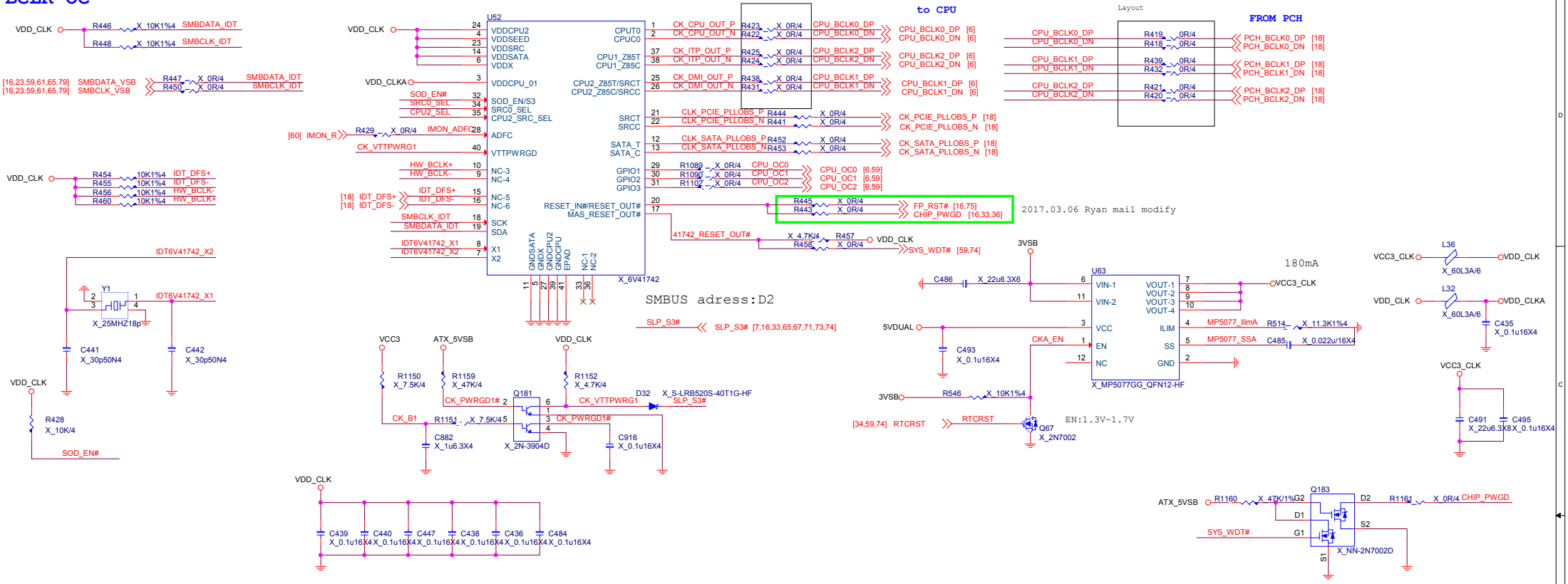
BCLK OC



SRC0_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

CPU2_SRC_SEL	Description	CPU	H_PROC_ID1
0	Source from CPUPLL	SKX	1
1	Source from PCIEPLL	KBX	0

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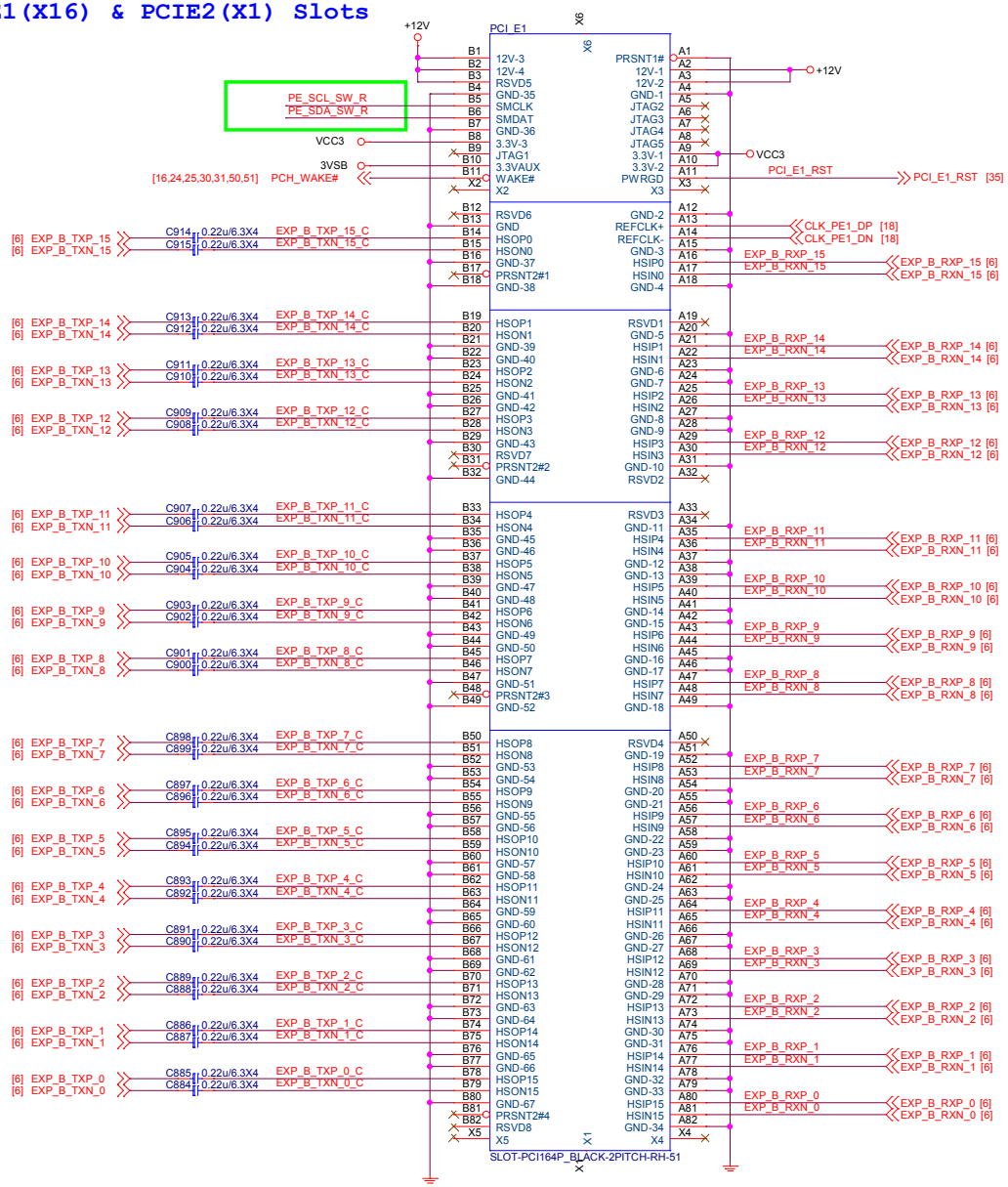
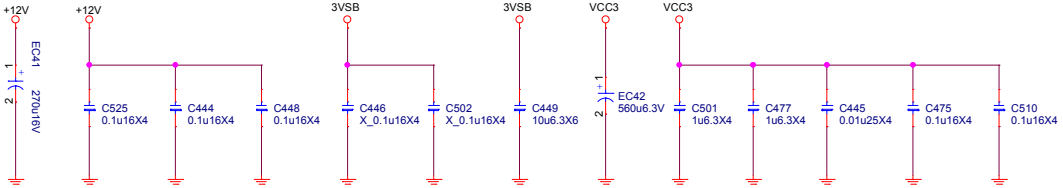
PCIE1(X16) & PCIE2(X1) Slots



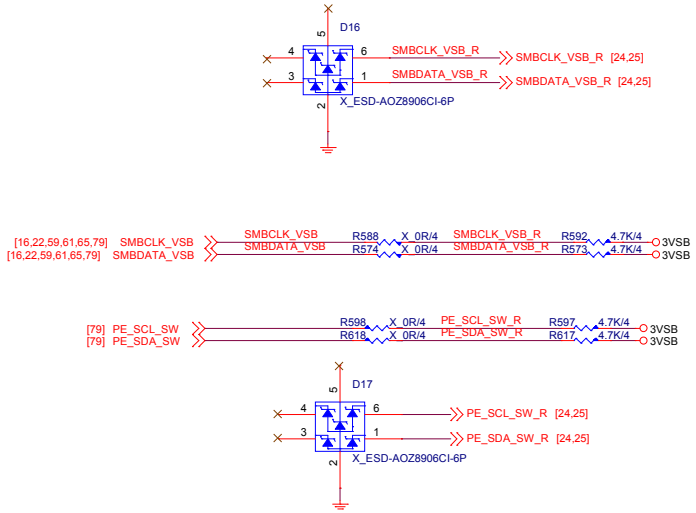


U1000

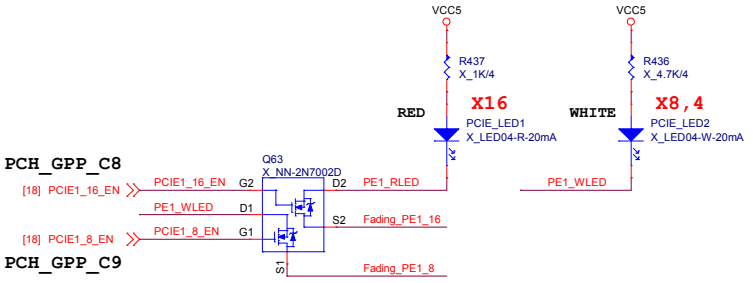
PCIE Slot S01

PCIE Slot S01

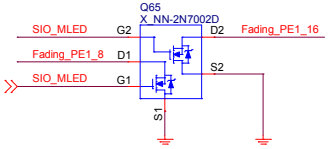
SMBUS ESD



PCIE SLOT LED



SIO PIN98



GPIO / LED	GPP_C8	GPP_C9
亮	GPO PO HIGH	GPO PO HIGH
滅	GPI (default LOW)	GPI (default LOW)

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MA-7A94..

Size	Document Description	Rev
Custom	PCIE1(X16)	1.0

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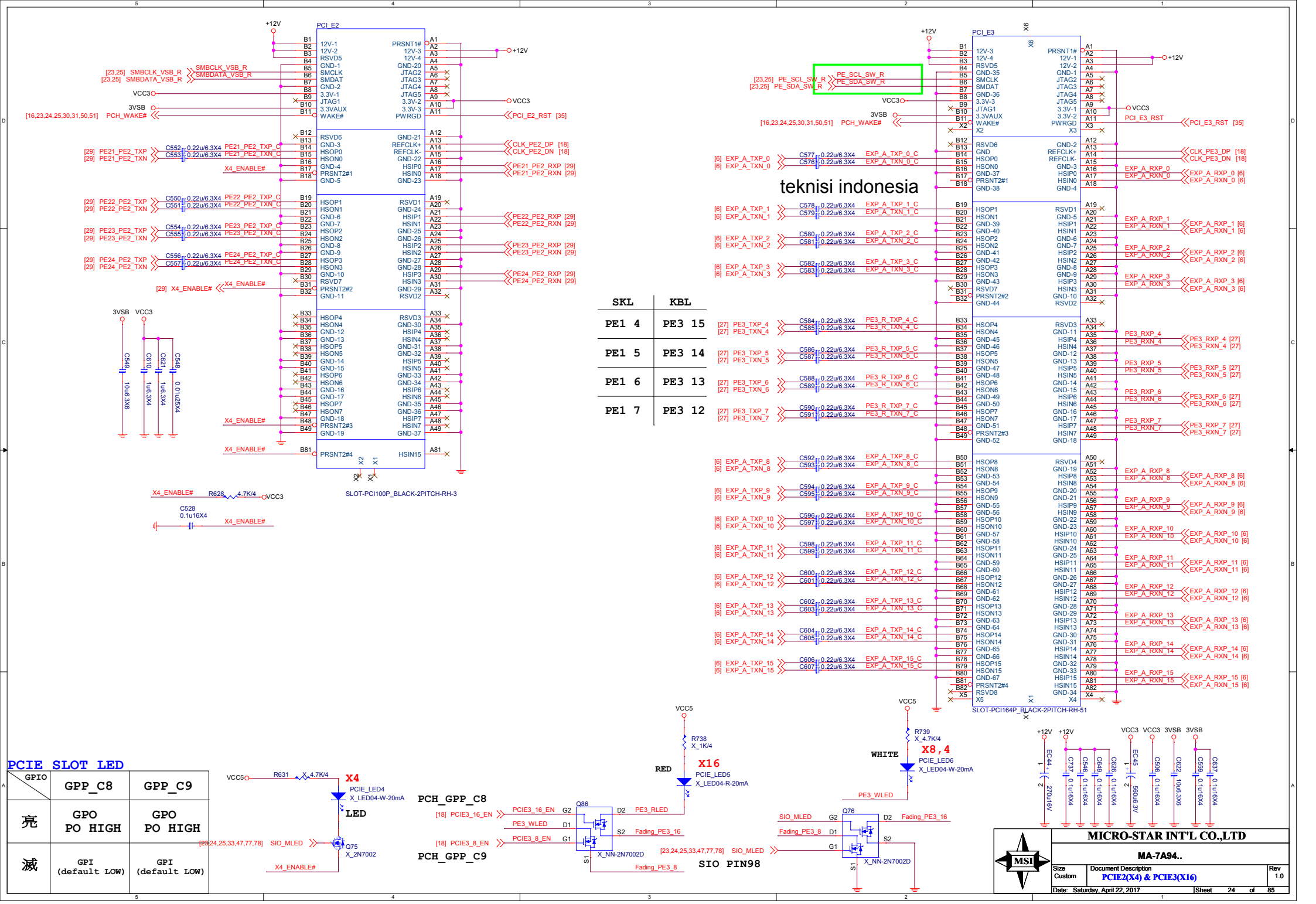
PCI_E2
SLOT-PCI100P_BLACK-2PITCH-RH-3
PCI_E3
SLOT-PCI164P_BLACK-2PITCH-RH-51
teknisi indonesia
SKL
KBL
PE1 4
PE3 15
PE1 5
PE3 14
PE1 6
PE3 13
PE1 7
PE3 12
PCIE SLOT LED
GPIO
GPP_C8
GPP_C9
亮
GPO PO HIGH
GPO PO HIGH
灭
GPI (default LOW)
GPI (default LOW)
PCH_GPP_C8
PCH_GPP_C9
SIO PIN98
RED
WHITE
LED
MICRO-STAR INT'L CO.,LTD
MA-7A94..
PCIE2(X4) & PCIE3(X16)
Rev 1.0
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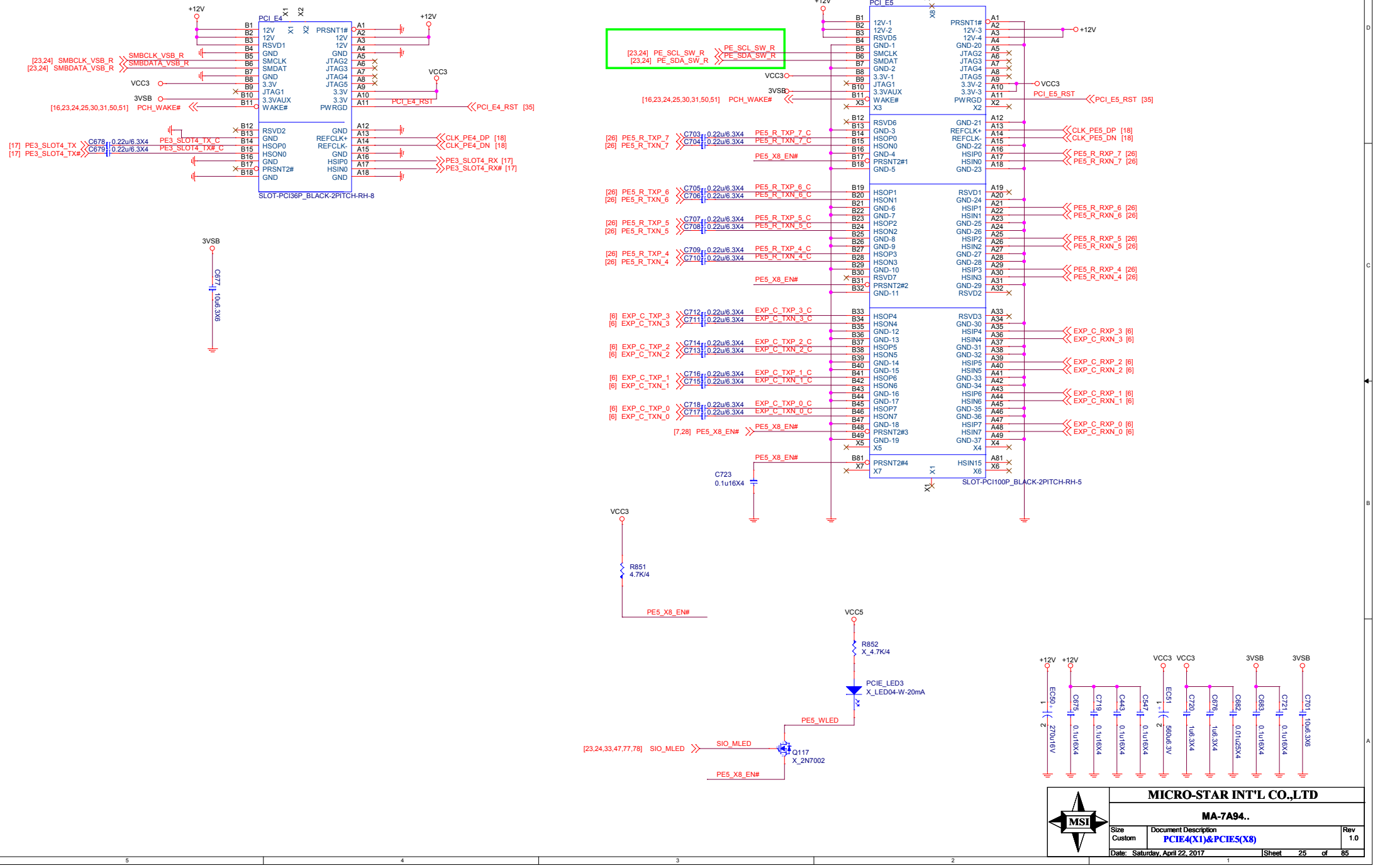

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Size: Custom	Document Description: PCIE4(X1)&PCIE5(X8)
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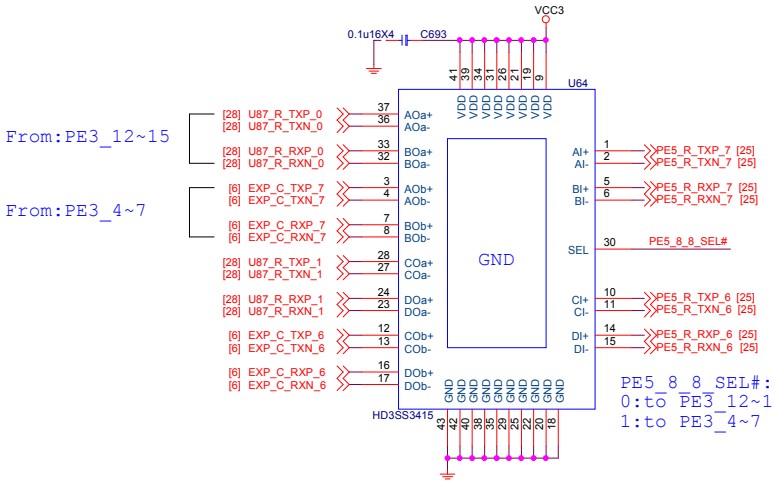
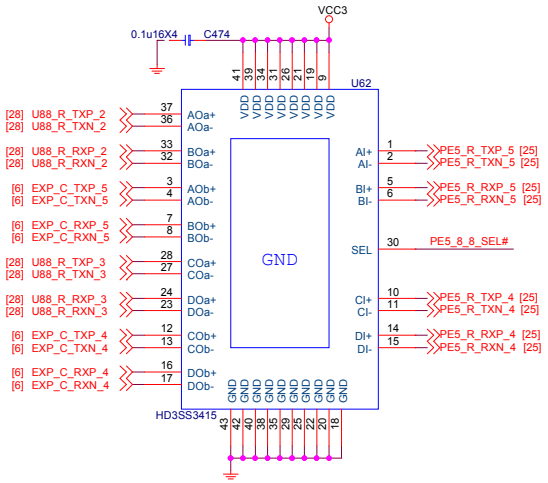
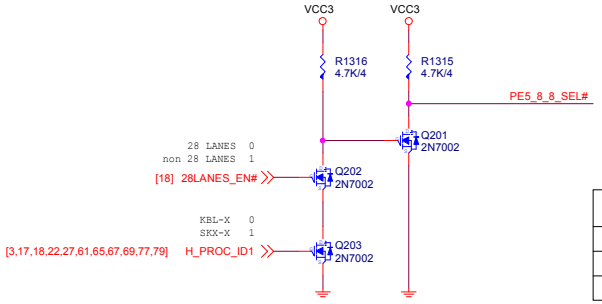
SEL:
0 : 28/16
1 : 44







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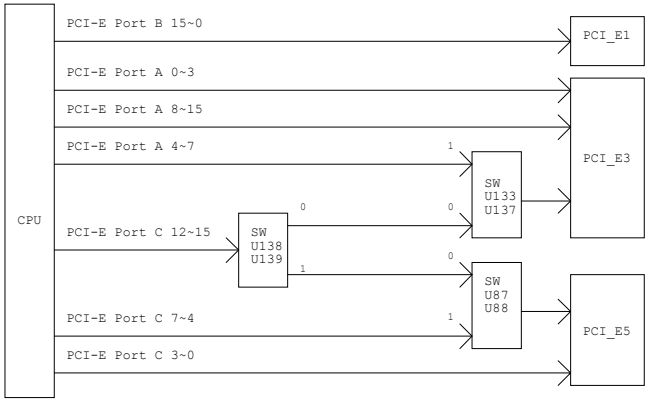
H_PROC_ID1	28LANES_EN#	PE5_8_8_SEL#	
1	1	1	44Lanes
1	0	0	28Lanes
0	1	0	16Lanes



	SKL-X 44L		SKL-X 28L		KBL-X			
PE1	X16:P2[15:0]		X16:P2[15:0]		X8:P2[15:8]		X8:P2[15:8]	
PE3	X16:P1[0:15]		X8:P1[0:7]		X4:P1[0:3]		X8:P2[0:3]+P3[15:12]	
PE5	X8:P3[7:0]		X4:P3[15:12]		X4:P3[15:12]		X0:	
PE4	PCH_PE3		PCH_PE3		PCH_PE3		PCH_PE3	
M2_1	PCH_PE9~12		PCH_PE9~12		PCH_PE9~12		PCH_PE9~12	
M2_2	PCH_PE17~20		PCH_PE17~20		PCH_PE17~20		PCH_PE17~20	
PE2	PCH_PE21~24	———	PCH_PE21~24	———	PCH	———	PCH	———
U.2	———	PCH_PE21~24	———	PCH_PE21~24	———	PCH	———	PCH

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Size	Document Description	Rev
Custom	PCIE-SWITCH	1.0

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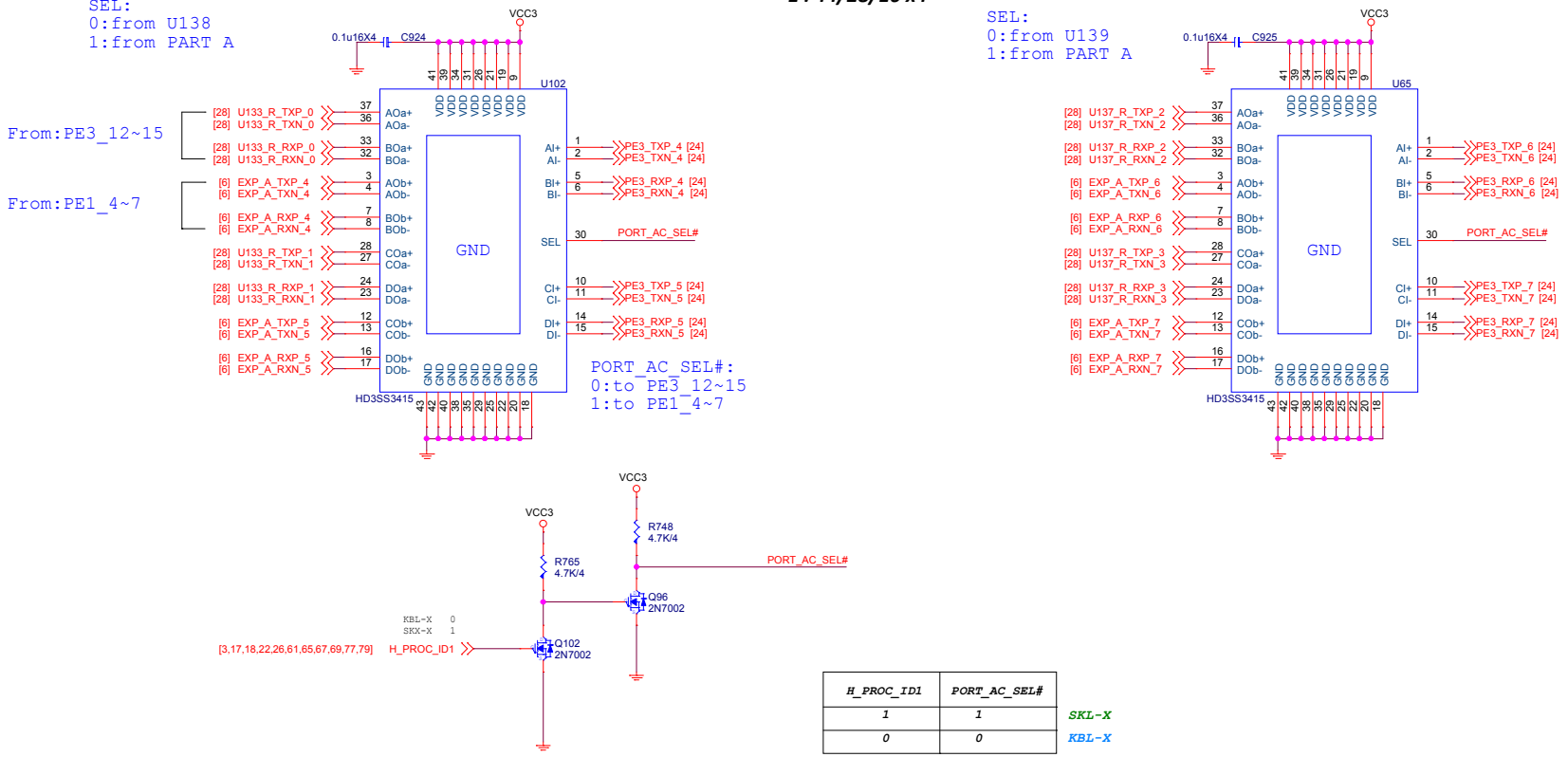
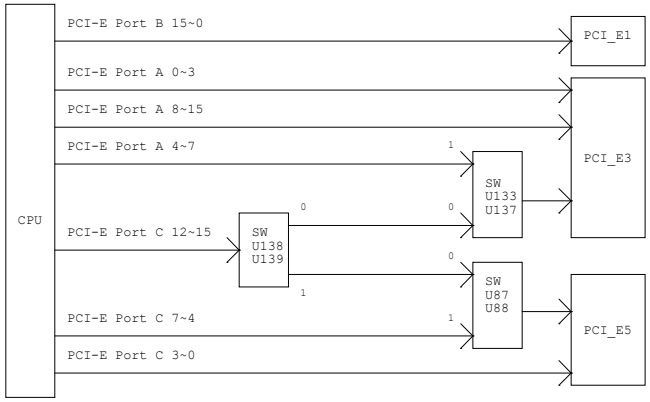


H_PROC_ID1	PORT_AC_SEL#	
1	1	SKL-X
0	0	KBL-X



	SKL-X 44L		SKL-X 28L		KBL-X			
PE1	X16:P2[15:0]		X16:P2[15:0]		X8:P2[15:8]		X8:P2[15:8]	
PE3	X16:P1[0:15]		X8:P1[0:7]		X4:P1[0:3]		X8:P2[0:3]+P3[15:12]	
PE5	X8:P3[7:0]		X4:P3[15:12]		X4:P3[15:12]		X0:	
PE4	PCH_PE3		PCH_PE3		PCH_PE3		PCH_PE3	
M2_1	PCH_PE9~12		PCH_PE9~12		PCH_PE9~12		PCH_PE9~12	
M2_2	PCH_PE17~20		PCH_PE17~20		PCH_PE17~20		PCH_PE17~20	
PE2	PCH_PE21~24	———	PCH_PE21~24	———	PCH	———	PCH	———
U.2	———	PCH_PE21~24	———	PCH_PE21~24	———	PCH	———	PCH

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MA-7A94..

Size	Document Description	Rev
Custom	PCIE-SWITCH	1.0

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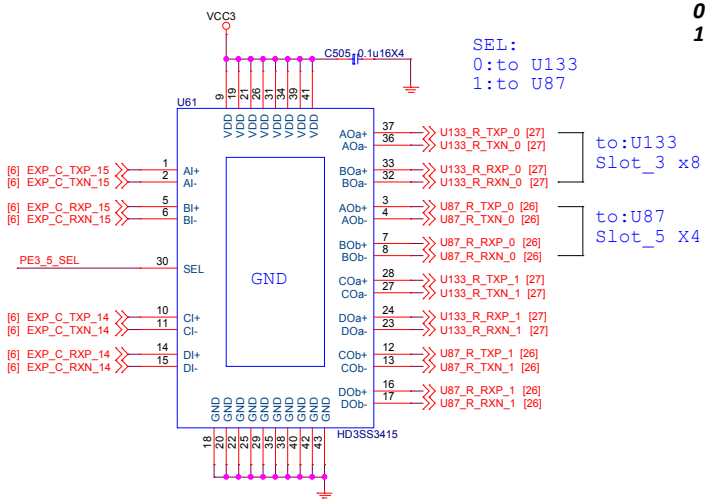
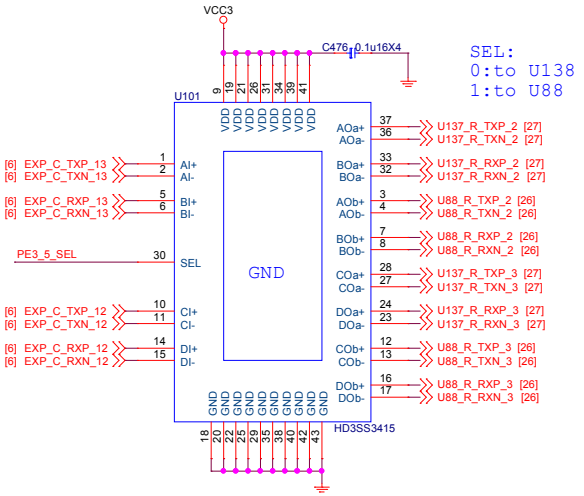
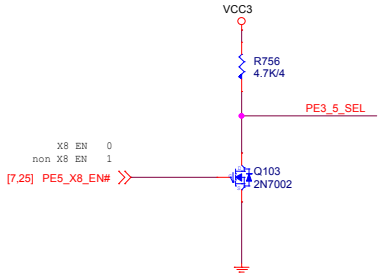


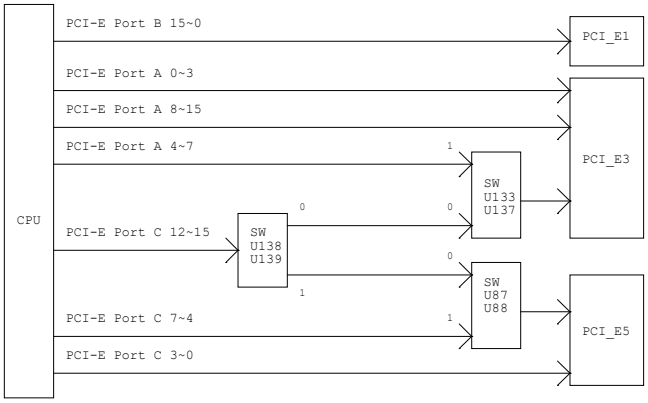
SEL:
0 : 44/28/16 x4
1 : 16 x8





PE5_X8_EN#	PE3_5_SEL
1	0
0	1

PE5 x4 in



	SKL-X 44L		SKL-X 28L		KBL-X			
PE1	X16:P2[15:0]		X16:P2[15:0]		X8:P2[15:8]		X8:P2[15:8]	
PE3	X16:P1[0:15]		X8:P1[0:7]		X4:P1[0:3]		X8:P2[0:3]+P3[15:12]	
PE5	X8:P3[7:0]		X4:P3[15:12]		X4:P3[15:12]		X0:	
PE4	PCH_PE3		PCH_PE3		PCH_PE3		PCH_PE3	
M2_1	PCH_PE9~12		PCH_PE9~12		PCH_PE9~12		PCH_PE9~12	
M2_2	PCH_PE17~20		PCH_PE17~20		PCH_PE17~20		PCH_PE17~20	
PE2	PCH_PE21~24	———	PCH_PE21~24	———	PCH	———	PCH	———
U.2	———	PCH_PE21~24	———	PCH_PE21~24	———	PCH	———	PCH

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Size: Custom | Document Description: SKX/KBX SWITCH | Rev: 1.0

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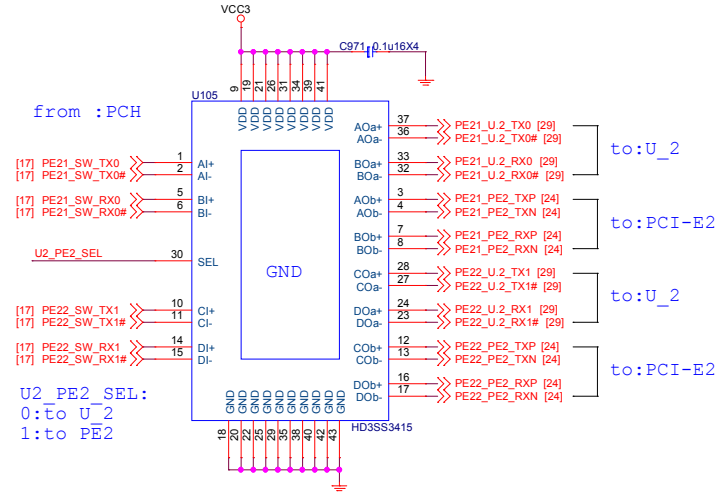

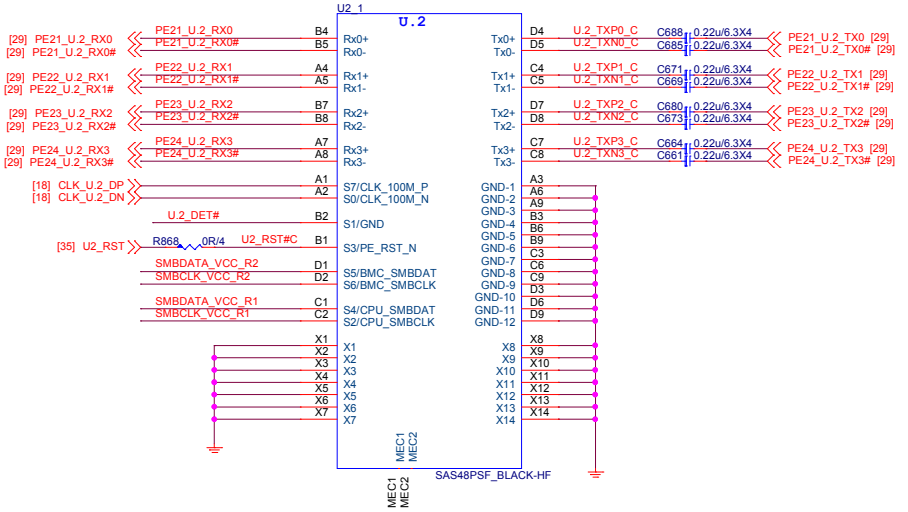

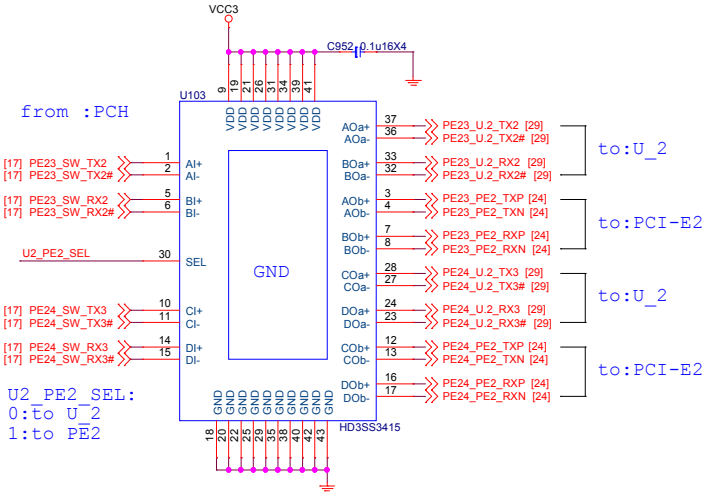

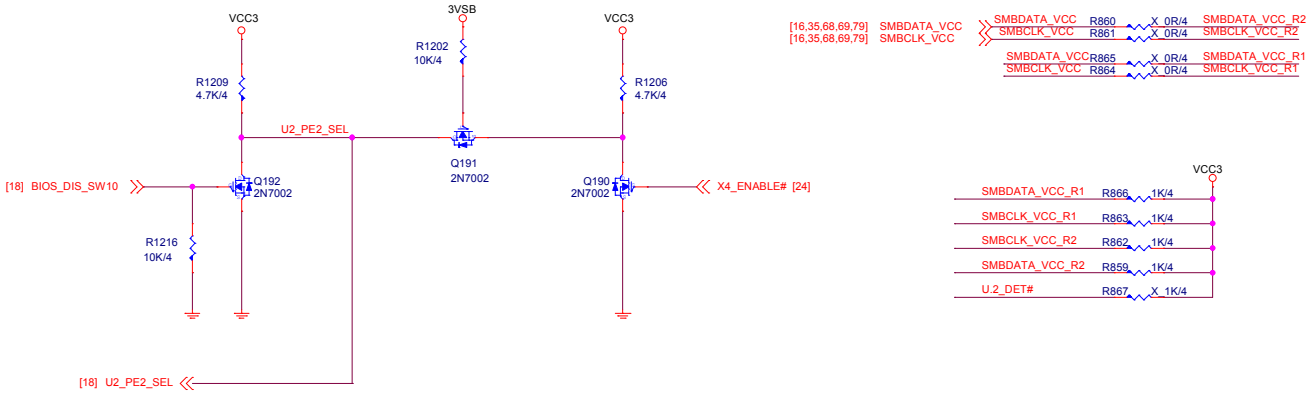

BIOS_DIS_SW10	
1	U2
default 0	PE2

X4_ENABLE#	U2_PE2_SEL	
1	0	
0	1	PE2 x4 in

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Size	Document Description	Rev
Custom	U2/PCH-SWITCH	1.0

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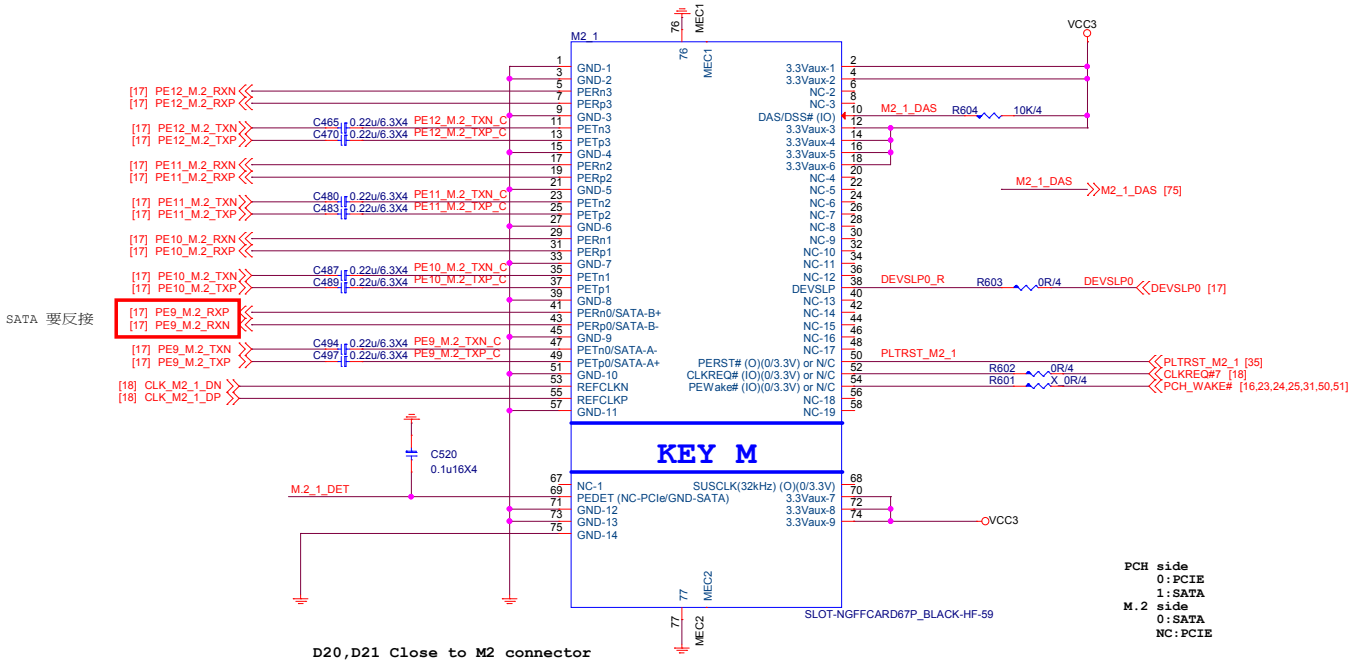
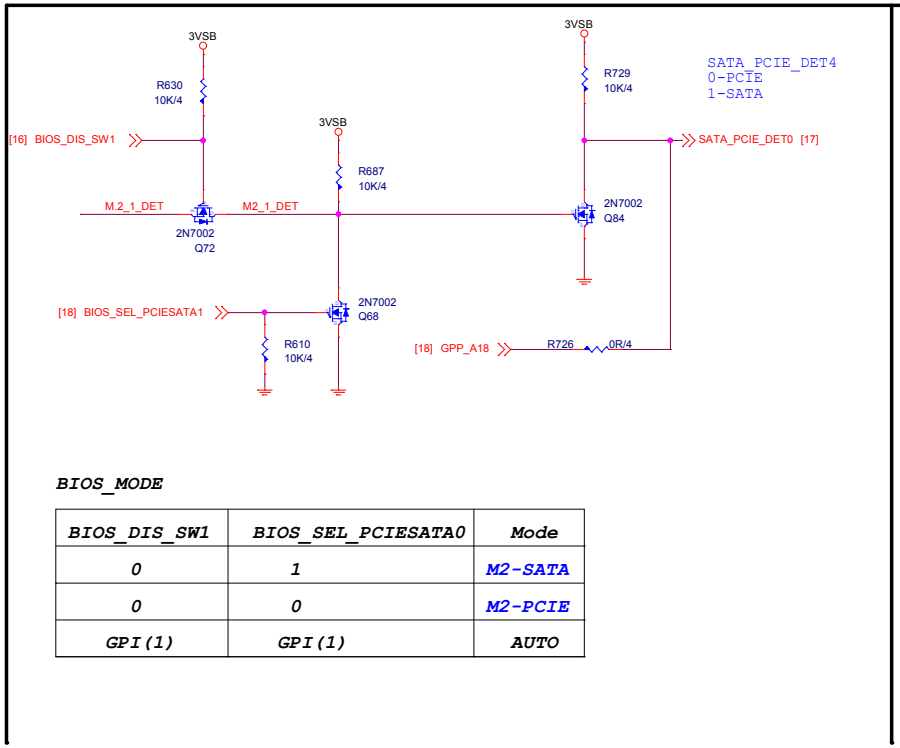
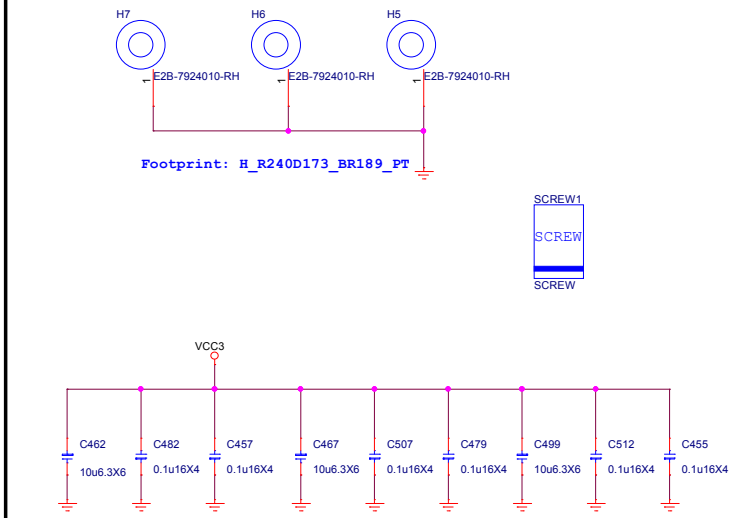




BIOS_MODE

BIOS_DIS_SW1	BIOS_SEL_PCIESATA0	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI(1)	GPI(1)	AUTO



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Size	Document Description	Rev
Custom	M2_1	1.0

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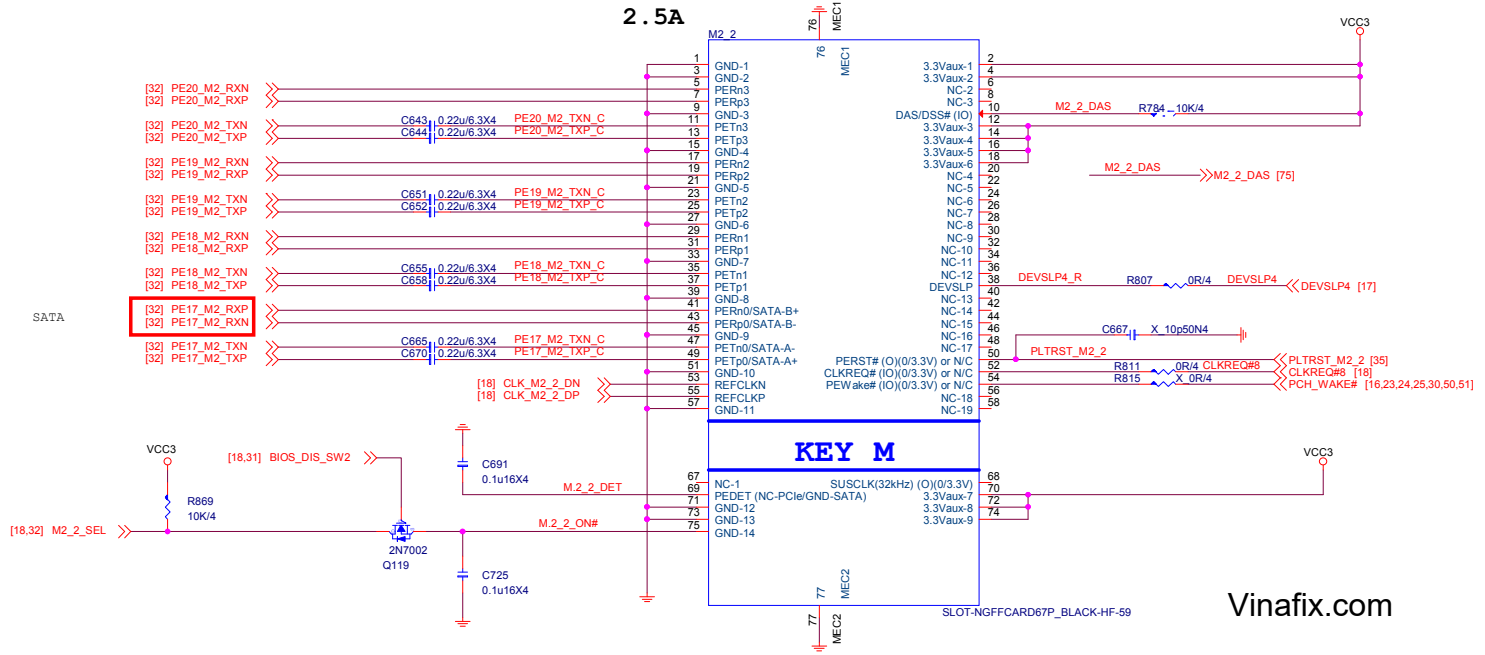
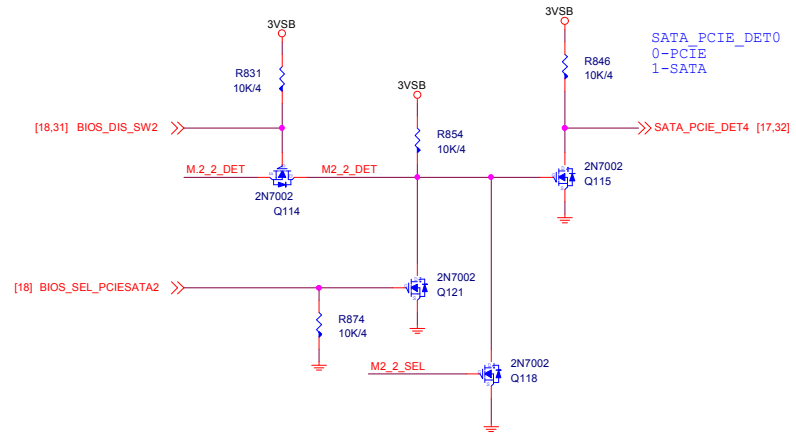
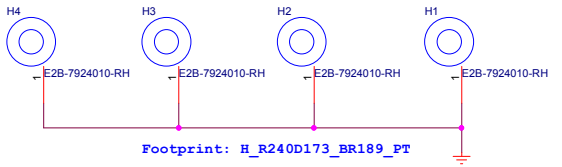
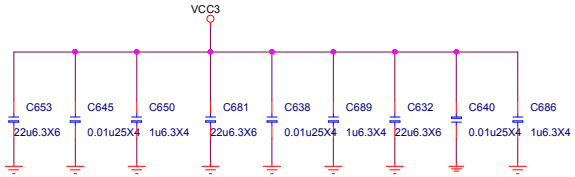




BIOS_MODE

M2_CPUSEL#	*BIOS_DIS_SW2*	*M2_2_SEL*	*BIOS_SEL_PCIESATA2*	*Mode*
GPI(1)	*GPI(1)*	*GPI(1)*	*GPI(0)*	*AUTO*
0	*0*	*1*	*1*	***M2-CPU***
1	*0*	*1*	*0*	***SATA***
1	*0*	*0*	*1*	***M2-SATA***
1	*0*	*0*	*0*	***M2-PCIE***





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Size	Document Description	Rev
Custom	M2_2	1.0

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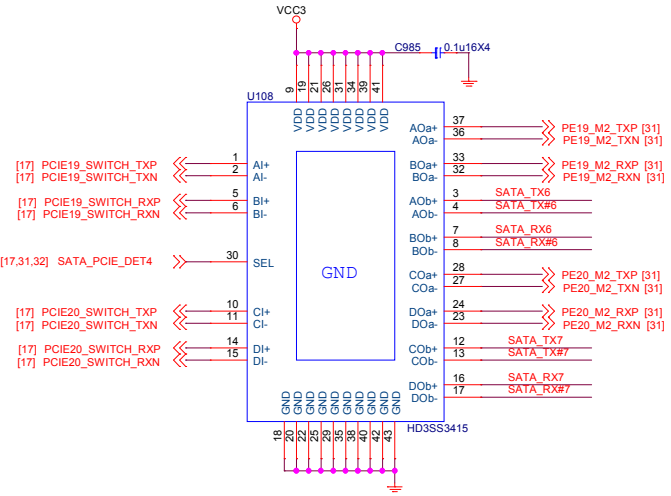
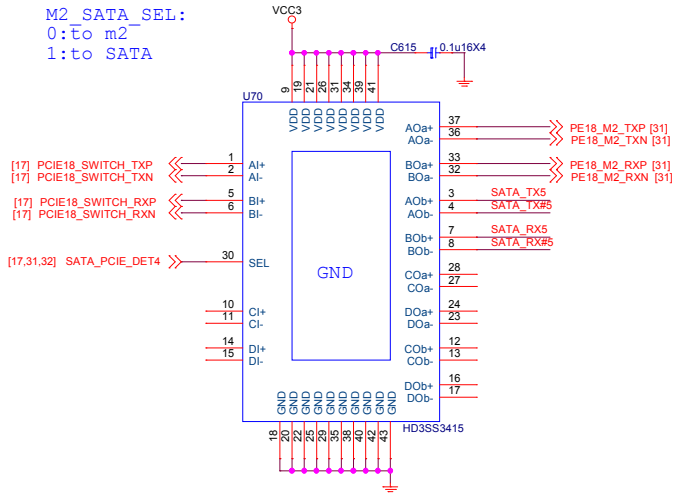
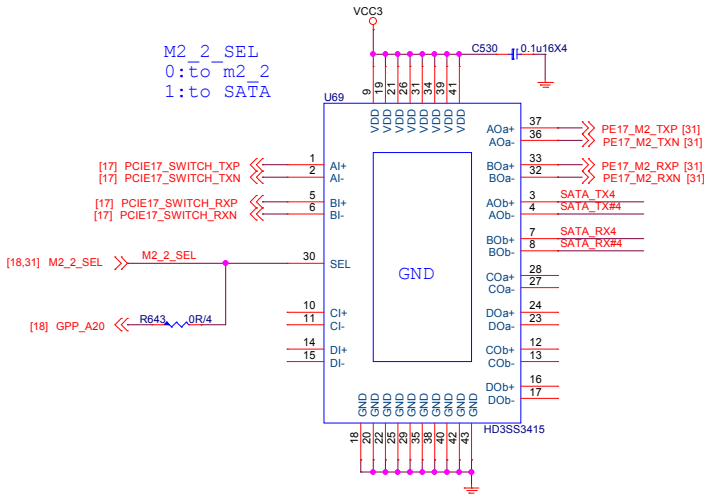
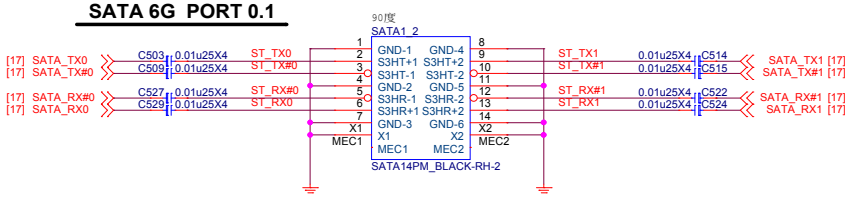


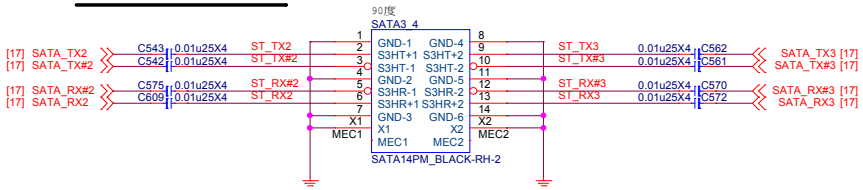




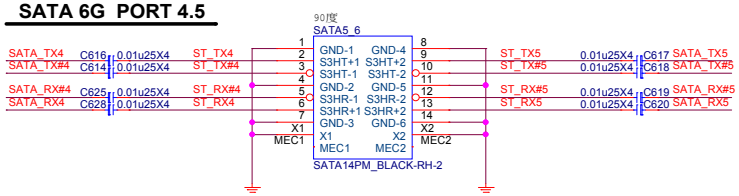
SATA 6G PORT 0.1



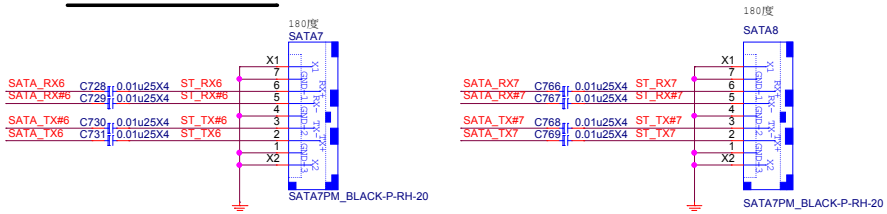
SATA 6G PORT 2.3



SATA 6G PORT 4.5



SATA 6G PORT 6.7



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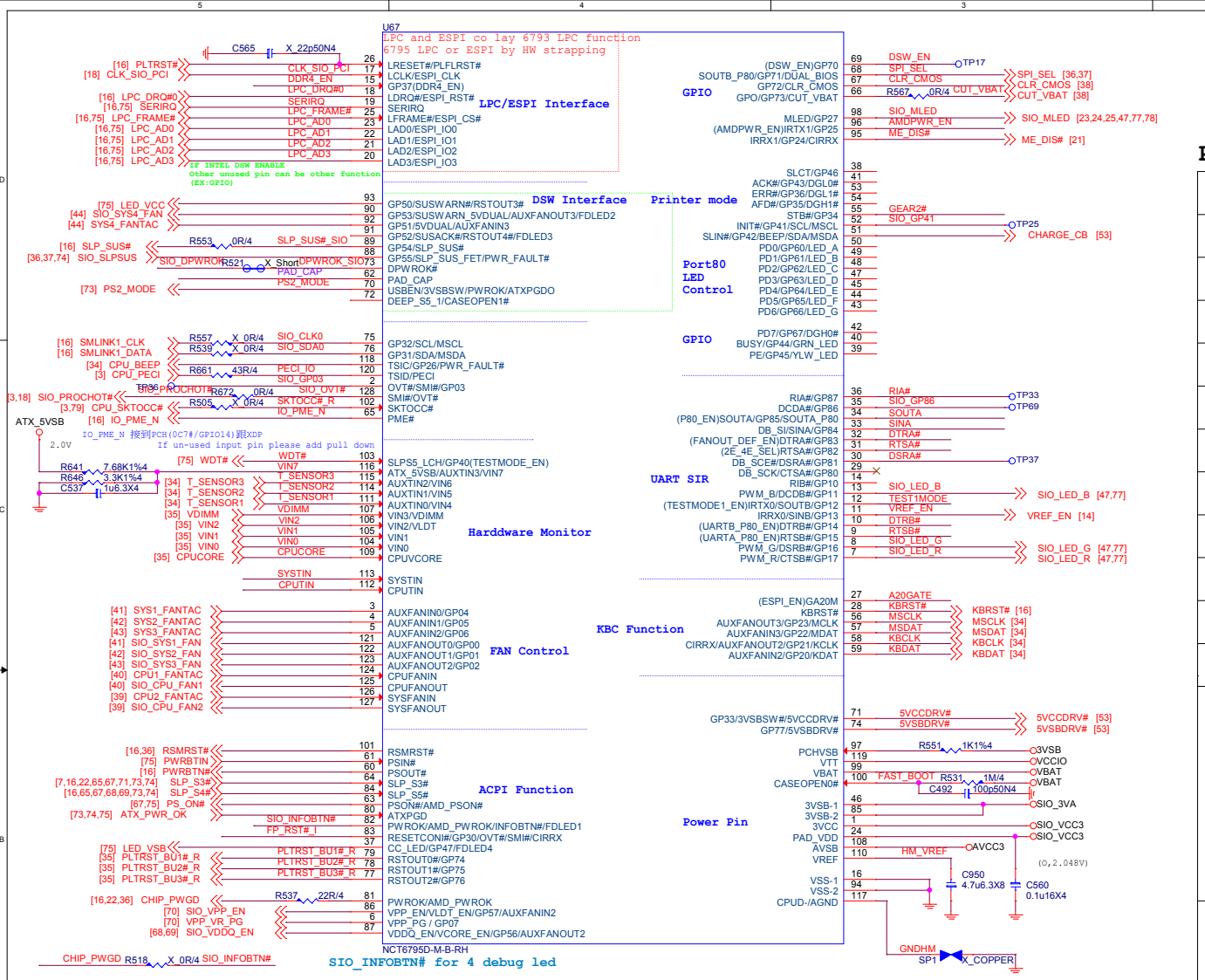
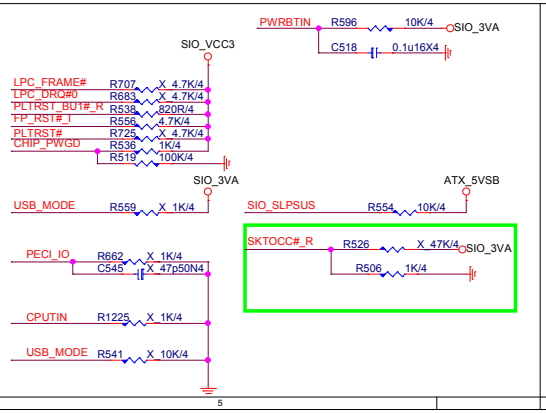
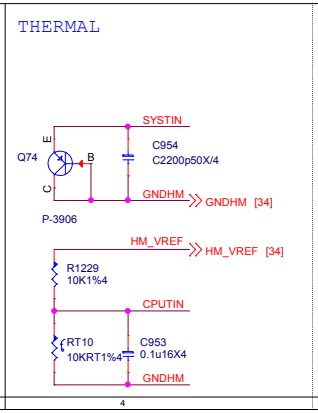
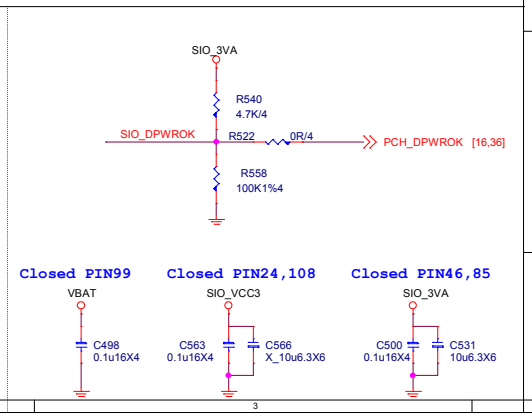
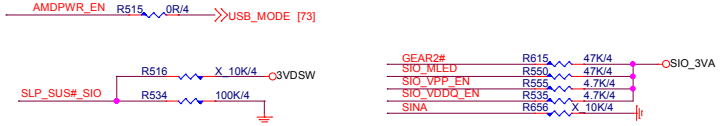






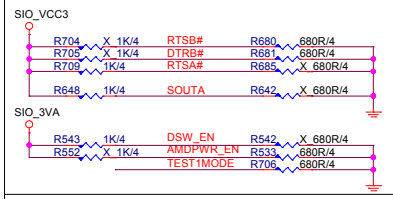


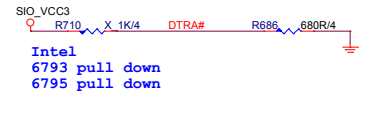


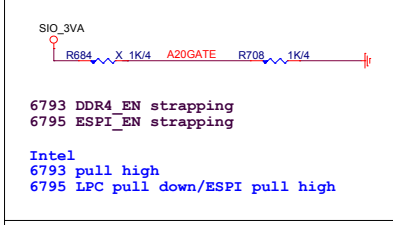
POWER ON STRAPPING PIN FOR NCT6793/6795

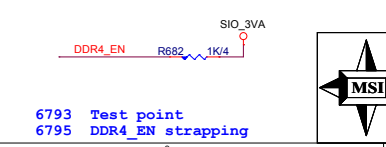
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TEST1MODE_EN	TEST1MODE	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	6793 test point 6795 DDR4_EN	6793 test point 6795 DDR4_EN	6793 NA 6795 Disable	6793 NA 6795 Enable	
27	6793 DDR4_EN 6795 ESPI_EN	A20GATE	6793 Disable 6795 Disable	6793 Enable 6795 Enable	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	6793 TESTMOD2_EN 6795 FANOUT_DEF_EN	DTRA#	6793 disable 6795 default 50%	6793 Enable 6795 default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	TESTMODE_EN	WDT#	DISABLE TESTMODE	ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

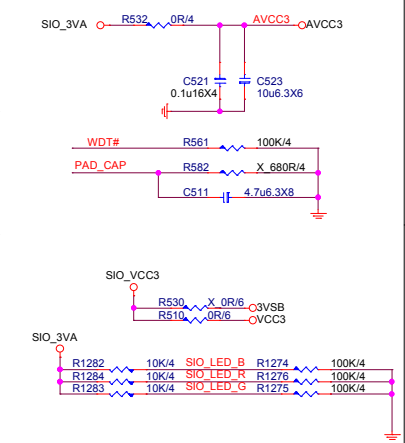








3V Analog Power



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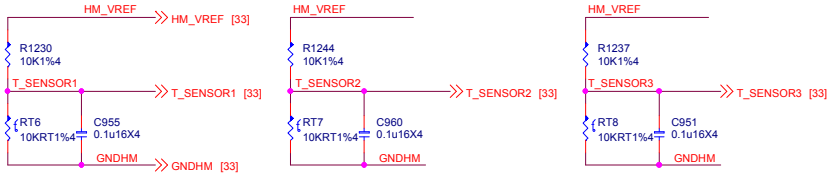
THERMAL



DEBUG LED

2017.04.10 PM Spec Remove

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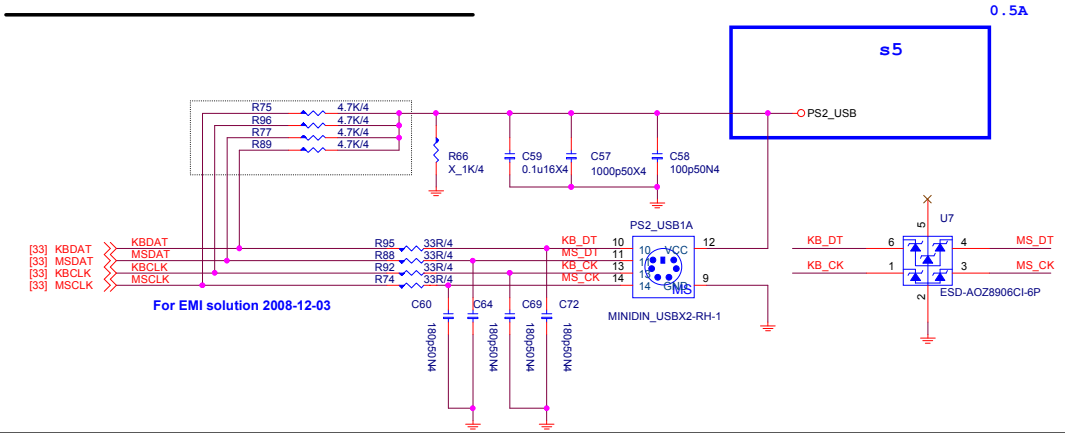
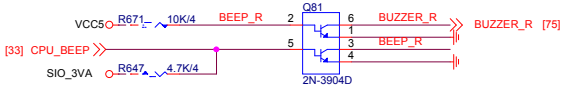
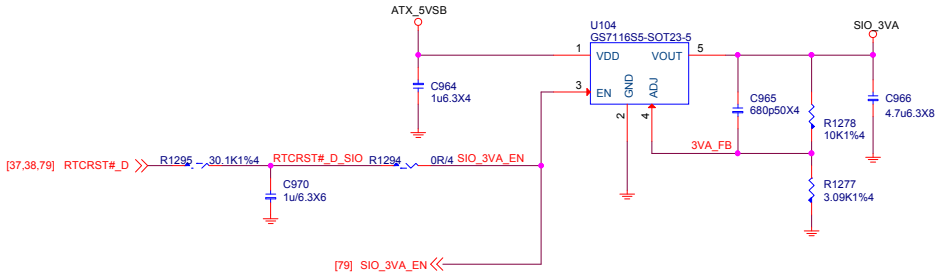
PS2 KEYBOARD & MOUSE CONNECTOR

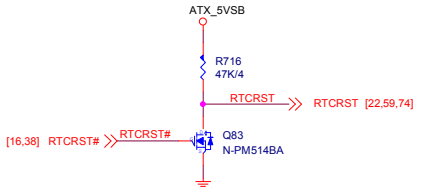


COM Port for BIOS Debug



SLP_SUS Co-lay circuit





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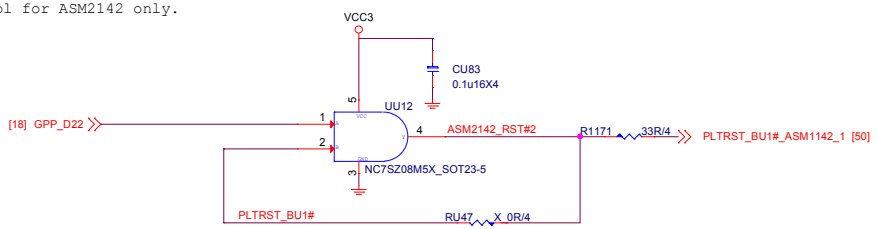
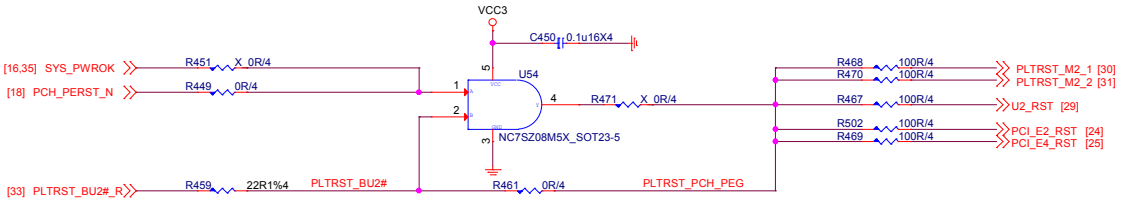
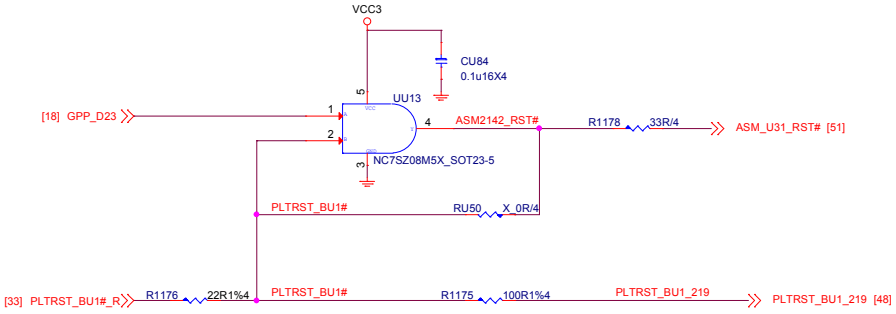
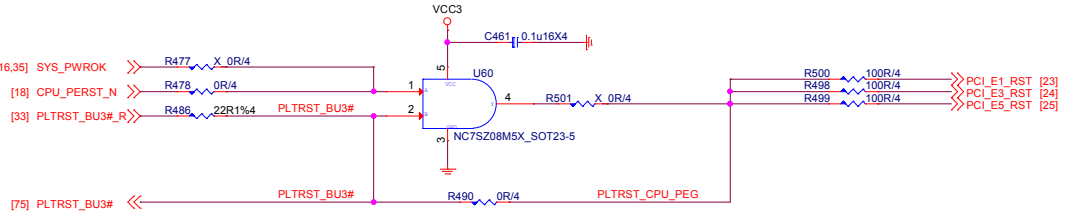
Reset control for ASM2142 only.



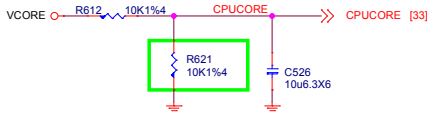


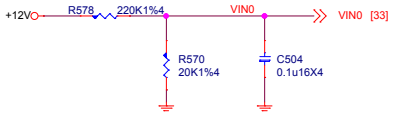


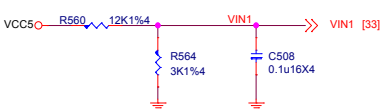


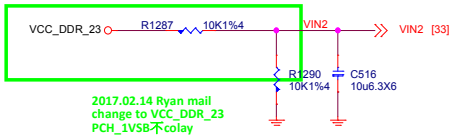
HW Monitor - Voltage

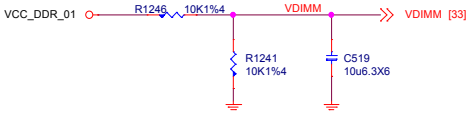
SIO HM Voltage voer 2V will not detect

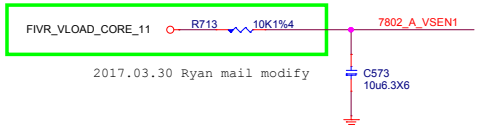


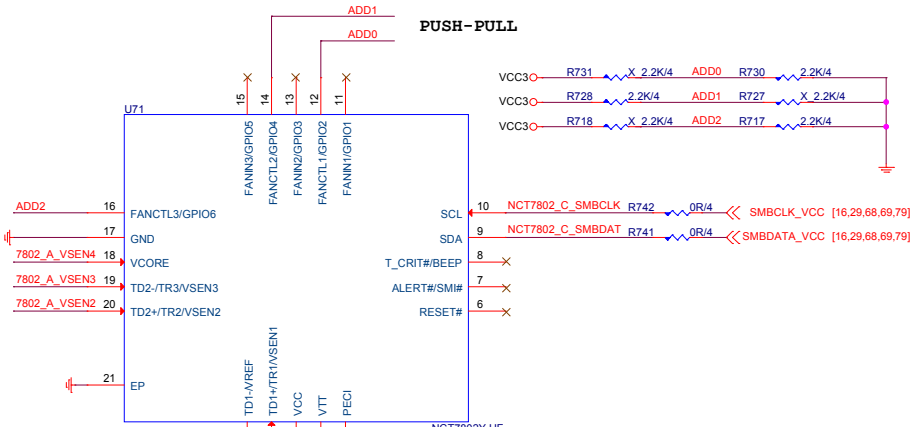




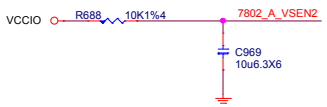


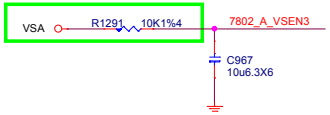


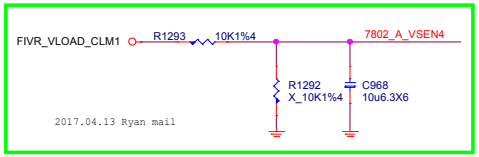




NCT7802Y to address 54h







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Part Number:N31-2061341-H06

[16] PCH_SPI_CS0# PCH_SPI_CS0#
[16,21] PCH_SPI_MOSI PCH_SPI_MOSI
[16,21] PCH_SPI_MISO PCH_SPI_MISO
[16] PCH_SPI_CLK PCH_SPI_CLK
[16,21] PCH_SPI_IO2 PCH_SPI_IO2
[16,21] PCH_SPI_IO3 PCH_SPI_IO3

SPI CS# < 25pF
D0G-0402510-SI0

close to JSPI1 for ESD use

SPI_VCC3 R845 0R/6 3VSB

SPI DEBUG PROT
Close to SPI ROM

SPI_VCC3 C697 0.1u16X4

SPI_VCC3 SPI_VCC3

JSPI1
PCH_SPI_MISO PCH_SPI_MOSI
PCH_SPI_CS# PCH_SPI_CLK
SPI_SW_SEL
PCH_SPI_IO2 PCH_SPI_IO3
H2X6[10]M-2PITCH_BLACK-RH-3

PCH_SPI_CS0# R838 0R/4
D21 ESD-AOZ8131DI
C698 0.1u16X4

For TL624-1.1 : Stuff D7
Old : Only RSVD (Because 12V level)

P.S Close to JSPI1

HW MODE

A BIOS
MEC1
BIOS_SW1 SW-DIP_BLACK-RH
SPI_SEL_R SPI2_SW
C732 X_0.1u16X4
R887 1K/4 SPI_SEL
R886 4.7K/4
SPI_VCC3
Skylake use SPI_VCC3

B BIOS
MEC2
SPI_VCC3 Skylake use SPI_VCC3

C726 0.1u16X4

R873 0R/4 For MCJ singal BIOS

SIO NCT6793 GP71

U80
PCH_SPI_CS# SPI_CS1#
SPI_SEL SPI_CS2#
NC7SB3157P6X_SOT323-6

[33,37] SPI_SEL
R877 100K1%4

GPI default low
Active push pull high switch to SPI2
For auto testing in factory.

IN=0 , D connected to S2 (SPI1- A Bios)
IN=1 , D connected to S1 (SPI2- B Bios)

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ATX_5VSB R856 10K/4 SPI_SW_SEL SPI_SW_SEL [79]

[16,33] PCH_DPWROK D23 S-LRB520S-40T1G-HF
[16,33] RSMRST# D24 S-LRB520S-40T1G-HF
[16,22,33] CHIP_PWGD D25 X_S-LRB520S-40T1G-HF
[33,37,74] SIO_SLPSUS D22 S-LRB520S-40T1G-HF

VCC5 R839 X_4.7K/4
A_BIOS1 X_LED04-R-20mA
VCC5 R875 X_1K/4
B_BIOS1 X_LED04-W-20mA

ATX_5VSB R858 X_47K/4
SPI_SEL Q120 G2 D2 D1 S2
SPI1_SW G1 S1
X_NN-2N7002D
SPI_SEL Q122 X_2N7002

SPI_VCC3
R836 X_1K/4 PCH_SPI_MOSI
R837 X_1K/4 PCH_SPI_MISO

SPI FLASH ROM

Place close to SB.

MXIC:M31-2512832-M24
WinB:M31-2512853-W03

32M ROM For X299

A BIOS
SPI_VCC3 R813 2.2K/4
A_SPI1
SPI_CS1# PCH_SPI_MISO PCH_SPI_IO2
R819 33R/4 R823 33R/4
SPI1_MISO SPI1_IO2
CS SO(SIO1) WP(SIO2) GND
VCC RESET(SIO3) SCLK SI(SIO0) EPAD
W25Q128JVSIQ-HF
C662 0.1u16X4
C668 10u6.3X6
SPI1_IO3 SPI1_CLK SPI1_MOSI
R814 R824 R828 33R/4
PCH_SPI_IO3 PCH_SPI_CLK PCH_SPI_MOSI

B BIOS
SPI_VCC3 R808 2.2K/4
SPI_CS2#
B_SPI1
PCH_SPI_MISO PCH_SPI_IO2
R820 R827 33R/4
SPI2_MISO SPI2_IO2
W25Q128JVSIQ-HF
C660 0.1u16X4
C663 10u6.3X6
SPI2_IO3 SPI2_CLK SPI2_MOSI
R812 R822 R829 33R/4
PCH_SPI_IO3 PCH_SPI_CLK PCH_SPI_MOSI

*SPI_CLK & SPI_MOSI must be length matched to within 500mils. < 6 inch
*SPI_CLK & SPI_CS0# must be length matched to within 500mils.

ATX_5VSB
U78 X_GS7116S5-SOT23-5
VDD VOUT EN GND ADJ
C724 X_1u6.3X4
R855 X_47K/4
C722 X_680p50X4
R870 X_10K1%4
SPI_FB
SIO_SLPSUS Q116 X_2N7002
R857 X_3.09K1%4
SPI_VCC3 C700 X_22u6.3X8

MICRO-STAR INT'L CO.,LTD
MA-7A94..
Size Custom
Document Description Dual BIOS
Rev 1.0
Date: Saturday, April 22, 2017
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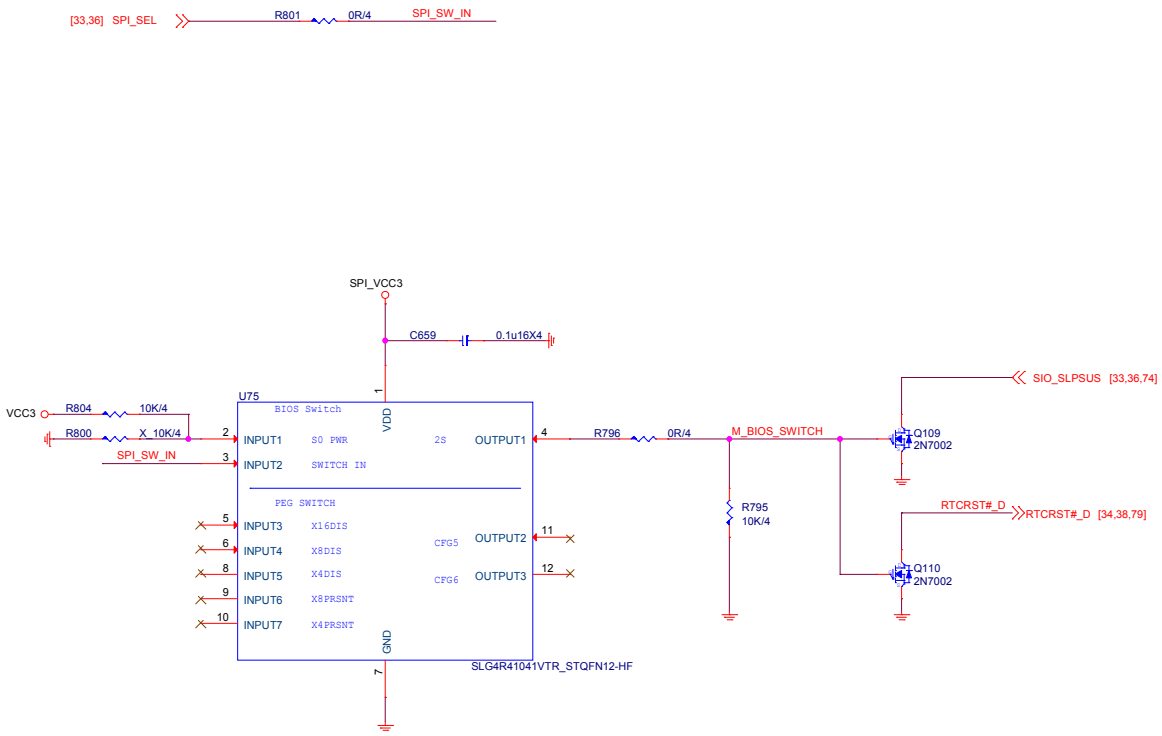
Skylake/Kabylake Path Circuit For Dual Bios



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MA-7A94..		
Size: Custom	Document Description: Dual bios control-Silego	Rev: 1.0
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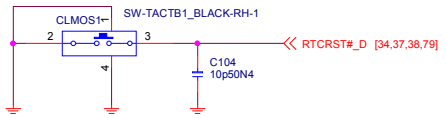
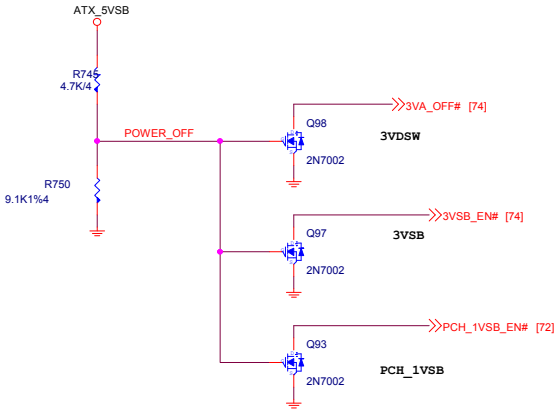
RTCRST# R462 X_0R/4 RTCRST#_D

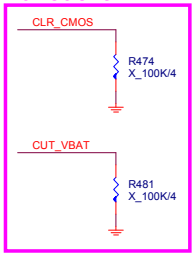
Clear CMOS button

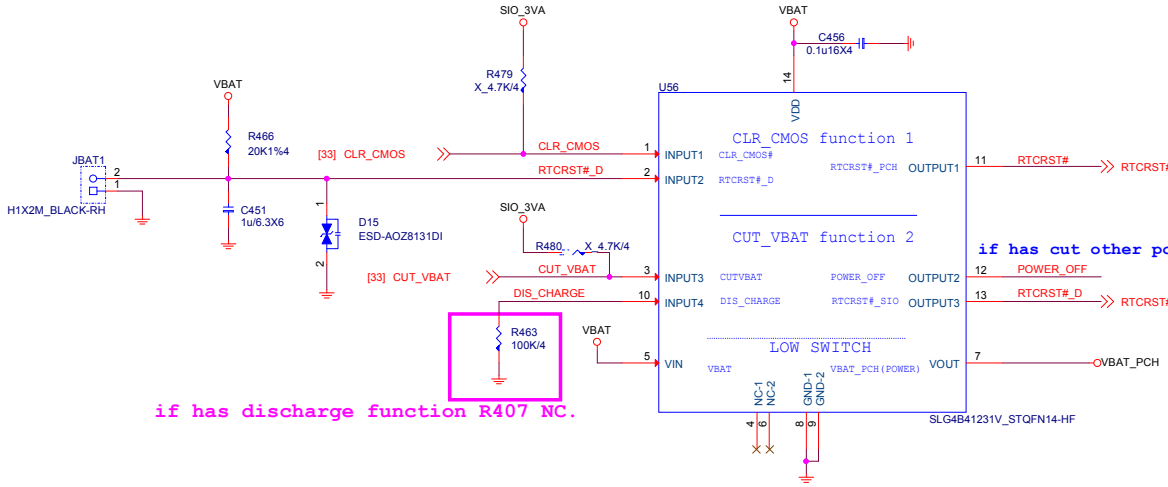


CUT VBAT



20160629

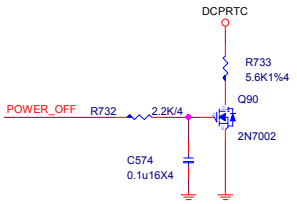




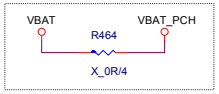
if has discharge function R407 NC.

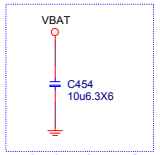
if has cut other power,please use output 2.

Add DCRTC dischage circuit

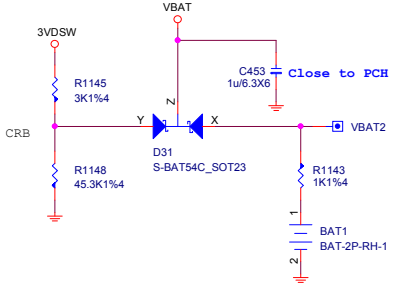


VBAT





have timming issue keep
0805 size don't removed



Vinafix.com

MSI	MICRO-STAR INT'L CO.,LTD	
	MA-7A94..	
Size: Custom	Document Description: CLR COMS/CUT VBAT	Rev: 1.0
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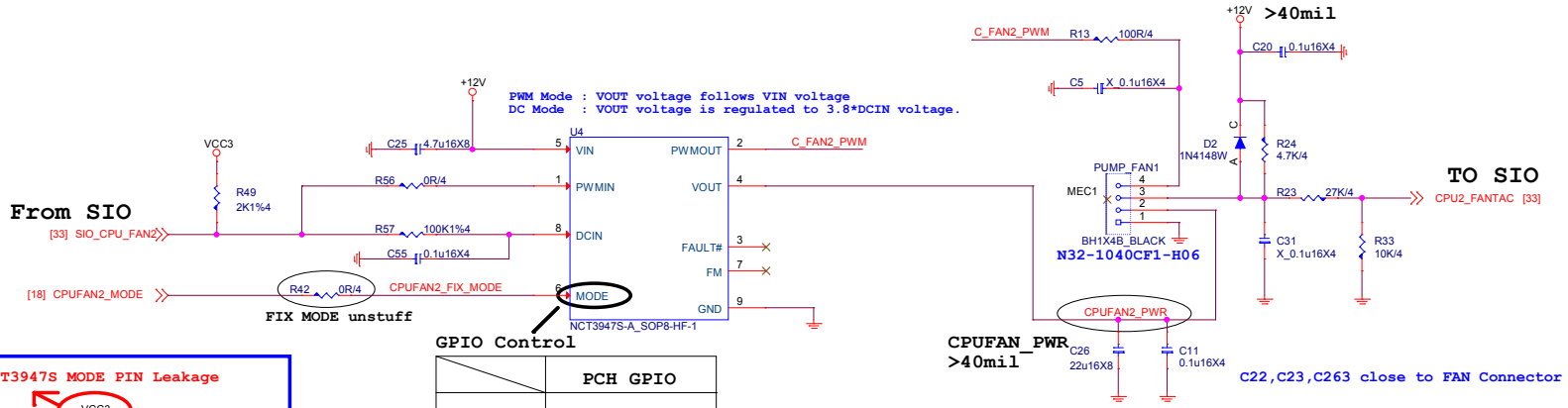
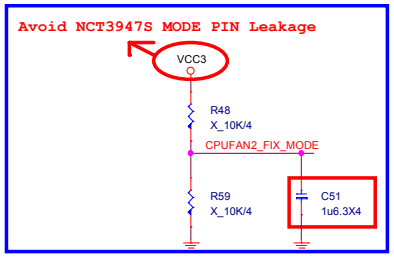
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

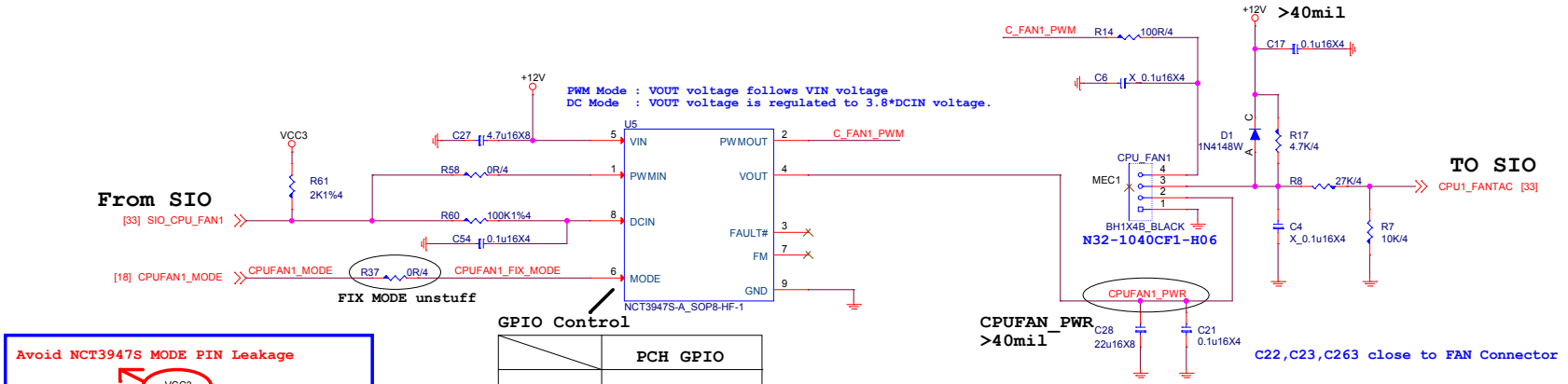
MICRO-STAR INT'L CO.,LTD

MA-7A94..

Size: Custom | Document Description: CPU FAN2 | Rev: 1.0

Date: Saturday, April 22, 2017 | Sheet 39 of 85

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

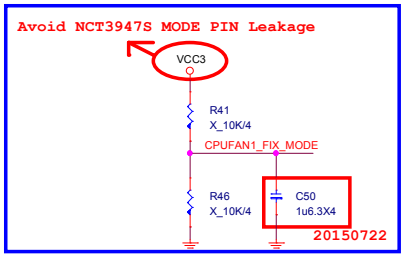


GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

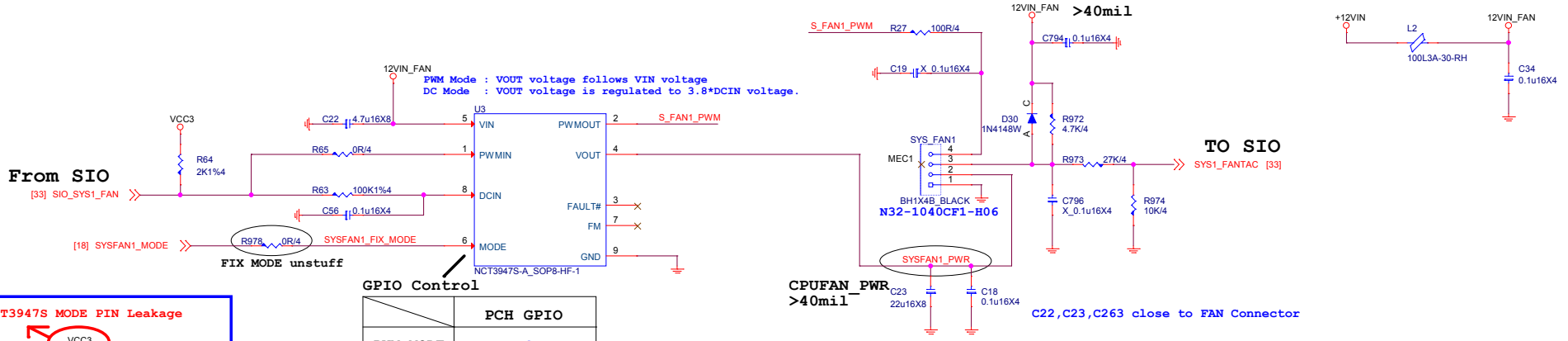
Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

MICRO-STAR INT'L CO.,LTD		
MA-7A94..		
Size: Custom	Document Description: CPU FAN1	Rev: 1.0
Date: Saturday, April 22, 2017	Sheet 40 of 85	

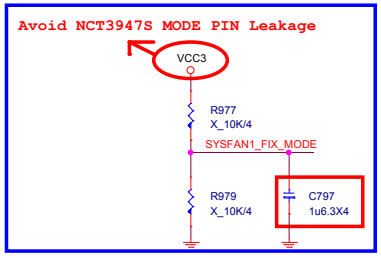
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

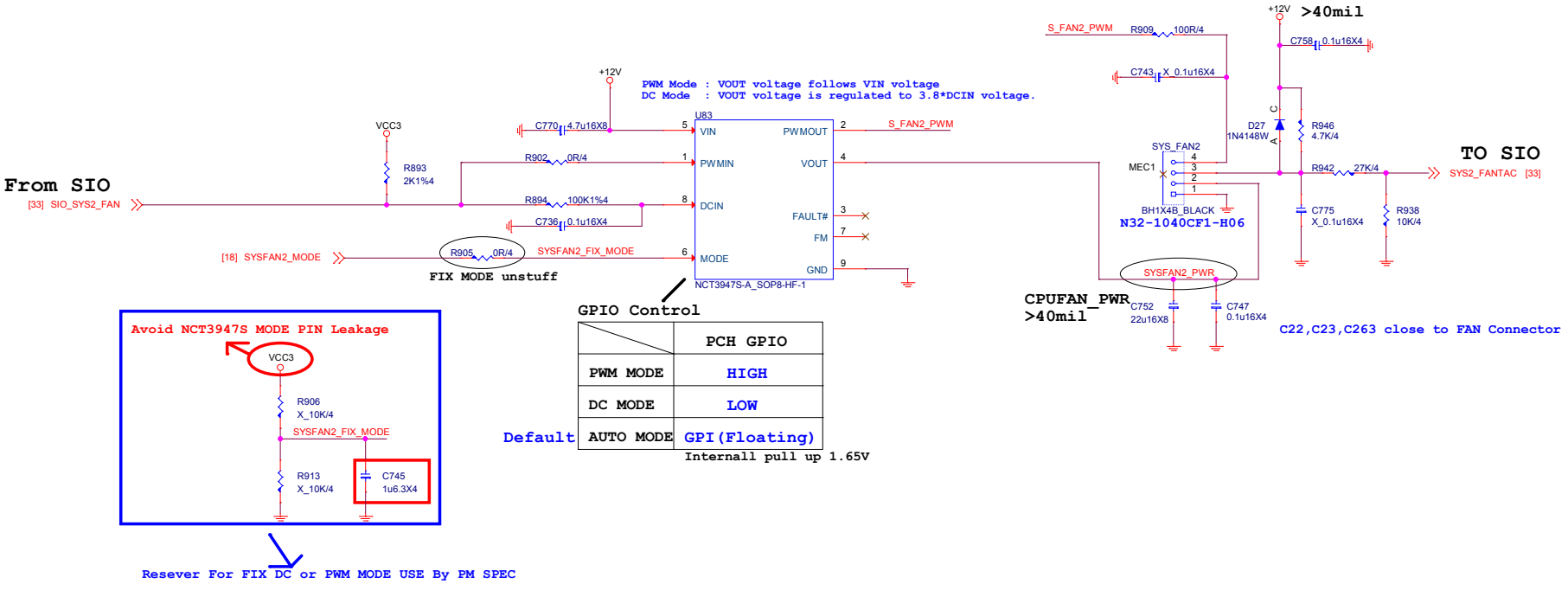
MICRO-STAR INT'L CO.,LTD

MA-7A94..

Size	Document Description	Rev
Custom	SYSTEM FAN1	1.0

Date: Saturday, April 22, 2017 Sheet 41 of 85

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

Internall pull up 1.65V

Resever For FIX DC or PWM MODE USE By PM SPEC

MICRO-STAR INT'L CO.,LTD

MA-7A94..

Size	Document Description	Rev
Custom	SYSTEM FAN2	1.0

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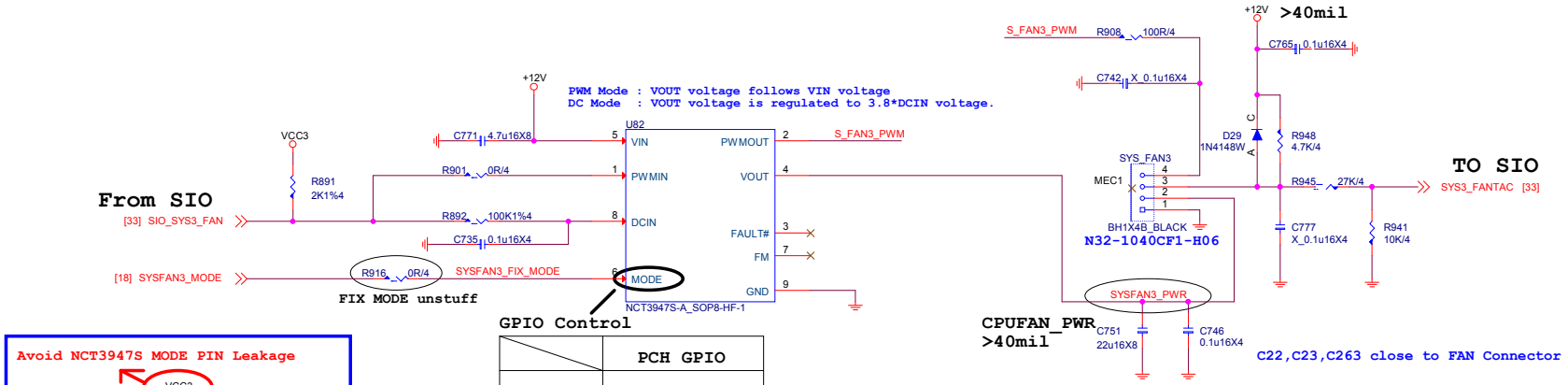
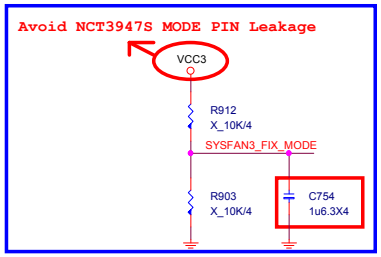
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

Default

Internall pull up 1.65V



Resever For FIX DC or PWM MODE USE By PM SPEC

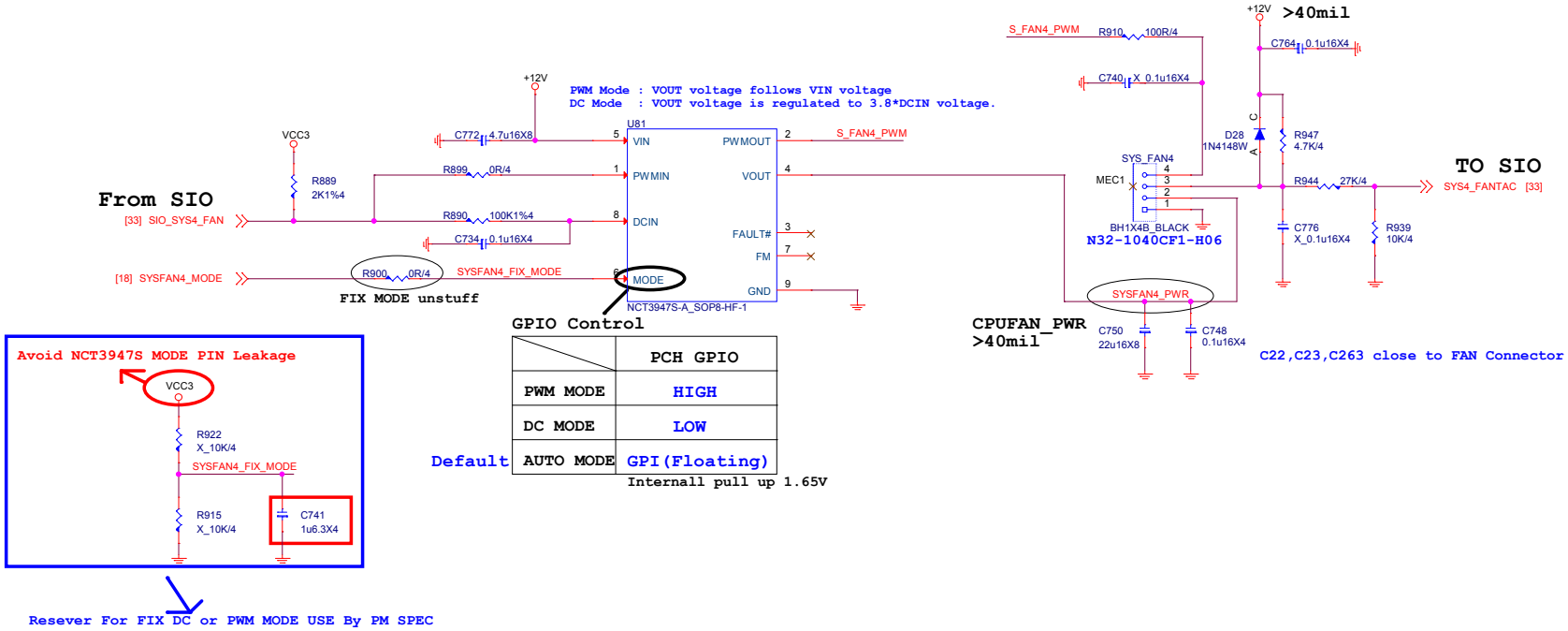
MICRO-STAR INT'L CO.,LTD

MA-7A94..

Size: Custom | Document Description: SYSTEM FAN3 | Rev: 1.0

Date: Saturday, April 22, 2017 | Sheet 43 of 85

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD

MA-7A94..

Size: Custom | Document Description: SYSTEM FAN4 | Rev: 1.0

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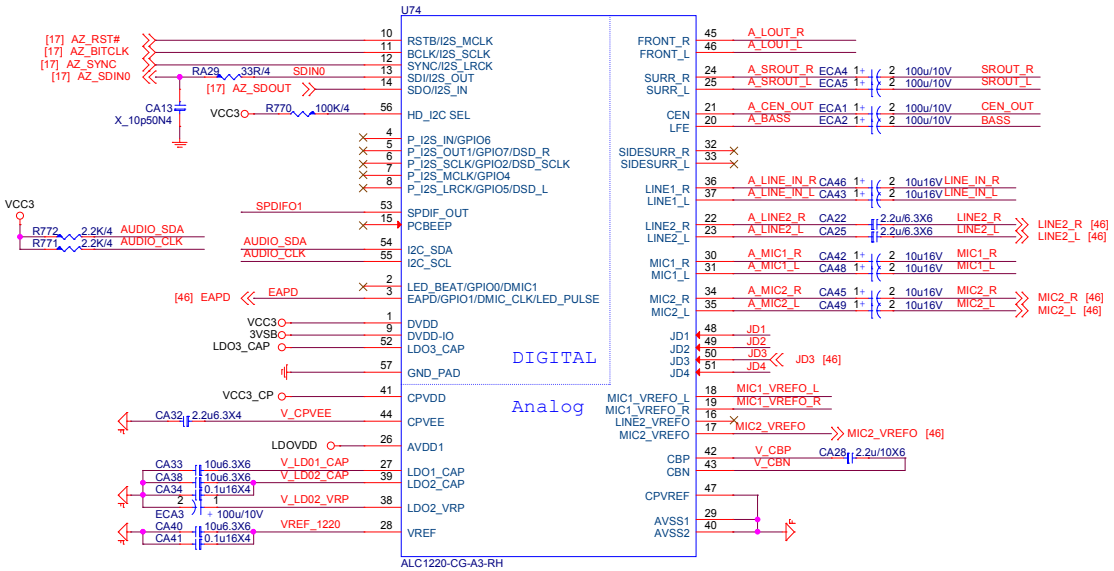
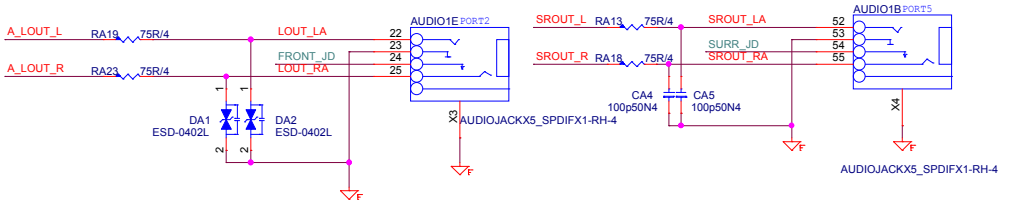
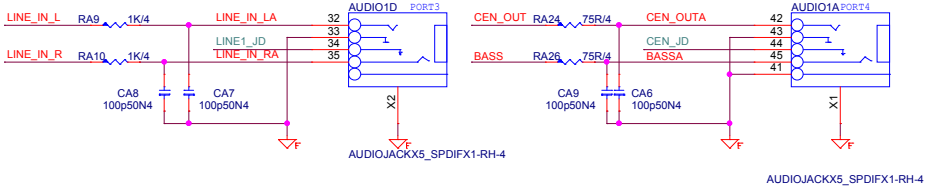
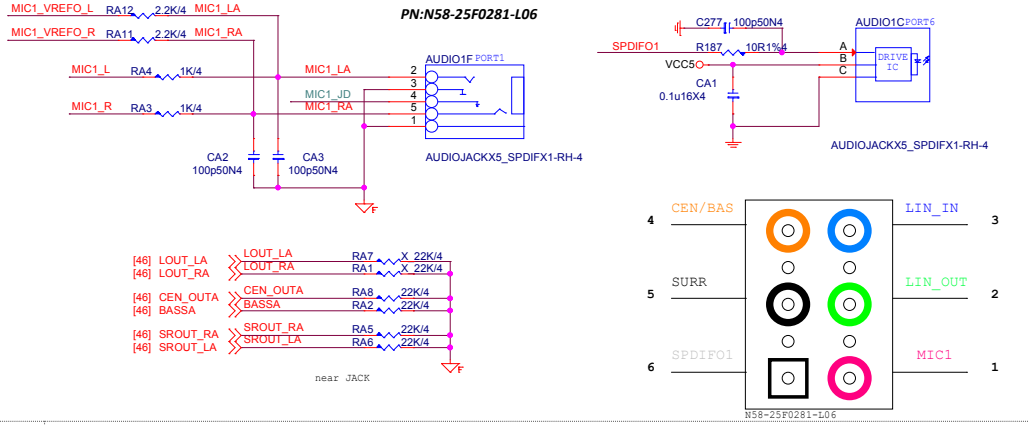
ALC1220

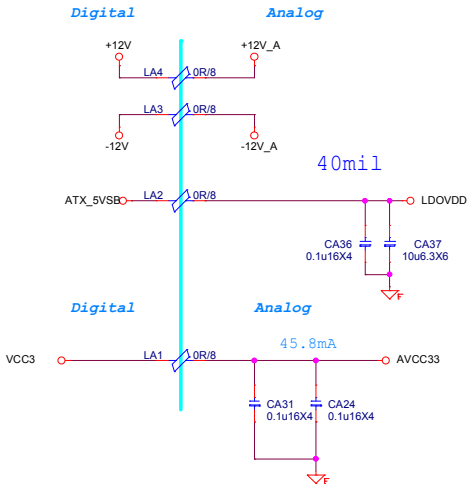




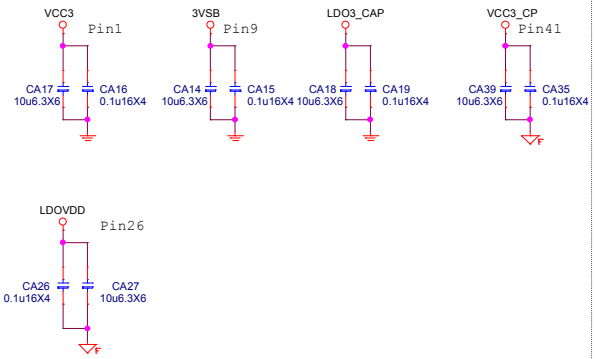


teknisi indonesia

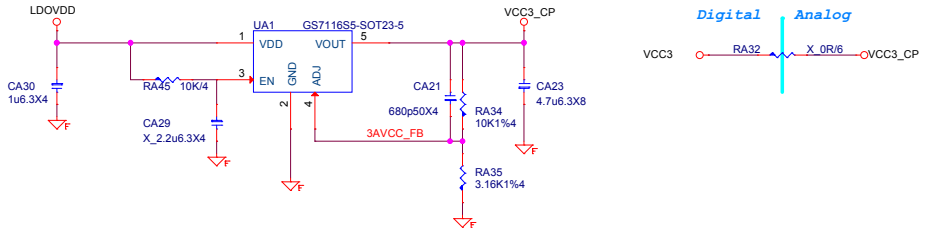


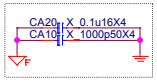


Closed Codec



CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V





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MA-7A94..		
Size: Custom	Document Description: AUDIO-ACL1220-1	Rev: 1.0
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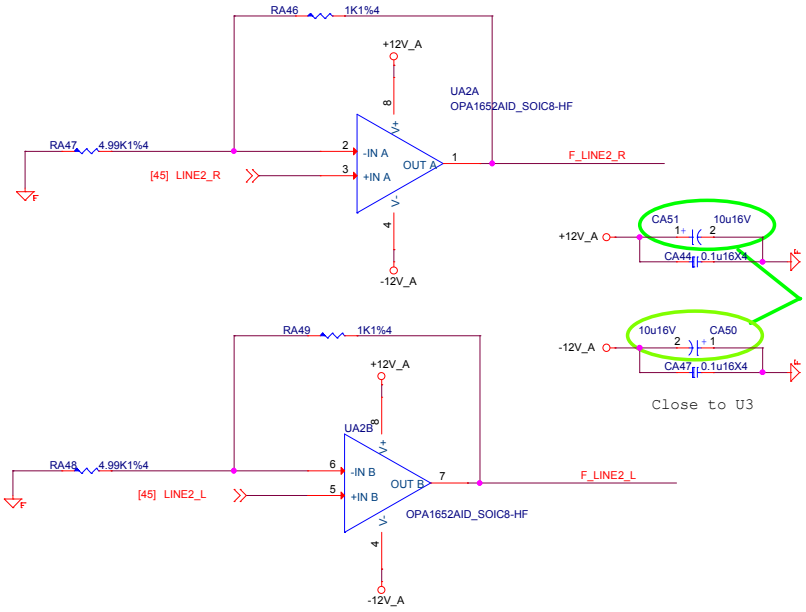
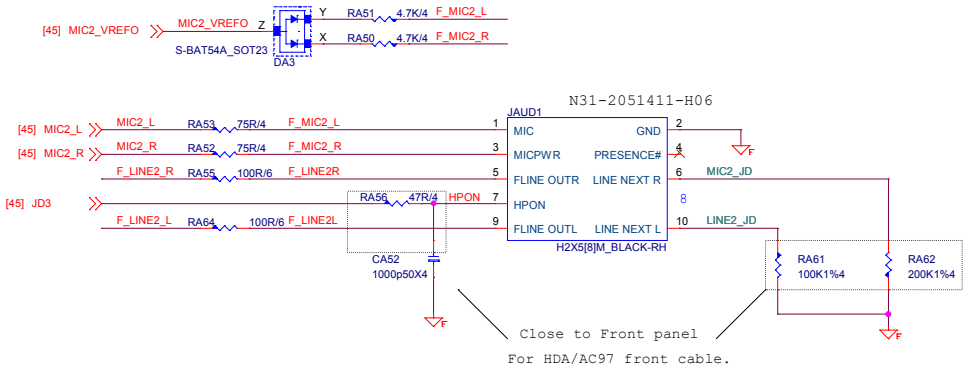
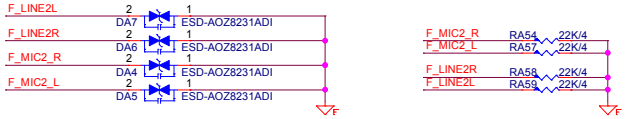




Close to Jack

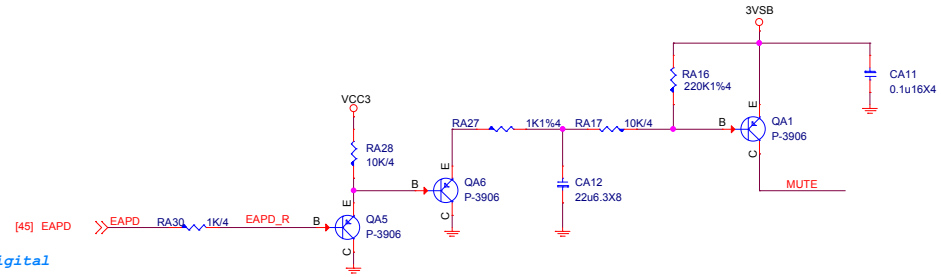
ESD protect

D0G-2950500-SI0
D0G-3010510-I05



Rear Line OUT De-POP circuit

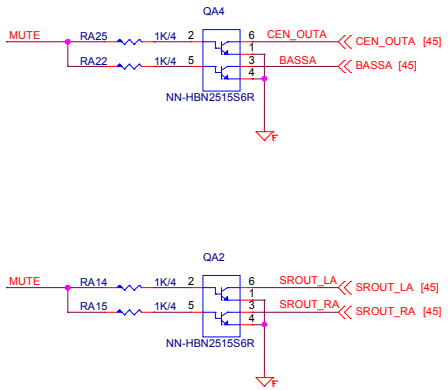
(De-pop circuit for Rear Line out & Front Headphone out)



Digital

Analog

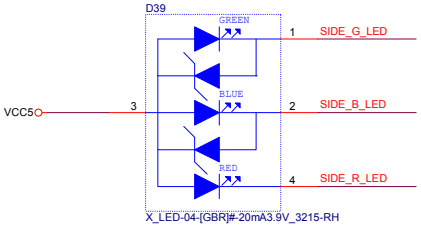
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA6,CA7, CA12, CA13, CA23, CA24 to TVS)

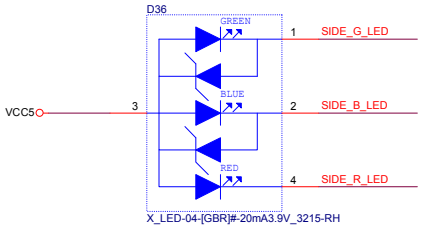


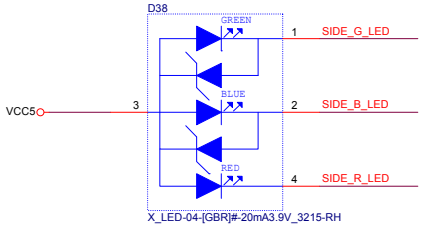
MICRO-STAR INT'L CO.,LTD		
MA-7A94..		
Size: Custom	Document Description: AUDIO-ACL1220-2	Rev: 1.0
Date: Saturday, April 22, 2017	Sheet 46 of 85	

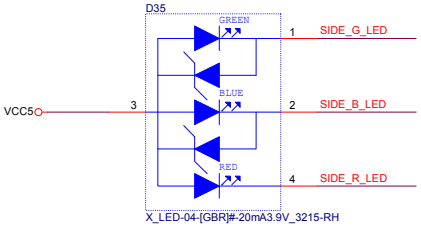
BOARD SIDE LED

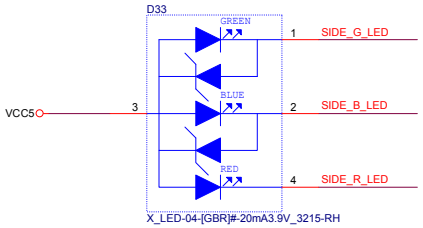
Audio moat is transparent and width 40mil

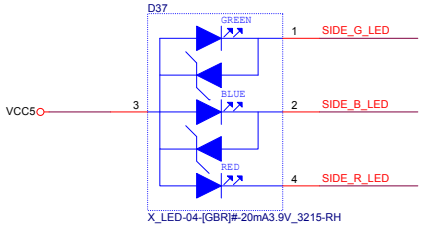


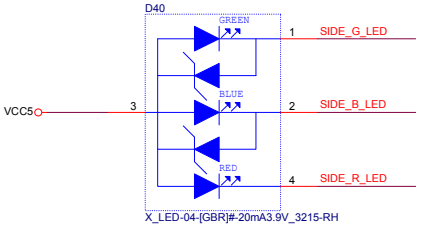


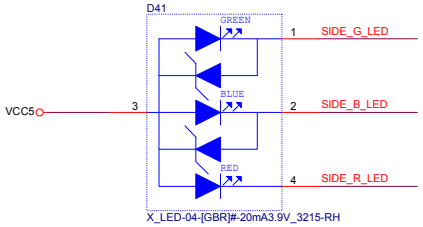


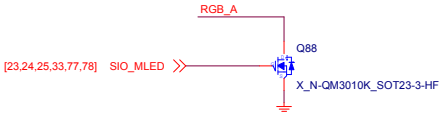


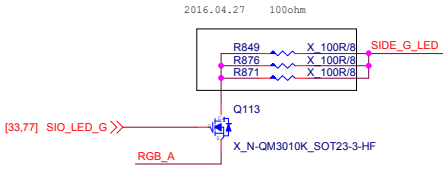




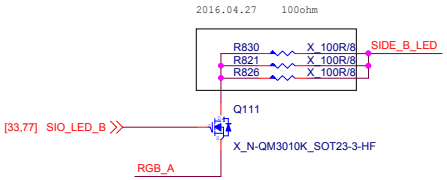




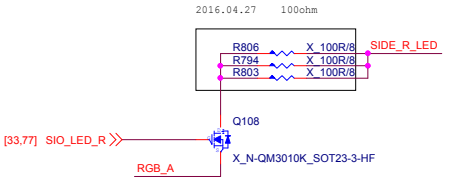




Vf=2.7 V~3.9V
5V-2.7V/100=0.023A
0.023A*0.023*100=0.0529W



Vf=2.7 V~3.9V
5V-2.7V/100=0.023A
0.023A*0.023*100=0.0529W



Vf=2.7 V~3.9V
5V-2.7V/100=0.023A
0.023A*0.023*100=0.0529W

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MA-7A94..

Size	Document Description	Rev
Custom	AUDIO-LED	1.0

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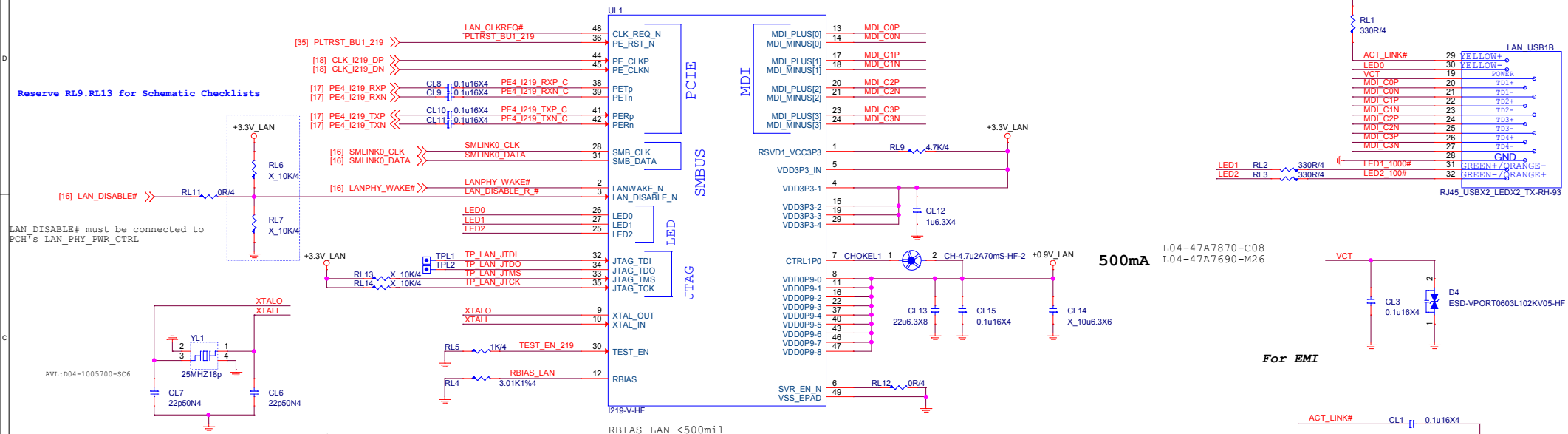
Intel I219V / I218V PHY



Reserve RL9.RL13 for Schematic Checklists

[16] LAN_DISABLE#

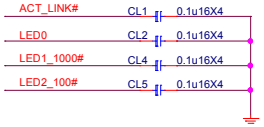
LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

RBIAS_LAN <500mil

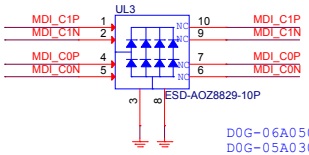
500mA

L04-47A7870-C08
L04-47A7690-M26

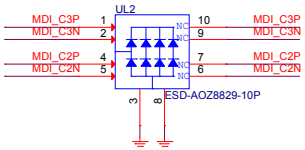
For EMI



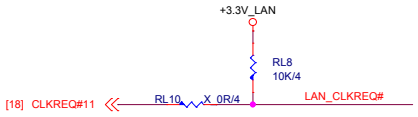
UL2&UL3 close to connector



D0G-06A050C-A68
D0G-05A0300-I14

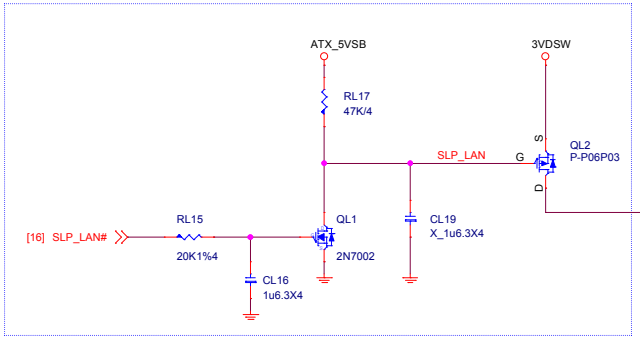


PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port.
If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN



The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



+3.3V_LAN

I218:132mA
I219:542mW

Note:These caps closed to PHY

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Size: Custom	Document Description: Intel Lan- i219	Rev: 1.0
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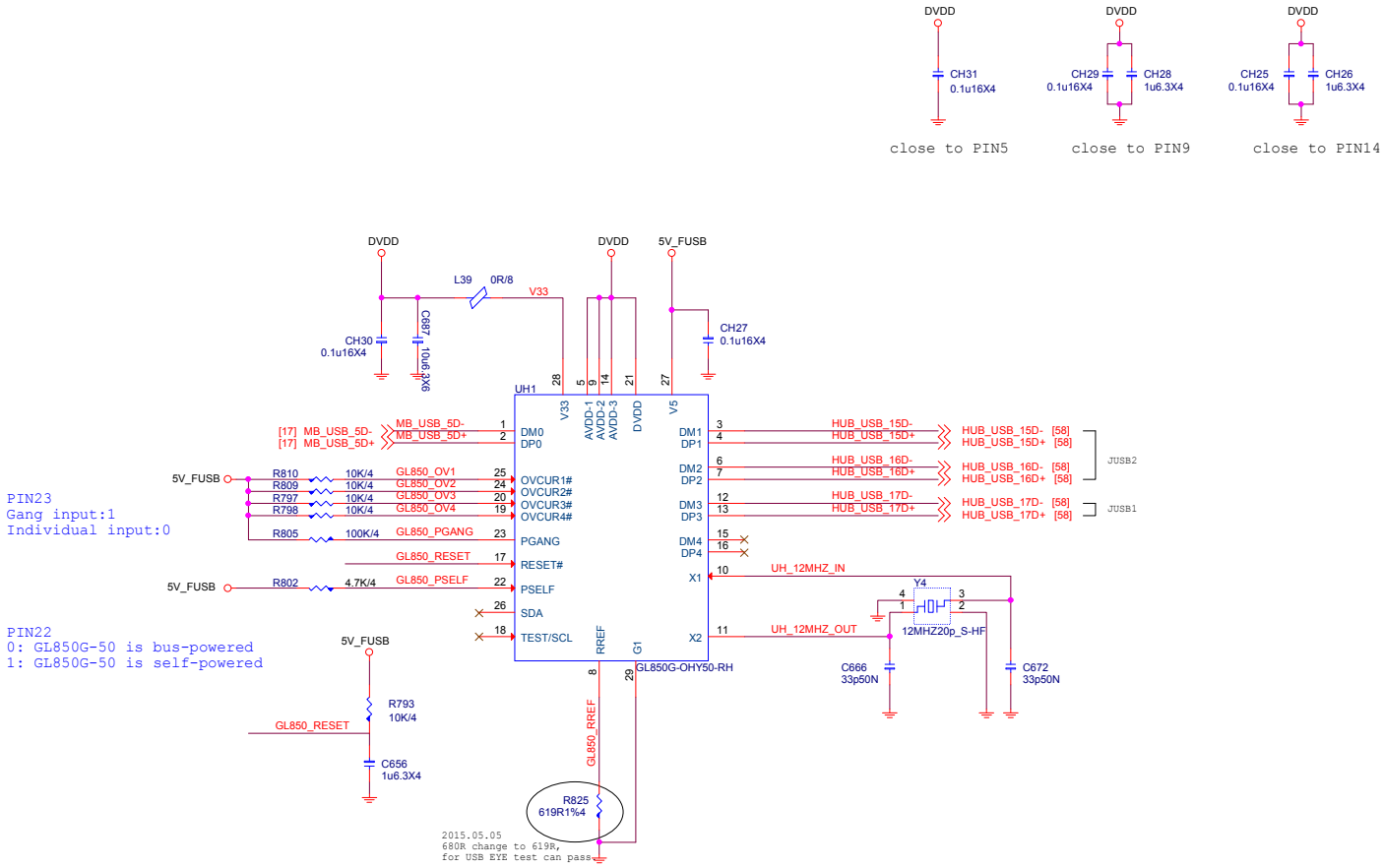

Follow 7A49

Vinafix.com

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	MA-7A94..	
Size: Custom	Document Description: USB HUB GL850G-50	Rev: 1.0
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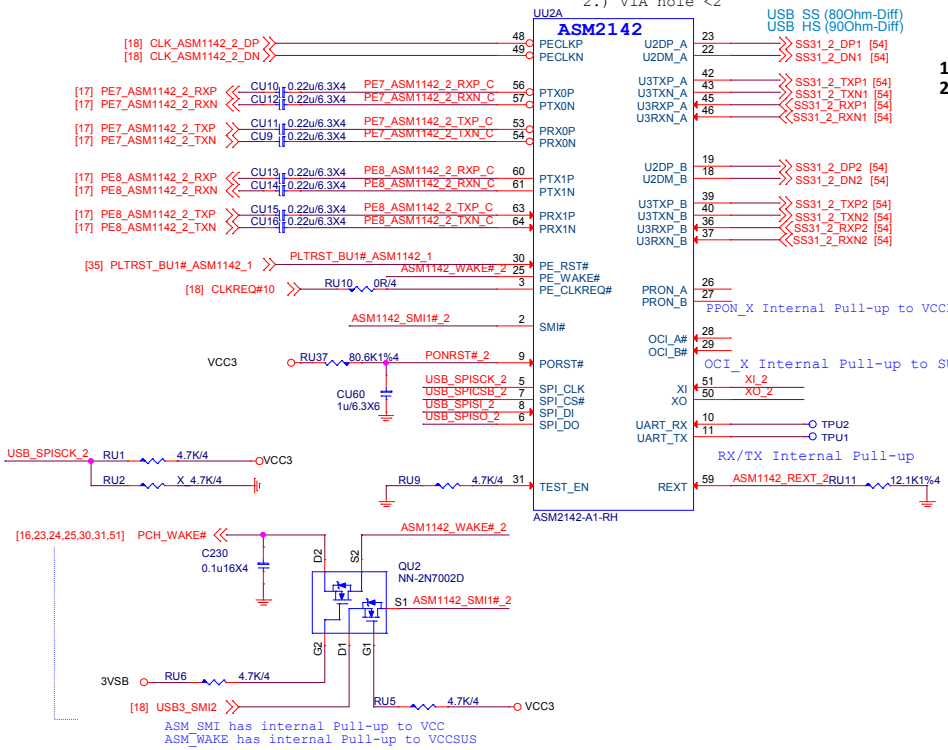
Layout Guide:

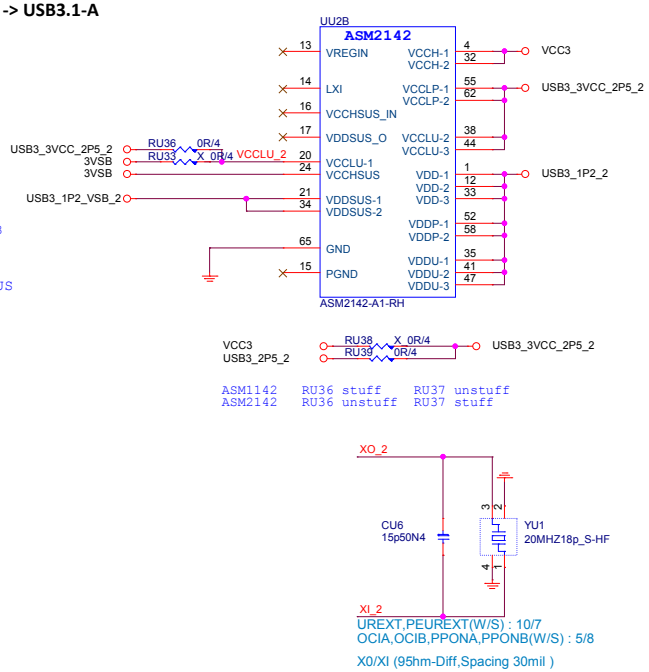
1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

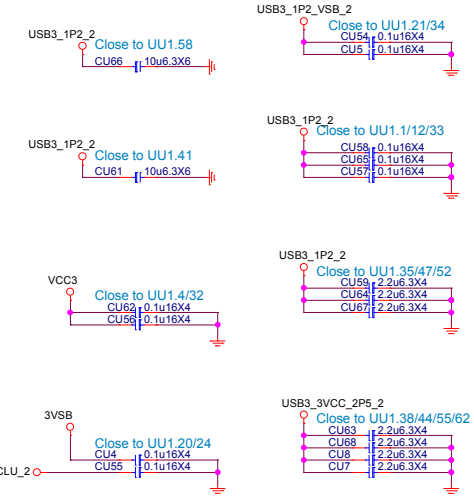


1 -> USB3.1-C
2 -> USB3.1-A

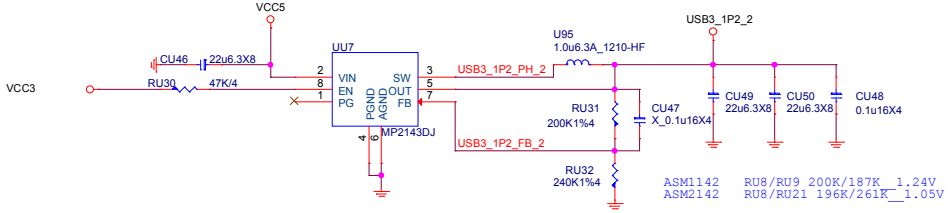
Power Consumption

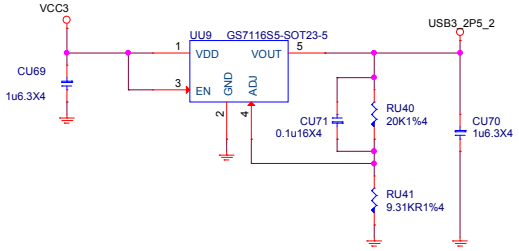
	3.3V	1.2V(1.05V)	3.3VSUS	1.05VSUS(1.2VSUS)	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP



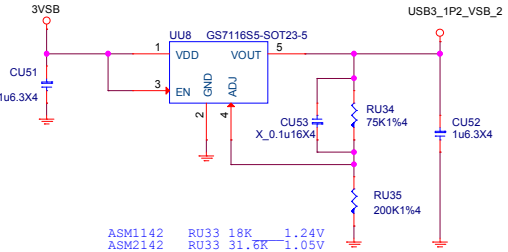


ASM1142 1.2 VCC Power

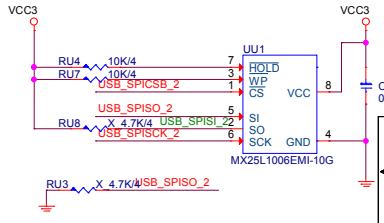




ASM1142 1.2 VSB Power



EEPROM



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Custom	USB3.1-ASM2142AE-2	1.0

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Use 0.22uF cap for GEN3 , Gen2 use 0.1uf by Upstream SPEC

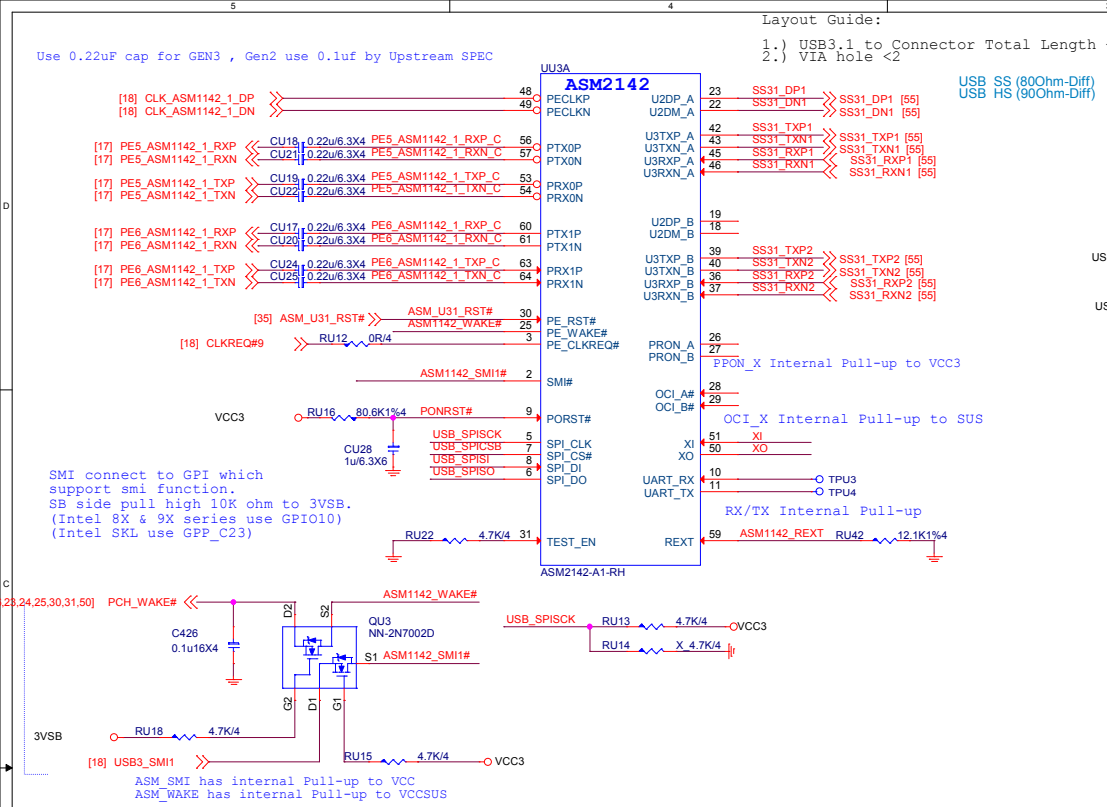
Layout Guide:

1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

USB SS (80Ohm-Diff)
USB HS (90Ohm-Diff)

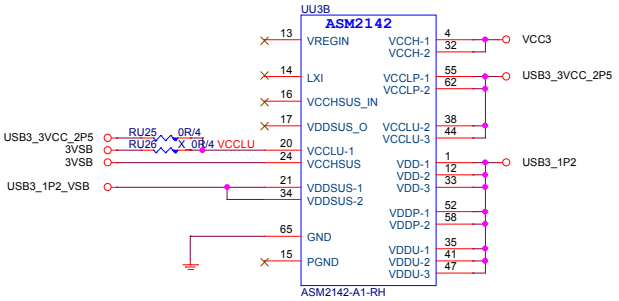
Power Consumption

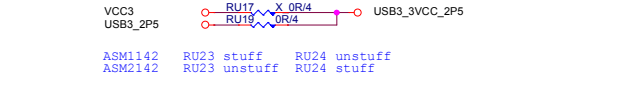
	3.3V	1.2V(1.05V	3.3VSUS	1.05VSUS(1.2VSUS	2.5V	Total Power
ASM1142	245mA	634mA	1mA	1mA	NA	1573.8(mW)
ASM2142	300mA	800mA	100mA	50mA	300mA	TDP



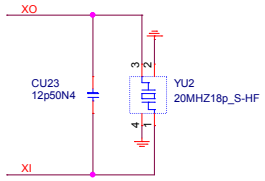
SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)

ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

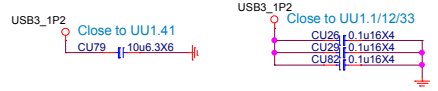


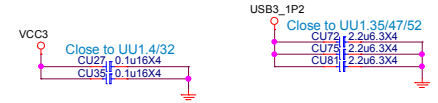


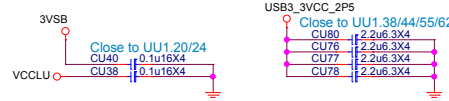
ASM1142 RU23 stuff RU24 unstuff
ASM2142 RU23 unstuff RU24 stuff



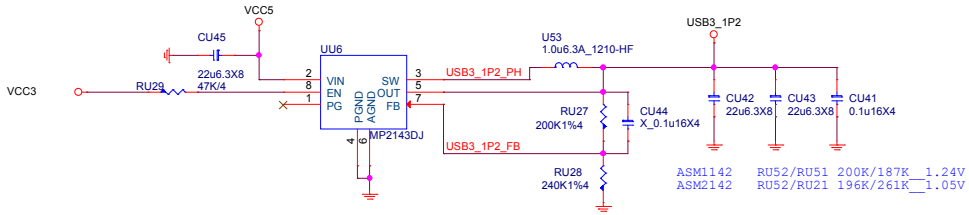
X0/XI (95hm-Diff,Spacing 30mil)



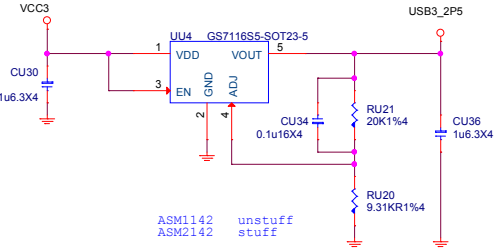




ASM1142 1.2 VCC Power

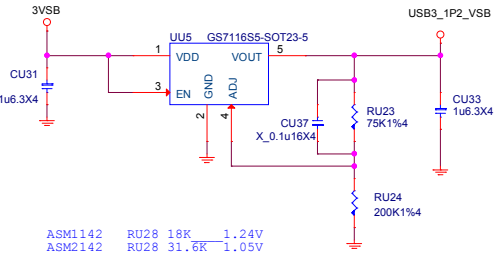


ASM1142 RU52/RU51 200K/187K 1.24V
ASM2142 RU52/RU21 196K/261K 1.05V



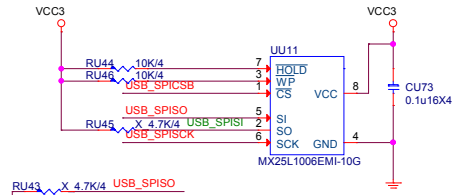
ASM1142 unstuff
ASM2142 stuff

ASM1142 1.2 VSB Power



ASM1142 RU28 18K 1.24V
ASM2142 RU28 31.6K 1.05V

EEPROM



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Size	Document Description	Rev
Custom	USB3.1-ASM2142AE-1	1.0

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F75504 layout placement must meet to spi/usb trace length spec with host.
As for as possible place near to host.

F75504 PM requst Remove 0407 mail

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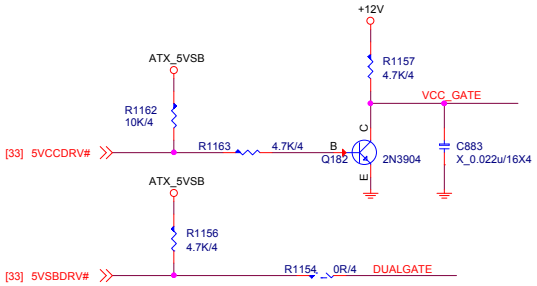
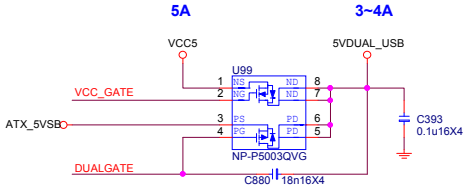
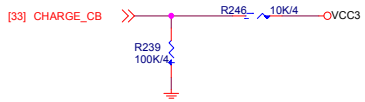
MA-7A94..	
Size: Custom	Document Description: PS2 USB
Rev: 1.0	
Date: Saturday, April 22, 2017	Sheet 52 of 85

5VDUAL_USB

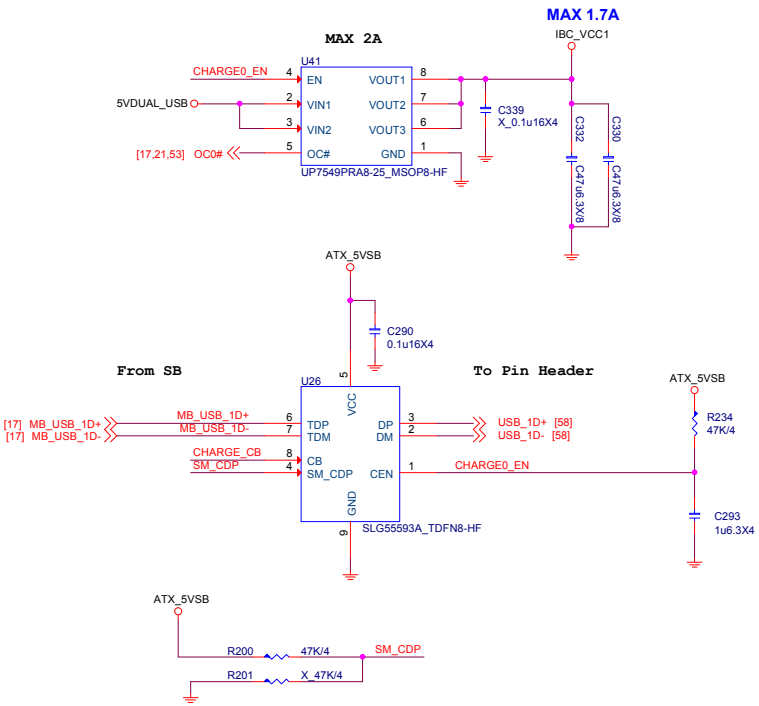




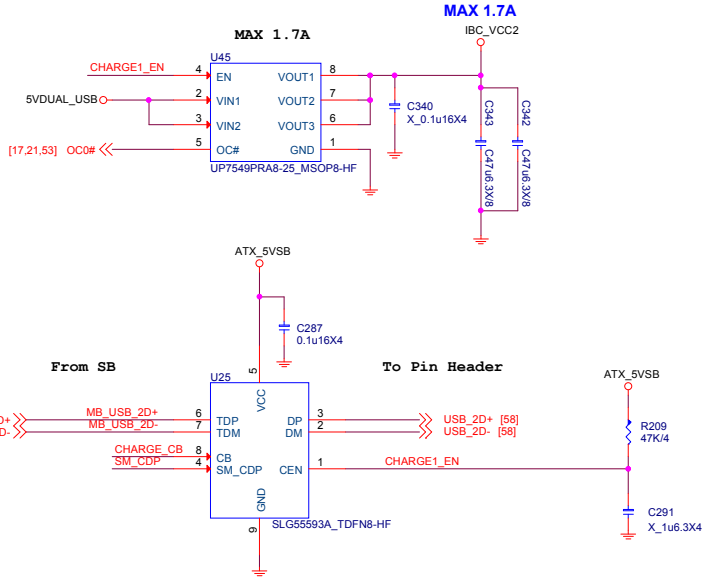
Pin power I_3VSB
Register power I_3VSB
Register reset I_3VSB



USB POWER PORT 0 For USB Charging



USB POWER PORT 1 For USB Charging



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	USB CHARGE_SLG55593A	1.0

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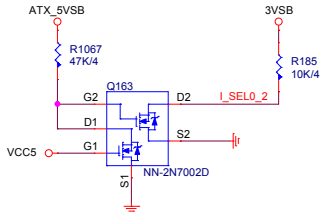
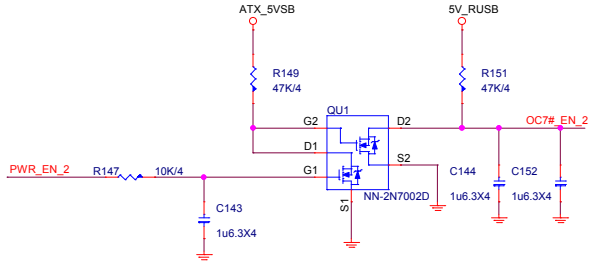
Current Mode

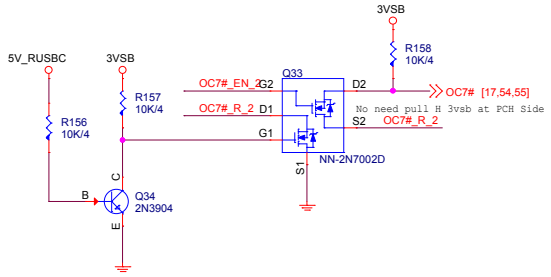


0	X	Default for 900mA
1	0	1.5A @5V
1	1	3A @5V

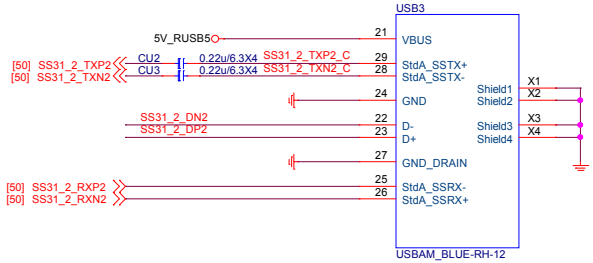
1.5A under S3 mode
3A under S0 mode

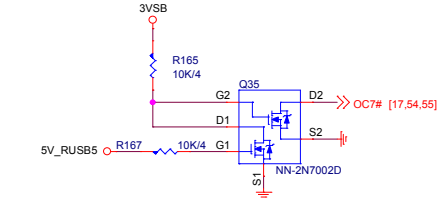
VBUS OC#

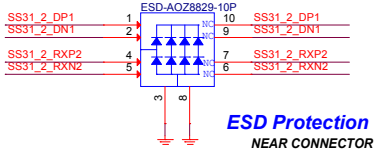




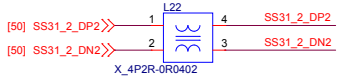
TYPE-A

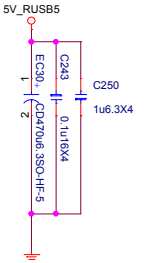




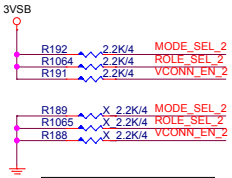


ESD Protection
NEAR CONNECTOR





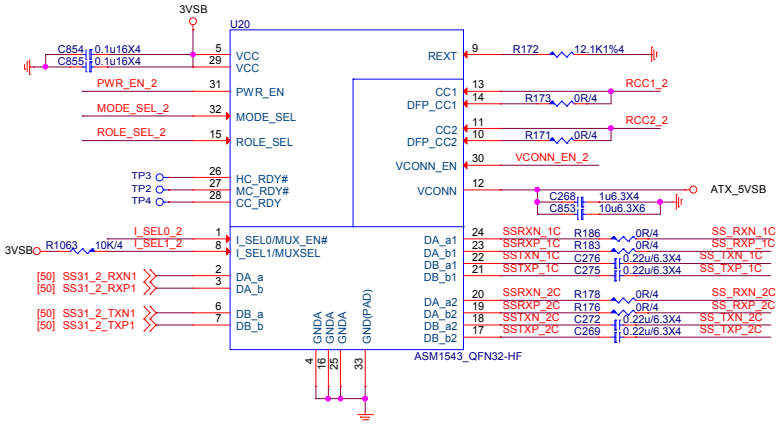
USB Type-C MUX with Configuration Channel (CC)

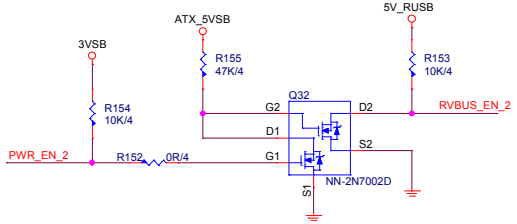


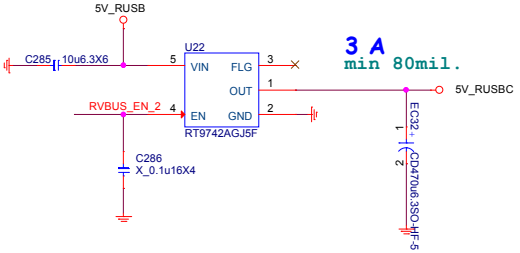
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

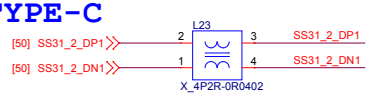
VCONN_EN	
1	enable
0	disable

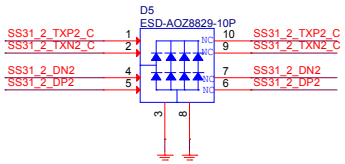




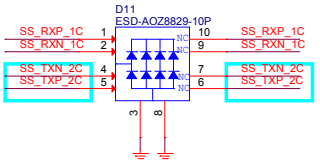


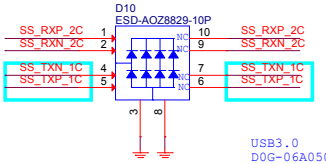
TYPE-C



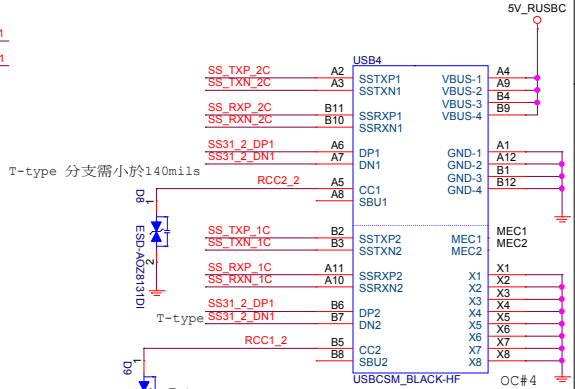


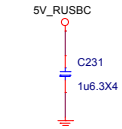
ESD Protection
NEAR CONNECTOR





USB3.0
D0G-06A050C-A68 Main
D0G-05A0300-I14 AVL
D0G-45B031C-O05 AVL





MSI	MICRO-STAR INT'L CO.,LTD		
	MA-7A94..		
Size: Custom	Document Description: USB TYPEC/A-2		Rev: 1.0
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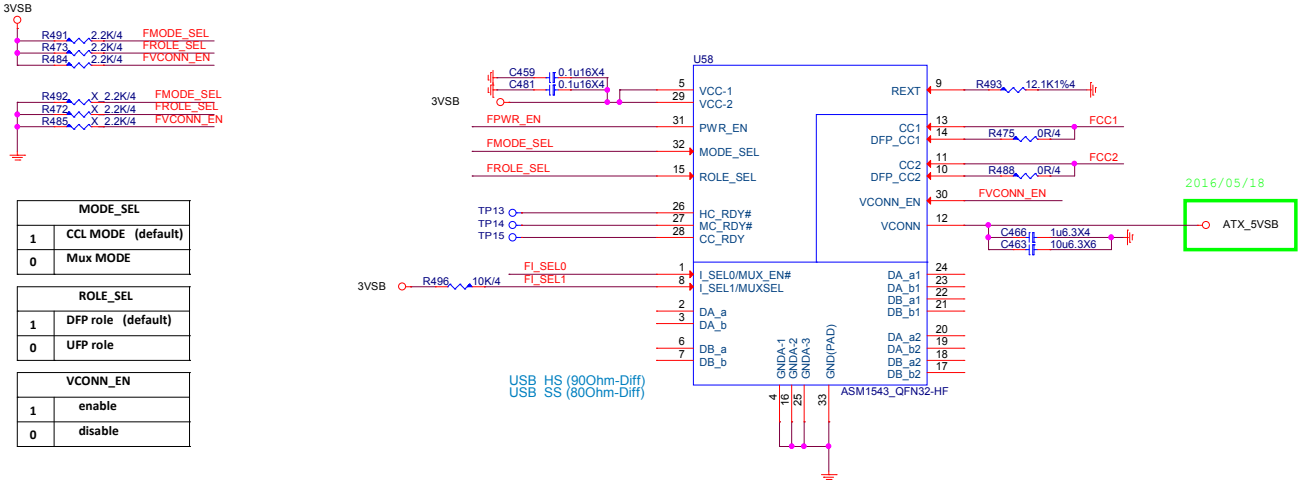
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

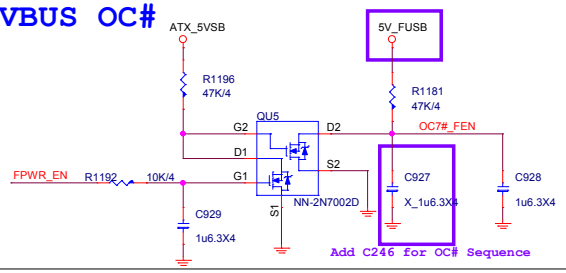


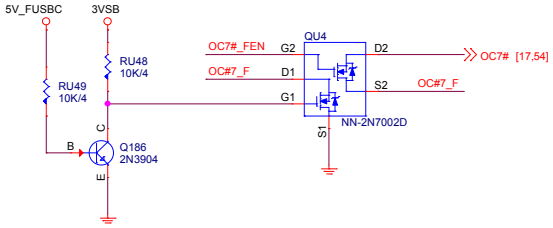
MODE_SEL	
1	CCL MODE (default)
0	Mux MODE

ROLE_SEL	
1	DFP role (default)
0	UFP role

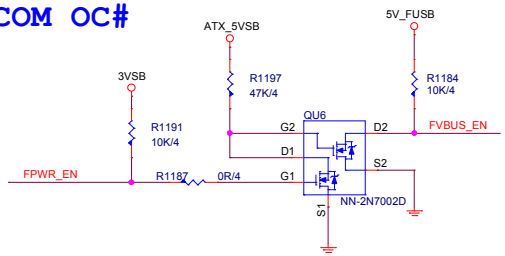
VCONN_EN	
1	enable
0	disable

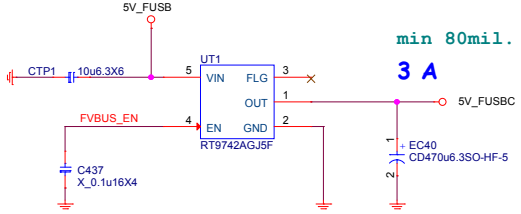
VBUS OC#



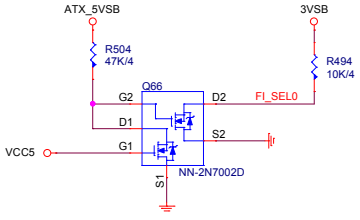


VCOM OC#





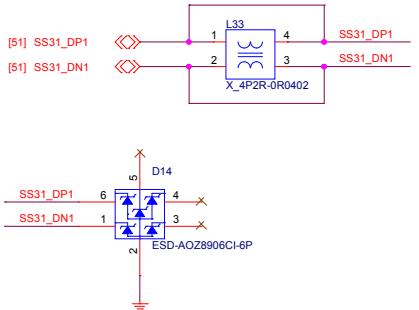
Current Mode

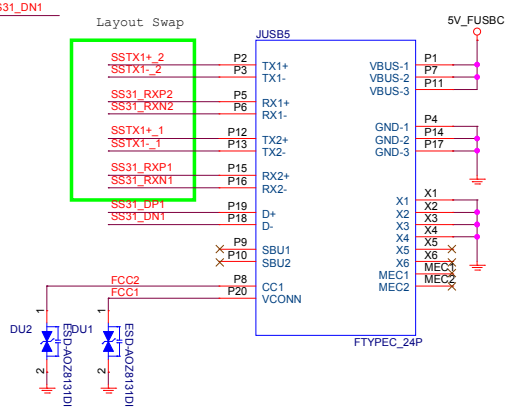


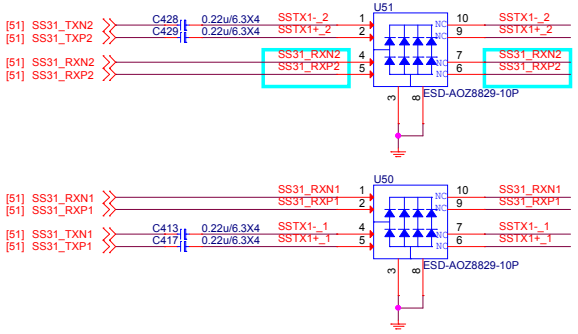
I_SEL0 : I_SEL1

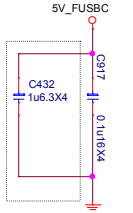
X	0	Default for 900mA
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode









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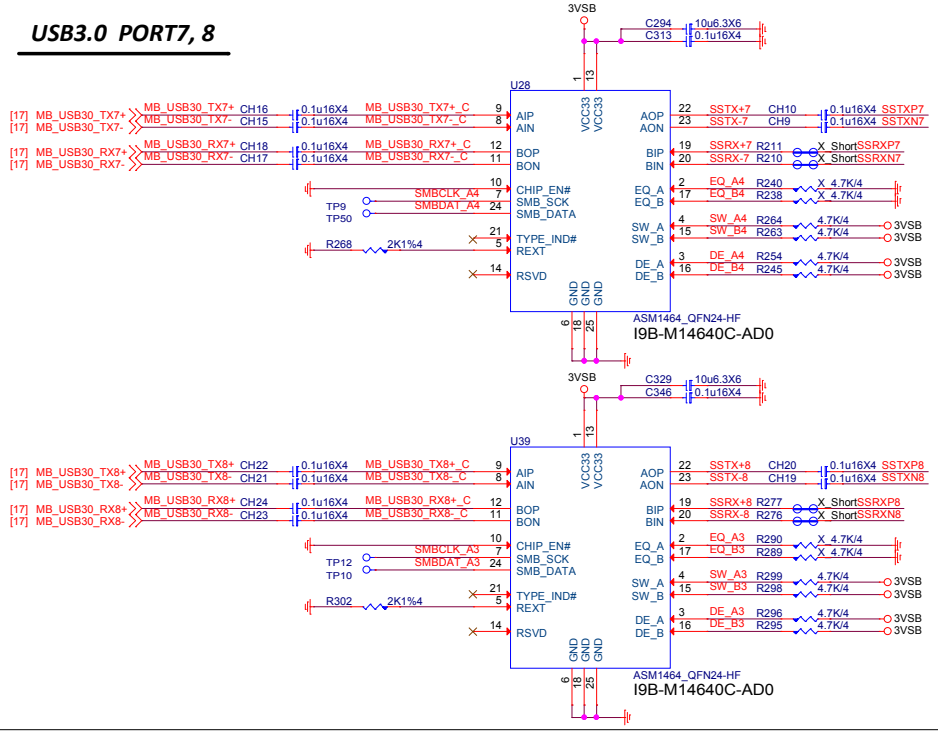
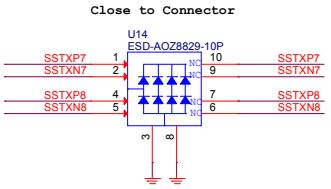
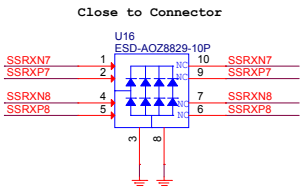
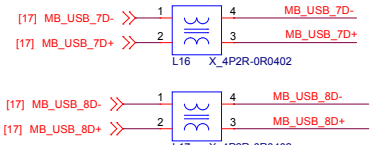
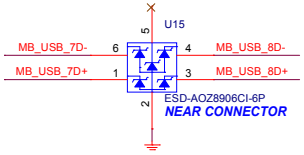
USB3.0 PORT7, 8

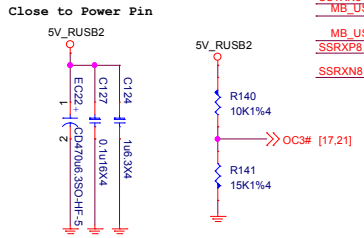


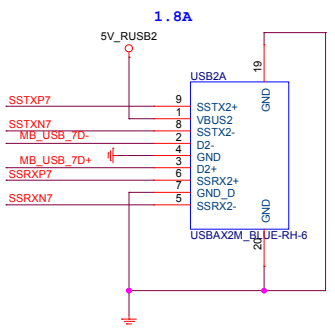


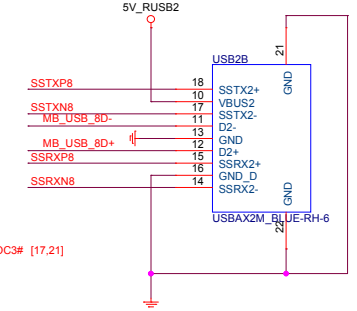




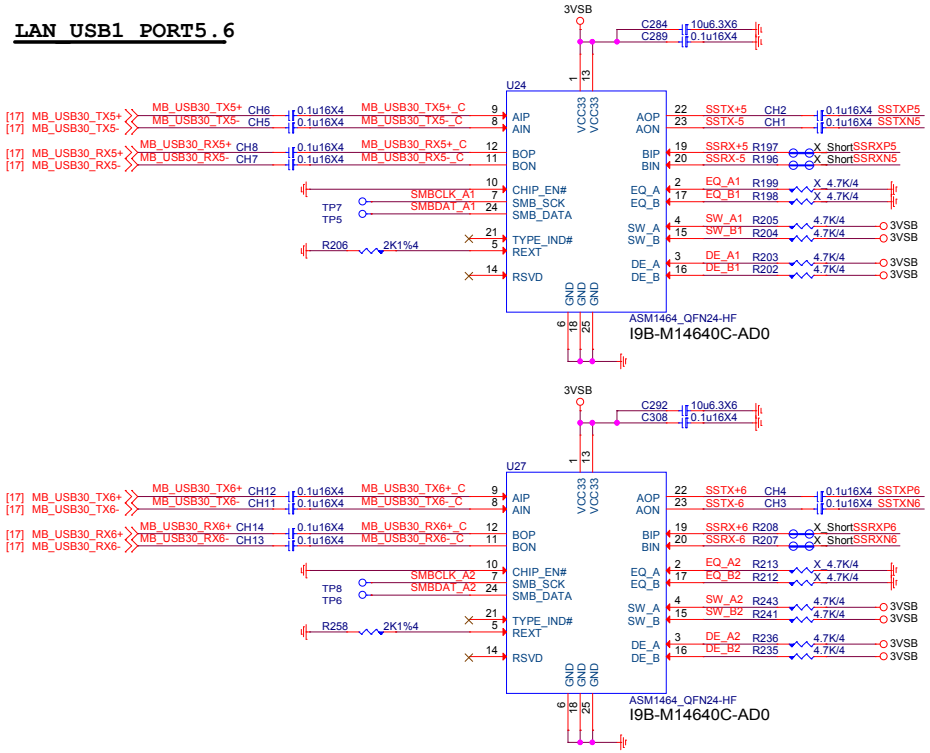


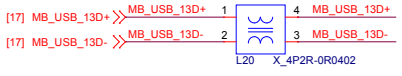


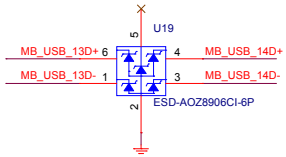


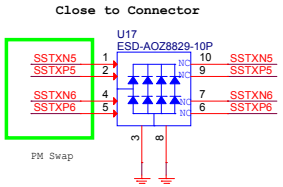


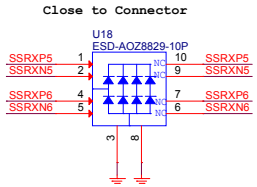
LAN_USB1 PORT5.6

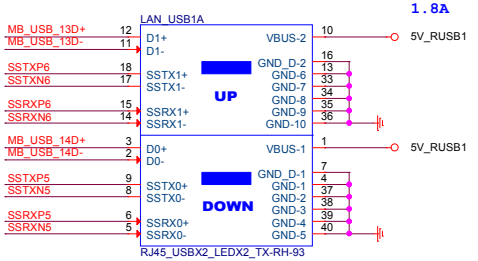


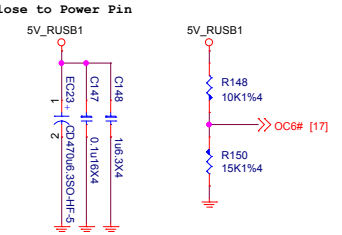












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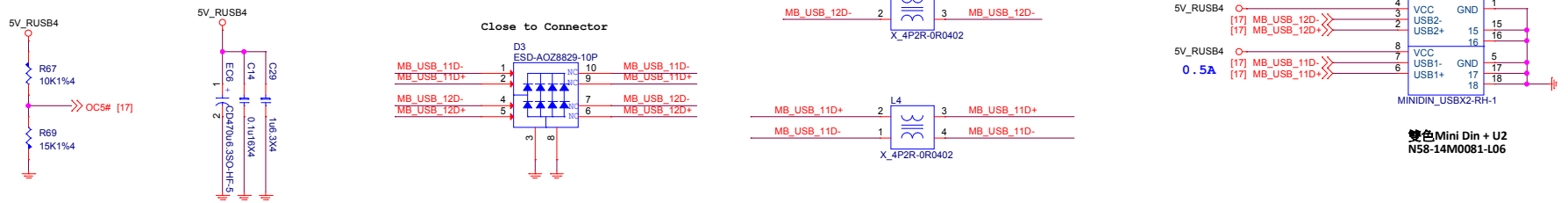
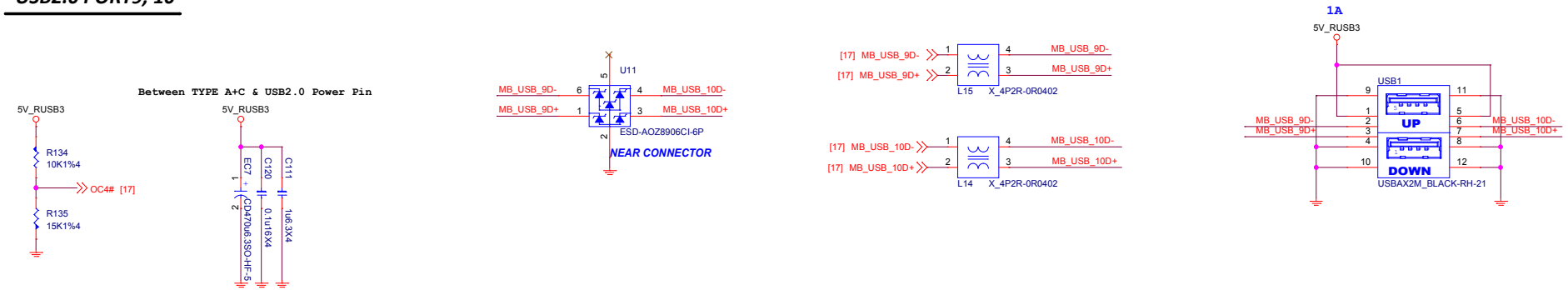
PS2_USB1



雙色Mini Din + U2
N58-14M0081-L06

USB2.0 PORT9, 10



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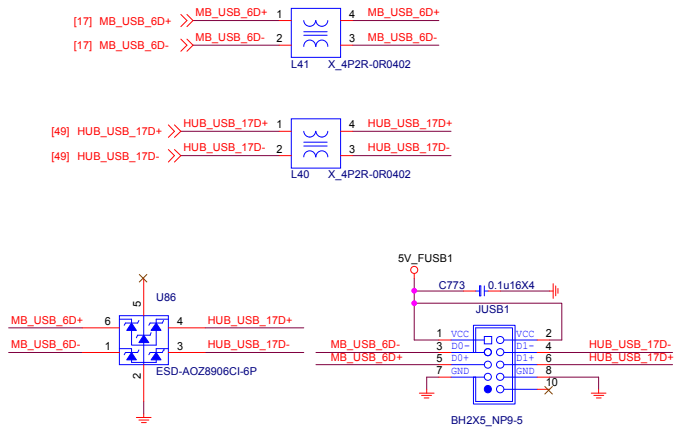
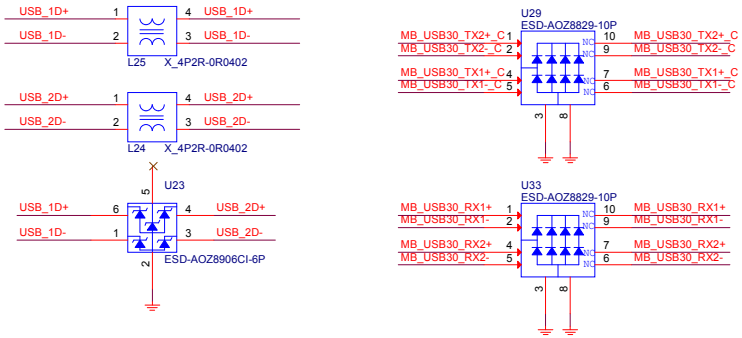
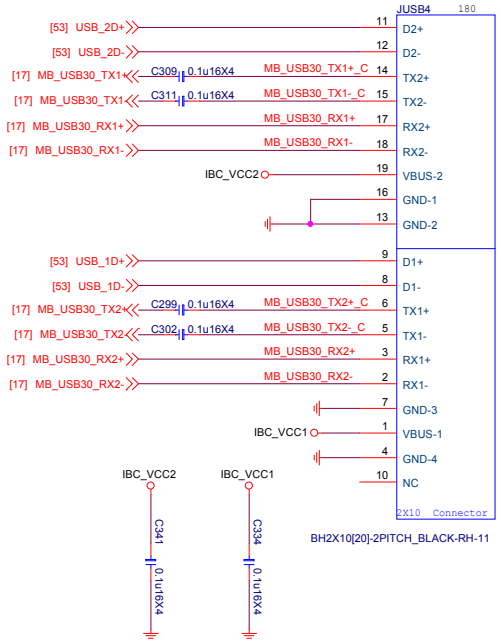
FRONT USB PORT 6. HUB PORT 17



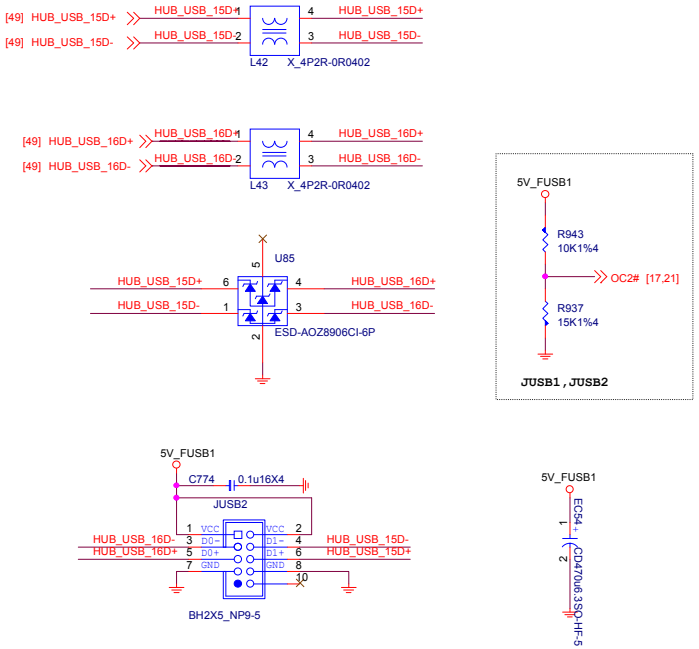
FRONT USB PORT 1,2



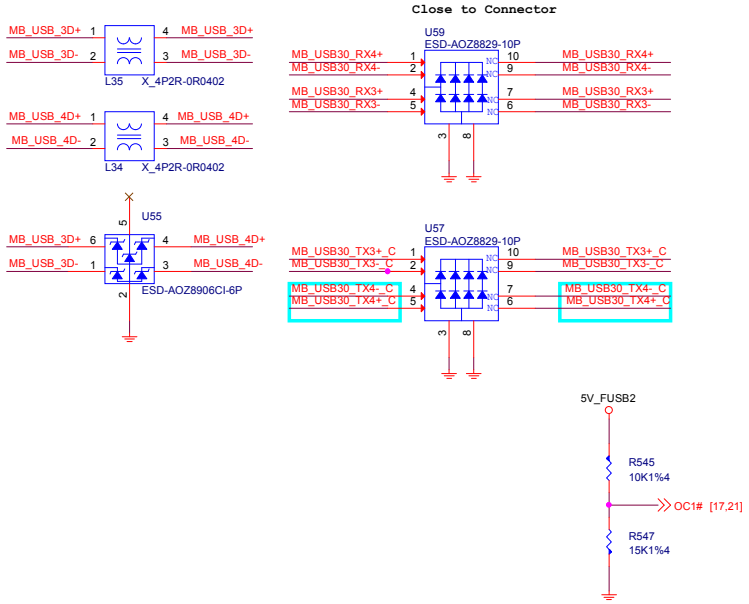
Vinafix.com

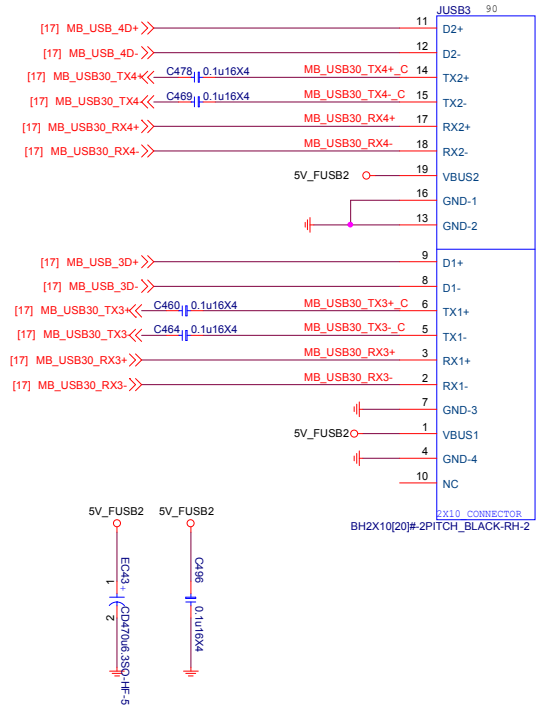


FRONT USB HUB PORT 15,16



FRONT USB PORT 3,4





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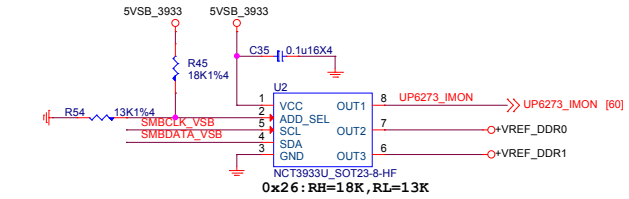
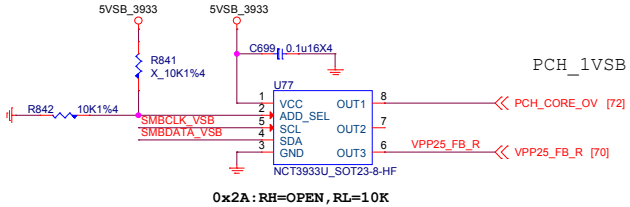
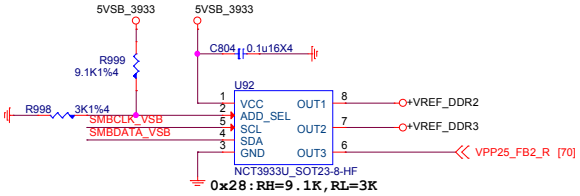
UPI VOLTAGE CONSOLE



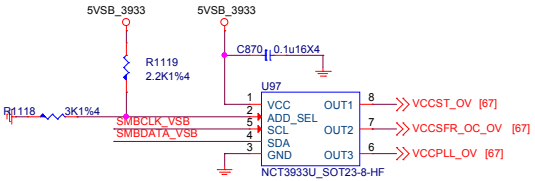
0x26:RH=18K,RL=13K



0x2A:RH=OPEN,RL=10K



0x28:RH=9.1K,RL=3K

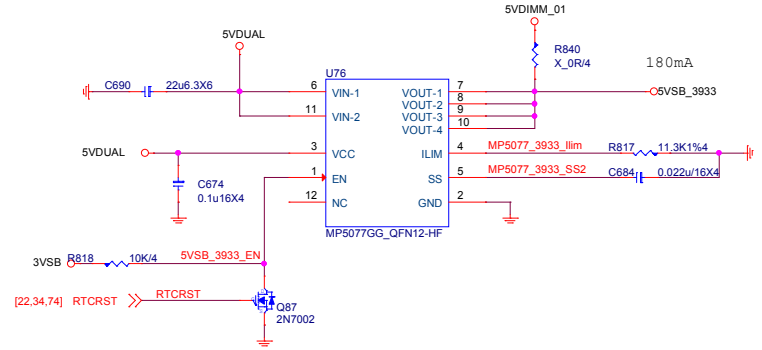


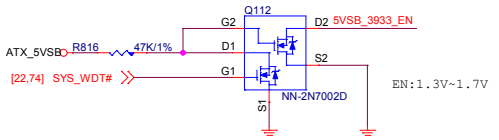
0x24:RH=2.2k,RL=3K

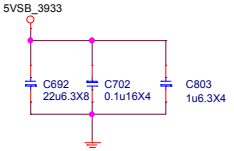
VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.2	3	3.9	OPEN
BUS_SEL	0%	25%	42%	58%	75%	100%

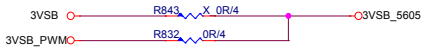
2017.04.14 Ryan mail Remove

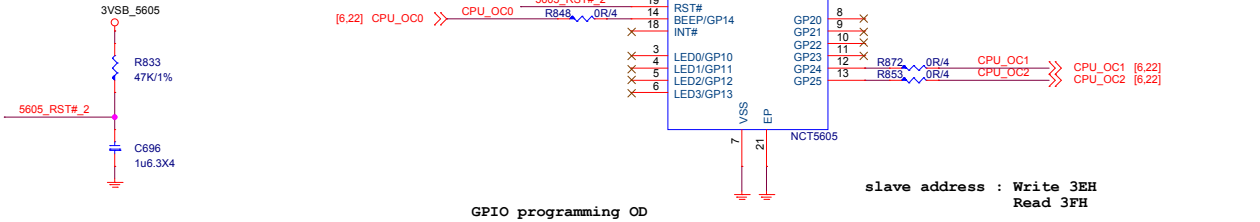






RSVD FOR OC





GPIO programming OD

slave address : Write 3EH
Read 3FH

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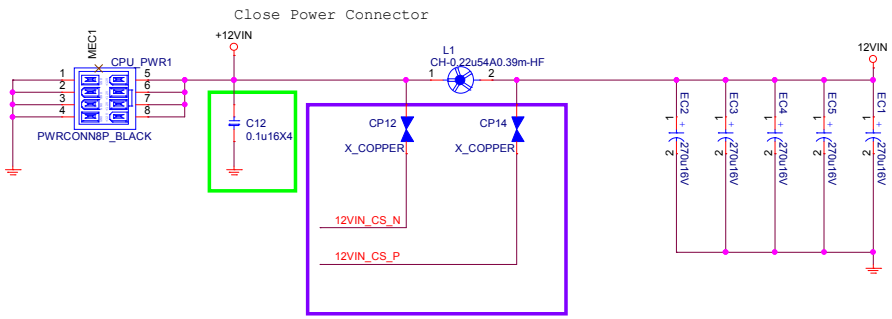
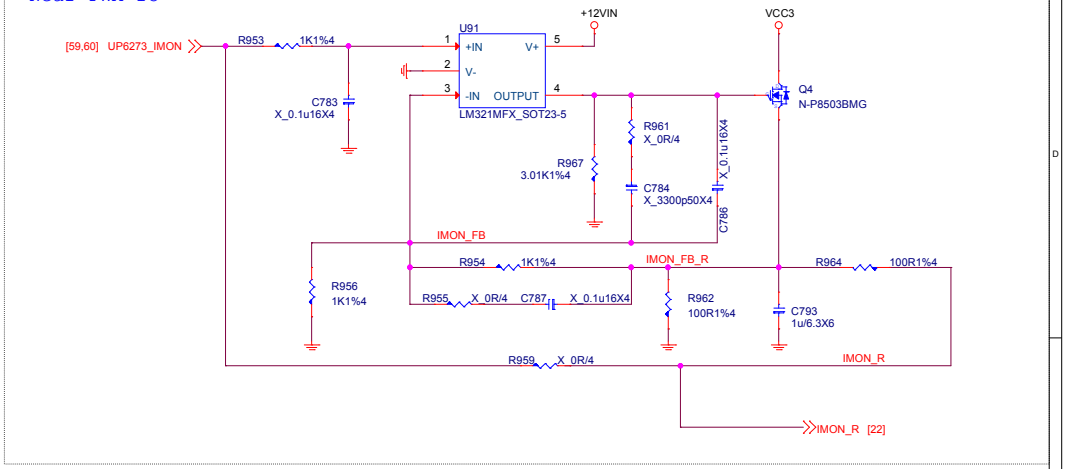
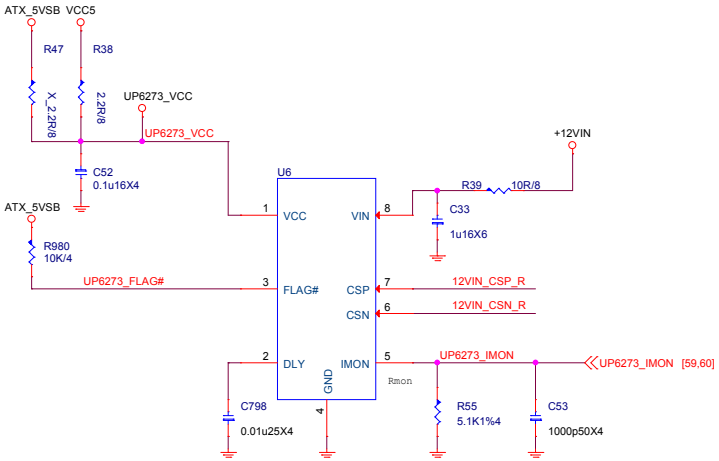


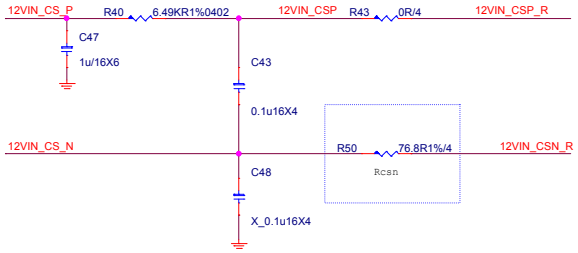


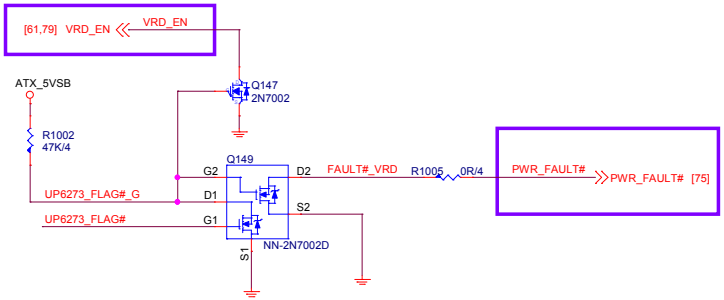


Iin=(Vmon*Rcsn)/(Rmon*Rdc)
Vmon=1.2
can change OCP trigger level by Rcsn and Rmon

一階2A
Rimon5.1Kohm
Rcsn0.0768Kohm
DCR0.39mohm
Vimon1.2V
Iocp46.33484163A

0.7* OCP * 400A *1.8V = 90% * 12 * I
I = 46.6 A





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VRMPWRGD LEVEL SHIFT

Vcore: ICC Max 100A
LL: 1.0 mohm
OCP: 400A

VSA: ICC Max 15A
OCP: 40A

0302 ADD

0302 ADD

0302 Remove

Close IC

Close IC

Close IC

RT6 close to Choke

Diff pair

Close to MOSFET

Close to PWM

防S5下漏電到VCC5

7B05 Add PWM6,7,8

teknisi indonesia

SMB Address: 0X70

0x26:RH=18K,RL=13K

PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X(IMVP8)

		VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X	0R
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R	X

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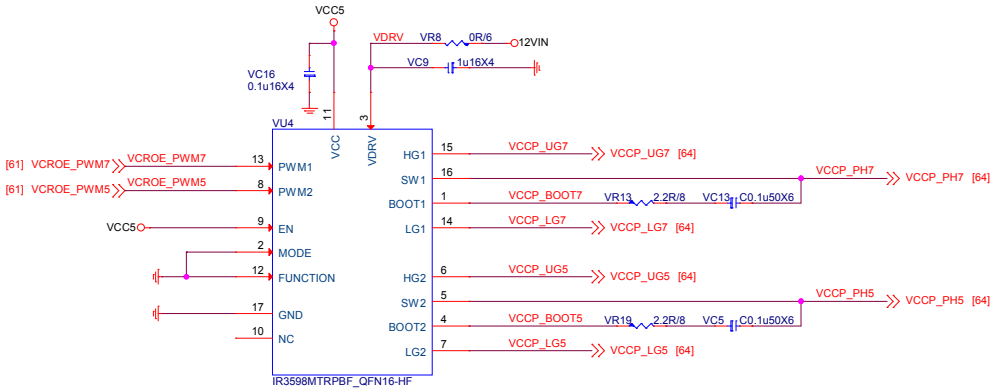

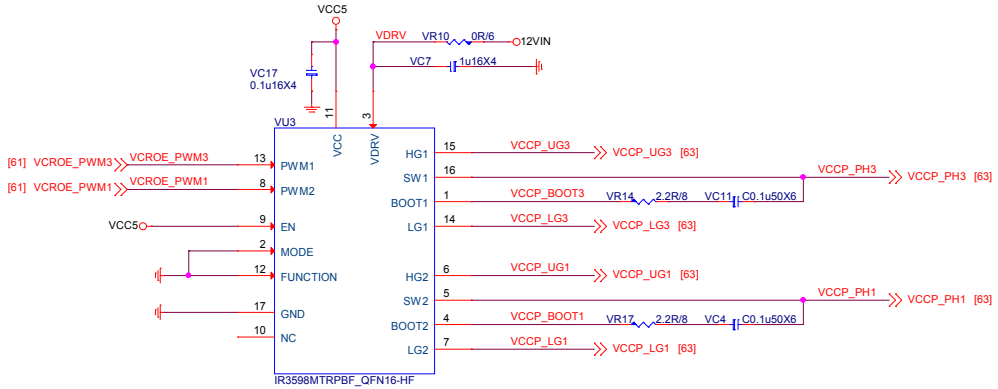

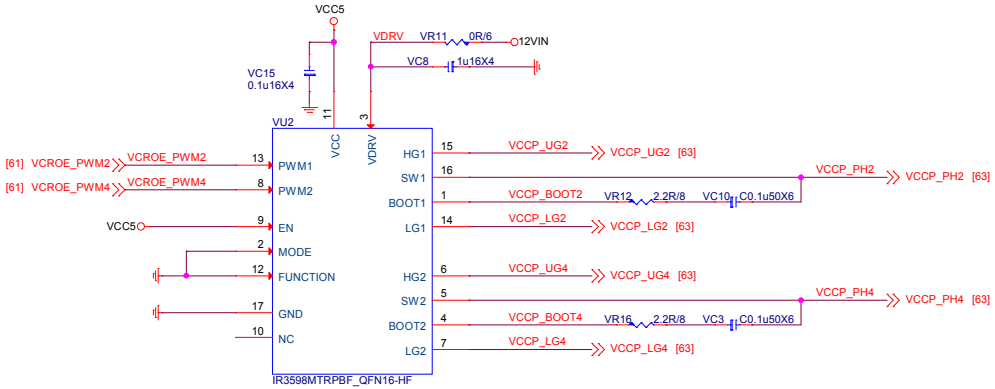

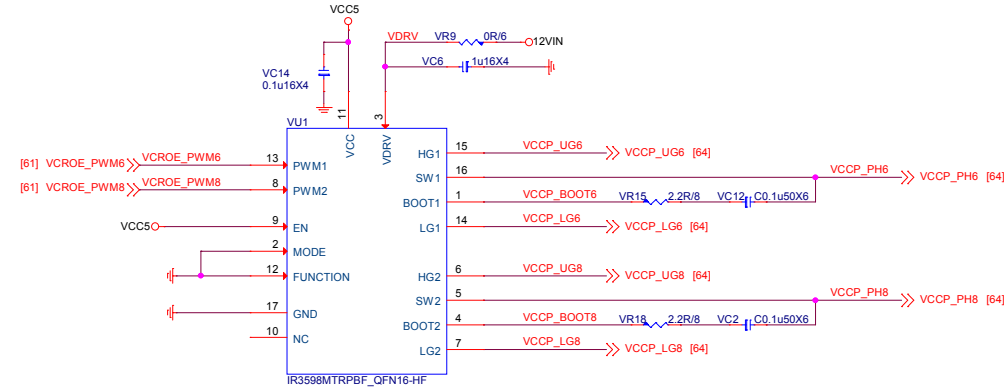

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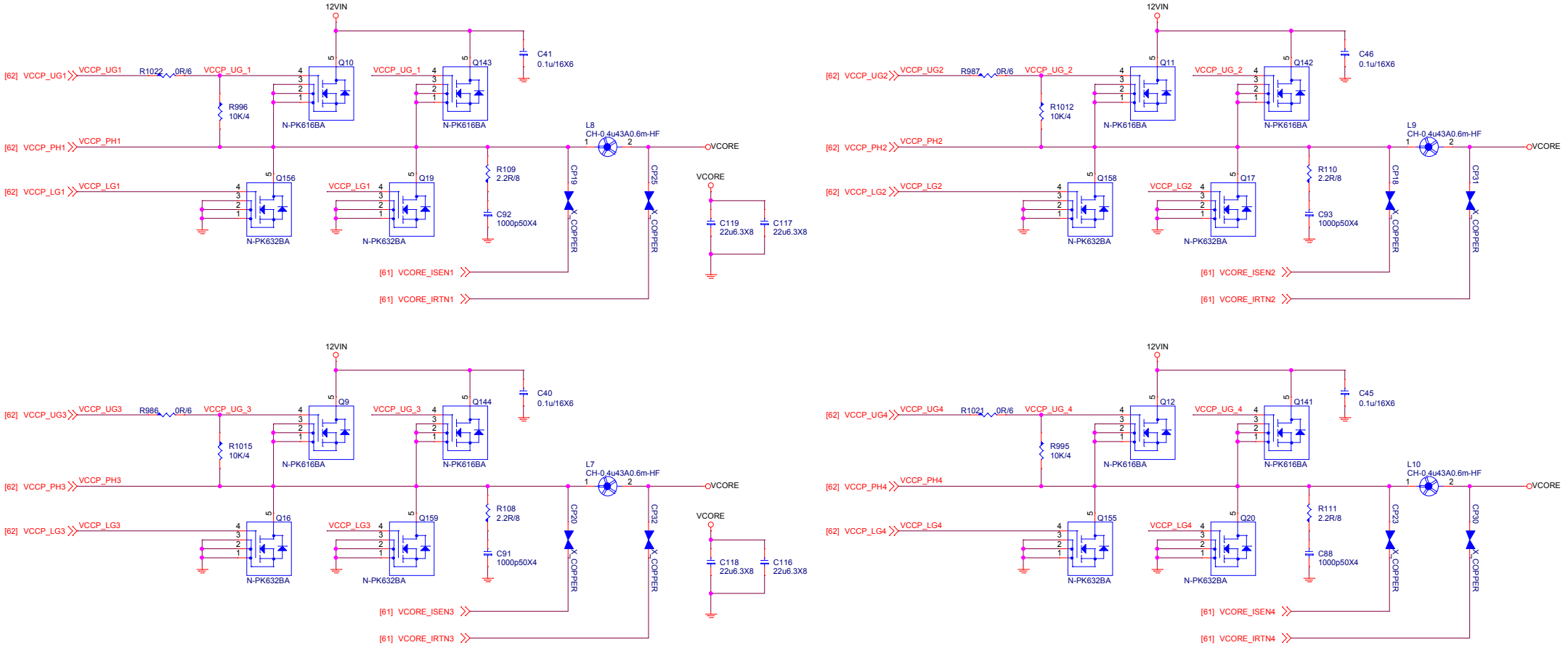

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MA-7A94..

Size	Document Description	Rev
Custom	CPU PWR-CORE-PH1~4	1.0

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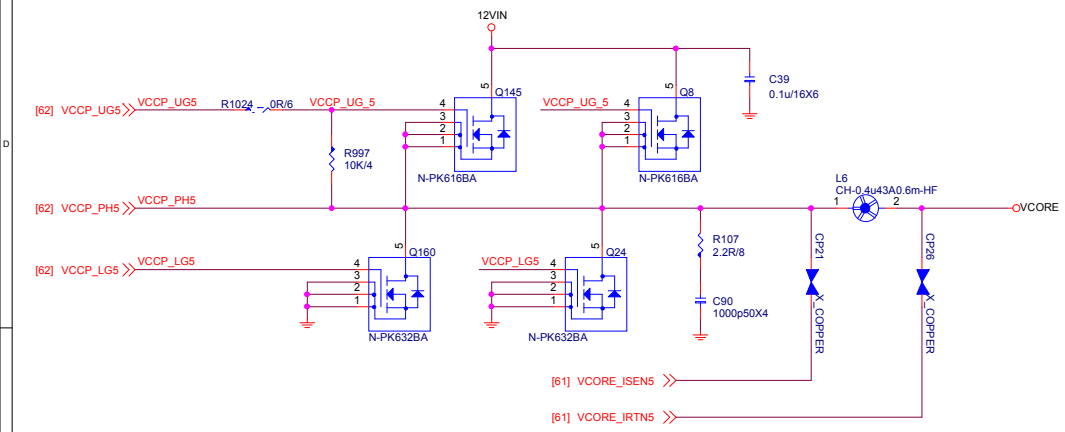

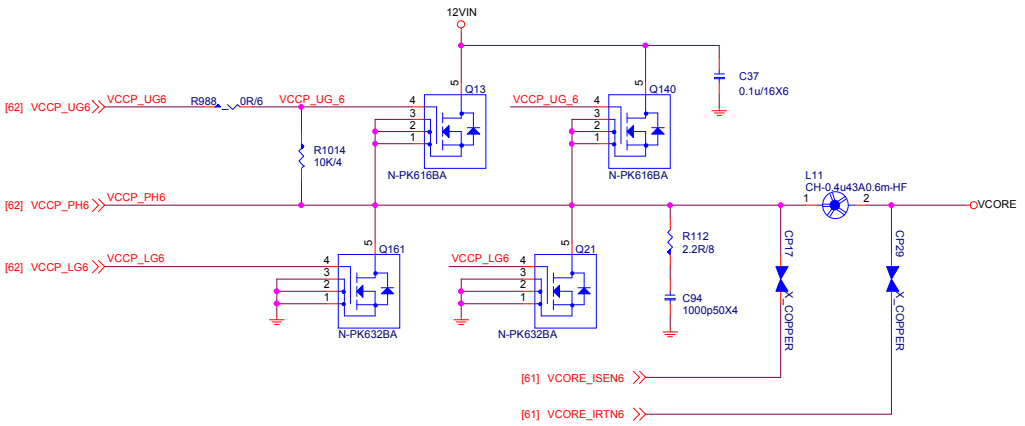

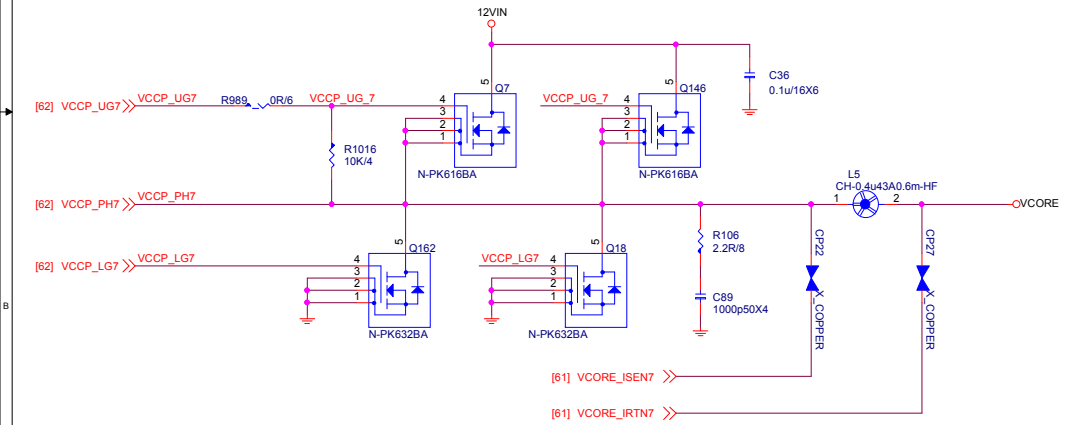

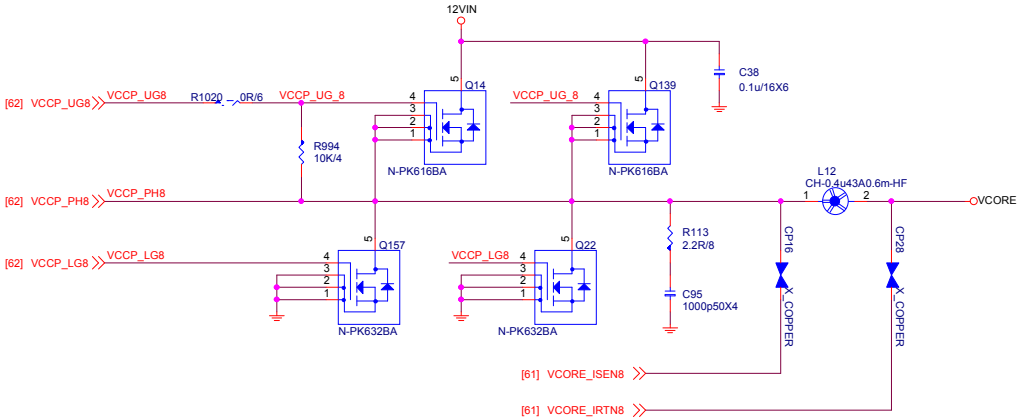

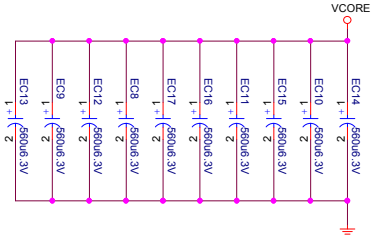

MICRO-STAR INT'L CO.,LTD

MA-7A94..

Size	Document Description	Rev
Custom	CPU PWR-CORE-PH5-8	1.0

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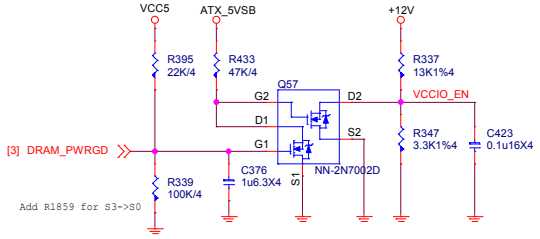
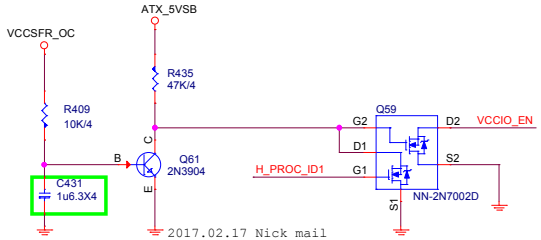
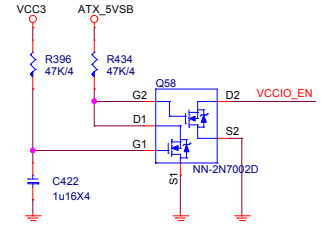
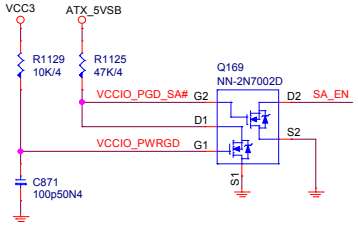
VCCIOPWRGD LEVEL SHIFT

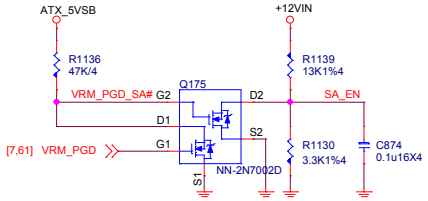


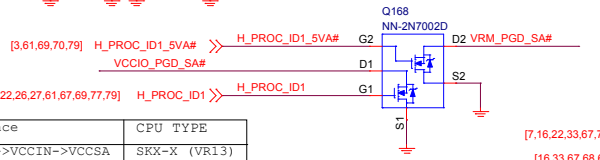
RSVD For KBL-X VCCIO Sequence



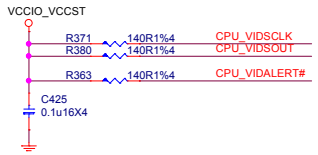


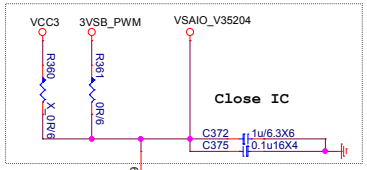




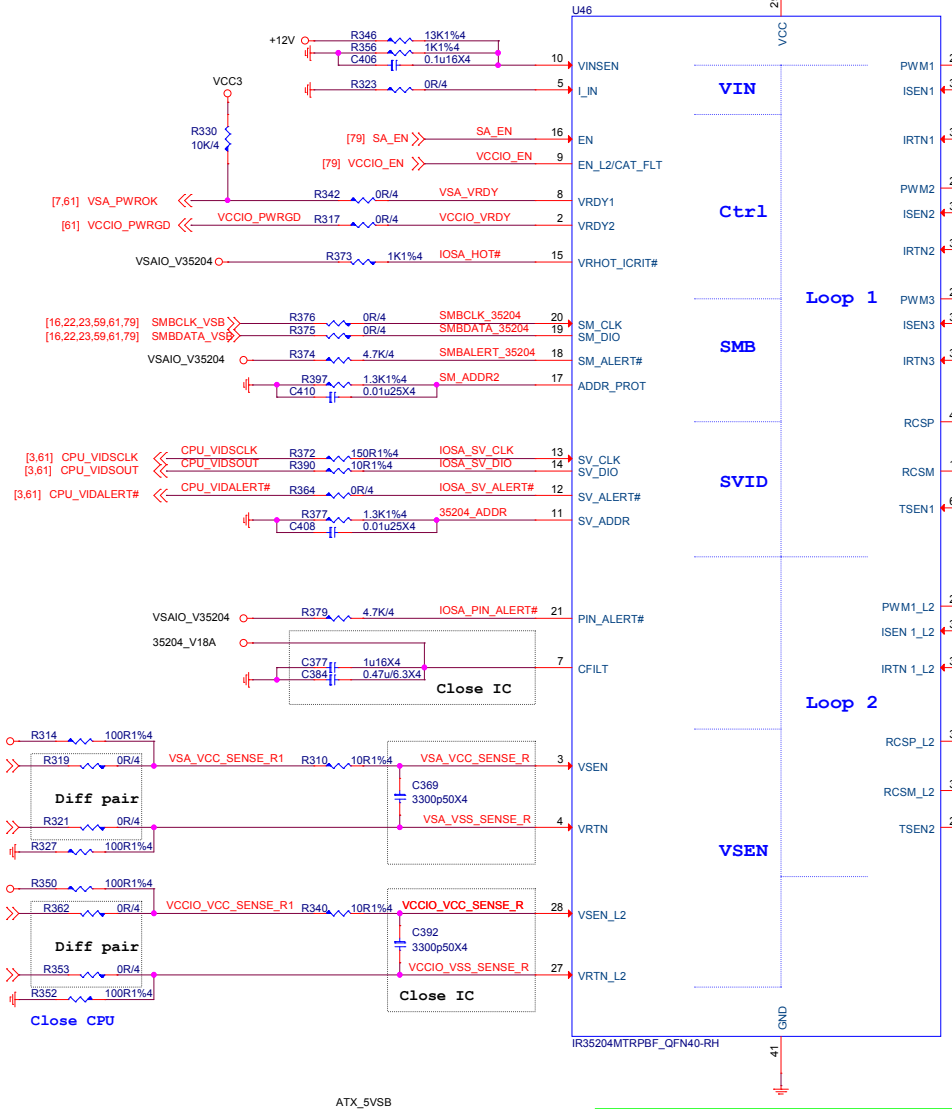


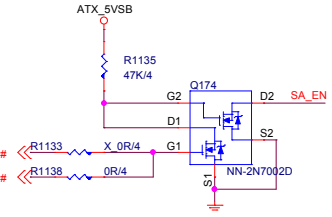
PROC_ID1	Sequence	CPU TYPE
1	VCCIO->VCCIN->VCCSA	SKX-X (VR13)
0	VCCIO->VCCSA->VCCIN	KBL-X(IMVP8)

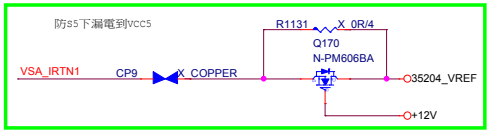


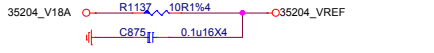


PROC_ID1	PROC_ID0	CPU TYPE
0	0	future CPU(IMVP9)
0	1	KBL-X(IMVP8)
1	0	future CPU
1	1	SKX-X (VR13)









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MA-7A94..	
Size: Custom	Document Description: VR13_VSA/VCCIO IR35204
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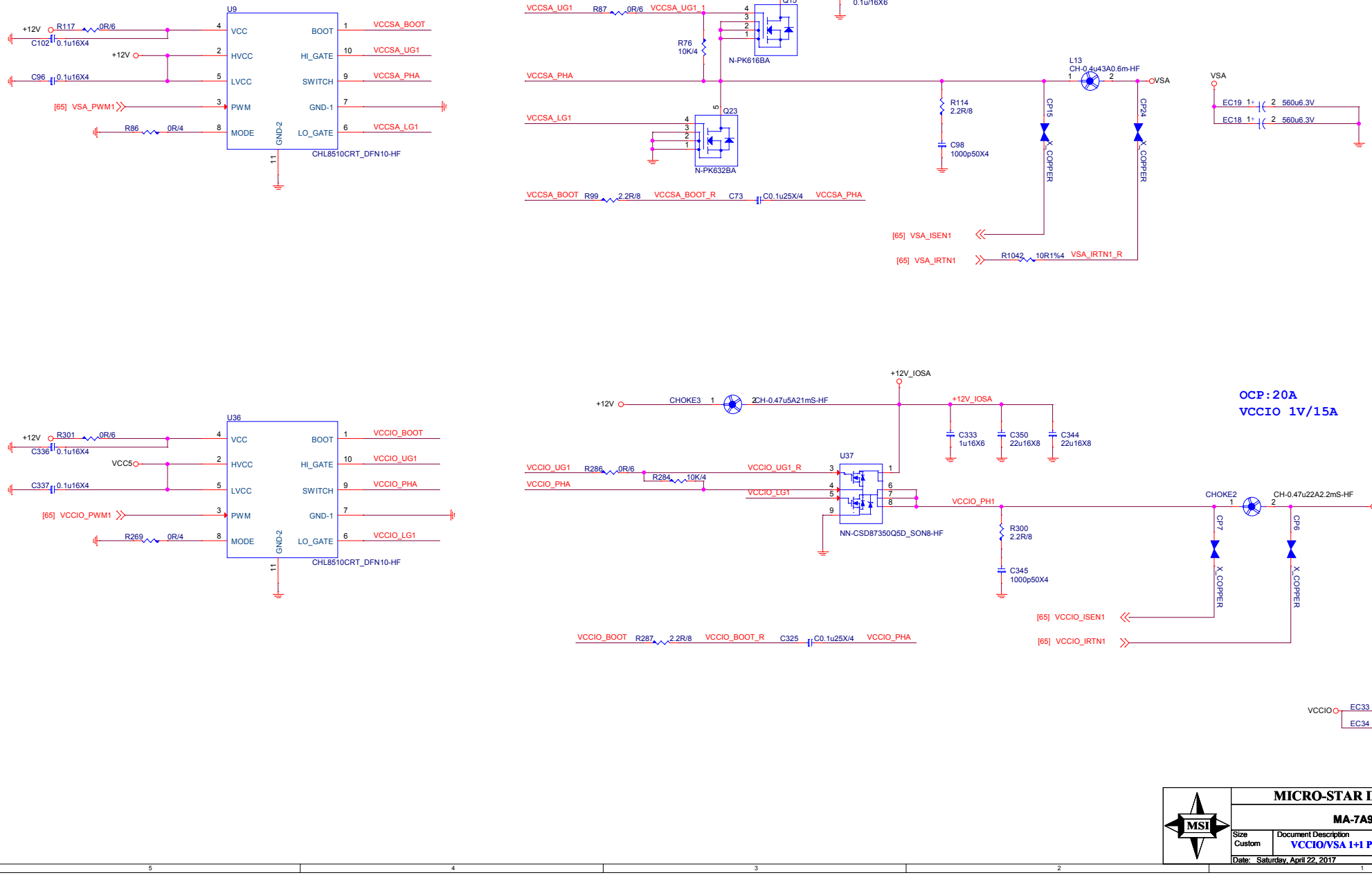
OCP:40A
VSA 0.5V-2.0V/ 15A
U9
+12V
R117 0R/6
C102 0.1u16X4
C96 0.1u16X4
[65] VSA_PWM1
R86 0R/4
VCC
HVCC
LVCC
PWM
MODE
GND-2
BOOT
HI_GATE
SWITCH
GND-1
LO_GATE
VCCSA_BOOT
VCCSA_UG1
VCCSA_PHA
VCCSA_LG1
CHL8510CRT_DFN10-HF
12VIN
C42 0.1u/16X6
Q15
N-PK616BA
R76 10K/4
VCCSA_UG1
R87 0R/6
VCCSA_UG1_1
Q23
N-PK632BA
VCCSA_LG1
VCCSA_BOOT
R99 2.2R/8
VCCSA_BOOT_R
C73 C0.1u25X/4
L13 CH-0.4u43A0.6m-HF
VSA
R114 2.2R/8
C98 1000p50X4
CP15 X_COPPER
CP24 X_COPPER
[65] VSA_ISEN1
[65] VSA_IRTN1
R1042 10R1%4
VSA_IRTN1_R
EC19 560u6.3V
EC18 560u6.3V
OCP:20A
VCCIO 1V/15A
U36
R301 0R/6
C336 0.1u16X4
VCC5
C337 0.1u16X4
[65] VCCIO_PWM1
R269 0R/4
VCCIO_BOOT
VCCIO_UG1
VCCIO_PHA
VCCIO_LG1
CHL8510CRT_DFN10-HF
+12V_IOSA
CHOKE3 CH-0.47u5A21mS-HF
C333 1u16X6
C350 22u16X8
C344 22u16X8
U37
R286 0R/6
R284 10K/4
VCCIO_UG1_R
NN-CSD87350Q5D_SON8-HF
VCCIO_PH1
R300 2.2R/8
C345 1000p50X4
CHOKE2 CH-0.47u22A2.2mS-HF
VCCIO
CP7 X_COPPER
CP6 X_COPPER
[65] VCCIO_ISEN1
[65] VCCIO_IRTN1
VCCIO_BOOT
R287 2.2R/8
VCCIO_BOOT_R
C325 C0.1u25X/4
EC33 560u6.3V
EC34 560u6.3V
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MA-7A94..
Size Custom
Document Description
VCCIO/VSA 1+1 PHASE
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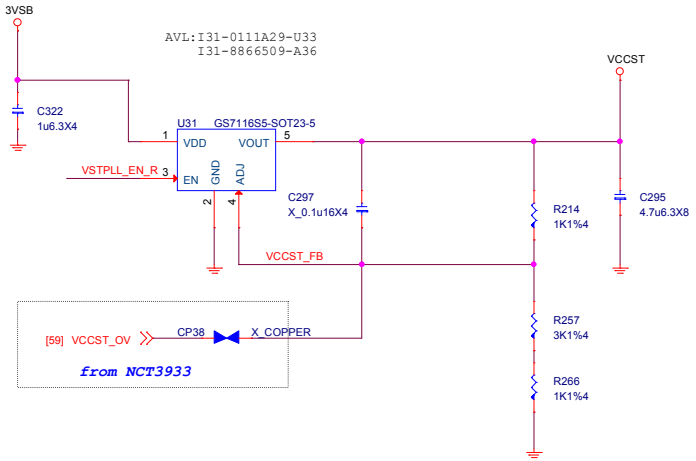
VCCST

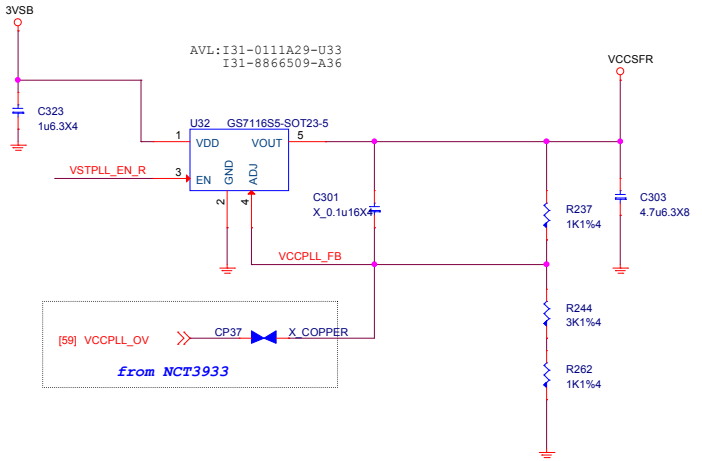
1.0V; 60mA



VCCIO ramped and stable before
beginning of VCCOPC/VCCEOPIO ramp
VCCST/PLL stable 1ms before PROCPWRGD

VCCSFR

1.0V; 150mA



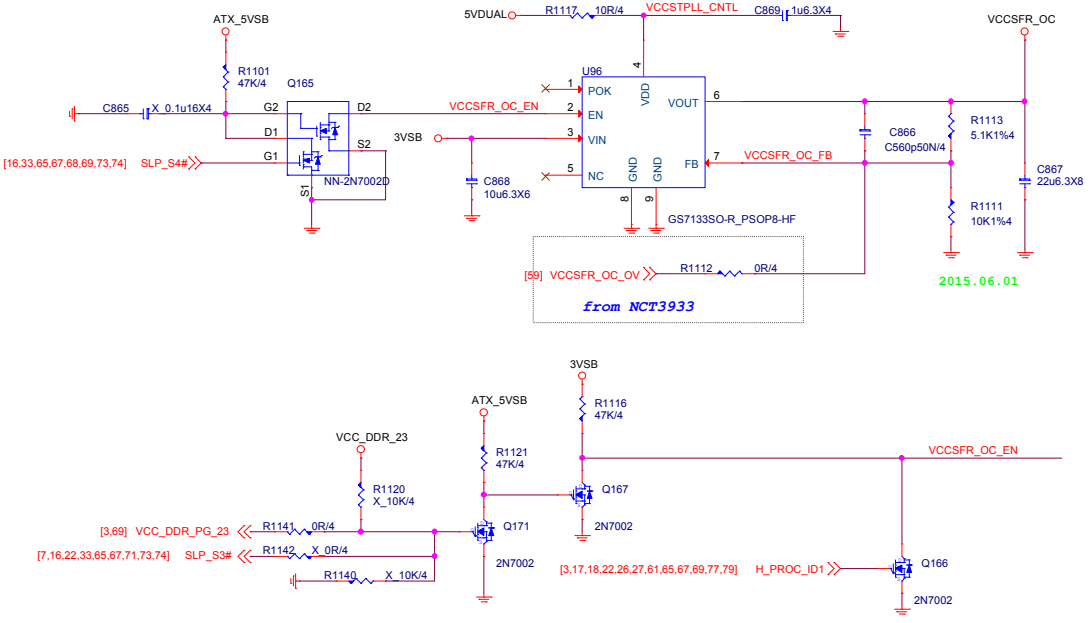
2017.03.27 Ryan mail remove vccst02

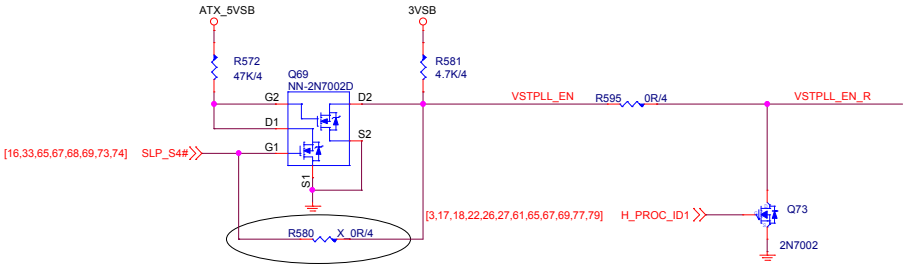
For non-OC system, configures +VCCSFR_OC as 1.2V

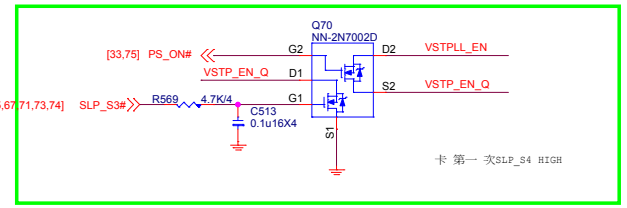
VCCSFR_OC

1.1V~1.5A; 500mA

EN:VIH1.2V
EN pin Maximum:VIN+0.3V







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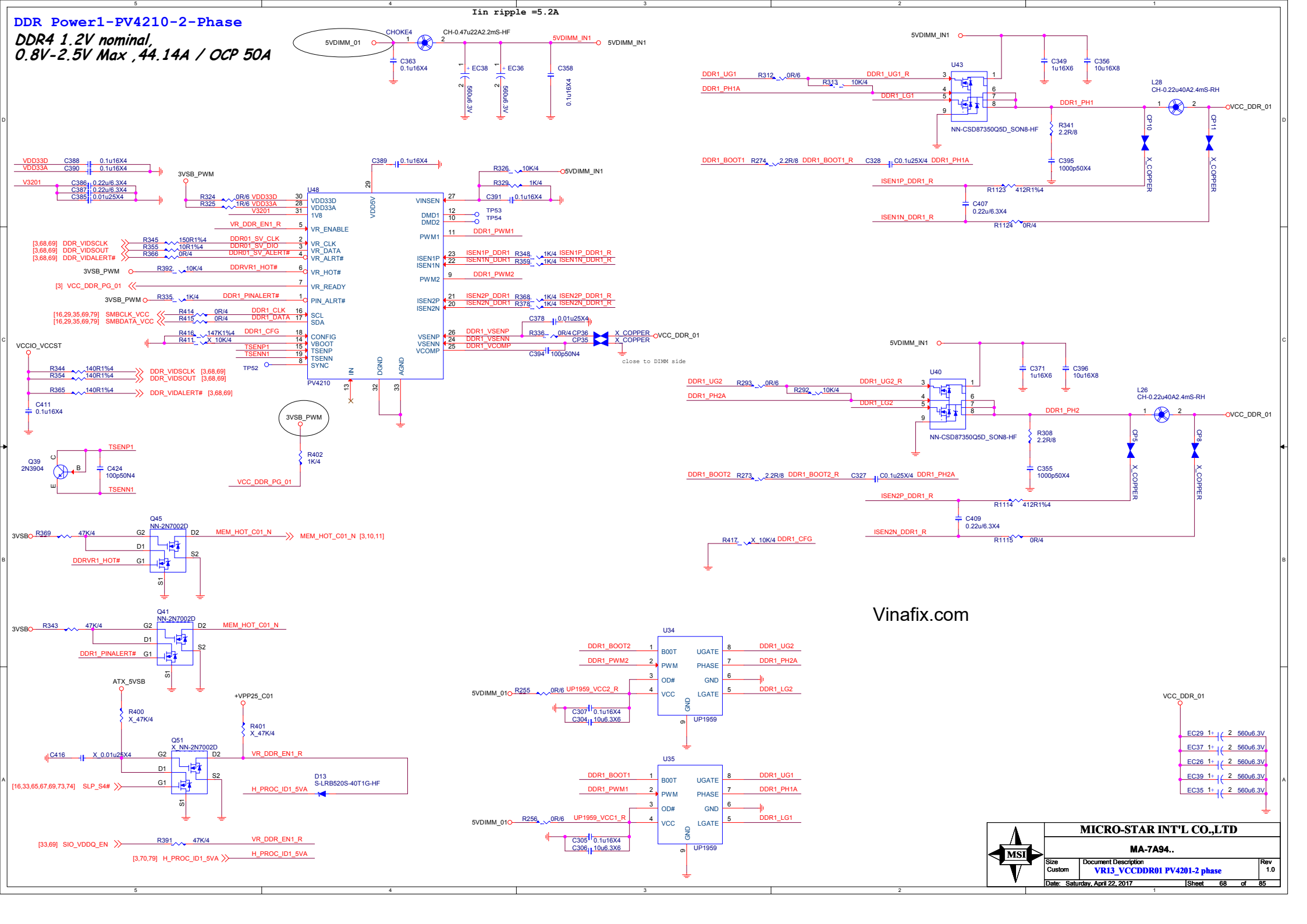
DDR Power1-PV4210-2-Phase

DDR4 1.2V nominal,
0.8V-2.5V Max ,44.14A / OCP 50A

Iin ripple =5.2A



Vinafix.com

MSI	MICRO-STAR INT'L CO.,LTD	
	MA-7A94..	
Size: Custom	Document Description: VR13_VCCDDR01 PV4201-2 phase	Rev: 1.0
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DDR Power1-PV4210-2-Phase

DDR4 1.2V nominal,
0.8V-2.5V Max ,44.14A / OCP 50A

Iin ripple =5.2A

5VDIMM_23 → CHOKE1 → CH-0.47u22A2.2mS-HF → 5VDIMM_IN2

C109 0.1u16X4 | EC20 560u6.3V | EC21 560u6.3V | C121 0.1u16X4

DDR2_BOOT1 R1048 2.2R/8 DDR2_BOOT1_R C812 0.1u/16X6 DDR2_PH1A

VDD33D_2 C75 0.1u16X4
VDD33A_2 C82 0.1u16X4
V4201_2 C67 0.22u/6.3X4
C68 0.22u/6.3X4
C66 0.01u25X4

3VSB_PWM → R94 0R/6 / R100 1R/6 → VDD33D_2 / VDD33A_2 / V4201_2

C78 0.1u16X4

U10 PV4210

29	VDD5V		
30	VDD33D	VINSEN	27
28	VDD33A	DMD1	12
31	1V8	DMD2	10
5	VR_ENABLE	PWM1	11
2	VR_CLK	ISEN1P	23
3	VR_DATA	ISEN1N	22
4	VR_ALRT#	PWM2	9
6	VR_HOT#	ISEN2P	21
7	VR_READY	ISEN2N	20
1	PIN_ALRT#	VSENP	26
16	SCL	VSENN	24
17	SDA	VCOMP	25
18	CONFIG		
14	VBOOT		
15	TSENP		
19	TSENN		
8	SYNC		
13	IN		
32	DGND		
33	AGND		

R103 10K/4 → 5VDIMM_IN2
R116 1K/4
C83 0.1u16X4
TP40 TP39
DDR2_PWM1
DDR2_PWM2

ISEN1P_DDR2 R123 1K/4 ISEN1P_DDR2_R
ISEN1N_DDR2 R122 1K/4 ISEN1N_DDR2_R
ISEN2P_DDR2 R121 1K/4 ISEN2P_DDR2_R
ISEN2N_DDR2 R120 1K/4 ISEN2N_DDR2_R

C99 0.01u25X4
DDR2_VSENP R124 0R/4 CP33 X_COPPER
DDR2_VSENN CP34 X_COPPER → VCC_DDR_23
DDR2_VCOMP C105 100p50N4
close to DIMM side

[3,68,69] DDR_VIDSCLK R85 150R1%4 DDR23_SV_CLK
[3,68,69] DDR_VIDSOUT R84 10R1%4 DDR23_SV_DIO
[3,68,69] DDR_VIDALERT# R83 0R/4 DDR23_SV_ALERT#
3VSB_PWM R82 10K/4 DDRVR2_HOT#
[3,67] VCC_DDR_PG_23
3VSB_PWM R1029 1K/4 DDR2_PINALERT#
[16,29,35,68,79] SMBCLK_VCC R104 0R/4 DDR2_CLK
[16,29,35,68,79] SMBDATA_VCC R115 0R/4 DDR2_DATA
DDR2_CFG
R101 X_10K/4
TSENP2
TSENN2
TP1

VCCIO_VCCST
R73 140R1%4 DDR_VIDSCLK [3,68,69]
R72 140R1%4 DDR_VIDSOUT [3,68,69]
R71 140R1%4 DDR_VIDALERT# [3,68,69]
C61 0.1u16X4

3VSB_PWM → R81 1K/4 → VCC_DDR_PG_23

Q31 2N3904 (C / B / E)
C811 100p50N4
TSENP2 / TSENN2

[3,17,18,22,26,27,61,65,67,77,79] H_PROC_ID1
DDR2_CFG R131 110K1%4
[3,61,65,70,79] H_PROC_ID1_5VA#
Q26 NN-2N7002D (G2 / D1 / D2 / S1 / S2)
R119 133K1%4 DDR2_CFG

2017.02.17 Nick mail

PROC_ID1	Config	CPU TYPE
1	133K	SKX-X (VR13) (SVID)
0	110K	KBL-X(IMVP8) (non SVID)

Q154 NN-2N7002D
3VSB R1031 47K/4 → G2 / D1 / G1 / D2 / S2 / S1
DDRVR2_HOT#
D2 → MEM_HOT_C23_N

Q153 NN-2N7002D
3VSB R1030 47K/4 → G2 / D1 / G1 / D2 / S2 / S1
DDR2_PINALERT#
D2 → MEM_HOT_C23_N → MEM_HOT_C23_N [3,12,13]

ATX_5VSB
R125 47K/4
C100 X_0.01u25X4
Q25 X_NN-2N7002D (G2 / D1 / G1 / D2 / S2 / S1)
[16,33,65,67,68,73,74] SLP_S4#
+VPP25_C23
R129 X_47K/4
VR_DDR_EN2_R
[33,68] SIO_VDDQ_EN
R130 47K/4 → VR_DDR_EN2_R

5VDIMM_IN2
U13 NN-CSD87350Q5D_SON8-HF
C126 1u16X6
DDR2_UG1 R137 0R/6 DDR2_UG1_R
R139 10K/4
DDR2_PH1A
DDR2_LG1
DDR2_PH1
L19 CH-0.22u40A2.4mS-RH
VCC_DDR_23
R143 2.2R/8
C129 1000p50X4
CP1 X_COPPER
CP4 X_COPPER
ISEN1P_DDR2_R
R1051 412R1%4
C107 0.22u/6.3X4
ISEN1N_DDR2_R
R1052 0R/4

5VDIMM_IN2
U12 NN-CSD87350Q5D_SON8-HF
C125 1u16X6
C123 10u16X8
DDR2_UG2 R136 0R/6 DDR2_UG2_R
R138 10K/4
DDR2_PH2A
DDR2_LG2
DDR2_PH2
L18 CH-0.22u40A2.4mS-RH
VCC_DDR_23
R142 2.2R/8
C128 1000p50X4
CP2 X_COPPER
CP3 X_COPPER
DDR2_BOOT2 R1047 2.2R/8 DDR2_BOOT2_R C813 0.1u/16X6 DDR2_PH2A
ISEN2P_DDR2_R
R1053 412R1%4
C106 0.22u/6.3X4
ISEN2N_DDR2_R
R1054 0R/4

U94 UP1959
DDR2_BOOT1 → B00T / DDR2_UG1
DDR2_PWM1 → PWM / PHASE / DDR2_PH1A
OD# / GND
5VDIMM_23 R1049 0R/6 UP1959_VCC3_R → VCC / LGATE / DDR2_LG1
C814 0.1u16X4
C816 10u6.3X6

U93 UP1959
DDR2_BOOT2 → B00T / DDR2_UG2
DDR2_PWM2 → PWM / PHASE / DDR2_PH2A
OD# / GND
5VDIMM_23 R1050 0R/6 UP1959_VCC4_R → VCC / LGATE / DDR2_LG2
C815 0.1u16X4
C817 10u6.3X6

VCC_DDR_23
EC27 560u6.3V
EC24 560u6.3V
EC28 560u6.3V
EC25 560u6.3V
EC31 560u6.3V

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Document Description: VR13_VCCDDR23 PV4201-2 phase
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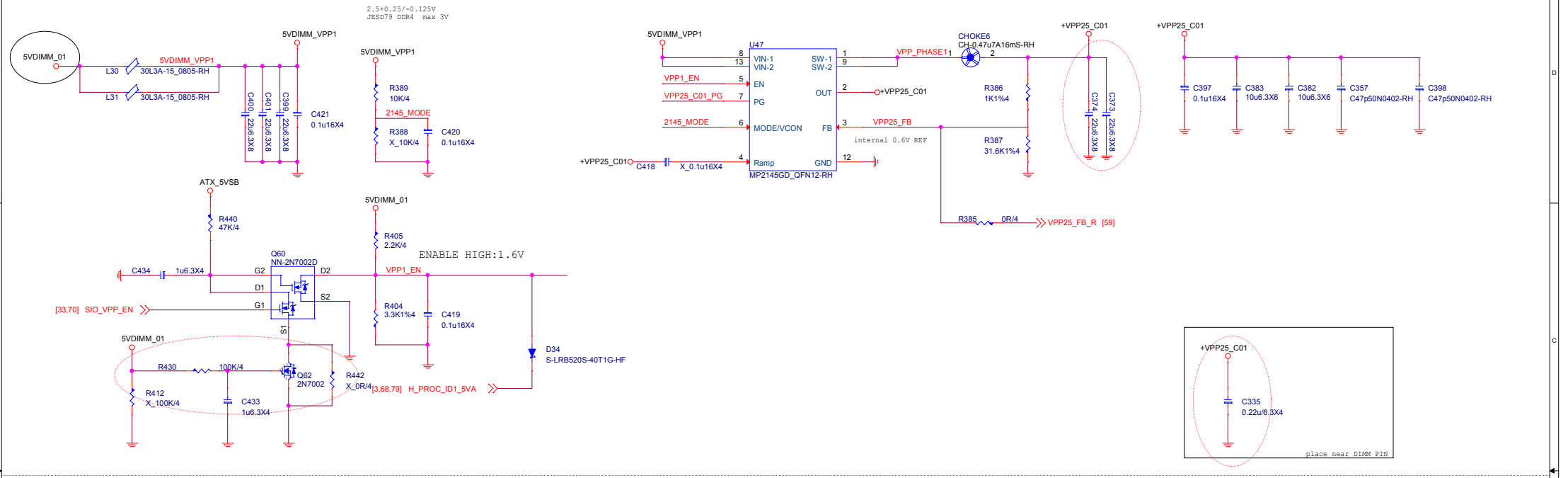
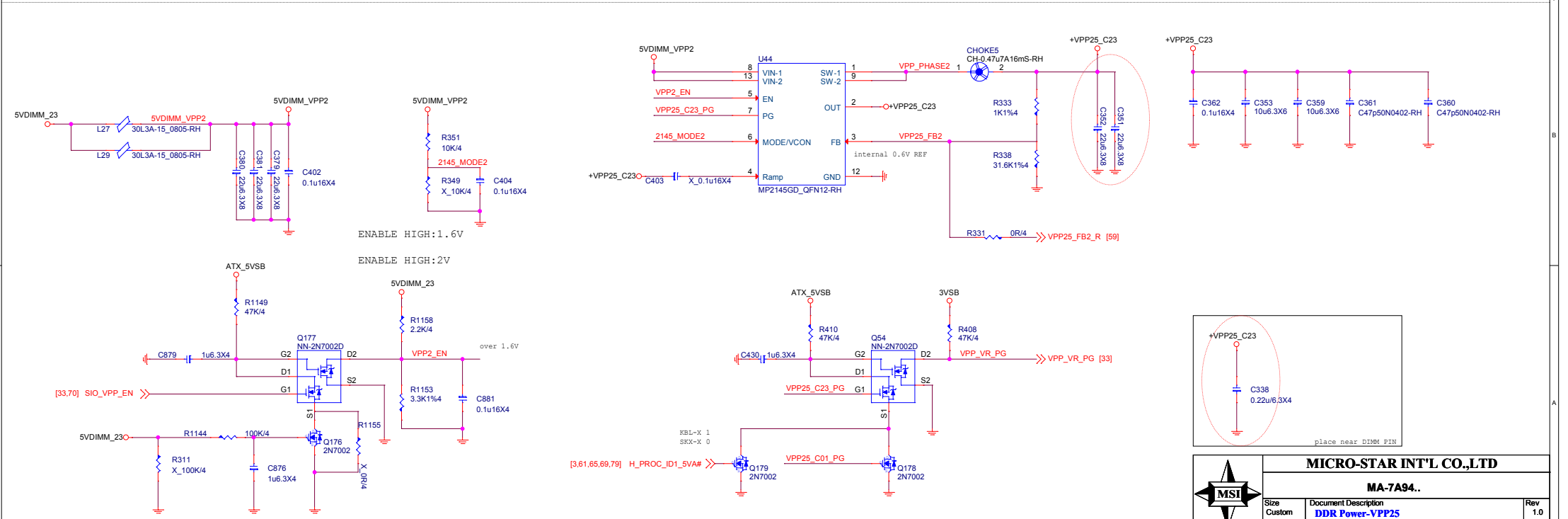
4DIMM :6A FOR DDR VPP





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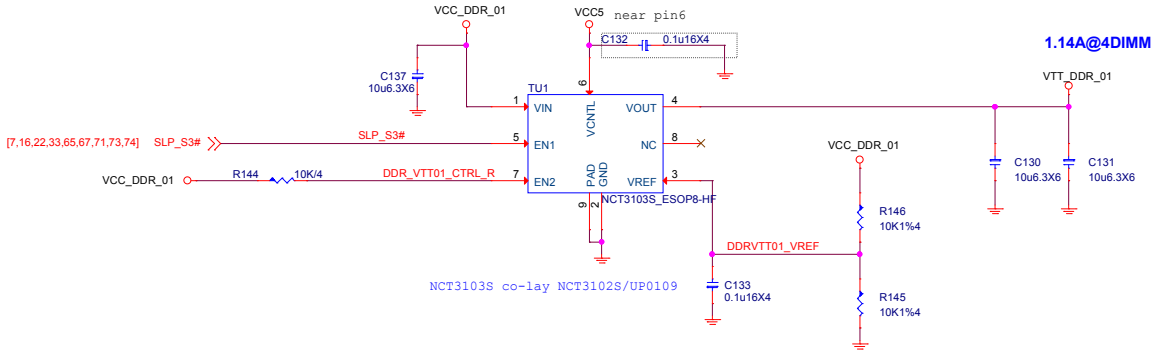
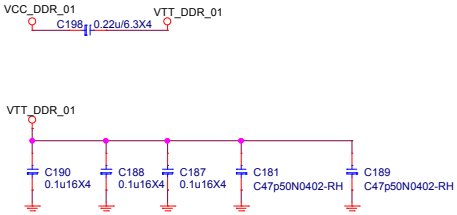
MA-7A94..		
Size: Custom	Document Description: DDR Power-VPP25	Rev: 1.0
Date: Saturday, April 22, 2017	Sheet 70 of 85	

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

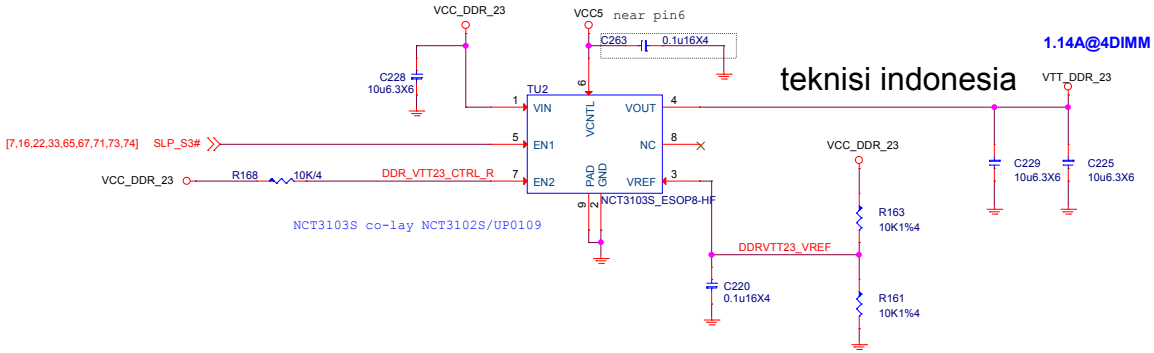


1.14A@4DIMM

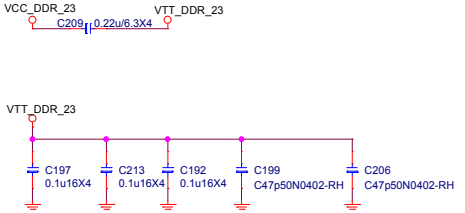


DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



1.14A@4DIMM



MICRO-STAR INT'L CO.,LTD		
MA-7A94..		
Size: Custom	Document Description: VTTDDR	Rev: 1.0
Date: Saturday, April 22, 2017	Sheet 71 of 85	

PCH_1VSB Power:1.0V,10A

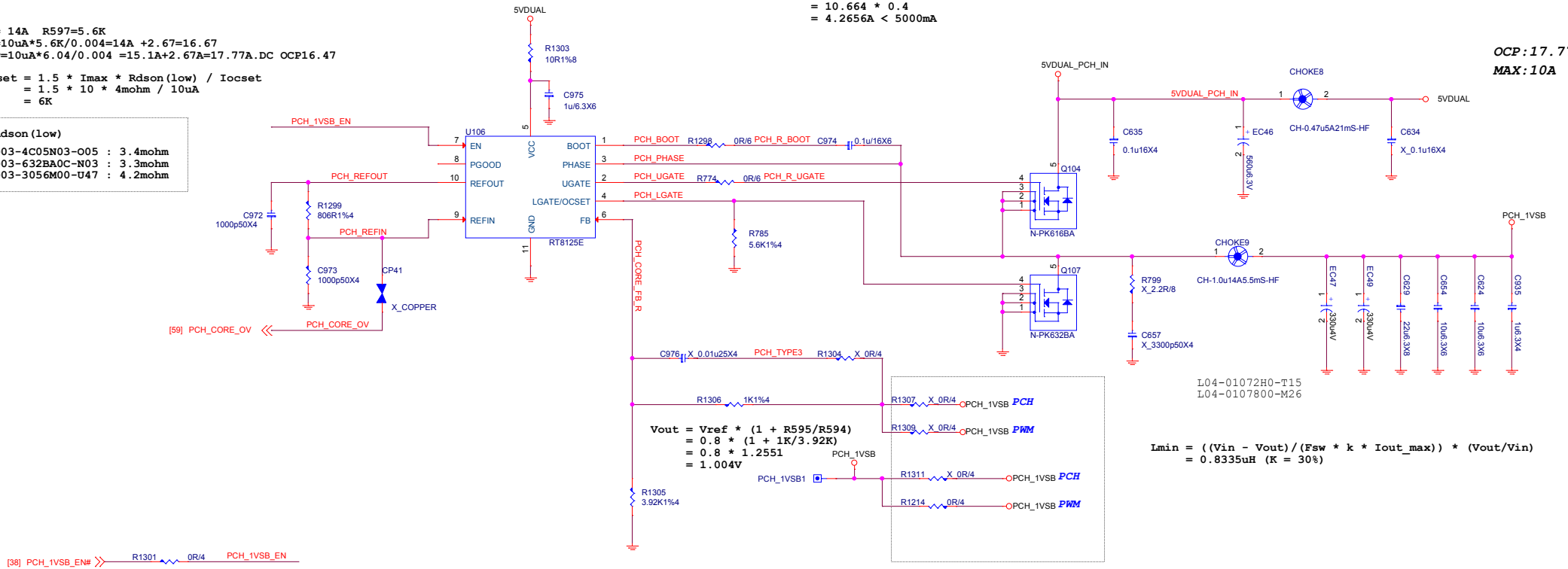
```
OCP = 14A  R597=5.6K
IOCP=10uA*5.6K/0.004=14A +2.67=16.67
*IOOP=10uA*6.04/0.004 =15.1A+2.67A=17.77A.DC OCP16.47

Rocset = 1.5 * Imax * Rdson(low) / Iocset
       = 1.5 * 10 * 4mohm / 10uA
       = 6K
```

Rdson(low)

D03-4C05N03-O05 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 10.664 * 0.4
     = 4.2656A < 5000mA
```

OCP:17.77
MAX:10A

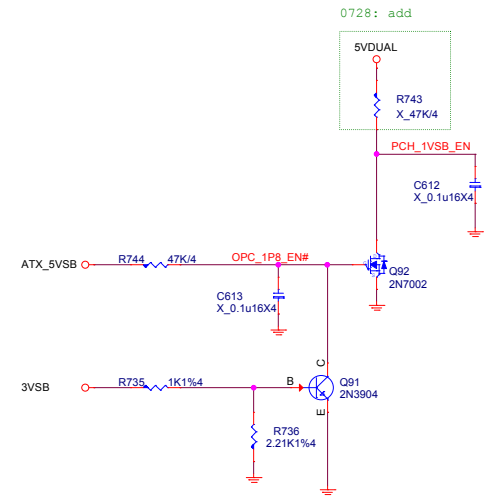



```
Vout = Vref * (1 + R595/R594)
     = 0.8 * (1 + 1K/3.92K)
     = 0.8 * 1.2551
     = 1.004V
```

L04-01072H0-T15
L04-0107800-M26

```
Lmin = ((Vin - Vout)/(Fsw * k * Iout_max)) * (Vout/Vin)
     = 0.8335uH (K = 30%)
```

[38] PCH_1VSB_EN# — R1301 0R/4 — PCH_1VSB_EN



MICRO-STAR INT'L CO.,LTD		
MA-7A94..		
Size: Custom	Document Description: PCH POWER-RT8125E	Rev: 1.0
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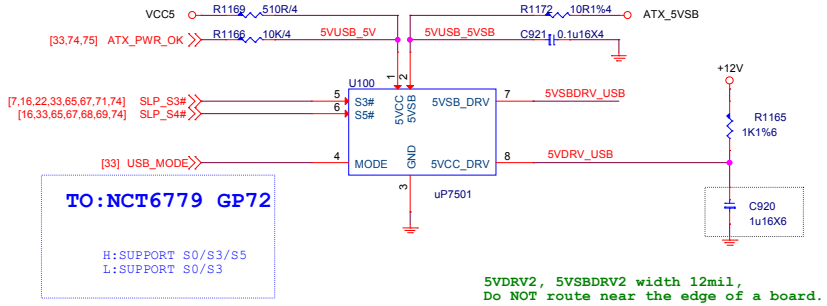
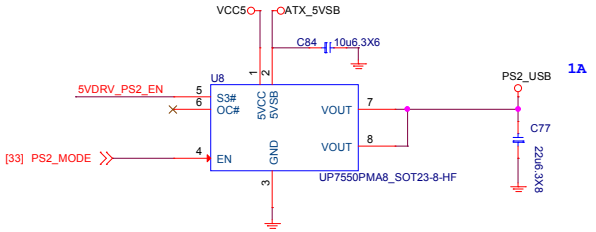
USB POWER

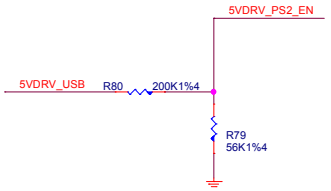


5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

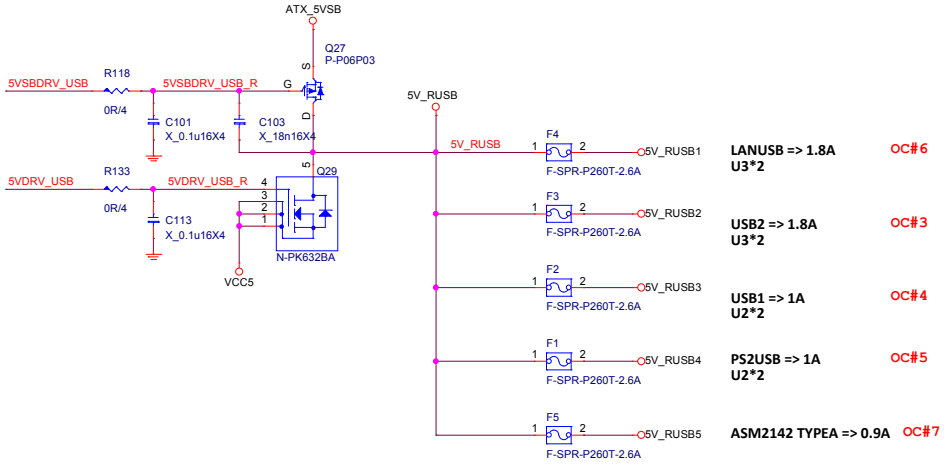
PS2 POWER



USB MODE

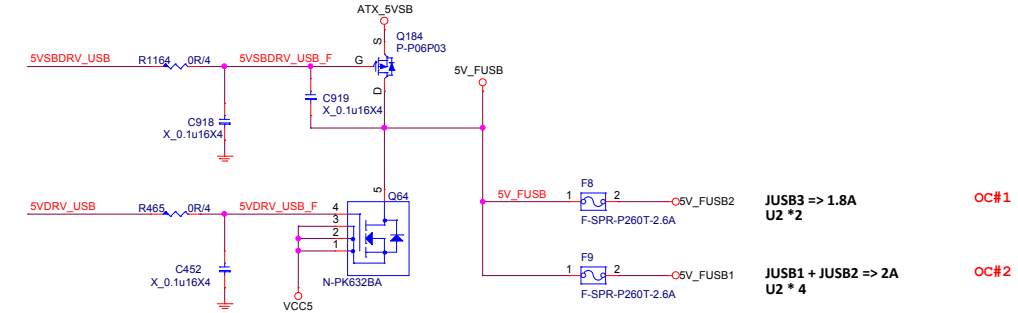


REAR USB PORT POWER



LANUSB => 1.8A U3*2	OC#6
USB2 => 1.8A U3*2	OC#3
USB1 => 1A U2*2	OC#4
PS2USB => 1A U2*2	OC#5
ASM2142 TYPEA => 0.9A	OC#7

FRONT USB PORT POWER



JUSB3 => 1.8A U2 *2	OC#1
JUSB1 + JUSB2 => 2A U2 * 4	OC#2

MICRO-STAR INT'L CO.,LTD		
MA-7A94..		
Size: Custom	Document Description: USB Power	Rev: 1.0
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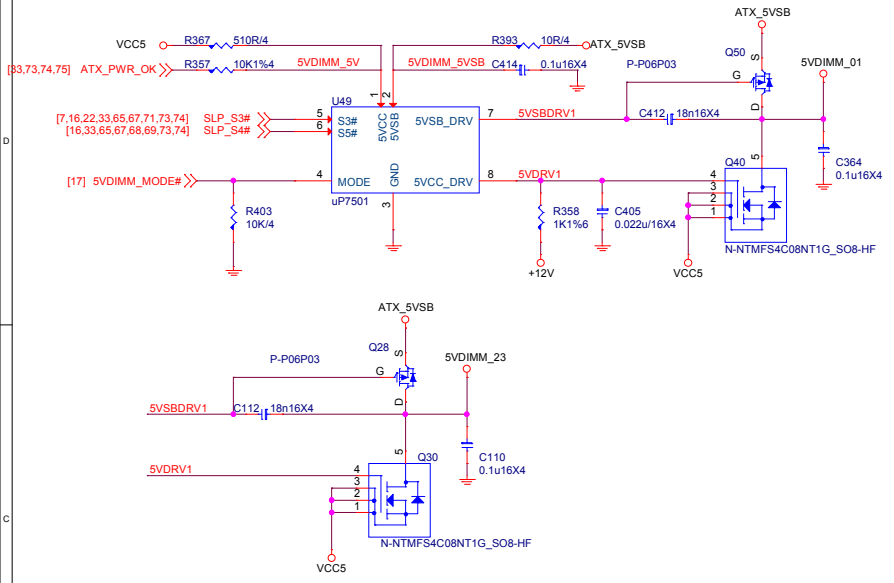
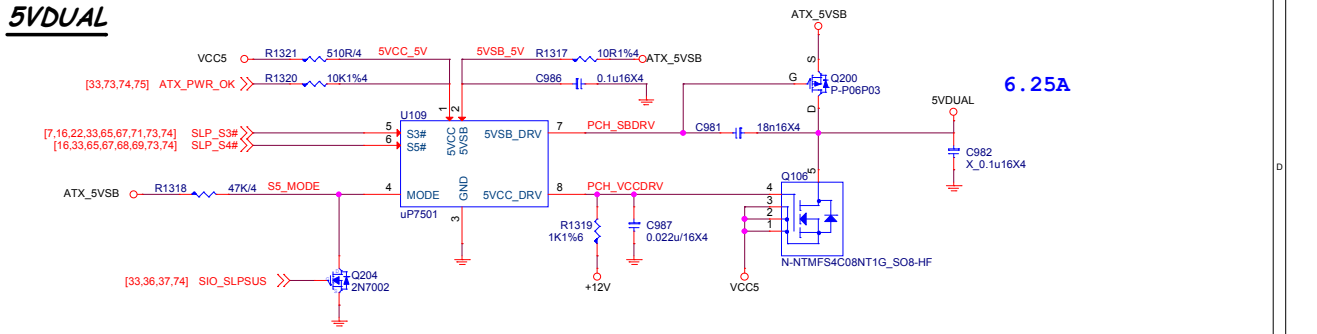
5VDIMM FOR DDR

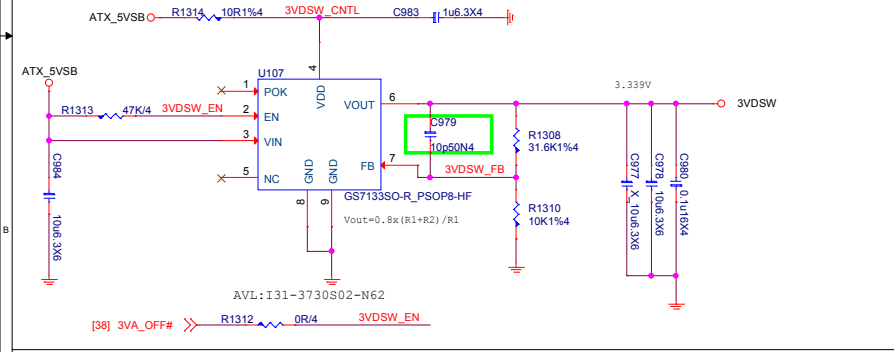


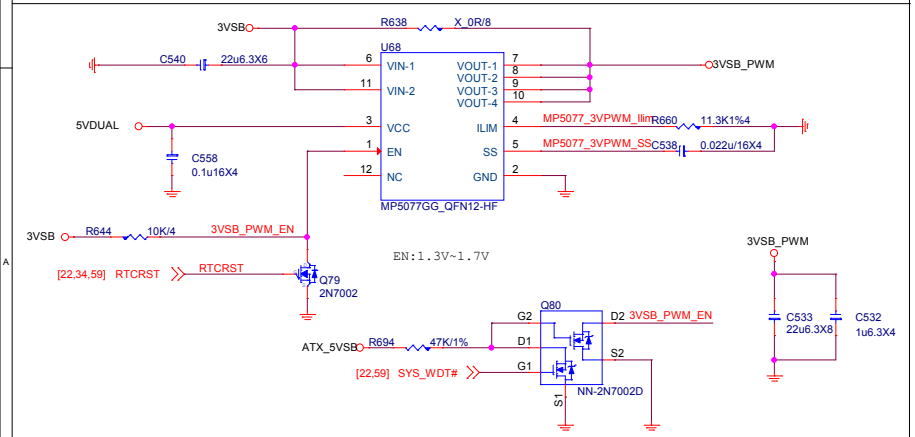
5VDUAL



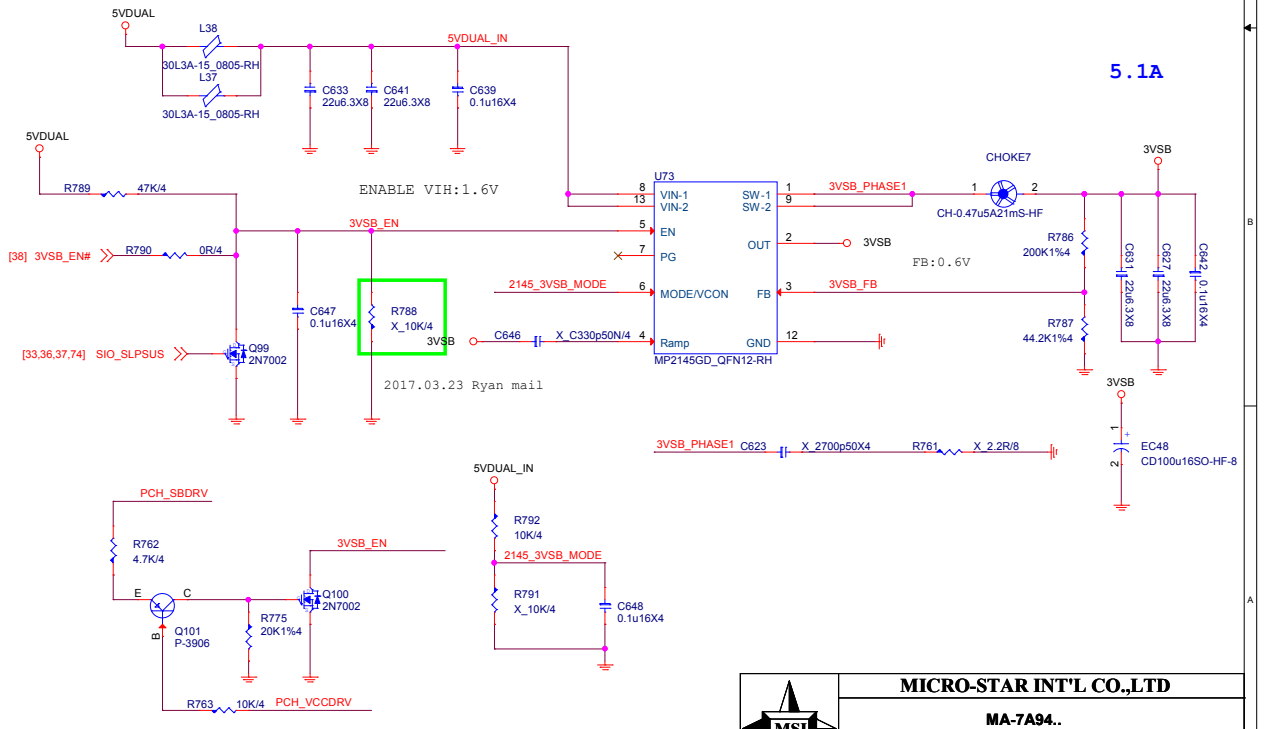
3VDSW

PCH 0.2A+I219 0.15=0.35A





3VSB for OC & Gaming



防G3-->S5底下5VSBDRV2瞬間有電變沒電,使得下一級電壓爬升有drop

MICRO-STAR INT'L CO.,LTD		
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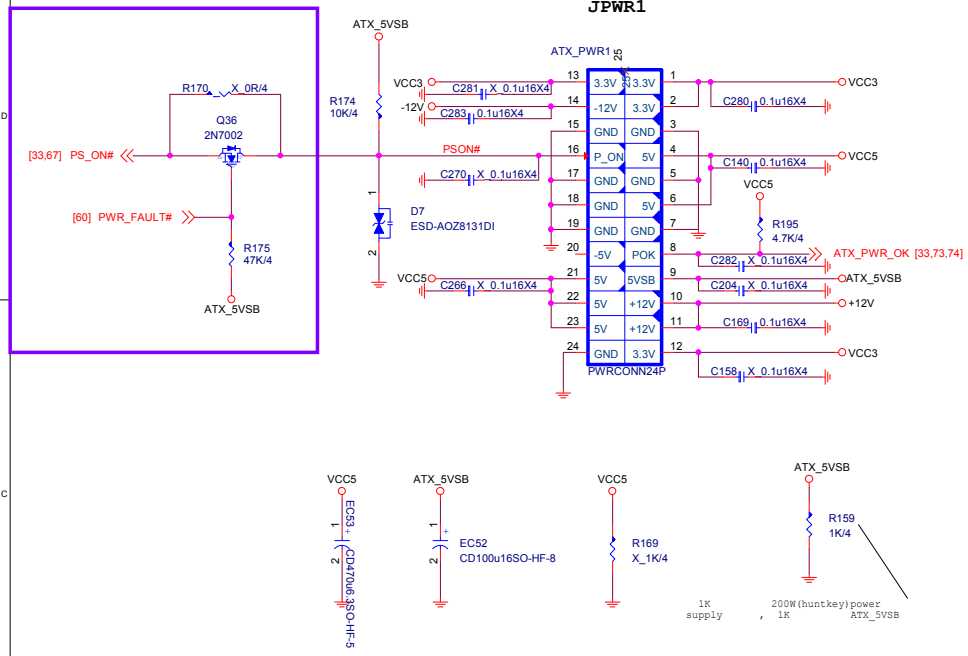
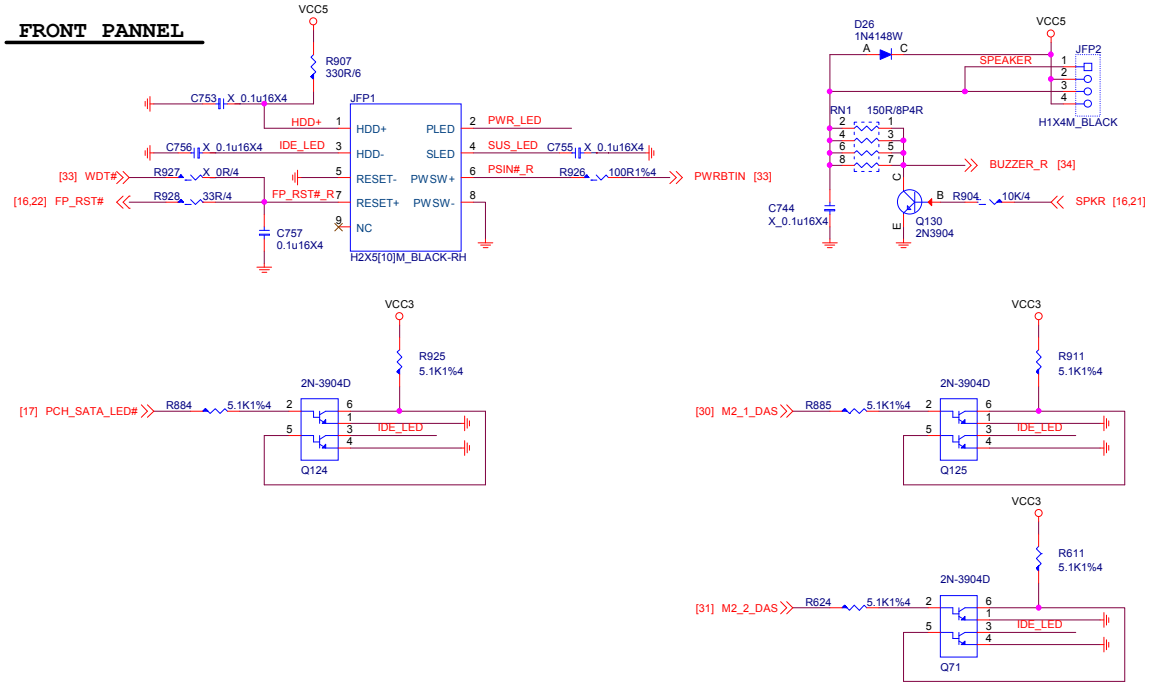
ATX POWER CONNECTOR



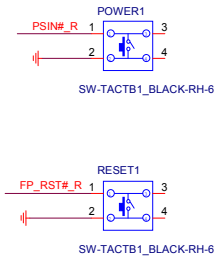
FRONT PANNEL



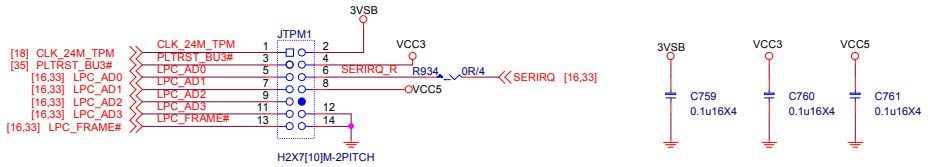
2017.03.27 Ryan mail remove JLN1

Vinafix.com

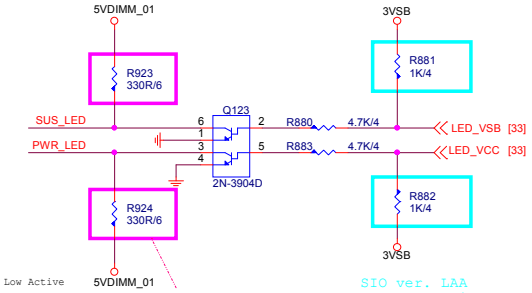
PWR/RST Botton



TPM Pin Header



Front Panel LED



MICRO-STAR INT'L CO.,LTD		
MA-7A94..		
Size: Custom	Document Description: ATX Connector/F_Panel	Rev: 1.0
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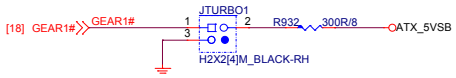
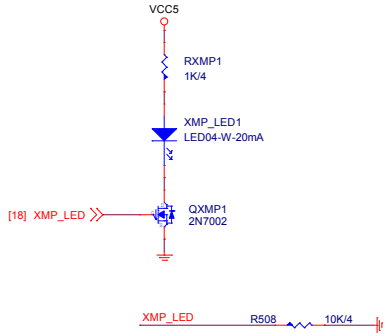
JTURBO

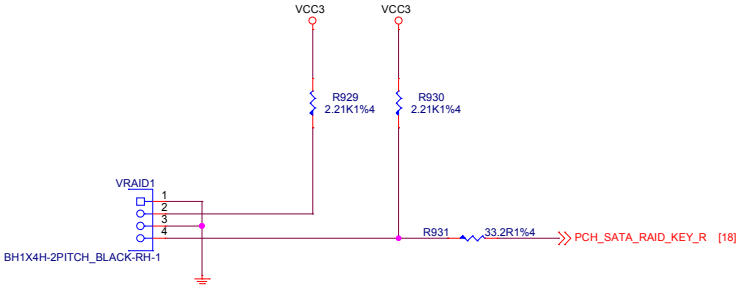


XMP LED

XMP LED >> (default) :DOC-040T200-H91



VROC



MSI	MICRO-STAR INT'L CO.,LTD	
	MA-7A94..	
Size: Custom	Document Description: Turbo/XMP LED/VROC	Rev: 1.0
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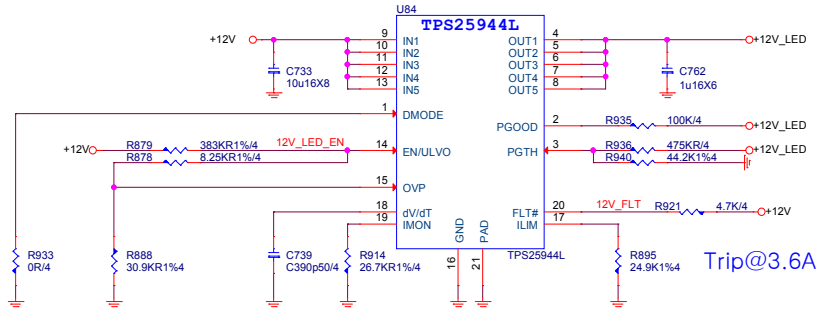
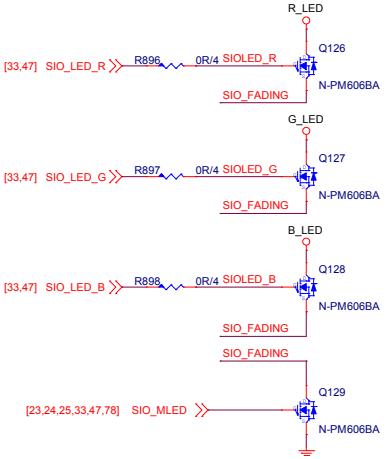
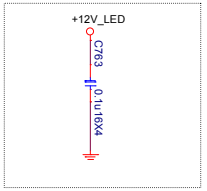
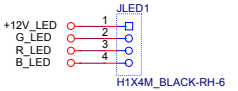
LED STRIPLINE



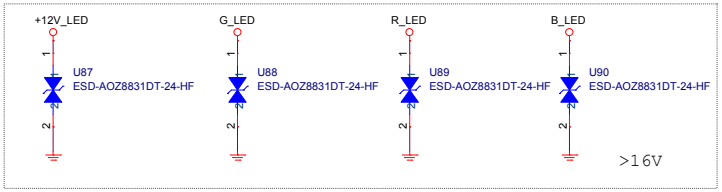


2016.08.02 Add +12V_LED 0.1uF



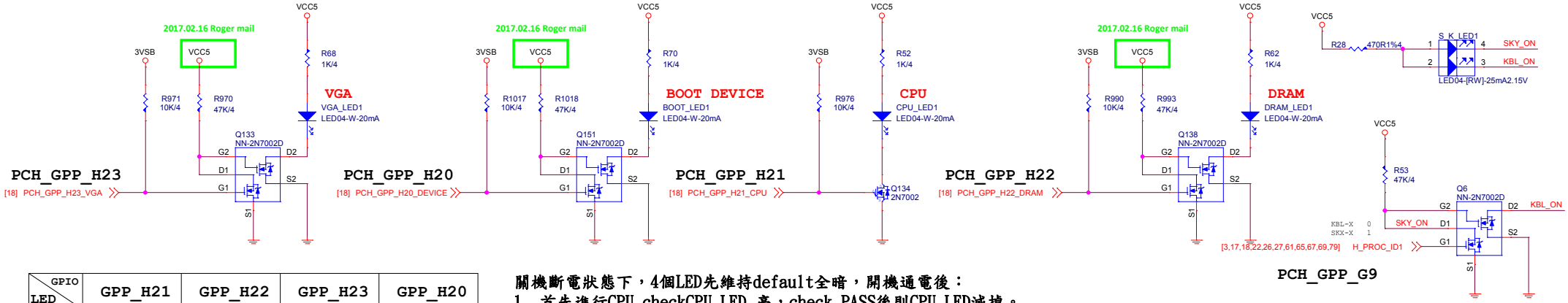


2016.07.06 only reserve now
2016.08.02 stuff ESD



EZ Debug

LED
白 : D0C-040T200-H91
AVL: D0C-040S200-E07



GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

關機斷電狀態下，4個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. BOOT DEVICE的check/BOOT LED亮，check PASS後則BOOT LED滅掉。
5. 因此最後正常順利開機後，四個LED燈都是滅掉的。
（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

MICRO-STAR INT'L CO.,LTD
MA-7A94..
Size: Custom
Document Description: LED STRIP/EZ Debug
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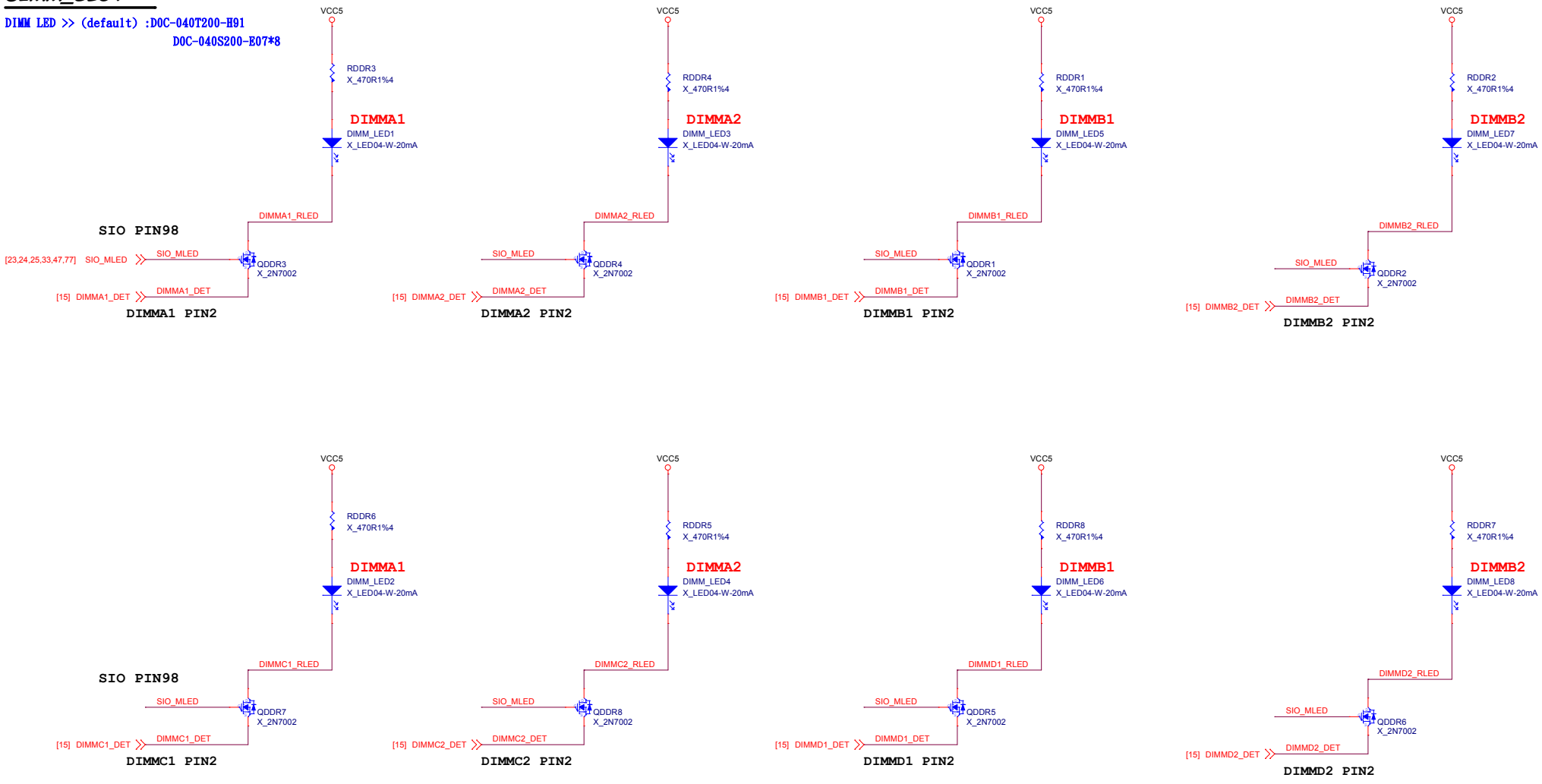
DIMM_SLOT

DIMM LED >> (default) :D0C-040T200-H91
D0C-040S200-E07*8



MSI	MICRO-STAR INT'L CO.,LTD	
	MA-7A94..	
Size: Custom	Document Description: DIMM LED	Rev: 1.0
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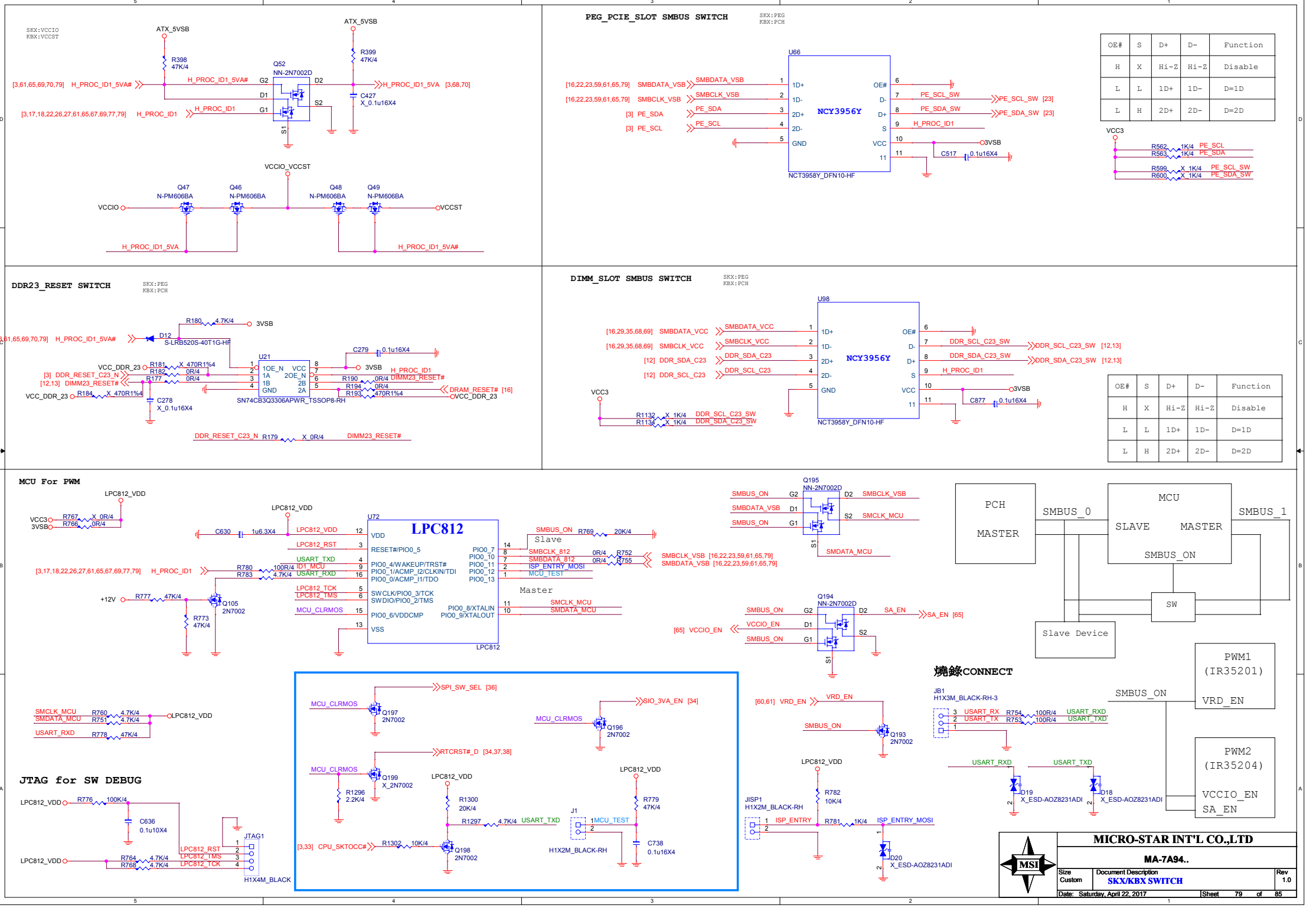
SKX:VCCIO
KBX:VCCST
ATX_5VSB
R398 47K/4
R399 47K/4
Q52 NN-2N7002D
H_PROC_ID1_5VA#
H_PROC_ID1_5VA
H_PROC_ID1
C427 X_0.1u16X4
VCCIO_VCCST
Q47 N-PM606BA
Q46 N-PM606BA
Q48 N-PM606BA
Q49 N-PM606BA
VCCIO
VCCST
PEG_PCIE_SLOT SMBUS SWITCH
SKX:PEG
KBX:PCH
U66
NCY3956Y
NCT3958Y_DFN10-HF
SMBDATA_VSB
SMBCLK_VSB
PE_SDA
PE_SCL
PE_SCL_SW
PE_SDA_SW
3VSB
C517 0.1u16X4
OE# S D+ D- Function
H X Hi-Z Hi-Z Disable
L L 1D+ 1D- D=1D
L H 2D+ 2D- D=2D
R562 1K/4 PE_SCL
R563 1K/4 PE_SDA
R599 X_1K/4 PE_SCL_SW
R600 X_1K/4 PE_SDA_SW
DDR23_RESET SWITCH
SKX:PEG
KBX:PCH
R180 4.7K/4
D12 S-LRB520S-40T1G-HF
U21
SN74CB3Q3306APWR_TSSOP8-RH
R181 X_470R1%4
R182 0R/4
R177 0R/4
R184 X_470R1%4
C278 X_0.1u16X4
C279 0.1u16X4
R190 0R/4
R194 0R/4
R193 470R1%4
DDR_RESET_C23_N
DIMM23_RESET#
DRAM_RESET# [16]
VCC_DDR_23
R179 X_0R/4
DIMM_SLOT SMBUS SWITCH
SKX:PEG
KBX:PCH
U98
NCY3956Y
NCT3958Y_DFN10-HF
SMBDATA_VCC
SMBCLK_VCC
DDR_SDA_C23
DDR_SCL_C23
DDR_SCL_C23_SW
DDR_SDA_C23_SW
C877 0.1u16X4
R1132 X_1K/4
R1134 X_1K/4
OE# S D+ D- Function
H X Hi-Z Hi-Z Disable
L L 1D+ 1D- D=1D
L H 2D+ 2D- D=2D
MCU For PWM
LPC812_VDD
VCC3
3VSB
R767 X_0R/4
R766 0R/4
C630 1u6.3X4
U72
LPC812
VDD
RESET#/PIO0_5
PIO0_4/WAKEUP/TRST#
PIO0_1/ACMP_I2/CLKIN/TDI
PIO0_0/ACMP_I1/TDO
SWCLK/PIO0_3/TCK
SWDIO/PIO0_2/TMS
PIO0_6/VDDCMP
VSS
PIO0_7
PIO0_10
PIO0_11
PIO0_12
PIO0_13
PIO0_8/XTALIN
PIO0_9/XTALOUT
LPC812_RST
USART_TXD
USART_RXD
LPC812_TCK
LPC812_TMS
MCU_CLRMOS
ID1_MCU
MCU_TEST
ISP_ENTRY_MOSI
SMBCLK_812
SMBDATA_812
SMBUS_ON
Slave
Master
SMBCLK_MCU
SMBDATA_MCU
R769 20K/4
R752 0R/4
R755 0R/4
R780 100R/4
R783 4.7K/4
R777 47K/4
R773 47K/4
Q105 2N7002
+12V
Q195 NN-2N7002D
Q194 NN-2N7002D
SMBUS_ON
SMBDATA_VSB
SMBCLK_VSB
SMBCLK_MCU
SMDATA_MCU
SA_EN
VCCIO_EN
PCH
MASTER
SMBUS_0
MCU
SLAVE
MASTER
SMBUS_ON
SMBUS_1
SW
Slave Device
PWM1 (IR35201)
VRD_EN
PWM2 (IR35204)
VCCIO_EN
SA_EN
燒錄CONNECT
JB1
H1X3M_BLACK-RH-3
USART_RX
USART_TX
R754 100R/4
R753 100R/4
D19 X_ESD-AOZ8231ADI
D18 X_ESD-AOZ8231ADI
D20 X_ESD-AOZ8231ADI
JISP1
H1X2M_BLACK-RH
ISP_ENTRY
R782 10K/4
R781 1K/4
SMCLK_MCU R760 4.7K/4
SMDATA_MCU R751 4.7K/4
USART_RXD R778 47K/4
JTAG for SW DEBUG
R776 100K/4
C636 0.1u10X4
R764 4.7K/4
R768 4.7K/4
JTAG1
H1X4M_BLACK
SPI_SW_SEL [36]
SIO_3VA_EN [34]
RTCRST#_D [34,37,38]
Q197 2N7002
Q196 2N7002
Q199 X_2N7002
Q198 2N7002
R1296 2.2K/4
R1300 20K/4
R1297 4.7K/4
R1302 10K/4
CPU_SKTOCC# [3,33]
J1
MCU_TEST
H1X2M_BLACK-RH
R779 47K/4
C738 0.1u16X4
MICRO-STAR INT'L CO.,LTD
MA-7A94..
Size Custom
Document Description SKX/KBX SWITCH
Rev 1.0
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HEATSINK

CPU_H1

CPU
鐵座

CPU_ILM1

2017.04.10 PM Change

PCB1

7A94_10

PD0-07A9410-G37

PD0-07A9410-E48

Mounting Holes

MH2 MH3 MH1

MH4 MH5 MH6

MH7 MH8 MH9

X_MH001

C749 0.1u16X4

C727 0.1u16X4

Simulation

SIM1 SIM2 SIM4 SIM3

X_PIN1*2

Optical Fiducial Marks-120

FM1 FM6 FM2 FM5

FM3 FM8 FM4 FM7

X_FM

Test point

VCORE	CPU
VSA	VCCSA
VCCIO	VCCIO
3VSB	3VSB
VBAT	VBAT
5VDUAL	5VDUAL
VCCSFR_OC	VCCSFR_OC
VCCST	VCCST
VCCSFR	VCC_SFR

VCC_DDR_01	VCC_DDR_01
VCC_DDR_23	VCC_DDR_23
VTT_DDR_23	VTT_DDR_23
VTT_DDR_01	VTT_DDR_01
5VDIMM_01	5VDIMM_01
5VDIMM_23	5VDIMM_23
+VPP25_C23	VPP25_C23
+VPP25_C01	VPP25_C01

2017.02.20 Ryan mail

VIRTUAL1

Label

VIRTUAL

BAT1_X1

BAT-BCR2032P-RH

COVER1

CHOKE Cover

X1 X2

CK_COVER

BIOS_LA1

AMI_BIOS LABLE

G51-M1SPXXA-A09

MOS_SINK1

MOS_HEATSINK

MOS_SINK1

MKT_LA1

MKT LABLE

G51-M1SPL38-Q13

LABLE5

SLI LABLE

Y01-RNVIDIM-000

PCH_SINK1

PCH_HEATSINK

PCH_SINK1

MKT_LA2

MKT LABLE

G51-M1SPL39-Q13

MICRO-STAR INT'L CO.,LTD

MA-7A94..

Size	Document Description	Rev
Custom	Manual Parts	1.0

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