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G Project M/B Schematics Document

AMD FP4 Bristol Ridge SOC with DDRVI

AMD R17M-M1-70

2016-11-09

REV:0.1

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Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: Cover Page

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 1 of 50

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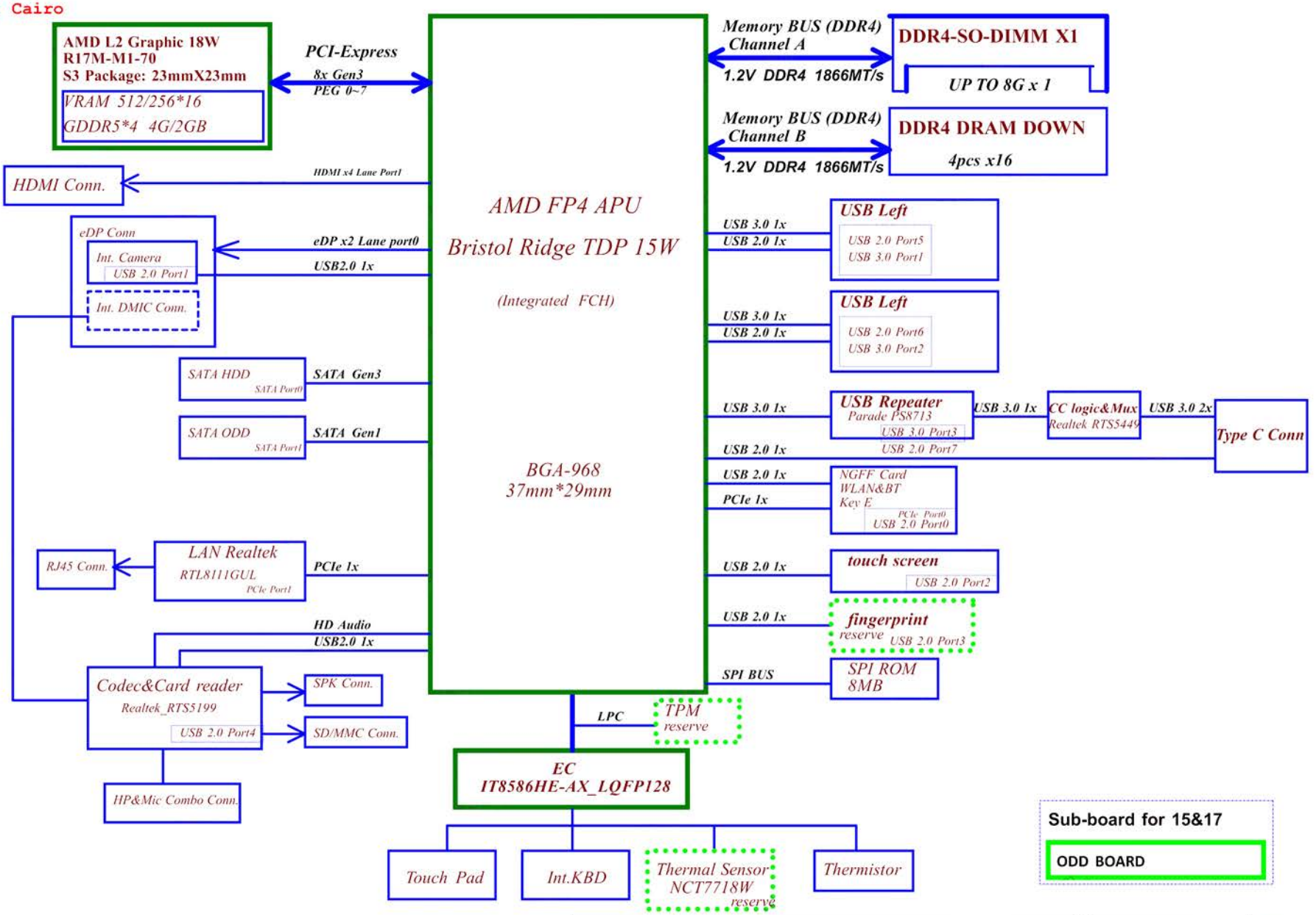
File Name : Cairo



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Title: Block Diagram

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 2 of 50

Voltage Rails (O --> Means ON , X --> Means OFF)

State \ power plane	B+ (+20VSB) +3VL +5VLP	+5VALW +3VALW (+3VALW_APU) +1.8VALW +0.95VALW +0.775VALW	+1.2V (+VSYSMEM_APU)	+5VS +3VS +1.8VS +1.5VS +0.95VS +0.6VS +2.5VS +APU_CORE +APU_CORE_NB +APU_GFX +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

DRAM Config.	BOARD_ID0 APIO8	BOARD_ID1 AGPIO10	BOARD_ID2 AGPIO16 internal pull up 40K
	0: 14''	0: Dis	0: No KBL
	1: 15''	1: UMA	0: KBL

USB Port Table

USB 2.0	USB 3.0	Port	Port device
EHCI0		0	Blue Tooth
		1	Camera
		2	Touch screen
		3	Finger print
xHCI	0	4	Card Reader USB 2.0 bus
	1	5	LEFT USB (3.0) 1#
	2	6	LEFT USB (3.0) 2#
	3	7	Type C

PCIE PORT LIST

	Port	Device
GPP	0	N/A
	1	WLAN
	2	LAN
	3	N/A
GFX	0	GPU
	1	
	2	
	3	
	4	
	5	
	6	
	7	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
ME@	Connector
14@	For 14" part
15@	For 15" part
EMC@	EMC Part
EMC_NS@	EMC reserve Part
EMC_14@	EMC 14 part
EMC_15@	EMC 15 part
RF@	RF Part
RF_PXNS@	RF GPU reserve part
UMA@	UMA SKU ID part
PX@	Discrete GPU SKU part
EXO@	EXO GPU Part
TOPAZ@	TOPAZ GPU Part
TPM@	TPM part
KBL@	keyboard backlight part
HDT@	HDT Debug part
BR@	Bristol Ridge Part
ST@	Stoney Ridge part
BRPX@	Bristol Ridge Discrete Part
S4GX4@	X76 SAMSUNG 2G
M4GX4@	X76 MICRON 2G
H4GX4@	X76 HYNIX 2G
S2G@	SAMSUNG 2G
M2G@	MICRON 2G
H2G@	HYNIX 2G
HDMI@	HDMI Logo

VRAM

SMBUS Control Table

	SOURCE	GPU	BATT	IT8586	SODIMM	WLAN	Thermal Sensor	APU	Charger	PMIC
EC_SMB_CK1 EC_SMB_DA1	IT8586 +3VL	X	V		X	X	X	X	V	X
EC_SMB_CK2 EC_SMB_DA2	IT8586 +3VL	X	X		X	X	X	X	X	V
EC_SMB_CK3 EC_SMB_DA3	IT8586 +3VS	V +3VS_VGA	X		X	X	V	V 1.8VS	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V	V	X		X	X

I2C Control Table

	SOURCE	Device
TP_I2C0_SCL TP_I2C0_SDA	APU +1.8VS	Touch Pad 3VS

APU I2C address

Device	Address
Elan: SA469 D 22 HA 69x104x1 0	?
Synaptics: T M P3255-008 69x104x1 0	?

EC SM Bus1 address

Device	Address
Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

Device	Address
PMIC	?

EC SM Bus3 address

Device	Address
Thermal Sensor	1001_100xb(reserve)
GPU	0x41(default)
APU SB-TSI	releate to F3x1E4[SbiAddr] or Address Select Pins setting

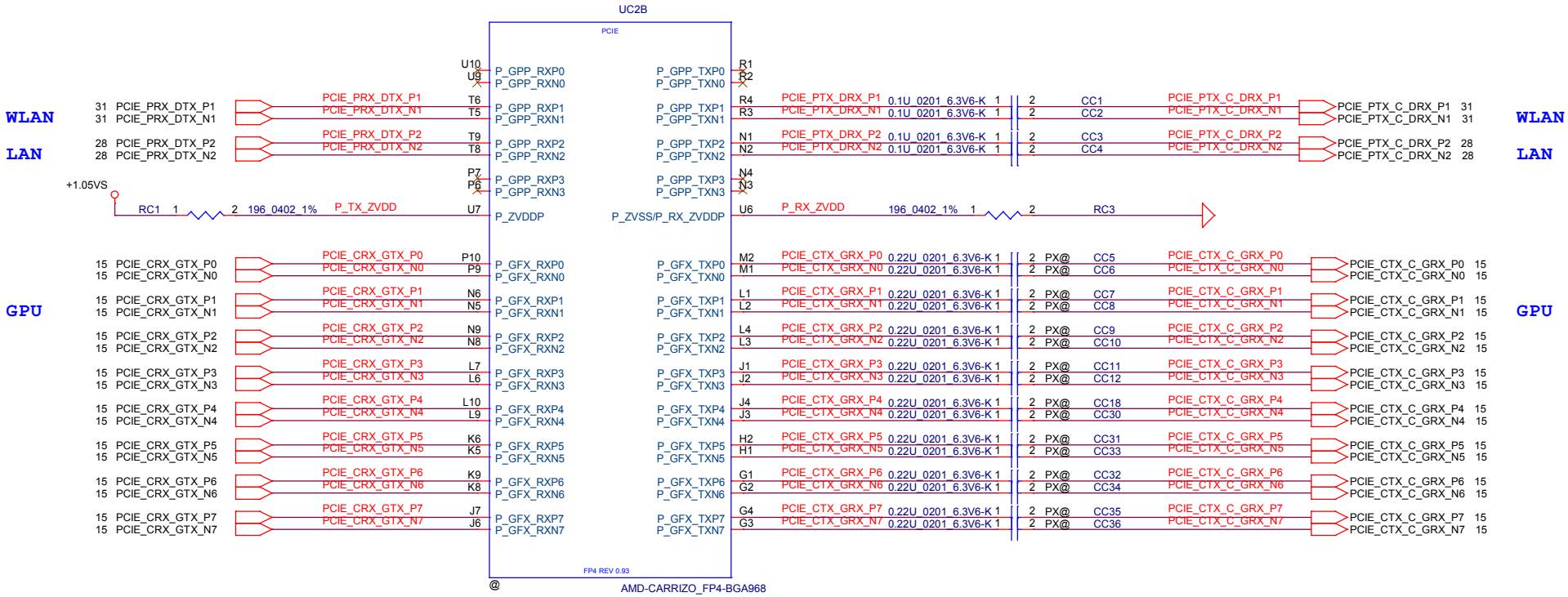
APU SM Bus address

Device	Address
DDR4 SO-DIMM	?
WLAN	RSVD

Title: Notes List

Size: Custom | Document Number: 320ABR | Rev: 0.1

Date: Thursday, January 12, 2017 | Sheet 3 of 50



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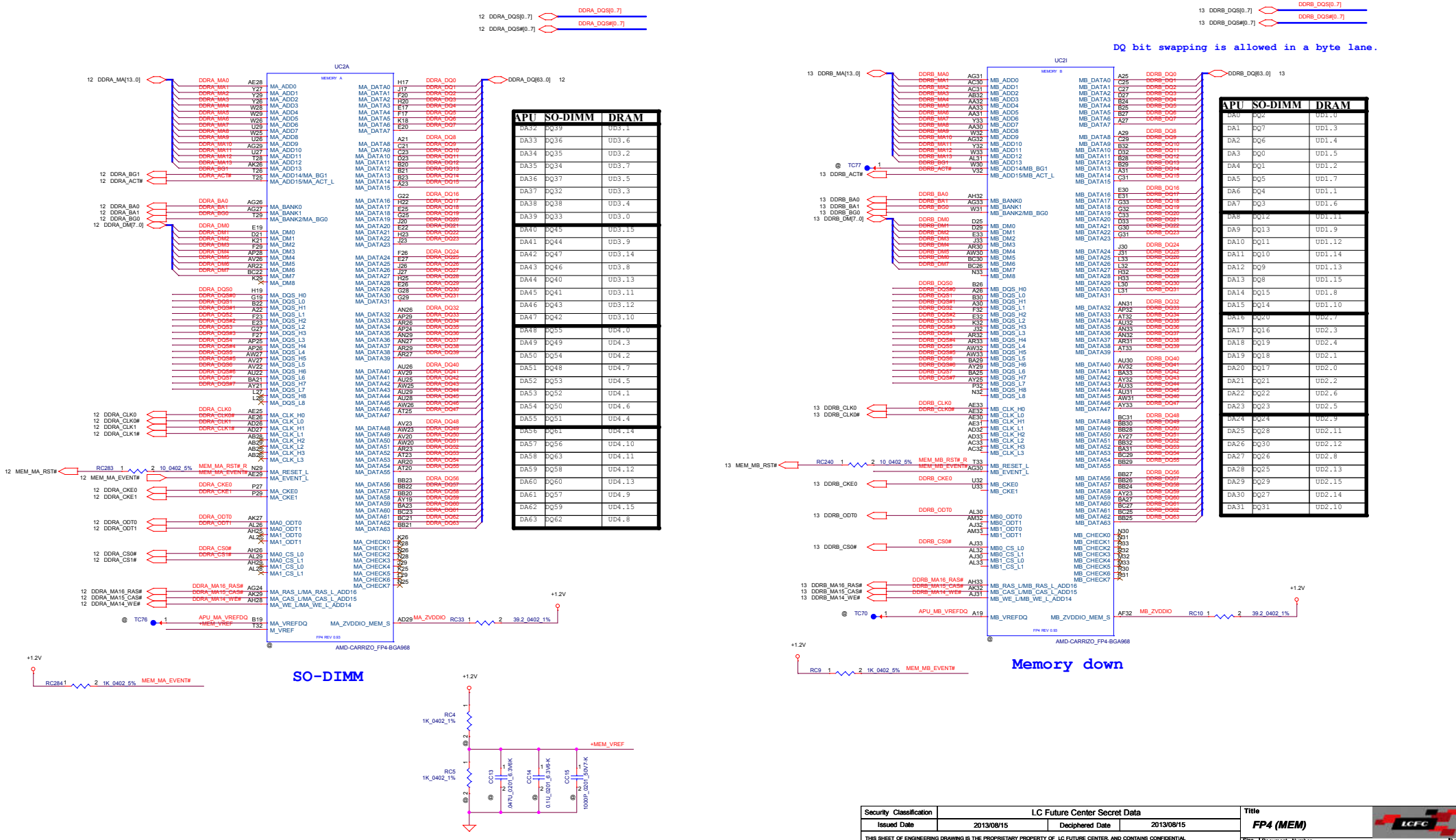
Title: **FP4 (PCIE I/F)**

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 4 of 50


DQ bit swapping is allowed in a byte lane.
SO-DIMM
Memory down
UC2A
UC2I
AMD-CARRIZO_FP4-BGA968
APU | SO-DIMM | DRAM
DA0 DQ39 UD3.1
DA1 DQ35 UD3.2
DA2 DQ34 UD3.7
DA3 DQ32 UD3.3
DA4 DQ38 UD3.4
DA5 DQ41 UD3.11
DA6 DQ43 UD3.12
DA7 DQ42 UD3.10
DA8 DQ55 UD4.0
DA9 DQ49 UD4.3
DA10 DQ54 UD4.2
DA11 DQ48 UD4.7
DA12 DQ53 UD4.5
DA13 DQ52 UD4.1
DA14 DQ50 UD4.6
DA15 DQ51 UD4.4
DA16 DQ61 UD4.14
DA17 DQ56 UD4.10
DA18 DQ63 UD4.11
DA19 DQ58 UD4.12
DA20 DQ59 UD4.15
DA21 DQ62 UD4.8
APU | SO-DIMM | DRAM
DA0 DQ2 UD1.0
DA1 DQ7 UD1.3
DA2 DQ6 UD1.4
DA3 DQ0 UD1.5
DA4 DQ1 UD1.2
DA5 DQ5 UD1.7
DA6 DQ4 UD1.1
DA7 DQ3 UD1.6
DA8 DQ12 UD1.11
DA9 DQ13 UD1.9
DA10 DQ11 UD1.12
DA11 DQ10 UD1.14
DA12 DQ9 UD1.13
DA13 DQ8 UD1.15
DA14 DQ15 UD1.8
DA15 DQ14 UD1.10
DA16 DQ20 UD2.7
DA17 DQ16 UD2.3
DA18 DQ19 UD2.4
DA19 DQ18 UD2.1
DA20 DQ17 UD2.0
DA21 DQ21 UD2.2
DA22 DQ22 UD2.6
DA23 DQ23 UD2.5
DA24 DQ24 UD2.9
DA25 DQ28 UD2.11
DA26 DQ30 UD2.12
DA27 DQ26 UD2.8
DA28 DQ25 UD2.13
DA29 DQ29 UD2.15
DA30 DQ27 UD2.14
DA31 DQ31 UD2.10
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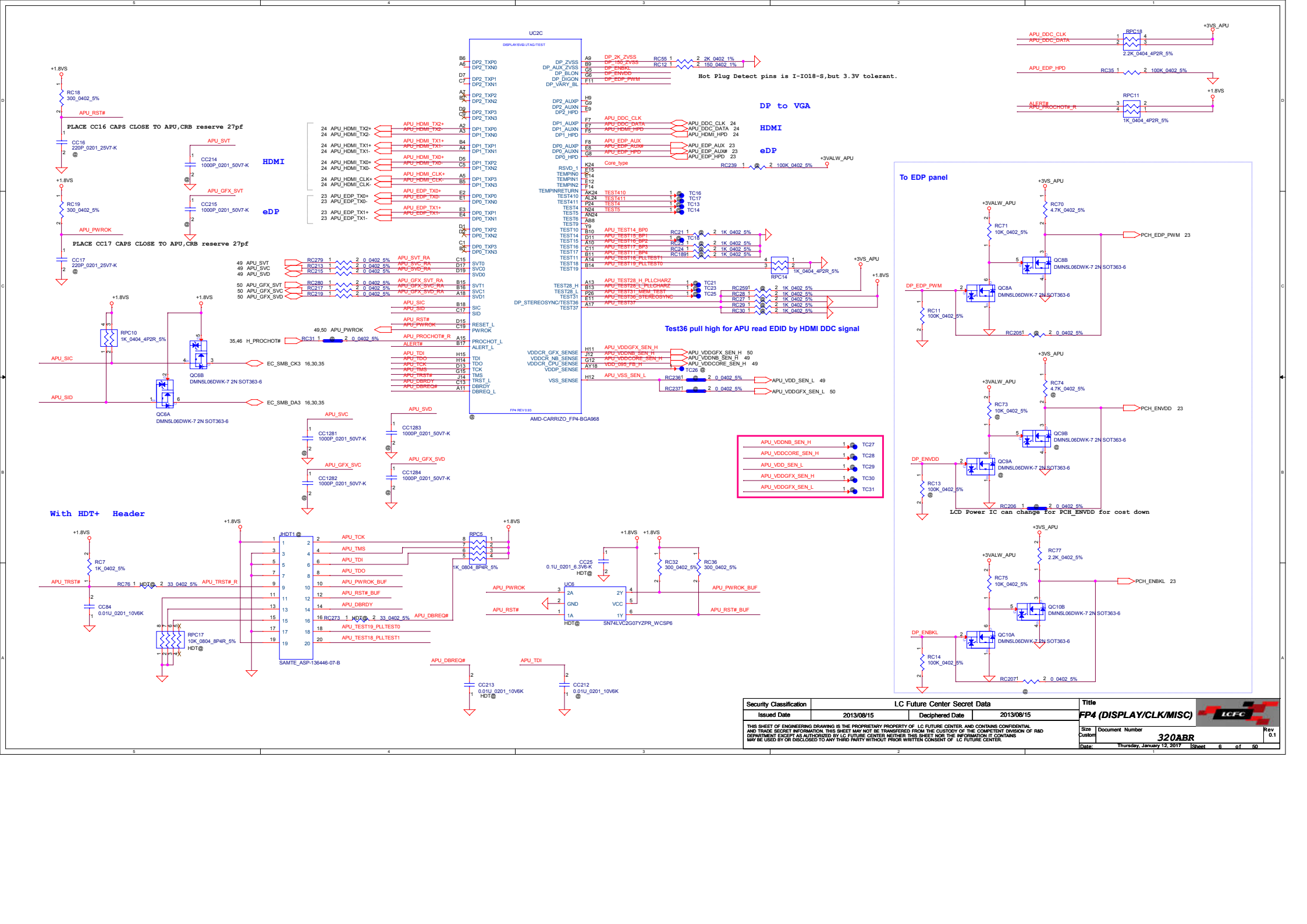
Size
Custom
Document Number
320ABR
Rev
0.1
Date:
Thursday, January 12, 2017
Sheet
5
of
50


PLACE CC16 CAPS CLOSE TO APU,CRB reserve 27pf
PLACE CC17 CAPS CLOSE TO APU,CRB reserve 27pf
HDMI
eDP
DP to VGA
HDMI
eDP
Hot Plug Detect pins is I-IO18-S,but 3.3V tolerant.
Test36 pull high for APU read EDID by HDMI DDC signal
To EDP panel
With HDT+ Header
LCD Power IC can change for PCH_ENVDD for cost down
AMD-CARRIZO_FP4-BGA968
SAMTE_ASP-136446-07-B
SN74LVC2G07YZPR_WCSP6
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Title
FP4 (DISPLAY/CLK/MISC)
Size
Custom
Document Number
320ABR
Rev
0.1
Date:
Thursday, January 12, 2017
Sheet
6
of
50

DRAM Config.	BOARD_ID3 APIO15	BOARD_ID4 AGPIOI3
Hynix	0	0
Micron	0	1
	1	0
Samsung	1	1

ID2--5 internal pull up 40K
ID6 internal pull low 40K

Connected to 10-ms RC-delay circuit on VDD_18_S5 power rail.
(CRB PWR Dealy: 22K/0.1uF)

EC set RSMRST OD output

DIMM1, DIMM2, Mini CARD

Touch pad

Max ESR < 65K ohm !!

2/22: change to 50K ohm for Crystal vendor suggest

change YC1 PN to ESPON S CRYSTAL 32.768KHZ X1A000141000300, footprint no change

BLINK isn't strap pin, don't need pull high

PXS_PWREN_R/PXS_RST#_R/VR_VGA_PWRGD internal pull up 40k

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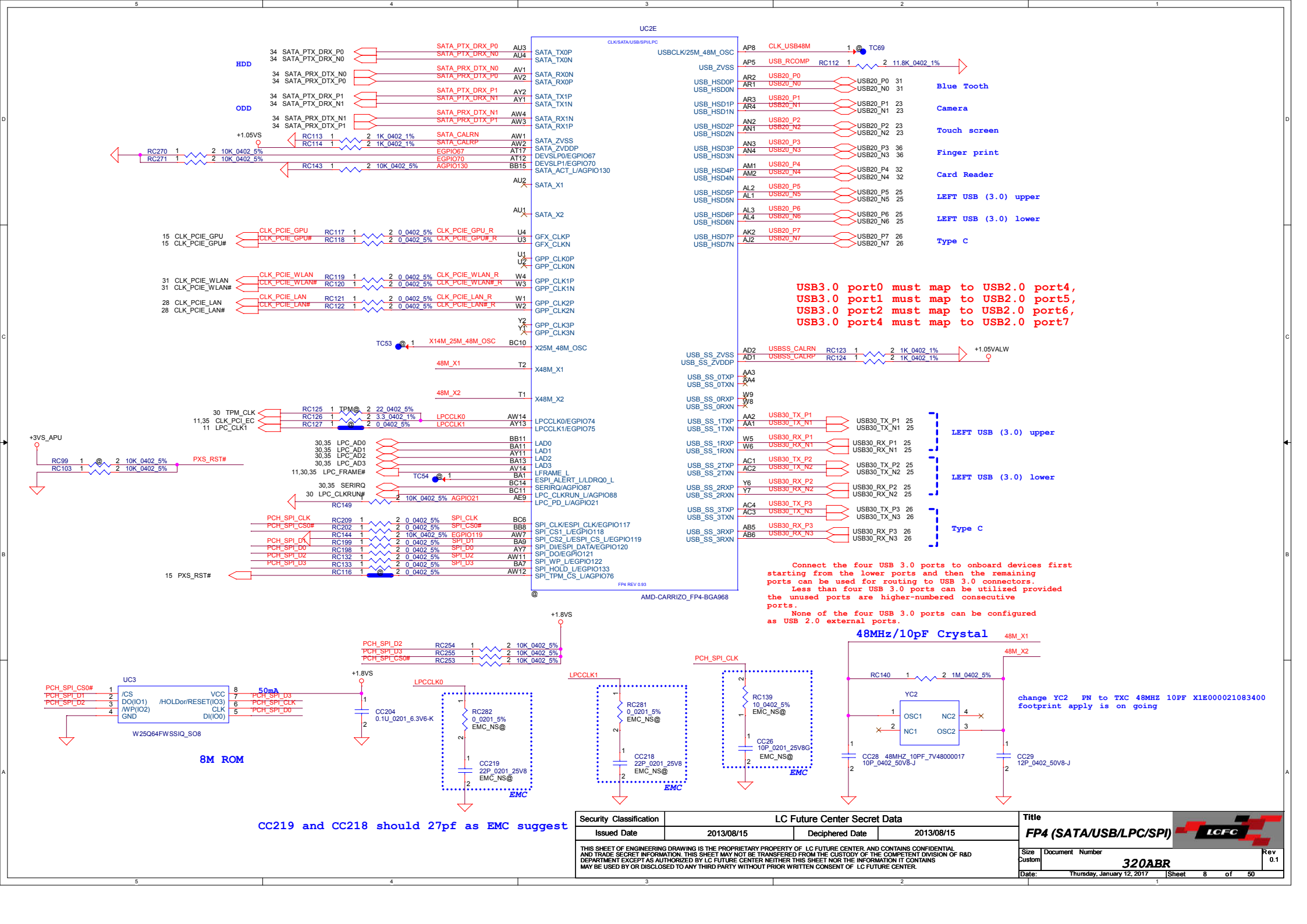
Title: FP4 (GEVENT/GPIO/SD/AZ)

Size: Custom | Document Number: 320ABR | Rev: 0.1

Date: Thursday, January 12, 2017 | Sheet 7 of 50



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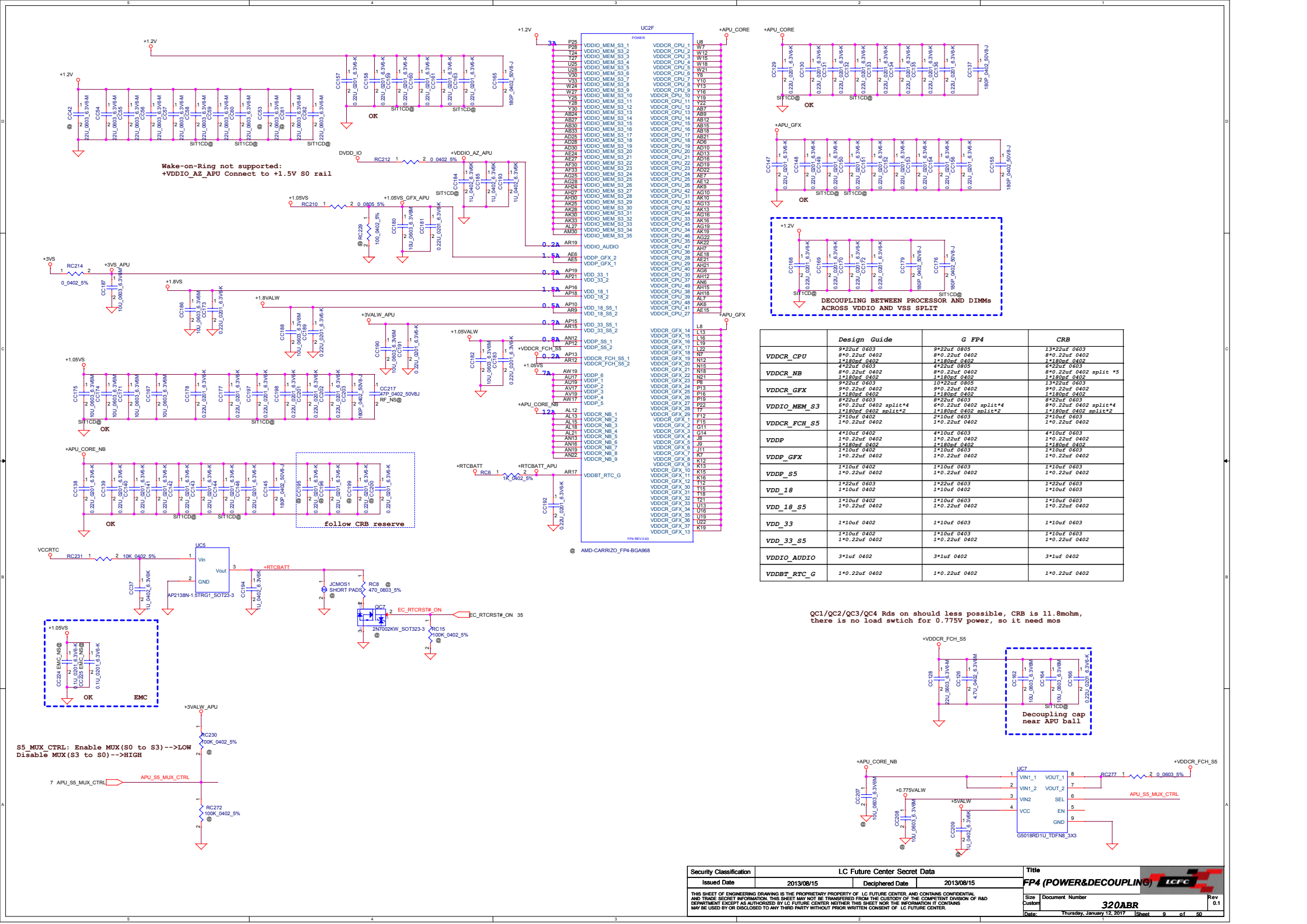
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: FP4 (SATA/USB/LPC/SPI)

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 8 of 50



	Design Guide	G FP4	CRB
VDDCR_CPU	9*22uf 0603 8*0.22uf 0402 1*180pf 0402	9*22uf 0805 8*0.22uf 0402 1*180pf 0402	13*22uf 0603 8*0.22uf 0402 1*180pf 0402
VDDCR_NB	4*22uf 0603 8*0.22uf 0402 1*180pf 0402	4*22uf 0805 8*0.22uf 0402 1*180pf 0402	6*22uf 0603 8*0.22uf 0402 split *5 1*180pf 0402
VDDCR_GFX	9*22uf 0603 9*0.22uf 0402 1*180pf 0402	10*22uf 0805 9*0.22uf 0402 1*180pf 0402	13*22uf 0603 9*0.22uf 0402 1*180pf 0402
VDDIO_MEM_S3	8*22uf 0603 6*0.22uf 0402 split*4 1*180pf 0402 split*2	8*22uf 0603 6*0.22uf 0402 split*4 1*180pf 0402 split*2	8*22uf 0603 8*0.22uf 0402 split*4 1*180pf 0402 split*2
VDDCR_FCH_S5	2*10uf 0402 1*0.22uf 0402	2*10uf 0603 1*0.22uf 0402	2*10uf 0603 1*0.22uf 0402
VDDP	4*10uf 0402 1*0.22uf 0402 1*180pf 0402	4*10uf 0603 1*0.22uf 0402 1*180pf 0402	4*10uf 0603 1*0.22uf 0402 1*180pf 0402
VDDP_GFX	1*10uf 0402 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402
VDDP_S5	1*10uf 0402 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402
VDD_18	1*22uf 0603 1*10uf 0402	1*22uf 0603 1*10uf 0402	1*22uf 0603 1*10uf 0603
VDD_18_S5	1*10uf 0402 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402
VDD_33	1*10uf 0402	1*10uf 0603	1*10uf 0603
VDD_33_S5	1*10uf 0402 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402	1*10uf 0603 1*0.22uf 0402
VDDIO_AUDIO	3*1uf 0402	3*1uf 0402	3*1uf 0402
VDDBT_RTC_G	1*0.22uf 0402	1*0.22uf 0402	1*0.22uf 0402

QC1/QC2/QC3/QC4 Rds on should less possible, CRB is 11.8mohm,
there is no load swtich for 0.775V power, so it need mos

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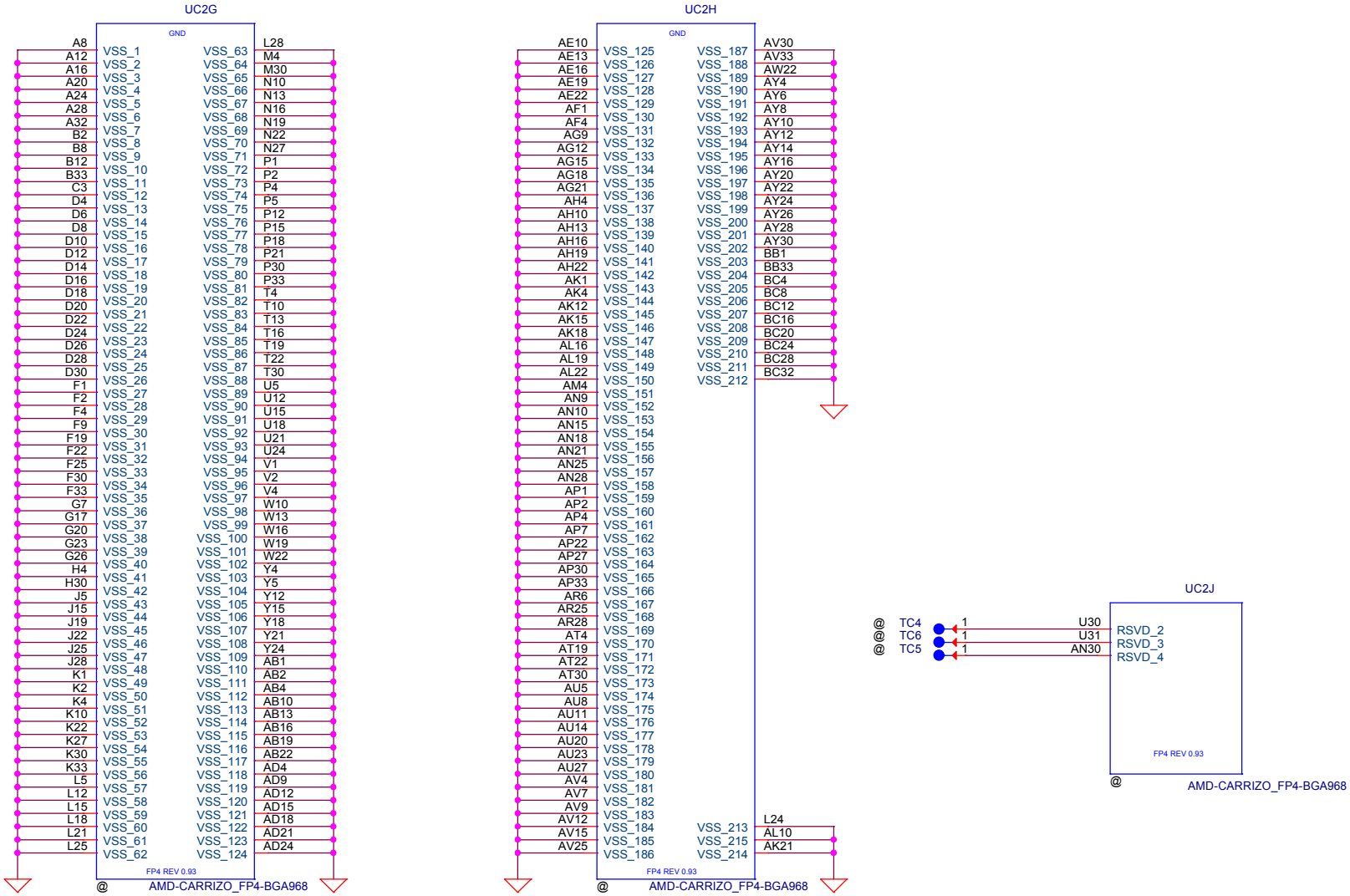
Title	FP4 (POWER&DECOUPLING)		
Size: Custom	Document Number: 320ABR		Rev: 0.1
Date: Thursday, January 12, 2017	Sheet 9 of 50		



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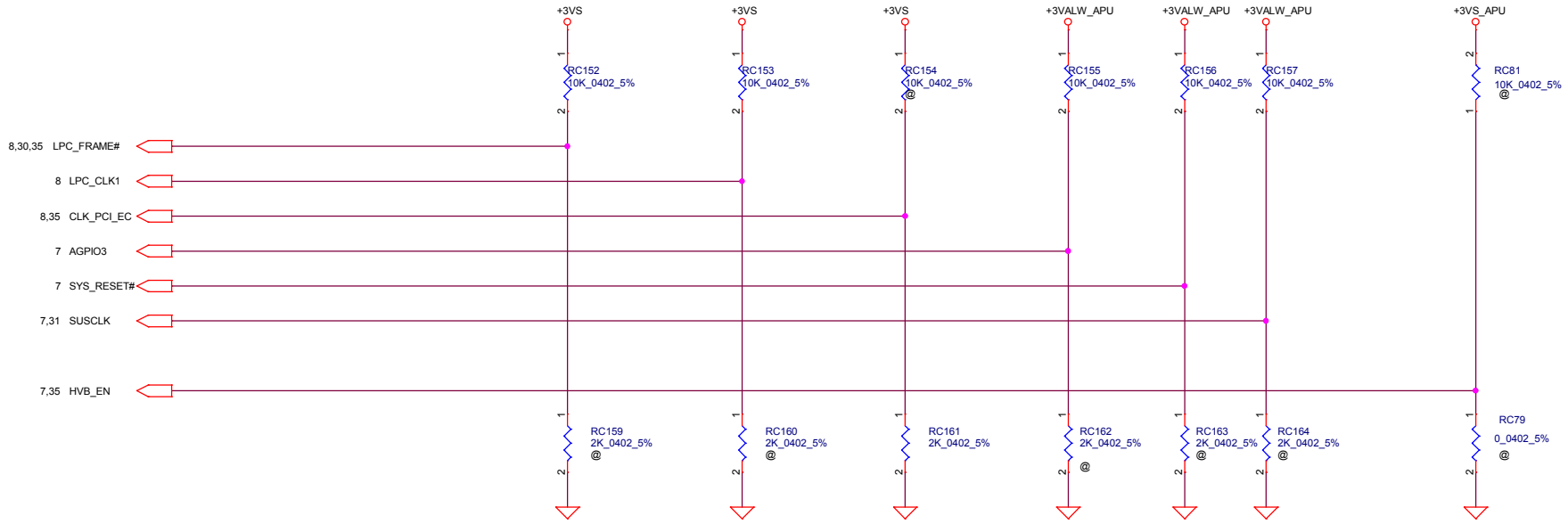
Title

FP4 (VSS)

Size: Custom	Document Number: 320ABR	Rev: 0.1
Date: Thursday, January 12, 2017	Sheet 10 of 50	



STRAP PINS

Signal	LFRAME_L	LPCCLK1	LPCCLK0	RTCCLK Int pull-up	SYS_RESET_L Int pull-up	AGPIO3 Int pull-up	HVB_EN
Type	II	II	II	I	I	I	
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	RTC Coin Battery is implemented Default	Normal Power Up &Reset Timing Default	Enhanced reset logic (for quicker S5 resume) Default	floating Disable HVB on FP4 platforms Default
PULL LOW	LPC ROM	Reserved	Boot Fail Timer Disabled Default	RTC Coin Battery is not implemented	Reserved	traditional reset logic	connected to VSS Enable HVB on FP4 platforms

Type I straps become valid immediately after capture with the rising edge of RSMRST_L,they are captured only once when power is first applied to the processor

Type II straps become valid after PWR_GOOD is asserted,straps are captured every time the systems powers up from the S5 state. A transition from S3 to S0 does not trigger capture.
Type II straps should be pulled up to S0 power rail to prevent leakage when the signal is connected to a device in S0 power domain.

If the LPC bus is connected to devices that are on S0 power rail, then a pull-up resistor to VDD_33 is implemented.

All Strap pins must be configured with either external pull-up or pull-down resistors.

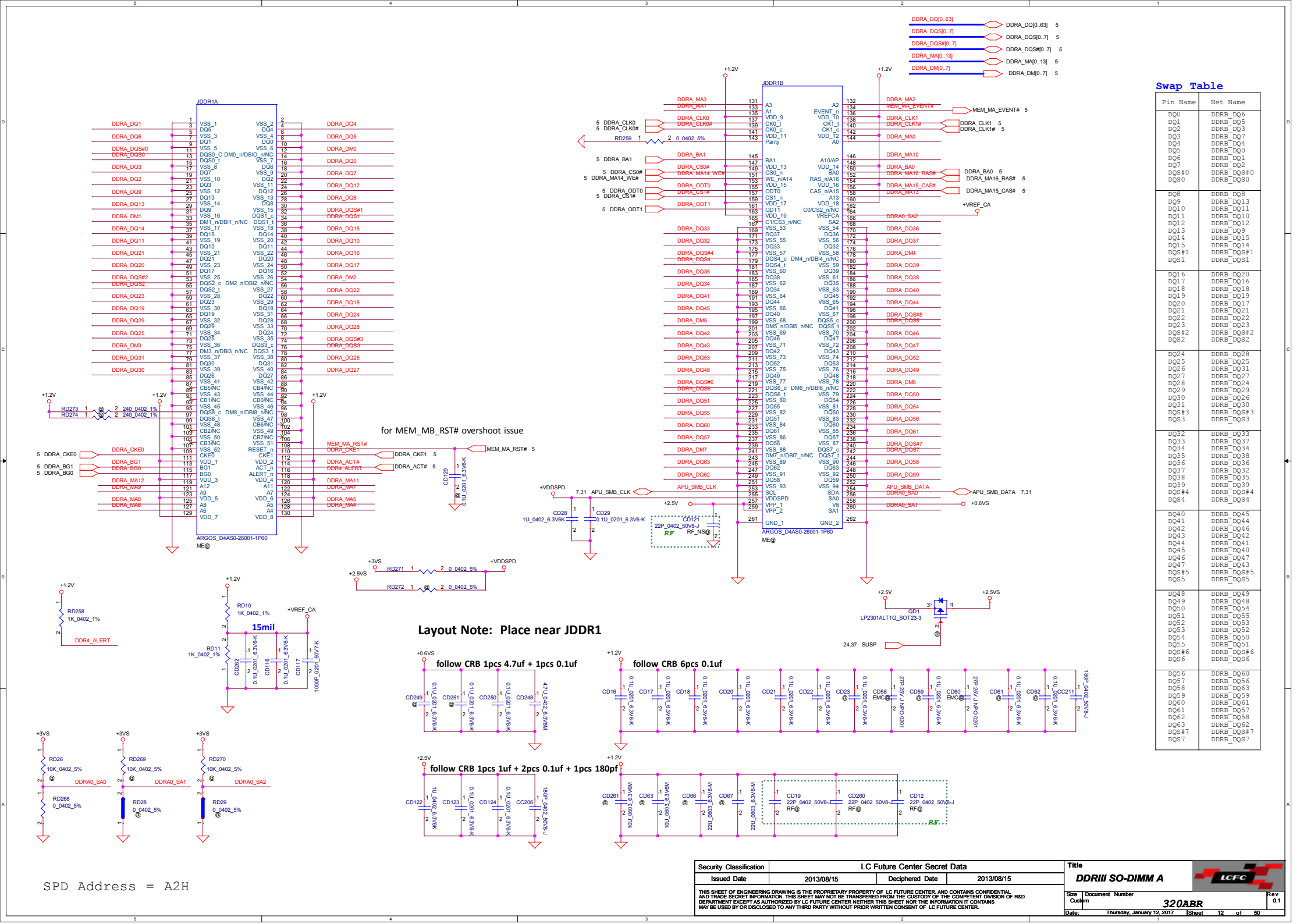
Platforms that are designed for AOAC complaint are recommended to use the Alternate Reset by strapping this pin to ' 1' for Ø AGPIO3

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: FP4 (STRAPS)

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 11 of 50



Swap Table

Pin Name	Net Name
DQ0	DDRB_DQ6
DQ1	DDRB_DQ5
DQ2	DDRB_DQ3
DQ3	DDRB_DQ7
DQ4	DDRB_DQ4
DQ5	DDRB_DQ0
DQ6	DDRB_DQ1
DQ7	DDRB_DQ2
DQS#0	DDRB_DQS#0
DQS0	DDRB_DQS0
DQ8	DDRB_DQ8
DQ9	DDRB_DQ13
DQ10	DDRB_DQ11
DQ11	DDRB_DQ10
DQ12	DDRB_DQ12
DQ13	DDRB_DQ9
DQ14	DDRB_DQ15
DQ15	DDRB_DQ14
DQS#1	DDRB_DQS#1
DQS1	DDRB_DQS1
DQ16	DDRB_DQ20
DQ17	DDRB_DQ16
DQ18	DDRB_DQ18
DQ19	DDRB_DQ19
DQ20	DDRB_DQ17
DQ21	DDRB_DQ21
DQ22	DDRB_DQ22
DQ23	DDRB_DQ23
DQS#2	DDRB_DQS#2
DQS2	DDRB_DQS2
DQ24	DDRB_DQ28
DQ25	DDRB_DQ25
DQ26	DDRB_DQ31
DQ27	DDRB_DQ27
DQ28	DDRB_DQ24
DQ29	DDRB_DQ29
DQ30	DDRB_DQ26
DQ31	DDRB_DQ30
DQS#3	DDRB_DQS#3
DQS3	DDRB_DQS3
DQ32	DDRB_DQ33
DQ33	DDRB_DQ37
DQ34	DDRB_DQ34
DQ35	DDRB_DQ38
DQ36	DDRB_DQ36
DQ37	DDRB_DQ32
DQ38	DDRB_DQ32
DQ39	DDRB_DQ39
DQS#4	DDRB_DQS#4
DQS4	DDRB_DQS4
DQ40	DDRB_DQ45
DQ41	DDRB_DQ44
DQ42	DDRB_DQ46
DQ43	DDRB_DQ42
DQ44	DDRB_DQ41
DQ45	DDRB_DQ40
DQ46	DDRB_DQ47
DQ47	DDRB_DQ43
DQS#5	DDRB_DQS#5
DQS5	DDRB_DQS5
DQ48	DDRB_DQ49
DQ49	DDRB_DQ48
DQ50	DDRB_DQ54
DQ51	DDRB_DQ55
DQ52	DDRB_DQ53
DQ53	DDRB_DQ52
DQ54	DDRB_DQ50
DQ55	DDRB_DQ51
DQS#6	DDRB_DQS#6
DQS6	DDRB_DQS6
DQ56	DDRB_DQ60
DQ57	DDRB_DQ56
DQ58	DDRB_DQ63
DQ59	DDRB_DQ59
DQ60	DDRB_DQ61
DQ61	DDRB_DQ57
DQ62	DDRB_DQ58
DQ63	DDRB_DQ62
DQS#7	DDRB_DQS#7
DQS7	DDRB_DQS7

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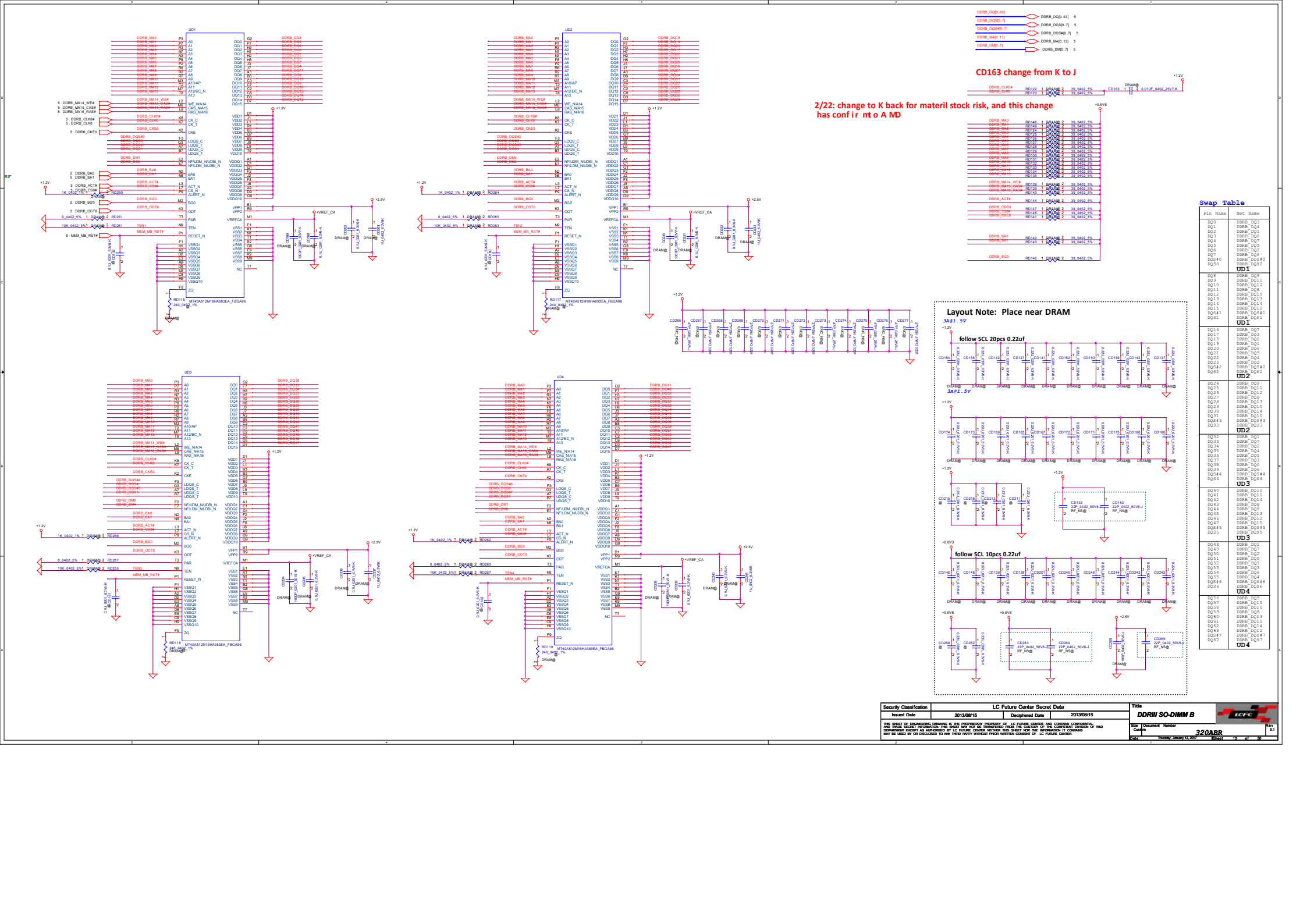
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: **DDRIII SO-DIMM A**

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 | Sheet 12 of 50


CD163 change from K to J
2/22: change to K back for materil stock risk, and this change has confir mto A MD
Layout Note: Place near DRAM
follow SCL 20pcs 0.22uf
follow SCL 10pcs 0.22uf
Swap Table
Pin Name
Net Name
UD1
UD2
UD3
UD4
LC Future Center Secret Data
Issued Date
2013/08/15
Deciphered Date
2013/08/15
DDRIII SO-DIMM B
320ABR
Thursday, January 12, 2017

Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

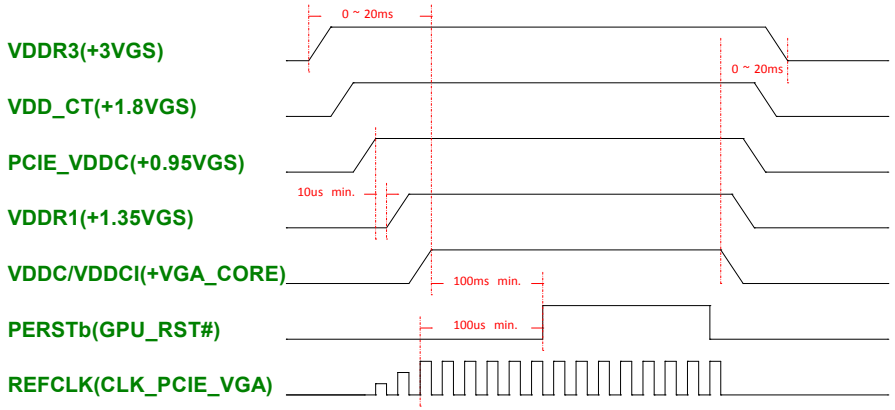
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µ s).

For power down, reversing the ramp-up sequence is recommended.



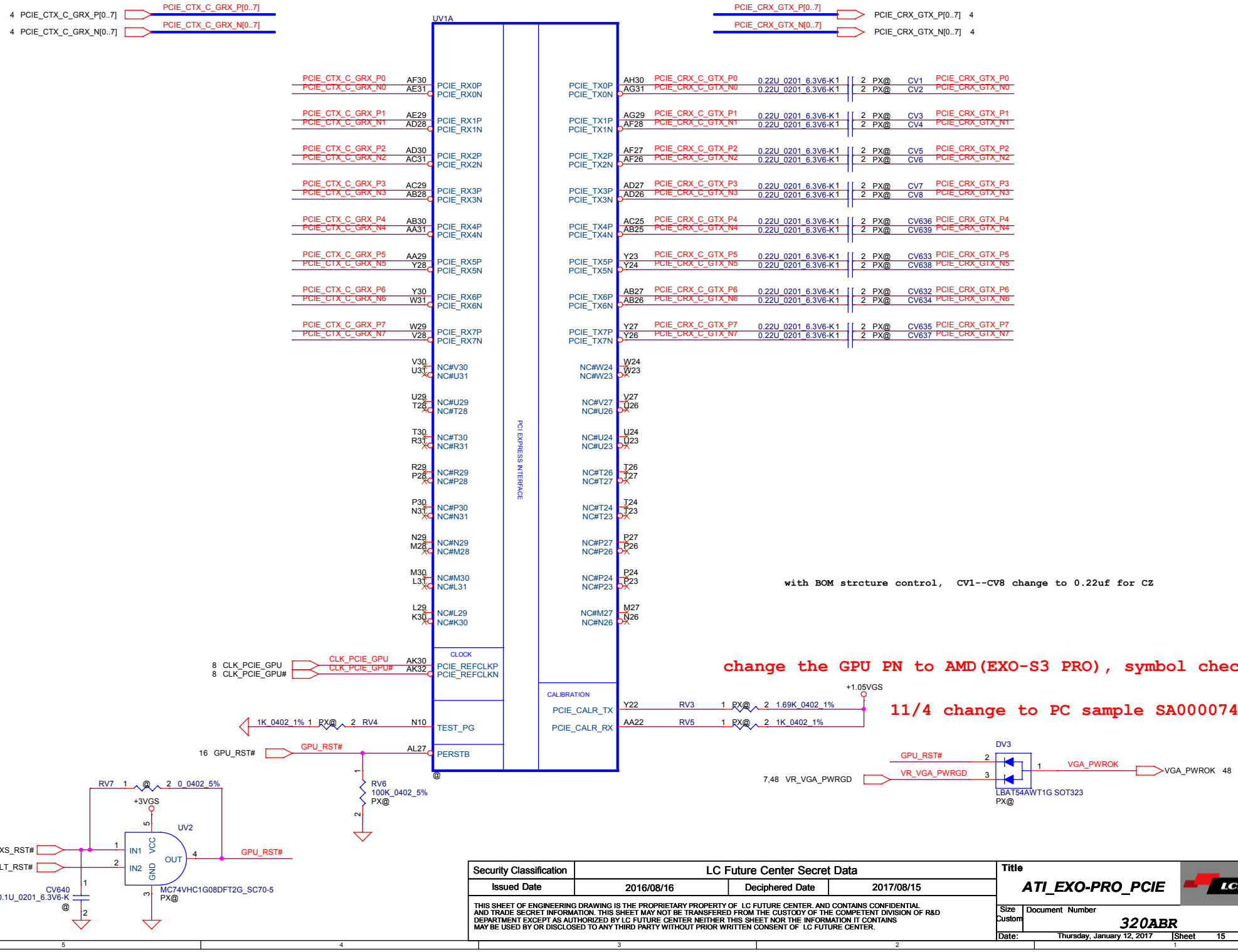
VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
4Gb GDDR5 256M x 16	Hynix H5GC4H24AJR-R0C 6.0Gbps@1.35V	100	4.53K	4.99K
	Micron EDW4032BABG-70-F 6.0Gbps@1.35V	111	4.75K	NC
	Samsung K4G41325FE-HC28 6.0Gbps@1.35V	110	3.4K	10K
8Gb GDDR5 512M x 16	Hynix H5GC8H24MJR-R0C 6.0Gbps@1.35V	000	NC	4.75K
	Micron MT51J256M32HF-70:A 6.0Gbps@1.35V	010	4.53K	2K
	Samsung K4G80325FB-HC28 6.0Gbps@1.35V	001	8.45K	2K

Title: VGA Notes List

Size: Custom | Document Number: 320ABR | Rev: 0.1

Date: Thursday, January 12, 2017 | Sheet 14 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: ATI_EXO-PRO_PCIE

Size: Custom	Document Number: 320ABR	Rev: 0.1
Date: Thursday, January 12, 2017	Sheet 15 of 50	

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 001 = 256MB	x
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 1= GEN3 is supported	x
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	x
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	x
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system' s VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 100 = Hynix 4Gb 000 = Hynix 8Gb 111 = Micron 4Gb 010 = Micron 8Gb 110 = Samsung 4Gb 001 = Samsung 8Gb	x
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 111= No usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are useable.	11

MLPS	Bit					BOM		
	5	4	3	2	1	R_pu( )	R_pd( )	C(nF)
PS_0[5:1]	1	1	0	0	1	RV71=8.45k	RV77=2K	CV15=NC
PS_1[5:1]	1	1	0	0	1	RV74=8.45K	RV80=2K	CV16=NC
PS_2[5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC
PS_3[5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=NC

with BOM strcture control,
RV63,RV70 change to different value to adjust VRAM config

with BOM strcture control,
when config PEG3
RV74 change to 8.45K,
RV80 change to 2K

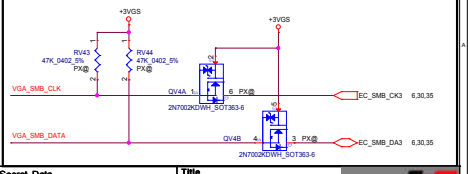
Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Internal VGA Thermal Sensor



Reserve

Reserve for Topaz

Pull down for none OBFF design

2016/09/02: Pull-down GPU_CLKREQ# at GPU side

no symbol for 8pf cap, PLM has PN,change the PN

(1.8V@20mA TSVDD)

Connect GPIO_28 to 10K pull down to enable MLPS.

For Topaz, RV23/RV24 stuff 100ohm
For EXO, RV23/RV24 stuff 0hm

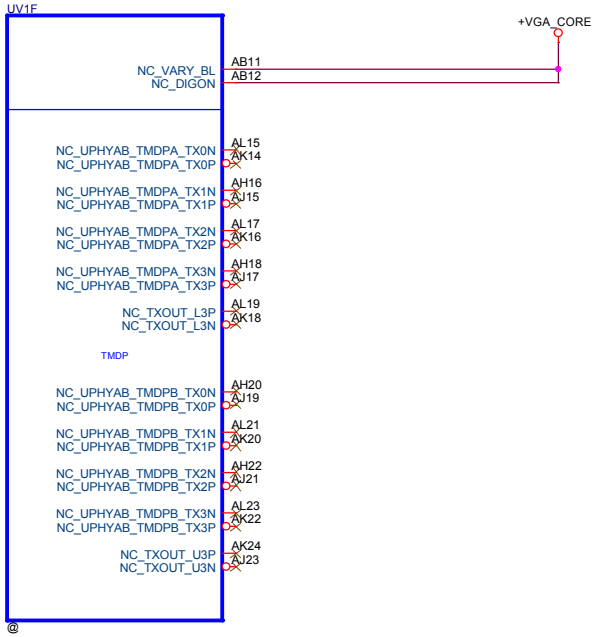
Security Classification	LC Future Center Secret Data	
Issued Date	2016/08/16	Deciphered Date 2017/08/15

Title: ATI_EXO-PRO_Main_MSIC

LCFC

Size	Document Number	Rev
Custom	320ABR	0.1

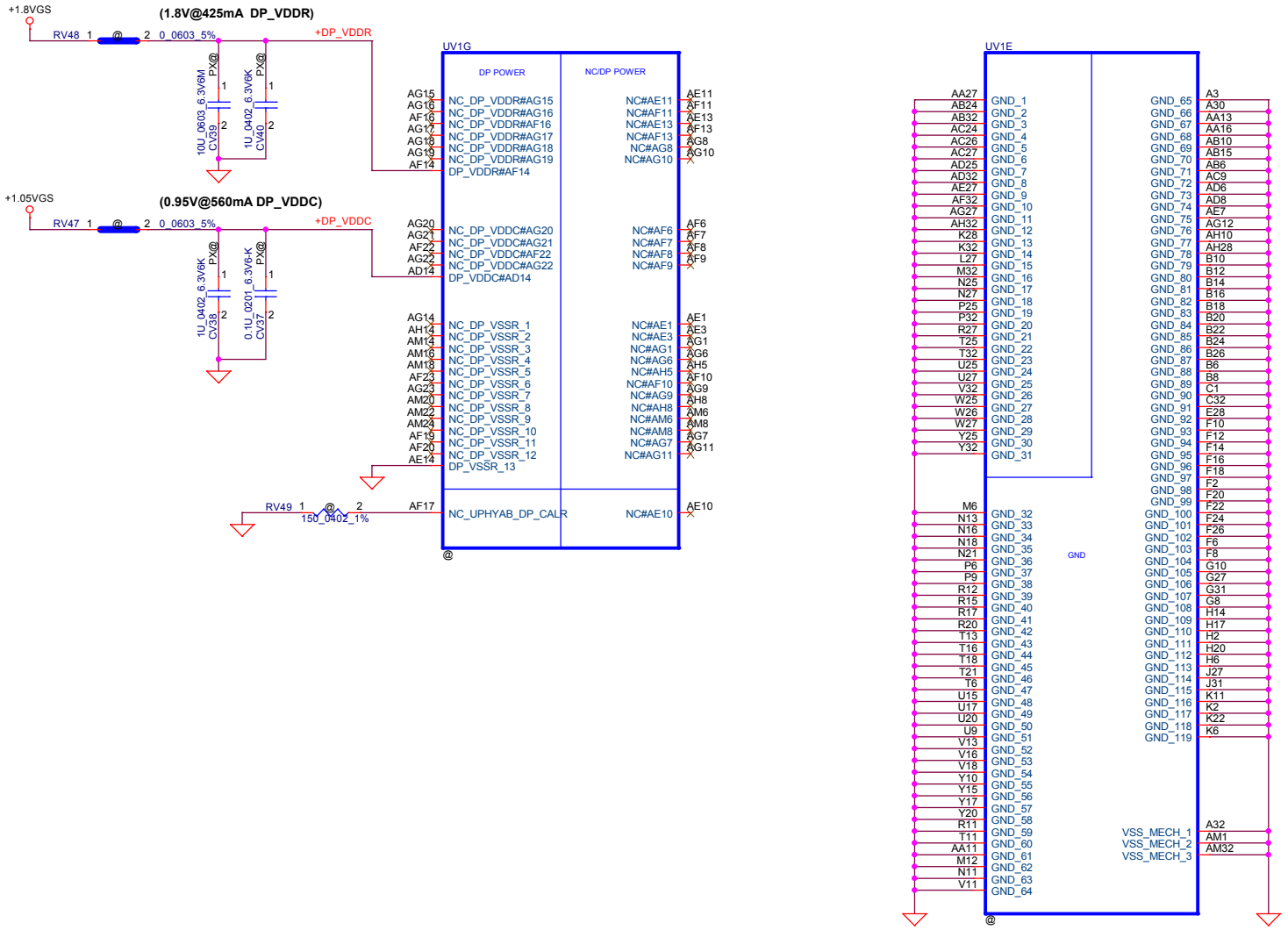
Date: Thursday, January 12, 2017 Sheet 16 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: ATI_EXO-PRO_TMDP

Size: Custom	Document Number: 320ABR	Rev: 0.1
Date: Thursday, January 12, 2017	Sheet 17 of 50	

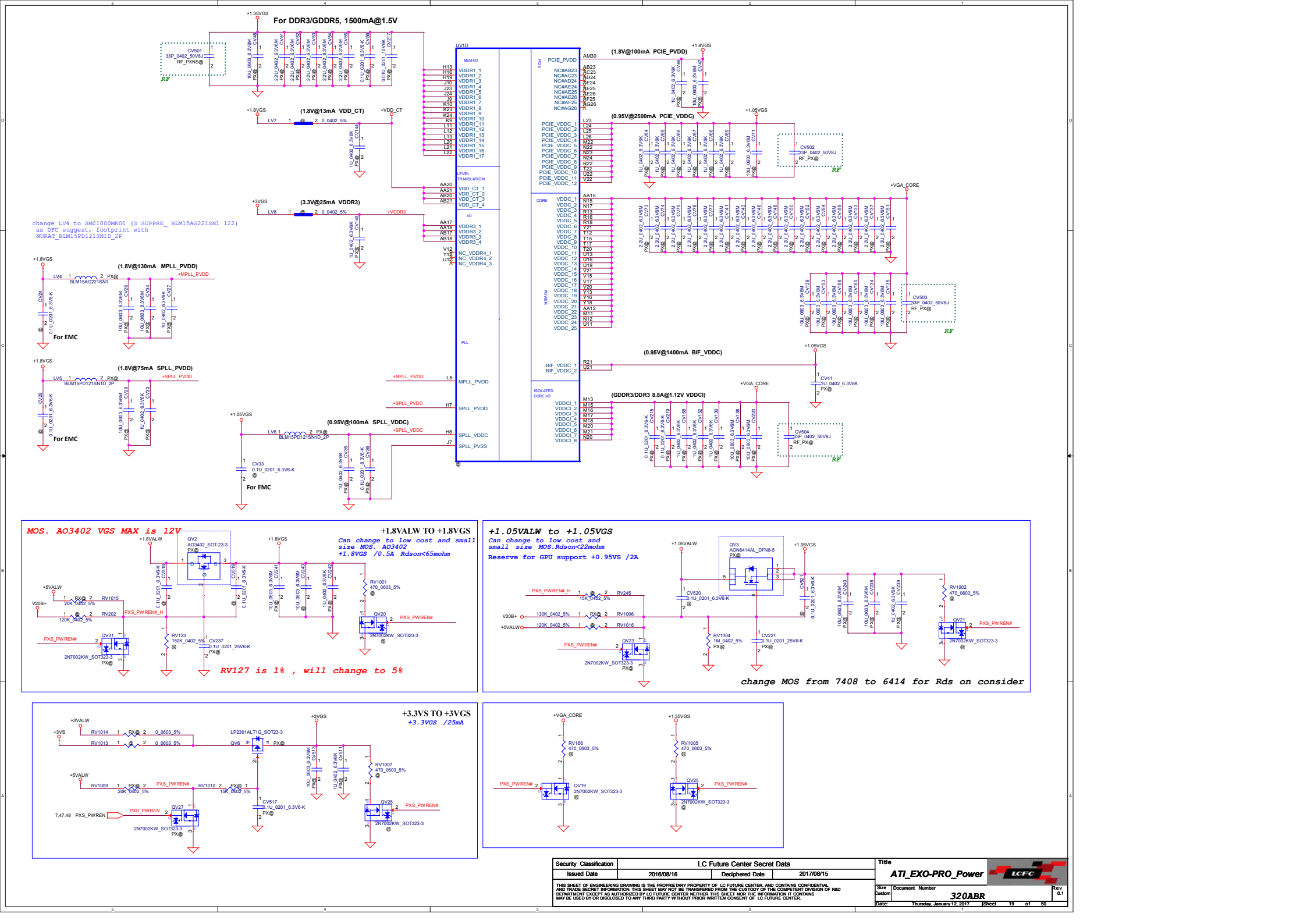


Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: ATI_EXO-PRO_DP Power

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 18 of 50

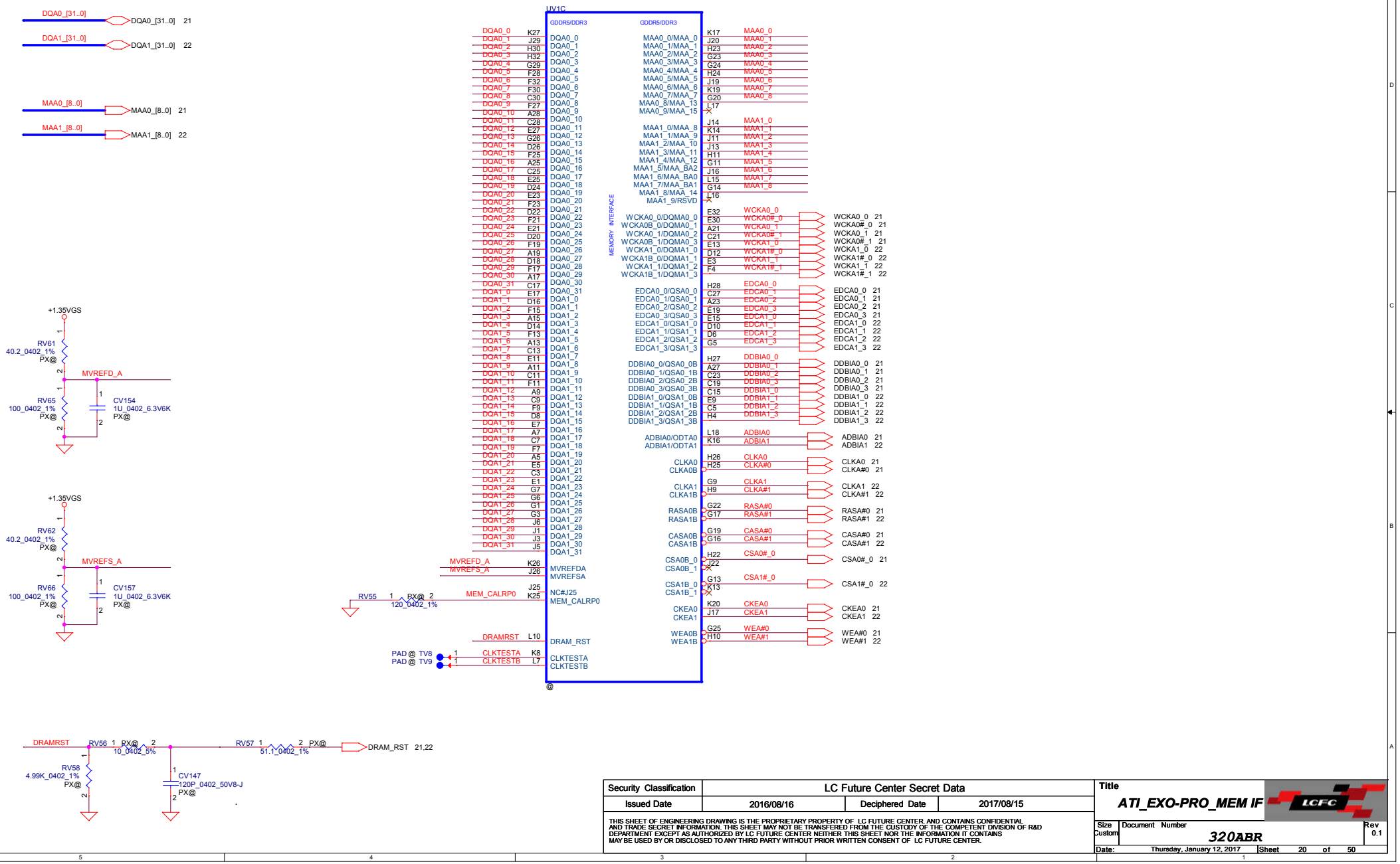


Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: ATI_EXO-PRO_Power

Size: Custom | Document Number: 320ABR | Rev: 0.1

Date: Thursday, January 12, 2017 | Sheet 19 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

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Title: ATI_EXO-PRO_MEM IF

Size	Document Number	Rev
Custom	320ABR	0.1

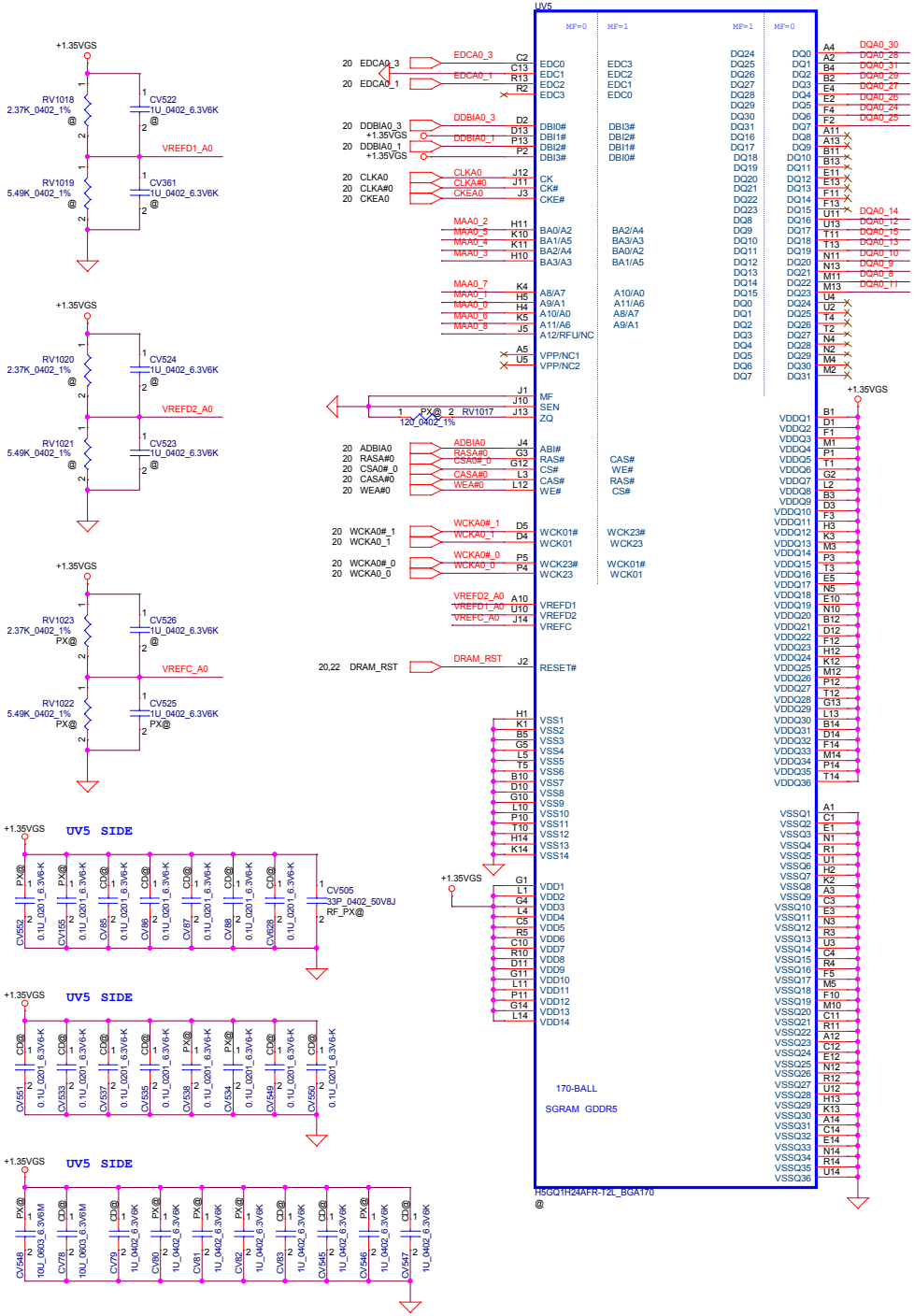
Date: Thursday, January 12, 2017 Sheet 20 of 50

Lower 32 bits

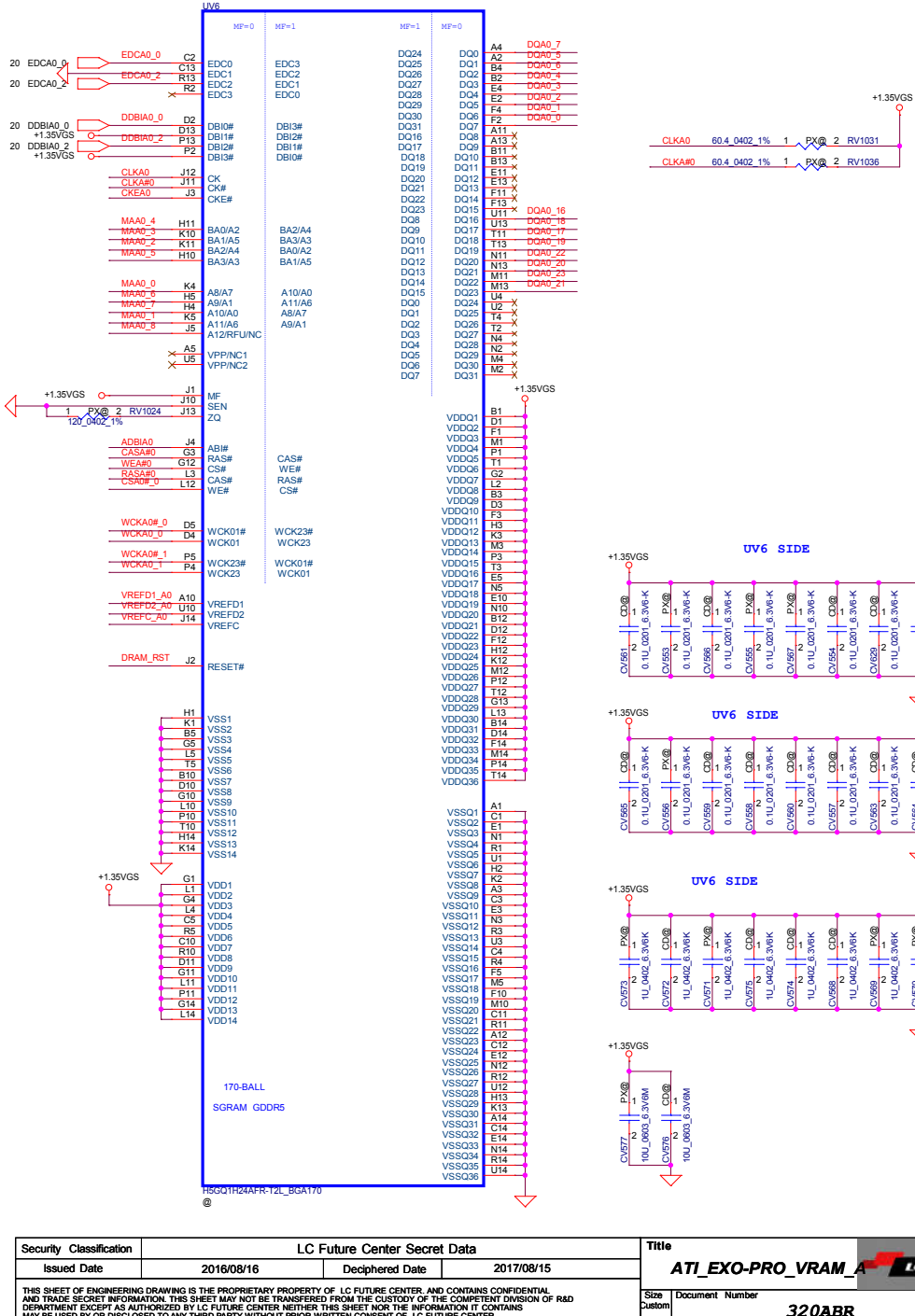
DQA0_[31..0] 20

MAA0_[8..0] 20

MF=0 No Mirror



MF=1 Mirror



UV5 SIDE

UV6 SIDE

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: ATI_EXO-PRO_VRAM_A

Size	Document Number	Rev
Custom	320ABR	0.1

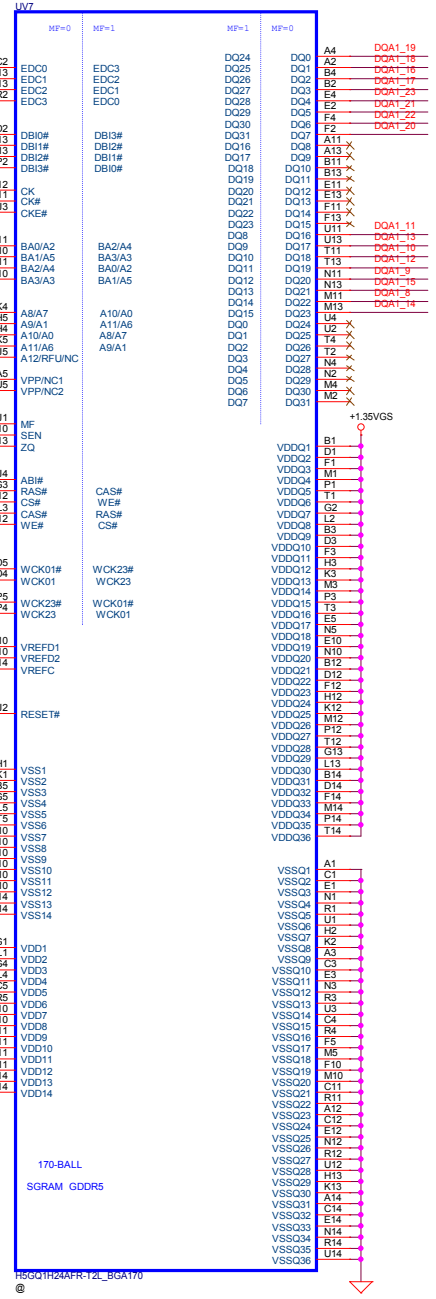
Date: Thursday, January 12, 2017 | Sheet 21 of 50

Upper 32 bits

DQA1_[31..0] 20

MAA1_[8..0] 20

MF=1 Mirror



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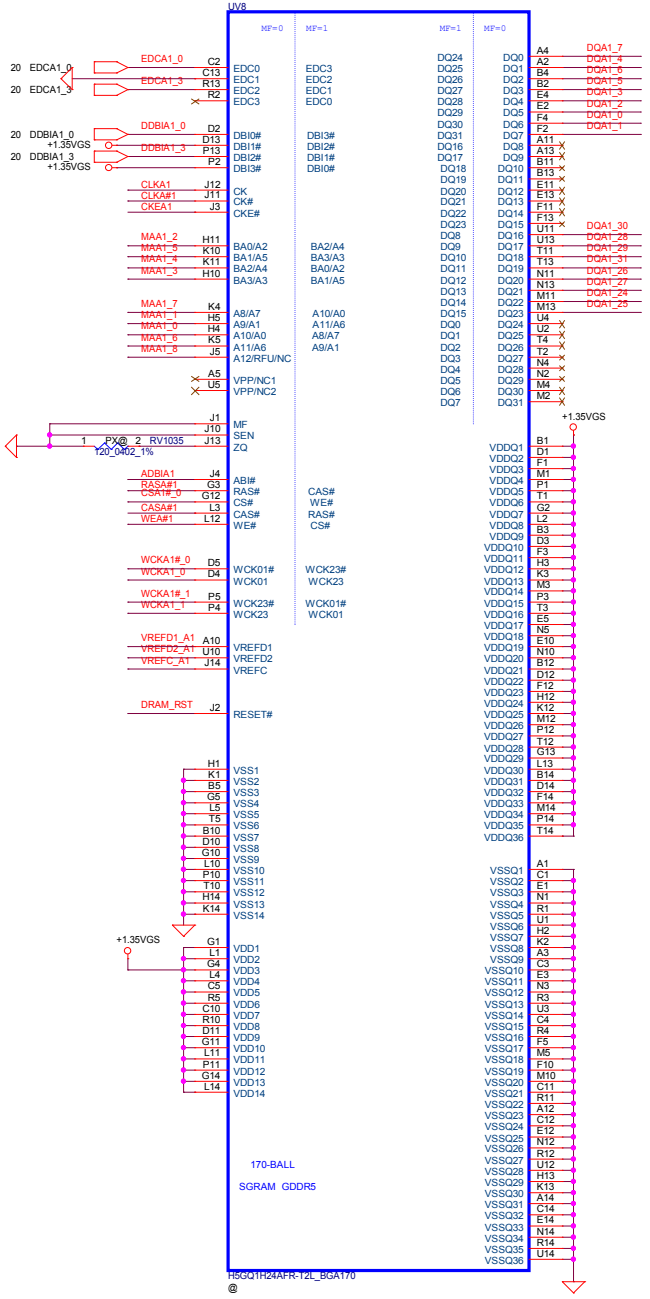
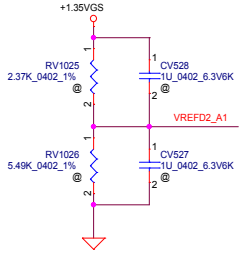
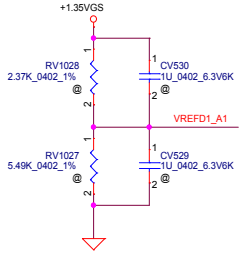
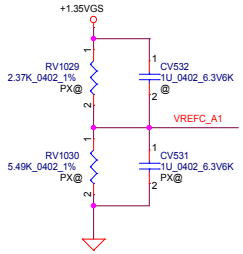
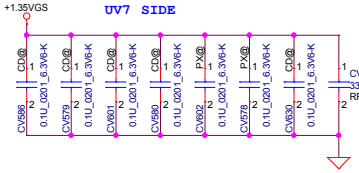
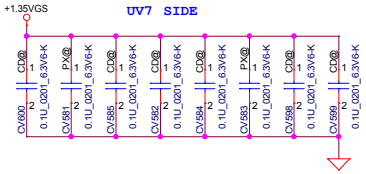


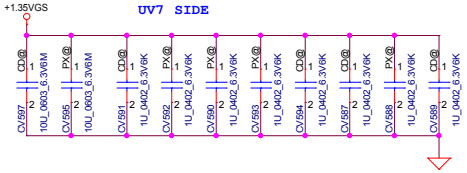


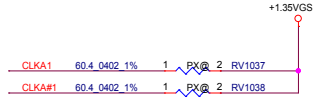


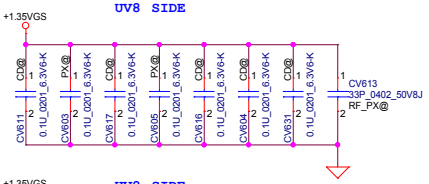


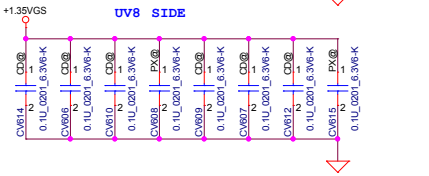


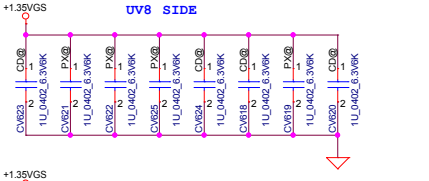


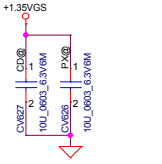












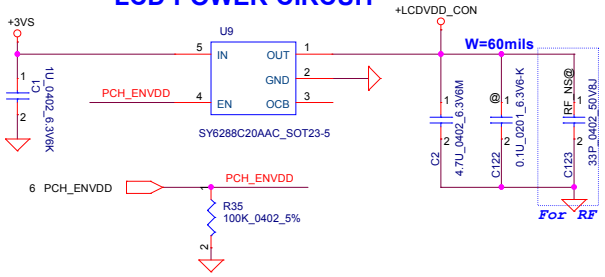
Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title: ATI_EXO-PRO_VRAM_B

Size	Document Number	Rev
Custom	320ABR	0.1

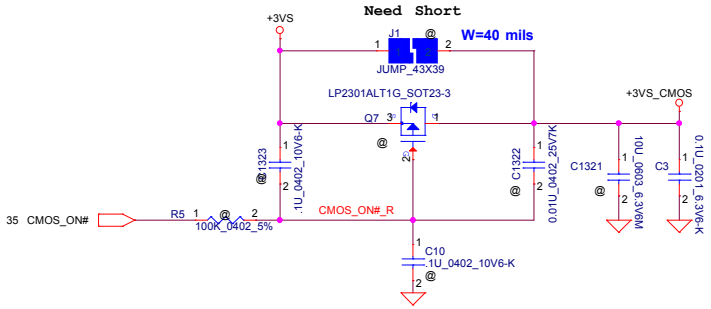
Date: Thursday, January 12, 2017 Sheet 22 of 50

LCD POWER CIRCUIT

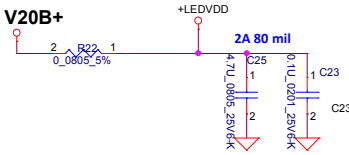


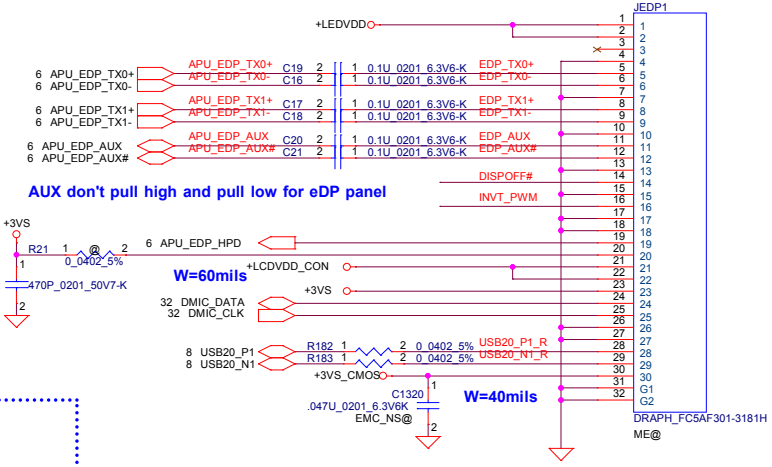
APU output enable Voh min is 1.8V-0.45V=1.35V

Need Short

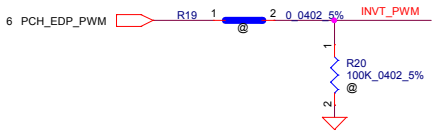


B+ to +LEDVDD POWER

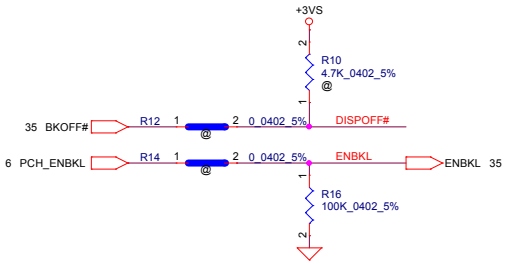




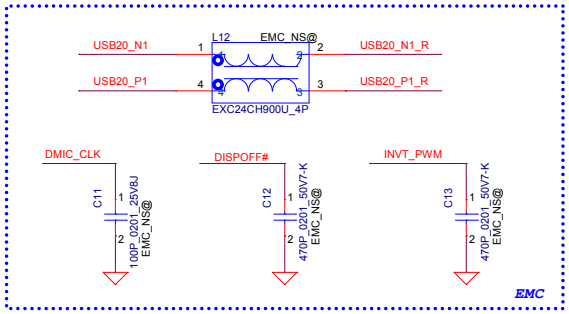
AUX don't pull high and pull low for eDP panel



Need Short

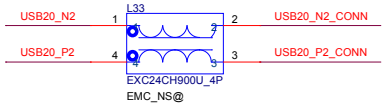


CMOS Camera

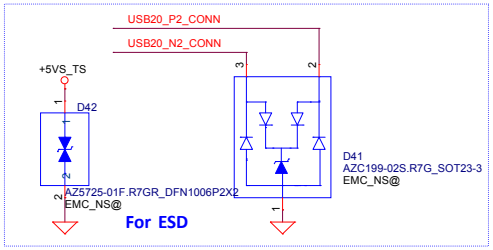


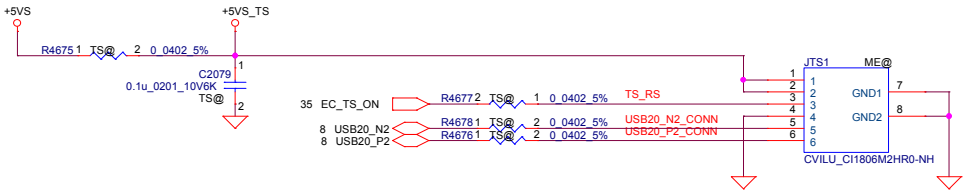
Touch Screen

Touch Screen



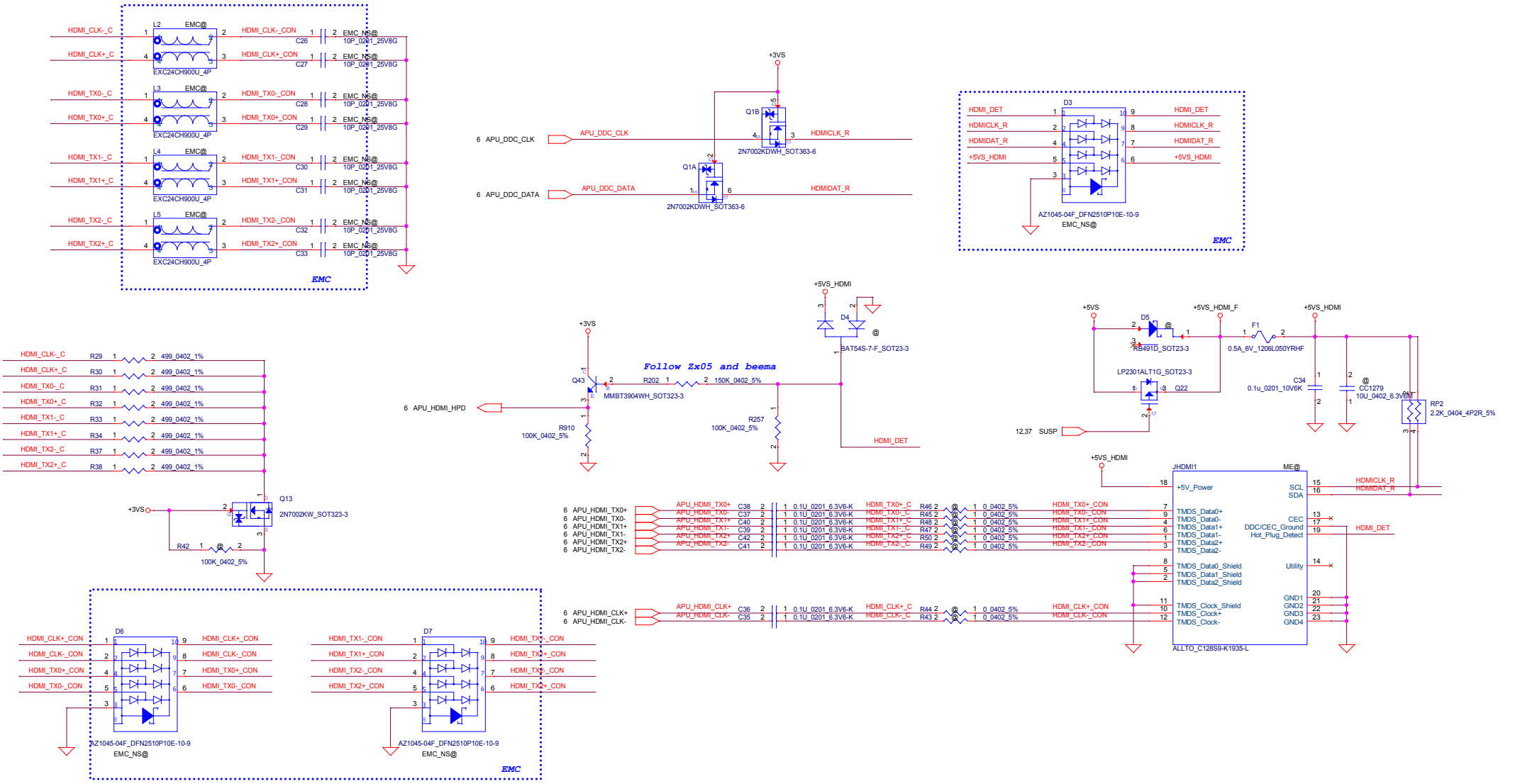
For EMI





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

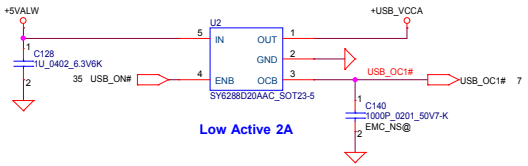
Title	eDP/CMOS/TS		
Size	Document Number		Rev
Custom	320ABR		0.1
Date:	Thursday, January 12, 2017	Sheet	23 of 50



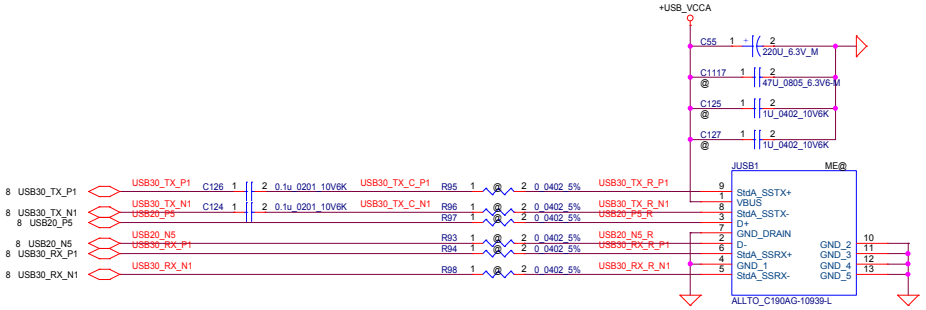
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

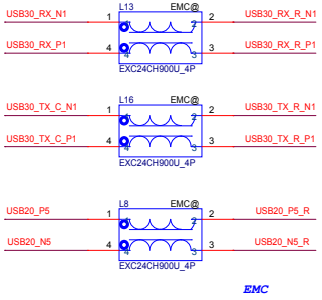
Title	HDMI_CONN		
Size	Document Number		Rev
Custom	320ABR		0.1
Date:	Thursday, January 12, 2017	Sheet	24 of 50

LEFT SIDE USB3.0 PORT x2

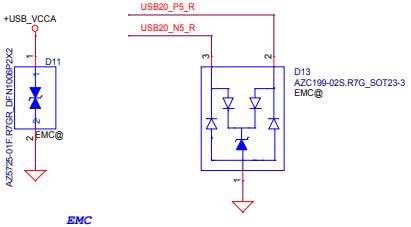


Low Active 2A

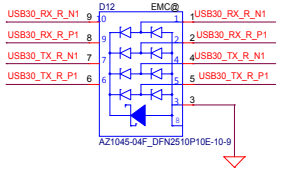


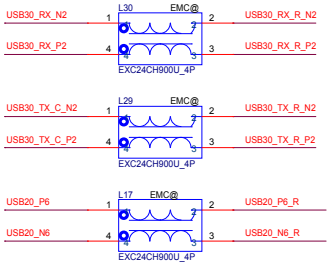


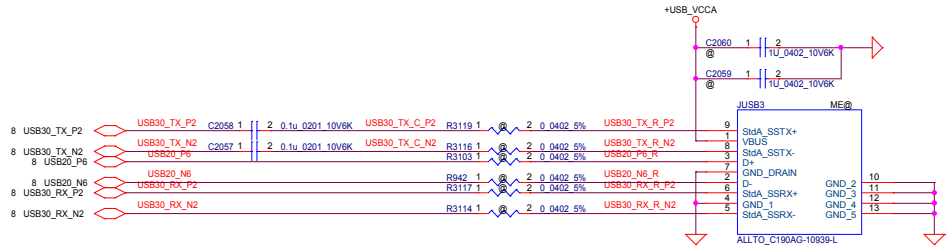
EMC



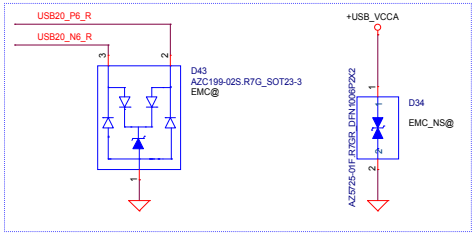
EMC

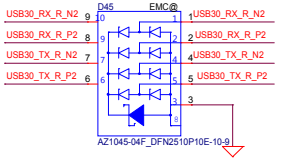






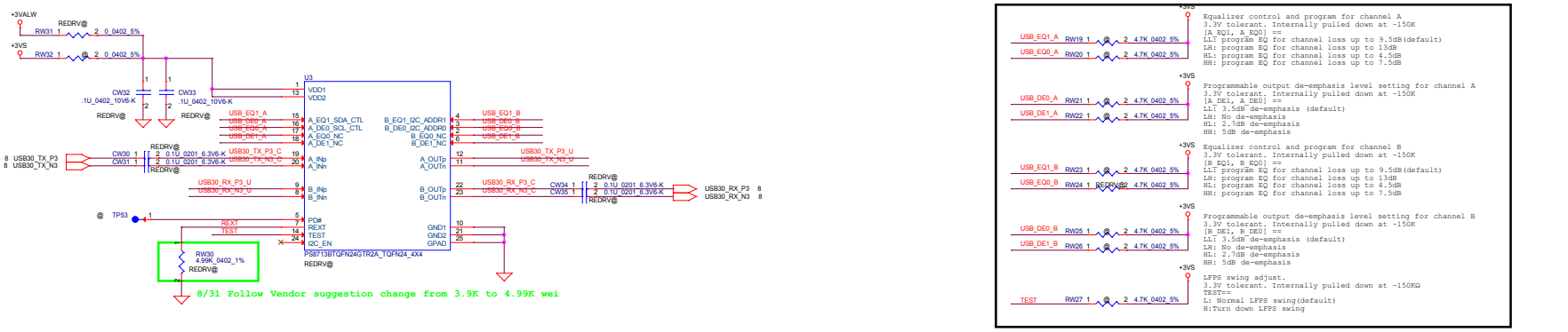
FOR ESD Close to Connector

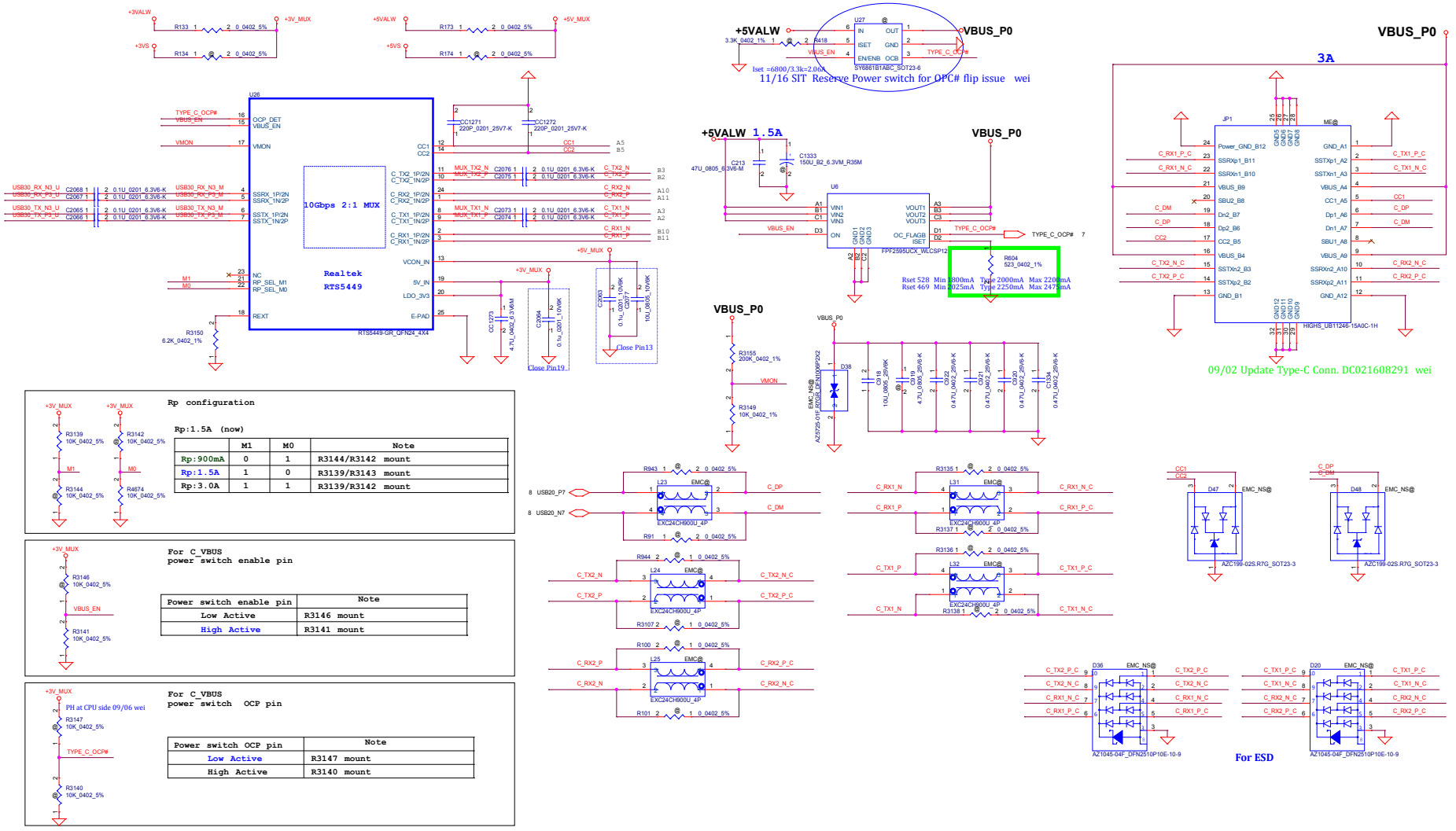




Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title	USB3.0 PORT (LEFT)		
Size C	Document Number 320ABR		Rev 0.1
Date: Thursday, January 12, 2017	Sheet 25 of 50		





Rp configuration

Rp:1.5A (now)

	M1	M0	Note
Rp:900mA	0	1	R3144/R3142 mount
Rp:1.5A	1	0	R3139/R3143 mount
Rp:3.0A	1	1	R3139/R3142 mount

For C_VBUS power switch enable pin

Power switch enable pin	Note
Low Active	R3146 mount
High Active	R3141 mount

For C_VBUS power switch OCP pin

PH at CPU side 09/06 wei

Power switch OCP pin	Note
Low Active	R3147 mount
High Active	R3140 mount

For ESD

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title	3D Camera		
Size: Custom	Document Number: 320ABR		Rev: 0.1
Date: Thursday, January 12, 2017	Sheet 26 of 50		

Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

Title

Blank

Size	Document Number	Rev
B	320ABR	0.1

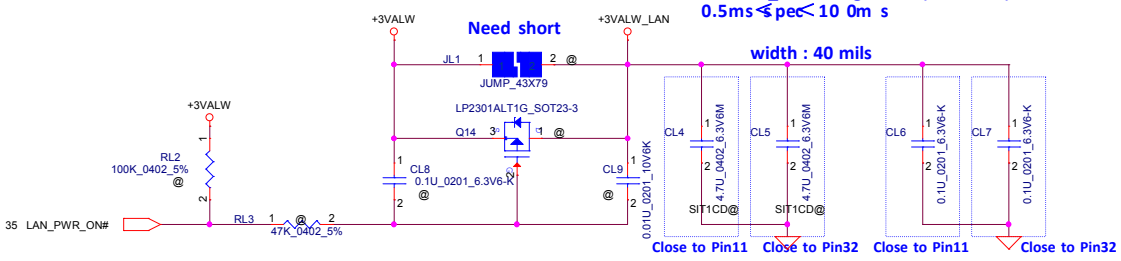
Date: Thursday, January 12, 2017 Sheet 27 of 50

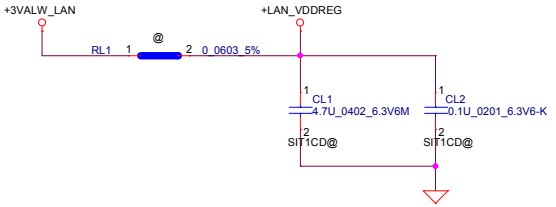
+3VALW TO +3VALW_LAN

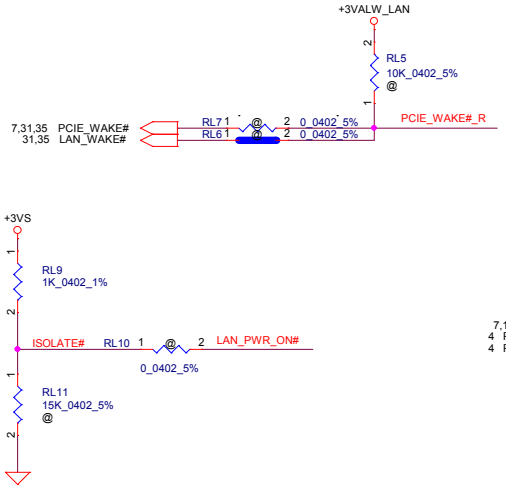
+3VALW_LAN rising time (10%~90%) 0.5ms<spec<10 0ms

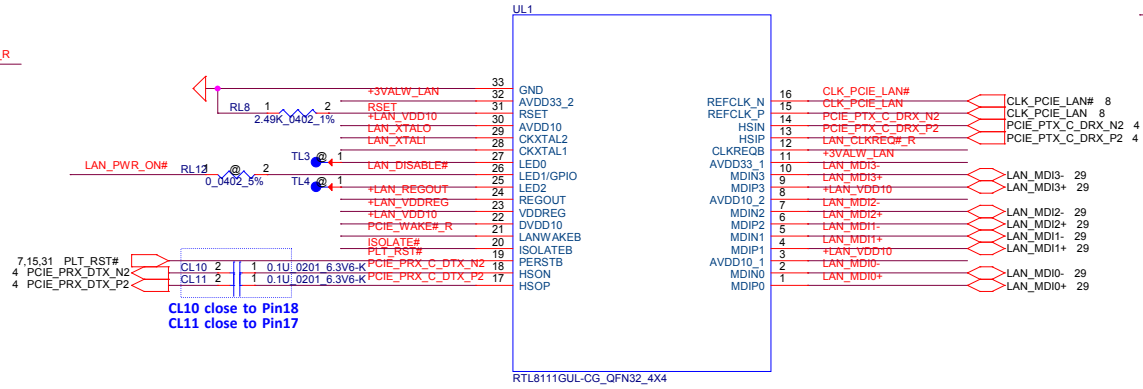
Need short

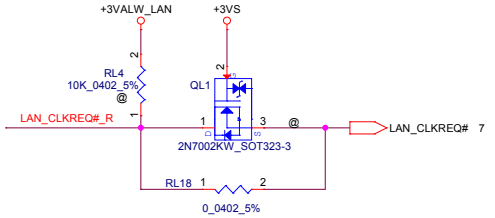
width : 40 mils



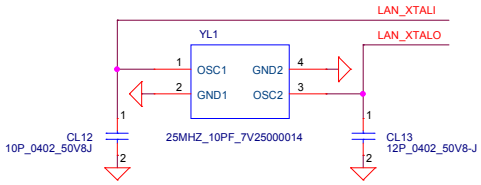






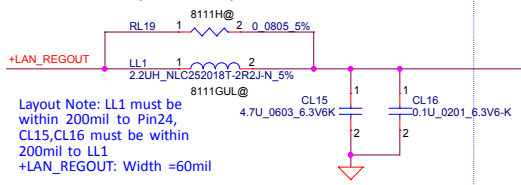


APU CLKREQ all both 3VS power plane

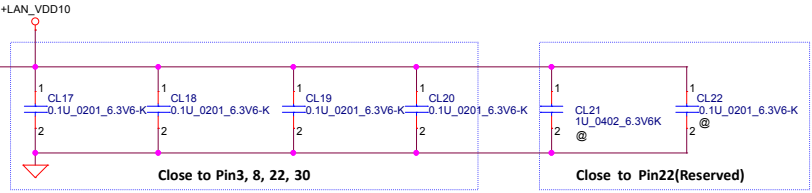


follow G CarrizoL 10pf

For RTL8111GUL/ RTL8106EUL (SWR mode)
For RTL8111H (LDO mode) RL19 stuf f



Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil



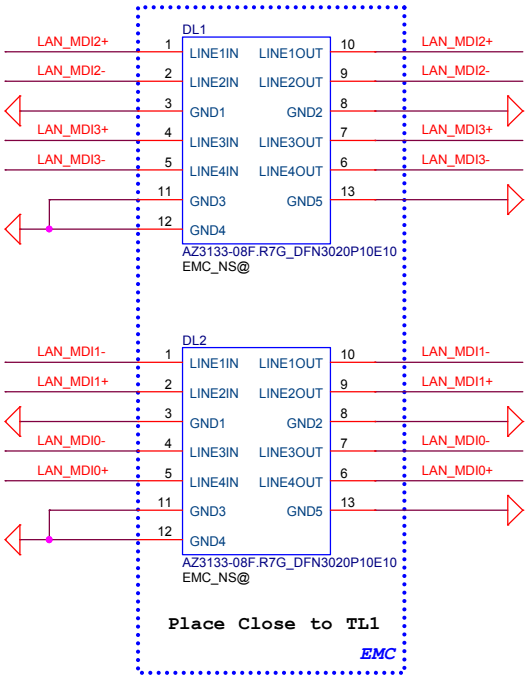
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

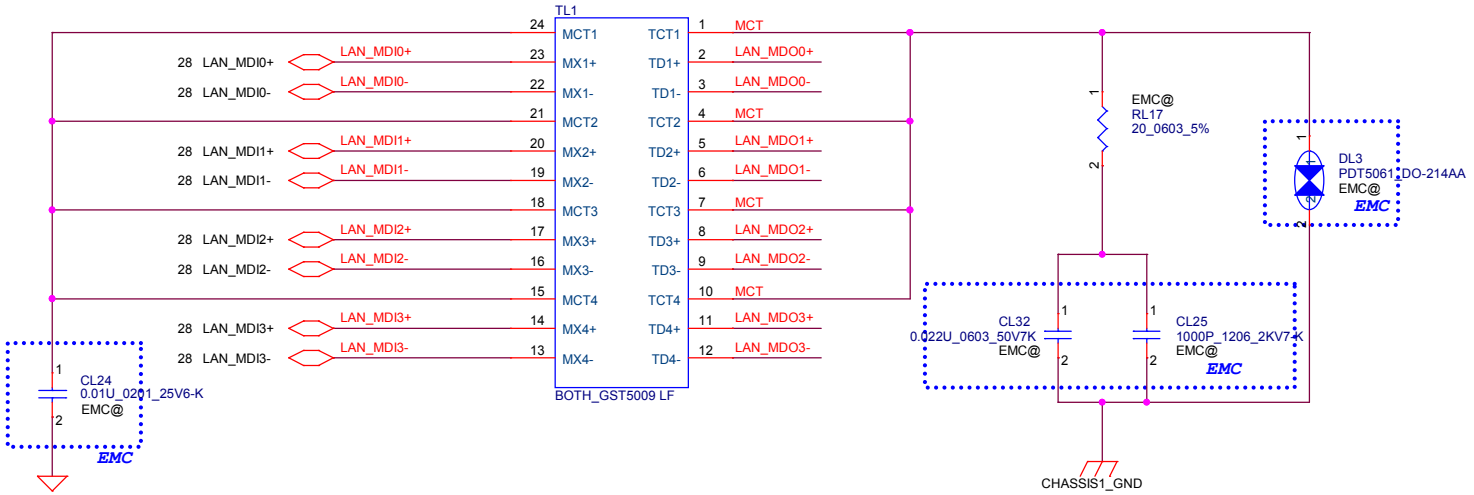
Title: LAN_RTL8111GUL

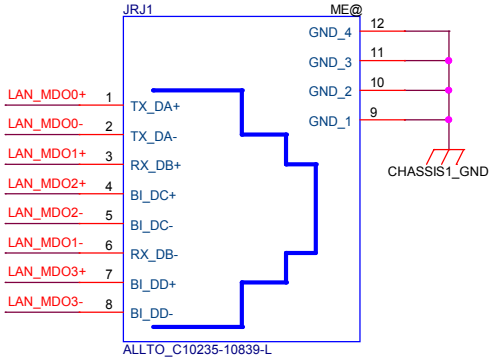
Size	Document Number	Rev
Custom	320ABR	0.1

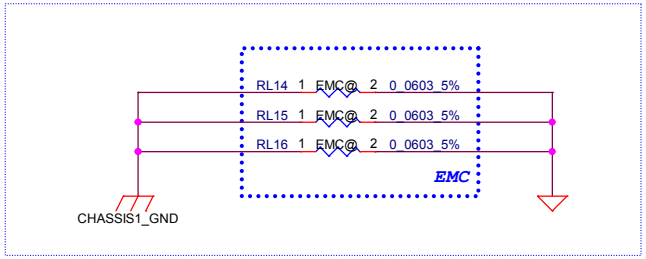
Date: Thursday, January 12, 2017 Sheet 28 of 50

DL1/DL2
1'S PN:SC300003M00







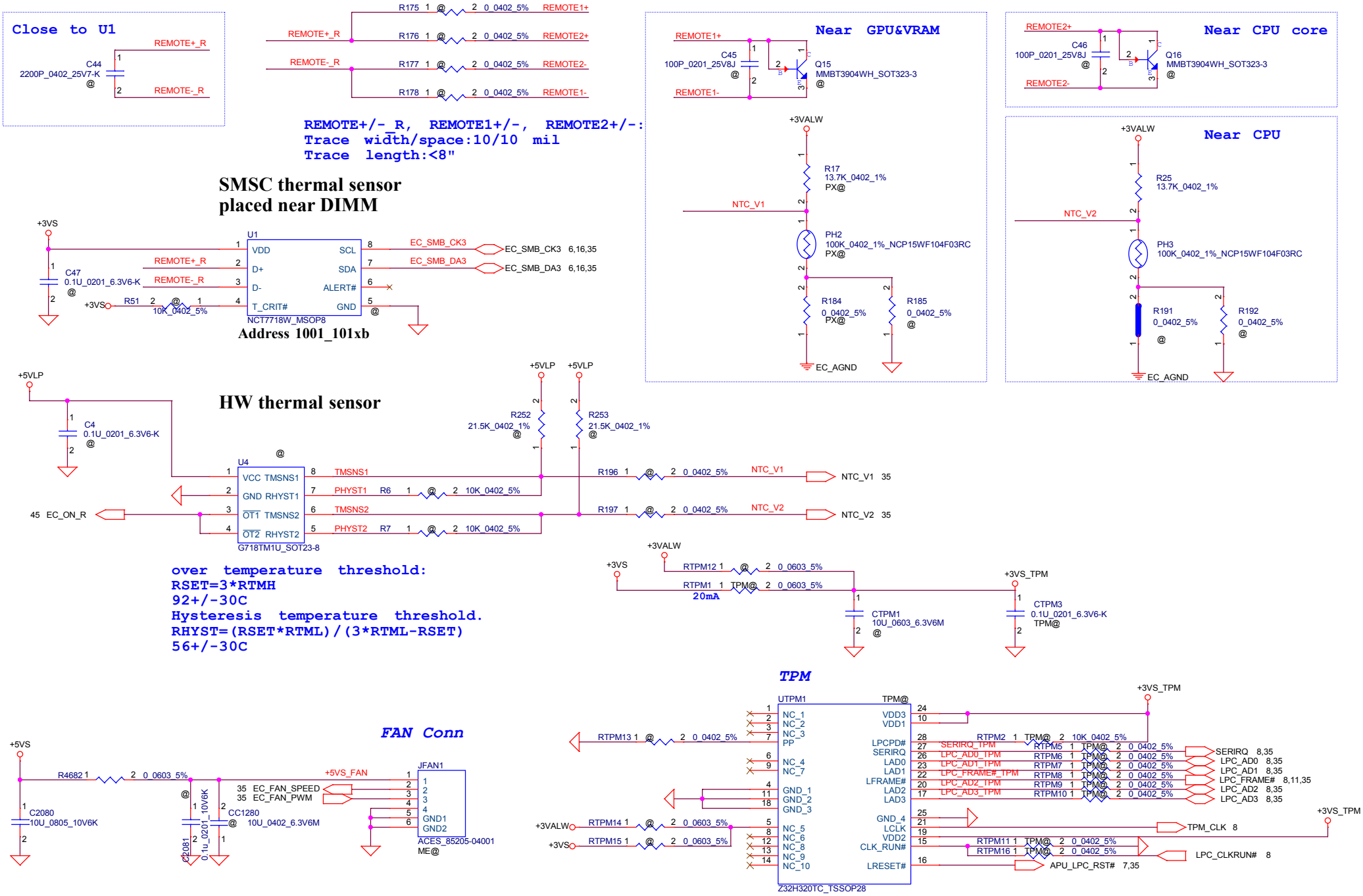


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: LAN_Transformer

Size	Document Number	Rev
Custom	320ABR	0.1

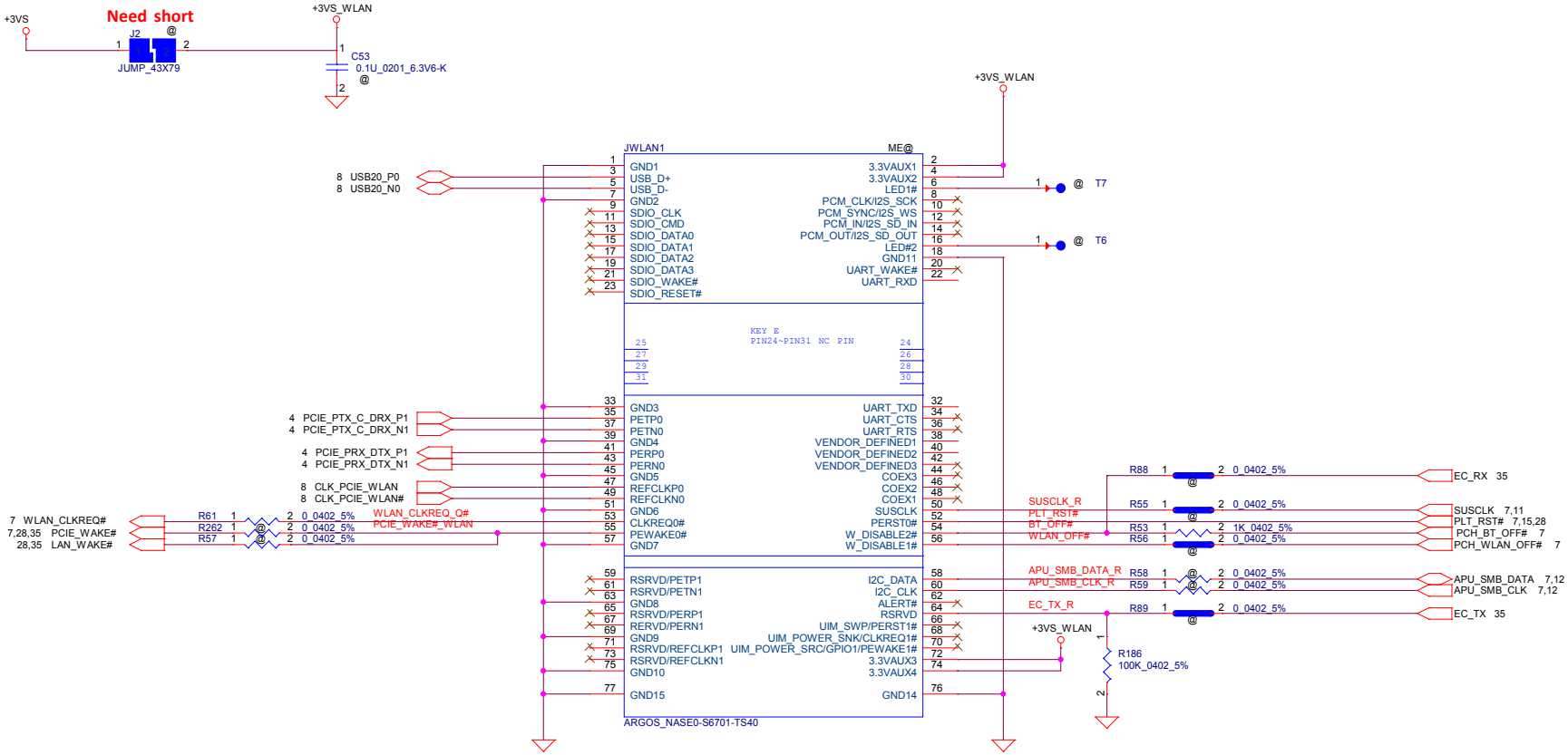
Date: Thursday, January 12, 2017 | Sheet 29 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	Thermal sensor/FAN CONN/TPM		
Size	Document Number		Rev
Custom	320ABR		0.1
Date:	Thursday, January 12, 2017	Sheet	30 of 50

Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	NGFF WLAN		
Size: Custom	Document Number: 320ABR		Rev: 0.1
Date: Thursday, January 12, 2017	Sheet 31 of 50		

Digital power for HDA link

Analog power for mixers, & IO ports

Power supply for full-bridge left/Right channel

8/29 Add +1.8VS Circuit for Audio wei

Analog power for DACs, ADCs

Digital power for digital I/O circuit

ABR USB leakage issue, card reader power need 3VALW

Power for combo jack depop circuit at system shutdown mode

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

8/16 Update Audio Jack P/N SP011509163 wei

8/16 Update Audio Jack P/N DC021608101 wei

Audio Jack

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Issued Date	2016/08/16	Deciphered Date	2017/08/15

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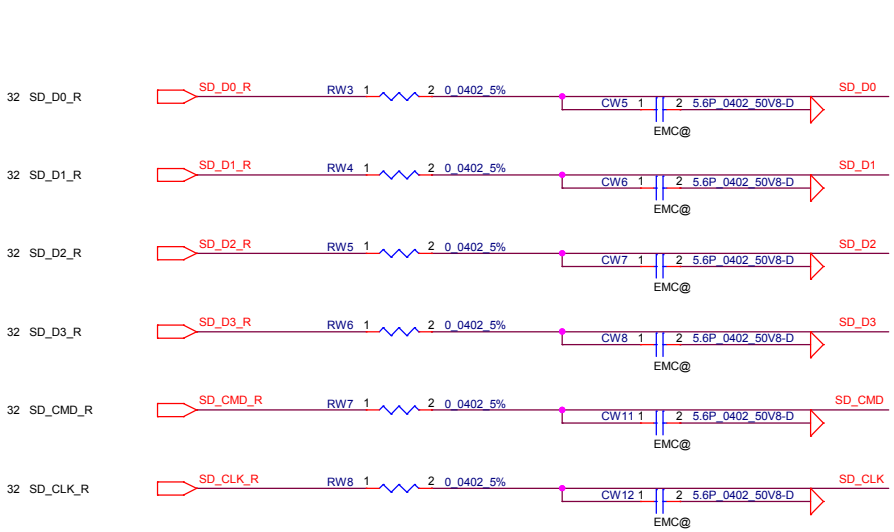
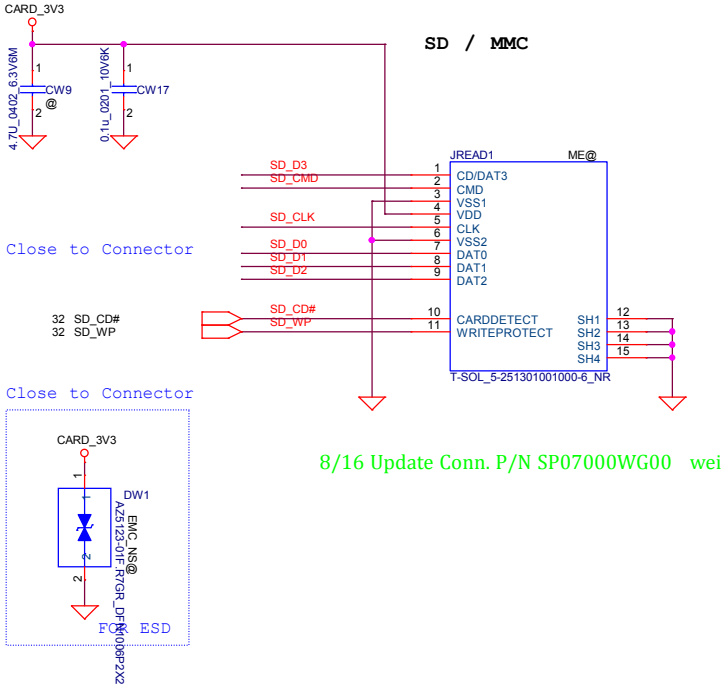
Title: Codec & CR_RTS5199

Size: Custom | Document Number: 320ABR | Rev: 0.1

Date: Thursday, January 12, 2017 | Sheet 32 of 50





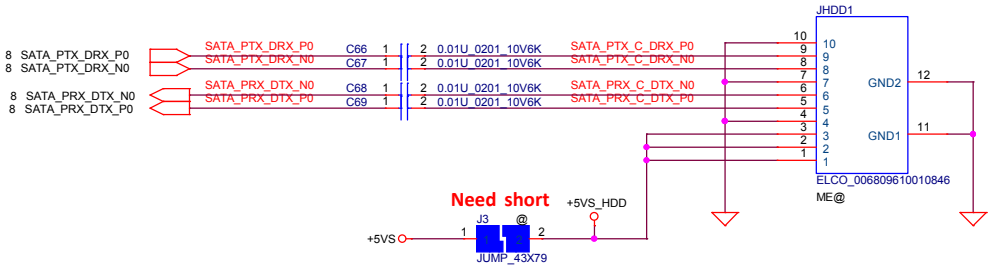
Security Classification	LC Future Center Secret Data		
Issued Date	2016/08/16	Deciphered Date	2017/08/15

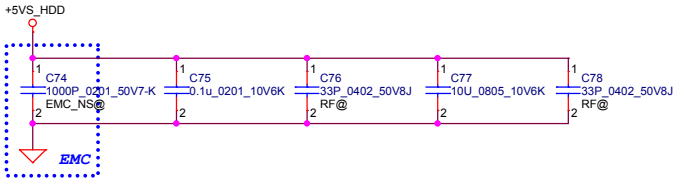
Title: **Cardreader**

Size	Document Number	Rev
Custom	320ABR	0.1

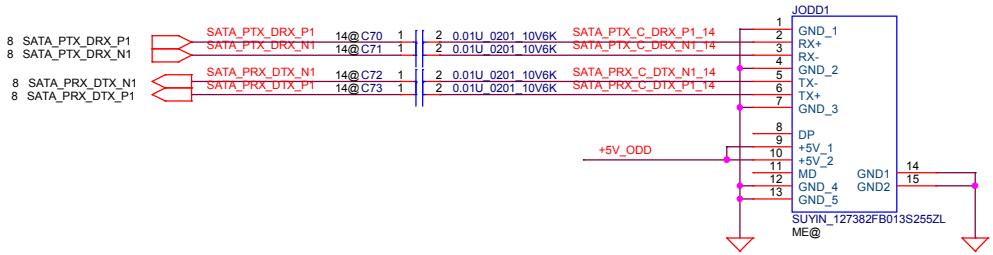
Date: Thursday, January 12, 2017 Sheet 33 of 50

SATA HDD Conn.





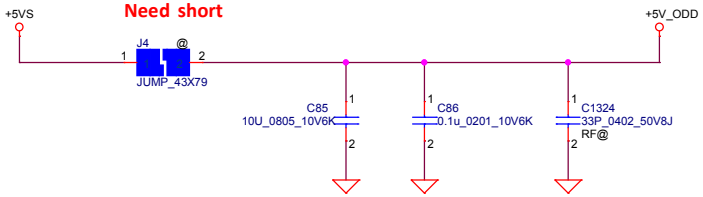
FOR 14" SATA ODD Conn.

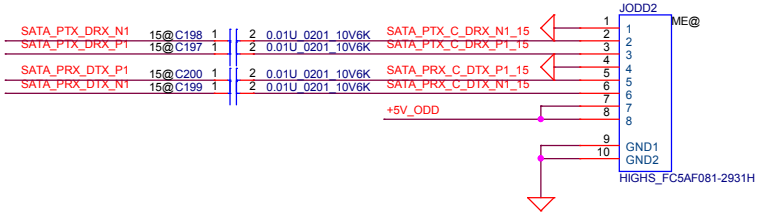


FOR 15" SATA ODD FFC Conn

SATA 15 ODD P/N pin assgin is different from G SKL

+5VS to +5V_ODD



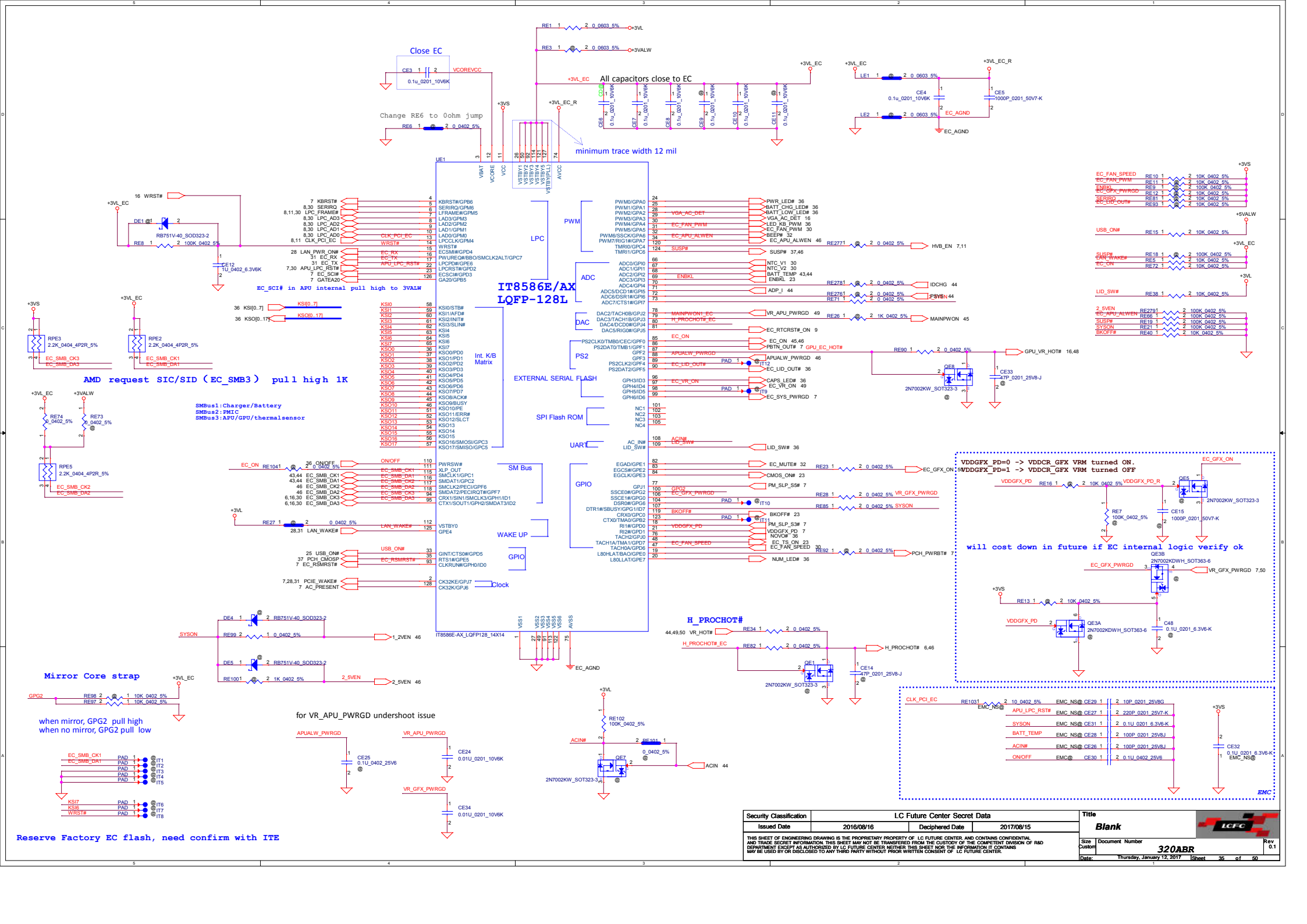


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **HDD/ODD CONN**

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 34 of 50



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Issued Date	2016/08/16	Deciphered Date	2017/08/15

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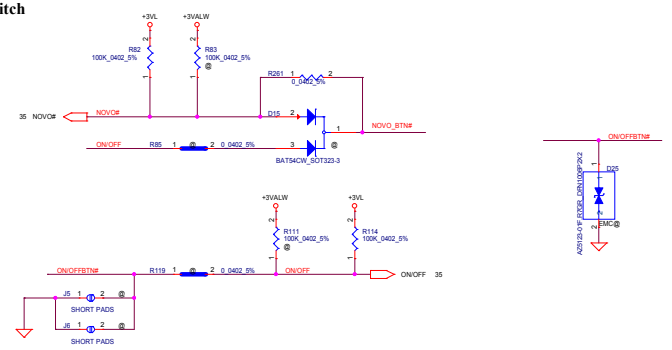
Title: **Blank**

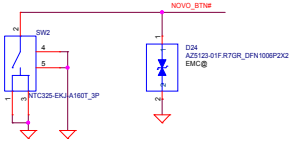
Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 35 of 50

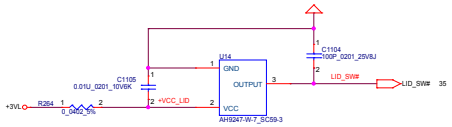
ON/OFF switch



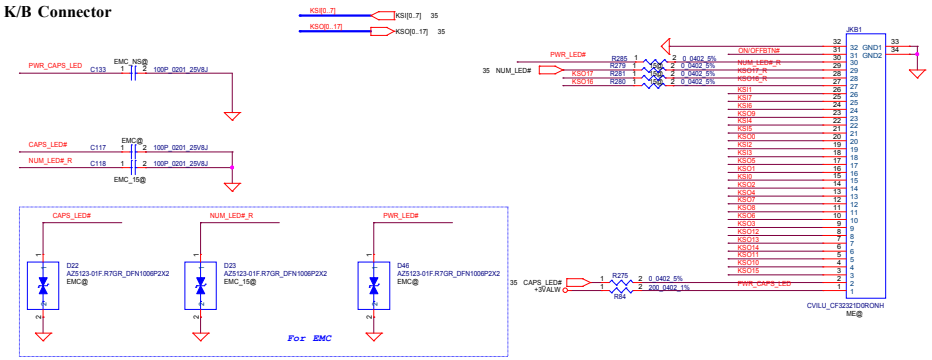
Novo button



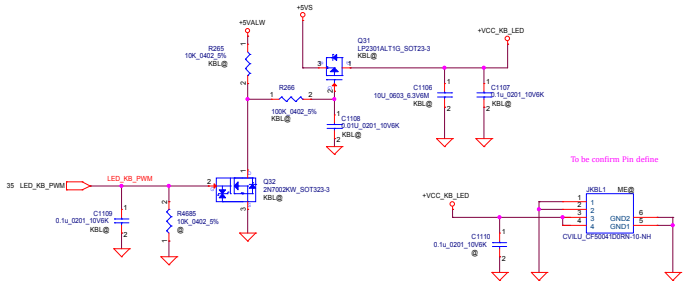
LID switch



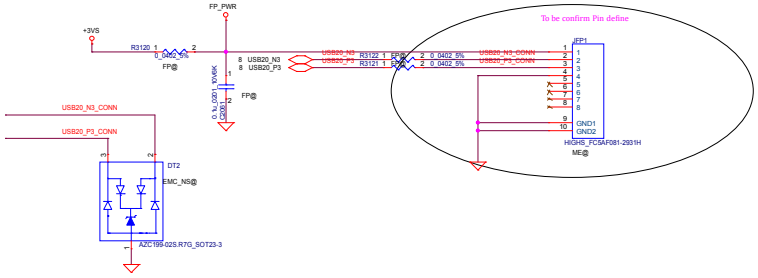
K/B Connector

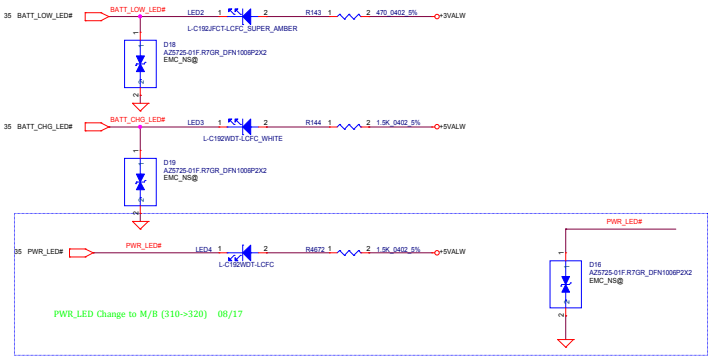


KB Backlight Connector

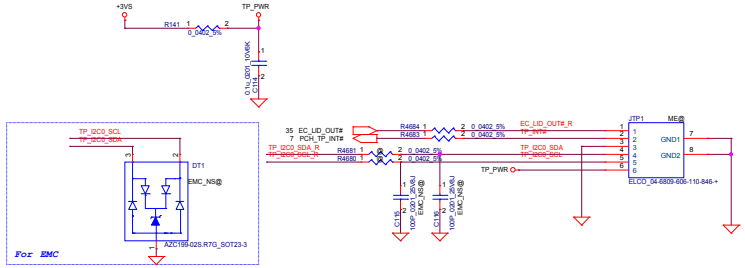


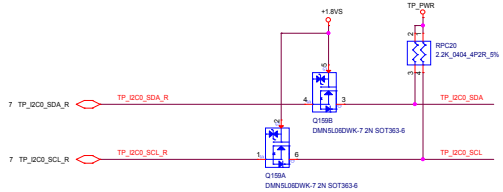
Finger Print Connector





TP/B Connector





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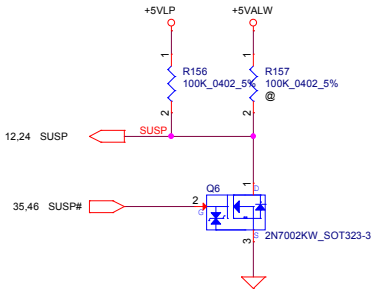
Title	KBD/PWR/IO/LED/TP Conn.		
Size: Custom	Document Number: 320ABR		Rev: 0.1
Date: Thursday, January 12, 2017	Sheet 36 of 50		



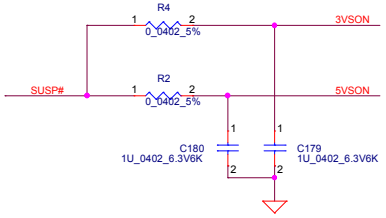
Load Switch

+5VALW To +5VS

+3VALW To +3VS

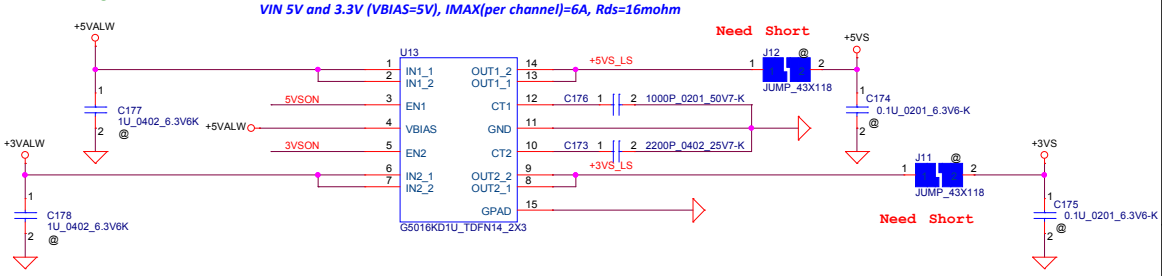
+3VS, C173 --> 5.78ms

+5VS, C176 --> 1.71ms



modify load swt ichfro mAPL3523 t o G5016KD1 UTDF N14P

VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

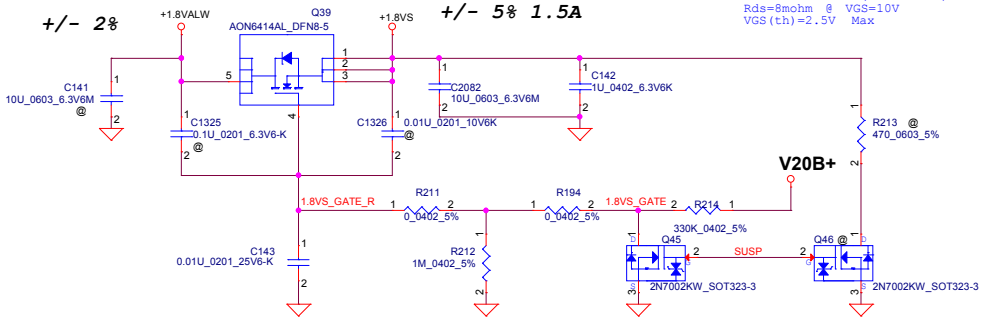


+1.8VALW to +1.8VS

+/- 2%

+/- 5% 1.5A

AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max



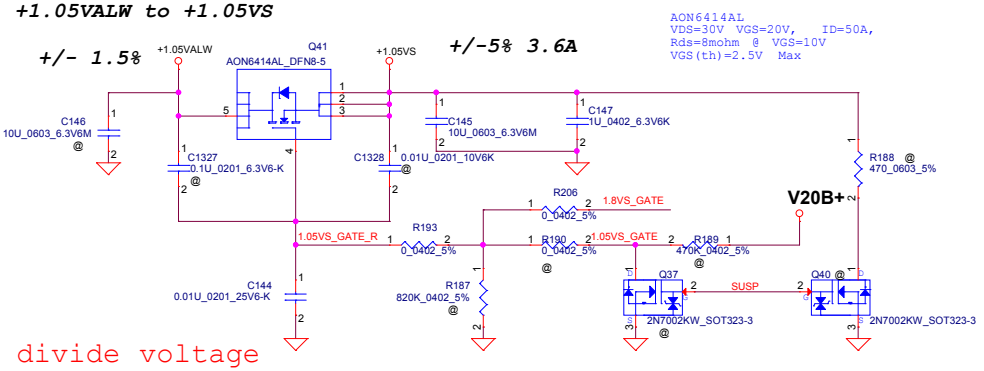
20VSB will change to 6V in DC mode, careful the Res divide voltage

+1.05VALW to +1.05VS

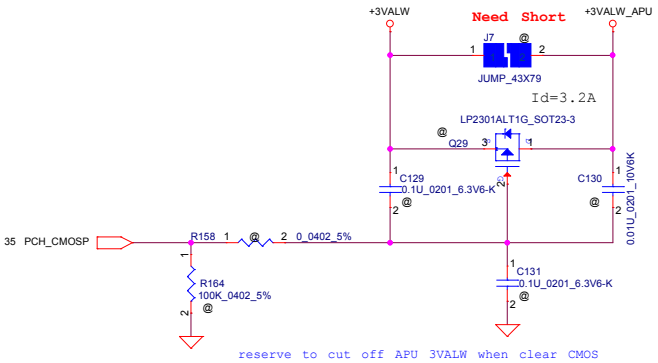
+/- 1.5%

+/-5% 3.6A

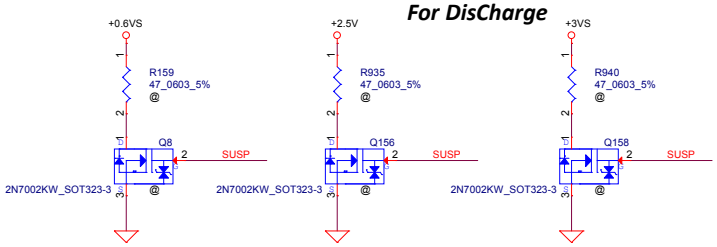
AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max

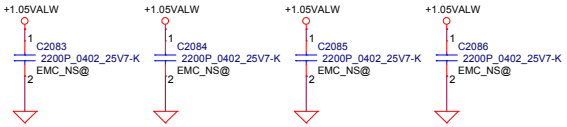


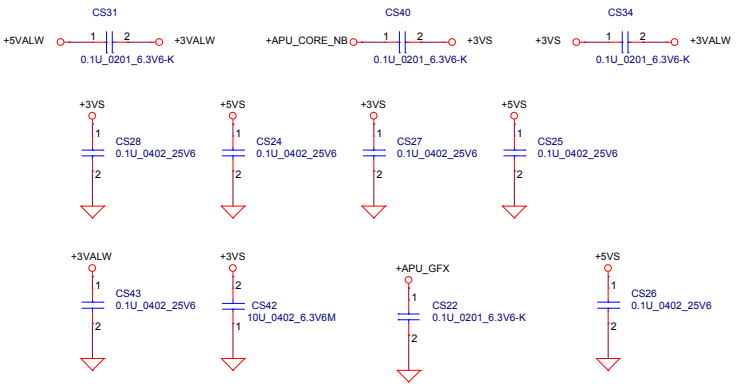
+3VALW to +3VALW_APU



For DisCharge







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: DC V TO VS INTERFACE

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 37 of 50

CPU Thermal Holex3

H1 HOLEA — pad_c6p0d4p0
H2 HOLEA — pad_c6p0d4p0
H3 HOLEA — pad_c6p0d4p0

GPU Thermal Holex2

H4 HOLEA — pad_c7p0d3p3
H5 HOLEA — pad_c7p0d3p3

Close to RJ45

H6 HOLEA — CHASSIS1_GND, pad_ct7p0b8p0d3p0

Close to Audio jack

H7 HOLEA — pad_ct7p0b8p0d3p0

PCB Fedical Mark PAD

FD1 FD2 FD3 FD4 FD5 FD6

WLAN Standoff

H10 HOLEA — pad_ct5p5d2p5
H11 HOLEA — pad_ct7p0b6p0d3p3
H12 HOLEA — pad_ct7p0d3p0
H13 HOLEA — pad_ct7p0d3p0
H15 HOLEA — pad_ct5p0d2p5
H16 HOLEA — pad_cb5p5d2p5

H17 HOLEA — pad_o2p6x2p9d2p6x2p9n
H18 HOLEA — PAD_CT7P0D3P0
H19 HOLEA — PAD_CT7P0D3P0
H20 HOLEA — pad_c3p3d3p3n

USB3.0 Shielding

SH1 ME@ — SPRING_FINGER_6.2X1.64
SH2 ME@ — SPRING_FINGER_6.2X1.64
SH3 ME@ — SPRING_FINGER_6.2X1.64
SH4 ME@ — SPRING_FINGER_6.2X1.64
SH5 ME@ — SPRING_FINGER_6.2X1.64
SH6 ME@ — SPRING_FINGER_6.2X1.64

DDR4 Shielding

SH12 ME@ — SPRING_FINGER_6.2X1.64
SH7 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH8 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH14 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH13 ME@ — SPRING_FINGER_6.2X1.64
SH9 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH10 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P
SH11 ME@ — SHIELDING_SUL-35A2M_9P2X3P3_1P

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: Hole

Size	Document Number	Rev
B	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 38 of 50

UL1 8111H@

RTL8111H-CG
SA000074W00

LAN Chip

UV1 PX@

R17M-M1-70 GPU
SA000086K00

GPU

ZZZ3 HDMI@

HDMI PN
RO00000040J

HDMI Royalty

UC2

BRISTOL FM980PADY44AB 2.7G PR 1.0
FX9800P@
SA00007RC10

UC2

BRISTOL AM970PADY44AB 2.5G PR 1.0
A129720P@
SA00008A900

UC2

BRISTOL AM960PADY44AB 2.4G PR 1.0
A109620P@
SA00008AA00

APU type

ZZZ9 DRAM_S4G@

Samsung
X7643U12002

ZZZ2 DRAM_M4G@

Micron
X7643S12002

ZZZ7 DRAM_H4G@

Hynix
X7643R12002

DRAM X76 BOM

ZZZ4 S4GX4@

Samsung
X7643P12001

ZZZ6 H4GX4@

Hynix
X7643Q12001

ZZZ10 M4GX4@

Micron
X7643T12001

ZZZ5 S8GX4@

Samsung
X7643U12001

ZZZ8 H8GX4@

Hynix
X7643R12001

ZZZ12 M8GX4@

Micron
X7643S12001

VRAM X76 BOM

UD1 MD_S8Gb@

K4A8G165WB-BCRC
SA00007TQ00

UD2 MD_S8Gb@

K4A8G165WB-BCRC
SA00007TQ00

UD3 MD_S8Gb@

K4A8G165WB-BCRC
SA00007TQ00

UD4 MD_S8Gb@

K4A8G165WB-BCRC
SA00007TQ00

RC257 MD_S8Gb@

10K_0402_5%
SD028100028J

RC265 MD_S8Gb@

10K_0402_5%
SD028100028J

DRAM_Samsung 4G

UV5 S4G_VR@

K4G41325FE-HC28
SA00007VQ10

UV6 S4G_VR@

K4G41325FE-HC28
SA00007VQ10

UV7 S4G_VR@

K4G41325FE-HC28
SA00007VQ10

UV8 S4G_VR@

K4G41325FE-HC28
SA00007VQ10

RV63 S4G_VR@

3.4K_0402_1%
SD03434018J

RV70 S4G_VR@

10K_0402_1%
SD03410028J

VRAM_Samsung 4GX4

UD1 MD_H8Gb@

H5AN8G6NAFR-UHC
SA00007X200

UD2 MD_H8Gb@

H5AN8G6NAFR-UHC
SA00007X200

UD3 MD_H8Gb@

H5AN8G6NAFR-UHC
SA00007X200

UD4 MD_H8Gb@

H5AN8G6NAFR-UHC
SA00007X200

RC258 MD_H8Gb@

2K_0402_5%
SD02820018J

RC264 MD_H8Gb@

2K_0402_5%
SD02820018J

DRAM_Hynix 4G

UV5 H4G_VR@

H5GC4H24AJR-R0C
SA000081A00

UV6 H4G_VR@

H5GC4H24AJR-R0C
SA000081A00

UV7 H4G_VR@

H5GC4H24AJR-R0C
SA000081A00

UV8 H4G_VR@

H5GC4H24AJR-R0C
SA000081A00

RV63 H4G_VR@

4.53K_0402_1%
SD03445318J

RV70 H4G_VR@

4.99K_0402_1%
SD03449918J

VRAM_Hynix 4GX4

UD1 MD_M8Gb@

MT40A512M16JY-083E:B
SA00007TS00

UD2 MD_M8Gb@

MT40A512M16JY-083E:B
SA00007TS00

UD3 MD_M8Gb@

MT40A512M16JY-083E:B
SA00007TS00

UD4 MD_M8Gb@

MT40A512M16JY-083E:B
SA00007TS00

RC258 MD_M8Gb@

2K_0402_5%
SD02820018J

RC265 MD_M8Gb@

10K_0402_5%
SD028100028J

DRAM_Micron 4G

UV5 M4G_VR@

EDW4032BABG-70-F
SA000081800

UV6 M4G_VR@

EDW4032BABG-70-F
SA000081800

UV7 M4G_VR@

EDW4032BABG-70-F
SA000081800

UV8 M4G_VR@

EDW4032BABG-70-F
SA000081800

RV63 M4G_VR@

4.75K_0402_1%
SD03447518J

VRAM_Micron 4GX4

ZZZ1 REDRV@

PCB PN
DA600013G00

PCB_MB with redriver

ZZZ13 NOREDRV@

PCB PN
DA600013F00

PCB_MB without redriver

UV5 S8G_VR@

K4G80325FB-HC28
SA000081C00

UV6 S8G_VR@

K4G80325FB-HC28
SA000081C00

UV7 S8G_VR@

K4G80325FB-HC28
SA000081C00

UV8 S8G_VR@

K4G80325FB-HC28
SA000081C00

RV63 S8G_VR@

8.45K_0402_1%
SD000011R00

RV70 S8G_VR@

2K_0402_1%
SD03420018J

VRAM_Samsung 8GX4

UV5 H8G_VR@

H5GC8H24MJR-R0C
SA000081600

UV6 H8G_VR@

H5GC8H24MJR-R0C
SA000081600

UV7 H8G_VR@

H5GC8H24MJR-R0C
SA000081600

UV8 H8G_VR@

H5GC8H24MJR-R0C
SA000081600

RV70 H8G_VR@

4.75K_0402_1%
SD03447518J

VRAM_Hynix 8GX4

UV5 M8G_VR@

MT51J256M32HF-70:A
SA000081700

UV6 M8G_VR@

MT51J256M32HF-70:A
SA000081700

UV7 M8G_VR@

MT51J256M32HF-70:A
SA000081700

UV8 M8G_VR@

MT51J256M32HF-70:A
SA000081700

RV63 M8G_VR@

4.53K_0402_1%
SD03445318J

RV70 M8G_VR@

2K_0402_1%
SD03420018J

VRAM_Micron 8GX4

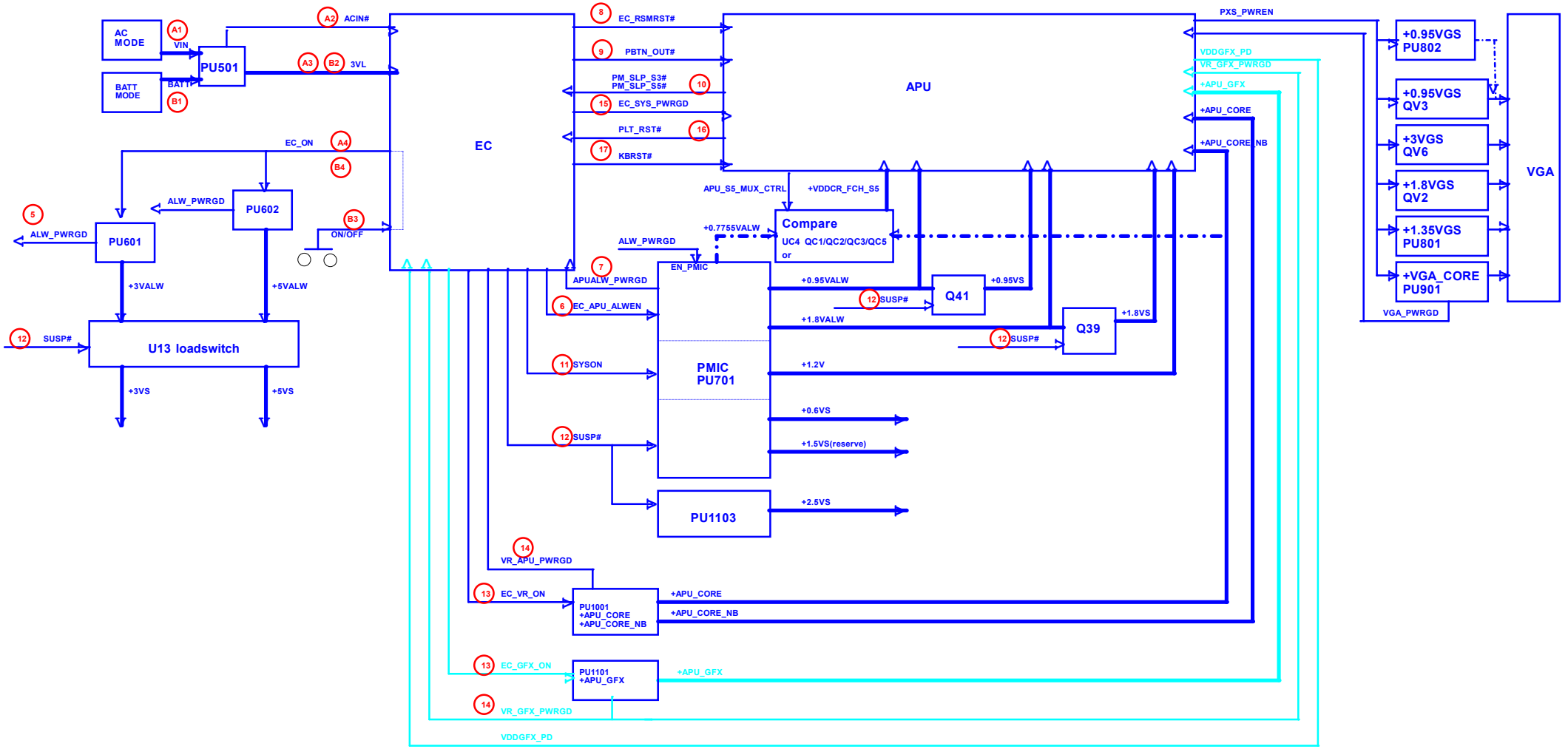
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ***Virtual symbol***

LCFC

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 39 of 50

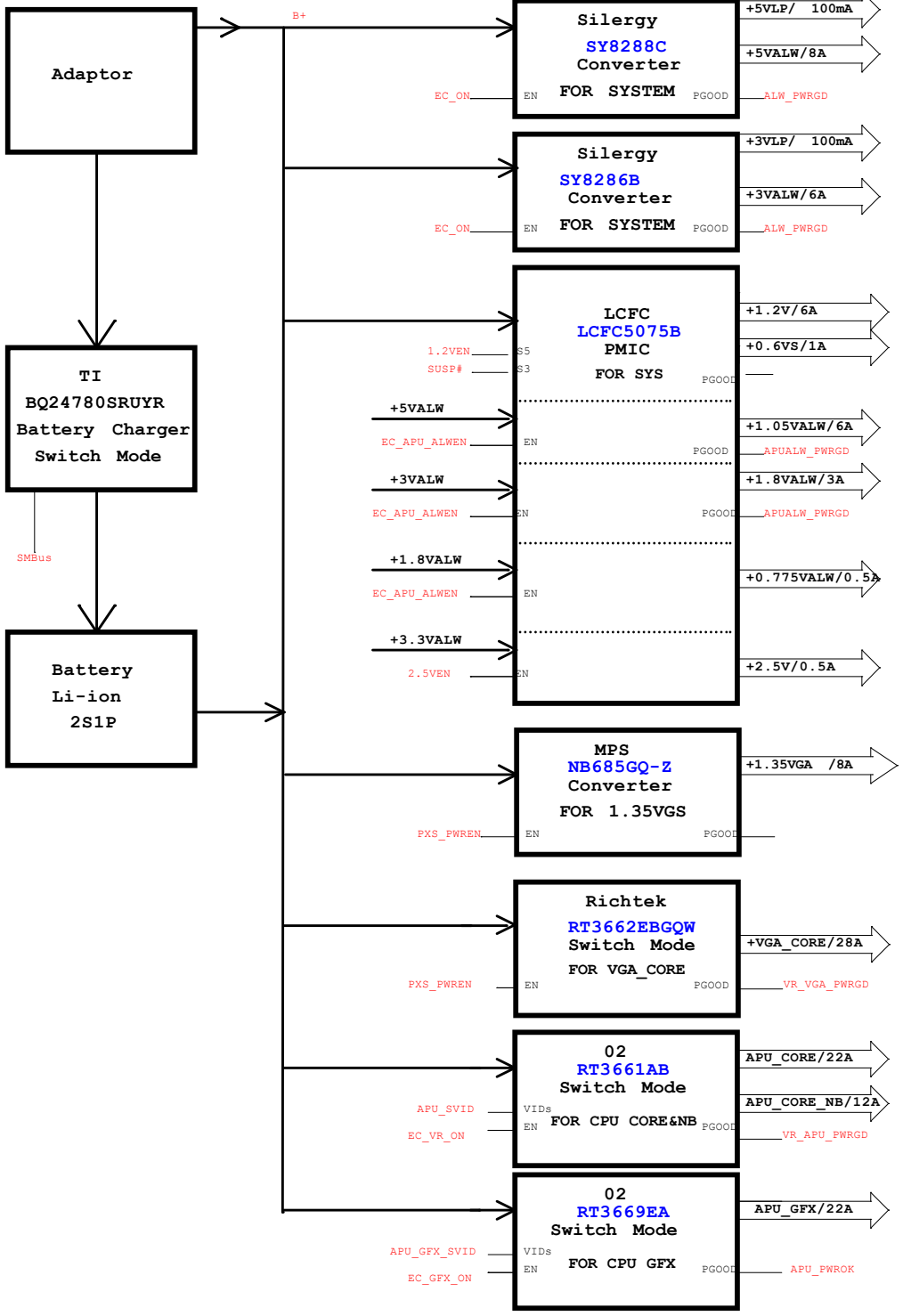


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: *Power sequence Block*

Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 40 of 50



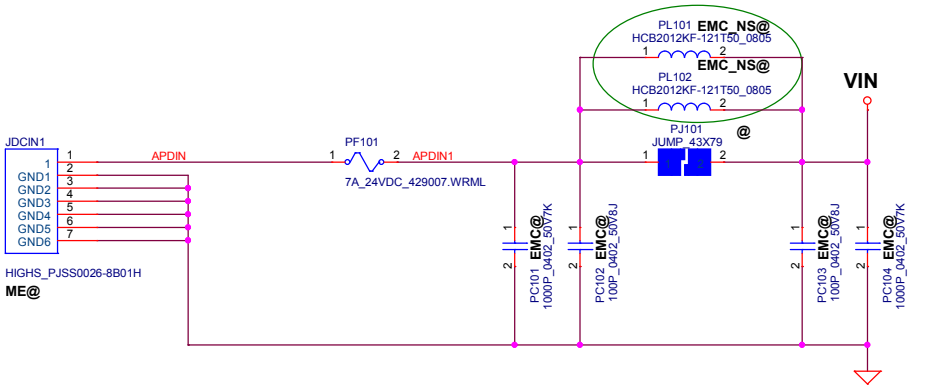
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

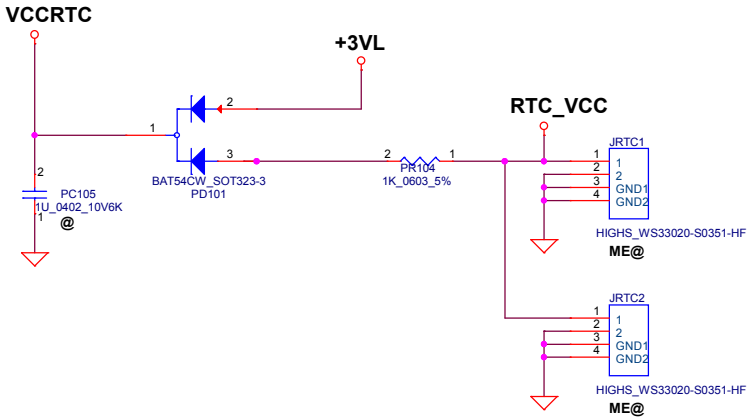
Title: **Power Diagram**

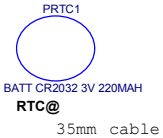
Size	Document Number	Rev
Custom	320ABR	0.1

Date: Thursday, January 12, 2017 Sheet 41 of 50

Cost down PL101,PL102 if EMC test pass







35mm cable

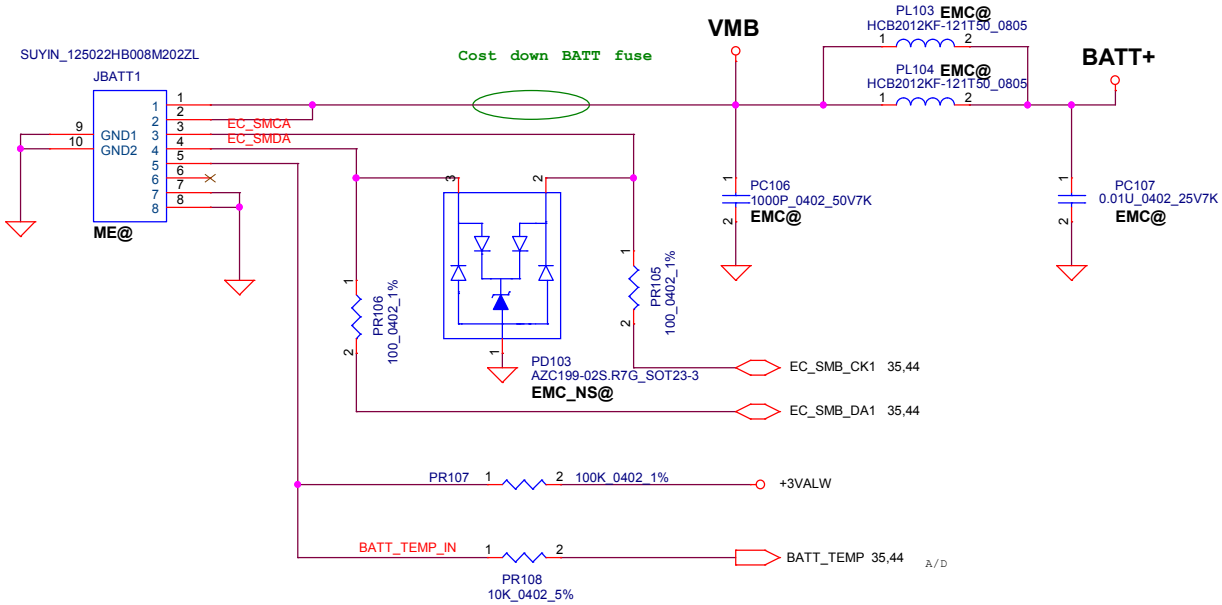
RTC Battery for GCM BOM
(2nd source and quoted price)

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: DCIN / RTC

Size	Document Number	Rev
Custom	320ABR	0.1

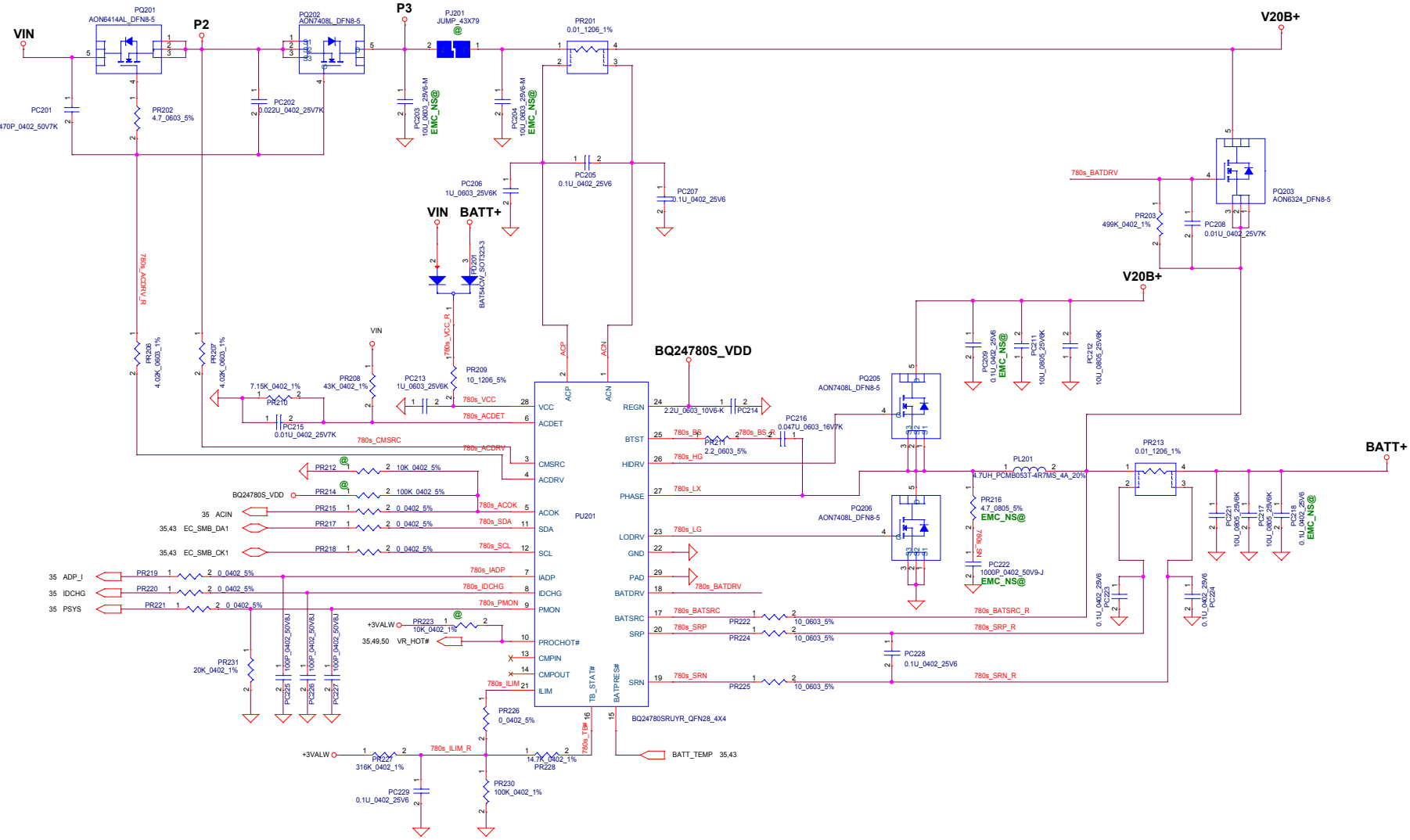
Date: Thursday, January 12, 2017 Sheet 42 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: ***BATTERY CONN/OTP***

Size	Document Number	Rev
B	320ABR	0.1
Date: Thursday, January 12, 2017	Sheet 43 of 50	



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Issued Date	2013/08/08	Deciphered Date	2013/08/05

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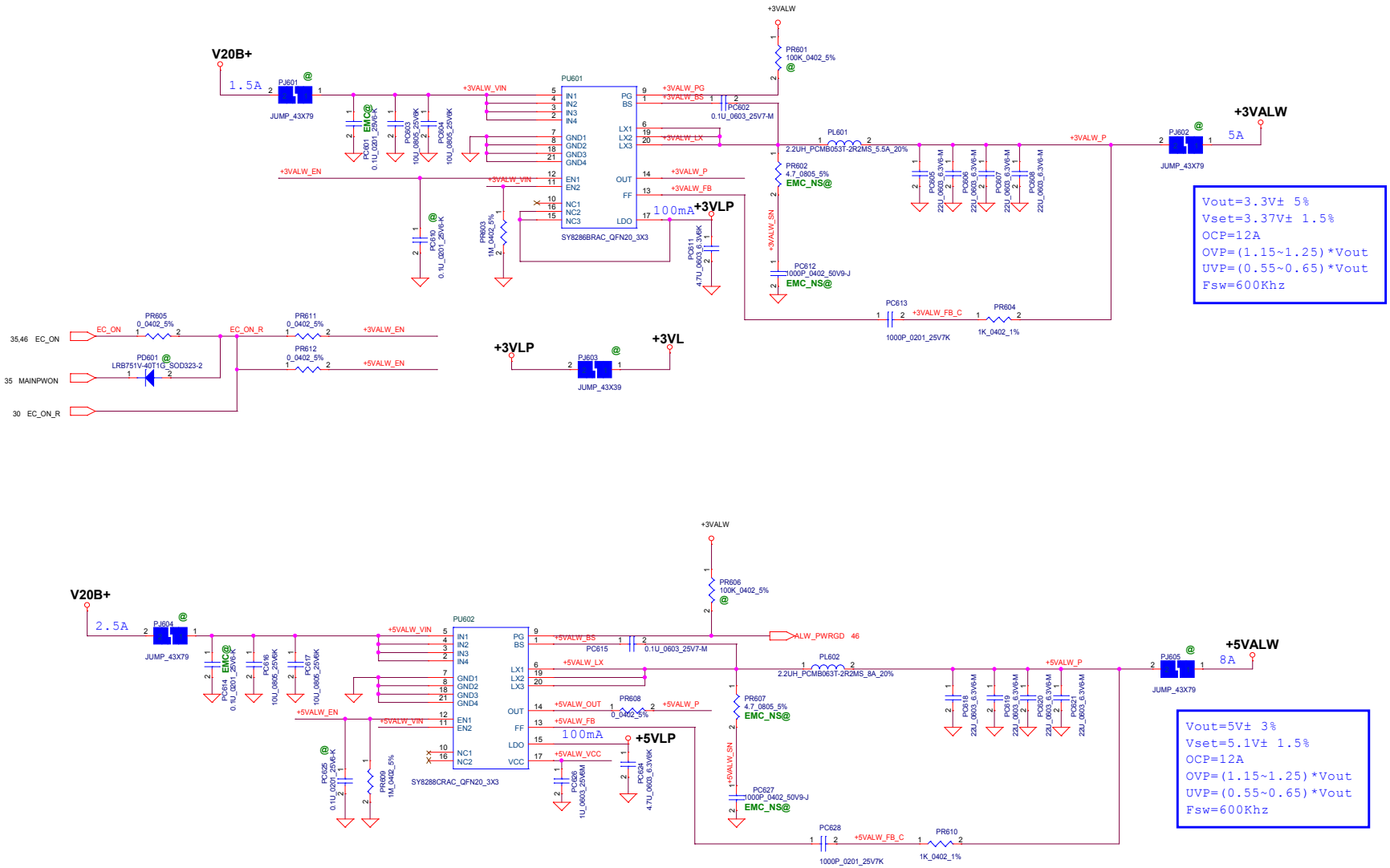
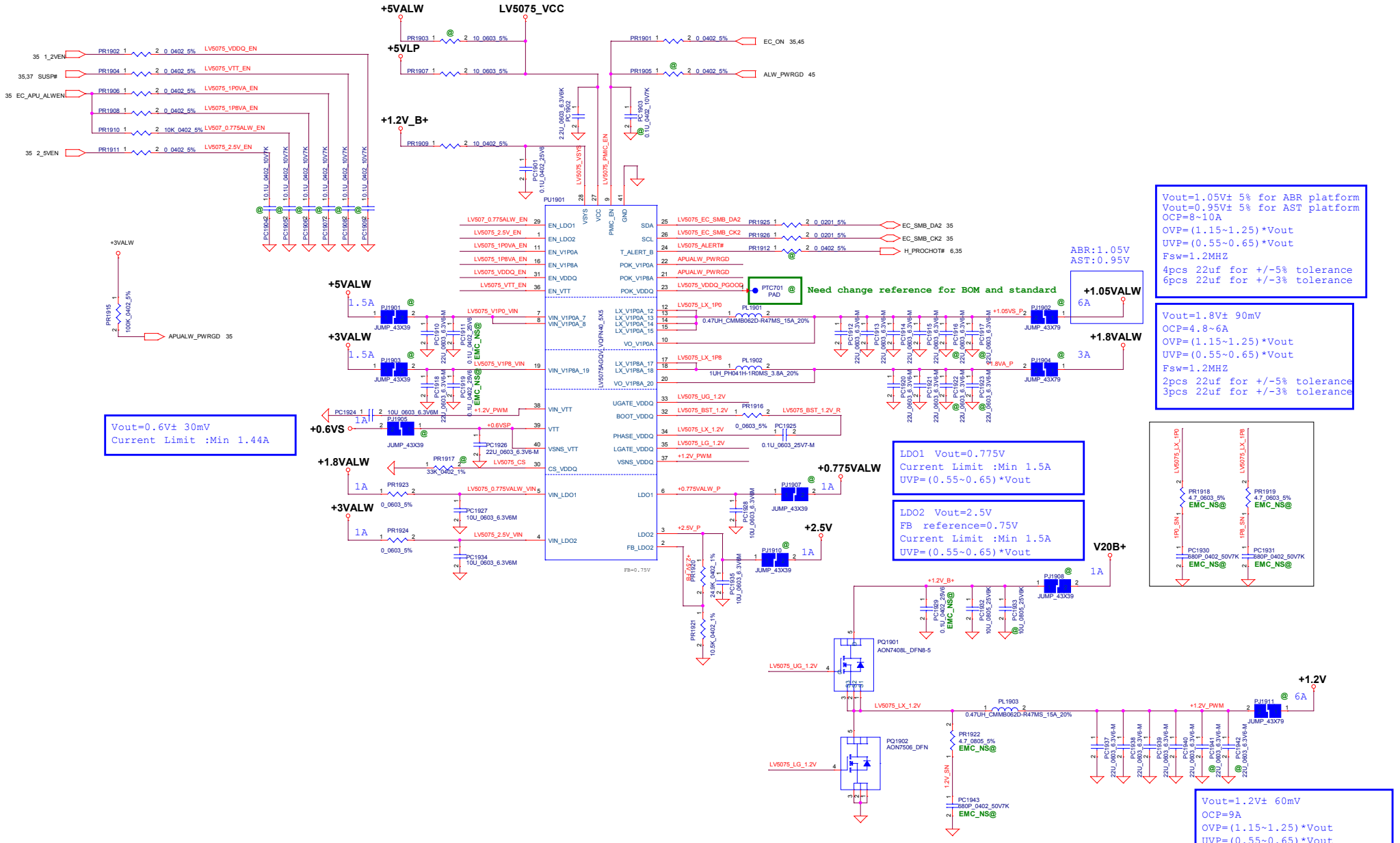
Title	CHARGER	
Size	Document Number	Rev
C	320ABR	0.1
Date:	Thursday, January 12, 2017	Sheet 44 of 50



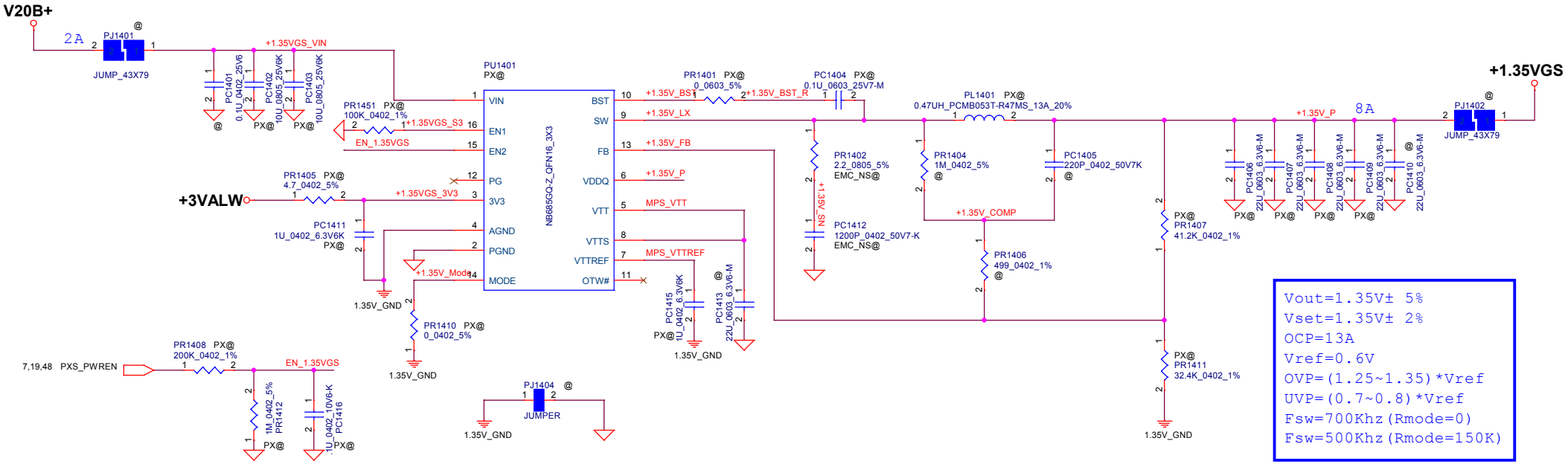
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	320ABR		0.1
Date:	Thursday, January 12, 2017	Sheet	45 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2014/02/20	Deciphered Date	2014/02/20

Title	System PMIC		
Size	Document Number		Rev
A2	320ABR		0.1
Date:	Thursday, January 12, 2017	Sheet	46 of 50

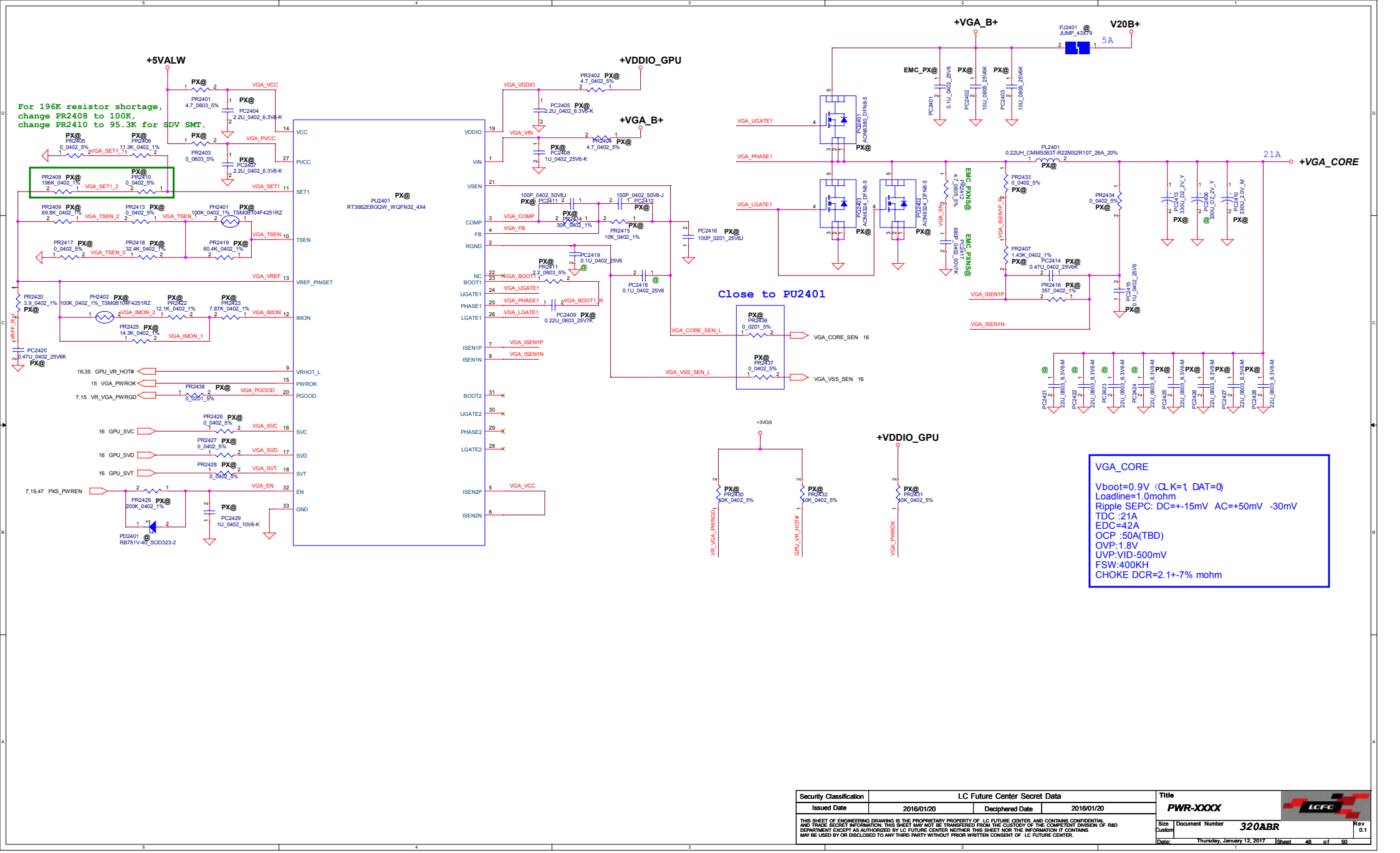


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: *1.35VGS*

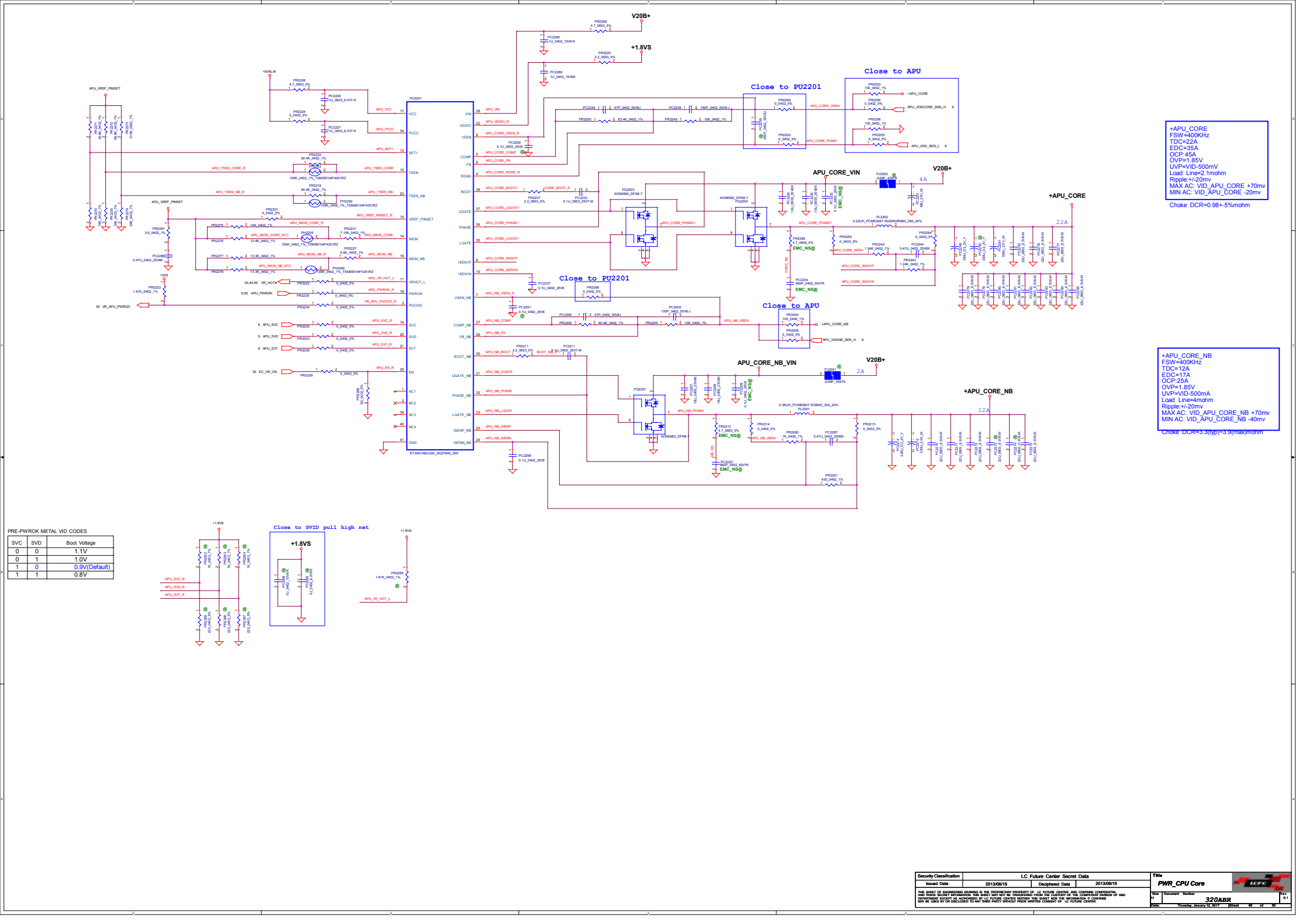
Size	Document Number	Rev
A3	*320ABR*	0.1

Date: Thursday, January 12, 2017 Sheet 47 of 50



Security Classification	LC Future Center Secret Data		
Issued Date	2016/01/20	Deciphered Date	2016/01/20

Title	PWR-XXXX		
Size: Custom	Document Number: 320ABR		Rev: 0.1
Date: Thursday, January 12, 2017	Sheet 48 of 50		

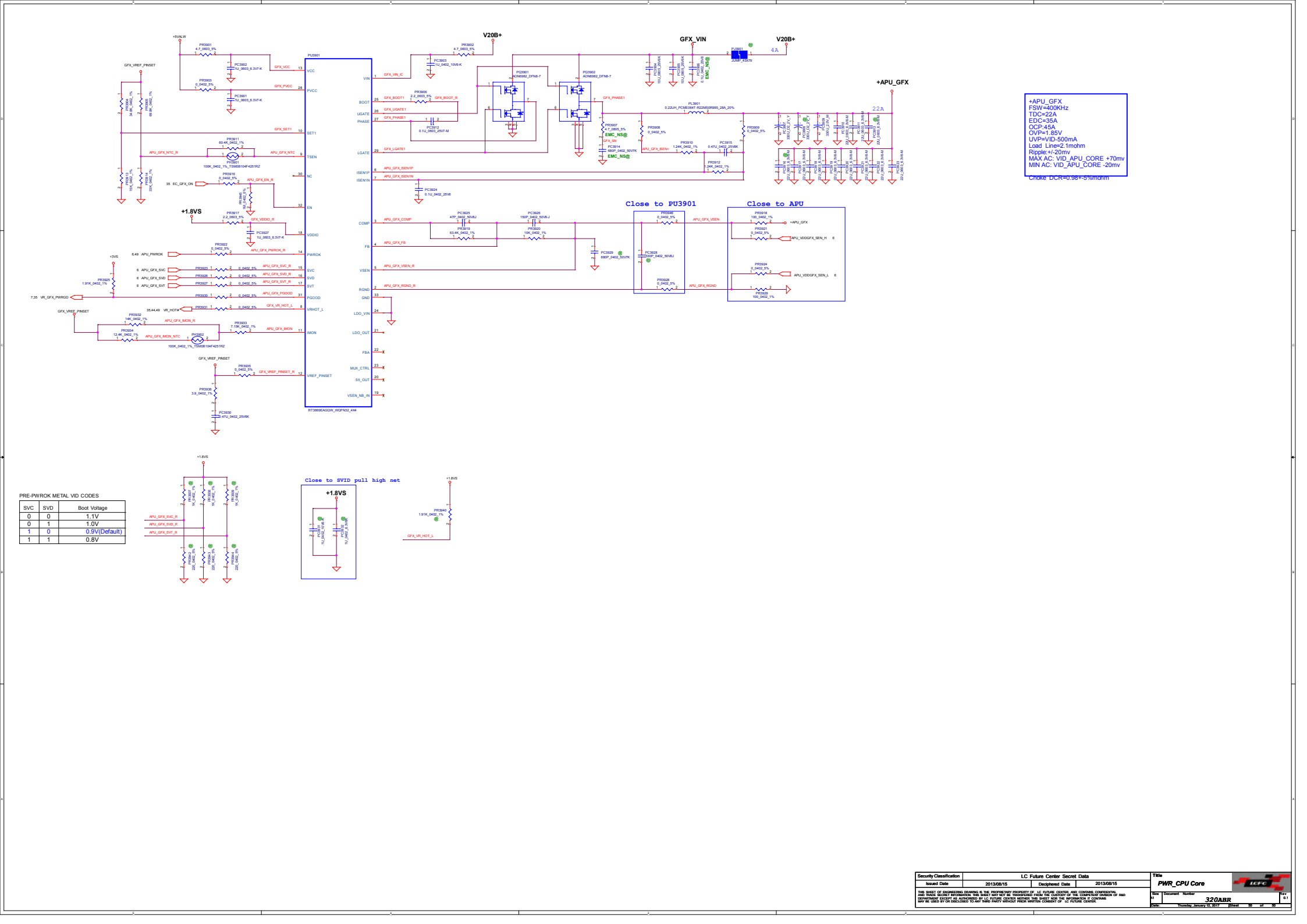


PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title	PWR_CPU Core		
Size: A1	Document Number: 320ABR		Rev: 0.1
Date: Thursday, January 02, 2014	Sheet 49 of 55		


+APU_GFX
FSW=400KHz
TDC=22A
EDC=35A
OCP:45A
OVP=1.85V
UVP=VID-500mA
Load Line=2.1mohm
Ripple:+/-20mv
MAX AC: VID_APU_CORE +70mv
MIN AC: VID_APU_CORE -20mv
Choke DCR=0.984+-5%mohm
Close to PU3901
Close to APU
Close to SVID pull high net
PRE-PWROK METAL VID CODES
SVC SVD Boot Voltage
0 0 1.1V
0 1 1.0V
1 0 0.9V(Default)
1 1 0.8V
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/15
Deciphered Date
2013/08/15
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Title
PWR_CPU Core
Size
A1
Document Number
320ABR
Rev
0.1
Date:
Thursday, January 02, 2014
Sheet
30
of
55