LCFC Confidential

Customer Product name
E14 Gen4 Intel/E15 Gen4 Intel

Project Code:
JE442/JE542

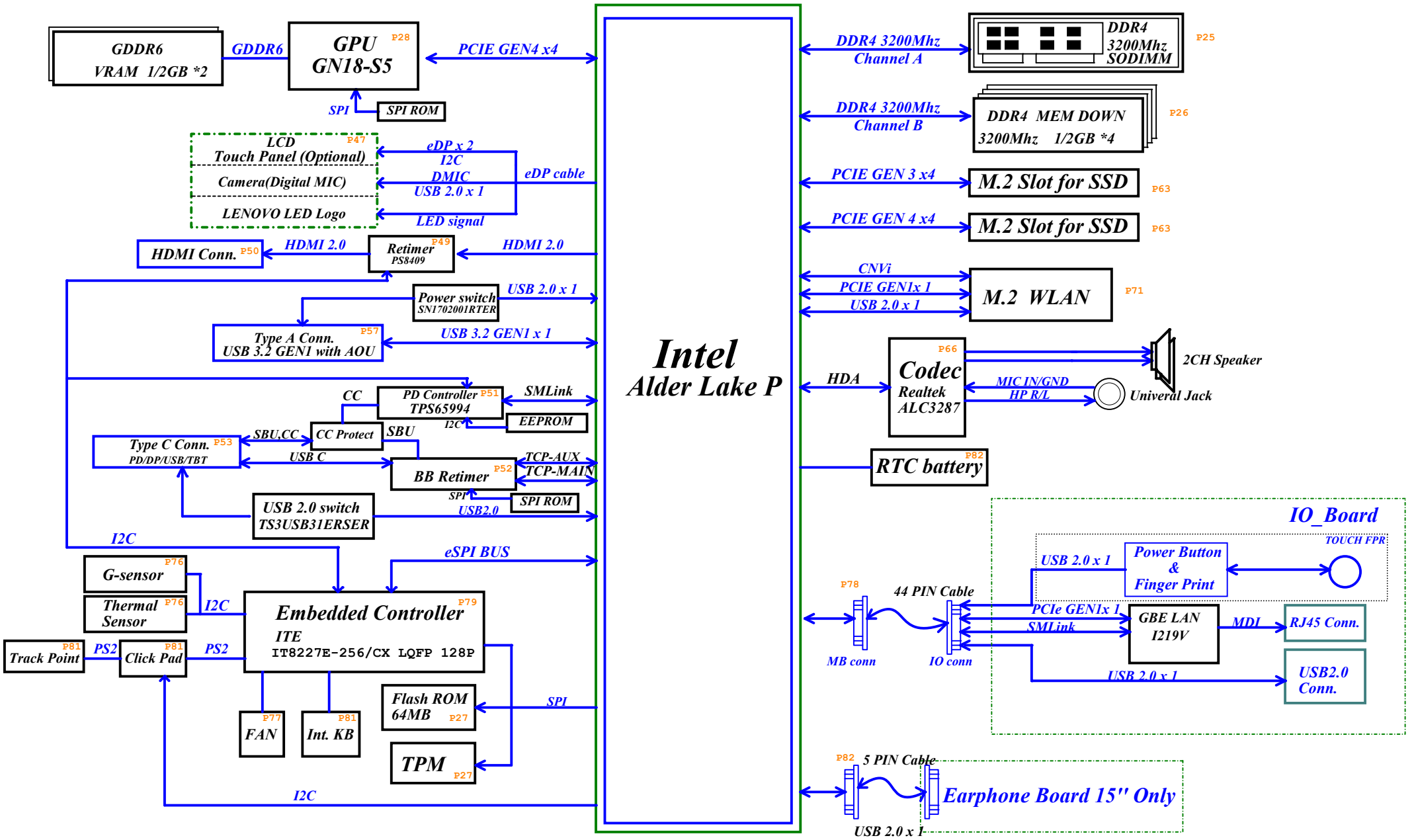
Board Number:
NM-E211

Customer Project name:
Mercury/Mars3.0

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: COVER PAGE

Size: Custom	Document Number: E14/E15 NM-E211	Rev: 0.1
Date: Wednesday, March 02, 2022	Sheet 1 of 108	



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

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Title: BLOCK DIAGRAM

Size: Document Number: E14/E15 NM-E211 Rev: 0.1

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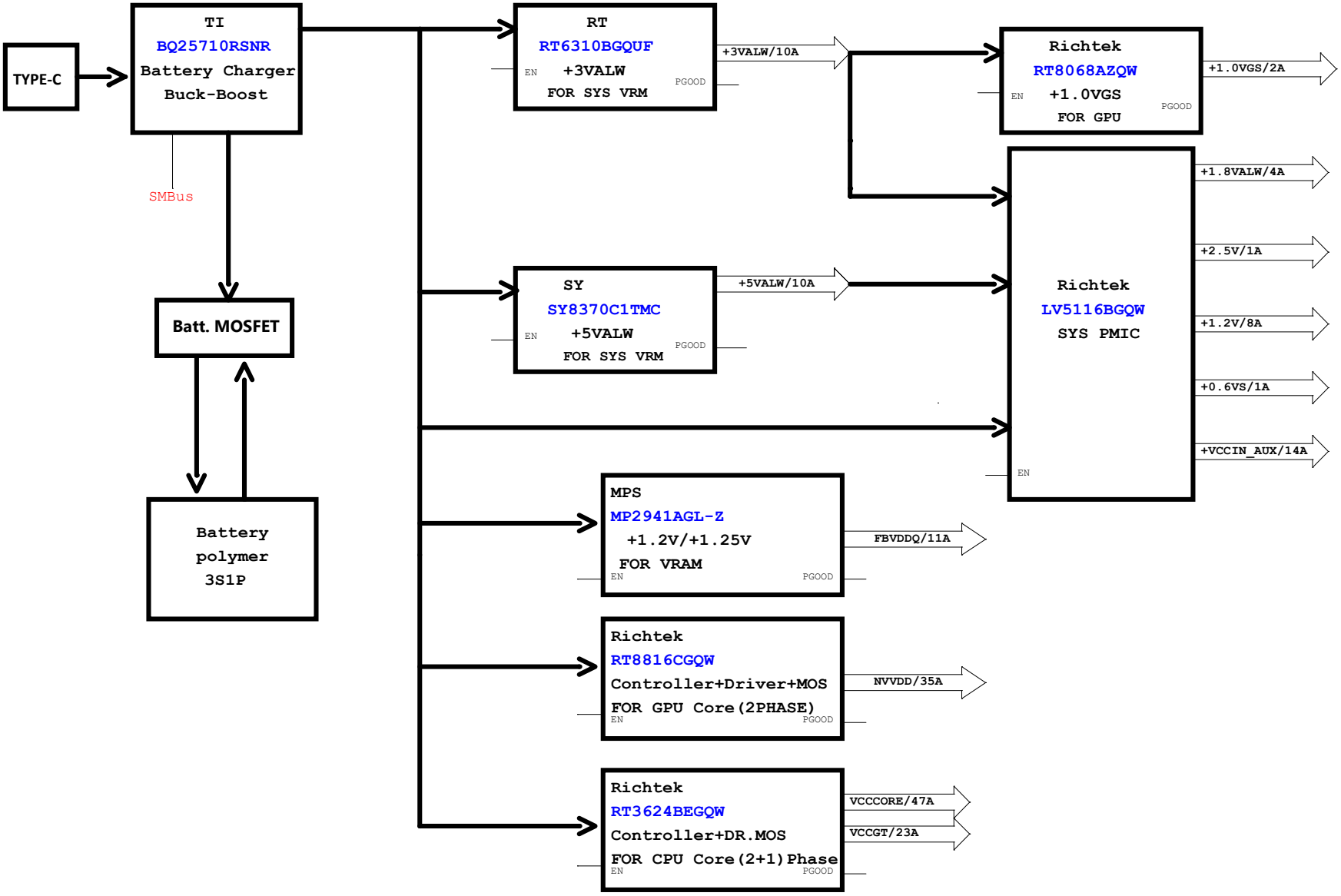

<Variant Name>

Security Classification	LC Future Center Secret Data		
Issued Date		Deciphered Date	

Title: *Power Block Diagram*

Size	Document Number	Rev
C	E14/E15 NM-D011	0.1

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V9B+ +3VL +5VL	+5VALW +3VALW	+3VALW_PCH +1.8VALW	1.2V +VCCST_CPU	+5VS +3VS +1.8VS
S0	O	O	O	O	O
S0Ix	O	O	O	O	O
S4/S5 DC	O	O	O	X	X
S4/S5 DEEP SLEEP	O	O	X	X	X
S4/S5 AC	O	O	O	X	X
S4/S5 AC ONLY	O	O	O	X	X

HSIO Matrix

HSIO PORT		Function
USB2.0	1	TYPE-C TBT4
	2	EARPHONE
	3	IOB USB
	4	NC
	5	NC
	6	FINGER PRINTER
	7	Camera
	8	NC
	9	USB3.2 AOU
	10	WLAN
USB3.0	1	USB3.2 AOU Port
	2	NC
	3	NC
	4	NC
PCH PCIE3	5	NC
	6	WLAN
	7	NC
	8	LAN
	9	SSD1
	10	
	11	
	12	
CPU PCIE4-A	0	SSD2
	1	
	2	
	3	
CPU PCIE4-B	0	GPU
	1	
	2	
	3	
CPU PCIE5	0-3	NC
	4-7	
CPU DDI	A	eDP
	B	HDMI
CPU TCP	0	TYPE-C TBT4
	1	NC
	2	NC
	3	NC

SMBUS Control Table

EC SMBus1 address

Device	Address
GPU(GN18-S5)	1001_110
G-Sensor(LIS2DWLTR)	0011_000
Thermal Sensor(F75303M)	1001_101
Thermal Sensor(NCT7718)	1001_100
Battery	0001_011
Charger	0001_001

EC SMBus4 address

Device	Address
PD	TBD
HDMI Retimer	0x10-0x2F
PMIC	0x34

PCH SMB address

Device	Address
SO-DIMM	1010_000
Click Pad	TBD

PCH SML0 address

Device	Address
BB Re-timer	0X56
LAN	0XC8

PCH SML1 address

Device	Address
PD	0X23/27

CPU I2C2 address

Device	Address
Touch Panel	TBD

Title: DDR4 SUB CHANNEL-A

Size: Custom | Document Number: E14/E15 NM-E211 | Rev: 0.1

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GPU

GN18-S5

OPT_GN18S@

UG11

S IC GN18-S5-A1 BGA 771P GPU MP 01 !

SA0000C7B40

GN20-S5

OPT_GN20S@

UG11

S IC GN20-S5-A1 BGA 771P GPU MP 01 !

SA0000C7C50

VRAM PN	RAMCFG[2:0] STRAP 2	STRAP 1	STRAP 1	STRAP 0	
V2G_SAM@ UG15 S IC D6 8G/1750 K4Z80325BC-HC14 FBGA 01! SA00009L410 V2G_SAM@ UG16 S IC D6 8G/1750 K4Z80325BC-HC14 FBGA 01! SA00009L410	V2G_SAM@ RG3106 S RES 1/20W 100K +-5% 0201 SD0431003YT	V2G_SAM@ RG3105 S RES 1/20W 100K +-5% 0201 SD0431003YT		V2G_SAM@ RG3104 S RES 1/20W 100K +-5% 0201 SD0431003YT	Samsung 8Gb(0x0)
V2G_HYX0@ UG15 S IC D6 256MX32 H56C8H24AIR-S2C 01 ! SA0000B4E00 V2G_HYX0@ UG16 S IC D6 256MX32 H56C8H24AIR-S2C 01 ! SA0000B4E00	V2G_HYX0@ RG3106 S RES 1/20W 100K +-5% 0201 SD0431003YT	V2G_HYX0@ RG3102 S RES 1/20W 100K +-5% 0201 SD0431003YT		V2G_HYX0@ RG3104 S RES 1/20W 100K +-5% 0201 SD0431003YT	Hynix 8Gb(0x2)
V2G_HYX1@ UG15 S IC D6 256MX32 H56G32CS4DX005 FBGA 01! SA0000C8K00 V2G_HYX1@ UG16 S IC D6 256MX32 H56G32CS4DX005 FBGA 01! SA0000C8K00	V2G_HYX1@ RG3103 S RES 1/20W 100K +-5% 0201 SD0431003YT	V2G_HYX1@ RG3105 S RES 1/20W 100K +-5% 0201 SD0431003YT		V2G_HYX1@ RG3101 S RES 1/20W 100K +-5% 0201 SD0431003YT	Hynix 8Gb(0x5)
V4G_SAM@ UG15 S IC D6 16G/1750 K4ZAF325BM-HC14 01 ! SA00009QV20 V4G_SAM@ UG16 S IC D6 16G/1750 K4ZAF325BM-HC14 01 ! SA00009QV20	V4G_SAM@ RG3106 S RES 1/20W 100K +-5% 0201 SD0431003YT	V4G_SAM@ RG3105 S RES 1/20W 100K +-5% 0201 SD0431003YT	V4G_SAM@ RG3102 S RES 1/20W 100K +-5% 0201 SD0431003YT	V4G_SAM@ RG3104 S RES 1/20W 100K +-5% 0201 SD0431003YT	Samsung 16Gb(0x9)
V4G_MIC@ UG15 S IC D6 4GB MT61K512M32KPA-14 :C MP 01 ! SA0000C0940 V4G_MIC@ UG16 S IC D6 4GB MT61K512M32KPA-14 :C MP 01 ! SA0000C0940	V4G_MIC@ RG3103 S RES 1/20W 100K +-5% 0201 SD0431003YT	V4G_MIC@ RG3102 S RES 1/20W 100K +-5% 0201 SD0431003YT		V4G_MIC@ RG3101 S RES 1/20W 100K +-5% 0201 SD0431003YT	Micron 16Gb(0x7)
V4G_HYX@ UG15 S IC D6 16G H56G42AS2DX014N BGA MP 01 ! SA0000CMU10 V4G_HYX@ UG16 S IC D6 16G H56G42AS2DX014N BGA MP 01 ! SA0000CMU10	V4G_HYX@ RG3106 S RES 1/20W 100K +-5% 0201 SD0431003YT	V4G_HYX@ RG3105 S RES 1/20W 100K +-5% 0201 SD0431003YT		V4G_HYX@ RG3104 S RES 1/20W 100K +-5% 0201 SD0431003YT V4G_HYX@ RG3101 S RES 1/20W 100K +-5% 0201 SD0431003YT	Hynix 16Gb(0x8)

X76

X76_V2G_SAM@ ZZZ9 ALT. GROUP PARTS SAMSUNG V2G JE442 X764EU01004

X76_V2G_HYX0@ ZZZ8 ALT. GROUP PARTS HYNIX V2G JE442 X764EU01005

X76_V2G_HYX1@ ZZZ11 ALT. GROUP PARTS HYNIX2 V2G JE442 X764EU0100A

X76_V4G_SAM@ ZZZ10 ALT. GROUP PARTS SAMSUNG V4G JE442 X764EU01009

X76_V4G_MIC@ ZZZ13 ALT. GROUP PARTS MICRON V4G JE442 X764EU0100B

X76_V4G_HYX@ ZZZ12 ALT. GROUP PARTS HYNIX V4G JE442 X764EU0100C

OPT_GN20S@

UG12

S IC FL 16M W25Q16JWSNIQ SOIC 8P

SA0000AU500

Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title: Cover Page

Size	Document Number	Rev
C	E14/E15 NM-E211	0.1

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Virtual Symbol_EE

PCB

PANEL_E14@ — ZZZ1 — PCB JE442 NM-E211 NS-E211 — DAZ2E700100

PANEL_E15@ — ZZZ1 — PCB JE542 NM-E211 NS-E212/E213 — DAZ2E600100

PCB_E14@ — ZZZ — PCB JE442 NM-E211 REV1 M/B — DA80001AQ10

PCB_E14@ — ZZZ — PCB JE442 NS-E211 REV1 IO/B — DA80001AS10

PCB_E15@ — ZZZ — PCB JE542 NM-E211 REV1 M/B — DA80001AR10

PCB_E15@ — ZZZ — PCB JE542 NS-E212 REV1 IO/B — DA80001AT10

PCB_E15@ — ZZZ — PCB JE542 NS-E213 REV1 EARPHONE/B — DA80001AU10

CPU

U28_I7_SQS@ — UC1 — S IC FJ80715047866O7 SRLD6 L0 2.1G 01 ! — SA0000D0P10

U28_I5_SQS@ — UC1 — S IC FJ80715047879O7 SRLD9 L0 1.7G 01 ! — SA0000D0Q10

U15_I7@ — UC1 — S IC FJ80715048266O7 SRLFP R0 1.7G 01 ! — SA0000D2130

U15_I5@ — UC1 — S IC FJ80715048268O2 SRLFQ R0 1.3G 01 ! — SA0000D1S40

U15_I5S@ — UC1 — S IC FJ80715048268O3 SRLFR R0 1.3G 01 ! — SA0000D2P20

U15_I3@ — UC1 — S IC FJ80715048271O0 SRLFT R0 1.2G 01 ! — SA0000D2S30

U15_I3S@ — UC1 — S IC FJ80715048271O1 SRLFU R0 1.2G 01 ! — SA0000D2T20

DRAM /Board ID

BOARD ID:6,5

D8G_SAM@ UD1 — S IC D4 1GX16/3200 K4AAG165WB-BCWE 01 ! — SA0000C6N00	D8G_SAM@ UD2 — S IC D4 1GX16/3200 K4AAG165WB-BCWE 01 ! — SA0000C6N00	D8G_SAM@ UD3 — S IC D4 1GX16/3200 K4AAG165WB-BCWE 01 ! — SA0000C6N00	D8G_SAM@ UD4 — S IC D4 1GX16/3200 K4AAG165WB-BCWE 01 ! — SA0000C6N00	D8G_SAM@ RC4229 — S RES 1/20W 10K +-5% 0201 — SD0431002YT	D8G_SAM@ RC4221 — S RES 1/20W 10K +-5% 0201 — SD0431002YT
D8G_HYX@ UD1 — S IC D4 16G/3200 H5ANAG6NCJR-XNC 96P 01! — SA0000B5K00	D8G_HYX@ UD2 — S IC D4 16G/3200 H5ANAG6NCJR-XNC 96P 01! — SA0000B5K00	D8G_HYX@ UD3 — S IC D4 16G/3200 H5ANAG6NCJR-XNC 96P 01! — SA0000B5K00	D8G_HYX@ UD4 — S IC D4 16G/3200 H5ANAG6NCJR-XNC 96P 01! — SA0000B5K00	D8G_HYX@ RC4222 — S RES 1/20W 10K +-5% 0201 — SD0431002YT	D8G_HYX@ RC4228 — S RES 1/20W 10K +-5% 0201 — SD0431002YT
D8G_MIC@ UD1 — S IC D4 16GB/3200 MT40A1G16RC-062E:B 01! — SA0000A4K10	D8G_MIC@ UD2 — S IC D4 16GB/3200 MT40A1G16RC-062E:B 01! — SA0000A4K10	D8G_MIC@ UD3 — S IC D4 16GB/3200 MT40A1G16RC-062E:B 01! — SA0000A4K10	D8G_MIC@ UD4 — S IC D4 16GB/3200 MT40A1G16RC-062E:B 01! — SA0000A4K10	D8G_MIC@ RC4229 — S RES 1/20W 10K +-5% 0201 — SD0431002YT	D8G_MIC@ RC4228 — S RES 1/20W 10K +-5% 0201 — SD0431002YT
D8G_KSN@ UD1 — S IC D4 16G/3200 MT40A1G16RC-062E:B 01 ! — SA0000A4K30	D8G_KSN@ UD2 — S IC D4 16G/3200 MT40A1G16RC-062E:B 01 ! — SA0000A4K30	D8G_KSN@ UD3 — S IC D4 16G/3200 MT40A1G16RC-062E:B 01 ! — SA0000A4K30	D8G_KSN@ UD4 — S IC D4 16G/3200 MT40A1G16RC-062E:B 01 ! — SA0000A4K30	D8G_KSN@ RC4229 — S RES 1/20W 10K +-5% 0201 — SD0431002YT	D8G_KSN@ RC4228 — S RES 1/20W 10K +-5% 0201 — SD0431002YT

X76

X76_D8G_MIC@ — ZZZ2 — ALT_GROUP PARTS MICRON D8G JE442 — X764EU01001

X76_D8G_HYX@ — ZZZ2 — ALT_GROUP PARTS HYNIX D8G JE442 — X764EU01002

X76_D8G_SAM@ — ZZZ2 — ALT_GROUP PARTS SAMSUNG D8G JE442 — X764EU01003

X76_D8G_KSN@ — ZZZ2 — ALT_GROUP PARTS D8G KINGSTON JE442 — X764EU0100D

BOM Structure

BOM Structure	Description
@	Not stuff
PCB@	For PCB part
ME@	For ME part
EMC@	For EMC part
EMC_NS@	For EMC not stuff part
RF@	For RF part
RF_NS@	For RF not stuff part
FPR@	For Finger Print
NON-FPR@	For Non Finger Print
TPM@	For TPM
NON-TPM@	For Non TPM
U28_I7@	For U28 I7 CPU
U28_I5@	For U28 I5 CPU
U15_I7@	For U15 I7 CPU
U15_I5@	For U15 I5 CPU
U15_I5S@	For U15 I5S CPU
U15_I3@	For U15 I3 CPU
U15_I3S@	For U15 I3S CPU
D8G_MIC@	For 16Gb Micron Memory X76
D8G_HYX@	For 16Gb Hynix Memory X76
D8G_SAM@	For 16Gb Samsung Memory X76
UMA@	For UMA part
OPT@	For GPU part
OPT_NS@	For GPU not Stuff part
OPT_EMC@	For GPU EMC part
OPT_RF@	For GPU RF part
OPT_RF_NS@	For GPU RF not stuff part
OPT_GN18S@	For GN18-S5 part
OPT_GN18S_NS@	For GN18-S5 not stuff part
OPT_GN20S@	For GN20-S5 part
OPT_GN20S_NS@	For GN20-S5 not stuff part
V4G_SAM@	For 4G Samsung VRAM X76
V2G_SAM@	For 2G Samsung VRAM X76
V2G_HYX0@	For 2G Hynix VRAM X76
OPT_RT8816@	For GPU Power
OPT_RT8816NS@	For GPU Power
OPT_UP1666@	For GPU Power
OPT_UPI1666@	For GPU Power
OPT_UPI1666NS@	For GPU Power
OPT_US5650@	For GPU Power
OPT_NCP45492@	For GPU Power
U15@	For U15 CPU Power
U28@	For U28 CPU Power

memory down SPD

Vender	Capacity	Types	Board ID[6:5]
Samsung	16Gb	1R*SDP*16Gb	01
Hynix	16Gb	1R*SDP*16Gb	10
Micron	16Gb	1R*SDP*16Gb	00

Title: BLOCK DIAGRAM

LCFC

Size	Document Number	Rev
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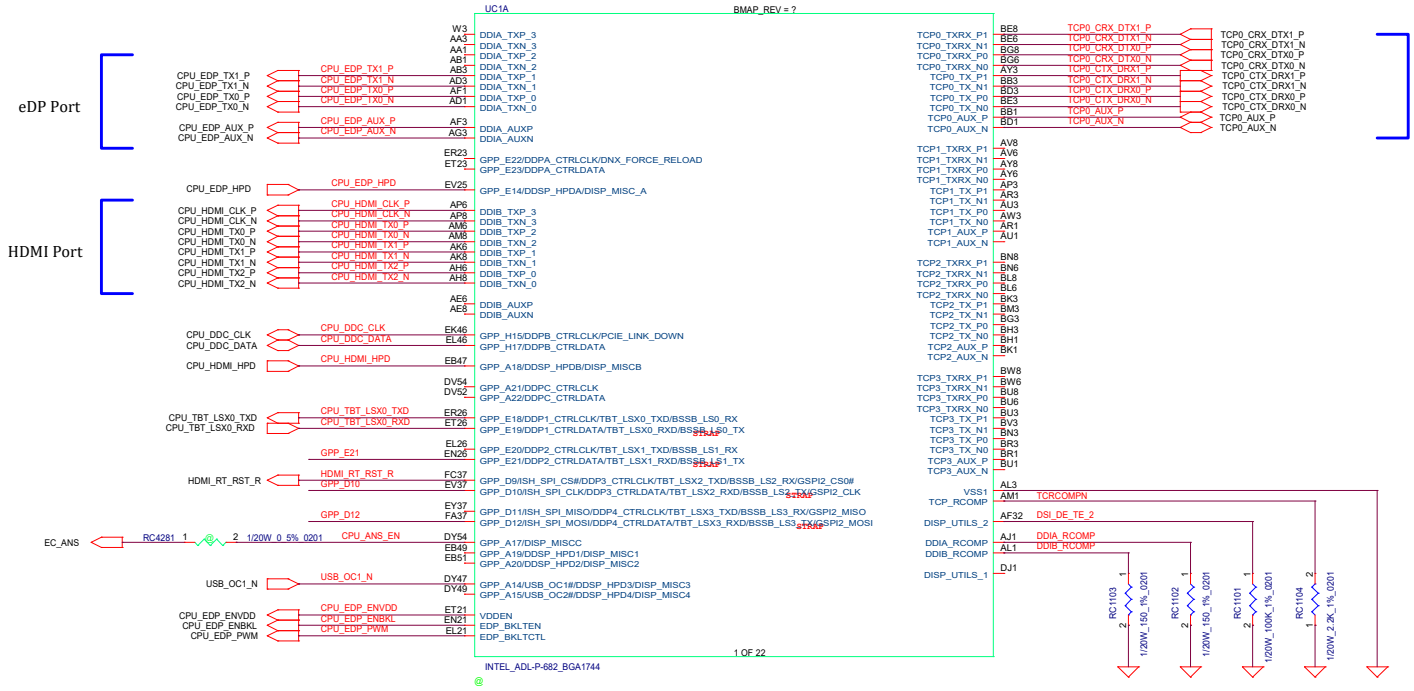

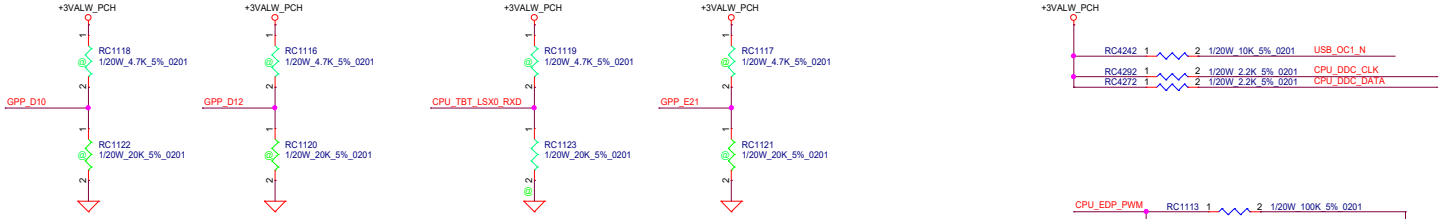

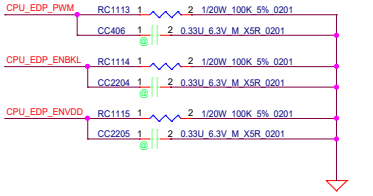

GPP_D10:
Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP3_I2C / TBT_LSX2 / BBSB_LS2 pins at 1.8V
1 = DDP3_I2C / TBT_LSX2 / BBSB_LS2 pins at 3.3V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

GPP_D12:
Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP4_I2C / TBT_LSX3 / BBSB_LS3 pins at 1.8V
1 = DDP4_I2C / TBT_LSX3 / BBSB_LS3 pins at 3.3V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

GPP_E19(CPU_TBT_LSX0_RXD):
DDP2 I2C /TBT_LSX1 /BBSB_LS1 pins VCC configuration
Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP1 I2C / TBT_LSX0 / BBSB_LS0 pins at 1.8V
1 = DDP1 I2C / TBT_LSX0 / BBSB_LS0 pins at 3.3V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

GPP_E21 :
DDP2 I2C /TBT_LSX1 /BBSB_LS1 pins VCC configuration
Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
0 = DDP2 I2C / TBT_LSX1 / BBSB_LS1 pins at 1.8V
1 = DDP2 I2C / TBT_LSX1 / BBSB_LS1 pins at 3.3V
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: X60-TGL-H

LCFC

Size	Document Number	Rev
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DDRA_DQ[63:0]

?
?

UC1B

BMAP_REV = ?

(DDR4(IL) / DDR4(NIL) / DDR5(NIL) / LP4x-LP5(NIL))

Byte0[0~7]

DDRA_DQ7	DH58	DDR0_DQ_0_7/DDR0_DQ_0_7/DDR0_DQ_0_7/DDR0_DQ_0_7
DDRA_DQ6	DG57	DDR0_DQ_0_6/DDR0_DQ_0_6/DDR0_DQ_0_6/DDR0_DQ_0_6
DDRA_DQ5	DH56	DDR0_DQ_0_5/DDR0_DQ_0_5/DDR0_DQ_0_5/DDR0_DQ_0_5
DDRA_DQ4	DG60	DDR0_DQ_0_4/DDR0_DQ_0_4/DDR0_DQ_0_4/DDR0_DQ_0_4
DDRA_DQ3	DL60	DDR0_DQ_0_3/DDR0_DQ_0_3/DDR0_DQ_0_3/DDR0_DQ_0_3
DDRA_DQ2	DK56	DDR0_DQ_0_2/DDR0_DQ_0_2/DDR0_DQ_0_2/DDR0_DQ_0_2
DDRA_DQ1	DL57	DDR0_DQ_0_1/DDR0_DQ_0_1/DDR0_DQ_0_1/DDR0_DQ_0_1
DDRA_DQ0	DK58	DDR0_DQ_0_0/DDR0_DQ_0_0/DDR0_DQ_0_0/DDR0_DQ_0_0

Byte1[8~15]

DDRA_DQ15	DA58	DDR0_DQ_1_7/DDR0_DQ_1_7/DDR0_DQ_1_7/DDR0_DQ_1_7
DDRA_DQ14	CY57	DDR0_DQ_1_6/DDR0_DQ_1_6/DDR0_DQ_1_6/DDR0_DQ_1_6
DDRA_DQ13	DB56	DDR0_DQ_1_5/DDR0_DQ_1_5/DDR0_DQ_1_5/DDR0_DQ_1_5
DDRA_DQ12	CY60	DDR0_DQ_1_4/DDR0_DQ_1_4/DDR0_DQ_1_4/DDR0_DQ_1_4
DDRA_DQ11	DE60	DDR0_DQ_1_3/DDR0_DQ_1_3/DDR0_DQ_1_3/DDR0_DQ_1_3
DDRA_DQ10	DD56	DDR0_DQ_1_2/DDR0_DQ_1_2/DDR0_DQ_1_2/DDR0_DQ_1_2
DDRA_DQ9	DE57	DDR0_DQ_1_1/DDR0_DQ_1_1/DDR0_DQ_1_1/DDR0_DQ_1_1
DDRA_DQ8	DD58	DDR0_DQ_1_0/DDR0_DQ_1_0/DDR0_DQ_1_0/DDR0_DQ_1_0

Byte2[16~23]

DDRA_DQ23	DG50	DDR1_DQ_0_7/DDR0_DQ_2_7/DDR0_DQ_2_7/DDR1_DQ_0_7
DDRA_DQ22	DG47	DDR1_DQ_0_6/DDR0_DQ_2_6/DDR0_DQ_2_6/DDR1_DQ_0_6
DDRA_DQ21	DH48	DDR1_DQ_0_5/DDR0_DQ_2_5/DDR0_DQ_2_5/DDR1_DQ_0_5
DDRA_DQ20	DG53	DDR1_DQ_0_4/DDR0_DQ_2_4/DDR0_DQ_2_4/DDR1_DQ_0_4
DDRA_DQ19	DL53	DDR1_DQ_0_3/DDR0_DQ_2_3/DDR0_DQ_2_3/DDR1_DQ_0_3
DDRA_DQ18	DK48	DDR1_DQ_0_2/DDR0_DQ_2_2/DDR0_DQ_2_2/DDR1_DQ_0_2
DDRA_DQ17	DM47	DDR1_DQ_0_1/DDR0_DQ_2_1/DDR0_DQ_2_1/DDR1_DQ_0_1
DDRA_DQ16	DL50	DDR1_DQ_0_0/DDR0_DQ_2_0/DDR0_DQ_2_0/DDR1_DQ_0_0

Byte3[24~31]

DDRA_DQ31	CY50	DDR1_DQ_1_7/DDR0_DQ_3_7/DDR0_DQ_3_7/DDR1_DQ_1_7
DDRA_DQ30	CY47	DDR1_DQ_1_6/DDR0_DQ_3_6/DDR0_DQ_3_6/DDR1_DQ_1_6
DDRA_DQ29	DB48	DDR1_DQ_1_5/DDR0_DQ_3_5/DDR0_DQ_3_5/DDR1_DQ_1_5
DDRA_DQ28	DA53	DDR1_DQ_1_4/DDR0_DQ_3_4/DDR0_DQ_3_4/DDR1_DQ_1_4
DDRA_DQ27	DE53	DDR1_DQ_1_3/DDR0_DQ_3_3/DDR0_DQ_3_3/DDR1_DQ_1_3
DDRA_DQ26	DC48	DDR1_DQ_1_2/DDR0_DQ_3_2/DDR0_DQ_3_2/DDR1_DQ_1_2
DDRA_DQ25	DE47	DDR1_DQ_1_1/DDR0_DQ_3_1/DDR0_DQ_3_1/DDR1_DQ_1_1
DDRA_DQ24	DE50	DDR1_DQ_1_0/DDR0_DQ_3_0/DDR0_DQ_3_0/DDR1_DQ_1_0

Byte4[32~39]

DDRA_DQ39	BU58	DDR0_DQ_2_7/DDR0_DQ_4_7/DDR1_DQ_0_7/DDR2_DQ_0_7
DDRA_DQ38	BT57	DDR0_DQ_2_6/DDR0_DQ_4_6/DDR1_DQ_0_6/DDR2_DQ_0_6
DDRA_DQ37	BU56	DDR0_DQ_2_5/DDR0_DQ_4_5/DDR1_DQ_0_5/DDR2_DQ_0_5
DDRA_DQ36	BT60	DDR0_DQ_2_4/DDR0_DQ_4_4/DDR1_DQ_0_4/DDR2_DQ_0_4
DDRA_DQ35	BV60	DDR0_DQ_2_3/DDR0_DQ_4_3/DDR1_DQ_0_3/DDR2_DQ_0_3
DDRA_DQ34	BW56	DDR0_DQ_2_2/DDR0_DQ_4_2/DDR1_DQ_0_2/DDR2_DQ_0_2
DDRA_DQ33	BY57	DDR0_DQ_2_1/DDR0_DQ_4_1/DDR1_DQ_0_1/DDR2_DQ_0_1
DDRA_DQ32	BW58	DDR0_DQ_2_0/DDR0_DQ_4_0/DDR1_DQ_0_0/DDR2_DQ_0_0

Byte5[40~47]

DDRA_DQ47	BL58	DDR0_DQ_3_7/DDR0_DQ_5_7/DDR1_DQ_1_7/DDR2_DQ_1_7
DDRA_DQ46	BK57	DDR0_DQ_3_6/DDR0_DQ_5_6/DDR1_DQ_1_6/DDR2_DQ_1_6
DDRA_DQ45	BL56	DDR0_DQ_3_5/DDR0_DQ_5_5/DDR1_DQ_1_5/DDR2_DQ_1_5
DDRA_DQ44	BK60	DDR0_DQ_3_4/DDR0_DQ_5_4/DDR1_DQ_1_4/DDR2_DQ_1_4
DDRA_DQ43	BP60	DDR0_DQ_3_3/DDR0_DQ_5_3/DDR1_DQ_1_3/DDR2_DQ_1_3
DDRA_DQ42	BN56	DDR0_DQ_3_2/DDR0_DQ_5_2/DDR1_DQ_1_2/DDR2_DQ_1_2
DDRA_DQ41	BP57	DDR0_DQ_3_1/DDR0_DQ_5_1/DDR1_DQ_1_1/DDR2_DQ_1_1
DDRA_DQ40	BN58	DDR0_DQ_3_0/DDR0_DQ_5_0/DDR1_DQ_1_0/DDR2_DQ_1_0

Byte6[48~55]

DDRA_DQ55	BT50	DDR1_DQ_2_7/DDR0_DQ_6_7/DDR1_DQ_2_7/DDR3_DQ_0_7
DDRA_DQ54	BT47	DDR1_DQ_2_6/DDR0_DQ_6_6/DDR1_DQ_2_6/DDR3_DQ_0_6
DDRA_DQ53	BU48	DDR1_DQ_2_5/DDR0_DQ_6_5/DDR1_DQ_2_5/DDR3_DQ_0_5
DDRA_DQ52	BT53	DDR1_DQ_2_4/DDR0_DQ_6_4/DDR1_DQ_2_4/DDR3_DQ_0_4
DDRA_DQ51	BY53	DDR1_DQ_2_3/DDR0_DQ_6_3/DDR1_DQ_2_3/DDR3_DQ_0_3
DDRA_DQ50	BW48	DDR1_DQ_2_2/DDR0_DQ_6_2/DDR1_DQ_2_2/DDR3_DQ_0_2
DDRA_DQ49	CA47	DDR1_DQ_2_1/DDR0_DQ_6_1/DDR1_DQ_2_1/DDR3_DQ_0_1
DDRA_DQ48	BY50	DDR1_DQ_2_0/DDR0_DQ_6_0/DDR1_DQ_2_0/DDR3_DQ_0_0

Byte7[56~63]

DDRA_DQ63	BJ50	DDR1_DQ_3_7/DDR0_DQ_7_7/DDR1_DQ_3_7/DDR3_DQ_1_7
DDRA_DQ62	BJ47	DDR1_DQ_3_6/DDR0_DQ_7_6/DDR1_DQ_3_6/DDR3_DQ_1_6
DDRA_DQ61	BL48	DDR1_DQ_3_5/DDR0_DQ_7_5/DDR1_DQ_3_5/DDR3_DQ_1_5
DDRA_DQ60	BK53	DDR1_DQ_3_4/DDR0_DQ_7_4/DDR1_DQ_3_4/DDR3_DQ_1_4
DDRA_DQ59	BP53	DDR1_DQ_3_3/DDR0_DQ_7_3/DDR1_DQ_3_3/DDR3_DQ_1_3
DDRA_DQ58	BN48	DDR1_DQ_3_2/DDR0_DQ_7_2/DDR1_DQ_3_2/DDR3_DQ_1_2
DDRA_DQ57	BP47	DDR1_DQ_3_1/DDR0_DQ_7_1/DDR1_DQ_3_1/DDR3_DQ_1_1
DDRA_DQ56	BP50	DDR1_DQ_3_0/DDR0_DQ_7_0/DDR1_DQ_3_0/DDR3_DQ_1_0

DDR4

CD49	DDRA_CLK1_P	DDRA_CLK1_P
CD48	DDRA_CLK1_N	DDRA_CLK1_N
CH61		
CF61		
CN49		
CN48		
CU61	DDRA_CLK0_P	DDRA_CLK0_P
CR61	DDRA_CLK0_N	DDRA_CLK0_N

DDR4

CF51		
CH51		
CE57		
CF58		
CR51		
CU51		
CR58		
CP57		

DDR4(IL) / DDR4(NIL)

BN51	DDRA_DQS7_P	DDRA_DQS7_P
BL51	DDRA_DQS7_N	DDRA_DQS7_N
BW51	DDRA_DQS6_P	DDRA_DQS6_P
BU51	DDRA_DQS6_N	DDRA_DQS6_N
BL61	DDRA_DQS5_P	DDRA_DQS5_P
BN61	DDRA_DQS5_N	DDRA_DQS5_N
BU61	DDRA_DQS4_P	DDRA_DQS4_P
BW61	DDRA_DQS4_N	DDRA_DQS4_N
DC51	DDRA_DQS3_P	DDRA_DQS3_P
DB51	DDRA_DQS3_N	DDRA_DQS3_N
DK51	DDRA_DQS2_P	DDRA_DQS2_P
DH51	DDRA_DQS2_N	DDRA_DQS2_N
DB61	DDRA_DQS1_P	DDRA_DQS1_P
DC61	DDRA_DQS1_N	DDRA_DQS1_N
DH61	DDRA_DQS0_P	DDRA_DQS0_P
DK61	DDRA_DQS0_N	DDRA_DQS0_N

DDR4

CM60	DDRA_MA5	DDRA_MA5
CL55	DDRA_MA7	DDRA_MA7
CM57	DDRA_MA6	DDRA_MA6
CP60	DDRA_MA8	DDRA_MA8
CU58		
CU56		
CM47	DDRA_BA1	DDRA_BA1
CM53	DDRA_MA16	DDRA_MA16
CT46	DDRA_MA15	DDRA_MA15
CP53	DDRA_MA14	DDRA_MA14
CW47	DDRA_CS1_N	DDRA_CS1_N
CV53	DDRA_ODT1	DDRA_ODT1
CC60	DDRA_CKE0	DDRA_CKE0
CB55	DDRA_CKE1	DDRA_CKE1
CC57	DDRA_BG0	DDRA_BG0
CE60	DDRA_BG1	DDRA_BG1
CH56	DDRA_MA12	DDRA_MA12
CH58	DDRA_MA9	DDRA_MA9
CC53		
CC47		
CE53		
CH46		
CK47	DDRA_MA10	DDRA_MA10
CJ53	DDRA_BA0	DDRA_BA0

DDR4

CV60	DDRA_MA3	DDRA_MA3
CR56	DDRA_MA4	DDRA_MA4
CU48	DDRA_MA13	DDRA_MA13
CM50	DDRA_ODT0	DDRA_ODT0
CJ57	DDRA_ACT_N	DDRA_ACT_N
CF56		
CH48	DDRA_PARITY	DDRA_PARITY
CC50	DDRA_MA2	DDRA_MA2

DDR4

CV50	DDRA_CS0_N	DDRA_CS0_N
CJ50	DDRA_MA0	DDRA_MA0
CV57	DDRA_MA1	DDRA_MA1
CJ60	DDRA_MA11	DDRA_MA11

DDR4

BF61		
BG60	DDRA_VREF_CA_CPU	DDRA_VREF_CA_CPU

BG50		DDR_PG_CTRL
EE53		
A56	DDR_COMP	RC802 2 1 1/20W_100_1%_0201
B56		

DDR_VTT_CTL
DRAM_RESET#
DDR_COMP_1
DDR_COMP_2

2 OF 22

INTEL_ADL-P-682_BGA1744

@

+1.2V
RC4293 1/20W_1K_5%_0201
DDR_VTT_PG_CTRL
QC1 MMBT3904WH_SOT323-3
+3VALW
RC15 1/20W_100K_5%_0201
DDR_VTT_PG_CTRL
RC16 1/20W_10K_5%_0201
+1.2V
RC17 1/20W_470_5%_0201
DRAMRST_N
RC622 1 @ 2 0_0201_5%
DRAMRST_N_R
DRAMRST_N_R

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Title	X60-TGL-H		
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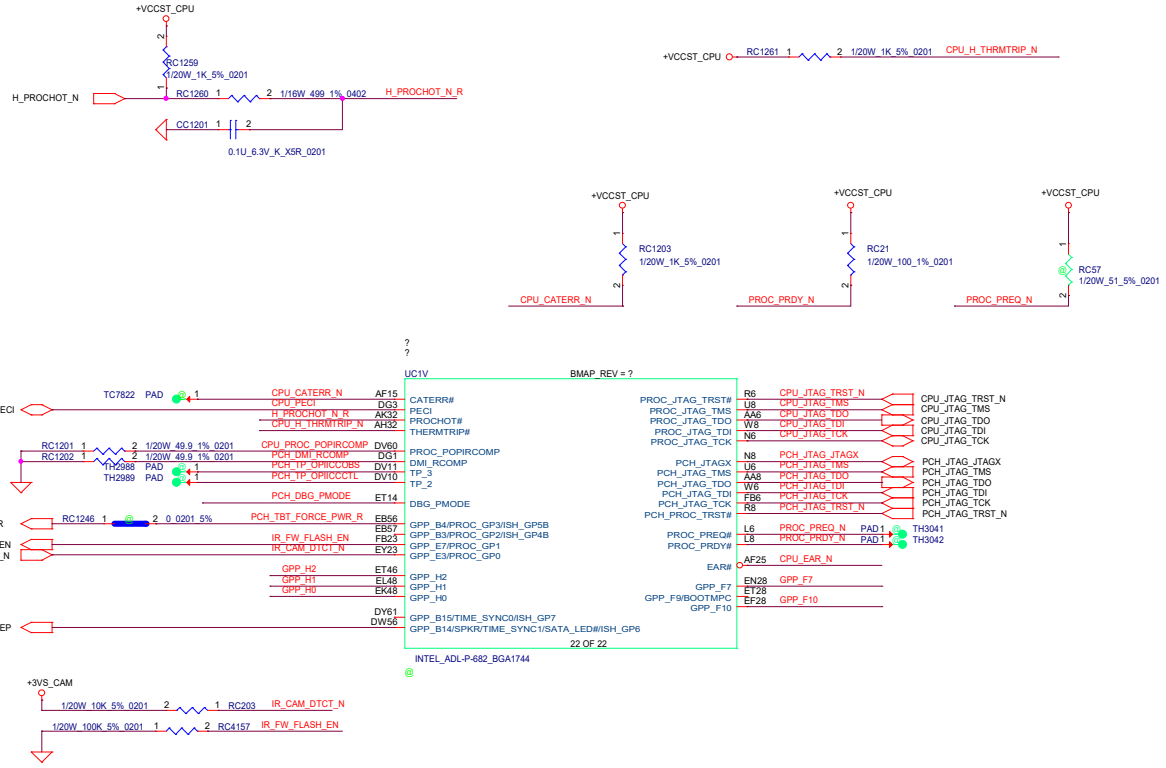
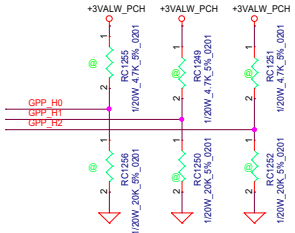
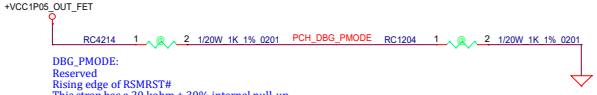




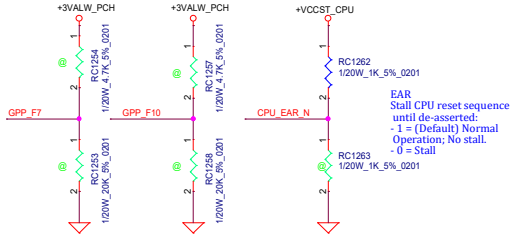
GPP_H0: Boot Strap 1
GPP_H1: Boot Strap 2
GPP_H2: Boot Strap 3
Boot Strap, Rising edge of RSMRST#
These straps has a 20 kohm ± 30% internal pull-down.
They are bit [3:1] of a total of 4-bit encoded pin straps
for boot configuration.
Refer to Boot Strap 0 (on GPP_C5) for the encoding.
Notes: 1. The internal pull-down is disabled after
RSMRST# de-asserts.
2. This signal is in the primary well.
* 0000 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is enabled
0010 = Master Attached Flash Configuration (BIOS / CSME on SPI). eSPI is disabled
0100 = BIOS on eSPI Peripheral Channel; CSME on master attached SPI
1000 = Slave Attached Flash Configuration (BIOS / CSME on eSPI attached device).
1100 = BIOS on eSPI peripheral Channel; CSME on slave attached SPI.



DBG_PMODE:
Reserved
Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-up.
This strap should sample high. There should NOT be any on-board device
driving it to opposite direction during strap sampling.
Notes:1. The internal pull-up is disabled after RSMRST# deasserts.
2. This signal is in the primary well.

Pin Straps

GPP_B14:
Rising edge of PCH_PWROK
The strap has a 20 kohm ± 30% internal pull-down.
0 = Disable Top Swap mode. (Default)
1 = Enable Top Swap mode. This inverts an address on access to SPI
and firmware hub, so the processor believes it fetches the alternate
boot block instead of the original boot-block. PCH will invert A16
(default) for cycles going to the upper two 64-KB blocks in the FWH
or the appropriate address lines (A16, A17, or A18) as selected
in Top Swap Block size soft strap.
Notes:
1. The internal pull-down is disabled after PCH_PWROK is high.
2. Software will not be able to clear the Top Swap bit until the system
is rebooted.
3. The status of this strap is readable using the Top Swap bit
(Bus0, Device31, Function0, offset DCh, bit4).
4. This signal is in the primary well.



EAR
Stall CPU reset sequence
until de-asserted:
- 1 = (Default) Normal
Operation; No stall.
- 0 = Stall

GPP_F7 and GPP_F10:
Reserved, Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
This strap should sample LOW. There should NOT be any onboard
device driving it to opposite direction during strap sampling.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

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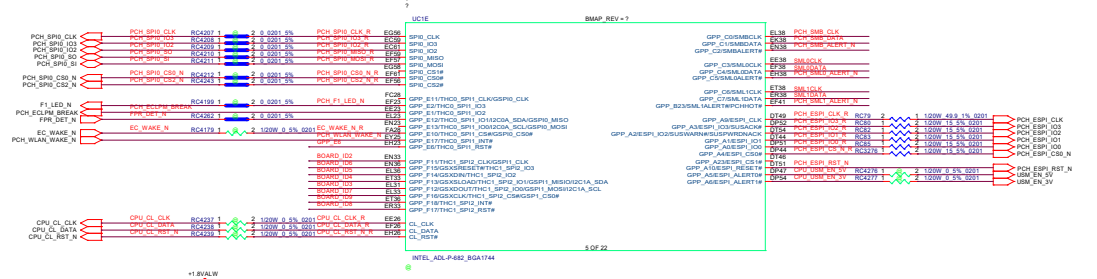
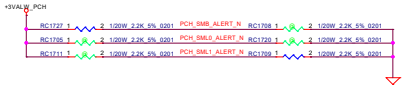
Pin Straps





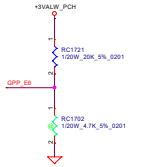
GPP_C2 /SMBALERT#
Rising edge of RSMRST#
The strap has a 20 kohm ± 30% internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

GPP_C5 /SML0ALERT#
Rising edge of RSMRST#
The strap has a 20 kohm ± 30% internal pull-down.
This is bit 0(LSB) of a total of 4-bit encoded pin straps for boot configuration. Used in with Boot Strap1,2,3 ({GPP_H[0:2]}
0 = eSPI Enable (for EC). (Default)
1 = eSPI Disable (for EC).

GPP_B23 /SML1ALERT#
Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
0 = 38.4 MHz clock (direct from crystal) (default)
1 = 19.2 MHz clock (derived from 38.4 MHz crystal)
Notes: 1. The internal pull-down is disabled after RSMRST# de-asserts.
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.
3. This signal is in the primary well.

SPI0_MOSI (PCH_SPI0_MOSI_R):
Rising edge of RSMRST#
External pull-up is required. Recommend 4.7 kohm pull up.
This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.

SPI0_IO2 and SPI0_IO3:
Rising edge of RSMRST#
External pull-up is required.
Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any onboard device driving it to opposite direction during strap sampling.



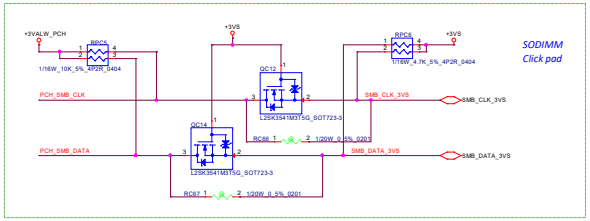
GPP_E6:
ITAG ODT Disable
Rising edge of RSMRST#
This strap does not have an internal pull-up or pull-down.
External pull-up is recommended
0=> JTAG ODT is disabled
1=> JTAG ODT is enabled

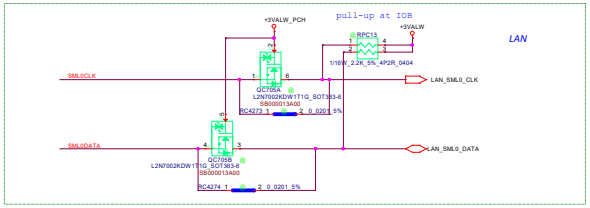
Board ID for IOB

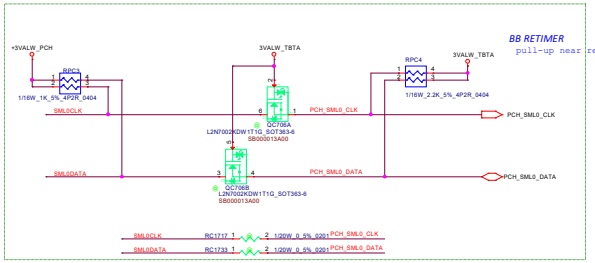
	SOM-FFR	FFR
FFR_DET_N	1	0

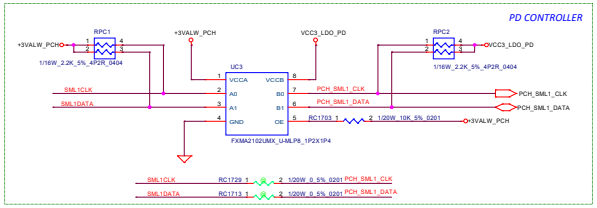
Glitch Free Requirements:
Cap or pull-down resistor is required

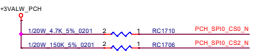
100K for 3.3V Signaling Mode
75K for 1.8V Signaling Mode



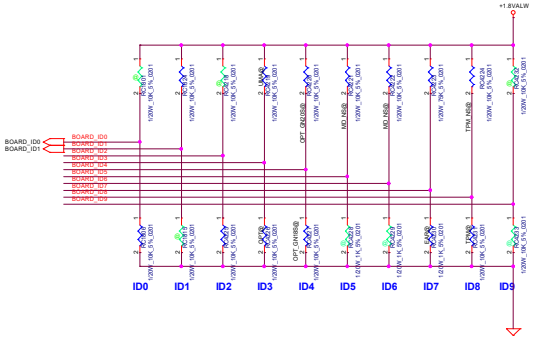








Board ID	Description	Stuff R
Board_ID [2,1,0]	000 EVT	RC1601
	001 FVT	RC1615
	010 SIT	RC4225
	011 SITR	
	100 SVT	
Board_ID3	0 DIS	RC4226
	1 UMA	RC4219
Board_ID4	0 GN18S	RC4227
	1 GN20S	RC4220
Board_ID [2,6,5]	000 Micron	RC4229 RC4228
	001 Samsung	RC4229 RC4221
	010 SK Hynix	
	100 Micron 2	RC4222 RC4228
	X11 no mem down	RC4222 RC4221
Board_ID7	0 Earphone	RC4230
	1 No Earphone	
Board_ID8	0 TPM	RC4231
	1 NO TPM	RC4224
Board_ID9	Reserved	



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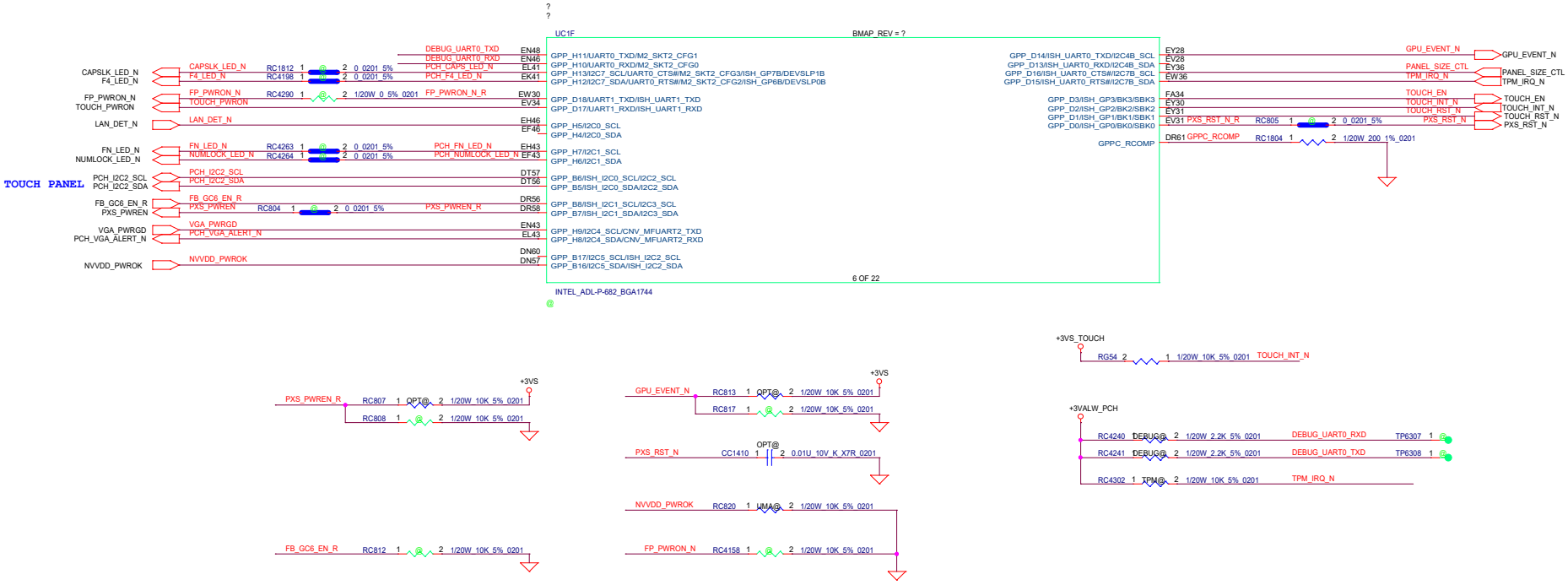

Board ID for IOB

	without LAN	with LAN
LAN_DET_N	1	0

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Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: X60-TGL-H

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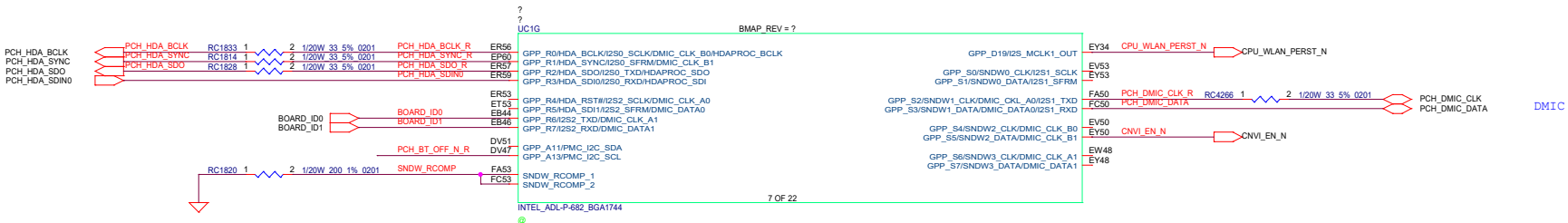
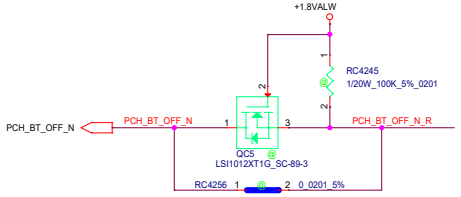


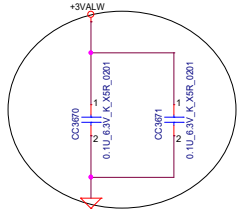
DMIC

Pin Straps

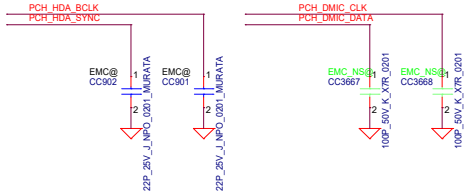
GPP_R2/HDA_SDO (PCH_HDA_SDO_R)
The strap has a 20 kohm ± 30% internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.



Signal:CPU_BT_OFF_M_N
Voltage Level:1.8V
LSI1012XT1G_SC-89-3
Vds max=20V
Vgs max=+/- 6V
Vgs(th)=0.45V/0.9V(min/max)
Rds(ON)=1.25ohm(max,Vgs=1.8 V)
Id=350mA(TA =25 C)
Ton Delay=5ns
Rise time=5ns



add split cap for DMIC at 6/29



Security Classification	LCFC Highly Confidential Information		
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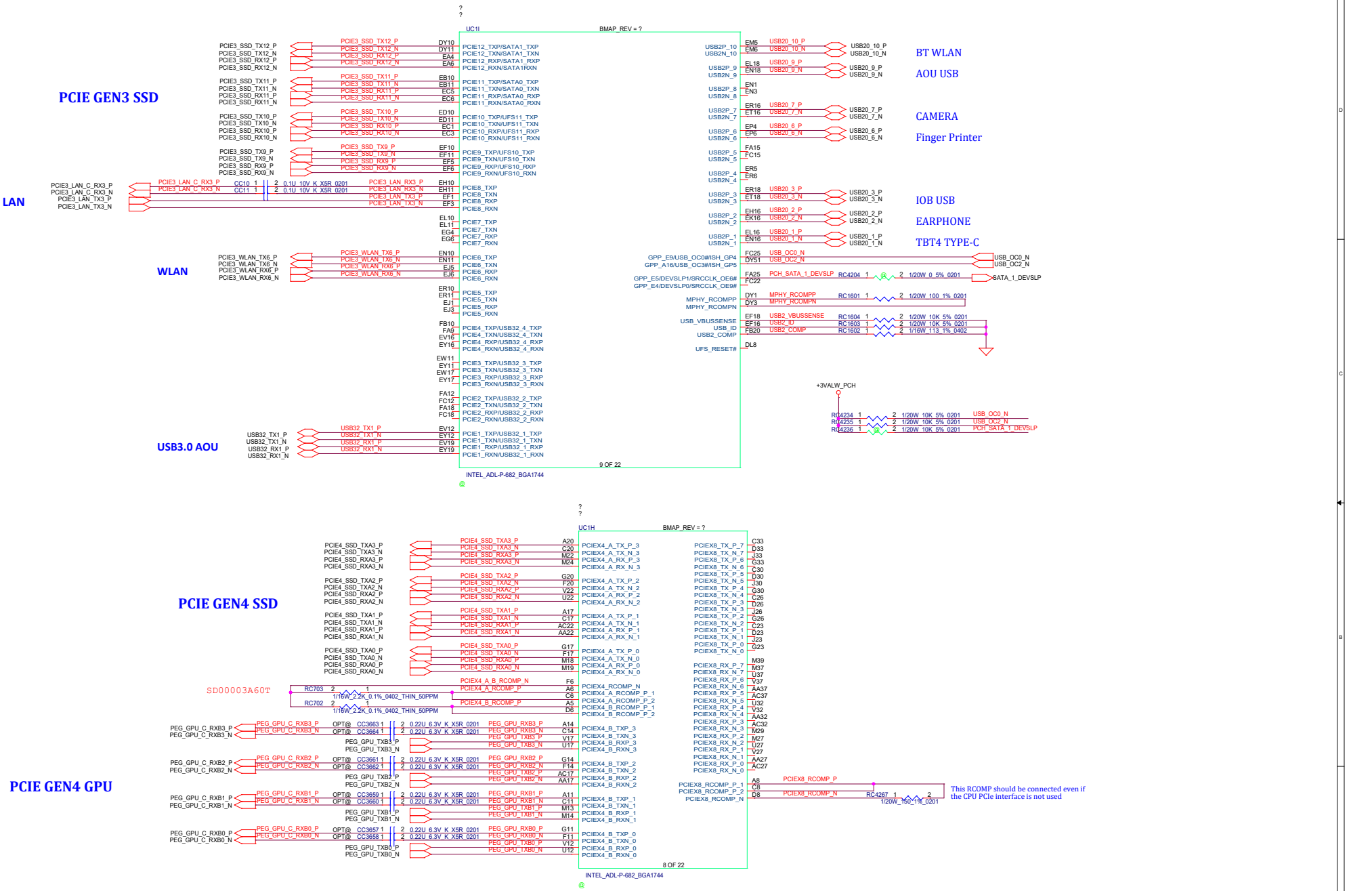

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: X60-TGL-H

LCFC

Size	Document Number	Rev
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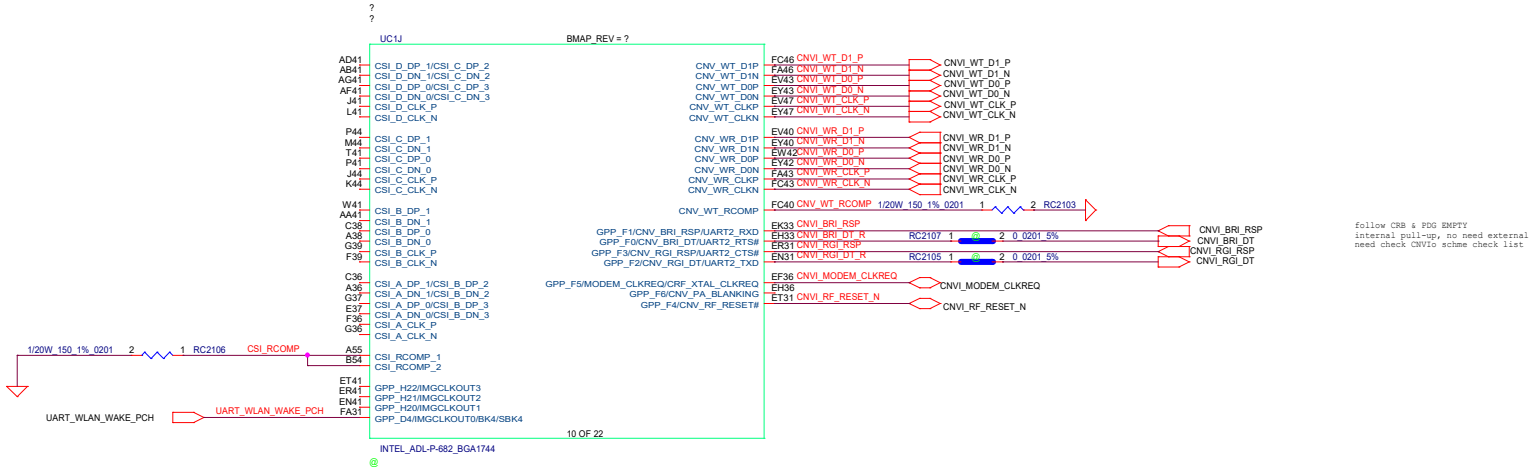
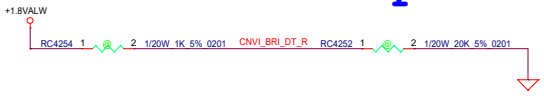
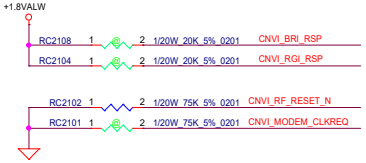


Pin Straps





GPP_F0 /CNV_BRI_DT /UART2_RTS#(CNV_BRI_DT_R)
XTAL Frequency Selection, Rising edge of RSMRST#
This strap has a 20 kohm ± 30% internal pull-down.
This strap should not be pulled high since 24 MHz crystal is not supported on the PCH.
0 = 38.4 MHz (default)
1 = 24 MHz
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

GPP_F2 /CNV_RGI_DT /UART2_TXD(CNV_RGI_DT_R):
M.2 CNVI MODES, Rising edge of RSMRST#
This strap does not have an internal pull-up or pull-down.
A weak external pull-up is required.
0 = Integrated CNVi enabled.
1 = Integrated CNVi disabled.
Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pulldown resistor will pull the strap low to enable CNVi interface.

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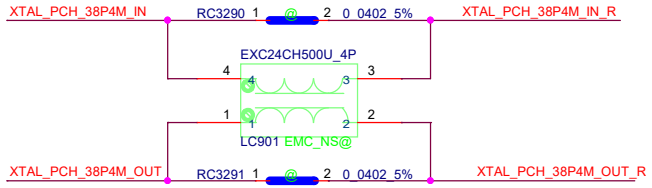
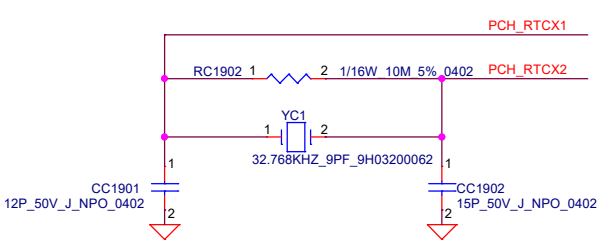
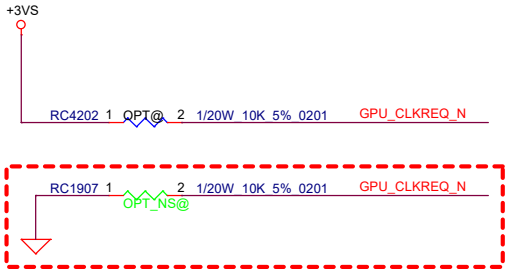
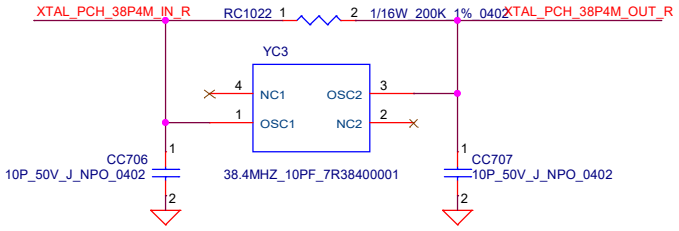
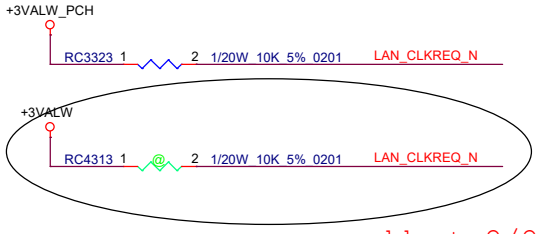
All processor based platforms are required to provide a 38.4MHz input to the PCH to enable the PCH to generate all of its internal reference clocks and all of the single-ended and differential platform clock outputs





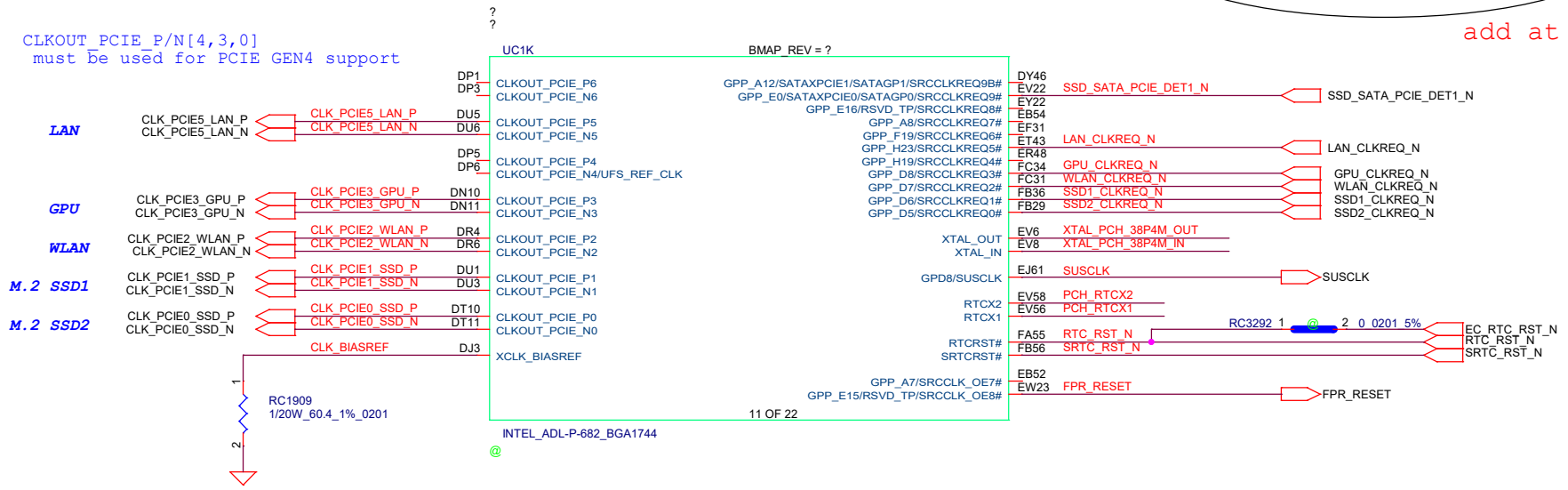






add at 2/23

CLKOUT_PCIE_P/N[4,3,0]
must be used for PCIE GEN4 support



Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	X60-TGL-H		
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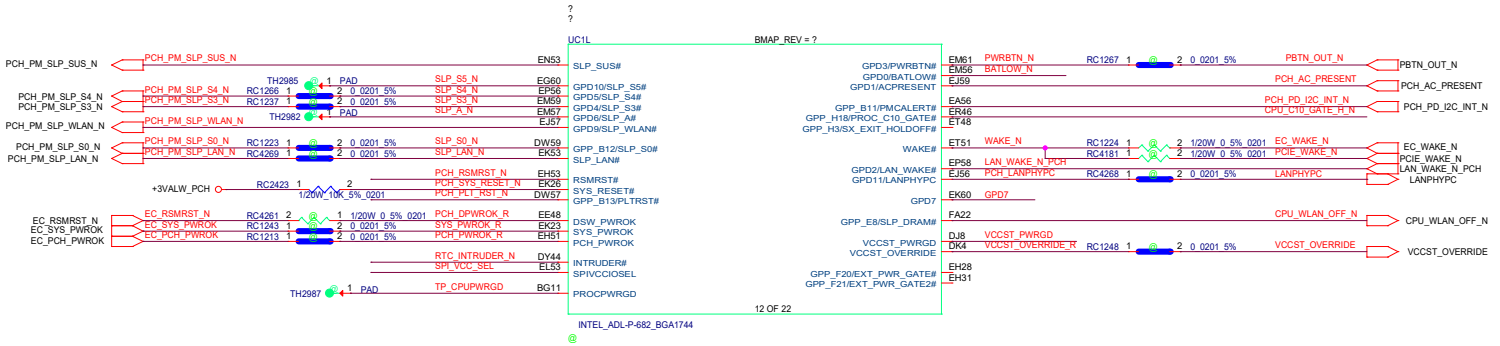
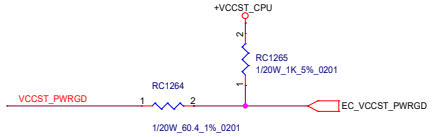
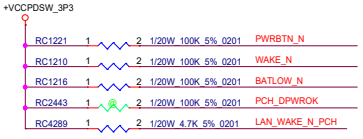
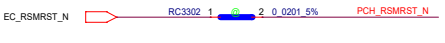
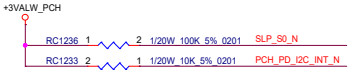
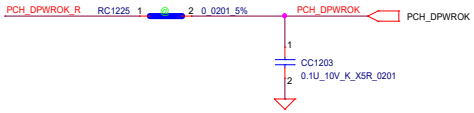


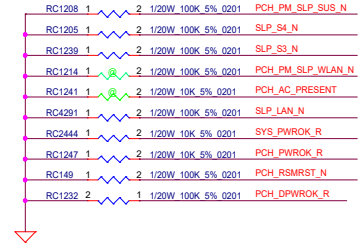


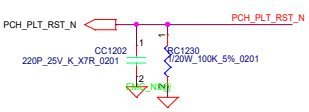




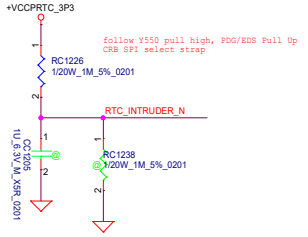


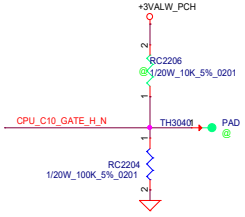




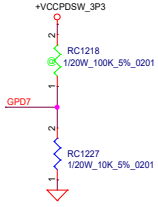


Emergency Power Loss Early De-assertion of DSW_PWROK control circuit

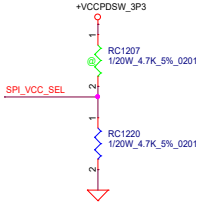




Pin Straps



GPD7:
Rising edge of DSW_PWROK
This strap has a 20Kohm±30% internal pull-down
This strap should sample LOW. There should
not be any on-board device driving it to opposite direction
during strap sampling.
NOTES: 1. The internal pull-down is disabled after
DSW_PWROK is high.
2. This signal is in the DSW well.



SPIVCCIOSEL(SPI_VCC_SEL):
SPI Operation Voltage Select
Rising edge of DSW_PWROK
There is no internal pull-up or pull-down on the strap. An
external resistor is required.
0 = SPI voltage is 3.3V (4.7 kohm pull-down to GND)
1 = SPI voltage is 1.8V (4.7K pull-up to DSW_3P3)

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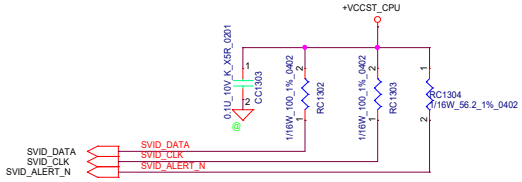

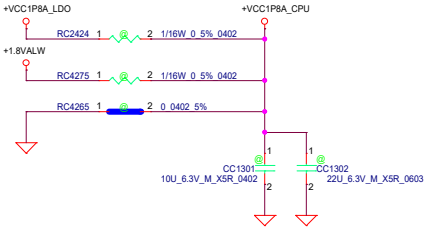

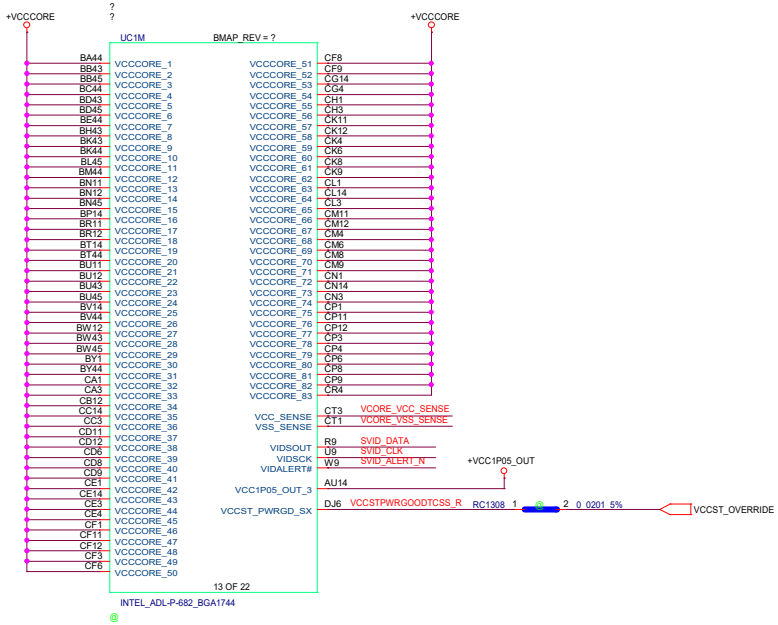

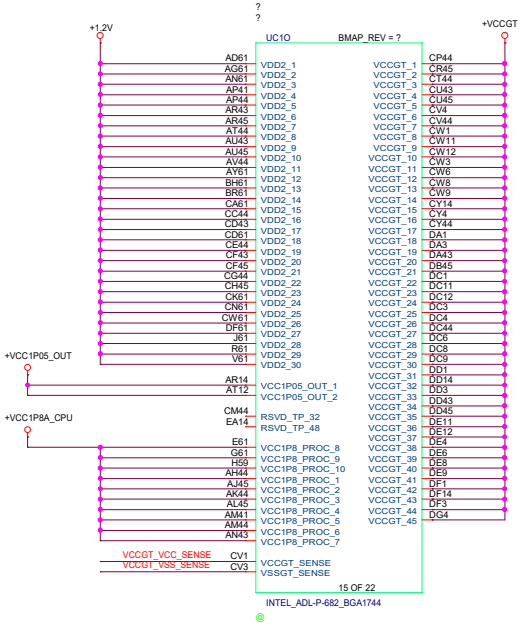

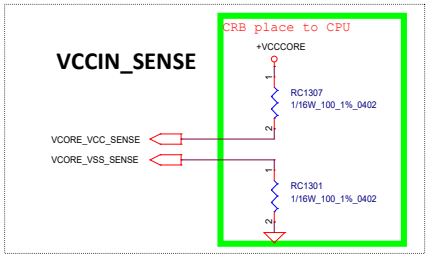

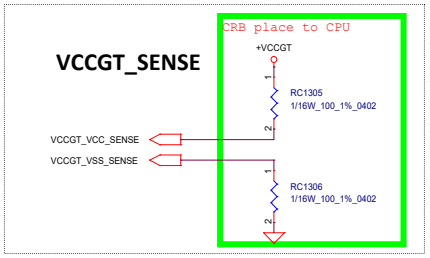

Security Classification	LCFC Highly Confidential Information		
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Title: X60-TGL-H

LCFC

Size	Document Number	Rev
C	CPU (8/9) PWR,BYPASS	0.1

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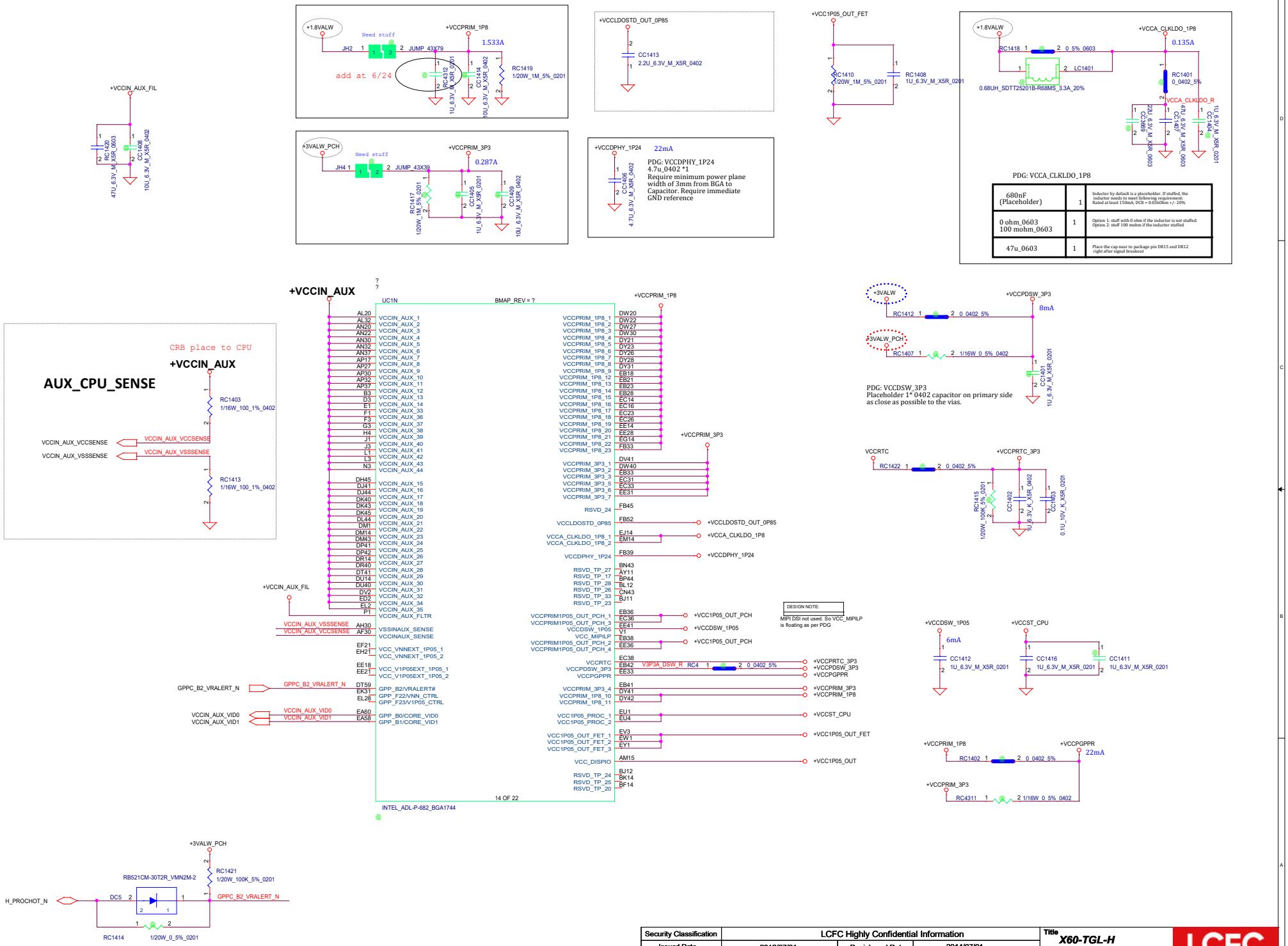

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: X60-TGL-H

LCFC

Size	Document Number	Rev
C	CPU (8/9) PWR,BYPASS	0.1

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Title	<Title>		
Size C	Document Number <Doc>		Rev <RevCode>
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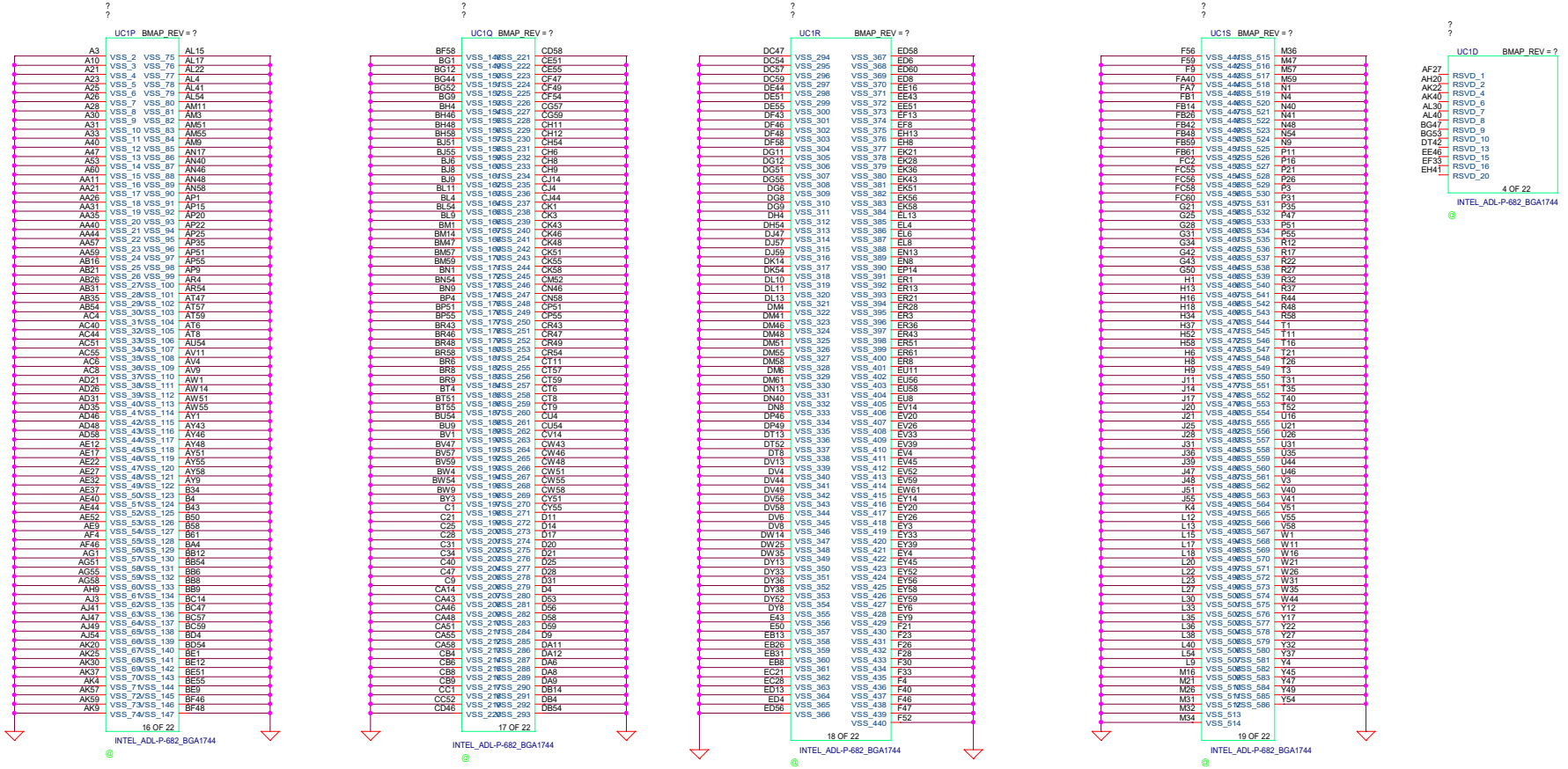

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: X60-TGL-H

LCFC

Size	Document Number	Rev
C	PCH (8/8) VSS	0.1

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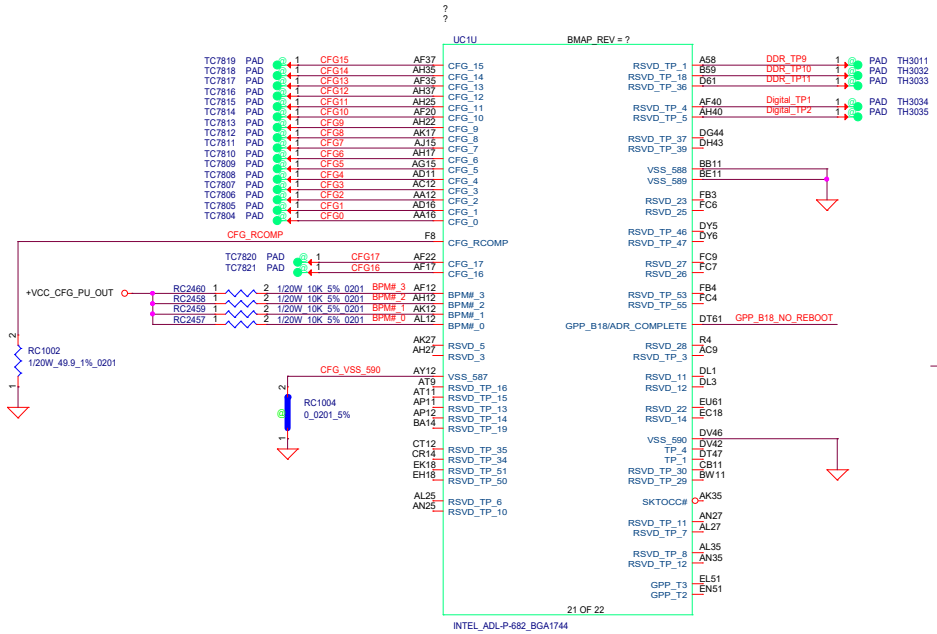
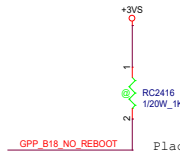
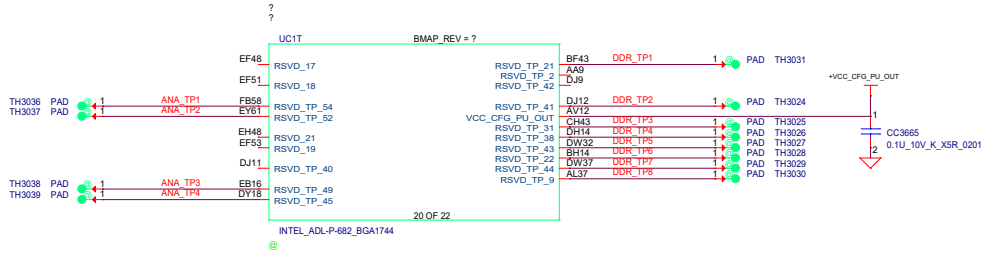
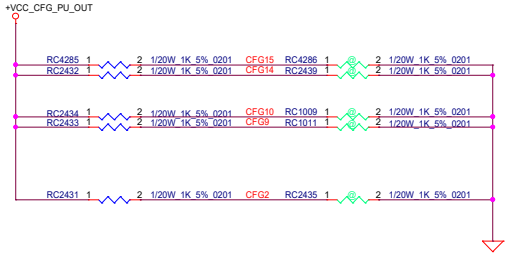




Pin STRAPS

GPP_B18_NO_REBOOT
Rising edge of PCH_PWROK
The strap has a 20 kohm ± 30% internal pull-down.
0 = Disable "No Reboot" mode. (Default)
1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.





Pin Name	Description	Termination	Resistor
CFG[0,1]	RSVD	None	
CFG[2]	PCI Express* Static x8(PEG 10/11) Lanes Numbering Reversal	Pull-up to VCC_CFG_PU_OUT/ Pull-down-Platform design dependent	1K
CFG[3]	RSVD	None	
CFG[4]	RSVD	None	
CFG[6:5]	RSVD	None	
CFG[8:7]	RSVD	None	
CFG[10:9]	RSVD	Pull-up to VCC_CFG_PU_OUT	
CFG[13:11]	RSVD	None	1K
CFG[14]	PEG60 Lane Reversal: -1- (Default)Normal -0-Reversed	Pull-up to VCC_CFG_PU_OUT/ Pull-down-Platform design dependent	1K
CFG[15]	PEG62 Lane Reversal: -1- (Default)Normal -0-Reversed	Pull-up to VCC_CFG_PU_OUT/ Pull-down-Platform design dependent	1K
CFG[17:16]	RSVD	None	

Security Classification	LCFC Highly Confidential Information		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

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LCFC

Size	Document Number	Rev
C	CPU (4/9) PM,XDP,CLK,CFG	0.1

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TABLE : CPU ITP DEBUG REPORT

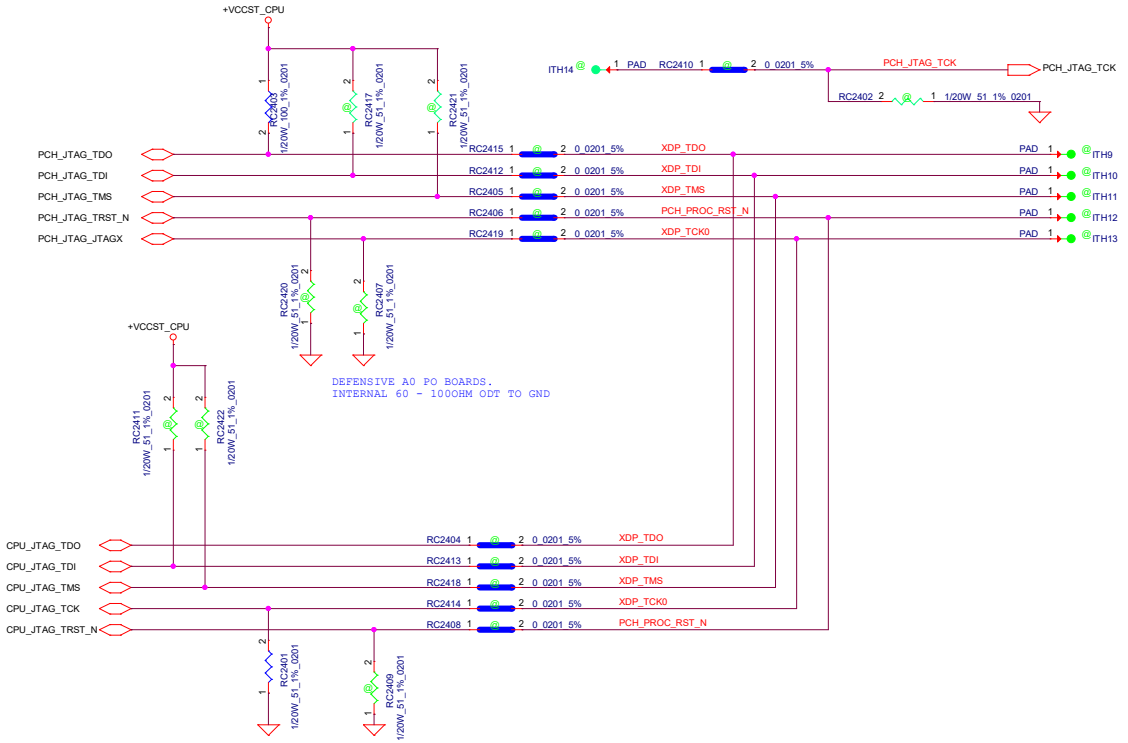
	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

LOGIC

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

LOGIC



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	XDP		
Size	Document Number		Rev
Custom	Y550		0.1
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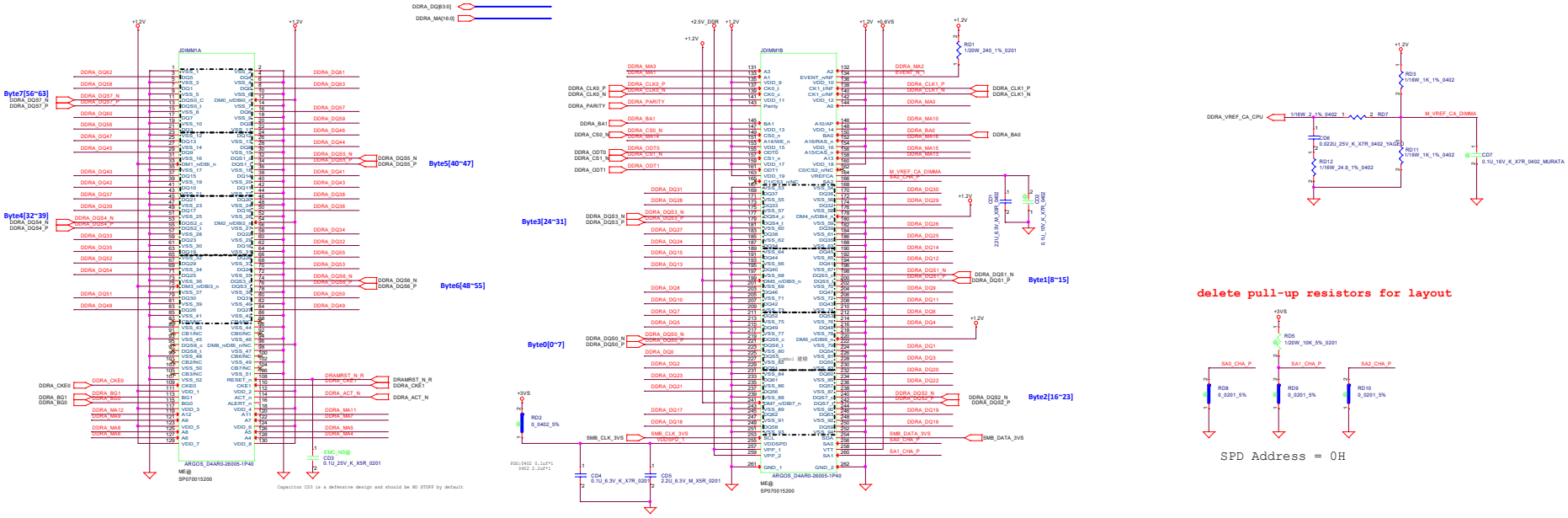

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title	DDR4 SUB CHANNEL-A		
Size: D	Document Number: E14/E15 NM-E211		Rev: 0.1
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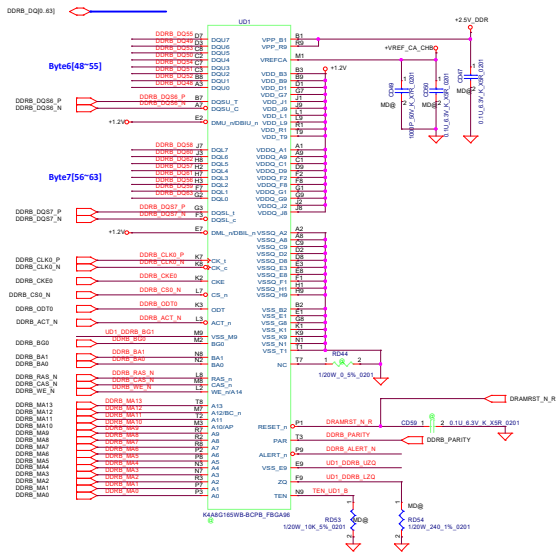
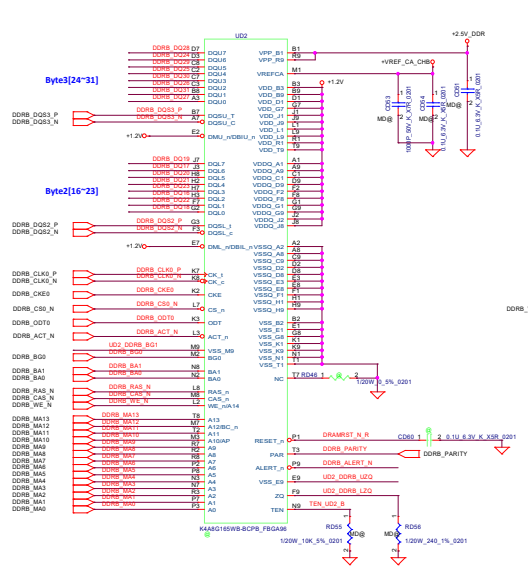
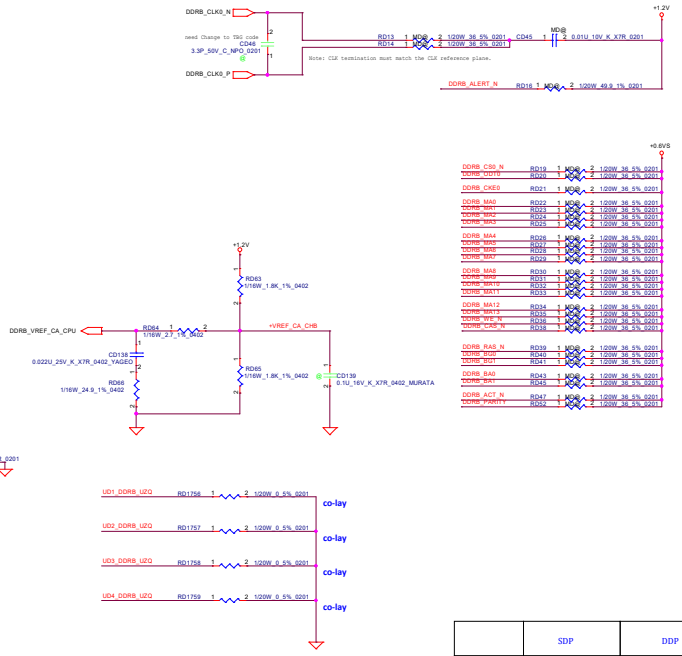
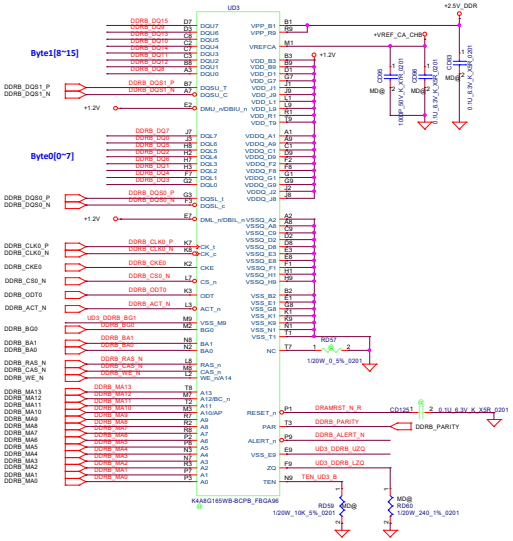
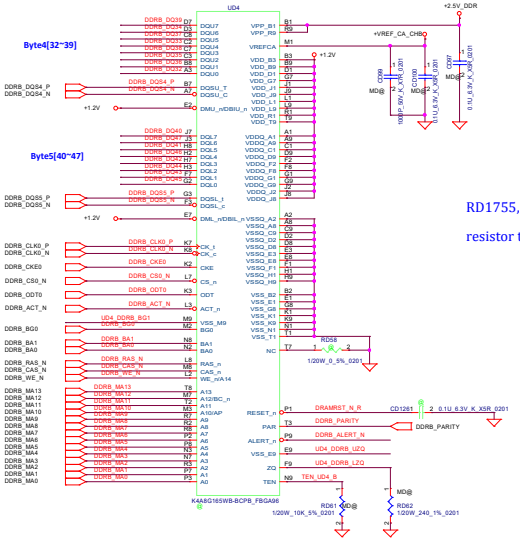






	SDP		DDP	
BG1 STUFF	RD1755	RD1761	RD1754	RD1760
	RD1763	RD1765	RD1762	RD1764
UZQ STUFF	RD1756	RD1757	RD1718	RD1723
	RD1758	RD1759	RD1731	RD1735





source	8Gb		
Samsung	K4A8G165WC-BCWE	SA0000C6N00	NOT USE
SK	H5AN8G6NDJR-XNC		NOT USE
Micron	MT40A512M16TB-062E:R		NOT USE

source	16Gb		
Samsung	K4AAG165WB-BCWE	SA0000C6N00	SDP
SK	H5ANAG6NCJR-XNC	SA0000B5K00	SDP
Micron	MT40A1G16RC-062E:B	SA0000A4K10	SDP

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Issued Date	2019/10/29	Deciphered Date	2019/10/29

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Title	DDR4 SUB CHANNEL-B		
Size	Document Number		Rev
D	E14/E15 NM-E211		0.1
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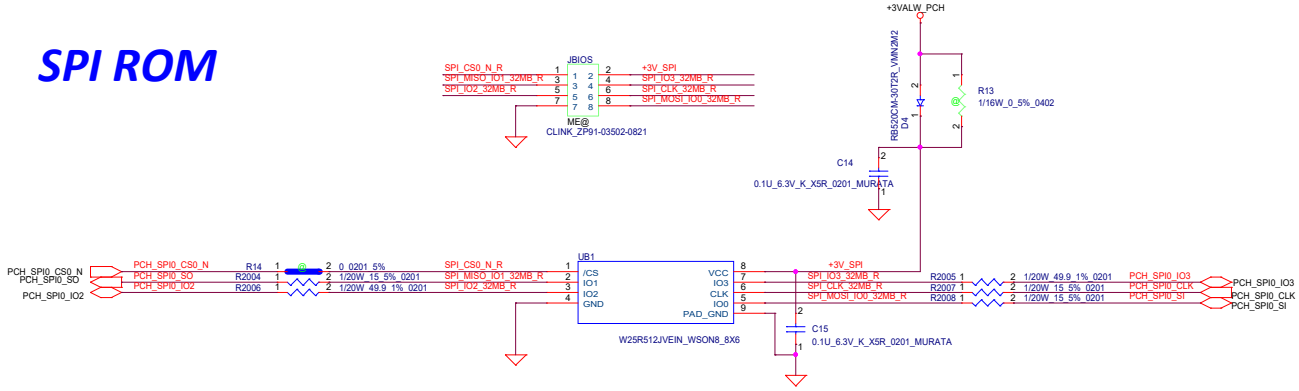
SPI ROM



TPM IC

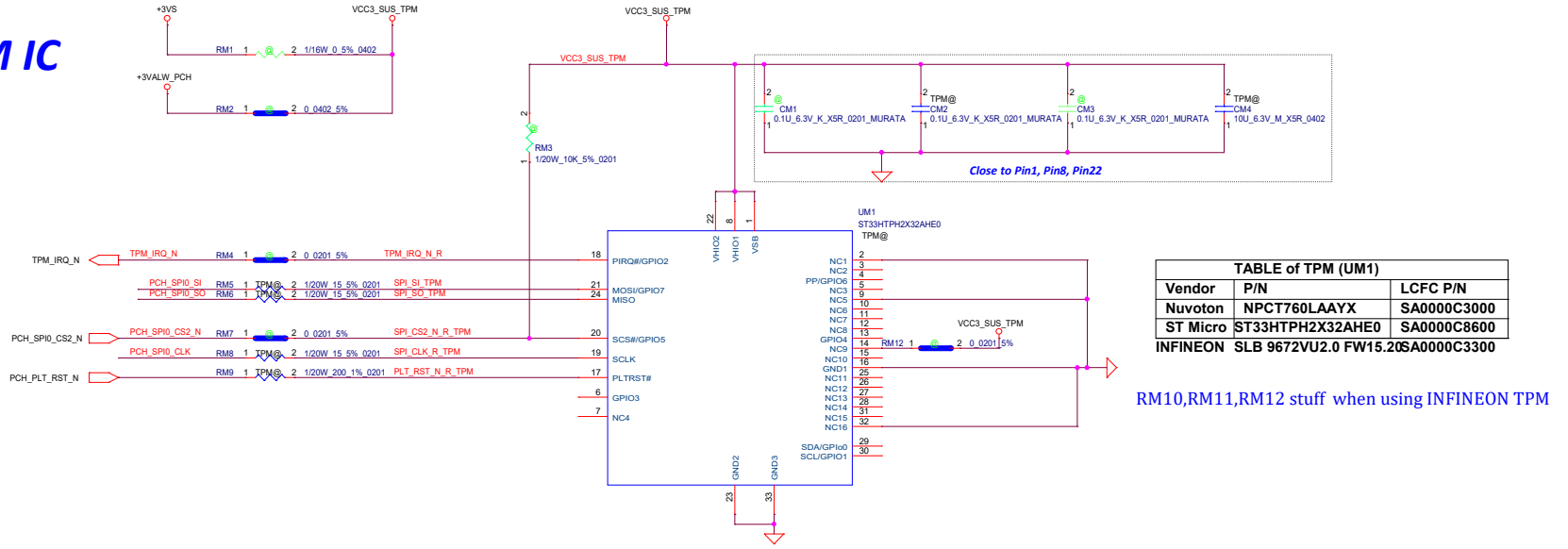


TABLE of TPM (UM1)		
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Nuvoton	NPCT760LAAYX	SA0000C3000
ST Micro	ST33HTPH2X32AHE0	SA0000C8600
INFINEON	SLB 9672VU2.0 FW15.20	SA0000C3300

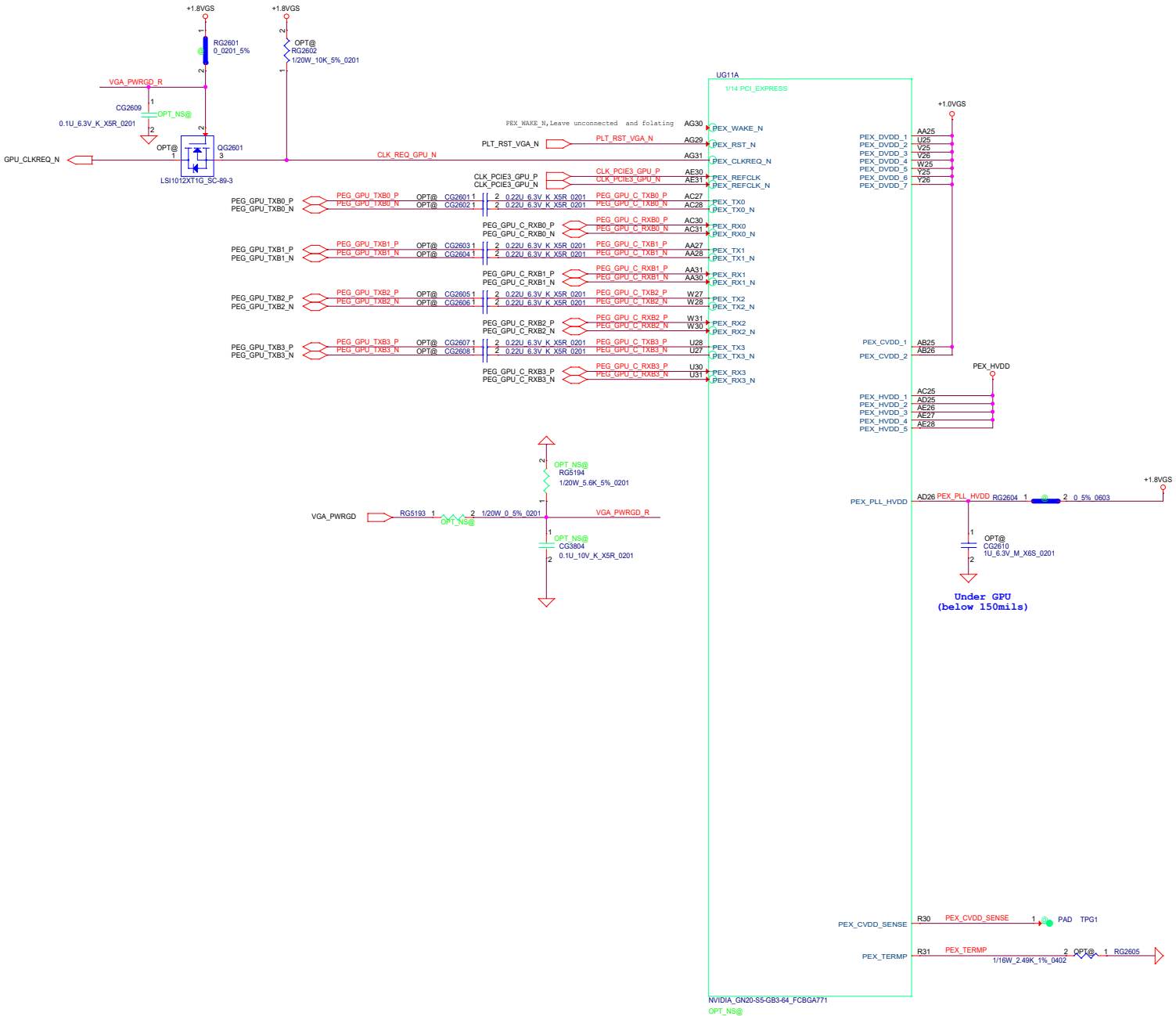
RM10,RM11,RM12 stuff when using INFINEON TPM

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: *SPI FLASH*

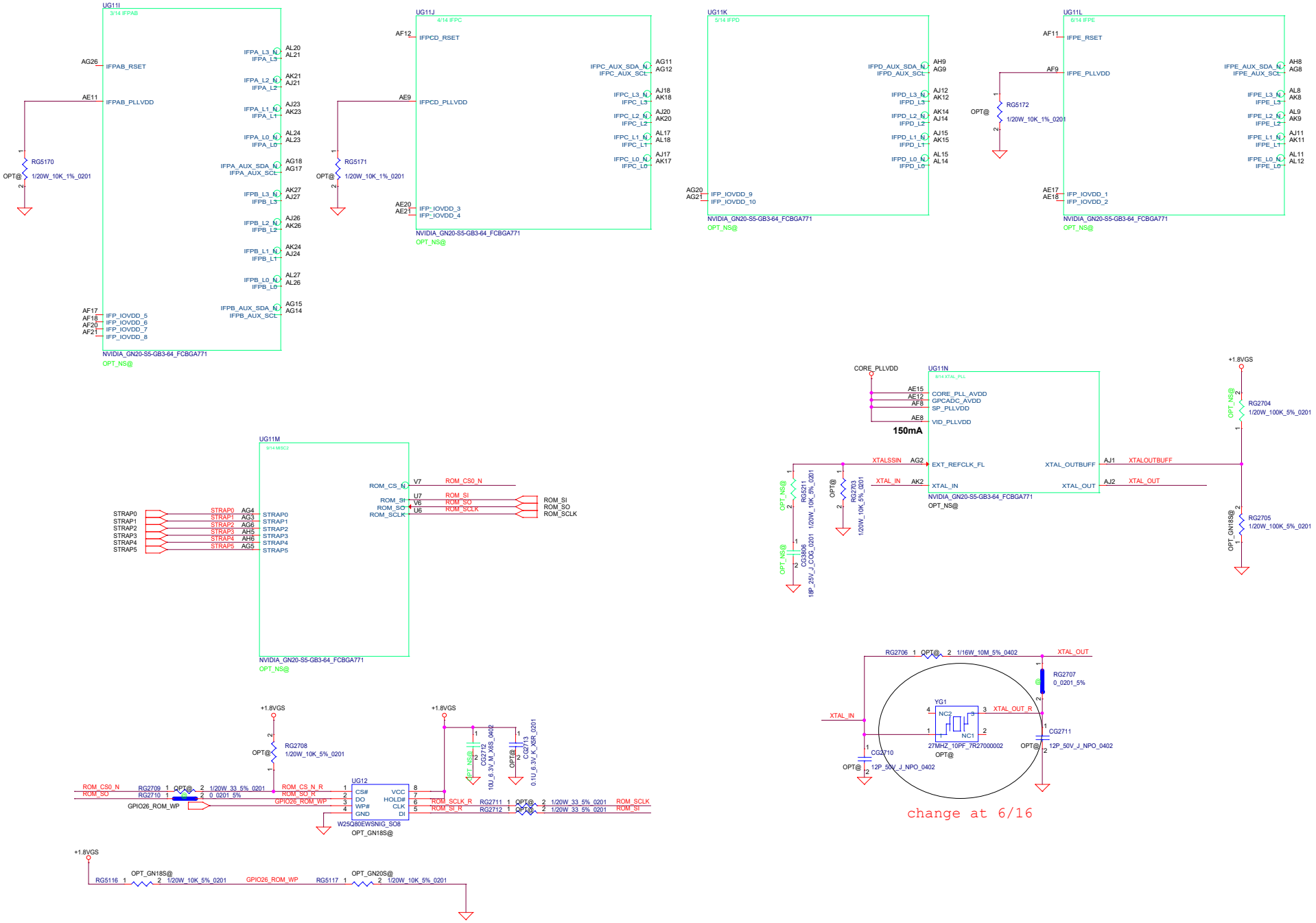
Size	Document Number	Rev
C	E14/E15 NM-E211	0.1

Date: Wednesday, March 02, 2022 Sheet 27 of 108



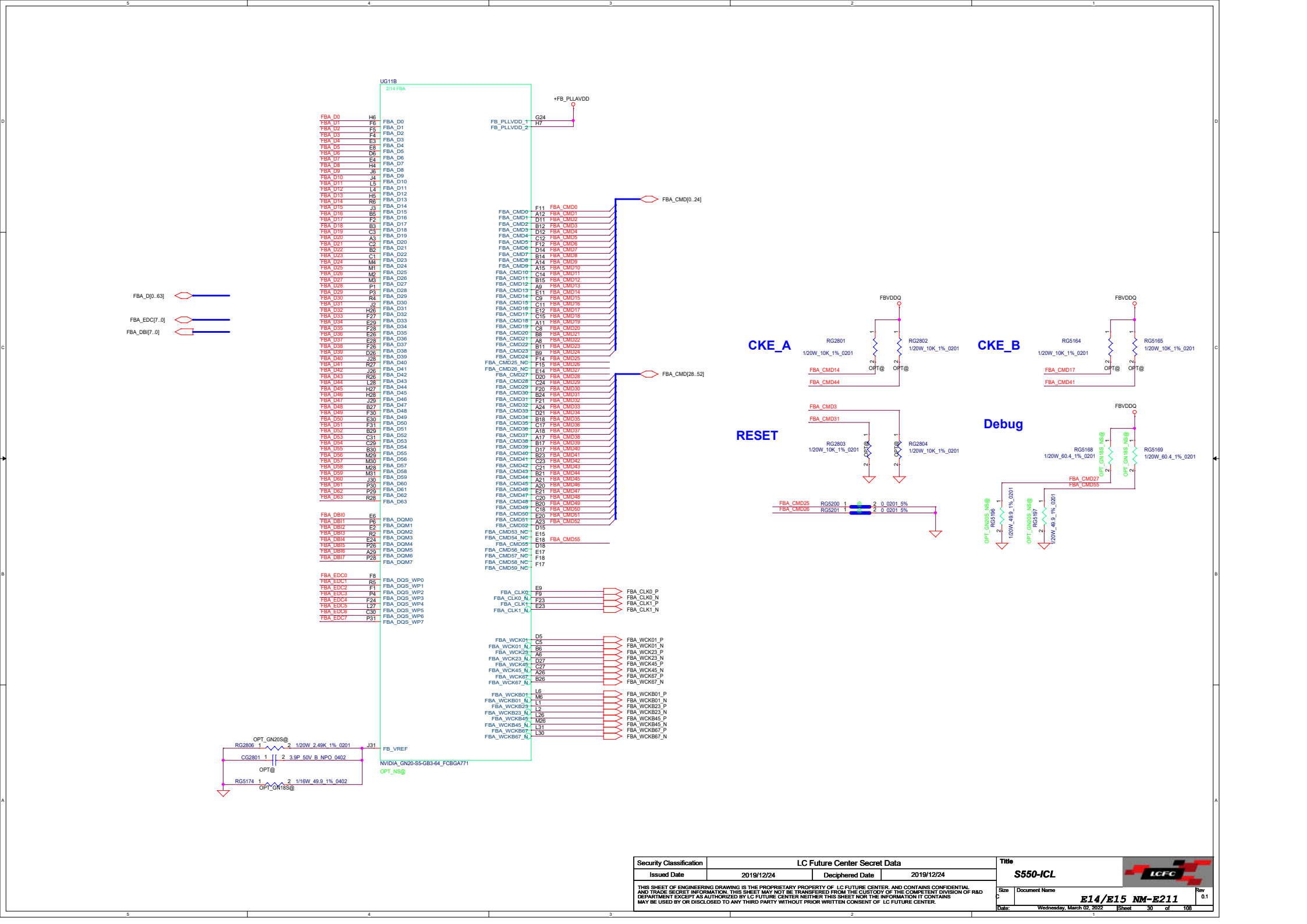
Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title	S550-ICL		
Size: C	Document Name: E14/E15 NM-E211		Rev: 0.1
Date: Wednesday, March 02, 2022	Sheet 28 of 108		



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title	S550-ICL		
Size	Document Name		Rev
C	E14/E15 NM-E211		0.1
Date:	Wednesday, March 02, 2022	Sheet	29 of 108



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title	S550-ICL		
Size	Document Name		Rev
C	E14/E15 NM-E211		0.1
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Security Classification	LC Future Center Secret Data		
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Title

S550-ICL

Size	Document Name	Rev
C	E14/E15 NM-D011	0.1

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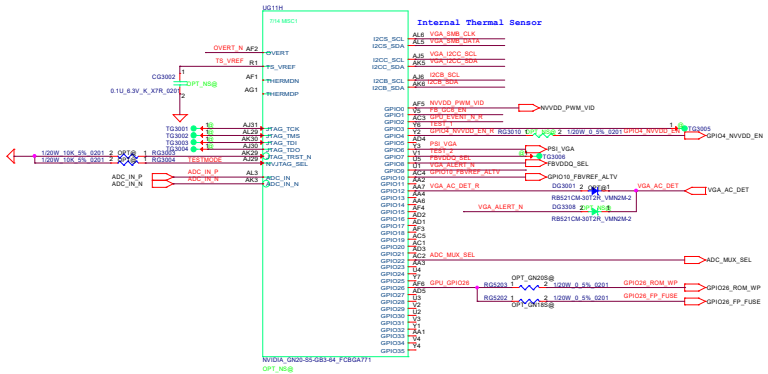
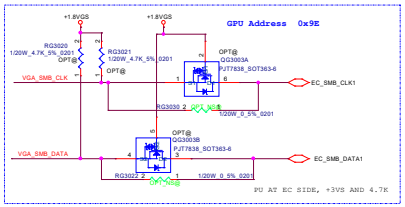
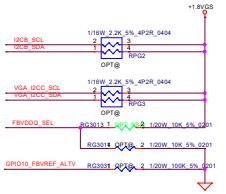
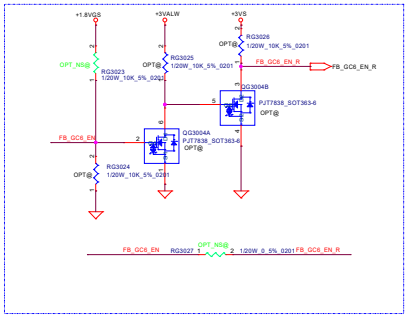
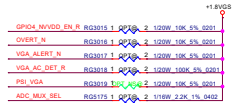
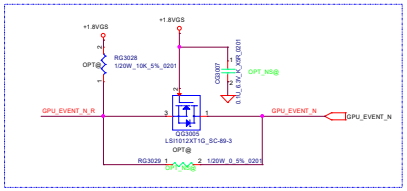


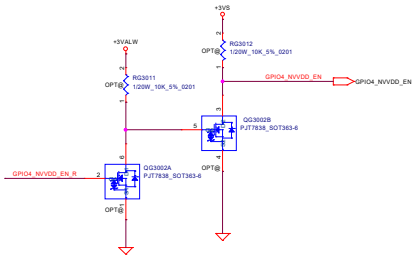


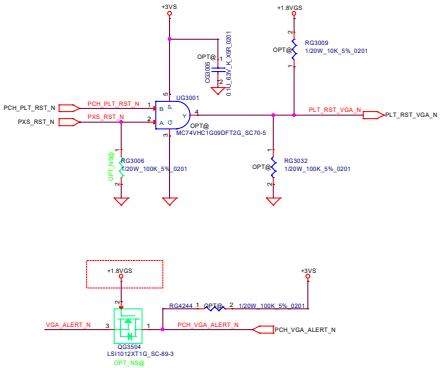




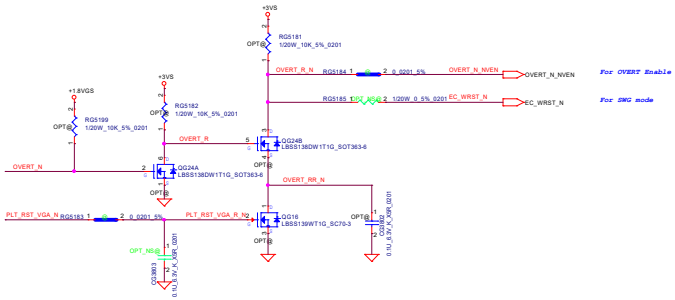








FS_OVERT# FUNCTION



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

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Title	S550-ICL		
Size	Document Name		Rev
D	E14/E15 NM-E211		0.1
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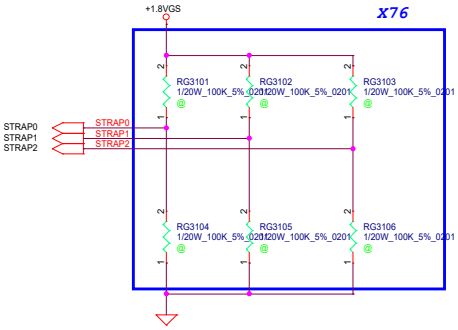
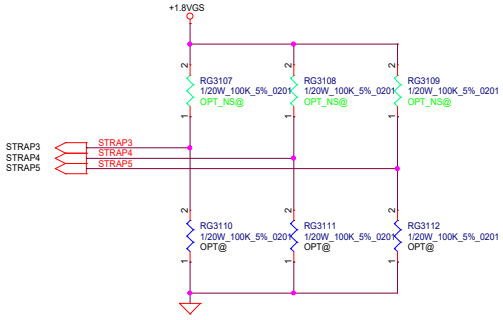


VRAMCFG

GPU VRAM	FB Memory (GDDR6)		RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
2*8Gb	Samsung 8Gb	K4Z80325BC-HC14	0x0	L	L	L
	Hynix 8Gb	H56C8H24AIR-S2C	0x2	L	H	L
	Hynix 8Gb	H56G32CS2DX005	0x5	H	L	H
2*16Gb	Samsung 16Gb	K4ZAF325BM-HC14	0x9	L	M	L
	Micron 16Gb	MT61K512M32KPA-14:C	0x7	H	H	H
	Hynix 16Gb	H56G42AS2DX014	0x8	L	L	M



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Default

1: SMB_ALT_ADDR ENABLE
0: SMB_ALT_ADDR DISABLE

1: DEVID_SEL REBRAND
0: DEVID_SEL ORIGNAL

1: PCIE_CFG LOW POWER
0: PCIE_CFG HIGH POWER

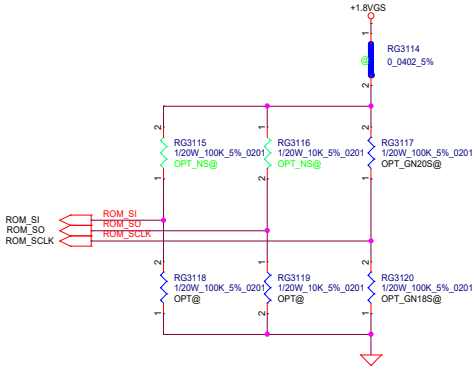
1: VGA_DEVICE ENABLE
0: VGA_DEVICE DISABLE

DEVID_SEL	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

PCIE_CFG	
0	(Default)
1	

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)



	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT*Function
GN20-S5	L	L	L	FS_OVERT*function DISABLE
	L	L	H	FS_OVERT*function ENABLE(default)

	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT*Function
GN18-S5	L	M	L	FS_OVERT*function DISABLE
	L	L	L	FS_OVERT*function ENABLE(default)

Title: S550-ICL

Size	Document Name	Rev
C	E14/E15 NM-E211	0.1

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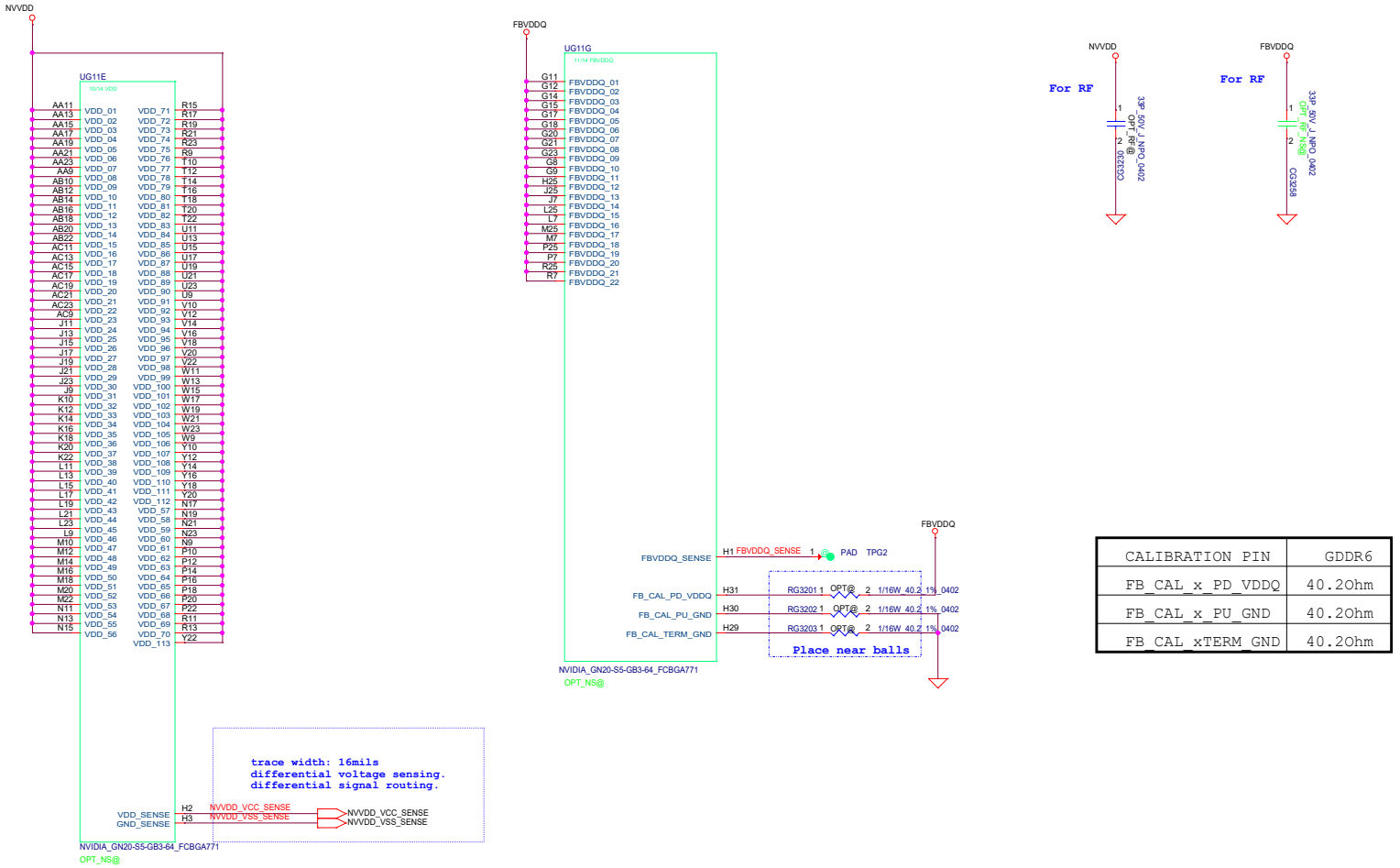

CALIBRATION PIN	GDDR6
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	40.2Ohm

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: S550-ICL

Size	Document Name	Rev
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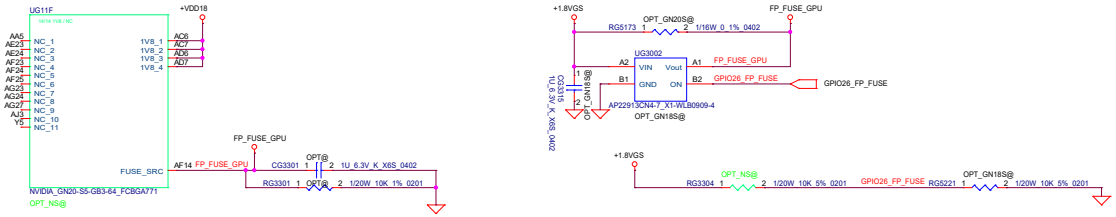
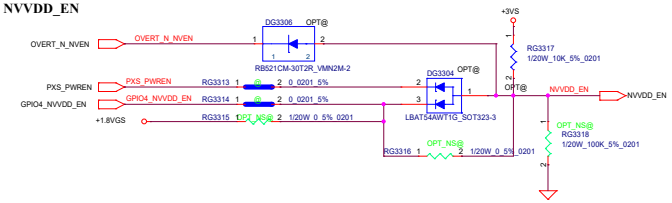
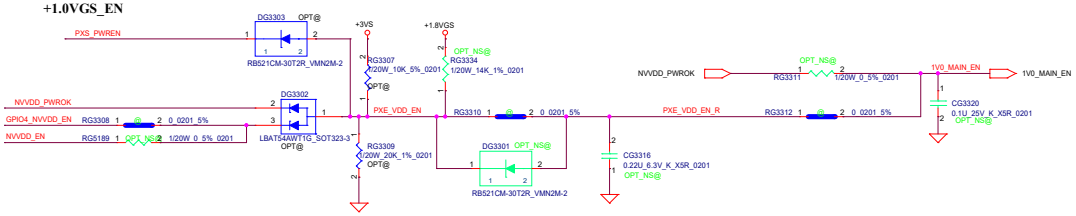


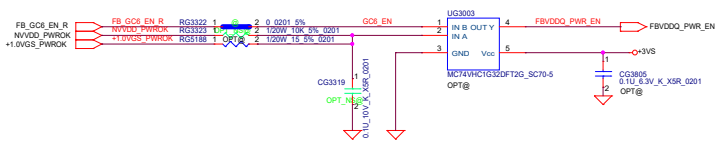
NVVDD_EN



+1.0VGS_EN

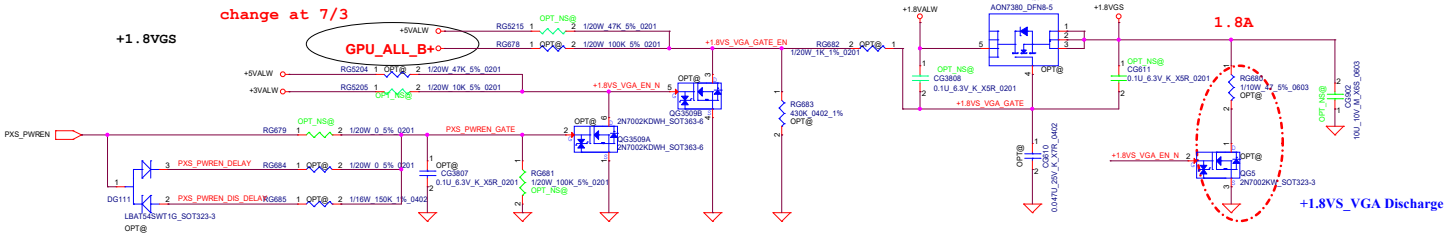


FBVDDQ_PWR_EN



+1.8VGS

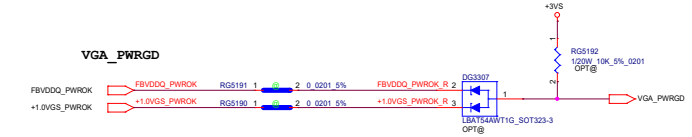
change at 7/3



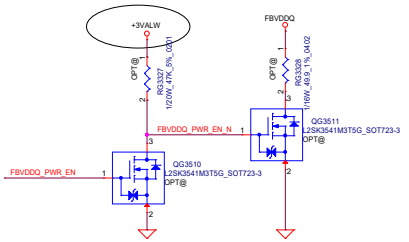
1.8A

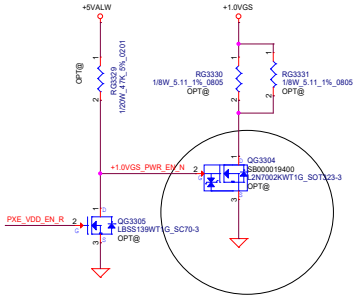
+1.8VS_VGA Discharge

VGA_PWRGD

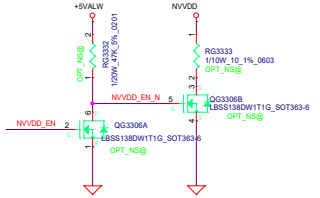


change at 7/3 Discharge





change at 7/1



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: S550-ICL

Size: Custom | Document Name: E14/E15 NM-D011 | Rev: 0.1

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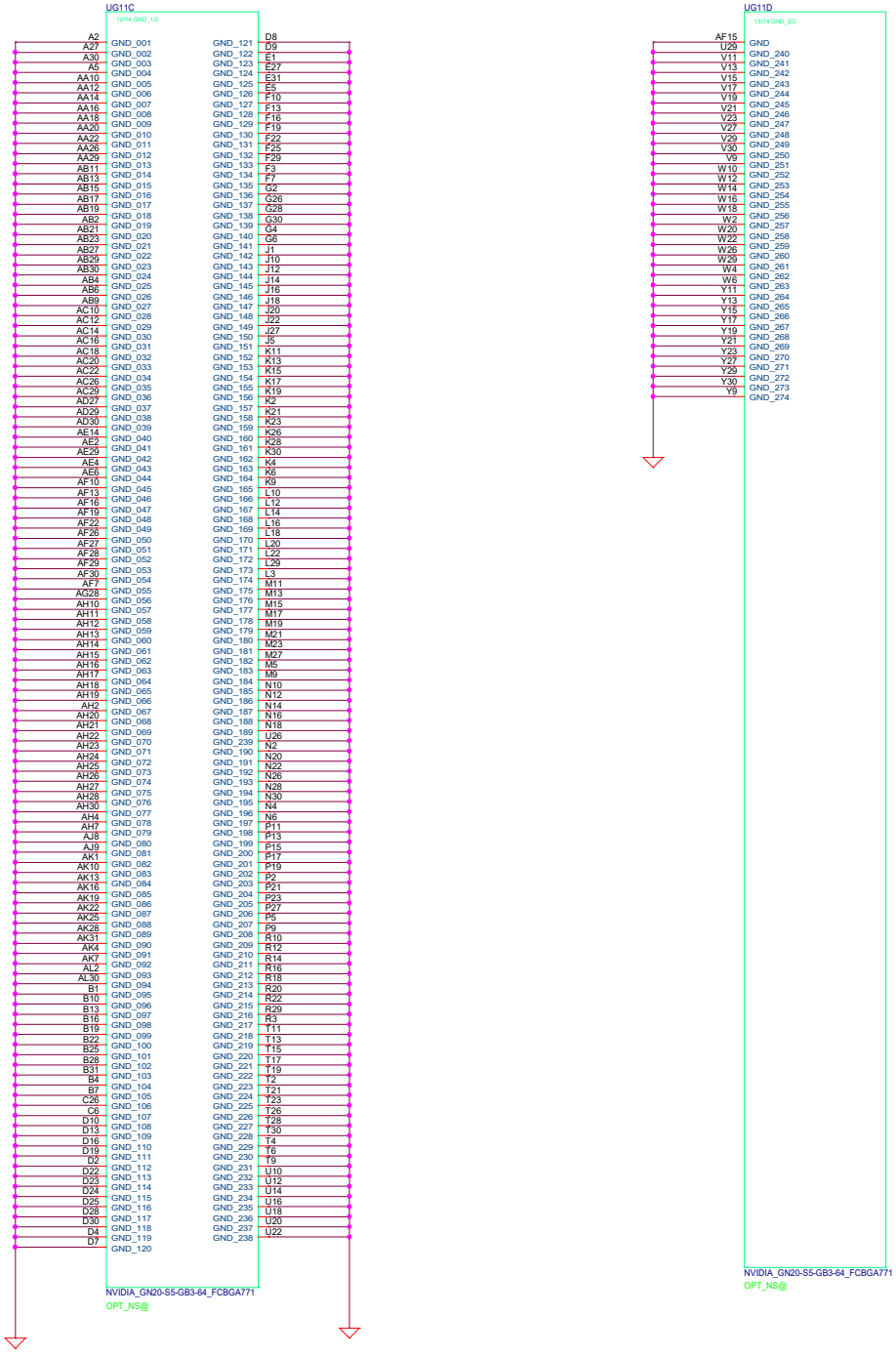


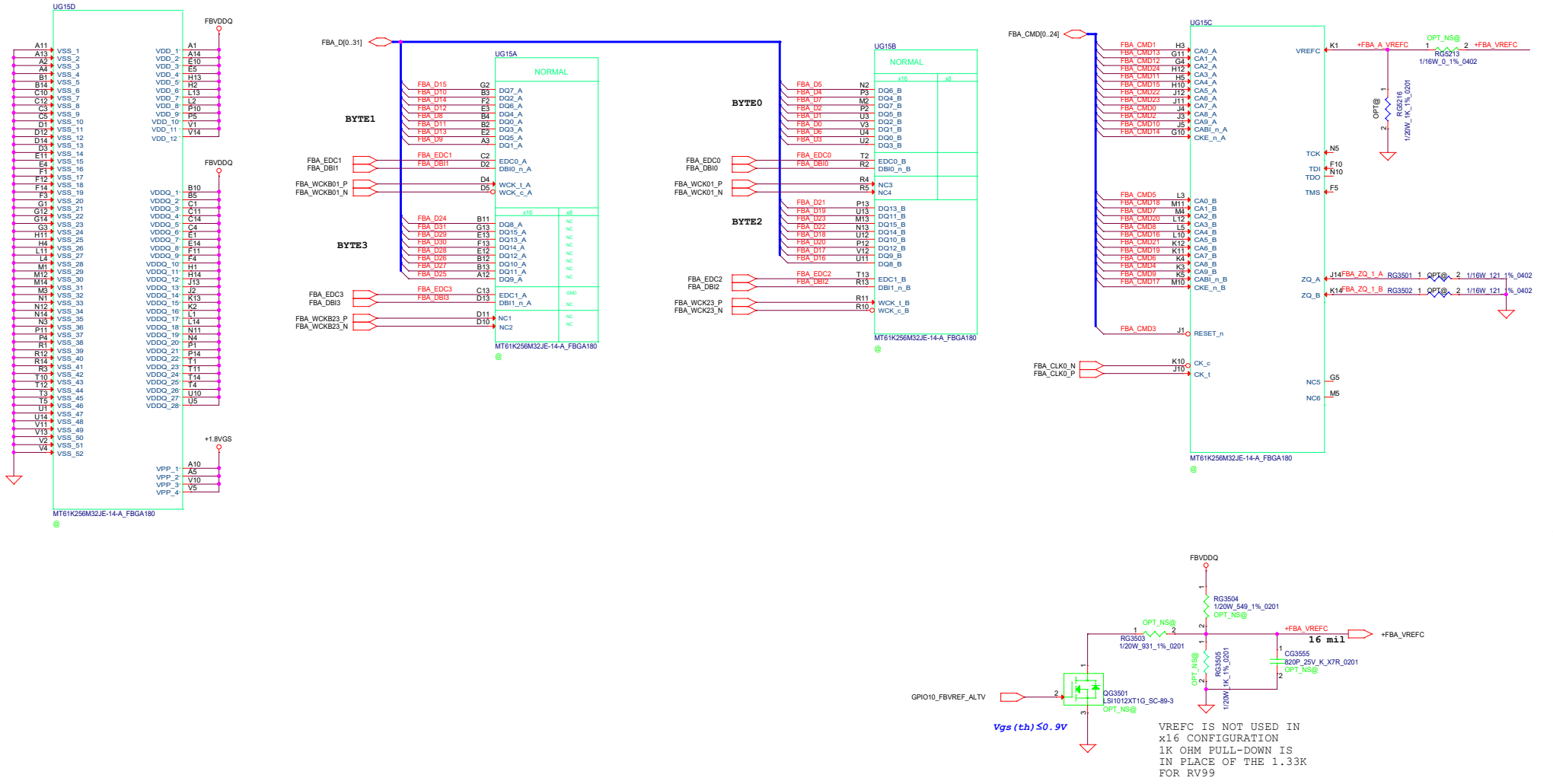
Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: **S550-ICL**

Size	Document Name	Rev
C	E14/E15 NM-D011	0.1

Date: Wednesday, March 02, 2022 Sheet 36 of 108

GN20-S5/GN18-S5_GDDR6_A_[31_0]



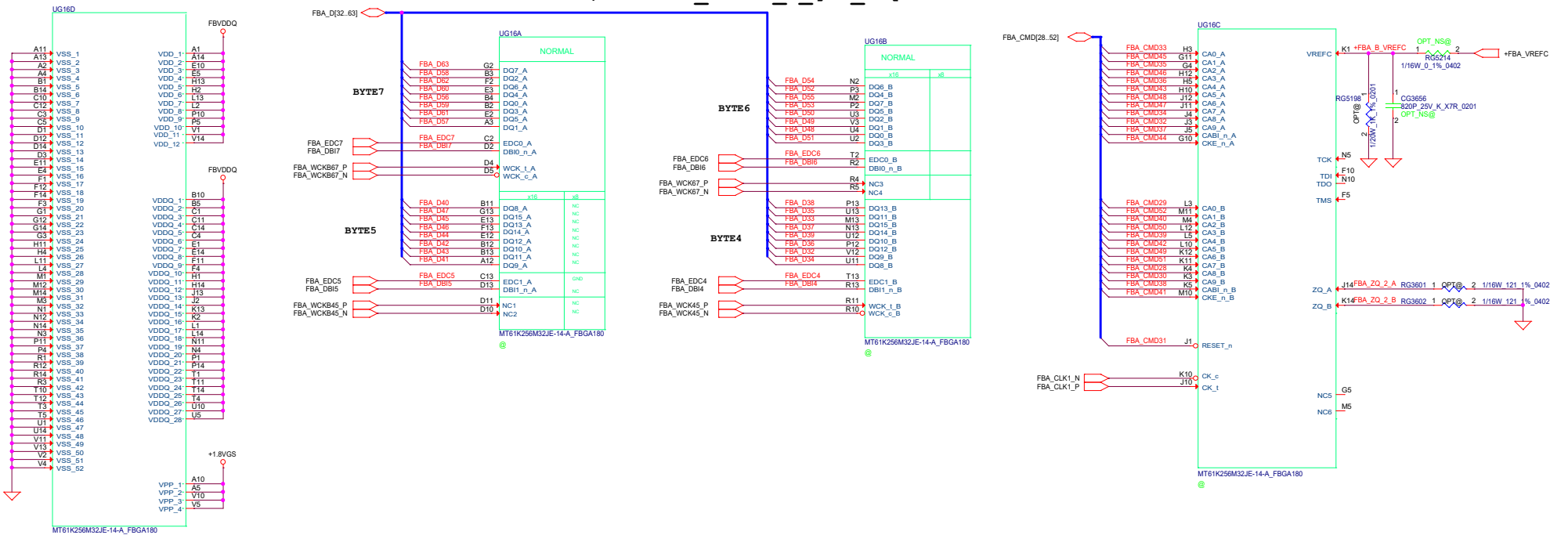
Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: S550-ICL

Size	Document Name	Rev
C	E14/E15 NM-D011	0.1

Date: Wednesday, March 02, 2022 Sheet 37 of 108

GN20-S5/GN18-S5_GDDR6_A_[63_32]



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: S550-ICL

Size	Document Name	Rev
C	E14/E15 NM-D011	0.1

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Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title

Cover Page

Size	Document Number	Rev
C	E14 GEN4 INTEL	0.1

Date: Wednesday, March 02, 2022 Sheet 39 of 108

Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title

Cover Page

Size	Document Number	Rev
C	E14 GEN4 INTEL	0.1

Date: Wednesday, March 02, 2022 Sheet 40 of 108

Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title

Cover Page

Size	Document Number	Rev
C	E14 GEN4 INTEL	0.1

Date: Wednesday, March 02, 2022 Sheet 41 of 108

Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title

Cover Page

Size	Document Number	Rev
C	E14 GEN4 INTEL	0.1

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Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title

Cover Page

Size	Document Number	Rev
C	E14 GEN4 INTEL	0.1

Date: Wednesday, March 02, 2022 Sheet 43 of 108

Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title

Cover Page

Size	Document Number	Rev
C	E14 GEN4 INTEL	0.1

Date: Wednesday, March 02, 2022 Sheet 44 of 108

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/01/19	Deciphered Date	2022/01/19

Title: *ThinkPad E14 GEN4*

LCFC

Size	Document Number	Rev
C	P045-eDP MUX	1.0

Date: Wednesday, March 02, 2022 Sheet 45 of 108

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/01/19	Deciphered Date	2022/01/19

Title: *ThinkPad E14 GEN4*

LCFC

Size	Document Number	Rev
C	P046-NV DDS LOGIC	1.0

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LCD POWER SWITCH

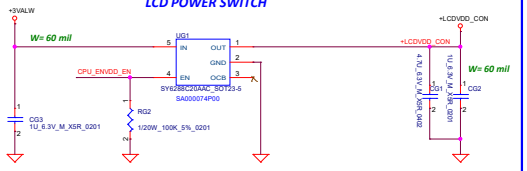
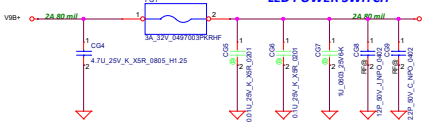
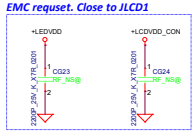


TABLE of POWER SWITCH (U1)		
Vendor	LCFC P/N	Description
SILERGY	SA000074P00	S IC SY6288C20AAC SOT23 5P POWER SWITCH
GMT	SA00007S700	S IC G5247T11U SOT-23 5P POWER SWITCH

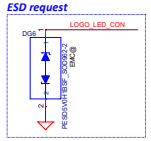
LED POWER SWITCH

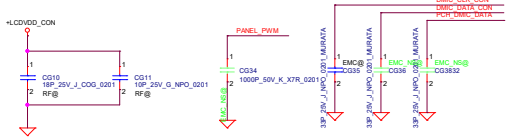


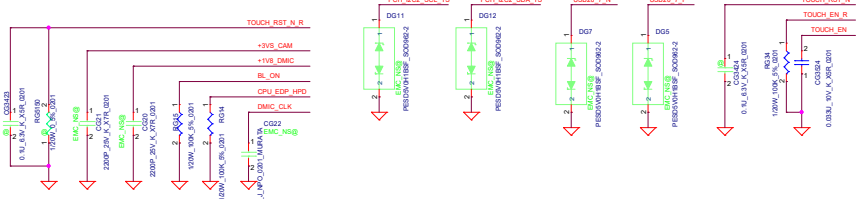
EMC requset. Close to JLCD1



ESD request

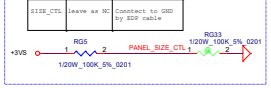




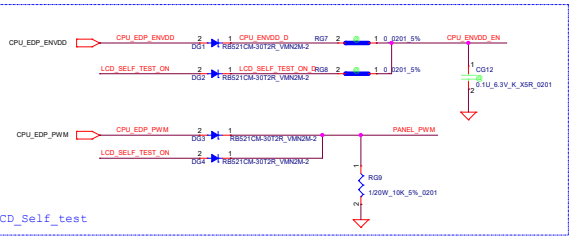


Board ID defined by EDP cable

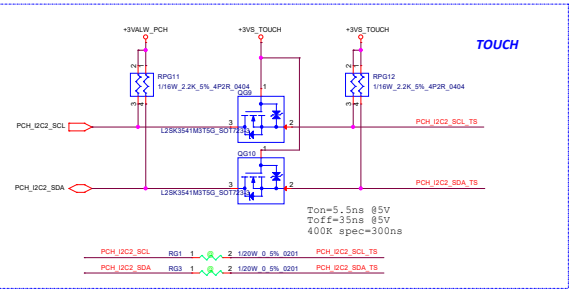
	14'	15'
SIZE_CTL	leave as NC	Connect to GND by EDP cable



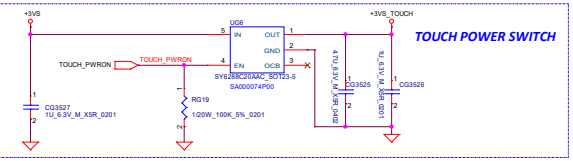
LOGO LED



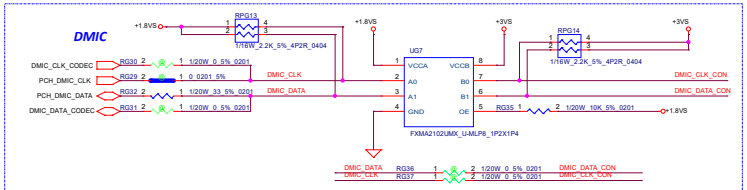
TOUCH



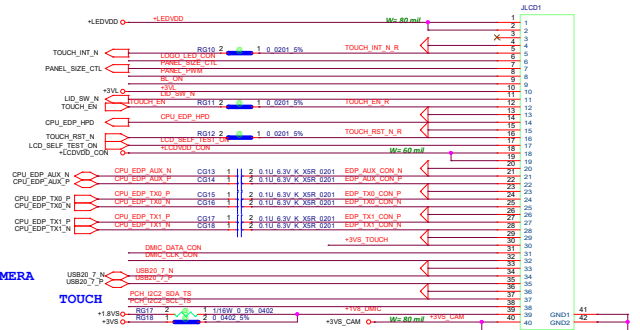
TOUCH POWER SWITCH



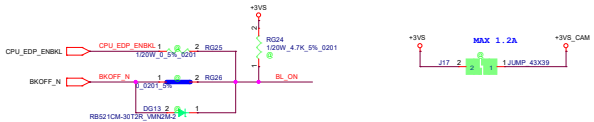
DMIC



eDP/CAMERA/DMIC/LOGO-LED CONN.



add at 2022/1/28



Title: LCD CAMERA/MIC/TOUCH SREEN

Size	Document Number	Rev
Custom	E14/E15 NM-D011	0.1

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Security Classification	LC Future Center Secret Data		
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Title

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C	E14 GEN4 INTEL	0.1

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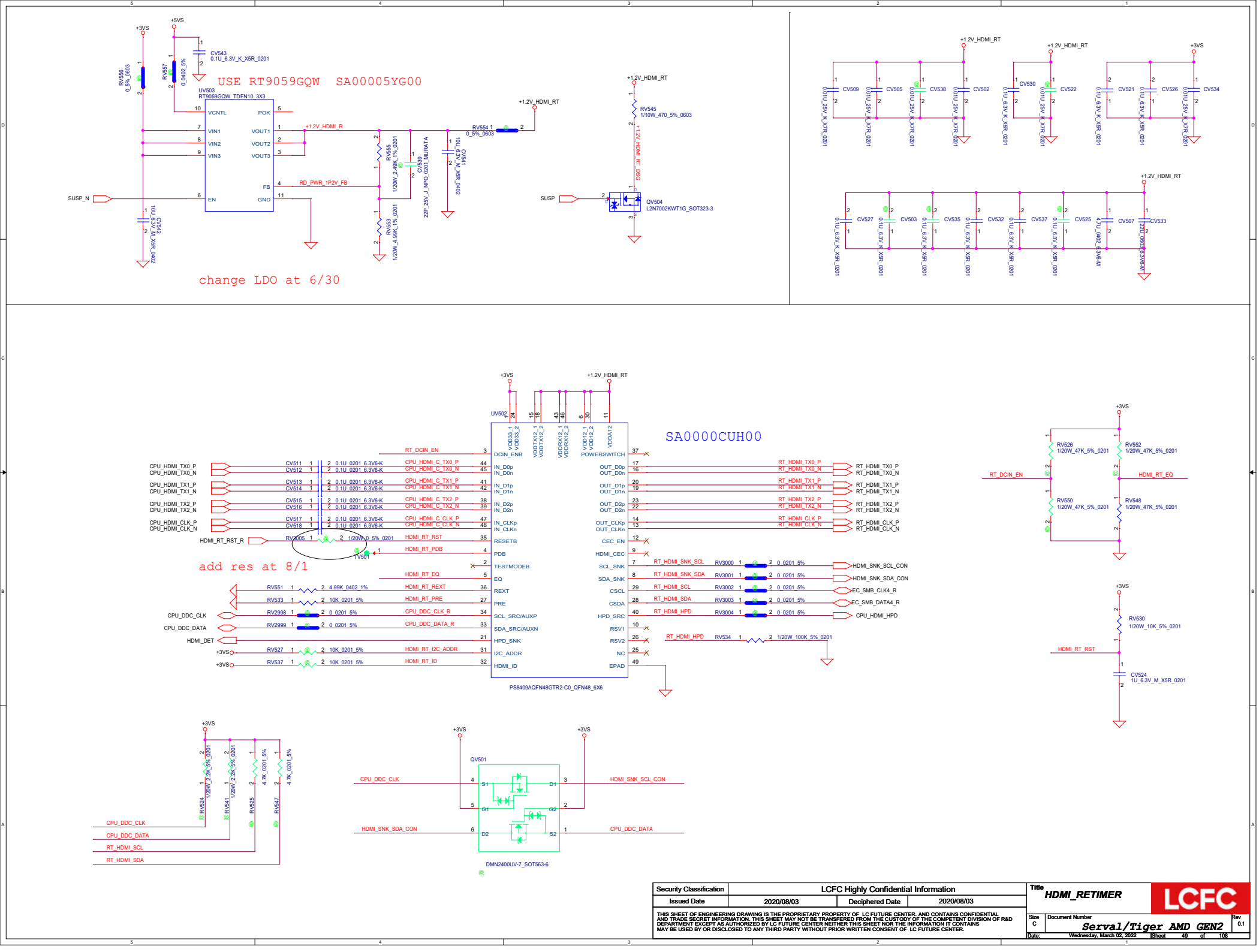

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/03	Deciphered Date	2020/08/03

Title: HDMI_RETIMER

LCFC

Size	Document Number	Rev
C	Serval/Tiger AMD GEN2	0.1

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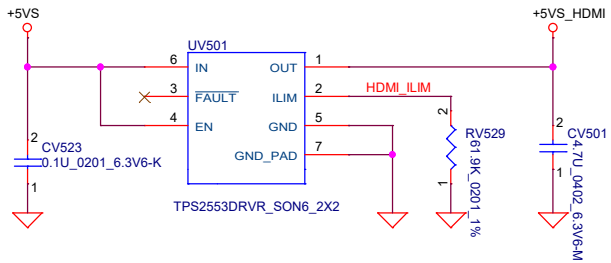
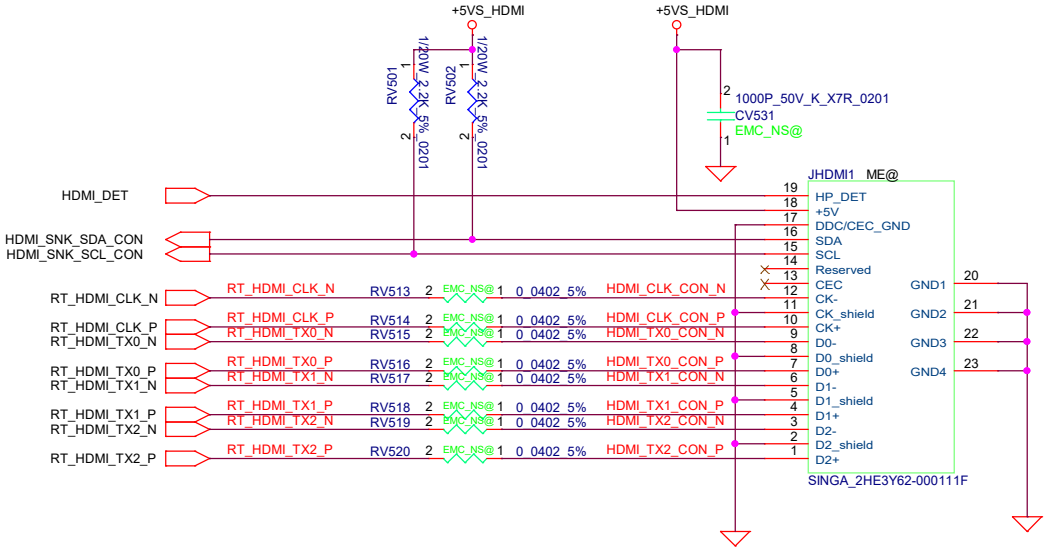
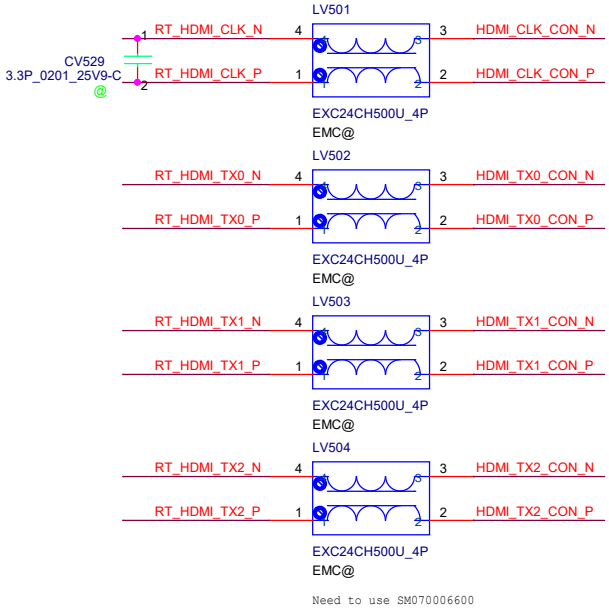
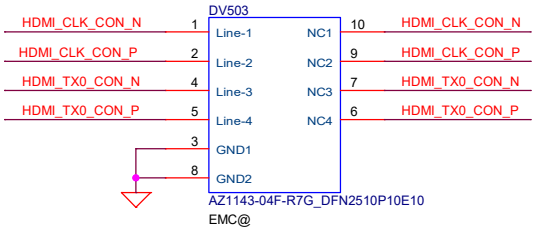
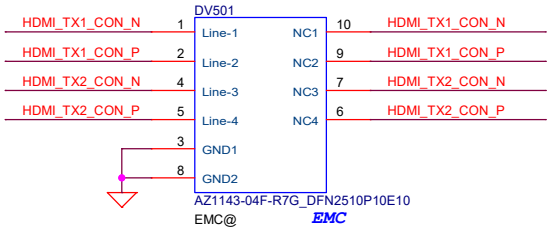
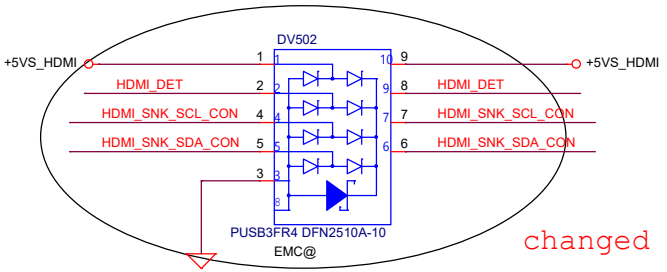








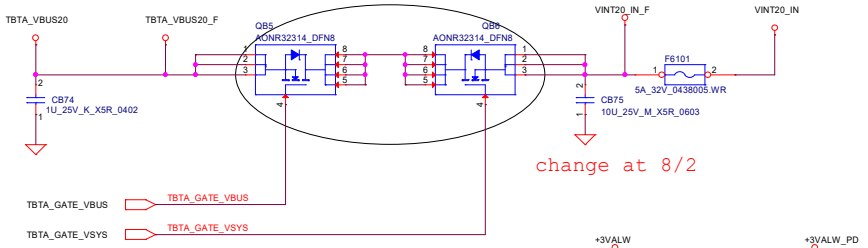




changed at 10/29

Security Classification	LCFC Highly Confidential Information		
Issued Date	2020/08/03	Deciphered Date	2020/08/03

Title	HDMI_CONN		
Size	B	Document Number	Serval/Tiger AMD GEN2
Rev	A		
Date:	Wednesday, March 02, 2022	Sheet	50 of 108



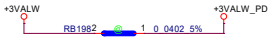
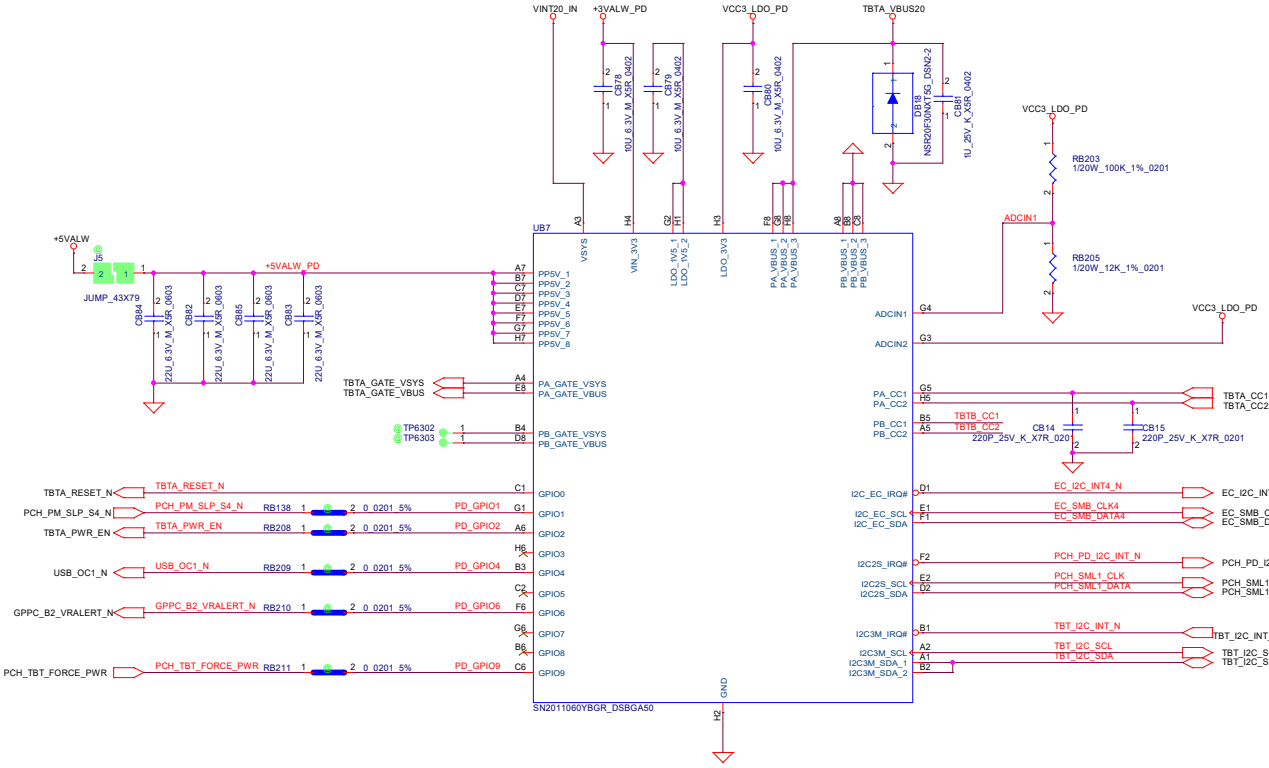
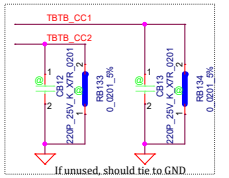
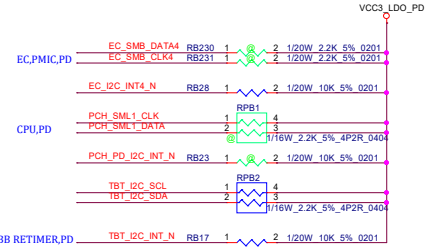


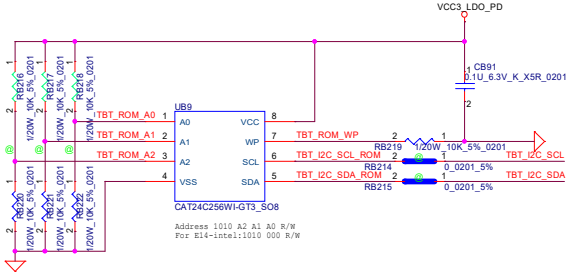
TABLE I2C Addressing

I2C1	Master: EC	TBTB PORT	0x23
	Slave: PD	TBTC PORT	0x27
I2C2	Master: PMC	TBTB PORT	0x23
	Slave: PD	TBTC PORT	0x27
I2C3	Master: PD	TBTB PORT	T.B.D.
	Slave: RT	TBTC PORT	T.B.D.









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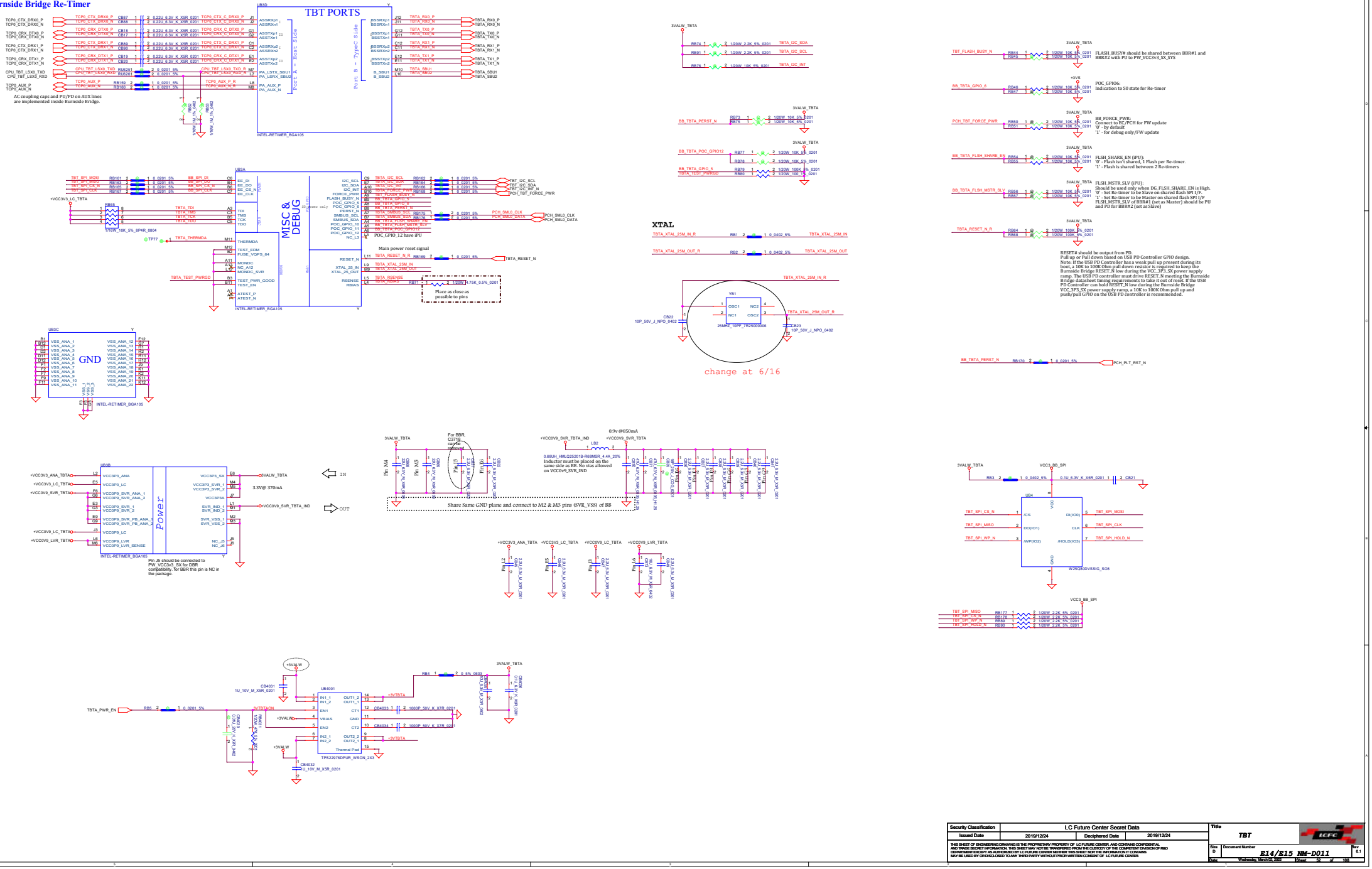
Burnside Bridge Re-Timer



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

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Title	TBT	
Size: D	Document Number: E14/E15 NM-D011	Rev: 0.1
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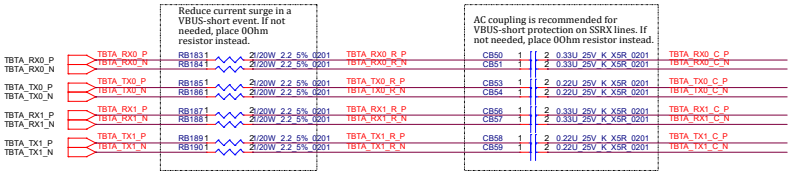

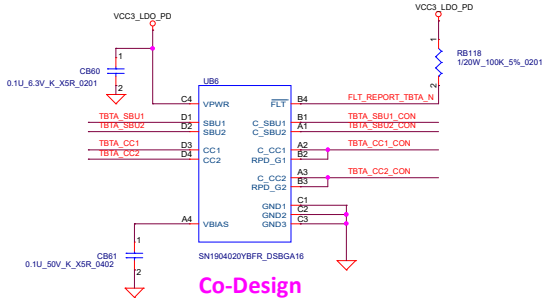

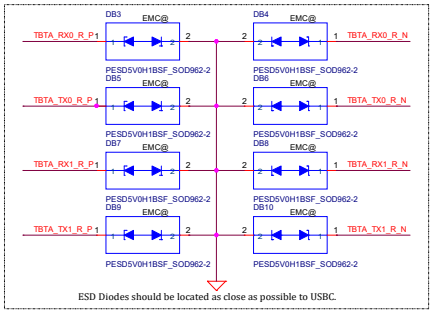

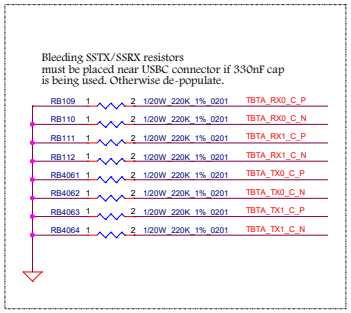

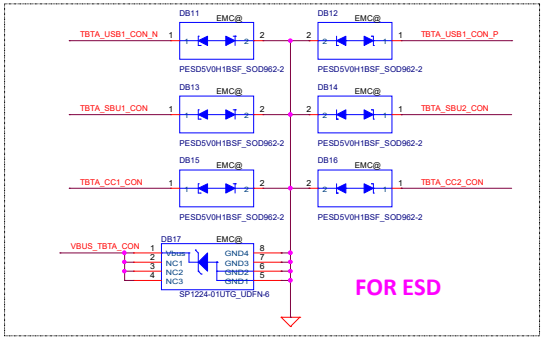

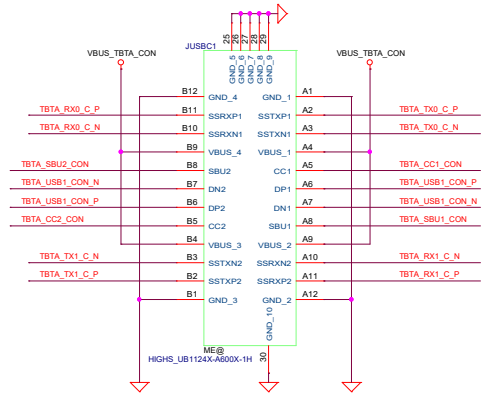

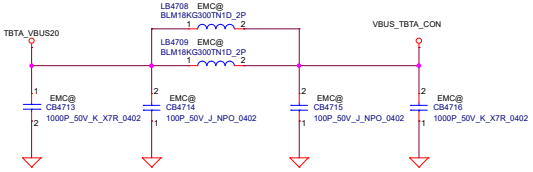

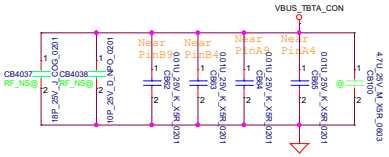

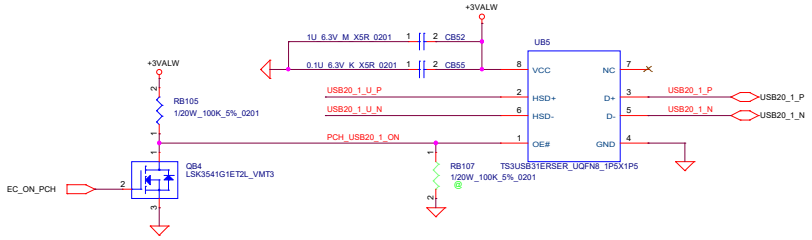

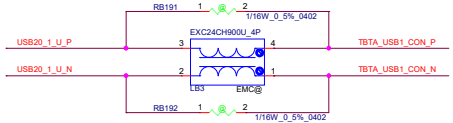

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Title	TBT		
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Title: *TBT*

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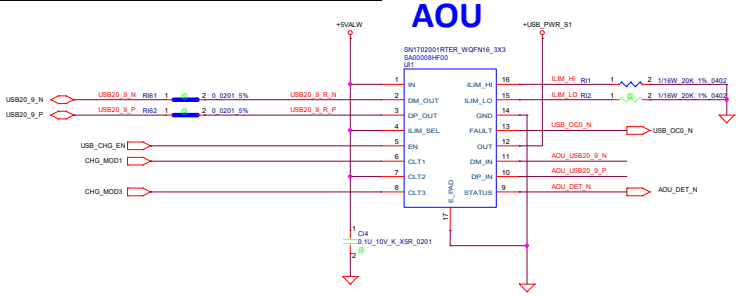
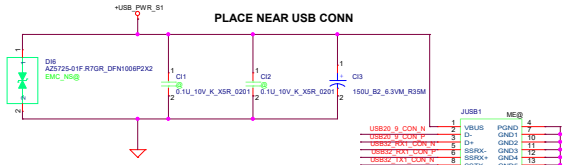
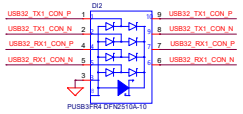
CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	**DCH**	OUT held low
1	1	1	1	**CDP**	Data Connected and Port Power Mgt. Function Active
1	1	1	0	**SDP2**	Data Connected
1	1	0	X	**SDP1**	Data Connected
0	1	0	X	**SDP1**	Data Connected
1	0	0	X	**DCP_Short**	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	**DCP_Divider**	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	**DCP_Auto**	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	**DCP_Auto**	Data Disconnected and Power Wake Function Active

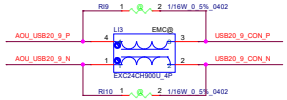
AOU

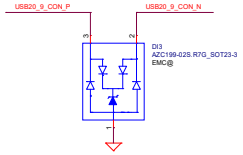




debug circuit delete at 6/21







Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: **USB TYPE-A CONNECTOR**

Size: Custom | Document Number: **E14/E15 NM-D011** | Rev: 0.1

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Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/01/19	Deciphered Date	2022/01/19

Title: *ThinkPad E14 GEN4*

LCFC

Size: B	Document Number: *P060-USB HUB*	Rev: 1.0
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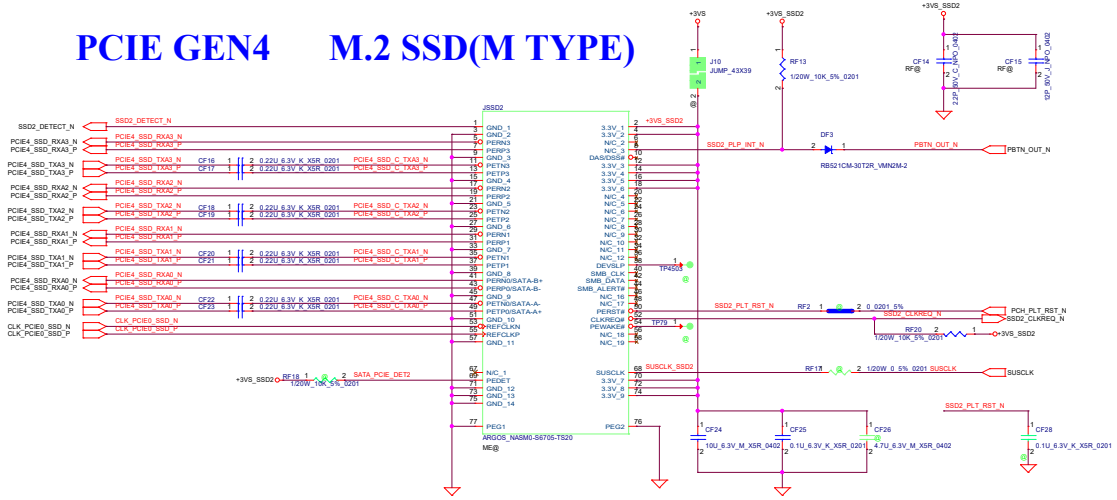
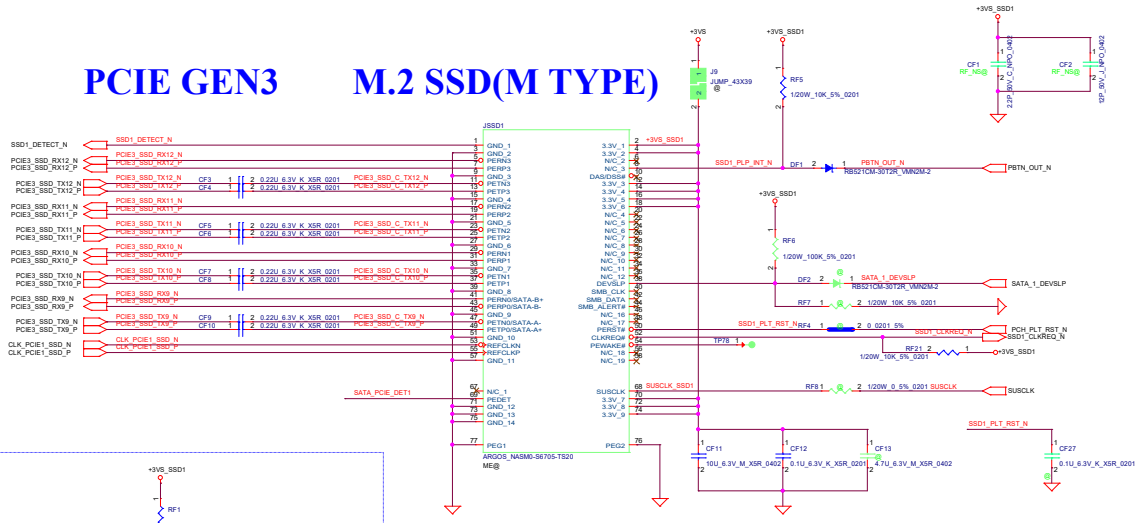
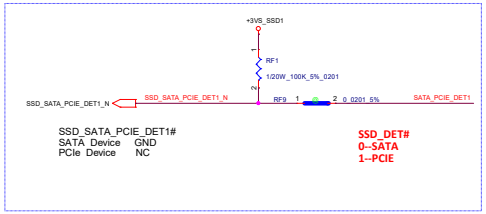
PCIE GEN4 M.2 SSD(M TYPE)



PCIE GEN3 M.2 SSD(M TYPE)





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Issued Date	2019/12/24	Deciphered Date	2019/12/24

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Title: M.2 SOCKET PCIE GEN4 MODULE

Size: Custom | Document Number: E14/E15 NM-D011 | Rev: 0.1

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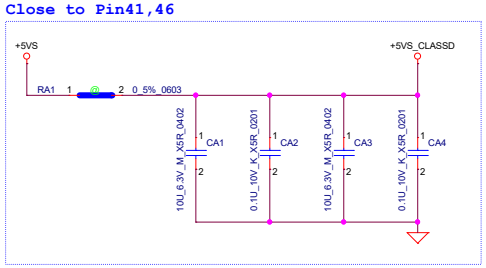
Close to Pin41,46



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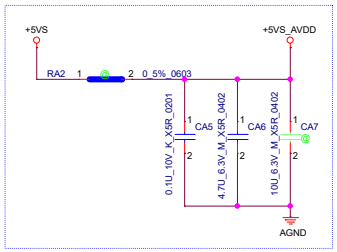
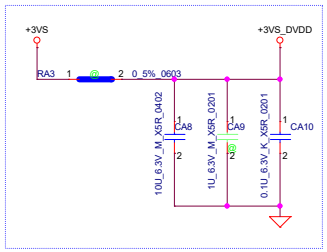
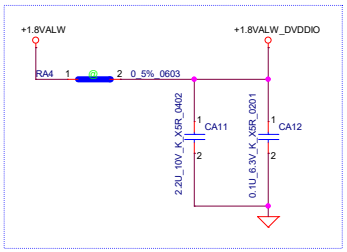


Please Close to Pin3



Close to Pin18



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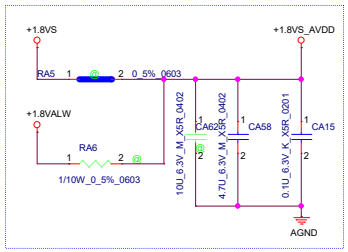
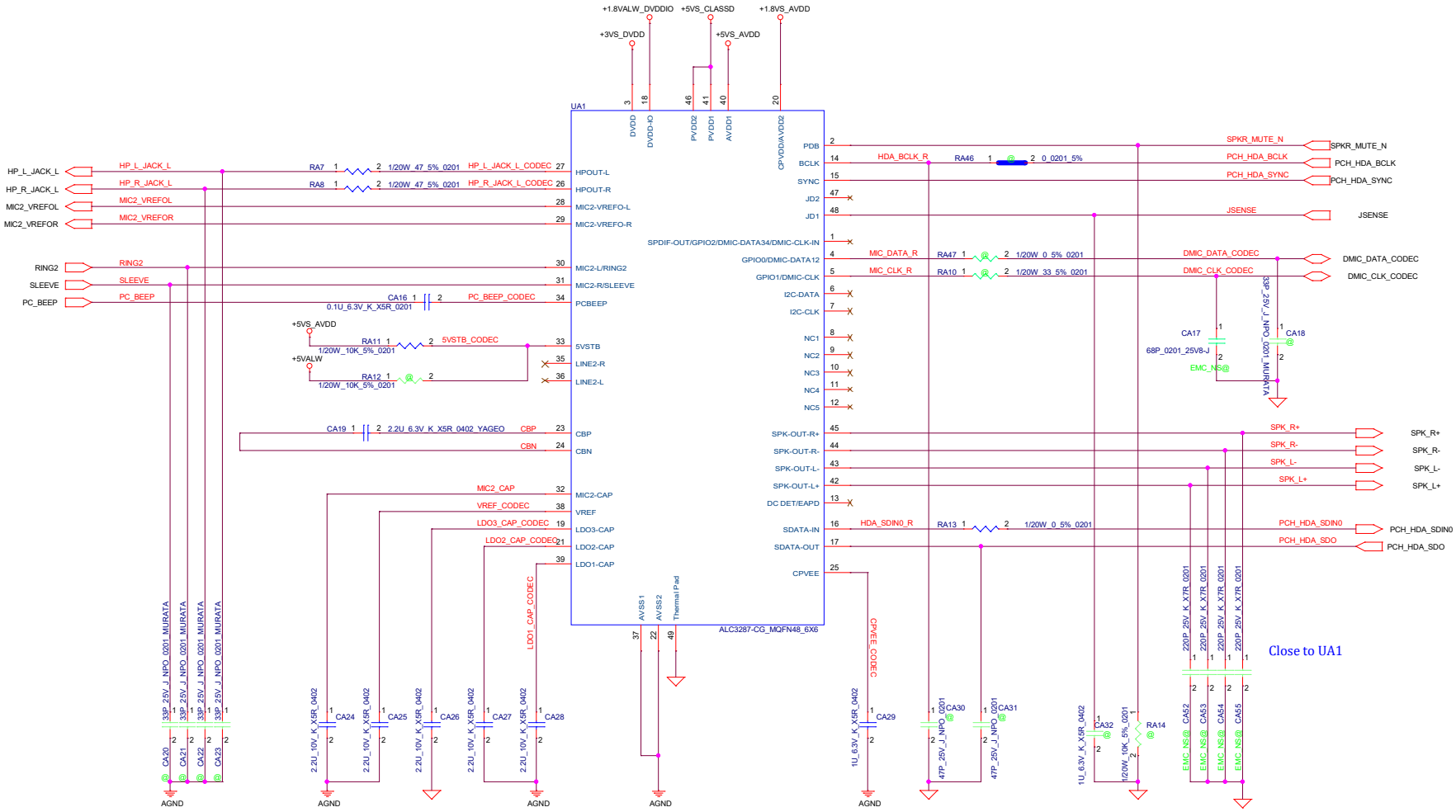
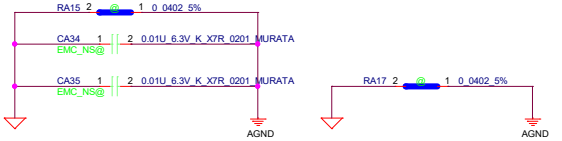




PLACE UNDER ALC3287



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: **AUDIO**

Size	Document Number	Rev
Custom	E14/E15 NM-E211	0.1
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Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title

Cover Page

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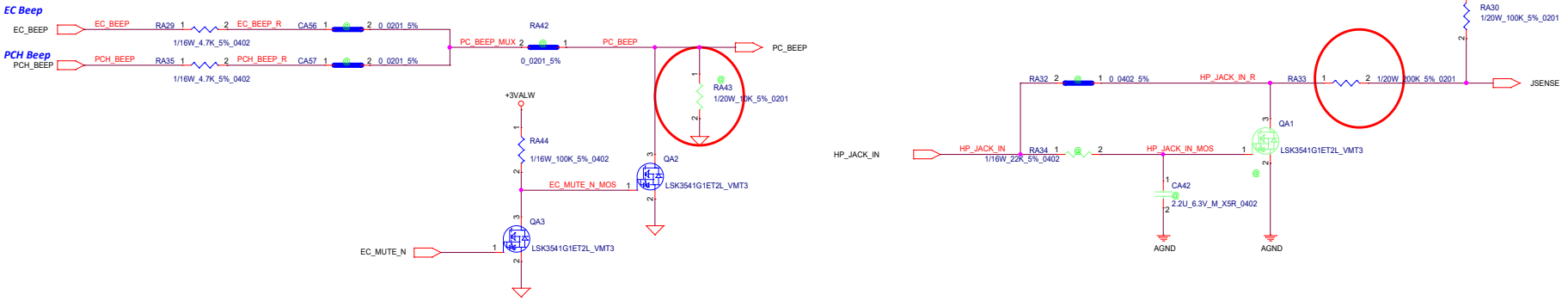
PC Beep



Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

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Size	Document Number		Rev
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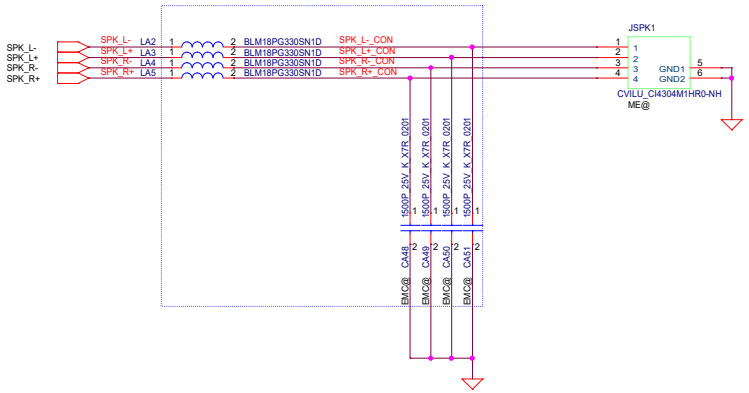
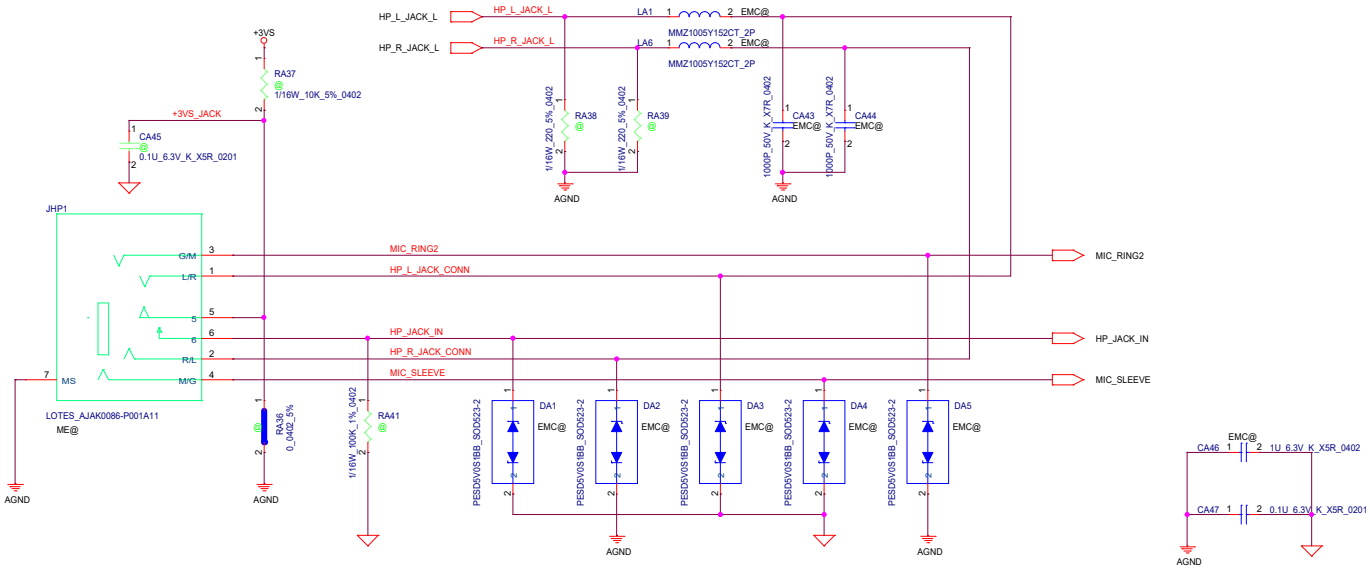
SPK CONN.





Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title	AUDIO		
Size	Document Number		Rev
C	E14/E15 NM-E211		0.1
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Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title: NA

Size	Document Number	Rev
B	E14/E15 NM-E211	0.1

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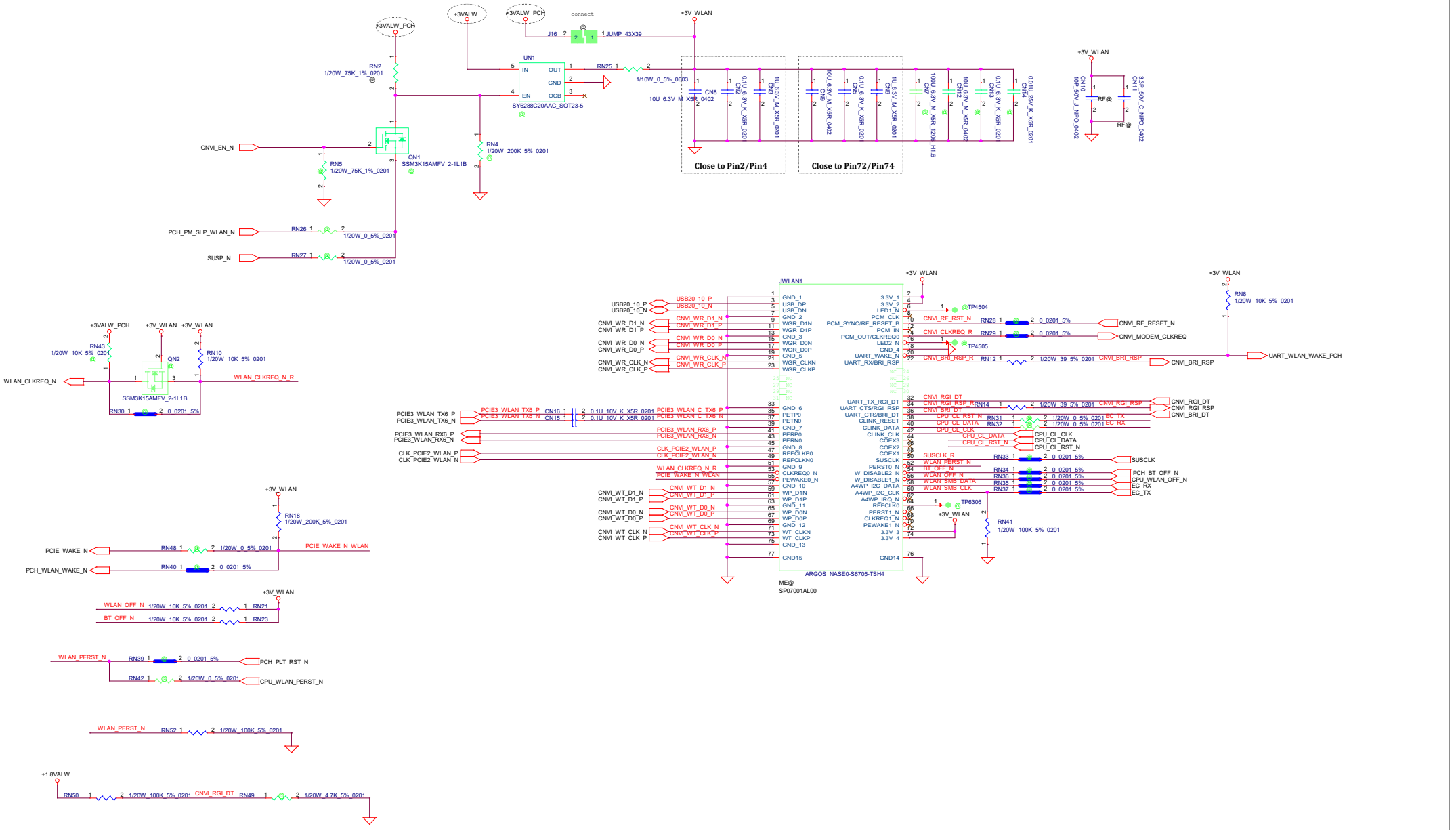
Mini-Express Card(WLAN/WiMAX)



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: **WLAN NGFF CONN.**

Size: Custom | Document Number: **E14/E15 NM-E211** | Rev: 0.1

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Security Classification	LC Future Center Secret Data		
Issued Date	2021/03/18	Deciphered Date	2021/03/18

Title: NA

Size	Document Number	Rev
B	E14/E15 NM-E211	0.1

Date: Wednesday, March 02, 2022 Sheet 72 of 108

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Title

NA

Size	Document Number	Rev
B	*E14/E15 NM-E211*	0.1

Date: Wednesday, March 02, 2022 Sheet 73 of 108

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Title

NA

Size	Document Number	Rev
B	*E14/E15 NM-E211*	0.1

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Title

NA

LCFC

Size	Document Number	Rev
B	*E14/E15 NM-E211*	0.1

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APS G-Sensor

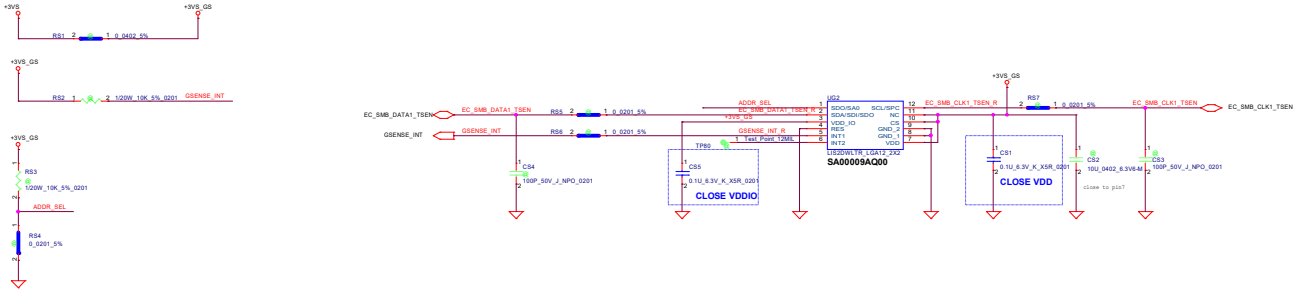
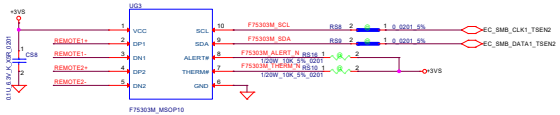


TABLE of G-Sersor (UG1)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00
BOSCH	BMA422	SA0000C1V00

TABLE

P/N	ADDR_SEL	Address
LIS2DWLTR	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)
BMA280	H	0X18
	L	0X19

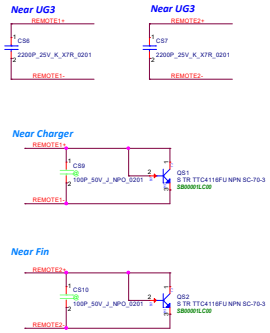
Thermal Sensor



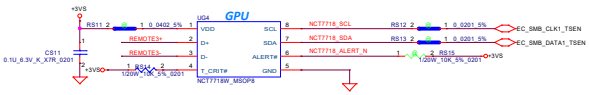
Address 1001_101xb

Internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

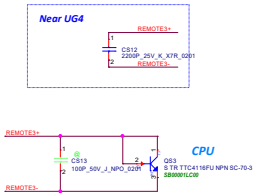
TABLE of Thermal Sensor (UTH1)		
Vendor	LCFC P/N	Description
FINTEK	SA000046C0J	S IC F75303M MSOP 10P SENSOR



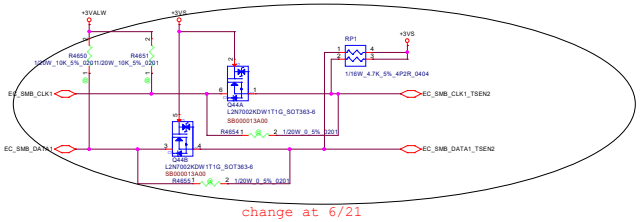
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



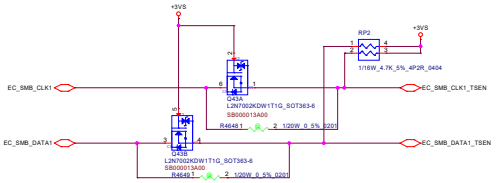
NCT7718W I2
C/ SMBusTM address is 1001100xb (x is R/W bit).



REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



change at 6/21



Security Classification	LC Future Center Secret Data		Title
Issued Date	2019/12/24	Deciphered Date 2019/12/24	APS G-SENSOR

Size	Document Number	Rev
D	E14/E15 NM-E211	0.1

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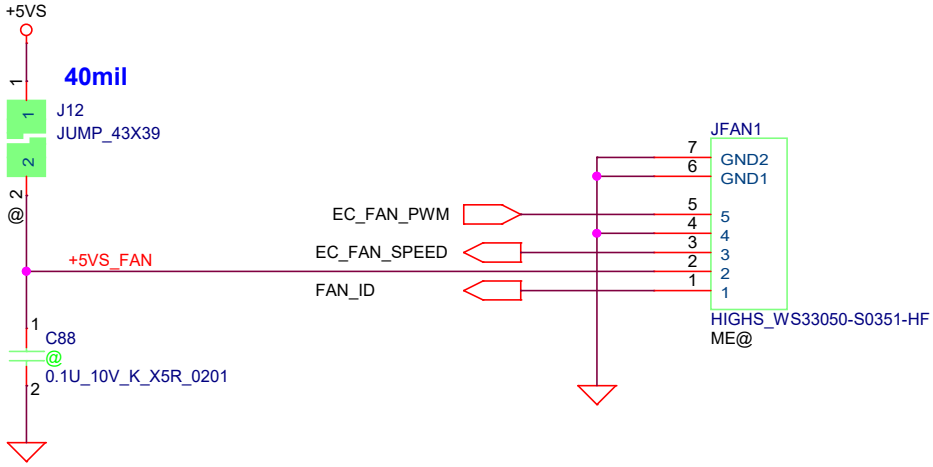

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title

FAN CONNECTOR

Size	Document Number	Rev
Custom	E14/E15 NM-E211	0.1

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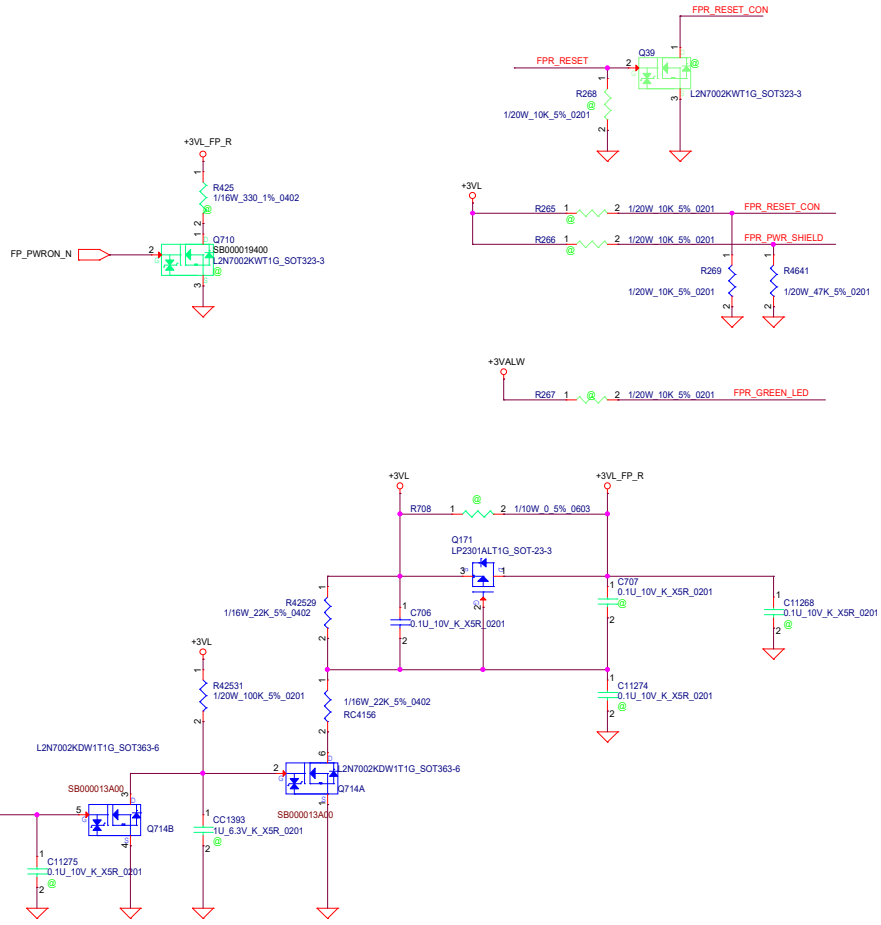
IO_44_Pin conn

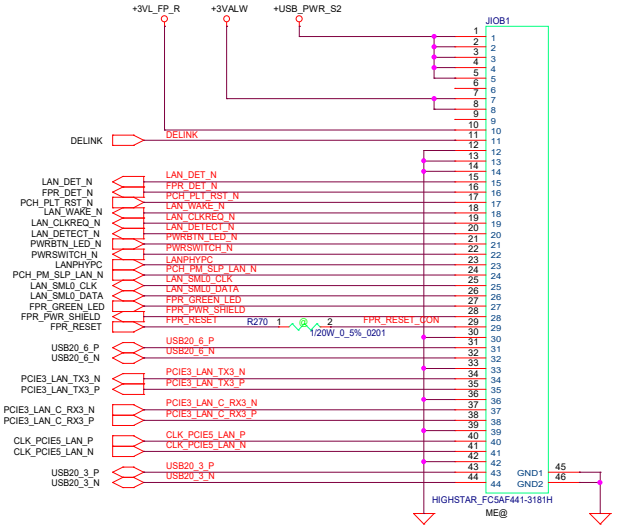


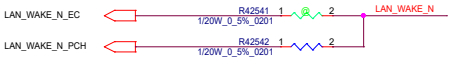
Finger Printer

CPU <-- LAN

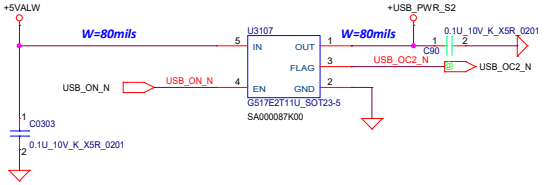
CPU --> LAN

IOB USB





USB POWER SWITCH



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: **IO BOARD CONN.**

Size	Document Number	Rev
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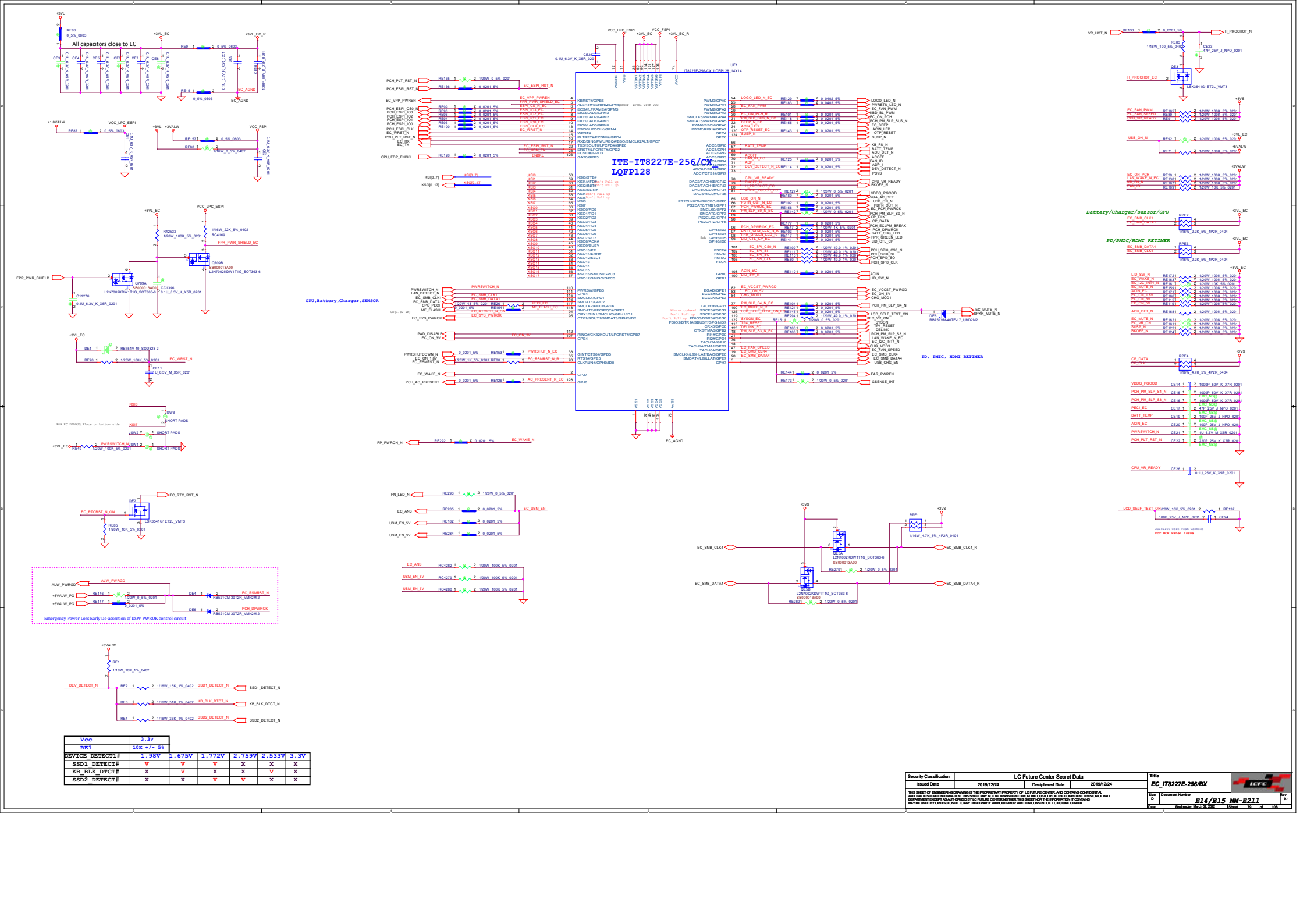

Vcc	3.3V					
R1	10K +/- 5%					
DEVICE_DETECT1#	1.98V	1.675V	1.772V	2.759V	2.533V	3.3V
SSD1_DETECT#	V	V	V	X	X	X
KB_BLK_DTCT#	X	V	X	X	V	X
SSD2_DETECT#	X	X	V	V	X	X

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: EC_IT8227E-256/BX

Size: D | Document Number: E14/E15 NM-E211 | Rev: 0.1

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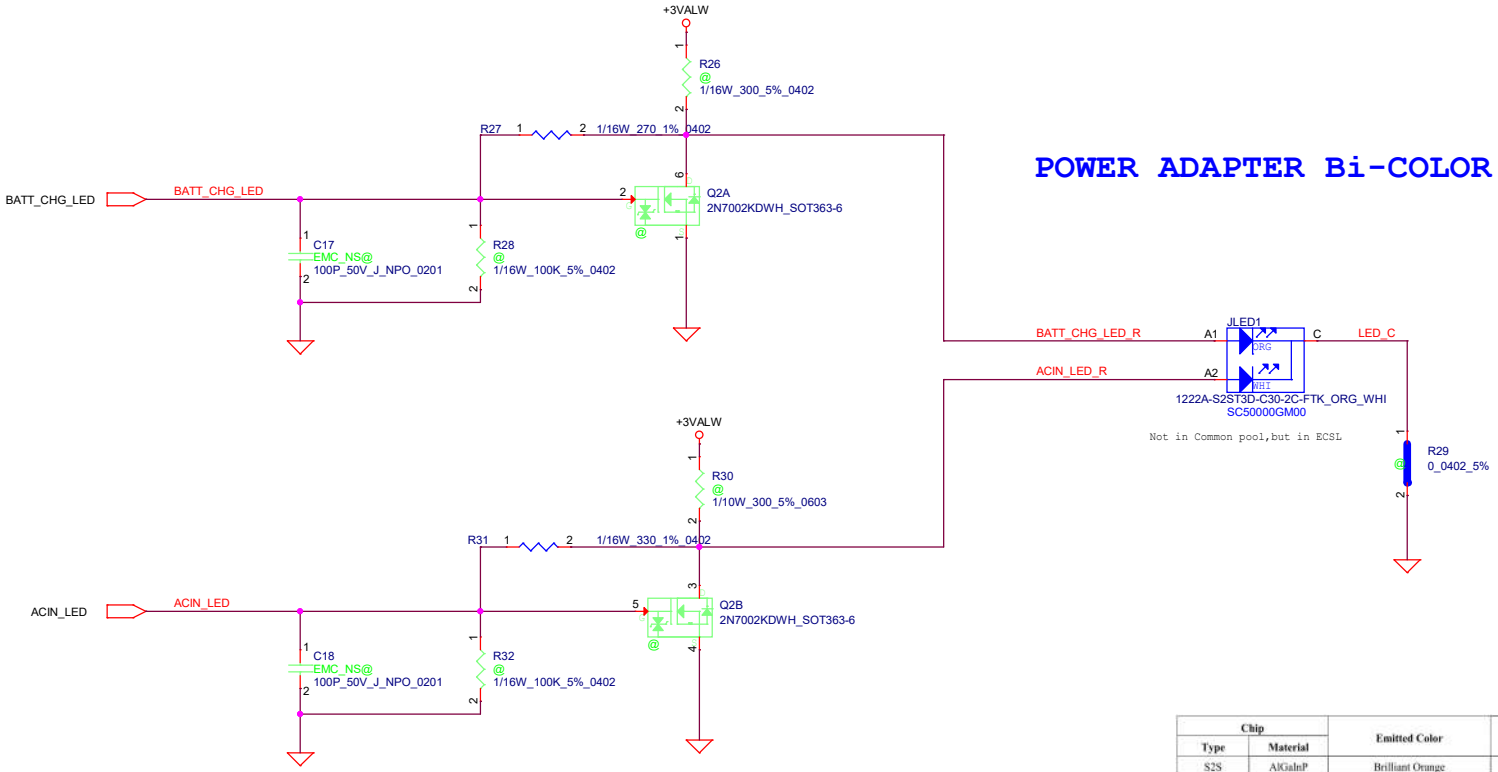

POWER ADAPTER Bi-COLOR(ORANGE/WHITE)

Chip		Emitted Color	Resin Color
Type	Material		
S2S	AlGaInP	Brilliant Orange	Yellow Diffused
T3	InGaN	Pure White	

Title: **Power LED**

Size	Document Number	Rev
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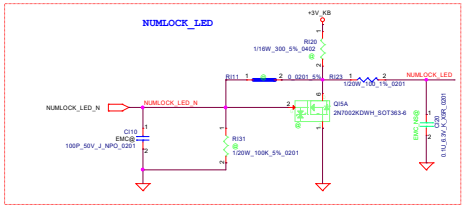
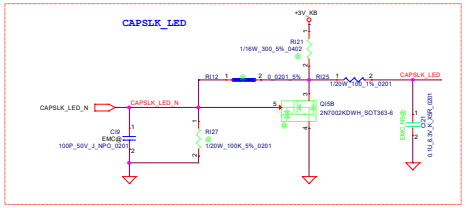
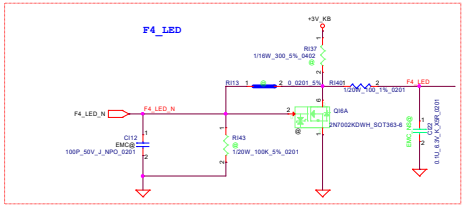
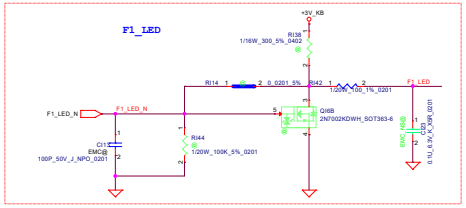
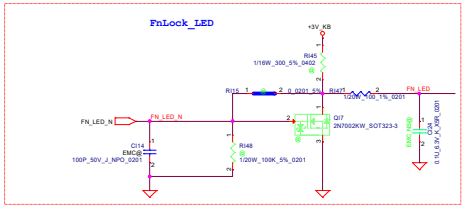
Keyboard CONN

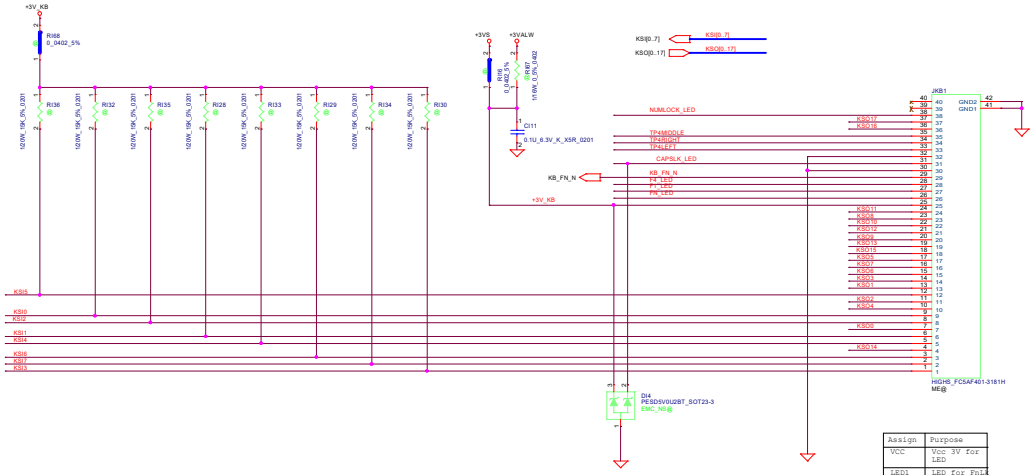










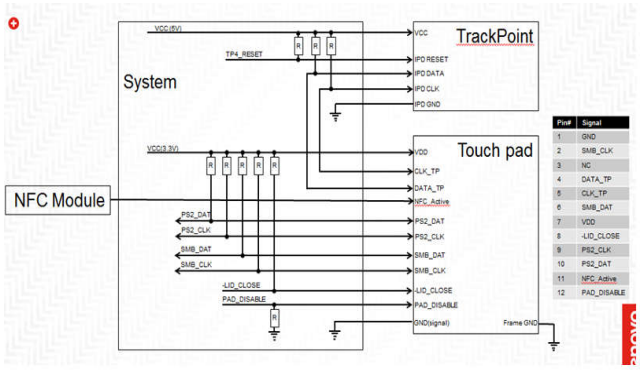


Pin#	Assign
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV0
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	VCC
26	LED1
27	LED2
28	LED3
29	HOTKEY
30	GND
31	LED4
32	MC
33	M1
34	M2
35	M3
36	DRV16
37	DRV17
38	LED5
39	NC
40	NC

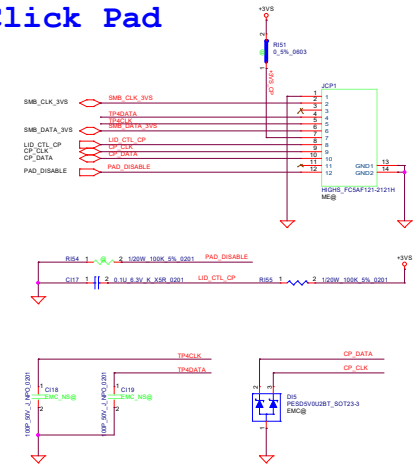
Assign	Purpose
VCC	Vcc 3V for LED
LED1	LED for FnLk
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLK
LED5	LED for NumLock

Assign	Purpose
MC	Common pin for TrackPoint click button
M1	Left button
M2	Right button
M3	Center button

Click Pad

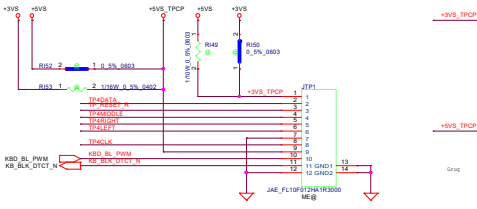


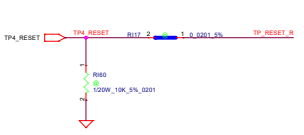
Pin#	Signal
1	GND
2	SMB_CLK
3	NC
4	DATA_TP
5	CLK_TP
6	SMB_DAT
7	VDD
8	-LID_CLOSE
9	PS2_CLK
10	PS2_DAT
11	NFC_Active
12	PAD_DISABLE

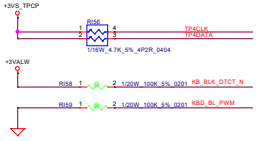


Track Point

Pin #	Assign
1	VCC5(5V)
2	TPD DATA
3	TPD RST
4	MIDDILE
5	RIGHT
6	LEFT
7	TPD GND
8	TPD CLK
9	LED VCC5 (5V)
10	LED PWM
11	BL detection
12	LED GND







Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: CP/TPOINT/KB CONN

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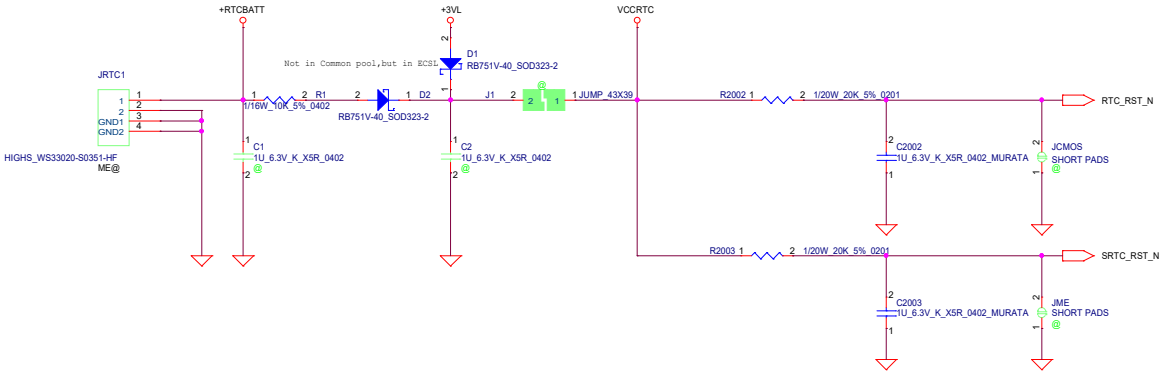
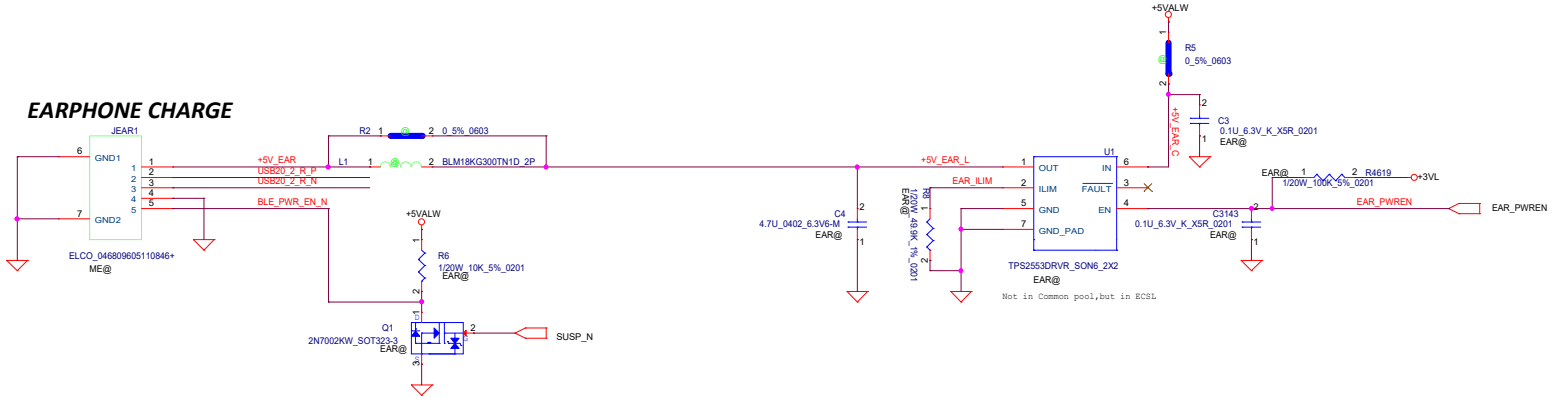
RTC BATTERY



Earphone CONN.

EARPHONE CHARGE



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: RTC BATTERY

Size	Document Number	Rev
C	E14/E15 NM-E211	0.1

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Title

AUDIO DEBUG

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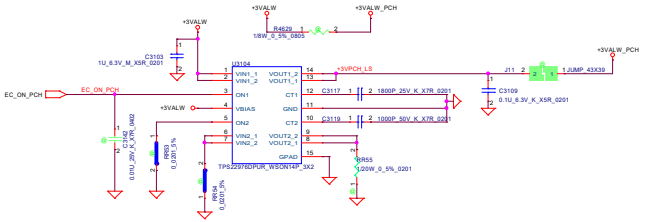
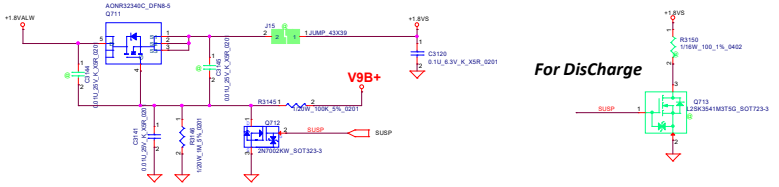
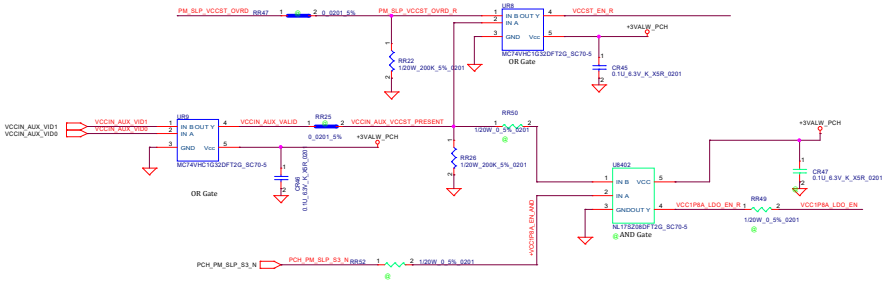
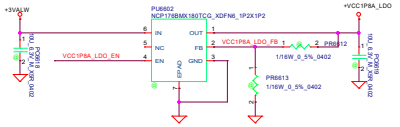
+3VALW_PCH/ +1.8VS



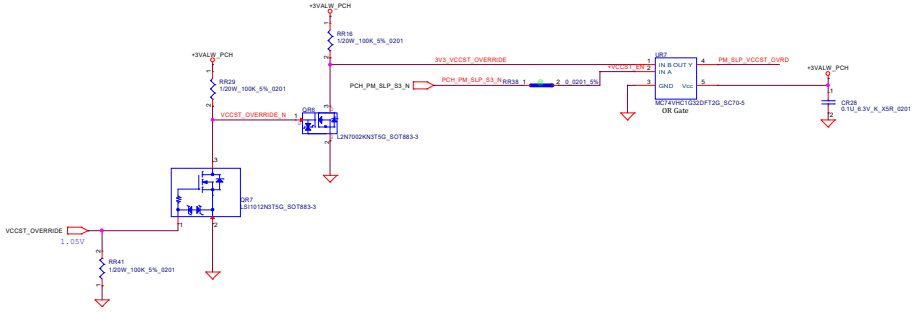


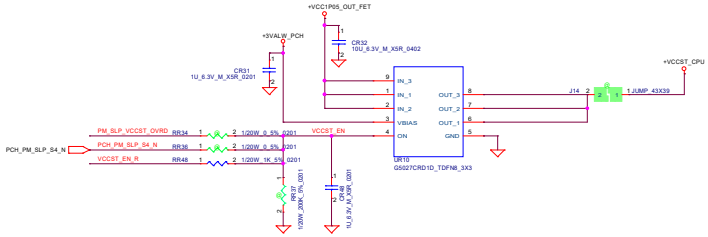
VCCST_EN / +1.8V_LDO_EN





VCCST





Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title	PWR		
Size	Document Number		Rev
D	E14/E15 NM-E211		0.1
Date:	Wednesday, March 02, 2022	Sheet 84 of 108	

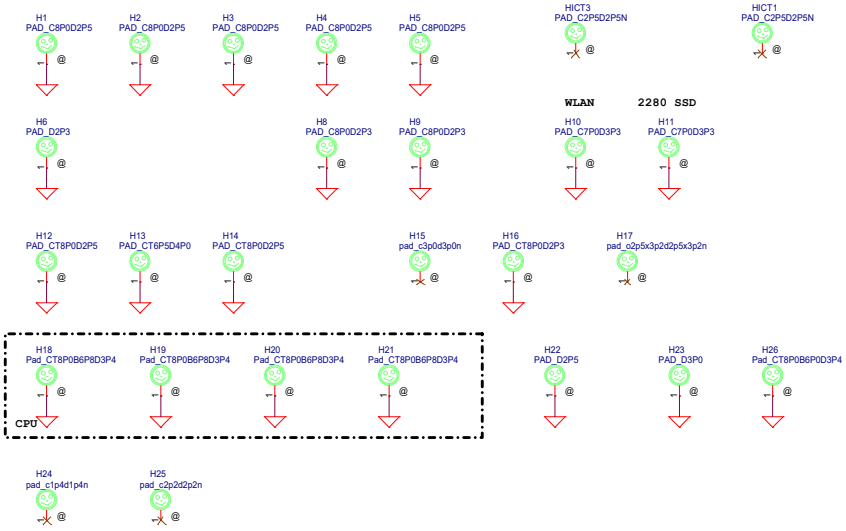
Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title

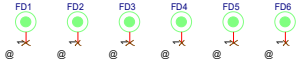
Change Lise_PWR

Size C	Document Number *E14/E15 NM-E211*	Rev 0.1
Date: Wednesday, March 02, 2022	Sheet 85 of 108	

Screw Hole

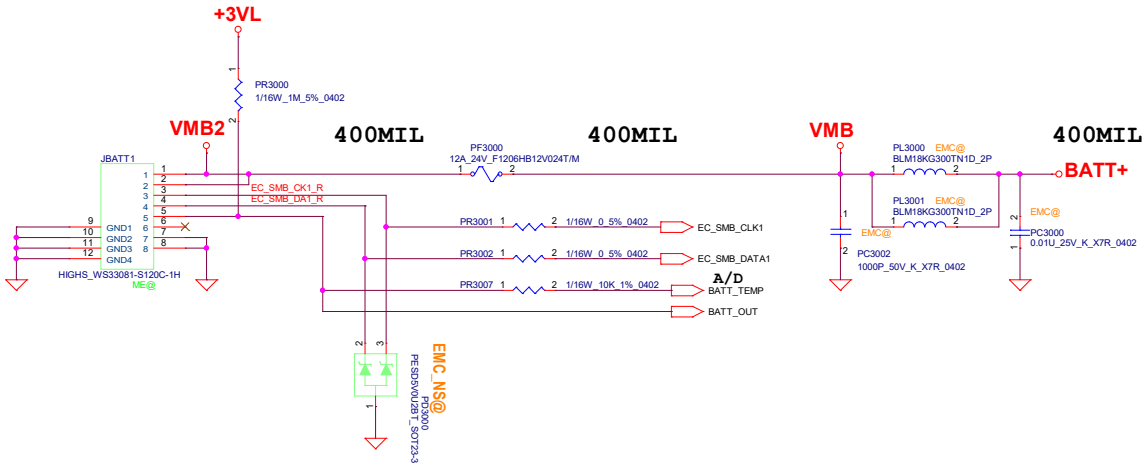


PCB Fedical Mark PAD

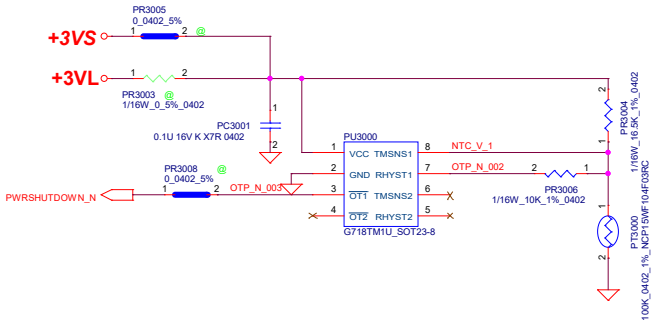


Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title	SCREW HOLE		
Size	Document Number		Rev
C	E14/E15 NM-E211		0.1
Date:	Wednesday, March 02, 2022	Sheet	86 of 108



PT3000 under CPU bottom side for CPU thermal protection.
This is for thermal team request.

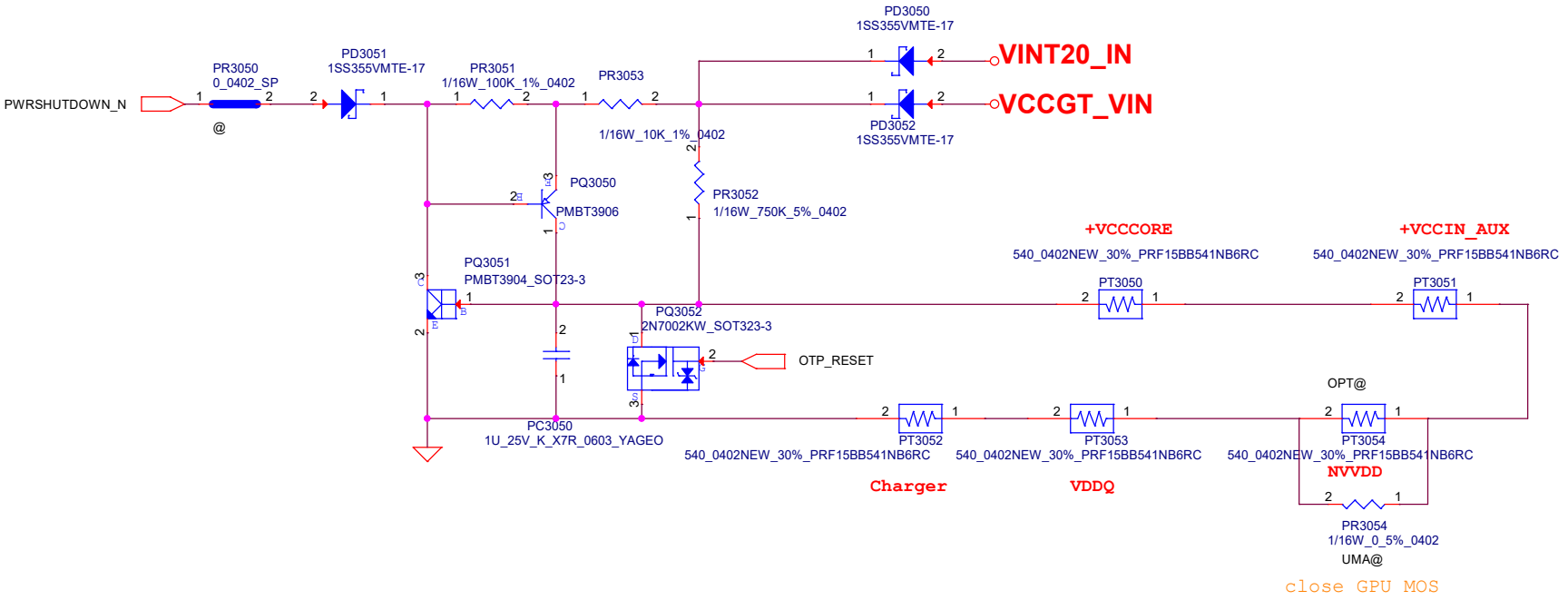


Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: *DCIN/RTC*

Size	Document Number	Rev
Custom	*ThinkPad E14 GEN4*	

Date: Wednesday, March 02, 2022 | Sheet 87 of 108

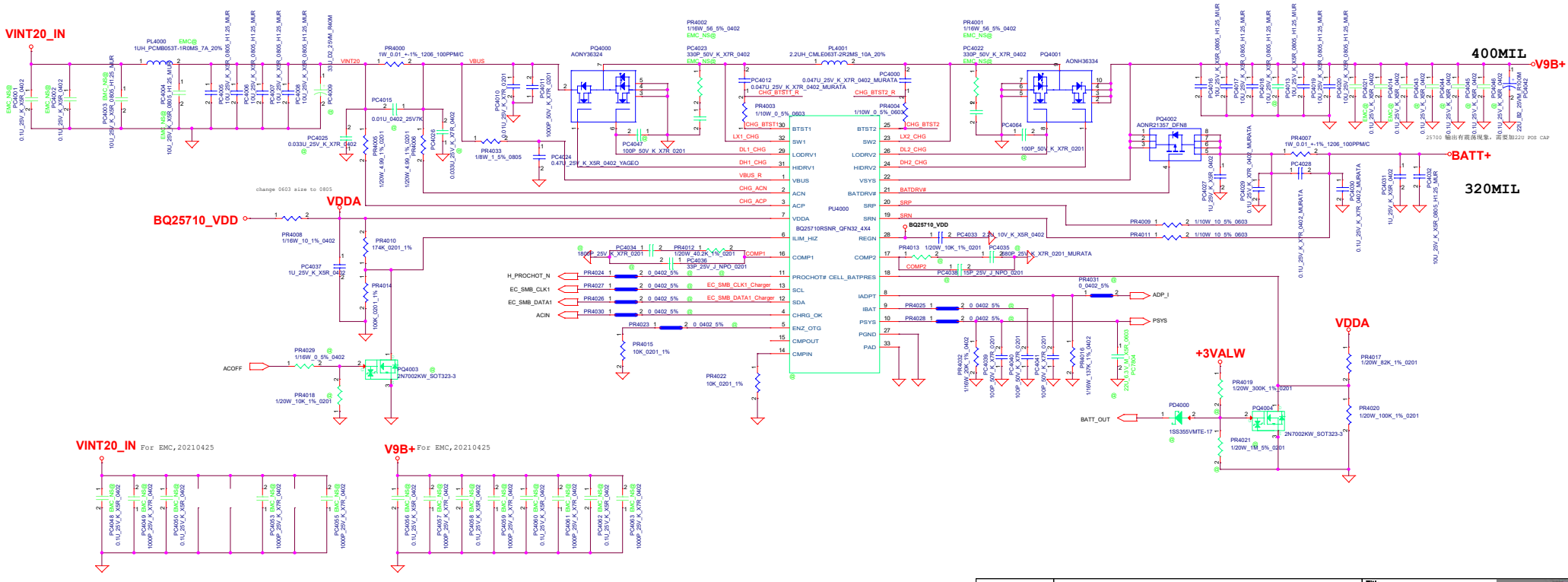


Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: *OTP*

Size	Document Number	Rev
Custom	ThinkPad E14 GEN4	1

Date: Wednesday, March 02, 2022 Sheet 88 of 108



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

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Title	BATTERY CHARGER(BQ25700A)		
Size: Custom	Document Number: E14/E15 NM-D011		Rev: 0.1
Date: Wednesday, March 02, 2022	Sheet 89 of 108		

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

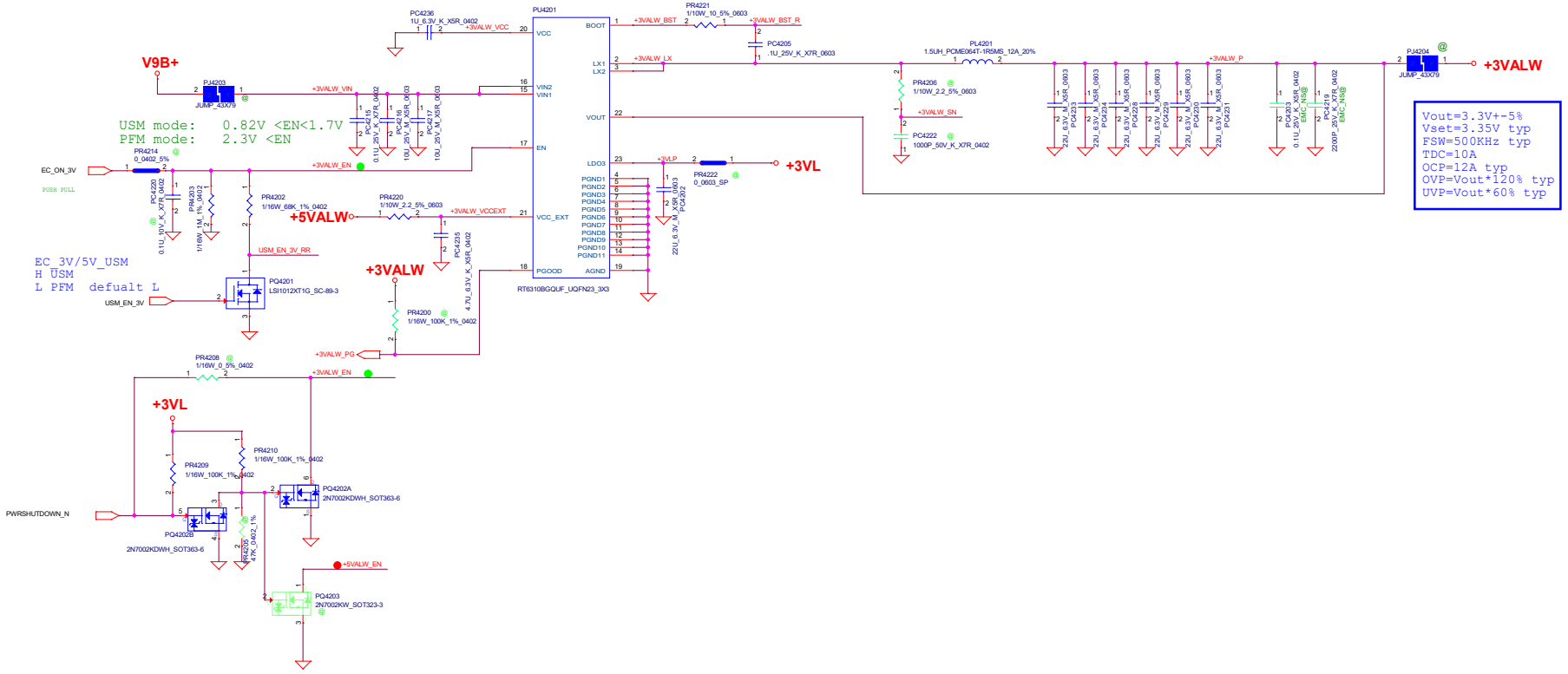
Title

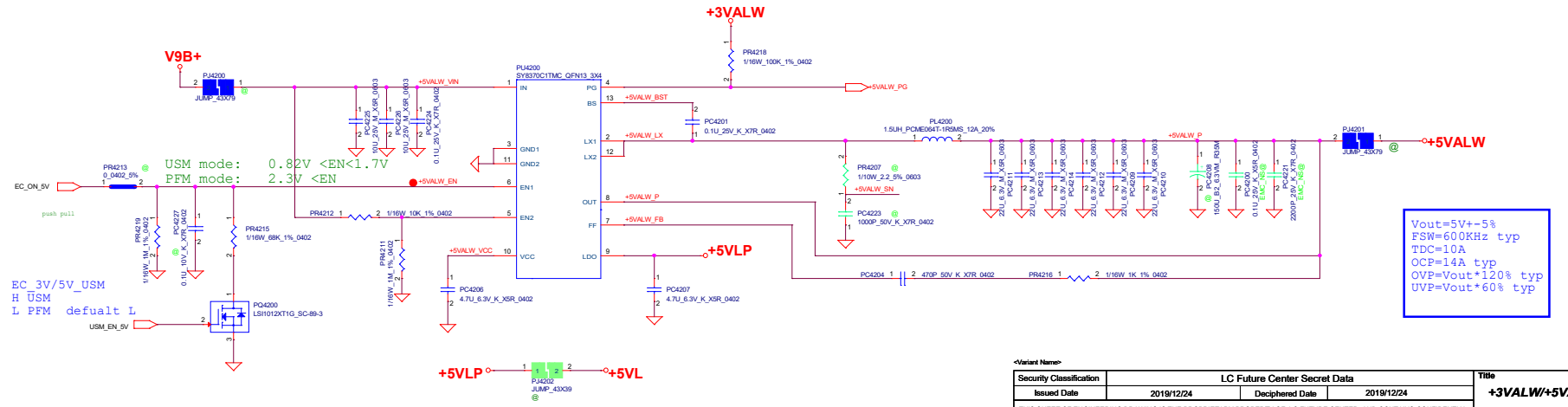
NA

LCFC

Size	Document Number	Rev
A	***ThinkPad E14 GEN4***	1

Date: Wednesday, March 02, 2022 Sheet 90 of 108





<Variant Name>

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: +3VALW/+5VALW

Size: Document Number: ThinkPad E14 GEN4 Rev: 1

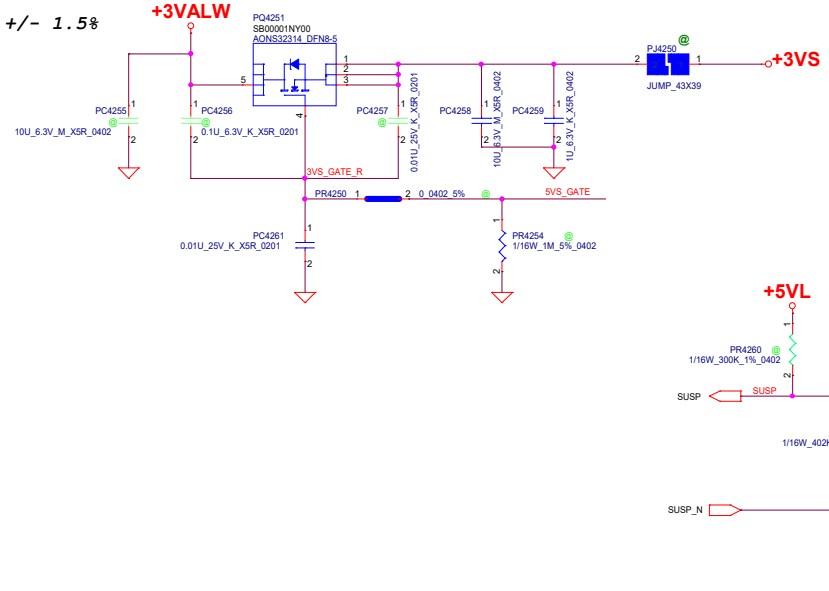
Date: Wednesday, March 02, 2022 Sheet 91 of 108

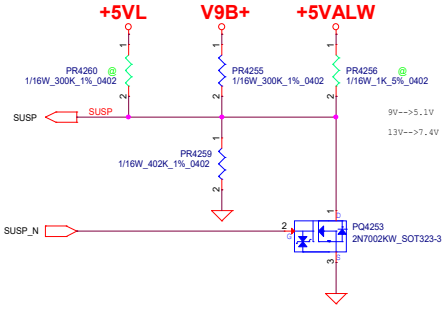
+3VS load Switch

+3VALW to +3VS 6.2A request

VSYS15 9V--13V

Load MOS N MOS Id =< 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm

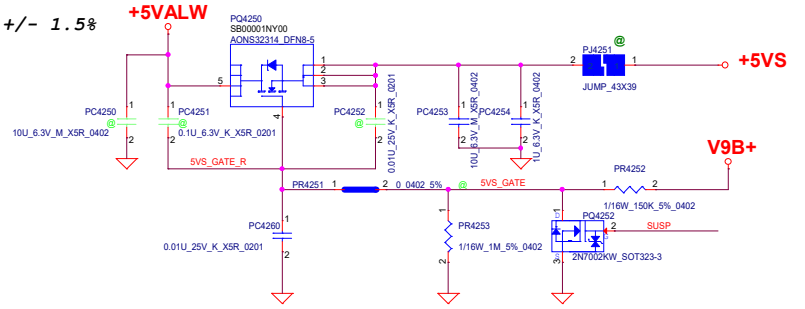


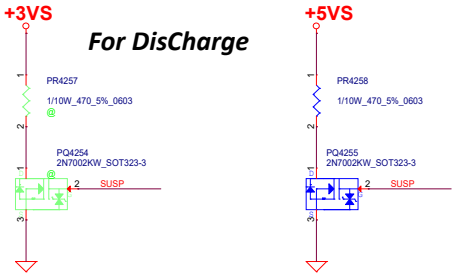


+5VS load Switch

+5VALW to +5VS 2.6A request

Load MOS N MOS Id =< 40A Vgs(th) Max >= 2.6V
Rds(on) >= 7.5mohm





Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: +3VS/+5VS

Size: C | Document Number: ThinkPad E14 GEN4 | Rev: 1

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Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/01/19	Deciphered Date	2022/01/19

Title: LPDDR5

LCFC

Size	Document Number	Rev
D	ThinkPad E14 GEN4	1

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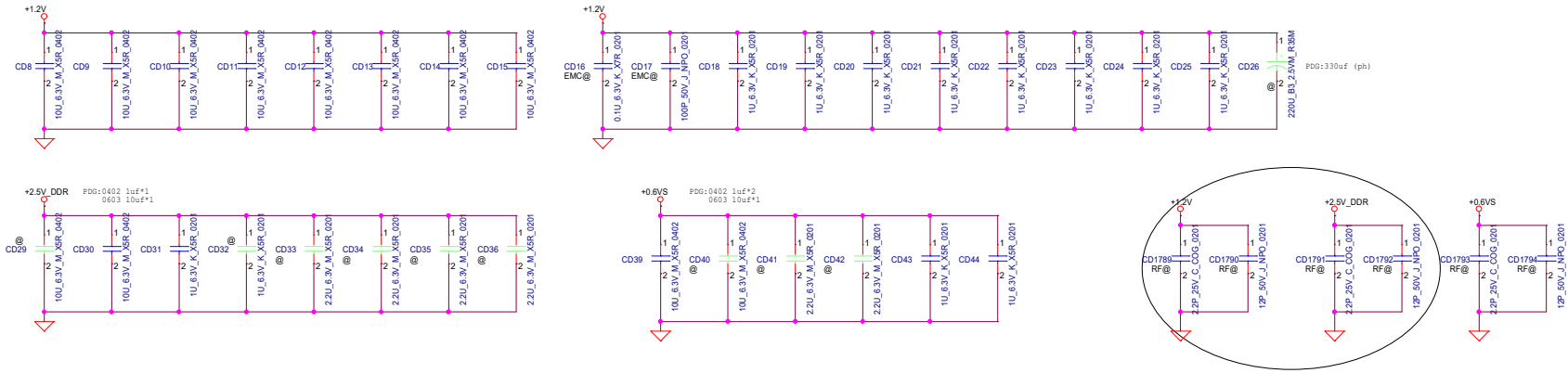
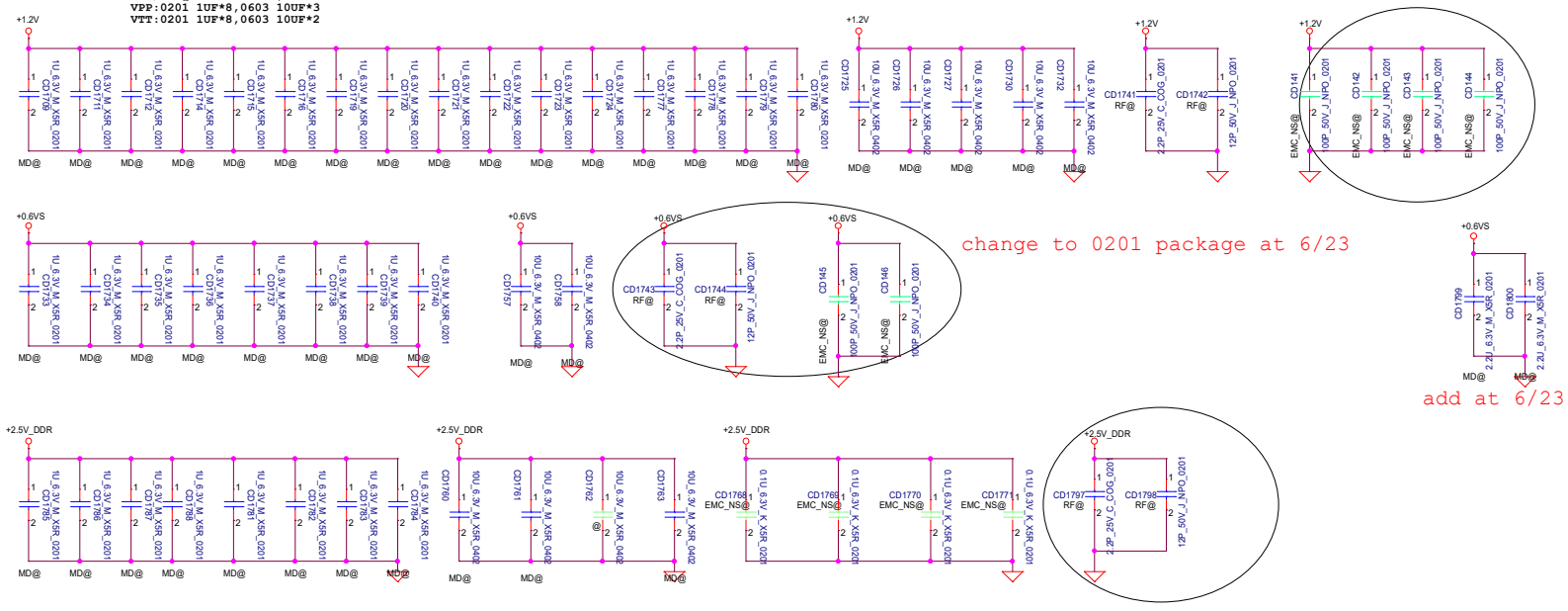
SO-DIMM

PDG:0201 1uf*8
PDG:0603 10uf*8
PDG:7343 330uf*1(PH)



MEMORY DOWN

PDG:
VDD/VDDQ:0201 1UF*16,0603 10UF*5
VPP:0201 1UF*8,0603 10UF*3
VTT:0201 1UF*8,0603 10UF*2



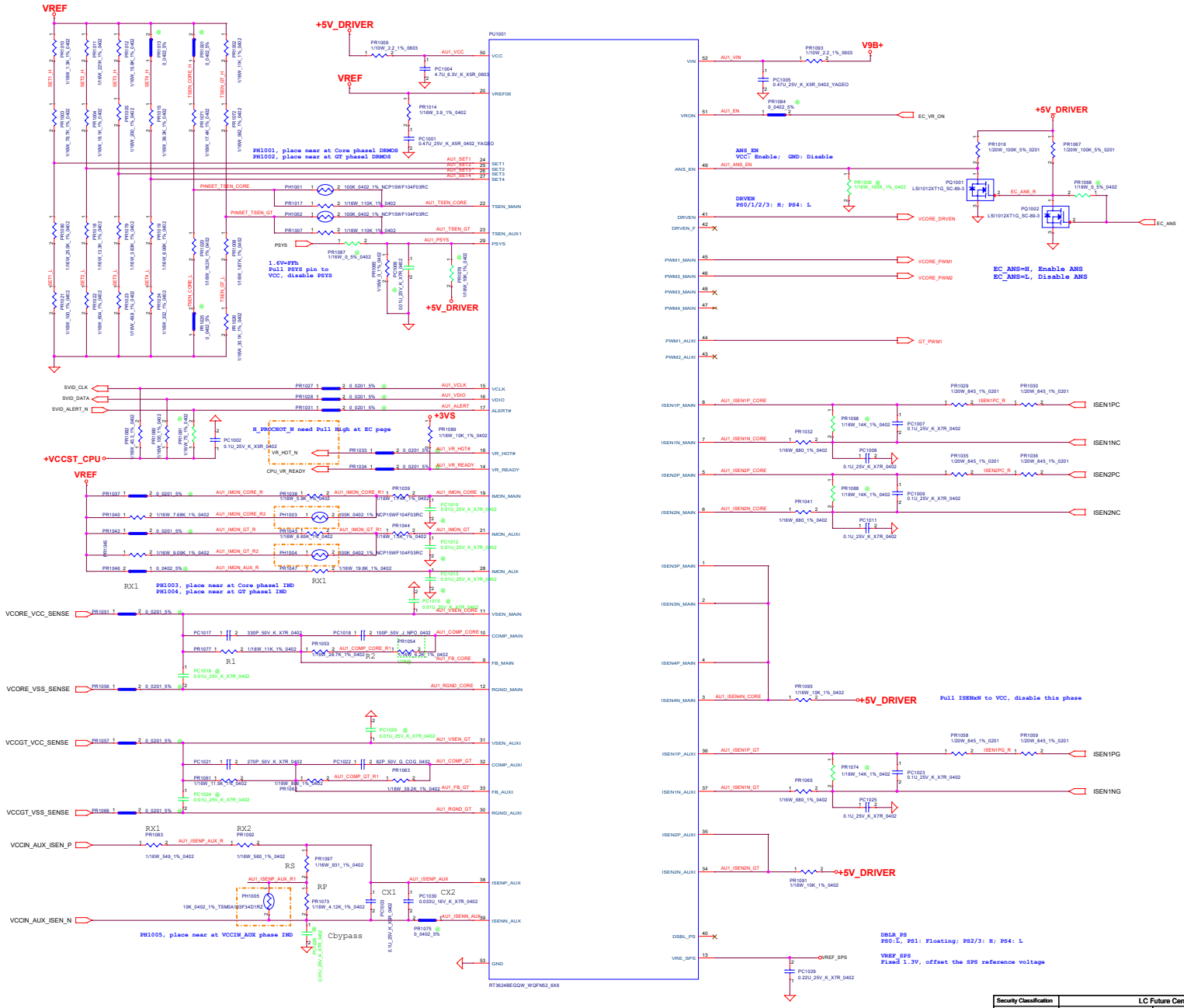
Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/01/19	Deciphered Date	2022/01/19

Title: LPDDR5 Decoupling

LCFC

Size	Document Number	Rev
C	ThinkPad E14 GEN4	1

Date: Wednesday, March 02, 2022 Sheet 94 of 108

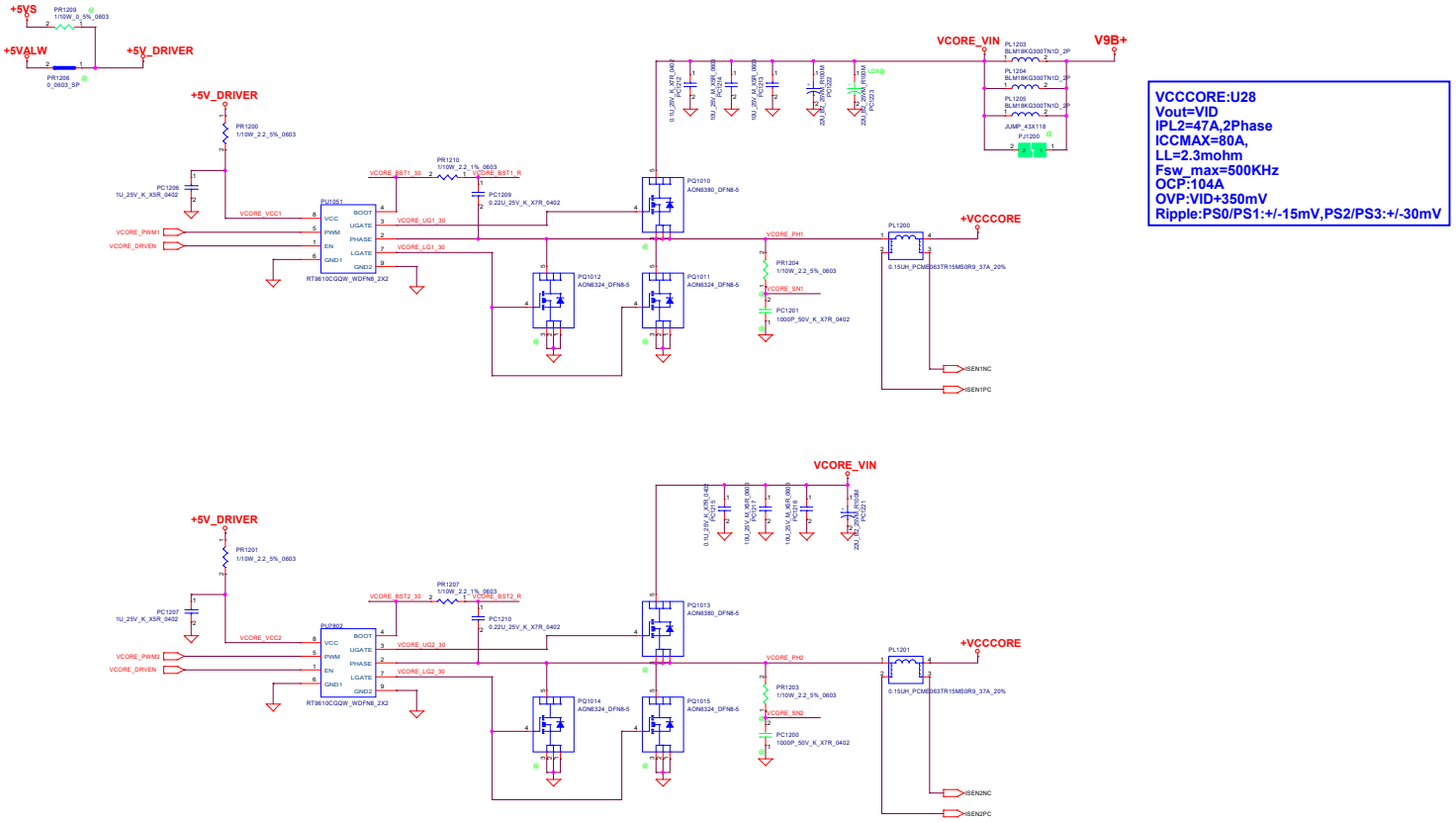


Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: CPU CONTROLLER

Size: D | Document Number: ThinkPad E14 GEN4 | Rev: 1

Date: Wednesday, March 02, 2022 | Sheet 65 of 108



VCCCORE:U28
Vout=VID
IPL2=47A,2Phase
ICCMAX=80A,
LL=2.3mohm
Fsw_max=500KHz
OCP:104A
OVP:VID+350mV
Ripple:PS0/PS1:+/-15mV,PS2/PS3:+/-30mV

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

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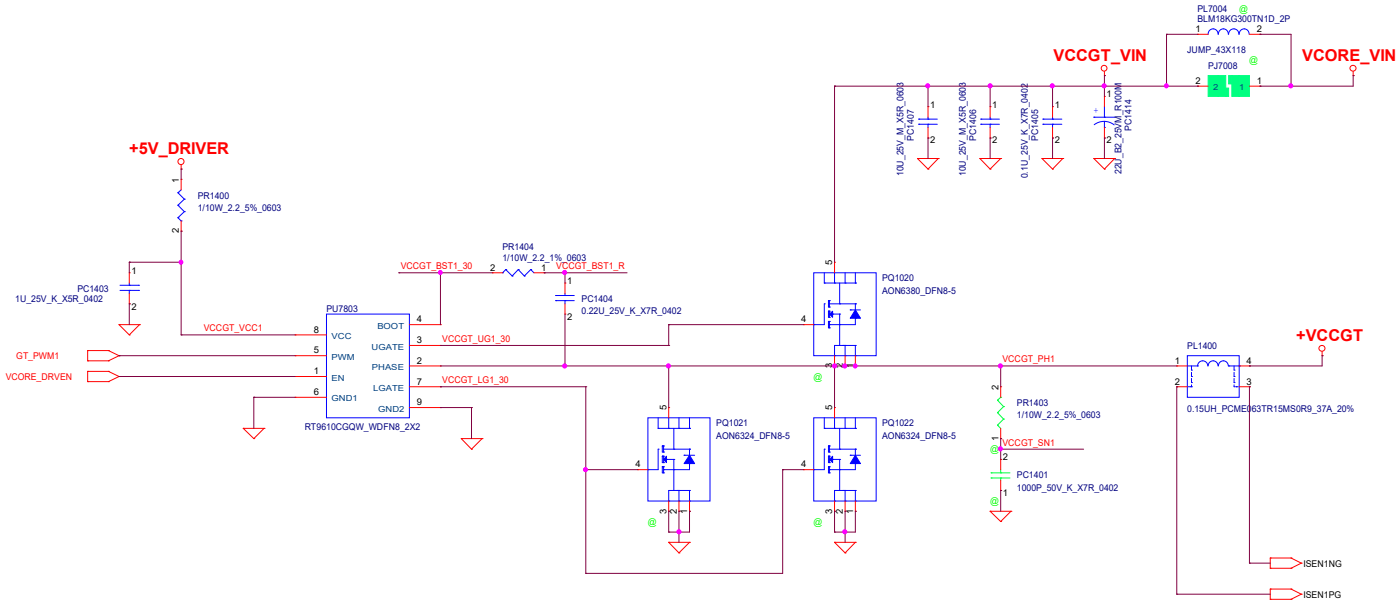
Title	VCCCORE	
Size: D	Document Number: ThinkPad E14 GEN4	Rev: 1
Date: Wednesday, March 02, 2022	Sheet 98 of 103	



VCCGT:
Vout:VID
IPL2=23A,1Phase
ICCMAX=40A,
LL=3.2mohm
Fsw_max=400KHz
OCP:52A
OVP:VID+350mV
Ripple:Reference to EDS

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: GT

Size	Document Number	Rev
C	ThinkPad E14 GEN4	1

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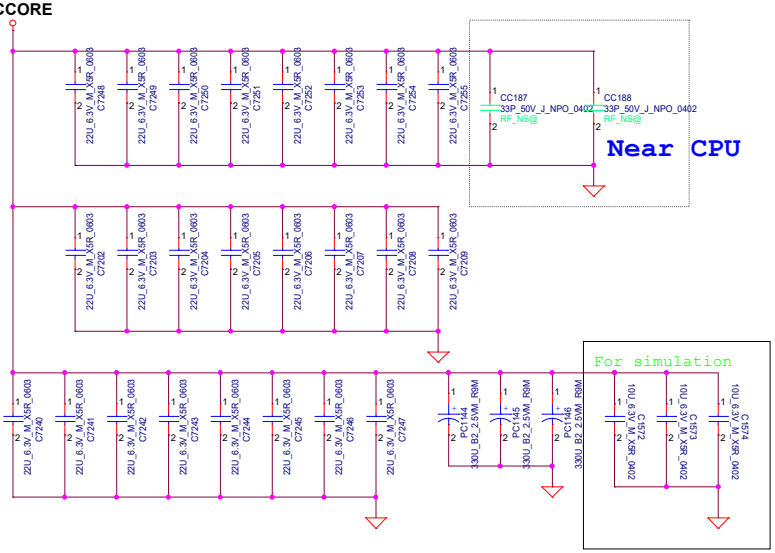
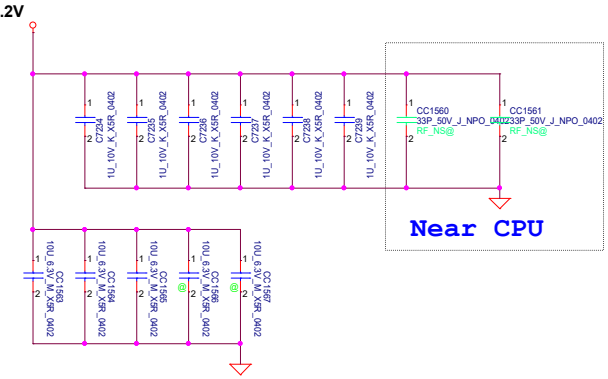
+VCCCORE



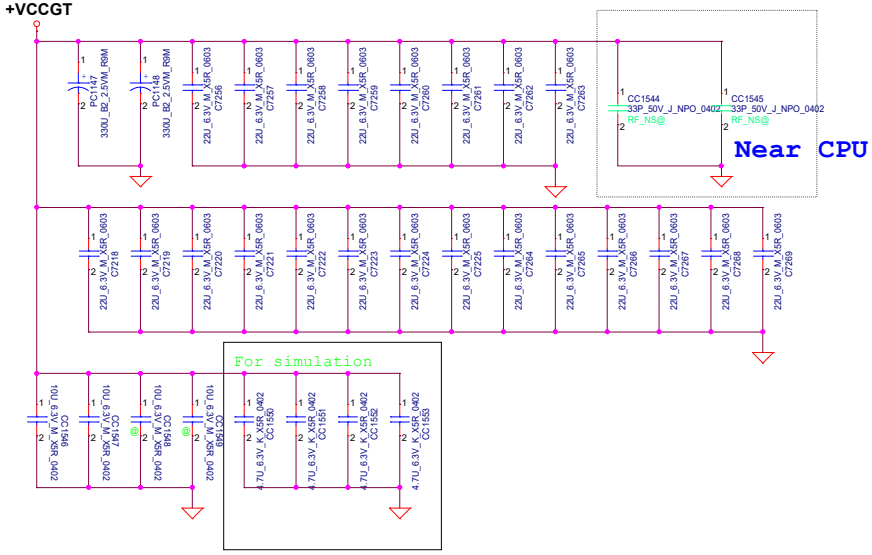
Follow PDG v0.81: 47uF*8pcs+22uF*8pcs+330uF*3
E14: 22uF*24pcs+330uF*3

+1.2V



Follow PDG v0.81: 10uF*3pcs+1uF*6pcs+placeholder*2PCS

+VCCGT



Follow PDG v0.81: 47uF*7pcs+22uF*8pcs+330uF*2
E14: 22uF*22pcs+330uF*2

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *CPU Decoupling*

Size	Document Number	Rev
C	*ThinkPad E14 GEN4*	1

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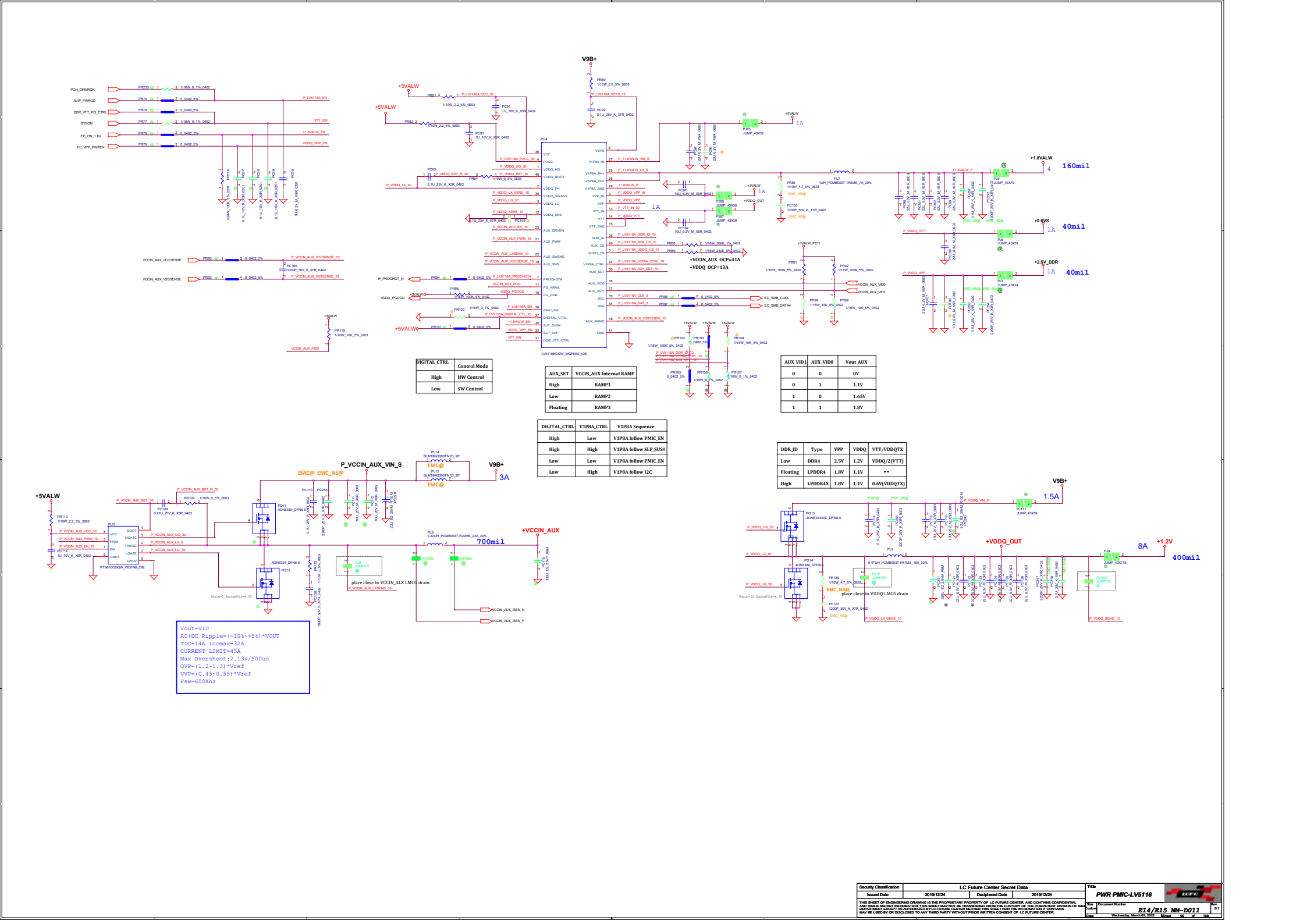

DIGITAL_CTRL	Control Mode
High	HW Control
Low	SW Control

AUX_SET	VCCIN_AUX Internal RAMP
High	RAMP1
Low	RAMP2
Floating	RAMP3

DIGITAL_CTRL	V1P8A_CTRL	V1P8A Sequence
High	Low	V1P8A follow PMIC_EN
High	High	V1P8A follow SLP_SUS#
Low	Low	V1P8A follow PMIC_EN
Low	High	V1P8A follow I2C

AUX_VID1	AUX_VID0	Vout_AUX
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

DDR_ID	Type	VPP	VDDQ	VTT/VDDQTX
Low	DDR4	2.5V	1.2V	VDDQ/2(VTT)
Floating	LPDDR4	1.8V	1.1V	--
High	LPDDR4X	1.8V	1.1V	0.6V(VDDQTX)

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

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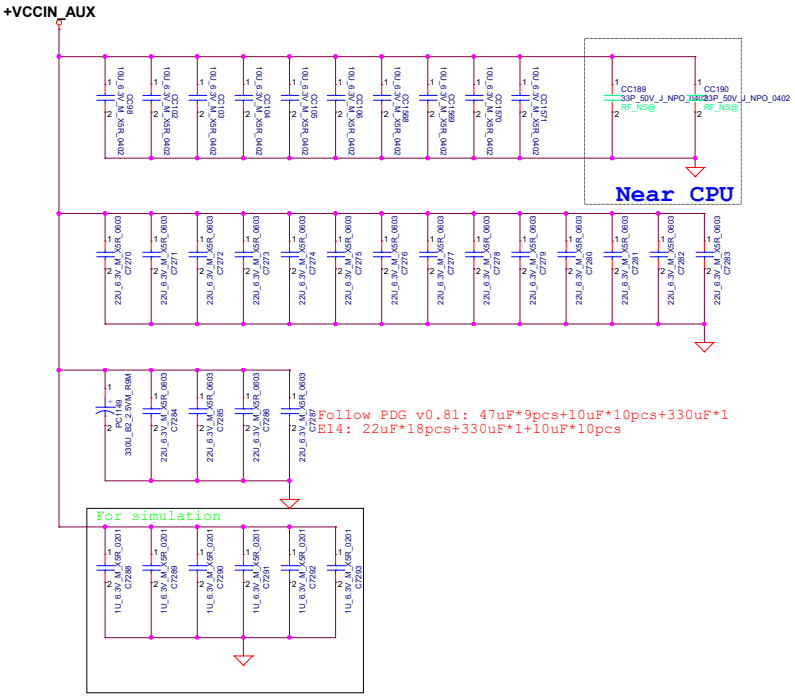
Title	PWR PMIC-LV5116	
Size: Custom	Document Number: R14/R15_MM-D011	Rev: 0.1
Date: Wednesday, March 02, 2022	Sheet 59 of 105	

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *1.8VALW*

Size	Document Number	Rev
C	ThinkPad E14 GEN4	1

Date: Wednesday, March 02, 2022 | Sheet 100 of 108



Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

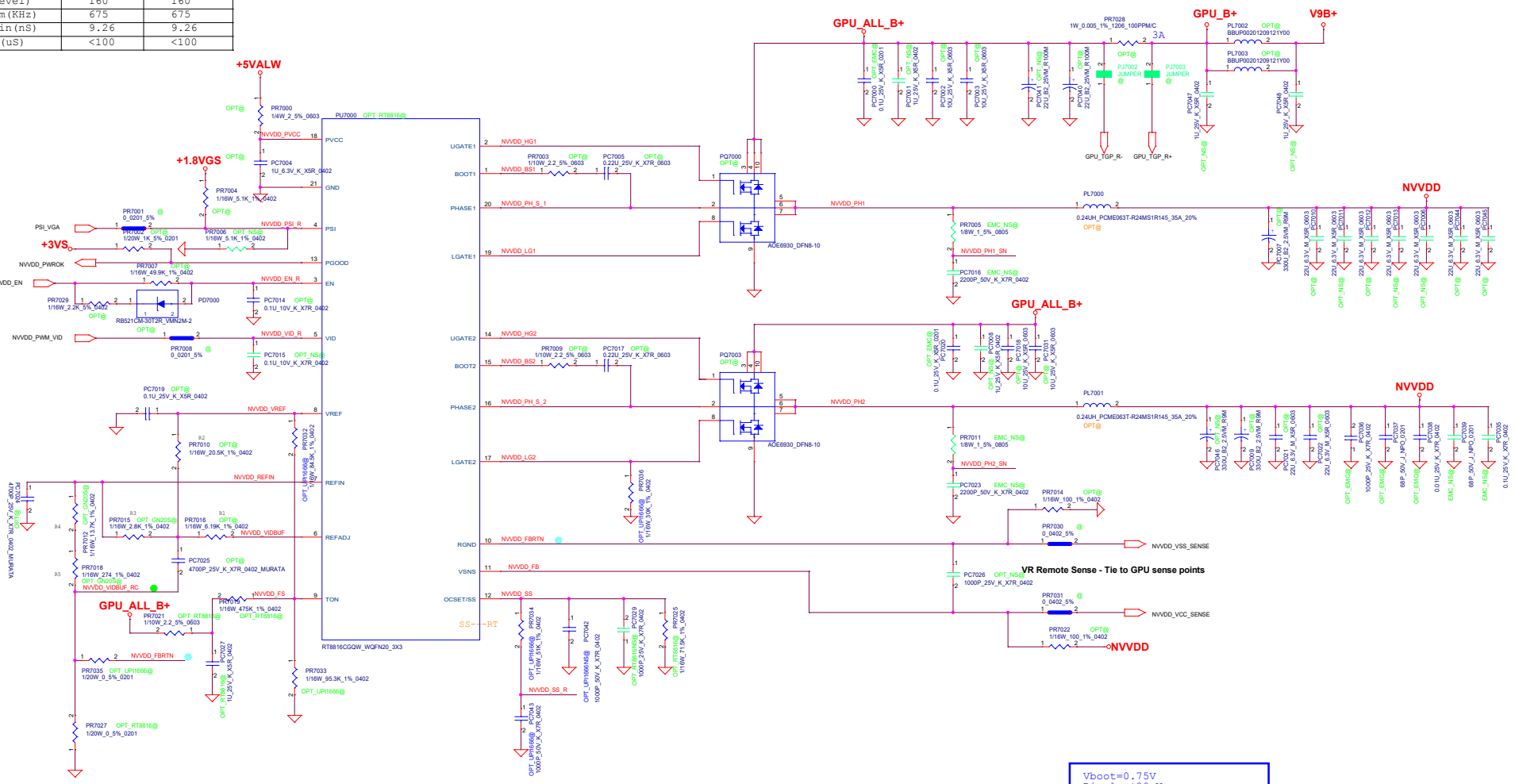
Title: *PCH Decoupling*

Size	Document Number	Rev
Custom	*ThinkPad E14 GEN4*	1

Date: Wednesday, March 02, 2022 | Sheet 101 of 108

PWM-VID Specification		
	GN18S	GN20S
Vmin(V)	0.3	0.3
Vmax(V)	1.3	1.3
Vboot(V)	0.8	0.75
Vstep(mV)	6.25	6.25
N(level)	160	160
Fpwm(KHz)	675	675
Tdmin(nS)	9.26	9.26
T(uS)	<100	<100

RT8816 PSI	~~UP1666 PSI~~	Phase Configuration
1.6V~5.5V	~~1.6~5.5V~~	2Phase CCM
1.08~1.35V	~~1~1.4V~~	2Phase DEM
0.7~0.88V	~~0.4V~0.8V~~	1Phase CCM
0~0.4V	~~0~0.2V~~	1Phase DEM

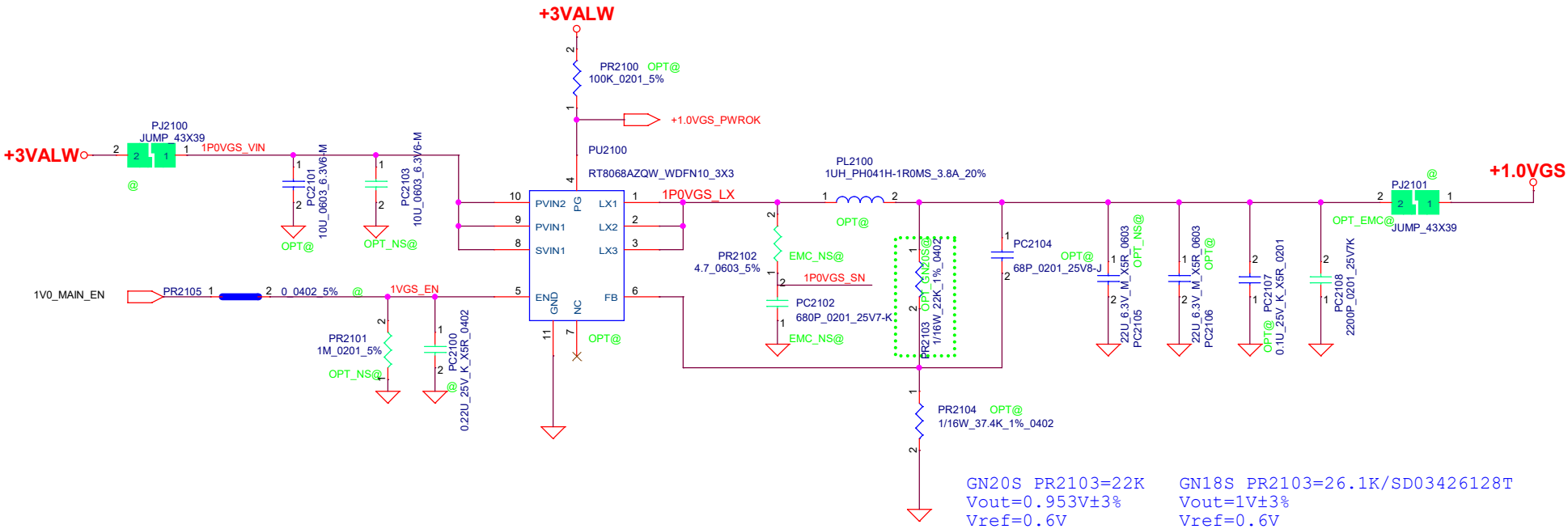


Component	Value	GN18S	PN
R5(KΩ)	PR7018	309	SD00001XX0T
R4(KΩ)	PR7012	16.5K	SD03416520T
R3(KΩ)	PR7015	4.32K	SD00000J28T

Vboot=0.75V
Ripple=±20mV
TDC=31A
Vref=2V
FUVP:Vfb=0.2V
SUVP:Vcomp=3V
OVP:Vfb=2V
Fsw=320KHz
AOE6930:
Rdson=0.8mohm
Vgsth=1.2V/1.5V/1.9V

Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title	GPU Controller		
Size: Custom	Document Number: ThinkPad E14 GEN4		Rev: 1
Date: Wednesday, March 02, 2022	Sheet 102 of 108		



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: 1VGS

Size	Document Number	Rev
Custom	ThinkPad E14 GEN4	1

Date: Wednesday, March 02, 2022 Sheet 103 of 108

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title

NA

Size	Document Number	Rev
C	ThinkPad E14 GEN4	1

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PR7016 OPT_GN18S@ S RES 1/16W 309 +-1% 0402 SD00001X00T
PR7012 OPT_GN18S@ S RES 1/16W 16.5K +-1% 0402 SD034165Z0T
PR7015 OPT_GN18S@ S RES 1/16W 4.32K +-1% 0402 SD00000J28T
PR2103 OPT_GN18S@ S RES 1/16W 26.1K +-1% 0402 SD034261Z8T
For GN18S

PR1054 U15@ S RES 1/16W 0 +-1% 0402 SD000023B0T
For U15

X76_OPT_US5650@
ZZZ15
ALT. GROUP PARTS GPU US5650 JE440
X764EA0100H

X76_OPT_NCP45492@
ZZZ14
ALT. GROUP PARTS GPU NCP45492 JE440
X764EA0100G

PR7614 OPT_US5650@ S RES 1/16W 332 1% 0402 SD00002PY0T
PR7610 OPT_US5650@ S RES 1/16W 475 +-1% 0402 SD034475I0T
PR7605 OPT_US5650@ S RES 1/16W 499 +-1% 0402 SD034499I0T
PR7613 OPT_US5650@ S RES 1/16W 499 +-1% 0402 SD034499I0T
PR7602 OPT_US5650@ S RES 1/16W 316K +-1% 0402 SD03431638T
PU7601 OPT_US5650@ S IC US5650QQKI WQFN 32P PREFILTER SA00009YH00
PR7677 OPT_US5650@ 1/16W 0 1% 0402 SD00WZDJB0T
For US5650 GPU monitor

PR7614 OPT_NCP45492@ 1/16W 442 1% 0402 SD0007TWE0T
PR7610 OPT_NCP45492@ 1/16W 634 1% 0402 SD0007PK60T
PR7605 OPT_NCP45492@ 1/16W 665 1% 0402 SD0007DJ07T
PR7613 OPT_NCP45492@ 1/16W 665 1% 0402 SD0007DJ0TT
PR7602 OPT_NCP45492@ 1/16W 237K 1% 0402 SD034257S0T
PU7601 OPT_NCP45492@ NCP45492XMNTWG_QFN32_4X4 SA0006AFT00
PR7618 OPT_NCP45492@ 1/16W 0 1% 0402 SD00WZDJB0T
For NCP45492 GPU monitor

X76_BQ25710@
ZZZ16
ALT. GROUP PARTS CHARGER BQ25710 JE440
X764EA0100J

X76_SC8885L@
ZZZ17
ALT. GROUP PARTS CHARGER SC8885L JE440
X764EU0100K

PU4000 BQ25710@ BQ25710RSNR_QFN32_4X4 SA0009MC300
PC4025 BQ25710@ 0.033U 25V_K_X7R_0402 SE0000070T
PC4026 BQ25710@ 0.033U 25V_K_X7R_0402 SE0000070T
PC4034 BQ25710@ 1800P 25V_K_X7R_0201 SE0000DZY0T
PC4036 BQ25710@ 33P 25V_J_NPO_0201 SE174330JMT
PR4012 BQ25710@ 1/20W 40.2K 1% 0201 SD0000T3G8T
PC4035 BQ25710@ 680P 25V_K_X7R_0201_MURATA SE0000W0W Y0T
PC4038 BQ25710@ 15P 25V_J_NPO_0201 SE0000123T
PR4013 BQ25710@ 1/20W 10K 1% 0201 SD0411T0ZYT
For BQ25710 charger

PU4000 SC8885L@ S IC SC8885LQDER QFN 32P SA0006CTY00
PC4009 SC8885L@ 33U_D2_25VM_R40M SGA3D0J6W00
PC4034 SC8885L@ 1000P 25V_K_X7R_0201 SE1701D2KMT
PC4036 SC8885L@ 10P 25V_G_NPO_0201 SE0D000V70T
PR4012 SC8885L@ 1/20W 100K 1% 0201 SD0411D030T
PC4035 SC8885L@ 1000P 25V_K_X7R_0201 SE1701D2KMT
PC4038 SC8885L@ 220P 25V_K_X7R_0201 SE0000R0M3T
PR4013 SC8885L@ 1/20W 330K 1% 0201 SD0000T220T
For SC8885L charger

X76_CPU MOS_AOS@
ZZZ18
ALT. GROUP PARTS CPU CORE MOS JE442
X764EU0100G

X76_CPU MOS_NIKO@
ZZZ19
ALT. GROUP PARTS CPU CORE MOS JE442
X764EU0100H

X76_CPU MOS_SINOPOWER@
ZZZ20
ALT. GROUP PARTS CPU CORE MOS JE442
X764EU0100J

PQ1013 AOS@ AON6380 SB00001FQ00
PQ1010 AOS@ AON6380 SB00001FQ00
PQ1020 AOS@ AON6380 SB00001FQ00
PQ11 AOS@ AON6380 SB00001FQ00
PQ1011 AOS@ AON6324 SB00001H100
PQ1012 AOS@ AON6324 SB00001H100
PQ1014 AOS@ AON6324 SB00001H100
PQ1015 AOS@ AON6324 SB00001H100
PQ1021 AOS@ AON6324 SB00001H100
PQ1022 AOS@ AON6324 SB00001H100
PQ12 AOS@ AON6324 SB00001H100

PQ1013 NIKO@ PK632BA SB000018M00
PQ1010 NIKO@ PK632BA SB000018M00
PQ1020 NIKO@ PK632BA SB000018M00
PQ11 NIKO@ PK632BA SB000018M00
PQ1011 NIKO@ PK632BA SB000018K00
PQ1012 NIKO@ PK632BA SB000018K00
PQ1014 NIKO@ PK632BA SB000018K00
PQ1015 NIKO@ PK632BA SB000018K00
PQ1021 NIKO@ PK632BA SB000018K00
PQ1022 NIKO@ PK632BA SB000018K00
PQ12 NIKO@ PK632BA SB000018K00

PQ1013 SINOPOWER@ SM4503BNHKPC SB00001HZ00
PQ1010 SINOPOWER@ SM4503BNHKPC SB00001HZ00
PQ1020 SINOPOWER@ SM4503BNHKPC SB00001HZ00
PQ11 SINOPOWER@ SM4503BNHKPC SB00001HZ00
PQ1011 SINOPOWER@ SM4513NHKPCTRG SB00001J000
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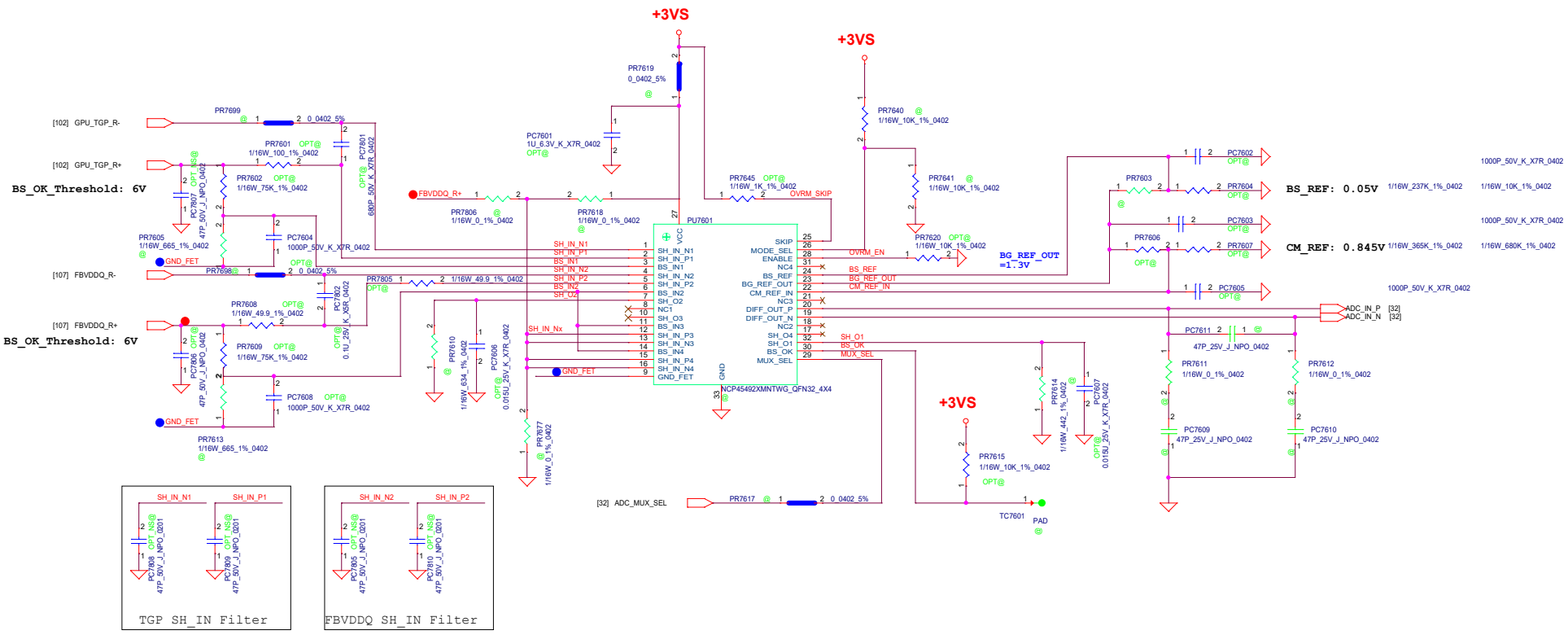
PQ1021 SINOPOWER@ SM4513NHKPCTRG SB00001J000
PQ1022 SINOPOWER@ SM4513NHKPCTRG SB00001J000
PQ12 SINOPOWER@ SM4513NHKPCTRG SB00001J000

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title	NA		
Size D	Document Number	ThinkPad E14 GEN4	Rev 1
Date: Wednesday, March 02, 2022	Sheet 104 of 108		



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R25=PR7610=634
R23=PR7605=665
R26=PR7613=665
R17=PR7603=237K

UPI-US5650
R21=PR7614=332
R25=PR7610=475
R23=PR7605=499
R26=PR7613=499
R17=PR7603=316K

Security Classification	LCFC Highly Confidential Information		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *GPU Monitor*

LCFC

Size	Document Number	Rev
C	*ThinkPad E14 GEN4*	1

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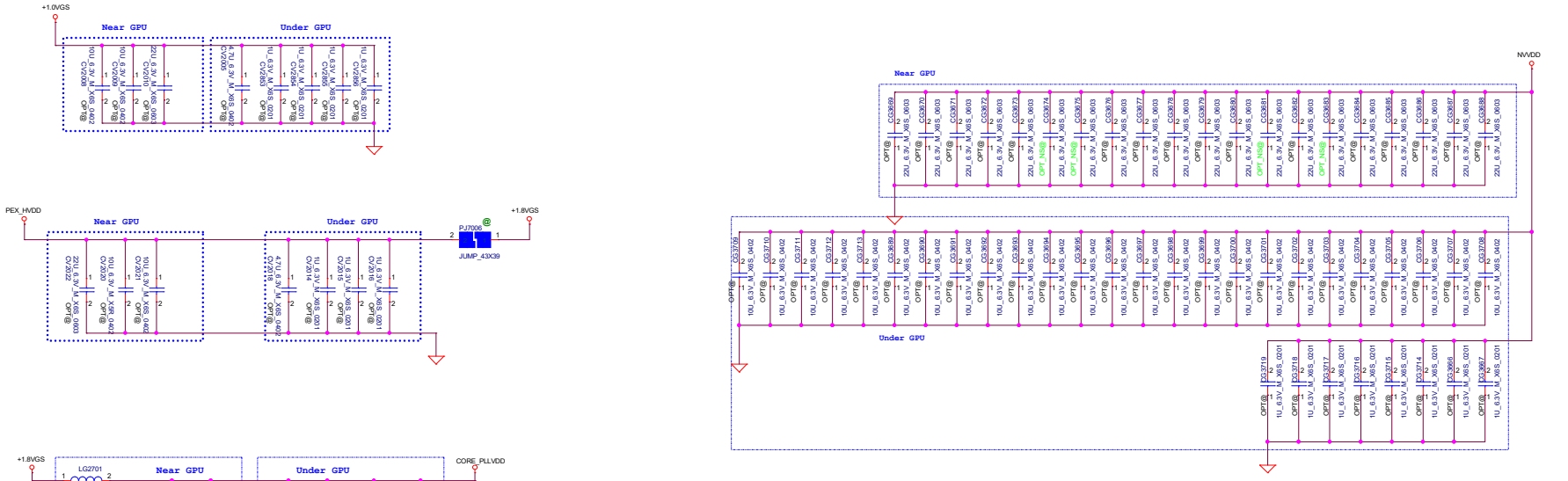

Security Classification	LC Future Center Secret Data		
Issued Date	2018/08/02	Deciphered Date	2018/08/02

Title: *GPU Decoupling*

Size: D	Document Number: ThinkPad E14 GEN4		Rev: 1
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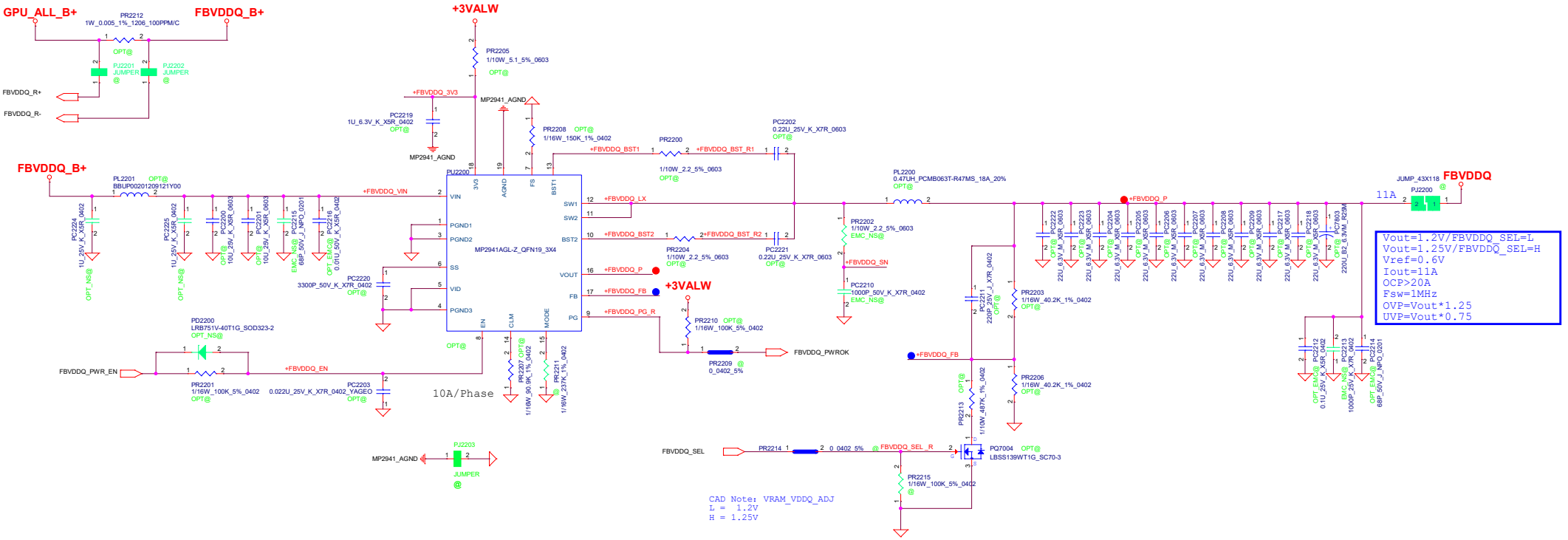

Tabel---1:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Tabel---2:FS Select

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

Tabel---3:CLM Select for per phase

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	12A	150k
M4	15A	>230k or float

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/15	Deciphered Date	2013/08/15

Title: FBVDDQ

Size: Custom | Document Number: ThinkPad E14 GEN4 | Rev: 1

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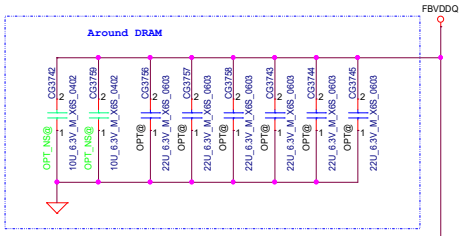
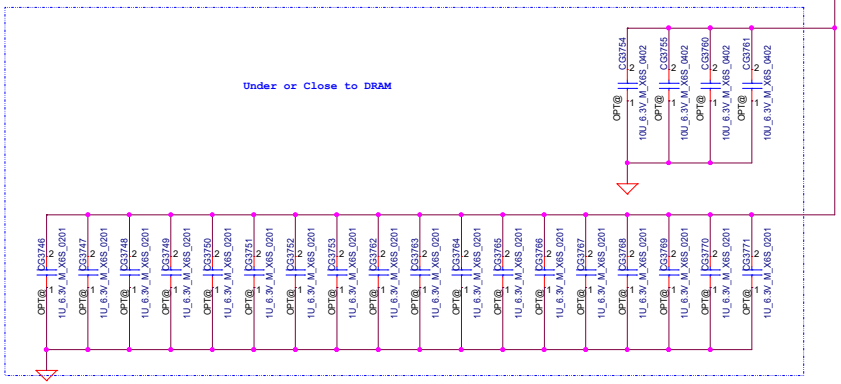
VRAM

NV:6x10uF 0402 18x1uF 0201 6x22uF,
Reserve 2x220uF 5x22uF 0805





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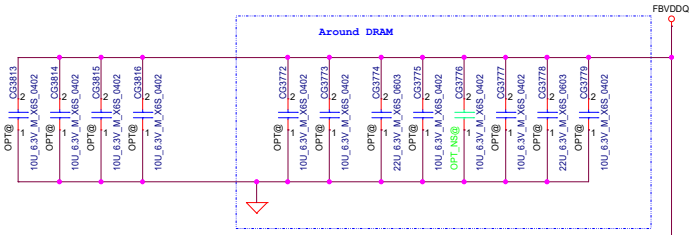
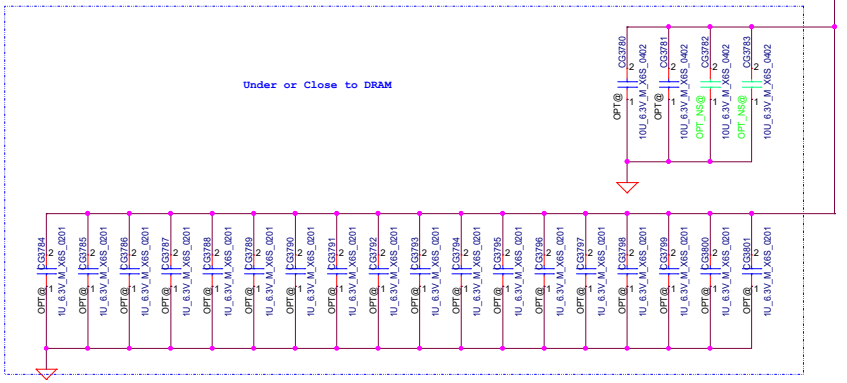
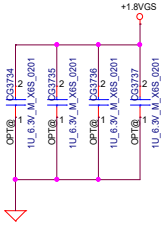
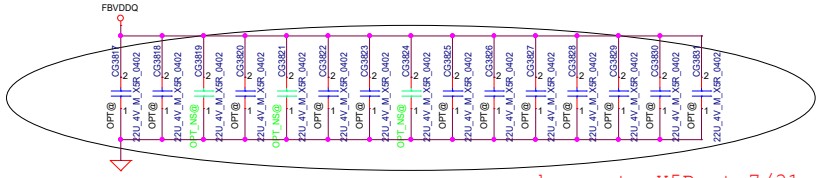




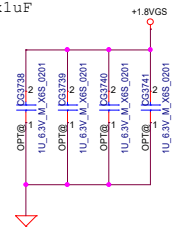
NV:4x1uF



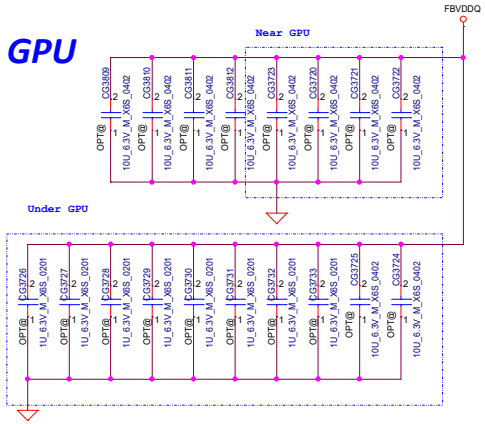


change to X5R at 7/31

NV:4x1uF



GPU



Security Classification	LC Future Center Secret Data		
Issued Date	2019/12/24	Deciphered Date	2019/12/24

Title: VRAM Decoupling

Size	Document Number	Rev
C	ThinkPad E14 GEN4	1

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