NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

LAIKA

INTEL ICE LAKE-U 15W

MV

WLAN

2020.01.16

BIOS

BUILD_ID H L	BUILD_ID1 R4609 : 1 R4606 : 0	BUILD_ID0 R4610 : 1 R4607 : 0
DB	0	0
SI	0	1
PV	1	0
MV	1	1

BOARD_ID H L	BOARD_ID0 R4616 : 1 R4620 : 0	BOARD_ID1 R4619 : 1 R4621 : 0	BOARD_ID2 R4617 : 1 R4618 : 0
WLAN	0	0	0
WWAN	0	0	1

EC

Phase_ID	SI	DB	PV / MV
R326	10K_short	10K_short	10K_open
R327	10K_open	10K_short	10K_short
	3V	1.5V	0V

Marking	Description
I	Install
NI	Non-install
PROTO	Proto type
MP	Mass Production
TAA	Install for TAA
CRITICAL	Critical Parts

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK	by Andy		
APPROVAL	by Andy		
FILE NAME	MLB 17.3 - RANGERS		
PCB P/N	50.XXXXX.XXXX	PCB VER	XXX

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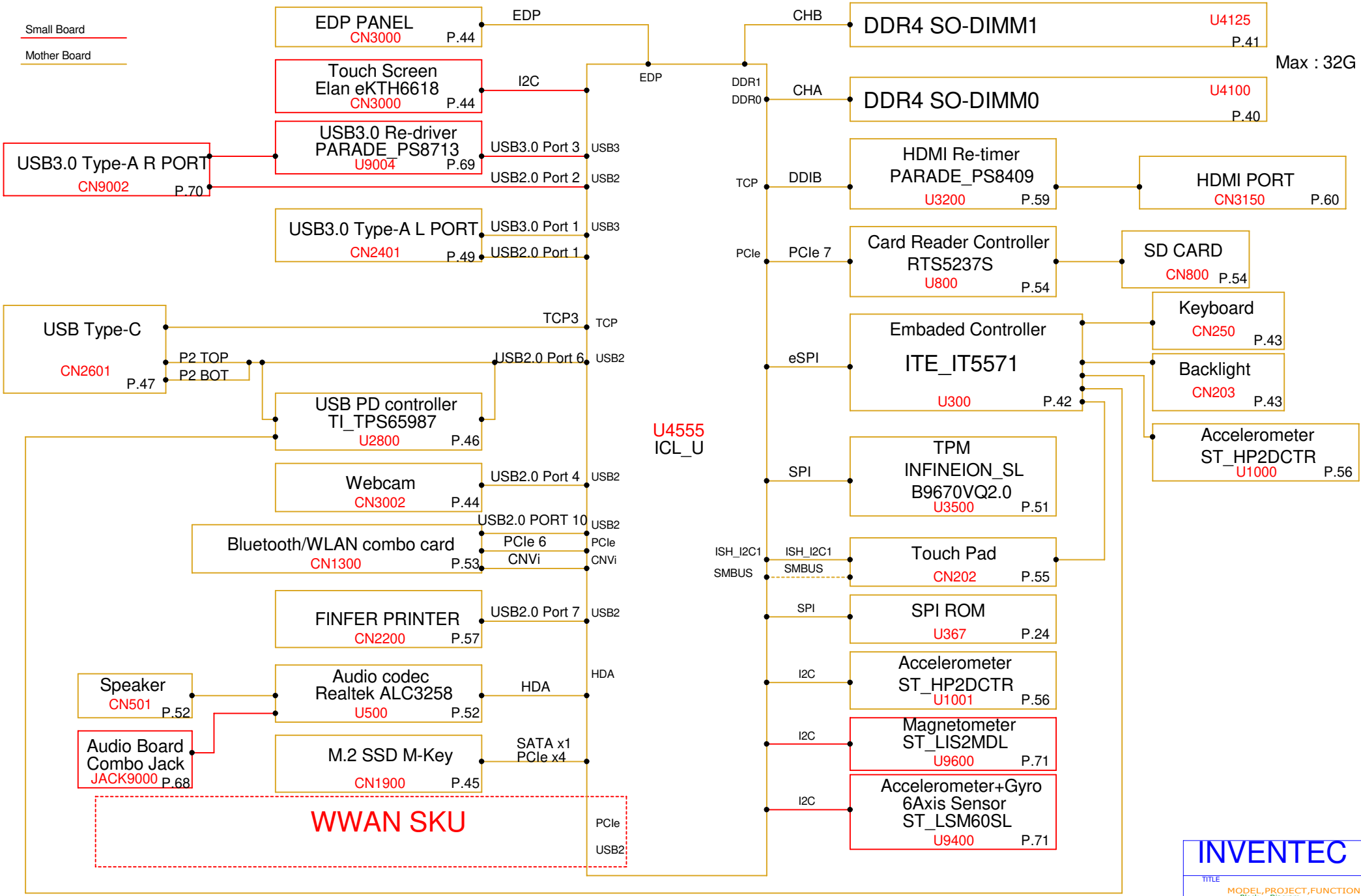

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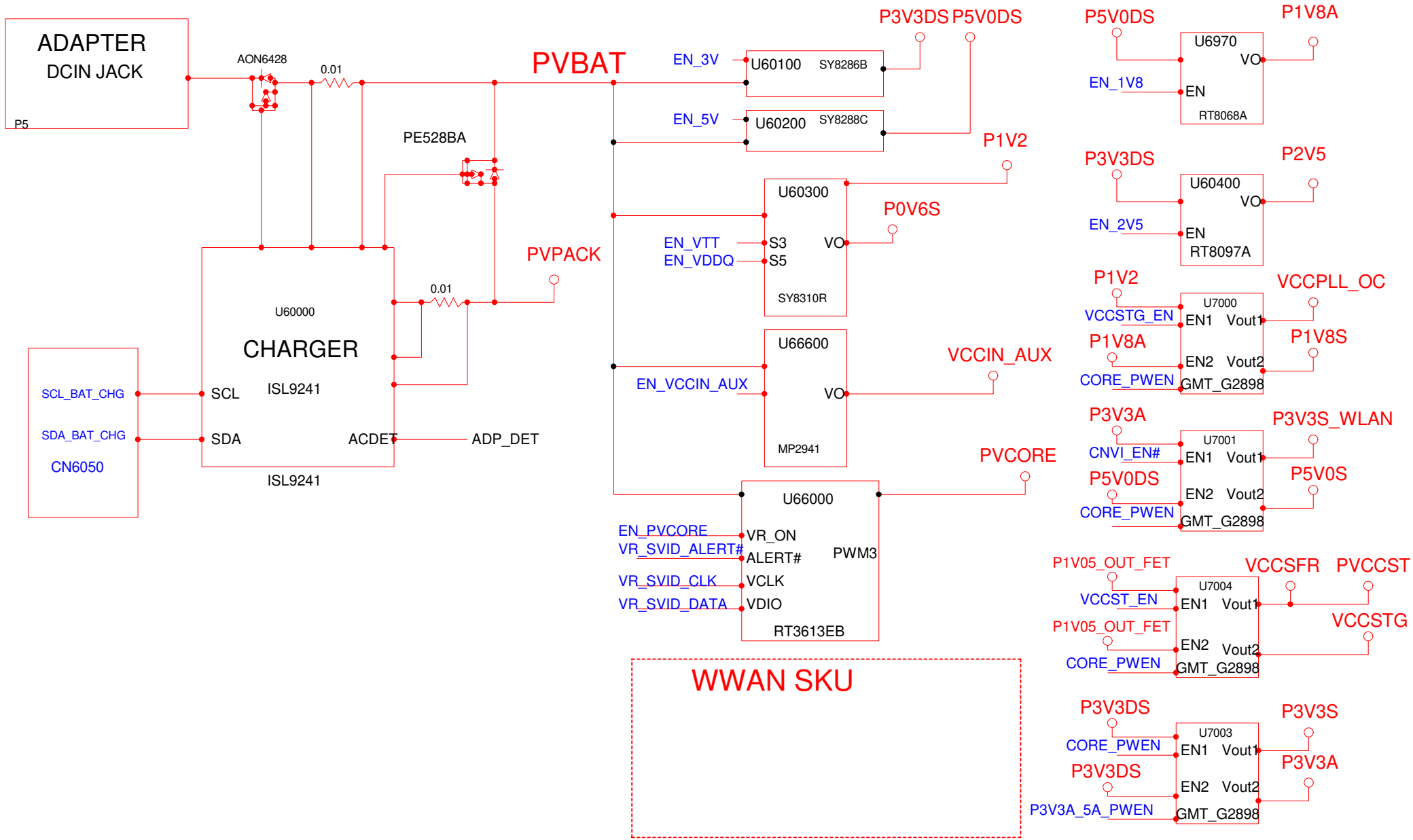

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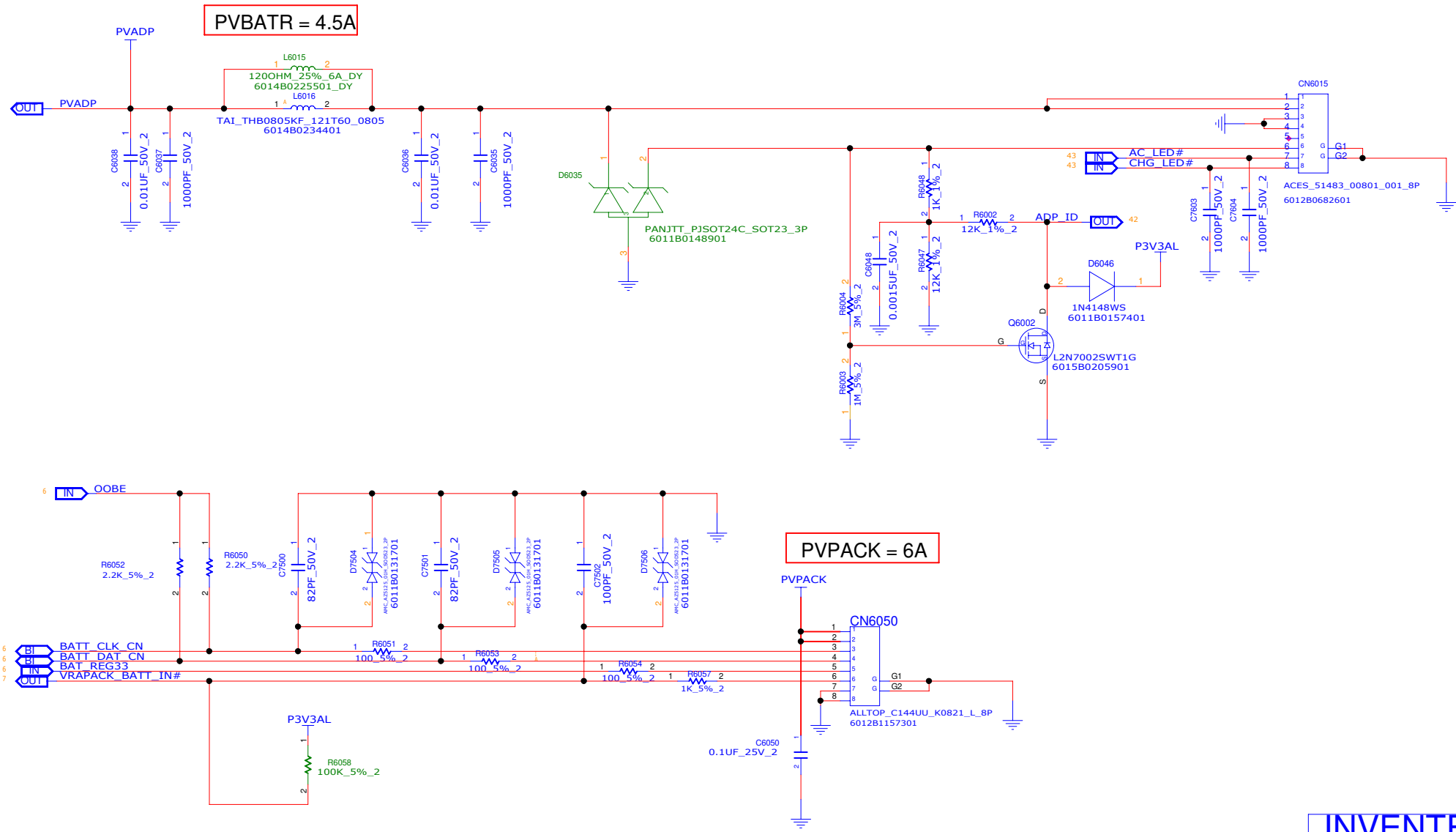
SELETOR

VER.04_20171113



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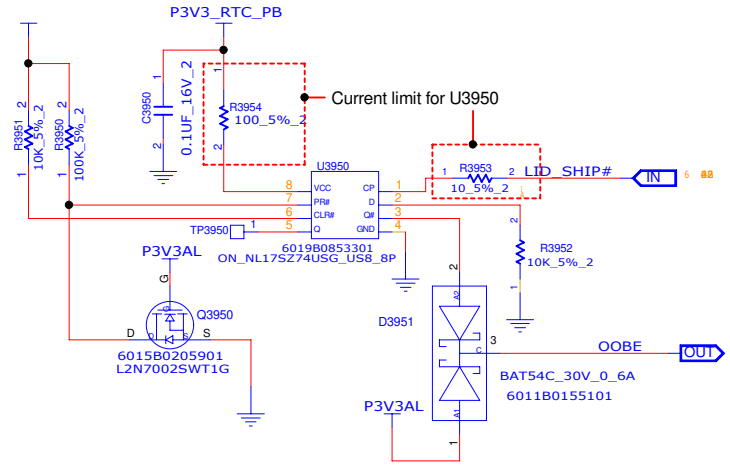
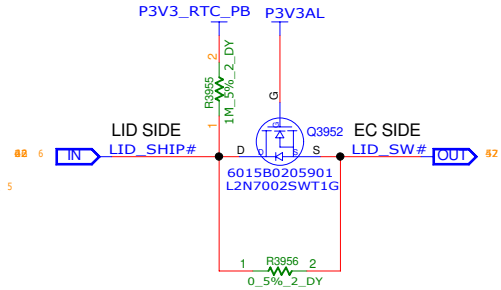
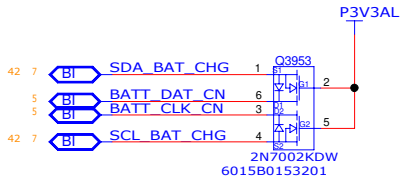
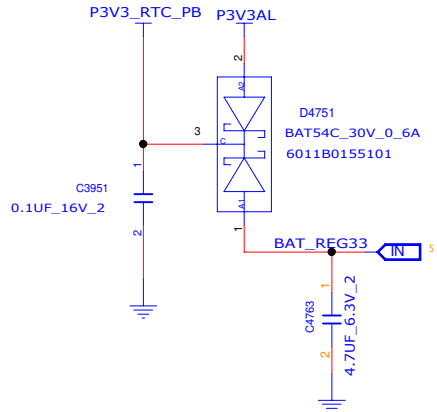
STORAGE MODE

VER.01_20170918









TRUTH TABLE

INPUT				OUTPUT		OPARATING MODE
PR#	CLR#	CP	D	Q	Q#	
L	H	X	X	H	L	ASYNCHRONOUS SET
H	L	X	X	L	H	ASYNCHRONOUS CLEAR
L	L	X	X	H	H	UNDETERNLNED
H	H	↑	H	H	L	LOAD AND READ REGISTER
H	H	↑	L	L	H	

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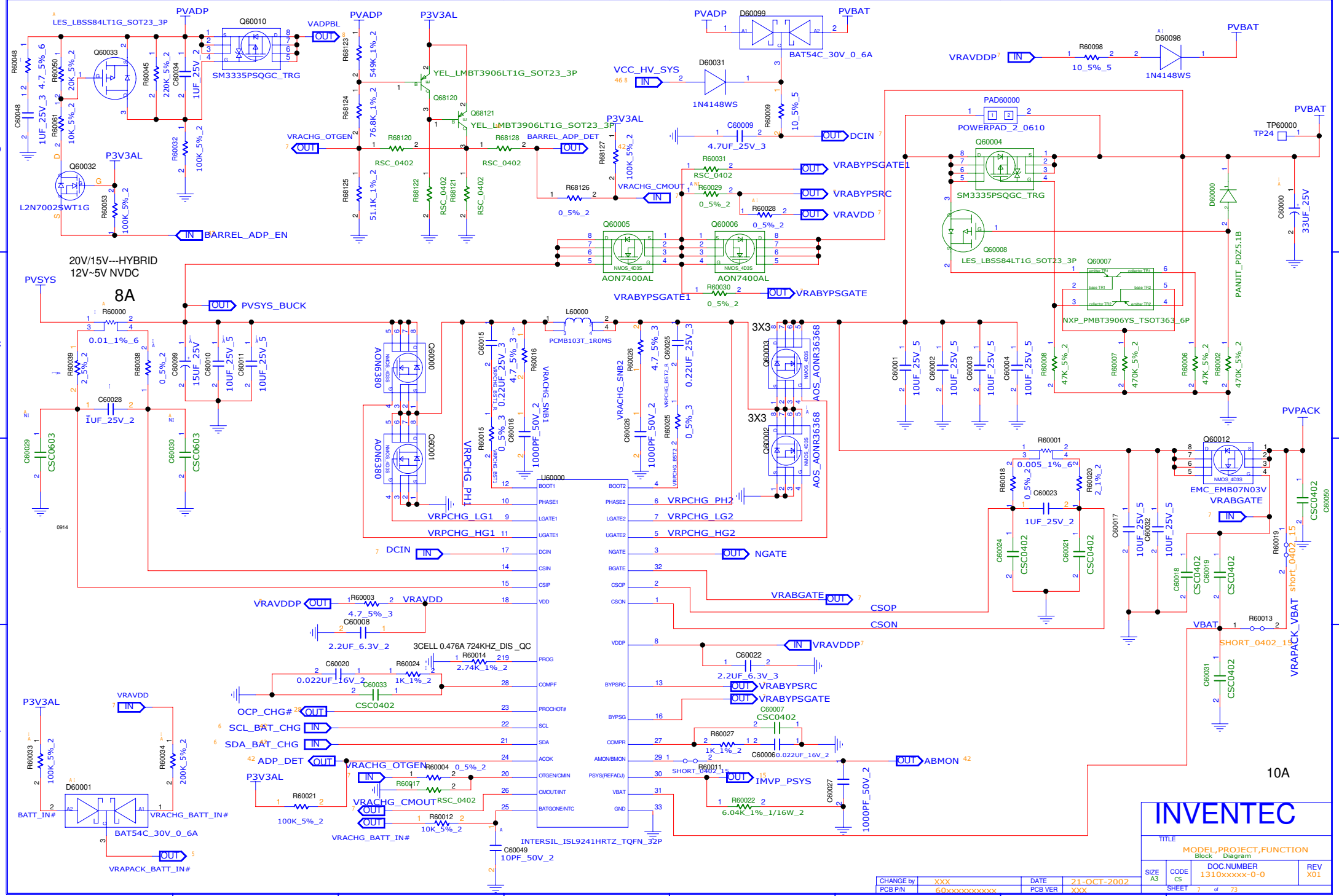
20V/15V---HYBRID
12V~5V NVDC
8A
10A
PVSYS
PVADP
PVBAT
PVPACK
VRAVDDP
VRAVDD
VRABYPSGATE1
VRABYPSGATE
VRABYPSRC
VRABGATE
DCIN
VCC_HV_SYS
VRACHG_OTGEN
VRACHG_CMOUT
VRACHG_BATT_IN#
VRAPACK_BATT_IN#
BARREL_ADP_EN
PVSYS_BUCK
VADPBL
BARREL_ADP_DET
ADP_DET
OCP_CHG#
SCL_BAT_CHG
SDA_BAT_CHG
VRPCHG_LG1
VRPCHG_HG1
VRPCHG_PH1
VRPCHG_PH2
VRPCHG_LG2
VRPCHG_HG2
NGATE
CSOP
CSON
ABMON
IMVP_PSYS
VBAT
VRAPACK_VBAT
LES_LBSS84LT1G_SOT23_3P
SM3335PSQGC_TRG
YEL_LMBT3906LT1G_SOT23_3P
L2N7002SWT1G
1N4148WS
BAT54C_30V_0_6A
POWERPAD_2_0610
AON7400AL
AON6380
AOS_AONR36368
NXP_PMBT3906YS_TSOT363_6P
PANJIT_PDZ5.1B
EMC_EMB07N03V
PCMB103T_1R0MS
INTERSIL_ISL9241HRTZ_TQFN_32P
3CELL 0.476A 724KHZ_DIS _QC
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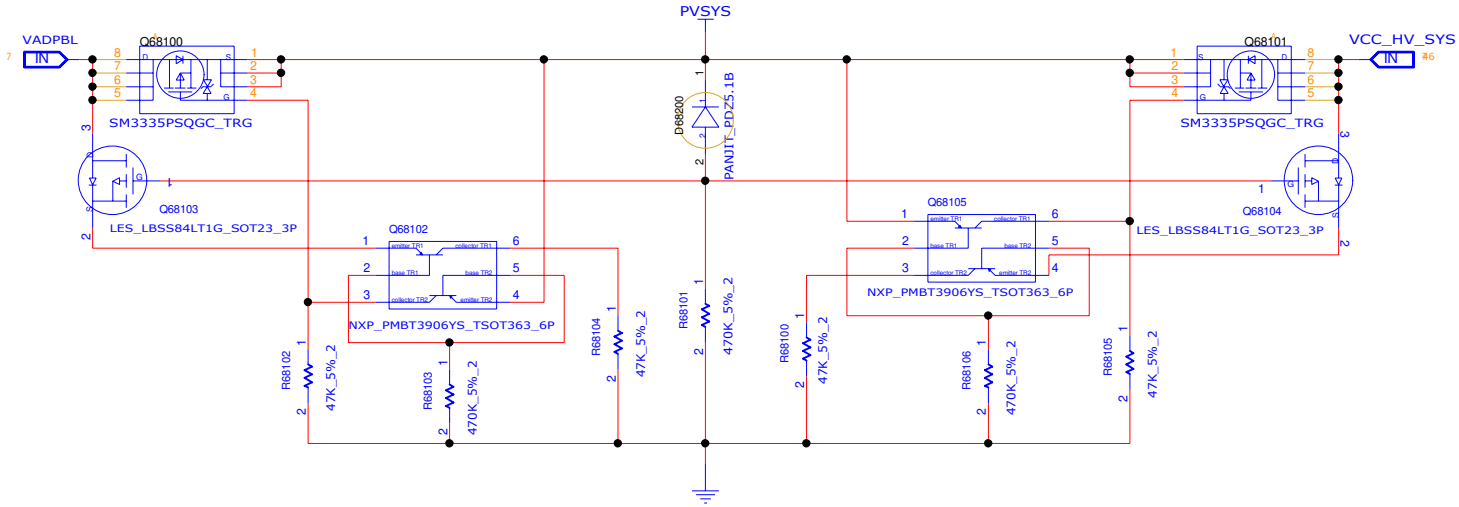

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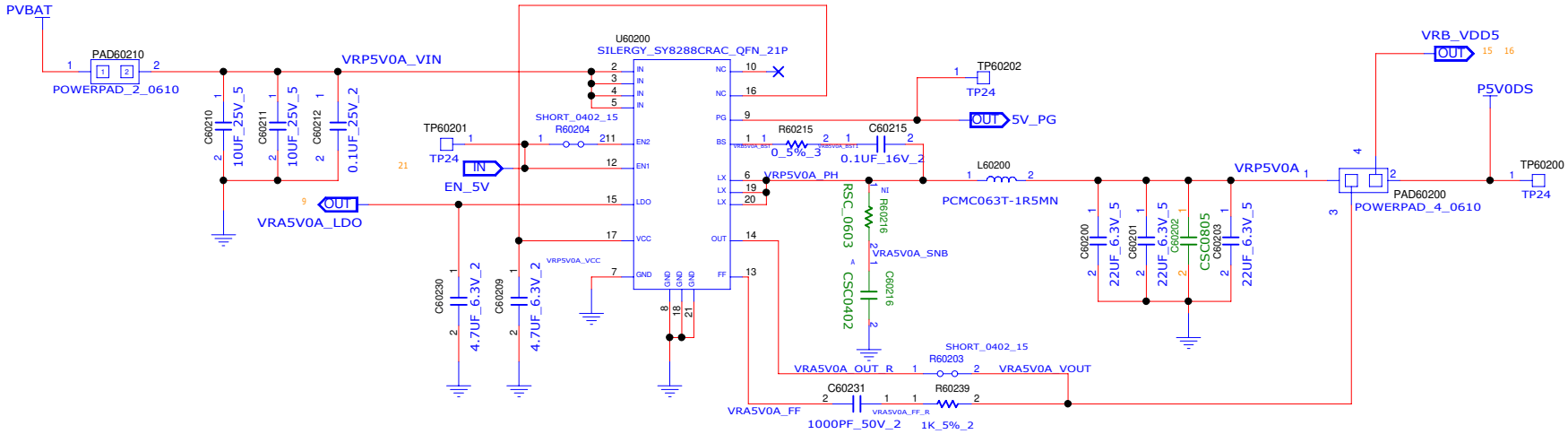

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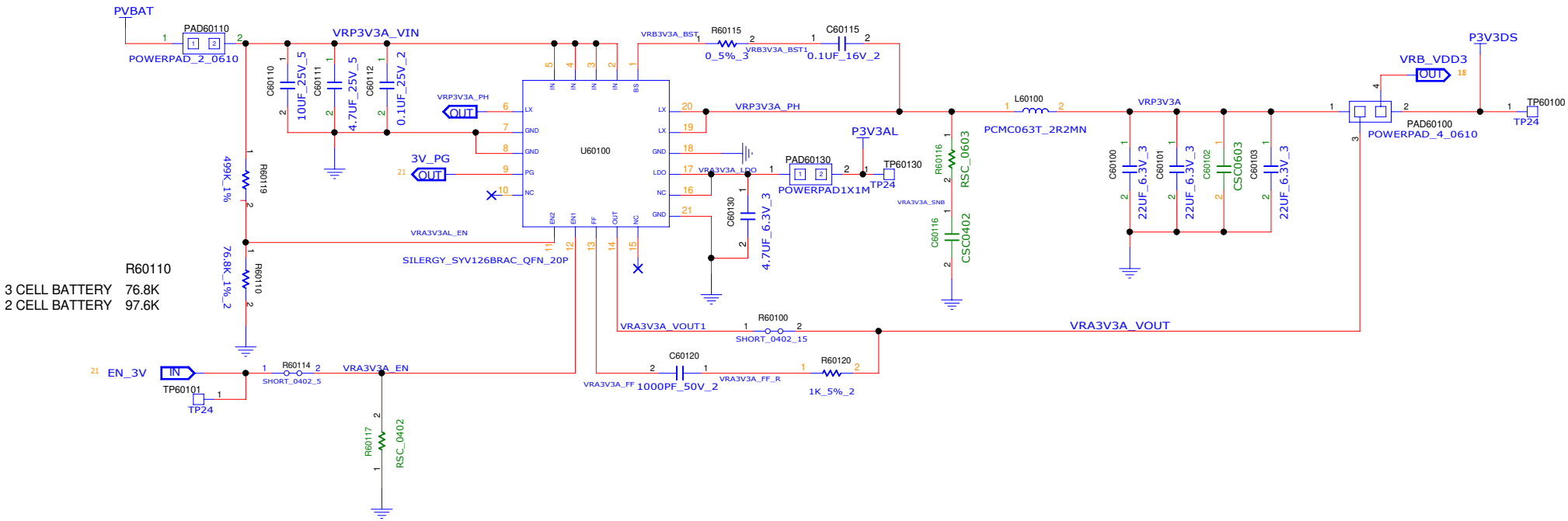

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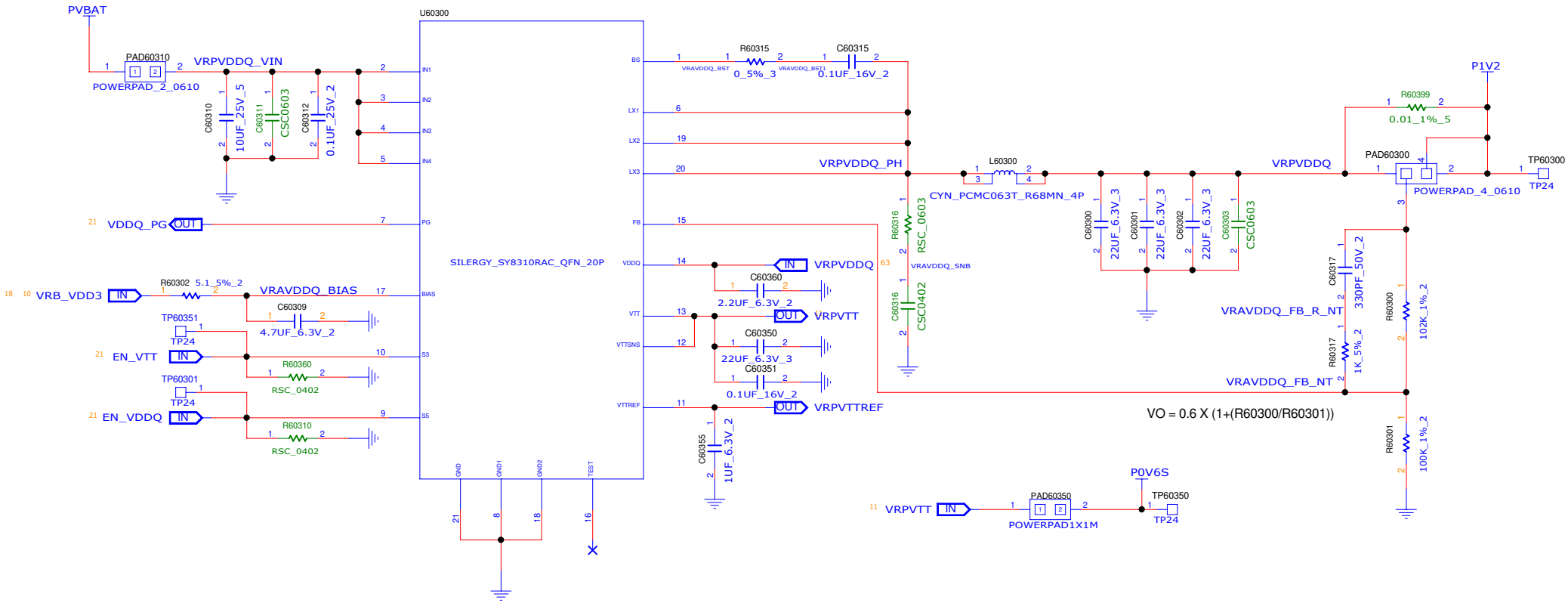

S3	S5	STATE	BUCK	VTTREF	VTT
High	High	S0	On	On	On
Low	High	S3	On	On	Off (High-Z)
Low	Low	S4/S5	Off (Discharge)	Off (Discharge)	Off (Discharge)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
S5/S3 Rising Threshold	$V_{S,R}$		1			V
S5/S3 Falling Threshold	$V_{S,F}$				0.3	V
S5 Voltage for USM Mode	$V_{S5,USM}$		1		1.8	V
S5 Voltage for PFM Mode	$V_{S5,PFM}$		2.1		V_{IN}	V

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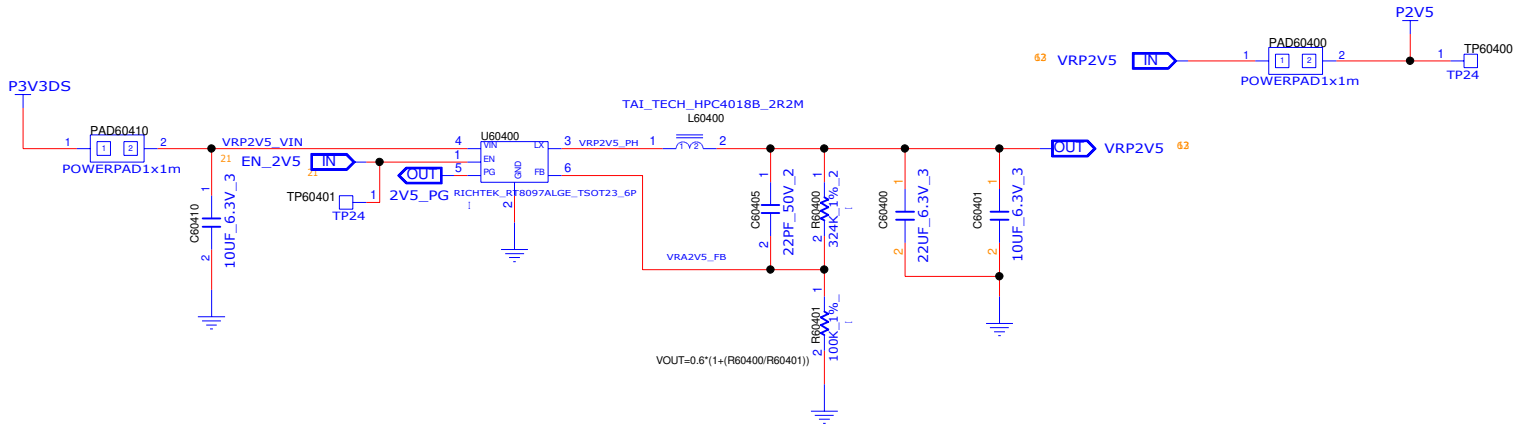

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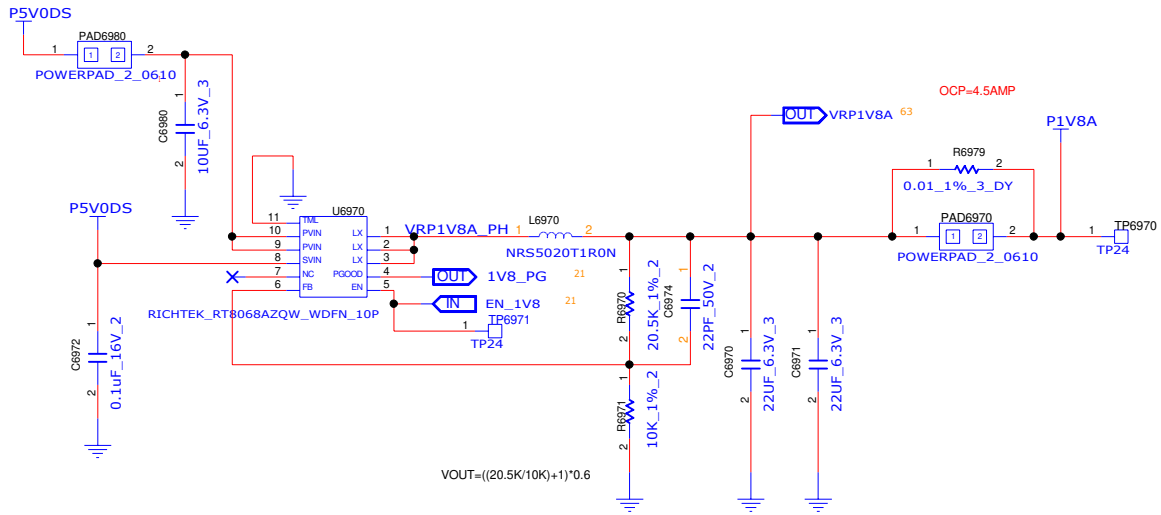

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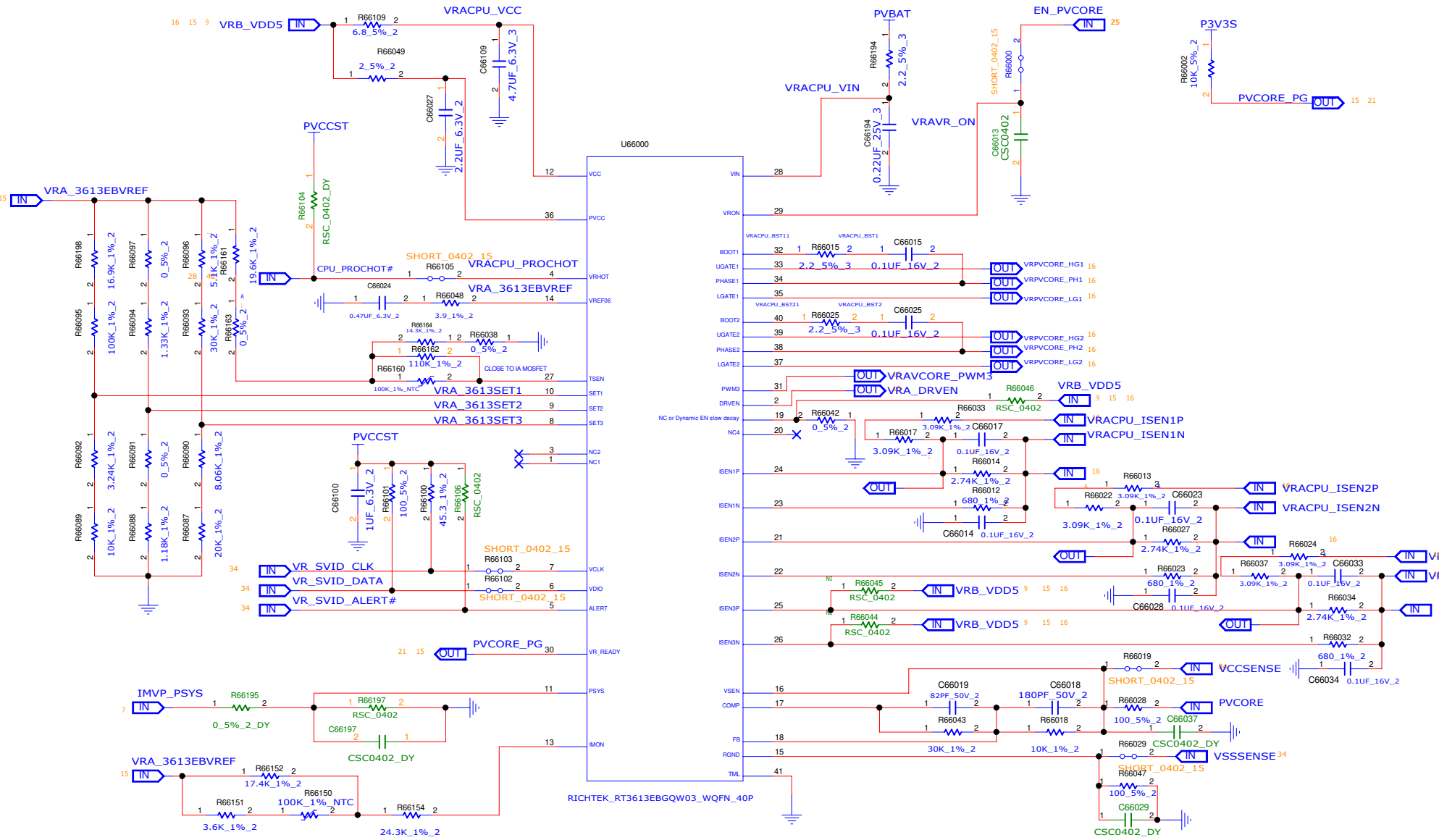

		IA				AUX			PL(W)	
ICL	Thermal sku	IccMax (A)	I_PL2 (A)	I_dI (A)	LL (mΩ)	IccMax (A)	I_PL2 (A)	I_dI (A)	PL1	PL2
U42	Baseline	54	25	46	2	32	14	12.8	15	46
U42	Performance	70	39	46	2	32	14	12.8	15	61
U22	Baseline/ Performance	55	30	46	2	32	14	12.8	15	50

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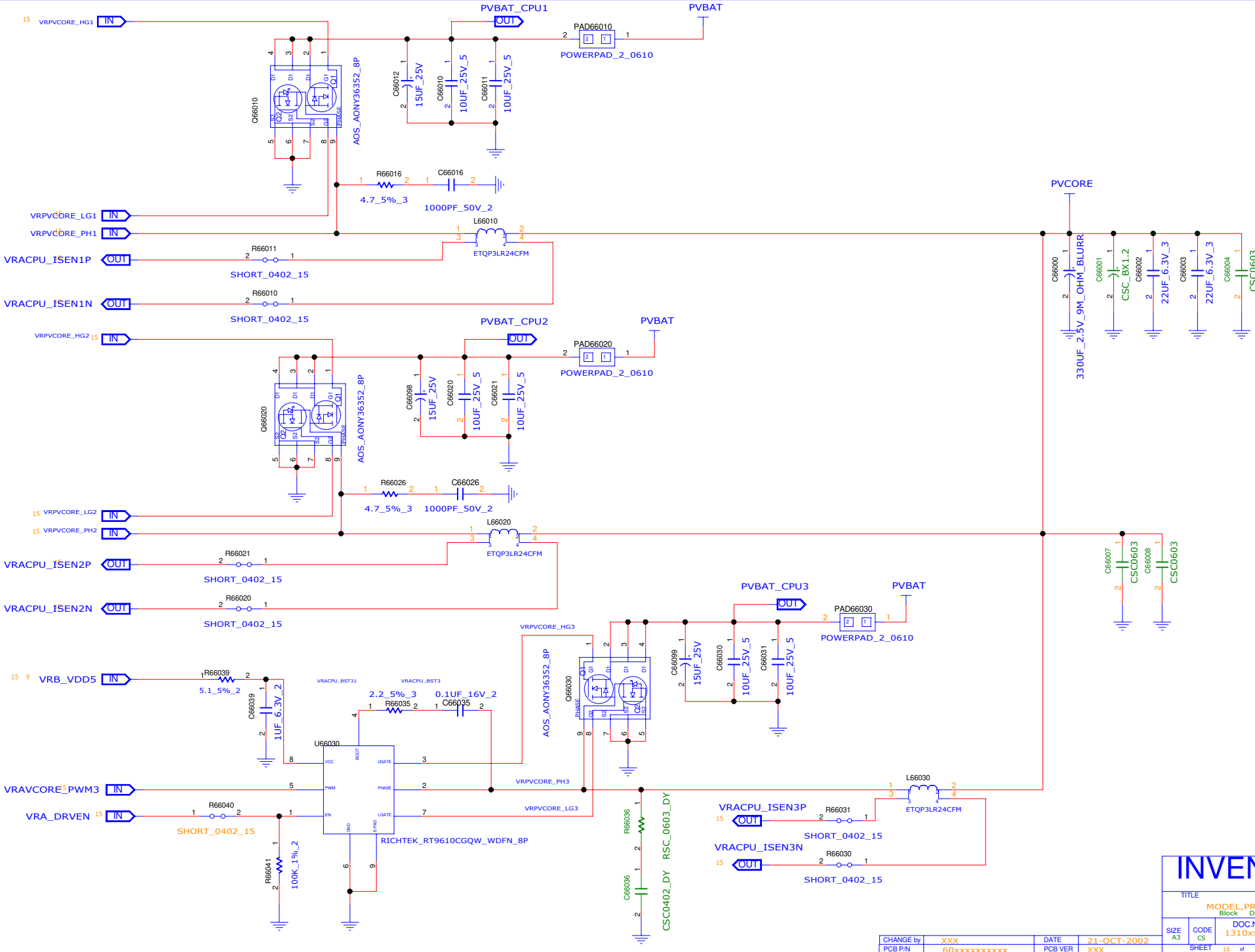
PVBAT_CPU1
PVBAT
PAD66010
POWERPAD_2_0610
VRPVCORE_HG1
VRPVCORE_LG1
VRPVCORE_PH1
AOS_AONY36352_8P
C66012 15UF_25V
C66010 10UF_25V_5
C66011 10UF_25V_5
R66016 4.7_5%_3
C66016 1000PF_50V_2
L66010 ETQP3LR24CFM
VRACPU_ISEN1P
VRACPU_ISEN1N
R66011 SHORT_0402_15
R66010 SHORT_0402_15
PVCORE
C66000 330UF_2.5V_9M_OHM_BLURR
C66001 CSC_BX1.2
C66002 22UF_6.3V_3
C66003 22UF_6.3V_3
C66004 CSC0603
PVBAT_CPU2
PAD66020
POWERPAD_2_0610
VRPVCORE_HG2
VRPVCORE_LG2
VRPVCORE_PH2
C66098 15UF_25V
C66020 10UF_25V_5
C66021 10UF_25V_5
R66026 4.7_5%_3
C66026 1000PF_50V_2
L66020 ETQP3LR24CFM
VRACPU_ISEN2P
VRACPU_ISEN2N
R66021 SHORT_0402_15
R66020 SHORT_0402_15
C66007 CSC0603
C66008 CSC0603
PVBAT_CPU3
PVBAT
PAD66030
POWERPAD_2_0610
VRPVCORE_HG3
VRPVCORE_LG3
VRPVCORE_PH3
C66099 15UF_25V
C66030 10UF_25V_5
C66031 10UF_25V_5
VRB_VDD5
R66039 5.1_5%_2
C66039 1UF_6.3V_2
VRACPU_BST31
VRACPU_BST3
R66035 2.2_5%_3
C66035 0.1UF_16V_2
U66030
RICHTEK_RT9610CGQW_WDFN_8P
VRAVCORE_PWM3
VRA_DRVEN
R66040 SHORT_0402_15
R66041 100K_1%_2
R66036 RSC_0603_DY
C66036 CSC0402_DY
L66030 ETQP3LR24CFM
VRACPU_ISEN3P
VRACPU_ISEN3N
R66031 SHORT_0402_15
R66030 SHORT_0402_15
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Ice Lake	2 phase	3 phase
R66013	2.61K (6013A008810M)	3.09K
R66014	3.01K (6013A008810W)	2.74K
R66017	2.61K (6013A008810M)	3.09K
R66022	2.61K (6013A008810M)	3.09K
R66027	3.01K (6013A008810W)	2.74K
R66033	2.61K (6013A008810M)	3.09K
R66043	27.4K (6013A0014401)	30K
R66088	1.15K (6013B0108301)	1.18K
R66092	3.65K (6013A0088207)	3.24K
R66094	1.37K (6013B0124201)	1.33K
R66095	60.4K (6013A0073401)	100K
R66151	2.05K (6013A008810B)	3.6K
R66152	18.7K (6013A0017101)	17.4K
R66154	28.7K (6013A0017401)	24.3K
R66198	27.4K (6013A0014401)	16.9K
R66035	NI	2.2
R66039	NI	5.1
R66040	NI	0
R66041	NI	100K
C66035	NI	0.1UF
C66039	NI	1UF
C66030	NI	10UF
C66031	NI	10UF
R66030	NI	SHORT_0402_15
R66031	NI	SHORT_0402_15
U66030	NI	RT9610CGQW
Q66030	NI	AONY36352
L66030	NI	PCME063T-R24MS1R195
PAD66030	NI	I
R66024	NI	3.09K
R66032	NI	680
R66034	NI	2.74K
R66037	NI	3.09K
C66033	NI	0.1UF
C66034	NI	0.1UF
R66044	10K (60130B1030ZT)	NI
R66045	10K (60130B1030ZT)	NI
C66099	NI	15UF_25V (6010B0185101)

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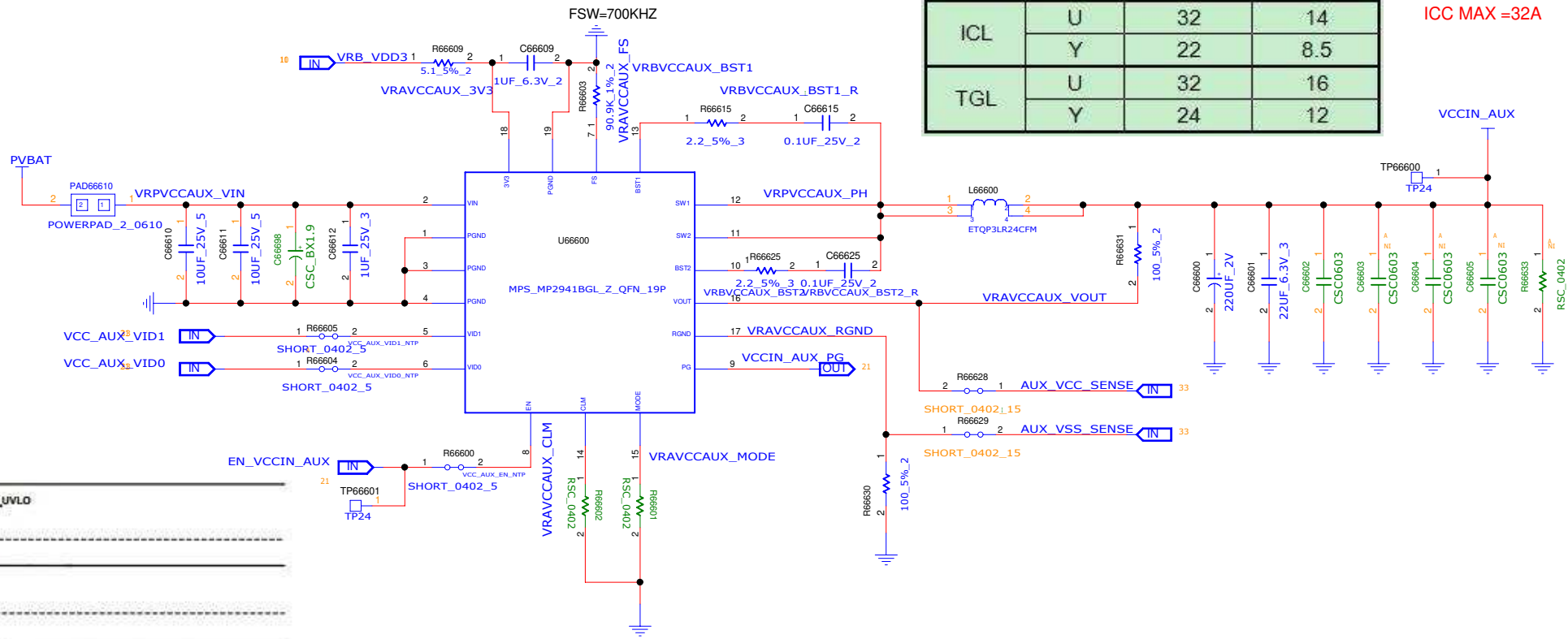
Platfrom		IccMAX (A)	TDC (A)
ICL	U	32	14
	Y	22	8.5
TGL	U	32	16
	Y	24	12

TDC=16A
ICC MAX =32A



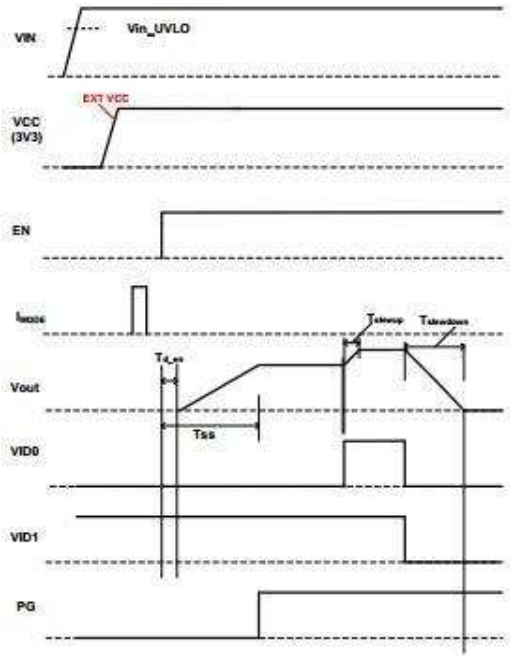


Figure 4—Start-up power sequence

Table 1—MODE Select

State	Interleaving	VID Down	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90 K
M3	Y	Decay	150 K
M4	N	Decay	>230 K or float

Table 2—FS Selection

State	Fs	Resistor to GND
M1	500kHz	0
M2	700kHz	90 K
M3	1000kHz	150 K
M4	1200kHz	>230 K or float

Table 3—VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table 4—CLM/Phase Selection

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90 K
M3	13A	150 K
M4	16A	>230 K or float

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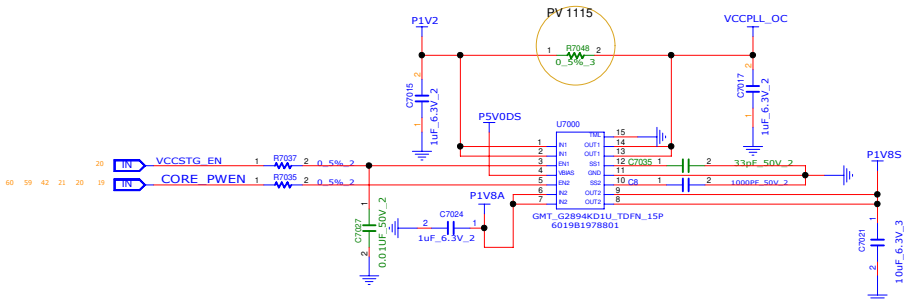
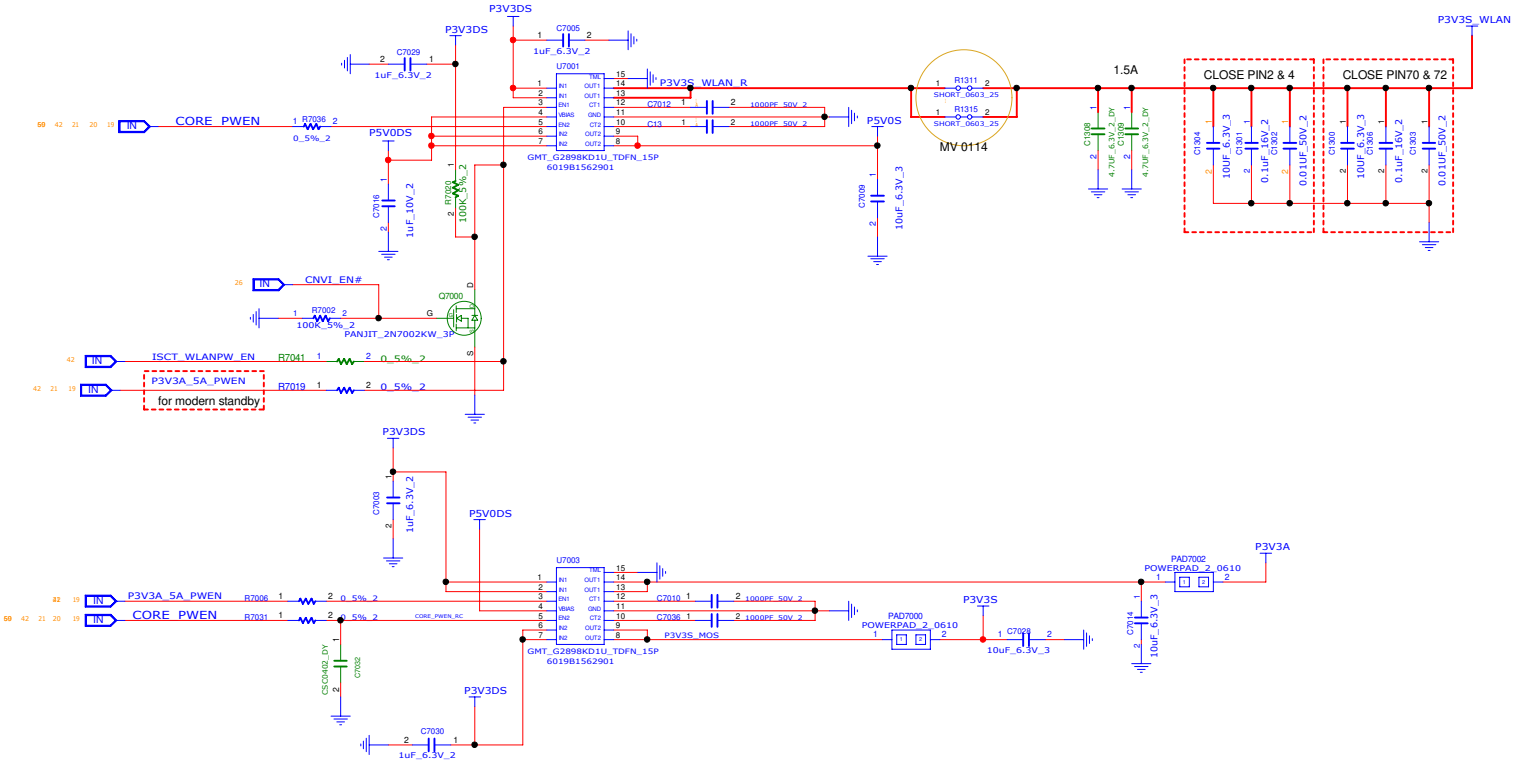


WWAN SKU



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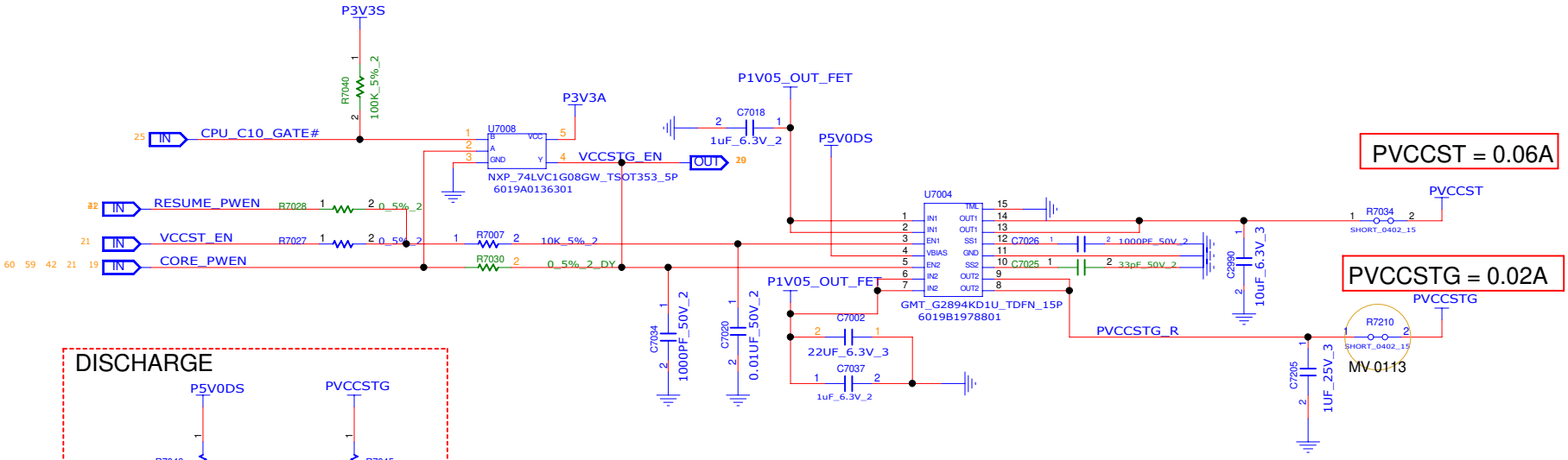

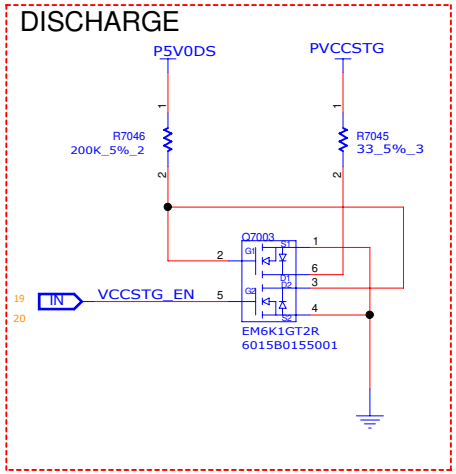

Differences between Power Maps

Volume	Premium
VccSTG and VccST are merged and gated by SLP_S4#	VccSTG gated by {CPU_C10_GATE#}
VccPLL_OC is supplied directly from VDDQ	VccPLL_OC is supplied from VDDQ through a load switch
VCC1P8A on the CPU is supplied directly by V1.8A	VCC1P8A is supplied from V1.8A and gated by *CPU_C10_GATE #*
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC _V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load
Various system devices share load switches	Various system devices have their own independent load switches

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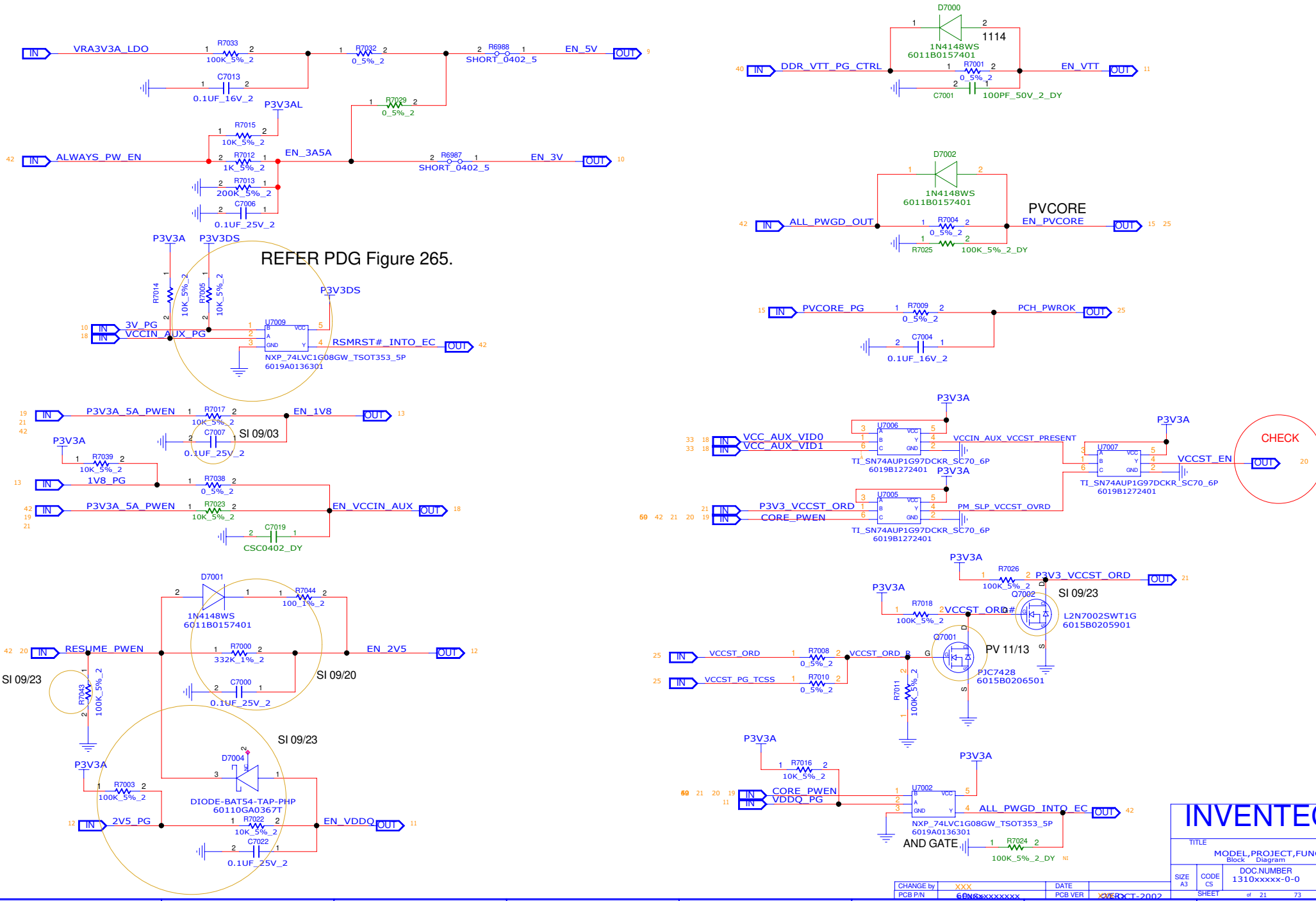
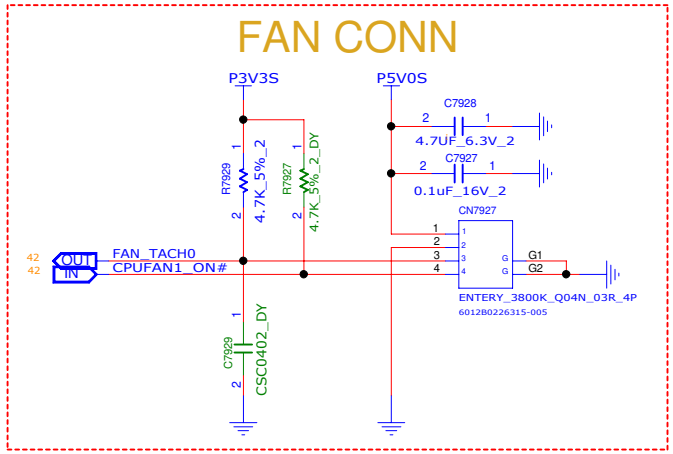

VRA3V3A_LDO
R7033 100K_5%_2
C7013 0.1UF_16V_2
R7032 0_5%_2
R6988 SHORT_0402_5
EN_5V
R7029 0_5%_2
P3V3AL
R7015 10K_5%_2
ALWAYS_PW_EN
R7012 1K_5%_2
EN_3A5A
R7013 200K_5%_2
C7006 0.1UF_25V_2
R6987 SHORT_0402_5
EN_3V
REFER PDG Figure 265.
P3V3A
P3V3DS
R7014 10K_5%_2
R7005 10K_5%_2
3V_PG
VCCIN_AUX_PG
U7009
NXP_74LVC1G08GW_TSOT353_5P
6019A0136301
RSMRST#_INTO_EC
P3V3A_5A_PWEN
R7017 10K_5%_2
EN_1V8
C7007 0.1UF_25V_2
SI 09/03
R7039 10K_5%_2
1V8_PG
R7038 0_5%_2
R7023 10K_5%_2
EN_VCCIN_AUX
C7019 CSC0402_DY
D7001
1N4148WS
6011B0157401
R7044 100_1%_2
RESUME_PWEN
R7000 332K_1%_2
EN_2V5
C7000 0.1UF_25V_2
SI 09/20
SI 09/23
R7043 100K_5%_2
D7004
DIODE-BAT54-TAP-PHP
60110GA0367T
R7003 100K_5%_2
2V5_PG
R7022 10K_5%_2
EN_VDDQ
C7022 0.1UF_25V_2
D7000
1N4148WS
6011B0157401
1114
DDR_VTT_PG_CTRL
R7001 0_5%_2
EN_VTT
C7001 100PF_50V_2_DY
D7002
1N4148WS
6011B0157401
ALL_PWGD_OUT
R7004 0_5%_2
PVCORE
EN_PVCORE
R7025 100K_5%_2_DY
PVCORE_PG
R7009 0_5%_2
PCH_PWROK
C7004 0.1UF_16V_2
P3V3A
VCC_AUX_VID0
VCC_AUX_VID1
U7006
TI_SN74AUP1G97DCKR_SC70_6P
6019B1272401
VCCIN_AUX_VCCST_PRESENT
U7007
VCCST_EN
CHECK
P3V3_VCCST_ORD
CORE_PWEN
U7005
PM_SLP_VCCST_OVRD
R7026 100K_5%_2
P3V3_VCCST_ORD
SI 09/23
Q7002
L2N7002SWT1G
6015B0205901
R7018 100K_5%_2
VCCST_ORD#
Q7001
PV 11/13
PJC7428
6015B0206501
VCCST_ORD
VCCST_PG_TCSS
R7008 0_5%_2
R7010 0_5%_2
R7011 100K_5%_2
R7016 10K_5%_2
CORE_PWEN
VDDQ_PG
U7002
NXP_74LVC1G08GW_TSOT353_5P
6019A0136301
ALL_PWGD_INTO_EC
AND GATE
R7024 100K_5%_2_DY
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET of 21 73
CHANGE by XXX
PCB P/N 60NXXXXXXXX
DATE
PCB VER
OCT-2002

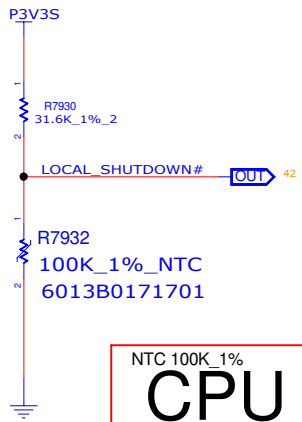
FAN & THERMAL

FOR BIG CORE USE

VER.04_20171011

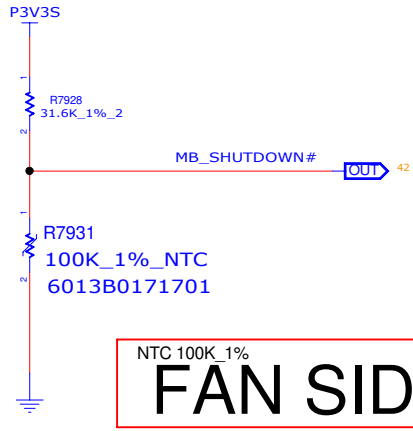


THERMAL



NTC 100K_1%

CPU SIDE



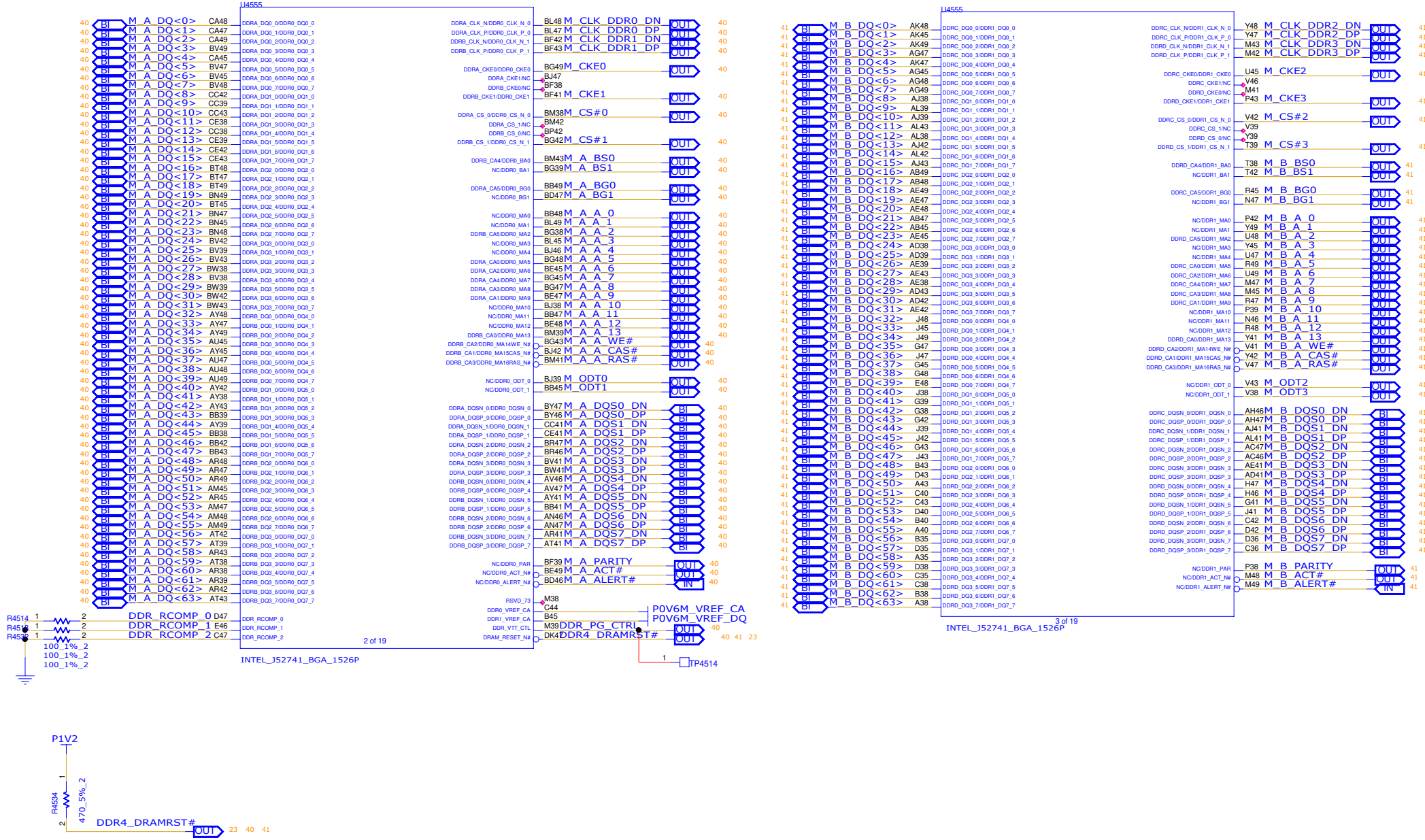
NTC 100K_1%

FAN SIDE

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION THERMAL & FAN		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 22 of 73			

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

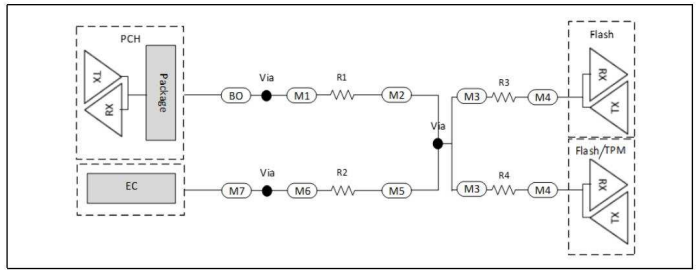


INVENTEC

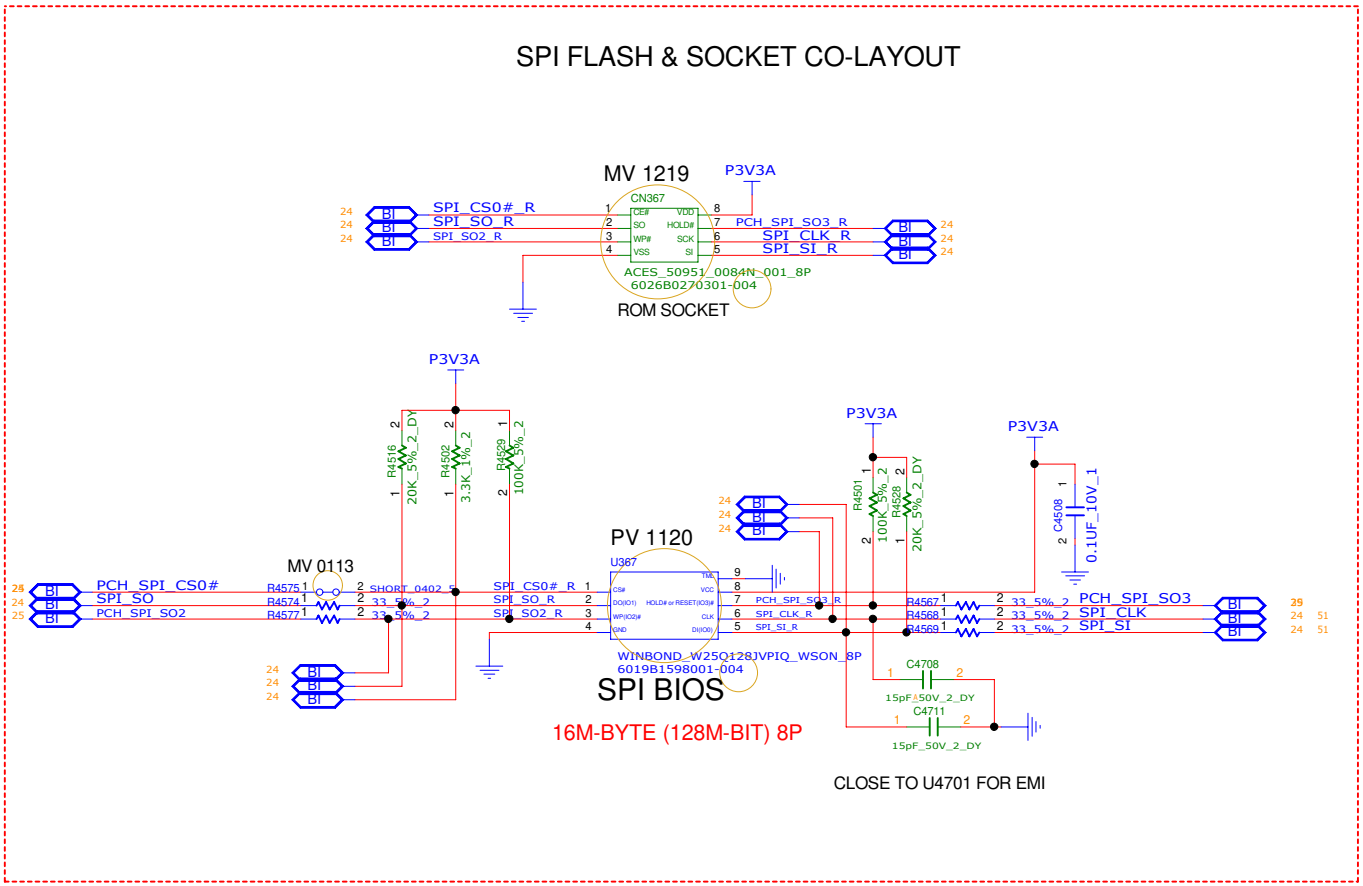
TITLE: MODEL,PROJECT,FUNCTION (MCP5-DDR)					
CHANGE by: XXX	DATE: 21-OCT-2002	SIZE: A3	CODE: CS	DOC.NUMBER: 1310xxxxx-0-0	REV: X01
PCB P/N: 60xxxxxxxxx	PCB VER: XXX			SHEET 23 of 73	

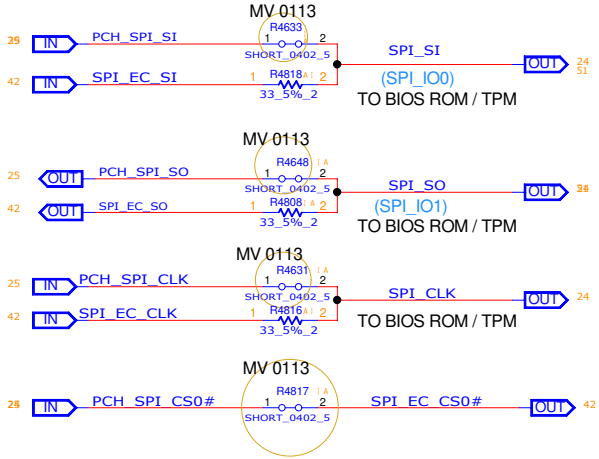
CORE - SPI ROM

Figure 6-84. SPI0 2-Load(1 Flash and 1 Flash/1 TPM) EC G3 Flash Sharing with Wire-OR Topology



SPI FLASH & SOCKET CO-LAYOUT





PACKAGE TYPE	DENSITY	PRODUCT NUMBER	TOP SIDE MARKING
S SOIC-8 208-mil	128M-bit	W25Q128JVSIQ	25Q128JVSQ
F SOIC-16 300-mil	128M-bit	W25Q128JVFIQ	25Q128JVFQ
P WSON-8 6x5-mm	128M-bit	W25Q128JVPIQ	25Q128JVPQ
E WSON-8 8x6-mm	128M-bit	W25Q128JVEIQ	25Q128JVEQ
B(1) TFBGA-24 8x6-mm (5x5 Ball Array)	128M-bit	W25Q128JVBIQ	25Q128JVBQ
C(1) TFBGA-24 8x6-mm (6x4 Ball Array)	128M-bit	W25Q128JVCIQ	25Q128JVCQ

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CPU-2

SPI
SMBUS
SYSTEM SEQUENCE

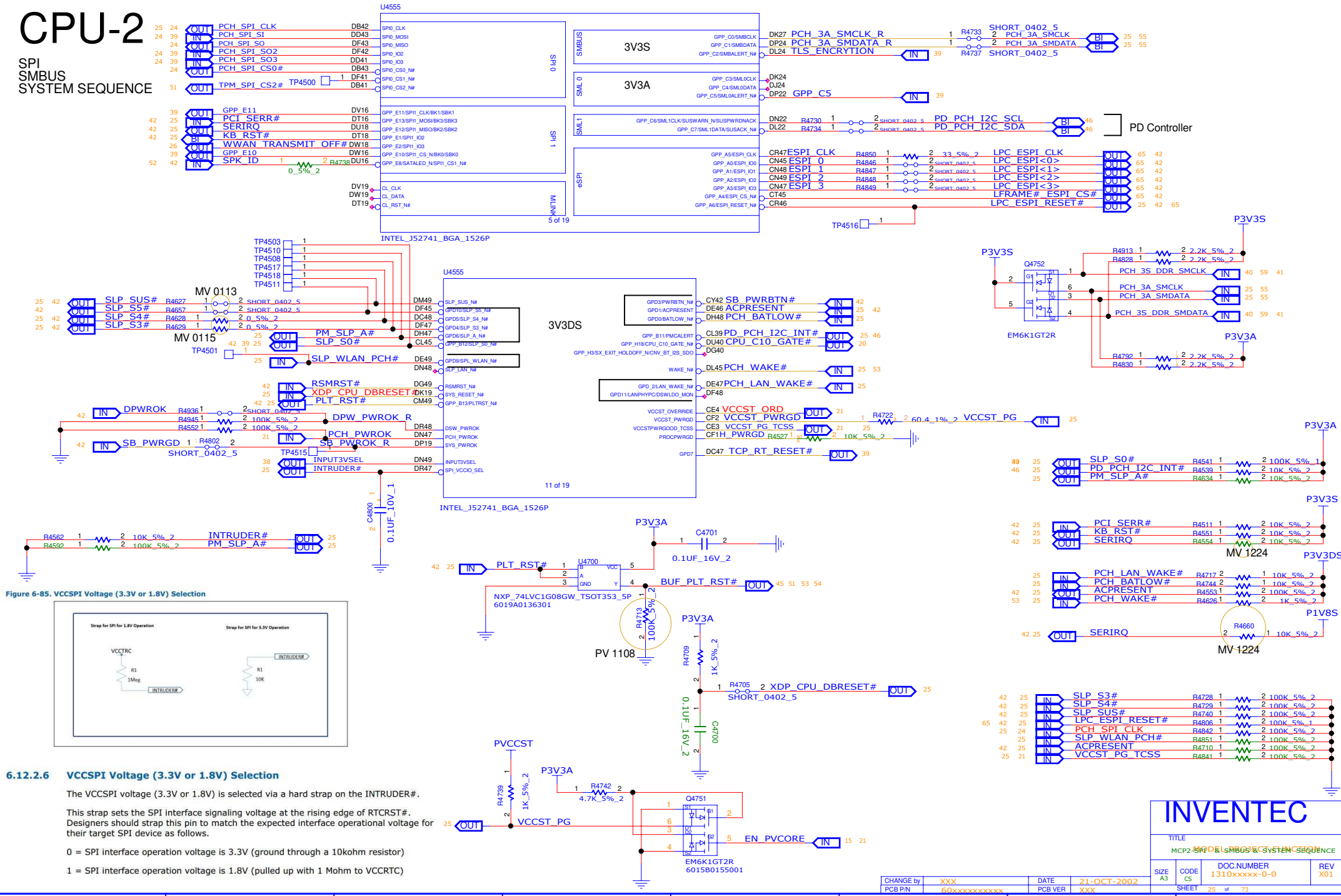


Figure 6-85. VCCSPI Voltage (3.3V or 1.8V) Selection

6.12.2.6 VCCSPI Voltage (3.3V or 1.8V) Selection

The VCCSPI voltage (3.3V or 1.8V) is selected via a hard strap on the INTRUDER#.

This strap sets the SPI interface signaling voltage at the rising edge of RTCRST#. Designers should strap this pin to match the expected interface operational voltage for their target SPI device as follows.

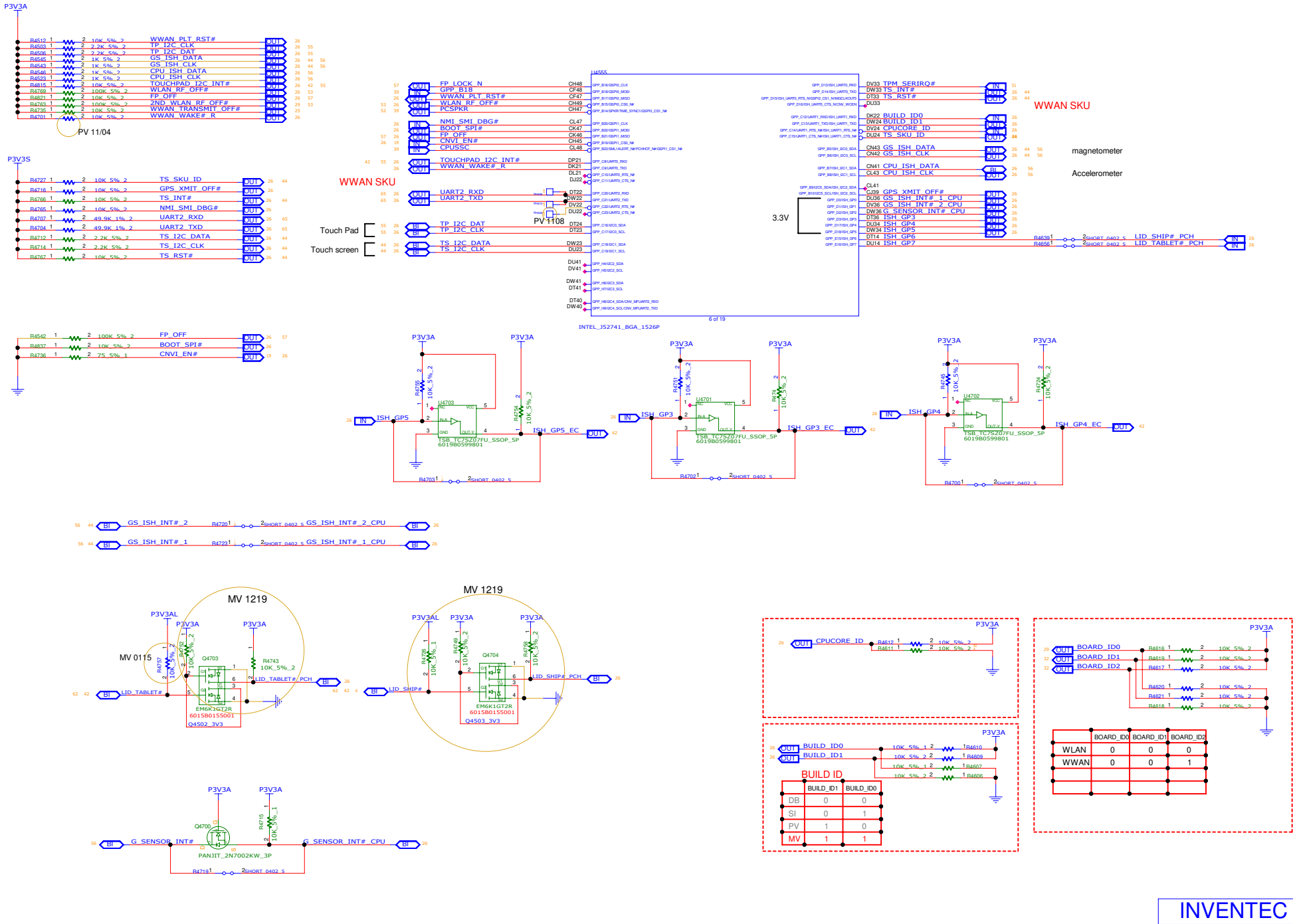
0 = SPI interface operation voltage is 3.3V (ground through a 10kohm resistor)

1 = SPI interface operation voltage is 1.8V (pulled up with 1 Mohm to VCCRTC)

INVENTEC

TITLE: MCP2-SPI & SMBUS & SYSTEM SEQUENCE			
SIZE: A3	CODE: CS	DOC.NUMBER: 1310xxxxx-0-0	REV: X01
CHANGE by: XXX	DATE: 21-OCT-2002	SHEET: 25 of 73	
PCB P/N: 60xxxxxxxxx	PCB VER: XXX		

CPU-3 GPIO



REFERENCE NUMBER:4500~4699

CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

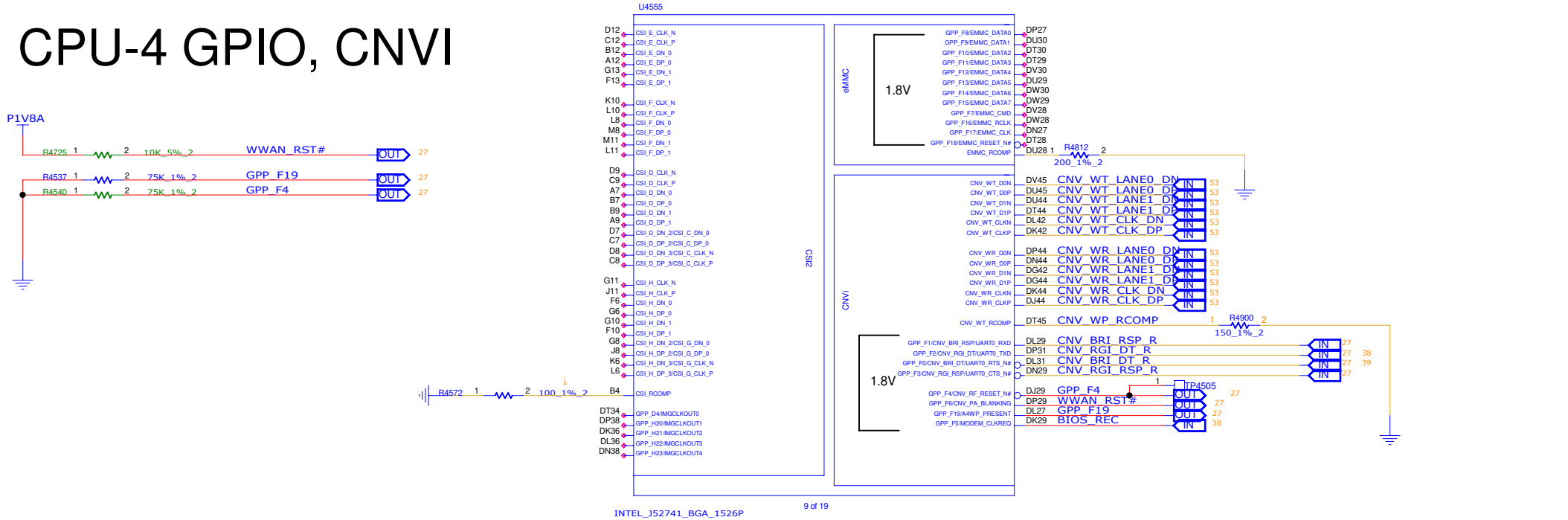
INVENTEC

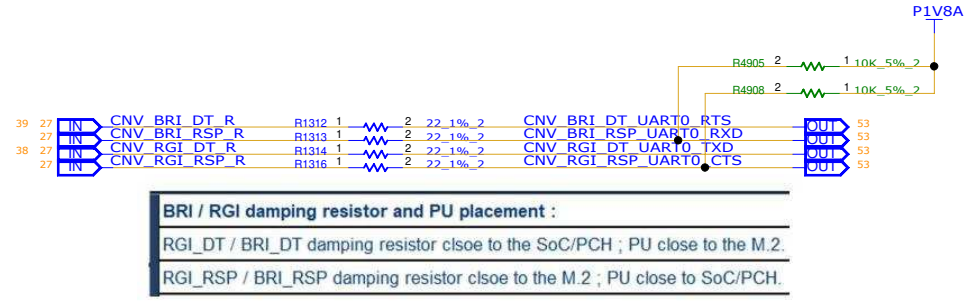
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 26 of 73

CPU-4 GPIO, CNVI





INVENTEC

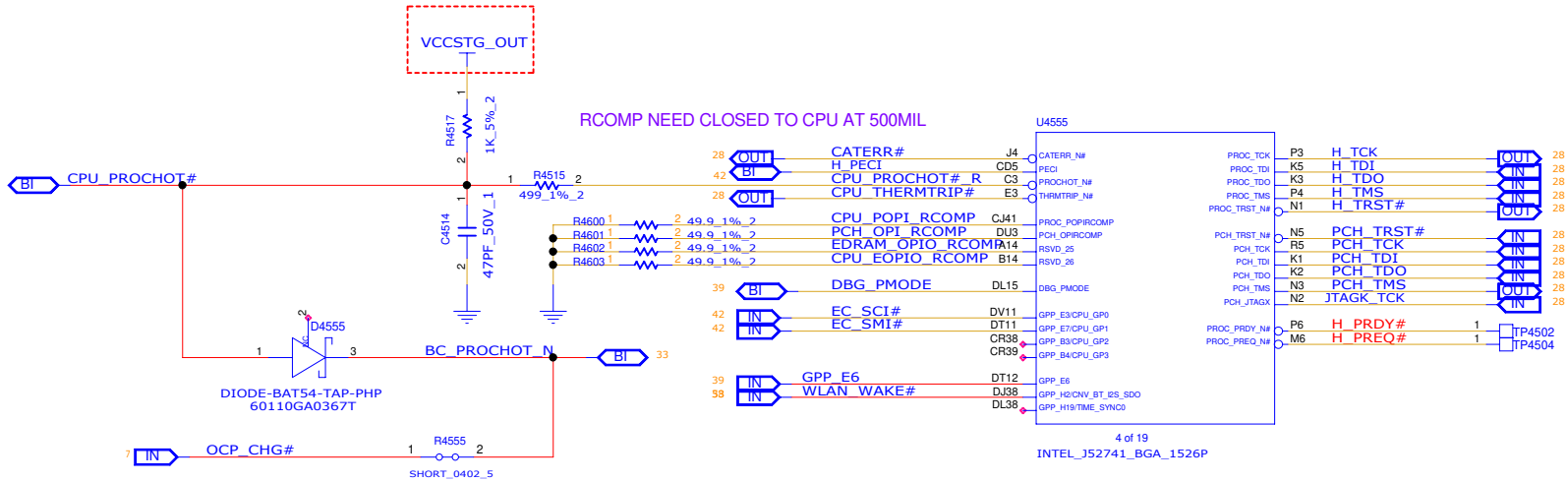
TITLE: MODEL PROJECT FUNCTION
MCP4-GPIO & CNVI

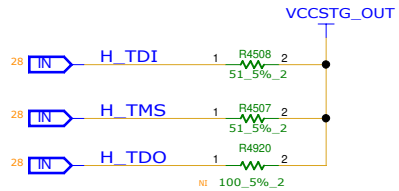
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

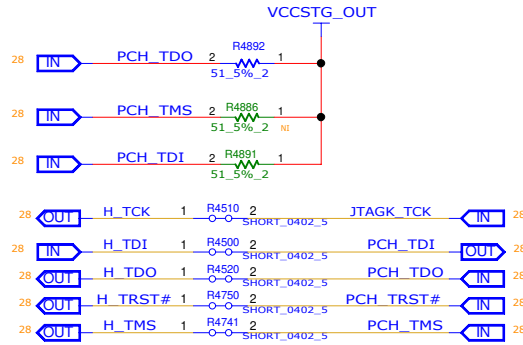
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

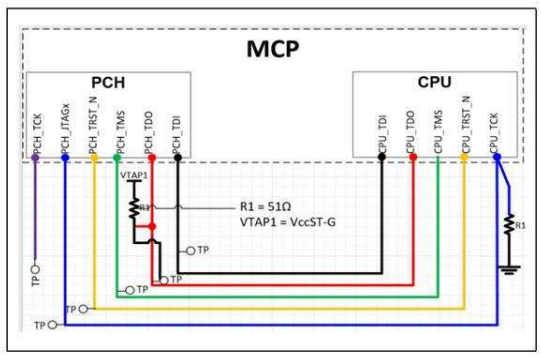
SHEET 27 of 73

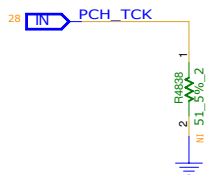
CPU-5 MISC

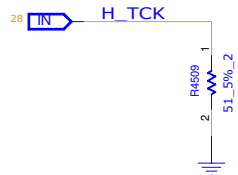












INVENTEC

TITLE: MCP1 MISC

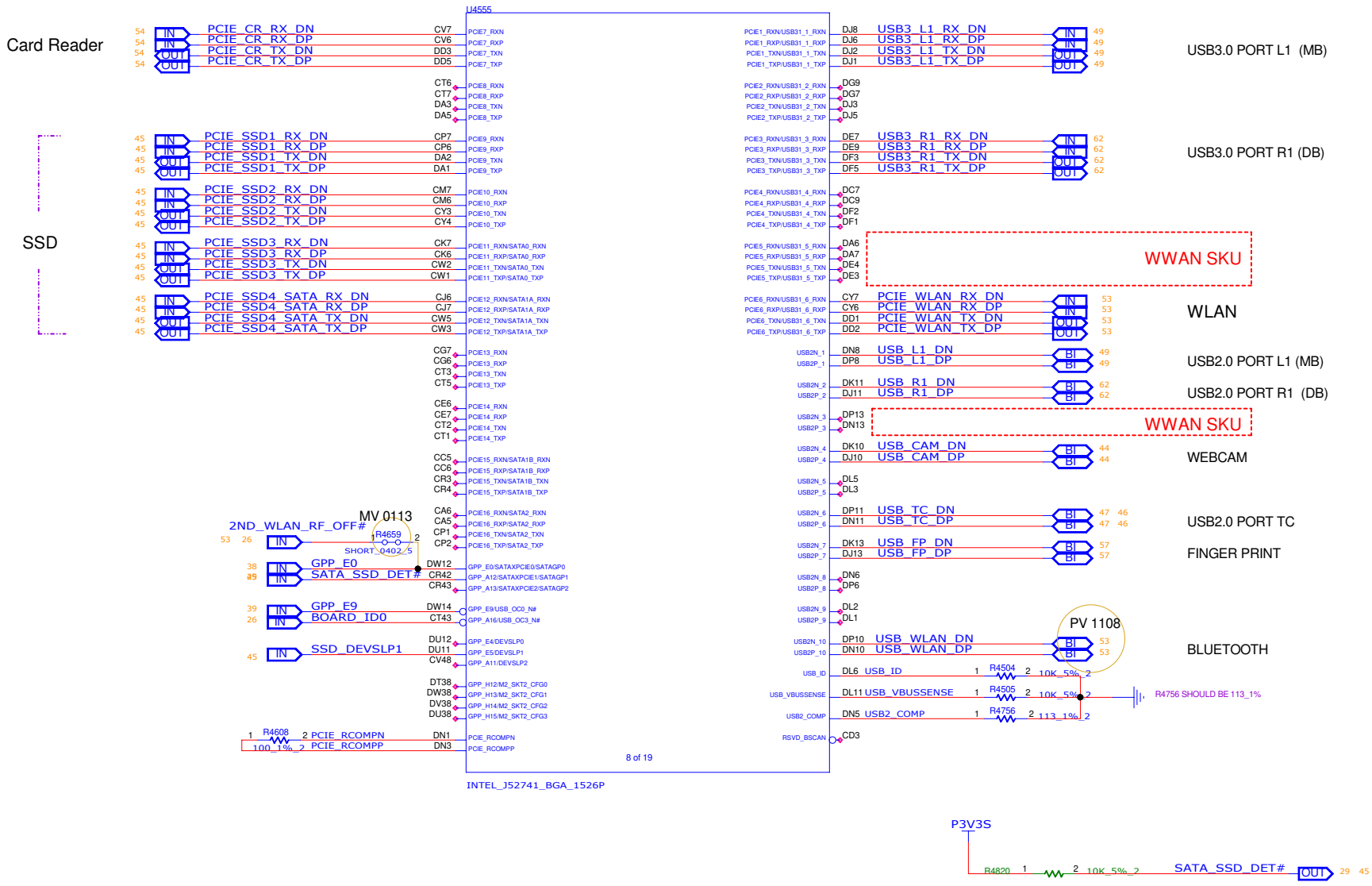
MODEL, PROJECT, FUNCTION

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 28 of 73

CPU-6 PCIE, USB



INVENTEC

TITLE: MCP6, PCIE & USB

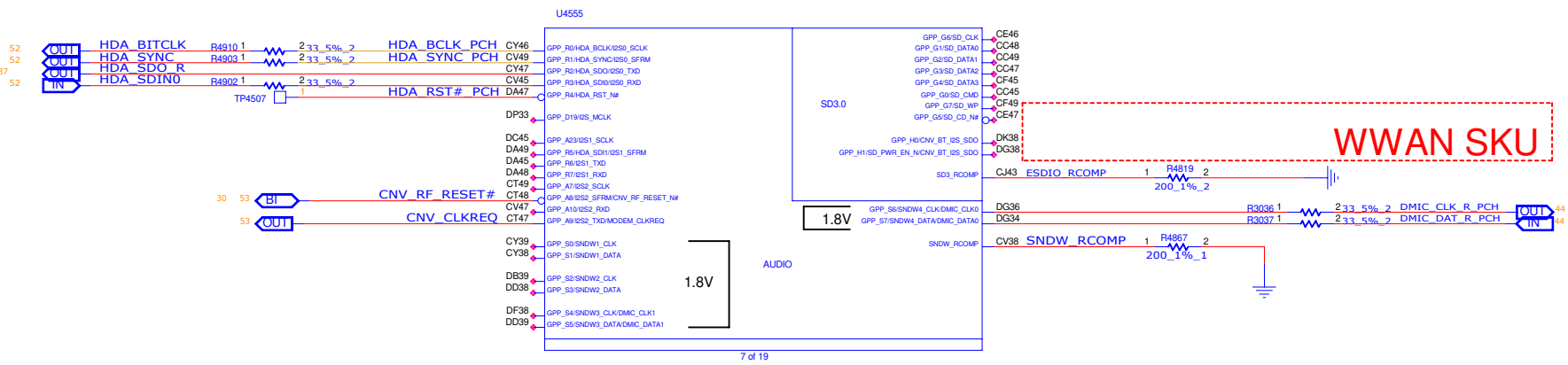
MODEL PROJECT FUNCTION

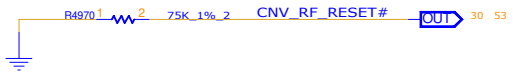
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 29 of 73

CPU-7 RTC, AUDIO, SATA





WWAN SKU

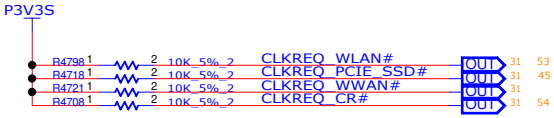
INVENTEC

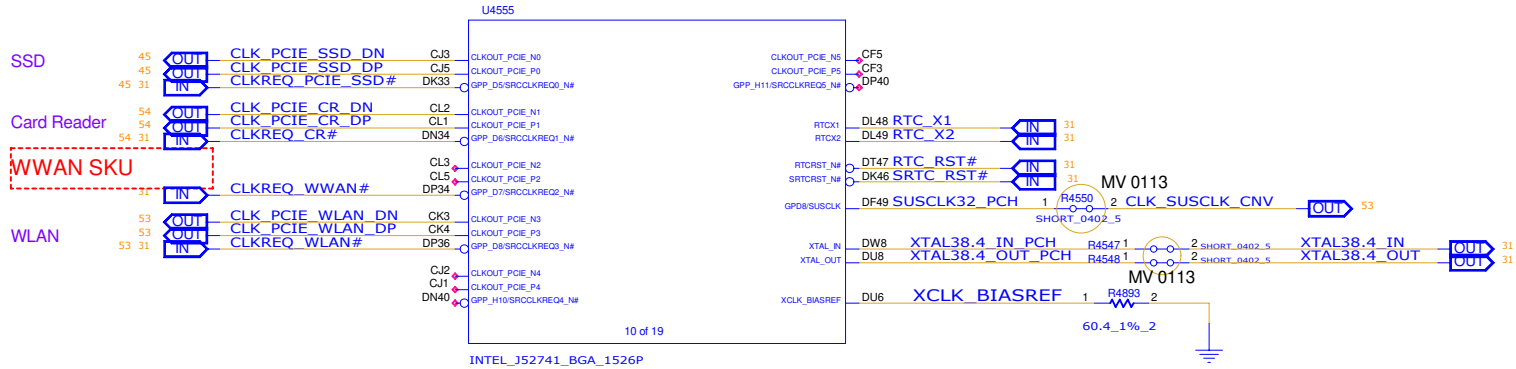
TITLE	MODEL,PROJECT,FUNCTION MCP7-RTC & AUDIO & SATA		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 30 of 73			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

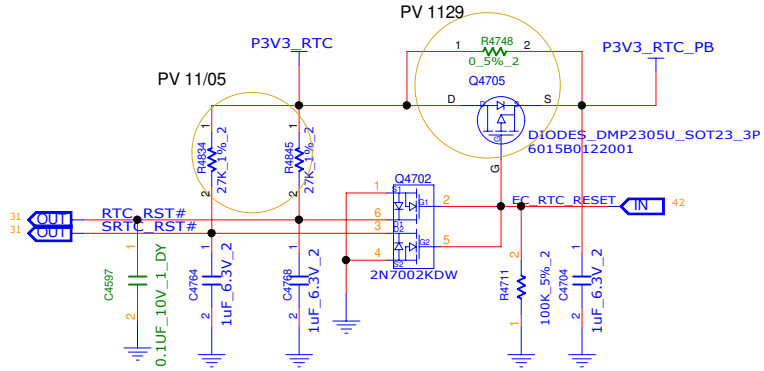
CPU-8

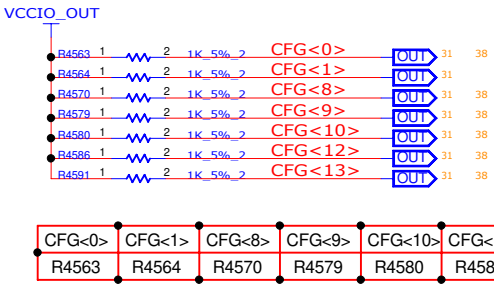
CLOCK, RESERVED



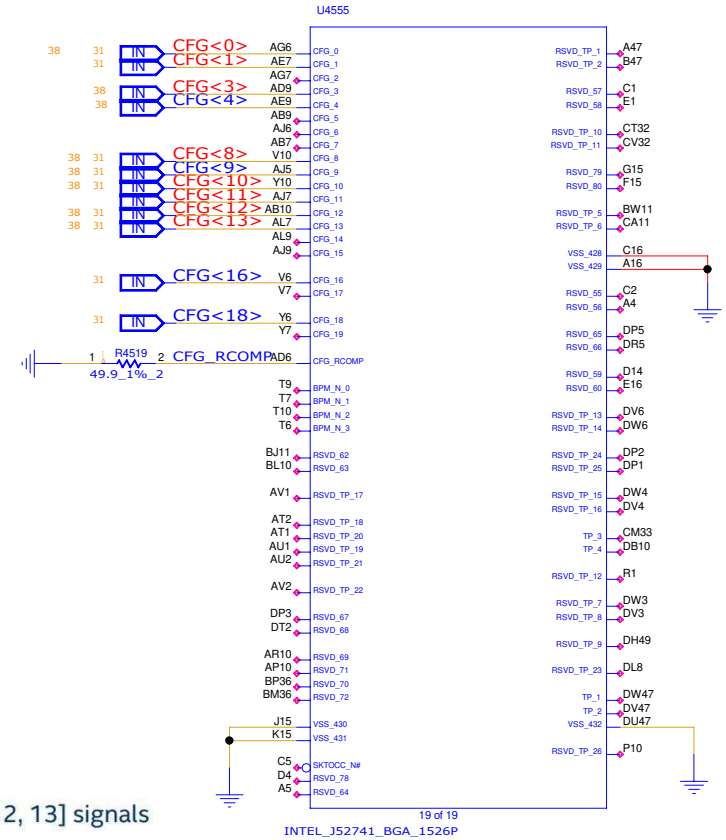


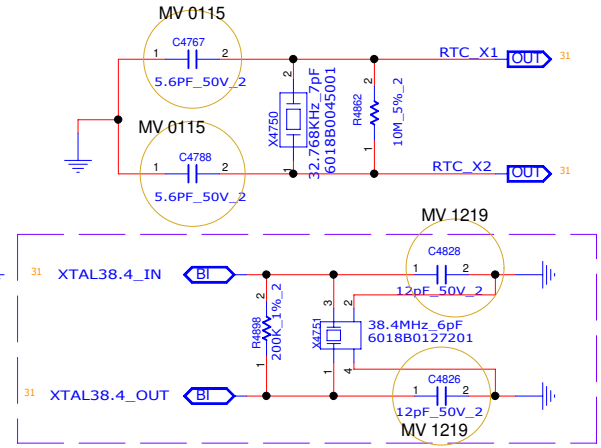
RTC





CFG<0>	CFG<1>	CFG<8>	CFG<9>	CFG<10>	CFG<12>	CFG<13>
R4563	R4564	R4570	R4579	R4580	R4586	R4591



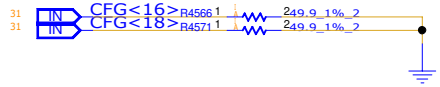


For ICL i3 QS CPU only

Platform Workaround:

- Pull-up CFG[0, 1, 8, 9, 10, 12, 13] signals to VCCIO_OUT
- Different configuration options:

  1. Add 1K Ohm pull-up resistors to each of the CFG[0, 1, 8, 9, 10, 12, 13] signals



INVENTEC

TITLE: MODEL_PROJECT_FUNCTION
MCP8-CLOCK & RESERVED

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CPU-9 DP

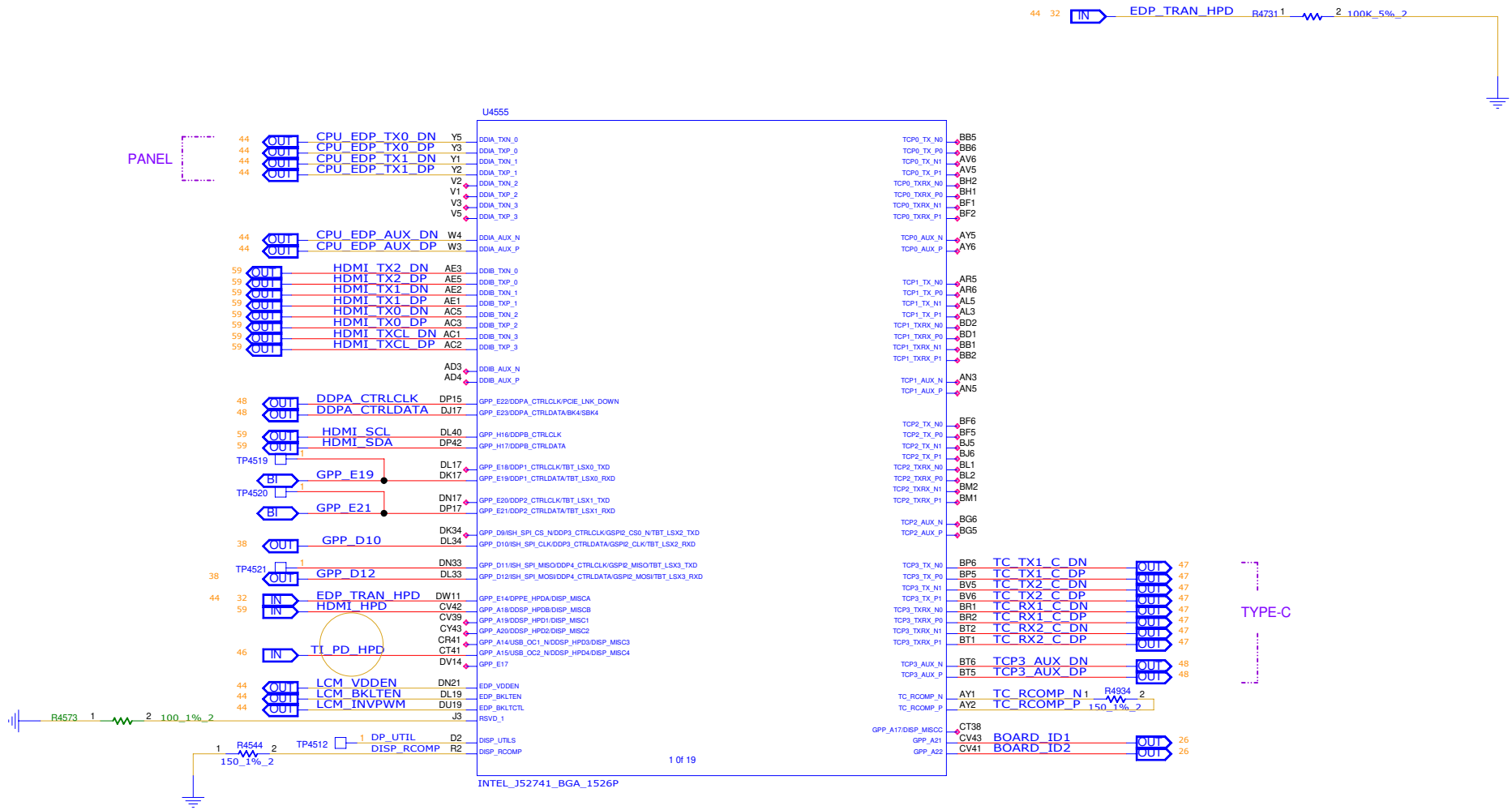

Table 1-6. HDMI* Checklist

Port	Function	DDI Signal Name	HDMI* Signal Name
DDI B	Main Link	DDIB_TXP[0]	DDIB_HDMI_DATA2_P
		DDIB_TXN[0]	DDIB_HDMI_DATA2_N
		DDIB_TXP[1]	DDIB_HDMI_DATA1_P
		DDIB_TXN[1]	DDIB_HDMI_DATA1_N
		DDIB_TXP[2]	DDIB_HDMI_DATA0_P
		DDIB_TXN[2]	DDIB_HDMI_DATA0_N
		DDIB_TXP[3]	DDIB_HDMI_CLK_P
		DDIB_TXN[3]	DDIB_HDMI_CLK_N
	DDC	DDPB_CTRLCLK	DDIx_HDMI_OB_SCL
		DDPB_CTRLDATA	DDIx_HDMI_OB_SDA
	HPD	DDSP_HPDB	HDMIB_HPD

Table 5-53. TCP Port Signal Mapping for HDMI*

Description	Signal Mapping	
	TCP	HDMI
Main Link (Tx)	TCP_TX0	HDMI Data_2
	TCP_TX1	HDMI Data_0
	TCP_TXRX0	HDMI Data_1
	TCP_TXRX1	HDMI CLK

Note: Apply to TCP ports only.

INVENTEC

TITLE: MCP4-GPIO & CDP FUNCTION

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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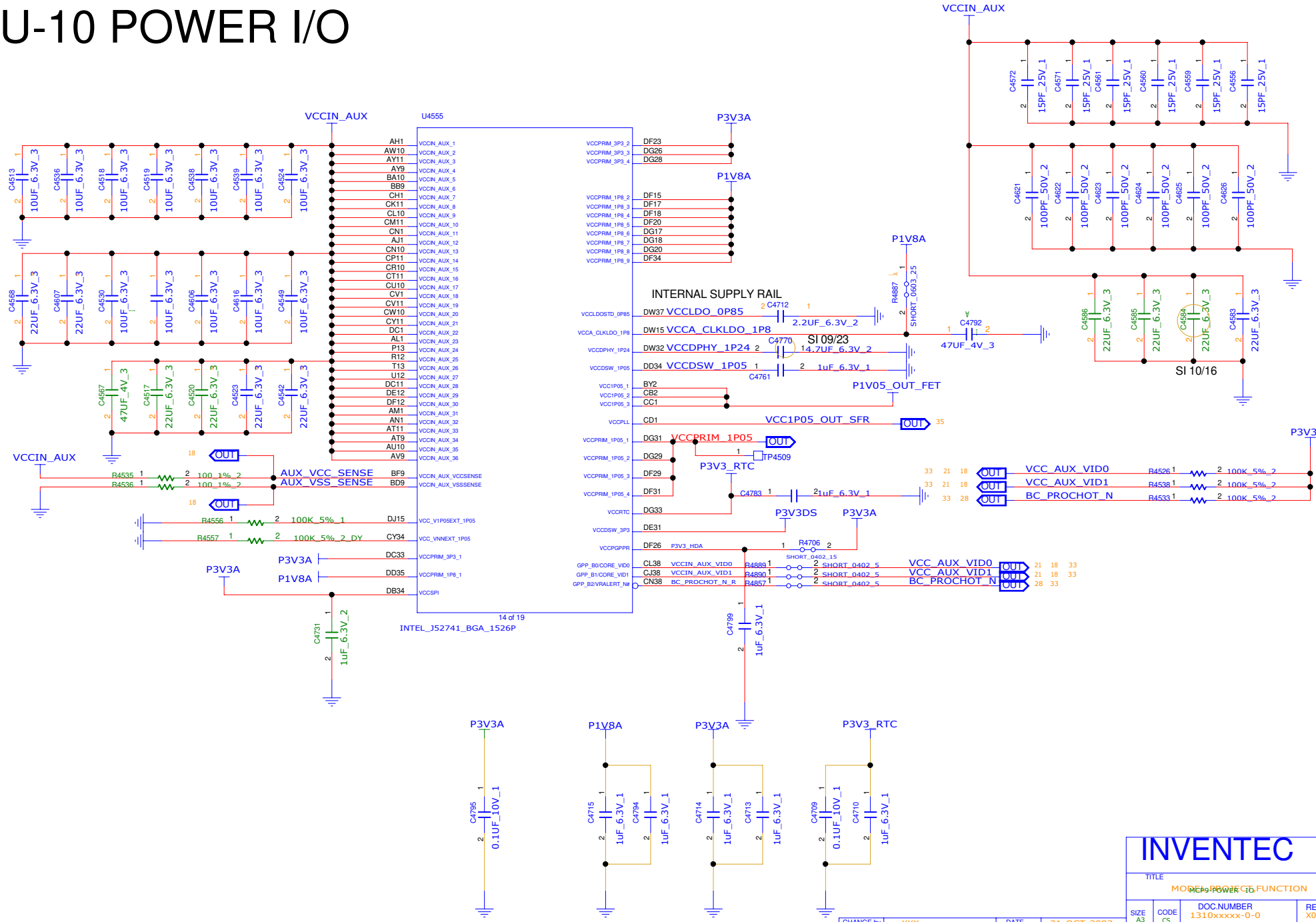
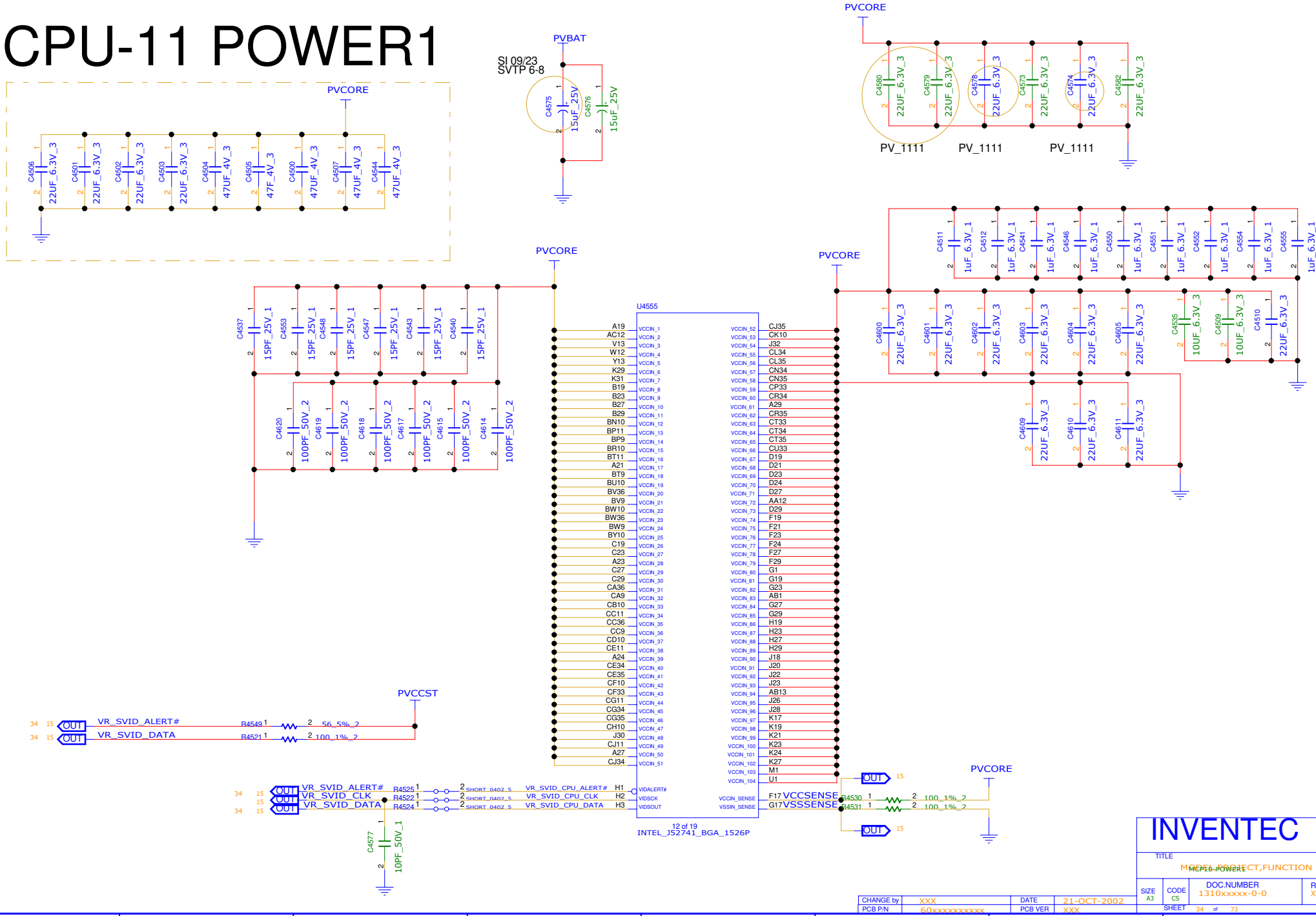
CPU-10 POWER I/O

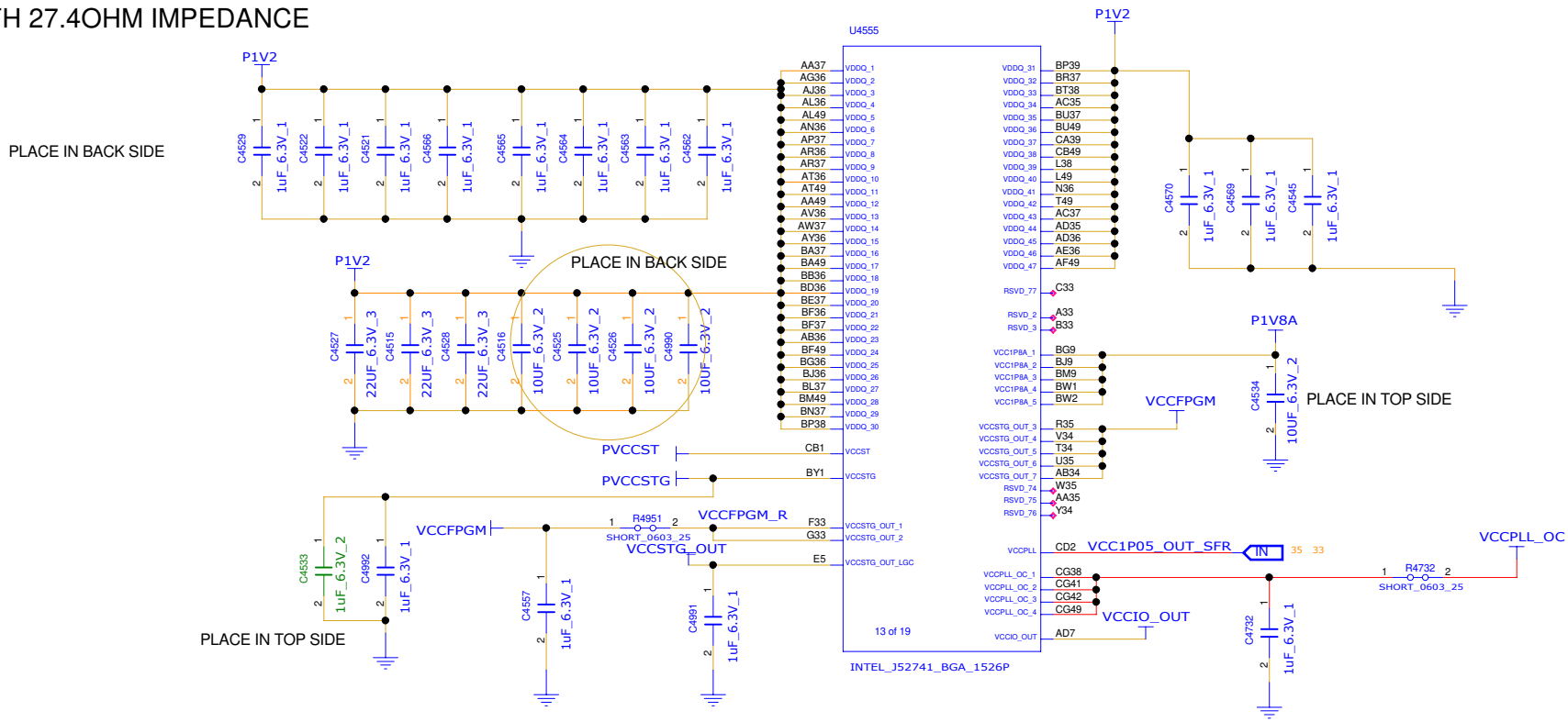


CPU-11 POWER1



CPU-12 POWER2

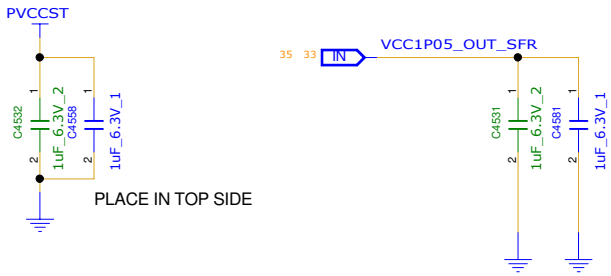
ROUTE VCCSENSE WITH 27.4OHM IMPEDANCE



PLEASE PLACE CAPS CLOSE TO CPU

Table 11-8. Differences between Power Maps

Volume	Premium
VccSTG gated by SLP_S3#	VccSTG gated by {CPU_C10_GATE#}
VccPLL_OC is supplied directly from VDDQ	VccPLL_OC is supplied from VDDQ through a load switch
VCC1P8A on the CPU is supplied directly by V1.8A	VCC1P8A is supplied from V1.8A and gated by *CPU_C10_GATE #*
VCC_VNNEXT_1P05 is not used	VCC_VNNEXT_1P05 is supplied by small dedicated VNN VR to bypass PCH FIVR during light load
VCC_V1P05EXT_1P05 is not used	VCC _V1P05EXT_1P05 is supplied by small dedicated V1.05A VR to bypass PCH FIVR during light load



INVENTEC

TITLE: MCP11 POWER2

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
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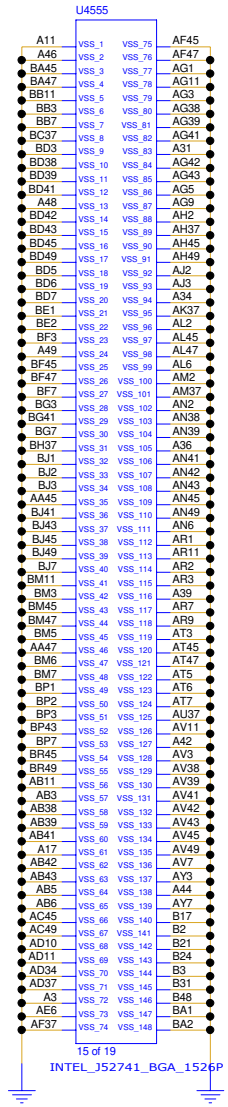
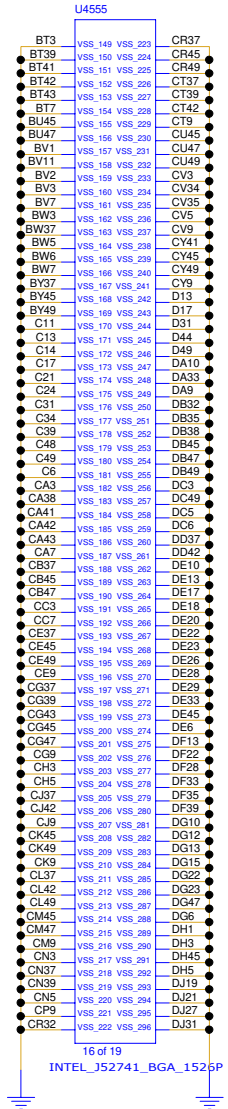
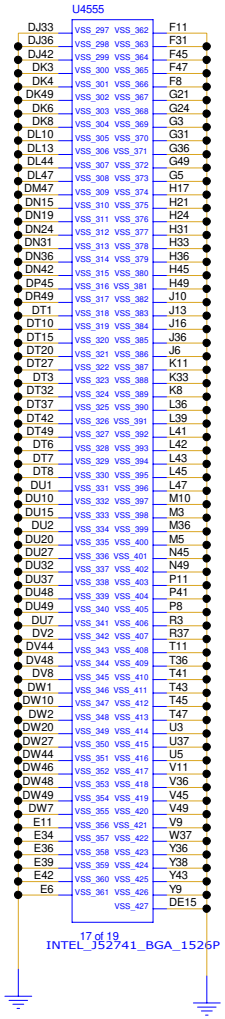
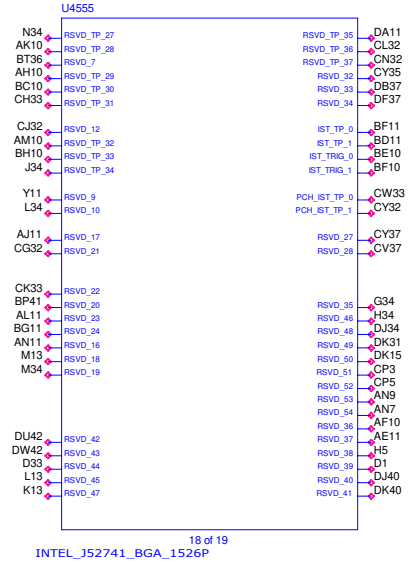
CPU-13 GND









REFERENCE:4500~4949

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
MCP12-GND

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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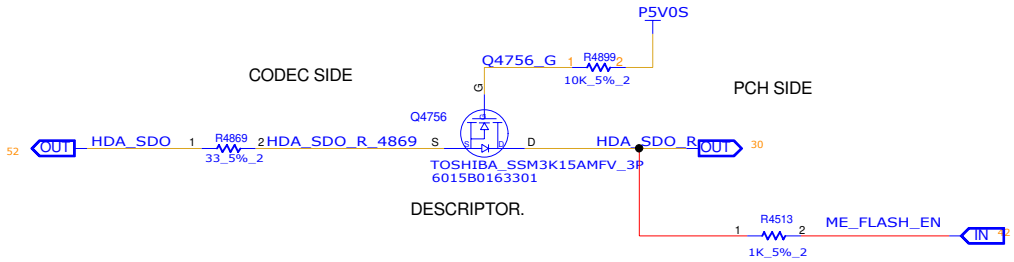
CPU-14 STRAP



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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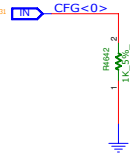
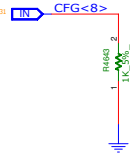
CPU-14 STRAP 1



EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED

1:(DEFAULT) NORMAL OPERATION; NO STALL

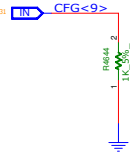
0:STALL



ALLOW THE USE OF NOA ON LOCKED UNITS

1: DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE
DISABLED IN LOCKED UNITS AND
ENABLED IN UN-LOCKED UNITS

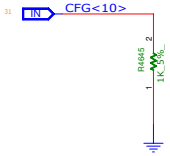
0: ENABLED; NOA WILL BE
AVAILABLE REGARDLESS OF THE
LOCKING OF THE UNIT



NO SVID PROTOCOL CAPABLE VR CONNECTED

1:VRS SUPPORTING SVID PROTOCOL ARE PRESENT

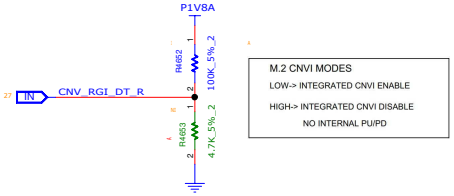
0:NO VR SUPPORTING SVID
IS PRESENT. THE CHIP WILL NOT
GENERATE (OR RESPOND TO) SVID ACTIVITY



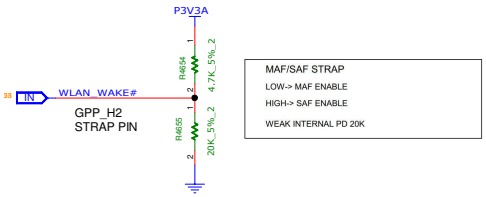
SAFE MODE BOOT

1: POWER FEATURES ACTIVATED DURING RESET

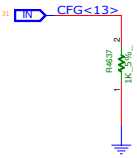
0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED



M.2 CNVI MODES
LOW-> INTEGRATED CNVI ENABLE
HIGH-> INTEGRATED CNVI DISABLE
NO INTERNAL PU/PD



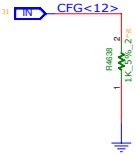
MAF/SAF STRAP
LOW-> MAF ENABLE
HIGH-> SAF ENABLE
WEAK INTERNAL PD 20K



PMSYNC AYNC MODE- PM SYNC

1' - (DEFAULT)SYNCHCRONOUS (1 24 MHZ CYCLE PER BIT)

0' - ASYNC - 4-24MHZ CYCLES PER BIT

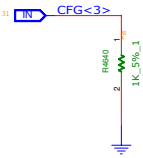


PM SYNC LEGACY

THIS STRAP IS NEW IN SKL. IT TELL THE CPU THAT IT IS CONNECTED
PCH SUPPORTING OLDER VERSION OF PMSYNC PROTOCOL
IN LEGACY MORE CPU DOESN'T WAIT FOR EPOC MESSAGE FROM THE PCH

1' - (DEFAULT) PMSYNC 2.0

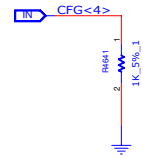
0' – LEGACY



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)

0 : ENABLED
SET DFX ENABLED BIT IN DEBUG INTERFACE MSR

1 : DISABLED

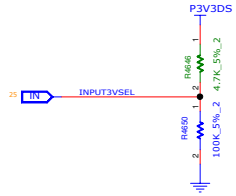


DISPLAY PORT PRESENCE STRAP

0: ENABLED

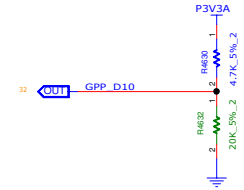
EMBEDDED DISPLAY PORT

1: DISABLED
NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

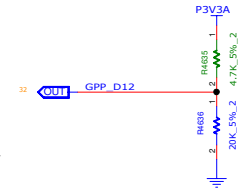


VCCDSW_3P3 power well

3V SELECT STRAP
LOW-> 3.3V +/-5%
HIGH->3.0V +/-5%



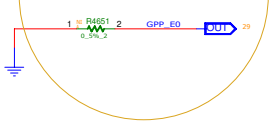
TBT LSX #2 PINS VCCIO CONFIGURATION
HIGH: 3.3V
LOW: 1.8V
NO INTERNAL PU/PD

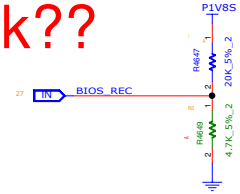


TBT LSX #3 PINS VCCIO CONFIGURATION
HIGH: 3.3V
LOW: 1.8V
NO INTERNAL PU/PD

Notes:
1. An external pull-up resistor is required if the pin is used as HDMI Display I^2C, instead of TBT_LSX.
2. This signal is in the primary well.

To be check??





STRAP/GPIO NAME	DEFAULT CONFIG REQUIRED	CONFIG CHANGE IF REQ
SATA_HOT_PLUG	OPEN(NO HOT PLUG)	CLOSED(HOT PLUG)
BIOS RECOVERY	OPEN(NO BIOS REC)	CLOSED (BIOS REC)

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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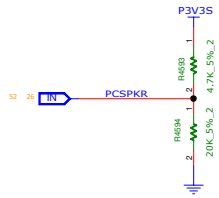
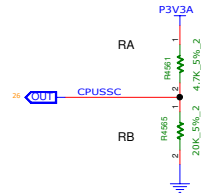
CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	50xxxxxxxxx	PCB VER	XXX

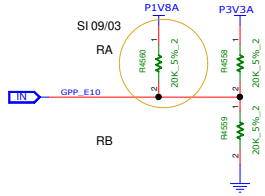
CPU-14 STRAP 2



TOP SWAP OVERRIDE
HIGH- TOP SWAP ENABLED
LOW-DISABLED
WEAK INTERNAL PD 20K



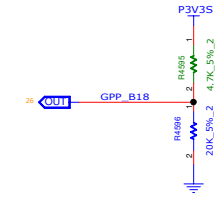
CPUNSSC CLOCK FREQ
HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)
LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)
WEAK INTERNAL PD 20K



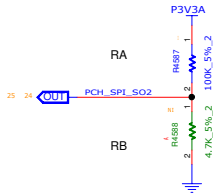
XTAL INPUT FREQUENCY [0] HVM ONLY

00 – DIVIDER BYPASS
01 – DIVIDE BY 2 (HVM: 38.4MHZ INPUT)
10 – DIVIDE BY 10 (HVM: 250MHZ INPUT)
11 – DIVIDE BY 4 (BI: 100MHZ INPUT)

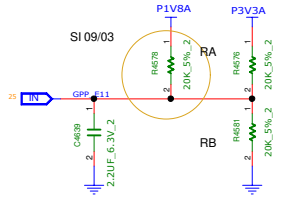
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD



NO REBOOT
HIGH - NO REBOOT
LOW- REBOOT ENABLED
WEAK INTERNAL PD 20K



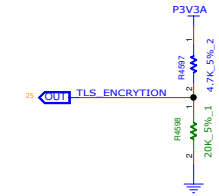
CONSENT STRAP
HIGH: DISABLED
LOW: ENABLED
NO INTERNAL PU/PD



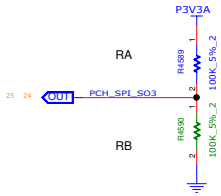
XTAL INPUT FREQUENCY [1] HVM ONLY

00 – DIVIDER BYPASS
01 – DIVIDE BY 2 (HVM: 38.4MHZ INPUT)
10 – DIVIDE BY 10 (HVM: 250MHZ INPUT)
11 – DIVIDE BY 4 (BI: 100MHZ INPUT)

(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

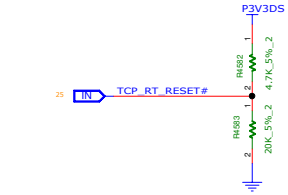


TLS CONFIDENTIALITY
LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE
WEAK INTERNAL PD 20K

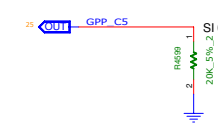


A0 PERSONALITY STRAP
HIGH: DISABLED
LOW: ENABLED
NO INTERNAL PU/PD

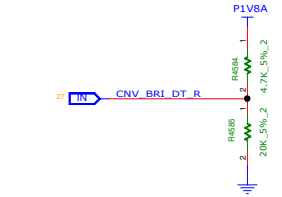
SPI9_SO3	Reserved	Rising edge of SUS0STAT#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.0V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



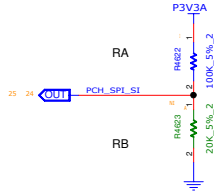
XTAL INPUT MODE
LOW: XTAL IS ATTACHED
HIGH: XTAL INPUT IS SINGLE ENDED
WEAK INTERNAL PD 20K



ESPI OR EC LESS
HIGH: ESPI IS DISABLED
LOW: ESPI SELECTED
WEAK INTERNAL PD 20K

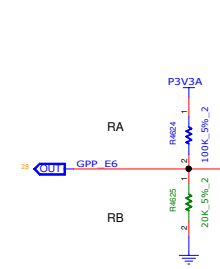


XTAL SEL
LOW: 38.4/19.2MHZ (DEFAULT)
HIGH = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)
WEAK INTERNAL PD 20K

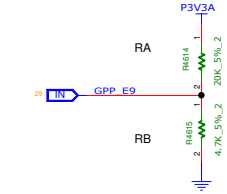


BOOT HALT
HIGH - DISABLED
LOW- ENABLED
NO INTERNAL PU/PD

DFXTESTMODE
PGDMON
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED
WEAK INTERNAL PU 20K



JTAG ODT DISABLE
LOW: JTAG ODT DISABLED
HIGH: JTAG ODT ENABLED
NO INTERNAL PU/PD



RING OSCILLATOR BYPASS
LOW: RING OSCILLATOR
HIGH :BYPASS MODE ENABLED
(QUALIFIED BY DFXTESTMODE)
NO INTERNAL PU/PD

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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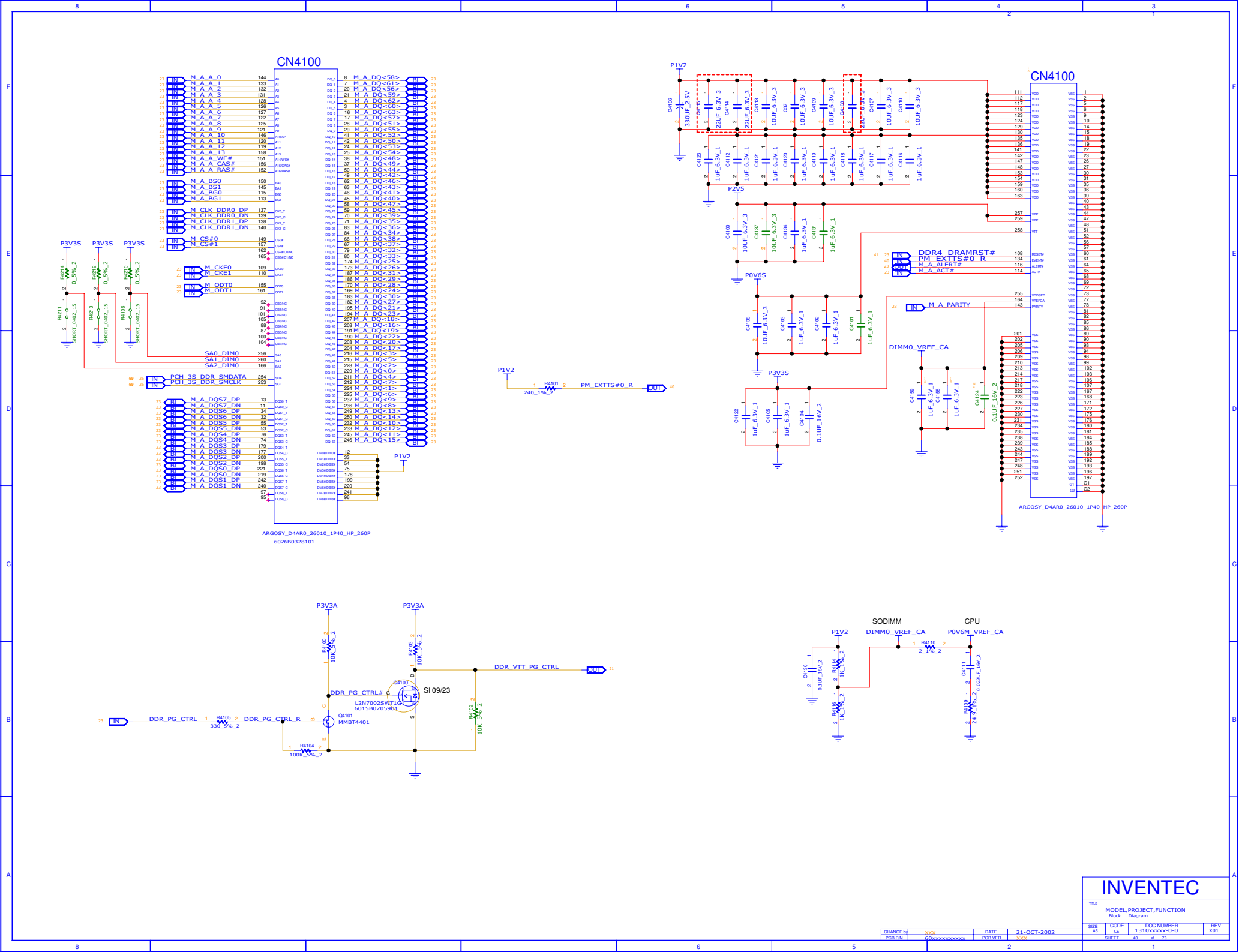
CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX


CN4100
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M_A_A_1
M_A_A_2
M_A_A_3
M_A_A_4
M_A_A_5
M_A_A_6
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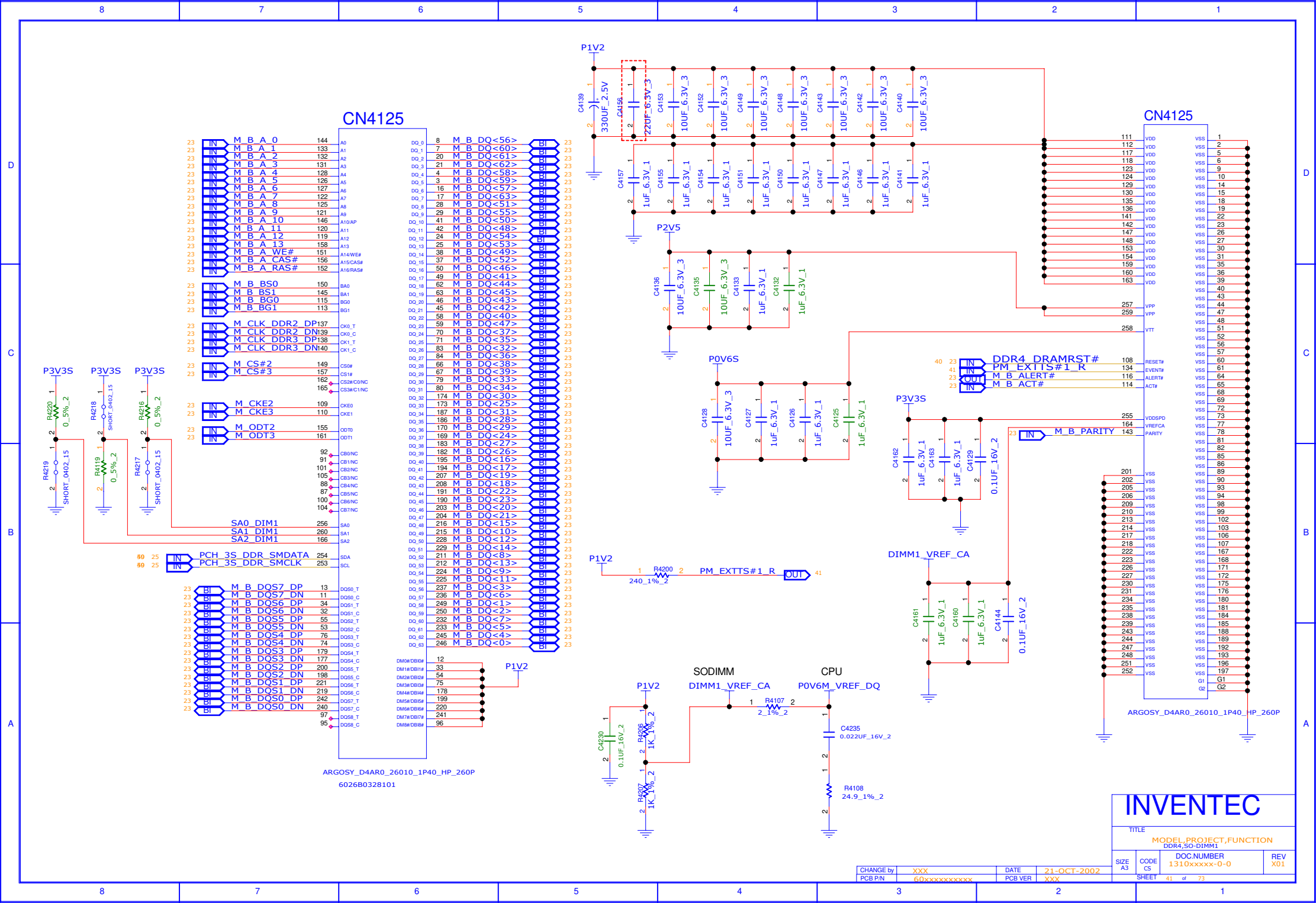
M_A_A_8
M_A_A_9
M_A_A_10
M_A_A_11
M_A_A_12
M_A_A_13
M_A_WE#
M_A_CAS#
M_A_RAS#
M_A_BS0
M_A_BS1
M_A_BG0
M_A_BG1
M_CLK_DDR0_DP
M_CLK_DDR0_DN
M_CLK_DDR1_DP
M_CLK_DDR1_DN
M_CS#0
M_CS#1
M_CKE0
M_CKE1
M_ODT0
M_ODT1
SA0_DIM0
SA1_DIM0
SA2_DIM0
PCH_3S_DDR_SMDATA
PCH_3S_DDR_SMCLK
M_A_DQS7_DP
M_A_DQS7_DN
M_A_DQS6_DP
M_A_DQS6_DN
M_A_DQS5_DP
M_A_DQS5_DN
M_A_DQS4_DP
M_A_DQS4_DN
M_A_DQS3_DP
M_A_DQS3_DN
M_A_DQS2_DP
M_A_DQS2_DN
M_A_DQS1_DP
M_A_DQS1_DN
M_A_DQS0_DP
M_A_DQS0_DN
M_A_DQ<63:0>
P3V3S
R4214 0_5%_2
R4212 0_5%_2
R4210 0_5%_2
R4211 SHORT_0402_15
R4213 SHORT_0402_15
R4106 SHORT_0402_15
ARGOSY_D4AR0_26010_1P40_HP_260P
6026B0328101
P1V2
R4101 240_1%_2
PM_EXTTS#0_R
P2V5
P0V6S
P3V3S
DDR4_DRAMRST#
PM_EXTTS#0_R
M_A_ALERT#
M_A_ACT#
M_A_PARITY
DIMM0_VREF_CA
ARGOSY_D4AR0_26010_1P40_HP_260P
P3V3A
R4100 10K_5%_2
R4103 10K_5%_2
Q4100
L2N7002SWT1G
6015B0205901
SI 09/23
DDR_VTT_PG_CTRL
DDR_PG_CTRL#
DDR_PG_CTRL
R4105 330_5%_2
DDR_PG_CTRL_R
Q4101
MMBT4401
R4104 100K_5%_2
R4102 10K_5%_2
SODIMM
DIMM0_VREF_CA
CPU
P0V6M_VREF_CA
R4110 2_1%_2
R4108 1K_1%_2
R4109 24.9_1%_2
C4111 0.022UF_16V_2
C4130 0.1UF_16V_2
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
CHANGE NO XXX
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxx
PCB VER XXX
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 40 of 73



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
DDR4,SO-DIMM1

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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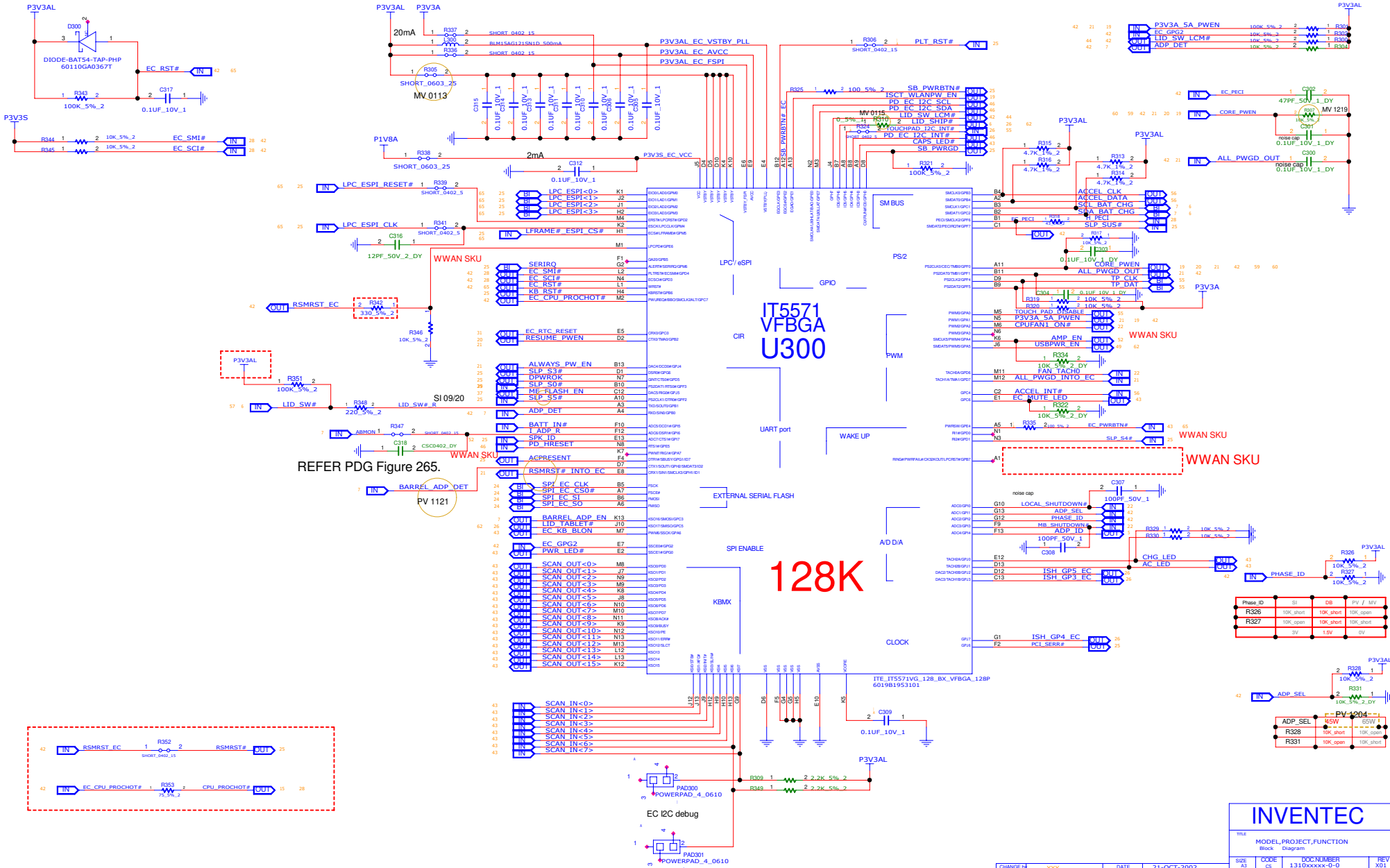
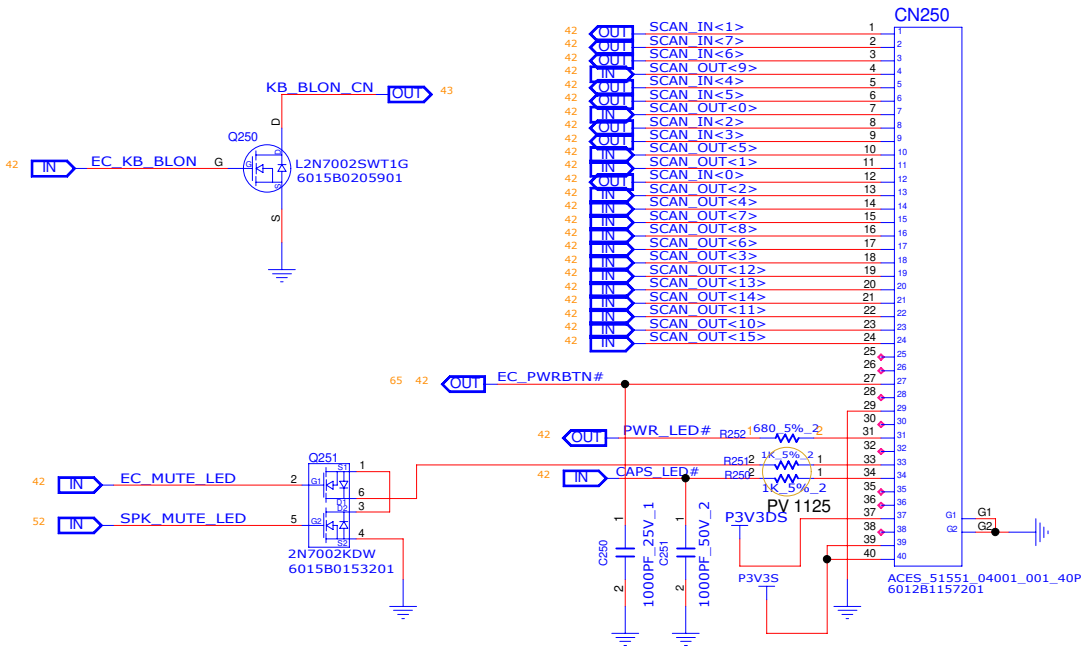
EC

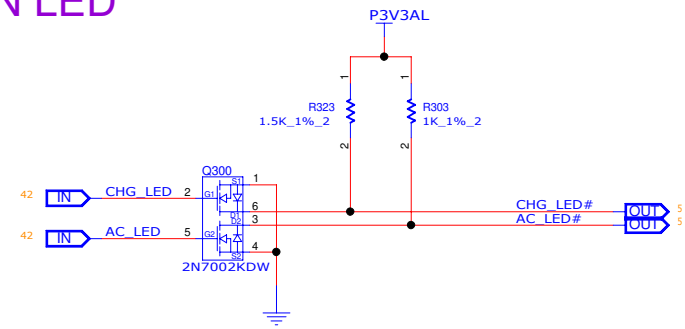

IT5571
VFBGA
U300
128K
ITE_IT5571VG_128_BX_VFBGA_128P
6019B1953101
SM BUS
PS/2
LPC / eSPI
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK
WWAN SKU
REFER PDG Figure 265.
SI 09/20
PV 1121
MV 0113
MV 1219
PV 1204
EC I2C debug
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram

KEYBOARD CONNECTOR

KEYBOARD CONN(40 PIN)

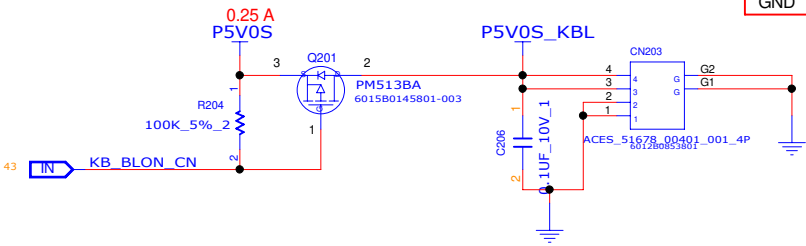


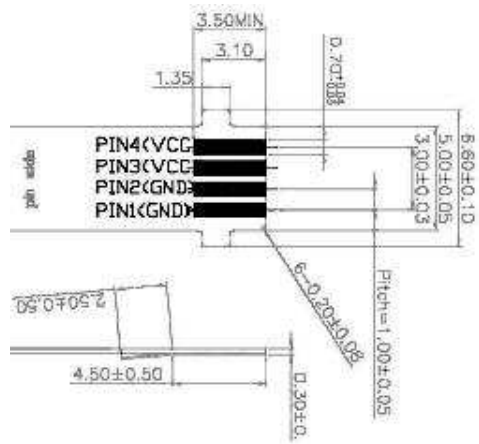
AC-IN LED



CONNECTOR KEY BOARD 200~299

KEYBOARD BACKLIGHT





INVENTEC

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

TITLE: MODEL,PROJECT,FUNCTION
KB CONN & LED

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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LCM :

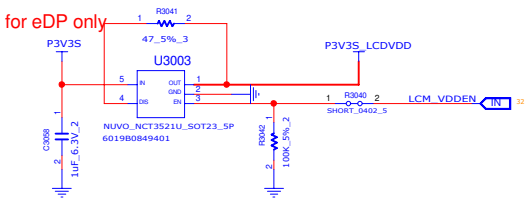
LOCATION 3000 ~ 3049

VER.14_20171119

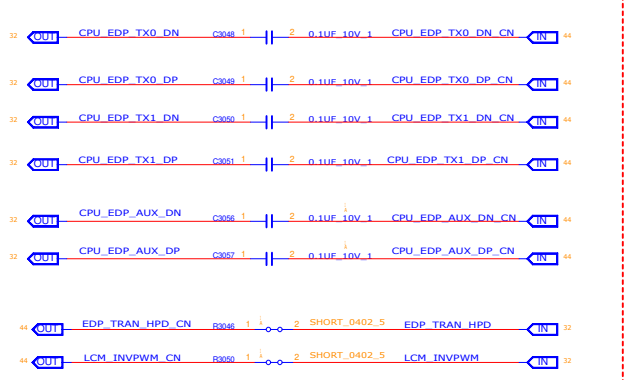
EDP + TOUCH SCREEN + G-SENSOR

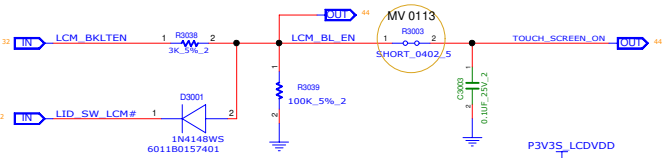
eDP

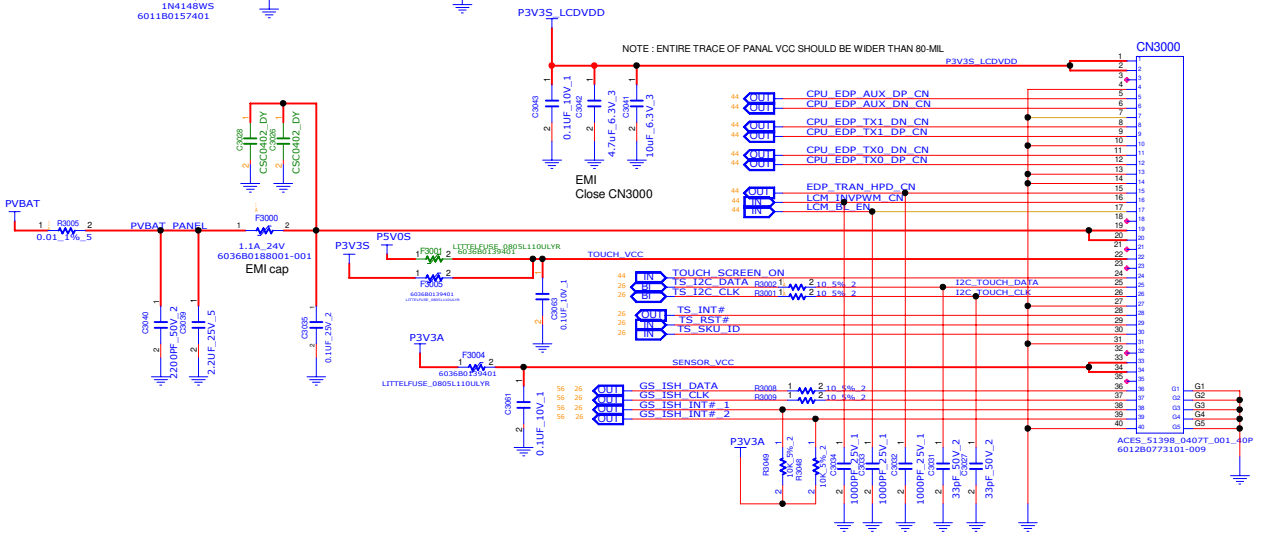
for eDP only

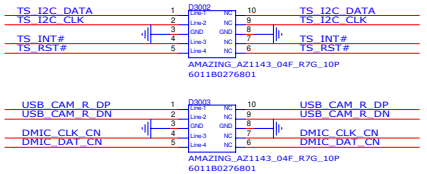


eDP

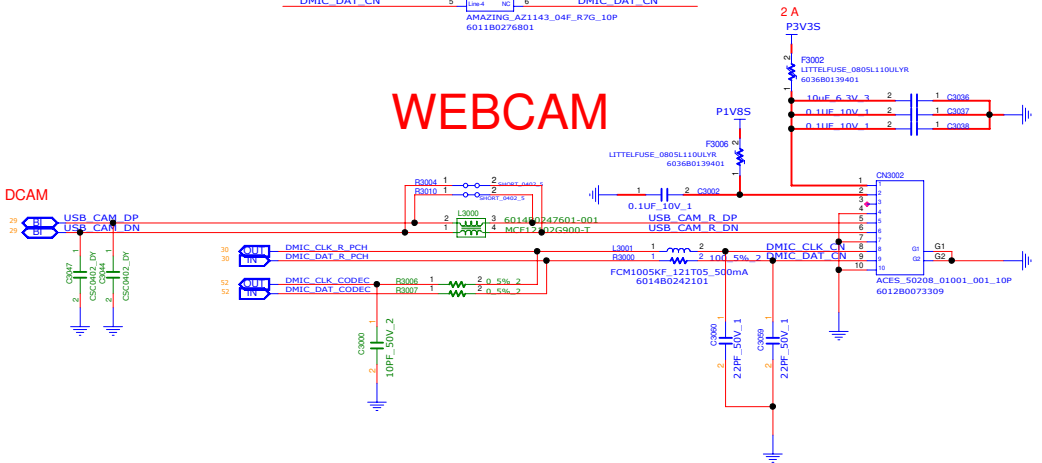








WEBCAM



INVENTEC

MODEL,PROJECT,FUNCTION

LVDS

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

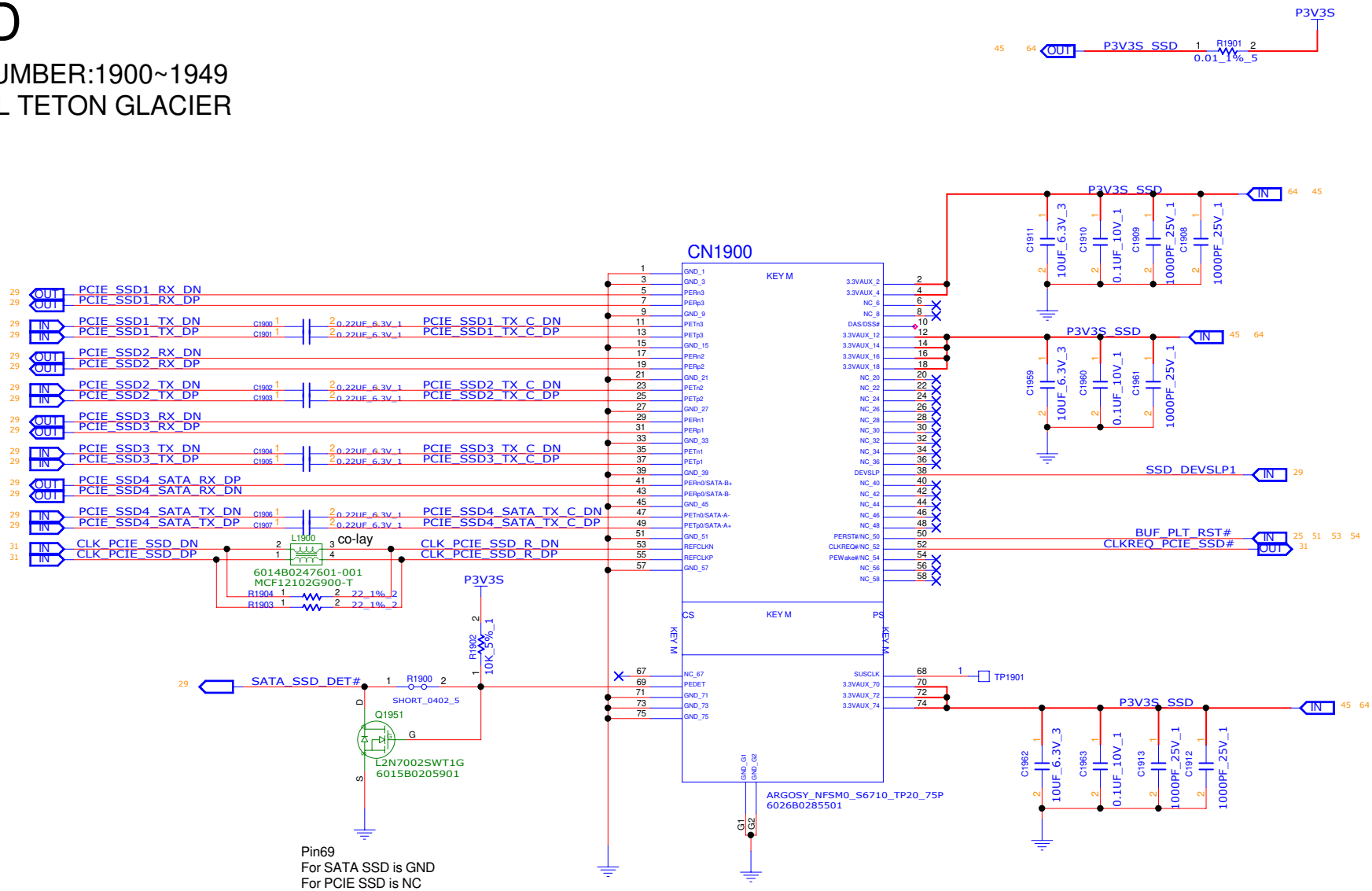
SHEET # 44 73

CHANGE by XXX DATE

PCB P/N 60xxxxxxxxxx PCB VER2.1 CHECK by 002

M.2 SSD

REFERENCE NUMBER:1900~1949
SUPPORT INTEL TETON GLACIER



CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
NGFF- SSD

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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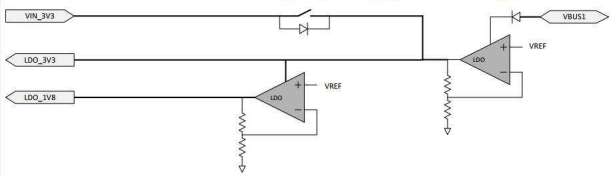
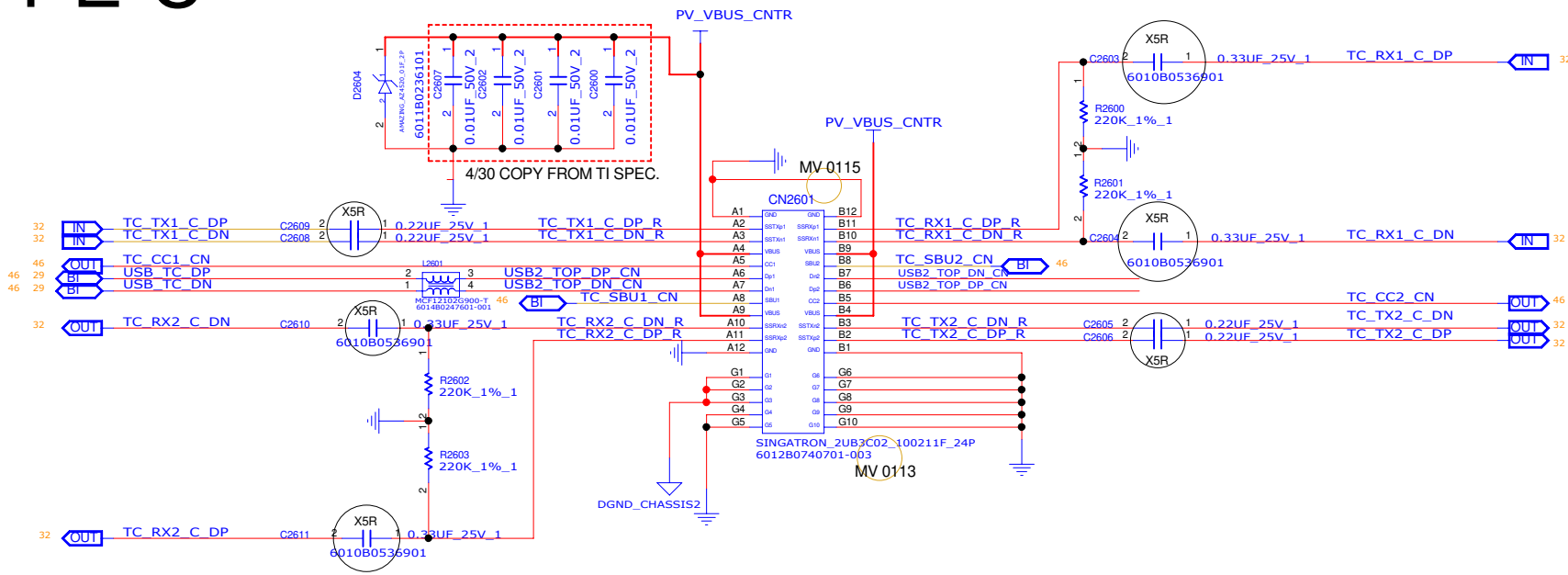
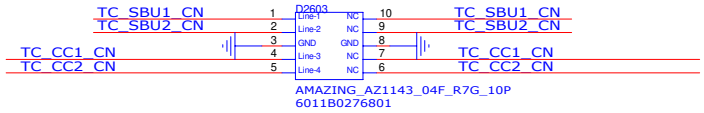
PD CONTROLLER

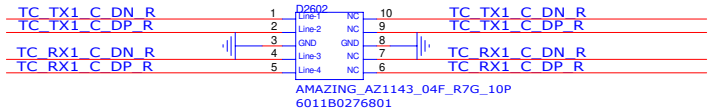


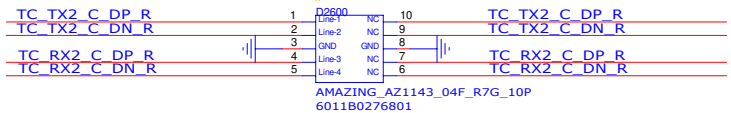
The TPS65987D power management block receives power and generates voltages to provide power to the TPS65987D internal circuitry. These generated power rails are LDO_3V3 and LDO_1V8. LDO_3V3 may also be used as a low power output for external flash memory. The power supply path is shown in Figure 12.

TYPE-C

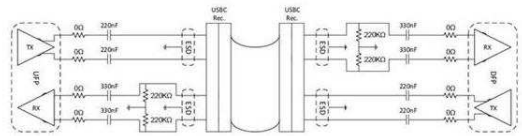








New TBT3 CIO Lines Topology



- ✓ 0Ω resistor might change up to 3Ω to better limit the surge current in an event of VBUS-short to SSTX/RX.
- ✓ RX capacitor (330nF ± 10%) was added for better VBUS-short protection on SSRX lines.
- ✓ Discharge resistor (220KΩ) was added to bias SSRX lines due to the new 330nF RX capacitor.
- ✓ TX capacitor (220nF ± 20%) didn't change.
- ✓ ESD (TVS diodes) didn't change.

THUNDERBOLT.

INVENTEC

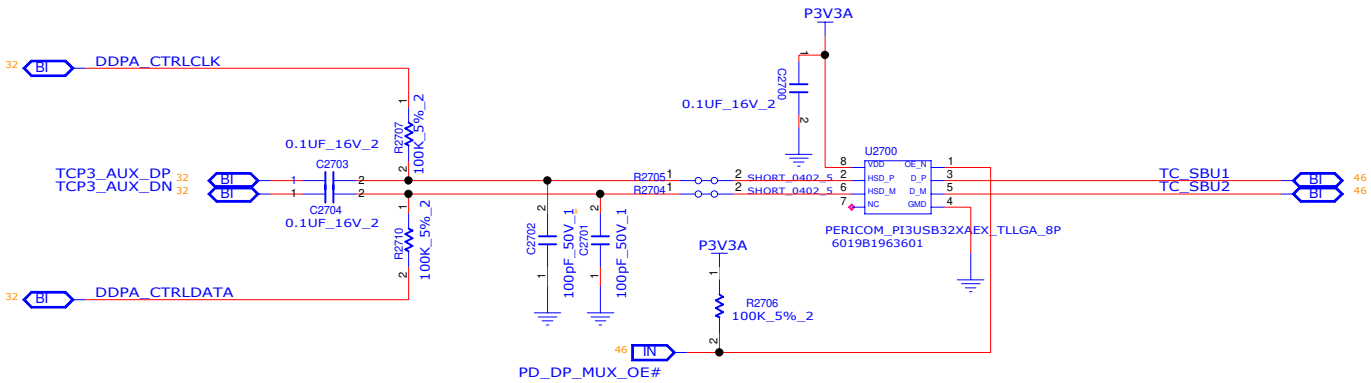
TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 47 of 73			

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

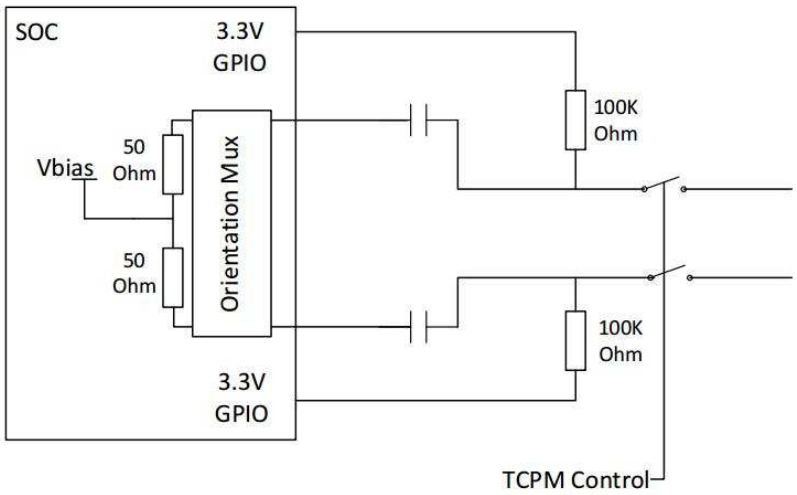
ICL DP ALTERNATE MODE W/O RE-TIMER

TYPE C CONNECTOR

SOC



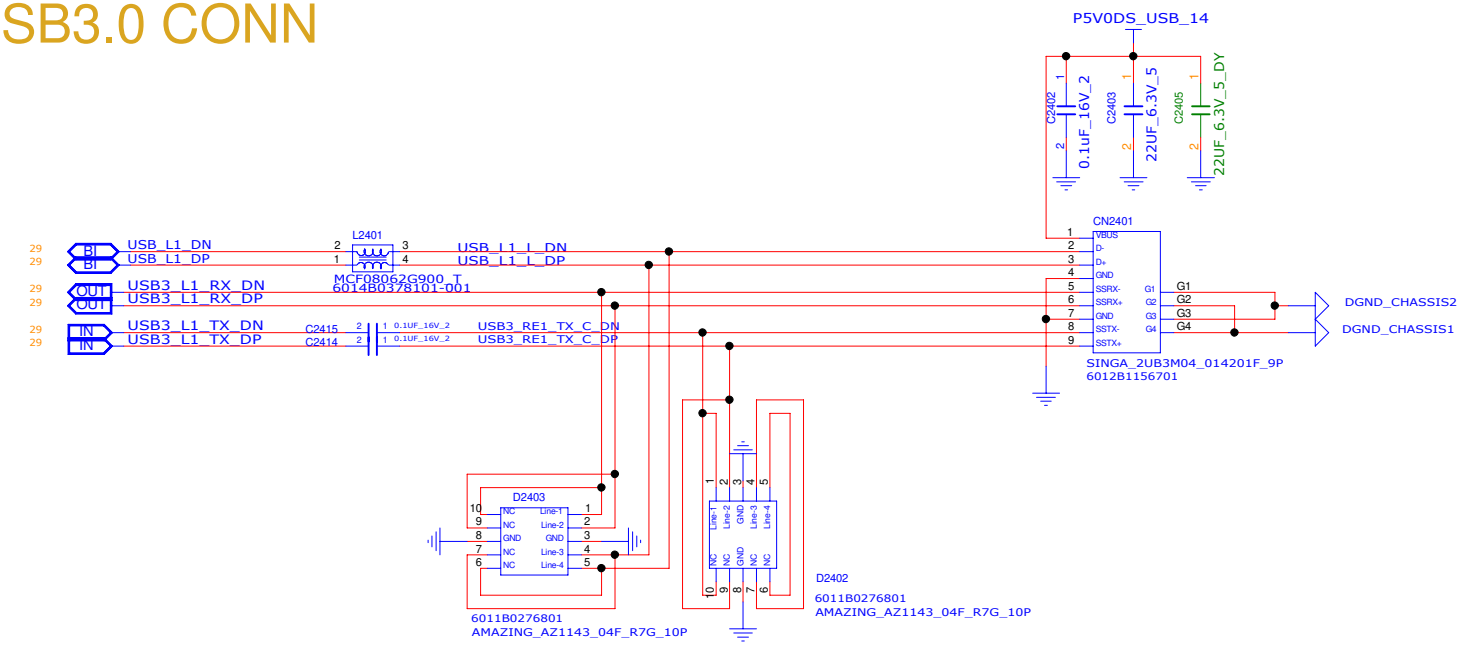
PD



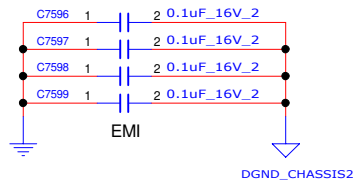
INVENTEC

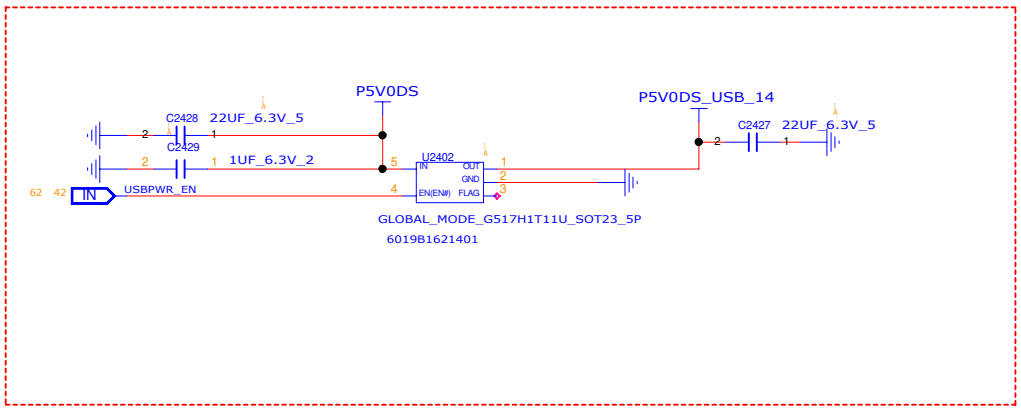
TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by XXX	DATE 21-OCT-2002	SHEET 48 of 73	
PCB P/N 60xxxxxxxxx	PCB VER XXX		

USB3.0 CONN



TOP X2, Bottom x2





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
USB 3.0 CONN & M/B TO D/B CONN

CHANGE by	XXX	DATE	
PCB P/N	60NBxxxxxxxx	PCB VER	XX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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OCT-2002

USB3.0 CHARGER

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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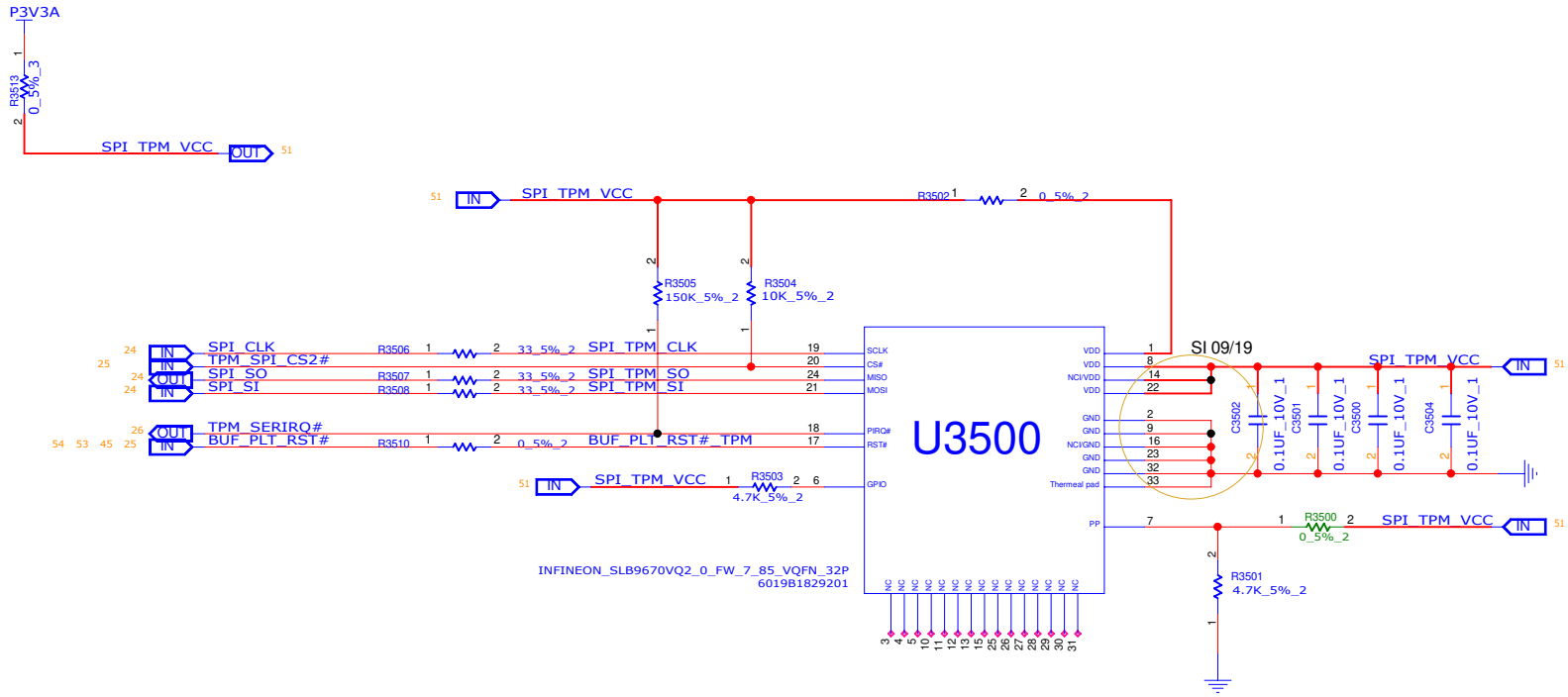
TPM2.0



CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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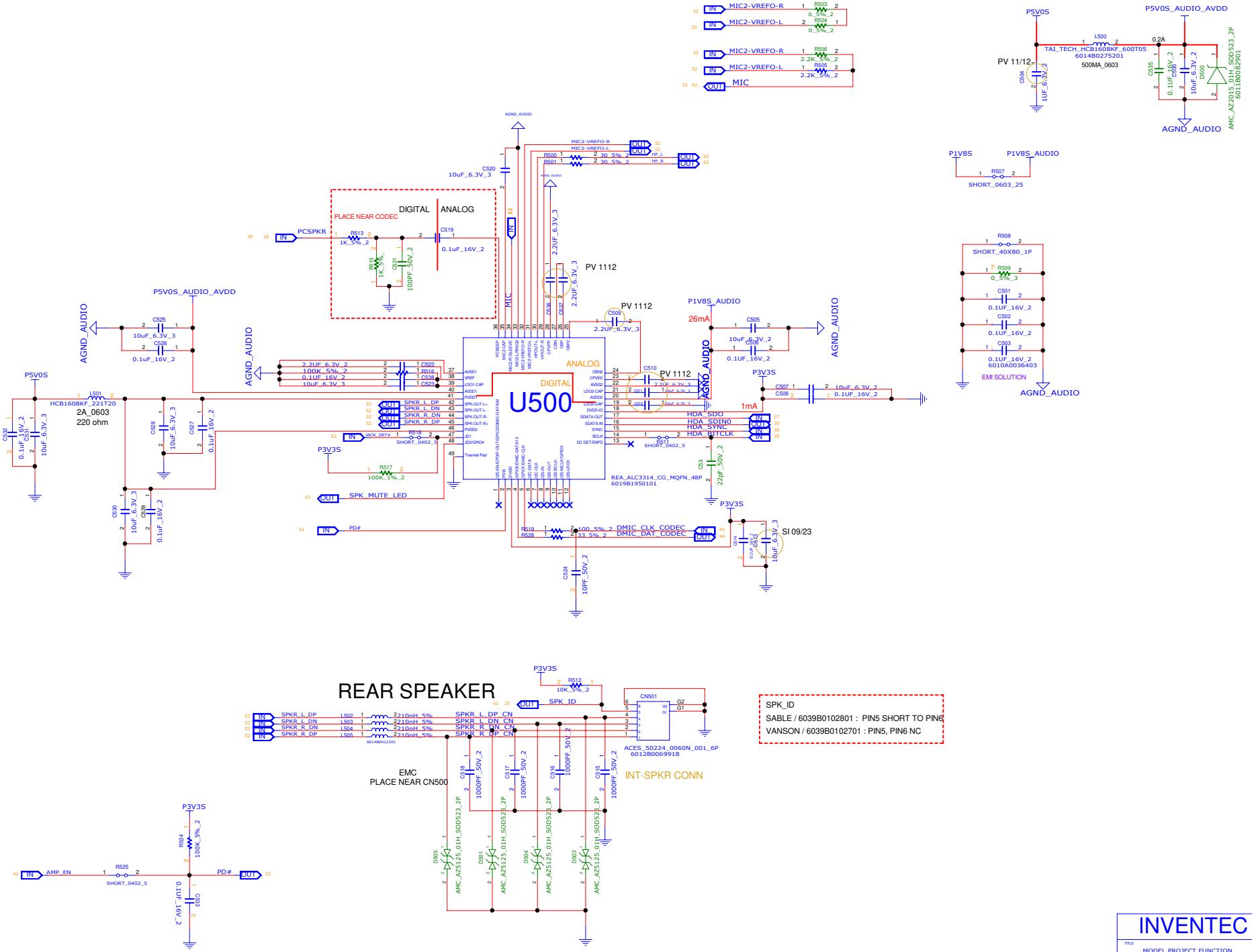
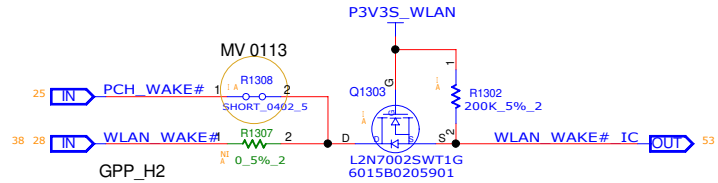
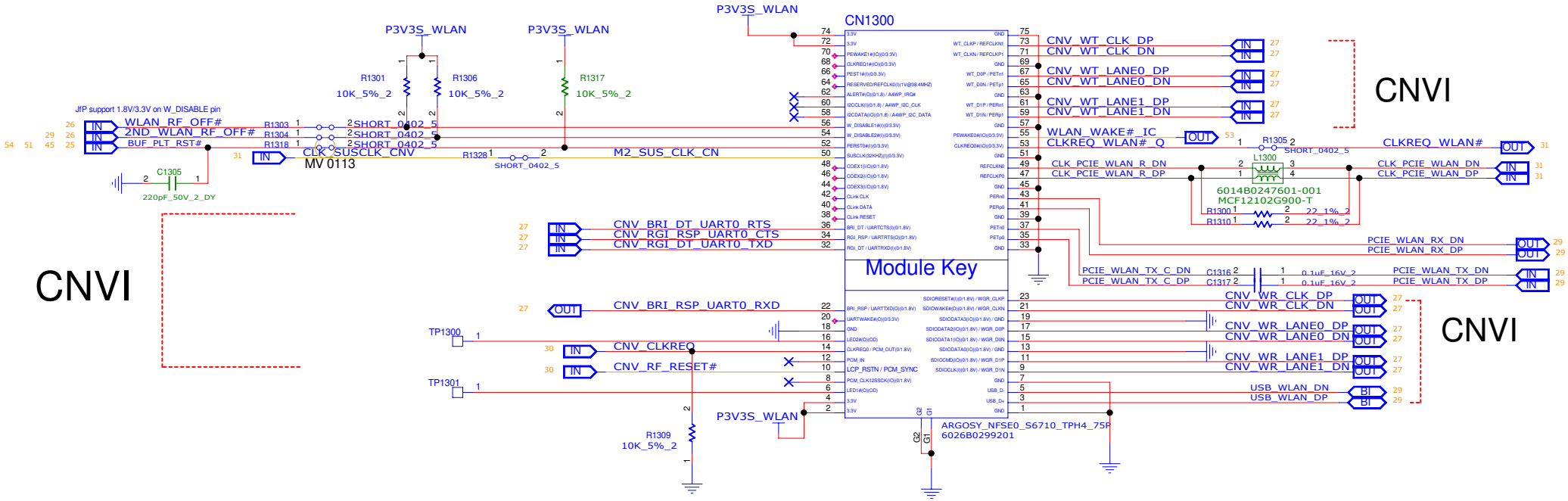
Audio Codec


MIC2-VREFO-R
MIC2-VREFO-L
MIC
P5V0S
P5V0S_AUDIO_AVDD
P1V8S
P1V8S_AUDIO
AGND_AUDIO
U500
REA_ALC3314_CG_MQFN_48P
6019B1950101
ANALOG
DIGITAL
PLACE NEAR CODEC
PCSPKR
SPK_L_DP
SPK_L_DN
SPK_R_DN
SPK_R_DP
JACK_DET#
SPK_MUTE_LED
PD#
DMIC_CLK_CODEC
DMIC_DAT_CODEC
HDA_SDO
HDA_SDTN0
HDA_SYNC
HDA_BITCLK
P3V3S
HCB1608KF_221T20
2A_0603
220 ohm
TAI_TECH_HCB1608KF_600T05
6014B0275201
500MA_0603
AMC_AZ2015_01H_SOD523_2P
6011B0083901
SHORT_0603_25
SHORT_40X80_1P
EMI SOLUTION
6010A0036403
PV 1112
PV 11/12
26mA
1mA
SI 09/23
REAR SPEAKER
SPK_ID
SABLE / 6039B0102801 : PIN5 SHORT TO PIN6
VANSON / 6039B0102701 : PIN5, PIN6 NC
CN501
ACES_50224_0060N_001_6P
6012B0069918
INT-SPKR CONN
EMC
PLACE NEAR CN500
AMP_EN

CNVI-WLAN

HYBRIDE-M.2E KEY





CHANGE by	XXX	DATE	
PCB P/N	60NSxxxxxxx	PCB VER	XX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
WLAN & BT

SIZE	CODE	DOC.NUMBER	REV
3	CS	1310xxxxx-0-0	X01

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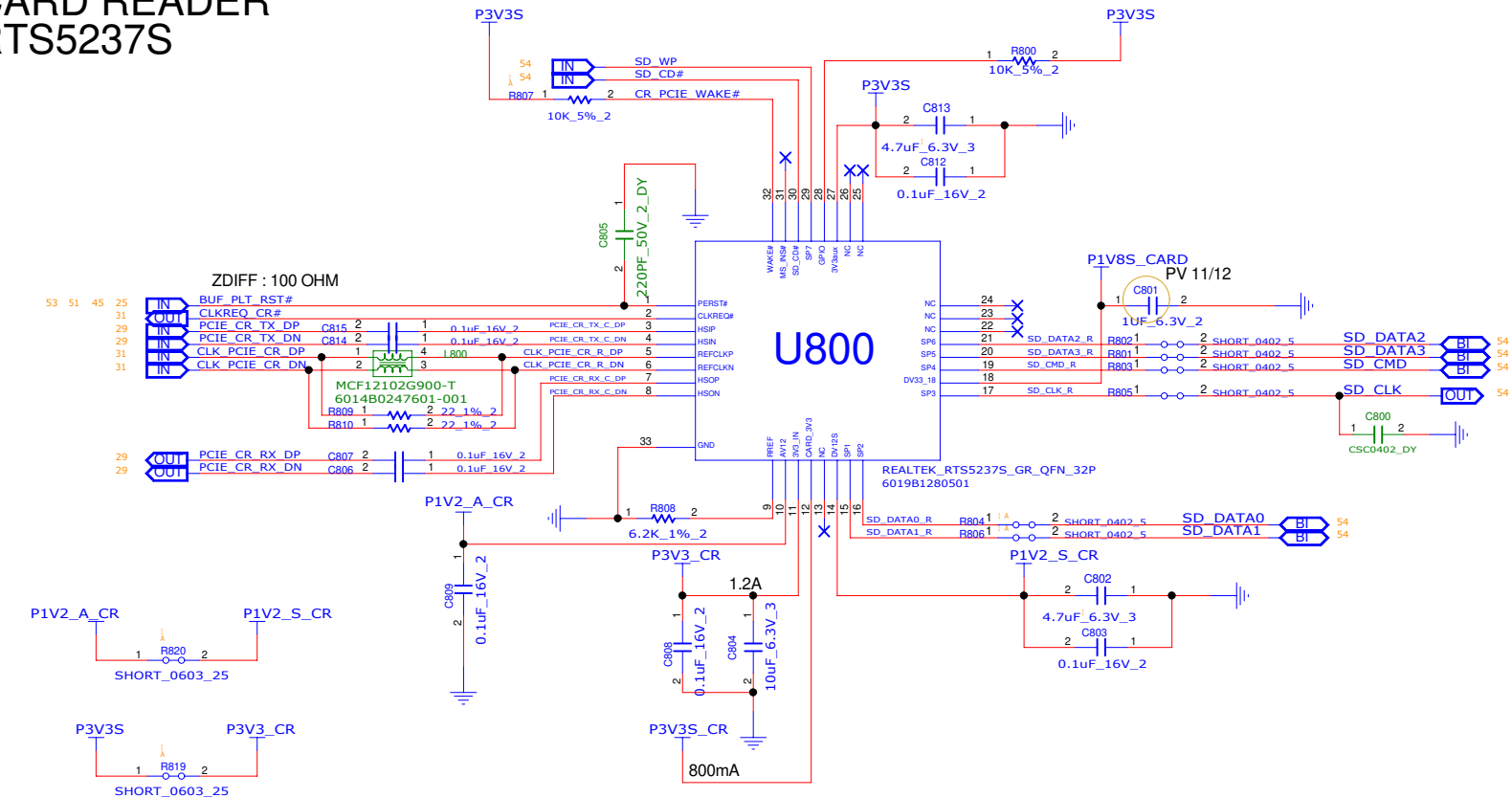
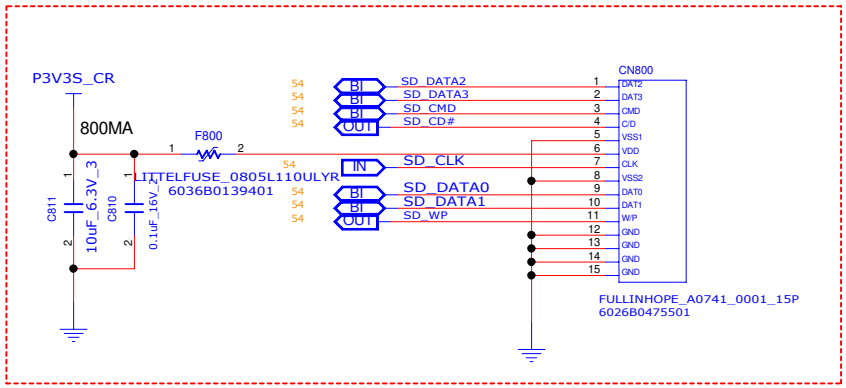
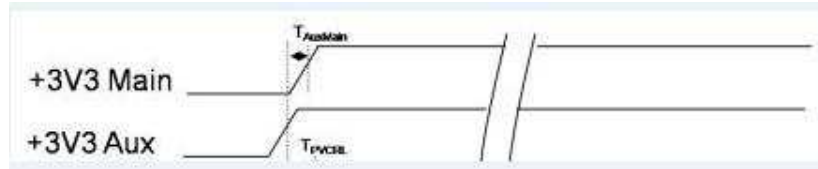
CARD READER
RTS5237S







Symbol	Description	Min.	Max.	Unit
TAUXMAIN	Power-on timing between AUX_PWR to MAIN_PWR	0	100	us

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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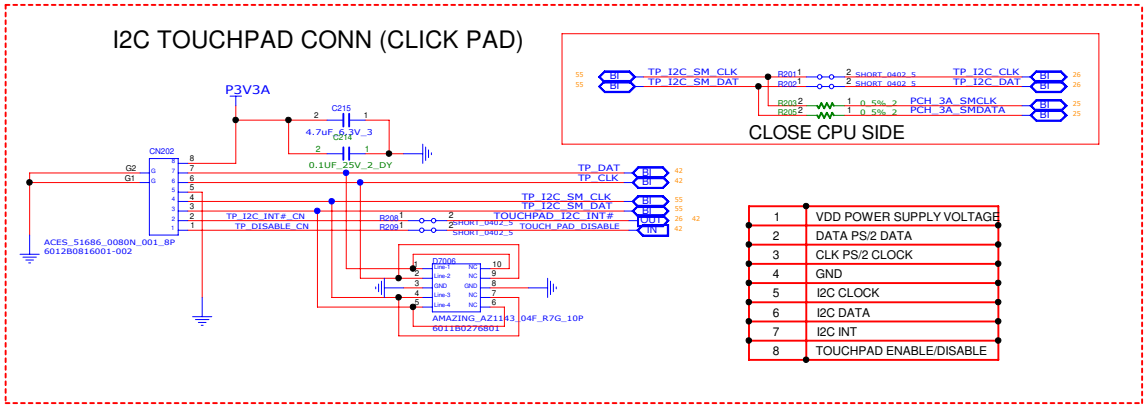
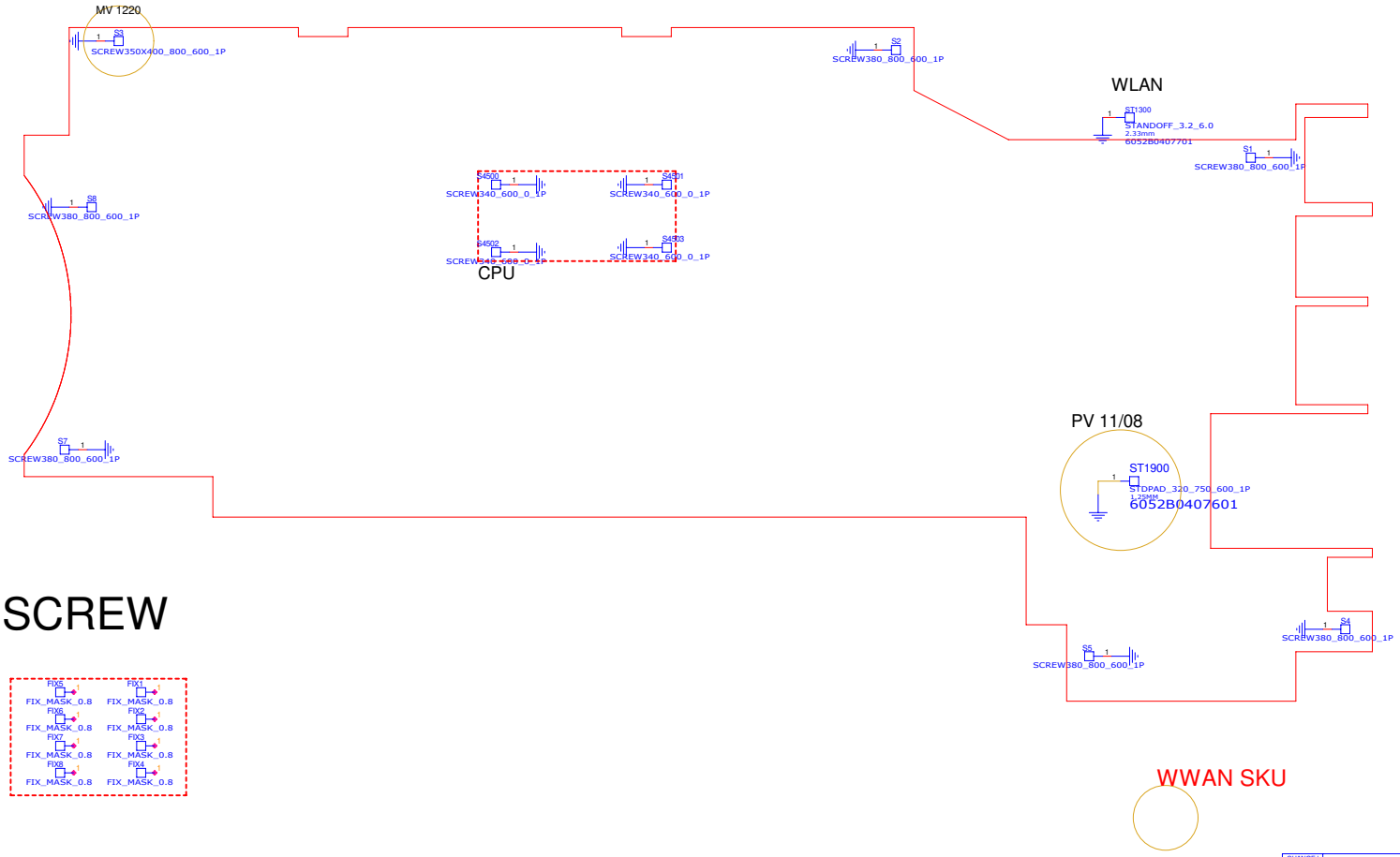
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

TOUCH PAD



1	VDD POWER SUPPLY VOLTAGE
2	DATA PS/2 DATA
3	CLK PS/2 CLOCK
4	GND
5	I2C CLOCK
6	I2C DATA
7	I2C INT
8	TOUCHPAD ENABLE/DISABLE



SCREW

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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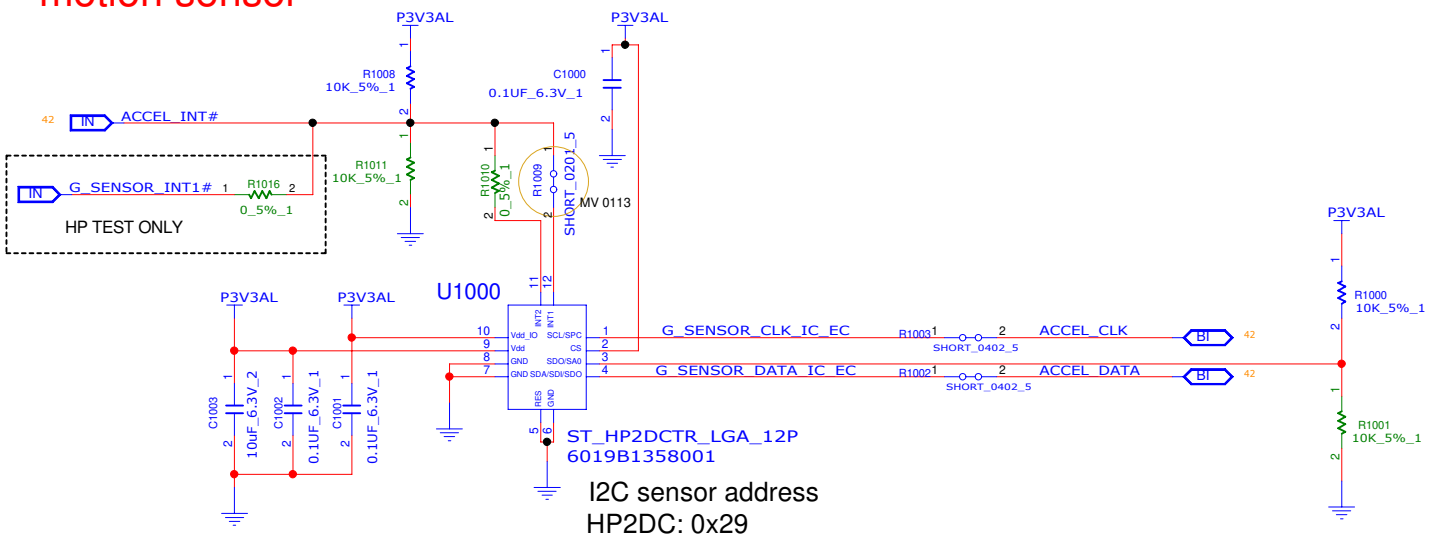
CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

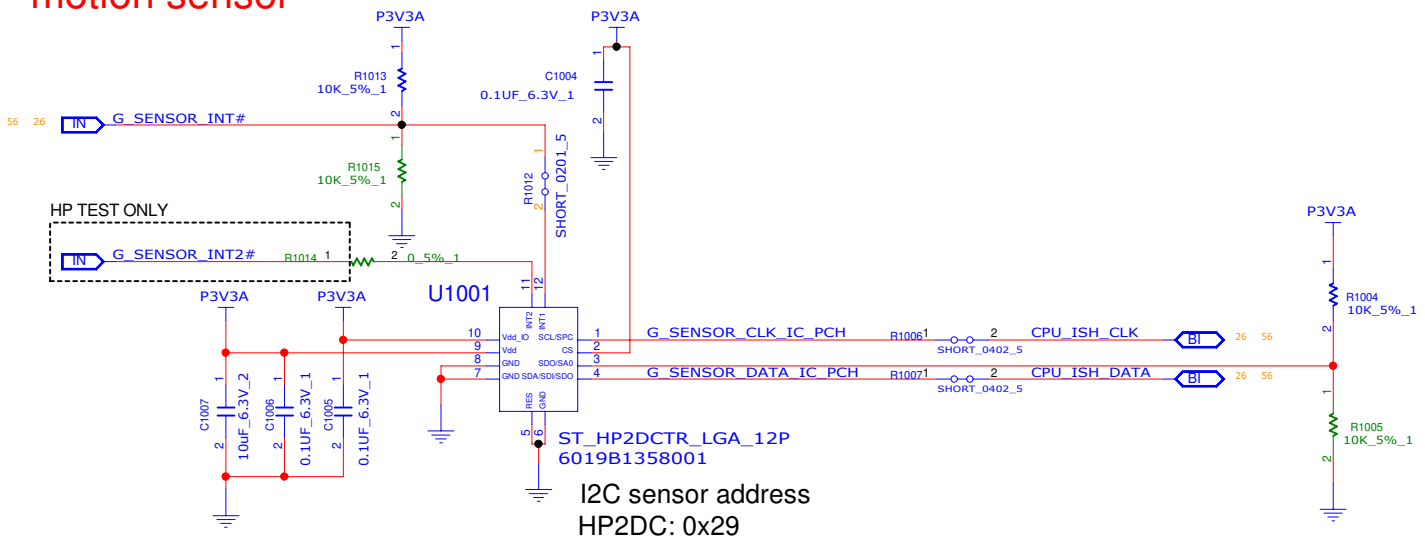
3-axis "femto" accelerometer
motion sensor

EC SIDE



3-axis "femto" accelerometer
motion sensor

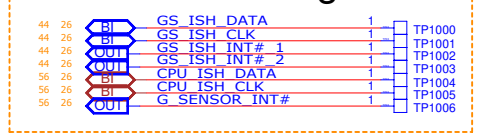
PCH SIDE



Applications

- Motion-activated functions
- Display orientation
- Shake control
- Pedometer
- Gaming and virtual reality input devices
- Impact recognition and logging

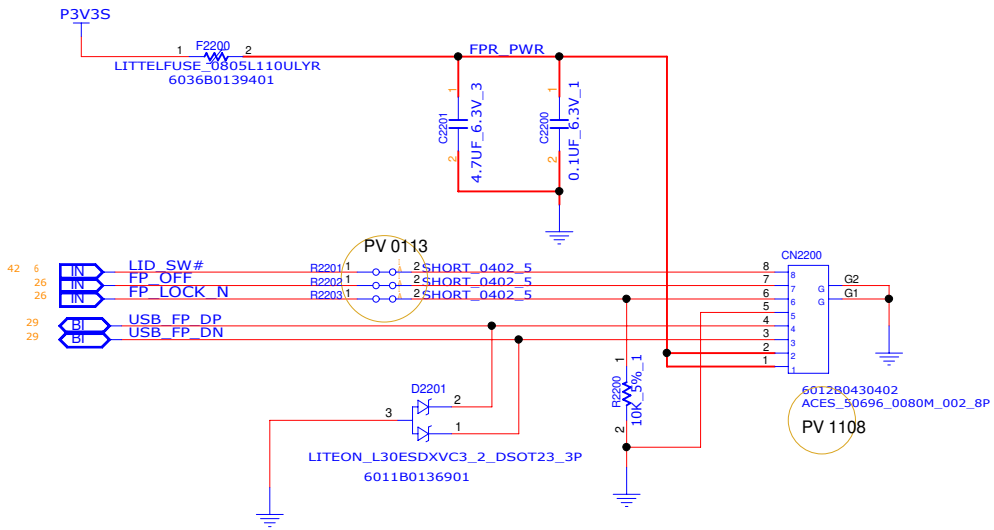
Sensor Debug Port



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION CAMERA		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 56 of 73			
CHANGE by XXX		DATE 21-OCT-2002	
PCB P/N 60xxxxxxxxx		PCB VER XXX	

FINGER PRINTER



Pin Define	
PIN 1	3.3v
PIN 2	3.3V
PIN 3	D-
PIN 4	D+
PIN 5	GND
PIN 6	LOCK_N
PIN 7	FPR_OFF
PIN 8	Lid-Close

CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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FINGER CLIP FOR MEMORY

6053B1063701

DDR

CP7514 EMI_STOP_SUL_15A8M_1P
CP7515 EMI_STOP_SUL_15A8M_1P 6053B1063701
CP7500 EMI_STOP_SUL_15A8M_1P
CP7501 EMI_STOP_SUL_15A8M_1P
CP7513 EMI_STOP_SUL_15A8M_1P
CP7502 EMI_STOP_SUL_15A8M_1P
CP7512 EMI_STOP_SUL_15A8M_1P
CP7503 EMI_STOP_SUL_15A8M_1P
CP7511 EMI_STOP_SUL_15A8M_1P
CP7510 EMI_STOP_SUL_15A8M_1P
CP7509 EMI_STOP_SUL_15A8M_1P
CP7508 EMI_STOP_SUL_15A8M_1P
CP7507 EMI_STOP_SUL_15A8M_1P
CP7506 EMI_STOP_SUL_15A8M_1P
CP7505 EMI_STOP_SUL_15A8M_1P
CP7504 EMI_STOP_SUL_15A8M_1P

SSD

CP7527 EMI_STOP_SUL_15A8M_1P
CP7516 EMI_STOP_SUL_15A8M_1P
CP7526 EMI_STOP_SUL_15A8M_1P
CP7517 EMI_STOP_SUL_15A8M_1P
CP7525 EMI_STOP_SUL_15A8M_1P
CP7518 EMI_STOP_SUL_15A8M_1P
CP7524 EMI_STOP_SUL_15A8M_1P
CP7519 EMI_STOP_SUL_15A8M_1P
CP7523 EMI_STOP_SUL_15A8M_1P
CP7520 EMI_STOP_SUL_15A8M_1P
CP7522 EMI_STOP_SUL_15A8M_1P
CP7521 EMI_STOP_SUL_15A8M_1P

CHANGE NO	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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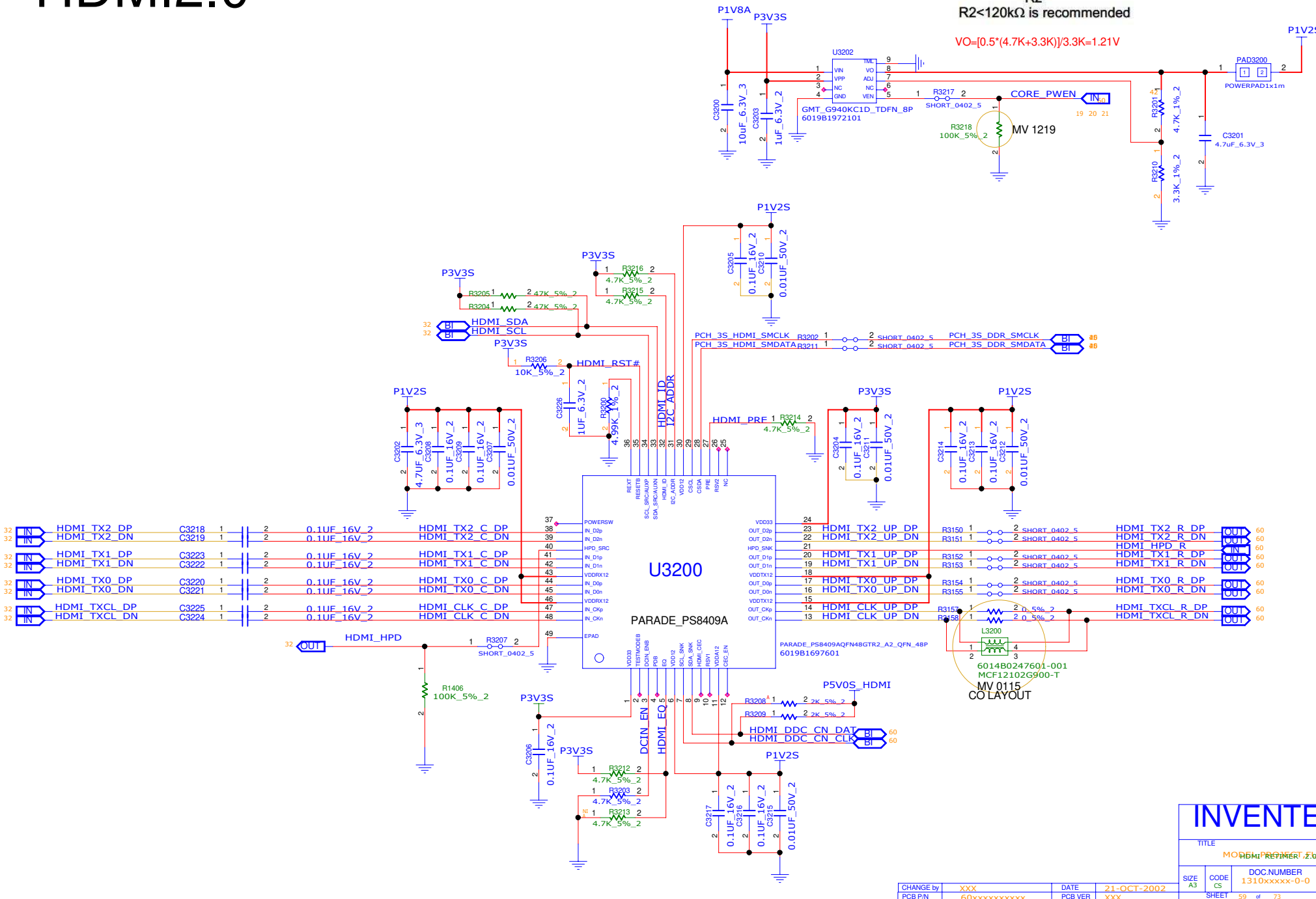
HDMI2.0

$$VO = \frac{0.5\,(R1+R2)}{R2}\ \text{Volts}$$

R2<120kΩ is recommended

VO=[0.5*(4.7K+3.3K)]/3.3K=1.21V



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL PROJECT FUNCTION — HDMI RETIMER 2.0 /CONN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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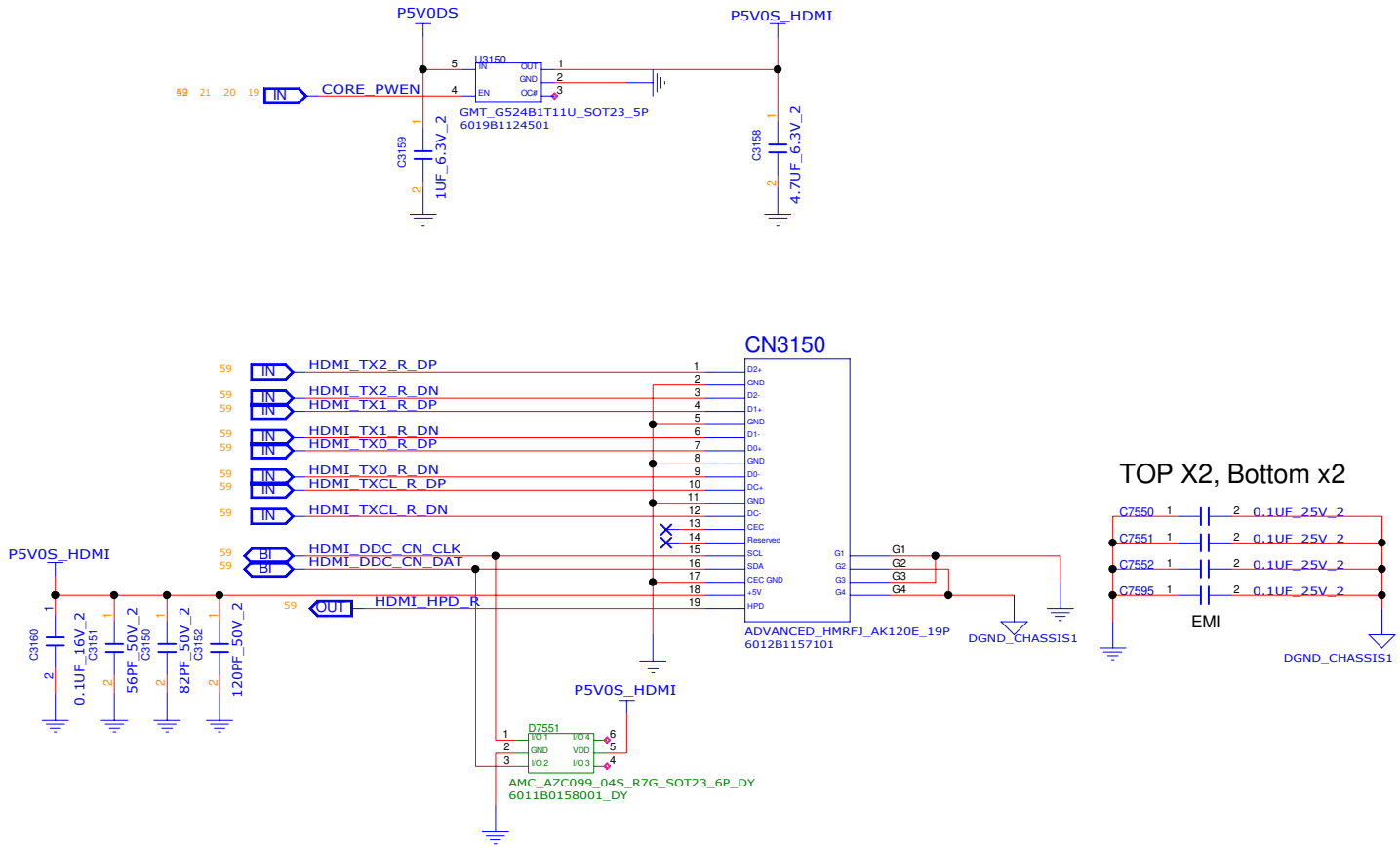
HDMI



CHANGE by	<ENG>	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	<VER>

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
HDMI CONN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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X360

M.2 WWAN

CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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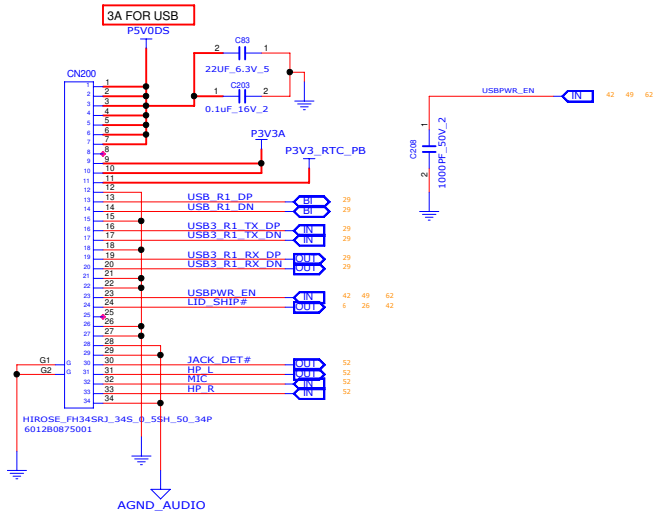
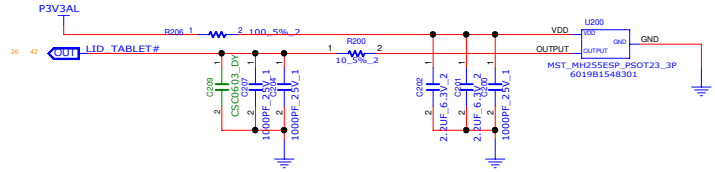
MB TO USB AUDIO BOARD CONN

MB TO USB&AUDIO



LID SW 2



CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

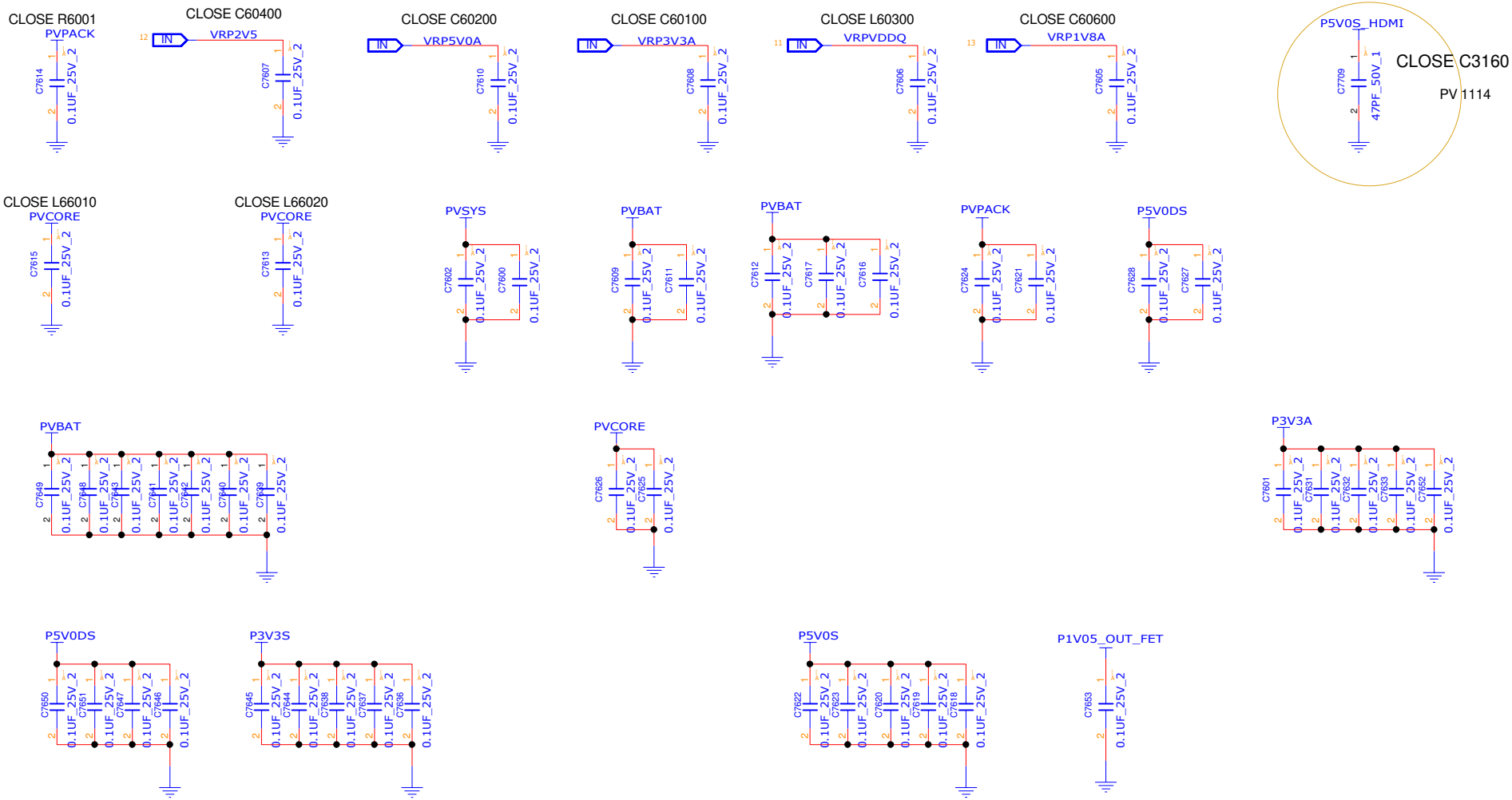
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 62 of 73

EMI SOLUTION



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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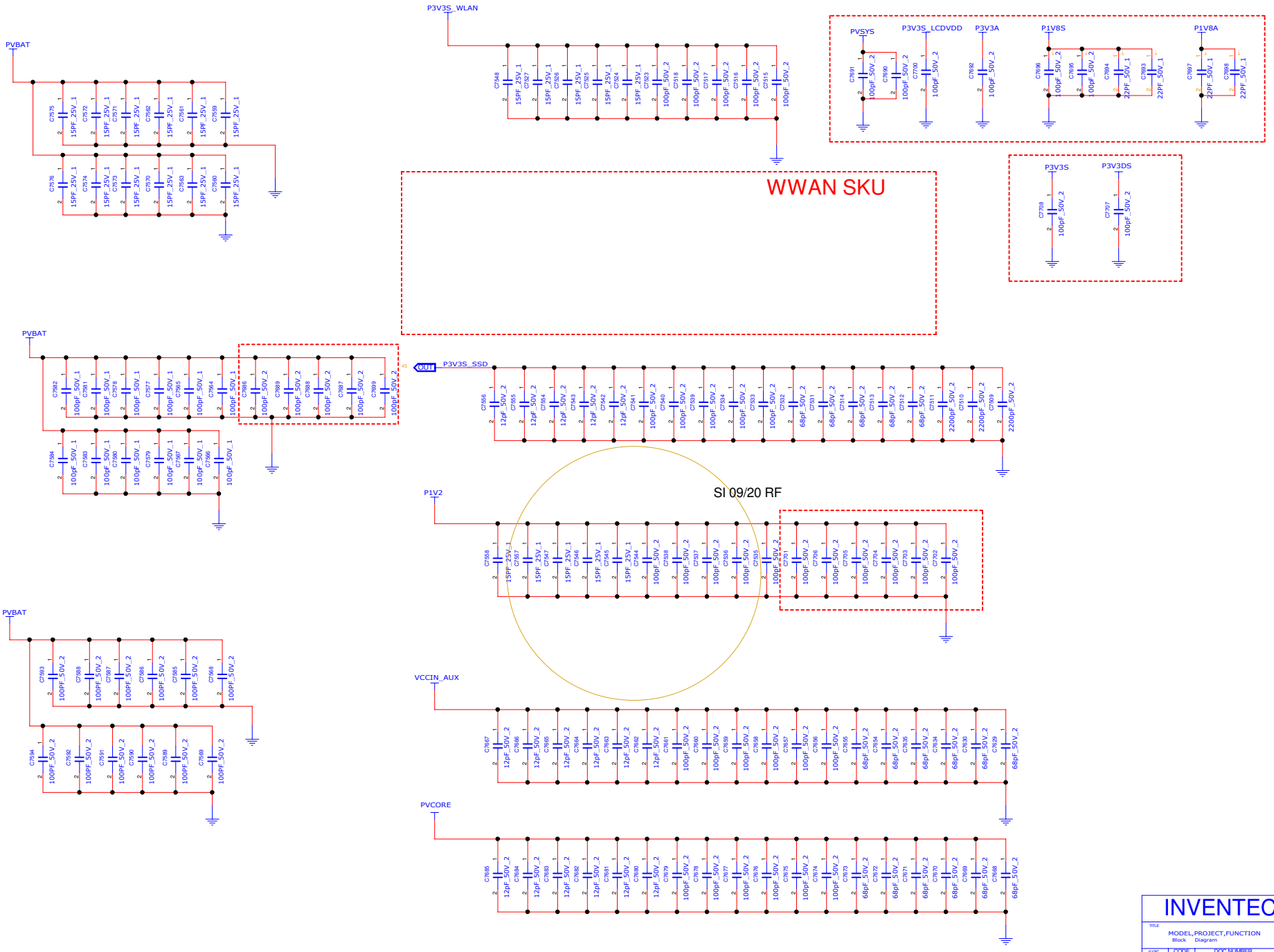
RF SOLUTION

LOCATION: 7500 - 7599



INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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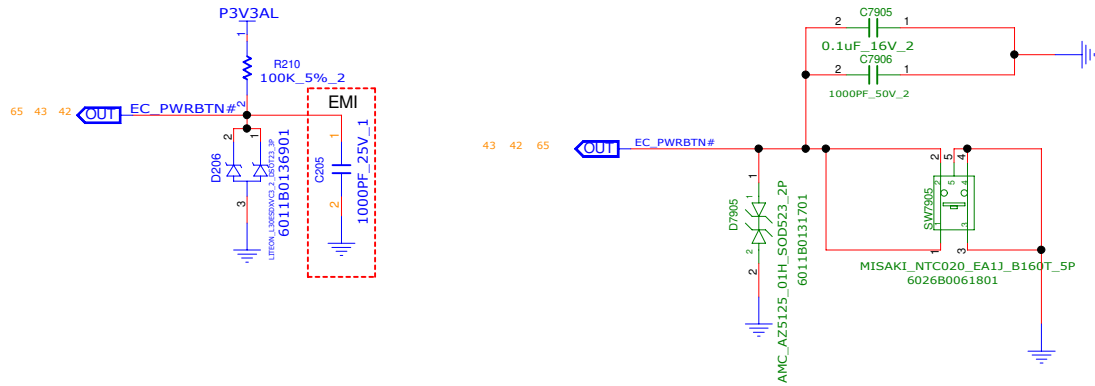
CHANGE N	XXX	DATE	21-OCT-2002
PCB P/N	50xxxxxxxxx	PCB VER	XXX

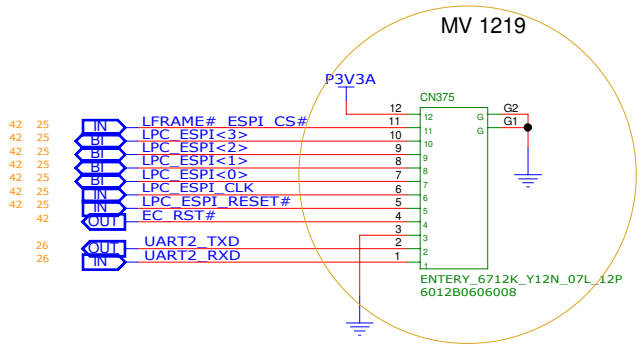
DEBUG PORT / ESPI DEBUG CNTR

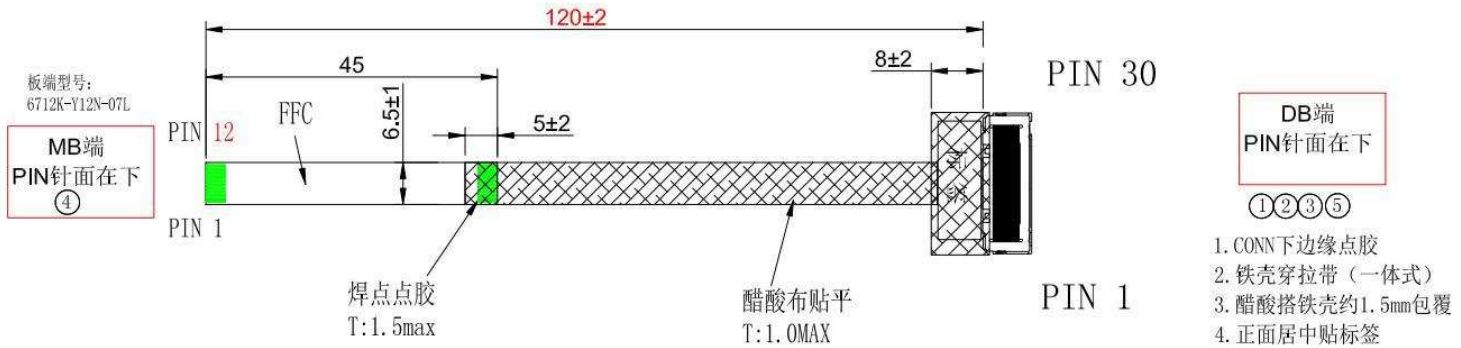
DEBUG PORT

DB	MB	PIN DEFINE
22	1	P3V3A
6	2	LPC_FRAME_ESPI_CS
7	3	LPC_ESPI_IO<3>
8	4	LPC_ESPI_IO<2>
9	5	LPC_ESPI_IO<1>
10	6	LPC_ESPI_IO<0>
11	7	ESPI_CLK_33MHz
12	8	ESPI_RST_N
16	9	EC_RST#
3	10	DGND
28	11	UART_HEADER_TXD
29	12	UART_HEADER_RXD

TACK SWITCH







INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SCREW HOLE

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

SMALL BOARD

DATE	CHANGE NO.	REV
21-OCT-2002		A

DESIGN / DRAWER	SEB CHANG	DATE	21-OCT-2002
CHECK	SEB CHANG		
APPROVAL	CHO ADAM		
FILE NAME	W:\WINCE\TOUCH SCREEN BPARD		
PCB P/N	50xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE MODEL,PROJECT,FUNCTION

SIZE	CODE	DOC.NUMBER	REV
A3	CS	131Dxxxxx-0-0	X01

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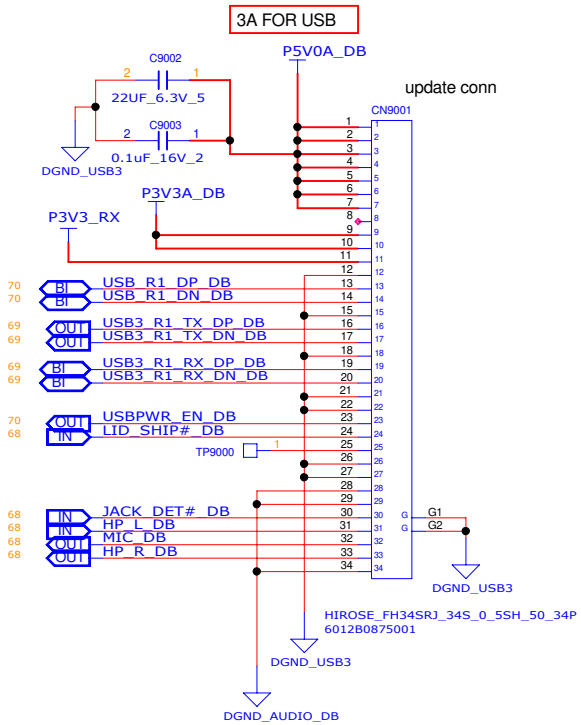
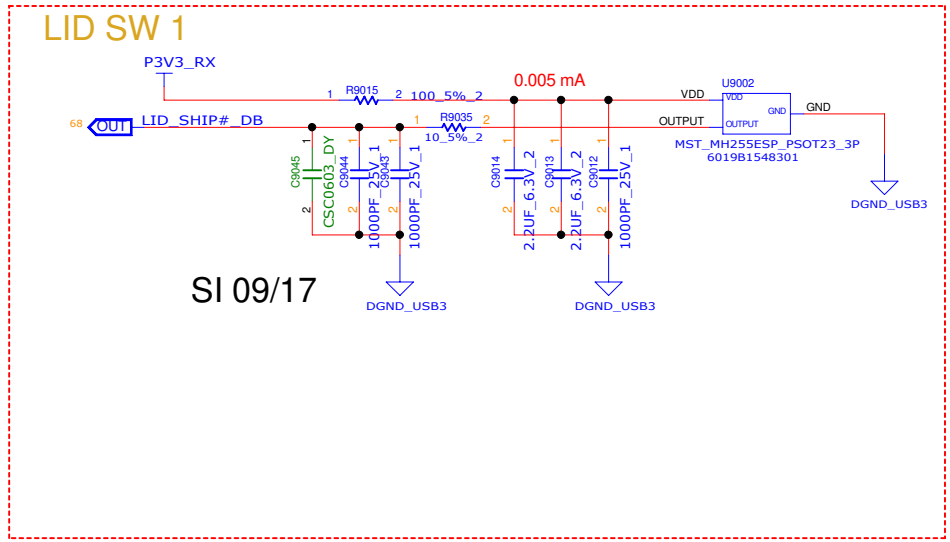
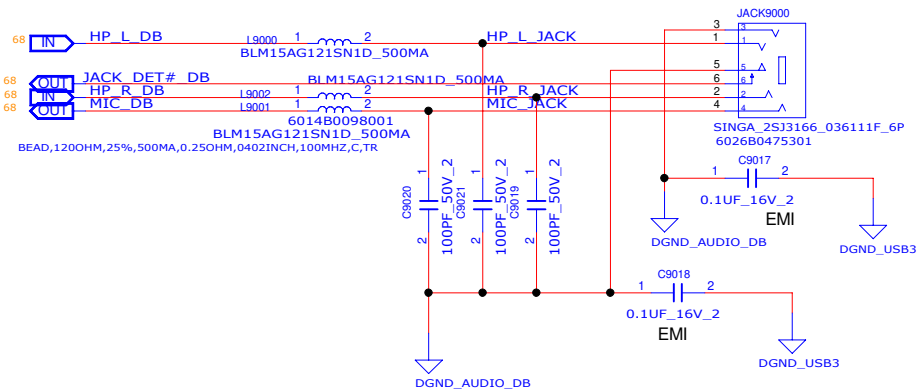
USB BOARD

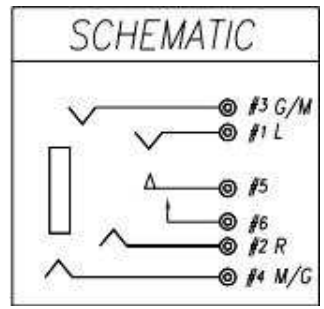
VER.09_20171109
LOCATION: 9000~9200





COMBO JACK





INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	
PCB P/N	60.NXXXX.XXXX	PCB VER	XX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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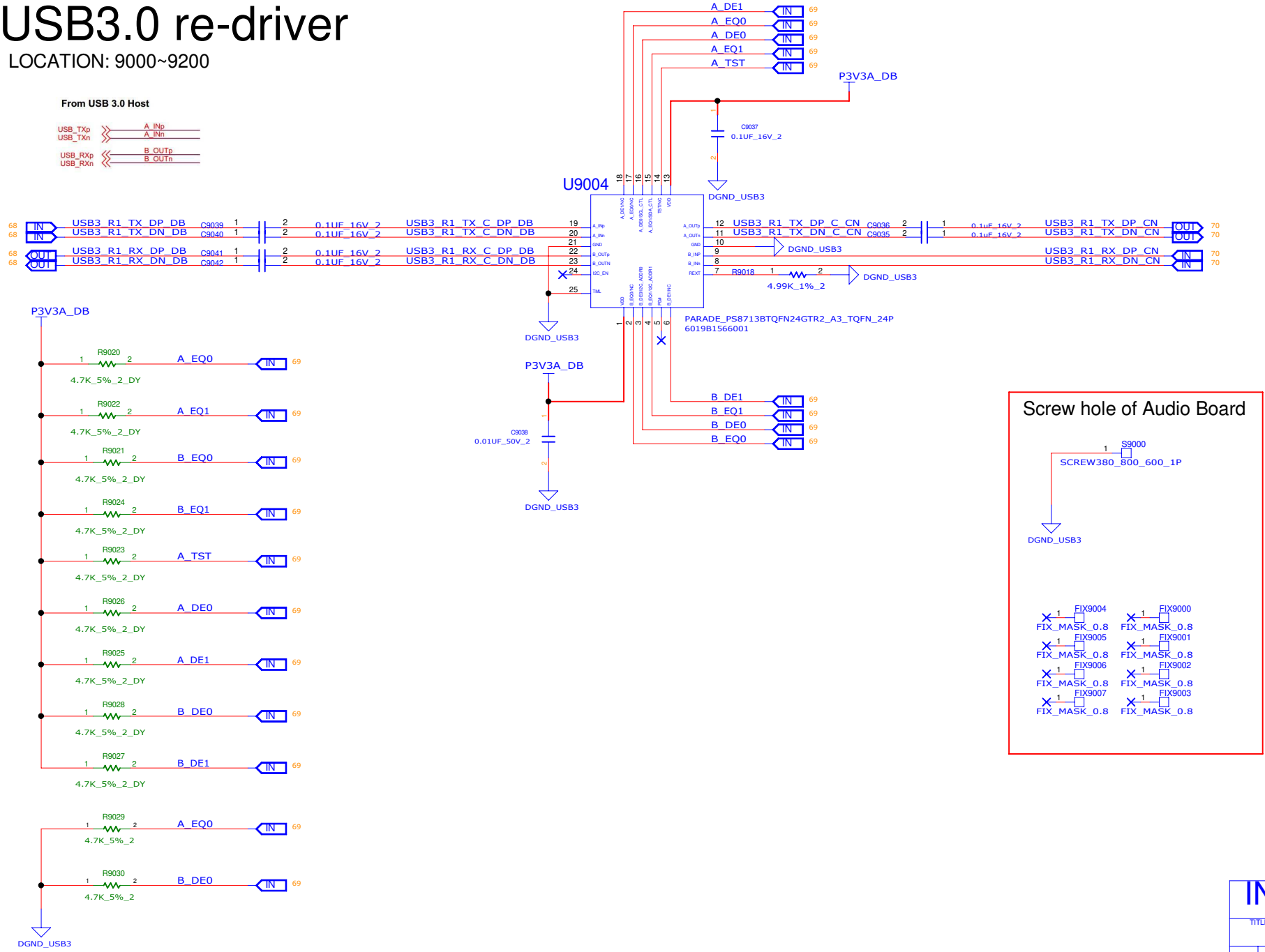
USB3.0 re-driver

LOCATION: 9000~9200



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
USB 3.0 CONN & M/B TO D/B CONN

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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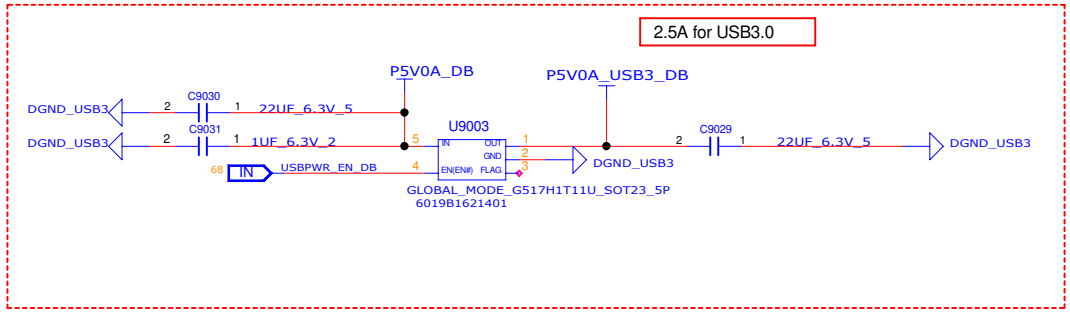
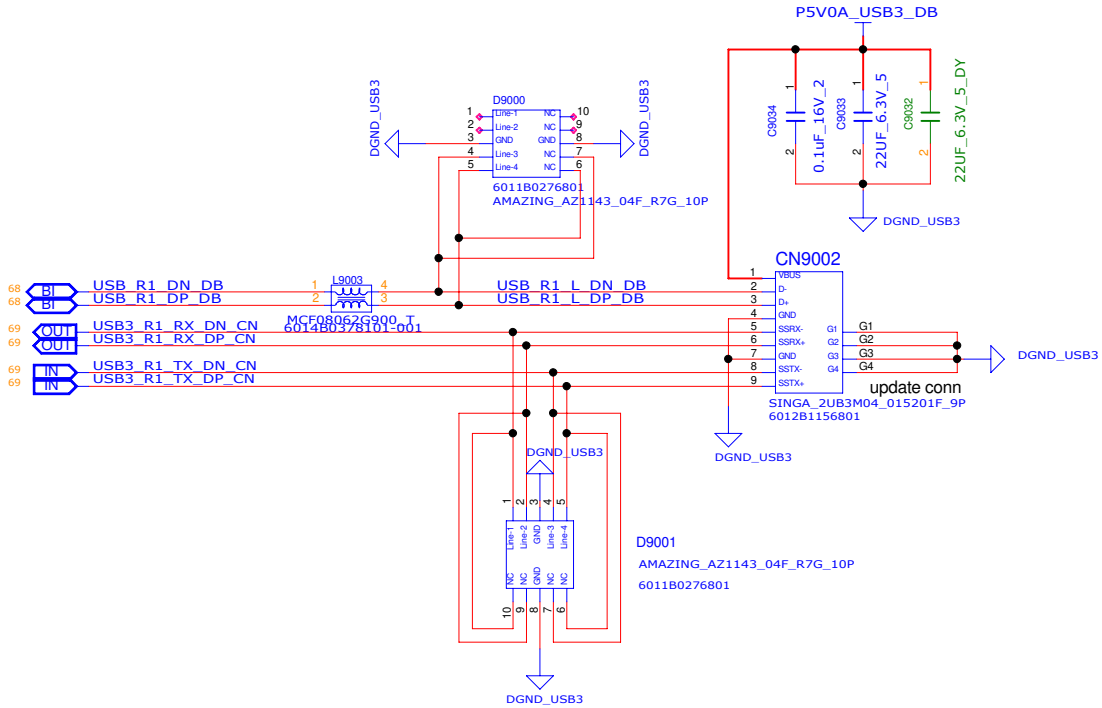
CHANGE by	XXX	DATE	
PCB P/N	60NBxxxxxxxx	PCB VER	XXOCT-2002

USB3.0

LOCATION 2400~2499

LOCATION: 9000~9200





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
USB 3.0 CONN & M/B TO D/B CONN

CHANGE by	XXX	DATE	
PCB P/N	60NS6xxxxxxx	PCB VER	XVER

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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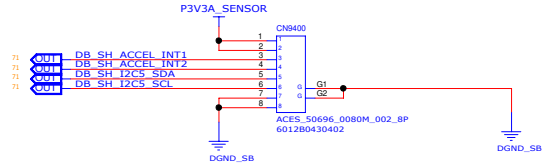
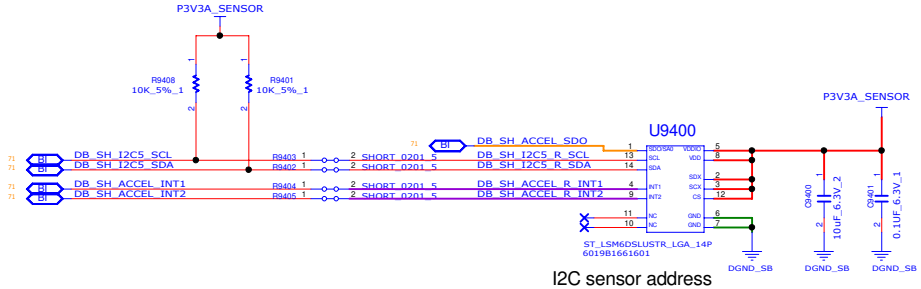
G-Sensor Board

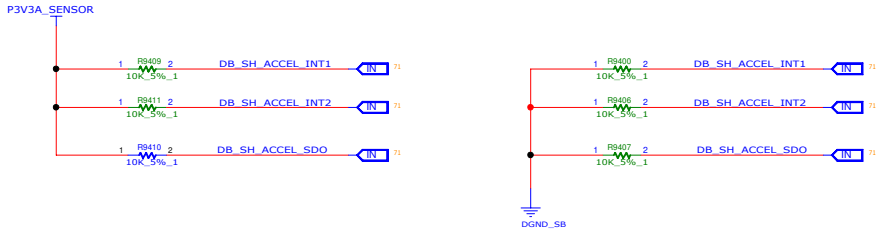
REFERENCE NUMBER:9400~9499

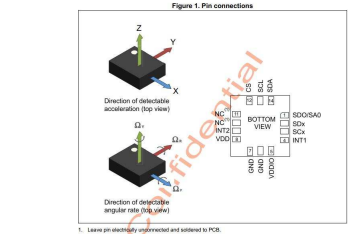
I = Monut
NI = No Monut





I2C sensor address
LSM6DSL: 0x6b





4.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		1.71	1.8	3.6	V
Vdd_IO	Power supply for I/O		1.62		3.6	V
IddHP	Gyroscope and accelerometer current consumption in high-performance mode	ODR = 1.6 kHz		0.65		mA
IddNM	Gyroscope and accelerometer current consumption in normal mode	ODR = 208 Hz		0.45		mA
IddLP	Gyroscope and accelerometer current consumption in low-power mode	ODR = 52 Hz		0.20		mA

I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address (7 bits) and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When no address is sent, each device in the system compares the first seven bits after a START condition with its address. If they match, the device considers itself addressed by the master.

The Serial Address (SAD) associated to the LSM6DSLUS is 1101l1xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is '1' (address 1101101b); else if the SDO/SA0 pin is connected to ground, the LSb value is '0' (address 1101100b). This solution permits to connect and address two different inertial modules to the same I²C bus.

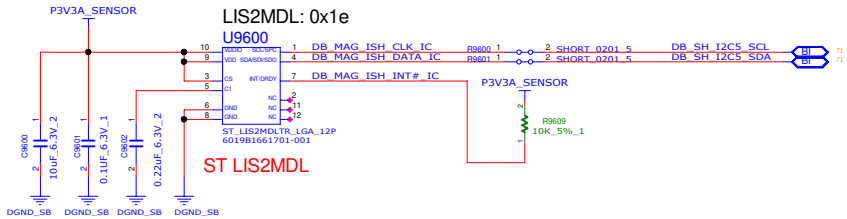
LSM6DSLUS
6D orientation
always-on 3D accelerometer and 3D gyroscope

3-axis magnetometer

magnetic sensor

I = Monut
NI = No Monut

I2C sensor address
LIS2MDL: 0x1e



Applications

- Tilt-compensated compasses
- Map rotation
- Intelligent power saving for handheld devices
- Gaming and virtual reality input devices

Base on Balos schematic , the I2C slave address is as following.
LIS2MDL: 0x1e
HP2DC: 0x29
LSM6DSL: 0x6b

CHANGE by	XXX	DATE	
PCB P/N	60.xxxxx.xxxx	PCB VER	XXXRev

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
LVDS

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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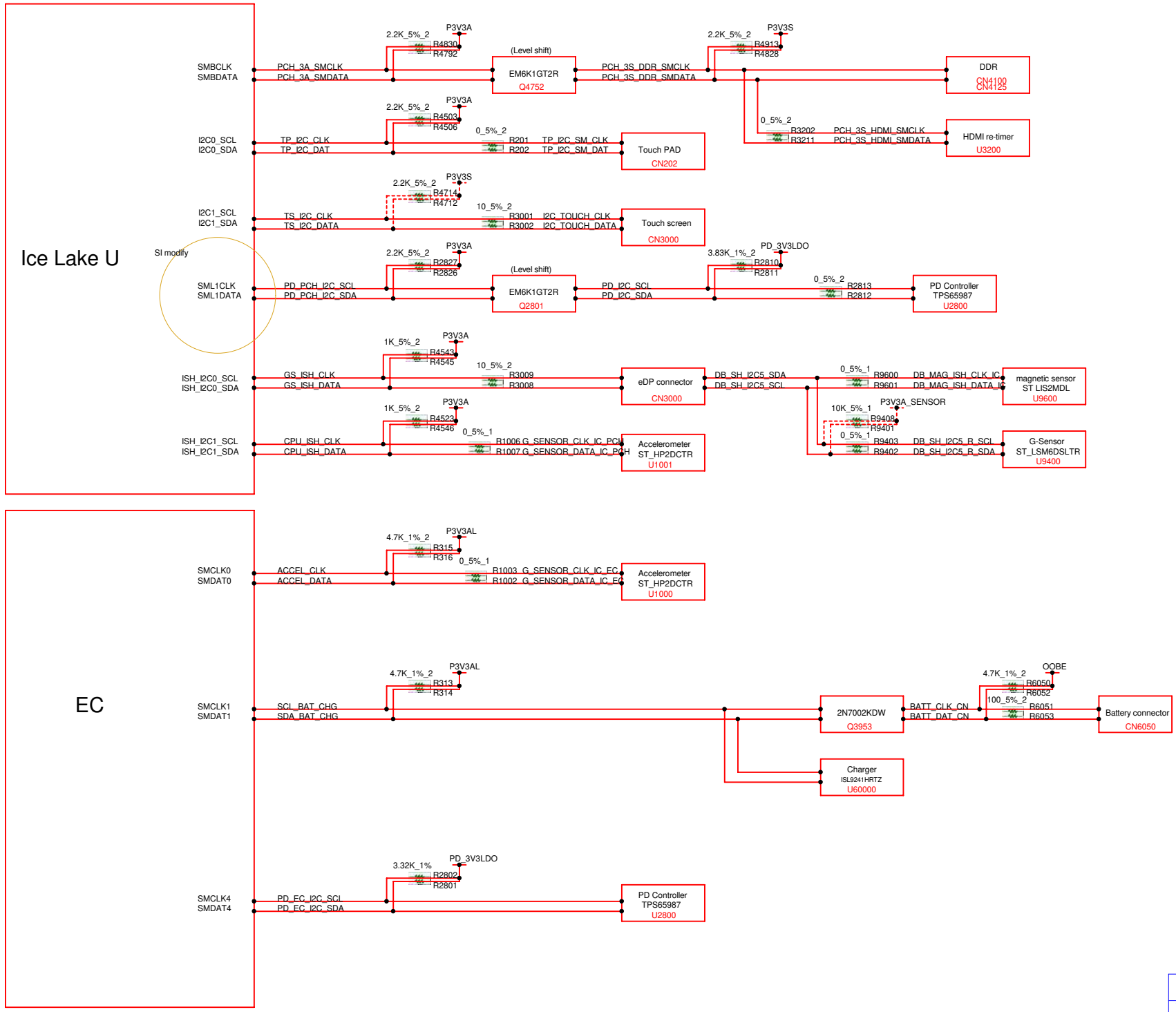
Ice Lake U
SI modify
SMBCLK
SMBDATA
PCH_3A_SMCLK
PCH_3A_SMDATA
2.2K_5%_2
P3V3A
R4830
R4792
(Level shift)
EM6K1GT2R
Q4752
PCH_3S_DDR_SMCLK
PCH_3S_DDR_SMDATA
2.2K_5%_2
P3V3S
R4913
R4828
DDR
CN4100
CN4125
I2C0_SCL
I2C0_SDA
TP_I2C_CLK
TP_I2C_DAT
2.2K_5%_2
P3V3A
R4503
R4506
0_5%_2
R201
R202
TP_I2C_SM_CLK
TP_I2C_SM_DAT
Touch PAD
CN202
0_5%_2
R3202
R3211
PCH_3S_HDMI_SMCLK
PCH_3S_HDMI_SMDATA
HDMI re-timer
U3200
I2C1_SCL
I2C1_SDA
TS_I2C_CLK
TS_I2C_DATA
2.2K_5%_2
P3V3S
R4714
R4712
10_5%_2
R3001
R3002
I2C_TOUCH_CLK
I2C_TOUCH_DATA
Touch screen
CN3000
SML1CLK
SML1DATA
PD_PCH_I2C_SCL
PD_PCH_I2C_SDA
2.2K_5%_2
P3V3A
R2827
R2826
(Level shift)
EM6K1GT2R
Q2801
PD_I2C_SCL
PD_I2C_SDA
3.83K_1%_2
PD_3V3LDO
R2810
R2811
0_5%_2
R2813
R2812
PD Controller
TPS65987
U2800
ISH_I2C0_SCL
ISH_I2C0_SDA
GS_ISH_CLK
GS_ISH_DATA
1K_5%_2
P3V3A
R4543
R4545
10_5%_2
R3009
R3008
eDP connector
CN3000
DB_SH_I2C5_SDA
DB_SH_I2C5_SCL
0_5%_1
R9600
R9601
DB_MAG_ISH_CLK_IC
DB_MAG_ISH_DATA_IC
magnetic sensor
ST LIS2MDL
U9600
ISH_I2C1_SCL
ISH_I2C1_SDA
CPU_ISH_CLK
CPU_ISH_DATA
1K_5%_2
P3V3A
R4523
R4546
0_5%_1
R1006 G_SENSOR_CLK_IC_PCH
R1007 G_SENSOR_DATA_IC_PCH
Accelerometer
ST_HP2DCTR
U1001
P3V3A_SENSOR
10K_5%_1
R9408
R9401
0_5%_1
R9403
R9402
DB_SH_I2C5_R_SCL
DB_SH_I2C5_R_SDA
G-Sensor
ST_LSM6DSLTR
U9400
EC
SMCLK0
SMDAT0
ACCEL_CLK
ACCEL_DATA
4.7K_1%_2
P3V3AL
R315
R316
0_5%_1
R1003 G_SENSOR_CLK_IC_EC
R1002 G_SENSOR_DATA_IC_EC
Accelerometer
ST_HP2DCTR
U1000
SMCLK1
SMDAT1
SCL_BAT_CHG
SDA_BAT_CHG
4.7K_1%_2
P3V3AL
R313
R314
2N7002KDW
Q3953
BATT_CLK_CN
BATT_DAT_CN
4.7K_1%_2
OOBE
R6050
R6052
100_5%_2
R6051
R6053
Battery connector
CN6050
Charger
ISL9241HRTZ
U60000
SMCLK4
SMDAT4
PD_EC_I2C_SCL
PD_EC_I2C_SDA
3.32K_1%
PD_3V3LDO
R2802
R2801
PD Controller
TPS65997
U2800
INVENTEC
MODEL,PROJECT,FUNCTION
KBC
SIZE A3
CODE CS
DOC NUMBER 1310xxxxx-0-0
REV X01
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CHANGE N
PCB P/N
KEWG-
60xxxxxxxxx
DATE
21-OCT-2002
PCB VER
XXX

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE

MODEL,PROJECT,FUNCTION

Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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