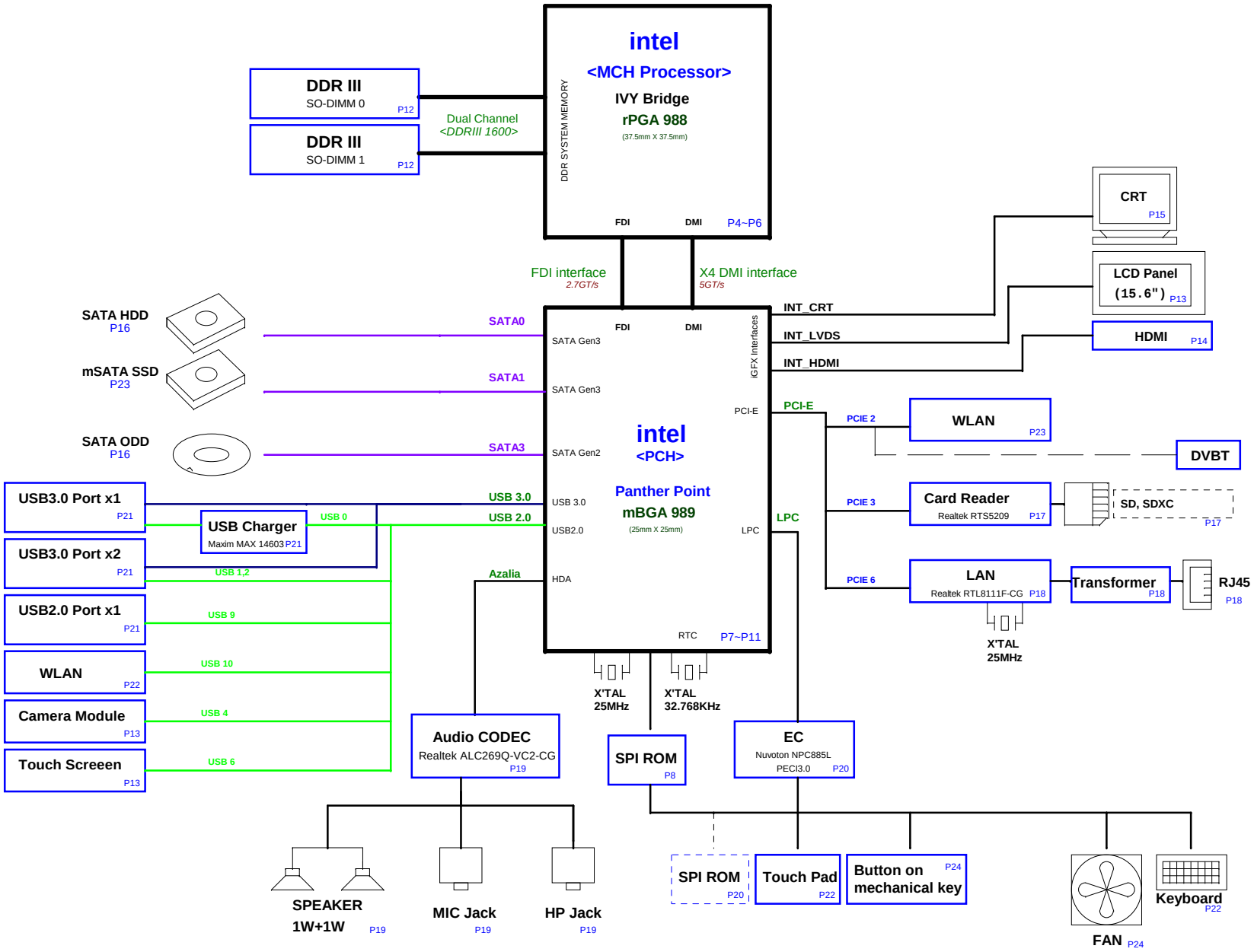
MODEL	REV	CHANGE LIST
FF4 M/B	1A	

Page	FF4 Main BOARD	
	FROM	TO
1		1A
2		1A
3		1A
4		1A
5		1A
6		1A
7		1A
8		1A
9		1A
10		1A
11		1A
12		1A
13		1A
14		1A
15		1A
16		1A
17		1A
18		1A
19		1A
20		1A
21		1A
22		1A
23		1A
24		1A
25		1A
26		1A
27		1A
28		1A
29		1A
30		1A
31		1A
32		1A
33		1A
34		1A
35		1A

QUANTA COMPUTER				
PROJECT : FF4	DOCUMENT NO : 204	TITLE : M/B	ASSEMBLY P/N : .	
APPROVED BY: Frank Tsui	DRAWING BY Thomas Kang	REV : 1C	DATE :	Sheet 1 of 35

FF4 SYSTEM BLOCK DIAGRAM



vinafix

Quanta Computer Inc.		
PROJECT : FF4		
Size	Document Number: SYSTEM BLOCK DIAGRAM	Rev: 1C
Date: Sunday, December 11, 2011	Sheet 2 of 35	

Table of Contents

FF4 (SF4) Power Rails

Power	Voltage	S0	S3	S4	S5	Ctl Signal
+5VPCU	5V	V	V	V	V	6237LDO5
+3VPCU	3.3V	V	V	V	V	6237LDO5
+3V_LAN	3.3V	V	V	NOTE 1	NOTE 1	LAN_ON_D
+5V_S5	5V	V	V	NOTE 2	NOTE 2	RVCCD
+3V_S5	3.3V	V	V	NOTE 2	NOTE 2	RVCCD
+1.5V_SUS	1.5V	V	V			SUS_ON
+3V_SUS	3.3V	V	V			SUSD
+0.75V_DDR_VTT	0.75V	V				+1.5V_CPUVDDQ_PG
+SMDDR_VREF	0.75V	V	V			SUS_ON
+5V_RUN	5V	V				MAIND
+3V_RUN	3.3V	V				MAIND
+1.8V	1.8V	V				+3V_RUN
+1.5V	1.5V	V				MAIND
+1.05V	1.05V	V				RUN_ON
+VCCSA	By VID	V				1.05V_VTT_PWRGD
+VCC_GFX	By VID	V				ALL_SYS_PWRGD
+VCC_CORE	By VID	V				ALL_SYS_PWRGD

NOTE 1:ON AT WOL FUNCTION ENABLE

NOTE 2:ON FOR WAKE UP FUNCTION DURING S4/S5

PCB STACK UP

6L

LAYER 1 : TOP

LAYER 2 : GND

LAYER 3 : IN1

LAYER 4 : IN2

LAYER 5 : VCC

LAYER 6 : BOT

Quanta Computer Inc.

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FRONT PAGE

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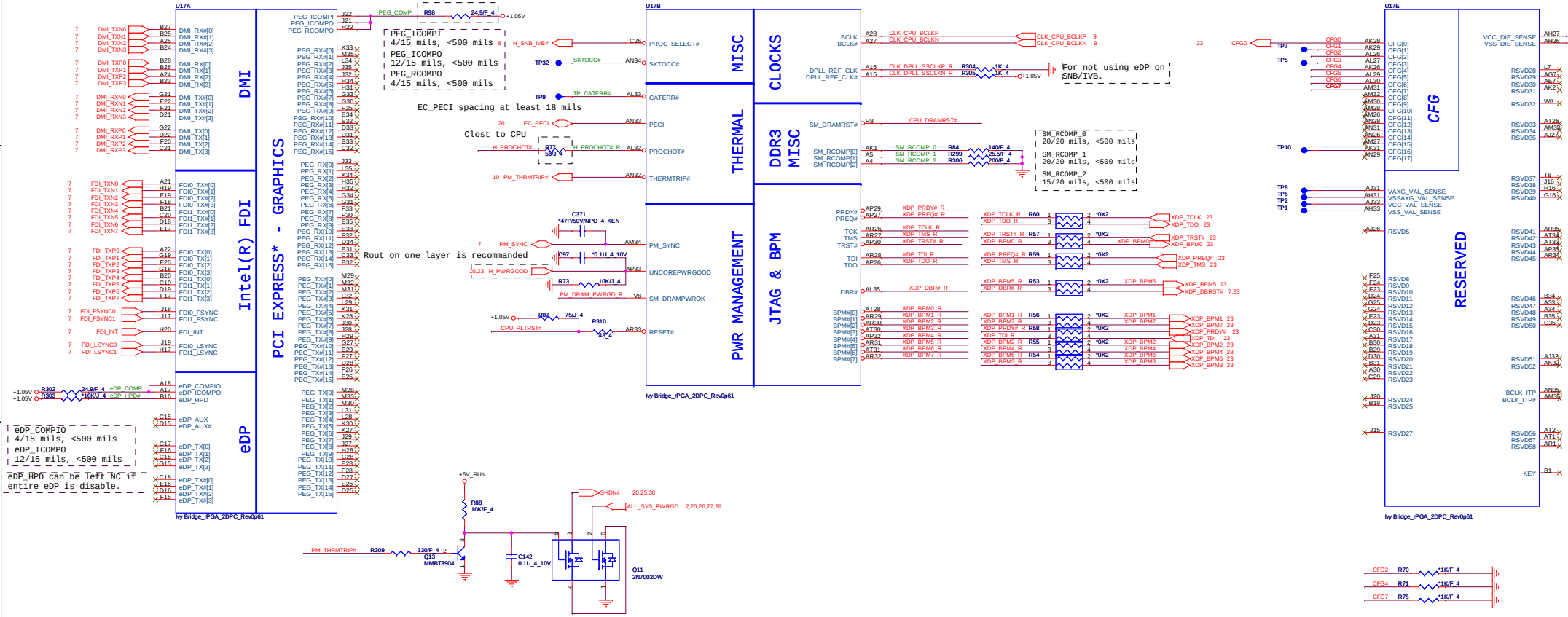
IVYB 1/4(HOST&PCIE&CFG)

IVY Bridge Processor (DMI,PEG,FDI)

IVY Bridge Processor (CLK,MISC,JTAG)

IVY Bridge Processor (RSVD, CFG)



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - X16 PEG interface
10: PEG x8 x8 bifurcation enableddisabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

The CFG signals have a default value of '1' if not terminated on the board.

Processor Strapping

	1	0
CFG2 (PEG Static Lane Reversal)	**Normal Operation**	Lane Reversed
CFG4 (DP Presence Strap)	**Disable; No physical DP attached to eDP**	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	**PEG train immediately following xxRESETB de assertion**	PEG wait for BIOS training

Quanta Computer Inc.
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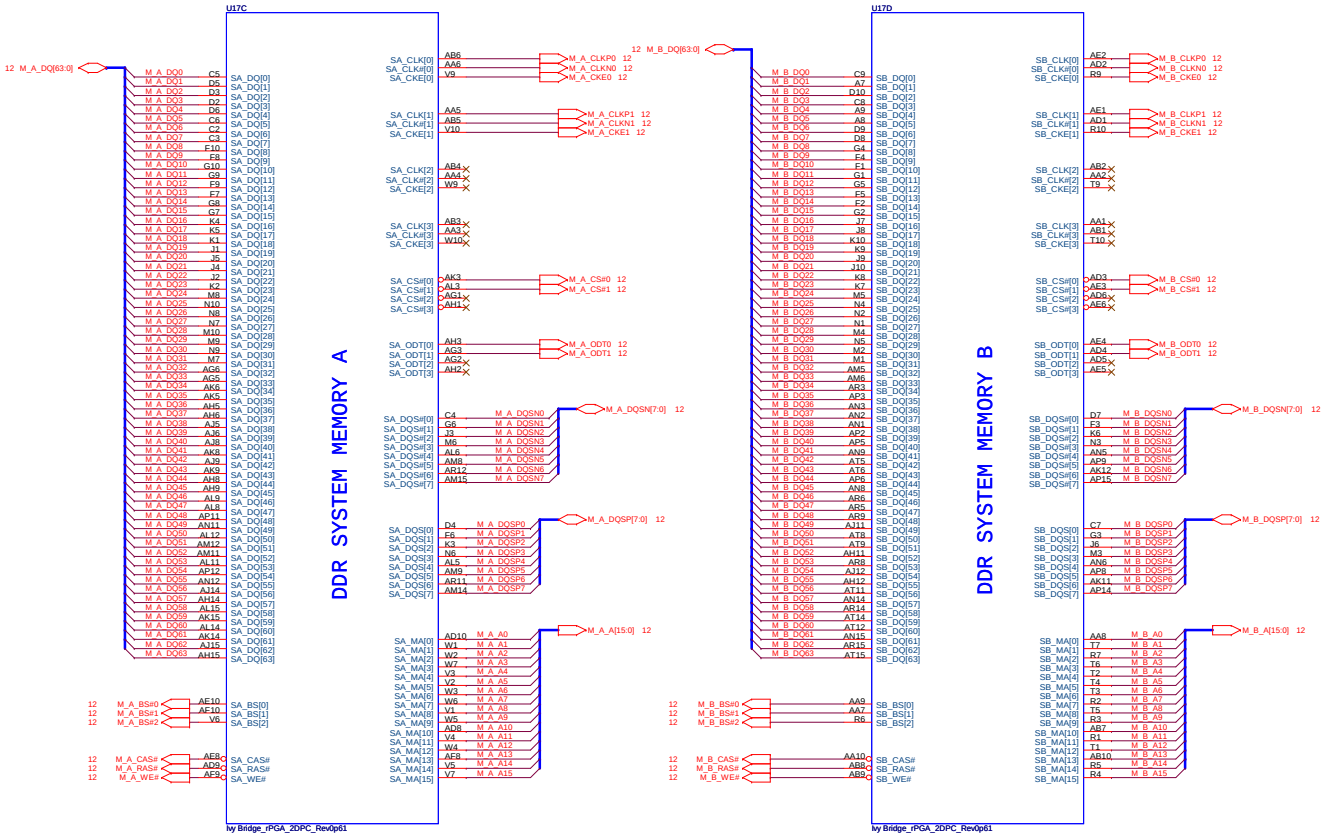
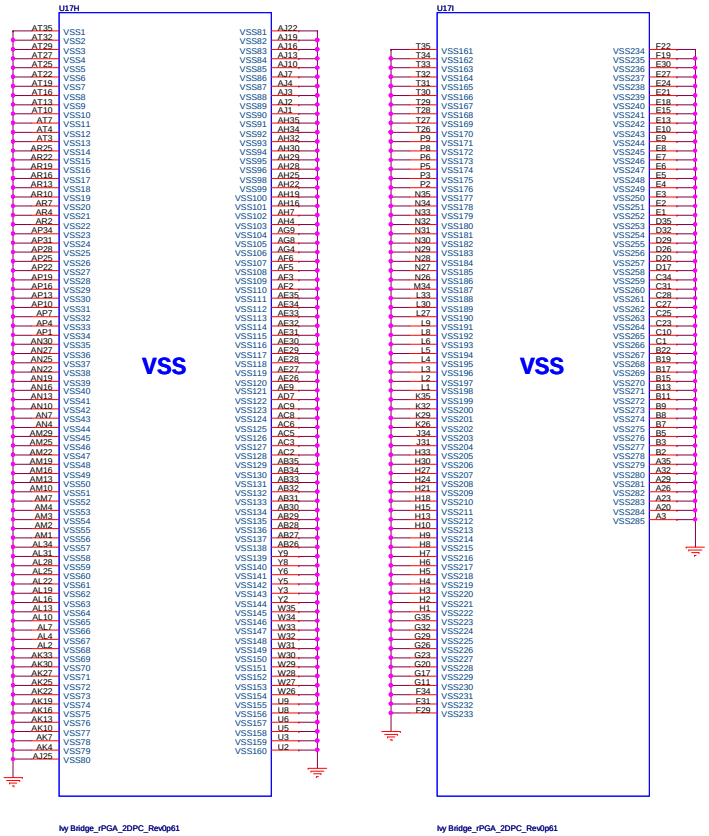
IVYB 2/3(DDR3 I/F&GND)

IVY Bridge Processor (DDR3)



IVY Bridge Processor (GND)



Quanta Computer Inc.			
PROJECT : FF4			
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	IVYB 2/3(DDR3 I/F&GND)		1C
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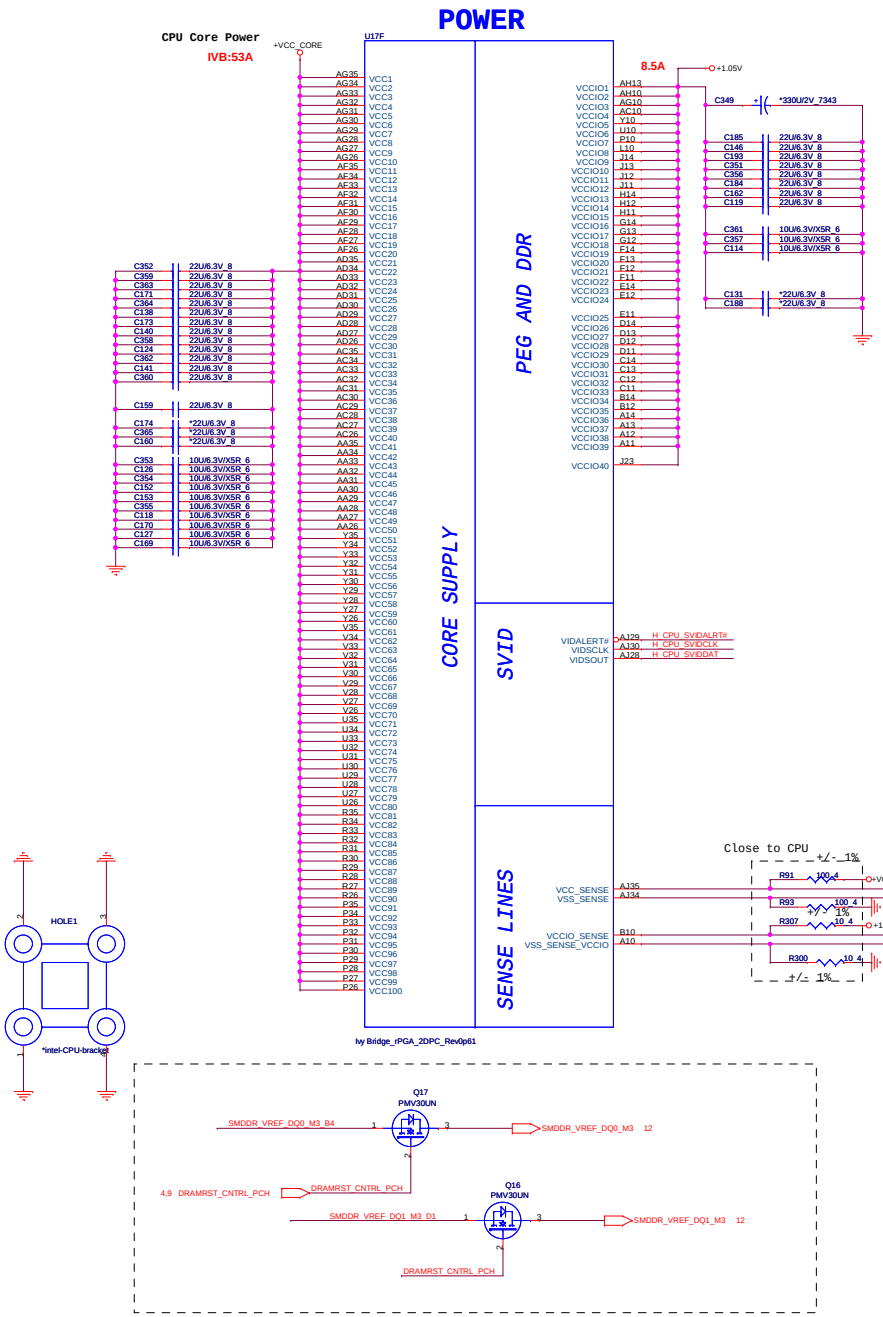
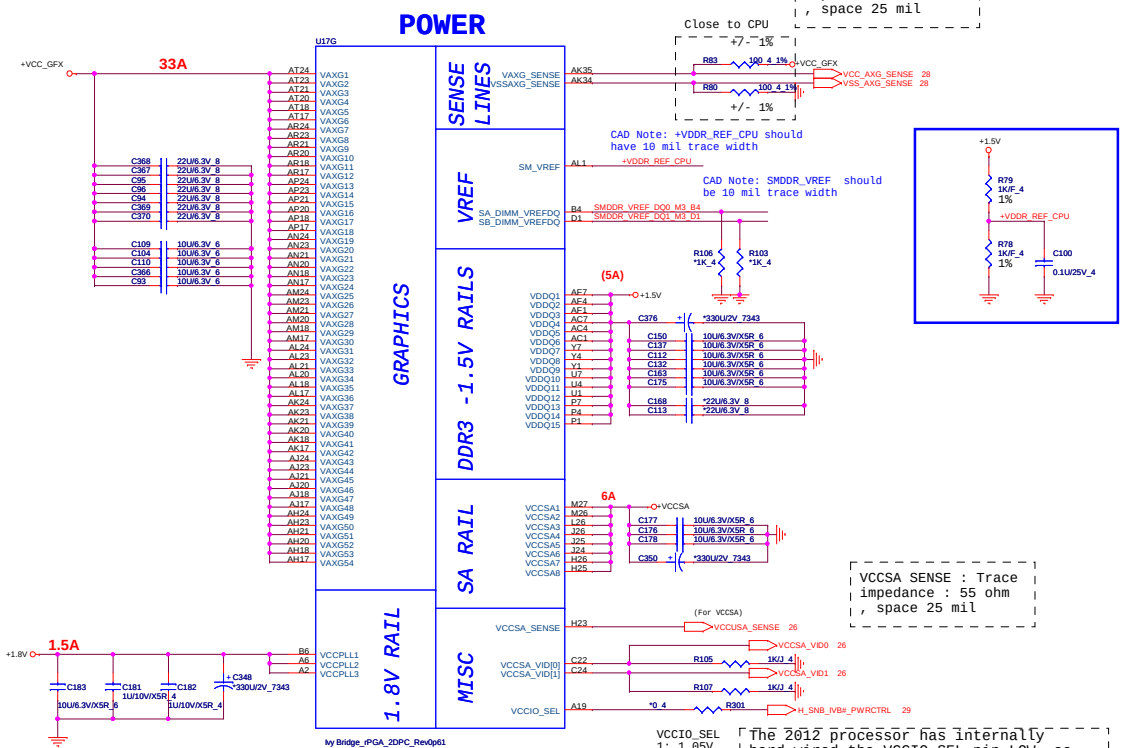
IVY Bridge Processor (POWER)



VCC SENSE : Trace impedance : 27~33 ohm , space 25 mil

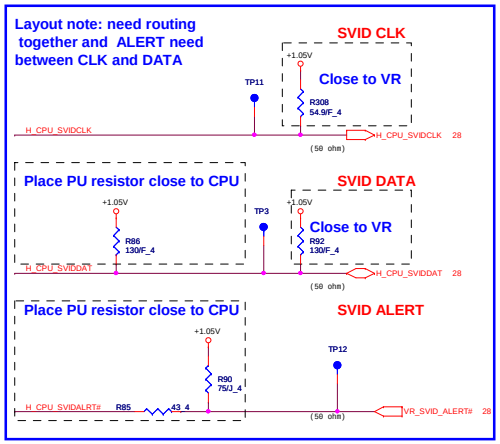
VCCIO SENSE : Trace impedance : 55 ohm , space 25 mil

IVY Bridge Processor (GRAPHIC POWER)



VCCIO_SEL
1: 1.05V
0: 1.00V

The 2012 processor has internally hard-wired the VCCIO_SEL pin LOW ,so removal of this series resistor will restore the signal to the "1" level for a 1.05-V selection --CR_PDDG rev_0.8



Quanta Computer Inc.
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IVYB 3/3(POWER) | 1C
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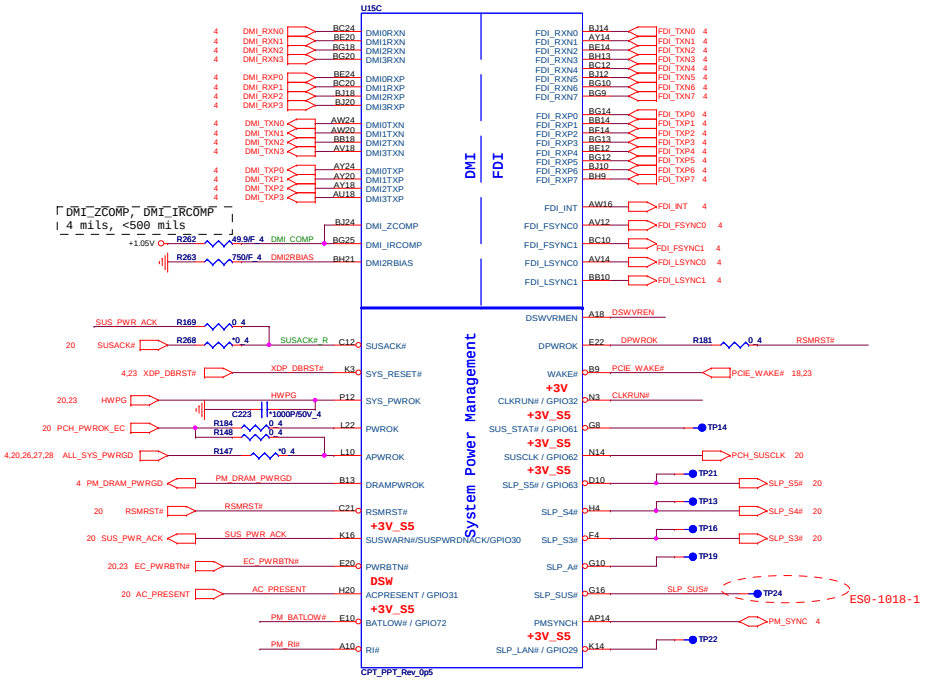
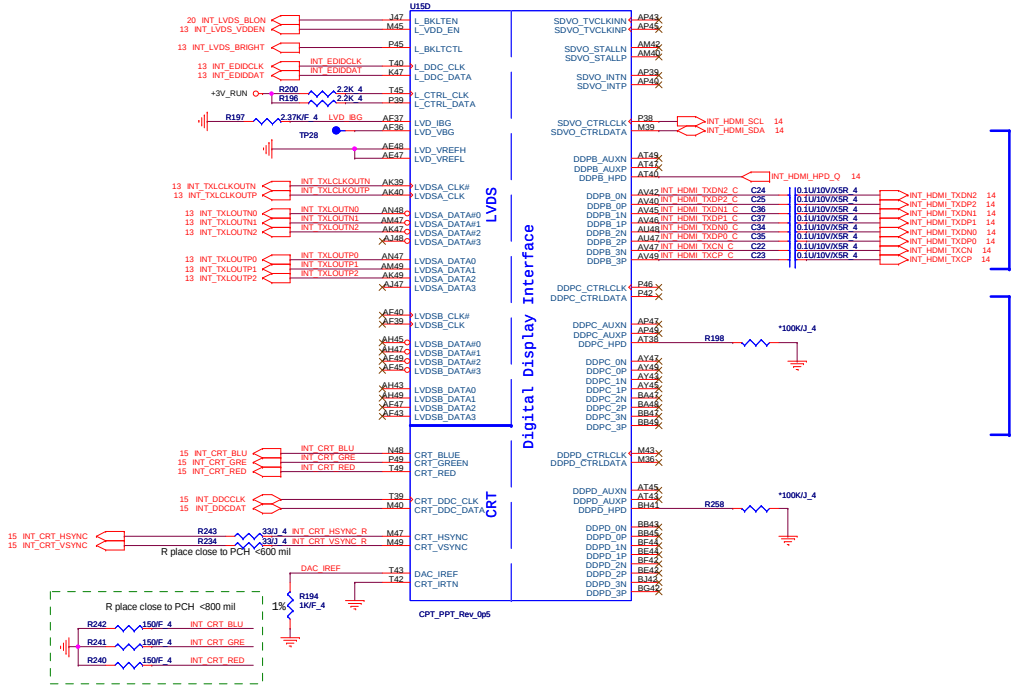
PCH 1/5 (DMI/FDI/VIDEO)

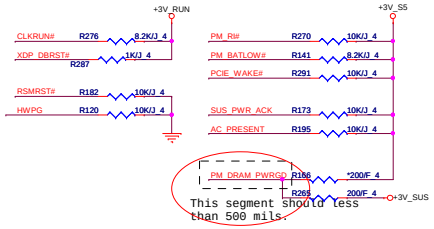
Panther Point (DMI,FDI,PM)



Panther Point (LVDS,DDI)



PCH Pull-high/low(CLG)




```
----- No Deep S4/S5, No ME ------
#SYS_RESET: Like DT reset button, NC.
#SYS_PWROK: The latest PWROK means all power in platform is stable,
After getting this signql, PCH prepares to deliver PLT_RST#.
#PWROK: All power in platform except to VCC_CORE and VCC_GFX_CORE is stable
#APWROK: Can be the same as SLP_S3 PWR stable if ME is not implemented.
#DRAMPWROK: Indicates RAM power is stable, go after the PWROK is high and
can be set time by register.
#:SUSWARN#/SUSPWRDNACK: Asserted by the PCH on behalf of the Intel ME when it
does not require the PCH Suspend well to be powered. WHAT DOES IT MEAN??
#:DPWROK: Connect to RSMRST#
#:SLP_SUS#: NC
#:SLP_A#: Can the same as or earlier than SLP_S3#, Connect to SLP_S3#
#:SLP_LAN#: Can be the same as or earlier than SLP_A#.
#:SUS_ACK#: Tell PCH that got the massage of entering Deep S4/S5 or not.
```

Quanta Computer Inc.
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Size | Document Number: PCH 1/5 (DMI/FDI/VIDEO) | Rev 1C
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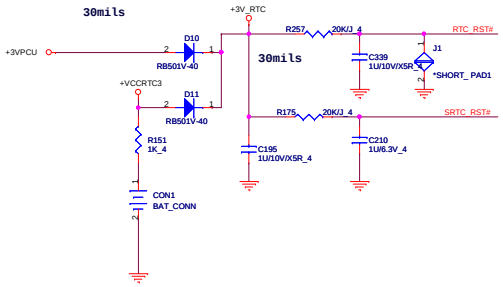
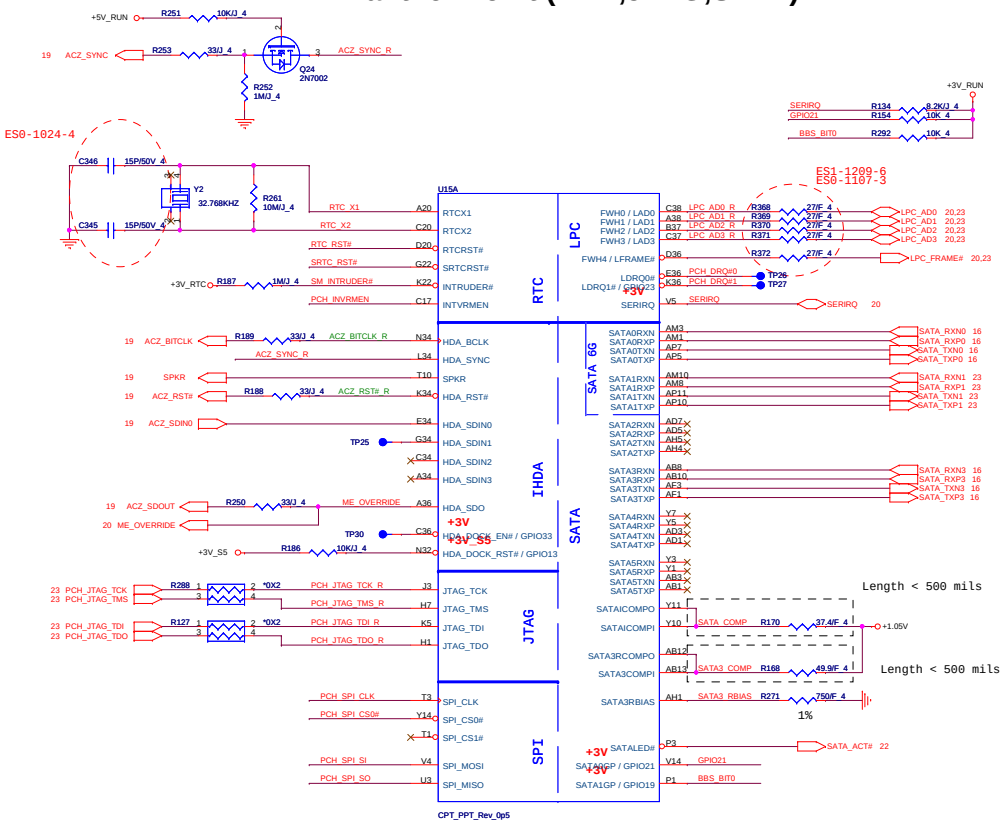
PCH 2/5(SATA/RTC/HDA/LPC)

RTC Circuitry (RTC)



Panther Point (HDA,JTAG,SATA)

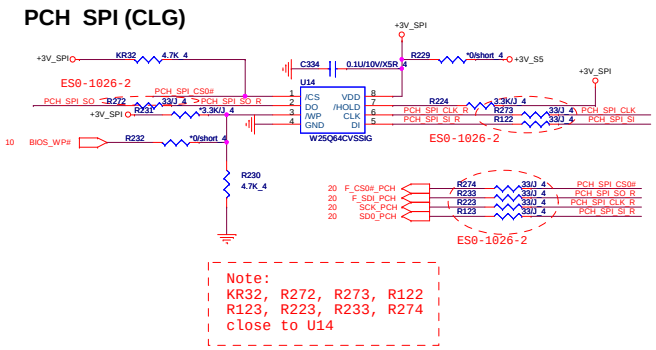


PCH Strap Table

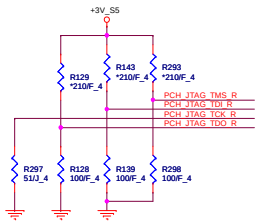
Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]**
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	PWROK	1= Override 0 = Default (weak pull-down20K)
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V

GNT1#	GNT0#	Boot Location
1	1	SPI *
0	0	LPC

PCH SPI (CLG)

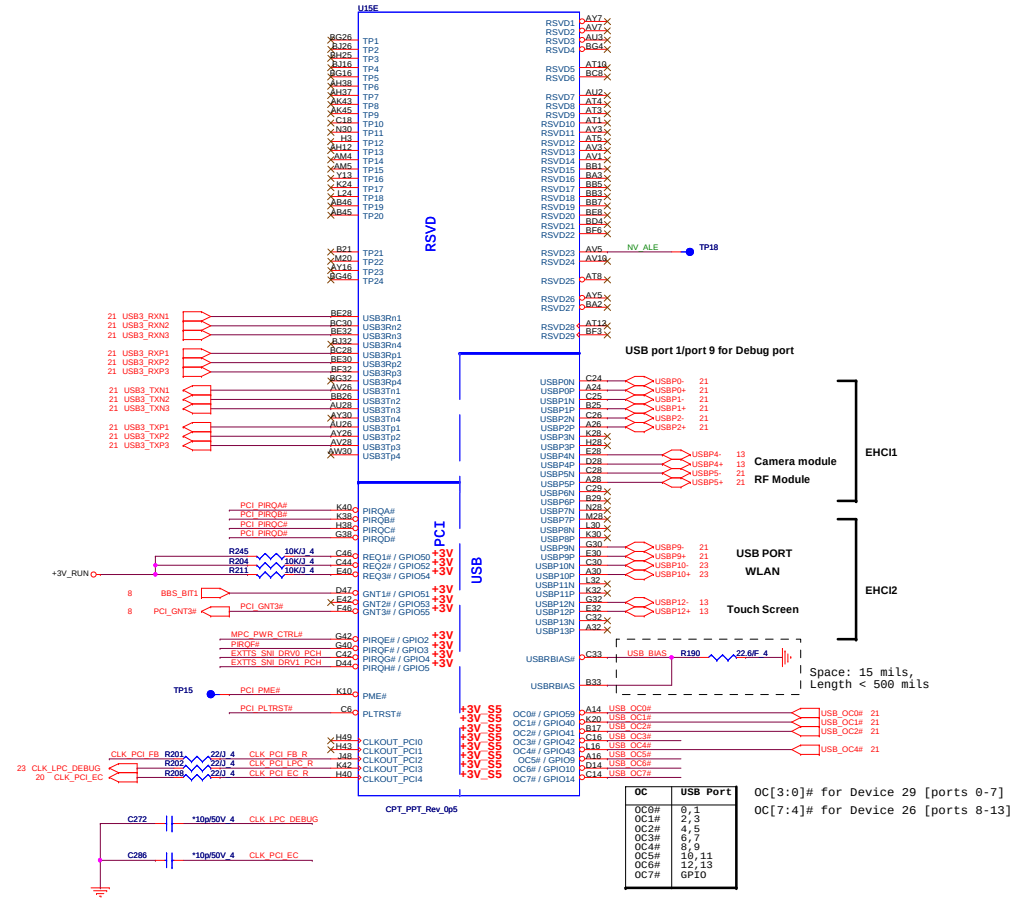


PCH JTAG Debug (CLG)



PCH 3/5(PCIE/USB/CLK/NV)

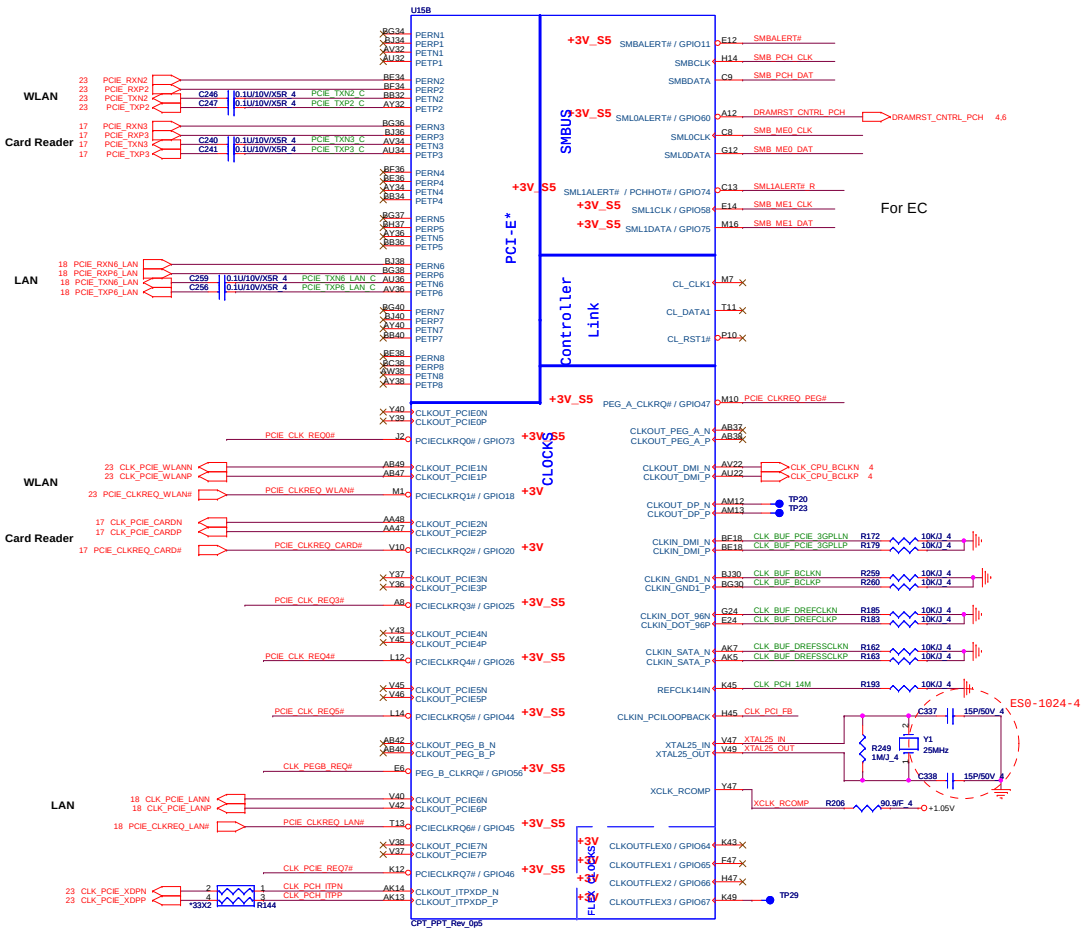
Panther Point-M (PCI,USB,NVRAM)



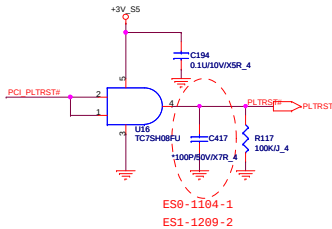
OC	USB Port
OC0#	0,1
OC1#	2,3
OC2#	4,5
OC3#	6,7
OC4#	8,9
OC5#	10,11
OC6#	12,13
OC7#	GPIO

OC[3:0]# for Device 29 [ports 0-7]
OC[7:4]# for Device 26 [ports 8-13]

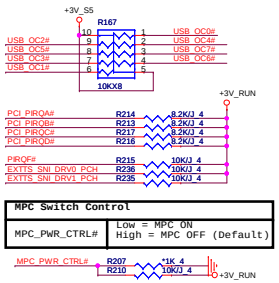
Panther Point-M (PCI-E,SMBUS,CLK)



PLTRST#(CLG)



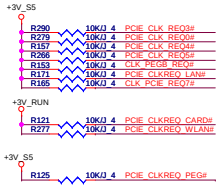
PCI/USBOC# Pull-up(CLG)



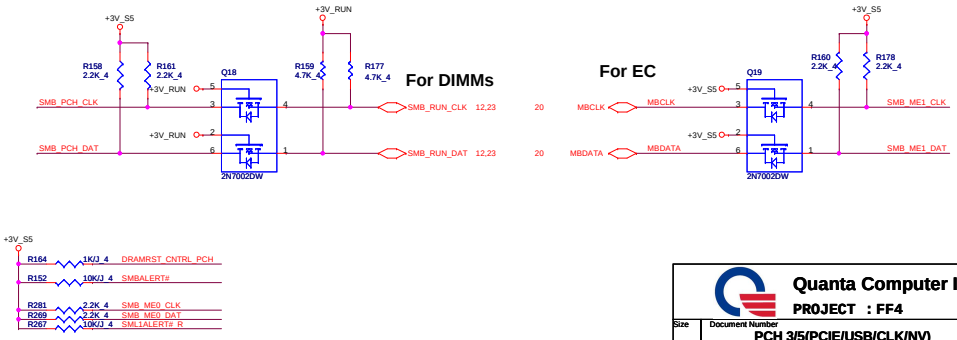
MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



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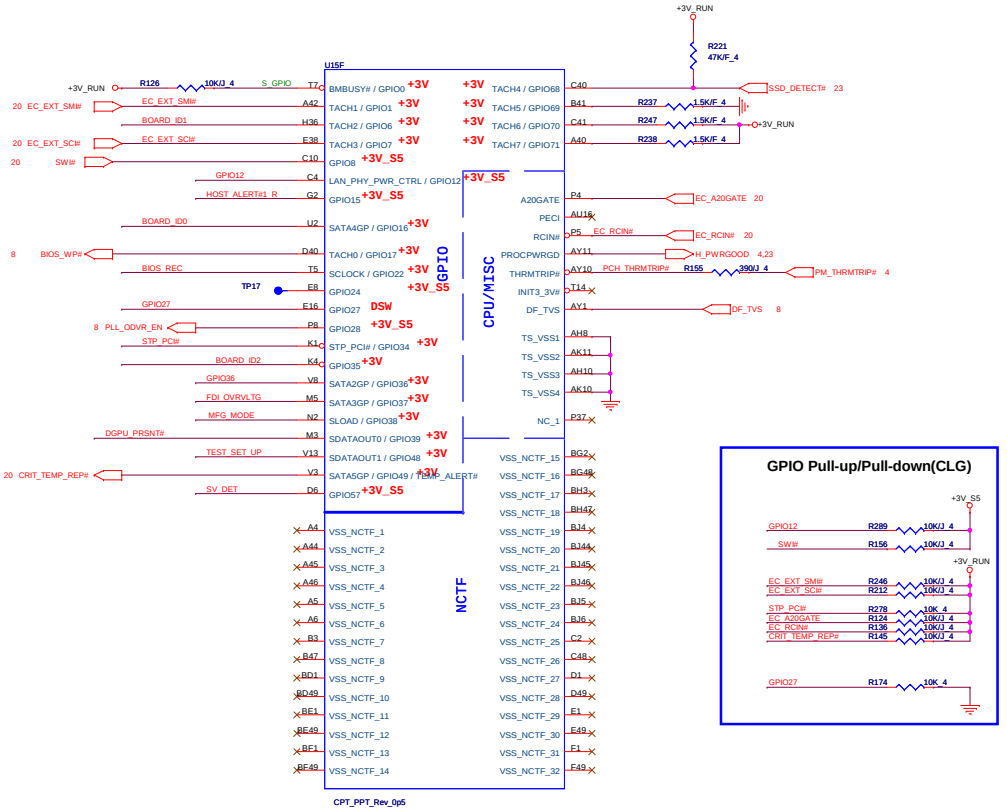
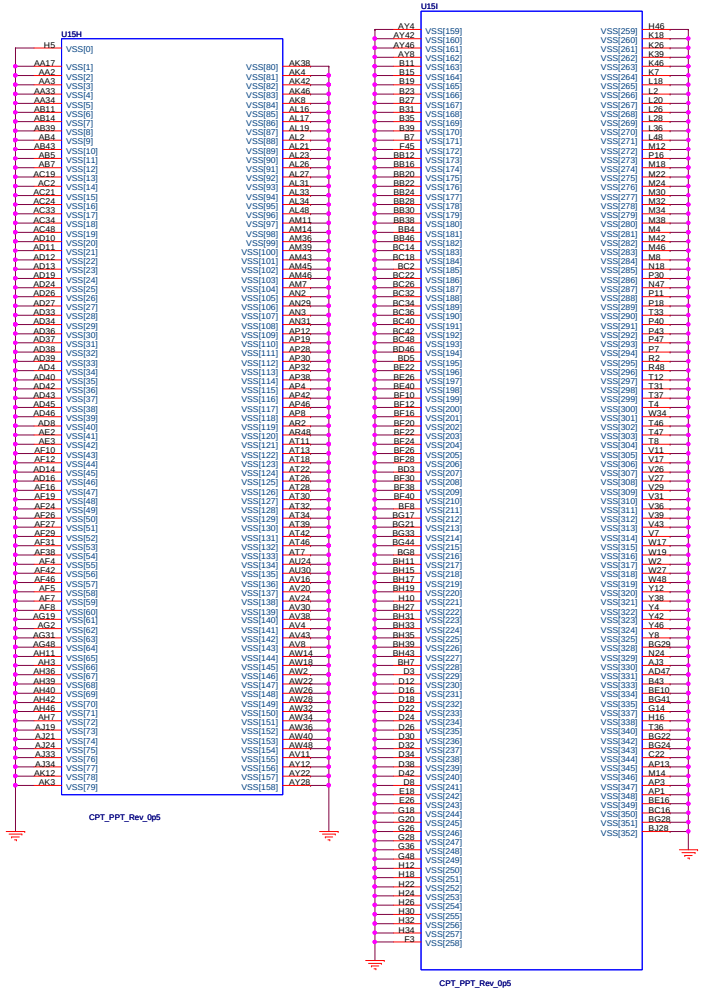
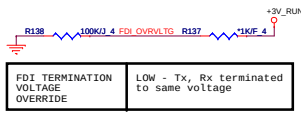
PCH 4/5(GPIO/CPU/STRAP/GND)

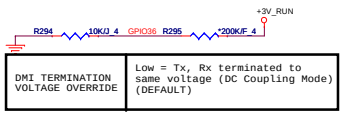
Panther Point (GPIO,VSS_NCTF,RSVD)

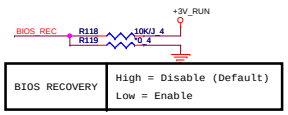


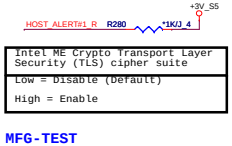
Panther Point (GND)



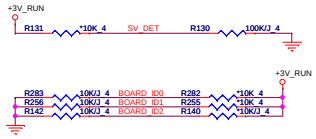




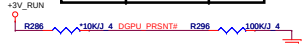


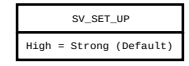


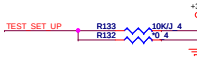
MFG-TEST



	SWITCHABLE	UMA
Stuff	R8489	R8490
No Stuff	R8490	R8489







1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : FF4

Size	Document Number	Rev
	PCH 4/5(GPIO/CPU/STRAP/GND)	1C
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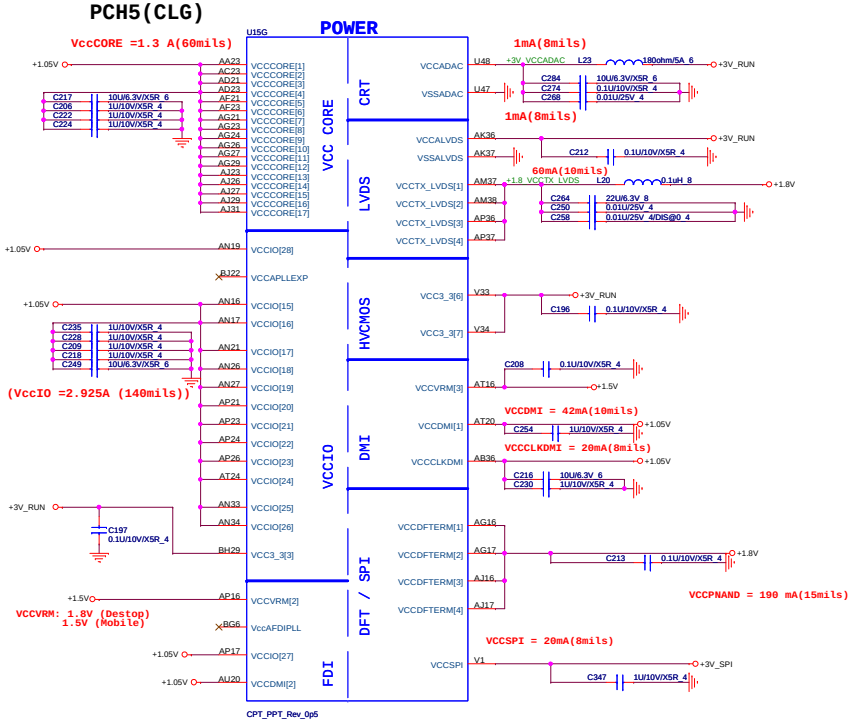
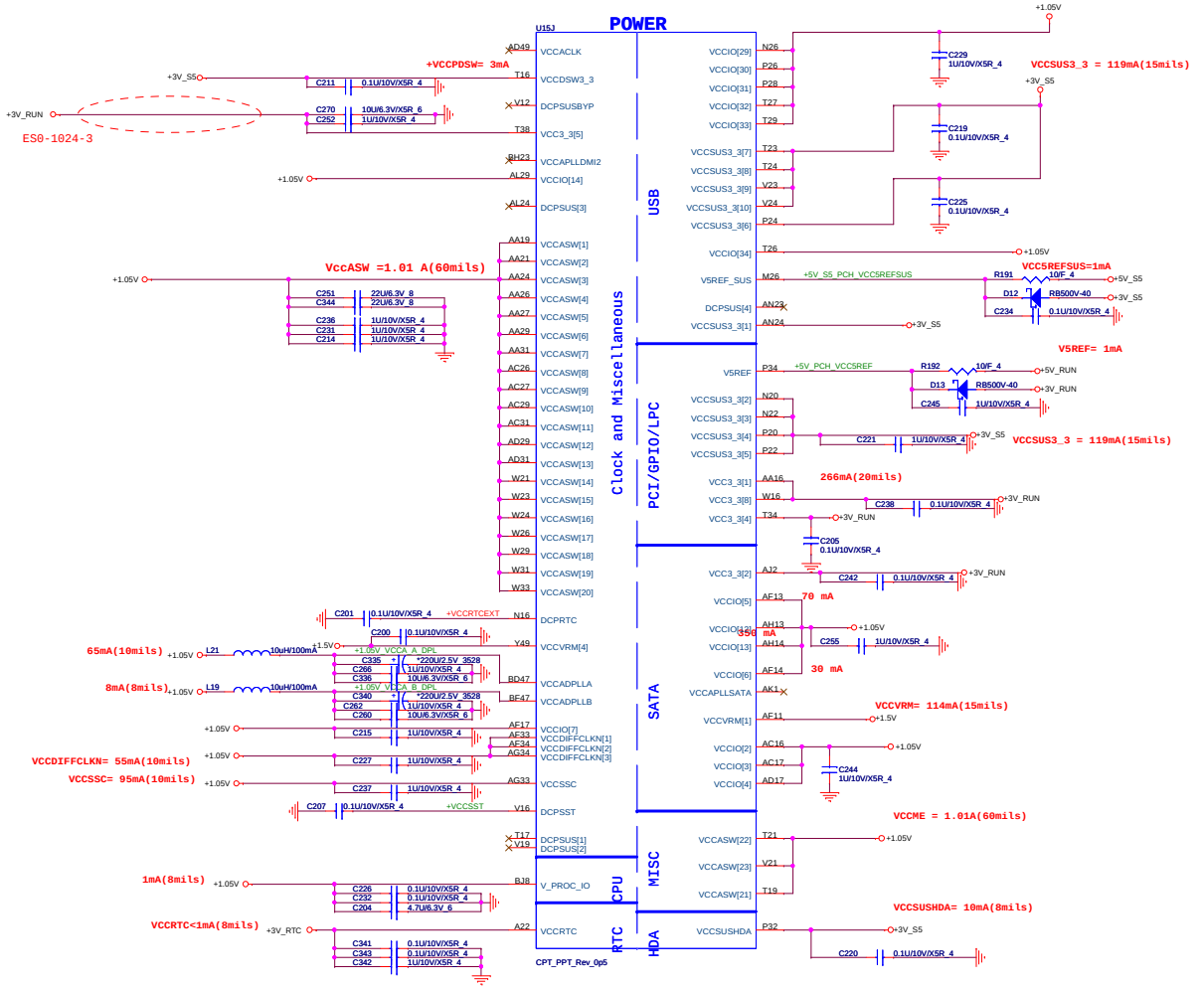
Panther Point (POWER)



Panther Point-M (POWER)



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PCH 5/5(POWER) | 1C
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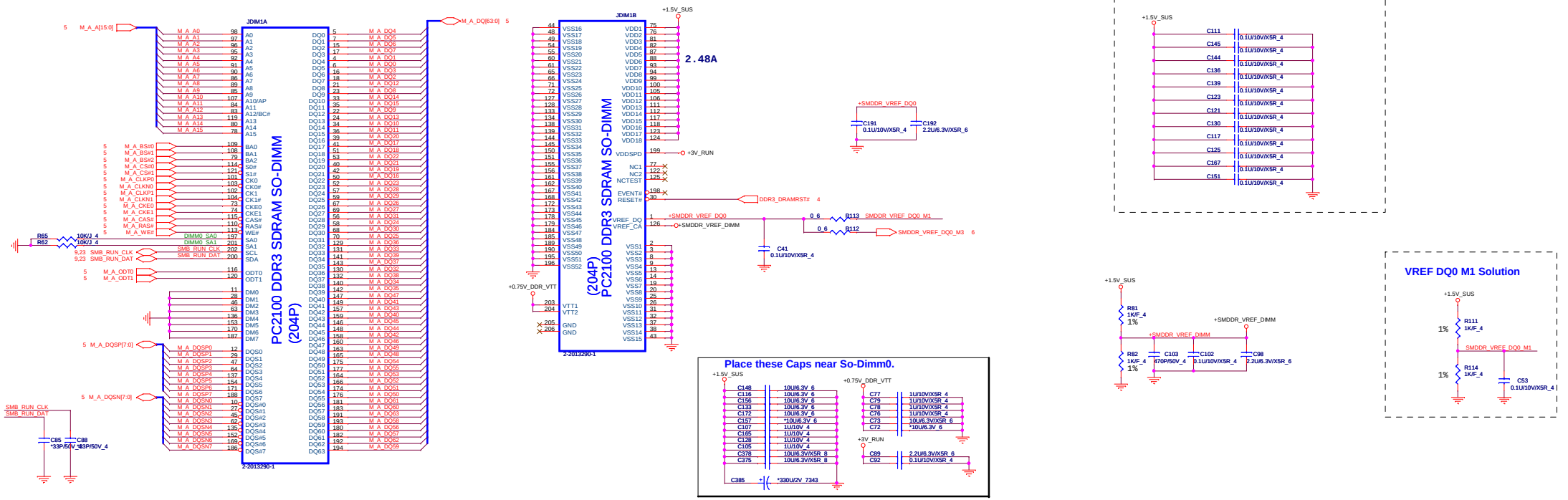
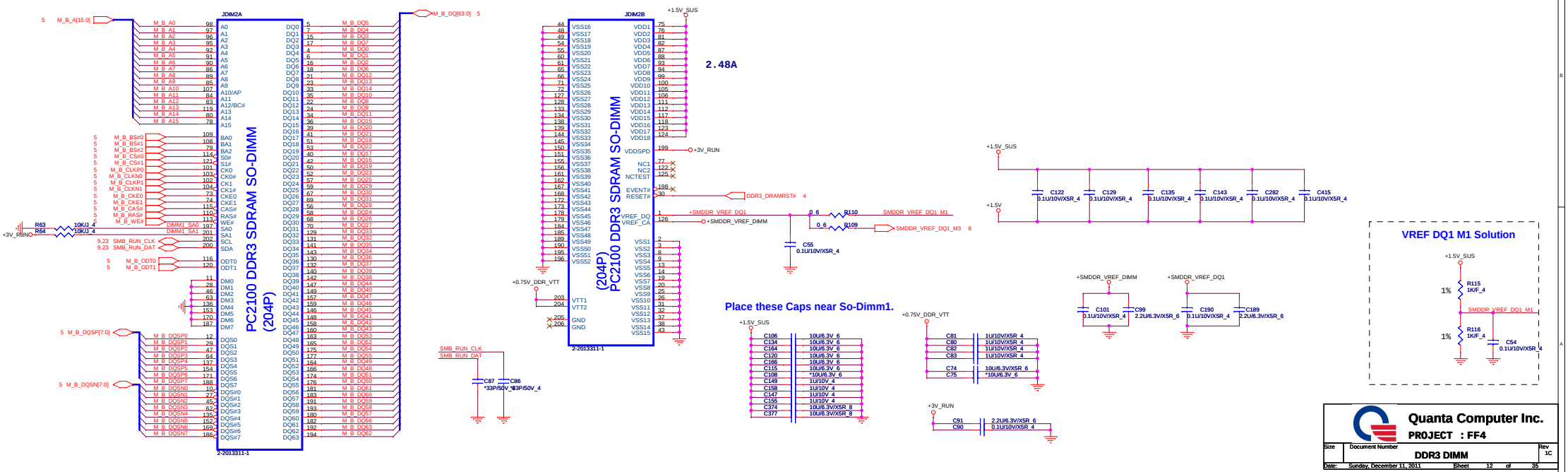
DDR3 DIMM-0-STD(8H)



DDR3 DIMM-1-STD(4H)



Quanta Computer Inc.
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	DDR3 DIMM	1C
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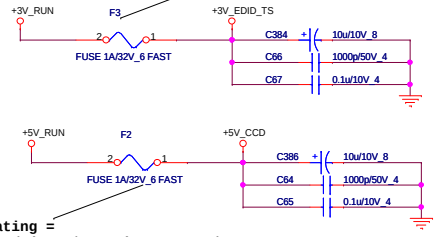
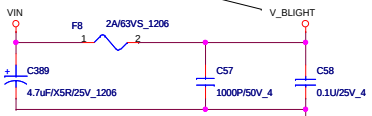
LED Panel BACKLIGHT POWER

Fuse Rating =
IR(max) / (0.75* 0.75) = 0.5A / 0.5625 = 0.889A



Fuse Rating =
IR(max) / (0.75* 0.75) = 0.17A / 0.5625 = 0.302A

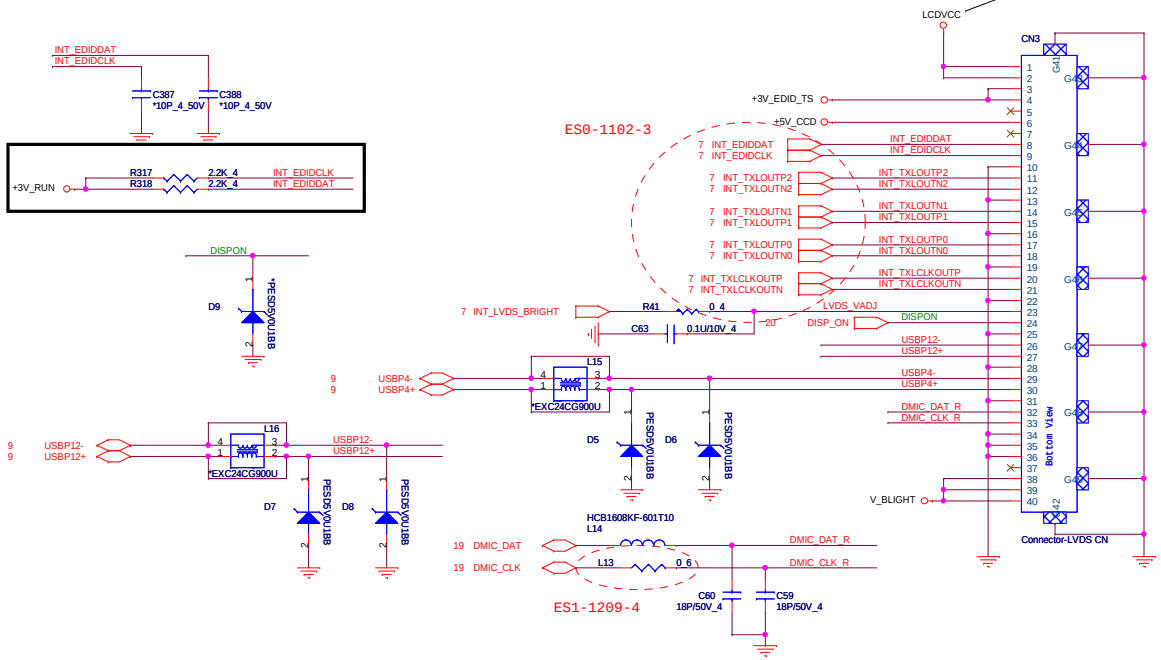
80mils



Fuse Rating =
IR(max) / (0.75* 0.75) = 0.55A / 0.5625 = 0.978A

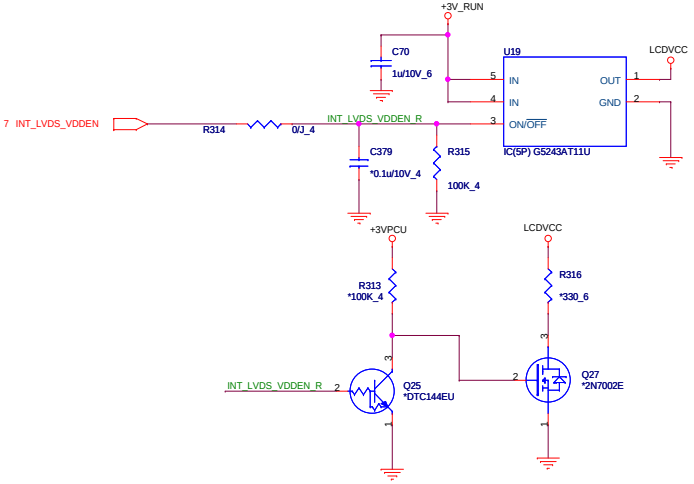
LED Panel(LVDS)

1.5A (100mils)



LED Panel POWER SWITCH(LVDS)

100mils



Quanta Computer Inc.		
PROJECT : FF4		
Size	Document Number: LCD CONN	Rev: 1C
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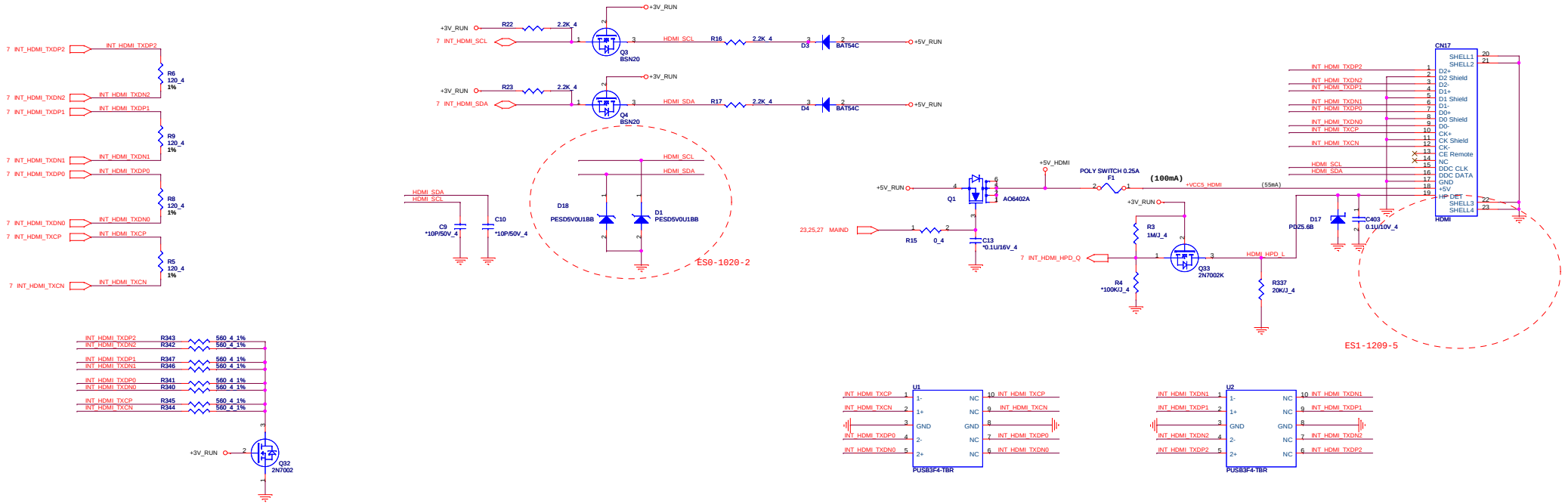
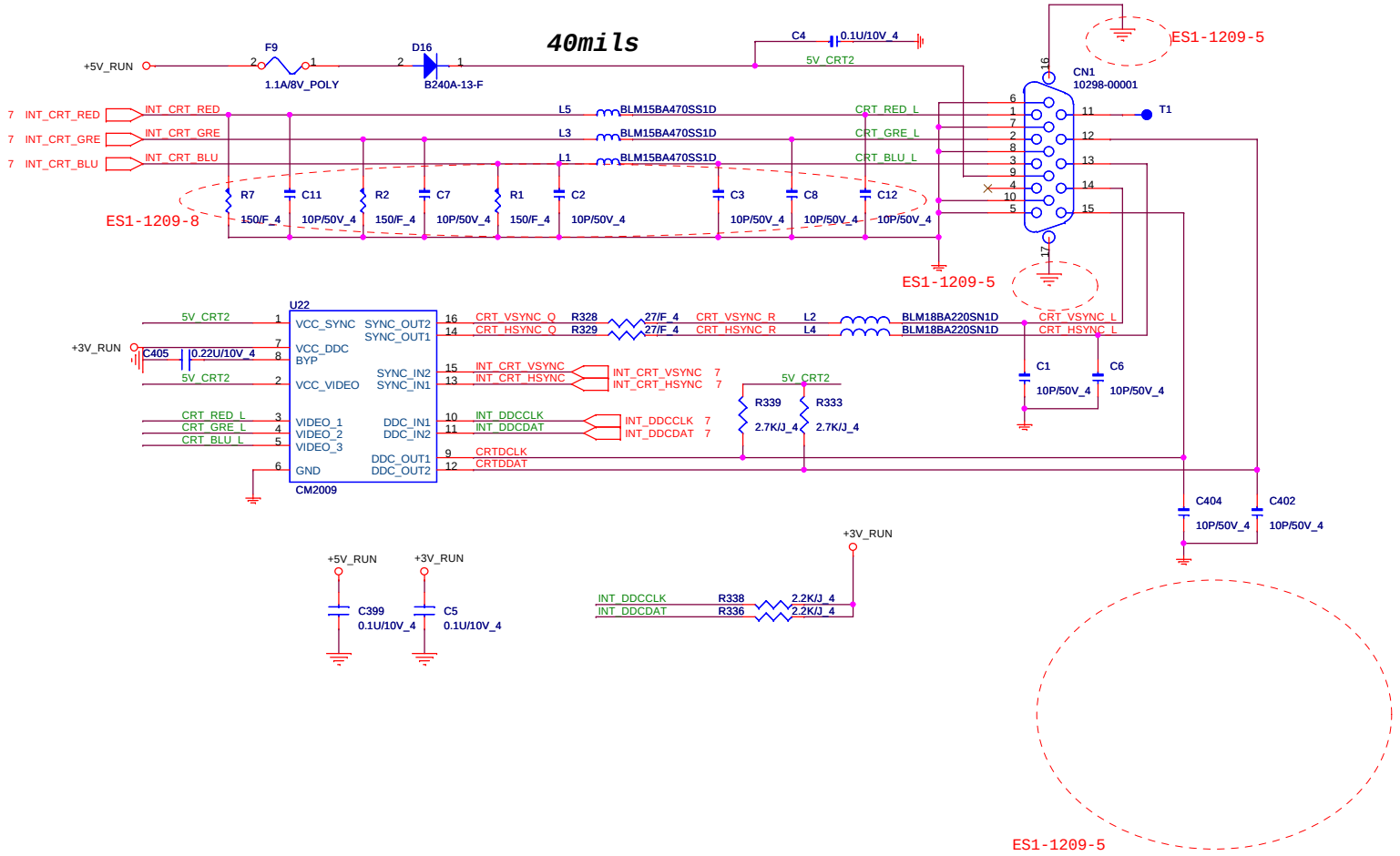
HDMI



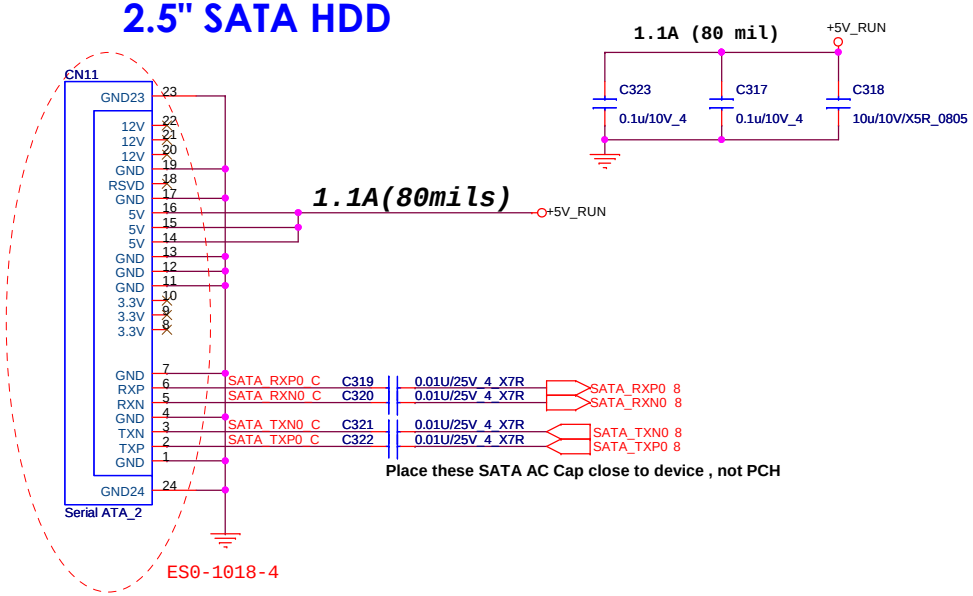
Quanta Computer Inc.			
PROJECT : FF4			
Size	Document Number		Rev
	HDMI CON		1C
Date: Sunday, December 11, 2011	Sheet 14 of 35		

CRT CONN/DDC LEVEL SHIFT

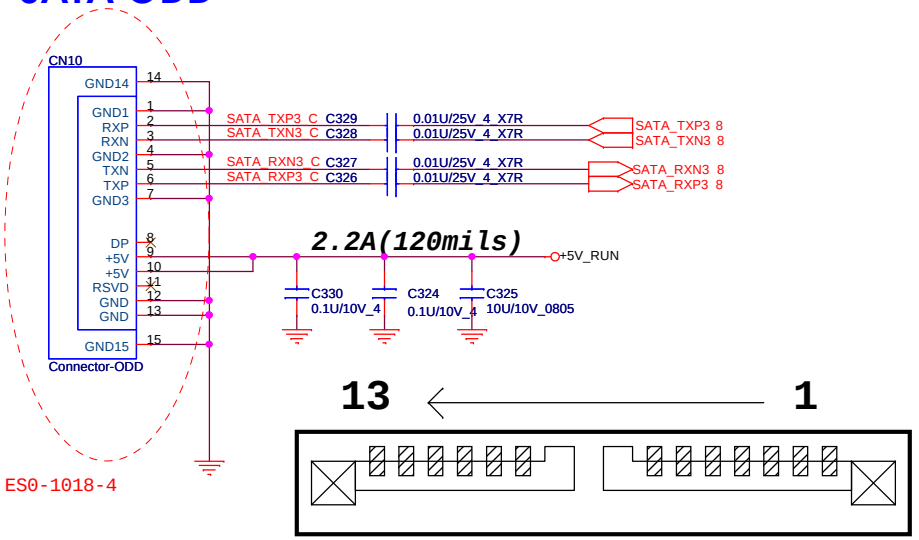


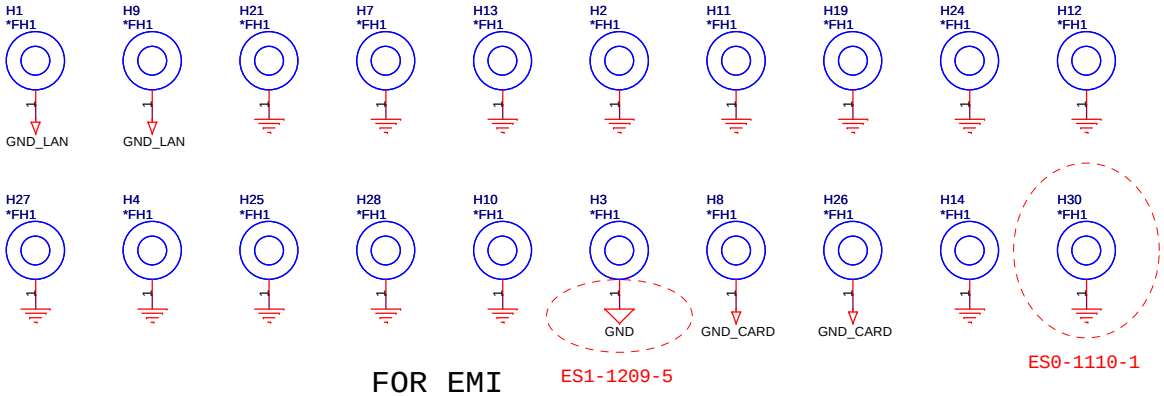
Quanta Computer Inc.			
PROJECT : FF4			
Size	Document Number		Rev
	CRT CONN		1C
Date: Sunday, December 11, 2011		Sheet 15 of 35	

2.5" SATA HDD



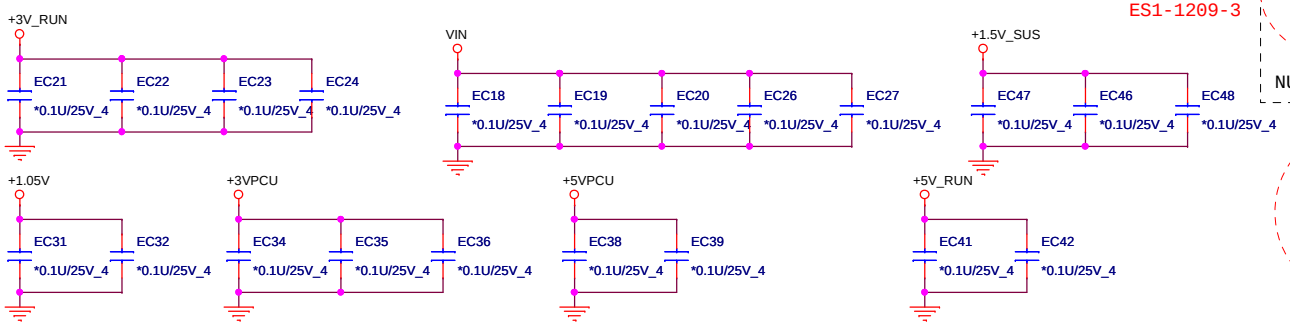
SATA ODD

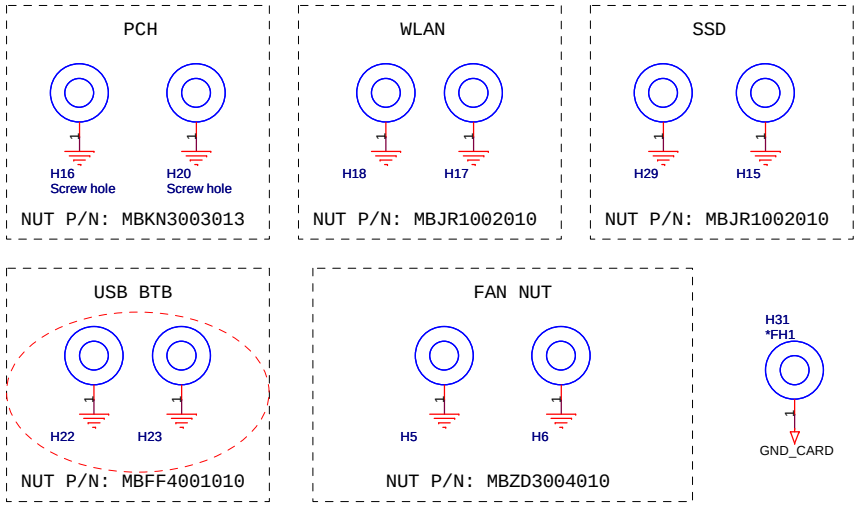




FOR EMI

ES1-1209-3





Quanta Computer Inc.

PROJECT : FF4

Size	Document Number	Rev
	HDD/ ODD/HOLE	1C

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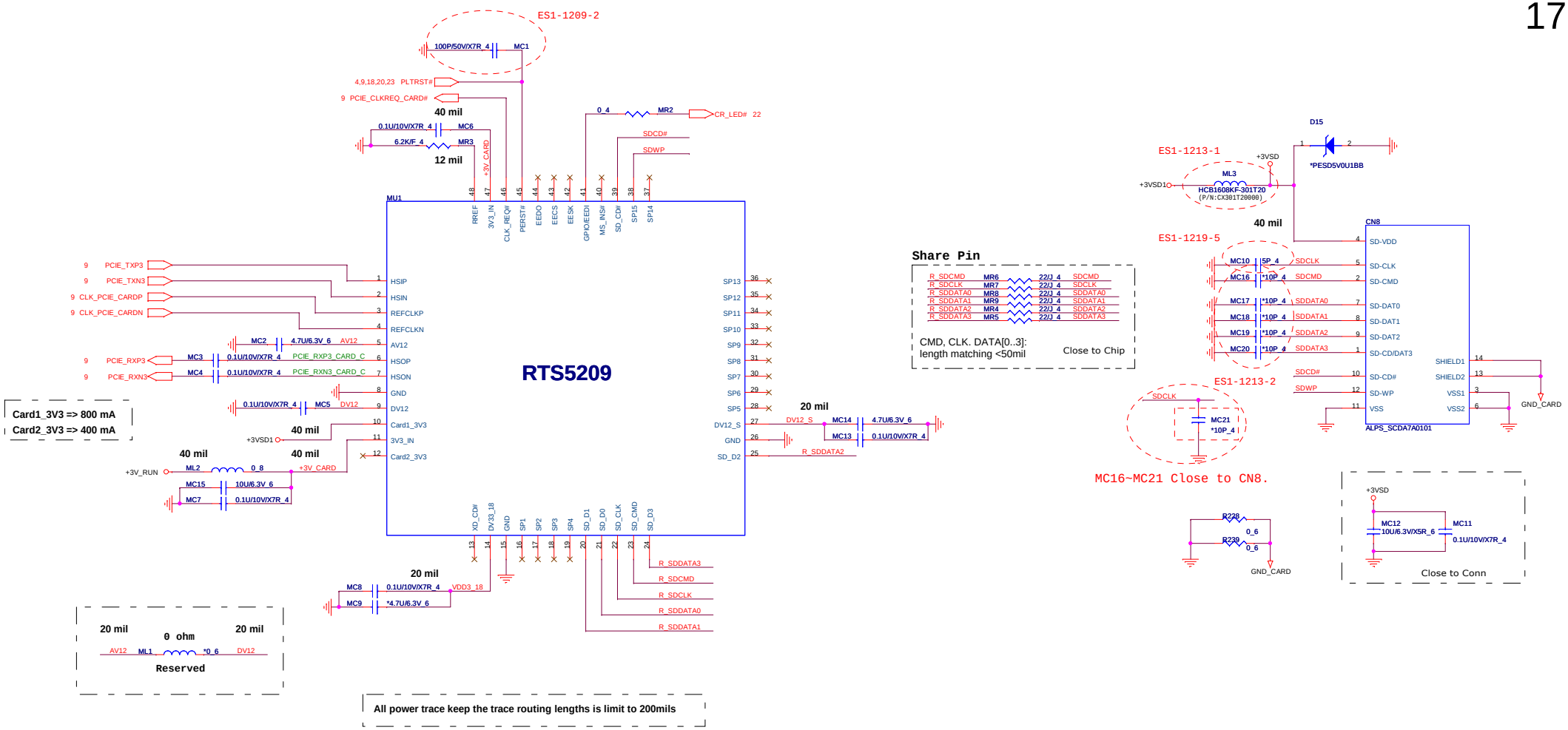
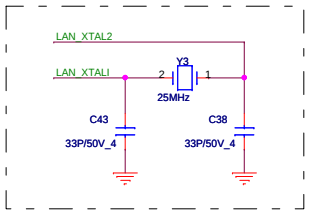
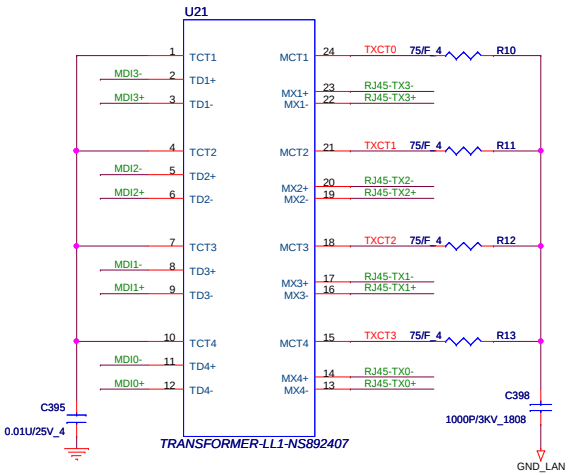


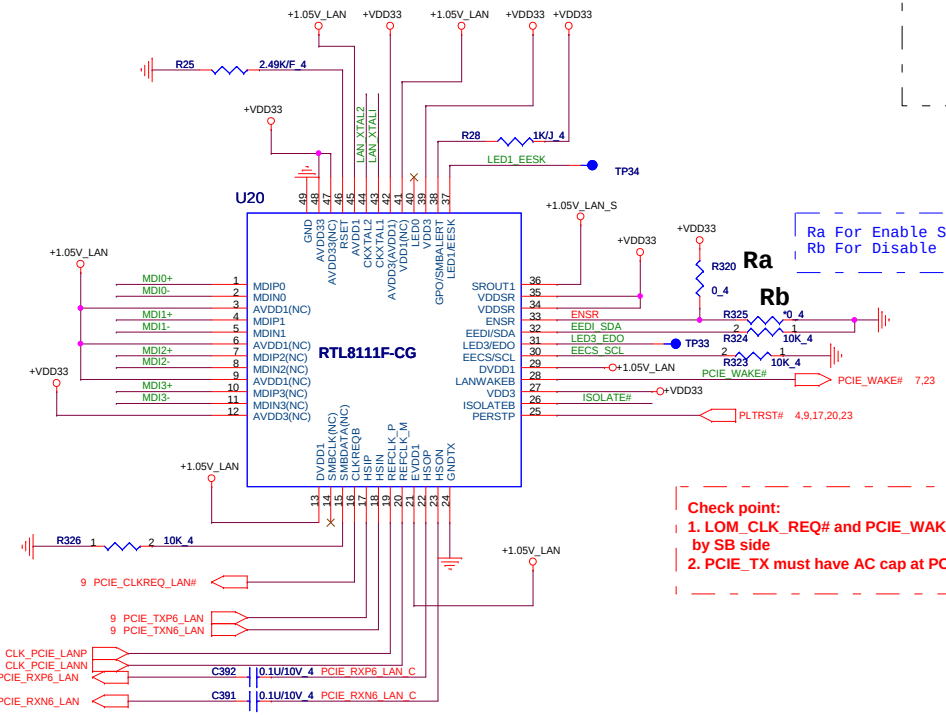
Quanta Computer Inc.		
PROJECT : FF4		
Size	Document Number	Rev
	CARD READER (RTS5209)	1C
Date: Monday, December 19, 2011	Sheet 17 of 35	

X'tal 25MHz

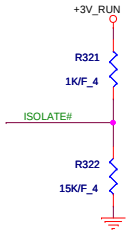


TRANSFORMER



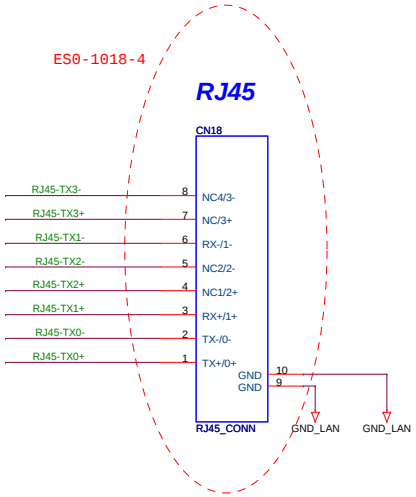


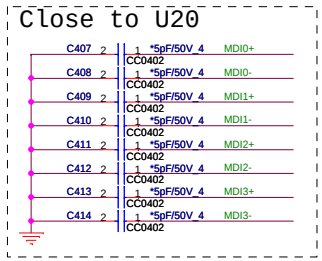
Ra For Enable Switch Regulator.
Rb For Disable Switch Regulator.

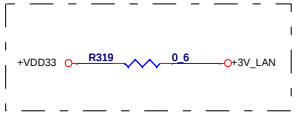


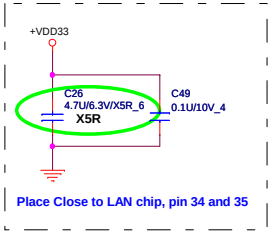
Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needsto be pull up by SB side
2. PCIE_TX must have AC cap at PCH side

RJ45



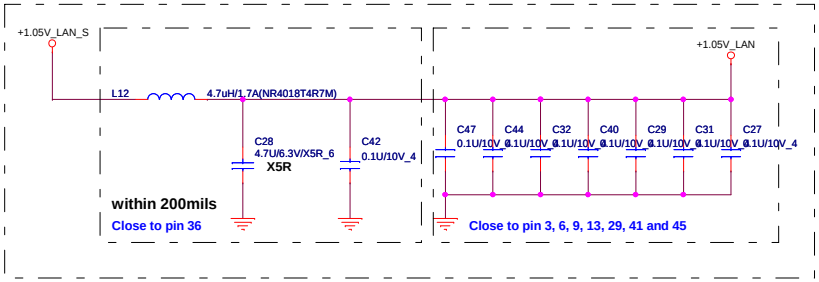


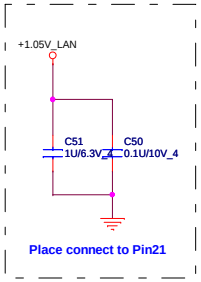


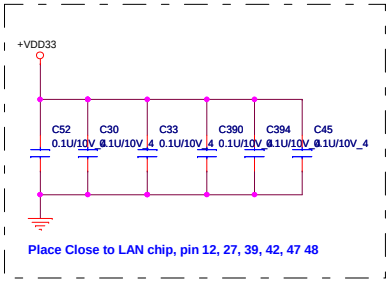


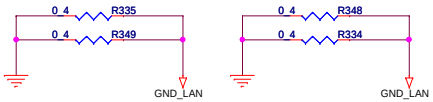
Place Close to LAN chip, pin 34 and 35

LAN Power









Quanta Computer Inc.
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	LAN_RTL8111F-CG/RJ45	1C

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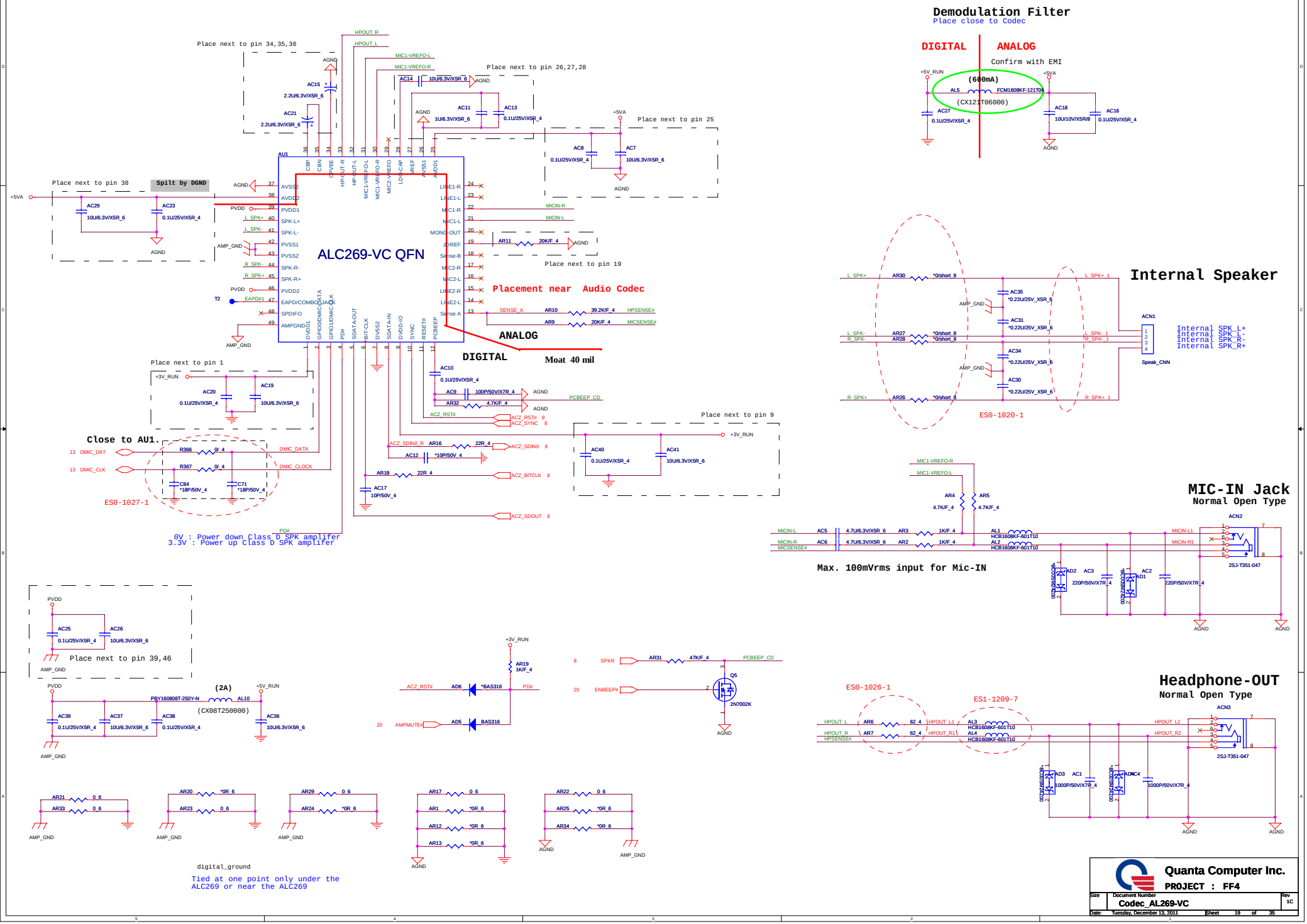
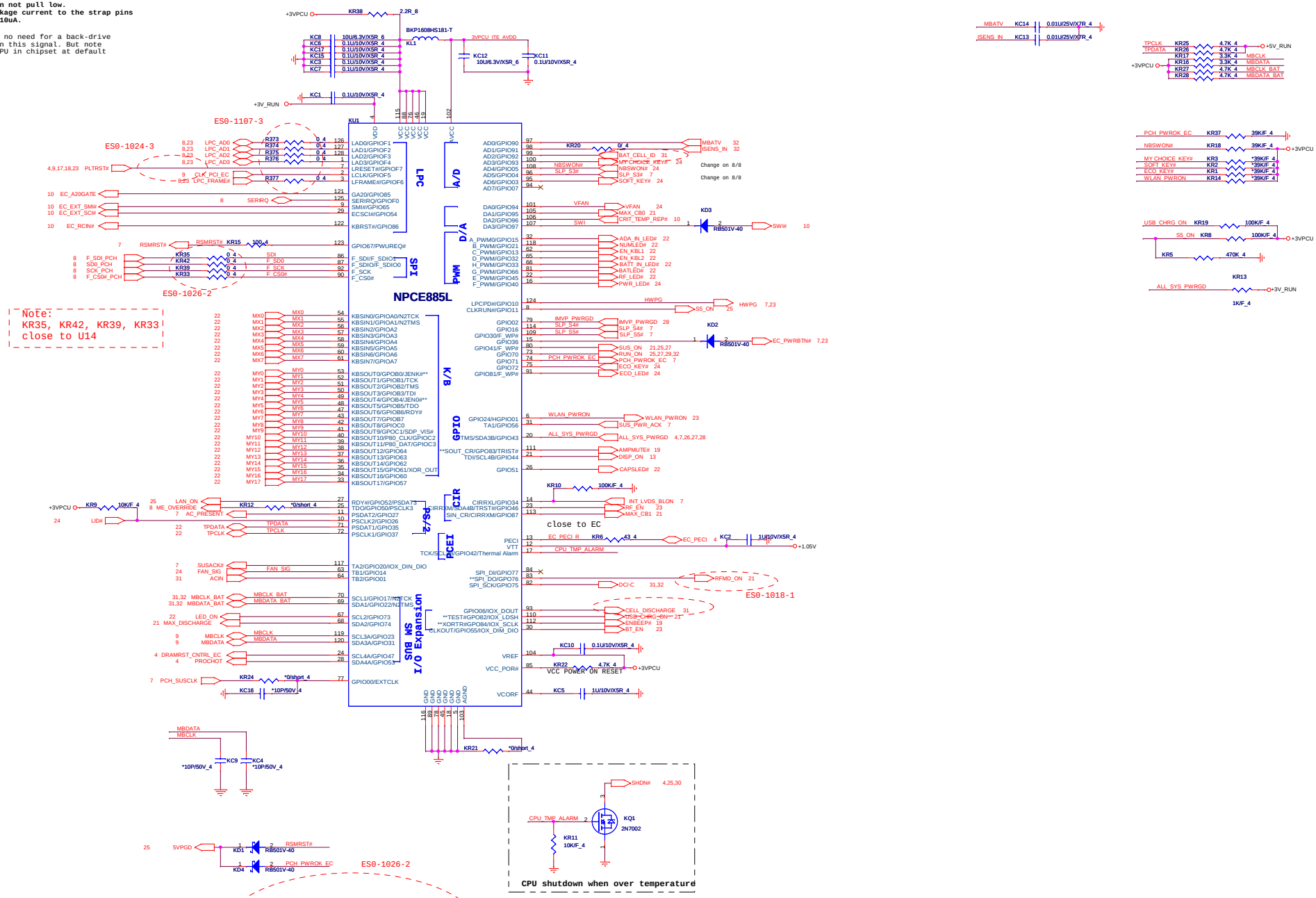

Demodulation Filter
Place close to Codec
DIGITAL
ANALOG
Confirm with EMI
(600mA)
(CX121T06000)
Internal Speaker
ES0-1020-1
MIC-IN Jack
Normal Open Type
Max. 100mVrms input for Mic-IN
Headphone-OUT
Normal Open Type
ES0-1026-1
ES1-1209-7
ALC269-VC QFN
Placement near Audio Codec
Moat 40 mil
Spilt by DGND
Close to AU1.
ES0-1027-1
0V : Power down Class D SPK amplifer
3.3V : Power up Class D SPK amplifer
digital_ground
Tied at one point only under the
ALC269 or near the ALC269
Quanta Computer Inc.
PROJECT : FF4
Codec_AL269-VC
Tuesday, December 13, 2011

KBC-WPCE791L/WPCE795L

**** Straping Pin,Can not pull low.**
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default



Quanta Computer Inc.
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Size | Document Number | Rev
EC-NPCE885L | 1C
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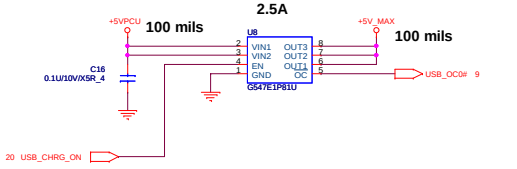
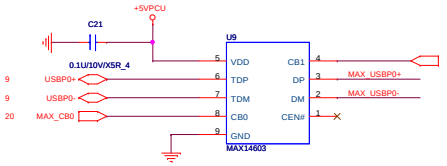
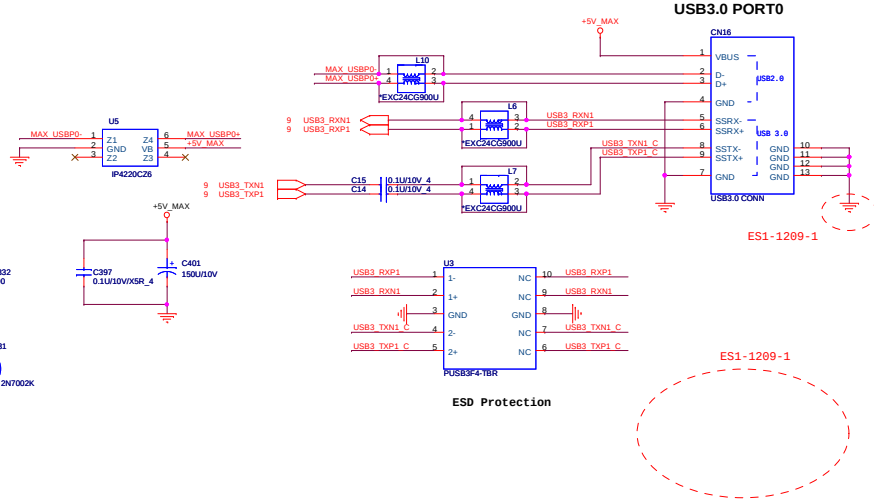
USB CHARGER







USB Charger Enable

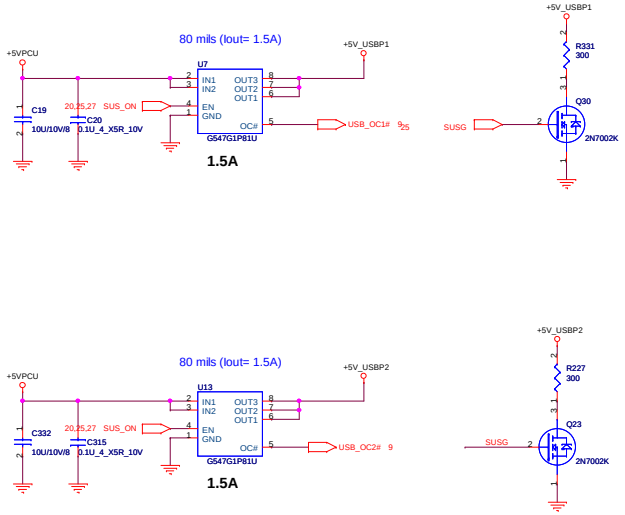
Power State	Mode	CB0	CB1	USB_CHRG_ON	MAX_DISCHARGE	Power Source
S0	PM	1	0	1->0->1	0->1->0	AC or DC
S3	AM	0	0	1->0->1	0->1->0	AC*1
S4/S5	AM	0	0	1->0->1	0->1->0	AC*1
S3	PM	1	0	0	1	DC
S4/S5	PM	1	0	0	1	DC
G3->S5						Base on AC or DC

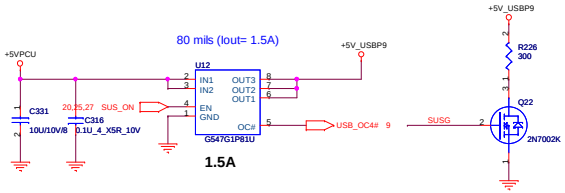
USB Charger Disable

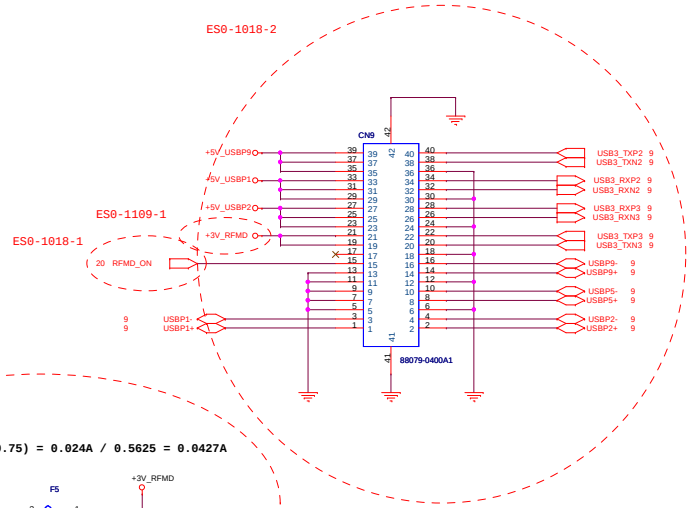
Power State	Mode	CB0	CB1	USB_CHRG_ON	MAX_DISCHARGE	Power Source
S0	PM	1	0	1	0	AC or DC
S3	PM	1	0	1	0	AC
S4/S5	PM	1	0	0	1	AC
S3	PM	1	0	1	0	DC
S4/S5	PM	1	0	0	1	DC
G3->S5						Base on AC or DC

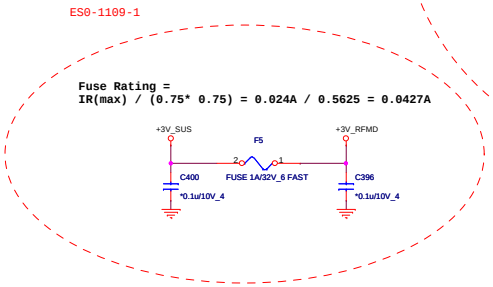
*1 : Discharge min. 700ms

CB0	CB1	Mode	Status
0	0	AM	Auto Detection Charger Mode
0	1	FM	Force Dedicated Charger Mode: DP/DM shorted
1	0	PM	USB Pass-Through Mode: DP/DM connected to TDP/TDM
1	1	CM	USB Pass-Through Mode with CDP Emulation: auto connects DP/DM to TDP/TDM depending on CDP status









Quanta Computer Inc.
PROJECT : FF4

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	USB3.0	1C

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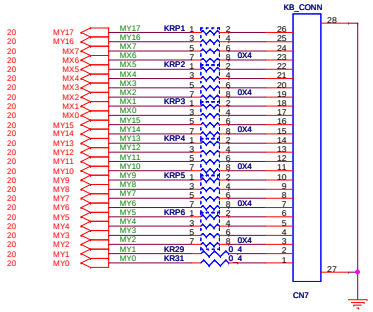
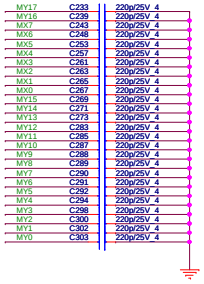
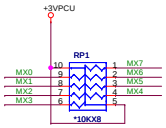
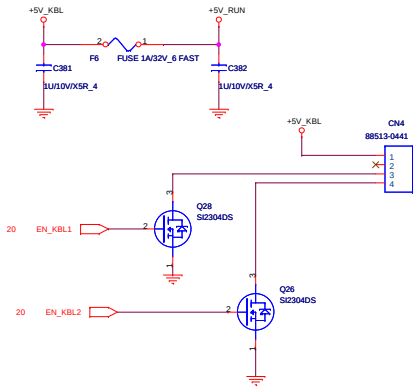
Keyboard(KBC)





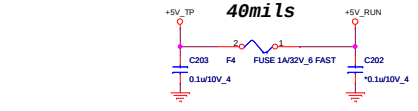


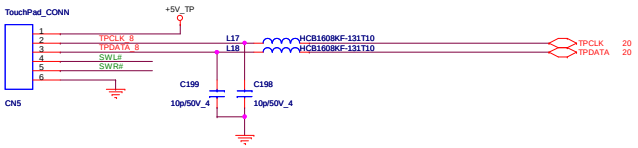
Fuse Rating =
IR(max) / (0.75* 0.75) = 0.29A / 0.5625 = 515.6mA



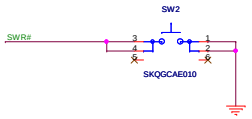
Touch Pad D/B (TPD)

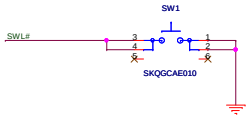
Fuse Rating =
IR(max) / (0.75* 0.75) = 0.006A / 0.5625 = 0.011A





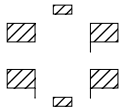
Right Side

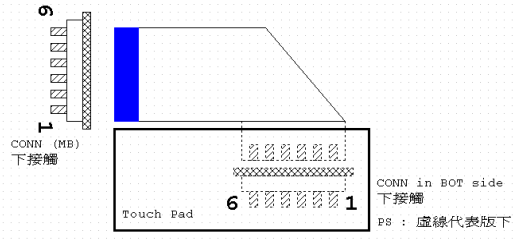




Left Side

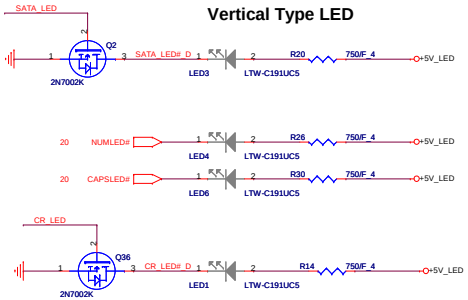
SW Footprint



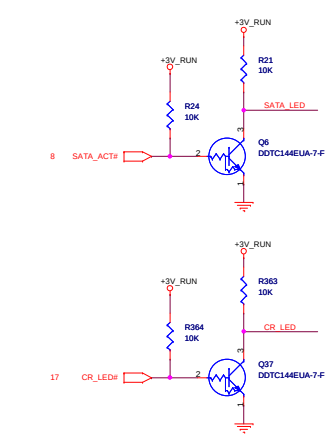


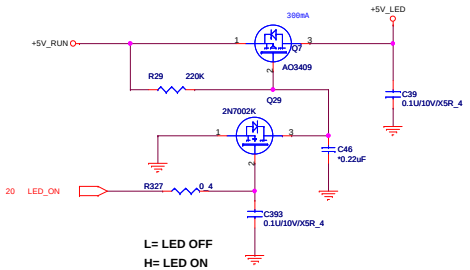
Rear Side

Vertical Type LED



Card LED HDD/ODD NUM Lock CAP LOCK

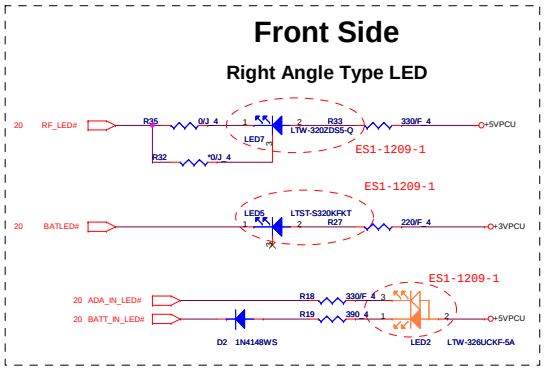




L= LED OFF
H= LED ON

Front Side

Right Angle Type LED



Power state CHARGE RF

	VF MIN	VF MAX	A
Amber LED	2.0V	2.4V	4.09 mA / 5.91 mA

AMBER (3.3- 2.0)V / 220Ω = 5.909mA
(3.3- 2.4)V / 510 Ω = 4.09 mA

	VF MIN	VF MAX	A
White LED	2.7V	3.15V	2.47mA / 3.1 mA

(5- 2.7)V / 750 Ω = 3.1 mA
(5 - 3.15)V / 750Ω = 2.47 mA

	VF MIN	VF MAX	A
White LED	2.7V	3.15V	5.61mA / 6.97 mA

(5- 2.7)V / 330 Ω = 6.97 mA
(5 - 3.15)V / 330 Ω = 5.61 mA

	VF MIN	VF MAX	A
LED W	2.9 V	3.2 V	5.45 mV / 6.36mA
LED A	2.0 V	2.4 V	4.8 mA / 5.8 mV

WHITE (5 - 3.2)V / 330Ω = 5.45 mA
(5 - 2.9)V / 330 Ω = 6.36mA

AMBER (5 - 2.0 - 0.7)V / 390 Ω = 5.8 mA
(5 - 2.4 - 0.7)V / 390 Ω = 4.8 mA

Quanta Computer Inc.
PROJECT : FF4

Size	Document Number	Rev
	KB/TP/LED	1C

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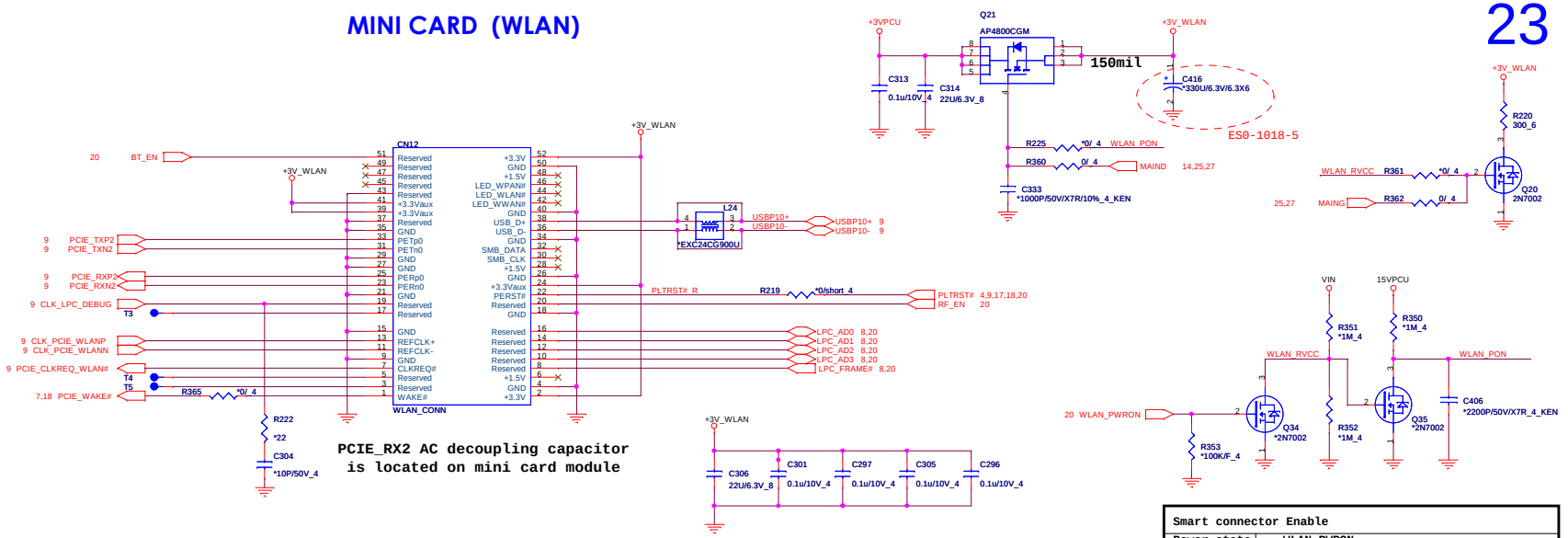
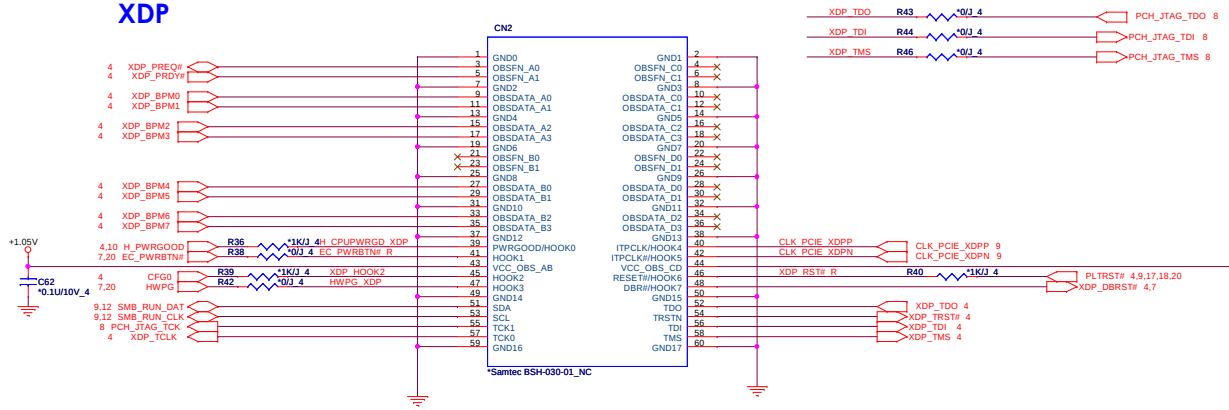
MINI CARD (WLAN)



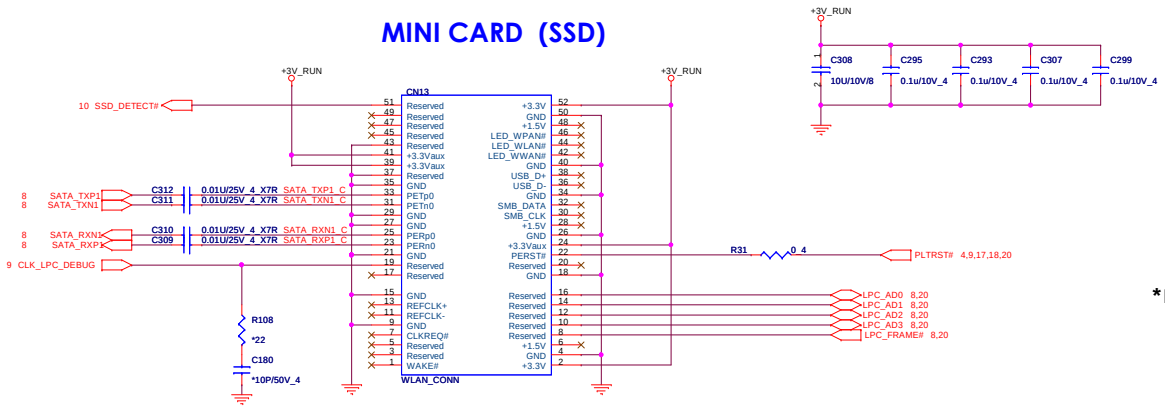
PCIE_RX2 AC decoupling capacitor is located on mini card module

Smart connector Enable	
Power state	WLAN_PWRON
S0	1
S3	1
S4/S5	0
Smart connector Disable	
Power state	WLAN_PWRON
S0	1
S3	0
S4/S5	0

XDP



MINI CARD (SSD)



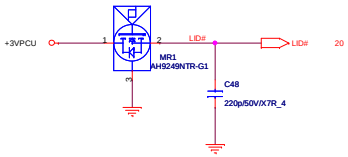
Signal	Pin
TX+	23
TX-	25
RX+	33
RX-	31
Present	51
Power	2, 24, 39, 41, 52
GND	4, 9, 15, 18, 21, 26, 27, 29, 34, 35, 37, 40, 43, 50

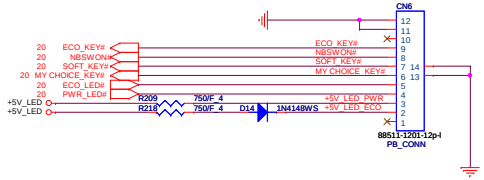
***PCIE interface is based on SSD side.**

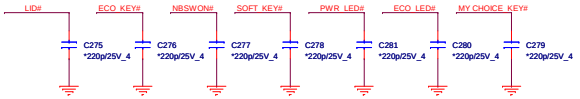
Quanta Computer Inc.
PROJECT : FF4

Size	Document Number	Rev
	MINI CARD(WLAN)	1C
Date: Sunday, December 11, 2011	Sheet 23 of 35	

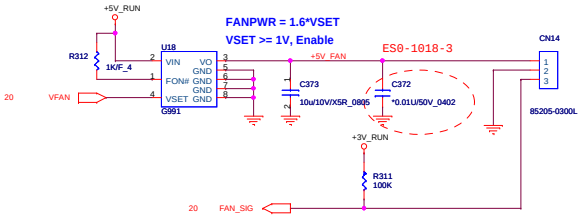
Magnetic Lid Switch



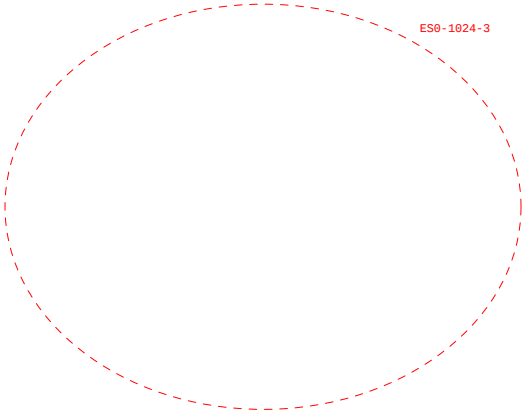




CPU FAN CTRL



CPU Thermal Sensor



Quanta Computer Inc.		
PROJECT : FF4		
Size	Document Number: SW CON/FAN/HW THRM PROTEC	Rev: 1C
Date: Tuesday, December 20, 2011	Sheet 24 of 35	

3.3V & 5V

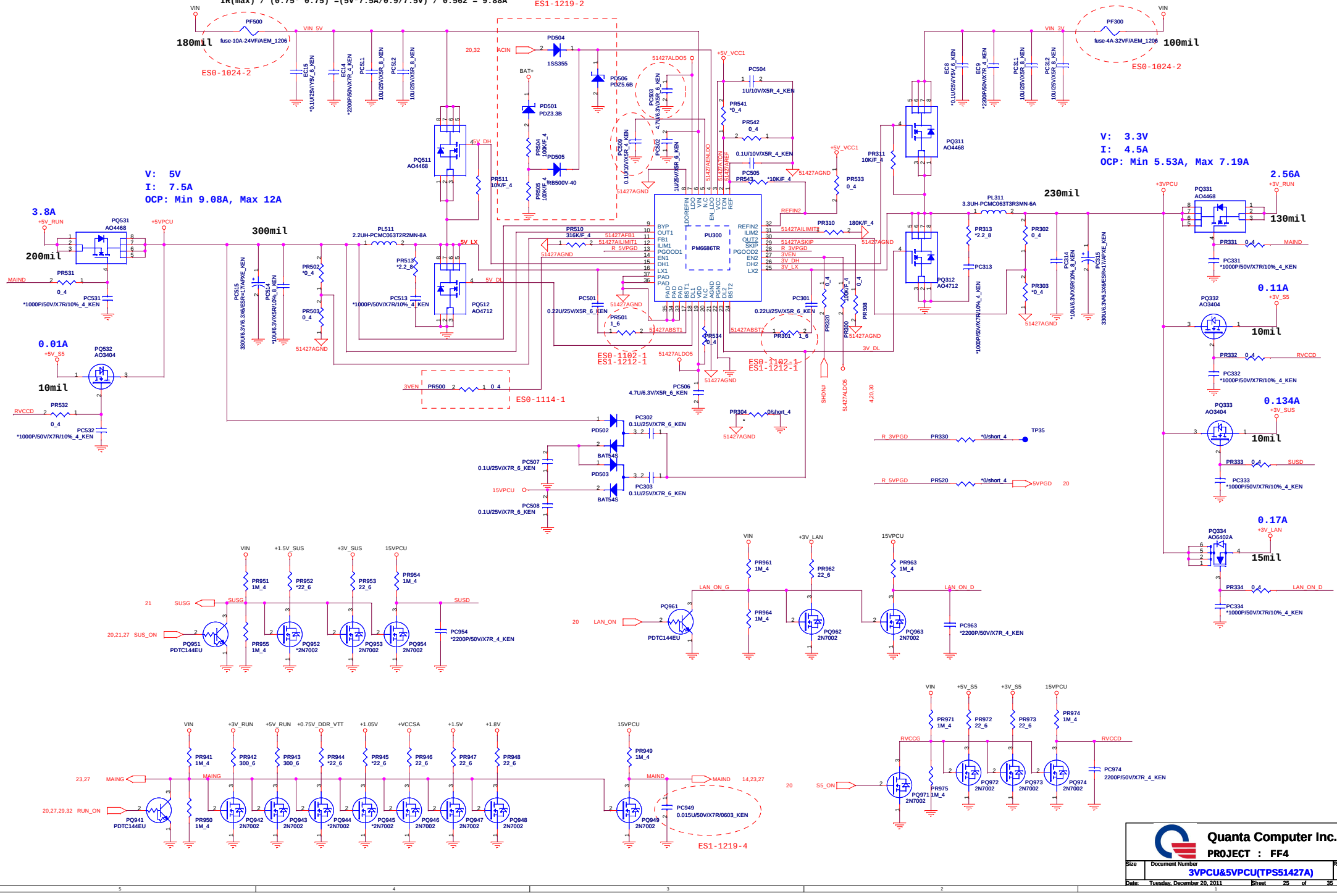
Fuse Rating =
IR(max) / (0.75* 0.75) =(5V*7.5A/0.9/7.5V) / 0.562 = 9.88A

Fuse Rating =
IR(max) / (0.75* 0.75) =(3.3V*4.5A/0.9/7.5V) / 0.5625 = 3.91A

V: 5V
I: 7.5A
OCP: Min 9.08A, Max 12A

V: 3.3V
I: 4.5A
OCP: Min 5.53A, Max 7.19A

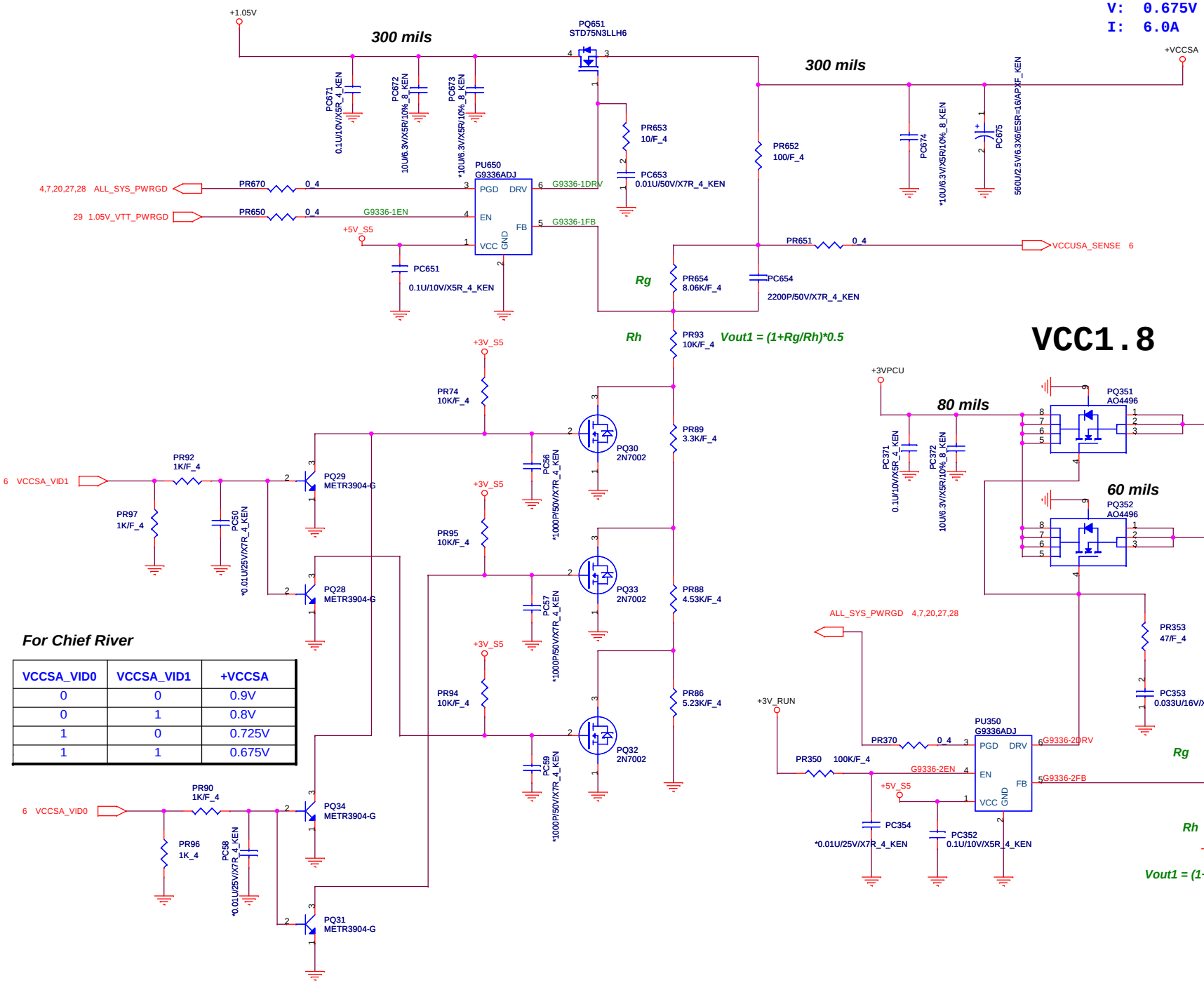
PM6686TR



Quanta Computer Inc.	
PROJECT : FF4	
Size	Document Number: 3VPCU&5VPCU(TPS51427A) Rev: 1C
Date: Tuesday, December 20, 2011	Sheet 25 of 35

+VCCSA

V: 0.675V to 0.9V
I: 6.0A



For Chief River

VCCSA_VID0	VCCSA_VID1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCC1.8

V: 1.8V
I: 1.45A

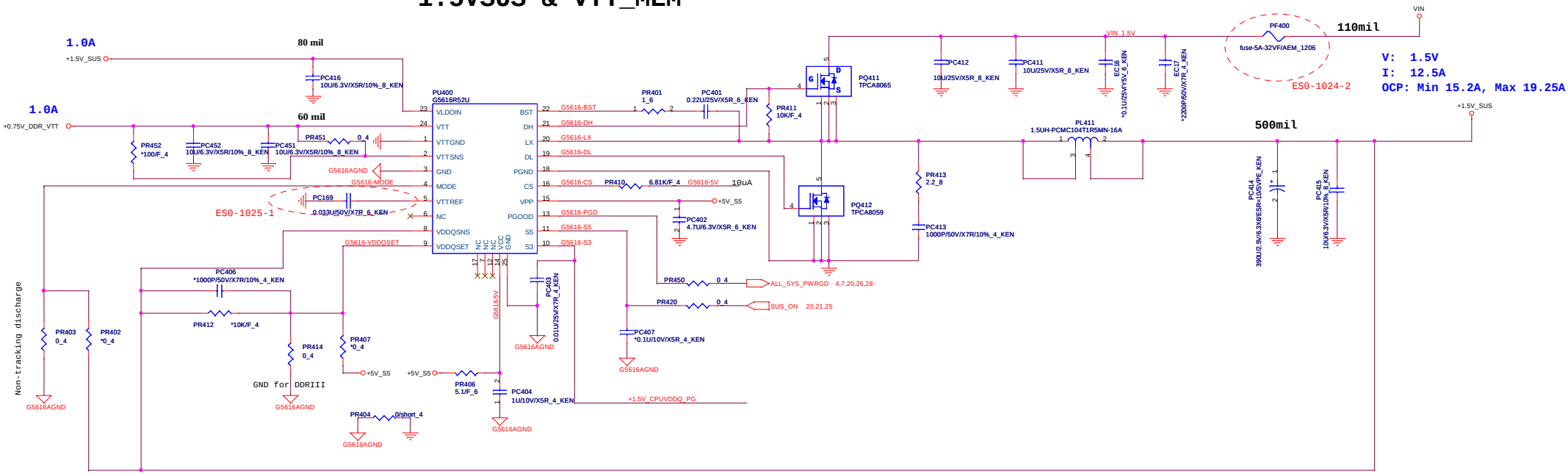
Quanta Computer Inc.
PROJECT : FF4

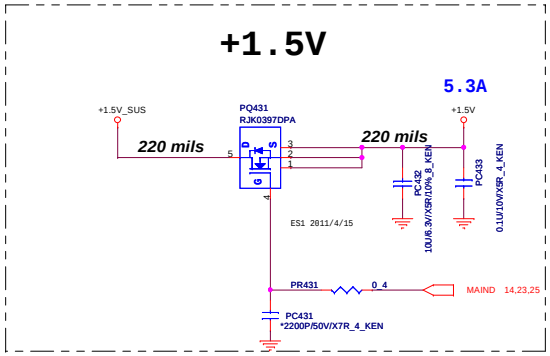
Size	Document Number	Rev
	POWER +VCCSA/VCC1.8V	1C

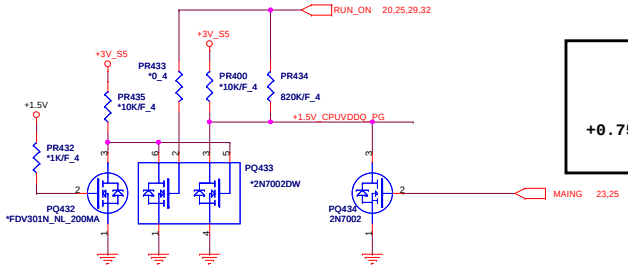
Date: Monday, December 19, 2011 Sheet 26 of 35

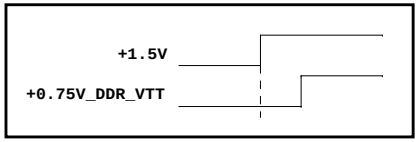
1.5VSUS & VTT_MEM

Fuse Rating =
IR(max) / (0.75* 0.75) =(1.5V*12.5A/0.9/7.5V)/ 0.5625
= 4.94A









MODE	DISCHARGE MODE
+5V	No discharge
+1.5V	Tracking discharge
GND	Non-tracking discharge

VDDQSET	VDDQ(V)	VTTREF & VTT	NOTE
GND	1.5 fixed	VDDQSNS/2	DDR3
5V	1.8 fixed	VDDQSNS/2	DDR2
FB-Resistor	Adjustable	VDDQSNS/2	1.5V<VDDQ<3V

VTT = VTTREF = VDDQSNS/2 = 0.75V

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	on	on	on
S3	0	1	on	on	off
S4/S5	0	0	off	off	off

Quanta Computer Inc.
PROJECT : FF4

Size	Document Number	Rev
	POWER 1.5VSUS/VTT_MEM	1C

Date: Monday, December 19, 2011 Sheet 27 of 35

Fuse Rating =
IR(max) / (0.75* 0.75) =(1.23V*33A/0.9/7.5V) / 0.5625 = 10.69A

GFX_CORE LL: -3.9mV/A for GT2

Parallel

Fsw Setting=300KHz

PU100
ISL95836HRTZ

Place NTC close to the GFX_CORE inductor

Place NTC close to the VCORE Hot-Spot.

Parallel
VCORE LL: -1.9mV/A

Place NTC close to the VCORE inductor of phase 1

V:0V to 1.23V
I:33A max for GT2
OCP: Min 36.32A, Max 43.34A

ES0-1024-2

ES0-1114-2

Fuse Rating =
IR(max) / (0.75* 0.75) =
(1.05V*53A/0.9/7.5V) / 0.5625= 14.66A

ES0-1110-02

V:0.3V to 1.23V
I:53A
OCP:Min 58.72A, 68.45A

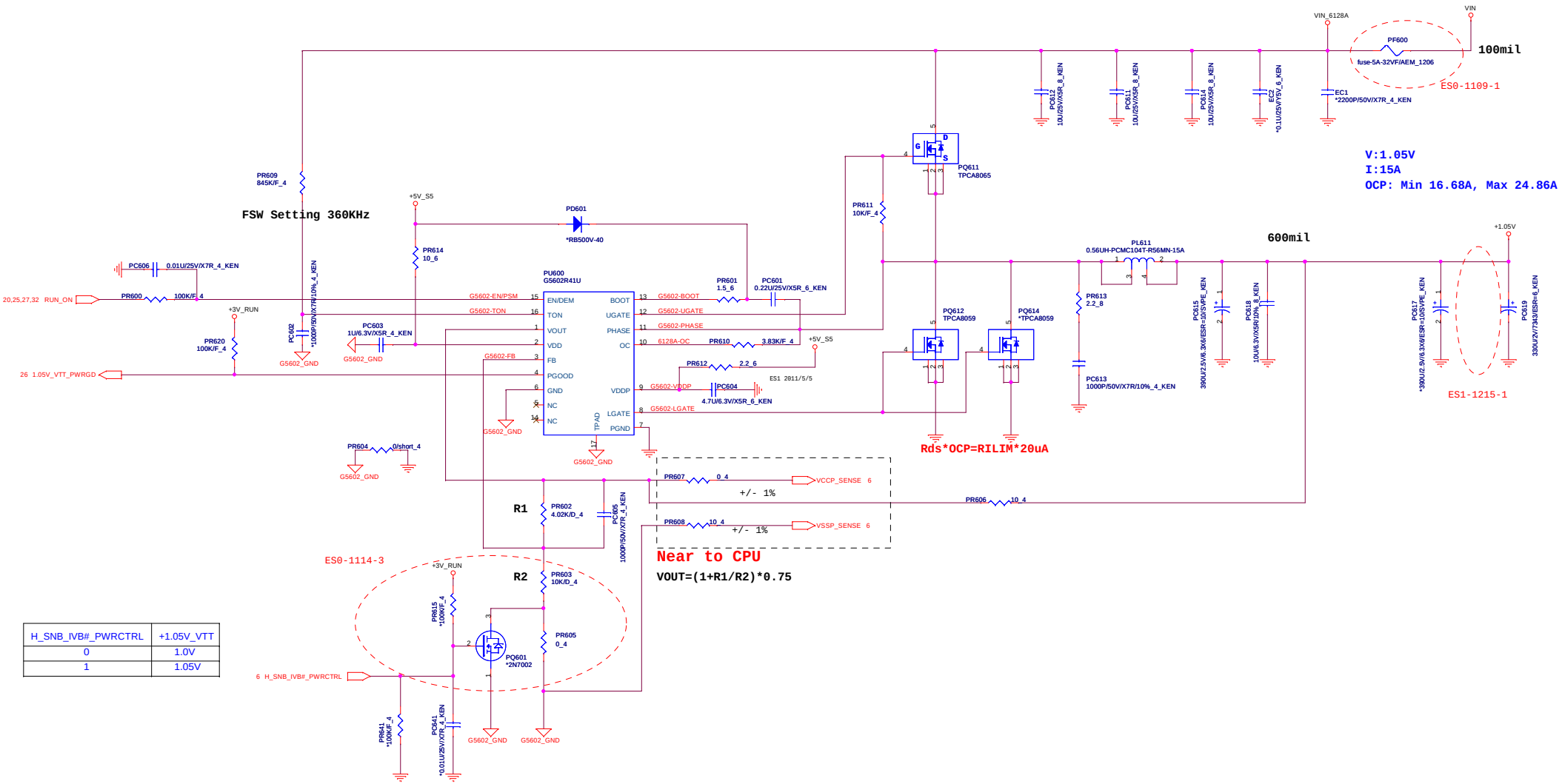
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Quanta Computer Inc.
PROJECT : FF4

Size	Document Number	Rev
	POWER +VCC_CORE (ISL95836)	1C
Date: Monday, December 19, 2011	Sheet 28 of 35	

+1.05V / 15.0A

Fuse Rating =
IR(max) / (0.75* 0.75) =(1.05V*15/0.9/7.5V) / 0.5625
= 4.15A

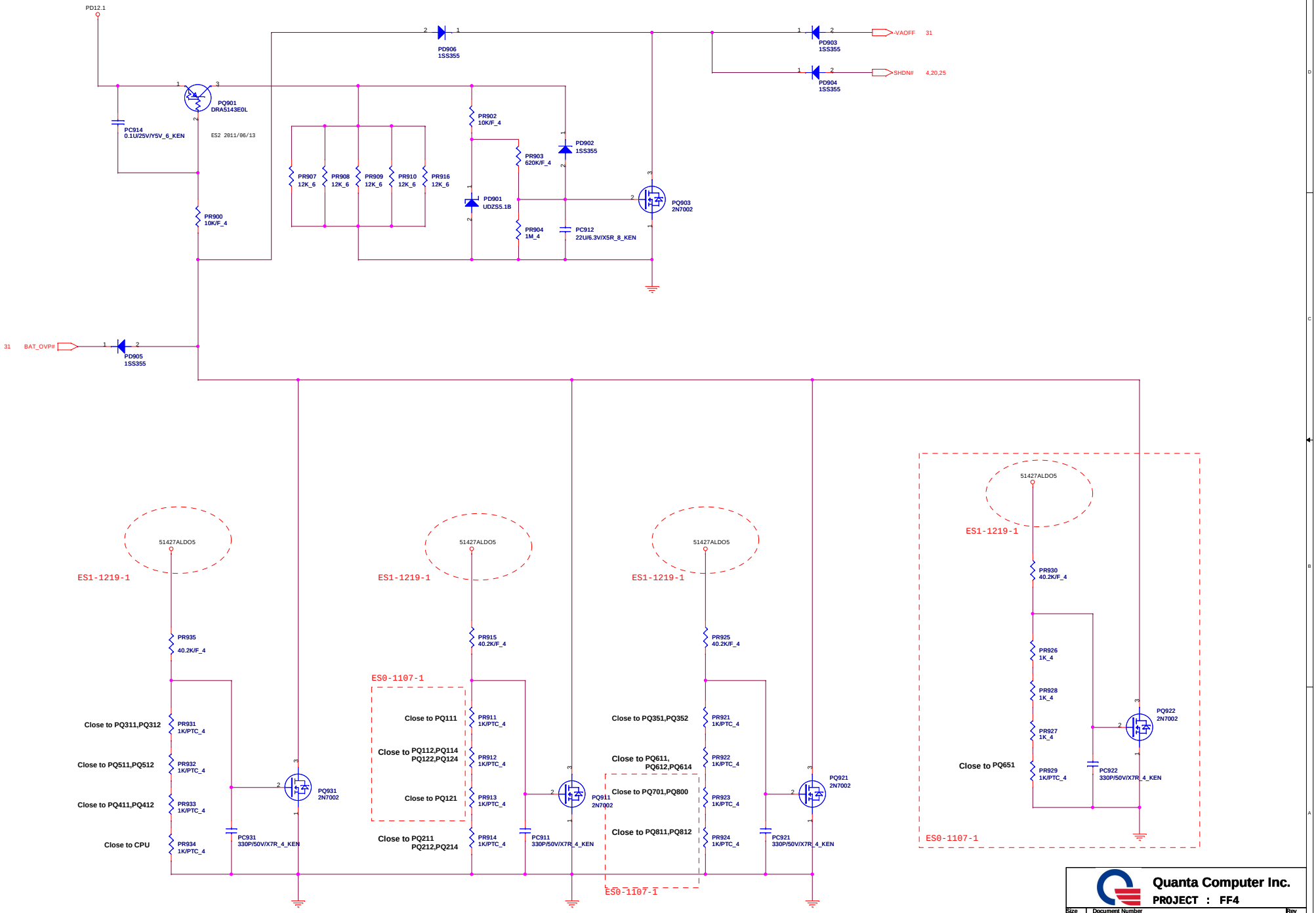


H_SNB_IVB#_PWRCTRL	+1.05V_VTT
0	1.0V
1	1.05V

Quanta Computer Inc.
PROJECT : FF4

Size	Document Number	Rev
	POWER +1.05V(G5602R41U_-15A	1C

Date: Monday, December 19, 2011 Sheet 29 of 35



Quanta Computer Inc.
PROJECT : FF4

Size	Document Number	Rev
	POWER Thermal Protection	1C

Date: Monday, December 19, 2011 Sheet 30 of 35

AC ADAPTOR IN CONN

Fuse Rating =
IR(max) / (0.75* 0.75) =4.74A / 0.5625 = 8.427A

ES0-1024-2

240mil

PCN700

ACS-20288-044L

VAIN+

VAIN-

EL4 0_8

EL3 0_8

EL2 0_8

EL1 0_8

PC701 0.1U/50V/X7R_6_KEN

PC702 1000P/50V/X7R_4_KEN

PC703 0.1U/50V/X7R_6_KEN

PF700

fuse-10A-24VF/AEM_1206

VA+

PD703

PDS1040

PD12.1

PQ734B RN4603

PQ701 AOD403

VA

PD701 P4SMAJ20A

PD702 P4SMAJ20A

PD731 UDZS15B-7-F

PC734 0.1U/50V/X7R_6_KEN

PR734 220K_4

PC735 0.1U/50V/X7R_6_KEN

PC736 0.01U/50V/X7R_4_KEN

PC737 0.1U/50V/X7R_6_KEN

PR735 220K_4

ES0-1108-1

20 ACIN

PR732 4.7K/F_4

30 -VAOFF

-VAOFF

PD853 UDZS5.1B

PD732 PDZ3.3B

PR731 4.7K/F_4

PQ734A RN4603

20,32 DC/-C

PC739 0.1U/10V/X5R_4_KEN

Adapter UVP

VA+

PD751 UDZS15B-7-F

PR752 220K_4

PD752 1SS355

-VAOFF

PD753 1SS355

ACIN 20

PR751 47K/F_4

PQ751 PDTC144EU

PR753 196K/F_4

PC753 4.7U/10V/X5R_6_KEN

PQ752 2N7002K

Max UVP Threshold VA+ =17.12V
Typ UVP Threshold VA+ =16.46V
Min UVP Threshold VA+ =15.41V

ES0-1024-1

BATTERY OVP

Latched until remove both BAT and ADP

ES1-1212-2

BAT+

PR851 200K/B_4

PC855 1000P/50V/X7R_4_KEN

G682L09TT12U

CD RESET GND VSEN VCC

PU850

PR852 12.1K/B_4

PC852 1U/10V/X5R_4_KEN

ES1-1212-2

PR854 150K_4

+3VPCU

PR956 470K/F_4

BAT_CELL_ID

PQ269 SSM3K09FU

PQ853 2N7002

BAT_OVP# 30

PC854 1000P/50V/X7R_4_KEN

PD12.1

PR853 147K/F_4

PC853 0.1U/50V/X7R_6_KEN

PD851 UDZS5.1B

(Typ) trip point of BAT+=13.81V
(Max) trip point of BAT+=14.11V
(Min) trip point of BAT+=13.51V

ES0-1024-1

BAT+

PQ762 DRA5143E0L

BAT_OVP#

PD762 1SS355

PR766 10K_4

20 CELL_DISCHARGE

PR767 100K_4

PC767 0.1U/10V/X5R_4_KEN

PQ764 2N7002

VA+

PQ761 DRA5143E0L

-VAOFF

PD761 1SS355

PR763 160_2512

PR761 4.7K/F_1206

PR762 470_2512

PR764 160_2512

Fuse Rating =
IR(max) /(0.75*0.75) = 80W/7.5V / 0.5625 =18.96A

ES0-1109-1

PF102

fuse-20A-24VF/AEM_1206

400mil

BAT+

PCN800

ALLTOP-C144JS-107A7-L

P_MBAT

P_DATA

P_CLK

PR843 100_4

PR842 100_4

ES0-1102-2

MBDATA_BAT 20,32

MBCLK_BAT 20,32

PC843 47P/50V/NPO_4_KEN

PC842 47P/50V/NPO_4_KEN

PD804 PDZ5.6B

PD805 PDZ5.6B

PD806 PDZ5.6B

PC844 0.1U/25V/X7R_6_KEN

PC845 0.1U/25V/X7R_6_KEN

PC846 0.1U/25V/X7R_6_KEN

BAT_CELL_ID 20

PC834 0.01U/50V/X7R_4_KEN

ES0-1109-1

ES0-1024-1

CELL_ID voltage :		
	4cell_4S1P	6cell_3S2P
Battery only	2.2V	0V
Adapter only	3.3V	3.3V
Battery+Adapter	2.2V	0V

Quanta Computer Inc.
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Size	Document Number	Rev
	POWER ADP IN / BAT IN	1C

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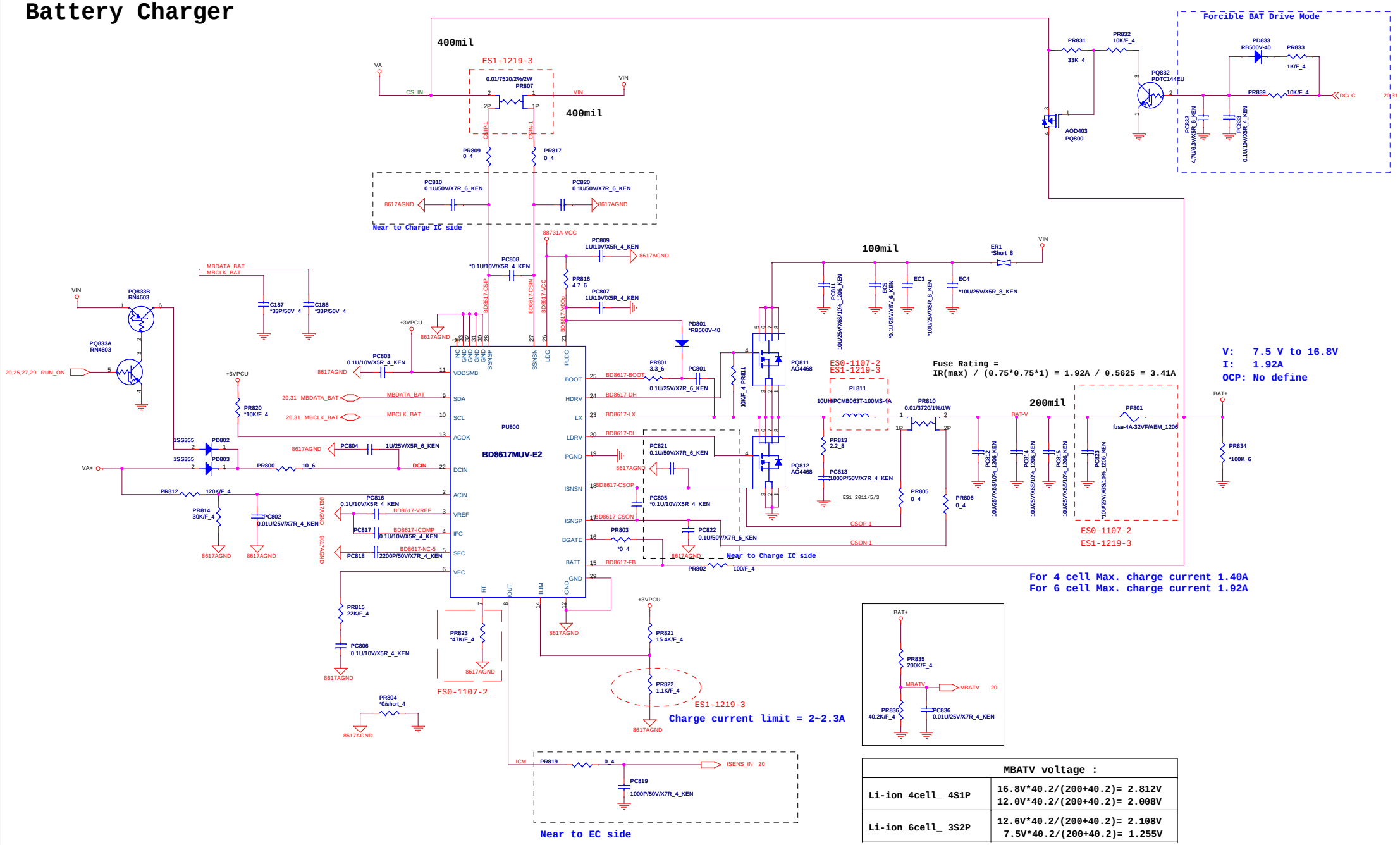
Battery Charger



MBATV voltage :	
Li-ion 4cell_ 4S1P	16.8V*40.2/(200+40.2)= 2.812V 12.0V*40.2/(200+40.2)= 2.008V
Li-ion 6cell_ 3S2P	12.6V*40.2/(200+40.2)= 2.108V 7.5V*40.2/(200+40.2)= 1.255V

Quanta Computer Inc.
PROJECT : FF4

Size	Document Number	Rev
	POWER CHARGER (BD8617MUV-E2))	1C

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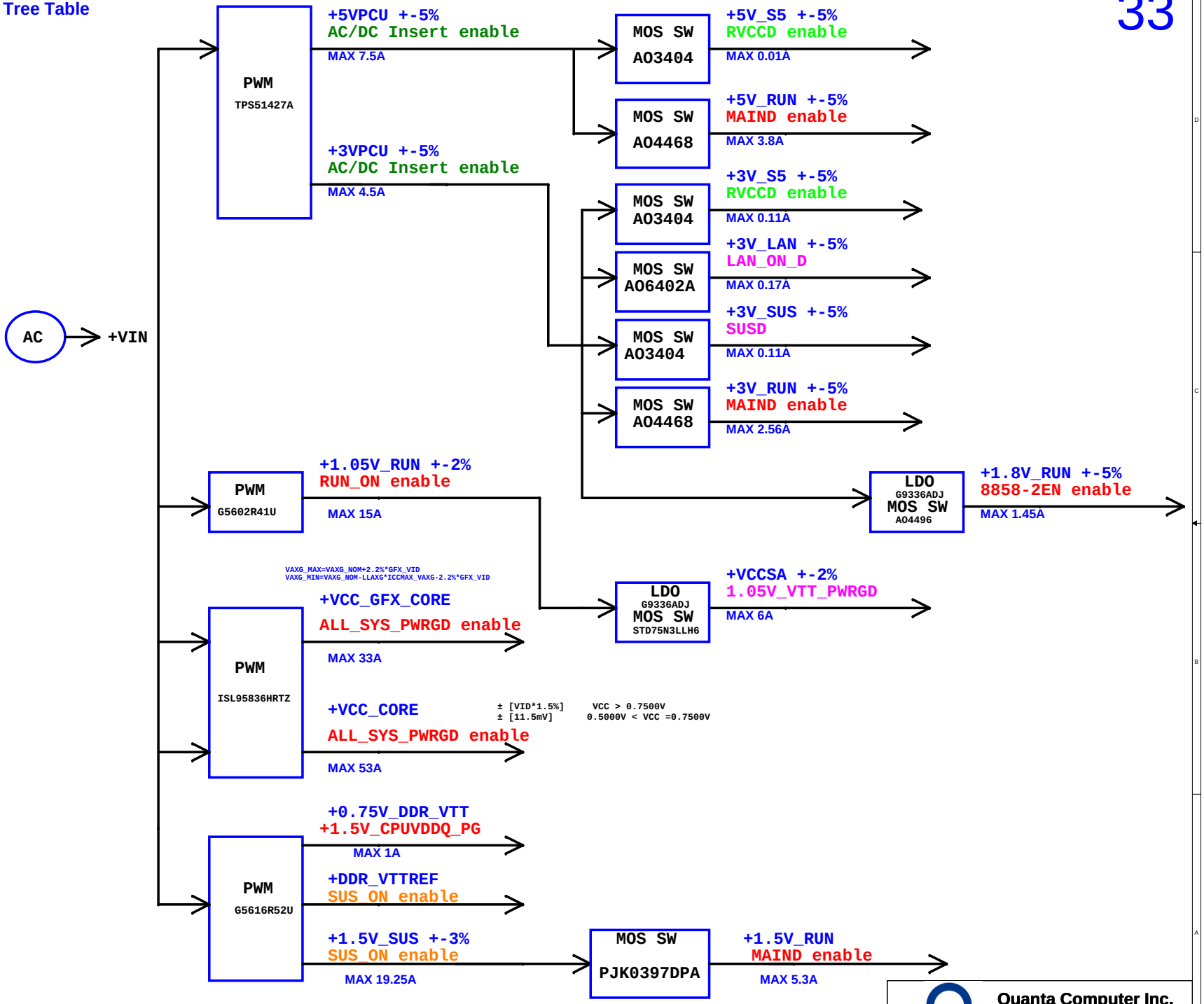
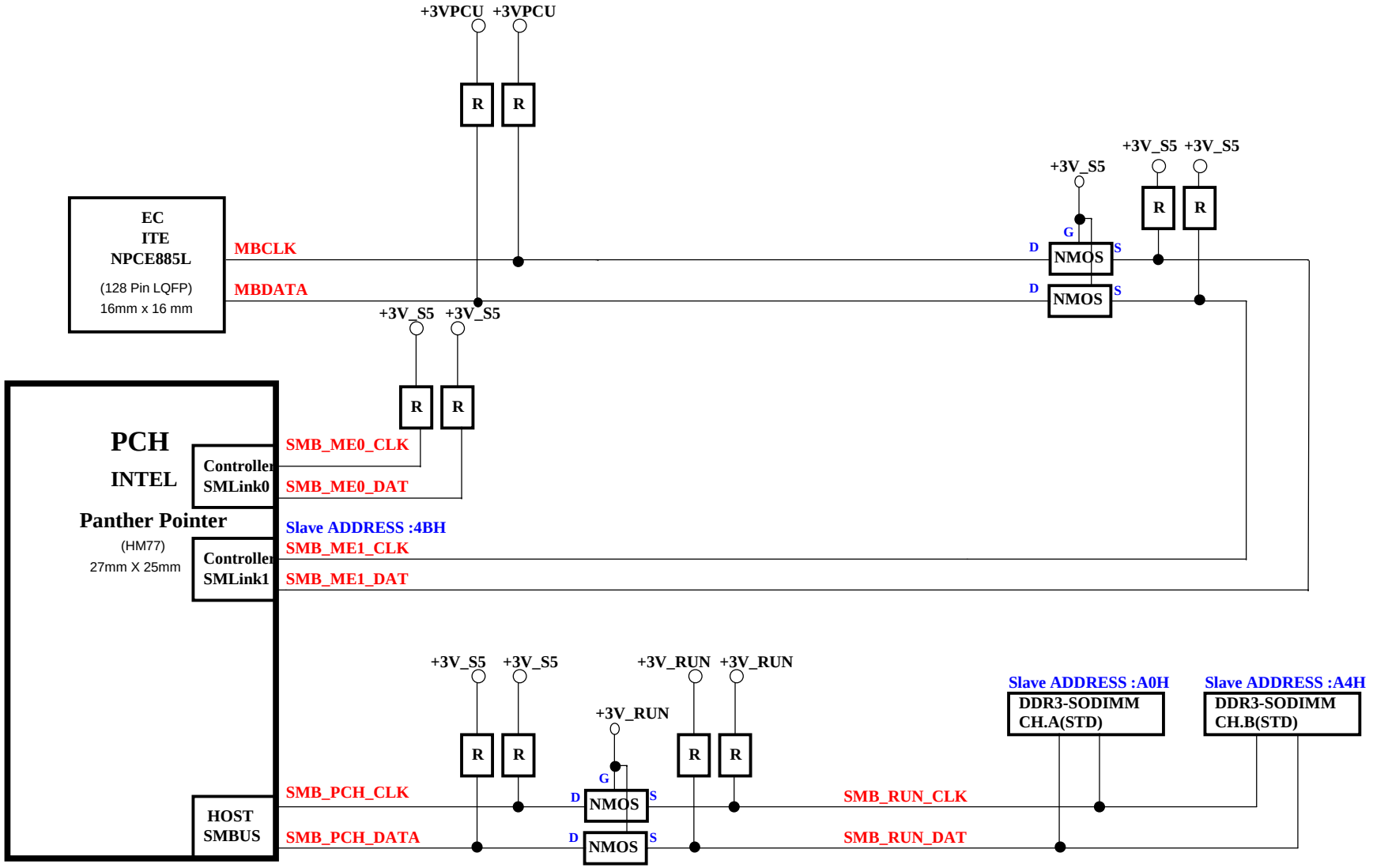
Power Tree Table



Quanta Computer Inc.		
PROJECT : FF4		
Size	Document Number: Power Tree	Rev: 1C
Date: Monday, December 19, 2011	Sheet 33 of 35	



Quanta Computer Inc.

PROJECT : FF4

Size	Document Number	Rev
	SM BUS	1C

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Change List

Item	Page	Reason	Detail
	ALL		ES0 release
ES0-1018-1	21	Add signal for RF module.	Add RFMD_ON.
ES0-1018-2	21	Change BTB connector for more signals and power.	CN9 change from 30 pin to 40 pin and re-define sginals.
ES0-1018-3	24	Change footprint of C372.	C372 change from 0603 to 0402.
ES0-1018-4	16,18	Change connectors.	Change connector of CN10, CN11,CN18.
ES0-1018-5	23	Add a reserved capator for WLAN power.	Add C416 and reserved.
ES0-1020-1	19	Change circuit of speaker portion.	Remove AL6~AL9, AC32, AC33; change AR26~AR28, AR30 from 1206 0hm to 0805 default short.
ES0-1020-2	14	For HDMI criteria solution.	Change diodes for HDMI DDC bus.
ES0-1020-3	4	Delete un-used circuit.	Delete Q12, R95.
ES0-1024-1	31	Add battery OVP, BAT+ discharge, and CELL_ID circuit	
ES0-1024-2	27,28,31 35	Modify D2D Fuse for 6cell battery.	
ES0-1024-3	11,20,24	Remove un-necessary circuit.	Delete R199, L22, R205, KR4, KR7 and thermal protect circuit.
ES0-1024-4	8,9	Change capacitors of XTALs as vendor's suggestion.	C337,C338, C345, C346 change from 18P to 15P.
ES0-1025-1	27	Add a 0.033U capacitor to correct voltage level of 0.75V.	Add PC169 at PU400 pin 5.
ES0-1026-1	19	For meet the requirement headphone jack output with 32ohm in DA test, change series resistor at headphone.	AR6, AR7change from 75 ohm to 62 ohm.
ES0-1026-2	20	Delete SPI rom for EC and its relative circuit.	Delete KU2 and its relative circuit; adjust resistors for SPI ROM U14.
ES0-1027-1	19	Reserve RC circuit for DMIC clock and data.	Add R366, R367, C71, C84(capacitors are reserved).
ES0-1102-1	25	Modify Boost resistor	PR301 change from 1 ohm to 2.2 ohm, PR501 change from 1 ohm to 4.7 ohm,
ES0-1102-2	31	Modify SMbus resistor for EE request	PR842,PR843 change from 330 ohm to 100 ohm,
ES0-1102-3	13	Modify LVDS signals to connector for layout more smooth.	Modify EDID, DATA and Clock to CN3.
ES0-1102-3	9	To prevent glitch of PLTRST#, add a capactor.	Add C417 close to U16.
ES0-1107-1	30	Add Posistor circuit and modify some posistors location.	Add PR926~PR930,PQ922,PC922
ES0-1107-2	32	Modify Schmetic for 6 cell battery	Change PL811 frome 10uH-4A to6.8uH-4.5A, add PC823 , Change PF801 frome 5A to 10A, Prepare PR823 to modify switch frequency
ES0-1107-3	8,20	Reserve series resistors for LCP signal overshoot and undershoot.	Add R368~R372 close to PCH; R373~R377 close to EC.
ES0-1108-1	32	Change snubber circuit to " P4SMAJ20A" for DC-IN area.	Delet PR737,PR736~PR739, Add PD701,PD702
ES0-1109-1	31	Change batttery connector to fit battery pack (SANYO's request for safety).	Change PCN800.
ES0-1110-1	16	Add a screw hole near CRT connector to fix board.	Add H30.
ES0-1110-2	28	Change "+VIN_VCC_CORE" input capacitor.	Change PC23,PC29,PC30 from 27u to 47u.
ES0-1111-1	25	Modify for 6 cell battery input	Change PD501 from 5.1V to 3.3V,PR504 from 100K to 147K, PR505 from 330K to 120K.
ES0-1114-1	25	Add PR500	Add PR500
ES0-1114-2	26	Inrcease the current rating of PL811.	Change PL811 from "PCMB104T-R36MT"(30A) to "FDU1040D-H-R36M=P3"(33A)
ES0-1114-3	29	Fix +1.05V_VTT output voltage to 1.05V	Change PR605 from 2.05K to 0 ohm, Delete PR615,PQ601
ES1-1209-1	22	Change front side LED's footprint to fit vendor's spec.	Change footprint of LED2, LED5, LED7.
ES1-1209-2	9,17	For solving ringback of PLTRST#.	Stuff MC1 100P and C417 is reserved.
ES1-1209-3	16	For request of facetory to reduce tolerance of nut length, change nut.	Change NUT at H22, H23.
ES1-1209-4	13	For better signal quality, remove bead at DMIC_CLK.	Chagne L13 from bead to 0 ohm.
ES1-1209-5	14,15,16,21	For EMI's request, remove shield ground for I/O ports.	Remove SHIELD_GND and R37, R45, R354~R357.
ES1-1209-6	8	For better sginal quality, change series resistors of LPC.	Change R368~R372 from 0 ohm to 27 ohm.
ES1-1209-7	19	For better sginal quality, change series bead of HP.	Change bead of AL3, AL4.
ES1-1209-8	15	For EMI's request, change capacitors of CRT's R,G,B signals.	Change C2, C3, C7, C8, C11, C12 from 4.7P to 10P.
ES1-1212-1	25	Change Control IC from "TI51427" to "PM6686"	PR301 change from 2.2 ohm to 1 ohm, PR501 change from 4.7 ohm to 1 ohm, PR504 change from 147K ohm to 100K ohm, PR505 change from 120K ohm to 100K ohm, PC503 change from 10uF to 4.7uF, PC509 change from 1uF to 0.1uF, Add "PM6686_ENLDO" signal.
ES1-1212-2	31	Modify for VSEN/VCC timing, BAT_CELL_ID voltage	Add PR854 150K ohm, PR956 change from 1M ohm to 470K ohm, PC852 change from 1000P to 1uF.
ES1-1213-1	17	For ESD protect of SD Card work, add a bead on SD power.	Change R34 to ML3.
ES1-1213-2	17	For compatibility of SD card, add capacitors for signals.	Add MC16~MC21.
ES1-1214-1	16	For factory's request to prevent LED. Reserve a position for NUT.	Add H32.
ES1-1215-1	29	For layout space consideration, remove unused capacitor of +1.05V.	Remove PC616.
ES1-1219-1	30	Modify Net name from 62371LDO5 to 51427ALDO5	Change Net name from 62371LDO5 to 51427ALDO5
ES1-1219-2	25	Modify 51427AENLDO circuit for Battery latch issue	
ES1-1219-3	32	Add Charge current limit = 2~2.3A, modfiy PR807 for de-rating Because charging current was reduced ,we modify PL811,PF801,PC823	Add PR822, 1.07K ohm,charge PR807 from 1W to 2W. Change PL811 from 5.6 uH to 10 uH, PF811 from 10A to 4A, Remove PC823
ES1-1219-4	25	For +3V_RUN glitch when using Sandisk SSD, change capacitor at MAIND.	Change PC949 from 2200P to 0.015U.
ES1-1219-5	17	For EMI of SD Card, add capacitor at SD CLK.	Add MC10 with 5P capacitor.