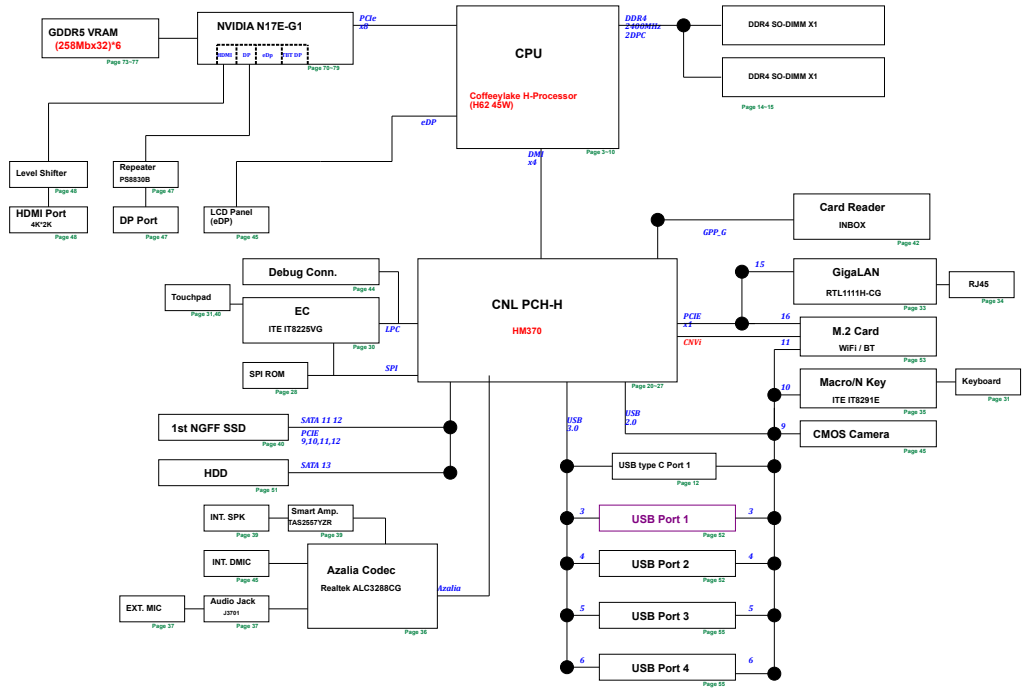
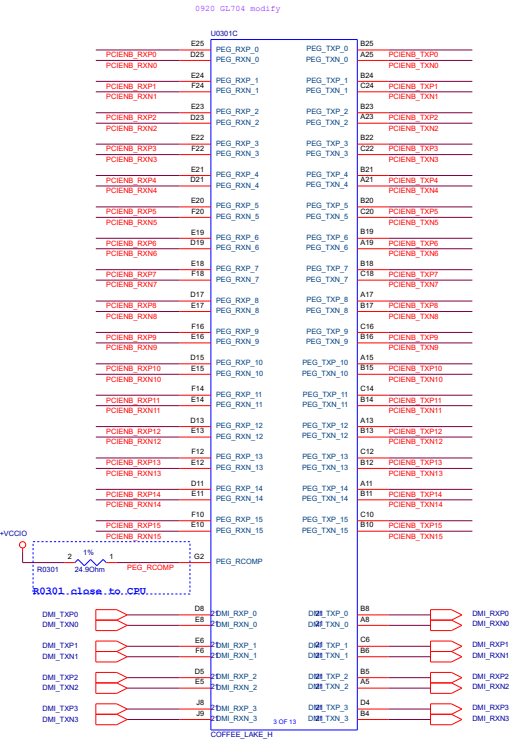
GL704GM Block Diagram

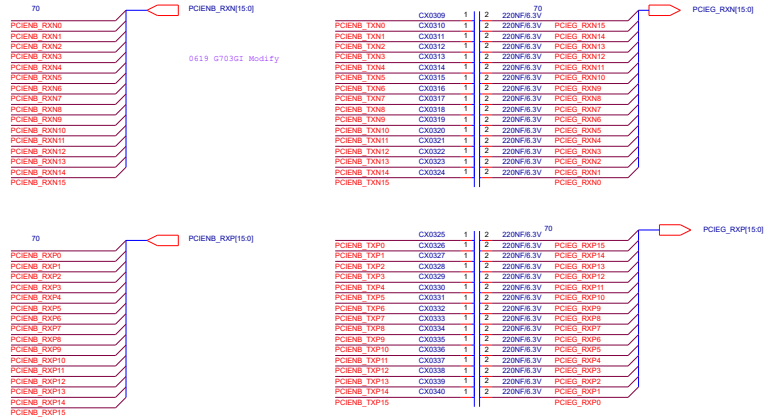
Coffeelake H Platform



ASUS	Project Name: GL704GSM		Rev: 0.1
Title :	Block Diagram		
Size: D	Dept.: ASUSTeK COMPUTER INC	Engineer:	NB1 RD2 EE1
Date: Friday, July 27, 2018		Sheet: 1	of 103

PCIEG





Display

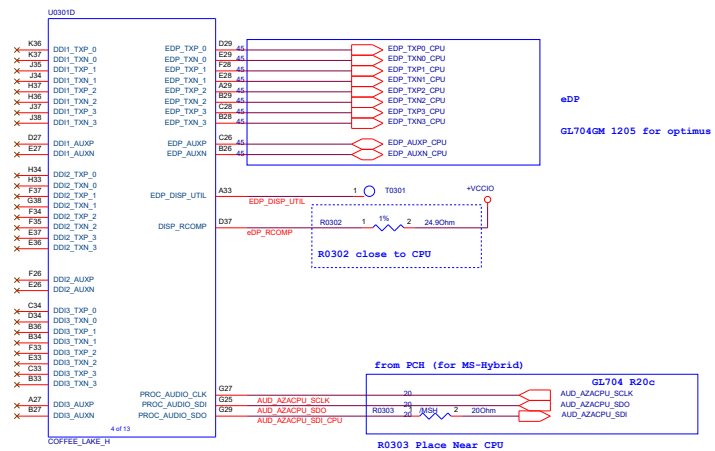


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 8.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane12.

Refer to CFL-H PDG P.363 (Doc.571391)

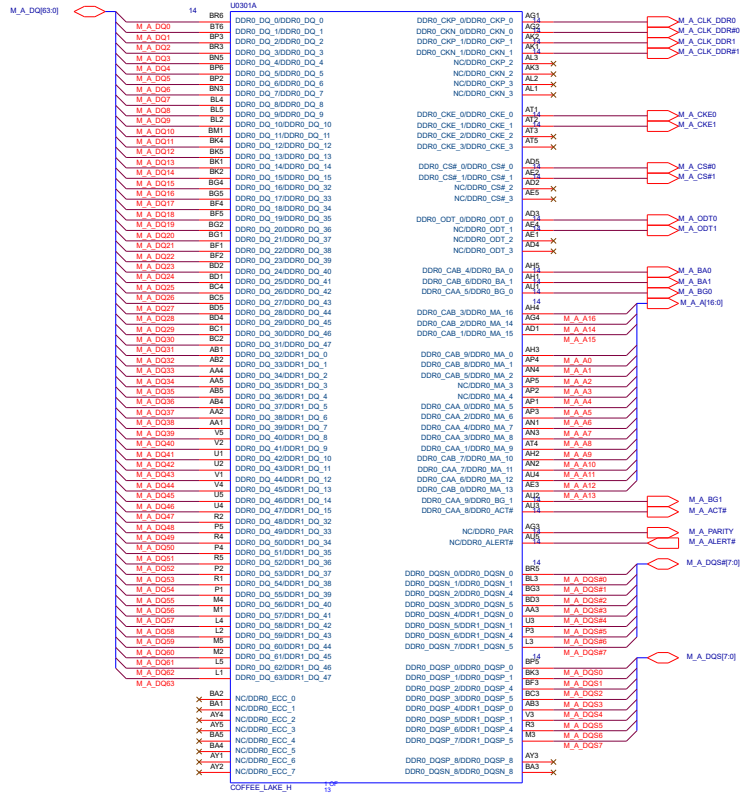
31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~2KΩ), PROC_AUDIO_SDO can be left unconnected.

Project Name: GL704GSM			Rev: R1.1
Title : CPU_DMI,PEG,FDI,eDP,DDI			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 3	of	103

Memory Channel A



Memory Channel B

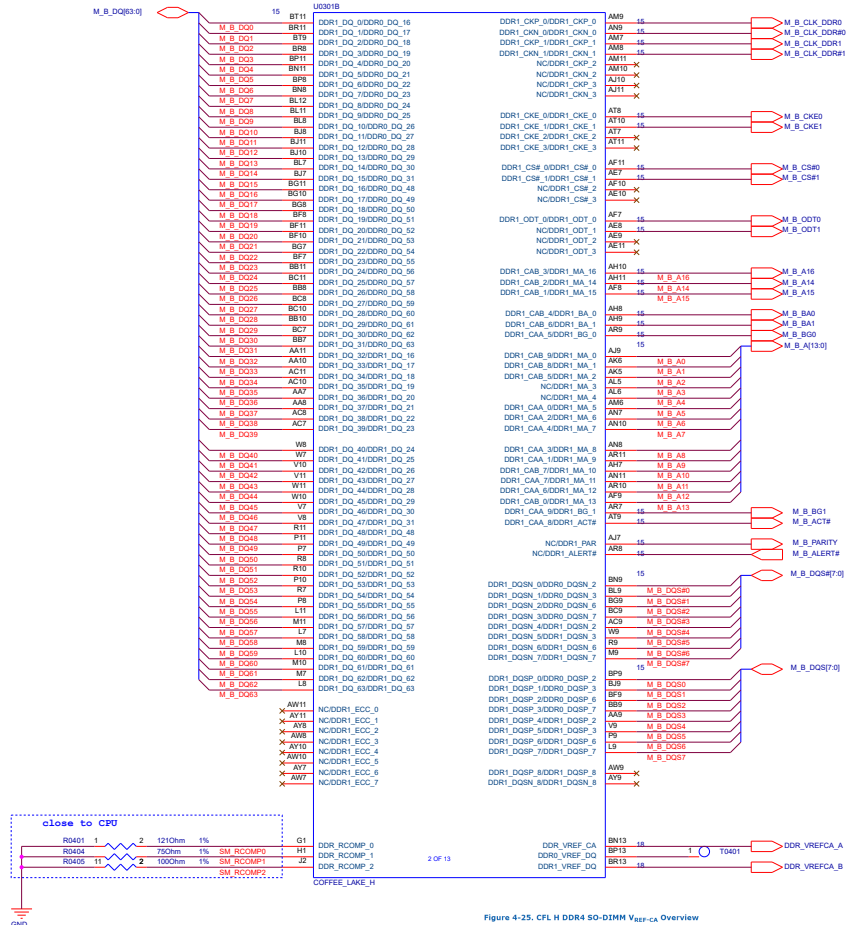
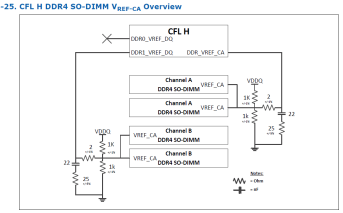
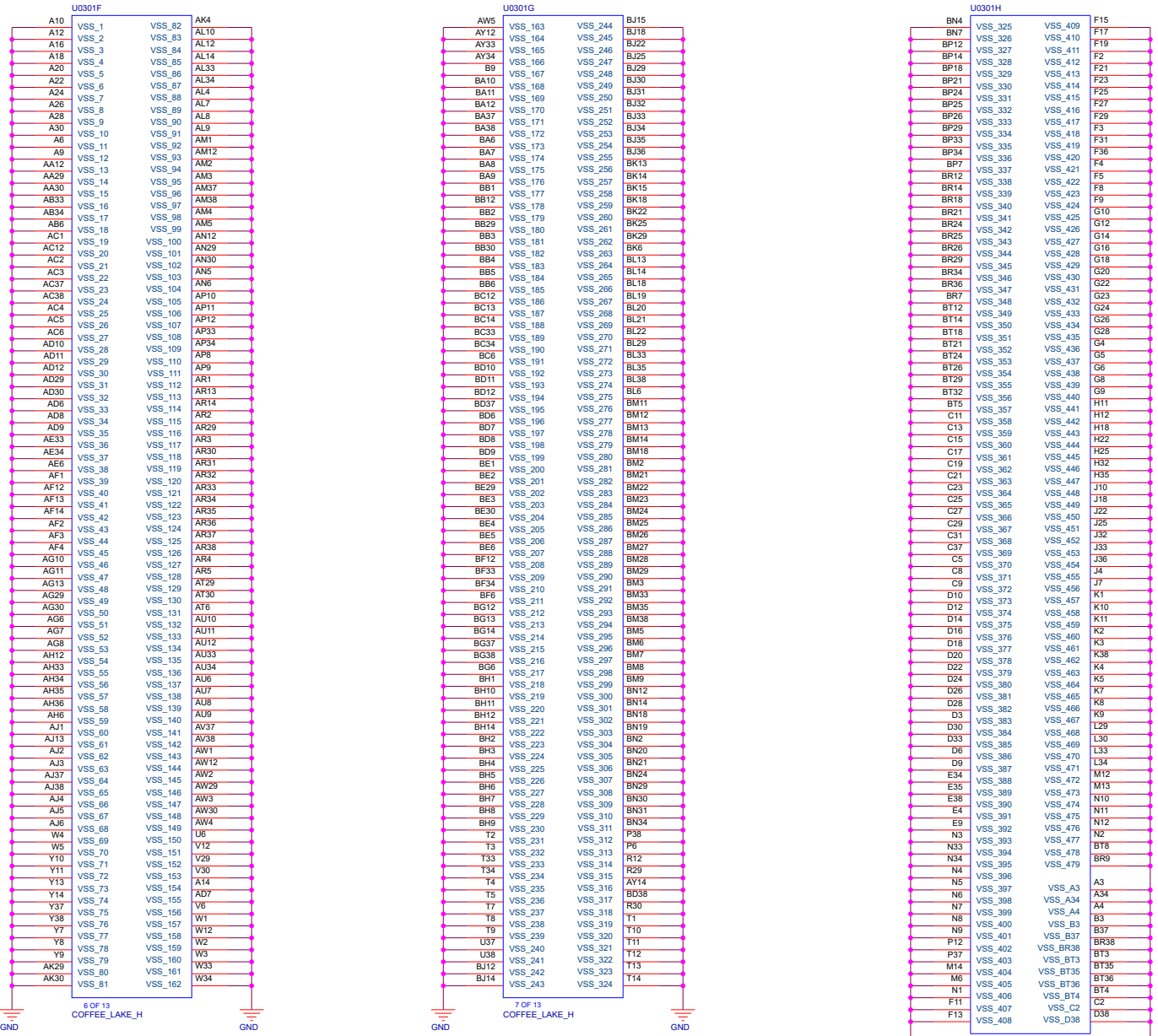


Figure 4-25. CFL H DDR4 SO-DIMM V_{REF-CA} Overview

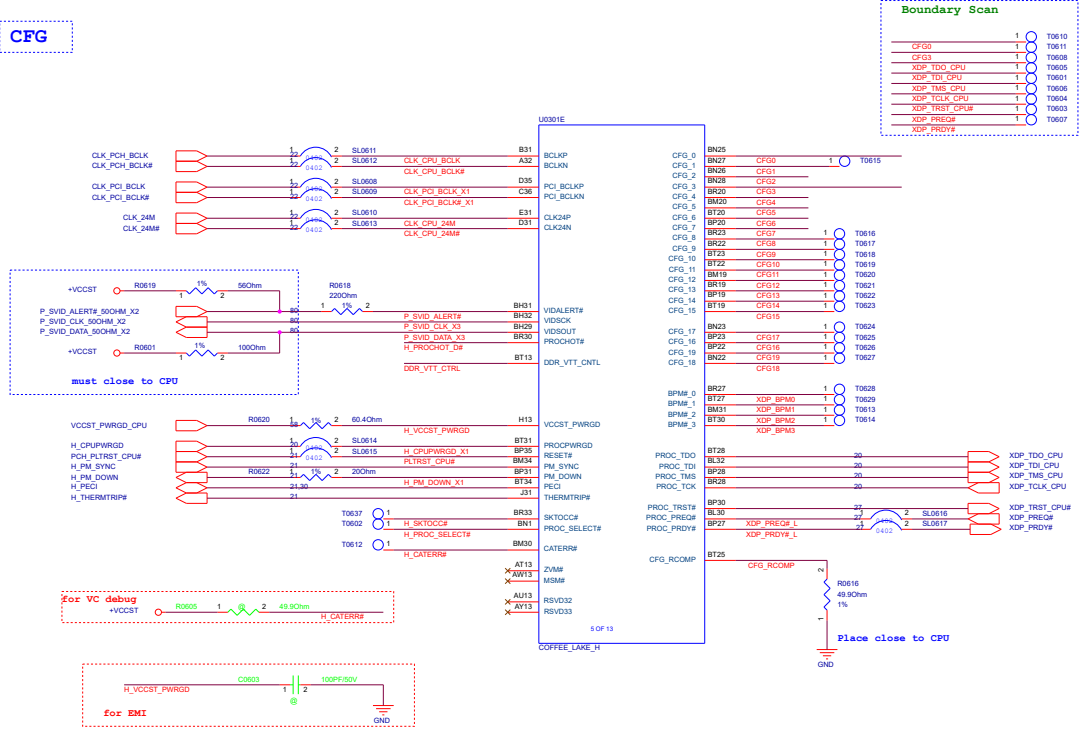


ASUS	Project Name: GL704GSM		Rev: R1.1
Title : CPU_DDR4			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 4 of 103		

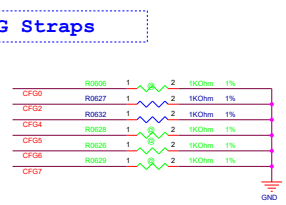


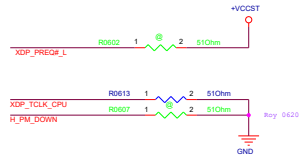
ASUS	Project Name: GL704GSM	Rev: R1.1
Title : CPU_GND		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 5 of 103	

CFG



CFG Straps





CFG Straps for Processor

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Expres* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

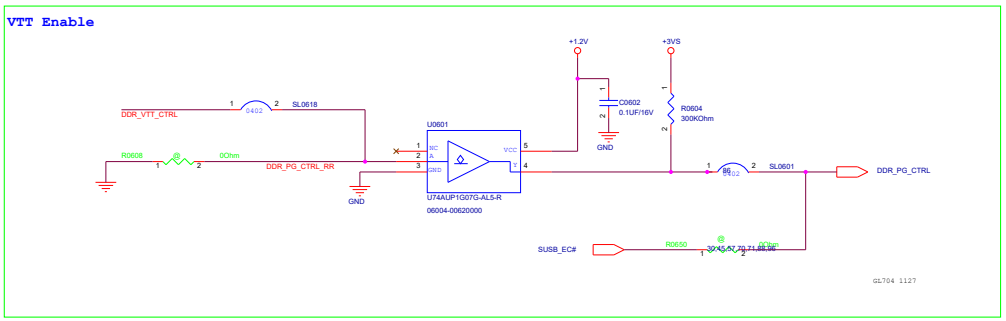
CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes

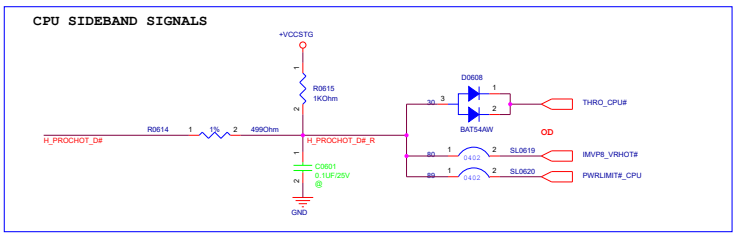
Refer : Intel 570805_CFL_EDS_Vol1_Rev1.1, Table 6-7, P.116

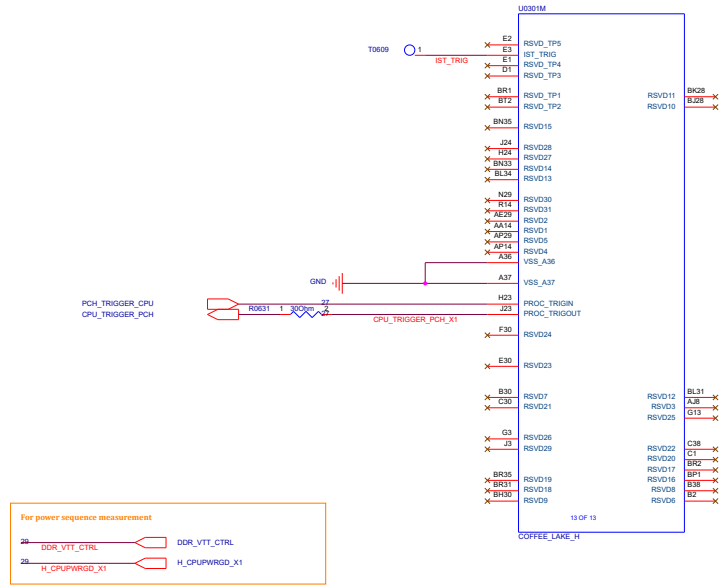
DDR_VTT_CNTL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator in C8 and deeper and S3.

VTT Enable



CPU SIDEBAND SIGNALS



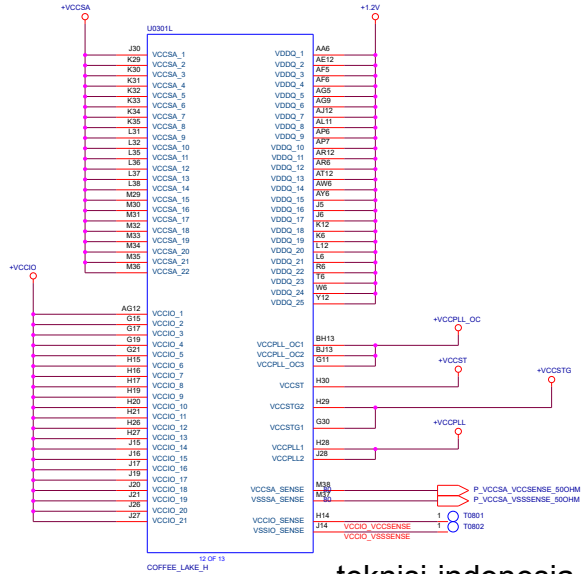


For power sequence measurement

DDR_VTT_CTRL
H_CPUPWRGD_X1

Project Name	GL704GSM
Rev	R1.1
Title :	CPU_CFG,RSVD
Size	C
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Gaming RD4 EE1
Date:	Friday, July 27, 2018
Sheet	6 of 103

Main Board



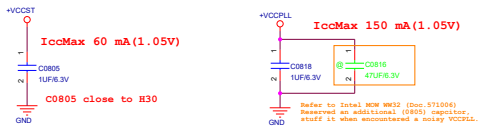
teknisi-indonesia

Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
VccST off in S3	On in S3	+25-30mW
VccPLL_OC off in S0/C10	On in S0/C10	+3-10mW
VccPLL_OC off in S0ix	On in S0ix	+3-10mW

Main Source	1st PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	+1.05V_VCCST
		+VCCSTG	+1.05V_VCCPLL
	+1.2V	+VDDQ_CPU	
		+VCCPLL_OC	
	+VCCSA		
	+VCCIO		

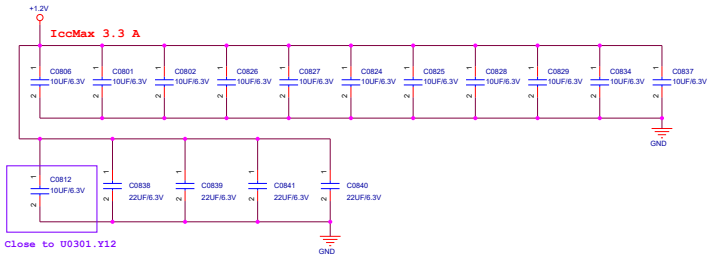
+VCCST/+VCCPLL DECAPS Place Back Side (TOP)

Roy 0620

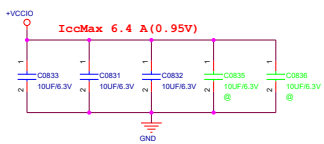


+VDDQ DECAPS Place Back Side (TOP)

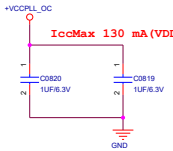
10UF x 11
22uF x4



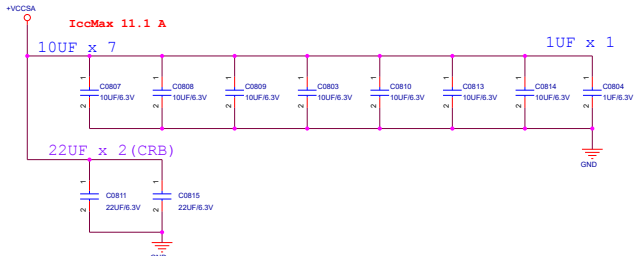
+VCCIO DECAPS Place Back Side (TOP)



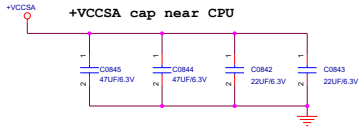
+VCCPLL_OC DECAPS Place Back Side (TOP)



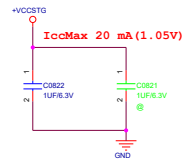
+VCCSA DECAPS Place Back Side (TOP)



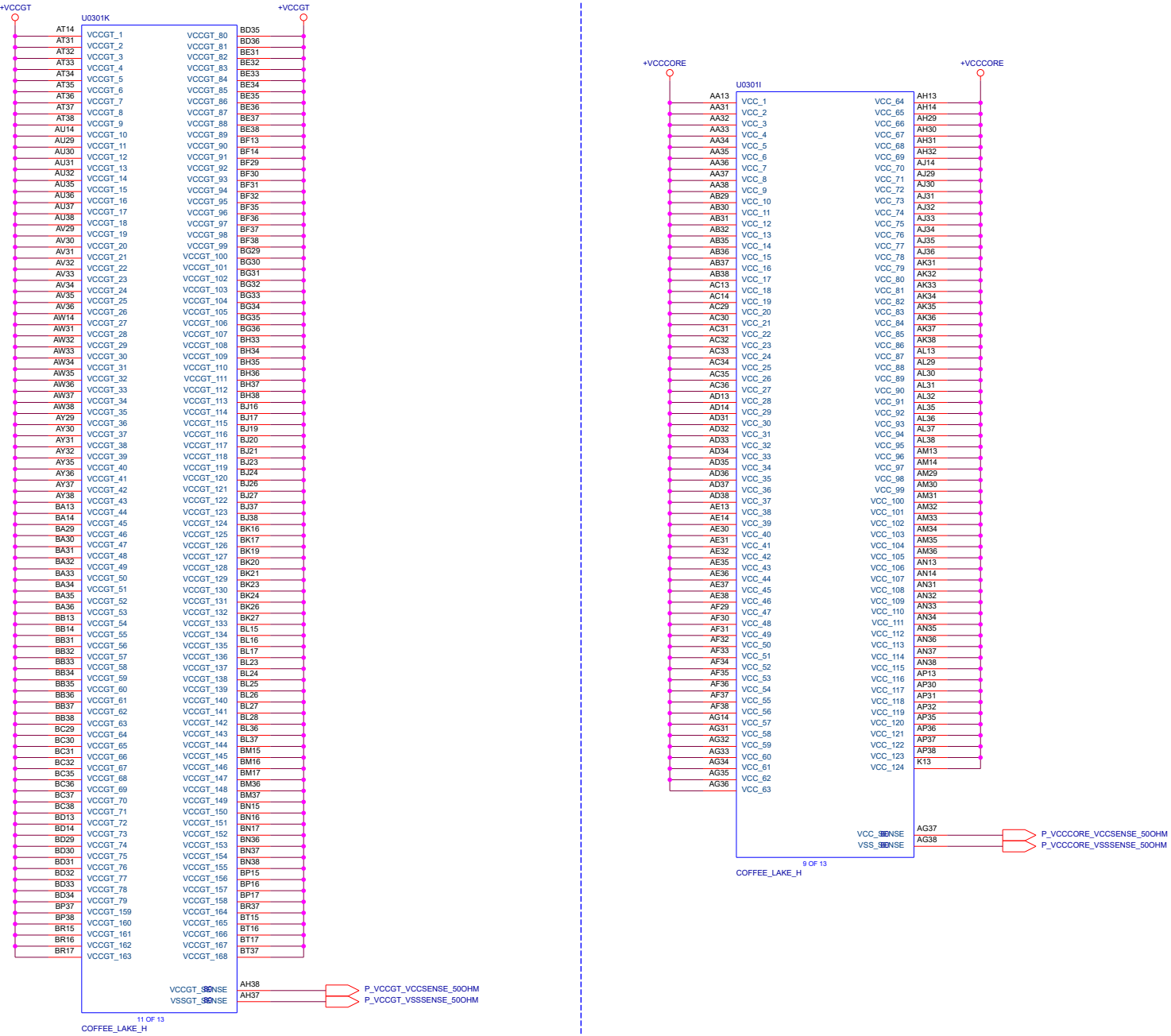
+VCCSA cap near CPU



+VCCSTG DECAPS Place Back Side (TOP)



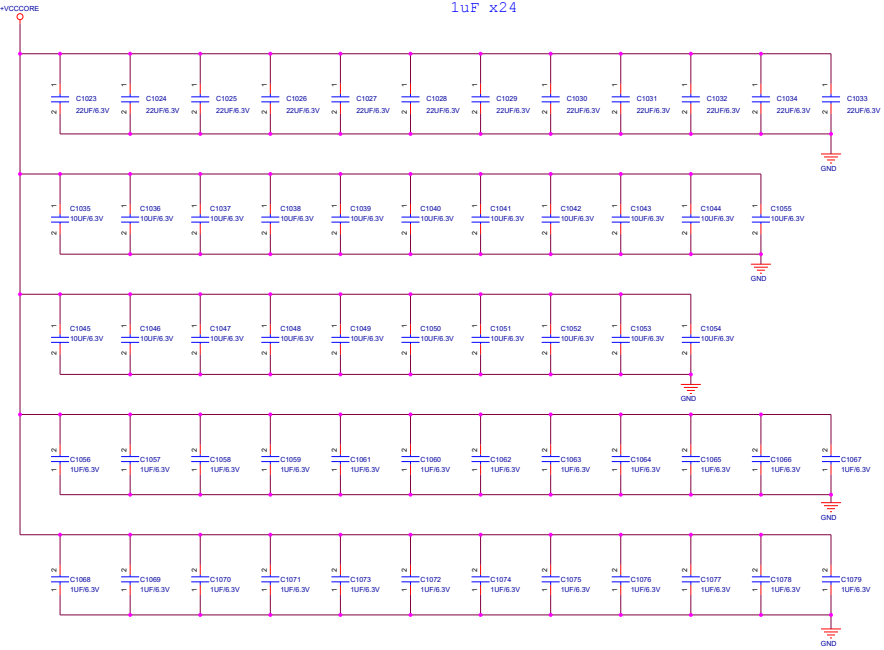
Project Name: GL704GSM			Rev: R1.1
Title: CPU_PWR			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 8 of 103		



ASUS	Project Name: GL704GSM	Rev: R1.1
Title : CPU_PWR		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 9 of 103	

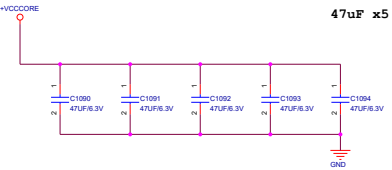
+VCCCORE DECAPS Place Back Side (TOP)

22uF x12
10uF x21
1uF x24



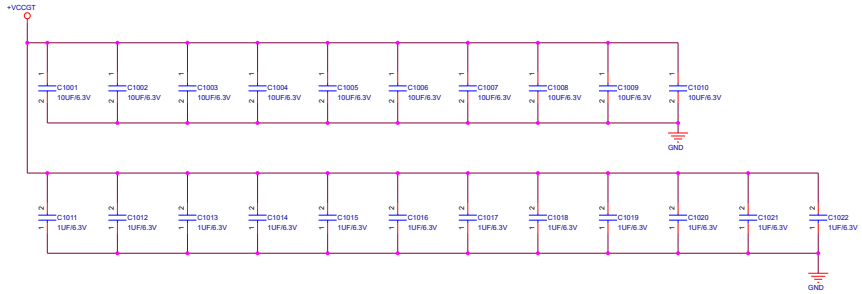
+VCCCORE cap near CPU

47uF x5



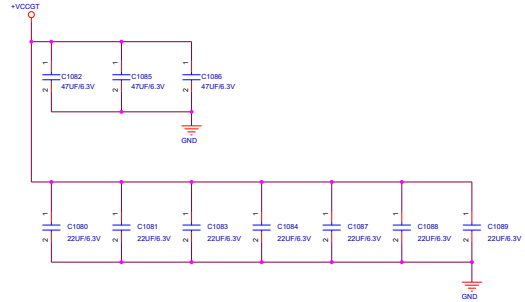
+VCCGT DECAPS Place Back Side (TOP)

10uF x10
1uF x12



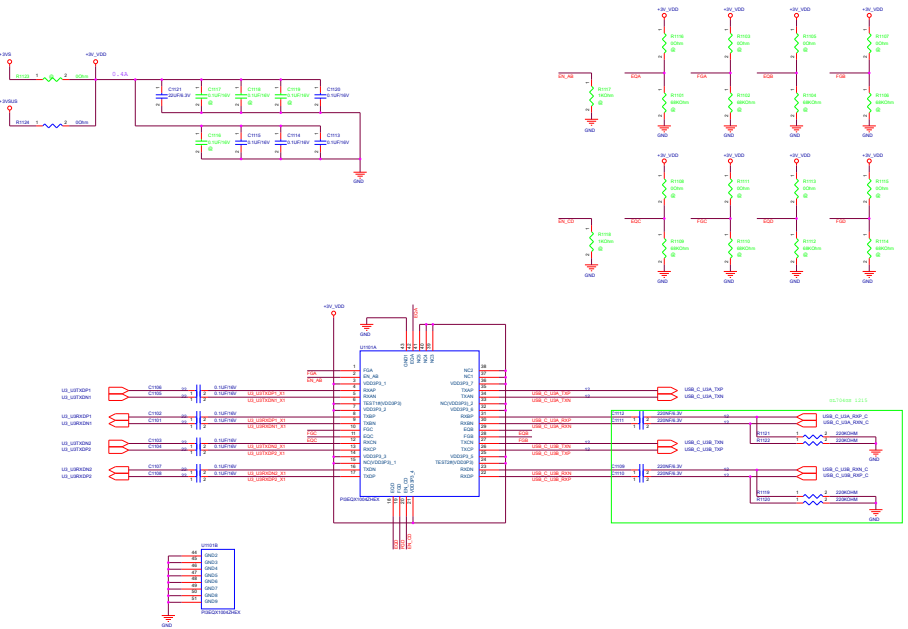
+VCCGT cap near CPU

47uF x3
22uF x7



Project Name: GL704GSM		Rev: R1.1
Title : CPU_POWER_CAP		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 10 of 103	

Main Board



	Equalizer setting(dB)
EQ A/B/C/D	@5Ghz
0(1k to Gnd)	10.9
R(Rext to Gnd)	6.7
F(Floating)	8.9
1(0 to VDD)	13.1

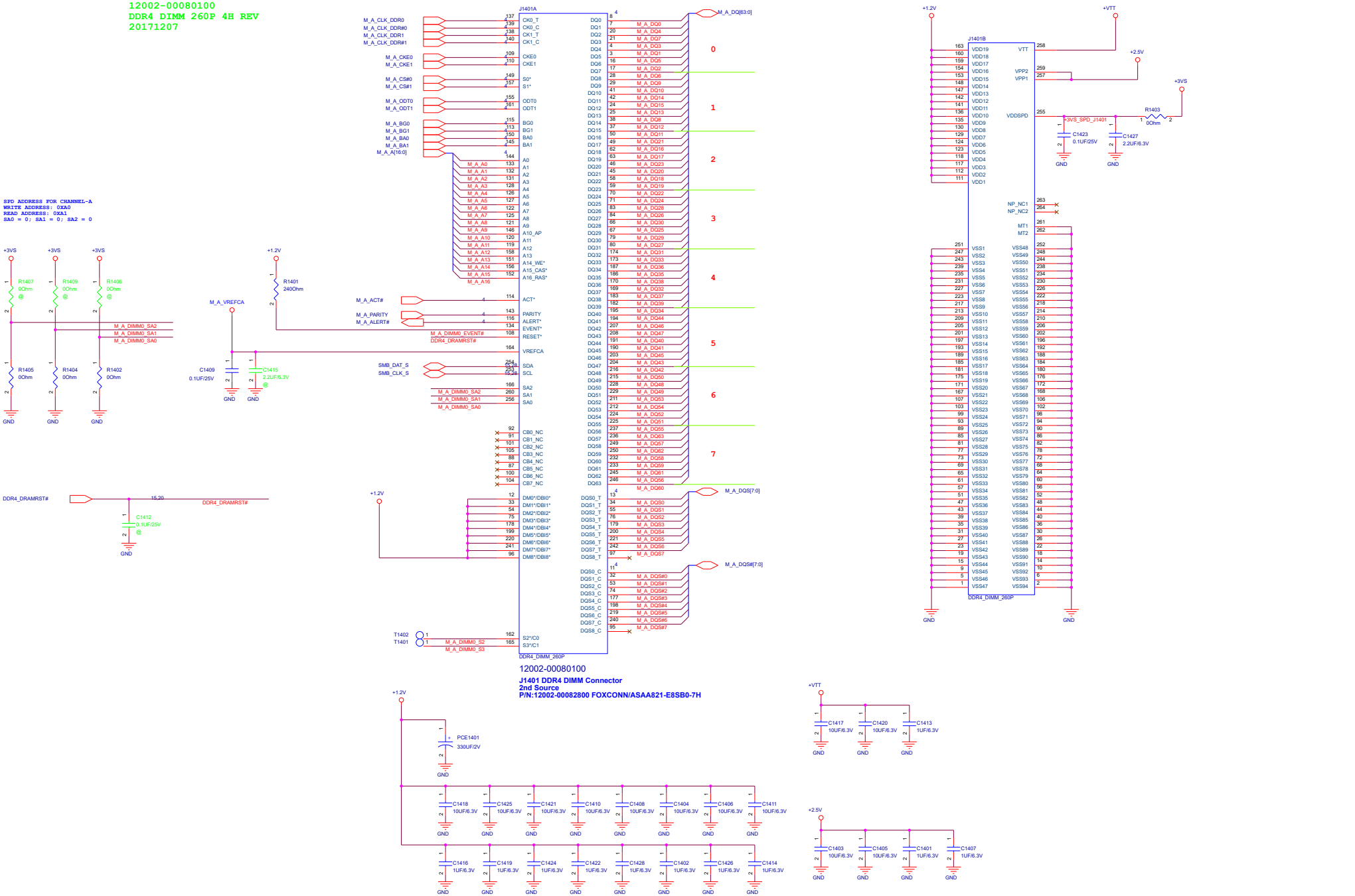
	Flat Gain setting
FG A/B/C/D	dB
0(1k to Gnd)	-3
R(Rext to Gnd)	-1.5
F(Floating)	0
1(0 to VDD)	+2

	Channel Enable setting
EN	With internal 300kohm pull-up Resister
0	Disable
1	Enable

Project Name	GL704GSM
Rev.	A1.1
Title :	TBT_Alpine-Ridge
Size: C	Dept.: ASUSTeK COMPUTER INC
	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 10 of 100

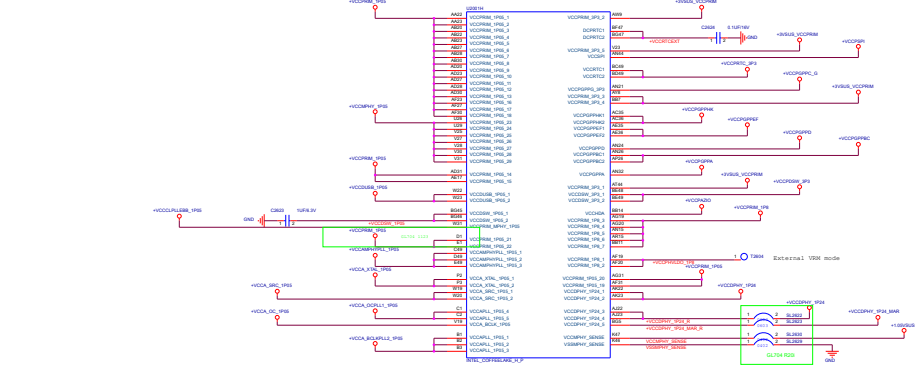
SODIMM CHA-DIMM0
BOT H8.0mm REV (J1401)

12002-00080100
DDR4 DIMM 260P 4H REV
20171207



12002-00080100
J1401 DDR4 DIMM Connector
2nd Source
P/N:12002-00082800 FOXCONN/ASAA821-E8SB0-7H

ASUS	Project Name: GL704GSM		Rev: R1.1
Title :	DIM_DDR4 SO-DIMM A(0)		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 14 of 103		



Refer to CNL-H PCH EDS R1.0 (Doc.571182)

Table 8-1. Power Descriptions for PCH in CNL-H

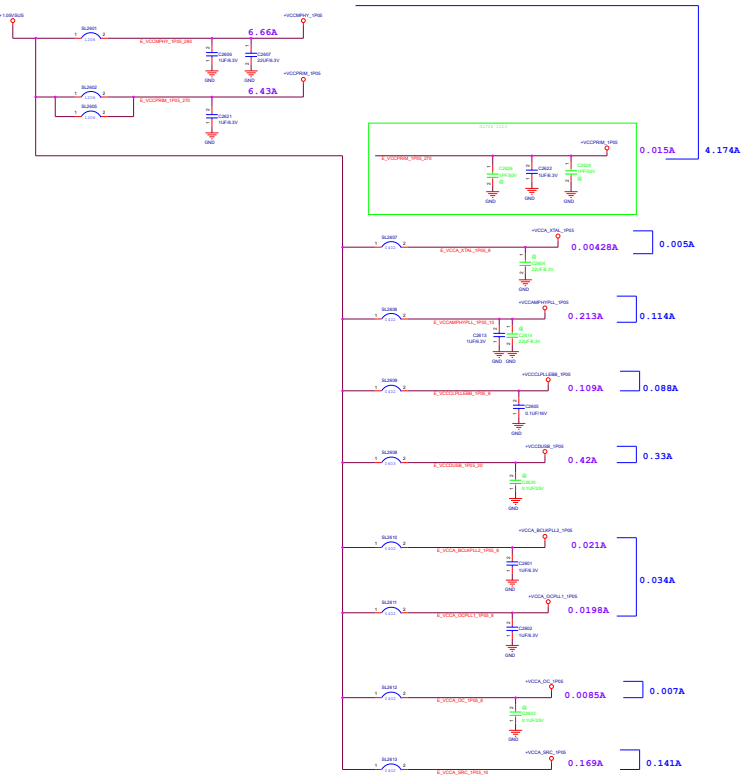
Name	Description
VCCPHVLDO_1P8	**1.8V Primary Well.** On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.

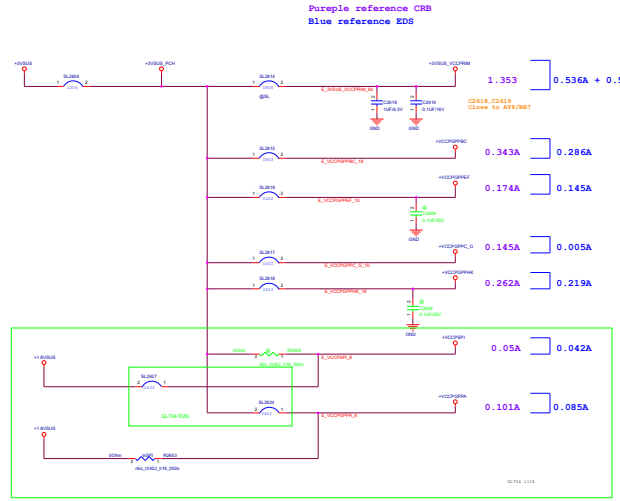
VCCPHVLDO_1P8	AF19
VCCPHVLDO_1P8	AF20

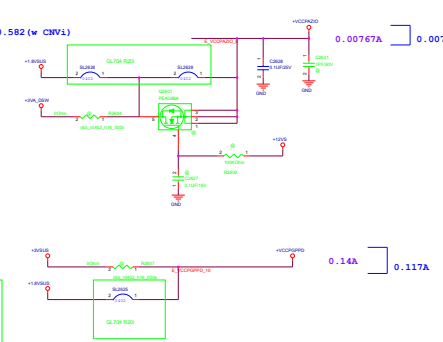
VCCDPHY_1P24	**1.24V for CNVi logic**. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Cannon Lake -U/Y PDG for implementation details.

GPIO Voltage Level

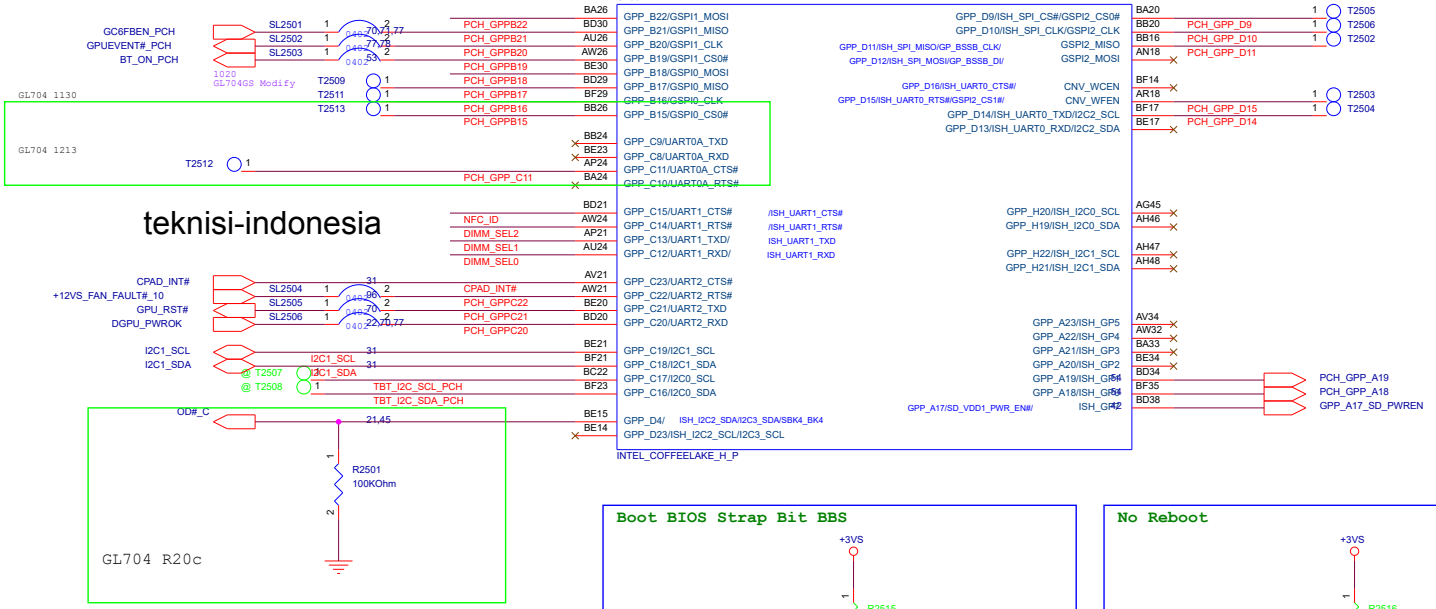
Group	Power pin	Power option	Power plane
GPP_A	VCCGPPA	1.8V or 3.3V	+3VSUS
GPP_B	VCCGPPBC	1.8V or 3.3V	+3VSUS
GPP_C	VCCGPPBC	1.8V or 3.3V	+3VSUS
GPP_D	VCCGPPD	1.8V or 3.3V	+1.8VSUS
GPP_E	VCCGPPEF	1.8V or 3.3V	+3VSUS
GPP_F	VCCGPPEF	1.8V or 3.3V	+3VSUS
GPP_G	VCCGPPG_3P3 VCCPRIM_1P8	Dynamic voltage to be config SDIO	+3VSUS
GPP_H	VCCGPPHK	1.8V or 3.3V	+3VSUS
GPP_I	VCCPRIM_3P3	3.3V Only	+3VSUS
GPP_J	VCCPRIM_1P8	1.8V Only	+1.8VSUS
GPP_K	VCCGPPHK	1.8V or 3.3V	+3VSUS
GPD	VCCDSW_3P3	3.3V Only	+3VA_DSW



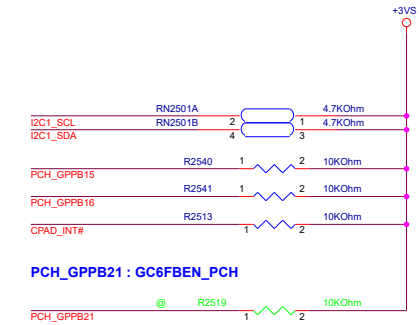




ASUS	Project Name: GL704GSM		Rev: 0.1
Title : 026_PCH_POWER,GND			
Size: D	Dept.: ASUSTEK COMPUTER INC	Engineer:	Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet: 26 of 193		

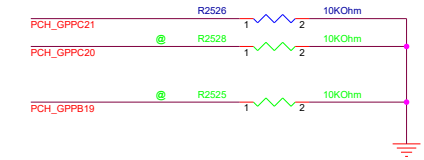


GL704 0111

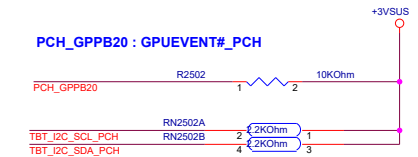


PCH_GPPB21 : GC6FBEN_PCH

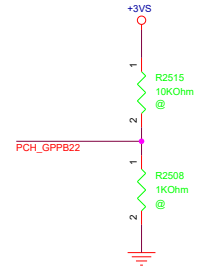
PCH_GPPC21 : GPU_RST#
PCH_GPPC20 : DGPU_PWROK



PCH_GPPB20 : GPUEVENT#_PCH

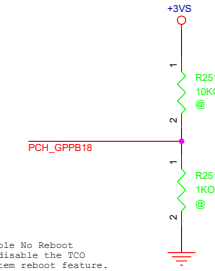


Boot BIOS Strap Bit BBS



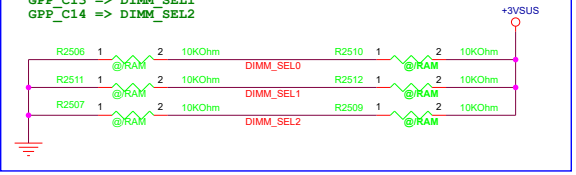
PCH_GPPB22: weal internal pull down	
PU	LPC
PD	SPI (Default)

No Reboot



PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable (Default)

Onboard Memory PCB-ID:
GPP_C12 => DIMM_SEL0
GPP_C13 => DIMM_SEL1
GPP_C14 => DIMM_SEL2

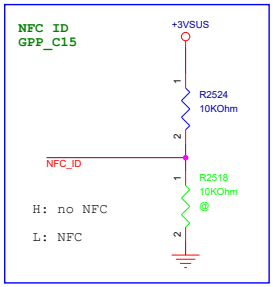


	Hynix(2Gb)	XXX (2Gb)	Micron(2Gb)
DIMM_SEL0			
DIMM_SEL1			
DIMM_SEL2			

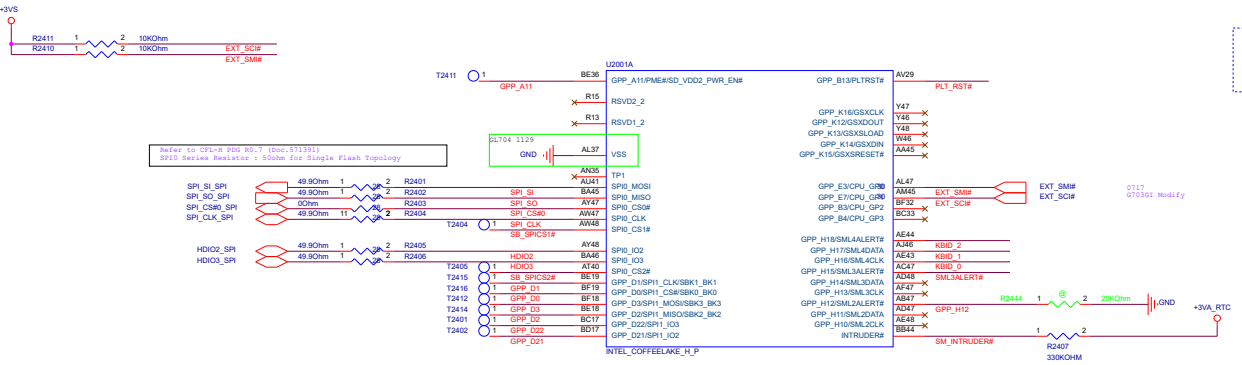
	US	UK	JP
KB_LANG_ID0 (KB pin33)	1	0	0
KB_LANG_ID1 (KB pin34)	0	0	1

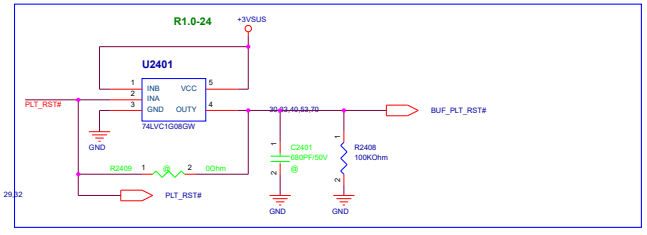
US:PIN 33 NC , PIN 34 GND
UK:PIN 33,34 GND
JP:PIN 33 GND , PIN 34 NC

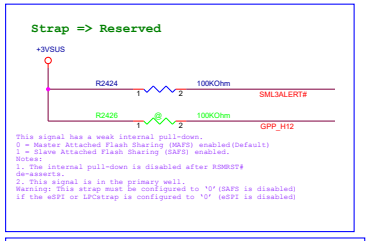
NFC ID
GPP_C15



ASUS	Project Name: GL704GSM		Rev: R1.1
Title : PCH_GPIO			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018		Sheet 25 of 103	

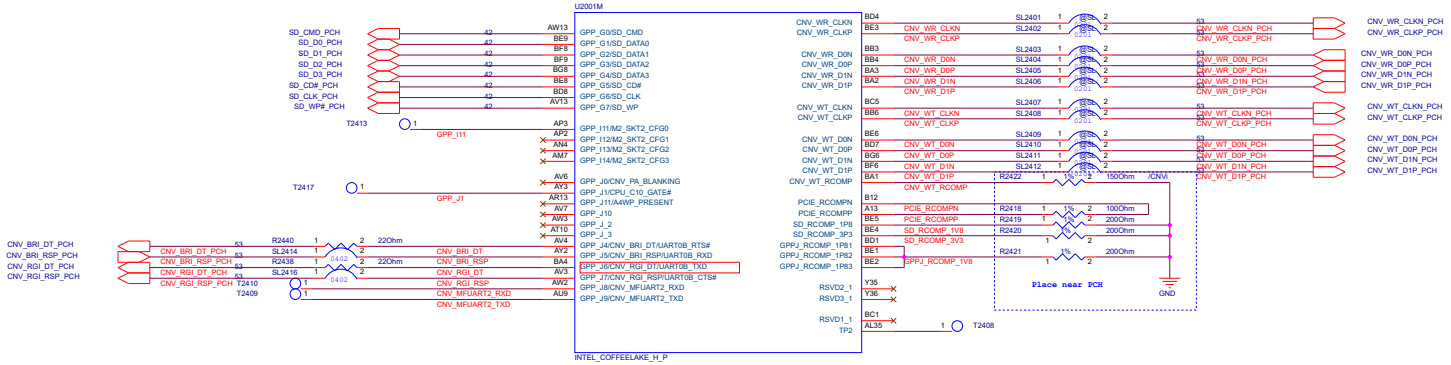


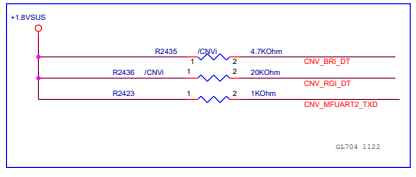




PCH Side (HW 請依照此表格做設計判斷)				
Code	ROG RGB KB Type	KBID 2 (GPP_H18)	KBID 1 (GPP_H17)	KBID 0 (GPP_H16)
0x00	Non-RGB	H	H	H
0x01	RGB per Region via QWER/WASD modes	H	H	L
0x02	RGB per Region via 4 zones	H	L	H
0x03	RGB per key	H	L	L

5. 需請 BIOS RD 在 KB ID 讀取的部分，額外加入 Reverse code，以符合第 1 點 table





GPP_J4(CNV_BRI_DT):
This signal has a weak internal pull down.
0 = 38.4MHz XTAL frequency selected.(Default)
1 = 24MHz XTAL frequency selected.

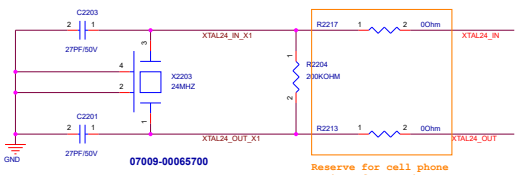
(MOW39)
Pin Strap for XTAL frequence selection.
An external 4.7K PU to VCC(1.8V or 3.3V) is required
on this strap for PCH 24 MHZ XTAL operation

GPP_J6(CNV_RGI_DT):
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
(Intel FAE)
RGI_DT has an automatic detect CNVi mechanism,
please do not use external PD.
The CRF has an internal strong 1K PD already.
Do not leave this pin float,
if CNVi is not used, it still need a 20K ohm PU.

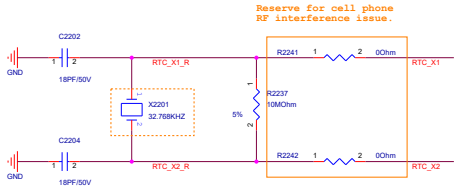
GPP_J9/CNV_MFUART2_TXD:
The signal has a weak internal pull-down
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

ASUS	Project Name: GL704GSM		Rev: R1.1
Title : PCH_SPI			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 24 of 103		

XTAL 24MHz



RTC CRYSTAL 32.768KHz

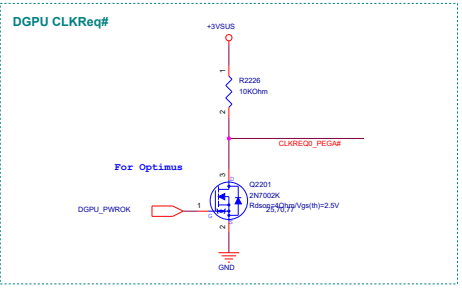


X2201: 32.768KHZ +/-20ppm/12.5pF (3215)

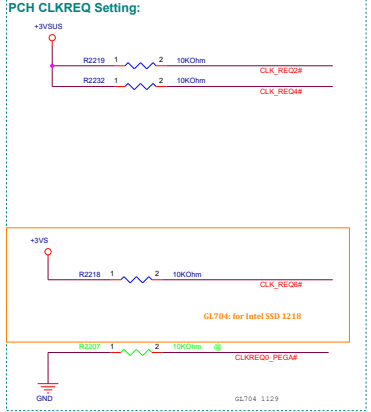
1st: P/N:07009-00111800 SIWARD/XTL721-M99-113

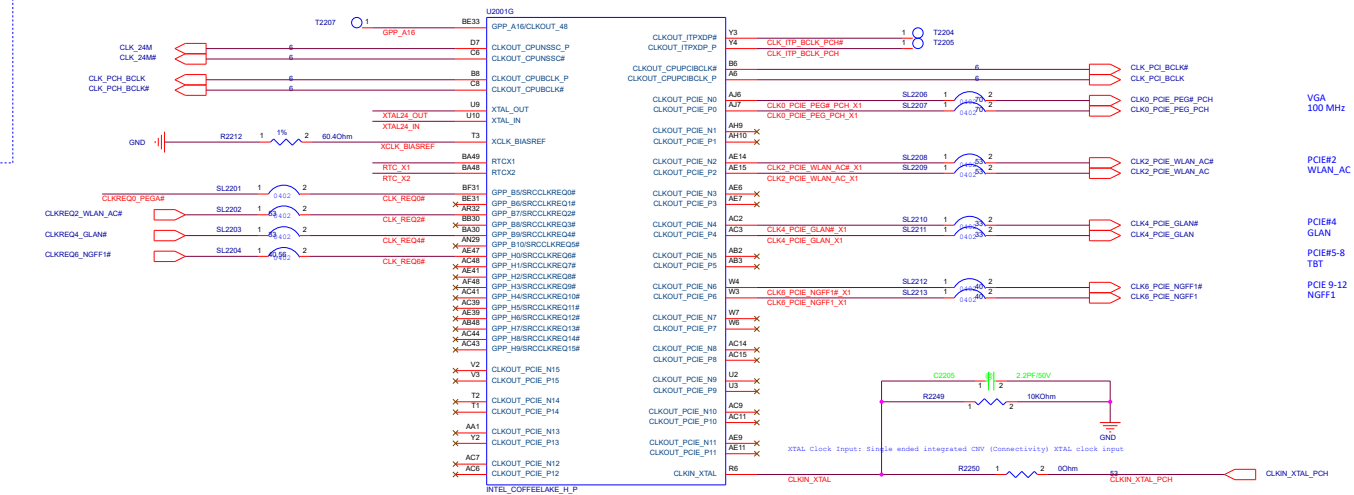
2nd: P/N:07009-00112500 TXC/9H03200052

DGPU CLKReq#



PCH CLKREQ Setting:





ASUS	Project Name: GL704GSM		Rev: R1.1
Title : PCH_CLK,LPC,USB3			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 22 of 103		

GL704GS Port Assignment

USB Setting

USB 2.0	
USB2_01	
USB2_02	
USB2_03	USB3.0 typc A
USB2_04	USB3.0 typc A
USB2_05	USB3.0 typc A
USB2_06	USB3.0 typc A
USB2_07	
USB2_08	
USB2_09	Camera
USB2_10	N-Key + KB BL control
USB2_11	
USB2_12	
USB2_13	TypeC
USB2_14	BT

USB 3.0	
USB3_01	
USB3_02	
USB3_03	USB3.0 typc A
USB3_04	USB3.0 typc A
USB3_05	USB3.0 typc A
USB3_06	USB3.0 typc A
USB3_07	
USB3_08	

PCIE/SATA Function define

		Function
PCIE-01	(USB3#7)	USB3 Card Reader
PCIE-02	(USB3#8)	
PCIE-03	(USB3#9)	
PCIE-04	(USB3#10)	
PCIE-05		TBT (x4)
PCIE-06		
PCIE-07		
PCIE-08		
PCIE-09		PCIE SSD (x4)
PCIE-10		
PCIE-11	(SATA-0a)	
PCIE-12	(SATA-1a)	SATA SSD

		Function
PCIE-13	(SATA-0b)	SATA HDD
PCIE-14	(SATA-1b)	
PCIE-15	(SATA-2)	GLAN
PCIE-16	(SATA-3)	WLAN-AC
PCIE-17	(SATA-4)	SATA SSD
PCIE-18	(SATA-5)	PCIE SSD (x4)
PCIE-19	(SATA-6)	
PCIE-20	(SATA-7)	
PCIE-21		PCIE SSD (x4)
PCIE-22		
PCIE-23		
PCIE-24		

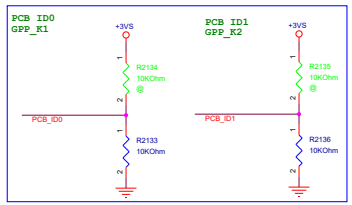
	Function
CLKREQ-0	DGPU
CLKREQ-1	
CLKREQ-2	WLAN-AC
CLKREQ-3	
CLKREQ-4	GLAN
CLKREQ-5	TBT
CLKREQ-6	PCIE SSD
CLKREQ-7	PCIE SSD
CLKREQ-8	PCIE SSD
CLKREQ-9	PCIE SSD
CLKREQ-10~15	

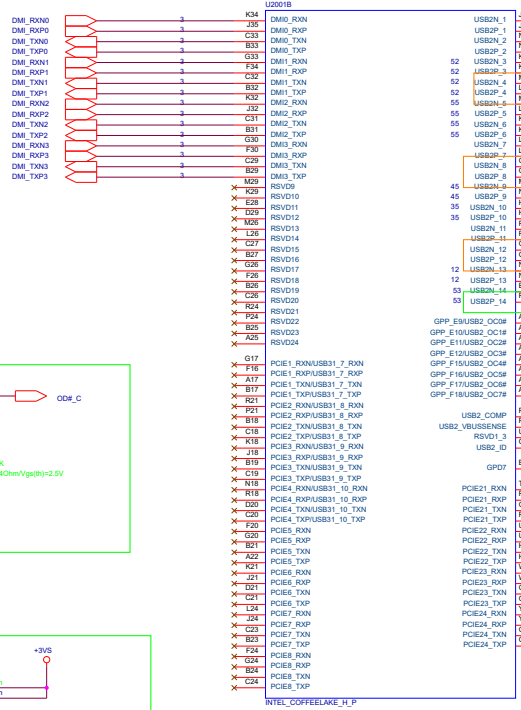
Design IP

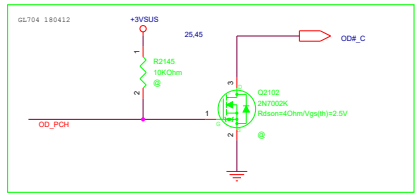
USB2.0	Devices Assign	
USB2.0 #1	USB3.1 Typc C (port1)	
USB2.0 #2	USB3.1 Typc C (port2)	
USB2.0 #3	USB3.0 Typc A (port1)	charger
USB2.0 #4	USB3.0 Typc A (port2)	
USB2.0 #5	USB3.0 Typc A (port3)	
USB2.0 #6	USB3.0 Typc A (port4)	
USB2.0 #7	Card Reader	
USB2.0 #8	XBOX WLAN	
USB2.0 #9	Camera	
USB2.0 #10	N-Key + KB BL control	
USB2.0 #11	BT	
USB2.0 #12	Tobii IS4	
USB2.0 #13	TBT	
USB2.0 #14	Macro Key	

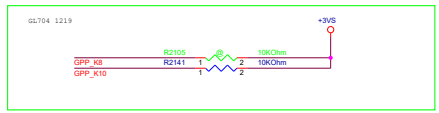
Design IP

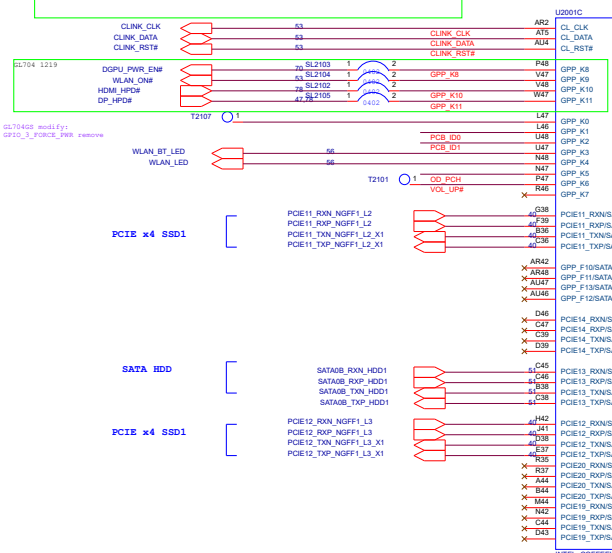
HSIO	HM370	QM370	CM246	IRST	Devices Assign	
0	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #1		port1) USB3.1 Typ C	
1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #2		port2) USB3.1 Typ C	
2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #3		port3) USB3.0 Typ A	
3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #4		port4) USB3.0 Typ A	
4	USB3.1 Gen1 #5	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #5		port5) USB3.0 Typ A	only for QM370 / CM246
5	USB3.1 Gen1 #6	USB3.1 Gen1/Gen2 #6	USB3.1 Gen1/Gen2 #6		port6) USB3.0 Typ A	only for QM370 / CM246
6	USB3.1 Gen1 #7	USB3.1 Gen1 #7	USB3.1 Gen1 #7		CR (USB3.0 / PCIE)	
7	USB3.1 Gen1 #8	USB3.1 Gen1 #8	USB3.1 Gen1 #8			
8	NA	USB3.1 Gen1 #9	USB3.1 Gen1 #9			
9	NA	USB3.1 Gen1 #10	USB3.1 Gen1 #10			
10	NA	PCIE #5	PCIE #5			
11	NA	PCIE #6	PCIE #6			
12	NA	PCIE #7	PCIE #7			
13	NA	PCIE #8	PCIE #8			
14	PCIE #9	PCIE #9	PCIE #9			
15	PCIE #10	PCIE #10	PCIE #10			
16	PCIE #11	PCIE #11	PCIE #11			
17	PCIE #12	PCIE #12	PCIE #12			
18	PCIE #13	PCIE #13	PCIE #13			
19	PCIE #14	PCIE #14	PCIE #14			
20	PCIE #15	PCIE #15	PCIE #15			
21	PCIE #16	PCIE #16	PCIE #16			
22	PCIE #17	PCIE #17	PCIE #17			
23	PCIE #18	PCIE #18	PCIE #18			
24	PCIE #19	PCIE #19	PCIE #19			
25	PCIE #20	PCIE #20	PCIE #20			
26	PCIE #21	PCIE #21	PCIE #21			
27	PCIE #22	PCIE #22	PCIE #22			
28	PCIE #23	PCIE #23	PCIE #23			
29	PCIE #24	PCIE #24	PCIE #24			

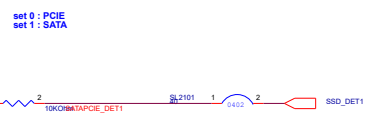


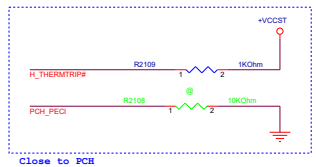












ASUS	Project Name: GL704GSM		Rev: R1.1
Title :	PCH_PCIE,SATA,USB2,MISC		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet: 21	of: 103	

Main Board

HD Audio

ACZ_SDOUT_AUD
ACZ_SYNC_AUD
ACZ_BCLK_AUD
ACZ_RST#_AUD

33OHM x4 (RN2004D, RN2004C, RN2004B, RN2004A)

ACZ_SDOUT_AUD_X1
ACZ_SYNC_AUD_X1
ACZ_BCLK_AUD_X1
ACZ_RST#_AUD_X1

C2007 10PF/50V
C2005 10PF/50V
C2004 10PF/50V
C2009 10PF/50V

Refer to CFL-H PDG R1.0 (Doc. 571391),section 31.1.2.1 reserve C2007,C2005,C2004,C2009,C3603

20171228

RF requirement

GND

ACZ_SDOUT:
(1) PCH: Internal PD 20k ohm, VIL=0.35V, VIH=0.65~3.3V
(2) ALC295:VIL<0.4*3.3V, VIH>0.6*3.3V

+VCCPAZIO

20180112

R2005 2.2KOhm
R2223 1 5OHM
R2002 1KOhm
R2006 330Ohm

Q2002B EM6K1-G-T2R
Q2002A EM6K1-G-T2R
Q2201_D

ACZ_SDOUT_AUD_X1

PCH_SPI_OV

ACZ_SDOUT is a signal used for Flash Descriptor security Override/ME debug mode
HIGH : get overrideen, LOW : disable override

GND

Refer CFL-H PDG(Doc.571391), Page 381, 20K ohm for RTC_RST# and SRTC_RST#

+3VA_RTC

R2024 1 20KOhm RTC_RST# → RTC_RST#

C2002 2.2UF/6.3V
JRST2001 SGL_JUMP

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)

R2008 1 20KOhm SRTC_RST#

C2003 1UF/6.3V
JRST2002 SGL_JUMP

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

GND

RTC battery

+V3.3A_RTC GENERATION

+3VA
RTC Max=3.2V
+RTCBAT
SL2016
3.3A_RTC_D
+RTC_BAT
R2040 45.3KOhm 1%
D2001 BAT54CW
RTC_BAT
+3VA_RTC
C2001 1UF/6.3V
C2006 0.1UF/16V
BAT2001 SIDE1 SIDE2
WTOB_CON_2P
R2023 1 5% 2 1KOhm
GND

12G17100002C

BAT2001 RTC BATTERY Connector

2nd Source: P/N:12017-00020200 ENTERY/3802K-F02N-10R

ACZ_SDIN0_AUD

ACZ_BCLK_AUD_X1
ACZ_SDIN0_AUD
ACZ_SDOUT_AUD_X1
ACZ_SYNC_AUD_X1
ACZ_RST#_AUD_X1

GL704 R20c

AUD_AZACPU_SDO
AUD_AZACPU_SDI
AUD_AZACPU_SCLK

R2060 1 33R 2 30Ohm HDACPU_SDO
R2061 1 33R 2 30Ohm HDACPU_SCLK

M.2_BT_PCMCLK
M.2_BT_PCMIN
M.2_BT_PCMOUT_CLKREQ0
M.2_BT_PCMFRM_CRF_RST_N

SL2006 SL2007 SL2008 SL2009 0402
PCH_GPD8 PCH_GPD7 PCH_GPD2 PCH_GPD5

GPP_C2_BT_UART_WAKE_N
SMB_CLK
SMB_SDA
PCH_GPPC5_WLAN_WAKE

To SPD, XDP

RTC_RST#
SRTC_RST#
PM_PWROK_X1
PM_RSMRST#_X1
DPWROK_R

SML1_CLK
SML1_DAT

U2001D

HDA_BCLK/I2S0_SCLK
HDA_SDI0/I2S0_RXD
HDA_SDO/I2S0_TXD
HDA_SYNC/I2S0_SFRM
HDA_RST#/I2S1_SCLK
HDA_SDI1/I2S1_RXD
I2S1_TXD/SNDW2_DATA
I2S1_SFRM/SNDW2_CLK
HDACPU_SDO
HDACPU_SDI
HDACPU_SCLK
GPP_D8/I2S2_SCLK
GPP_D7/I2S2_RXD
GPP_D6/I2S2_TXD/MODEM_CLKREQ
GPP_D5/I2S2_SFRM/CNV_RF_RESET#
GPP_D20/DMIC_DATA0/SNDW4_DATA
GPP_D19/DMIC_CLK0/SNDW4_CLK
GPP_D18/DMIC_DATA1/SNDW3_DATA
GPP_D17/DMIC_CLK1/SNDW3_CLK
RTCRST#
SRTCRST#
PCH_PWROK
RSMRST#
DSW_PWROK
GPP_C2/SMBALERT#
GPP_C3/SMBCLK
GPP_C1/SMBDATA
GPP_C5/SML0ALERT#
GPP_C9/SML0CLK
GPP_C4/SML0DATA
GPP_B23/SML1ALERT#/PCHHOT#
GPP_C8/SML1CLK
GPP_C7/SML1DATA

INTEL_COFFEELAKE_H_P

GPP_A12/BM_BUSY#/SH_GPI0

SX_EXIT_HOLDOFF#
GPP_A8/CLKRUN#
GPD11/LANPHYPC
GPD8/SLP_WLAN#
DRAM_RESET#
GPP_B2/VRALERT#
GPP_B1/GSPI1_CS1#/TIME_SYNC1
GPP_B0/GSPI0_CS1#
GPP_K17/ADR_COMPLETE
GPP_B11/I2S_MCLK
SYS_PWROK
PM_SYSPWROK_X1
WAKE#
GPD8/SLP_A#
SLP_LAN#
GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
GPD6/SUSCLK
GPD0/BATLOW#
GPP_A15/SUSACK#
GPP_A13/SUSWARN#/SUSPWRDNACK
GPD2/LAN_WAKE#
GPD1/ACPRESENT
SLP_SUS#
GPD3/PWRBTN#
SYS_RESET#
GPP_B14/SPKR
CPUPWRGD
ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK

CLKRUN#
LAN_PWREN
SLP_WLAN#
DRAMRST#_x4
PCH_GPP_B2
PCH_GPP_B3
PCH_GPP_B0
PM_SYSPWROK_X1
PCIE_WAKE#_X1
SLP_A#
SLP_LAN#
SLP_S0#
SLP_S3#
SLP_S4#
SLP_S5#
SUS_CLK
PM_BATLOW#
PM_SUSACK#
ME_SusPwrDnAck
LAN_WAKE#_X1
ME_AC_PRESENT_X1
PM_SLP_SUS#
PWRBTN#_X1
PM_SYSRST#_PCH
H_CPUPWRGD
PCH_ITP_PMODE
PCH_JTAGX
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_TCK

SL2001 0402 PM_CLKRUN#
GL704 1117, reserved for eSPI

T2012
T2015
GL704GS Modify : TBT remove
PCH_GPP_B2
PCH_GPP_B0

SL2014 0402 PCIE_WAKE#
SL2002 SL2003 PM_SUSB# PM_SUSC#
SL2015 0402 SUS_CLK
PCH_SUSACK#
SUSWARN#
SL2005 PM_SLP_SUS# PM_PWRBTN#
SL2010 XDP_TCLK_CPU
SL2011 XDP_TMS_CPU
SL2012 XDP_TDO_CPU
SL2013 XDP_TDI_CPU

---

eSPI or LPC

+3VSUS
GL704 1213
R2037 1KOhm /eSPI
R2038 1KOhm
PCH_GPPC5

PCH_GPPC5: weak internal pull down	
PU	eSPI
PD	LPC (default)

Top Swap Override

+3VS
R2050 10KOhm
R2049 1KOhm
PCH_GPPB14

PCH_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

SMBUS

+3VSUS
R2044 1 2.2K 2 150KOHM SML1ALERT#

RN2002A 1 2.2KOHM 2
RN2002B 3 2.2KOHM 4 SMB_SDA
RN2002C 5 2.2KOHM 6 SMB_CLK
RN2002D 7 2.2KOHM 8

RN2001A 1 2.2KOHM 2
RN2001D 7 2.2KOHM 8 SML0_CLK
RN2001B 3 2.2KOHM 4 SML1_DAT
RN2001C 5 2.2KOHM 6 SML0_DAT
SML1_CLK

Boundary Scan

PCH_JTAG_TMS T2008
PCH_JTAG_TDO T2007
PCH_JTAG_TDI T2011
PCH_JTAG_TCK T2009
PCH_ITP_PMODE T2010
PM_SYSRST#_PCH T2004
PM_RSMRST#_X1 T2005
SML1ALERT# T2006

For power sequence measurement

DPWROK_R
ME_SusPwrDnAck
SLP_S4#
PWRBTN#
ME_AC_PRESENT_X1
PM_PWROK_X1
PM_RSMRST#_X1
PM_SYSPWROK_X1

PM_PWROK,PM_RSMRST#: previous platform solution.

ME_PWROK,ME_AC_PRESENT: reserved for test.

+3VSUS +3VA_DSW

R2018 R2032 R2033 R2034 10KOhm

09'MoW04:
Optional if ME FW is Ignition FW

PM_SYSPWROK
ALL_SYSTEM_PWRGD
PM_PWROK
PM_RSMRST#
ME_AC_PRESENT

R2019 10KOhm PM_SYSPWROK_X1
R2036 0Ohm
R2013 10KOhm PM_PWROK_X1
R2014 1KOhm PM_RSMRST#_X1
R2015 10KOhm ME_AC_PRESENT_X1
1N4148WS D2002

R2017 10KOhm R2016 10KOhm

D2002: Prevent EC drive high, SUS_PWRGD sink low in S5-->G3.

Power failure solution (S0-->G3,S5-->G3):

R1.0-34

D2004 IMVP8_PWRGD PM_SYSPWROK_X1 PM_PWROK_X1 BAT54CW

D2005 3VA_DSW_PWRGD PM_RSMRST#_X1 DPWROK_R BAT54CW

Power failure solution (S0-->G3,S5-->G3):

DPWROK_EC R2020 10KOhm DPWROK_R

R2021 10KOhm

C2020 100PF/50V
C2021 100PF/50V
For EMI

+1.2V R2001 1% 470Ohm

DRAMRST# 0.1UF/25V C2008 SL2004 DDR4_DRAMRST#

3VA_DSW_PWRGD D2006 PM_SUSACK# BAT54CTB ME_AC_PRESENT_X1

Change D2040 to 10Kohm if mount D2006

Deep SX discharge (S0-->DSX,S5-->DSX)

R1.1-03

Project Name	GL704GSM	Rev
Title :	PCH_HDA,SMB,SYS PWR,JTAG	R1.1
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 20 of 103	

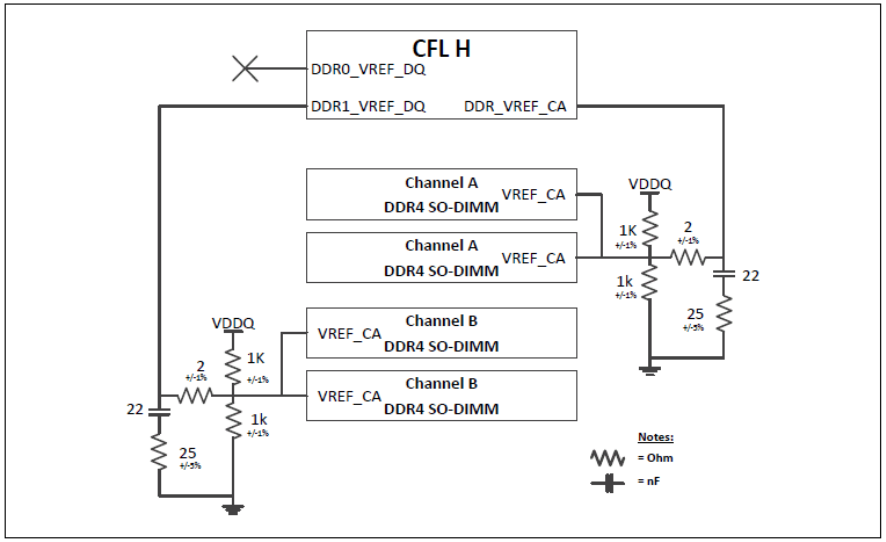
	Project Name **GL704GSM**	Rev R1.1

Title : *****

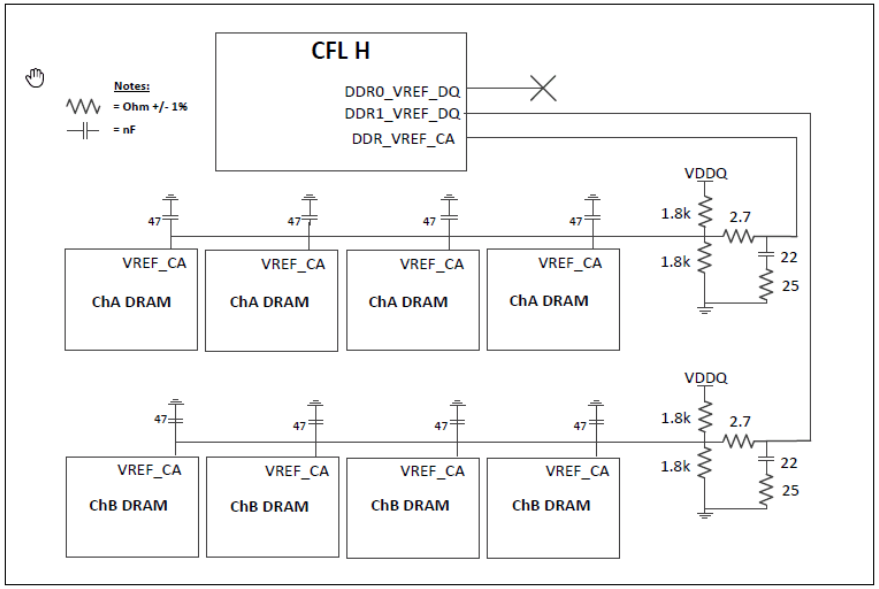
Size B	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Gaming RD4 EE1

Date: Friday, July 27, 2018	Sheet	19	of	103

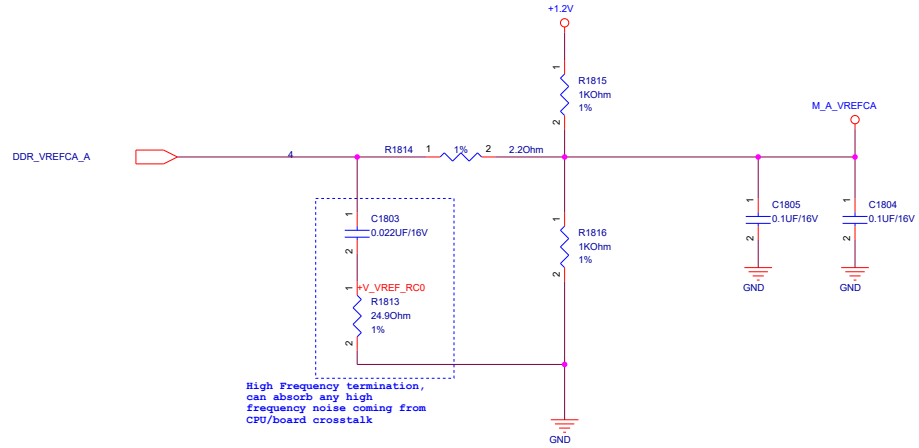
CFL H DDR4 SO-DIMM V_{REF-CA} Overview



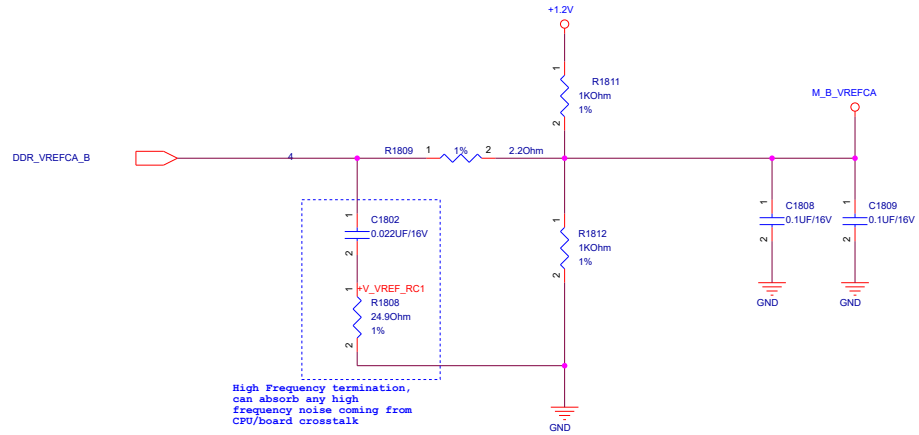
CFL H DDR4 x16 Memory Down V_{REF-CA} Overview



Vref for CHA_DIMM0



Vref for CHB_DIMM0

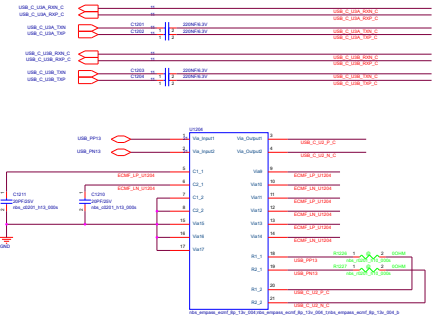


Project Name: GL704GSM		Rev: R1.1
Title : DIM_CA/DQ Voltage		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 18 of 103	

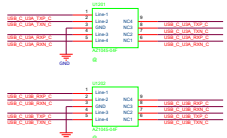
SODIMM CHB-DIMM1
TOP H4.0mm REV (J1701)

SODIMM CHA-DIMM1
TOP H4.0mm STD (J1601)

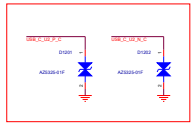
PCH USB3.0 / USB2.0



USB3.0 ESD-Protection

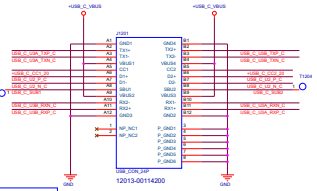


USB2.0 ESD-Protection



R1.5-02-0215

TYPE-C Connector



12013-00114200

U4702 & U4703 ESD PROTECTION

1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

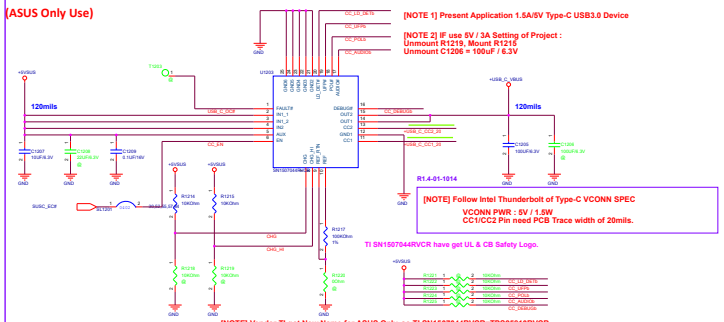
D4701 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

TI CC Logic SN1507044RVCR = TPS25810RVCR, DFP (Host), 5V / 1.5A

(ASUS Only Use)



[NOTE 1] Present Application 1.5A/5V Type-C USB3.0 Device

[NOTE 2] IF use 5V / 3A Setting of Project :
Unmount R1219, Mount R1218
Unmount C1206 = 100uF / 6.3V

120mils

120mils

R1.4-01-1014

[NOTE] Follow Intel Thunderbolt of Type-C VCONN SPEC
VCONN PWR : 5V / 1.5W
CC1/CC2 Pin need PCB Trace width of 20mils.

TI SN1507044RVCR have get UL & CB Safety Logo.

[NOTE] Vendor TI got New Name for ASUS Only, so TI SN1507044RVCR=TPS25810RVCR.
Please Follow Design IP : TYPE-C CC Logic IC need use P/N:06050-00280000 TI/SN1507044RVCR

Set CC
I limit = 1.7A

Table 3. USB Type-C Current Advertisement

CHG	CHG_HI	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.7 A	NA
1	1	3 A	3.4 A	1.95 A

6.7.2 Thunderbolt VCONN Source Electrical Requirements

The Thunderbolt Power Provider VCONN Electrical Parameters are specified Table 6-3.

Table 6-3. Thunderbolt VCONN Source Electrical Requirements

Parameter	Description	Min	Typ	Max	Units	Note
VSrc_Swap	Minimum voltage provided to port in suspend	4.75	5	5.5	V	7.5mA min
VSrc_Active[1]	Minimum power provided to port in Active	4.75	5	5.5	V	1.5W min

[1] Note: Thunderbolt Specific Requirement

3.5.3 VCONN Requirements

The Thunderbolt Active Cable shall be powered from VCONN not VBUS.

The USB Type-C full featured active cable shall consume 1 W maximum from VCONN by default and 1.5W maximum from VCONN when in Thunderbolt or DisplayPort Alternate Modes. Ra shall be connected to VCONN on initial connection.

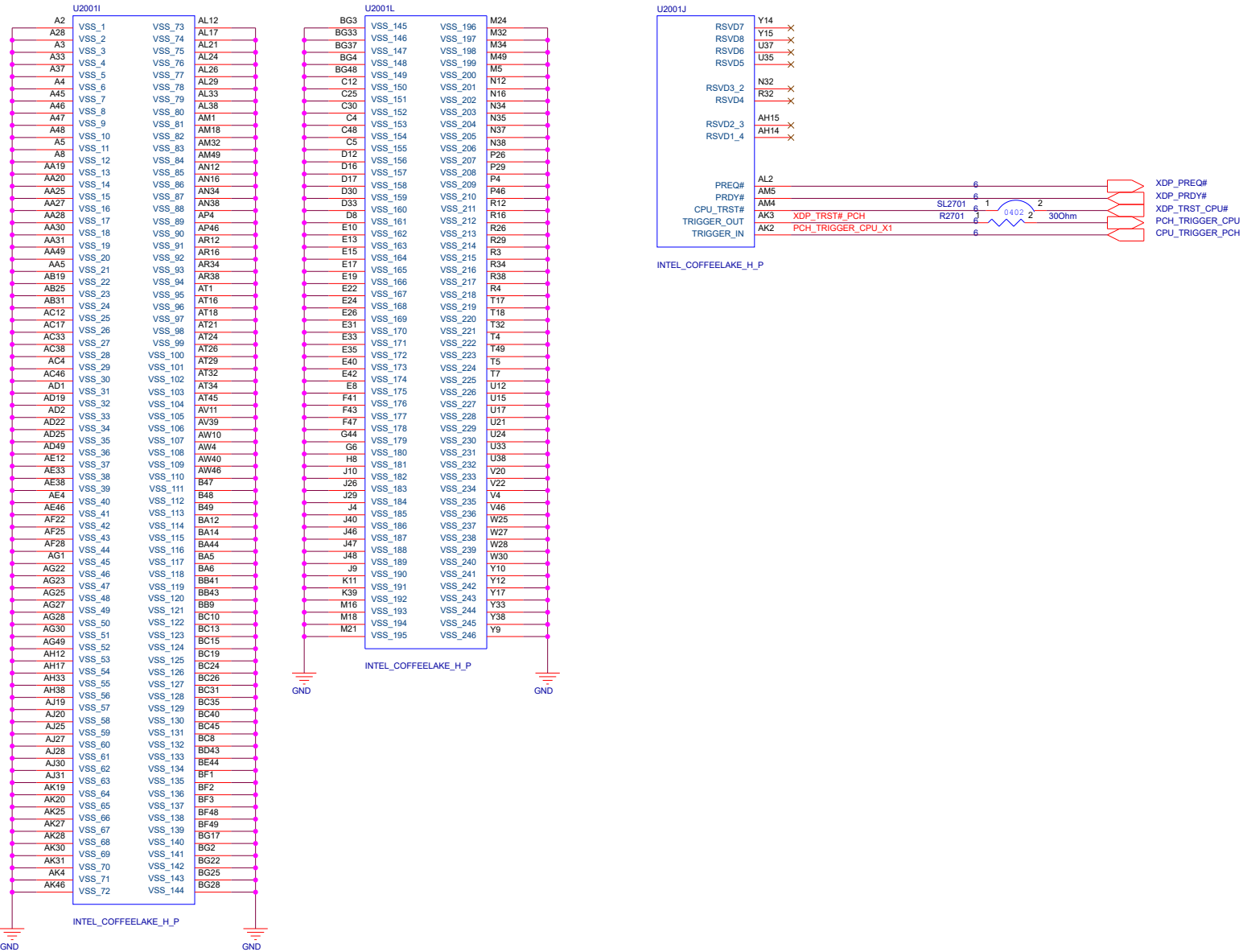
The Thunderbolt Active cable shall respond to SOP' and SOP'' messages. The cable shall respond to SOP' from the side of the cable which receives VCONN from the USB Type-C connector. The cable responds to SOP'' from the side which does not receive VCONN. The cable shall continue to respond to SOP' and SOP'' after a ***VCONN_Swap***.

[NOTE] PCH USB3.0 & Asmedia USB3.1 Co-layout of Design Rule :

1. Co-layout 元件擺置，盡量靠TYPE-C Connector 越近越好。
2. Co-layout Y-型走線要越短越好.

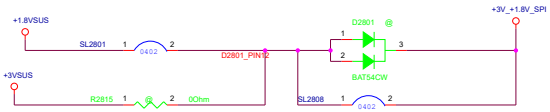
ASUS	Project Name: GL704GSM	Rev: 0.1
Title : TBT_TPS65982&Type C		
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 12 of 103	

ASUS	Project Name: GL704GSM	Rev: R1.1
Title : TBT_PWR		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 13 of 103	



ASUS	Project Name: GL704GSM	Rev: R1.1
Title : PCH_POWER,GND		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 27 of 103	

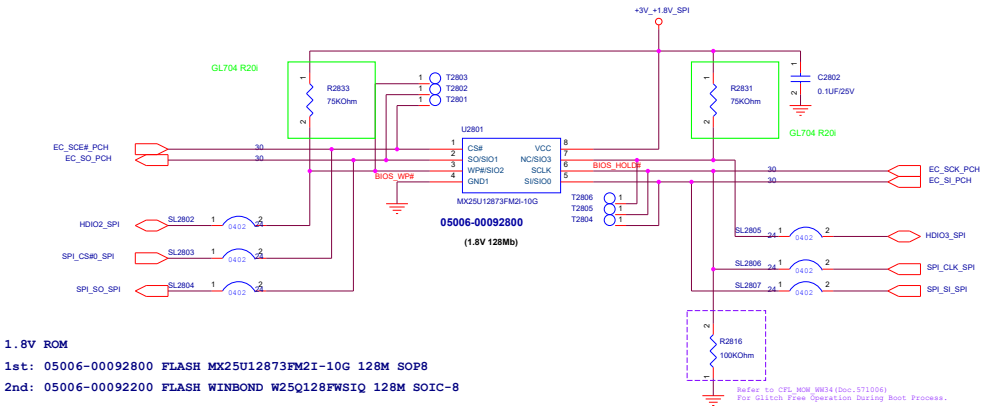
SPI Power



SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L

2nd: 05006-00093100 FLASH GD25B127DSIG

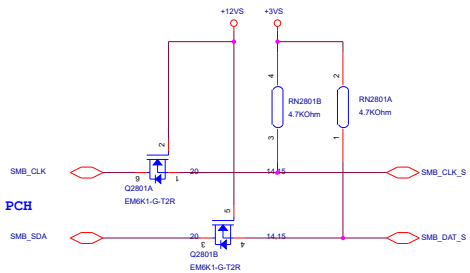


1.8V ROM

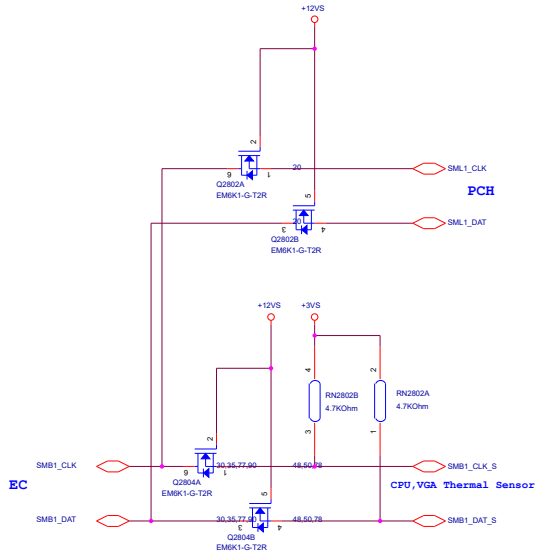
1st: 05006-00092800 FLASH MX25U12873FM2I-10G 128M SOP8

2nd: 05006-00092200 FLASH WINBOND W25Q128FWSIQ 128M SOIC-8

SMBus Interface



System Management Interface



Project Name: GL704GSM		Rev: R1.1
Title: PCH_SPI ROM,OTH		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 28 of 103	

For power sequence measurement

+1.0V_VCCPLL ----------> R0809

H_VCCST_PWRGD ----------> R0620

ASUS	Project Name: GL704GSM	Rev: R1.1
Title : <Title>		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 29 of 103	

EC 8225

Only 3V Torlence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]

Can be adjusted to Open-Drain for port:

GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

ITE Version	ASUS P/N
IT8225VG/BX	06037-00260000

Power

R1.0-29

+3VS
+3VA_EC
+3VPLL
+3VACC
EC_AGND
C3002 0.1UF/16V
C3051 0.1UF/16V
C3052 0.1UF/16V
C3053 0.1UF/16V
C3054 0.1UF/16V
C3004 0.1UF/16V
C3005 0.1UF/16V
C3007 0.1UF/16V
C3001 0.1UF/16V
SL3005 0603
SL3006 0603
SL3007 0603

PU/PD

+1V8_AUD_DVDD
Q3003A EM6K1-G-T2R
Rdson=13Ohm/Vgs(th)=1.5V
EC_GPA7
AMP_SLEEP#
Q3003B EM6K1-G-T2R
Rdson=13Ohm/Vgs(th)=1.5V
GL704 1208

0Ohm /eSPI R3013 GL704 R20i
+1.8VSUS
SL3020 0402
+3VS
GL704 1116, reserved for eSPI
LCD_BACKOFF#
45
VCC_EC
+3VA_EC
+3VPLL
+3VACC

U3001

LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
CLK_KBCPCI_PCH
LPC_FRAME#
R3046 15Ohm LPC_AD0_R
R3047 15Ohm LPC_AD1_R
R3048 15Ohm LPC_AD2_R
R3049 15Ohm LPC_AD3_R
SL3004 22,44 LPC_FRAME# R
ESPI_RESET#
BUF_PLT_RST#
R3020 /eSPI 0Ohm
SL3023 0402
GL704 R20i
GL704 1116, reserved for eSPI
INT_SERIRQ
EXT_SMI#
EXT_SCI#
NKey_WRST
RC_IN#
EC_RST#
SL3024 0402
SERIRQ
EXT_SMI#
SL3016 0402
EC_GPB5
SL3025 0402
GL704 R20i
12/23 for N key
DGPU_LIMIT
EC_SCK_PCH
R3019 78
T3010
EC_SCK
EC_GPG6
EC_SO_PCH
EC_SI_PCH
EC_SCE#_PCH
R3021 15Ohm
R3010 15Ohm
SL3009 0402
EC_SO
EC_SI
EC_SCE#
EC_GPG2
BUF_PLT_RST# /eSPI 0Ohm R3016 EXT_SMI#
GL704 1116, reserved for eSPI
PCI_INTA# /eSPI 0Ohm R3028 22,44 SERIRQ
GL704 1117, reserved for eSPI

KSI0_EC
KSI1_EC
KSI2_EC
KSI3_EC
KSI4_EC
KSI5_EC
T3001
EC_KSI6
KSO0_EC
KSO1_EC
KSO2_EC
KSO3_EC
KSO4_EC
KSO5_EC
KSO6_EC
KSO7_EC
KSO9_EC
T3003
EC_KSO8
T3005
T3006
T3007
T3008
T3009
T3012
EC_KSO10
EC_KSO11
EC_KSO12
EC_KSO13
EC_KSO14
EC_KSO15

PM_PWRBTN#
PM_SUSC#
NKEY_INT#
T3022
CAP_LED#
T3021
P_SMB0_CLK
P_SMB0_DAT
TP_CLK
TP_DAT
PWR_SW#
PS_ON_EC
SMB1_CLK
SMB1_DAT
H_PECI
PCH_SPI_IO
SL3008 0402
EC_GPB3
R3023 6.2,30hm
EC_PECI

1020
GL704GS Modify
Battery
Thermal sensor

2015.08.21 EMI Modify
For EMI
C3012 100PF/50V EC_RST#
C3013 100PF/50V PM_SYSPWROK
C3014 100PF/50V PM_PWROK
C3015 100PF/50V DPWROK_EC
C3031 100PF/50V RC_IN#
C3023 100PF/50V 3VSUS_PWRGD
C3025 100PF/50V CHG_FULL_LED#
GL704 1128
C3027 100PF/50V CHG_LED#
C3029 100PF/50V ALL_SYSTEM_PWRGD
C3030 100PF/50V IMVP8_PWRGD
2016.02.18 EMI Modify
C3040 100PF/50V 3VA_DSW_PWRGD

For EMI
2015.08.21 EMI Modify
C3019 15PF/50V 3VADSW_ON
C3003 33PF/50V A/D_MAX_POWER
Close U3001

2015.12.29 EMI Modify
C3050 100PF/50V PM_RSMRST#

C3018 8.2PF/50V CLK_KBCPCI_PCH
C3011 0.01UF/16V BAT1_IN_OC#
C3010 0.01UF/16V PWR_SW#
C3009 0.01UF/16V BUF_PLT_RST#

IT8225VG-128/CX
06037-00260300

PWM0/GPA0
PWM1/GPA1
PWM2/GPA2
PWM3/GPA3
PWM4/GPA4
PWM5/GPA5
PWM6/SSCK/GPA6
PWM7/RIG1#/GPA7
EC_PWR_LED
T3016
CHG_LED#
CHG_FULL_LED#
FAN2_PWM
T3015
EC_GPA6
FAN1_PWM
SL3017 0402
FAN_V_Switch
GL704 1128
GL704 1122

AC_IN#/GPB0
LID_SW#/GPB1
CTX0/TMA0/GPB2
VSTBY0
EC_GPB2
+3VA
AC_IN_OC#
LID_SW#
SL3019 0402
REST_AMP#

CRX0/GPC0
EC_GPC0
T3014
GPC4
EC_GPC4
SL3011 0402
PM_SUSB#
GPC6
SIN0/PWUREQ#/BBO/SMCLK2ALT/GPC7
EC_GPC7
SL3014 0402
BAT1_IN_OC#
NKEY_PWR_EN

RI1#/GPD0
RI2#/GPD1
GINT/CTS0#/GPD5
TACH0A/GPD6
TACH1A/TMA1/GPD7
EC_OV_DDR
EC_GPD1
EC_GPD5
T3023
SL3010
SL3013
ME_AC_PRESENT
OP_SD#
FAN1_TACH
FAN2_TACH

L80HLAT/BAO/GPE0
EGAD/GPE1
EGCLK/GPE3
EGCS#/GPE2
BTN#/GPE4
RTS1#/GPE5
SOUT0/LPCPD#/GPE6
L80LLAT/GPE7
EC_GPE0
EC_GPE1
SL3003
SL3012
SUSB_EC#
SUSC_EC#
5VSUS_ON
1.2V_ON
VSUS_ON
3VADSW_ON
WLAN_PWR_EN
THRO_CPU#

DTR1#/GPG1/ID7
EC_SUSACK#
VFSPI
SL3018
+3V_+1.8V_SPI
GL704 1123, reserved for eSPI

CLKRUN#/GPH0/ID0
CRX1/SIN1/SMCLK3/GPH1/ID1
CTX1/SOUT1/SMDAT3/GPH2/ID2
GPH3/ID3
GPH4/ID4
GPH5/ID5
GPH6/ID6
PM_CLKRUN#
SMCLK3
SMDAT3
PM_RSMRST#
DPWROK_EC
PM_PWROK
PM_SYSPWROK

ADC0/GPI0
ADC1/SPI1
ADC2/SPI2
ADC3/GPI3
ADC4/GPI4
ADC5/DCD1#/GPI5
ADC6/DSR1#/GPI6
ADC7/CTS1#/GPI7
PM_SLP_SUS#
3VSUS_PWRGD
ALL_SYSTEM_PWRGD
IMVP8_PWRGD
3VA_DSW_PWRGD_EC
EC_SUSWARN#
A/D_MAX_POWER
MB_MAX_POWER

TACH2/GPJ0
GPJ1
DAC2/TACH4B/GPJ2
DAC3/TACH1B/GPJ3
DAC4/DCD0#/GPJ4
DAC5/RIG0#/GPJ5
EC_GPJ0
EC_GPJ2
EC_GPJ3
EC_GPJ4
EC_GPJ5
T3002
T3017
T3018
T3019
T3013
GC_STATE_EC

PWRSW/GPB3
XLP_OUT/GPB4
SMCLK1/GPC1
SMDAT1/GPC2
SMCLK2/PECI/GPF6
SMDAT2/PECIRQT#/GPF7
PS2CLK0/TMB0/CEC/GPF0
PS2DAT0/TMB1/GPF1
SMCLK0/GPF2
SMDAT0/GPF3
PS2CLK2/GPF4
PS2DAT2/GPF5

GL704 1120
+1.8VSUS
Q3002A EM6K1-G-T2R
Rdson=13Ohm/Vgs(th)=1.5V
EC_SUSWARN#
SUSWARN#
/eSPI
SL3026
GL704 R20i
Q3002B EM6K1-G-T2R
EC_SUSACK#
PCH_SUSACK#
/eSPI
SL3027
GL704 R20i

GL704 1201
+1.8V_3.3V_IOVDD
Q3001A EM6K1-G-T2R
SMCLK3
SMB3_CLK_SA
Q3001B EM6K1-G-T2R
SMDAT3
SMB3_DAT_SA
SL3028
SL3029
GL704 R20i

R1.0-34
+3VA_DSW
+3VS
R3034 100KOhm
R3033 100KOhm
3VA_DSW_PWRGD
IMVP8_PWRGD
SL3015 0402
3VA_DSW_PWRGD_EC
3VA_DSW_PWRGD

NKey_WRST R3029 10KOhm
PWR_SW# R3026 100KOhm
AC_IN_OC# R3037 100KOhm
LID_SW# R3024 100KOhm
+3VA

+3VA_EC
EC_GPA7 R3018 100KOhm
EC_GPG2 100KOhm
SMB1_DAT RN3001A 6.7KOHM
SMB1_CLK RN3001B 6.7KOHM
P_SMB0_CLK RN3001D 6.7KOHM
P_SMB0_DAT RN3001C 6.7KOHM
SMCLK3 RN3002A 4.7KOhm
SMDAT3 RN3002B 4.7KOhm

3VADSW_ON R3032 100KOhm
R3006 100KOhm
5VSUS_ON R3035 1MOhm
R3030 100KOhm
VSUS_ON R3022 1MOhm
for load code

+3VS
TP_DAT RN3004A 4.7KOhm
TP_CLK RN3004B 4.7KOhm
ClickPad Schematic

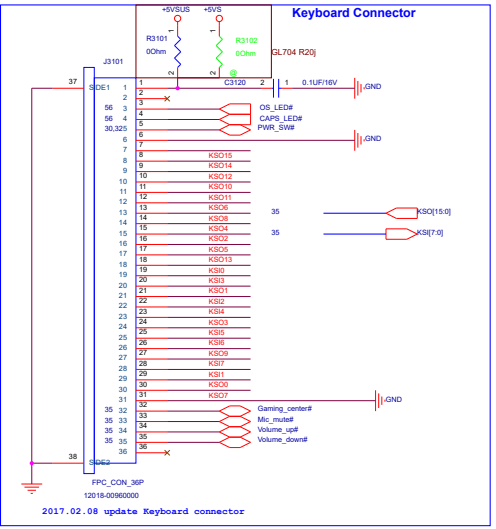
+3VS
RC_IN# R3003 10KOhm
+3VSUS
PM_PWRBTN# R3025 10KOhm
EC_SUSWARN# R3041 /eSPI 10KOhm
+1.8VSUS
PCH_SUSACK# R3044 /eSPI 10KOhm
GL704 1120

+3VA_EC
BAT1_IN_OC# R3038 100KOhm
R3008 100KOhm
PM_SLP_SUS# R3012 100KOhm
PM_SUSC# R3004 100KOhm
PM_SUSB# R3005 100KOhm
SUSB_EC# R3042 4.7KOhm
SUSC_EC# R3043 4.7KOhm
WLAN_PWR_EN R3002 100KOhm
NKEY_PWR_EN R3007 10KOhm
PM_RSMRST# R3036 10KOhm

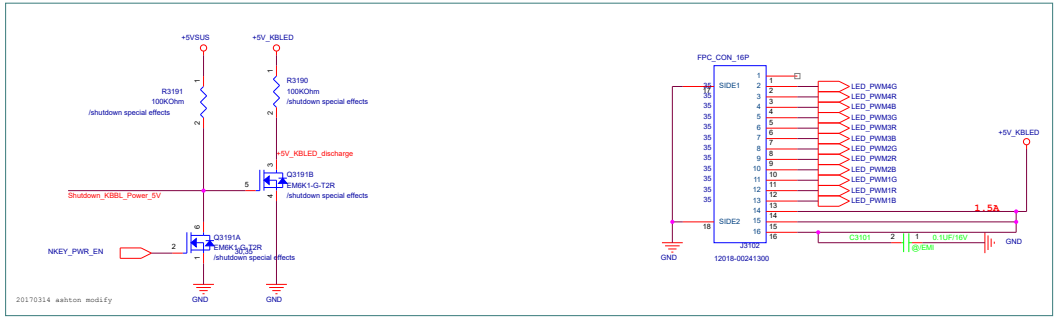
ASUS	Project Name: GL704GSM		Rev: R1.1
Title: KBC_IT8225			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018		Sheet 30 of 103	

Main Board

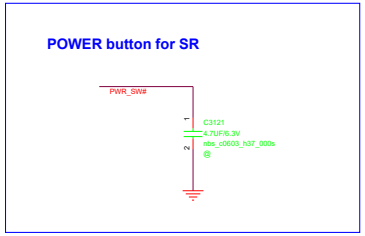
Keyboard Connector



Keyboard LED Connector

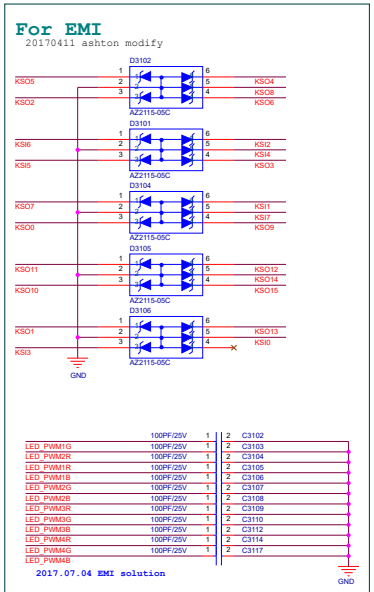


POWER button for SR

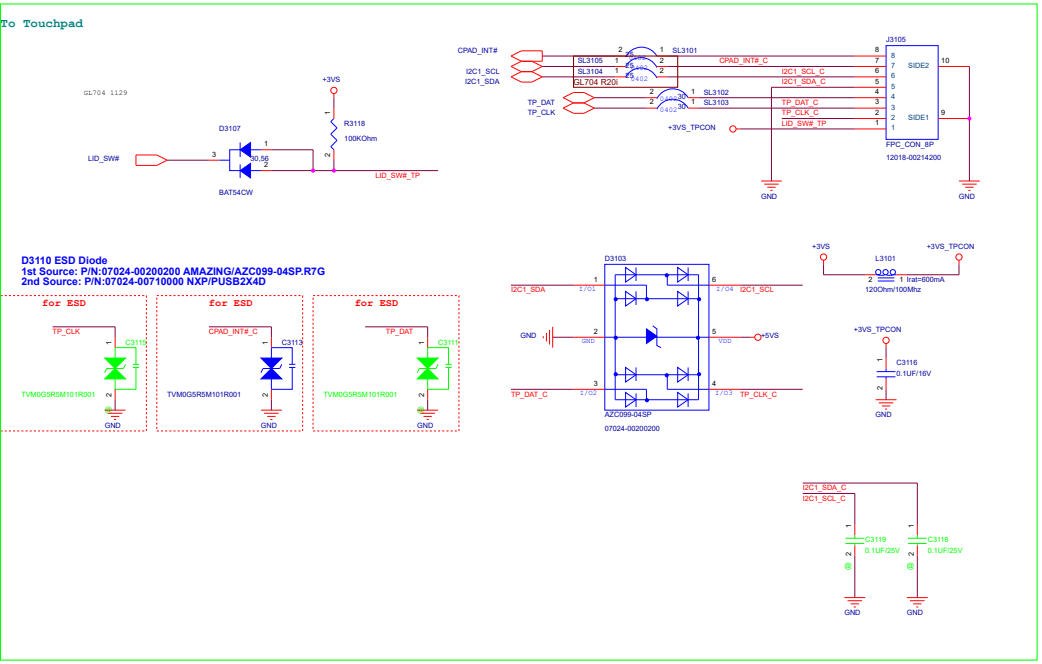


For EMI

20170411 ashton modify



To Touchpad



D3110 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

<Core Design>

ASUSTeK COMPUTER

Title : KBC_KB & TP

Engineer: Gaming RD4 EE1

Size	Project Name	Rev
C	GL704GSM	R1.1

Date: Friday, July 27, 2018 Sheet 31 of 103

PCH_CPU GPIO

	Default	Use As	Signal Name	INT PUPD	EXT PUPD	Power
GPP_A0	ACZRST	Native	RC_IN#		EXT PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		EXT PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		EXT PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		EXT PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	GPO	GPP_A11			
GPP_A12	GPI	GPO				
GPP_A13	SUSWARN#/	Native	ME_SusPwrDnAck			
GPP_A14	SUS_STAT#	Native	ESPI_RESET#			
GPP_A15	SUS_ACK#	Native	PCH_SUSACK#		EXT PU 10K	+1.8VSUS
GPP_A16	Native/GPI	GPO	GPP_A16			
GPP_A17	GPI	GPO	GPP_A17_SID_PWREN			
GPP_A18	GPI	GPO	PCH_GPP_A18			
GPP_A19	GPI	GPO	PCH_GPP_A19			
GPP_A20	GPI	GPO	X			
GPP_A21	GPI	GPO	X			
GPP_A22	GPI	GPO	X			
GPP_A23	GPI	GPO	X			

	Default	Use As		INT PUPD		
GPP_B0	GPO	GPO	PCH_GPP_B0			
GPP_B1	GPI	GPI	PCH_GPP_B1			
GPP_B2	GPI	GPO	PCH_GPP_B2			
GPP_B3	GPI	GPO	X			
GPP_B4	GPI	GPO	X			
GPP_B5	GPI	Native	CLK_REQ0#			
GPP_B6	GPI	Native	X			
GPP_B7	GPI	Native	CLK_REQ1#		EXT PU 10K	+3VSUS
GPP_B8	GPI	Native	X			
GPP_B9	GPI	Native	CLK_REQ4#		EXT PU 10K	+3VSUS
GPP_B10	GPI	Native	X			
GPP_B11	GPO	GPO	X			
GPP_B12	SLP_SO#	Native	SLP_SO#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPP_B14	PD		
GPP_B15	GPI	GPI	PCH_GPP_B15		EXT PU 10K	+3VS
GPP_B16	GPI	GPI	PCH_GPP_B16		EXT PU 10K	+3VS
GPP_B17	GPI	GPI	PCH_GPP_B17			
GPP_B18	GPO	Strap	PCH_GPP_B18	PD		
GPP_B19	GPI	GPO	PCH_GPP_B19/BT_ON_PCH			
GPP_B20	GPI	GPO	PCH_GPP_B20/GPUEVENT#_PCH		EXT PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPP_B21/GC5FWEN_PCH			
GPP_B22	GPO	Strap	PCH_GPP_B22	PD		
GPP_B23	GPO	Native	SML1ALERT#	PD	EXT PU 150K	+3VSUS

	Default	Use As		INT PUPD		
GPP_C0	SMBCLK	Native	SMB_CLK		EXT PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		EXT PU 2.2K	+3VSUS
GPP_C2	GPO	GPI	GPP_C2_BT_UART_WAKE_N	PD	EXT PU 4.7K	+3V_NGFF_WLAN
GPP_C3	SMLOCLK	Native	SMB0_CLK		EXT PU 2.2K	+3VSUS
GPP_C4	SMLOGATA	Native	SMB0_DAT		EXT PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5_WLAN_WAKE	PD	EXT PU 1K	+3VSUS
GPP_C6	SMLICLK	Native	SML1_CLK		EXT PU 2.2K	+3VSUS
GPP_C7	SMLIDATA	Native	SML1_DAT		EXT PU 2.2K	+3VSUS
GPP_C8	GPI	GPO	X			
GPP_C9	GPI	GPO	X			
GPP_C10	GPI	GPO	X			
GPP_C11	GPI	GPI	PCH_GPP_C11			
GPP_C12	GPI	GPI	DIMM_SEL0			
GPP_C13	GPI	GPI	DIMM_SEL1			
GPP_C14	GPI	GPI	DIMM_SEL2			
GPP_C15	GPI	GPI	NTC_ID		EXT PU 10K	+3VSUS
GPP_C16	GPI	Native	TBT_I2C_SCL0_PCH		EXT PU 2.2K	+3VSUS
GPP_C17	GPI	Native	TBT_I2C_SDA1_PCH		EXT PU 2.2K	+3VSUS
GPP_C18	GPI	Native	I2C1_SDA		EXT PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		EXT PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20		PU 10K	+3VS
GPP_C21	GPI	GPO	PCH_GPPC21		EXT PD 10K	
GPP_C22	GPI	GPI	+12VS_FAN_FAULT#_10		EXT PU 150K/PD 10	+3VSUS
GPP_C23	GPI	GPI	CPAD_INT#		EXT PU 10K	+3VS

	Default	Use As		INT PUPD		
GPP_D0	GPI	GPO	GPP_D0			
GPP_D1	GPI	GPO	GPP_D1			
GPP_D2	GPI	GPO	GPP_D2			
GPP_D3	GPI	GPO	GPP_D3			
GPP_D4	GPI	GPO				
GPP_D5	GPI	Native3	PCH_GPPD5			
GPP_D6	GPI	Native3	PCH_GPPD6			
GPP_D7	GPI	GPO	PCH_GPPD7			
GPP_D8	GPI	GPO	PCH_GPPD8			
GPP_D9	GPI	GPO	PCH_GPP_D9			
GPP_D10	GPI	GPO	PCH_GPP_D10			
GPP_D11	GPI	GPO				
GPP_D12	GPI	GPO				
GPP_D13	GPI	GPO	X			
GPP_D14	GPI	GPO	PCH_GPP_D14			
GPP_D15	GPI	GPO				
GPP_D16	GPI	GPO				
GPP_D17	GPI	GPO	X			
GPP_D18	GPI	GPO	X			
GPP_D19	GPI	GPO	X			
GPP_D20	GPI	GPO	X			
GPP_D21	GPI	GPO	GPP_D21			
GPP_D22	GPI	GPO	GPP_D22			
GPP_D23	GPI	GPO	X			

	Default	Use As	Signal Name	INT PUPD	EXT PUPD	Power
GPP_E0	GPI	Native	X			
GPP_E1	GPI	Native	SATAPCIE_DET1		EXT PU 10K	+3VS
GPP_E2	GPI	Native	X			
GPP_E3	GPI	GPI	EXT_SMI#(BUF_PLT_RST#)		EXP PU 10K/PD 100K +3VS	
GPP_E4	GPI	Native	SATA2_HDD1_DEVSLP			
GPP_E5	GPI	Native	X			
GPP_E6	GPI	Native	X			
GPP_E7	GPI	GPI	EXT_SCI#		EXT PU 10K	+3VS
GPP_E8	GPI	Native	SATA_LED#		EXT PU 10K	+3VS
GPP_E9	GPI	Native	USB_OC#0		EXT PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1		EXT PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2		EXT PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3		EXT PU 10K	+3VSUS

	Default	Use As		INT PUPD		
GPP_F0	GPI	Native	X			
GPP_F1	GPI	Native	X			
GPP_F2	GPI	GPO	(N.C)			
GPP_F3	GPI	GPO	X			
GPP_F4	GPI	GPO	X			
GPP_F5	GPI	GPO	X			
GPP_F6	GPI	GPO	X			
GPP_F7	GPI	GPO	X			
GPP_F8	GPI	GPO	X			
GPP_F9	GPI	GPO	X			
GPP_F10	GPI	GPO	X			
GPP_F11	GPI	GPO	X			
GPP_F12	GPI	GPO	X			
GPP_F13	GPI	GPO	X			
GPP_F14	GPI	GPO	X			
GPP_F15	GPI	Native	USB_OC#4		EXT PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		EXT PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		EXT PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		EXT PU 10K	+3VSUS
GPP_F19	GPI	GPO	X			
GPP_F20	GPI	GPO	X			
GPP_F21	GPI	GPO	X			
GPP_F22	GPI	GPO	X			
GPP_F23	GPI	GPO	X			

	Default	Use As		INT PUPD		
GPP_G0	GPI	GPO	SD_CMD_PCH			
GPP_G1	GPI	GPO	SD_D0_PCH			
GPP_G2	GPI	GPO	SD_D1_PCH			
GPP_G3	GPI	GPO	SD_D2_PCH			
GPP_G4	GPI	GPO	SD_D3_PCH			
GPP_G5	GPI	GPO	SD_CD#_PCH			
GPP_G6	GPI	GPO	SD_CLK_PCH			
GPP_G7	GPI	GPO	SD_WP_PCH			

	Default	Use As		INT PUPD		
GPP_H0	GPI	Native	CLK_REQ6#		EXT PU 10K	+3VS
GPP_H1	GPI	Native	X			
GPP_H2	GPI	Native	X			
GPP_H3	GPI	Native	X			
GPP_H4	GPI	Native	X			
GPP_H5	GPI	Native	X			
GPP_H6	GPI	Native	X			
GPP_H7	GPI	Native	X			
GPP_H8	GPI	Native	X			
GPP_H9	GPI	Native	X			
GPP_H10	GPO	GPO	GPP_H10	PD		
GPP_H11	GPI	GPO	X			
GPP_H12	GPO	GPO	GPP_H12	PD		
GPP_H13	GPI	GPO	X			
GPP_H14	GPI	GPO	X			
GPP_H15	GPI	GPO	SML1ALERT#		EXT PU 150K/PU 100K 3VSUS/+3VSUS	
GPP_H16	GPI	GPI	KBID_0		EXT PU 10K	+3VSUS
GPP_H17	GPI	GPI	KBID_1			
GPP_H18	GPI	GPI	KBID_2		EXT PU 10K	+3VSUS
GPP_H19	GPI	GPO	X			
GPP_H20	GPI	GPO	X			
GPP_H21	GPI	GPO	X			
GPP_H22	GPI	GPO	X			
GPP_H23	GPI	GPO	X			

	Default	Use As		INT PUPD		
GPP_I0	GPI	GPO	X			
GPP_I1	GPI	GPO	X			
GPP_I2	GPI	GPO	X			
GPP_I3	GPI	GPO	X			
GPP_I4	GPI	GPO	X			
GPP_I5	GPI	GPO	X			
GPP_I6	GPI	GPO	X			
GPP_I7	GPI	GPO	X			
GPP_I8	GPI	GPO	X			
GPP_I9	GPI	GPO	X			
GPP_I10	GPI	GPO	X			
GPP_I11	GPI	GPO	X			
GPP_I12	GPI	GPO	X			
GPP_I13	GPI	GPO	X			
GPP_I14	GPI	GPO	EDP_HPD		EXT PD 100K	
GPP_I15	GPI	GPO	X			
GPP_I16	GPI	GPO	X			
GPP_I17	GPI	GPO	X			
GPP_I18	GPO	GPO	X			
GPP_I19	GPI	GPO	X			
GPP_I20	GPO	GPO	X			

	Default	Use As		INT PUPD		
GPP_J0	GPI	GPO	X			
GPP_J1	CPU_MISC1_PWR_DATA#	Native	CPU_C10_GATE#_PCH		EXT PU 150K	+1.8VSUS
GPP_J2	GPI	GPO				
GPP_J3	GPI	GPO				
GPP_J4	CNV_BRI_DT	Native	CNV_BRI_DT		EXT PU 20K	+1.8VSUS
GPP_J5	CNV_BRI_RSP	Native	CNV_BRI_RSP		EXT PU 20K	+1.8VSUS
GPP_J6	CNV_RGI_DT	Native	CNV_RGI_DT		EXT PU 20K	+1.8VSUS
GPP_J7	CNV_RGI_RSP	Native	CNV_RGI_RSP		EXT PU 20K	+1.8VSUS
GPP_J8	GPI	GPO	CNV_MFUART2_RXD		EXT PU 1K	+1.8VSUS
GPP_J9	GPO	GPO	CNV_MFUART2_TXD			
GPP_J10	GPI	GPO	X			
GPP_J11	A4WP_PRESENT	GPO	X			

	Default	Use As		INT PUPD		
GPP_K0	GPI	GPO	N31526294			
GPP_K1	GPI	GPI	PCB_ID0		EXT PD 10K	
GPP_K2	GPI	GPI	PCB_ID1		EXT PD 10K	
GPP_K3	GPI	GPO	WLAN_BT_LED		EXT PD 100K	
GPP_K4	GPI	GPO	WLAN_LED		EXT PD 100K	
GPP_K5	GPI	GPO	VOL_DOWN#			
GPP_K6	GPI	GPO	VOL_UP#			
GPP_K7	GPI	GPO	X			
GPP_K8	Reserved	GPO	GPP_K8			
GPP_K9	Reserved	GPO	N44752060			
GPP_K10	Reserved	GPO	GPP_K10		EXT PU 10K	+3VS
GPP_K11	Reserved	GPO	GPP_K11			
GPP_K12	GPI	GPO	X			
GPP_K13	GPI	GPO	X			
GPP_K14	GPI	GPO	X			
GPP_K15	GPI	GPO	X			
GPP_K16	GPI	GPO	X			
GPP_K17	GPI	GPO	X			
GPP_K18	GPI	GPO	PCH_GPPK18			
GPP_K19	GPI	GPO	PCH_GPPK19			
GPP_K20	Reserved	GPO	X			
GPP_K21	Reserved	GPO	X			
GPP_K22	GPI	GPO	X			
GPP_K23	GPI	GPO	X			

	Default	Use As		INT PUPD		
GPD0	BATLOW#	Native	PM_BATLOW#		EXT PU 10K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		EXT PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		EXT PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#			
GPD4	SLP_S3#	Native	SLP_S3#			
GPD5	SLP_S4#	Native	SLP_S4#			
GPD6	SLP_A#	Native	SLP_A#			
GPD7	GPO	GPO	PCH_GPD7		EXT PU 10K	+3VA_DSW
GPD8	SUSCLK	Native	SUS_CLK#			
GPD9	SLP_WLAN#	Native	SLP_WLAN#			
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	GPO	LAN_PWREN			

IT8225VG-128/BX GPIO

	Default	Use As	Signal Name	EXT PUPD	Power
GPA0	0	GPO	PWR_LED(N.C)		
GPA1	OD	GPO	CHG_LED#		
GPA2	OD	GPO	CHG_FULL_LED#		
GPA3	Alt	PWM	FAN2_PWM		
GPA4	0	GPO	EC_GPA4(N.C)		
GPA5	Alt	PWM	FAN1_PWM		
GPA6	Alt	GPO	EC_GPA6(N.C)		
GPA7	0	GPO	EC_GPA7(N.C)		

	Default	Use As	Signal Name	EXT PUPD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	EC_GPB2(N.C)		
GPB3	Alt	GPI	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PB_ON_EC		
GPB5	0	GPO	EC_GPB5/KBKey_WKUP	PD 10K	
GPB6	OD	GPO	EC_3W#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PUPD	Power
GPC0	0	GPO	EC_GPC0		
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	0	GPO	PM_PBSOUT#	PU 10K(@)	+3V(DS)
GPC4	I	GPI	EC_GPC4/PM_SUSB#	PU 100K	
GPC5	I	GPI	PM_SUSC#	PU 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PU 100K	
GPC7	0	GPO	EC_GPC7/RSMRST_PWR_EN	PU 10K(@)	

	Default	Use As	Signal Name	EXT PUPD	Power
GPD0	I	GPO	EC_GPD0/EC_CV_DIR		
GPD1	0	GPO	EC_GPD1/MB_AC_PRESENT		
GPD2	Alt	GPI	BOT_PLT_RST#	PU 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	0	GPO	EC_GPD5/GP_SI#		
GPD6	Alt	GPI	FAN1_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN2_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PUPD	Power
GPE0	0	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	0	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	0	GPO	3.3V_ON		
GPE3	0	GPO	5VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE4	0	GPO	VSUS_ON	PD 1M & PU 100K	+3VA_EC
GPE5	I	GPO	5VALW_ON	PU 100K	+3VA_EC
GPE6	OD	GPO	WLAN_PWR_EN	PD 100K	
GPE7	OD	GPO	TURBO_CPU#	PU 10K	+3VA_DSW

	Default	Use As	Signal Name	EXT PUPD	Power
GPF0	0	GPO	CAP_LED		
GPF1	0	GPO	NUM_LED#		
GPF2	Alt	SMBus	P_SMB2_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB2_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_PECI	PU 10K(@)	
GPF7	0	GPO	PCH_SPI_CS#		

	Default	Use As	Signal Name	EXT PUPD	Power
GPG0	0	GPO	DGPU_LIDET		
GPG1	0	GPO	PCH_RSTBACK#		
GPG2	I	GPI	EC_GPG2	PU 100K	+3VA_EC
GPG6	0	GPO	EC_GPG6(N.C)		

	Default	Use As	Signal Name	EXT PUPD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK/TBT_I2C_SCL_EC	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT/TBT_I2C_SDA_EC	PU 4.7K	+3VA_EC
GPH3	0	GPO	PM_SUSB2#	PU 10K	
GPH4	0	GPO	SPROUT_EC	PU 10K	
GPH5	0	GPO	PM_PWROK	PU 10K	
GPH6	0	GPO	PM_SYSPWROK	PU 10K	
GPH7	0	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PUPD	Power
GPI0	I	GPI	PM_SLP_SUS#	PU 100K(@)	
GPI1	I	GPI	3VPOK_PWRGD	PU 100K	+3V(DS)
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	1HOPE_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_5VA_PWRGD_EC	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#/	PU 100K(@)	+3V(DS)
GPI6	Alt	AD	A/D_MAX_POWER		
GPI7	Alt	AD	MB_MAX_POWER	PU 150K&PD 470K	+3VACC

	Default	Use As	Signal Name	EXT PUPD	Power
GPJ0	0	GPO	EC_GPJ0		
GPJ1	0	GPI	GC6FBEN_PCH	PU 10K(@)	+3VS
GPJ2	Alt	GPI	EC_GPJ2/PSTA_I2C_INT_EC		
GPJ3	0	GPO	EC_GPJ3/USB_BC1.2_OFF#		
GPJ4	Alt	GPO	EC_GPJ4/USB30_SYNC0		
GPJ5	0	GPI	EC_GPJ5/MB_DOCK_DACK_DETECT	PU 100K(@)	+3VA
GPJ6	I	GPI	SERIO_INT#	PU 10K	+VTR_DSW_3Dual/PWR
GPJ7	0	GPO	USB_CHARGE_CB#		

	Default	Use As	Signal Name	EXT PUPD	Power
GPM0	LAD0/EI00		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EI01		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EI02		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EI03		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/EI04		CLK_KBCPCI_PCH		
GPM5	LFRAME#/EI05#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

G703GI Source:

SM_BUS ADDRESS :

PCH Master	
SM-Bus Device	**SM-Bus Address**
SO-DIMM A(0)	A0h
SO-DIMM B(0)	A4h
SO-DIMM A(1)	A2h
SO-DIMM B(1)	A6h
EC Master (SMB1)	**SM-Bus Address**
SM-Bus Device	
CPU INT. Thermal sensor	98h, 9Ch
CPU Thermal Sensor	90h
TI, TAS5766M*2	98h, 9Ah
AGM1562	66h
GPU (Thermistor sense)	74h
PWR(Thermistor sense)	76h, 7Ch, 7Ah, 78h, 7Eh

Device Identification

CPU Thermal Sensor		
1st	0h(0x31)/1h(0x33)	0x1777777U
2nd		

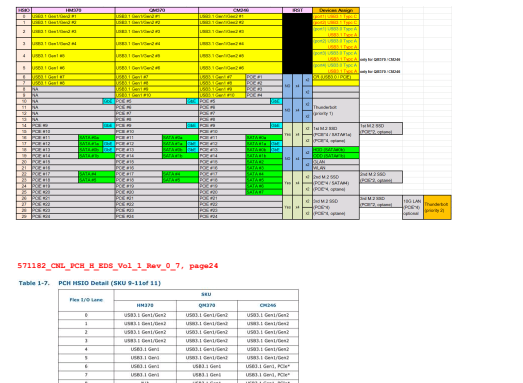
GPU Thermistor		
1st	0h(0)/1h(0x0200)	APL0630AR-TRG
2nd		

USB3.0/PCIE/SATA Setting

1	USB3@1	
2	USB3@2	
3	USB3@3	USB Port1
4	USB3@4	USB Port2
5	USB3@5	USB Port3
6	USB3@6	USB Port4
7	USB3@7	Card Reader
8	PCIE@2	
9	PCIE@3	
10	PCIE@4	
11	PCIE@5	
12	PCIE@6	ThunderBolt x4
13	PCIE@7	
14	PCIE@8	
15	PCIE@9	
16	PCIE@10	PCIE3.0 x 4 SSD
17	PCIE@11	
18	PCIE@12	
19	PCIE@13(SATA3@)	SATA HDD
20	PCIE@14(SATA1@)	
21	PCIE@15	GLAN
22	PCIE@16	WLAN_11AC
23	PCIE@17	
24	PCIE@18	PCIE3.0 x 4 SSD
25	PCIE@19	
26	PCIE@20	
27	PCIE@21	
28	PCIE@22	PCIE3.0 x 4 SSD
29	PCIE@23	
30	PCIE@24	

USB2.0 Setting

1	USB2@1	
2	USB2@2	
3	USB2@3	USB Port1
4	USB2@4	USB Port2
5	USB2@5	USB Port3
6	USB2@6	USB Port4
7	USB2@7	Card Reader
8	USB2@8	XBOX WLAN
9	USB2@9	Camera
10	USB2@10	N-Key
11	USB2@11	BT
12	USB2@12	Tobii IS4
13	USB2@13	TWP
14	USB2@14	



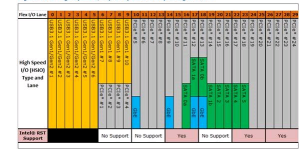
571182_CNL_PCH_H_EDS_Vol_1_Rev_0_7, page24

Table 1-7. PCH HSIO Detail (SKU 9-11of 11)

Flex I/O Lane	SKU		
	HM370	QM370	CM246
0	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
3	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
4	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
5	USB3.1 Gen1	USB3.1 Gen1/Gen2	USB3.1 Gen1/Gen2
6	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
7	USB3.1 Gen1	USB3.1 Gen1	USB3.1 Gen1, PCIe*
8	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
9	N/A	USB3.1 Gen1	USB3.1 Gen1, PCIe*
10	GbE	PCIe*, GbE	PCIe*, GbE
11	N/A	PCIe*	PCIe*
12	N/A	PCIe*	PCIe*
13	N/A	PCIe*	PCIe*
14	PCIe*, GbE	PCIe*, GbE	PCIe*, GbE
15	PCIe*	PCIe*	PCIe*
16	PCIe*, SATA 0A	PCIe*, SATA 0A	PCIe*, SATA 0A
17	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A	PCIe*, GbE, SATA 1A
18	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B	PCIe*, GbE, SATA 0B
19	PCIe*, SATA 1B	PCIe*, SATA 1B	PCIe*, SATA 1B
20	PCIe*	PCIe*	PCIe*, SATA 2
21	PCIe*	PCIe*	PCIe*, SATA 3
22	PCIe*, SATA 4	PCIe*, SATA 4	PCIe*, SATA 4
23	PCIe*, SATA 5	PCIe*, SATA 5	PCIe*, SATA 5
24	PCIe*	PCIe*	PCIe*, SATA 6
25	PCIe*	PCIe*	PCIe*, SATA 7
26	PCIe*	PCIe*	PCIe*
27	PCIe*	PCIe*	PCIe*
28	PCIe*	PCIe*	PCIe*
29	PCIe*	PCIe*	PCIe*

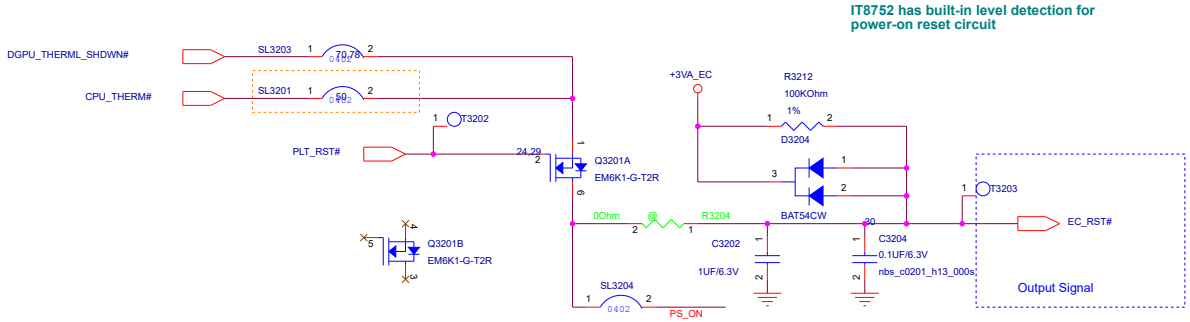
571391_CFL_H_RDG_Rev0p71, page 230

Figure 14-1. High Speed I/O (HSIO) Lane Multiplexing in PCH-H

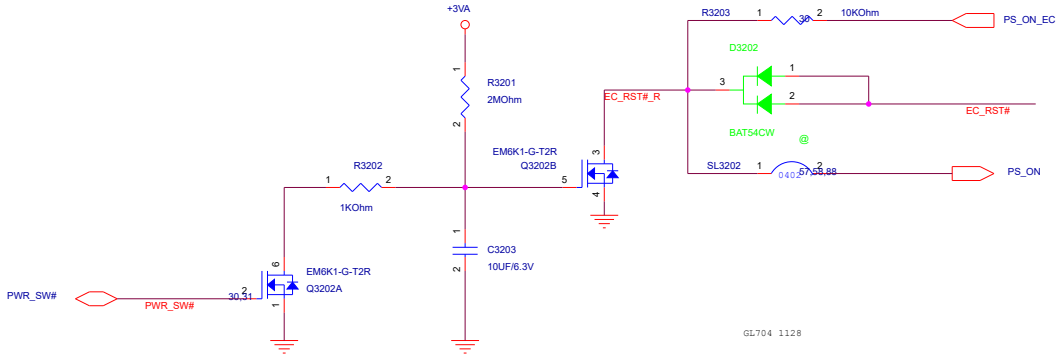


Project Name	GL704GSM	Rev
Title :	System Setting	
Size	Dept. :	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 2 of 130	

Thermal Policy



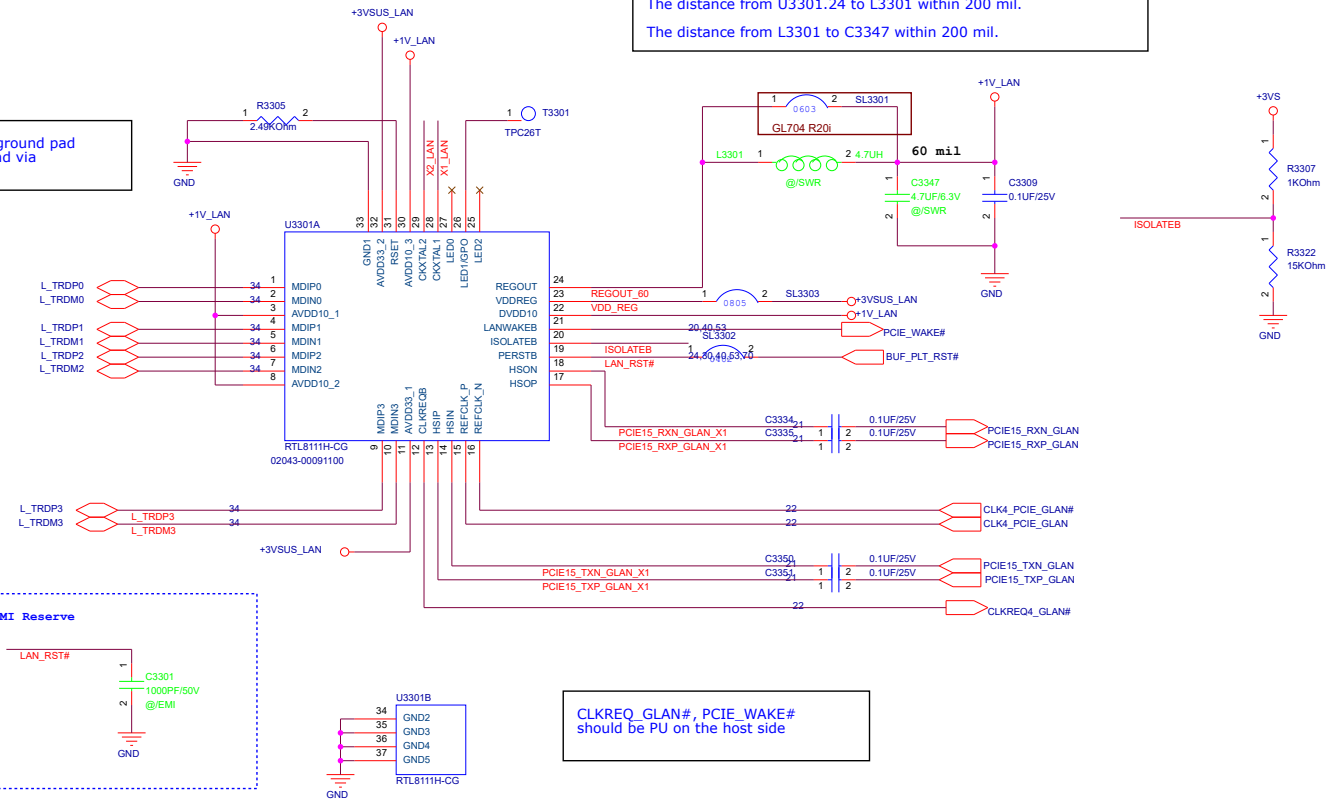
battery embedded (press pwr_sw 10sec, then reset ec)



Project Name: GL704GSM		Rev: R1.1
Title : RST_Reset Circuit		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 32 of 103	

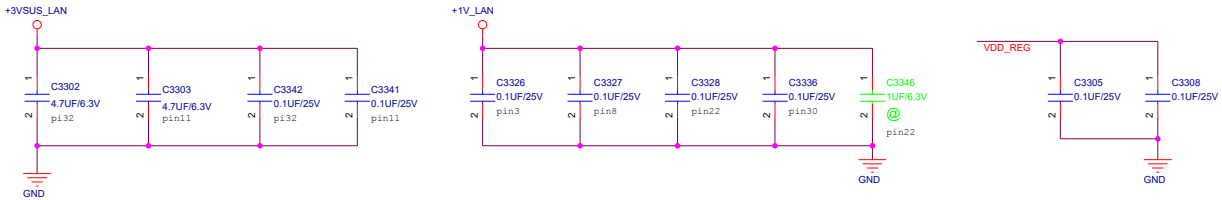
The distance from U3301.24 to L3301 within 200 mil.
The distance from L3301 to C3347 within 200 mil.

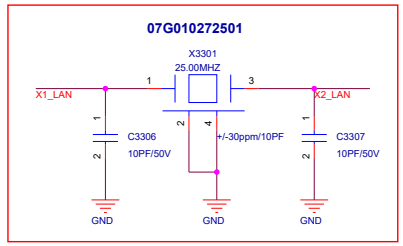
33/34 pin ground pad
need ground via



EMI Reserve

CLKREQ_GLAN#, PCIE_WAKE#
should be PU on the host side



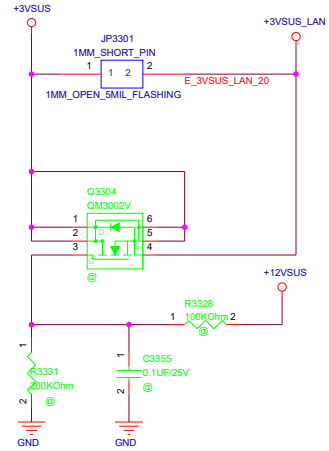


X3301: 25MHZ +/-30ppm/10pF (3225)

1st: P/N:07G010272501 TXC/7V25000011

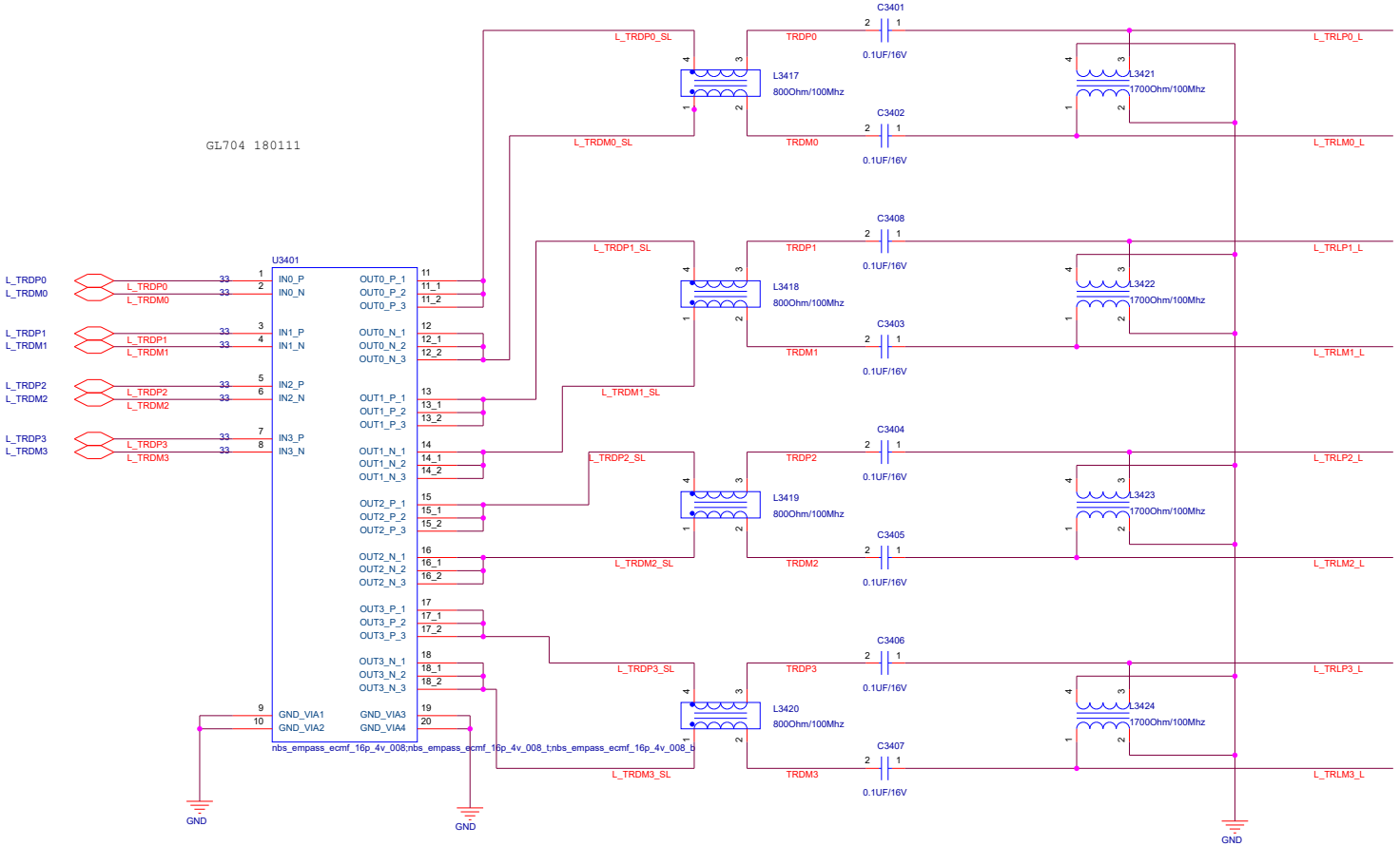
2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms

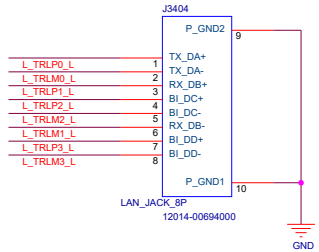


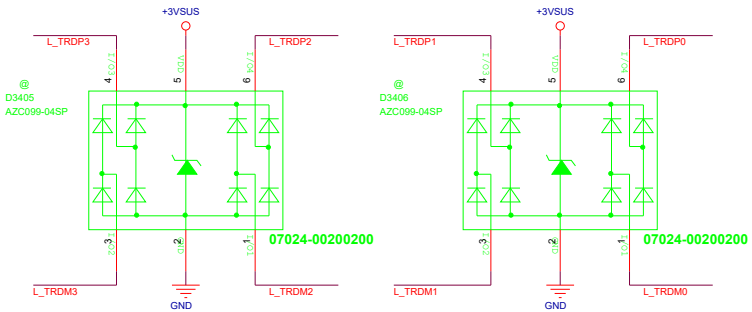
Project Name: GL704GSM		Rev: R1.1
Title : LAN RTL8111GUX-CG		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 33 of 103	

GL704 180111



LAN Connector





D3401,D3402 ESD Diode

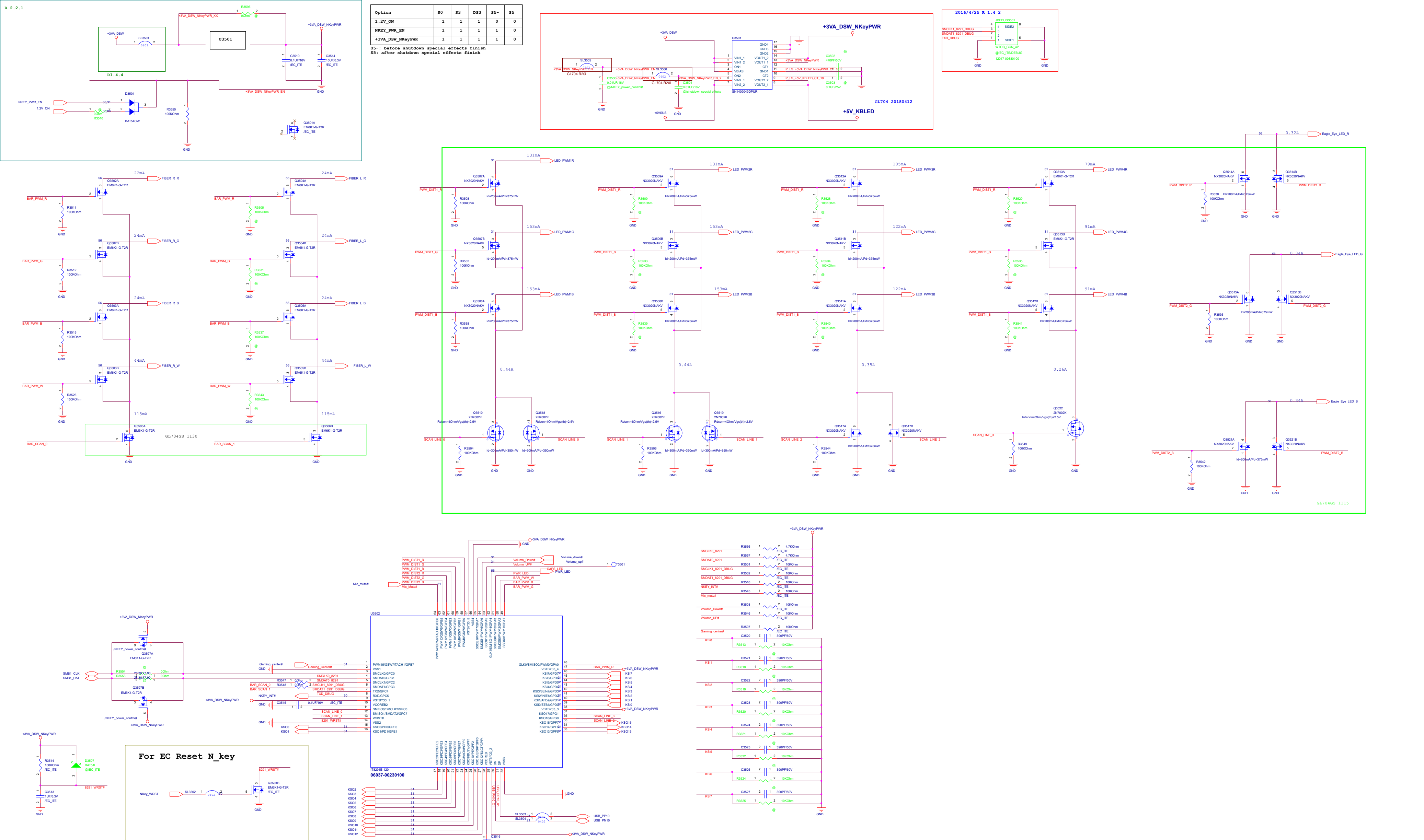
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

Project Name: GL704GSM			Rev: R1.1
Title : LAN_RJ45_CON			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 34 of 103		

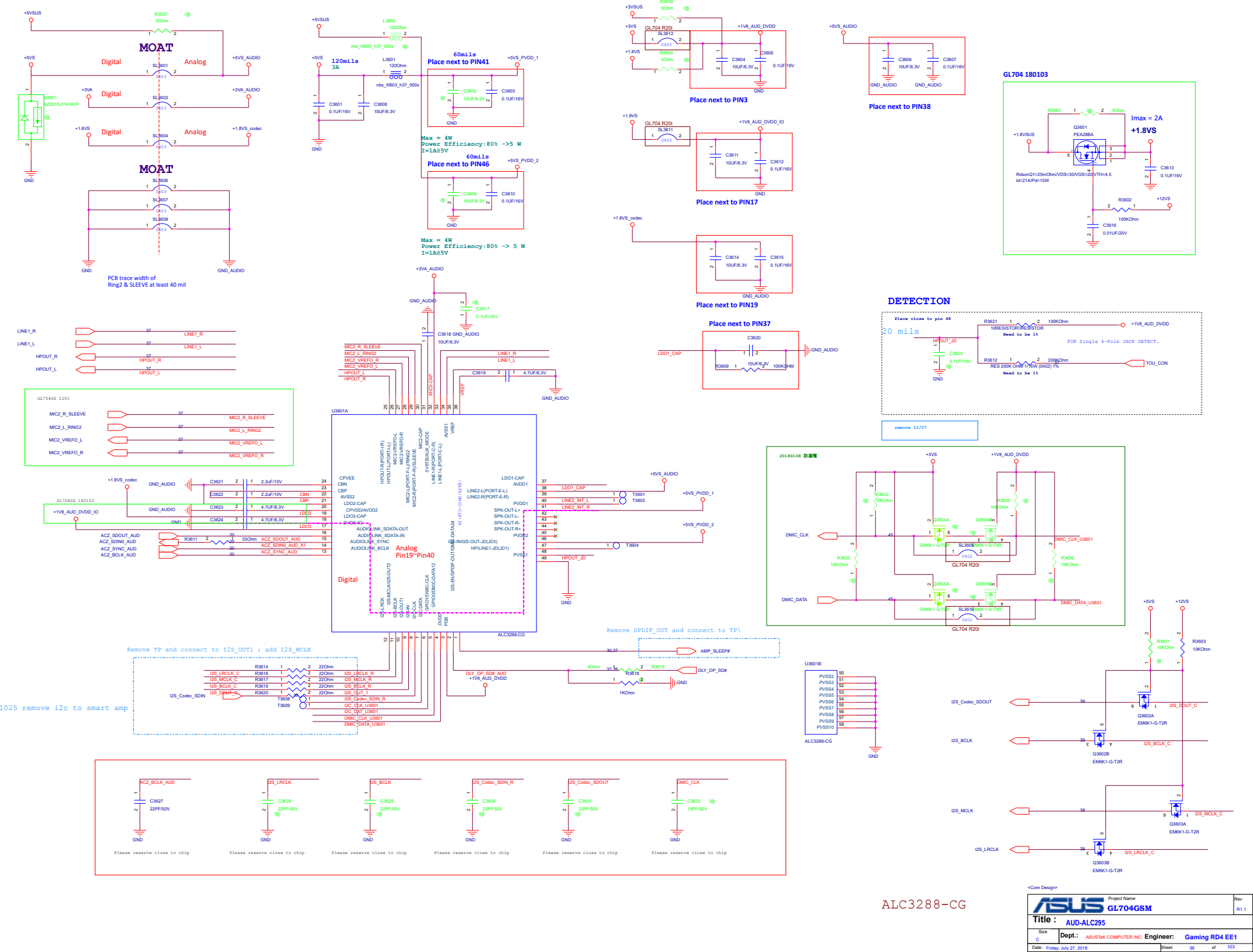
Option	S0	S3	DS3	S5-	S5
1.2V_ON	1	1	1	0	0
NKEY_PWR_EN	1	1	1	1	0
+3VA_DSW_NKeyPWR	1	1	1	1	0

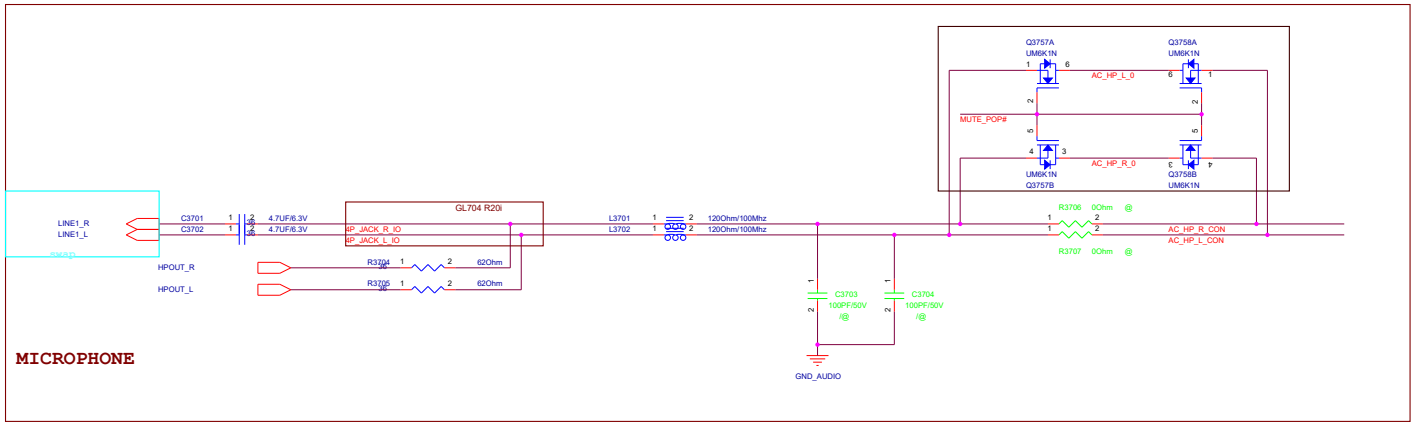
S5-: before shutdown special effects finish
S5: after shutdown special effects finish

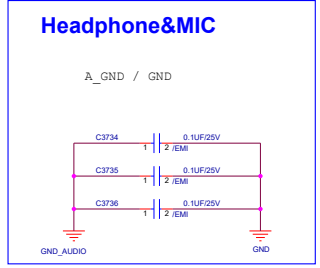


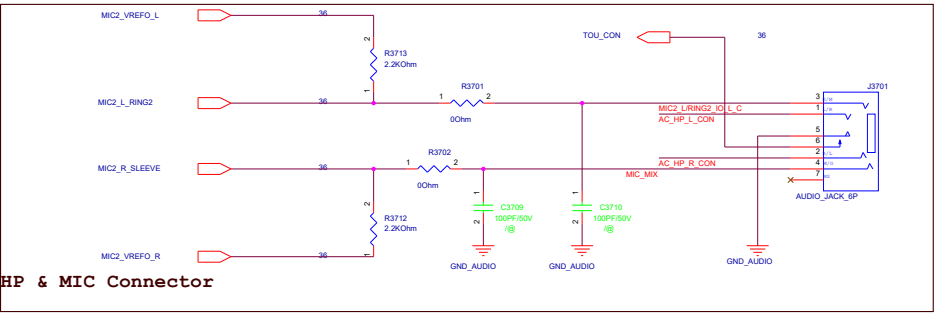
<Core Design>

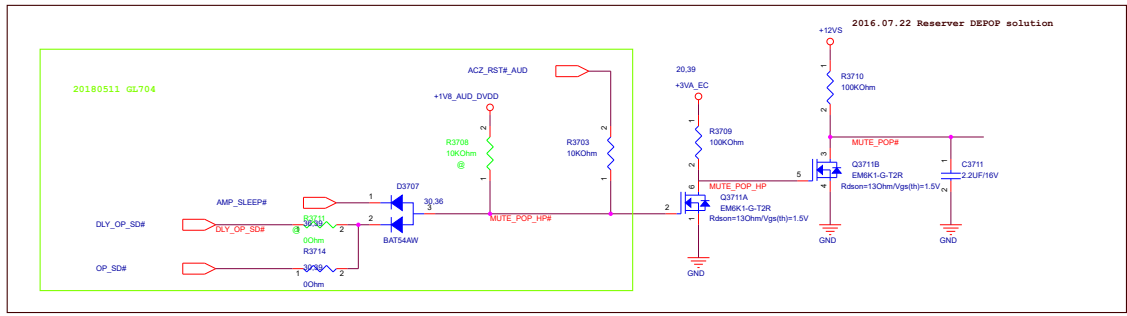
Project Name	GL704GSM
Rev	R1.1
Title :	Macro&N_KEY_ITE8291
Size	D
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Gaming RD4 EE1
Date:	Friday, July 27, 2018
Sheet	35 of 103


MOAT
Digital
Analog
PCB trace width of
Ring2 & SLEEVE at least 40 mil
120mils
3A
60mils
Place next to PIN41
Max = 4W
Power Efficiency:80% ->5 W
I=1A@5V
60mils
Place next to PIN46
Max = 4W
Power Efficiency:80% -> 5 W
I=1A@5V
Place next to PIN3
Place next to PIN38
Place next to PIN17
Place next to PIN19
Place next to PIN37
GL704 180103
Imax = 2A
+1.8VS
DETECTION
20 mils
FOR Single 4-Pole JACK DETECT.
remove 12/07
Analog
Pin19~Pin40
Digital
Remove TP and connect to I2S_OUT1 ; add I2S_MCLK
Remove SPDIF_OUT and connect to TP\
1025 remove i2c to smart amp
Please reserve close to chip
ALC3288-CG
GL704 R20i
Project Name
GL704GSM
Title :
AUD-ALC295
Dept.:
ASUSTeK COMPUTER INC.
Engineer:
Gaming RD4 EE1
Date:
Friday, July 27, 2018
Sheet
36
of
103



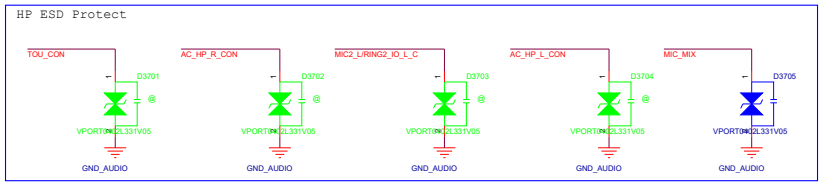






EXTERNAL MICROPHONE

Remove MIC Jack



ASUS	Project Name: GL704GSM		Rev: R1.1
Title : AUD_EXT Jack			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 37 of 103		

<Core Design>

	Project Name **GL704GSM**	Rev R1.1

Title : *****

Size B	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Gaming RD4 EE1

Date: Friday, July 27, 2018	Sheet	38	of	103

Max = 4W / Channel = 8W
Power Efficiency:85% -> 9.5 W
I=1.05A@9V 0.8 A@12V

Power

+5VS-->+5VSUS

+5VS-->+5VSUS

2017.03.21 AMP Change SNL04M25555

+3VA_DSW

Imax = 300mA

Iq=50uA , Isd=1.5uA

+5VSUS_AMP_2

Iq=50uA , Isd=1.5uA

1116 pull high to +3VA_DSW

Need connect to
U3001 D2

teknisi-indonesia

4A

4A

Need connect to
U3001 E8 D7
Need 1.8V 3.3V level shift

2015.04.14 3 pole mic design and VB2 Reserve

MUTE CONTROL

MUTE CONTROL new solution for 1.8V HDA BUG 0318

Smart Amp I2C address

AMP L	SPK vender 1	0x4C
AMP R	SPK vender 1	0x4D
AMP L	SPK vender 2	0x4E
AMP R	SPK vender 2	0x4F

Table 1. I²C Address Selection

ADR0_SCLK Pin Connection	ADR1_MSIO Pin Connection	I²C Device Address
GND	GND	0x4C
IOVDD	GND	0x4D
GND	IOVDD	0x4E
IOVDD	IOVDD	0x4F

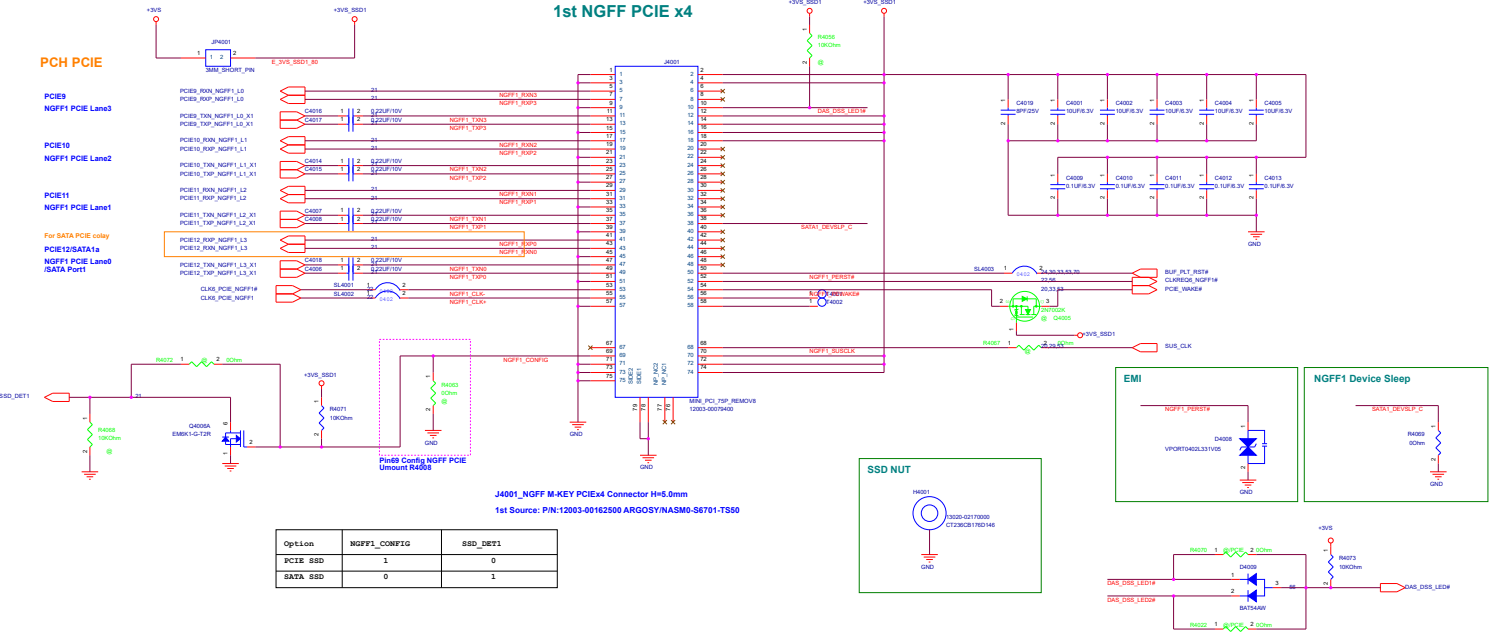
INTERNAL SPK1 Conn.

SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 30mils

Max = 4W / Channel
I = 0.7 A (@Speaker : 8 Ohm)

remove INTERNAL SPK2 Conn. 11/08

Project Name	GL704GSM	Rev	R1.1
Title :	AUD_INT SPK		
Size	Custom	Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Gaming RD4 EE1		
Date:	Friday, July 27, 2018	Sheet	39 of 103



Option	NGFF1_CONFIG	SSD_DET1
PCIE SSD	1	0
SATA SSD	0	1

ASUS	Project Name: GL704GSM		Rev: R1.1
Title : NGFF_SSD_PCIE_CON			
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 40 of 103		

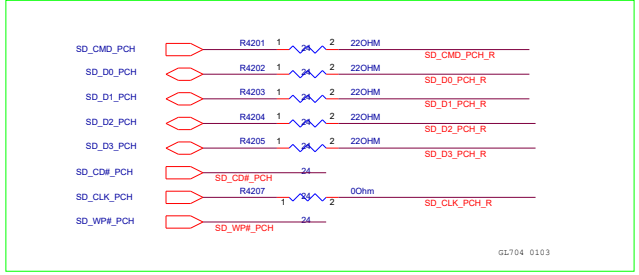
<Core Design>

	Project Name **GL704GSM**	Rev R1.1

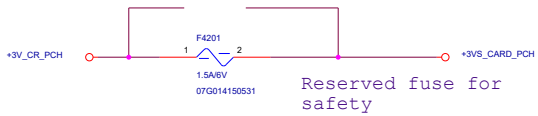
Title : NGFF_SSD_SATA_CON

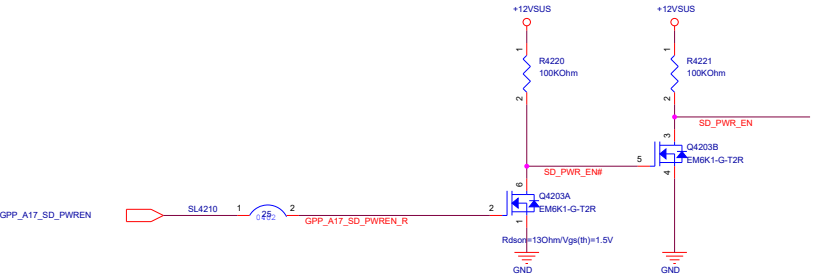
Size B	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Gaming RD4 EE1

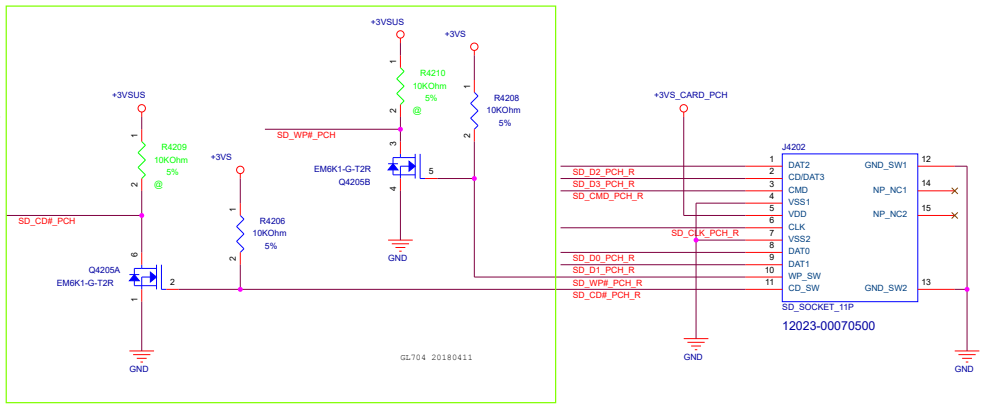
Date: Friday, July 27, 2018	Sheet	41	of	103

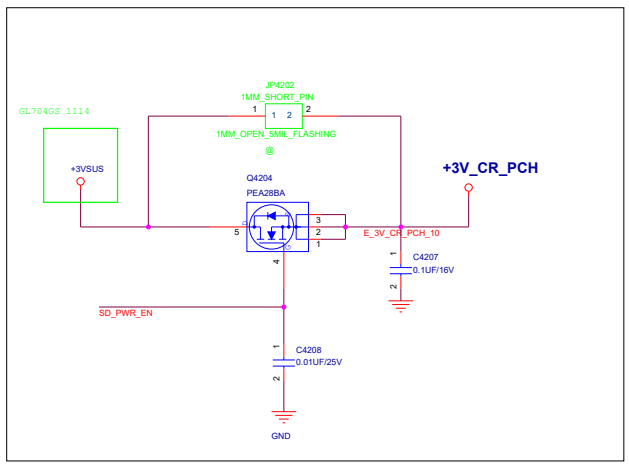


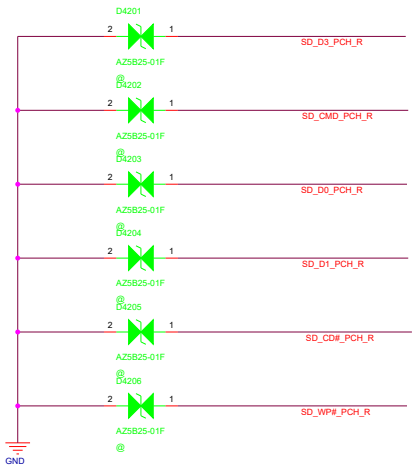
CR Socket









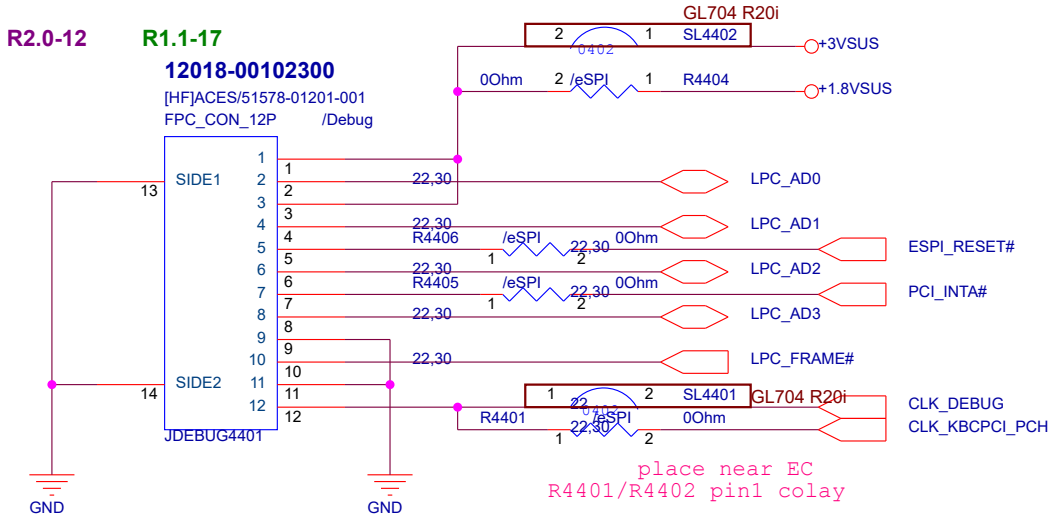


Project Name: GL704GSM			Rev: R1.1
Title: CR_GL3215			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 42 of 103		

LPC Debug Port

ASUS	Project Name: GL704GSM	Rev: R1.1
Title : *****		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 43 of 103	

LPC Debug Port

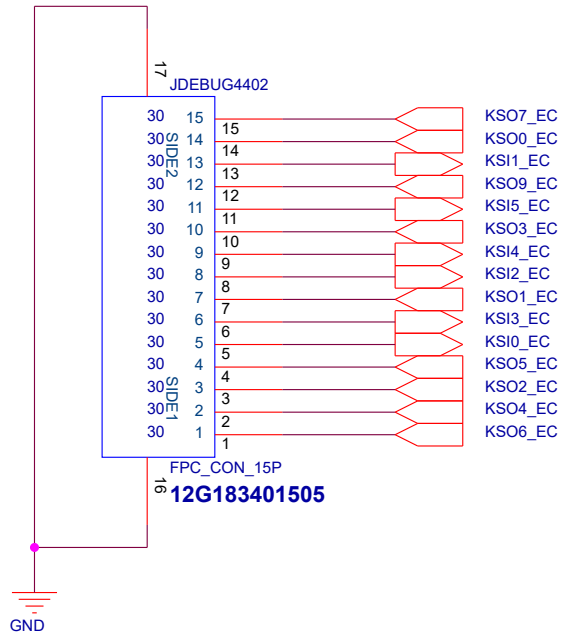


JDEBUG4401 Connector (MP USE)

1st Source: P/N:12018-00102300 ACES/51578-01201-001

2nd Source: P/N:12018-00102100 ENTERY/6705K-Y12N-00L

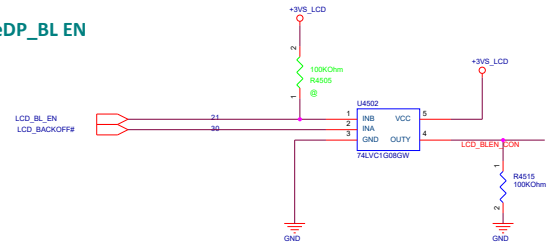
GL704 1128



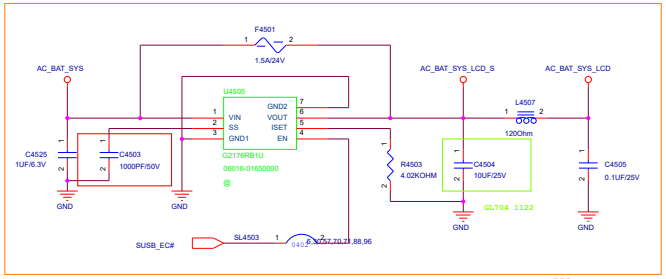
Project Name: GL704GSM		Rev: R1.1
Title : BUG_LPC		
Size: A	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 44 of 103	

Main Board

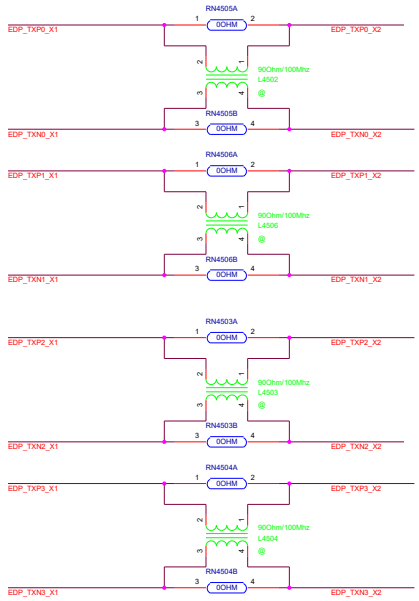
eDP_BL EN



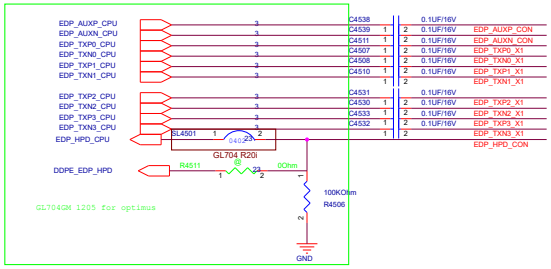
Panel BL Power



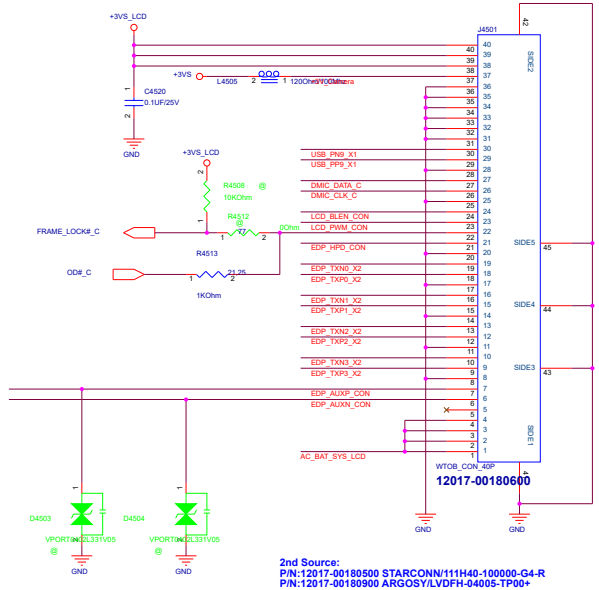
For EMI



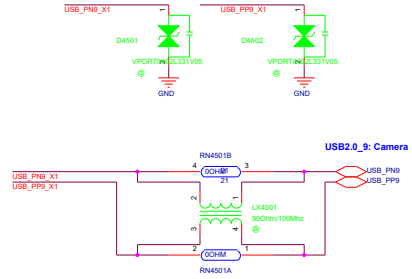
eDP circuit



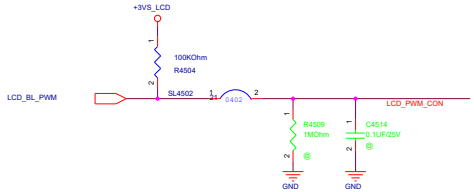
eDP Panel Conn.



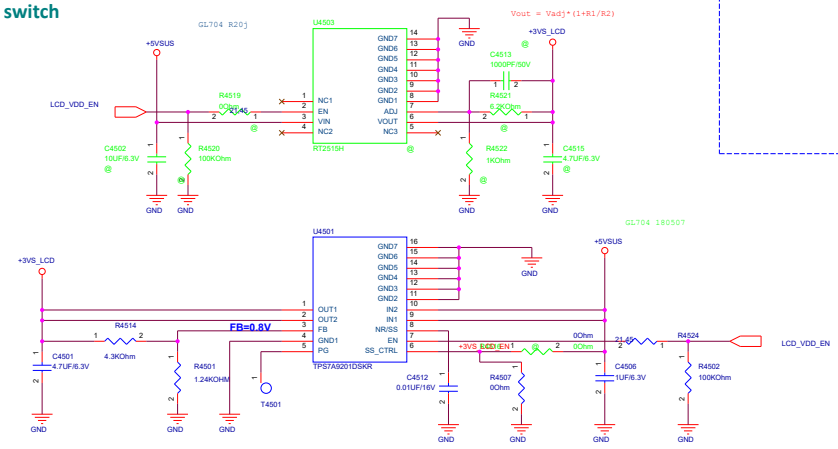
Camera & D-MIC



eDP_BL PWM

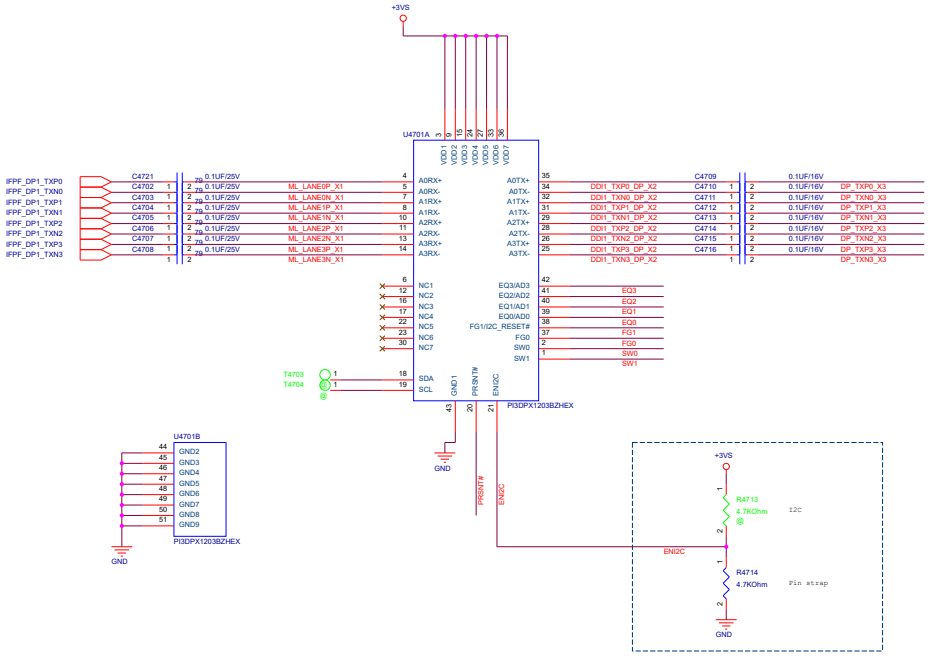


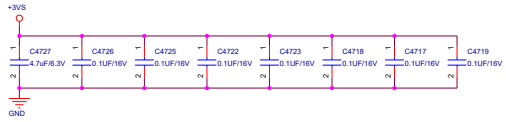
LCD Power switch

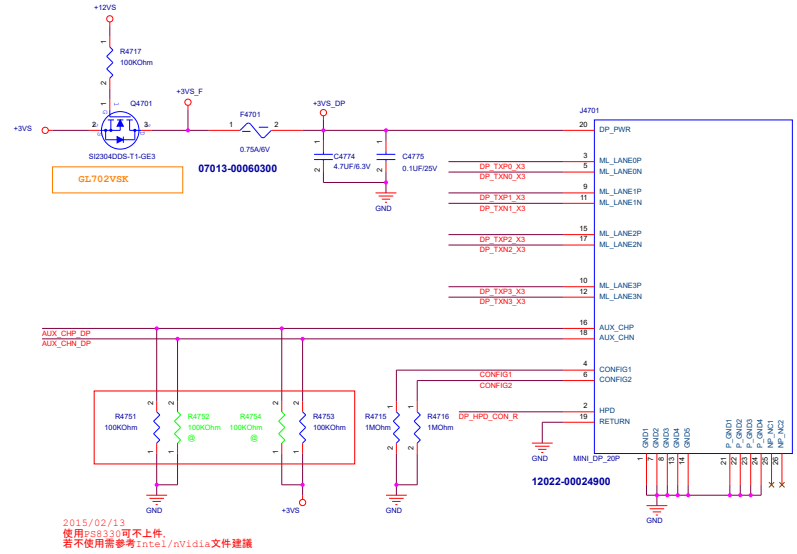


Project Name: GL704GSM			Rev: R1.1
Title: eDP_CON & Tobii IS4_CON			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 45 of 103		

DP Repeater_PI3DPX1203B







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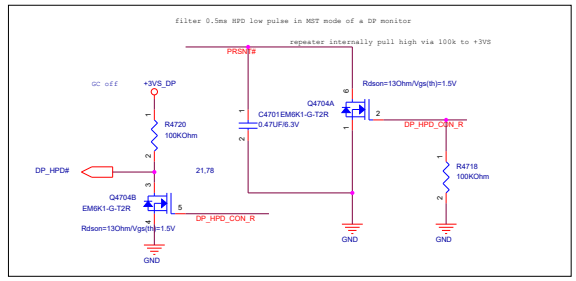
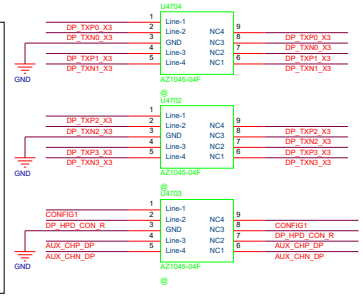
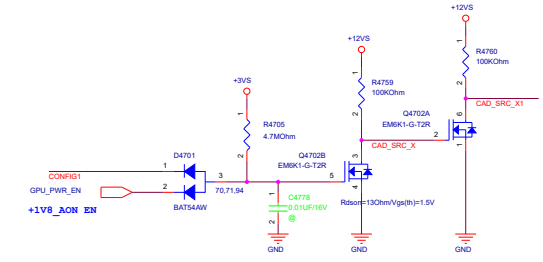
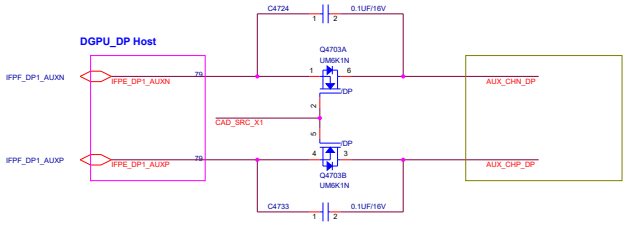
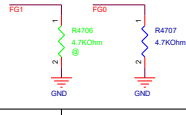


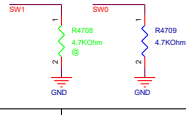








FG1	FG0	Gain (dB)
0	0	-3.5
0	1	-1.5
1	0	0.5
1	1	2.5

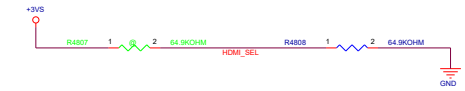


SW1	SW0	mVppd @ 8G
0	0	700
0	1	800
1	0	900
1	1	1000

EQ3	EQ2	EQ1	EQ0	2.7 Gbps Input EQ(dB)	5.4 Gbps Input EQ(dB)	8 Gbps Input EQ(dB)
0	0	0	0	2.3	3.2	3.9
0	0	0	1	2.4	3.5	4.4
0	0	1	0	2.5	3.8	4.9
0	0	1	1	2.6	4.1	5.5
0	1	0	0	2.7	4.5	6.0
0	1	0	1	2.9	4.8	6.5
0	1	1	0	3.0	5.1	6.9
0	1	1	1	3.1	5.5	7.4
1	0	0	0	3.2	5.8	7.8
1	0	0	1	3.4	6.1	8.3
1	0	1	0	3.5	6.4	8.7
1	0	1	1	3.7	6.7	9.0
1	1	0	0	3.8	7.0	9.4
1	1	0	1	4.0	7.4	9.8
1	1	1	0	4.1	7.6	10.1
1	1	1	1	4.3	7.9	10.4

ASUS	Project Name: GL704GSM	Rev: R1.1
Title : Display Port		
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 47 of 103	

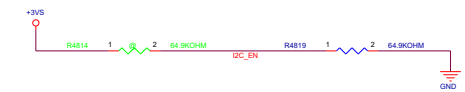
Slew rate control when I2C_EN/PIN = Low.
SLEW_CTL = H, fastest data rate
SLEW_CTL = L, 5 ps slow
SLEW_CTL = No Connect, 10 ps slow



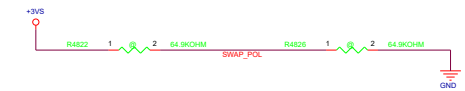
HDMI_SEL when I2C_EN/PIN = Low
HDMI_SEL = High: Device configured for DVI
HDMI_SEL = Low: Device configured for HDMI

Input Receive Equalization pin strap when I2C_EN/PIN = Low
EQ_SEL = L: Fixed EQ at 7.5 dB
EQ_SEL = No Connect: Adaptive EQ
EQ_SEL = H: Fixed at 14 dB

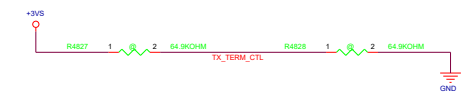
De-emphasis pin strap when I2C_EN/PIN = Low.
PRE_SEL = L: - 2 dB de-emphasis level
PRE_SEL = No Connect: 0 dB
PRE_SEL = H: Reserved



I2C_EN/PIN = High; puts device into I2C control mode
I2C_EN/PIN = Low; puts device into pin strap mode



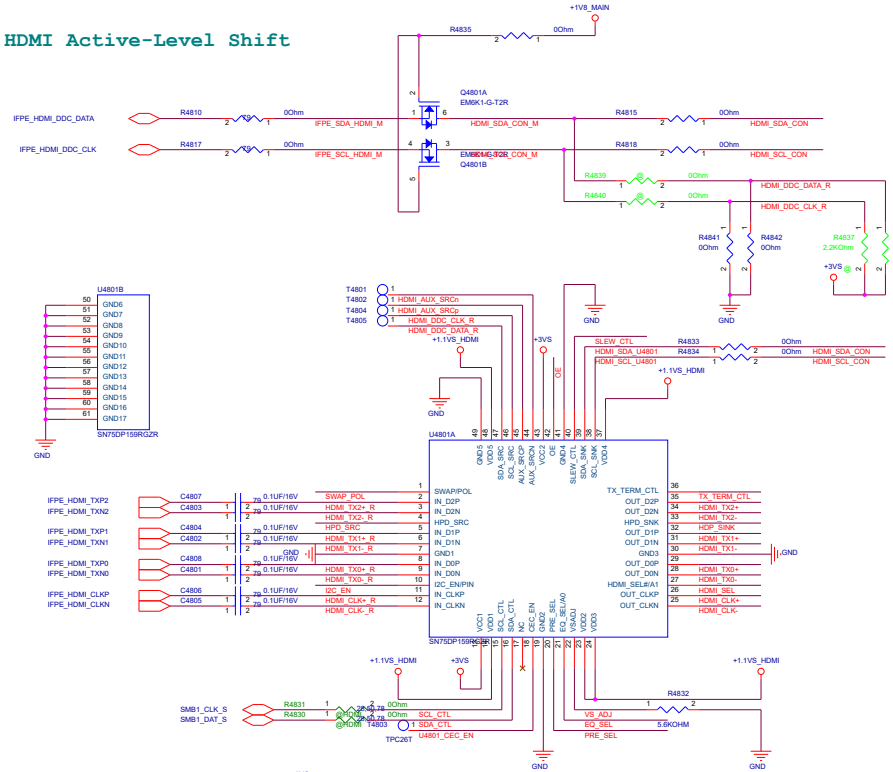
Input lane SWAP and polarity control pin when I2C_EN/PIN = Low
SWAP/POL = H receive lane polarity swap (retimer mode only)
SWAP/POL = L receive lanes swap (retimer and redriver mode)
SWAP/POL = No Connect normal working

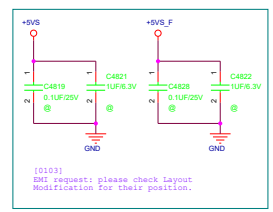


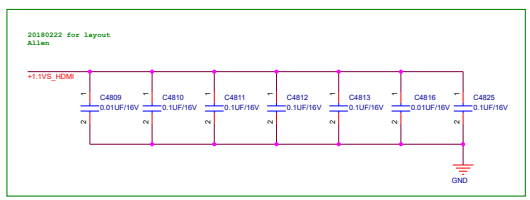
Transmit Termination Control when I2C_EN/PIN = Low
TX_TERM_CTL = H, No transmit termination
TX_TERM_CTL = L, Transmit termination impedance in 75 to about 150 Ω
TX_TERM_CTL = No Connect, automatically selects the termination impedance

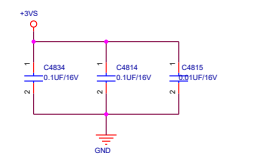
Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

HDMI Active-Level Shift

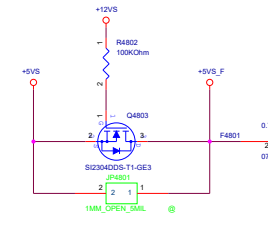




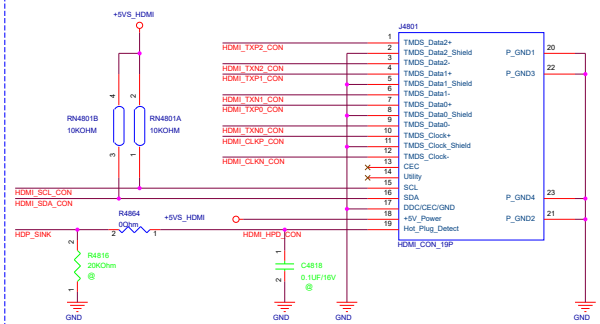




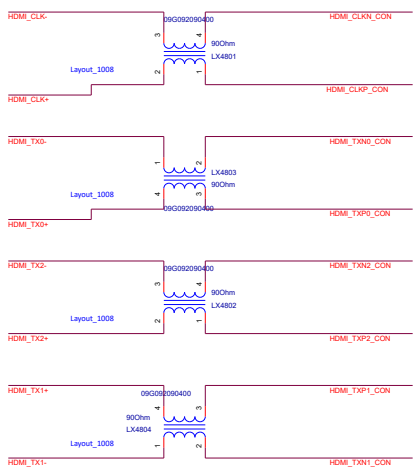
HDMI PWR_+5VS_HDMI



HDMI Conn.

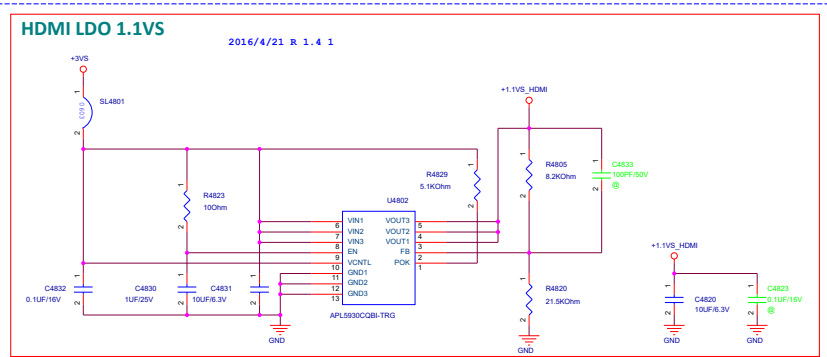


HDMI EMI



HDMI LDO 1.1VS

2016/4/21 R 1.4 1



ASUS	Project Name: GL704GSM		Rev: R1.1
Title : HDMI			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 48 of 103		

<Core Design>

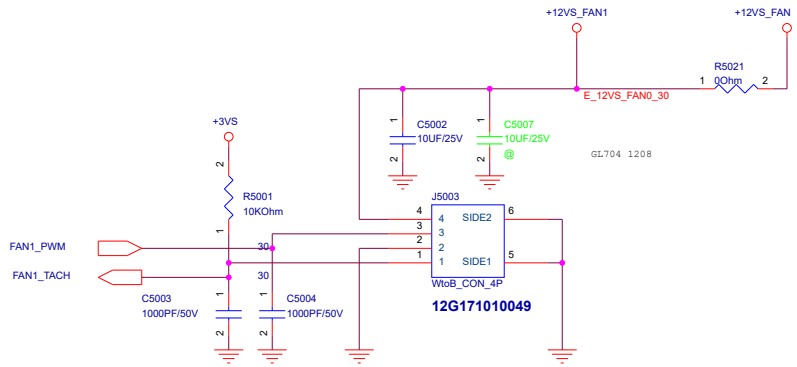
	Project Name **GL704GSM**	Rev R1.1

Title : *****

Size B	**Dept.:** ASUSTeK COMPUTER INC.	**Engineer:** Gaming RD4 EE1

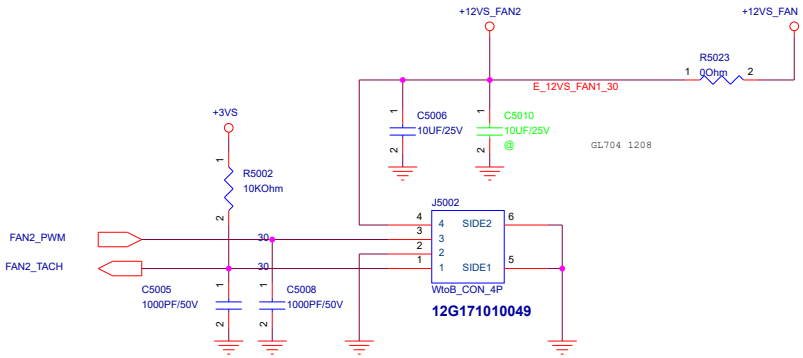
Date: Friday, July 27, 2018	Sheet	49	of	103

PWM CPU Fan



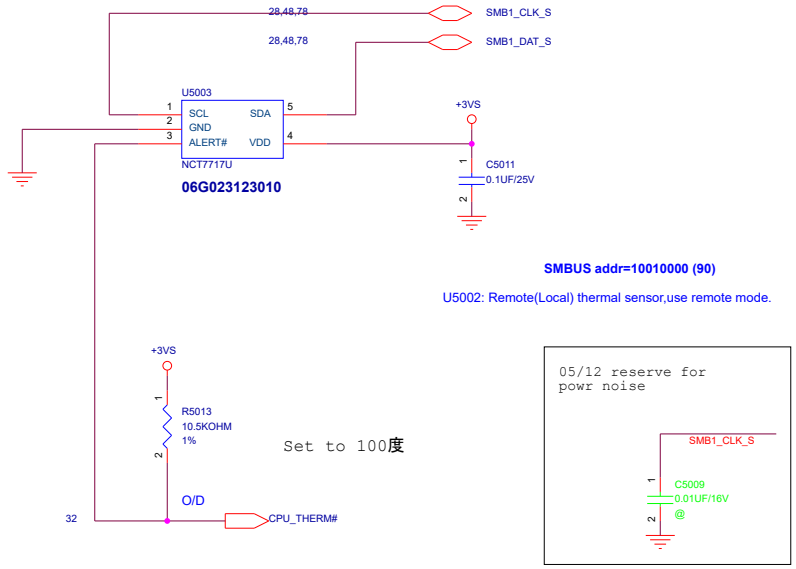
J5001 FAN Connector
2nd Source:
P/N:12G17000004V ENTERY/3801-F04C-01R

PWM VGA Fan

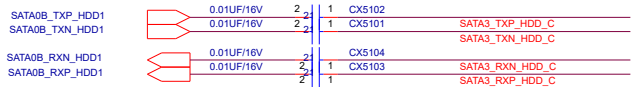


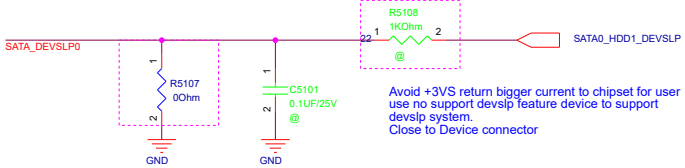
J5002 FAN Connector
2nd Source:
P/N:12G17000004V ENTERY/3801-F04C-01R

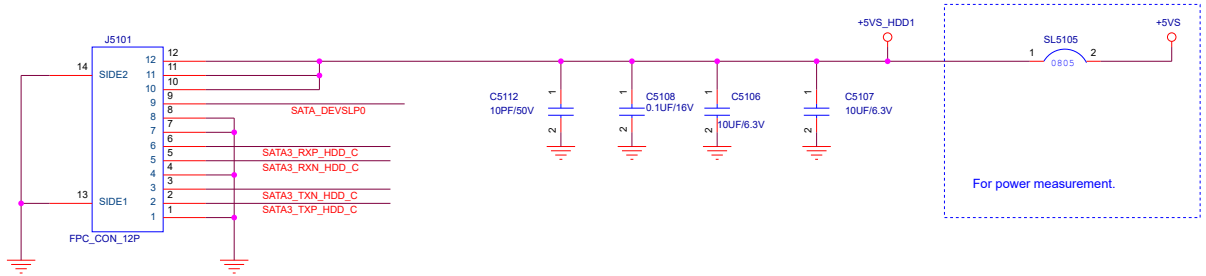
CPU Thermal Sensor



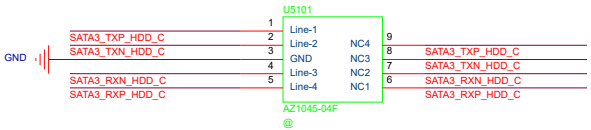
ASUS	Project Name: GL704GSM		Rev: R1.1
Title : FAN_Thermal Sensor & Fan			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 50 of 103		







EMI Request



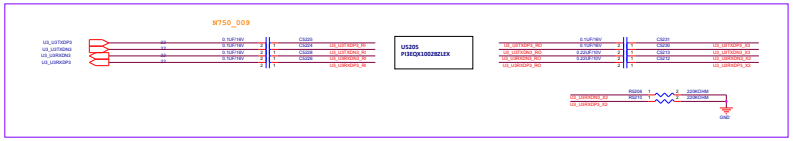
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F

2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

<Core Design>

ASUS	Project Name: GL704GSM	Rev: R1.1
Title : HDD		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 51 of 103	

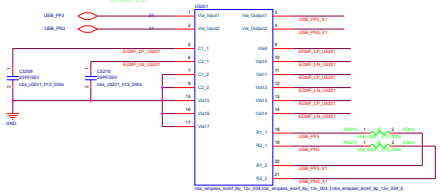
USB3.1_Port3



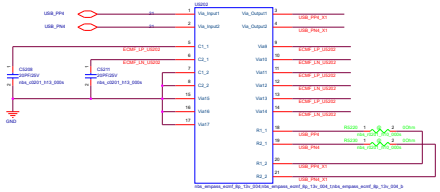
USB3.0_Port4

USB2.0 EMI-Protection With ECMF(PCB 1.25mm_8Layer)

From PCH USB2.0 Port

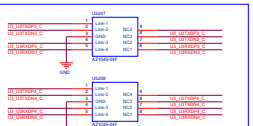


From PCH USB2.0 Port



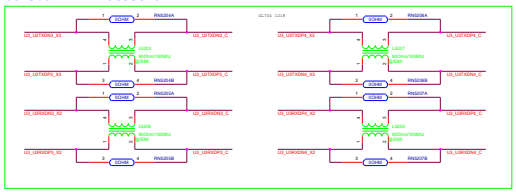
Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. C5209&C5210 / C5211&C5208 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7/8/11/12 must be connected to system ground
4. Pin13/14/15/16 are floated in regular scheme

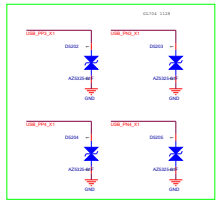
USB3.0 ESD-Protection



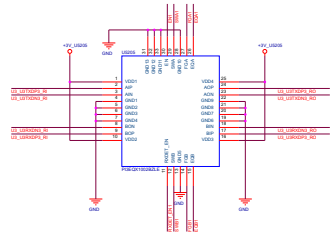
US202 ESD PROTECTION
1st Source: P/N:97G028076030 ESD PROTECTION AZ1045-04F
2nd Source: P/N:97G029153010 ESD PROTECTION IP4284CZ10-TB

USB3.0 EMI-Protection



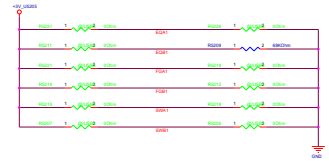


Pericom : 06113-00210000 REDRIVER IC PI3EQX1002BZLEX



< Channel / Receiver setting for Pericom 1002B >

Setting	Channel Enable [EN]	Receiver Detection [RXDET_EN]
0 : 0 Ω to GND	Disable	Disable
1 : 0 Ω to VDD	Enable(Default)	Enable(Default)
Note	Channel Enable / Receiver detection With internal 300K pull-up R.	



< Fine tune table for Pericom (One port Gen2) >

< EQ table for Pericom 1002B >

EQ[A:B]	Gen 1 @2.5GHz(dB)	Gen 2 @5GHz(dB)
0 : 0 Ω to GND	5.1	10.9
R : Rest to GND	1.9	6.7
F : Leave Open	3.5(Default)	8.9(Default)
1 : 0 Ω to VDD	6.8	13.1

Note : With internal 100Kohm pull-up Rup and 200Kohm pull-down Rdown.
Rest = 68Kohm

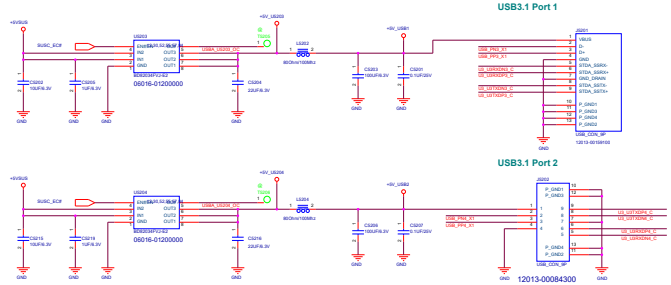
< FG table for Pericom 1002B >

FG[A:B]	Flat Gain (dB)
0 : 0 Ω to GND	-3.0
R : Rest to GND	-1.5
F : Leave Open	0 (Default)
1 : 0 Ω to VDD	+2.0

< SW table for Pericom 1002B >

SW[A:B]	Output Linear Swing (mV)
0 : 0 Ω to GND	800
R : Rest to GND	1200
F : Leave Open	1000 (Default)
1 : 0 Ω to VDD	1100

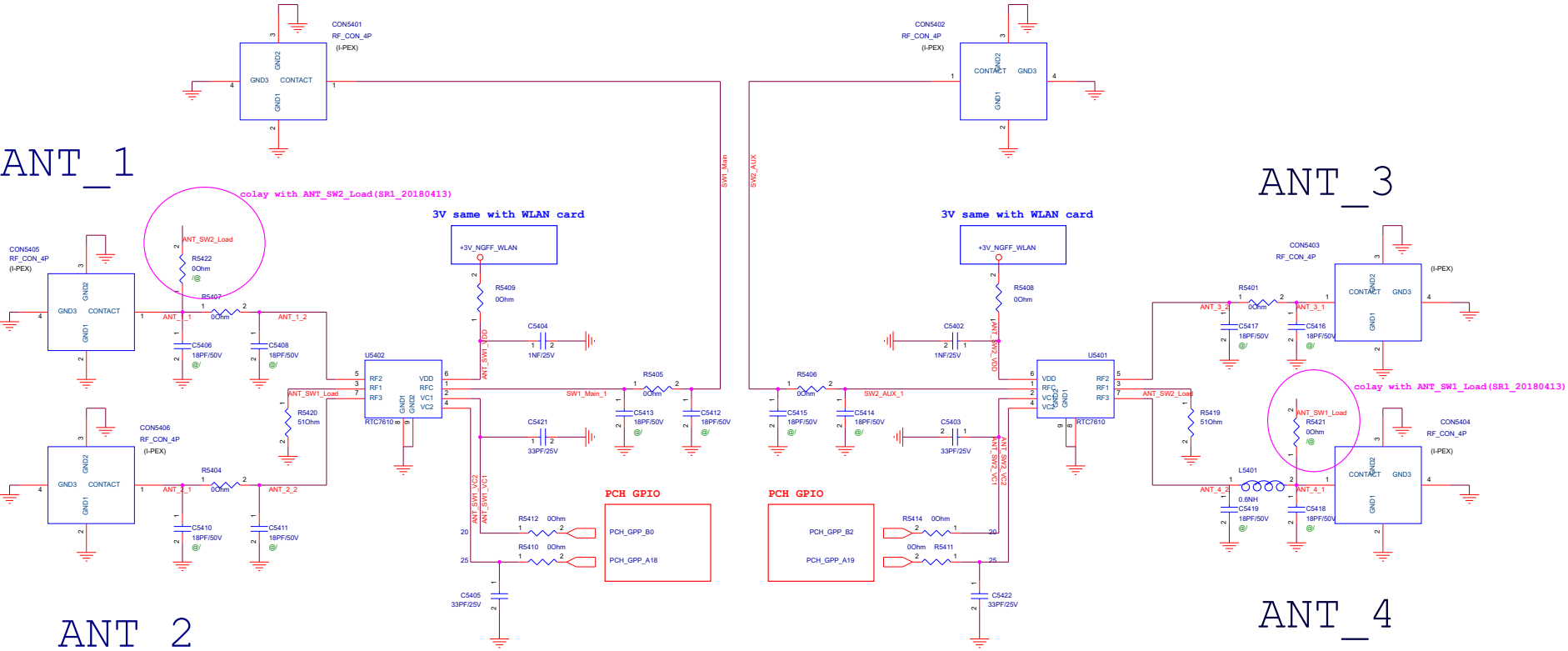
USB3.0_PORT1/2



ASUS	Project Name: GL704GSM		Rev: 1.0
Title :	USB3.0 Port		
Size:	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 22, 2016	Sheet	of	

Module_Main

Module_AUX



U5402 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

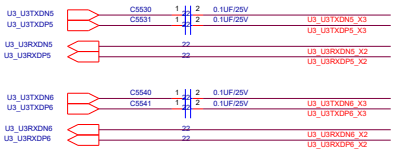
U5401 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

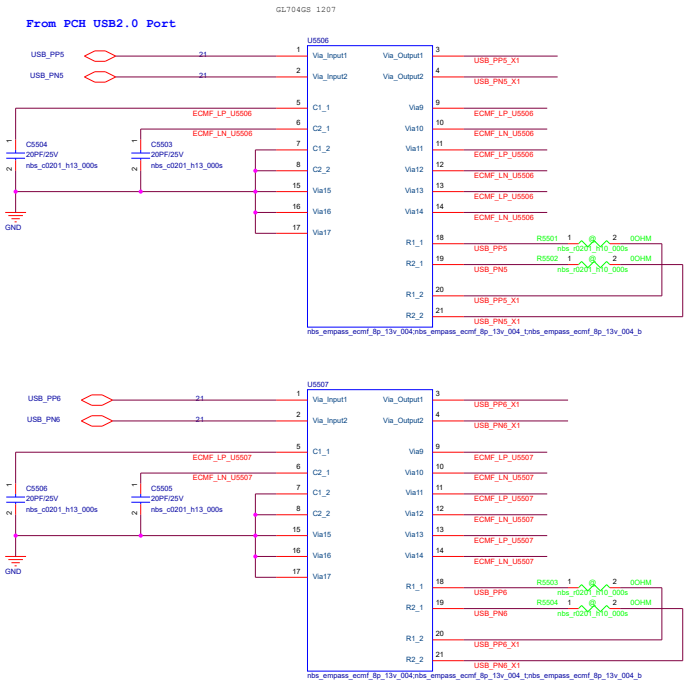
<Core Design>

Project Name: GL704GSM		Rev: R1.1
Title : ANT		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 54 of 103	

USB3.0_Port5 & USB3.0_Port6



USB2.0 EMI-Protection With ECMF(PCB 1.25mm_8Layer)

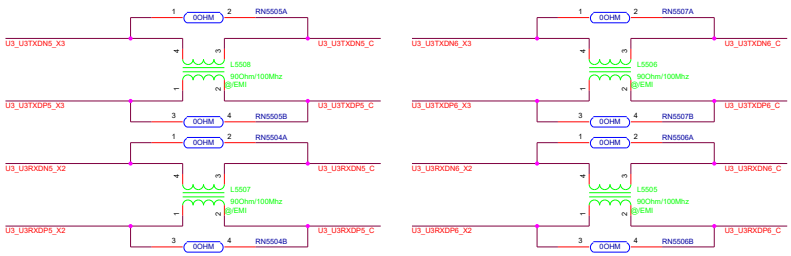


Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I

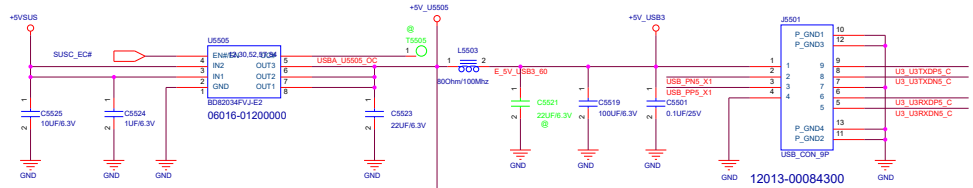
Please check your project must matching the thickness , DF and DK value of PCB every layer

2. C5504&C5503 / C5505&C5506 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13,14,15,16 are floated in regular scheme

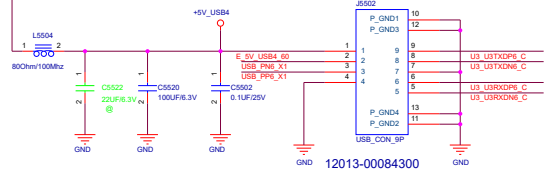
USB3.0 EMI-Protection



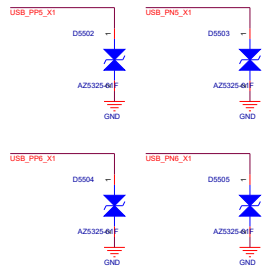
USB3.0 Port 3



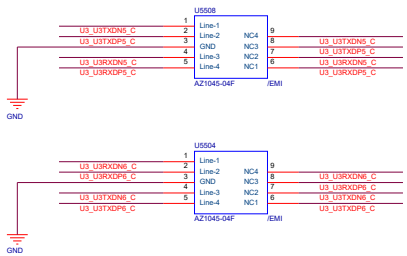
USB3.0 Port 4



USB2.0 ESD-Protection



USB3.0 ESD-Protection

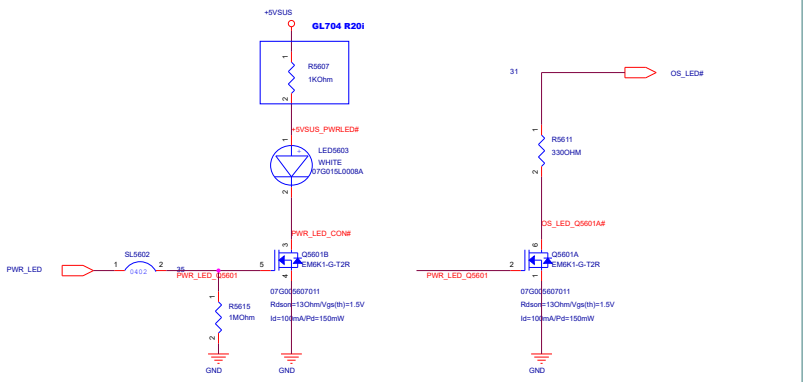


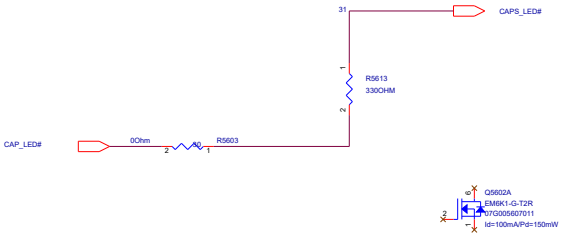
走線請直接由U5504、U5508穿過
至零件另一側之對應 pin 勿成分枝狀走線

U5504, U5508 ESD Diode
1st Source: P/N:07G028076030 ESD PROTECTION AZ1045-04F
2nd Source: P/N:07G028153010 ESD PROTECTION IP4284CZ10-TB

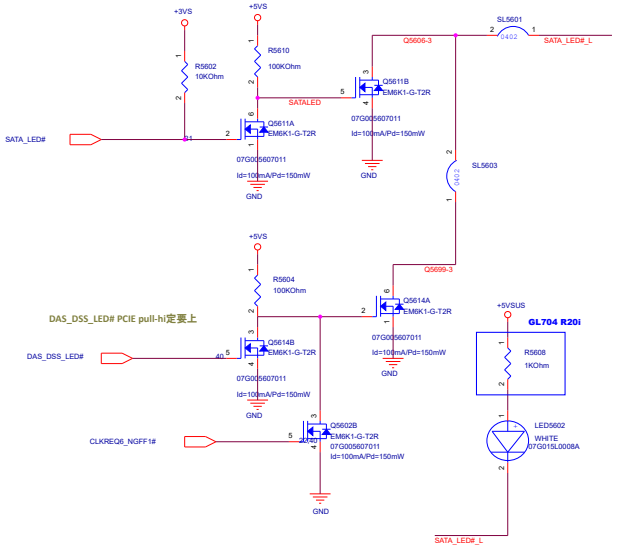
Project Name: GL704GSM			Rev: R1.1
Title : USB3.0 Port			
Size: C	Dept.: ASUSTeK COMPUTER INC	Engineer:	Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 55 of 103		

PWR LED

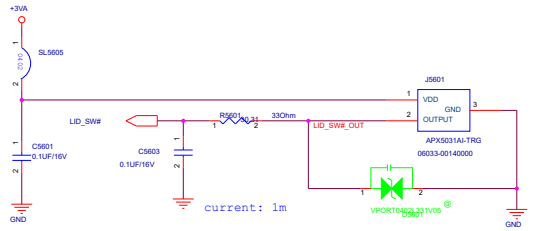




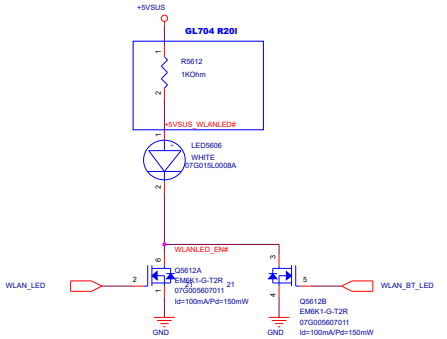
HDD LED & PCIE SSD LED



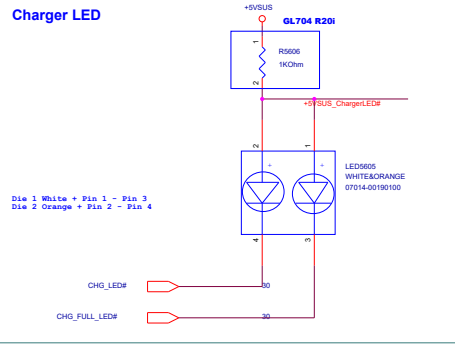
HALL SENSOR
06033-00140000



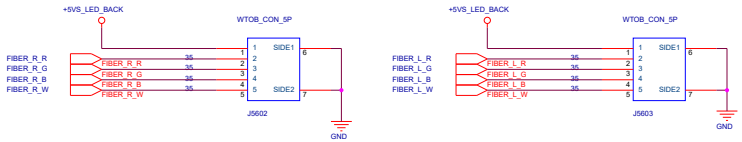
BT/WLAN LED



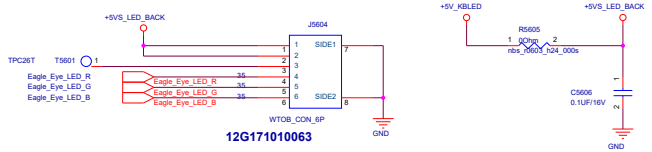
Charger LED



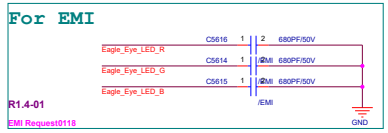
For FIBER LED CTRL



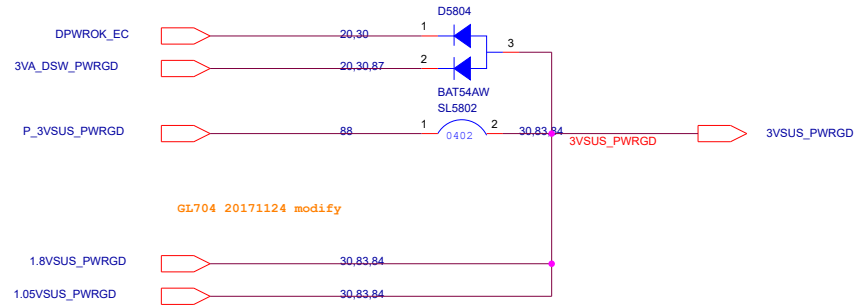
For Eagle Eye LED CTRL

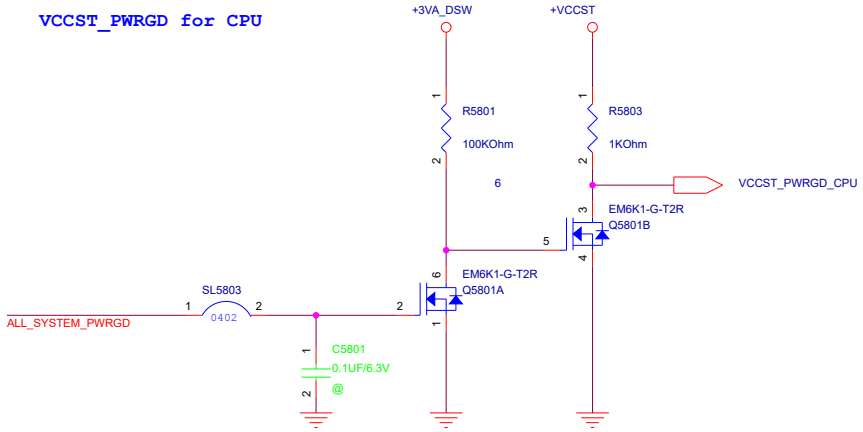


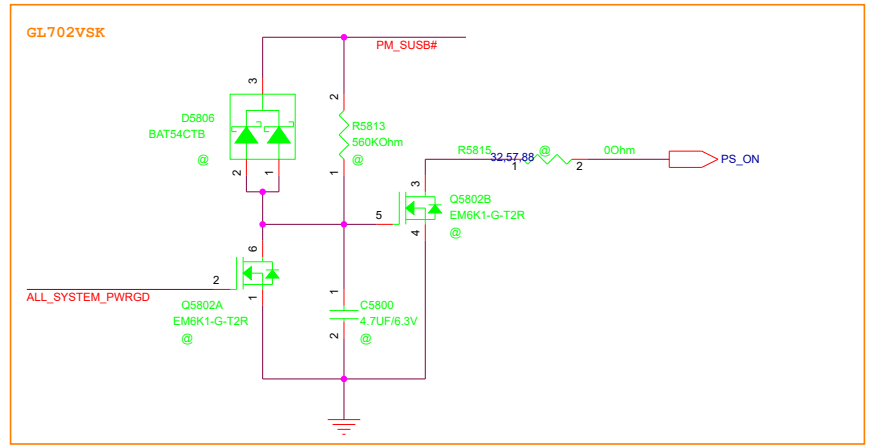
For EMI

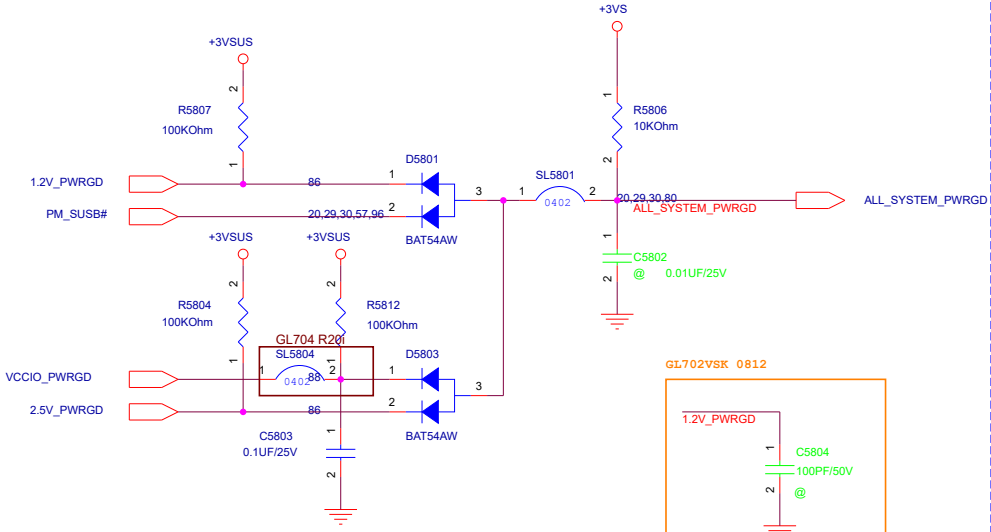


ASUS	Project Name: GL704GSM	Rev: R1.1
Title : LED Indicator		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 56 of 102	

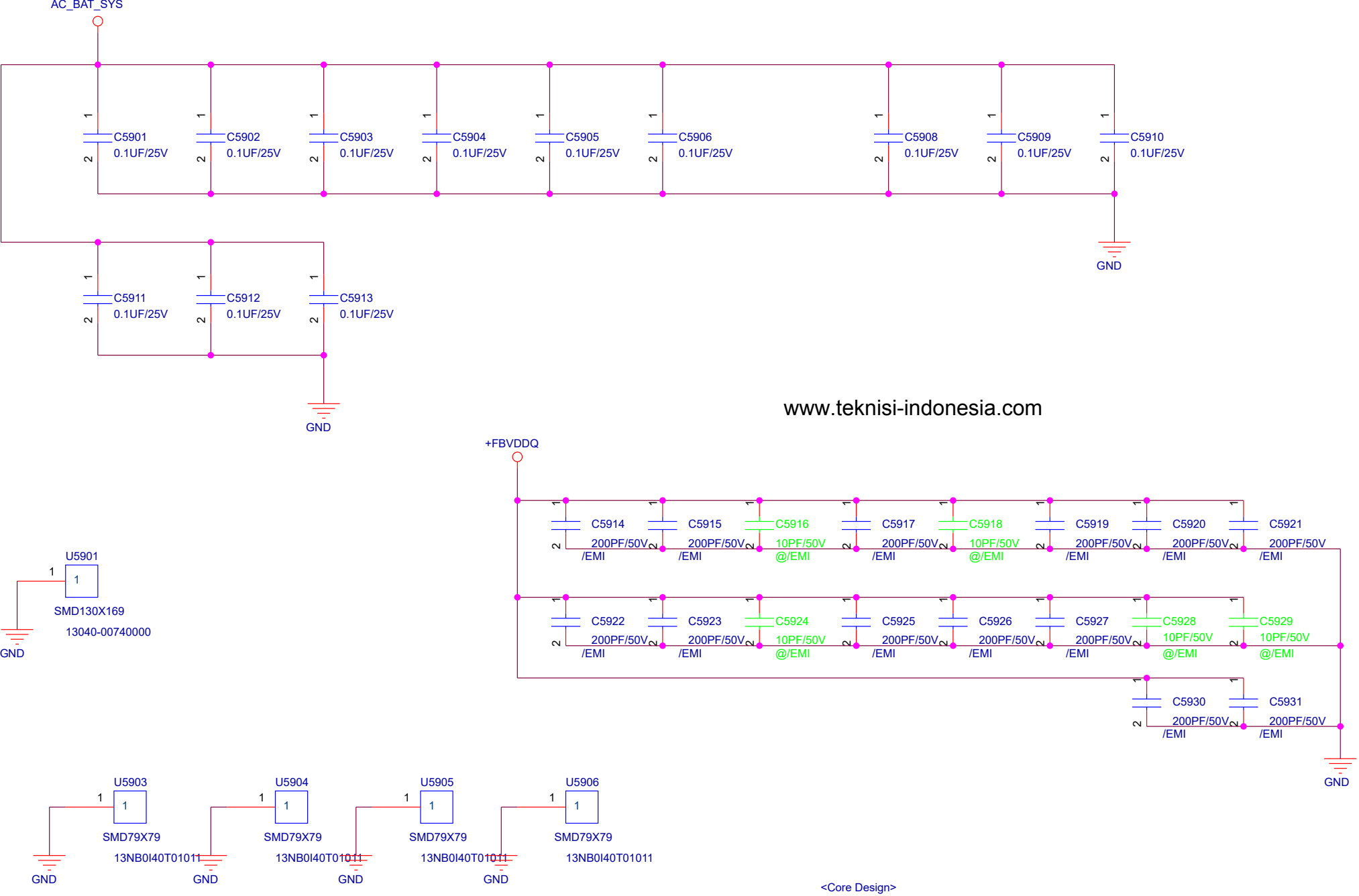








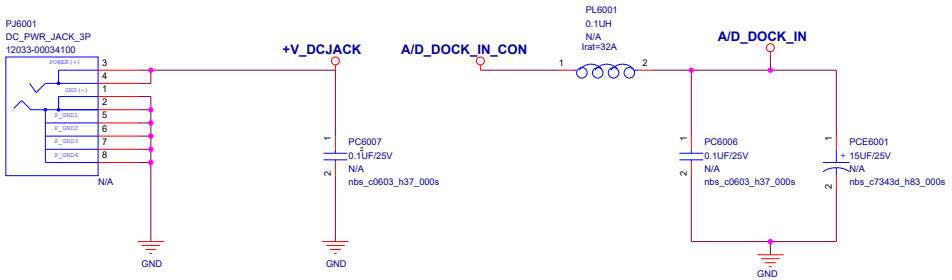
ASUS	Project Name: GL704GSM	Rev: R1.1
Title : Power Protect		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 58 of 103	



<Core Design>

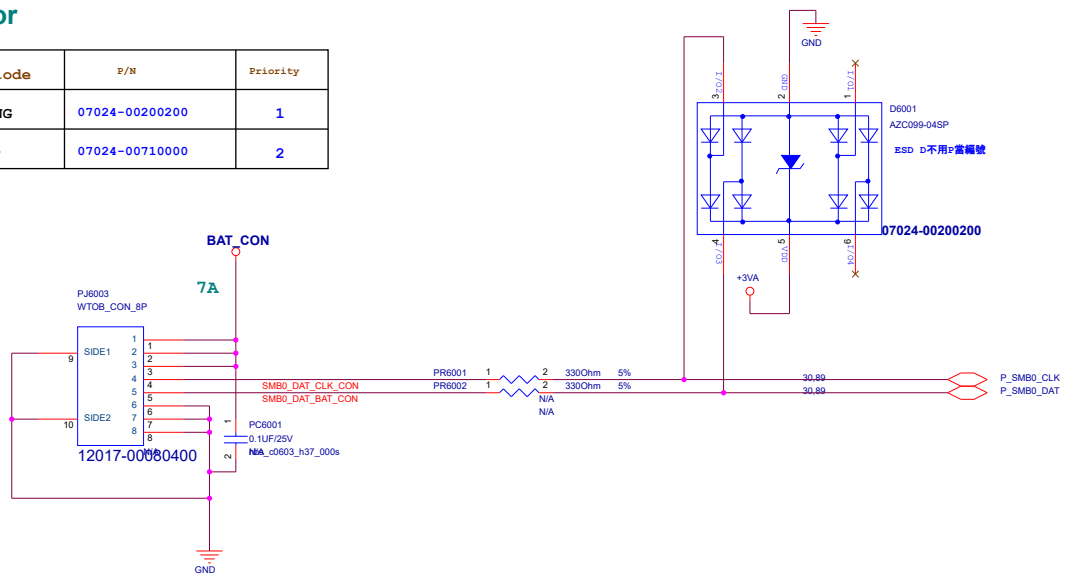
ASUS	Project Name: GL704GSM	Rev: R1.1
Title : EMI		
Size: A	Dept.: ASUSTeK COMPUTER INC. Engineer:	
Date: Friday, July 27, 2018	Sheet 59 of 103	

DC-IN Connector



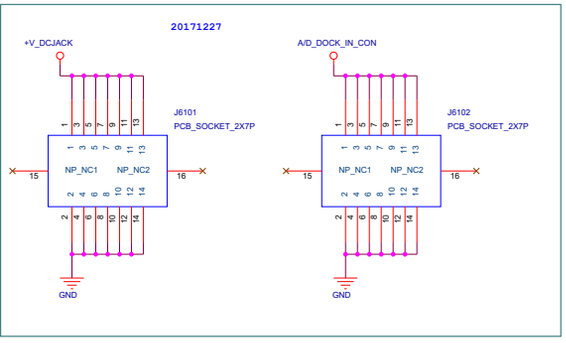
Battery Connector

ESD Diode	P/N	Priority
AMAZING	07024-00200200	1
NXP	07024-00710000	2



Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

Project Name: GL704GM			Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: Hon	
Date: Friday, July 27, 2018	Sheet 60 of 103		



<Core Design>

Project Name: GL704GSM		Rev: R1.1
Title : *****		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 61 of 103	

Project Name

GL704GSM

Rev

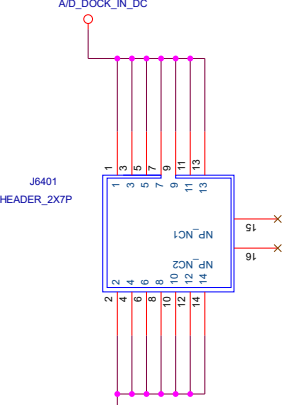
R1.1

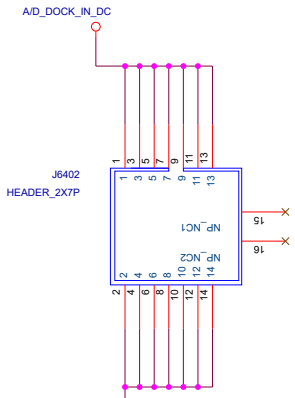
Title : *****

Size	Dept.:	Engineer:
B	ASUSTeK COMPUTER INC.	Gaming RD4 EE1

Date:	Sheet	of
Friday, July 27, 2018	62	103

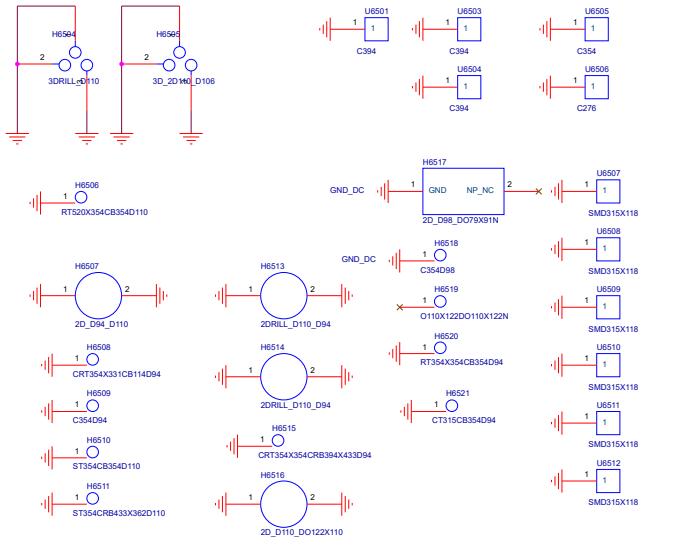
ASUS	Project Name: GL704GSM	Rev: R1.1
Title : Power Button_IO_BD		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 63 of 103	



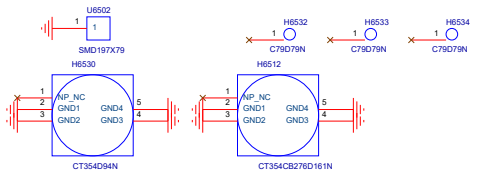


Project Name: GL704GSM		Rev: R1.1
Title : DC_BD		
Size: C	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 64 of 103	

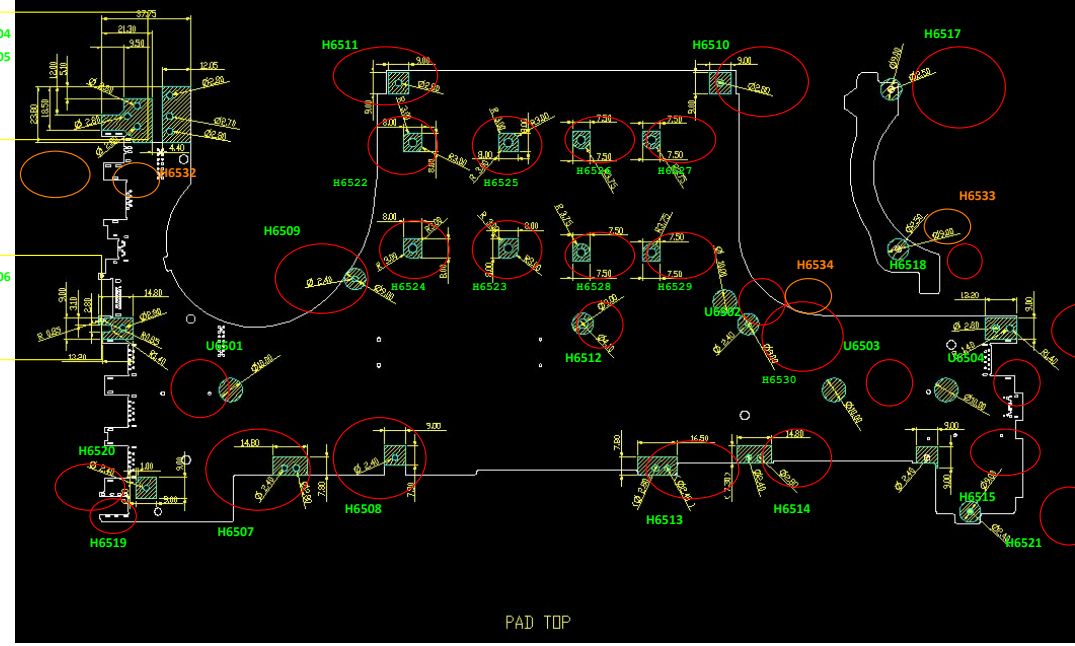
SKEW HOLE & PAD

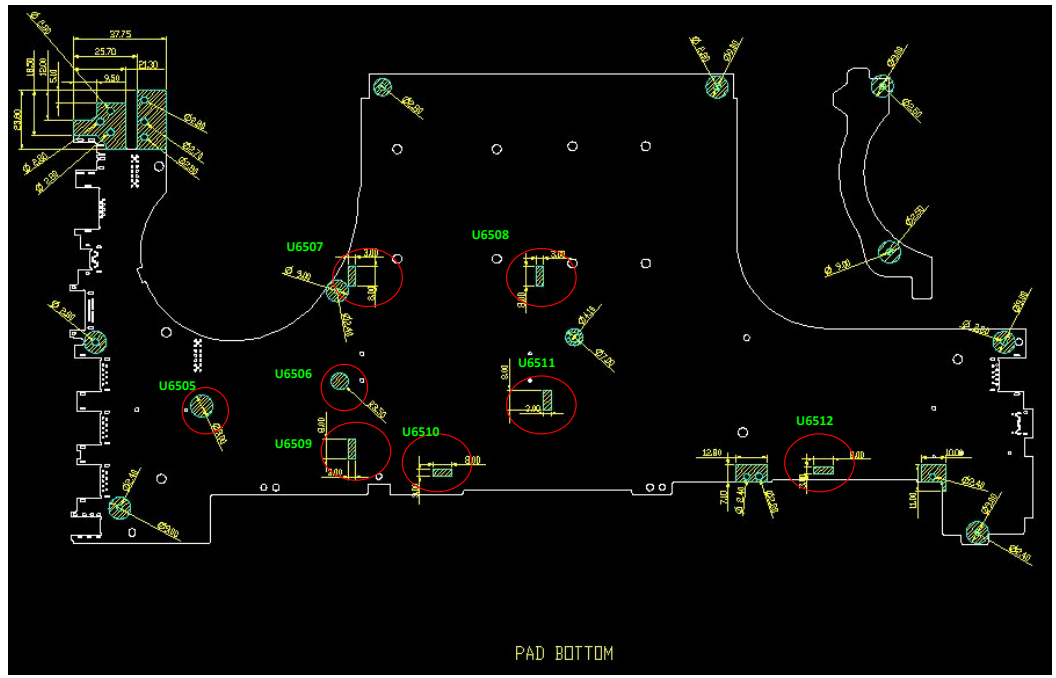


20180416 SR2 update

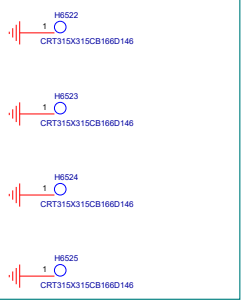


R20e fan hole

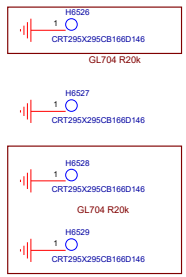




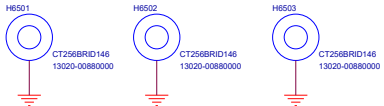
CPU bracket



GPU bracket



FAN NUT



PCH NUT

ASUS	Project Name: GL704GSM		Rev: R1.1
Title : ME_W2B conn. & NUT			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 65 of 103		

Project Name

GL704GSM

Rev

R1.1

Title : *****

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Size	Dept.:	Engineer:
B	ASUSTeK COMPUTER INC.	Gaming RD4 EE1

Date: Friday, July 27, 2018

Sheet 66 of 103

Project Name

GL704GSM

Rev

R1.1

Title : *****

Size	Dept.:	Engineer:
B	ASUSTeK COMPUTER INC.	Gaming RD4 EE1

Date:	Sheet	of
Friday, July 27, 2018	67	103

Project Name

GL704GSM

Rev

R1.1

Title : *****

Size	Dept.:	Engineer:
B	ASUSTeK COMPUTER INC.	Gaming RD4 EE1

Date:	Sheet	of
Friday, July 27, 2018	68	103

Project Name

GL704GSM

Rev

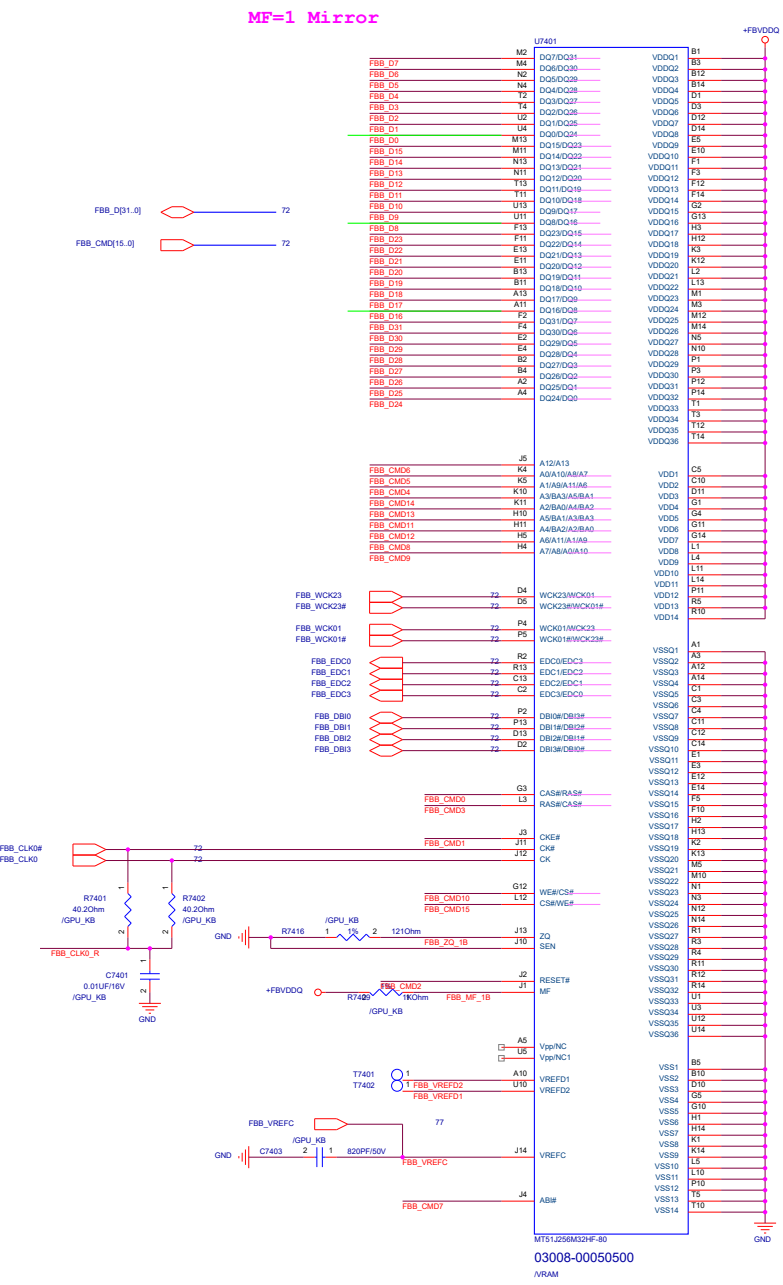
R1.1

Title : *****

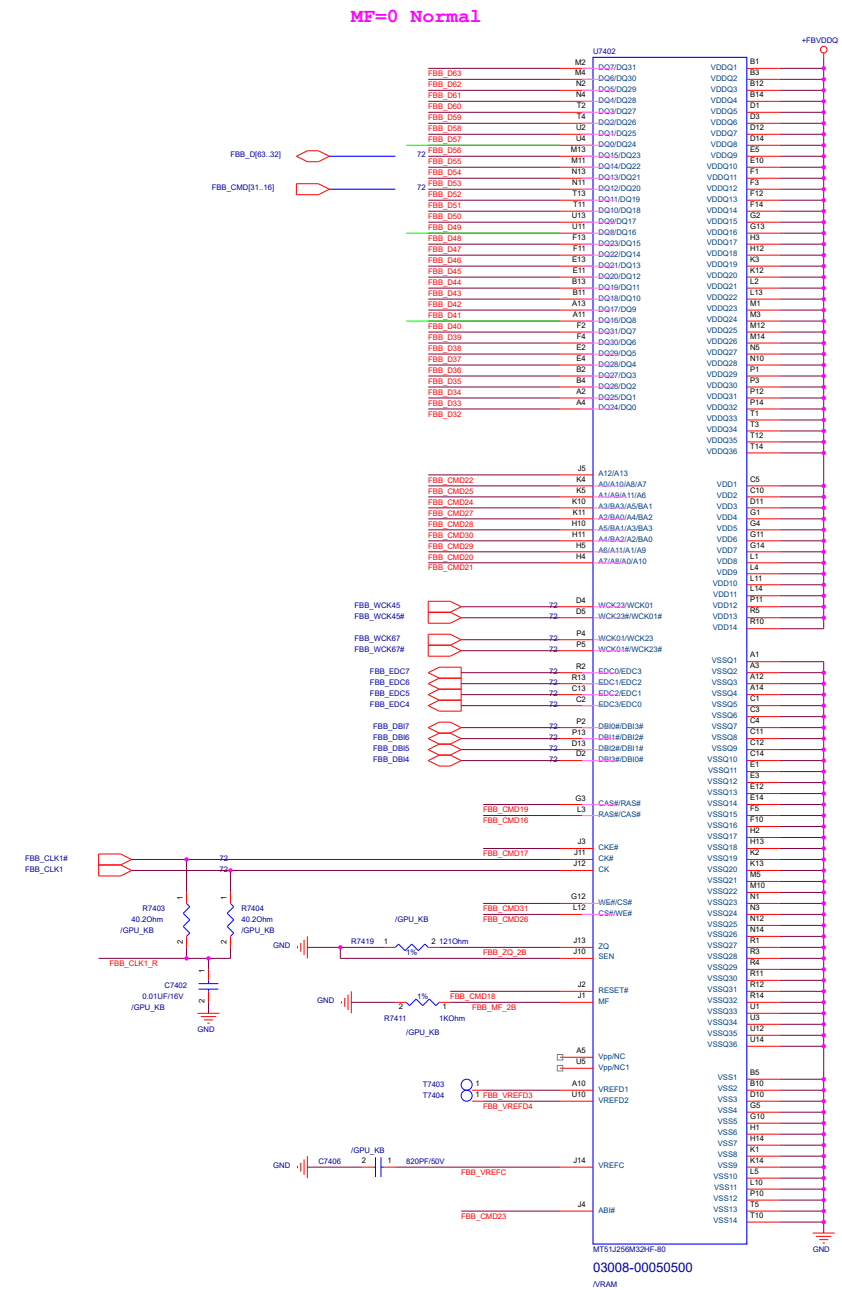
Size	Dept.:	Engineer:
B	ASUSTeK COMPUTER INC.	Gaming RD4 EE1

Date:	Sheet	of
Friday, July 27, 2018	69	103

FBB Partition Memory (1 of 2)



FBB Partition Memory (2 of 2)



R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

ASUSTeK COMPUTER INC. NB1

Title : VRAM-CHANNEL B

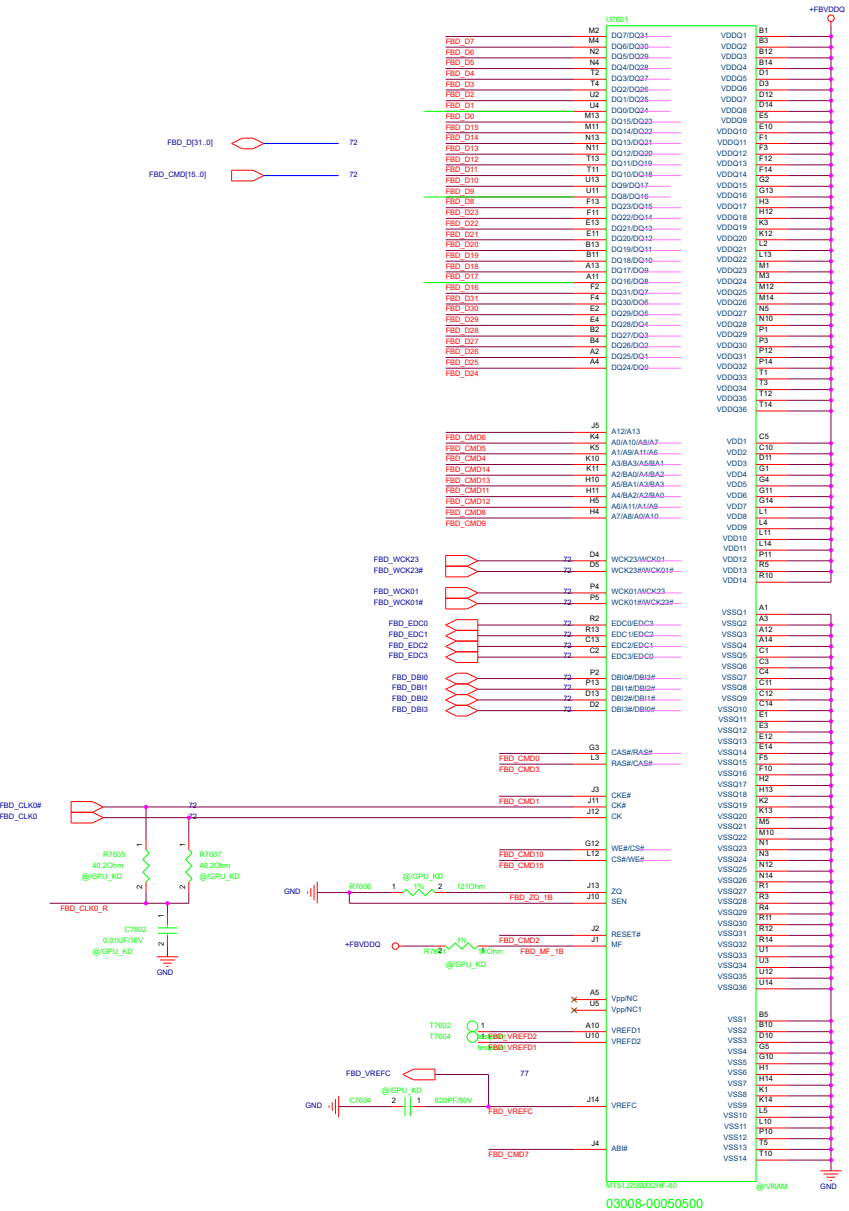
Engineer: Gaming RD4 EE1

Size	Project Name	Rev
C	GL704GSM	R1.1

Date: Friday, July 27, 2018 Sheet 74 of 103

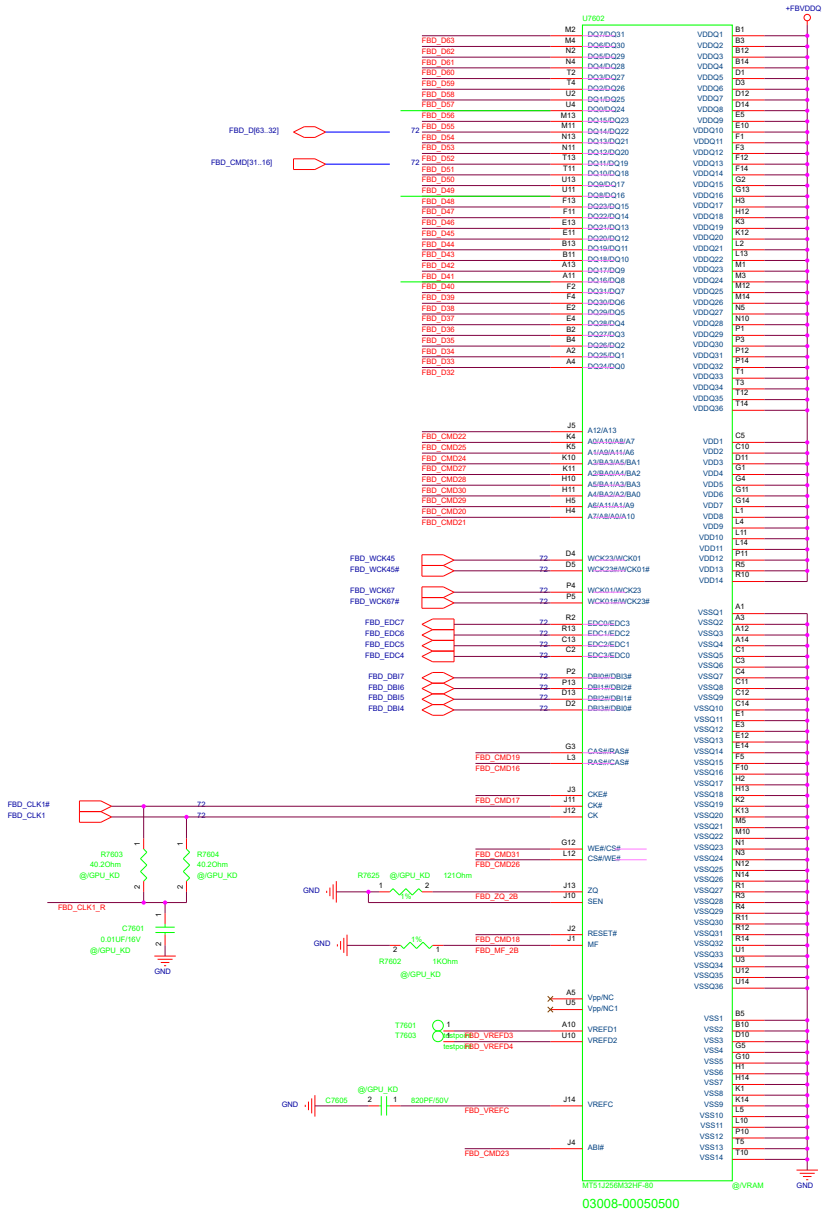
FBD Partition Memory (1 of 2)

MF=1 Mirror



FBD Partition Memory (2 of 2)

MF=0 Normal



R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

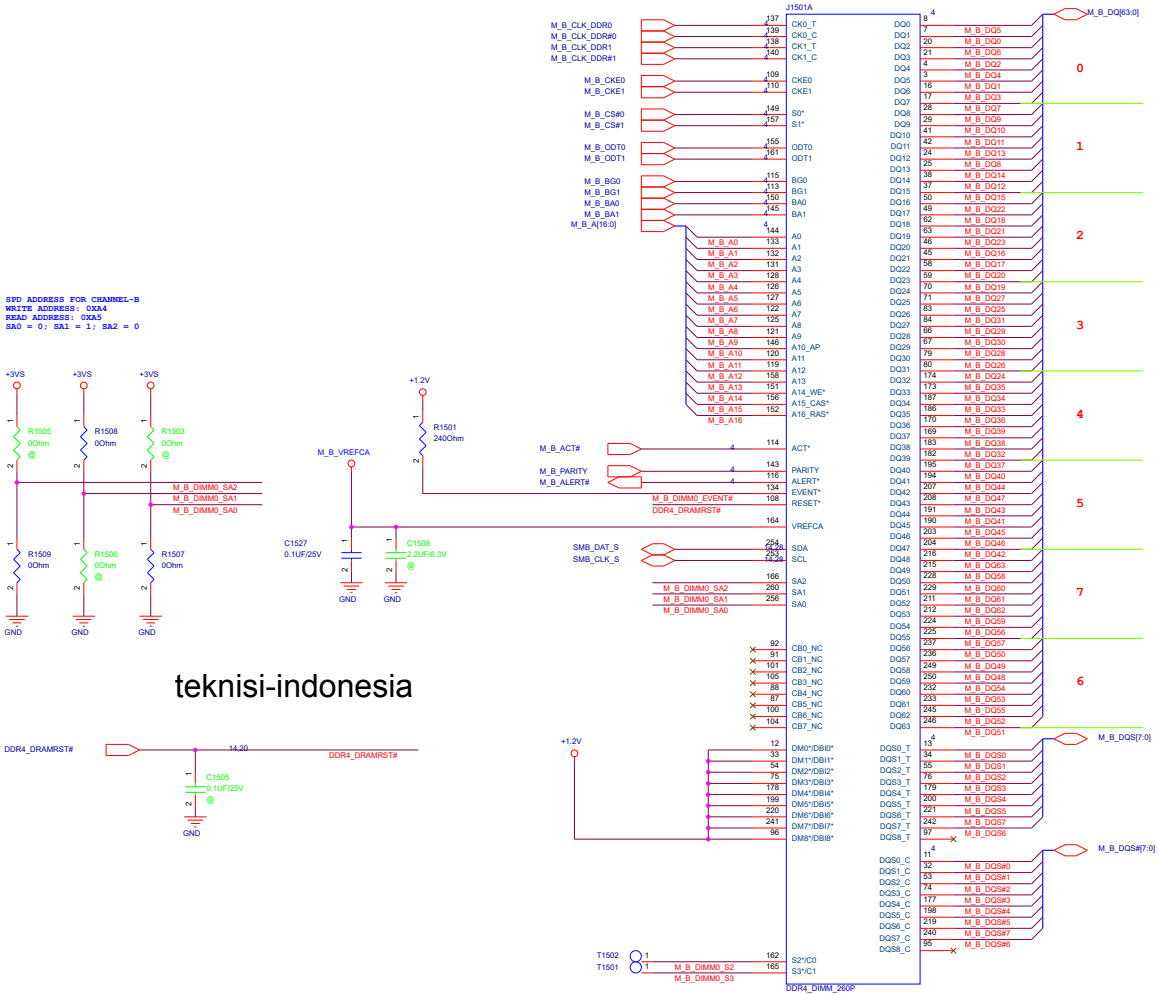
3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

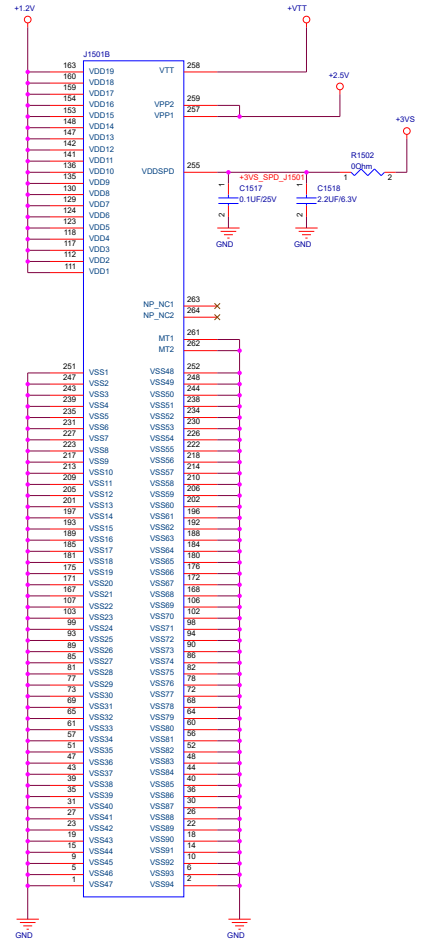
GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

ASUS	Project Name: GL704GSM		Rev: R1.1
Title : VRAM-CHANNEL D			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 76 of 103		

SODIMM CHB-DIMM0
BOT H4.0mm STD (J1501)





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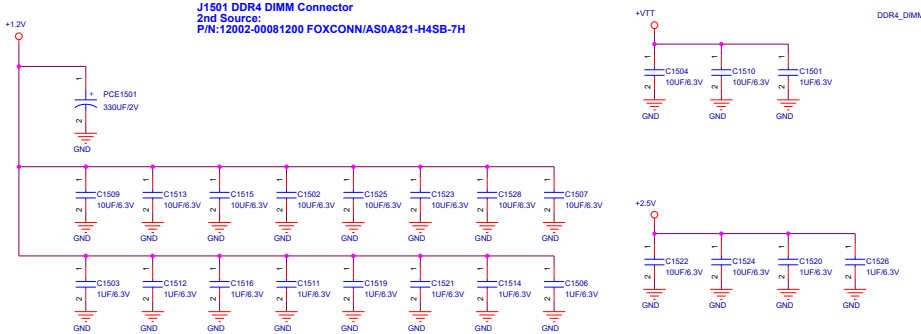
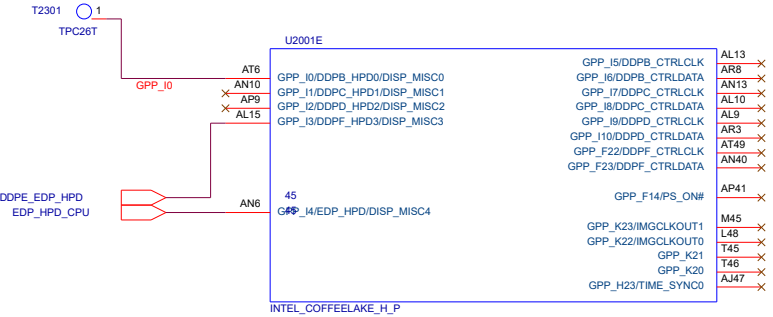
12002-00080300

J1501 DDR4 DIMM Connector
2nd Source:
P/N:12002-00081200 FOXCONN/AS0A821-H4SB-7H

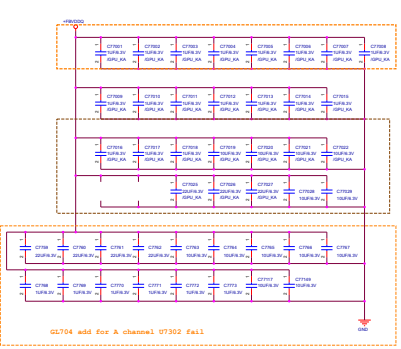


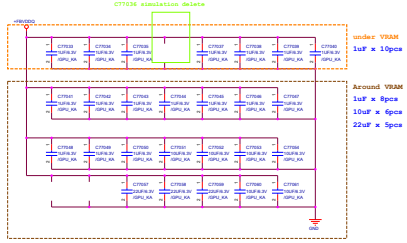
ASUS	Project Name: GL704GSM		Rev: R1.1
Title :	DIM_DDR4 SO-DIMM B(0)		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 15 of 103		



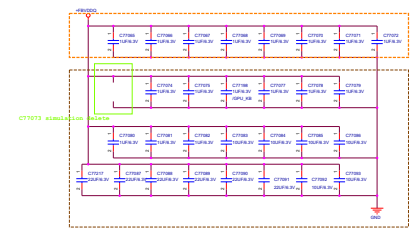
Project Name: GL704GSM		Rev: R1.1
Title : PCH_LVDS,eDP,DP		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 23 of 103	

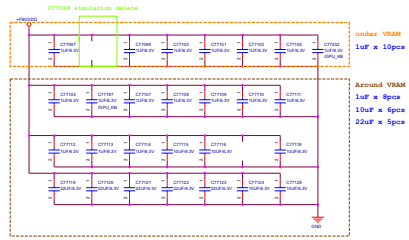
Channel A



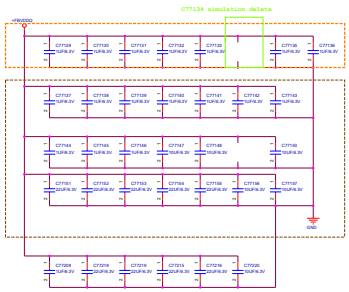


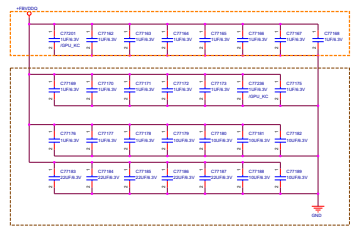
Channel B



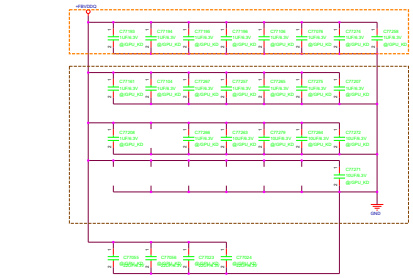


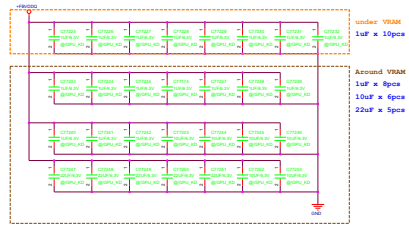
Channel C



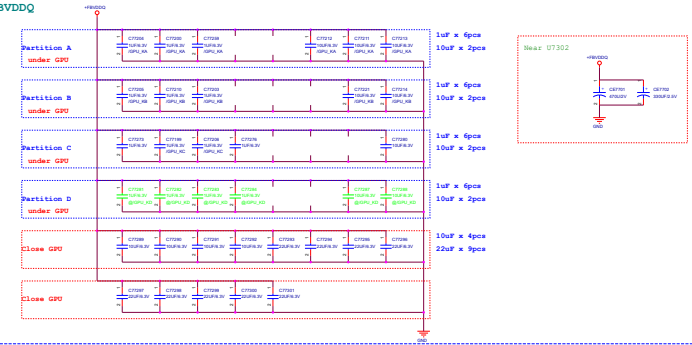


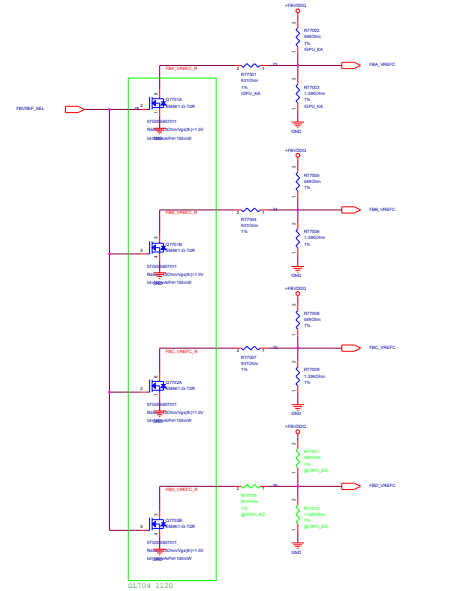
Channel D



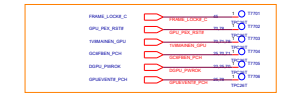


VRAM_PWR_FBVDDQ





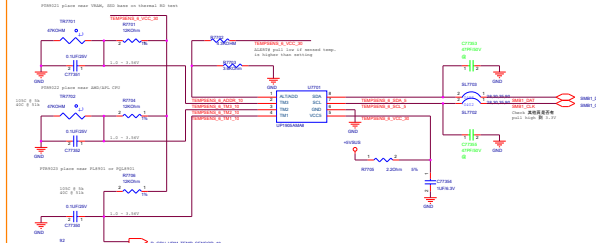
For power sequence measurement

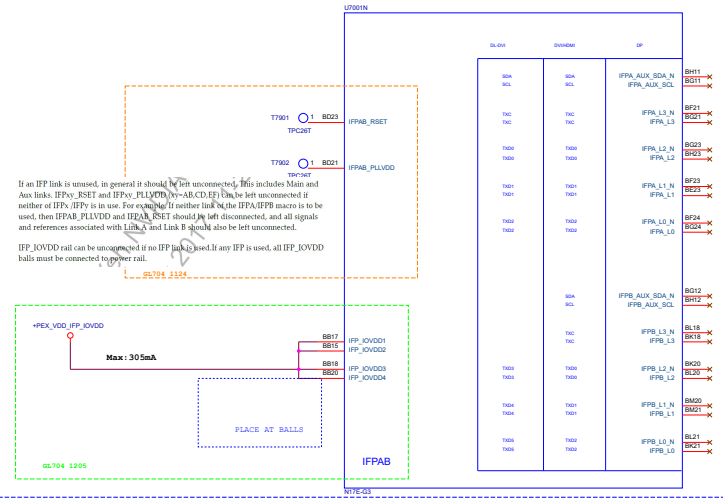


Address Selection Table

Address	0x78	0x7A	0x7C	0x7E	0x74	0x76	0x72	0x70
R7702	10k	1.8k	2k	3.4k	4.7k	6.8k	8.2k	9k
R7703	Open	4.7k	6.8k	8.2k	10k	13k	15k	18k

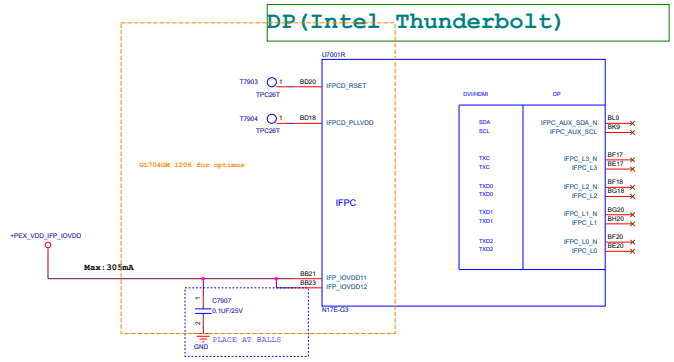
GL702VSK UP1905

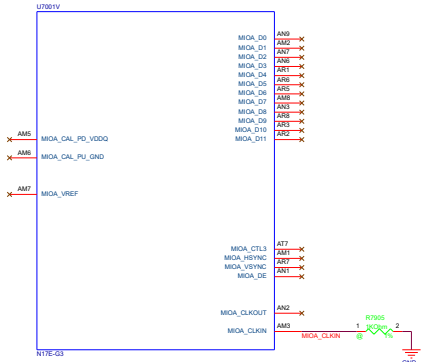


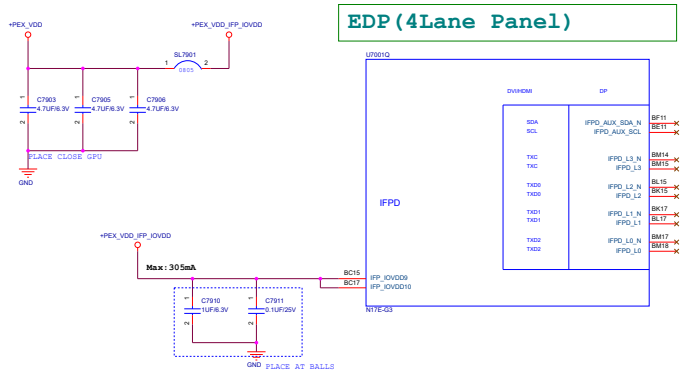


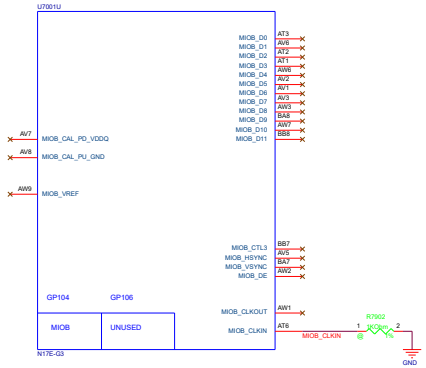
If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx. IFPy is in use. For example, if neither link in the IFPA/IFPB macro is to be used, then IFPAB_PLLVDD and IFPAB_RSET should be left disconnected, and all signals and references associated with Link A and Link B should also be left unconnected.

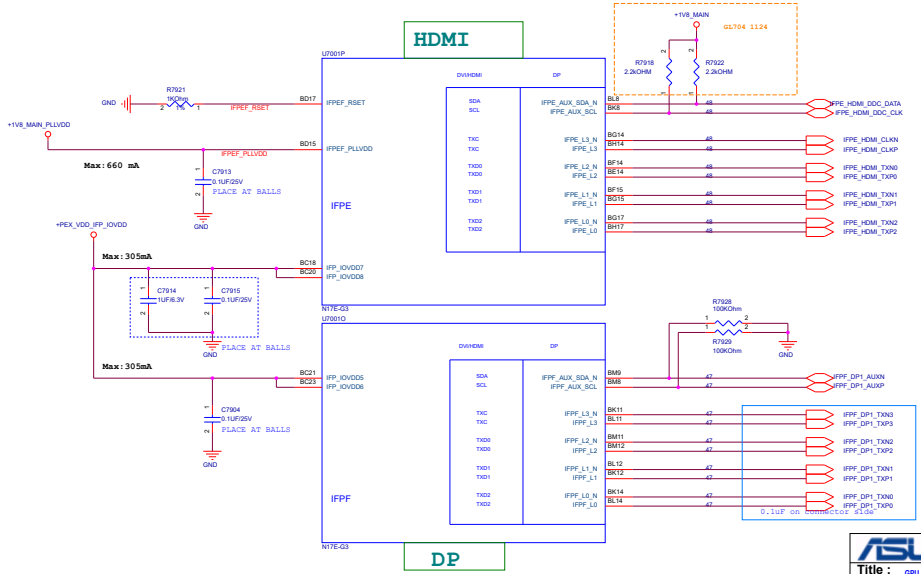
IFP_IOVDD rail can be unconnected if no IFP link is used.If any IFP is used, all IFP_IOVDD balls must be connected to power rail.











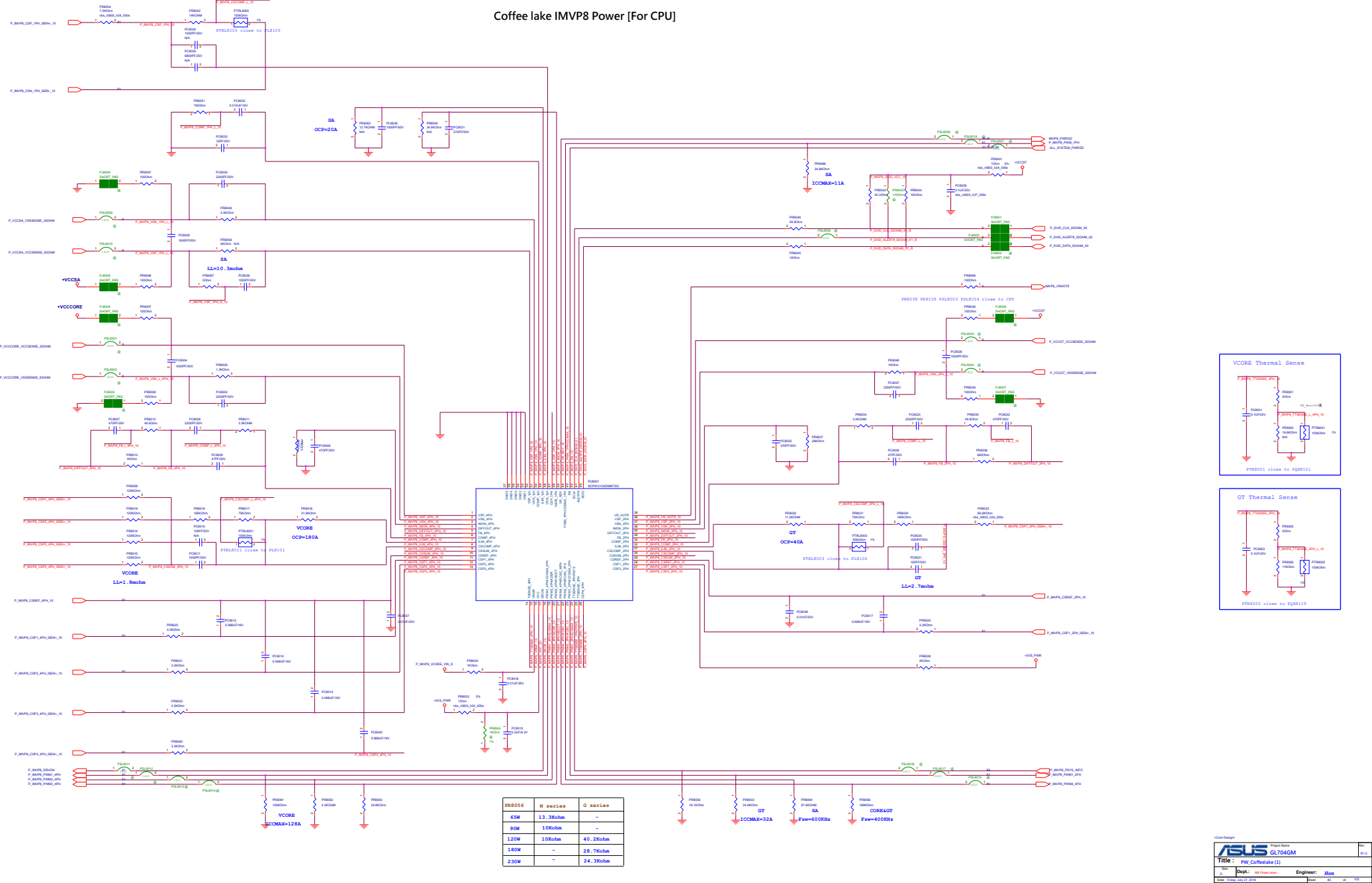
15.2.3 Unconnected Signals (NC)

The following guidelines apply to unused MIO interfaces:

- Power up all VDD18 pins.
- Leave MIO data pins and clock pins floating.

ASUS	Project Name: GL704GSM			Rev: R1.1
Title : GPU_DP/EDP/HDMI/LVDS/CRT				
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1		
Date: Friday, July 27, 2018	Sheet: 79	of: 103		

Coffee lake IMVP8 Power [For CPU]



PR8056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm

<Core Design>

	Project Name **GL704GSM**	Rev R1.1
Title : *****		
Size B	**Dept.:** ASUSTeK COMPUTER INC. **Engineer:** **Gaming RD4 EE1**	
Date: Friday, July 27, 2018	Sheet 46 of 103	

R1.1-02

NGFF M.2 TYPE_E-KEY WIFI

Main Board

BT
USB2.0: BT

PCIE3: WLAN_AC

GPP_C2 BT_UART_WAKE N(PCH_GPP_C2): weak internal pull down
0 : Disable Intel ME Crypto Transport Layer Security(TLS) cipher suite (no confidentiality). (Default)
1 : Enable Intel ME Crypto Transport Layer Security(TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.

J5301_NGFF E-KEY WLAN Connector H=2.0mm
1st Source: P/N:12003-00076000 ARGOSY/NASE0-S6701-TP20
2nd Source: P/N:12003-00075200 DRAGONSTATE/213EBAA2FFB
3rd Source: P/N:12003-00075800 LOTES/APCI0062-P001A

12003-00160100

WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSUS

WLAN CLKREQ#

WLAN & BT ON

To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

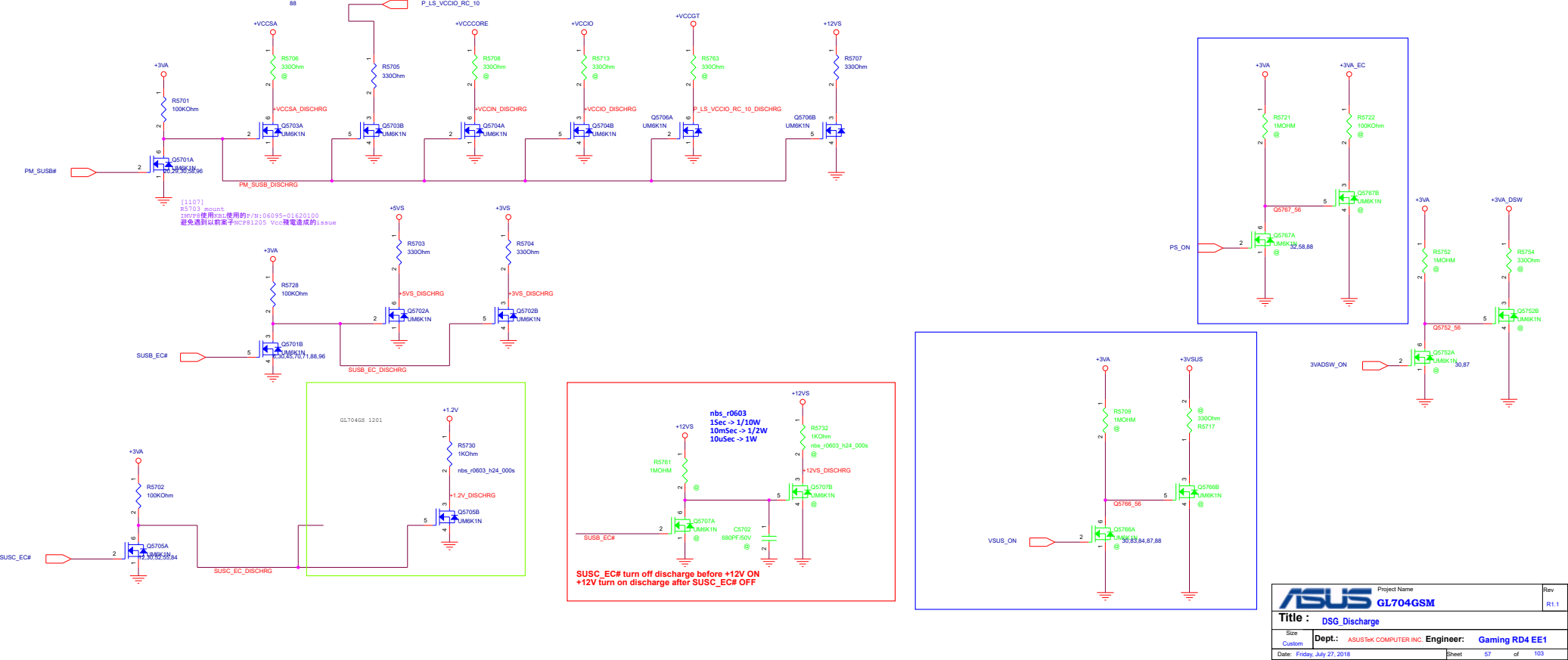
High active

Project which use the combo card schematic should make sure that BT_ON signal can't be High at S3/S4/S5 state to prevent leakage

WLAN_Wake# Control

For EMI

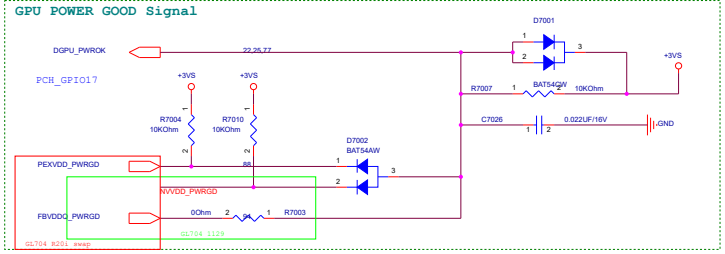
WLAN NUT

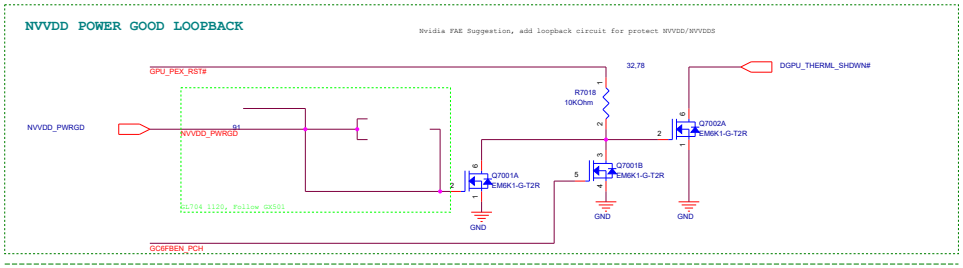


Project Name: GL704GSM		Rev: R1.1
Title: DSG_Discharge		
Size: Custom	Dept.: ASUSTeK COMPUTER INC. Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 57 of 103	

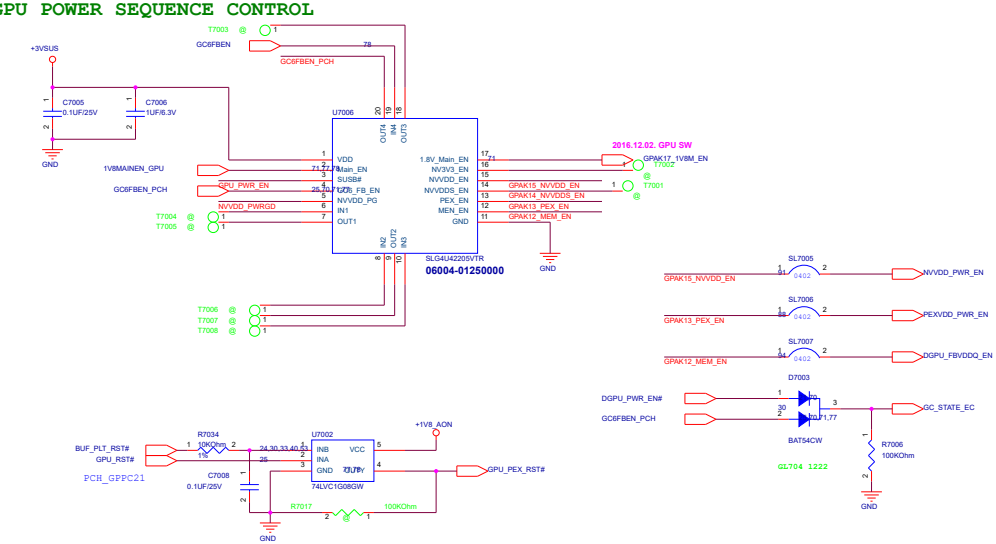
PCI EXPRESS_Graphics

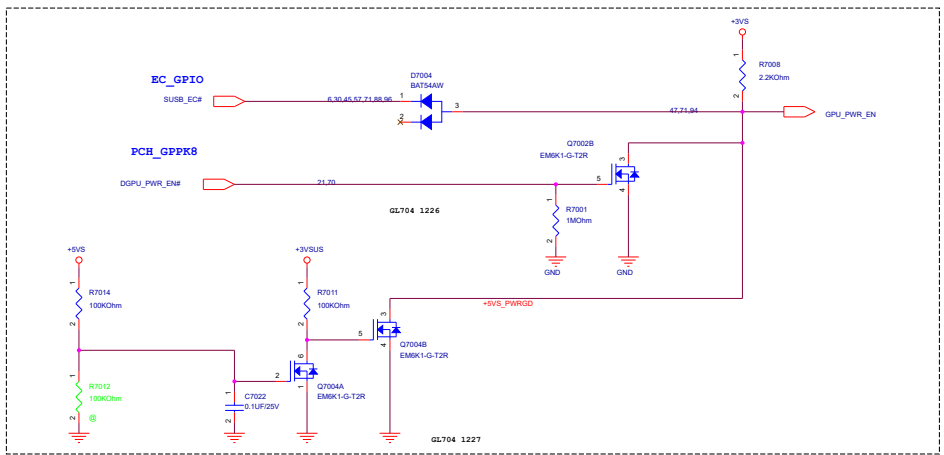
REVERSED Type PCIE X16

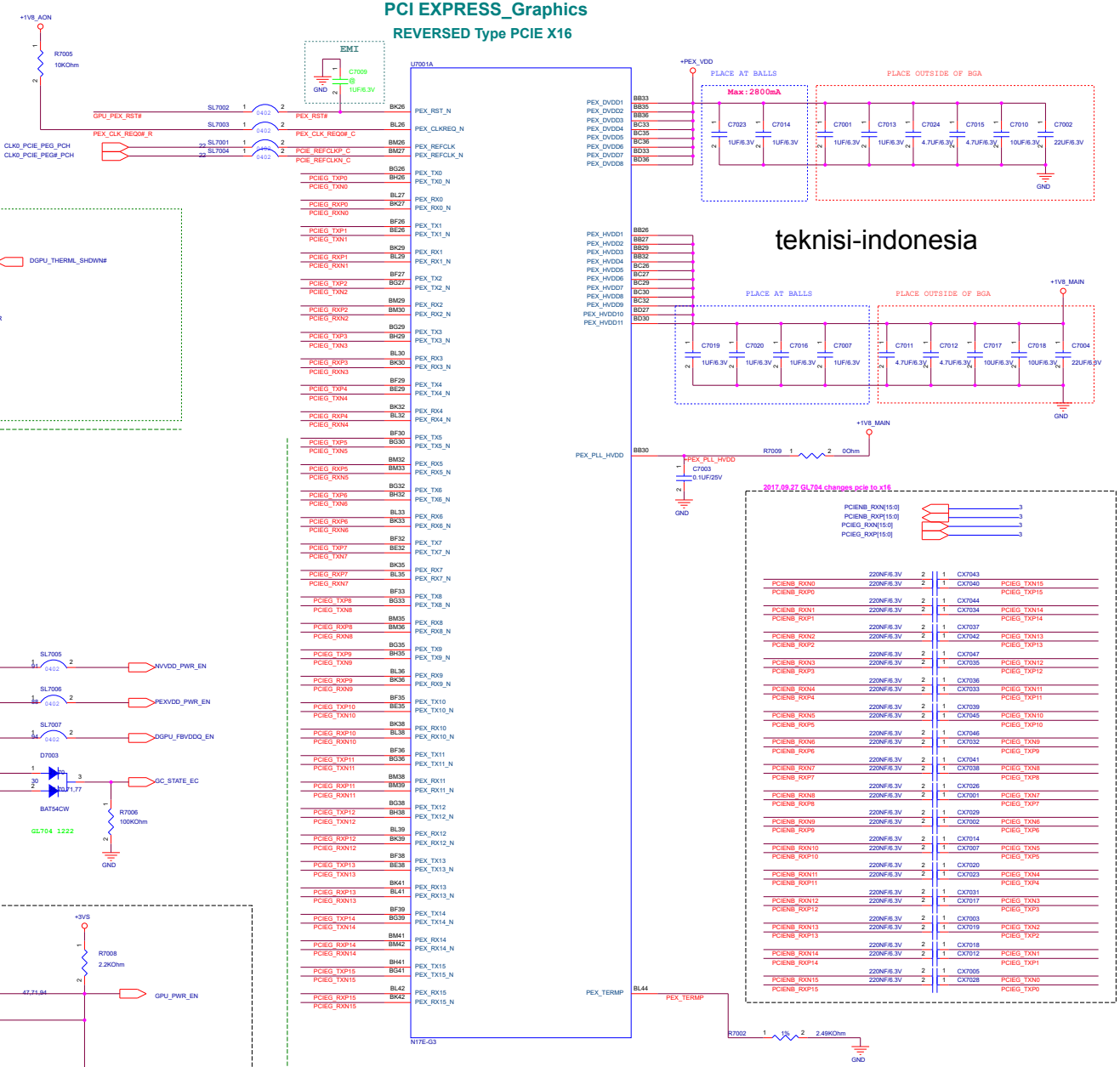




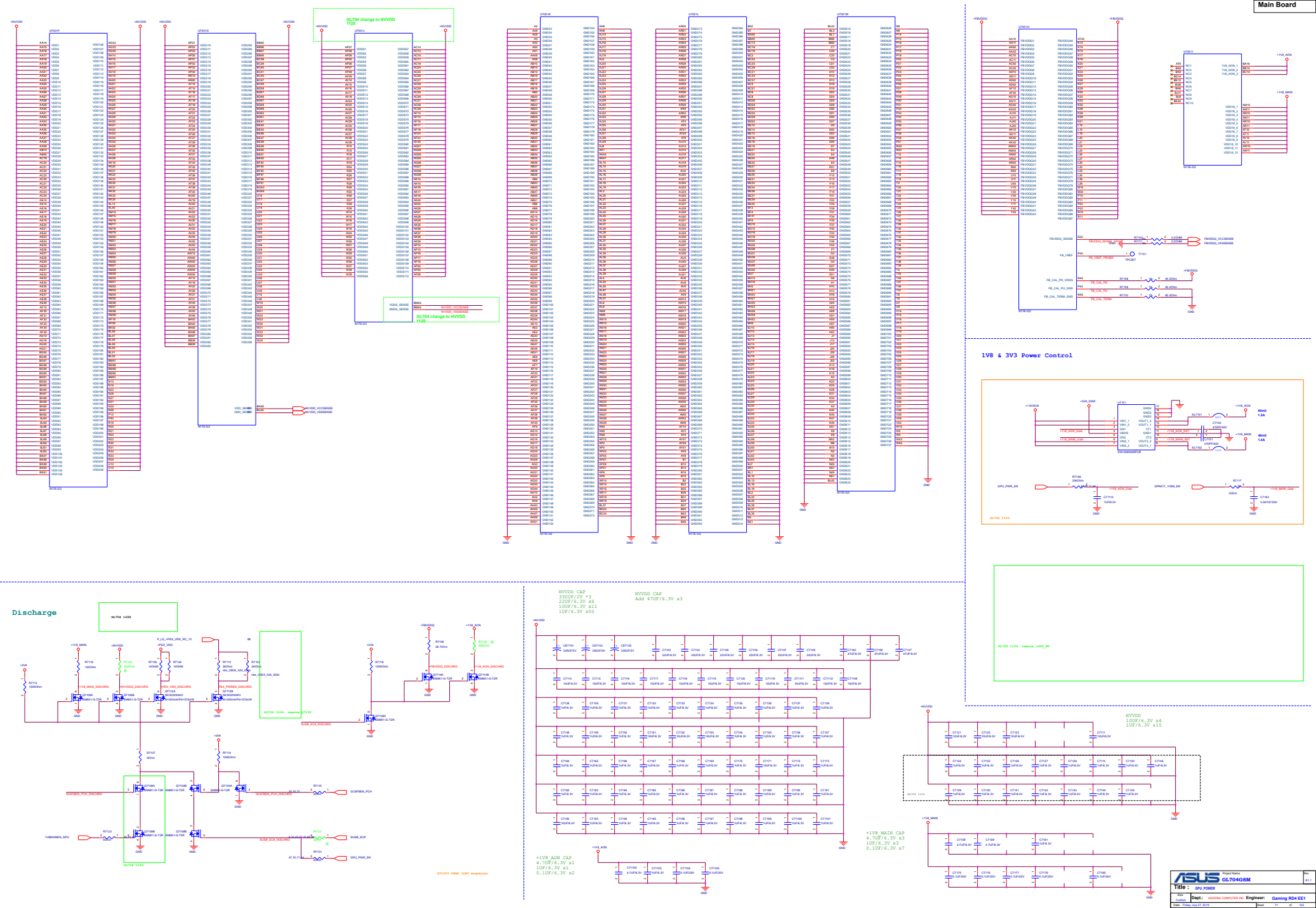
GPU POWER SEQUENCE CONTROL



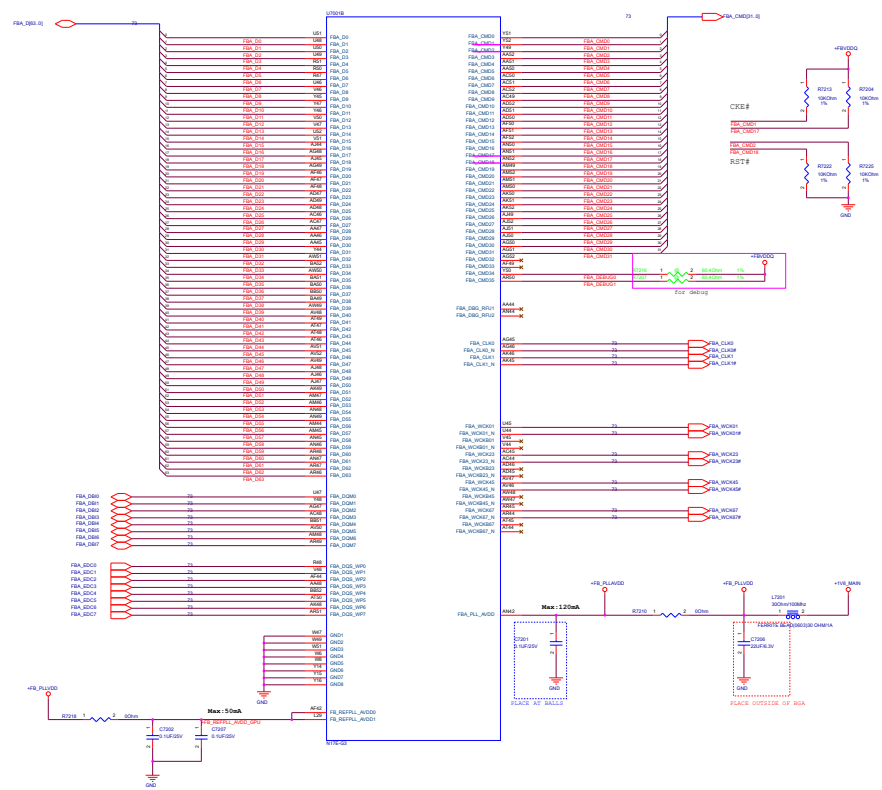




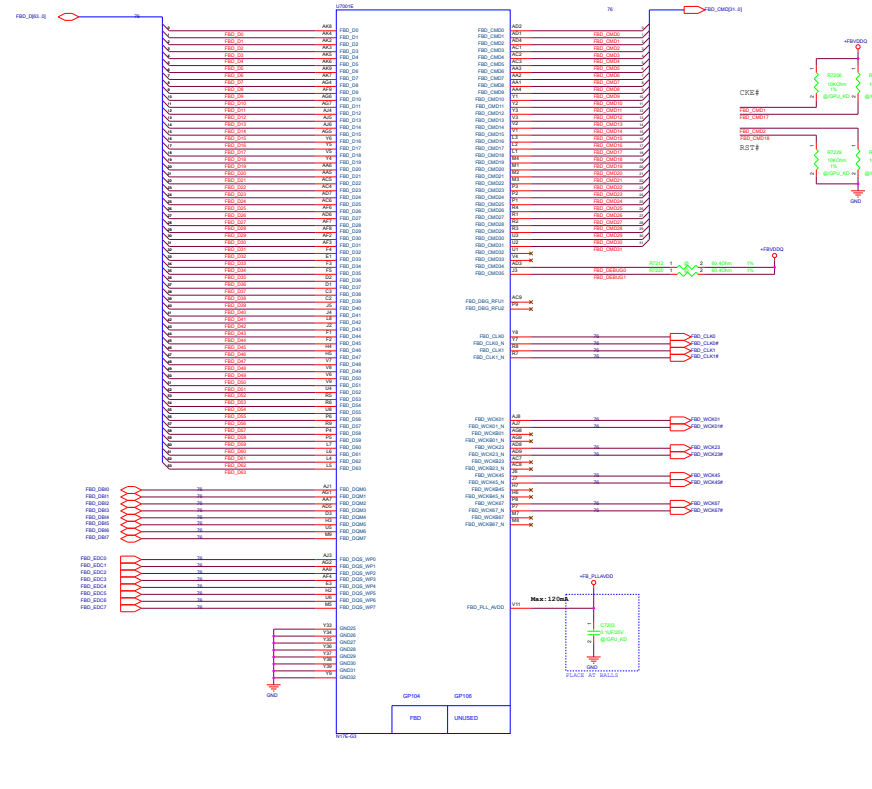
ASUS	Project Name: GL704GSM		Rev: R1.1
Title : GPU_PCIE I/F			
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: Gaming RD4 EE1	
Date: Friday, July 27, 2018	Sheet 70 of 103		


Main Board
GL704 change to NVVDD
1120
GL704 change to NVVDD
1120
1V8 & 3V3 Power Control
Discharge
NVVDD CAP
330UF/2V *3
220UF/6.3V x6
100UF/6.3V x11
10UF/6.3V x50
NVVDD CAP
Add 47UF/6.3V x3
NVVDD
100UF/6.3V x4
10UF/6.3V x15
+1V8_MAIN CAP
4.7UF/6.3V x3
10UF/6.3V x3
0.1UF/6.3V x7
+1V8_AON CAP
4.7UF/6.3V x1
10UF/6.3V x1
0.1UF/6.3V x2
ASUS
Project Name
GL704GSM
Title :
GPU_POWER
Dept.:
Engineer:
Gaming RD4 EE1

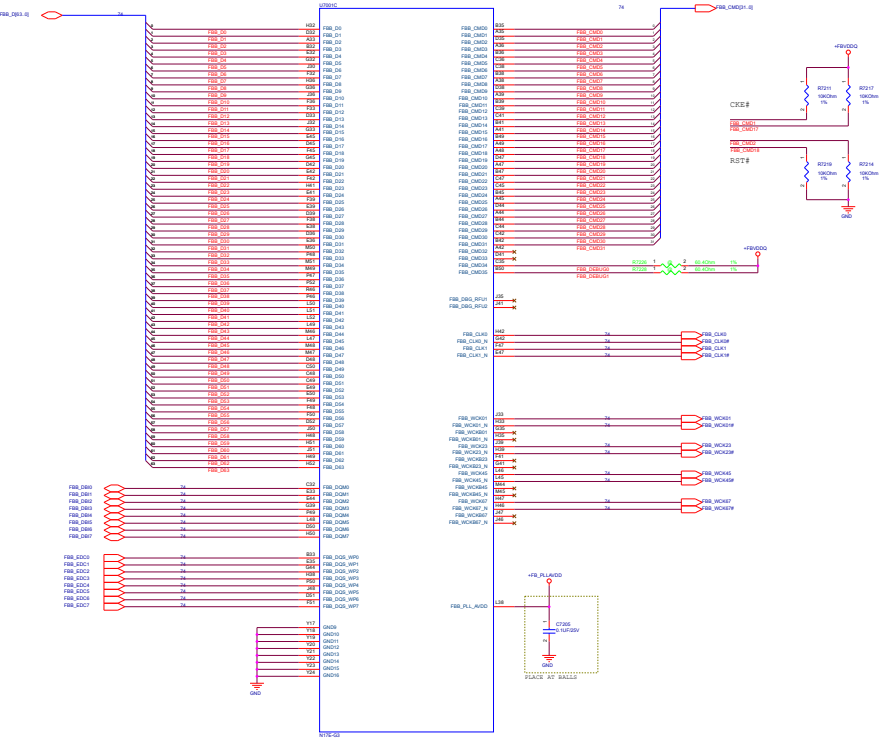
MEMORY: GPU FB Partition A



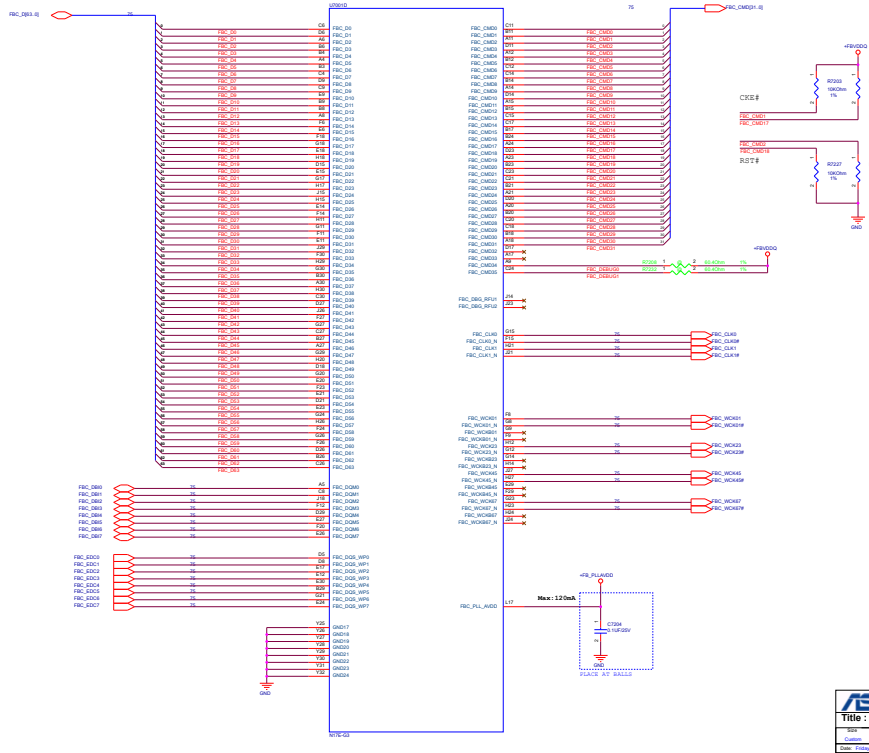
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B



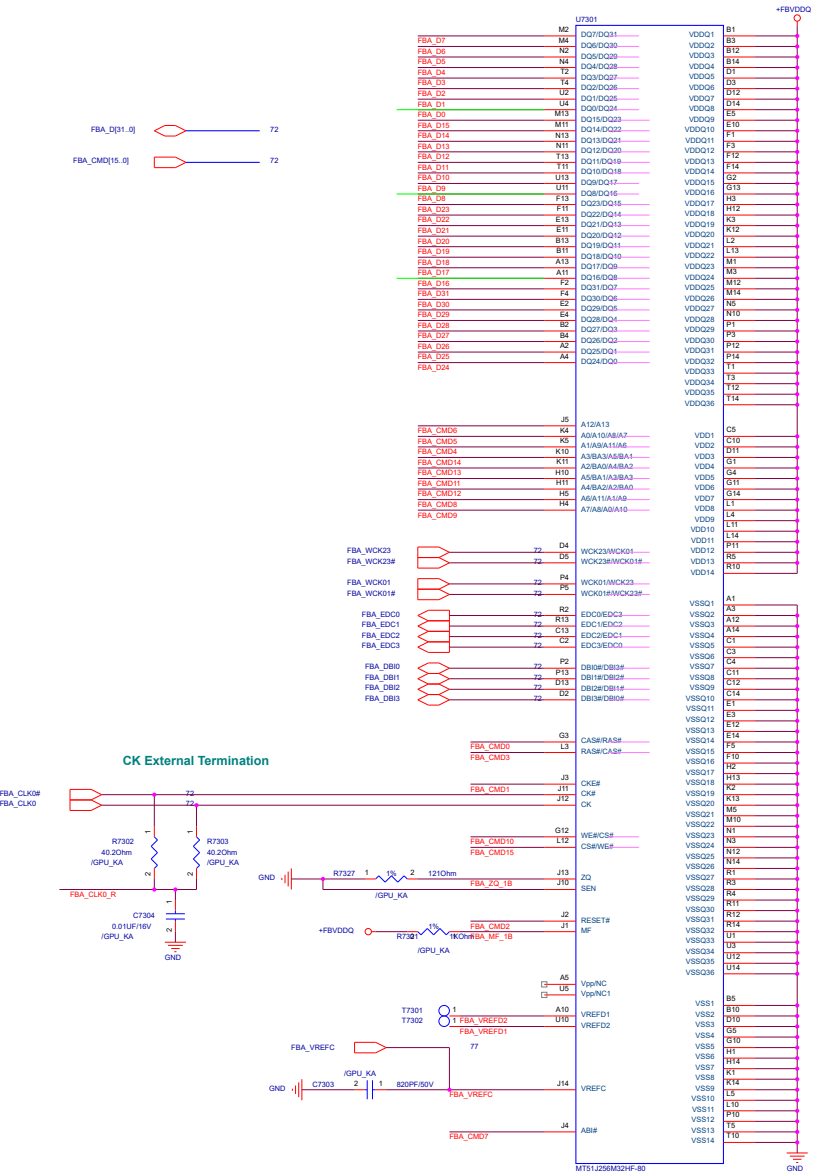
MEMORY: GPU FB Partition C



ASUS	Project Name: GL704GSM		Rev: 81.1
Title : GPU_FRAME BUFFER			
Size: Custom	Dept.: ASUSTek COMPUTER INC	Engineer:	Gaming RD4 EE1
Date: Friday, July 27, 2018	Sheet 12 of 160		

FBA Partition Memory (1 of 2)

MF=1 Mirror



FBA Partition Memory (2 of 2)

MF=0 Normal

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

ASUSTeK COMPUTER INC. NB1

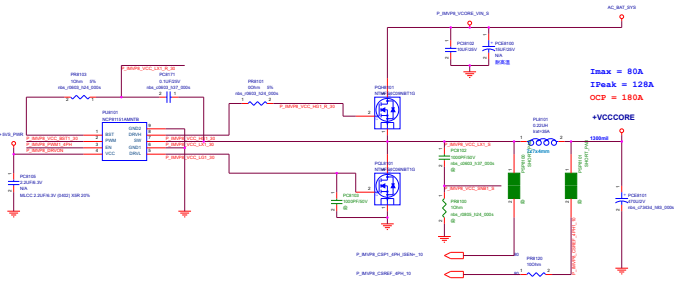
Title : VRAM-CHANNEL A

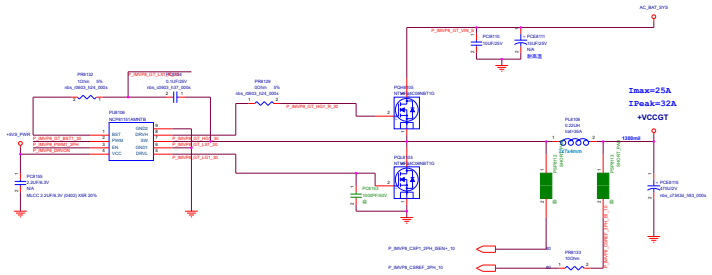
Engineer: Gaming RD4 EE1

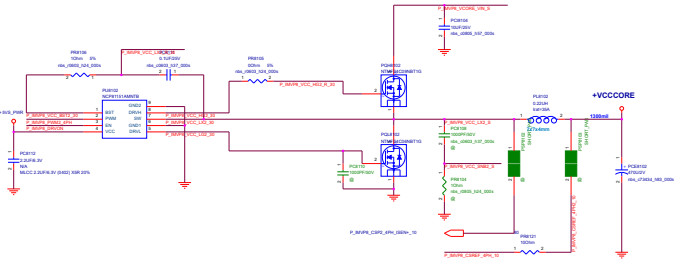
Size	Project Name	Rev
C	GL704GSM	R1.1

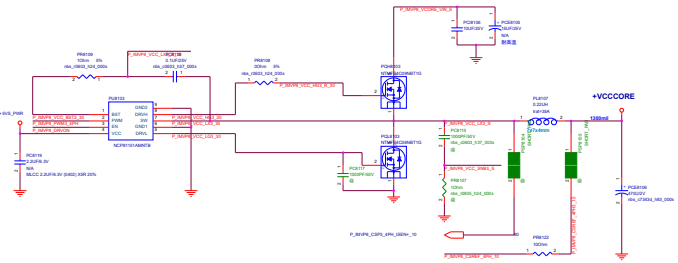
Date: Friday, July 27, 2018 Sheet 73 of 103

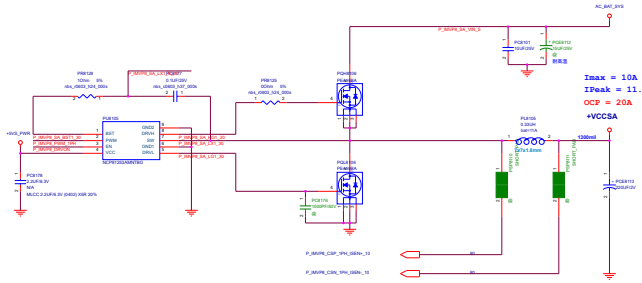
Coffee lake IMVP8 Power [For CPU]

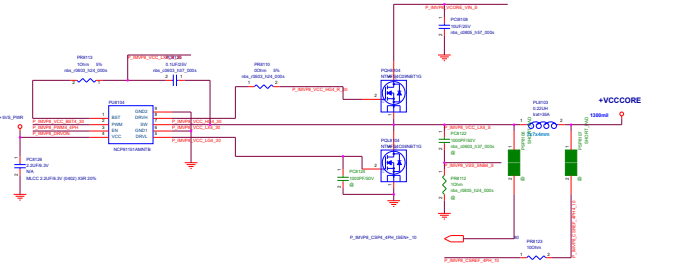






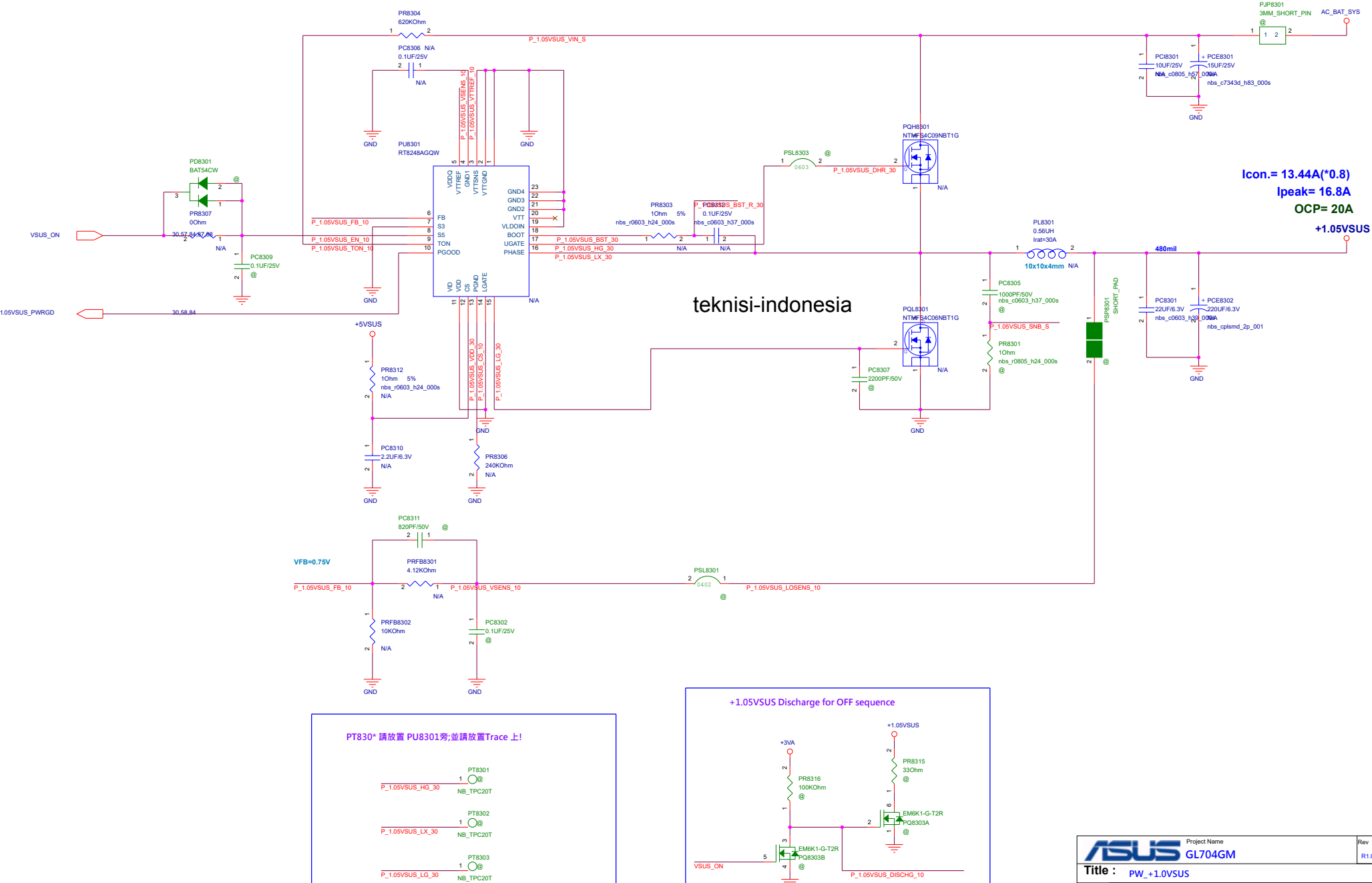






ASUS GL704GM
Project Name: PW_COFFEELAKE (2)
Title :
Size: A3
Dept.: NB Power team
Engineer: Hsin
Date: Friday, July 27, 2018
Sheet 61 of 103

+1.05VSUS [For PCH]

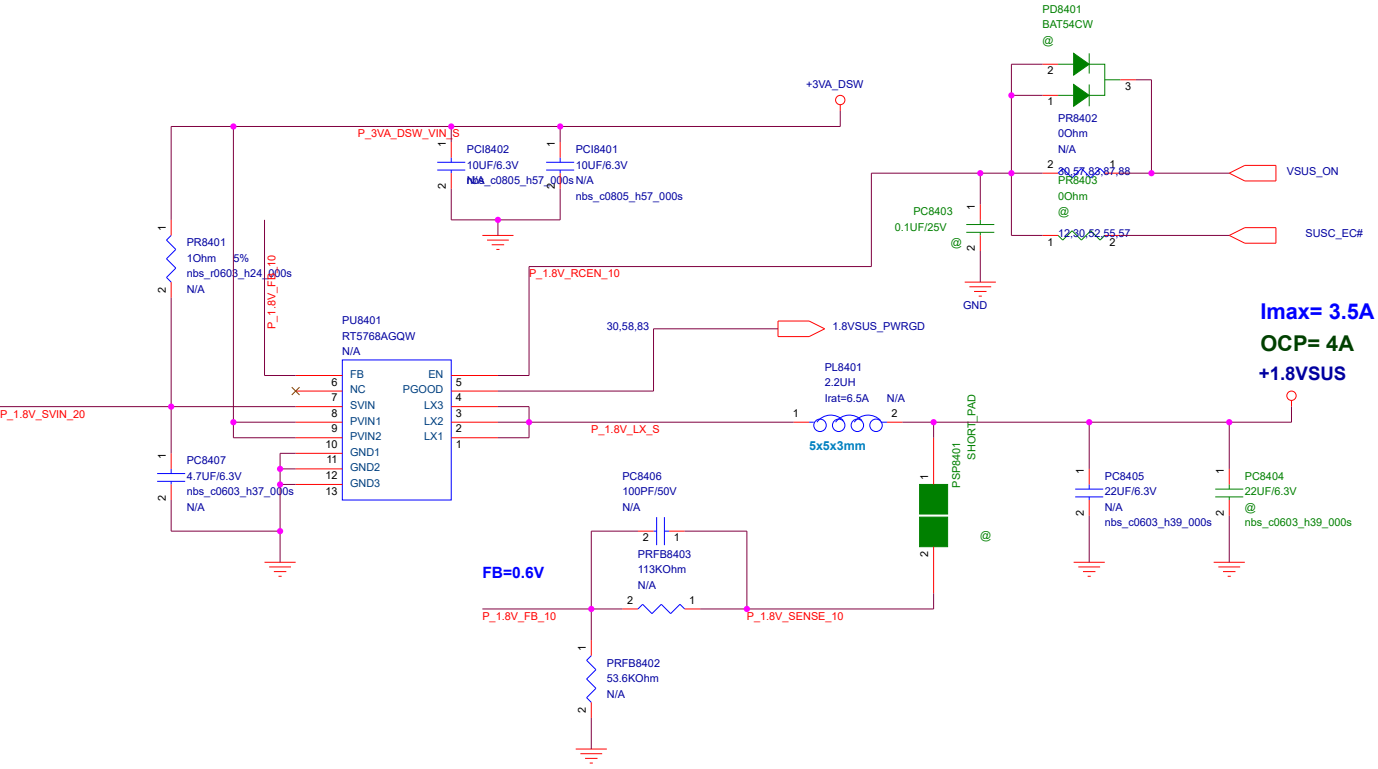


PT830* 請放置 PU8301旁;並請放置Trace 上!

+1.05VSUS Discharge for OFF sequence

ASUS	Project Name: GL704GM		Rev: R1.0
Title : PW_+1.0VSUS			
Size: A3	Dept.: NB Power team	Engineer: Hon	
Date: Friday, July 27, 2018	Sheet 83 of 103		

+1.8VSUS [For PCH]



<Variant Name>

ASUS	Project Name: GL704GM	Rev: R1.0
Title : PW_+1.8VSUS		
Size: A3	Dept.: NB Power Team	Engineer: Hon
Date: Friday, July 27, 2018	Sheet 84 of 103	

Project Name

Coffe Lake-H

Rev

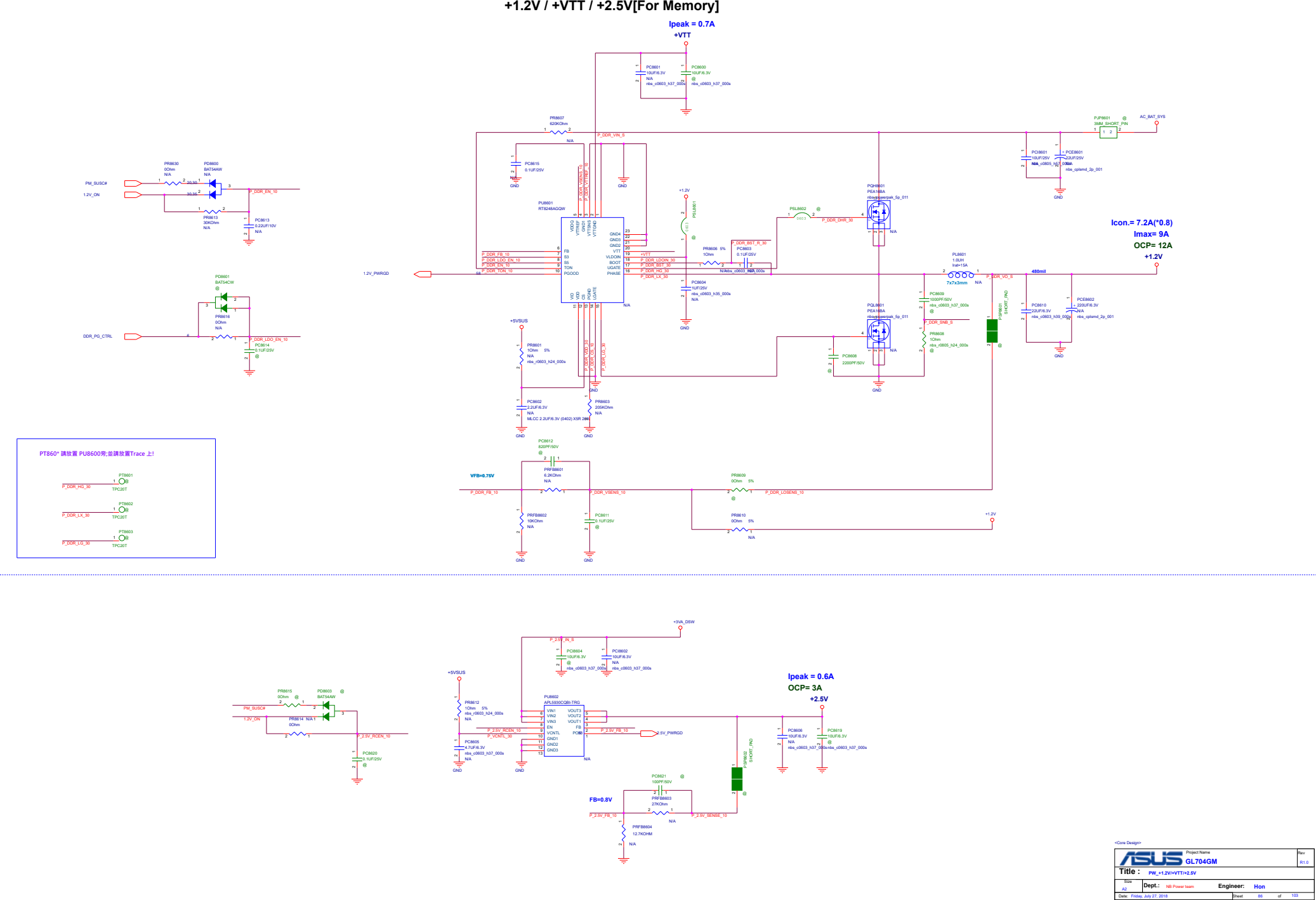
R1.0

Title : PW_

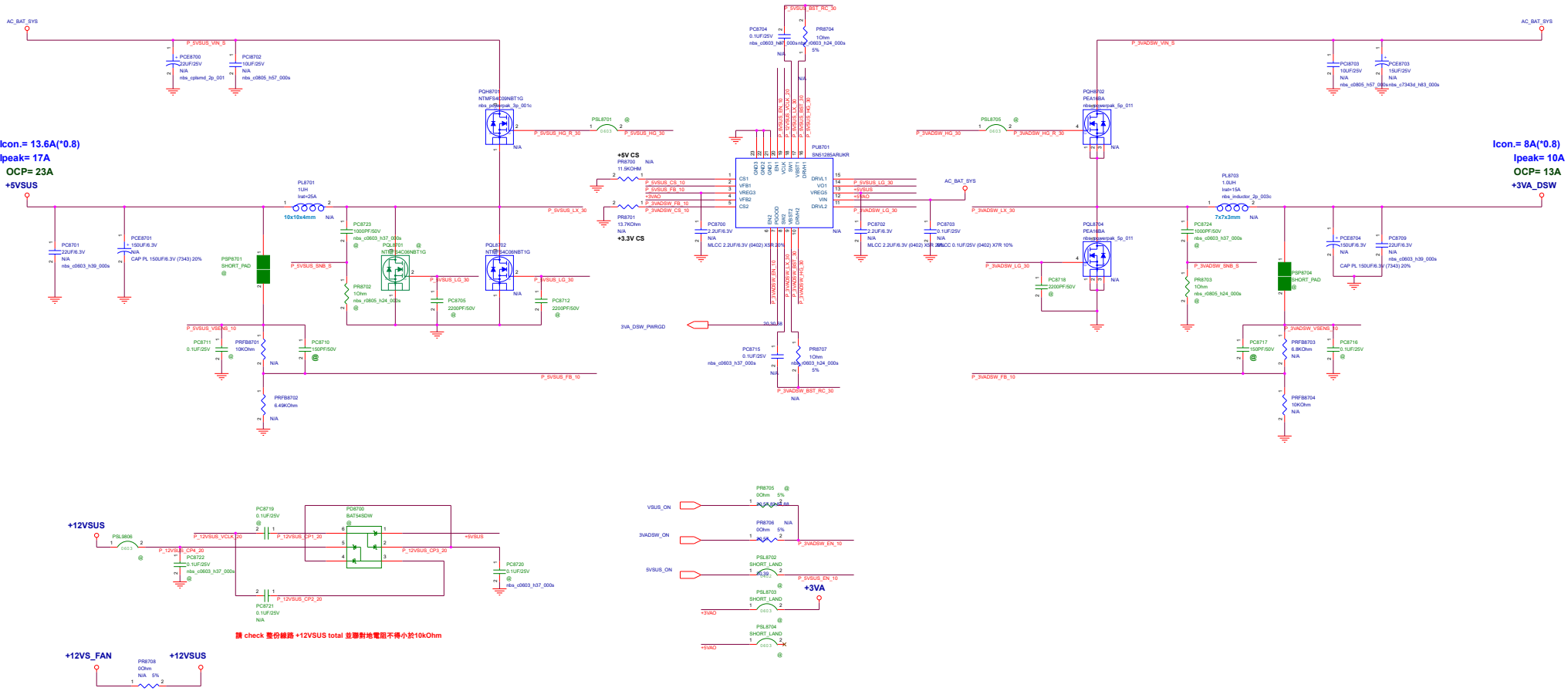
Size	Dept.:	Engineer:
A3	NB Power team	Benson

Date:	Sheet	of
Friday, July 27, 2018	85	103

+1.2V / +VTT / +2.5V[For Memory]



+3VA_DSW / +5VSUS [System Power]



請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

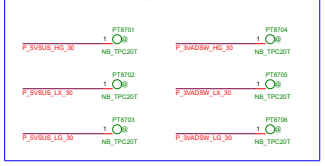
Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

PT870* 請放置 PU8700旁;並請放置Trace 上!

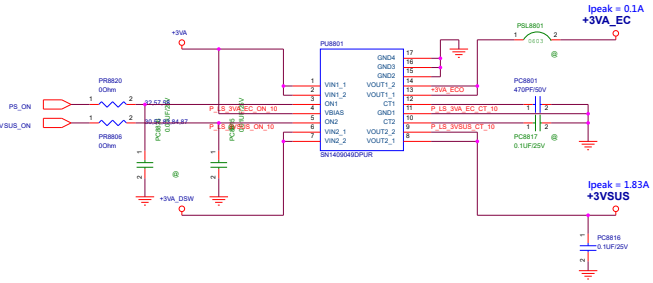


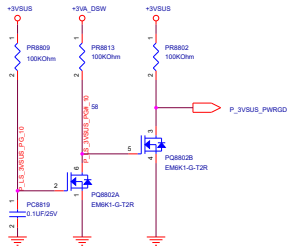
<variant_name>

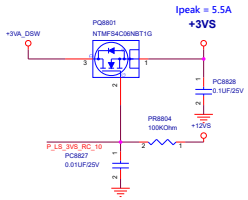
ASUS	Project Name: GL704GM	Rev: R1.0
Title : PW_+3VA_DSW/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Hon
Date: Friday, July 27, 2018	Sheet: 87 of 103	

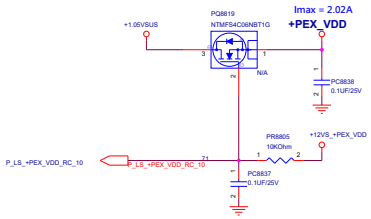
Load Switch

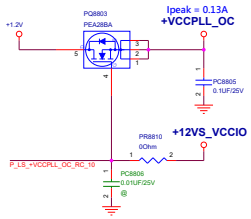
Main Board

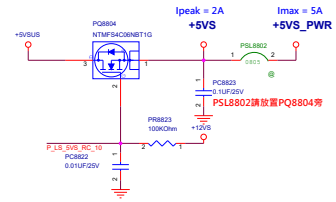


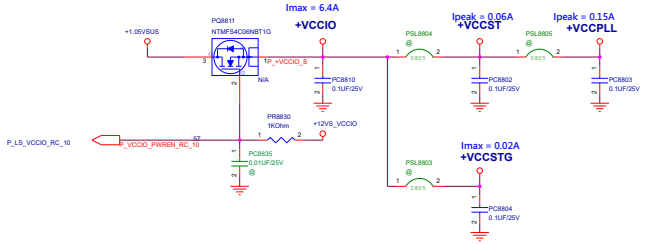


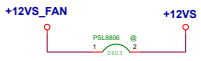


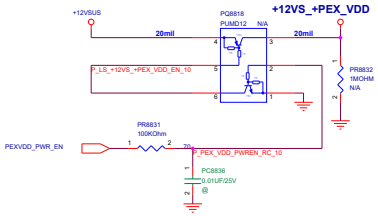


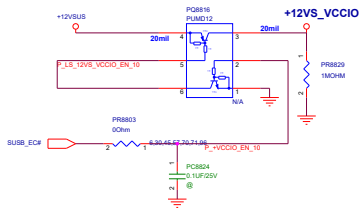


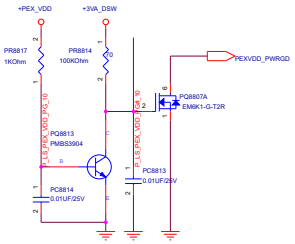


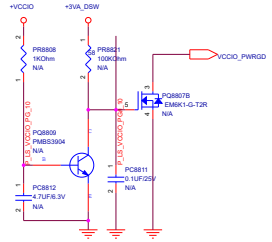




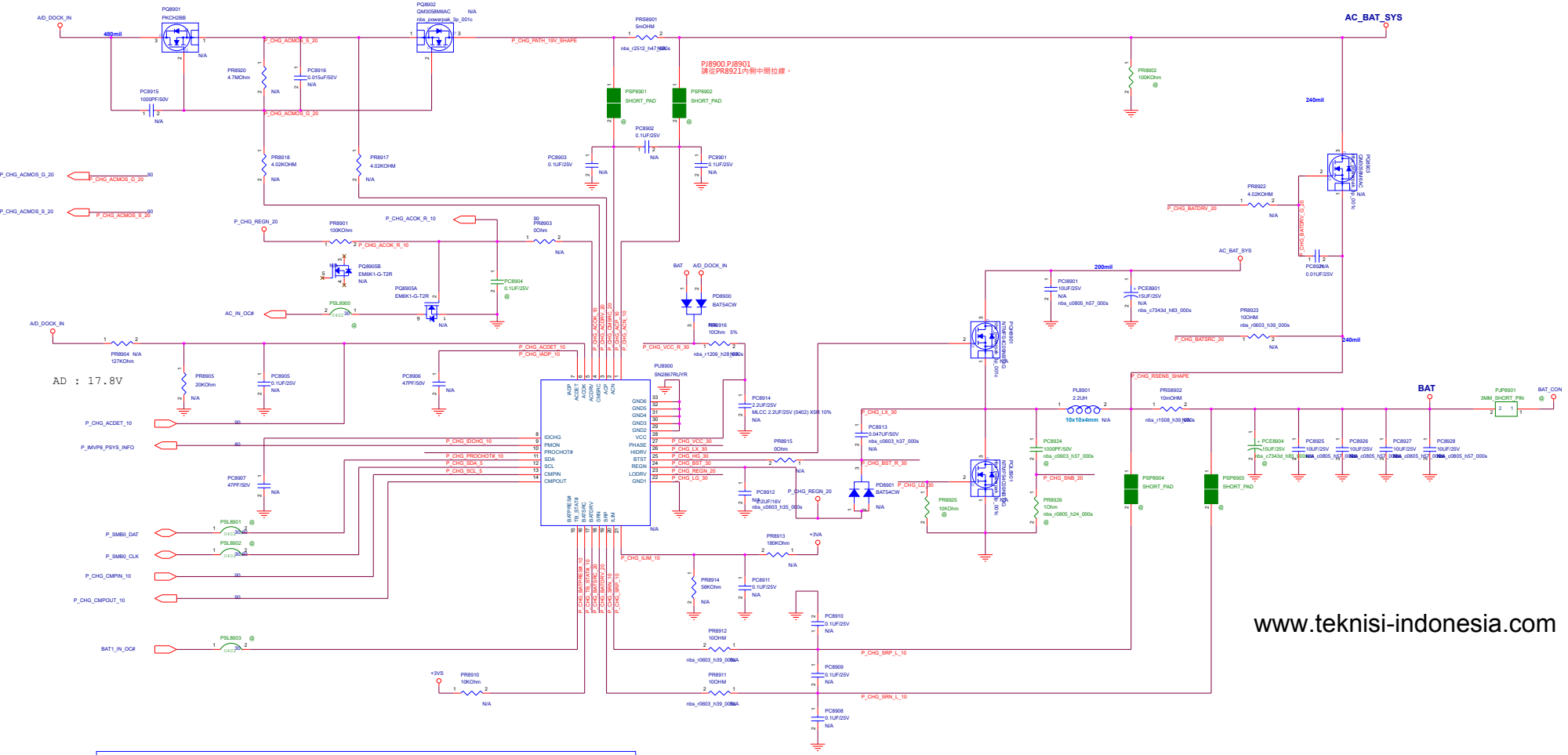




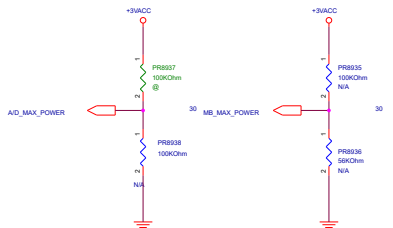




ASUS	Project Name: GL704GM		Rev: R1.0
Title : PW_LOAD SWITCH			
Size: A2	Dept.: NB Power team	Engineer: Hon	
Date: Friday, July 27, 2018	Sheet: 88	of: 103	



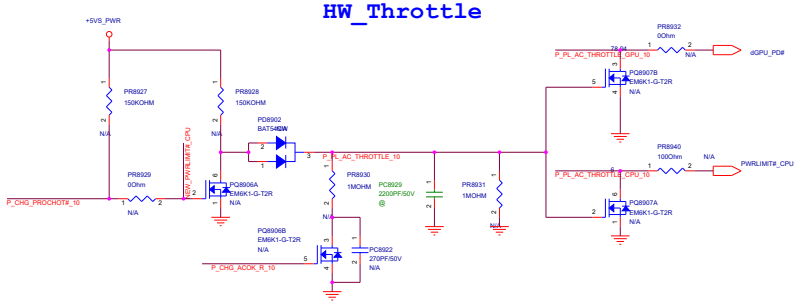
Adaptor select



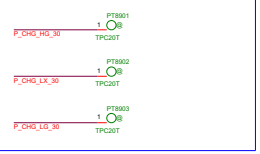
Adaptor select		N Series	G Series
PR8921		10m	5m
PR8936			
14K	0.4V	30W	120W
31.6K	0.8V	40W	150W
56K	1.2V	45W	180W
93.1K	1.6V	65W	230W
150K	2.0V	75W	280W
270K	2.4V	90W	330W
560K	2.8V	120W	400W

HW_Throttle

dGPU_PD# ---> GPIO12



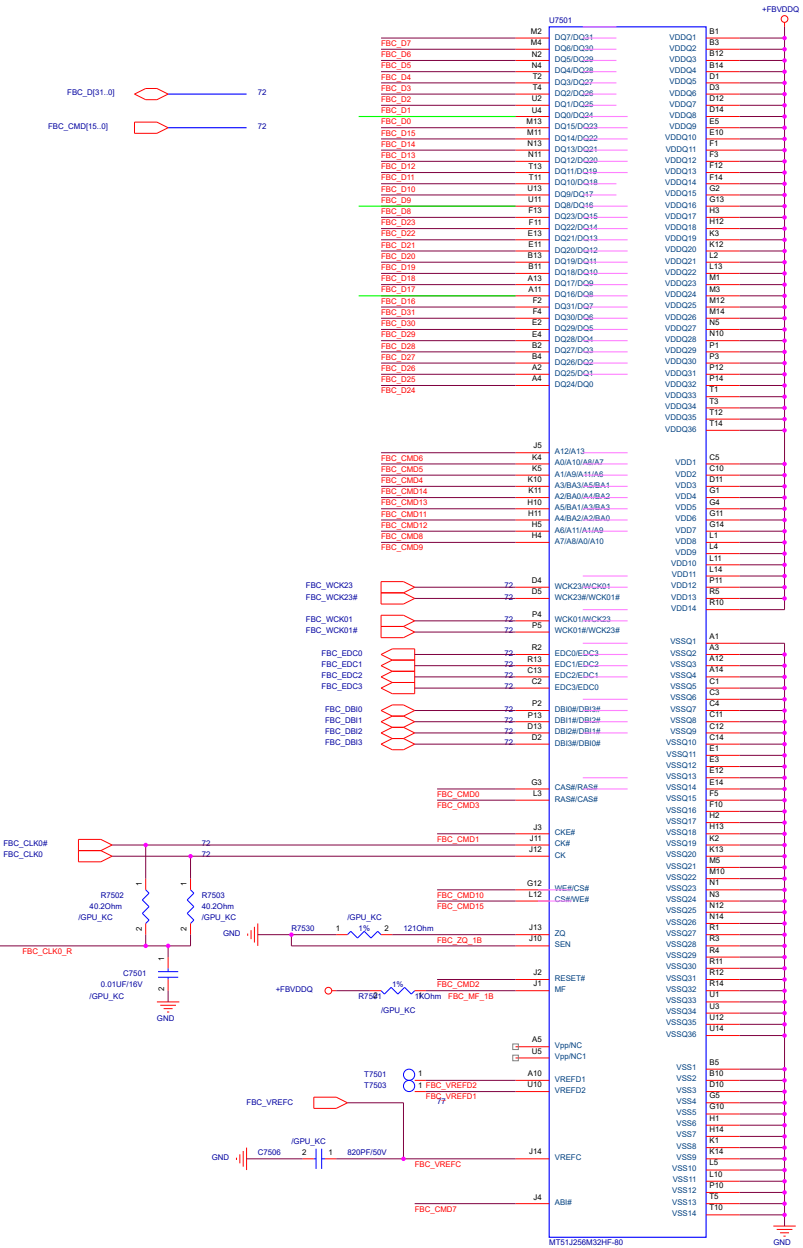
PT890* 請放置 PU8900旁;並請放置Trace 上!



Project Name: GL704GM			Rev: R1.0
Title: PW_CHARGER			
Size: A2	Dept.: NB Power Team	Engineer: Hon	
Date: Friday, July 27, 2018	Sheet 89 of 103		

FBC Partition Memory (1 of 2)

MF=1 Mirror

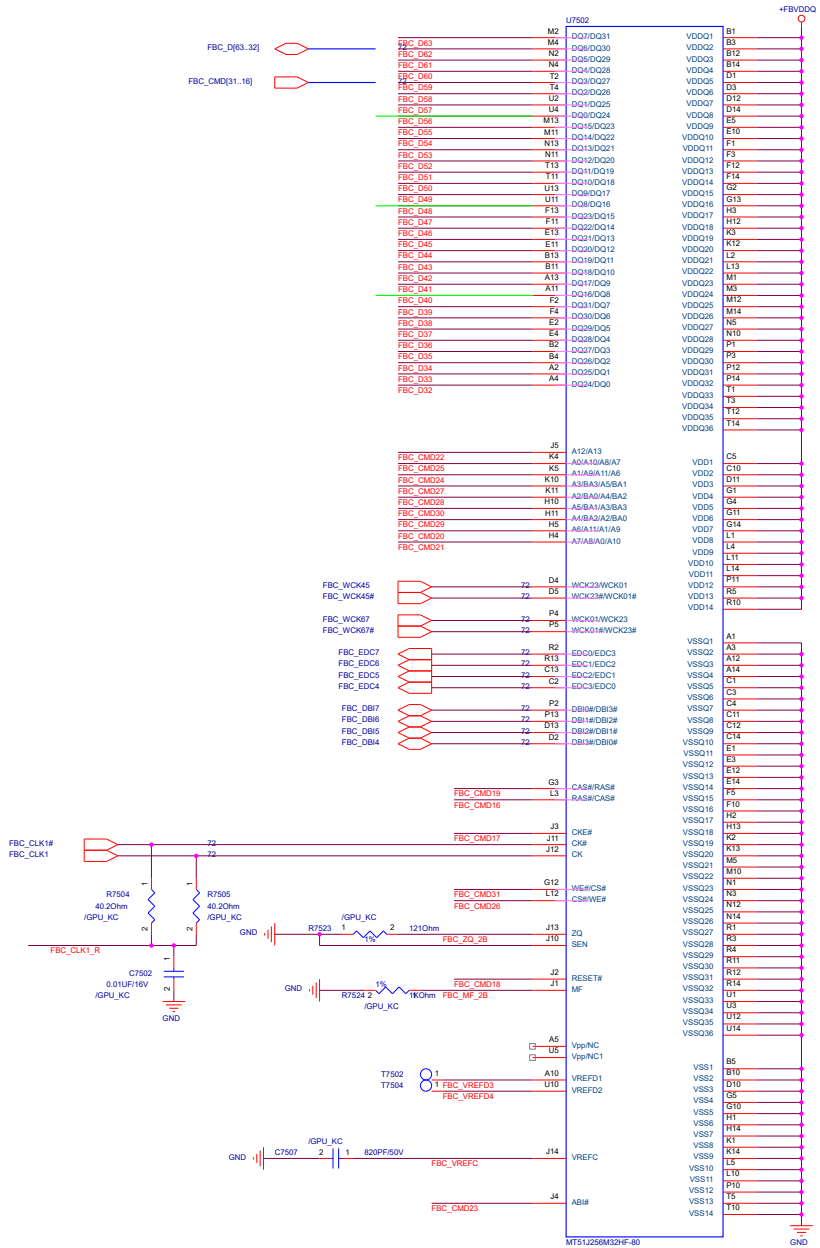


03008-00050500

/VRAM

FBC Partition Memory (2 of 2)

MF=0 Normal



03008-00050500

/VRAM

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

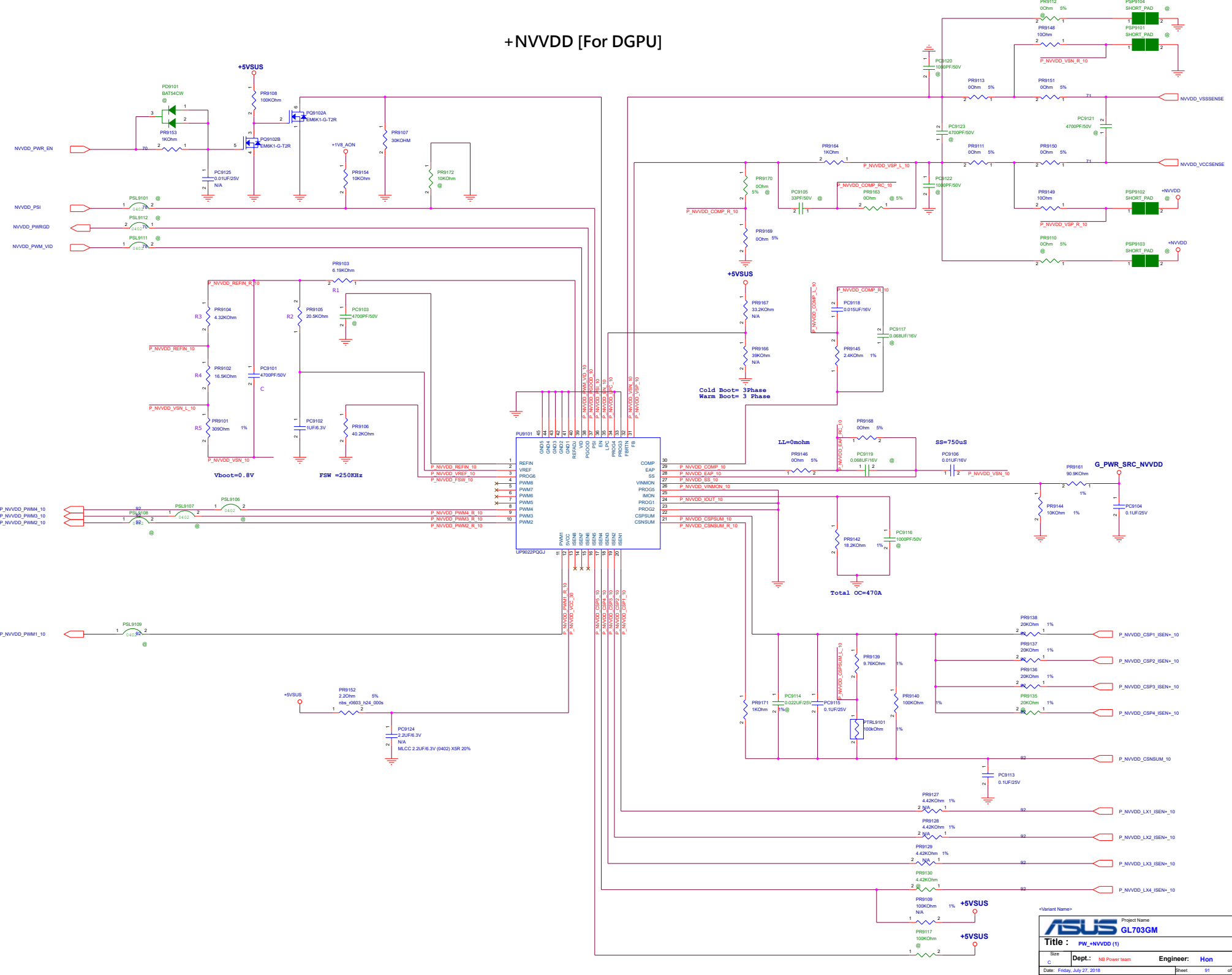
3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

Project Name	GL704GSM		Rev R1.1
Title :	VRAM-CHANNEL C		
Size C	Dept.: ASUSTeK COMPUTER INC.	Engineer:	Gaming RD4 EE1
Date: Friday, July 27, 2018		Sheet 75	of 103

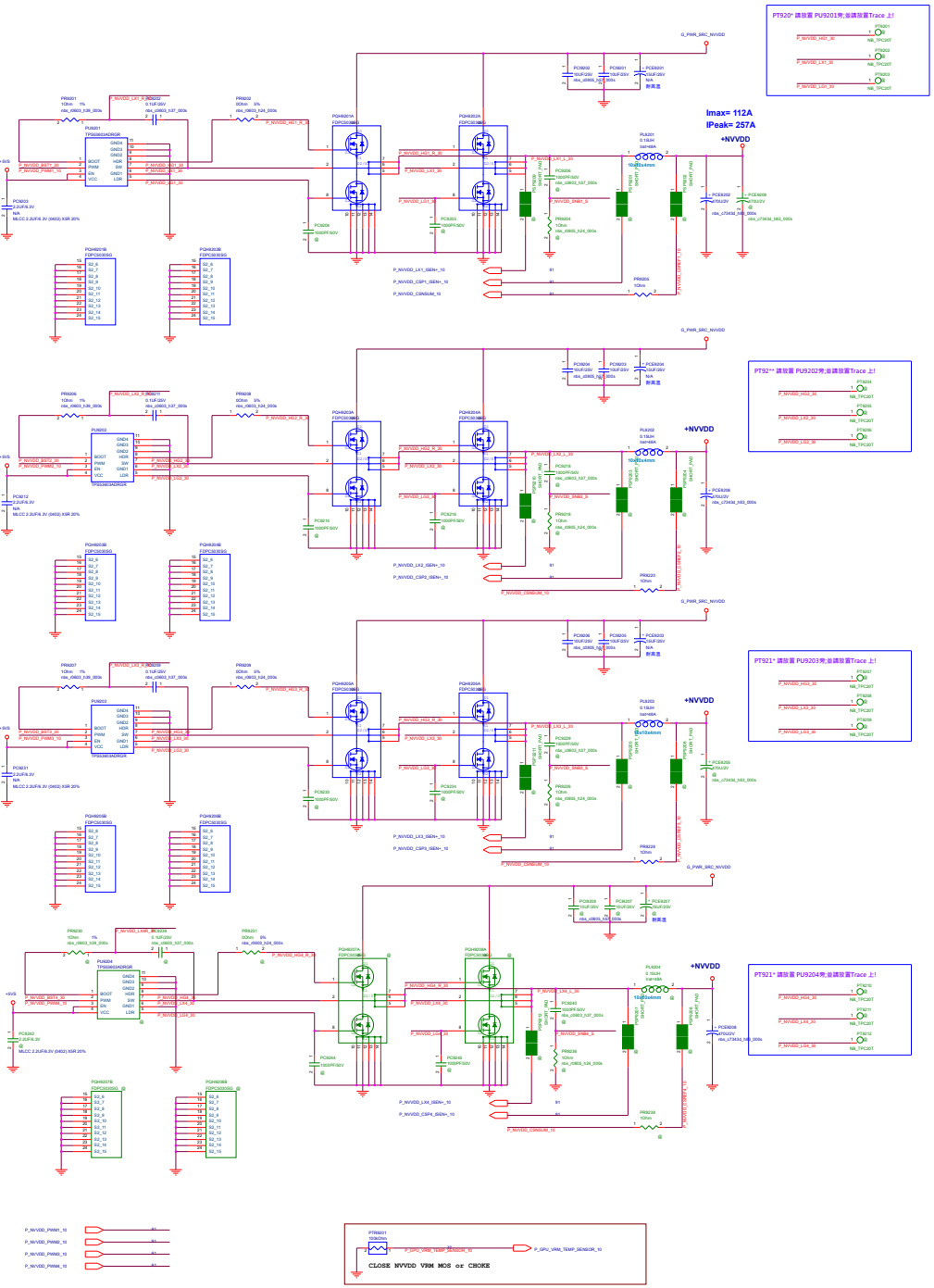
+NVVDD [For DGPU]



<Variant Name>

ASUS	Project Name: GL703GM	Rev: R1.0
Title : PW_+NVVDD (1)		
Size: C	Dept.: NB Power team	Engineer: Hon
Date: Friday, July 27, 2018	Sheet 91 of 102	

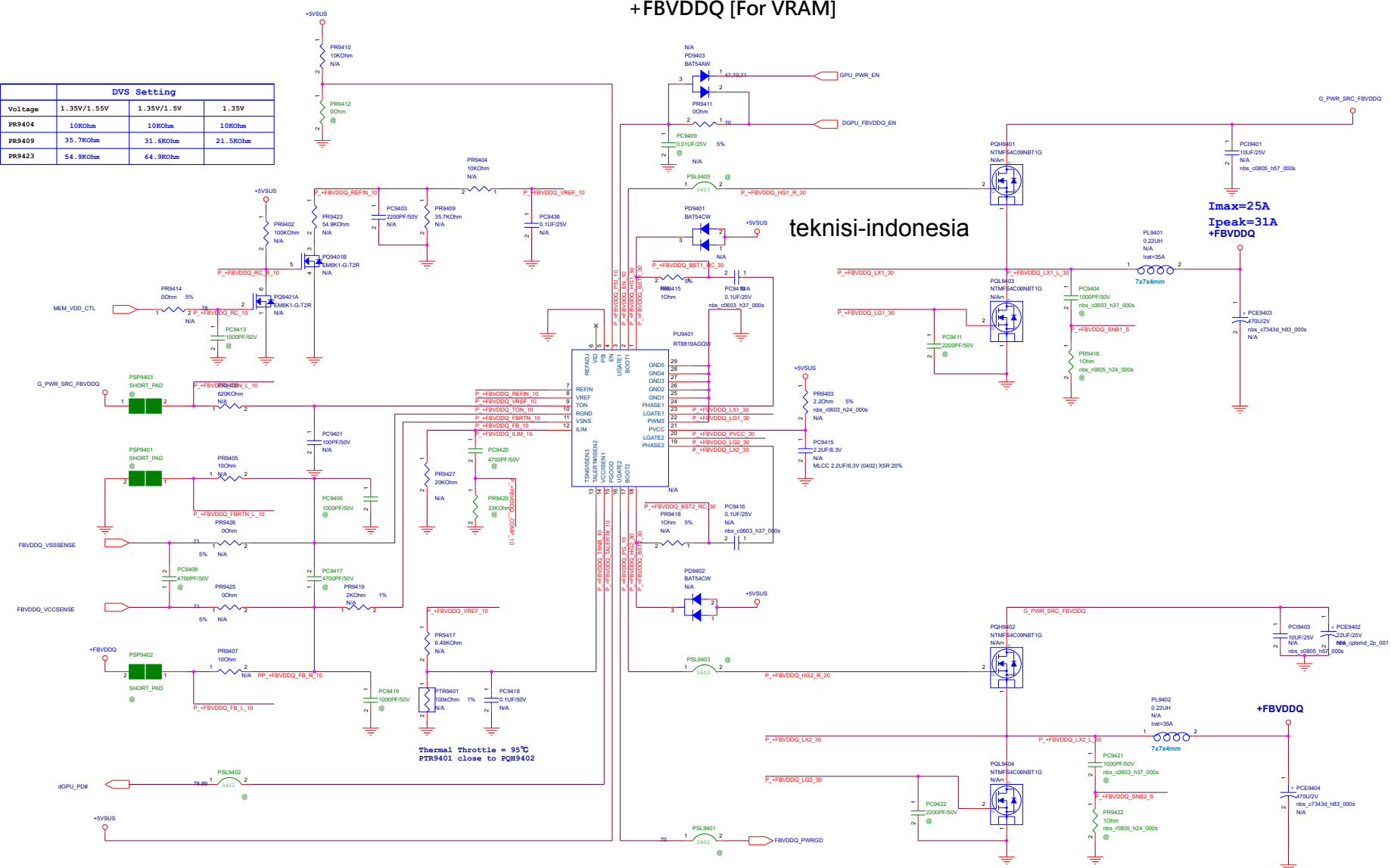
+NVVDD [For DGPU]



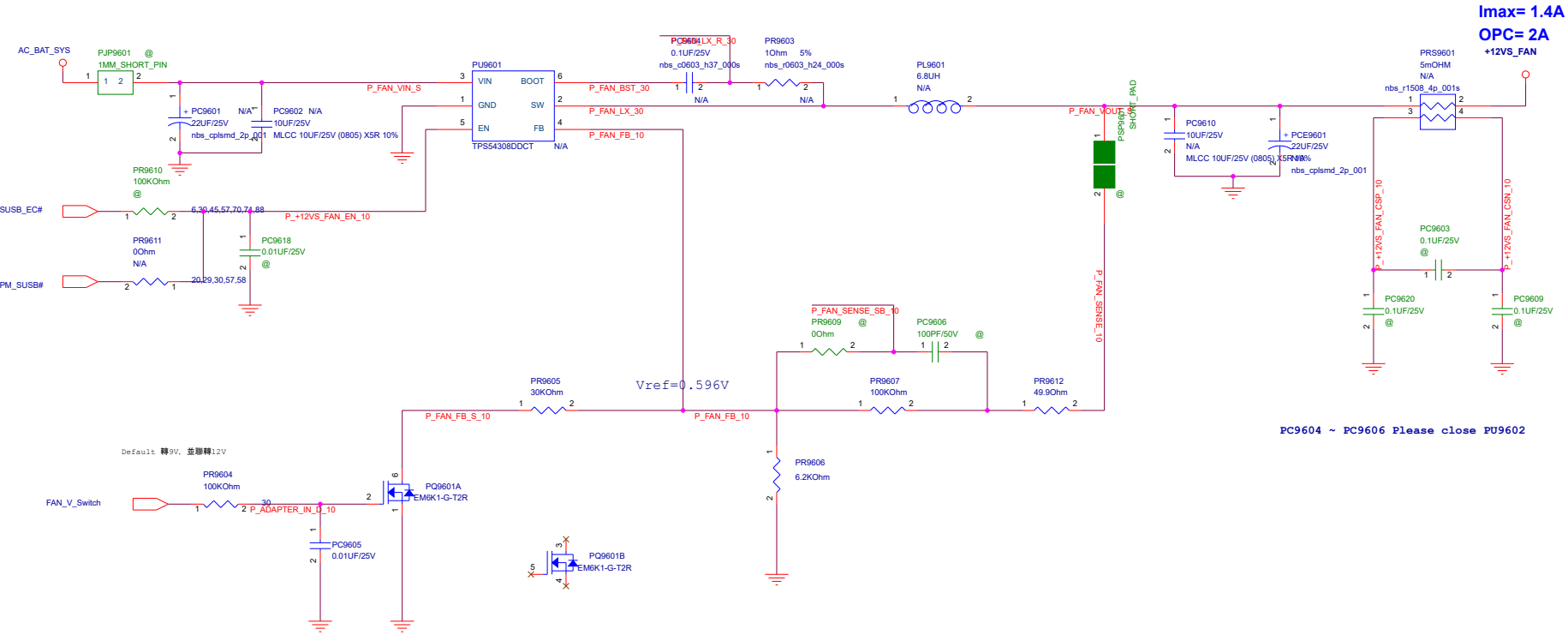
ASUS	Project Name: GL703GS		Rev: 1.0
Title : PW_+NVVDD (2)			
Size: A1	Dept.: NB Power team	Engineer: Hon	
Date: Friday, July 27, 2018	Sheet: 92 of 162		

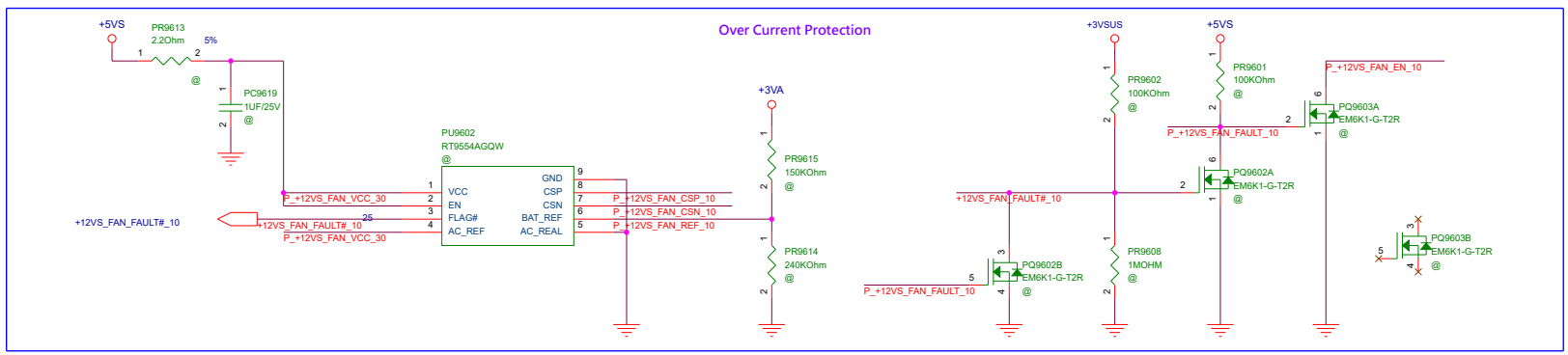
+FBVDDQ [For VRAM]

DVS Setting			
Voltage	1.35V/1.55V	1.35V/1.5V	1.35V
PR9404	10KOhm	10KOhm	10KOhm
PR9409	35.7KOhm	31.6KOhm	21.5KOhm
PR9423	54.9KOhm	64.9KOhm	



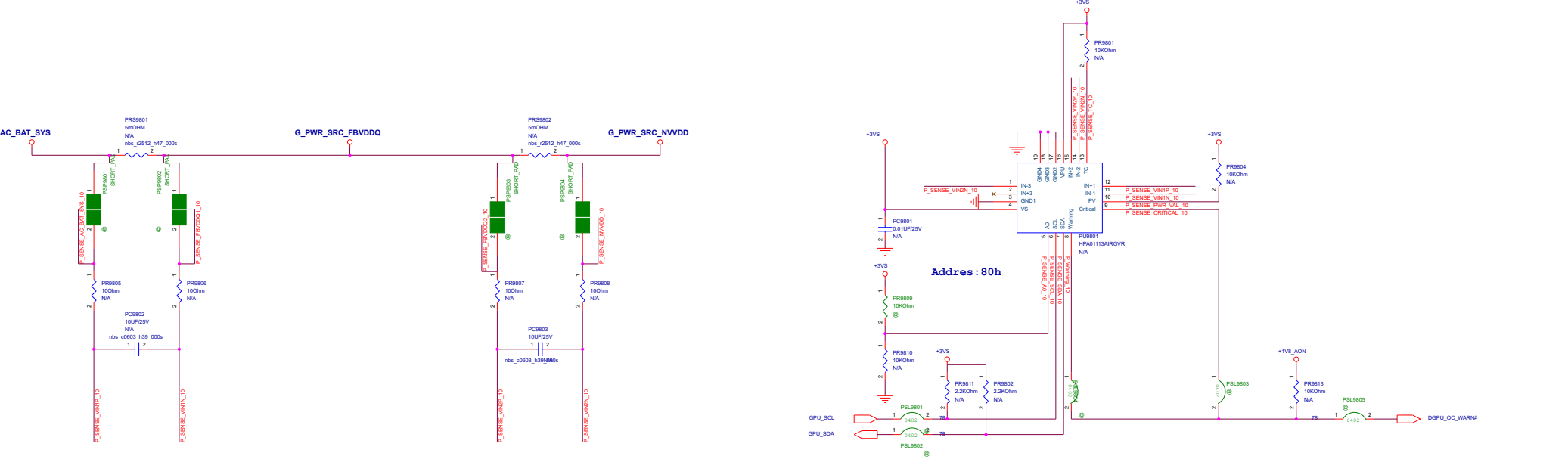
+12VS_FAN [For FAN]





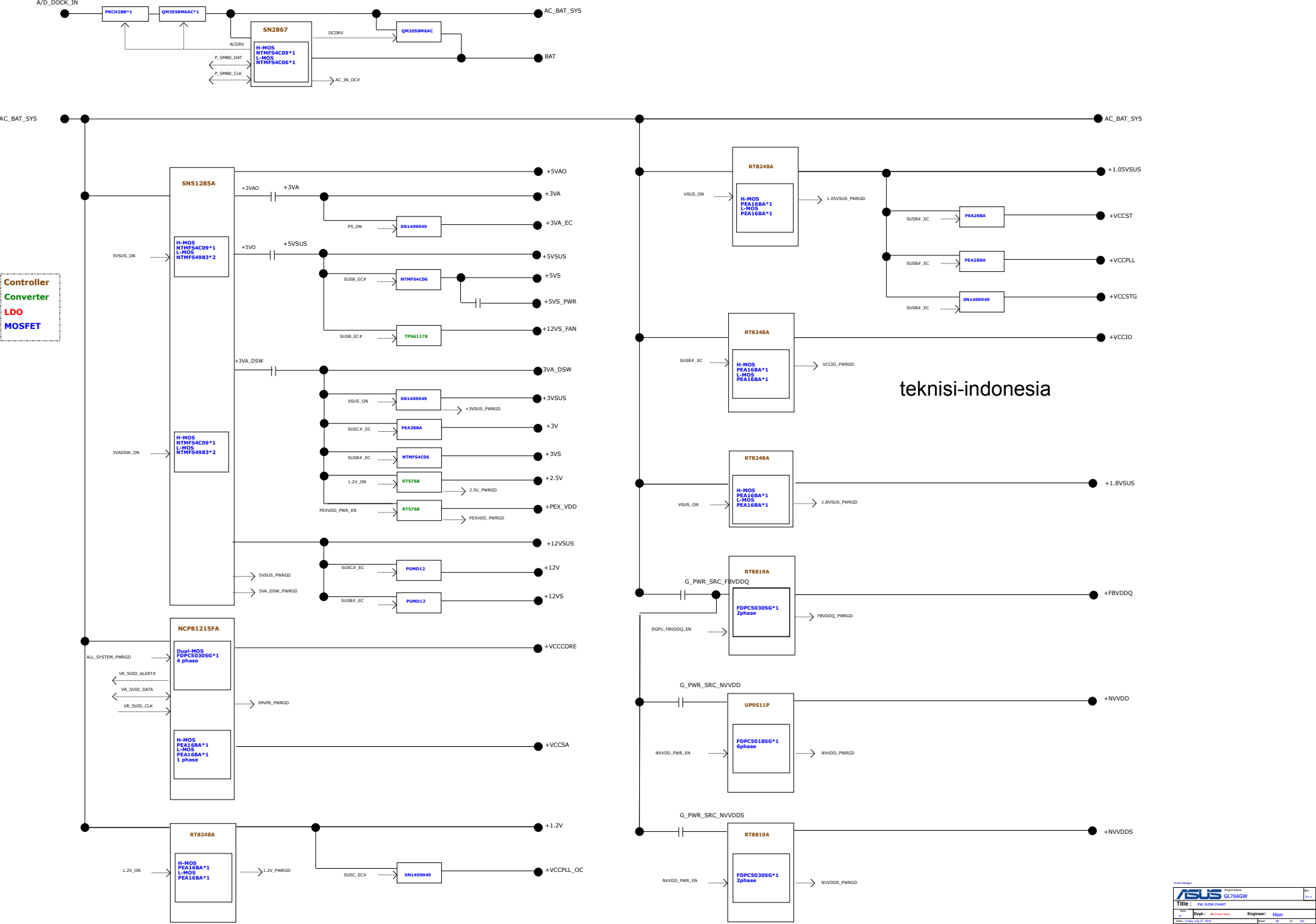
<Variant Name>

ASUS	Project Name: GL704GS	Rev: R1.0
Title : PW_+12VS_FAN		
Size: A3	Dept.: NB Power team	Engineer: Hon
Date: Friday, July 27, 2018	Sheet 96 of 103	



<Variant Name>

ASUS	Project Name: GL704GS	Rev: R1.0
Title : PW_IPC		
Size: Custom	Dept.: Power Team	Engineer: Hon
Date: Friday, July 27, 2018	Sheet 98 of 103	

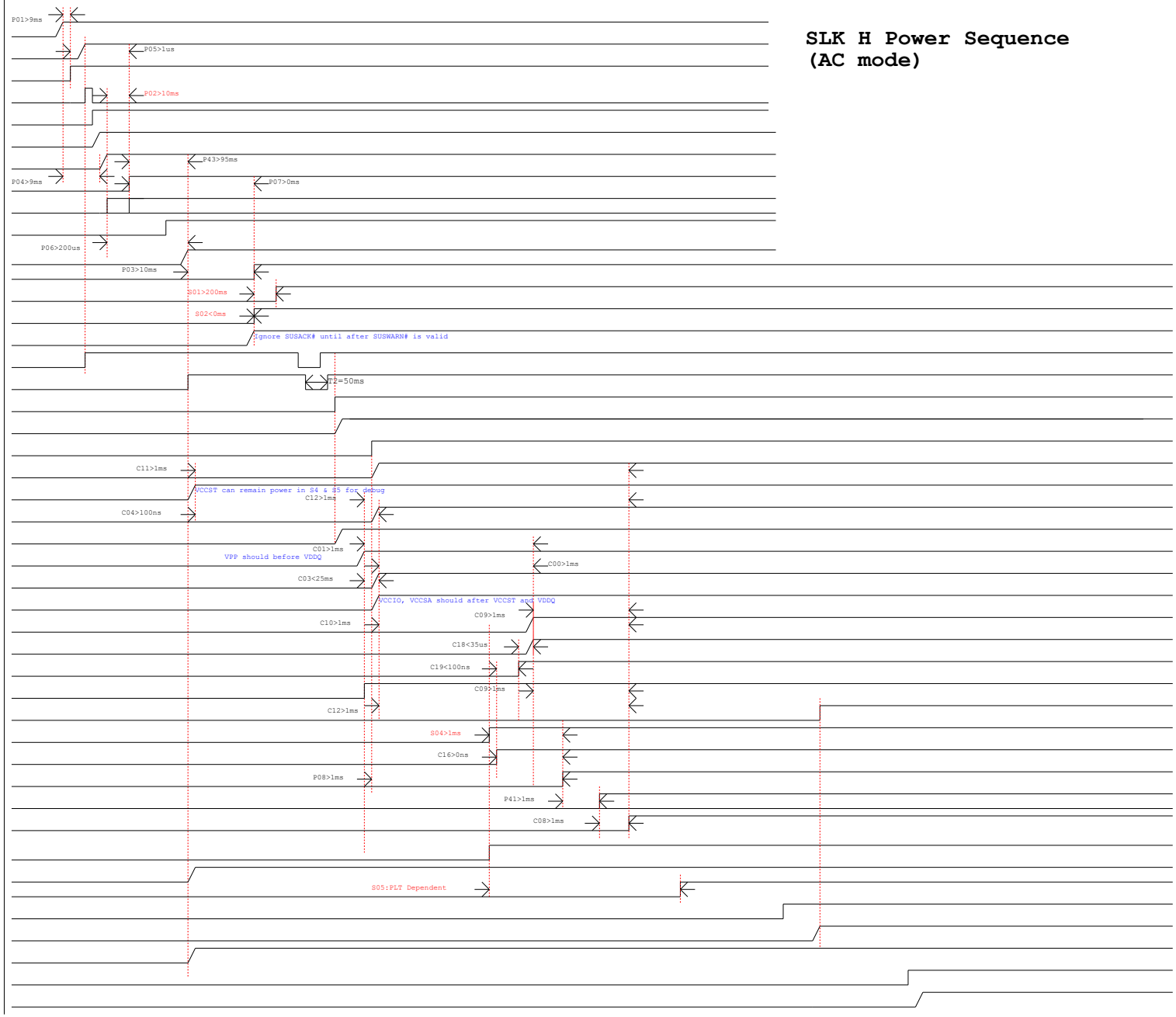

A/D_DOCK_IN
PKCH2BB*1
QM30S8M6AC*1
SN2867
H-MOS NTMFS4C09*1 L-MOS NTMFS4C06*1
ACDRV
DCDRV
P_SMB0_DAT
P_SMB0_CLK
AC_IN_OC#
QM30S8M6AC
AC_BAT_SYS
BAT
Controller
Converter
LDO
MOSFET
SN51285A
H-MOS NTMFS4C09*1 L-MOS NTMFS4983*2
5VSUS_ON
3VADSW_ON
+3VAO
+3VA
+5VO
+5VSUS
+3VA_DSW
PS_ON
SUSB_EC#
SUSC#_EC
SUSB#_EC
1.2V_ON
PEXVDD_PWR_EN
VSUS_ON
5VSUS_PWRGD
3VA_DSW_PWRGD
+5VAO
+3VA_EC
+5VS
+5VS_PWR
+12VS_FAN
3VA_DSW
+3VSUS
+3V
+3VS
+2.5V
+PEX_VDD
+12VSUS
+12V
+12VS
SN1409049
NTMFS4C06
TPS61178
RT5768
PUMD12
2.5V_PWRGD
PEXVDD_PWRGD
+3VSUS_PWRGD
PEA288A
NCP81215FA
Dual-MOS FDPC5030SG*1 4 phase
H-MOS PEA168A*1 L-MOS PEA168A*1 1 phase
ALL_SYSTEM_PWRGD
VR_SVID_ALERT#
VR_SVID_DATA
VR_SVID_CLK
IMVP8_PWRGD
+VCCCORE
+VCCSA
RT8248A
H-MOS PEA168A*1 L-MOS PEA168A*1
1.2V_PWRGD
SUSC_EC#
+1.2V
+VCCPLL_OC
AC_BAT_SYS
RT8248A
H-MOS PEA168A*1 L-MOS PEA168A*1
VSUS_ON
1.05VSUS_PWRGD
SUSB#_EC
+1.05VSUS
+VCCST
+VCCPLL
+VCCSTG
SN1409049
PEA288A
RT8248A
H-MOS PEA168A*1 L-MOS PEA168A*1
SUSB#_EC
VCCIO_PWRGD
+VCCIO
RT8248A
H-MOS PEA168A*1 L-MOS PEA168A*1
VSUS_ON
1.8VSUS_PWRGD
+1.8VSUS
RT8819A
FDPC5030SG*1 2phase
G_PWR_SRC_FBVDDQ
DGPU_FBVDDQ_EN
FBVDDQ_PWRGD
+FBVDDQ
G_PWR_SRC_NVVDD
UP9511P
FDPC5018SG*1 6phase
NVVDD_PWR_EN
NVVDD_PWRGD
+NVVDD
G_PWR_SRC_NVVDDS
RT8819A
FDPC5030SG*1 2phase
NVVDD_PWR_EN
NVVDDS_PWRGD
+NVVDDS
teknisi-indonesia
ASUS
Project Name: GL704GW
Rev: 0G.2
Title : PW_FLOW CHART
Dept.: NB Power team
Engineer: Hon
Date: Friday, July 07, 2016
Sheet 90 of 150

AC-IN Mode

SLK H Power Sequence (AC mode)

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST, VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



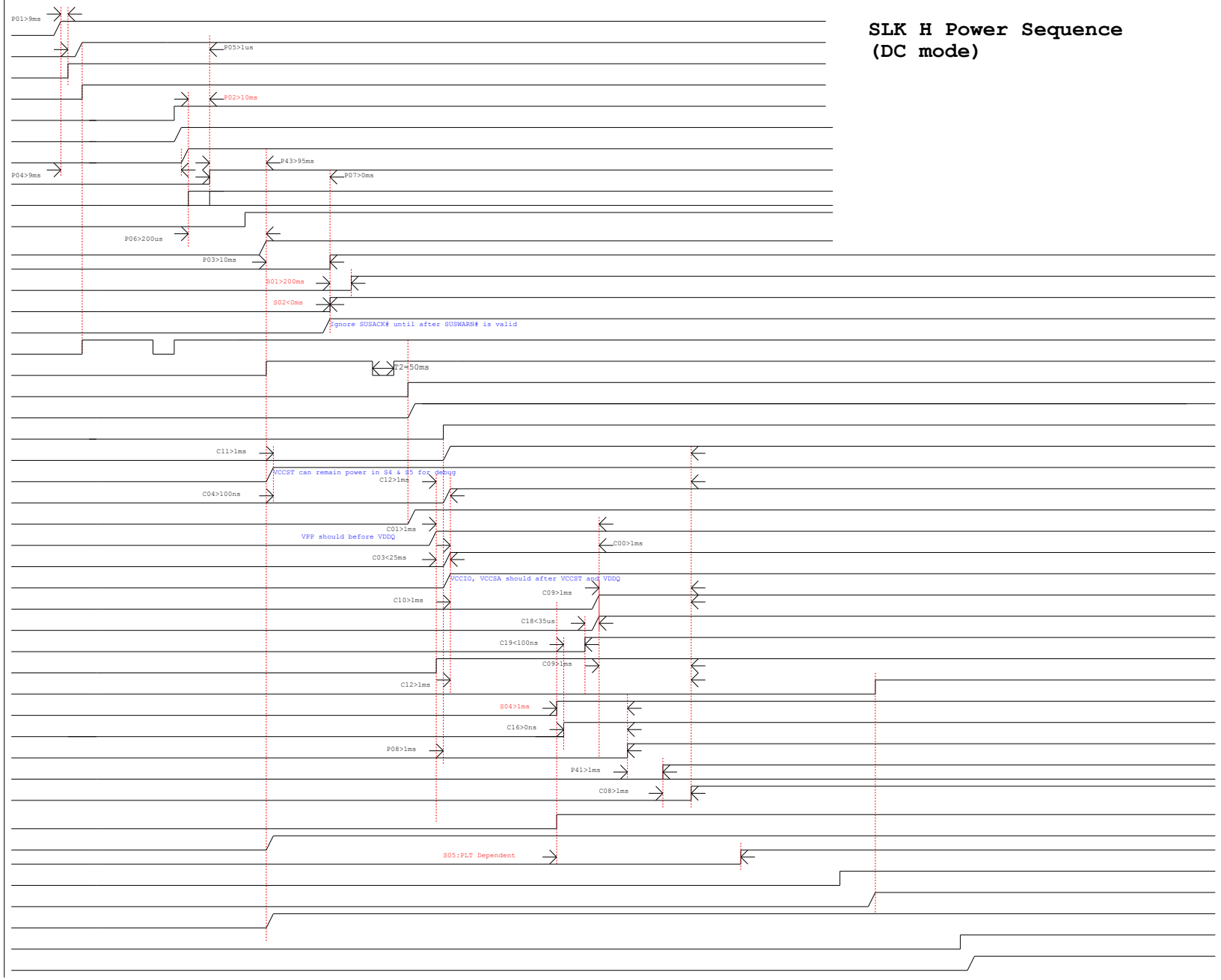
ASUS	Project Name: GL704GM		Rev: R1.1
Title : Power On Timing–AC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Friday, July 27, 2018	Sheet 100 of 103		

SLK H Power Sequence (DC mode)

DC-IN Mode

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT) +3VA_RTC
(AC_BAT_SYS) +3VA/+5VA
(+3VA_RTC) RTCRST# (PCH)
(Power) AC_IN_OC# (EC)
(EC) PS_ON (+3VA_EC)
(PS_ON) +3VA_EC (EC)
(3VADSW_ON) +3VA_DSW (3VA_DSW_PWRGD)
(EC) DPWROK_EC (PCH)
(+3VA_DSW) PM_BATLOW# (PCH)
(PCH) PM_SLP_SUS# (EC)
(VSUS_ON) +1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
(EC) PM_RSMRST#_PCH (PCH)
(PCH) SUSWARN# (EC)
(EC) ME_AC_PRESENT_PCH (PCH)
(EC) PCH_SUSACK# (PCH)
(PWR Switch) PWR_SW# (EC)
(EC) PM_PWRBTN# (PCH)
(EC) SUSC_EC# (Power)
(SUSC_EC#) +12V/+5V/+3V
(EC) SUSB_EC# (Power)
(SUSB_EC#) +12VS/+5VS/+3VS
(VSUS_ON) +1.0V_VCCST,VCCPLL (VCCST_PWRGD)
(+VCCIO) +VCCSTG
(1.2V_ON) +2.5V (2.5V_PWRGD)
(1.2V_ON) +VDDQ_CPU (1.2V_PWRGD)
(+12VS) +VCCPLL_OC
(SUSB_EC#) +VCCIO (VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD) +VCCSA (IMVP8_PWRGD)
(DDR_VTT_CTRL) +0.6V
(CPU) DDR_VTT_CTRL (Power)
(Power) 1.2V_PWRGD (AND)
(Power) IMVP8_PWRGD
(AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
(EC) PM_PWROK_PCH (PCH)
(PCH) CLK_PCH_BCLK (CPU)
(PCH) H_CPUPWRGD (CPU)
(ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
(CPU) P_SVID_DATA_X2 (Power)
(EC) PM_SYSPWROK_PCH (PCH)
(PCH) PLT_RST# (CPU/EC/Device)
(P_IMVP8_DRVON) +VCCCORE (IMVP8_PWRGD)
(CPU) H_THERMTRIP# (PCH)
(PCH) DDR4_DRAMRST# (Memory)
+VCCGT



ASUS	Project Name: GL704GM		Rev: R1.1
Title : Power On Timing-DC mode			
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Friday, July 27, 2018	Sheet 101 of 103		

Project Name

GL704GM

Rev

R1.1

Title : *****

Size	Dept.:	Engineer:
B	ASUSTeK COMPUTER INC.	NB1 RD2 EE1

Date:	Sheet	of
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Rev	Date	Description
R1.0	2017/09/27	Page12, TypeC U2_1/2 connect to PCH U2_13/14 Page21: GL704: remove Tobi eye tracking Page21: GL704: remove Xbox WLAN Page03,70, pcie0 changes to x16 Page41, remove lnk M.2 SSD Page52,55, update page52, 55 USB port update power schematic 20171016 CLK_REQ#_8 pull high to +3VS for intel SSD Page16,17 remove DIMM connector A1/B1 Page11,12,13 remove TBT alpine-ridge schematic Page40. remove NGFF2 connector Page52, remove U3 rerdriver Page48, HDMI retimer changes to PERICOM PI3HDX2711 Page47, add DP rerdriver in schematic Page79, remove DP output for TBT update Audio schematic Page11,12,13 remove TBT alpine-ridge schematic Page40. remove NGFF2 connector Page52, remove U3 rerdriver Page48, HDMI retimer changes to PERICOM PI3HDX2711 Page47, add DP rerdriver in schematic Page79, remove DP output for TBT update Audio schematic Page42, Card reader schematic Page43, Lan transformer schematic add NGFF2 SSD back in schematic update Page72/73/74/75/76, GD3R5 schematic page52, reserve U3 Gen1 rerdriver for SXF modify page42, remove GL3215 schematic, connect CR from PCH combine NVDD/NVDD5 update audio schematic D4501 VIN改+3VSUS SDcard power 改+3VSUS update page11/Page52 rerdriver sch update page35 KSBL/FIBER/Eagle eye MOSFET update power schematic1112 update Page72/74/52/75, ECNF update audio schematic 11141400 Page26, reserve 1.8VSUS power for GPDA group Page26, reserve 1.8VSUS power for SPIROM Page31, reserve 1.8VSUS power for EC Page20/22, update schematic for eSPI Page71/70, NVDD/NVDD5 merge Page48, remove 1.2V LDO Page35, 0P2GM5497HG08CK# reserve Level-shift for eSPI Q3601 改为SI2302 +1.8V_AON 增加 R3601 470ohm for +1.8VSUS +3V_AON 增加 R3602 10K ohm for +3VSUS Q3603,Q7109,Q7701,CT702,Q7801,Q7803 改用 070005607011 Q3711,Q3791,Q3792 改用 070005407011 C3905 and C3915 改用 1U0J35222625320 C3919 and C3928 22uF 改用1U0J35210612320 Page51, update HDD connector Page12/52/55, ECNF update temp_T_001582 update power schematic 1122, page 30 GPA6 add net FAN_V_switch C4504 改用1U0J35210612320 C3621 and C3622 改用 1U0J35222626320 C3001,C3002,C3003,C3004,C3005,C3006,C3007,C3008, D2001,D2004,D2005,D3001,D3002,D3301,D7001,D7801 改用 070004069020 C0602,C1804,C1805,C1808,C1809,C2006,C2605,C2614,C2617,C2619,C2624,C2627,C3001,C3002, C3004,C3005,C3007,C3008,C3051,C3052,C3053,C3054,C4207 改用 1U0J32201411390 update page24 PCH sch update Page36 AUD sch Page71, update +1.8V_AON/+1.8V_Main sch Page71, EC_VSP1 connects to RUN power +3V_+1.8V_SP1 Page79, remove IPPAR_PLL power Page71, remove Q7102'discharge circuit Page71, remove +3VS_RV power Page78, I2C pull up via 2.2k to +1V8_MAIN Page79, HDMI pull high to +1V8_MAIN update Page38 power protect sch update power sche 1124 Page47, DP 1.3/1.4 rerdriver sch Page48, EMI chock option set @ Page42, CR signale 10ohm change to shortland, C4201~C4206 option default set @ Page46, delete 50hm on PCIE RX route, reserve shortland on CLK lane Page4, U0601 change PN to 08004-00630000 Page52, delete 50hm on J5202 RX Page50, delete 50hm on J5501/J5502 RX Page26, VCCSPI connect to 1.8VSUS,reserve 3VSUS power Page24, GPP_F9 pull up to 1.8VSUS via 10ohm Page24, JDEB004401 vertically rotate/reverserve eSPI IF Page41, eSPI debug card Page36, delete connector PWR_LED & EMI CAP Page41, add M.2 SSD Page11, add SW1025 power switch Page52, J5202 add its own current protect/ESD component in sch for WE design Page78, I2C sch pull-up change to +1.8_AON update power sch 1128, 7-phase NVDD Page12, Unmount R1219, Mount R1215,Unmount C1206 Page22, delete u-used CLKREQ# pull-up Resistors Page27/70, add CT003 and gate in sch for NV GC off Page31, update LID GBE to Touchpad sch Page24, pin AL37 connects to VSS, follow G703G1 schematic1110 Page25/47/78, add HPD_Event to PCH for GC-off Page52, Q3506 change to 1k+200mA MOS Page43/44, Debug port reserve 0ohm for eSPI update power schematic1201 Page39, update Mute control circuit Page36/37, delete 0ohm on MIC_SLEEVE/RING/L/R Page71, delete Q7102, discharge circuit for +3V Page71, add R7115/CLK3 pull high via 4.7kohm to +3VA_EC Page39, SMB3_2nd_DA pull high via 4.7kohm to +1.8V_3.3V_IOVDD Page71, reserve ELC1010/EL7102 for measurement Page78, delete R7654/R7906 Page78/79, IPP configure follow GL504, IPP_IOVDD1/2/3/4 connect to +PEX_VDD_IPP_IOVDD Page36, CAP_LED net connects to EC GPP_F5 Page36, EC GPP_F0 CAP_LED keep floating Page35, Q3506 Change'MOS back to 1A+100mA Page36-39, update Audio sch 1201 Page46, Net name swap NGFF1_RXN0/NGFF1_RXN0 NGFF2_RXP0/NGFF2_RXN0 Page71, delete R7102 for GL704 VCORA component, 7*7*2.4 Page12/52/55, ECNF update, temp_BOM_000008 Page14/15, DIMM connector update Page36-39, update Audio sch 1207 Page12/52/55, USB 4 TypeC connector update PN Page42, update CR connector PN Page50, delete 680P CAP Page36, add Q3603 level-shifter, R3014 for GPA7 pull high update Audio sch 1208, mount R3939 Page71, delete SLC10L, delete J5103 connector, ADD connector/sch follow GL703VE update CR/EMC/miniLDP/NGFF SSD/WLAN/FAN/DC-in connector PN Page78, The option of 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Transformer follow GL50XG Page51, D5302/T5307/T5350/C7304/D7301/C7303/C7302/R7314/C7301/C7402/C7401/C7403/R7411/C7406/R7409/ C7501/R7501/R7524/C7502/C7506/C7507/R7602/R7601/C7601/C7604/C7605/C7602 change footprint to nbs R2D component PN change from 0702801010 to 07024-01170000(nbs footprint) 20171220 Page53, R3510 change component size from 0603 to 0402 R7003/D7001/D7003/C7502/C7503/D3202/C3204/C2401/D2001/D2004/D2005/ESPI_SWO4301/C3519/C3516/D3507/R3545/ C3523/R3527/R3546/R3510/R3513/C3521/R3522/R3502/C3527/R3517 change footprint from hb to nbs update power schematic1220, hb footprint change to nbs 20171221 Page34, U3401/U3402 change PN to 0905I150501U Page37, Net name P_LE_PEX_VDD_AC_10 changes to P_PEX_VDD_PWRGD_AC_10 Page37/38, add D7003 for GC-off Page42, R2200 change PN to 07009-00111800, R2203 changes PN to 07009-00065700 Page42, add C2205 (Intel Document:Wireless_Technical_Advisory_GLK_ESD_mitigation_recommendation_V1.1) Page21, GPP_E8 reserve R2105 to pull high to +3VS Page25, delete T2510 Page25, delete R2506 for A/D_MAX_POWER Page71, R7006 change PN to 04024-01250000 Page31, add EL3101/EL3102/EL3103/EL3110/EL3120, reserve C3118/C3119 for I2C Page24, replace SLC413/SLC415 with R2440/R2438 respectively Page53, add R5330/R5331 2Ohm in sch by Intel's suggestion Page53, R5321 change option to N/A. by Intel's suggestion. Page53, delete R5323/R5324, The pull-up of CHV_BAT/CHV_EQI move to page 24. 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Page36,add R3401 Page25,add R2401 Page42, replace SL2216 with R2250 for BEAD colay 20180104 C5401 改为1U0J32210411070 C7010改为1U0J32210511320 C3613 改为1U0J32210411070 C3001,C3002,C3003,C3004,C3005,C3006,C1202,C1203,C1204 改为 1U0J31222425320 R3101,R3547,R3548 改为0GJ12300004010 R3631,R3933 改为0GJ21210304010 R4715,R4716 改为0GJ21210504031 R3712,R3713 改为0GJ21222004010 R3601 改为0GJ12330004031 R2009,R2056 改为0GJ21510504070 20180105 Page53, Q3507/Q3508/Q3509/Q3511/Q3512/Q3514/Q3515/Q3517/Q3521 change PN to 07005-00870100. delete Q3523 20180108 update Power schematic1D180, replace PCB6601/PCB7700/PCB7703/PCB8901 with 7343 CAP update Aud sch0108 Page27/55/48, EMI & ESD netswap by Layout suggestion 20180109 Page59, add U5901/U5902, C5914~C5929 by EMI request Page59, replace R5E3031 with 7343 CAP Page24, delete R2442 delete DC board page 20180110 update Audio sch0110 update power sch 0110 Page36, add 3V_LP_EC/3V_AUD_DVDD Page44, add DC BD back to sch Page45, add R4501~R4503 FAN MUT Page53, U5903~U5906 EMI Spring Page34, update U3401 LAN CGB PN Page56, update Light bar connector Page56, delete R5E3031 Page44, add SSD MUT Page47/25, update page54 ANT schematic Page45, add R4505 pin1connects to GND Page20, update ACZ_SDOUT sch update screw hole & PAD Page46, replace R7/R5/R2E700 change PN to RGSCAP 20180111 update power sch 0115 update screw hole & PAD delete C7808 & C7812 20180116 update power sch GL704GM 180115 Page03, connect +VCCST Page21, add C1001-C1022/C1080-C1089 for +VCCGT Cap Page21, EDP connect to CPU for optimaze Page23, AN6 connect to EDP_AUX_CPU, AN10 connect to DDI2_HDMI_HPD Page23, EDP connect to CPU for optimaze,add R4506 100k ohm, R4510 0 ohm, R4511 0 ohm option set @ Page39, EDP disconnect for optimaze Page39, delete R3944/C3504/R3517 Page71, delete R7102 Page78, on mount R7840, R7845 option set @ replace D5501 with D5502-05505 by EMI suggestion 20180117 update audio sch 0117 page6, add CD603 for EMI delete Page36, 07d_VAN=CHANNEL D Page71, delete R7204, Channel D, R7206, R7230, R7229, R7215, C7203 Page71, delete R7310,R77311,R77312 Page77, disconnect PBD_VREFC Page71, delete vram channel D Cap, C77193~C77221, C77225~C77253 Page57, add Q5706, R5763 option set @ for +VCCGT discharge	20180118 Page24, R2435 change from 20k ohm to 4.7kohm update power sch 0118 20180119 Page77, add T7707 Page65, R6519 disconnect to GND change sch 1002312224535320 to 11202-00089000 Page52, delete net R_5V_USB1_4G, T5206 net name change from USBA_USB20_OC to USBA_USB04_OC 20180122 Page58 update component name to C3402, C33 to C3403, C34 to C3404, C35 to C3405, C36 to C3406, C37 to C3407 Page65, update PAN NUT H6501-M6503 Page43, add USEB004303 Page60, R2600 change to P2603 Page78, R7800 option set to @/do-sync, R7818 option set to /non G-sync RAD304/RAD501/RAD503/L5301/01202 Netswap for Layout Page58, delete R5809 component name to JUSB004303 update power sch 0122 add C5930 & C4813 for EMI 20180123 update power sch 0123 Page37, delete 'reserve' VRAM channel D part Page Page37, reserve VRAM channel D part Page78, R7802 option set @ 20180124 J5602/J5603 change PN update H6516, delete D6502 page45, D4501 VIN connects to +3VSUS page45, add C4524 H6517/H6518 connect to GND DC update G3601 symbol & footprint 20180125 Page59, delete C5930, C5907 Page45, Delete H6512/H6514/H6505/H6513, replace with H6503/H6504 update U3301/U4805/U4701/U1101 symbol/part Page52, Delete USB CONN connector Page46, U6401/U6402 change name to J6401/J6402 update audio sch 01251030 20180126 Page45, update hole H6504/H6506/H6516/H6521 Page61, update J3105 to 12018-0021A2006 Page43, add eSPI board hole H4301/H4302 Page47, R4705 change from 10K ohm to 4.7K ohm Page37, R3708 change from 100K ohm to 2.2K ohm Page71, R7117 change from 100K ohm to 0 ohm, R7146 change from 0 ohm to 20k ohm, mount C71113 10F Page71, C7163 change from 0.01UF to 0.047UF, C7101 chane from 150PF to 470PF, Page25, R2D501 change from 2.2K ohm to 4.7K ohm Page48, R84804/R84805/R84806/R84807 option set @/EMI, LX4801/LX4802/LX4803/LX4804 option set /EMI Page48, C4812 option set N/A update power sch 0126 20180209 RL116/R1103/R1108/R1111/R5231/R5221 @~~N/A R4717/R4719 N/A~~@, R4718 @~~N/A C4844/C4846 0.01uF~~0.1uF 20180409 HW2 R1.1 20180409 Page45, LCD_VDD_EN_GPU to CPU,LCD_BL_PWM to CPU, LCD_BL_EN to CPU,add R4504 100k ohm to +3VS_LCD,add R4505@ Page45, set R4558 R4559 @, add R4512@ R4513,R4501,22'to Panel_ON Page21, LCD_VDD_EN_GPU to R4524.1, LCD_BL_PWM to EL4502.1, LCD_BL_EN_DG to U4502.1, R5 to Panel_ON Page71, disconnect LCD_VDD_EN_GPU,LCD_VDD_EN_CPU,LCD_BL_PWM_GPU,LCD_BL_EN_GPU Page78, delete LCD_PWAR_LOCK Q7801A R7848; disconnect LCD_VDD_GPU,LCD_BL_PWM_GPU Page78, delete R7844 R7845 set N/A update power sch 0408 Page24, SPI_D2 pull up to 1.8VSUS via 75kohm(R2425) Page46, copy Page49 HDMI redriver sch from G7D/G7 Page30 Q3502 pull high to 1.8VSUS Page30, 5V, add CHG_DEN controlled by EC Page53, Q3504/Q3505/R3503/R3506 change PN to 07005-00870100 change to R, R5301 change to N/A Page53, delete R5302, R5304, R5305, R5306 for Card detect inverter Page21, C1306/C1307 change component size to 0402 Page52'55, change ESD component D5202-D5205/D5502-D5505 to 07024-00640000, J5201 remove bypass routing Page61, R2106 changes option to N/A Page42, Q2401 R2602 C2627 changes option to @, R2611 change option to N/A Page36, R0632 change option to N/A Page37, R3708.1 change to +3VS Page71, R7117 change to 0 ohm set N/A update power sch 0408 Page56, U5903~U5906 change to 13N0G140T01011 Page48, copy Page48 HDMI redriver sch from GL504GM R20 0410 Page45, Panel_OD change to OD_C page45, add Q5102 Page45, add Q5702 20180411 update power sch 0410 Page44, R2425 change to pull high +3V +1.8V_SP1 Page39, U3904 IOC_GP23 exchange with GP2010' Page36, R0632 change option to N/A, R3631 set to @ Page71, C0110/C0111 change from to 2713D/C7109 Page71, C7124~C7128 change to 1uF Page71, delete Q7102, add Q3711,Q3712,Q3713,R2147@/R2148 20180412 Page42, C4206.1 net name change to SD_WP#_PCH Page21, delete Q2103,R2146/R2147@/R2148 ,add Q2102 Page71, add Q7708/Q7708A,R7707/R7708/R7709 Page71, P_PEX_VDD_PWRGD_AC_10 change to +12VS_+PEX_VDD, R7113 option change to N/A Page71, R7114 to 0 ohm N/A Page71, delete Q3504, add Q3501, R3517, C3530/C3501/C3502/C3503 Page31, delete Q3190, R3192, C3190 Page45, update HDMI redriver part (12vla), J4801 P/N change to 12022-00099800 update power sch 0411 20180413 update power sch 0412 Page45, add R4523/R4527 Page71, add C7719~C7787 Page25, add R3523/R3527,C3524 Page21, update Q1201/Q1202 E&O 20180416 Page45, update H6504/H6503/H6512/H6511,add H6502, H6531~H6534 Page37,C3702 nbs change to 3528,3300K,C7028/C7029/C7091/C7092/C7023/C7024/C7055/C7056 to 0402 size Page37,C7202 change to nbs footprint update AP_ANT sch 0418 Page43, delete eSPI board circuit Page61, update redriver EQ/PU setting Page30/56, update CAP LED netname for high active and update p56 sch update power sch 0416 20180417 Page48, L84801~L84804 change P/N to 09023-00020900 , option set N/A. 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SL2621 0402~~>0603, SL2414 0603~>0805 Page36, R3615 set @, R3618 set N/A change to 0402 560k ohm Page36, R3611/R3612/R3613/R3614 set @ Page36, R3611/R3614/R3615/C3502 set @ Page39, delete Q3501, add D3501, R3594 change to 1M update power sch 0511 Page70,CE7700 change to 1U0J15233792 Page71/72, C1109, C1110, C1111, C1121, C1201, C1202, C1203, C1204 change to 11202-00089000 Page71, Q7110 change to 07005-00870100, R7105 change to 140ohm, add R7124 20180514 Page45, U4501.7 change to +3VS_LCD_EN, R4512/R4513 also change to 0402 20180515 update power sch 0515 Page35, add R3502, R3584 change to 100k set @ Page45, R4504 560~~>0402 Page42, R4206/R4208 power plane~~>+3VS, add R4209/R4210 update power sch 0516 20180517 Page36, R3618 change to 1k ohm Page71, D3501 change to 07000406020 Page78, R7846 set N/A Page48, L84801~L84804 change P/N to 09009209400, J4801 update footprint to nbo_u_hdmi_19p_108 Page45, add D4201~4206 D2DIESD for layout, delete D4201-D4206/C4201-C4206 20180518 update power sch 0518 Page36, delete Q3801/R3801/R3803/R3810 Page36, delete R2443 Page37, delete Q5708/R5710/R5711, Q5707/R5761/R5732 option set @ Page35, delete R3584/C3504/R3517 Page48, LX4801~L84804 pin swap for layout 20180521 update power sch 0521 Page37, R5705 set N/A update power sch 0521-1 20180522 Page36, R3809 set N/A Page37, R3708 set N/A, R7840 set @ Page45, R4514 change to 4.3k ohm, R4501 change to 1.24k ohm update power sch 0522 20180523 update power sch 0523	20180524 Page71, R7113.1 change to P_LS +PEX_VDD_RC_10 Page48, R84801 change to 10K ohm Page48, P48805 change to 10K ohm GL704GM R1.1 R11a update power sch0524, 4phase 1V+10 NVDD Page71, add R7102 Page71, add C7151/C7152/C7153/C7171/C7192 ~~>0402 10uF option @/GPU_EG ~~~>/GPU_EG R12b update power sch 0525, delete GP/2A zunber R11c update power sch 0528, delete R29P401/R29P701 R11d update power sch 0528 R11e update power sch0529 1102321821140200 YAGEO~~~> 1102321821140240 TAIYO 1120З-00183000 YAGEO~~~> 1120З-00184000 TAIYO 1102321821140300 YAGEO~~~> 1102321821140340 TAIYO 1102321070040330 YAGEO~~~> 1102321070040370 WALSIN 1102321101210200 YAGEO~~~> 1102321103120460 TAIYO 1102321473120300 YAGEO~~~> 1102321473120320 WORAN 1102321681140200 YAGEO~~~> 1102321681140340 TAIYO R110 C7172改C77215/C77216/C77218/C77219/C77220 option /GPU_ED ~~~> /GPU_EC C7723改C7724/C77255/C77256 option /GPU_EA ~~~> /GPU_ED GL704GS R2.0 R20a Q3515B.5 PWM_D1P72_R rename ~~~> PWM_D1P72_G Page30/56, CAP_LED rename ~~~> CAP_LED# , change to low Active R20b Page31, replace JSE8531B with C3121 D7801 changes footprint to nbs R20c Page48, add R4837/R4838/R4839/R4840 option set @, add R4841/R4842 Page21, Q2102 option change to @ Page25, add R2501, GPP_D4 connect to R4513.1 Page63, add R6301/R6302/R6303/R6304/R6305, add R0303, ADD AZ4C80-B1LF-7 SSD1 to Page20, add R2060/R2061, ADD_AZ4C80-B1LF/SDD/SDI to page03 update power sch 0620 R20d Page31, J3101 Volume_up# and Volume_down# swap Page45, GD_C change to GD# C Page45, GD change to GD# C Page71, ~~OC~~ change to OC# C, GD# PCH change to OD_PCH Page35, R3505/R3509/R3528/R3529/R3531/R3533/R3534/R3535/R3537/R3539/ R3540/R3541/R3543 option set @ R20e Page48, delete R4824/R4825, R4837/R4838 change to 2.2k @ Page77, delete C77036/C77037/C77098/C77134, add C77035/C77097/C77133 option to GPU_KA for simulation recommend Page45, add R4545/R4546 R20f Page48, R4832 change to 5.6k ohm Page71, CE7101/CE7102/CE7103 change to 11020-00355100 R201 Page6, R0640 change to SL0401 Page21, R2102 change to SL2101 delete SL2016/SL2001 Page25, R2520 change to SL2504 Page26, R2655/R2658 change to SL2622/SL2623, R2605/R2606/R2608/R2610/R2611/R2651/R2652 change to SL2624~SL2630 Page28, R2814 change to SL2801,R2831/R2833 change to 75k ohm,1002127524020 Page30,R3008/R3013/R3015/R3017/R3021/R3023/R3040 change to SL3000~SL3027 Page31,R3119/R3120 change to SL3104/SL3105 Page35,R3501/R3502/R3503 change to 0ohm Page35,R3523/R3527 change to SL3505/SL3506 Page36,R3623/R3624 change to SL3609/SL3610,R2622/R2628 change to SL3611/SL3612 Page37,delete R3702 Page39,R3901/R3905 change to SL3901/SL3904 ,R3918/R3920/R3936/R3940 change to SL3907~SL3910 ,R3924/R3925/R3931/R3932/R3933/R3935/R3934 Page40,R4001/R4002/R4003 change to SL4001 Page44,R4402/R4403 change to SL4401/SL4402 Page45,R4510 change to SL4501 Page58,R5606/R5607 change to 1k ohm Page58,R5809 change to SL5804 Page65, R6520 change to sl2778 Page70, R7003.2 net (PERVDD_PWRGD) swap R7004.2 net (PWVDDQ_PWRGD) update power sch 0702 R203 Page31,add R3101/R3102, R3102 option @ Page45,add D4503@, R4532@/R4533@/R4528@, C4502@/C4513@/C4515@ Page49,delete C5912, add R5900/R5901, /C5921/C5922/C5923/C5925/C5926/C5927 change to 200pf R206 Page65,R6536 change to s09292, R6526/R6528/R6529 change to sl2381 R201 Page56,R5612 change to 1k ohm,LED5604.1 net name change to +5VSUS_WLANLED# Page45,R4521 change to 6.2k ohm,R4522 change to 1k ohm R200 Page11,R1106 option set N/A, R1114 option set @ GM R200 Page72,76,77,ALL option /GPU_ED change to @/GPU_EG update GM power sch 0629

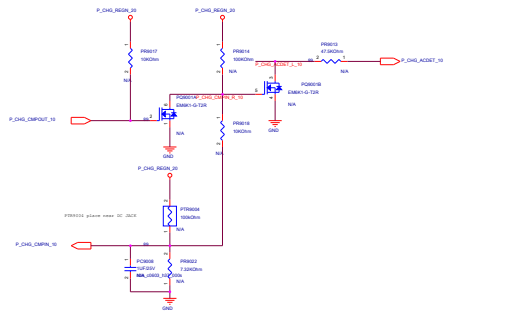
Address Selection Table

Address	0x78	0x7C	0x7A	0x7E	0x76	0x72	0x70
PER011	10k	1.5k	0k	3.65k	6.98k	6.19k	5.23k	8k
PER012	Open	6.19k	8.25k	6.65k	4.75k	5.49k	2.74k	2k

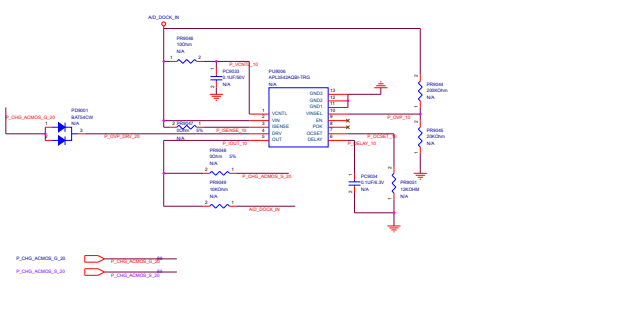
Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	R	W	W	R	R	R	R
Function	Temp. Alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

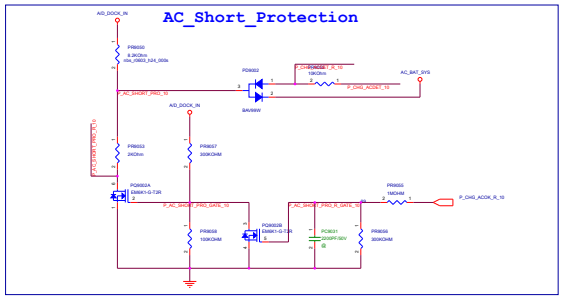
DC Jack thermal Protection

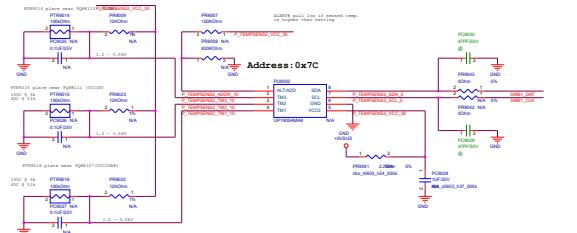


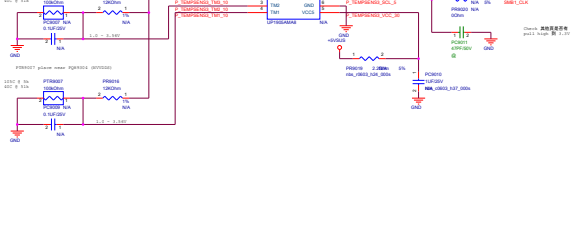
OVP Protection circuit(OVLO=24.3V,UVLO=6.875V)

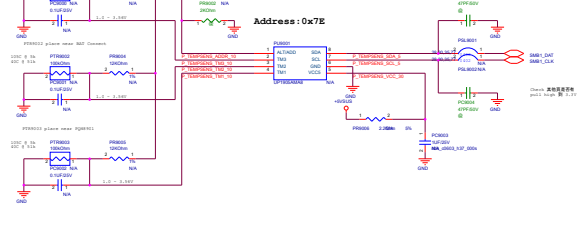


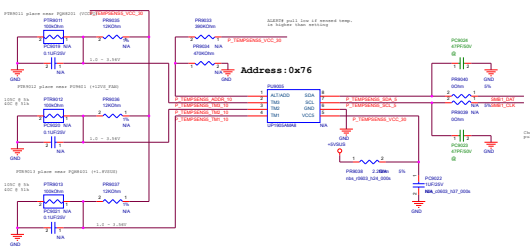
AC_Short_Protection

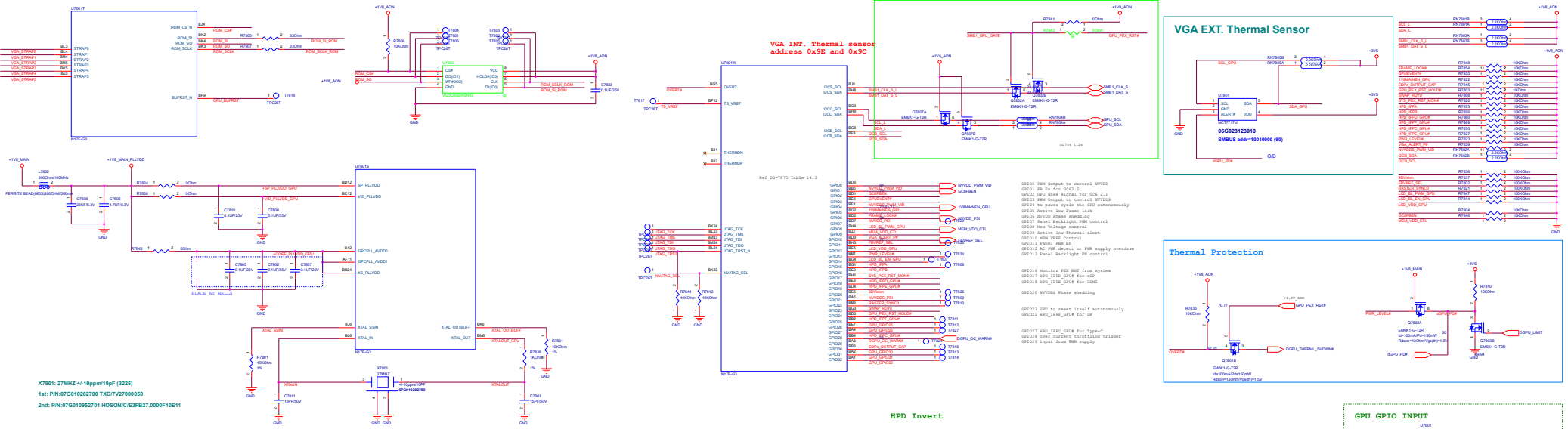


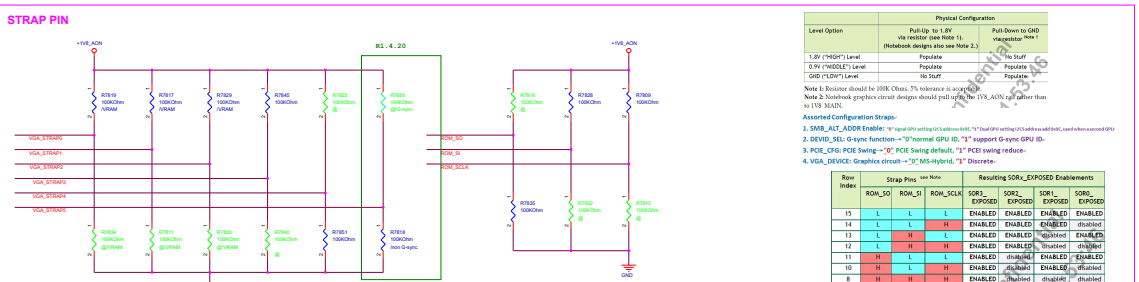












Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
M	H	L	14 (0x000E)
M	H	H	15 (0x000F)
H	L	M	16 (0x0010)
M	M	L	17 (0x0011)
M	M	H	18 (0x0012)
H	M	M	19 (0x0013)
L	M	M	20 (0x0014)
M	L	M	21 (0x0015)
M	M	L	22 (0x0016)
M	M	H	23 (0x0017)
M	H	M	24 (0x0018)
H	M	M	25 (0x0019)
M	M	M	26 (0x001A)

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	1	1
L	H	L	0	0	M	0
L	H	H	0	1	0	1
H	L	L	0	1	1	0
H	L	H	0	1	M	1
H	H	L	0	M	0	0
H	H	H	0	M	1	1
L	L	M	1	0	0	0
L	M	L	1	0	M	1
L	M	H	1	1	0	0
M	L	L	1	1	1	0
M	L	H	1	M	0	1
M	H	L	1	M	1	0
M	H	H	1	M	M	1

Level Option	Physical Configuration	
	Pull-Up to 1.8V via resistor (see Note 1). (Notebook designs also see Note 2.)	Pull-Down to GND via resistor Note 1
1.8V ("HIGH") Level	Populate	No Stuff
0.9V ("MIDDLE") Level	Populate	Populate
GND ("LOW") Level	No Stuff	Populate

Note 1: Resistor should be 10Kk Ohms. 5% tolerance is acceptable.
Note 2: Notebook graphics circuit designs should pull up to the 1V8_AON rail rather than to 1V8 MAIN.

Assorted Configuration Straps:
1. SMB_ALT_ADDR Enable: "0" signal GPU setting I2C5 address=0x9E, "1" Dual GPU setting I2C5 address add 0x9C, used when a second GPU
2. DEVID_SEL: G-sync function→"0"normal GPU ID, "1" support G-sync GPU ID.
3. PCIE_CFG: PCIE Swing→"0" PCIE Swing default, "1" PCEI swing reduce.
4. VGA_DEVICE: Graphics circuit→"0" MS-Hybrid, "1" Discrete.

Row Index	Strap Pins See Note			Resulting SOR±_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	H	X	X	(reserved, do not configure)			
	All other Strap Configurations			(Reserved)			

Total Display Links (HDMI, DP or DVI) — See This Row ref Table 5.4

	Total Enabled for Audio (HDMI, DP or DVI)	Is eDP Supported on: IFPA or IFPB?	IFPC or IFPD?	IFPE or IFPF?	
4	4	--	--	--	15
4	3	yes	--	--	14
4	3	--	yes	--	13
4	3	--	--	yes	11
3	3	--	--	--	10
3	2	yes	--	--	12
3	2	--	yes	--	12
3	2	--	--	yes	10
2	2	--	--	--	12
2	1	yes	--	--	8
2	1	--	yes	--	8
2	1	--	--	yes	8
1	1	--	--	--	8
1	0	yes	--	--	0
1	0	--	yes	--	0
1	0	--	--	yes	0

NVIDIA GC6 2.0 follow DG-07290-001_v01
GPU_GPIO 5 --> FRAME_LOCK# (Input, Open Drain)
High -->driver display ,Low Normal

FRAME_LOCK#_C Pull High +3VS_LCD at Panel side

For EMI

Project Name	GL704GSM
Rev	81.1
Title :	GPU_CLOCK/STRAP/GPIO
Size: Custom	
Dept.:	ASUSTeK COMPUTER INC.
Engineer:	Gaming RD4 EE1
Date:	Friday, July 27, 2018
Sheet	78 of 103