MS_7641 VER: 3.1

CPU:

AMD AM3

System Chipset:

AMD/ATI 760G/785G/880G

AMD/ATI RS710

On Board Chipset:

FINTEK Super I/O -- F71869AD
LAN -- RLT8111E
HD Codec --ALC887/892
BIOS -- SPI ROM 8M

Main Memory:

DDR III X 2 (Max 8GB)

Expansion Slots:

PCI-E X1 X1
PCI-E X16 X1
PCI 2.2 Slot X1

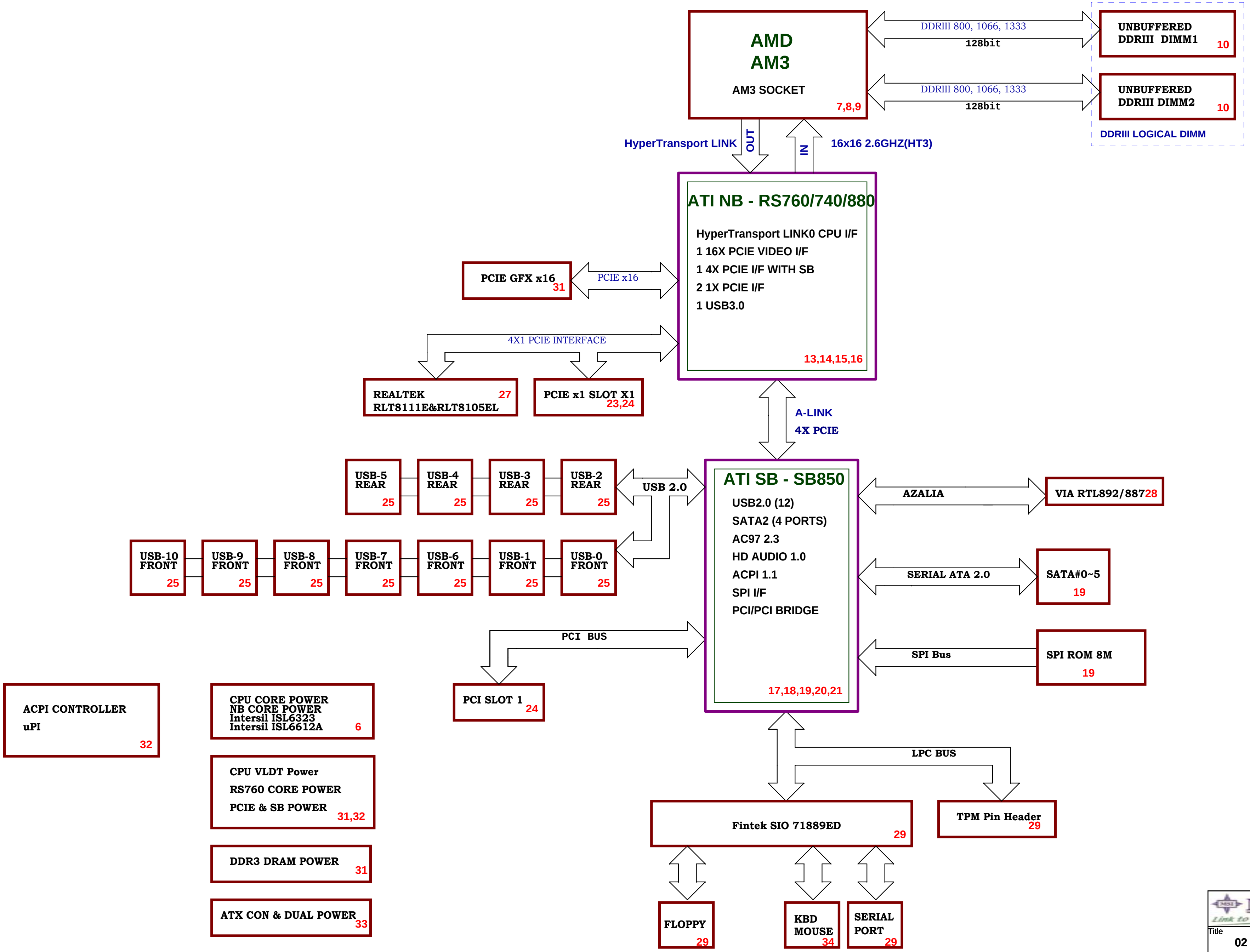
Clock Generator:

Controller--RTM-880N-793

PWM:

UPI1601

Project RS-740/760 BLOCK DIAGRAM



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title		
02 BLOCK DIAGRAM		
Size: Custom	Document Number: MS_7641	Rev: 0A
Date: Monday, July 25, 2011	Sheet 2 of 36	

SB700/750 GPIO Config

GPIO Name	Type	Function description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	19
REQ3#/GPIO70		PREQ#3	AE6	19
REQ4#/GPIO71		PREQ#4	AB6	19
GNT3#/GPIO72		Unused	AC6	19
GNT4#/GPIO73		Unused	AE5	19
INTE#/GPIO33		PCI_INTA#	AD3	19
INTF#/GPIO33		PCI_INTB#	AC4	19
INTG#/GPIO33		PCI_INTC#	AE2	19
INTH#/GPIO33		PCI_INTD#	AE3	19
LDRQ1#/GNT5#/GPIO68		Unused	AB8	19
BMREQ#/REQ5#/GPIO68		PREQ#5	AD7	19
RI#/EXTEVNT0#		RI#	E2	19
SLP_S2/GPM9#		Unused	H7	19
GA20IN/GEVENT0#		A20GATE	Y15	19
KBRST#/GEVENT1#		KBRST#	W15	19
LPC_PME#/GEVENT3#		LPC_PME#	K4	19
LPC_SMI#/EXTEVNT1#		LPC_SMI3	K24	19
S3_STATE/GEVENT5#		Unused	F1	19
SYS_RESET#/GPM7#		FP_RST#	J2	19
WAKE#/GEVENT8#		WAKE#	H6	19
BLINK/GPM6#		Unused	F2	19
MBALERT#THRMTRIP#/GEVENT2#		SMBALERT#	J6	19
SATA_ISO#/GPIO10		SB_GPIO10	AE18	19
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6	AD18	19
SMARTVOLT/SATA_IS2/GPIO4		SB_GPIO4	AA19	19
CLK_REQ0#SATA_IS3#/GPIO0		SB_GPIO0	W18	19
CLK_REQ1#/SATA_IS4#/GPIO3		SB_GPIO39	V17	19
CLK_REQ2#/SATA_IS5#/GPIO40		SB_GPIO40	W20	19
SPKR/GPIO2		SPKR	W21	19
SCL0/GPOC0#		SCLK	AA18	19
SDA0/GPOC1#		SDATA	W18	19
SCL1/GPOC2#		SCLK1	K1	19
SDA1/GPOC3#		SDATA1	K2	19
DDC1_SCL/GPIO9		Unused	AA20	19
DDC1_SDA/GPIO8		SPI_WP#	Y18	19
LLB3/GPIO66		LC_SENSE	C1	19
SHUTDOWN#/GPIO5		SB_GPIO5	Y19	21
DDR3_RST#/GEVENT7#		Unused	G5	21
SB_OC6#/IR_TX1/GEVENT6#		OC6#	B9	21
USB_OC5#/IR_TX0/GPM5#		OC5#	B8	21
USB_OC4#IO_RX0/GPM4#		OC4#	A8	21
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	21
USB_OC2#/GPM2#		OC2#	E5	21
USB_OC1#/GPM1#		OC1#	F8	21
USB_OC0#/GPM0#		OC0#	E4	21
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	21
AZ_SDIN1/GPIO43		Unused	J8	21
AZ_SDIN2/GPIO44		Unused	L8	21
AZ_SDIN3/GPIO46		Unused	M3	21

SB700/750 GPIO Config

GPIO Name	Type	Function description	Pin	Page
AZ_DOCK_RST#/GPM8#	3.3V	Unused	L5	21
PS2_DAT/EC_GPIO0		Unused	H19	21
PS2_CLK/EC_GPIO1		Unused	H20	21
SPI_CS2#/EC_GPIO2		Unused	H21	21
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	21
PS2KB_DAT/EC_GPIO4		Unused	D22	21
PS2KB_CLK/EC_GPIO5		Unused	E24	21
PS2M_DAT/EC_GPIO6		Unused	E25	21
PS2M_CLK/EC_GPIO7		Unused	D23	21
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	21
KSO_16/EC_GPIO8		Unused	A18	21
KSO_17/EC_GPIO9		Unused	B18	21
EC_PWM0/EC_GPIO10		Unused	F21	21
SCL2/EC_GPIO11		Unused	D21	21
SDA2/EC_GPIO12		Unused	F19	21
SCL3_LV/EC_GPIO13		Unused	E20	21
SDA3_LV/EC_GPIO14		Unused	E21	21
EC_PWM1/EC_GPIO15		Unused	E19	21
EC_PWM2/EC_GPIO16		SB_GP16	D19	21
EC_PWM3/EC_GPIO17		Unused	E18	21
KSI_0/EC_GPIO18		Unused	G20	21
KSI_1/EC_GPIO19		Unused	G21	21
KSI_2/EC_GPIO20		Unused	D25	21
KSI_3/EC_GPIO21		Unused	D24	21
KSI_4/EC_GPIO22		Unused	C25	21
KSI_5/EC_GPIO23		Unused	C24	21
KSI_6/EC_GPIO24		Unused	B25	21
KSI_7/EC_GPIO25		Unused	C23	21
KSO_0/EC_GPIO26		Unused	B24	21
KSO_1/EC_GPIO27		Unused	B23	21
KSO_2/EC_GPIO28		Unused	A23	21
KSO_3/EC_GPIO29		Unused	C22	21
KSO_4/EC_GPIO30		Unused	A22	21
KSO_5/EC_GPIO31		Unused	B22	21
KSO_6/EC_GPIO32		Unused	B21	21
KSO_7/EC_GPIO33		Unused	A21	21
KSO_8/EC_GPIO34		Unused	D20	21
KSO_9/EC_GPIO35		Unused	C20	21
KSO_10/EC_GPIO36		Unused	A20	21
KSO_11/EC_GPIO37		Unused	B20	21
KSO_12/EC_GPIO38		Unused	B19	21
KSO_13/EC_GPIO39		Unused	A19	21
KSO_14/EC_GPIO40		Unused	D18	21
KSO_15/EC_GPIO41		Unused	C18	21
SATA_ACT#/GPIO67		SATA_LED#	W11	21
IDE_D0/GPIO15		Unused	AD24	21
IDE_D1/GPIO16		Unused	AD23	21
IDE_D2/GPIO17		Unused	AE22	21
IDE_D3/GPIO18		Unused	AC22	21

SB700/750 GPIO Config

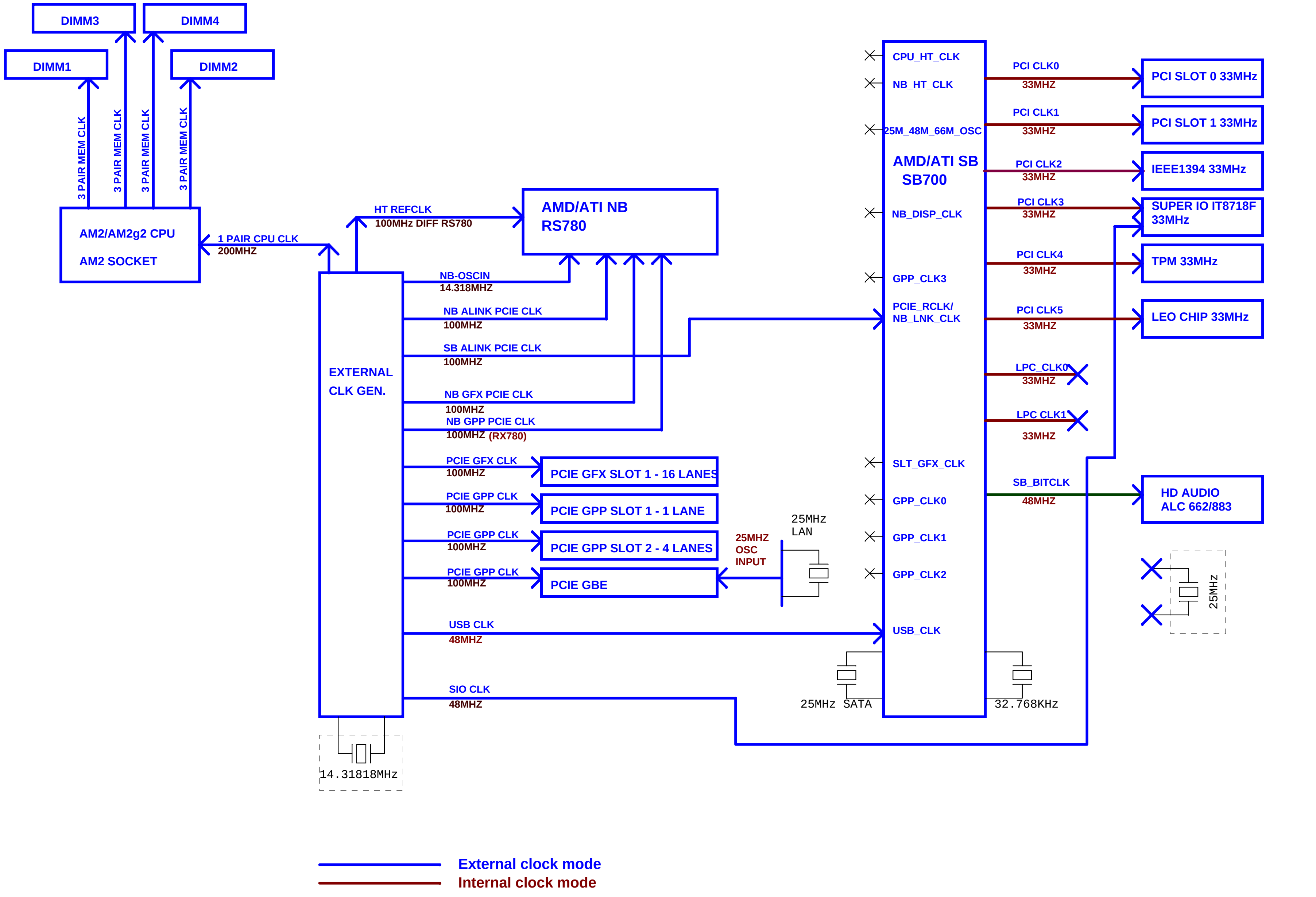
GPIO Name	Type	Function description	Pin	Page
IDE_D4/GPIO19	3.3V	Unused	AD21	20
IDE_D5/GPIO20		Unused	AE20	
IDE_D6/GPIO21		Unused	AB20	
IDE_D7/GPIO22		Unused	AD19	
IDE_D8/GPIO23		Unused	AE19	
IDE_D9/GPIO24		Unused	AC20	
IDE_D10/GPIO25		Unused	AD20	
IDE_D11/GPIO26		Unused	AE21	
IDE_D12/GPIO27		Unused	AB22	
IDE_D13/GPIO28		Unused	AD22	
IDE_D14/GPIO29		Unused	AE23	
IDE_D15/GPIO30		Unused	AC23	
SPI_DI/GPIO12		SPI_DATAIN	G6	
SPI_DO/GPIO11		SPI_DATAOUT	D2	
SPI_CLK/GPIO47		SPI_CLK	D1	
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	
SPI_CS#/GPIO32		SPI_CS#	F3	
LAN_RST#/GPIO14		CPU_PRESENT#	U15	
ROM_RST#/GPIO14		Unused	J1	
FANOUT0/GPIO3		Unused	M8	
FANOUT1/GPIO48		COM_GPIO	M5	
FANOUT2/GPIO49		Unused	M7	
FANIN0/GPIO50		Unused	P5	
FANIN1/GPIO51		Unused	P8	
FANIN2/GPIO52		Unused	E8	
TEMPIN0/GPIO61		Unused	B6	
TEMPIN1/GPIO62		Unused	A6	
TEMPIN2/GPIO63		Unused	A5	
TEMPIN3/TALERT#/GPIO64		TALERT3	B5	
VIN0/GPIO53		Unused	A4	
VIN1/GPIO54		Unused	B4	
VIN2/GPIO55		Unused	C4	
VIN3/GPIO56		Unused	D4	
VIN4/GPIO57		Unused	D5	
VIN5/GPIO58		Unused	D6	
VIN6/GPIO59		Unused	A7	
VIN7/GPIO60		Unused	B7	

F71882 GPIO Config

GPIO Name	Type	Function description	Pin	Page
VIDO5/GP27	3.3V	Unused	AD21	20
VIDO4/GP26		Unused	AE20	
VIDO1/GP21/VGP0		Unused	AB20	
PME#/GP54		Unused	AD19	
KRST#/GP62		Unused	AE19	
GA20/JP7		Unused	AC20	
KDAT/GP61		Unused	AD20	
KCLK/GP60		Unused	AE21	
MDAT/GP57		Unused	AB22	
MCLK/GP56		Unused	AD22	
SUSC#/GP53		Unused	AE23	
PSON#/GP42		Unused	AC23	
PANSWH#/GP43		SPI_DATAIN	G6	
PWRON#/GP44		SPI_DATAOUT	D2	
PCIRST3#/GP11		SPI_CLK	D1	
PCIRST2#/GP12		SPI_HOLD_L	F4	
FAN_CTL3/GP36		SPI_CS#	F3	
FAN_TAC3/GP36		CPU_PRESENT#	U15	
FAN_CTL2/GP51		Unused	J1	
FAN_TAC2/GP52		Unused	M8	
FAN_CTL1		COM_GPIO	M5	
FAN_TAC1		Unused	M7	
VID2/GP32		Unused	P5	
VID3/GP33		Unused	P8	
VID3/GP33		Unused	E8	
VID4/GP34		Unused	B6	
VID5/GP35		Unused	A6	

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTE# PCI_INTF# PCI_INTG# PCI_INTH#	PREQ#0 PGNT#0	AD21	PCICLK0
PCI Slot 2	PCI_INTF# PCI_INTG# PCI_INTH# PCI_INTE#	PREQ#1 PGNT#1	AD22	PCICLK1



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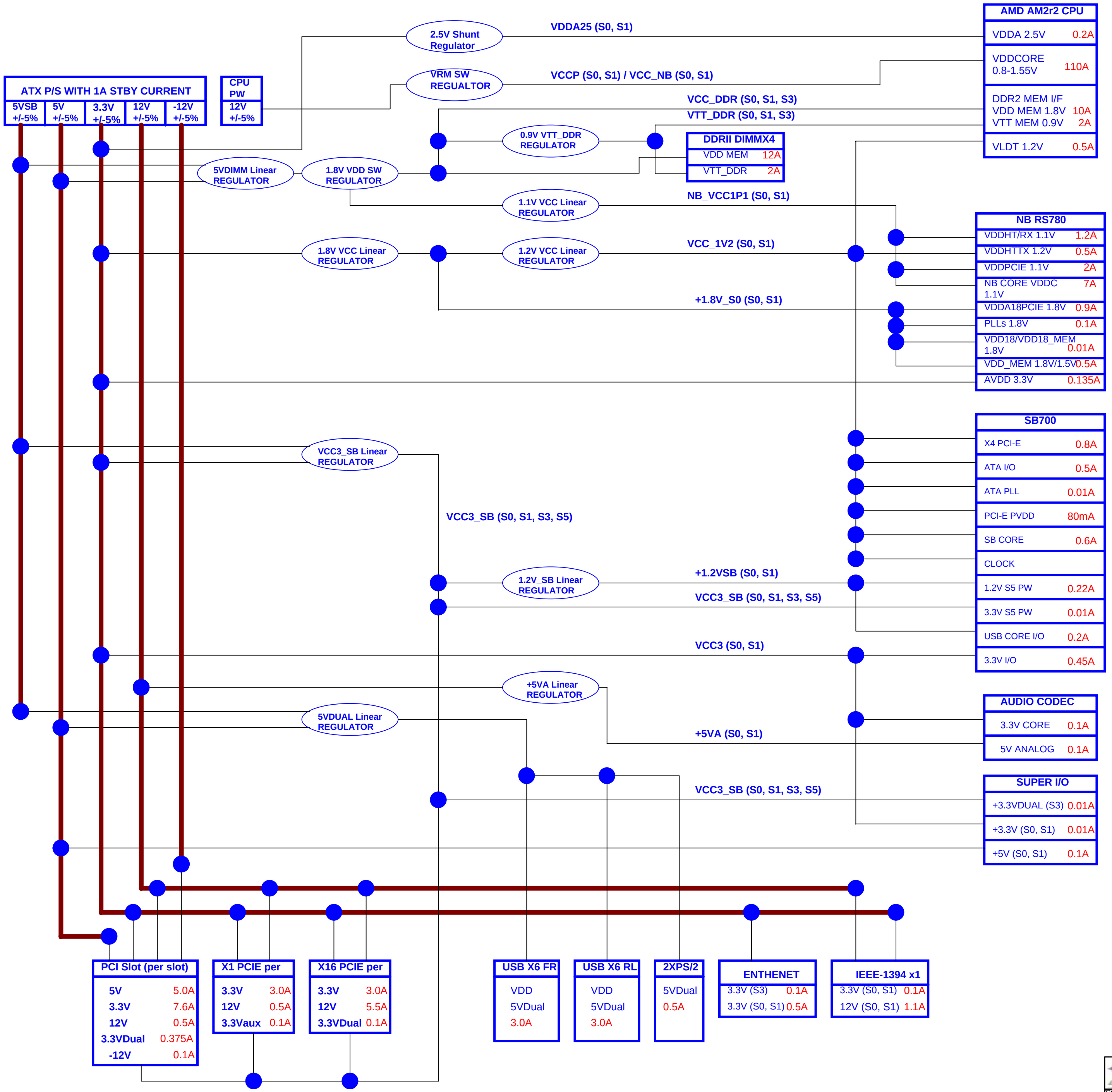
MICRO-START INT'L CO.,LTD.

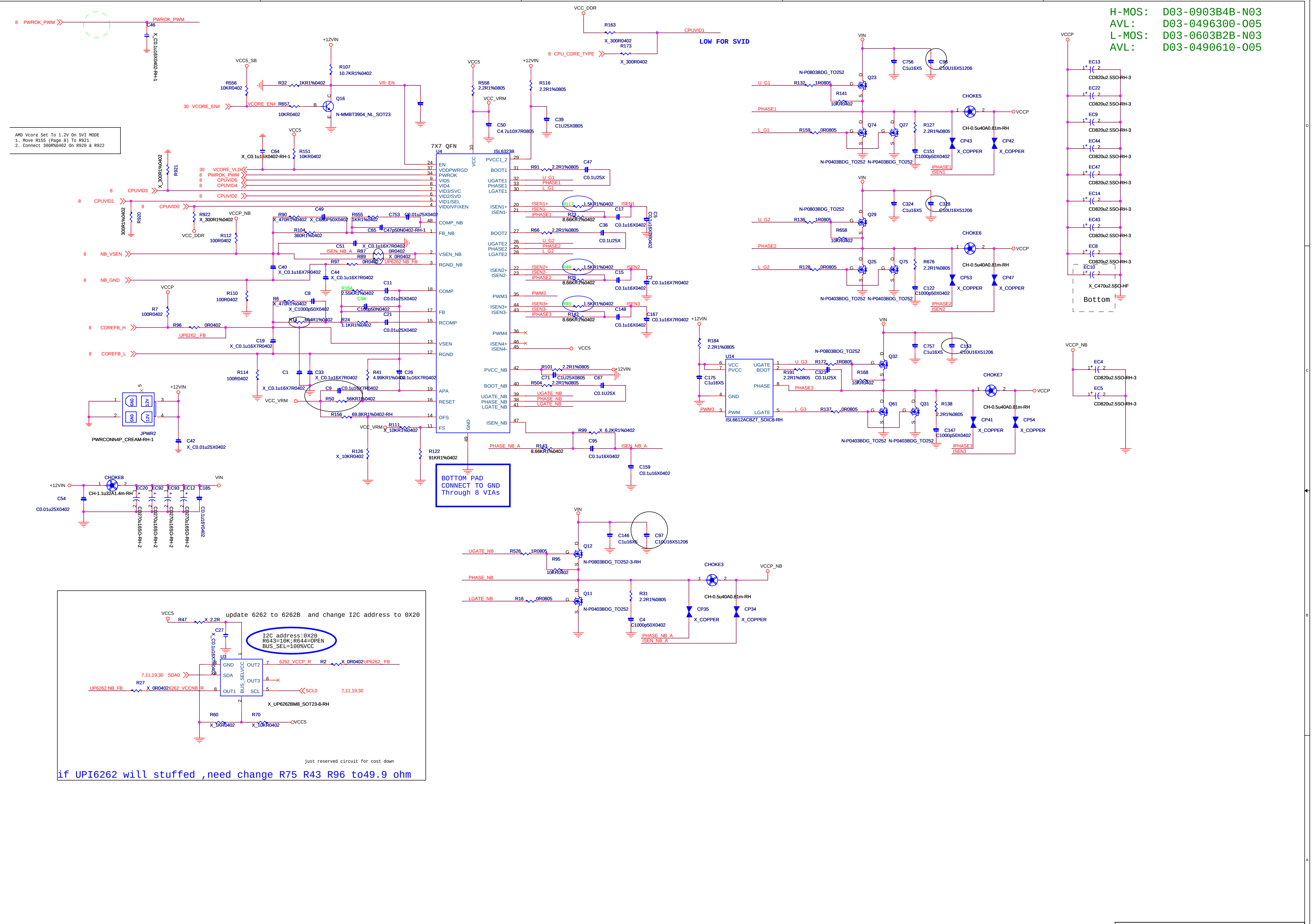
Title	04 Clock Distribution	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Monday, July 25, 2011	Sheet 4 of 36	

Power Deliver Chart



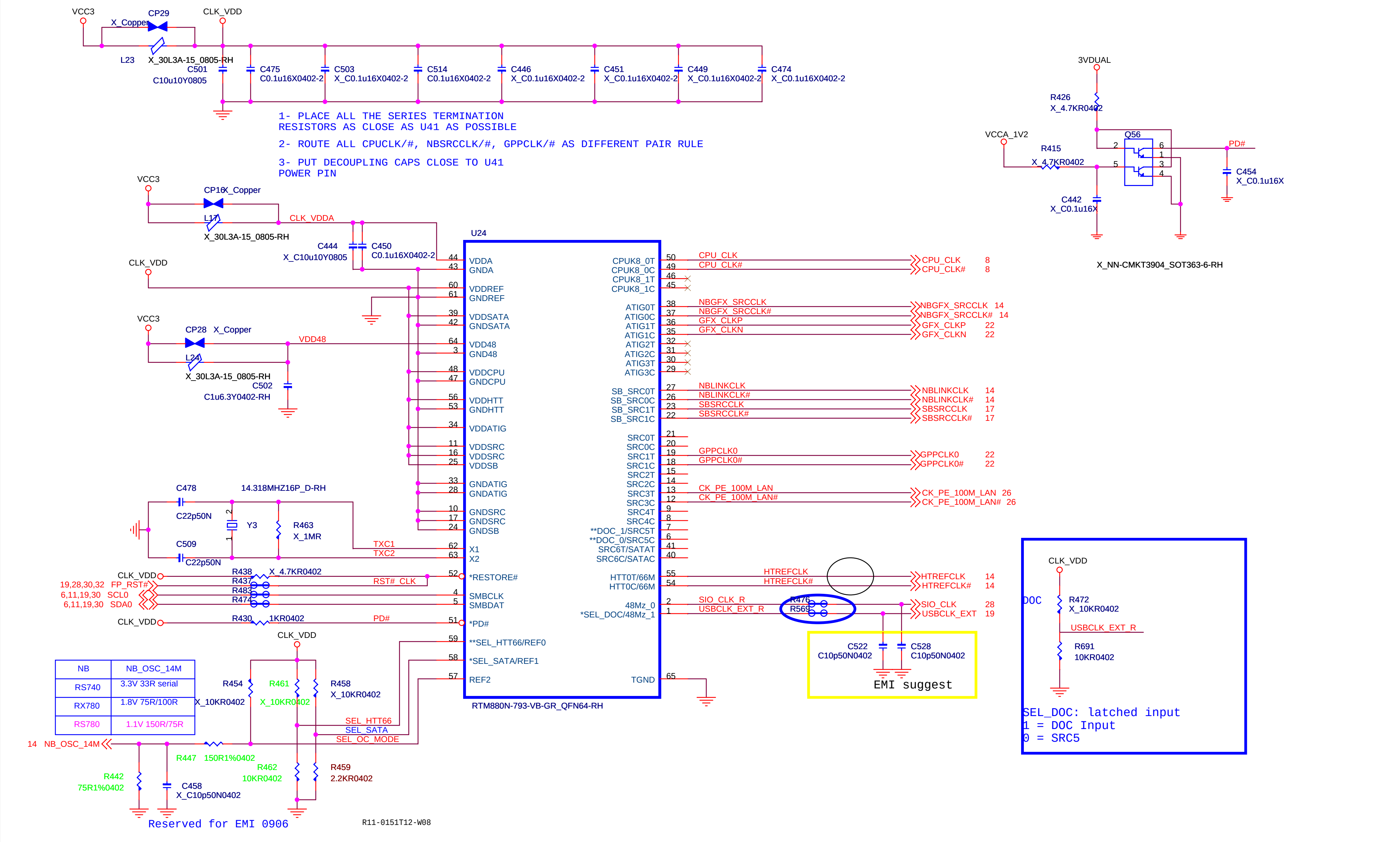
MSI MICRO-START INT'L CO.,LTD.

Title	05 Power Deliver Chart	
Size C	Document Number MS_7641	Rev 30
Date: Monday, July 25, 2011	Sheet 5 of 36	



MSI MICRO-START INT'L CO.,LTD.

Title	06 INTSIL ISL6323B	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Monday, August 01, 2011	Sheet 6 of 36	



NB	NB_OSC_14M
RS740	3.3V 33R serial
RX780	1.8V 75R/100R
RS780	1.1V 150R/75R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title: 07 Clock-Gen RTM880N-793

Size: Custom | Document Number: MS_7641 | Rev: 30

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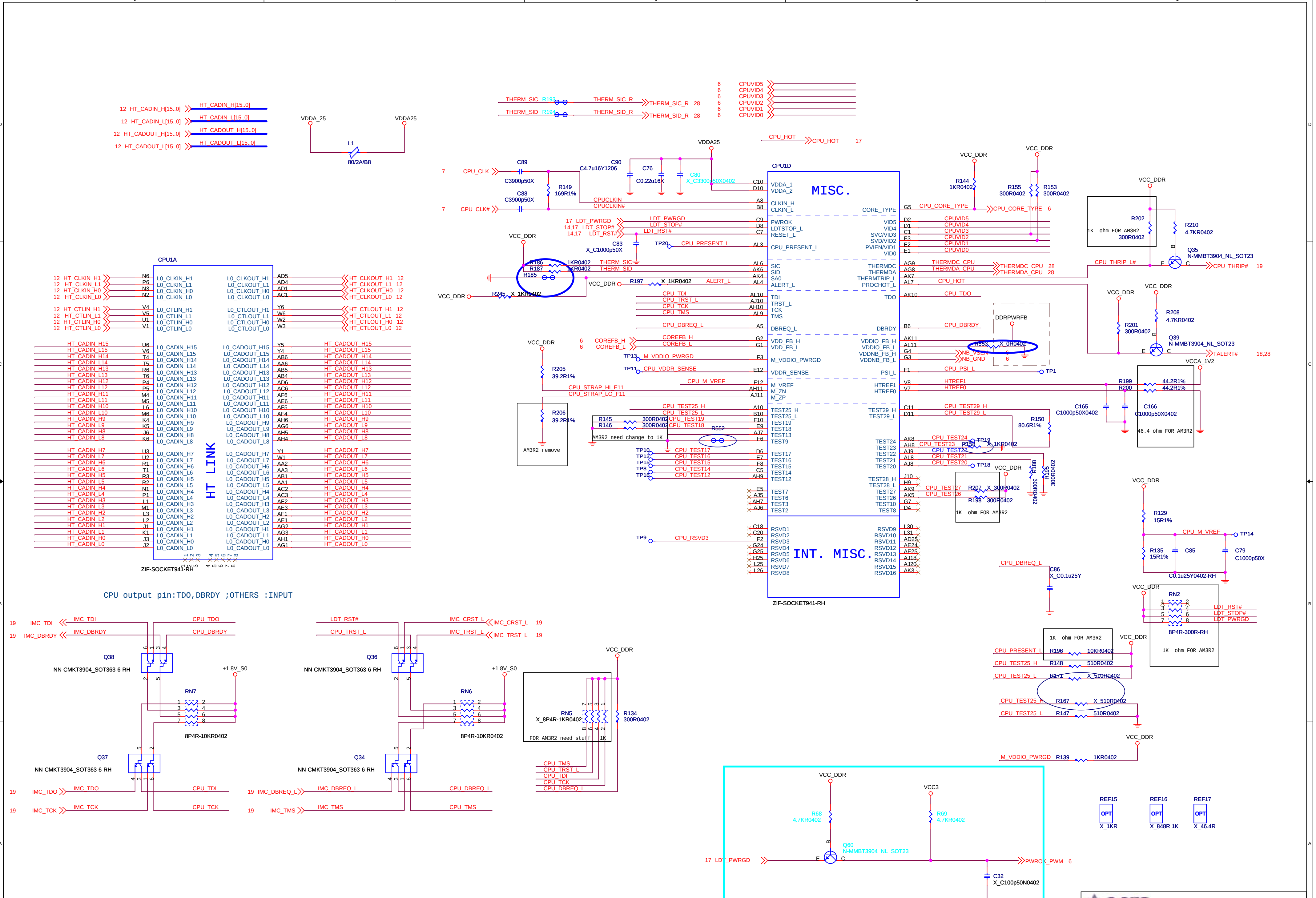
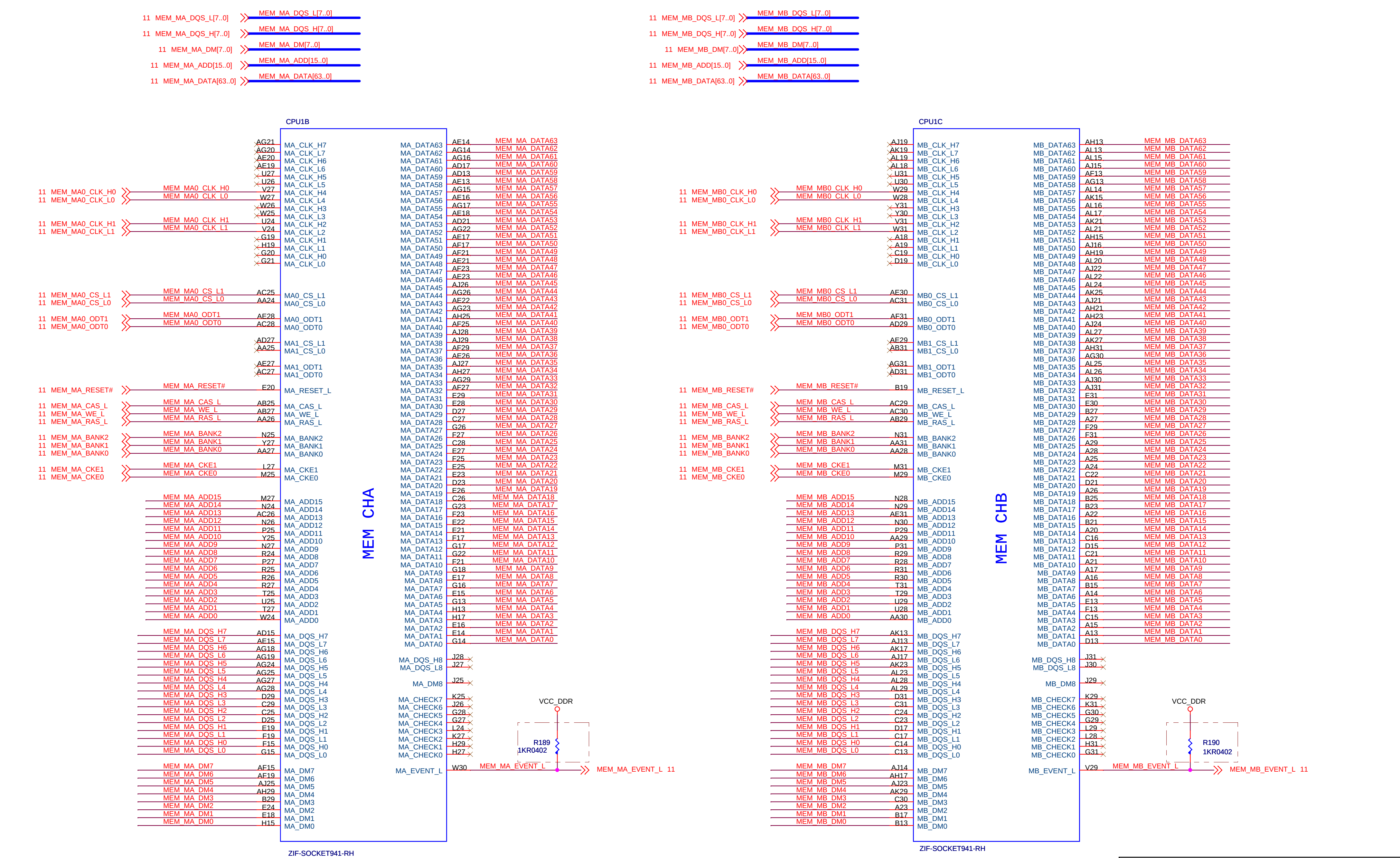


MICRO-START INT'L CO.,LTD.

Title	08 AM3 HT I/F,CTRL&DEBUG	
Size Custom	Document Number MS_7641	Rev 30
Date: Tuesday, August 02, 2011	Sheet 8 of 36	



MSI MICRO-START INT'L CO.,LTD.

Title: 09 AM3 DDR MEMORY I/F

Size	Document Number	Rev
Custom	MS_7641	30

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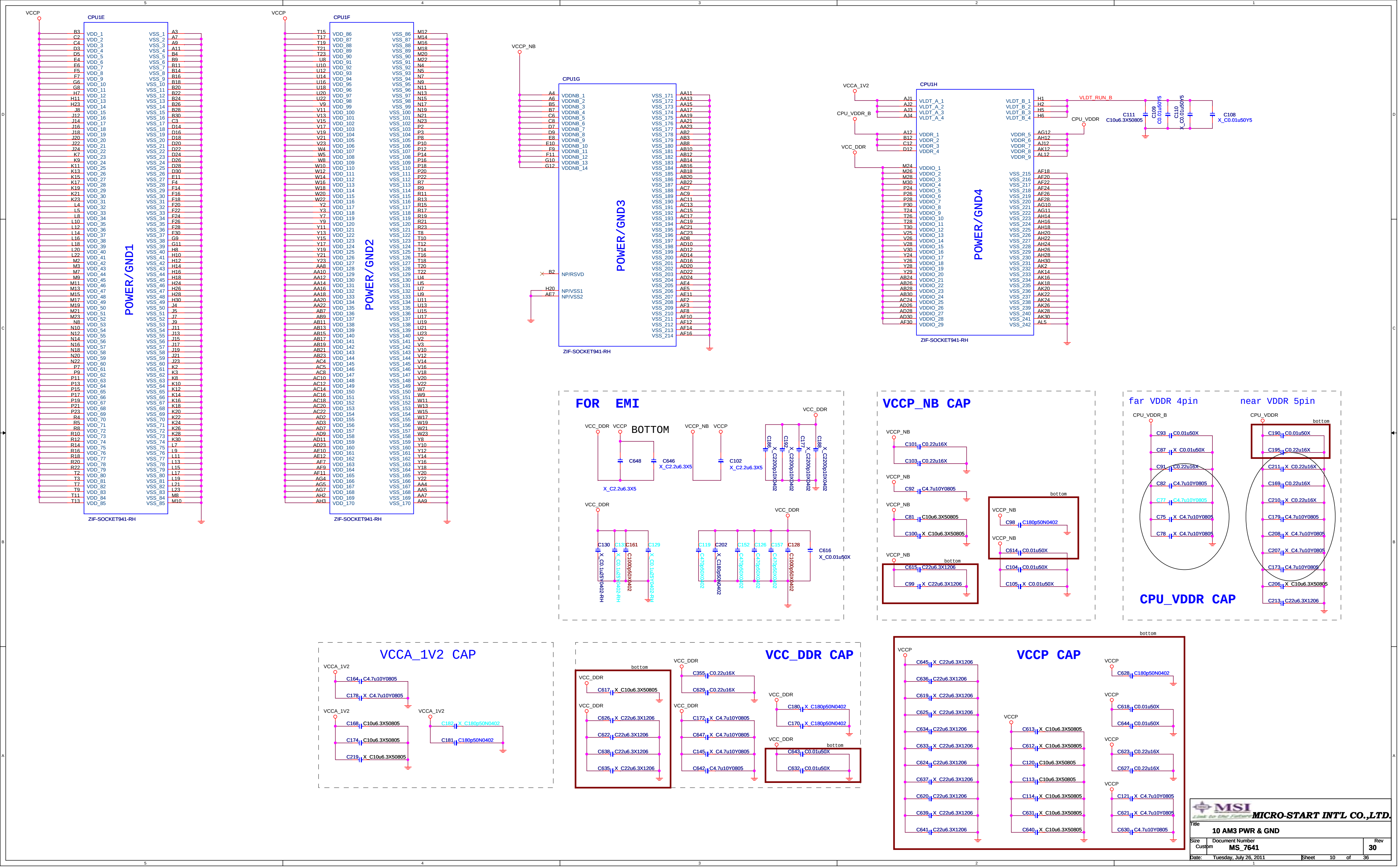
CPU1E
POWER/GND1
ZIF-SOCKET941-RH
CPU1F
POWER/GND2
ZIF-SOCKET941-RH
CPU1G
POWER/GND3
ZIF-SOCKET941-RH
CPU1H
POWER/GND4
ZIF-SOCKET941-RH
VCCP
VCCP_NB
VCCA_1V2
CPU_VDDR_B
VCC_DDR
CPU_VDDR
VLDT_RUN_B
NP/RSVD
NP/VSS1
NP/VSS2
FOR EMI
BOTTOM
VCCP_NB CAP
far VDDR 4pin
near VDDR 5pin
CPU_VDDR CAP
VCCA_1V2 CAP
VCC_DDR CAP
VCCP CAP
bottom
MICRO-START INT'L CO.,LTD.
Title
10 AM3 PWR & GND
Size
Custom
Document Number
MS_7641
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30
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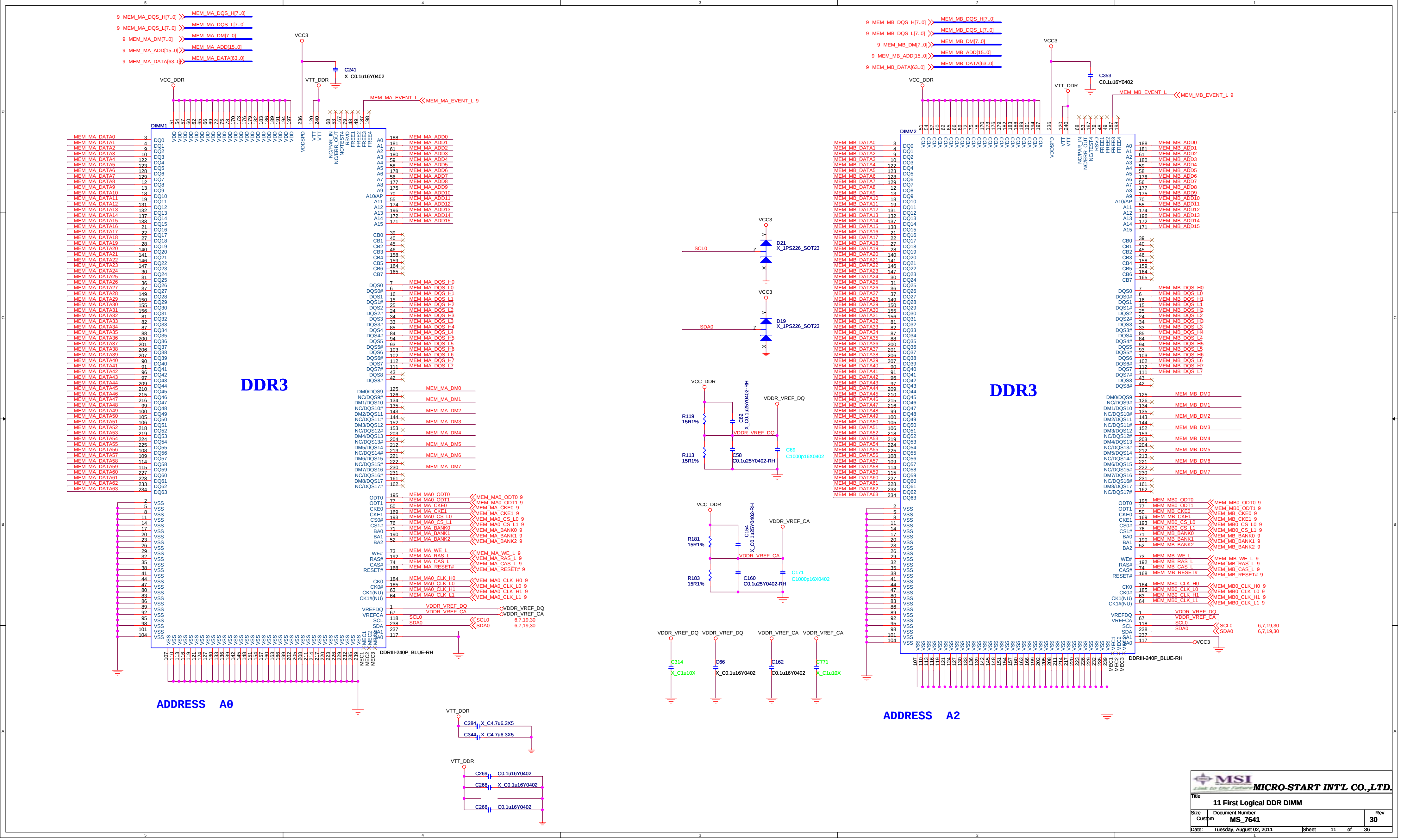
DDR3
DDR3
DIMM1
DIMM2
DDRIII-240P_BLUE-RH
DDRIII-240P_BLUE-RH
ADDRESS A0
ADDRESS A2
VCC_DDR
VCC3
VTT_DDR
VDDR_VREF_DQ
VDDR_VREF_CA
MEM_MA_DQS_H[7..0]
MEM_MA_DQS_L[7..0]
MEM_MA_DM[7..0]
MEM_MA_ADD[15..0]
MEM_MA_DATA[63..0]
MEM_MB_DQS_H[7..0]
MEM_MB_DQS_L[7..0]
MEM_MB_DM[7..0]
MEM_MB_ADD[15..0]
MEM_MB_DATA[63..0]
MEM_MA_EVENT_L
MEM_MB_EVENT_L
C241 X_C0.1u16Y0402
C353 C0.1u16Y0402
D21 X_1PS226_SOT23
D19 X_1PS226_SOT23
SCL0
SDA0
R119 15R1%
R113 15R1%
C62 X_C0.1u25Y0402-RH
C58 C0.1u25Y0402-RH
C69 C1000p16X0402
R181 15R1%
R183 15R1%
C154 X_C0.1u25Y0402-RH
C160 C0.1u25Y0402-RH
C171 C1000p16X0402
C314 X_C1u10X
C66 X_C0.1u16Y0402
C162 C0.1u16Y0402
C771 X_C1u10X
C284 X_C4.7u6.3X5
C344 X_C4.7u6.3X5
C269 C0.1u16Y0402
C268 X_C0.1u16Y0402
C266 C0.1u16Y0402
MSI
MICRO-STAR INT'L CO.,LTD.
Title
11 First Logical DDR DIMM
Size Custom
Document Number MS_7641
Rev 30
Date: Tuesday, August 02, 2011
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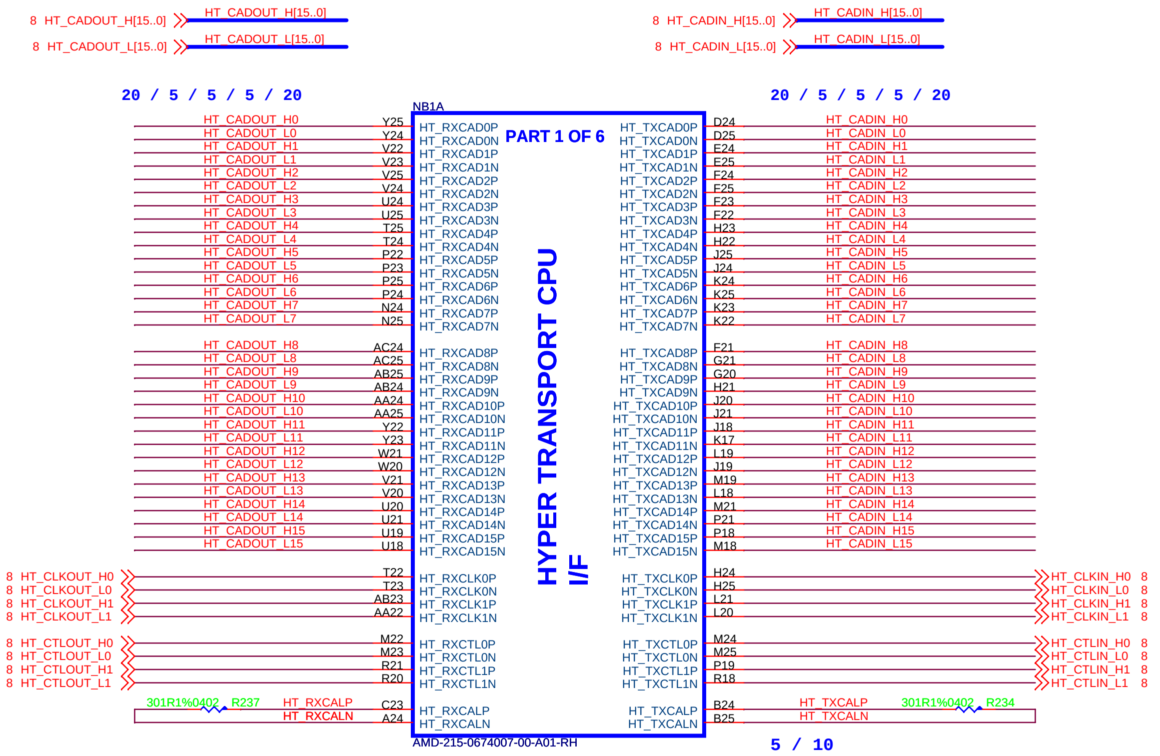
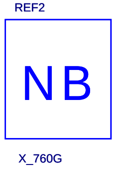
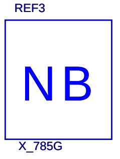


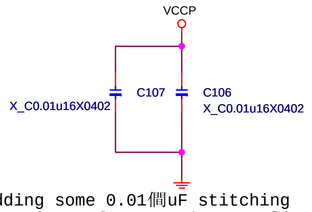




Check U10 New Version : Port Number

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R



Adding some 0.01個uF stitching
capacitors for crossing a split when
these signals change different reference
layer.

MICRO-START INT'L CO.,LTD.

Title	13 760G&785G&880G-HT
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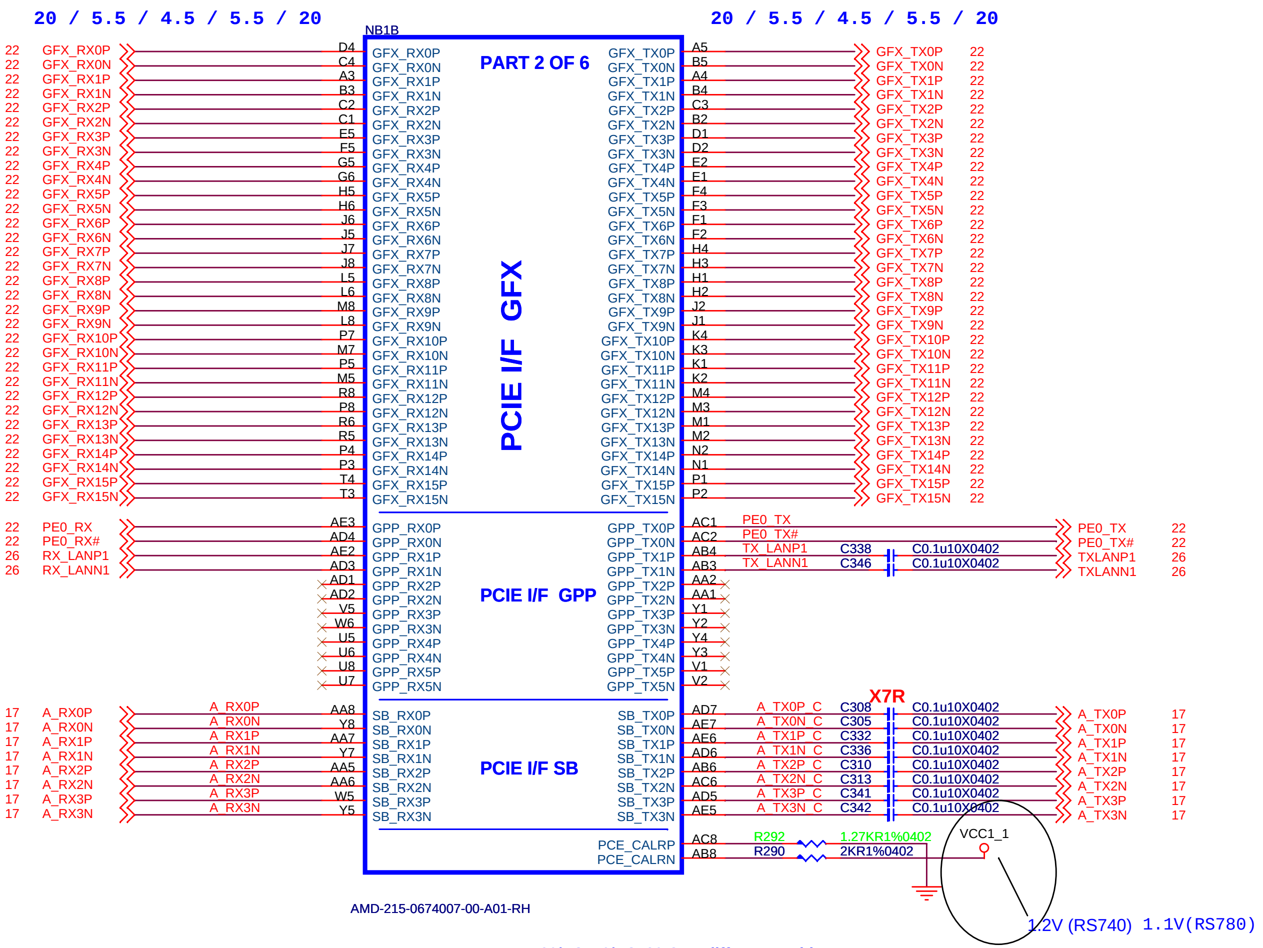

RX780/RS740/RS780 GPP difference table

	RS740	RX780/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RX780/RS740/RS780 GPP Routing table

	RS740	RX780/RS780
GPP X4 CONNECTOR	GPP[2:0]	GPP[3:0]
GPP X1 CONNECTOR		GPP4
GIGABIT ETHERNET	GPP3	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

MSI MICRO-START INT'L CO.,LTD.

Title: 14 760G&785G&880G-PCIE I/F

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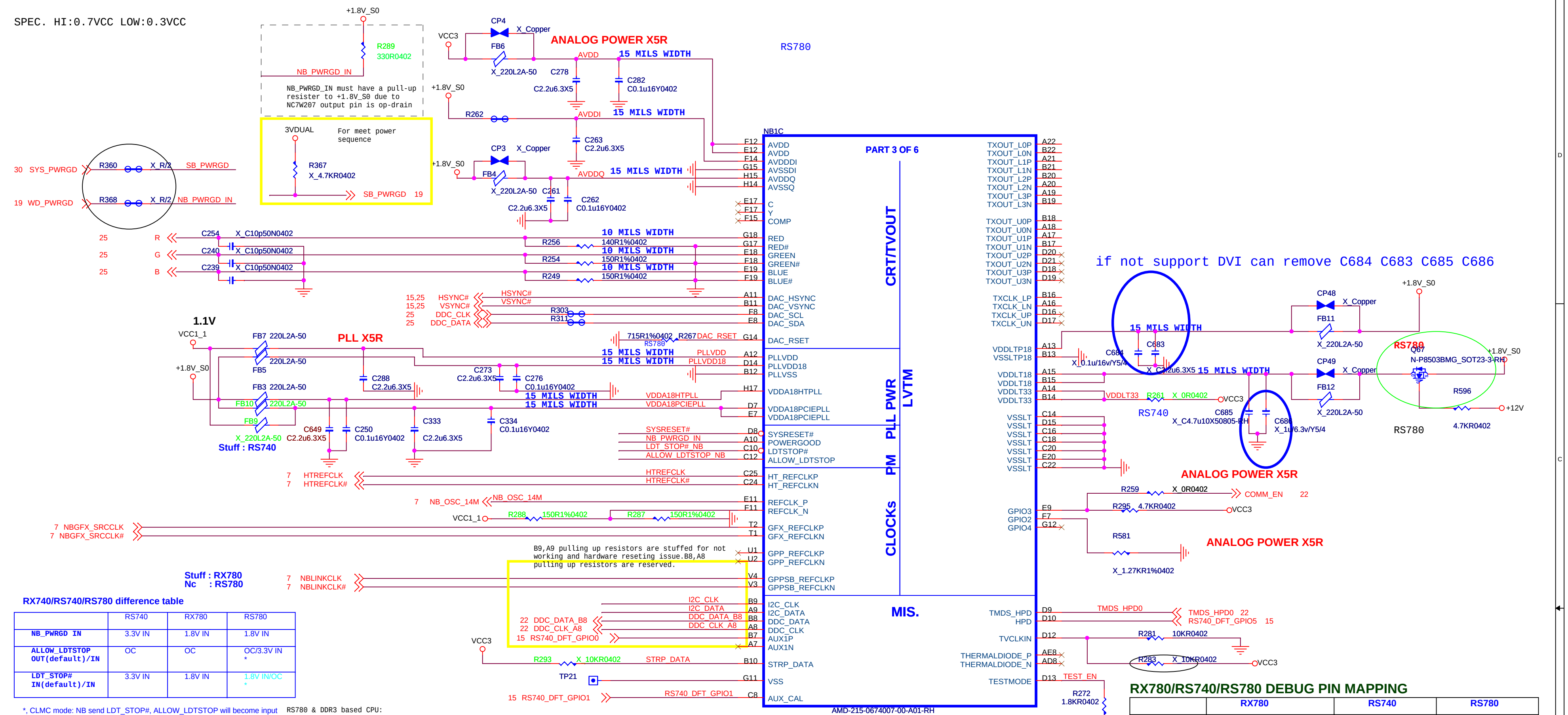
SPEC. HI:0.7VCC LOW:0.3VCC



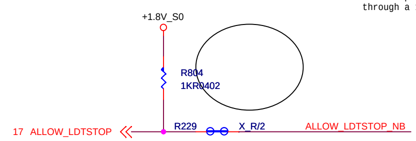
RX740/RS740/RS780 difference table

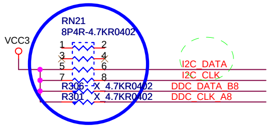
	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC	OC	OC/3.3V IN *
LDT_STOP# IN(default)/IN	3.3V IN	1.8V IN	1.8V IN/OC *

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

RS780 & DDR3 based CPU: use an open-drain buffer and pulled up to 1.8V_S0 through a 1-kR 5% resistor on the Northbridge side

STRP_DATA
If not implemented:
RS740: Pulled up to 3.3 V with a 10-k? 5% resistor.
RS780: Not Connected.
RX780: Pulled up to 1.8 V with a 10-k? 5% resistor.





RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)

RX780: pin DFT_GPIO5
RS780: pin VSYNC

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)

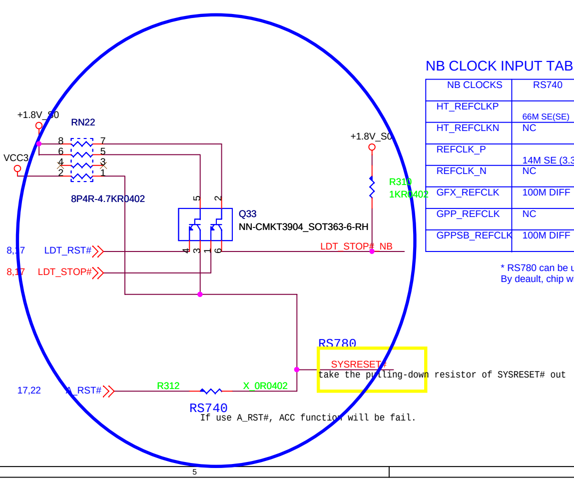
RX740/RS740/RS780 JTAG PIN MAPPING

	RX780	RS740/RS780
TRST	TEST_EN	TEST_EN
TMS(TP220)	PCIE_RST3(TP222)	DDC_DATA(TP223)
TDI	I2C_DATA	I2C_DATA
TCK	I2C_CLK	I2C_CLK
TDO(TP218)	PWM_GPIO6(TP219)	TMDS_HPD(TP221)

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.



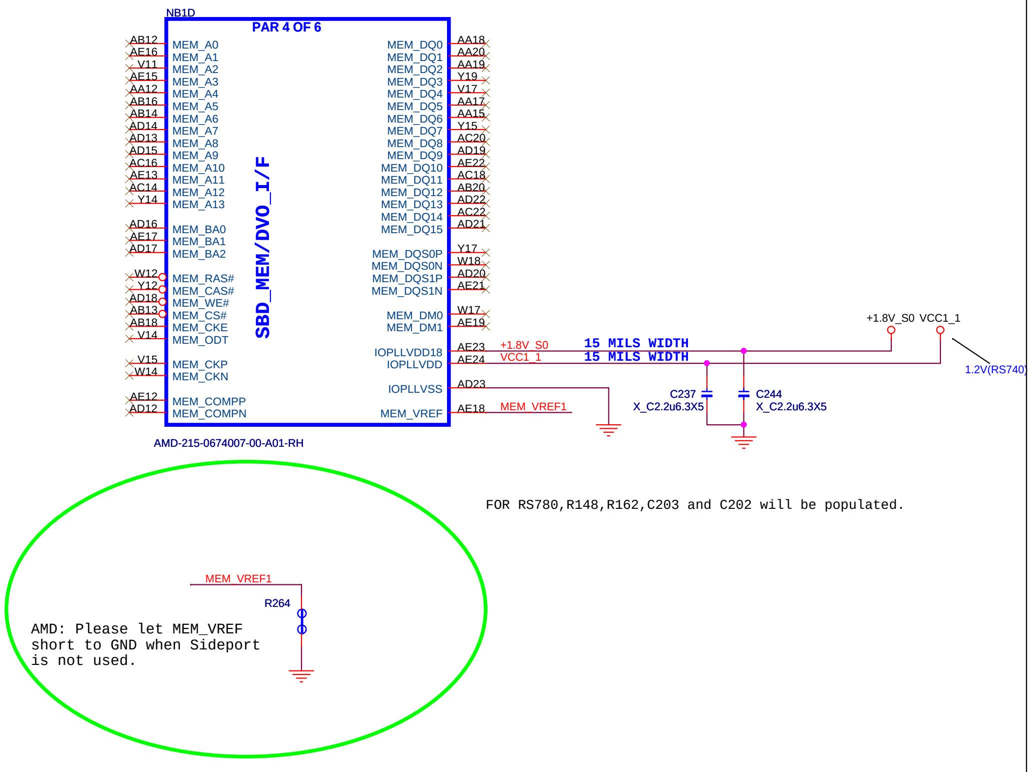
RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

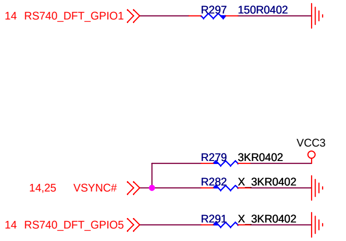
Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS780: pin HSYNC
RX780: Not Appicable



FOR RS780,R148,R162,C203 and C202 will be populated.

RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL,
place close to pin C8



RS740/RX780/RS780: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EEPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1

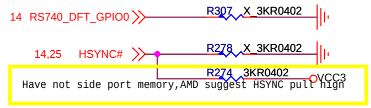
RS780: pin SUS_STAT#

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5

RS780: pin VSYNC

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE



Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC

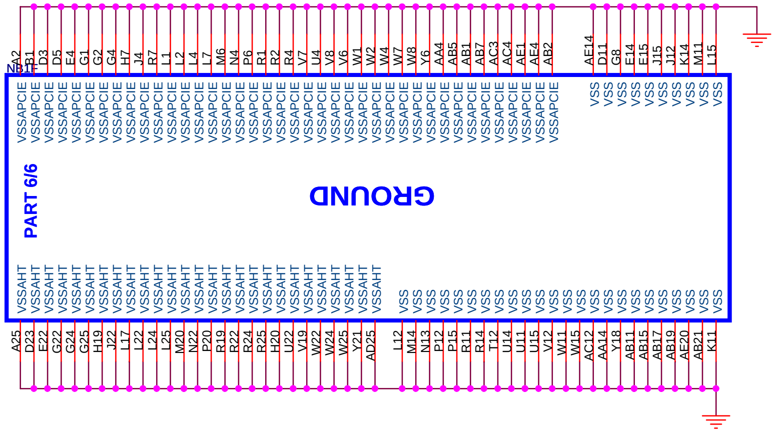
RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

Enables Test debug bus
using PCIE bus
1. Disable (can be enabled
thru nbcfg register)
0 : Enable

RS780: configurable thru register
setting only
RS740: Not supported

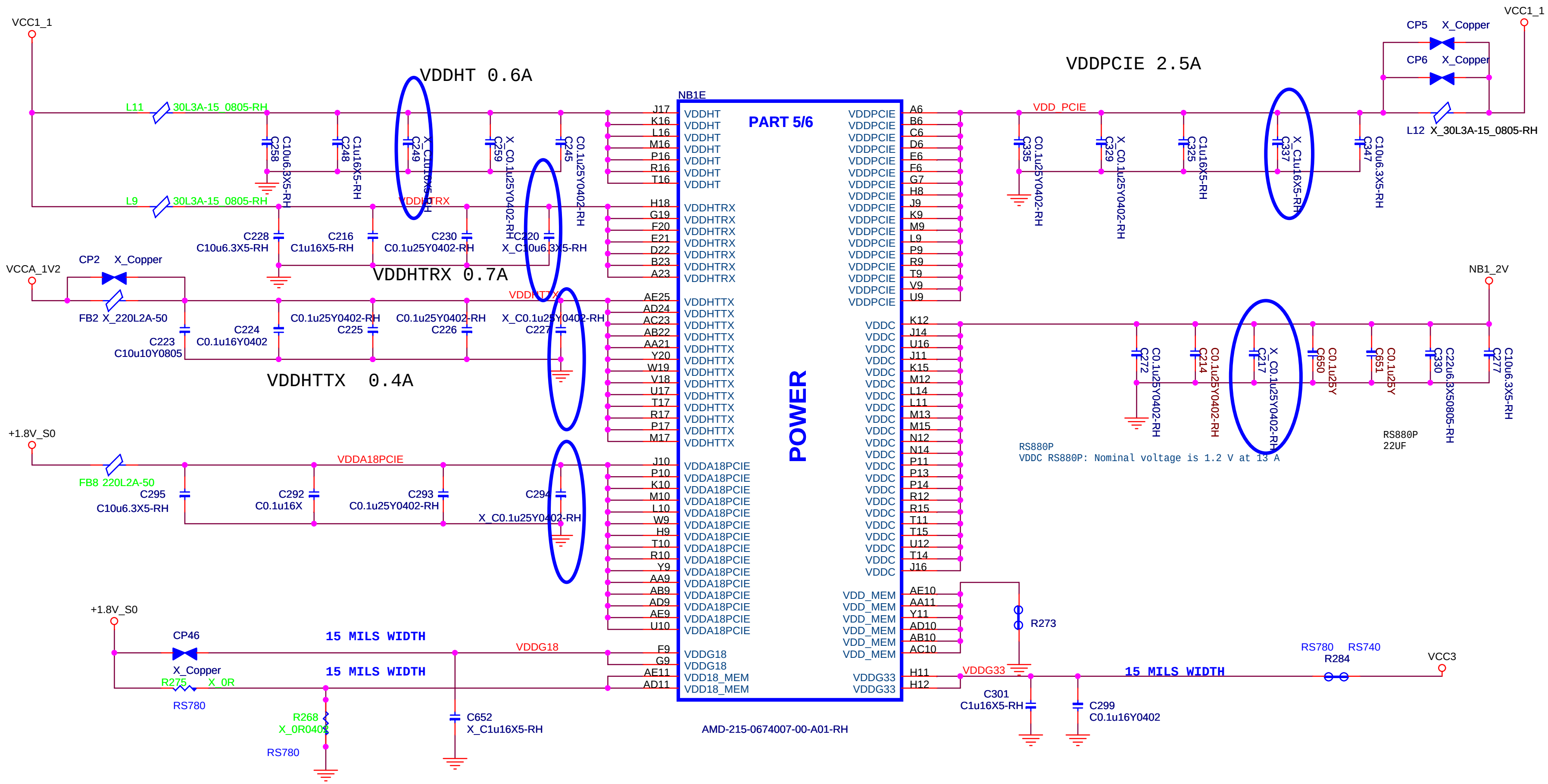
MSI MICRO-START INT'L CO.,LTD.

Title	16 760G&785G&880G-SPMEM/STRAPS	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Tuesday, July 26, 2011	Sheet 15 of 36	



RS740/RX780/RS780 POWER DIFFERENCE TABLE

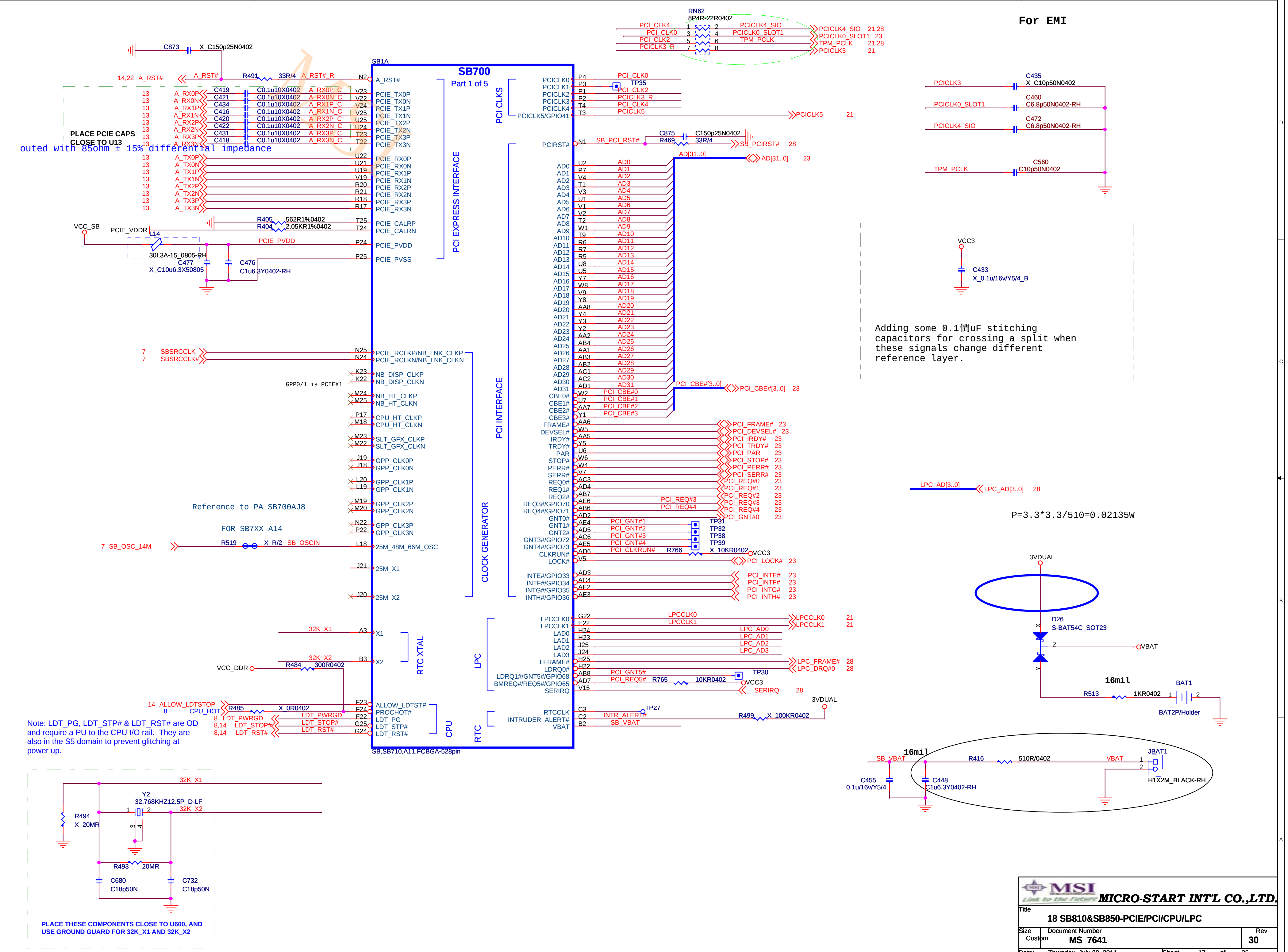
PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



VDD18_MEM
RS780 without Side-Port/RX781/RS780C/RS780L/RS780MC:
Connected to GND plane (preferred) or connected to 1.8V_S0 power rail.

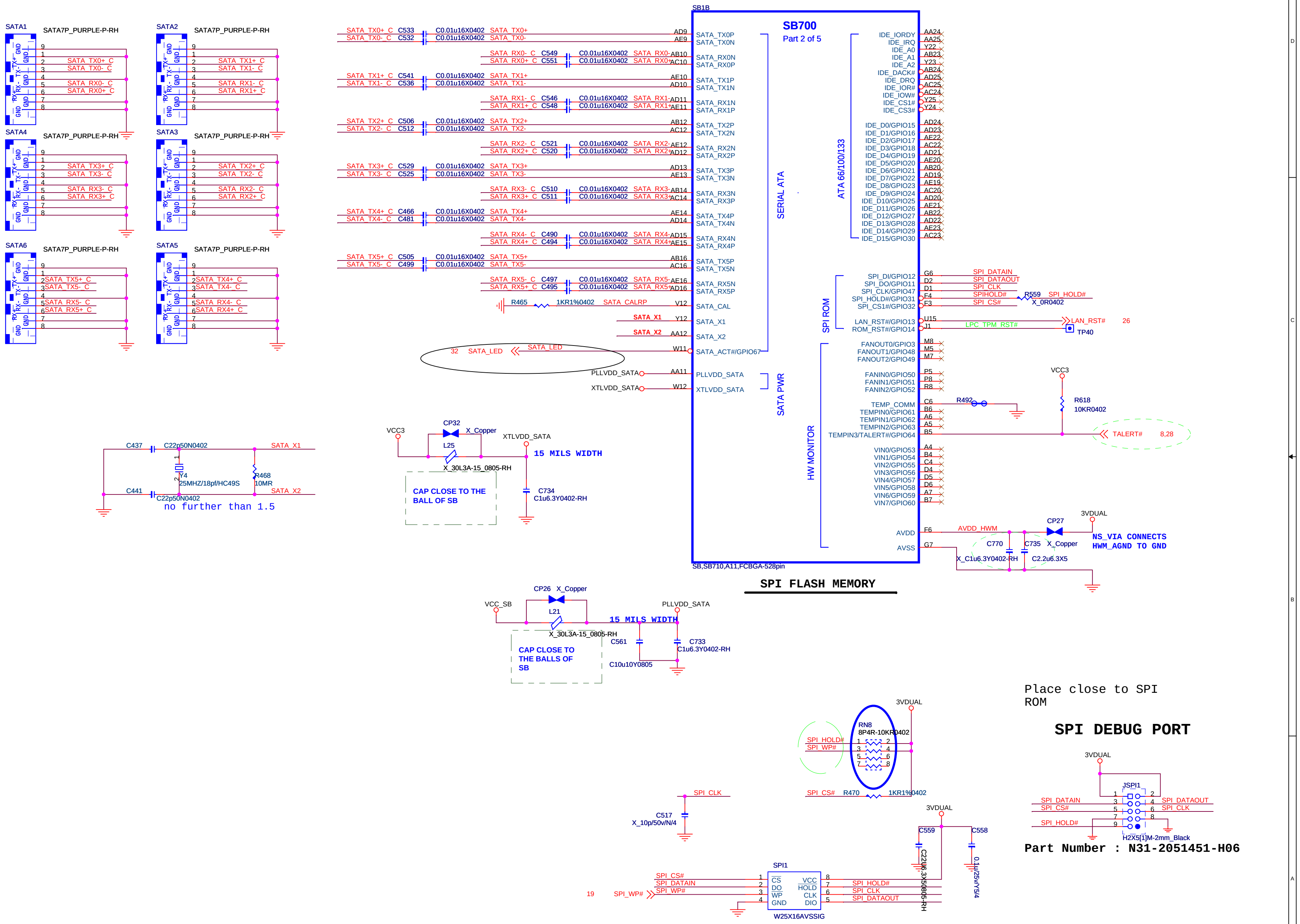
MSI Link to the Future **MICRO-START INT'L CO.,LTD.**

Title	17 760G&785G&880G-POWER		
Size: Custom	Document Number: MS_7641		Rev: 30
Date: Tuesday, August 02, 2011	Sheet 16 of 36		



MSI MICRO-STAR INT'L CO.,LTD.

Title	18 SB810&SB850-PCIE/PCI/CPU/LPC	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Thursday, July 28, 2011	Sheet 17 of 36	



SPI ROM change to M31-25Q8003-W03

SB8X0 Pin USBCLK input ,or14M_25M_48M_OSC ouput
Function set output pin by BIOS.

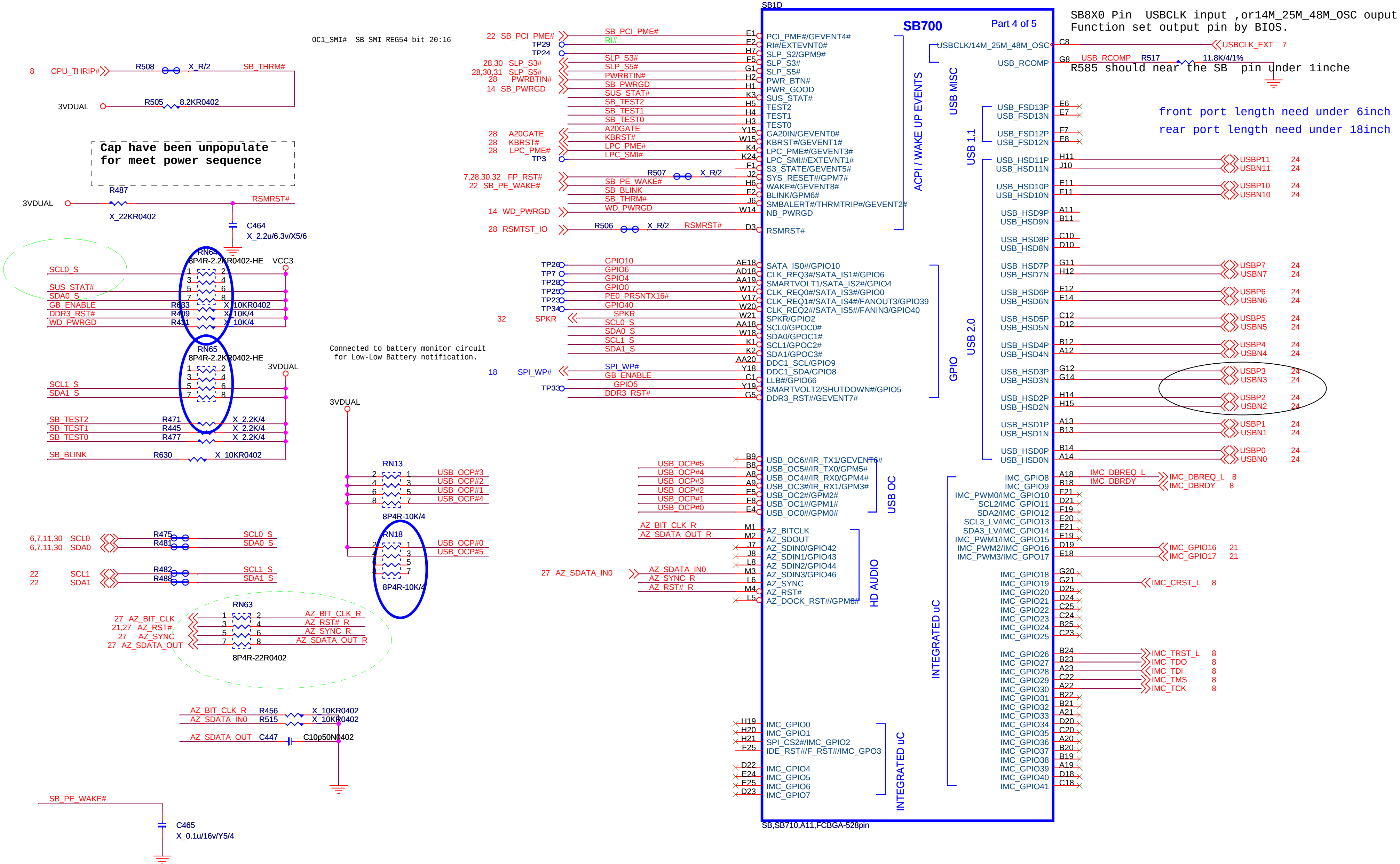
R585 should near the SB pin under 1inche

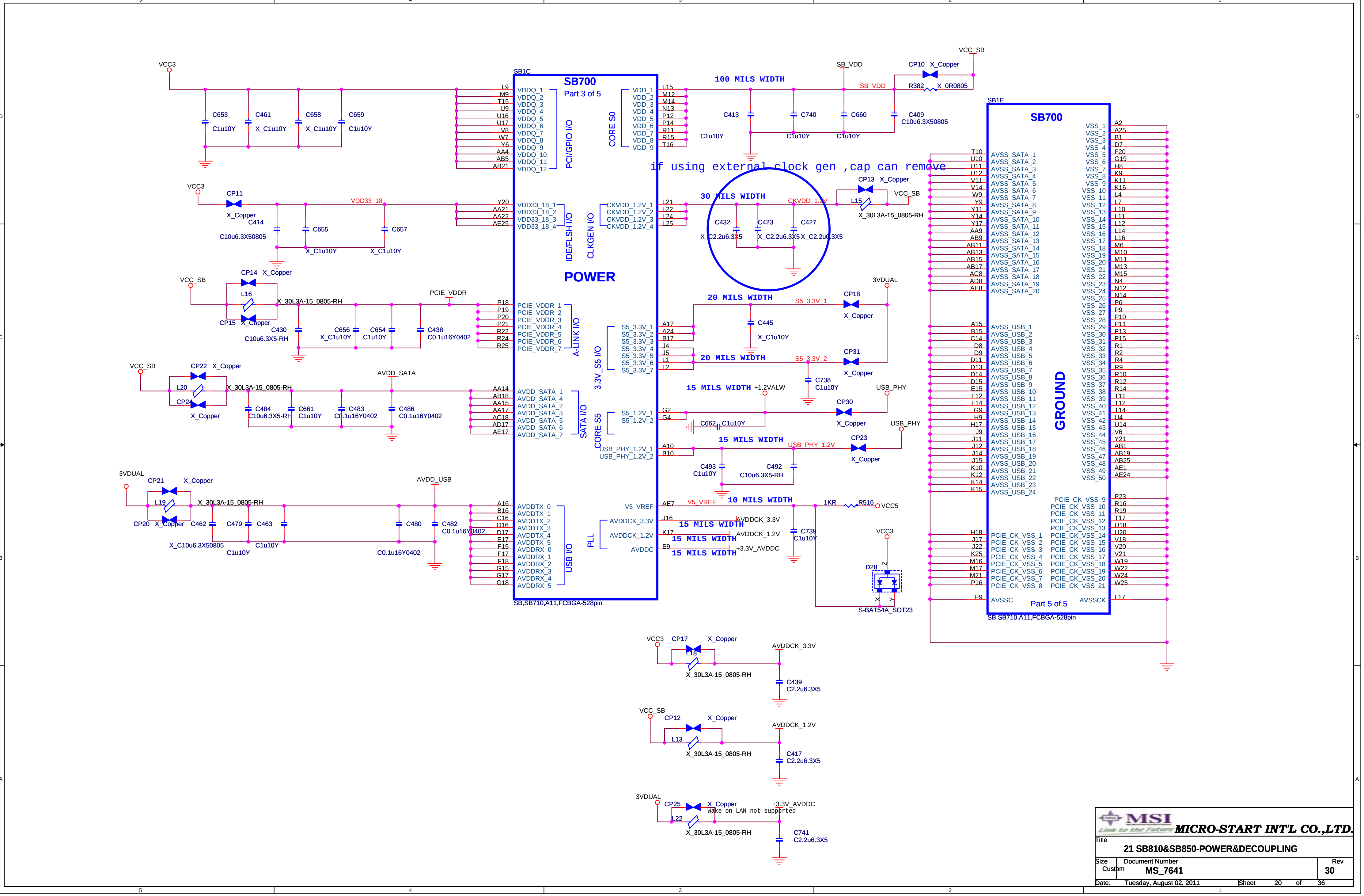
front port length need under 6inch
rear port length need under 18inch

Cap have been unpopulate
for meet power sequence

OC1_SMI# SB SMI REG54 bit 20:16

Connected to battery monitor circuit
for Low-Low Battery notification.





MICRO-START INT'L CO.,LTD.

Title: 21 SB810&SB850-POWER&DECOUPLING

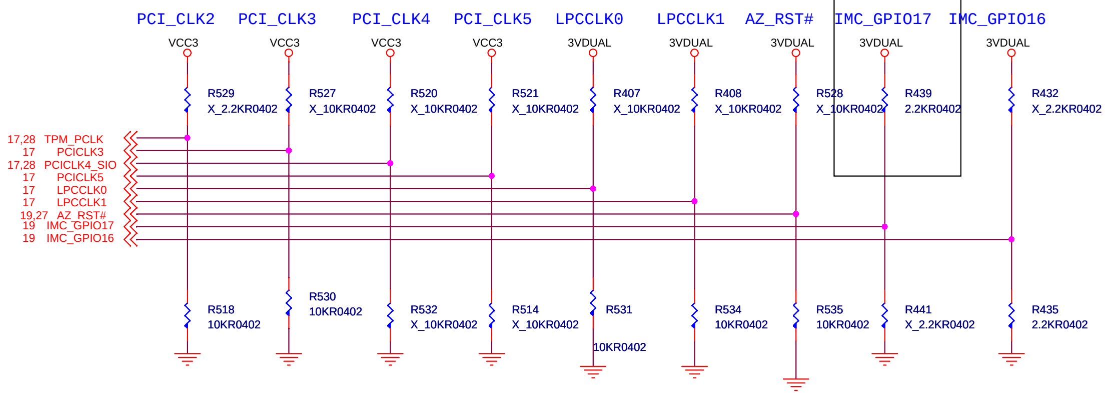
Size	Document Number	Rev
Custom	MS_7641	30

Date: Tuesday, August 02, 2011 Sheet 20 of 36

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

Note: SB700/SB750 A12 IMC_GPO[17:16] require external pull-up/pull-down resistors to configure ROM straps. However, SB710/SB750 A14 IMC_GPO[17:16] require only external pull-down resistors to configure ROM straps.



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved; H, L = SPI ROM DEFAULT; L, H = LPC ROM; L, L = FWH ROM	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT		

DEBUG STRAPS

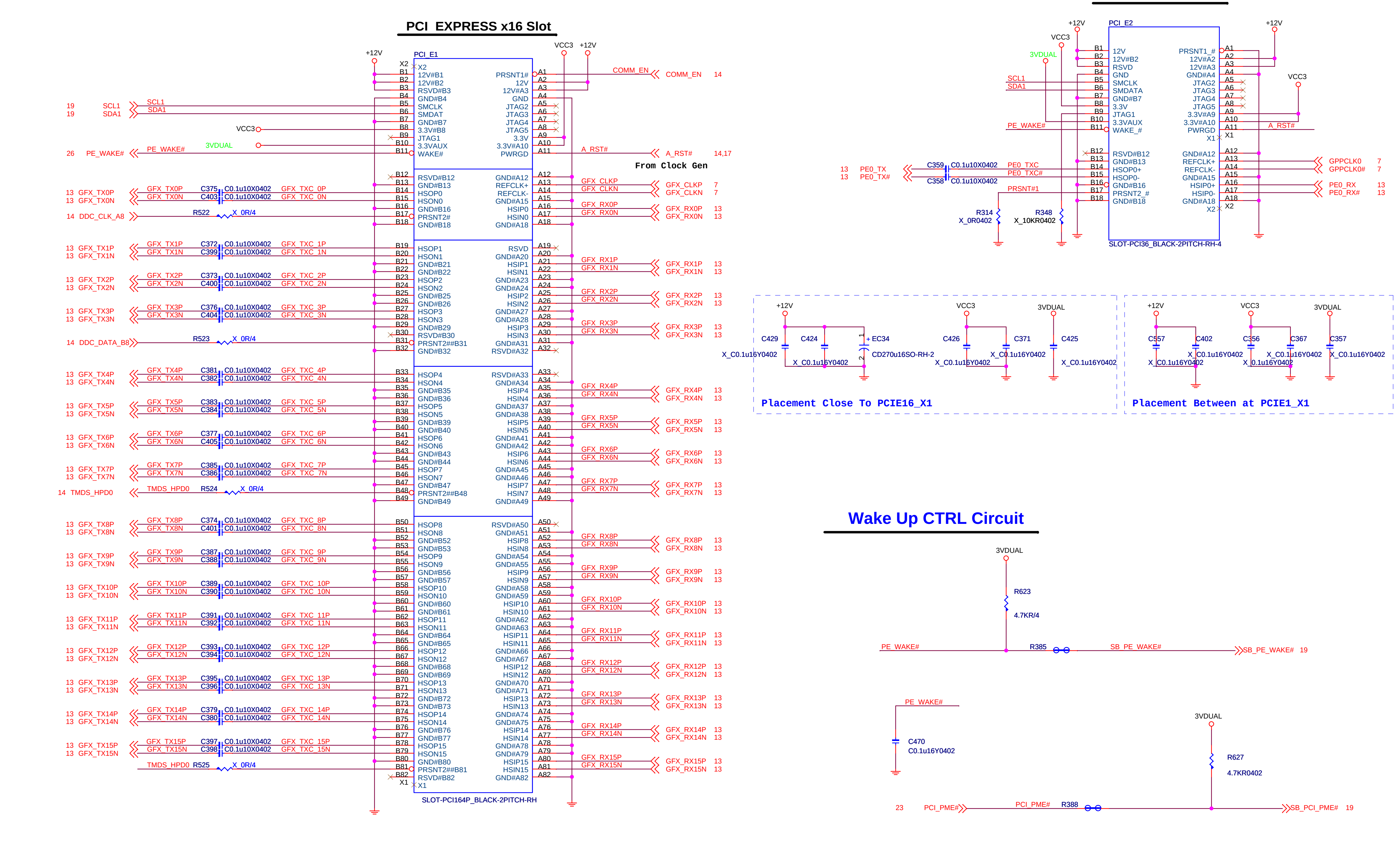
SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

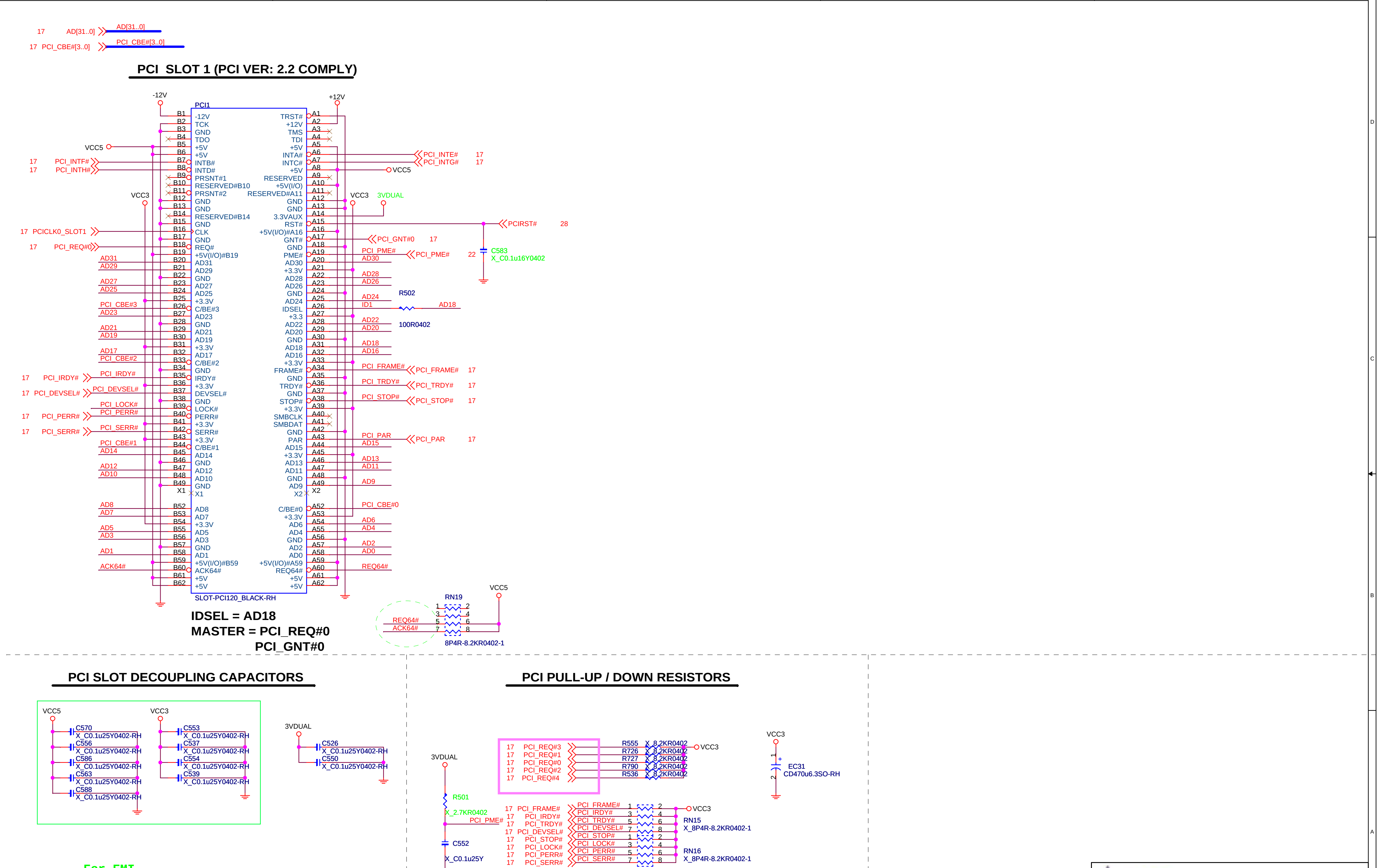
MICRO-START INT'L CO.,LTD.

Title	22 SB810&SB850-STRAPS		
Size: Custom	Document Number: MS_7641		Rev: 30
Date: Wednesday, July 27, 2011	Sheet 21 of 36		

PCI Express Slot x16/x1



MSI MICRO-START INT'L CO.,LTD.		
Title	23 PCI EXPRESS X16 & X 1 SLOT	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Tuesday, July 26, 2011	Sheet 22 of 36	

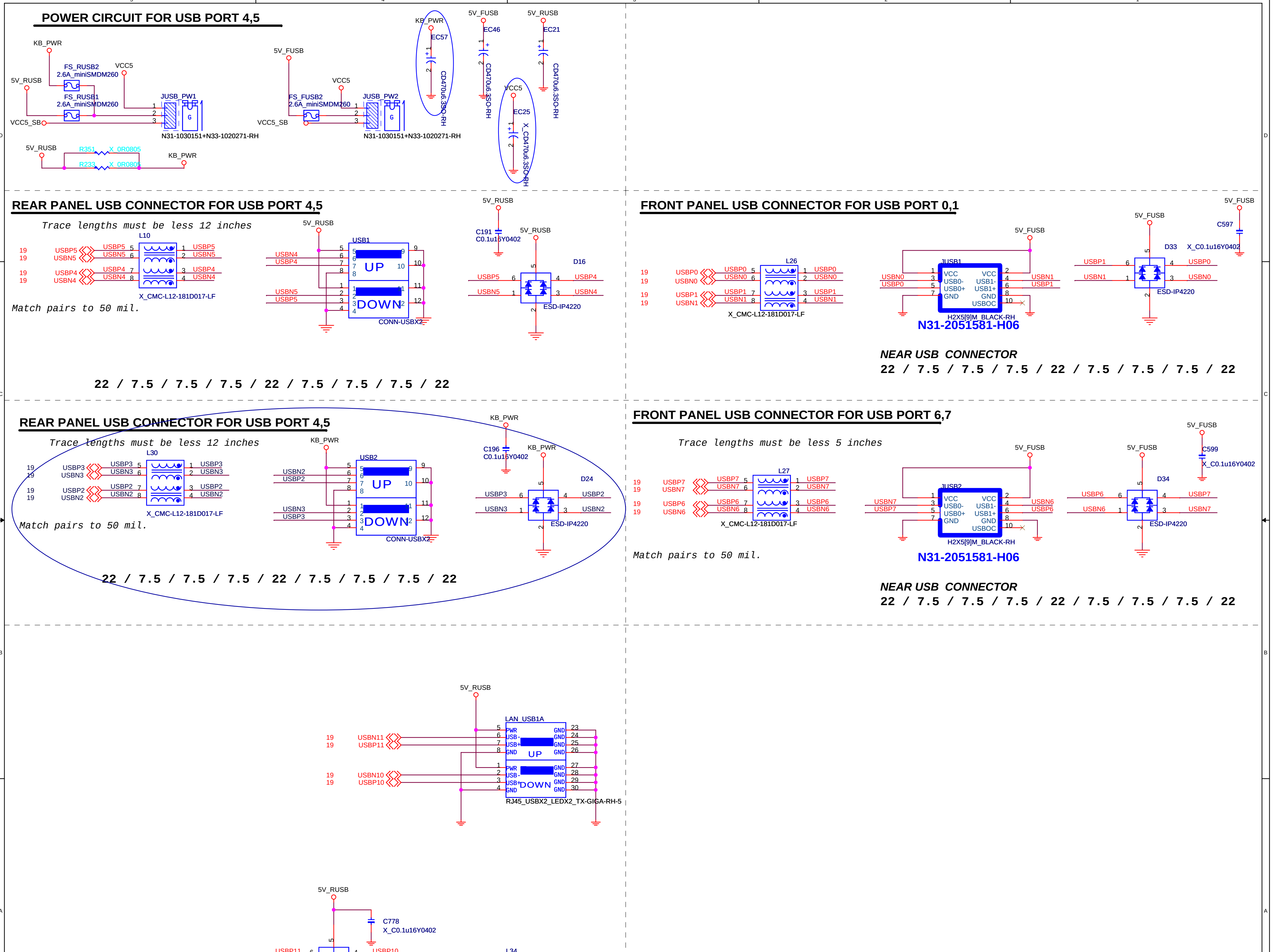


MICRO-START INT'L CO.,LTD.

Title: 24 PCI Slot 1 & PCIE X 1 SLOT

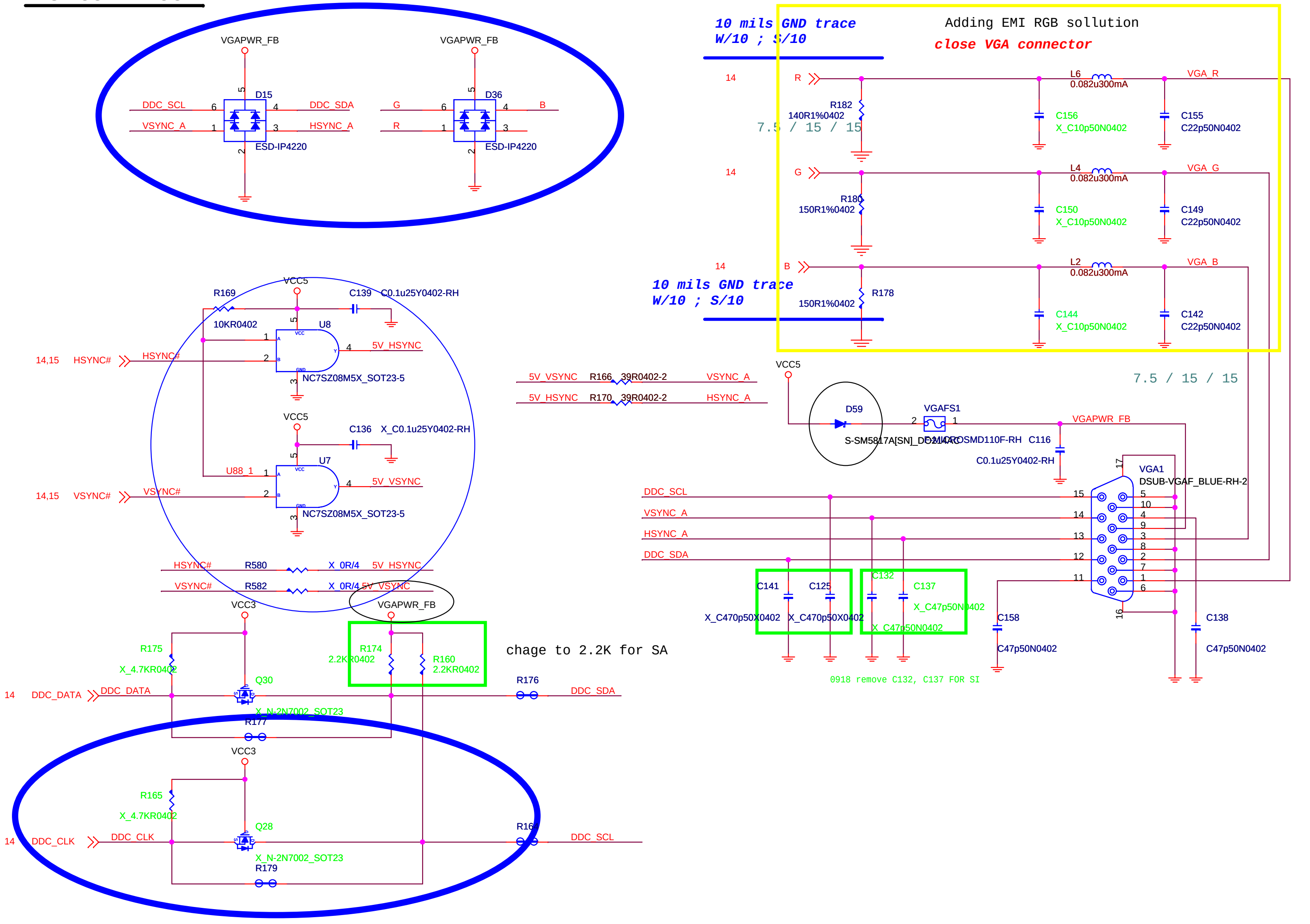
Size	Document Number	Rev
Custom	MS_7641	30

Date: Friday, July 29, 2011 Sheet 23 of 36



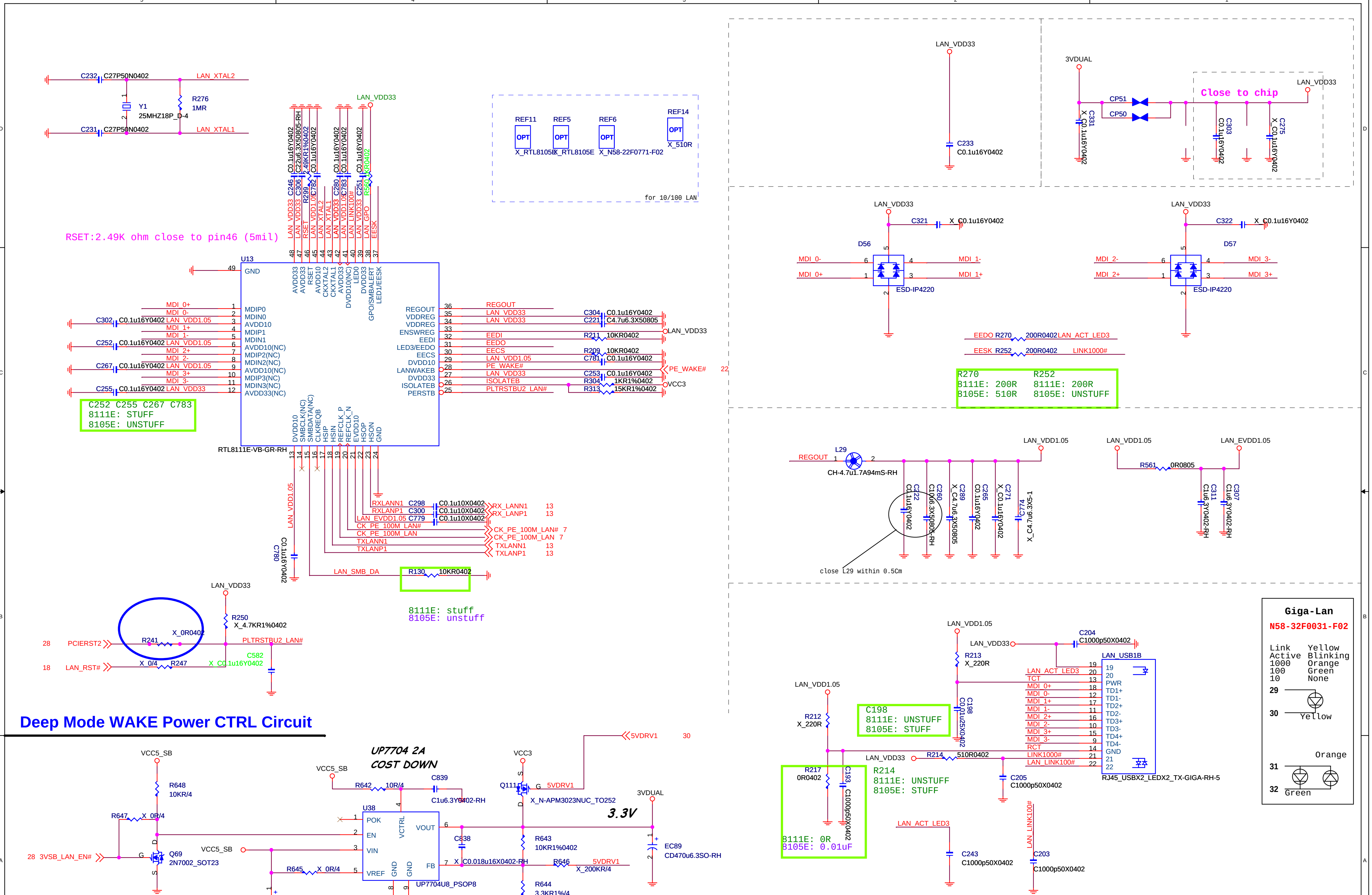
MSI	MICRO-START INT'L CO.,LTD.
Title	25 USB connectors
Size: Custom	Document Number: MS_7641 — Rev 30
Date: Tuesday, July 26, 2011	Sheet 24 of 36

VGA CONN BLOCK



MICRO-START INT'L CO.,LTD.

Title	26 VGA&HDMI&DVI CONN	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Monday, August 01, 2011	Sheet 25 of 36	

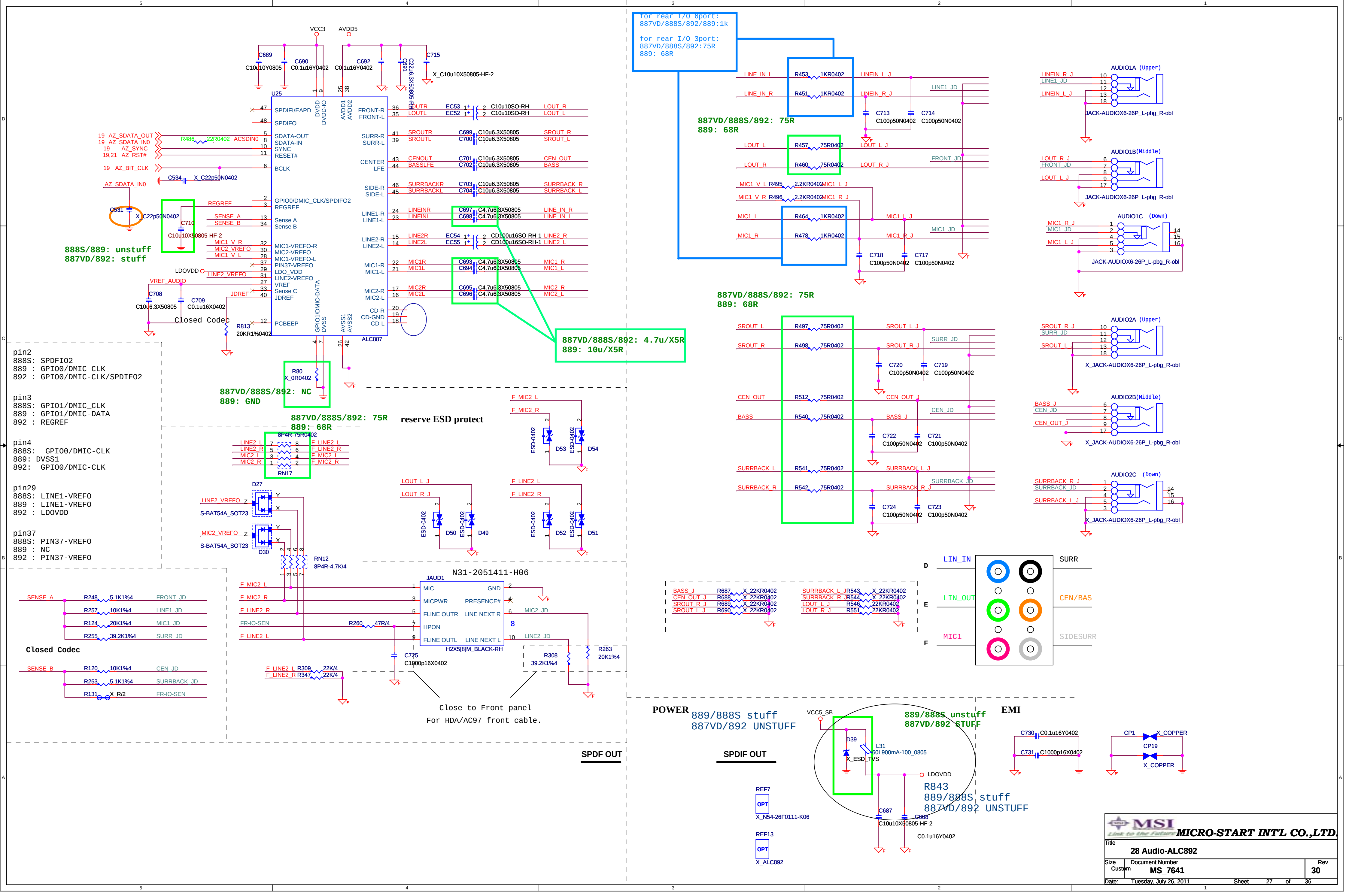


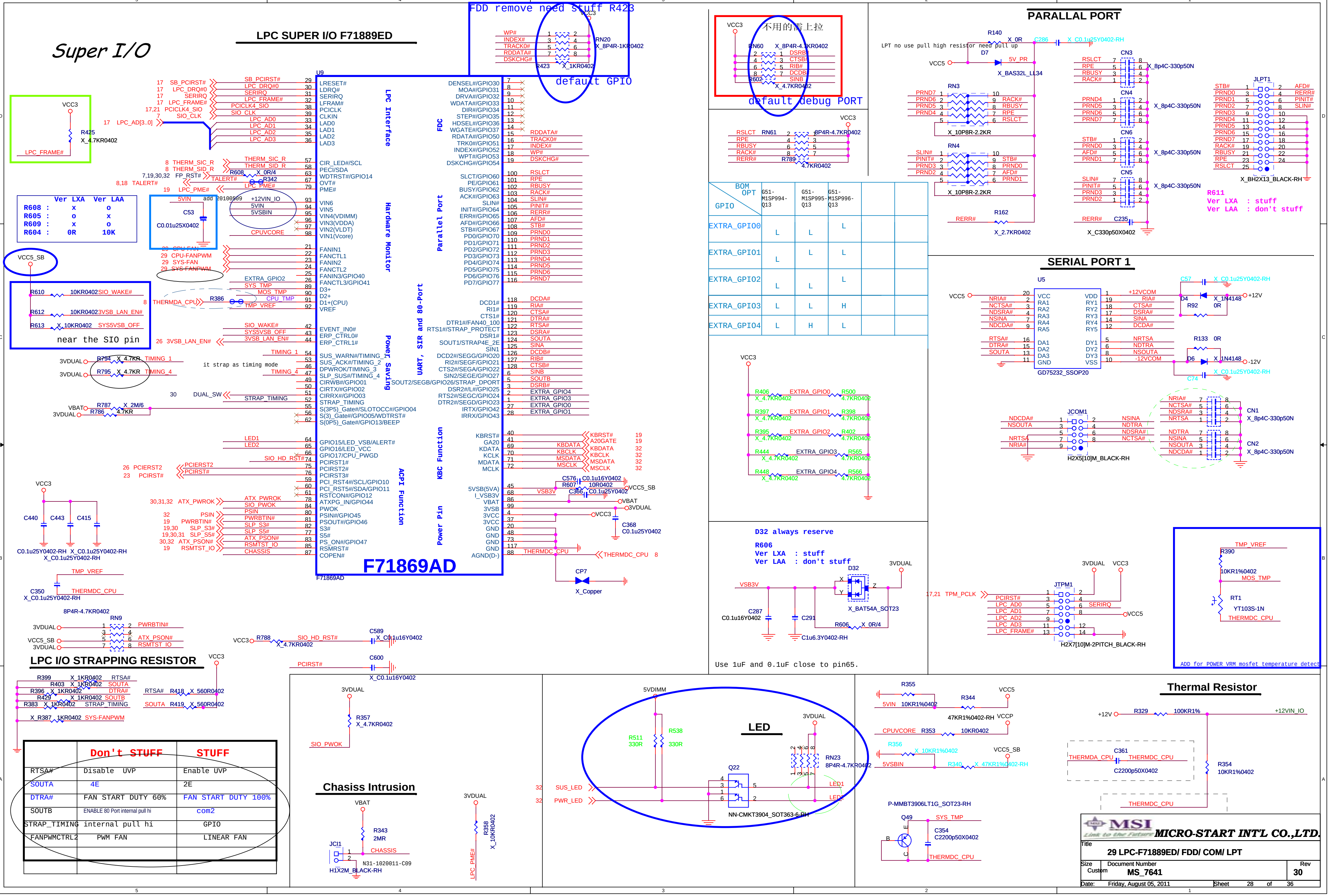
MICRO-START INT'L CO.,LTD.

Title: 27 LAN RTL8111DL/RTL8103EL

Size	Document Number	Rev
Custom	MS_7641	30

Date: Tuesday, July 26, 2011 Sheet 26 of 36


for rear I/O 6port:
887VD/888S/892/889:1k
for rear I/O 3port:
887VD/888S/892:75R
889: 68R
887VD/888S/892: 75R
889: 68R
888S/889: unstuff
887VD/892: stuff
Closed Codec
887VD/888S/892: 4.7u/X5R
889: 10u/X5R
887VD/888S/892: NC
889: GND
887VD/888S/892: 75R
889: 68R
reserve ESD protect
pin2
888S: SPDFIO2
889 : GPIO0/DMIC-CLK
892 : GPIO0/DMIC-CLK/SPDIFO2
pin3
888S: GPIO1/DMIC_CLK
889 : GPIO1/DMIC-DATA
892 : REGREF
pin4
888S: GPIO0/DMIC-CLK
889: DVSS1
892: GPIO0/DMIC-CLK
pin29
888S: LINE1-VREFO
889 : LINE1-VREFO
892 : LDOVDD
pin37
888S: PIN37-VREFO
889 : NC
892 : PIN37-VREFO
Closed Codec
N31-2051411-H06
Close to Front panel
For HDA/AC97 front cable.
SPDF OUT
POWER
889/888S stuff
887VD/892 UNSTUFF
SPDIF OUT
889/888S unstuff
887VD/892 STUFF
R843
889/888S stuff
887VD/892 UNSTUFF
EMI
LIN_IN
SURR
LIN_OUT
CEN/BAS
MIC1
SIDESURR
MICRO-START INT'L CO.,LTD.
Title
28 Audio-ALC892
Size Custom
Document Number MS_7641
Rev 30
Date: Tuesday, July 26, 2011
Sheet 27 of 36



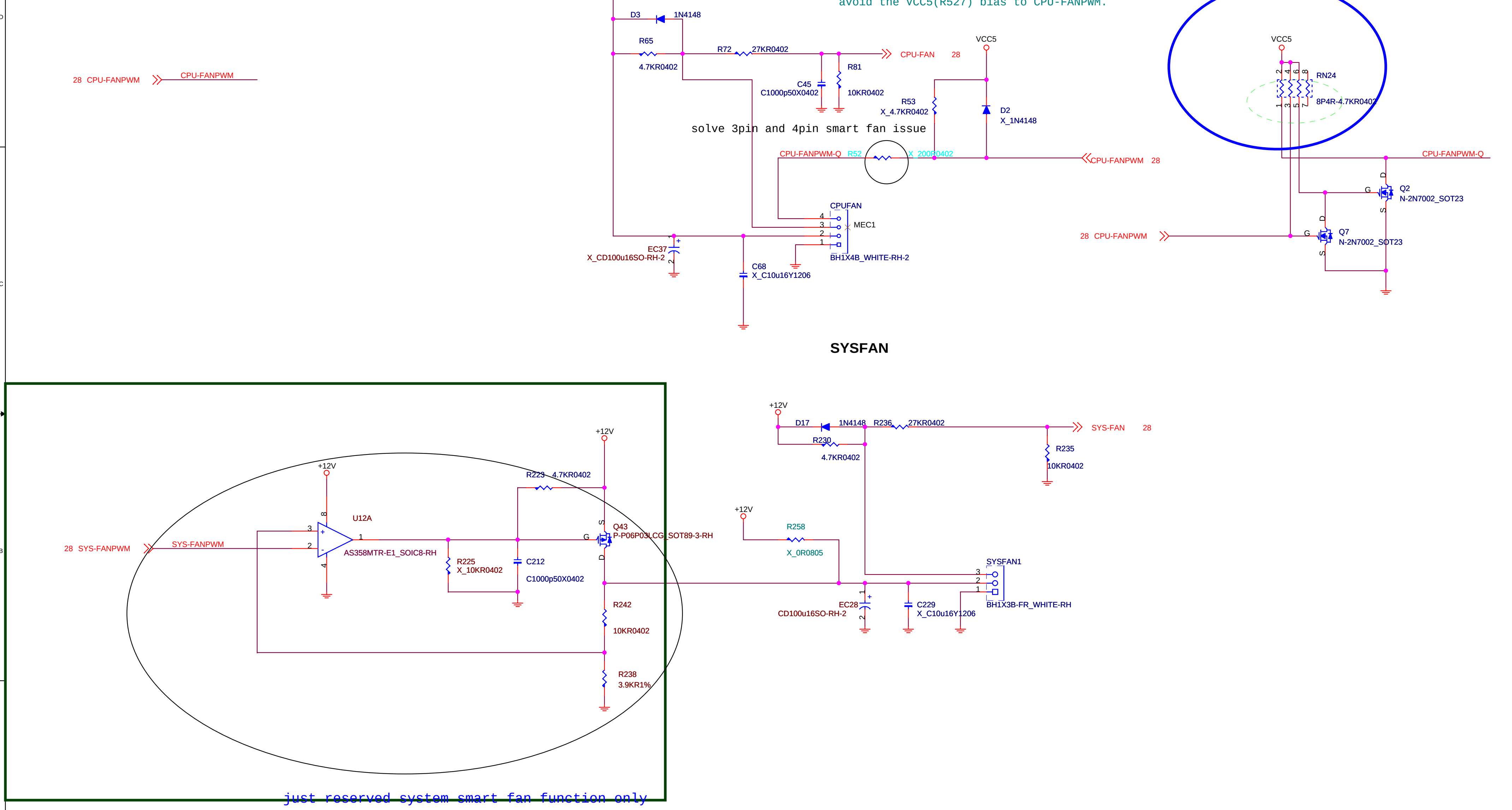
BOM OPT / GPIO	G51-M1SP994-Q13	G51-M1SP995-Q13	G51-M1SP996-Q13		
EXTRA_GPIO0	L	L	L		
EXTRA_GPIO1	L	L	L		
EXTRA_GPIO2	L	L	L		
EXTRA_GPIO3	L	L	H		
EXTRA_GPIO4	L	H	L		

	Don't STUFF	STUFF
RTSA#	Disable UVP	Enable UVP
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
SOUTB	ENABLE 80 Port internal pull hi	com2
STRAP_TIMING	internal pull hi	GPIO
FANPWMCTRL2	PWM FAN	LINEAR FAN

MSI MICRO-START INT'L CO.,LTD.

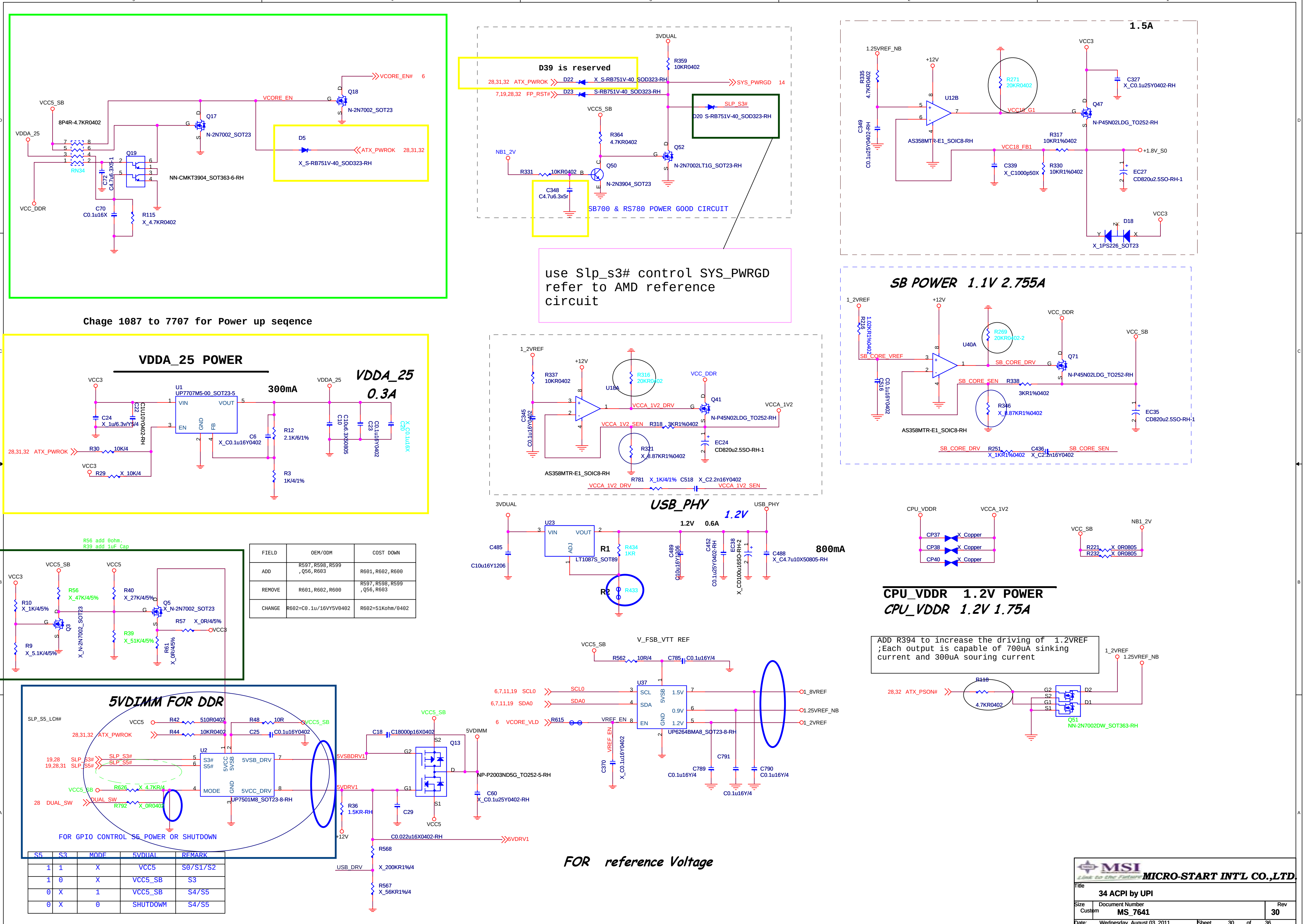
Title	29 LPC-F71889ED/ FDD/ COM/ LPT	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Friday, August 05, 2011	Sheet 28 of 36	

FAN CONTROL



MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title: 30 FAN		
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Friday, July 29, 2011	Sheet 29 of 36	

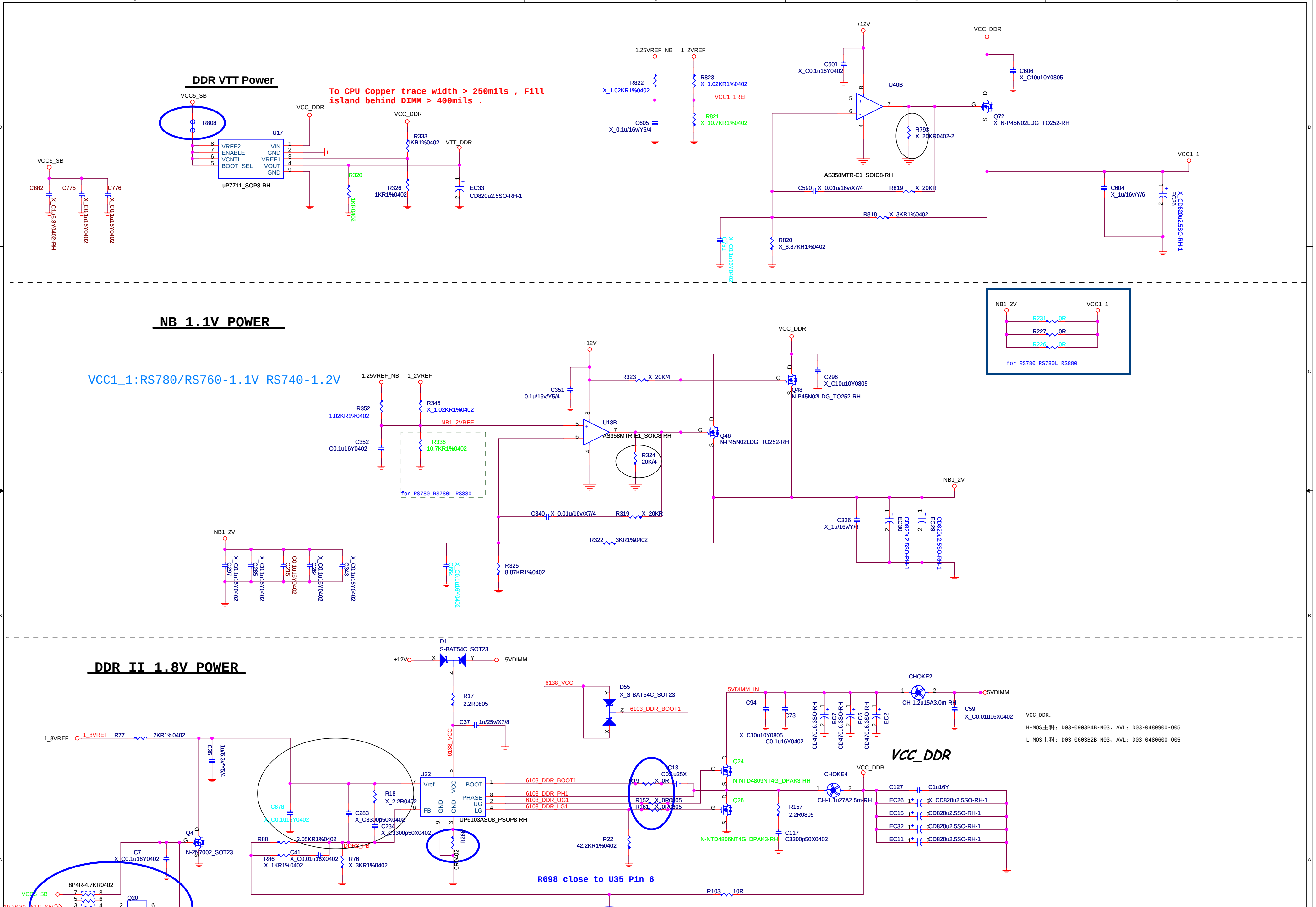


FIELD	OEM/ODM	COST DOWN
ADD	R597,R598,R599 ,Q56,R603	R601,R602,R600
REMOVE	R601,R602,R600	R597,R598,R599 ,Q56,R603
CHANGE	R602=C0.1u/16VY5V0402	R602=51Kohm/0402

S5	S3	MODE	5VDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWM	S4/S5

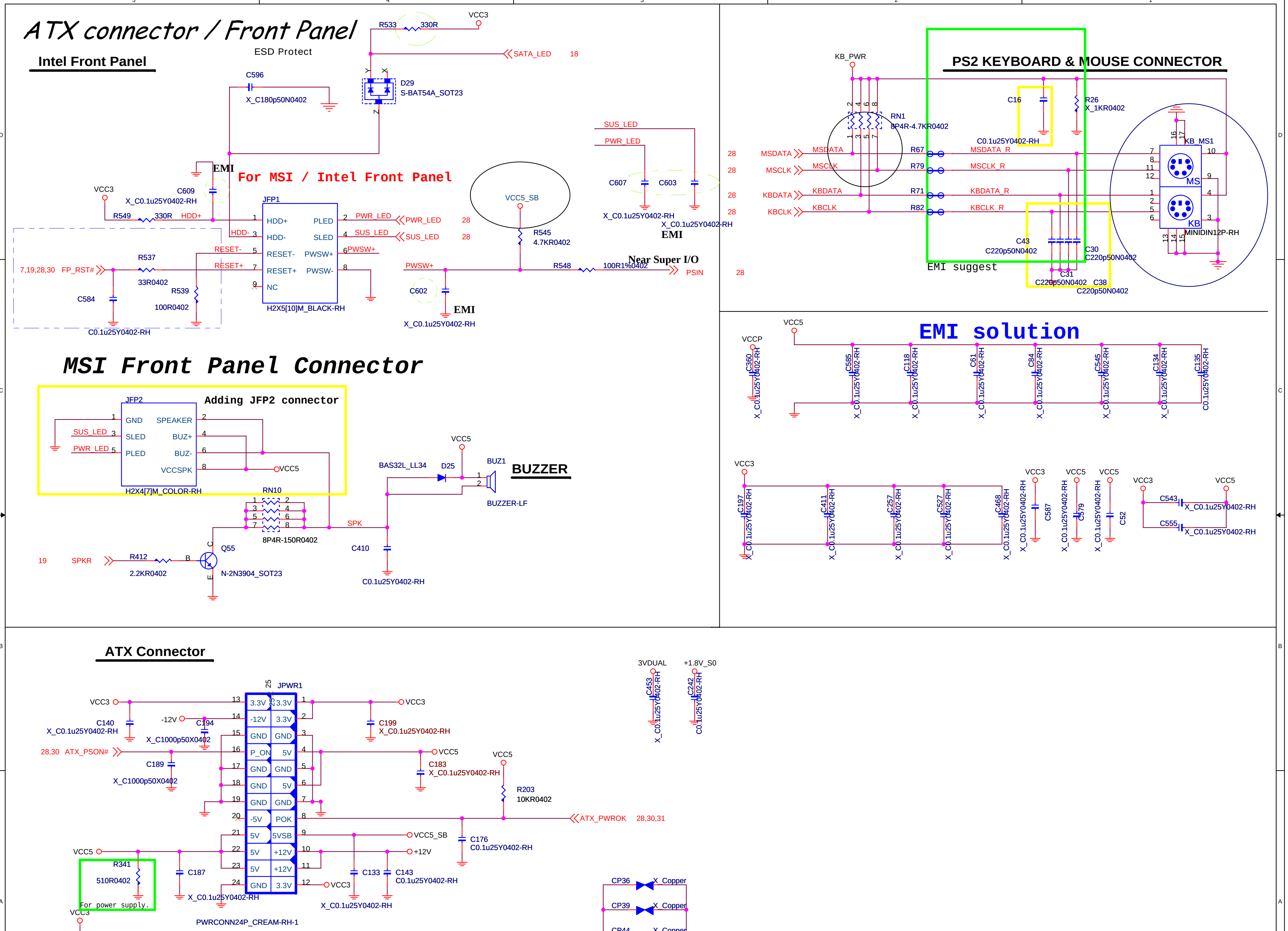
MSI MICRO-START INT'L CO.,LTD.

Title	34 ACPI by UPI	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Wednesday, August 03, 2011	Sheet 30 of 36	



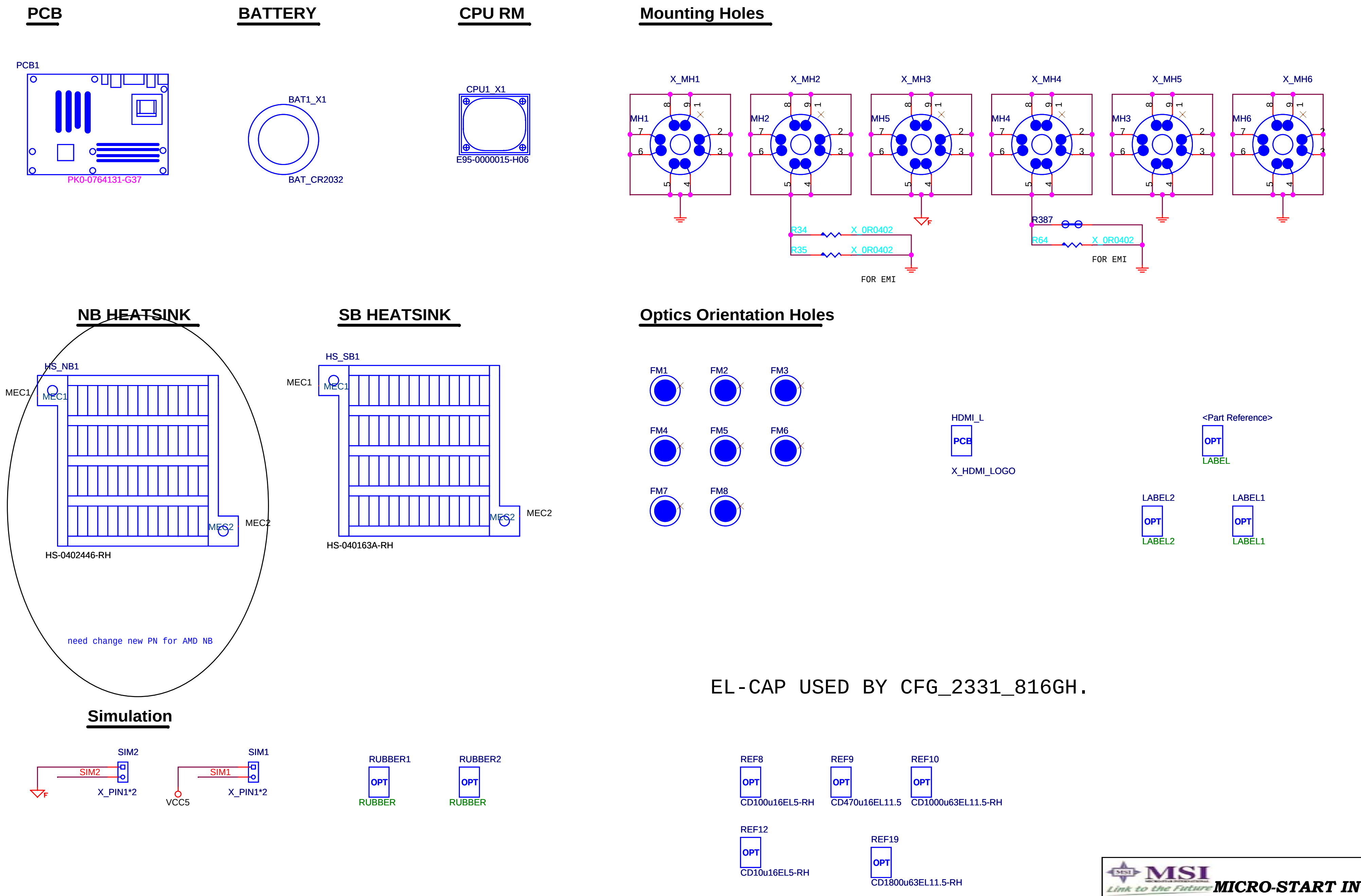
MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

Title	35 VCC_DDR&VCC1_1 NB	
Size C	Document Number MS_7641	Rev 30
Date: Tuesday, August 02, 2011	Sheet 31 of 36	



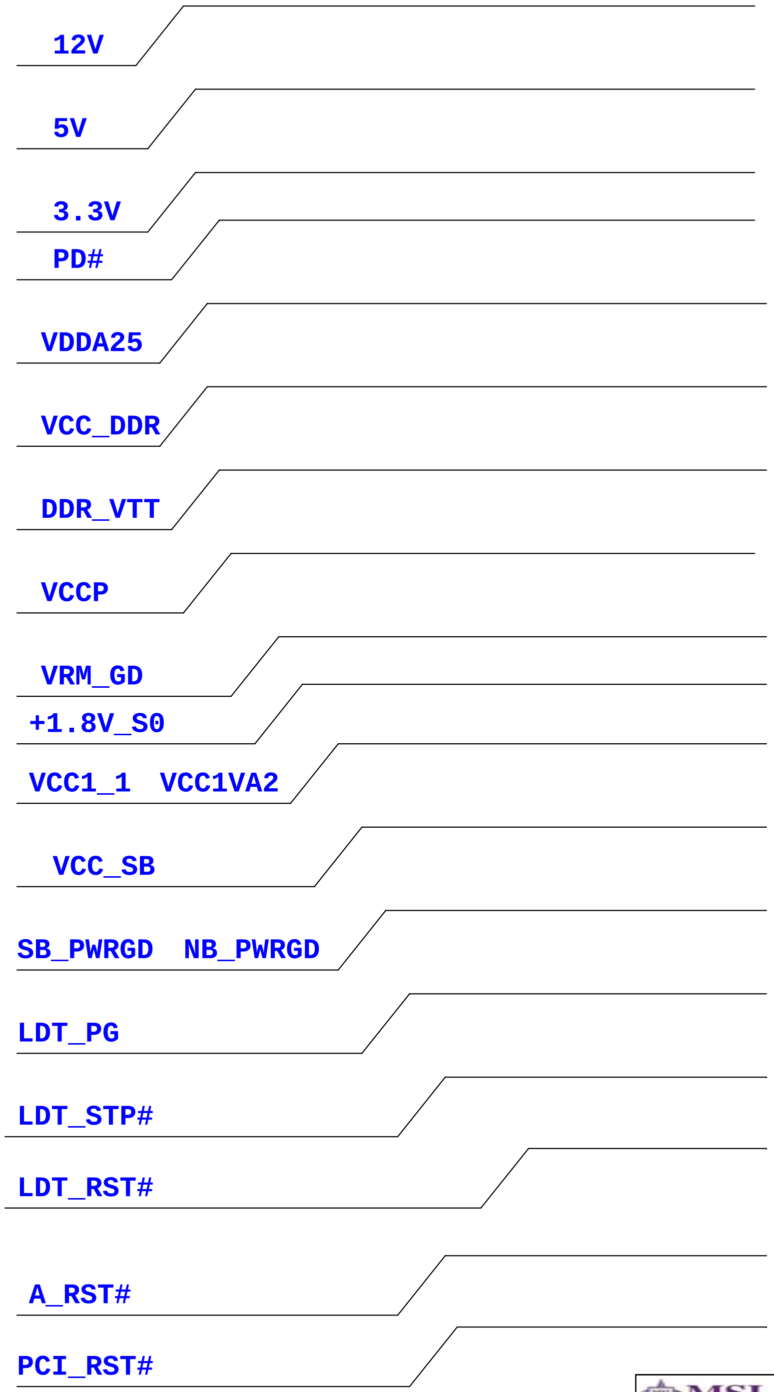
MSI Link to the Future MICRO-START INT'L CO.,LTD.

Title	36 ATX/Front Panel/KB/EMI	
Size Custom	Document Number MS_7641	Rev 30
Date: Tuesday, August 02, 2011	Sheet 32 of 36	



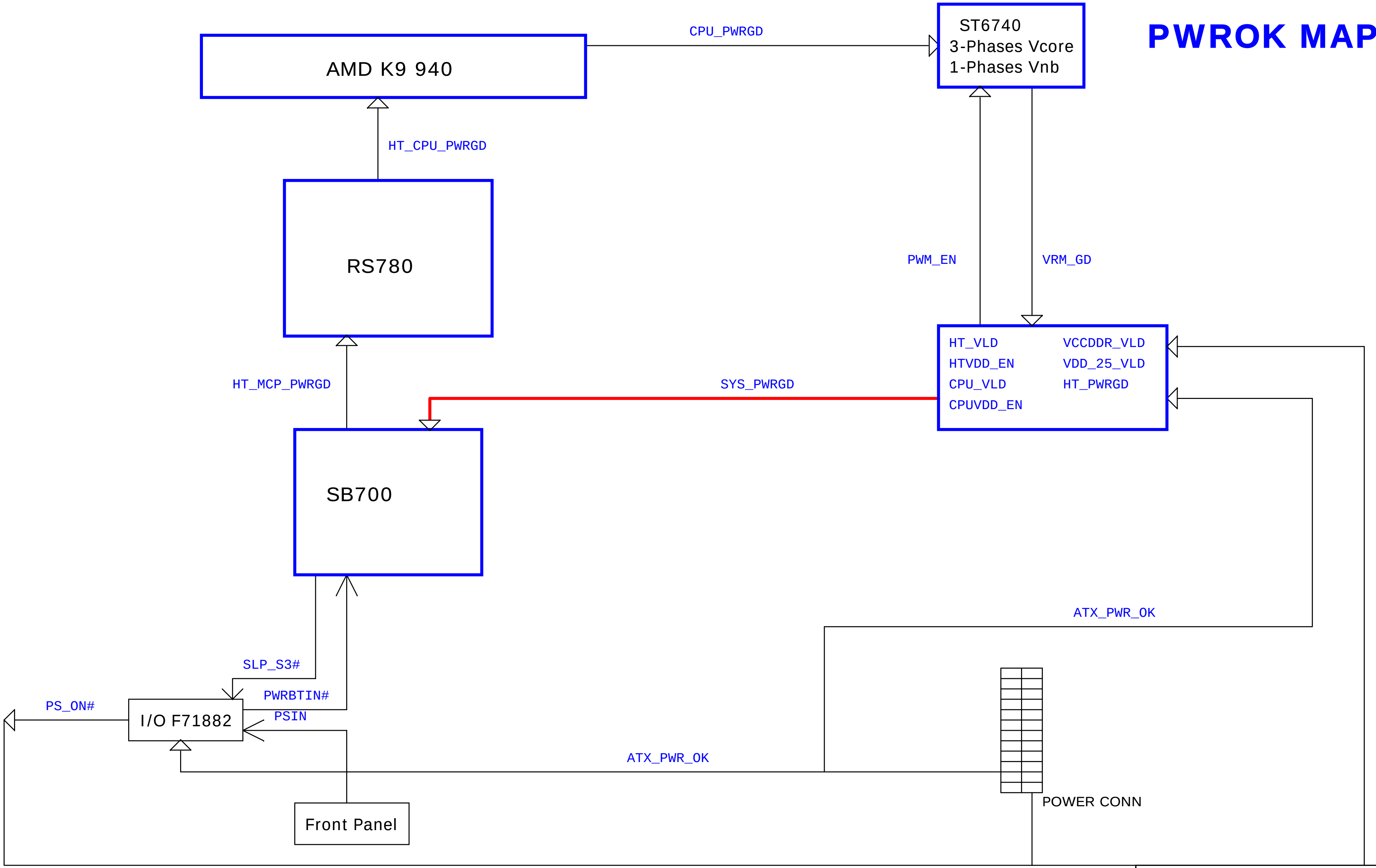
MICRO-START INT'L CO.,LTD.

Title	37 Mannual parts for BOM	
Size Custom	Document Number MS_7641	Rev 30
Date: Friday, August 05, 2011	Sheet 33 of 36	



MSI Link to the Future **MICRO-START INT'L CO.,LTD.**		
Title: **38 POS MAP**		
Size: Custom	Document Number: **MS_7641**	Rev: **30**
Date: Monday, July 25, 2011	Sheet 34 of 36	

PWROK MAP



MICRO-START INT'L CO.,LTD.

Title	39 Power OK MAP	
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Monday, July 25, 2011	Sheet 35 of 36	

MS-7641-0A

Base on 7623-4.1 change as follow:

remove MARVELL ,USB3.0 ,1394,2DIMM,OC switch
change ps2 to ps2+usb port
change lan connector to LAN+USB2.0 connector
remove print port pin header FDD
change vrm to 3 phase and add mosfet temperature detect circuit
change 1394+USB connector to usb connector

MS-7641-30

Base on 7641.10 change as follow:

P6 change vrm intsil6323 to upI1601

P24 add usb2

P25 remove HDMI

P27 remove jcd1

P28 Change sio F71869ED to F71869AD

P32 change ps2+usb port to ps2

P25 CHANGE VGA DVI POWER SOURCE
P8 ADD R245

P32 CHANGE USB2 NET NAME

P29 ADD EC37

P30 CHANGE 1_2VREF NET NAME

P27 remove r812 r843

P24 remove EC56
P6 REMOVE Q1 R18 R21 R1 C12 R4 LED1
P14 REMOVE Q39 R224 R305

P25 REMOVE Q66 Q65

P28 ADD EXTRA_GPIO3 EXTRA_GPIO4

P25 ADD Q66 Q65
P28 ADD R794 R795
P30 ADD R118
P17 CHANGE JBAT1 3PIN TO 2PIN

P31 REMOVE R244 R222 R38 R315

P31 ADD C283 C234 R18

P29 ADD R121

MSI Link to the Future — MICRO-START INT'L CO.,LTD.		
Title: 40 Modify History		
Size: Custom	Document Number: MS_7641	Rev: 30
Date: Monday, July 25, 2011	Sheet 36 of 36	