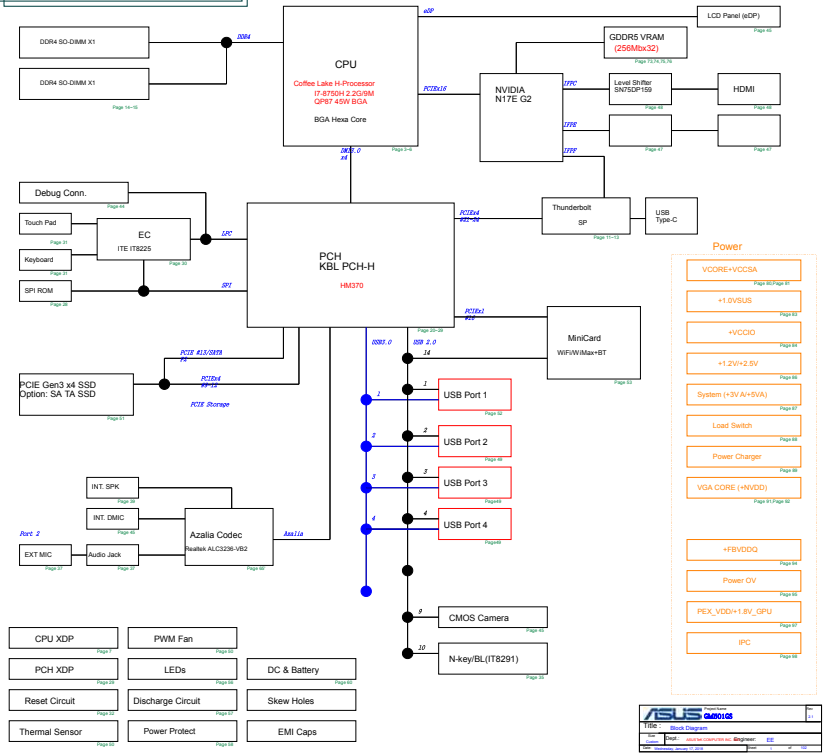
GM501GS Block Diagram

Coffee Lake Platform



ASUSTeK Computer Inc.
Title : Block Diagram
Size: C
Custom
Date: Wednesday, January 17, 2018
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PCH_CPU GPIO

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_A0	RCIN#	Native	RC_IN#		PU 10K	+3VS
GPP_A1	LAD0	Native	LPC_AD0			
GPP_A2	LAD1	Native	LPC_AD1			
GPP_A3	LAD2	Native	LPC_AD2			
GPP_A4	LAD3	Native	LPC_AD3			
GPP_A5	LFRAME#	Native	LPC_FRAME#			
GPP_A6	SERIRQ	Native	INT_SERIRQ		PU 10K	+3VS
GPP_A7	PIRQA#	Native	PCI_INTA#		PU 10K	+3VS
GPP_A8	CLKRUN#	Native	PM_CLKRUN#		PU 8.2K	+3VS
GPP_A9	CLKOUT_LPC0	Native	CLK_KBCPCI_PCH_X1			
GPP_A10	CLKOUT_LPC1	Native	CLK_DEBUG_X1			
GPP_A11	PME#	Native	PCI_PME#			
GPP_A12	GPI	GPI	PCH_GPP_A12			
GPP_A13	SUSWARN#	Native	ME_SusPwrDnAck		PU 10K(@)	+3VSUS
GPP_A14	SUS_STAT#	Native	PCH_SUS_STAT#			
GPP_A15	SUS_ACK#	Native	PM_SUSACK#			
GPP_A16	Native/GPI	GPI	GPP_A16			
GPP_A17	GPI	GPI	(N.C)			
GPP_A18	GPI	GPI	(N.C)			
GPP_A19	GPI	GPI	(N.C)			
GPP_A20	GPI	GPI	(N.C)			
GPP_A21	GPI	GPI	(N.C)			
GPP_A22	GPI	GPI	(N.C)			
GPP_A23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_B0	GPO	GPO	(N.C)			
GPP_B1	GPI	GPI	TBT_I2C_INT_PCH			
GPP_B2	GPO	GPO	VRALERT#(TP)			
GPP_B3	GPI	GPI	CIO_PLUG_EVENT			
GPP_B4	GPI	GPI	(N.C)			
GPP_B5	GPI	Native	CLK_REQ0#/CLKREQ0_PEGA#		PU 10K	+3VSUS
GPP_B6	GPI	Native	CLK_REQ1#		PU 10K	+3VSUS
GPP_B7	GPI	Native	CLK_REQ2#/CLKREQ2_WLAN_AC#		PU 10K	+3VSUS
GPP_B8	GPI	Native	CLK_REQ3#		PU 10K	+3VSUS
GPP_B9	GPI	Native	CLK_REQ4#/CLKREQ4_GLAN#		PU 10K	+3VSUS
GPP_B10	GPI	Native	NC		PU 10K	+3VSUS
GPP_B11	GPO	GPO	MPHY_PWREN		PU 10K	+3VSUS
GPP_B12	SLP_S0#	Native	SLP_S0#			
GPP_B13	PLTRST#	Native	PLT_RST#			
GPP_B14	GPO	Strap	PCH_GPPB14	PD		
GPP_B15	GPI	GPI	TBT_HDP_EN_dGPU#		PU 10K	+3VS
GPP_B16	GPI	Native	TP		PU 10K	+3VS
GPP_B17	GPI	Native	TP			
GPP_B18	GPO	Strap	PCH_GPPB18	PD		
GPP_B19	GPI	GPO	PCH_GPPB19/BT_ON_PCH		PD 10K(@)	
GPP_B20	GPI	GPO	PCH_GPPB20/GPUEVENT#_PCH		PU 10K	+3VSUS
GPP_B21	GPI	GPI	PCH_GPPB21/GC6FBEN_PCH		PU 10K(@)	+3VS
GPP_B22	GPO	Strap	PCH_GPPB22	PD		
GPP_B23	GPO	GPO	SML1ALERT#	PD	PU 150K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_C0	SMBCLK	Native	SMB_CLK		PU 2.2K	+3VSUS
GPP_C1	SMBDATA	Native	SMB_SDA		PU 2.2K	+3VSUS
GPP_C2	GPO	Strap	GPP_C2_BT_UART_WAKE_N		PU 4.7K	+3V_NGFF_WLAN
GPP_C3	SML0CLK	Native	SML0_CLK		PU 2.2K	+3VSUS
GPP_C4	SML0DATA	Native	SML0_DAT		PU 2.2K	+3VSUS
GPP_C5	GPO	Strap	PCH_GPPC5	PD		
GPP_C6	GPI	Native	SML1_CLK		PU 2.2K	+3VSUS
GPP_C7	GPI	Native	SML1_DAT		PU 2.2K	+3VSUS
GPP_C8	GPI	GPI	DGPU_PWR_EN#(NC)			
GPP_C9	GPI	GPI	PCH_GPPC9			
GPP_C10	GPI	GPI	PCH_GPPC10			
GPP_C11	GPI	GPI	WLAN_ON#			
GPP_C12	GPI	GPI	DIMM_SEL0		PD 10K	
GPP_C13	GPI	GPI	DIMM_SEL1		PD 10K	
GPP_C14	GPI	GPI	DIMM_SEL2		PD 10K	
GPP_C15	GPI	GPI	NFC_ID		PU 10K	+3VSUS
GPP_C16	GPI	GPO	TBT_I2C_SDA_PCH		PU 10K(@)	+3VSUS
GPP_C17	GPI	GPO	TBT_I2C_SCL_PCH		PU 10K(@)	+3VS
GPP_C18	GPI	Native	I2C1_SDA		PU 2.2K	+3VS
GPP_C19	GPI	Native	I2C1_SCL		PU 2.2K	+3VS
GPP_C20	GPI	GPI	PCH_GPPC20/DGPU_PWROK		PU 10K	+3VS_NV
GPP_C21	GPI	GPO	PCH_GPPC21/GPU_RST#		PD 10K	
GPP_C22	GPI	GPO	+12VS_FAN_FAULT#_10		PD 100K	+3VSUS
GPP_C23	GPI	GPI	CPAD_INT#		PU 10K	+3VS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_D0	GPI	GPI	(N.C)			
GPP_D1	GPI	GPO	(N.C)			
GPP_D2	GPI	GPI	(N.C)			
GPP_D3	GPI	GPI	(N.C)			
GPP_D4	GPI	GPI	(N.C)			
GPP_D5	GPI	GPI	PCH_GPPD5/M.2_BT_PCMFRM_CRF_RST_N			
GPP_D6	GPI	GPI	PCH_GPPD6/M.2_BT_PCMOUT_CLKREQ0			
GPP_D7	GPI	GPO	PCH_GPPD7/M.2_BT_PCMIN			
GPP_D8	GPI	GPI	PCH_GPPD8/M.2_BT_PCMCLK			
GPP_D9	GPI	Strap	(N.C)		PD 10K	
GPP_D10	GPI	Strap	(N.C)		PD 10K	
GPP_D11	GPI	Strap	TOUCHPAD_ID			
GPP_D12	GPI	Strap	TOUCH_PANEL_ID			
GPP_D13	GPI	GPI	PCH_GPP_D13			
GPP_D14	GPI	GPO	(N.C)			
GPP_D15	GPI	GPO	(N.C)			
GPP_D16	GPI	GPI	(N.C)			
GPP_D17	GPI	GPI	SNDW3_CLK			
GPP_D18	GPI	GPI	SNDW3_DATA			
GPP_D19	GPI	GPI	(N.C)			
GPP_D20	GPI	GPI	(N.C)			
GPP_D21	GPI	GPO	(N.C)			
GPP_D22	GPI	GPI	(N.C)			
GPP_D23	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_E0	GPI	GPI	(N.C)			
GPP_E1	GPI	GPI	SATAPCIE_DET1		PU 10K	+3VS
GPP_E2	GPI	GPI	(N.C)			
GPP_E3	GPI	GPI	EXT_SMI#			
GPP_E4	GPI	Native	SATA0_HDD1_DEVSLP			
GPP_E5	GPI	Native	(N.C)			
GPP_E6	GPI	Native	(N.C)			
GPP_E7	GPI	GPI	EXT_SCI#			
GPP_E8	GPI	Native	SATA_LED#		PU 10K(@)	+3VS
GPP_E9	GPI	Native	USB_OC#0	PD	PU 10K	+3VSUS
GPP_E10	GPI	Native	USB_OC#1	PD	PU 10K	+3VSUS
GPP_E11	GPI	Native	USB_OC#2	PD	PU 10K	+3VSUS
GPP_E12	GPI	Native	USB_OC#3	PD	PU 10K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_F0	GPI	GPI	SATAPCIE_DET3		PU 10K	+3VS
GPP_F1	GPI	GPO	SATAPCIE_DET4			
GPP_F2	GPI	GPI	(N.C)			
GPP_F3	GPI	GPI	(N.C)			
GPP_F4	GPI	GPI	(N.C)			
GPP_F5	GPI	Native	(N.C)			
GPP_F6	GPI	Native	(N.C)			
GPP_F7	GPI	GPI	(N.C)			
GPP_F8	GPI	GPI	(N.C)			
GPP_F9	GPI	GPI	(N.C)			
GPP_F10	GPI	GPI	(N.C)			
GPP_F11	GPI	GPI	(N.C)			
GPP_F12	GPI	GPI	(N.C)			
GPP_F13	GPI	GPI	(N.C)			
GPP_F14	GPI	GPI	(N.C)			
GPP_F15	GPI	Native	USB_OC#4		PU 10K	+3VSUS
GPP_F16	GPI	Native	USB_OC#5		PU 10K	+3VSUS
GPP_F17	GPI	Native	USB_OC#6		PU 10K	+3VSUS
GPP_F18	GPI	Native	USB_OC#7		PU 10K	+3VSUS
GPP_F19	GPI	Native	L_VDDEN_PCH_X1		PD 100K	
GPP_F20	GPI	Native	LCD_BACKEN_PCH_X1		PU 100K	+3VS_LCD(@)
GPP_F21	GPI	Native	L_BKLTCTL_PCH_X1		PU 100K	+3VS_LCD
GPP_F22	GPI	GPI	DDPF_CTRLCLK		PU 2.2K	+3VSUS
GPP_F23	GPI	GPI	DDPF_CTRLDATA		PU 2.2K	+3VSUS

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_G0	GPI	GPI	(N.C)			
GPP_G1	GPI	GPO	(N.C)			
GPP_G2	GPI	GPI	(N.C)			
GPP_G3	GPI	GPI	(N.C)			
GPP_G4	GPI	GPI	(N.C)			
GPP_G5	GPI	GPI	(N.C)			
GPP_G6	GPI	GPI	(N.C)			
GPP_G7	GPI	GPI	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_H0	GPI	Native	CLKREQ6_NGFF1#		PU 10K	+3VSUS
GPP_H1	GPI	Native	CLKREQ7_NGFF2#		PU 10K	+3VSUS
GPP_H2	GPI	Native	CLKREQ8_NGFF3#		PU 10K	+3VSUS
GPP_H3	GPI	Native	CLK_REQ9#		PU 10K	+3VSUS
GPP_H4	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H5	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H6	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H7	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H8	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H9	GPI	Native	(N.C)		PU 10K	+3VSUS
GPP_H10	GPI	GPI	(N.C)			
GPP_H11	GPI	GPI	(N.C)			
GPP_H12	GPO	GPO	(N.C)	PD		
GPP_H13	GPI	GPI	(N.C)			
GPP_H14	GPI	GPI	(N.C)			
GPP_H15	GPI	GPI	SML3ALERT#			
GPP_H16	GPI	GPI	(N.C)			
GPP_H17	GPI	GPI	(N.C)			
GPP_H18	GPI	GPI	(N.C)			
GPP_H19	GPI	GPI	(N.C)			
GPP_H20	GPI	GPI	(N.C)			
GPP_H21	GPI	GPI	(N.C)			
GPP_H22	GPI	GPI	(N.C)			
GPP_H23	GPI	GPO	WLAN_WAKE_CTRL_CRB			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_I0	GPI	Native	(N.C)		PD 100K	
GPP_I1	GPI	Native	DDI2_HDMI_HPD		PD 100K	
GPP_I2	GPI	GPI	(N.C)			
GPP_I3	GPI	Native	DDPE_EDP_HPD			
GPP_I4	GPI	Native	EDP_HPD_CPU		PD 100K	
GPP_I5	GPI	Native	(N.C)			
GPP_I6	GPO	Native	(N.C)			
GPP_I7	GPI	Native	DDI2_CTRLCLK_HDMI		PU 2.2K	+3VS
GPP_I8	GPO	Native	DDI2_CTRLDATA_HDMI		PU 2.2K	+3VS
GPP_I9	GPI	Native	(N.C)			
GPP_I10	GPO	Native	(N.C)			
GPP_I11	GPO	Native	(N.C)			
GPP_I12	GPO	Native	(N.C)			
GPP_I13	GPO	Native	(N.C)			
GPP_I14	GPO	Native	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_J0	GPO	GPO	(N.C)			
GPP_J1	GPO	Native	CPU_C10_GATE#_PCH		PU 100K	+1.8VSUS
GPP_J2	GPO	GPO	(N.C)			
GPP_J3	GPO	GPO	(N.C)			
GPP_J4	GPO	Native	CNV_BRI_DT		PU 4.7K	+1.8VSUS
GPP_J5	GPO	Native	CNV_BRI_RSP		PU 20K	+1.8VSUS
GPP_J6	GPO	Native	CNV_RGI_DT		PU 75K	+1.8VSUS
GPP_J7	GPO	Native	CNV_RGI_RSP		PU 20K	+1.8VSUS
GPP_J8	GPO	GPO	CNV_MFUART2_RXD (TP)			
GPP_J9	GPO	GPO	CNV_MFUART2_TXD (TP)			
GPP_J10	GPO	GPO	(N.C)			
GPP_J11	GPO	GPO	(N.C)			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPP_K0	GPO	GPO	GPIO_3_FORCE_PWR			
GPP_K1	GPO	GPI	PCB_ID0			
GPP_K2	GPO	GPI	PCB_ID1			
GPP_K3	GPO	GPO	GPP_K3/WLAN_BT_LED			
GPP_K4	GPO	GPO	GPP_K4/WLAN_LED			

	Default	Use As	Signal Name	INT PU/PD	EXT PU/PD	Power
GPD0	BATLOW#	Native	PM_BATLOW#		PU 8.2K	+3VA_DSW
GPD1	ACPRESENT	Native	ME_AC_PRESENT_X1		PU 100K	+3VA_DSW
GPD2	LAN_WAKE#	Native	LAN_WAKE#		PU 10K	+3VA_DSW
GPD3	PWRBTN#	Native	PWRBTN#/PM_PWRBTN#		PU 10K(@)	+3VSUS
GPD4	SLP_S3#	Native	SLP_S3#/PM_SUSB#		PD 100K	
GPD5	SLP_S4#	Native	SLP_S4#/PM_SUSC#		PD 100K	
GPD6	SLP_A#	Native	SLP_A#			
GPD7	RSVD	GPO	(N.C)			
GPD8	SUSCLK	Native	SUS_CLK#/SUS_CLK			
GPD9	SLP_WLAN#	Native	SLP_WLAN#		PU 10K(@)	+3VA_DSW
GPD10	SLP_S5#	Native	SLP_S5#			
GPD11	LANPHYPC	GPO	iGPU_dGPU_switch		PD100K	

EC IT8995 GPIO

	Default	Use As	Signal Name	EXT PU/PD	Power
GPA0	O	GPO	PWR_LED	PD 1M	
GPA1	OD	GPO	CHG_LED#	PU 10K (@)	+3VA_EC
GPA2	OD	GPO	CHG_FULL_LED#	PU 10K (@)	+3VA_EC
GPA3	Alt	PWM	FAN1_PWM		
GPA4	O	GPO	EC_GPA4		
GPA5	Alt	PWM	FAN0_PWM		
GPA6	Alt	PWM	KB_LED_PWM		
GPA7	O	GPO	OS_LED#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPB0	Alt	GPI	AC_IN_OC#	PU 100K	+3VA
GPB1	I	GPI	LID_SW#	PU 100K	+3VA
GPB2	OD	GPO	NUM_LED#		
GPB3	Alt	GPO	EC_GPB3/PWR_SW#	PU 100K	+3VA
GPB4	I	GPO	PS_ON_EC		
GPB5	O	GPO	NKey_WRST	PD 10k	
GPB6	OD	GPO	RC_IN#	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPC0	O	GPO	PM_EXTTS#0	PU 10K (@)	+3VA_EC
GPC1	Alt	SMBus	SMB1_CLK	PU 4.7K	+3VA_EC
GPC2	Alt	SMBus	SMB1_DAT	PU 4.7K	+3VA_EC
GPC3	O	GPO	PM_PWRBTN#	PU 10K (@)	+3VSUS
GPC4	I	GPI	EC_GPC4/INTB#	PU 10K	+3VSUS
GPC5	I	GPI	PM_SUSC#	PD 100K	
GPC6	Alt	GPI	BAT1_IN_OC#	PD 100K	
GPC7	O	GPO	EC_GPC7		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPD0	I	GPI	EC_GPD0/PCH_SLP_S0#		
GPD1	O	GPO	EC_GPD1/ME_AC_PRESENT	PU 100K	+3VA_DSW
GPD2	Alt	GPI	BUF_PLT_RST#	PD 100K	
GPD3	OD	GPO	EXT_SCI#	PU 10K	+3VS
GPD4	OD	GPO	EXT_SMI#	PU 10K	+3VS
GPD5	O	GPO	EC_GPD5/OP_SD#		
GPD6	Alt	GPI	FAN0_TACH	PU 10K	+3VS
GPD7	Alt	GPI	FAN1_TACH	PU 10K	+3VS

	Default	Use As	Signal Name	EXT PU/PD	Power
GPE0	O	GPO	EC_GPE0/SUSB_EC#	PD 4.7K	
GPE1	O	GPO	EC_GPE1/SUSC_EC#	PD 4.7K	
GPE2	O	GPO	1.2V_ON		
GPE3	O	GPO	SUSWARN#_wCC		
GPE4	O	GPO	USB_BC1.2_OFF#		
GPE5	I	GPI	PM_SUSB#	PD 100K	
GPE6	OD	GPO	CAP_LED#		
GPE7	OD	GPO	THRO_CPU#	PU 10K(@)	+3VA_EC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPF0	O	GPO	5VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF1	O	GPO	VSUS_ON	PU 100K&PD 1M	+3VA_EC
GPF2	Alt	SMBus	P_SMB0_CLK	PU 4.7K	+3VA_EC
GPF3	Alt	SMBus	P_SMB0_DAT	PU 4.7K	+3VA_EC
GPF4	Alt	PS2	TP_CLK	PU 4.7K	+3VS
GPF5	Alt	PS2	TP_DAT	PU 4.7K	+3VS
GPF6	Alt	PECI	EC_GPF6/PECI_EC		
GPF7	O	GPO	PCH_SPI_OV		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPG0	O	GPO	DGPU_LIMIT		
GPG1	O	GPO	PCH_SUSACK#		
GPG2	I	GPI	EC_GPG2/PWRLIMIT_EC#	PU 100K	+3VA_EC
GPG3	GPI		EC_SCE#/EC_SCE#_PCH		
GPG4	GPI		EC_SI/EC_SI_PCH		
GPG5	GPI		EC_SO/EC_SO_PCH		
GPG6	O	GPO	USB30_5VBUS		
GPG7	GPI		EC_SCK_PCH	PD 10K (@)	

	Default	Use As	Signal Name	EXT PU/PD	Power
GPH0	Alt	PCI	PM_CLKRUN#	PU 8.2K	+3VS
GPH1	Alt	SMBus	P_SMB3_CLK	PU 4.7K	+3VA_EC
GPH2	Alt	SMBus	P_SMB3_DAT	PU 4.7K	+3VA_EC
GPH3	O	GPO	PM_RSMRST#	PD 10K(@)	
GPH4	O	GPO	DPWROK_EC	PD 10K	
GPH5	O	GPO	PM_PWROK	PD 10K	
GPH6	O	GPO	PM_SYSPWROK	PD 10K	
GPH7	O	GPO	LCD_BACKOFF#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPI0	I	GPI	PM_SLP_SUS#		
GPI1	I	GPI	3VSUS_PWRGD		
GPI2	I	GPI	ALL_SYSTEM_PWRGD	PU 10K	+3VS
GPI3	I	GPI	IMVP8_PWRGD	PU 100K	+3VS
GPI4	I	GPI	3VA_DSW_PWRGD	PU 100K	+3VA_DSW
GPI5	I	GPI	SUSWARN#		
GPI6	Alt	AD	A/D_MAX_POWER	PD 0	+3VACC
GPI7	Alt	AD	MB_MAX_POWER	PU 100K & PD 56K	+3VACC

	Default	Use As	Signal Name	EXT PU/PD	Power
GPJ0	O	GPI	EC_GPJ0/USB31_5VBUS#	PU 10K	+3VSUS
GPJ1	O	GPO	3VADSW_ON	PU 100K	+3VA_EC
GPJ2	Alt	DA	PL_REF_EC		
GPJ3	O	GPO	EC_GPJ3 / PCH_SUS_STAT#		
GPJ4	Alt	DA	IBAT_REF_EC		
GPJ5	O	GPO	EC_GPJ5		
GPJ6	I	GPI	KB_WAKE#	PU 100K	+3VA_DSW
GPJ7	O	GPO	USB_CHARGE_ON#		

	Default	Use As	Signal Name	EXT PU/PD	Power
GPM0	LAD0/EIO0		LPC_AD0_R/LPC_AD0		
GPM1	LAD1/EIO1		LPC_AD1_R/LPC_AD1		
GPM2	LAD2/EIO2		LPC_AD2_R/LPC_AD2		
GPM3	LAD3/EIO3		LPC_AD3_R/LPC_AD3		
GPM4	LPCCLK/ESCK		CLK_KBCPCI_PCH		
GPM5	LFRAME#/ECS#		LPC_FRAME#		
GPM6	SERIRQ/ALERT#		INT_SERIRQ	PU 10K	+3VS

N501VW Setting

SM_BUS ADDRESS :

PCH Master		
SM-Bus Device	SM-Bus Address	
SO-DIMM A(0)	A0h	
SO-DIMM B(0)	A2h	
EC Master (SMB1)	SM-Bus Address	
SM-Bus Device		
VGA Thermal Sensor	96h	
CPU Thermal Sensor	90h	
Power Thermal Sensor	7Eh	

Device Identification

CPU Thermal Senser		
1st	06G023123010	NCT7717U
2nd		

N501VW PCIE & USB Function define

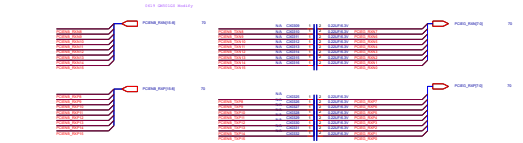
Skylake HM170

HSIO	HSIO Capabilies	Funcon	SRC
	PCIEG (From GPU)	dGPU	SRC0
01	USB3#01	USB3.0 Port1	
02	USB3#02 / SSIC#01	USB3.0 Port2	
03	USB3#03 / SSIC#02		
04	USB3#04		
05	USB3#05	USB3.0 Port3	
06	USB3#06	USB3.0 Port4	
07	USB3#07 / PCIE#01	CardReader_USB3(RSV)	
08	USB3#08 / PCIE#02		SRC2
09	PCIE#03	WLAN	SRC3
10	PCIE#04 / GBE	LAN	SRC4
11	PCIE#05 / GBE	Thunderbolt	SRC5
12	PCIE#06		
13	PCIE#07		
14	PCIE#08		
15	PCIE#09 / SATA#0 / GBE	SATA#1 SSD	SRC6
16	PCIE#10 / SATA#1	PCIE*4 SSD	
17	PCIE#11		
18	PCIE#12 / GBE		
19	PCIE#13 / SATA#0 / GBE		
20	PCIE#14 / SATA#1		
21	PCIE#15 / SATA#2		
22	PCIE#16 / SATA#3	SATA#3 HDD	
23			
24			
25			
26			

USB 2.0	Funcon
USB2_01	USB3.0 MB Port1(Charger)
USB2_02	USB3.0 MB Port2
USB2_03	XBOX
USB2_04	Camera
USB2_05	USB3.0 MB Port3
USB2_06	USB3.0 MB Port4
USB2_07	Card Reader
USB2_08	N key
USB2_09	BT
USB2_10	
USB2_11	
USB2_12	

ASUS Project Name: GM501GS		Rev 2.1
Title : System Setting		
Size: Custom	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Date: Wednesday, January 17, 2018	Sheet 2 of 102	

PCIEG



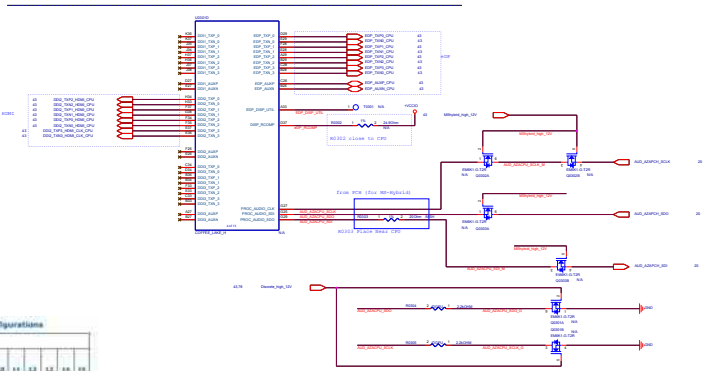


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Registered Bricks	x8 Controller Registered Bricks	x4 Controller Registered Bricks	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	8	9	1	2	3	6	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	8	9	1	2	3	6	5	6	7
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	6	5	2	1	0

NOTES:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configurations), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
   — Connect lane 0 of 1st device to lane 0.
   — Connect lane 0 of 2nd device to lane 4.
   — Connect lane 0 of 3rd device to lane 12.
   For example:
   a. When using 1x4 + 2x4, the 8 lane device must use lanes 0:7.
   b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9
   c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9,one lane device must use lane 12.

Refer to CPU-8 EDS P.163 (Rev.1.7)(Jul.2019)

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

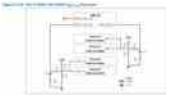
When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. ~1KΩ). PROC_AUDIO_SDO can be left unconnected.

ASUS	Project Name: G15CB/G15		Rev: 1.0
Title: CPU_PEG,PCIE,FDI,DMI			
Size: C	Dept:	Model Net: G15CB/G15 SKU	Engineer: NB1 RD2 EE1
Date: Wednesday, January 27, 2021		Sheet 1 of 102	

Memory Channel A

Memory Channel B

Main Board



ASUSTeK Computer Inc.

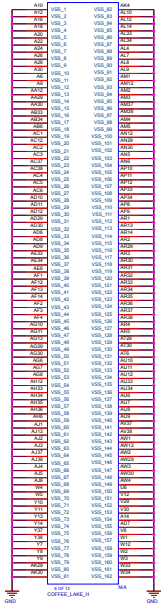
Title: CPU_DDR4

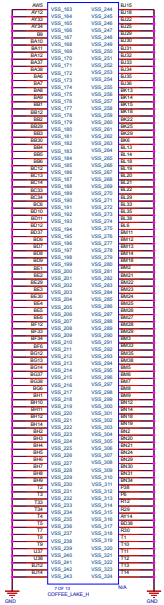
Size: Document Number: Rev: 1.0

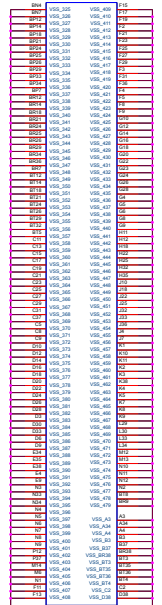
Date: Sheet of

File: Drawn By: Checked By: Approved By:

Engineer: NB1 RD2 EE1

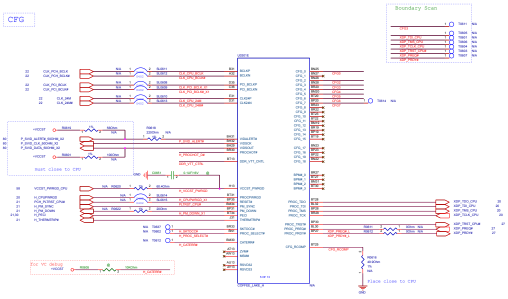


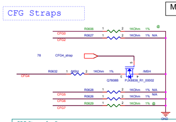




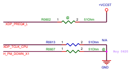
Main Board

ASUS	Project Name: GM501GS		Rev: 2.1
Title : CPU_GND			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Wednesday, January 17, 2018	Sheet 5 of 102		





Main Board



CFG Straps for Processor

CFG[0] : Stall reset sequence after PCU PLL lock until de-asser ted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express* Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Expres* Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

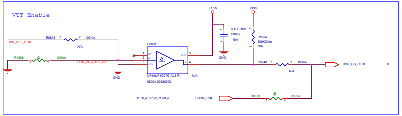
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

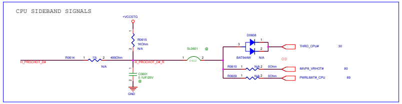
CFG[19:8] : Reserved Configuration Lanes

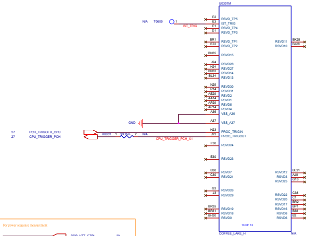
Reserved Configuration Lanes

Refer : Intel 570805_CFL_EDS_Vol1_Rev1.1, Table 6-7, P.116

DDR_VTT_CNTL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator in C8 and deeper and S3.

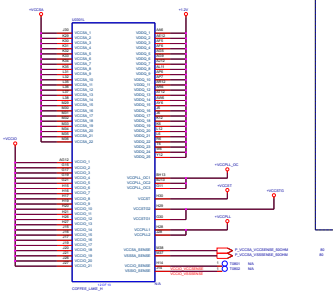


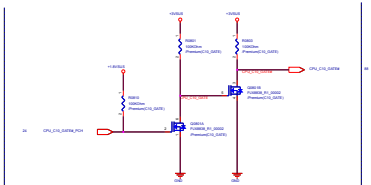




ASUS	Project Name: GM501GS
Title :	CPU_CFG,RSVD
Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1
Size: C	Rev: 2.1
Date: Thursday, January 18, 2018	Sheet 6 of 102

Main Board



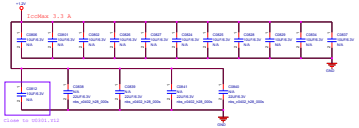


Main Source	1st PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSDGS	+VDDQ_CPU	+1.05V_VCCSTG
		+VCCSTG	+1.05V_VCCPLL
	+1.2V	+VCCPLL_OC	
	+VCCSA		
	+VCCIO		

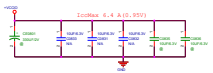
+VCCST/+VCCPLL
DECAPS Place Back Side (TOP)

+VDDQ DECAPS Place Back Side (TOP)

10UF x 11
22UF x4

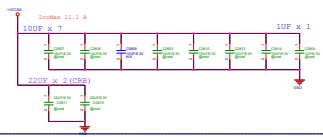


+VCCIO DECAPS Place Back Side (TOP)



+VCCPLL_OC DECAPS Place Back Side (TOP)

+VCCSA DECAPS Place Back Side (TOP)

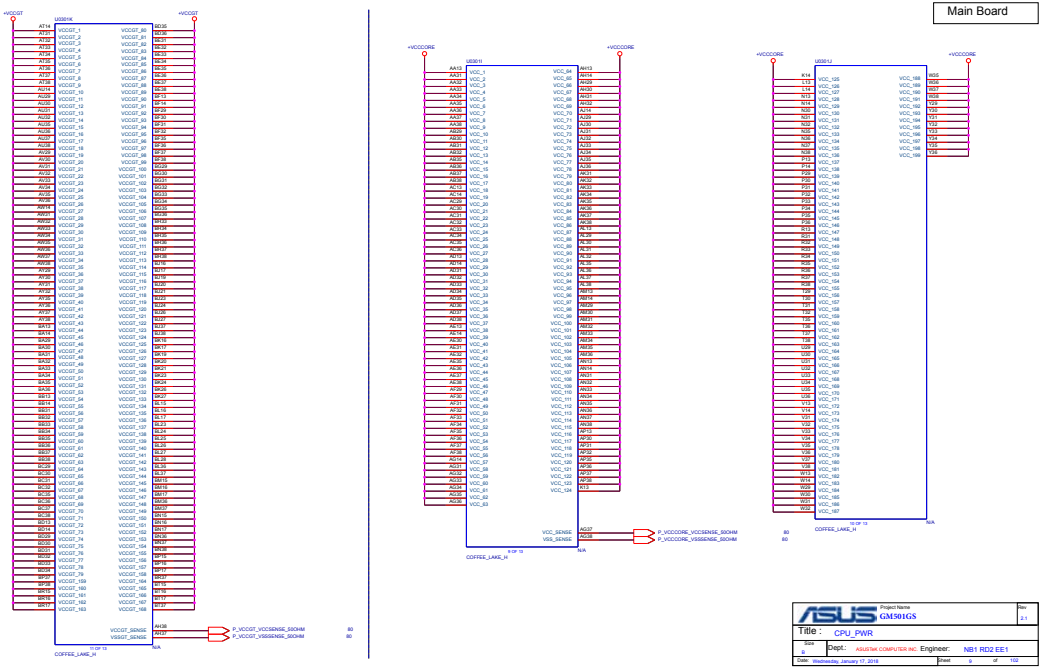


+VCCSTG DECAPS Place Back Side (TOP)

+VCCSA cap near CPU

Title :	CPU_PWR		
Size :	Dept. :	Engineer :	NB1 RD2 EE1
Date : Thursday, January 16, 2014		Sheet	of

Main Board

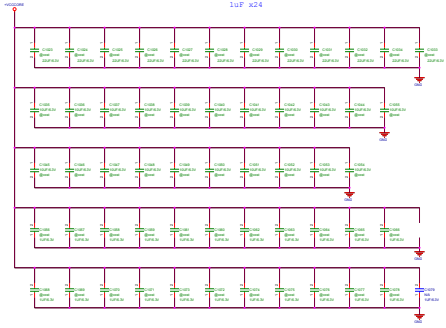


ASUS	Project Name: GM501GS		Rev: 2.1
Title : CPU_PWR			
Size: B	Dept: ASUSTeK COMPUTER INC	Engineer: NB1 RD2 EE1	
Date: Wednesday, January 17, 2018		Sheet: 9 of 102	

Main Board

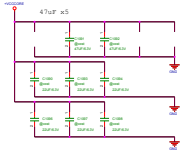
+VCCCORE DECAPS Place Back Side (TOP)

22uF x12
10uF x21
1uF x24



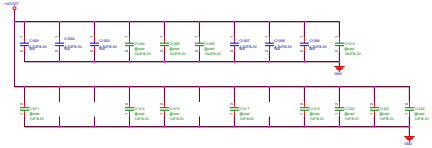
+VCCCORE cap near CPU

47uF x5



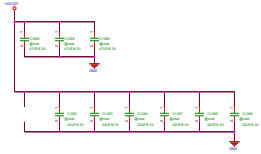
+VCCGT DECAPS Place Back Side (TOP)

10uF x10
1uF x12

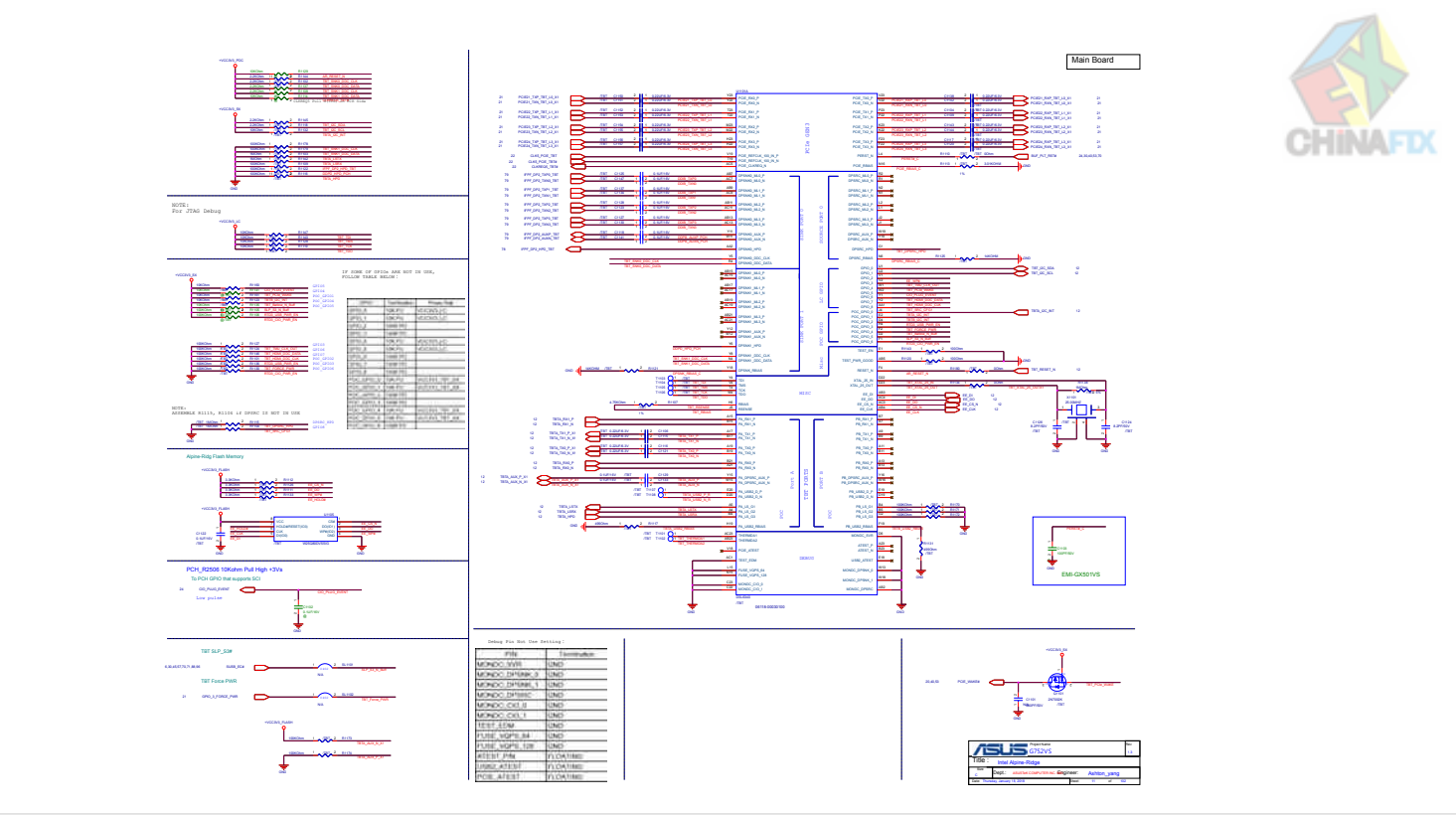


+VCCGT cap near CPU

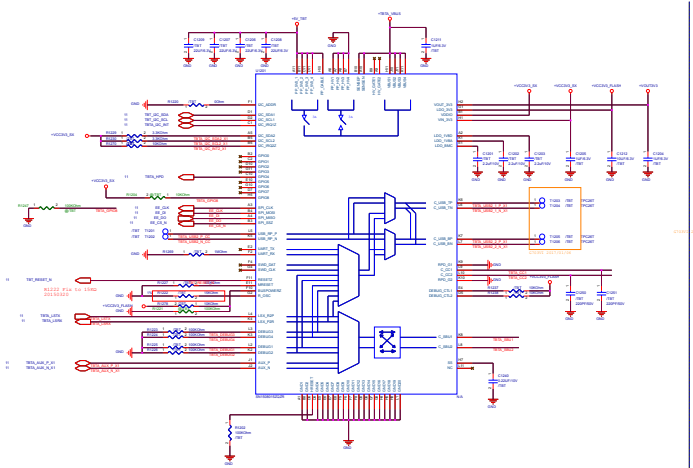
47uF x3
22uF x7

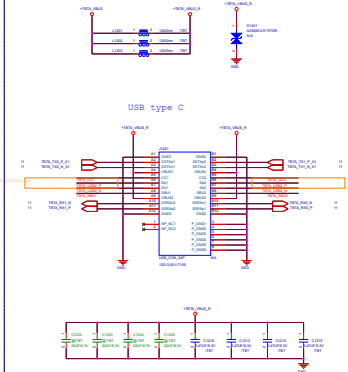


ASUS	Project Name: GM501GS		Rev: 1.0
Title : CPU_POWER_CAP			
Size: Custom	Doc#:	Date: Wednesday, January 07, 2015	Sheet: 13 of 100
Engineer:	NB1 RD2 EE1		

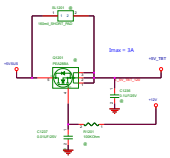

Main Board
NOTE:
For JTAG Debug
IF SOME OF SPIOs ARE NOT IN USE,
FOLLOW TABLE BELOW :
NOTE:
ASSEMBLE R1119, R1106 if SPDBC IS NOT IN USE
Alpine-Ridg Flash Memory
PCH_R2508 10Kohm Pull High +3Vs
Low pulse
TBT SLP_S3#
TBT Force PWR
Debug Pin Out Use Setting :
EMI-GX501VS

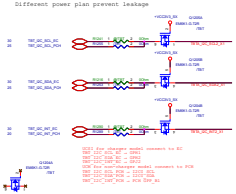
Main Board



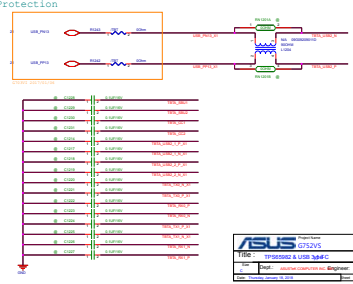


TBT 5V Power

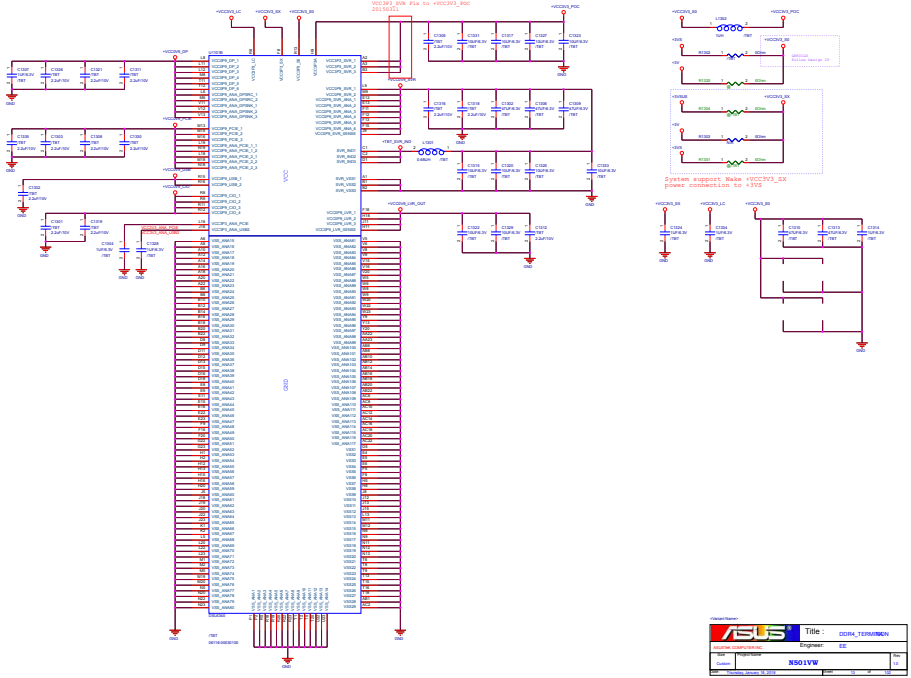


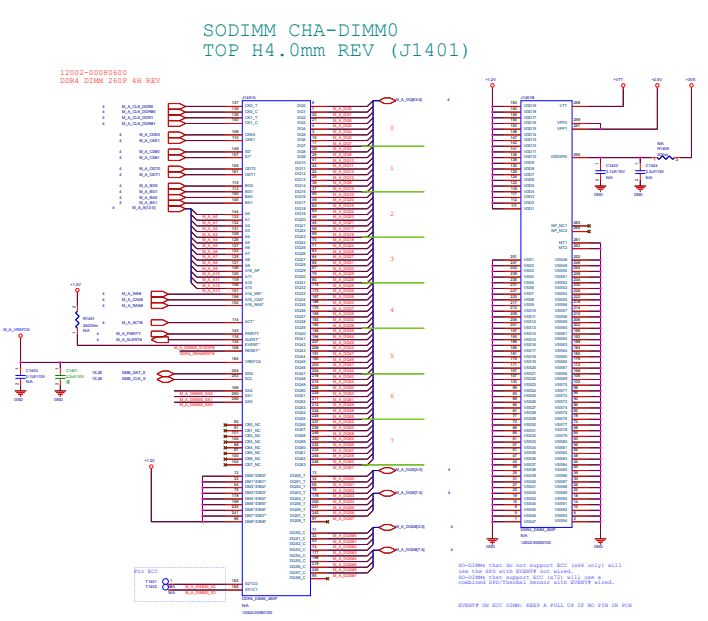


ESD-Protection

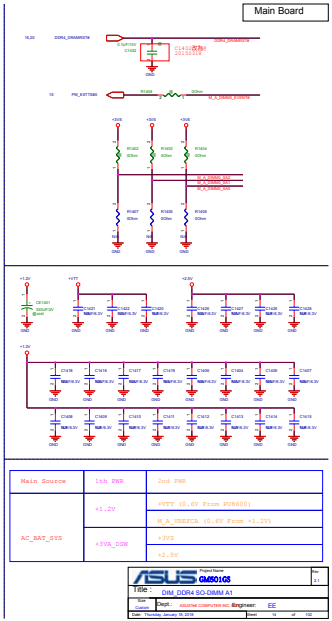


Project Name:	G752VS
Title :	TP5658802 & USB 3.0/Type-C
Dept :	Engineer: Ashton_yang
Date :	Thursday, January 18, 2018


VCC3V3_SVK Fix to +VCC3V3_POC
20150311
System support Wake
power connection to +3VS
Title :
DDR4_TERMINATION
Engineer:
EE
N501VW



Main Board

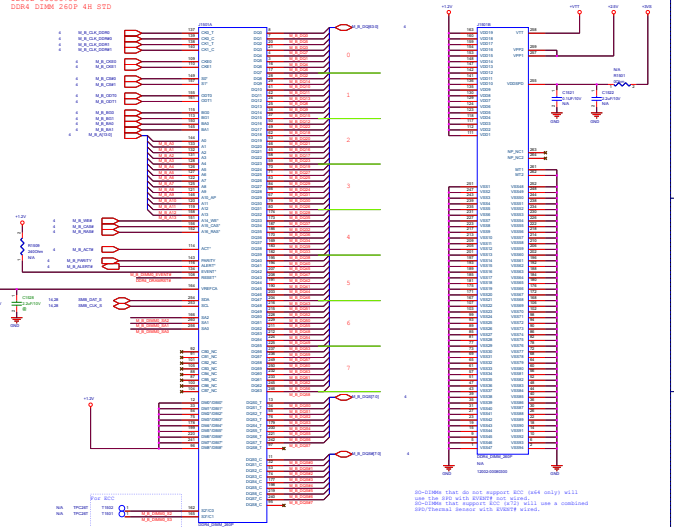


Main Source	1th PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PCH&SOC)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

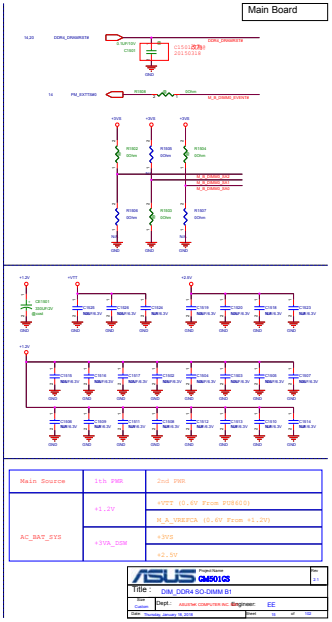
Project Name	GM501GS	Rev 2.1
Title :	DIM_DDR4 SO-DIMM A1	
Size	Custom	
Date: Thursday, January 18, 2018	Sheet 16 of 150	
Dept. : ASUSTeK COMPUTER INC.	Engineer: EE	

SODIMM CHB-DIMM0
TOP H4.0mm STD (J1501)

12002-00080700
DDR4 DIMM 260P 4H STD



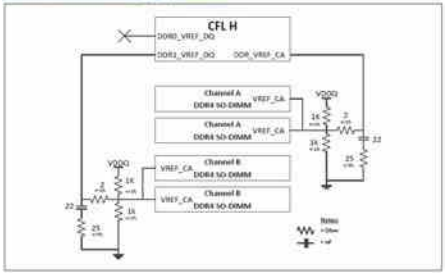
Main Board



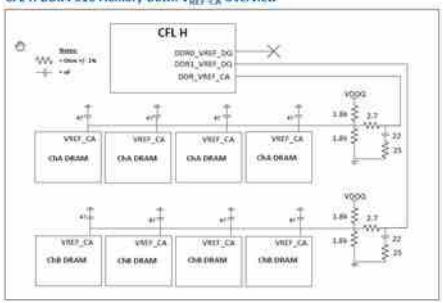
Main Source	1ch PWR	2nd PWR
AC_BAT_SYS	+1.2V	+VTT (0.6V From PU8803)
		M_A_VREFCA (0.6V From +1.2V)
	+3VA_DSW	+3VS
		+2.5V

ASUS	Project Name: GM501GS		Rev: X1
Title :	DIM_DDR4 SO-DIMM B1		
Size:	Document Number:		
Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: EE	
Date: Thursday, January 18, 2018	Sheet 15 of 100		

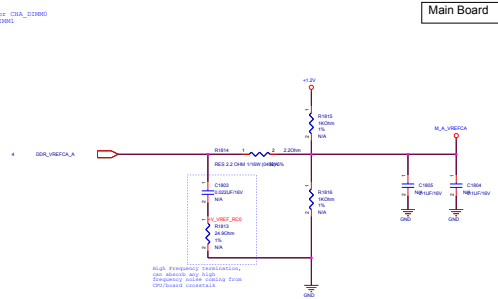
CFL H DDR4 SO-DIMM V_{REF_CA} Overview

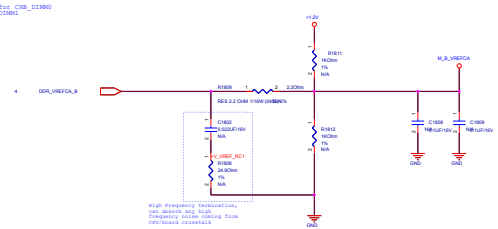


CFL H DDR4 x16 Memory Down V_{REF_CA} Overview

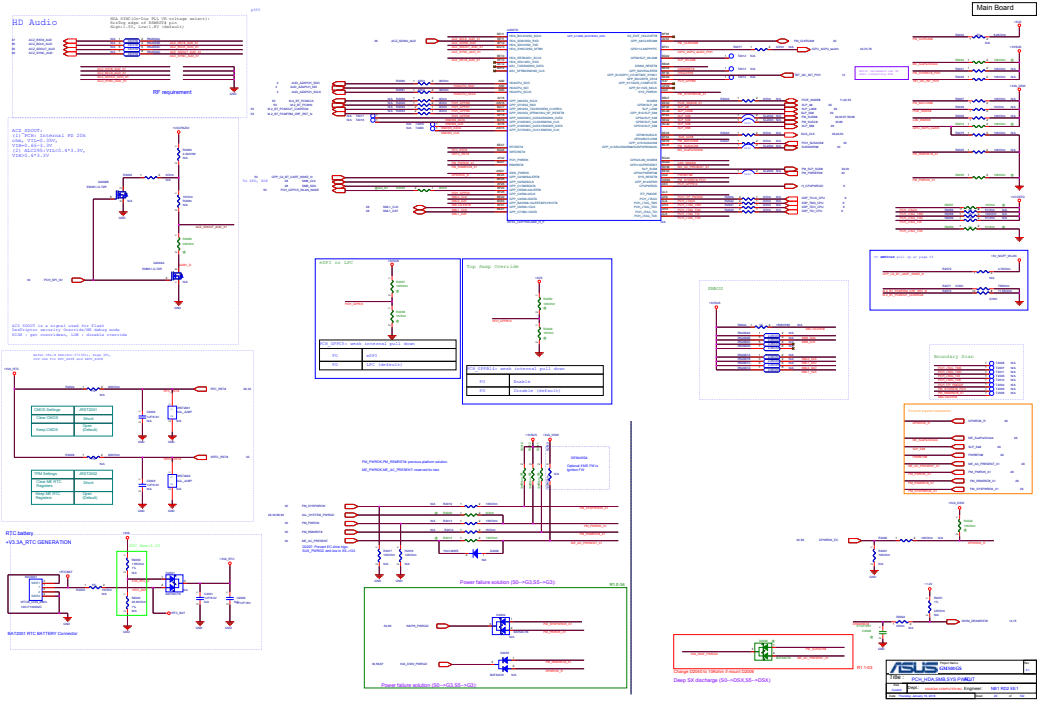


Main Board





ASUS	Project Name: GM501GS		Rev: 2.1
Title :	DIM_CA/DQ Page		
Size: B	Dept.: ASUSTeK COMPUTER INC	Engineer:	NB1 RD2 EE1
Date: Wednesday, January 17, 2018		Sheet: 16 of 102	


Main Board
HD Audio
RF requirement
ACE_RSOUT#:
(1) "PCB: Internal PU 20k
ohm, VTT=1.05V;
VCCIO=1.05V
(2) ALC269:VTT=0.675V,
VCCIO,AVL=3.3V
ACE_RSOUT# is a signal used for Flash
Configurator security (Override ME debug mode
RSOUT# = pwr overvoltage, LOW = disable override
SPI_CS0#, weak internal pull down
PU
weak
PD
SPI (default)
SPI_CS1#, weak internal pull down
PU
Disable
PD
Disable (default)
Stop Bump Override
RTC battery
+V3.3A_RTC GENERATION
MAT2001 RTC BATTERY Connector
Power failure solution (S0->G3,S5->G3)
Power failure solution (S0->G3,S5->G3)
Deep SX discharge (S0->S5,S5->DSX)
Change CMOS to Vaturn if mount 0.022R
ASUSTeK Computer Inc.
Title: PCH_HDA,SMB,SYS PWR(2/7
Size: Document Number:
Date: Sheet of

USB Setting

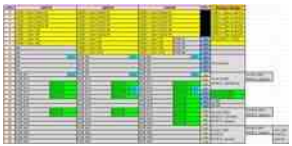
USB 2.0	
USB2_01	
USB2_02	
USB2_03	USB3.0 type A
USB2_04	USB3.0 type A
USB2_05	USB3.0 type A
USB2_06	USB3.0 type A
USB2_07	Card Reader
USB2_08	XBOX WLAN
USB2_09	Camera
USB2_10	N-Key + KB BL control
USB2_11	BT
USB2_12	Tobii IS4
USB2_13	TBT
USB2_14	

USB 3.0	
USB3_01	
USB3_02	
USB3_03	USB3.0 type A
USB3_04	USB3.0 type A
USB3_05	USB3.0 type A
USB3_06	USB3.0 type A
USB3_07	Card Reader
USB3_08	

GM501GS PCIE/SATA Function define

	Funcsen		Funcsen
PCIE-01	[USB3-7] USB3 Card Reader	PCIE-13 [SATA-0B]	SATA HDD
PCIE-02		PCIE-14 [SATA-1B]	SATA SSD
PCIE-03		PCIE-15 [SATA-2]	
PCIE-04		PCIE-16 [SATA-3]	WLAN AC
PCIE-05	TBT AR	PCIE-17 [SATA-4]	PCIE /SATA SSD
PCIE-06	TBT AR	PCIE-18 [SATA-5]	PCIE SSD
PCIE-07	TBT AR	PCIE-19 [SATA-6]	PCIE SSD
PCIE-08	TBT AR	PCIE-20 [SATA-7]	PCIE SSD
PCIE-09	PCIE /SATA SSD	PCIE-21	GLAN
PCIE-10	PCIE SSD	PCIE-22	GLAN
PCIE-11 [SATA-0A]	PCIE SSD	PCIE-23	
PCIE-12 [SATA-1A]	PCIE SSD	PCIE-24	

	Funcsen
CLKREQ-0	DGPU
CLKREQ-1	
CLKREQ-2	WLAN-AC
CLKREQ-3	
CLKREQ-4	GLAN
CLKREQ-5	TBT AR
CLKREQ-6	PCIE SSD
CLKREQ-7	PCIE SSD
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	



Main Board

USB3.0 Port1 : JS201 (Charger Port)
USB3.0 Port2 : JS202
USB3.0 Port3 : J4901
USB3.0 Port4 : J4902

CardReader : U4201
XBOX WLAN : JS202
Camera : J4501
N-Key + KB BL control : U3502

Tobii IS4 : J4502
TBT : J1501
BT : JS301

USB3.0 Port7 For CR

Thunderbolt

PCIE x4 3301

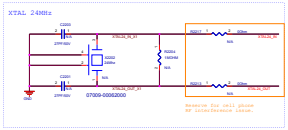
CLKREQ

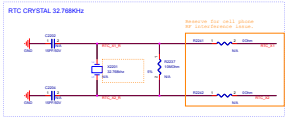
SATA HDD

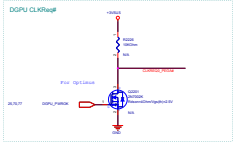
PCIE x4 3301

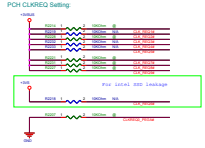
R1.0-31 sel 0 :PCIE
sel 1 :SATA

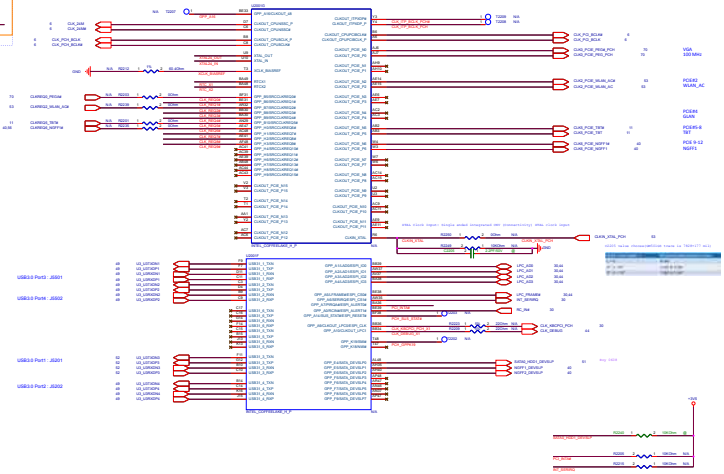
must close to PCH


XTAL 24Mhz
07009-60002000
Reserve for cell phone RF interference issue.


RTC CRYSTAL 32.768KHz
Reserve for cell phone RF interference issue.

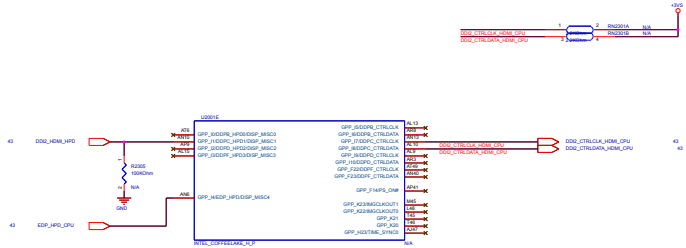

DGPU CLKReq#
For Optimus


PCH CLKREQ Setting:
For Intel SSC leakage

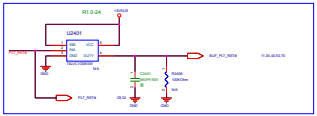

USB3.0 Port3 : J5201
USB3.0 Port4 : J5202
USB3.0 Port1 : J5201
USB3.0 Port2 : J5202


Project Name: GM5HGS
Title: PCH_CLK,UPC,USB3
Engineer: NB1-RD2 EE1

Main Board

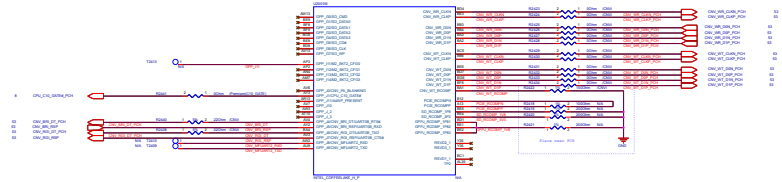


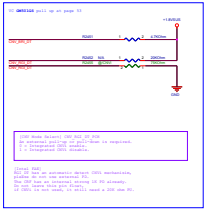
Project Name: GM501GS			Rev: 2.1
Title: PCH_VDS,eDP			
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer:	NB1 RD2 EE1
Date: Wednesday, January 17, 2018	Sheet: 23	of:	102



Code	KBID 2 (SPI_MISO)	KBID 1 (SPI_MOSI)	KBID 0 (SPI_SCK)
0x00	L	L	L
0x01	L	L	H
0x02	L	H	L
0x03	L	H	H
0x04	H	L	L
0x05	H	L	H
0x06	H	H	L
0x07	H	H	H

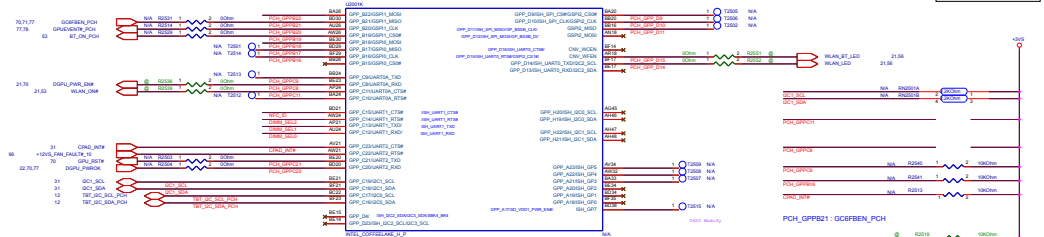
5. 建議 BIOS RD 在 KB ID 選取的區分，預先加入 Reverse code，以符合第 1 點 table



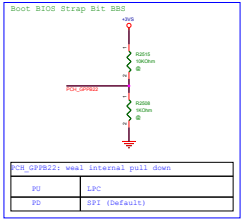


Project Name	GM5NXGS
Rev	2.1
Title :	PCH_SPI
Size	A3
Dept :	
Engineer :	
Date	Thursday, January 18, 2018
Sheet	22 of 102

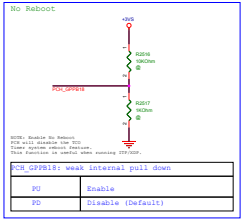
Main Board



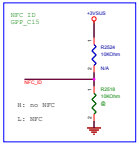
	Hynix(2Gb)	XXX (2Gb)	Micron(2Gb)
DIMM_SEL0			
DIMM_SEL1			
DIMM_SEL2			



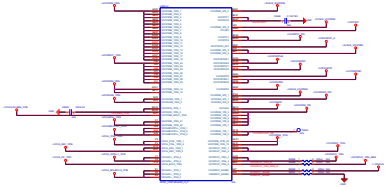
PCH_GPPB22: weak internal pull down	
PU	LPC
PD	SPI (Default)



PCH_GPPB18: weak internal pull down	
PU	Enable
PD	Disable (Default)

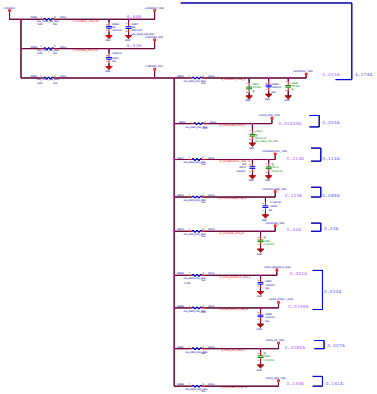


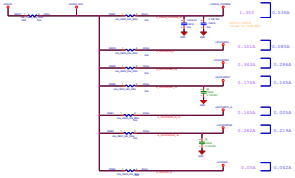
Project Name: GM501GS			Rev: 2.1
Title: PCH_GPIO			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Thursday, January 18, 2018	Sheet: 25	of: 102	

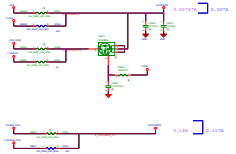


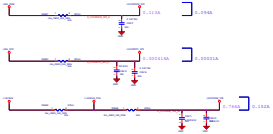
GPIO Voltage Level

Device	Power pin	Power option	Power plane
GPP_A	VCCGPIO	3.3V	+VSUS
GPP_B	VCCGPIO	3.3V	+VSUS
GPP_C	VCCGPIO	3.3V	+VSUS
GPP_D	VCCGPIO	3.3V or 1.8V	+1.8VSUS
GPP_E	VCCGPIO	3.3V	+VSUS
GPP_F	VCCGPIO	3.3V	+VSUS
GPP_G	VCCSDIO, VCCGPIO	3.3V only	+VSUS
GPP_H	VCCGPIO	3.3V	+VSUS
GPP_I	VCCSDIO, VCCGPIO	3.3V only	+VSUS
GPP_J	VCCGPIO, VCCGPIO	3.3V only	+1.8VSUS
GPP_K	VCCGPIO	3.3V	+VSUS
GPD	VCCSUS_3P3	3.3V only	+3VA_SUS

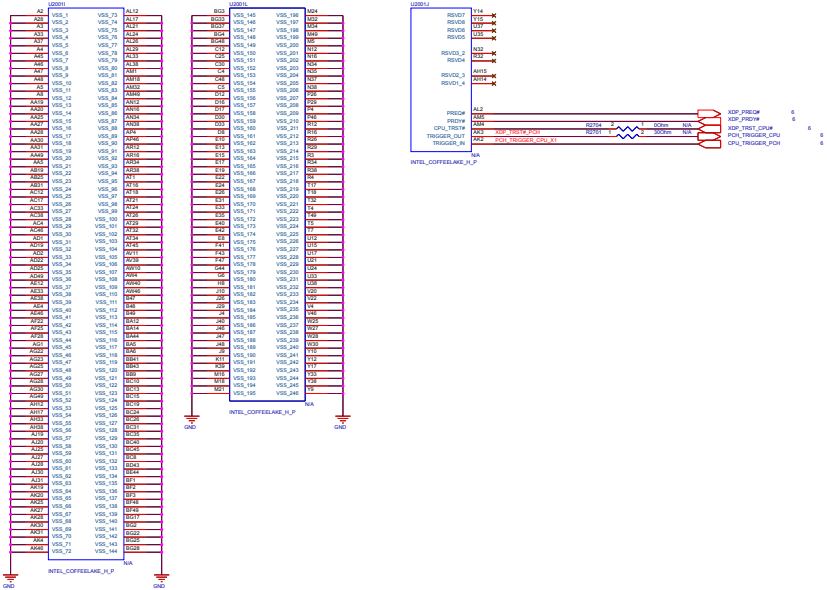






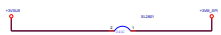


Main Board

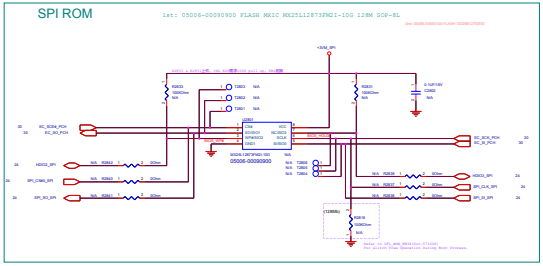


Project Name: GM501GS			Rev: 2.1
Title : PCH_POWER,GND			
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB1 RD2 EE1	
Date: Wednesday, January 17, 2018	Sheet 27 of 102		

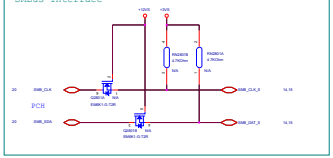
SPI Power



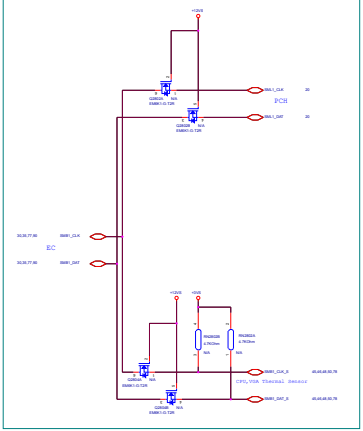
SPI ROM



SMBus Interface



System Management Interface



ASUS	Project Name: GM5616GS		Rev: X1
Title:	PCH_SPI ROM.OTH		
Size:	Dept:	Industrial Liquid Solution Inc.	Engineer: NB1 RD2 EE1
Date: Wednesday, January 17, 2018		Sheet: 28 of: 100	

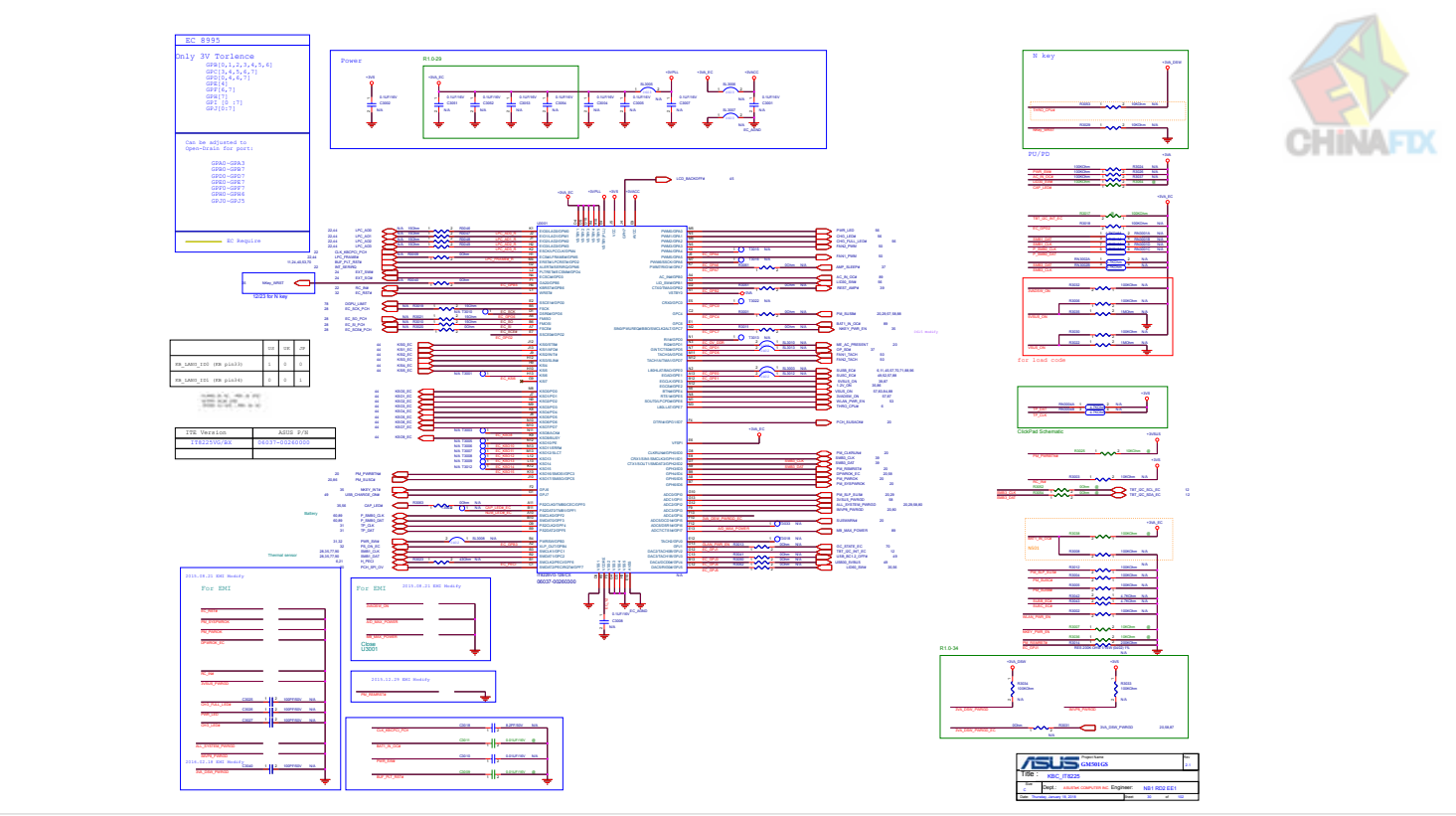
Main Board

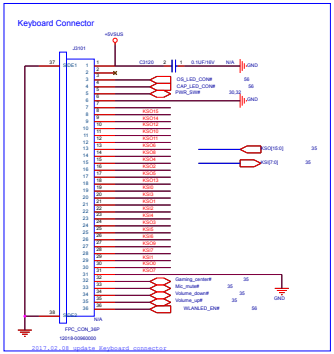
For power sequence measurement, place on CPU & GPU side of PCB

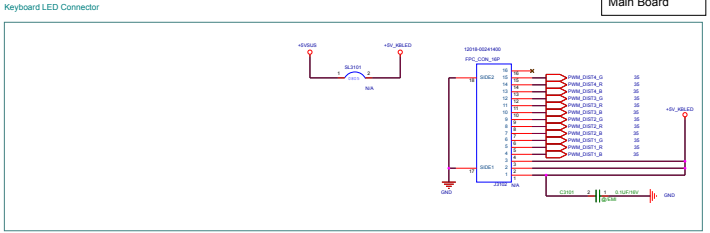
+1.0V_VCCPLL ----------> R6809

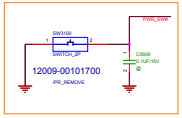
H_VCCST_PWRGD ----------> RC420

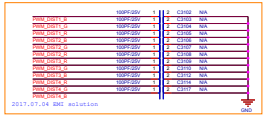
ASUS	Project Name: GM501GS		Rev: 2.1
Title :	<Title>		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer:	NB1 RD2 EE1
Date: Wednesday, January 17, 2018	Sheet 29	of	102

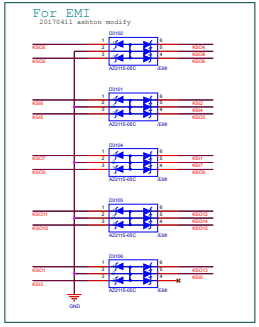

EC 8995
Only 3V Torlence
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[2,4,6,7]
GPE[4,7]
GPF[7]
GPI [0 :7]
GPJ[0:7]
Can be adjusted to
Open-Drain for port:
GPA0-GPA3
GPB0-GPB7
GPC0-GPC7
GPD0-GPD7
GPE0-GPE7
GPF0-GPF6
GPJ0-GPJ5
EC Require
Power
R1.0-29
N key
PD/PD
for load code
ClickPad Schematic
R1.0-34
ASUSTeK Computer Inc.
CM30GI.GS
Title : NBC_ITE8295
Size : C
Dept. : Industrial COMPUTER INC.
Engineer:
NB1 RD2 EE1
Date : Thursday, January 18, 2018
Sheet 1 of 100
2015.08.21 EMC Modify
For EMI
Close
U2001
2015.12.29 EMC Modify
2016.02.18 EMC Modify

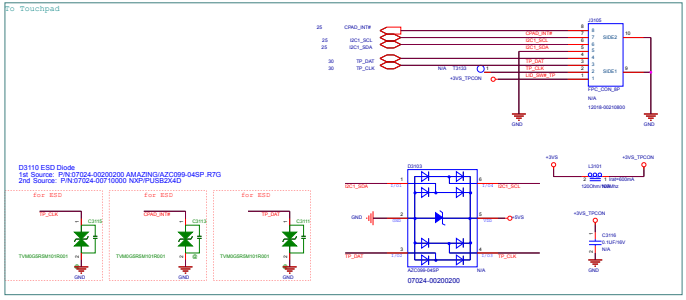

Keyboard Connector
+5VSUS
JIN01
KSO[15:0]
KSI[7:0]
OS_LED_CON#
CAP_LED_CON#
PWR_SW#
Gaming_center#
Mic_mute#
Volume_down#
Volume_up#
WLANLED_EN#
FPC_CON_36P
12019-03060030
2017.02.08 update Keyboard connector


Keyboard LED Connector
+5VSUS
+5V_KBLED
SLIH01
12019-00241400
FPC_CON_18P
PWM_DIST4_G
PWM_DIST4_R
PWM_DIST4_B
PWM_DIST3_G
PWM_DIST3_R
PWM_DIST3_B
PWM_DIST2_G
PWM_DIST2_R
PWM_DIST2_B
PWM_DIST1_G
PWM_DIST1_R
PWM_DIST1_B
C3101
0.1UF/16V


PWR_SW#
SW3100
SWITCH_2P
12009-00101700
#N_REMOVE
C5609
0.1UF/16V


PWM_DIST1_R
PWM_DIST1_G
PWM_DIST1_B
PWM_DIST2_R
PWM_DIST2_G
PWM_DIST2_B
PWM_DIST3_R
PWM_DIST3_G
PWM_DIST3_B
PWM_DIST4_R
PWM_DIST4_G
PWM_DIST4_B
100PF/25V
C3102
C3103
C3104
C3105
C3106
C3107
C3108
C3109
C3110
C3111
C3112
C3113
C3114
C3117
2017.07.04 EMI solution


For EMI
20170411 ashton modify
D3102
D3101
D3104
D3103
D3105
AZ0719-02EC
KSO4
KSO5
KSO6
KSO0
KSO1
KSO2
KSO3
KSO7
KSO8
KSO9
KSO10
KSO11
KSO12
KSO13
KSO14
KSO15
KSO16

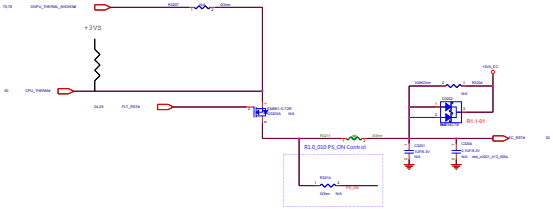

To Touchpad
CPAD_INT#
SIC1_SCL
SIC1_SDA
TP_DAT
TP_CLK
+3VS_TPCON
J3105
FPC_CON_8P
12019-00210800
D3110 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D
for ESD
TVM0GSRSM101R001
D3103
AZC099-04SP
07024-00200200
+3VS
LSH01
12MHz
C3116
0.1UF/16V

Main Board
<Variant Name>
Title : KBC_KB & TP
Engineer: EE
Size: B
Project Name: GM501GS
Rev: 2.1
Date: Thursday, January 18, 2018
Sheet 31 of 102

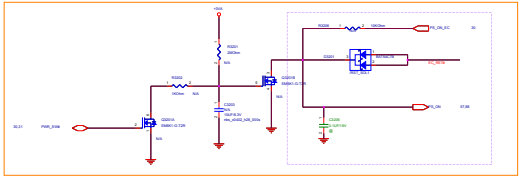
Main Board

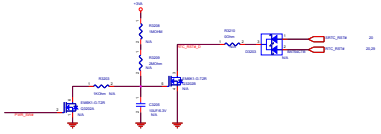
Reset Circuit

Pull up +3VS through R7507(10Kohm-1025Ohm)
When +3VS0 ready, R7507(10kOhm) and R5203(7.5kOhm) will be in parelle.
The CPU temperature point is protected ahead of time.
Increasing R7507 value can reduce to affect R5203.



Battery embedded (press pwr_sw 10sec, then reset ec)

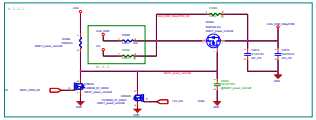




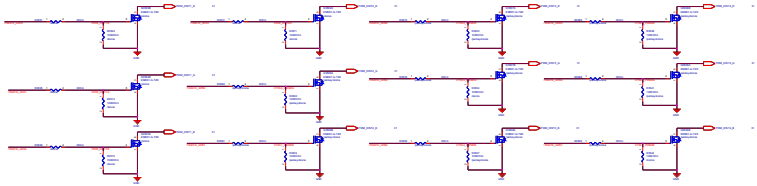
EC power off solution:
Solution1 Mount R3308, D3201/ Unmount R3216
Solution2 Mount R3308/R3216/ Unmount D3201/ for reserved 0402 f outprint

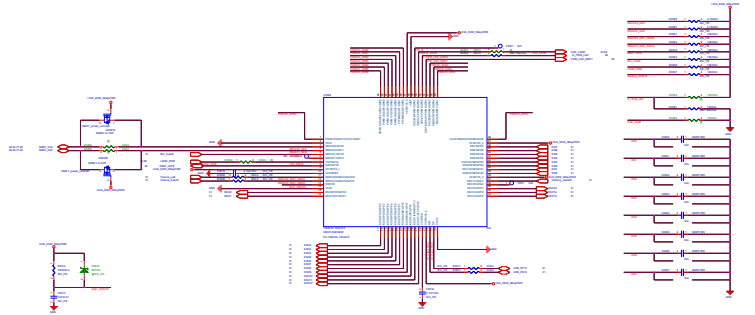
R1.2-65

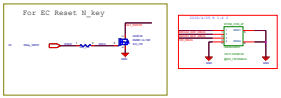
	Title :	RST_Reset Circuit	
ASUSTeK COMPUTER	Engineer:	EE	
Size	Project Name		Rev
A3	GM501GS		0.1
Date: Thursday, January 09, 2020	Sheet 35 of 45		

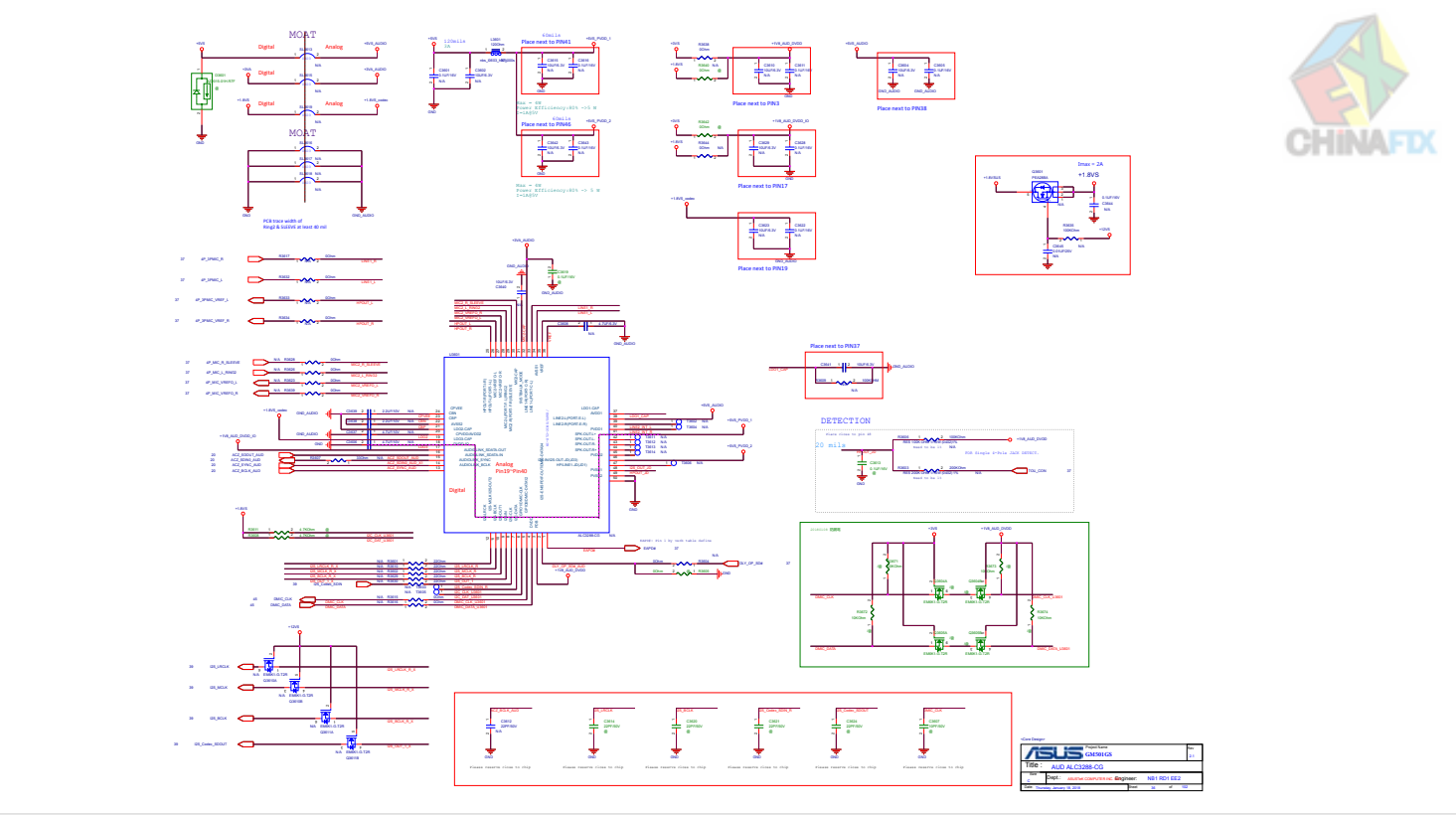


Signal name	S0	S3	S4/AC	S4/DC	S5
PWR_EN	H	L	L	L	L
PWR_EN_1V8	H	H	L	L	L
PWR_SRC_DELAY#1	H	H	H	L	L



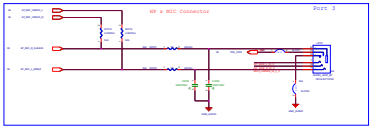


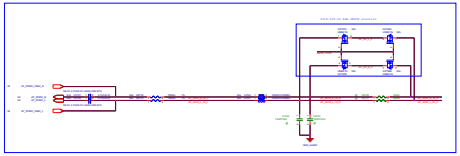


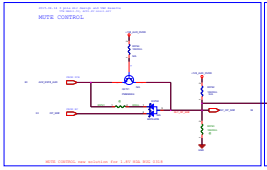

MOAT
Digital
Analog
PCB trace width of
Ring3 & SUSVS at least 40 mil
Place next to PIN41
Place next to PIN45
Place next to PIN3
Place next to PIN38
Place next to PIN17
Place next to PIN19
Place next to PIN37
Imax = 2A
+1.8VS
DETECTION
Analog
Pin19~Pin40
Digital
AUD AL3288-CG
GM5814GS
N81 RD1 E62
Engineer:
Title :

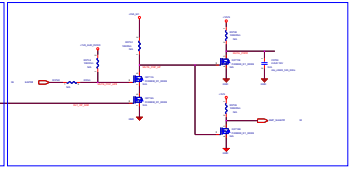
Main Board

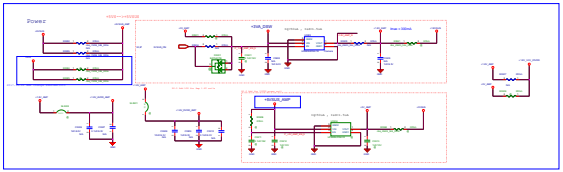
Headphone & MIC single 4-Pole Jack

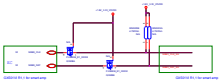


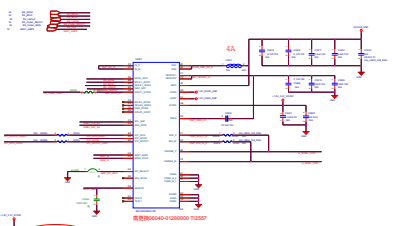


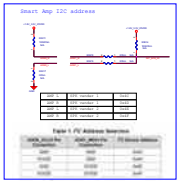


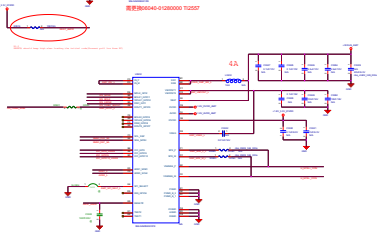


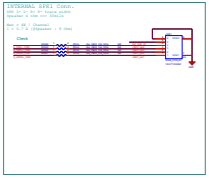

Power

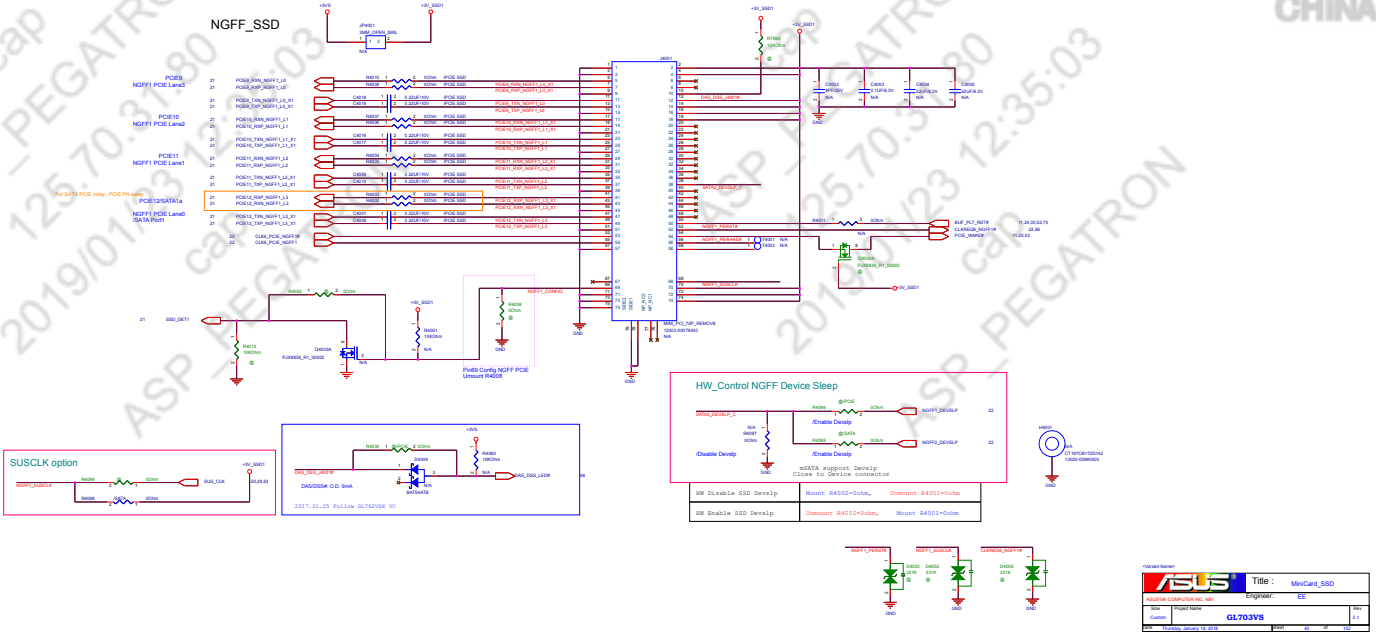





Smart Amp I2C address

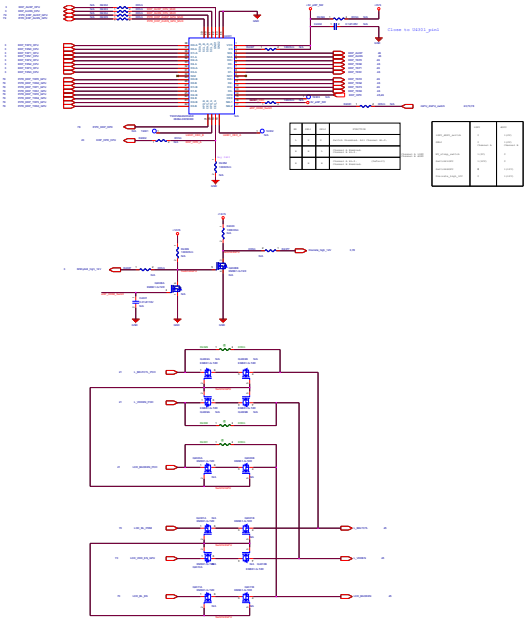



INTERNAL SPK1 Conn.

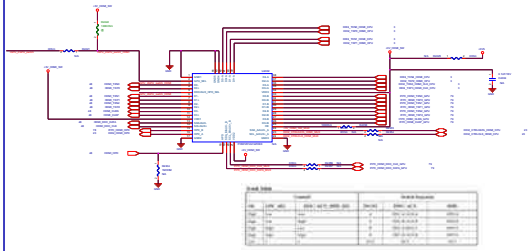


Title :	MiniCard_SSD		
Engineer:	EE		
Size	Project Name		Rev
Custom	GL703VS		2.1
Date:	Thursday, January 18, 2018	Sheet	46 of 100

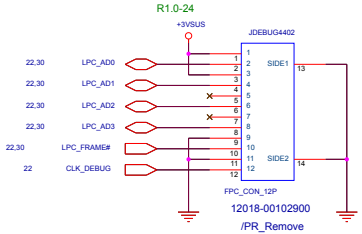
eDP Switch



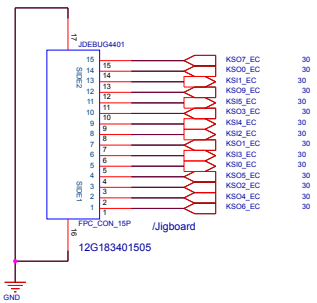
HDMI Switch



LPC Debug Port

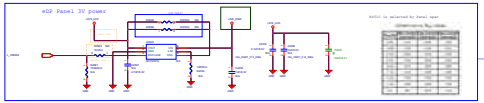


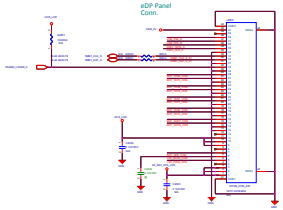
2016/03/21

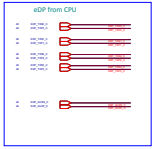


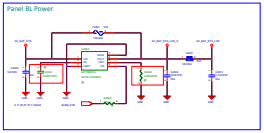
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DEBUG_LPC		
	Engineer: EE		
Size: A	Project Name: GM501GS		Rev: 2.1
Date: Wednesday, January 17, 2018	Sheet 44 of 102		

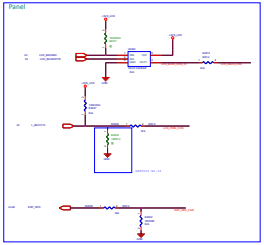

eDP Panel 3V power

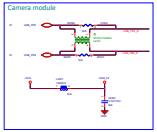

eDP Panel
Conn.

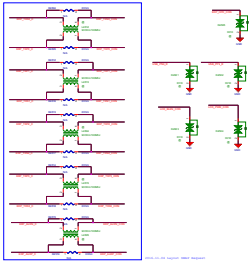

eDP from CPU


Panel BL Power


MIC

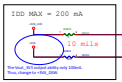

Panel


Camera module


For EMI


Title
CRT_eDP
Size
Custom
Document Number
CRT0001A
Rev
1.0
Date:
Sheet
of

UX370UAF Refresh Change with redriver 版本 TUSB546-DCI



HSD90
R1.1 將&Google漏電問題+3VS_MUX改open drain 0310
R1.2 MUX power change to +3VS_MUX改回touch pull
R1.2 +3VS_MUX change to +VOUT3V3

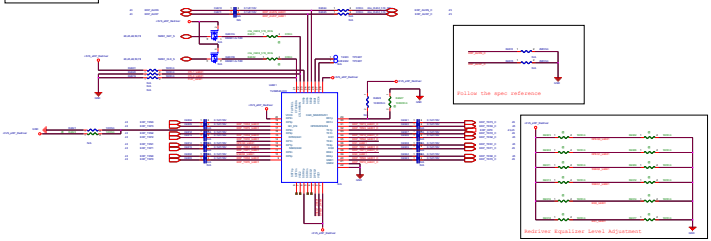


Table 7. TUSB546-DCI Receiver Equalization GPIO Control

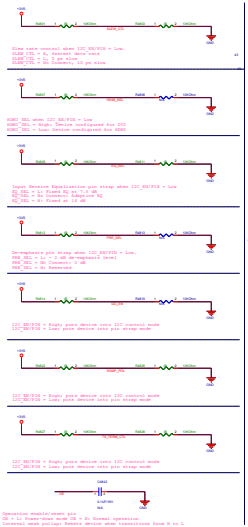
Equalization Setting #	USB3 – Channel Insertion Loss at 4 GHz			USB 2.0 and Shared Channel Path			ALL BUT DP++/HDMI Cables		
	4.5-dB Slot (dB)	Equalizer Gain (dB)	PEI Data at 4 GHz (dB)	Source Side (dB)	Sink Side (dB)	Slot Data at 4 GHz (dB)	Source Side (dB)	Sink Side (dB)	Slot Data at 4 GHz (dB)
0	0	0	0	0	0	0	0	0	0
1	0	1.5	1.5	0	1.5	1.5	0	1.5	1.5
2	0	3	3	0	3	3	0	3	3
3	0	4.5	4.5	0	4.5	4.5	0	4.5	4.5
4	0	6	6	0	6	6	0	6	6
5	0	7.5	7.5	0	7.5	7.5	0	7.5	7.5
6	0	9	9	0	9	9	0	9	9
7	0	10.5	10.5	0	10.5	10.5	0	10.5	10.5
8	1	0	1	1	0	1	1	0	1
9	1	1.5	2.5	1	1.5	2.5	1	1.5	2.5
10	1	3	4	1	3	4	1	3	4
11	1	4.5	5.5	1	4.5	5.5	1	4.5	5.5
12	1	6	7	1	6	7	1	6	7
13	1	7.5	8.5	1	7.5	8.5	1	7.5	8.5
14	1	9	10	1	9	10	1	9	10
15	1	10.5	11.5	1	10.5	11.5	1	10.5	11.5

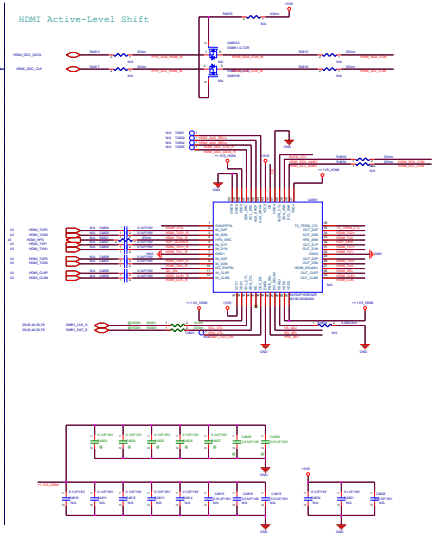
8.3.3 4-level Inputs

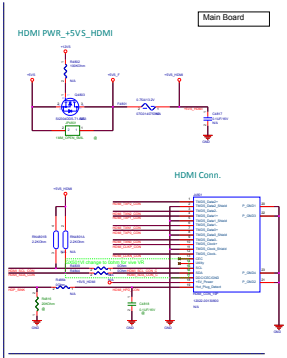
The TUSB546-DCI has I2C_EN, EQ1 (I), DPSEQ1 (I), and SSEQ1 (I) 4-level inputs pins that are used to control the equalization gain and place TUSB546-DCI into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There is an internal 30 kΩ pull-up and a 94 kΩ pull-down. These resistors, together with the external resistor connection combine to achieve the desired voltage level.

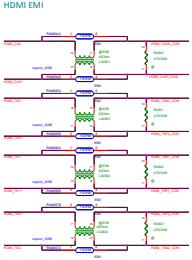
Table 8. 4-Level Control Pin Settings

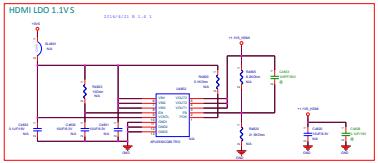
LEVEL	SETTINGS
0	Option 1: Tie 11kΩ 5% to GND Option 2: Tie directly to GND
R	Tie 20 kΩ 5% to GND
F	Float (leave pin open)
1	Option 1: Tie 11 kΩ 5% to V_{CC} Option 2: Tie directly to V_{CC}

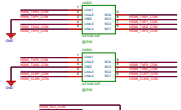


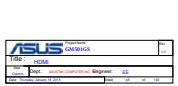

HDMI Active-Level Shift

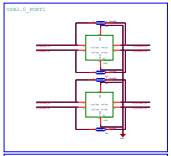

Main Board
HDMI PWR_+5VS_HDMI
HDMI Conn.

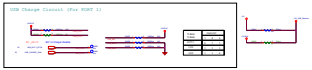

HDMI EMI

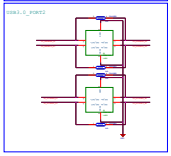

HDMI LDO 1.1VS

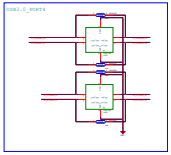


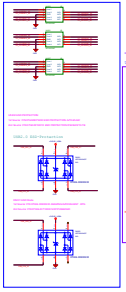

ASUS
Project Name: G3478KUS
Title: HDMI
Engineer:
Date: Thursday, January 09, 2014

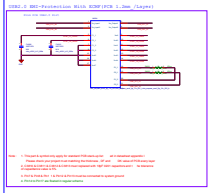

USB3.0_PORT1

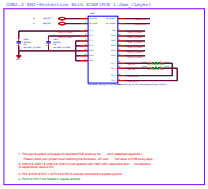

USB Charge Circuit (For PORT 1)

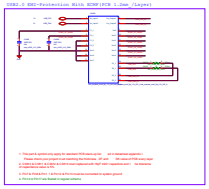

USB3.0_PORT2

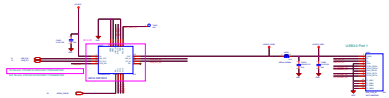

USB3.0_PORT3

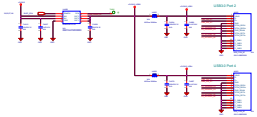

USB3.0 ESD+Protection
USB3.0 ESD+Protection

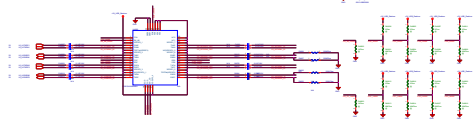

USB3.0 ESD+Protection With RCMP(PCB 1.2mm /Layer)

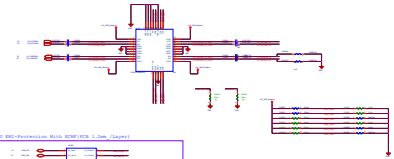

USB3.0 ESD+Protection With RCMP(PCB 1.2mm /Layer)


USB3.0 ESD+Protection With RCMP(PCB 1.2mm /Layer)


USB3.0 Port 1

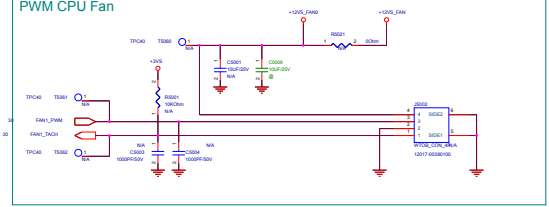

USB3.0 Port 2
USB3.0 Port 3



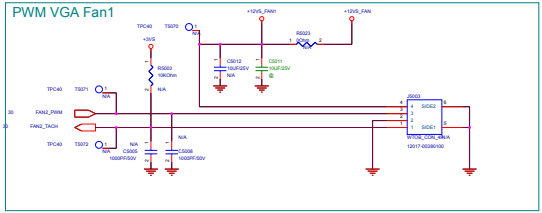


CHINAFIX

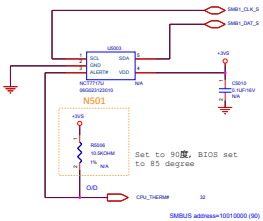
PWM CPU Fan



PWM VGA Fan1

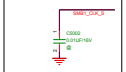


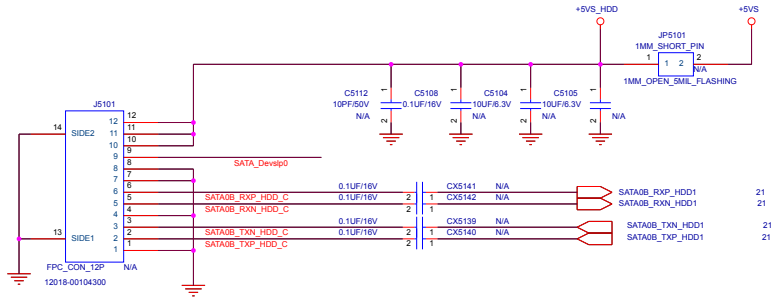
CPU Thermal Sensor

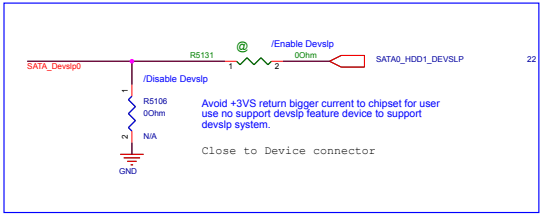


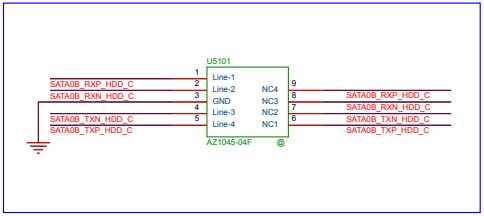
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Reserve for
powr noise









<Variant Name>

ASUSTeK COMPUTER INC. NB1

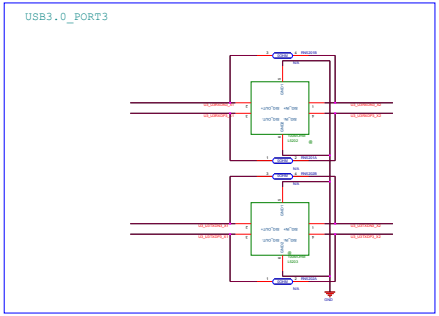
Title : XDD_HDD & ODD CON

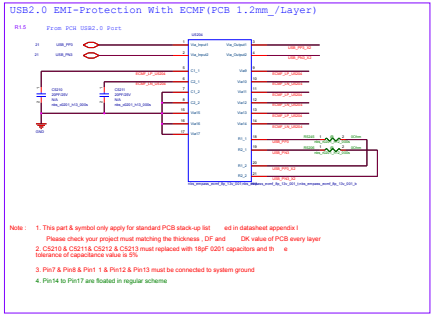
Engineer: EE

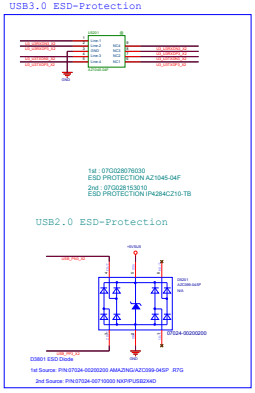
Size	Project Name	Rev
A	GL703VS	2.1

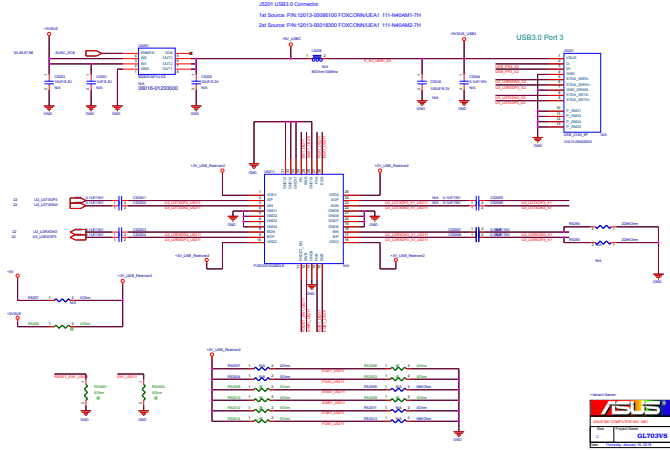
Date: Thursday, January 18, 2018 Sheet 51 of 102

Main Board

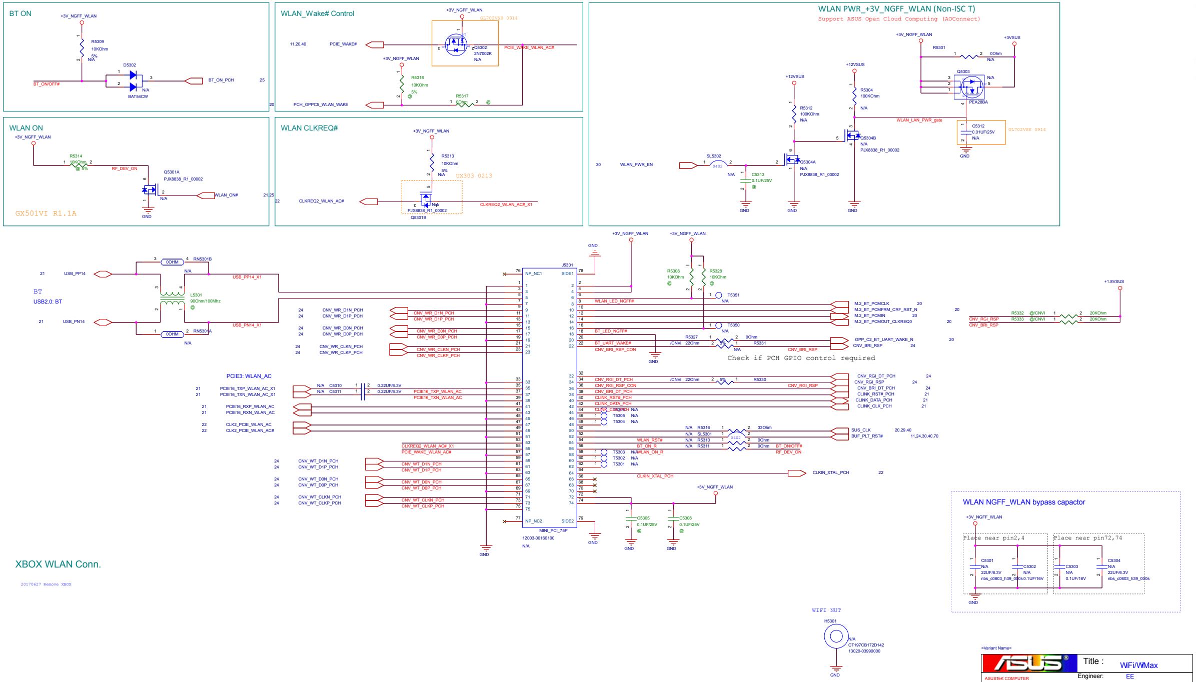

USB3.0_PORT3


USB2.0 EMI-Protection With ECMF(PCB 1.2mm_/Layer)
R15
From PCH USB2.0 Port
Note : 1. This part & symbol only apply for standard PCB stack-up list ed in datasheet appendix I
Please check your project must matching the thickness _DF and DK value of PCB every layer
2. CS210 & CS211& CS212 & CS213 must replaced with 18pF 0201 capacitors and th e tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin1 1 & Pin12 & Pin13 must be connected to system ground
4. Pin14 to Pin17 are floated in regular scheme


USB3.0 ESD-Protection
1st : 07020280760300
ESD PROTECTION AZ1045-04F
2nd : 07002B153010
ESD PROTECTION IP4284CZ10-TB
USB2.0 ESD-Protection
07024-00200200
D3801 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP .R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2A4Q


JS201 USB3.0 Connector
1st Source: P/N:10013-00080100 FOXCONN/UEA1 111-N4GAM1-7H
2nd Source: P/N:10013-00018D00 FOXCONN/UEA1 111-N4GAM2-7H
USB3.0 Port 3


Title : USB Charger
Engineer:
GL703VS



<Variant Name>

ASUS

Title : WiFi/WMax

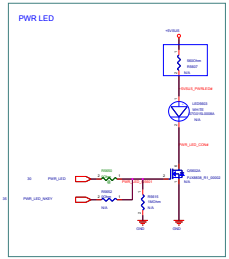
ASUSTeK COMPUTER

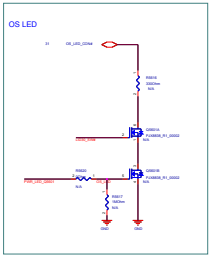
Engineer: EE

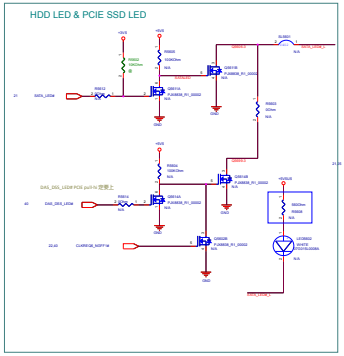
Size: Custom | Project Name: GM501GS | Rev: 2.1

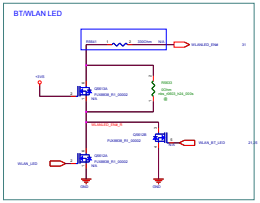
Date: Thursday, January 18, 2018 | Sheet 53 of 102

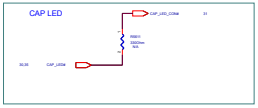
Main Board

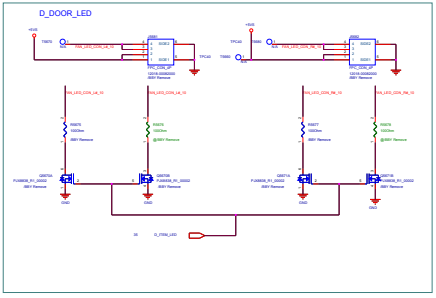


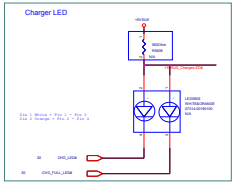


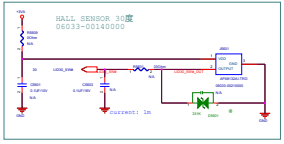


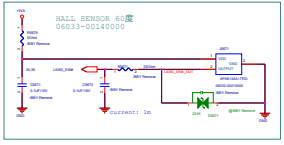






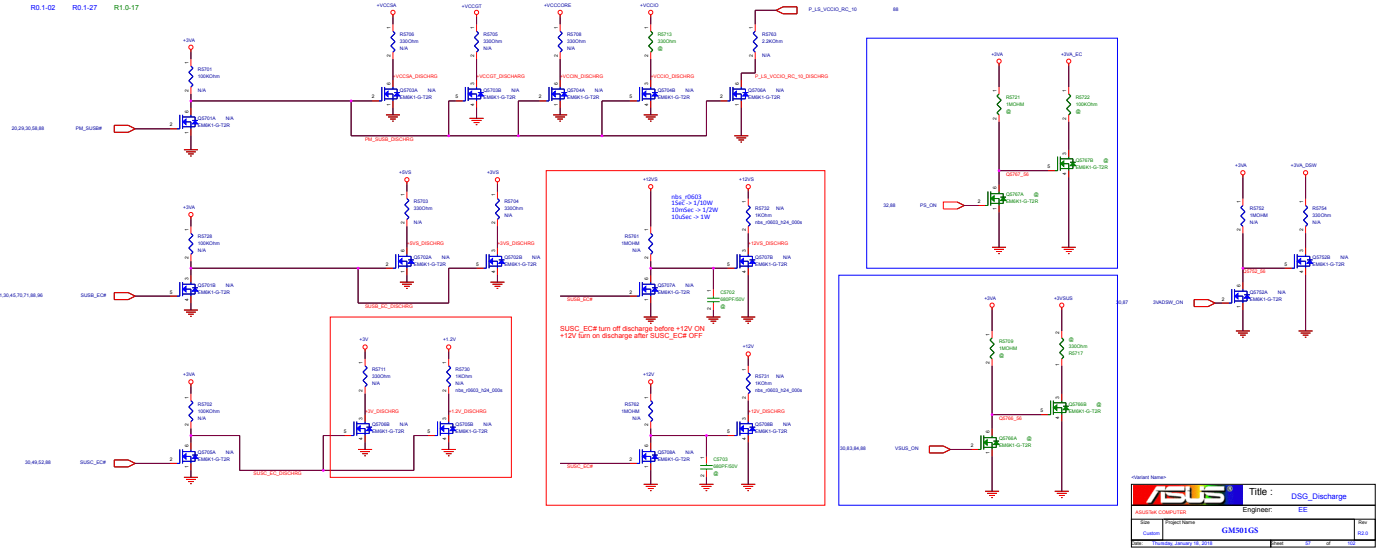


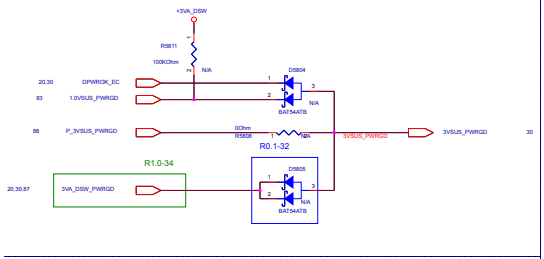


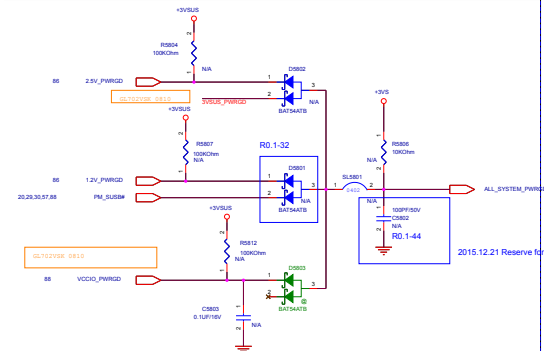


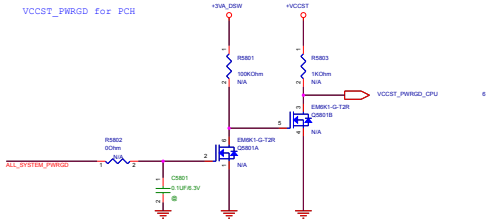
For Eagle Eye LED CTRL

ASUS Compal Electronics			Rev
Title : LED Indicator			
Size	Dept.	Engineer: EE	
Date: Thursday, January 29, 2015	Sheet 30 of 103		


R0.1-02
R0.1-27
R1.0-17
+VCCSA
+VCCGT
+VCCGTGRE
+VCCIO
P_LS_VCCIO_RC_10
+3VA
R3701
100KOhm
N/A
Q3701A
N/A
SI3865K1-G-T2R
20,29,30,58,88
PM_SUSB#
VCCSA_DISCHRG
VCCGT_DISCHRG
VCCIN_DISCHRG
VCCIO_DISCHRG
P_LS_VCCIO_RC_10_DISCHRG
PM_SUSB_DISCHRG
R3706
330Ohm
R3705
330Ohm
R3708
330Ohm
R3713
33KOhm
R3763
2.2KOhm
Q3702A
Q3703B
Q3704A
Q3704B
Q3706A
+5VS
+3VS
R3703
330Ohm
R3704
330Ohm
R3738
100KOhm
Q3701B
6,11,30,43,70,71,88,96
SUSB_EC#
5VS_DISCHRG
3VS_DISCHRG
SUSB_EC_DISCHRG
Q3702A
Q3703B
+3V
+1.2V
R3711
330Ohm
R3730
1MOhm
mlw_r0603_N24_500x
3V_DISCHRG
+1.2V_DISCHRG
R3702
100KOhm
Q3705A
30,49,52,88
SUSC_EC#
SUSC_EC_DISCHRG
Q3705B
SUSC_EC# turn off discharge before +12V ON
+12V turn on discharge after SUSC_EC# OFF
+12VS
+12V
nbs_r0603
1S4C -> 1/10W
10mSec -> 1/2W
10uSec -> 1W
R3761
1MOhm4
R3732
N/A
R3731
N/A
+5VS_DISCHRG
+12V_DISCHRG
Q3707A
Q3707B
CS702
1800PF-50V
CS703
R3762
1MOhm4
Q3708A
Q3708B
+3VA_EC
R3721
1MOhm
R3722
100KOhm
Q3707_S6
Q3707A
Q3707B
32,88
PS_ON
+3VA_DSW
R3752
1MOhm
R3754
330Ohm
Q3702_S6
Q3702A
Q3702B
58,87
3VADSW_ON
+3VSUS
R3733
1MOhm
R3717
330Ohm
Q3706_S6
Q3706A
Q3706B
30,83,84,88
VSUS_ON
<Variant Name>
ASUSTeK COMPUTER
Title : DSG_Discharge
Engineer: EE
Size: Custom
Project Name: GM501GS
Rev: R2.0
Date: Thursday, January 15, 2015
Sheet 57 of 102





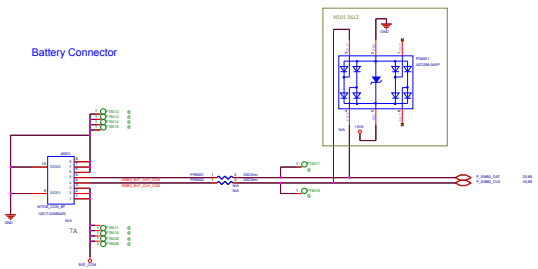


<Variant Name>

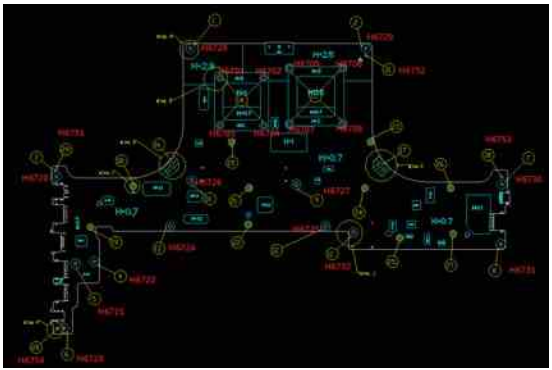
ASUSTeK COMPUTER	Title : Power Protect	
	Engineer: EE	
Size: Custom	Project Name: GM501GS	Rev: 2.1
Date: Thursday, January 18, 2018	Sheet 58 of 102	

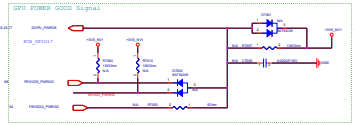
DC-IN Connector

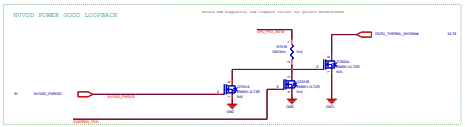
Battery Connector

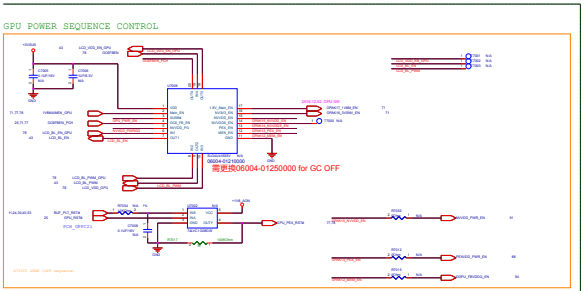


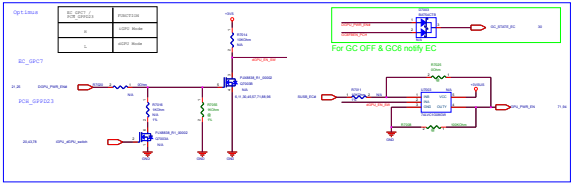
Title :	DC & BAT IN		
Engineer:			
Size:	Project Name:	GM501GS	Rev: 1.0
Date:	Thursday, January 19, 2012	Sheet	32 of 52

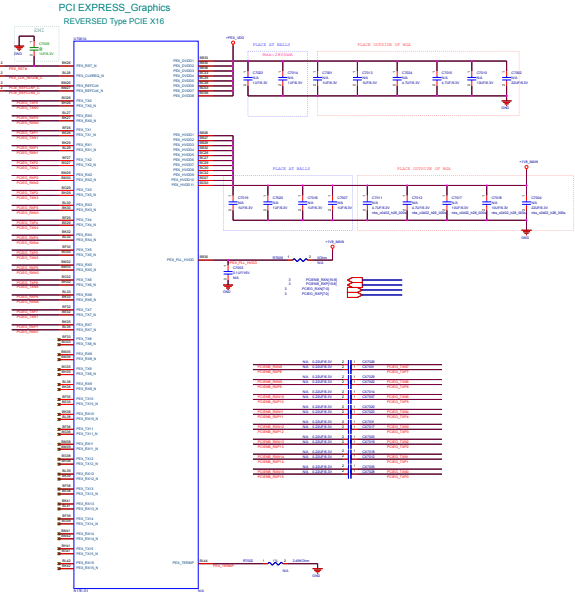



GPU POWER GOOD Signal


NVVDD POWER GOOD LOOPBACK

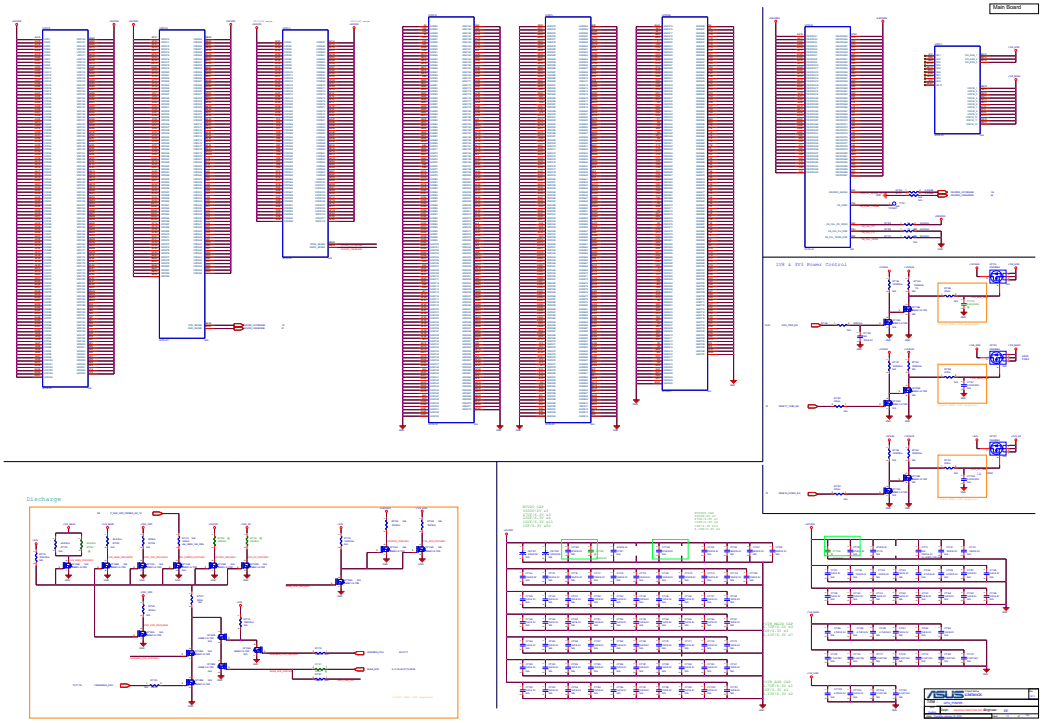

GPU POWER SEQUENCE CONTROL
06004-01250000
需更換06004-01250000 for GC OFF


For GC OFF & GC6 notify EC


PCI EXPRESS_Graphics
REVERSED Type PCIE X16

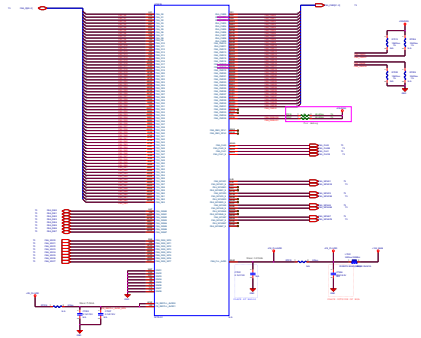

For EMI


ASUS
GM501GS
Title : GPU_PCIE dT
Engineer:
Thursday, January 30, 2020

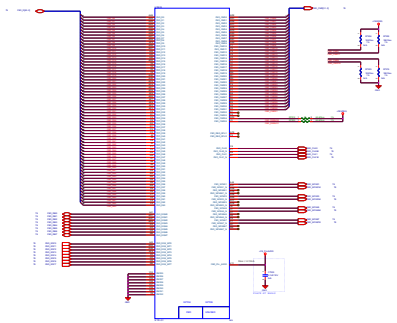

Main Board
USB & DVI Power Control
Discharge

Main Board

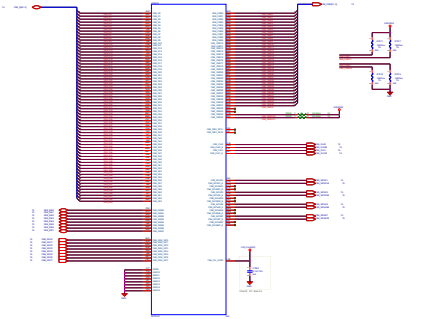
MEMORY: GPU FB Partition A



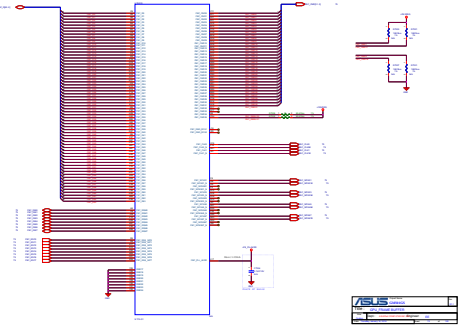
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B



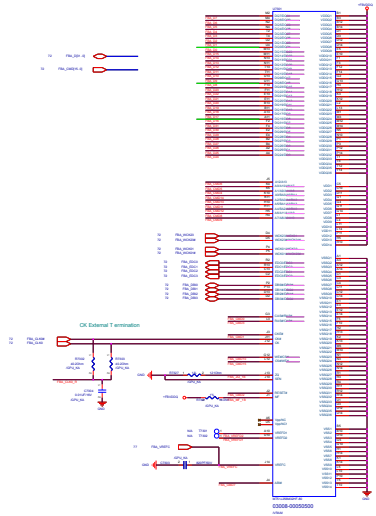
MEMORY: GPU FB Partition C



Main Board

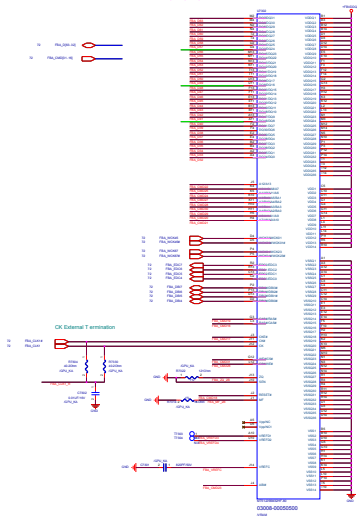
FBA Partition Memory (1 of 2)

MF=1 Mirror



FBA Partition Memory (2 of 2)

MF=0 Normal



USE GDDR5 VRAM 128Bits x 32 (512MB)

1st P/N:03008-00320103 H5TQ2G63DFR-T2C (M-die) ,Strap: 0 x2

2nd P/N:03008-00330400 SAMSUNG K4W1G2F5C-HC03 ,Strap: 0x3

3rd P/N:03008-00330400 Micron(EDW4032BABG-60-F ,B-die) ,Strap: 0x4

GDD5 MODE SELECTION

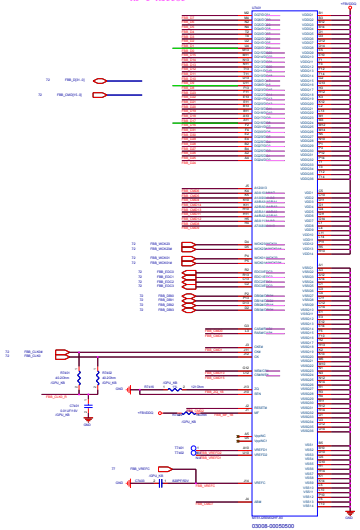
MR0	MR1	MR2	MR3
x32	0	0	0x00
x32	0	0x04	0x00
x16, Interleave	0x40	0x04	0
x16, non-Interleave	0x40	0x24	0x00

Title :	VRAM-CHANNEL A		
Engineer :	EE		
Size :	Document Number :		Rev :
C	G2M5XG5		
Date : 10/Friday, January 08, 2010	Sheet 14 of 45		

Main Board

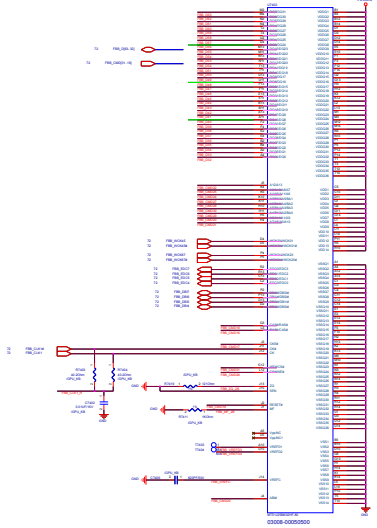
FBB Partition Memory (1 of 2)

MF=1 Mirror



FBB Partition Memory (2 of 2)

MF=0 Normal



R13-02 R12-25

USE GDDR5 VRAM 128Bit x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3rd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MA[12]	MF	EDC1	EDC0
H,M	H	VDD[Q]	VDD[Q]
H,M	L	VDD[Q]	VDD[Q]
L,M	H	VDD[Q]	X
L,M	L	VDD[Q]	VDD[Q]

Title : VRAM-CHANNEL B

Engineer: RK

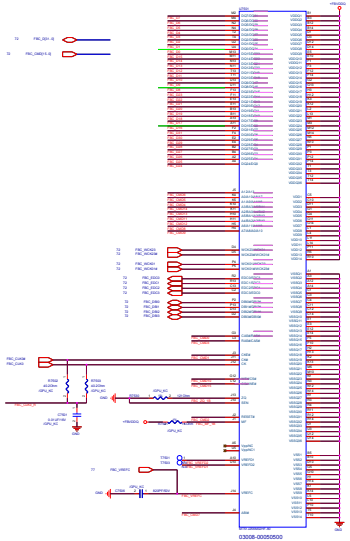
Size: C | Project Name: E326G05-GS | Rev:

Date: 2014/10/06 | Sheet 1 of 10

Main Board

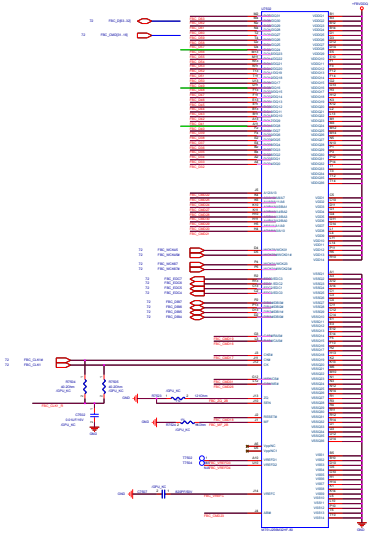
FBC Partition Memory (1 of 2)

MF=1 Mirror



FBC Partition Memory (2 of 2)

MF=0 Normal



1H-3458 01-2-23

USE GDDR5 VRAM *2(8Bit) x 32 (512M)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (fill-dot) ,Strap: 0 x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3rd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (fill-dot) ,Strap: 0x4

GDD5 MODE SELECTION

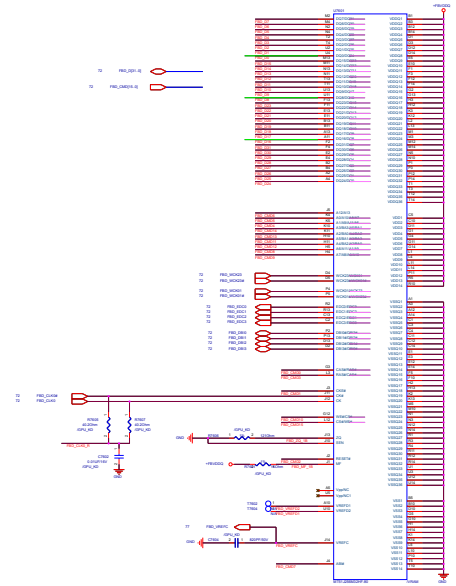
MODE	A8	BA1	BA0
x32	0	VDDQ	VDDQ
x32	1	VDDQ	VSSQ
x16 terminated	VSSQ	VDDQ	0
x32 terminated	VSSQ	VDDQ	VSSQ

ASUS	Project Name: G1S/G1GS		Rev: 1.1
Title:	VRAM-CHANNEL C		
Size:	Document Number:	Engineer:	EE
Date: Wednesday, January 07, 2015		Sheet: 15 of 50	

Main Board

FBD Partition Memory (1 of 2)

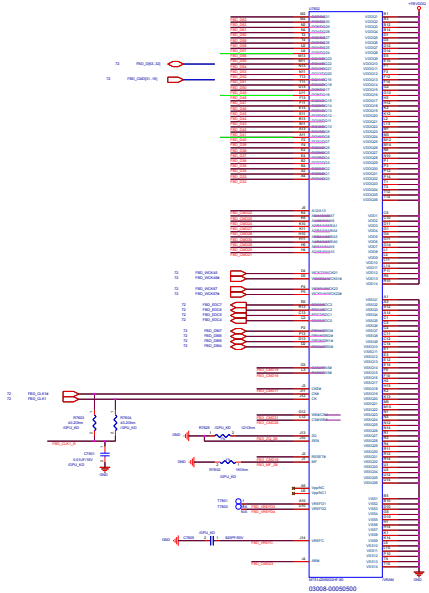
MF=1 Mirror



03008-00050500

FBD Partition Memory (2 of 2)

MF=0 Normal



03008-00050500

R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0 x2

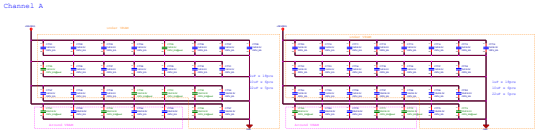
2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

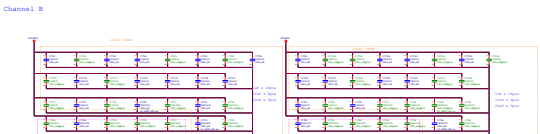
3nd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

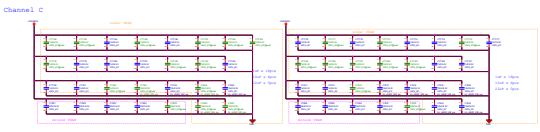
GDD5 MODE SELECTION

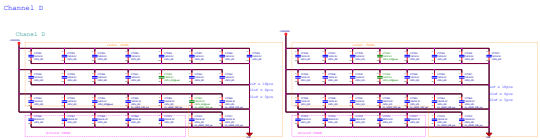
MA[10]	MF	EDC1	EDC3
H,M	0	0	VDDQ
L,M	0	VDDQ	VDDQ
H,M (terminate)	VDDQ	VDDQ	0
L,M (terminate)	VDDQ	VDDQ	VDDQ

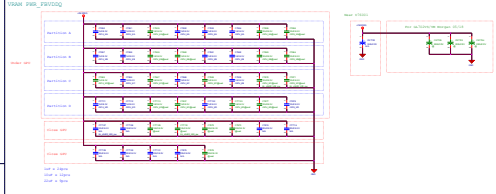
Project Name:	N15M-SGS	Rev:	2.1
Title:	VRAM-CHANNEL D		
Size:	Document Number:	Engineer:	EE
Date: Wednesday, January 27, 2010		Sheet: 15 of 100	

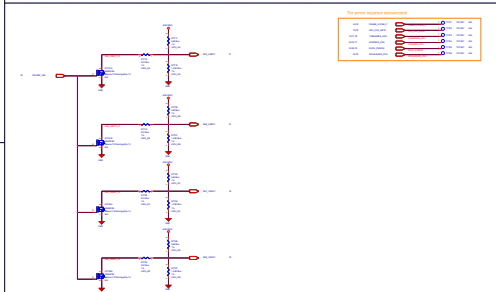

Channel A

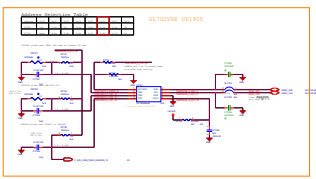

Channel B

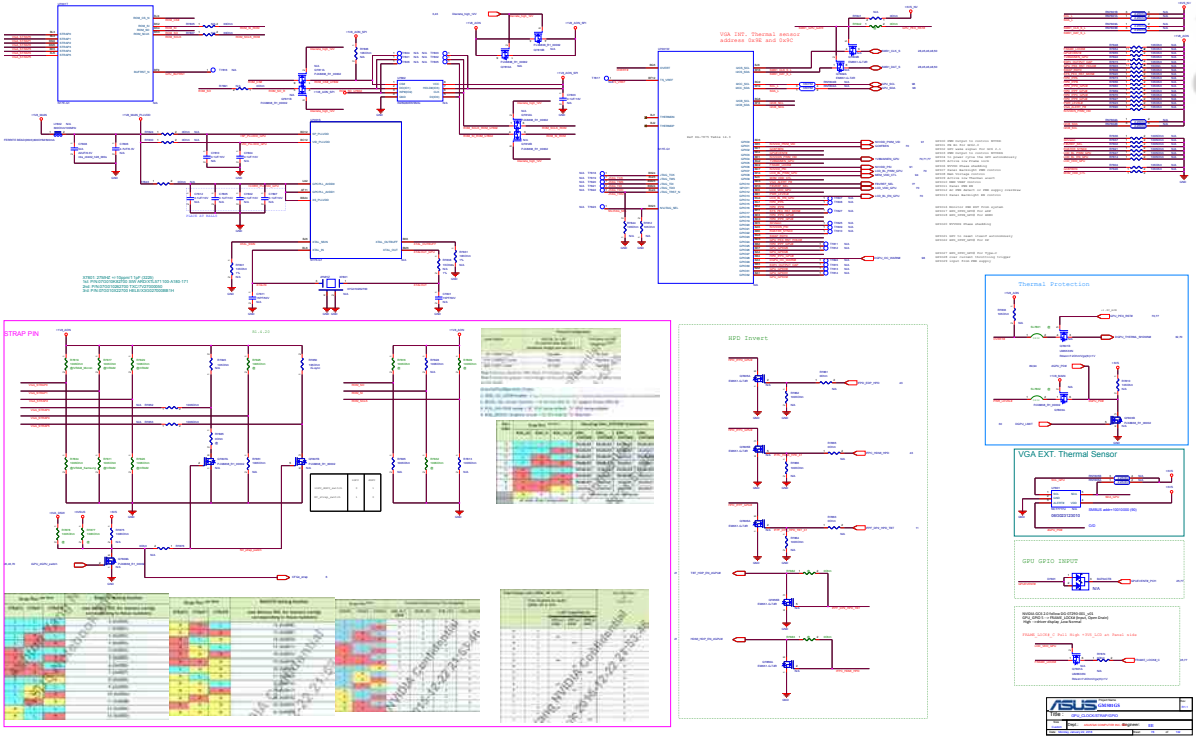

Channel C

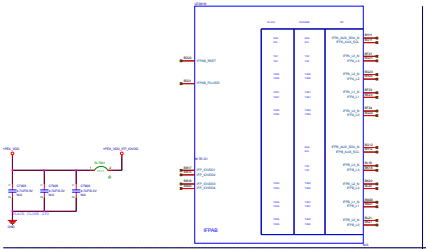

Channel D

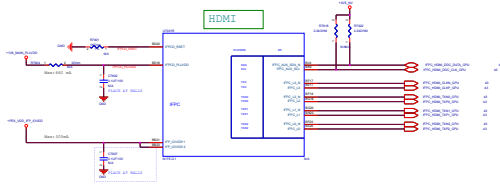

VRAM PWR_FBVDDQ

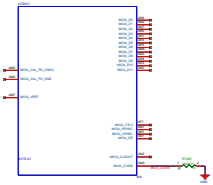


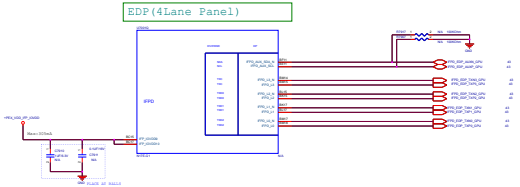

GL702VSK DP1905

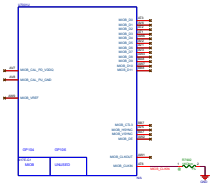

VGA INT. Thermal sensor address 0x98 and 0x9C
STRAP PIN
RPD Invert
Thermal Protection
VGA EXT. Thermal Sensor
GPU GPIO INPUT
ASUSTeK COMPUTER INC.

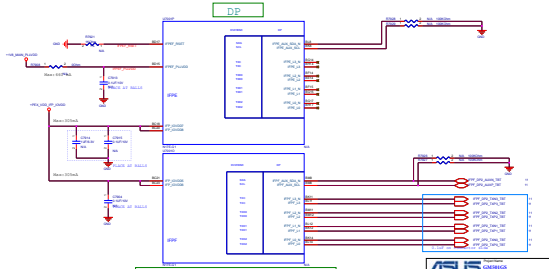


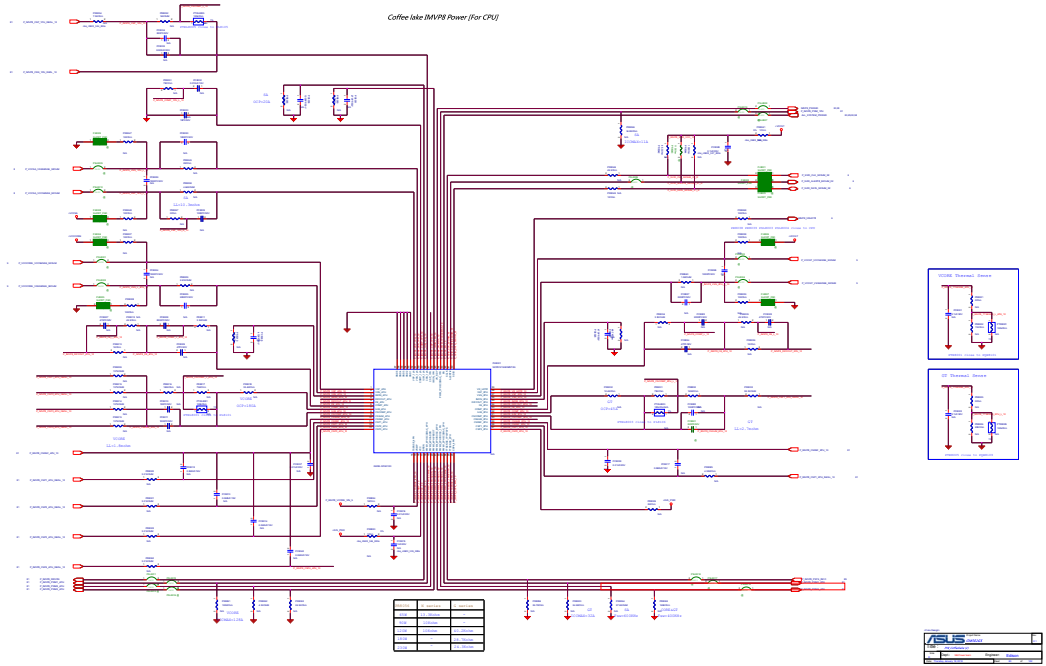

HDMI

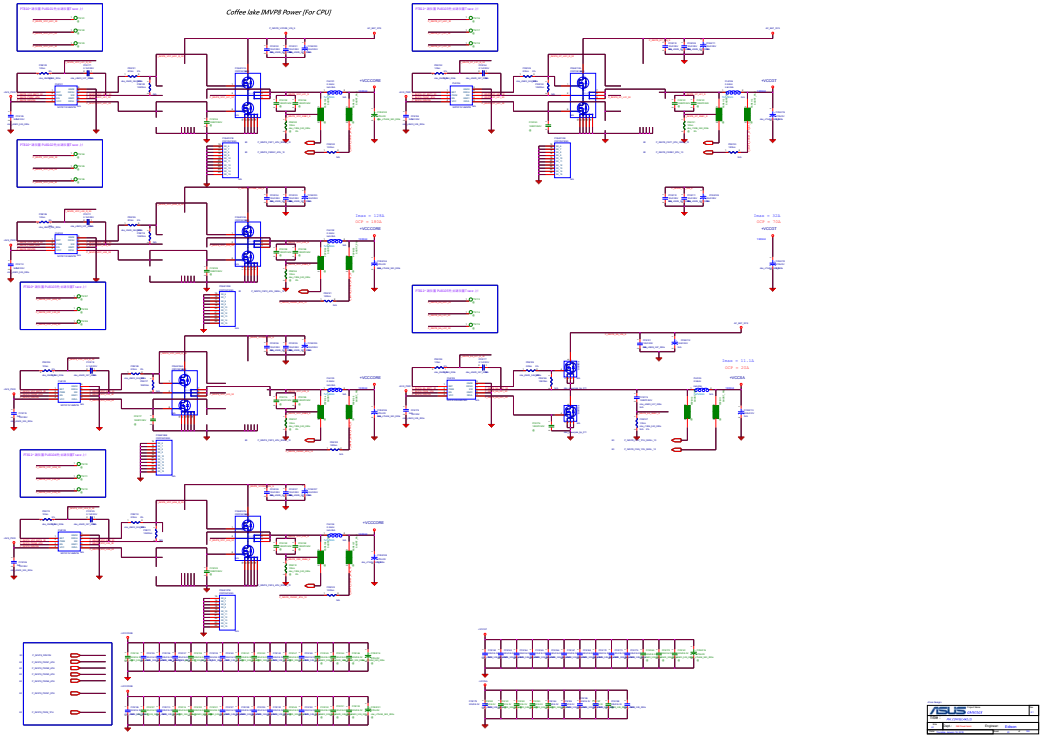



EDP(4Lane Panel)

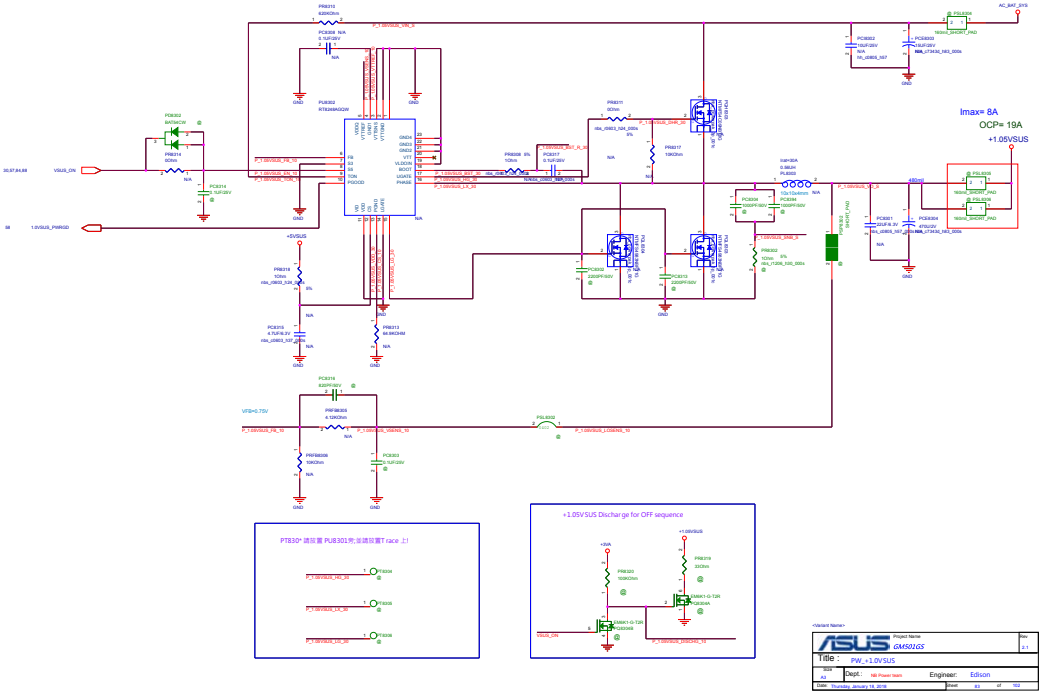



DP
DP(Intel Thunderbolt)

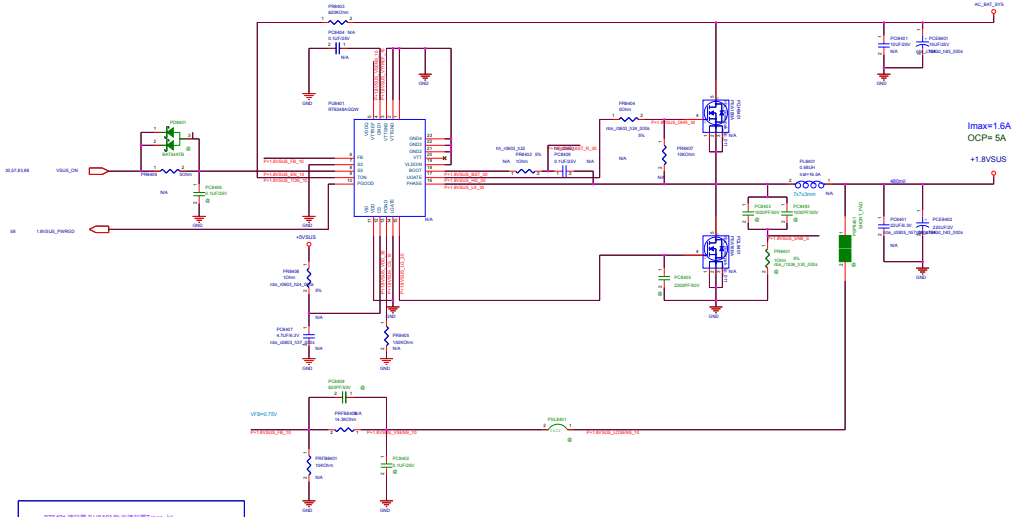

Coffee lake IMVP8 Power (For CPU)


Coffee lake IMVP8 Power [For CPU]

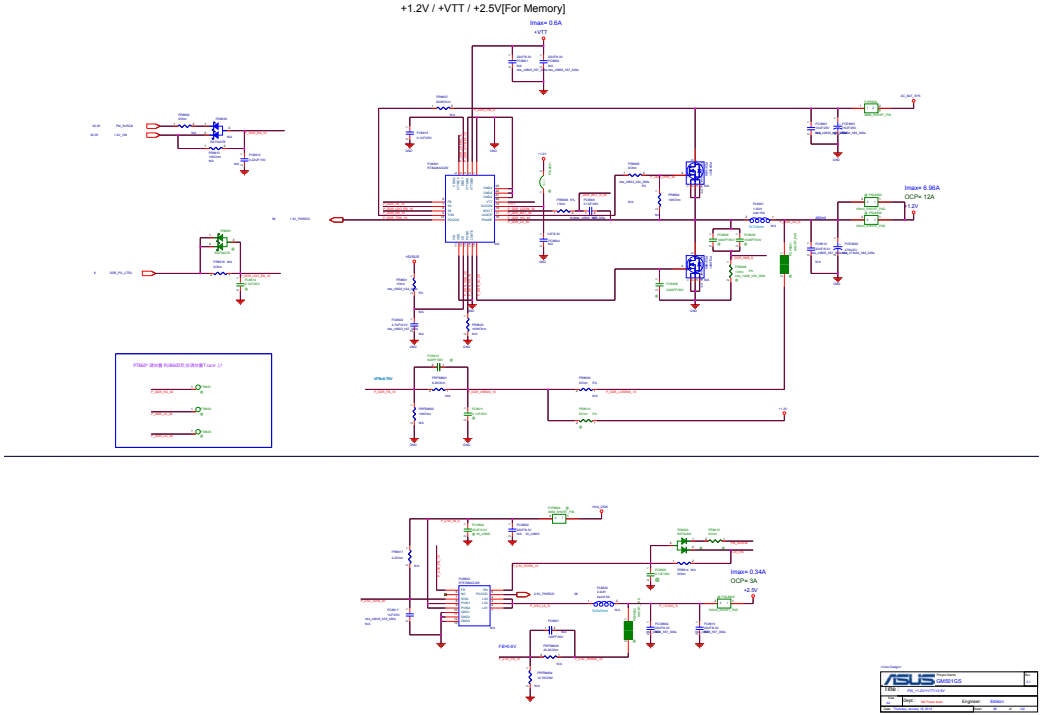
+1.05VSUS [For PCH]



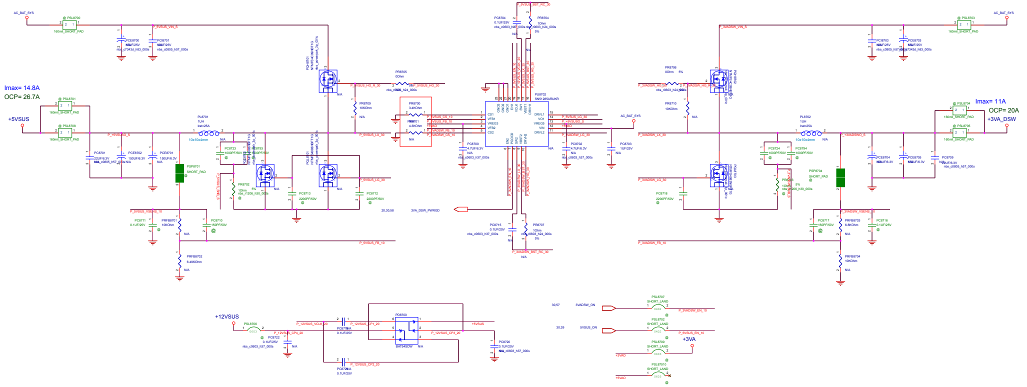
+1.8VSUS [For PCH]



<Variant Name>			
ASUS	Project Name: GM501GS		Rev: 2.1
Title : PW_+1.8VSUS			
Size: A3	Dept.: NB Power Sect.	Engineer: Edison	
Date: Thursday, January 16, 2018	Sheet: 84	of: 103	


+1.2V / +VTT / +2.5V[For Memory]
Imax= 0.6A
+VTT
Imax= 6.96A
OCP= 12A
+1.2V
Imax= 0.34A
OCP= 3A
+2.5V
ASUS
G4RD1GS

+3VA_DSW / +5VSUS [System Power]



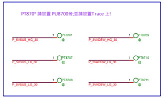
請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

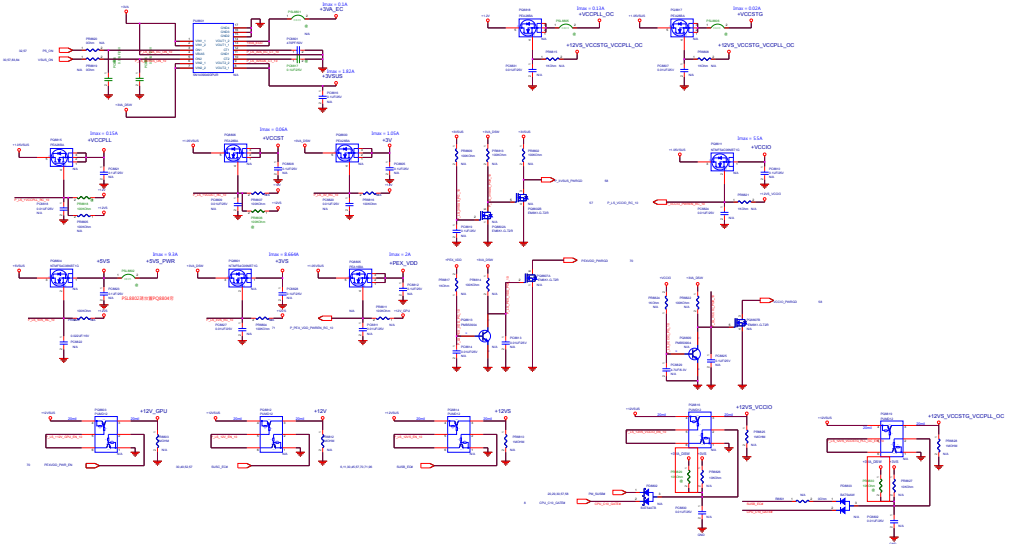


<Variant Name>

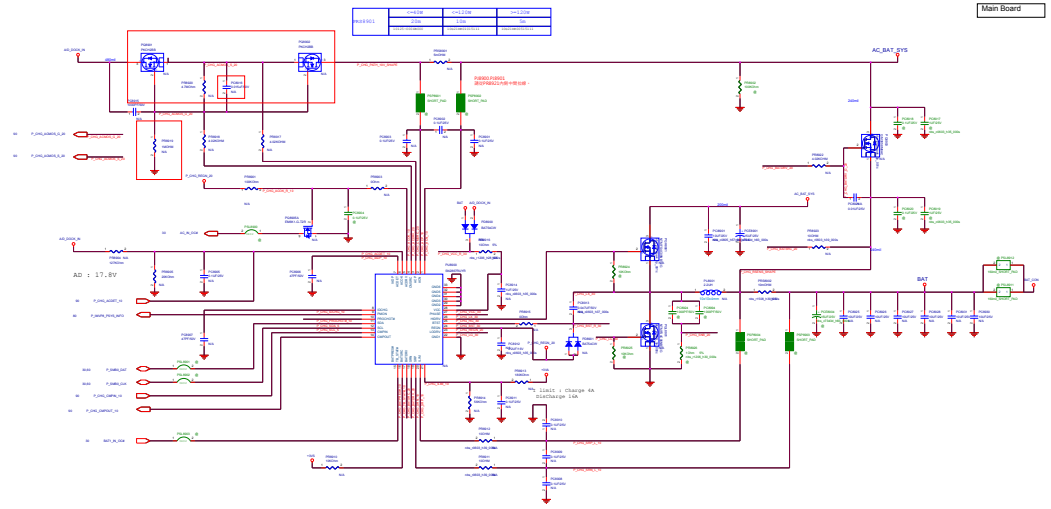
ASUS	Project Name: GM501GS	Rev: 2.1
Title : PW_+3VA_DSW/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Edison
Date: Thursday, January 18, 2018	Sheet 87	of 102

Load Switch

Main Board

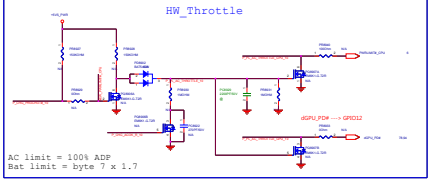


Title:	PIR_LOAD SWITCH		
Size:	Project Name: GM5GQGS		Rev:
Date: Thursday, January 09, 2014	Sheet:	of	
Dept.: AE Power team	Engineer: Eulleon		



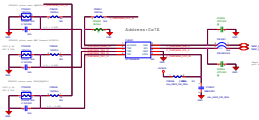
Adaptor select
total power = 90% ADP

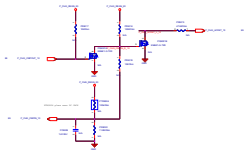
Adaptor select		
PR9931	110n	5m
PR993E		
14K	9.4V	30W
21.4K	9.8V	40W
56K	11.2V	45W
93.1K	11.6V	65W
150K	12.0V	75W
270K	12.4V	90W
560K	12.8V	120W

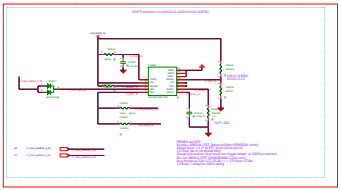


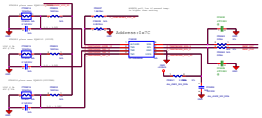
ASUS	Project Name: GM501GS		Rev: 1.0
Title: PM_CHARGER			
Size:	Project: GM501GS_Rev1.0.0	Engineer: Edison	
Date: Monday, January 09, 2016		Sheet: 40 of 74	


Address Selection Table
Register Address


Address=0x74



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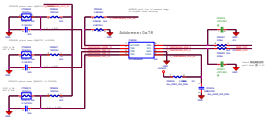
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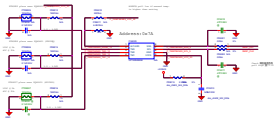
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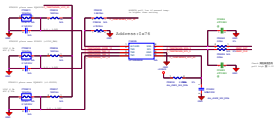
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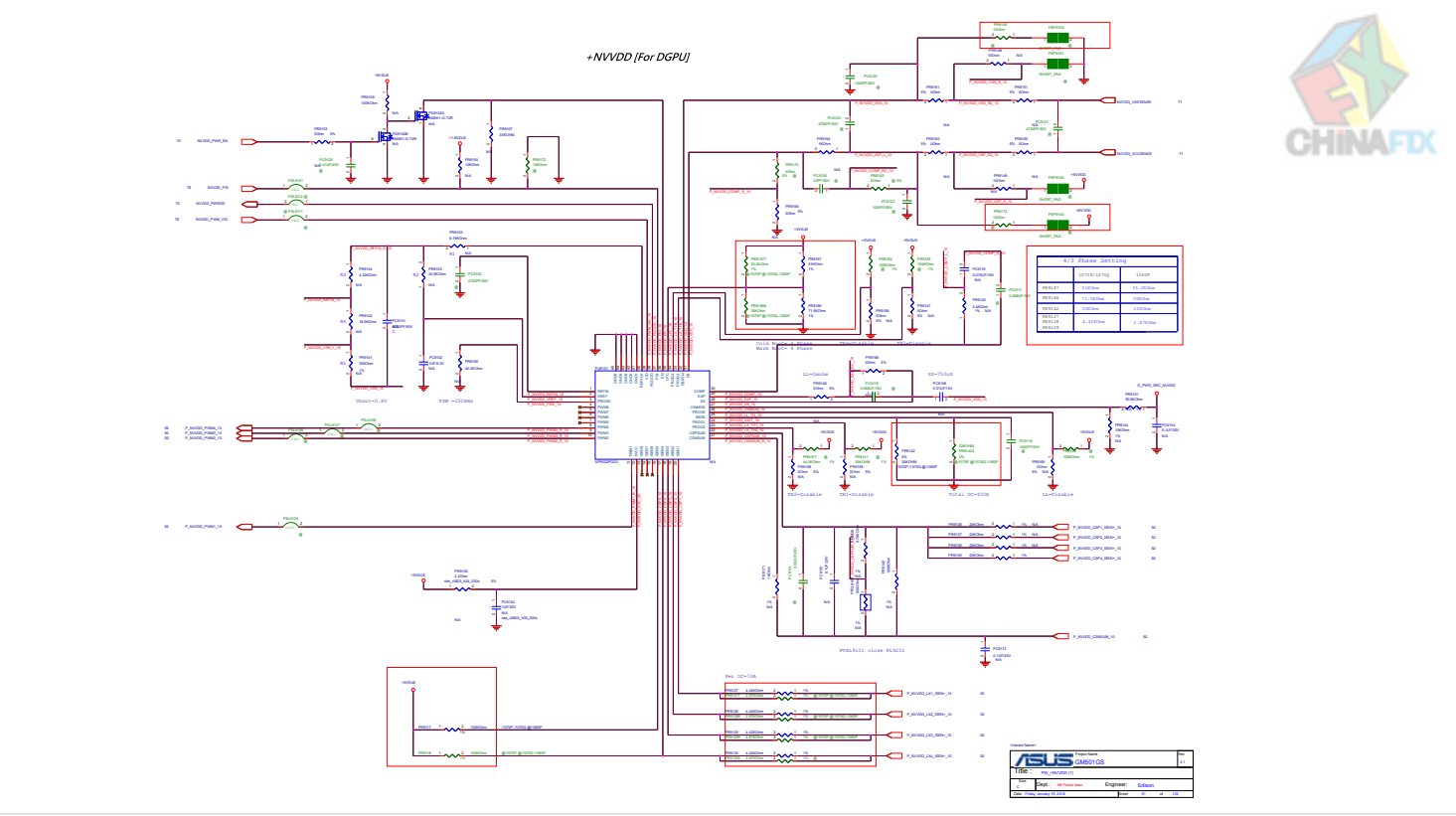
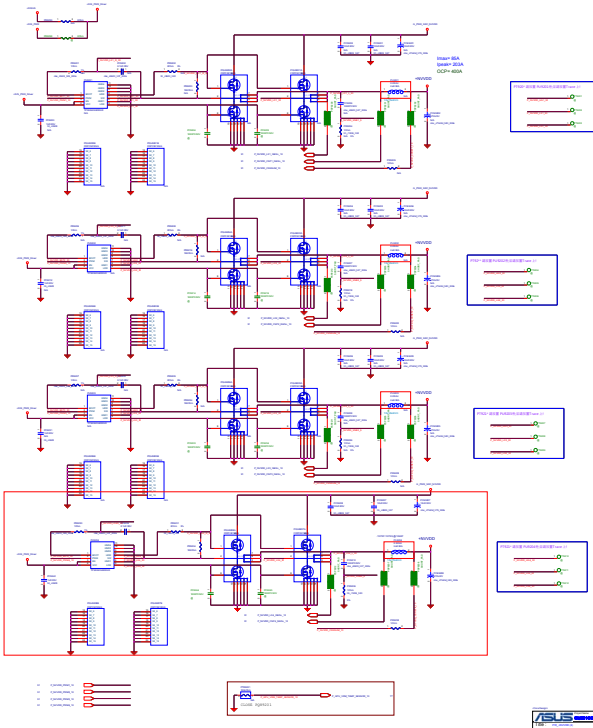
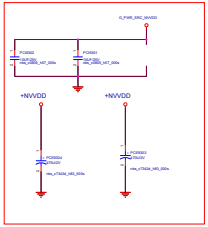

+NVVDD [For DGPU]
4/3 Phase Setting
GM501 QS
Project Name
Title : PWR_NVVDD (1)
Size : A3
Dept. : MB Power team
Engineer: Edison
Date : Friday, January 15, 2016
Sheet 50 of 102

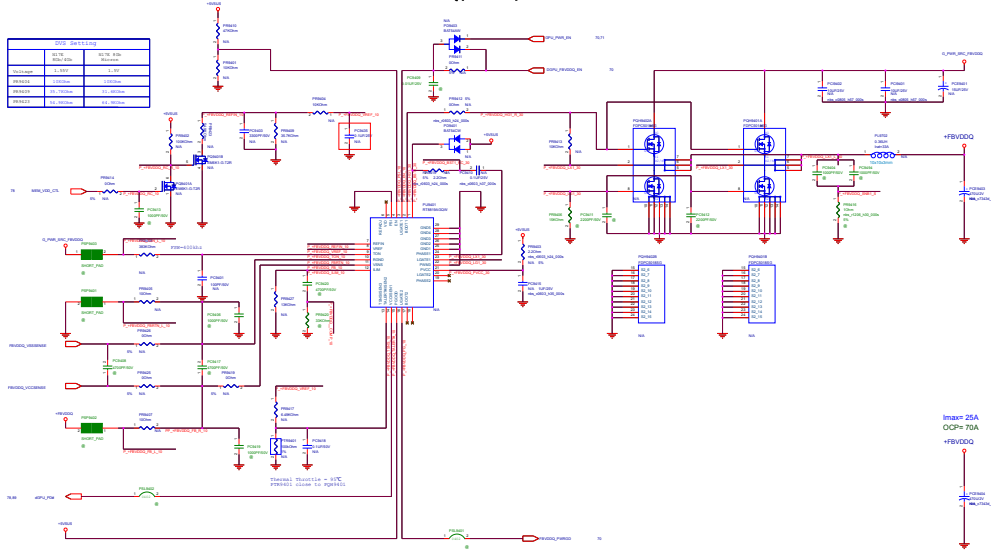
+NVVDD [For DGPU]

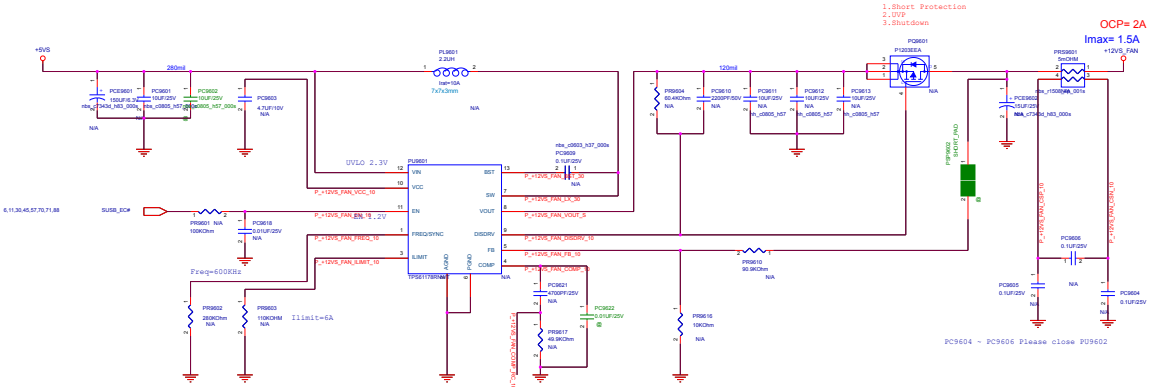


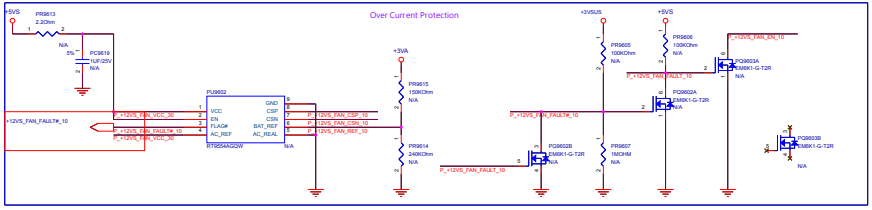
+NVVDDS [For DGPU +NVVDD combine]



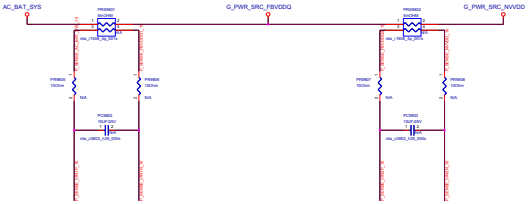
+FBVDDQ [For VRAM]

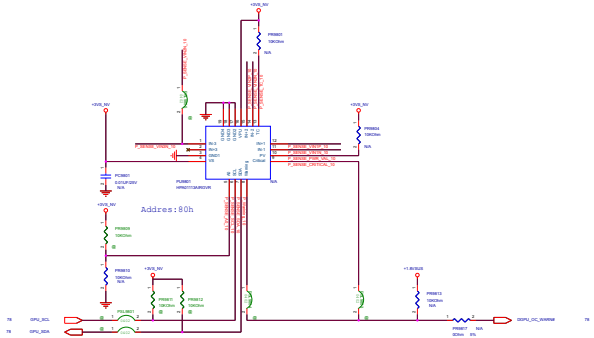



1.Short Protection
2.UVP
3.Shutdown
OCP= 2A
Imax= 1.5A
+5VS
+12VS_FAN
280mil
120mil
PL9601
2.2UH
Imax=10A
7x7x3mm
PQ9601
P1203EEA
PR9601
5mOHM
PJP9602
SHORT_PAD
UVLO 2.3V
UVLO 2.2V
PU9601
TPS61178RNMR
VIN
VCC
EN
FREQ/SYNC
ILIMIT
BST
SW
VOUT
DISDRV
FB
COMP
GND
PGND
SUSB_EC#
Freq=600KHz
Ilimit=6A
PC9604 ~ PC9606 Please close PU9602


Over Current Protection
+5VS
+3VA
+3VSUS
PU9602
RT9504AGSP
+12VS_FAN_FAULT#_10
PQ9602A
PQ9602B
PQ9603A
PQ9603B
PT970* 請放置 PU9701旁;並請放置T race 上!
PT9601
PT9602

ASUS
GM501GS
Title : PW_+12VS_FAN
Dept.: NB Power team
Engineer: Edison
Thursday, January 18, 2018

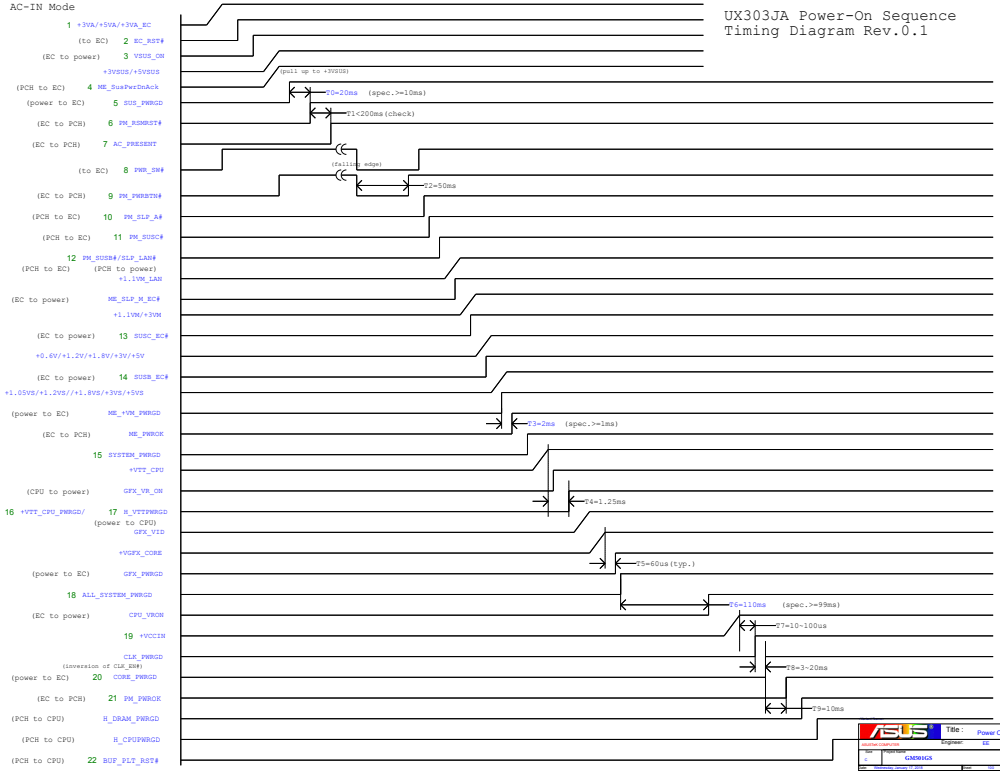




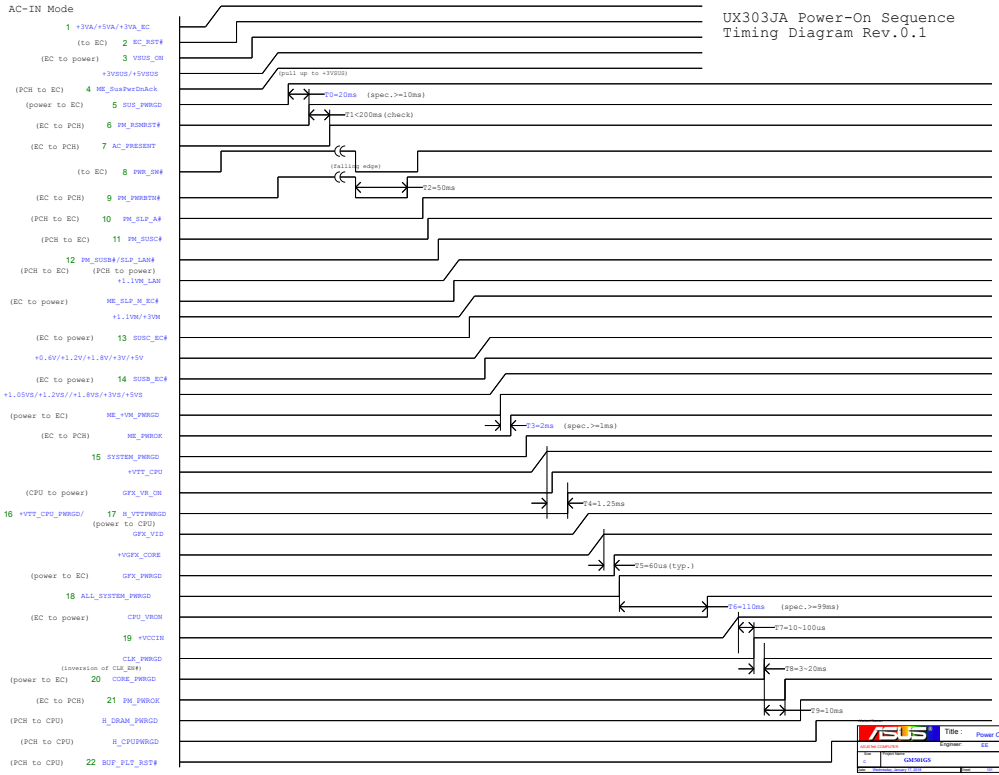
<Variant Name>

ASUS	Project Name: GM501GS	Rev: 1.0
Title: PW_IPC		
Size: Custom	Project: Power Team	Engineer: Edison
Date: Thursday, January 19, 2017	Sheet: 90 of: 100	

UX303JA Power-On Sequence Timing Diagram Rev.0.1



UX303JA Power-On Sequence Timing Diagram Rev.0.1



Rev.	Date	Description
A00	2025-08-01	Initial release

Rev.	Date	Description
A00	2025-08-01	Initial release

Rev.	Date	Description
A00	2025-08-01	Initial release

Rev.	Date	Description
A00	2025-08-01	Initial release