MS-7715 Ver:11

CPU

AMD M3 Phenom/Athlon 64 FX AM3

System Chipset

AMD RX780

ATI SB710

On Board Chip

FINTEK Super I/O -- F71889ED

LAN -- RTL8111EL

HD Codec --ALC887 Colay ALC892

BIOS -- SPI ROM 8M

Clock Generator

Controller--RTM880N-793

PWM

Controller--Intersil ISL6323 4+1 Phase
Vcore 4 Phase (MOS HIGHX2 LOWX2)
Vnb 1 Phase (MOS HIGHX1 LOWX2)

Main Memory

DDR III X 2 (Max 8GB)

Expansion Slots

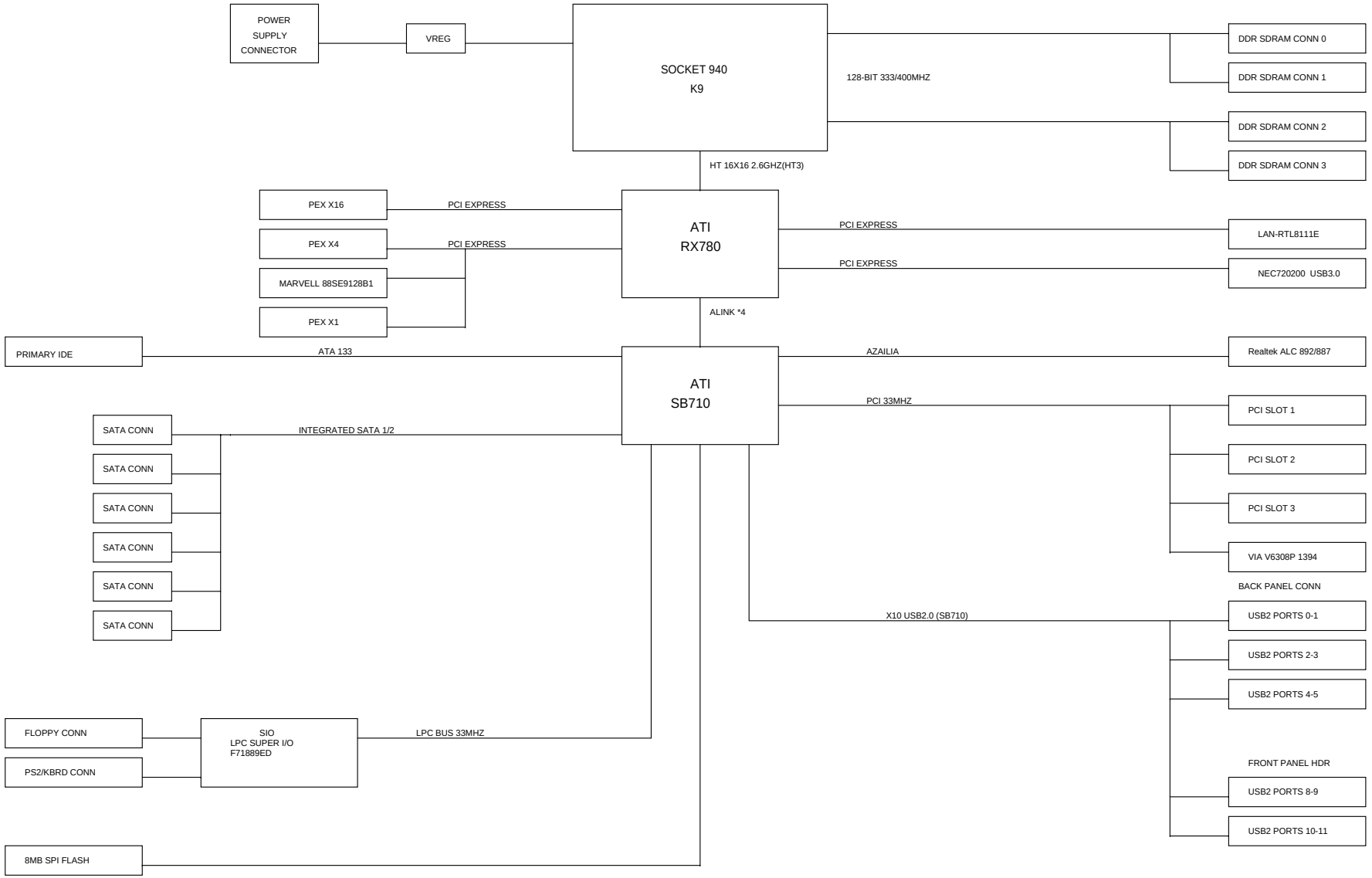
PCI-E X 16*1

PCI-E X 1 *1,2,3

PCI 2.2 Slot 1,2

CFG & BOM table:		
601-7715-010	for net use	CFG-7715V10-net
601-7715-020	for channell use	CFG-7715V10-channel

BLOCK DIAGRAM



Micro Star Restricted Secret		
Title: Block Diagram		Rev: 10
Document Number: MS-7715		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Monday, October 11, 2010	
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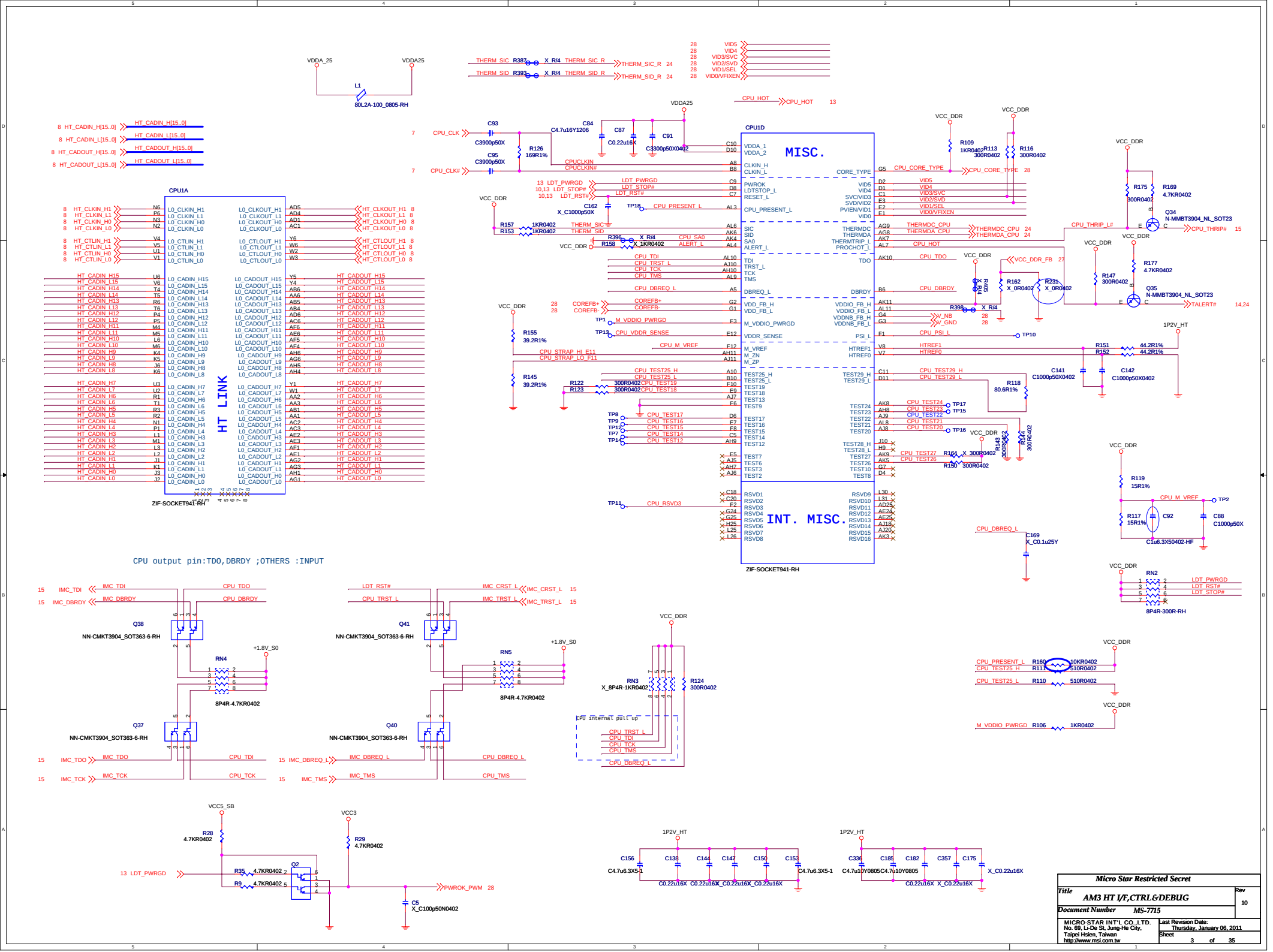
CPU1A
HT LINK
ZIF-SOCKET941-RH
CPU1D
MISC.
INT. MISC.
ZIF-SOCKET941-RH
CPU output pin:TDO,DBRDY ;OTHERS :INPUT
Micro Star Restricted Secret
Title
AM3 HT I/F,CTRL&DEBUG
Rev
10
Document Number
MS-7715
MICRO-STAR INT'L CO.,LTD.
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Taipei Hsien, Taiwan
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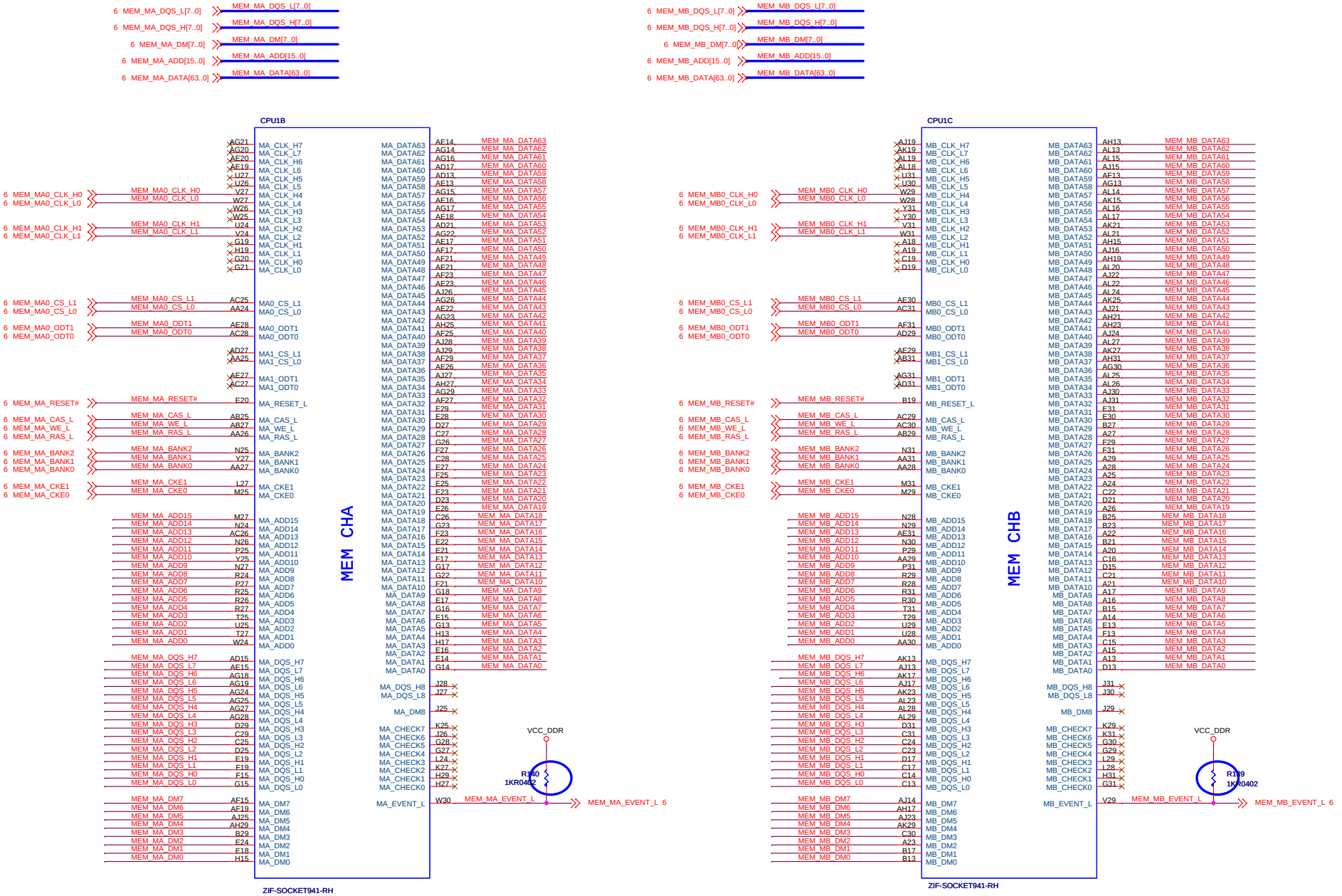

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Title	AM3 DDR MEMORY I/F
Rev	10
Document Number	MS-7715

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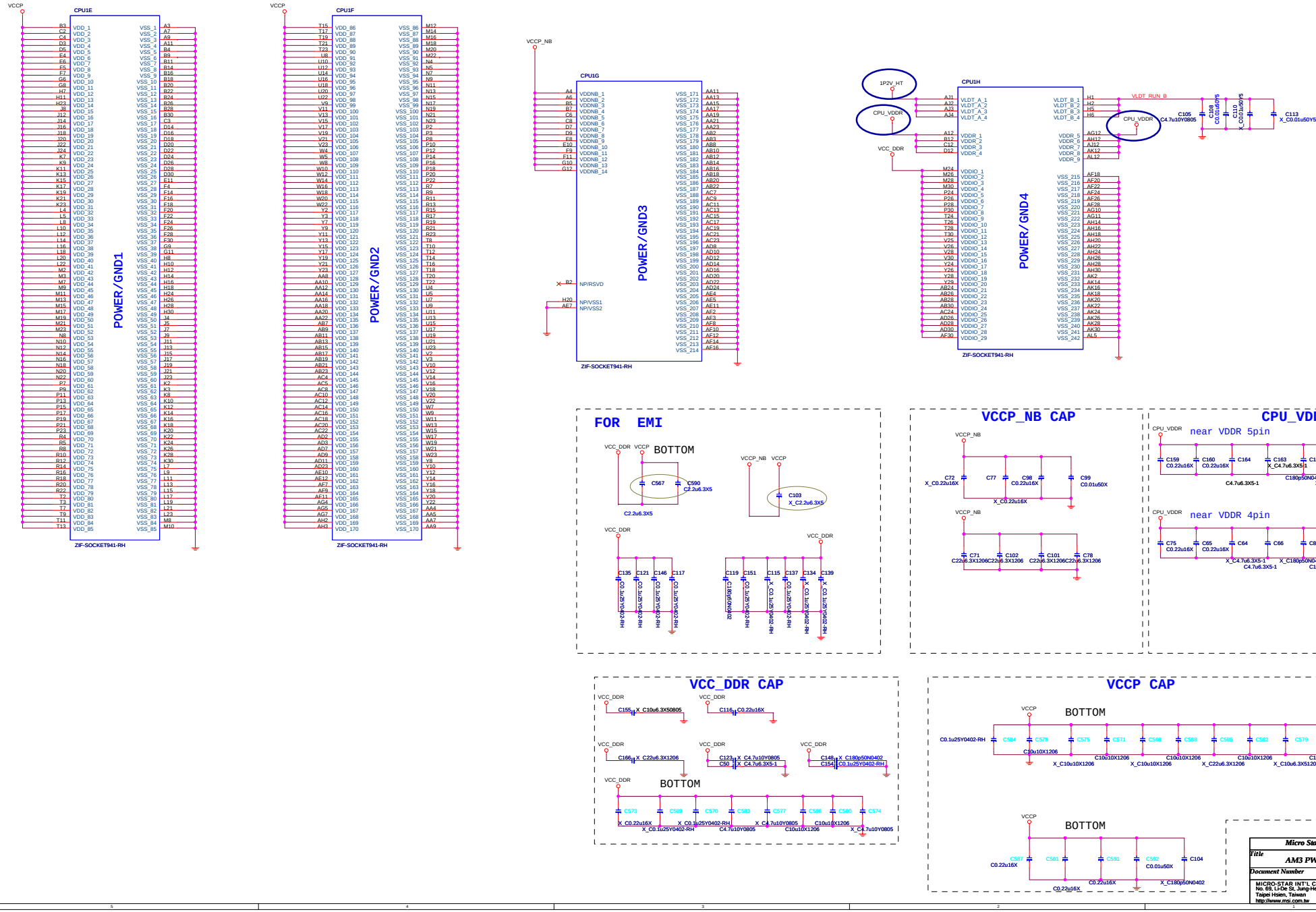
CPU1E
POWER/GND1
ZIF-SOCKET941-RH
CPU1F
POWER/GND2
ZIF-SOCKET941-RH
CPU1G
POWER/GND3
NP/RSVD
NP/VSS1
NP/VSS2
ZIF-SOCKET941-RH
CPU1H
POWER/GND4
ZIF-SOCKET941-RH
1P2V_HT
CPU_VDDR
VCC_DDR
VCCP_NB
VLDT_RUN_B
C105 C4.7u10Y0805
C108 C0.01u50Y5
C110 C0.01u50Y5
C113 X_C0.01u50Y5
FOR EMI
BOTTOM
C567 C590 C2.2u6.3X5
C103 X_C2.2u6.3X5
VCCP_NB CAP
C72 X_C0.22u16X
C77 C98 C0.22u16X
C99 C0.01u50X
X_C0.22u16X
C71 C22u6.3X1206
C102 C22u6.3X1206
C101 C22u6.3X1206
C78 C22u6.3X1206
CPU_VDDR CAP
near VDDR 5pin
C159 C0.22u16X
C160 C0.22u16X
C164
C163 X_C4.7u6.3X5-1
C161
C176
C180
C181
C180p50N0402
X_C1000p50X
C4.7u6.3X5-1
near VDDR 4pin
C75 C0.22u16X
C65 C0.22u16X
C64
C66
C86
C90
C81
C45
C1000p50X
VCC_DDR CAP
C155 X_C10u6.3X50805
C116 C0.22u16X
C166 X_C22u6.3X1206
C123 X_C4.7u10Y0805
C50 X_C4.7u6.3X5-1
C148 X_C180p50N0402
C154 C0.1u25Y0402-RH
C573 C589 C570 C583 C577 C586 C580 C574
X_C0.22u16X
X_C0.1u25Y0402-RH
X_C4.7u10Y0805
C10u10X1206
VCCP CAP
C584 C578 C575 C571 C568 C588 C585 C582 C579 C576 C572 C569
C10u10X1206
X_C22u6.3X1206
C10u6.3X51206
C597 C581 C591 C592 C0.01u50X C104
X_C180p50N0402
Micro Star Restricted Secret
Title
AM3 PWR & GND
Rev
10
Document Number
MS-7715
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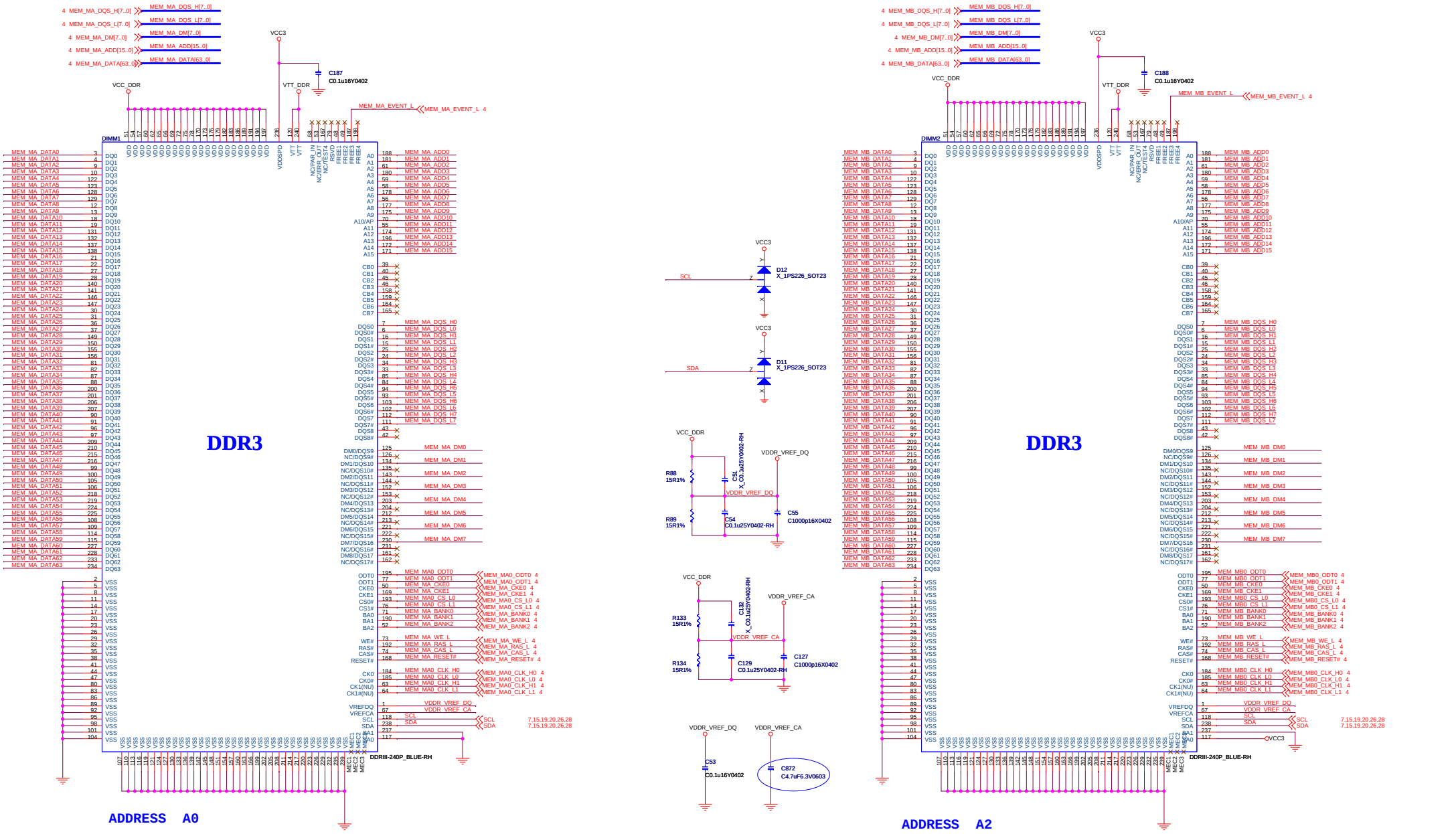

SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6

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Title: FIRST LOGICAL DDR DIMM

Rev: 10

Document Number: MS-7715

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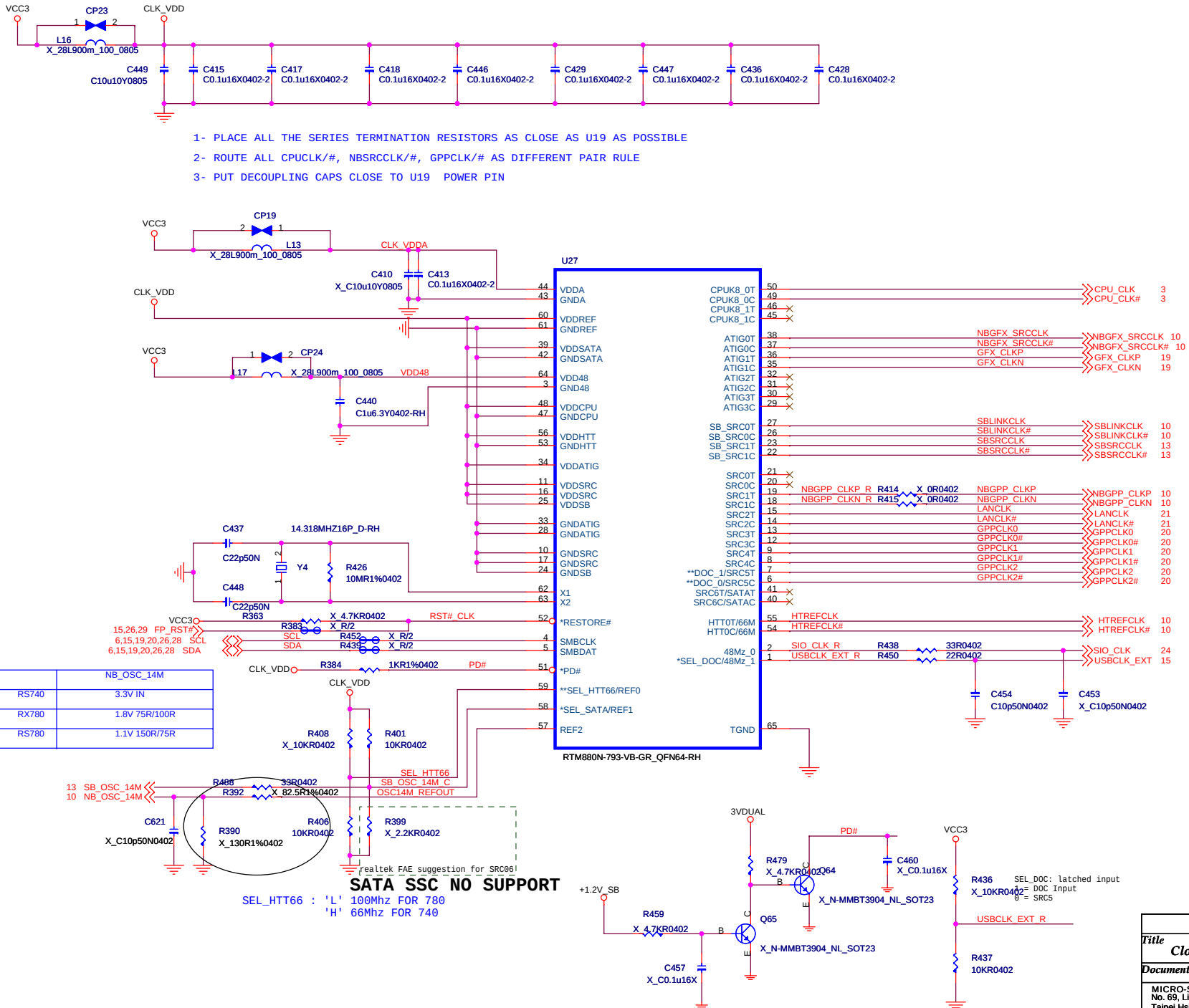

	NB_OSC_14M
RS740	3.3V IN
RX780	1.8V 75R/100R
RS780	1.1V 150R/75R

SATA SSC NO SUPPORT

SEL_HTT66 : 'L' 100Mhz FOR 780
'H' 66Mhz FOR 740

Micro Star Restricted Secret

Title	Clock Generator RTM880N-793
Rev	10
Document Number	MS-7715

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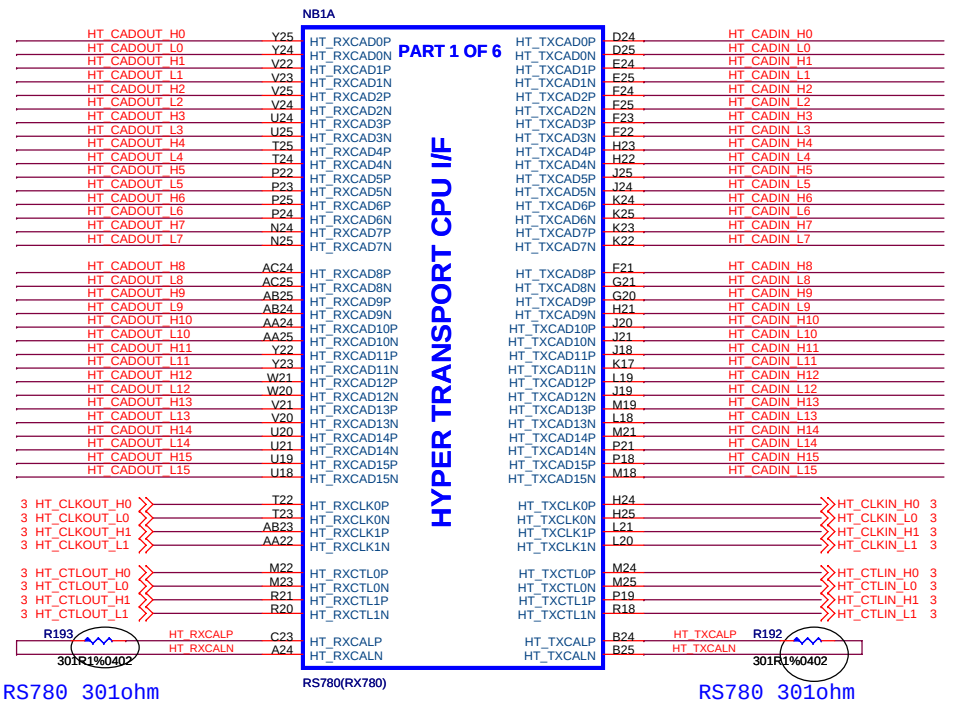
3 HT_CADIN_H[15..0] — HT_CADIN_H[15..0]

3 HT_CADIN_L[15..0] — HT_CADIN_L[15..0]

3 HT_CADOUT_H[15..0] — HT_CADOUT_H[15..0]

3 HT_CADOUT_L[15..0] — HT_CADOUT_L[15..0]



RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP HT_TXCALN	100R	1.21K	301R

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Title: *RD780-HT LINK I/F*	Rev: 10
Document Number: *MS-7715*	

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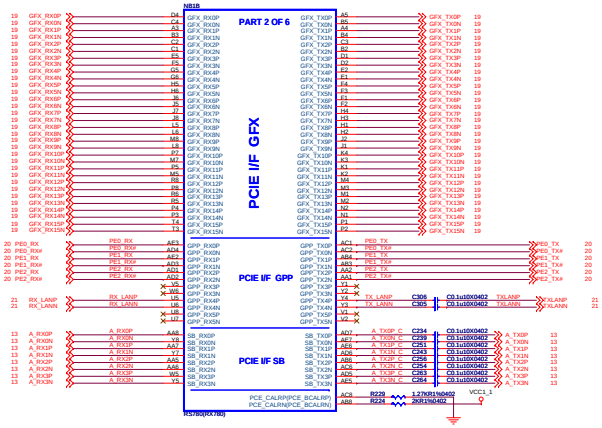

RX740/RS740/RS780 difference table (PCIE LINK)

	RS740	RX740/RS780
PCIE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Title	RD780-PCIE I/F
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RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL

	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OD	OD	OD/3.3V IN
LDT_STOP# IN(default)/OUT	3.3V IN	1.8V IN	3.3V IN/OD
SYSTEMRESETb IN	3.3V IN	1.8V IN	3.3V IN

	RS780	RX780	SB700	CPU
LDT_STOP#	3.3V IN	VDD18/IN	OD	1.8V IN
LDT_RST#	SYSREST 3.3VIN	SYSREST VDD18VIN	OD	1.8V IN
ALLOW_STOP#	OD	0D/VDD18	3.3V IN	NA
POWERGOOD	VDD18/IN	VDD18/IN	NA	NA

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIE refereence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```
Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable  (RS740); Disable(RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1   Mode L   default
110: 1-1-1-1-1-1   Mode L
101: 2-0-2-0-2-0   Mode C2
100: 2-0-2-0-1-1   Mode K
011: 2-0-1-1-1-1   Mode E
010: 1-1-1-1-1-1   Mode L
001: 4-0-0-0-1-1   Mode C
000: 4-0-0-0-2-0   Mode B
```

PCIE4X_SX1	RD780_DFT_GPIO4	RD780_DFT_GPIO3
LOW	LOW	LOW
HIGH	HIGH	HIGH

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1.  Disable (can be enabled
      thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register
            setting only
RS740: Not supported
```

CHANGE TO 1.0

RS780 stuff

R233 RS780 stuff

Title	RD780-SYSTEM I/F
Rev	10
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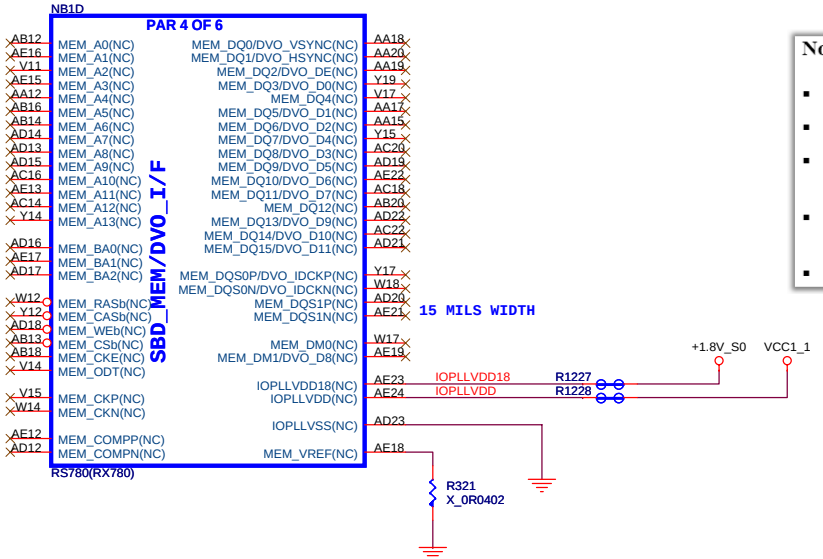
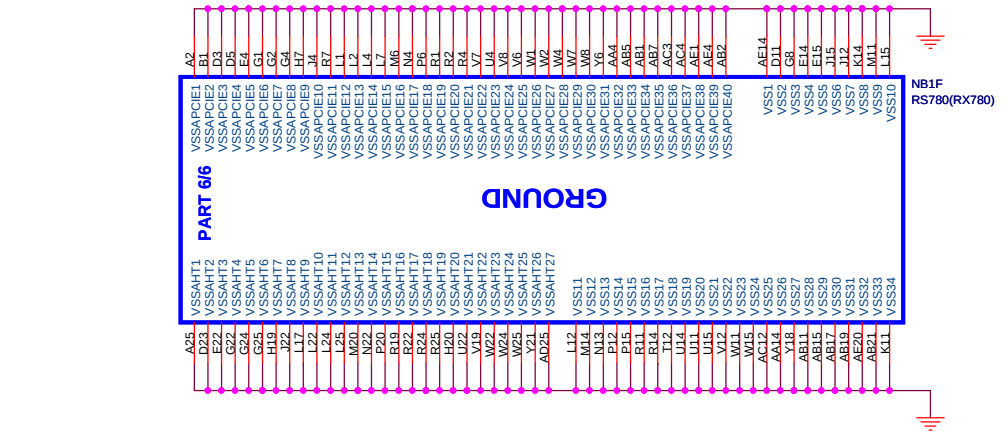


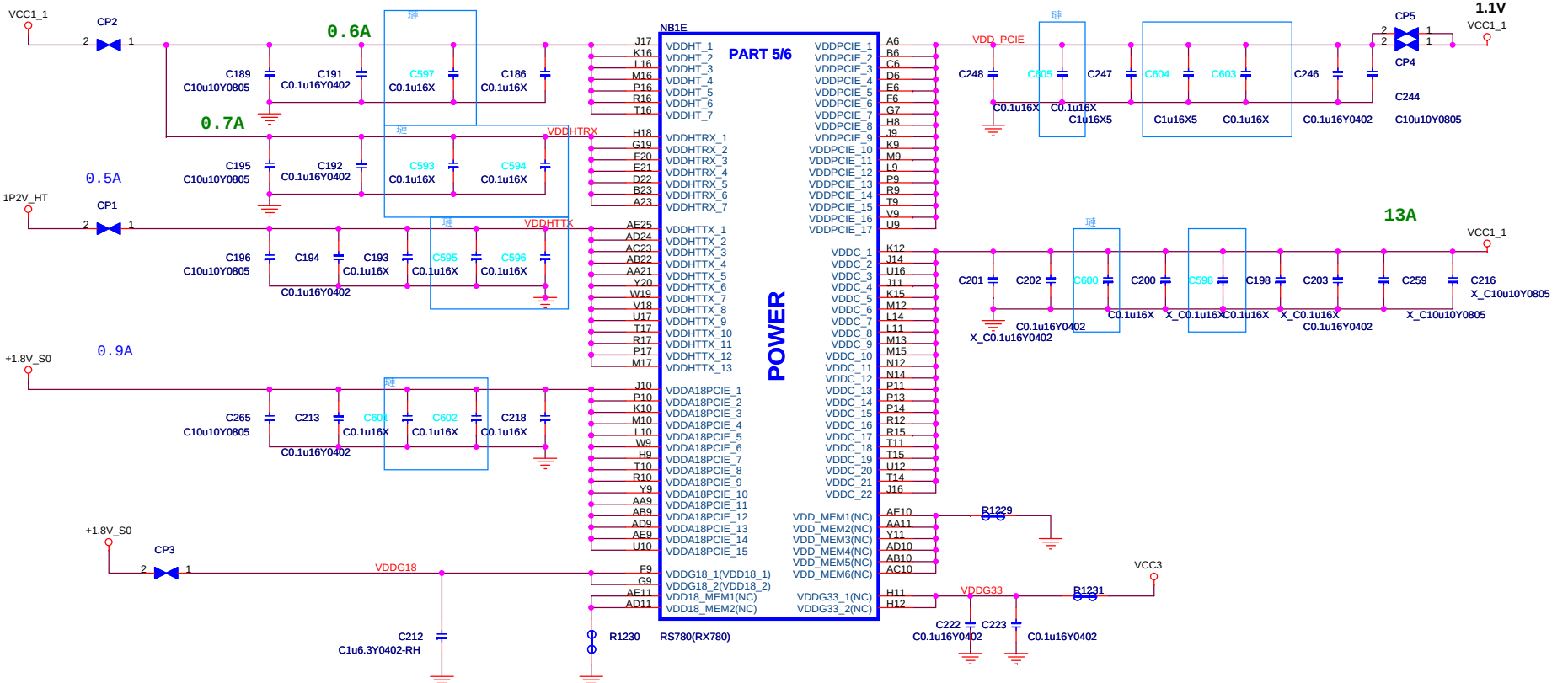
Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC



Micro Star Restricted Secret	
Title: RD780-POWER	Rev: 10
Document Number: MS-7715	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Friday, January 07, 2011
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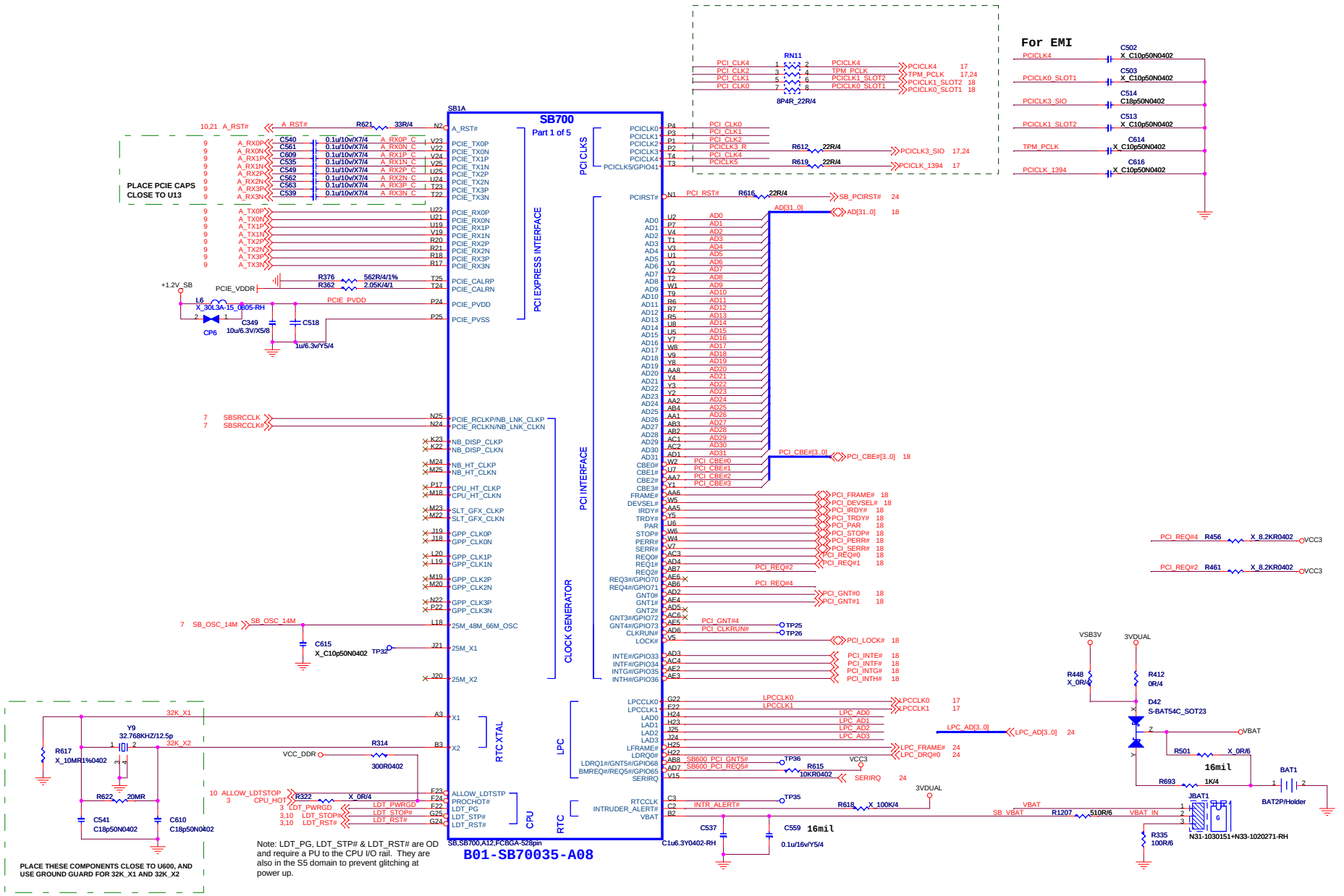
SB700
Part 1 of 5
SB1A
PCI EXPRESS INTERFACE
PCI CLKS
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC
CPU
RTC XTAL
PLACE PCIE CAPS CLOSE TO U13
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
For EMI
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.
SB,SB700,A12,FCBGA-528pin
B01-SB70035-A08
Micro Star Restricted Secret
Title
SB700-PCIE/PCI/CPU/LPC
Rev
10
Document Number
MS-7715
MICRO-STAR INT'L CO.,LTD.
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Impendance 90 Ohm,refer to AN_SB700AB2

SATA1

SATA7PM_BLACK-P-RH

SATA2

SATA7PM_BLACK-P-RH

SATA3

X_SATA7PM_BLACK-P-RH

SATA4

X_SATA7PM_BLACK-P-RH

SATA5

X_SATA7PM_BLACK-P-RH

SATA6

X_SATA7PM_BLACK-P-RH

SB1B

SB700
Part 2 of 5

SERIAL ATA

ATA 66/100/133

SPI ROM

SATA PWR

HW MONITOR

SB,SB700,A12,FCBGA-528pin

N5N-07M0231-H06

R624 IS 1K 1% FOR XTAL,
4.99K 1% FOR INTERNAL CLK

Reserved for EMI 0906

TEMP _COMM
connect to GND
for AMD recommand

NS_VIA CONNECTS
HWM_AGND TO GND

SPI FLASH MEMORY

SPI DEBUG PORT
Place close to SPI ROM

Part Number : N31-2051451-H06

15 MILS WIDTH

CAP CLOSE TO THE BALLS OF SB

CAP CLOSE TO THE BALL OF SB

Micro Star Restricted Secret	
Title: SB700-SATA/IDE/HWM/SPI	Rev: 10
Document Number: MS-7715	
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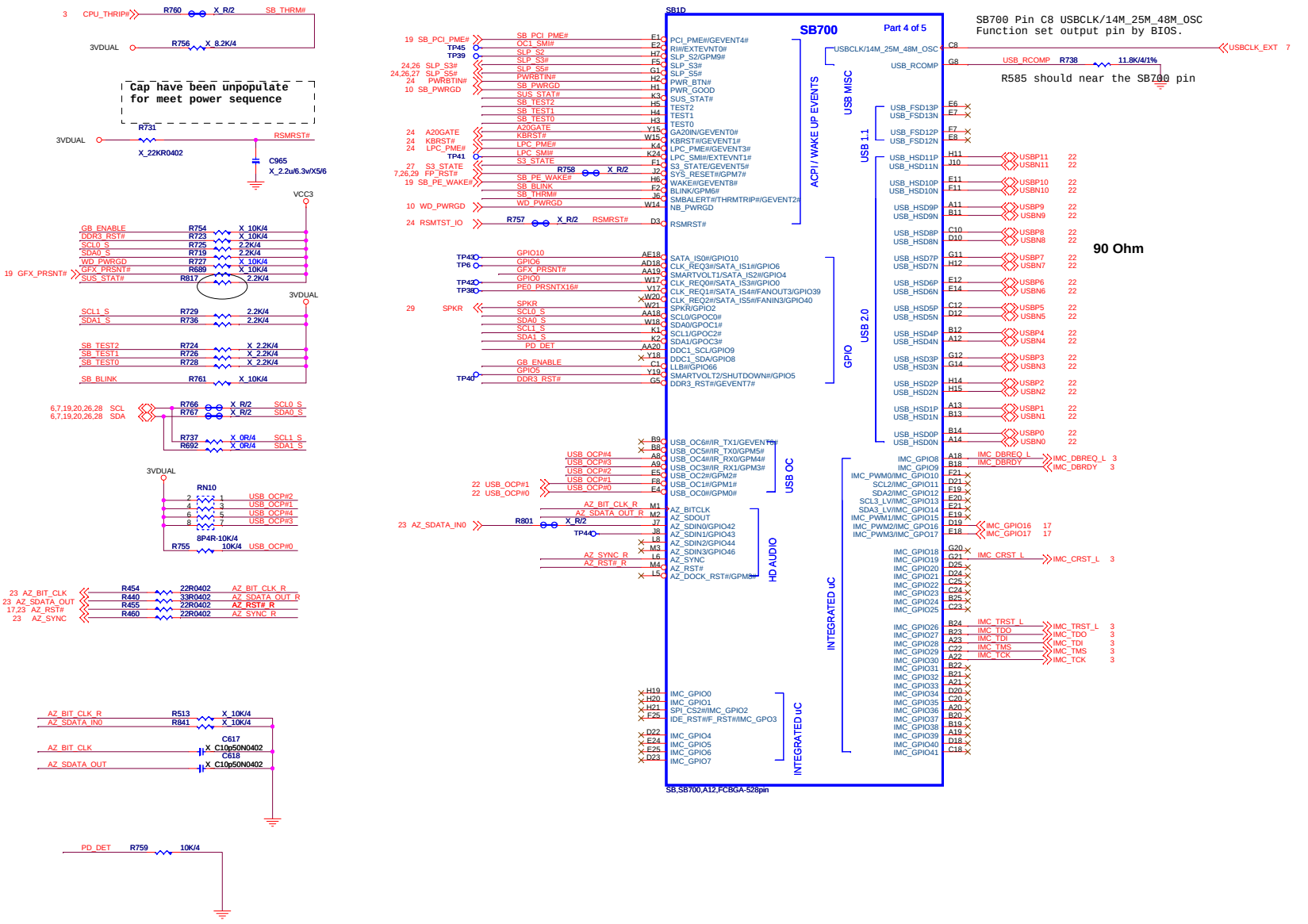

Micro Star Restricted Secret	
Title: SB700-ACPI/GPIO/USB/AUDIO	Rev: 10
Document Number: MS-7715	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Thursday, January 06, 2011
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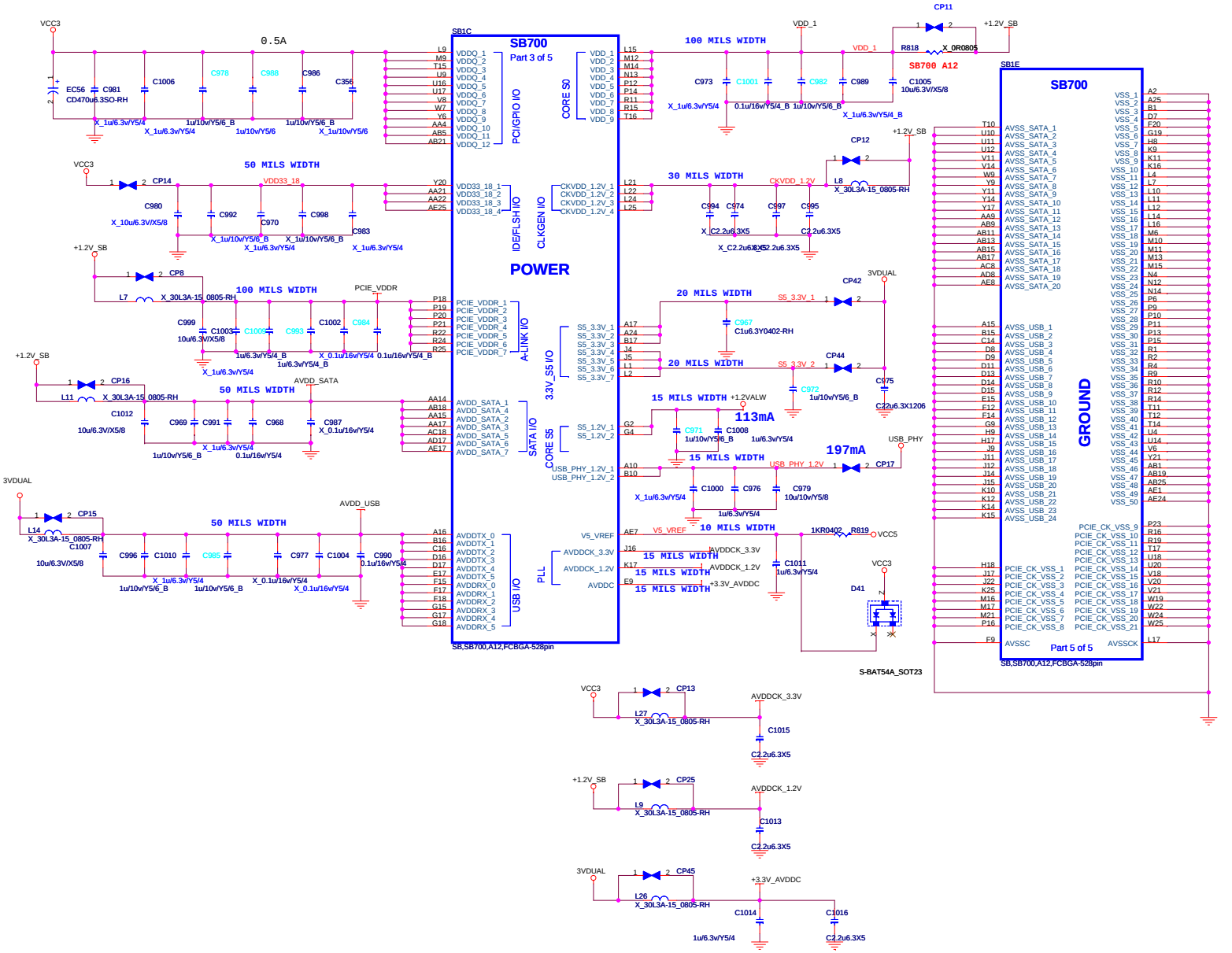
SB700
Part 3 of 5
POWER
SB1C
SB,SB700,A12,FCBGA-528pin
SB700 A12
SB1E
Part 5 of 5
GROUND
0.5A
100 MILS WIDTH
50 MILS WIDTH
30 MILS WIDTH
20 MILS WIDTH
15 MILS WIDTH
10 MILS WIDTH
113mA
197mA
CORE S0
PCI/GPIO I/O
IDE/FLSH I/O
CLKGEN I/O
A-LINK I/O
3.3V_S5 I/O
SATA I/O
CORE S5
USB I/O
PLL
S-BAT54A_SOT23
Micro Star Restricted Secret
SB700-POWER & DECOUPLING
MS-7715
MICRO-STAR INT'L CO.,LTD.
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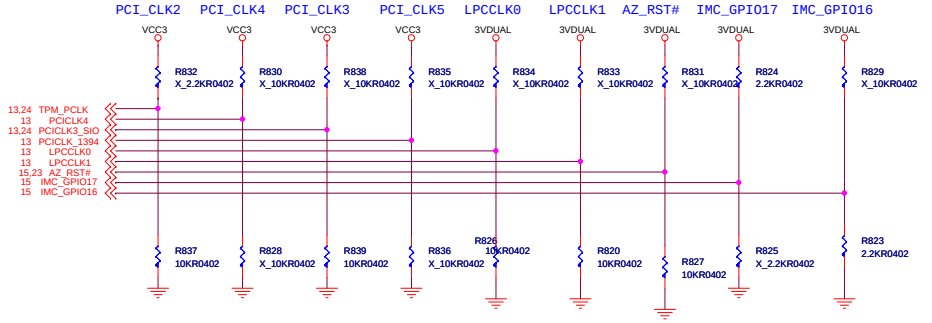
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK4	PCI_CLK3	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	RESERVED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT		IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

Title	*SB700-STRAPS*
Rev	10
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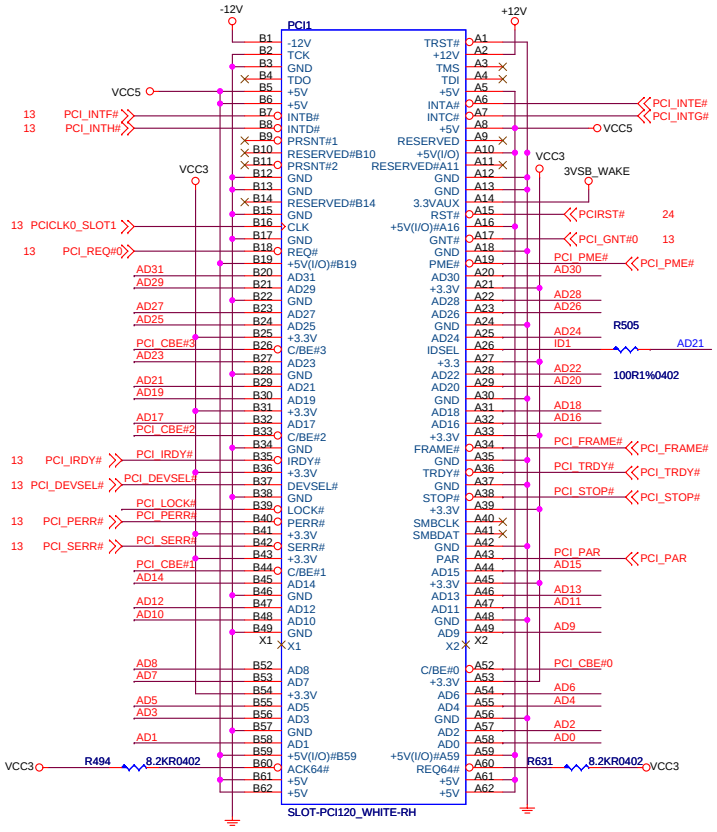
13 AD[31..0] AD[31..0]

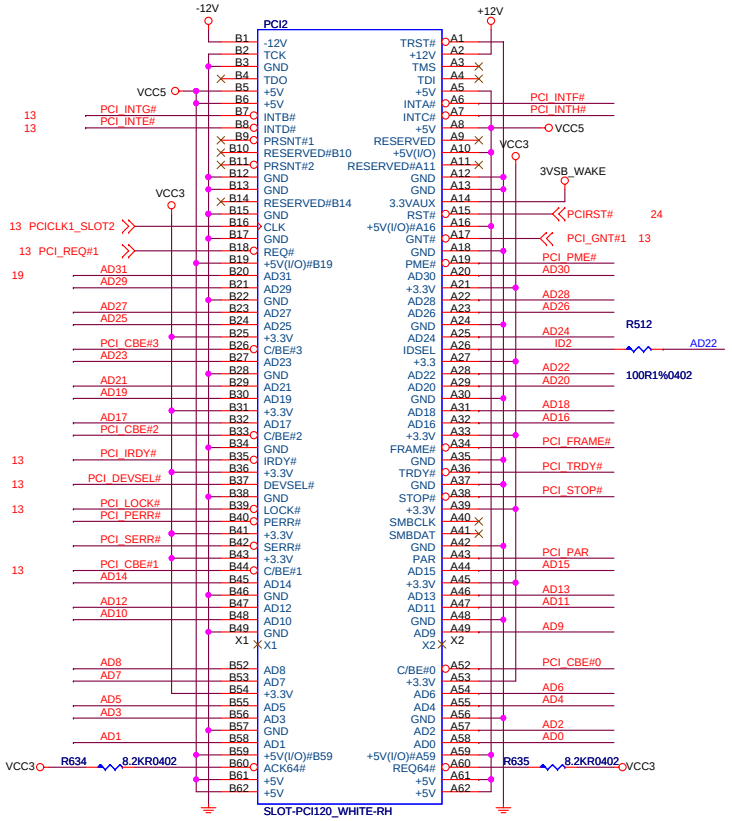
13 PCI_CBE#[3..0] PCI_CBE#[3..0]

PCI SLOT 1 (PCI VER: 2.2 COMPLY)



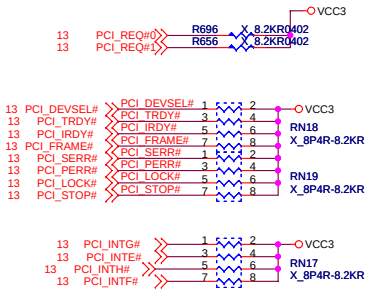
IDSEL = AD21
MASTER = PCI_REQ#0
PCI_GNT#0

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



IDSEL = AD22
MASTER = PCI_REQ#1
PCI_GNT#1

PCI PULL-UP / DOWN RESISTORS



Micro Star Restricted Secret	
Title: PCI Slot 1,2	Rev: 10
Document Number: MS-7715	
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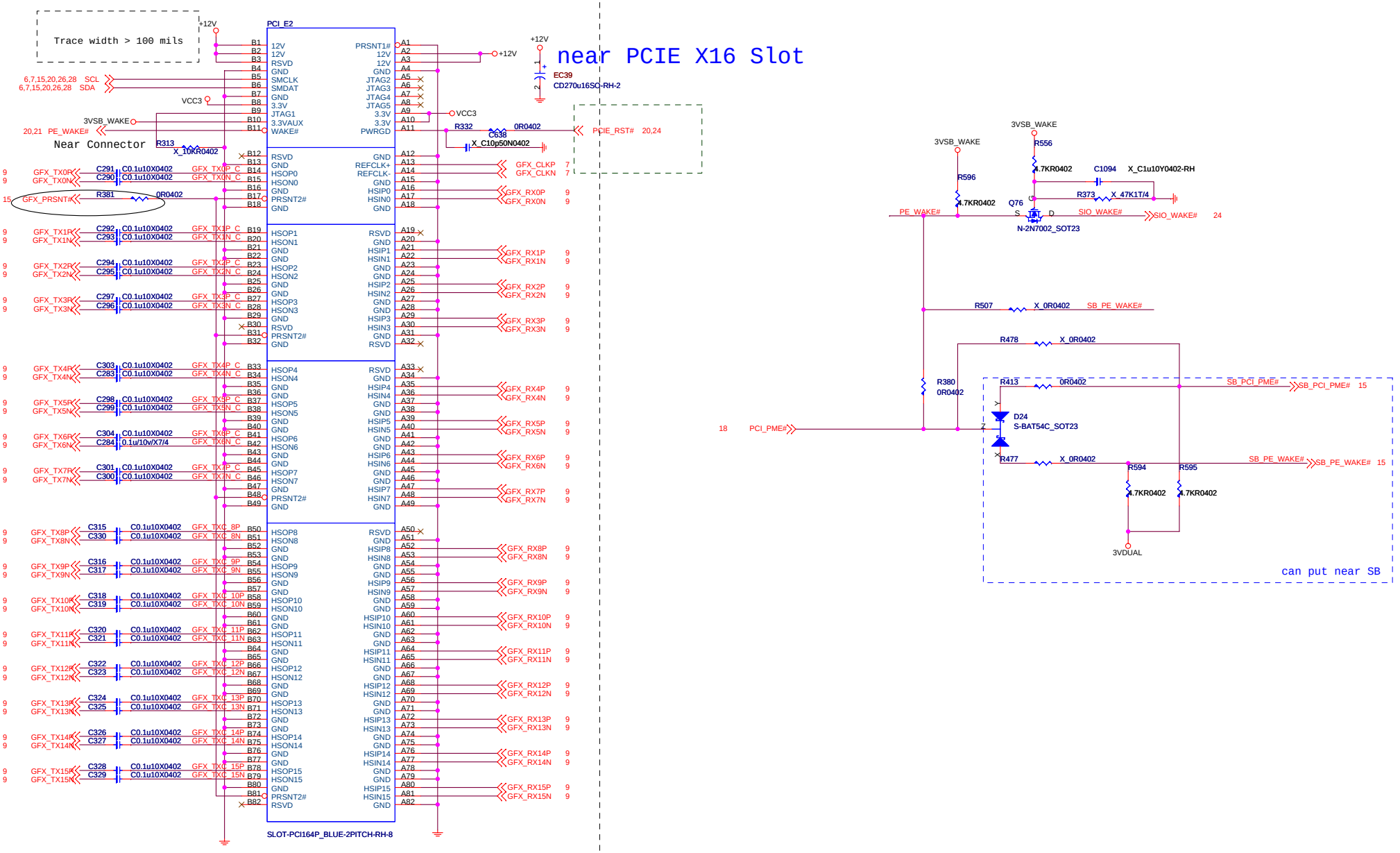
	Sheet 18 of 35

PCI EXPRESS_16

Trace width > 100 mils

near PCIE X16 Slot

Near Connector



Micro Star Restricted Secret	
Title: PCI-E X16 , X1 Slot	Rev: 10
Document Number: MS-7715	
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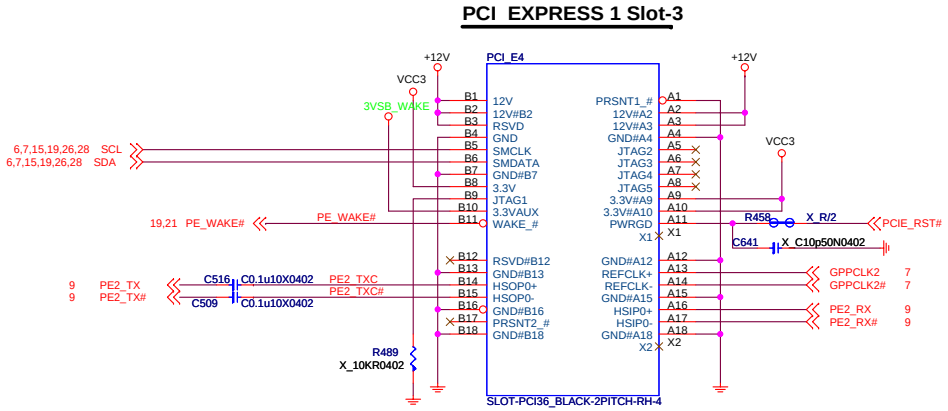
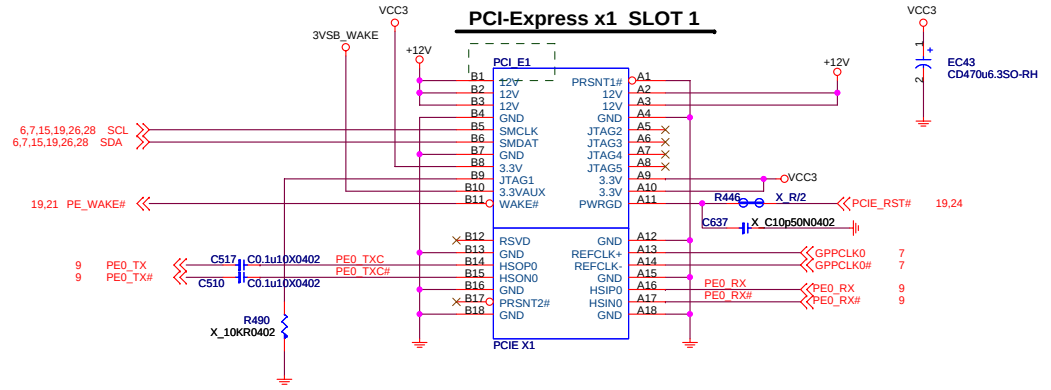
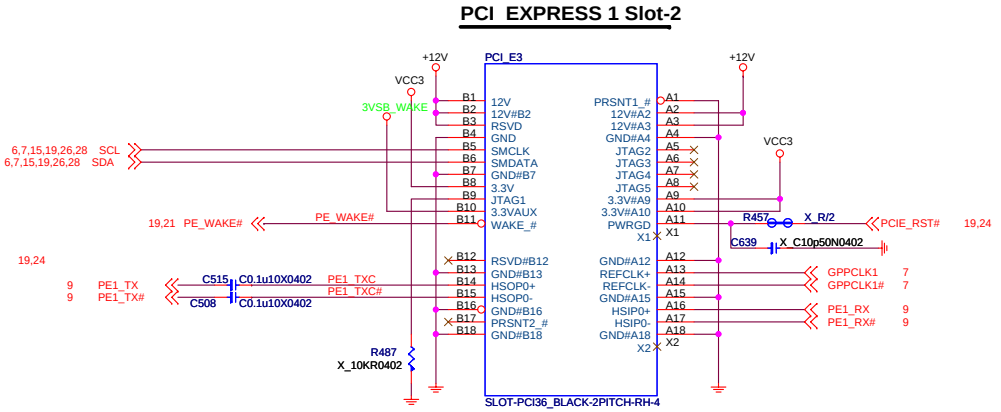


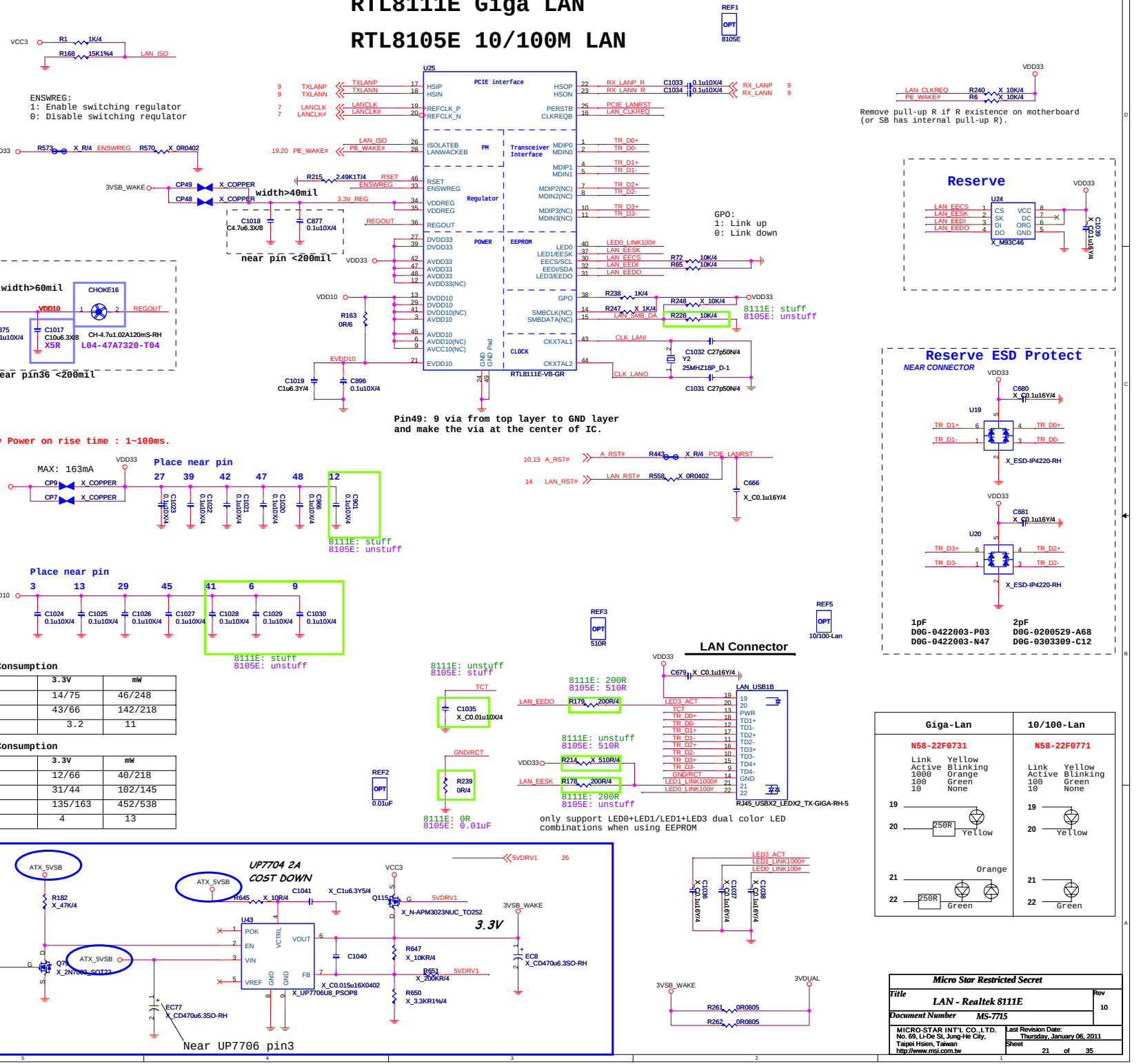




Micro Star Restricted Secret	
Title PCIE X1 Slots	Rev 10
Document Number MS-7715	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Thursday, January 06, 2011 Sheet 20 of 35

RTL8111E Giga LAN

RTL8105E 10/100M LAN



Micro Star Restricted Secret		
Title: LAN - Realtek 8111E		Rev: 10
Document Number: MS-7715		
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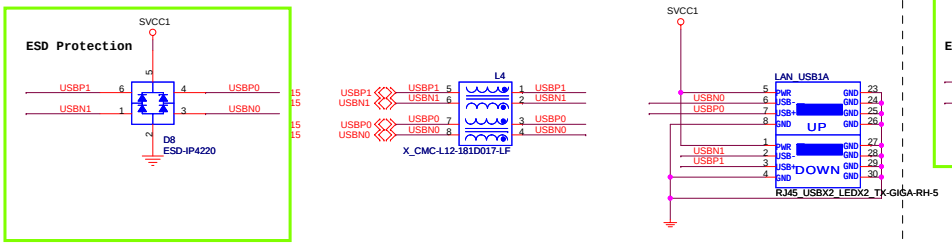
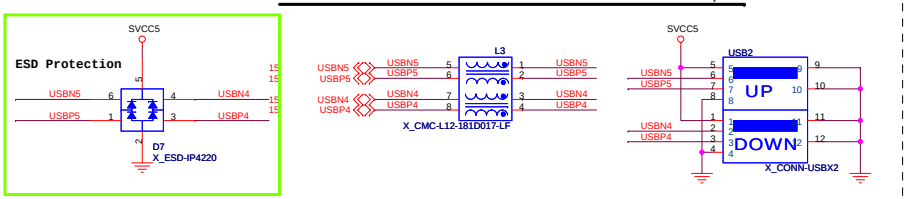
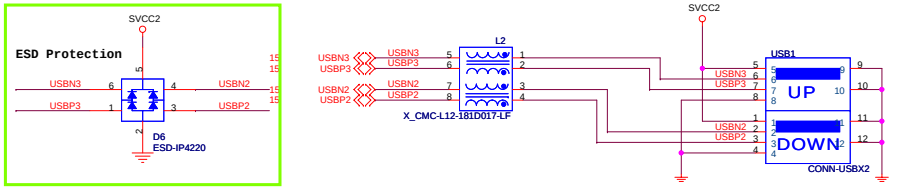
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

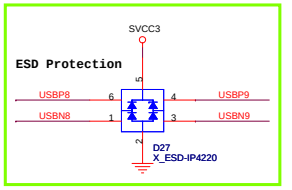


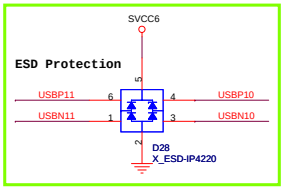
REAR PANEL USB CONNECTOR FOR USB PORT 4,5

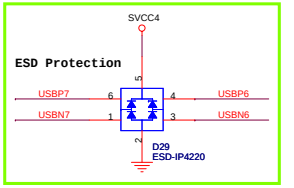


REAR PANEL USB CONNECTOR FOR USB PORT 2,3



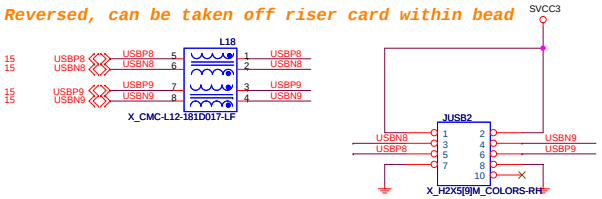




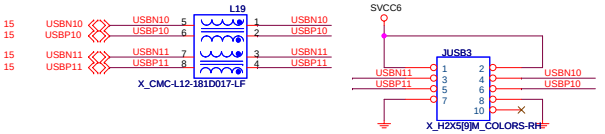


FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

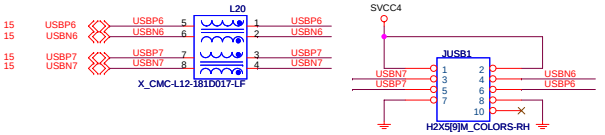
Reversed, can be taken off riser card within bead



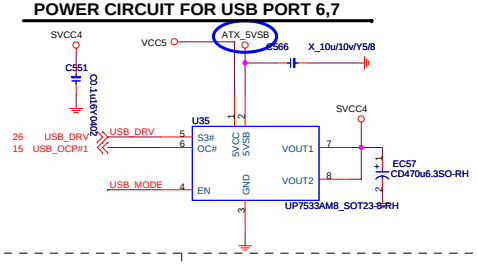
FRONT PANEL USB CONNECTOR FOR USB PORT 10,11



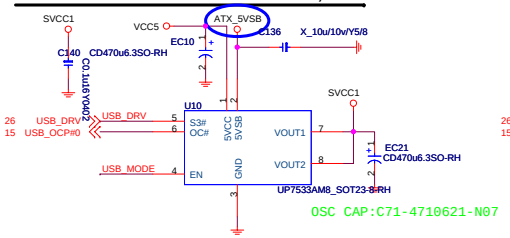
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



POWER CIRCUIT FOR USB PORT 6,7

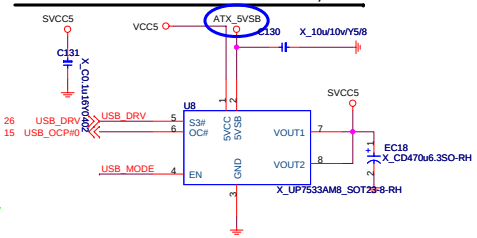


POWER CIRCUIT FOR USB PORT 0,1

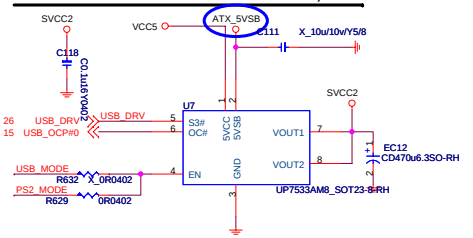


OSC CAP:C71-4710621-N07

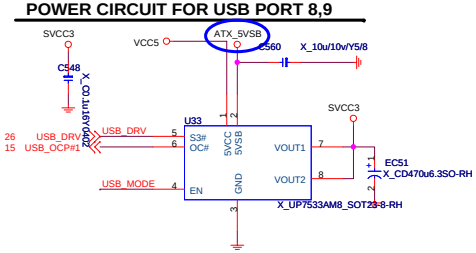
POWER CIRCUIT FOR USB PORT 4,5



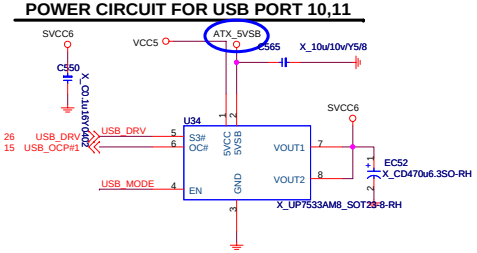
POWER CIRCUIT FOR USB PORT 2,3



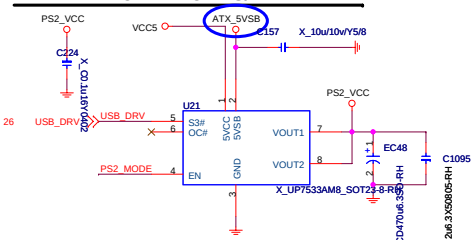
POWER CIRCUIT FOR USB PORT 8,9

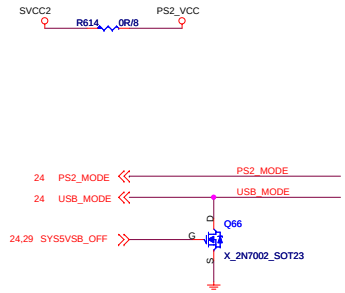


POWER CIRCUIT FOR USB PORT 10,11



POWER FOR PS/2





Micro Star Restricted Secret		
Title: USB CONNECTORS		Rev: 10
Document Number: MS-7715		
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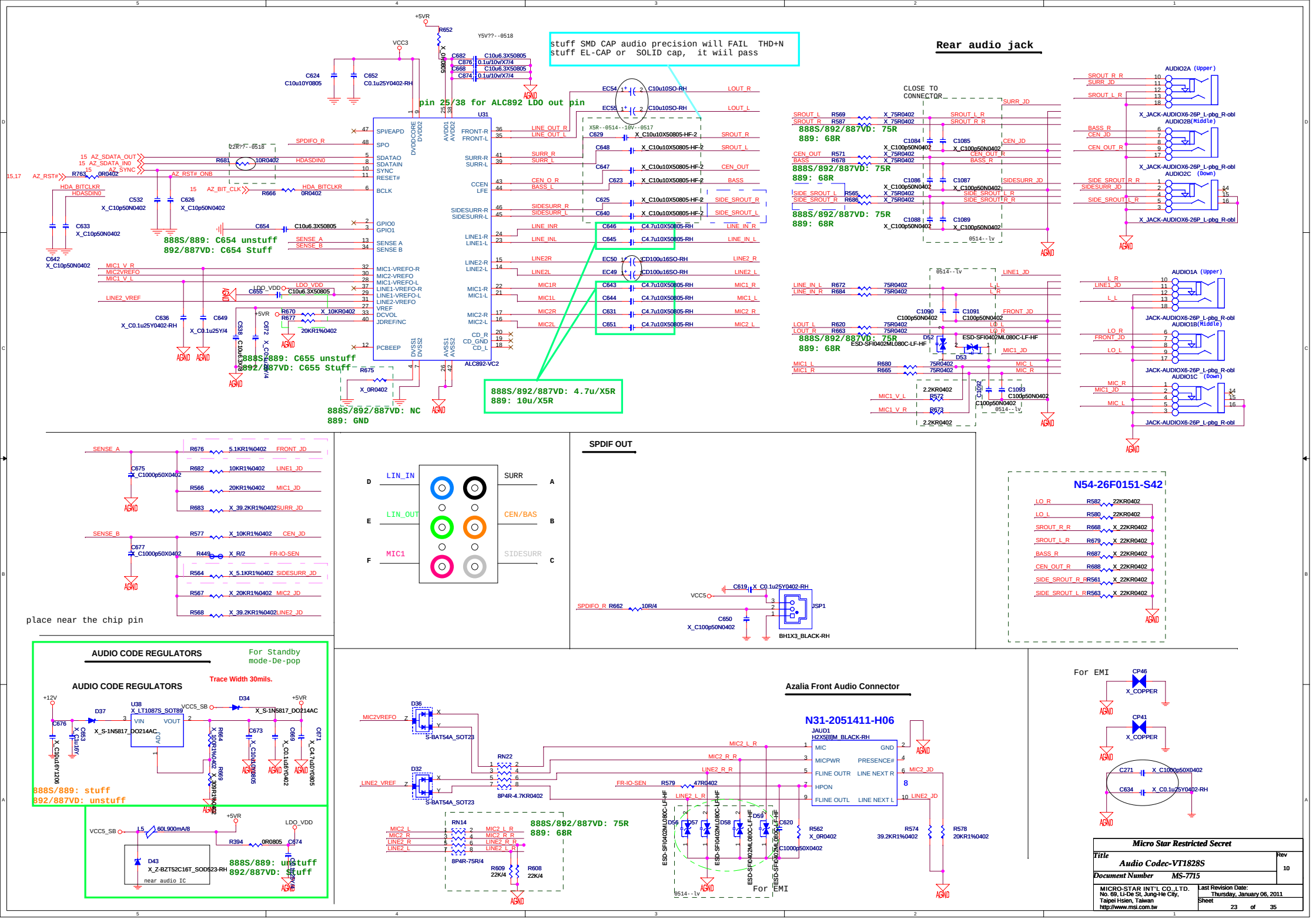
stuff SMD CAP audio precision will FAIL THD+N
stuff EL-CAP or SOLID cap, it wiil pass
pin 25/38 for ALC892 LDO out pin
888S/889: C654 unstuff
892/887VD: C654 Stuff
888S/889: C655 unstuff
892/887VD: C655 Stuff
888S/892/887VD: NC
889: GND
888S/892/887VD: 4.7u/X5R
889: 10u/X5R
ALC892-VC2
Rear audio jack
CLOSE TO CONNECTOR
888S/892/887VD: 75R
889: 68R
AUDIO2A (Upper)
AUDIO2B(Middle)
AUDIO2C (Down)
AUDIO1A (Upper)
AUDIO1B(Middle)
AUDIO1C (Down)
JACK-AUDIOX6-26P_L-pbg_R-obl
SPDIF OUT
ESD-SFI0402ML080C-LF-HF
N54-26F0151-S42
LIN_IN
LIN_OUT
MIC1
SURR
CEN/BAS
SIDESURR
place near the chip pin
AUDIO CODE REGULATORS
For Standby mode-De-pop
Trace Width 30mils.
888S/889: stuff
892/887VD: unstuff
888S/889: unstuff
892/887VD: stuff
near audio IC
Azalia Front Audio Connector
N31-2051411-H06
JAUD1
H2X5[8]M_BLACK-RH
888S/892/887VD: 75R
889: 68R
For EMI
Micro Star Restricted Secret
Audio Codec-VT1828S
Rev 10
Document Number MS-7715
MICRO-STAR INT'L CO.,LTD.
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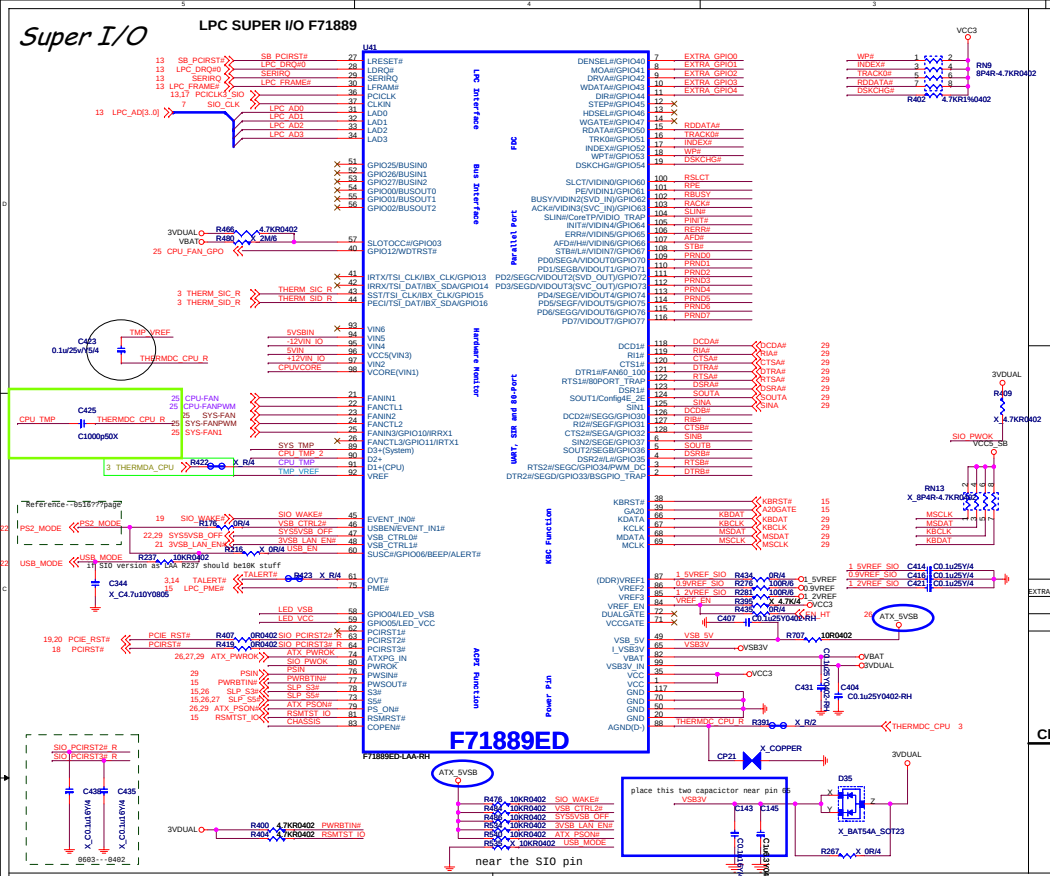
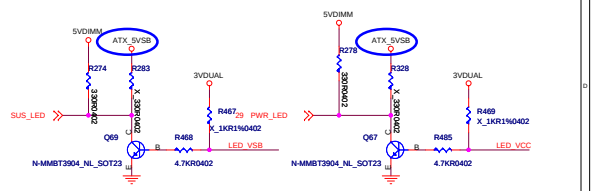
Super I/O

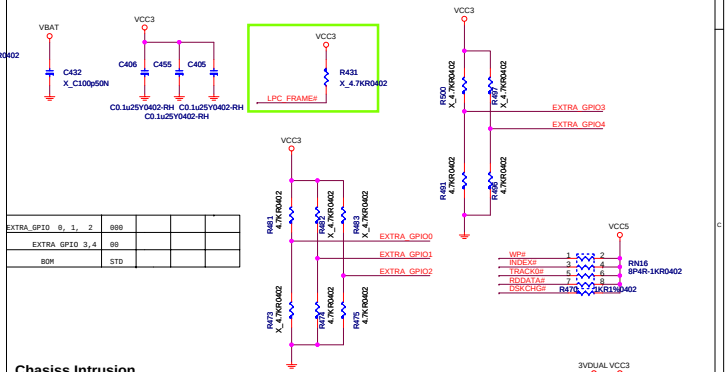
LPC SUPER I/O F71889



Super I/O

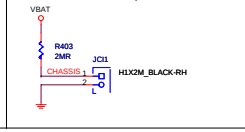
	audio_card_detect	PCIE_GND
OnBo_Audio	1	1
PCIE_Audio	1	0

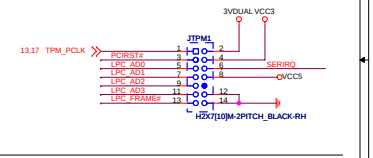




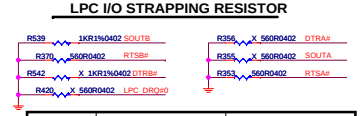
EXTRA_GPIO 0, 1, 2	000			
EXTRA GPIO 3,4	00			
BOM	STD			

Chasis Intrusion





LPC I/O STRAPPING RESISTOR

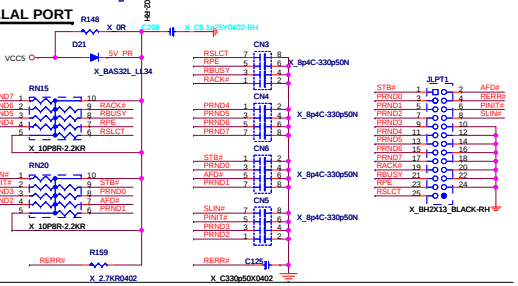


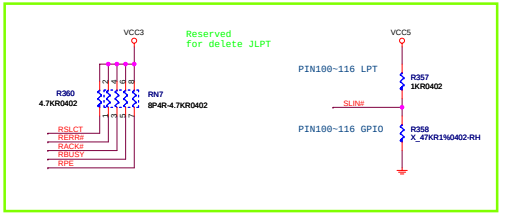
	Don't STUFF	STUFF
RTS2#	PWM FAN	LINEAR FAN
RTSA#	80Port enable	80Port disable
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
DTR2	PIN51~56 as GPIO	PIN51~56 as BUS I/F
SOUT2	PIN51~56 as GPIO	PIN51~56 as BUS I/F

for LAA version only

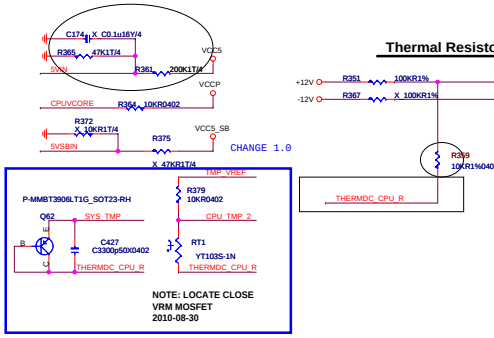
for LXA version only

PARALLAL PORT

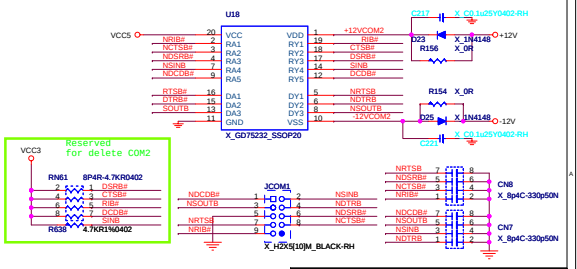




Thermal Resistor



SERIAL PORT 2



Title	LPC SUPER I/O & LPC & CONNECTORS	Rev 10
Document Number	MS-7715	

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FAN CONTROL

CPU FAN

CPU-FANPWM connect to 627EHF pin 115;default is PWM mode

If using 4 pin fan, The GPIO must drive to high.

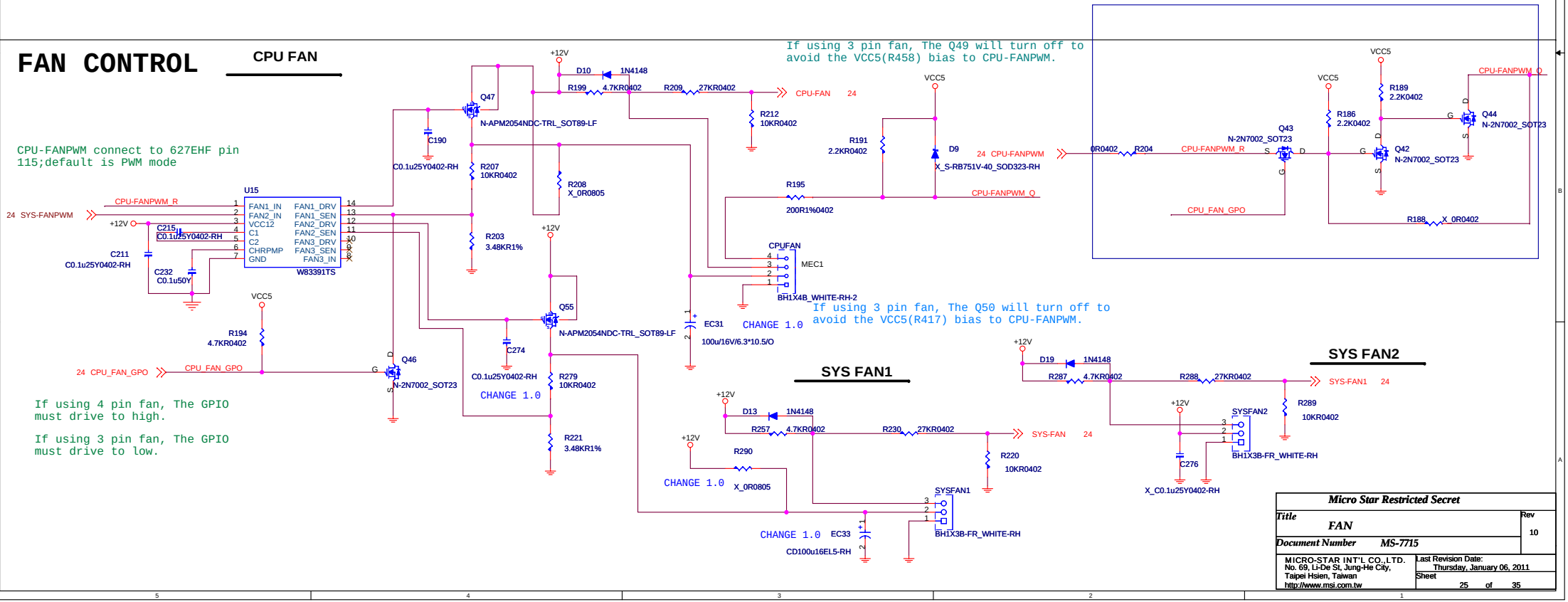
If using 3 pin fan, The GPIO must drive to low.

If using 3 pin fan, The Q49 will turn off to avoid the VCC5(R458) bias to CPU-FANPWM.

If using 3 pin fan, The Q50 will turn off to avoid the VCC5(R417) bias to CPU-FANPWM.

SYS FAN1

SYS FAN2



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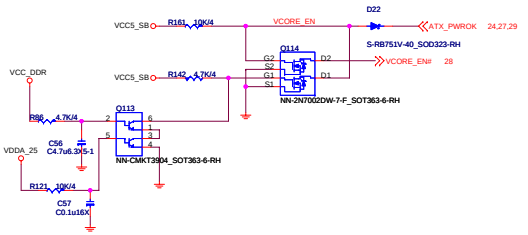
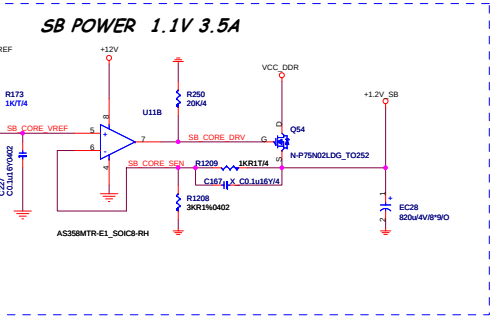
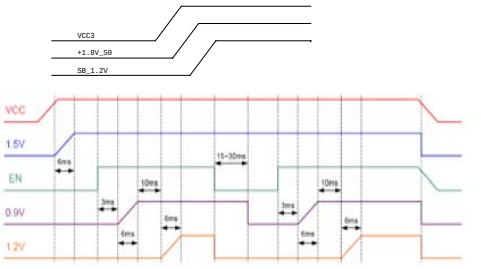
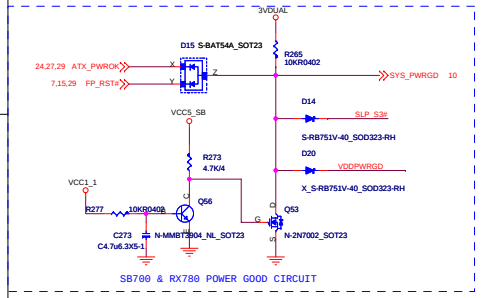
Title: FAN		Rev: 10
Document Number: MS-7715		
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Thursday, January 06, 2011	Sheet 25 of 35

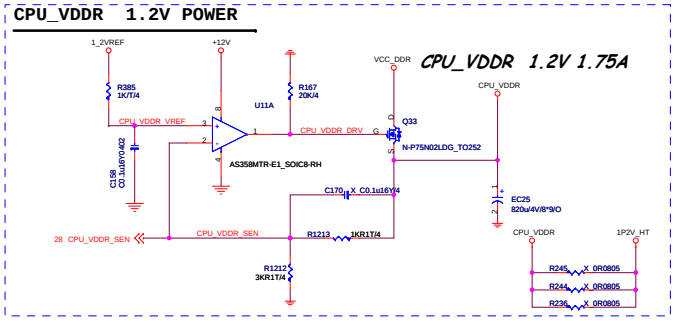


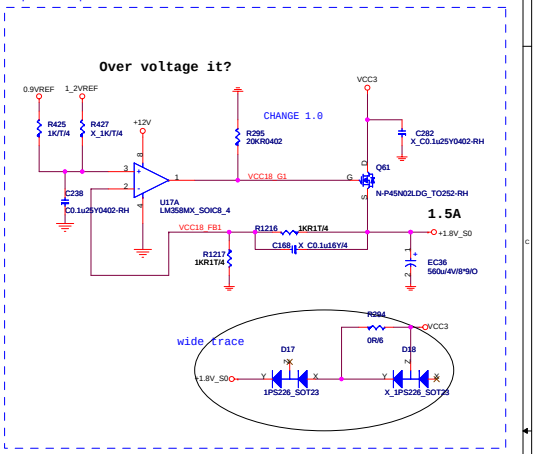


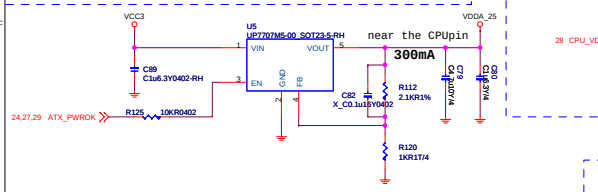


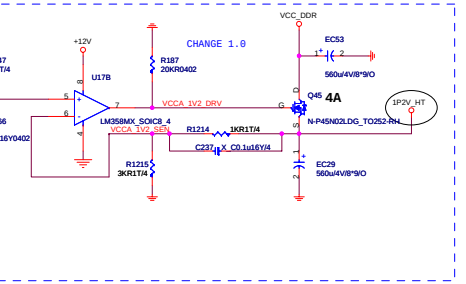
power sequence 3.3v-1.8v-1.1v

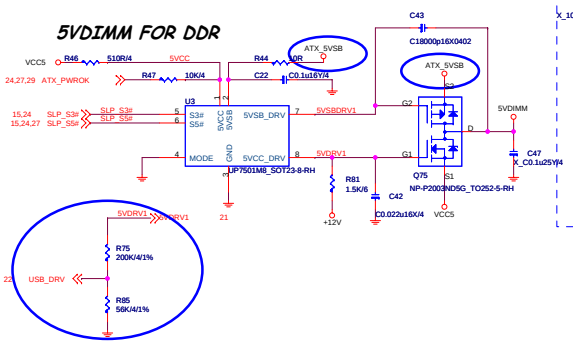




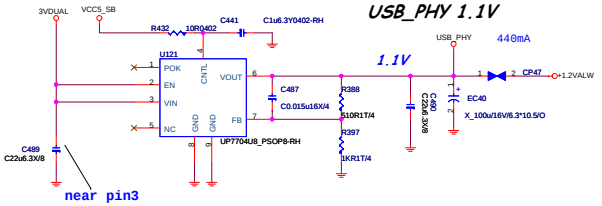


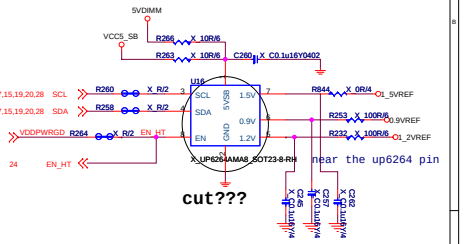


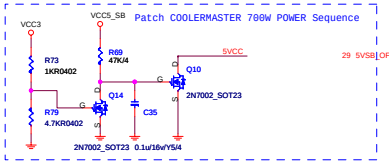


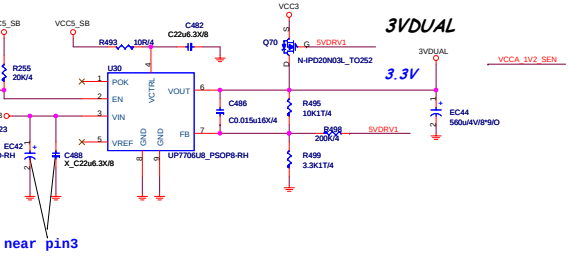


S5	S3	MODE	5VDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWM	S4/S5









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RX780 power up sequence

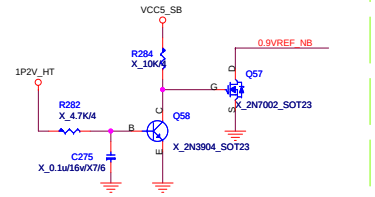
VCC3

VCC1.8_S0

1P2V_HT

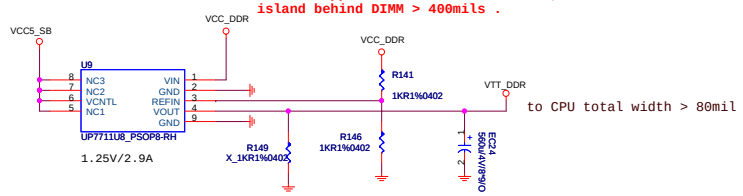
VCC1_1

Reserve for RX780 POS



DDR VTT Power

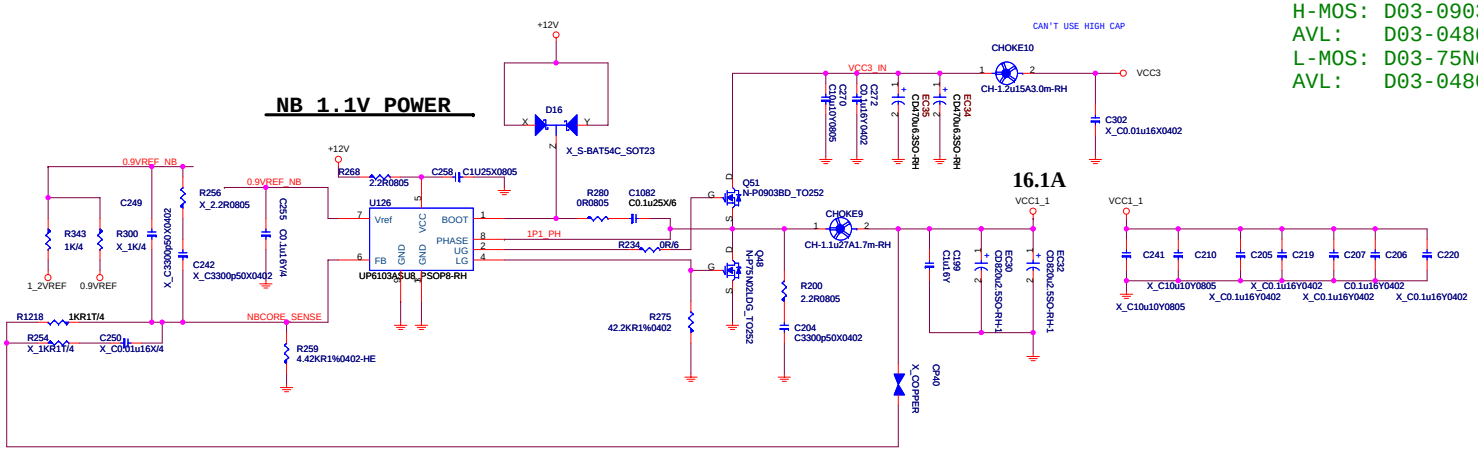
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



to CPU total width > 80mil

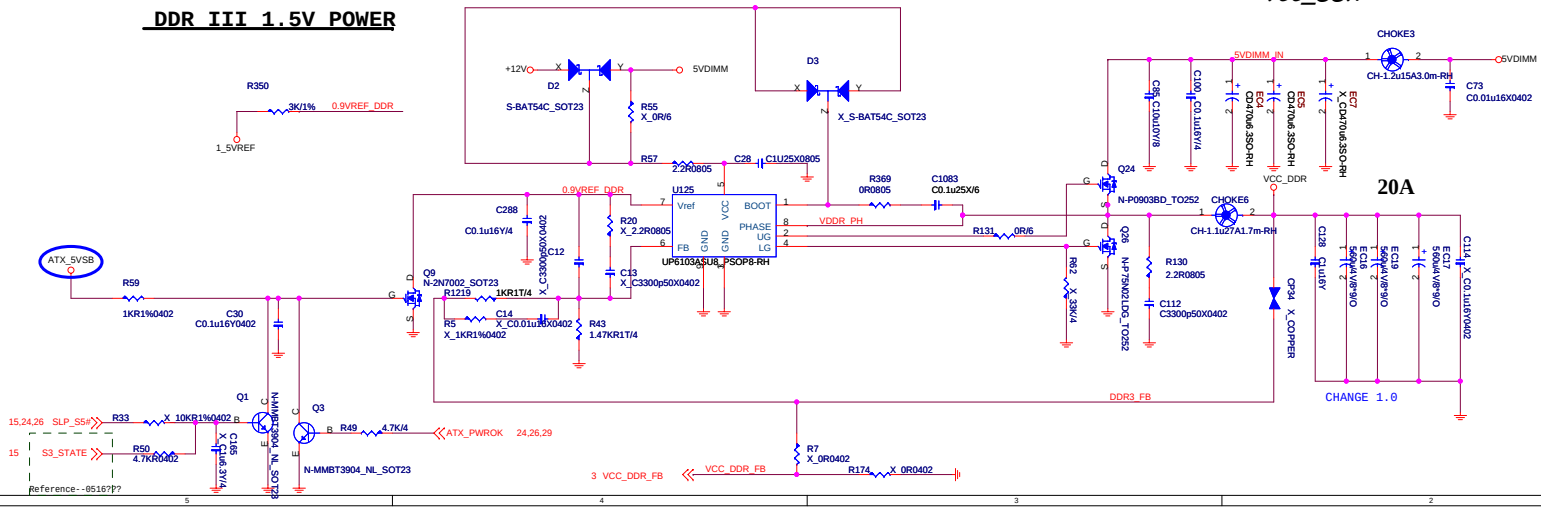
H-MOS: D03-0903BDB-N03
AVL: D03-0480900-O05
L-MOS: D03-75N022B-N03
AVL: D03-0480600-O05

NB 1.1V POWER



DDR III 1.5V POWER

VCC_DDR



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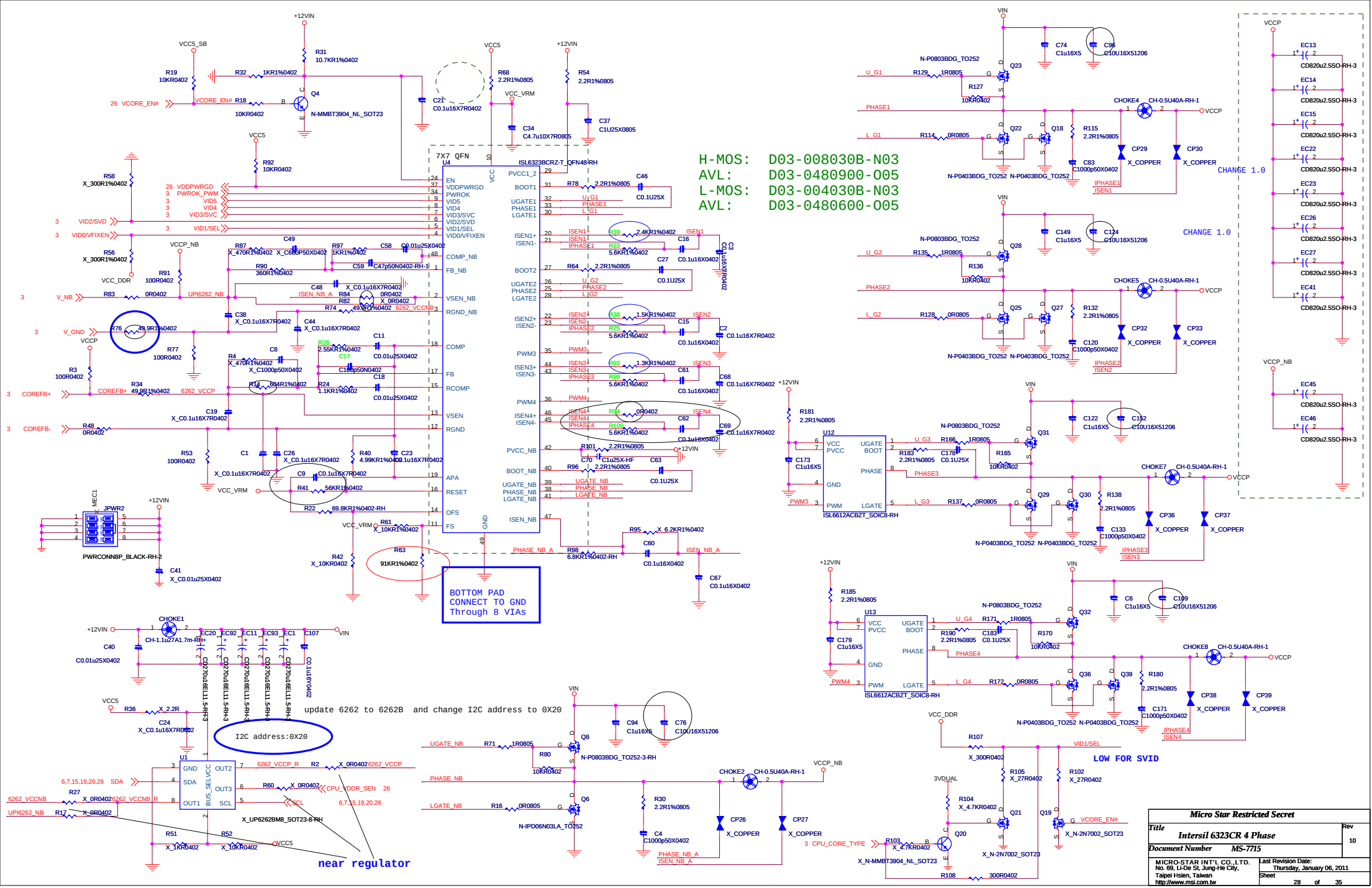
H-MOS: D03-008030B-N03
AVL: D03-0480900-005
L-MOS: D03-004030B-N03
AVL: D03-0480600-005
CHANGE 1.0
CHANGE 1.0
7X7 QFN
ISL6323BCRZ-T_QFN48-RH
BOTTOM PAD
CONNECT TO GND
Through 8 VIAs
update 6262 to 6262B and change I2C address to 0X20
I2C address:0X20
near regulator
LOW FOR SVID
ISL6612ACBZT_SOIC8-RH
ISL6612ACBZT_SOIC8-RH
X_UP6262BM8_SOT23-8-RH
PWRCONN8P_BLACK-RH-2
Micro Star Restricted Secret
Intersil 6323CR 4 Phase
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ATX connector / Front Panel

Intel Front Panel

ESD Protect

For MSI / Intel Front Panel

EMI

Near Super I/O

CHANGE 1.0

follow latest technology suggestion

PS2 KEYBOARD & MOUSE CONNECTOR

SERIAL PORT 1

ATX Connector

5VSB Power Switch

Reference--0515???

Trace Width 80mils.

Option ..... for Normal State

use DIP CAP 10uF or 22uF

use X7R or X5R

change to 0603 10K ohm

Tune 5VSB inrush current to 2A from 4A

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MK1
X_G51-M1SP692-Q13

HS_MOS1
X_OE3-7660002

HS_NB1
HS-0403883-RH

HS_SB1
SB_HEATSINK

PCB1
PK0-0771511-G37
PCB

VBAT1-S1
BAT-BCR2032P-RH

CPU1_1
E91-0000076

Rubber1
PCB
rubber1/2

Rubber2
PCB
rubber1/2

Optics Orientation Holes

FM11 X_FM
FM2 X_FM
FM12 X_FM
FM1 X_FM
FM13 X_FM
FM10 X_FM
FM3 X_FM
FM9 X_FM
FM8 X_FM

Mounting Holes

MH3 X_MH001
MH4 X_MH001
MH5 X_MH001
AGND
MH6 X_MH001
MH1 X_MH001
MH2 X_MH001

Simulation

X_JS1
SIM2
AGND
X_PIN1*2

X_JS2
SIM1
AGND
X_PIN1*2

Lable_01S
OPT
G51-M1SP801

Lable_02S
OPT
G51-M1SP800

REF4
OPT
1000uF 6.3V

REF6
OPT
100uF 16V

REF10
OPT
470uF 16V

REF8
OPT
10uF 16V_audio

REF9
OPT
100uF 16V_audio

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Document Number	*MS-7715*	
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