H61H2-CM

Rev : 1.0.

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/07/29	Base on H67(H61)H2-CM MRS v1.1 2010-08-13
V.1.0	2010/10/26	1:change PWM RT8859AGQW+RT9619APS to ISL6364CRZ +ISL6612ACBZ solution ; 2:change IT8893E BX to CX; 3:change RTL8111E VB to VL version and change RTL8105E VC to VL version; 4:add Power & SI & bug solution; 5:add colay onboard TPM function;
V.1.0.	2010/12/08	1:add STP64 for METS test

1-3. Cougar Point Desktop SKUs

Feature Set		SKU Name(s)					
		Q67	Q65	B65	H67	P67	H61
PCI Express* 2.0 Ports		8	8	8	8	8	6[9]
PCI Interface		Yes	Yes	Yes	No[10]	No[10]	No[10]
USB 2.0 Ports		14	14	12[6]	14	14	10[7]
Total number of SATA ports		6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)		2[4]	1[5]	1[5]	2[4]	2[4]	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)		4	5	5	4	4	4[8]
HDMI/DVI/VGA/DisplayPort*/eDP*		Yes	Yes	Yes	Yes	No	Yes
Integrated Graphics Support with PAVP		Yes	Yes	Yes	Yes	No	Yes
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes	Yes	No
	RAID 0/1/5/10 Support	Yes	No	No	Yes	Yes	No
Intel® AT		Yes	Yes	No	No	No	No
Intel® AMT 7.0		Yes	No	No	No	No	No
Intel® Remote PC Assist Technology - Proactive		Yes	No	Yes	No	No	No
Intel® Remote PC Assist Technology - Reactive		No	No	Yes	Yes	No	No

NOTES:

1. Contact your local Intel Field Sales Representative for currently available PCH SKUs.
2. Table above shows feature differences between the PCH SKUs. If a feature is not listed in the table it is considered a Base feature that is included in all SKUs
3. The PCH provides hardware support for AHCI functionality when enabled by appropriate system configurations and software drivers.
4. SATA 6 Gb/s support on port 0 and port 1. SATA ports 0 and 1 also support 3 Gb/s and 1.5 Gb/s.
5. SATA 6 Gb/s support on port 0 only. SATA port 0 also supports 3 Gb/s and 1.5 Gb/s.
6. USB ports 6 and 7 are disabled.
7. USB ports 6, 7, 12 and 13 are disabled.
8. SATA ports 2 and 3 are disabled.
9. PCIe ports 7 and 8 are disabled.
10. PCI Legacy Mode may optionally be used allowing external PCI bus support through a PCIe-to-PCI bridge. See section 5.1.9 for more details.

NOTE:
Design by
428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev1_5
443554_443554_Cougar_Point_Chipset_Family_EDS_Rev_1.2

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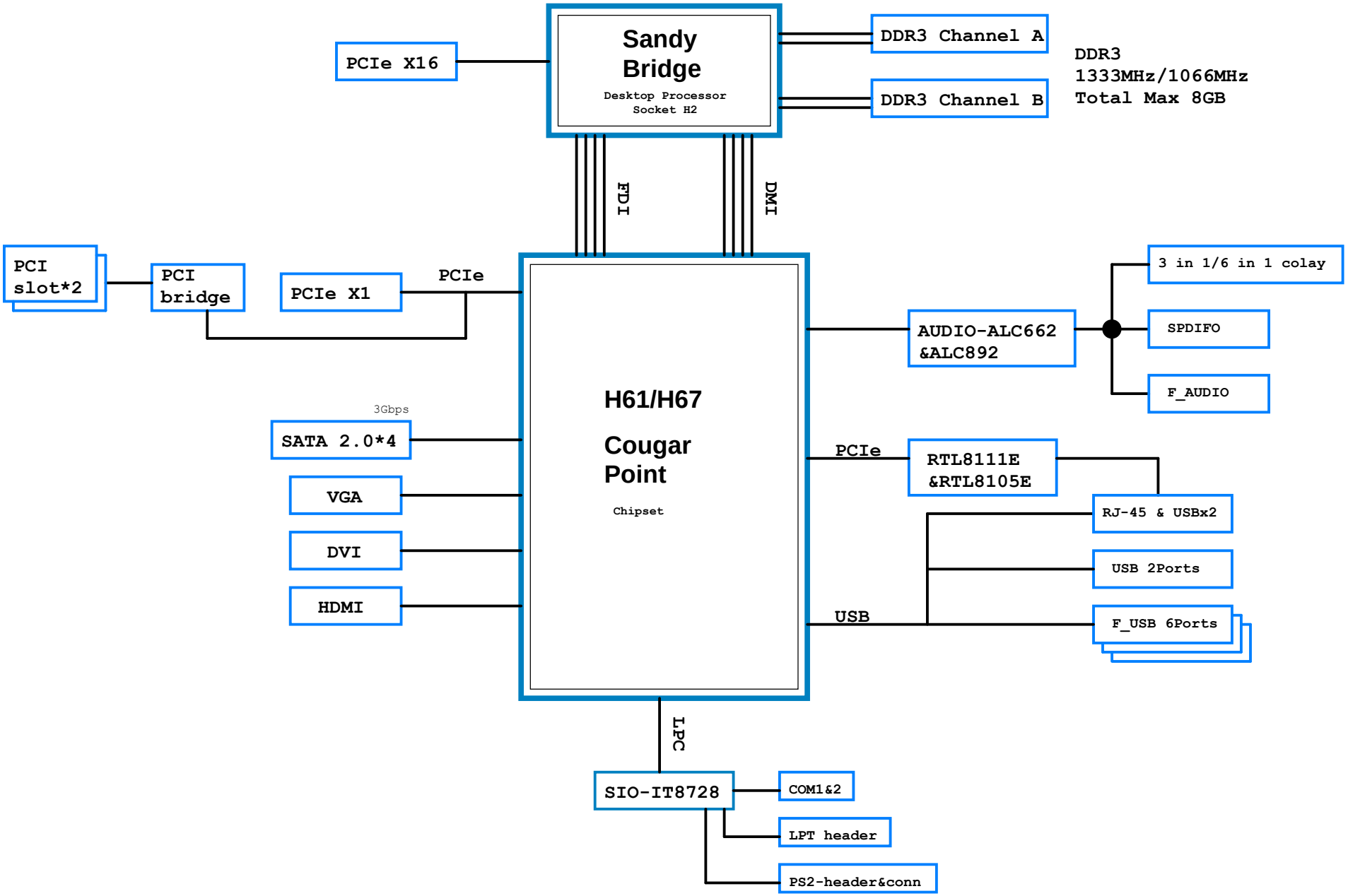

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PCH-GPIO function

	Pin Name	Power Well	Usage	Default Status
	GPIO7	VCC3	SPI_WP0_L	GPI
	GPIO9	3VSB	USB_OC_L5	Native
	GPIO10	3VSB	USB_OC_L6	Native
✶	GPIO12	3VSB	GP12_BOMDET4	Native
	GPIO13	3VSB	LPC_PME_L	GPI
	GPIO14	3VSB	USB_OC_L7	Native
	GPIO16	VCC3	Reserve for TPM	GPI
	GPIO23	VCC3	F_AUD_DETECT_SB	GPI
	GPIO24	3VSB	PCH_SKTOCC_L	GPO
	GPIO40	3VSB	USB_OC_L1	Native
	GPIO41	3VSB	USB_OC_L2	Native
	GPIO42	3VSB	USB_OC_L3	Native
	GPIO43	3VSB	USB_OC_L4	Native
	GPIO49	VCC3	Reserve for TPM	GPI
✶	GPIO57	3VSB	GP57_5V_DETECT	GPI
	GPIO59	3VSB	USB_OC_L0	Native
	GPIO61	VCC3	LPCPD_L	Native
✶	GPIO72	3VSB	GPIO72_BOMDET5	Native

SIO-GPIO function

	Pin Name	Power Well	Usage	Default Status
	GP16	VCC3	SIO_BEEP	
	GP23	3VSB	Power LED	
	GP22	3VSB	Power LED	
	GP40	3VSB	+DIMM_5VDUAL_Control	
✶	GP34	VCC3	RESERVE	
✶	GP35	VCC3	RESERVE	
✶	GP36	VCC3	RESERVE	
✶	GP37	VCC3	RESERVE	

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Title: GPIO Function Map

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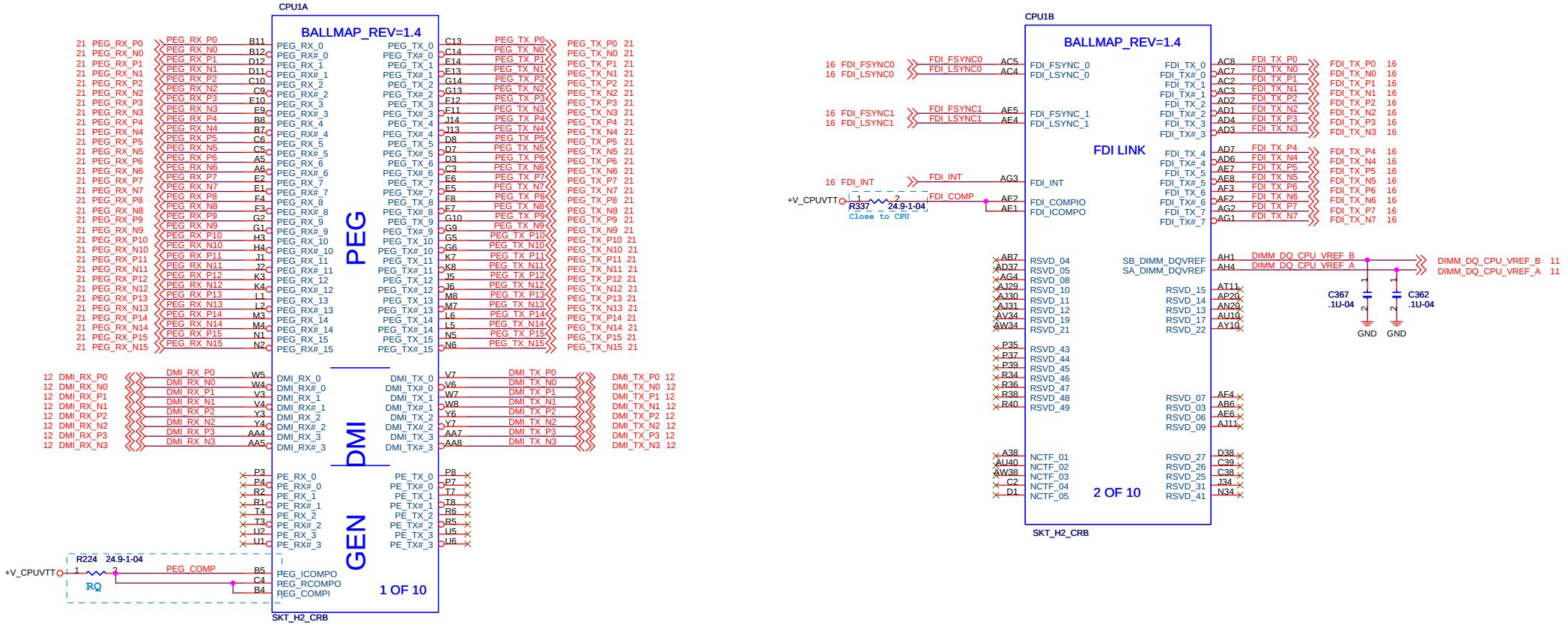

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+V_1P8_SFR
R244 1 2 2.2K-04 PROC_SEL
C242 1 2 .1U-10VX-04 PROC_SEL
GND

DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS
REGARDLESS OF THIS STRAP

+V_CPUVTT
R226 2 1 90.9-1-04-O SVID_CK
R230 2 1 110-1-04 SVID_DATAOUT
R225 2 1 75-1-04 SVID_ALERT_L
Close to CPU

37 VR_SVID_CK
37 VR_SVID_DATAOUT
37 VR_SVID_ALERT_L
VR_SVID_CK
VR_SVID_DATAOUT
VR_SVID_ALERT_L
P13 Short PAD-04
P14 Short PAD-04
P15 Short PAD-04
SVID_ALERT_L R223 1 2 44.2-1-04
SVID_CK C37
SVID_DATAOUT B37
VIDALERT_R_L A37

37 VR_HOT_L
VR_HOT_L P16 Short PAD-04 PROCHOT_L
14 DRAM_PWROK
DRAM_PWROK R340 2 1 120-04 DRAM_PWROK_RC
C331 1 2 .1U-10VX-04-O GND
14 CPU_PWROK
CPU_PWROK R289 2 1 0-04 CPU_PWROK_RC
C255 1 2 .1U-10VX-04-O GND

29 SIO_PCIRST2_L
SIO_PCIRST2_L R17 1 2 2K-1-04 CPU_RST_L
1.1V
R261 2 1 0-04 CPU_RST_L_RC
C247 1 2 .1U-10VX-04-O GND
R22 1K-1-04
GND

CPU1E
BALLMAP_REV=1.4

15 CK_CPU_100M_P
15 CK_CPU_100M_N
CK_CPU_100M_P W2
CK_CPU_100M_N W1
BCLK_0
BCLK#_0
VIDSCLK
VIDSOUT
VIDALERT#

CPU_PWROK_RC J40
DRAM_PWROK_RC AJ19
CPU_RST_L_RC F36
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#

13 PM_SYNC
29 PECI
PM_SYNC E38
PECI J35
CATERR_L F37
PROCHOT_L H34
13 CPU_THERMTRIP_L
CPU_THERMTRIP_L G35
PM_SYNC
PECI
CATERR#
PROCHOT#
THERMTRIP#

14,37 H_SKTOCC_L
16 PROC_SEL
H_SKTOCC_L AJ33
PROC_SEL K32
SKTOCC#
PROC_SEL

DIMM_VREF_CPU AJ22
SM_VREF

R273 1 2 1K-04-O CFG_0 H36
R250 1 2 1K-04-O CFG_1 J36
R258 1 2 1K-04-O CFG_2 J37
R251 1 2 1K-04-O CFG_3 K36
R271 1 2 1K-04-O CFG_4 L36
R293 1 2 1K-04-O CFG_5 N35
R286 1 2 1K-04-O CFG_6 L37
R285 1 2 1K-04-O CFG_7 M36
R270 1 2 1K-04-O CFG_8 J38
R259 1 2 1K-04-O CFG_9 L35
R309 1 2 1K-04-O CFG_10 M38
R294 1 2 1K-04-O CFG_11 N36
R307 1 2 1K-04-O CFG_12 N38
R306 1 2 1K-04-O CFG_13 N39
R308 1 2 1K-04-O CFG_14 N37
R305 1 2 1K-04-O CFG_15 N40
R247 1 2 1K-04-O CFG_16 G37
R246 1 2 1K-04-O CFG_17 G36
Near CPU
GND

CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17

AT14
AY3
H7
H8
RSVD_016
RSVD_023
RSVD_028
RSVD_029

VCCP_SELECT P33
VCCSA_VID P34
VCCSA_SENSE T2
VTT_SEL
VCCSA_VID 35
VCCSA_SEN 35

VCC_SENSE A36
VSS_SENSE B36
VCC_SEN 37
VSS_SEN 37

VCCIO_SENSE AB4
VSSIO_SENSE AB3
VCCIO_SEN 36
VSSIO_SEN 36

VCCAXG_SENSE L32
VSSAXG_SENSE M32
VCCAXG_SEN 37
VSSAXG_SEN 37

TDO L39
TDI L40
TCK M40
TMS L38
TRST# J39
PRDY# K38
PREQ# K40
DBR# E39
H_TDO
H_TDI
H_TCK
H_TMS
H_TRST_L
H_PRDY_L
H_PREQ_L
CPU_DRB
STP53
STP52
STP51
STP50
STP49
STP48
STP47

RSVD_001 C40
RSVD_002 D40
XDP_H_CLK_DP
XDP_H_CLK_DN

BPM#_0 H40
BPM#_1 H38
BPM#_2 G38
BPM#_3 G40
BPM#_4 G39
BPM#_5 F38
BPM#_6 E40
BPM#_7 E40
BPM_L_0
BPM_L_1
BPM_L_2
BPM_L_3
BPM_L_4
BPM_L_5
BPM_L_6
BPM_L_7
STP54
STP55
STP56
STP57
STP58
STP59
STP60
STP61

RSVD_024 B39
RSVD_030 J33
RSVD_037 L34
RSVD_036 L33
RSVD_033 K34
RSVD_040 N33
RSVD_039 M34
RSVD_018 AV1
RSVD_020 AW2
RSVD_038 L9
RSVD_032 J9
RSVD_034 K9
RSVD_035 L31
RSVD_050 J31
RSVD_053 K31
RSVD_051 AD34
RSVD_052 AD35

5 OF 10
SKT_H2_CRB

+VCC
R264 10K-04
R263 4.7K-04
GND
VTT_SEL 36

+3VSB
R297 220-04-O
P17 Short PAD-04
FP_RST_L
FP_RST_L 14,31

R276 2 1 0-04-O XDP_CPU_CLK_DP 15
R291 2 1 0-04-O XDP_CPU_CLK_DN 15
XDP_CPU_CLK_DP 15
XDP_CPU_CLK_DN 15
0729 Change

+V_CPUVTT
RN26 51-8P4R-O
H_TRST_L
H_TMS
H_TDI
H_TCK
R310 51.1-1-04-O
H_TDO
GND

EDS P68/132 has internal PU

+V_CPUVTT
CPU_PWROK R290 51.1-04-O
PECI R235 1K-04-O
CATERR_L R260 1K-04-O
PROCHOT_L R243 51-04
CPU_THERMTRIP_L R236 51-04-O
CATERR_L, CPU_THERMTRIP_L Pull Up Resistor 2010 MoW05 Remove

+3VSB
R300 10K-04
VR_EN
VR_EN 37
TO VRD FOR S0->S5
C269 2.2U-O
QN2_C R320 1K-04 QN1_B QN8 PMBS3904-S
R299 10K-04 QN2_B QN6 PMBS3904-S
SLP3_L
14,25,28,29,33,34,35 SLP3_L
QN3_C R324 100-04 VR_READY
VR_READY 14,37
FROM VRD
QN3_B R319 1K-04 QN10 PMBS3904-S
QN4_C R321 100-04-O CPU_PWROK
CPU_PWROK 14
R322 1K-04
QN4_B R328 1K-04-O QN9 PMBS3904-S-O
GND

Power Down Sequencing Circuit

+DIMM_5VDUAL
R600 Short PAD
R611 Short PAD
U30B LM358DS-O
GND

V1.0: 若有沒用到的OP請如下圖接法，
input pin通過short pad短路後共同下地，
output pin開NC

Mcpu
+3VSB
Address:??ch
+V_1P5_SM
+DIMM_5VDUAL
C354 .1U-X7-04-O
U28
VDD A
GND W
SCL SDA
AD5247-O
SMBCLK_STBY
SMBDATA_STBY
R367 12.1K-1-04-O
C352 1U-6V3X-04-O
C364 1U-25V-08-O
DIMM_VREF_CPU_1
R372 12.1K-1-04-O
U30A LM358DS-O
DIMM_VREF_CPU_2
R370 2.2-04-O
MCPU_NCPU
R369 12.1K-1-04-O
C353 1U-04-O
GND

Ncpu
R364 0-04-O

Pcpu
+V_1P5_SM
R365 100-1-04
R363 100-1-04
Place Pcpu in Socket Cavity.

Layout Note:
All Parts Close yo CPU

SMBCLK_STBY
SMBDATA_STBY
SMBCLK_STBY 14,15,21
SMBDATA_STBY 14,15,21

DIMM_VREF_CPU
SC26 .1U-04-X

DIMM_VREF_CPU Control Mode:

Control Mode / Part	Divider	PCH + Controller
Mcpu	X	V
Ncpu	X	V
Pcpu	V	X

Default

Programmable DIMM_VREF_CPU CIRCUIT

DIMM_VREF_CPU Control Circuit

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

*

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

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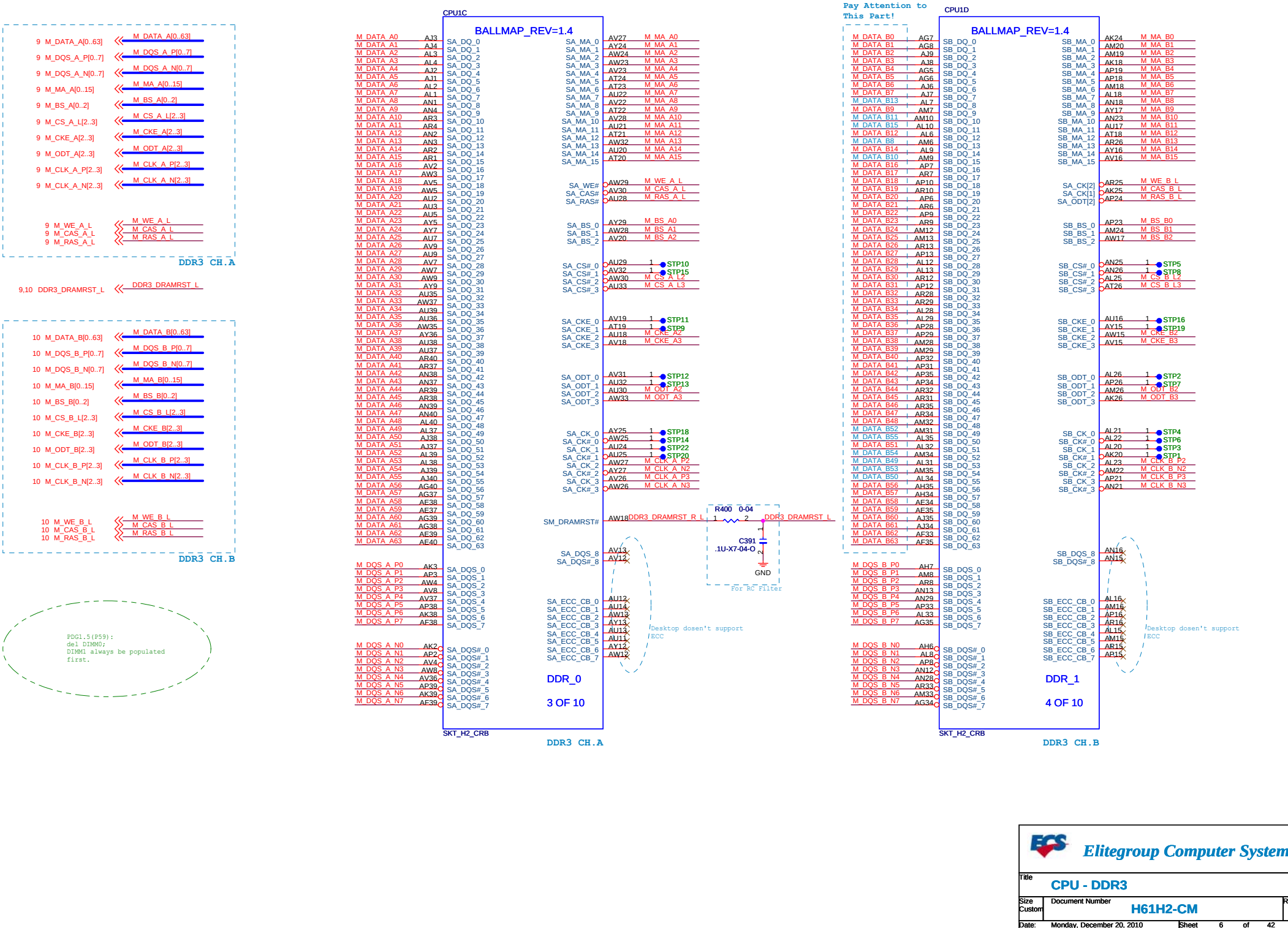

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MAX 112A
In +VCORE

CPU1F

BALLMAP_REV=1.4

SKT_H2_CRB

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MAX 112A
In +VCORE

1.05V/1.00V
MAX 8.5A
In +V_CPUVTT

CPU1G

BALLMAP_REV=1.4

0.925V/0.85V
MAX 8.8A
In +V_SA

1.8V
MAX 1A
In +V_1P8_SFR

POWER
7 OF 10

SKT_H2_CRB

1.5V
MAX 4.5A
In +V_1P5_SM

MAX 35A
In +VAXG

CPU1H

VBALLMAP_REV=1.4

8 OF 10

SKT_H2_CRB

+V_CPUVTT

C318 .1U-10VX-04 C336 .1U-10VX-04 C235 .1U-10VX-04 C327 .1U-10VX-04 C261 .1U-10VX-04
C311 .1U-10VX-04 C293 .1U-10VX-04 C317 .1U-10VX-04 C232 .1U-10VX-04
C233 .1U-10VX-04 C231 .1U-10VX-04 C249 .1U-10VX-04 C258 .1U-10VX-04
C251 .1U-10VX-04 C234 .1U-10VX-04 C268 .1U-10VX-04

GND

DECOUPLING & STITCHING CAPS.

+V_CPUVTT +V_SA

C218 22U-6VX-08
C262 22U-6VX-08
SC69 22U-6VX-08-X-O
V1.0:reserve

GND

PLACE NEAR SKT EDGE
OUTSIDE CAVITY.

+VCORE

C229 22U-6VX-08-O C227 22U-6VX-08-O C228 22U-6VX-08-O C230 22U-6VX-08-O
V1.0:unstuff for power

GND

PLACE NEAR SKT EDGE
OUTSIDE CAVITY.

+V_1P8_SFR

C315 .1U-10VX-04 C312 22U-6VX-08

GND

+VCORE

C570 22U-6VX-08 C572 22U-6VX-08 C573 22U-6VX-08 C575 22U-6VX-08 C577 22U-6VX-08
V1.0 : add 5*top+3*bottom
SC71 22U-6VX-08-X-O SC72 22U-6VX-08-X SC73 22U-6VX-08-X
V1.0:stuff SC72 for power

GND

+V_CPUVTT

V1.0:remove C296,C272

C322 22U-6VX-08 C298 22U-6VX-08 C319 22U-6VX-08 C297 22U-6VX-08
C299 22U-6VX-08 C302 22U-6VX-08 C294 22U-6VX-08 C295 22U-6VX-08

GND

+VAXG

C307 22U-6VX-08 C287 22U-6VX-08 C283 22U-6VX-08 SC10 22U-6VX-08-X
V1.0:Power Team
SC20 22U-6VX-08-X C300 22U-6VX-08 SC65 22U-6VX-08-X SC66 22U-6VX-08-X
V1.0 : add 2*bottom

GND

+VCORE

V1.0:stuff SC8 for power

SC5 22U-6VX-08-X SC9 22U-6VX-08-X SC8 22U-6VX-08-X SC7 22U-6VX-08-X C276 22U-6VX-08 C281 22U-6VX-08 C280 22U-6VX-08 SC68 22U-6VX-08-X
V1.0:Reserve
SC2 22U-6VX-08-X SC6 22U-6VX-08-X C278 22U-6VX-08 C279 22U-6VX-08 C277 22U-6VX-08 C273 22U-6VX-08 SC4 22U-6VX-08-X SC67 22U-6VX-08-X
V1.0 : add 2*bottom

GND

+V_1P5_SM

C313 22U-6VX-08 C320 22U-6VX-08 C321 22U-6VX-08

GND

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY, TOPSIDE.

+V_CPUVTT

SC23 22U-6VX-08-O SC18 22U-6VX-08-O SC24 22U-6VX-08-O SC17 22U-6VX-08-O
SC14 22U-6VX-08-O SC25 22U-6VX-08-O SC11 22U-6VX-08-O
V1.0:del C285,C288,SC3, SC16,SC13,SC15,SC19,SC21

GND

+VAXG

SC22 22U-6VX-08-X-O SC12 22U-6VX-08-X
C574 22U-6VX-08 C578 22U-6VX-08
V1.0 : add 2*top

GND

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY, BACKSIDE.

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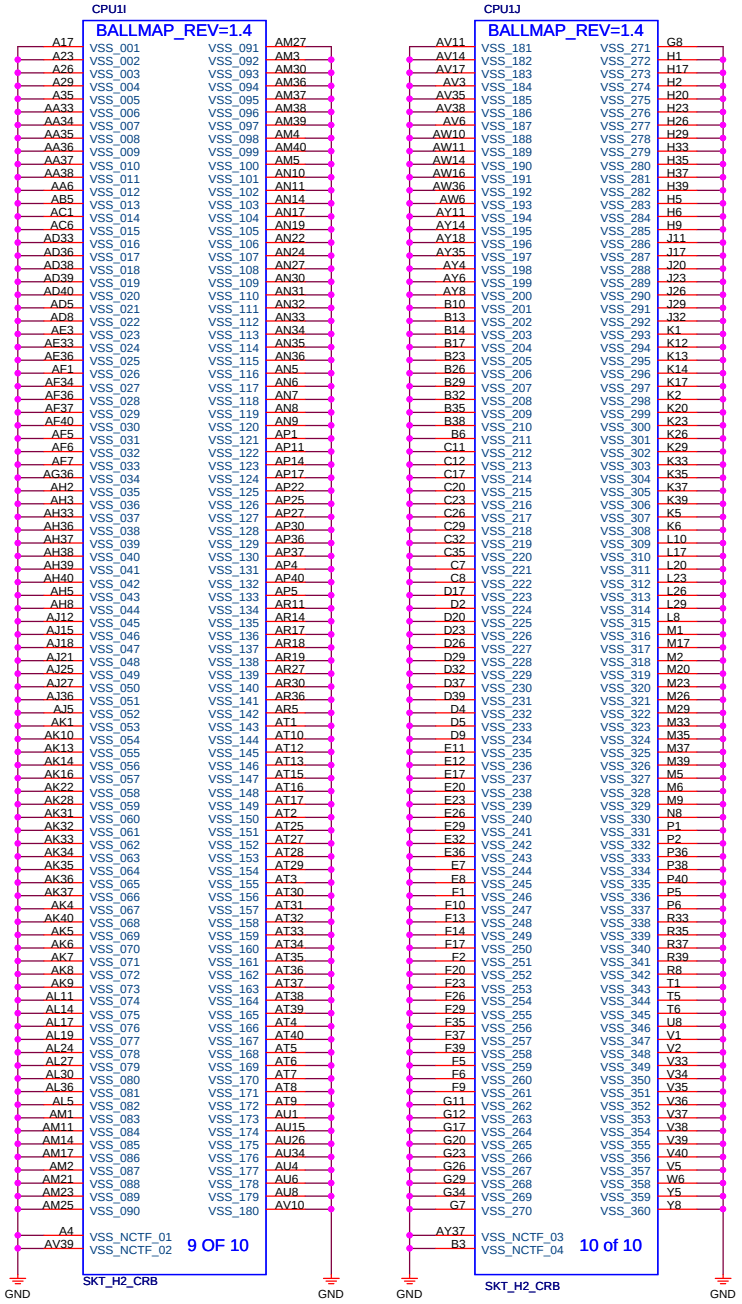

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Title: CPU - GND

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CHANNEL A DIMM

CH.A	SA1	SA0
DIMM0	L	L
DIMM1	L	H

M_DQS_A_P[0..7] M_DQS_A_P[0..7] 6
M_DQS_A_N[0..7] M_DQS_A_N[0..7] 6

Desktop dosen't support ECC

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

M_DATA_A[0..63] M_DATA_A[0..63] 6

DDR3-240P DIMM1

+V_SM_VTT
0.75V
MAX 1A

+V_1P5_SM
1.5V
MAX 15A
S3 1.0A

6 M_ODT_A[2..3] M_ODT_A[2..3]
6 M_CS_A_L[2..3] M_CS_A_L[2..3]
6 M_CKE_A[2..3] M_CKE_A[2..3]
6 M_CLK_A_P[2..3] M_CLK_A_P[2..3]
6 M_CLK_A_N[2..3] M_CLK_A_N[2..3]

11 DIMM_VREF_CA_A DIMM_VREF_CA_A
11 DIMM_VREF_DQ_A DIMM_VREF_DQ_A
10,15,19 SMBCLK_MAIN SMBCLK_MAIN
10,15,19 SMBDATA_MAIN SMBDATA_MAIN

6 M_BS_A[0..2] M_BS_A[0..2]

M_MA_A[0..15] M_MA_A[0..15] 6

M_WE_A_L M_WE_A_L 6
M_RAS_A_L M_RAS_A_L 6
M_CAS_A_L M_CAS_A_L 6
DDR3_DRAMRST_L DDR3_DRAMRST_L 6,10

Design note:
DIMM: CH A BANK 2
CH A SMB ADDRESS 001
CH A SPD READ/WR: 0*A3, 0*A2
SPD=SERIAL PRESENCE DETECT

+V_1P5_SM
V1.0:unstuff
C417 1U-10VX-04
C415 1U-10VX-04
C421 1U-10VX-04
C386 1U-10VX-04
C389 1U-10VX-04
+V_SM_VTT
C368 4.7U-25VX5-08
C372 .1U-04
GND
CH A V_SM_VTT DECOUPLING CAPS

+V_1P5_SM
V1.0:unstuff
C454 22U-6VX-08
C457 22U-6VX-08
C424 22U-6VX-08
C414 22U-6VX-08
C446 22U-6VX-08
GND
Between CHA&CHB

+VCC3
C445 .1U-04-O
C404 .1U-04-O
GND
PLACE BETWEEN CHA &CHB.
DO NOT PUNCH VIA.

Elitegroup Computer Systems

Title	DDR3 - CHA DIMM1		
Size: Custom	Document Number: H61H2-CM		Rev: V1.0
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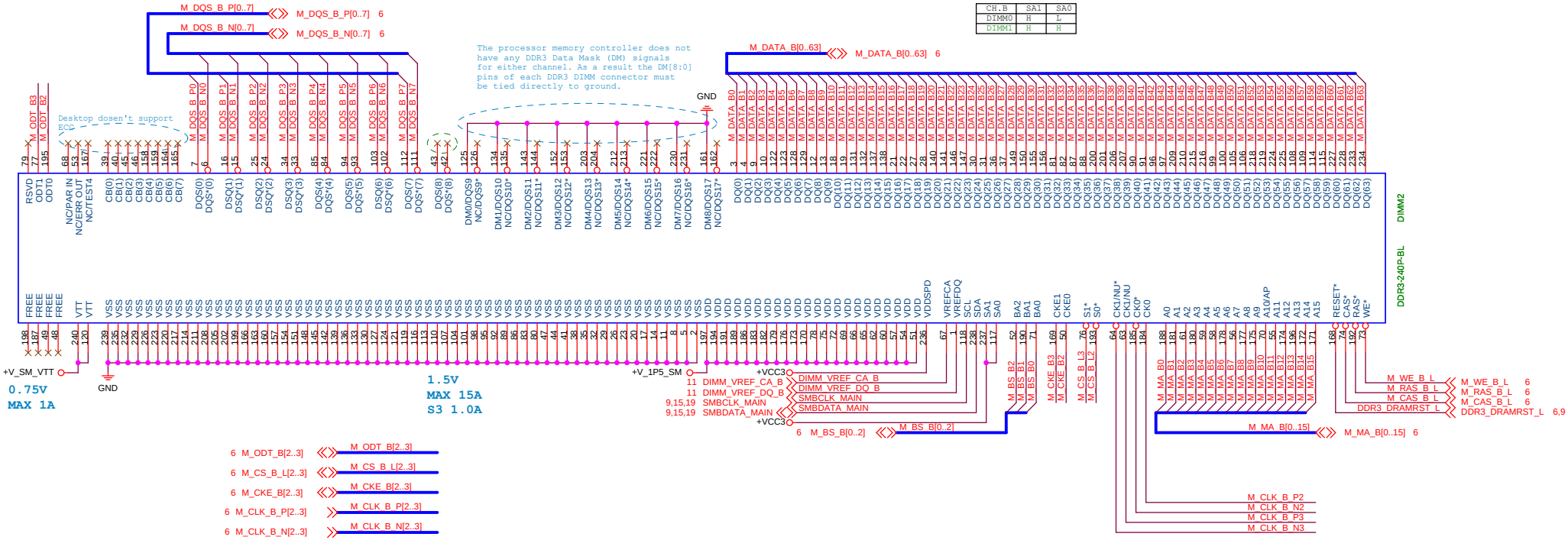
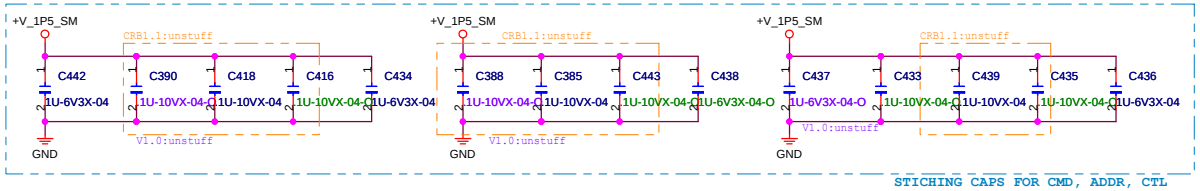
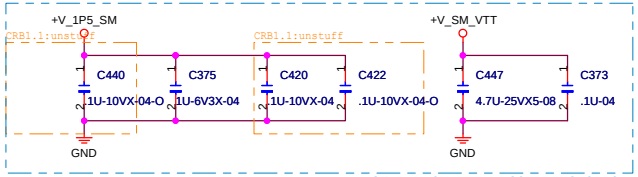
CHANNEL B DIMMs



CH.B	SA1	SA0
DIMM0	H	L
DIMM1	H	H





Design note:
DIMM: CH B BANK 2
CH B SMB ADDRESS 011
CH B SPD READ/WR: 0*A7, 0*A6
SPD=SERIAL PRESENCE DETECT

Elitegroup Computer Systems

Title	DDR3 - CHB DIMM1	
Size: Custom	Document Number: H61H2-CM	Rev: V1.0
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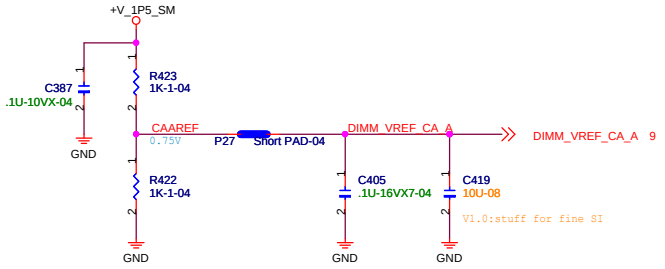
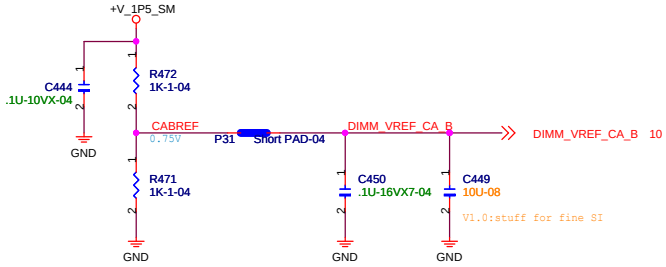
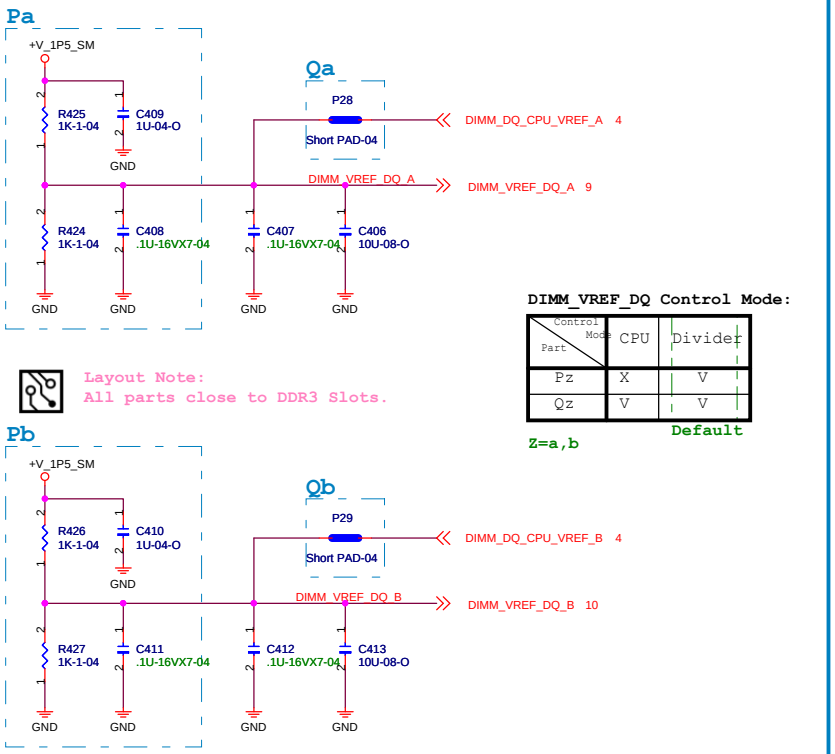




DIMM_VREF_CA Circuit



DIMM_VREF_DQ Control Mode:

Part \ Control Mode	CPU	Divider
Pz	X	V
Qz	V	V

Default

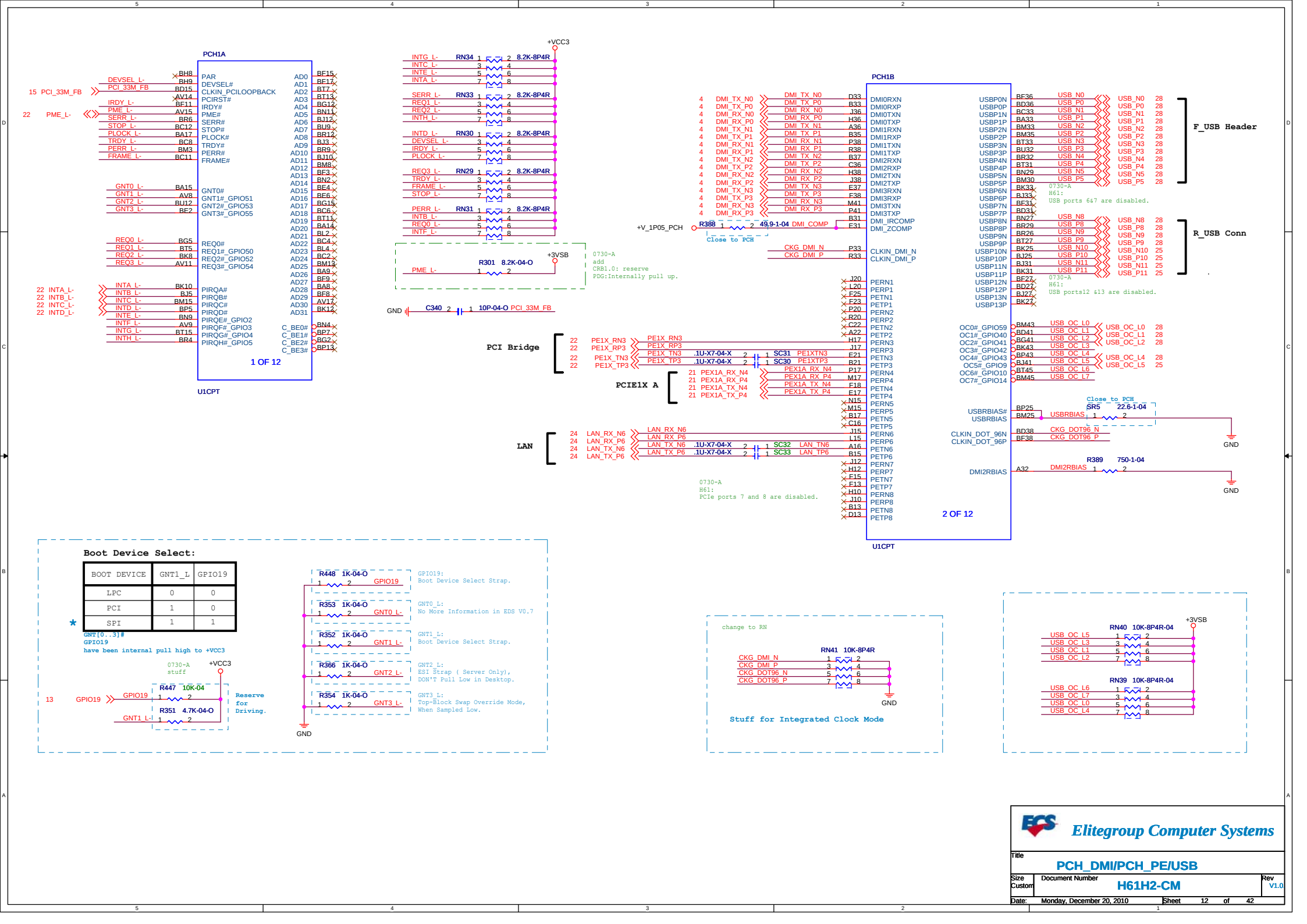
Z=a,b

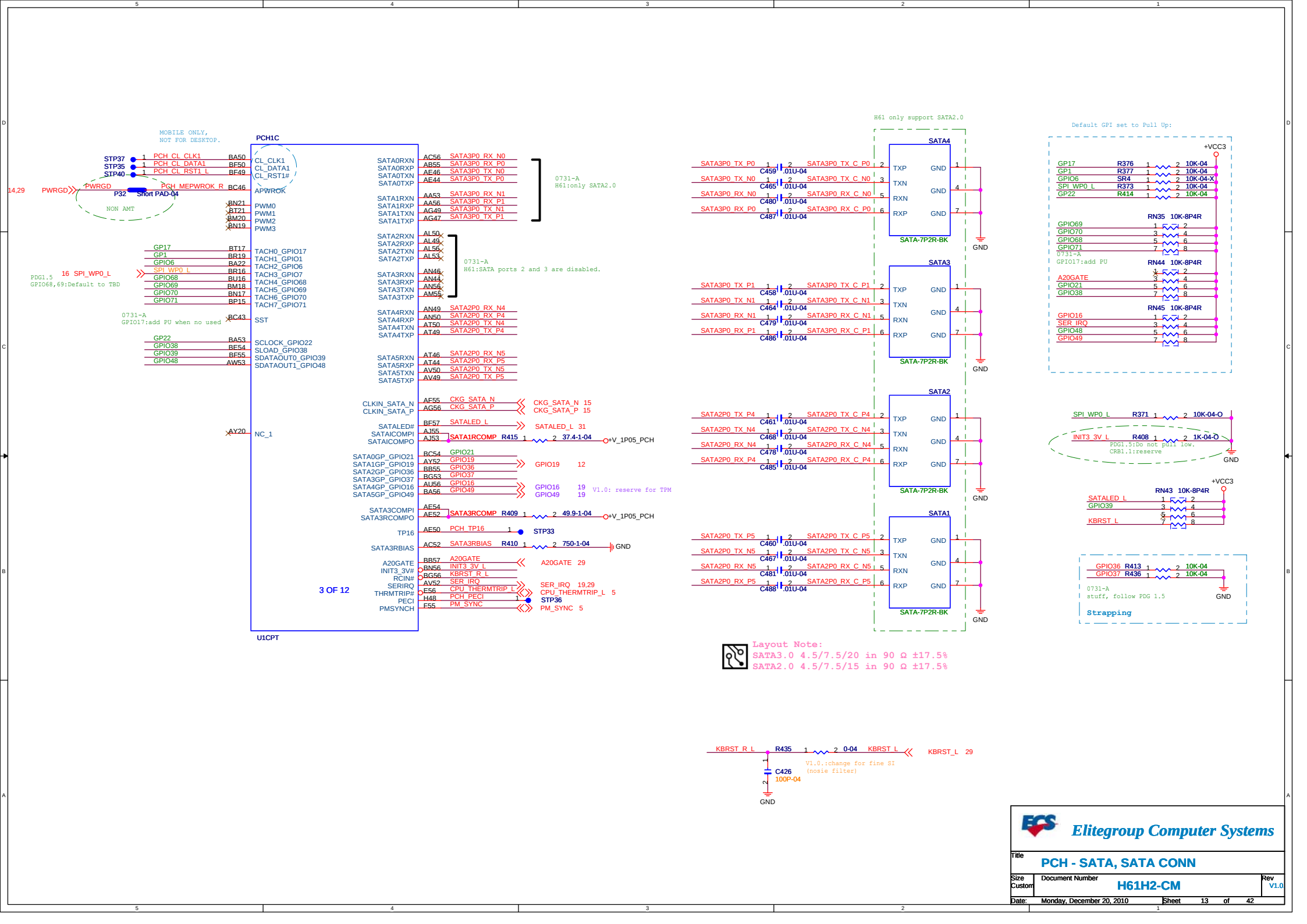
DIMM_VREF_DQ Control Circuit

0729
REMOVE Programmable VREFDQ circuit For PDG 1.5 update

Elitegroup Computer Systems

Title: DDR3 - VREF		
Size: Custom	Document Number: H61H2-CM	Rev: V1.0
Date: Monday, December 20, 2010	Sheet 11 of 42	


PCH1A
1 OF 12
U1CPT
PCH1B
2 OF 12
PCI Bridge
PCIE1X A
LAN
F_USB Header
R_USB Conn
Boot Device Select:
Stuff for Integrated Clock Mode
Elitegroup Computer Systems
PCH_DMI/PCH_PE/USB
H61H2-CM
Monday, December 20, 2010



Elitegroup Computer Systems

Title	PCH - SATA, SATA CONN	
Size: Custom	Document Number: H61H2-CM	Rev: V1.0
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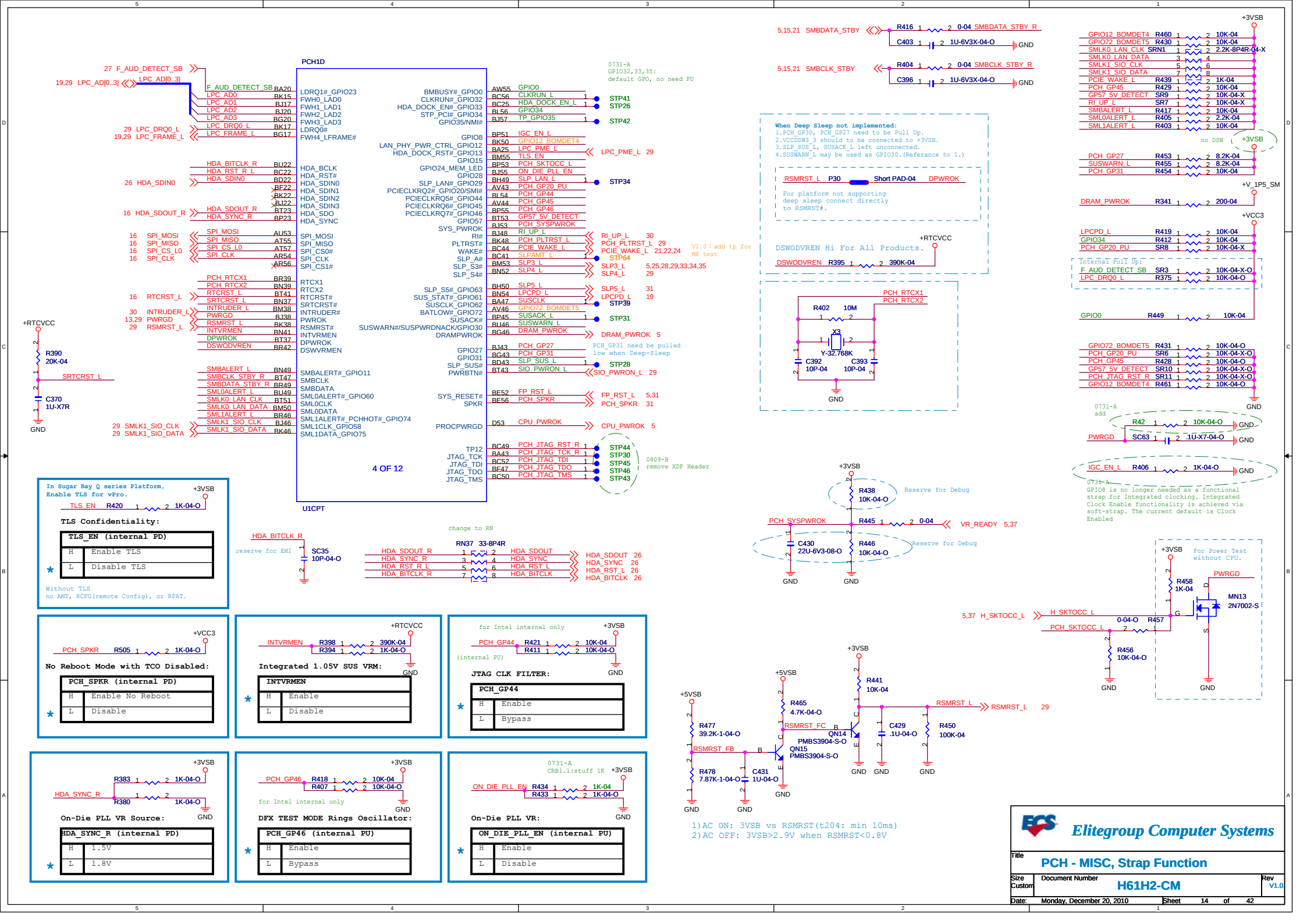
PCH1D
U1CPT
4 OF 12
0731-A
GPIO32,33,35:
default GPO, no need PU
When Deep Sleep not implemented:
1.PCH_GP30, PCH_GP27 need to be Pull Up.
2.VCCDSW3_3 should to be connected to +3VSB.
3.SLP_SUS_L, SUSACK_L left unconnected.
4.SUSWARN_L may be used as GPIO30.(Reference to 1.)
RSMRST_L P30 Short PAD-04 DPWROK
For platform not supporting deep sleep connect directly to RSMRST#.
DSWODVREN Hi For All Products.
DSWODVREN R395 390K-04
+RTCVCC
PCH_RTCX1
PCH_RTCX2
R402 10M
X3
Y-32.768K
C392 10P-04
C393 10P-04
GND
5,15,21 SMBDATA_STBY
R416 0-04 SMBDATA_STBY_R
C403 1U-6V3X-04-O
5,15,21 SMBCLK_STBY
R404 0-04 SMBCLK_STBY_R
C396 1U-6V3X-04-O
+3VSB
GPIO12_BOMDET4 R460 10K-04
GPIO72_BOMDET5 R430 10K-04
SMLK0_LAN_CLK SRN1 2.2K-8P4R-04-X
SMLK0_LAN_DATA
SMLK1_SIO_CLK
SMLK1_SIO_DATA
PCIE_WAKE_L R439 10K-04
PCH_GP45 R429 10K-04
GP57_5V_DETECT SR9 10K-04-X
RI_UP_L SR7 10K-04-X
SMBALERT_L R417 10K-04
SMLK0ALERT_L R405 2.2K-04
SMLK1ALERT_L R403 10K-04
no DSW
PCH_GP27 R453 8.2K-04
SUSWARN_L R455 8.2K-04
PCH_GP31 R454 10K-04
+V_1P5_SM
DRAM_PWROK R341 200-04
+VCC3
LPCPD_L R419 10K-04
GPIO34 R412 10K-04
PCH_GP20_PU SR8 10K-04-X
Internal Pull Up:
F_AUD_DETECT_SB SR3 10K-04-X-O
LPC_DRQ0_L R375 10K-04-O
GPIO0 R449 10K-04
GPIO72_BOMDET5 R431 10K-04-O
PCH_GP20_PU SR6 10K-04-X-O
PCH_GP45 R428 10K-04-O
GP57_5V_DETECT SR10 10K-04-X-O
PCH_JTAG_RST_R SR11 10K-04-X-O
GPIO12_BOMDET4 R461 10K-04-O
0731-A add
R42 10K-04-O
PWRGD SC63 .1U-X7-04-O
IGC_EN_L R406 1K-04-O
0731-A
GPIO8 is no longer needed as a functional strap for Integrated clocking. Integrated Clock Enable functionality is achieved via soft-strap. The current default is Clock Enabled
+RTCVCC
R390 20K-04
SRTCRST_L
C370 1U-X7R
GND
In Sugar Bay Q series Platform, Enable TLS for vPro.
TLS_EN R420 1K-04-O
TLS Confidentiality:
TLS_EN (internal PD)
H Enable TLS
L Disable TLS
Without TLS no AMT, RCFG(remote Config), or RPAT.
HDA_BITCLK_R
reserve for EMI
SC35 10P-04-O
change to RN
RN37 33-8P4R
HDA_SDOUT_R
HDA_SYNC_R
HDA_RST_R_L
HDA_BITCLK_R
HDA_SDOUT 26
HDA_SYNC 26
HDA_RST_L 26
HDA_BITCLK 26
+3VSB
R438 10K-04-O
Reserve for Debug
PCH_SYSPWROK
R445 0-04
VR_READY 5,37
C430 22U-6V3-08-O
R446 10K-04-O
Reserve for Debug
GND
+VCC3
PCH_SPKR R505 1K-04-O
No Reboot Mode with TCO Disabled:
PCH_SPKR (internal PD)
H Enable No Reboot
L Disable
+RTCVCC
INTVRMEN R398 390K-04
R394 1K-04-O
Integrated 1.05V SUS VRM:
INTVRMEN
H Enable
L Disable
for Intel internal only
PCH_GP44 R421 10K-04
R411 10K-04-O
(internal PU)
JTAG CLK FILTER:
PCH_GP44
H Enable
L Bypass
+3VSB
R383 1K-04-O
HDA_SYNC_R
R380 1K-04-O
On-Die PLL VR Source:
HDA_SYNC_R (internal PD)
H 1.5V
L 1.8V
PCH_GP46 R418 10K-04
R407 10K-04-O
for Intel internal only
DFX TEST MODE Rings Oscillator:
PCH_GP46 (internal PU)
H Enable
L Bypass
0731-A
CRB1.1:stuff 1K
ON_DIE_PLL_EN R434 1K-04
R433 1K-04-O
On-Die PLL VR:
ON_DIE_PLL_EN (internal PU)
H Enable
L Disable
+5VSB
R477 39.2K-1-04-O
RSMRST_FB
R478 7.87K-1-04-O
C431 1U-04-O
R465 4.7K-04-O
RSMRST_FC
QN15 PMBS3904-S-O
QN14 PMBS3904-S-O
R441 10K-04
C429 .1U-04-O
R450 100K-04
RSMRST_L
RSMRST_L 29
1)AC ON: 3VSB vs RSMRST(t204: min 10ms)
2)AC OFF: 3VSB>2.9V when RSMRST<0.8V
For Power Test without CPU.
5,37 H_SKTOCC_L
H_SKTOCC_L
PCH_SKTOCC_L
0-04-O R457
R458 1K-04
R456 10K-04-O
MN13 2N7002-S
PWRGD
Elitegroup Computer Systems
Title
PCH - MISC, Strap Function
Size Custom
Document Number H61H2-CM
Rev V1.0
Date: Monday, December 20, 2010
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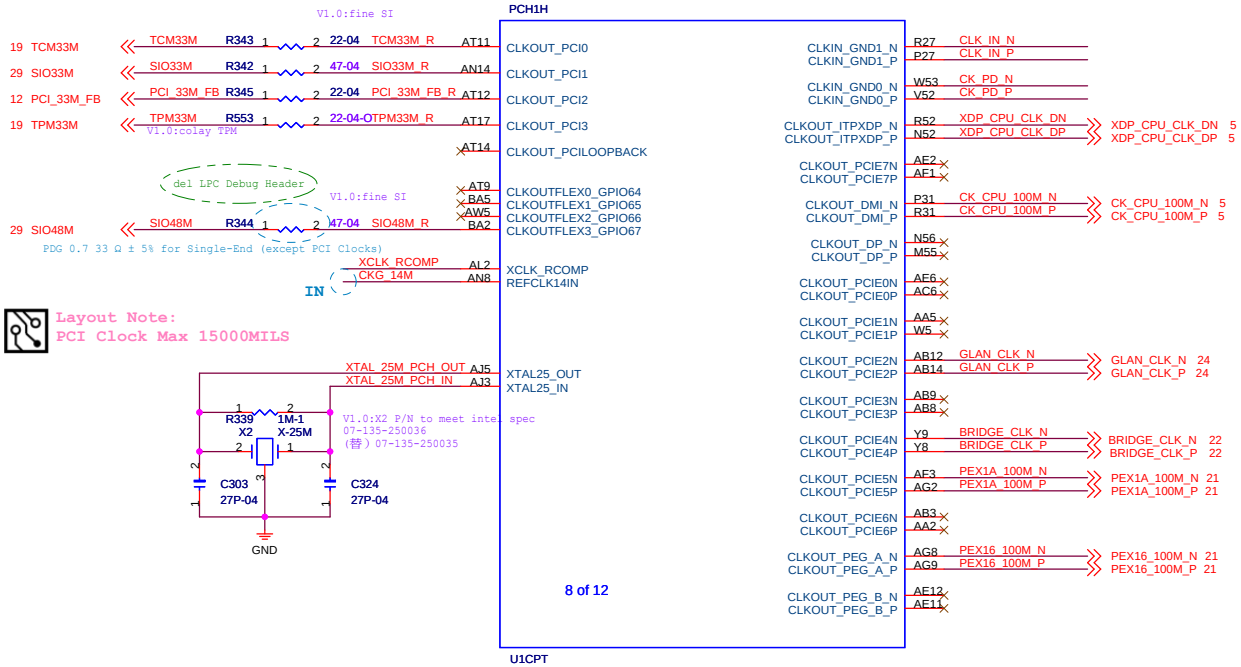

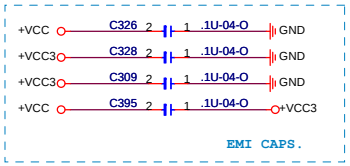

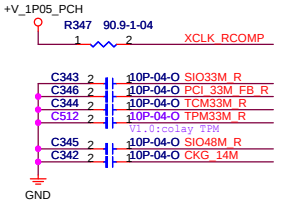

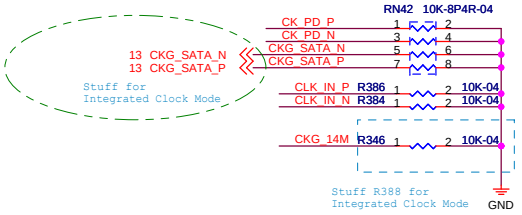

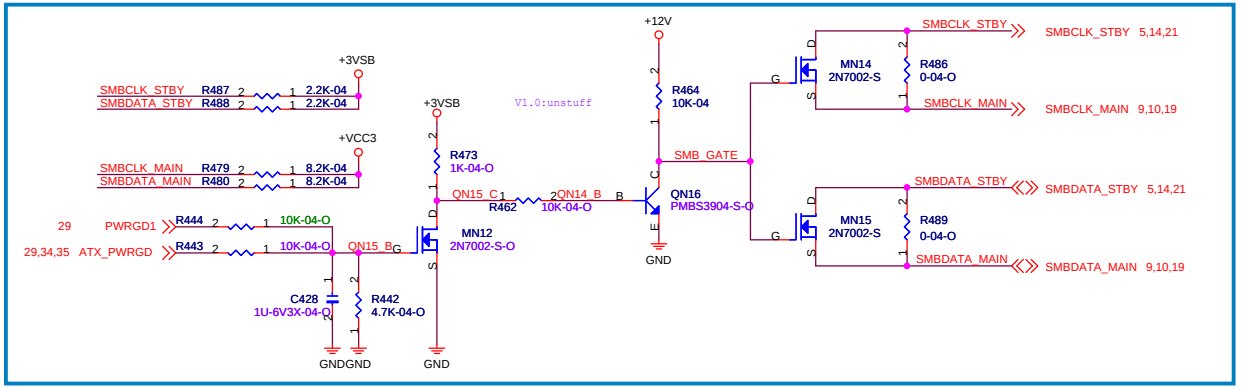

SMBUS Logic Circuit

Elitegroup Computer Systems			
Title: PCH - CLK IO,SMbu			
Size: Custom	Document Number: H61H2-CM		Rev: V1.0
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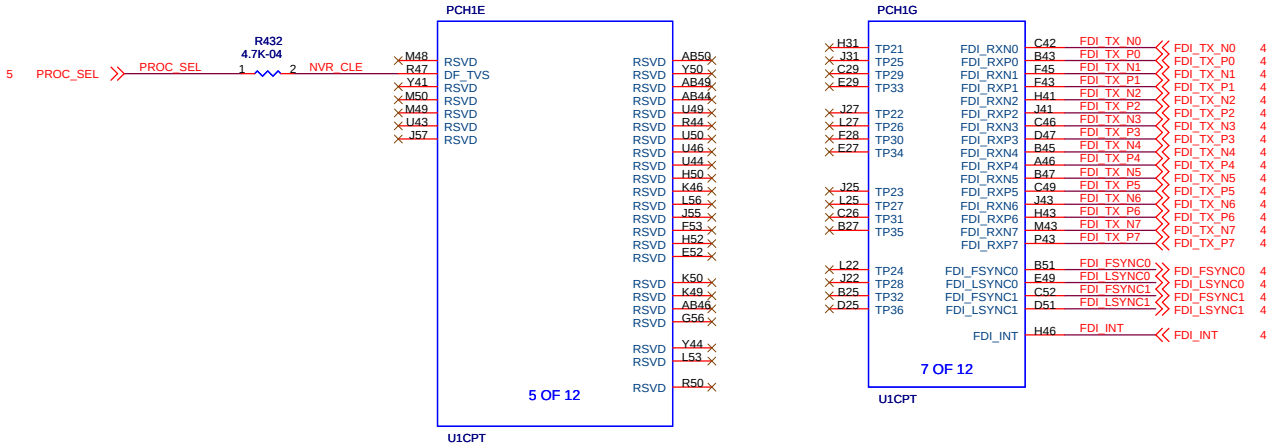
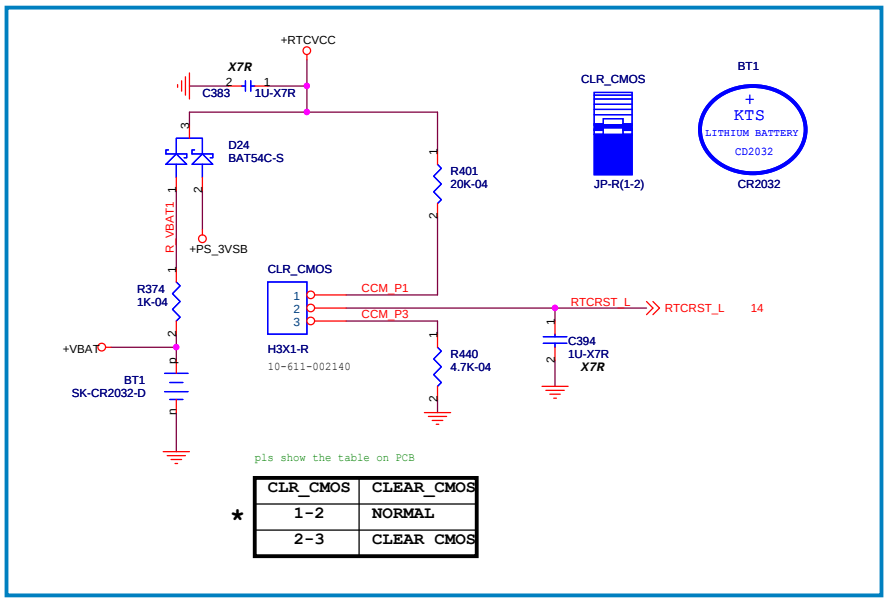
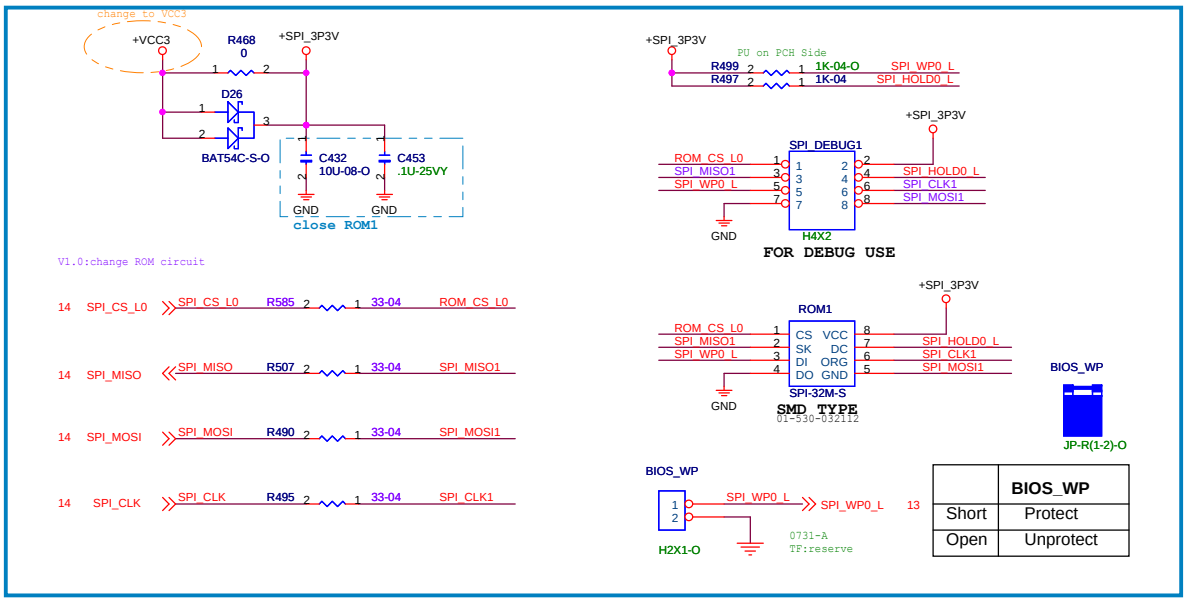




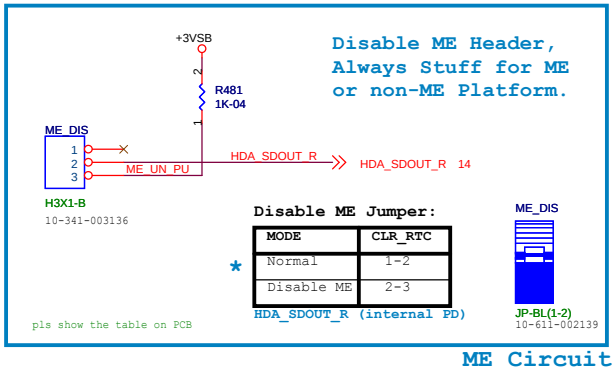
CLR_CMOS	CLEAR_CMOS
1-2	NORMAL
2-3	CLEAR CMOS

CLR_CMOS Circuit



BIOS_WP	
Short	Protect
Open	Unprotect

SPI ROM Circuit



MODE	CLR_RTC
Normal	1-2
Disable ME	2-3

ME Circuit

Elitegroup Computer Systems

Title: FDI,CLR_CMOS,ROM

Size	Document Number	Rev
Custom	H61H2-CM	V1.0

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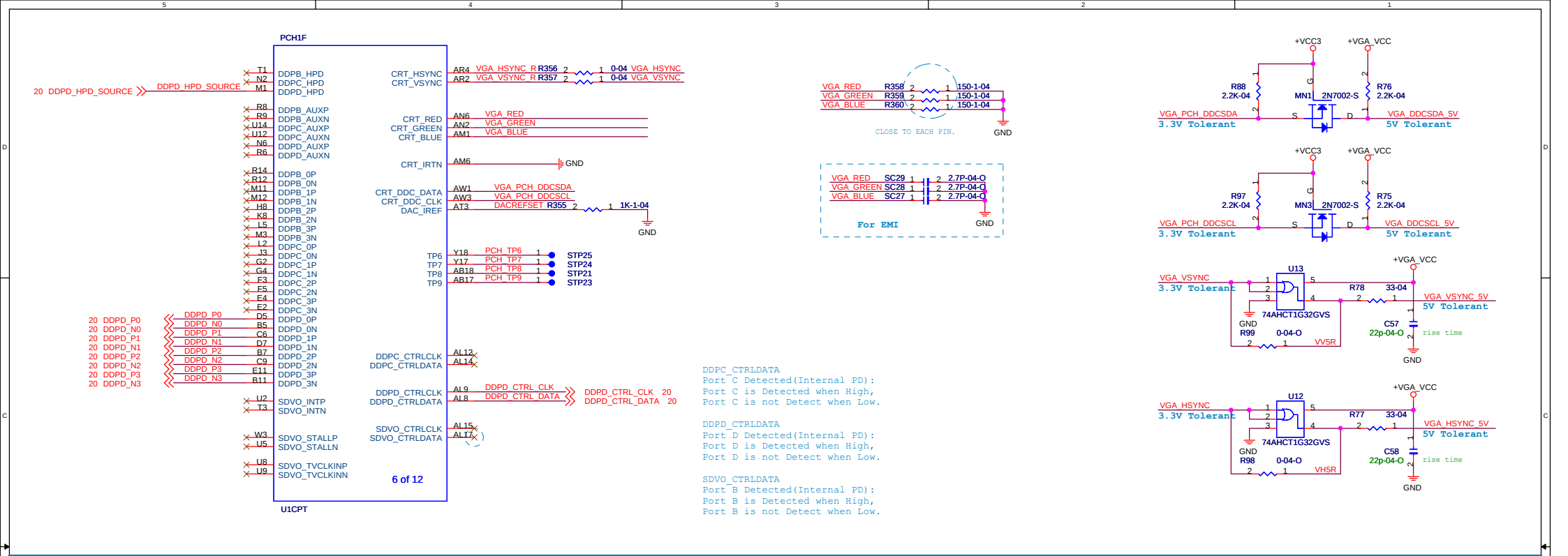
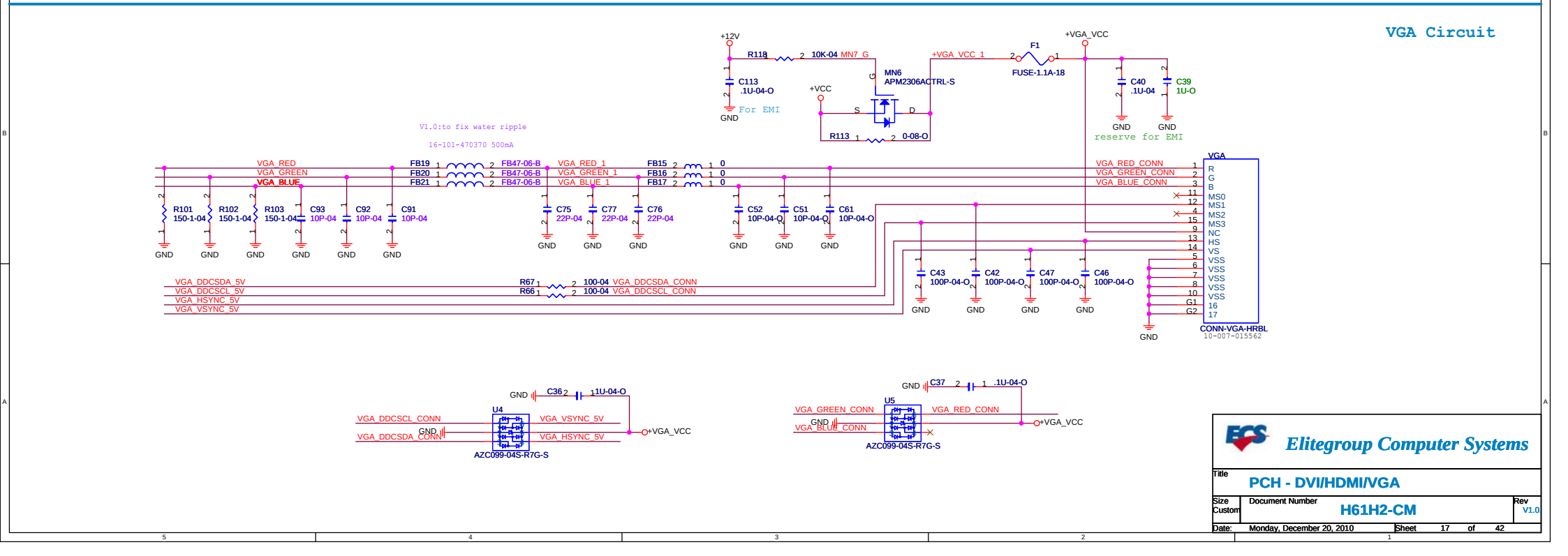

PCH1F
DDPB_HPD
DDPC_HPD
DDPD_HPD
DDPB_AUXP
DDPB_AUXN
DDPC_AUXP
DDPC_AUXN
DDPD_AUXP
DDPD_AUXN
DDPB_0P
DDPB_0N
DDPB_1P
DDPB_1N
DDPB_2P
DDPB_2N
DDPB_3P
DDPB_3N
DDPC_0P
DDPC_0N
DDPC_1P
DDPC_1N
DDPC_2P
DDPC_2N
DDPC_3P
DDPC_3N
DDPD_0P
DDPD_0N
DDPD_1P
DDPD_1N
DDPD_2P
DDPD_2N
DDPD_3P
DDPD_3N
SDVO_INTP
SDVO_INTN
SDVO_STALLP
SDVO_STALLN
SDVO_TVCLKINP
SDVO_TVCLKINN
6 of 12
U1CPT
DDPD_HPD_SOURCE
CRT_HSYNC
CRT_VSYNC
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_IRTN
CRT_DDC_DATA
CRT_DDC_CLK
DAC_IREF
VGA_HSYNC_R R356
VGA_VSYNC_R R357
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
GND
VGA_PCH_DDCSDA
VGA_PCH_DDCSCL
DACREFSET R355
1K-1-04
PCH_TP6
PCH_TP7
PCH_TP8
PCH_TP9
STP25
STP24
STP21
STP23
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPD_CTRLCLK
DDPD_CTRLDATA
SDVO_CTRLCLK
SDVO_CTRLDATA
DDPD_CTRL_CLK
DDPD_CTRL_DATA
R358
R359
R360
150-1-04
CLOSE TO EACH PIN.
SC29
SC28
SC27
2.7P-04-O
For EMI
+VCC3
+VGA_VCC
R88
2.2K-04
MN1
2N7002-S
R76
VGA_PCH_DDCSDA
3.3V Tolerant
VGA_DDCSDA_5V
5V Tolerant
R97
MN3
R75
VGA_PCH_DDCSCL
VGA_DDCSCL_5V
U13
VGA_VSYNC
74AHCT1G32GVS
R78
33-04
VGA_VSYNC_5V
R99
0-04-O
VV5R
C57
22p-04-O
rise time
U12
VGA_HSYNC
R77
VGA_HSYNC_5V
R98
VH5R
C58
DDPC_CTRLDATA
Port C Detected(Internal PD):
Port C is Detected when High,
Port C is not Detect when Low.
DDPD_CTRLDATA
Port D Detected(Internal PD):
Port D is Detected when High,
Port D is not Detect when Low.
SDVO_CTRLDATA
Port B Detected(Internal PD):
Port B is Detected when High,
Port B is not Detect when Low.


VGA Circuit
+12V
R118
10K-04
MN7_G
C113
.1U-04-O
For EMI
MN6
APM2306ACTRL-S
+VGA_VCC_1
F1
FUSE-1.1A-18
C40
.1U-04
C39
1U-O
reserve for EMI
R113
0-08-O
V1.0:to fix water ripple
16-101-470370 500mA
VGA_RED
VGA_GREEN
VGA_BLUE
FB19
FB20
FB21
FB47-06-B
VGA_RED_1
VGA_GREEN_1
VGA_BLUE_1
FB15
FB16
FB17
R101
150-1-04
R102
R103
C93
10P-04
C92
C91
C75
22P-04
C77
C76
C52
10P-04-O
C51
C61
VGA_RED_CONN
VGA_GREEN_CONN
VGA_BLUE_CONN
VGA
CONN-VGA-HRBL
10-007-015562
VGA_DDCSDA_5V
VGA_DDCSCL_5V
VGA_HSYNC_5V
VGA_VSYNC_5V
R67
R66
100-04
VGA_DDCSDA_CONN
VGA_DDCSCL_CONN
C43
100P-04-O
C42
C47
C46
U4
C36
1U-04-O
AZC099-04S-R7G-S
U5
C37
.1U-04-O
VGA_GREEN_CONN
VGA_BLUE_CONN
Elitegroup Computer Systems
PCH - DVI/HDMI/VGA
H61H2-CM
V1.0
Monday, December 20, 2010
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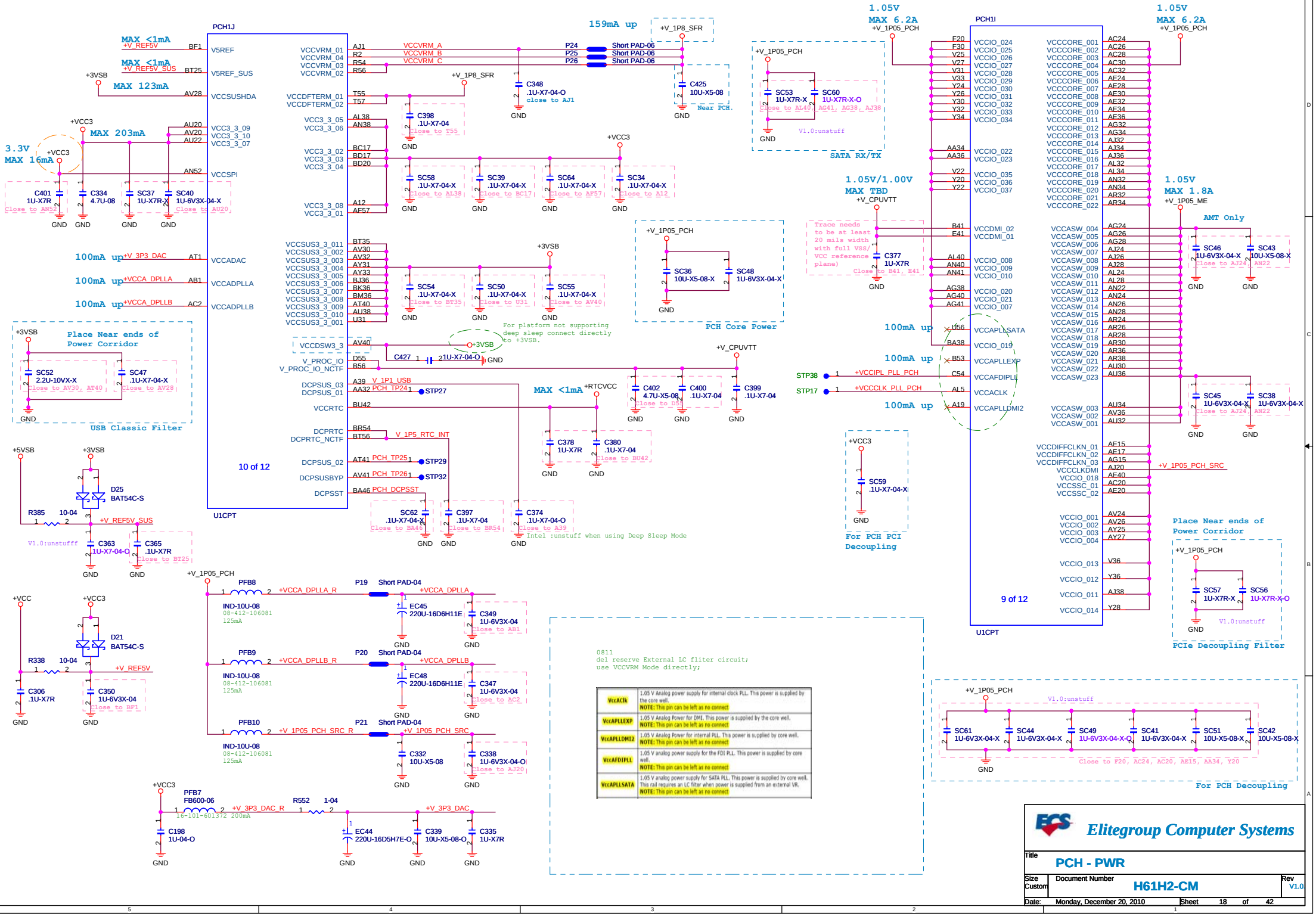
PCH1J
MAX <1mA
+V_REF5V
BF1
V5REF
MAX <1mA
+V_REF5V_SUS
BT25
V5REF_SUS
+3VSB
MAX 123mA
AV28
VCCSUSHDA
+VCC3
MAX 203mA
AU20
AV20
AU22
VCC3_3_09
VCC3_3_10
VCC3_3_07
3.3V
MAX 16mA
+VCC3
AN52
VCCSPI
C401
1U-X7R
Close to AN52
C334
4.7U-08
SC37
1U-X7R-X
SC40
1U-6V3X-04-X
Close to AU20
GND
100mA up
+V_3P3_DAC
AT1
VCCADAC
100mA up
+VCCA_DPLLA
AB1
VCCADPLLA
100mA up
+VCCA_DPLLB
AC2
VCCADPLLB
+3VSB
Place Near ends of
Power Corridor
SC52
2.2U-10VX-X
Close to AV30, AT40
SC47
.1U-X7-04-X
Close to AV28
USB Classic Filter
+5VSB
+3VSB
D25
BAT54C-S
R385
10-04
+V_REF5V_SUS
V1.0:unstuff
C363
.1U-X7-04-O
C365
.1U-X7R
Close to BT25
+VCC
+VCC3
D21
BAT54C-S
R338
10-04
+V_REF5V
C306
.1U-X7R
C350
1U-6V3X-04
Close to BF1
VCCVRM_01
VCCVRM_04
VCCVRM_03
VCCVRM_02
AJ1
R2
R54
R56
VCCVRM_A
VCCVRM_B
VCCVRM_C
159mA up
+V_1P8_SFR
P24
P25
P26
Short PAD-06
Short PAD-06
Short PAD-06
C348
.1U-X7-04-O
close to AJ1
C425
10U-X5-08
Near PCH.
GND
VCCDFTERM_01
VCCDFTERM_02
T55
T57
C398
.1U-X7-04
Close to T55
VCC3_3_05
VCC3_3_06
AL38
AN38
VCC3_3_02
VCC3_3_03
VCC3_3_04
BC17
BD17
BD20
SC58
.1U-X7-04-X
Close to AL38
SC39
.1U-X7-04-X
Close to BC17
SC64
.1U-X7-04-X
Close to AF57
SC34
.1U-X7-04-X
Close to A12
VCC3_3_08
VCC3_3_01
A12
AF57
VCCSUS3_3_011
VCCSUS3_3_002
VCCSUS3_3_003
VCCSUS3_3_004
VCCSUS3_3_005
VCCSUS3_3_006
VCCSUS3_3_007
VCCSUS3_3_008
VCCSUS3_3_009
VCCSUS3_3_010
VCCSUS3_3_001
BT35
AV30
AV32
AY31
AY33
BJ36
BK36
BM36
AT40
AU38
U31
SC54
.1U-X7-04-X
Close to BT35
SC50
.1U-X7-04-X
Close to U31
SC55
.1U-X7-04-X
Close to AV40
+3VSB
VCCDSW3_3
AV40
C427
.1U-X7-04-O
For platform not supporting
deep sleep connect directly
to +3VSB.
V_PROC_IO
V_PROC_IO_NCTF
D55
B56
DCPSUS_03
DCPSUS_01
VCCRTC
A39
AA32
BU42
V_1P1_USB
PCH_TP24
STP27
MAX <1mA
+RTCVCC
C378
1U-X7R
C380
.1U-X7-04
Close to BU42
DCPRTC
DCPRTC_NCTF
BR54
BT56
V_1P5_RTC_INT
AT41
AV41
PCH_TP25
PCH_TP26
STP29
STP32
DCPSUS_02
DCPSUSBYP
DCPSST
BA46
PCH_DCPSST
SC62
.1U-X7-04-X
Close to BA46
C397
.1U-X7-04
Close to BR54
C374
.1U-X7-04-O
Close to A39
Intel :unstuff when using Deep Sleep Mode
10 of 12
U1CPT
+V_1P05_PCH
SC36
10U-X5-08-X
SC48
1U-6V3X-04-X
PCH Core Power
+V_CPUVTT
C402
4.7U-X5-08
Close to D55
C400
.1U-X7-04
C399
.1U-X7-04
STP38
STP17
+VCCIPL_PLL_PCH
+VCCCLK_PLL_PCH
100mA up
100mA up
100mA up
U56
BA38
B53
C54
AL5
A19
VCCAPLLSATA
VCCIO_019
VCCAPLLEXP
VCCAFDIPLL
VCCACLK
VCCAPLLDMI2
+VCC3
SC59
.1U-X7-04-X
For PCH PCI
Decoupling
PFB8
IND-10U-08
08-412-106081
125mA
+VCCA_DPLLA_R
P19
Short PAD-04
+VCCA_DPLLA
EC45
220U-16D6H11E
C349
1U-6V3X-04
Close to AB1
PFB9
IND-10U-08
08-412-106081
125mA
+VCCA_DPLLB_R
P20
Short PAD-04
+VCCA_DPLLB
EC48
220U-16D6H11E
C347
1U-6V3X-04
Close to AC2
PFB10
IND-10U-08
08-412-106081
125mA
+V_1P05_PCH_SRC_R
P21
Short PAD-04
+V_1P05_PCH_SRC
C332
10U-X5-08
C338
1U-6V3X-04-O
Close to AJ20
PFB7
FB600-06
16-101-601372 200mA
+V_3P3_DAC_R
R552
1-04
+V_3P3_DAC
C198
1U-04-O
EC44
220U-16D5H7E-O
C339
10U-X5-08-O
C335
1U-X7R
0811
del reserve External LC fliter circuit;
use VCCVRM Mode directly;
VccAClk
1.05 V Analog power supply for internal clock PLL. This power is supplied by the core well.
NOTE: This pin can be left as no connect
VccAPLLEXP
1.05 V Analog Power for DMI. This power is supplied by the core well.
NOTE: This pin can be left as no connect
VccAPLLDMI2
1.05 V Analog Power for internal PLL. This power is supplied by core well.
NOTE: This pin can be left as no connect
VccAFDIPLL
1.05 V analog power supply for the FDI PLL. This power is supplied by core well.
NOTE: This pin can be left as no connect
VccAPLLSATA
1.05 V analog power supply for SATA PLL. This power is supplied by core well. This rail requires an LC filter when power is supplied from an external VR.
NOTE: This pin can be left as no connect
1.05V
MAX 6.2A
+V_1P05_PCH
SATA RX/TX
SC53
1U-X7R-X
SC60
1U-X7R-X-O
Close to AL40, AG41, AG38, AJ38
V1.0:unstuff
1.05V/1.00V
MAX TBD
+V_CPUVTT
Trace needs
to be at least
20 mils width
with full VSS/
VCC reference
plane)
C377
1U-X7R
Close to B41, E41
PCH1I
F20
F30
V25
V27
V31
V33
Y24
Y26
Y30
Y32
Y34
VCCIO_024
VCCIO_025
VCCIO_026
VCCIO_027
VCCIO_028
VCCIO_029
VCCIO_030
VCCIO_031
VCCIO_032
VCCIO_033
VCCIO_034
AA34
AA36
VCCIO_022
VCCIO_023
V22
Y20
Y22
VCCIO_035
VCCIO_036
VCCIO_037
B41
E41
VCCDMI_02
VCCDMI_01
AL40
AN40
AN41
VCCIO_008
VCCIO_009
VCCIO_010
AG38
AG40
AG41
VCCIO_020
VCCIO_021
VCCIO_007
9 of 12
U1CPT
VCCCORE_001
VCCCORE_002
VCCCORE_003
VCCCORE_004
VCCCORE_005
VCCCORE_006
VCCCORE_007
VCCCORE_008
VCCCORE_009
VCCCORE_010
VCCCORE_011
VCCCORE_012
VCCCORE_013
VCCCORE_014
VCCCORE_015
VCCCORE_016
VCCCORE_017
VCCCORE_018
VCCCORE_019
VCCCORE_020
VCCCORE_021
VCCCORE_022
AC24
AC26
AC28
AC30
AC32
AE24
AE28
AE30
AE32
AE34
AE36
AG32
AG34
AJ32
AJ34
AJ36
AL32
AL34
AN32
AN34
AR32
AR34
1.05V
MAX 6.2A
+V_1P05_PCH
1.05V
MAX 1.8A
+V_1P05_ME
AMT Only
SC46
1U-6V3X-04-X
Close to AJ24, AN22
SC43
10U-X5-08-X
VCCASW_004
VCCASW_005
VCCASW_006
VCCASW_007
VCCASW_008
VCCASW_009
VCCASW_010
VCCASW_011
VCCASW_012
VCCASW_013
VCCASW_014
VCCASW_015
VCCASW_016
VCCASW_017
VCCASW_018
VCCASW_019
VCCASW_020
VCCASW_021
VCCASW_022
VCCASW_023
AG24
AG26
AG28
AJ24
AJ26
AJ28
AL24
AL28
AN22
AN24
AN26
AN28
AR24
AR26
AR28
AR30
AR36
AR38
AU30
AU36
SC45
1U-6V3X-04-X
Close to AJ24, AN22
SC38
1U-6V3X-04-X
VCCASW_003
VCCASW_002
VCCASW_001
AU34
AV36
AU32
VCCDIFFCLKN_01
VCCDIFFCLKN_02
VCCDIFFCLKN_03
VCCCLKDMI
VCCIO_018
VCCSSC_01
VCCSSC_02
AE15
AE17
AG15
AJ20
AE40
AC20
AE20
+V_1P05_PCH_SRC
VCCIO_001
VCCIO_002
VCCIO_003
VCCIO_004
AV24
AV26
AY25
AY27
VCCIO_013
VCCIO_012
VCCIO_011
VCCIO_014
V36
Y36
AJ38
Y28
Place Near ends of
Power Corridor
+V_1P05_PCH
SC57
1U-X7R-X
SC56
1U-X7R-X-O
V1.0:unstuff
PCIe Decoupling Filter
+V_1P05_PCH
V1.0:unstuff
SC61
1U-6V3X-04-X
SC44
1U-6V3X-04-X
SC49
1U-6V3X-04-X-O
SC41
1U-6V3X-04-X
SC51
10U-X5-08-X
SC42
10U-X5-08-X
Close to F20, AC24, AC20, AE15, AA34, Y20
For PCH Decoupling
Elitegroup Computer Systems
Title
PCH - PWR
Size
Custom
Document Number
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Rev
V1.0
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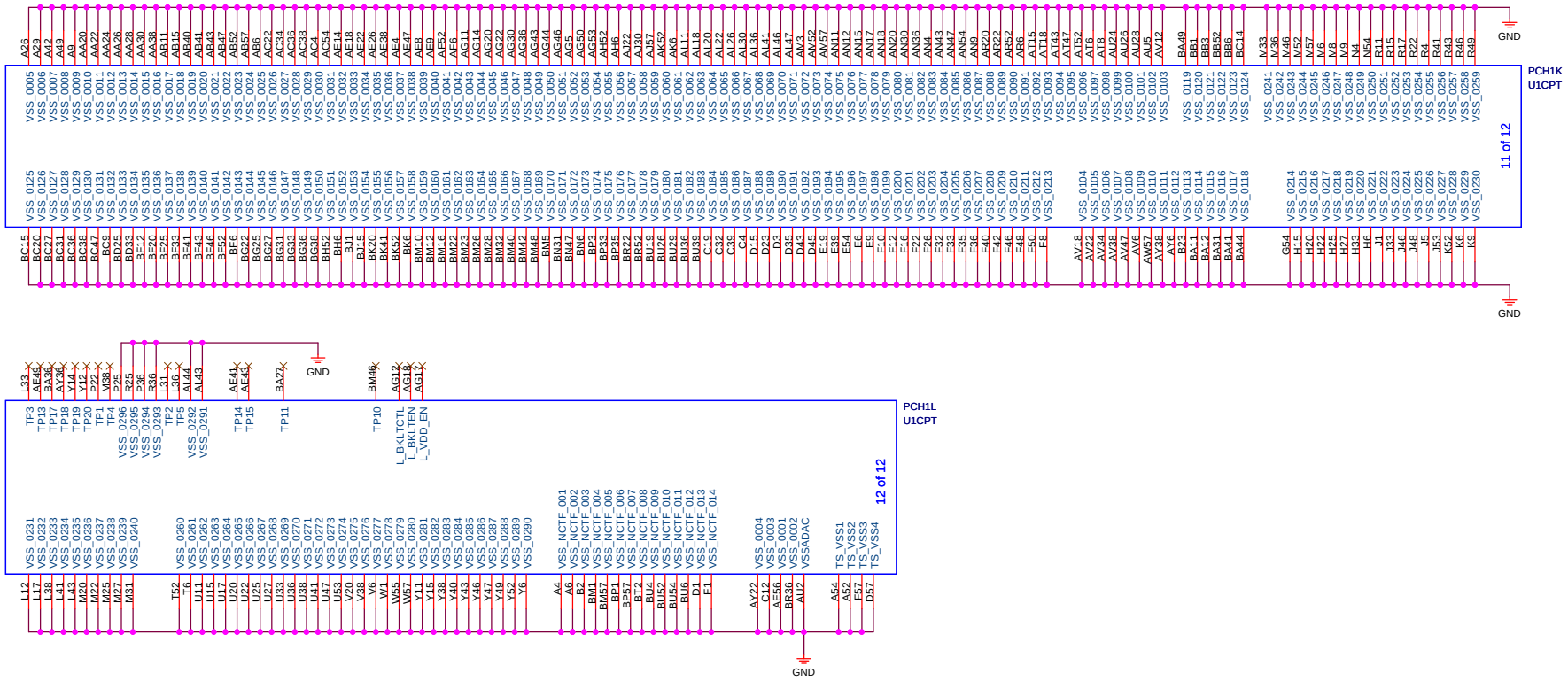
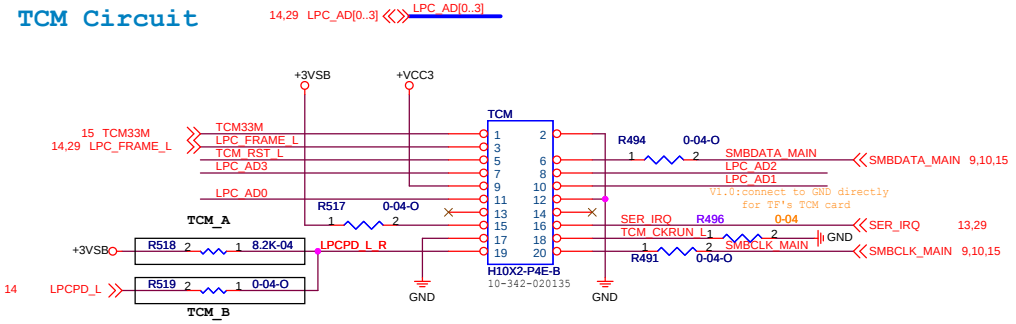


TCM Circuit

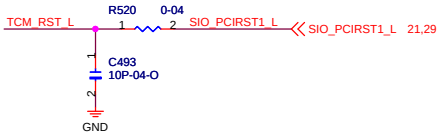


BOM Difference

	TongFang TCM	normal TCM
TCM_A	v	x
TCM_B	x	v

* V:stuff X:NC

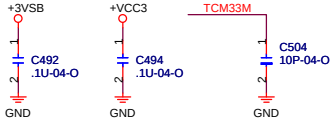
TF note: keep pin 13,14,6,15,20 no connect



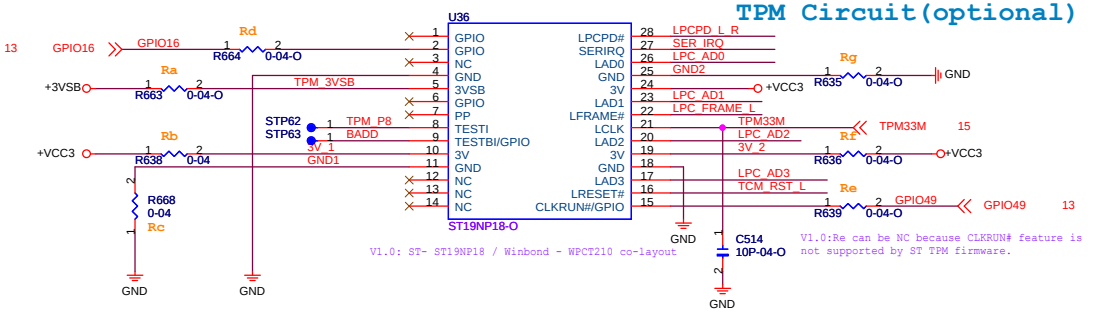
BOM Difference

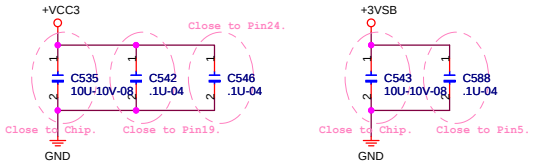
	china one	other customer
R496	0 OHM	check TCM Card spec

*



TPM Circuit(optional)





*

02-440-918264:
IC TPM.ST19NP18ER28PVLR..TSSOP 28P.3.3V.....LEAD-FREE(RoHS).ST

02-440-210900:
IC TPM.WPCT210CA0WX..TSSOP 28P.....HF.LEAD-FREE.NUVOTON

	Ra	Rb	Rc	Rd	Re	Rf	Rg
ST	X	V	V	X	X	X	X
Winbond	V	X	X	X	X	V	V

Elitegroup Computer Systems

Title: PCH - GND,TCM Header

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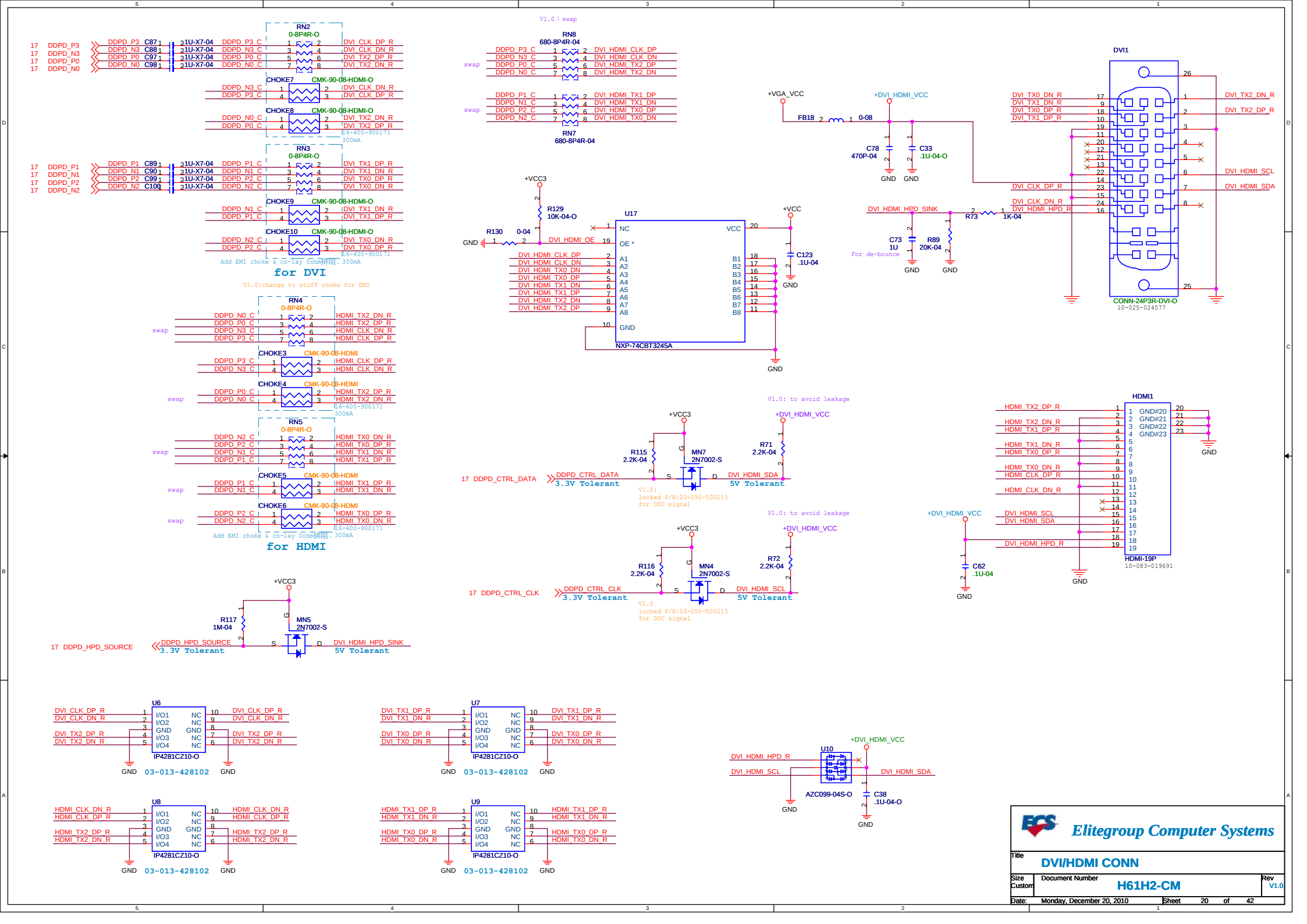
RN2
0-8P4R-O
CHOKE7 CMK-90-08-HDMI-O
CHOKE8 CMK-90-08-HDMI-O
RN3
0-8P4R-O
CHOKE9 CMK-90-08-HDMI-O
CHOKE10 CMK-90-08-HDMI-O
for DVI
V1.0:change to stuff choke for EMI
RN4
0-8P4R-O
CHOKE3 CMK-90-08-HDMI
CHOKE4 CMK-90-08-HDMI
RN5
0-8P4R-O
CHOKE5 CMK-90-08-HDMI
CHOKE6 CMK-90-08-HDMI
for HDMI
V1.0 : swap
RN8
680-8P4R-04
RN7
680-8P4R-04
DVI1
CONN-24P3R-DVI-O
HDMI1
HDMI-19P
U17
NXP-74CBT3245A
U6
U7
U8
U9
U10
IP4281CZ10-O
AZC099-04S-O
03-013-428102
V1.0: to avoid leakage
locked P/N:03-050-500213
for DDC signal

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DVI/HDMI CONN
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PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A

PCI-E X16

PCIE16X

PCIEX16-BK

CRB V0.7
Change to .22U-X7-04

PCI-E X16 Decoupling Cap.

PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A

PCI-E X1 A

PCIE1X_1

PCIEX1-BK

PCI-E X1 A Decoupling Cap.

Between PEX16 & PEX1A

Between PEX1A& PCI

Title	PCIE*16,PCIE*1 Slot
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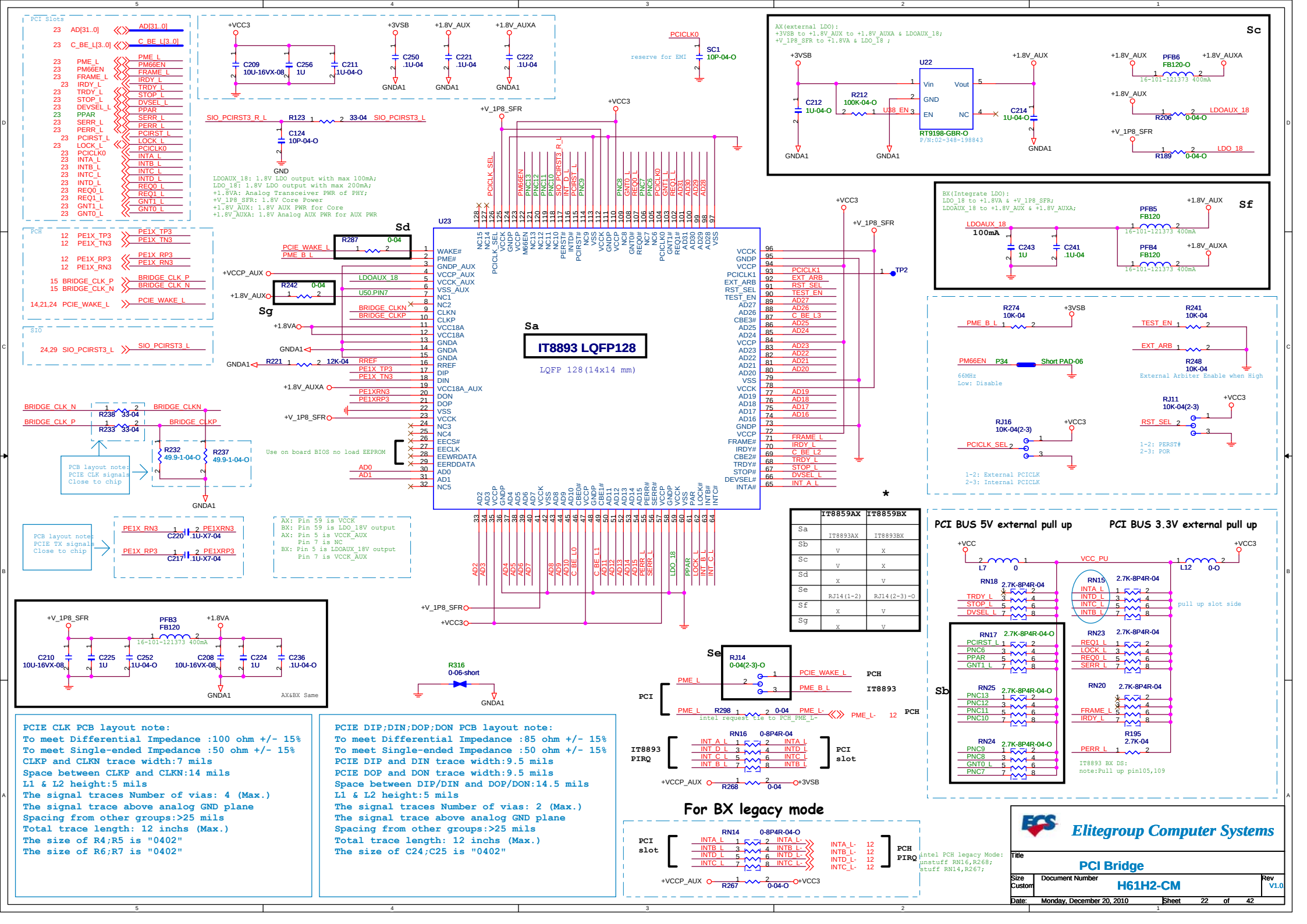
PCI Slots
AD[31..0]
C_BE_L[3..0]
PME_L
PM66EN
FRAME_L
IRDY_L
TRDY_L
STOP_L
DVSEL_L
PPAR
SERR_L
PERR_L
PCIRST_L
LOCK_L
PCICLK0
INTA_L
INTB_L
INTC_L
INTD_L
REQ0_L
REQ1_L
GNT1_L
GNT0_L
PCH
PE1X_TP3
PE1X_TN3
PE1X_RP3
PE1X_RN3
BRIDGE_CLK_P
BRIDGE_CLK_N
PCIE_WAKE_L
SIO
SIO_PCIRST3_L
+VCC3
+3VSB
+1.8V_AUX
+1.8V_AUXA
C209 10U-16VX-08
C256 1U
C211 .1U-04-O
C250 .1U-04
C221 .1U-04
C222 .1U-04
GNDA1
PCICLK0
reserve for EMI
SC1 10P-04-O
SIO_PCIRST3_R_L
R123 33-04
SIO_PCIRST3_L
C124 10P-04-O
GND
LDOAUX_18: 1.8V LDO output with max 100mA;
LDO_18: 1.8V LDO output with max 200mA;
+1.8VA: Analog Transceiver PWR of PHY;
+V_1P8_SFR: 1.8V Core Power
+1.8V_AUX: 1.8V AUX PWR for Core
+1.8V_AUXA: 1.8V Analog AUX PWR for AUX PWR
Sd
U23
PCIE_WAKE_L
PME_B_L
R287 0-04
+VCCP_AUX
+1.8V_AUX
R242 0-04
LDOAUX_18
U50.PIN7
Sg
+1.8VA
GNDA1
R221 12K-04
RREF
BRIDGE_CLKN
BRIDGE_CLKP
PE1X_TP3
PE1X_TN3
+1.8V_AUXA
PE1XRN3
PE1XRP3
+V_1P8_SFR
Use on board BIOS no load EEPROM
AD0
AD1
Sa
IT8893 LQFP128
LQFP 128(14x14 mm)
WAKE#
PME#
GNDP_AUX
VCCP_AUX
VCCK_AUX
VSS_AUX
NC1
NC2
CLKN
CLKP
VCC18A
VCC18A
GNDA
GNDA
GNDA
RREF
DIP
DIN
VCC18A_AUX
DON
DOP
VSS
VCCK
NC3
NC4
EECS#
EECLK
EEWRDATA
EERDDATA
AD0
AD1
NC5
VCCK
GNDP
VCCP
PCICLK1
EXT_ARB
RST_SEL
TEST_EN
AD27
AD26
CBE3#
AD25
AD24
VCCP
AD23
AD22
AD21
AD20
VSS
VCCK
AD19
AD18
AD17
AD16
GNDP
VCCP
FRAME#
IRDY#
CBE2#
TRDY#
STOP#
DEVSEL#
INTA#
TP2
BRIDGE_CLK_N
BRIDGE_CLK_P
R238 33-04
R233 33-04
BRIDGE_CLKN
BRIDGE_CLKP
R232 49.9-1-04-O
R237 49.9-1-04-O
PCB layout note:
PCIE CLK signals
Close to chip
GNDA1
PCB layout note:
PCIE TX signals
Close to chip
PE1X_RN3
C220 .1U-X7-04
PE1XRN3
PE1X_RP3
C217 .1U-X7-04
PE1XRP3
AX: Pin 59 is VCCK
BX: Pin 59 is LDO_18V output
AX: Pin 5 is VCCK_AUX
Pin 7 is NC
BX: Pin 5 is LDOAUX_18V output
Pin 7 is VCCK_AUX
+V_1P8_SFR
PFB3 FB120
16-101-121373 400mA
+1.8VA
C210 10U-16VX-08
C225 1U
C252 .1U-04-O
C208 10U-16VX-08
C224 1U
C236 .1U-04-O
GNDA1
AX&BX Same
R316 0-06-short
GNDA1
Se
RJ14 0-04(2-3)-O
PCIE_WAKE_L
PME_L
PME_B_L
PCH
IT8893
PCI
PME_L
R298 0-04
PME_L-
intel request tie to PCH_PME_L-
PME_L-
12
PCH
RN16 0-8P4R-04
IT8893 PIRQ
INT_A_L
INT_D_L
INT_C_L
INT_B_L
INTA_L
INTD_L
INTC_L
INTB_L
PCI slot
+VCCP_AUX
R268 0-04
+3VSB
For BX legacy mode
RN14 0-8P4R-04-O
PCI slot
INTA_L
INTB_L
INTD_L
INTC_L
INTA_L- 12
INTB_L- 12
INTD_L- 12
INTC_L- 12
PCH PIRQ
+VCCP_AUX
R267 0-04-O
+VCC3
intel PCH legacy Mode:
unstuff RN16,R268;
stuff RN14,R267;
PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"
PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inchs (Max.)
The size of C24;C25 is "0402"
IT8859AX IT8859BX
Sa IT8893AX IT8893BX
Sb V X
Sc V X
Sd X V
Se RJ14(1-2) RJ14(2-3)-O
Sf X V
Sg X V
Sc
AX(external LDO):
+3VSB to +1.8V_AUX to +1.8V_AUXA & LDOAUX_18;
+V_1P8_SFR to +1.8VA & LDO_18 ;
U22
Vin
Vout
GND
EN
NC
U38_EN
C212 1U-04-O
R212 100K-04-O
C214 1U-04-O
RT9198-GBR-O
P/N:02-348-198843
PFB6 FB120-O
16-101-121373 400mA
R206 0-04-O
LDOAUX_18
R189 0-04-O
LDO_18
Sf
BX(Integrate LDO):
LDO_18 to +1.8VA & +V_1P8_SFR;
LDOAUX_18 to +1.8V_AUX & +1.8V_AUXA;
LDOAUX_18
100mA
C243 1U
C241 .1U-04
PFB5 FB120
PFB4 FB120
16-101-121373 400mA
R274 10K-04
PME_B_L
PM66EN
P34
Short PAD-06
66MHz
Low: Disable
R241 10K-04
TEST_EN
EXT_ARB
R248 10K-04
External Arbiter Enable when High
RJ11 10K-04(2-3)
RST_SEL
1-2: PERST#
2-3: POR
RJ16 10K-04(2-3)
PCICLK_SEL
1-2: External PCICLK
2-3: Internal PCICLK
PCI BUS 5V external pull up
PCI BUS 3.3V external pull up
L7 0
VCC_PU
L12 0-O
RN18 2.7K-8P4R-04
TRDY_L
STOP_L
DVSEL_L
RN15 2.7K-8P4R-04
INTA_L
INTD_L
INTC_L
INTB_L
pull up slot side
Sb
RN17 2.7K-8P4R-04-O
PCIRST_L
PNC6
PPAR
GNT1_L
RN23 2.7K-8P4R-04
REQ1_L
LOCK_L
REQ0_L
SERR_L
RN25 2.7K-8P4R-04-O
PNC13
PNC12
PNC11
PNC10
RN20 2.7K-8P4R-04
FRAME_L
IRDY_L
RN24 2.7K-8P4R-04-O
PNC9
PNC8
GNT0_L
PNC7
R195 2.7K-04
PERR_L
IT8893 BX DS:
note:Pull up pin105,109
Elitegroup Computer Systems
Title
PCI Bridge
Size Custom
Document Number H61H2-CM
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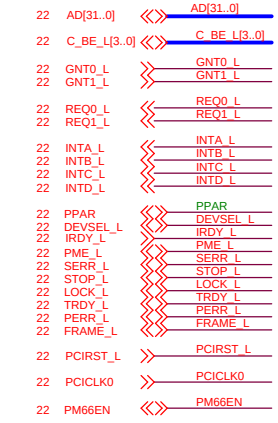
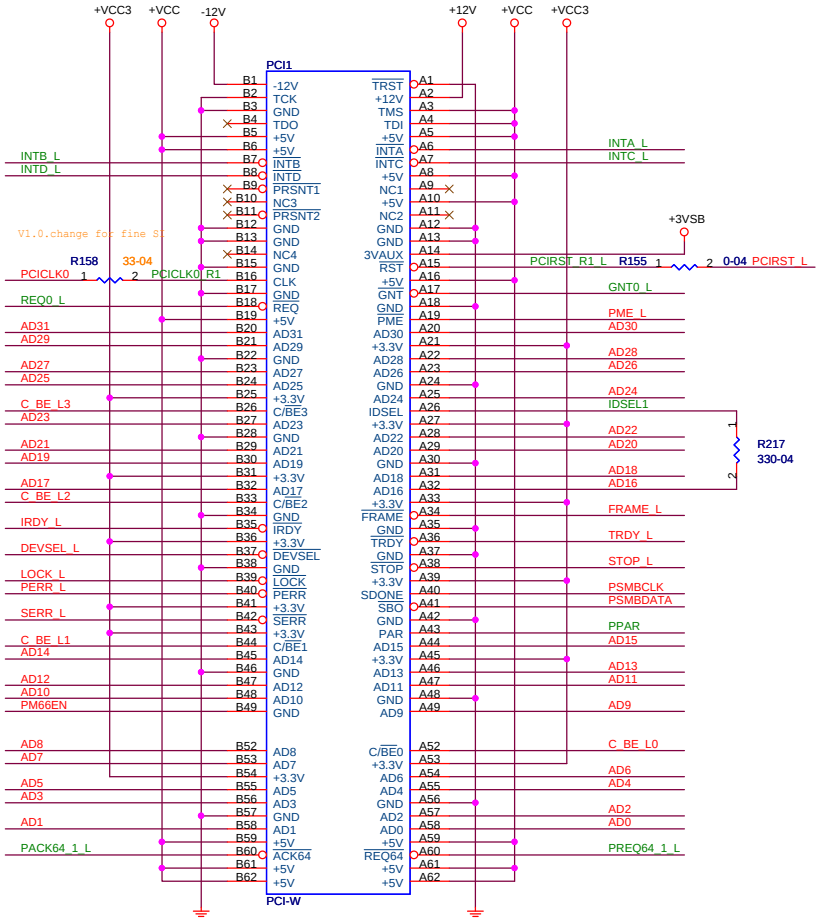
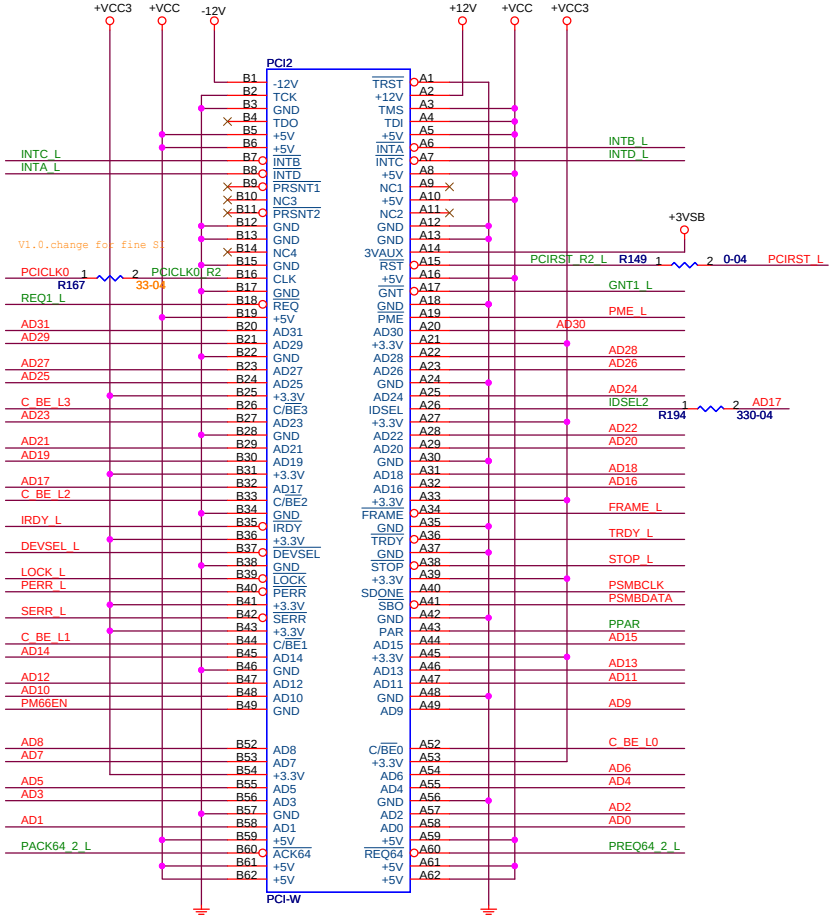
PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A

PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A



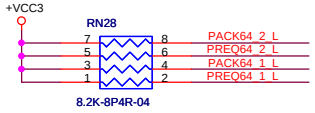


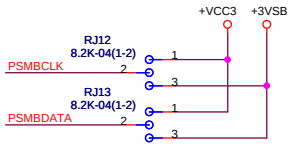


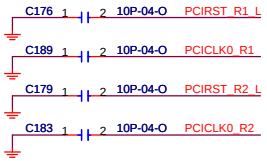
IDSEL=AD16
INT[A,B,C,D]
Legacy mode from PCH
INT[A,B,C,D]

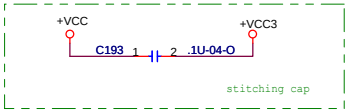
IDSEL=AD17
INT[B,C,D,A]
Legacy mode from PCH
INT[B,C,D,A]

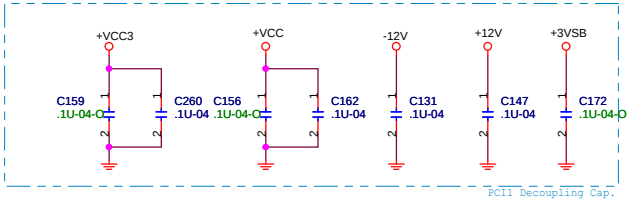
external pull up resistor is 2.7K if use 5V

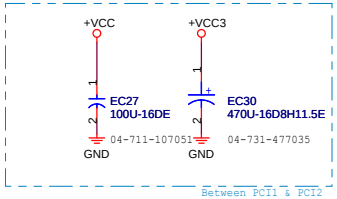


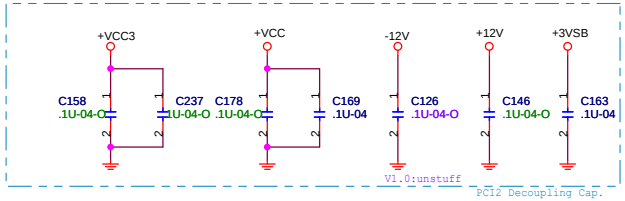












Elitegroup Computer Systems

Title: PCI Slot

Size	Document Number	Rev
Custom	H61H2-CM	V1.0

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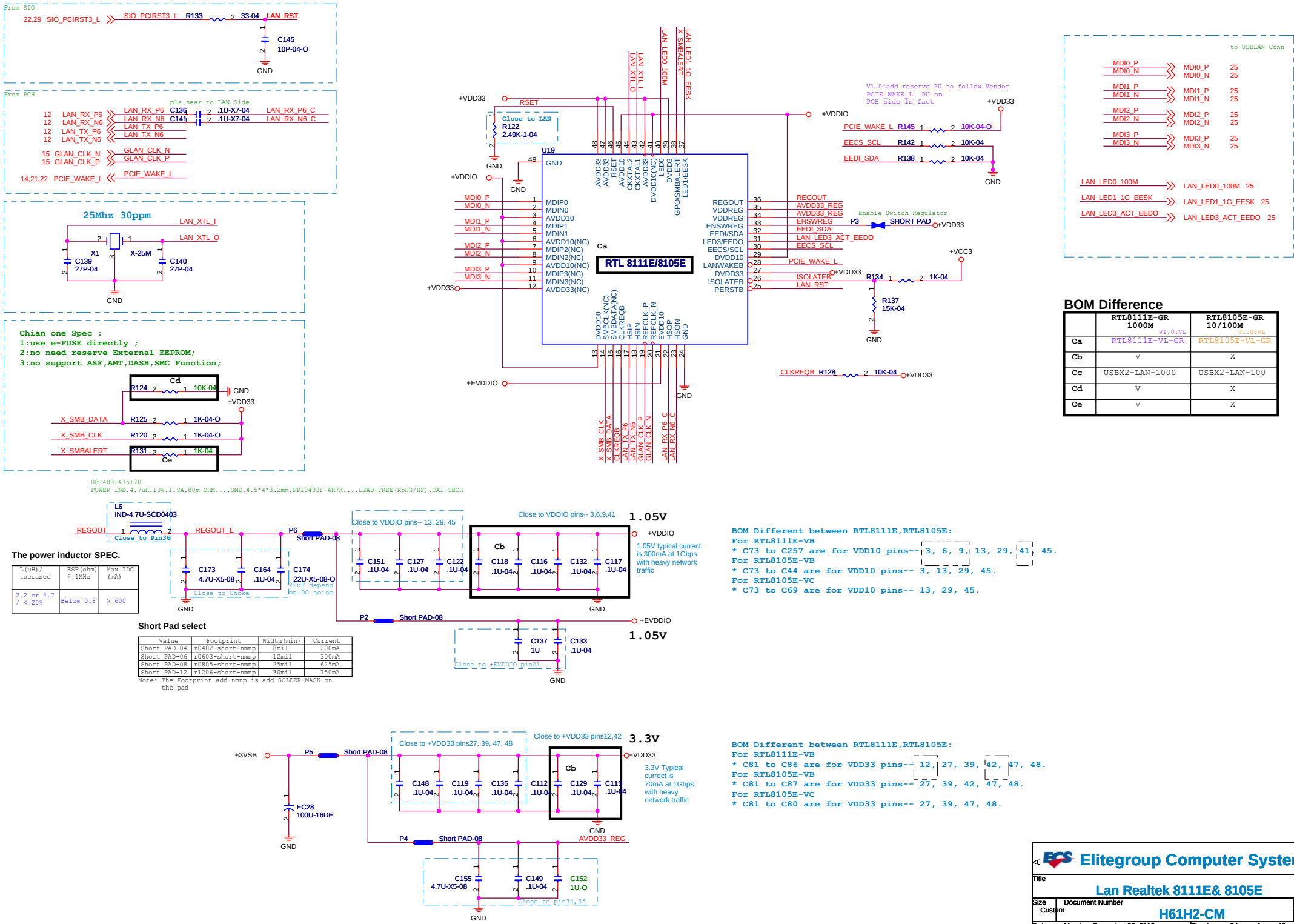

BOM Difference

	RTL8111E-GR 1000M V1.0:VL	RTL8105E-GR 10/100M V1.0:VL
Ca	RTL8111E-VL-GR	RTL8105E-VL-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	V	X
Ce	V	X

The power inductor SPEC.

L(uH) / toerance	ESR(ohm) @ 1MHz	Max IDC (mA)
2.2 or 4.7 / <=20%	Below 0.8	> 600

Short Pad select

Value	Footprint	Width(min)	Current
Short PAD-04	r0402-short-nmnp	8mil	200mA
Short PAD-06	r0603-short-nmnp	12mil	300mA
Short PAD-08	r0805-short-nmnp	25mil	625mA
Short PAD-12	r1206-short-nmnp	30mil	750mA

Note: The Footprint add nmnp is add SOLDER-MASK on the pad

BOM Different between RTL8111E,RTL8105E:
For RTL8111E-VB
* C73 to C257 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.
For RTL8105E-VB
* C73 to C44 are for VDD10 pins-- 3, 13, 29, 45.
For RTL8105E-VC
* C73 to C69 are for VDD10 pins-- 13, 29, 45.

BOM Different between RTL8111E,RTL8105E:
For RTL8111E-VB
* C81 to C86 are for VDD33 pins-- 12, 27, 39, 42, 47, 48.
For RTL8105E-VB
* C81 to C87 are for VDD33 pins-- 27, 39, 42, 47, 48.
For RTL8105E-VC
* C81 to C80 are for VDD33 pins-- 27, 39, 47, 48.

Elitegroup Computer Systems

Title: Lan Realtek 8111E& 8105E

Size: Custom | Document Number: H61H2-CM | Rev: V1.0.

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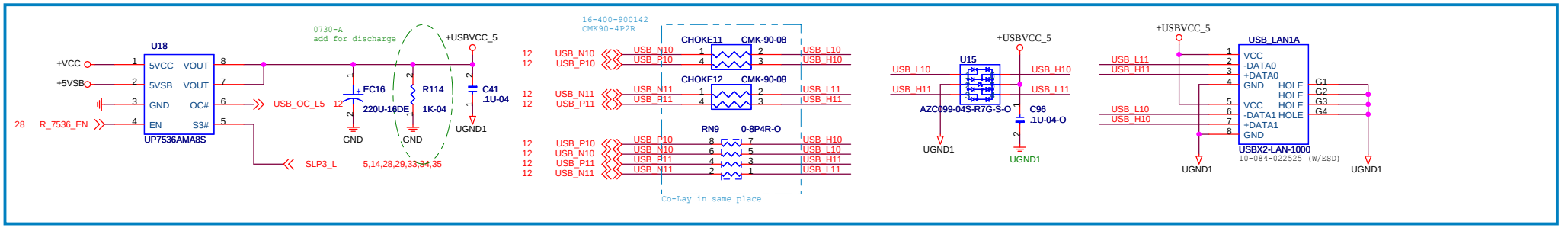
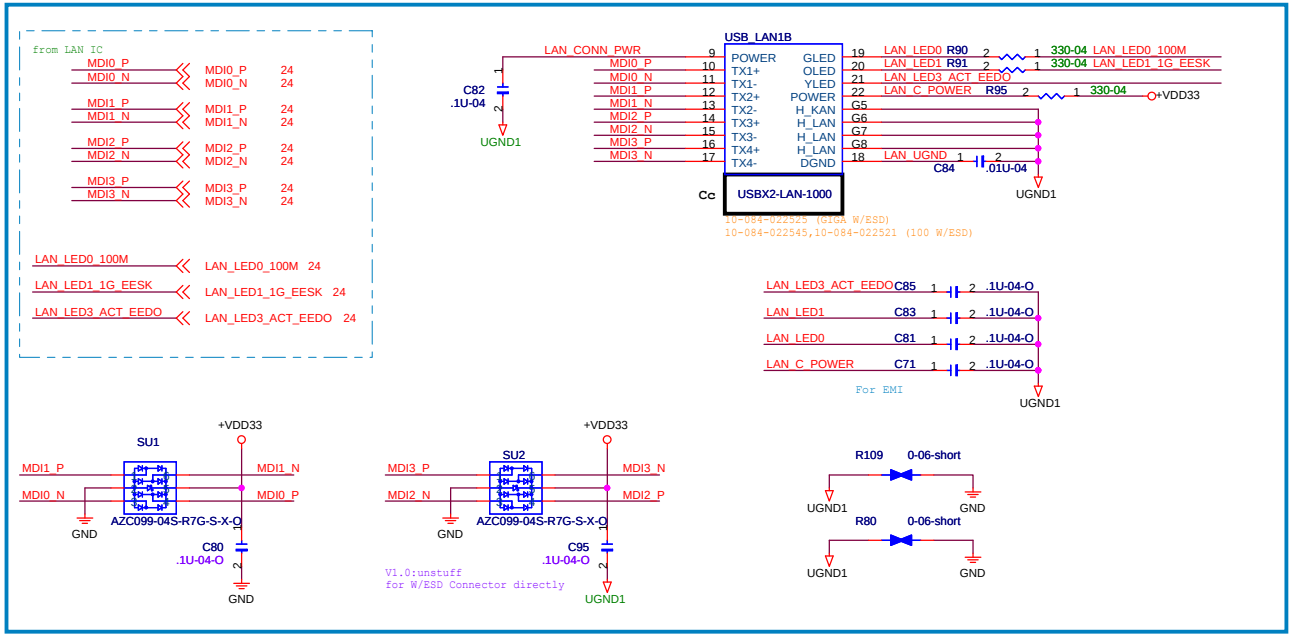
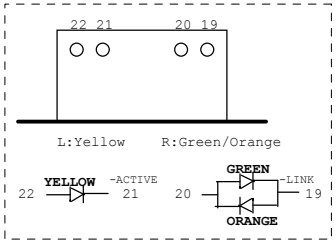




REAR SIDE 2 PORTS ON LANUSB CONN.



For China-one LED Light:

	Status	Yellow	Grn/Org
	No Link	Off	Off
	S3/S4/S5	Off	Off
	10M, inactive	Off	Off
	10M, active		Off
	100M, inactive	Off	
	100M, active		
	1G, inactive	Off	
	1G, active		
	Blinking		

REAR SIDE 2 PORTS ON LANUSB CONN.

RTL8111E-VB-GR_Datasheet_1.3

Table 12. Customized LEDs

	LINK			ACT/Full
Speed	Link 10M	Link 100M	Link 1000M	-
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
Not Defined	Bit 8	Bit 9	Bit 10	Bit 11
LED 3	Bit 12	Bit 13	Bit 14	Bit 15

LED Pin	ACT=0	ACT=1
LINK=0	Floating	All Speed ACT
LINK>0	Selected Speed LINK	Selected Speed LINK+ACT

Note1: ACT means blinking TX and RX. LINK indicates Link 10M/100M/1000M.
Note2: There are four special modes:

Mode A: LED OFF Mode → Set all bits to 0

Mode B: Full Duplex LED Mode → Set LED 0=0, and either LED 1 or LED 3 >0
LED 0 = Full Duplex
LED 1 = Follow Customized LED rule
LED 3= Follow Customized LED rule

Mode C: Separated TX/RX Mode → Set LED 0=0, LED1 = 0, LED3 = 1
LED 0 = TX
LED 1 = RX
LED 3= LINK

Mode D: Separated Speed ACT Mode → Set LED 0=0, LED1 =1 , LED3 = 1
LED 0 = 10ACT
LED 1 = 100ACT
LED 3= 1000ACT

RTL8111E-VB-GR_Datasheet_1.3

Table 7. LEDs

Symbol	Type	Pin No	Description
LED0	O	40	
LED1	O	37	
LED3	O	31	

LEDS1-0	00	01	10	11
LED0	ACT_{ALL}	$Link_{ALL}$/ ACT_{ALL}	Link10/ ACT_{ALL}	LINK10/ ACT_{10}
LED1	LINK100	LINK100	LINK100	LINK100/ ACT_{100}
LED3	LINK1000	LINK1000	LINK1000	LINK1000 /ACT_{1000}

Note 1: During power down mode, the LED signals are logic high.
Note 2: LEDS1-0's initial value comes from the EEPROM. If there is no EEPROM, the default value of the (LEDS1, LEDS0)=(1, 1).

Customized LEDs

	RTL8111E(1G) LED TABLE
LEDS1~0	N/A (Coutomization)
LED0	LINK100
LED1	LINK1000
LED3	LINK(all) /ACT(all)

★ Active Low

Elitegroup Computer Systems

Title: USBLAN Connector

Size: Custom | Document Number: H61H2-CM | Rev: V1.0

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14 HDA_RST_L → HDA_RST_L
14 HDA_BITCLK → HDA_BITCLK
14 HDA_SYNC → HDA_SYNC
14 HDA_SDIN0 → HDA_SDIN0
14 HDA_SDOUT → HDA_SDOUT
27 FP_AUD_DETECT → FP_AUD_DETECT

Verfout bias for stereo microphone.

RJ2 4.7K-04(2-3)-O — PER_C — PORT-E_R
D1 BAT54A-S-O — LINE2_VREFO — PEVR / PEVL
RJ1 4.7K-04(2-3)-O — PEL_C — PORT-E_L
Richtek: stuff for F_Re_tasking Function

RJ4 4.7K-04(2-3) — PFR_C — PORT-F_R
D2 BAT54A-S — MIC2_VREFO — PFVR / PFVL
RJ3 4.7K-04(2-3) — PFL_C — PORT-F_L
Ct

Placement near to codec

use 75 ohm for ESD,retasking 75,only output 75,only input 1K.

Cx: C16 10U-X5-08-O, EC4 100U-16D6.3H5E, PDR_C, R8 75-04, PORT-D_R; C17 10U-X5-08-O, EC3 100U-16D6.3H5E, PDL_C, R9 75-04, PORT-D_L

MC1 10U-16VX-08-O, C26 .1U-04-O (reserve cap for VIA) — AUGND

MIC1_VREFO_R, LINE2_VREFO, MIC2_VREFO, MIC1_VREFO_L

+LDOVDD; C22 10U-X5-08, C19 .1U-04-O (near chip) X5R; +5VA; C23 10U-X5-08

Cs: CLOSE TO CODEC — AUGND — R68 20K-1-04 — AUDVREFP40; C63 100P-04-O (reserve cap for VIA)

AUDIO1 pins: PDR, PDL, NETB, VCAP, VREF_FILT, AVSS1, AVDD1, SENSE B, FOUT_R/PORT-D_R, FOUT_L/PORT-D_L, DCVOL/VrefOut-G, MIC1_VREFO_R/VrefOut-D, LINE2_VREFO/VrefOut-E, MIC2_VREFO/VrefOut-F, LINE1_VREFO/VrefOut-C_L, MIC1_VREFO_L/VrefOut-B_L

Ca: PORT-A_L, PORT-A_R, PORT-G_L, PORT-G_R, PORT-H_L, PORT-H_R — R25/R23/R47/R50/R49/R48 75-04-O — PAL_C, PAR_C, PGL_C, PGR_C, PHL_C, PHR_C — 10U-25D4H5E-O — EC10 PAL, EC9 PAR, EC14 PGL, EC13 PGR, EC8 PHL, EC7 PHR

AUGND; C34 .1U-04; +5VA; AUDVREFP40

SPO → SPO

Cd: ALC662-VC-GRS, 02-301-662691

VrefOut-A, AVDD2, PORT-A_L/SURR_L, VrefOut-H, PORT-A_R/SURR_R, AVSS3, PORT-G_L/CEN_OUT, PORT-G_R/LEF_OUT, PORT-H_L/SIDESURR_L, PORT-H_R/SIDESURR_R, S/PDIF IN / EAPD, S/PDIF-OUT

LINE1_R/PORT-C_R, LINE1_L/PORT-C_L, MIC1_R/PORT-B_R, MIC1_L/PORT-B_L, CD-R, CD-G, CD-L, MIC2_R/PORT-F_R, MIC2_L/PORT-F_L, LINE2_R/PORT-E_R, LINE2_L/PORT-E_L, SENSE A

Ci: EC5/EC6/EC1/EC2 10U-25D4H5E, C10/C11/C1/C2 4.7U-X5-08-O — PCR, PCL, PBR, PBL — Ce: R12/R13/R1/R2 75-04 — PORT-C_R, PORT-C_L, PORT-B_R, PORT-B_L

Cq: C20/C21 4.7U-X5-08 — PFR_C, PFL_C — R19/R20 1K-04 — PORT-F_R, PORT-F_L
Richtek: 100U+75ohm for Re_tasking Function; 4.7U+1K for no Re_tasking Function
VIA: 220U+16ohm for Re_tasking Function; 100U+16ohm for no Re_tasking Function

Cr: EC12 PER_C, EC15 PEL_C — 100U-25VD6H11E — R65/R74 75-04 — PORT-E_R, PORT-E_L
VIA: 220U+16ohm for Re_tasking Function; 100U+16ohm for no Re_tasking Function

NETA

GPIO(front panel detection) select table

	ALC892	ALC888S-VC	ALC662-VC
PIN-2	GPIO0/SPDIF-OUT2	SPDIF-OUT2	GPIO0
PIN-3	REGREF	GPIO0	GPIO1
PIN-4	GPIO1	GPIO1	DVSS

+VCC3; 38 / 23 mA; R302 0-04; AUD_VCC

DVDD_CORE, XI / DVSS, XO / DVDD_IO, DVSS, SDO, BCLK, DVSS, SDI, DVDD_CORE, SYNC, RESET#, PC_BEEP

PCBEEP → TP1

HDA_RST_L_RC — R108 0-04 — HDA_RST_L
HDA_SYNC
HDA_SDIN0_R — R107 33-04 — HDA_SDIN0
HDA_BITCLK
HDA_SDOUT

+12V; C171 .1U-04; GND

Ck: ONLY for ALC892 — 03-012-712517 — D14 AZ5125-01H-O — P, N, GND — 16-101-121373 400mA — PFB2, FB120-O

Cl: ONLY for ALC662 — R112 0-04, R105 0-04

FP_AUD_DETECT

Cm: R106 0-04-O — C108 10U-X5-08-O (ONLY for ALC892)

C104 22U-X5-08; C109 .1U-04; C110 22P-04-O; C111 .1U-04-O

+PS_5VSB

Cj: D15 BAT54C-S — 5VA_1
02-343-805180
IC REG.L78L05ACZ-AP..TO-92.5V..LEAD-FREE.ST
Pd = 0.27 W
+12V — R146 0 — R_AUDIO_VIN — U20 APL78L05-ECS (VIN, VOUT, GND) — 5VA_OUT
MN8 APM2306ACTRL-S
EC25 100U-16DE-O
EC17 22U-25DE (change for layout)
C128 .1U-04
ONLY for ALC662

Cn: R127 0 — +5VA — ONLY for ALC662

Co: R126 0-O — +LDOVDD — ONLY for ALC892

5V Max:38 mA

AUD_VCC — R277 0-04-O — AUD_P9
+3VSB — R292 0-04
to fix HDA_SDO strap issue;

Resistors Networks

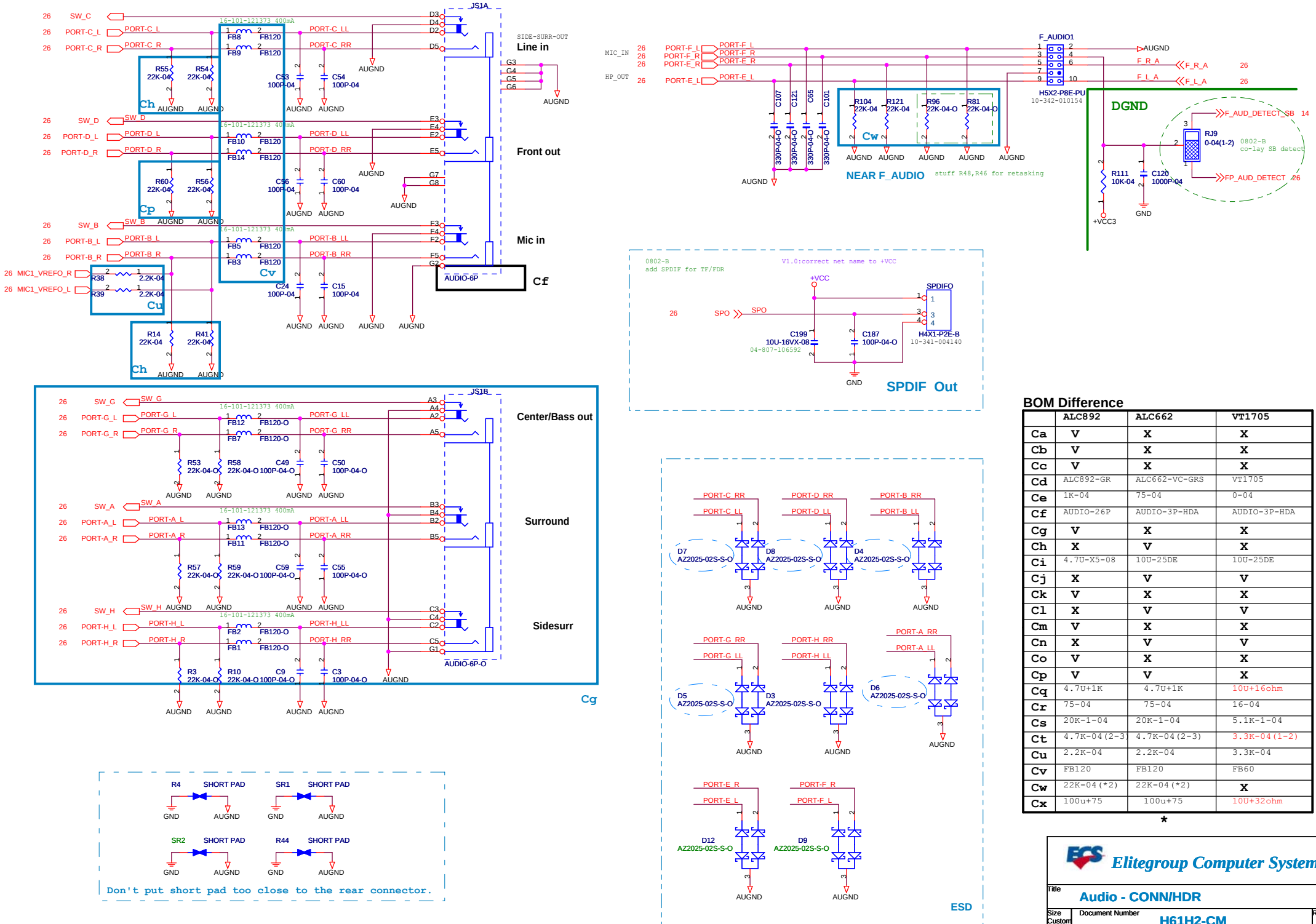
Placement near to codec

NETA — C68 100P-04-O (reserve cap for VIA) — AUGND
R84 5.1K-1-04 SW_D — SW_D 27
R85 10K-1-04 SW_C — SW_C 27
R83 20K-1-04 SW_B — SW_B 27
R82 39.2K-1-04-O SW_A — SW_A 27
Cb

NETB — C18 100P-04-O (reserve cap for VIA) — AUGND
R35 20K-1-04 F_R_A — F_R_A 27
R34 39.2K-1-04 F_L_A — F_L_A 27
R36 10K-1-04-O SW_G — SW_G 27
R37 5.1K-1-04-O SW_H — SW_H 27
Cc

Elitegroup Computer Systems

Title	Audio -ALC892 COLAY 662	
Size: Custom	Document Number: H61H2-CM	Rev: V1.0
Date: Monday, December 20, 2010	Sheet 26 of 42	



BOM Difference

	ALC892	ALC662	VT1705
Ca	V	X	X
Cb	V	X	X
Cc	V	X	X
Cd	ALC892-GR	ALC662-VC-GRS	VT1705
Ce	1K-04	75-04	0-04
Cf	AUDIO-26P	AUDIO-3P-HDA	AUDIO-3P-HDA
Cg	V	X	X
Ch	X	V	X
Ci	4.7U-X5-08	10U-25DE	10U-25DE
Cj	X	V	V
Ck	V	X	X
Cl	X	V	V
Cm	V	X	X
Cn	X	V	V
Co	V	X	X
Cp	V	V	X
Cq	4.7U+1K	4.7U+1K	10U+16ohm
Cr	75-04	75-04	16-04
Cs	20K-1-04	20K-1-04	5.1K-1-04
Ct	4.7K-04(2-3)	4.7K-04(2-3)	3.3K-04(1-2)
Cu	2.2K-04	2.2K-04	3.3K-04
Cv	FB120	FB120	FB60
Cw	22K-04(*2)	22K-04(*2)	X
Cx	100u+75	100u+75	10U+32ohm

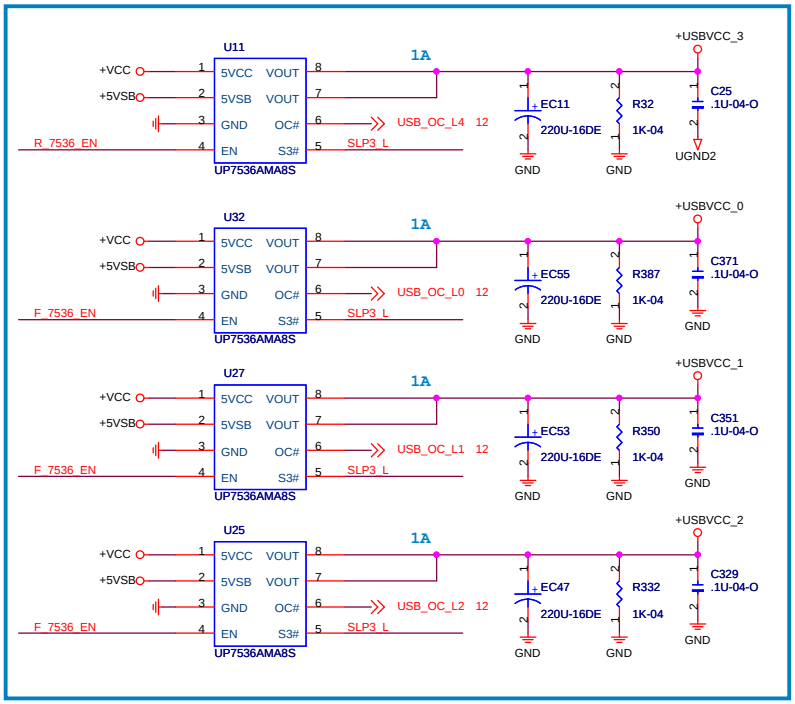
*

Elitegroup Computer Systems

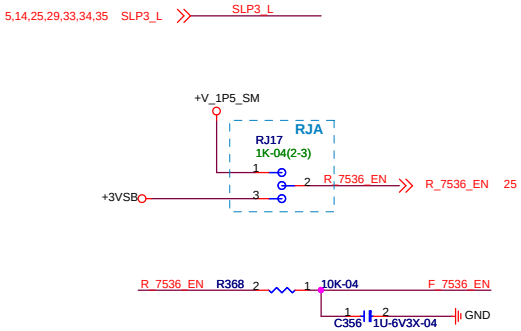
Title: Audio - CONN/HDR

Size: Custom | Document Number: H61H2-CM | Rev: V1.0

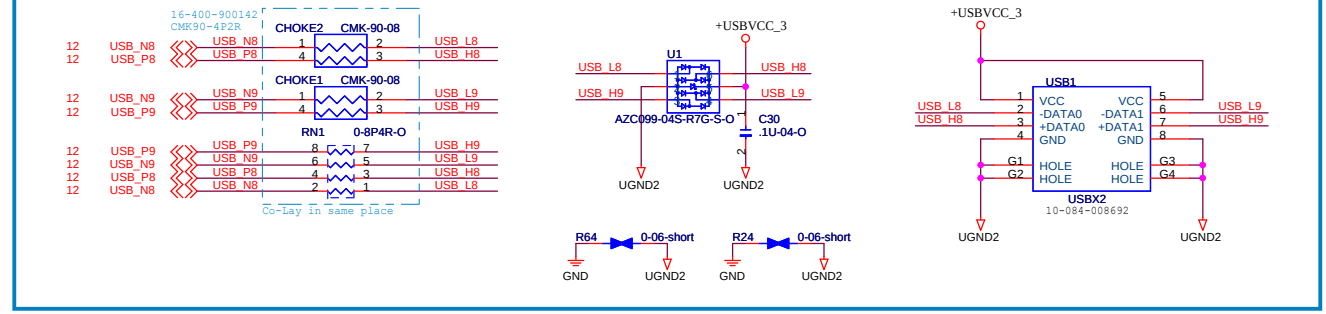
Date: Monday, December 20, 2010 | Sheet 27 of 42



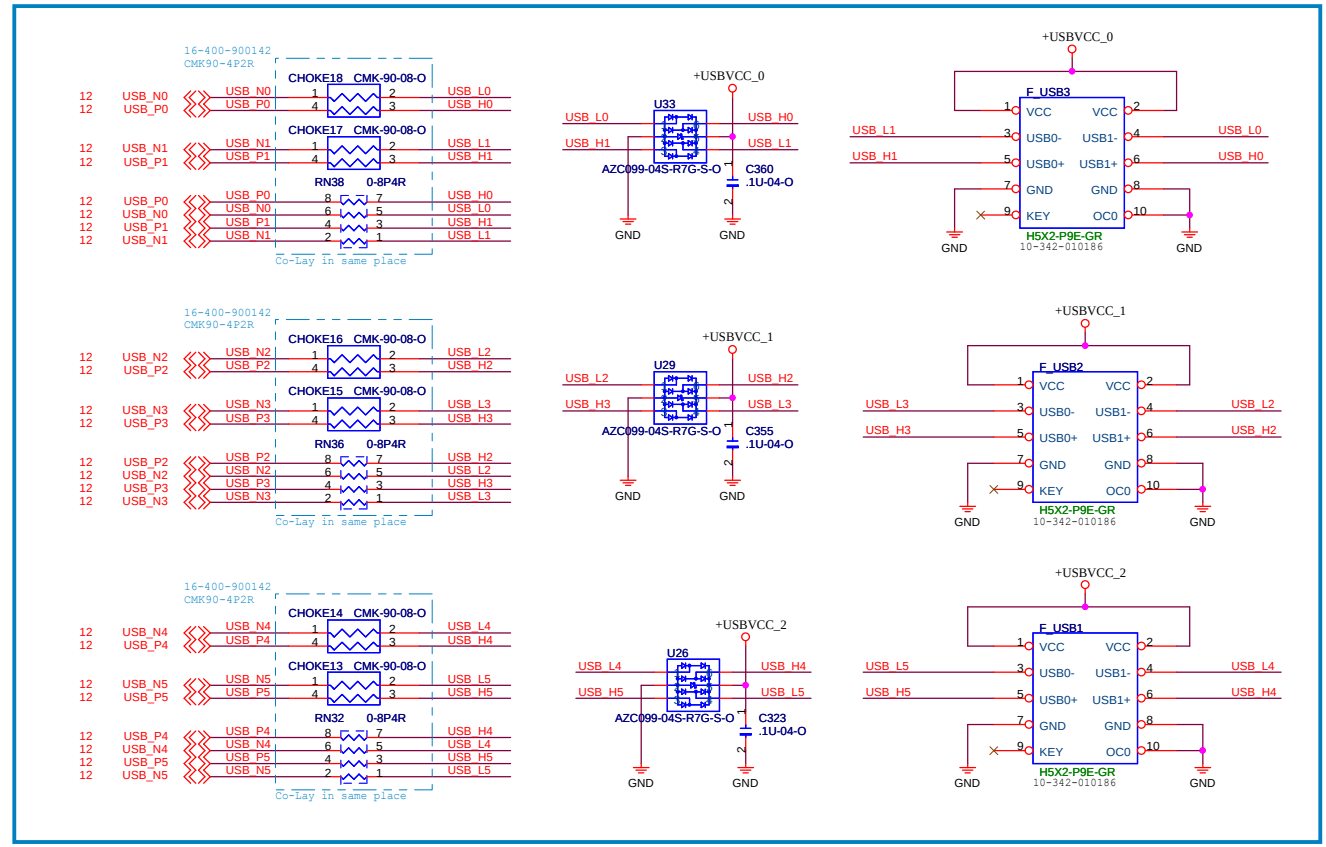
USB POWER CIRCUIT.



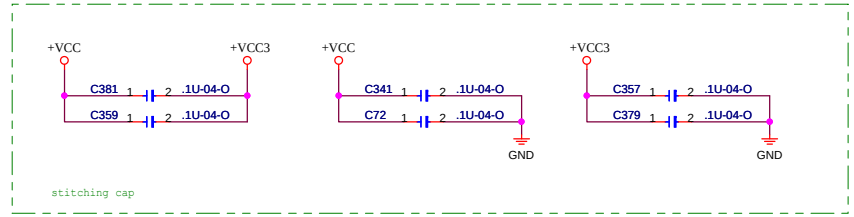
uP7536 Enable use	RJA	S4/S5 USB_5V_DUAL	Customer
VDIMM	0ohm (1-2)	0 Volt	FDR: may be reserved TF: W/USB_5V_DUAL S4/S5 W/USB_5V_DUAL
* +3VSB	1K (2-3)	5 Volt	



REAR SIDE 2 PORTS ON SINGLE USB CONN.



FRONT SIDE 6 PORTS on USB Header



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Title: USB - PWR/CONN/HDR

Size: Custom | Document Number: H61H2-CM | Rev: V1.0

Date: Monday, December 20, 2010 | Sheet 28 of 42

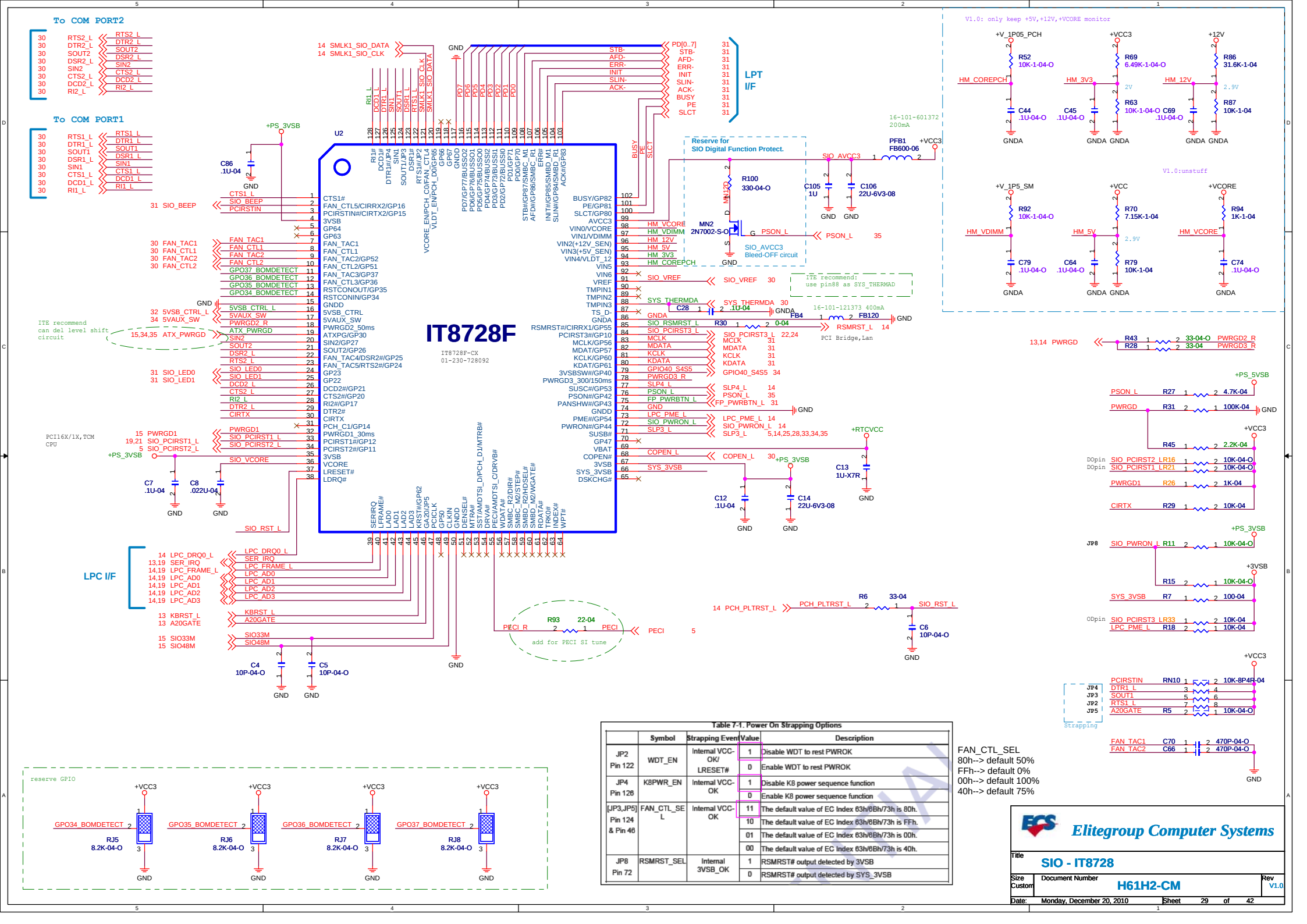
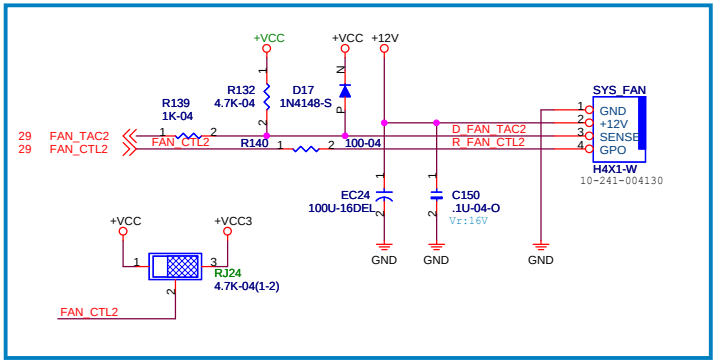


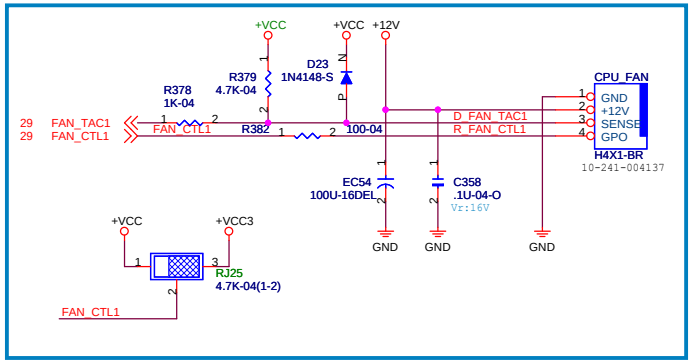
Table 7-1. Power On Strapping Options

	Symbol	Strapping Event	Value	Description
JP2 Pin 122	WDT_EN	Internal VCC-OK/ LRESET#	1	Disable WDT to rest PWROK
			0	Enable WDT to rest PWROK
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
[JP3,JP5] Pin 124 & Pin 46	FAN_CTL_SEL	Internal VCC-OK	11	The default value of EC Index 63h/6Bh/73h is 80h.
			10	The default value of EC Index 63h/6Bh/73h is FFh.
			01	The default value of EC Index 63h/6Bh/73h is 00h.
			00	The default value of EC Index 63h/6Bh/73h is 40h.
JP8 Pin 72	RSMRST_SEL	Internal 3VSB_OK	1	RSMRST# output detected by 3VSB
			0	RSMRST# output detected by SYS_3VSB

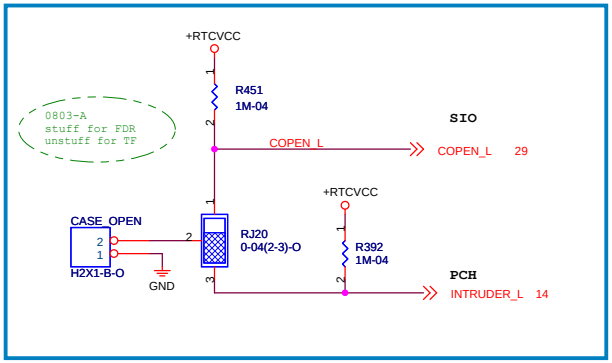
Elitegroup Computer Systems			
Title: SIO - IT8728			
Size: Custom	Document Number: H61H2-CM		Rev: V1.0
Date: Monday, December 20, 2010	Sheet 29 of 42		



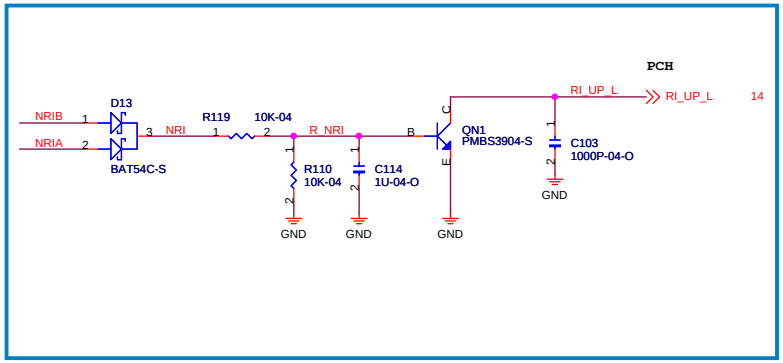
SYS FAN 4-PIN Circuit



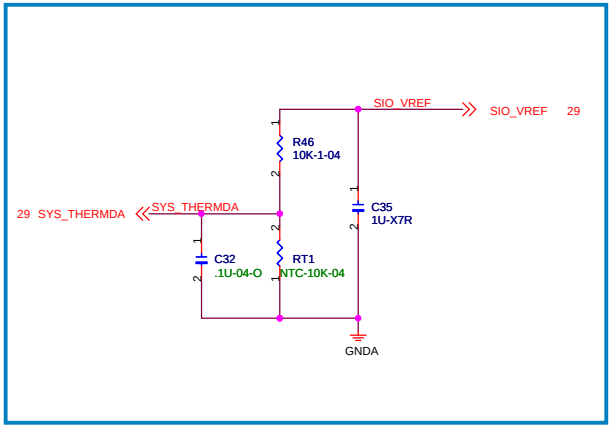
CPU FAN 4-PIN Circuit



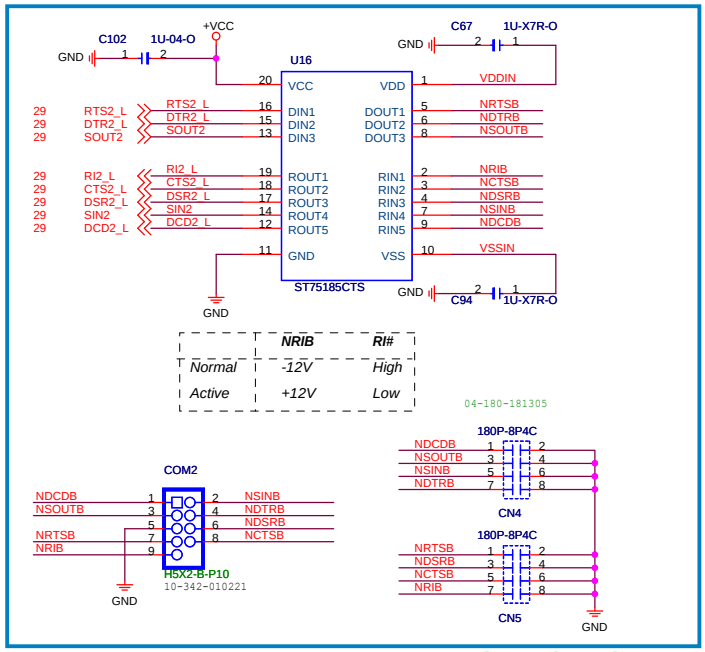
CASE Open Circuit



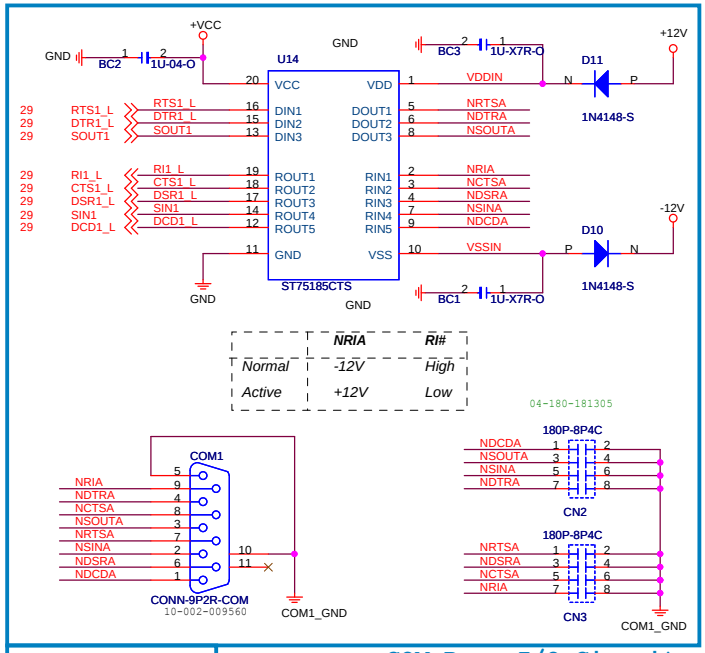
COM RI# Wake Up Circuit



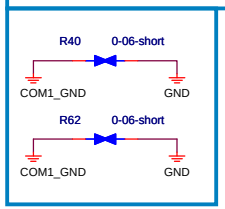
Thermal Sense



COM Header Circuit



COM Rear I/O Circuit



Elitegroup Computer Systems

Title: FAN, COM, CASE_OPEN, THERM

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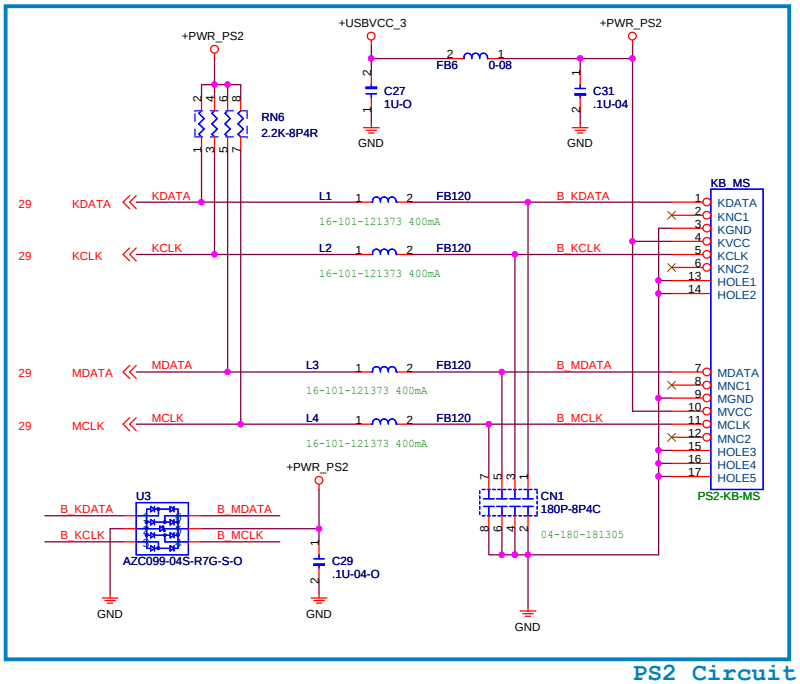
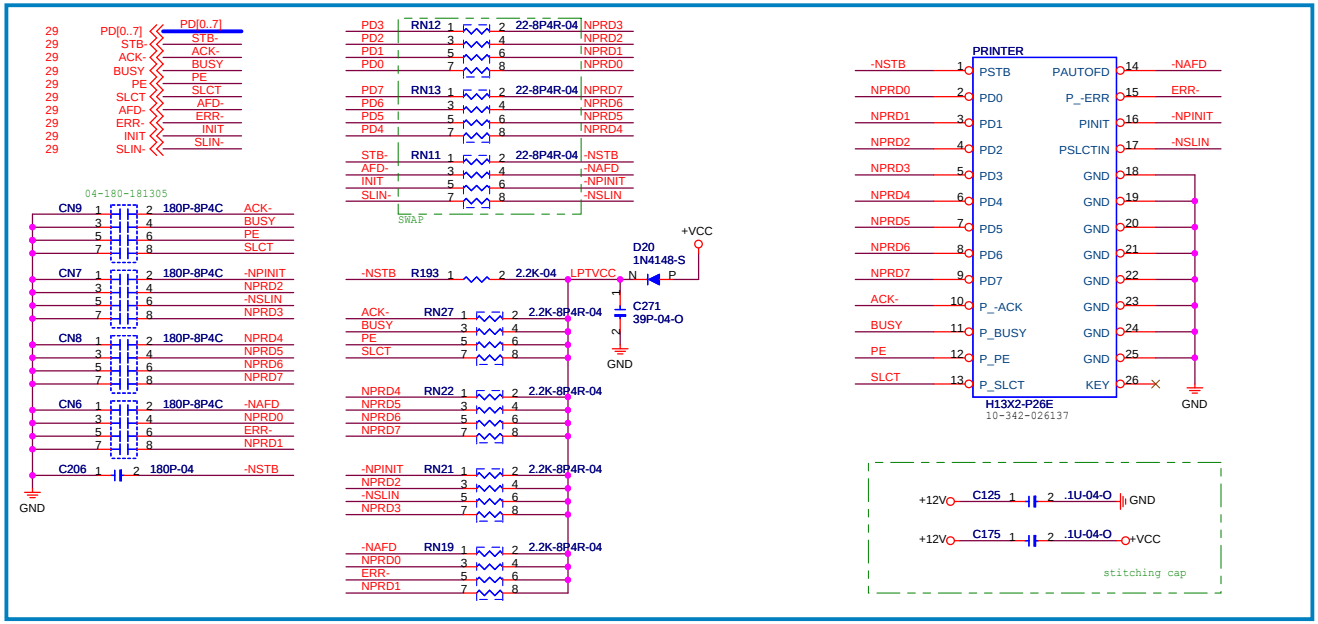
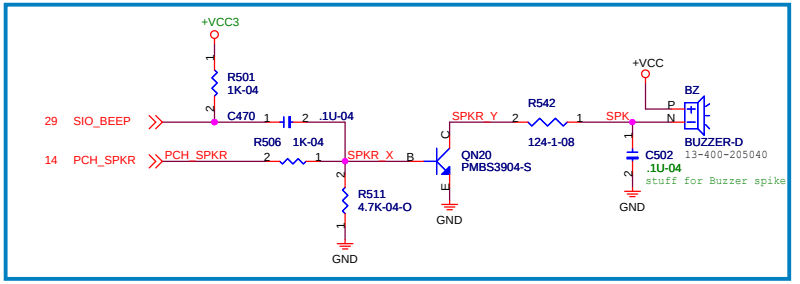


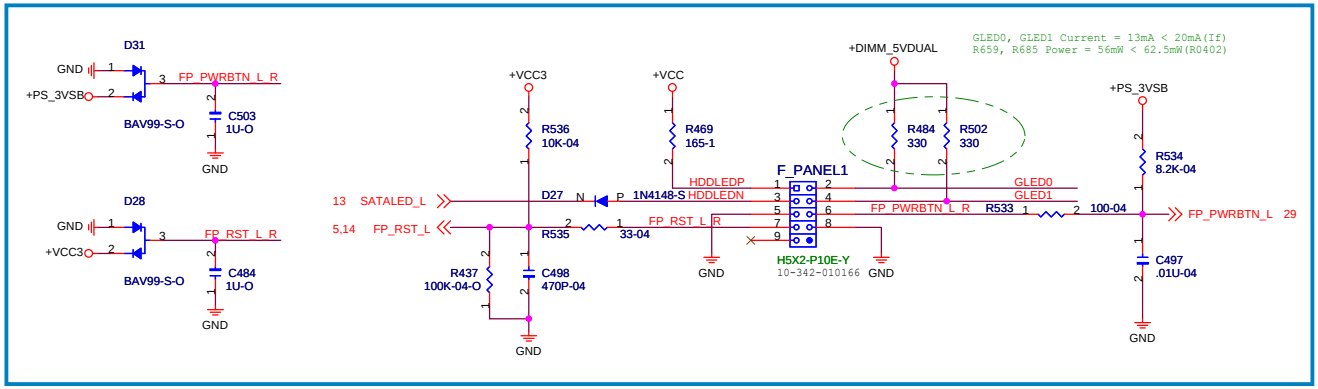
PS2 Circuit



LPT Header Circuit



Buzzer Circuit

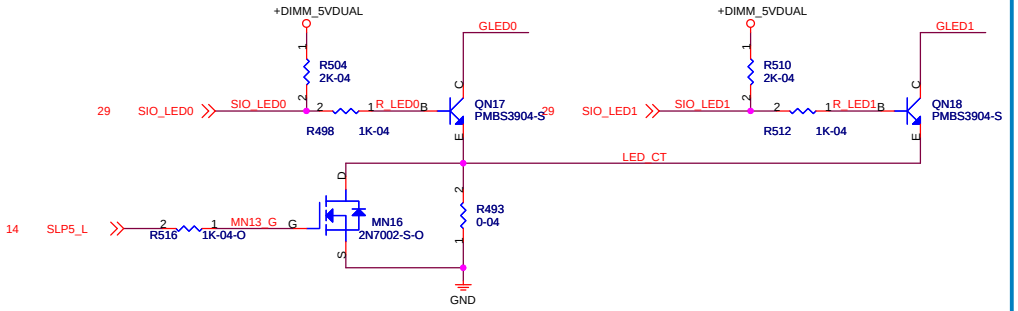


Front Panel Circuit

China-one PWR_LED SPEC

SYSTEM STATUS	SIGNAL-PWR_LED
NORMAL	STEADY_GREEN
S1	GREEN_BLINKING
S3,S4,S5	OFF

Intel GLED0 G GLED1



Front LED

Elitegroup Computer Systems

Title	F_PANEL, BUZ, PS2, LPT	
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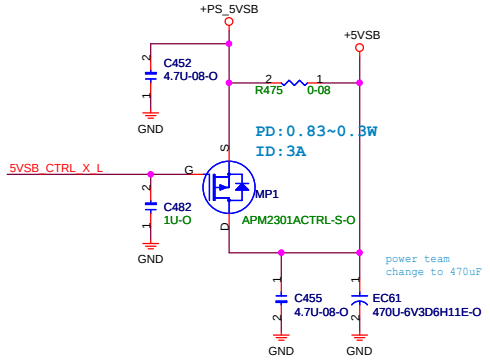
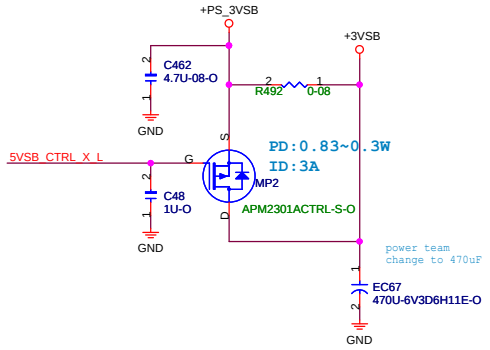
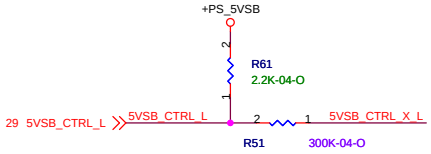
EuP Lot6 Power Saving Circuit







add R51 to Fix EUP enable STBY drop

V1.0:因1M會跟MOS內阻分壓導致5VSB_CTRL_X_L位準偏低造成漏電。

Layout Note:
Close to ATX 24P2R Connector.

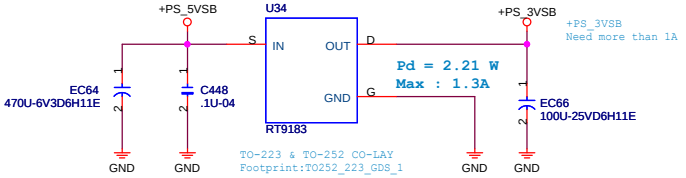
EuP Lot6 2013 0.5W:

PWR STATE	+5VSB Source
S0	+PS_5VSB
S3	+PS_5VSB
S4	OFF
S5	OFF

*** China one Enery Saving Spec**

Customer	S3	S5
TF	< 0.4A	< 0.18A
FDR	< 0.3A	< 0.15A

+3VSB Circuit



★ 02-347-183840: 0.74W
IC REG.RT9183-33GGF..SOT-223(F-TYPE).
3.3V.1.5A.....LEAD-FREE(RoHS/HF).RICHTEK
XX-XXX-XXXXXX: 1.333W
RT9183-33GLF TO-252

3VSB Non-EuP Lot6 Mode:

Power Name	Current
4 Slots	0.375 X4 = 1.5A
LAN	16m + 49m = 65mA
PCH	123mA
TPM(WPCT210)	50mA
EPW	16mA
SPI	mA
SIO	mA
Total Current	+ 1.754 A

Del PCH_MEPWROK Circuit

del 3VDual ,VCC3_EPW control

Elitegroup Computer Systems

Title: DC/DC 3VDUAL,EUP		
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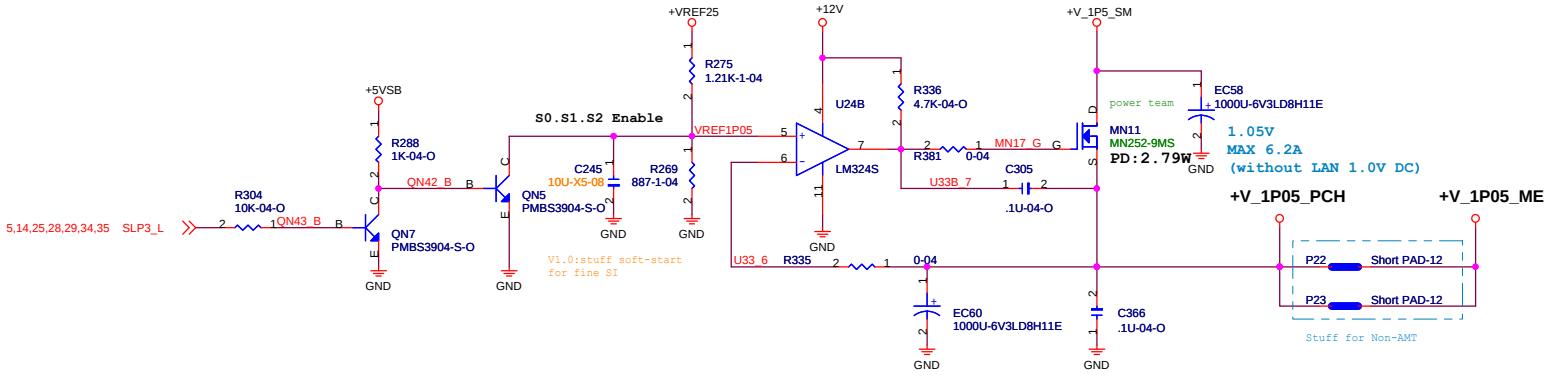
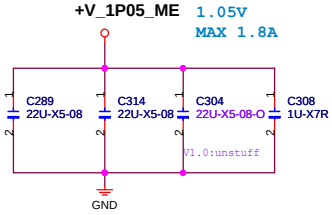
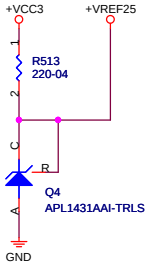
V1P05_PCH

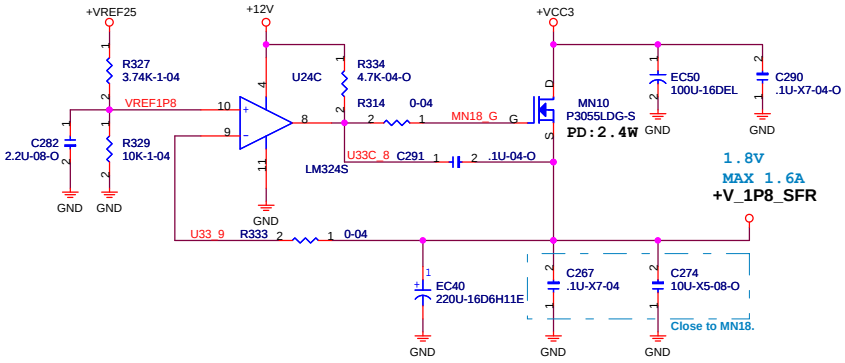


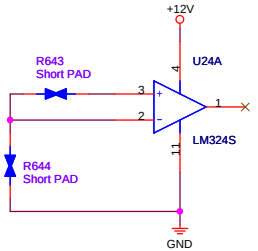


VREF25



V1P8_SFR(1.5A max)





del 1.05V ME power

V1P05_ME

Elitegroup Computer Systems		
Title: DC/DC V1P05_PCH,ME/V1P8_SFR		
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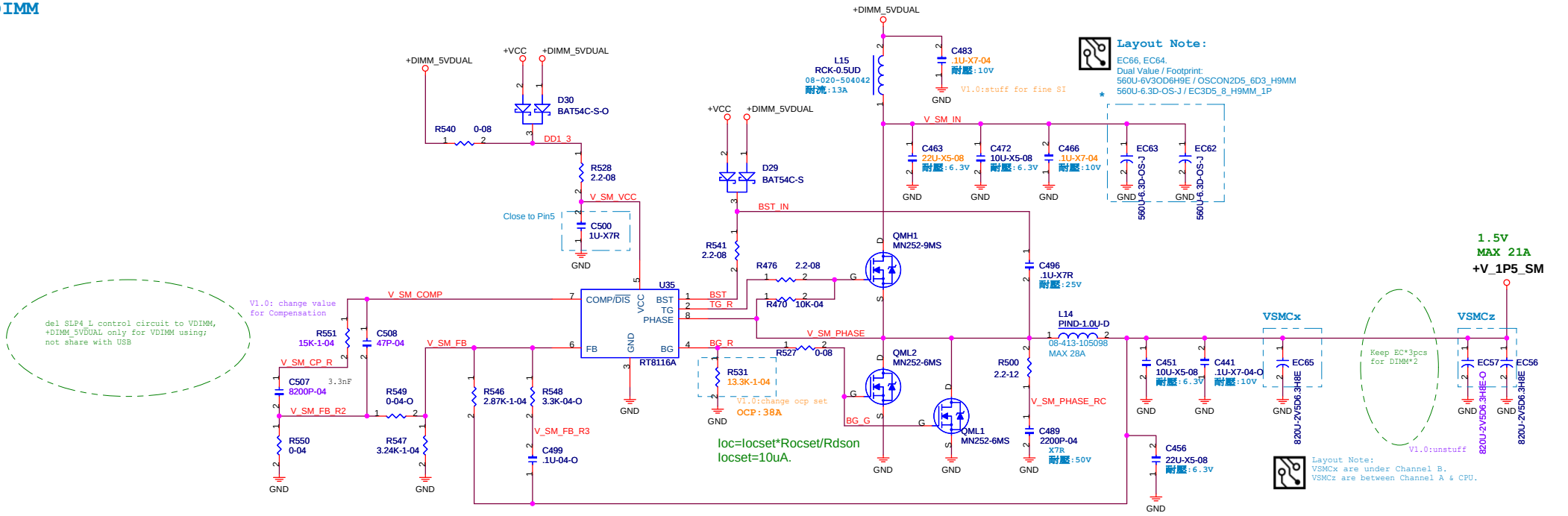
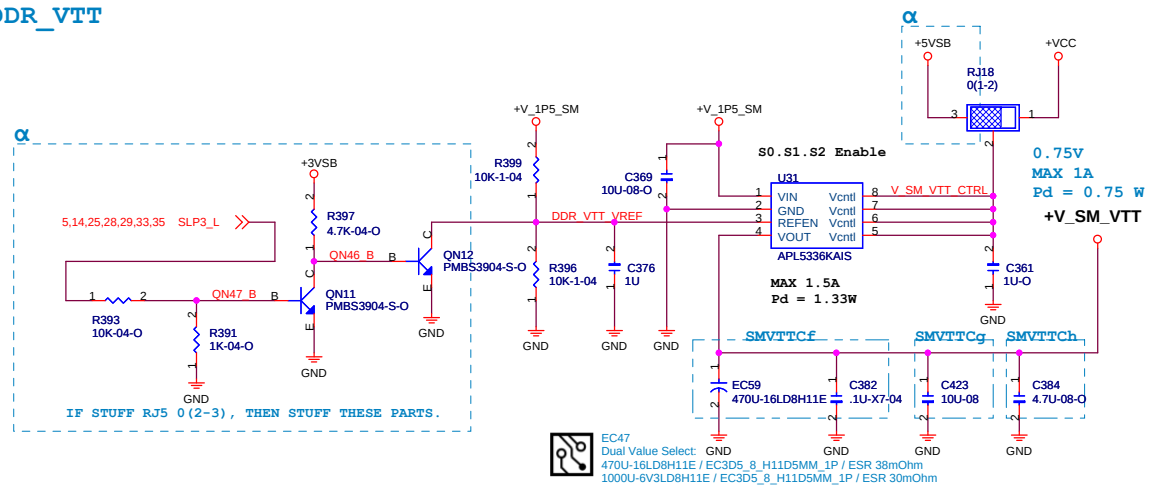
VDIMM

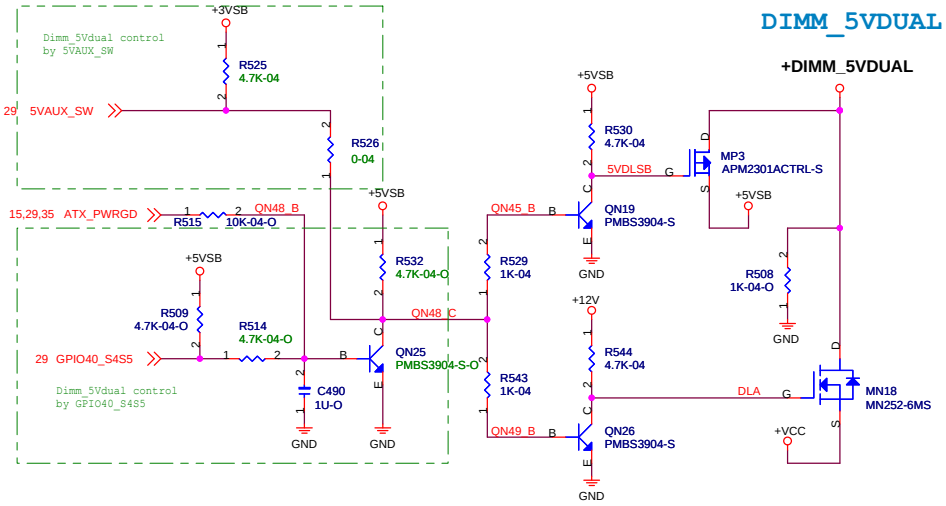


DDR_VTT



Layout Note:
SMVTTCf close to U39 Pin4.
SMVTTCg are between Channel A & B.
SMVTTCh are between Channel A & CPU.

DIMM_5VDUAL



*		S5	S0	S3
	5VAUX_SW	0	0	1
	GPIO40_S4S5	1	1	0
	+DIMM_5VDUAL	0	VCC	+5VSB

Elitegroup Computer Systems

Title: DC/DC VDIMM/DDR_VTT/5VDUAL

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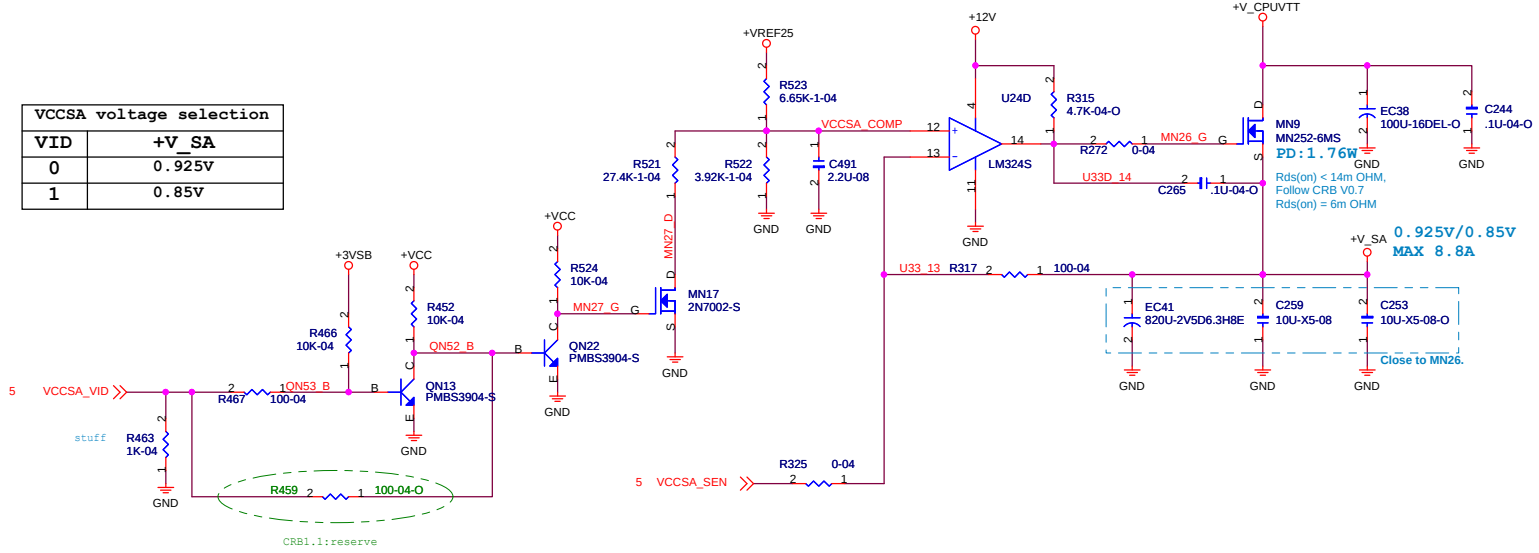
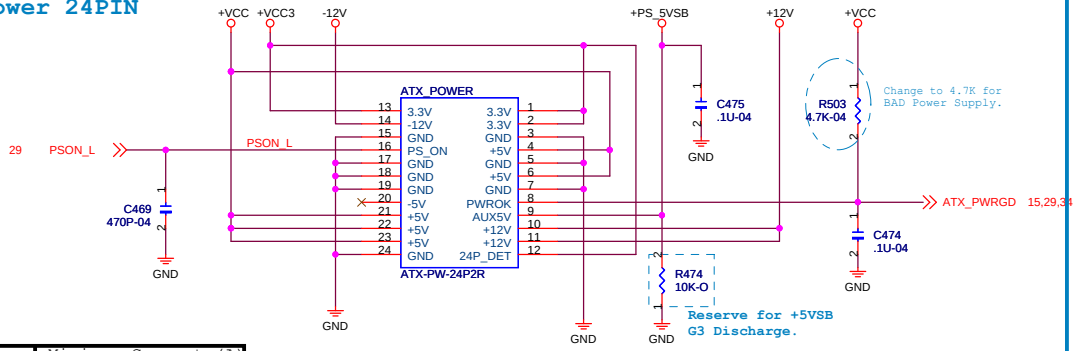
+V_SA

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

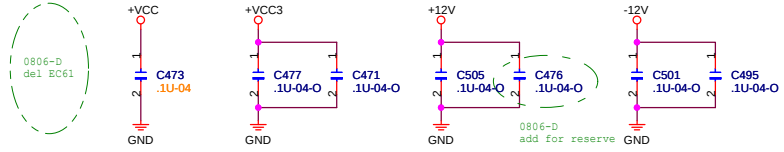
*

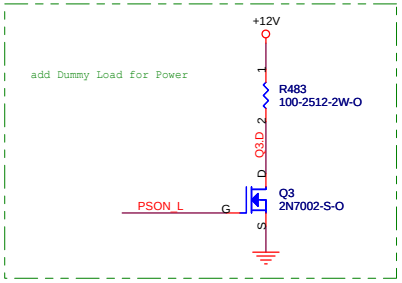


ATX Power 24PIN

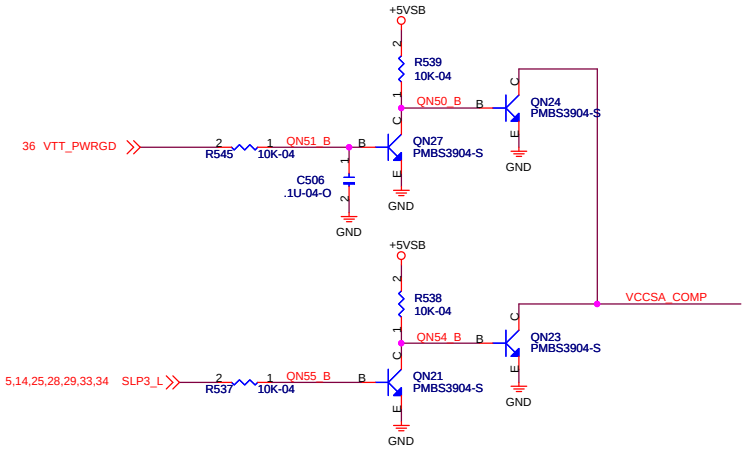


OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0





VCCSA Sequence



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Title	DC/DC VCCSA, ATXPWR	
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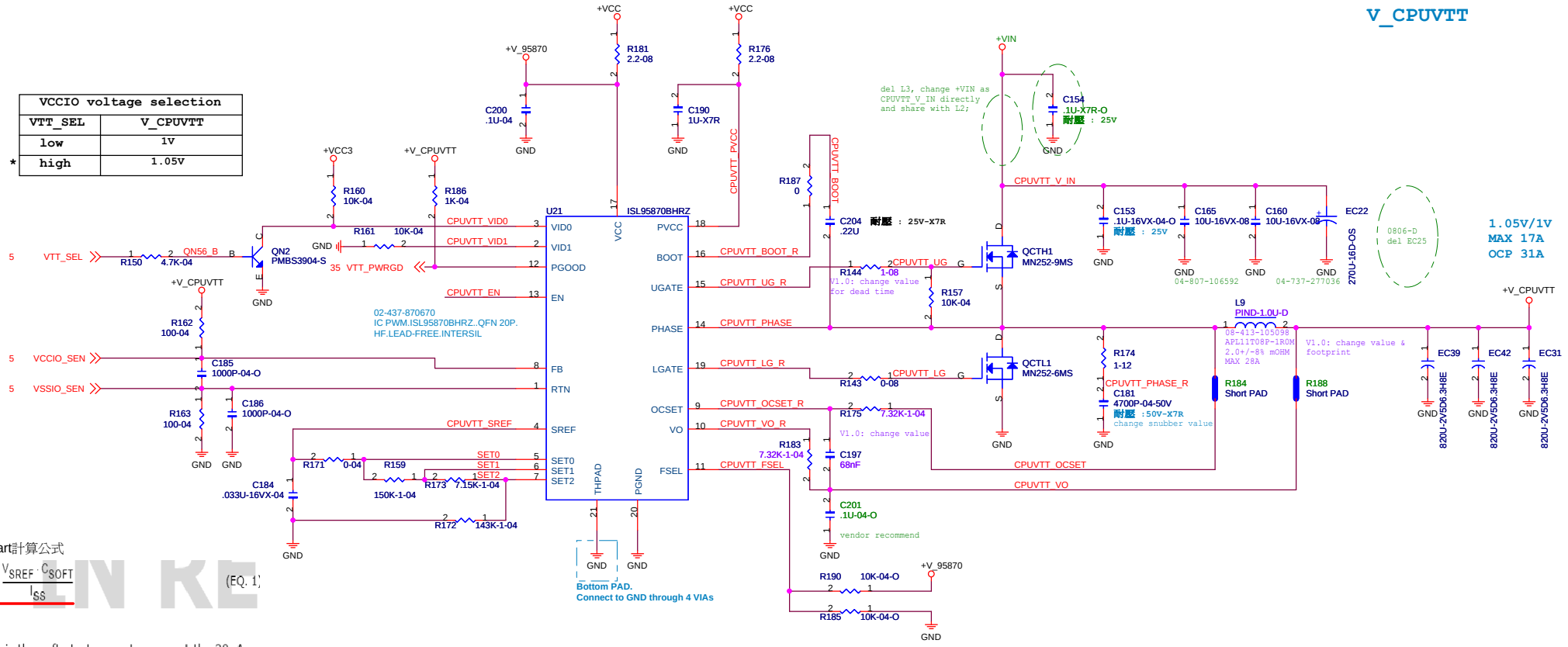
V_CPUVTT

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
* high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad \text{(EQ. 1)}$$

Where:

- I_{SS} is the soft-start current source at the 20µA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad \text{(EQ. 21)}$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 22)}$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 23)}$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \text{(EQ. 24)}$$

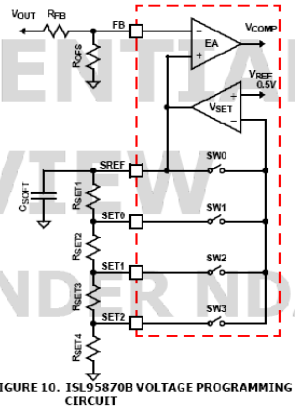
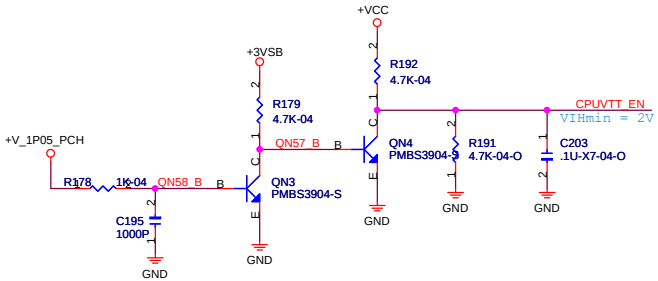


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC



Elitegroup Computer Systems

Title: DC/DC V_CPUVTT

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V1.0:change PWM IC

0608_DEL_SVID_DEBUG_PORT

02-437-364670
IC PWM ISL6364CRZ_QFN 48P.
HF LEAD-FREE INTERSIL

U37 ISL6364CRZ

In VR12 SPEC,
Serial VID includes IMON Data.

Bottom PAD.
Connect to GND through 8 VIAs

V1.0:change for IMON & IMOS
FS_DRP & FS_DRPS RSET
SICI

V1.0:change for FBS & HFCOMPS/DVCS COMPS

V1.0:change for R-C Mach Vcore & Vaxg RISEN CT

0623 ADD

Stuff for Disable PWM4.

Vendor:L/DCR=R*C , 0.3/0.65=0.1*R, R*1.25=5.76K

For VR_READY Power On Sequence

Elitegroup Computer Systems			
Title: DC/DC VCORE/VAXG1			
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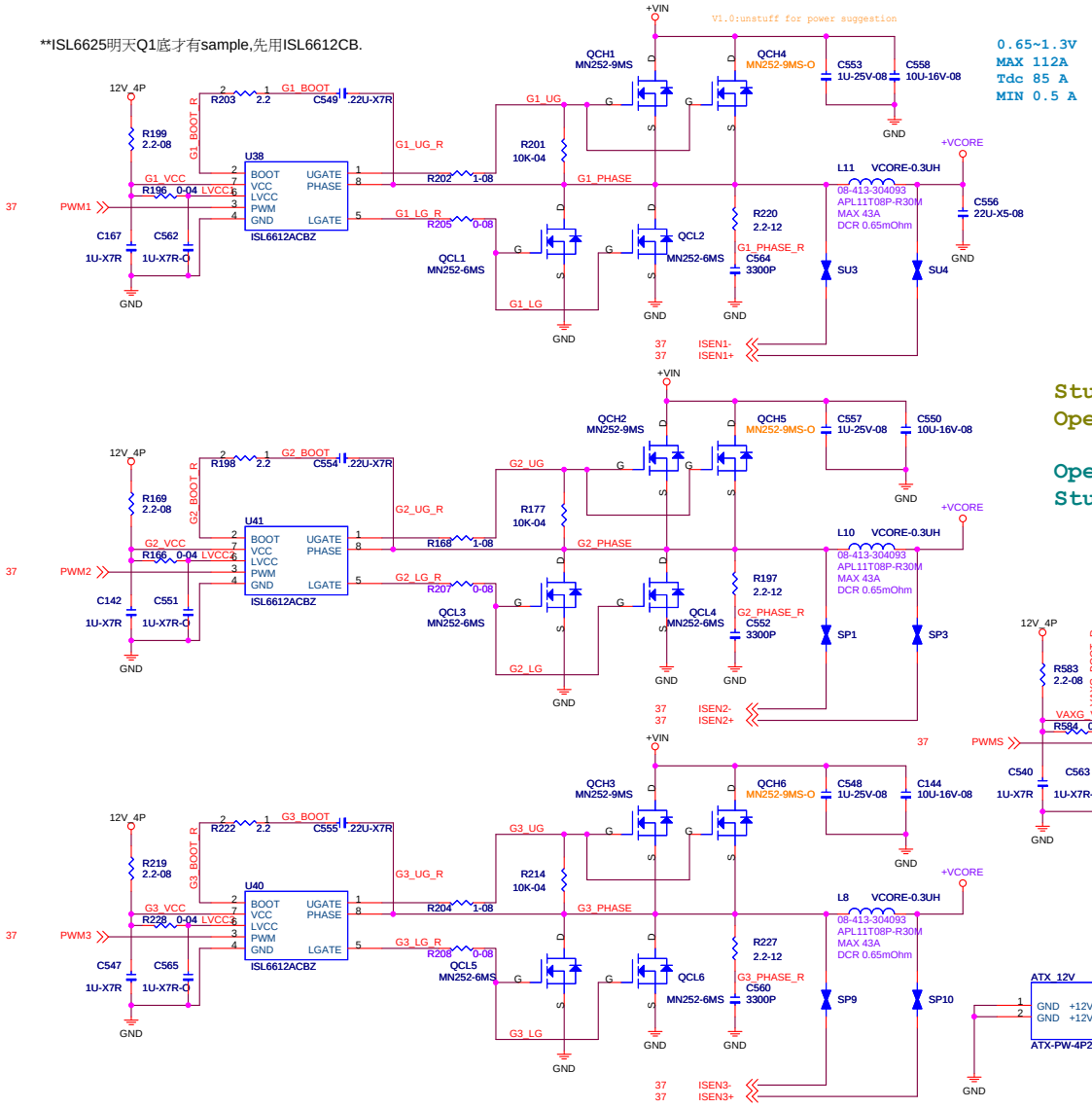
V1.0:change PWM IC

**ISL6625明天Q1底才有sample,先用ISL6612CB.



Elitegroup Computer Systems

Title	DC/DC VCORE/VAXG2	
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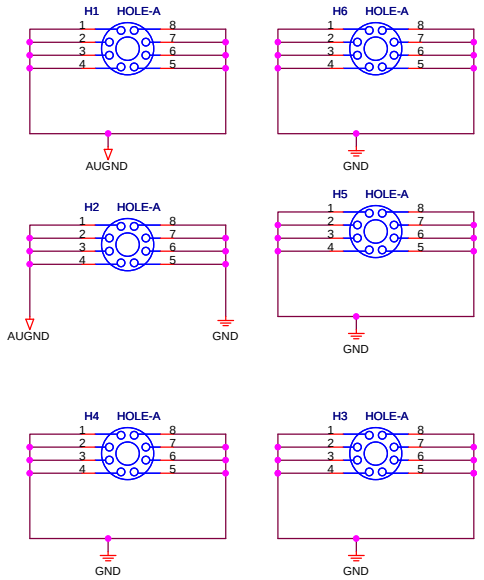
PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down，No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up，intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up，“topblock swap” mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up，Integrated 1.05V VRM Enable
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up，The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up，The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TVS	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Enable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

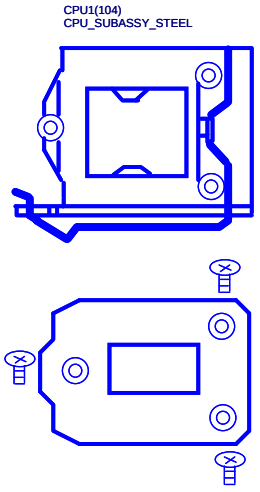
Table 7-1. Power On Strapping Options

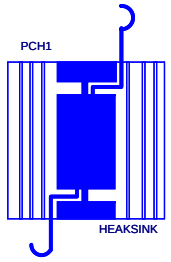
	Symbol	Strapping Event	Value	Description
JP2 Pin 122	Flashseg1_EN	Internal VCC-OK/ LRESET#	1	Disable
			0	Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
[JP3,JP5] Pin 124 & Pin 46	FAN_CTL_SEL	Internal VCC-OK	11	The default value of EC Index 63h/6Bh/73h is 80h.
			10	The default value of EC Index 63h/6Bh/73h is FFh.
			01	The default value of EC Index 63h/6Bh/73h is 00h.
			00	The default value of EC Index 63h/6Bh/73h is 40h.

V1.0.:update hole,del pin9, and use pin1

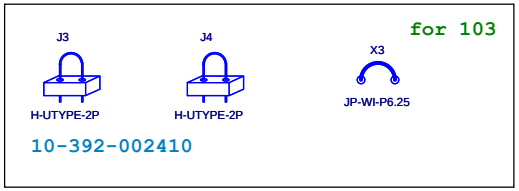


15-Y84-011090 PCB M/B.H61H2-CM.V1.0(.)....244*200*1.6mm.4L..LEAD-FREE.GREEN.OSP.....GE1





20-120-Y84000
20-120-Y84001



Elitegroup Computer Systems

Title	104 & STRAPPING	
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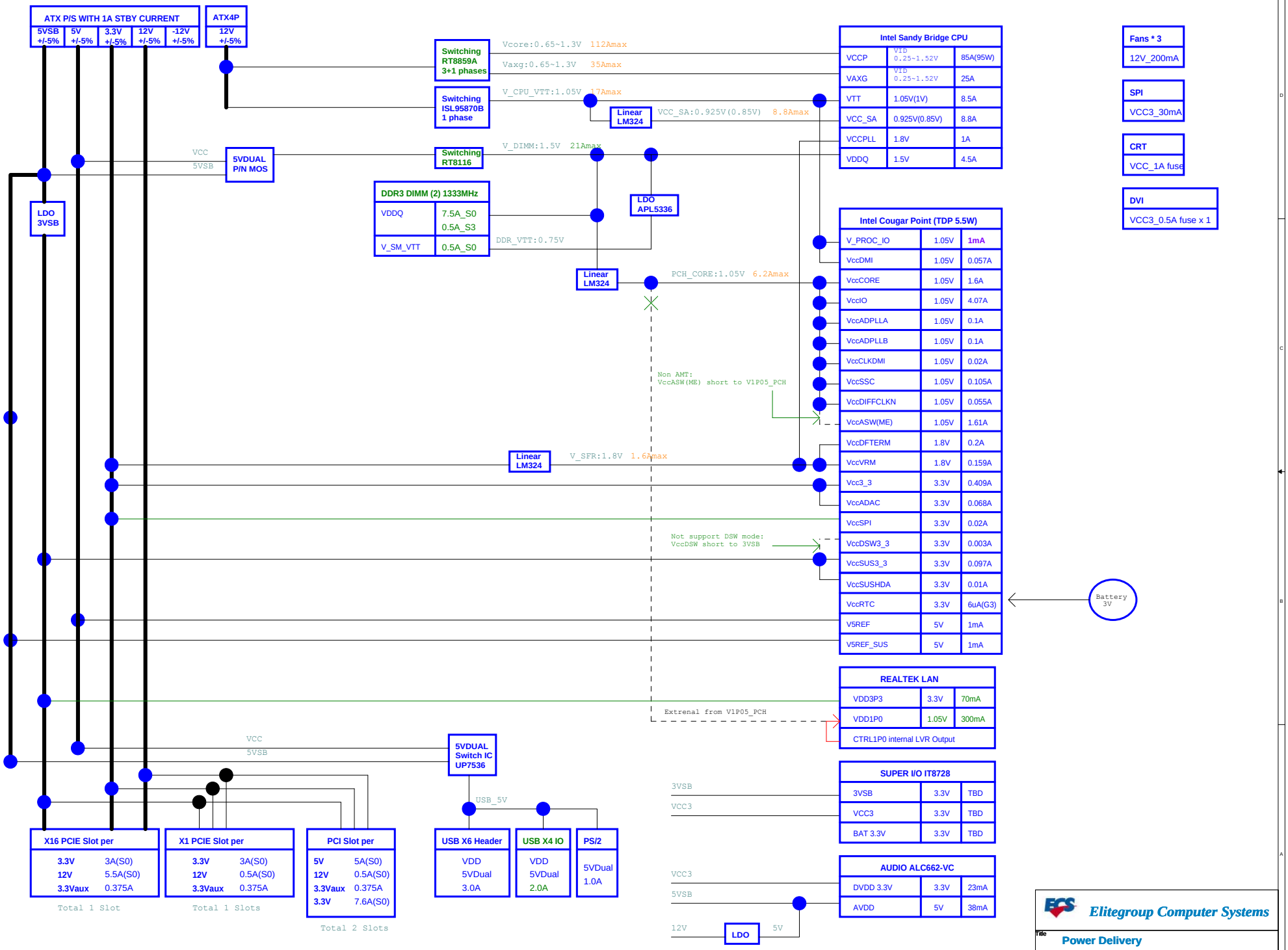
ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
ATX4P
12V +/-5%
Switching RT8859A 3+1 phases
Vcore:0.65~1.3V 112Amax
Vaxg:0.65~1.3V 35Amax
Switching ISL95870B 1 phase
V_CPU_VTT:1.05V 17Amax
Linear LM324
VCC_SA:0.925V(0.85V) 8.8Amax
Intel Sandy Bridge CPU
VCCP VID 0.25~1.52V 85A(95W)
VAXG VID 0.25~1.52V 25A
VTT 1.05V(1V) 8.5A
VCC_SA 0.925V(0.85V) 8.8A
VCCPLL 1.8V 1A
VDDQ 1.5V 4.5A
Fans * 3
12V_200mA
SPI
VCC3_30mA
CRT
VCC_1A fuse
DVI
VCC3_0.5A fuse x 1
VCC
5VSB
5VDUAL P/N MOS
Switching RT8116
V_DIMM:1.5V 21Amax
DDR3 DIMM (2) 1333MHz
VDDQ 7.5A_S0 0.5A_S3
V_SM_VTT 0.5A_S0
LDO APL5336
DDR_VTT:0.75V
LDO 3VSB
Linear LM324
PCH_CORE:1.05V 6.2Amax
Intel Cougar Point (TDP 5.5W)
V_PROC_IO 1.05V 1mA
VccDMI 1.05V 0.057A
VccCORE 1.05V 1.6A
VccIO 1.05V 4.07A
VccADPLLA 1.05V 0.1A
VccADPLLB 1.05V 0.1A
VccCLKDMI 1.05V 0.02A
VccSSC 1.05V 0.105A
VccDIFFCLKN 1.05V 0.055A
VccASW(ME) 1.05V 1.61A
VccDFTERM 1.8V 0.2A
VccVRM 1.8V 0.159A
Vcc3_3 3.3V 0.409A
VccADAC 3.3V 0.068A
VccSPI 3.3V 0.02A
VccDSW3_3 3.3V 0.003A
VccSUS3_3 3.3V 0.097A
VccSUSHDA 3.3V 0.01A
VccRTC 3.3V 6uA(G3)
V5REF 5V 1mA
V5REF_SUS 5V 1mA
Non AMT:
VccASW(ME) short to V1P05_PCH
Not support DSW mode:
VccDSW short to 3VSB
Battery 3V
Linear LM324
V_SFR:1.8V 1.6Amax
REALTEK LAN
VDD3P3 3.3V 70mA
VDD1P0 1.05V 300mA
CTRL1P0 internal LVR Output
Extrenal from V1P05_PCH
VCC
5VSB
5VDUAL Switch IC UP7536
USB_5V
3VSB
VCC3
SUPER I/O IT8728
3VSB 3.3V TBD
VCC3 3.3V TBD
BAT 3.3V 3.3V TBD
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 1 Slots
PCI Slot per
5V 5A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
3.3V 7.6A(S0)
Total 2 Slots
USB X6 Header
VDD
5VDual
3.0A
USB X4 IO
VDD
5VDual
2.0A
PS/2
5VDual
1.0A
VCC3
5VSB
12V
LDO
5V
AUDIO ALC662-VC
DVDD 3.3V 3.3V 23mA
AVDD 5V 38mA
Elitegroup Computer Systems
Title
Power Delivery
Size C
Document Number H61H2-CM
Rev V1.0
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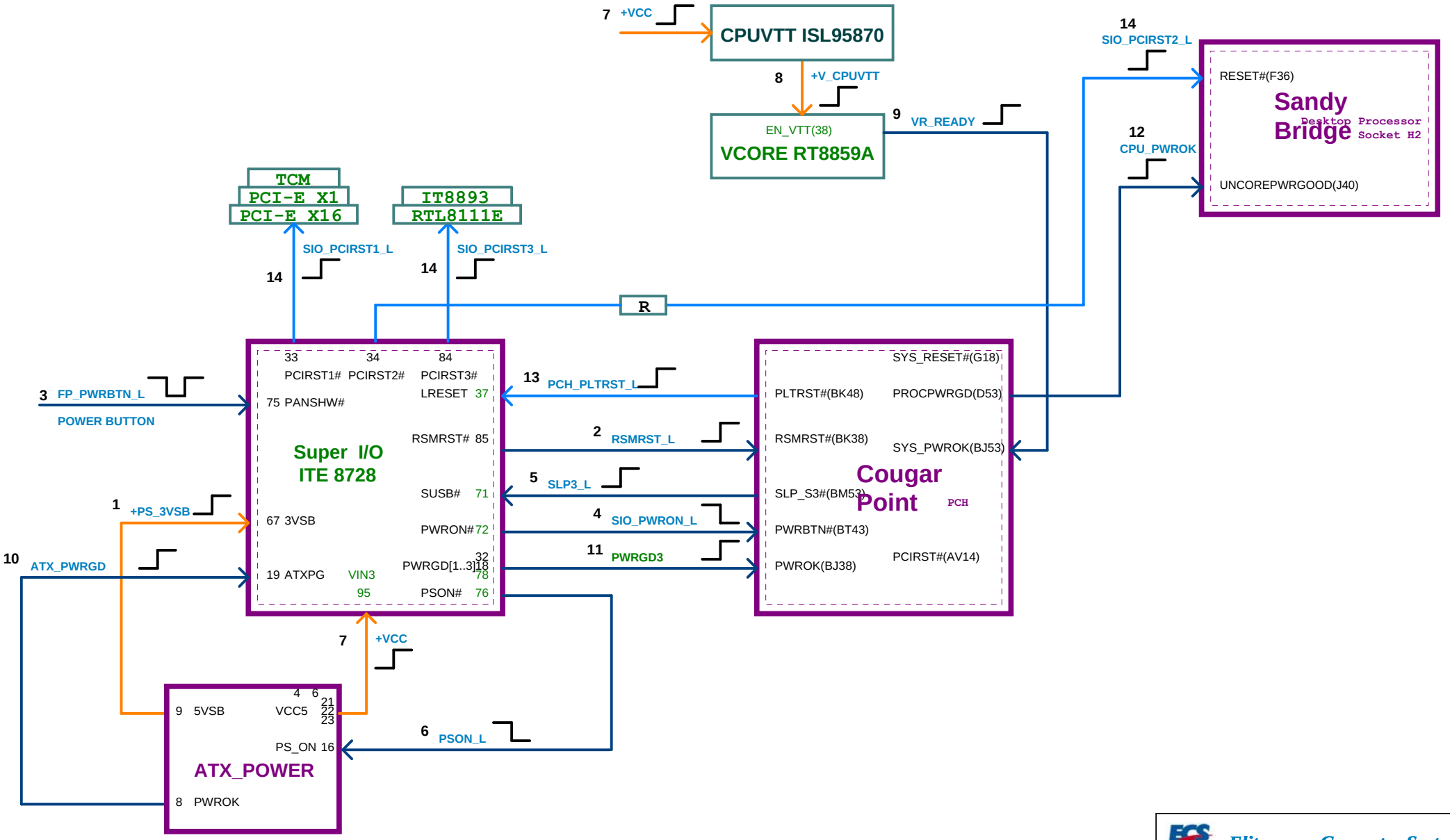

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Title	Power Sequence, Reset Diagram	
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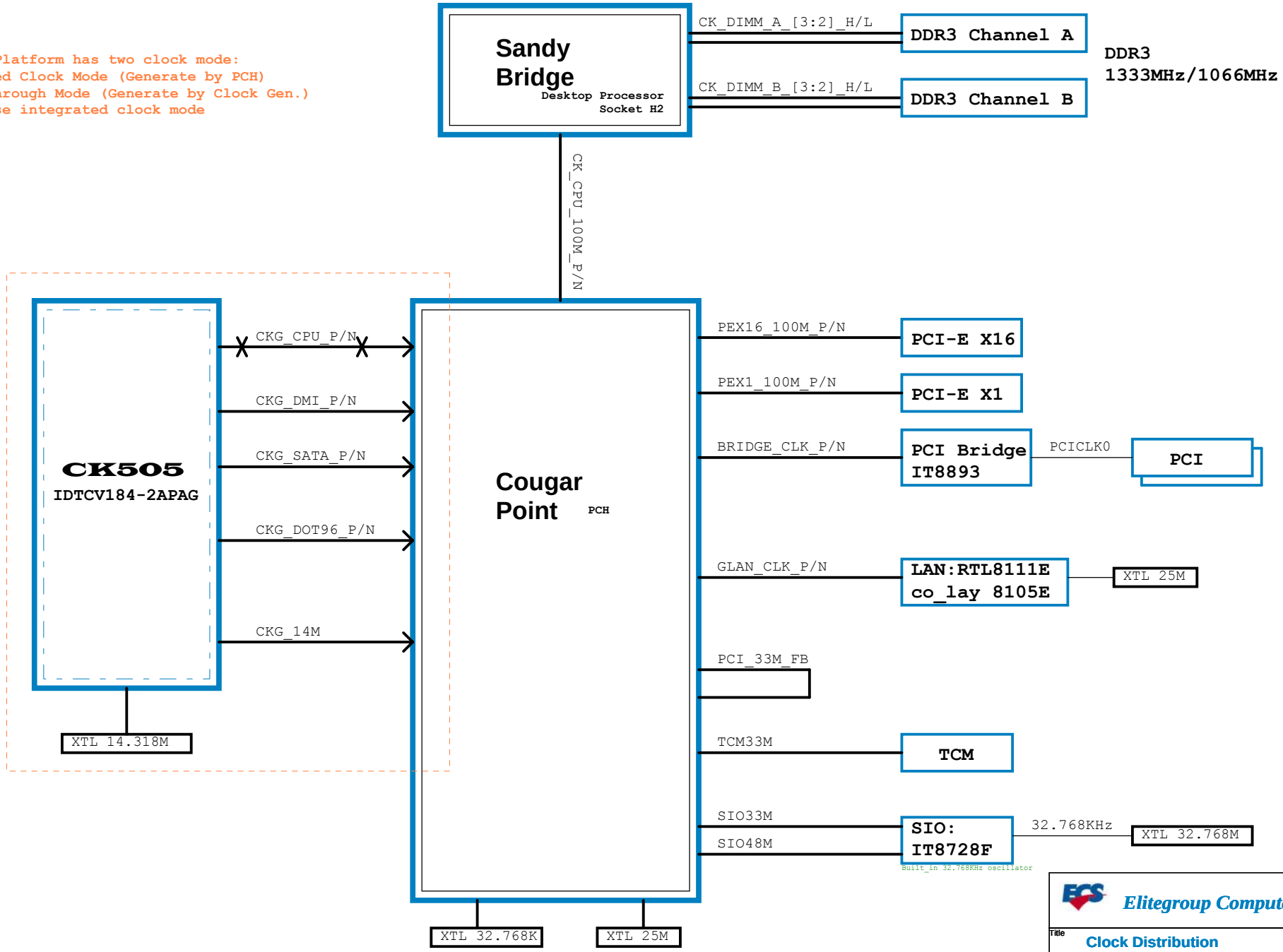
NOTE:

Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
H61H2-CM use integrated clock mode



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Title: Clock Distribution		
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