MS-7853 Ver: 1.0

CPU:

INTEL - Celeron 887 BGA1023

System Chipset:

INTEL - NM70 BGA989

OnBoard Chipset:

HD Audio Codec:ALC662-VD
LAN:RTL8105E-VD Co-lay RTL8111F-VB
SIO:Nuvoton NCT5533D
Flash ROM: 64Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) *1

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 1
Mini PCIE Slot * 1

PWM:

Controller: Intersil / ISL95837 1+1 Phase
CPU+GPU: Intersil / ISL95837 1 Phase
CPU VTT:INTERSIL/ISL95870BHRZ-T 1 Phase
CPU SA : INTERSIL/ISL95870BHRZ-T 1 Phase
DDR:ON Semiconductor/NCP1589LMNTWG

ACPI:

UPI

Other:

SATA2.0 x1 (PCH)
SATA3.0 x1 (PCH)
USB2.0 RearX4 Front x4
D-SUB/HDMI/*1

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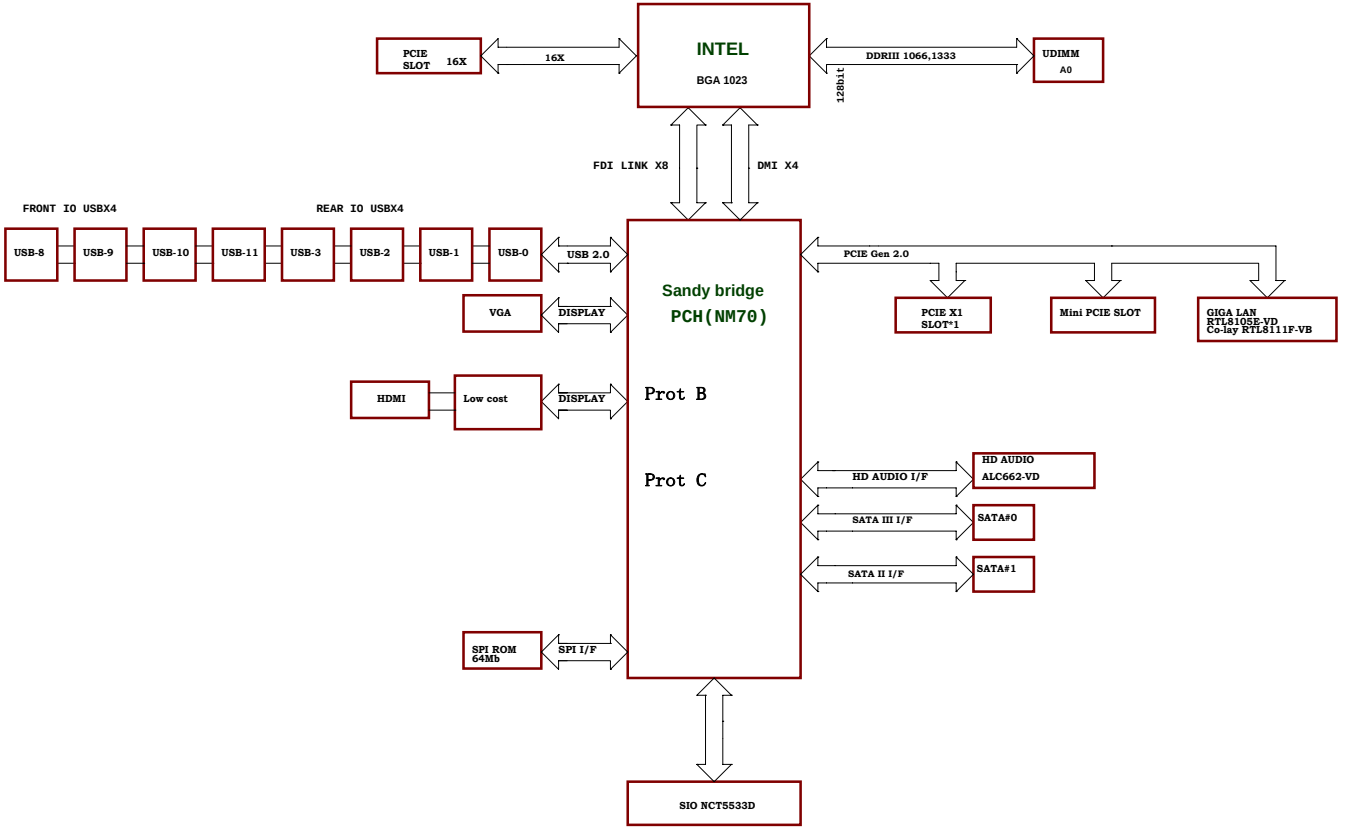

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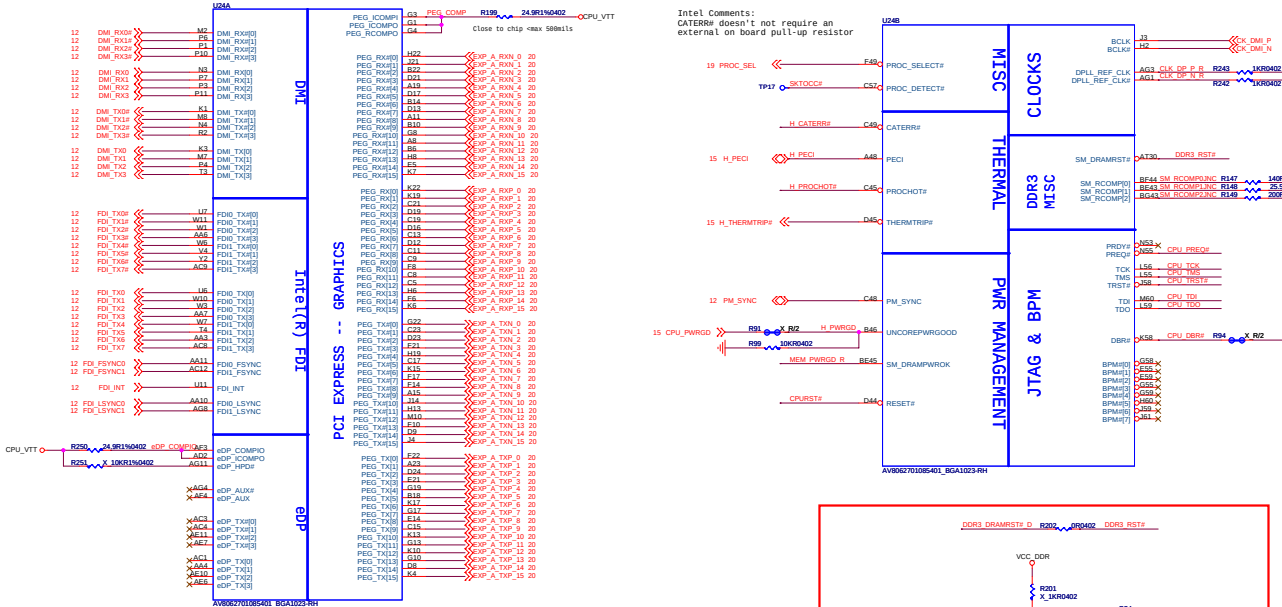
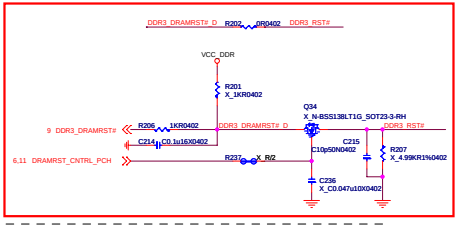
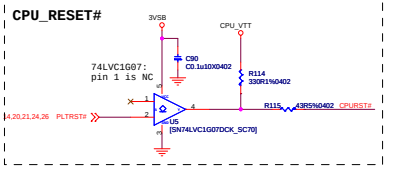
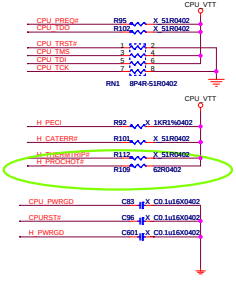
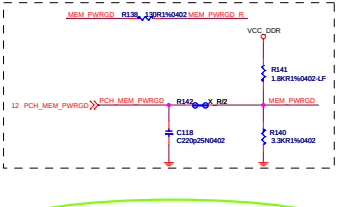
SANDY BRIDGE 2C BGA PROCESSOR (DMI,DP,PEG,FDI)



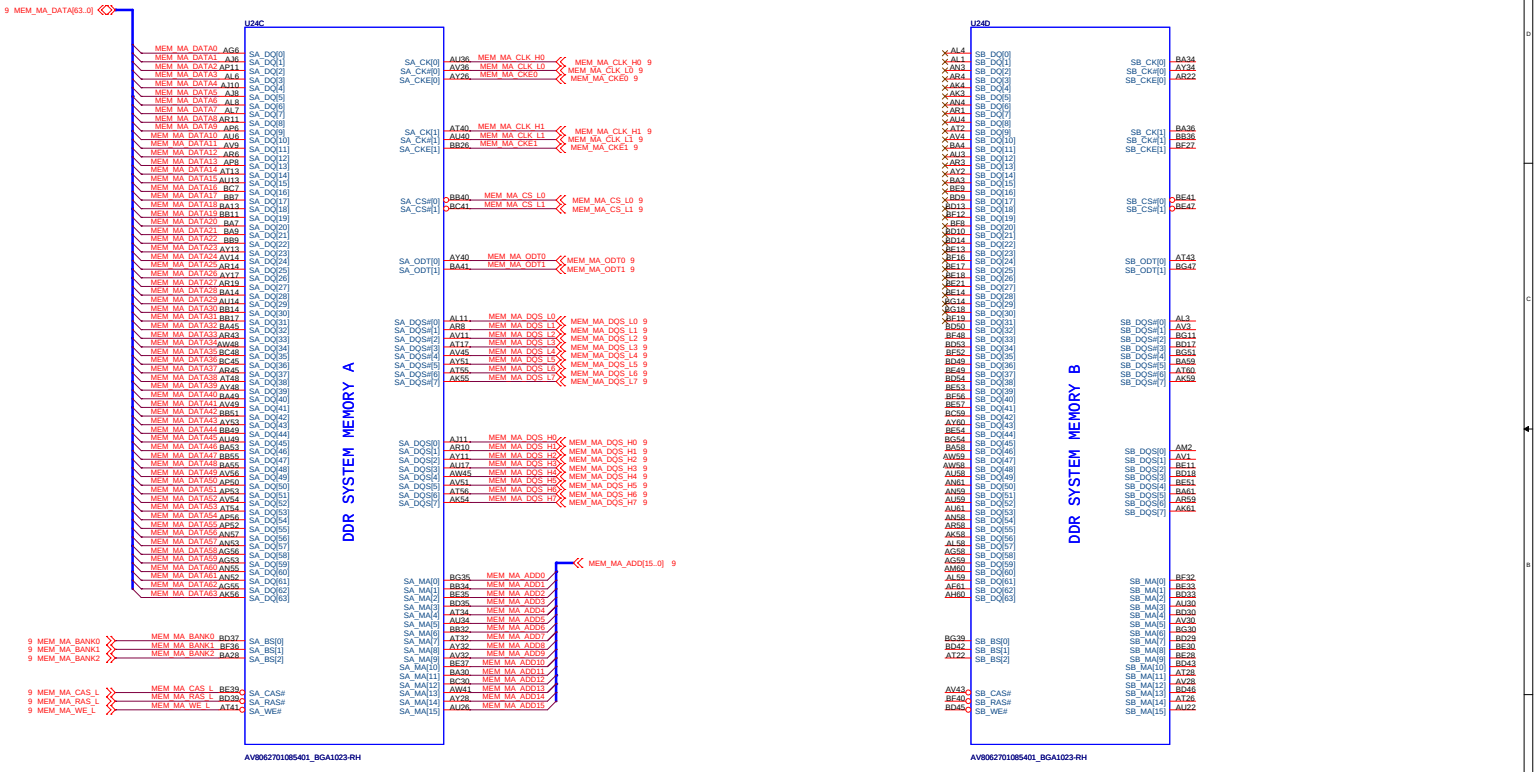








SANDY BRIDGE 2C BGA PROCESSOR (DDR3)



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Custom	PROCESSOR-2 (DDR3)	1.0

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SANDY BRIDGE 2C BGA PROCESSOR (POWER)

For SV CPU

POWER

U24F

VCCP

CORE SUPPLY

A26 VCC[1]
A29 VCC[2]
A31 VCC[3]
A34 VCC[4]
A35 VCC[5]
A38 VCC[6]
A39 VCC[7]
A42 VCC[8]
C26 VCC[9]
C27 VCC[10]
C32 VCC[11]
C34 VCC[12]
C37 VCC[13]
C39 VCC[14]
C42 VCC[15]
D27 VCC[16]
D32 VCC[17]
D34 VCC[18]
D37 VCC[19]
D39 VCC[20]
D42 VCC[21]
E26 VCC[22]
E28 VCC[23]
E32 VCC[24]
E34 VCC[25]
E37 VCC[26]
E38 VCC[27]
F25 VCC[28]
F26 VCC[29]
F28 VCC[30]
F32 VCC[31]
F34 VCC[32]
F37 VCC[33]
F39 VCC[34]
F42 VCC[35]
G42 VCC[36]
H25 VCC[37]
H26 VCC[38]
H28 VCC[39]
H29 VCC[40]
H32 VCC[41]
H34 VCC[42]
H35 VCC[43]
H37 VCC[44]
H38 VCC[45]
H40 VCC[46]
J25 VCC[47]
J26 VCC[48]
J28 VCC[49]
J29 VCC[50]
J32 VCC[51]
J34 VCC[52]
J35 VCC[53]
J37 VCC[54]
J38 VCC[55]
J40 VCC[56]
J42 VCC[57]
K26 VCC[58]
K27 VCC[59]
K29 VCC[60]
K32 VCC[61]
K34 VCC[62]
K35 VCC[63]
K37 VCC[64]
K39 VCC[65]
K42 VCC[66]
L25 VCC[67]
L28 VCC[68]
L29 VCC[69]
L33 VCC[70]
L36 VCC[71]
L40 VCC[72]
N26 VCC[73]
N30 VCC[74]
N34 VCC[75]
N38 VCC[76]

PEG IO AND DDR IO

CPU_VTT

VCCIO[1] AF46
VCCIO[3] AG48
VCCIO[4] AG50
VCCIO[5] AG51
VCCIO[6] A17
VCCIO[7] A21
VCCIO[8] AJ25
VCCIO[9] AJ43
VCCIO[10] AJ47
VCCIO[11] AK50
VCCIO[12] AK51
VCCIO[13] AL14
VCCIO[14] AL15
VCCIO[15] AL16
VCCIO[16] AL20
VCCIO[17] AL22
VCCIO[18] AL26
VCCIO[19] AL45
VCCIO[20] AL48
VCCIO[21] AM16
VCCIO[22] AM17
VCCIO[23] AM21
VCCIO[24] AM43
VCCIO[25] AM47
VCCIO[26] AN20
VCCIO[27] AN42
VCCIO[28] AN45
VCCIO[29] AN48

CPU_VTT

VCCIO[30] AA14
VCCIO[31] AA15
VCCIO[32] AB17
VCCIO[33] AB20
VCCIO[34] AC13
VCCIO[35] AD16
VCCIO[36] AD18
VCCIO[37] AD21
VCCIO[38] AE14
VCCIO[39] AE15
VCCIO[40] AF16
VCCIO[41] AF18
VCCIO[42] AF20
VCCIO[43] AG15
VCCIO[44] AG16
VCCIO[45] AG17
VCCIO[46] AG20
VCCIO[47] AG21
VCCIO[48] AJ14
VCCIO[49] AJ15

VCCIO50 W16
VCCIO51 W17

QUIET RAILS

VCCIO_SEL BC22 VCCIO_SEL TP25

CPU_VTT

VCCPQE[1] AM25
VCCPQE[2] AN22
C557 C1u6.3X50402-HF

SVID

VIDALERT# A44 VID_ALERT# R122 44.2R1%0402-RH-1
VIDSCLK B43 H_VIDSCLK_R R125 0R0402
VIDSOUT C44 H_VIDSOUT

H_VIDALERT# 35
H_VIDSCLK 35
H_VIDSOUT 35

CPU_VTT

R125 130R1%0402
R123 75R0402

C104 X_C0.01u16X0402

SENSE LINES

VCC_SENSE F43
VSS_SENSE G43

CPU_VCC_SENSE 35
CPU_VSS_SENSE 35

VCCIO_SENSE AN16
VSS_SENSE_VCCIO AN17

CPU_VTT_SENSE 33
CPU_VTT_SENSE_RTN 33

AV80627010854O1_BGA1023-RH

VCCP

C545 C544 C136 C129 C112 C122 C123 C543 C128 C135 C542 C113 C603 C604 C605

C/T/6.3X0305-HF
C22/6.3X0305-RH

Place C603,C604,C605 at the bottom of CPU.

CPU_VTT

C156 C550 C546 C552

C22/6.3X0305-RH
C/T/6.3X0305-HF

Bottom

CPU_VTT

C159 C589 C590

C22/6.3X6-HF

CPU_VTT

C608 X_C0.047u10X0402
C607
C22/6.3X6-HF

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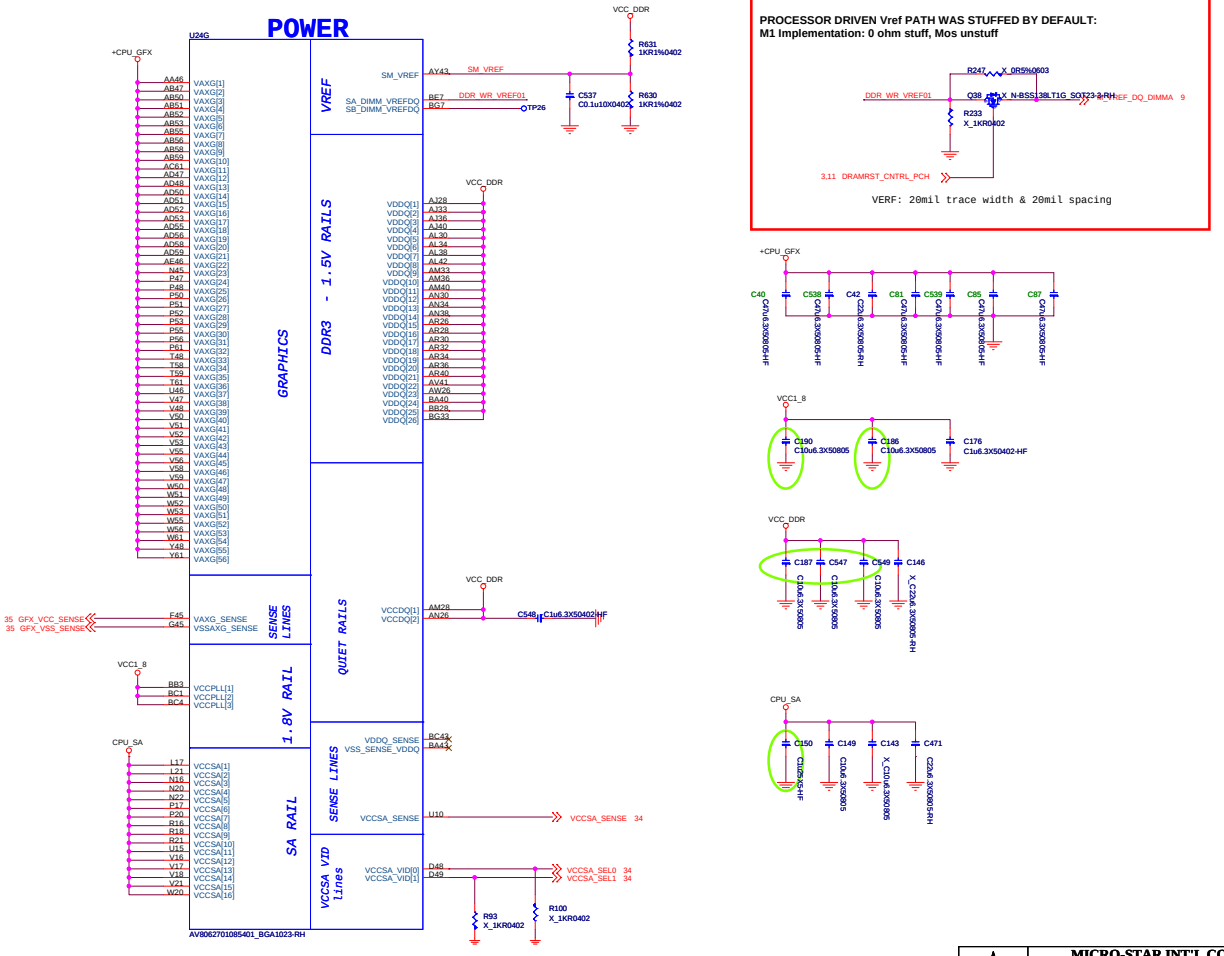
SANDY BRIDGE 2C BGA PROCESSOR (GRAPHICS POWER)



PROCESSOR DRIVEN Vref PATH WAS STUFFED BY DEFAULT:
M1 Implementation: 0 ohm stuff, Mos unstuff

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Size: Custom	Document Description: PROCESSOR-4 (GRAPHICS POWER) — Rev: 1.0
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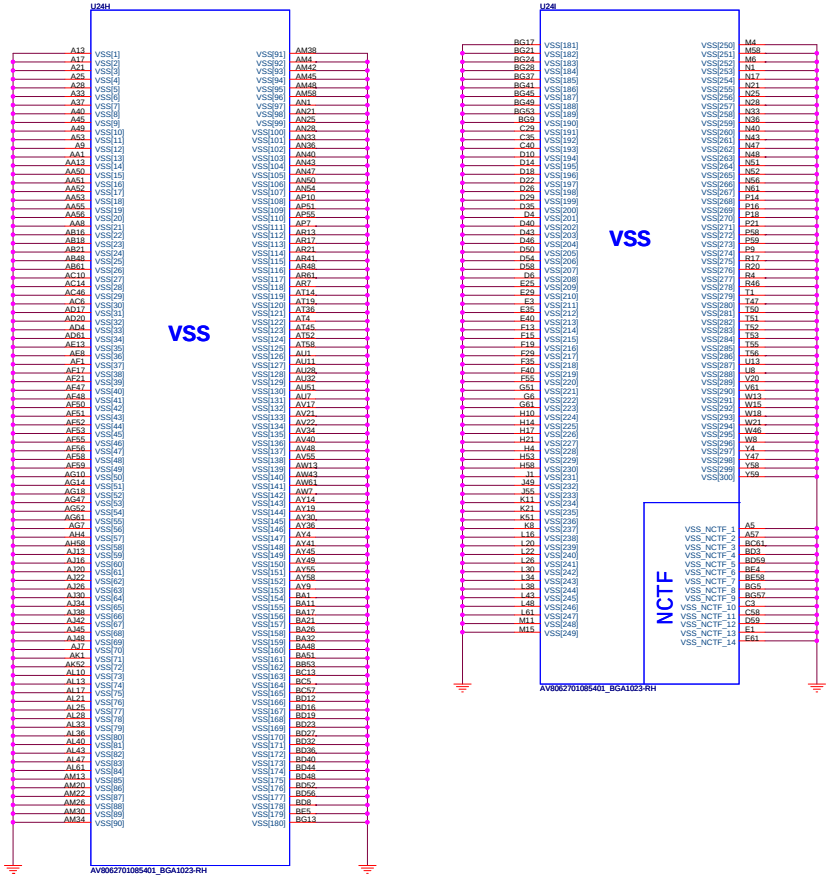
SANDY BRIDGE 2C BGA PROCESSOR (GND)



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MS-7853	
Size: Custom	Document Description: PROCESSOR-5 (GND)
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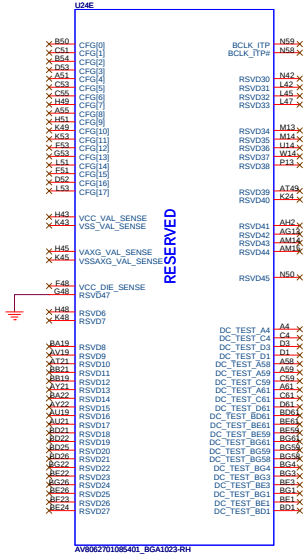
SANDY BRIDGE 2C BGA PROCESSOR (RESERVED)



CFG2 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (NC in DG) 0:Enabled; An external Display Port device is connected to the Embedded Display Port (Pull down to GND through a 1K ± 5% resistor)

PCI-Express Configuration Select	
CFG[5:6]	00 = 1 x 8, 2 x 4 PCI Express 01 = reserved 10 = 2 x 8 PCI Express 11 = 1 x 16 PCI Express (Default)

PEG DEFER TRAINING	
CFG7	1 :(Default)PEG train immediately following xxRESETB de assertion 0 :PEG wait for BIOS for training

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Size: Custom	Document Description: PROCESSOR-6 (RESERVE)	Rev: 1.0
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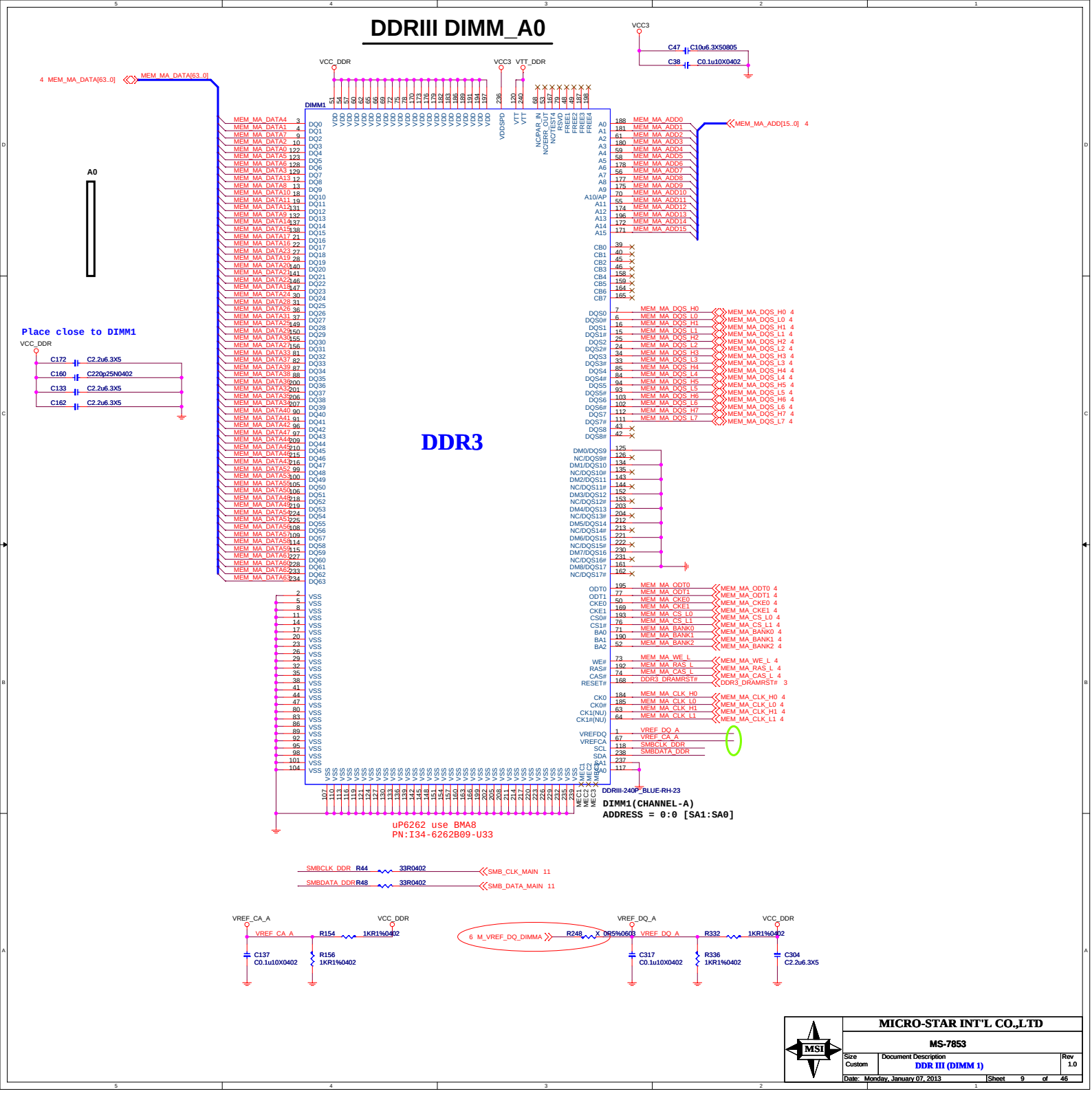
DDRIII DIMM_A0



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Size: Custom	Document Description: DDR III (DIMM 1)	Rev: 1.0
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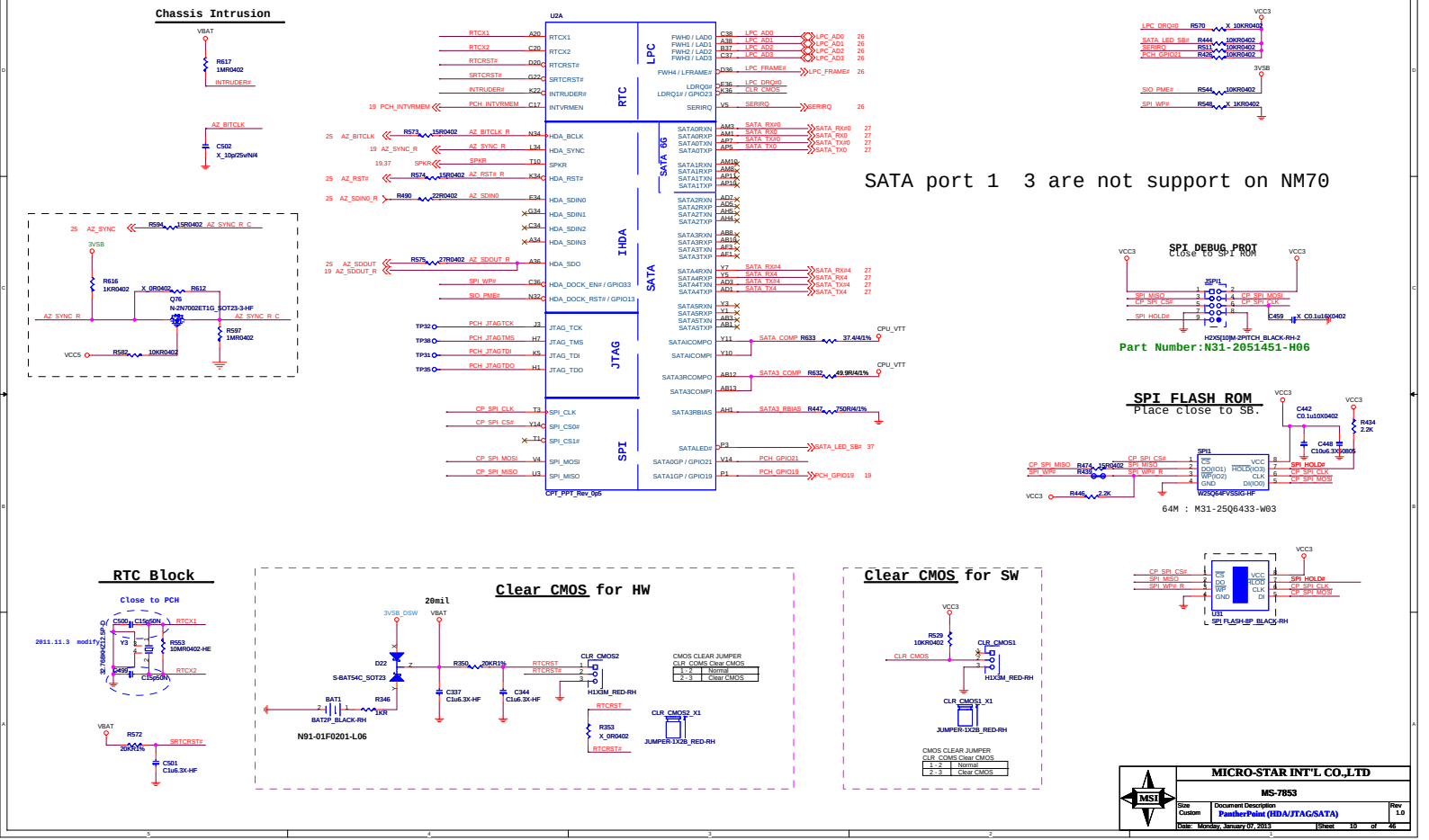
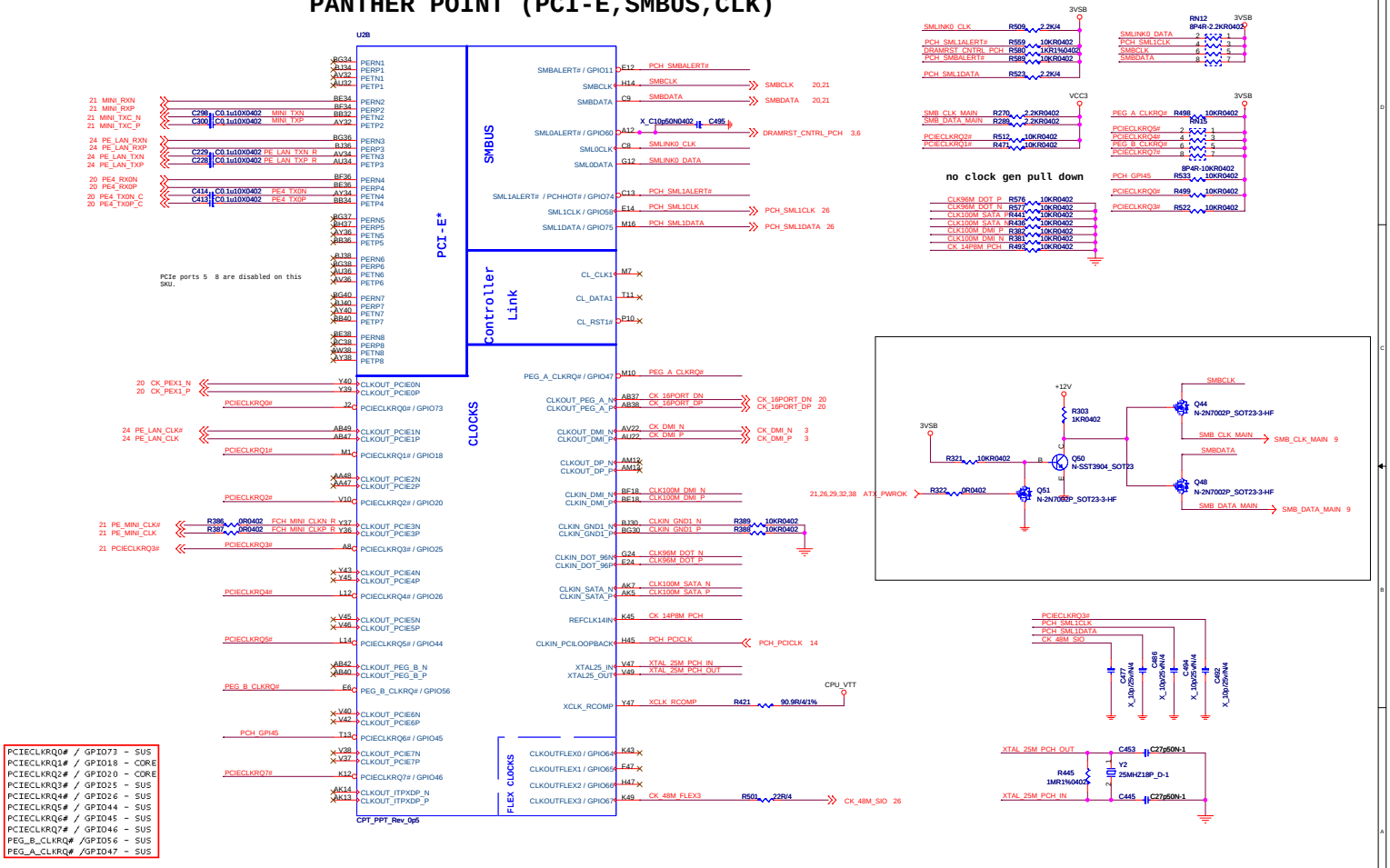
PANTHER POINT (HDA,JTAG,SATA)



PANTHER POINT (PCI-E,SMBUS,CLK)



PCIECLKRQ0# / GPIO73 - SUS
PCIECLKRQ1# / GPIO18 - CORE
PCIECLKRQ2# / GPIO20 - CORE
PCIECLKRQ3# / GPIO25 - SUS
PCIECLKRQ4# / GPIO26 - SUS
PCIECLKRQ5# / GPIO44 - SUS
PCIECLKRQ6# / GPIO45 - SUS
PCIECLKRQ7# / GPIO46 - SUS
PEG_B_CLKRQ# /GPIO56 - SUS
PEG_A_CLKRQ# /GPIO47 - SUS

Intel Comments:
If CLKREQ# control is not needed, say for a free running clock, DO NOT pull-down signal to GND. This will increase leakage in Sx states.

PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKRQx# pin on PCH with 10 k ±10% external pull-up resistor instead of No Connect.
Only PCIECLKRQ[2:1]# on PCH are core well powered. All other PCIECLKRQx# are suspend well powered.

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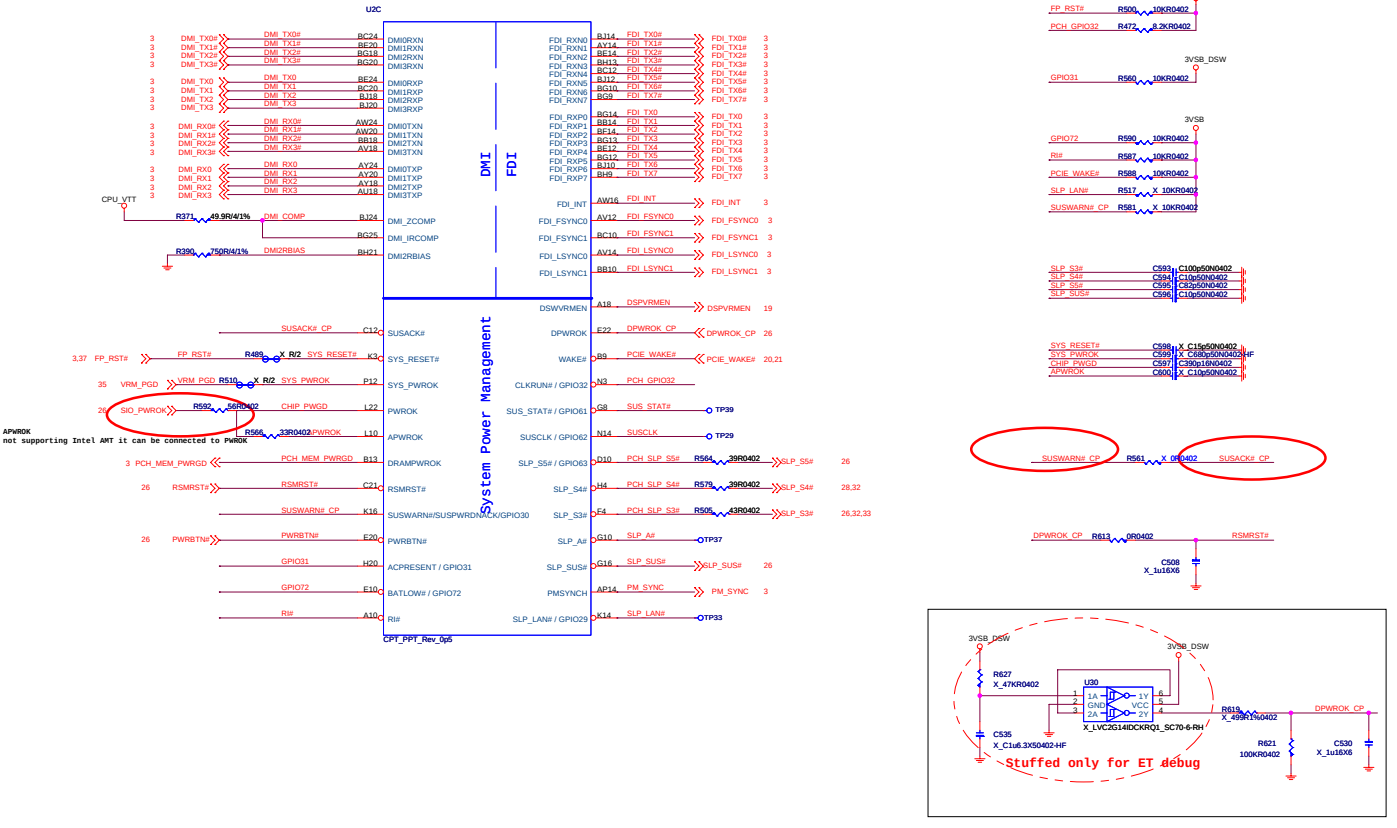
PANTHER POINT (DMI,FDI,GPIO)



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Size: Custom	Document Description: PantherPoint (DMI/FDI/GPIO)	Rev: 1.0
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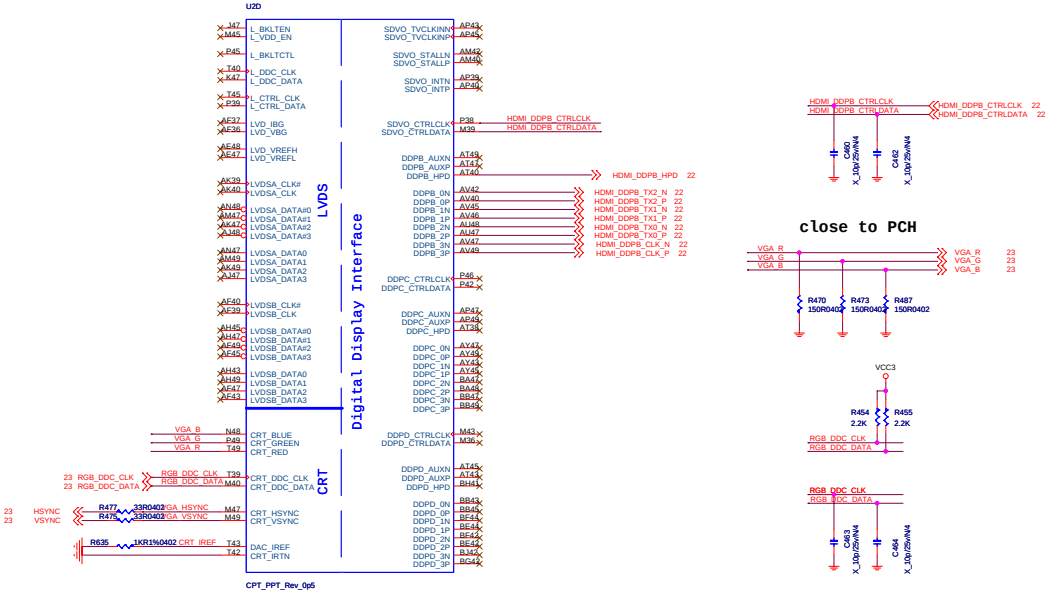
PANTHER POINT (LVDS,DDI)



close to PCH

MSI	MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PantherPoint (LVDS/DDI)		Rev: 1.0
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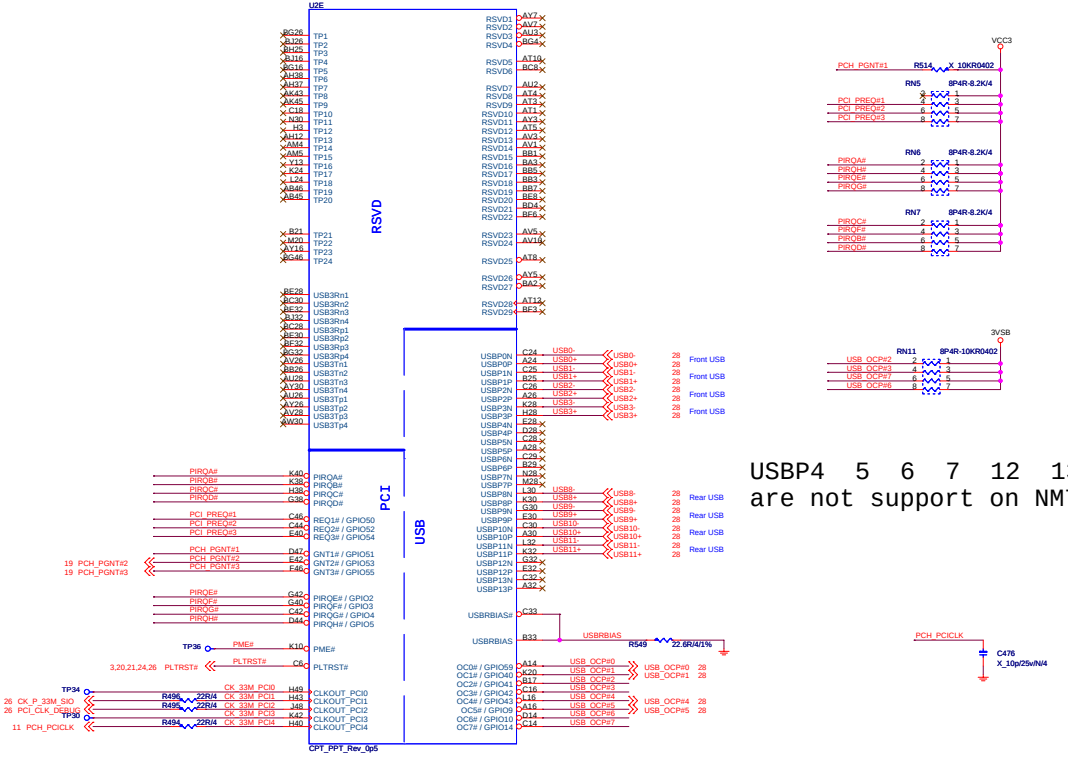
PANTHER POINT (PCI,USB,NVRAM)



USBP4 5 6 7 12 13
are not support on NM70

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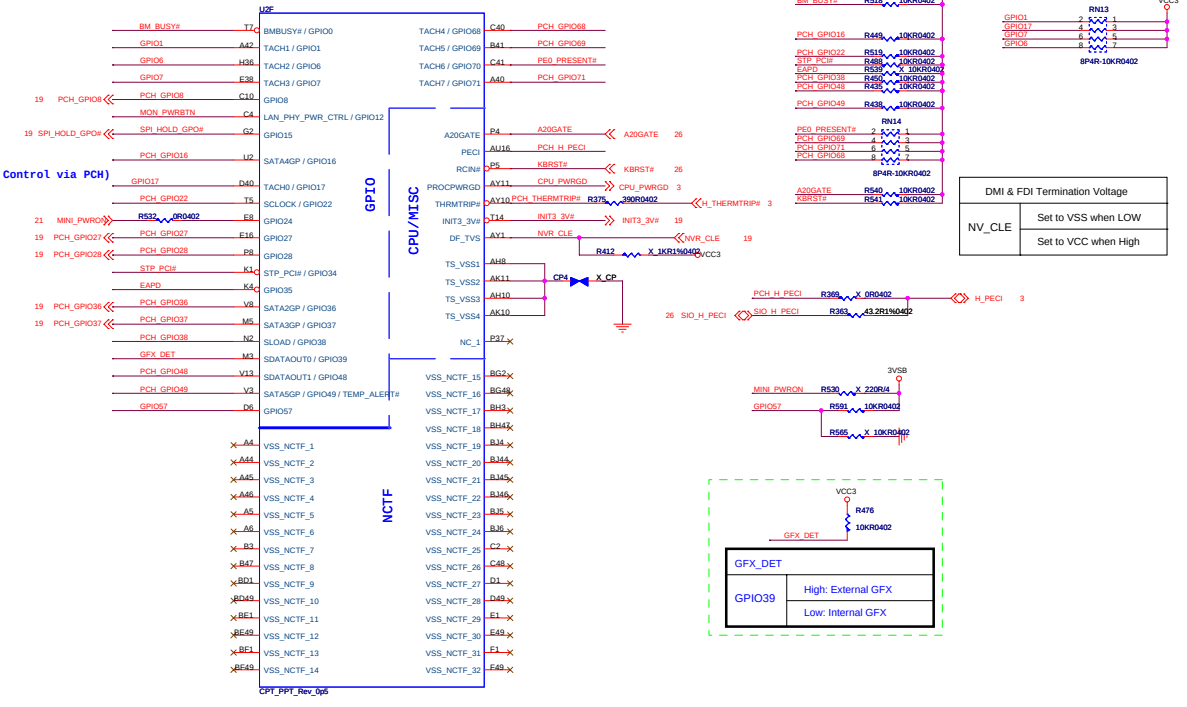
PANTHER POINT (GPIO,VSS_NCTF,RSVD)



Integrated Clock Chip Enable	
ICC_EN	High: use CK505 (buffer through mode) intelnal pull high Low: use PCH(interated clock mode)

Stuff (WLAN Control via PCH)

DMI & FDI Termination Voltage	
NV_CLE	Set to VSS when LOW
	Set to VCC when High

GFX_DET	
GPIO39	High: External GFX
	Low: Internal GFX

TLS Confidentiality	
TLSEN	Low = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
	High = Intel ME Crypto TLS cipher suite with confidentiality

GPIO0 & 6 & 16 & 17 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN

GPIO57 --If not used,require pull up 3VSUS

GPIO15--Not support AMT,Transport Layer Security Disable(High is support TLS,internal pull-down)

GPIO27 is deep S4 & S5 weak up event,internal pull high,& It's VCCFDIPLL internal VRM strapping pin

GPIO35 --Define to EDID Select (If not used,require pull down)

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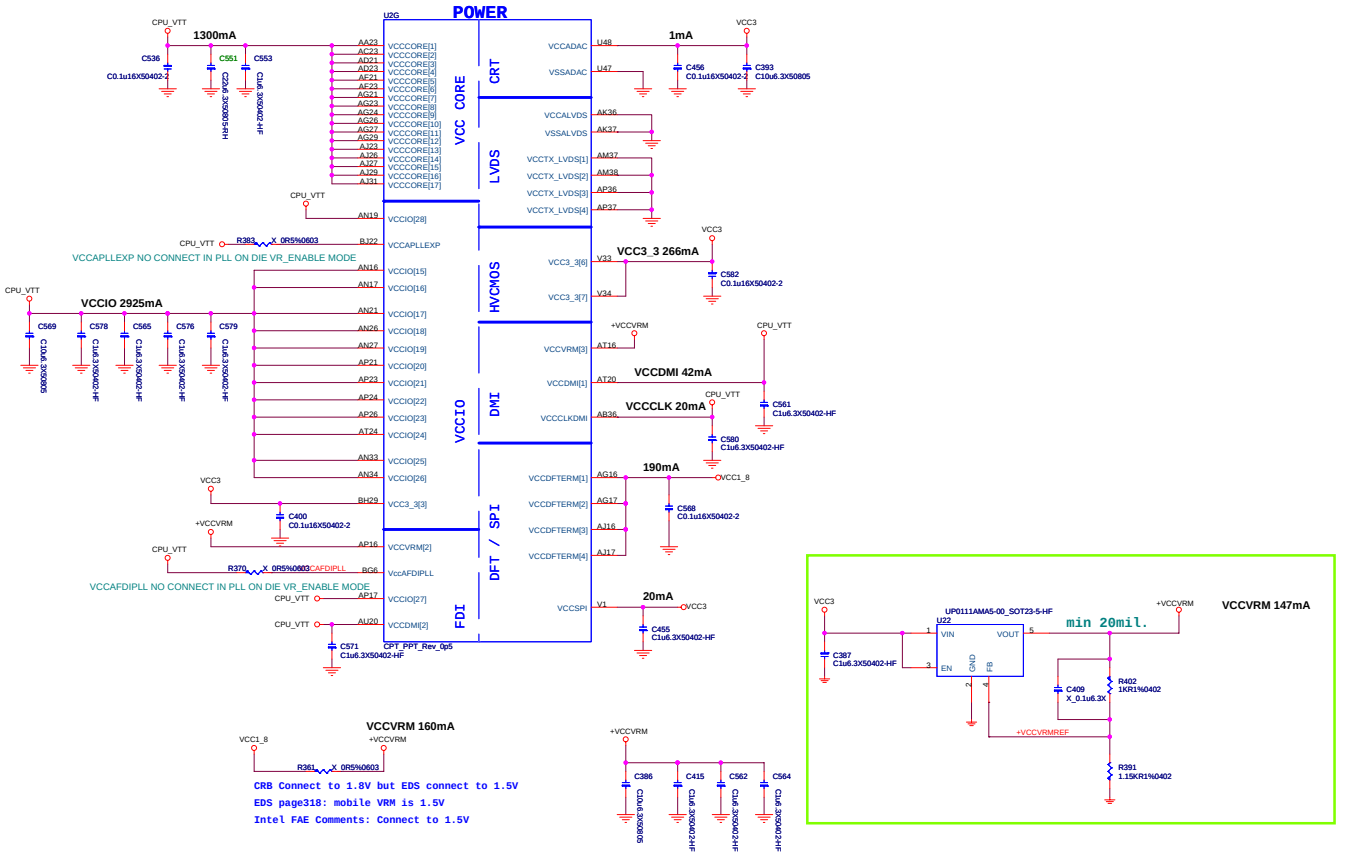
PANTHER POINT (POWER)



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PANTHER POINT (POWER)

If not support Deep SX VCCDSW3_3 can tie to 3VSB

VCCACLK NO CONNECT IN PLL ON DIE VR_ENABLE MODE

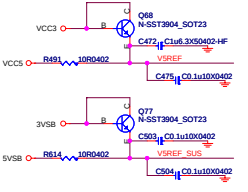
VCCAPLLDMI2 NO CONNECT IN PLL ON DIE VR_ENABLE MODE

EMI 20120326 request

VCCAPLLSATA NO CONNECT IN PLL ON DIE VR_ENABLE MODE

for ME & internal LAN use.

5VREF & 5VREF_SUS Sequencing Circuit



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PANTHER POINT (GND)

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CP REQUIRED STRAPS

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	0	1
SPI	1	1

DMI termination voltage override	
GPIO36	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

GPIO36 --CRB connector to 3V

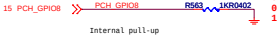
This signal has a weak internal pull-down.
NOTES:
1. The internal pull-down is disabled after PLTRST# deasserts.
2. This signal should not be pulled high when strap is sampled.

FDI termination voltage override	
GPIO37	Low-- TX,RX terminated to same vlotage (DC coupling mode)default

This signal has a weak internal pull-down.
NOTES:
1. The internal pull-down is disabled after PLTRST# deasserts.
2. This signal should not be pulled high when strap is sampled.

DMI AC/DC MODE
0 : AC
1 : DC *

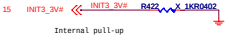
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

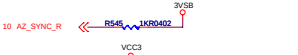
GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable



INT3_3V#

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

HDA_SDO
Disable ME in Manufacturing Mode when pull LOW

Disable ME in Manufacturing mode

1 - 2	Normal
2 - 3	ME

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY

DMI/FDI TERMINATION VOLTAGE
This signal has a weak internal pull-down.
NOTE: The internal pull-down is disabled after PLTRST# deasserts.

Internal Voltage Regulator Enable: This signal enables the internal 1.05 V regulators when pulled high.
This signal must be always pulled-up to VccRTC on desktop platform and may optionally be pulled low on mobile platforms if using an external VR for the DcpSus rail.

In Deep Sleep Power Well.

If not used,require a weak pull-up(8.2k~10k) to VccDSW3_3

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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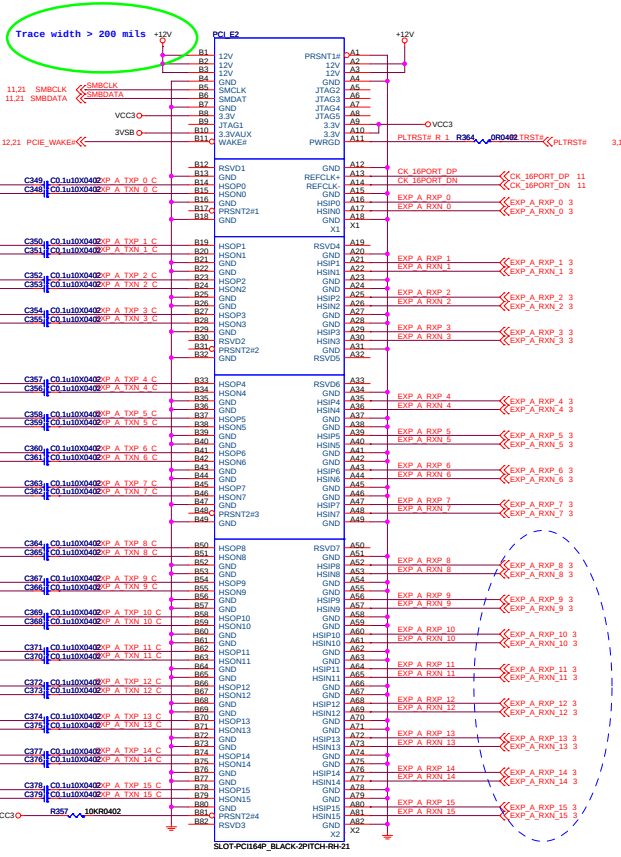
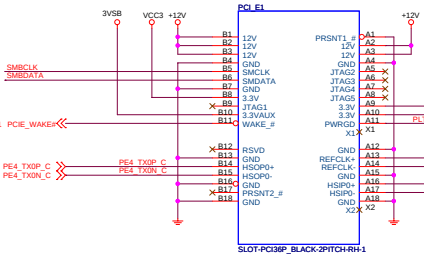
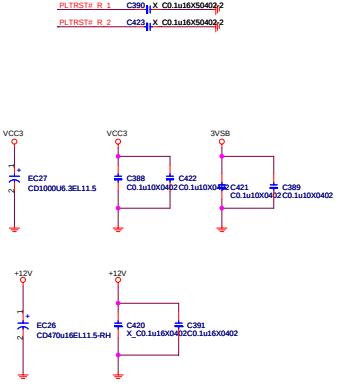
PCI_Express X16 Slot



PCI EXPRESS x1-PORT





MICRO-STAR INT'L CO.,LTD		
MS-7853		
Size: Custom	Document Description: PCIE x16/x1	Rev: 1.0
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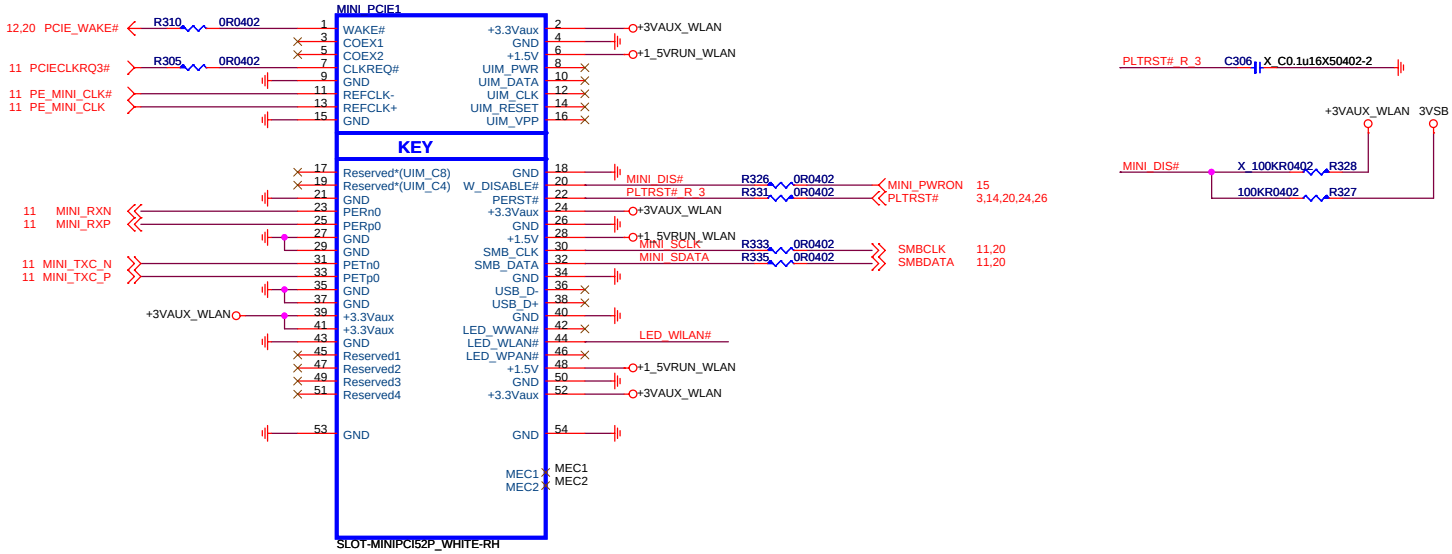

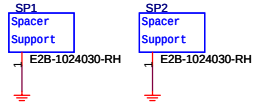

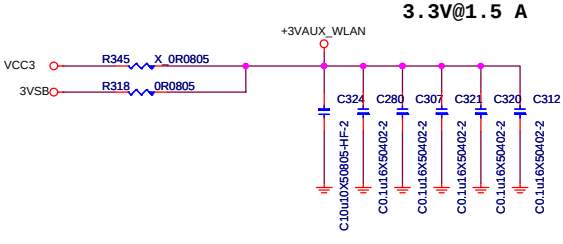

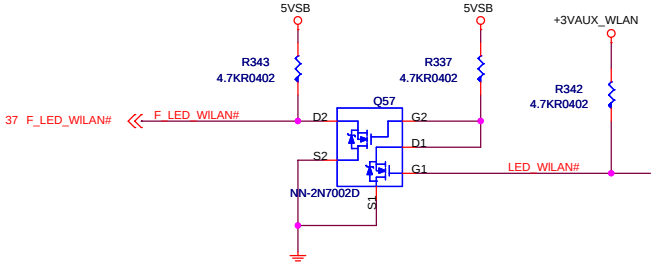

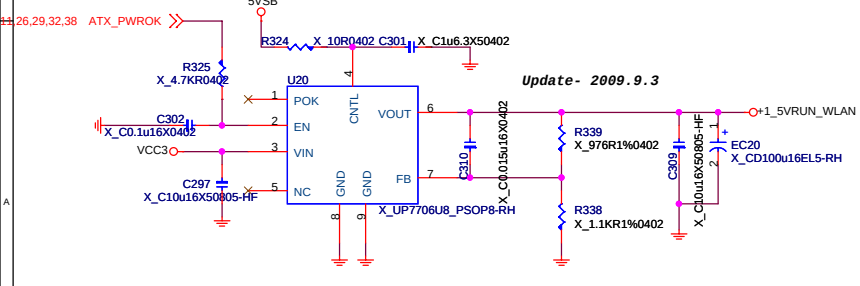

MSI MICRO-START INT'L CO.,LTD.
Link to the Future

Title	MINI PCIE SLOT	
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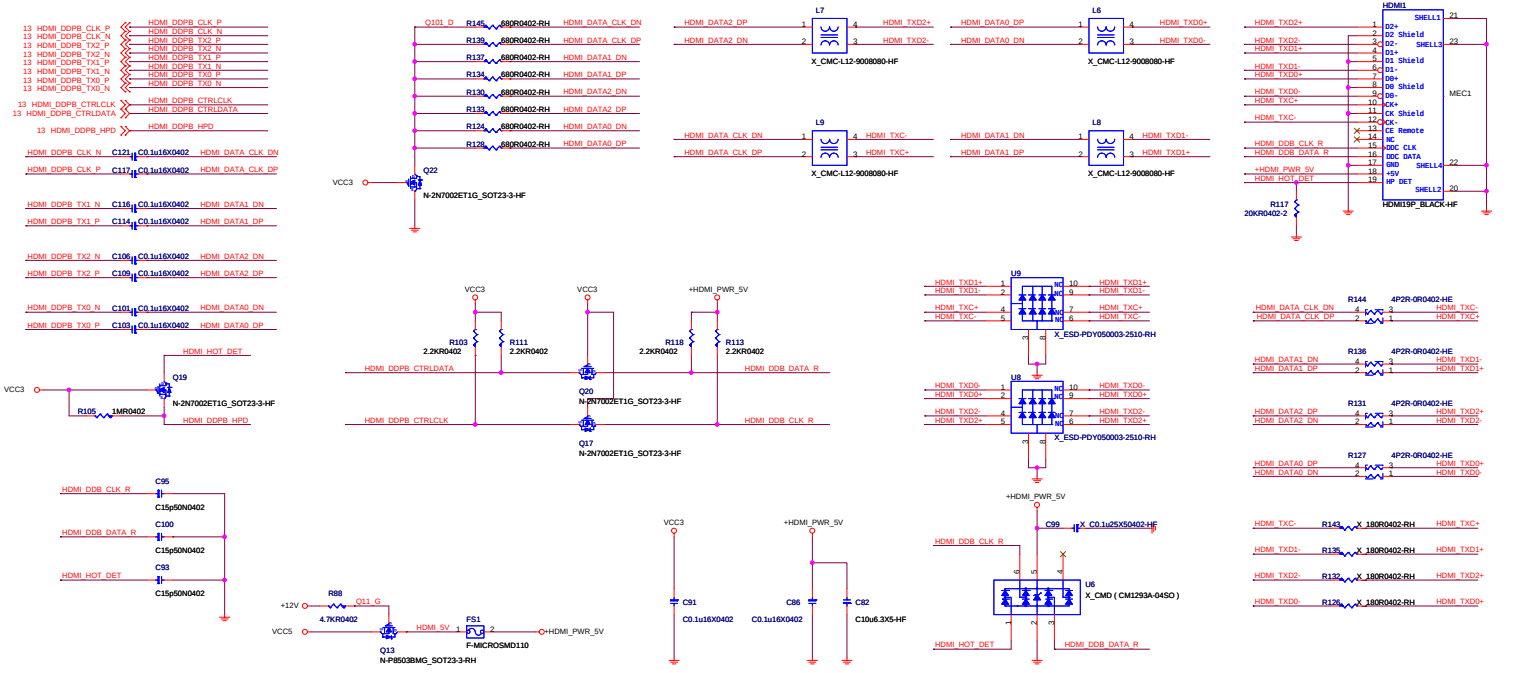
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

HDMI Port



MICRO-STAR INT'L CO.,LTD		
MS-7853		
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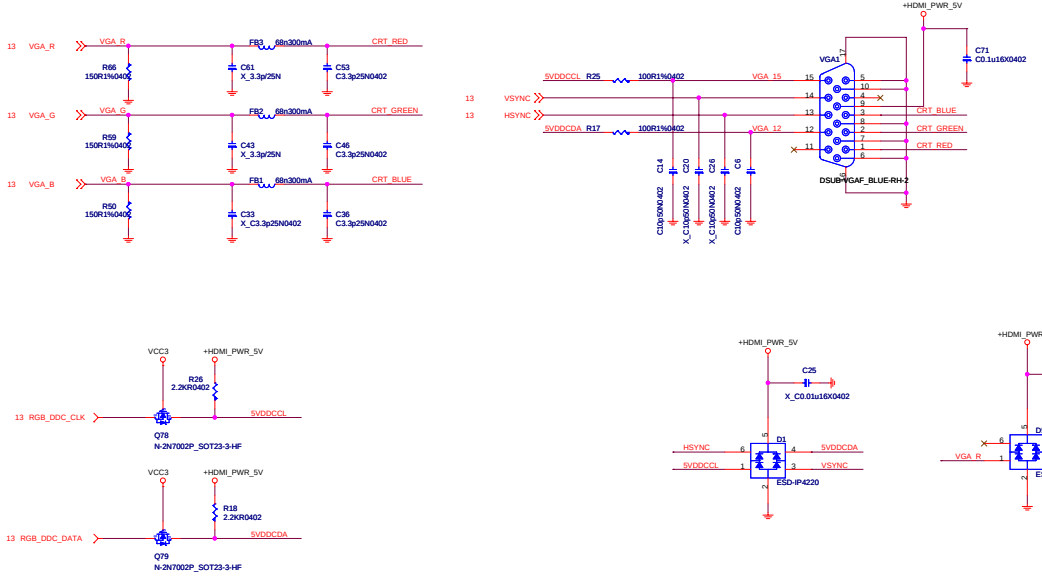
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



MICRO-STAR INT'L CO.,LTD		
MS-7853		
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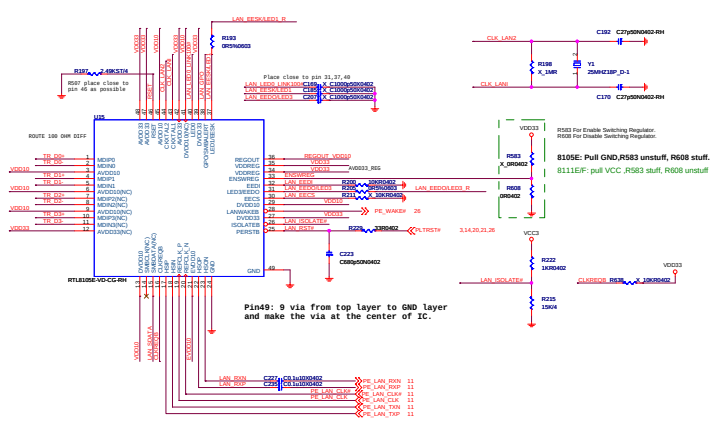
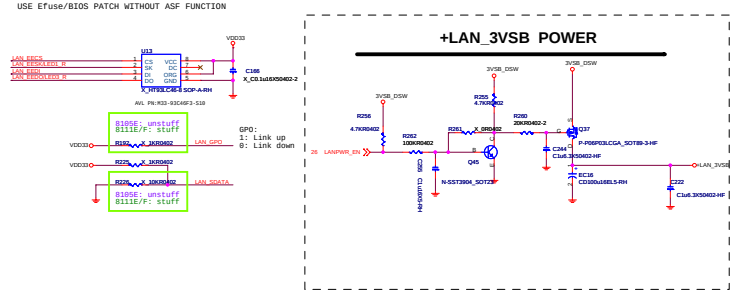
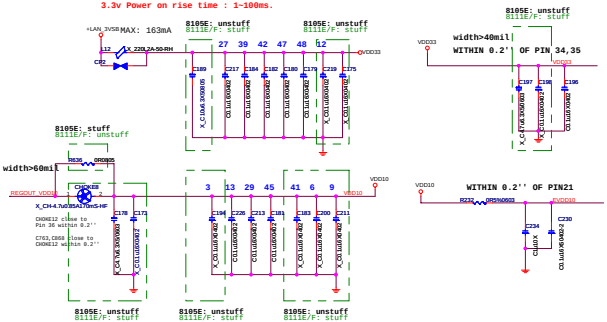
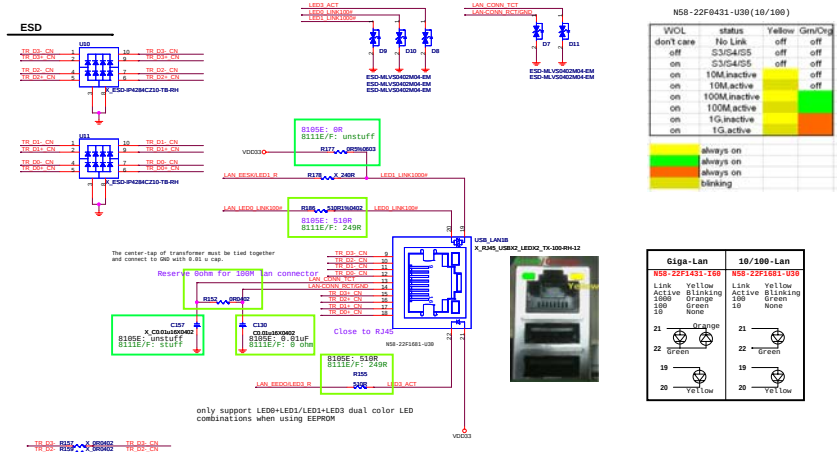
RTL8105E-VD Co-lay RTL8111F-VB Default RTL8105E-VD









N58-22F0431-U30(10/100)

WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off	S3/S4/S5	off	off
on	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

always on
always on
always on
blinking

Giga-Lan		10/100-Lan	
N58-22F1431-I60		N58-22F1681-U30	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None		

Orange
Green
Yellow

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
10 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	4527538
ALDPS	4	13

MICRO-START INT'L CO.,LTD.

Title	RTL8105E-VD Co-lay RTL8111F-VB	
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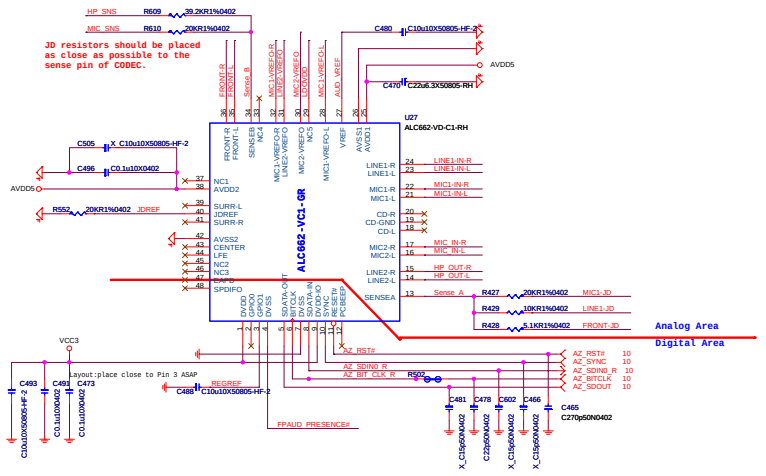
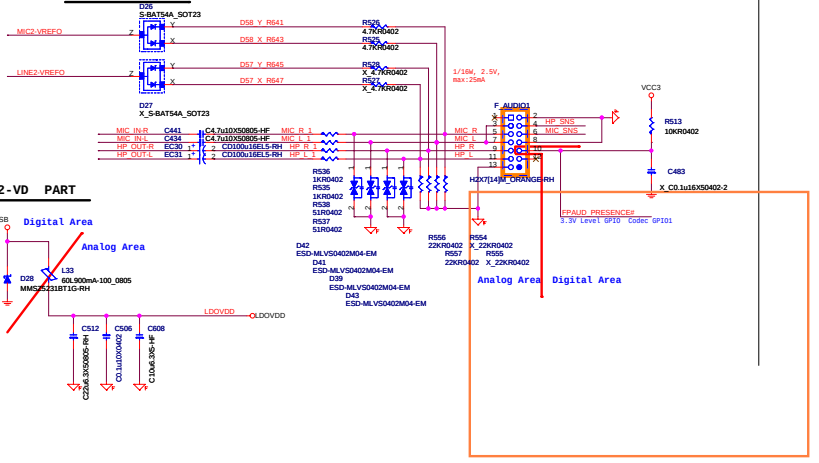
Audio Codec ALC662 VD

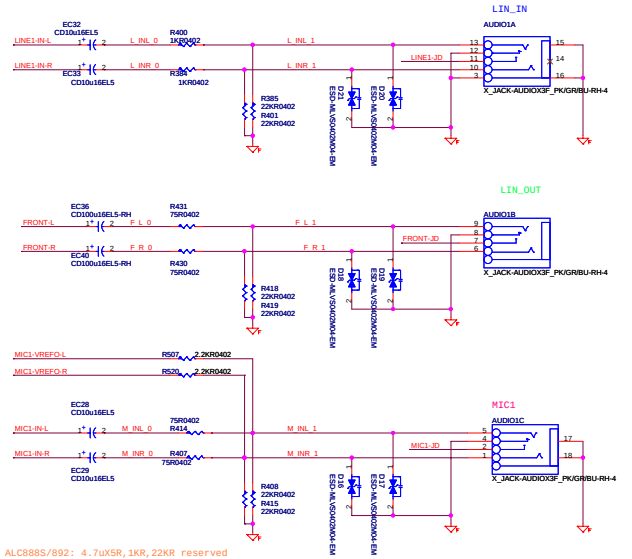


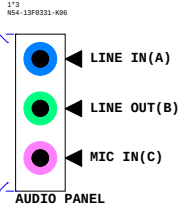
Front Audio Jack



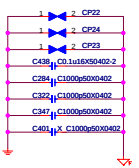
ALC662-VD PART

Rear Phone Jack 3 IN 1





Tied at one point only under the codec or near the codec



MSI Link for the Future	MICRO-START INT'L CO.,LTD.		
Title	ALC662-VD		
Size: Custom	Document Number: MS-7853		Rev: 1.0
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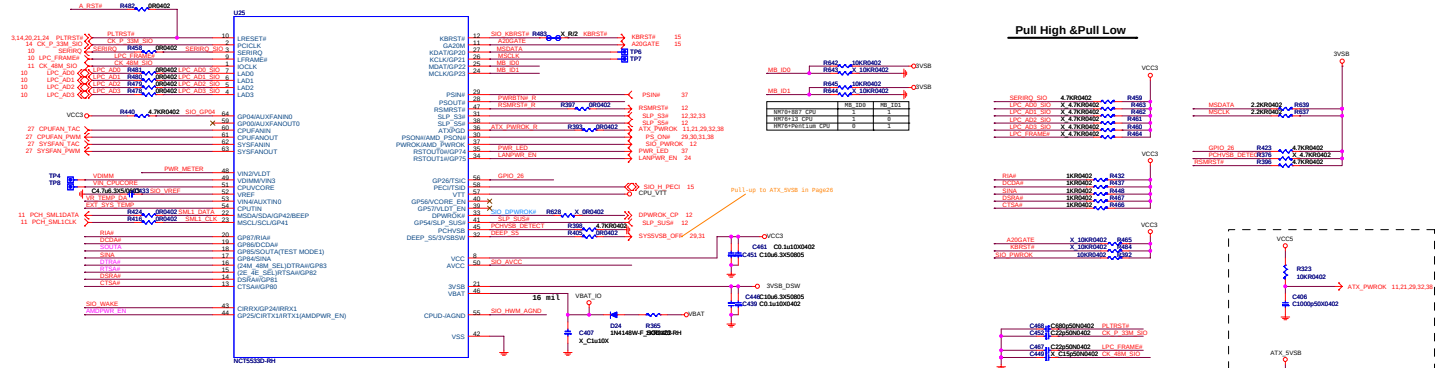
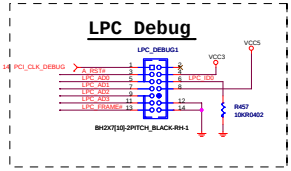
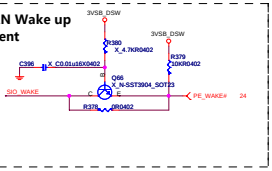


Pull High &Pull Low

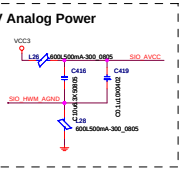
LPC Debug



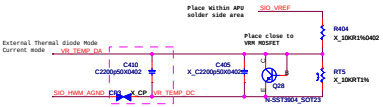
LAN Wake up event



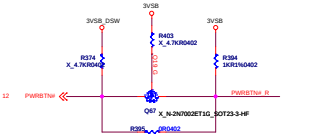
3V Analog Power



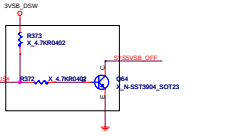
Voltage And Temp Sensing



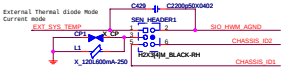
Pwrbtn# Schematic



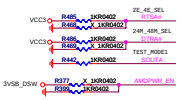
5533D DSW Support



Thermal sensor header



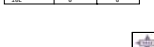
SUPER I/O STRAPPING RESISTOR



NCT5533D POWER ON STRAPPING PIN

PIN	Name	0	1	Power	Description
15	2E_4E_SEL	2E	4E	VCC	I/O Configuration Address
16	24M_48M_SEL	24MHz	48MHz	VCC	Clock Source Selection
18	TEST_MODE1	TEST MODE 1 DSISABLE	TEST MODE1 ENABLE	VSB	1K Pull Low Recommend
44	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	VSB	AMD SEQ FUNCTION

MB_ID0	MB_ID1	
NH70+887 CPU	1	1
NH70+13 CPU	1	0
NH70+Pentium CPU	0	1



CHASSIS_TYPE	CHASSIS_ID1	CHASSIS_ID2
25L DEFAULT	1	1
17L	1	0
13L	0	1
10L	0	0

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	SUPER I/O NCT5533D	
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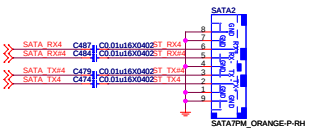
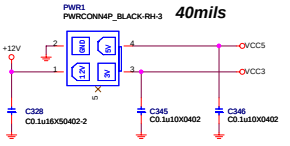
SATA 6Gb/s

NM70: SATA 6 Gb/s support on port 0 only.

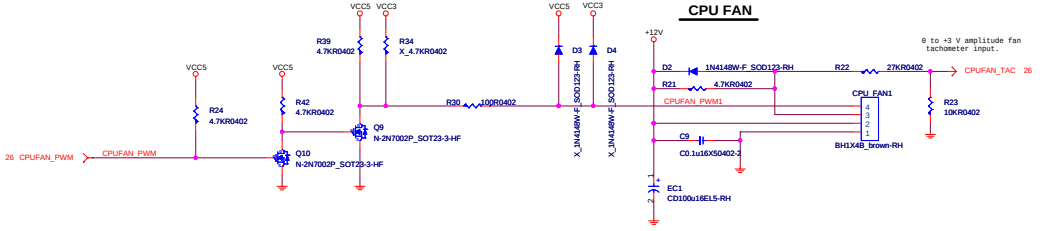
SATA 3Gb/s

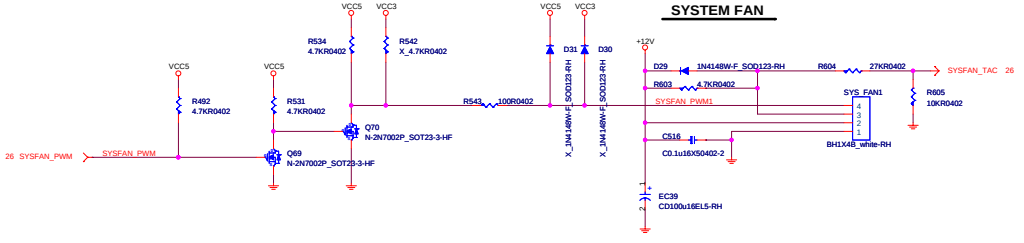


Supply power for SATA



CPU FAN and System FAN





MICRO-START INTL CO.,LTD.

Title	SATAI/eSATA/PS2/ FAN	
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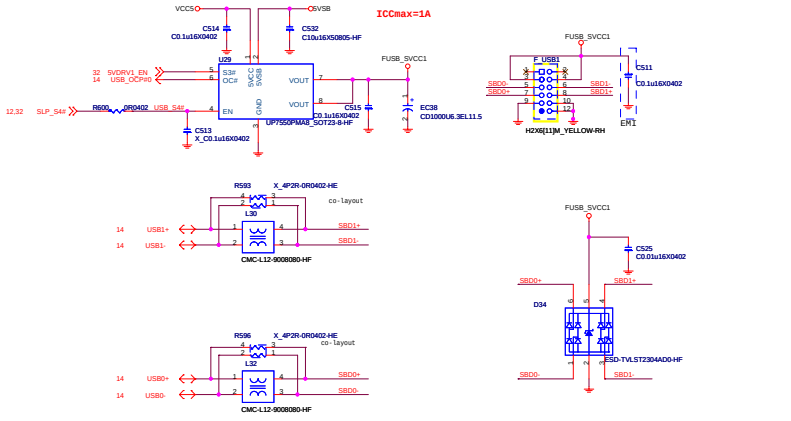
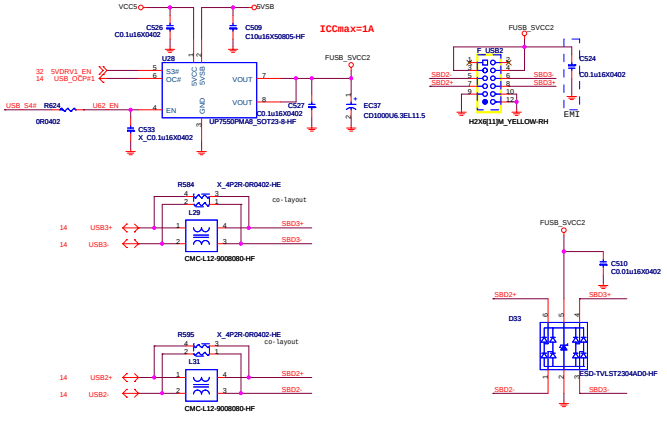
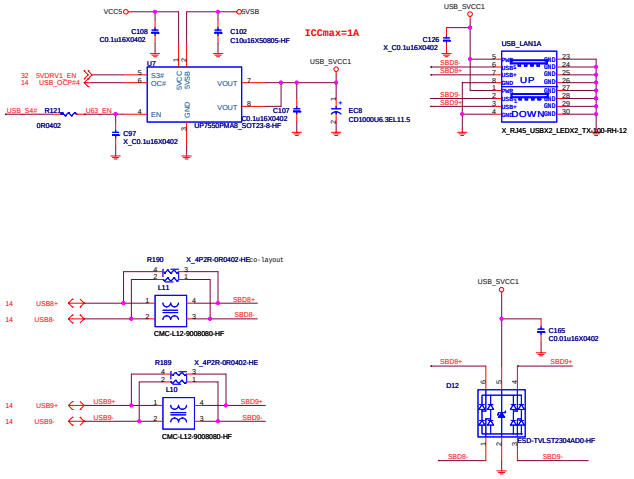
Front Panel USB Connnector For USB Port 0/ 1



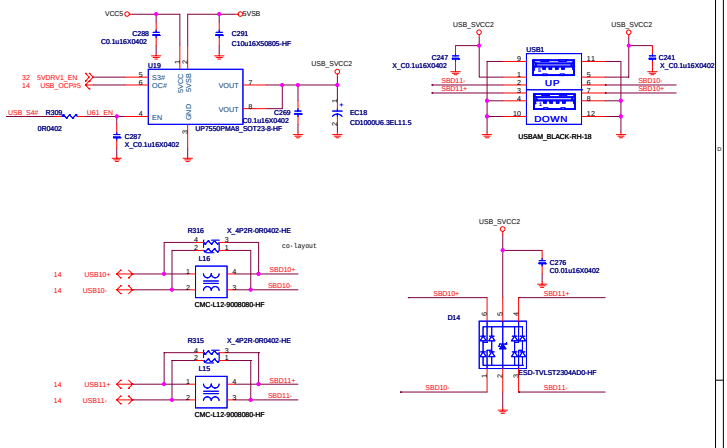
Front Panel USB Connnector For USB Port 2 / 3



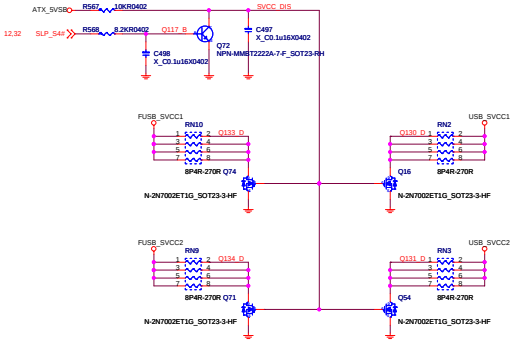
Rear USB Connnector For USB Port 8 / 9

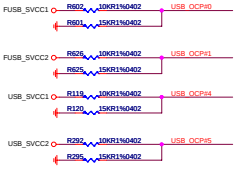


Rear USB Connnector For USB Port 10 / 11

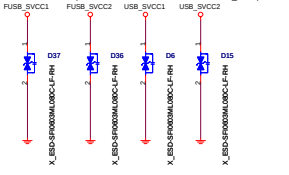


USB power discharge circuit





Lenovo Consumer MB common spec V0 2:
Must reserve ESD protection diode on USB front header 5V_Dual power.



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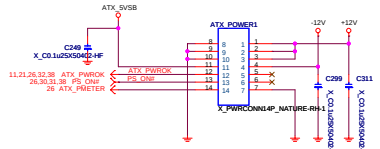
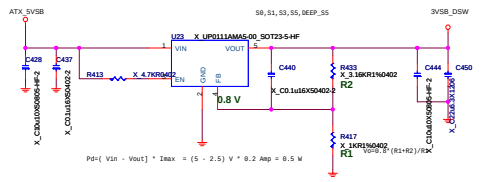
14 Pin ATX Power Connector



Single power:stuff;
DC_IN:unstuff;

3VSB_DSW



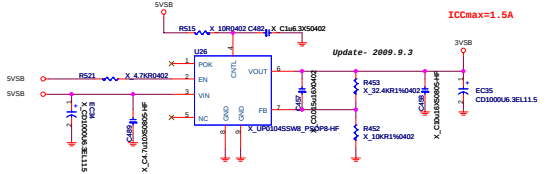
3.3V Standby Power

3.3V - 0.95A - 3.1W

Vo=0.8*(R1+R2)/R1=0.8*(10+32.4)/10=3.392 V

3.3VSB

Single power:stuff;
DC_IN:unstuff;

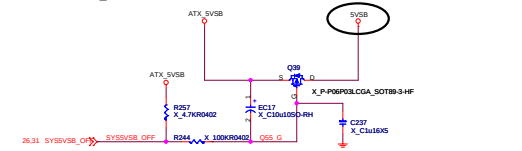


Single power:stuff;
DC_IN:unstuff;

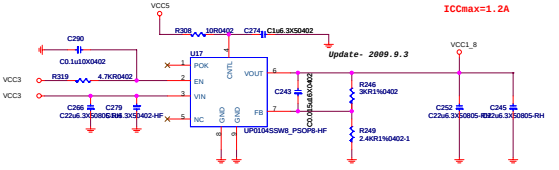
5VSB Power Switch

Tune ATX_5VSB inrush current to 2A from 4A

5VSB Trace Width 80mils



VCC1_8REF



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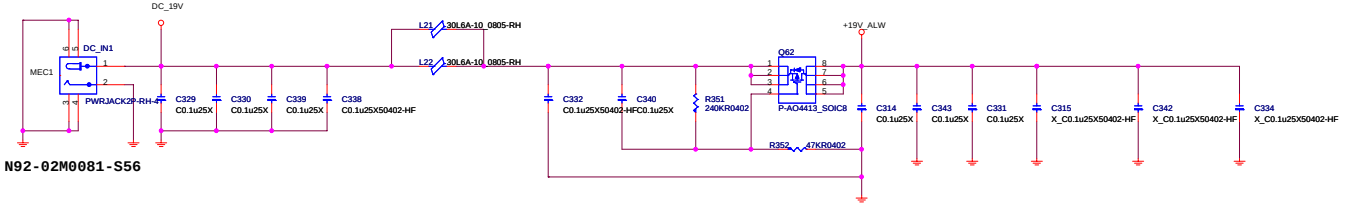
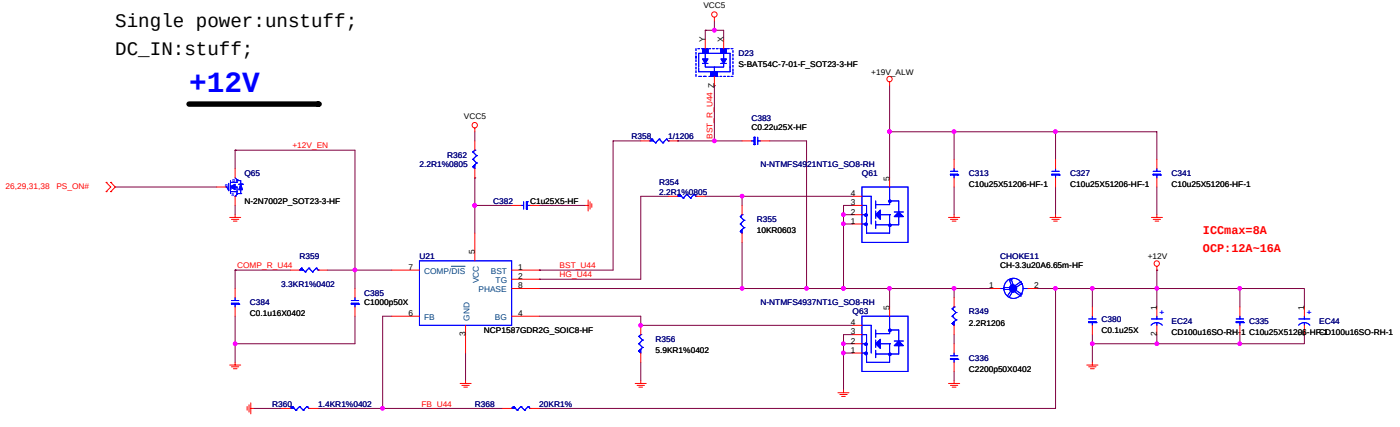
Single power:unstuff;
DC_IN:stuff;



N92-02M0081-S56

Single power:unstuff;
DC_IN:stuff;

+12V



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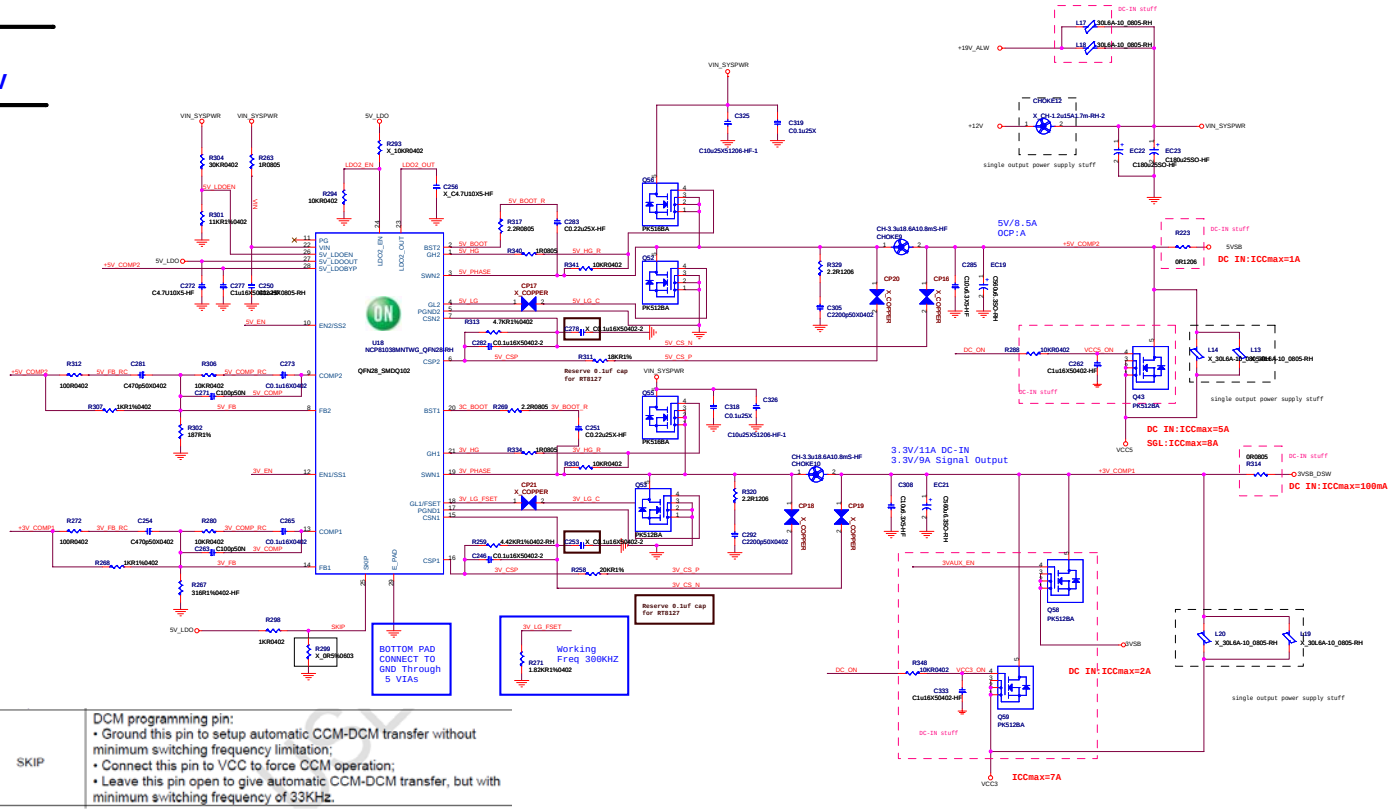
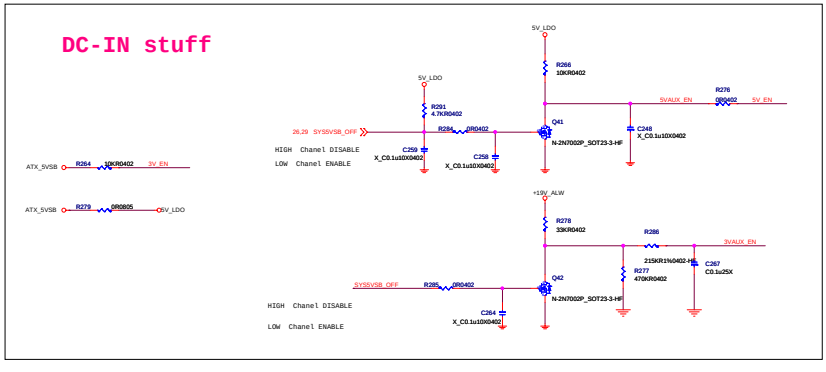
+5V

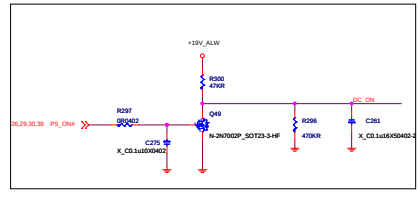
+3.3V



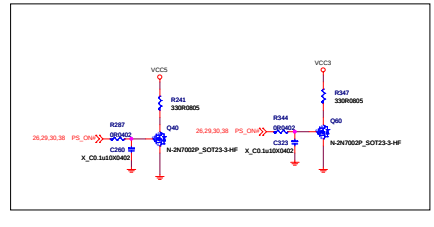
SKIP	DCM programming pin: • Ground this pin to setup automatic CCM-DCM transfer without minimum switching frequency limitation; • Connect this pin to VCC to force CCM operation; • Leave this pin open to give automatic CCM-DCM transfer, but with minimum switching frequency of 33KHz.

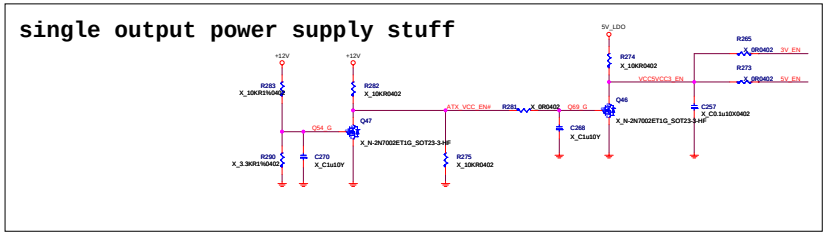
VCC3&VCC5 Power Enable





Discharge





MICRO-STAR INT'L CO.,LTD		
MS-7853		
Size: Custom	Document Description: USB Connector	Rev: 1.0
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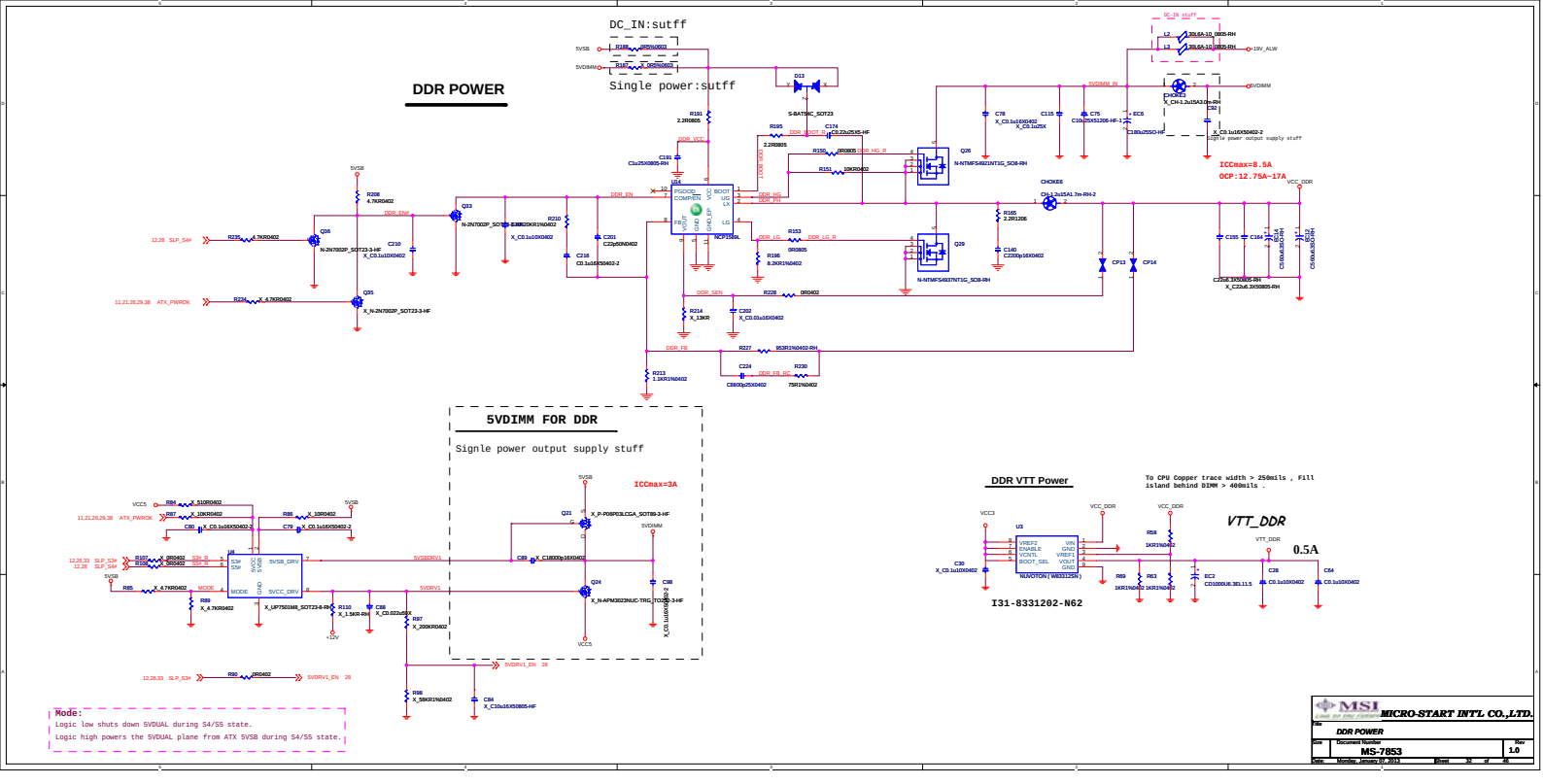
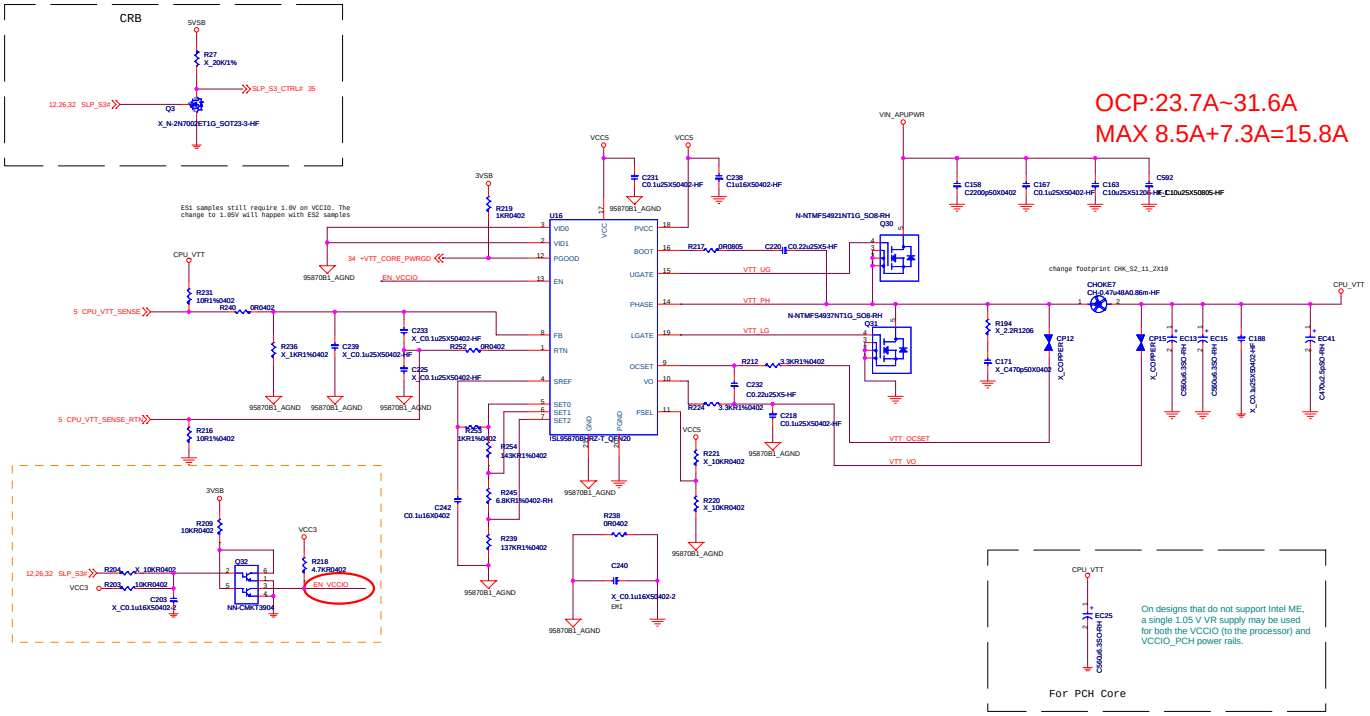

DDR POWER
DC_IN:sutff
Single power:sutff
ICCmax=8.5A
OCP:12.75A~17A
5VDIMM FOR DDR
Signle power output supply stuff
ICCmax=3A
DDR VTT Power
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .
VTT_DDR
0.5A
I31-8331202-N62
Mode:
Logic low shuts down 5VDUAL during S4/S5 state.
Logic high powers the 5VDUAL plane from ATX 5VSB during S4/S5 state.
MICRO-STAR INTL CO.,LTD.
DDR POWER
MS-7853
1.0

CPU_VTT:1.05V



MSI	MICRO-STAR INT'L CO.,LTD		
	MS-7853		
Size: C	Document Description: CPU_VTT - ISL95870 1-Phase		Rev: 1.0
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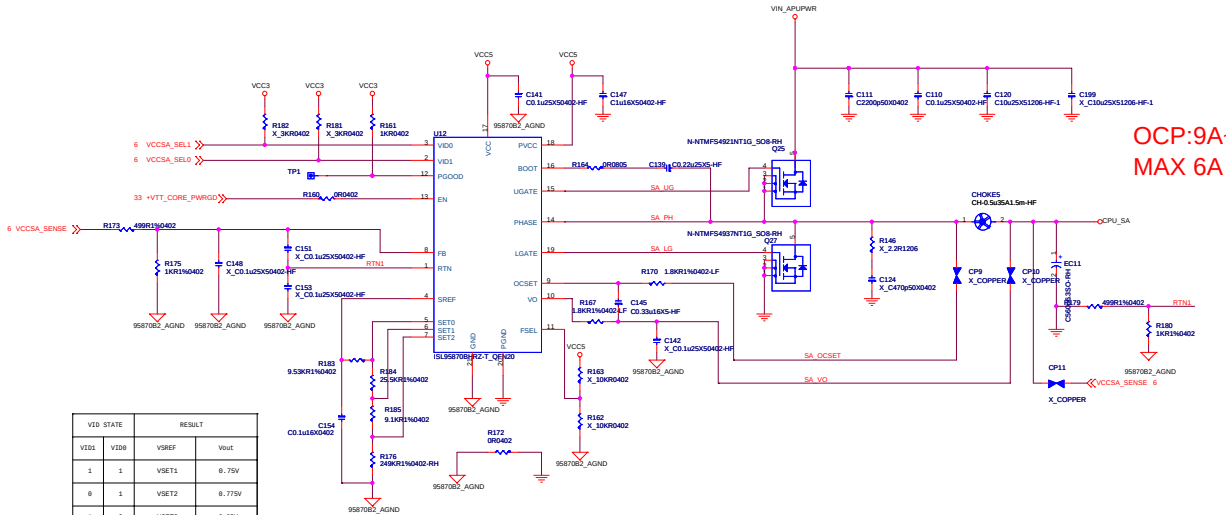
CPU_SA



VID STATE		RESULT	
VID1	VID0	VSREF	Vout
1	1	VSET1	0.75V
0	1	VSET2	0.775V
1	0	VSET3	0.85V
0	0	VSET4	0.9V

MICRO-STAR INT'L CO.,LTD		
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Size: C	Document Description: CPU_SA - OP+MOS	Rev: 1.0
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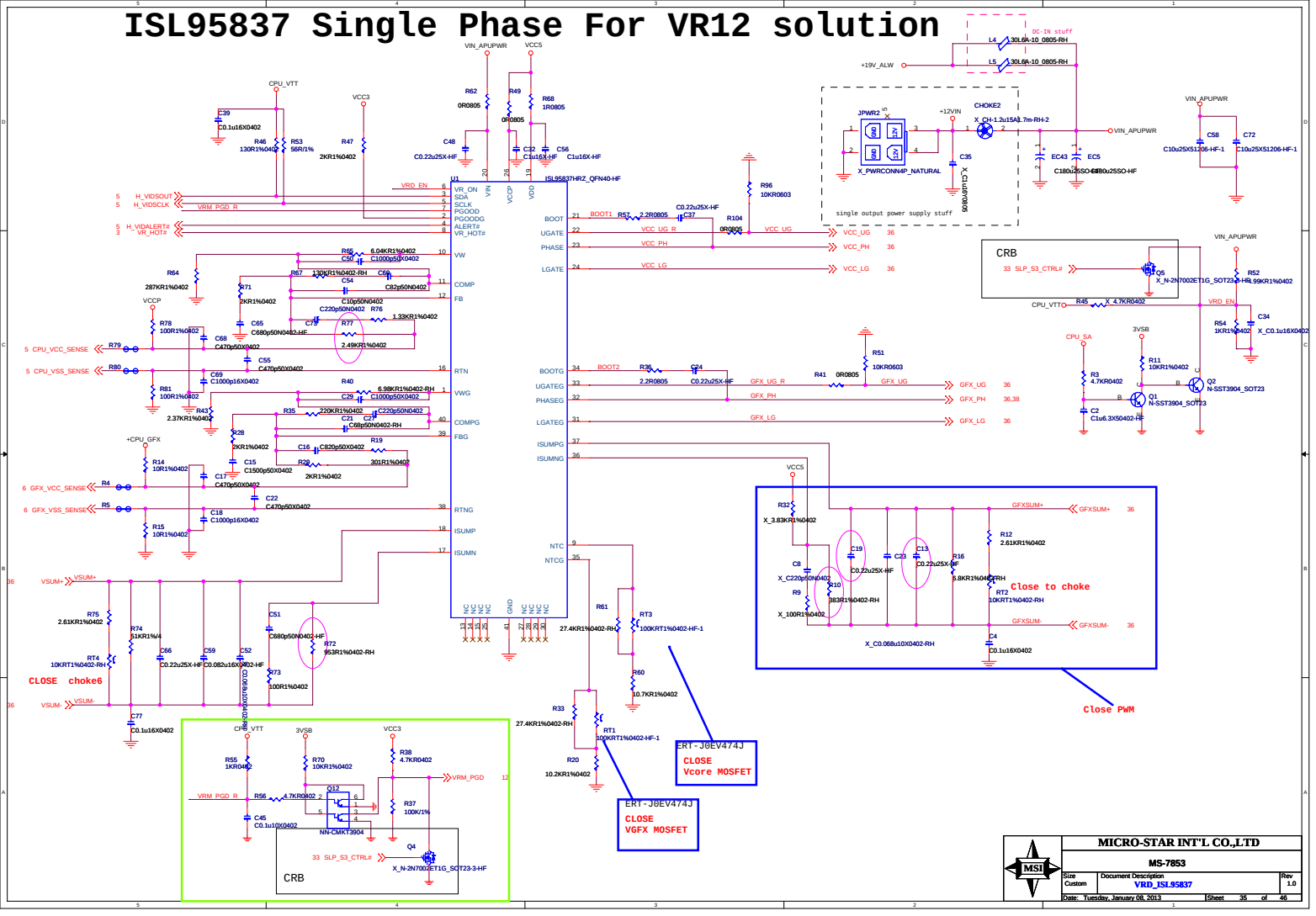
ISL95837 Single Phase For VR12 solution



MICRO-STAR INT'L CO.,LTD	
MS-7853	
Size: Custom	Document Description: VRD_ISL95837
Rev: 1.0	
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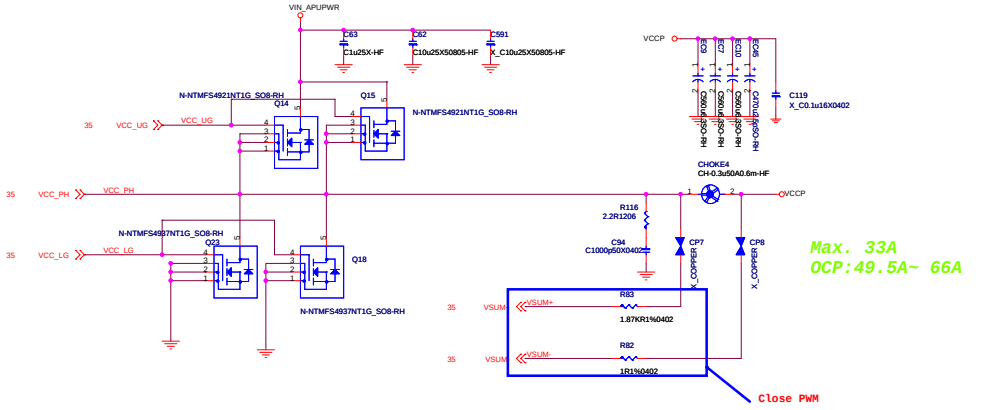

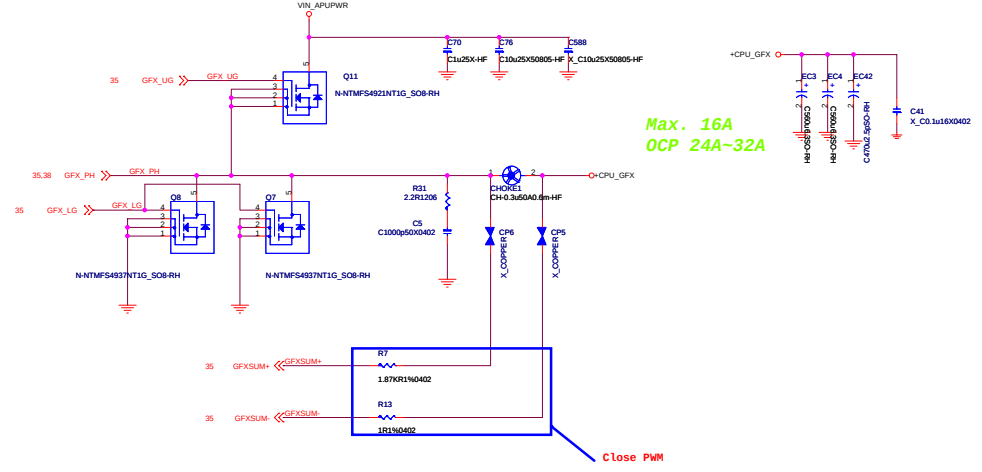

MICRO-STAR INT'L CO.,LTD		
MS-7853		
Size: Custom	Document Description: VCCP & GFX MOS CHOKE CAP	Rev: 1.0
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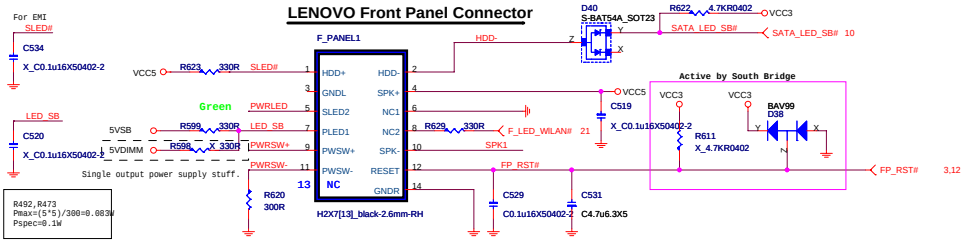
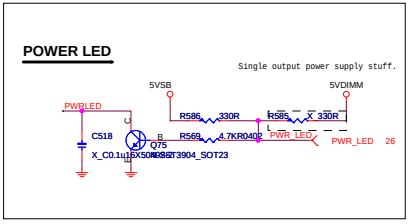
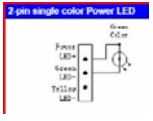
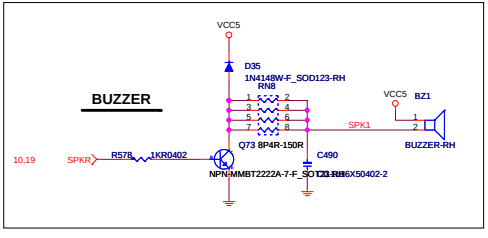


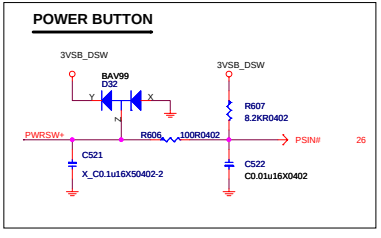


power LED definition

LED Status (Dual color LED)	
System State	Dual Color POWER LED State
S0	Steady Green
S1	Green Blanking (frequency is under 1Hz)
S3	Steady Yellow
S4/S5	Off
Default S5 in lose power	Vista series revision is 1Hz







MSI Link to the Future	MICRO-START INT'L CO.,LTD.		
Title	DC-IN&Front Panel		
Size	Document Number MS-7853		Rev 1.0
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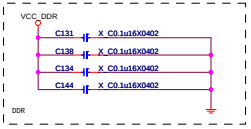
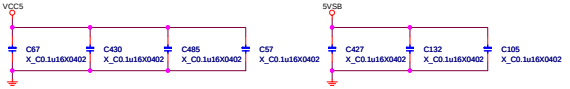
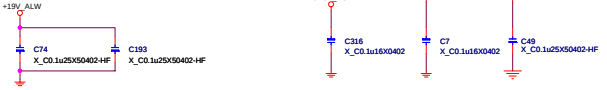
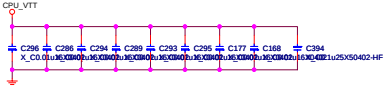
EMI

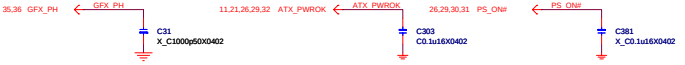


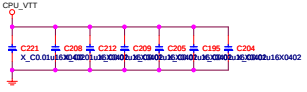


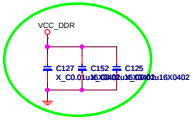


For PCIE 16X & FDI DMI Lanes reference not continuous









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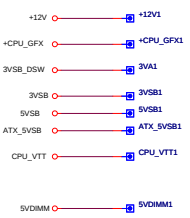
MS-7853-0A

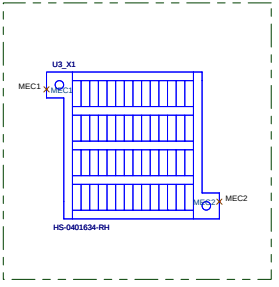
OPT	Configure	BOM	Function

Voltage test point

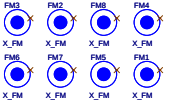


Simulation

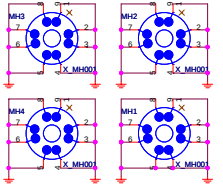
MANUAL PART

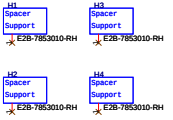


Optical Fiducial Marks-120



Mounting Holes





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Size: Custom	Document Description: XDP / Manual Parts	Rev: 1.0
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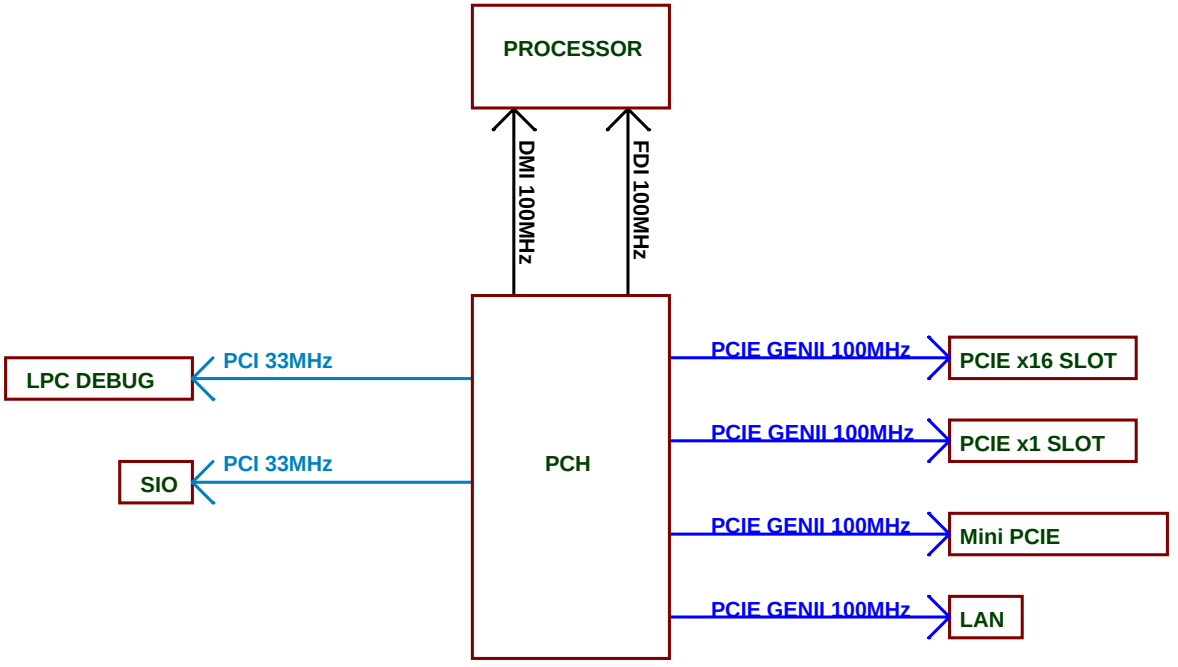

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Size B	Document Number <Doc>	Rev 1.0
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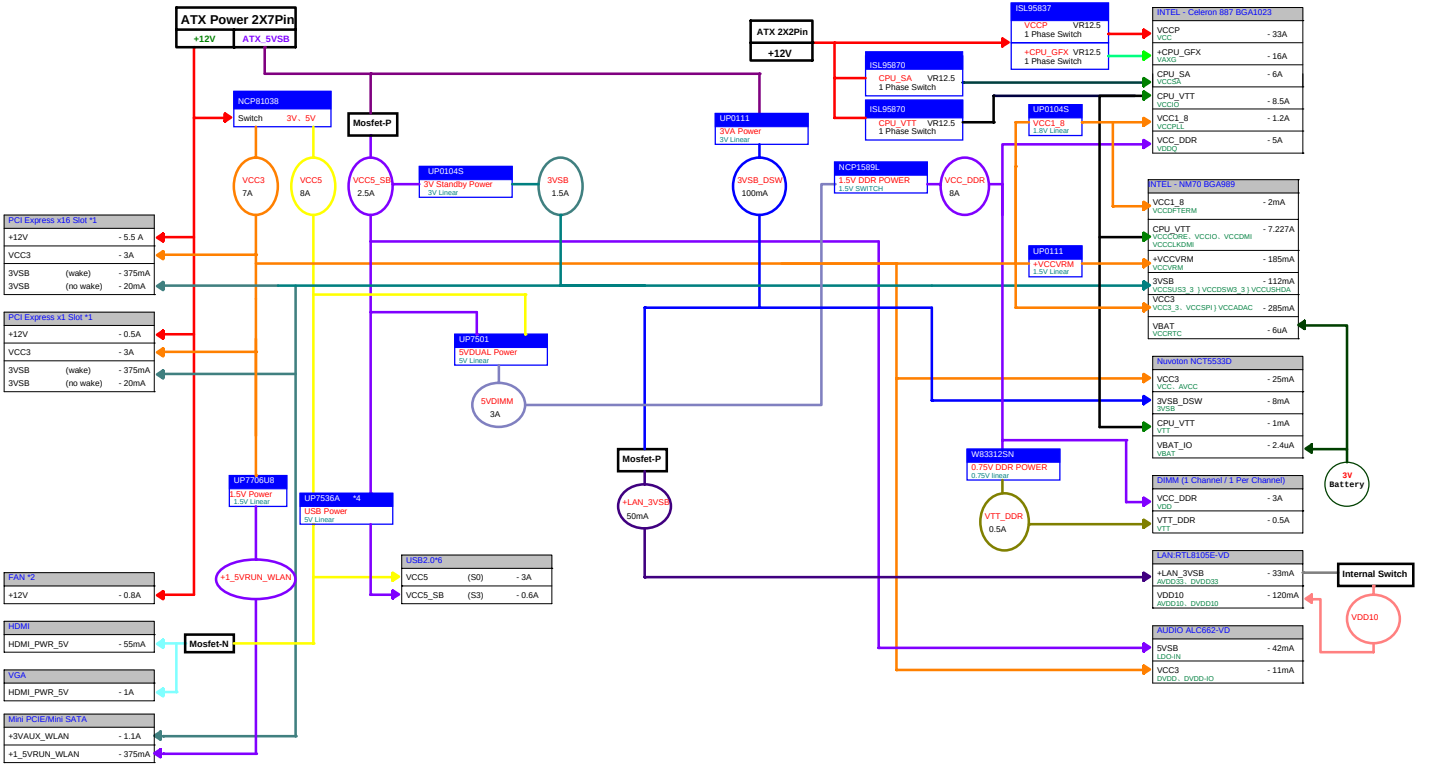
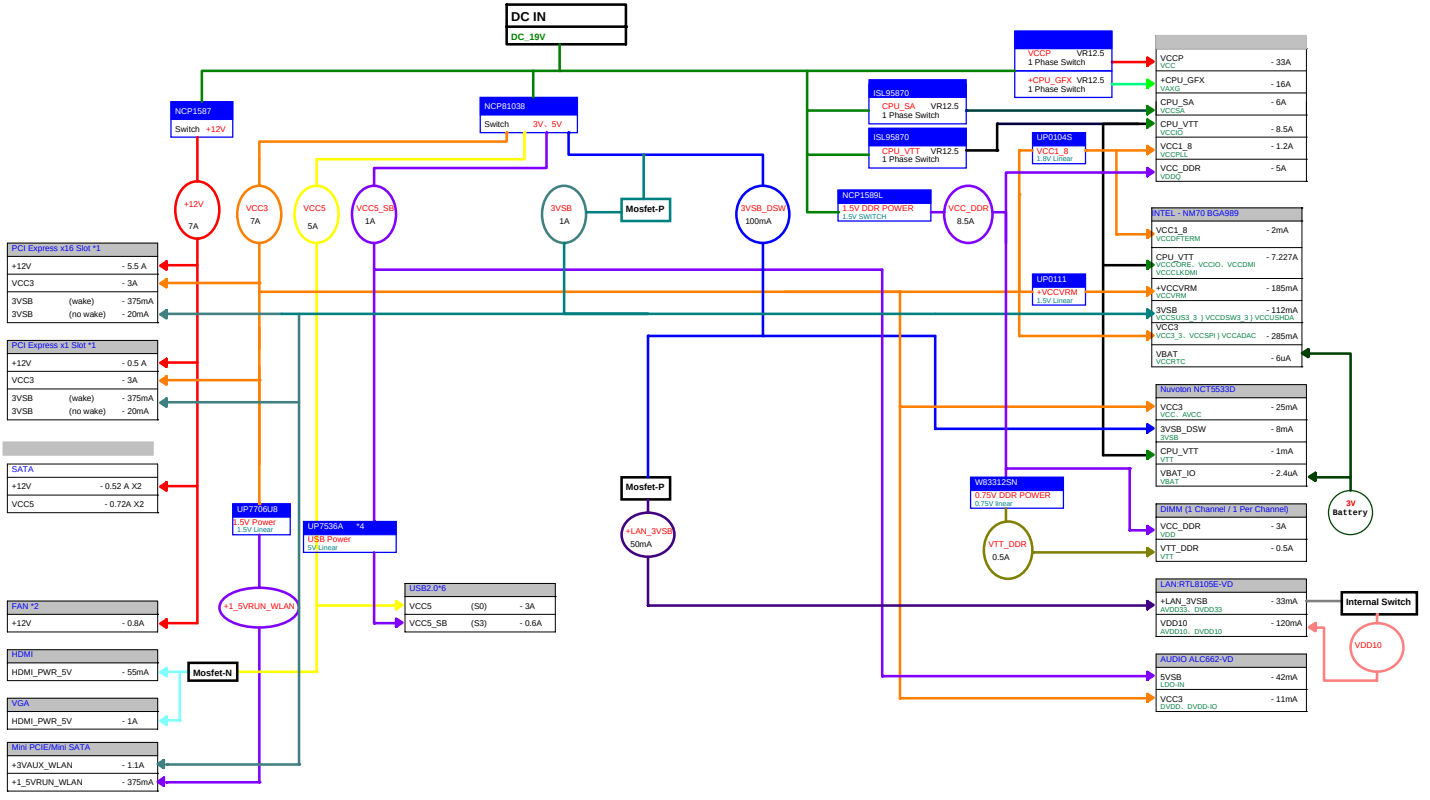
Single output power supply



DC IN Power Supply



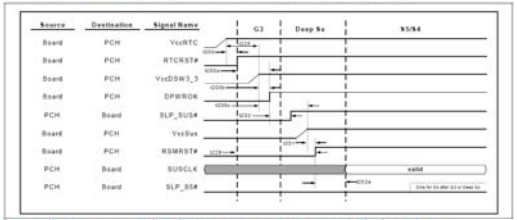
MICRO-START INT'L CO.,LTD.

Power Map

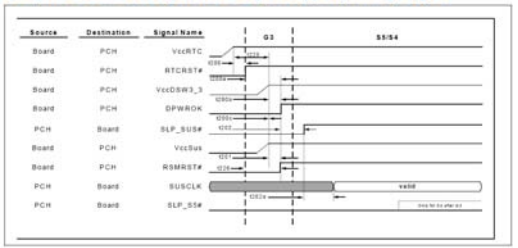
IH81M

1.0

G3 w/RTC Loss to S4/S5 (With Deep Sx Support) Timing Diagram

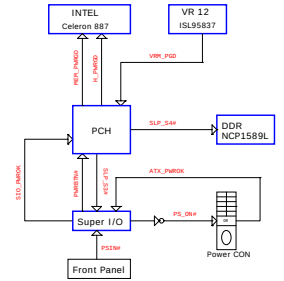


G3 w/RTC Loss to S4/S5 (Without Deep Sx Support) Timing Diagram

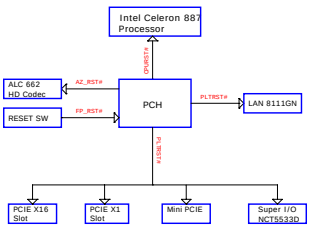


S5 to S0 Timing Diagram

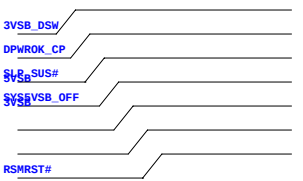
PWROK MAP



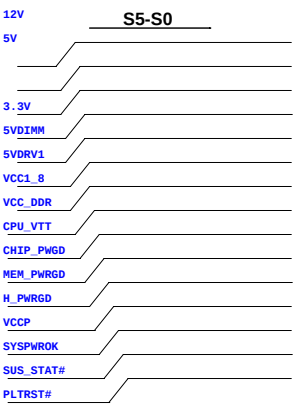
RESET MAP



G3-S5



S5-S0



MSI
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Title	Power Map	
Size	Document Number	Rev
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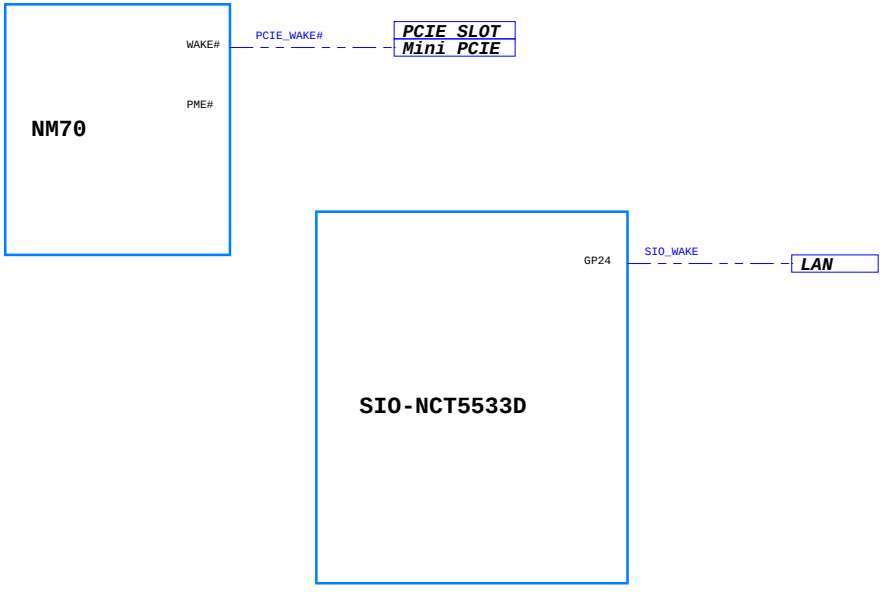
GPIO Map



MICRO-STAR INT'L CO.,LTD		
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PCH

GPIO	Alt Function	I/O/NC	Power	Tol	Default	Signal Name	Input/Output	Pull-Hi/Pull-Low
GPIO[0]	BMBUSY#	I/O	Main	3.3V	GPI	BM_BUSY#	Input	Pull-Hi
GPIO[1]	TACH1	I/O	Main	3.3V	GPI	GPIO1	Input	Pull-Hi
GPIO[2]	PIRQE#	I/O	Main	5V	GPI	PIRQE#	Output	Pull-Hi
GPIO[3]	PIRQF#	I/O	Main	5V	GPI	PIRQF#	Input	Pull-Hi
GPIO[4]	PIRQG#	I/O	Main	5V	GPI	PIRQG#	Input	Pull-Hi
GPIO[5]	PIRQH#	I/O	Main	5V	GPI	PIRQH#	Input	Pull-Hi
GPIO[6]	TACH2	I/O	Main	3.3V	GPI	GPIO6	Input	Pull-Hi
GPIO[7]	TACH2	I/O	Main	3.3V	GPI	GPIO7	Input	Pull-Hi
GPIO[8]	Unmuxed	I/O	Resume	3.3V	GPO	GPIO8	Output	Pull-Hi
GPIO[9]	OC5#	I/O	Resume	3.3V	Native	USB_OCP#5	Input	Pull-Hi
GPIO[10]	OC6#	I/O	Resume	3.3V	Native	USB_OCP#6	Input	Pull-Hi
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	PCH_SMBALERT#	Output	Pull-Hi
GPIO[12]	LAN_PHY_PWR_CTRL	I/O	Resume	3.3V	Native	MON_PWRBTN	Output	NC
GPIO[13]	HDA_DOCK_RST#	I/O	Resume	3.3V	GPI	SIO_PME#	Input	Pull-Hi
GPIO[14]	OC7#	I/O	Resume	3.3V	Native	USB_OCP#7	Input	Pull-Hi
GPIO[15]	Unmuxed	I/O	Resume	3.3V	GPO	SPI_HOLD_GPO#	Output	Pull-Hi
GPIO[16]	SATA4GP	I/O	Main	3.3V	GPI	PCH_GPIO16	Input	Pull-Hi
GPIO[17]	TACH0	I/O	Main	3.3V	GPI	GPIO17	Input	Pull-Hi
GPIO[18]	PCIECLKRQ1#	I/O	Main	3.3V	Native	PCIECLKRQ1#	Input	Pull-Hi
GPIO[19]	SATA1GP	I/O	Main	3.3V	GPI	PCH_GPIO19	Input	Pull-Hi
GPIO[20]	PCIECLKRQ2#	I/O	Main	3.3V	Native	PCIECLKREQ2#	Input	Pull-Hi
GPIO[21]	SATA0GP	I/O	Main	3.3V	GPI	PCH_GPIO21	Input	Pull-Hi
GPIO[22]	SCLOCK	I/O	Main	3.3V	GPI	PCH_GPIO22	Input	Pull-Hi
GPIO[23]	LDRQ1#	I/O	Main	3.3V	Native	CLR_CMOS	Input	NC
GPIO[24]	Unmuxed	I/O	Resume	3.3V	GPO	MINI_PWRON	Output	Pull-Hi
GPIO[25]	PCIECLKRQ3#	I/O	Resume	3.3V	Native	PCIECLKRQ3#	Input	Pull-Hi
GPIO[26]	PCIECLKRQ4#	I/O	Resume	3.3V	Native	PCIECLKRQ4#	Input	Pull-Hi
GPIO[27]	Unmuxed	I/O	DSW	3.3V	GPI	PCH_GPIO27	Output	Pull-Hi
GPIO[28]	Unmuxed	I/O	Resume	3.3V	GPO	PCH_GPIO28	Input	Pull-Hi
GPIO[29]	SLP_LAN#	I/O	Resume	3.3V	Native	SLP_LAN#	Output	NC
GPIO[30]	SUS_PWRDN_ACK/SUS_WARN#	I/O	Resume	3.3V	GPI	SUSWARN#_CP	Output	NC
GPIO[31]	Unmuxed	I/O	DSW	3.3V	GPI	GPIO31	Input	Pull-Hi
GPIO[32]	CLKRUN#	I/O	Main	3.3V	GPO	PCH_GPIO32	Output	NC
GPIO[33]	HDA_DOCK_EN#	I/O	Main	3.3V	GPO	SPI_WP#	Output	Pull-Hi
GPIO[34]	STP_PCI	I/O	Main	3.3V	GPI	STP_PCI#	Input	Pull-Hi
GPIO[35]	Unmuxed	I/O	Main	3.3V	GPO	EAPD	Output	NC
GPIO[36]	SATA2GP	I/O	Main	3.3V	GPI	PCH_GPIO36	Input	NC

PCH

GPIO	Alt Function	I/O/NC	Power	Tol	Default	Signal Name	Input/Output	Pull-Hi/Pull-Low
GPIO[37]	SATA3GP	I/O	Main	3.3V	GPI	PCH_GPIO37	Input	Pull-Hi
GPIO[38]	SLOAD	I/O	Main	3.3V	GPI	PCH_GPIO38	Input	Pull-Hi
GPIO[39]	SDATAOUT0	I/O	Main	3.3V	GPI	GFX_DET	Input	Pull-Hi
GPIO[40]	OC1#	I/O	Resume	3.3V	Native	USB_OCP#1	Input	Pull-Hi
GPIO[41]	OC2#	I/O	Resume	3.3V	Native	USB_OCP#2	Input	Pull-Hi
GPIO[42]	OC3#	I/O	Resume	3.3V	Native	USB_OCP#3	Input	Pull-Hi
GPIO[43]	OC4#	I/O	Resume	3.3V	Native	USB_OCP#4	Input	Pull-Hi
GPIO[44]	PCIECLKRQ5#	I/O	Resume	3.3V	Native	PCIECLKREQ5#	Input	Pull-Hi
GPIO[45]	PCIECLKRQ6#	I/O	Resume	3.3V	Native	PCH_GPIO45	Input	Pull-Hi
GPIO[46]	PCIECLKRQ7#	I/O	Resume	3.3V	Native	PCIECLKRQ7#	Input	Pull-Hi
GPIO[48]	SDATAOUT1	I/O	Main	3.3V	GPI	PCH_GPIO48	Input	Pull-Hi
GPIO[49]	SATA5GP	I/O	Main	3.3V	GPI	PCH_GPIO49	Input	Pull-Hi
GPIO[50]	Unmuxed	I/O	Main	3.3V	GPI	PCI_PREQ#1	Input	Pull-Hi
GPIO[51]	Unmuxed	I/O	Main	3.3V	GPO	PGNT#1	Input	NC
GPIO[52]	Unmuxed	I/O	Main	3.3V	GPI	PCI_REQ2#	Input	Pull-Hi
GPIO[53]	Unmuxed	I/O	Main	3.3V	GPO	PGNT#2	Output	NC
GPIO[54]	Unmuxed	I/O	Main	3.3V	GPI	PCI_REQ3#(	Input	Pull-Hi
GPIO[55]	Unmuxed	I/O	Main	3.3V	GPO	PGNT#3	Output	NC
GPIO[57]	Unmuxed	I/O	Resume	3.3V	GPI	GPIO57	Input	Pull-Hi
GPIO[58]	SML1CLK#	I/O	Resume	3.3V	Native	PCH_SML1CLK	Output	Pull-Hi
GPIO[59]	OC0#	I/O	Resume	3.3V	Native	USB_OCP#0	Input	Pull-Hi
GPIO[60]	SML0ALERT#	I/O	Resume	3.3V	Native	DRAMRST_CNTRL_PCH	Output	Pull-Hi
GPIO[61]	SUS_STAT#	I/O	Resume	3.3V	Native	SUS_STAT#	Output	NC
GPIO[62]	SUSCLK	I/O	Resume	3.3V	Native	SUSCLK	Output	NC
GPIO[63]	SLP_S5#	I/O	Resume	3.3V	Native	PCH_SLP_S5#	Output	NC
GPIO[64]	CLKOUTFLEX0	I/O	CORE	3.3V	Native	NC	Output	NC
GPIO[65]	CLKOUTFLEX1	I/O	CORE	3.3V	Native	NC	Output	NC
GPIO[66]	CLKOUTFLEX2	I/O	CORE	3.3V	Native	NC	Output	NC
GPIO[67]	CLKOUTFLEX3	I/O	CORE	3.3V	Native	CK_48M_SIO	Output	NC
GPIO[68]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO68	Input	Pull-Hi
GPIO[69]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO69	Input	Pull-Low
GPIO[70]	Unmuxed	I/O	CORE	3.3V	GPI	PE0_PRESENT#	Output	Pull-Low
GPIO[71]	Unmuxed	I/O	CORE	3.3V	GPI	PCH_GPIO71	Output	Pull-Hi
GPIO[72]	Unmuxed	I/O	DSW	3.3V	Native	GPIO72	Output	Pull-Hi
GPIO[73]	PCIECLKRQ0#	I/O	Resume	3.3V	Native	PCIECLKRQ0#	Input	Pull-Hi
GPIO[74]	SML1ALERT#	I/O	Resume	3.3V	Native	PCH_SML1ALERT#	Output	Pull-Hi
GPIO[75]	SML1DATA	I/O	Resume	3.3V	Native	PCH_SML1DATA	Output	Pull-Hi

SIO(NCT5533D)

PIN NAME	USAGE	Input/Output	NOTES
GPIO0	NA	NA	NA
GPIO4	SIO_GP04	Input	NA
GPIO20	NA	NA	NA
GPIO21	NA	NA	NA
GPIO22	NA	NA	NA
GPIO23	NA	NA	NA
GPIO24	SIO_WAKE	Input	Wake up signal from LAN
GPIO25	AMDPWR_EN	Input	Pin strap which disabled AMD power sequence
GPIO26	GPIO_26	NA	NA
GPIO41	SML1_CLK	Input	SMBus master clock
GPIO42	SML1_DATA	Bi-direct	SMBus master bi-directional Data
GPIO54	SLP_SUS#	Input	DSW signal
GPIO56	NA	NA	NA
GPIO57	NA	NA	NA
GPIO74	PWR_LED	Output	Power LED control signal.
GPIO75	LANPWR_EN	Output	LAN power enable signal.
GPIO80	CTSA#	NA	NA
GPIO81	DSRA#	NA	NA
GPIO82	RTSA#	NA	NA
GPIO83	DTRA#	NA	NA
GPIO84	SINA	NA	NA
GPIO85	SOUTA	NA	NA
GPIO86	DCDA#	NA	NA
GPIO87	RIA#	NA	NA

GPIO87	RIA#	Input	COM port signal

DDR-III DIMM Config

DEVICE	ADDRESS(SA1:SA0)	CLOCK
DIMM 1	00	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1

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GPIO Table

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1106

1. DC_ON change to +19V_ALW pull high

2. R356 change to 10K ohm.

1113

3. CORE
R72=887 ohm
R65=6.04K
R77=2.32K

VTT
R212=3.3K
R224=3.3K
C232=0.22u

VCCSA
R170=1.8K
R167=1.8K
R185=9.1K
Add C471=22uF MLCC socket よ

3.3V
R259=4.42K
R258=18K

DDR
R196=6.49K

4. MD_ID:Add R642,R643,R644,R645

5. Remove RN41,add R637,R639.

1119

1. VGA: Remove Q6 add Q78,Q79

1. USB IC: U7,U19,U28,U29 change I36-7536A19-U33 to I36-7550P09-U33.

0B->0C

1211

1. Remove C381

1213

1. For ME disable header:Remove R547, R546 上件，add ME_DIS header, ME_DIS_X1 帽子。

2.AZ_SDIN0_R: add C602,但不上件。

1219

Power solution

CORE
R77=2.32K->2.49K
R67=49.9K->130K
R72=887R->953R
C51=X->690p
R73=X->100R
C59=0.22u->82n
Q15=X->Add MOS
C545=C544=C112=C122=C123=C543=C542=C113=22u->47u
外加3顆47u MLCC於CPU下方

GFX
R35=140K?220K
C16=470p->820p
R29=1.91K->2K
C85=C40=C538=C539=C81=C87=22u->47u
EC42=X->470u

VCCIO
C546=C550=C551=C552=22u->47u
C218=X->0.1u
EC41=X->470u

+12V
R356=10K->5.9K
CHOKE11=1.2uH->3.3uH (L04-33A7411-L65)

+3.3V
C265=2200p->0.1u
C263=47p->100p
R258=18K->20K

+5V
C273=2200p->0.1u

1220

1. RGB:C36,C46,C53 change 10pf to 3.3 pf.

2.PCH_MEM_PWRGD: C118 change 0.047uf to 220pf.

1221

1. Remove test point:TP10~TP16;TP18~TP24;TP40~TP48.

1224

1. VCCP: add EC45.

1226

1. CPU_VTT: add C606，上件。add C607,不上件。

2. VR_HOT:R20,R60 value change to 11 Kohm.

1227

1. LDOVDD:C512 change to 22UF,add C608,10uf.remove test point:LDOVDD1

2.DDR_DRAMRST#:C214 change to 0.1uf，C215 change to 10pf

3.AZ_SYNC:Change R594 from 27 ohm to 15 ohm.

1228

1. CHIP_PWGD:Change R592 from 0 ohm to 56 ohm，C597 to 390pf

2.VR_HOT: change R60 to 10.7 Kohm，R20 to 10.2 Kohm

0106

1.Delay 3VAUX_EN:R286=820Kohm。