Cyborg N5-H Schematic

Intel TGL-H EVT

2020/07/30

REV : X00

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

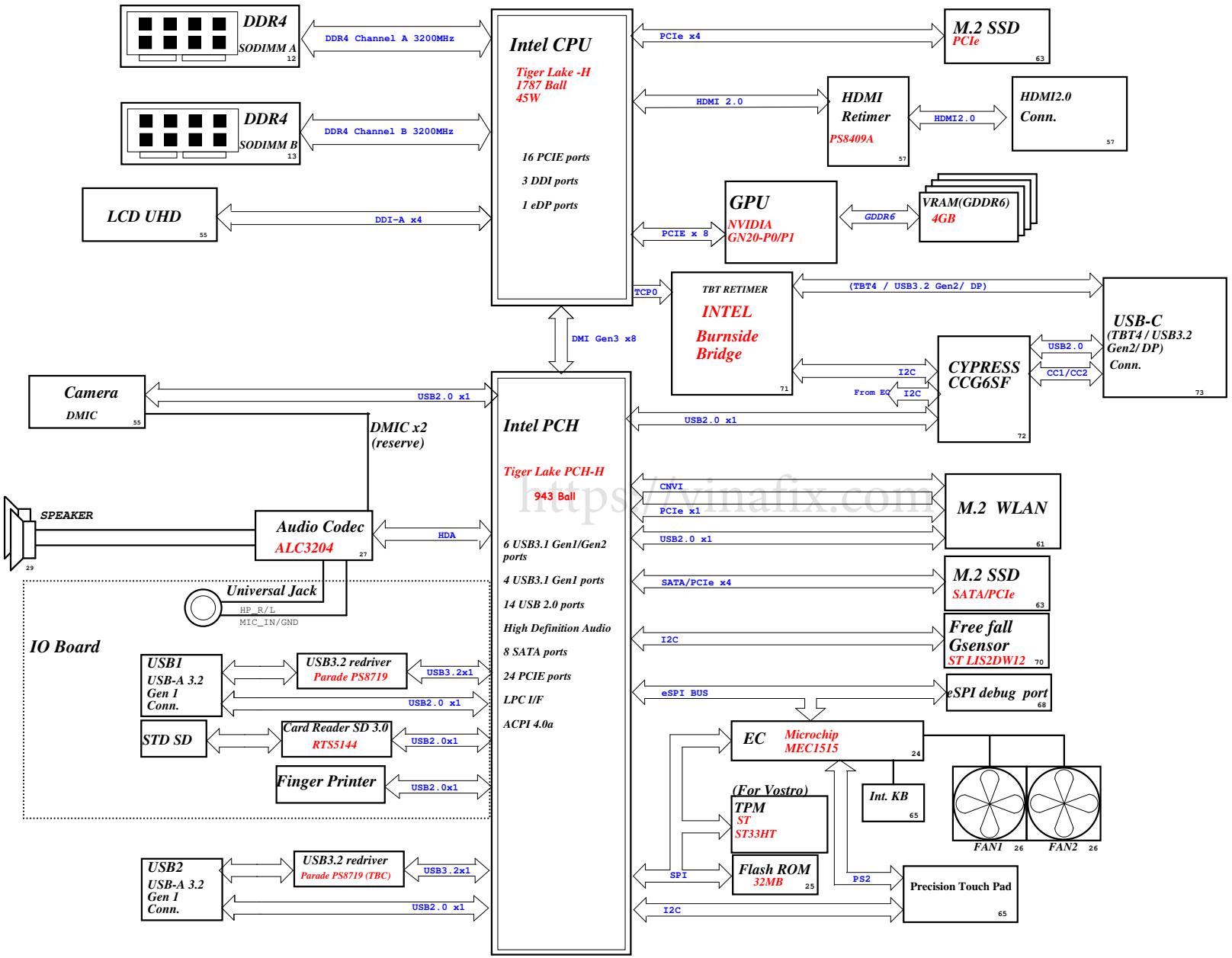
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A4	Document Number: Cyborg N5-H	Rev: X00
Date: Friday, November 13, 2020	Sheet 1 of 106	

Project Code : QRQY00000944
PCB P/N : 19844-SA
Revision : X01

Cyborg N5-H System Block Diagram



CHARGER ISL9538 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC SY8288CRAC-GP SY8288BRAC-GP 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5

CPU Core Power NCP81215MNTXG 46~50 NCP302045MNTWG*5 NCP302035LMNTWG	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS TPS51486RJER-GP 51	
INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3

CPU VCCPRIM_CORE 1V 11	
INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A AOZ2262QI-10-GP-U 53	
INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V APL5934KAI-TRG-GP-U 54	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 G2898KD1U-GP 40	
INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

1D8V_VGA_S0 G2898KD1U-GP 86	
INPUTS	OUTPUTS
3D3V_S0	1D8V_VGA_S0

1V_VGACORE_S0 MP86941GQVT-Z-GP 85	
INPUTS	OUTPUTS
DCBATOUT	1V_VGACORE_S0

0D95V_VGA_S0 RT5797ALGQW-GP 86	
INPUTS	OUTPUTS
DCBATOUT	0D95V_VGA_S0

1D35V_VGA_S0 RT8816BGQW-GP 86	
INPUTS	OUTPUTS
DCBATOUT	1D35V_VGA_S0

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Title: Block Diagram

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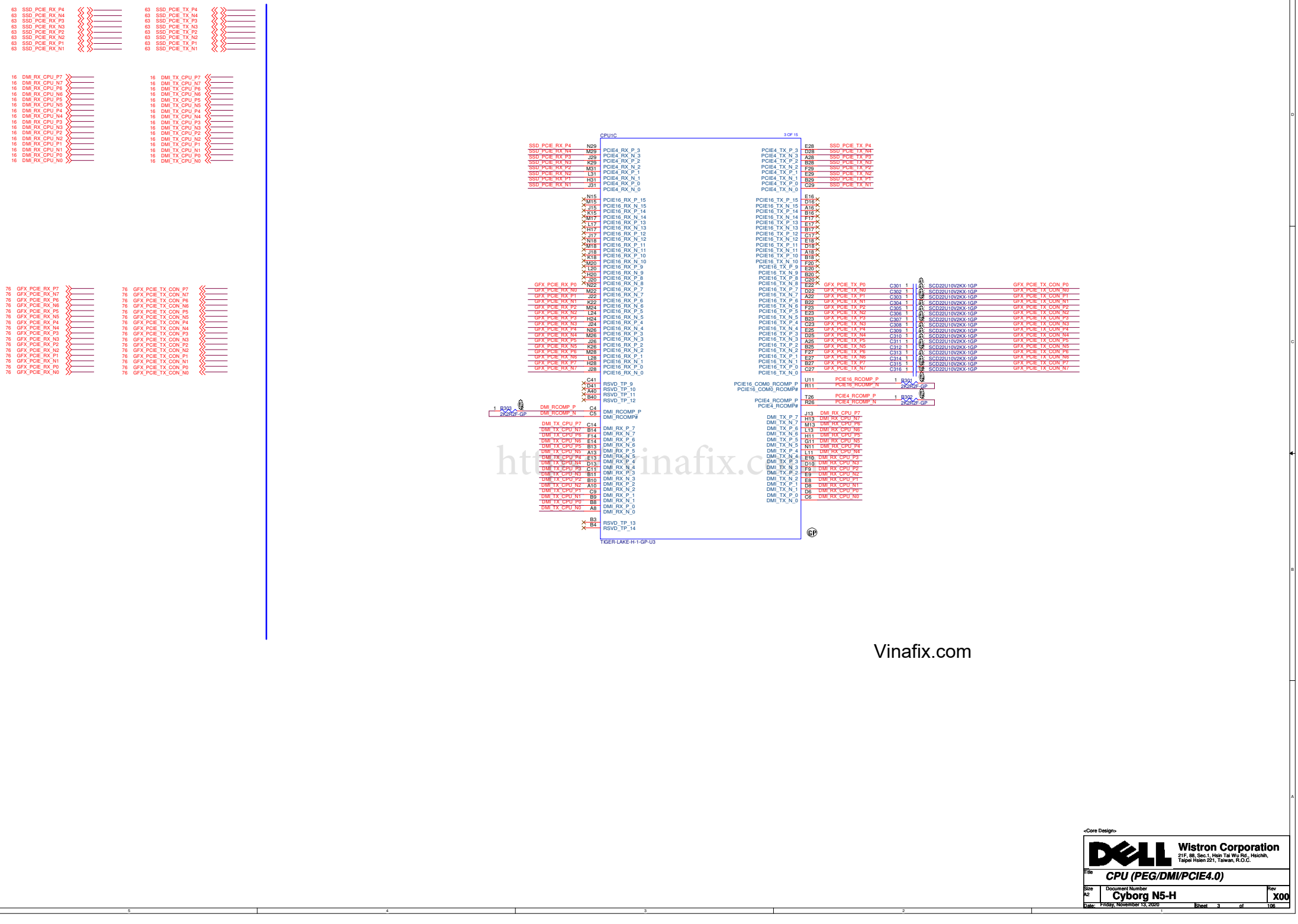
SSD_PCIE_RX_P4
SSD_PCIE_RX_N4
SSD_PCIE_RX_P3
SSD_PCIE_RX_N3
SSD_PCIE_RX_P2
SSD_PCIE_RX_N2
SSD_PCIE_RX_P1
SSD_PCIE_RX_N1
SSD_PCIE_TX_P4
SSD_PCIE_TX_N4
SSD_PCIE_TX_P3
SSD_PCIE_TX_N3
SSD_PCIE_TX_P2
SSD_PCIE_TX_N2
SSD_PCIE_TX_P1
SSD_PCIE_TX_N1
DMI_RX_CPU_P7
DMI_RX_CPU_N7
DMI_RX_CPU_P6
DMI_RX_CPU_N6
DMI_RX_CPU_P5
DMI_RX_CPU_N5
DMI_RX_CPU_P4
DMI_RX_CPU_N4
DMI_RX_CPU_P3
DMI_RX_CPU_N3
DMI_RX_CPU_P2
DMI_RX_CPU_N2
DMI_RX_CPU_P1
DMI_RX_CPU_N1
DMI_RX_CPU_P0
DMI_RX_CPU_N0
DMI_TX_CPU_P7
DMI_TX_CPU_N7
DMI_TX_CPU_P6
DMI_TX_CPU_N6
DMI_TX_CPU_P5
DMI_TX_CPU_N5
DMI_TX_CPU_P4
DMI_TX_CPU_N4
DMI_TX_CPU_P3
DMI_TX_CPU_N3
DMI_TX_CPU_P2
DMI_TX_CPU_N2
DMI_TX_CPU_P1
DMI_TX_CPU_N1
DMI_TX_CPU_P0
DMI_TX_CPU_N0
GFX_PCIE_RX_P7
GFX_PCIE_RX_N7
GFX_PCIE_RX_P6
GFX_PCIE_RX_N6
GFX_PCIE_RX_P5
GFX_PCIE_RX_N5
GFX_PCIE_RX_P4
GFX_PCIE_RX_N4
GFX_PCIE_RX_P3
GFX_PCIE_RX_N3
GFX_PCIE_RX_P2
GFX_PCIE_RX_N2
GFX_PCIE_RX_P1
GFX_PCIE_RX_N1
GFX_PCIE_RX_P0
GFX_PCIE_RX_N0
GFX_PCIE_TX_CON_P7
GFX_PCIE_TX_CON_N7
GFX_PCIE_TX_CON_P6
GFX_PCIE_TX_CON_N6
GFX_PCIE_TX_CON_P5
GFX_PCIE_TX_CON_N5
GFX_PCIE_TX_CON_P4
GFX_PCIE_TX_CON_N4
GFX_PCIE_TX_CON_P3
GFX_PCIE_TX_CON_N3
GFX_PCIE_TX_CON_P2
GFX_PCIE_TX_CON_N2
GFX_PCIE_TX_CON_P1
GFX_PCIE_TX_CON_N1
GFX_PCIE_TX_CON_P0
GFX_PCIE_TX_CON_N0
CPU1C
3 OF 15
PCIE4_RX_P_3
PCIE4_RX_N_3
PCIE4_RX_P_2
PCIE4_RX_N_2
PCIE4_RX_P_1
PCIE4_RX_N_1
PCIE4_RX_P_0
PCIE4_RX_N_0
PCIE4_TX_P_3
PCIE4_TX_N_3
PCIE4_TX_P_2
PCIE4_TX_N_2
PCIE4_TX_P_1
PCIE4_TX_N_1
PCIE4_TX_P_0
PCIE4_TX_N_0
PCIE16_RX_P_15
PCIE16_RX_N_15
PCIE16_RX_P_14
PCIE16_RX_N_14
PCIE16_RX_P_13
PCIE16_RX_N_13
PCIE16_RX_P_12
PCIE16_RX_N_12
PCIE16_RX_P_11
PCIE16_RX_N_11
PCIE16_RX_P_10
PCIE16_RX_N_10
PCIE16_RX_P_9
PCIE16_RX_N_9
PCIE16_RX_P_8
PCIE16_RX_N_8
PCIE16_RX_P_7
PCIE16_RX_N_7
PCIE16_RX_P_6
PCIE16_RX_N_6
PCIE16_RX_P_5
PCIE16_RX_N_5
PCIE16_RX_P_4
PCIE16_RX_N_4
PCIE16_RX_P_3
PCIE16_RX_N_3
PCIE16_RX_P_2
PCIE16_RX_N_2
PCIE16_RX_P_1
PCIE16_RX_N_1
PCIE16_RX_P_0
PCIE16_RX_N_0
PCIE16_TX_P_15
PCIE16_TX_N_15
PCIE16_TX_P_14
PCIE16_TX_N_14
PCIE16_TX_P_13
PCIE16_TX_N_13
PCIE16_TX_P_12
PCIE16_TX_N_12
PCIE16_TX_P_11
PCIE16_TX_N_11
PCIE16_TX_P_10
PCIE16_TX_N_10
PCIE16_TX_P_9
PCIE16_TX_N_9
PCIE16_TX_P_8
PCIE16_TX_N_8
PCIE16_TX_P_7
PCIE16_TX_N_7
PCIE16_TX_P_6
PCIE16_TX_N_6
PCIE16_TX_P_5
PCIE16_TX_N_5
PCIE16_TX_P_4
PCIE16_TX_N_4
PCIE16_TX_P_3
PCIE16_TX_N_3
PCIE16_TX_P_2
PCIE16_TX_N_2
PCIE16_TX_P_1
PCIE16_TX_N_1
PCIE16_TX_P_0
PCIE16_TX_N_0
RSVD_TP_9
RSVD_TP_10
RSVD_TP_11
RSVD_TP_12
DMI_RCOMP_P
DMI_RCOMP#
DMI_RX_P_7
DMI_RX_N_7
DMI_RX_P_6
DMI_RX_N_6
DMI_RX_P_5
DMI_RX_N_5
DMI_RX_P_4
DMI_RX_N_4
DMI_RX_P_3
DMI_RX_N_3
DMI_RX_P_2
DMI_RX_N_2
DMI_RX_P_1
DMI_RX_N_1
DMI_RX_P_0
DMI_RX_N_0
RSVD_TP_13
RSVD_TP_14
PCIE16_COMP_RCOMP_P
PCIE16_COMP_RCOMP#
PCIE4_RCOMP_P
PCIE4_RCOMP#
DMI_TX_P_7
DMI_TX_N_7
DMI_TX_P_6
DMI_TX_N_6
DMI_TX_P_5
DMI_TX_N_5
DMI_TX_P_4
DMI_TX_N_4
DMI_TX_P_3
DMI_TX_N_3
DMI_TX_P_2
DMI_TX_N_2
DMI_TX_P_1
DMI_TX_N_1
DMI_TX_P_0
DMI_TX_N_0
TIGER-LAKE-H-1-GP-U3
R309
2K2R2F-GP
R301
2K49F-GP
R302
2K49F-GP
C301
C302
C303
C304
C305
C306
C307
C308
C309
C310
C311
C312
C313
C314
C315
C316
SCD22U10V2KX-1GP
Vinafix.com
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (PEG/DMI/PCIE4.0)
Size
A2
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Cyborg N5-H
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X00
Date:
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eDP

55 eDP_TX_CPU_N3
55 eDP_TX_CPU_P3
55 eDP_TX_CPU_N2
55 eDP_TX_CPU_P2
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P

USB-C Port1

71 USB1_TCSS_TX_N0
71 USB1_TCSS_TX_P0
71 USB1_TCSS_TX_N1
71 USB1_TCSS_TX_P1
71 USB1_TCSS_RX_N0
71 USB1_TCSS_RX_P0
71 USB1_TCSS_RX_N1
71 USB1_TCSS_RX_P1
71 USB1_TCSS_AUX_N
71 USB1_TCSS_AUX_P

Others

20 AUD_AZACPU_SDI
20 AUD_AZACPU_SDO_R
20 AUD_AZACPU_SCLK

57 DP3_DDI_TX_P0
57 DP3_DDI_TX_N0
57 DP3_DDI_TX_P1
57 DP3_DDI_TX_N1
57 DP3_DDI_TX_P2
57 DP3_DDI_TX_N2
57 DP3_DDI_TX_P3
57 DP3_DDI_TX_N3

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USB1_TCSS_TX_P1 BL38 TCP0_TX_P1
USB1_TCSS_TX_N1 BL37 TCP0_TX_N1
USB1_TCSS_TX_P0 BP37 TCP0_TX_P0
USB1_TCSS_TX_N0 BP38 TCP0_TX_N0
USB1_TCSS_RX_P1 BK40 TCP0_TXRX_P1
USB1_TCSS_RX_N1 BK41 TCP0_TXRX_N1
USB1_TCSS_RX_P0 BL41 TCP0_TXRX_P0
USB1_TCSS_RX_N0 BL40 TCP0_TXRX_N0

USB1_TCSS_AUX_P BN37 TCP0_AUX_P
USB1_TCSS_AUX_N BN38 TCP0_AUX#

BD40 RSVD_TP_1
BD41 RSVD_TP_2
BD37 RSVD_TP_3
BD36 RSVD_TP_4

1 R404 2K2R2F-GP TCP_DFX_RCOMP
BP41 RSVD_2.2K_PD
BP40 RSVD_TP_5

BG38 TCP1_TX_P1
BG37 TCP1_TX_N1
BJ37 TCP1_TX_P0
BJ38 TCP1_TX_N0
BG40 TCP1_TXRX_P1
BG41 TCP1_TXRX_N1
BH41 TCP1_TXRX_P0
BH40 TCP1_TXRX_N0

BH37 TCP1_AUX_P
BH38 TCP1_AUX#

BW37 TCP2_TX_P1
BW38 TCP2_TX_N1
BT38 TCP2_TX_P0
BT37 TCP2_TX_N0
BW41 TCP2_TXRX_P1
BW40 TCP2_TXRX_N1
BU40 TCP2_TXRX_P0
BU41 TCP2_TXRX_N0

BU38 TCP2_AUX_P
BU37 TCP2_AUX#

CD37 TCP3_TX_P1
CD38 TCP3_TX_N1
CB38 TCP3_TX_P0
CB37 TCP3_TX_N0
CC41 TCP3_TXRX_P1
CC40 TCP3_TXRX_N1
CB40 TCP3_TXRX_P0
CB41 TCP3_TXRX_N0

CC38 TCP3_AUX_P
CC37 TCP3_AUX#

AFTP401 AFTE14P-1-GP 1 DSI_DE_TE D34 RSVD_TP_45
E34 DISP_UTILS

AUD_AZACPU_SDI_R A32 AUDOUT
AUD_AZACPU_SDO_R A31 AUDIN
AUD_AZACPU_SCLK B32 AUDCLK

CPU_EAR F36 EAR_N

TIGER-LAKE-H-1-GP-U3

DPIP3_RXP_3 AC40
DPIP3_RXN_3 AC41
DPIP3_RXP_2 AD39
DPIP3_RXN_2 AD40
DPIP3_RXP_1 AC37
DPIP3_RXN_1 AC38
DPIP3_RXP_0 AD36
DPIP3_RXN_0 AD37

DPIP3_AUX_P AN38
DPIP3_AUX# AN39

DPIP2_RXP_3 AE40
DPIP2_RXN_3 AE41
DPIP2_RXP_2 AF39
DPIP2_RXN_2 AF40
DPIP2_RXP_1 AF36
DPIP2_RXN_1 AF37
DPIP2_RXP_0 AG37
DPIP2_RXN_0 AG38

DPIP2_AUX_P AR39
DPIP2_AUX# AR40

DPIP1_RXP_3 AG40
DPIP1_RXN_3 AG41
DPIP1_RXP_2 AJ39
DPIP1_RXN_2 AJ40
DPIP1_RXP_1 AJ36
DPIP1_RXN_1 AJ37
DPIP1_RXP_0 AK37
DPIP1_RXN_0 AK38

DPIP1_AUX_P AR36
DPIP1_AUX# AR37

DPIP0_RXP_3 AL36
DPIP0_RXN_3 AL37
DPIP0_RXP_2 AK40
DPIP0_RXN_2 AK41
DPIP0_RXP_1 AL39
DPIP0_RXN_1 AL40
DPIP0_RXP_0 AM37
DPIP0_RXN_0 AM38

DPIP0_AUX_P AT37
DPIP0_AUX# AT38

RSVD_TP_6 AM41
RSVD_TP_7 AM40
RSVD_TP_8 AN41

AC35 DPIP0_HPD3
AE37 DPIP0_HPD2
AE35 DPIP0_HPD1
AE38 DPIP0_HPD0

DPIP3_HPD
DPIP2_HPD
DPIP1_HPD
DPIP0_HPD

DPIP3_RCOMP
DPIP2_RCOMP
DPIP1_RCOMP
DPIP0_RCOMP

AT41 DPIP3_RCOMP R413 2F-1-GP
AU40 DPIP2_RCOMP R414 50R2F-1-GP
AU39 DPIP1_RCOMP R408 50R2F-1-GP
AT40 DPIP0_RCOMP R409 50R2F-1-GP

RN401 SRN100KJ-5-GP
1 8
2 7
3 6
4 5

For RTX

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DDR4(IL) / DDR4(NIL) / DDR5(IL)

AL8 NC/NC/DDR3_DQSP_4
AL9 NC/NC/DDR3_DQSN_4
AL3 NC/NC/DDR1_DQSP_4
AL4 NC/NC/DDR1_DQSN_4

AJ8 NC/NC/DDR3_DQ4_3
AJ9 NC/NC/DDR3_DQ4_2
AJ6 NC/NC/DDR3_DQ4_1
AH7 NC/NC/DDR3_DQ4_0
AJ3 NC/NC/DDR1_DQ4_3
AJ4 NC/NC/DDR1_DQ4_2
AJ1 NC/NC/DDR1_DQ4_1
AH2 NC/NC/DDR1_DQ4_0

DDR4 / DDR5

BT9 NC/DDR2_CLK_N2
BT8 NC/DDR2_CLK_P2
BT4 NC/DDR0_CLK_N2
BT3 NC/DDR0_CLK_P2
AT2 NC/DDR1_CLK_N2
AT1 NC/DDR1_CLK_P2
AT7 NC/DDR3_CLK_N2
AT6 NC/DDR3_CLK_P2

BT6 NC/DDR2_CLK_P3
BT7 NC/DDR2_CLK_N3
BT1 NC/DDR0_CLK_P3
BT2 NC/DDR0_CLK_N3
AT3 NC/DDR1_CLK_P3
AT4 NC/DDR1_CLK_N3
AT8 NC/DDR3_CLK_P3
AT9 NC/DDR3_CLK_N3

BH9 NC/NC_1
BH8 NC/NC_2
BG9 NC/NC_3
BH4 NC/NC_4
BH3 NC/NC_5
BG4 NC/NC_6
AY1 NC/NC_7
AW1 NC/DDR1_CS2

BD3 NC/NC_8
BF2 NC/NC_9
BE8 NC/NC_10
BE3 NC/DDR1_CS3
BG3 NC/DDR0_CS2
BG8 NC/DDR2_CS2
AW7 NC/DDR3_CS2
BD8 NC/NC_11
BF7 NC/NC_12
BD7 NC/DDR3_CS3

C40 NC_1
CR40 NC_2
CR2 NC_3
C2 NC_4

TIGER-LAKE-H-1-GP-U3

DDIA_TXP_3 AU36 eDP_TX_CPU_P3
DDIA_TXN_3 AU37 eDP_TX_CPU_N3
DDIA_TXP_2 AV40 eDP_TX_CPU_P2
DDIA_TXN_2 AV41 eDP_TX_CPU_N2
DDIA_TXP_1 AV37 eDP_TX_CPU_P1
DDIA_TXN_1 AV38 eDP_TX_CPU_N1
DDIA_TXP_0 AW39 eDP_TX_CPU_P0
DDIA_TXN_0 AW40 eDP_TX_CPU_N0

DDIA_AUX_P BA40 eDP_AUX_CPU_P
DDIA_AUX# BA41 eDP_AUX_CPU_N

DDI_RCOMP BC38 eDP_RCOMP 2 R401 1 150R2F-1-GP
RSVD_4 BD39

DDIB_TXP_3 AW36 DP3_DDI_TX_P3
DDIB_TXN_3 AW37 DP3_DDI_TX_N3
DDIB_TXP_2 BB39 DP3_DDI_TX_P0
DDIB_TXN_2 BB40 DP3_DDI_TX_N0
DDIB_TXP_1 BA37 DP3_DDI_TX_P1
DDIB_TXN_1 BA38 DP3_DDI_TX_N1
DDIB_TXP_0 BB36 DP3_DDI_TX_P2
DDIB_TXN_0 BB37 DP3_DDI_TX_N2

DDIB_AUX_P BC35
DDIB_AUX# BC36

CSI_A_CLK_P U39
CSI_A_CLK# U40
CSI_A_DP_1/CSI_B_DP_2 R37
CSI_A_DN_1/CSI_B_DN_2 R38
CSI_A_DP_0/CSI_B_DP_3 U36
CSI_A_DN_0/CSI_B_DN_3 U37

CSI_B_CLK_P R40
CSI_B_CLK# R41
CSI_B_DP_1 P36
CSI_B_DN_1 P37
CSI_B_DP_0 P39
CSI_B_DN_0 P40

CSI_RCOMP R35 CSI_RCOMP 2 R405 1 150R2F-1-GP

1D05V_VCCSTG
1 R402 1KR2J-1-GP 2 CPU_EAR

AUD_AZACPU_SDI R406 1 20R2J-3-GP AUD_AZACPU_SDI_R

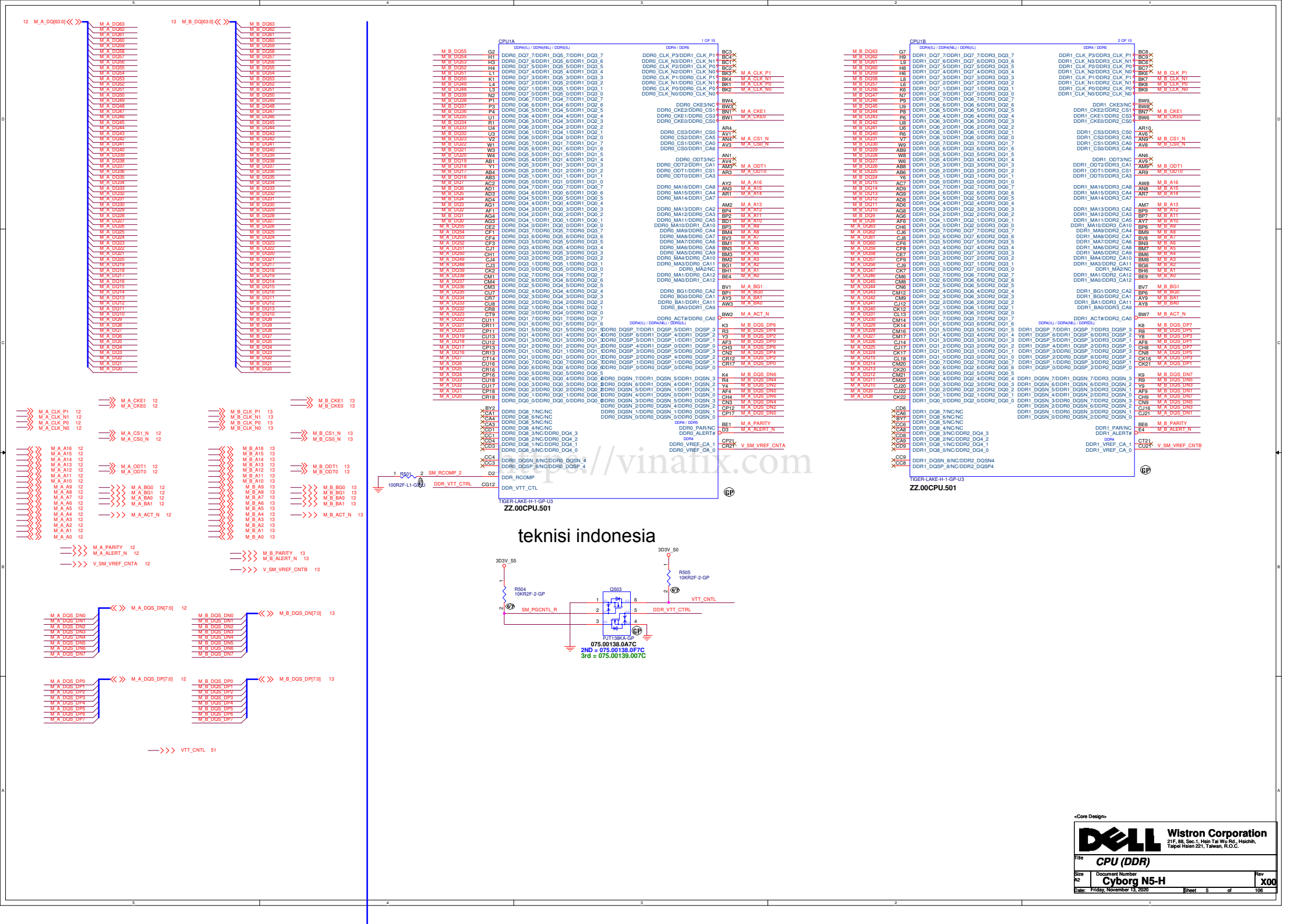
<Core Design>

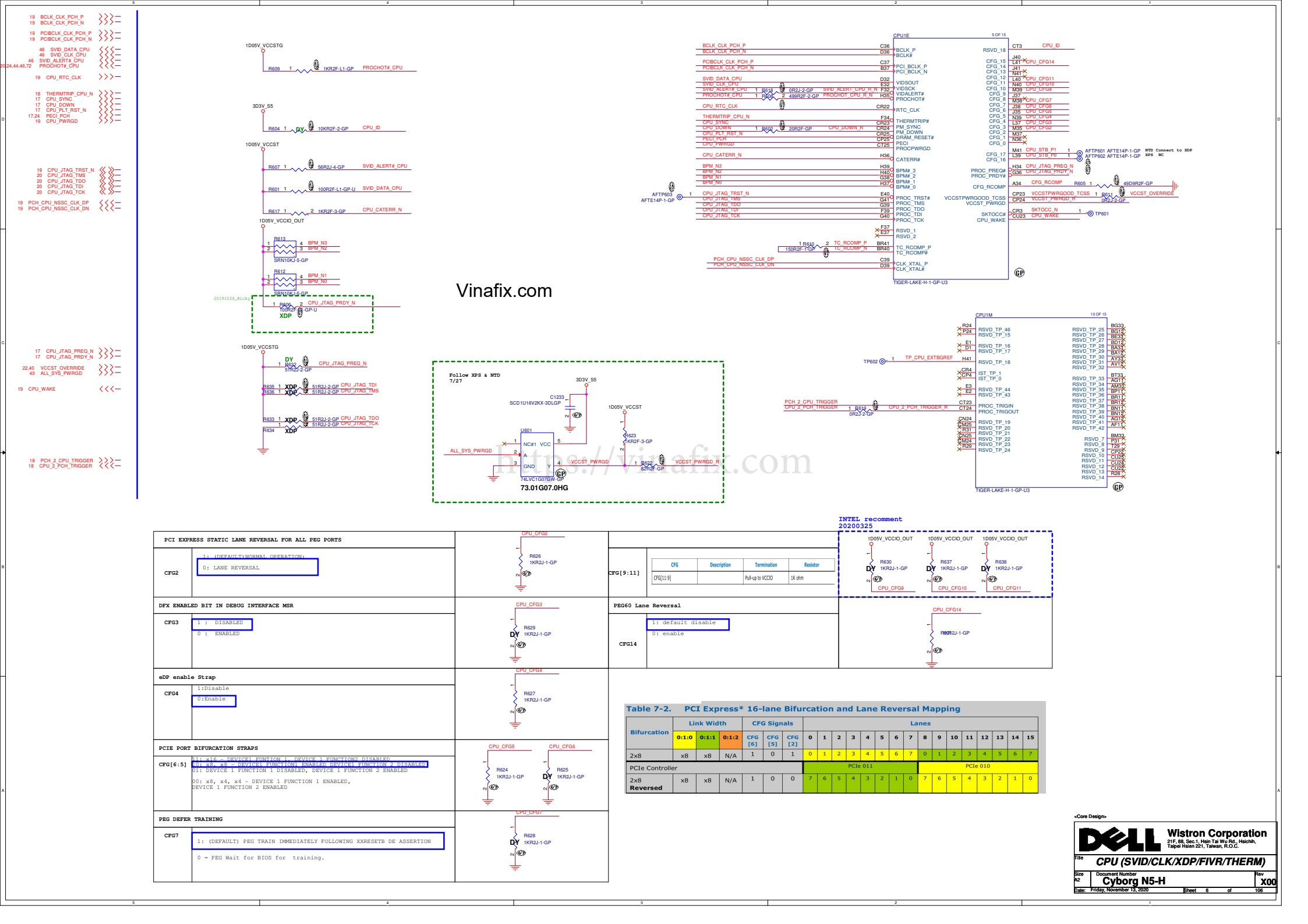
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDI/EDP/TCP/DP/CSI)

Size: A3 | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 4 of 106


CPU1A
CPU1B
TIGER-LAKE-H-1-GP-U3
ZZ.00CPU.501
teknisi indonesia
https://vinafix.com
R504 10KR2F-2-GP
R505 10KR2F-2-GP
Q503
PJT138KA-GP
075.00138.0A7C
2ND = 075.00138.0F7C
3rd = 075.00139.007C
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (DDR)
Cyborg N5-H
X00
Friday, November 13, 2020
Sheet 5 of 106



PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS

CFG2

1: (DEFAULT)NORMAL OPERATION;

0: LANE REVERSAL

DFX ENABLED BIT IN DEBUG INTERFACE MSR

CFG3

1 : DISABLED

0 : ENABLED

eDP enable Strap

CFG4

1:Disable

0:Enable

PCIE PORT BIFURCATION STRAPS

CFG[6:5]

11: x16 – DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED

10: x8, x8 – DEVICE1 FUNCTION1 ENABLED,DEVICE1 FUNCTION 2 DISABLED

01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED

00: x8, x4, x4 – DEVICE 1 FUNCTION 1 ENABLED,
DEVICE 1 FUNCTION 2 ENABLED

PEG DEFER TRAINING

CFG7

1: (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION

0 = PEG Wait for BIOS for training.

CFG[9:11]

CFG	Description	Termination	Resistor
CFG[11:9]		Pull-up to VCCIO	1K ohm

PEG60 Lane Reversal

CFG14

1: default disable

0: enable

Table 7-2. PCI Express* 16-lane Bifurcation and Lane Reversal Mapping

Bifurcation	Link Width			CFG Signals			Lanes													
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2x8	x8	x8	N/A	1	0	1	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
PCIe Controller							PCIe 011								PCIe 010							
2x8 **Reversed**	x8	x8	N/A	1	0	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (SVID/CLK/XDP/FIVR/THERM)

Size: A2 | Document Number: Cyborg N5-H | Rev: X00

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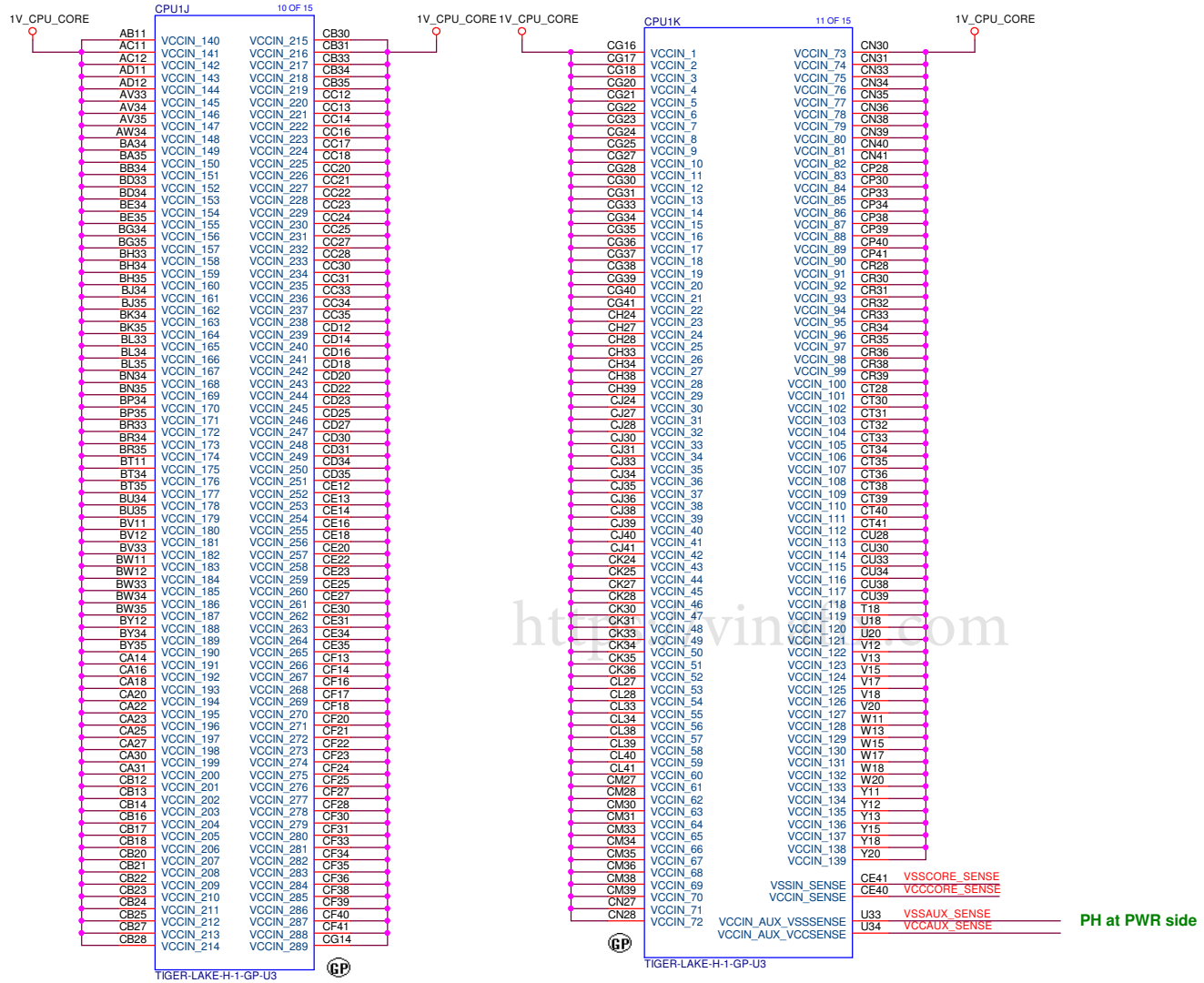
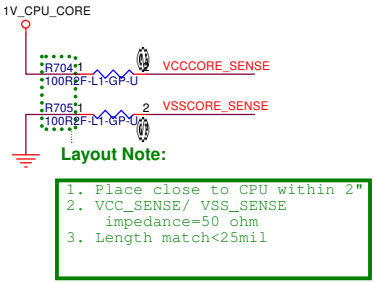
46 VCCCORE_SENSE
46 VSSCORE_SENSE
50 VSSAUX_SENSE
50 VCCAUX_SENSE

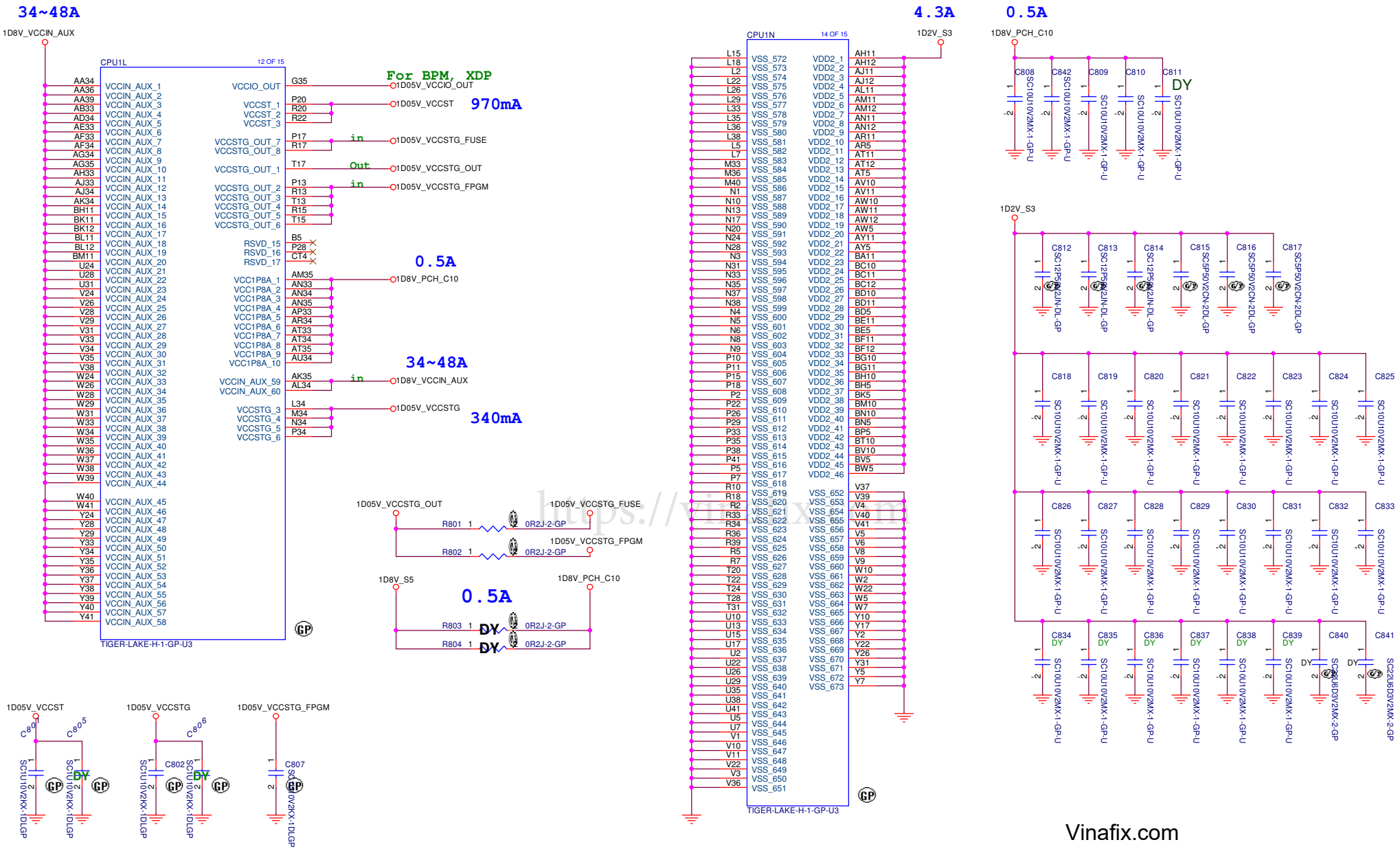




<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCIN)
Size: A3
Document Number: Cyborg N5-H
Rev: X00
Date: Friday, November 13, 2020
Sheet 7 of 106



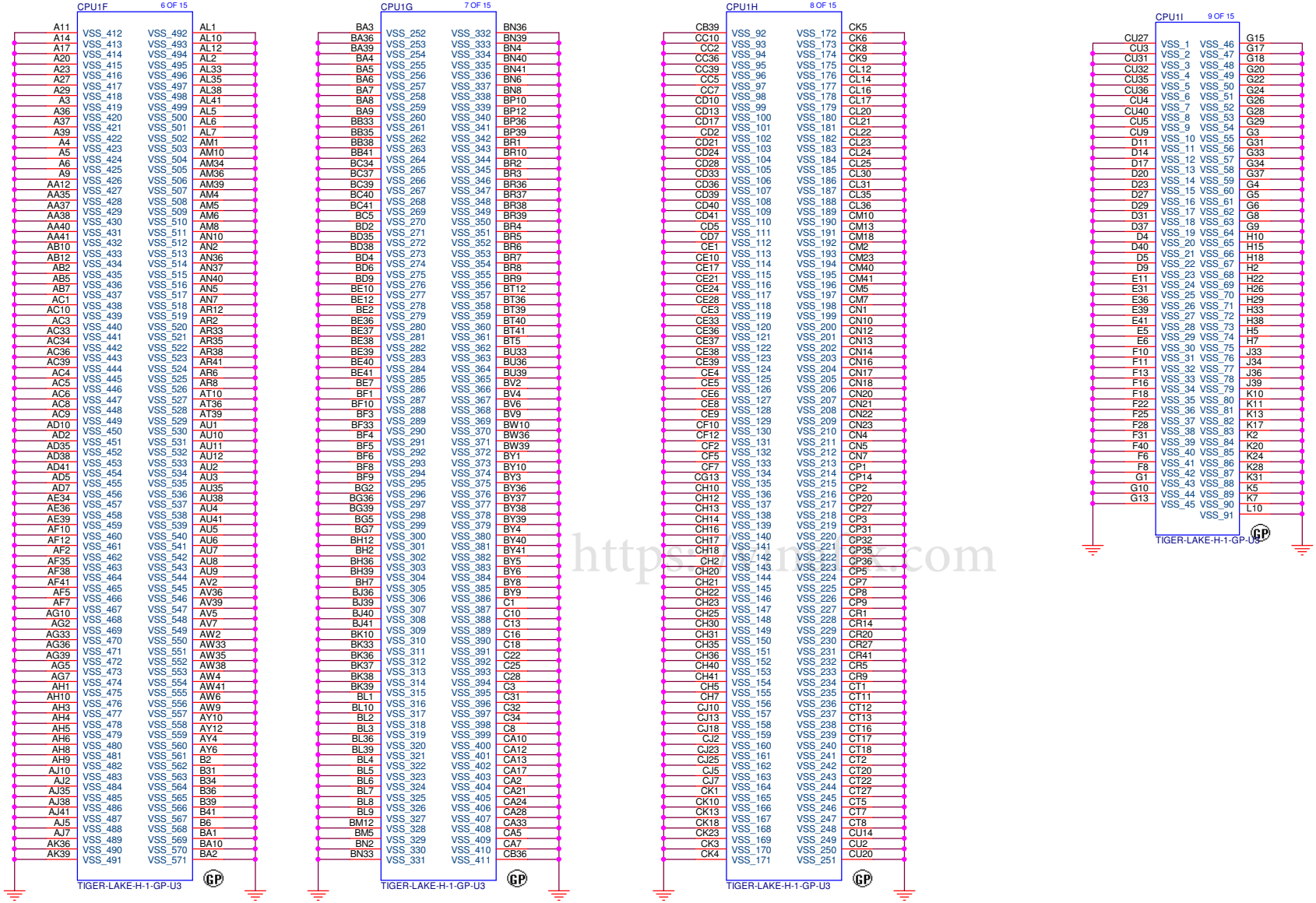
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCCIN_AUX/VCCST/VCCSTG/VCCDD2/Others)

Size: A3 | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 8 of 106



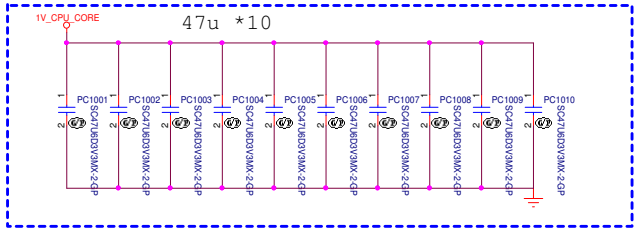
<Core Design>

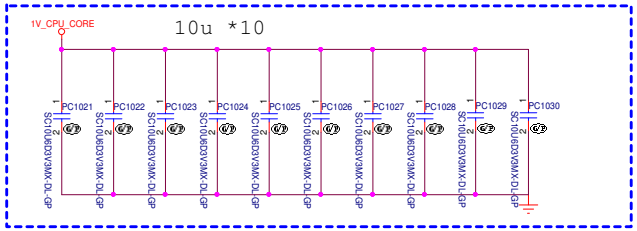
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

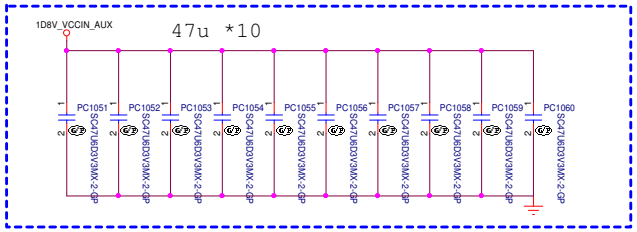
Title: CPU (VSS)

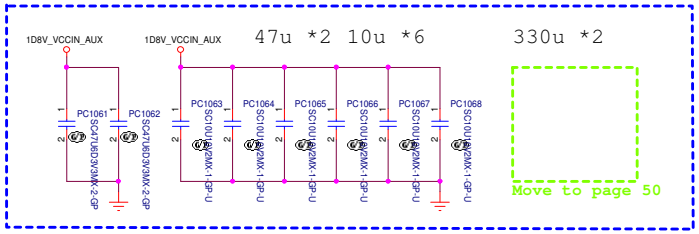
Size	Document Number	Rev
A3	Cyborg N5-H	X00

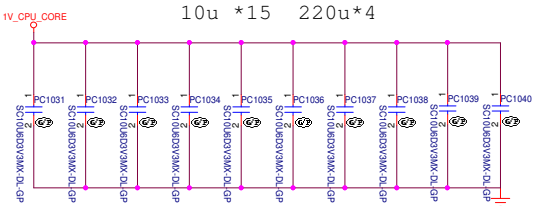
Date: Friday, November 13, 2020 Sheet 9 of 106

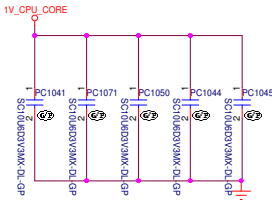


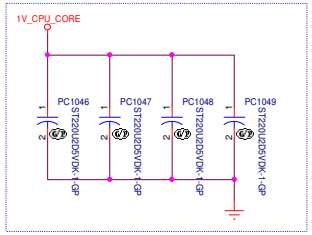




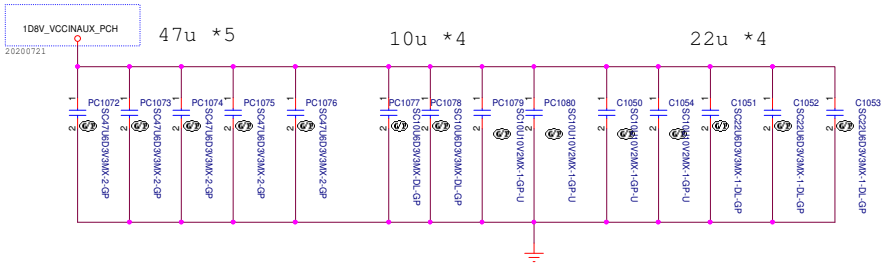


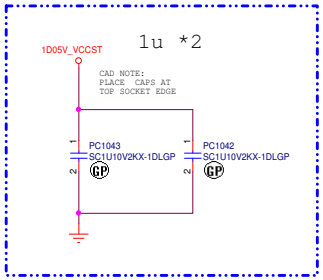


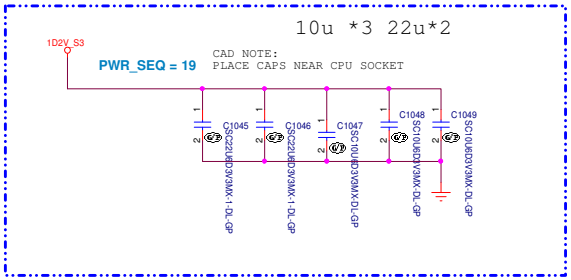


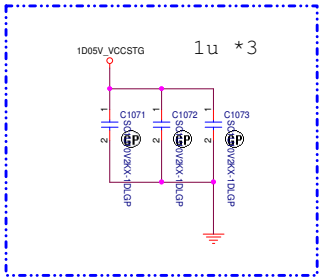


20200708
Change to 2.5V 7343H40









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (CORE Power Cap1)

Size: C | Document Number: Cyborg N5-H | Rev: X00

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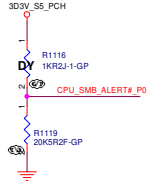
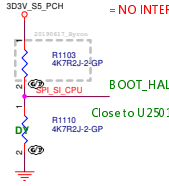
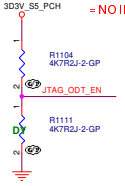
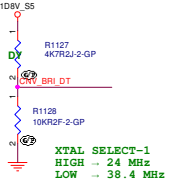
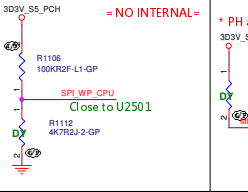
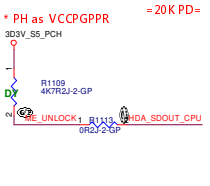
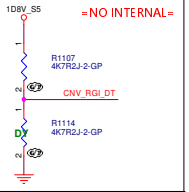
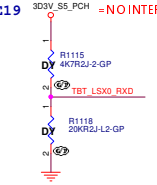
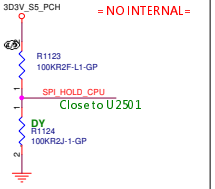
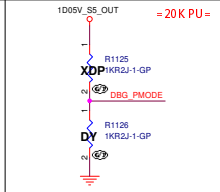
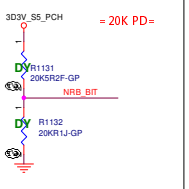
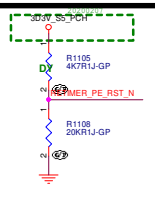
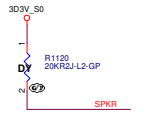
Need Check wuth XPS & NTD

GPIO	GPP_C5	SPI_SI	GPP_H15	GPP_J2	SPI_IO_2	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_J4)
Schematic							
High	ESPI Disable	Enable No Reboot mode	JTAG ODT is Enable	24 MHz	Disable	Disable Flash Descriptor Security	INTEGRATED CNVI DISABLE
Low	Enable =default=	Disable No Reboot mode	JTAG ODT is Disable	38.4 MHz =default=	Enable	Enable Flash Descriptor security measures	INTEGRATED CNVI ENABLE

GPIO	TBT LSX VCCIO conf.#0	TBT LSX VCCIO conf.#1	TBT LSX VCCIO conf.#2	TBT LSX VCCIO conf.#3	SPI_IO_3		GPP_B18	GPD_7
Schematic	E19 	E21 =NO INTERNAL=	D10 =NO INTERNAL=	D12				
High	DDP4 I2C/TBT_LSX0/BBSB_LSO pins at 3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)		
Low	DDP4 I2C/TBT_LSX0/BBSB_LSO pins at 1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED		

GPIO	GPP_B14/SPKR
Schematic	 TOP SWAP OVERRIDE HIGH- TOP SWAP ENABLED LOW-DISABLE WEAK INTERNAL PD
High	TOP SWAP ENABLED
Low	DISABLE

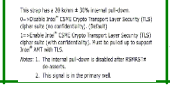
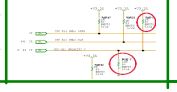
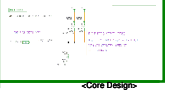
XTAL INPUT MODE

HIGH : XTAL INPUT IS SINGLE ENDED

LOW : XTAL IS ATTACHED

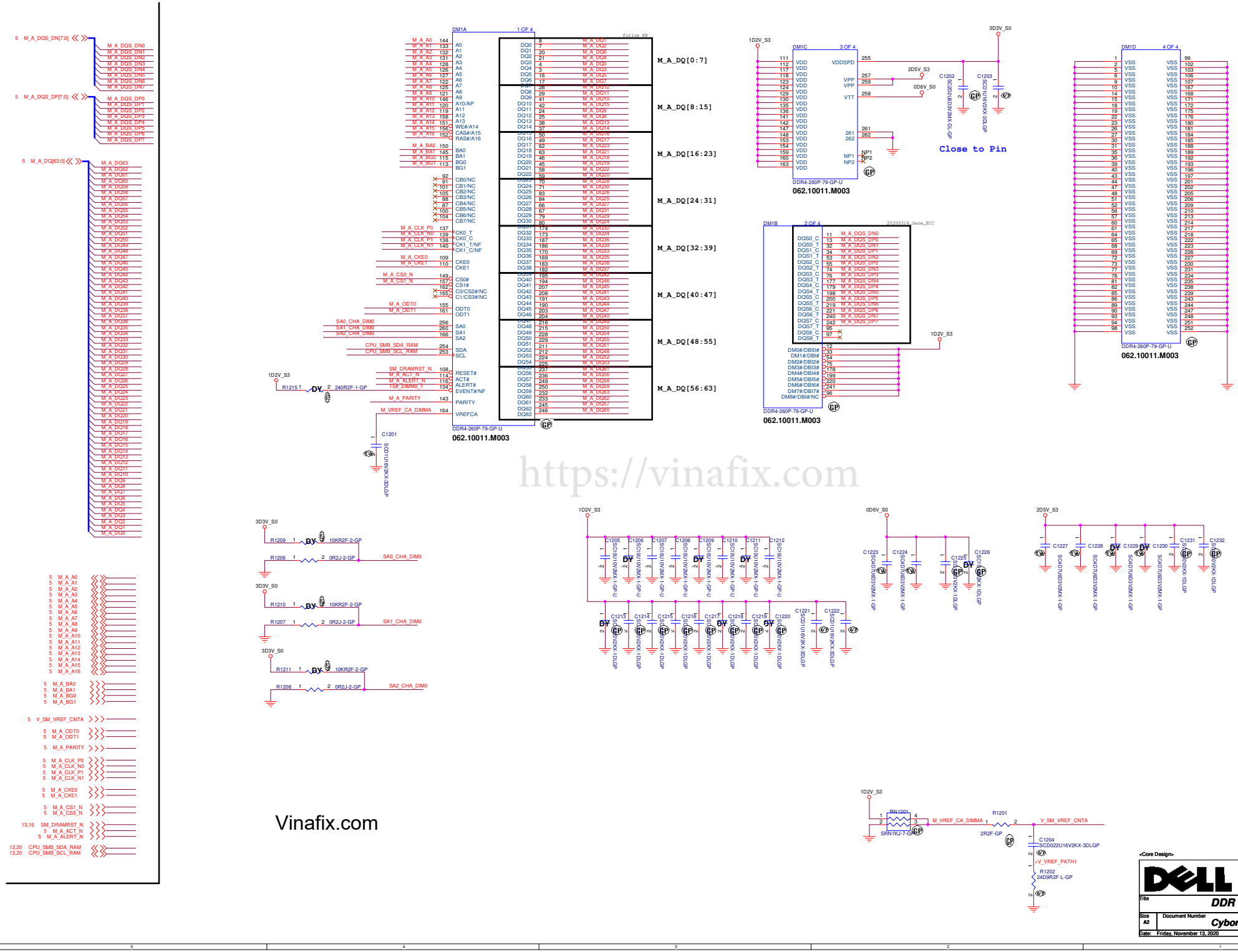
Original Ref.

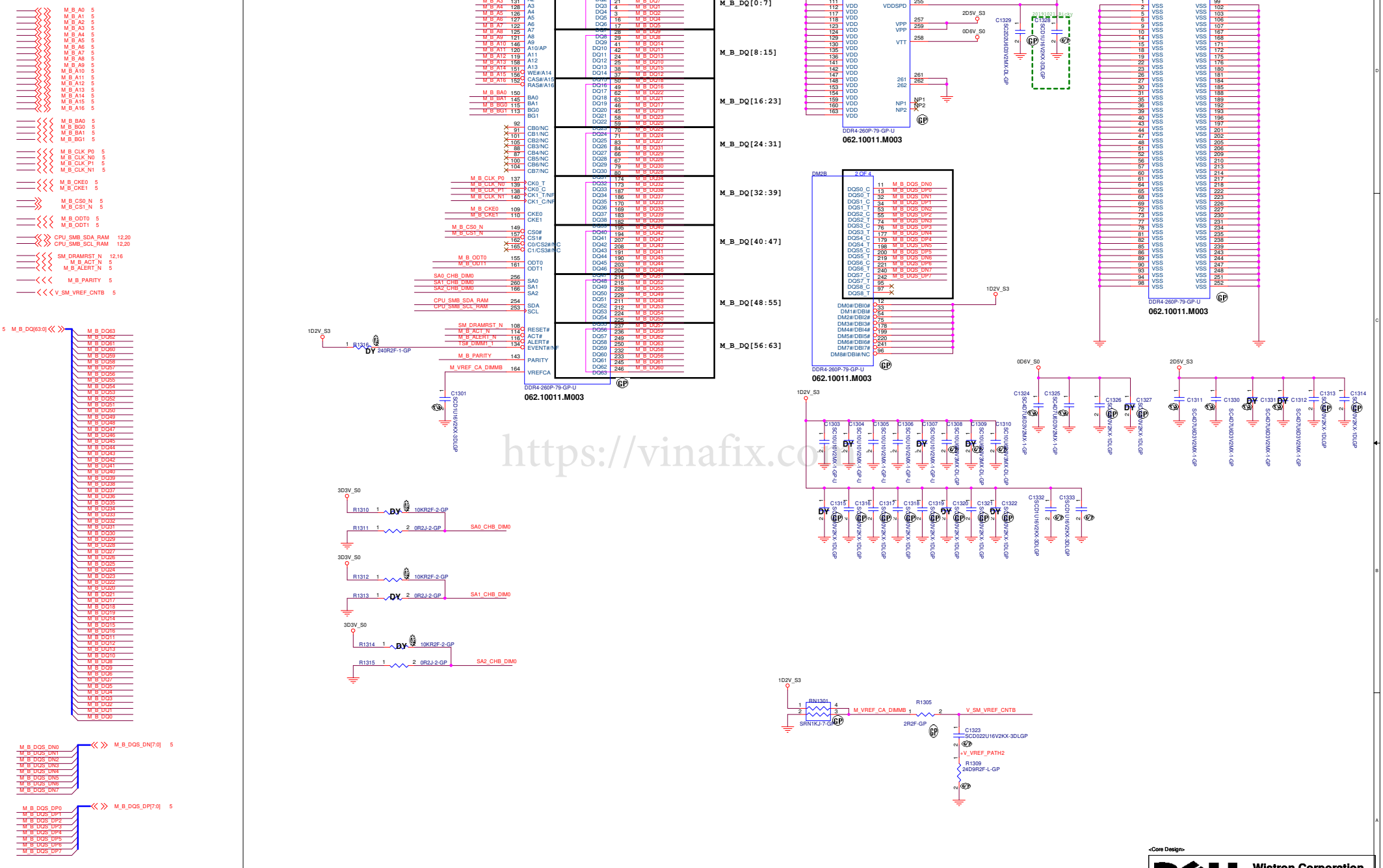
GPP_C5	SPI0_MOSI	GPP_H15 / SML3ALERT#	GPP_J2/ CNV_BRI_DT	SPI0_IO2	GPP_R2 / HDA_SDO	GPP_J4/ CNV_RGI_DT	GPP_G13/ TBT_LSX0_VCC config	GPP_G15/ TBT_LSX1_VCC config	GPP_G9/ TBT_LSX2_VCC config
ESPI LOW :ESPI IS DISABLED High :ESPI IS Enabled WEAK INTERNAL PD	External pull-up is required. Recommend 4.7 kohm pull up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	JTAG ODT DISABLE HIGH :JTAG ODT DISABLED LOW :JTAG ODT ENABLED	XTAL SELECT-1 HIGH -> 24 MHz LOW -> 38.4 MHz	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.		This strap does not have an internal pull-up or pull-down. A weak external pull-up is required. 0=>Integrated CNVi enabled. 1=>Integrated CNVi disabled. Note: When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap low to enable CNVi interface.			

GPP_G11/ TBT_LSX3_VCC config	SPI0_IO3	DBG_PMODE	GPP_B18/ GSPI0_MOSI	GPD7	GPP_B14 / SPKR	GPP_C2/ SMBALERT#	GPP_B23/ SML1ALERT#	GPP_H12/ SML2ALERT#	GPP_B22/ GSPI1_MOSI
	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	This strap has a 20 kohm ± 30% internal pull-up. This strap should sample high. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-up is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.	No REBOOT HIGH :NO REBOOT LOW :REBOOT ENABLED WEAK INTERNAL PD	This strap has a 20 kohm ± 30% internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. Notes: 1. The internal pull-down is disabled after DSW_PWROK is high. 2. This signal is in the DSW well.					

<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: CPU (STRAP)			
Size: A2	Document Number: Cyborg N5-H		Rev: X00
Date: Friday, November 13, 2020	Sheet 11 of 106		





<Core Design>

Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DDR (DDR4-CHB)		
Size: A2	Document Number: Cyborg N5-H	Rev: X00
Date: Friday, November 13, 2020	Sheet 13 of 106	

<Core Design>

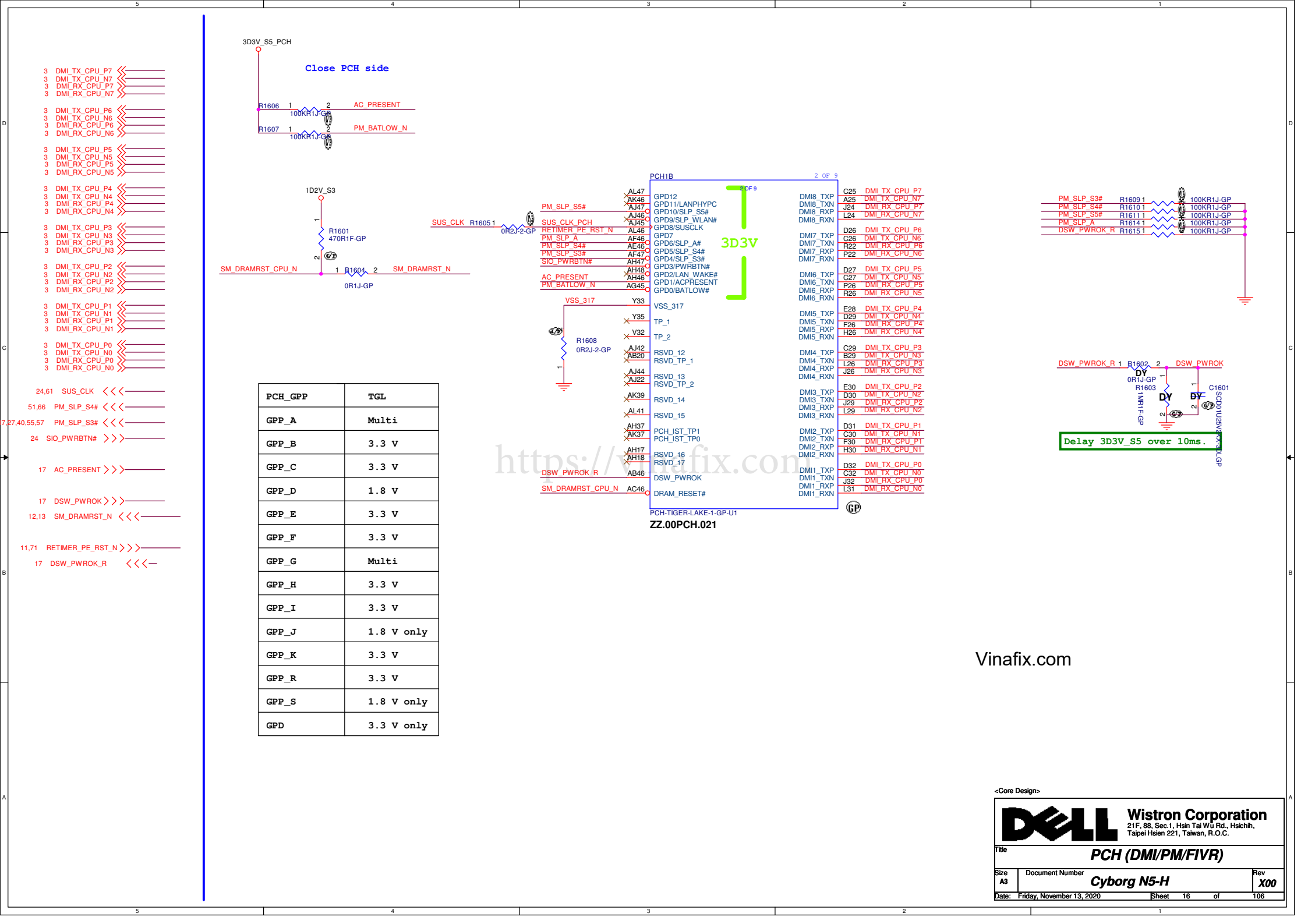
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR (RSVD) (DDR4-CHA1)***

Size	Document Number	Rev
A4	***Cyborg N5-H***	***X00***

Date: Friday, November 13, 2020 Sheet 14 of 106

Wistron Corporation
DDR (RSH0) (DDR4-CHB1)
Cyborg M5-H
Sheet



PCH_GPP	TGL
GPP_A	Multi
GPP_B	3.3 V
GPP_C	3.3 V
GPP_D	1.8 V
GPP_E	3.3 V
GPP_F	3.3 V
GPP_G	Multi
GPP_H	3.3 V
GPP_I	3.3 V
GPP_J	1.8 V only
GPP_K	3.3 V
GPP_R	3.3 V
GPP_S	1.8 V only
GPD	3.3 V only

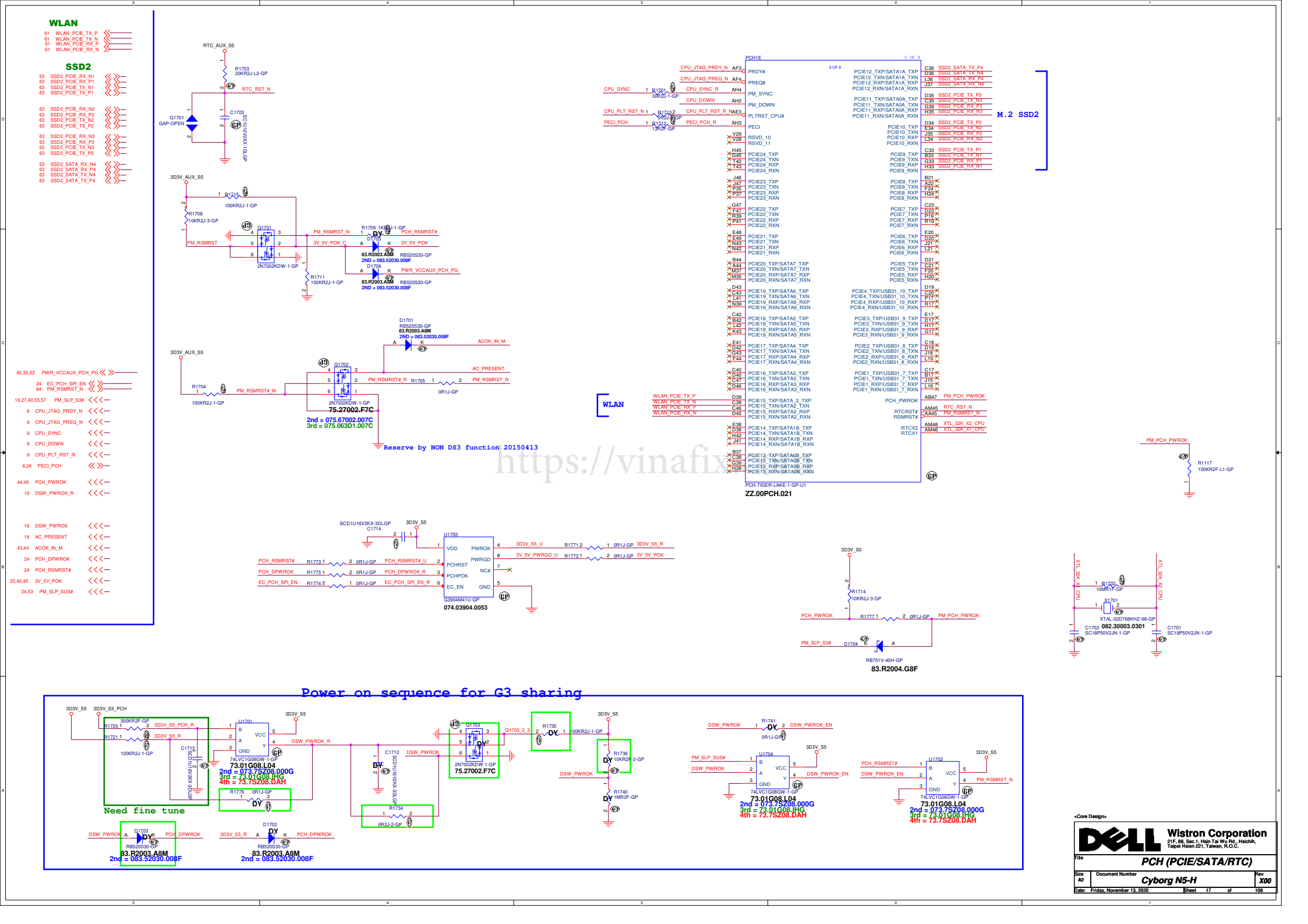
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DMI/PM/FIVR)

Size: A3 | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 16 of 106

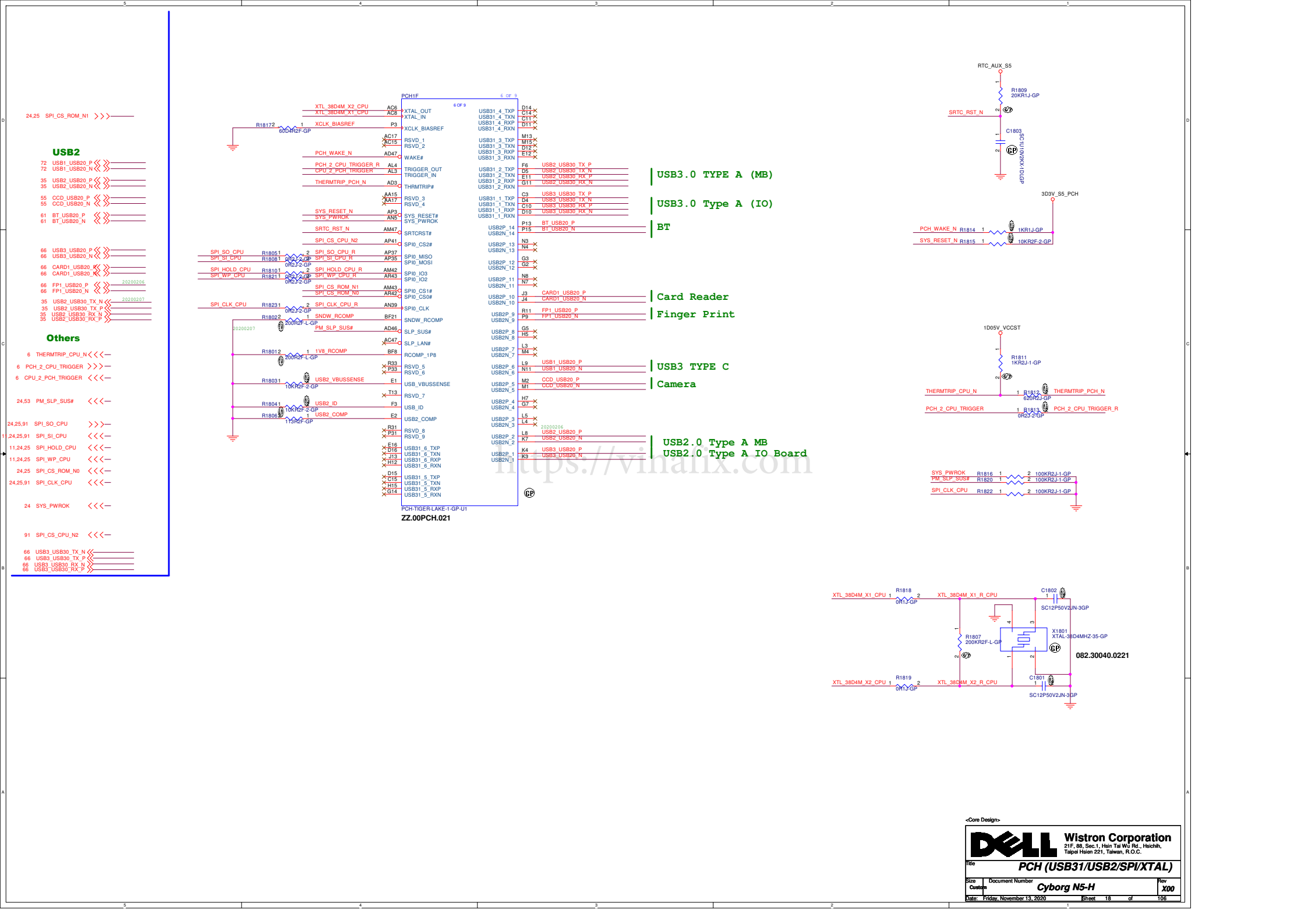


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCIE/SATA/RTC)

Size: A2 | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 17 of 106


USB2
Others
PCH1F
6 OF 9
PCH-TIGER-LAKE-1-GP-U1
ZZ.00PCH.021
USB3.0 TYPE A (MB)
USB3.0 Type A (IO)
BT
Card Reader
Finger Print
USB3 TYPE C
Camera
USB2.0 Type A MB
USB2.0 Type A IO Board
RTC_AUX_S5
3D3V_S5_PCH
1D05V_VCCST
082.30040.0221
https://vinafix.com
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (USB31/USB2/SPI/XTAL)
Cyborg N5-H
X00
Friday, November 13, 2020

SSD

63 SSD2_CLK_CPU_P
63 SSD2_CLK_CPU_N

63 SSD_CLK_CPU_P
63 SSD_CLK_CPU_N

dGPU

76 GFX_CLK_CPU_P
76 GFX_CLK_CPU_N

WLAN

61 WLAN_CLK_CPU_P
61 WLAN_CLK_CPU_N

6,19 CPU_WAKE

CNVi

61 CNV_WT_DP1
61 CNV_WT_DN1
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_CLKP
61 CNV_WT_CLKN

61 CNV_WR_DP1
61 CNV_WR_DN1
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_CLKP
61 CNV_WR_CLKN

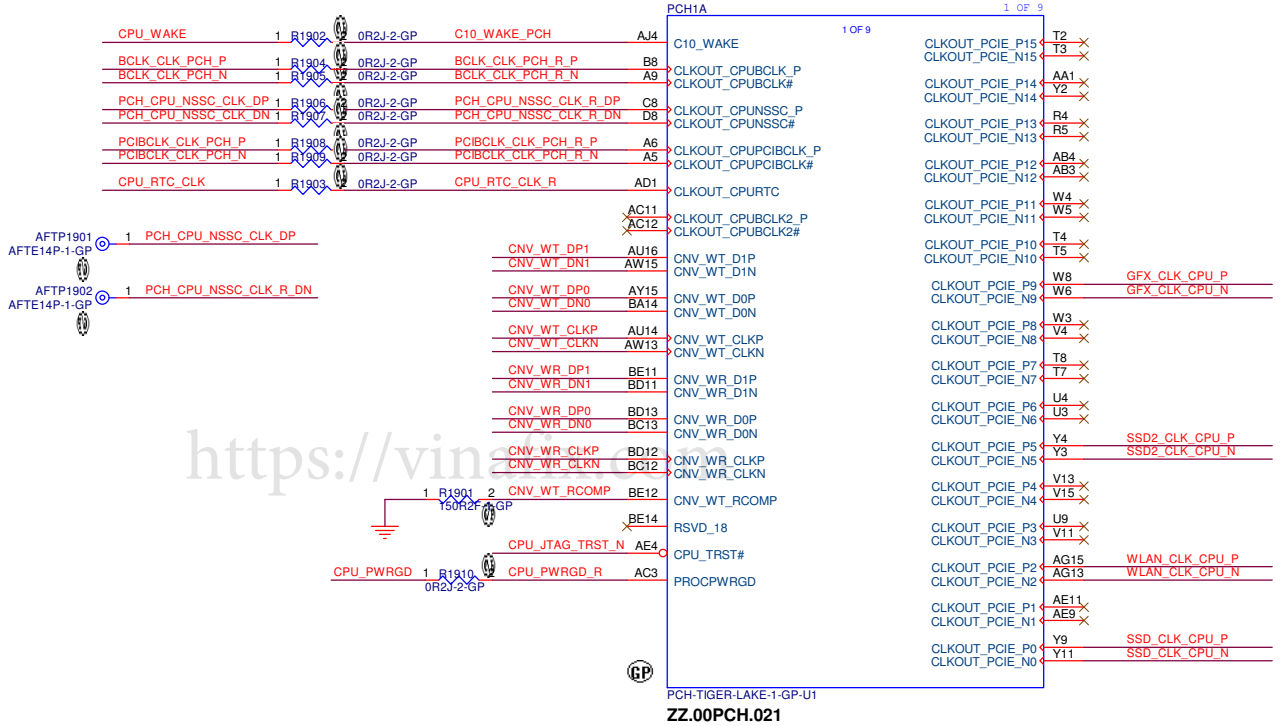
6 CPU_JTAG_TRST_N
6 CPU_PWRGD
6,19 CPU_WAKE

6 BCLK_CLK_PCH_P
6 BCLK_CLK_PCH_N

6 PCH_CPU_NSSC_CLK_DP
6 PCH_CPU_NSSC_CLK_DN

6 PCIBCLK_CLK_PCH_P
6 PCIBCLK_CLK_PCH_N

6 CPU_RTC_CLK



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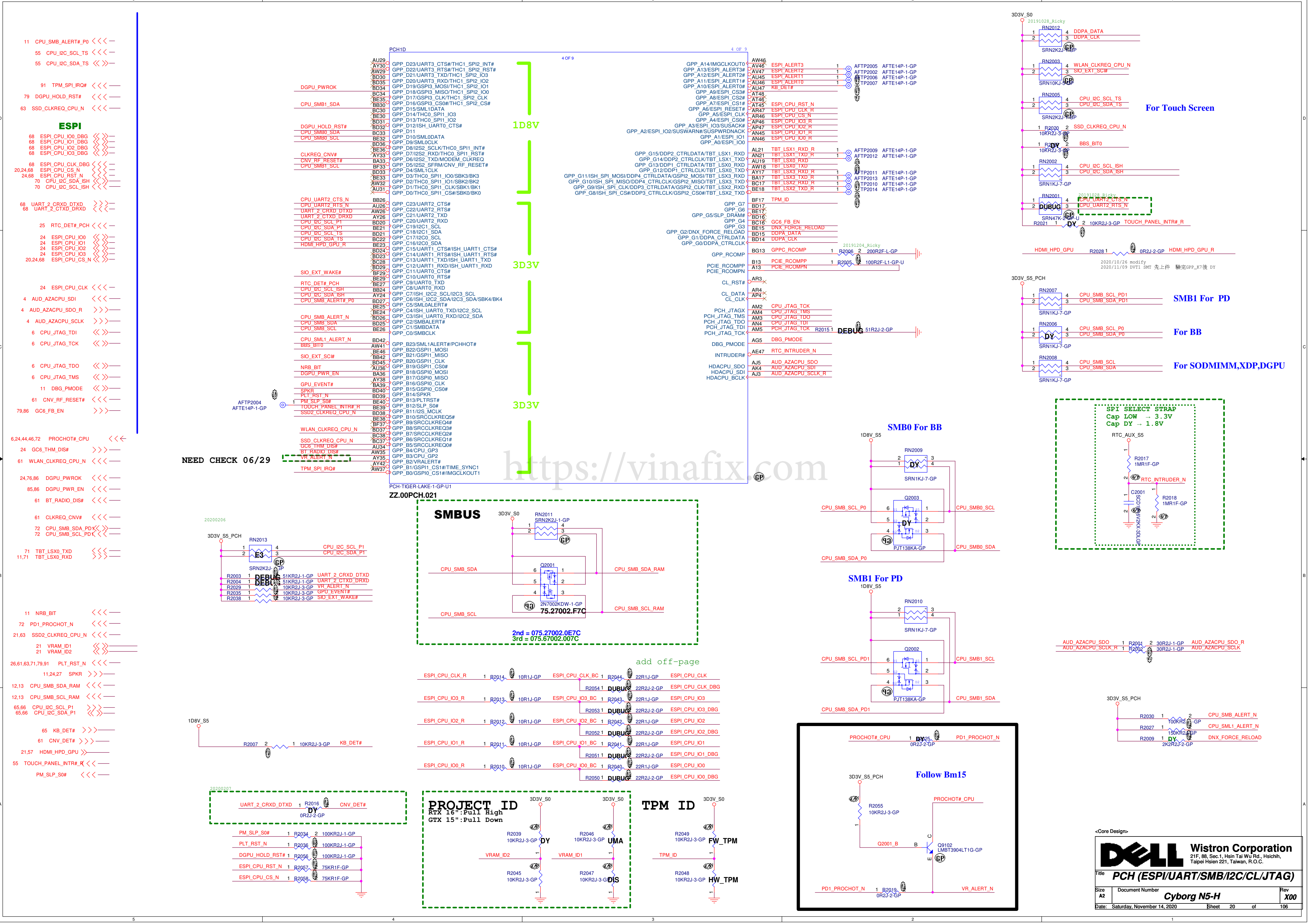
<Core Design>

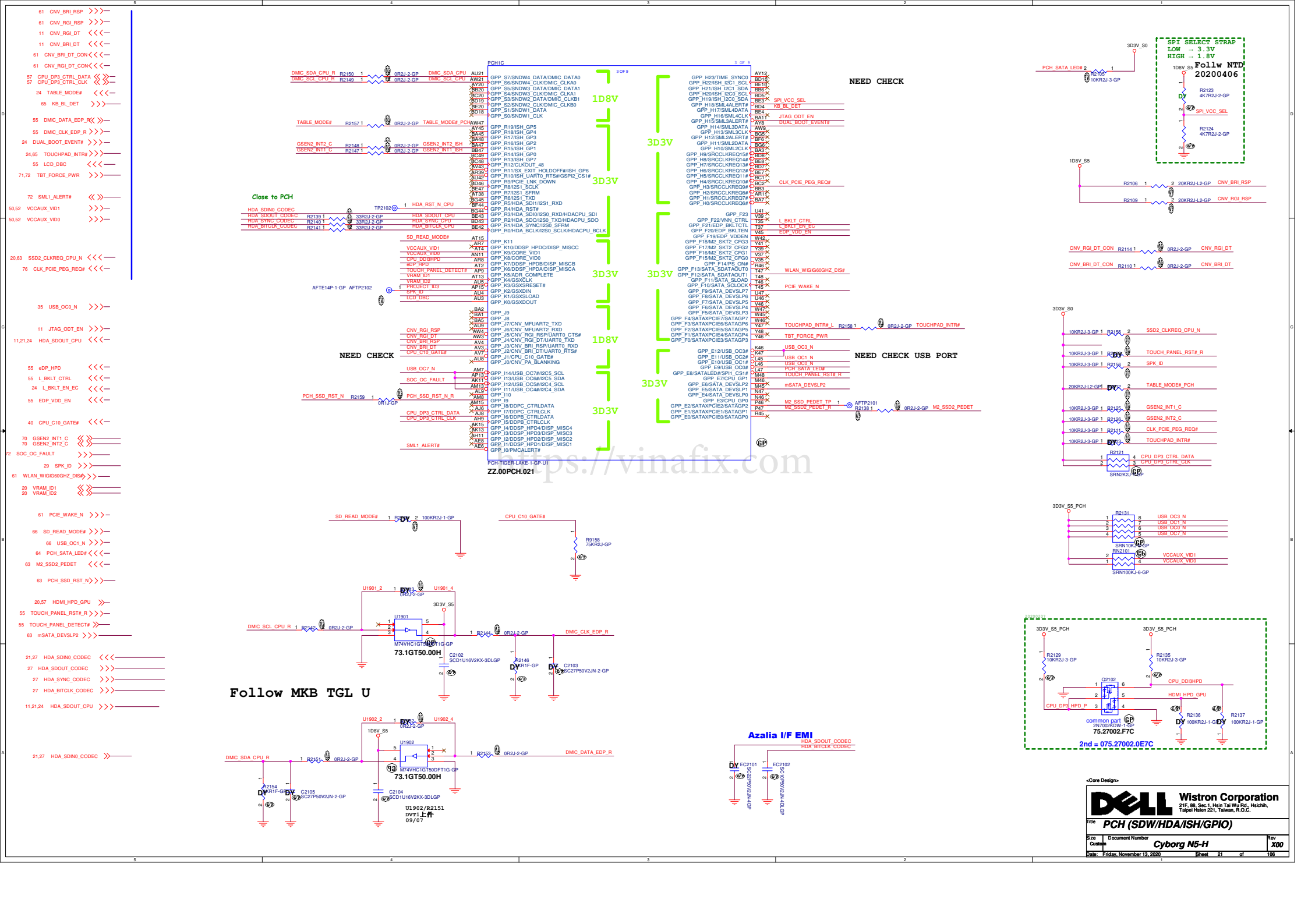
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

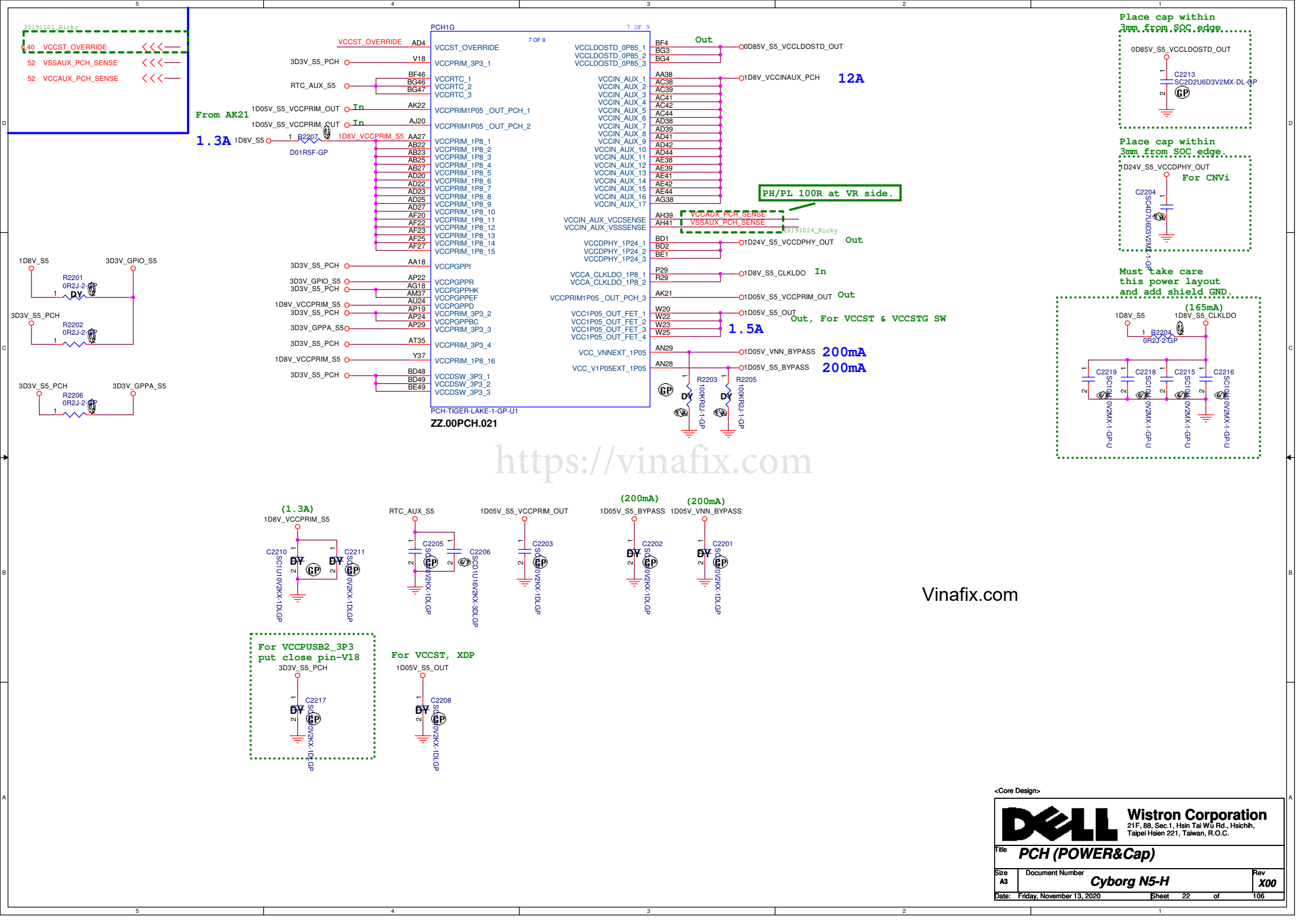
Title: PCH (CLK/CNVi)

Size: A3 | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 19 of 106


ESPI
PCH1D
4 OF 9
1D8V
3D3V
3D3V
NEED CHECK 06/29
PCH-TIGER-LAKE-1-GP-U1
ZZ.00PCH.021
SMBUS
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.27002.0E7C
3rd = 075.67002.007C
add off-page
PROJECT ID
RTX 16":Pull High
GTX 15":Pull Down
TPM ID
FW_TPM
HW_TPM
UMA
DIS
For Touch Screen
SMB1 For PD
For BB
For SODMIMM,XDP,DGPU
SPI SELECT STRAP
Cap LOW → 3.3V
Cap DY → 1.8V
SMB0 For BB
SMB1 For PD
Follow Bm15
2020/10/26 modify
2020/11/09 DVT1 SMT 先上件 驗完GPP_K7後 DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (ESPI/UART/SMB/I2C/CL/JTAG)
Size A2
Document Number
Cyborg N5-H
Rev X00
Date: Saturday, November 14, 2020
Sheet 20 of 106

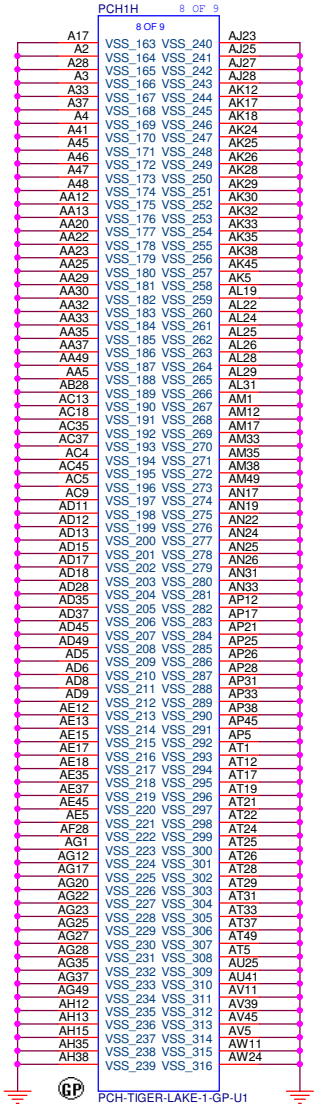

PCH1C
PCH-TIGER-LAKE-1-GP-U1
ZZ.00PCH.021
NEED CHECK
NEED CHECK USB PORT
Close to PCH
SPI SELECT STRAP
LOW → 3.3V
HIGH → 1.8V
Follw NTD 20200406
Follow MKB TGL U
73.1GT50.00H
Azalia I/F EMI
U1902/R2151
DVT1_F-ff
09/07
2nd = 075.27002.0E7C
common part
2N7002KDW-7-GP
75.27002.F7C
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (SDW/HDA/ISH/GPIO)
Cyborg N5-H
Date: Friday, November 13, 2020
Sheet 21 of 106



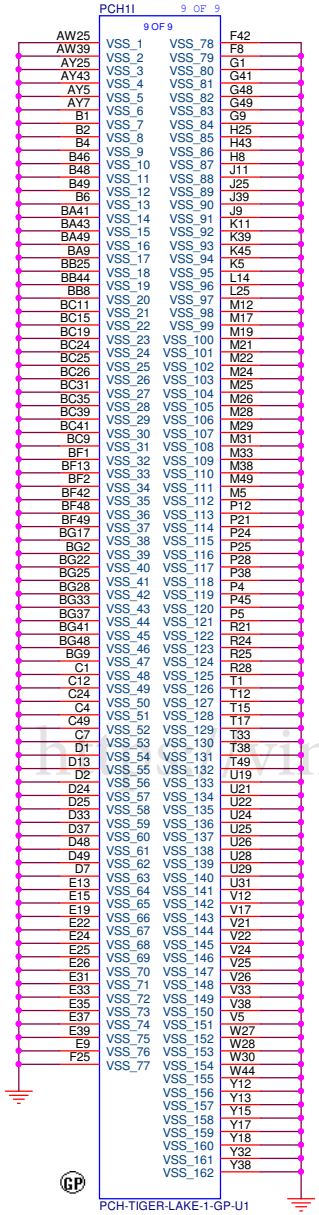
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (POWER&Cap)	
Size A3	Document Number: Cyborg N5-H	Rev: X00
Date: Friday, November 13, 2020	Sheet 22 of 106	



ZZ.00PCH.021



ZZ.00PCH.021

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size: A3 | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 23 of 106

Main Func = KBC

#	MODEL_ID(GPIO202)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	GTX 15" DIS	100K	10K	3
2	GTX 16" DIS	100K	17.8K	2.801
3	RTX 16" DIS	100K	27K	2.598
4		100K	37.4K	2.402
5	GTX 16" UMA	100K	49.9K	2.201
6	GTX 15" UMA	100K	64.9K	2.001
7		100K	82.5K	1.808
8		100K	107K	1.594
9		100K	154K	1.299
10		100K	200K	1.1

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

Vinafix.com

TABLE 2-6: STRAP PINS

Pin Name	Strap Name	Strap define and value	I/O Power rail
GPIO055/SHD_CS 0#	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for BootNote 2 0=Use the eSPI Flash Channel for Boot Note 1	VTR2

Note 1: If the eSPI Flash Channel is used for booting, i.e., eSPI Master Attached Flash Sharing (MAFS), the GPIO055/PWM2/SHD_CS0# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. In addition, the GPIO016/GPT-P_IN1/SHD_IO3/ICT3 pin must be used as DSW_PWROK.This pin will also be driven high by the boot ROM code to support Deep Sleep Well timing requirements

2: If the Shared SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

3: The comparator strap option is an optional feature that may be enabled in OTP to enable the Boot ROM to configure and lock the Comparator 0 pins. If the feature is enabled in OTP, and external pull-up/pull-down is required to determine the default comparator behavior. If the strap option is not enabled in OTP, the CMP_STRAP# is not supported and no external pull-up or pull-down required. Application firmware may enable the comparator if supported by the specific package.

2.4.16 SHARED SPI FLASH CHIP SELECT PULL-UP RESISTOR RECOMMENDATION

GPIO055/SHD_CS0# pin is used to determine the boot source (eSPI Flash channel or shared SPI). In addition, the GPIO055/SHD_CS0# pin is used as an indication that the Shared SPI is powered. This pin must be at a high level for the device to load code from the SPI Flash device.

There is presently a requirement for a pull-up resistor on the SHD_CS0# pin on the board if the Shared SPI flash interface is used so that the SPI CS0# is detected hich while RSMRST# is low.

Wistron Corporation
KBC MEC1515
Cyborg N5-H
X00

SSID = Flash.ROM **SPI FLASH ROM (32M byte) for PCH**

R2521.R2524.R2518.R2526.R2520 R2523.R2517.R2525.R2519.R2522	
SPI ROM	33 ohm 64.33R05.6DL
SHARE ROM	15 ohm 63.15034.1DL

18,24 SPI_CS_ROM_N0
18,24,91 SPI_SO_CPU
11,18,24 SPI_WP_CPU
11,18,24 SPI_HOLD_CPU
18,24,91 SPI_CLK_CPU
11,18,24,91 SPI_SI_CPU
18,24 SPI_CS_ROM_N1
20 RTC_DET#_PCH
24 RTCRST_ON
24 VCCDSW_EN#
17,40,45 3V_5V_POK
53 3V_5V_DSW_OK

3D3V_S5_PCH
C2501 SC10U6D3V3MX-DL-GP
C2502 SCD1U16V2KX-3DLGP
R2501 4K7R2J-2-GP
SPI25
CS# DO/IO1 IO2 GND VCC IO3 CLK DI/IO0
W25Q256JVEIQ-GP
072.25256.0N01
R2518 R2517 33R2J-2-GP
R2519 R2520 R2521 33R2J-2-GP
SPI_CS_ROM_N0 SPI_SO_ROM SPI_WP_ROM SPI_HOLD_ROM SPI_CLK_ROM SPI_SI_ROM
SPI_HOLD_CPU SPI_CLK_CPU SPI_SI_CPU
R2502 4K7R2J-2-GP DY
SPI251
CS# SO/SIO1 SIO2 GND VCC SIO3 SCLK SI/SIO0
MX25L12872FM2I-10G-GP
072.25128.0D61
R2526 R2525 R2522 R2523 R2524
SPI_CS_ROM_N1 SPI_SO_ROM SPI_WP_ROM SPI_HOLD_ROM SPI_CLK_ROM SPI_SI_ROM

Main Func = RTC

RTC GEN9

3D3V_S5
R2509 100KR2J-1-GP
VCCDSW_EN#
C2505 SC1U10V2KX-1GP DY
3V_5V_POK
D2502 BAT54A-11-GP
3V_5V_DSW_OK
R2510 10KR2J-3-GP
75.BAT54.07D
2ND = 75.00054.07D
U2502 RT9742CGJ5-GP
EN/EN# VIN FLG# GND VOUT
C2506 SC1U10V2KX-1GP
074.09742.0A9F
2nd = 074.51712.009F

3D3V_RTC_AUX
Q2501 PJA3413-1-GP
084.03413.0031
2nd = 084.02301.0031
RTC_AUX_S5
R2514 4K7R2J-2-GP
RTC_3P3_EN_D
Q2502 2N7002K-2-GP-U
84.2N702.J31
RTCRST_ON
R2512 1MR2J-1-GP
RTC_3P3_EN_G
R2513 100KR2J-1-GP
C2504 SCD022U16V2KX-3DLGP

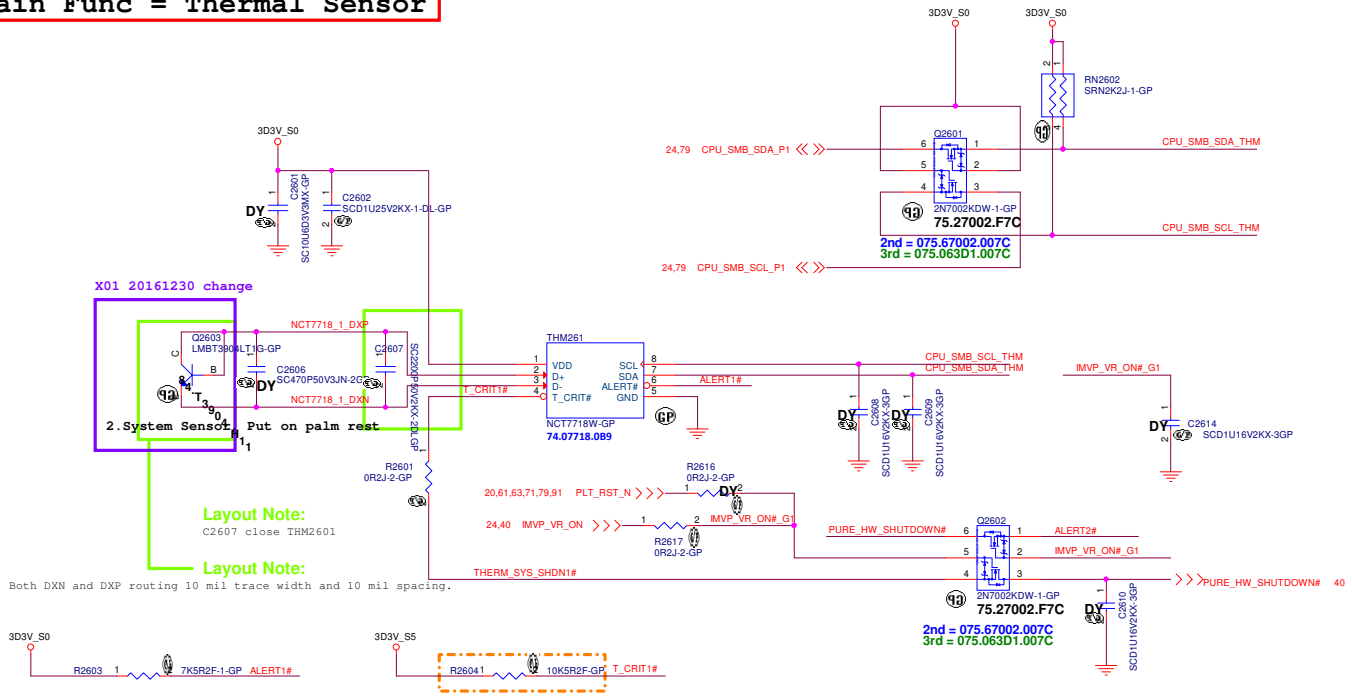
3D3V_AUX_S5
R2505 0R2J-2-GP
3D3V_RTC_SYS
R2503 47KR2F-GP DY
D2501 BAT54C-12-GP
75.00054.A7D
3D3V_RTC_AUX
C2503 SC1U10V2KX-1DLGP
BATT_RTC
3D3V_S5_PCH
R2541 10KR2J-3-GP
Q2505 2N7002K-2-GP-U
84.2N702.J31
R2504 10MR2J-L-GP
RTC_DET#_PCH

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

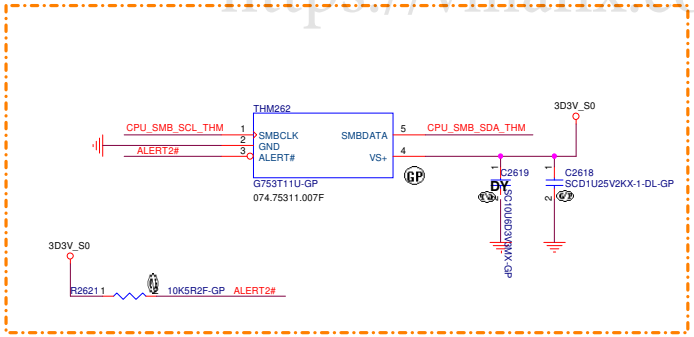
Title: Flash/RTC
Size: Custom
Document Number: Cyborg N5-H
Rev: X00
Date: Friday, November 13, 2020
Sheet 25 of 106

Main Func = Thermal Sensor

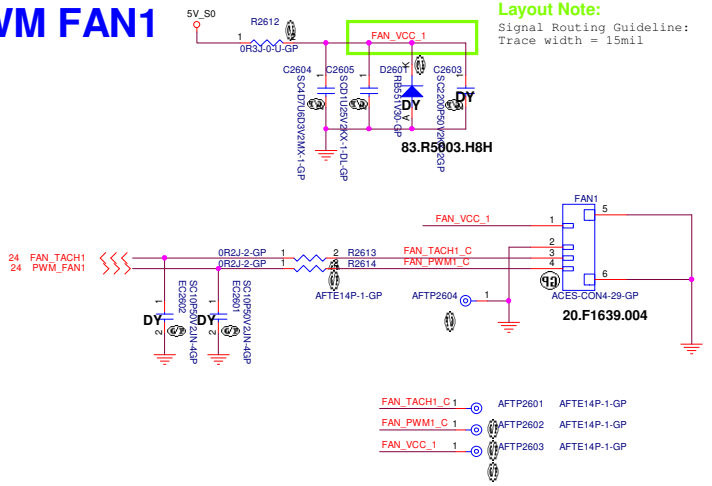


T_CRIT# ;ALERT# :Open-drain output pin with 12 mA sink capability

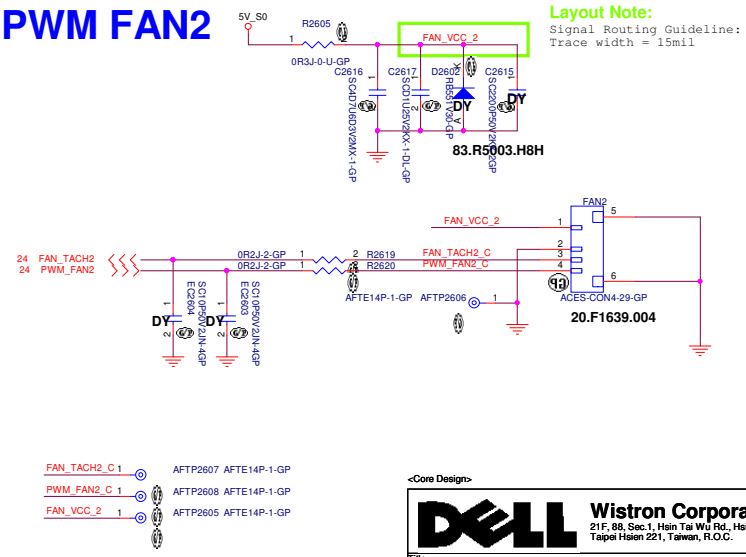
TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



PWM FAN1



PWM FAN2



<Core Design>

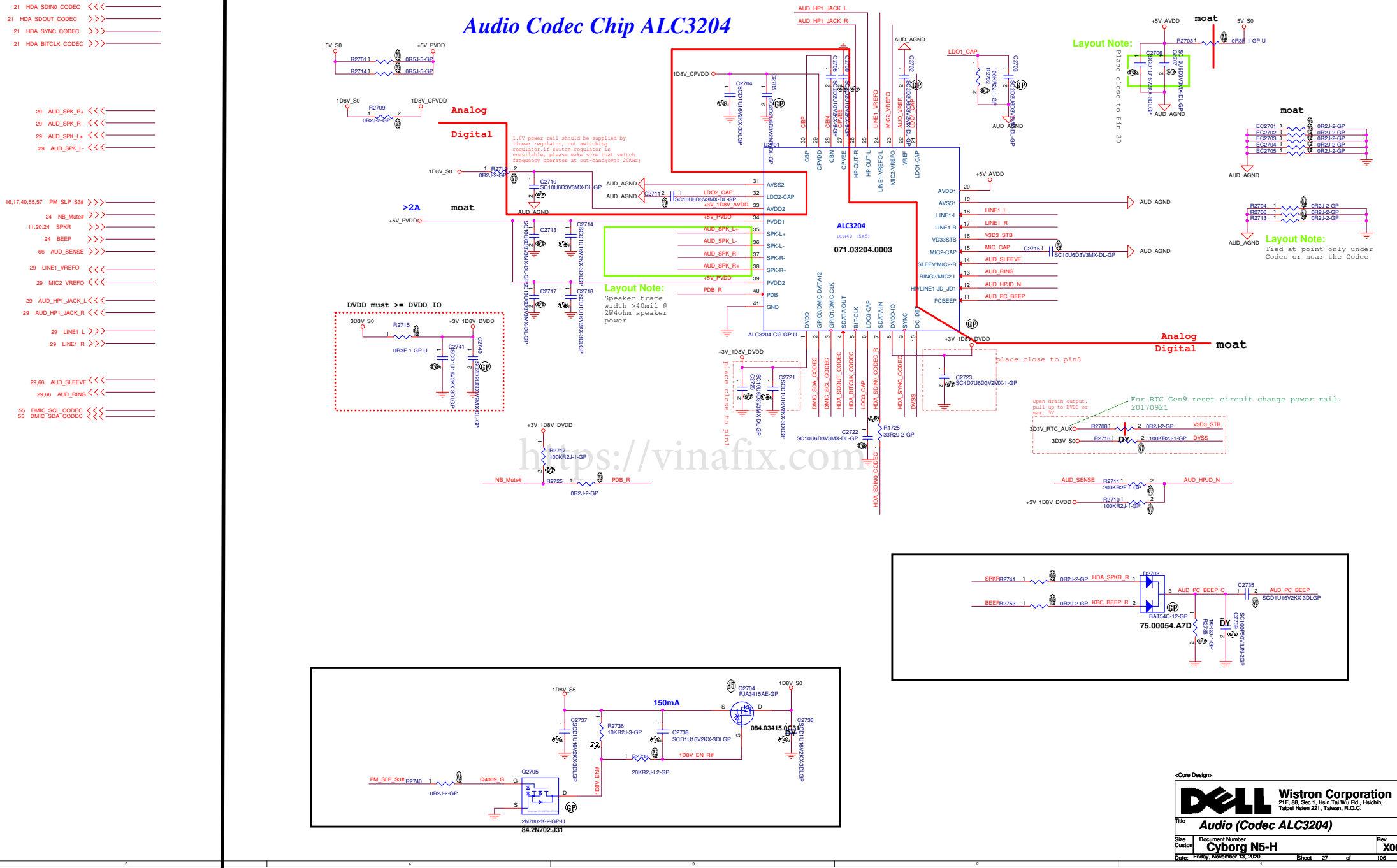
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (Thermal/Fan)

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 26 of 106

Main Func = Audio



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (Codec ALC3204)

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 27 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Audio (RSVD)

Size	Document Number	Rev
A4	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 28 of 106

Main Func = Audio

27 AUD_SPK_L+
27 AUD_SPK_L-
27 AUD_SPK_R+
27 AUD_SPK_R-

21 SPK_ID
27,29 LINE1_L
27,29 LINE1_R

From Codec

27 MIC2_VREFO

27 AUD_HP1_JACK_L
27,29 LINE1_L
27,29 LINE1_R
27 AUD_HP1_JACK_R

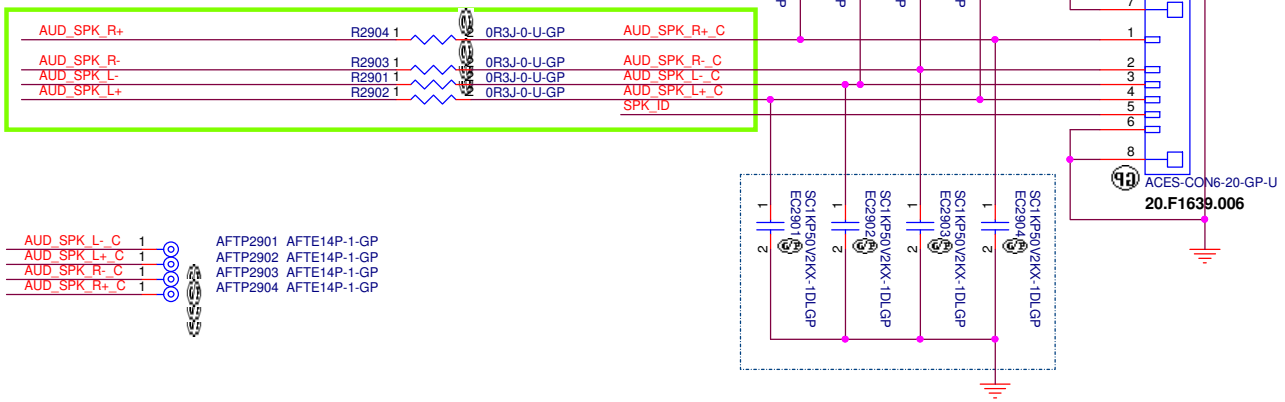
27 LINE1_VREFO

To IO Board

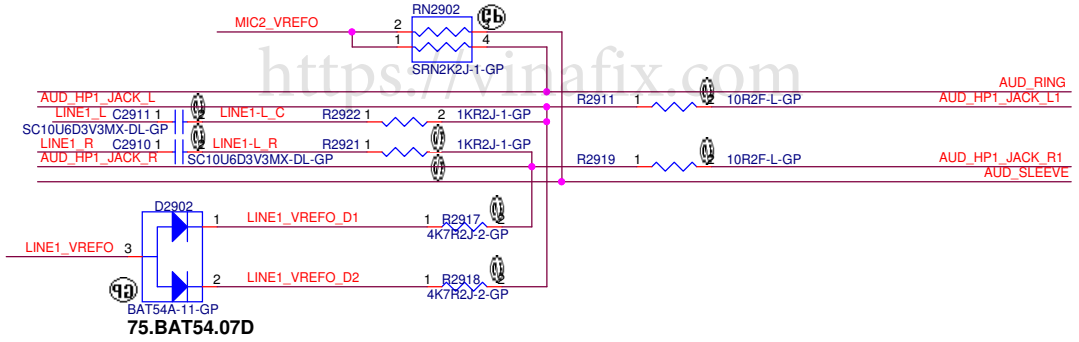
27,66 AUD_RING
66 AUD_HP1_JACK_L1
66 AUD_HP1_JACK_R1
27,66 AUD_SLEEVE

Speaker

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power



12/17 Clark move close to connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio (HP/SPK/MIC Jack)

Size	Document Number	Rev
Custom	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 29 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Audio (RSVD)

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 30 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN (RSVD)

Size	Document Number	Rev
Custom	Cyborg N5-H	X00

Date: Friday, November 14, 2008 Sheet 31 of 100

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LAN (RSVD)***

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 32 of 106

SSID = Card Reader

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

Size	Document Number	Rev
A4	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 33 of 106

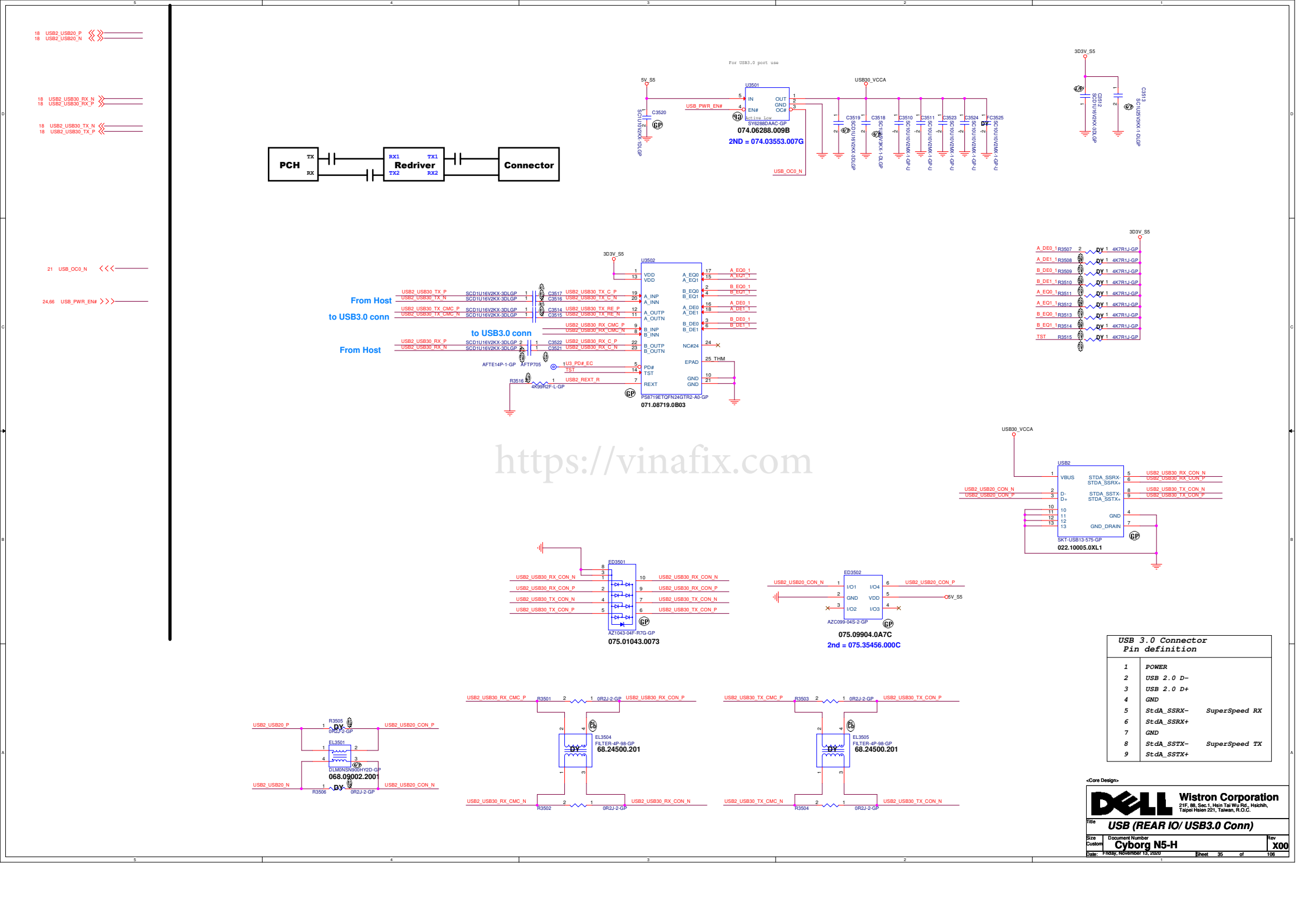
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)

Size	Document Number	Rev
A	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 34 of 106



USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB (REAR IO/ USB3.0 Conn)

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 35 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 36 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB (RSVD)***

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 37 of 106

SSID = USB3.0 Redrivere

<Core Design>

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Title: *USB (RSVD)*

Size	Document Number	Rev
A4	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 38 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sequence(RSVD)*

Size	Document Number	Rev
Custom	Cyborg N5-H	X00
Date: Friday, November 13, 2020	Sheet 39 of 106	

Power Sequence

5V_S0

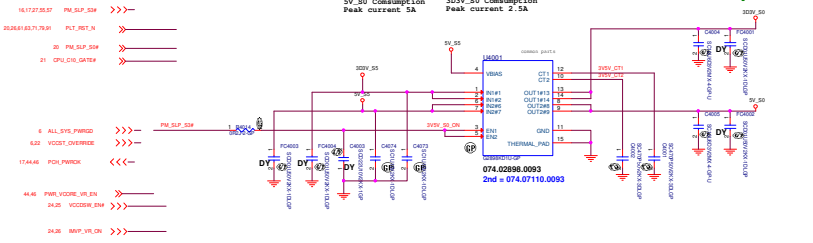
5V_S0 Consumption
Peak current 5A

3D3V_S0

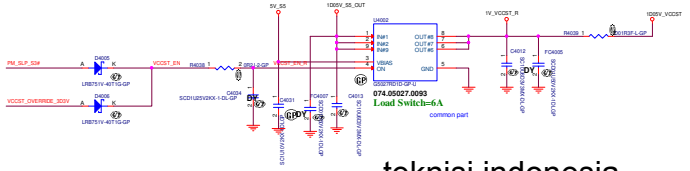
3D3V_S0 Consumption
Peak current 2.5A

ROSA Run Power

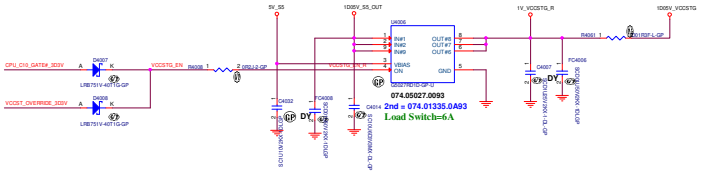
6A Continuous Switch Current per channel

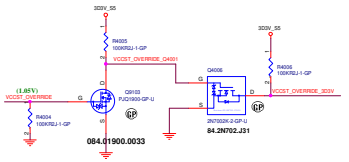


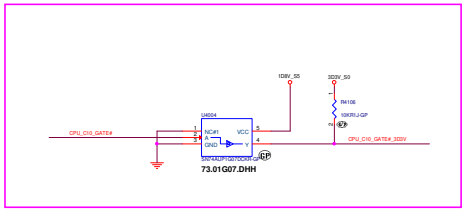
1V_VCCST

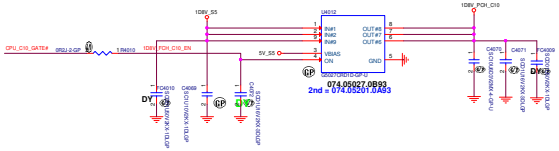


1V_VCCSTG

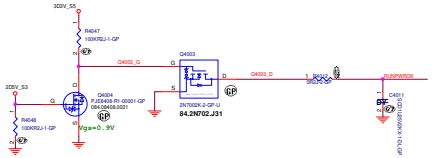






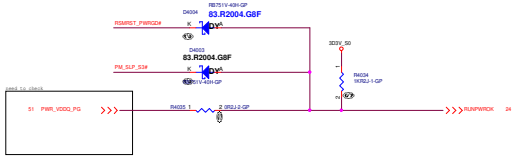


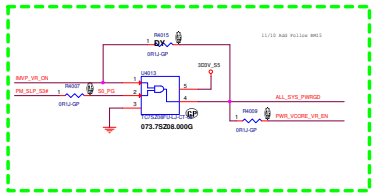
V_TREE



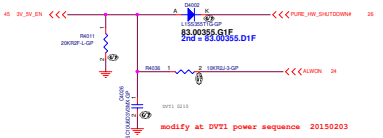
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	20	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250uA	0.3	0.64	0.9	V

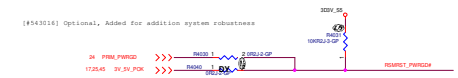
Power Sequence / Pull High PWRGD





Non VNN-Connect to EC PRIM_PWRGD





Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Sequence (Power on)
Size: Document Number: Cyborg N5-H
Rev: X00
Date: Friday, November 13, 2015
Sheet 45 of 105

Main Func = Power & Sequence

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sequence (DS3/S0ix)*

Size: A3 | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 41 of 106

<Core Design>

Wistron Corporation
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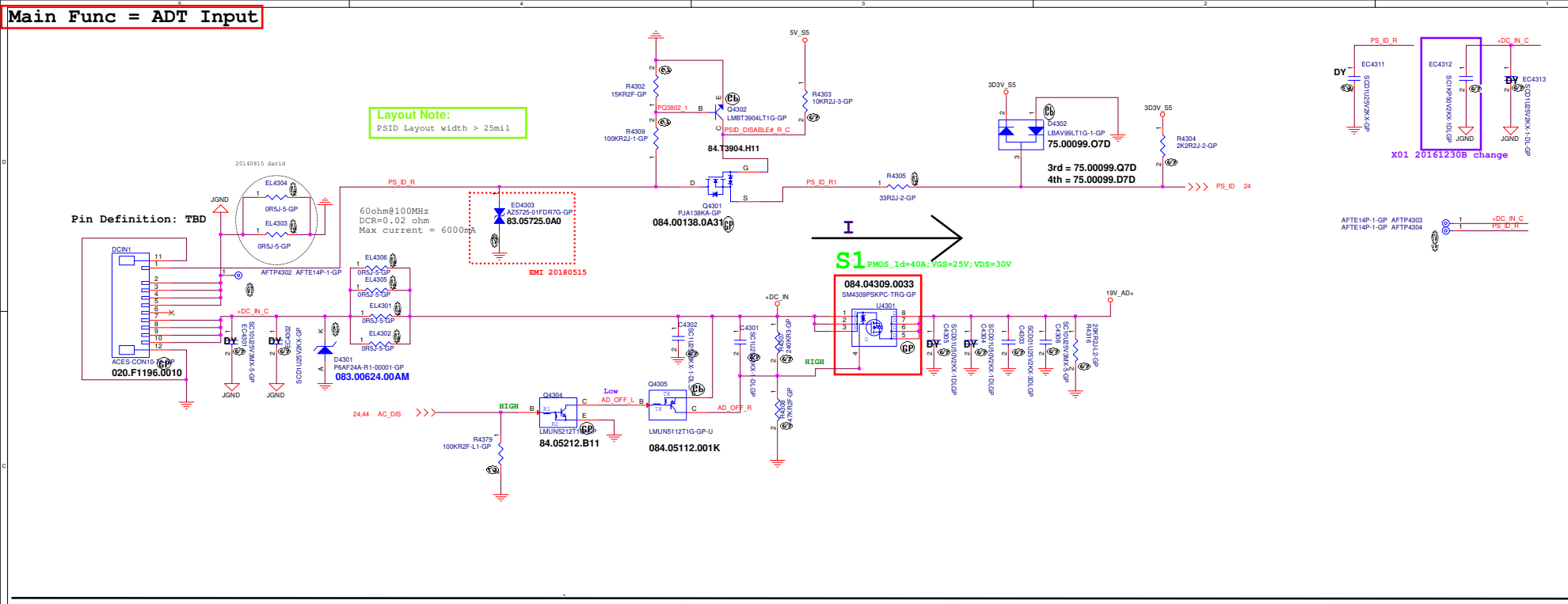
Title
INT IO (Current meter)

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 42 of 106

Main Func = ADT Input



Main Func = M-BAT Input

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: INT IO (ATX/ DC/ BATT Conn)
Size: Custom | Document Number: Cyborg N5-H | Rev: X00
Date: Friday, November 13, 2020 | Sheet 43 of 106

ISL9538C For Charger

Main Func = Charger

OFFPAGE

EE needs check it!!

I2C form EC

To EC

From NXP ACK

OVP

E3

Adaptor IN

Charger IN

+SDC_IN(TypeC In)

SYSTEM 19V

Battery IN

S2 PMOS_Id=40A; VGS=25V; VDS=30V

084.04309.0033

075.07321.0073

Syntec| 12.6mm x 13.8mm x 3.5mm
DCR: 7.2m~ 8mOhm
Idc : 16A , Isat : 29A

084.21307.0037

+3D3V_VDD_DCIN

Vcore_OVP

0523

PU 3V3_AON_S0 on GPU side

PU +VCCSTG = 1.0 V on CPU side

TypeC Prochot
Follow customer circuits.

need to check the function

CHECK EE
follow customer circuits.

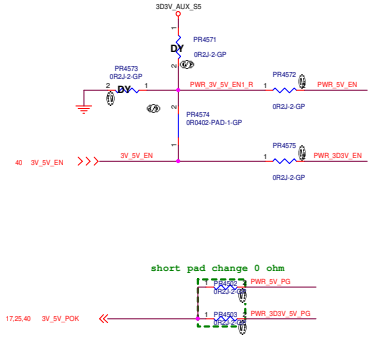
TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ) MIN	TYP 1%	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ACLIm&L Reg(A)
0			1	733kHz	No	0.476
8.45				733kHz	No	1.5
14.7				1MHz	No	1.5
21.0				1MHz	No	0.476
28.0				733kHz	Yes	0.476
35.7				733kHz	Yes	1.5
43.2			2	733kHz	Yes	1.5
52.3				733kHz	Yes	0.476
61.9				1MHz	No	0.476
71.5				1MHz	No	1.5
82.5				733kHz	No	1.5
93.1				733kHz	No	0.476
105			3	733kHz	No	0.476
118				733kHz	No	1.5
133				1MHz	No	1.5
147				1MHz	No	0.476
162				733kHz	Yes	0.476
178				733kHz	Yes	1.5
196			4	733kHz	Yes	1.5
215				733kHz	Yes	0.476
237				1MHz	No	0.476
261				1MHz	No	1.5
287				733kHz	No	1.5
316				733kHz	No	0.476
348			1	733kHz	No	0.476

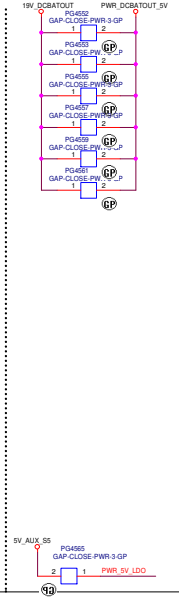
Wistron Corporation
Power (Charger_ISL9538)
Cyborg N5-H

SSID = PWR.Plane.Regulator_5V

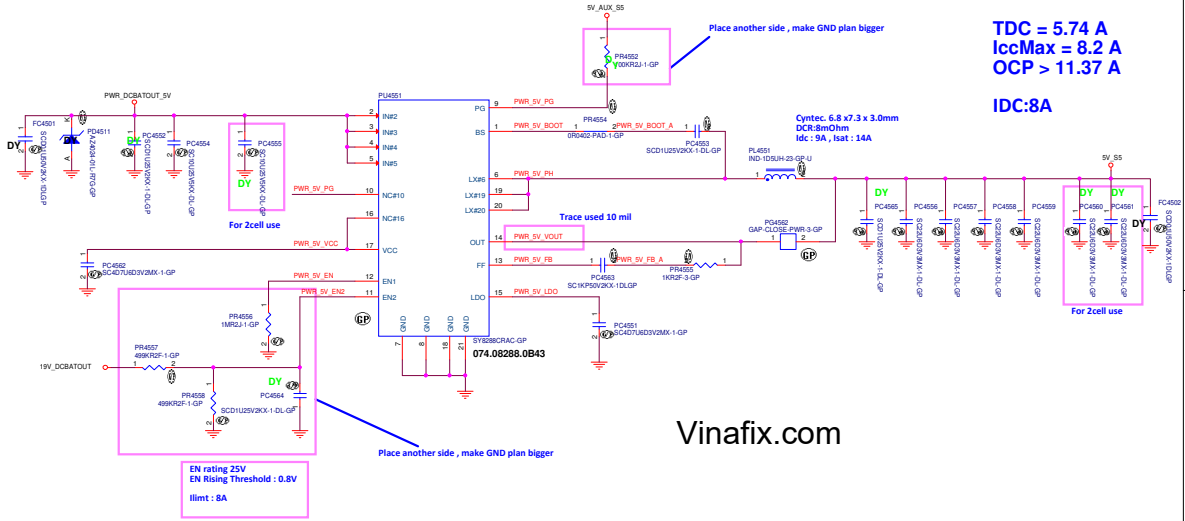
OFFPAGE-Signal



OFFPAGE-GAP



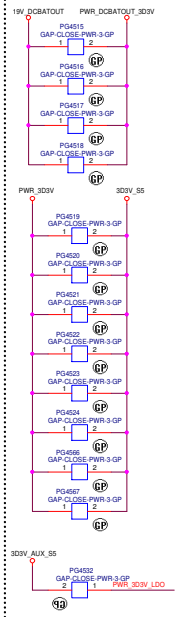
SY8288C For 5V



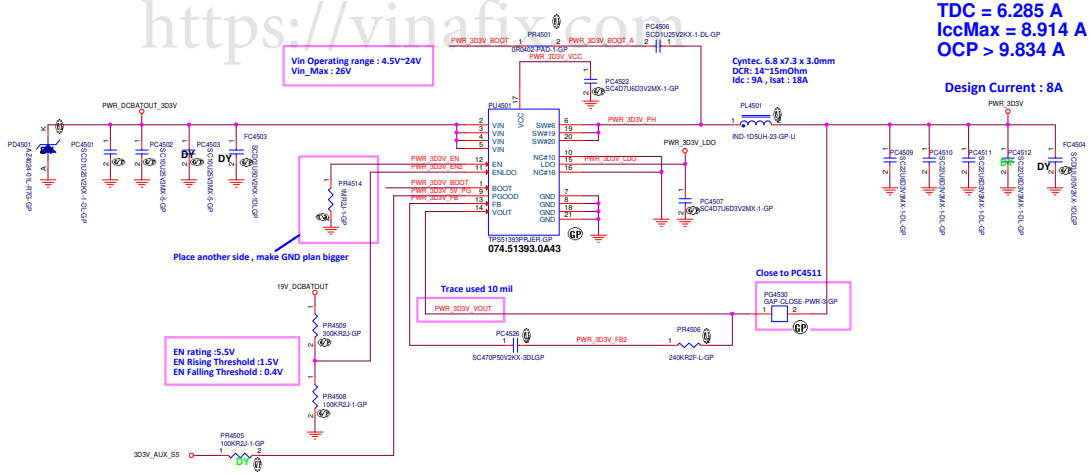
SSID = PWR.Plane.Regulator_3D3V

OFFPAGE-Signal

OFFPAGE-GAP



TPS51393 For 3D3V



<Core Design>

DELL Wistron Corporation
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Title: POWER (SY8288_5V/TPS51393_3D3V)

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 19, 2010 | Sheet 45 of 100

Tigerlake IMVP9 Power - H-line 45W 4 phase

OFFPAGE

6 SVID_DATA_CPU — SVID_DATA_CPU
6 SVID_CLK_CPU — SVID_CLK_CPU
6 SVID_ALERT#_CPU — SVID_ALERT#_CPU
17,44 PCH_PWROK
40,44 PWR_VCORE_VR_EN
PH on CPU side — 6,20,24,44,72 PROCHOT#_CPU — PROCHOT#_CPU
VCCCORE_SENSE — 7,46 VCCCORE_SENSE — VCCCORE_SENSE
VSSCORE_SENSE — 7,46 VSSCORE_SENSE — VSSCORE_SENSE
44 CHGR_PSYS_IMVP — CHGR_PSYS_IMVP
EE side Link
SVID Pull High V
1D05V_VCCST — PG4601 GAP-CLOSE-PWR-3-GP — +PWR_VCORE_VCCST

PROCHOT#_CPU — PR4631 0R2J-2-GP — PWR_VCORE_VR_HOT#
CHGR_PSYS_IMVP — PR4654 0R2J-2-GP — PWR_VCORE_PSYS

H81 45 Baseline
ICCMAX=86A
TDC=68A
LOADLINE=1.5m OHM

H81 45W Performance
ICCMAX=110A
TDC=87A
LOADLINE=1.5m OHM

PWR_DCBATOUT_VCCCORE — Need to Check Net name

PUT CLOSE TO PWM — PC4621 SCU1UH0V2KX-1DLGP

5x5 40PIN QFN

PU4601 NCP81307MNTXG

39	EN	PWR_VCORE_EN_A	
38	VR_RDY	PWR_VCORE_VR_RDY_A	
4	DIFFOUT	PWR_VCORE_DIFFOUT	
6	COMP	PWR_VCORE_COMP	PR4605 49D9R2F-GP; PC4605 SC470P50V2KX-3DLGP; PC4604 SC47P50V2JN-5DLGP; PR4606 1KR2F-3-GP 1V_CPU_CORE; PR4635 453KR2F-GP; PC4619 SC2200P50V2KX-2DLGP
5	FB	PWR_VCORE_FB	PR4604 100R2F-L1-GP-U
1	VSP	PWR_VCORE_VSP	7,46 VCCCORE_SENSE; PR4607 0R2F-1-GP; PC4601 SC1K50V2KX-2DLGP
2	VSN	PWR_VCORE_VSN	7,46 VSSCORE_SENSE; PR4633 2K2F-3-GP; PC4615 SC2200P50V2KX-2DLGP; PR4605 100R2F-L1-GP-U
3	IOUT	PWR_VCORE_IOUT	PR4623 28K7R2F-GP; PC4610 SC470P50V2KX-3DLGP
33	ROSC	PWR_VCORE_ROSC	
40	PSYS	PWR_VCORE_PSYS	PR4642 20KR2F-L-GP
37	VR_HOT#	PWR_VCORE_VR_HOT#	
23	TSENSE	PWR_VCORE_TSENSE	PR4625 1K91R2F-1-GP; PR4624 4K02R2F-GP; PC4611 SCD1U16V2KX-3DLGP; PR4652 NTC-100K-12-GP-U PUT COLSE TO VCORE MOSFET HOT SPOT
10	CSREF	PWR_VCORE_CSREF	PC4620 SCD01U25V2KX-3DLGP
41	THMB	GND	BOTTOM PAD CONNECT TO GND Through 5 VIAs

34	SDIO	PWR_VCORE_SDIO	PR4611 0R2J-2-GP; SVID_DATA_CPU
36	SCLK	PWR_VCORE_SCLK	PR4612 0R2J-2-GP; SVID_CLK_CPU
35	ALERT#	PWR_VCORE_ALERT#	PR4608 0R2J-2-GP; SVID_ALERT#_CPU
24	DRON	PWR_VCORE_DRON	PWR_VCORE_DRON 47
25	PWM1/ICCMAX	PWR_VCORE_PWM1	PWR_VCORE_PWM1 47
22	CSN1	PWR_VCORE_CSN1	PWR_VCORE_CSN1 47
21	CSP1	PWR_VCORE_CSP1_A	PR4603 1 100KR2F-L1-GP; PWR_VCORE_CSP1 47; PC4613 1 SCD1U25V2KX-1-DL-GP; PWR_VCORE_CSP1 1 2K05R2F-GP
26	PWM2/ADD/VBOOT/SR	PWR_VCORE_PWM2	PWR_VCORE_PWM2 47
20	CSN2	PWR_VCORE_CSN2_A	PWR_VCORE_CSN2 47
19	CSP2	PWR_VCORE_CSP2_A	PR4610 1 100KR2F-L1-GP; PWR_VCORE_CSP2 47; PC4612 1 SCD1U25V2KX-1-DL-GP; PWR_VCORE_CSP2 1 2K05R2F-GP
27	PWM3	PWR_VCORE_PWM3	PWR_VCORE_PWM3 47
18	CSN3	PWR_VCORE_CSN3_A	PWR_VCORE_CSN3 47
17	CSP3	PWR_VCORE_CSP3_A	PR4601 1 100KR2F-L1-GP; PWR_VCORE_CSP3 47; PC4603 1 SCD1U25V2KX-1-DL-GP; PWR_VCORE_CSP3 1 3K05R2F-GP
28	PWM4	PWR_VCORE_PWM4	PWR_VCORE_PWM4 47
16	CSN4	PWR_VCORE_CSN4	PWR_VCORE_CSN4 47
15	CSP4	PWR_VCORE_CSP4_A	PR4638 1 100KR2F-L1-GP; PWR_VCORE_CSP4 47; PC4616 1 SCD1U25V2KX-1-DL-GP; PWR_VCORE_CSP4 1 2K05R2F-GP
29	NC#29		
14	NC#14		
13	NC#13		
30	NC#30		
12	NC#12		
11	NC#11	PWR_VCORE_CSP6	5V_S5 PR4650 2KR2F-3-GP
9	CSSUM	PWR_VCORE_CSSUM	PR4617 75KR2F-GP; PR4618 165KR2F-GP
8	CSCOMP	PWR_VCORE_CSCOMP	PWR_VCORE_CSCOMP_A; PC4608 SC820P50V2KX-1-DL-GP
7	ILIM	PWR_VCORE_ILIM	PR4619 21K5R2F-GP; PR4653 NTC-100K-12-GP-U; PC4609 SC330P50V2KX-3-DL-GP

PR4616 1 — 162KR3F-GP — PWR_VCORE_CSP1
PR4629 1 — 162KR3F-GP — PWR_VCORE_CSP2
PR4630 1 — 162KR3F-GP — PWR_VCORE_CSP3
PR4637 1 — 162KR3F-GP — PWR_VCORE_CSP4

PR4638 1 — 10R2F-L-GP — PWR_VCORE_CSN1
PR4620 1 — 10R2F-L-GP — PWR_VCORE_CSN2
PR4621 1 — 10R2F-L-GP — PWR_VCORE_CSN3
PR4622 1 — 10R2F-L-GP — PWR_VCORE_CSN4

PR4615 100R2F-L1-GP-U; PR4614 45D3R2F-L-GP; PR4613 75R2F-2-GP

PWR_VCORE_PWM2 — PR4628 26K1R2F-2-GP
ADDRESS=00H
VBOOT=0V
SR=48mV/uS

PWR_VCORE_PWM1 — PR4627 82KR2F-1-GP
VCORE IMAX SET AT 110A(Performance)
VCORE IMAX SET AT 86A(Baseline)

PWR_VCORE_ROSC — PR4626 84K5R2F-GP
ROSC Work F= 600Khz

For 3 Phase
5V_S5 — PR4655 2KR2F-3-GP — PWR_VCORE_CSP4_A

Performance and Baseline co-lay Bom

	Performance	Baseline
PR4627	86.6K(64.86625.6DL)	68.1K(64.68125.6DL)
PR4649	2.05K(64.20515.6DL)	DY
PC4616	0.1uF(78.10421.2FLDL)	DY
PR4619	21.5K(64.21525.6DL)	16.9K(64.16925.6DL)
PR4637	165K(64.16535.55L)	DY
PR4655	DY	2K(64.20015.6DL)

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: POWER (SY8288_5V/TPS51393_3D3V)
Size: Custom | Document Number: Cyborg N5-H | Rev: X00
Date: Friday, November 13, 2020 | Sheet 46 of 106

OFFPAGE

46 PWR_VCORE_DRON — PWR_VCORE_DRON

46 PWR_VCORE_PWM1 — PWR_VCORE_PWM1
46 PWR_VCORE_PWM2 — PWR_VCORE_PWM2
46 PWR_VCORE_PWM3 — PWR_VCORE_PWM3
46 PWR_VCORE_PWM4 — PWR_VCORE_PWM4

46 PWR_VCORE_CSP1 — PWR_VCORE_CSP1
46 PWR_VCORE_CSN1 — PWR_VCORE_CSN1
46 PWR_VCORE_CSP2 — PWR_VCORE_CSP2
46 PWR_VCORE_CSN2 — PWR_VCORE_CSN2
46 PWR_VCORE_CSP3 — PWR_VCORE_CSP3
46 PWR_VCORE_CSN3 — PWR_VCORE_CSN3
46 PWR_VCORE_CSP4 — PWR_VCORE_CSP4
46 PWR_VCORE_CSN4 — PWR_VCORE_CSN4

19V_DCBATOUT — PWR_DCBATOUT_VCCCORE — 19V_DCBATOUT

PWR_DCBATOUT_VCCCORE

PC4767 0.1UF/50V/X7R/0402-1-GP
077.C1071.0071
2nd = 077.C1071.0101
PC4768 220UF/25V/SMD-GP
080.22612.0001

Acoustic

33uF/25V,
ESR=42mohm,
Ripple_Current=3200mA

Phase1

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.

Phase2

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.

Phase3

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.

Phase4

Max Current = 3.50(A)

PWR_DCBATOUT_VCCCORE

MLCCs must be placed symmetrically on Top and Bottom.

This circuit is for Hexa core.
Please refer to the table in next page.

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Title: POWER (SY8288_5V/TPS51393_3D3V)
Size: A3 | Document Number: Cyborg N5-H | Rev: XXX
Date: Friday, November 14, 2008 | Sheet 37 of 46

<Core Design>

Wistron Corporation
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Title
Power (RSVD)

Size	Document Number	Rev
A4	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 48 of 106

<Core Design>

Wistron Corporation
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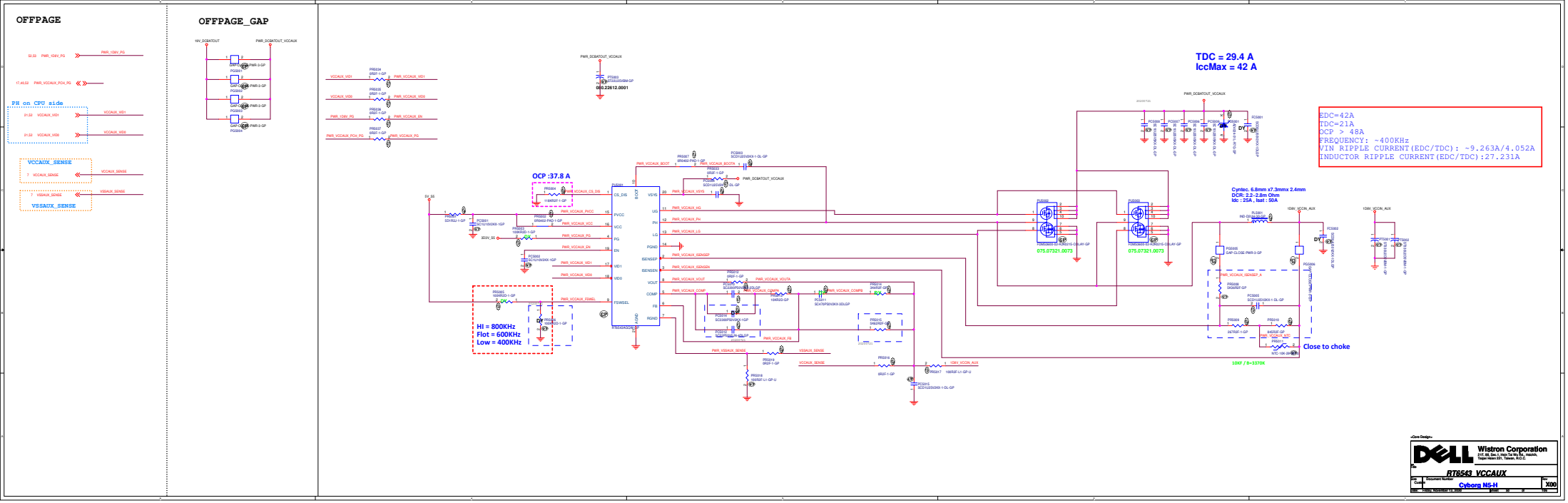
Title

Size	Document Number	Rev
Custom	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 49 of 106



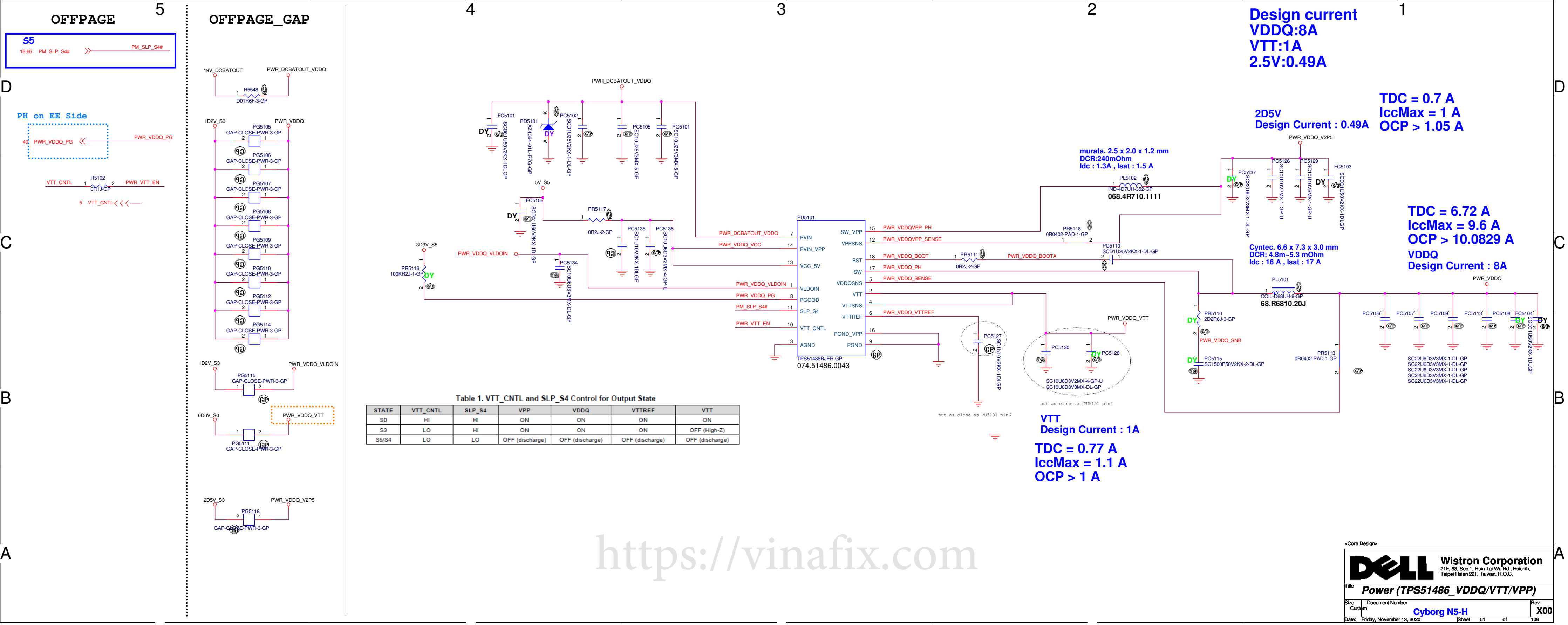


Table 1. VTT_CNTL and SLP_S4 Control for Output State

STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
S5/S4	LO	LO	OFF (discharge)	OFF (discharge)	OFF (discharge)	OFF (discharge)

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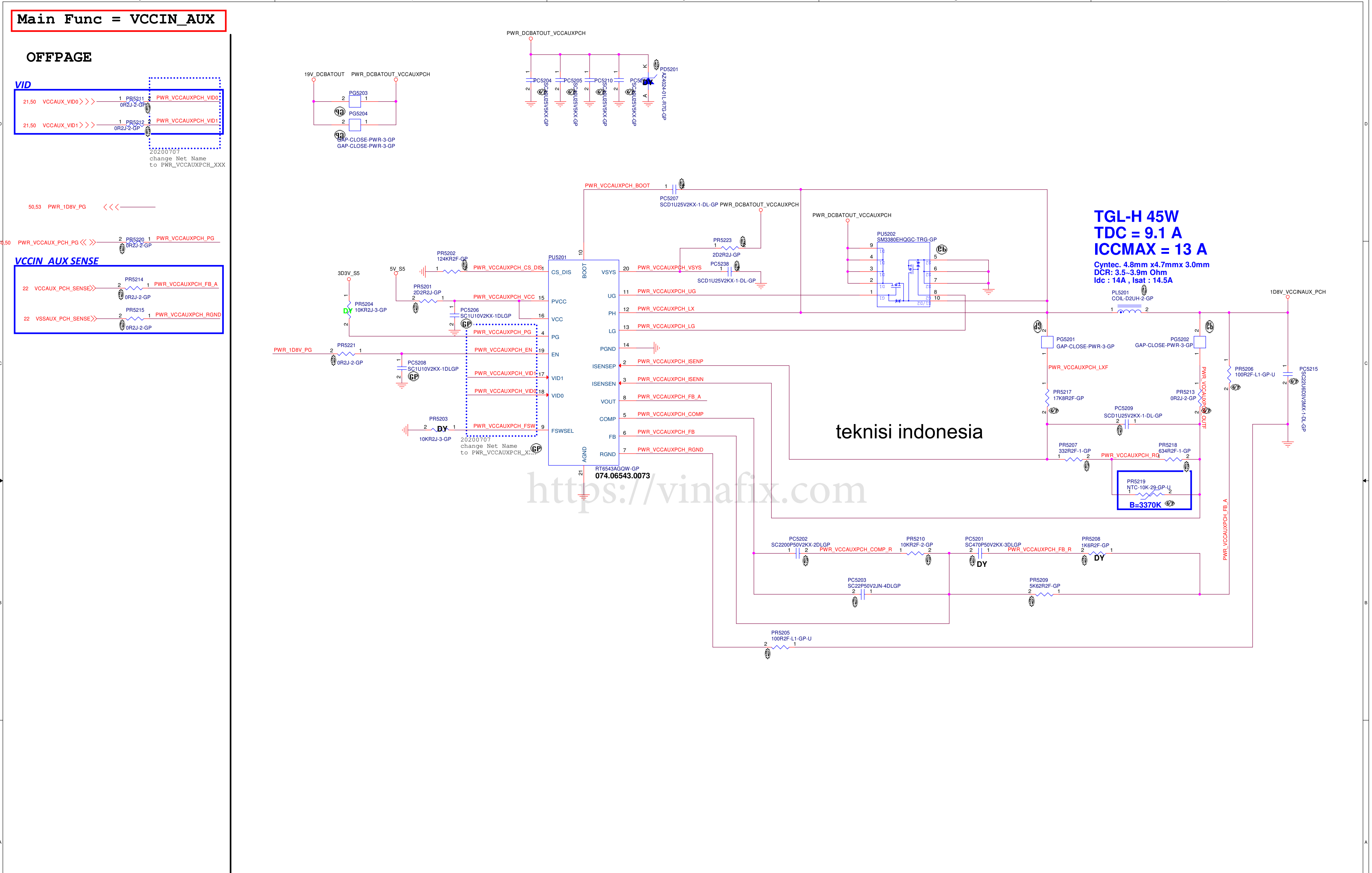
Title: Power (TPS51486_VDDQ/VTT/VPP)

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 51 of 106


Main Func = VCCIN_AUX
OFFPAGE
VID
VCCAUX_VID0
VCCAUX_VID1
PWR_VCCAUXPCH_VID0
PWR_VCCAUXPCH_VID1
20200707 change Net Name to PWR_VCCAUXPCH_XXX
PWR_1D8V_PG
PWR_VCCAUX_PCH_PG
PWR_VCCAUXPCH_PG
VCCIN_AUX SENSE
VCCAUX_PCH_SENSE
VSSAUX_PCH_SENSE
PWR_VCCAUXPCH_FB_A
PWR_VCCAUXPCH_RGND
PWR_DCBATOUT_VCCAUXPCH
19V_DCBATOUT
GAP-CLOSE-PWR-3-GP
PU5201
RT6543AGQW-GP
074.06543.0073
PU5202
SM3380EHQGC-TRG-GP
TGL-H 45W
TDC = 9.1 A
ICCMAX = 13 A
Cyntec. 4.8mm x4.7mmx 3.0mm
DCR: 3.5~3.9m Ohm
Idc : 14A , Isat : 14.5A
PL5201
COIL-D2UH-2-GP
1D8V_VCCINAUX_PCH
B=3370K
teknisi indonesia
https://vinafix.com

Main Func = 1D8V

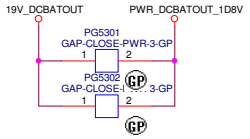
SY8386RHC for 1D8V

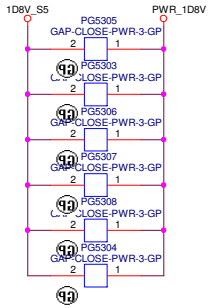
TDC : 4.16 A
IccMax : 5.52 A
OCP > 6 A

IDC:6 A

OFFPAGE

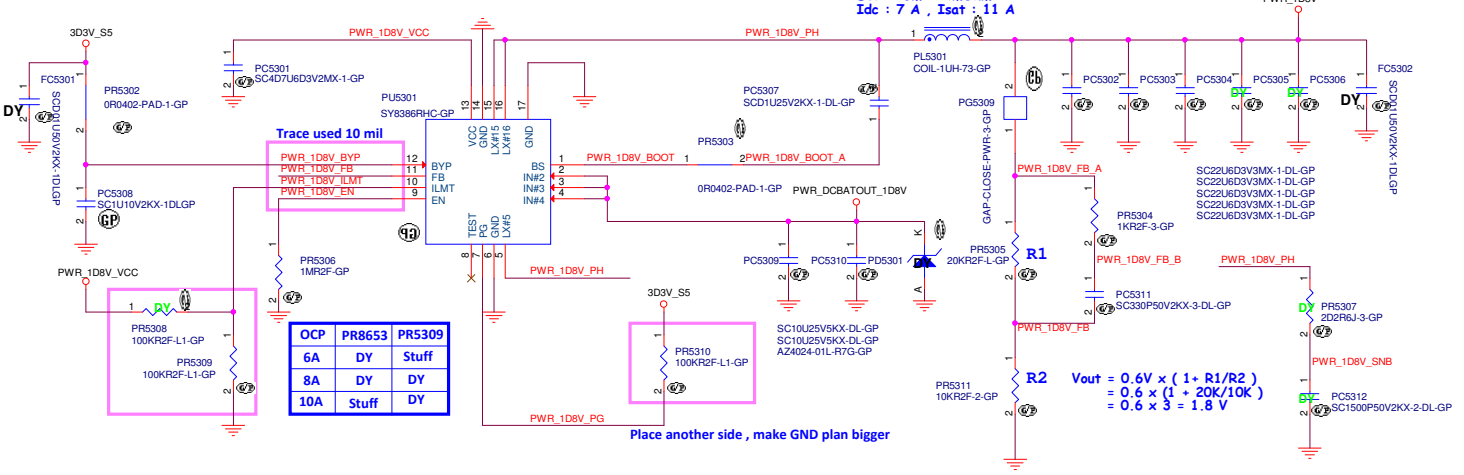
OFFPAGE_GAP





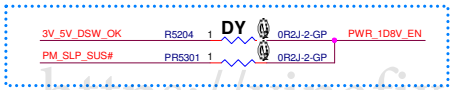
PH on EE Side

Cyntec, 5.2 mm x 4.9mm x 3.0mm
DCR: 13m ~14mOhm
Idc : 7 A , Isat : 11 A



OCP	PR8653	PR5309
6A	DY	Stuff
8A	DY	DY
10A	Stuff	DY

Vout = 0.6V x (1+ R1/R2)
= 0.6 x (1 + 20K/10K)
= 0.6 x 3 = 1.8 V



<Core Design>

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Title: Power (1D8V)
Size: Custom | Document Number: Cyborg N5-H | Rev: X00
Date: Friday, November 13, 2020 | Sheet 53 of 106

no need VNN/V1P05V
Power for Volume design!!

<Core Design>

Wistron Corporation
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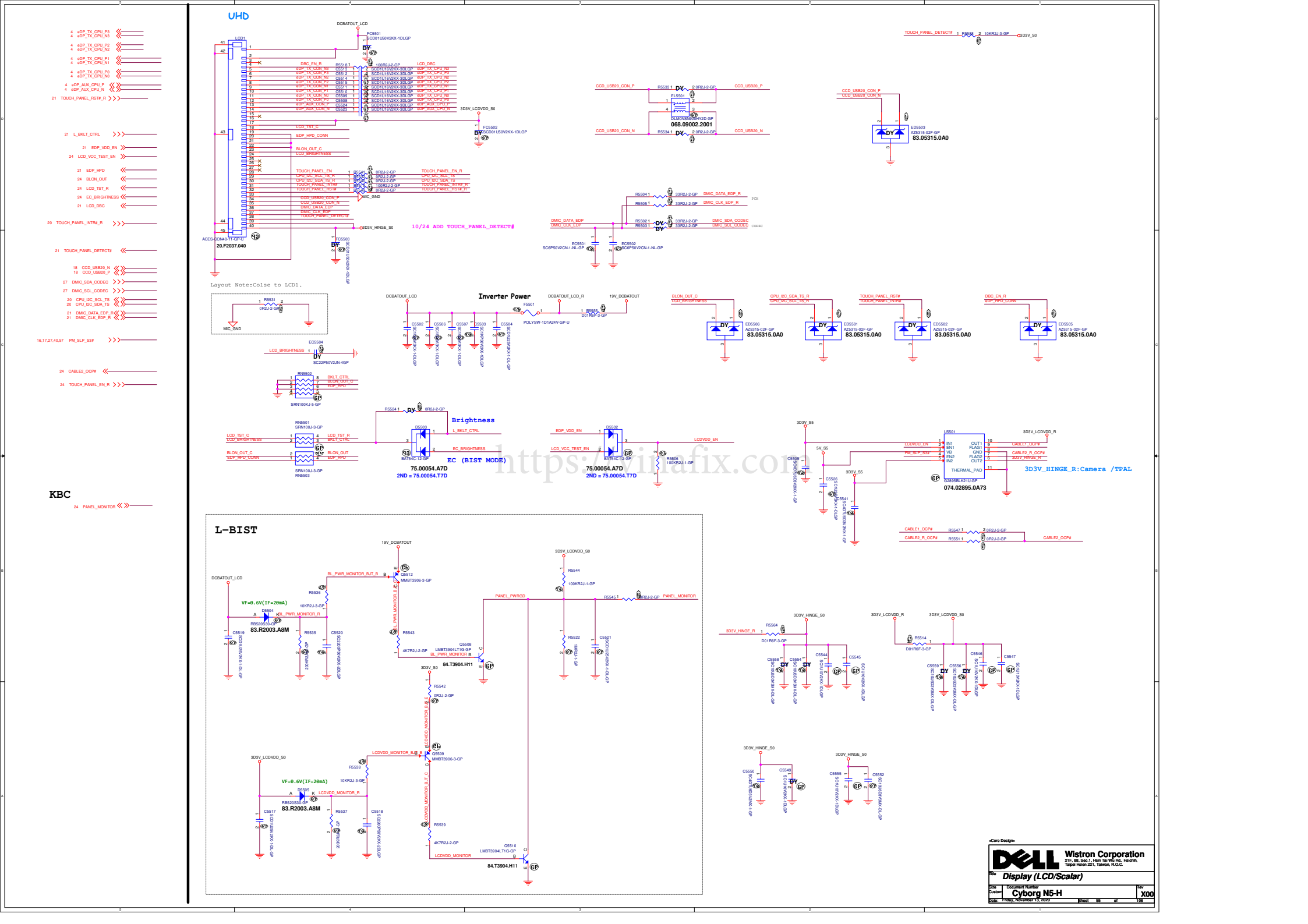
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (VCCIO/VCC_PRIM /BYPSS/ 12V

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 54 of 106



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Display (CRT/IR Camera)

Size	Document Number	Rev
Custom	Cyborg N5-H	X00

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SSID = HDMI

GPU (HDMI2.0)

20,21 HDMI_HPD_GPU
24 HDMI_HPD
16,17,27,40,55 PM_SLP_S3#

(HDMI2.0)

24,65 DAT_TP_SIO_I2C_CLK
24,65 CLK_TP_SIO_I2C_DAT

CPU (HDMI2.0)

4 DP3_DDI_TX_P0
4 DP3_DDI_TX_N0
4 DP3_DDI_TX_P1
4 DP3_DDI_TX_N1
4 DP3_DDI_TX_P2
4 DP3_DDI_TX_N2
4 DP3_DDI_TX_P3
4 DP3_DDI_TX_N3

U5701
PS8409AQFN48GTR2-A2-GP
071.08409.0B03

3D3V_HDMI_VDD
1D2V_HDMI_VDD
1D2V_HDMI_VDDTX
1D2V_HDMI_VDDRX
1D2V_HDMI_VDDA
POWERSWITCH
HDMI_ID
REXT
PS8409A_RST#
PS8409A_PU#
HDMI_CEC
TESTMODEB
CEC_EN
NC#25
GND

HDMI_DDI_TX_CMC_P2
HDMI_DDI_TX_CMC_N2
HDMI_DDI_TX_CMC_P1
HDMI_DDI_TX_CMC_N1
HDMI_DDI_TX_CMC_P0
HDMI_DDI_TX_CMC_N0
HDMI_DDI_TX_CMC_P3
HDMI_DDI_TX_CMC_N3
HDMI_HPD_CON
HDMI_HPD_SRC
HDMI_SCL_CON
HDMI_SDA_CON
CSCL
CSDA
I2C_ADDR
PRE
DCIN_ENB
EQ

DP3_DDI_TX_P2 C5746 SCD1U25V2KX-1-DL-GP HDMI_DDI_TX_ALS_P2
DP3_DDI_TX_N2 C5729 SCD1U25V2KX-1-DL-GP HDMI_DDI_TX_ALS_N2
DP3_DDI_TX_P1 C5754 SCD1U25V2KX-1-DL-GP HDMI_DDI_TX_ALS_P1
DP3_DDI_TX_N1 C5778 SCD1U25V2KX-1-DL-GP HDMI_DDI_TX_ALS_N1
DP3_DDI_TX_P0 C5775 SCD1U25V2KX-1-DL-GP HDMI_DDI_TX_ALS_P0
DP3_DDI_TX_N0 C5777 SCD1U25V2KX-1-DL-GP HDMI_DDI_TX_ALS_N0
DP3_DDI_TX_P3 C5772 SCD1U25V2KX-1-DL-GP HDMI_DDI_TX_ALS_P3
DP3_DDI_TX_N3 C5770 SCD1U25V2KX-1-DL-GP HDMI_DDI_TX_ALS_N3

HDMI_HPD_CON_R R5782 1 0R2J-2-GP HDMI_HPD_GPU
R5781 2KR2J-2-GP
R5780 2KR2J-2-GP

HDMI_DDI_TX_CMC_P2 R5765 0R2J-2-GP HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CMC_N2 R5766 0R2J-2-GP HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_CMC_P1 R5767 0R2J-2-GP HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CMC_N1 R5768 0R2J-2-GP HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CMC_P0 R5769 0R2J-2-GP HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CMC_N0 R5770 0R2J-2-GP HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CMC_P3 R5771 0R2J-2-GP HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CMC_N3 R5772 0R2J-2-GP HDMI_DDI_TX_CON_N3
C5747 SC470P50V2BN-2-GP

EL5701 FILTER-4P-264-2-GP 068.24900.2021
EL5702 FILTER-4P-264-2-GP 068.24900.2021
EL5703 FILTER-4P-264-2-GP 068.24900.2021
EL5704 FILTER-4P-264-2-GP 068.24900.2021

ED5701 AZ1043-04F-R7G-GP 075.01043.0073
ED5702 AZ1043-04F-R7G-GP 075.01043.0073
ED5703 AZ1043-04F-R7G-GP 075.01043.0073

HDMI_DDI_TX_CON_N1 HDMI_DDI_TX_CON_N1
HDMI_DDI_TX_CON_P1 HDMI_DDI_TX_CON_P1
HDMI_DDI_TX_CON_N2 HDMI_DDI_TX_CON_N2
HDMI_DDI_TX_CON_P2 HDMI_DDI_TX_CON_P2
HDMI_DDI_TX_CON_P0 HDMI_DDI_TX_CON_P0
HDMI_DDI_TX_CON_N0 HDMI_DDI_TX_CON_N0
HDMI_DDI_TX_CON_P3 HDMI_DDI_TX_CON_P3
HDMI_DDI_TX_CON_N3 HDMI_DDI_TX_CON_N3
HDMI_SCL_CON HDMI_SCL_CON
HDMI_SDA_CON HDMI_SDA_CON
HDMI_HPD_CON_R HDMI_HPD_CON_R

teknisi indonesia

5V_S0
D5701 BAW56-9-GP-U 75.00056.07D
HDMI_SDA_R
HDMI_SCL_R
R5755 2KR2J-2-GP
R5751 2KR2J-2-GP

Vgs_th max=1.1V
21 CPU_DP3_CTRL_DATA R5781 0R2J-2-GP HDMI_SDA_GPU_R
21 CPU_DP3_CTRL_CLK R5780 0R2J-2-GP HDMI_SCL_GPU_R
U5702 PJT138KA-GP 075.00138.0A7C
3V3_S0
3D3V_S0
HDMI_SDA_CON
HDMI_SCL_CON

5V_S0 F5701 POLYSW-1D1A6V-9-GP-U 69.48001.08
2nd = 69.50011.081
5V_HDMI_S0
HDMI1 HDMI CONN
+5V_POWER
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
RESERVED#14
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
GND
SKT-HDMI23-261-GP-U 022.10025.0841
R5764 100KR2J-1-GP

3D3V_S0 3D3V_HDMI_VDD
L5701 0R3J-0-U-GP
C5759 C5779 C5750 SCD1U25V2KX-1DLGP SCD1U25V2KX-1-DL-GP

for digital logic
1D2V_HDMI 1D2V_HDMI_VDD
L5702 0R3J-0-U-GP
C5763 C5755 C5756 C5757 C5758 SCD1U25V2KX-1-DL-GP SCD1U50V2KX-1DLGP

for DP receiver
1D2V_HDMI 1D2V_HDMI_VDDRX
VDDRX12 power rail is extremely senstive. Control the power ripple to be < 30mV
L5704 0R3J-0-U-GP
C5766 C5767 C5768 C5769 C2427U6D3V2KX-1-GP SCD1U25V2KX-1-DL-GP SCD1U25V2KX-3DLGP

for HDMI transmitter
1D2V_HDMI 1D2V_HDMI_VDDTX
L5706 0R3J-0-U-GP
C5773 C5774 C5776 SCD1U25V2KX-1-DL-GP SCD1U50V2KX-1DLGP

for analog
1D2V_HDMI 1D2V_HDMI_VDDA
L5703 0R3J-0-U-GP
C5760 C5761 C5762 SCD1U25V2KX-1-DL-GP SCD1U25V2KX-3DLGP

3D3V_HDMI_VDD
R5744 10KR2J-3-GP PS8409A_PD#
R5737 10KR2J-3-GP PS8409A_RST#
C5725 SC1U10V2KX-1DLGP

R5738 4K7R2J-2-GP CSDA
R5739 4K7R2J-2-GP CSCL
R5740 4K7R2J-2-GP I2C_ADDR
R5746 4K7R2J-2-GP HDMI_ID
R5741 4K7R2J-2-GP PRE
R5742 4K7R2J-2-GP DCIN_ENB

U5703 2N7002KDW-1-GP 75.27002.F7C
CSCL DAT_TP_SIO_I2C_CLK
CSDA CLK_TP_SIO_I2C_DAT

R5747 100KR2F-L1-GP HPD_Q
U5705 2N7002KDW-1-GP 75.27002.F7C
R5748 100KR2F-L1-GP HDMI_HPD
HDMI_HPD_CON_R
07/31 HDMI HPD Add Level Shift
Connect to EC Follow SP13

APL5934 for HDMI 1D2V
5V_S5
1D2V_HDMI_VIN
U5704 APL5934KAI-TRG-GP-U 074.05934.003D
VCNTL POK EN VIN#9 VIN#5 VOUT#4 VOUT#3 FB GND
G5701 GAP-CLOSE-PWR-3-GP
3D3V_S5
1D2V_HDMI_FB
1D2V_HDMI_EN_R
PM_SLP_S3# R5775 0R2J-2-GP
R5773 9K1R2F-2-GP
R5774 10KR2F-2-GP
C5745 SC68P50V2JN-1DLGP
C5765 SC1U6D3V3MX-DL-GP
C5794 SC1U6D3V3MX-DL-GP
C5743 SC1U10V2KX-1DLGP
C5744 C5742 SC1U10V2KX-1-DL-GP
Design Current = 550mA
Vout=0.8V*(R1+R2)/R2
20180409 Follow RO13

3D3V_HDMI_VDD
R5745 4K7R2J-2-GP
R5743 4K7R2J-2-GP
EQ

R5734 should be place close to REXT pin
REXT_R R5704 0R2J-2-GP REXT
R5724 4K99R2F-L-GP

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: Display (HDMI Conn/Retimer)
Size: A2
Document Number: Cyborg N5-H
Rev: X00
Date: Friday, November 13, 2020
Sheet 57 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display (DP Conn/Redriver / DVI)***

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 58 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Display (Backlight PWR)***

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 59 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (HDD/ODD)*

Size	Document Number	Rev
A4	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 60 of 106

Main Func = WLAN

17 WLAN_PCIE_RX_N
17 WLAN_PCIE_RX_P
17 WLAN_PCIE_TX_N
17 WLAN_PCIE_TX_P
19 WLAN_CLK_CPU_P
19 WLAN_CLK_CPU_N
20 WLAN_CLKREQ_CPU_N

18 BT_USB20_N
18 BT_USB20_P

20,26,63,71,79,91 PLT_RST_N

19 CNV_WR_DN1
19 CNV_WR_DP1
19 CNV_WR_DN0
19 CNV_WR_DP0
19 CNV_WR_CLKN
19 CNV_WR_CLKP
19 CNV_WT_DN1
19 CNV_WT_DP1
19 CNV_WT_DN0
19 CNV_WT_DP0
19 CNV_WT_CLKN
19 CNV_WT_CLKP
21 CNV_BRI_RSP
21 CNV_RGI_DT_CON
21 CNV_BRI_DT_CON
21 CNV_RGI_RSP
20 CNV_RF_RESET#

20 CLKREQ_CNV#

21 WLAN_WIGIG60GHZ_DIS#
20 BT_RADIO_DIS#

16,24 SUS_CLK

20 CNV_DET#

21 PCIE_WAKE_N

ARD:WLAN_WAKE>>BOM:Use R6106

3D3V_S5 — R6107 0R5J-5-GP — 3D3V_WLAN

C6101 SCD1U16V2KX-3DLGP
C6103 SCD1U16V2KX-3DLGP
C6104 SC221E6D3V3MX-1DL-GP

R6111 2 0R2J-2-GP
BT_USB20_P — EL6101 DY DLM0NSN900HY2D-GP — BT_USB20_P_CON
BT_USB20_N — BT_USB20_N_CON
068.09002.2001
R6113 2 0R2J-2-GP

3D3V_WLAN
R6109 10KR2J-3-GP
WLAN_WIGIG60GHZ_DIS# R6134 0R2J-2-GP WLAN_WIGIG60GHZ_DIS#_R

3D3V_WLAN
R6133 DY 0R2J-2-GP
R6110 10KR2J-3-GP
BT_RADIO_DIS# RB520S30-GP D6102 BT_RADIO_DIS#_R

83.R2003.A8M
2ND = 083.52030.008F

1090mA

WLAN1 SKT-NGFF75P-164-GP
062.10003.0B11

NP1		NP2	
	1		
GND	3	3_3VAUX	2
USB_D+	5	3_3VAUX	4
USB_D-	7	LED#1	6
GND	9	PCM_CLK	8
SDIO_CLK	11	PCM_SYNC	10
SDIO_CMD	13	PCM_IN	12
SDIO_DAT0	15	PCM_OUT	14
SDIO_DAT1	17	LED#2	16
SDIO_DAT2	19	GND	18
SDIO_DAT3	21	UART_WAKE	20
SDIO_WAKE	23	UART_RX	22
SDIO_RESET			
	33	UART_TX	32
GND	35	UART_RTS	34
PETP0	37	UART_CTS	36
PETN0	39	CLINK_RESET	38
GND	41	CLINK_DATA	40
PERP0	43	CLINK_CLK	42
PERN0	45	COEX3	44
GND	47	COEX2	46
REFCLKP0	49	COEX1	48
REFCLKN0	51	SUSCLK_32KHZ	50
GND	53	PERST0#	52
CLKREQ0#	55	RESERVED#54/W_DISABLE#2	54
PEWAKE0#	57	W_DISABLE#1	56
GND	59	NFC_I2C_SM_DATA	58
RESERVED#59/2ND_LANE_PETP1	61	NFC_I2C_SM_CLK	60
RESERVED#61/2ND_LANE_PETN1	63	NFC_I2C_IRQ/MGPIO5	62
GND	65	GPIO0_NFC_RESET#/MGPIO7	64
RESERVED#65/2ND_LANE_PERP1	67	RESERVED#66	66
RESERVED#67/2ND_LANE_PERN1	69	RESERVED#68	68
GND	71	RESERVED#70	70
RESERVED#71	73	3_3VAUX	72
RESERVED#73	75	3_3VAUX	74
GND	77		76

NGFF_KEY_E_75P

BT_USB20_P_CON
BT_USB20_N_CON

CNV_WR_DN1 R6114 0R2J-2-GP CNV_WR_DN1_R
CNV_WR_DP1 R6115 0R2J-2-GP CNV_WR_DP1_R
CNV_WR_DN0 R6116 0R2J-2-GP CNV_WR_DN0_R
CNV_WR_DP0 R6118 0R2J-2-GP CNV_WR_DP0_R
CNV_WR_CLKN R6119 0R2J-2-GP CNV_WR_CLKN_R
CNV_WR_CLKP R6120 0R2J-2-GP CNV_WR_CLKP_R

WLAN_PCIE_TX_P C6115 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_P_C
WLAN_PCIE_TX_N C6102 SCD1U16V2KX-3DLGP WLAN_PCIE_TX_N_C

WLAN_PCIE_RX_P
WLAN_PCIE_RX_N
WLAN_CLK_CPU_P
WLAN_CLK_CPU_N
WLAN_CLKREQ_CPU_N
PCIE_WAKE_N

CNV_WT_DN1 R6121 0R2J-2-GP CNV_WT_DN1_R
CNV_WT_DP1 R6122 0R2J-2-GP CNV_WT_DP1_R
CNV_WT_DN0 R6123 0R2J-2-GP CNV_WT_DN0_R
CNV_WT_DP0 R6124 0R2J-2-GP CNV_WT_DP0_R
CNV_WT_CLKN R6125 0R2J-2-GP CNV_WT_CLKN_R
CNV_WT_CLKP R6126 0R2J-2-GP CNV_WT_CLKP_R

3D3V_WLAN
FC6101 DY SCD01U50V2KX-1DLGP
R6132 DY 0R2J-2-GP CNV_DET#
CNV_RF_RESET#
CLKREQ_CNV#
CNV_BRI_RSP_R R6127 49D9R2F-GP CNV_BRI_RSP
CNV_RGI_DT_CON
CNV_RGI_RSP_R R6112 49D9R2F-GP CNV_RGI_RSP
CNV_BRI_DT_CON
SUS_CLK_WLAN R6135 33R2J-2-GP SUS_CLK
WLAN_RST# R6131 0R2J-2-GP PLT_RST_N
BT_RADIO_DIS#_R
WLAN_WIGIG60GHZ_DIS#_R
PULSAR_38P4M_REFCLK 1 TP6101
3D3V_WLAN

2017.10.16
Andy share CNV_DET connect to CNV_RST PIN .
Need to confirm Hi det/low det to ph/pl

3D3V_WLAN
PCIE_WAKE_N R6117 10KR2F-GP DY
CNV_RF_RESET# R6101 75KR2F-GP DY
CLKREQ_CNV# R6102 75KR2F-GP DY

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (WLAN M.2)
Size: Custom
Document Number: Cyborg N5-H
Rev: X00
Date: Friday, November 13, 2020
Sheet 61 of 105

SSID = Wireless

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *INT IO (RSVD) WWAN*

Size	Document Number	Rev
A	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 62 of 106

Mini Card Connector (NGFF m-SATA)

SSID = m-SATA

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

SSD M.2 CONN_2nd

SSD1

SKT-NGFF75P-224-GP

062.10003.0F31

NGFF_KEY_M 75P

SSD M.2 CONN_Main

SSD2

SKT-NGFF75P-224-GP

062.10003.0F31

NGFF_KEY_M 75P

Current Sense R

11/10 Add

U6301 TC7SZ08FU-LJ-CY-GP 073.7SZ08.000G

AFTP6307 AFTE14P-1-GP

AFTP6304 AFTE14P-1-GP

AFTP6306 AFTE14P-1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

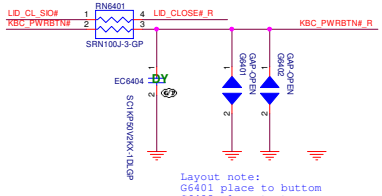
Title: INT IO (SSD M.2/ eMMC)

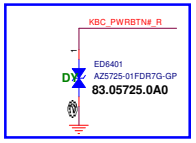
Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 63 of 106

Main Func = Power BTN

close to IOBD1



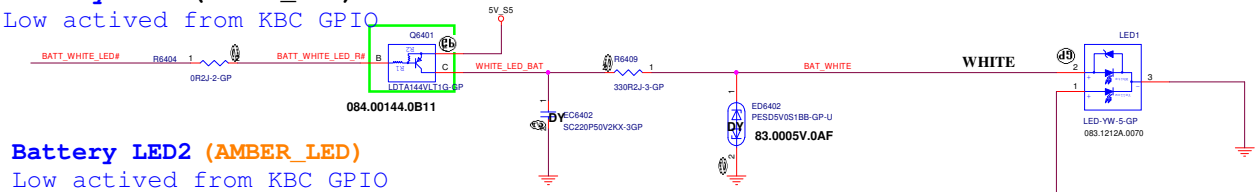


0614 Layout HT

24,66 LID_CL_SIO#
24,64 KBC_PWRBTN#
66 KBC_PWRBTN#_R
66,67 LID_CLOSE#_R

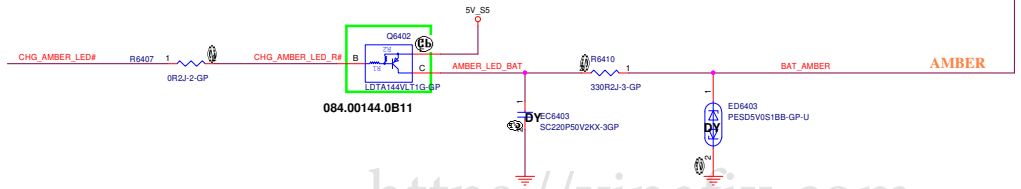
Battery LED1 (WHITE_LED)

Low actived from KBC GPIO



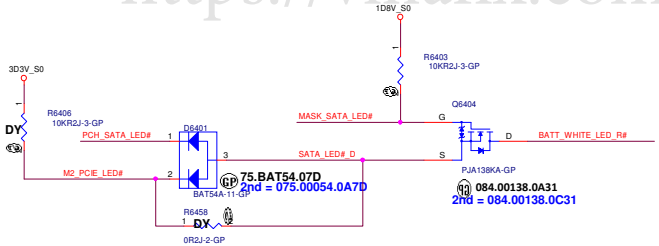
Battery LED2 (AMBER_LED)

Low actived from KBC GPIO



24 BATT_WHITE_LED#
21 PCH_SATA_LED#
24 MASK_SATA_LED#
63 M2_PCIE_LED#

SATA LED

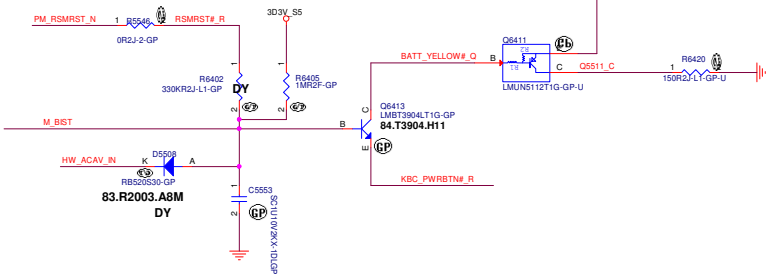


17 PM_RSMRST_N
24,44 HW_ACAV_IN
24,64 KBC_PWRBTN#

KBC

24 M_BIST
24 CHG_AMBER_LED#

M-BIST for G10 (Proposed schematic) follow bandon



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED / Button / Power Button

Size: A2 | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 64 of 106

Main Func = Keyboard

KB Backlight Power Consumption: 285mA max.

5V_S0 → F6502 POLYSW-1D1A6V-9-GP-U → +5V_KB_BL

69.48001.081
2nd = 69.50011.081

C6501 SCD1U25V2KX-1-DL-GP

X01 20161228 change

+5V_KB_BL
KB_LED_DET_C
KB_BL_CTRL#
KBBL1 ACES-CON4-90-GP-U
020.K0298.0004

Change ESD 2KV

24 KB_LED_PWM → R6509 100KR2J-1-GP → Q6501 PJA138KA-GP (G, D, S) → KB_BL_CTRL#

084.00138.0A31
2nd = 084.00138.0C31

21 KB_BL_DET → R6507 51KR2J-1-GP → KB_LED_DET_C
R6508 100KR2J-1-GP
C6504 SCD1U16V2KX-3GP

+5V_KB_BL → AFTP6529 AFTE14P-1-GP
KB_BL_CTRL# → AFTP6530 AFTE14P-1-GP

X02 0414

24 CAP_LED#_R → R6512 2KR2J-2-GP → CAP_LED_R#

Q6505 LDTA144VLT1G-GP
5V_S5
CAP_LED_Q → R6513 1KR2J-1-GP → CAP_LED

EC6507 SCD1U16V2KX-4-GP

short pad change 0 ohm

084.00144.0B11

CAP LED Control
LOW actived from KBC GPIO

24 KSI[0..7] → KSI0 … KSI7

24 KSO00 … KSO16

20 KB_DET# → AFTE14P-1-GP AFTP6542 … AFTP6566

KB1 PTWO-CON30-18-GP
020.K0210.0030

Main Func = TPAD

24 PTP_DIS#

TP_VDD
3D3V_S5_PCH
R6514 1 0R3J-0-U-GP
ARD:TP_WAKE>>BOM:Use R6514

R6557 10KR2J-3-GP
PTP_DIS# → D6501 RB520S30-GP → PTP_CON_DIS#

83.R2003.A8M
2ND = 083.52030.008F

RN6503 SRN2K2J-1-GP

TPAD1 PTWO-CON8-16-GP
020.K0255.0008

Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

EC I2C
I2C

24,57 DAT_TP_SIO_I2C_CLK
24,57 CLK_TP_SIO_I2C_DAT
20,66 CPU_I2C_SCL_P1
20,66 CPU_I2C_SDA_P1

0R2J-2-GP
R6515 CPU_I2C_SCL_TP
R6516 CPU_I2C_SDA_TP
R6505 CPU_I2C_SCL_TP
R6506 CPU_I2C_SDA_TP

C6505 SCD1U25V2KX-1-DL-GP
C4347 SC1KP50V2KX-1DLGP
C4348 SC1KP50V2KX-1DLGP
EC6501 SC33P50V2JN-3GP

21,24 TOUCHPAD_INTR#
PTP_CON_DIS#
AFTE14P-1-GP AFTP6540

Placement: Close to TPAD1

Change pindefine DVT1 0210 1330

Need to check if it is Active High or Active Low
and check if there is PH on TPAD side.

X02 0415

TP_VDD
R6511 10KR2J-3-GP
TOUCHPAD_INTR#

TP_VDD → AFTP6531
CPU_I2C_SCL_TP → AFTP6534
CPU_I2C_SDA_TP → AFTP6535
TOUCHPAD_INTR# → AFTP6536
PTP_DIS# → AFTP6537

<Core Design>

Wistron Corporation
21F, 88, Sec 1 Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (KB/TP)
Size: Custom | Document Number: Cyborg N5-H | Rev: X00
Date: Friday, November 13, 2020 | Sheet 65 of 106

USB3.1

18 USB3_USB30_TX_N
18 USB3_USB30_TX_P
18 USB3_USB30_RX_N
18 USB3_USB30_RX_P

18 USB3_USB20_P
18 USB3_USB20_N

USB Power

20200206 SLG5_USB_PWR_EN#
21 USB_OC1_N

FP

24 FPR_SCAN#
64 KBC_PWRBTN#_R
18 FP1_USB20_N
18 FP1_USB20_P

16,51 PM_SLP_S4#

21 SD_READ_MODE#

18 CARD1_USB20_N
18 CARD1_USB20_P

20,65 CPU_I2C_SCL_P1
20,65 CPU_I2C_SDA_P1

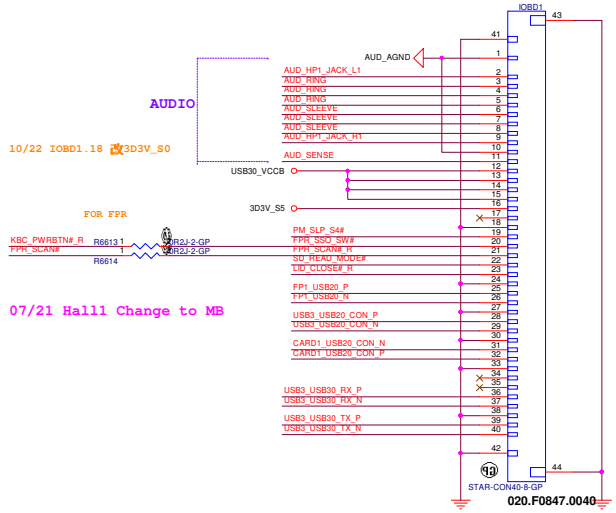
44 BT_PWR_IN-
44 BT_PWR_IN+

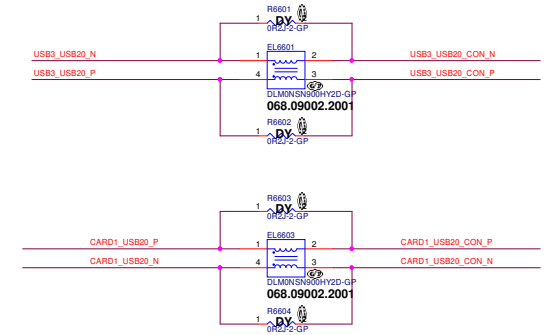
AUDIO

27 AUD_SENSE
29 AUD_HP1_JACK_L1
29 AUD_HP1_JACK_R1
27,29 AUD_RING
27,29 AUD_SLEEVE

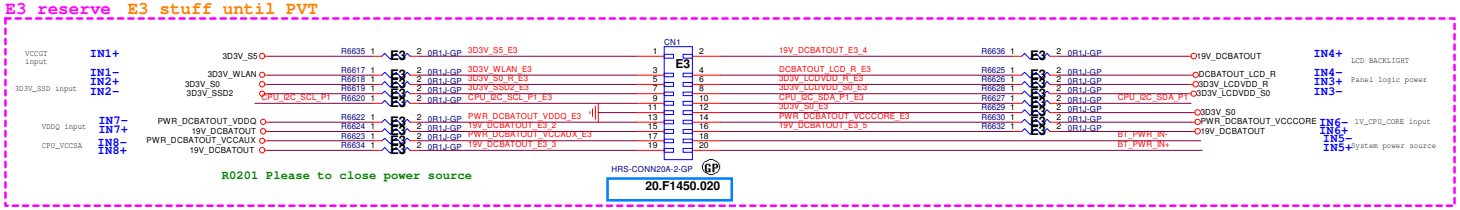
LID

24 LID_POWER_ON#
24,64 LID_CL_SIO#
67 LID_CL_NB#
64,67 LID_CLOSE#_R

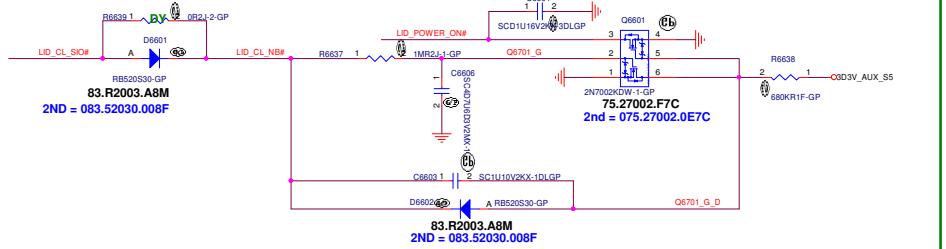


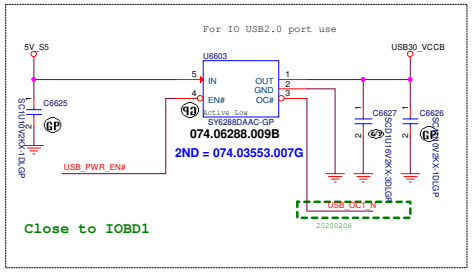


E3 reserve E3 stuff until PVT



LID sensor





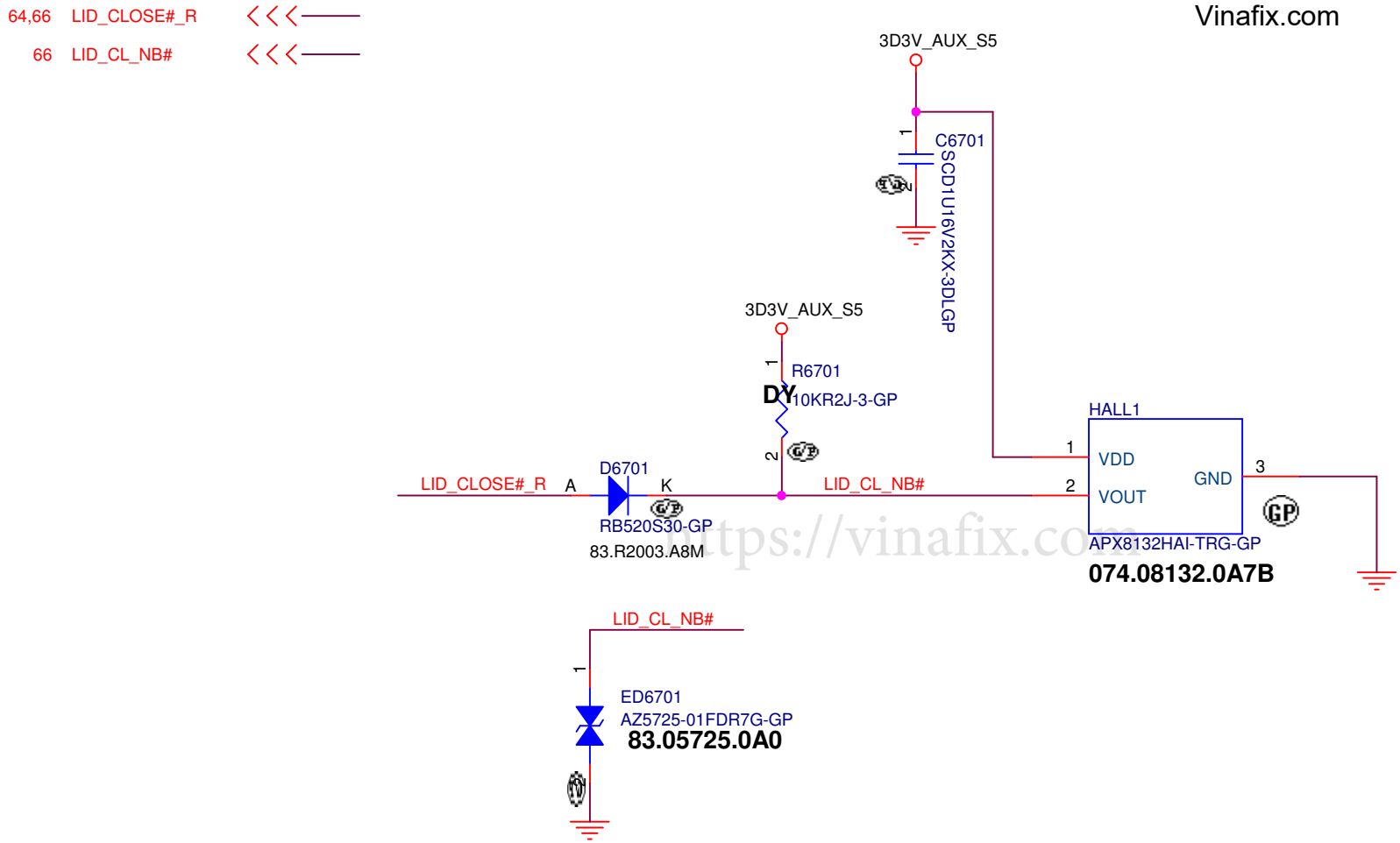
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Conn (USB/AUDIO/CR..etc)

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 66 of 106



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Sensor (Hall-Sensor)***

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 67 of 106

Main Func = Debug

20 ESPI_CPU_IO0_DBG
20 ESPI_CPU_IO1_DBG
20 ESPI_CPU_IO2_DBG
20 ESPI_CPU_IO3_DBG
20 ESPI_CPU_CLK_DBG
20,24 ESPI_CPU_CS_N
20,24 ESPI_CPU_RST_N

20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD

20200206

20200206

ESPI_CPU_CLK_DBG
ESPI_CPU_RST_N
ESPI_CPU_CS_N
ESPI_CPU_IO3_DBG
ESPI_CPU_IO2_DBG
ESPI_CPU_IO1_DBG
ESPI_CPU_IO0_DBG

Debug Connector

DBG1
15
1
2
3
4
5
6
7
8
9
10
11
12
13
14
16
zz.F0765.01401
DEBUG
GP
ACES-CON14-5-GP

20.F0765.014

X01 20161223 change

3D3V_S0

24 HOST_DEBUG_TX
R6801 1 DY 2 0R2J-2-GP HOST_DEBUG_TX_CON

UART_2_CRXD_DTXD
R6803 1 DEBUG 0R2J-2-GP UART_2_CRXD_DTXD_CON

UART_2_CTXD_DRXD
R6802 1 DEBUG 0R2J-2-GP UART_2_CTXD_DRXD_CON

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Debug (LPC debug)

Size: Custom
Document Number: Cyborg N5-H
Rev: X00

Date: Friday, November 13, 2020
Sheet 68 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sensor (RSVD)*

Size	Document Number	Rev
A4	Cyborg N5-H	X00

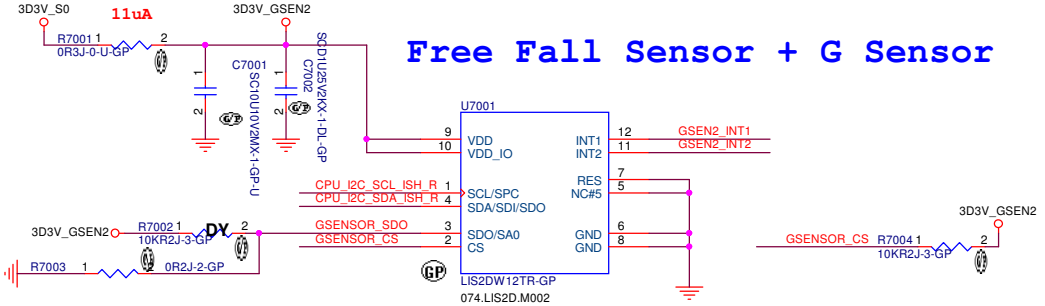
Date: Friday, November 13, 2020 Sheet 69 of 106

SSID = Free Fall Sensor

21 GSEN2_INT1_C
21 GSEN2_INT2_C

20 CPU_I2C_SDA_ISH
20 CPU_I2C_SCL_ISH

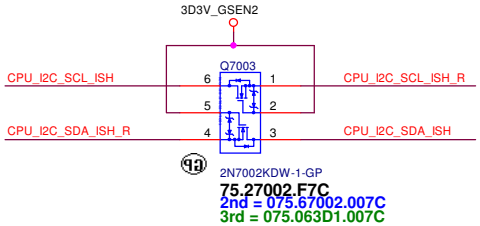
Free Fall Sensor + G Sensor



pch
3.3VV_S0

GSEN2_INT1_C R7005 1 0R2J-2-GP GSEN2_INT1
GSEN2_INT2_C R7006 1 0R2J-2-GP GSEN2_INT2

3.3V_S0



CPU

3.3V_S5

CPU_I2C_SCL_ISH R7007 1 DY 0R2J-2-GP CPU_I2C_SCL_ISH_R
CPU_I2C_SDA_ISH R7009 1 DY 0R2J-2-GP CPU_I2C_SDA_ISH_R

3.3V_S0

3D3V_GSEN2
R7045 10KR2J-3-GP
R7044 10KR2J-3-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Sensor (G-sensor)
Size: Custom
Document Number: Cyborg N5-H
Rev: X00
Date: Friday, November 13, 2020
Sheet 70 of 106

Main Func = TBT

HP team on applying, only murata have sample can meet Intel request

220nF AC cap must be placed on RX lines close to SOC side

TBT PORTS

MISC & DEBUG

Power

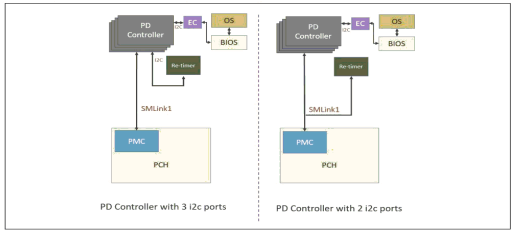
GND

Type-C PD

USB1

Main Func = TypeC

Figure 87. SMBus / SMlink Connectivity for USB Type-C PD Controller



Type-C PD

PD to SOC

PD to EC

PD to BB

PD to EC

CCG5's I2C address is decided by the SWD clock pin.
Don't mount R8 and R9 for the I2C address 0x08. This is the default one.
Mount only R9 for the I2C address 0x40.
Mount only R8 for the I2C address 0x42.

ID1

ID2

	Dell TGL Platform MOD_ID Options NEW		
Project	MOD_ID1	MOD_ID2	Description
Cyborg-TGL-H	L3	L2	TGL-H/BB8040/CCG6SF

	CCG6_ID	R7216	R7218	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.10035.6DL (100K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(2/3)/Type C CC Logic)
Size: A2 | Document Number: Cyborg N5-H | Rev: X00
Date: Friday, November 13, 2020 | Sheet 72 of 106

Main Func = TypeC

USB1

71 USB1_SSTX_CON_P0
71 USB1_SSTX_CON_N0
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N1

71 USB1_SSRX_AR_P0
71 USB1_SSRX_AR_N0
71 USB1_SSRX_AR_P1
71 USB1_SSRX_AR_N1

72 USB1_USB20_CMCT_P
72 USB1_USB20_CMCT_N
72 USB1_USB20_CMCB_P
72 USB1_USB20_CMCB_N

72 USB1_CON_CC1
72 USB1_CON_CC2

72 USB1_CON_SBU1
72 USB1_CON_SBU2

71 USB1_SSTX_C_P0
71 USB1_SSTX_C_N0
71 USB1_SSTX_C_P1
71 USB1_SSTX_C_N1

71 USB1_SSRX_C_P0
71 USB1_SSRX_C_N0
71 USB1_SSRX_C_P1
71 USB1_SSRX_C_N1

TYPEC1
SKT-USB28-45-GP
062.10009.M077

20V_VCCPD_VBUS
GND
SSTXP1
SSTXN1
VBUS#A4
CC1
DP1
DN1
RFU1
VBUS#A9
SSRXN2
SSRXP2
GND
SSTXP2
SSTXN2
VBUS#B4
CC2
DP2
DN2
RFU2
VBUS#B9
SSRXN1
SSRXP1
GND
CHASSIS#13
CHASSIS#14
CHASSIS#15
CHASSIS#16

FC7305 SCD1U25V2KX-1DL-GP

C7301 C7302 C7303 C7304 SCD1U25V1KX-GP

R7302 0R2J-2-GP
R7303 0R2J-2-GP
R7301 0R2J-2-GP
R7304 0R2J-2-GP
EL7302
EL7301
DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.01012.2011

teknisi indonesia

ED7301 ED7302 ED7303 ED7304 ED7305 ED7306 ED7307 ED7308
ED7309 ED7310 ED7311 ED7312 ED7313 ED7314 ED7315 ED7316
PESD5V0H1BSFYL-GP-U1
083.5V0H1.00AF
2nd = 083.08017.00AF

R7305 2MR2F-GP
R7306 2MR2F-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (Thunderbolt(3/3)/Type C Conn)
Size: A3
Document Number: Cyborg N5-H
Rev: X00
Date: Friday, November 13, 2020
Sheet 73 of 106

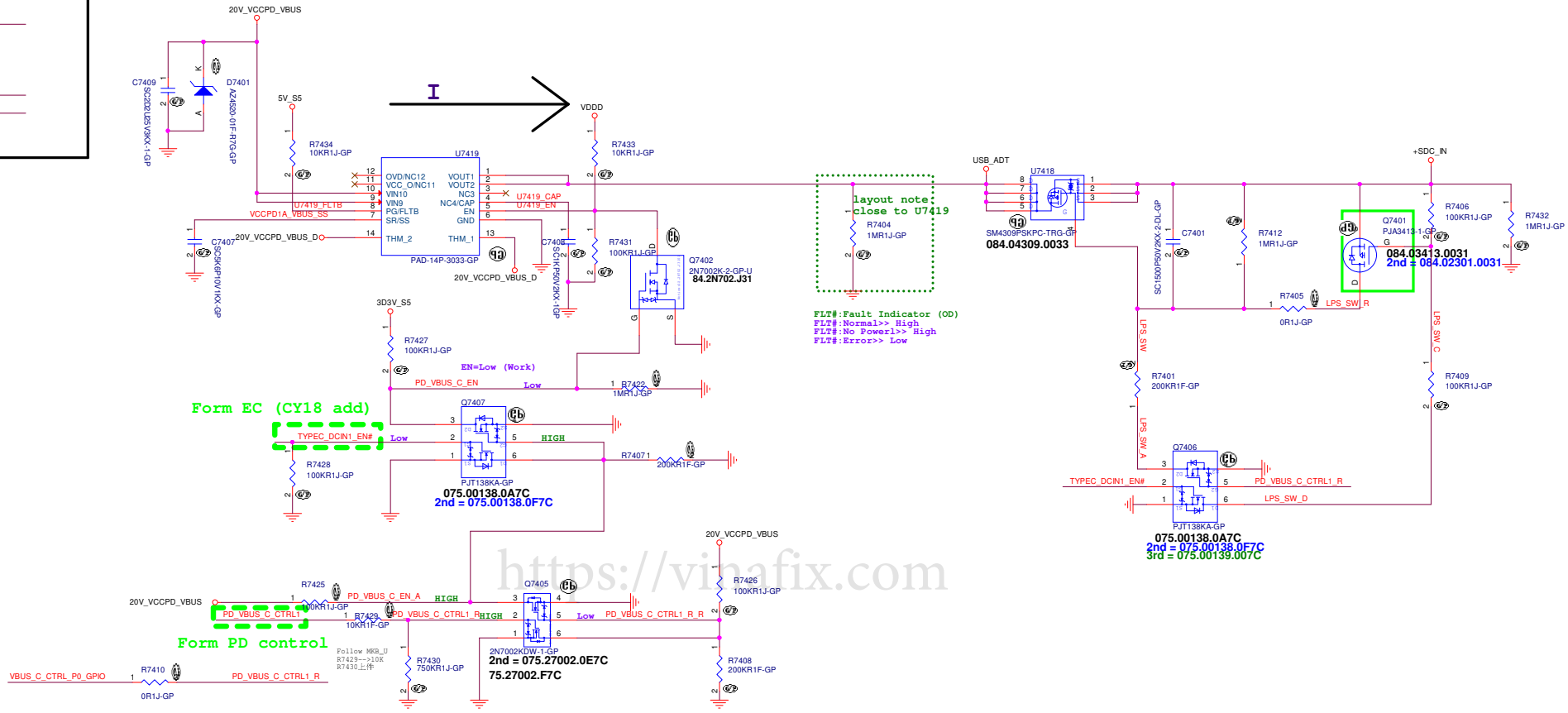
Main FUNC = LPS

D7401 Need change to AOZ8S515UDS-20 0928

44,72 PD_VBUS_C_CTRL1

72 VBUS_C_CTRL_P0_GPIO

24 TYPEC_DCIN1_EN#



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EXT IO (TYPEC Power delivery/VBUS)

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 13, 2020 | Sheet 74 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **EXT IO (RSVD)**

Size	Document Number	Rev
A	Cyborg N5-H	X00

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DG-09845-001_v01 P.46

Table 5. PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population GB5-128	Population GB5B-128	Location
PEX_DVDD and PEX_CVDD Supply Rails					
GB5-128, GB5B-128	1.0 µF	X6S	0402 or 0201W		
	4.7 µF	X6S	0603	2	2 Under GPU
	10 µF	X6S	0805	2	2 Near GPU
	22 µF	X6S	0805	1	1 Near GPU
PEX_HVDD and PEX_PLL_HVDD Supply Rails					
GB5-128, GB5B-128	1.0 µF	X6S	0402 or 0201W	3	3 Under GPU
	4.7 µF	X6S	0603	2	2 Under GPU
	10 µF	X6S	0805	2	2 Near GPU
	22 µF	X6S	0805	1	1 Near GPU

▶ PEX_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8_AON.

EMI Reserved

VGA_RST#

EC7601 SCD22U10V2KX-2GP

20,24,86 DGPU_PWROK
21 CLK_PCIE_PEG_REQ#
79 VGA_RST#
19 GFX_CLK_CPU_P
19 GFX_CLK_CPU_N

3 GFX_PCIE_RX_P0 / 3 GFX_PCIE_RX_N0 / 3 GFX_PCIE_TX_CON_P0 / 3 GFX_PCIE_TX_CON_N0
3 GFX_PCIE_RX_P1 / 3 GFX_PCIE_RX_N1 / 3 GFX_PCIE_TX_CON_P1 / 3 GFX_PCIE_TX_CON_N1
3 GFX_PCIE_RX_P2 / 3 GFX_PCIE_RX_N2 / 3 GFX_PCIE_TX_CON_P2 / 3 GFX_PCIE_TX_CON_N2
3 GFX_PCIE_RX_P3 / 3 GFX_PCIE_RX_N3 / 3 GFX_PCIE_TX_CON_P3 / 3 GFX_PCIE_TX_CON_N3
3 GFX_PCIE_RX_P4 / 3 GFX_PCIE_RX_N4 / 3 GFX_PCIE_TX_CON_P4 / 3 GFX_PCIE_TX_CON_N4
3 GFX_PCIE_RX_P5 / 3 GFX_PCIE_RX_N5 / 3 GFX_PCIE_TX_CON_P5 / 3 GFX_PCIE_TX_CON_N5
3 GFX_PCIE_RX_P6 / 3 GFX_PCIE_RX_N6 / 3 GFX_PCIE_TX_CON_P6 / 3 GFX_PCIE_TX_CON_N6
3 GFX_PCIE_RX_P7 / 3 GFX_PCIE_RX_N7 / 3 GFX_PCIE_TX_CON_P7 / 3 GFX_PCIE_TX_CON_N7

DGPU_PWROK
PJA138KA-GP Q7602
CLK_PCIE_PEG_REQ#
1D8V_AON_S0
R7604 10KR2J-3-GP
VGA_RST#
GFX_CLKREQ_dGPU_N

GFX_CLK_CPU_P / GFX_CLK_CPU_N

GFX_PCIE_RX_P0 / GFX_PCIE_RX_N0 — C7601 / C7602 SCD22U10V2KX-2-GP — GFX_PCIE_RX_C_P0 / GFX_PCIE_RX_C_N0
GFX_PCIE_TX_CON_P0 / GFX_PCIE_TX_CON_N0
GFX_PCIE_RX_P1 / GFX_PCIE_RX_N1 — C7603 / C7604 SCD22U10V2KX-2-GP — GFX_PCIE_RX_C_P1 / GFX_PCIE_RX_C_N1
GFX_PCIE_TX_CON_P1 / GFX_PCIE_TX_CON_N1
GFX_PCIE_RX_P2 / GFX_PCIE_RX_N2 — C7605 / C7606 SCD22U10V2KX-2-GP — GFX_PCIE_RX_C_P2 / GFX_PCIE_RX_C_N2
GFX_PCIE_TX_CON_P2 / GFX_PCIE_TX_CON_N2
GFX_PCIE_RX_P3 / GFX_PCIE_RX_N3 — C7607 / C7608 SCD22U10V2KX-2-GP — GFX_PCIE_RX_C_P3 / GFX_PCIE_RX_C_N3
GFX_PCIE_TX_CON_P3 / GFX_PCIE_TX_CON_N3
GFX_PCIE_RX_P4 / GFX_PCIE_RX_N4 — C7609 / C7610 SCD22U10V2KX-2-GP — GFX_PCIE_RX_C_P4 / GFX_PCIE_RX_C_N4
GFX_PCIE_TX_CON_P4 / GFX_PCIE_TX_CON_N4
GFX_PCIE_RX_P5 / GFX_PCIE_RX_N5 — C7611 / C7612 SCD22U10V2KX-2-GP — GFX_PCIE_RX_C_P5 / GFX_PCIE_RX_C_N5
GFX_PCIE_TX_CON_P5 / GFX_PCIE_TX_CON_N5
GFX_PCIE_RX_P6 / GFX_PCIE_RX_N6 — C7613 / C7614 SCD22U10V2KX-2-GP — GFX_PCIE_RX_C_P6 / GFX_PCIE_RX_C_N6
GFX_PCIE_TX_CON_P6 / GFX_PCIE_TX_CON_N6
GFX_PCIE_RX_P7 / GFX_PCIE_RX_N7 — C7615 / C7616 SCD22U10V2KX-2-GP — GFX_PCIE_RX_C_P7 / GFX_PCIE_RX_C_N7
GFX_PCIE_TX_CON_P7 / GFX_PCIE_TX_CON_N7

GPU1A 1 OF 17
1/17 PCI_EXPRESS

AP11	PEX_WAKE#	
AN11	PEX_RST#	
AU11	PEX_CLKREQ#	
AR12	PEX_REFCLK	
AT12	PEX_REFCLK#	
AN13	PEX_TX0	GFX_PCIE_RX_C_P0
AP13	PEX_TX0#	GFX_PCIE_RX_C_N0
AV13	PEX_RX0	
AW13	PEX_RX0#	
AR14	PEX_TX1	GFX_PCIE_RX_C_P1
AT14	PEX_TX1#	GFX_PCIE_RX_C_N1
AW14	PEX_RX1	
AY14	PEX_RX1#	
AN15	PEX_TX2	GFX_PCIE_RX_C_P2
AP15	PEX_TX2#	GFX_PCIE_RX_C_N2
AV15	PEX_RX2	
AW15	PEX_RX2#	
AR16	PEX_TX3	GFX_PCIE_RX_C_P3
AT16	PEX_TX3#	GFX_PCIE_RX_C_N3
AW16	PEX_RX3	
AY16	PEX_RX3#	
AN17	PEX_TX4	GFX_PCIE_RX_C_P4
AP17	PEX_TX4#	GFX_PCIE_RX_C_N4
AV17	PEX_RX4	
AW17	PEX_RX4#	
AR18	PEX_TX5	GFX_PCIE_RX_C_P5
AT18	PEX_TX5#	GFX_PCIE_RX_C_N5
AW18	PEX_RX5	
AY18	PEX_RX5#	
AN19	PEX_TX6	GFX_PCIE_RX_C_P6
AP19	PEX_TX6#	GFX_PCIE_RX_C_N6
AV19	PEX_RX6	
AW19	PEX_RX6#	
AR20	PEX_TX7	GFX_PCIE_RX_C_P7
AT20	PEX_TX7#	GFX_PCIE_RX_C_N7
AW20	PEX_RX7	
AY20	PEX_RX7#	
AN21	PEX_TX8	
AP21	PEX_TX8#	
AV21	PEX_RX8	
AW21	PEX_RX8#	
AR22	PEX_TX9	
AT22	PEX_TX9#	
AW22	PEX_RX9	
AY22	PEX_RX9#	
AN23	PEX_TX10	
AP23	PEX_TX10#	
AV23	PEX_RX10	
AW23	PEX_RX10#	
AR24	PEX_TX11	
AT24	PEX_TX11#	
AW24	PEX_RX11	
AY24	PEX_RX11#	
AN25	PEX_TX12	
AP25	PEX_TX12#	
AV25	PEX_RX12	
AW25	PEX_RX12#	
AR26	PEX_TX13	
AT26	PEX_TX13#	
AW26	PEX_RX13	
AY26	PEX_RX13#	
AN27	PEX_TX14	
AP27	PEX_TX14#	
AV27	PEX_RX14	
AW27	PEX_RX14#	
AR28	PEX_TX15	
AT28	PEX_TX15#	
AW28	PEX_RX15	
AY28	PEX_RX15#	

NG-GN20-P0-GP
DIS

PCIE/PLL DIGITAL PWR — 1V Interface

PEX_DVDD_1	AL27
PEX_DVDD_2	AL28
PEX_DVDD_3	AL29
PEX_DVDD_4	AM26
PEX_DVDD_5	AM28
PEX_DVDD_6	AM29
PEX_DVDD_7	AM30
PEX_DVDD_8	AN29
PEX_DVDD_9	AN30
PEX_DVDD_10	AP30
PEX_DVDD_11	AR30
PEX_DVDD_12	AT30
PEX_DVDD_13	AU30
PEX_DVDD_14	AV30
PEX_DVDD_15	AW30
PEX_DVDD_16	AY30
PEX_CVDD_1	AL24
PEX_CVDD_2	AL25
PEX_CVDD_3	AL26
PEX_CVDD_4	AM24

PCIE/PLL ANALOG PWR — 1.8V Interface

PEX_HVDD_1	AL17
PEX_HVDD_2	AL18
PEX_HVDD_3	AL19
PEX_HVDD_4	AL20
PEX_HVDD_5	AL21
PEX_HVDD_6	AL22
PEX_HVDD_7	AL23
PEX_HVDD_8	AM16
PEX_HVDD_9	AM18
PEX_HVDD_10	AM20
PEX_PLL_HVDD	AM22
PEX_CVDD_SENSE	AU29
PEX_TERMP	AW29

PEX_TERMP — R7607 2K49R2F-GP — R7607 Close to GPU

1V_VGA_S0

1U 0201*4 X6S Place under GPU: C7627 C7628 C7629 C7630 C7631 C7632 SCU1U4V1MX-1NF-GP
4.7U 0603*2 X6S Place under GPU: C7633 C7634 C7635 SC4D7U10V6KX-6GP
10U 0805*2 X6S Place near GPU: C7650 C7624 C7623 SC10U6D3V5KX-3DGP
22U 0603*1 X6S Place near GPU: C7636 C7637 SC22U6D3V3MX-1GP

1D8V_VGA_S0

1U 0201*3 X6S Place under GPU: C7638 C7639 C7640 C7641 C7642 C7643 C7652 SCU1U4V1MX-1NF-GP
4.7U 0603*2 X6S Place under GPU: C7645 C7646 C7647 SC4D7U10V6KX-6GP
10U 0805*2 X6S Place near GPU: C7648 C7649 C7651 SC10U6D3V5KX-3DGP
22U 0603*1 X6S Place near GPU: C7660 C7661 SC22U6D3V3MX-1GP

ref sch not stuff
PDP-09900-004_v01_GB5-128_GDDR6_REF_SCH P.3

1U 0201*1 X6S Place under GPU: C7644 SCU1U4V1MX-1NF-GP

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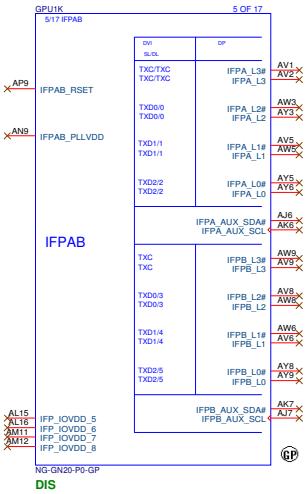
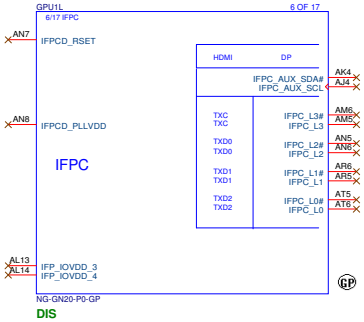
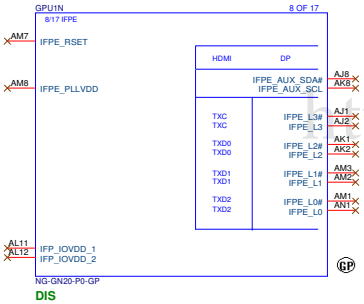
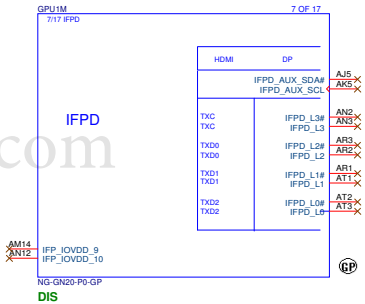
Main Func = dGPU









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Group A

Group B

1.8V Interface

FRAME BUFFER PLL PWR

Place Under GPU

1U 0201*1 X6S

Follow reference schematic

G6 x16 MODE_3 CMD MAPPING

Low 32Bits Mapping

High 32Bits Mapping

Table 8.36 CKE1* and CKE2* Pull-Up Resistors

GDDR5 DRAM Connectivity Mode	CKE* Signals for Any Frame Buffer Partition	
	CKE1*	CKE2*
32-Bit Mode	Pull-up resistor, 10 KΩ to FBVDDQ	Pull-up resistor, 10K Ω to FBVDDQ

Group A

CKE_A

CKE_B

Reset

Group B

CKEB

Check Value DIS

DA-09899-001_v03 P.9

DA-09899-001_v03 P.32

Table 13. GB5-128 and GB5B-128 FB BOM Differences

DA-09899-001_v03 P.23

Table 3. Frame Buffer Core and IO Decoupling and Filtering

Table 4. Frame Buffer PLL3 Decoupling and Filtering

Partition A

Partition B

Place under GPU

4.7U 0603*2 X6S

22U 0603*5 X6S

10U 0603*2 X6S

68.00334.051

Reference schematic : 0.47uF (Need to apply P/N)

PDP-09900-004_v01_GB5-128_GDDR6_REF_SCH P.20

FBVDDQ

FBVDDQ_SENSE

FB_CAL_PD_VDDQ

FB_CAL_PU_GND

FB_CAL_TERM_GND

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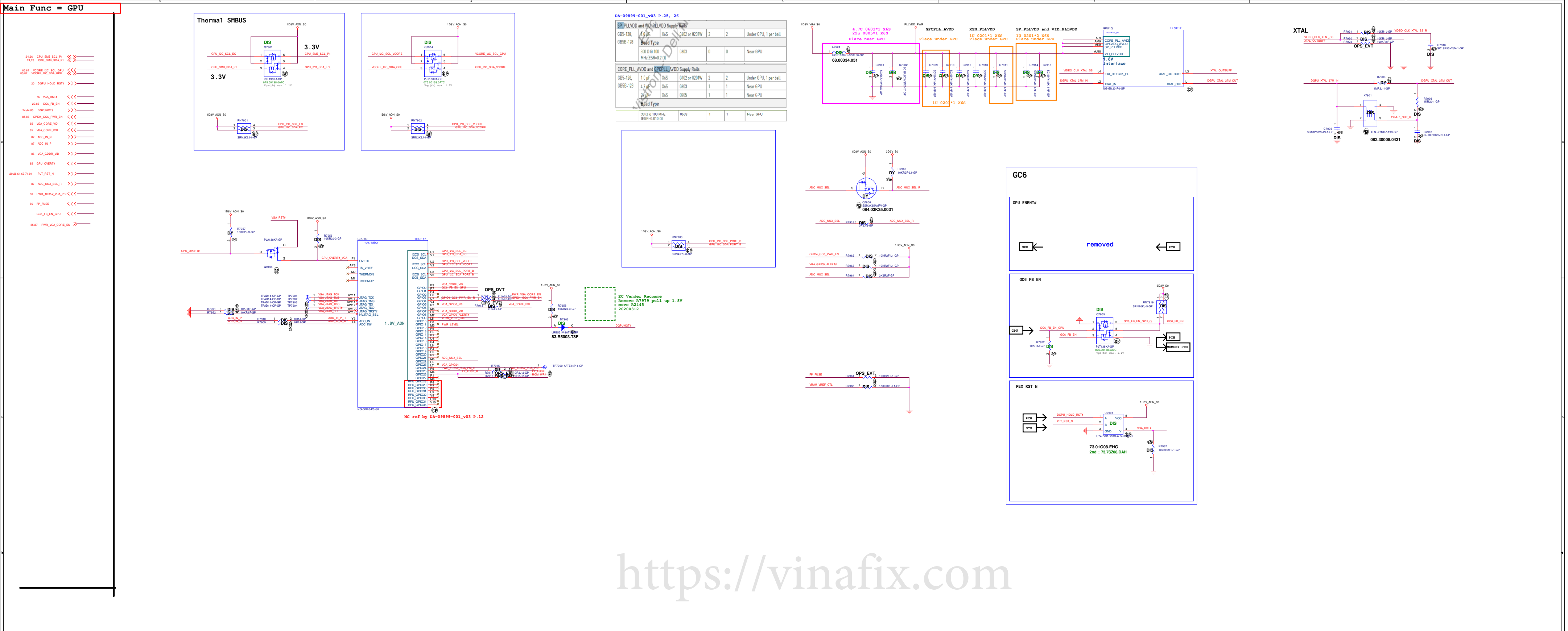
GPU (VRAM 3/5)

Cyborg N5-H

X00



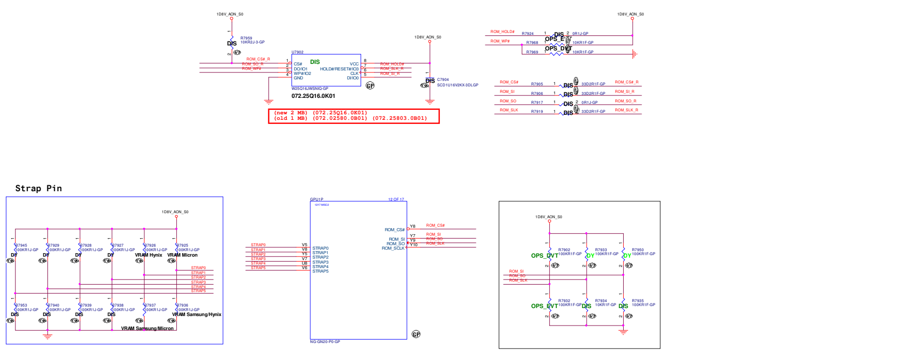


Table 4. GN20-P1/P0 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001[2]	Full	Production candidate
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate
			Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940[3]	Full	Production candidate

Notes:
[1] DVS is required to run WCLK > 5500 MHz.
[2] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.
[3] Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
For GN20-P1/P0, the maximum allowable memory case temperature is 95 °C.

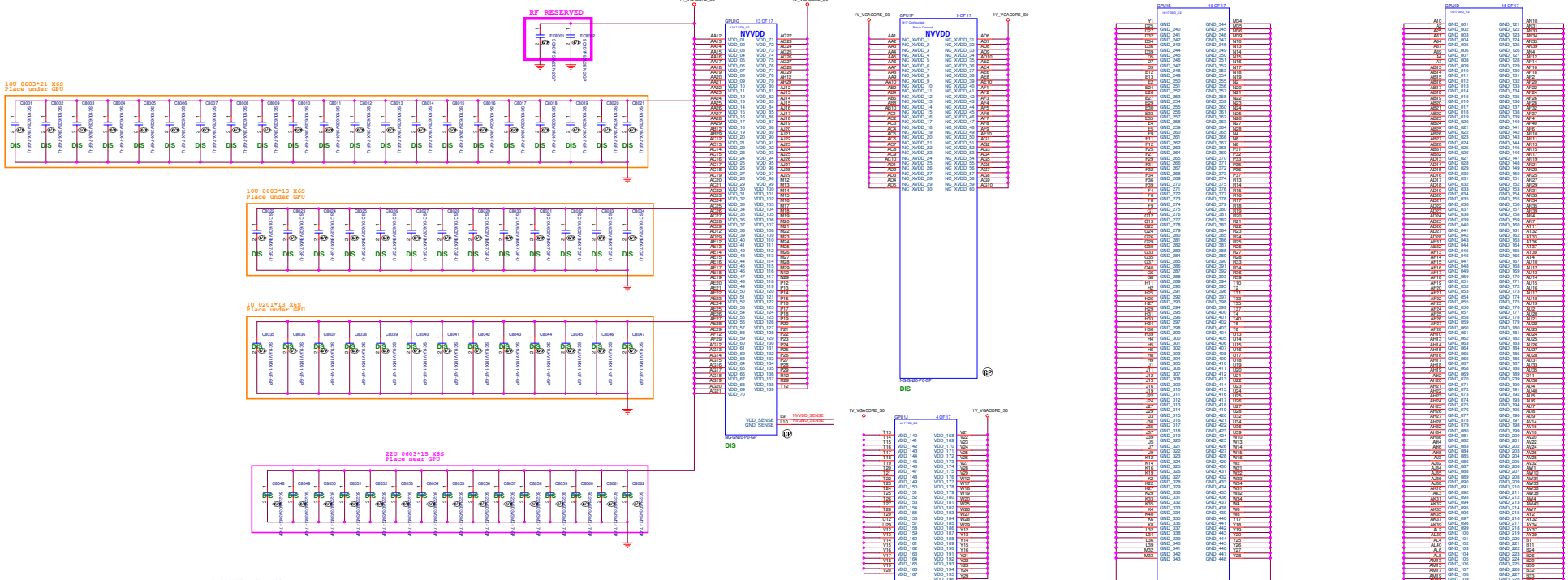
Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)

Table 15.1 GPIO Descriptions for GB4D-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	No PU/PD
GPIO1	GC6: GC6_FB_EN	I/O	FB Enable for GC6 2.1	10 kΩ pull-down
GPIO2	GC6:GPU_EVENT	I/O	GPU wake signal for GC6 2.1	10 kΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	UNUSED	O		
GPIO4	GC6: 1V8_MAIN_EN	I	GPU power sequencing for GC6 2.1	10 kΩ pull-up to 1V8_AON
GPIO5	FRAME_LOCK*	O	Active low Frame Lock	10 kΩ pull-up to 1V8_AON
GPIO6	NVVDD_PSI*		Phase Shedding (see Section 15.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	LCD Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT*	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	10K Pull Up
GPIO13	UNUSED			
GPIO14	HPD_IFPA*	I	Hot Plug Detect for IFPA	10K Pull Up to 1V8_AON
GPIO15	HPD_IFPB*	I	Hot Plug	10K Pull Up to 1V8_AON
GPIO16	UNUSED			
GPIO17	HPD_IFPD*	I	Hot Plug Detect for IFPD	10K Pull Up to 1V8_AON
GPIO18	HPD_IFPE*	I	Hot Plug Detect for IFPE	10K Pull Up to 1V8_AON
GPIO19	UNUSED	O		
GPIO20	GC6:NB_GC6	I/O		10K Pull Down
GPIO21	LCD_BLEN	O	LCD Panel Backlight enable	100K Pull Down
GPIO22	INA_HT* / ADC_MUX_SEL			2.2K Pull Up See circuit
GPIO23	Reserved			100K Pull Down
GPIO24	UNUSED	I		
GPIO25	FBVDD_PSI*			PU/PD with series resistor depending on PSI topology
GPIO26	FP_FUSE			10K Pull Down
GPIO27	HPD_IFPC*	I	Hot plug detect for IFPC	10K Pull Up to 1V8_AON

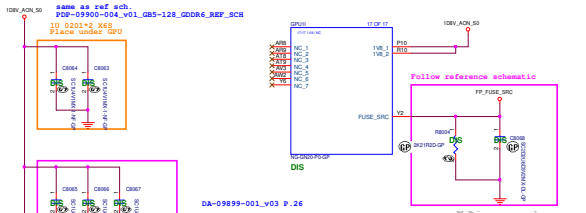
Main Func = GPU



DA-09899-001_v03 P.23

Table 2. NVVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population GB5-128	Population GB5B-128	Location
NVVDD Supply Net					
GB5-128	1 µF	X6S	0402 or 0201W	13	13	Under GPU
GB5B-128	10 µF	X6S	0603	34	34	Under GPU
	22 µF	X6S	0805	15	15	Near GPU



DA-09899-001_v03 P.26

Table 8. 1V8 Decoupling

GPU	Capacitor Type	Footprint	Population GB5-128	Population GB5B-128	Location
1V8 Supply Rails					
GB5-128,	1.0 µF	X6S	0402 or 0201W	2	2	Under GPU
GB5B-128	1.0 µF	X6S	0402 or 0201W	3	3	Near GPU
	4.7 µF	X6S	0603	3	3	Near GPU

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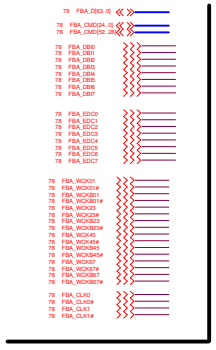
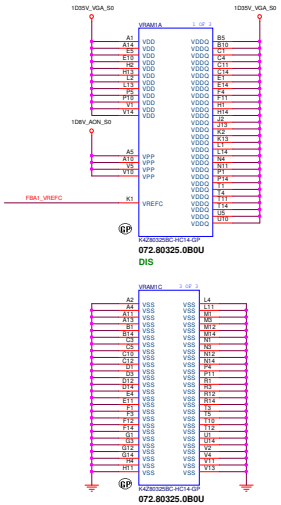
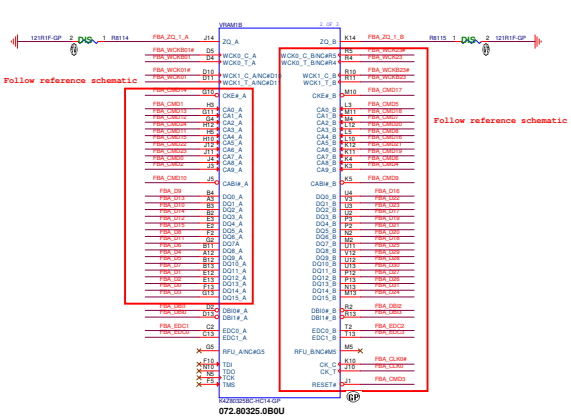
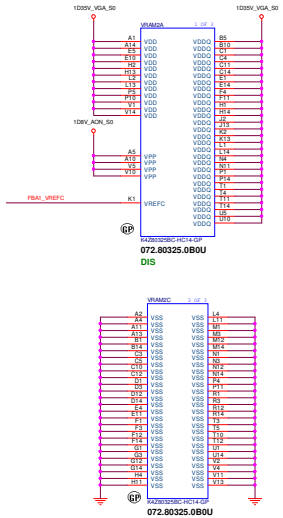
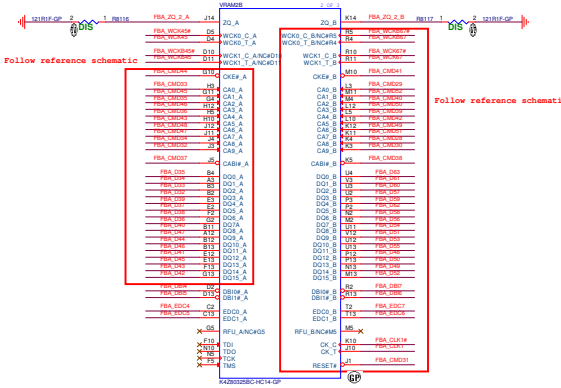










8.2.2.14 GDDR6 DRAM VREFC

GDDR6 DRAMs include an integrated VREFC (VREF for CMD and ADDR). Figure 8.8 illustrates use of the integrated VREFC for x16 mode GDDR6 DRAMs. Refer to the reference schematics for final component values.

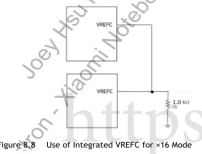
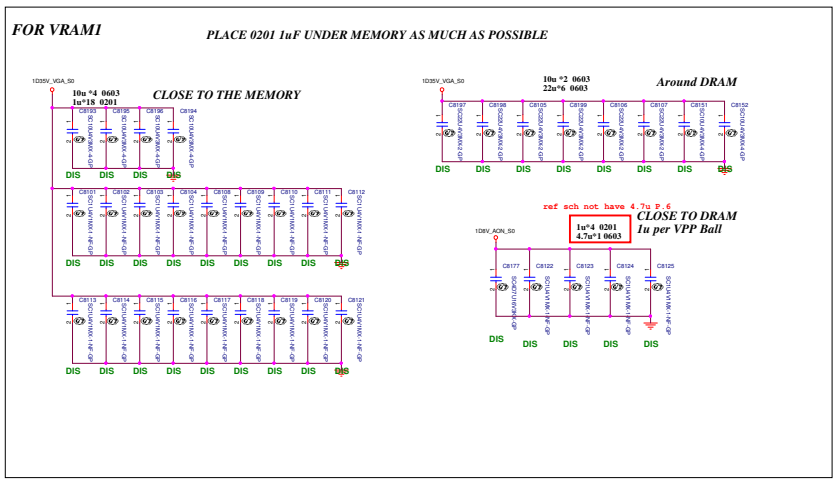
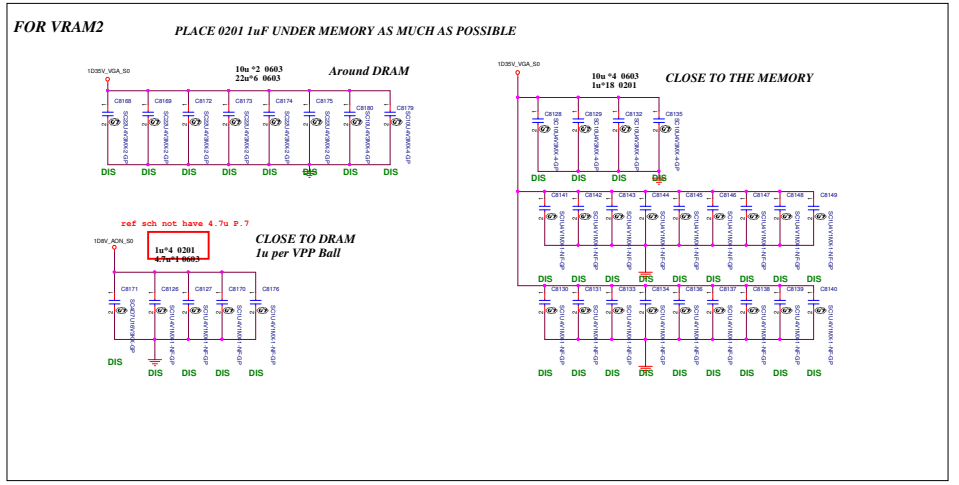


Figure 8.8 Use of Integrated VREFC for ×16 Mode





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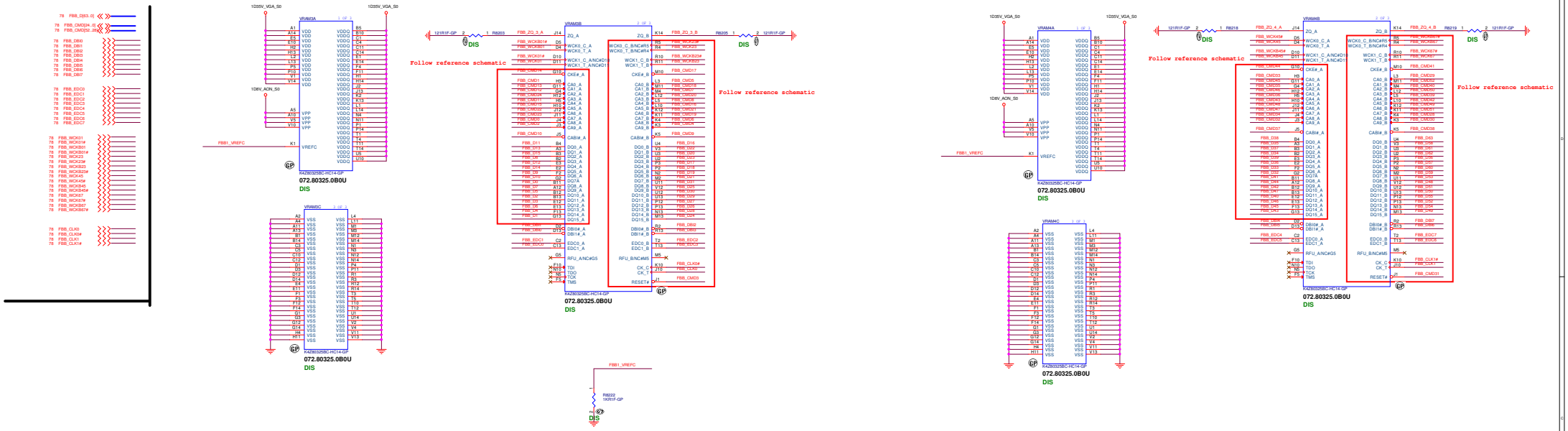
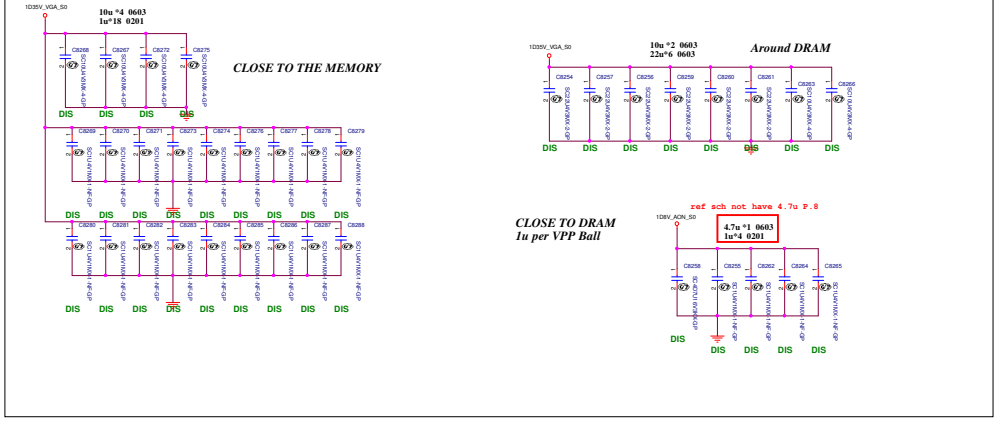
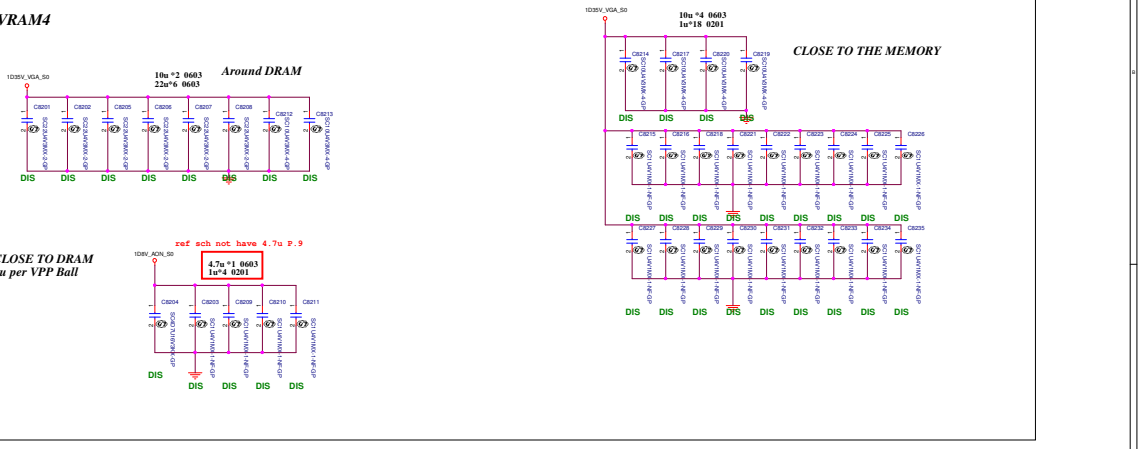


FOR VRAM3



FOR VRAM4



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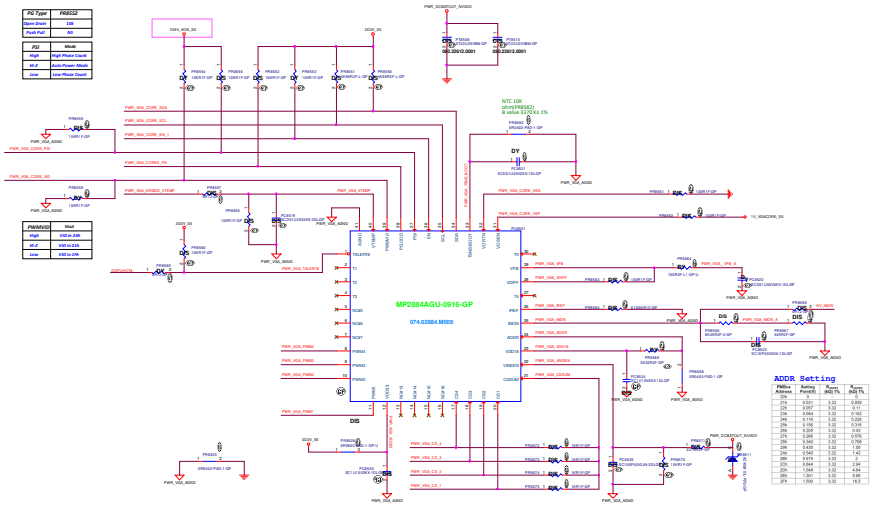
MP2884A For VGA core

VGA : GN20-P0
EDP-Continuous : 52 A
EDP-Peak : 211 A



PG Type	PR8512
Open Drain	10k
Push Pull	NO

PSI	Mode
High	High Phase Count
Mid	Auto-Power Mode
Low	Low Phase Count

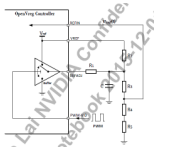
PWMVID	Vout
High	VID to 2Vh
Mid	VID to 21h
Low	VID to 19h

ADDR Setting

PMBus Address	Setting Point (K)	R_{ADDR} (KΩ) TOL. 1%	R_{ADDR} (KΩ) TOL. 1%
219	0.511	3.32	0.899
224	0.557	3.32	0.11
229	0.604	3.32	0.402
234	0.649	3.32	0.698
239	0.715	3.32	0.249
244	0.309	3.32	0.43
249	0.358	3.32	0.976
254	0.340	3.32	0.768
259	0.392	3.32	1.15
264	0.543	3.32	1.43
269	0.675	3.32	2
274	0.844	3.32	2.49
279	1.048	3.32	4.64
284	1.215	3.32	8.66
289	1.504	3.32	14.3

Table 7.8 PWM-VID Spec and Component Values

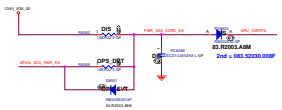
PWM-VID Specification		Config
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{PWM}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.887
C	nF	0.1



	PR8590	PR8591	PR8592	PR8593	PHASE5	PHASE6
6 Phase	DY	DY	DY	DY	stuff	stuff
4 Phase	10kOhm	10kOhm	DY	DY	DY	DY
3 Phase	10kOhm	10kOhm	10kOhm	DY	DY	DY
2 Phase	10kOhm	10kOhm	10kOhm	10kOhm	DY	DY

Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification		Config
Vmin	V	0.3
Vmax	V	1.3
Vboot	V	0.8
Voltage Step Vstep	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F_{PWM}	kHz	675
PWM Minimum Pulse Width T_{PWM}	ns	9.26
VID Transient Time T	us	<100
Component Value		
R1 (1%)	KΩ	6.19
R2 (1%)	KΩ	20.5
R3 (1%)	KΩ	4.32
R4 (1%)	KΩ	16.5
R5 (1%)	KΩ	0.887
C	nF	0.1



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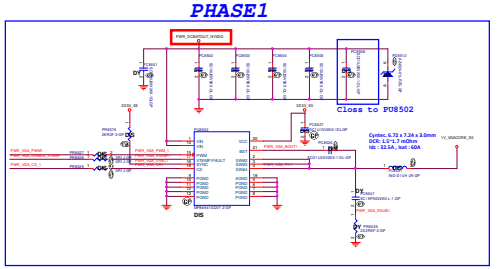

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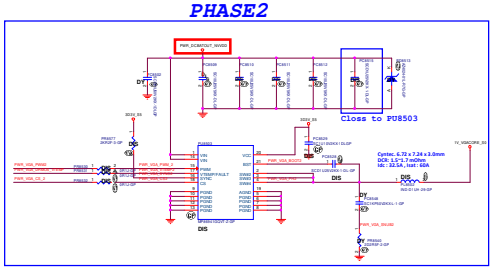

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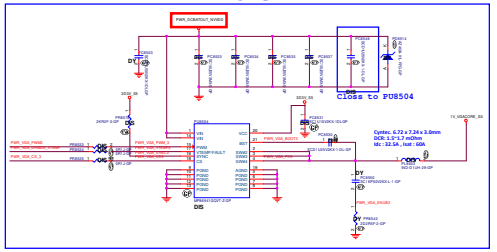

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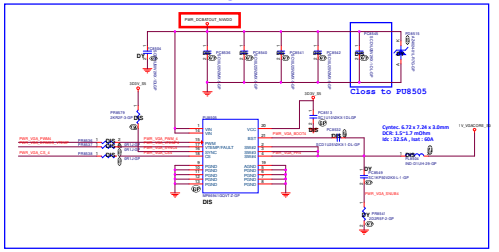
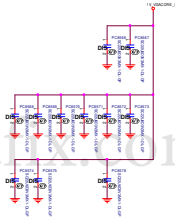
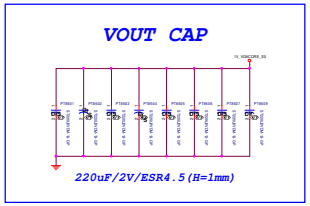


Vout MLCC



VOUT CAP



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GPU VCORE POWER
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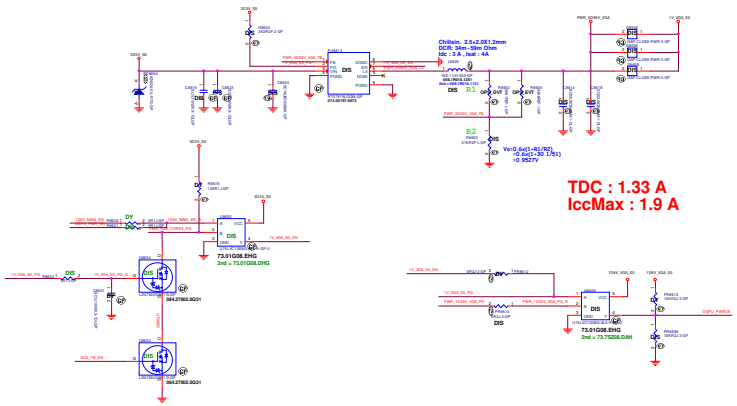
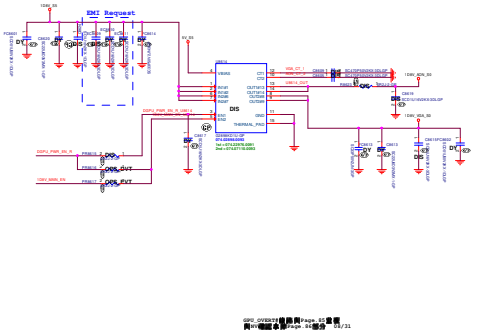
RT5797 for 0D95V_VGA_S0



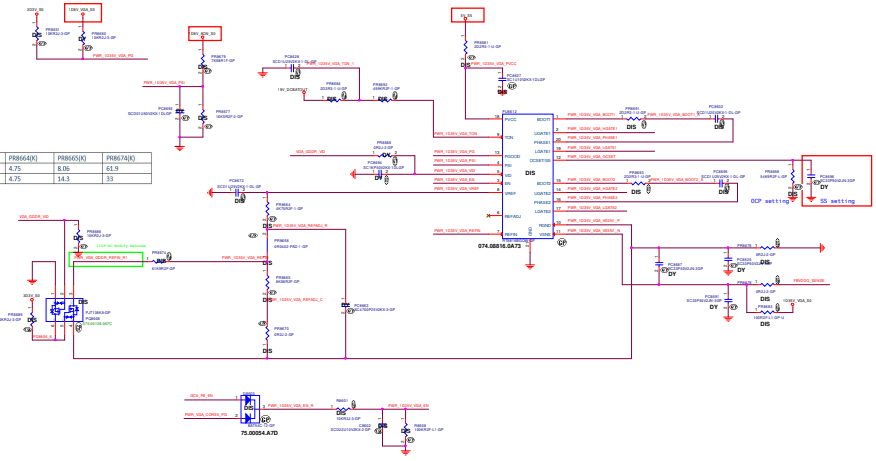
AOZ2260 For VGA 1D8V

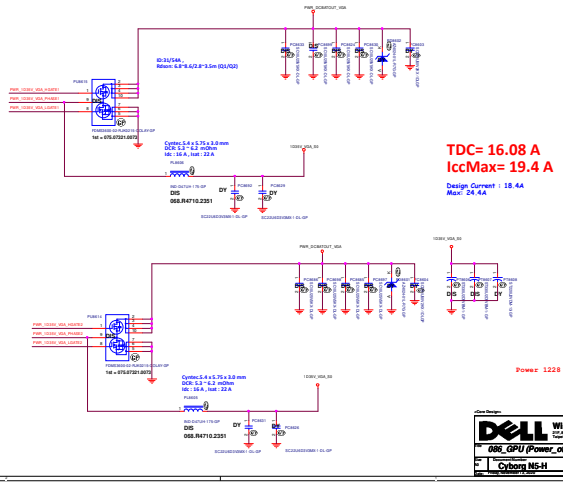


FP_FUSE_SRC

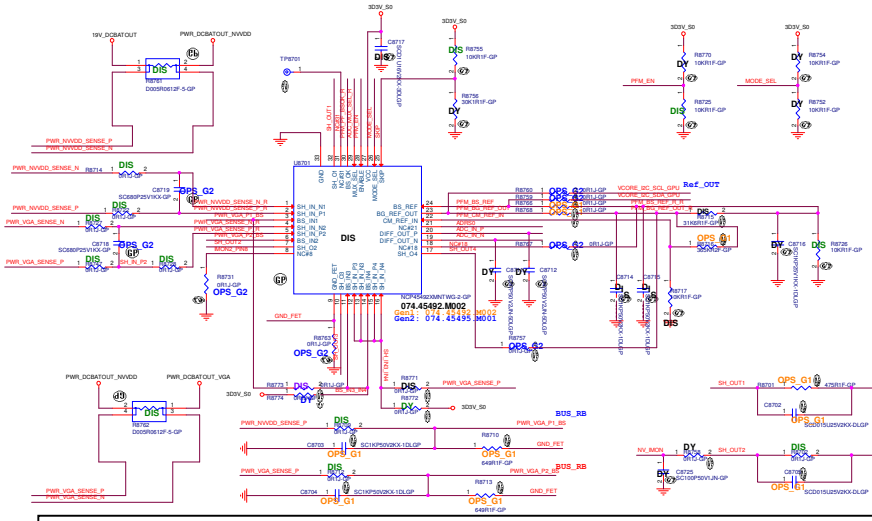
RT8816B for 1D35V_VGA_S0

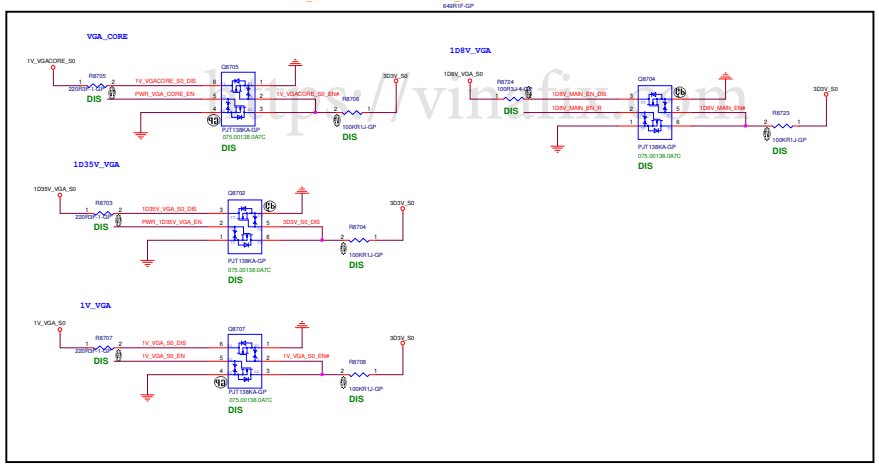
		P8866(K)	P8865(K)	P8674(K)
GDDR6	1.25/1.2v	4.75	8.06	61.9
GDDR5	1.5/1.35	4.75	14.3	33





Wistron Corporation
086_GPU (Power_others)
Cyborg N5-H
X00





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Title: 087_GPU (EE_Power)

Size: D | Document Number: Cyborg N5-H | Rev: X00

Date: Friday, November 19, 2010 | Sheet 87 of 106

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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *GPU (Discharge/Sequence)*

Size	Document Number	Rev
A4	Cyborg N5-H	X00

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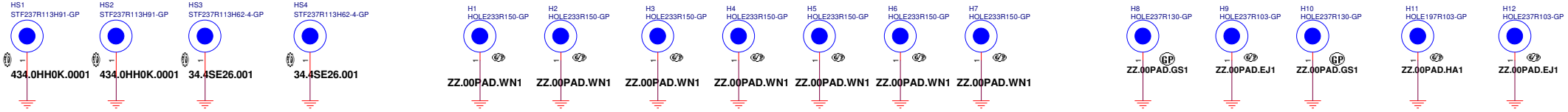
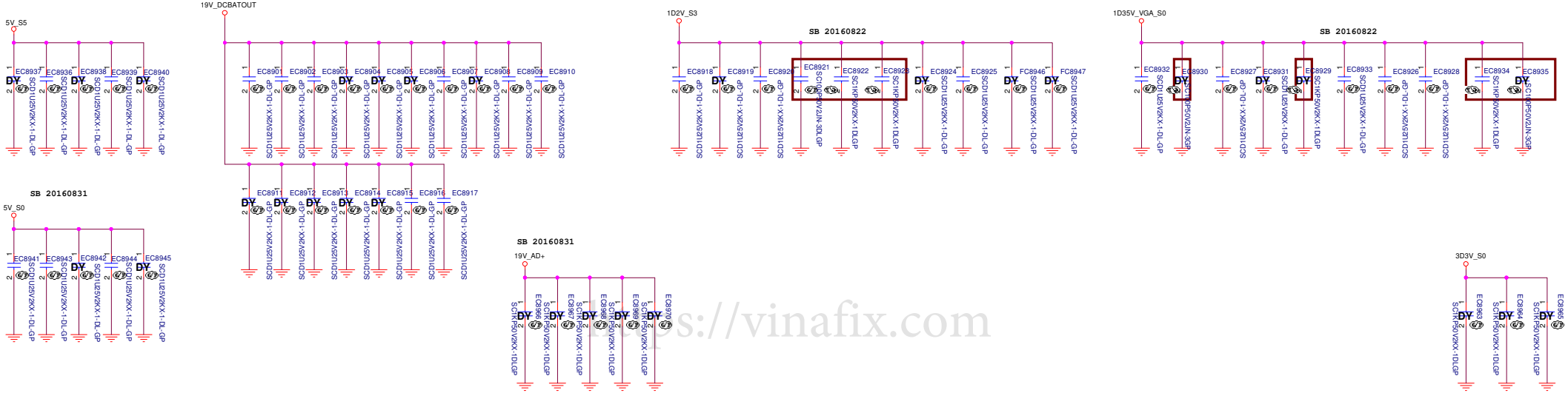
Main Func = UnusedParts

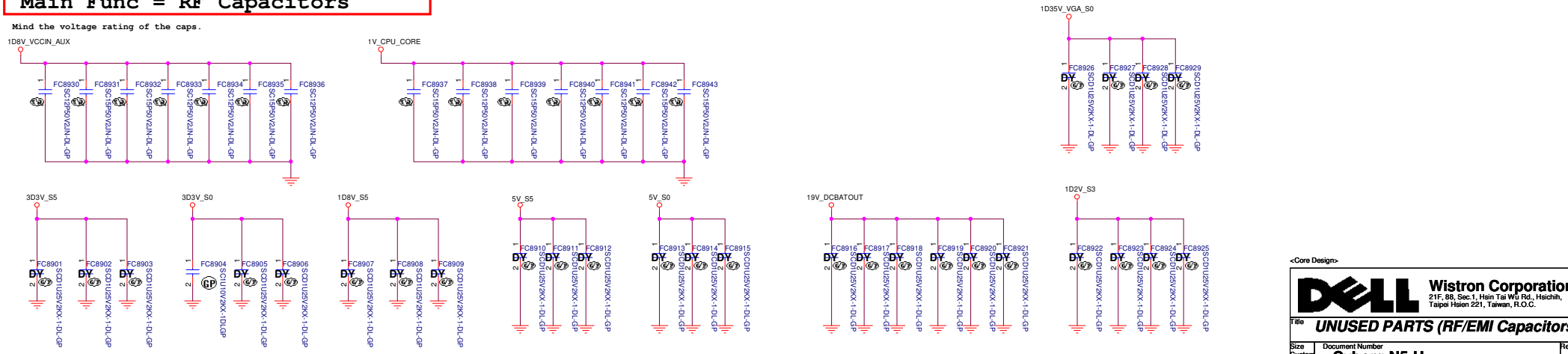


Main Func = EMI Capacitors



Main Func = RF Capacitors

Mind the voltage rating of the caps.



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Title: UNUSED PARTS (RF/EMI Capacitors)

Size	Document Number	Rev
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Title: *INT IO (NFC/Camera/Touch)*

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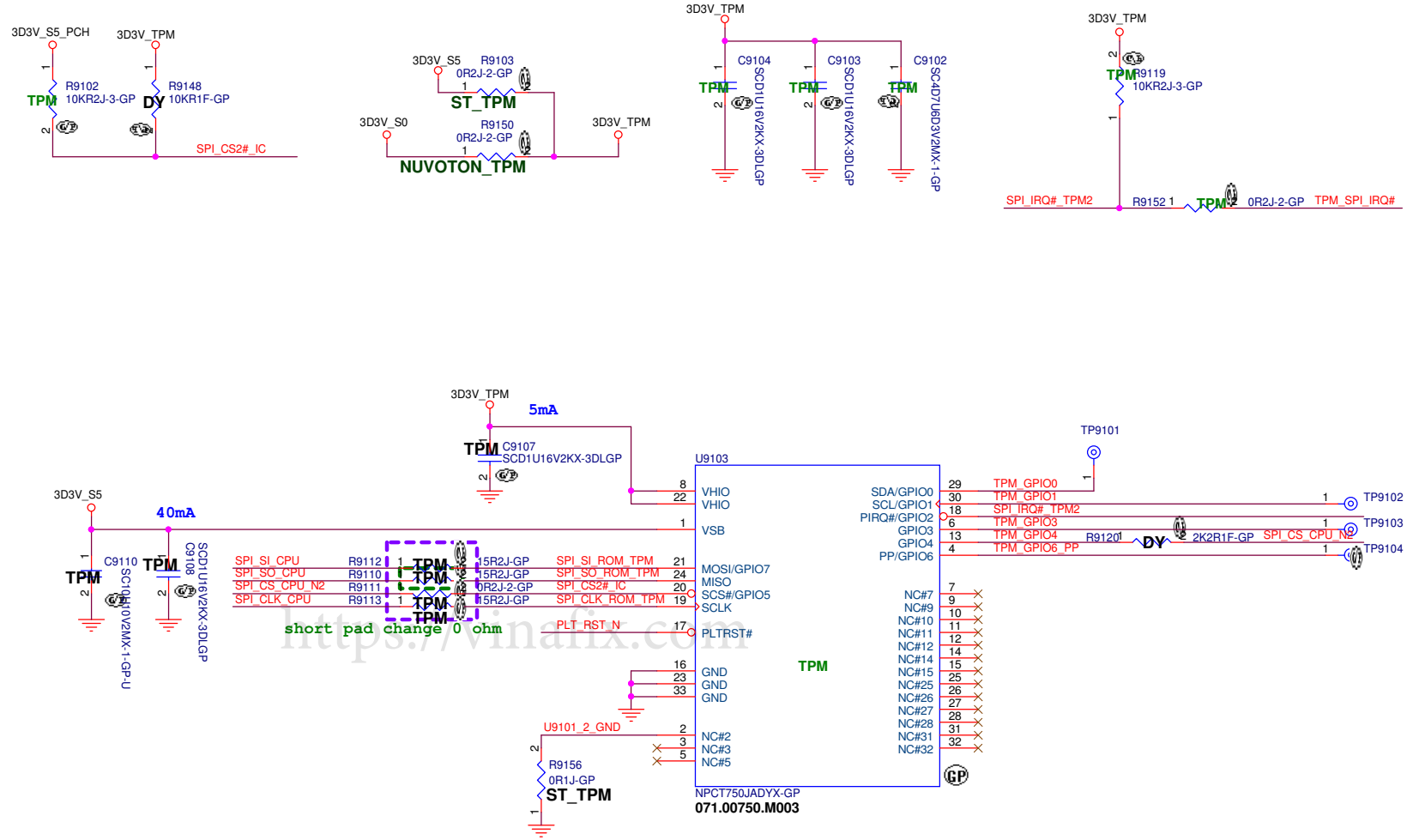
SSID = TPM

18,24,25 SPI_SO_CPU
18,24,25 SPI_CLK_CPU
11,18,24,25 SPI_SI_CPU
18 SPI_CS_CPU_N2

20,26,61,63,71,79 PLT_RST_N
20 PM_SLP_S0#

20 TPM_SPI_IRQ#

R9110.R9112.R9113	
SPI ROM	33 ohm 64.33R05.6DL
SHARE ROM	15 ohm 63.15034.1DL



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Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (TPM)

Size: Custom | Document Number: Cyborg N5-H | Rev: X00

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Title: *INT IO (RSVD)*

Size: A3 | Document Number: *Cyborg N5-H* | Rev: *X00*

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<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(RSVD)*

Size	Document Number	Rev
A	Cyborg N5-H	X00

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<Core Design>

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Title: ***(RSVD)***

Size	Document Number	Rev
A4	**Cyborg N5-H**	**X00**

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title ***(RSVD)***

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

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Core Design

DELL Wistron Corporation
No. 21, Sec. 1, Hsi Chih Rd., Hsichih,
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Title: Commercial (RSVD)

Size: D | Document Number: Cyborg N5-H | Rev: X00

Date: Tuesday, February 27, 2007 | Sheet: 55 of 57

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Commercial (RSVD)***

Size	Document Number	Rev
A	**Cyborg N5-H**	**X00**

Date: Friday, November 13, 2020 Sheet 97 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Commercial (RSVD)*

Size	Document Number	Rev
C	Cyborg N5-H	X00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title *(RSVD)*

Size	Document Number	Rev
A3	Cyborg N5-H	X00

Date: Friday, November 13, 2020 Sheet 99 of 106

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(RSVD)*

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A	Cyborg N5-H	X00

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8/29 add XDP
9/26 3.3V(PU4501),DDR(PU5101),1.05V(PU5201)change to solution.

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Title *(RSVD)*

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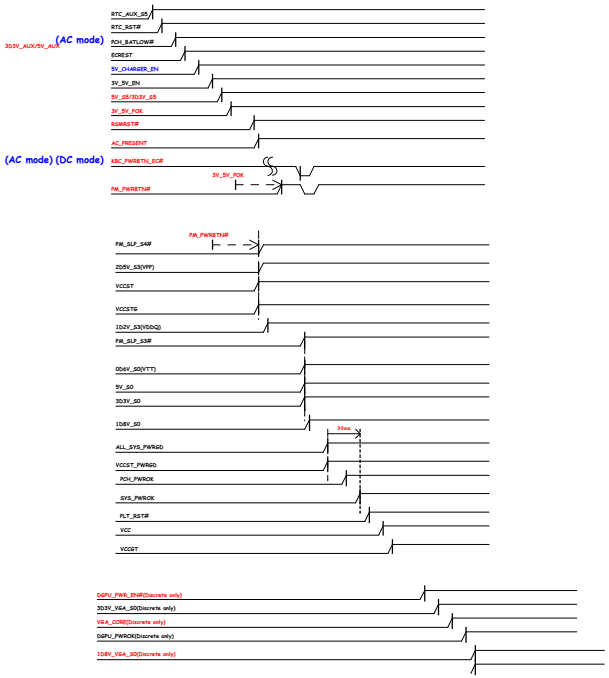
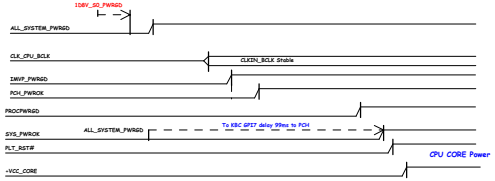
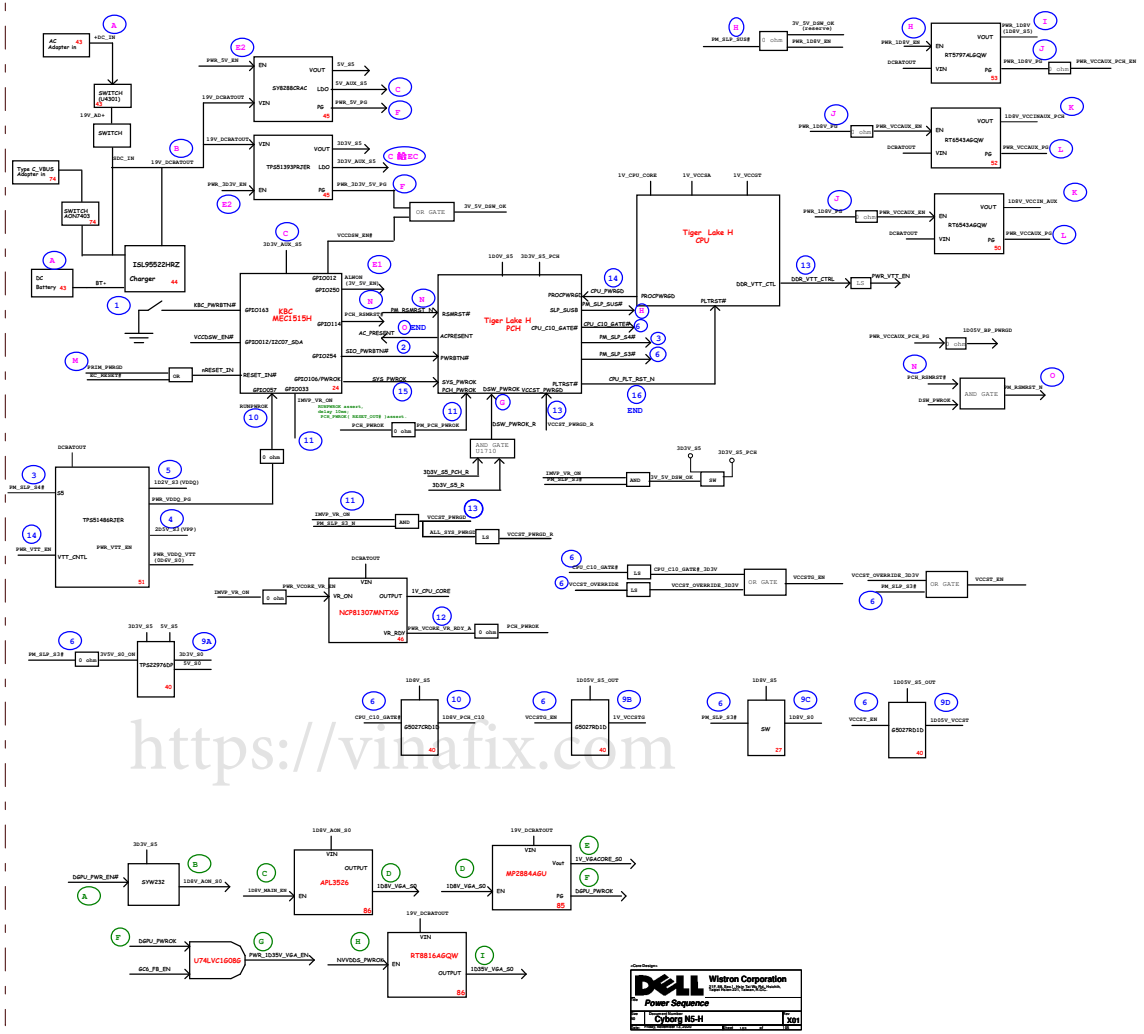
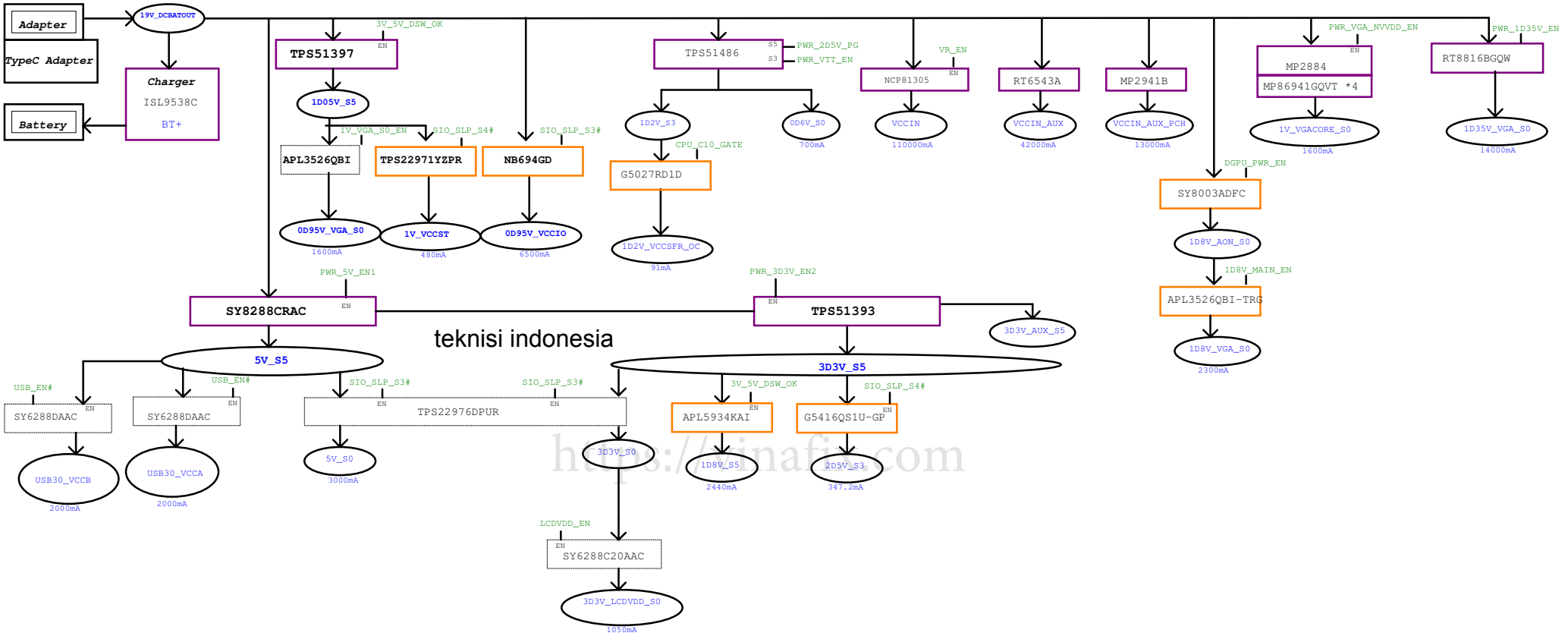
Intel-Power Up Sequence









Power Shape

Regulator | LDO | Switch

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Title: Power Block Diagram

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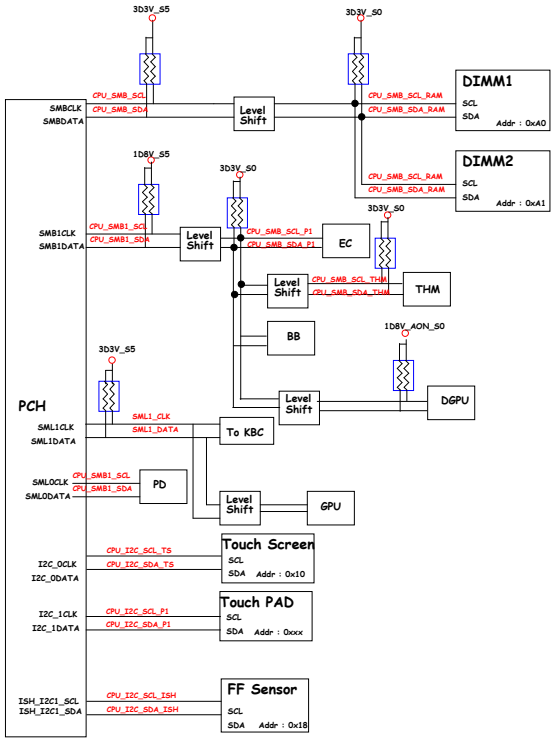
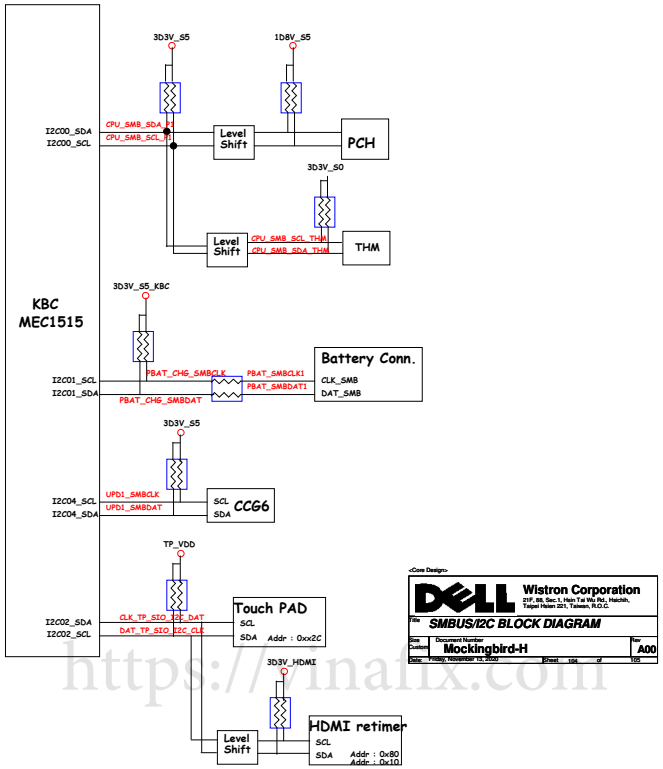
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS/I2C BLOCK DIAGRAM

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Custom	Mockingbird-H	A00

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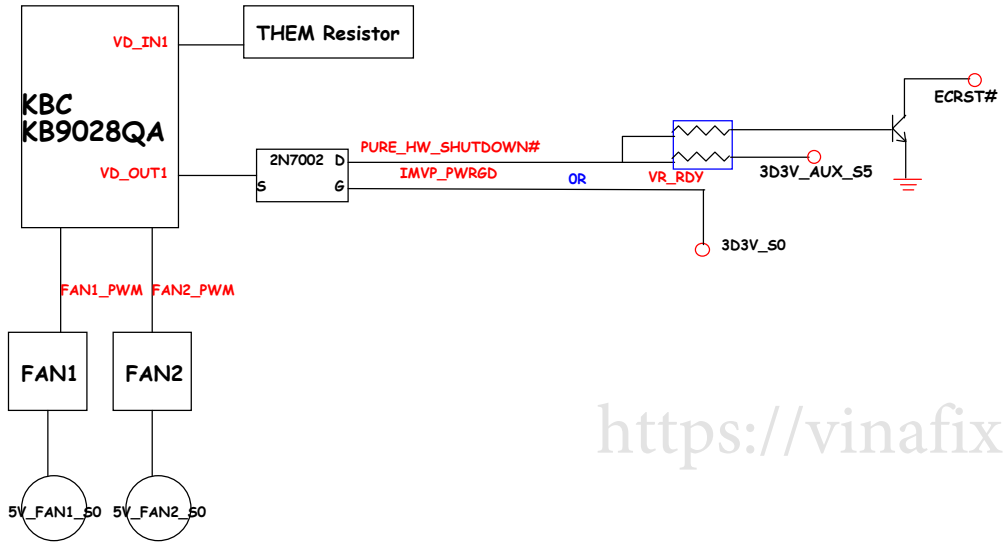
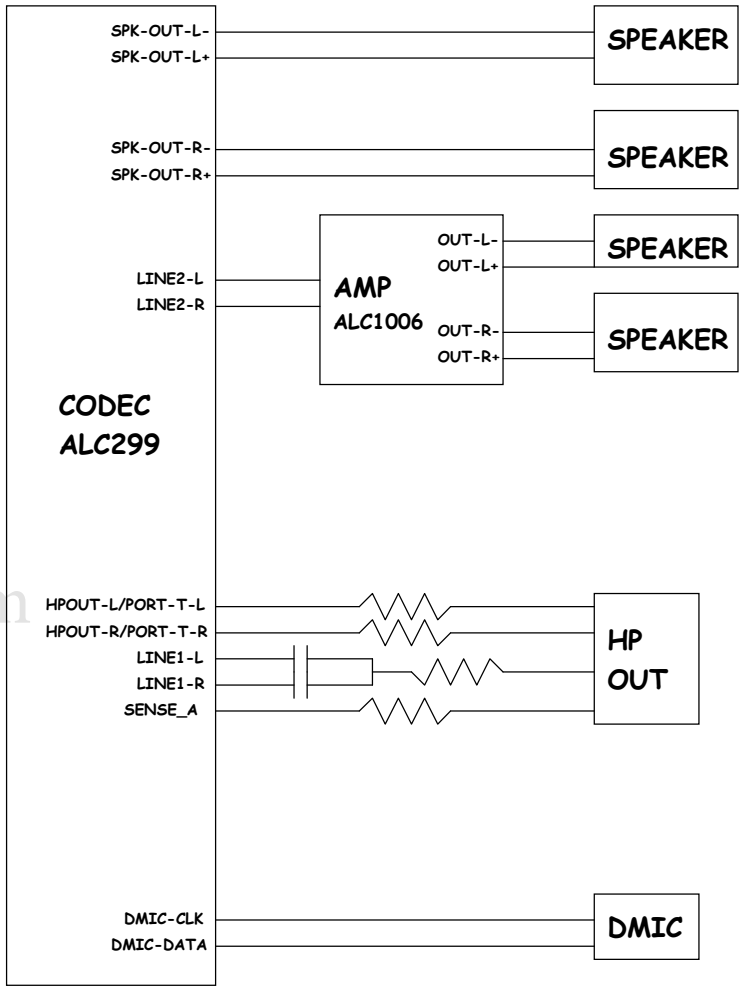
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

Size	Document Number	Rev
Custom	Cyborg N5-H	X00

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Title <Title>		
Size A	Document Number Cyborg N5-H	Rev X00
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