Lennon2-L&Lennon-S-R

ENE micom

CPU : INTEL CEDARVIEW-M
Chip Set : INTEL TIGERPOINT-M
Remarks : DC, DDR3

Model Name : CEDAR TRAIL-M
PCB Part No : BA41-01747A(GCE)
BA41-01748A(HANNSTAR)

Dev. Step : PR
Revision : 1.1
T.R. Date : 2011.01.11

DRAW	CHECK	APPROVAL
Tang cuili	Sun xiao	BC LEE

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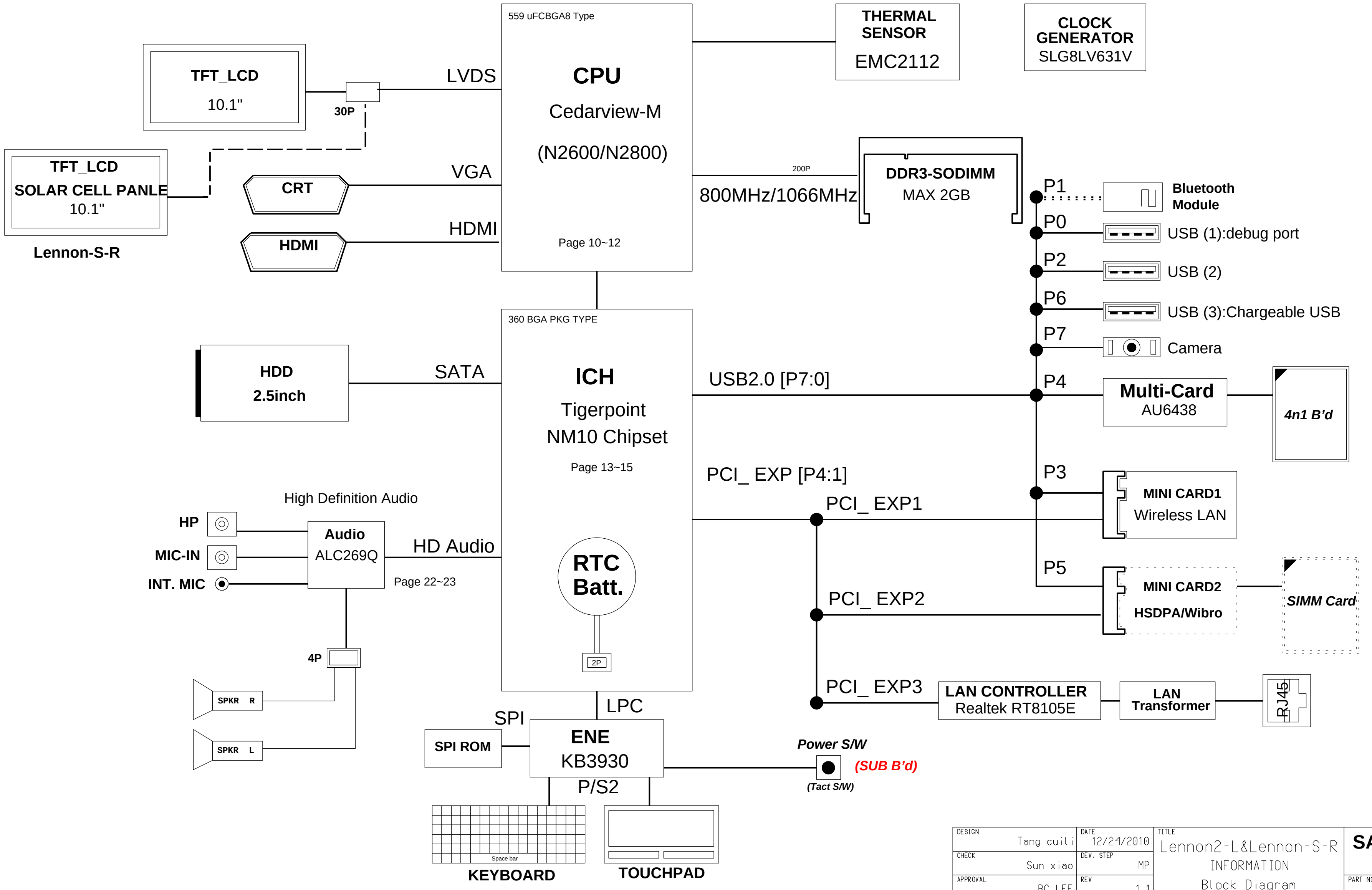
OPERATION BLOCK DIAGRAM



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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Power Sequence Timing

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
USB	AD29(internal)	Programable	
Hub to PCI	AD30(internal)		
LPC Bridge/IDE/AC97/SMBUS	AD31(internal)		
Internal MAC	AD24(internal)		

I²C / SMB Address

Devices	Address	Hex	Bus
TigerPoint	Master		SMBUS Master
CK-505M (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable
SODIMM0	1010 000X	A0h	-
CPU Thermal Sensor	0111 101X	7Ah	Thermal Sensor

USB PORT Assign

Port Number		ASSIGNED TO	Port Number		ASSIGNED TO
UHCI_0	0	USB Port(Debug port)	UHCI_2	4	CardBus Cont.
	1	Touchscreen Pannel		5	Bluetooth Module
UHCI_1	2	USB Port	UHCI_3	6	USB Port(Chargeable)
	3	Mini Card (For WLAN/WWAN)		7	CAMERA

PCI Express Assign

Port Number	ASSIGNED TO
1	Mini Card 1(Wireless LAN)
2	NA
3	LOM

Voltage Rails

Power Rail	Descriptions
PRTC_BAT	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well.
VDC	Primary DC system power supply (9 to 19V)
P1.05V(VCCP)	VTT for CPU, Calistoga & ICH7-M
P3.3V_MICOM	3.3V always power rail(for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
CPU_CORE	Core voltage for Atom CPU

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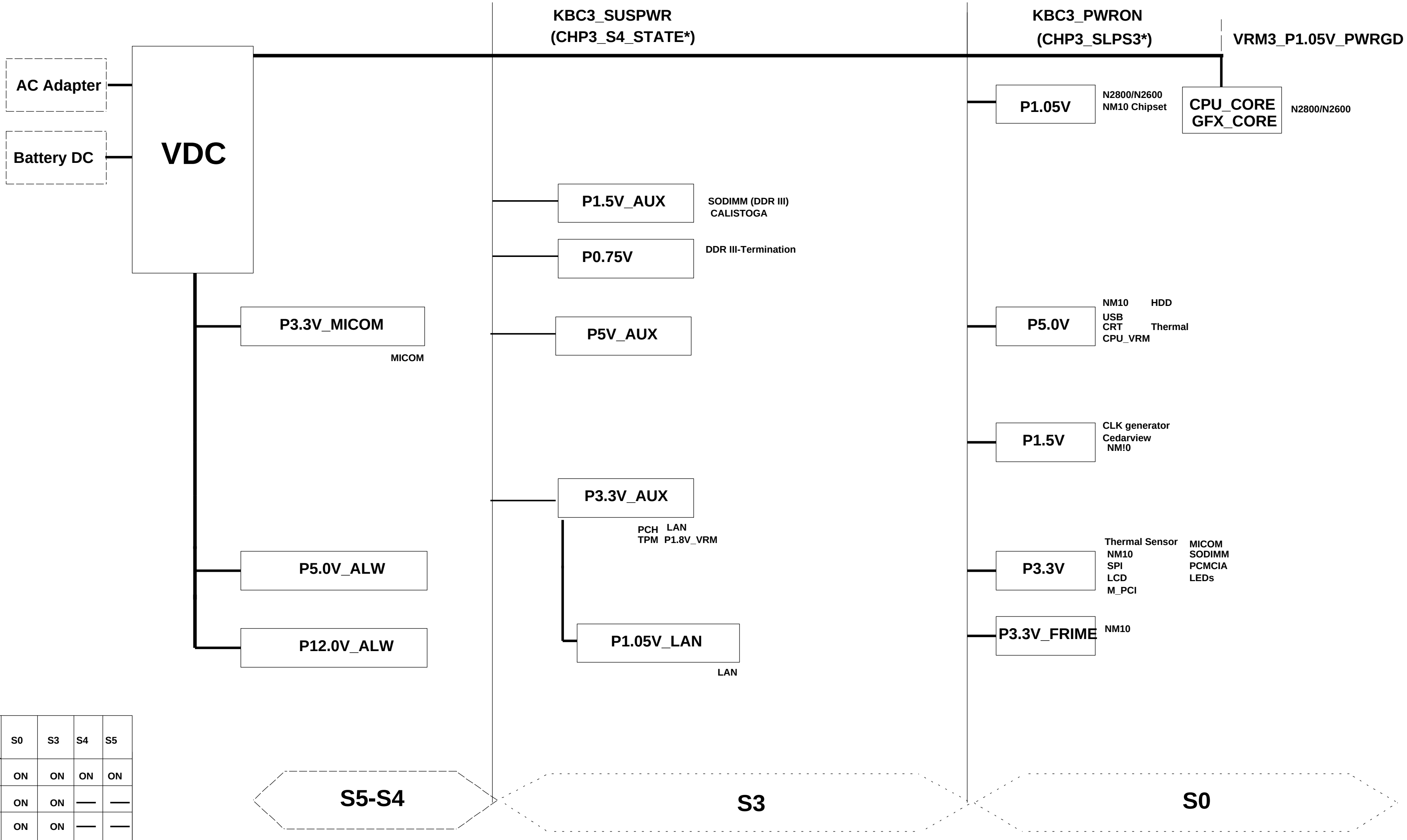
POWER DIAGRAM

Rev 0.1



Rail / State	S0	S3	S4	S5
+V*A(LWS)	ON	ON	ON	ON
+V*LAN	ON	ON	—	—
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

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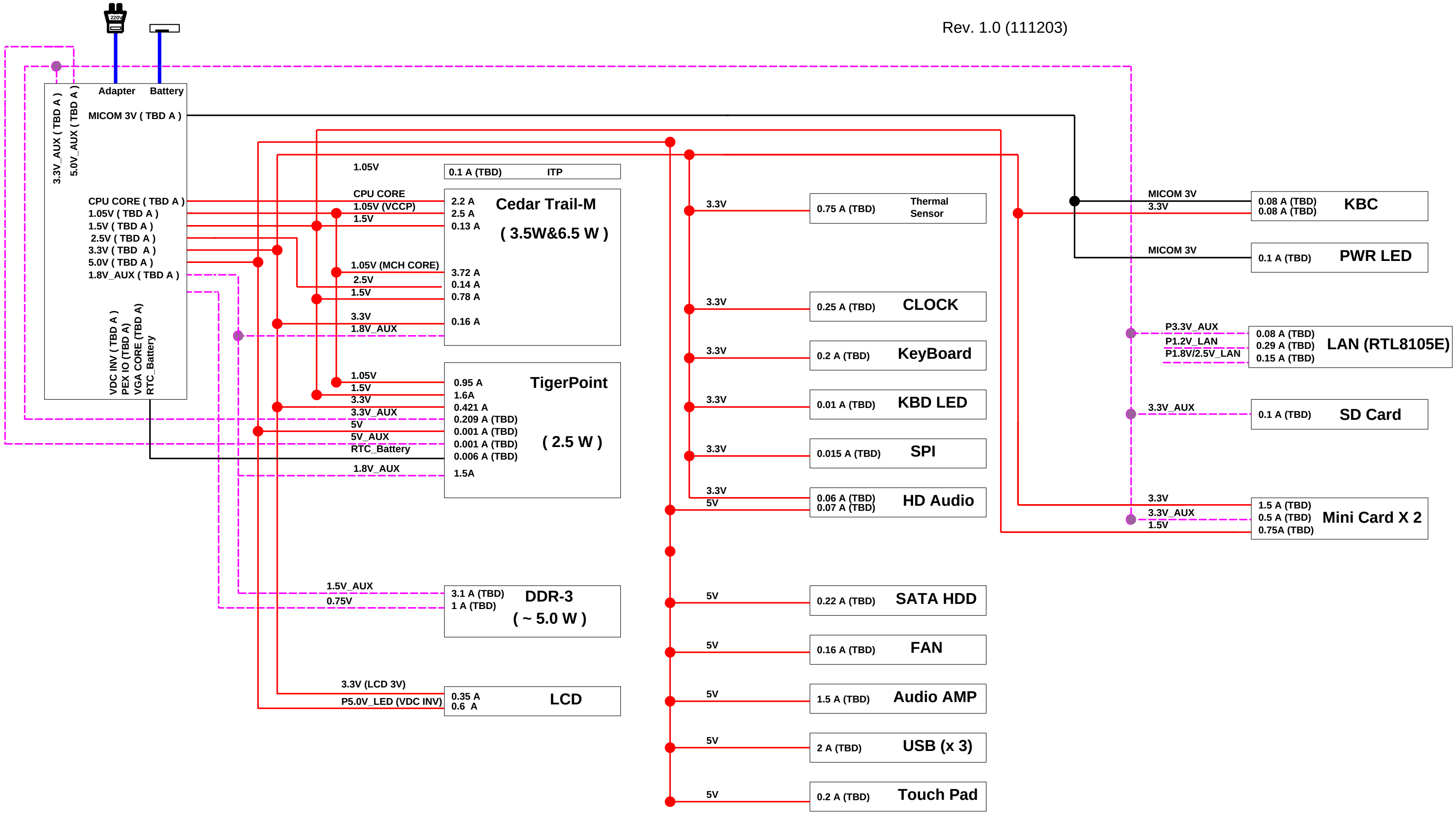
POWER RAILS ANALYSIS

Rev. 1.0 (111203)



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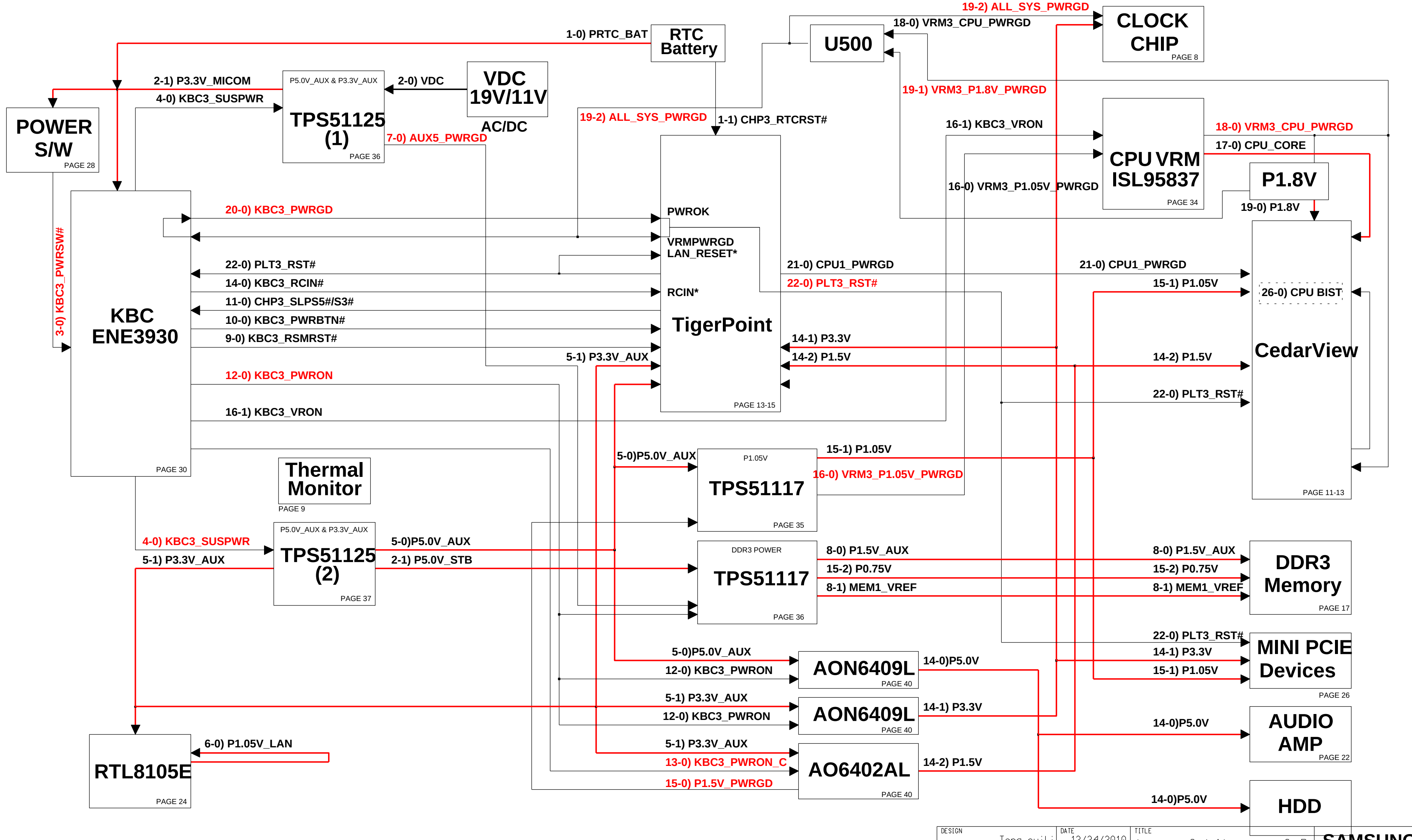
POWER SEQUENCE BLOCK DIAGRAM



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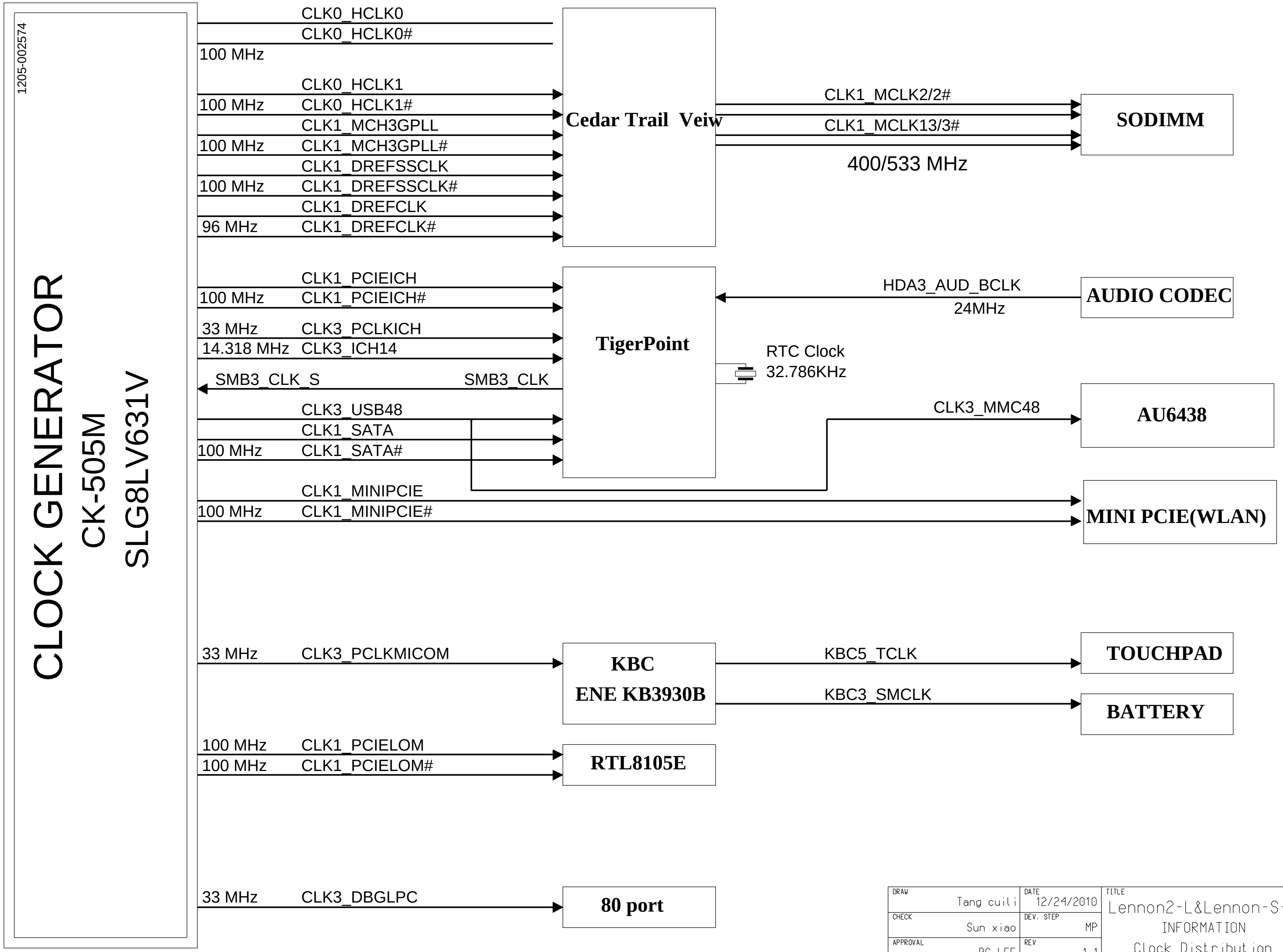
CLOCK DISTRIBUTION



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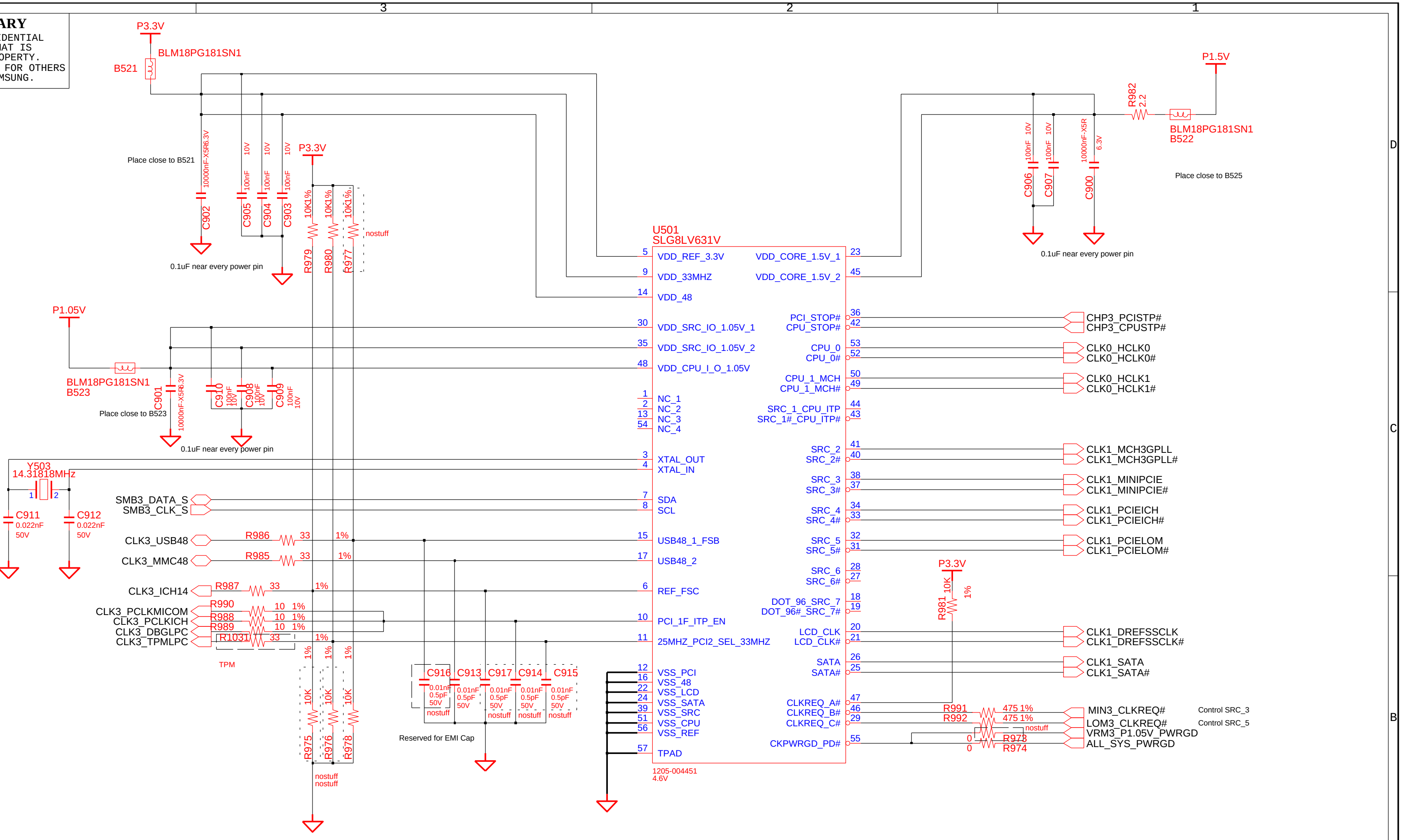

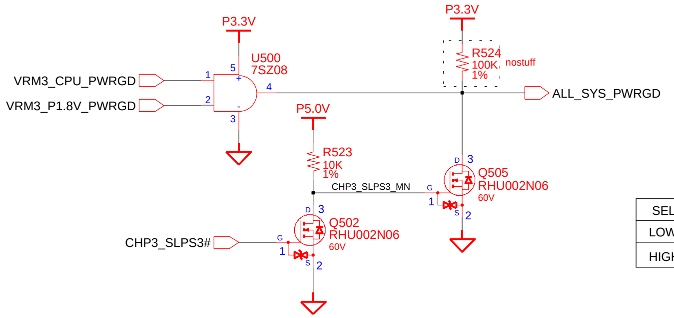

SEL_33MHz(to select Pin11)	
LOW	Pin11 as 25MHz
HIGH	Pin11 as 33MHz

FS_C	FS_B	HOST CLK
0	0	133 MHz
0	1	166 MHz
1	1	200 MHz
1	0	100 MHz

DRAW Tang cuili	DATE 01/08/2009	TITLE Lennon2-L&Lennon-S-R Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
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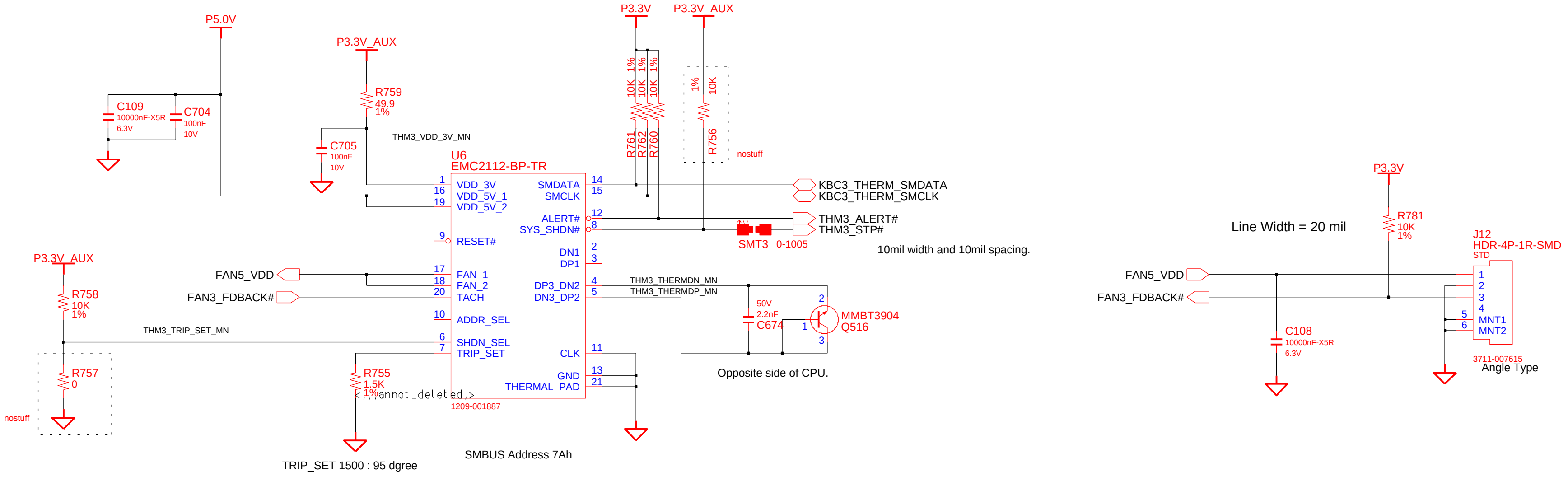
THERMAL SENSOR & FAN CONTROL



Line Width = 20 mil

10mil width and 10mil spacing.

Opposite side of CPU.

SMBUS Address 7Ah

TRIP_SET 1500 : 95 dgree

Place thermal chip under CPU

DESIGN Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R Thermal Sensor EMC2112 THERMAL SENSOR	SAMSUNG ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
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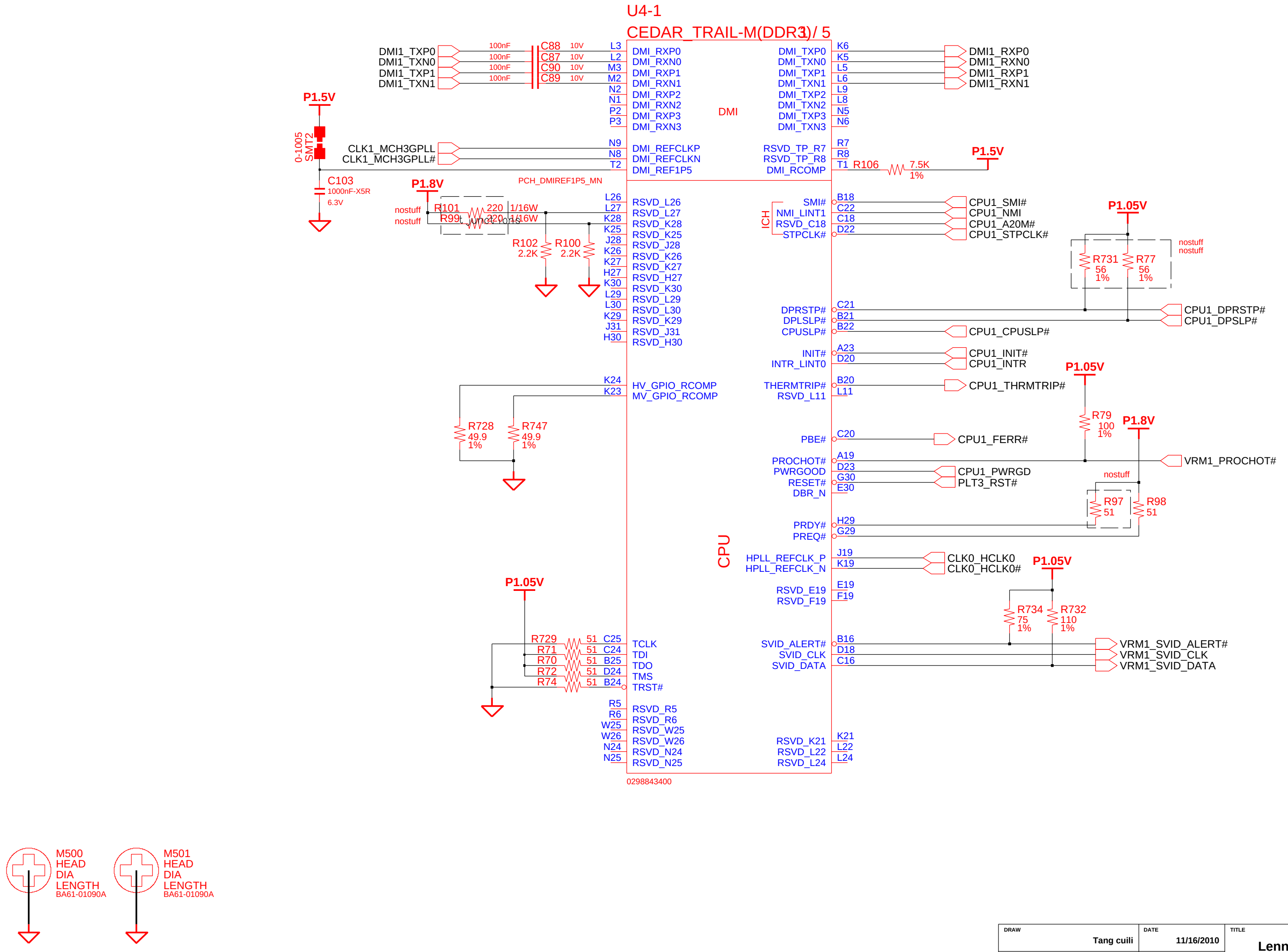
CEDAR TRAIL PROCESSOR (1/3)



DRAW	DATE	TITLE	
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CHECK Sun xiao	DEV. STEP MP	CPU	
APPROVAL BC LEE	REV 1.1	Lincroft (2/5)	PART NO. BA41-0XXXXA
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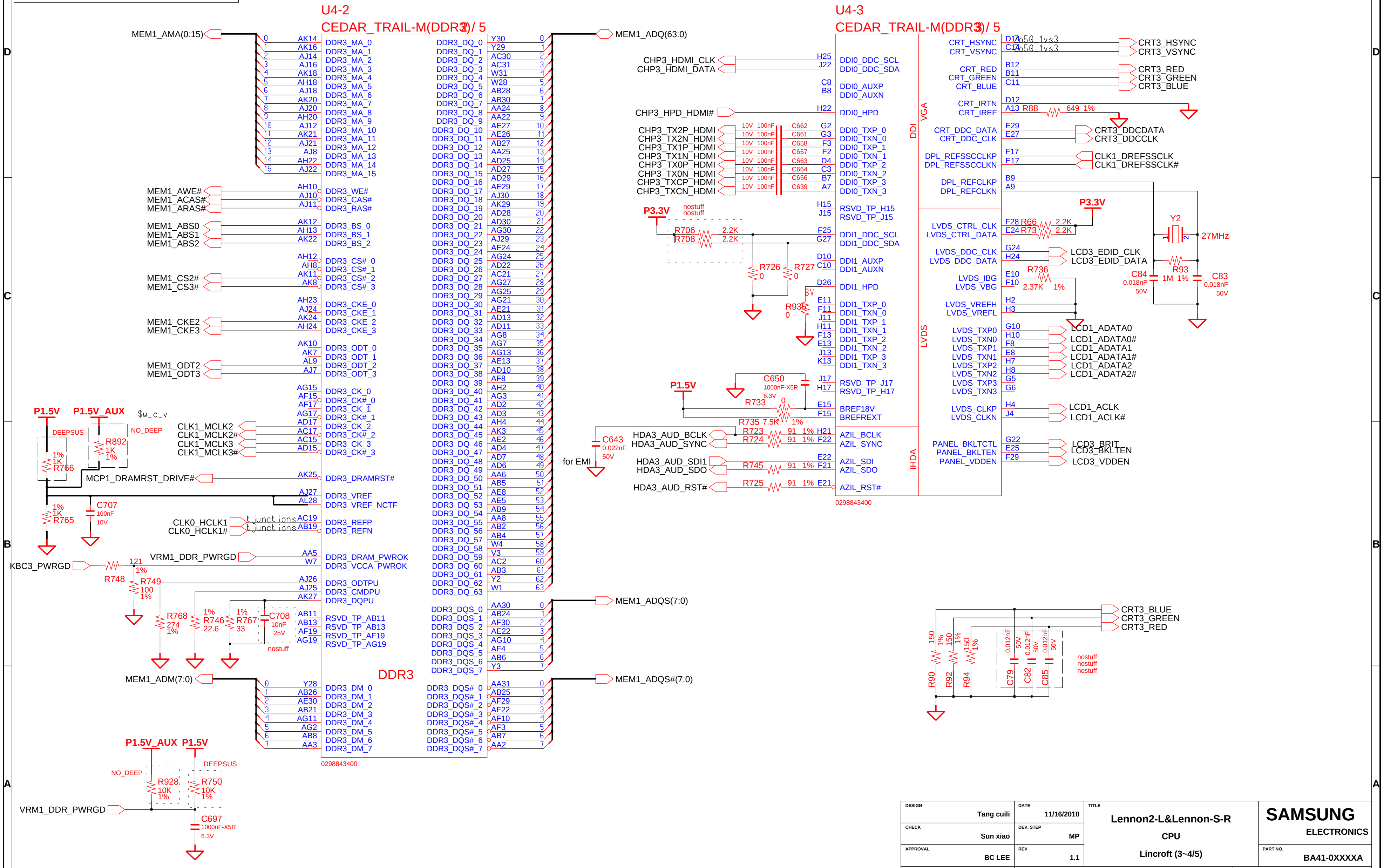
CEDAR TRAIL PROCESSOR (2/5)



DESIGN Tang cuili	DATE 11/16/2010	TITLE Lennon2-L&Lennon-S-R CPU Lincroft (3~4/5)	SAMSUNG ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
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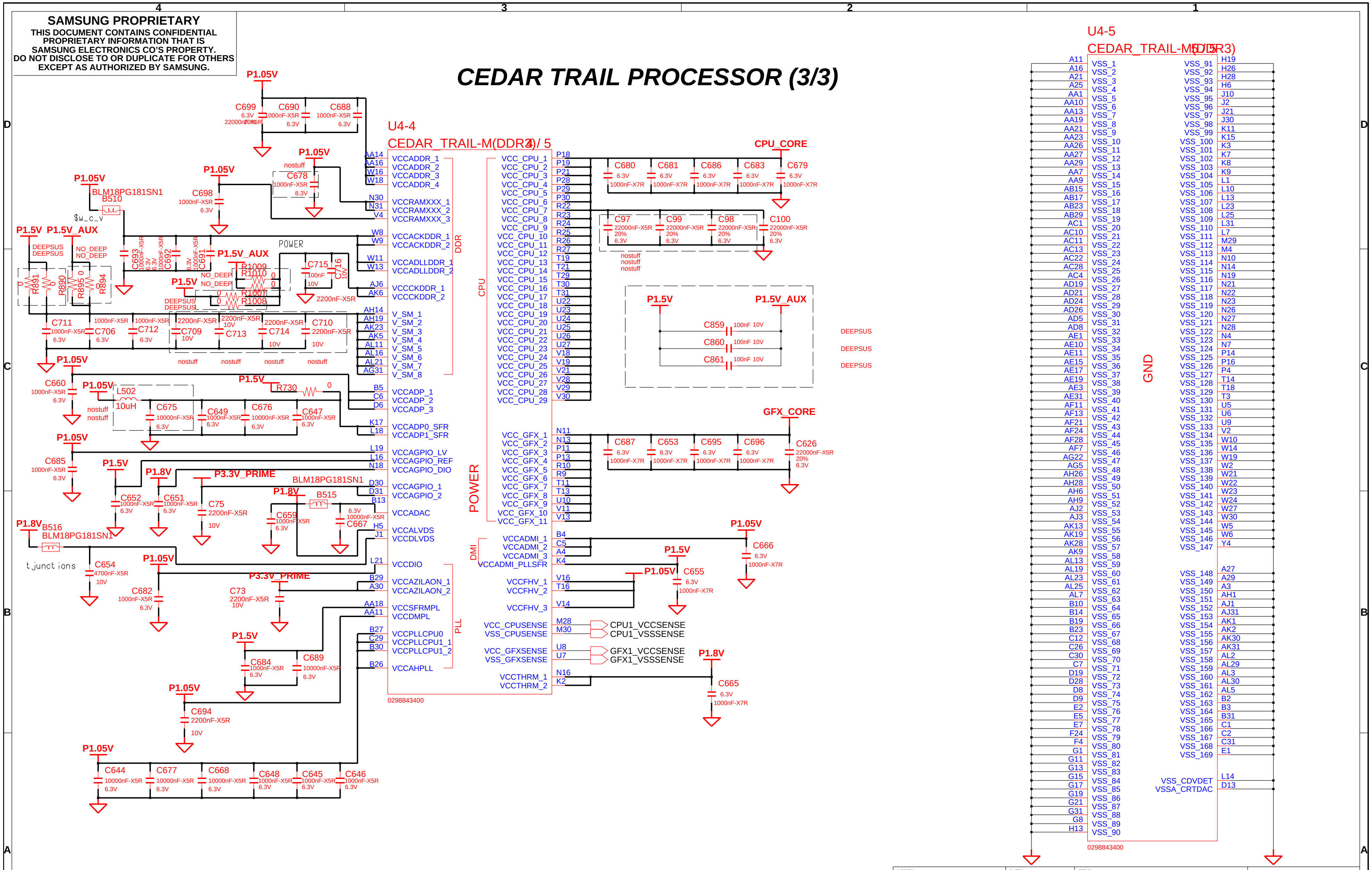
CEDAR TRAIL PROCESSOR (3/3)



DESIGN	DATE	TITLE	
Tang cuili	11/16/2010	Lennon2-L&Lennon-S-R	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP	CPU	
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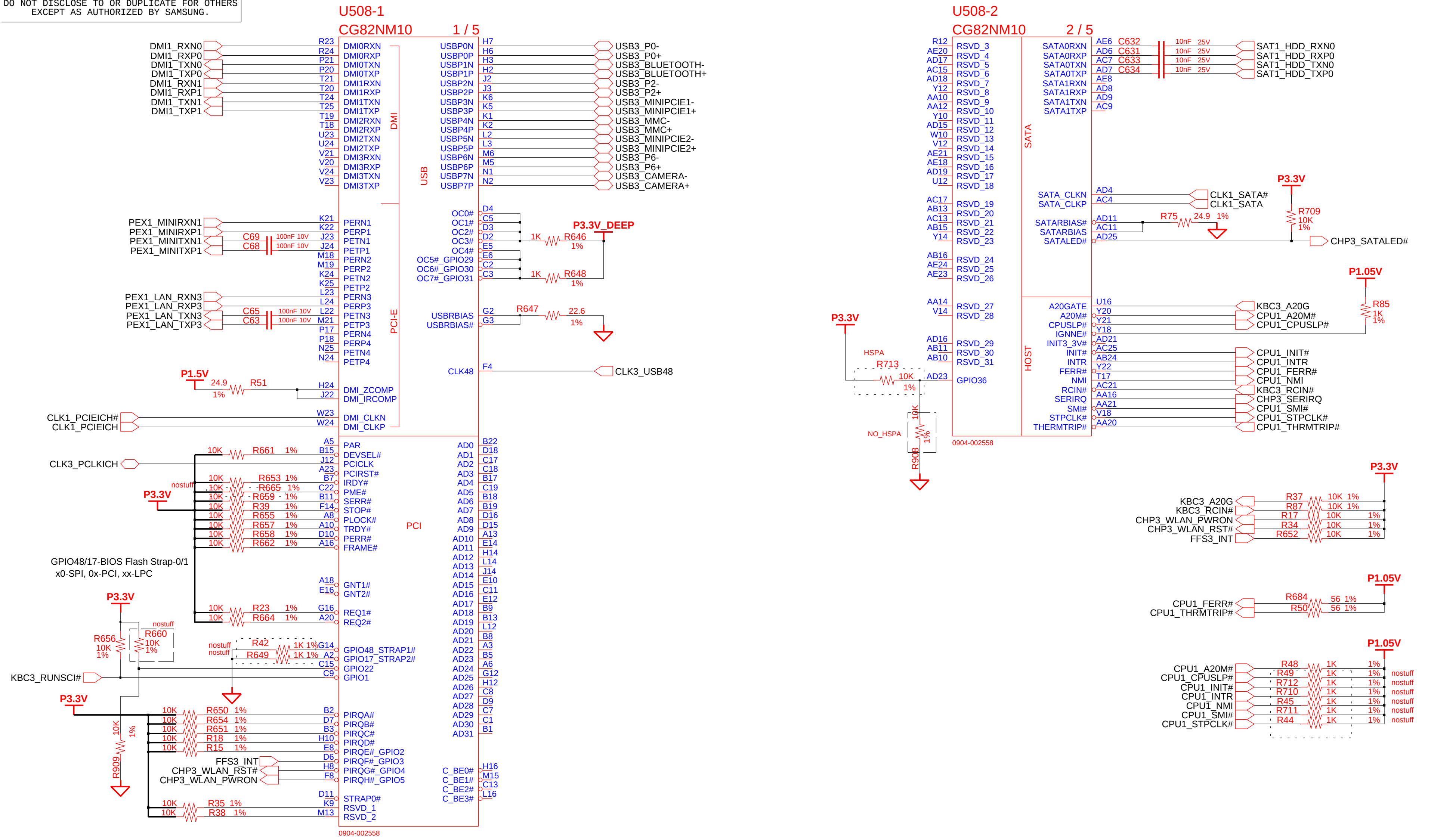
Tigerpoint (1/3)



DRAW	DATE	TITLE	
Tang cuili	12/24/2010	Lennon2-L&Lennon-S-R CHIPSET TIGERPOINT(1/3)	**SAMSUNG** ELECTRONICS
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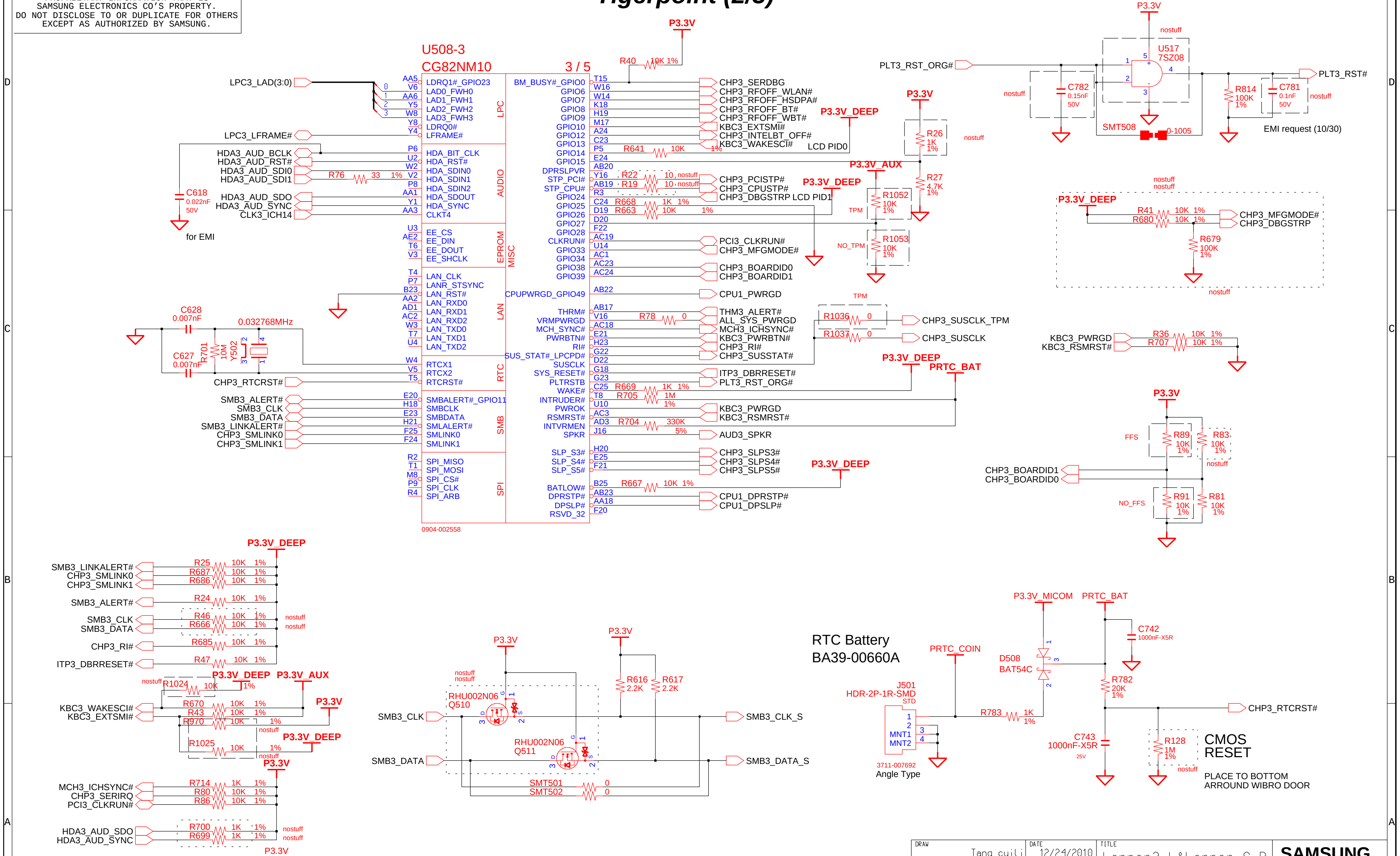
Tigerpoint (2/3)



DRAW	DATE	TITLE	**SAMSUNG** ELECTRONICS
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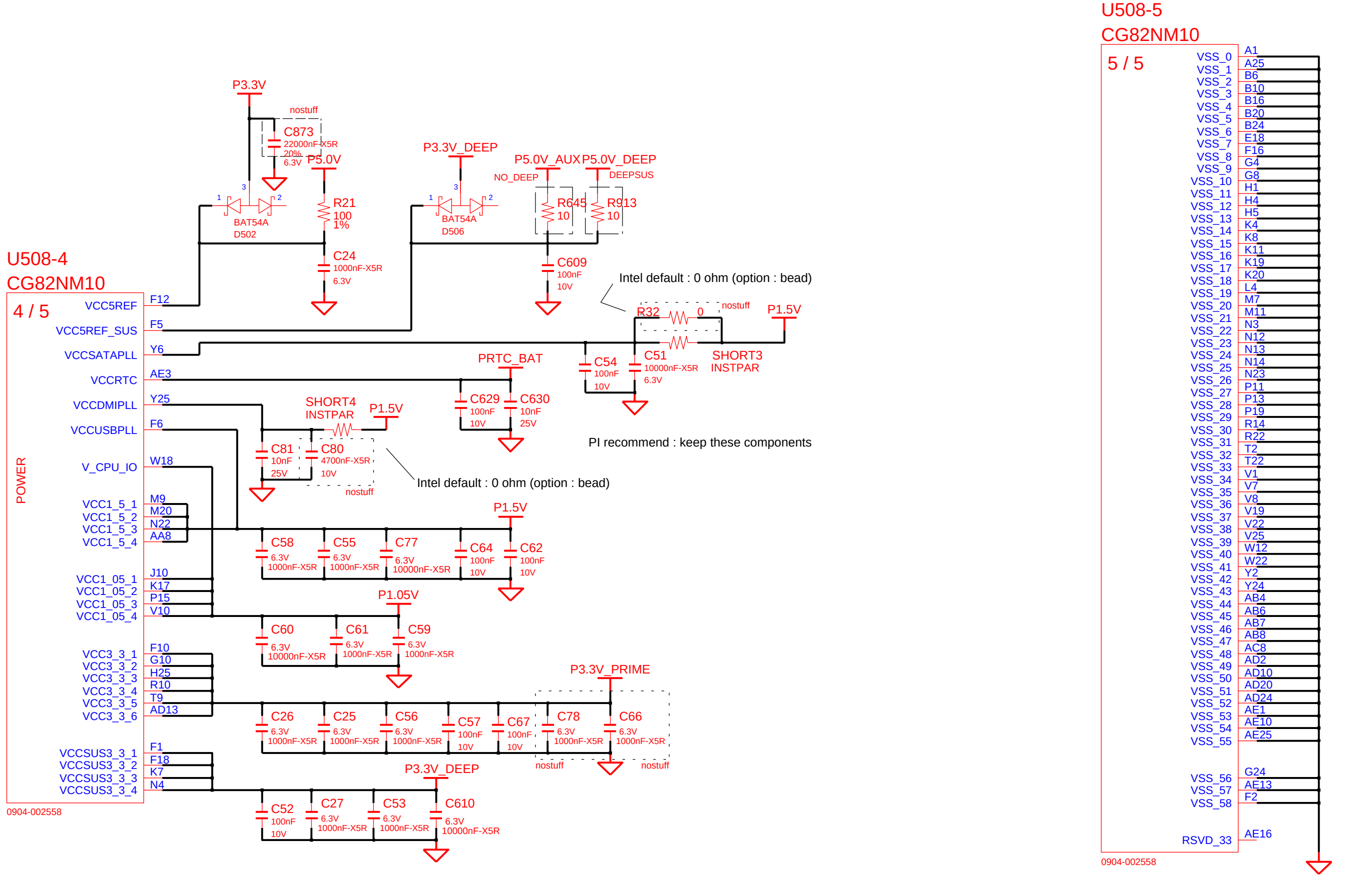
Tigerpoint (3/3)



DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R CHIPSET TIGERPOINT(3/3)	**SAMSUNG** ELECTRONICS
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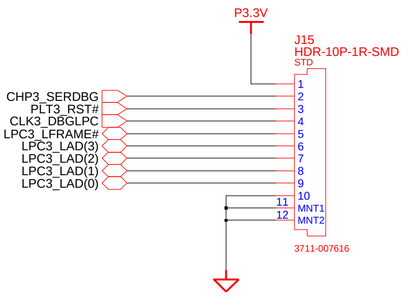
80H DECODER CONNECTOR AND DEBUG CODE

AMI Aptio 4.x Status Codes

80H DECODER CONNECTOR



PEI Status Codes

Progress Codes

10	PEI Core is started
11	Pre-memory CPU initialization is started
12	Pre-memory CPU initialization(CPU module specific)
13	Pre-memory CPU initialization(CPU module specific)
14	Pre-memory CPU initialization(CPU module specific)
15	Pre-memory North Bridge initialization is started)
16	Pre-memeory North Bridge initialization(North Bridge module specific)
17	Pre-memeory North Bridge initialization(North Bridge module specific)
18	Pre-memeory North Bridge initialization(North Bridge module specific)
19	Pre-memory South Bridge initialization is started
1A	Pre-memory South Bridge initialization (South Bridge module specific)
1B	Pre-memory South Bridge initialization (South Bridge module specific)
1C	Pre-memory South Bridge initialization (South Bridge module specific)
1D-2A	OEM pre -memory initialization codes
2B	Memoriy initialization.Serial Presence Detect (SPD) data reading
2C	Memoriy initialization.Memoryl presence Detection
2D	Memoriy initialization. Programming memory timing information
2E	Memoriy initialization. Configuring memory
2F	Memoriy initialization.(other)
30	Reserved for ASL (see ASL Statue Codes section below)
31	Memory Installed
32	CPU post-memory initialization is started
33	CPU post-memory initialization. Cache initialization
34	CPU post-memory initialization. Application Processor(s) (AP) intialization
35	CPU post-memory initialization. Boot Strap Processor(BSP) selection
36	CPU post-memory initialization.Syetem Management Mode (SMM) intialization
37	Post-Memory North Bridge initialization is started
38	Post-Memory North Bridge initialization (North Bridge module specific)
39	Post-Memory North Bridge initialization (North Bridge module specific)
3A	Post-Memory North Bridge initialization (North Bridge module specific)
3B	Post-Memory South Bridge initialization is started
3C	Post-Memory South Bridge initialization (South Bridge module specific)
3D	Post-Memory South Bridge initialization (South Bridge module specific)
3E	Post-Memory South Bridge initialization (South Bridge module specific)
3F-4E	OEM post memory initialization codes
4F	DXE IPL is started

PEI Error Codes

50	Memory initialization error.Invalid memory type or incompatible memory speed.
51	Memory initialization error.SPD reading has failed
52	Memory initialization error.Invalid memory size or memory modules do not match
53	Memory initialization error.No useable memory detected
54	Unspecified memory initialization error
55	Memory not installed
56	Invalid CPU type or Speed
57	CPU mismatch
58	CPU self test failed or possible CPU cache error
59	CPU micro-code is not found or micro-code update is failed
5A	Internal CPU error
5B	reset PPI is not available
5C-5F	Reserved for future AMI error codes

S3 Resume Progress Codes

E8	S3 Resume Failed in PEI
E9	S3 Resume PPI not Found
EA	S3 Resume Boot Script Error
EB	S3 OS Wake Error
EC-EF	Reserved for future AMI error codes

Recovery Progress Codes

F0	Recovery condition triggered by firmware(Auto recovery)
F1	Recovery condition triggered by user(Forced recovery)
F2	Recovery process started
F3	Recovery firmware image is found
F4	Recovery firmware image is loaded
F5-F7	Reserved for future AMI progress codes

Recovery Error Codes

F8	Recovery PPI is not available
F9	Recovery capsule is not found
FA	Invalid recovery capsule
FB-FF	Reserved for future AMI error codes
5A	Internal CPU error
5B	reset PPI is not available
5C-5F	Reserved for future AMI error codes

ACPI/ASL Status Codes

01	System is entering S1 sleep state
02	System is entering S2 sleep state
03	System is entering S3 sleep state
04	System is entering S4 sleep state
05	System is entering S5 sleep state
10	System is waking up from the S1 sleep state
20	System is waking up from the S1 sleep state
30	System is waking up from the S1 sleep state
40	System is waking up from the S1 sleep state
AC	System has transitioned into ACPI mode(PIC)
AA	System has transitioned into ACPI mode(ACPI)

DXE Status Codes

Progress Codes

60	DXE Core is started
61	NVRAM initialization
62	Installation fo the South Bridge Runtime Services
63	CPU DXE initialization is started
64	CPU DXE initialization(CPU moudle specific)
65	CPU DXE initialization(CPU moudle specific)
66	CPU DXE initialization(CPU moudle specific)
67	CPU DXE initialization(CPU moudle specific)
68	PCI host bridge initialization
69	North Bridge DXE initialization is started
6A	North Bridge DXE SMM initialization is started
6B	North Bridge DXE initialization(North Bridge module specific)
6C	North Bridge DXE initialization(North Bridge module specific)
6D	North Bridge DXE initialization(North Bridge module specific)
6E	North Bridge DXE initialization(North Bridge module specific)
6F	North Bridge DXE initialization(North Bridge module specific)
70	South Bridge DXE initialization is started
71	South Bridge DXE SMM initialization is started
72	South Bridge devices initialization
73	South Bridge DXE initialization(South Bridge module specific)
74	South Bridge DXE initialization(South Bridge module specific)
75	South Bridge DXE initialization(South Bridge module specific)
76	South Bridge DXE initialization(South Bridge module specific)
77	South Bridge DXE initialization(South Bridge module specific)
78	ACPI module initialization
79	CSM initialization
7A-7F	Reserved for future AMI DEX codes
80-8F	OEM DEX initialization codes
90	Boot Device Selection (BDS) phase is started
91	Driver connecting is started
92	PCI Bus initialization is started
93	PCI Bus Hot Plug Controller Initialization
94	PCI Bus Enumeration
95	PCI Bus Request Resources
96	PCI Bus Assign Resources
97	Console Output devices connect
98	Console Input devices connect
99	Super IO Initialization
9A	USB initialization is started
9B	USB Reset
9C	USB Detect
9D	USB Enable
9E-9F	Reserved for future AMI codes
A0	IDE initialization is started
A1	IDE Reset
A2	IDE Detect
A3	IDE Enable
A4	SCSI Initialization is started
A5	SCSI Reset
A6	SCSI Detect
A7	SCSI Enable
A8	Setup Verifing Password
A9	Start of Setup
AA	Reserved for ASL (see ASL Status Codes section below)
AB	Setup Input Wait
AC	Reserved for ASL (see ASL Statue Codes section below)
AD	Readay To Boot event
AE	Legacy Boot Event
AF	Exit Boot Services event
B0	Runtime Set Virtual Address MAP Begin
B1	Runtime Set Virtual MAP End
B2	Legacy Option ROM Initialization
B3	**System Reset**
B4	**USB Hot Plug**
B5	**PCI Bus Hot Plug**
B6	Clean-up of NVRAM
B7	Configuration Reset (reset of NVRAM settings)
B8-BF	Reserved for future AMI codes
C0-CF	OEM BDS initialization codes

DXE Error Codes

D0	CPU initialization error
D1	North Bridge initialization error
D2	South Bridge initialization error
D3	Some of the Architectural Protocols are not available
D4	PCI resource allocation error.Out of Resources
D5	No Space for Legacy Option ROM
D6	No Console Output Devices are found
D7	No Console Input Devices are found
D8	Invalid password
D9	Error loading Boot Option(Loadimage returned error)
DA	Boot Option is failed(Startimage returned error)
DB	Flash update is failed
DC	Reset protocol is not available

DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R SPI_BIOS_ROM SPI_BIOS_ROM	**SAMSUNG** ELECTRONICS
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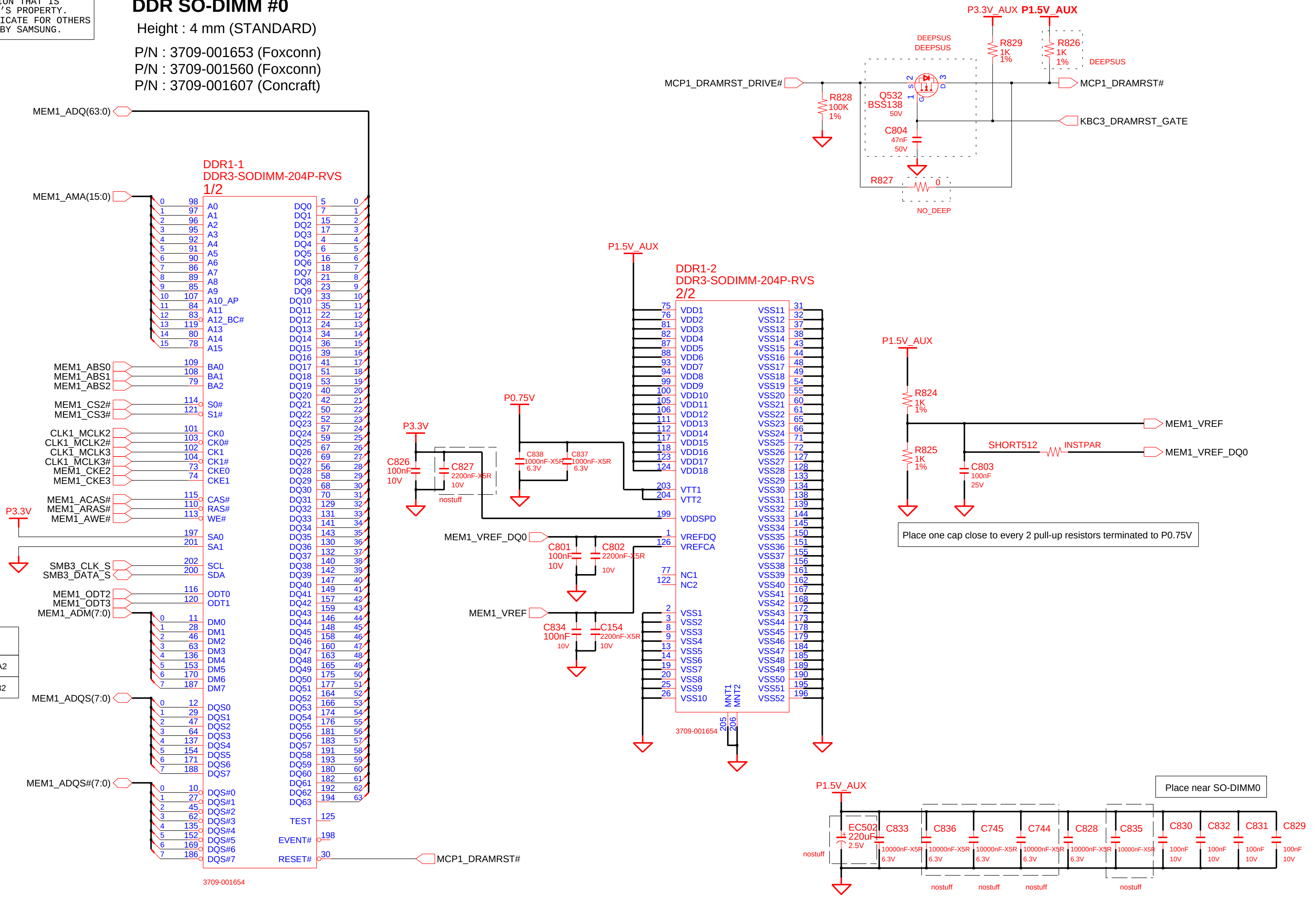
DDR SO-DIMM #0

Height : 4 mm (STANDARD)

P/N : 3709-001653 (Foxconn)
P/N : 3709-001560 (Foxconn)
P/N : 3709-001607 (Concraft)



Place one cap close to every 2 pull-up resistors terminated to P0.75V

Place near SO-DIMM0

SA0 SA1	0 0	0 1
SPD ADD	0xA0	0xA2
TS ADD	0x30	0x32

DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP	SODIMM_DDR3	
APPROVAL BC LEE	REV 1.1	SODIMM_DDR3 #1	PART NO. BA41-0XXXXA
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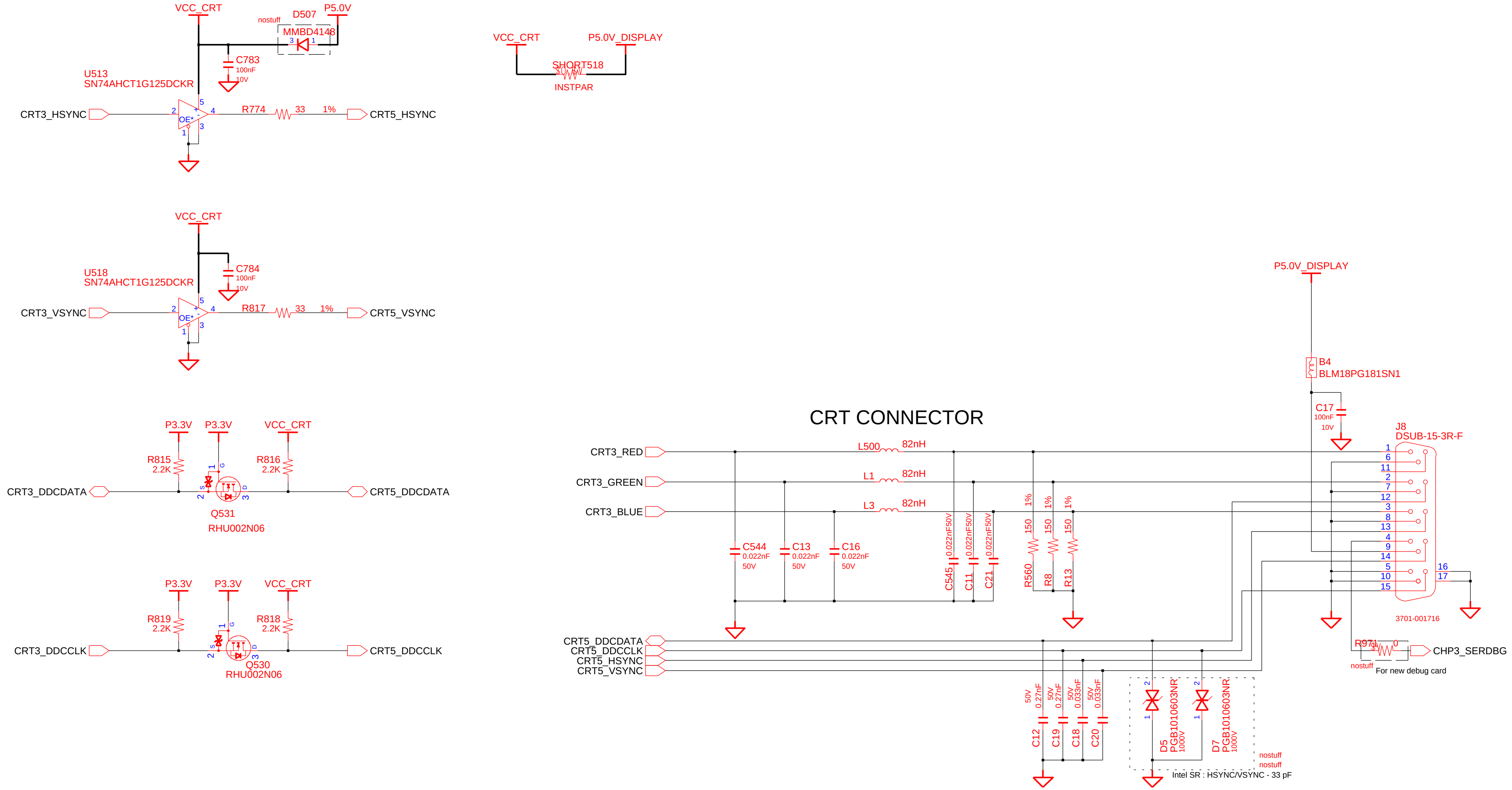
CRT



DESIGN	DATE	TITLE	**SAMSUNG** ELECTRONICS
Tang cuili	12/24/2010	Lennon2-L&Lennon-S-R GRAPHICS_IF CRT	
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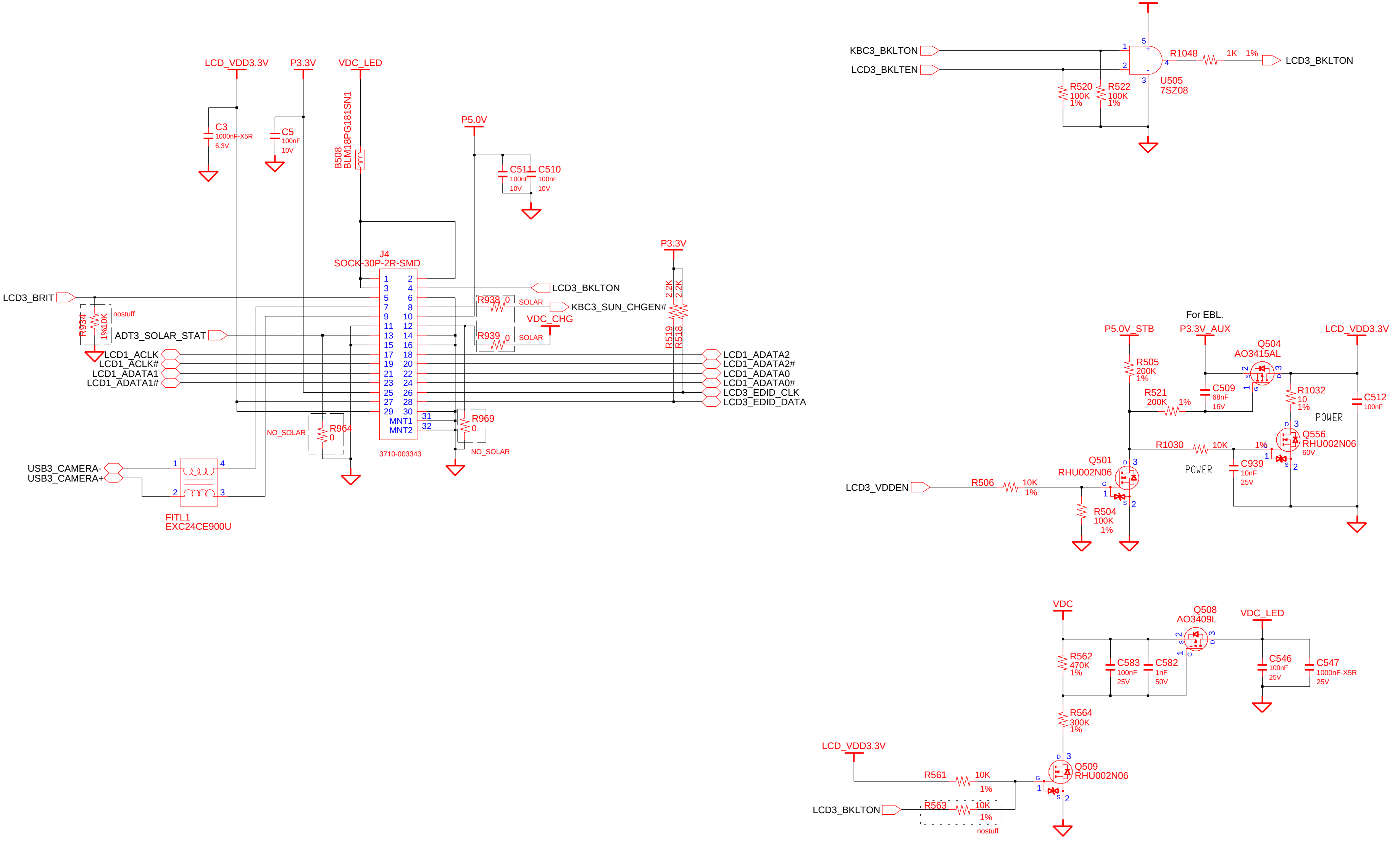

DESIGN Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R GRAPHICS_IF LED LCD I/F	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		PART NO. BA41-0XXXXA
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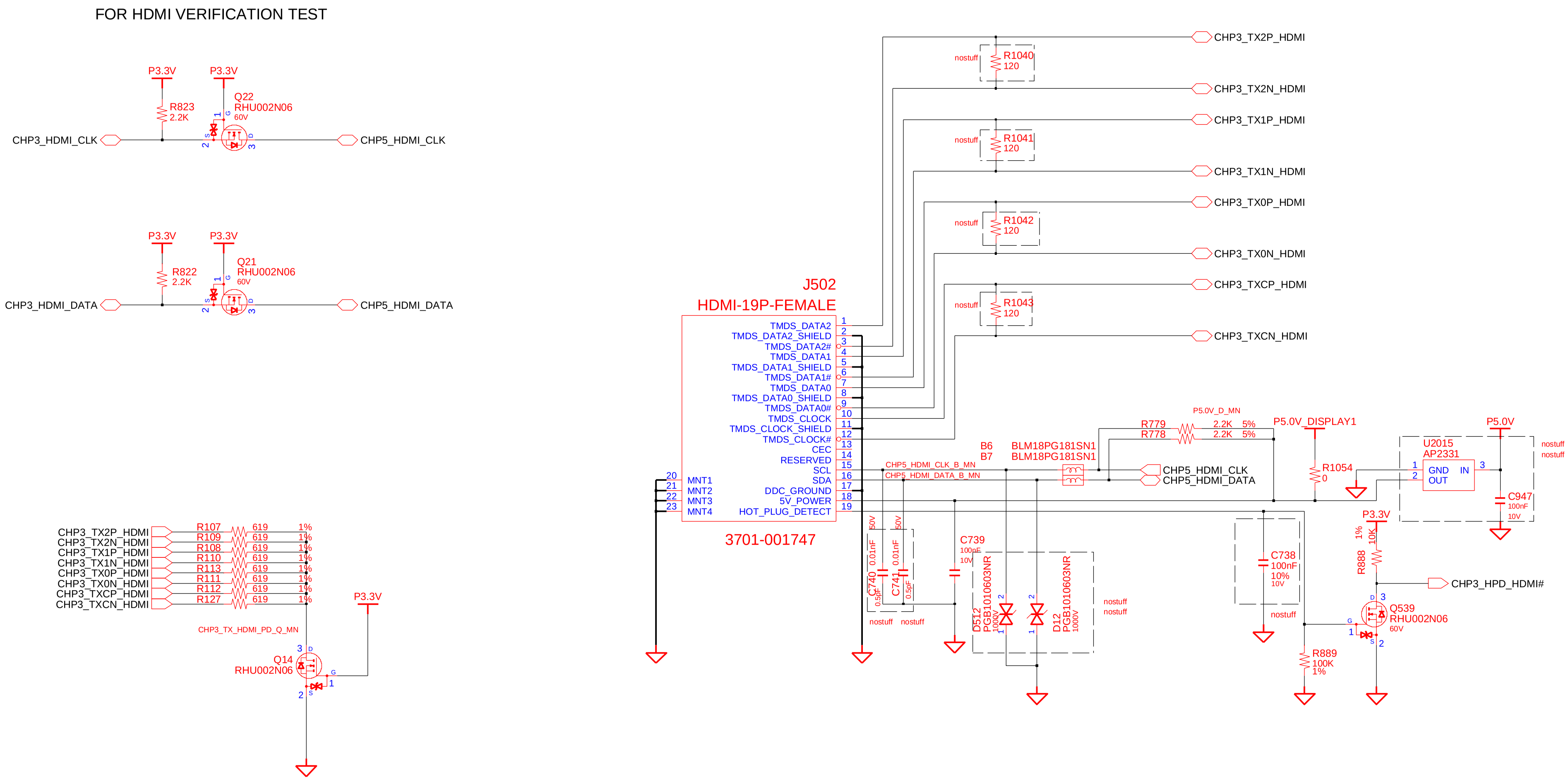
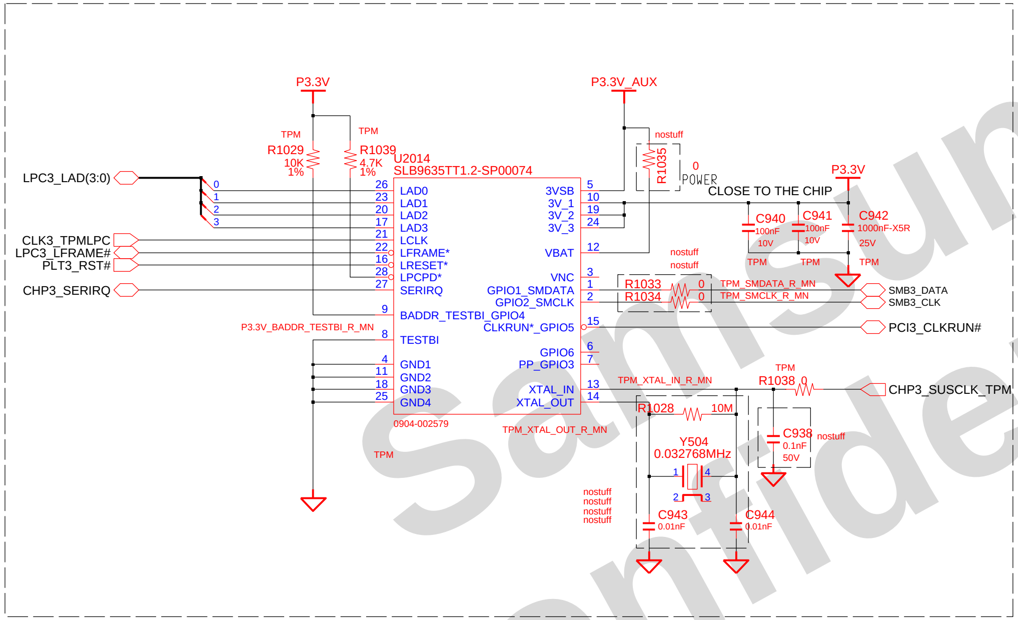
HDMI Graphic



DESIGN	Tang cuili	DATE	9/23/2008	TITLE	Lennon2-L&Lennon-S-R	SAMSUNG ELECTRONICS
CHECK	Sun xiao	DEV. STEP	MP		GRAPHICS_IF	
APPROVAL	BC LEE	REV	1.1		HDMI	PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	January 05, 2012 14:48:10 PM			PAGE 20 OF 43

TPM 1.2(Option.)

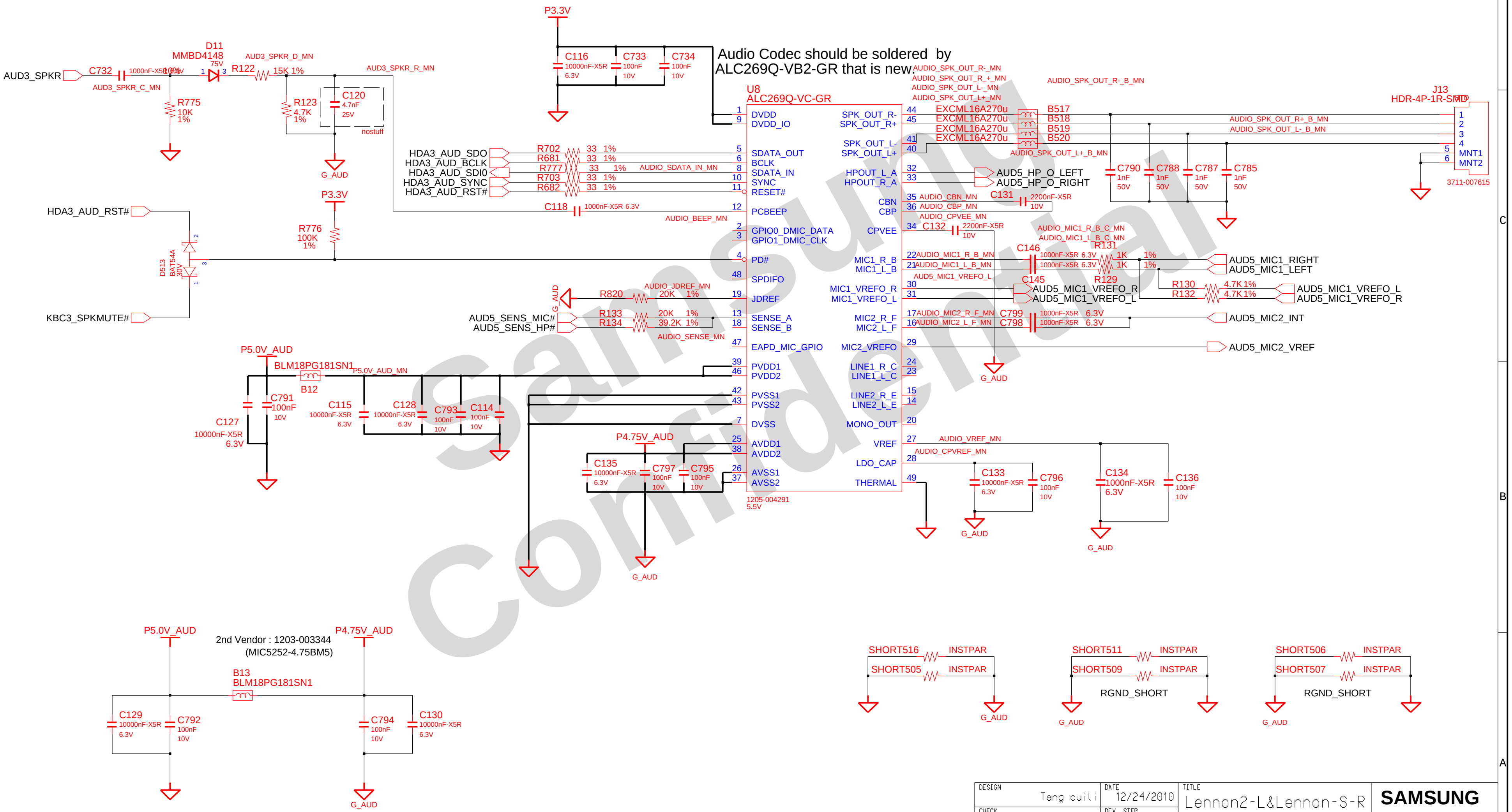


DRAW	DATE	TITLE	SAMSUNG
Tang cuili	10/06/2010	Lennon2-L&Lennon-S-R	ELECTRONICS
CHECK Sun xiao	DEV. STEP MP	TPM	
APPROVAL BC LEE	REV 1.1	TPM	PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT	January 05, 2012 14:48:10 PM	PAGE 21 OF 43

Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

Audio Codec

Audio Codec should be soldered by
ALC269Q-VB2-GR that is new



DESIGN	DATE	TITLE	
Tang cuili	12/24/2010	Lennon2-L&Lennon-S-R AUDIO ALC269Q-VB	**SAMSUNG** ELECTRONICS
CHECK	DEV. STEP		
Sun xiao	MP		
APPROVAL	REV		PART NO.
BC LEE	1.1		BA41-0XXXXA
MODULE CODE	LAST EDIT		
	January 05, 2012 14:48:10 PM		PAGE 22 OF 43

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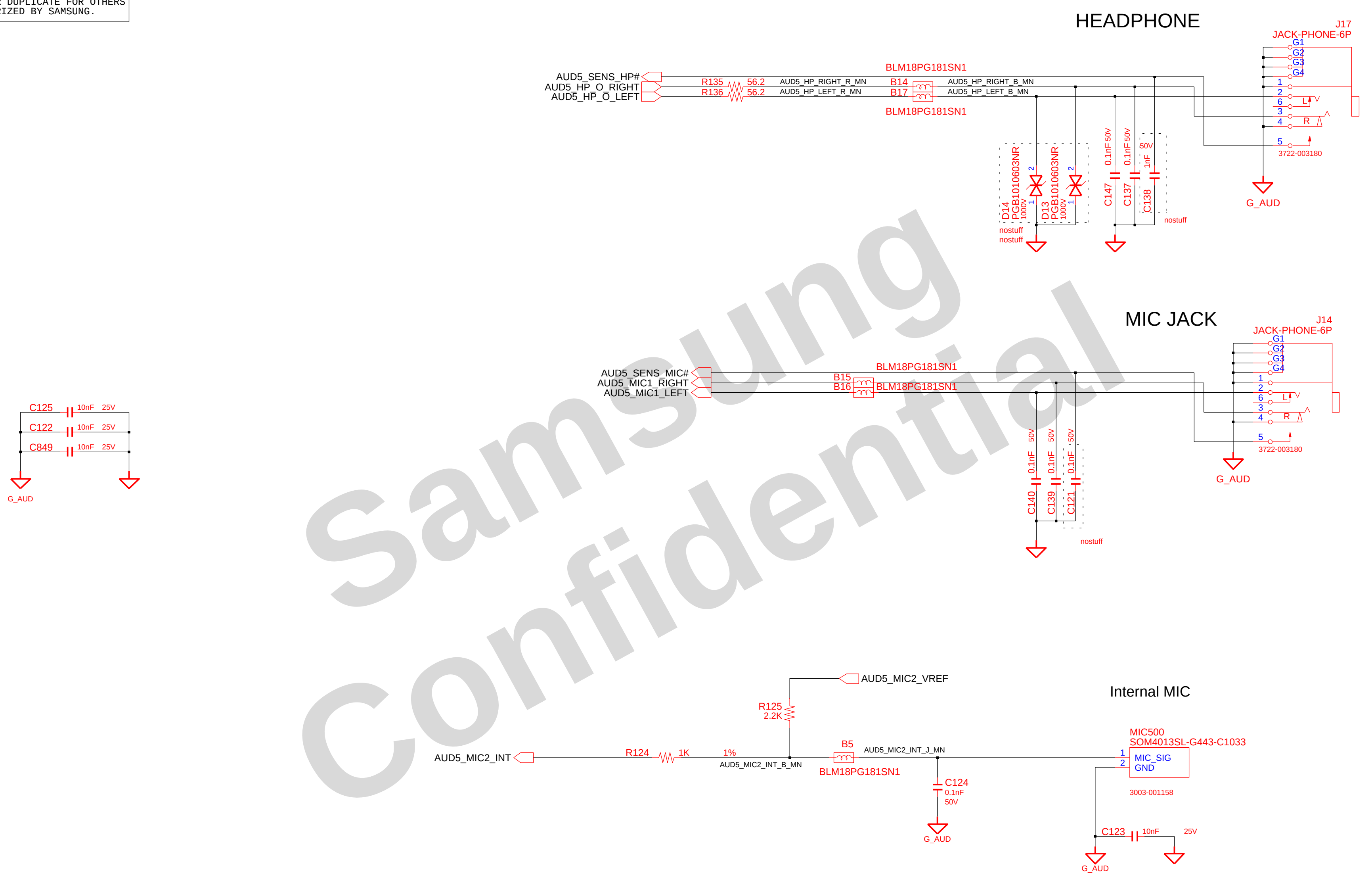
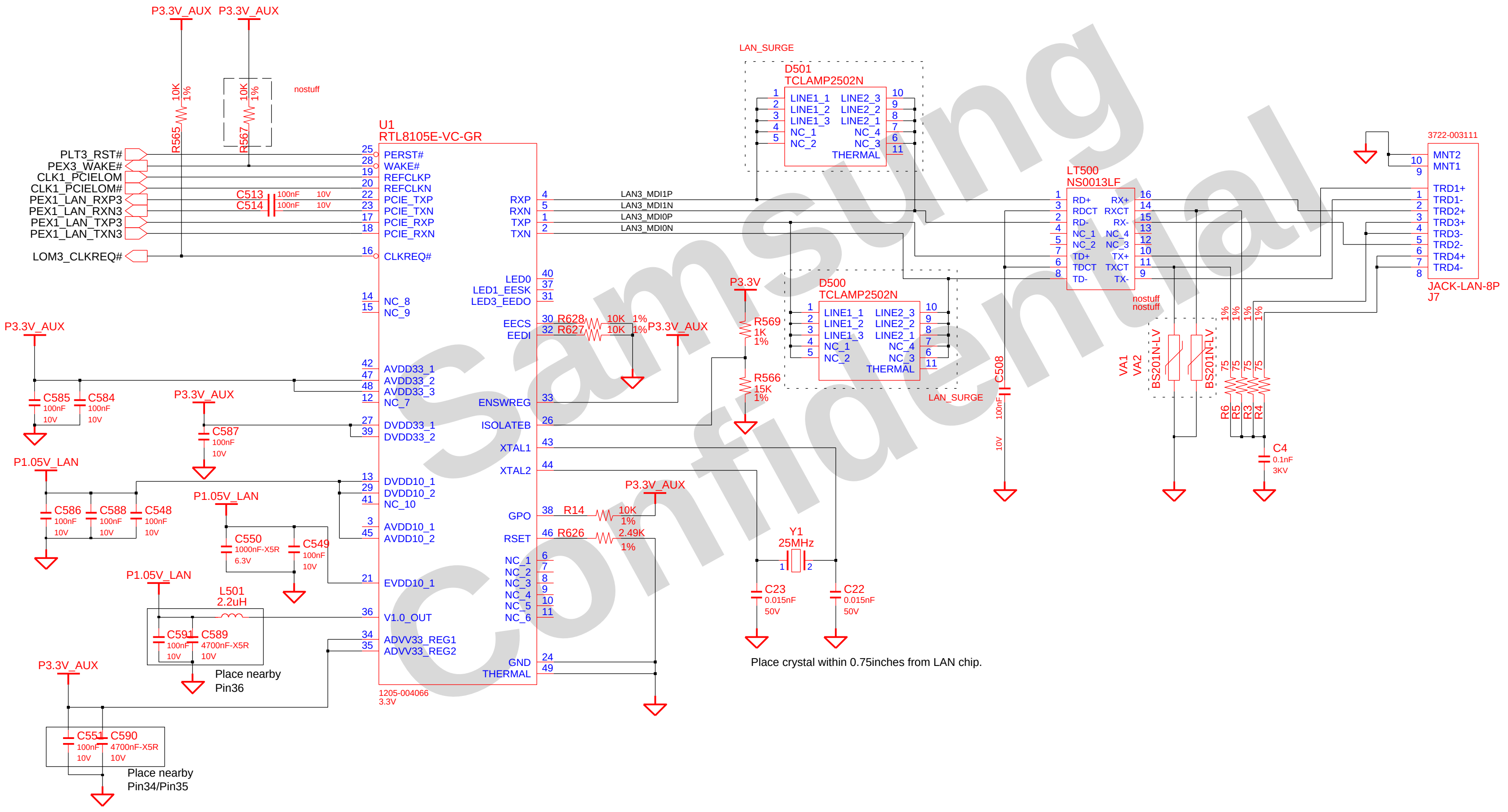


DESIGN	Tang cuili	DATE	12/24/2010	TITLE	SAMSUNG ELECTRONICS
CHECK	Sun xiao	DEV. STEP	MP	Lennon2-L&Lennon-S-R AUDIO AUDIO	PART NO. BA41-0XXXXA
APPROVAL	BC LEE	REV	1.1		
MODULE CODE		LAST EDIT	January 05, 2012 14:48:10 PM	PAGE 23	OF 43

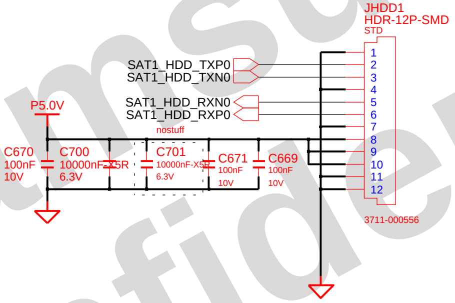
Realtek RTL8105E



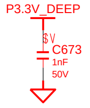
DESIGN	DATE	TITLE	
Tang cuili	12/24/2010	Lennon2-L&Lennon-S-R	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP	LAN	
APPROVAL BC LEE	REV 1.1	RTL8105E	PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT	January 05, 2012 14:48:10 PM	PAGE 24 OF 43

SATA I/F CONN

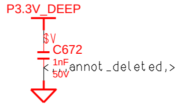
SATA HDD CONN



For EMI

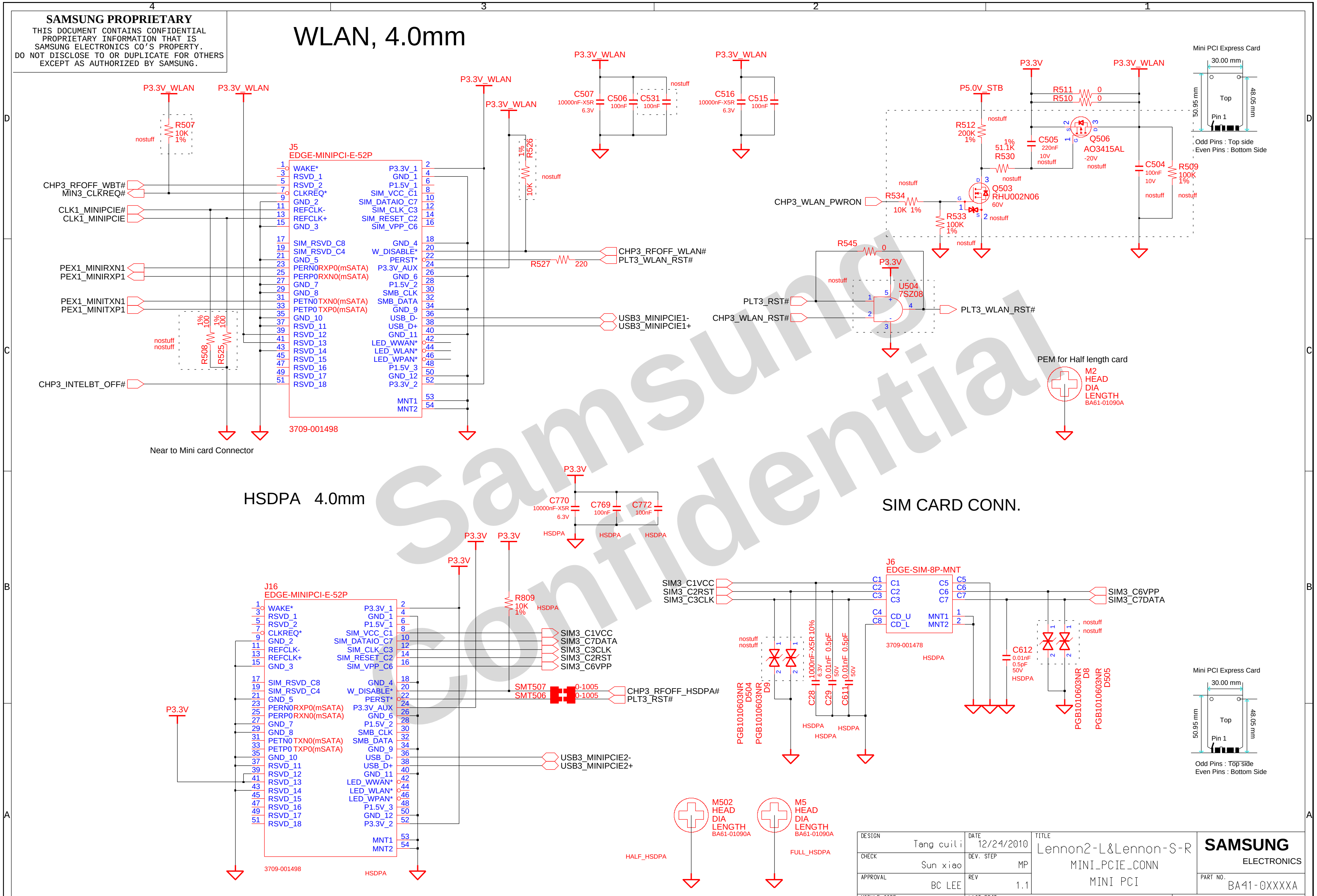


For Tx Signal at changing point of Layer



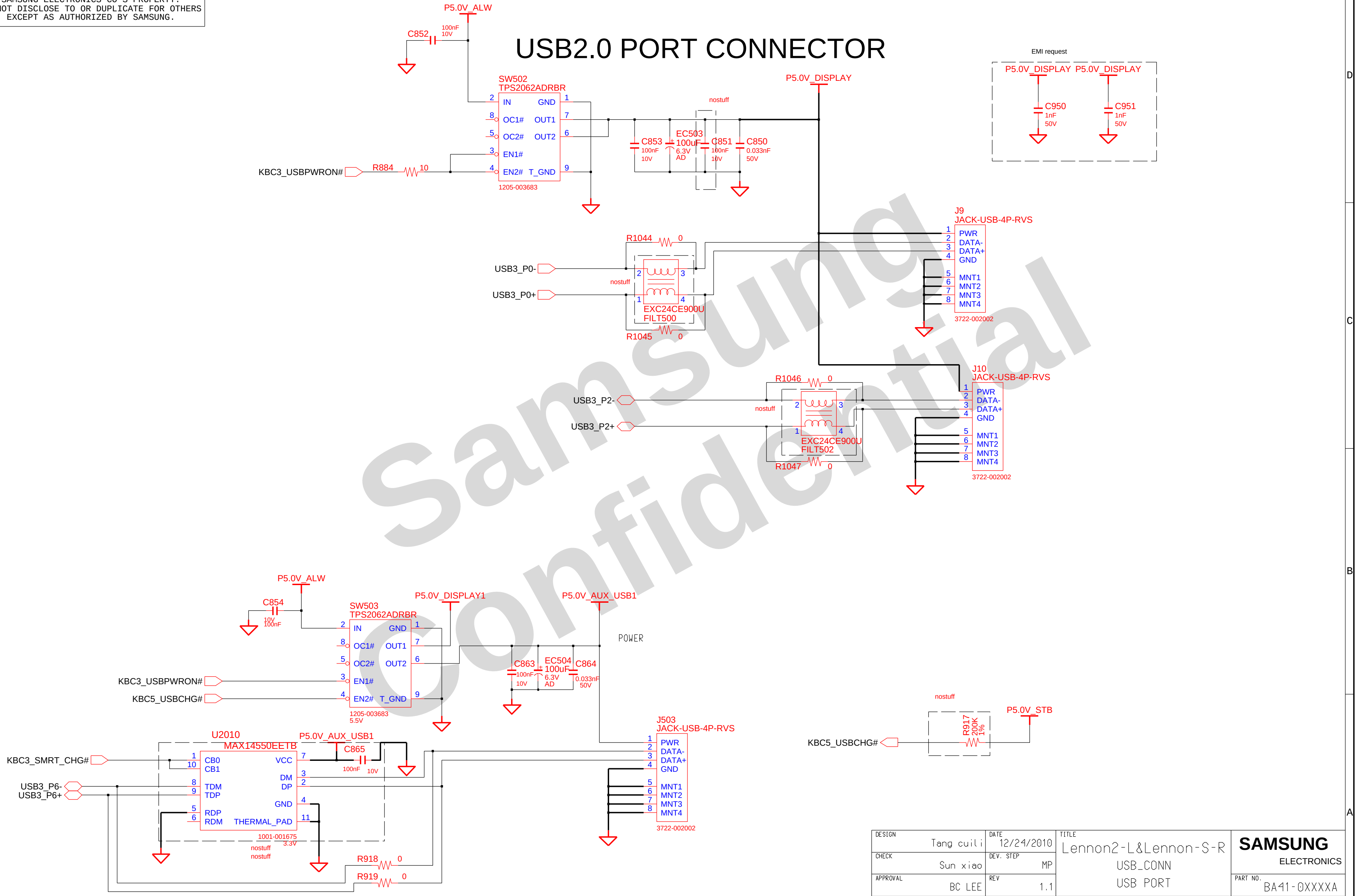
For Rx Signal at changing point of Layer

DESIGN Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R SATA_DEVICES SATA I/F	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM		PAGE 25 OF 43



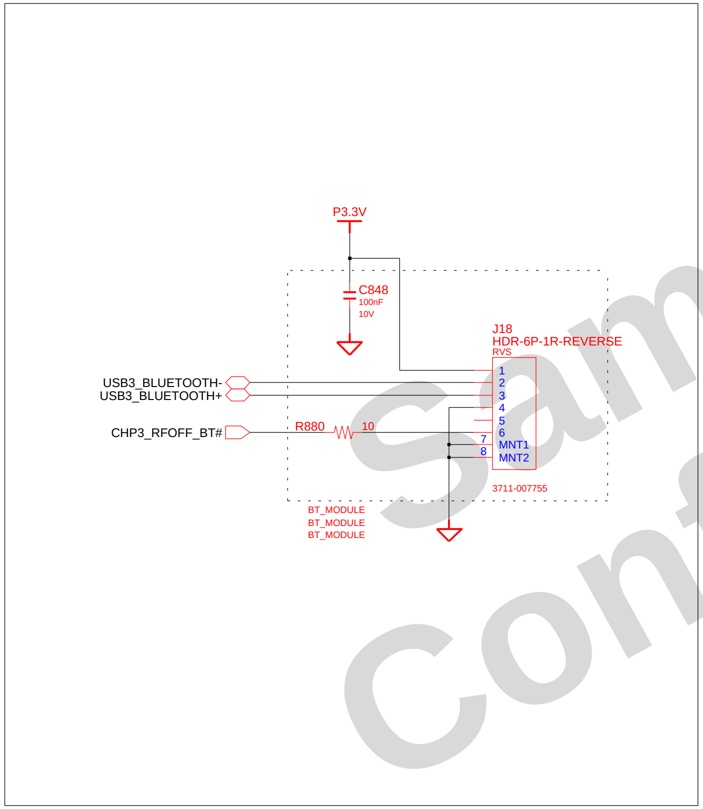
DESIGN	DATE	TITLE	SAMSUNG ELECTRONICS
Tang cuili	12/24/2010	Lennon2-L&Lennon-S-R MINI_PCIE_CONN MINI PCI	
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM	PAGE 26 OF 43	

USB2.0 PORT CONNECTOR

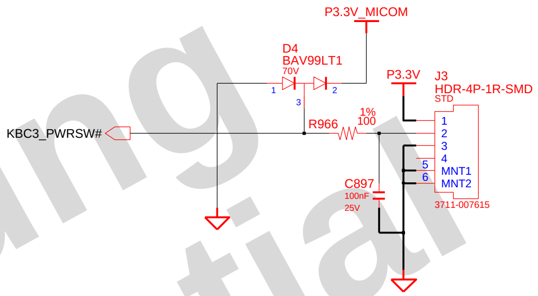


DESIGN	DATE	TITLE	**SAMSUNG** ELECTRONICS
Tang cuili	12/24/2010	Lennon2-L&Lennon-S-R	
CHECK Sun xiao	DEV. STEP MP	USB_CONN	
APPROVAL BC LEE	REV 1.1	USB PORT	PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM	PAGE 27 OF 43	

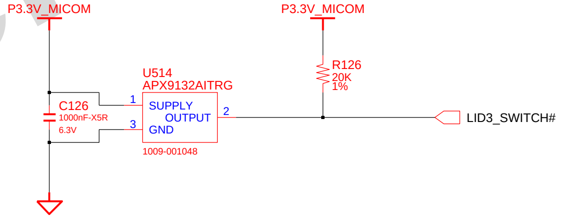
Bluetooth Interface



Power Switch Board Connector

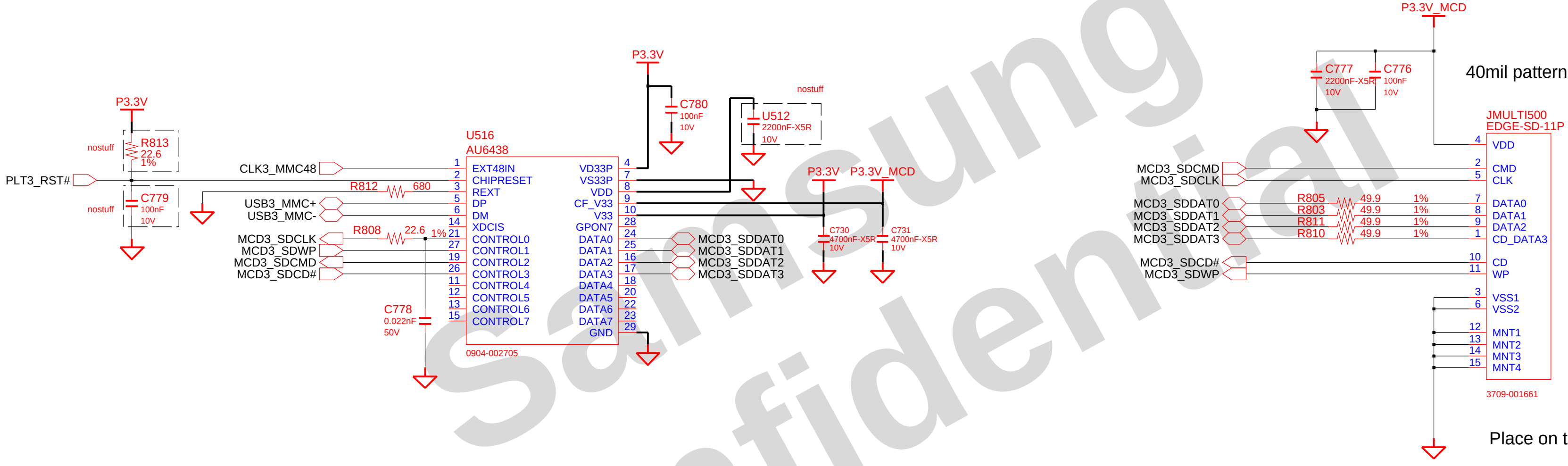


LID SWITCH



DESIGN Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R USB_DEVICES SB I/F BLUETOOTH, System B'D I/F	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM		PAGE 28 OF 43

MMC(AU6438)



40mil pattern

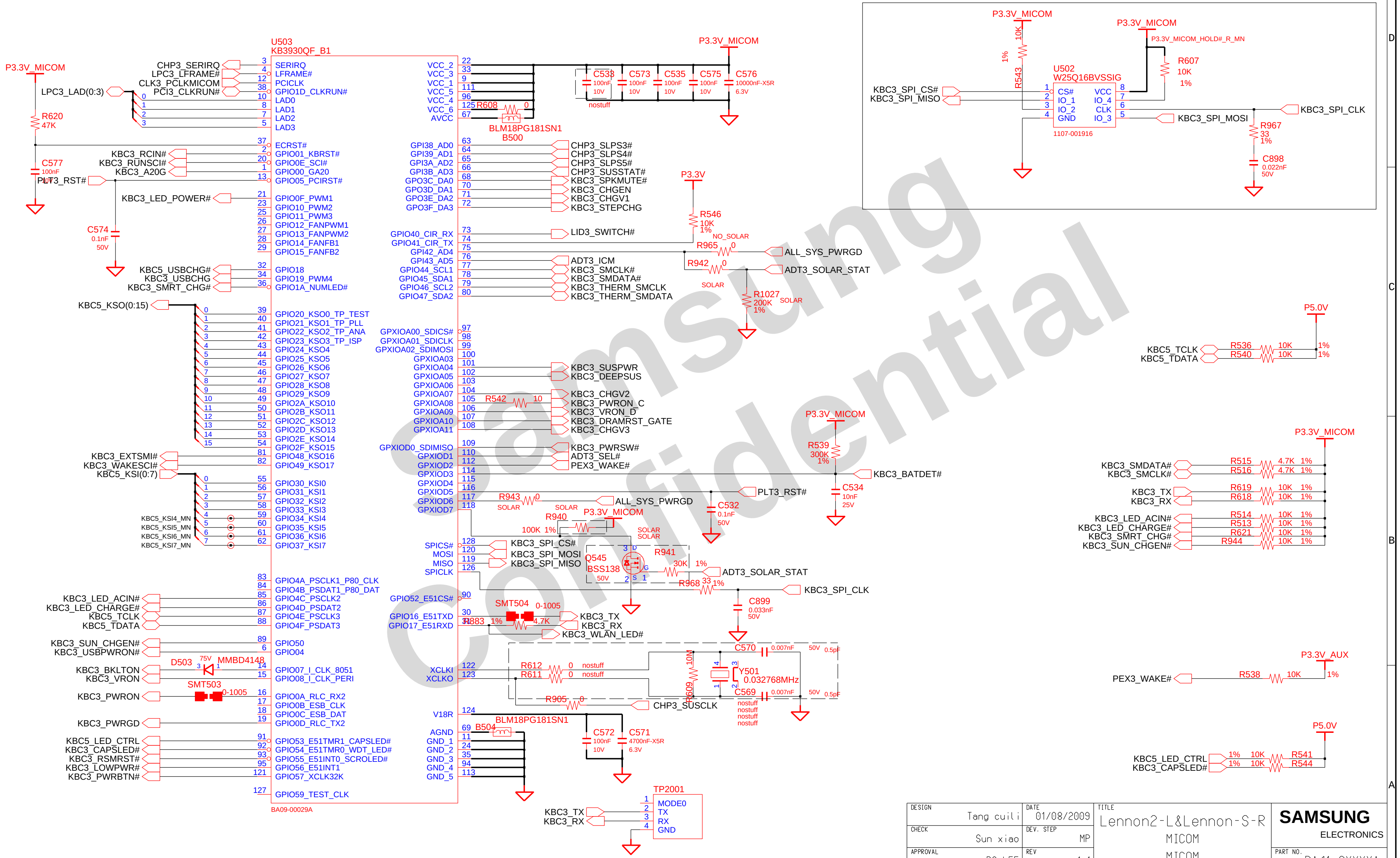
Place on top-side

40 mil trace for medica card socket ground

DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R MMC AU6437	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM	PAGE 29 OF 43	

MAIN BOARD (MICOM 3930)

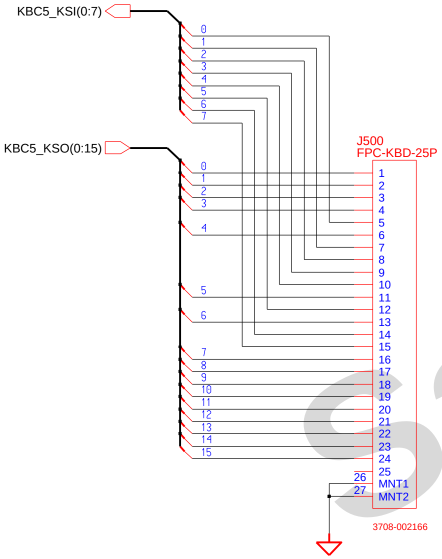
BE CAUTION SPI ROM SIZE!!



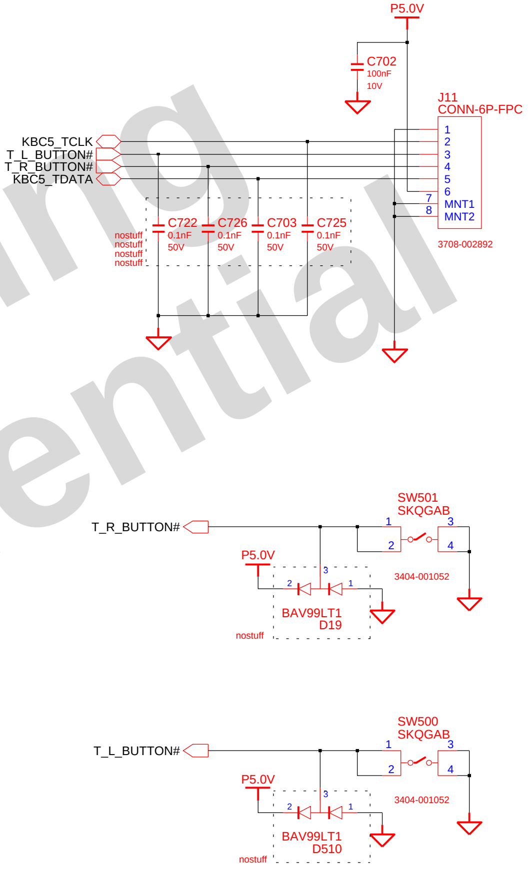
DESIGN	DATE	TITLE	SAMSUNG ELECTRONICS
Tang cuili	01/08/2009	Lennon2-L&Lennon-S-R	
CHECK Sun xiao	DEV. STEP MP	MICOM	
APPROVAL BC LEE	REV 1.1	MICOM	PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM	PAGE 30 OF 43	

Micom Glue Logic

KEYBOARD

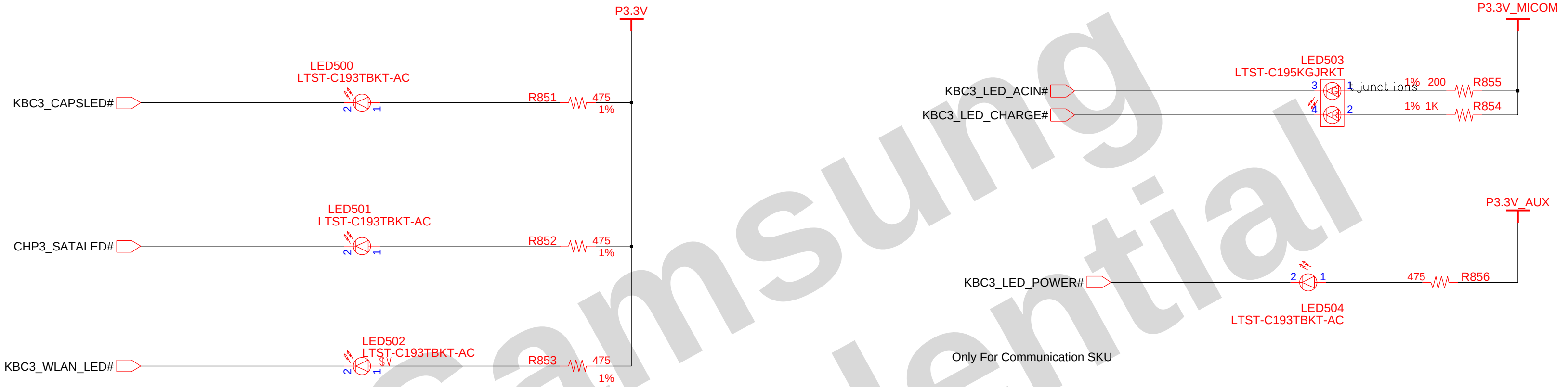


TOUCHPAD



DESIGN Tang cuili
CHECK Sun xiao
APPROVAL BC LEE
MODULE CODE
DATE 12/24/2010
DEV. STEP MP
REV 1.1
LAST EDIT January 05, 2012 14:48:10 PM
TITLE Lennon2-L&Lennon-S-R
MICOM
MICOM GLUE LOGIC
SAMSUNG
ELECTRONICS
PART NO. BA41-0XXXXA

LED SWITCH LOGIC



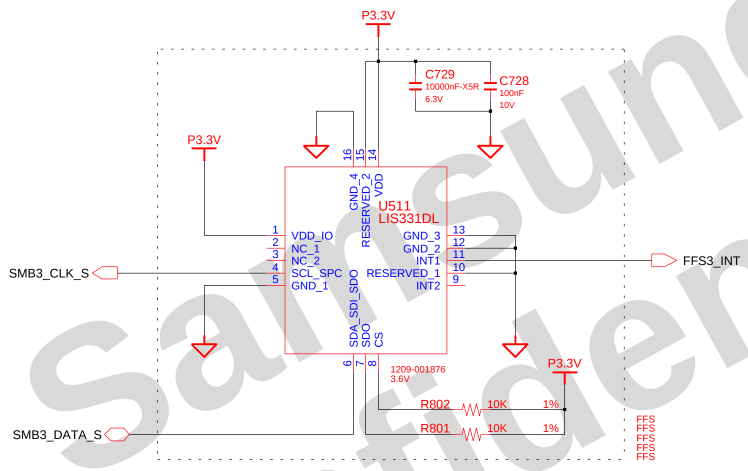
Only For Communication SKU

DRAW	DATE	TITLE	
Tang cuili	12/24/2010	Lennon2-L&Lennon-S-R	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP	LED_Switch	
APPROVAL BC LEE	REV 1.1	LED_Switch	PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM		

COM-22C-015(1996.6.5) REV. 3

D:/users/ecad60/MP1.1/Lennon2_L_MP1.1_power

FREE FALL SENSOR



DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R FFS FreeFallSensor		**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP			
APPROVAL BC LEE	REV 1.1			PART NO. BA41-0XXXXA
MODULE CODE undefined	LAST EDIT	January 05, 2012 14:48:10 PM	PAGE 33	OF 43

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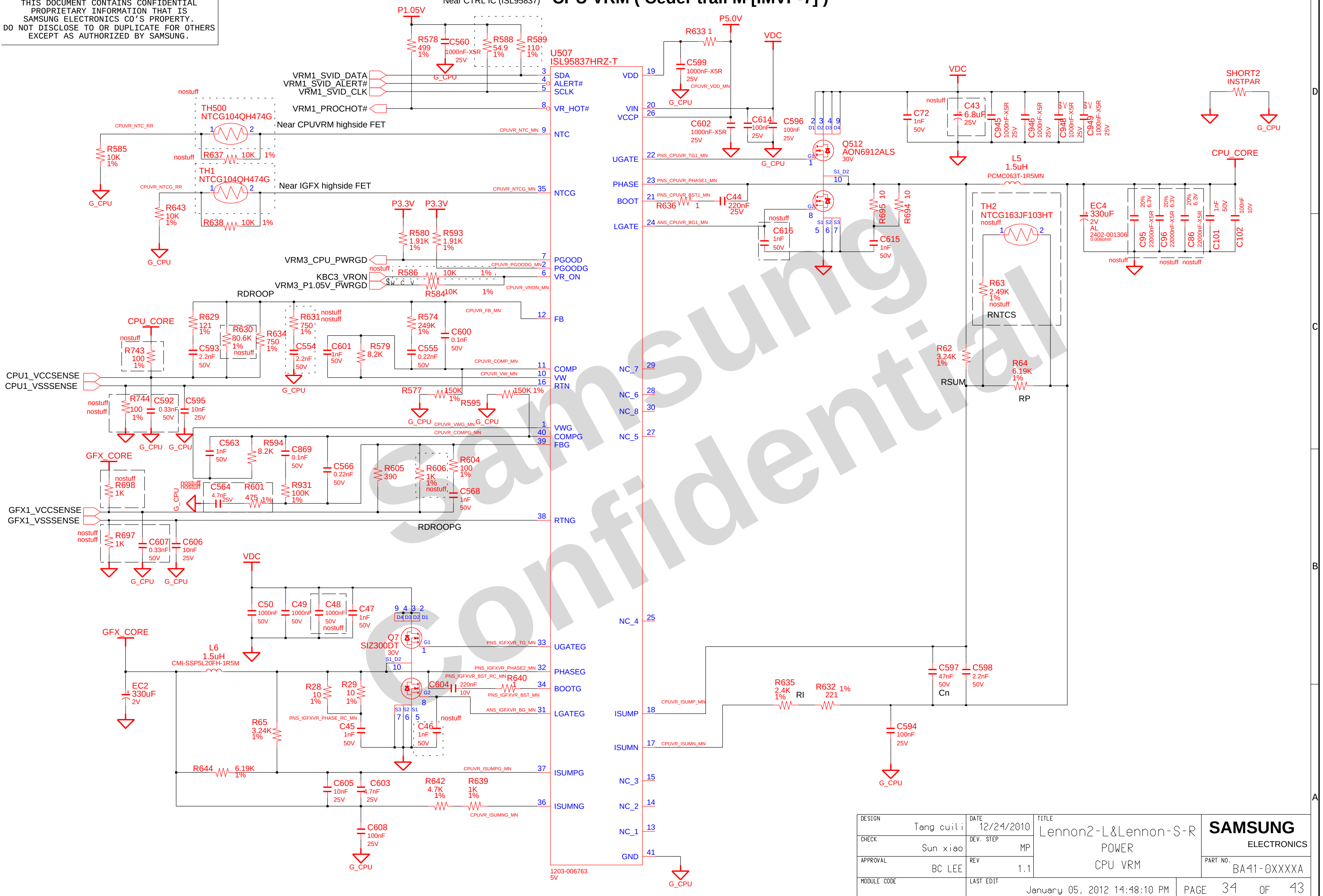
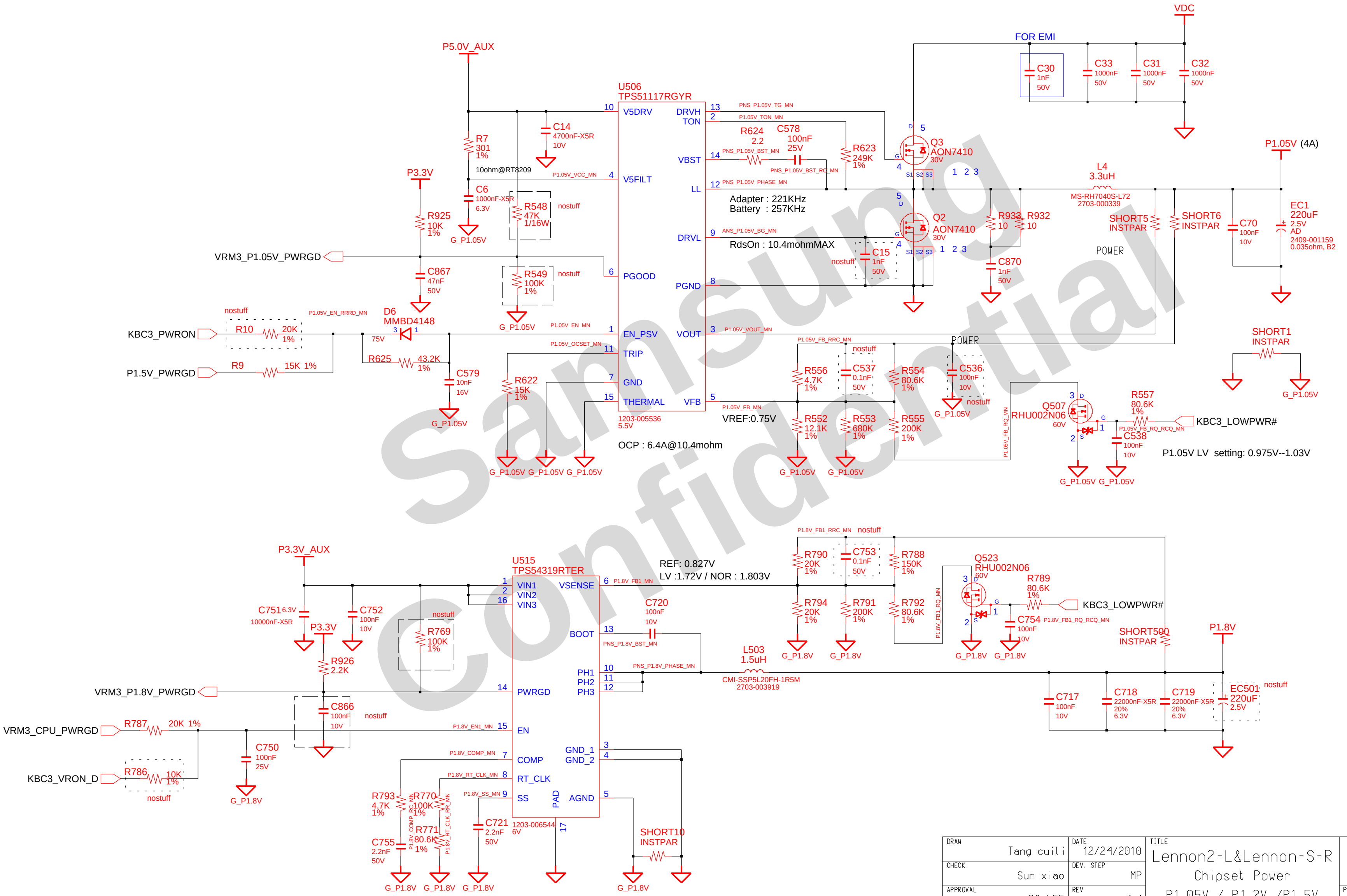
CPU VRM (Ceder trail M [IMVP-7])



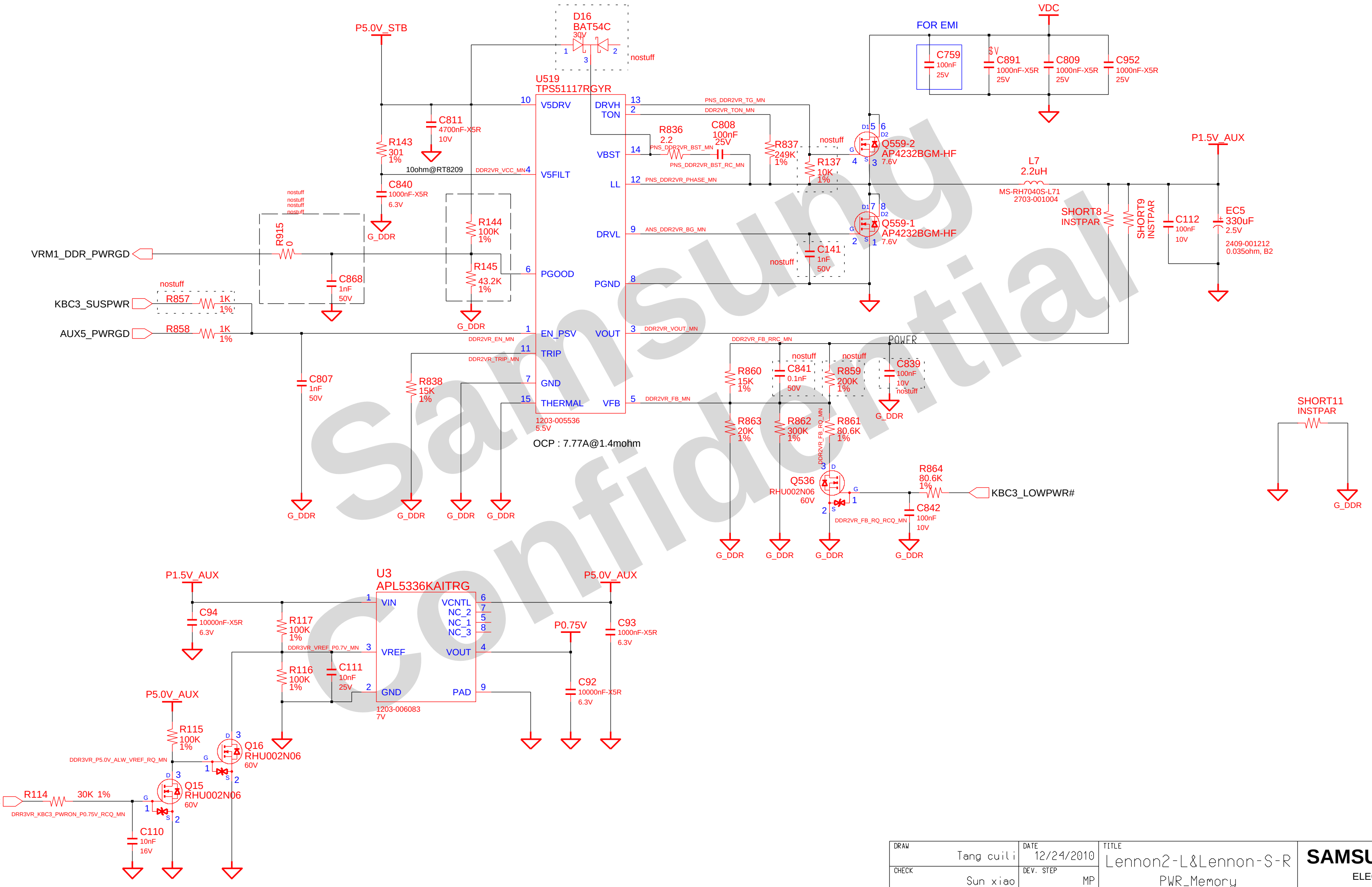
DESIGN	Tang cuili	DATE	12/24/2010	TITLE	**SAMSUNG** ELECTRONICS
CHECK	Sun xiao	DEV. STEP	MP	Lennon2-L&Lennon-S-R POWER CPU VRM	
APPROVAL	BC LEE	REV	1.1		PART NO. BA41-0XXXXA
MODULE CODE		LAST EDIT	January 05, 2012 14:48:10 PM	PAGE 34 OF 43	

Chipset Power (P1.8V & P1.05V)



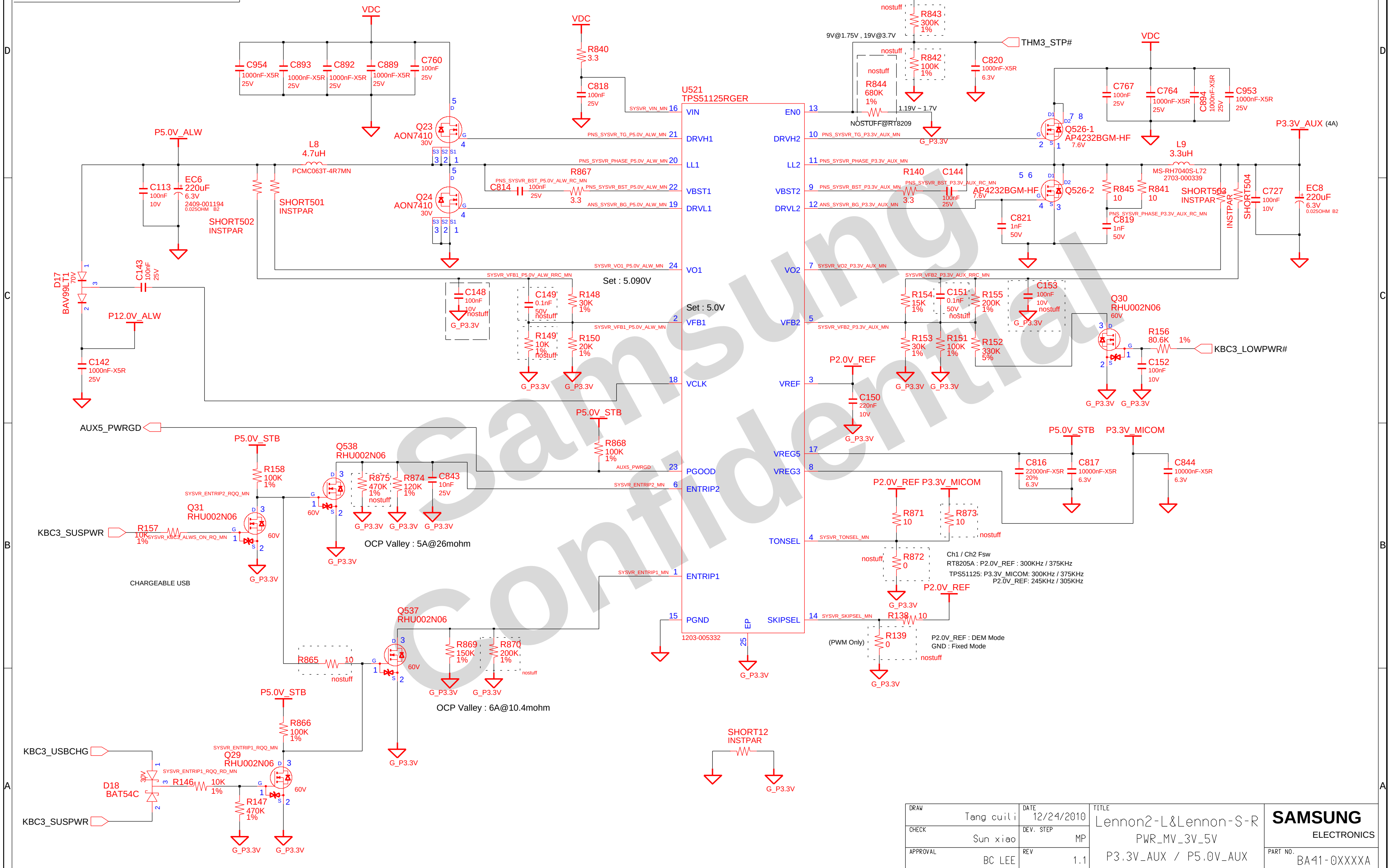
DRAW	DATE	TITLE	
Tang cuili	12/24/2010	Lennon2-L&Lennon-S-R	SAMSUNG ELECTRONICS
CHECK Sun xiao	DEV. STEP MP	Chipset Power	
APPROVAL BC LEE	REV 1.1	P1.05V / P1.2V /P1.5V	PART NO. BA41-0XXXXA
MODULE CODE undefined	LAST EDIT January 05, 2012 14:48:10 PM		PAGE 35 OF 43

DDR3 Power (P1.5V_AUX & 0.75V)



DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R PWR_Memory P1.8V_AUX	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE undefined	LAST EDIT January 05, 2012 14:48:10 PM	PAGE 36 OF 43	

P3.3V_AUX & P5.0V_ALW



DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE undefined	LAST EDIT January 05, 2012 14:48:10 PM	PAGE 37 OF 43	

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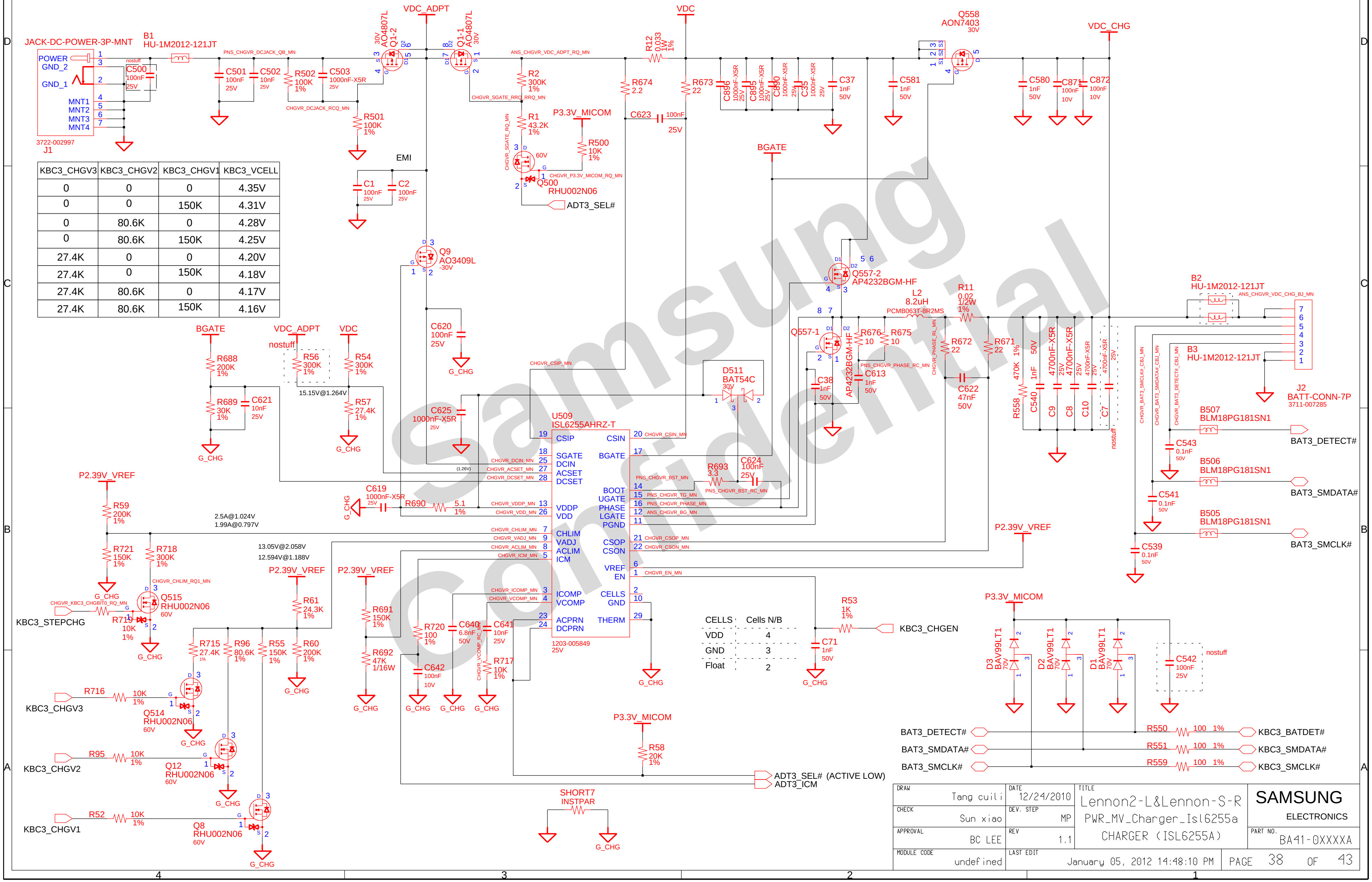
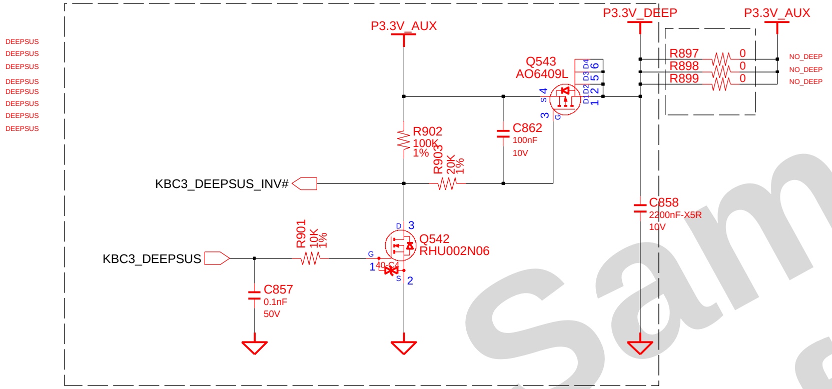
CHARGER & POWER MANAGEMENT



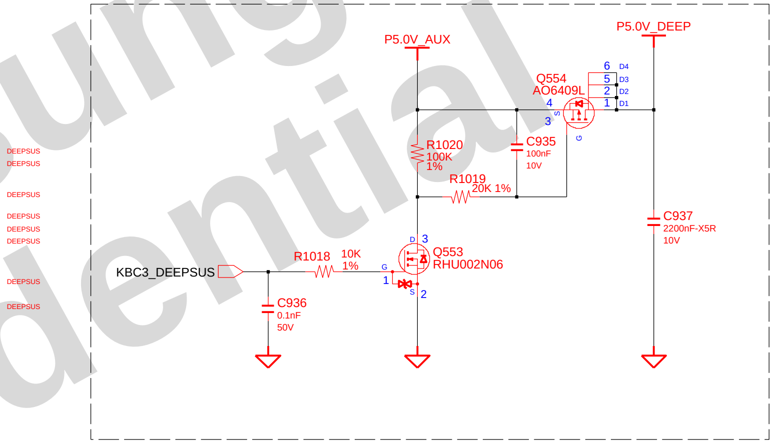
KBC3_CHGV3	KBC3_CHGV2	KBC3_CHGV1	KBC3_VCELL
0	0	0	4.35V
0	0	150K	4.31V
0	80.6K	0	4.28V
0	80.6K	150K	4.25V
27.4K	0	0	4.20V
27.4K	0	150K	4.18V
27.4K	80.6K	0	4.17V
27.4K	80.6K	150K	4.16V

DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R PWR_MV_Charger_Isl6255a CHARGER (ISL6255A)	SAMSUNG ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE undefined	LAST EDIT January 05, 2012 14:48:10 PM		PAGE 38 OF 43

Load Switch Control (P3.3V_DEEP)

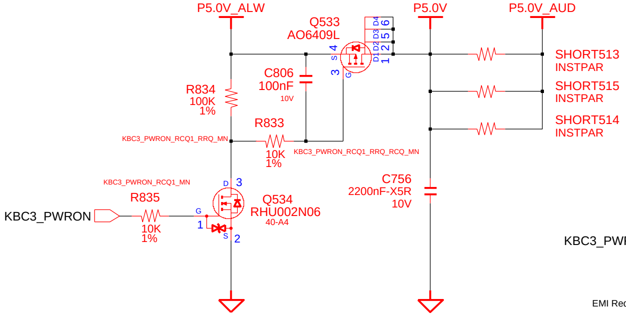


Load Switch Control (P5.0V_DEEP)

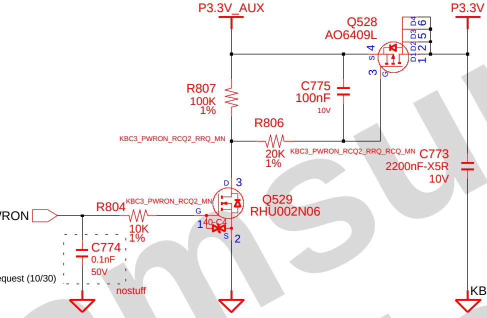


DESIGN Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R INT GFX POWER 0.89V	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM		PAGE 39 OF 43

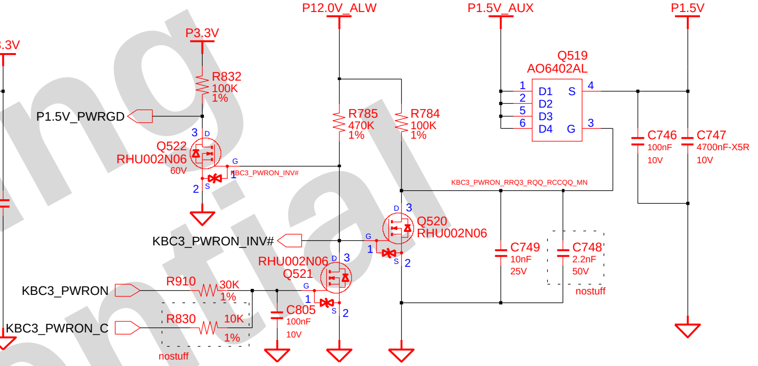
Load Switch Control (P5.0V)



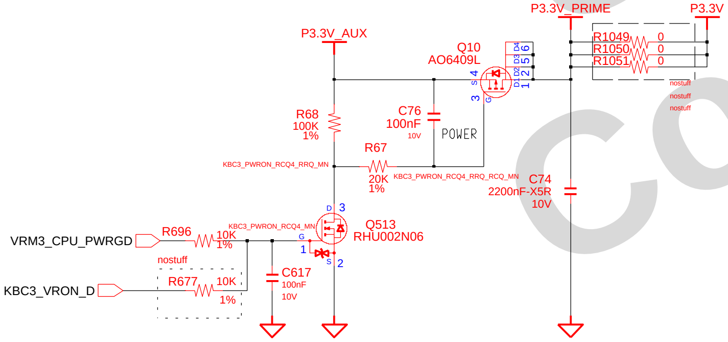
Load Switch Control (P3.3V)



Load Switch Control (P1.5V)

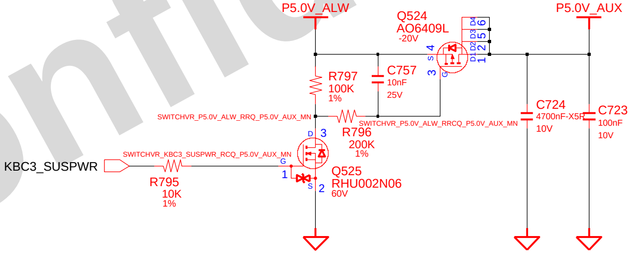


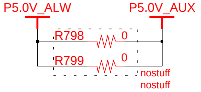
Load Switch Control (P3.3V_PRIME)



Sleep'n Charger

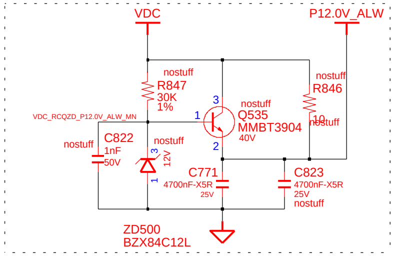
CHARGEABLE USB





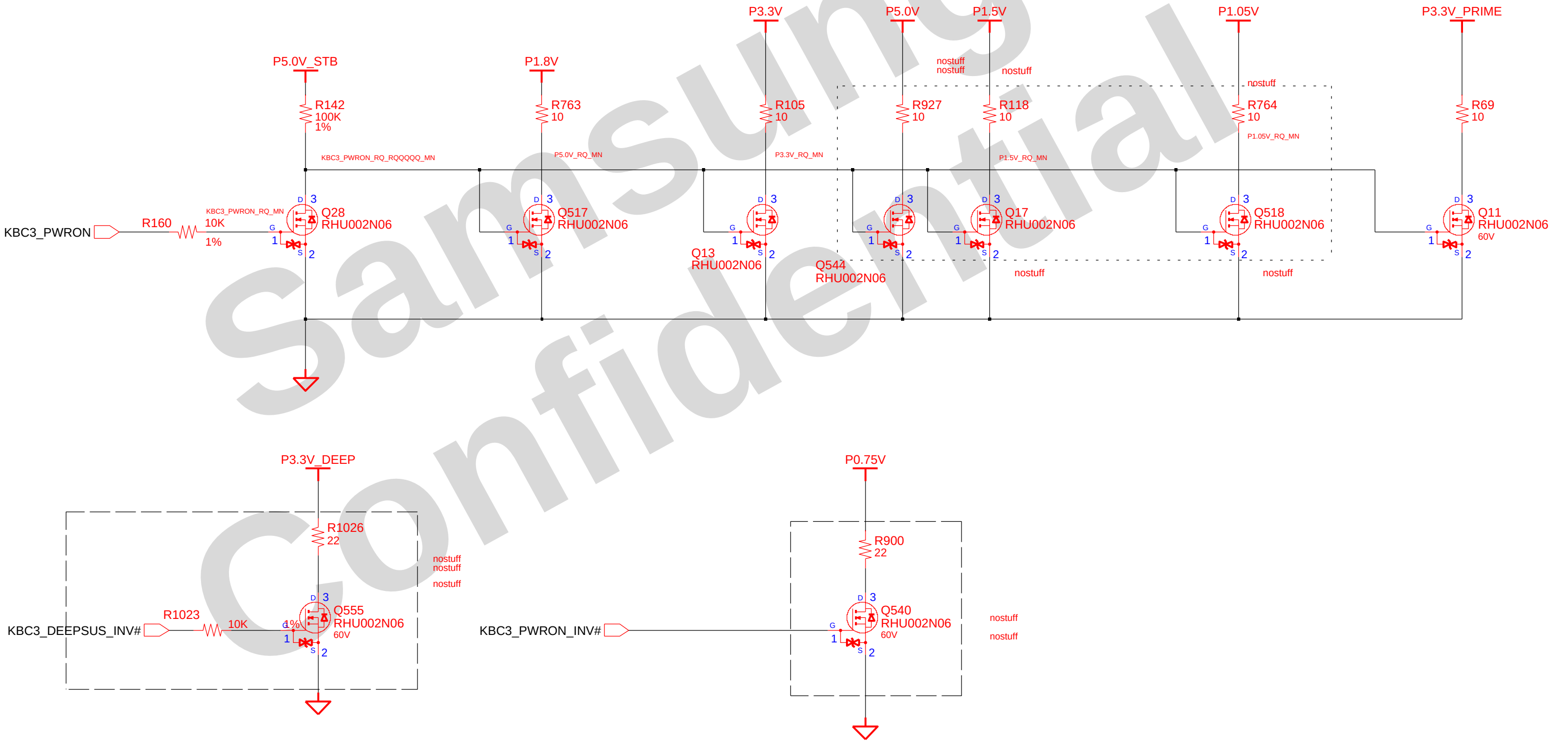
For Non-CHARGEABLE USB

P12V_ALW



DESIGN Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R Switched PWR Switched PWR	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		
APPROVAL BC LEE	REV 1.1		PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM		PAGE 40 OF 43

PWR Discharger



DRAW Tang cuili
CHECK Sun xiao
APPROVAL BC LEE
MODULE CODE

DATE 12/24/2010
DEV. STEP MP
REV 1.1
LAST EDIT January 05, 2012 14:48:10 PM

TITLE
Lennon2-L&Lennon-S-R
Discharger
Discharger

SAMSUNG
ELECTRONICS

PART NO. BA41-0XXXXA

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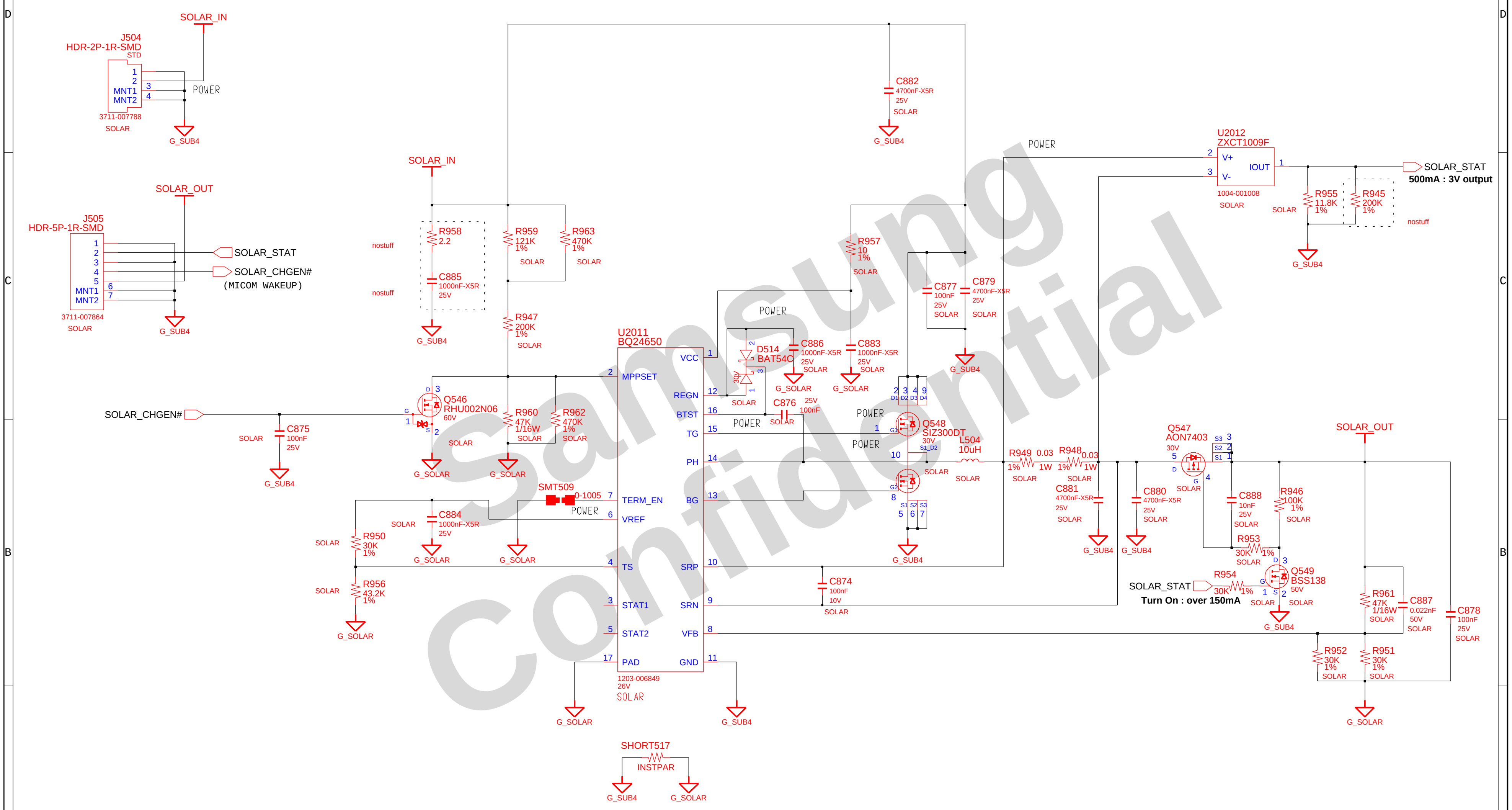
COM-22C-015(1996.6.5) REV. 3

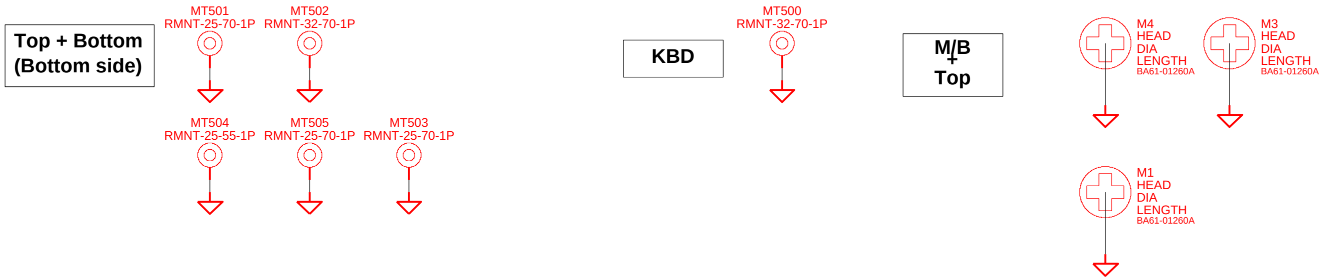
D:/users/ecad60/MP1.1/Lennon2_L_MP1.1_power

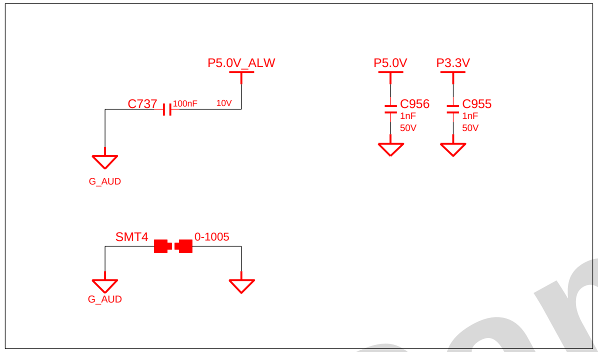
Solar Cell Logic Board

(ASSY CODE : BA92-09575A)

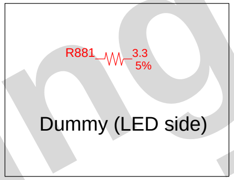


DESIGN Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R	**SAMSUNG** ELECTRONICS
CHECK Sun xiao	DEV. STEP MP	Solar Cell	
APPROVAL BC LEE	REV 1.1	Solar Cell	PART NO. BA41-0XXXXA
MODULE CODE	LAST EDIT	January 05, 2012 14:48:10 PM	PAGE 42 OF 43





FOR EMI



multi_assy selection

	BT_COMBO	BT_MODULE	HSDPA	LAN_SURGE	FFS
WLAN + BT Module	X	O	X	X	X
WLAN/BT Combo	O	X	X	X	X
WLAN Only	X	X	X	X	X
HSPA + WLAN/BT	O	X	O	X	X
HSPA + WLAN	X	X	O	X	X
For China	D/C	D/C	D/C	O	X

* D/C stands for "Don't Care"

DRAW Tang cuili	DATE 12/24/2010	TITLE Lennon2-L&Lennon-S-R ETC ETC	SAMSUNG ELECTRONICS
CHECK Sun xiao	DEV. STEP MP		PART NO. BA41-0XXXXA
APPROVAL BC LEE	REV 1.1		
MODULE CODE	LAST EDIT January 05, 2012 14:48:10 PM		PAGE 43 OF 43