H77H2-EM

Rev : A

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V.A	2011/XX/XX	Base on MRS of H77H2-EM (2011-XX-XX)
V.A	2011/05/26	Modify from H77H2-LM V.B (2011-05-16)
V.A	2011/08/29	Modify ISL6363 for Nph=4 to Nph=3.

NOTE:

Design by
29517_29517_Maho_Bay_and__PDG_Rev0_7.pvd
29057_29057_Panther Point_EDS_29057,0.5v1.pvd
MahoBay_Schematic_Rev0p70.pdf

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Title: Cover Page		
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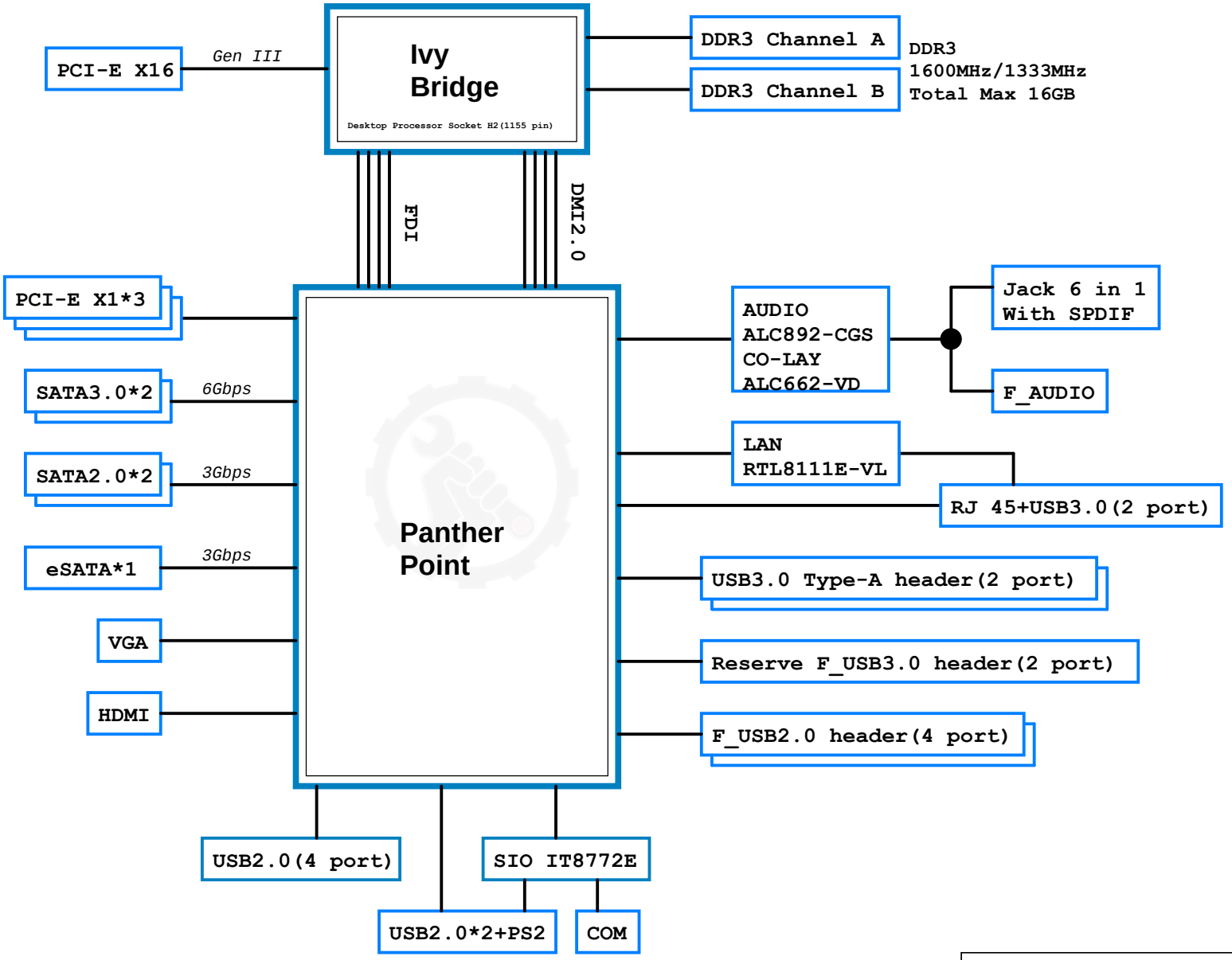

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Title: Block Diagram		
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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	GP1_BOMDET2	GPI
GPIO6	VCC3	GP6_BOMDET3	GPI
GPIO7	VCC3	GP7_BOMDET4	GPI
GPIO9	3VSB	USB_OC_L5	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO13	3VSB	LPC_PME	GPI
GPIO14	+DIMM_5VDUAL	PCH_LED1	Native
GPIO17	VCC3	GP17_BOMDET1	GPI
GPIO21	VCC3	GPIO21_COM2_DET	GPI
GPIO22	VCC3	CLR_CMOS_GP22	GPI
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO39	VCC3	GPIO39_CASE0	GPI
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO45	3VSB	WLAN_DIS_L	Native
GPIO48	VCC3	GPIO48_CASE1	GPI
GPIO59	3VSB	USB_OC_L0	Native
GPIO72	3VSB	GPIO72_BOMDET5	Native

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP10	3VSB	SIO_PCIRST3_L	PCIRST3#
GP12	VCC3	SIO_PCIRST1_L	PCIRST1#
GP22	3VSB	SIO_LED0	GP22
GP23	3VSB	DPWROK	CPU_PG
GP30	VCC3	ATXPWRGD	ATXPWRGD
GP31	VCC3	CTS1_L	CTS1#
GP32	VCC3	SIO_RI1_L	RI1#
GP33	VCC3	DCD1_L	DCD1#
GP36	VCC3	FAN_CTL2	FAN_CTL3
GP37	VCC3	FAN_TAC2	FAN_TAC3
GP40	3VSB	GPIO40_S4S5	3VSBSW#
GP41	3VSB	SIN1	SIN1
GP42	3VSB	PSON_L	PSON#
GP43	3VSB	FP_PWRBTN_L	PANSWH#
GP44	3VSB	SIO_PWRBTN_L	PWRON#
GP45	3VSB	DSR1_L	DSR1#
GP51	VCC3	FAN_CTL1	FAN_CTL2
GP52	VCC3	FAN_TAC1	FAN_TAC2
GP53	3VSB	SLP4_L	SUSC#
GP54	3VSB	LPC_PME_L	PME#
GP55	3VSB	RSMRST_L	RSMRST#
GP56	3VSB	MCLK	MCLK
GP57	3VSB	MDATA	MDAT
GP60	3VSB	KCLK	KCLK
GP61	3VSB	KDATA	KDAT
GP62	VCC3	KBRST_L	KRST#
GP65	3VSB	SMLK1_SIO_DATA	VLDT_EN

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Title: GPIO Function Map

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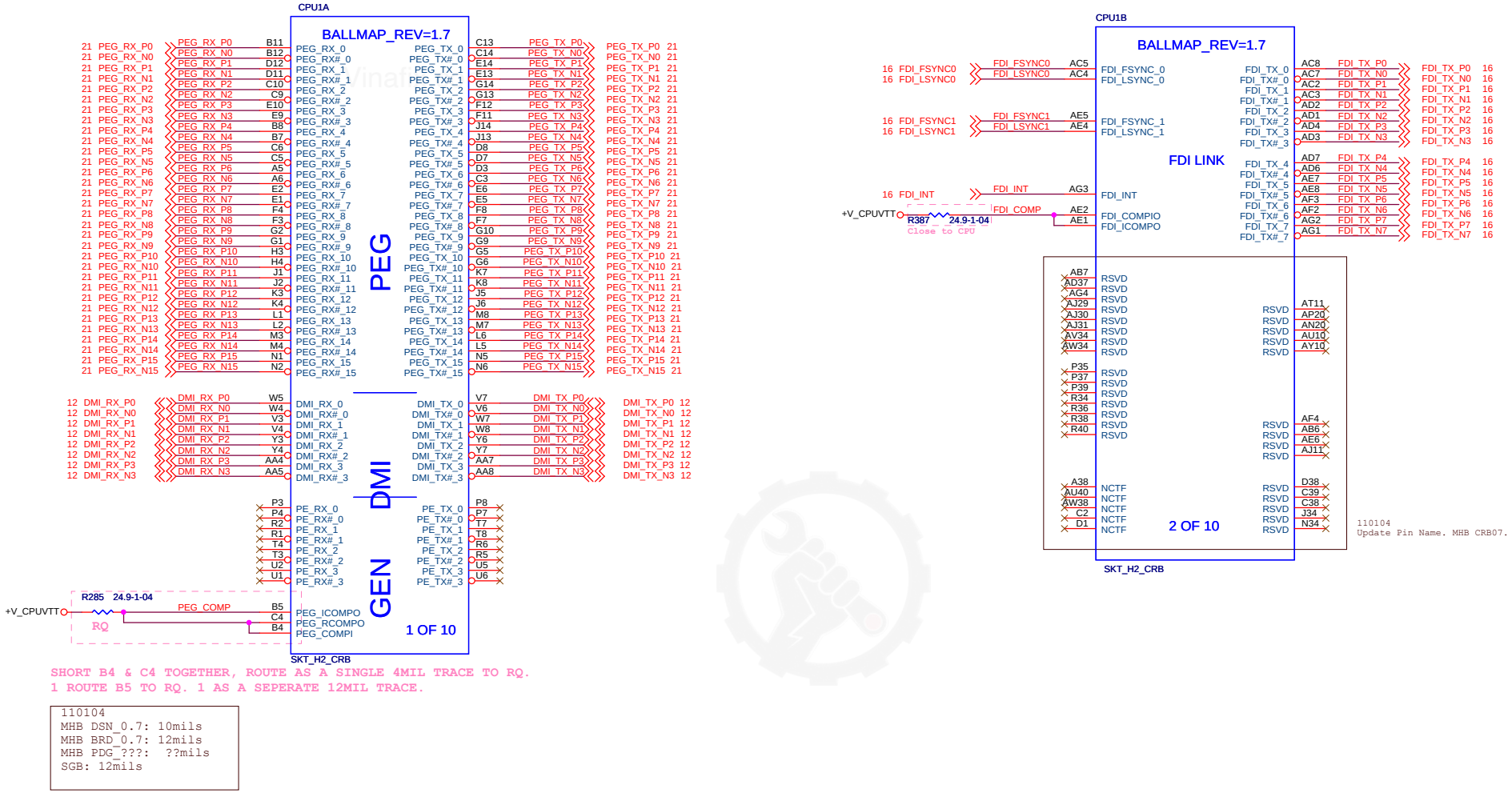

Title	CPU - DMI/FDI/PEG
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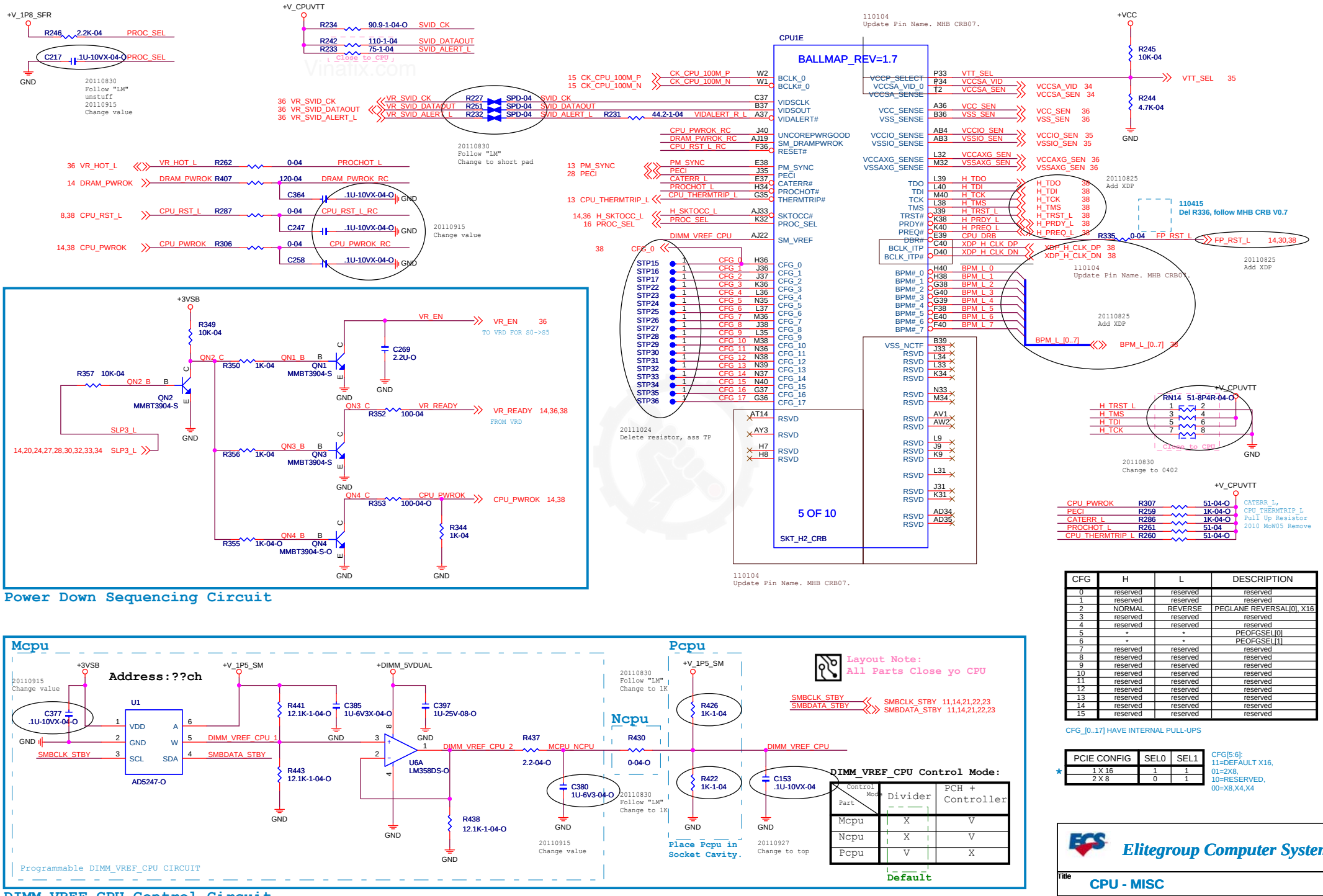

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

* CFG[5:6]: 11=DEFAULT X16, 01=2X8, 10=RESERVED, 00=X8,X4,X4

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Title: CPU - MISC

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DDR3 CH.A

9 M_DATA_A[0..63] — M_DATA_A[0..63]
9 M_DQS_A_P[0..7] — M_DQS_A_P[0..7]
9 M_DQS_A_N[0..7] — M_DQS_A_N[0..7]
9 M_MA_A[0..15] — M_MA_A[0..15]
9 M_BS_A[0..2] — M_BS_A[0..2]
9 M_CS_A_L[0..3] — M_CS_A_L[0..3]
9 M_CKE_A[0..3] — M_CKE_A[0..3]
9 M_ODT_A[0..3] — M_ODT_A[0..3]
9 M_CLK_A_P[0..3] — M_CLK_A_P[0..3]
9 M_CLK_A_N[0..3] — M_CLK_A_N[0..3]
9 M_WE_A_L — M_WE_A_L
9 M_CAS_A_L — M_CAS_A_L
9 M_RAS_A_L — M_RAS_A_L

9,10 DDR3_DRAMRST_L — DDR3_DRAMRST_L

DDR3 CH.B

10 M_DATA_B[0..63] — M_DATA_B[0..63]
10 M_DQS_B_P[0..7] — M_DQS_B_P[0..7]
10 M_DQS_B_N[0..7] — M_DQS_B_N[0..7]
10 M_MA_B[0..15] — M_MA_B[0..15]
10 M_BS_B[0..2] — M_BS_B[0..2]
10 M_CS_B_L[0..3] — M_CS_B_L[0..3]
10 M_CKE_B[0..3] — M_CKE_B[0..3]
10 M_ODT_B[0..3] — M_ODT_B[0..3]
10 M_CLK_B_P[0..3] — M_CLK_B_P[0..3]
10 M_CLK_B_N[0..3] — M_CLK_B_N[0..3]
10 M_WE_B_L — M_WE_B_L
10 M_CAS_B_L — M_CAS_B_L
10 M_RAS_B_L — M_RAS_B_L

CPU1C

BALLMAP_REV=1.7

M_DATA_A0	AJ3	SA_DQ_0	SA_MA_0	AV27	M_MA_A0
M_DATA_A1	AJ4	SA_DQ_1	SA_MA_1	AY24	M_MA_A1
M_DATA_A2	AL3	SA_DQ_2	SA_MA_2	AW24	M_MA_A2
M_DATA_A3	AL4	SA_DQ_3	SA_MA_3	AW23	M_MA_A3
M_DATA_A4	AJ2	SA_DQ_4	SA_MA_4	AY23	M_MA_A4
M_DATA_A5	AJ1	SA_DQ_5	SA_MA_5	AT24	M_MA_A5
M_DATA_A6	AL2	SA_DQ_6	SA_MA_6	AT23	M_MA_A6
M_DATA_A7	AL1	SA_DQ_7	SA_MA_7	AU22	M_MA_A7
M_DATA_A8	AN1	SA_DQ_8	SA_MA_8	AV22	M_MA_A8
M_DATA_A9	AN4	SA_DQ_9	SA_MA_9	AT22	M_MA_A9
M_DATA_A10	AR3	SA_DQ_10	SA_MA_10	AV28	M_MA_A10
M_DATA_A11	AR4	SA_DQ_11	SA_MA_11	AU21	M_MA_A11
M_DATA_A12	AN2	SA_DQ_12	SA_MA_12	AT21	M_MA_A12
M_DATA_A13	AN3	SA_DQ_13	SA_MA_13	AW32	M_MA_A13
M_DATA_A14	AR2	SA_DQ_14	SA_MA_14	AU20	M_MA_A14
M_DATA_A15	AR1	SA_DQ_15	SA_MA_15	AT20	M_MA_A15
M_DATA_A16	AV2	SA_DQ_16			
M_DATA_A17	AW3	SA_DQ_17			
M_DATA_A18	AV5	SA_DQ_18	SA_WE#	AW29	M_WE_A_L
M_DATA_A19	AW5	SA_DQ_19	SA_CAS#	AV30	M_CAS_A_L
M_DATA_A20	AU2	SA_DQ_20	SA_RAS#	AU28	M_RAS_A_L
M_DATA_A21	AU3	SA_DQ_21			
M_DATA_A22	AU5	SA_DQ_22			
M_DATA_A23	AY5	SA_DQ_23	SA_BS_0	AY29	M_BS_A0
M_DATA_A24	AY7	SA_DQ_24	SA_BS_1	AW28	M_BS_A1
M_DATA_A25	AU7	SA_DQ_25	SA_BS_2	AV20	M_BS_A2
M_DATA_A26	AV9	SA_DQ_26			
M_DATA_A27	AU9	SA_DQ_27			
M_DATA_A28	AV7	SA_DQ_28	SA_CS#_0	AU29	M_CS_A_L0
M_DATA_A29	AW7	SA_DQ_29	SA_CS#_1	AV32	M_CS_A_L1
M_DATA_A30	AW9	SA_DQ_30	SA_CS#_2	AW30	M_CS_A_L2
M_DATA_A31	AY9	SA_DQ_31	SA_CS#_3	AU33	M_CS_A_L3
M_DATA_A32	AU35	SA_DQ_32			
M_DATA_A33	AW37	SA_DQ_33			
M_DATA_A34	AU39	SA_DQ_34			
M_DATA_A35	AU36	SA_DQ_35	SA_CKE_0	AV19	M_CKE_A0
M_DATA_A36	AW35	SA_DQ_36	SA_CKE_1	AT19	M_CKE_A1
M_DATA_A37	AY36	SA_DQ_37	SA_CKE_2	AU18	M_CKE_A2
M_DATA_A38	AU38	SA_DQ_38	SA_CKE_3	AV18	M_CKE_A3
M_DATA_A39	AU37	SA_DQ_39			
M_DATA_A40	AR40	SA_DQ_40			
M_DATA_A41	AR37	SA_DQ_41			
M_DATA_A42	AN38	SA_DQ_42	SA_ODT_0	AV31	M_ODT_A0
M_DATA_A43	AN37	SA_DQ_43	SA_ODT_1	AU32	M_ODT_A1
M_DATA_A44	AR39	SA_DQ_44	SA_ODT_2	AU30	M_ODT_A2
M_DATA_A45	AR38	SA_DQ_45	SA_ODT_3	AW33	M_ODT_A3
M_DATA_A46	AN39	SA_DQ_46			
M_DATA_A47	AN40	SA_DQ_47			
M_DATA_A48	AL40	SA_DQ_48			
M_DATA_A49	AL37	SA_DQ_49	SA_CK_0	AY25	M_CLK_A_P0
M_DATA_A50	AJ38	SA_DQ_50	SA_CK#_0	AW25	M_CLK_A_N0
M_DATA_A51	AJ37	SA_DQ_51	SA_CK_1	AU24	M_CLK_A_P1
M_DATA_A52	AL39	SA_DQ_52	SA_CK#_1	AU25	M_CLK_A_N1
M_DATA_A53	AL38	SA_DQ_53	SA_CK_2	AW27	M_CLK_A_P2
M_DATA_A54	AJ39	SA_DQ_54	SA_CK#_2	AY27	M_CLK_A_N2
M_DATA_A55	AJ40	SA_DQ_55	SA_CK_3	AV26	M_CLK_A_P3
M_DATA_A56	AG40	SA_DQ_56	SA_CK#_3	AW26	M_CLK_A_N3
M_DATA_A57	AG37	SA_DQ_57			
M_DATA_A58	AE38	SA_DQ_58			
M_DATA_A59	AE37	SA_DQ_59			
M_DATA_A60	AG39	SA_DQ_60			
M_DATA_A61	AG38	SA_DQ_61			
M_DATA_A62	AE39	SA_DQ_62			
M_DATA_A63	AE40	SA_DQ_63			

SM_DRAMRST# — AW18 — DDR3_DRAMRST_R_L — R479 0-04 — DDR3_DRAMRST_L

C428 .1U-10VX-04-O — GND

20110915 Change value

For RC Filter

M_DQS_A_P0	AK3	SA_DQS_0	SA_DQS_8	AV13	
M_DQS_A_P1	AP3	SA_DQS_1	SA_DQS#_8	AV12	
M_DQS_A_P2	AW4	SA_DQS_2			
M_DQS_A_P3	AV8	SA_DQS_3			
M_DQS_A_P4	AV37	SA_DQS_4	SA_ECC_CB_0	AU12	
M_DQS_A_P5	AP38	SA_DQS_5	SA_ECC_CB_1	AU14	
M_DQS_A_P6	AK38	SA_DQS_6	SA_ECC_CB_2	AW13	
M_DQS_A_P7	AF38	SA_DQS_7	SA_ECC_CB_3	AY13	
			SA_ECC_CB_4	AU13	
			SA_ECC_CB_5	AU11	
M_DQS_A_N0	AK2		SA_ECC_CB_6	AY12	
M_DQS_A_N1	AP2	SA_DQS#_0	SA_ECC_CB_7	AW12	
M_DQS_A_N2	AV4	SA_DQS#_1			
M_DQS_A_N3	AW8	SA_DQS#_2			
M_DQS_A_N4	AV36	SA_DQS#_3			
M_DQS_A_N5	AP39	SA_DQS#_4			
M_DQS_A_N6	AK39	SA_DQS#_5			
M_DQS_A_N7	AF39	SA_DQS#_6			
		SA_DQS#_7			

Desktop dosen't support ECC

DDR_0

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SKT_H2_CRB

Pay Attention to This Part!

CPU1D

BALLMAP_REV=1.7

M_DATA_B0	AG7	SB_DQ_0	SB_MA_0	AK24	M_MA_B0
M_DATA_B1	AG8	SB_DQ_1	SB_MA_1	AM20	M_MA_B1
M_DATA_B2	AJ9	SB_DQ_2	SB_MA_2	AM19	M_MA_B2
M_DATA_B3	AJ8	SB_DQ_3	SB_MA_3	AK18	M_MA_B3
M_DATA_B4	AG5	SB_DQ_4	SB_MA_4	AP19	M_MA_B4
M_DATA_B5	AG6	SB_DQ_5	SB_MA_5	AP18	M_MA_B5
M_DATA_B6	AJ6	SB_DQ_6	SB_MA_6	AM18	M_MA_B6
M_DATA_B7	AJ7	SB_DQ_7	SB_MA_7	AL18	M_MA_B7
M_DATA_B13	AL7	SB_DQ_8	SB_MA_8	AN18	M_MA_B8
M_DATA_B9	AM7	SB_DQ_9	SB_MA_9	AY17	M_MA_B9
M_DATA_B11	AM10	SB_DQ_10	SB_MA_10	AN23	M_MA_B10
M_DATA_B15	AL10	SB_DQ_11	SB_MA_11	AU17	M_MA_B11
M_DATA_B12	AL6	SB_DQ_12	SB_MA_12	AT18	M_MA_B12
M_DATA_B8	AM6	SB_DQ_13	SB_MA_13	AR26	M_MA_B13
M_DATA_B14	AL9	SB_DQ_14	SB_MA_14	AY16	M_MA_B14
M_DATA_B10	AM9	SB_DQ_15	SB_MA_15	AV16	M_MA_B15
M_DATA_B16	AP7	SB_DQ_16			
M_DATA_B17	AR7	SB_DQ_17			
M_DATA_B18	AP10	SB_DQ_18	SB_WE#	AR25	M_WE_B_L
M_DATA_B19	AR10	SB_DQ_19	SB_CAS#	AK25	M_CAS_B_L
M_DATA_B20	AP6	SB_DQ_20	SB_RAS#	AP24	M_RAS_B_L
M_DATA_B21	AR6	SB_DQ_21			
M_DATA_B22	AP9	SB_DQ_22			
M_DATA_B23	AR9	SB_DQ_23	SB_BS_0	AP23	M_BS_B0
M_DATA_B24	AM12	SB_DQ_24	SB_BS_1	AM24	M_BS_B1
M_DATA_B25	AM13	SB_DQ_25	SB_BS_2	AW17	M_BS_B2
M_DATA_B26	AR13	SB_DQ_26			
M_DATA_B27	AP13	SB_DQ_27			
M_DATA_B28	AL12	SB_DQ_28	SB_CS#_0	AN25	M_CS_B_L0
M_DATA_B29	AL13	SB_DQ_29	SB_CS#_1	AN26	M_CS_B_L1
M_DATA_B30	AR12	SB_DQ_30	SB_CS#_2	AL25	M_CS_B_L2
M_DATA_B31	AP12	SB_DQ_31	SB_CS#_3	AT26	M_CS_B_L3
M_DATA_B32	AR28	SB_DQ_32			
M_DATA_B33	AR29	SB_DQ_33			
M_DATA_B34	AL28	SB_DQ_34			
M_DATA_B35	AL29	SB_DQ_35	SB_CKE_0	AU16	M_CKE_B0
M_DATA_B36	AP28	SB_DQ_36	SB_CKE_1	AY15	M_CKE_B1
M_DATA_B37	AP29	SB_DQ_37	SB_CKE_2	AW15	M_CKE_B2
M_DATA_B38	AM28	SB_DQ_38	SB_CKE_3	AV15	M_CKE_B3
M_DATA_B39	AM29	SB_DQ_39			
M_DATA_B40	AP32	SB_DQ_40			
M_DATA_B41	AP31	SB_DQ_41			
M_DATA_B42	AP35	SB_DQ_42	SB_ODT_0	AL26	M_ODT_B0
M_DATA_B43	AP34	SB_DQ_43	SB_ODT_1	AP26	M_ODT_B1
M_DATA_B44	AR32	SB_DQ_44	SB_ODT_2	AM26	M_ODT_B2
M_DATA_B45	AR31	SB_DQ_45	SB_ODT_3	AK26	M_ODT_B3
M_DATA_B46	AR35	SB_DQ_46			
M_DATA_B47	AR34	SB_DQ_47			
M_DATA_B48	AM32	SB_DQ_48			
M_DATA_B52	AM31	SB_DQ_49	SB_CK_0	AL21	M_CLK_B_P0
M_DATA_B55	AL35	SB_DQ_50	SB_CK#_0	AL22	M_CLK_B_N0
M_DATA_B51	AL32	SB_DQ_51	SB_CK_1	AL20	M_CLK_B_P1
M_DATA_B54	AM34	SB_DQ_52	SB_CK#_1	AK20	M_CLK_B_N1
M_DATA_B49	AL31	SB_DQ_53	SB_CK_2	AL23	M_CLK_B_P2
M_DATA_B53	AM35	SB_DQ_54	SB_CK#_2	AM22	M_CLK_B_N2
M_DATA_B50	AL34	SB_DQ_55	SB_CK_3	AP21	M_CLK_B_P3
M_DATA_B56	AH35	SB_DQ_56	SB_CK#_3	AN21	M_CLK_B_N3
M_DATA_B57	AH34	SB_DQ_57			
M_DATA_B58	AE34	SB_DQ_58			
M_DATA_B59	AE35	SB_DQ_59			
M_DATA_B60	AJ35	SB_DQ_60			
M_DATA_B61	AJ34	SB_DQ_61			
M_DATA_B62	AF33	SB_DQ_62			
M_DATA_B63	AF35	SB_DQ_63			

110104 Move from CPU Part2 to CPU Part4.

SB_DIMM_DQVREF — AH1 — DIMM_DQ_CPU_VREF_B — DIMM_DQ_CPU_VREF_B 11
SB_DIMM_DQVREF — AH4 — DIMM_DQ_CPU_VREF_A — DIMM_DQ_CPU_VREF_A 11

C384 .1U-10VX-04 — GND
C379 .1U-10VX-04 — GND

M_DQS_B_P0	AH7	SB_DQS_0	SB_DQS_8	AN16	
M_DQS_B_P1	AM8	SB_DQS_1	SB_DQS#_8	AN15	
M_DQS_B_P2	AR8	SB_DQS_2			
M_DQS_B_P3	AN13	SB_DQS_3			
M_DQS_B_P4	AN29	SB_DQS_4	SB_ECC_CB_0	AL16	
M_DQS_B_P5	AP33	SB_DQS_5	SB_ECC_CB_1	AM16	
M_DQS_B_P6	AL33	SB_DQS_6	SB_ECC_CB_2	AP16	
M_DQS_B_P7	AG35	SB_DQS_7	SB_ECC_CB_3	AR16	
			SB_ECC_CB_4	AL15	
			SB_ECC_CB_5	AM15	
M_DQS_B_N0	AH6		SB_ECC_CB_6	AR15	
M_DQS_B_N1	AL8	SB_DQS#_0	SB_ECC_CB_7	AP15	
M_DQS_B_N2	AP8	SB_DQS#_1			
M_DQS_B_N3	AN12	SB_DQS#_2			
M_DQS_B_N4	AN28	SB_DQS#_3			
M_DQS_B_N5	AR33	SB_DQS#_4			
M_DQS_B_N6	AM33	SB_DQS#_5			
M_DQS_B_N7	AG34	SB_DQS#_6			
		SB_DQS#_7			

Desktop dosen't support ECC

DDR_1

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SKT_H2_CRB

110104 Update Pin Name. MHB CRB07.

Elitegroup Computer Systems

Title: CPU - DDR3

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MAX 112A
In +VCORE

CPU1F

BALLMAP
REV=1.7

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SKT_H2_CRB

MAX 112A
In +VCORE

110104
Update Pin Name. MHB CRB07.

1.05V/1.00V
MAX 8.5A
In +V_CPUVTT

CPU1G

BALLMAP
REV=1.7

POWER
7 OF 10

SKT_H2_CRB

20111024
Change footprint, so delete pins

110104
Update Pin Name. MHB CRB07.

0.925V/0.85V
MAX 8.8A
In +V_SA

1.8V
MAX 1A
In +V_1P8_SFR

1.5V
MAX 4.5A
In +V_1P5_SM

MAX 35A
In +VAXG

CPU1H

BALLMAP
REV=1.7

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SKT_H2_CRB

110104
Update Pin Name. MHB CRB07.

+VCORE
C238 22U-X5-08-O
C236 22U-X5-08-O
C237 22U-X5-08-O
C239 22U-X5-08-O
GND

PLACE NEAR SKT EDGE
OUTSIDE CAVITY.

+V_CPUVTT
C256 22U-X5-08
GND

+V_SA
C287 22U-X5-08
GND

PLACE NEAR SKT EDGE
OUTSIDE CAVITY.

+V_1P8_SFR
C354 .1U-10VX-02
C351 22U-X5-08
GND

20110915
Change value

+V_CPUVTT
C365 .1U-10VX-02
C347 .1U-10VX-02
C362 .1U-10VX-02
C283 .1U-10VX-02
C279 .1U-10VX-04
C350 .1U-10VX-02
C368 .1U-10VX-02
C371 .1U-10VX-02
C245 .1U-10VX-04
C246 .1U-10VX-02
C244 .1U-10VX-02
C265 .1U-10VX-02
C274 .1U-10VX-04
C268 .1U-10VX-02
C243 .1U-10VX-02
C322 .1U-10VX-04
GND

20110915
Change value

DECOUPLING & STITCHING CAPS.

+V_CPUVTT
SC34 22U-X5-08-X-O
SC26 22U-X5-08-X-O
SC35 22U-X5-08-X-O
SC25 22U-X5-08-X-O
SC19 22U-X5-08-X-O
SC36 22U-X5-08-X-O
GND

110301
Del 5 +V_CPUVTT MLCCs in BOTTOM Side by Power Team Suggest.

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY, BACKSIDE.

+V_CPUVTT
20110927
Change to reserve
C300 22U-X5-08
C312 22U-X5-08
C321 22U-X5-08
C332 22U-X5-08
SC331 22U-X5-08-X-O
C330 22U-X5-08
C343 22U-X5-08
C329 22U-X5-08
20110927
Delete C334
GND

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY.

+VAXG
C346 22U-X5-08
C320 22U-X5-08
C311 22U-X5-08
C336 22U-X5-08
C339 22U-X5-08
C358 22U-X5-08
GND
SC29 22U-X5-08-X-
SC22 22U-X5-08-X-O
SC23 22U-X5-08-X-O
SC21 22U-X5-08-X-
SC33 22U-X5-08-X-O
SC18 22U-X5-08-X-O
GND

20110831
Modify by power team's suggestion

20110831
Modify by power team's suggestion

+V_1P5_SM
C352 22U-X5-08
C359 22U-X5-08
C360 22U-X5-08
GND

+VCORE
C306 22U-X5-08
C307 22U-X5-08
C305 22U-X5-08
C301 22U-X5-08
C304 22U-X5-08
C309 22U-X5-08
C308 22U-X5-08
C601 22U-X5-08
C615 22U-X5-08
C639 22U-X5-08
C595 22U-X5-08
C593 22U-X5-08
SC9 22U-X5-08-X-
SC13 22U-X5-08-X-
SC12 22U-X5-08-X-
SC16 22U-X5-08-X-
SC15 22U-X5-08-X-
SC14 22U-X5-08-X-
SC11 22U-X5-08-X-
SC69 22U-X5-08-X-
SC70 22U-X5-08-X-
SC71 22U-X5-08-X-
SC72 22U-X5-08-X-
SC68 22U-X5-08-X-O
GND

20110831
Modify by power team's suggestion

PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY.

Elitegroup Computer Systems

Title: CPU - PWR

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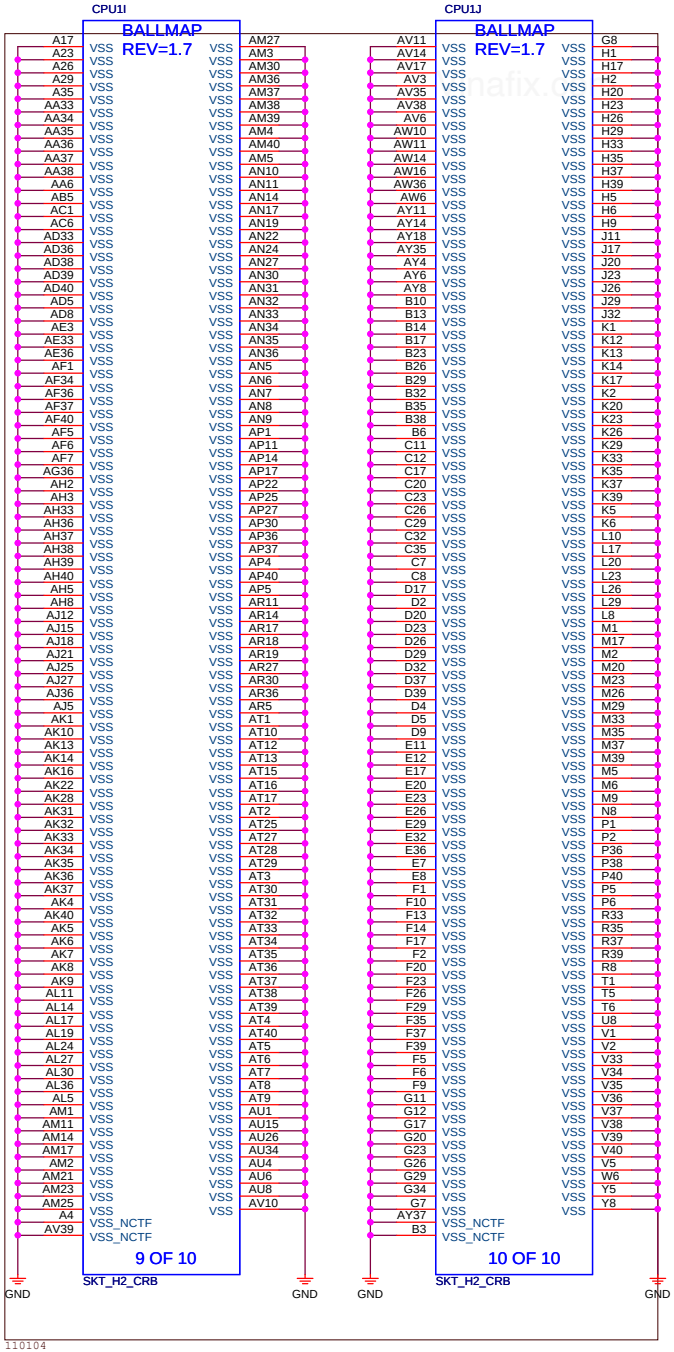
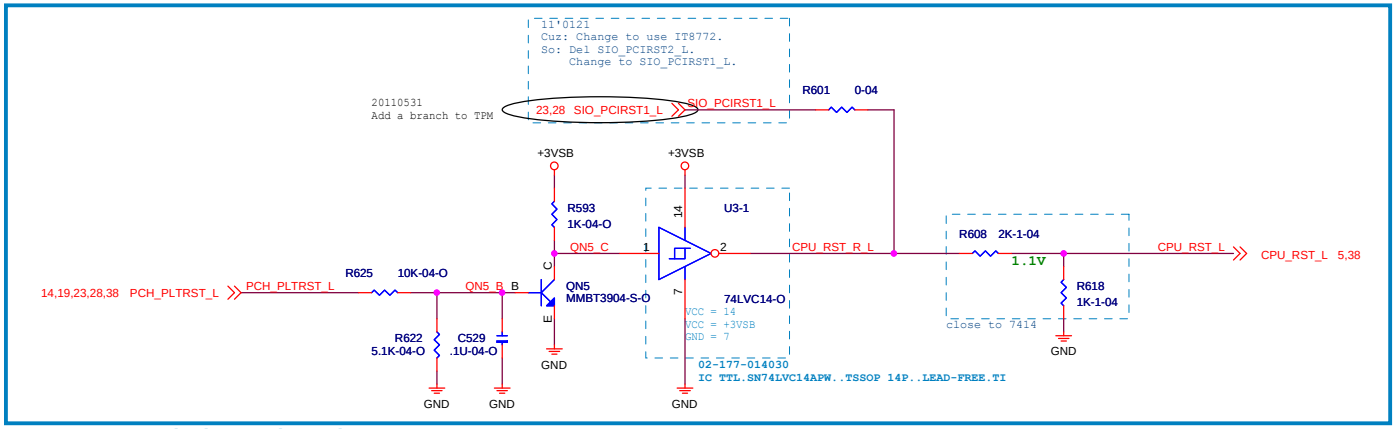
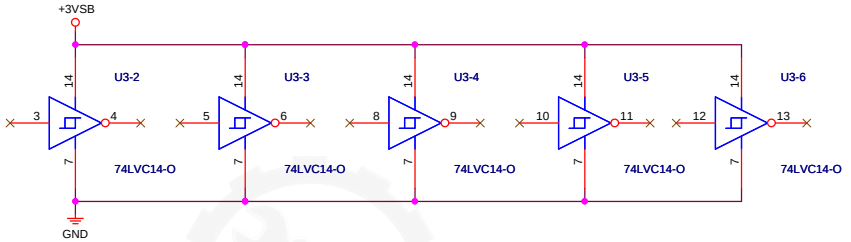


110104
Update Pin Name. MHB CRB07.



PLTRST_L Driving Circuit



CPU steel P/N

20-800-004611
SUBASSY.STEEL....LGA 1156P
W/BACK PLATE.ACA-ZIF-082-K01....LEAD-FREE(RoHS).LOTES

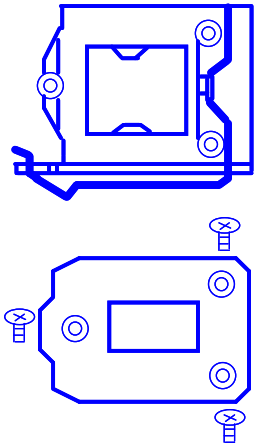
CPU1
CPU_SUBASSY_STEEL

20111101
Change material1

CPU socket P/N

11-018-115124
SOCKET.CPU..LGA 1155P SMD..G/F
BLACK.ACA-ZIF-096-P02....LEAD-FREE(RoHS/HF).LOTES

20111101
Change material1



Elitegroup Computer Systems

Title	CPU - GND, CPU_RST_L		
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DDR3 slot P/N

11-004-240101 DDR3 Gray KORTAK

11-004-240100 DDR3 White KORTAK

CHANNEL A DIMMs

M_DQS_A_P[0..7] M_DQS_A_P[0..7] 6

M_DQS_A_N[0..7] M_DQS_A_N[0..7] 6

M_DATA_A[0..63] M_DATA_A[0..63] 6

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

Desktop dosen't support ECC

DIMM1

DDR3-240P-GR

20110831 Change DIMM sequence

20110831 Change DIMM slot 20110914 Change value

6 M_ODT_A[0..3] M_ODT_A[0..3]

6 M_CS_A_L[0..3] M_CS_A_L[0..3]

6 M_CKE_A[0..3] M_CKE_A[0..3]

6 M_CLK_A_P[0..3] M_CLK_A_P[0..3]

6 M_CLK_A_N[0..3] M_CLK_A_N[0..3]

11 DIMM_VREF_CA_A DIMM_VREF_CA_A

11 DIMM_VREF_DQ_A DIMM_VREF_DQ_A

10,22,38 SMBCLK_MAIN SMBCLK_MAIN

10,22,38 SMBDATA_MAIN SMBDATA_MAIN

6 M_BS_A[0..2] M_BS_A[0..2]

M_MA_A[0..15] M_MA_A[0..15] 6

M_WE_A_L M_WE_A_L 6

M_RAS_A_L M_RAS_A_L 6

M_CAS_A_L M_CAS_A_L 6

DDR3_DRAMRST_L DDR3_DRAMRST_L 6,10

CH.A	SA1	SA0
DIMM0	L	L
DIMM1	L	H

+V_SM_VTT 0.75V MAX 1A

+V_1P5_SM 1.5V MAX 15A S3 1.0A

+VCC3

GND

DIMM2

DDR3-240P-W

20110831 Change DIMM sequence

20110902 Change DIMM slot 20110914 Change value

M_CLK_A_P2 M_CLK_A_P2

M_CLK_A_N2 M_CLK_A_N2

M_CLK_A_P3 M_CLK_A_P3

M_CLK_A_N3 M_CLK_A_N3

+V_1P5_SM +V_SM_VTT

C422 C424 C426 C423 C425 C488 C457

.1U-10VX-04 .1U-10VX-04 .1U-10VX-04 .1U-10VX-04 .1U-10VX-04 4.7U-X5-08 .1U-04

20110915 Change value

For CHAD1

+V_1P5_SM +V_SM_VTT

C473 C474 C402 C475 C476 C452 C455

22U-X5-08 22U-X5-08 22U-X5-08 22U-X5-08 22U-X5-08 4.7U-X5-08 .1U-04

For CHAD2

+VCC3

C495 C471

.1U-04-O .1U-04-O

PLACE BETWEEN CHA &CHB. DO NOT PUNCH VIA.

Elitegroup Computer Systems

Title: DDR3 - CHA DIMM0/1

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CHANNEL B DIMMs

M_DQS_B_P[0..7] M_DQS_B_P[0..7] 6
M_DQS_B_N[0..7] M_DQS_B_N[0..7] 6

M_DATA_B[0..63] M_DATA_B[0..63] 6

The processor memory controller does not have any DDR3 Data Mask (DM) signals for either channel. As a result the DM[8:0] pins of each DDR3 DIMM connector must be tied directly to ground.

Desktop dosen't support ECC

DIMM3 — DDR3-240P-GR

20110831 Change DIMM sequence
20110831 Change DIMM slot
20110914 Change value

6 M_ODT_B[0..3] M_ODT_B[0..3]
6 M_CS_B_L[0..3] M_CS_B_L[0..3]
6 M_CKE_B[0..3] M_CKE_B[0..3]
6 M_CLK_B_P[0..3] M_CLK_B_P[0..3]
6 M_CLK_B_N[0..3] M_CLK_B_N[0..3]

11 DIMM_VREF_CA_B
11 DIMM_VREF_DQ_B
9,22,38 SMBCLK_MAIN
9,22,38 SMBDATA_MAIN

6 M_BS_B[0..2] M_BS_B[0..2]

M_MA_B[0..15] M_MA_B[0..15] 6

M_WE_B_L M_WE_B_L 6
M_RAS_B_L M_RAS_B_L 6
M_CAS_B_L M_CAS_B_L 6
DDR3_DRAMRST_L DDR3_DRAMRST_L 6,9

CH.B	SA1	SA0
DIMM0	H	L
DIMM1	H	H

+V_SM_VTT 0.75V MAX 1A
+V_1P5_SM 1.5V MAX 15A S3 1.0A
+VCC3

DIMM4 — DDR3-240P-W

20110831 Change DIMM sequence
20110902 Change DIMM slot
20110914 Change value

M_CLK_B_P2
M_CLK_B_N2
M_CLK_B_P3
M_CLK_B_N3

STICHING CAPS FOR CMD, ADDR, CTL.BETWEEN CHBD1 & CHBD2

C497	C501	C511	C498	C554	C467	C468	C562	C558	C557	C553	C559	C555	C556
1U-6V3X-04	.1U-10VX-04	.1U-10VX-04	.1U-10VX-04	1U-6V3X-04	.1U-10VX-04	.1U-10VX-04	.1U-10VX-04	1U-6V3X-04	1U-6V3X-04	.1U-10VX-04	.1U-10VX-04	.1U-10VX-04	.1U-10VX-04

20110915 Change value

STICHING CAPS FOR CMD, ADDR, CTL.BELOW CHBD3.

C505	C503	C502	C549	C550	C551	C552	C561	C469	C470	C496	C512	C510
.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04	.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04-O	.1U-10VX-04-O

For CHBD1

C560	C399	C504	C509	C536	C544
.1U-10VX-04-O	1U-6V3X-04	.1U-10VX-04	.1U-10VX-04-O	4.7U-X5-08	.1U-04

For CHBD2

C507	C541
4.7U-X5-08	.1U-04

20110915 Change value
20110915 Change value

Elitegroup Computer Systems

Title: DDR3 - CHB DIMM0/1

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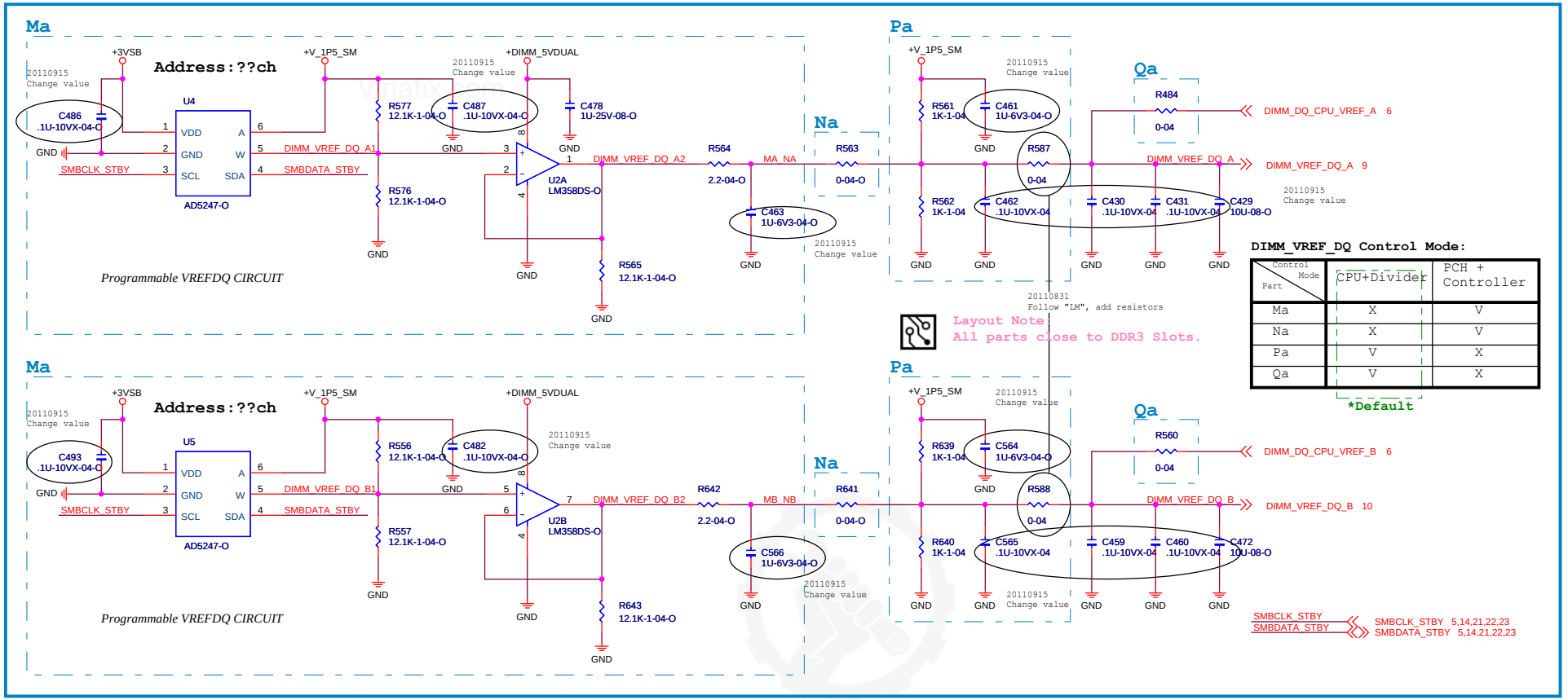
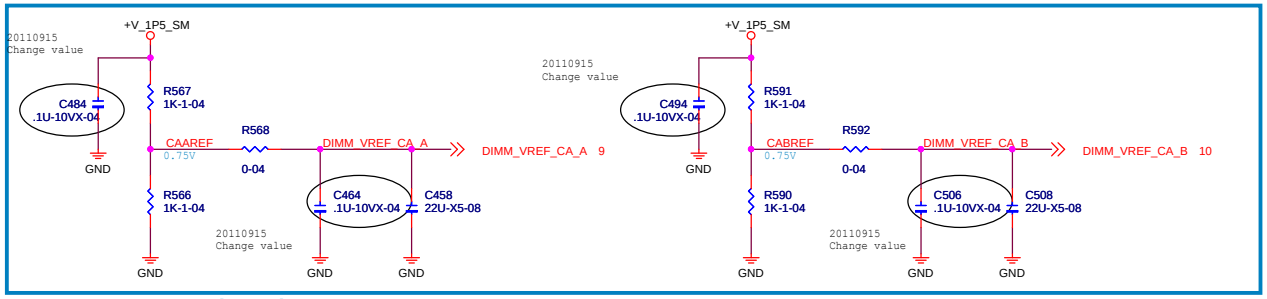
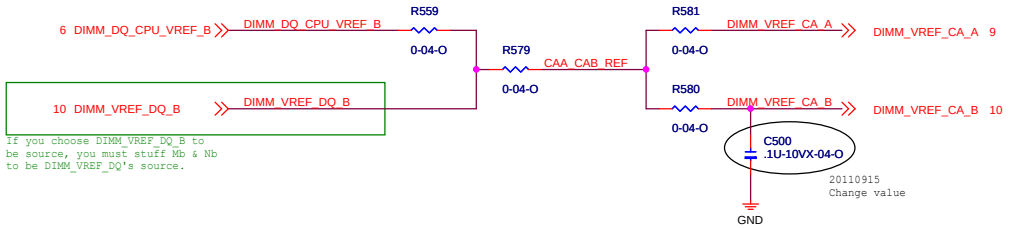


DIMM_VREF_DQ Control Circuit



DIMM_VREF_CA Circuit



Elitegroup Computer Systems

Title	DDR3 - VREF	
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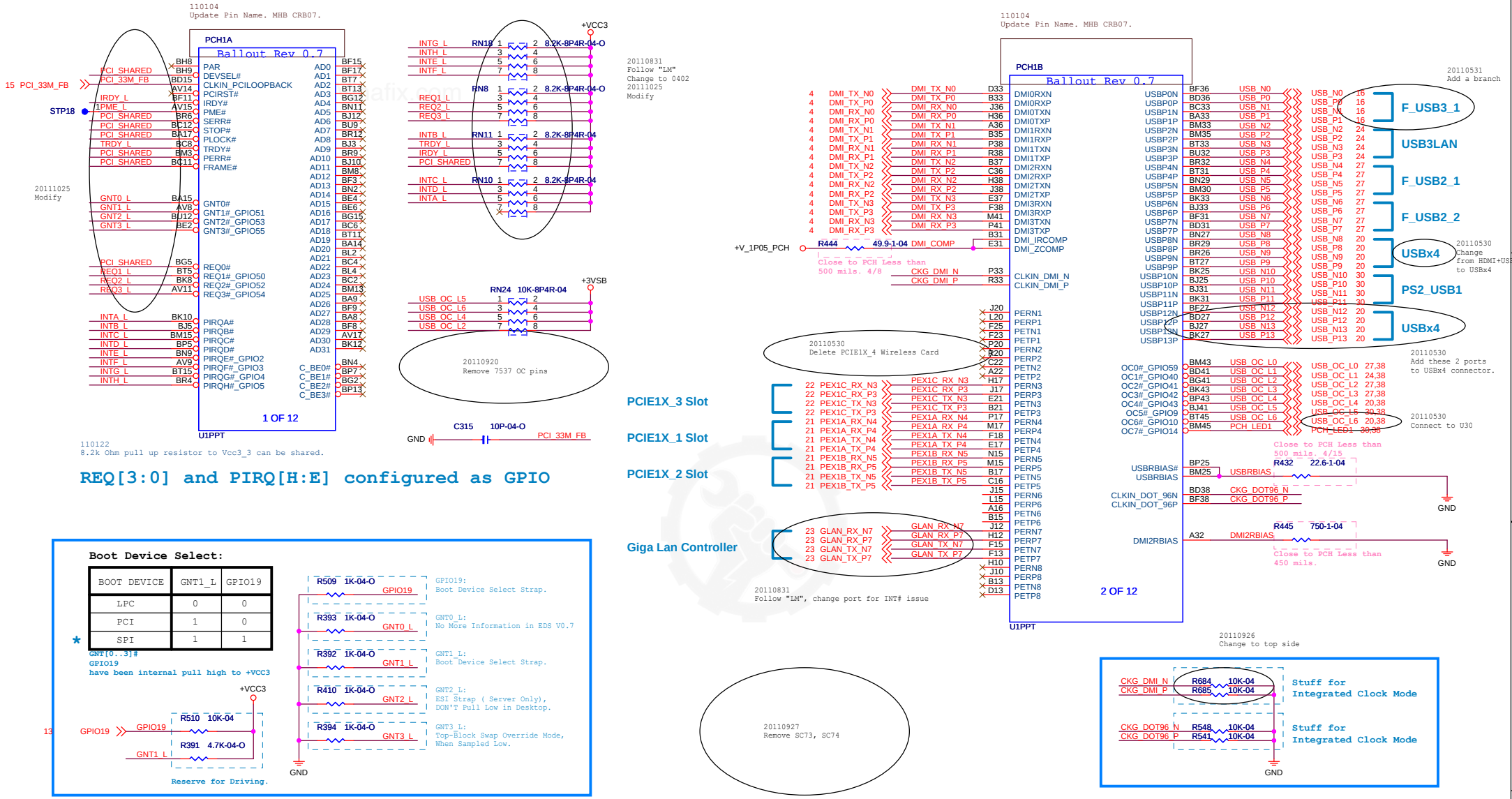

Function	INT port	PCI-E X1 port	Chipset
LAN Ethernet Controller	INTA#	PCI Express #7 Pin	Realtek RTL8111E
SATA Controller	INTB#	N/A	H77 intergrated

Elitegroup Computer Systems

Title: PCH - DMI/PCH-PE/USB

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110106
Update Pin Name. MHB CRB07.

MOBILE ONLY,
NOT FOR DESKTOP.

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0,
ALSO SUPPORT SATA2.0, SATA1.0.

PCH1C

Ballout Rev 0.7

STP13 1 PCH_CL_CLK1 BA50
STP12 1 PCH_CL_DATA1 BF50
STP14 1 PCH_CL_RST1_L BF49
14,22,28 PWRGD PWRGD R661 SPD-04 PCH_MEPWROK BC46

CL_CLK1
CL_DATA1
CL_RST1#
APWROK

BN21 PWM0
BT21 PWM1
BM20 PWM2
BN19 PWM3

GP17_BOMDET1 BT17
GP1_BOMDET2 BR19
GP6_BOMDET3 BA22
GP7_BOMDET4 BR16
TP_VGA BU16
BM18
PCH_GP70 BN17
PCH_GP71 BP15

TACH0_GPIO17
TACH1_GPIO1
TACH2_GPIO6
TACH3_GPIO7
TACH4_GPIO68
TACH5_GPIO69
TACH6_GPIO70
TACH7_GPIO71

20110831
Add GPIO for ICT test

20110526
Remove SW CLR_CMOS, add test point.
20110920
Remove TP, add pull high

BC43 SST

GPIO22 BA53
PCH_GP38 BE54
GPIO39 BF55
GPIO48 AW53

SCLOCK_GPIO22
SLOAD_GPIO38
SDATAOUT0_GPIO39
SDATAOUT1_GPIO48

20110902
Remove thermal header function

AY20 NC

SATA0RXN AC56 SATA3P0_RX_N0
SATA0RXP AB55 SATA3P0_RX_P0
SATA0TXN AE46 SATA3P0_TX_N0
SATA0TXP AE44 SATA3P0_TX_P0

SATA1RXN AA53 SATA3P0_RX_N1
SATA1RXP AA56 SATA3P0_RX_P1
SATA1TXN AG49 SATA3P0_TX_N1
SATA1TXP AG47 SATA3P0_TX_P1

SATA2RXN AL50 SATA2P0_RX_N2
SATA2RXP AL49 SATA2P0_RX_P2
SATA2TXN AL56 SATA2P0_TX_N2
SATA2TXP AL53 SATA2P0_TX_P2

SATA3RXN AN46 SATA2P0_RX_N3
SATA3RXP AN44 SATA2P0_RX_P3
SATA3TXN AN56 SATA2P0_TX_N3
SATA3TXP AM55 SATA2P0_TX_P3

SATA4RXN AN49 ESATA_RX_N4
SATA4RXP AN50 ESATA_RX_P4
SATA4TXN AT50 ESATA_TX_N4
SATA4TXP AT49 ESATA_TX_P4

SATA5RXN AT46
SATA5RXP AT44
SATA5TXN AV50
SATA5TXP AV49

CLKIN_SATA_N AF55 CKG_SATA_N
CLKIN_SATA_P AG56 CKG_SATA_P

SATALED# BF57 SATALED_L → SATALED_L 30
SATAICOMPI AJ55
SATAICOMPO AJ53 SATA1RCOMP R462 37.4-1-04 +V_1P05_PCH

20110601
Remove COM detect function.

SATA0GP_GPIO21 BC54 GPIO21
SATA1GP_GPIO19 AY52 GPIO19 → GPIO19 12
SATA2GP_GPIO36 BB55 GPIO36
SATA3GP_GPIO37 BG53 GPIO37
SATA4GP_GPIO16 AU56 GPIO16
SATA5GP_GPIO49 BA56 GPIO49

SATA3COMPI AE54
SATA3RCOMPO AE52 SATA3RCOMP R463 49.9-1-04 +V_1P05_PCH

TP16 AE50 PCH_TP16 1 STP11
SATA3RBIAS AC52 SATA3RBIAS R464 750-1-04 GND

A20GATE BB57 A20GATE → A20GATE 28
INIT3_3V# BN56 INIT3_3V_L
RCIN# BG56 KBRST_R_L
SERIRQ AV52 SER_IRQ → SER_IRQ 23,28
THRMTRIP# E56 CPU_THERMTRIP_L → CPU_THERMTRIP_L 5
PECI H48 PCH_PECI 1 STP20
PMSYNCH F55 PM_SYNC → PM_SYNC 5

20110531
Add a branch to TPM

3 OF 12

U1PPT

20110831
Add GPIO for ICT test

+VCC3
R434 4.7K-04
TP_VGA 1 TP_VGA

ICT test	
PCH GPIO68	
Low	On-board VGA
* High	PCIE*16

Default GPI set to Pull Up:

+VCC3

20110920
Add pull high for GPIO22
GPIO22 R429 10K-04

GP17_BOMDET1 R417 10K-04
GP1_BOMDET2 R423 10K-04
20110926
Change to top side
GP6_BOMDET3 R660 10K-04
GP7_BOMDET4 R415 10K-04

RN25 10K-8P4R-04
SATALED_L
20110902
Remove thermal header function
GPIO39
PCH_GP70
KBRST_L

RN26 10K-8P4R-04
PCH_GP71
20110601
Remove COM detect function.
A20GATE
GPIO21
PCH_GP38

RN27 10K-8P4R-04
GPIO16
20110902
Remove thermal header function
SER_IRQ
GPIO48
GPIO49

Layout SWAP needed

20110831
Change to 0402

GP17_BOMDET1 R418 10K-04-O
GP1_BOMDET2 R424 10K-04-O
GP6_BOMDET3 R598 10K-04-O
GP7_BOMDET4 R414 10K-04-O
INIT3_3V_L R461 1K-04-O
GND

20110926
Change to top side

CKG_SATA_N R585 10K-04
CKG_SATA_P R584 10K-04
GND

Stuff for
Integrated Clock Mode

GPIO36 R470 10K-04-O
GPIO37 R486 10K-04-O
110216
Follow CRB Reserve.
GND

Strapping

KBRST_R_L R373 0-04 KBRST_L → KBRST_L 28
C337 10P-04-O
GND

SATA1
SATA3P0_TX_P0 C491 .01U-04 SATA3P0_TX_C_P0
SATA3P0_TX_N0 C492 .01U-04 SATA3P0_TX_C_N0
SATA3P0_RX_N0 C515 .01U-04 SATA3P0_RX_C_N0
SATA3P0_RX_P0 C516 .01U-04 SATA3P0_RX_C_P0
TXP TXN RXN RXP GND
SATA-7P2R-GY
GND

20110526
Change SATA connectors of
H77H2-LM
20111027
Change footprint

20110830
Change to 2.0 conn.

SATA2
SATA3P0_TX_P1 C540 .01U-04 SATA3P0_TX_C_P1
SATA3P0_TX_N1 C539 .01U-04 SATA3P0_TX_C_N1
SATA3P0_RX_N1 C571 .01U-04 SATA3P0_RX_C_N1
SATA3P0_RX_P1 C570 .01U-04 SATA3P0_RX_C_P1
SATA-7P2R-GY
GND

20110830
Change to 2.0 conn.

SATA3
SATA2P0_TX_P2 C489 .01U-04 SATA2P0_TX_C_P2
SATA2P0_TX_N2 C490 .01U-04 SATA2P0_TX_C_N2
SATA2P0_RX_N2 C513 .01U-04 SATA2P0_RX_C_N2
SATA2P0_RX_P2 C514 .01U-04 SATA2P0_RX_C_P2
SATA-7P2R-W
GND

SATA4
SATA2P0_TX_P3 C532 .01U-04 SATA2P0_TX_C_P3
SATA2P0_TX_N3 C533 .01U-04 SATA2P0_TX_C_N3
SATA2P0_RX_N3 C563 .01U-04 SATA2P0_RX_C_N3
SATA2P0_RX_P3 C583 .01U-04 SATA2P0_RX_C_P3
SATA-7P2R-W
GND

ESATA
ESATA_TX_P4 C537 .01U-04 ESATA_TX_C_P4
ESATA_TX_N4 C568 .01U-04 ESATA_TX_C_N4
ESATA_RX_N4 C538 .01U-04 ESATA_RX_C_N4
ESATA_RX_P4 C569 .01U-04 ESATA_RX_C_P4
SATA-7P2R-BK
GND

Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω ±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%

Elitegroup Computer Systems

Title	PCH - SATA, SATA CONN	
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110106
Update Pin Name. MHB CRB07.

20110531
Add branches to TPM

20110531
Add a branch to TPM

PCH1D

Ballout Rev 0.7

19,23,28 LPC_AD[0..3] LPC_AD[0..3]
LPC_FRAME_L
LPC_DRQ0_L
LPC_DRQ1_L
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LDRQ0#
LDRQ1#_GPIO23
FWH0_LAD0
FWH1_LAD1
FWH2_LAD2
FWH3_LAD3
FWH4_LFRAME#

20110915
Change value
C333 .1U-10VX-04-O GND

25 HDA_BITCLK HDA_BITCLK R425 33-04 HDA_BITCLK_R
25 HDA_RST_L HDA_RST# R659 33-04 HDA_RST_R_L
HDA_SDIN0 25 HDA_SDIN0

20110926
Change to top side
15 HDA_SDOUT_R HDA_SDOUT_R
HDA_SDOUT R431 33-04
25 HDA_SYNC HDA_SYNC R427 33-04 HDA_SYNC_R

HDA_BCLK
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_SYNC

22 SPI_MOSI SPI_MOSI
22 SPI_MISO SPI_MISO
22 SPI_CS_L0 SPI_CS0#
22 SPI_CLK SPI_CLK
SPI_CS1#

PCH_RTCX1
PCH_RTCX2
RTCRST_L
SRTCRST_L
INTRUDER_L
PWRGD
RSMRST_L
INTVRMEN
DPWROK
DSWODVREN
28,38 DPWROK

RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
PWROK
RSMRST#
INTVRMEN
DPWROK
DSWVRMEN

15 RTCRST_L
15 SRTCRST_L
13,22,28 PWRGD

SMBALERT_L
SMBCLK_STBY_R
SMBDATA_STBY_R
SMLOALERT_L
SMLK0_LAN_CLK
SMLK0_LAN_DATA
SMLK1ALERT_L
SMLK1_SIO_CLK
SMLK1_SIO_DATA
28 SMLK1_SIO_CLK
28 SMLK1_SIO_DATA

SMBALERT#_GPIO11
SMBCLK
SMBDATA
SML0ALERT#_GPIO60
SML0CLK
SML0DATA
SML1ALERT#_PCHHOT#_GPIO74
SML1CLK_GPIO58
SML1DATA_GPIO75

C335 .1U-10VX-04-O GND DPWROK
20110915
Change value

4 OF 12

U1PPT

BMBUSY#_GPIO0
CLKRUN#_GPIO32
HDA_DOCK_EN#_GPIO33
STP_PCI#_GPIO34
GPIO35/NMI#
GPIO8
LAN_PHY_PWR_CTRL_GPIO12
HDA_DOCK_RST#_GPIO13
GPIO15
GPIO24_MEM_LED
GPIO28
SLP_LAN#_GPIO29
PCIECLKRQ2#/GPIO20/SMI#
PCIECLKRQ5#_GPIO44
PCIECLKRQ6#_GPIO45
PCIECLKRQ7#_GPIO46
GPIO57
SYS_PWROK
RI#
PLTRST#
WAKE#
SLP_A#
SLP_S3#
SLP_S4#
SLP_S5#_GPIO63
SUS_STAT#_GPIO61
SUSCLK_GPIO62
BATLOW#_GPIO72
SUSACK#
SUSWARN#/SUSPWRDNACK/GPIO30
DRAMPWROK
GPIO27
GPIO31
SLP_SUS#
PWRBTN#
SYS_RESET#
SPKR
PROCPWRGD
TP12
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_TMS

AW55 GPIO0
BC56 CLKRUN_L 1 TP16
BC25 HDA_DOCK_EN_L 1 STP5
BL56 GPIO34
BJ57 TP_GPIO35 1 STP19
BP51 IGC_EN_L
BK50 PCH_GP12
BA25 LPC_PME_L LPC_PME_L 28
BM55 TLS_EN
BP53 PCH_SKTOCC_L
BJ55 ON_DIE_PLL_EN
BH49 SLP_LAN_L 1 STP21
AV43 PCH_GP20_PU
BL54 PCH_GP44
AV44 PCH_GP45
BP55 PCH_GP46
BT53 GP57_5V_DETECT
BJ53 PCH_SYSPWROK
BJ48 PCH_RI_L PCH_RI_L 29
BK48 PCH_PLTRST_L PCH_PLTRST_L 8,19,23,28,38
BC44 PCIE_WAKE_L PCIE_WAKE_L 21,22,23
BC41 SLPAMT_L
BM53 SLP3_L SLP3_L 5,20,24,27,28,30,32,33,34
BN52 SLP4_L SLP4_L 28,30,33
BH50 SLP5_L 1 STP37
BN54 GPIO61 1 STP38
BA47 SUSCLK 1 STP10
AV46 GPIO72_BOMDET5
BP45 SUSACK_L SUSACK_L 28
BU46 SUSWARN_L SUSWARN_L 28
BG46 DRAM_PWROK DRAM_PWROK 5
BJ43 PCH_GP27
BG43 PCH_GP31
BD43 SLP_SUS_L SLP_SUS_L 31
BT43 SIO_PWRBTN_L SIO_PWRBTN_L 28,38
BE52 FP_RST_L FP_RST_L 5,30,38
BE56 PCH_SPKR PCH_SPKR 25,30
D53 CPU_PWROK CPU_PWROK 5,38
BC49 PCH_JTAG_RST_R PCH_JTAG_RST_R 38
BA43 PCH_JTAG_TCK_R PCH_JTAG_TCK_R 38
BC52 PCH_JTAG_TDI PCH_JTAG_TDI 38
BF47 PCH_JTAG_TDO PCH_JTAG_TDO 38
BC50 PCH_JTAG_TMS PCH_JTAG_TMS 38

110121
Cuz: Change to use RTL8111E-VL.
So: Change Net SLP_LAN_L to STP21.

20110530
Remove WLAN_DIS_L function, rename to PCH_GP45

20111026
Add STP
20111027
Change to bot

110121
Cuz: Change to use SIO+Intel EuP Solution.
So: Del PCH_GP30.
Add SUSACK_L, SUSWARN_L, SLP_SUS_L.

110128
Cuz: Add G3->S5 WOL Function.
So: DEL FP_PWRBTN_L.
Add PCH_PWRBTN_L

20110825
Add XDP

20110530
Remove WLAN_DIS_L function, rename to PCH_GP45

5,11,21,22,23 SMBDATA_STBY R473 0-04 SMBDATA_STBY_R C417 1U-6V3X-04-O GND
5,11,21,22,23 SMBCLK_STBY R457 0-04 SMBCLK_STBY_R C409 1U-6V3X-04-O GND

20110926
Change to top side
+3VSB
PCH_GP12 R502 10K-04-O
GPIO72_BOMDET5 R494 10K-04
SMLK0_LAN_CLK R55 2.2K-04
SMLK0_LAN_DATA R33 2.2K-04
SMLK1_SIO_CLK R32 2.2K-04
SMLK1_SIO_DATA R16 2.2K-04
PCIE_WAKE_L R483 1K-04
PCH_GP45 R496 10K-04
GP57_5V_DETECT R672 10K-04
PCH_RI_L R671 10K-04
SMBALERT_L R475 10K-04
SMLOALERT_L R458 2.2K-04
SML1ALERT_L R455 10K-04

110418
SR11 Change to Stuff.
110215
Cuz: Change to use SIO+Intel EuP Solution.
So: PCH_GP27, PCH_GP31 tie to +PS_3VSB.
+PS_3VSB
PCH_GP27 R499 8.2K-04
PCH_GP31 R500 10K-04

+V_1P5_SM
DRAM_PWROK R750 200-04

+VCC3
GPIO34 R469 10K-04
PCH_GP20_PU R675 10K-04
GPIO0 R493 10K-04

Internal Pull Up:
LPC_DRQ1_L R636 10K-04-O
LPC_DRQ0_L R416 10K-04-O

+RTCVCC
DSWODVREN Hi For All Products.
DSWODVREN R450 390K-04
INTRUDER_L R447 1M-04
110218 Del Case Open, Only Pull High.
GPIO72_BOMDET5 R505 10K-04-O
PCH_GP20_PU R673 10K-04-O
PCH_GP45 R495 10K-04-O
GP57_5V_DETECT R676 10K-04-O
PCH_JTAG_RST_R R678 10K-04-O
GND

20110530
Remove WLAN_DIS_L function, rename to PCH_GP45

20110926
Change to top side
R56 0-04-O GND
PWRGD C159 .1U-10VX-04-O GND
IGC_EN_L R459 1K-04-O GND
20110915
Change value
20110927

When Deep Sleep not implemented:

1.PCH_GP31, PCH_GP27 need to be Pull Up +3VSB.
2.VCCDSW3_3 should to be connected to +3VSB.
3.SLP_SUS_L, SUSACK_L left unconnected.
4.SUSWARN_L may be used as GPIO30.(Referance to 1.)

PCH_RTCX1
PCH_RTCX2
R453 10M
X4 X-32.768K 20PPM X4(wire)
C403 15P-04 C404 15P-04 JP-WI-P6.25
GND
SZ-146-327624
XTAL.32.768KHZ.20ppm.12.5pF.FUJICOM

20110830
Change crystal footprint,
and change frome holder to wire

Reserve for Debug
+3VSB
R482 10K-04-O
R488 0-04
PCH_SYSPWROK
VR_READY 5,36,38
C433 22U-6V3-08-O
R489 10K-04-O
GND GND

5,36 H_SKTOCC_L H_SKTOCC_L
PCH_SKTOCC_L
R491 1K-04
R490 10K-04-O
R487 0-04-O
PWRGD
MN1 QN7002-T1B-AT-S
GND GND
For Power Test
without CPU.

In Sugar Bay Q series Platform,
Enable TLS for vPro.
+3VSB
TLS_EN R477 1K-04-O

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

Without TLS
no AMT, RCFG(remote Config), or RPAT.

+RTCVCC
INTVRMEN R449 390K-04
R451 1K-04-O
GND

Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

+3VSB
PCH_GP44 R478 10K-04
R468 10K-04-O
GND

DFX TEST MODE Rings Oscillator:

PCH_GP44 (internal PU)	
H	Enable
L	Bypass

+VCC3
PCH_SPKR R756 1K-04-O

No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

+3VSB
PCH_GP46 R476 10K-04
R460 10K-04-O
GND

JTAG CLK FILTER:

PCH_GP46 (internal PU)	
H	Enable
L	Bypass

+3VSB
ON_DIE_PLL_EN R481 10K-04
R480 1K-04-O
GND

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

R485 1K-04-O +3VSB
R428 1K-04-O
HDA_SYNC_R
GND

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

110210
Del MEPWROK & PWROK Selection Circuit

+3VSB
+5VSB
R503 39.2K-1-04-O
RSMRST_FB
R527 7.87K-1-04-O
C445 1U-6V3X-04-O
R504 4.7K-04-O
RSMRST_FCB
QN6 MMBT3904-S-O
QN7 MMBT3904-S-O
R517 10K-04
RSMRST_L
RSMRST_L 28,38
C437 .1U-10VX-04-O
20110915
Change value
GND

RSMRST Reserve Circuit
1)AC ON: 3VSB vs RSMRST(t204: min 10ms)
2)AC OFF: 3VSB>2.9V when RSMRST<0.8V

ME_TEST
+PS_3VSB
+3VSB
SLP3_L
SLP4_L
SLPAMT_L
H3X2-B-O GND

PS_3VSB	SLP3_L
3VSB	SLP4_L
SLPA_L	GND

ME Test Header
Layout Note:Print this table near ME_TEST

Elitegroup Computer Systems

Title: PCH - MISC, Strap Function

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PCH1H

Ballout Rev 0.7

20111006
Change value ("LM" SI issue)

28 SIO33M — SIO33M — R374 47-04 — SIO33M_R — AT11

12 PCI_33M_FB — PCI_33M_FB — R378 22-04 — PCI_33M_FB_R — AN14

20110531
Add this clock for TPM

23 TPM33M — TPM33M — R381 22-04 — TPM33M_R — AT12

20111006
Change value ("LM" SI issue)

28 SIO48M — SIO48M — R376 47-04 — SIO48M_R — AT17

PDG 0.7 33 ohm 5% for Single-End (except PCI Clocks)

19 LDG33M — LDG33M — R377 22-04 — LDG33M_R — AT14

XCLK_RCOMP — AL2

CKG_14M — AN8

XTAL_25M_PCH_OUT — AJ5

XTAL_25M_PCH_IN — AJ3

R360 1M-1

X2 X-25M-30m20D

C277 27P-04

C291 27P-04

GND

07-135-250036
XTAL.25MHZ.30ppm.20pF

CLKOUT_PCI0	AT11	CLKIN_GND1_N	R27 CLK_IN_N
CLKOUT_PCI1	AN14	CLKIN_GND1_P	P27 CLK_IN_P
CLKOUT_PCI2	AT12	CLKIN_GND0_N	W53 CK_PD_N
CLKOUT_PCI3	AT17	CLKIN_GND0_P	V52 CK_PD_P
CLKOUT_PCI4	AT14	CLKOUT_ITPXDP_N	R52 XDP_CPU_CLK_DN → XDP_CPU_CLK_DN 38
CLKOUTFLEX0_GPIO64	BA5	CLKOUT_ITPXDP_P	N52 XDP_CPU_CLK_DP → XDP_CPU_CLK_DP 38
CLKOUTFLEX1_GPIO65	AW5	CLKOUT_PCIE7N	AE2 XDP_PCH_CLK_DN → XDP_PCH_CLK_DN 38
CLKOUTFLEX2_GPIO66	BA2	CLKOUT_PCIE7P	AF1 XDP_PCH_CLK_DP → XDP_PCH_CLK_DP 38
CLKOUTFLEX3_GPIO67		CLKOUT_DMI_N	P31 CK_CPU_100M_N → CK_CPU_100M_N 5
XCLK_RCOMP		CLKOUT_DMI_P	R31 CK_CPU_100M_P → CK_CPU_100M_P 5
REFCLK14IN		CLKOUT_DP_N	N56
XTAL25_OUT		CLKOUT_DP_P	M55
XTAL25_IN		CLKOUT_PCIE0N	AE6 PEX1B_100M_N → PEX1B_100M_N 21
		CLKOUT_PCIE0P	AC6 PEX1B_100M_P → PEX1B_100M_P 21
		CLKOUT_PCIE1N	AA5
		CLKOUT_PCIE1P	W5
		CLKOUT_PCIE2N	AB12 GLAN_CLK_N → GLAN_CLK_N 23
		CLKOUT_PCIE2P	AB14 GLAN_CLK_P → GLAN_CLK_P 23
		CLKOUT_PCIE3N	AB9
		CLKOUT_PCIE3P	AB8
		CLKOUT_PCIE4N	Y9 PEX1C_100M_N → PEX1C_100M_N 22
		CLKOUT_PCIE4P	Y8 PEX1C_100M_P → PEX1C_100M_P 22
		CLKOUT_PCIE5N	AF3 PEX1A_100M_N → PEX1A_100M_N 21
		CLKOUT_PCIE5P	AG2 PEX1A_100M_P → PEX1A_100M_P 21
		CLKOUT_PCIE6N	AB3
		CLKOUT_PCIE6P	AA2
		CLKOUT_PEG_A_N	AG8 PEX16_100M_N → PEX16_100M_N 21
		CLKOUT_PEG_A_P	AG9 PEX16_100M_P → PEX16_100M_P 21
		CLKOUT_PEG_B_N	AE12
		CLKOUT_PEG_B_P	AE11

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U1PPT

20110825
Add XDP

20110530
Delete PCIE1X_4 Wireless Card

+V_1P05_PCH — 20110926 Change to top side

R382 90.9-1-04 — XCLK_RCOMP

C338 10P-04-O SIO33M_R

C342 10P-04-O PCI_33M_FB_R

C349 10P-04-O TPM33M_R

C341 120P-04 LDG33M_R

C340 10P-04-O SIO48M_R

GND

20110909
Add Cap.

CK_PD_P R466 10K-04

CK_PD_N R465 10K-04

CLK_IN_P R682 10K-04

CLK_IN_N R681 10K-04

CKG_14M R680 10K-04

20110926
Change to top side

Stuff for Integrated Clock Mode

GND

+VCC3 — C302 .1U-04-O For HDA_BITCLK — GND

C348 .1U-04-O For PCH_RTCX1/2

EMI CAPS.

+V_1P05_PCH — C421 .1U-04-O

+VCC3 — C432 .1U-04-O — GND

20110927
Change to top

STITCHING CAPS.

+RTCVCC

D6 BAT54C-S

R_VBAT

+PS_3VSB

R365 1K-04

+VBAT

BT1 SK-CR2032-D

BT1 GND

20110901
Add +RTCVCC_SIO

+RTCVCC_SIO

20110909
Change reference

CLR_CMOS

H3X1-R

R188 20K-04

HCM_P3

RTCRST_L 14

R366 4.7K-04

C434 1U-16VX X7R

20110915
Change value

GND GND

110415
Update RTCRST_L Circuit.
Follow SIO Schematic Checklist V1.7.

20110909
Change reference

CLR_CMOS(1-2)

JP-R

CLR_CMOS_HW	CLEAR_CMOS
1-2	NORMAL
2-3	CLEAR CMOS

*

+ KTS LITHIUM BATTERY CD2032 CR2032

20111031
Fix reference and value

HW Clear CMOS Header

20110526
Remove SW CLR_CMOS

SW Clear CMOS Header

+RTCVCC

R226 20K-1-04

SRTCRST_L → SRTCRST_L 14

C210 1U-16VX

20110915
Change value

GND

For ME Reset.

20110530
Change to 2 pin header

+3VSB

R277 1K-04

ME_UNLOCK

ME_UN_PU

HDA_SDOUT_R → HDA_SDOUT_R 14

H2X1-BK

ME Enable/Disable

	ME_UNLOCK
1-2	UNLOCK
Float	LOCK

Disable ME Header,
Always Stuff for ME or
non-ME Platform.

Elitegroup Computer Systems

Title: PCH - CLK IO, CKG - IDT4180

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110106
Update Pin Name. MHB CRB07.

PCH1E
Ballout Rev 0.7

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U1PPT

20110913
Change value and footprint
20110923
SWAP
20111031
Unstuff

110106
Update Pin Name. MHB CRB07.

PCH1G
Ballout Rev 0.7

7 OF 12

U1PPT

20110901
Delete intersheet

20111019
Modify circuit

20111028
Add stitching cap.

FOR CHOKE OPTION

20111031
For choke option

USB3.0 TYPE-A CONNECTOR EMI

20110915
Change value

20110914
Delete 0 ohm res.

20110923
SWAP

20110913
Change footprint

20110901
Change value
20111031
Unstuff

USB3.0 TYPE-A CONNECTOR ESD Circuit

20111017
Change to reserve

USB3.0 TYPE-A CONNECTOR & HEADER

20110901
Modify USB3.0 circuit

10-094-009080
CONN.USB(3.0) A-TYPE..9P 180D DIP
UEA0112C-4FH1-4F....LEAD-FREE.FOXCONN

20110906
Change footprint
20111006
unstuff

Elitegroup Computer Systems

Title	PCH - FDI, CLR_CMOS	
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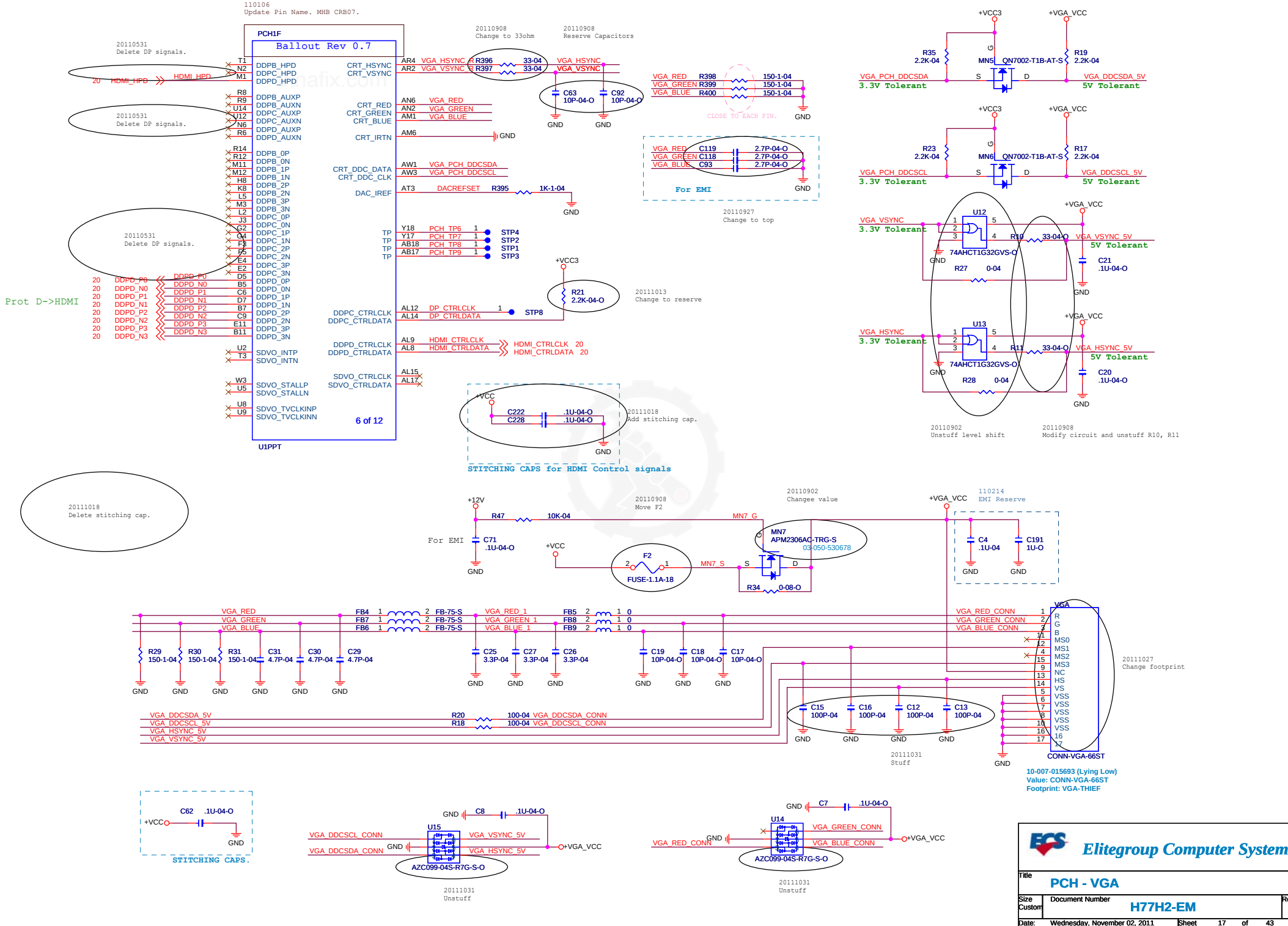
110106
Update Pin Name. MHB CRB07.
PCH1F
Ballout Rev 0.7
6 of 12
U1PPT
20110531
Delete DP signals.
HDMI_HPD
DDPB_HPD
DDPC_HPD
DDPD_HPD
DDPB_AUXP
DDPB_AUXN
DDPC_AUXP
DDPC_AUXN
DDPD_AUXP
DDPD_AUXN
DDPB_0P
DDPB_0N
DDPB_1P
DDPB_1N
DDPB_2P
DDPB_2N
DDPB_3P
DDPB_3N
DDPC_0P
DDPC_0N
DDPC_1P
DDPC_1N
DDPC_2P
DDPC_2N
DDPC_3P
DDPC_3N
DDPD_0P
DDPD_0N
DDPD_1P
DDPD_1N
DDPD_2P
DDPD_2N
DDPD_3P
DDPD_3N
SDVO_INTP
SDVO_INTN
SDVO_STALLP
SDVO_STALLN
SDVO_TVCLKINP
SDVO_TVCLKINN
CRT_HSYNC
CRT_VSYNC
CRT_RED
CRT_GREEN
CRT_BLUE
CRT_IRTN
CRT_DDC_DATA
CRT_DDC_CLK
DAC_IREF
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPD_CTRLCLK
DDPD_CTRLDATA
SDVO_CTRLCLK
SDVO_CTRLDATA
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
VGA_PCH_DDCSDA
VGA_PCH_DDCSCL
DACREFSET
R395 1K-1-04
PCH_TP6
PCH_TP7
PCH_TP8
PCH_TP9
STP4
STP2
STP1
STP3
DP_CTRLCLK
DP_CTRLDATA
STP8
HDMI_CTRLCLK
HDMI_CTRLDATA
Prot D->HDMI
20110908
Change to 33ohm
20110908
Reserve Capacitors
R396 33-04
R397 33-04
C63 10P-04-O
C92 10P-04-O
R398 150-1-04
R399 150-1-04
R400 150-1-04
CLOSE TO EACH PIN.
C119 2.7P-04-O
C118 2.7P-04-O
C93 2.7P-04-O
For EMI
20110927
Change to top
+VCC3
R21 2.2K-04-O
20111013
Change to reserve
C222 .1U-04-O
C228 .1U-04-O
20111018
Add stitching cap.
STITCHING CAPS for HDMI Control signals
20111018
Delete stitching cap.
R35 2.2K-04
R19 2.2K-04
MN5 QN7002-T1B-AT-S
VGA_PCH_DDCSDA
VGA_DDCSDA_5V
3.3V Tolerant
5V Tolerant
R23 2.2K-04
R17 2.2K-04
MN6 QN7002-T1B-AT-S
VGA_PCH_DDCSCL
VGA_DDCSCL_5V
U12
U13
74AHCT1G32GVS-O
R27 0-04
R28 0-04
R10 33-04-O
R11 33-04-O
VGA_VSYNC_5V
VGA_HSYNC_5V
C21 .1U-04-O
C20 .1U-04-O
20110902
Unstuff level shift
20110908
Modify circuit and unstuff R10, R11
+12V
R47 10K-04
MN7_G
MN7_S
MN7
APM2306AC-TRG-S
03-050-530678
R34 0-08-O
F2
FUSE-1.1A-18
For EMI
C71 .1U-04-O
20110902
Changee value
20110908
Move F2
110214
EMI Reserve
C4 .1U-04
C191 1U-O
FB4 FB-75-S
FB7 FB-75-S
FB6 FB-75-S
FB5 FB-75-S
FB8 FB-75-S
FB9 FB-75-S
R29 150-1-04
R30 150-1-04
R31 150-1-04
C31 4.7P-04
C30 4.7P-04
C29 4.7P-04
C25 3.3P-04
C27 3.3P-04
C26 3.3P-04
C19 10P-04-O
C18 10P-04-O
C17 10P-04-O
VGA_RED_CONN
VGA_GREEN_CONN
VGA_BLUE_CONN
VGA_DDCSDA_CONN
VGA_DDCSCL_CONN
R20 100-04
R18 100-04
C15 100P-04
C16 100P-04
C12 100P-04
C13 100P-04
VGA
R
G
B
MS0
MS1
MS2
MS3
NC
HS
VS
VSS
CONN-VGA-66ST
20111027
Change footprint
20111031
Stuff
10-007-015693 (Lying Low)
Value: CONN-VGA-66ST
Footprint: VGA-THIEF
C62 .1U-04-O
STITCHING CAPS.
U15
C8 .1U-04-O
AZC099-04S-R7G-S-O
20111031
Unstuff
U14
C7 .1U-04-O
20111031
Unstuff
Elitegroup Computer Systems
Title
PCH - VGA
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110106
Update Pin Name. MHB CRB07.

PCH1J
Ballout Rev 0.7

MAX <1mA
+V_REF5V
BF1 V5REF
MAX <1mA
+V_REF5V_SUS
BT25 V5REF_SUS
+3VSB
MAX 10mA
AV28 VCCSUSHDA
+VCC3
MAX 203mA
AU20 VCC3_3
AV20 VCC3_3
AU22 VCC3_3
3.3V
MAX 16mA
+VCC3
AN52 VCCSPI
C416 1U-16VX Close to AN52
C314 4.7U-X5-08
SC39 1U-16VX-X-O
SC43 1U-6V3X-04-X-O Close to AN52
20110915 Change value
20110902 Change to X5
20110915 Change value
20110927 Change to reserve
100 mA +V_3P3_DAC AT1 VCCADAC
100 mA +VCCA_DPLLA AB1 VCCADPLLA
100 mA +VCCA_DPLLB AC2 VCCADPLLB
+3VSB
Place Near ends of Power Corridor
SC55 2.2U-10VX-X-O Close to AY30, AT40
SC51 .1U-10VX-04-X-O Close to AY30
20110927 Change to reserve
20110915 Change value
GND
USB Classic Filter
+5VSB +3VSB
D3 BAT54C-S
R439 10-04
+V_REF5V_SUS
C389 .1U-X7R
C388 .1U-10VX-04 Close to BF35
20110915 Change value
GND GND
+VCC +VCC3
D4 BAT54C-S
R346 10-04
+V_REF5V
C280 .1U-X7R
C356 1U-6V3X-04 Close to BF1
GND GND
+V_1P05_PCH
PFB1 IND-10U-08 125 mA
R348 0-04
+VCCA_DPLLA_R +VCCA_DPLLA
EC40 220U-16D6.3H11E
C275 1U-6V3X-04 Close to AB1
PFB2 IND-10U-08 125 mA
R351 0-04
+VCCA_DPLLB_R +VCCA_DPLLB
EC45 220U-16D6.3H11E
C276 1U-6V3X-04 Close to AC2
PFB3 IND-10U-08 125 mA
R354 0-04
+V_1P05_PCH_SRC_R +V_1P05_PCH_SRC
C289 10U-X5-08
C284 1U-6V3X-04-O Close to AJ20
GND
+VCC3
PFB4 FB600-06 200 mA
R347 1-04
+V_3P3_DAC_R +V_3P3_DAC
C270 1U-6V3-04-O
EC37 220U-16D5H7E-O
C627 10U-X5-08-O
C319 10U-X5-08
C313 .1U-10VX-04
20110915 Change value
GND
20111011
Follow "LM", for VGA noise
11'0321
Stuff C319.
C313 Change to .1U-X7-04
follow Lenovo IPG Desktop Design Control Checklist rev1.2.

VCCVRM_A AJ1
VCCVRM_B R2
VCCVRM_C R54
VCCVRM R56
+V_1P8_SFR
VCCDFTERM T55 T57
C412 .1U-10VX-04 Close to T57
20110915 Change value
VCC3_3 AL38 AN38 BC17 BD17 BD20 A12 AF57 BT35 AV30 AV32 AY31 AY33 BJ36 BK36 BM36 AT40 AU38 U31
VCCSUS3_3
SC61 .1U-10VX-04-X-O Close to AL38
SC41 .1U-10VX-04-X-O Close to BC17
C158 .1U-10VX-04 Close to AF57
C156 .1U-10VX-04 Close to A12
20110927 Change to reserve
20110927 Change to top
SC57 .1U-10VX-04-X-O Close to BT35
SC53 .1U-10VX-04-X-O Close to AV30
SC58 .1U-10VX-04-X-O Close to AV40
11'0215
Cuz: Change to use SIO+Intel EuP Solution.
So: VCCDSW3_3 tie to +PS_3VSB.
VCCDSW3_3 AV40
D55 V_PROC_IO
B56 V_PROC_IO_NCTF
A39 V_1P1_USB
AA32 PCH_TP241
BU42 VCCRTC
BR54
BT56 V_1P5_RTC_INT
AT41 PCH_TP251
AV41 PCH_TP261
BA46 PCH_DCPSST
DCPSUS DCPSUSBYP DCPSST DCPRTC DCPRTC_NCTF
10 of 12
U1PPT
+PS_3VSB
C435 1U-10VX-04-O
C436 .1U-10VX-04
20110915 Change value
20110926 Add C436
For platform not supporting deep sleep, VCCDSW3_3 tie to +3VSB.
MAX <1mA
+RTCVCC
STP6 STP7 STP9
C394 16U-16VX
C396 .1U-10VX-04 Close to BU42
C415 4.7U-X5-08 Close to B5
C414 .1U-10VX-04
C413 .1U-10VX-04
+V_CPUVTT
+V_1P05_PCH
R456 0-04-O
R698 0-04-O
100mA up
+VCCUSB3_PLL_PCH A19
20110926 Change to top side
SC66 .1U-10VX-04-X-O Close to AR54
C410 .1U-10VX-04 Close to BR54
C391 .1U-10VX-04-O Close to AP54
20110927 Change to reserve
20110915 Change value
+V_1P8_SFR
VCCVRM_A R389 0-04
VCCVRM_B R390 0-04
VCCVRM_C R467 0-04
C353 .1U-10VX-04-O
C419 10U-X5-08
Near PCH.
20110915 Change value
+V_1P05_PCH
SC56 1U-16VX-X-O
SC63 1U-16VX-X-O
Close to AL40, AG41, AG39, AJ38
SATA RX/TX
20110915 Change value
20110927 Change to reserve
1.05V/1.00V
MAX TBD
+V_CPUVTT
Trace needs to be at least 20 mils width with full VSS/VCC reference plane)
C393 1U-16VX Close to B41, A41
20110915 Change value
+V_1P05_PCH
SC42 10U-X5-08-X-O
SC52 1U-6V3X-04-X-O
C163 10U-X5-08
20110927 Add C163
20110927 Change to reserve
PCH Core Power
100 mA +VCCSATA_PLL_PCH U56
100 mA +VCCDMI_PLL_PCH B53
+VCCIPL_PLL_PCH C54
+VCCCLK_PLL_PCH AL5
+VCCUSB3_PLL_PCH A19
VCCAPLLSATA VCCIO VCCAPLLEXP VCCAFDIPLL VCCACLK VCCAPLLDMI2
+VCC3
SC62 .1U-10VX-04-X-O
20110915 Change value
20110927 Change to reserve
For PCH PCI Decoupling
+V_1P05_PCH
PFB5 IND-10U-08-O 125 mA
C418 10U-X5-08-O
C411 1U-6V3X-04-O Close to U56
PFB6 IND-1U-08-LK-O 500 mA 08-402-105171
R419 0-04-O
+VCCUSB3_PLL_PCH_R +VCCUSB3_PLL_PCH
C382 10U-X5-08-O
C376 1U-6V3X-04-O Close to A19
PFB7 IND-1U-08-LK-O 500 mA 08-402-105171
R454 0-04-O
+VCCDMI_PLL_PCH_R +VCCDMI_PLL_PCH
C407 10U-X5-08-O
C405 1U-6V3X-04-O Close to B53
When we disable Internal VccVRM Mode, we should stuff all of them.

110106
Update Pin Name. MHB CRB07.

PCH1I
Ballout Rev 0.7
F20 F30 V25 V27 V31 V33 Y24 Y26 Y30 Y32 Y34 VCCIO
AA34 AA36 VCCIO
V22 Y20 Y22 VCCIO
B41 E41 VCCDMI
AL40 AN40 AN41 VCCIO
AG38 AG40 AG41 VCCIO
U56 VCCAPLLSATA
BA38 VCCIO
B53 VCCAPLLEXP
C54 VCCAFDIPLL
AL5 VCCACLK
A19 VCCAPLLDMI2
AE15 VCCDIFFCLKN_01
AE17 VCCDIFFCLKN_02
AG15 VCCDIFFCLKN_03
AJ20 VCCCLKDMI
AE40 VCCIO_018
AC20 VCCSSC_01
AE20 VCCSSC_02
AV24 AV26 AY25 AY27 VCCIO_001 VCCIO_002 VCCIO_003 VCCIO_004
V36 Y36 AJ38 Y28 VCCIO_013 VCCIO_012 VCCIO_011 VCCIO_014
9 of 12
U1PPT
AC24 AC26 AC28 AC30 AC32 AE24 AE28 AE30 AE32 AE34 AE36 AG32 AG34 AJ32 AJ34 AJ36 AL32 AL34 AN32 AN34 AR32 AR34 VCCCORE
AG24 AG26 AG28 AJ24 AJ26 AJ28 AL24 AL28 AN22 AN24 AN26 AN28 AR24 AR26 AR28 AR30 AR36 AR38 AU30 AU36 VCCASW
AU34 AV36 AV32 VCCASW
1.05V
MAX 6.2A
+V_1P05_PCH
1.05V
MAX 6.2A
+V_1P05_PCH
1.05V
MAX 1.8A
+V_1P05_PCH
AMT Only
SC48 1U-6V3X-04-X-O Close to AJ24, AN22
SC46 10U-X5-08-X-O
20110927 Change to reserve
SC49 1U-6V3X-04-X-O Close to AJ24, AN22
SC40 1U-6V3X-04-X-O
20mA
+V_1P05_PCH_SRC
20110927 Change to reserve
Place Near ends of Power Corridor
+V_1P05_PCH
SC60 1U-16VX-X-O
SC59 1U-16VX-X-O
20110915 Change value
20110927 Change to reserve
PCIe Decoupling Filter
+V_1P05_PCH
20110927 Change to reserve
SC65 1U-6V3X-04-X-O
SC47 1U-6V3X-04-X-O
SC50 1U-6V3X-04-X-O
SC44 1U-6V3X-04-X-O
SC54 10U-X5-08-X-O
C194 10U-X5-08
Close to F20, AC24, AC20, AE15, AA34, Y20
For PCH Decoupling

Elitegroup Computer Systems

Title	PCH - PWR	
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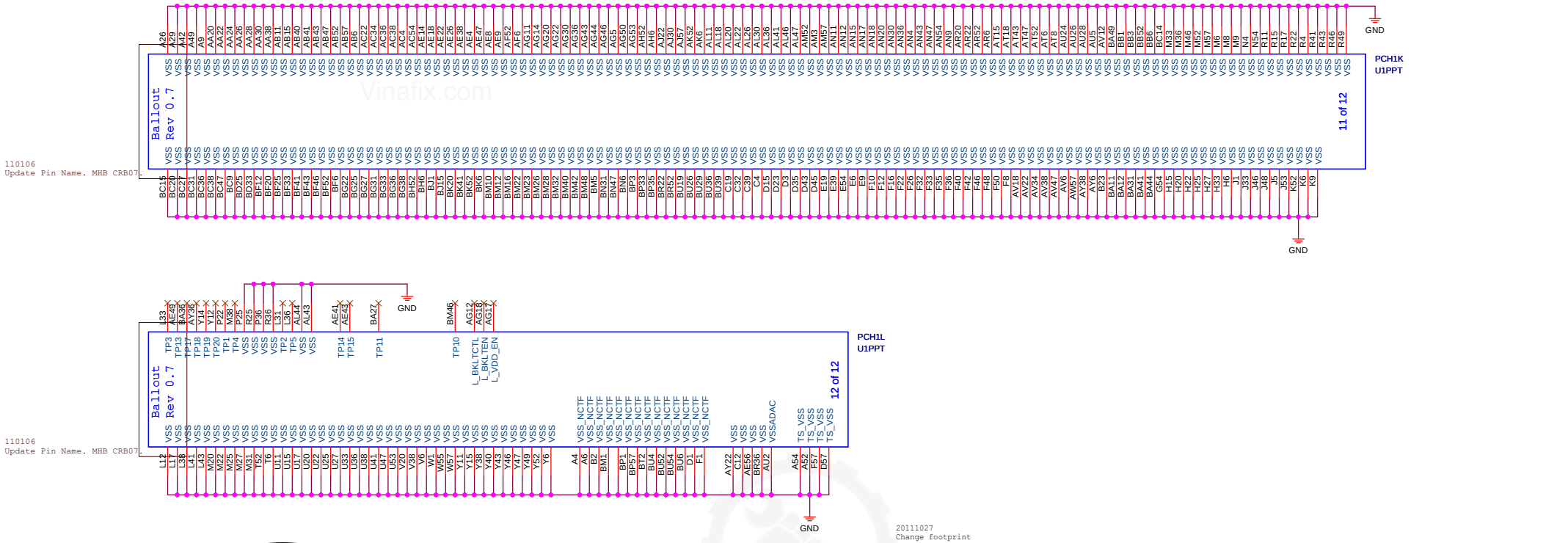
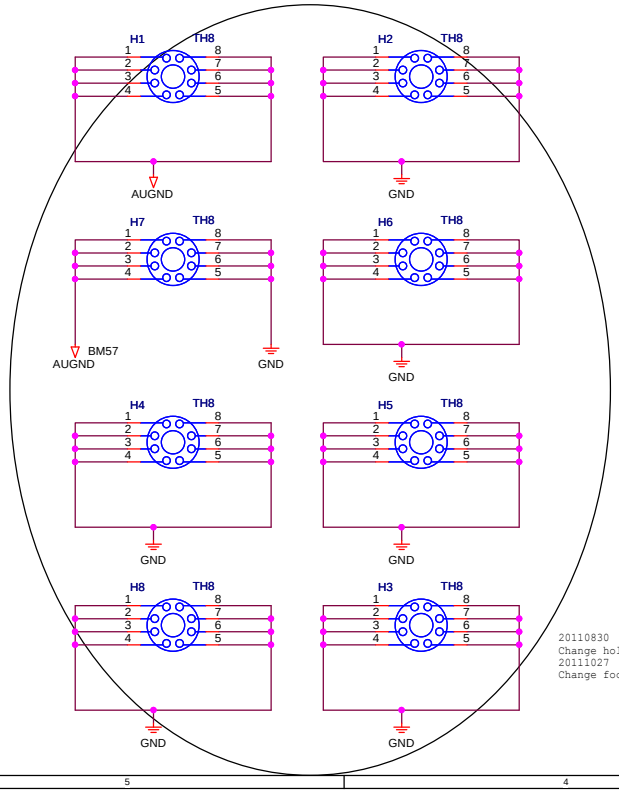
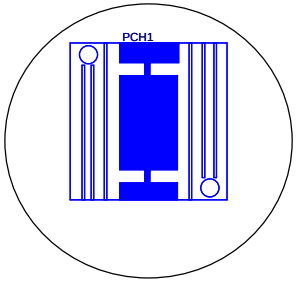
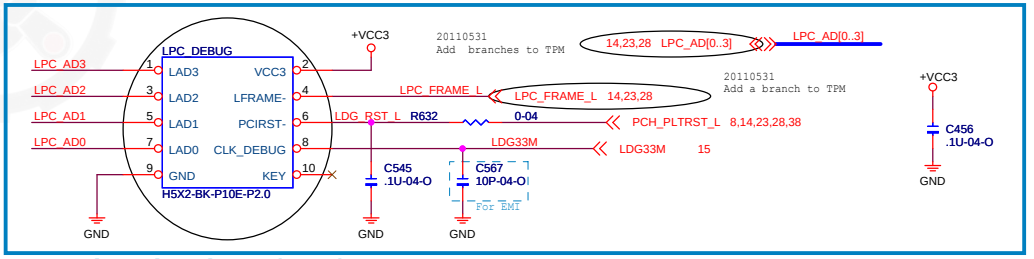




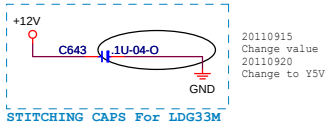
20110830
Change holes pin define
20111027
Change footprint



20110829
Change PCH heatsink
20110914
Change footprint



LPC Debug header Circuit



20110915
Change value
20110920
Change to Y5V

Elitegroup Computer Systems		
Title: PCH - GND, VGA CONN		
Size: Custom	Document Number: H77H2-EM	Rev: V.A
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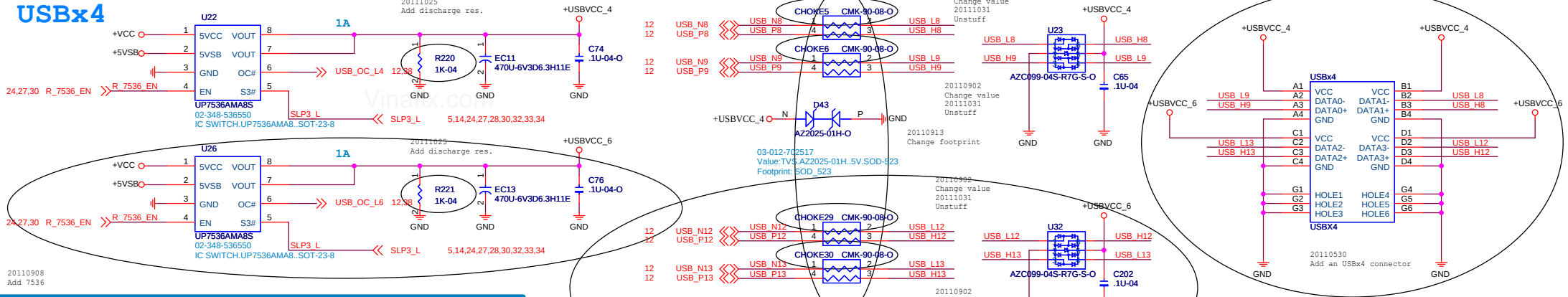
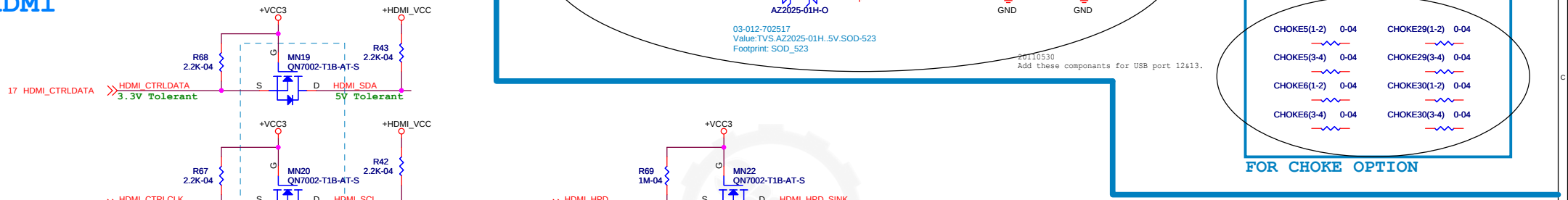
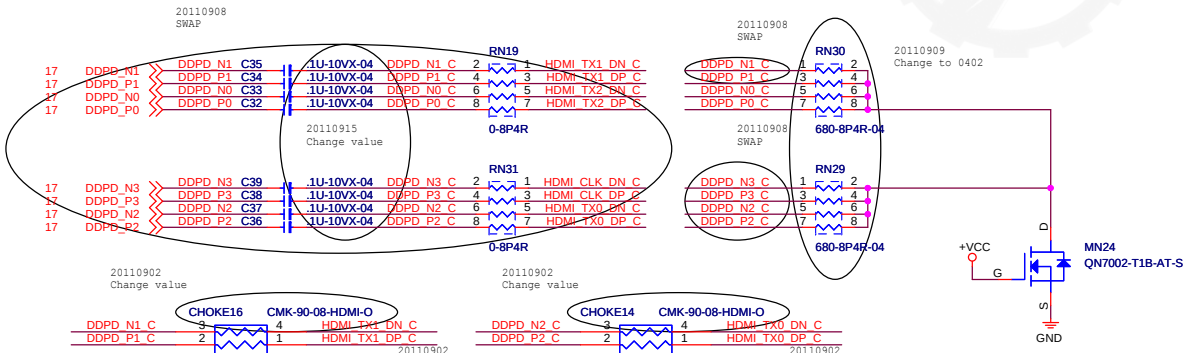
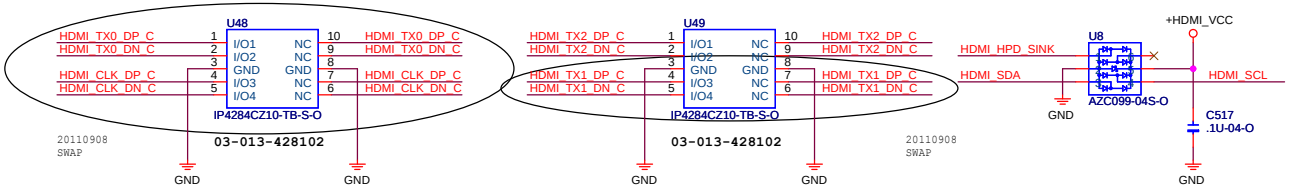
USBx4

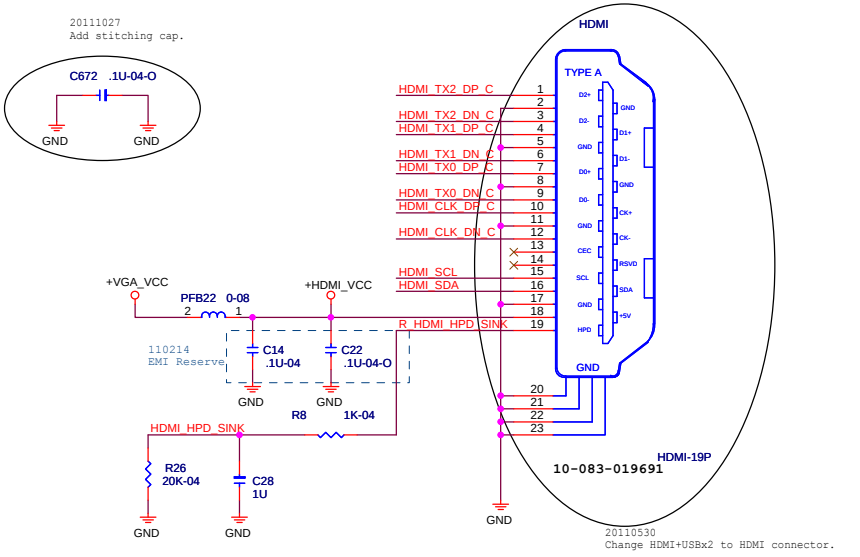


HDMI









Elitegroup Computer Systems			
Title: HDMI, USBx4			
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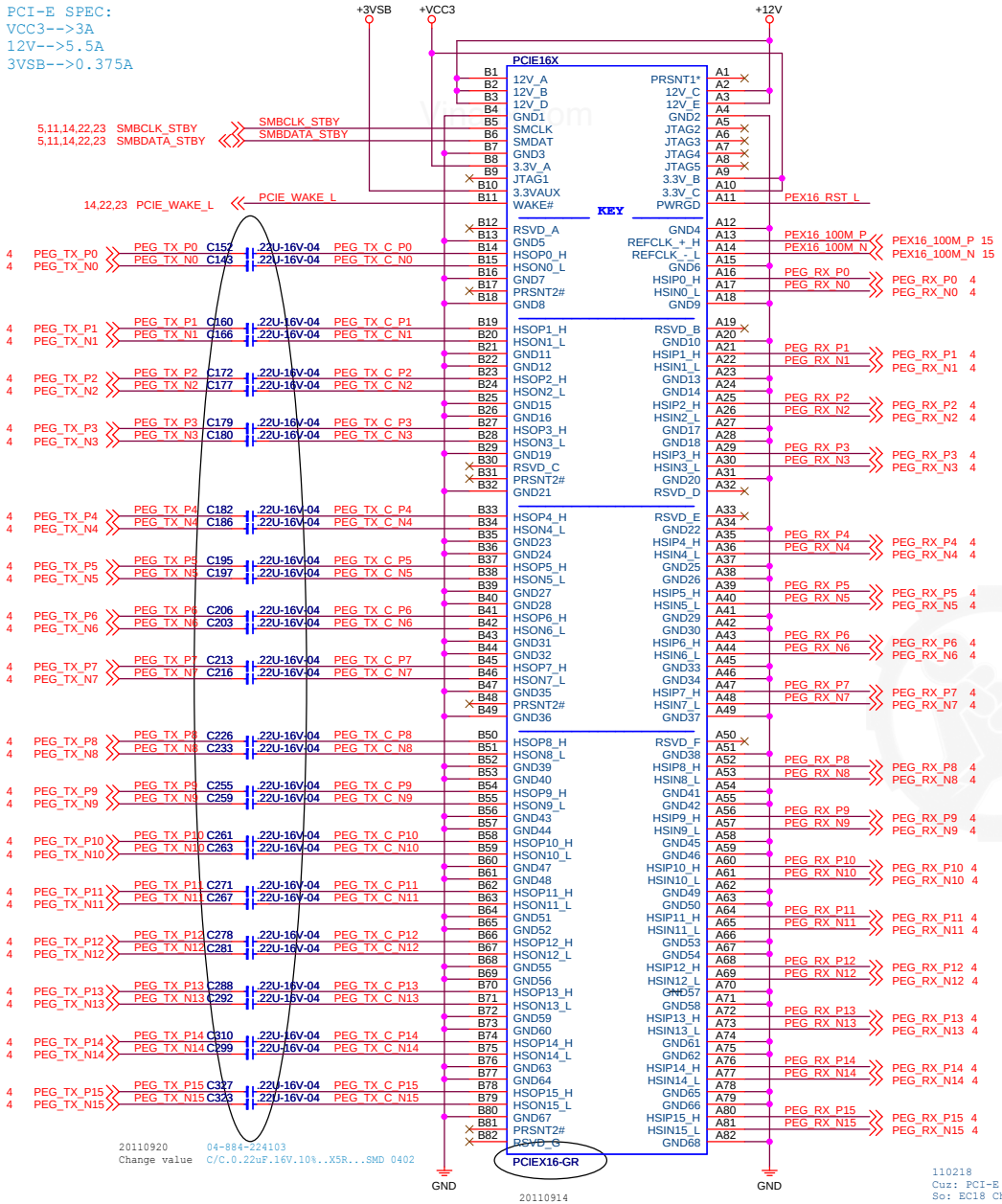
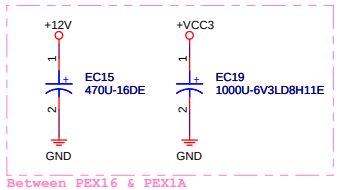
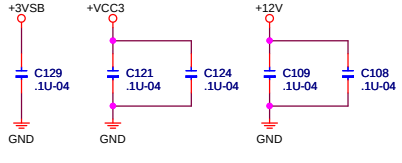
PCI-E SPEC:
VCC3-->3A
12V-->5.5A
3VSB-->0.375A



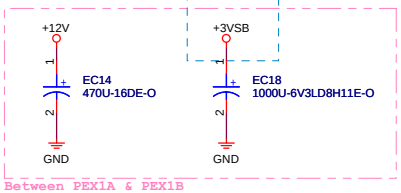
04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm....

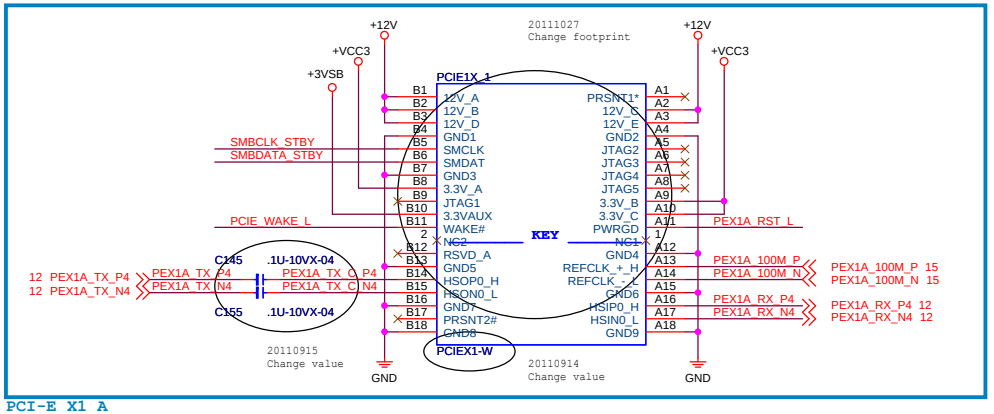




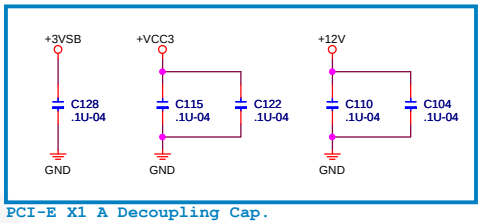
110218
Cuz: PCI-E Card +3VSB over 375mA SPEC issue
So: EC18 Change to +3VSB.

04-711-102073
E/C.1000uF.16V.20%...105C.RT D10*17mm....

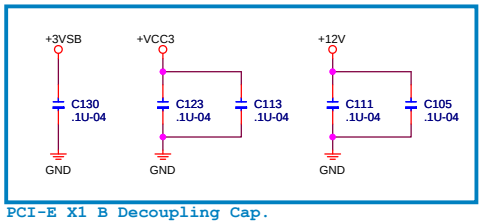




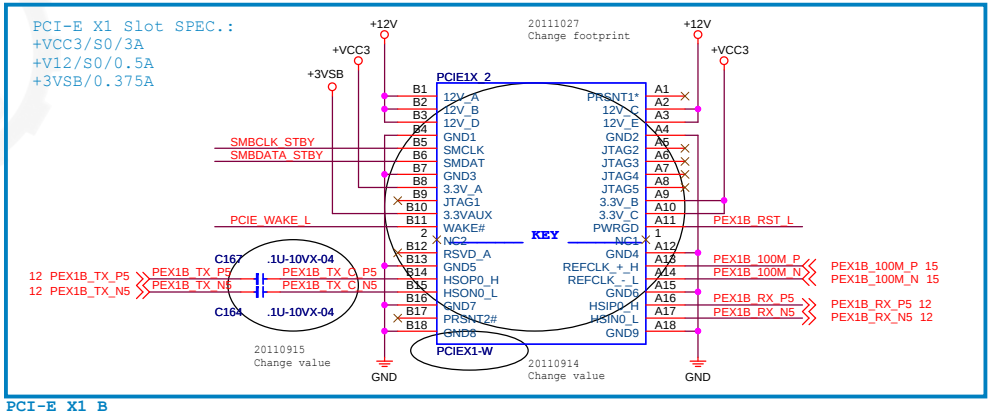
PCI-E X1 A



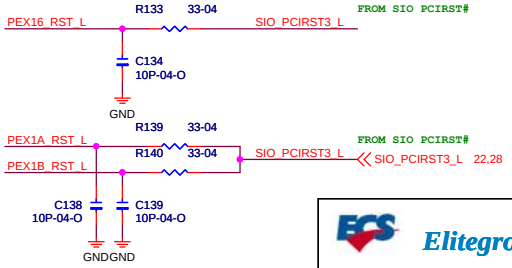
PCI-E X1 A Decoupling Cap.



PCI-E X1 B Decoupling Cap.



PCI-E X1 B



Elitegroup Computer Systems

Title	Slot - PCI-EX16/PCI-EX1	
Size: Custom	Document Number: H77H2-EM	Rev: V.A
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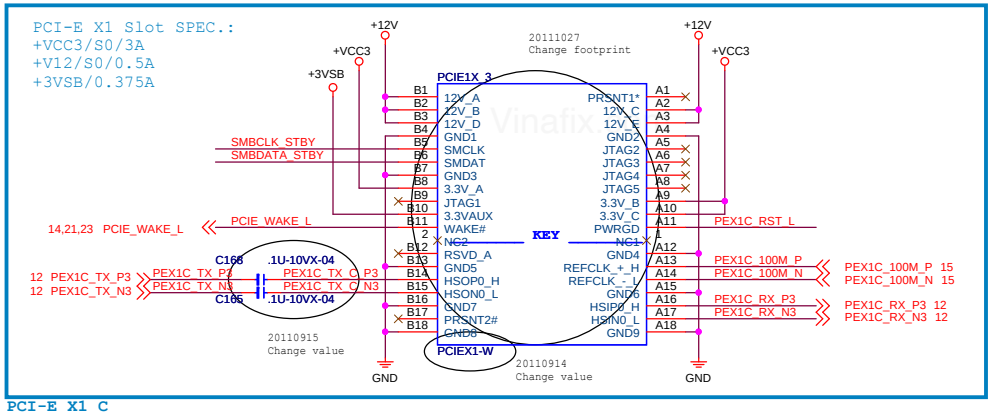
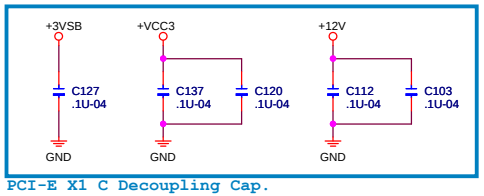
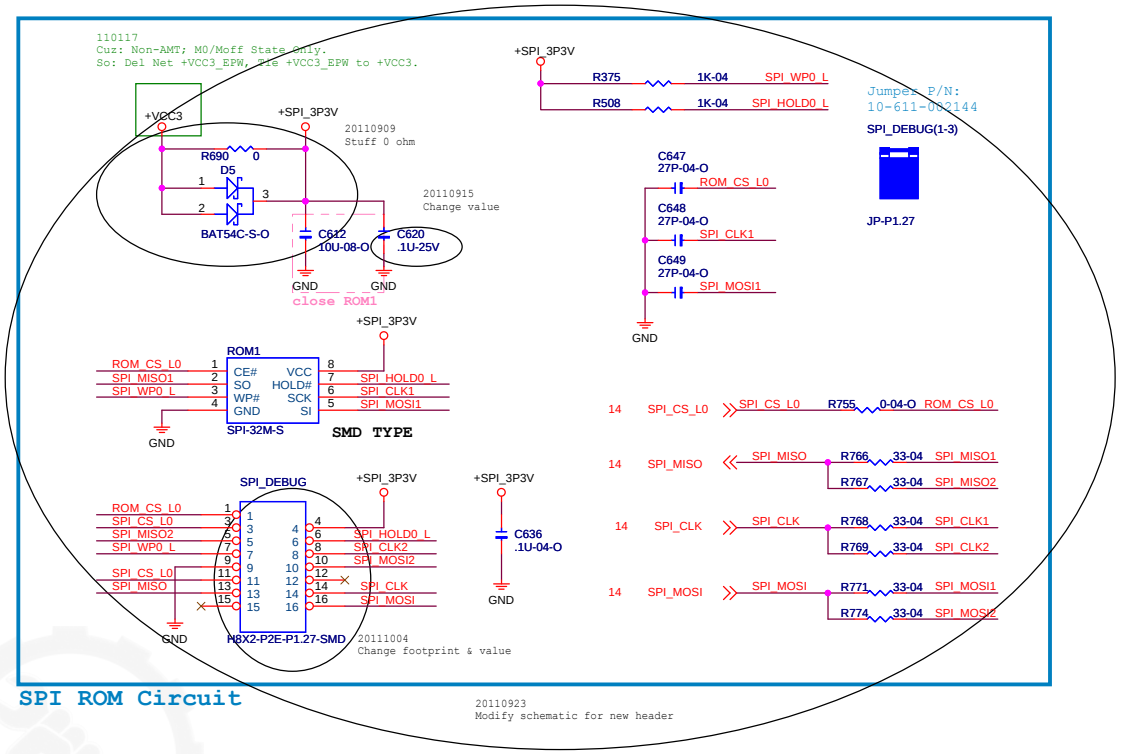


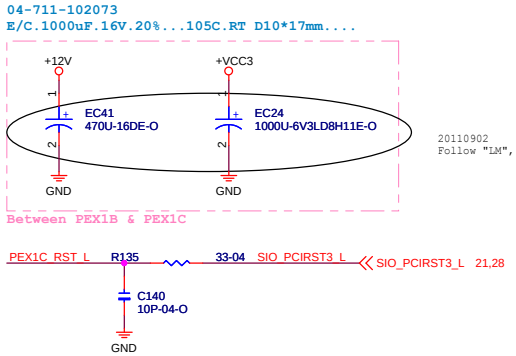
PCI-E X1 C

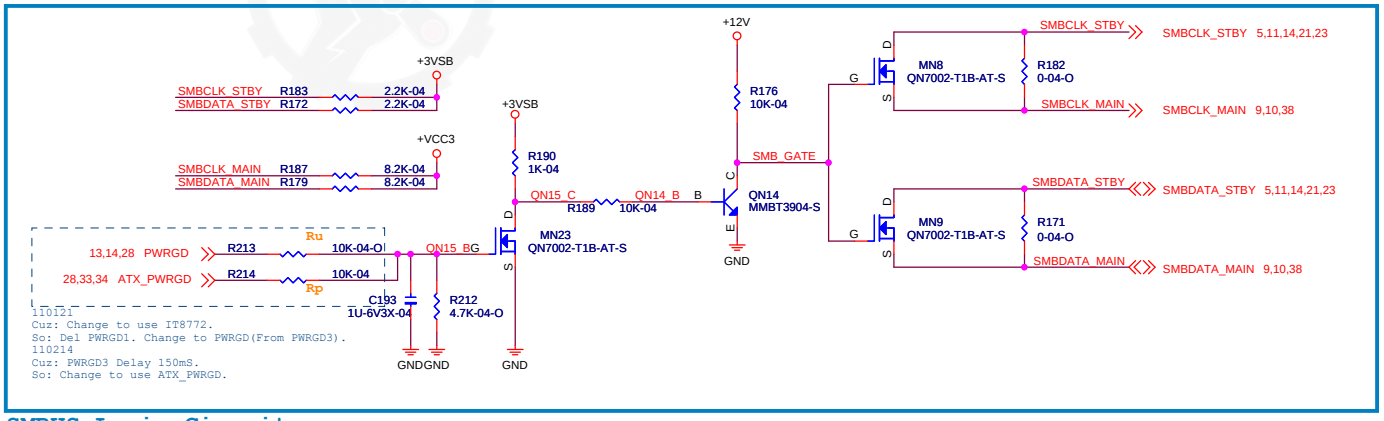


PCI-E X1 C Decoupling Cap.



SPI ROM Circuit





SMBUS Logic Circuit

Elitegroup Computer Systems

Title	Slot - PCIEX1, SPI ROM, SMBUS	
Size: Custom	Document Number: H77H2-EM	Rev: V.A
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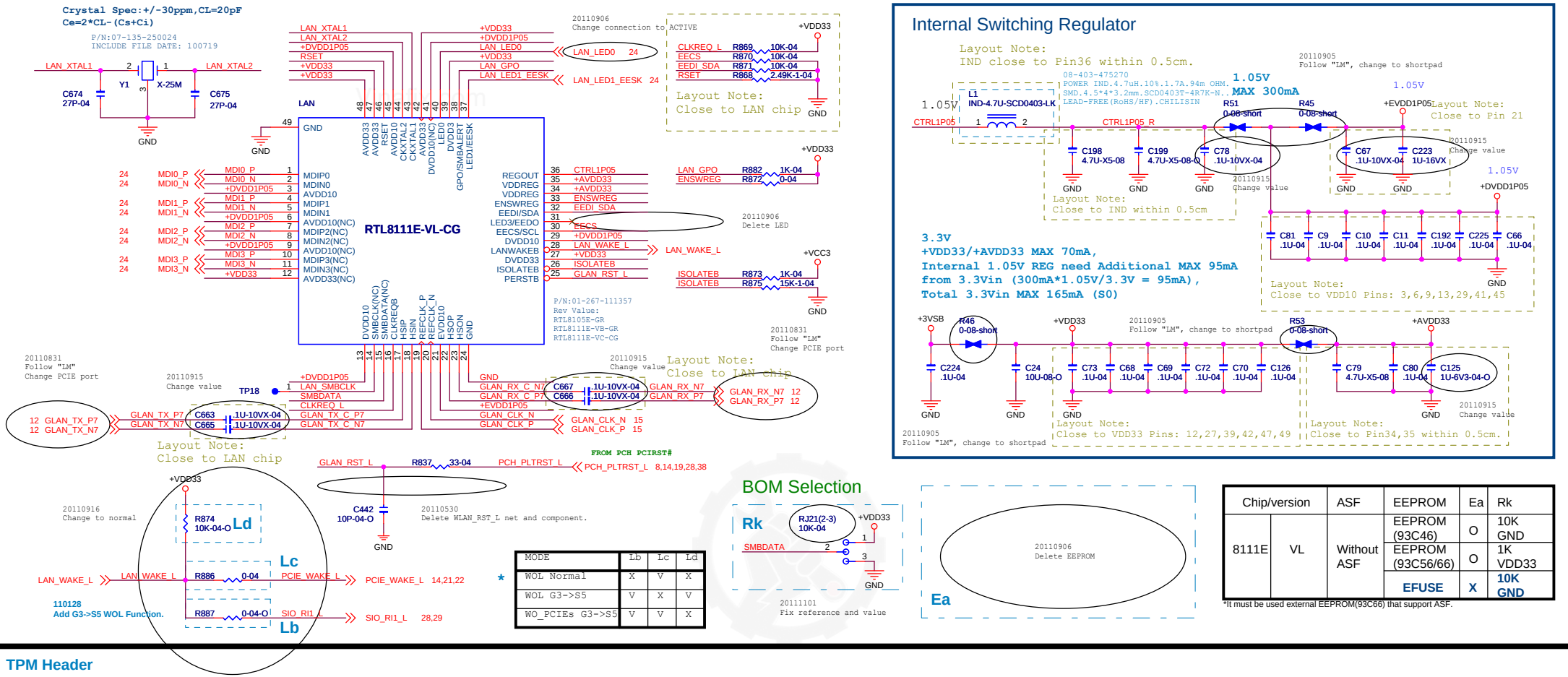
Crystal Spec:+/-30ppm,CL=20pF
Ce=2*CL-(Cs+Ci)
P/N:07-135-250024
INCLUDE FILE DATE: 100719
LAN_XTAL1
LAN_XTAL2
Y1
X-25M
C674 27P-04
C675 27P-04
GND
LAN
RTL8111E-VL-CG
MDI0_P
MDI0_N
MDI1_P
MDI1_N
MDI2_P
MDI2_N
MDI3_P
MDI3_N
+DVDD1P05
+VDD33
20110906
Change connection to ACTIVE
LAN_LED0 24
LAN_LED1_EESK 24
CLKREQ_L R869 10K-04
EECS R870 10K-04
EEDI_SDA R871 10K-04
RSET R868 2.49K-1-04
Layout Note:
Close to LAN chip
LAN_GPO R882 1K-04
ENSWREG R872 0-04
20110906
Delete LED
LAN_WAKE_L
+VCC3
ISOLATEB R873 1K-04
ISOLATEB R875 15K-1-04
P/N:01-267-111357
Rev Value:
RTL8105E-GR
RTL8111E-VB-GR
RTL8111E-VC-CG
20110831
Follow "LM"
Change PCIE port
20110915
Change value
TP18
GLAN_TX_P7
GLAN_TX_N7
C663 .1U-10VX-04
C665 .1U-10VX-04
GLAN_RX_C_N7
GLAN_RX_C_P7
C667 .1U-10VX-04
C666 .1U-10VX-04
GLAN_RX_N7 12
GLAN_RX_P7 12
GLAN_CLK_N 15
GLAN_CLK_P 15
Layout Note:
Close to LAN chip
GLAN_RST_L
R837 33-04
PCH_PLTRST_L
FROM PCH PCIRST#
PCH_PLTRST_L 8,14,19,28,38
C442 10P-04-O
20110530
Delete WLAN_RST_L net and component.
20110916
Change to normal
R874 10K-04-O
Ld
Lc
Lb
LAN_WAKE_L
R886 0-04
PCIE_WAKE_L
PCIE_WAKE_L 14,21,22
R887 0-04-O
SIO_RI1_L
SIO_RI1_L 28,29
110128
Add G3->S5 WOL Function.
MODE | Lb | Lc | Ld
WOL Normal | X | V | X
WOL G3->S5 | V | X | V
WO_PCIEs G3->S5 | V | V | X
BOM Selection
Rk
RJ21(2-3) 10K-04
SMBDATA
20111101
Fix reference and value
Ea
20110906
Delete EEPROM
Internal Switching Regulator
Layout Note:
IND close to Pin36 within 0.5cm.
08-403-475270
POWER IND.4.7uH.10%.1.7A.94m OHM.
SMD.4.5*4*3.2mm.SCD0403T-4R7K-N..
LEAD-FREE(RoHS/HF).CHILISIN
L1
IND-4.7U-SCD0403-LK
1.05V
MAX 300mA
CTRL1P05
CTRL1P05_R
R51 0-08-short
R45 0-08-short
+EVDD1P05
Layout Note:
Close to Pin 21
C198 4.7U-X5-08
C199 4.7U-X5-08-O
C78 .1U-10VX-04
C67 .1U-10VX-04
C223 1U-16VX
Layout Note:
Close to IND within 0.5cm
3.3V
+VDD33/+AVDD33 MAX 70mA,
Internal 1.05V REG need Additional MAX 95mA
from 3.3Vin (300mA*1.05V/3.3V = 95mA),
Total 3.3Vin MAX 165mA (S0)
C81 .1U-04
C9 .1U-04
C10 .1U-04
C11 .1U-04
C192 .1U-04
C225 .1U-04
C66 .1U-04
Layout Note:
Close to VDD10 Pins: 3,6,9,13,29,41,45
+3VSB
R46 0-08-short
+VDD33
R53 0-08-short
+AVDD33
C224 .1U-04
C24 10U-08-O
C73 .1U-04
C68 .1U-04
C69 .1U-04
C72 .1U-04
C70 .1U-04
C126 .1U-04
C79 4.7U-X5-08
C80 .1U-04
C125 1U-6V3-04-O
Layout Note:
Close to VDD33 Pins: 12,27,39,42,47,49
Layout Note:
Close to Pin34,35 within 0.5cm.
20110905
Follow "LM", change to shortpad
20110915
Change value
Chip/version | ASF | EEPROM | Ea | Rk
8111E | VL | Without ASF | EEPROM (93C46) | O | 10K GND
EEPROM (93C56/66) | O | 1K VDD33
EFUSE | X | 10K GND
*It must be used external EEPROM(93C66) that support ASF.
TPM Header
20110530
Delete PCIE1X_4 Wireless Card slot
20110531
Add TPM Header
20110913
Add resistor
TPM33M
LPC_FRAME_L
SIO_PCIRST1_L
LPC_AD3
LPC_AD0
R597 33-04
R514 0-04
R501 8.2K-04
R515 0-04-O
R511 0-04-O
SER_IRQ
SMBDATA_STBY 5,11,14,21,22
SMBCLK_STBY 5,11,14,21,22
LPC_AD2 14,19,28
LPC_AD1 14,19,28
TPM
H10X2-P4E-B
C446 .1U-04-O
C443 10P-04-O
C444 10P-04-O
C447 .1U-04-O
C522 .1U-04-O
20110914
Add cap,
C650 .1U-04-O
C657 .1U-04-O
20110919
Add stitching cap.
Elitegroup Computer Systems
Title
LAN(RTL8105E/8111E)
Size Custom
Document Number H77H2-EM
Rev V.A
Date: Wednesday, November 02, 2011
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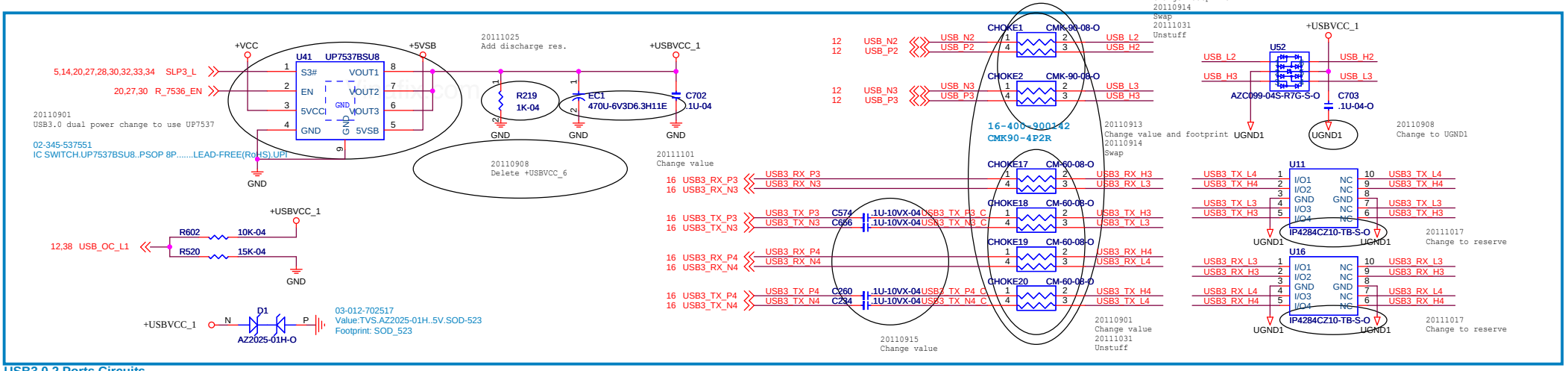
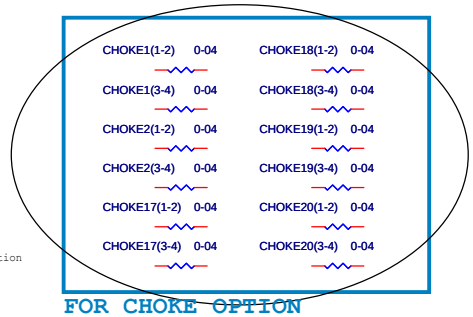
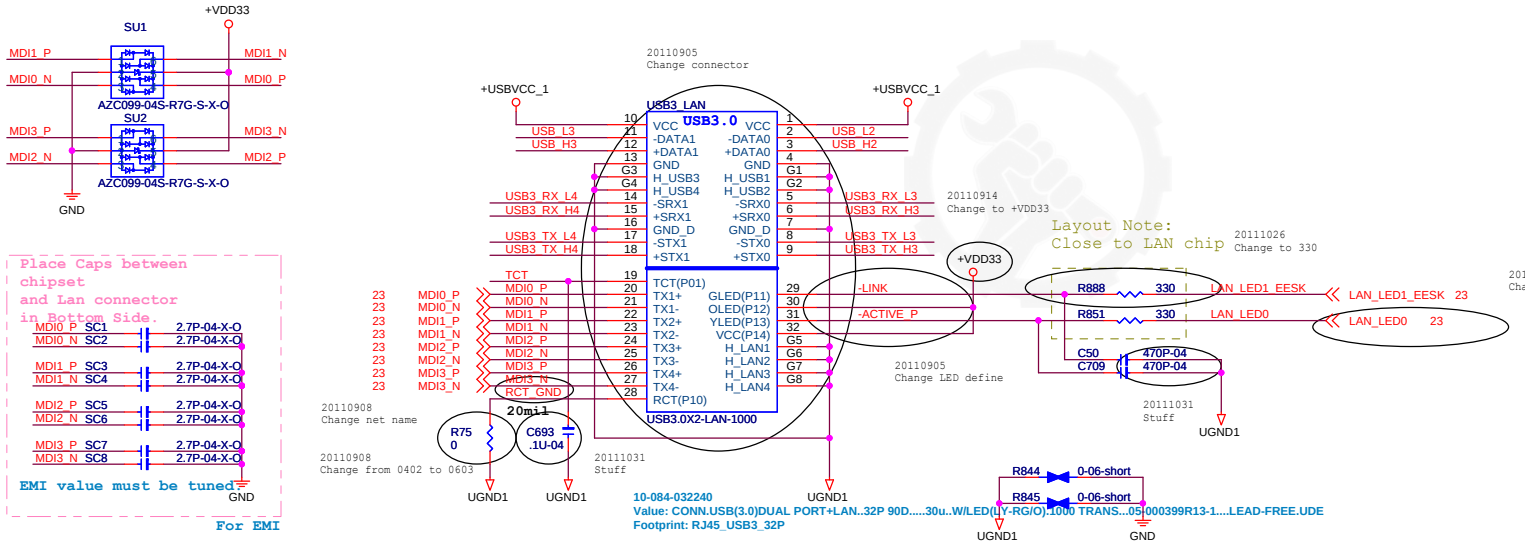
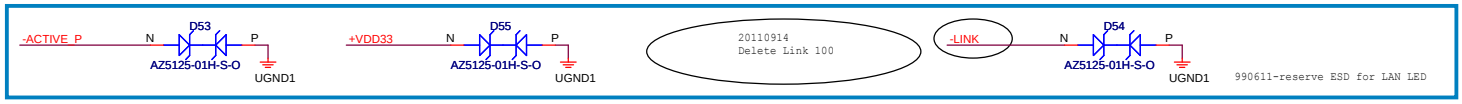
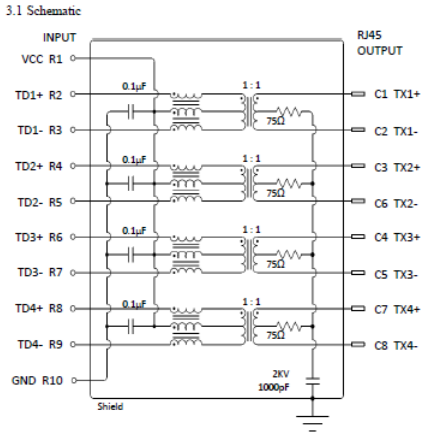


USB3.0 2 Ports Circuits









<Orgaddr1> Elitegroup Computer Systems

Title: USBLAN Connector

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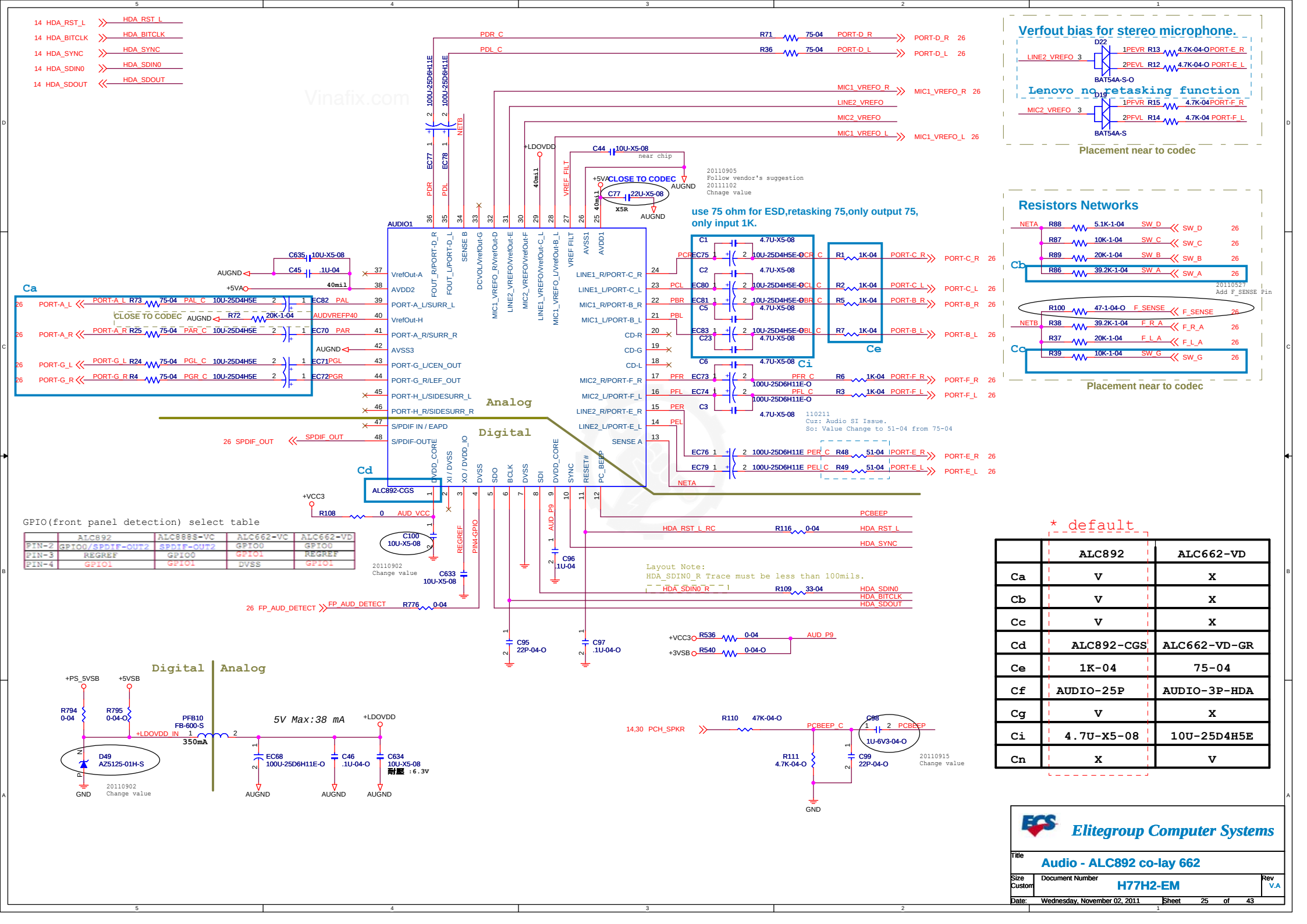
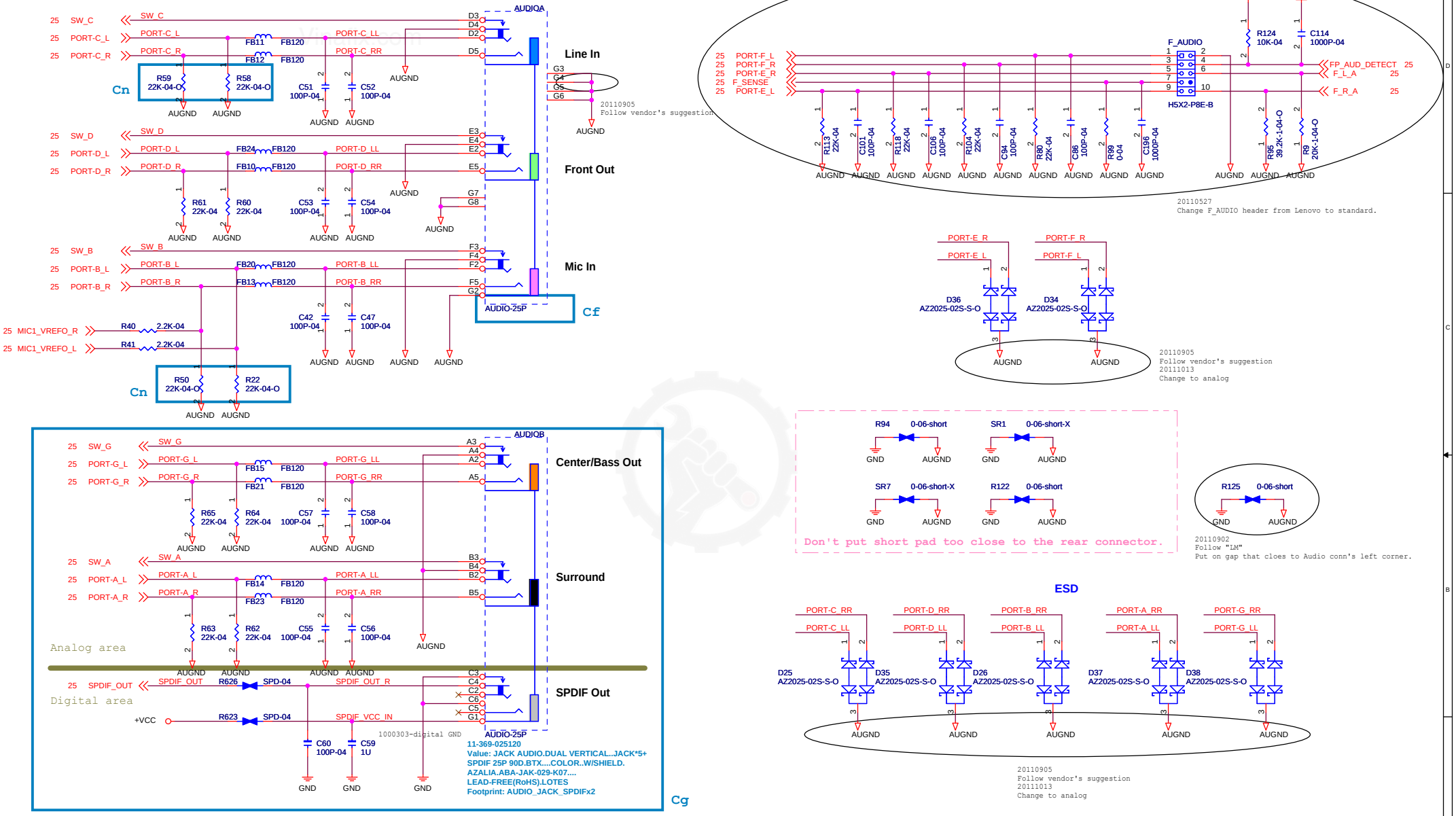


	ALC892	ALC662-VD
Ca	V	X
Cb	V	X
Cc	V	X
Cd	ALC892-CGS	ALC662-VD-GR
Ce	1K-04	75-04
Cf	AUDIO-25P	AUDIO-3P-HDA
Cg	V	X
Ci	4.7U-X5-08	10U-25D4H5E
Cn	X	V

* default

	ALC892	ALC888S-VC	ALC662-VC	ALC662-VD
PIN-2	GPIO0/SPDIF-OUT2	SPDIF-OUT2	GPIO0	GPIO0
PIN-3	REGREF	GPIO0	GPIO1	REGREF
PIN-4	GPIO1	GPIO1	DVSS	GPIO1



Elitegroup Computer Systems

Title	Audio - CONN/HDR	
Size: Custom	Document Number: H77H2-EM	Rev: V.A
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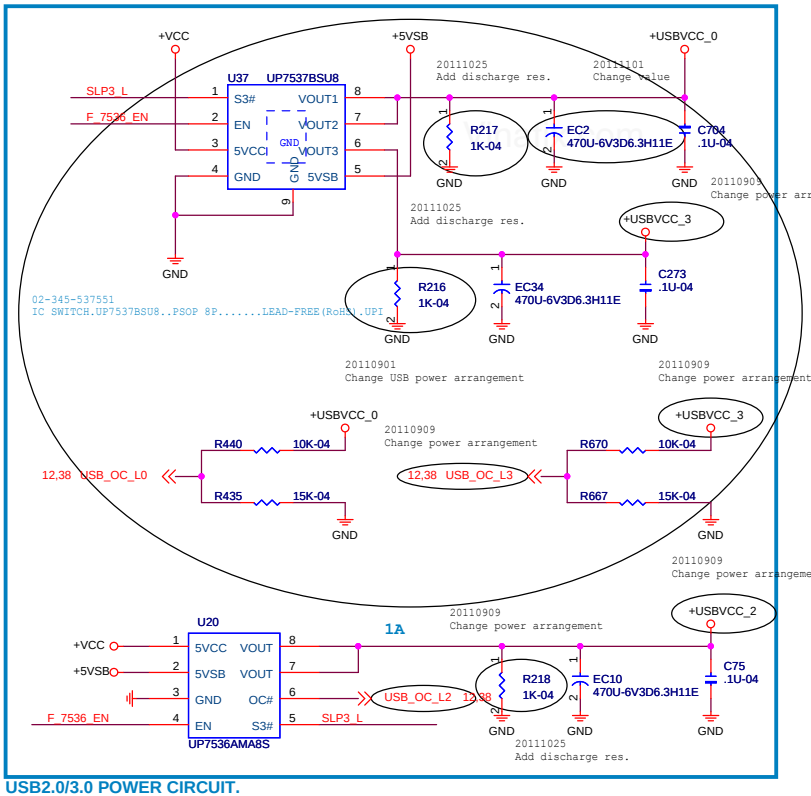
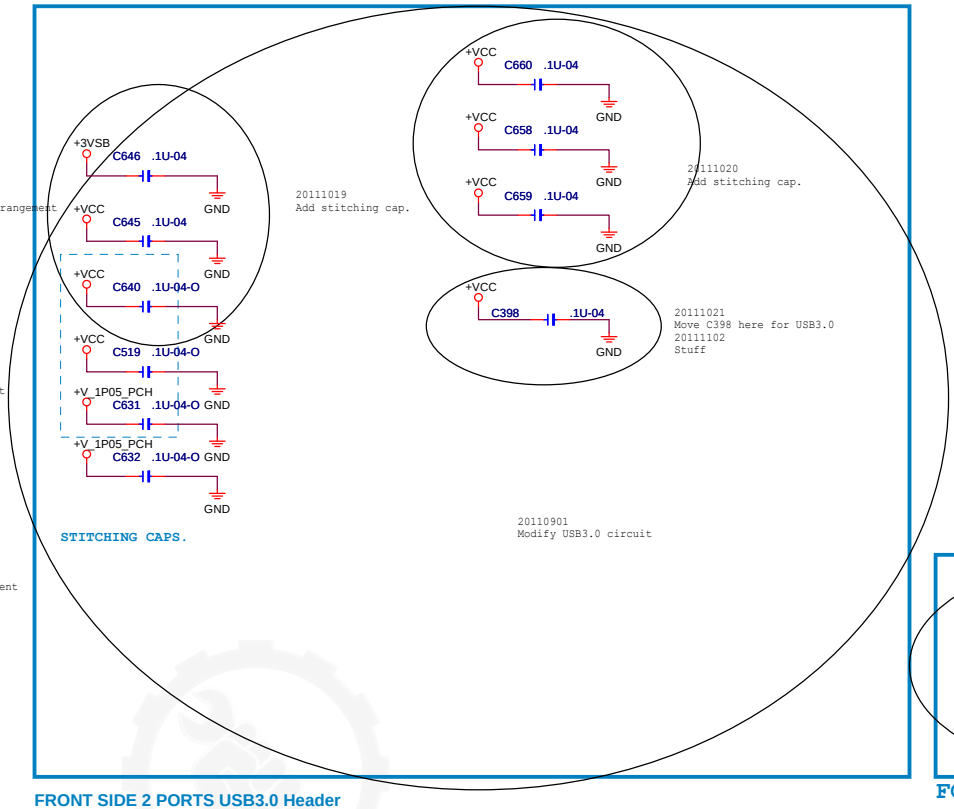
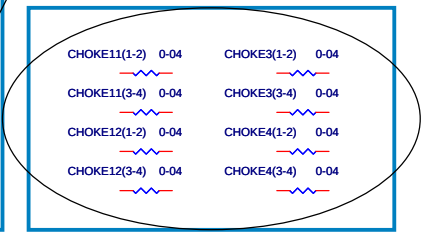


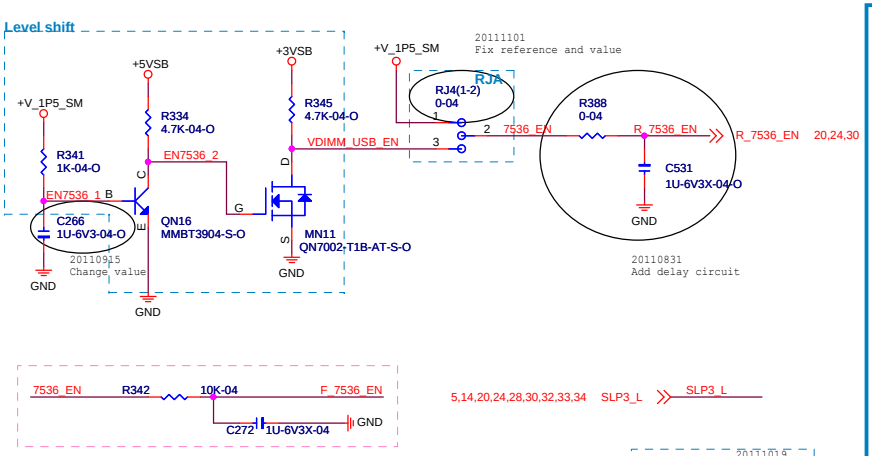
USB2.0/3.0 POWER CIRCUIT.



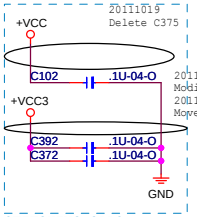
FRONT SIDE 2 PORTS USB3.0 Header

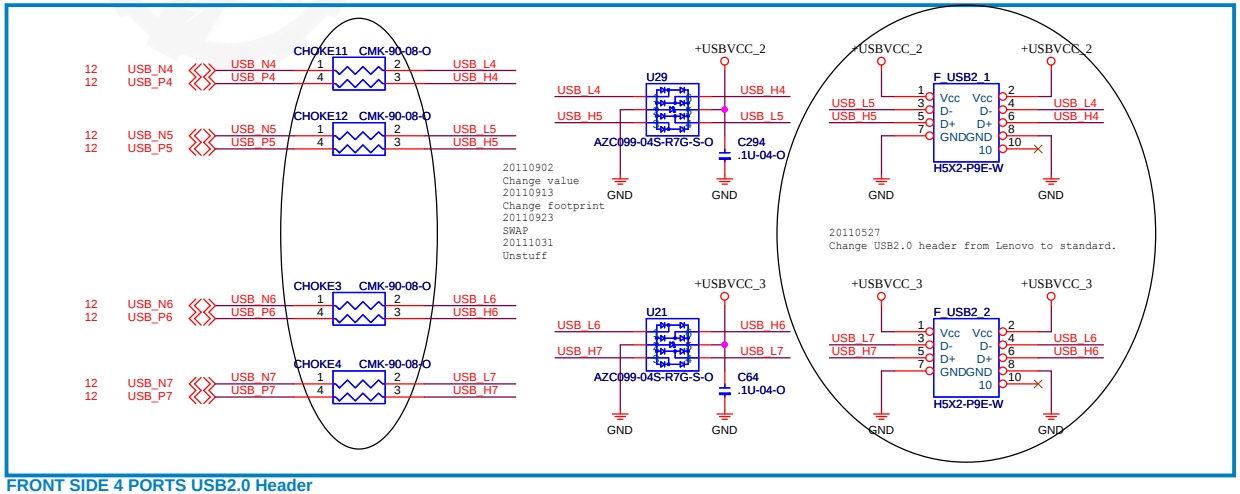


FOR CHOKE OPTION

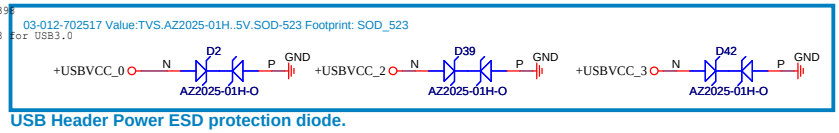


uP7536 Enable use	Level shift	RJA	RJB	S4/S5 USB_5V_DUAL	Customer
* VDIMM	N A	0ohm (1-2)	N A	0 Volt	Lenovo S4/S5 w/o USB_5V_DUAL
VDIMM level shift (3.3V)	Stuff	0ohm (2-3)	N A	0 Volt	





FRONT SIDE 4 PORTS USB2.0 Header



USB Header Power ESD protection diode.

Elitegroup Computer Systems

Title: USB - PWR/CONN/HDR

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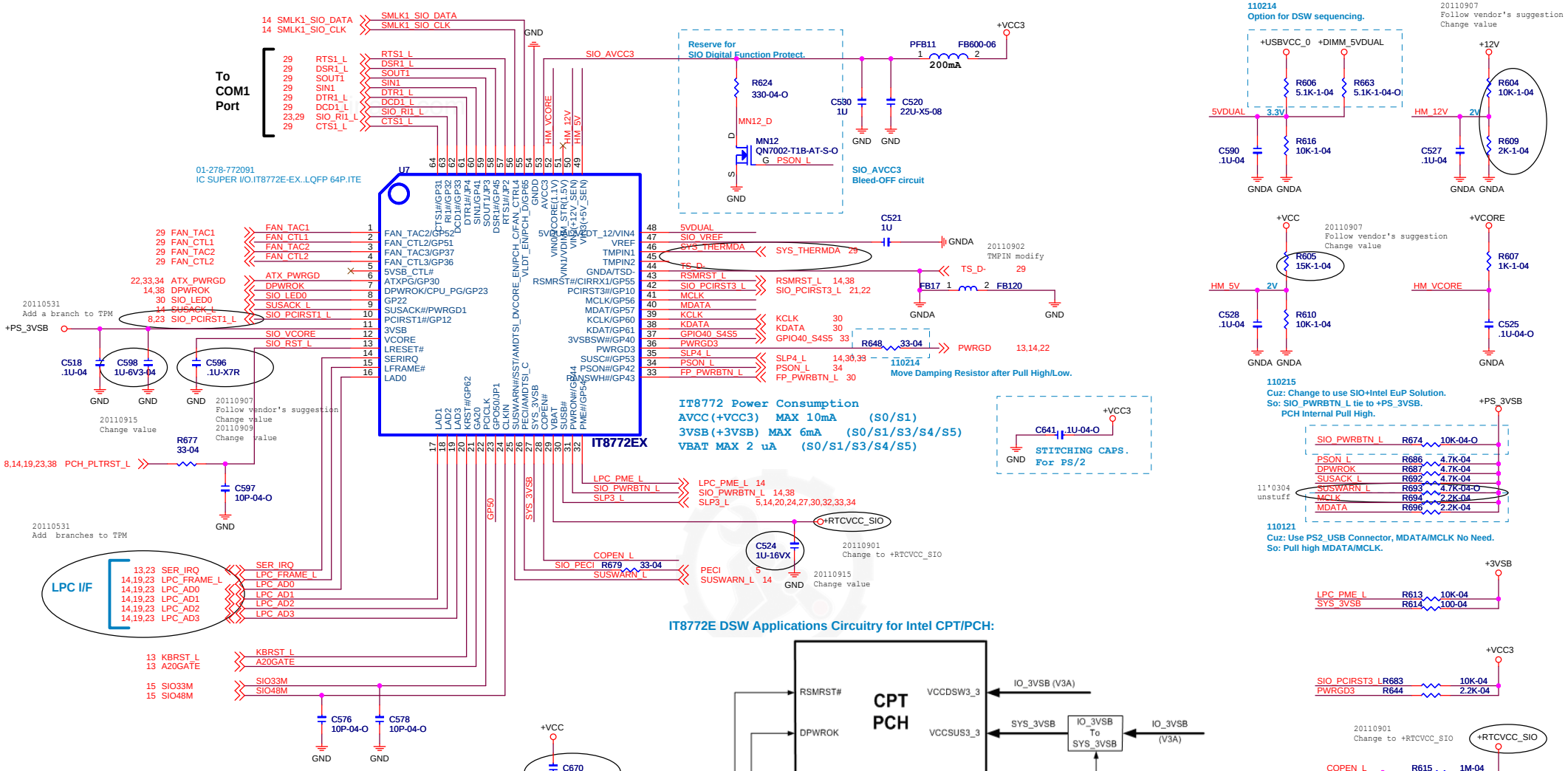

Power-On Strapping

	Symbol	Value		Description
JP1 Pin-23	DSW_EUP_SEL	1		EUP(default)
		0	*	DSW
JP2 Pin-57	WDT_EN	1	*	Disable WDT to reset PWROK(default)
		0		Enable WDT to reset PWROK
JP3 Pin-59	FAN_CTL_SEL	1	*	EC Index 6Bh/73h default = 80h
		0		EC Index 6Bh/73h default = 00h
JP4 Pin-61	K8PWR_EN	1	*	Disable K8 Power Sequence(default)
		0		Enable K8 Power Sequence

Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

Title	SIO - IT8728
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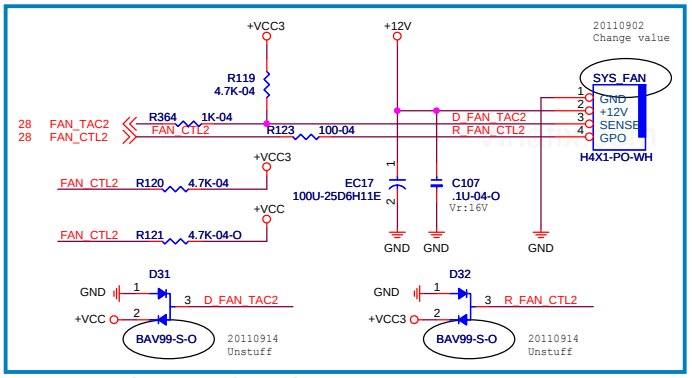
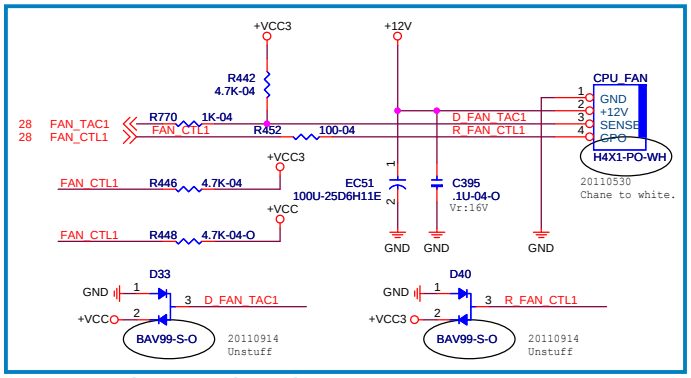
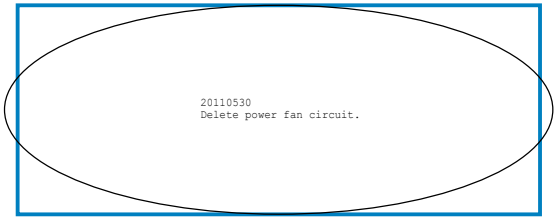


SYS FAN 4-PIN Circuit

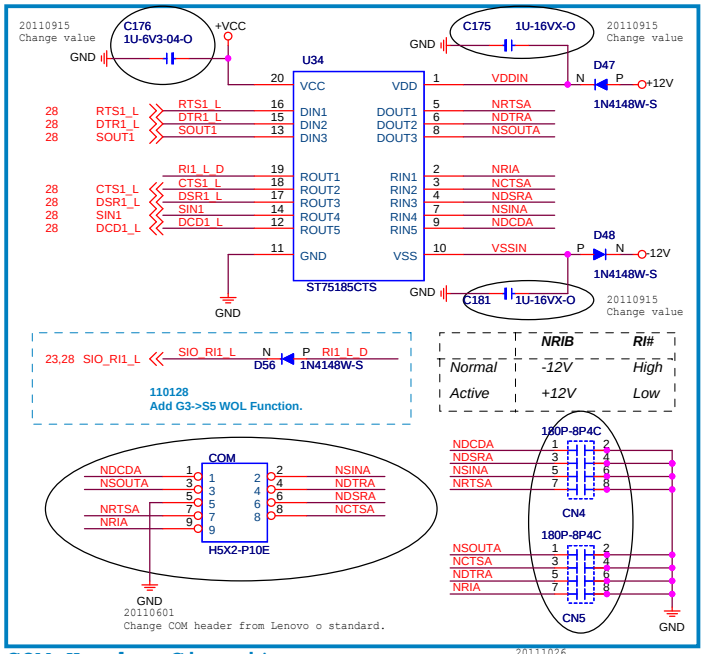


CPU FAN 4-PIN Circuit

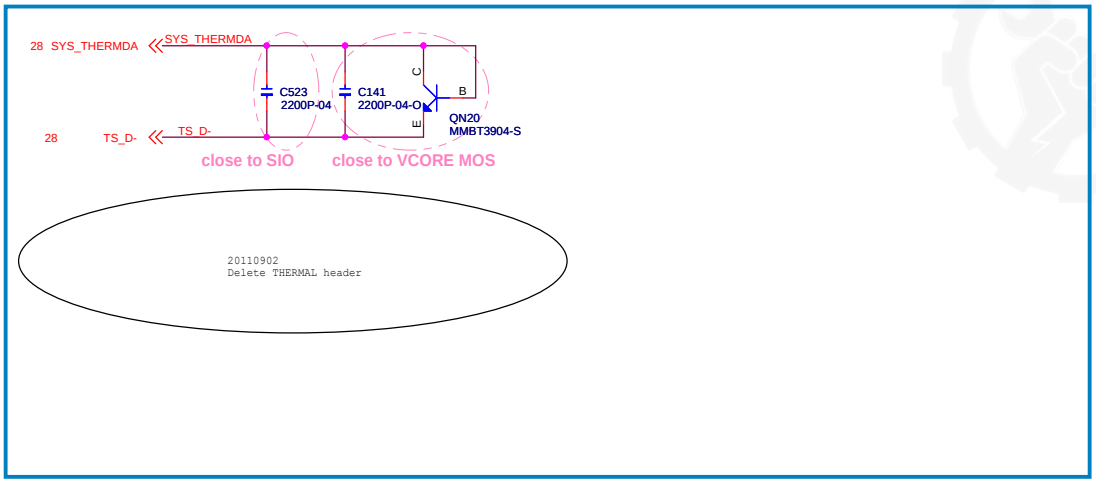


PWR FAN 3-PIN Circuit

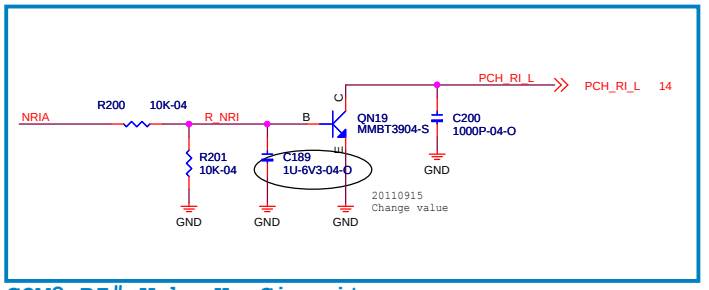
CASE Open Circuit



COM Header Circuit



Thermal Sense



COM2 RI# Wake Up Circuit

Elitegroup Computer Systems

Title: FAN, COM, CASE_OPEN, THERM

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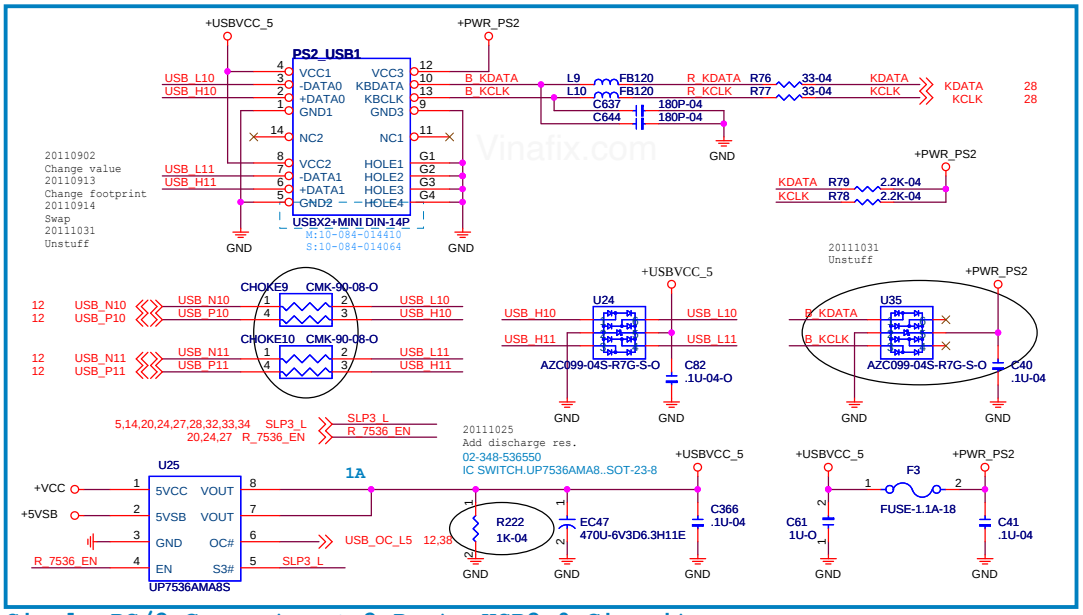
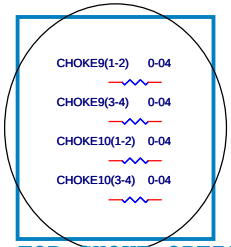
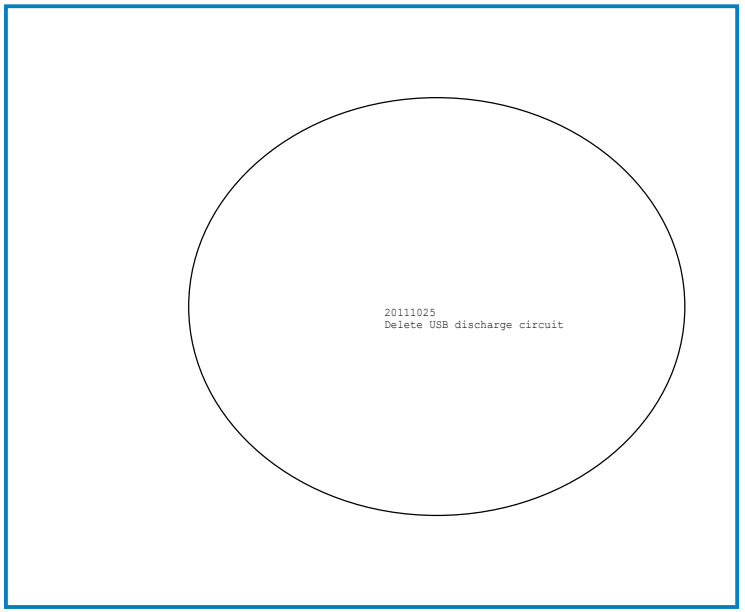


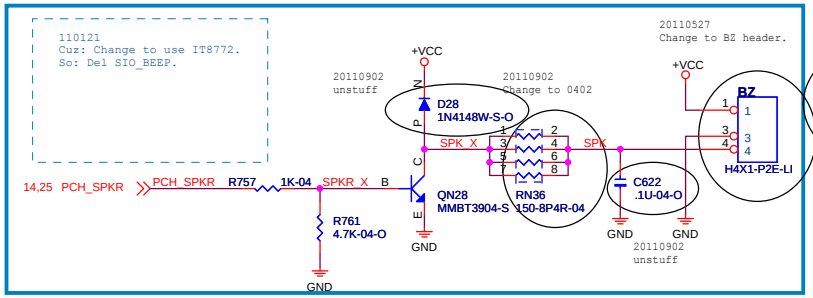
Single PS/2 Connector + 2 Ports USB2.0 Circuit



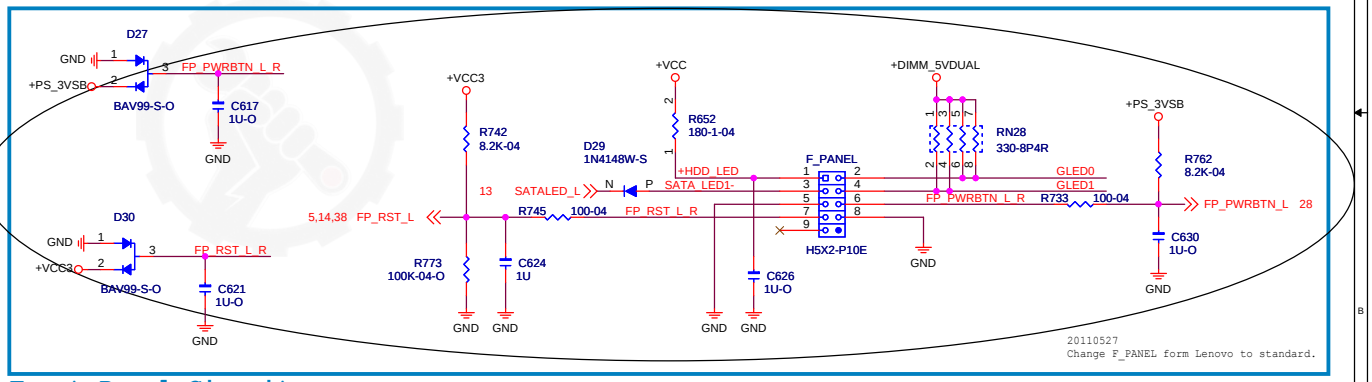
FOR CHOKE OPTION



USB Discharge Circuit

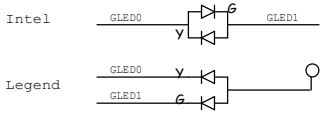


Buzzer Circuit

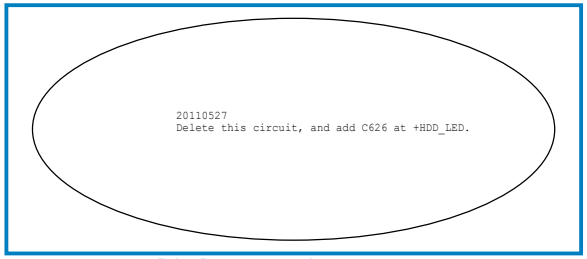


Front Panel Circuit

3-Pin Dual color LED	
S0	Steady Green
S1	Green-blinking
S3	Steady Yellow
S4,S5	Off
2-Pin Single color LED	
S0	Steady Green
S1,S3	LED-blinking
S4,S5	Off



Front LED



SATA LED Blink Once in Power On Issue

Elitegroup Computer Systems

Title	F_PANEL, BUZ, PS2, USB Discharge	
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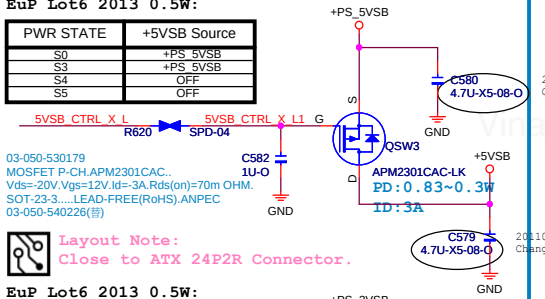
EuP Lot6 2013 0.5W:

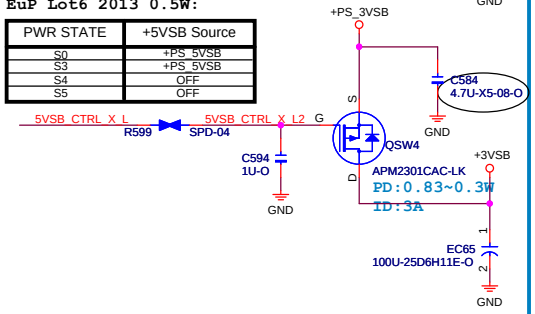
PWR STATE	+5VSB Source
S0	+PS_5VSB
S3	+PS_5VSB
S4	OFF
S5	OFF



Layout Note:
Close to ATX 24P2R Connector.

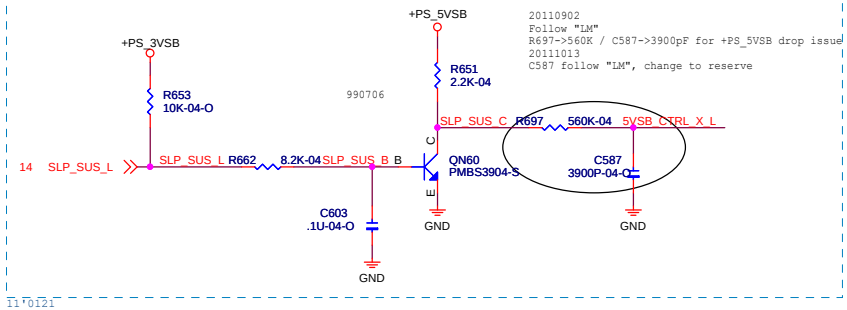
EuP Lot6 2013 0.5W:

PWR STATE	+5VSB Source
S0	+PS_5VSB
S3	+PS_5VSB
S4	OFF
S5	OFF



11'0121
Cuz: Change to use SIO+Intel EuP Solution.
So: Del 5VSB_CTRL_L.
Change to use GPIO40_S485

EuP Lot6 Power Saving Circuit



11'0121
Cuz: Change to use SIO+Intel EuP Solution.
So: Add SLP_SUS_L Circuit.

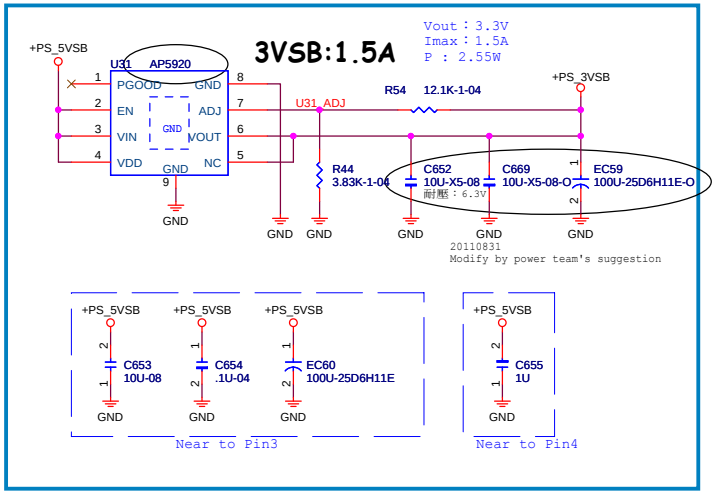
11'0210
Del PCH_MEPWROK Circuit

PCH_MEPWROK Circuit

3VSB (S0):

Power Name	Current
PCH	109mA
LAN RTL8111E-VL	165mA
SIO IT8772EX	6mA
EPW Non-AMT	0mA
SPI Non-AMT	0mA
PCI-E 4 Slots	0.375 X 4 = 1.5A
MINI PCI-E 1 Slots	1.1A
Total Current	0.28 + 2.6 = 2.88A

20111019
Change tp AP5920



Elitegroup Computer Systems

Title	DC/DC 3VDUAL	
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11'0210
Del +V_1P05_ME Power Circuit.

ME 1.05V
MAX 1.8A
+V_1P05_PCH

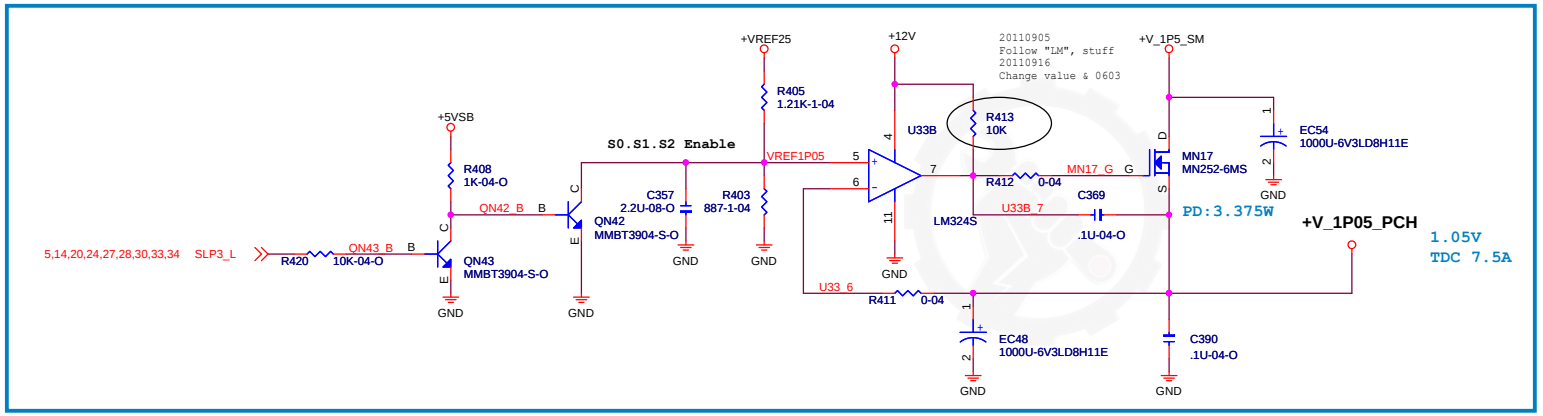
C303 22U-X5-08
C298 22U-X5-08
C290 22U-X5-08-O
C297 1U-16VX

20110915
Change value

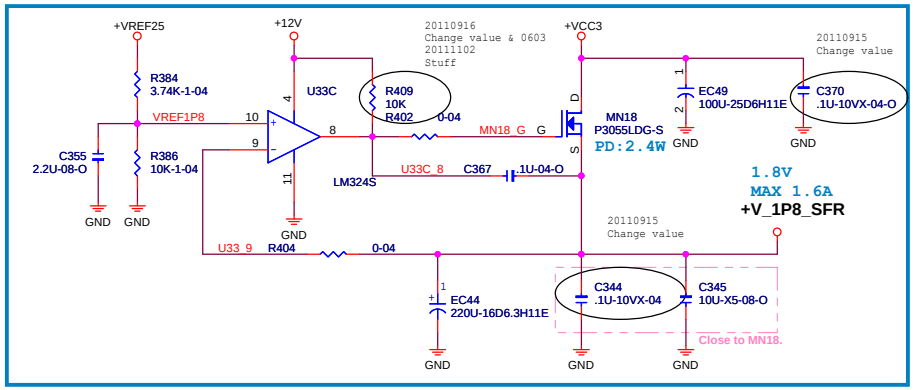
GND

110211
Cuz: Non-AMT
So: Still Need to Stuff these Cap..

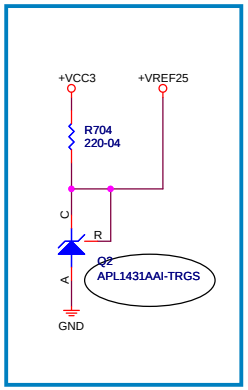
+V_1P05_ME



+V_1P05_PCH



V1P8_SFR(1.6A max)



20110905
Follow "LM", change value

VREF25

02-348-431705
Value:IC REG.APL1431AAI-TRL..SOT-23..2.5V
Footprint: SOT23_RAC_Z_2

Elitegroup Computer Systems

Title	DC/DC V1P05_PCH,ME/V1P8_SFR	
Size: Custom	Document Number: H77H2-EM	Rev: V.A
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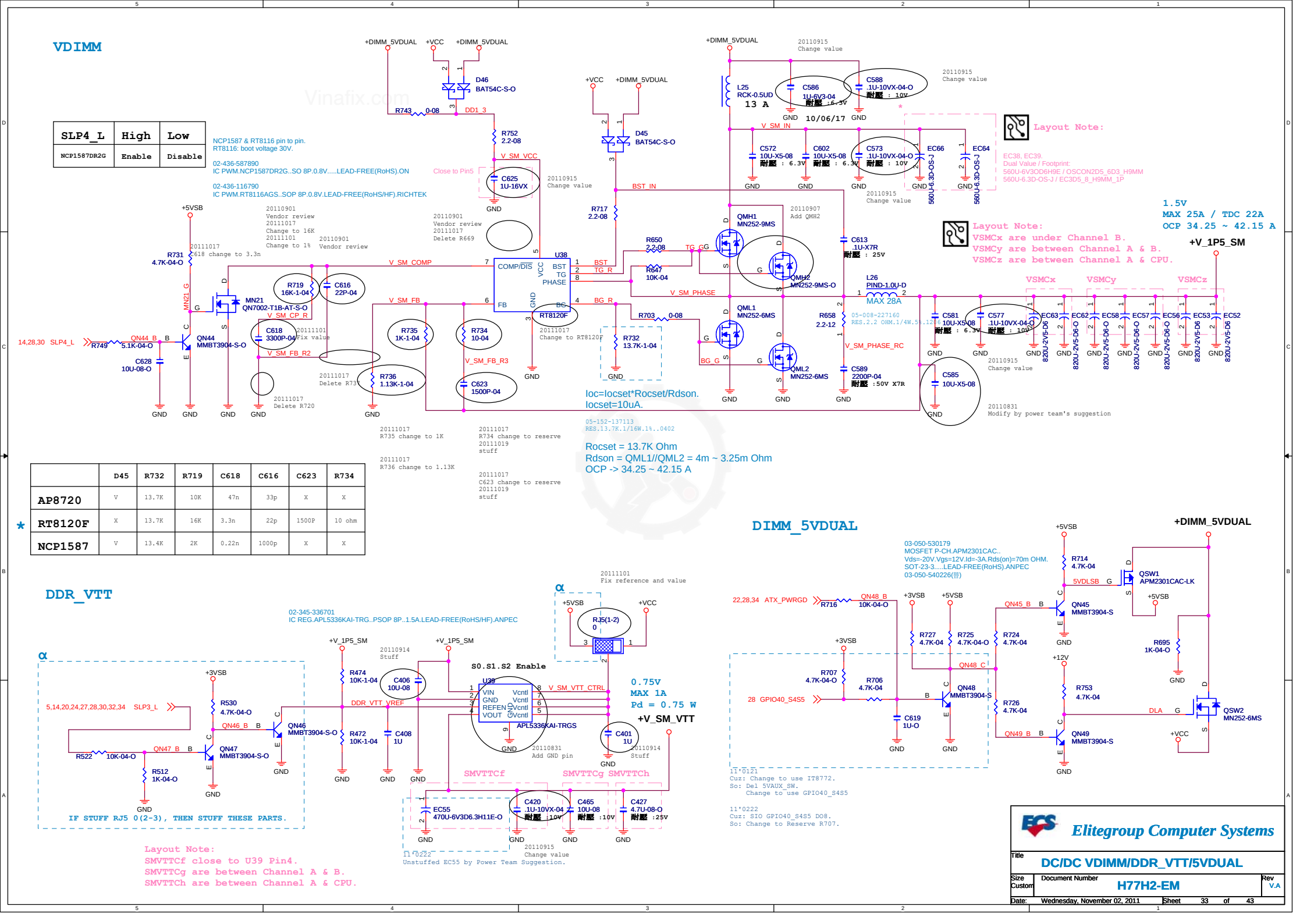
VDIMM
SLP4_L | High | Low
NCP1587DR2G | Enable | Disable
NCP1587 & RT8116 pin to pin.
RT8116: boot voltage 30V.
02-436-587890
IC PWM.NCP1587DR2G..SO 8P.0.8V.....LEAD-FREE(RoHS).ON
02-436-116790
IC PWM.RT8116AGS..SOP 8P.0.8V.LEAD-FREE(RoHS/HF).RICHTEK
+DIMM_5VDUAL
+VCC
D46 BAT54C-S-O
D45 BAT54C-S-O
R743 0-08
DD1_3
R752 2.2-08
V_SM_VCC
C625 1U-16VX
Close to Pin5
20110915 Change value
BST_IN
R717 2.2-08
U38
COMP/DIS
VCC
BST
TG
PHASE
FB
GND
BG
RT8120F
R650 2.2-08
R647 10K-04
TG_G
BST_R
TG_R
BG_R
V_SM_PHASE
R703 0-08
R732 13.7K-1-04
BG_G
QMH1 MN252-9MS
QMH2 MN252-9MS-O
QML1 MN252-6MS
QML2 MN252-6MS
20110907 Add QMH2
L25 RCK-0.5UD 13 A
C586 1U-6V3-04 耐壓 :6.3V
C588 .1U-10VX-04-O 耐壓 : 10V
10/06/17
V_SM_IN
C572 10U-X5-08 耐壓 : 6.3V
C602 10U-X5-08 耐壓 : 6.3V
C573 .1U-10VX-04-O 耐壓 : 10V
EC66 560U-6.3D-OS-J
EC64 560U-6.3D-OS-J
Layout Note:
EC38, EC39.
Dual Value / Footprint:
560U-6V3OD6H9E / OSCON2D5_6D3_H9MM
560U-6.3D-OS-J / EC3D5_8_H9MM_1P
1.5V
MAX 25A / TDC 22A
OCP 34.25 ~ 42.15 A
+V_1P5_SM
Layout Note:
VSMCx are under Channel B.
VSMCy are between Channel A & B.
VSMCz are between Channel A & CPU.
C613 .1U-X7R 耐壓 : 25V
L26 PIND-1.0U-D
MAX 28A
R658 2.2-12
V_SM_PHASE_RC
C589 2200P-04 耐壓 :50V X7R
C581 10U-X5-08 耐壓 : 6.3V
C577 .1U-10VX-04-O 耐壓 : 10V
C585 10U-X5-08
VSMCx
VSMCy
VSMCz
EC63 EC62 EC58 EC57 EC56 EC53 EC52
820U-2V5-D6
20110915 Change value
20110831 Modify by power team's suggestion
+5VSB
R731 4.7K-04-O
MN21_G
MN21 QN7002-T1B-AT-S-O
R719 16K-1-04
C616 22P-04
V_SM_COMP
V_SM_CP_R
C618 3300P-04
20111101 Fix value
V_SM_FB
V_SM_FB_R2
R735 1K-1-04
R734 10-04
V_SM_FB_R3
R736 1.13K-1-04
C623 1500P-04
20111017 Delete R720
20111017 Delete R735
20111017 R735 change to 1K
20111017 R736 change to 1.13K
20111017 R734 change to reserve
20111019 stuff
20111017 C623 change to reserve
20111019 stuff
20110901 Vendor review
20111017 Change to 16K
20111101 Change to 1%
20110901 Vendor review
20110901 Vendor review
20111017 Delete R669
20111017 618 change to 3.3n
14,28,30 SLP4_L
R749 5.1K-04-O
QN44_B
QN44 MMBT3904-S-O
C628 10U-08-O
Ioc=Iocset*Rocset/Rdson.
Iocset=10uA.
05-152-137113
RES.13.7K.1/16W.1%..0402
Rocset = 13.7K Ohm
Rdson = QML1//QML2 = 4m ~ 3.25m Ohm
OCP -> 34.25 ~ 42.15 A
GND
20110831 Modify by power team's suggestion
D45 D46 RT8120F 16K 22P 3300P 1.13K 1500P
AP8720 V 13.7K 10K 47n 33p X X
RT8120F X 13.7K 16K 3.3n 22p 1500P 10 ohm
NCP1587 V 13.4K 2K 0.22n 1000p X X
DDR_VTT
02-345-336701
IC REG.APL5336KAI-TRG..PSOP 8P..1.5A.LEAD-FREE(RoHS/HF).ANPEC
α
+3VSB
+V_1P5_SM
+VCC
+5VSB
RJ5(1-2) 0
R530 4.7K-04-O
5,14,20,24,27,28,30,32,34 SLP3_L
QN46_B
QN46 MMBT3904-S-O
QN47_B
QN47 MMBT3904-S-O
R522 10K-04-O
R512 1K-1-04
IF STUFF RJ5 0(2-3), THEN STUFF THESE PARTS.
R474 10K-1-04
C406 10U-08
20110914 Stuff
S0.S1.S2 Enable
U39
VIN
GND
REFEN
VOUT
Vcntl
APL5336KAI-TRGS
V_SM_VTT_CTRL
DDR_VTT_VREF
R472 10K-1-04
C408 1U
C401 1U
20110914 Stuff
20110831 Add GND pin
0.75V
MAX 1A
Pd = 0.75 W
+V_SM_VTT
SMVTTCf
SMVTTCg SMVTTCh
EC55 470U-6V3D6.3H11E-O
C420 .1U-10VX-04 耐壓 :10V
C465 10U-08 耐壓 :10V
C427 4.7U-08-O 耐壓 :25V
11'0222 Unstuffed EC55 by Power Team Suggestion.
20110915 Change value
Layout Note:
SMVTTCf close to U39 Pin4.
SMVTTCg are between Channel A & B.
SMVTTCh are between Channel A & CPU.
20111101 Fix reference and value
DIMM_5VDUAL
+DIMM_5VDUAL
03-050-530179
MOSFET P-CH.APM2301CAC..
Vds=-20V.Vgs=12V.Id=-3A.Rds(on)=70m OHM.
SOT-23-3.....LEAD-FREE(RoHS).ANPEC
03-050-540226(晉)
22,28,34 ATX_PWRGD
R716 10K-04-O
QN48_B
QN48 MMBT3904-S
R727 4.7K-04
R725 4.7K-04-O
QN48_C
R707 4.7K-04-O
R706 4.7K-04
28 GPIO40_S4S5
C619 1U-O
R714 4.7K-04
5VDLSB
QSW1 APM2301CAC-LK
QN45_B
QN45 MMBT3904-S
R724 4.7K-04
R695 1K-04-O
R726 4.7K-04
QN49_B
QN49 MMBT3904-S
R753 4.7K-04
DLA
QSW2 MN252-6MS
+12V
11'0121
Cuz: Change to use IT8772.
So: Del 5VAUX_SW.
Change to use GPIO40_S4S5
11'0222
Cuz: SIO GPIO40_S4S5 DO8.
So: Change to Reserve R707.
Elitegroup Computer Systems
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DC/DC VDIMM/DDR_VTT/5VDUAL
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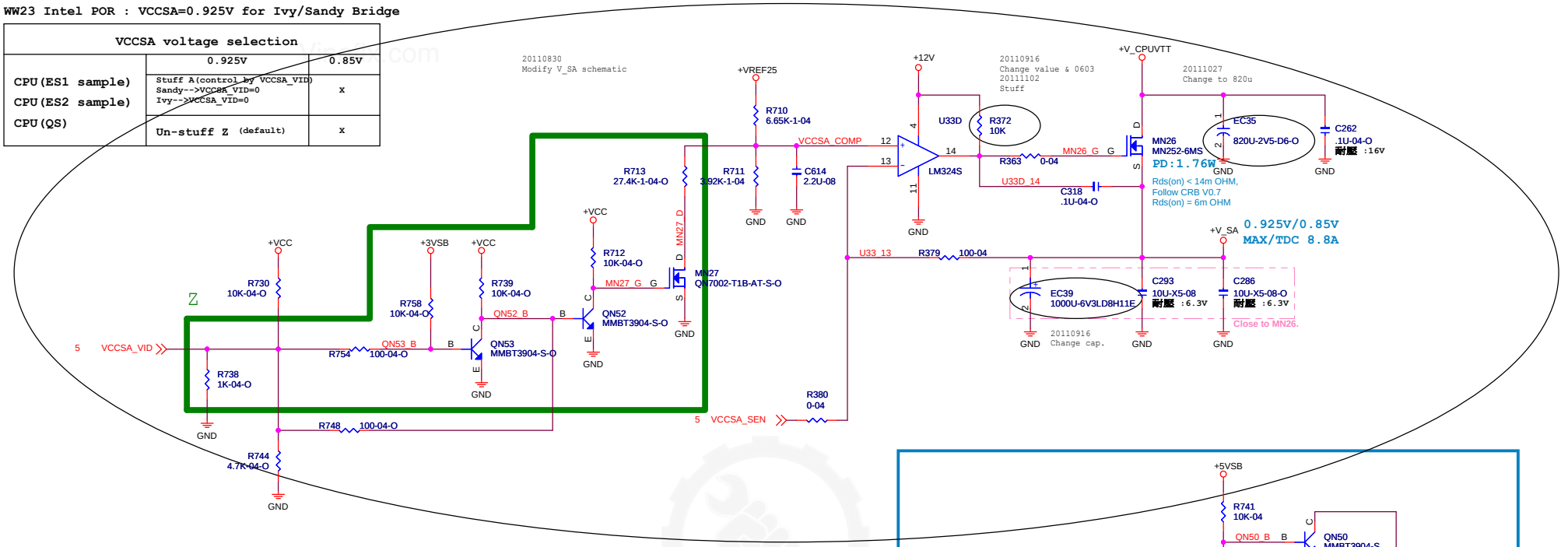
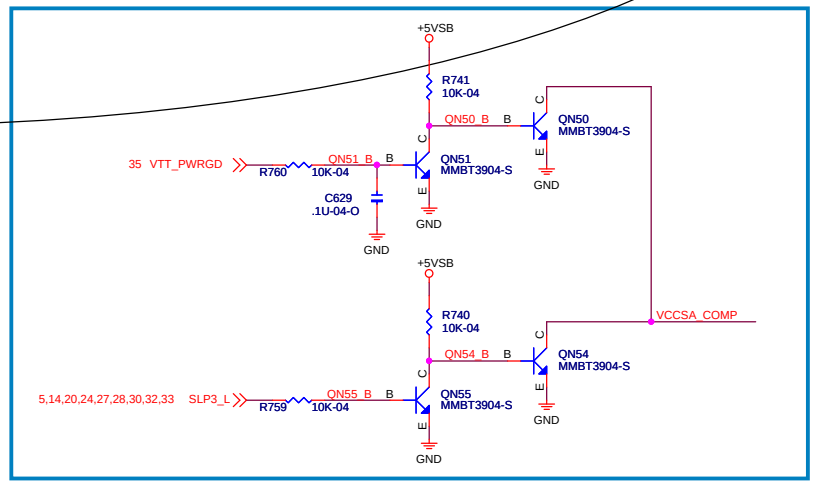
V_SA

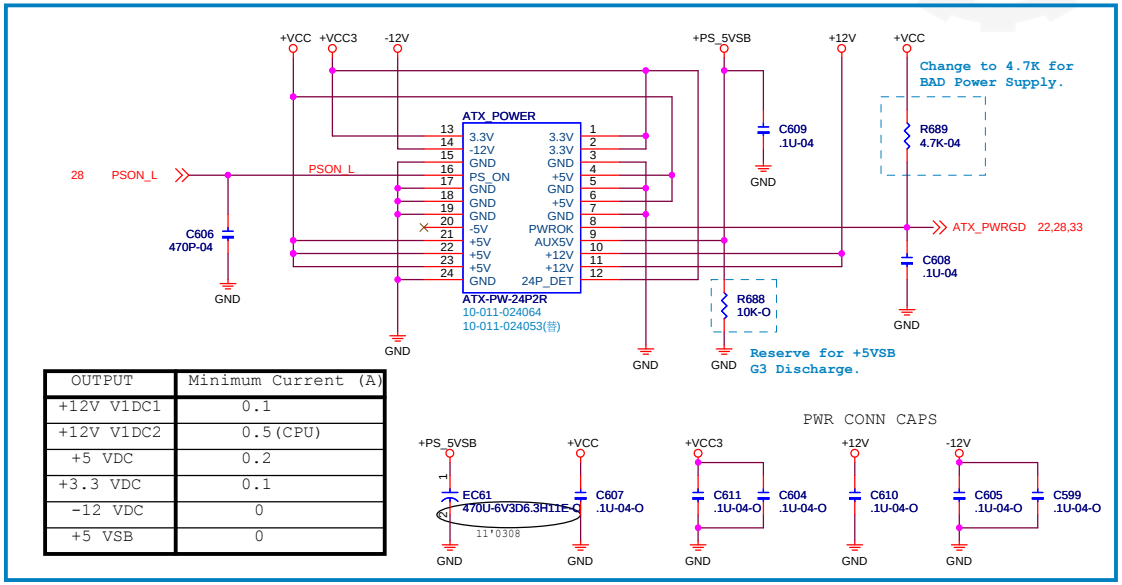
WW23 Intel POR : VCCSA=0.925V for Ivy/Sandy Bridge

VCCSA voltage selection		
	0.925V	0.85V
CPU(ES1 sample) CPU(ES2 sample)	Stuff A(control by VCCSA_VID) Sandy-->VCCSA_VID=0 Ivy-->VCCSA_VID=0	x
CPU(QS)	Un-stuff Z (default)	x



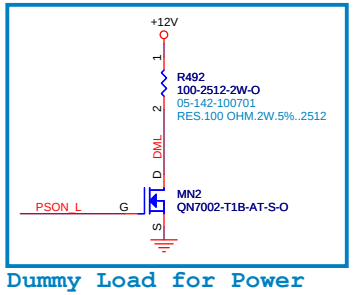


V_SA sequence



OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0

ATX Power 24PIN



Dummy Load for Power

Elitegroup Computer Systems

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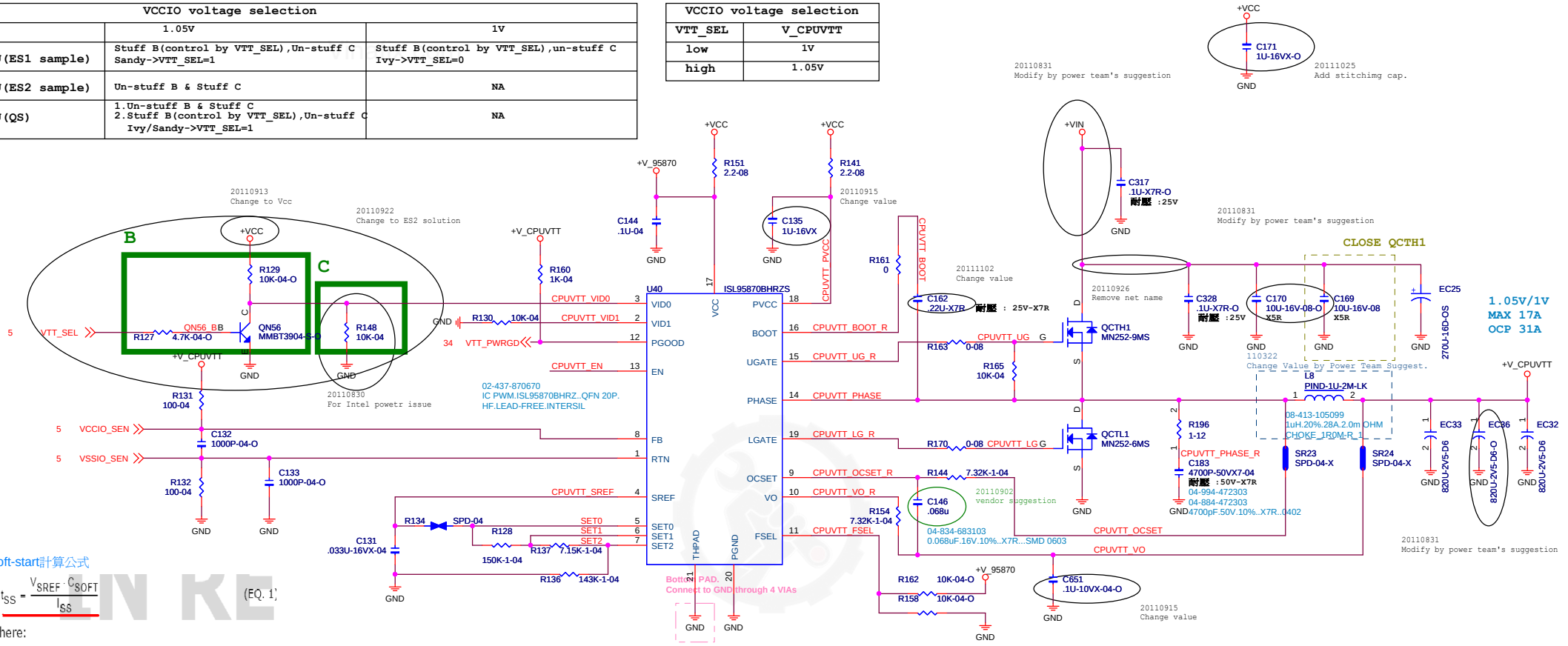
V_CPUVTT

WW23 Intel POR : VCCIO=1.05V for Ivy/Sandy Bridge

VCCIO voltage selection		
	1.05V	1V
CPU(ES1 sample)	Stuff B(control by VTT_SEL),Un-stuff C Sandy->VTT_SEL=1	Stuff B(control by VTT_SEL),un-stuff C Ivy->VTT_SEL=0
CPU(ES2 sample)	Un-stuff B & Stuff C	NA
CPU(QS)	1.Un-stuff B & Stuff C 2.Stuff B(control by VTT_SEL),Un-stuff C Ivy/Sandy->VTT_SEL=1	NA

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad \text{(EQ. 1)}$$

Where:

- I_{SS} is the soft-start current source at the 20µA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad \text{(EQ. 21)}$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 22)}$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 23)}$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \text{(EQ. 24)}$$

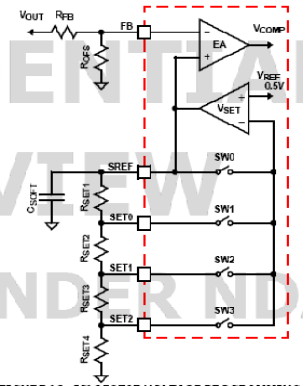


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

Note

1. Rocest = Iout*DCR/Iocset ; Iocset = 10uA
   If DCR = 2m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K
2. Csen = L/Rocset*DCR
   If DCR = 2m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

Elitegroup Computer Systems			
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Black Circle: 20110829 modified for Nph=4 to Nph=3.

Comp. Resistor Setting:

	Ra	Rb
4Phase/95W/112A	169K	23.2K
3Phase/95W/112A	79.8K	450.42K

CLOSE L4
VCORE Gate 1 Output L

CLOSE L20
VAXG Output L

H_SKTOCC_L State

H	CPU Unstuffs in socket
L	CPU Stuffs in socket

VBOOT= 0V Schematic

PROG1 / COMP

RPROG1 (kohm)	VBOOT (V)	ISL6363 IMAX_CR (A), Nph=4	ISL6363 IMAX_CR (A), Nph=3	ISL6363 IMAX_CR (A), Nph=2	ISL6363 IMAX_CR (A), Nph=1
0	Internal (1.1V Default)	92	69	46	23
7080	Internal (1.1V Default)	100	75	50	25
13200	Internal (1.1V Default)	108	81	54	27
20280	Internal (1.1V Default)	116	87	58	29
27120	Internal (1.1V Default)	124	93	62	31
37920	Internal (1.1V Default)	132	99	66	33
51840	Internal (1.1V Default)	140	105	70	35
67440	Internal (1.1V Default)	148	111	74	37
79800	0	148	111	74	37
94440	0	140	105	70	35
114360	0	132	99	66	33
138000	0	124	93	62	31
168000	0	116	87	58	29
198000	0	108	81	54	27
224400	0	100	75	50	25
298800	0	92	69	46	23

For VR_READY Power On Sequence

02-437-363671
Value: IC PWM.ISL6363CRZ..QFN 48P.....LEAD-FREE.INTERSIL
Footprint: QFN48_PT04-4D4X4D4MM

BOTTOM PAD
CONNECT TO GND
Through 8 VIAs

Disable VAXG

ERT-J0EV474J
CLOSE QCH1
CLOSE QCGH1

Elitegroup Computer Systems

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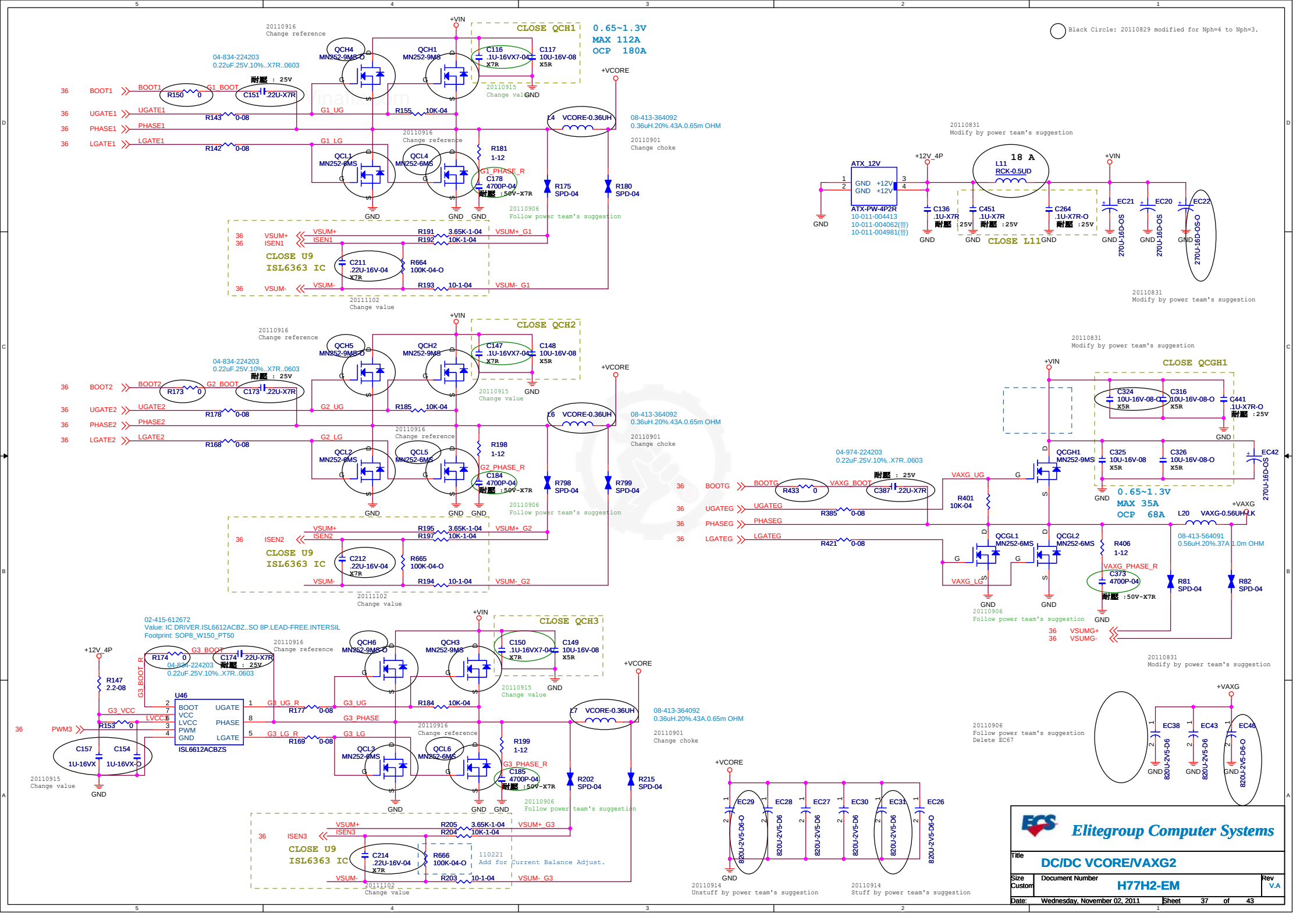
CLOSE QCH1
0.65~1.3V
MAX 112A
OCP 180A
+VIN
+VCORE
QCH4 MN252-9MS-O
QCH1 MN252-9MS
C116 .1U-16VX7-04 X7R
C117 10U-16V-08 X5R
BOOT1
UGATE1
PHASE1
LGATE1
R150 0
R143 0-08
R142 0-08
R155 10K-04
L4 VCORE-0.36UH
08-413-364092
0.36uH.20%.43A.0.65m OHM
QCL1 MN252-6MS
QCL4 MN252-6MS
R181 1-12
G1_PHASE_R
C178 4700P-04
耐壓 :50V-X7R
R175 SPD-04
R180 SPD-04
VSUM+ G1
VSUM- G1
R191 3.65K-1-04
R192 10K-1-04
R193 10-1-04
CLOSE U9
ISL6363 IC
C211 .22U-16V-04 X7R
R664 100K-04-O
CLOSE QCH2
QCH5 MN252-9MS-O
QCH2 MN252-9MS
C147 .1U-16VX7-04 X7R
C148 10U-16V-08 X5R
BOOT2
UGATE2
PHASE2
LGATE2
R173 0
R178 0-08
R168 0-08
R185 10K-04
L6 VCORE-0.36UH
08-413-364092
0.36uH.20%.43A.0.65m OHM
QCL2 MN252-6MS
QCL5 MN252-6MS
R198 1-12
G2_PHASE_R
C184 4700P-04
耐壓 :50V-X7R
R798 SPD-04
R799 SPD-04
VSUM+ G2
VSUM- G2
R195 3.65K-1-04
R197 10K-1-04
R194 10-1-04
CLOSE U9
ISL6363 IC
C212 .22U-16V-04 X7R
R665 100K-04-O
CLOSE QCH3
QCH6 MN252-9MS-O
QCH3 MN252-9MS
C150 .1U-16VX7-04 X7R
C149 10U-16V-08 X5R
+12V_4P
R174 0
C174 .22U-X7R
耐壓 : 25V
R147 2.2-08
G3_BOOT_R
U46
ISL6612ACBZS
BOOT
VCC
LVCC
PWM
GND
UGATE
PHASE
LGATE
PWM3
R153 0
C157 1U-16VX
C154 1U-16VX-O
R177 0-08
R184 10K-04
L7 VCORE-0.36UH
08-413-364092
0.36uH.20%.43A.0.65m OHM
QCL3 MN252-6MS
QCL6 MN252-6MS
R199 1-12
G3_PHASE_R
C185 4700P-04
耐壓 :50V-X7R
R202 SPD-04
R215 SPD-04
VSUM+ G3
VSUM- G3
R205 3.65K-1-04
R204 10K-1-04
R203 10-1-04
CLOSE U9
ISL6363 IC
C214 .22U-16V-04 X7R
R666 100K-04-O
Add for Current Balance Adjust.
ATX_12V
ATX-PW-4P2R
+12V_4P
L11 RCK-0.5UD
18 A
C136 .1U-X7R
C451 .1U-X7R
C264 .1U-X7R-O
EC21 270U-16D-OS
EC20 270U-16D-OS
EC22 270U-16D-OS-O
CLOSE L11
+VAXG
QCGH1 MN252-9MS
C324 10U-16V-08-O X5R
C316 10U-16V-08-O X5R
C441 1U-X7R-O
C325 10U-16V-08 X5R
C326 10U-16V-08-O X5R
EC42 270U-16D-OS
0.65~1.3V
MAX 35A
OCP 68A
L20 VAXG-0.56UH-LK
08-413-564091
0.56uH.20%.37A 1.0m OHM
R433 0
C387 .22U-X7R
R401 10K-04
R385 0-08
R421 0-08
QCGL1 MN252-6MS
QCGL2 MN252-6MS
R406 1-12
VAXG_PHASE_R
C373 4700P-04
R81 SPD-04
R82 SPD-04
VSUMG+
VSUMG-
EC38 820U-2V5-D6
EC43 820U-2V5-D6
EC46 820U-2V5-D6-O
EC29 820U-2V5-D6-O
EC28 820U-2V5-D6
EC27 820U-2V5-D6
EC30 820U-2V5-D6
EC31 820U-2V5-D6
EC26 820U-2V5-D6-O
Black Circle: 20110829 modified for Nph=4 to Nph=3.
Elitegroup Computer Systems
DC/DC VCORE/VAXG2
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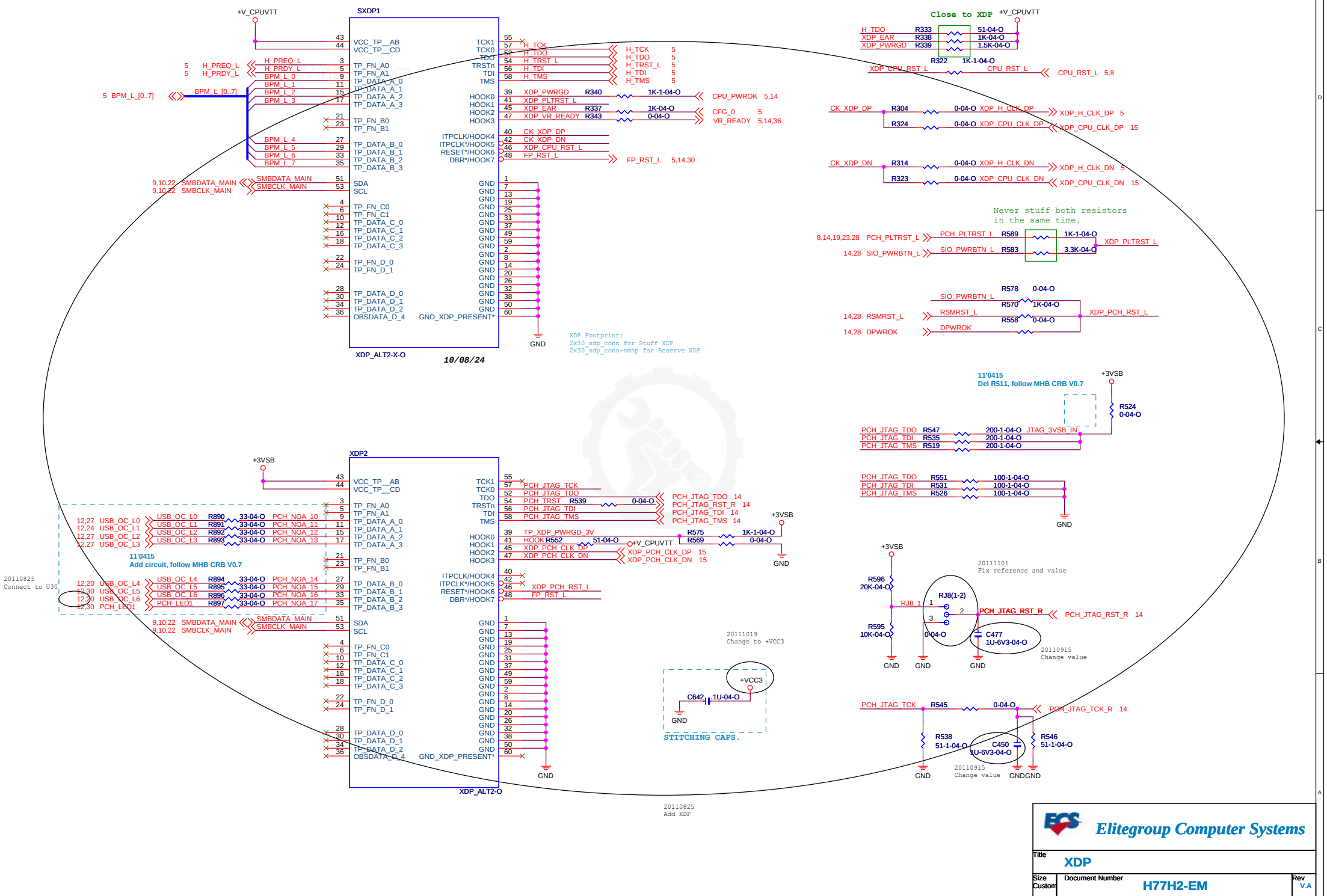
SXDP1
+V_CPUVTT
XDP_ALT2-X-O
10/08/24
XDP Footprint:
2x30_xdp_conn for Stuff XDP
2x30_xdp_conn-nmnp for Reserve XDP
Close to XDP
Never stuff both resistors
in the same time.
11'0415
Del R511, follow MHB CRB V0.7
XDP2
+3VSB
11'0415
Add circuit, follow MHB CRB V0.7
20110825
Connect to U30
20111019
Change to +VCC3
STITCHING CAPS.
20111101
Fix reference and value
20110915
Change value
20110825
Add XDP
XDP_ALT2-O
Elitegroup Computer Systems
XDP
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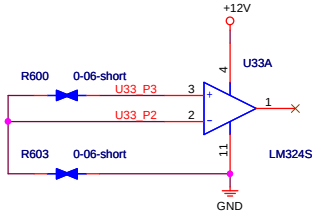
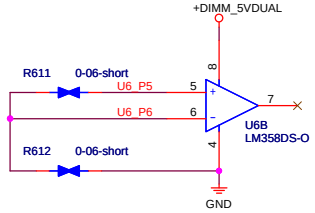
PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down，No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up，intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up，“topblock swap” mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up，Integrated 1.05V VRM Enable
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up，The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up，The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TVS	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Disable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.



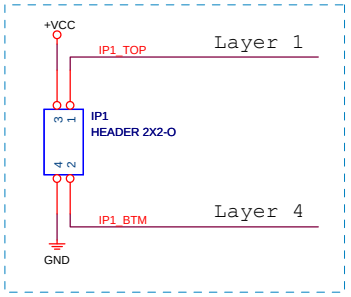


SIO Strap Pin

Power-On Strapping

	Symbol	Value		Description
JP1 Pin-23	DSW_EUP_SEL	1		EUP(default)
		0	*	DSW
JP2 Pin-57	WDT_EN	1	*	Disable WDT to reset PWROK(default)
		0		Enable WDT to reset PWROK
JP3 Pin-59	FAN_CTL_SEL	1	*	EC Index 6Bh/73h default = 80h
		0		EC Index 6Bh/73h default = 00h
JP4 Pin-61	K8PWR_EN	1	*	Disable K8 Power Sequence(default)
		0		Enable K8 Power Sequence

Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)



Impedance Test Header

Elitegroup Computer Systems

Title	STRAPPING	
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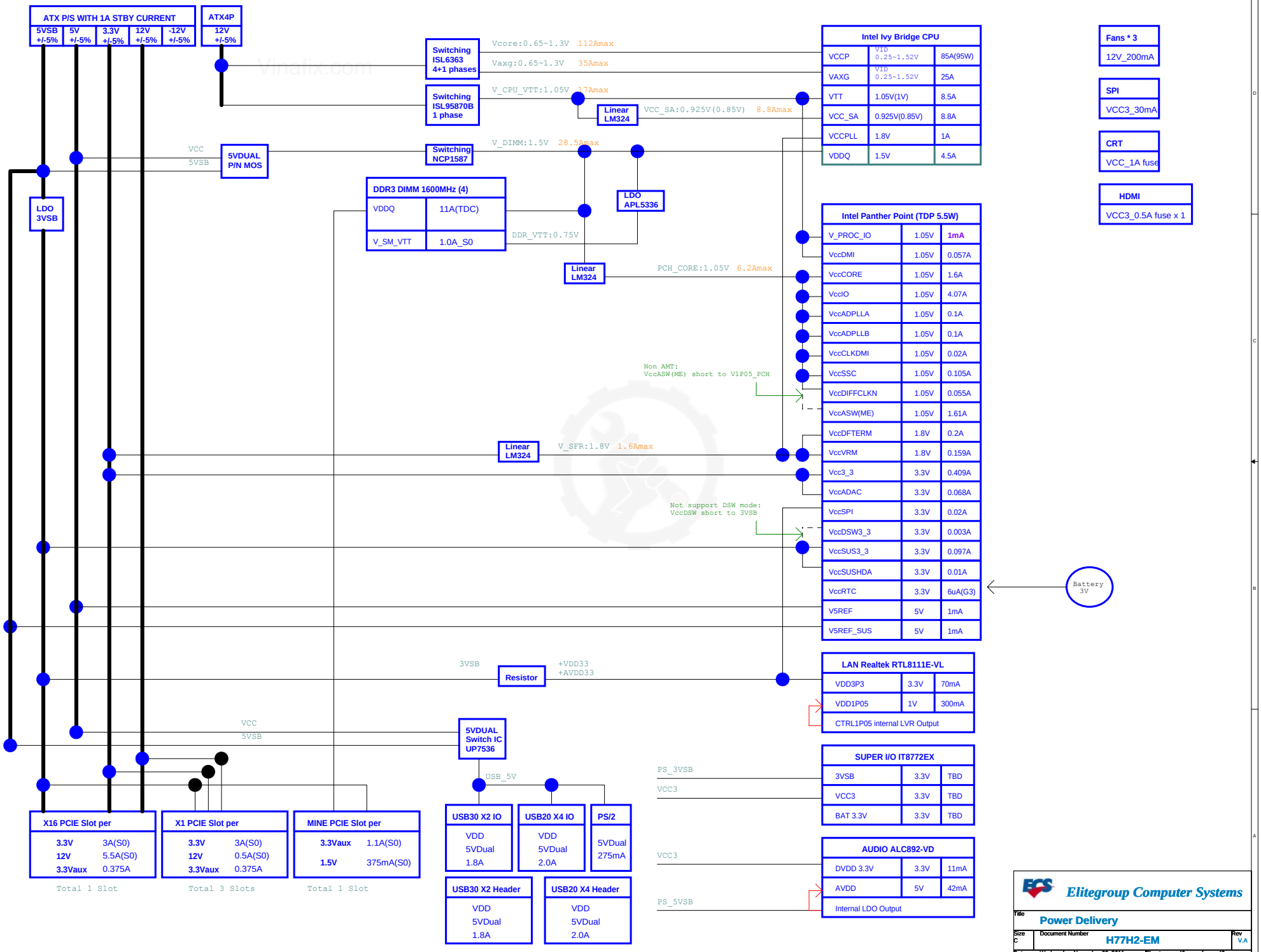
ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
ATX4P
12V +/-5%
Switching ISL6363 4+1 phases
Vcore:0.65~1.3V 112Amax
Vaxg:0.65~1.3V 35Amax
Switching ISL95870B 1 phase
V_CPU_VTT:1.05V 17Amax
Linear LM324
VCC_SA:0.925V(0.85V) 8.8Amax
Intel Ivy Bridge CPU
VCCP VID 0.25~1.52V 85A(95W)
VAXG VID 0.25~1.52V 25A
VTT 1.05V(1V) 8.5A
VCC_SA 0.925V(0.85V) 8.8A
VCCPLL 1.8V 1A
VDDQ 1.5V 4.5A
Fans * 3
12V_200mA
SPI
VCC3_30mA
CRT
VCC_1A fuse
HDMI
VCC3_0.5A fuse x 1
VCC
5VSB
5VDUAL P/N MOS
Switching NCP1587
V_DIMM:1.5V 28.5Amax
LDO 3VSB
DDR3 DIMM 1600MHz (4)
VDDQ 11A(TDC)
V_SM_VTT 1.0A_S0
LDO APL5336
DDR_VTT:0.75V
Linear LM324
PCH_CORE:1.05V 6.2Amax
Intel Panther Point (TDP 5.5W)
V_PROC_IO 1.05V 1mA
VccDMI 1.05V 0.057A
VccCORE 1.05V 1.6A
VccIO 1.05V 4.07A
VccADPLLA 1.05V 0.1A
VccADPLLB 1.05V 0.1A
VccCLKDMI 1.05V 0.02A
VccSSC 1.05V 0.105A
VccDIFFCLKN 1.05V 0.055A
VccASW(ME) 1.05V 1.61A
VccDFTERM 1.8V 0.2A
VccVRM 1.8V 0.159A
Vcc3_3 3.3V 0.409A
VccADAC 3.3V 0.068A
VccSPI 3.3V 0.02A
VccDSW3_3 3.3V 0.003A
VccSUS3_3 3.3V 0.097A
VccSUSHDA 3.3V 0.01A
VccRTC 3.3V 6uA(G3)
V5REF 5V 1mA
V5REF_SUS 5V 1mA
Non AMT:
VccASW(ME) short to V1P05_PCH
Linear LM324
V_SFR:1.8V 1.6Amax
Not support DSW mode:
VccDSW short to 3VSB
Battery 3V
3VSB
Resistor
+VDD33
+AVDD33
LAN Realtek RTL8111E-VL
VDD3P3 3.3V 70mA
VDD1P05 1V 300mA
CTRL1P05 internal LVR Output
VCC
5VSB
5VDUAL Switch IC UP7536
USB_5V
SUPER I/O IT8772EX
PS_3VSB
VCC3
3VSB 3.3V TBD
VCC3 3.3V TBD
BAT 3.3V 3.3V TBD
AUDIO ALC892-VD
VCC3
PS_5VSB
DVDD 3.3V 3.3V 11mA
AVDD 5V 42mA
Internal LDO Output
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 3 Slots
MINE PCIE Slot per
3.3Vaux 1.1A(S0)
1.5V 375mA(S0)
Total 1 Slot
USB30 X2 IO
VDD
5VDual
1.8A
USB20 X4 IO
VDD
5VDual
2.0A
PS/2
5VDual
275mA
USB30 X2 Header
VDD
5VDual
1.8A
USB20 X4 Header
VDD
5VDual
2.0A
Elitegroup Computer Systems
Title
Power Delivery
Size C
Document Number
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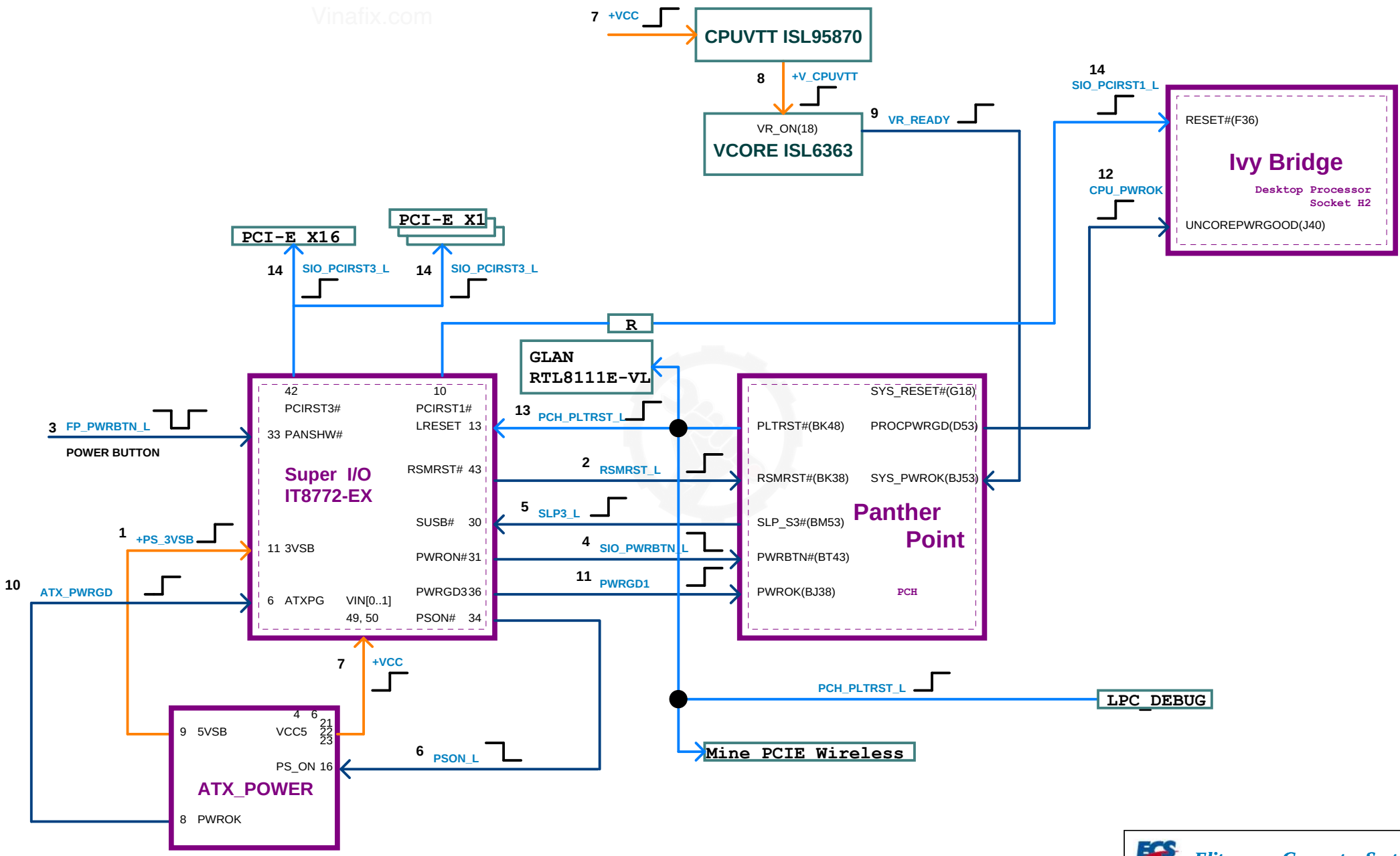

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Title: Power Sequence, Reset Diagram

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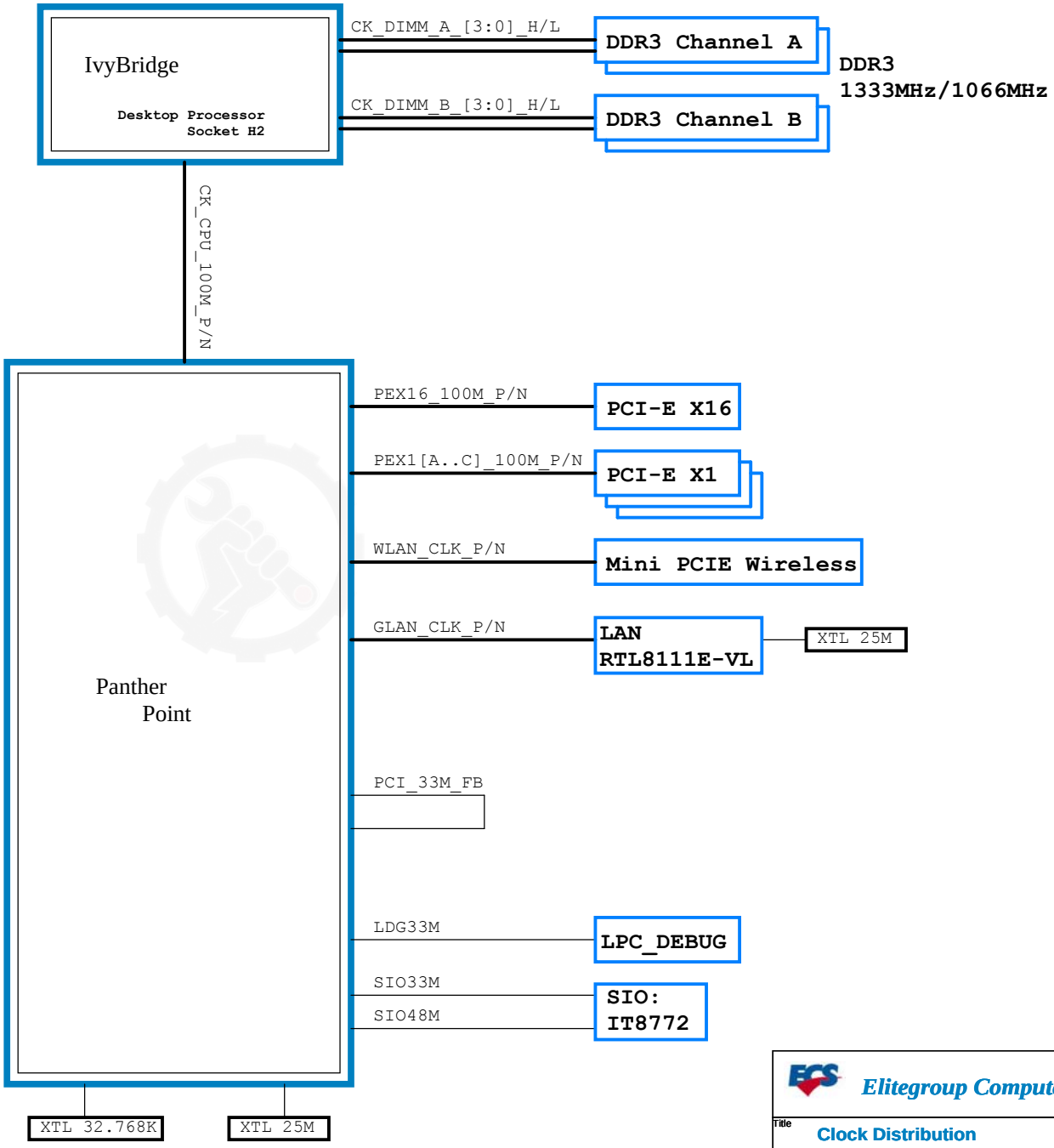

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