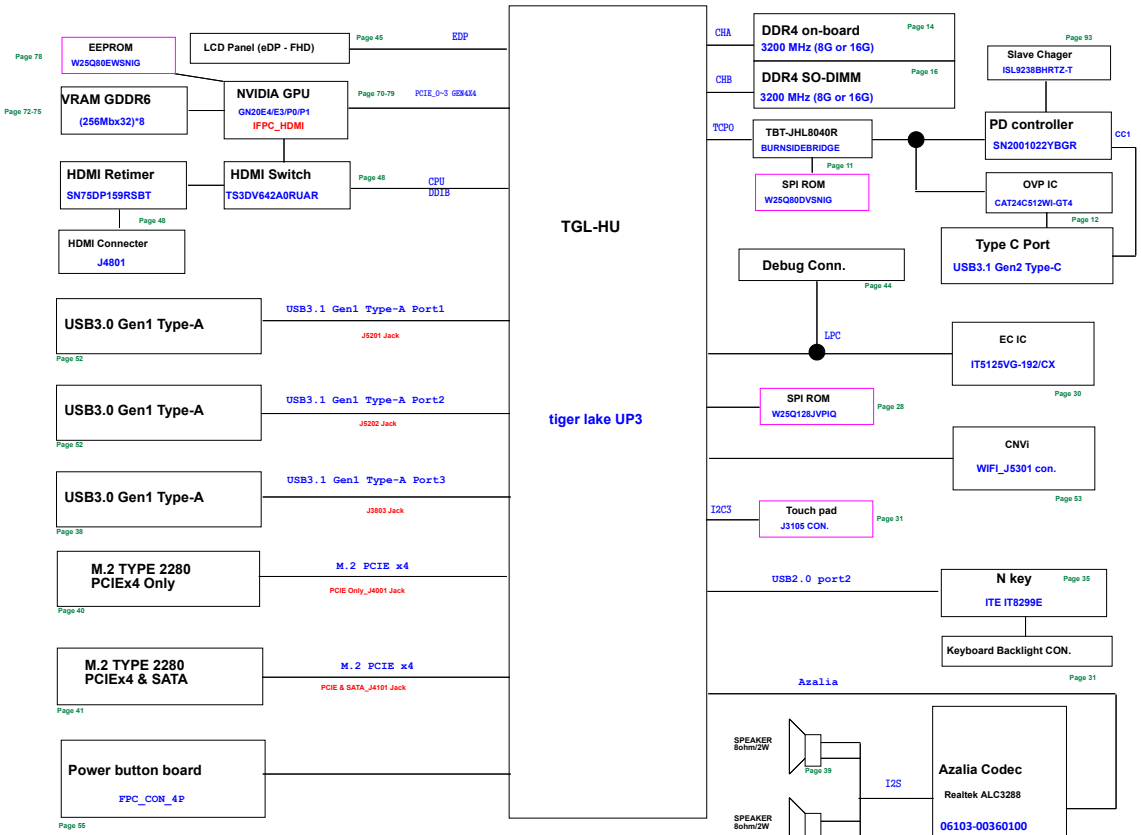
FX516PR SCHEMATIC

SYSTEM PAGE REF.

PAGE	Content
1	Block Diagram
2	System Setting
3	CPU_DMI,PEG,eDP,DDI
4	CPU_DDR
5	CPU_GND
6	CPU_CFG,RSVD
7	CPU_ESPI,SPI,SMB,CLINK
8	CPU_PCH_CSI2,EMMC,CNV
9	CPU_POWER
10	CPU_POWER_CAP
11	TBT_Titan Ridge SP
12	TBT_TPS65994AD&Type C
13	TBT
14	DIM_DDR4_ON-BOARD_A(1)
15	DIM
16	DIM_DDR4 SO-DIMM B(0) TOP
17	DIM_
18	DIM_CA/DQ Voltage
19	DDR4_TERMINATION*
20	PCH_HDA,SMBUS,SYS PWR
21	PCH-CPT(2)_PCIE,USB2,MISC
22	PCH-CPT(3)_CLK,LPC,USB3
23	PCH-CPT(4)_eDP,PCI,DP,MISC
24	PCH-CPT(5)_SPI
25	PCH-CPT(6)_GPIO
26	PCH-CPT(7)_POWER,GND
27	PCH-CPT(8)_POWER,GND
28	PCH-SPI ROM,OTH
30	KBC_IT8995
31	EC_KB_TP
36	AUD-ALC3288
38	Audio_Jack
39	SMART AMP TAS5766M
40	Card Reader AU6465
44	BUG_Debug
45	CRT_LCD Panel_CMOS_DMIC
48	HDMI
51	NGFF_SSD
52	USB Port
53	USB 3.0 MB Type-C
54	G-sensor
56	LED_Indicator
57	DSG_Discharge
58	PRO_PROTECT
60	DC_DC & BAT Conn.
62	ME_Conn & Skew Hole
63	EMI_RF Reserve
64	U3_B2B CONN
66	WLAN&BT SIP
67	LID_Switch / FAN_connector
70	GPU PCIE
71	GPU MEMORY Interface
72	Frame Buffer
74	GPU STRAP
75	GPU GPIO
76	GPU VDD/GND
77	GPU PWG Decopling
78	GPU Power
79	VGA Sensor
80	PW_IMVP8 (1)
81	PW_IMVP8 (2)
83	PW_+1.0VSUS / +1.8VSUS
86	PW_1.2V/+0.6VS
87	PW_+3VADSW/+5VSUS
88	PW_LOAD SWITCH
89	PW_CHARGER(BQ24780)
90	PW_PROTECTION
91	PW_NVVDD
94	PW_VRAM

BLOCK DIAGRAM

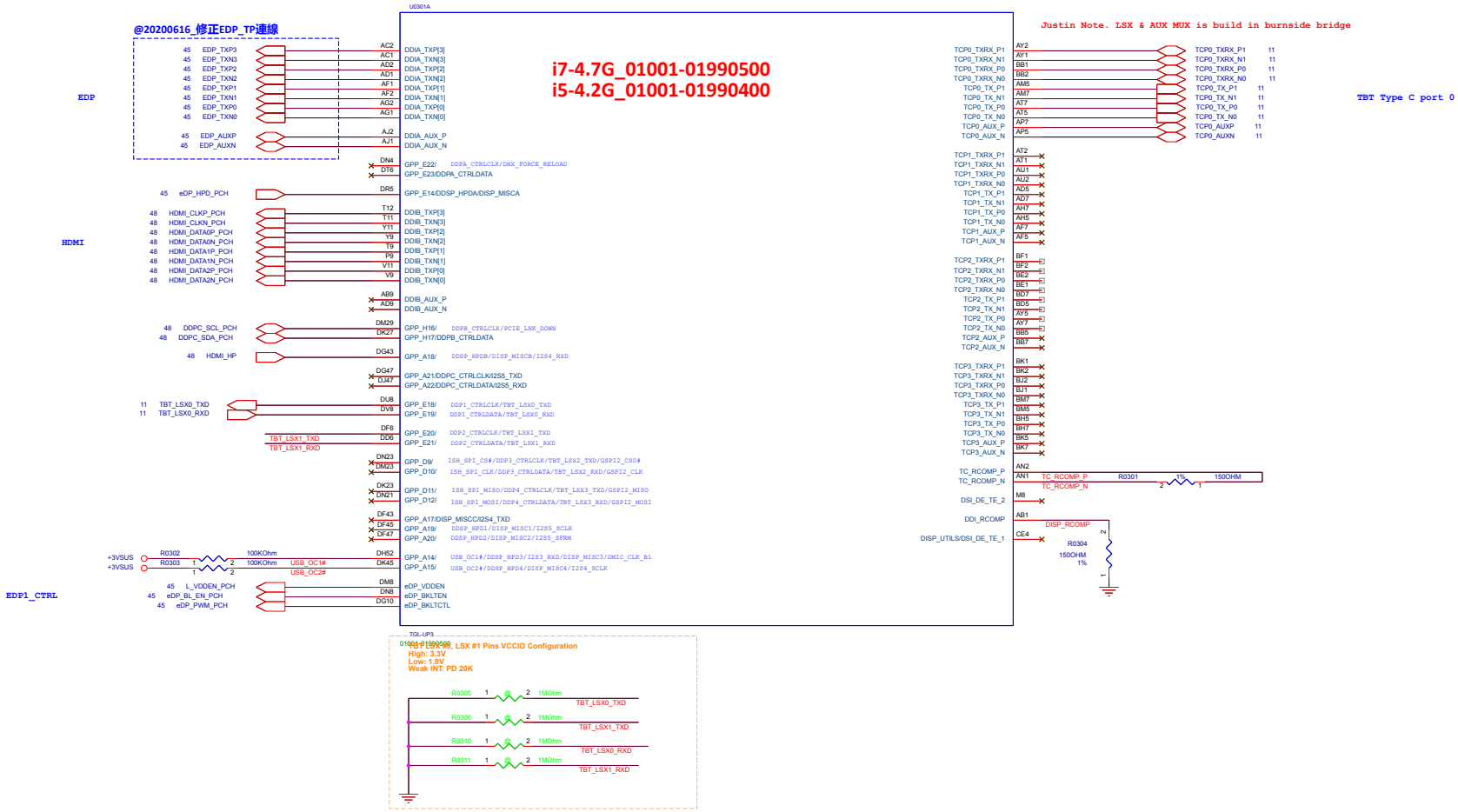


Power

- PW_IMVP9 — Page 80,81
- +3VADSW/+5VSUS — Page 87
- +1.8VSUS — Page 83
- +1.1V — Page 86
- PW +NVVDD — Page 91
- Page 94
- Charger — Page 89
- Load Switch — Page 88

<Variant Name>
Project Name: UX482
Rev: R0.1
Title : Block Diagram
Size: Custom
Dept.: NB1-RD3EE2
Engineer: EE
Date: Friday, October 16, 2020
Sheet 1 of 102

Main Board

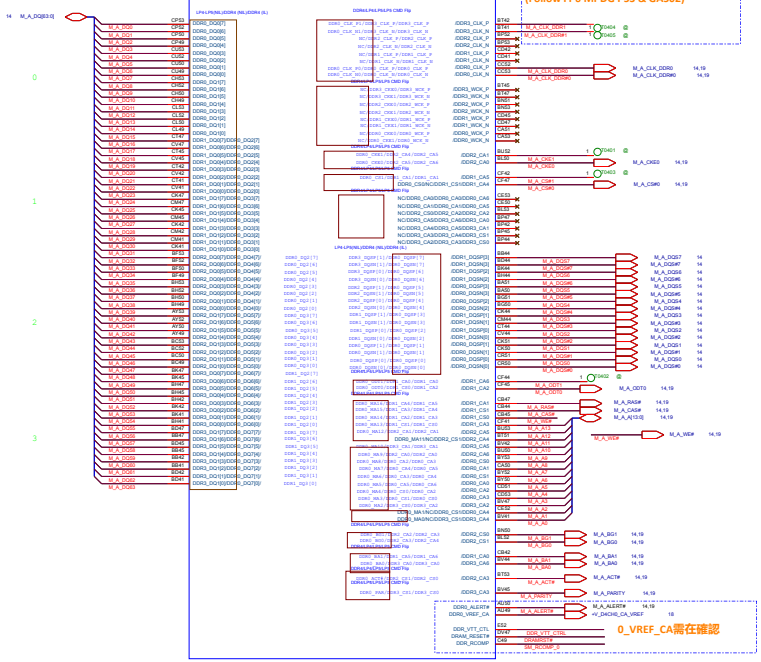

@20200616_修正EDP_TP連線
EDP
HDMI
EDP1_CTRL
U0301A
i7-4.7G_01001-01990500
i5-4.2G_01001-01990400
Justin Note. LSX & AUX MUX is build in burnside bridge
TBT Type C port 0
TGL-UP3
01001-01990500
TBT LSX #0, LSX #1 Pins VCCIO Configuration
High: 3.3V
Low: 1.8V
Weak INT. PD 20K

Memory Channel A

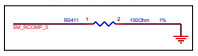
On Board DDR4

MA/B_
I/O-IOMEM-S/D VDDIO_MEM_S3 (S0_1.2)_FP6 (FDS)

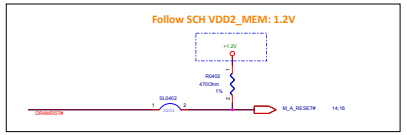
On board 只接一組
(Follow FP6 MPDG P53 & GA502)



LPDDR4X COMPENSATION SIGNALS



Follow SCH VDD2_MEM: 1.2V

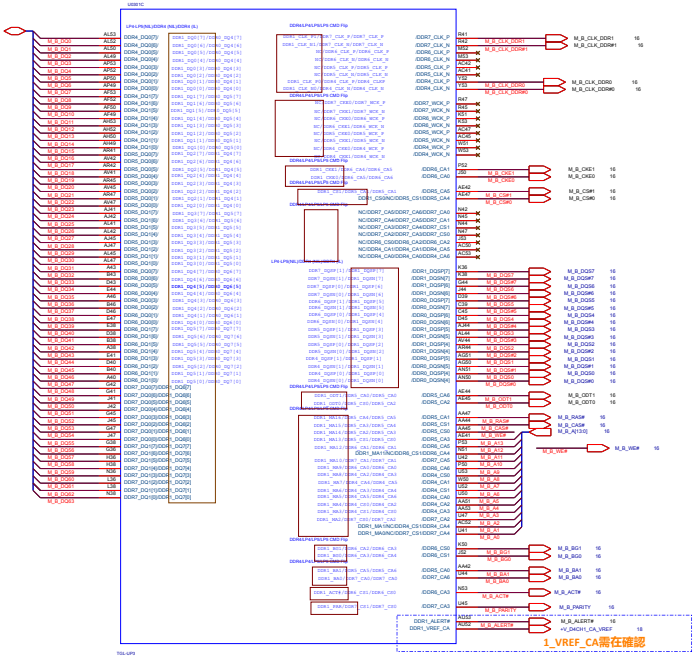


0_VREF_CA需在確認

DDR_VTT CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116

Memory Channel B

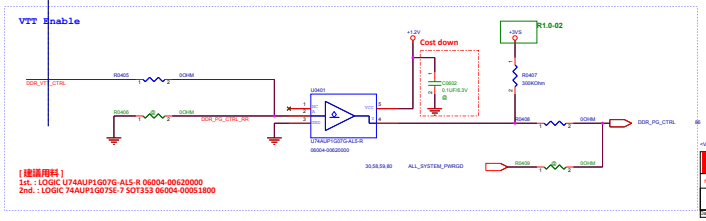
SO-DIMM DDR4



1_VREF_CA需在確認

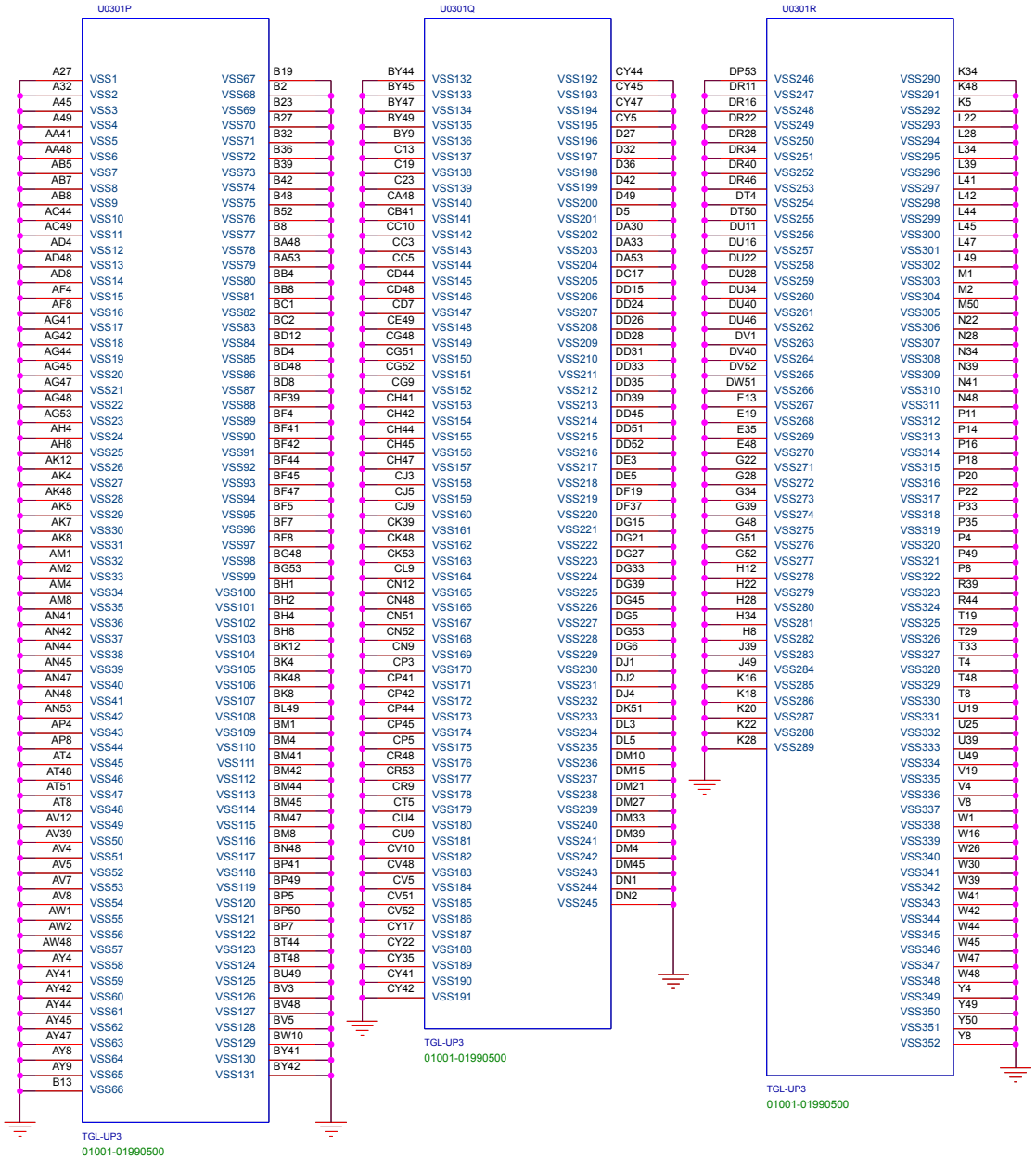
Main Board

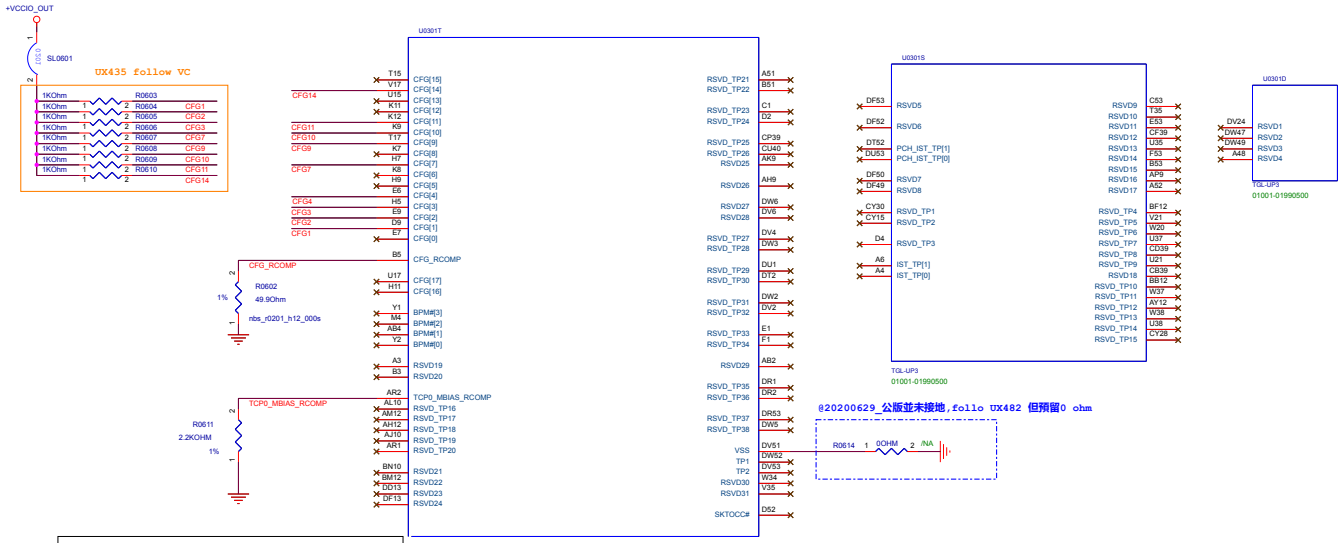
VTT Enable

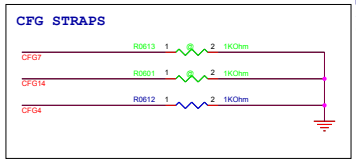


[建議用料]
1st. : LOGIC U74AUP1G07G-AL5-R 06004-00620000
2nd. : LOGIC 74AUP1G07SE-7 SOT353 06004-00051800

Title :	CPU_DDR4
Engineer:	EE
Size: Custom	Project Name: UX482
Rev:	00.1
Date: Friday, October 16, 2020	Sheet 4 of 102


U0301P
A27 A32 A45 A49 AA41 AA48 AB5 AB7 AB8 AC44 AC49 AD4 AD48 AD8 AF4 AF8 AG41 AG42 AG44 AG45 AG47 AG48 AG53 AH4 AH8 AK12 AK4 AK48 AK5 AK7 AK8 AM1 AM2 AM4 AM8 AN41 AN42 AN44 AN45 AN47 AN48 AN53 AP4 AP8 AT4 AT48 AT51 AT8 AV12 AV39 AV4 AV5 AV7 AV8 AW1 AW2 AW48 AY4 AY41 AY42 AY44 AY45 AY47 AY8 AY9 B13
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57 VSS58 VSS59 VSS60 VSS61 VSS62 VSS63 VSS64 VSS65 VSS66
VSS67 VSS68 VSS69 VSS70 VSS71 VSS72 VSS73 VSS74 VSS75 VSS76 VSS77 VSS78 VSS79 VSS80 VSS81 VSS82 VSS83 VSS84 VSS85 VSS86 VSS87 VSS88 VSS89 VSS90 VSS91 VSS92 VSS93 VSS94 VSS95 VSS96 VSS97 VSS98 VSS99 VSS100 VSS101 VSS102 VSS103 VSS104 VSS105 VSS106 VSS107 VSS108 VSS109 VSS110 VSS111 VSS112 VSS113 VSS114 VSS115 VSS116 VSS117 VSS118 VSS119 VSS120 VSS121 VSS122 VSS123 VSS124 VSS125 VSS126 VSS127 VSS128 VSS129 VSS130 VSS131
B19 B2 B23 B27 B32 B36 B39 B42 B48 B52 B8 BA48 BA53 BB4 BB8 BC1 BC2 BD12 BD4 BD48 BD8 BF39 BF4 BF41 BF42 BF44 BF45 BF47 BF5 BF7 BF8 BG48 BG53 BH1 BH2 BH4 BH8 BK12 BK4 BK48 BK8 BL49 BM1 BM4 BM41 BM42 BM44 BM45 BM47 BM8 BN48 BP41 BP49 BP5 BP50 BP7 BT44 BT48 BU49 BV3 BV48 BV5 BW10 BY41 BY42
TGL-UP3
01001-01990500
U0301Q
BY44 BY45 BY47 BY49 BY9 C13 C19 C23 CA48 CB41 CC10 CC3 CC5 CD44 CD48 CD7 CE49 CG48 CG51 CG52 CG9 CH41 CH42 CH44 CH45 CH47 CJ3 CJ5 CJ9 CK39 CK48 CK53 CL9 CN12 CN48 CN51 CN52 CN9 CP3 CP41 CP42 CP44 CP45 CP5 CR48 CR53 CR9 CT5 CU4 CU9 CV10 CV48 CV5 CV51 CV52 CY17 CY22 CY35 CY41 CY42
VSS132 VSS133 VSS134 VSS135 VSS136 VSS137 VSS138 VSS139 VSS140 VSS141 VSS142 VSS143 VSS144 VSS145 VSS146 VSS147 VSS148 VSS149 VSS150 VSS151 VSS152 VSS153 VSS154 VSS155 VSS156 VSS157 VSS158 VSS159 VSS160 VSS161 VSS162 VSS163 VSS164 VSS165 VSS166 VSS167 VSS168 VSS169 VSS170 VSS171 VSS172 VSS173 VSS174 VSS175 VSS176 VSS177 VSS178 VSS179 VSS180 VSS181 VSS182 VSS183 VSS184 VSS185 VSS186 VSS187 VSS188 VSS189 VSS190 VSS191
VSS192 VSS193 VSS194 VSS195 VSS196 VSS197 VSS198 VSS199 VSS200 VSS201 VSS202 VSS203 VSS204 VSS205 VSS206 VSS207 VSS208 VSS209 VSS210 VSS211 VSS212 VSS213 VSS214 VSS215 VSS216 VSS217 VSS218 VSS219 VSS220 VSS221 VSS222 VSS223 VSS224 VSS225 VSS226 VSS227 VSS228 VSS229 VSS230 VSS231 VSS232 VSS233 VSS234 VSS235 VSS236 VSS237 VSS238 VSS239 VSS240 VSS241 VSS242 VSS243 VSS244 VSS245
CY44 CY45 CY47 CY5 D27 D32 D36 D42 D49 D5 DA30 DA33 DA53 DC17 DD15 DD24 DD26 DD28 DD31 DD33 DD35 DD39 DD45 DD51 DD52 DE3 DE5 DF19 DF37 DG15 DG21 DG27 DG33 DG39 DG45 DG5 DG53 DG6 DJ1 DJ2 DJ4 DK51 DL3 DL5 DM10 DM15 DM21 DM27 DM33 DM39 DM4 DM45 DN1 DN2
TGL-UP3
01001-01990500
U0301R
DP53 DR11 DR16 DR22 DR28 DR34 DR40 DR46 DT4 DT50 DU11 DU16 DU22 DU28 DU34 DU40 DU46 DV1 DV40 DV52 DW51 E13 E19 E35 E48 G22 G28 G34 G39 G48 G51 G52 H12 H22 H28 H34 H8 J39 J49 K16 K18 K20 K22 K28
VSS246 VSS247 VSS248 VSS249 VSS250 VSS251 VSS252 VSS253 VSS254 VSS255 VSS256 VSS257 VSS258 VSS259 VSS260 VSS261 VSS262 VSS263 VSS264 VSS265 VSS266 VSS267 VSS268 VSS269 VSS270 VSS271 VSS272 VSS273 VSS274 VSS275 VSS276 VSS277 VSS278 VSS279 VSS280 VSS281 VSS282 VSS283 VSS284 VSS285 VSS286 VSS287 VSS288 VSS289
VSS290 VSS291 VSS292 VSS293 VSS294 VSS295 VSS296 VSS297 VSS298 VSS299 VSS300 VSS301 VSS302 VSS303 VSS304 VSS305 VSS306 VSS307 VSS308 VSS309 VSS310 VSS311 VSS312 VSS313 VSS314 VSS315 VSS316 VSS317 VSS318 VSS319 VSS320 VSS321 VSS322 VSS323 VSS324 VSS325 VSS326 VSS327 VSS328 VSS329 VSS330 VSS331 VSS332 VSS333 VSS334 VSS335 VSS336 VSS337 VSS338 VSS339 VSS340 VSS341 VSS342 VSS343 VSS344 VSS345 VSS346 VSS347 VSS348 VSS349 VSS350 VSS351 VSS352
K34 K48 K5 L22 L28 L34 L39 L41 L42 L44 L45 L47 L49 M1 M2 M50 N22 N28 N34 N39 N41 N48 P11 P14 P16 P18 P20 P22 P33 P35 P4 P49 P8 R39 R44 T19 T29 T33 T4 T48 T8 U19 U25 U39 U49 V19 V4 V8 W1 W16 W26 W30 W39 W41 W42 W44 W45 W47 W48 Y4 Y49 Y50 Y8
TGL-UP3
01001-01990500

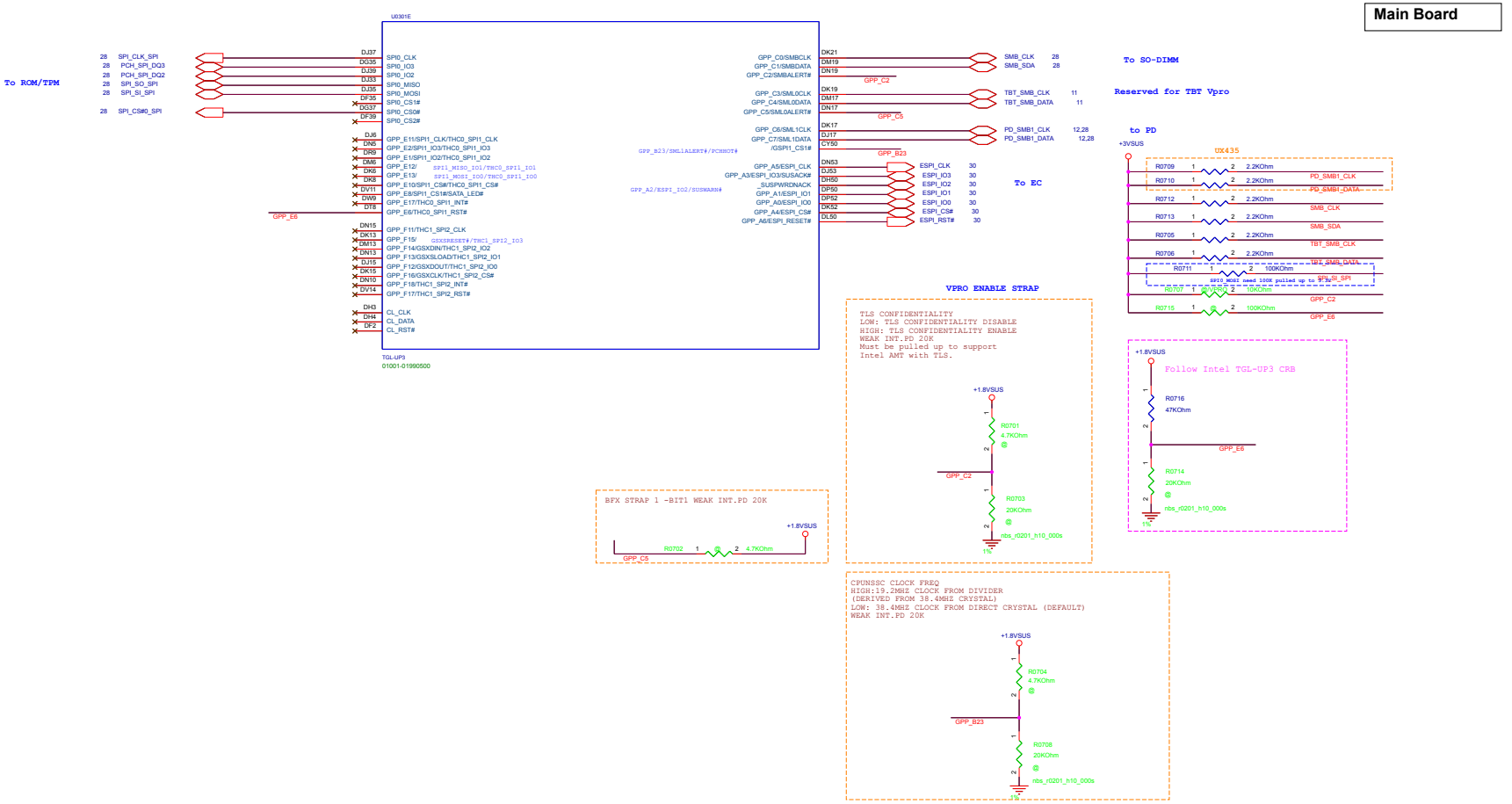




	1	0	NOTE
CFG4	DISABLE	ENABLE	eDP ENABLE

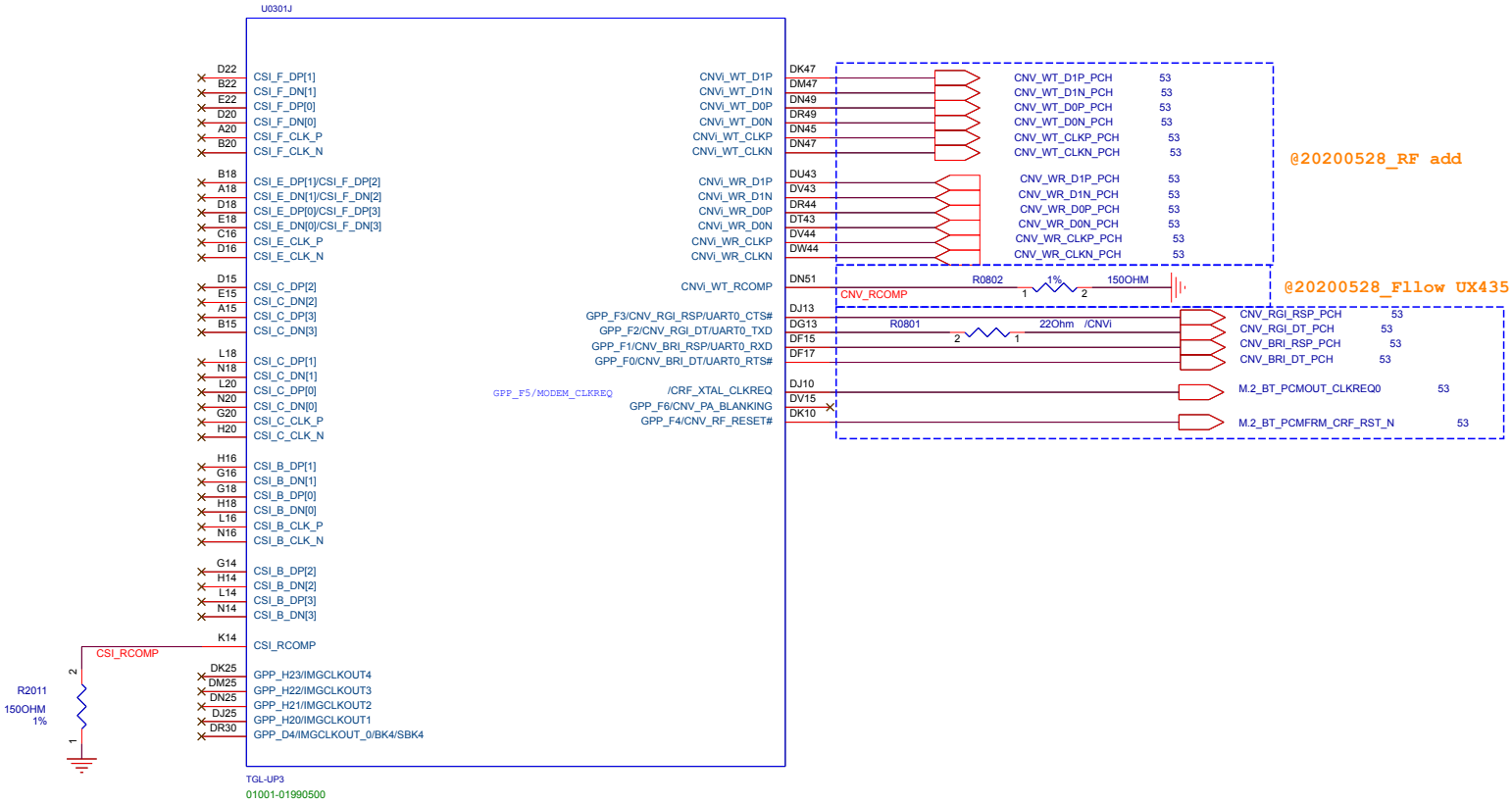
CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

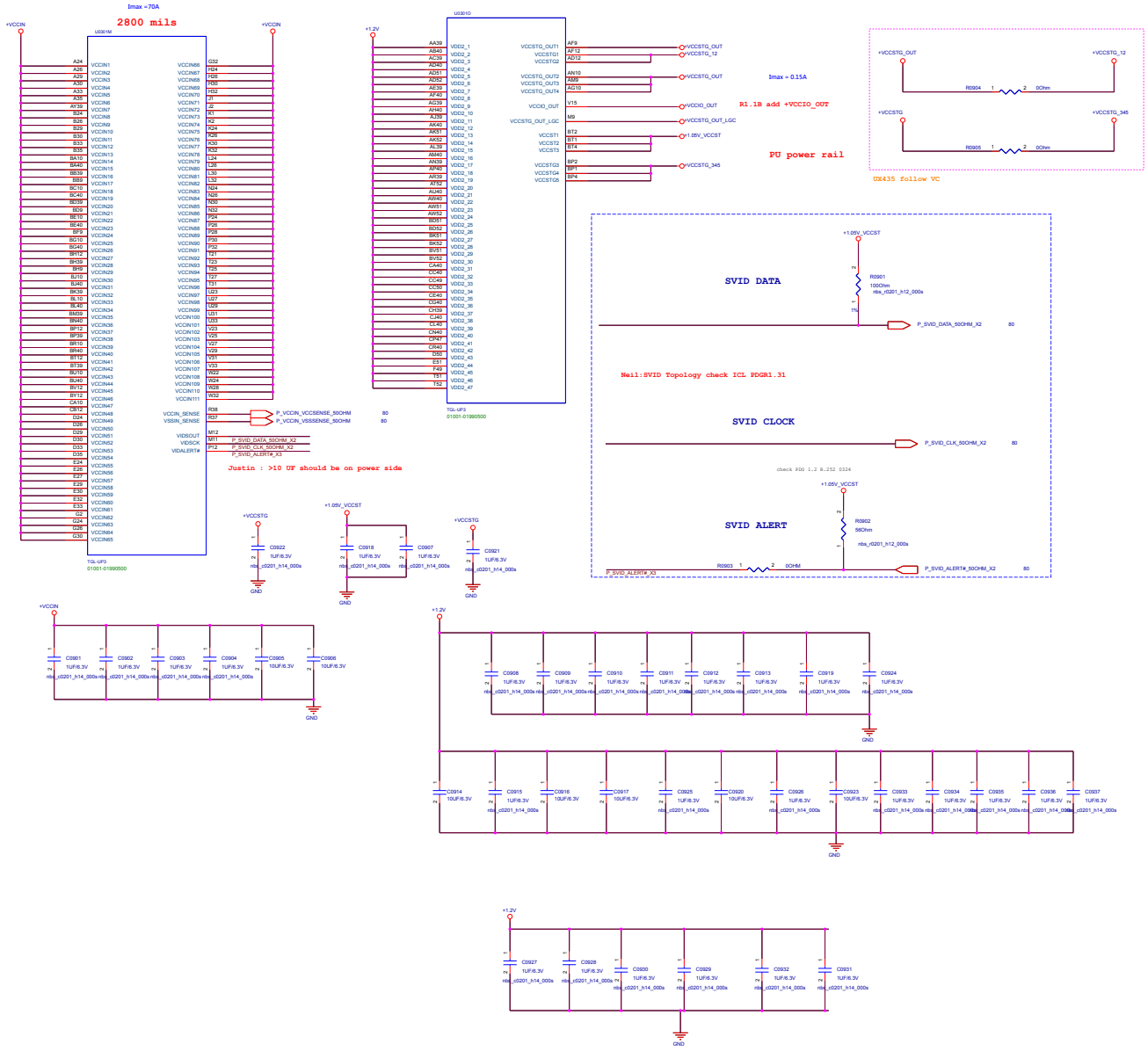
Main Board



<Variant Name>

ASUS	Project Name: UX482	Rev: R0.1
Title : CPU_LPC,SPI,SMB,CLINK		
Size: C	Dept.: NB1-RD3EE2	Engineer: EE
Date: Friday, October 16, 2020	Sheet 7 of 102	

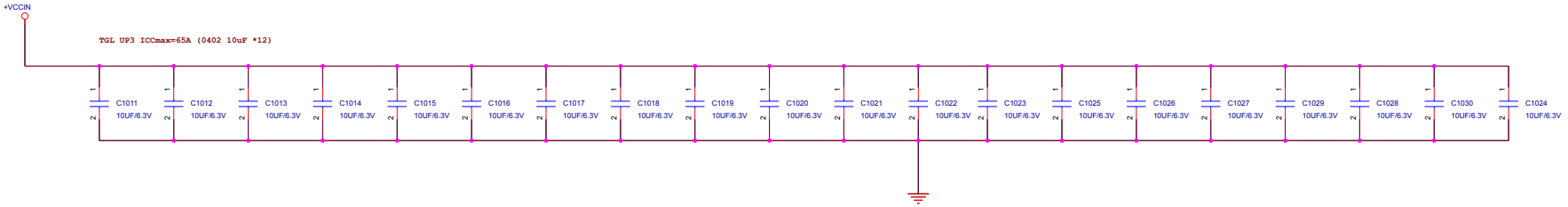

U0301J
D22 CSI_F_DP[1]
B22 CSI_F_DN[1]
E22 CSI_F_DP[0]
D20 CSI_F_DN[0]
A20 CSI_F_CLK_P
B20 CSI_F_CLK_N
B18 CSI_E_DP[1]/CSI_F_DP[2]
A18 CSI_E_DN[1]/CSI_F_DN[2]
D18 CSI_E_DP[0]/CSI_F_DP[3]
E18 CSI_E_DN[0]/CSI_F_DN[3]
C16 CSI_E_CLK_P
D16 CSI_E_CLK_N
D15 CSI_C_DP[2]
E15 CSI_C_DN[2]
A15 CSI_C_DP[3]
B15 CSI_C_DN[3]
L18 CSI_C_DP[1]
N18 CSI_C_DN[1]
L20 CSI_C_DP[0]
N20 CSI_C_DN[0]
G20 CSI_C_CLK_P
H20 CSI_C_CLK_N
H16 CSI_B_DP[1]
G16 CSI_B_DN[1]
G18 CSI_B_DP[0]
H18 CSI_B_DN[0]
L16 CSI_B_CLK_P
N16 CSI_B_CLK_N
G14 CSI_B_DP[2]
H14 CSI_B_DN[2]
L14 CSI_B_DP[3]
N14 CSI_B_DN[3]
K14 CSI_RCOMP
CSI_RCOMP
R2011
150OHM
1%
DK25 GPP_H23/IMGCLKOUT4
DM25 GPP_H22/IMGCLKOUT3
DN25 GPP_H21/IMGCLKOUT2
DJ25 GPP_H20/IMGCLKOUT1
DR30 GPP_D4/IMGCLKOUT_0/BK4/SBK4
TGL-UP3
01001-01990500
CNVi_WT_D1P DK47
CNVi_WT_D1N DM47
CNVi_WT_D0P DN49
CNVi_WT_D0N DR49
CNVi_WT_CLKP DN45
CNVi_WT_CLKN DN47
CNVi_WR_D1P DU43
CNVi_WR_D1N DV43
CNVi_WR_D0P DR44
CNVi_WR_D0N DT43
CNVi_WR_CLKP DV44
CNVi_WR_CLKN DW44
CNVi_WT_RCOMP DN51
GPP_F3/CNV_RGI_RSP/UART0_CTS# DJ13
GPP_F2/CNV_RGI_DT/UART0_TXD DG13
GPP_F1/CNV_BRI_RSP/UART0_RXD DF15
GPP_F0/CNV_BRI_DT/UART0_RTS# DF17
GPP_F5/MODEM_CLKREQ /CRF_XTAL_CLKREQ DJ10
GPP_F6/CNV_PA_BLANKING DV15
GPP_F4/CNV_RF_RESET# DK10
CNV_WT_D1P_PCH 53
CNV_WT_D1N_PCH 53
CNV_WT_D0P_PCH 53
CNV_WT_D0N_PCH 53
CNV_WT_CLKP_PCH 53
CNV_WT_CLKN_PCH 53
CNV_WR_D1P_PCH 53
CNV_WR_D1N_PCH 53
CNV_WR_D0P_PCH 53
CNV_WR_D0N_PCH 53
CNV_WR_CLKP_PCH 53
CNV_WR_CLKN_PCH 53
@20200528_RF add
R0802 1% 150OHM
CNV_RCOMP
@20200528_Fllow UX435
R0801 22Ohm /CNVi
CNV_RGI_RSP_PCH 53
CNV_RGI_DT_PCH 53
CNV_BRI_RSP_PCH 53
CNV_BRI_DT_PCH 53
M.2_BT_PCMOUT_CLKREQ0 53
M.2_BT_PCMFRM_CRF_RST_N 53



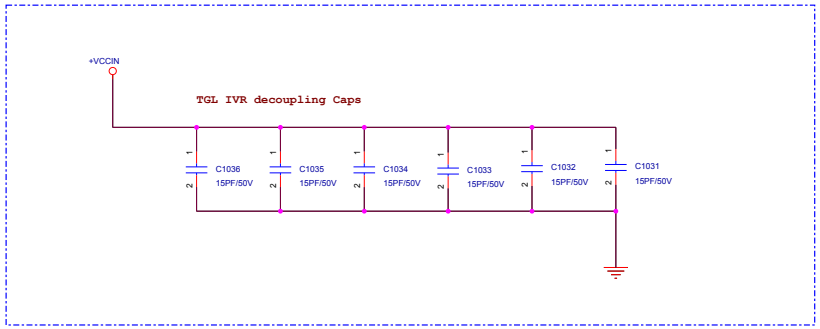
<Variant Name>

Project Name
UX482

CPU - VCCIN DECAPS- Underneath the package

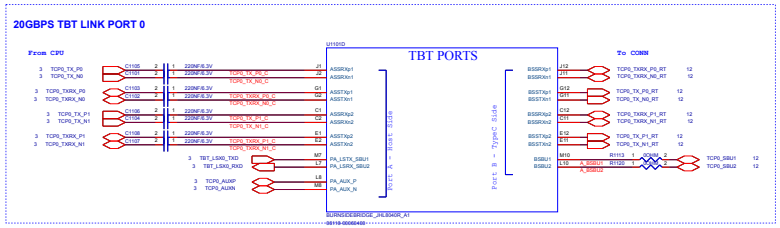


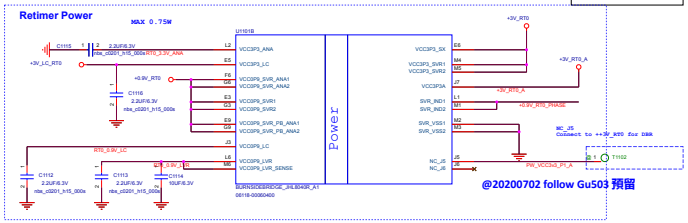
@20200616_add C1031~36: 15PF for EMI/RF

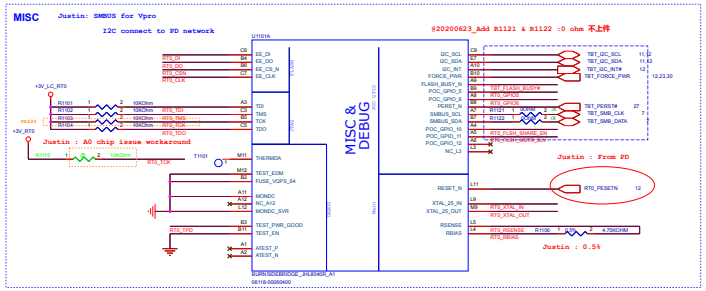


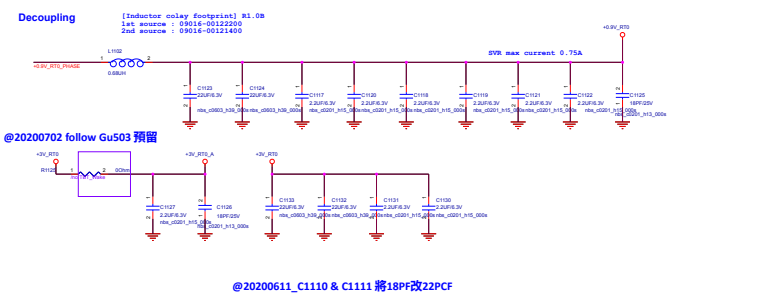
Project Name: UX482		Rev: R0.1
Title : CPU_POWER_CAP		
Size: C	Dept.: NB1-RD3EE2	Engineer: EE
Date: Friday, October 16, 2020	Sheet 10 of 102	

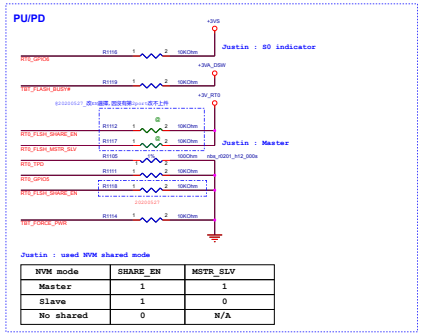
Main Board



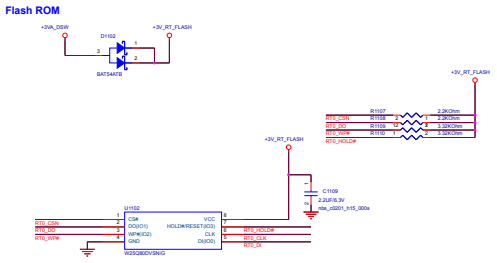


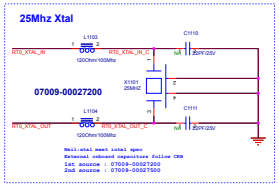


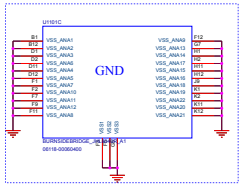




NVM mode	SHARE_EN	MSTR_SLV
Master	1	1
Slave	1	0
No shared	0	N/A



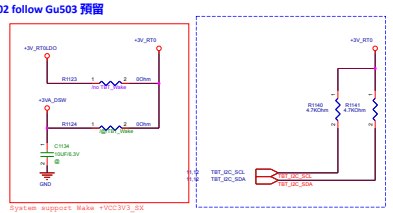




@20200611_C1110 & C1111 將18PF改22PCF

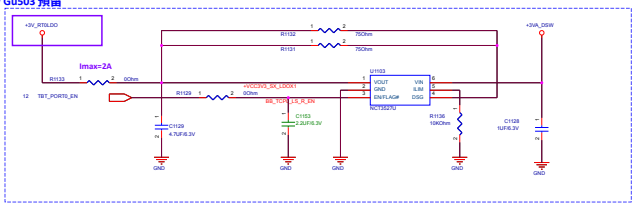
@2020831_TBT_I2C_SCL/TBT_I2C_SDA PU +3V_RT0

@20200702 follow Gu503 預留

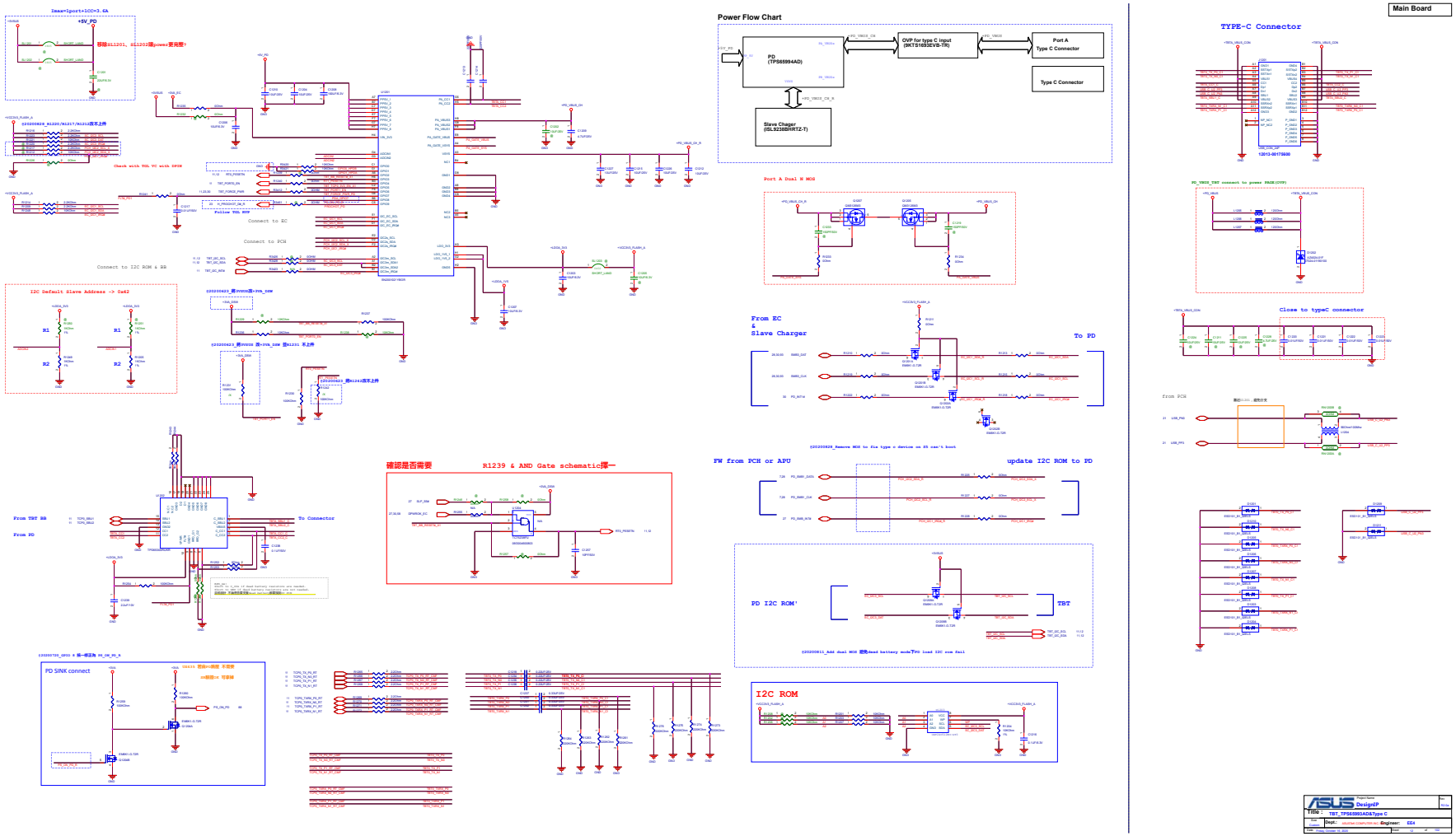


Check which power solution should be used

@20200702 follow Gu503 預留



Title :	Intel Titan-Ridge		
Size: C	Dept.:	Engineer:	
Date: Friday, October 16, 2020	Sheet 11 of 102		

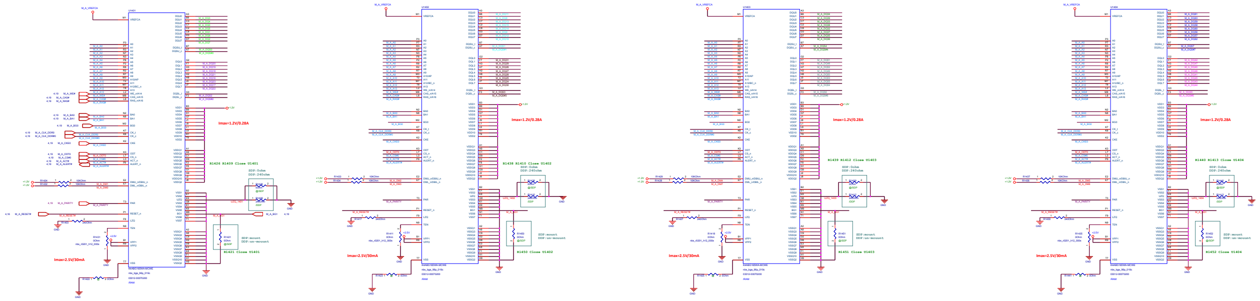


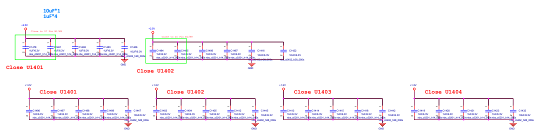
Project Name	DesignP
Rev	REV
Title	TBT_TPS65993AD&Type C
Size	Doc#
Date	Engineer: ED4
Sheet	of

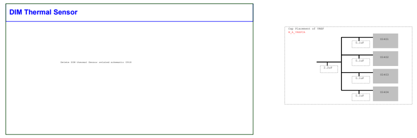
DDR4 3200 1024M*8 1.2V = 8G
SKU2_Micron: 03012-00030900
SKU3_Samsung: 03012-00031000

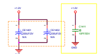
1Gx8(IO)
Total: 1Gx8ea = 8G

DDR4 3200 2048M*8 1.2V = 16G
SKU1_Micron: 03012-00060400 (此次更換_0609
SKU4_Samsung: 03012-00060100

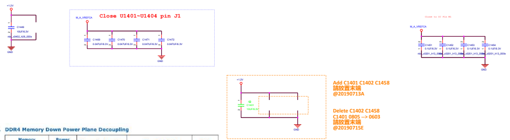








CE1402, CE1401 (220uf) change to CE1601 (330uf)
@20190626A



Add C1401 C1402 C1458
請放置末端
@20190713A

Delete C1402 C1458
C1401 0805 --> 0603
請放置末端
@20190715E

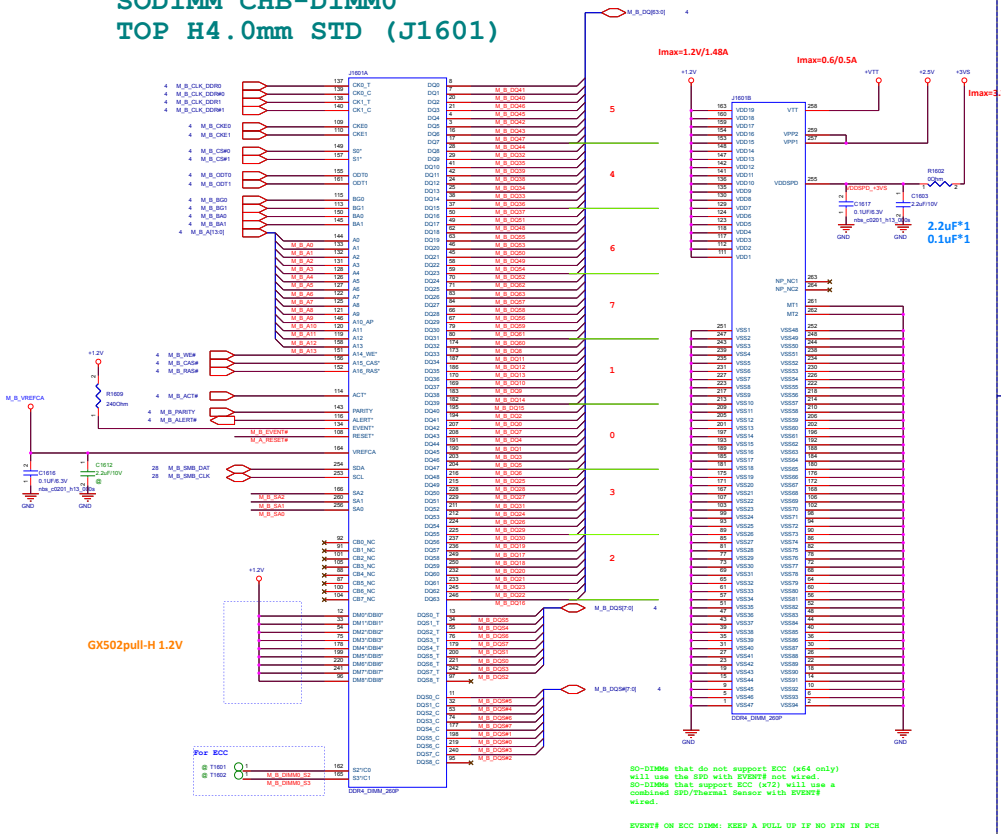
Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

<Variant Name>

Title :	DDR4_ON-BOARD_A1		
N91-RD3EE2	Engineer: EE		
Size: E	Project Name: UX482		Rev: R0.1
Date: Friday, October 16, 2020	Sheet 14 of 102		

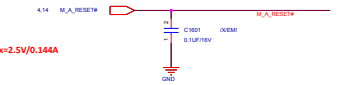
SODIMM CHB-DIMM0
TOP H4.0mm STD (J1601)



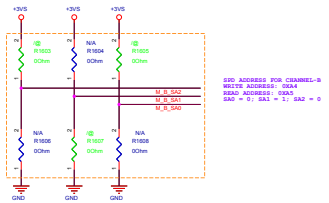
Main Board

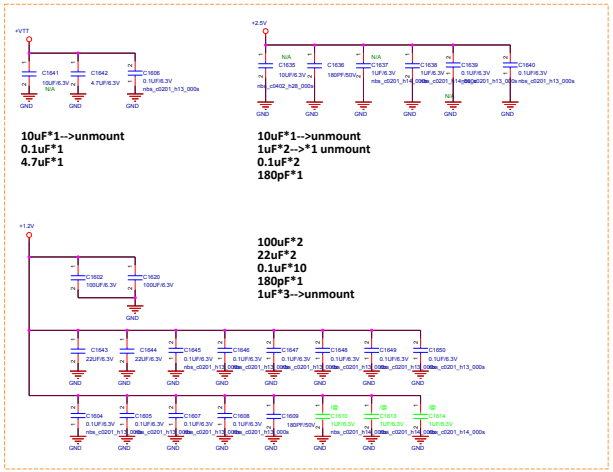
Change C1601 to monut & same with C4016
@20190219A

Imax=2.5V/0.144A



@20200619_依照公版修改SA2=0/ SA1=1/ SA0=0



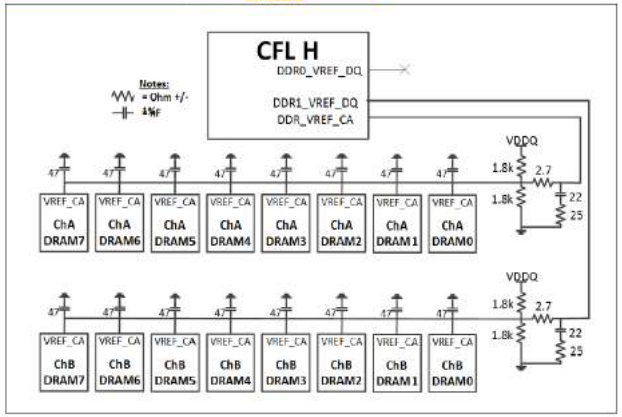


Follow FP6 CRB CAP number
@20190701A

Table 4-24. DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10µF (0603)	
		Placed on VTT plane close to DIMM	4x 1µF (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10µF (0603)	
		DIMM Pin side, 1 per DIMM	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview



Memory Down Vref

Main Board

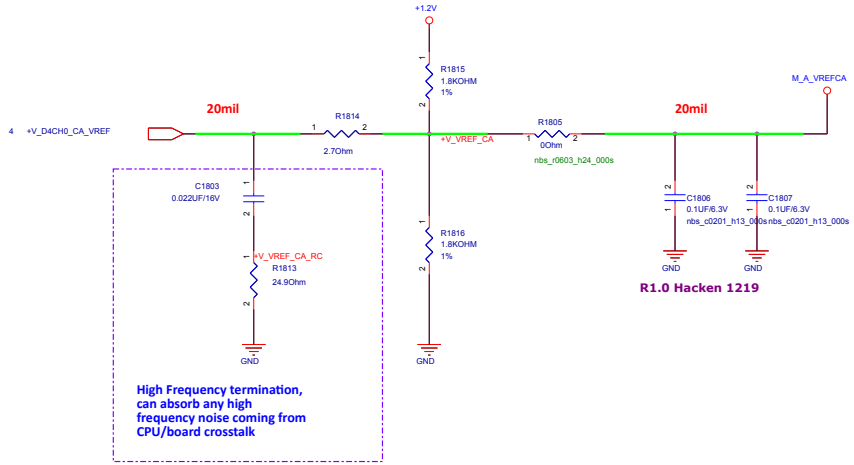
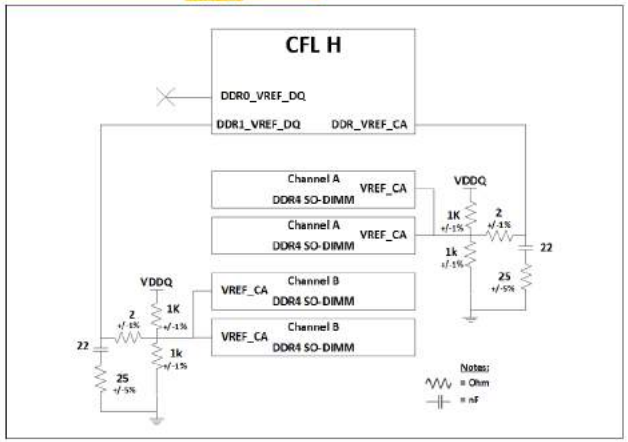
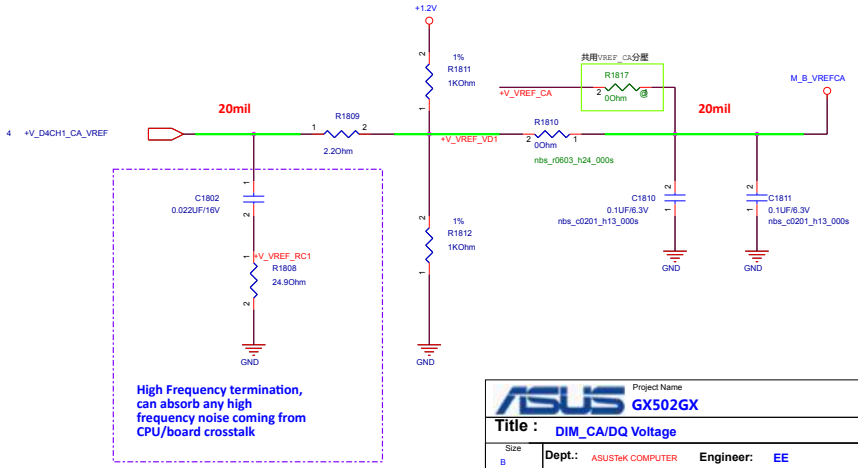


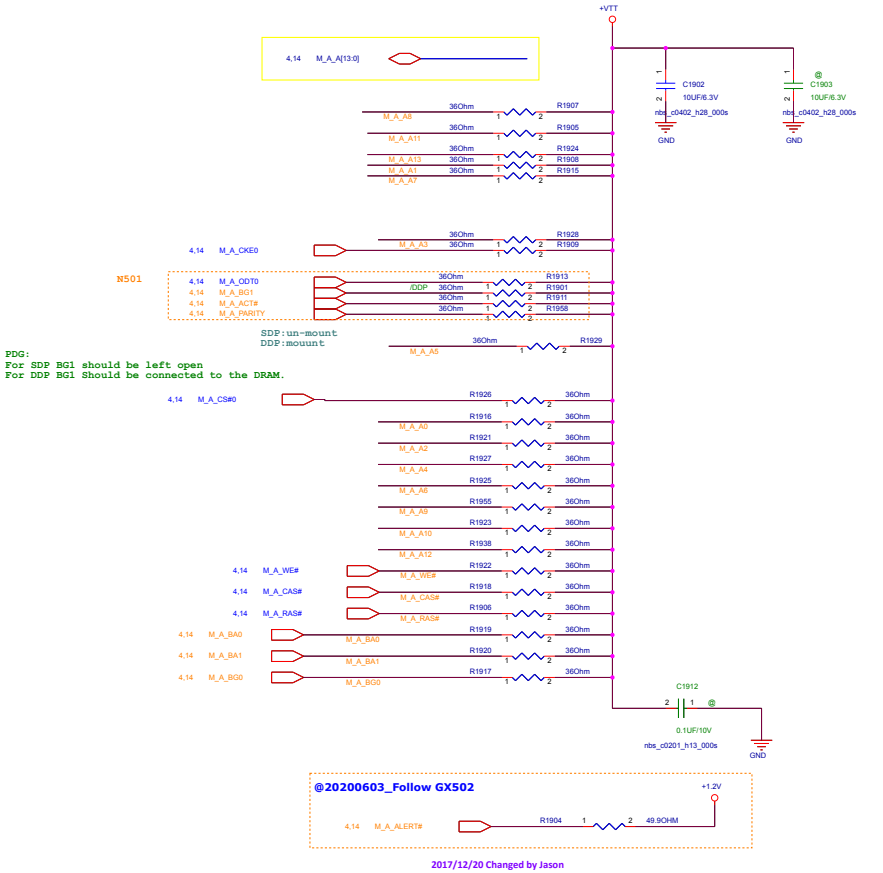
Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



SO-DIMM1 Vref

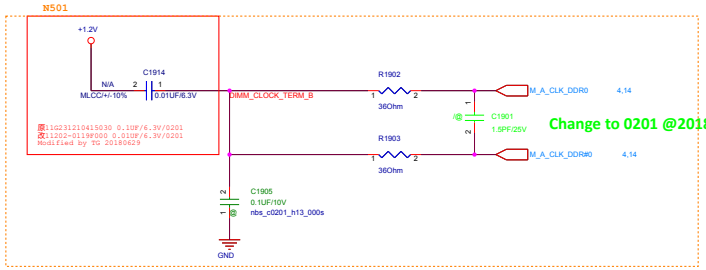


ASUS	Project Name: GX502GX	Rev: R1.2
Title :	DIM_CA/DQ Voltage	
Size: B	Dept.: ASUSTeK COMPUTER	Engineer: EE
Date: Friday, October 16, 2020	Sheet 18 of 102	



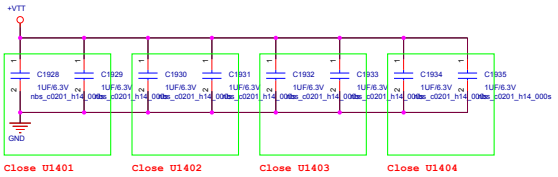
PDG:
For SDP BG1 should be left open
For DDP BG1 Should be connected to the DRAM.

2017/12/20 Changed by Jason



Clock Pull up power change from +0.6V to +1.2V (CFL PDG) 20820601

10uF*4
1uF*16



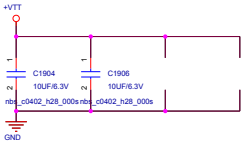
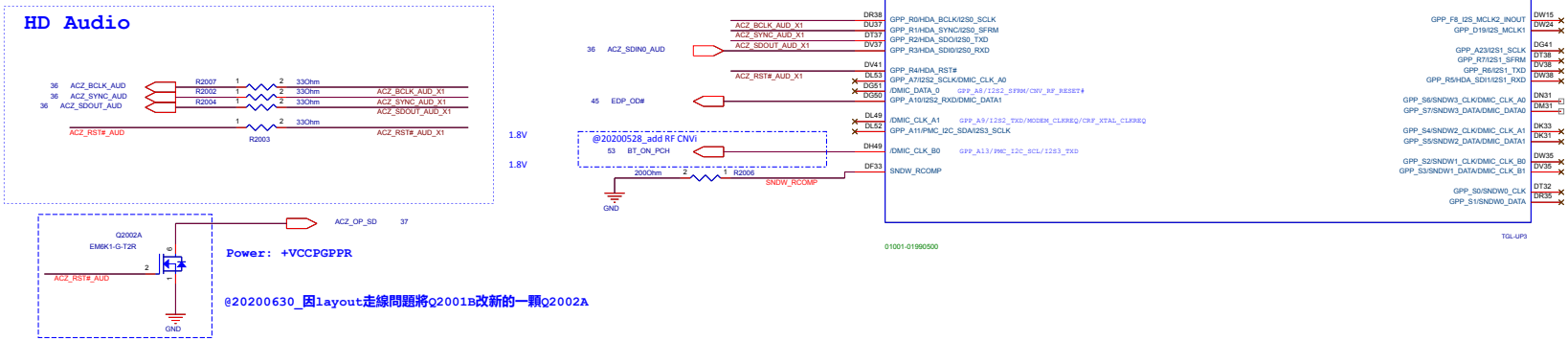


Table 4-25. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 Memory Down x8- 8 Devices per Channel	VDDQ/VDD (shorted)	4 as near each x8 DRAM device as possible	64x 1µF (0402) (min of 48 stuffed)	
		Distributed around the DRAM devices	20x 10µF (0603) (min of 12 stuffed)	
	VPP	2 as near each x8 DRAM device as possible	32x 1µF (0402)	
		Distributed around the DRAM devices	10x 10µF (0603)	
	VTT	Distributed along termination resistors	32x 1µF (0402)	
		Distributed evenly across domain	8x 10µF (0603)	

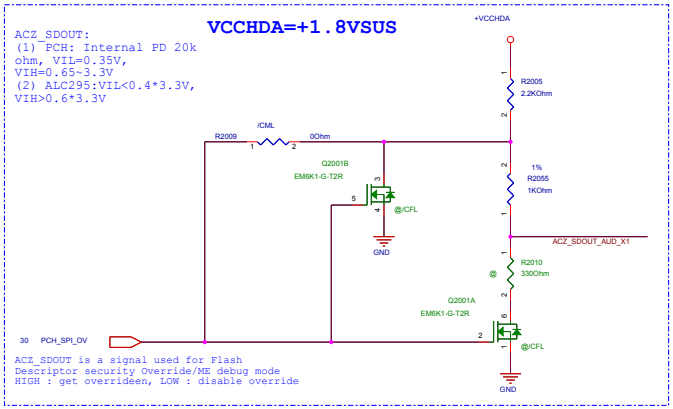
<Variant Name>



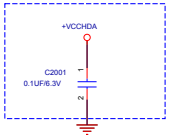
Power: +VCCPGPPR

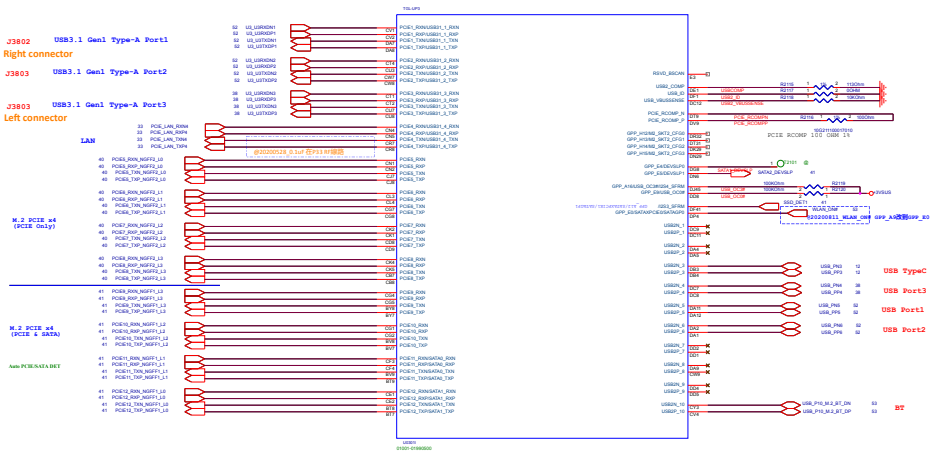
@20200630_因layout走線問題將Q2001B改新的一顆Q2002A

@20200817_Follow Gaming畫法

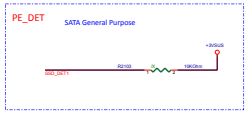


@20200612_add C2001 for CRB close to the PCH ball

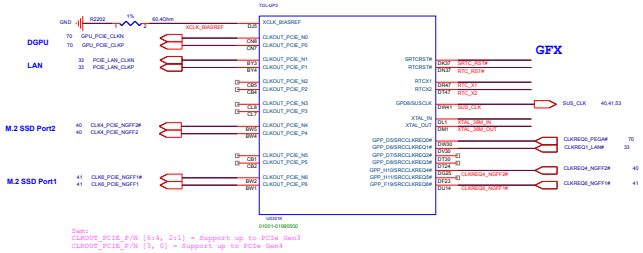




@20200611_R2103改不上電解漏電



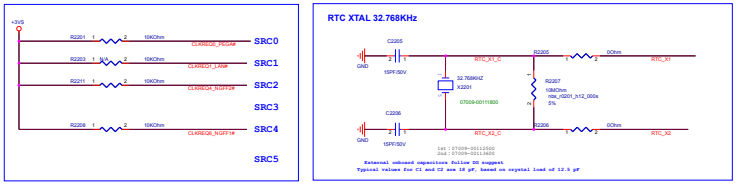
PCI-E* X1	PCIE GRADE DEFAULT/OPTION	Co-Lay	Clock
PCIE_1	N/A		
PCIE_2	N/A		
PCIE_3	N/A		
PCIE_4	N/A		
PCIE_5	N/A		
PCIE_6	N/A		
PCIE_7/SATA_0	N/A		
PCIE_8/SATA_1/2	N/A		
PCIE_9	N/A		
PCIE_10	N/A		
PCIE_11/SATA_3	N/A		
PCIE_12/SATA_1/2	PCIE SSD		
PCIE_13	PCIE SSD		
PCIE_14/SATA_0	PCIE SSD		
PCIE_15/SATA_0	PCIE SSD	SATA SSD	



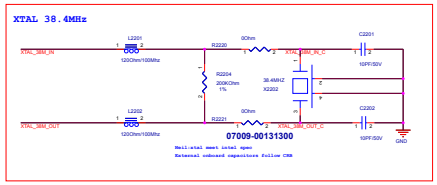
- CLKOUT_PCIE_P/N [3, 0] = Must be used for PCIe* Gen4 support

Any un-used CLKOUT_PCIE_P/N differential pair not being routed on a platform should be configured as "Disabled" through the Intel® Flash Image Tool (FIT) tool. The CLKOUT_PCIE_P/N differential pairs are called out as CLKOUT_SRC differential outputs in FIT as discussed in the SPI Programming Guide.

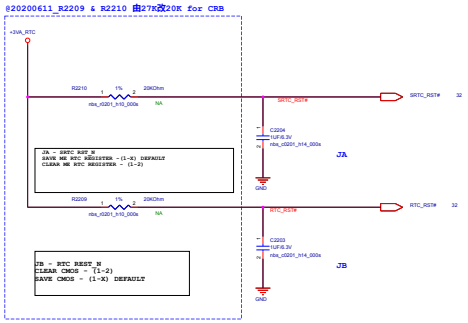
@20200630_XTAL change 07009-00111800 & 15PF for UX482

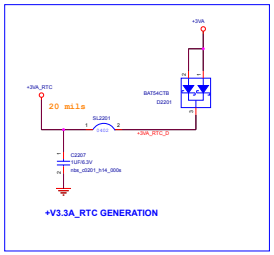


@20200630_将C2201& C2202 Change 10PF for UX482 R1.1



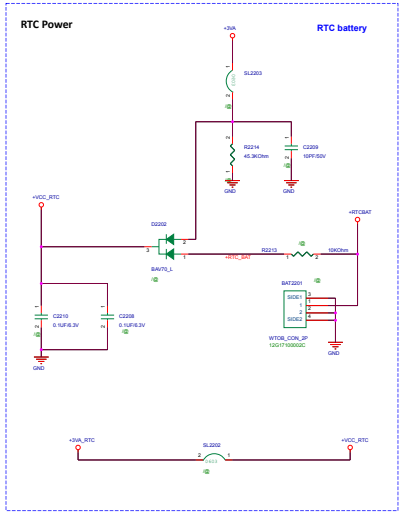
@20200611_R2209 & R2210 由27K改20K for CRB



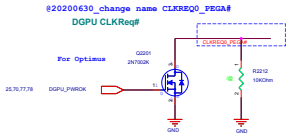


Justin : No used divided resisters. PCH has Rload inside and +3VA PU will cause VCCRTC drop to 2.7V in S0
VCCRTC must not exceed 3.3V and sustained operation at voltages below 3.0V is not recommended
Intel suggested to use diode circuit for long life relibility

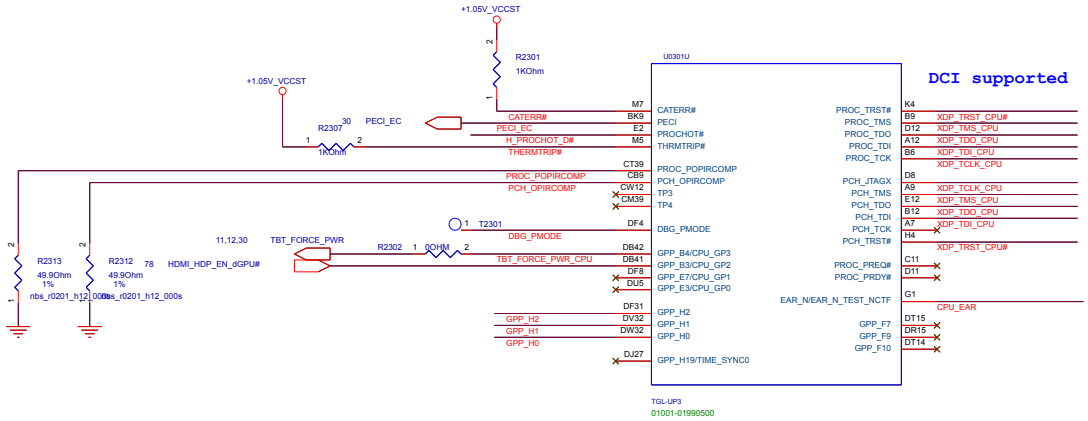
@20200702_add RTC battery

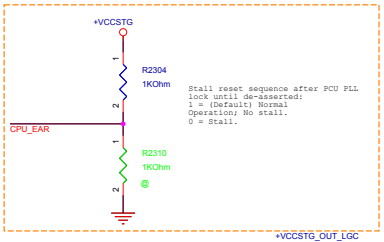


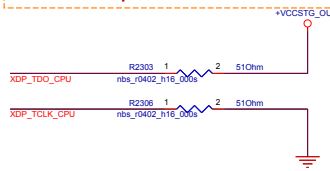
@20200630_change name CLKREQ0_PEGA#

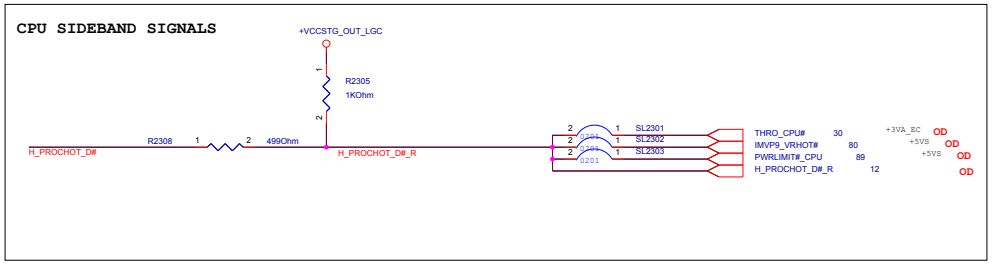


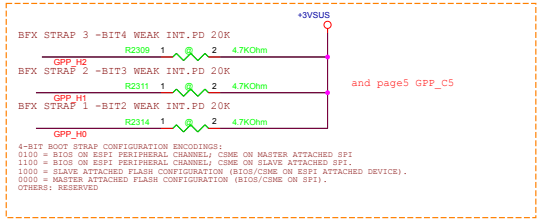
Title :	CPU_PCH_CLOCK SIGNALS,RTC		
Size: D	Dept.:	Engineer:	EE
Date: Friday, October 16, 2020	Sheet 22 of 102		





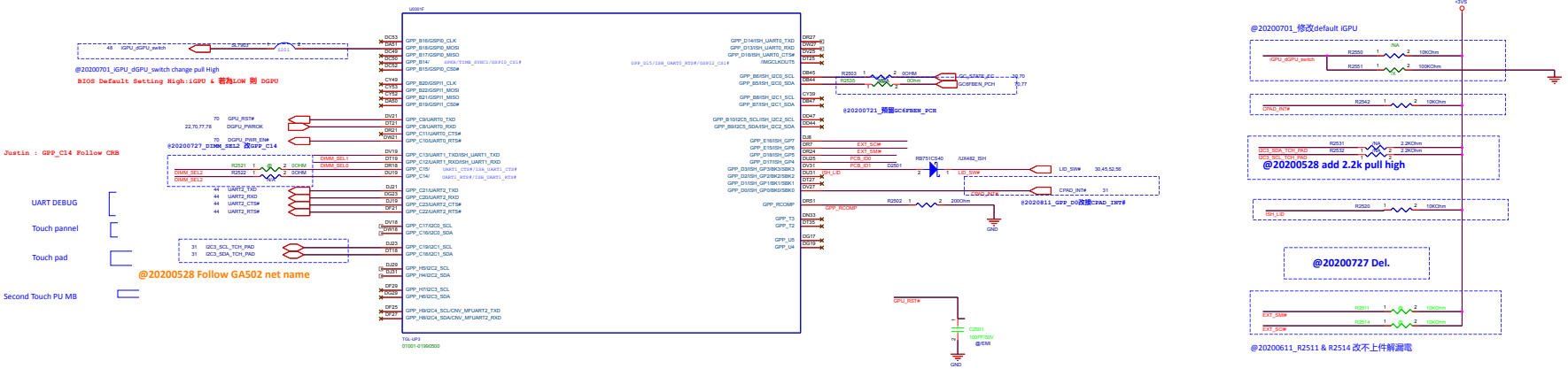


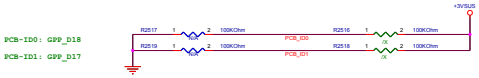


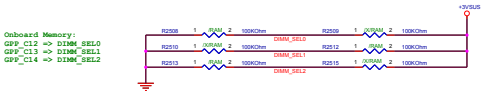


<Variant Name>

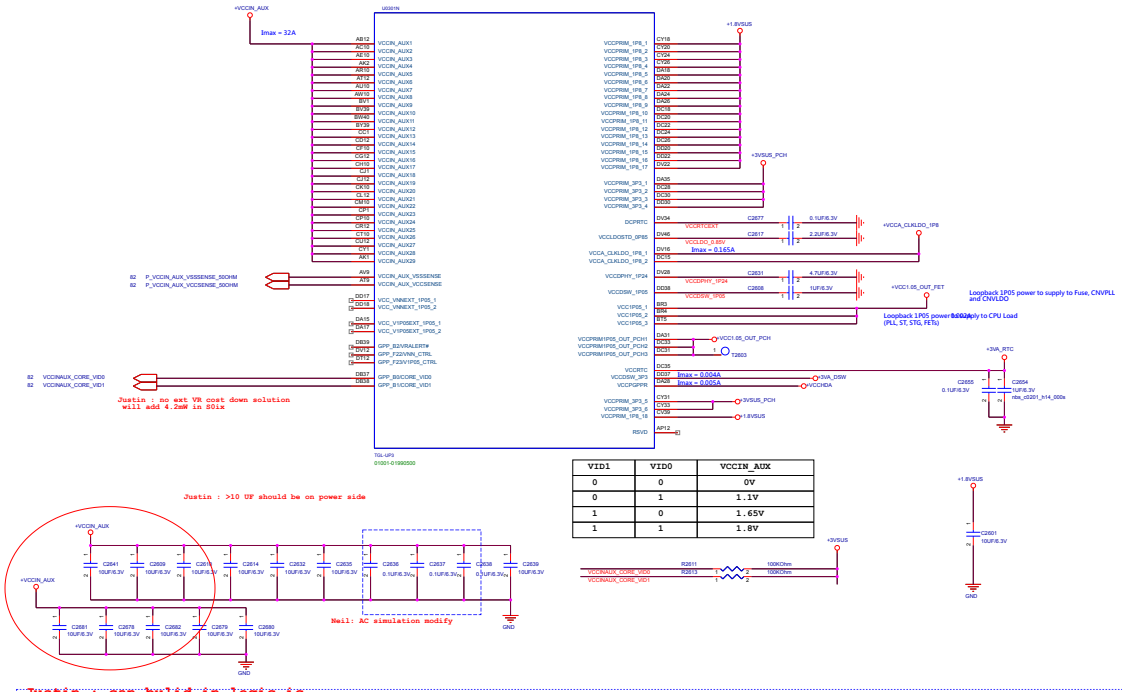
ASUS	Project Name: UX482	Rev: R0.1
Title : CPU_MISC,JTAG,CLK		
Size: C	Dept.: NB1-RD3EE2	Engineer: EE
Date: Friday, October 16, 2020	Sheet 23 of 102	



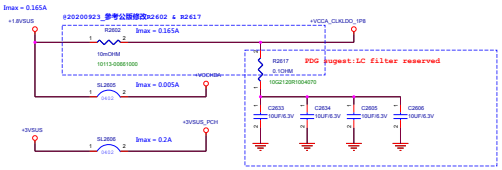


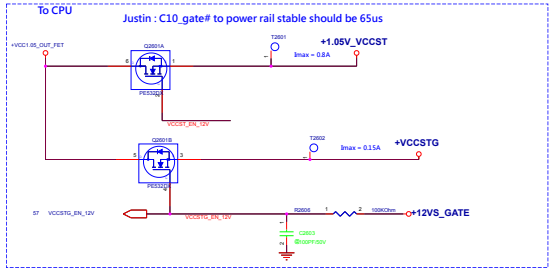


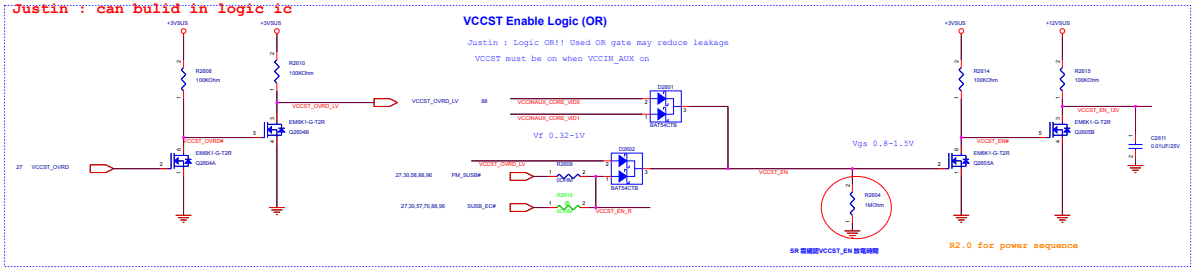
MEMORY DOWN Table			DIMM_SEL#			Key Part List
			GPP_C14	GPP_C13	GPP_C12	
			2	1	0	
03012-00070200	SKU3 目前線路	Samsung 16Gb	0	0	0	上件: R2508 / R2510 / R2513 不上件: R2509 / R2512 / R2515
			0	0	1	
03012-00040600	SKU4	MICRO 8Gb	0	1	0	上件: R2508 / R2512 / R2513 不上件: R2509 / R2510 / R2515
03012-00040700	SKU2	Samsung 8Gb	0	1	1	上件: R2509 / R2512 / R2513 不上件: R2508 / R2510 / R2515
			1	0	0	
03012-00070300	SKU1	Hynix 16Gb	1	0	1	上件: R2509 / R2510 / R2515 不上件: R2508 / R2512 / R2513
			1	1	1	

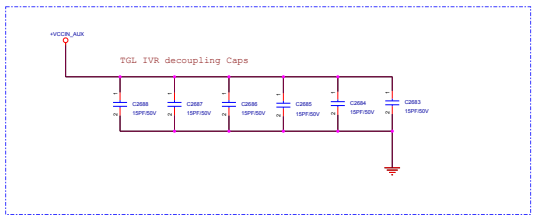


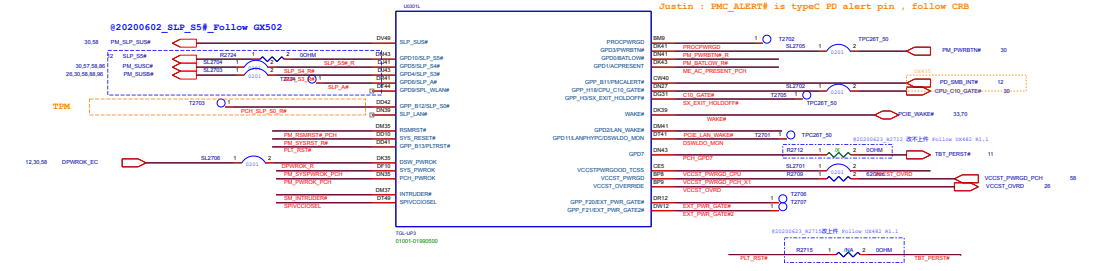
VID1	VID0	VCCIN_AUX
0	0	0V
0	1	1.1V
1	0	1.65V
1	1	1.8V

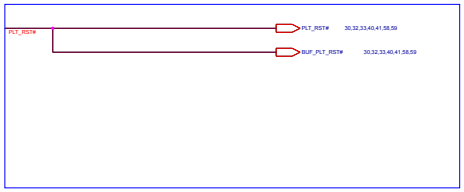


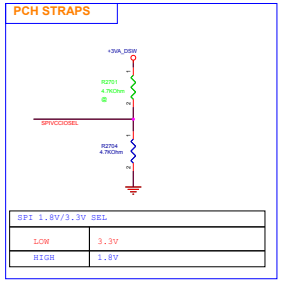


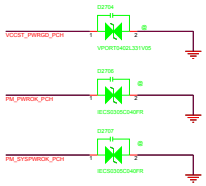


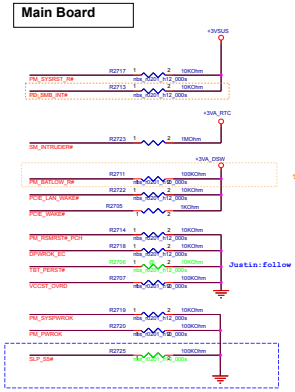




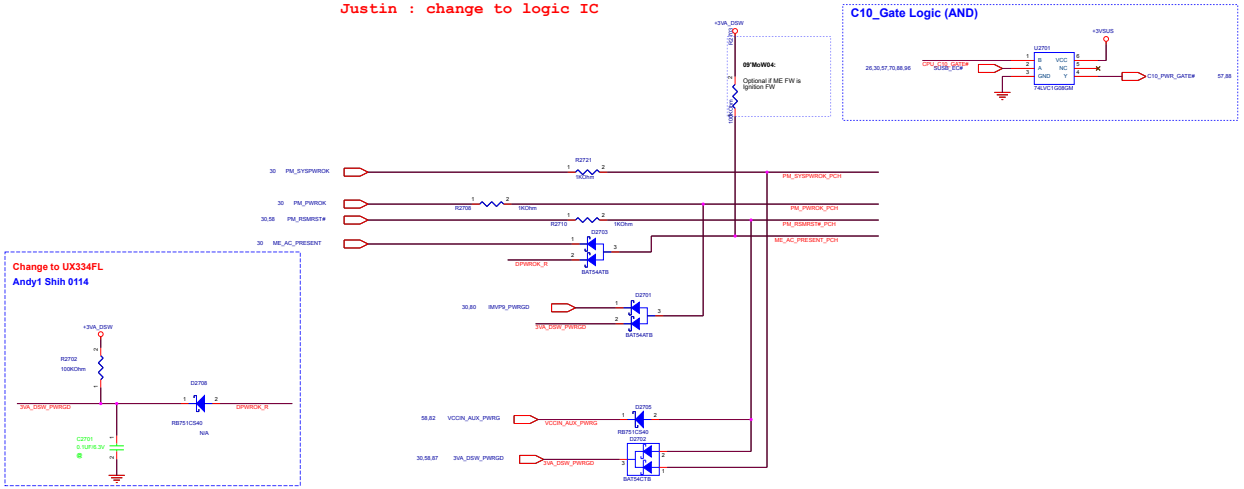








Justin : change to logic IC



Power failure solution (S0-->G3,S5-->G3):

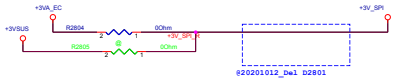
Justin : take DSW_PWROK low on emergency power loss, it must also take RSMRST# low at the same time

<Variant Name>

ASUS	Project Name: UX482	Rev: R0.1
Title : CPU_PCH_SYS_POWER		
Size: D	Dept.: NB1-RD3/EE2	Engineer: EE
Date: Friday, October 16, 2020	Sheet 27 of 102	

SPI PCH Power

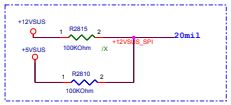
Justin : for PD platform using +3VA_EC to avoid dead battery issue.



SPI0 2-Load(1 Flash and 1TPM)
EC G3 flash sharing with Wire-OR Topology
Justin :Follow DG 6.12.3.2

Note. No TPM : R1 22 ohm
R2 75 ohm
R3 22 ohm
R4 X

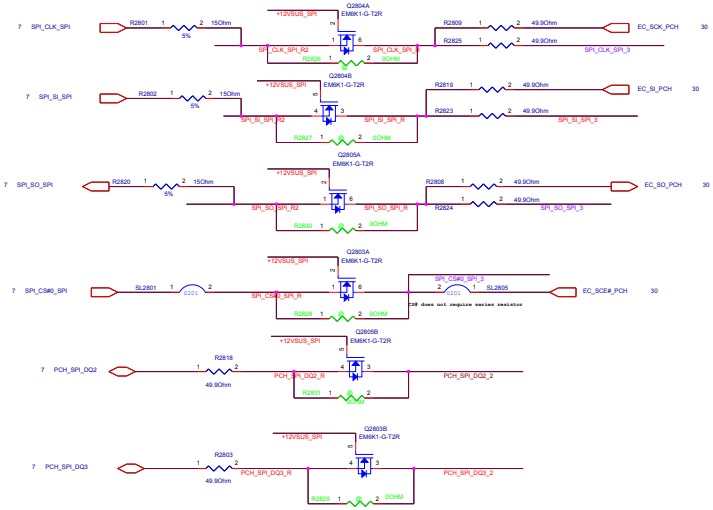
R1.3 PD project should use isolation aviod SPI leakage



@20200611_新增R2810 Pull 5VSUS
並將R2815改不上件,解漏電

PCH,TPM Side

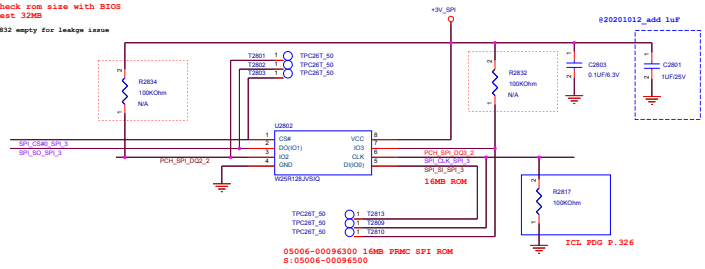
EC,SPI ROM Side



@20200709_modify 05006-00096300 16MB PRMC SPI ROM

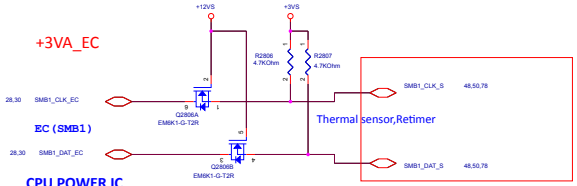
Justin : check rom size with BIOS
Intel suggest 32MB

6/6 R2834,R2832 empty for leakge issue



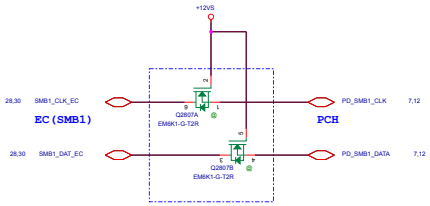
System Management Interface

+3VA_EC



CPU POWER IC
ADDR 0x7E

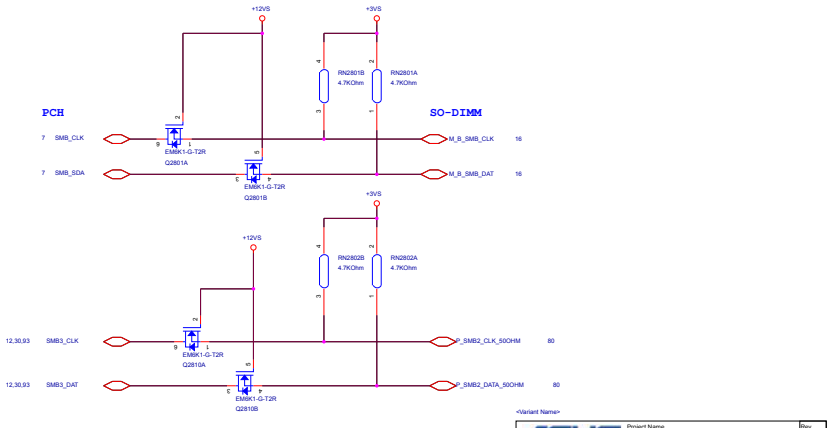
CPU Thermal sensor
ADDR 0x90
VRAM Thermal sensor
ADDR 0x91
GPU Thermal sensor
ADDR 0x92



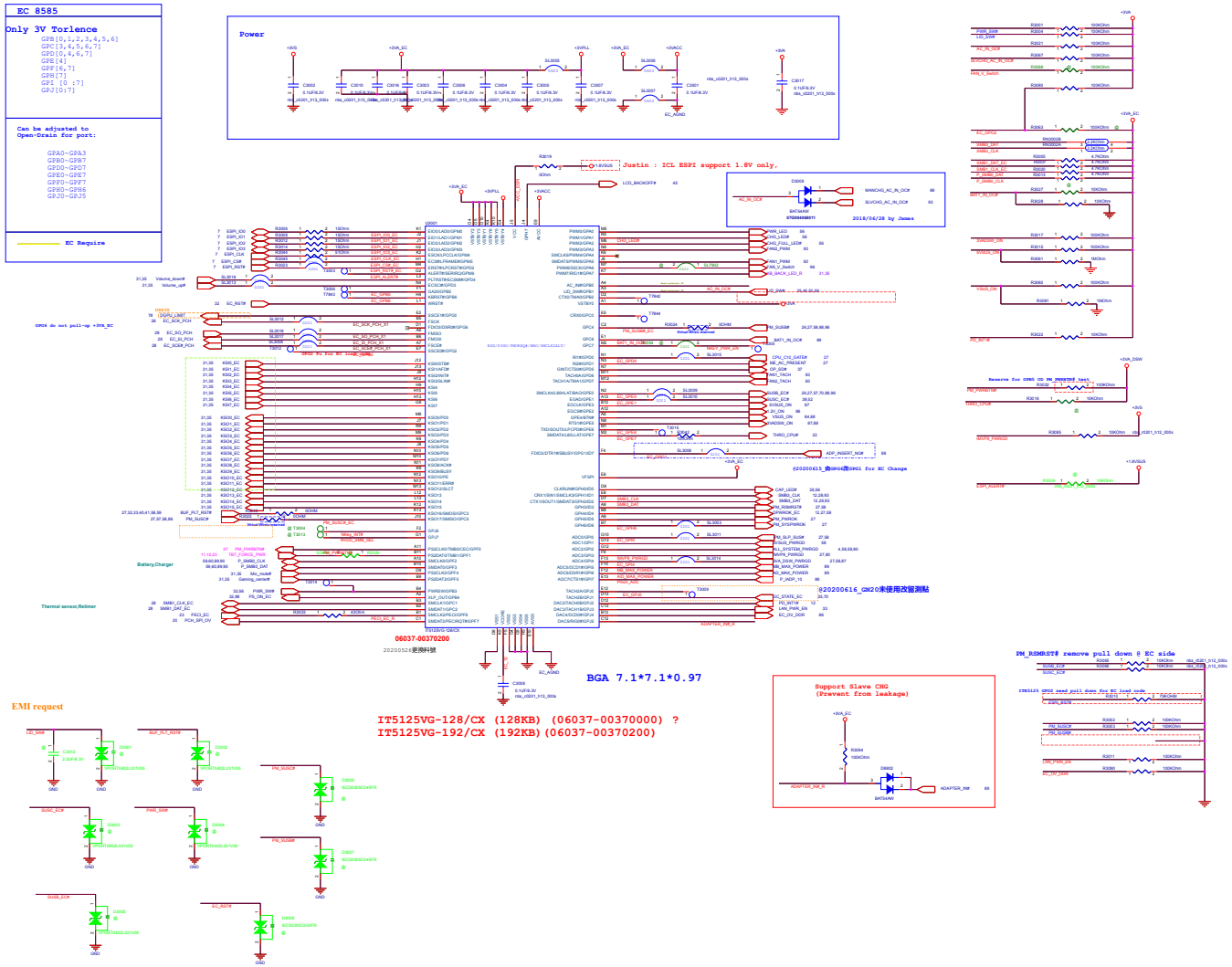
@20200707_改不上件

@20200602 Remove SMB_CLK to AMP & NVVDD CLK Switck

SMBus Interface



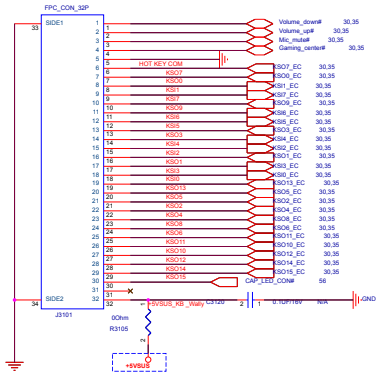
<Variant Name>


EC 8585
Only 3V Torlence
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]
Can be adjusted to Open-Drain for port:
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5
EC Require
Power
Justin : ICL ESPI support 1.8V only.
2018/06/28 by James
GPD6 do not pull-up +3VA_EC
GPD2 Fu for EC Loop back
Battery,Charger
Thermal sensor,Retimer
EMI request
06037-00370200
BGA 7.1*7.1*0.97
IT5125VG-128/CX (128KB) (06037-00370000) ?
IT5125VG-192/CX (192KB) (06037-00370200)
Support Slave CHG
(Prevent from leakage)
PM_RSMRST# remove pull down 8 EC side

Keyboard Connector

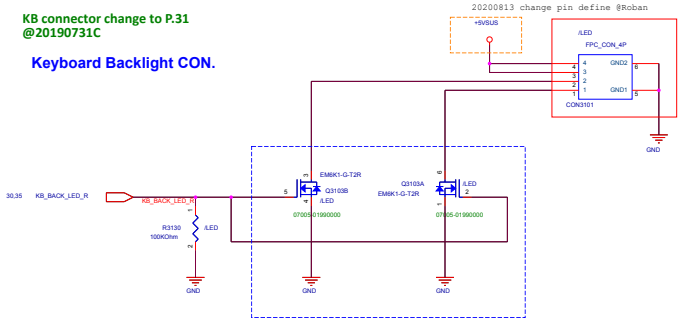
Main Board

@20200707_ME change 12018-00620100

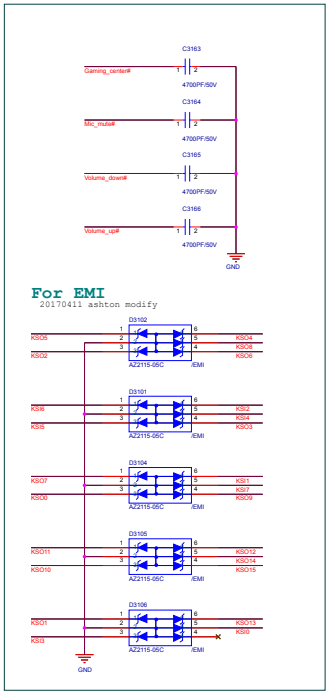


KB connector change to P.31
@20190731C

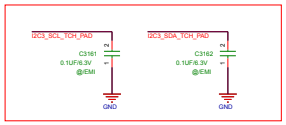
Keyboard Backlight CON.



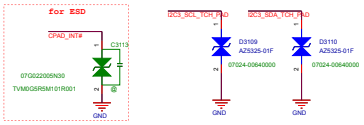
@20200619_KB 耗電量320mA 換一顆MOS 400mA



EMI Reserve
如要上件請確認容值(選擇Pico等級)

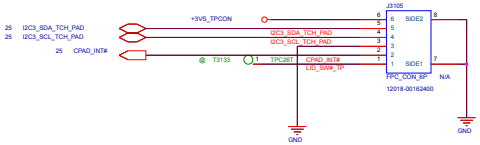


D3110 ESD Diode
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

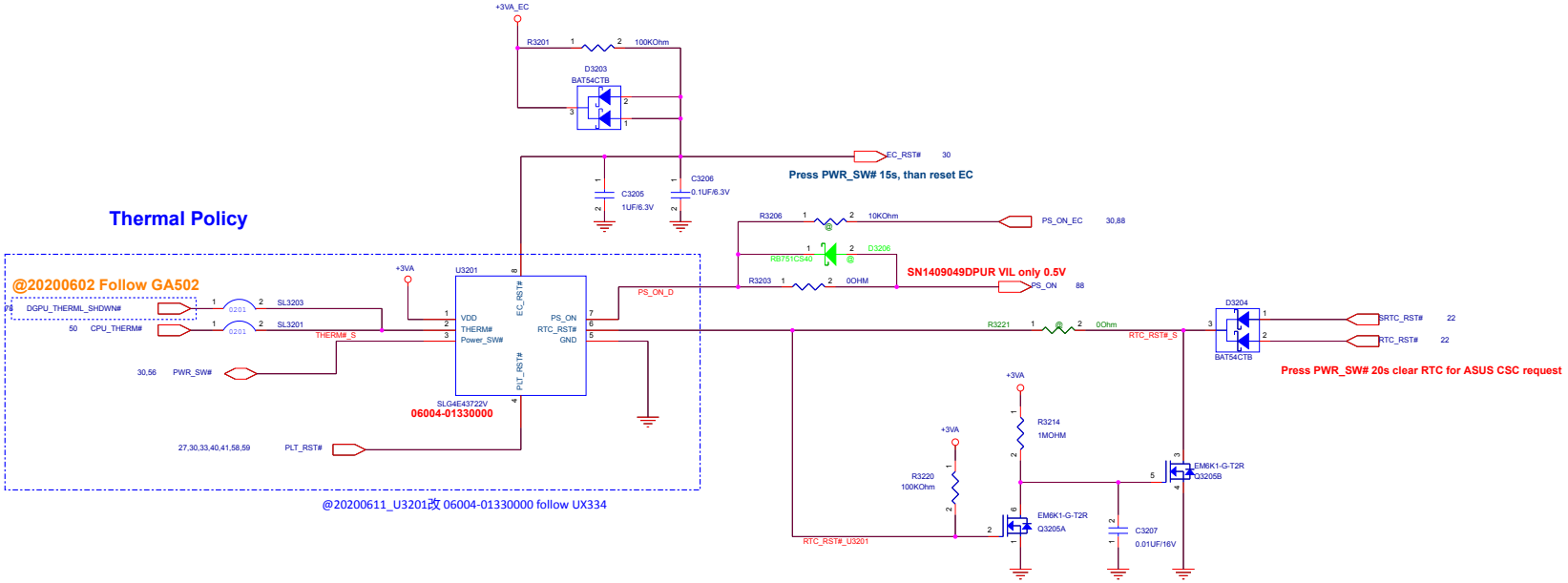


TP Connector

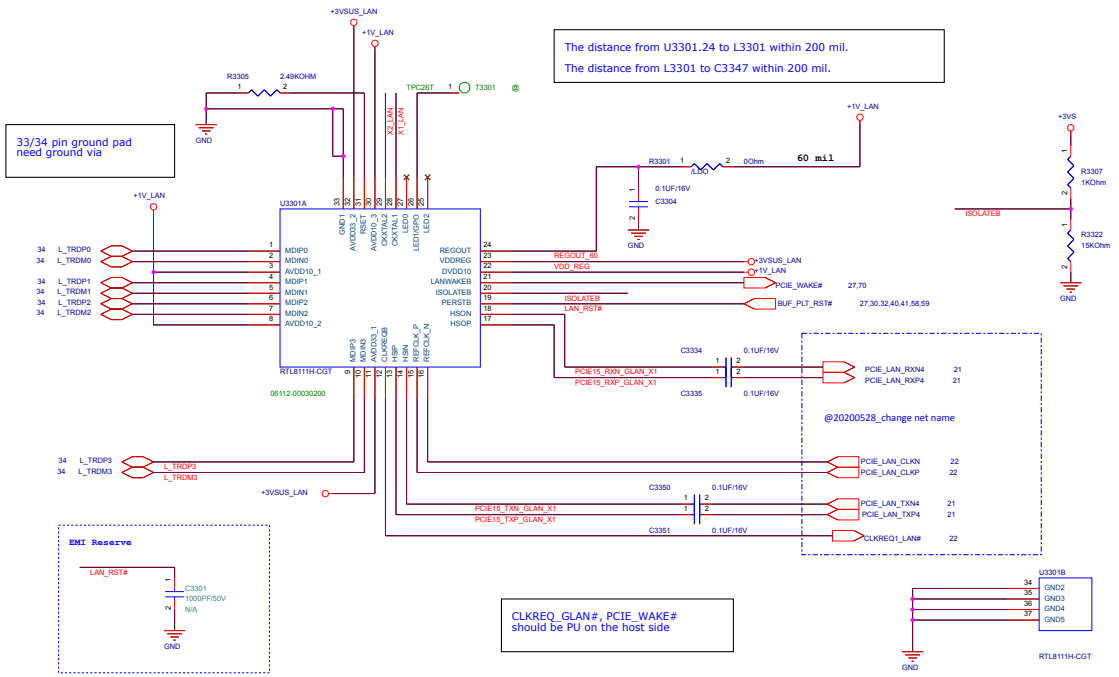
TP Conn.



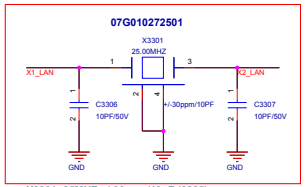
PD project should use Silego solution for EC/RTC reset



Main Board



@20200615_換回較常用XTAL 但體積較大 for GA502 & GX502

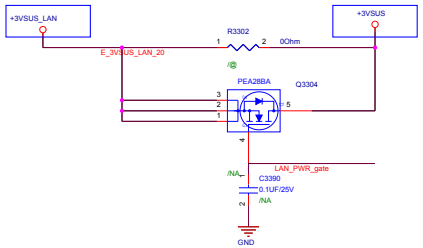


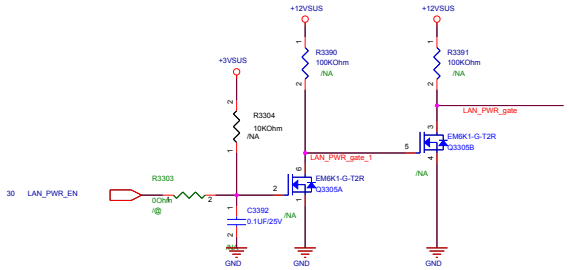
X3301: 25MHZ +/-30ppm/10pF (3225)

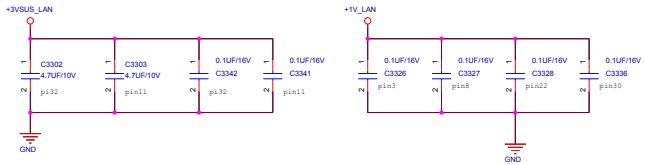
1st: P/N:07G010272501 TXC/7V25000011

2nd: P/N:07G010952500 HOSONIC/E3FB25

Realtek suggests 3V_LAN raise time >1ms

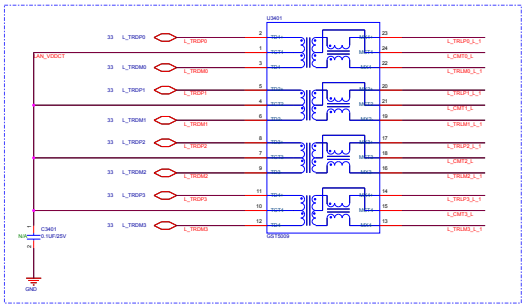


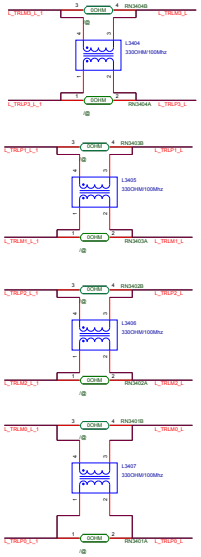




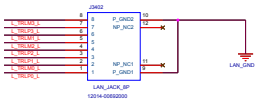
Main Board

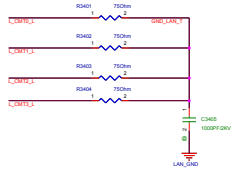
@20200702_RF要求修改連線順序



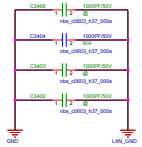


LAN Connector





EMI



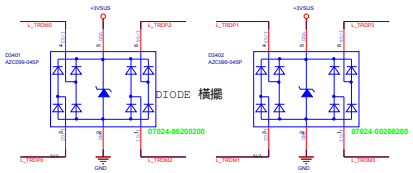
Place near chassis GND

GND_LAN_7 上禁止加任何零件

D3401,D3402 ESD Diode

1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

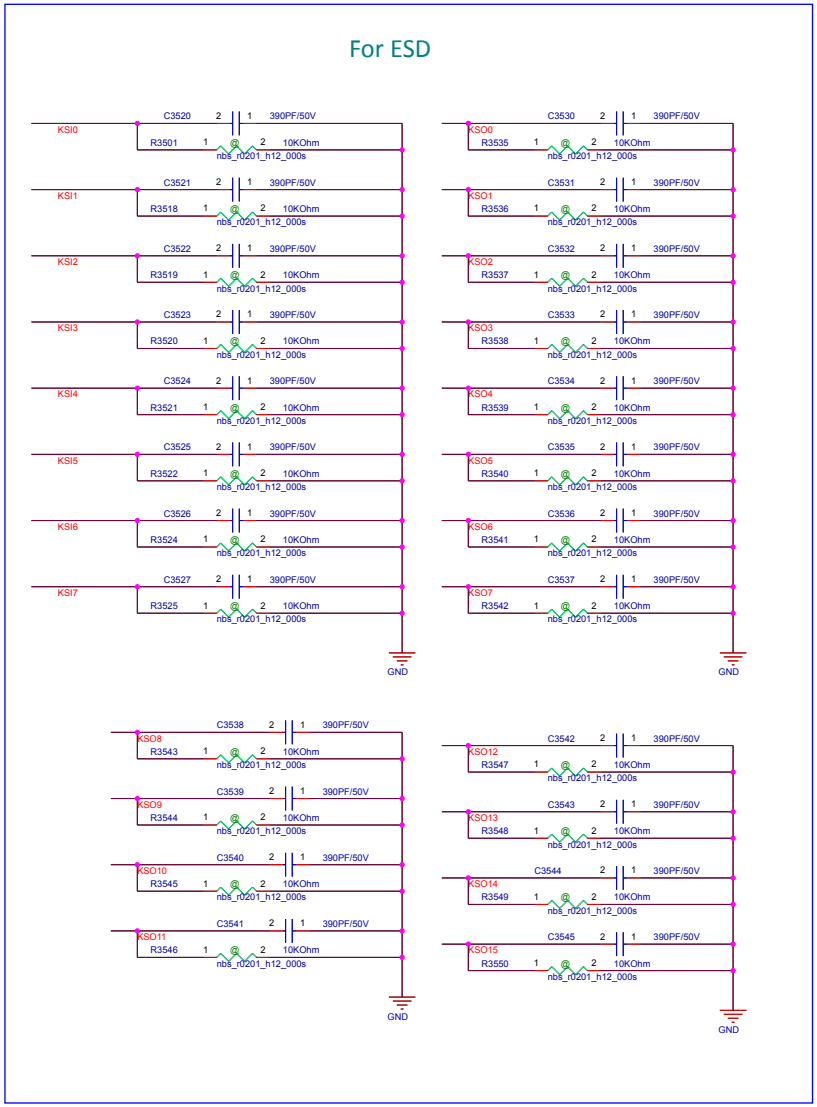


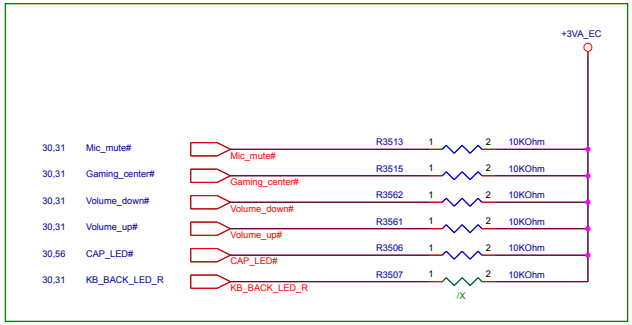
D3401,D3402 ESD Diode

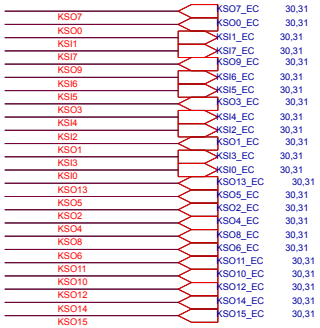
1st Source: P/N:07024-00200200 AMAZING/AZC099-04SP.R7G

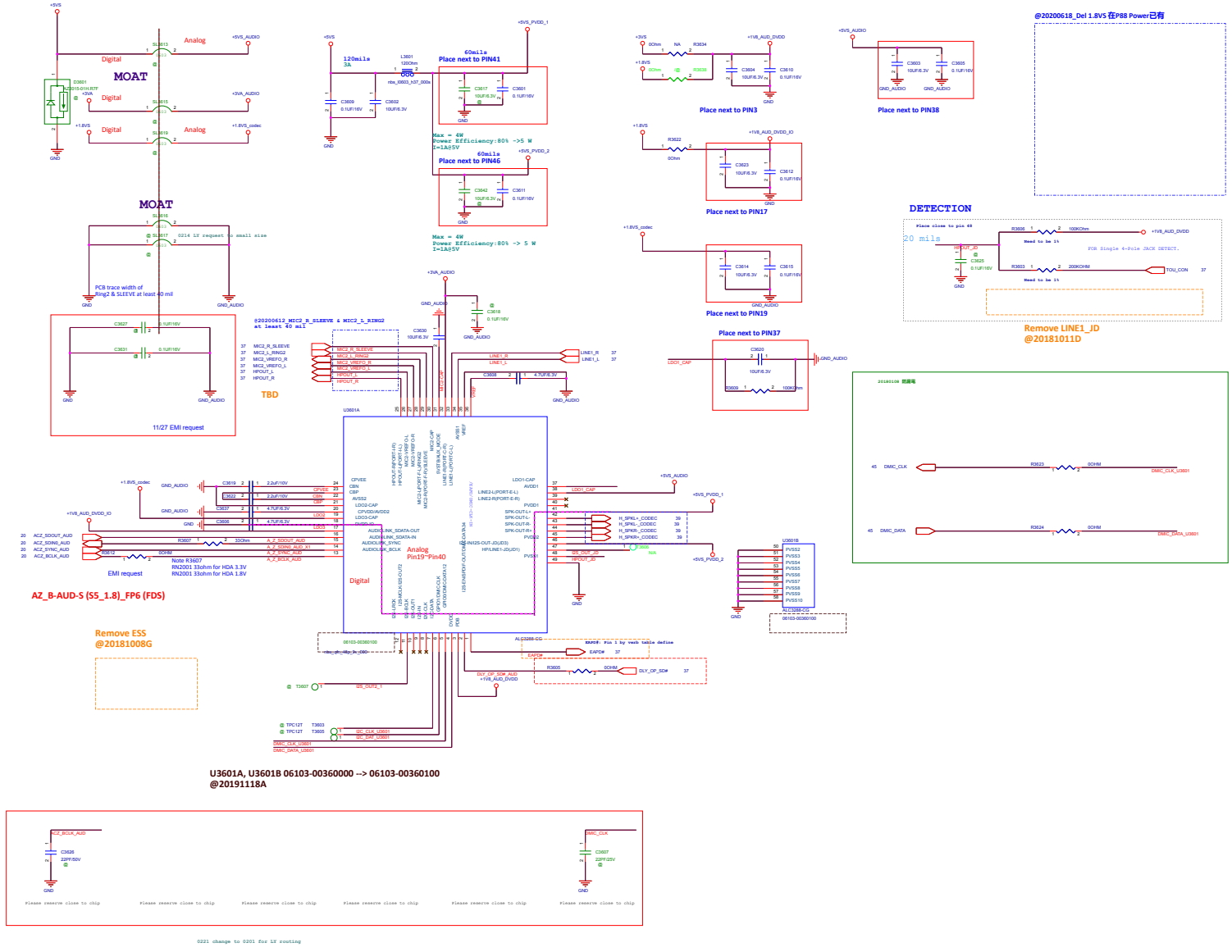
2nd Source: P/N:07024-00710000 NXP/PUSB2X4D

ASUS	Project Name: GX550LXS		Rev: R1.0
Title : LAN_RJ45_CON			
Size: C	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Friday, October 16, 2020	Sheet 34 of 102		


For ESD
C3520 2 1 390PF/50V
KSI0
R3501 1 2 10KOhm
nbs_r0201_h12_000s
C3521 2 1 390PF/50V
KSI1
R3518 1 2 10KOhm
nbs_r0201_h12_000s
C3522 2 1 390PF/50V
KSI2
R3519 1 2 10KOhm
nbs_r0201_h12_000s
C3523 2 1 390PF/50V
KSI3
R3520 1 2 10KOhm
nbs_r0201_h12_000s
C3524 2 1 390PF/50V
KSI4
R3521 1 2 10KOhm
nbs_r0201_h12_000s
C3525 2 1 390PF/50V
KSI5
R3522 1 2 10KOhm
nbs_r0201_h12_000s
C3526 2 1 390PF/50V
KSI6
R3524 1 2 10KOhm
nbs_r0201_h12_000s
C3527 2 1 390PF/50V
KSI7
R3525 1 2 10KOhm
nbs_r0201_h12_000s
GND
C3530 2 1 390PF/50V
KSO0
R3535 1 2 10KOhm
nbs_r0201_h12_000s
C3531 2 1 390PF/50V
KSO1
R3536 1 2 10KOhm
nbs_r0201_h12_000s
C3532 2 1 390PF/50V
KSO2
R3537 1 2 10KOhm
nbs_r0201_h12_000s
C3533 2 1 390PF/50V
KSO3
R3538 1 2 10KOhm
nbs_r0201_h12_000s
C3534 2 1 390PF/50V
KSO4
R3539 1 2 10KOhm
nbs_r0201_h12_000s
C3535 2 1 390PF/50V
KSO5
R3540 1 2 10KOhm
nbs_r0201_h12_000s
C3536 2 1 390PF/50V
KSO6
R3541 1 2 10KOhm
nbs_r0201_h12_000s
C3537 2 1 390PF/50V
KSO7
R3542 1 2 10KOhm
nbs_r0201_h12_000s
GND
C3538 2 1 390PF/50V
KSO8
R3543 1 2 10KOhm
nbs_r0201_h12_000s
C3539 2 1 390PF/50V
KSO9
R3544 1 2 10KOhm
nbs_r0201_h12_000s
C3540 2 1 390PF/50V
KSO10
R3545 1 2 10KOhm
nbs_r0201_h12_000s
C3541 2 1 390PF/50V
KSO11
R3546 1 2 10KOhm
nbs_r0201_h12_000s
GND
C3542 2 1 390PF/50V
KSO12
R3547 1 2 10KOhm
nbs_r0201_h12_000s
C3543 2 1 390PF/50V
KSO13
R3548 1 2 10KOhm
nbs_r0201_h12_000s
C3544 2 1 390PF/50V
KSO14
R3549 1 2 10KOhm
nbs_r0201_h12_000s
C3545 2 1 390PF/50V
KSO15
R3550 1 2 10KOhm
nbs_r0201_h12_000s
GND

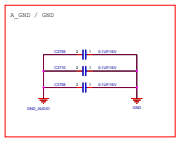

+3VA_EC
30,31 Mic_mute#
Mic_mute#
R3513 1 2 10KOhm
30,31 Gaming_center#
Gaming_center#
R3515 1 2 10KOhm
30,31 Volume_down#
Volume_down#
R3562 1 2 10KOhm
30,31 Volume_up#
Volume_up#
R3561 1 2 10KOhm
30,56 CAP_LED#
CAP_LED#
R3506 1 2 10KOhm
30,31 KB_BACK_LED_R
KB_BACK_LED_R
R3507 1 2 10KOhm
/X

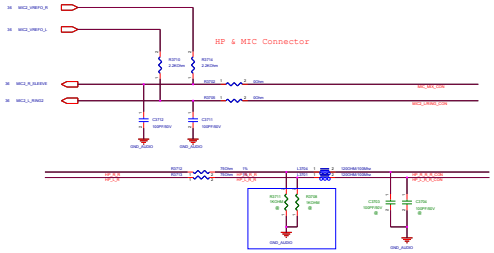

KSO7 KSO7_EC 30,31
KSO0 KSO0_EC 30,31
KSI1 KSI1_EC 30,31
KSI7 KSI7_EC 30,31
KSO9 KSO9_EC 30,31
KSI6 KSI6_EC 30,31
KSI5 KSI5_EC 30,31
KSO3 KSO3_EC 30,31
KSI4 KSI4_EC 30,31
KSI2 KSI2_EC 30,31
KSO1 KSO1_EC 30,31
KSI3 KSI3_EC 30,31
KSI0 KSI0_EC 30,31
KSO13 KSO13_EC 30,31
KSO5 KSO5_EC 30,31
KSO2 KSO2_EC 30,31
KSO4 KSO4_EC 30,31
KSO8 KSO8_EC 30,31
KSO6 KSO6_EC 30,31
KSO11 KSO11_EC 30,31
KSO10 KSO10_EC 30,31
KSO12 KSO12_EC 30,31
KSO14 KSO14_EC 30,31
KSO15 KSO15_EC 30,31

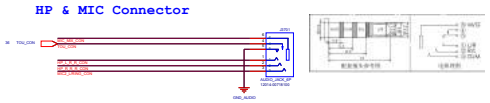

MOAT
Analog
Digital
Place next to PIN41
Place next to PIN46
Place next to PIN3
Place next to PIN38
Place next to PIN17
Place next to PIN19
Place next to PIN37
DETECTION
Remove LINE1_JD
@20181011D
TBD
11/27 EMI request
Note R3607
RN2001 33ohm for HDA 3.3V
RN2001 33ohm for HDA 1.8V
EMI request
AZ_B-AUD-S (SS_1.8)_FP6 (FDS)
Analog
Pin19~Pin40
Digital
Remove ESS
@20181008G
U3601A, U3601B 06103-00360000 --> 06103-00360100
@20191118A
@20200618_Del 1.8VS 在P88 Power已有
0221 change to 0201 for LY routing

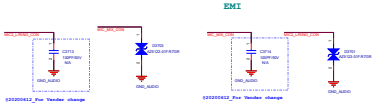
Main Board

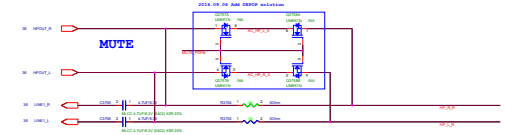
Headphone&MIC



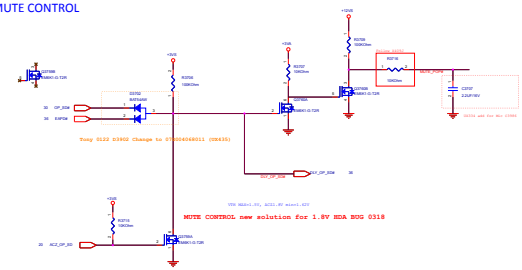








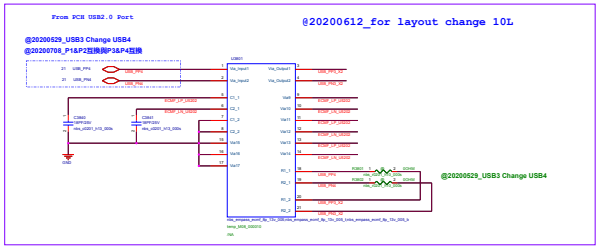
MUTE CONTROL



ASUS	Project Name: GX531GX	Rev: 1.0
Title : AUDIO ALC3236-CG/VB2 Jack		
Size: D	Dept.: ASUSTeK COMPUTER INC	Engineer:
Date: Friday, October 16, 2020	Sheet 37 of 102	

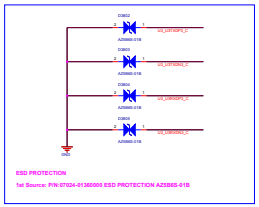
USB3.1_Port3

USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

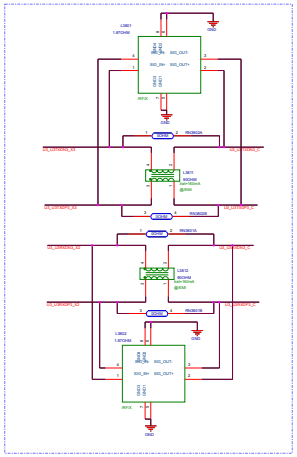


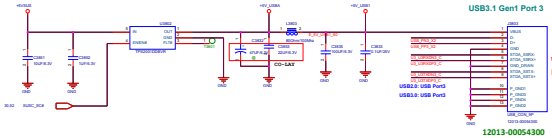
Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
2. CS2012/CS210 must replaced with 10pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

USB3.0 ESD-Protection

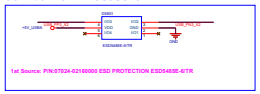


@20200615_新增L3801 & L3802 & L3811 & L3812 for EMI

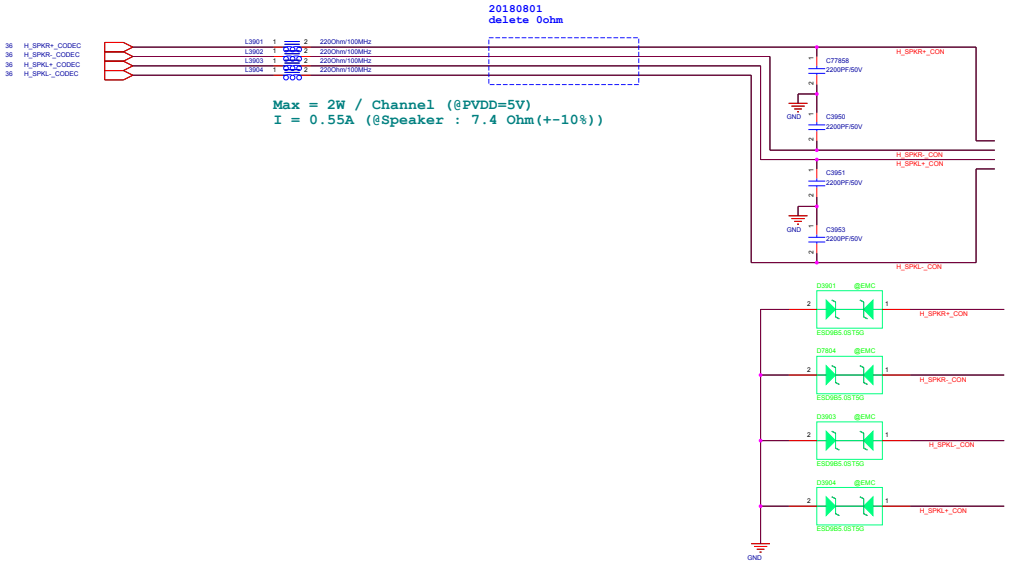


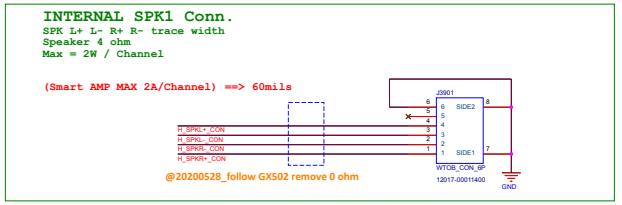


USB2.0 ESD-Protection

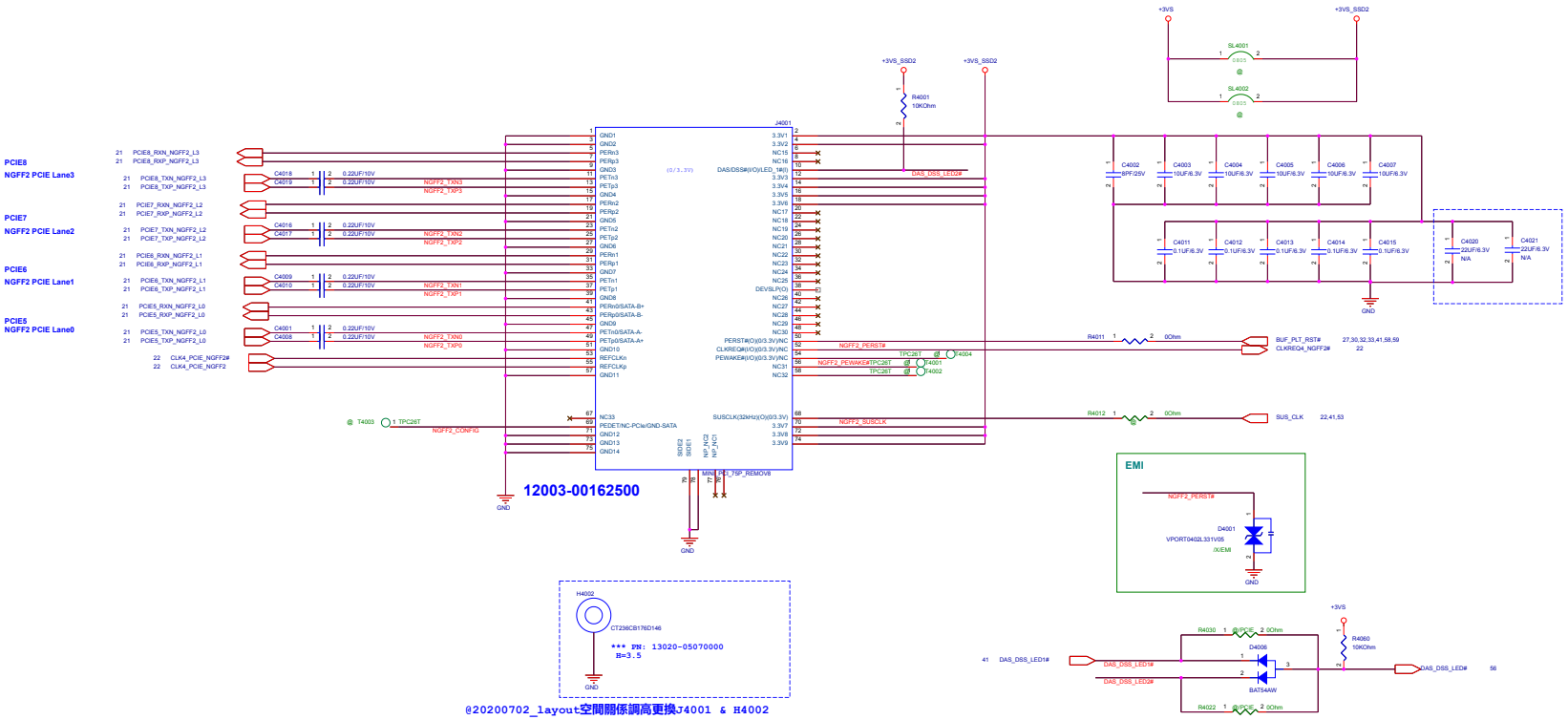


ASUS	Project Name: UX482		Rev: 2.0
Title : USB3.1 (Gen2)			
Size:	Dept.: MB-RD&EI	Engineer: EE	
Date: Friday, October 16, 2020		Sheet: 38 of 102	


20180801
delete 0ohm
36 H_SPKR+_CODEC
36 H_SPKR-_CODEC
36 H_SPKL+_CODEC
36 H_SPKL-_CODEC
L3901 220Ohm/100MHz
L3902 220Ohm/100MHz
L3903 220Ohm/100MHz
L3904 220Ohm/100MHz
Max = 2W / Channel (@PVDD=5V)
I = 0.55A (@Speaker : 7.4 Ohm(+-10%))
C77868 2200PF/50V
C3950 2200PF/50V
C3951 2200PF/50V
C3953 2200PF/50V
GND
H_SPKR+_CON
H_SPKR-_CON
H_SPKL+_CON
H_SPKL-_CON
D3901 @EMC
D7804 @EMC
D3903 @EMC
D3904 @EMC
ESD9B5.0ST5G

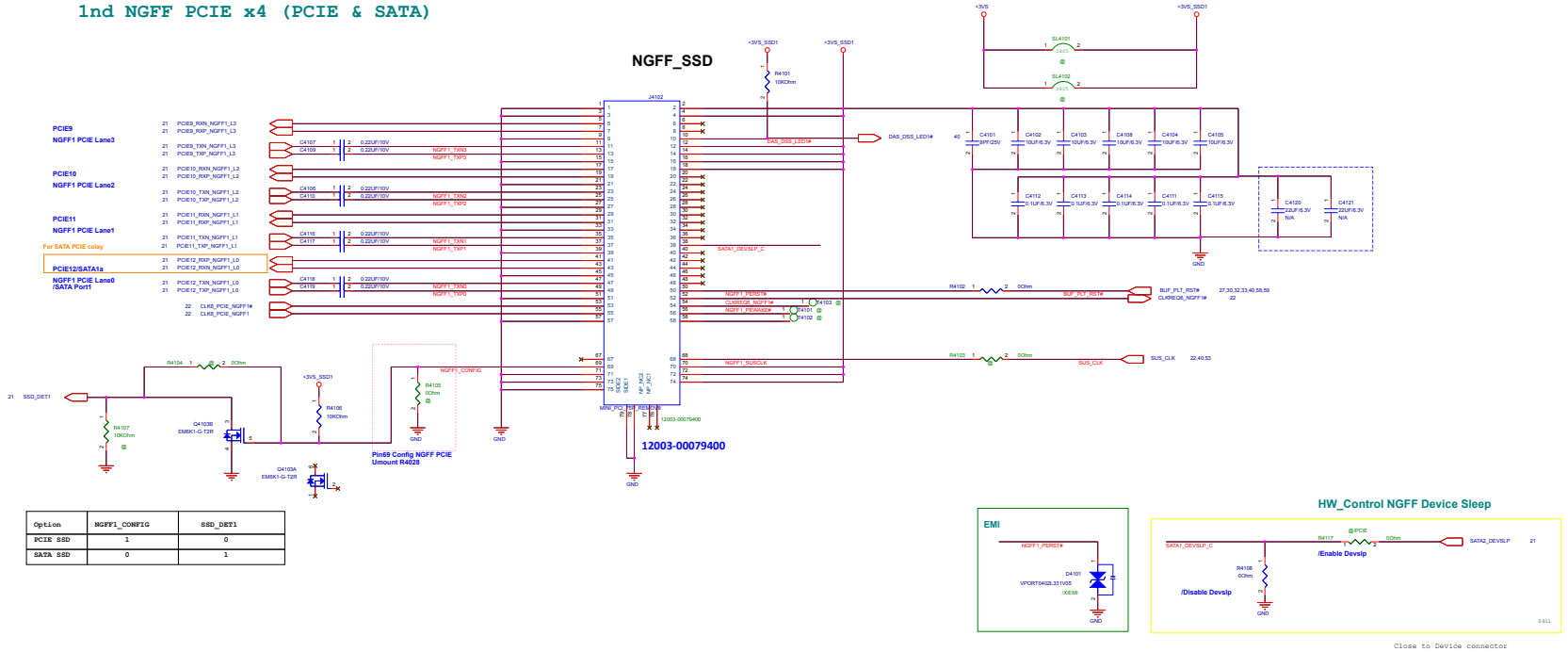

INTERNAL SPK1 Conn.
SPK L+ L- R+ R- trace width
Speaker 4 ohm
Max = 2W / Channel
(Smart AMP MAX 2A/Channel) ==> 60mils
H_SPKL+_CON
H_SPKL-_CON
H_SPKR-_CON
H_SPKR+_CON
J3901
SIDE2
SIDE1
WTOB_CON_8P
12017-00001400
GND
@20200528_follow GX502 remove 0 ohm

2 nd NGFF PCIE x4 (PCIE only)



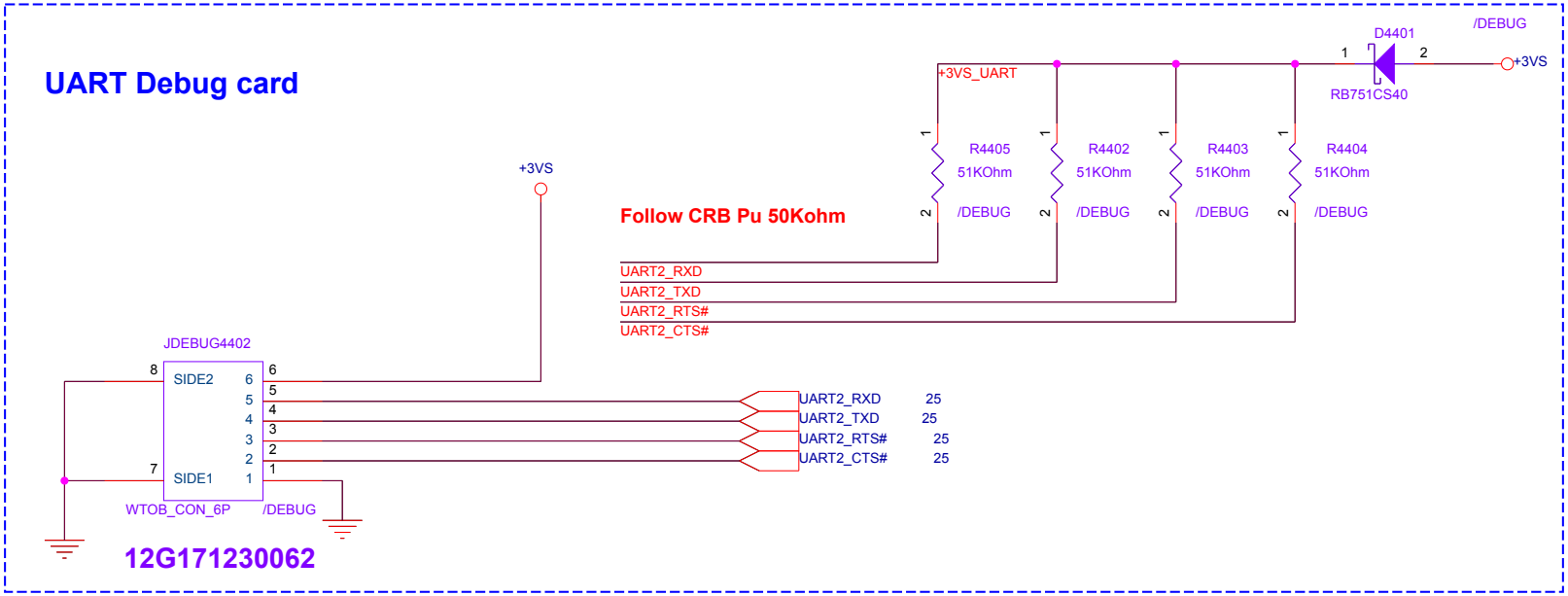
@20200702_layout空間關係調高更換J4001 & H4002

1nd NGFF PCIE x4 (PCIE & SATA)

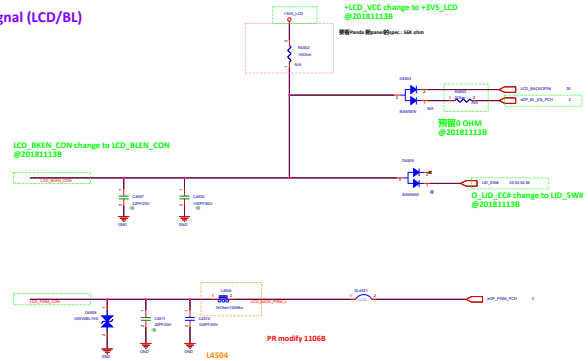


Option	NGFF1_CONFIG	SSD_DET1
PCIE SSD	1	0
SATA SSD	0	1

Close to Device connector


UART Debug card
+3VS
Follow CRB Pu 50Kohm
+3VS_UART
D4401
/DEBUG
RB751CS40
+3VS
R4405
51KOhm
/DEBUG
R4402
51KOhm
/DEBUG
R4403
51KOhm
/DEBUG
R4404
51KOhm
/DEBUG
UART2_RXD
UART2_TXD
UART2_RTS#
UART2_CTS#
JDEBUG4402
SIDE2
SIDE1
WTOB_CON_6P
/DEBUG
UART2_RXD 25
UART2_TXD 25
UART2_RTS# 25
UART2_CTS# 25
12G171230062

Controll Signal (LCD/BL)

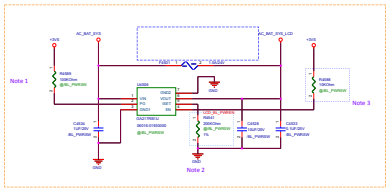


LCD VDDEN / +3VS_LCD

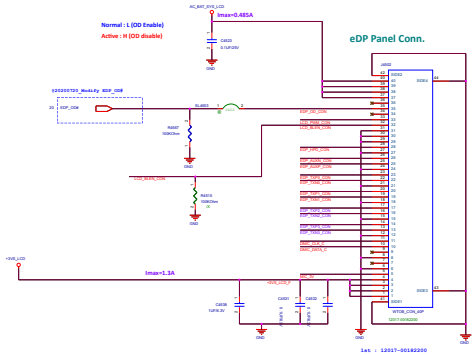
Panel BL Power

Design IP
@20190719C

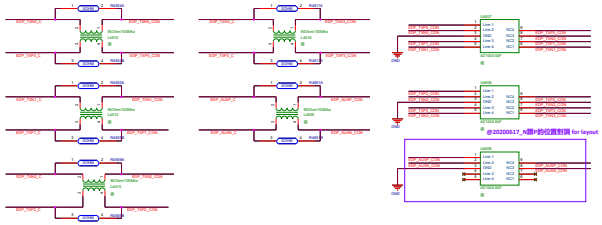
Delete R4569 0 OHM
@20191009A



eDP Panel Conn.



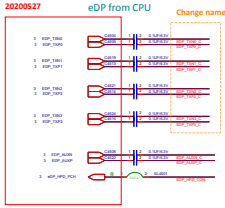
For EMI / For ESD



20200527 eDP from CPU

Change name Re-timer@20181023F

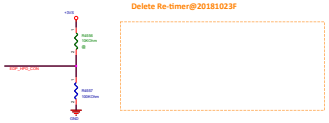
Delete Re-timer@20181023F



eDP_HPD (CPU)

Delete Re-timer@20181023F

Rename
@20181017H



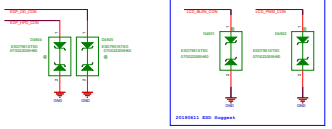
MIC module / MIC

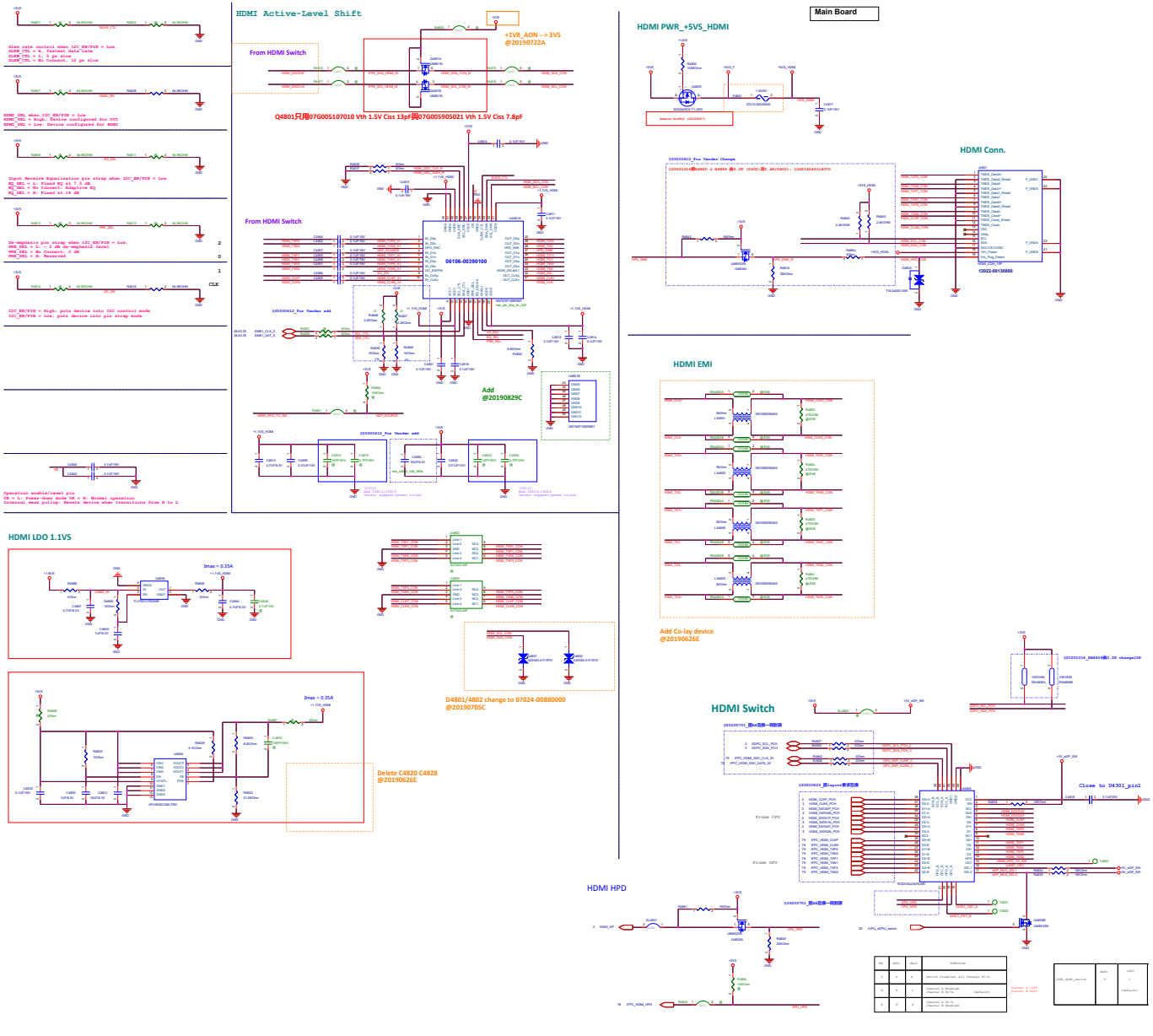
C4509 22PF --> 100PF
@20190719C

C4556 change to unmunt
R4507(10ohm) change to L4503
@20190102A

For ESD

Delete @20181022M




Main Board
HDMI Active-Level Shift
From HDMI Switch
+1V8_AON --> 3V5
@20190722A
Q4801只用07G005107010 Vth 1.5V Ciss 13pF與07G005905021 Vth 1.5V Ciss 7.8pF
From HDMI Switch
06106-00390100
Add
@20190829C
HDMI LDO 1.1VS
Imax = 0.35A
Imax = 0.35A
Delete C4820 C4828
@20190626E
D4801/4802 change to 07024-00880000
@20190705C
HDMI PWR_+5VS_HDMI
HDMI Conn.
120220-00130000
HDMI EMI
Add Co-lay device
@20190626E
HDMI Switch
Close to D4301_pin1
HDMI HPD
Design IP
Title : HDMI ReTimer_Revision
Dept.:

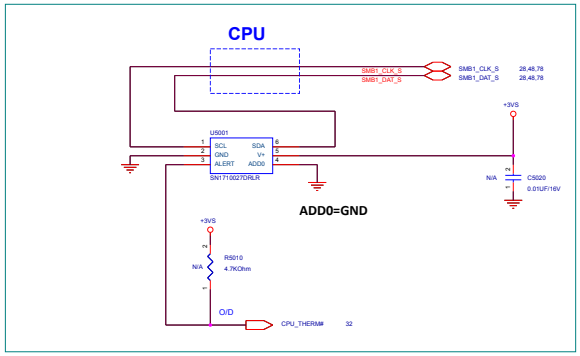
Main Board

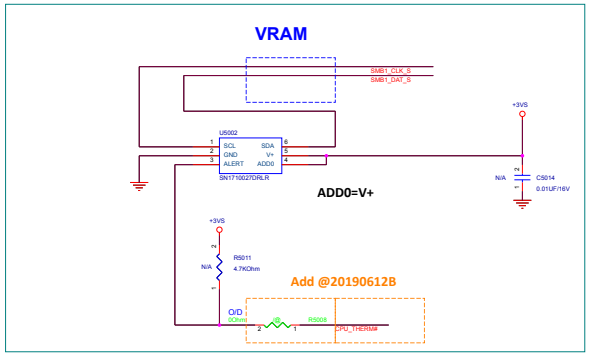
Thermal Sensor : SN170027

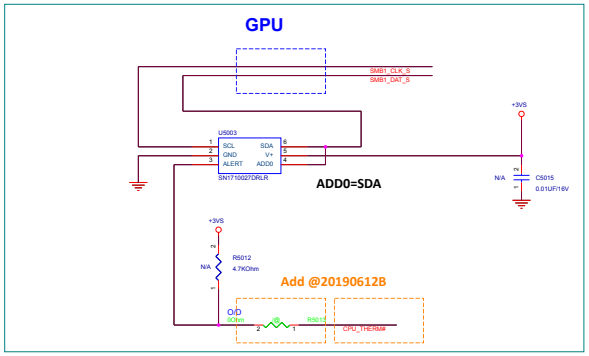
ALERT/SDA/SCL: Open-drain output; pullup resistor 5Kohm

Pin function Supply voltage.: 1.62 V to 3.6 V

@20200728_Modify thermal Del. 0 ohm







Near CPU

SMBUS addr=10010000 (90)

Near VRAM

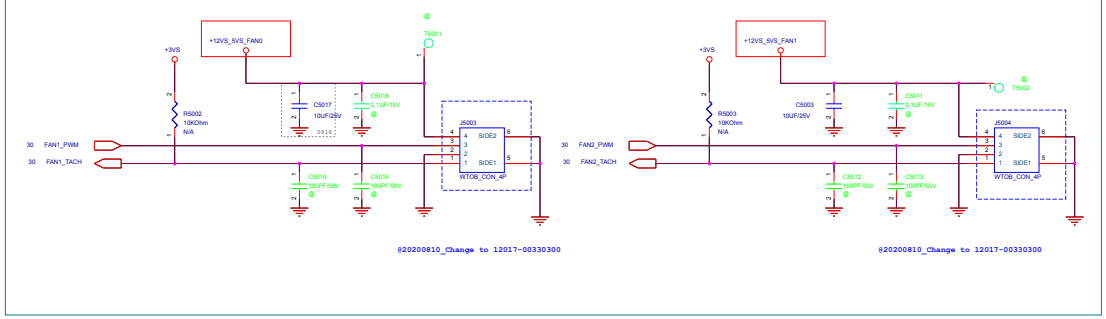
SMBUS addr=10010001 (91)

Near GPU

SMBUS addr=10010010 (92)

CPU&GPU FAN

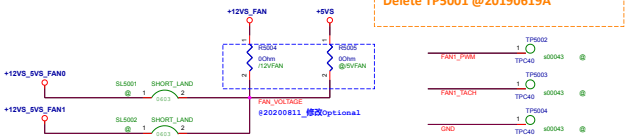
Note : connector and power are by project design



ADD0: Address select. Connect to GND, SDA, SCL, or V+

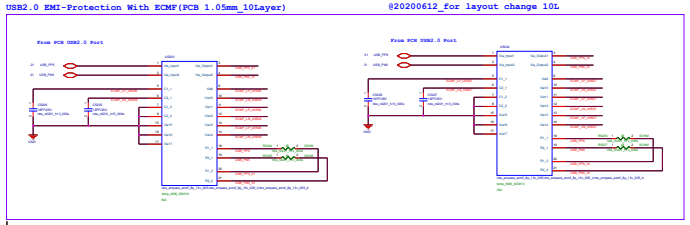
DEVICE TWO-WIRE ADDRESS		ADD0 PIN CONNECTION	Output
1001000	90	Ground	CPU
1001001	91	V+	VRAM
1001010	92	SDA	GPU
1001011	93	SCL	

Delete TP5001 @20190619A



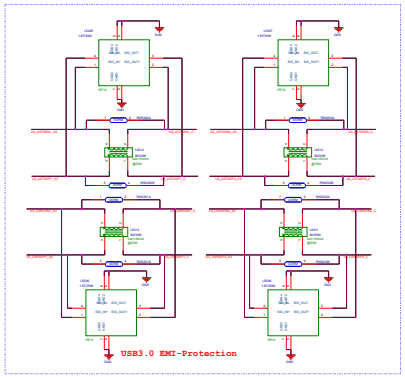
USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

@20200612_for layout change 10L

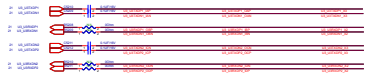


Note :
1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB layer
2. CS5048/CS503 / CS505&CS596 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
4. Pin13 to Pin16 are floated in regular scheme

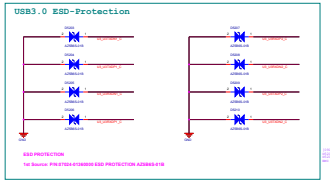
@20200401_ 更改封装LS205-09
@20200612_更改布局 For layout footprint
@20200615_15211-14 更改封装焊盘 For layout footprint & 修改焊接机械



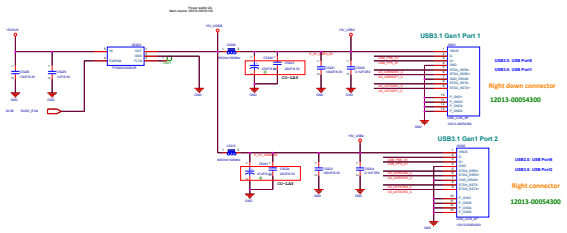
USB3.0_Port1 & USB3.0_Port2

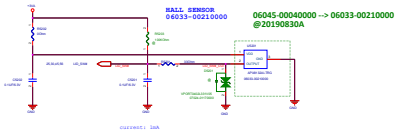


USB3.0 ESD-Protection



USB2.0 ESD-Protection



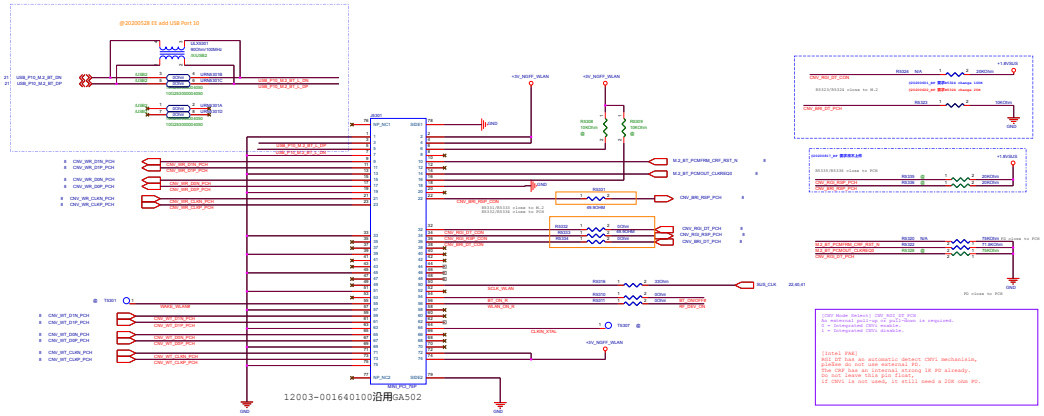


Project Name: UX482			Rev: 0A1
Title: AI_BD			
Size:	Drawn:	Engineer: EE	
Custom	Date: Friday, October 16, 2020	Sheet 1 of 1	

R1.1-02

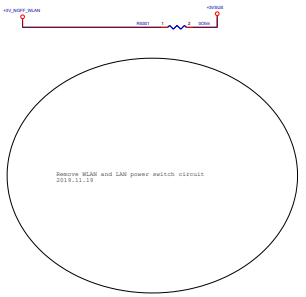
NGFF M.2 TYPE_E-KEY WIFI

Main Board



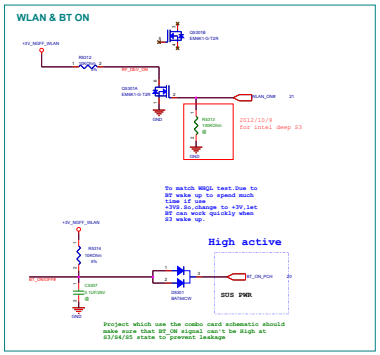
WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSOS

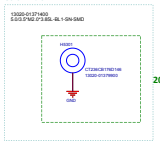


@20200611_del WLAN_Wake# Control for RF

WLAN & BT ON

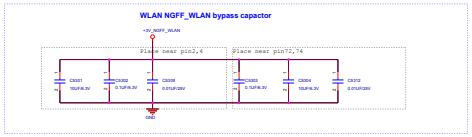


Screw Hole

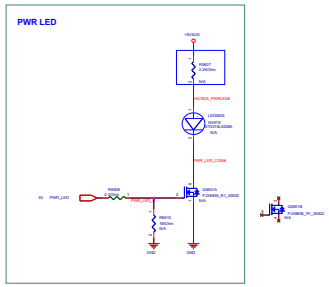


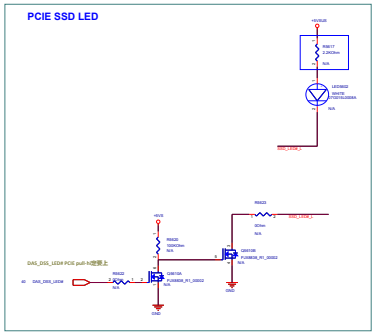
20200707 Rex 新增

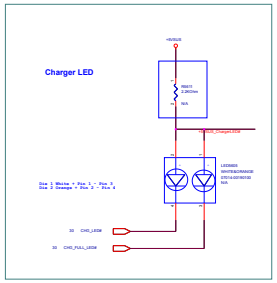
WLAN NGFF_WLAN bypass capactor



Title : WiFi/WiMax
Engineer: EE
Size: B
Project Name: GX502GX
Rev: 1.0
Friday, October 16, 2020
Sheet 93 of 102

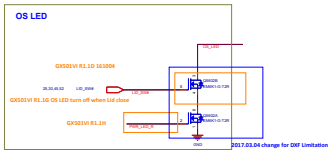


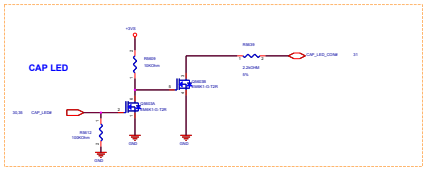


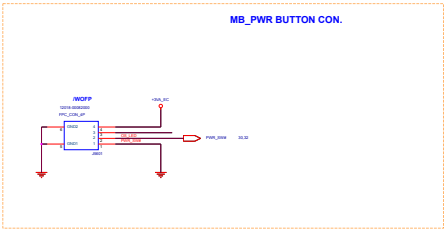


@20181013C

PWR LED PCIE SSD LED Charger LED







KB connector change to P.31
@20190731C

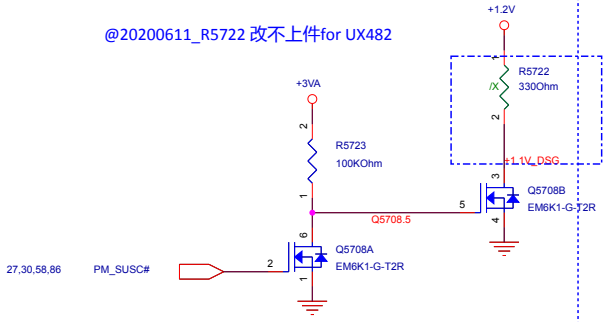
Change to monut @ 20181129A

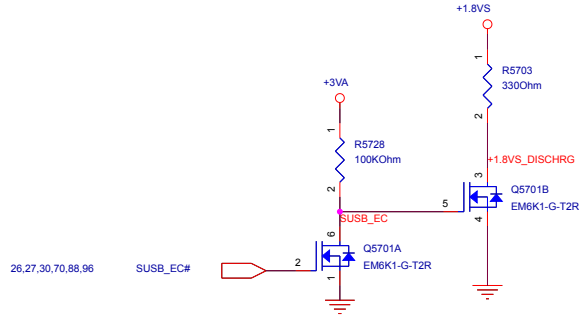
FP No	GA502 FP Pwrbtn	GA502 小板	GA502 小板 pin No
10	LED+	LED+	4
9	LED-	LED-	3
8	PWRBTN	PWRBTN	2
7	GND	GND	1
6	USB_D-	-	-
5	USB_D+	-	-
4	GND	-	-
3	SSO	-	-
2	ATC	-	-
1	RESETn	-	-

Justin : Removed no used Discharge circuit
1.8V ,VCCIO,+5VS load switch already build in 180~260 ohm discharge function

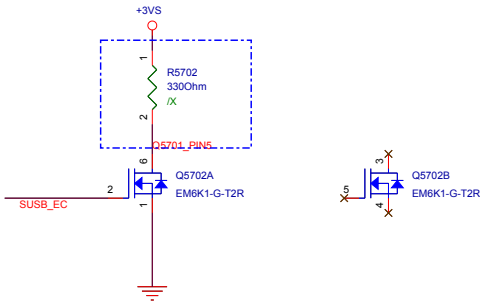
+1.1V DISCHARGE

@20200611_R5722 改不上件for UX482

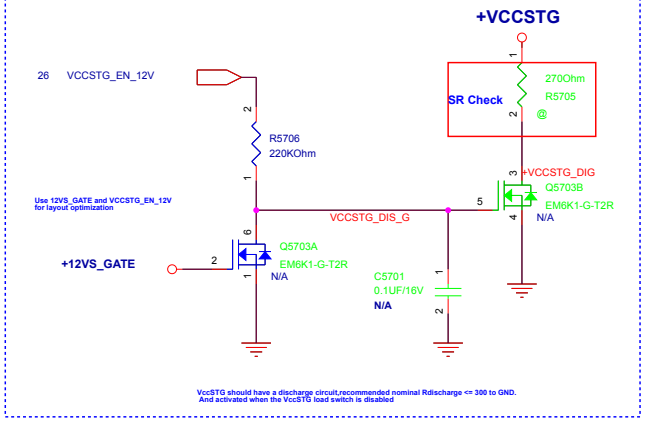




@20200611_R5702 改不上件for UX482

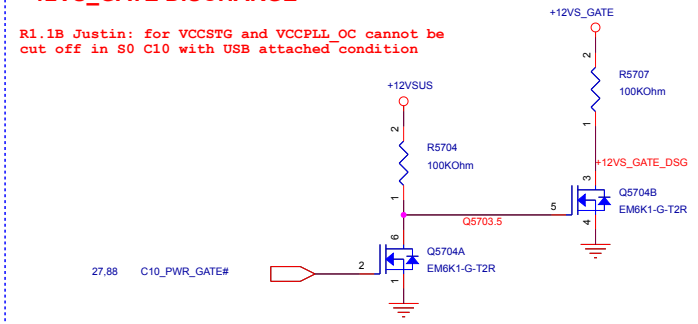


+VCCSTG

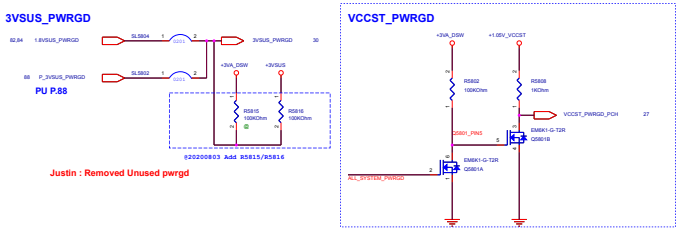


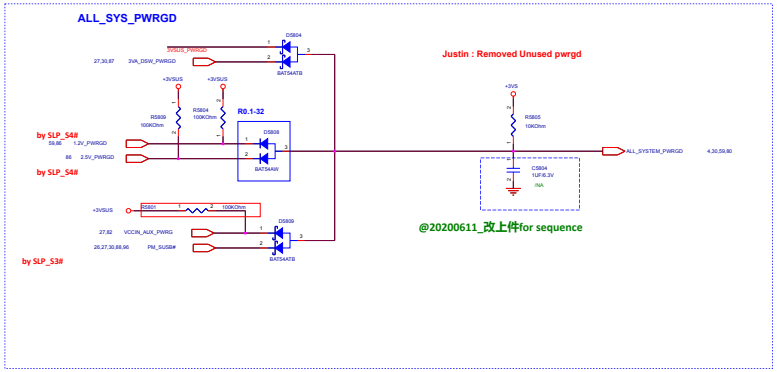
+12VS_GATE DISCHARGE

R1.1B Justin: for VCCSTG and VCCPLL_OC cannot be cut off in S0 C10 with USB attached condition

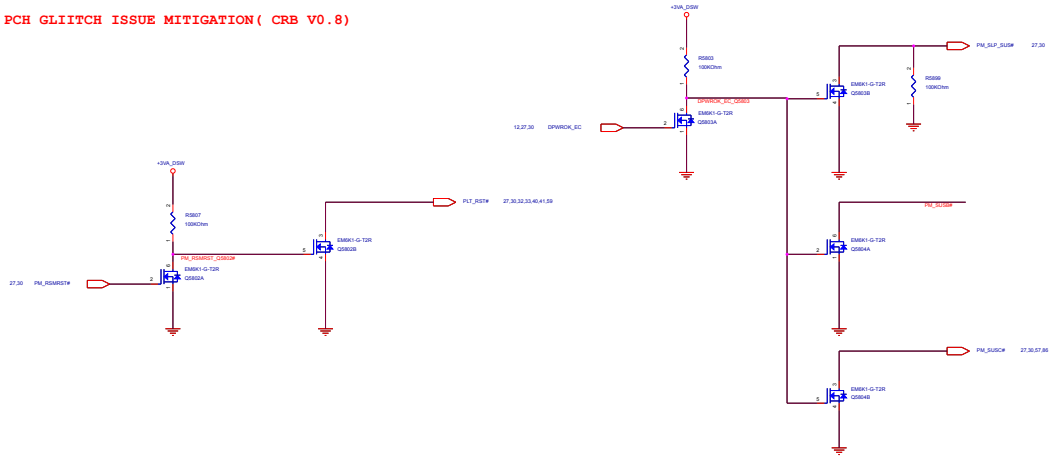


Main Board



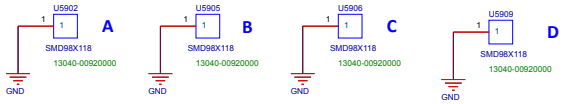


CNL PCH GLIITCH ISSUE MITIGATION(CRB V0.8)

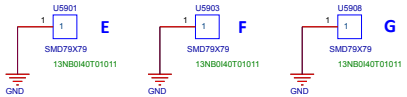


ASUS	Project Name: UX482		Rev: 00.1
Title : PRO_Protect			
Size: C	Dept.: NB1-RD2EE2	Engineer: EE	
Date: Friday, October 16, 2020	Sheet 59 of 102		

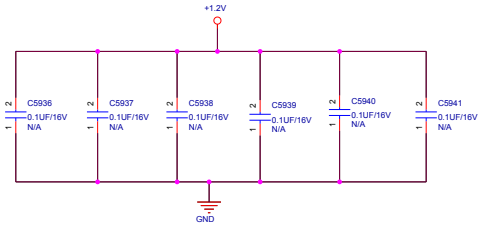
SMT EMI GASKET 2*2*2 13NR01N0T13011



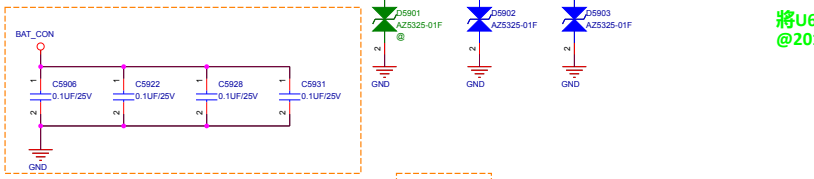
SMT EMI GASKET 2*1.5*2 13040-00850100



@20200708_SI CPU PI DC&AC sol: add 6PCS 0.1uF

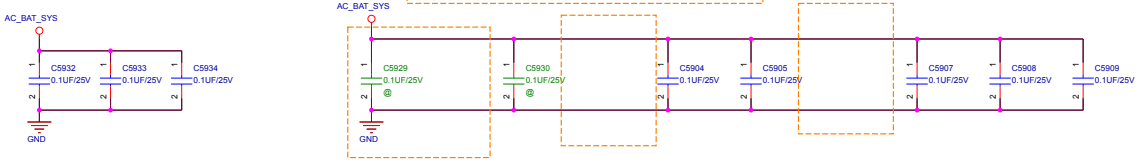


EMI request @20181026A

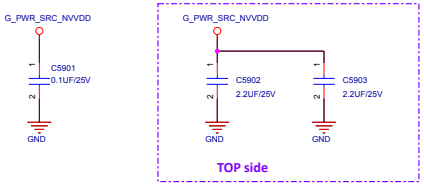


將U6904, U6908(改裸銅), U6905(改裸銅) 移除
@20181122C

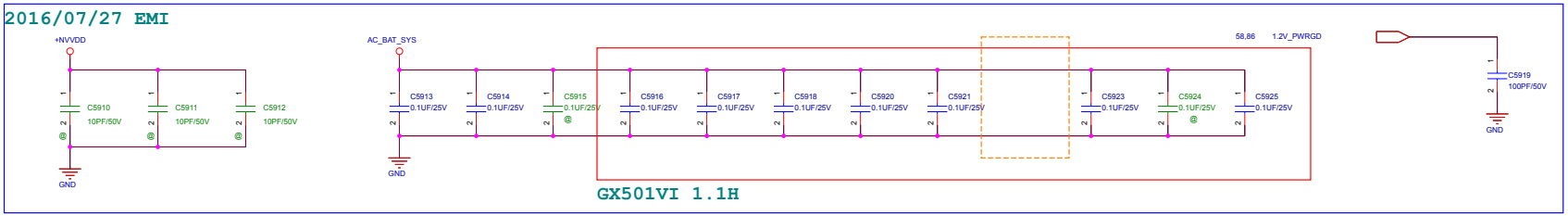
2017/04/05 EMI

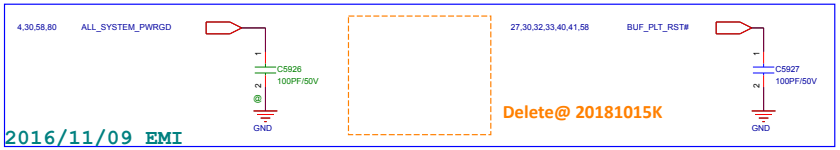


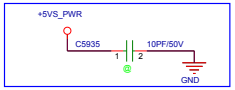
4/2 for EMI



2016/07/27 EMI







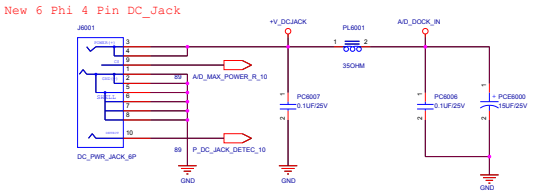
<Core Design> 2017.05.02 EMI Reserve

ASUSTeK COMPUTER	Title : OTH_EMI	
	Engineer: EE	
Size: B	Project Name: GX502GX	Rev: 1.0
Date: Friday, October 16, 2020	Sheet 59 of 102	

Main Board

DC-IN Connector

DC Jack使用請詢用River_Hsu



CHIP Cap (H=2.1)

J6001	3.4CH	1.55CH
	12033-00020200	12033-00020300

Battery Connector

12017-00080400

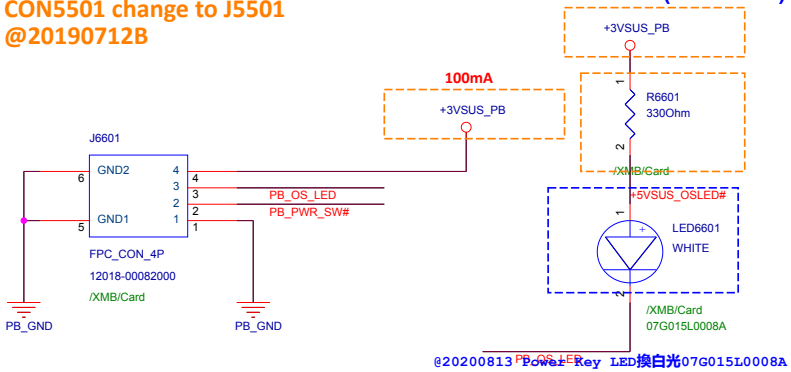
Note:Battery Connector 正確性與BAT1_IN_OC#是否預留!

Project Name: GA502IV			Rev: R1.0
Title : DC & BAT IN			
Size: A3	Dept.: NB_Power team	Engineer: CS Lin	
Date: Friday, October 16, 2020	Sheet 60 of 102		

Connected to MB Page56

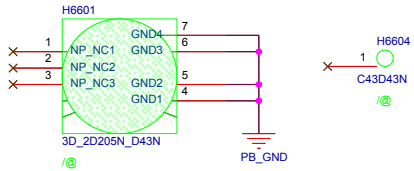
CON5501 change to J5501
@20190712B

OS LED (PWRBTN)

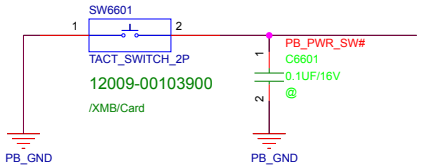


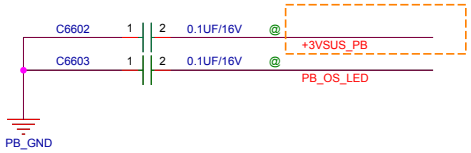
+5VSUS_PB --> +3VSUS_PB
R5510 750 OHM --> 330 OHM
@20190708A

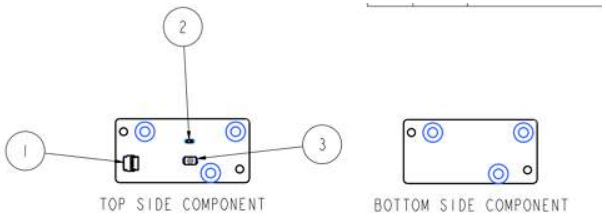
Change @20181026B



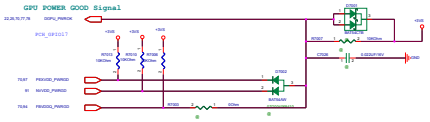
POWER button



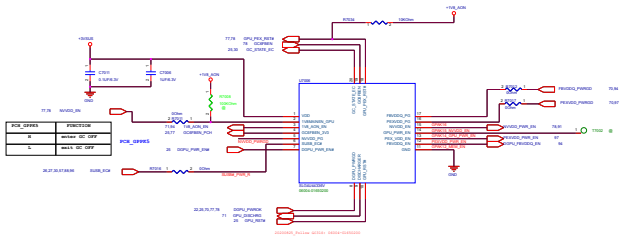




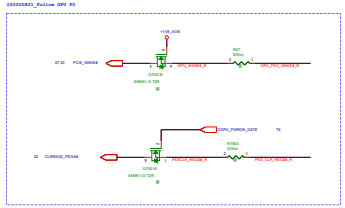
ASUSTeK COMPUTER	Title : IO Con. to MB	
	Engineer: EE	
Size: A	Project Name: GX502GX	Rev: 1.0
Date: Friday, October 16, 2020	Sheet 66 of 102	



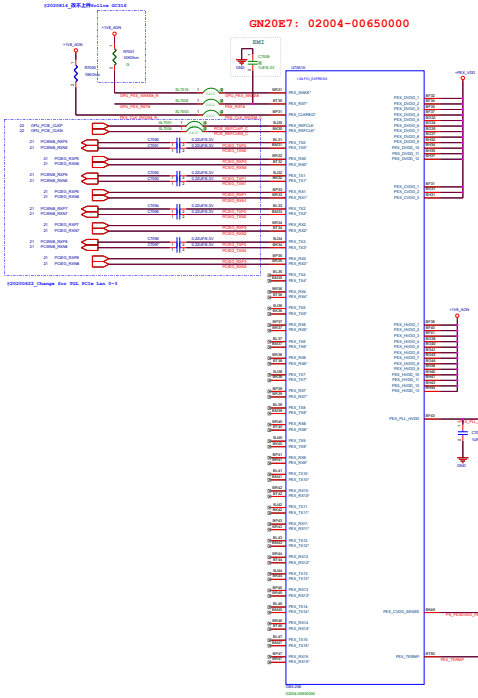
GPU POWER SEQUENCE CONTROL

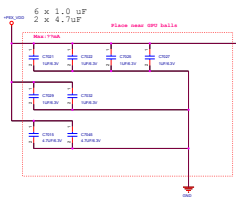


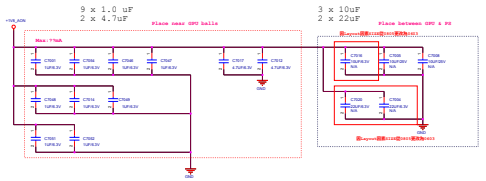
PCB_GPIO5	FUNCTION
H	enter GC OFF
L	exit GC OFF



GN20E7: 02004-00650000

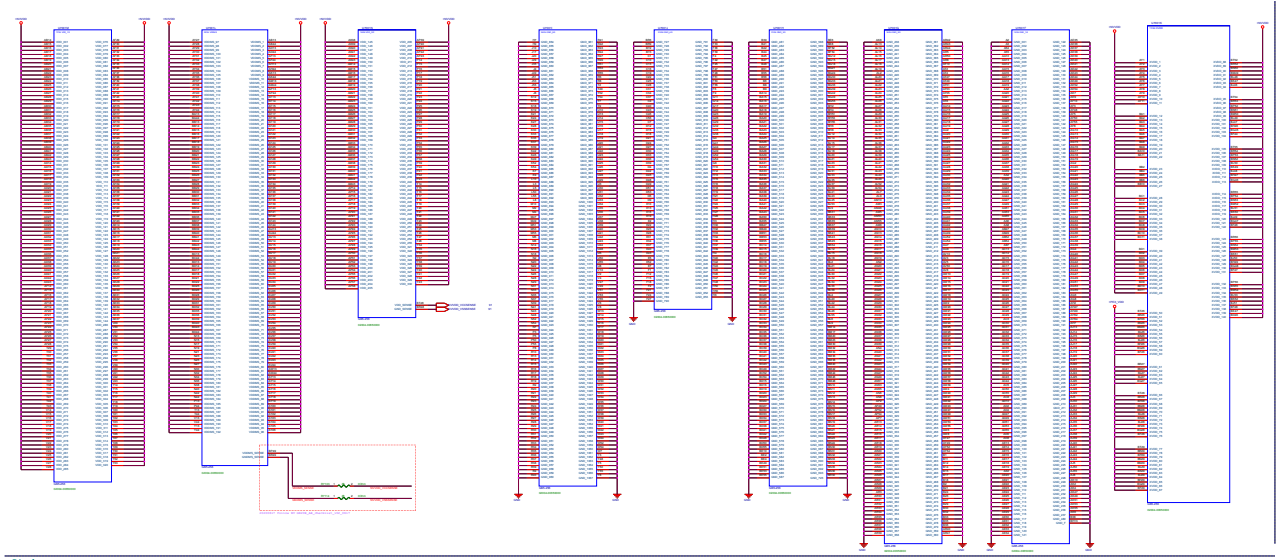


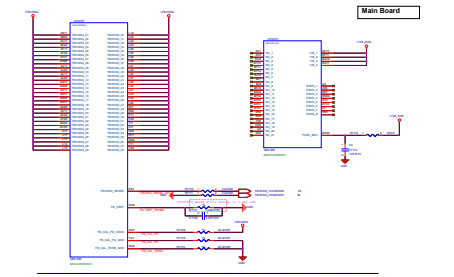


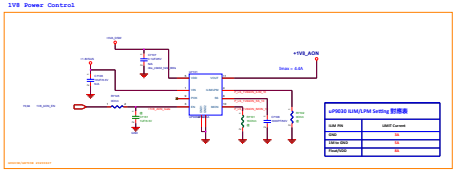


Main Board

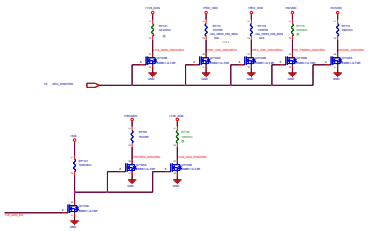
Project Name	GX502GX
Title :	GPU_PCIE1F
Size	
Custom	
Dept. :	
Engineer:	
Date :	Friday, February 19, 2021
Sheet	51 of 100

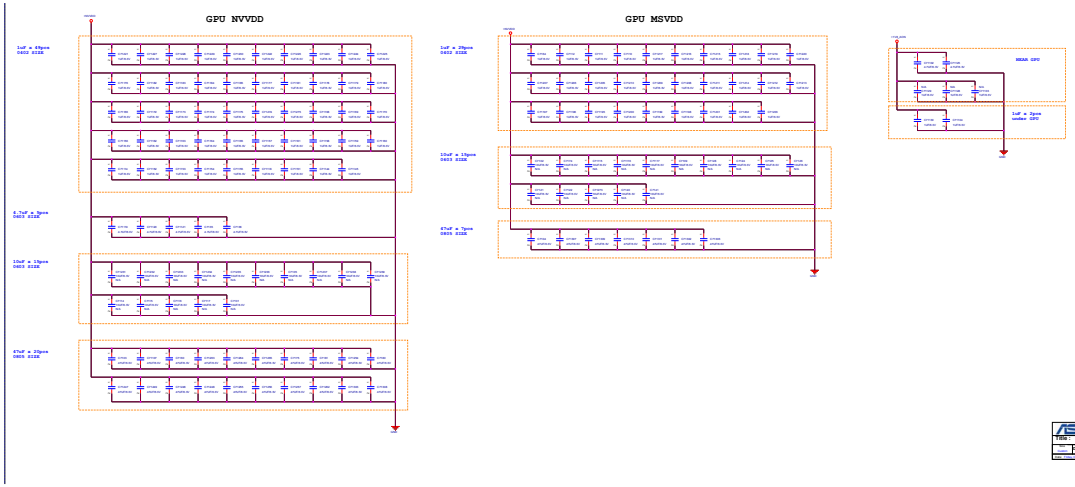






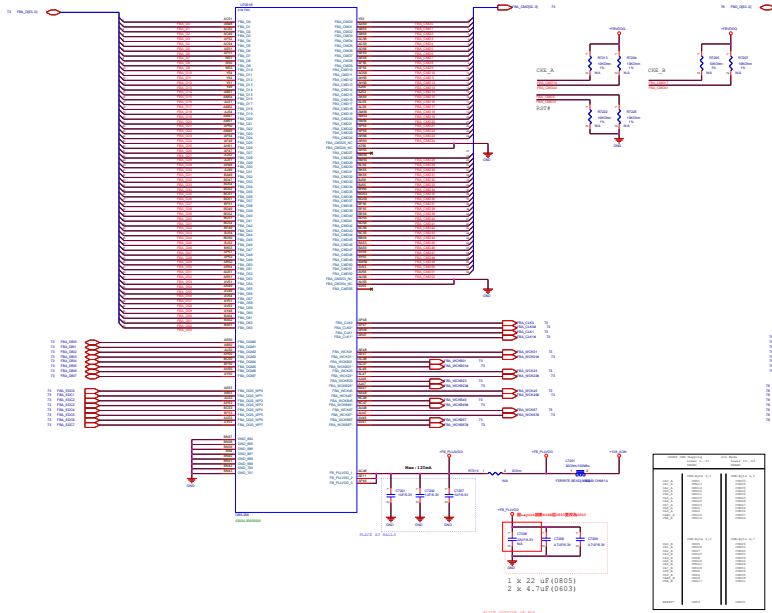
Discharge



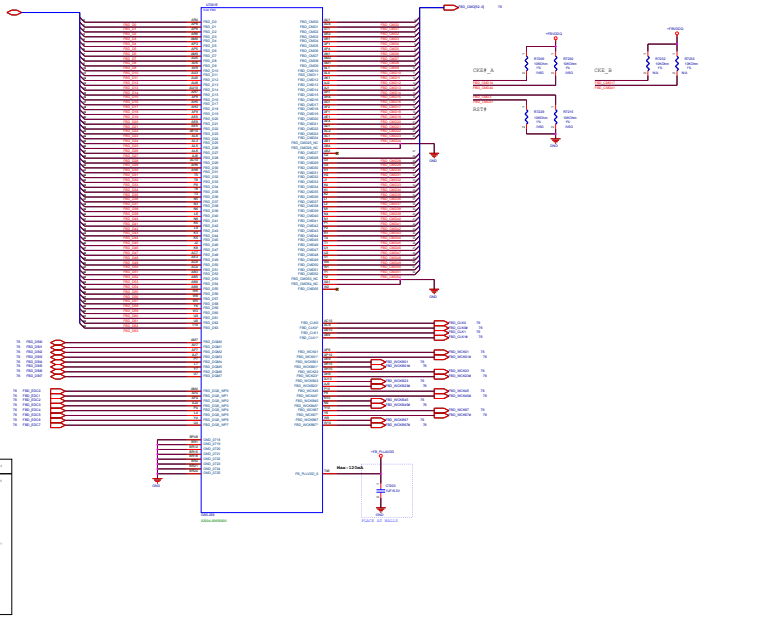


ASUS	Compal Electronics, Inc.	
	GX502GX	
TITLE : GPU_POWER		
Size:	Project name:GX502GX	Engineer: BE
Date:	Sheet of	

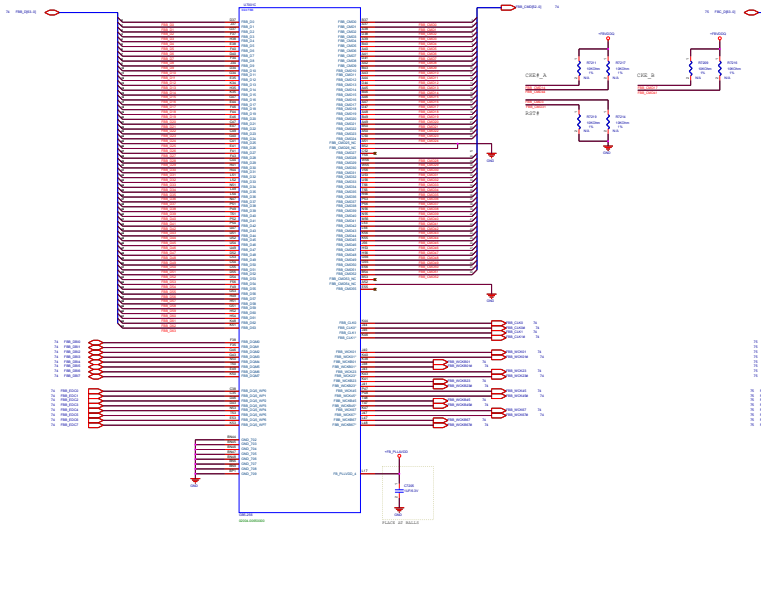
MEMORY: GPU FB Partition A



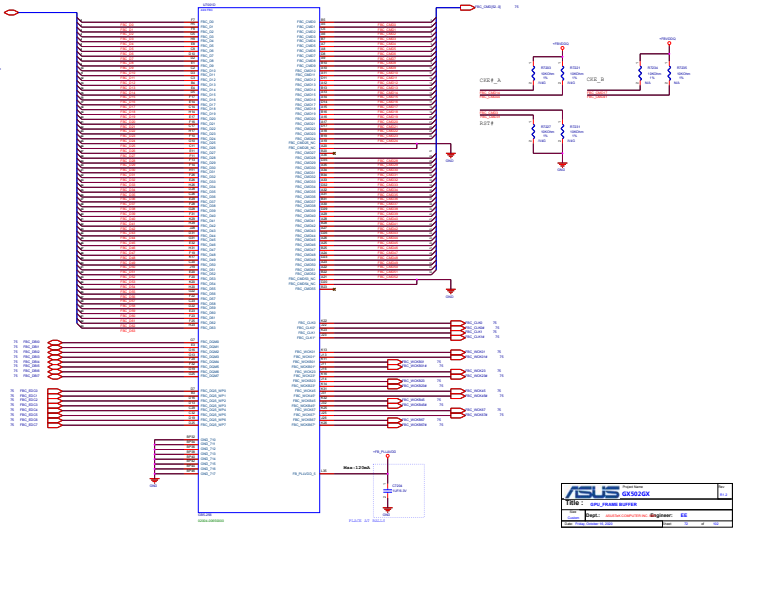
MEMORY: GPU FB Partition D



MEMORY: GPU FB Partition B



MEMORY: GPU FB Partition C

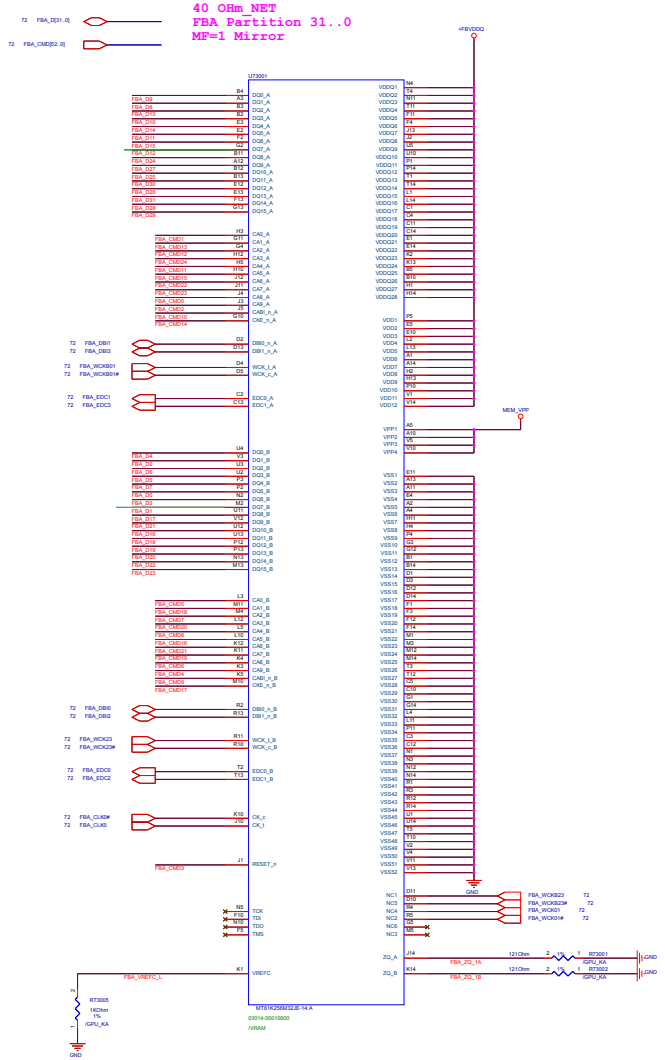


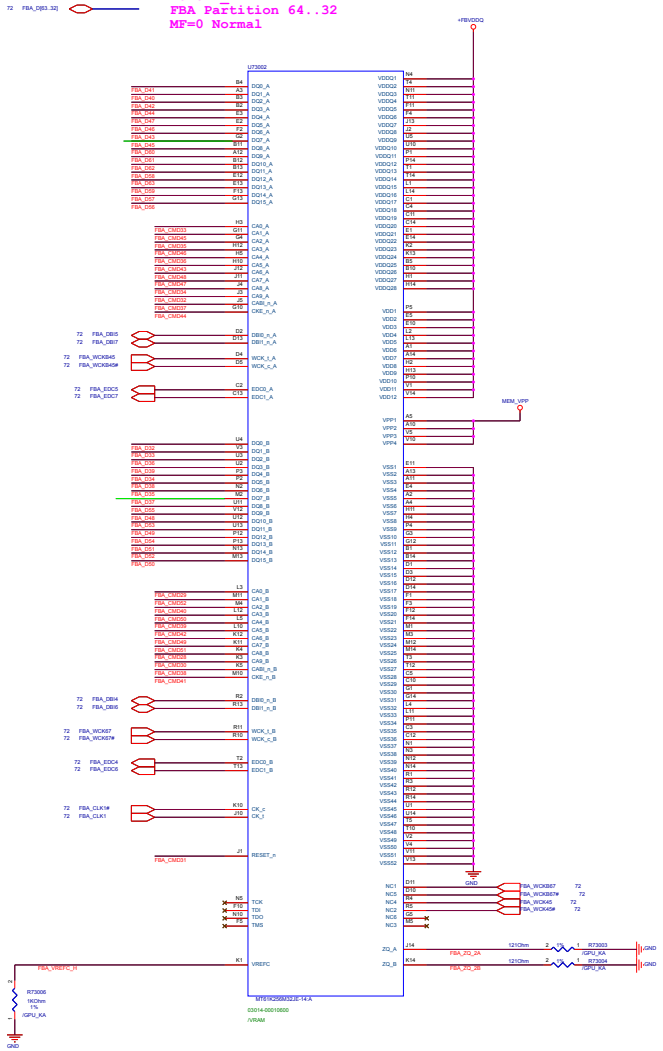
1 x 22 uF(0805)
2 x 4.7uF(0603)

PLACE OUTSIDE OF BGA

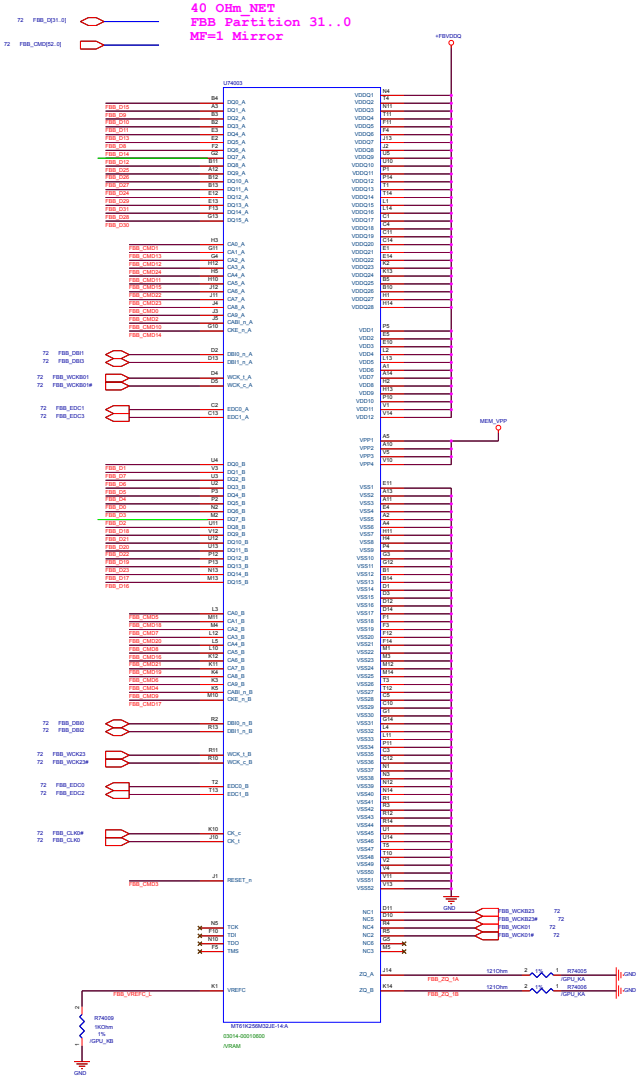
ASUS	Project Name: GX502GX		Rev: 1.1
Title: DRAM SUPPLY			
Size:	Document Number:	Engineer: EE	
Date: Friday, December 06, 2019	Sheet: 72 of 102		

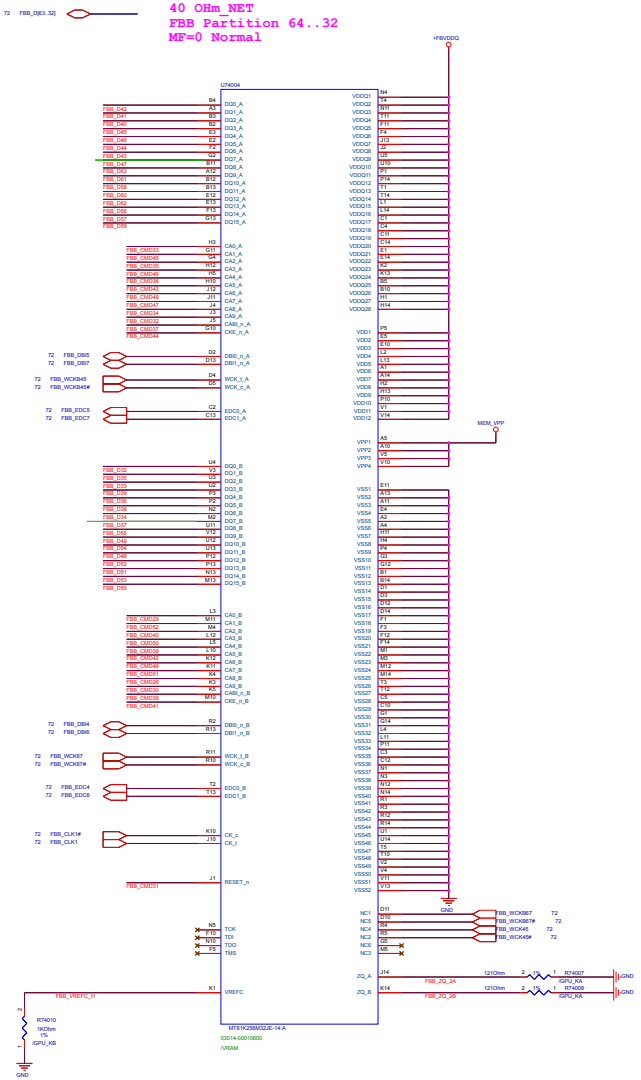
@20200705_Memory P/N
Samsung_256*32_K4Z80325BC : 03014-00010600(目前
Micron_256M*32_MT61K256M32JE: 03014-00010500





@20200705_Memory P/N
Samsung_256*32_K4Z80325BC : 03014-00010600(目前
Micron_256M*32_MT61K256M32JE: 03014-00010500





@20200705_Memory P/N
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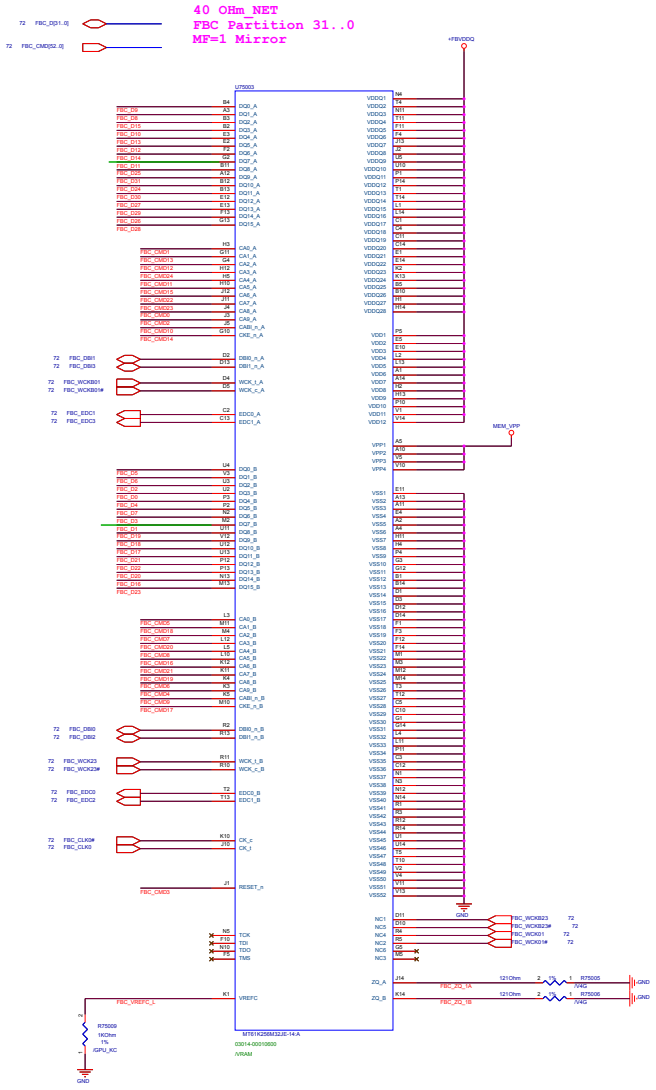
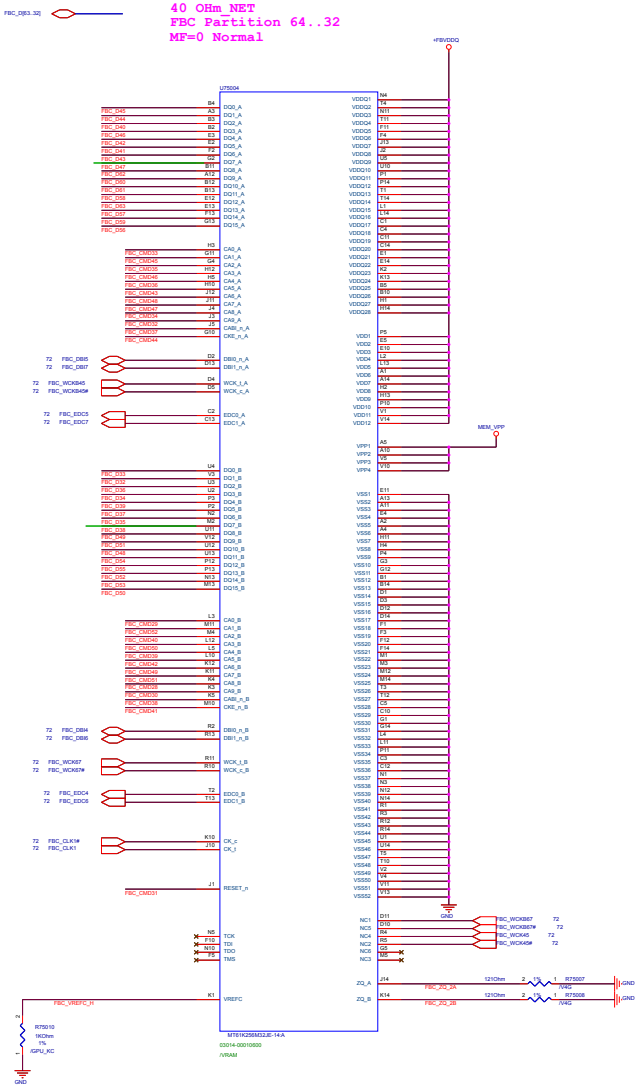
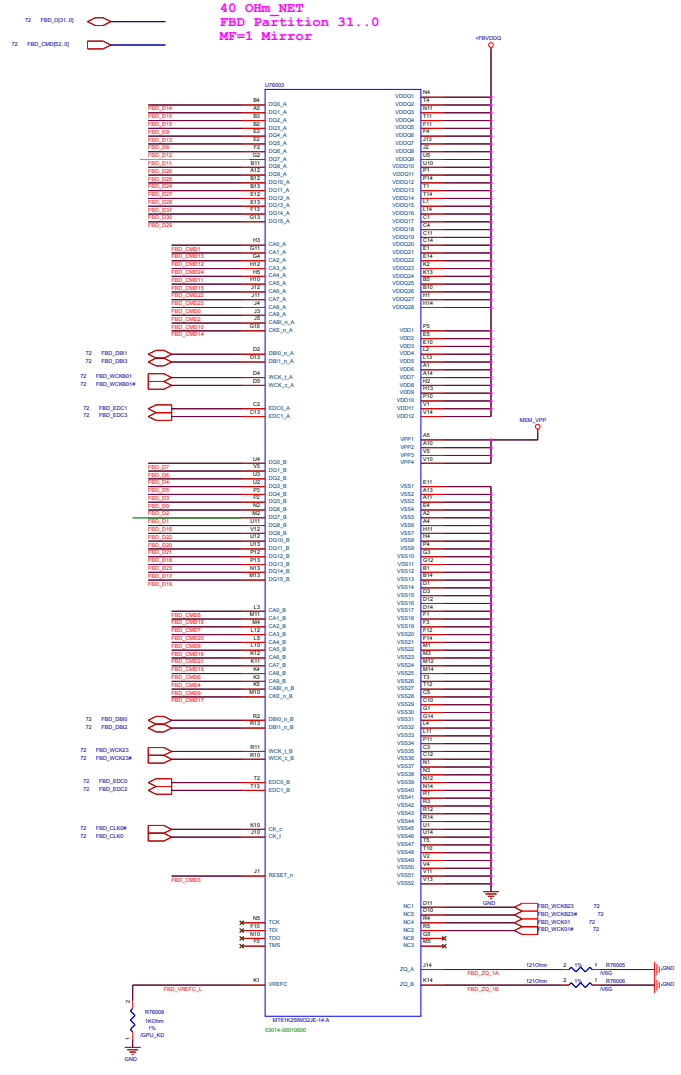
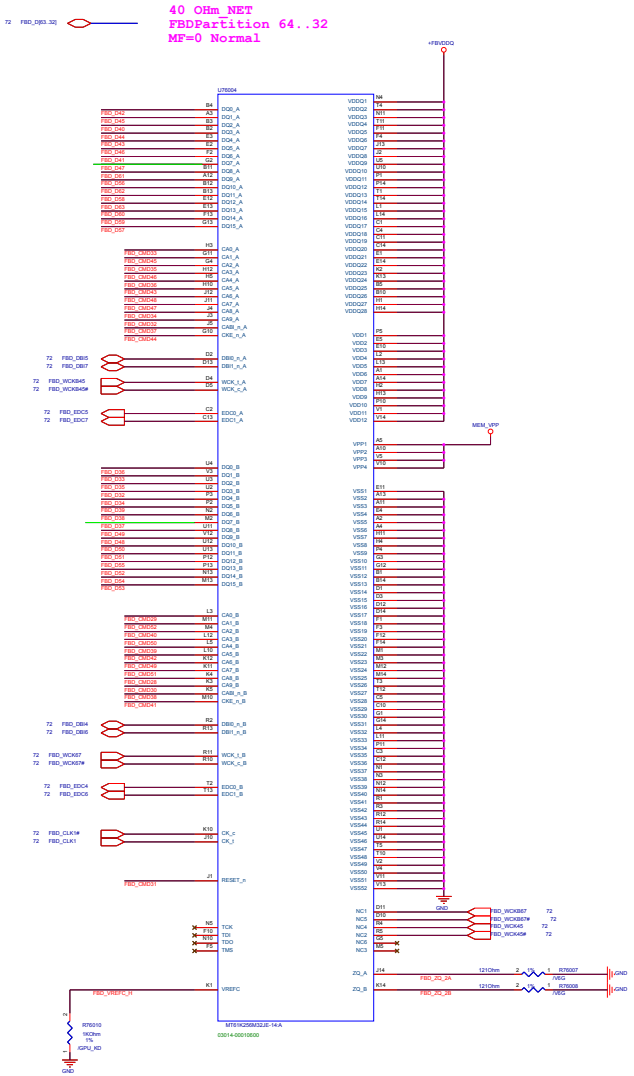
Micron_256M*32_MT61K256M32JE: 03014-00010500





@20200705_Memory P/N
Samsung_256*32_K4Z80325BC : 03014-00010600(目前
Micron_256M*32_MT61K256M32JE: 03014-00010500

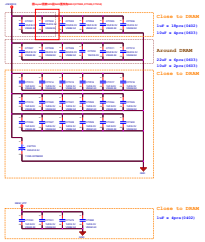


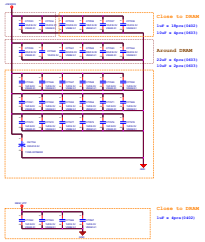


FBVDDQ
VRAM side

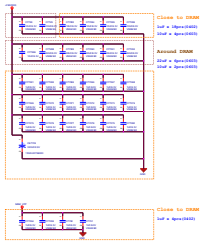
FBVDDQ
GPU side

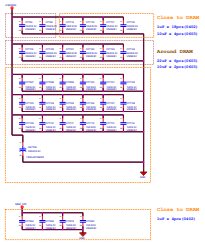
Channel A



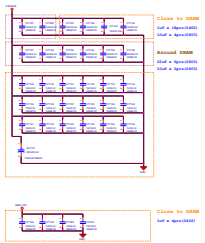


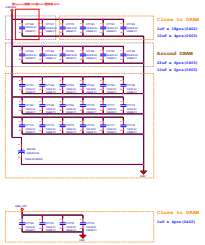
Channel B



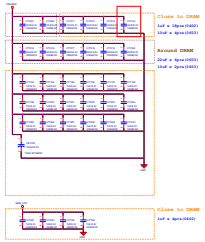


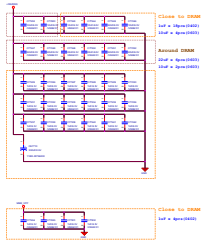
Channel C



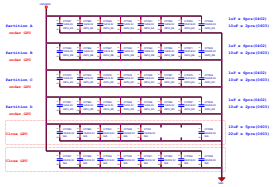


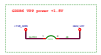
Channel D

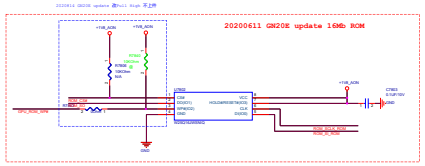


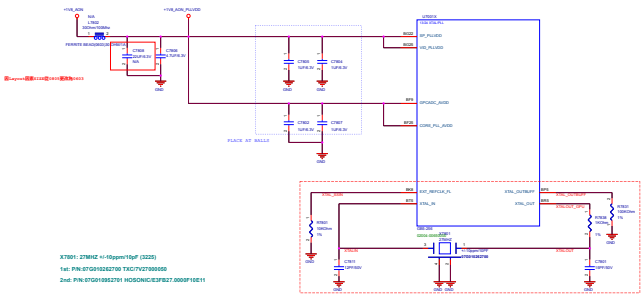


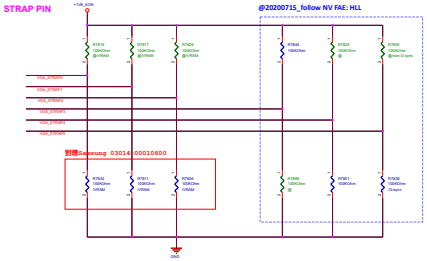
VRAM PWR_FBVDDQ

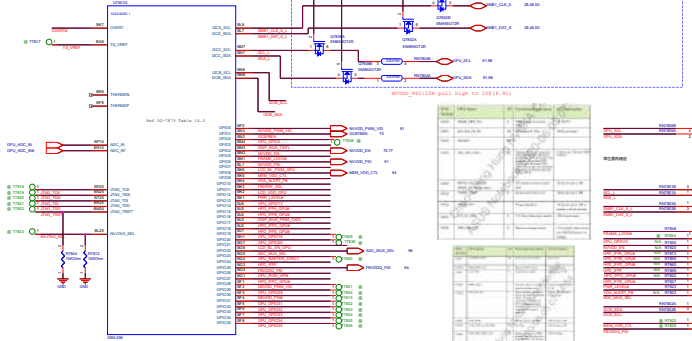


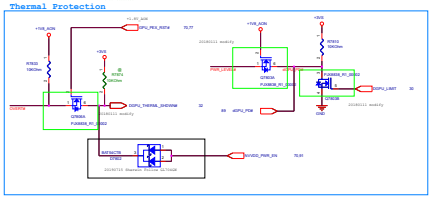


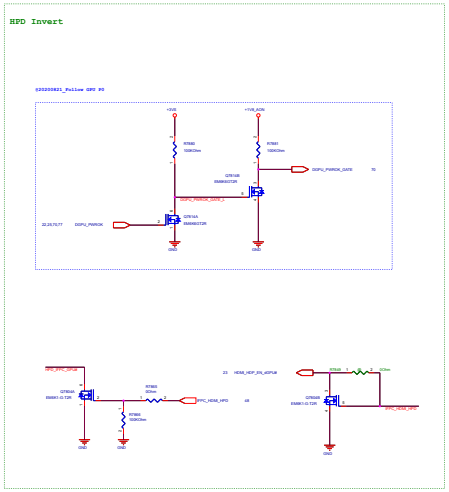

20200611 GN20E update 16Mb ROM

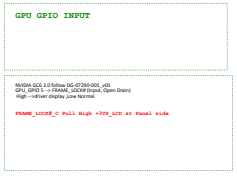

X7801: 27MHZ +/-10ppm/10pF (3225)
1st: P/N:07G010262700 TXC/7V27000050
2nd: P/N:07G010952701 HOSONIC/E3FB27.0000F10E11


STRAP PIN
@20200715_follow NV FAE: HLL
@20200705_follow NV FAE: LLH (Default)
Samsung 03014-00010600

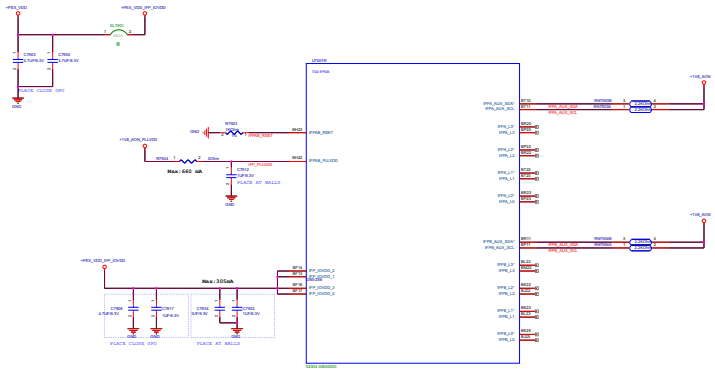

VGA INT. Thermal sensor
address 0x9E and 0x9C
@20200821_follow GPU P0

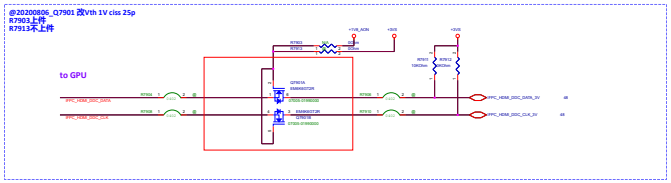

Thermal Protection


HPD Invert
@20200821_follow GPU P0

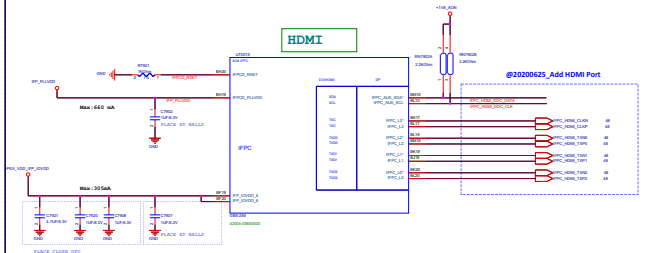

GPU GPIO INPUT

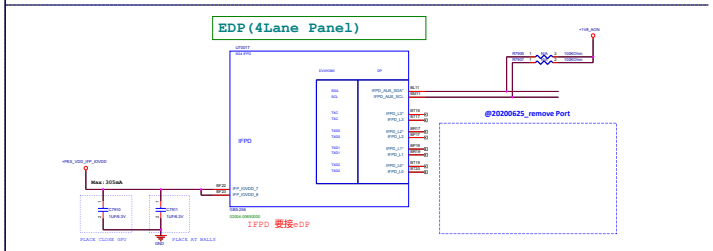

For EMI

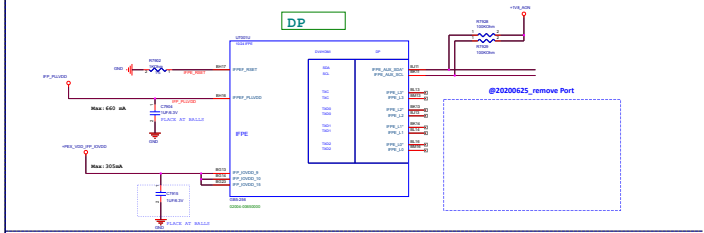


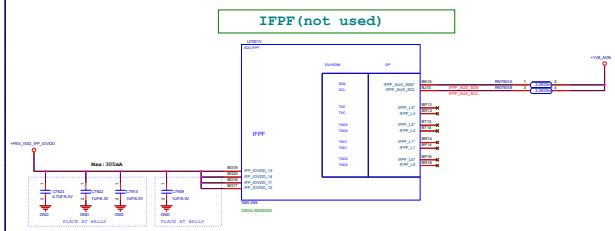


Main Board









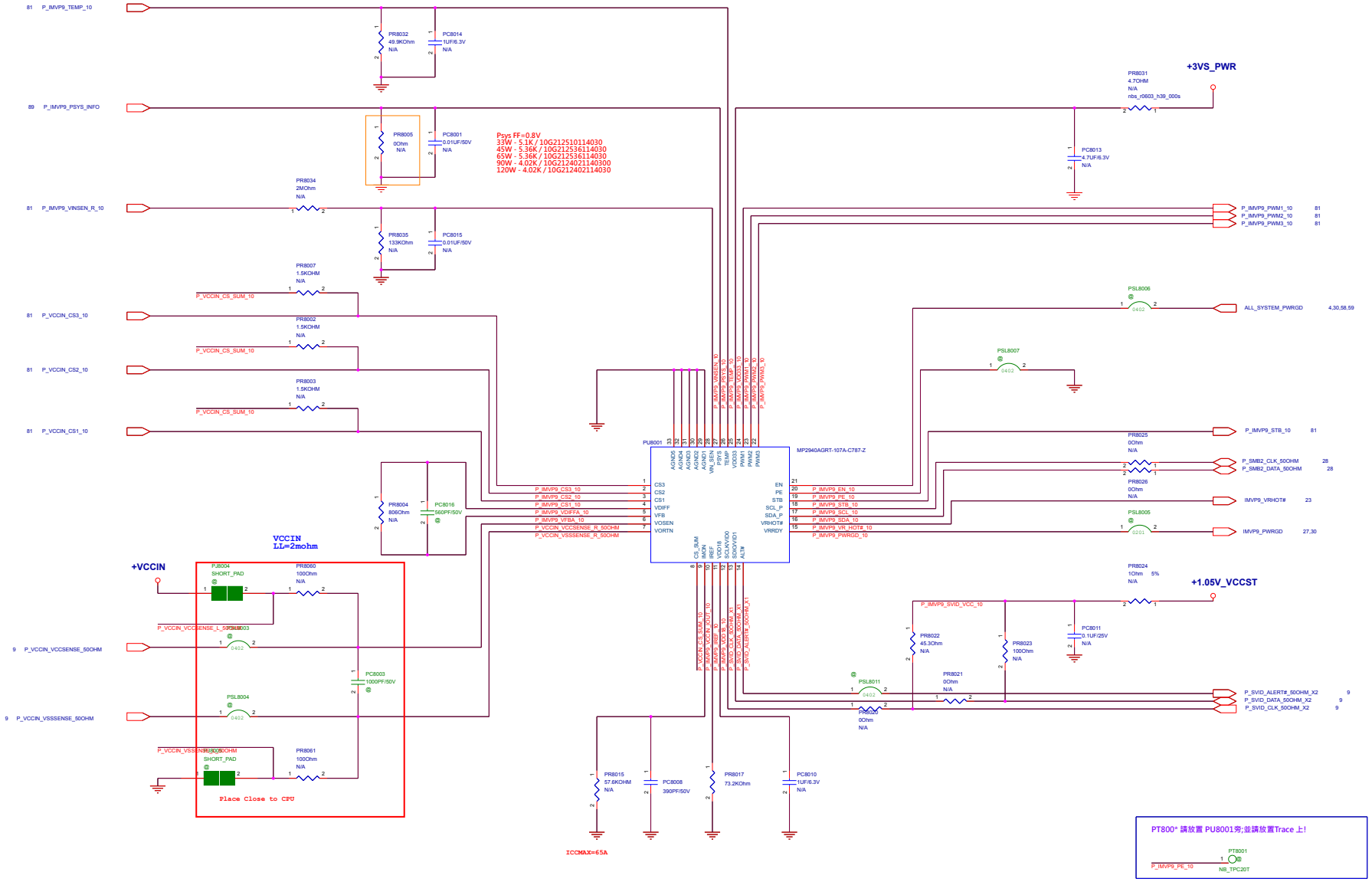
7.2 Unused pins

If an IFP link is unused, in general it should be left disconnected. This includes Main and Aux links. IFPx_RSET and IFPx_PLLVDD (x = A/B/C/D/E/F) can be left disconnected if neither of IFPx / IFPy is in use. For example, if neither link of the IFPA/IFPB may/may not be used, then IFPAB_PLLVDD and IFPAB_RSET should be left disconnected, or both signals and references associated with Link A and Link B should also be left unconnected.

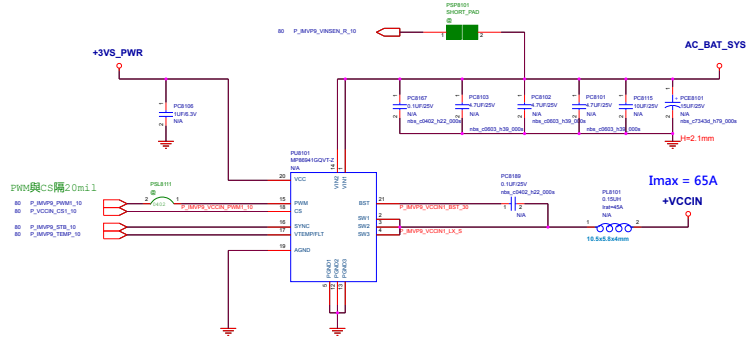
IFP_IOVDD rail can be left unconnected if no IFP link is used. If any IFP is used, all IFP_IOVDD balls must be connected to power rail.

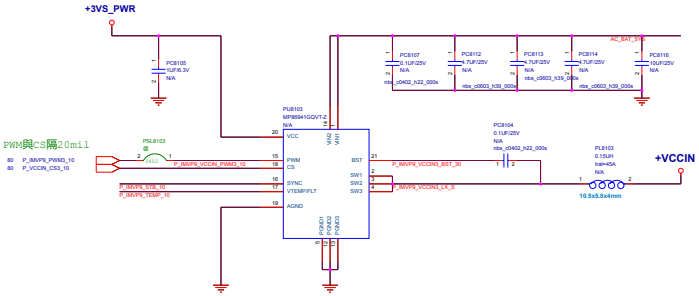
ASUS	Project Name: GX502GX	Rev:
Title : GPU_DP/EDP/HDMI/LVDS/CRT		
Size:	Dept.: ASUSTeK COMPUTER INC.	Engineer: EE
Custom		
Date: Friday, October 16, 2020	Sheet 76 of 102	

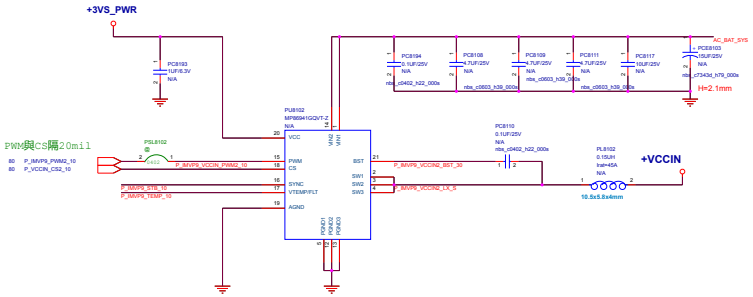
TGL IMVP9 (1) Power [For CPU]

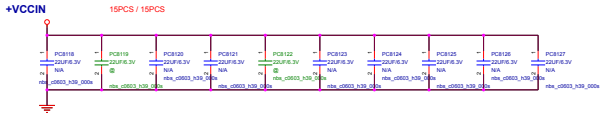


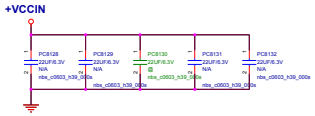
TGL IMVP9 (2) Power [For CPU]

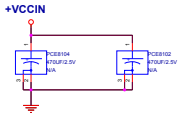




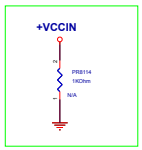




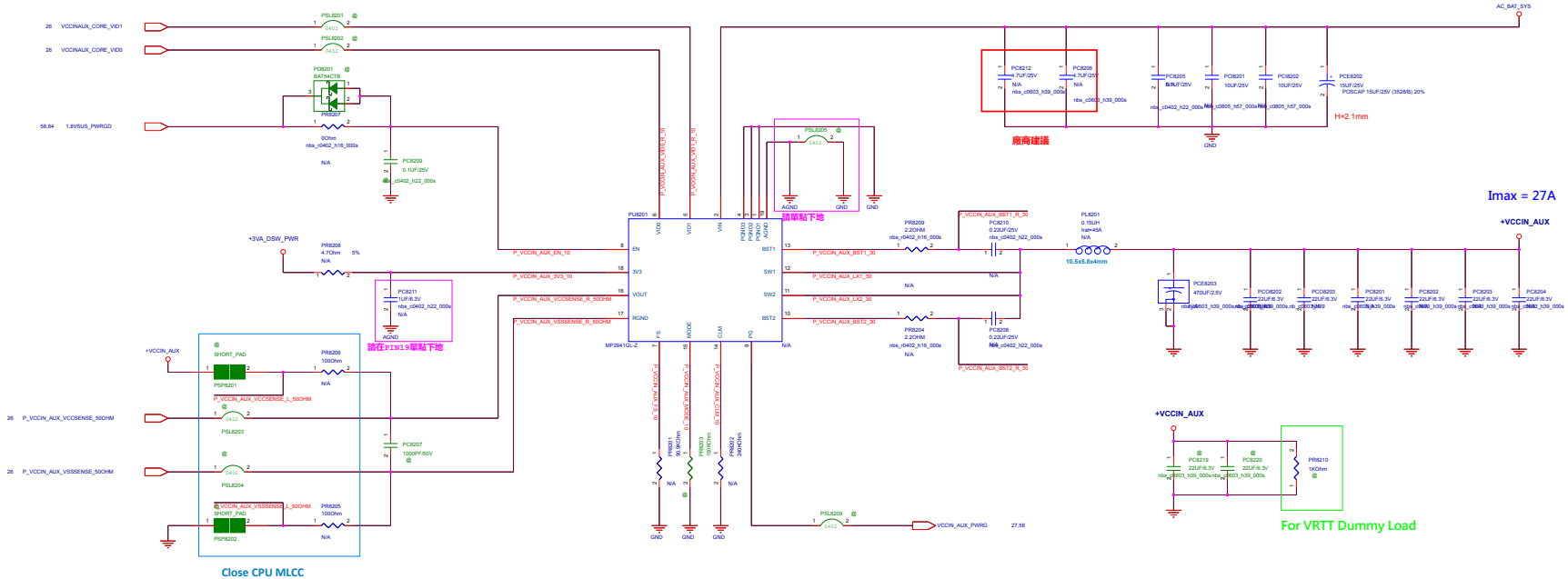




For VRTT Dummy Load



TGL IMVP9 (3) Power [For CPU]



<Variant Name>

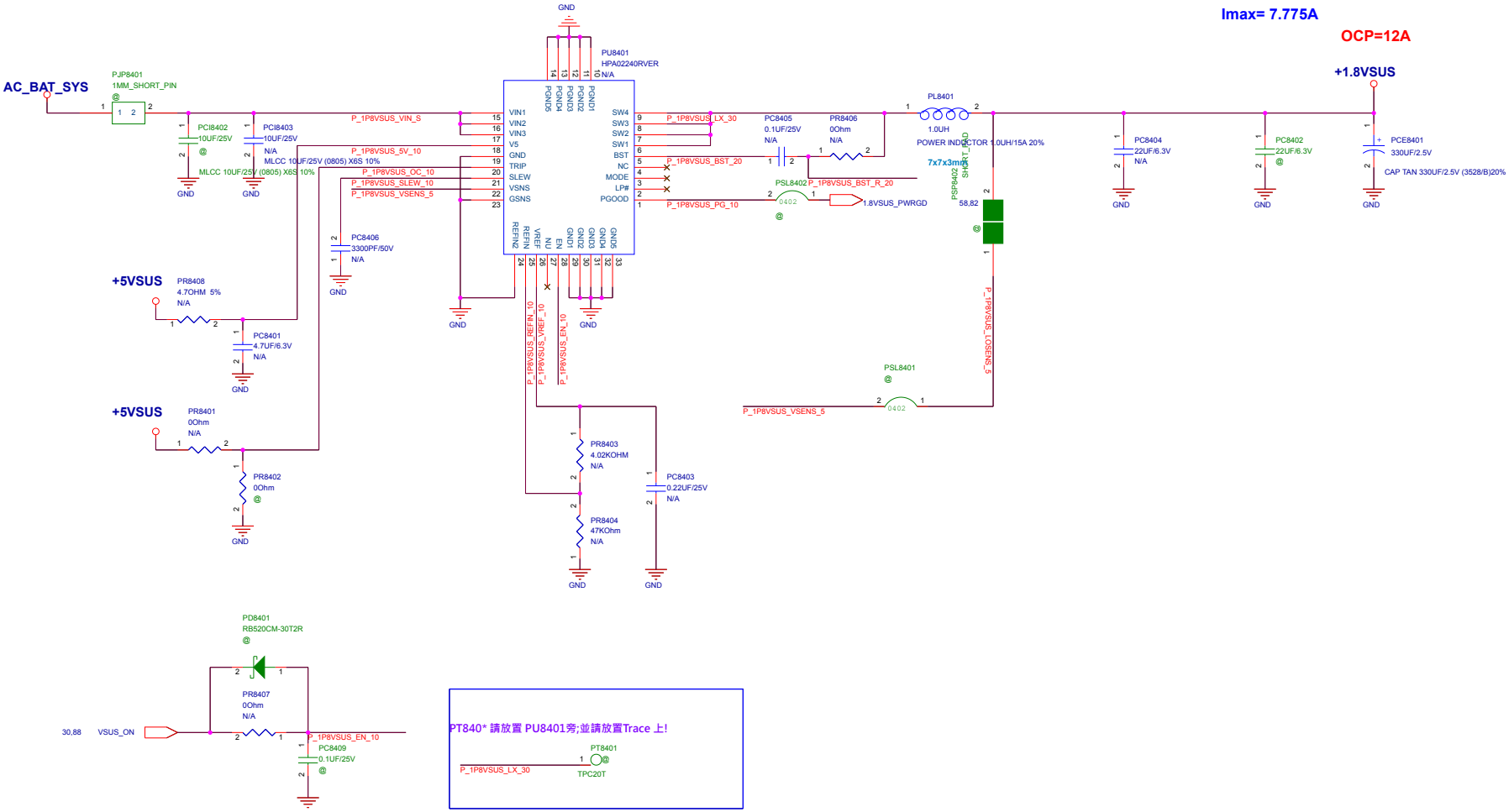
Project Name: FX516 | Rev: R0.1

Title : ICE LAKE IMVP9

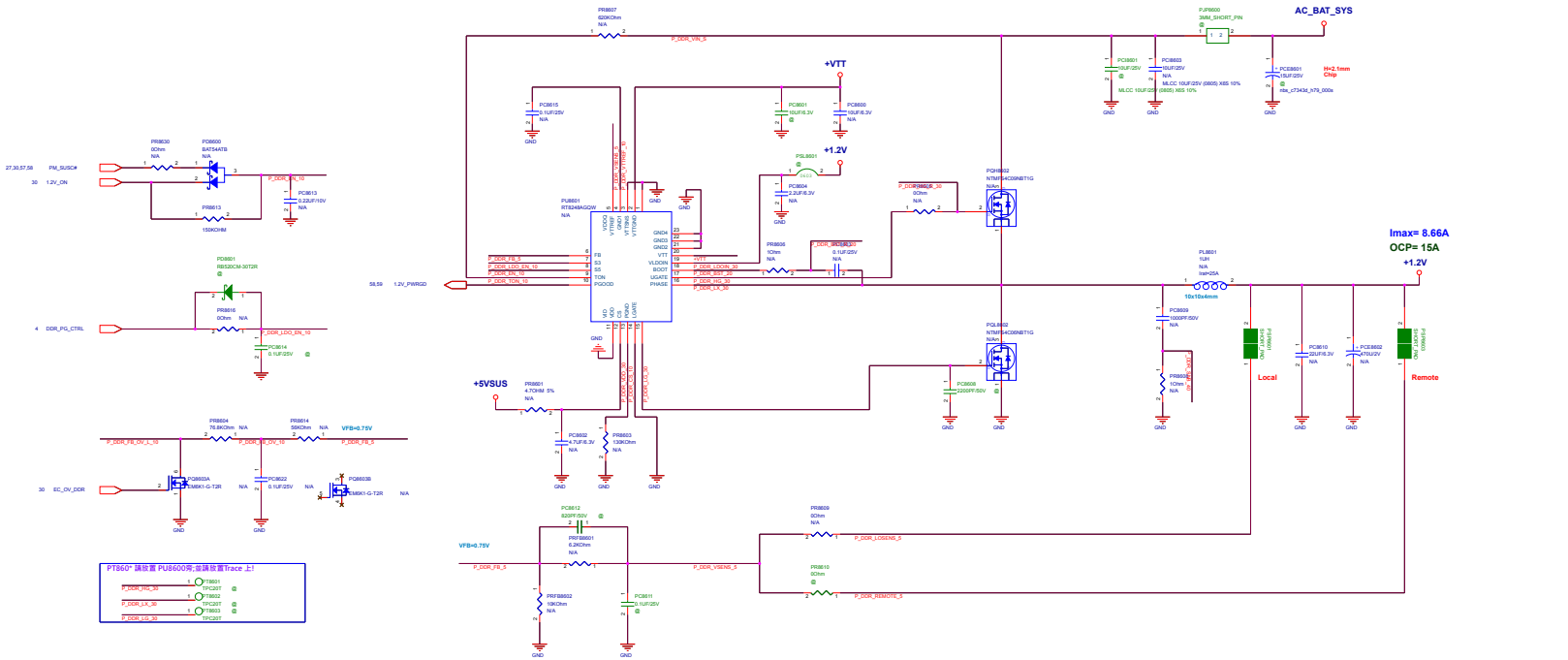
Size: Custom | Dept.: NB1-ROSE2 | Engineer: Matt

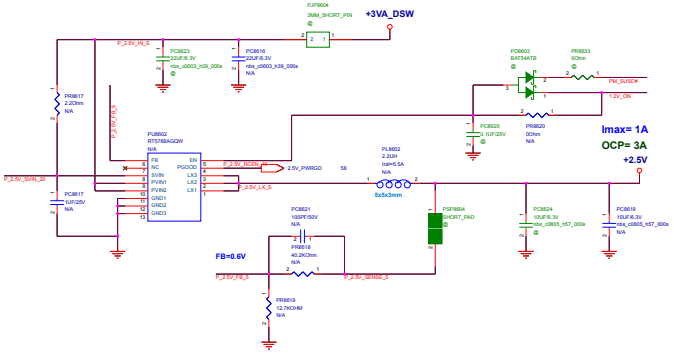
Date: Friday, October 16, 2020 | Sheet 82 of 102

+1.8VSUS [For PCH]



+1.2V / +VTT / +2.5V[For Memory]





<<Core Design>>

Project Name: Tiger Lake-H

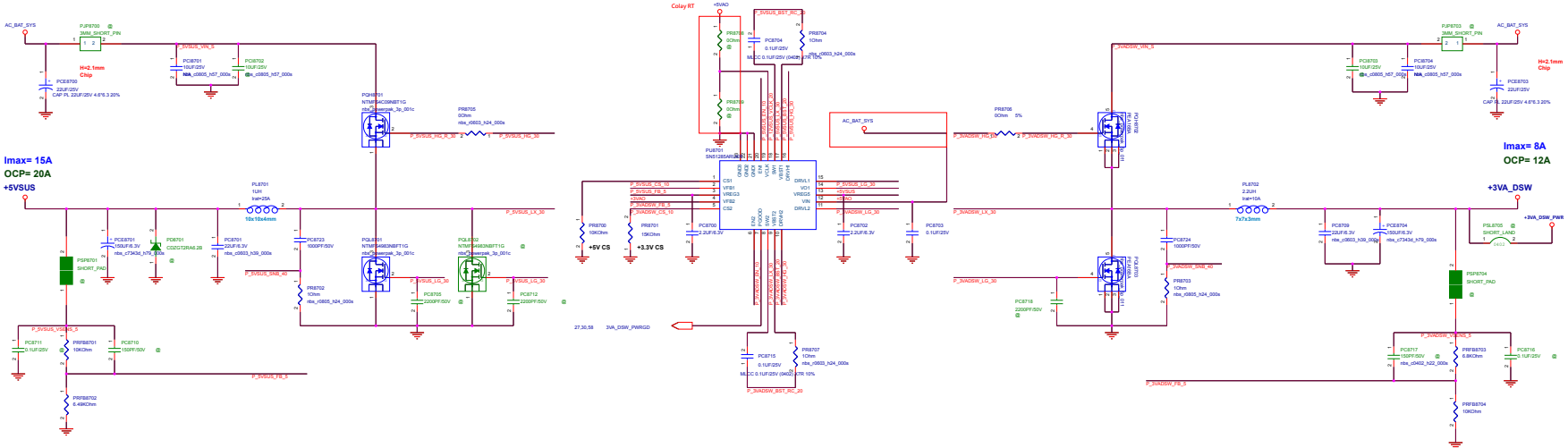
Rev: 31.0

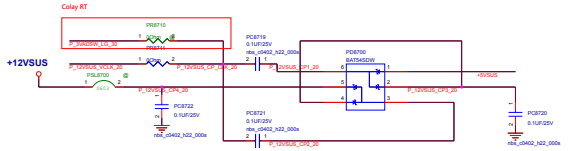
Title : PW_+1.2V/+VTT/+2.5V

Size: A2 | Dept.: NB Power team | Engineer: Power RD

Date: Friday, October 16, 2020 | Sheet 90 of 103

+3VA_DSW / +5VSUS [System Power]





請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm

Adaptor Mode (IMVP8)

	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	1	-	1
3VADSW_ON	1	-	1	-	1	-	1
3VSUS_ON	1	-	1	-	1	-	1
5VSUS_ON	1	-	1	-	1	-	1
1.35V_ON	1	-	1	-	0	-	0
SUSC_EC#	1	-	1	-	0	-	0
SUSB_EC#	1	-	0	-	0	-	0

Battery Mode (IMVP8)

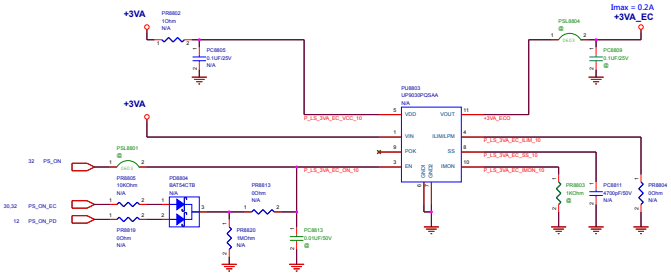
	S0	CS	S3	DS3	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0	1
3VADSW_ON	1	-	-	1	0	0	0
3VSUS_ON	1	-	-	0	0	0	0
5VSUS_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_EC#	1	-	-	0	0	0	0
SUSB_EC#	1	-	-	0	0	0	0

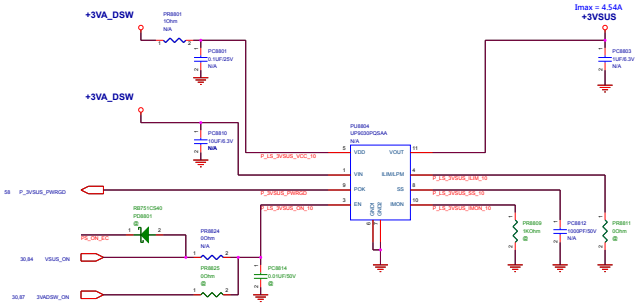
PT870* 請放置 PU8700旁;並請放置Trace 上!

<variant Name>

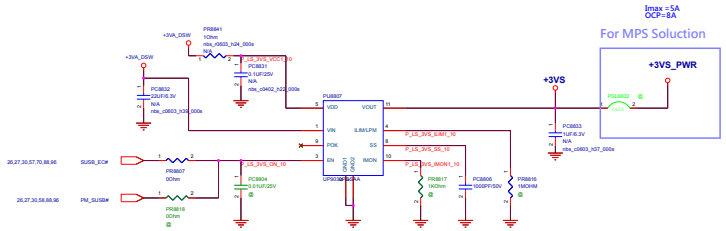
ASUS	Project Name: FX516	Rev: R1.0
Title : PW_+3VA_DSW/+5VSUS		
Size: A2	Dept.: NB Power team	Engineer: Matt
Date: Friday, October 16, 2020	Sheet: 87 of 103	

Load Switch

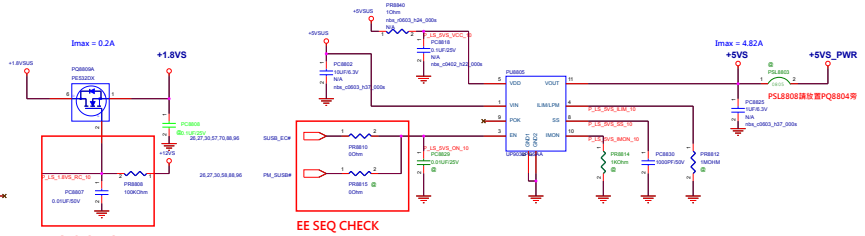




uP9030 ILIM/LPM Setting 對應表		
ILIM PIN	LPM (C10)	LIMIT Current
GND	Off	3A
1M to GND	Off	5A
Float/VDD	On	8A

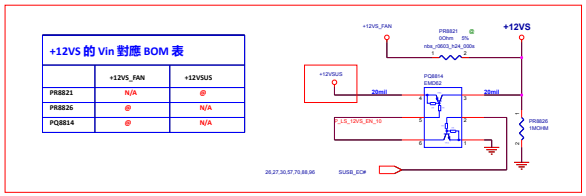


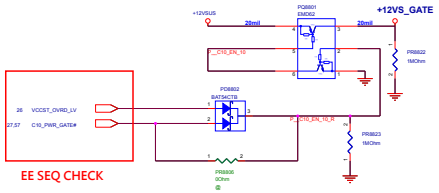
EE SEQ CHECK



EE SEQ CHECK

+12VS 的 Vin 對應 BOM 表		
	+12VS_FAN	+12VSUS
PR8821	N/A	@
PR8826	@	N/A
PQ8814	@	N/A





EE SEQ CHECK

BOM

ASUS	Project Name: FX516	Rev: REV.1
Title : PW_LOAD_SWITCH		
Size: A2	Dept.: NBI-RDSEE2	Engineer: Matt
Date: Friday, October 16, 2020	Sheet: 68 of 102	

Main Board

PRS8901	ADP<120W	ADP<230W	ADP>230W	ADP>330W
	TBD	5m	5m	2m
	N/A	10125-0108A320	10126-3202BE05	10126-3202BE05

PRS8903	ADP<120W	ADP<150W	ADP<180W	ADP<230W	ADP<240W	ADP<280W	ADP>330W
	200m	25m	X	X	330m	X	560m
	10114-0918B000	10114-0325100G	X	X	10421N3U31G16	X	10114-0D211G0R

AC_BAT_SYS

If you support Slow CHG, please select Green Box and check off-page net name with EE.

AD : 18V

I limit : Charge 6A
DisCharge 24A

BAT

HW_Throttle

AC limit = 100% ADP
Bat limit = byte 7 x 1.7

dGPU_PD# ---> GPIO12(EE page 75 or 78)

Plug HW Throttle(Out)

Plug HW Throttle(In)

AD : 17.5V
Place Close to PSR901

PTE901 讓就近 PU8900 與 溫讓就近Trace 上!

Adaptor select
total power = 90% ADP

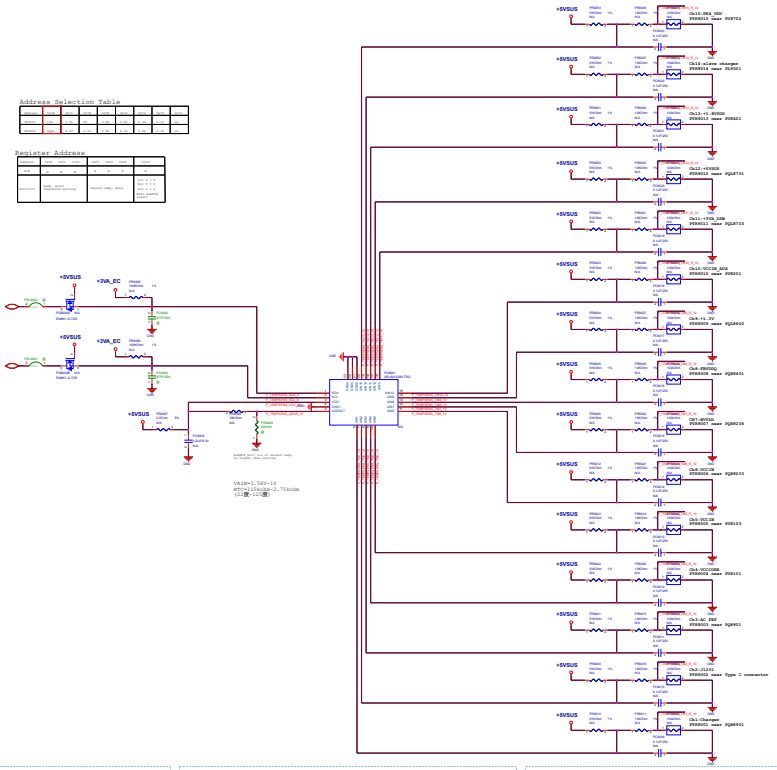
Adaptor select

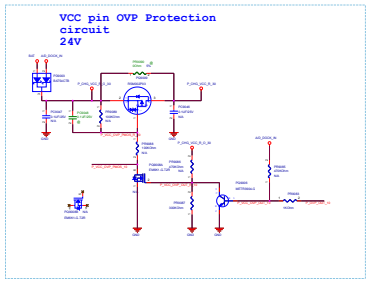
PRS8901	M Series	S Series
	10m	5m
PR8936		
1.6K	0.4V	45W	120W
31.6K	0.8V	150W	150W
54K	1.2V	180W	180W
93.1K	1.6V	65W	230W
130K	2.0V	NA	280W
270K	2.4V	90W	200W
540K	2.8V	120W	240W

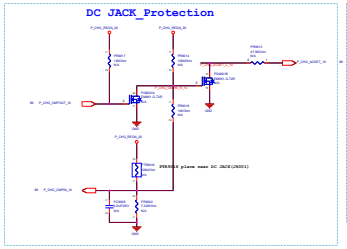
POP window

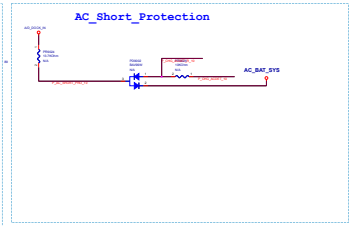
Project Name	FX516
Title :	PW_CHARGER
Dept.:	NB Power Team
Engineer:	Matt
Date: Friday, October 16, 2020	Sheet 38 of 100

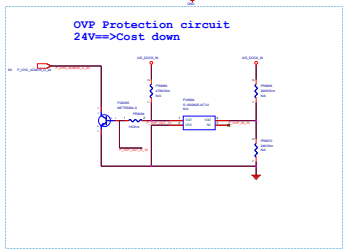
P90_PROTECTION

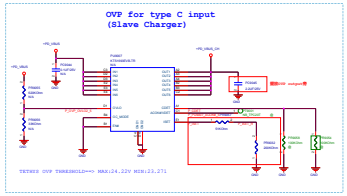




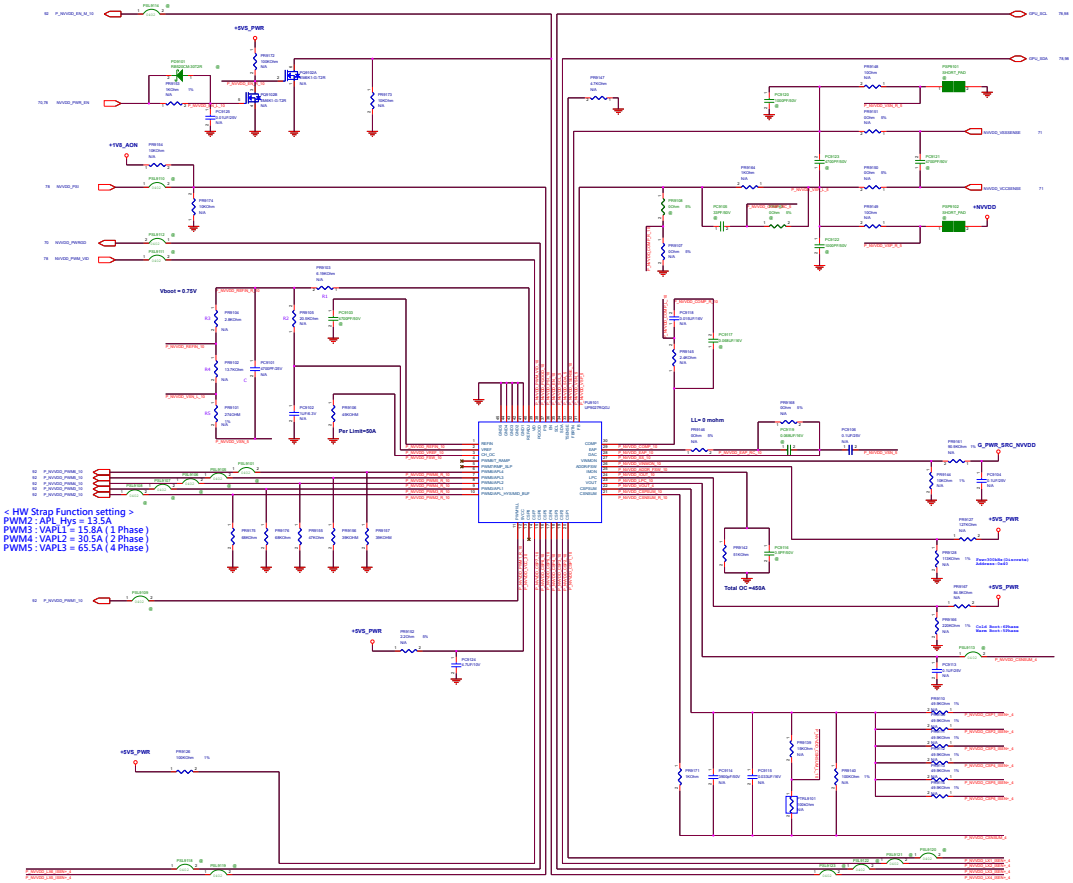




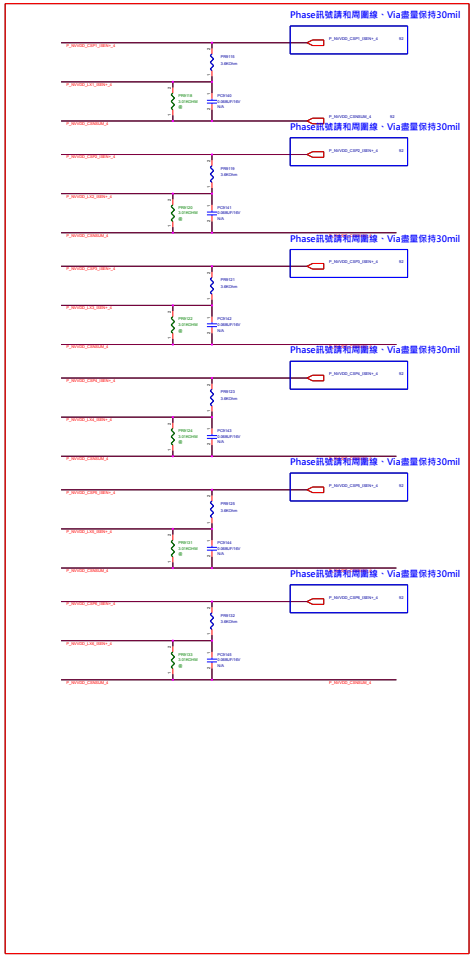




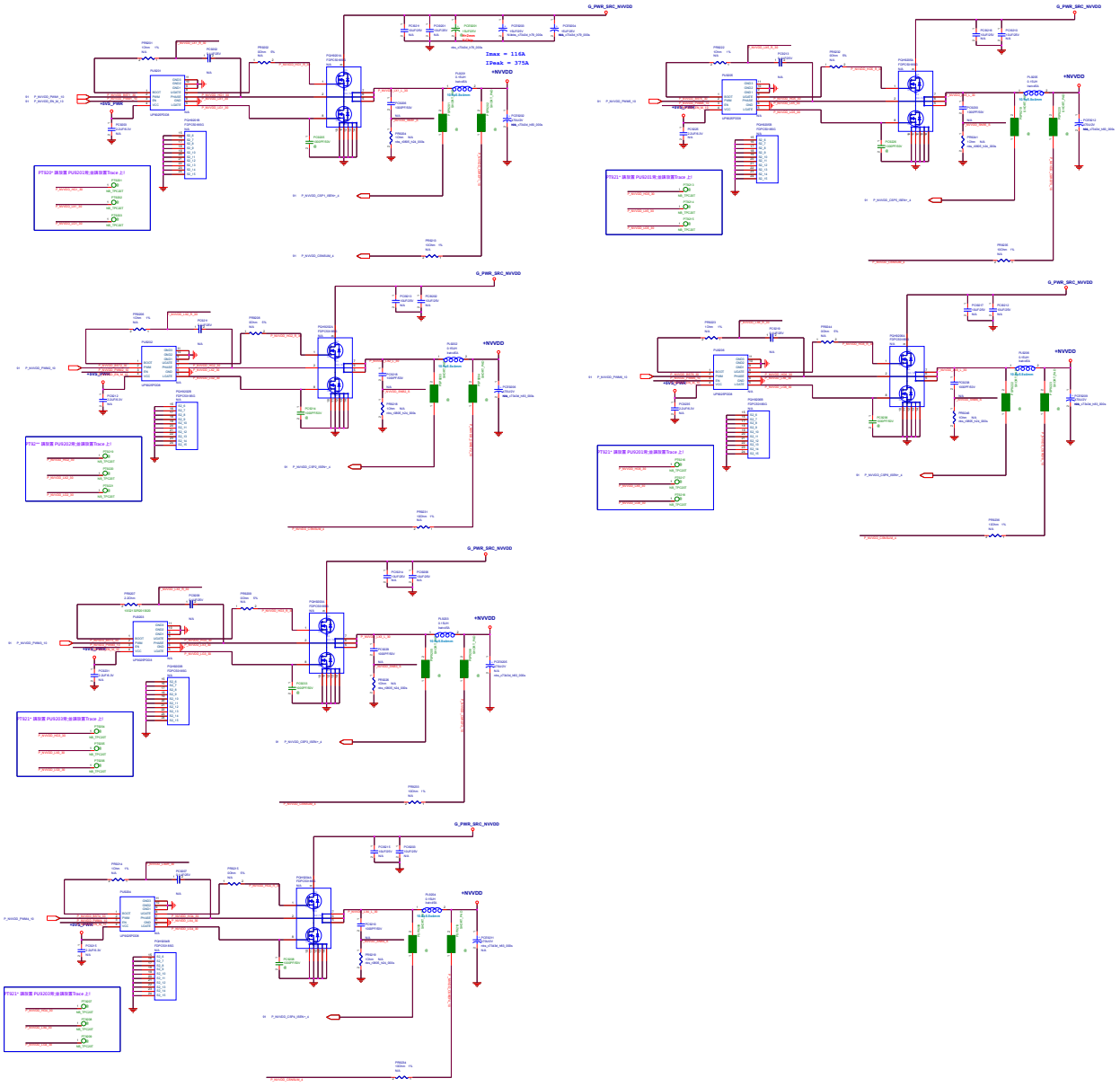
+NVVDD [For DGPU]



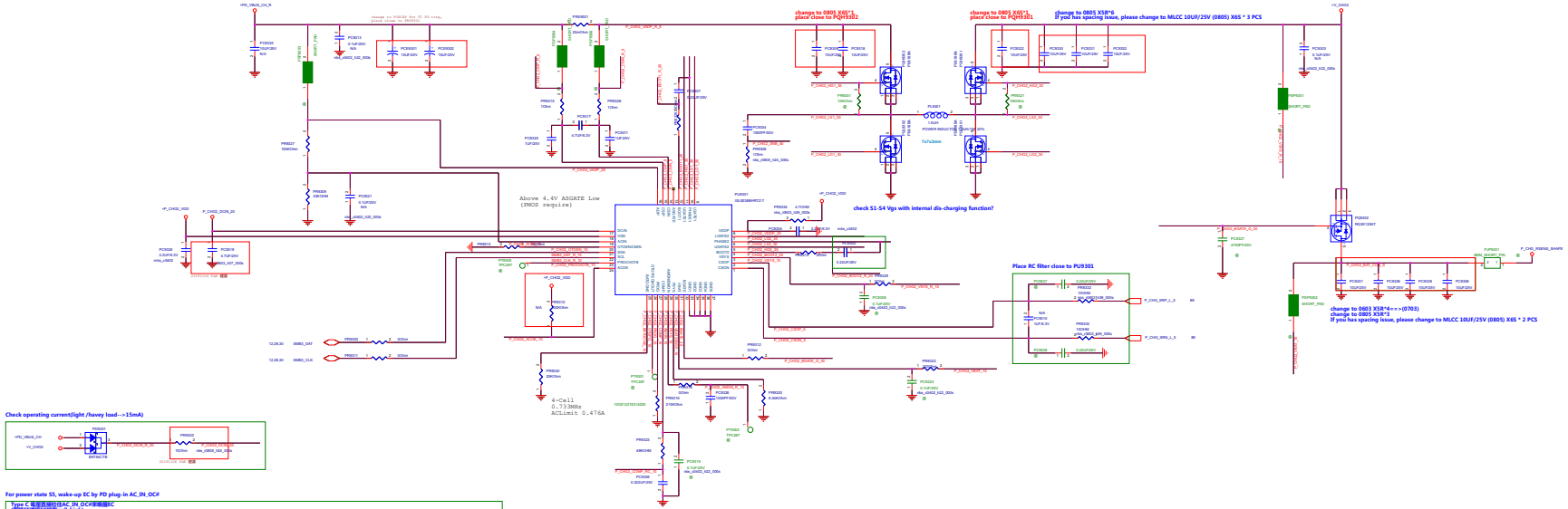
請放靠近PU9101



+NVVDD [For DGPU]



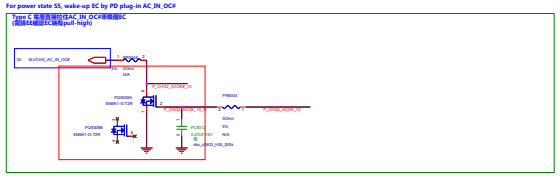
Charger ISL9238 (NVDC)



Check operating current(light /havey load-->15mA)

For power state S5, wake-up EC by PD plug-in AC_IN_OC#

Type C 電源具備PD且AC_IN_OC#準備就EC
(需接EC確認EC端是pull-high)



+FBVDDQ [For VRAM]

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.25V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	75KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.35V	1.2V
PR9404	10KOhm	
PR9409	21.5KOhm	
PR9423	53.6KOhm	

DVS Setting		
MEM_VDD_CTL	H	L
Voltage	1.25V	1.2V
PR9404	10KOhm	
PR9409	16.9KOhm	
PR9423	140KOhm	

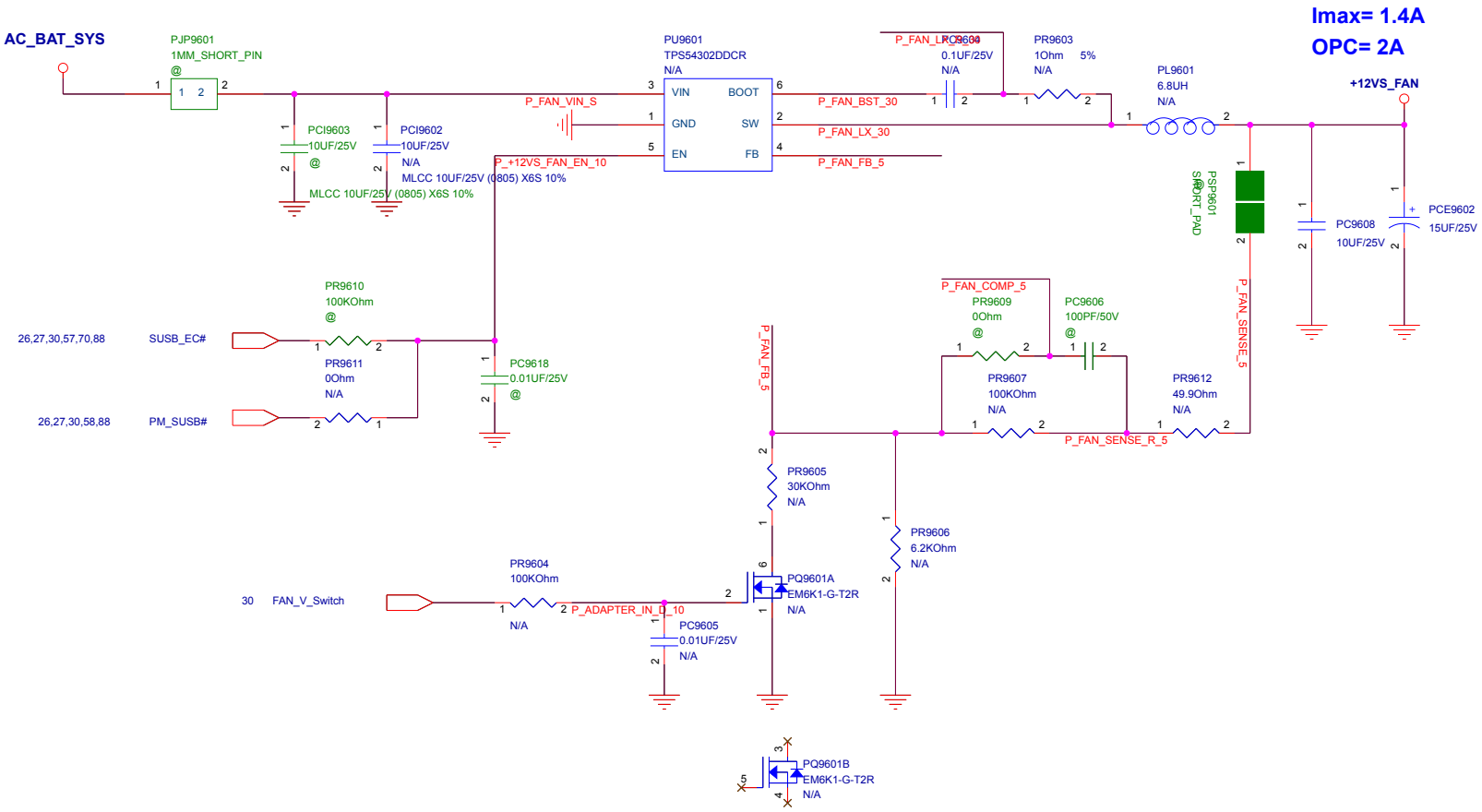
Fixed Vout		
@	PC9403/PR9423/PQ9401 PR9402/PR9414	
Voltage	1.25V	1.2V
PR9404	10KOhm	
PR9409	16.9KOhm	15.4KOhm

Vboot = ???V

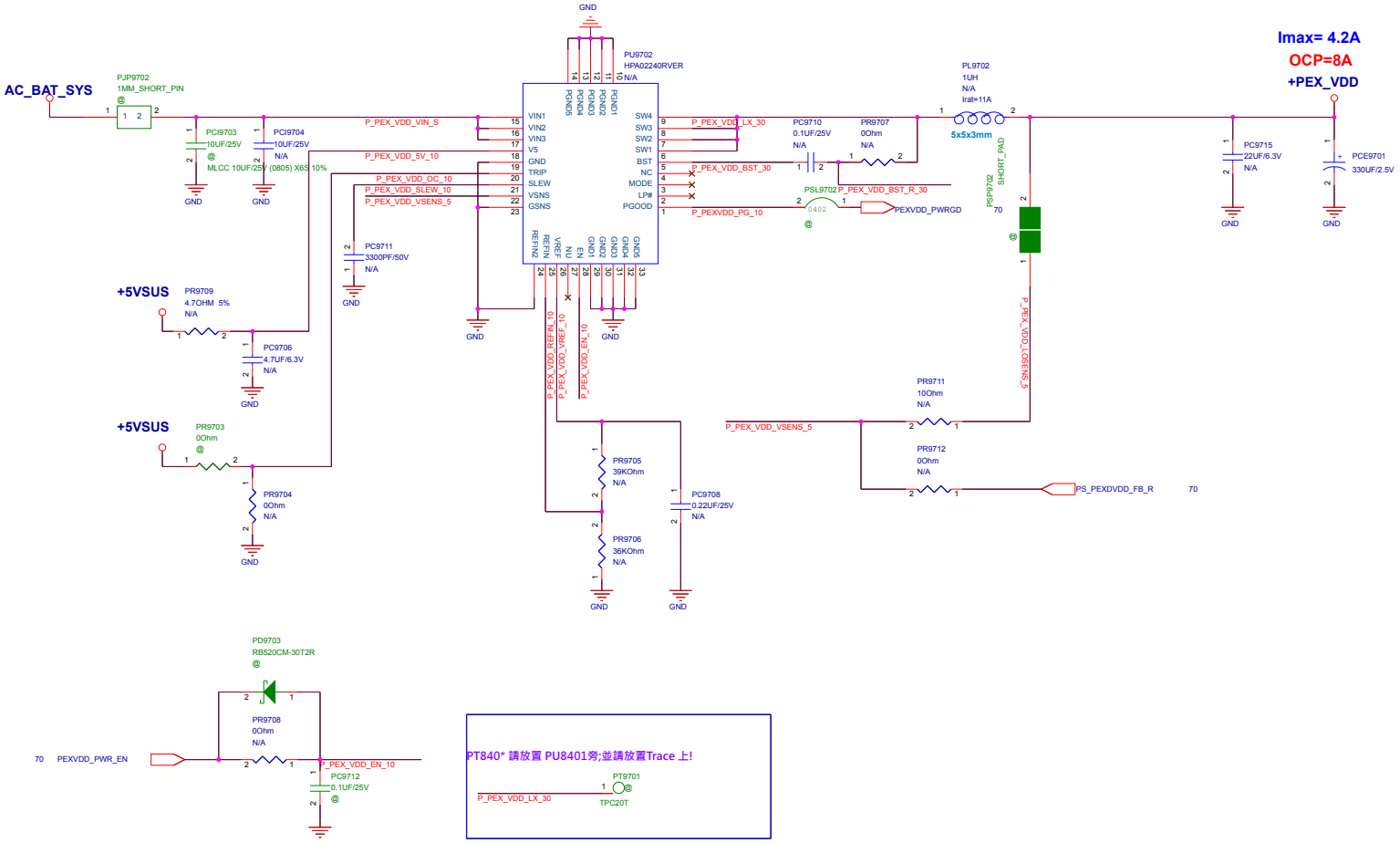
Imax= 32A
OCP= 70A

PT940* 請放置 PU9401旁;並請放置Trace 上!

+12VS_FAN [For FAN]

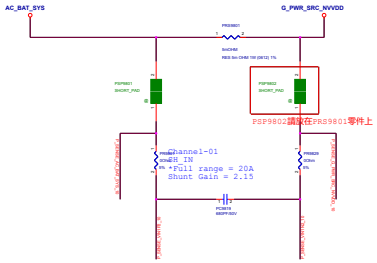


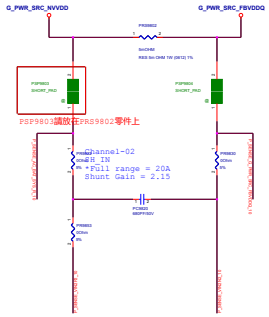
PEX_VDD [For GPU]

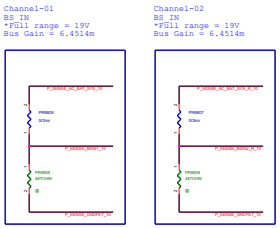


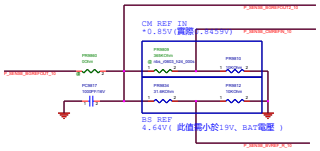
Project Name: Project Name		Rev: R1.0
Title : *****		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: Power RD	
Date: Friday, October 16, 2020	Sheet 97 of 103	

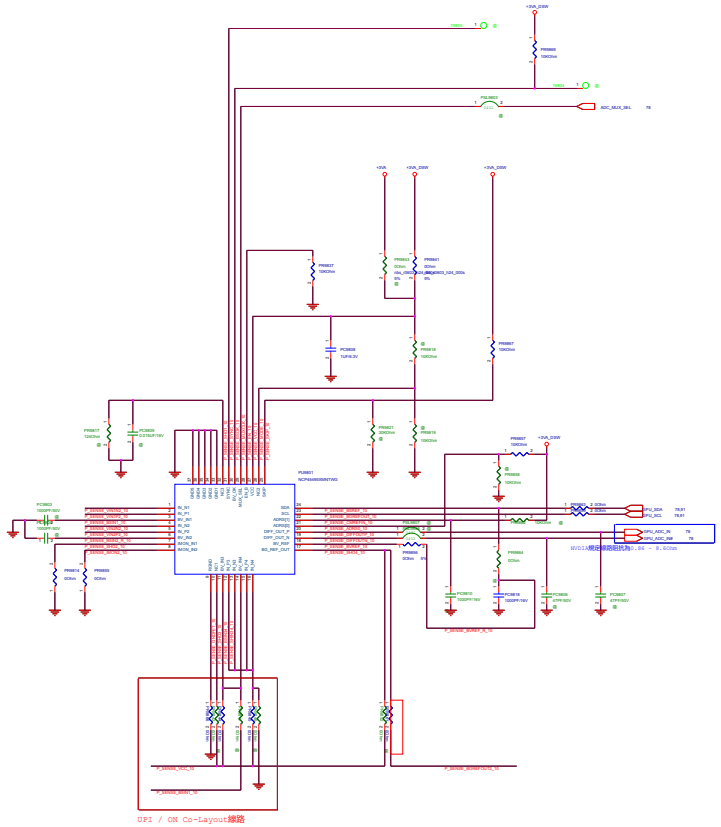
OVR-M GEN2 ONSEMI







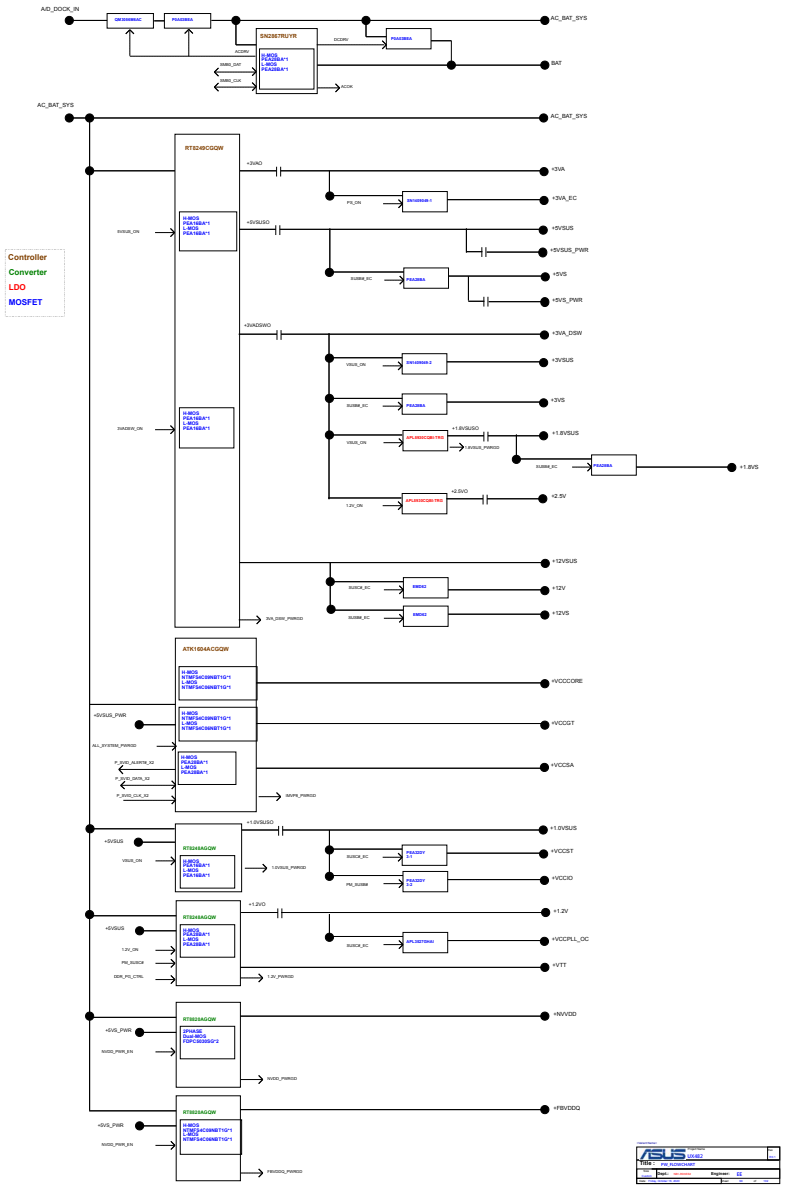




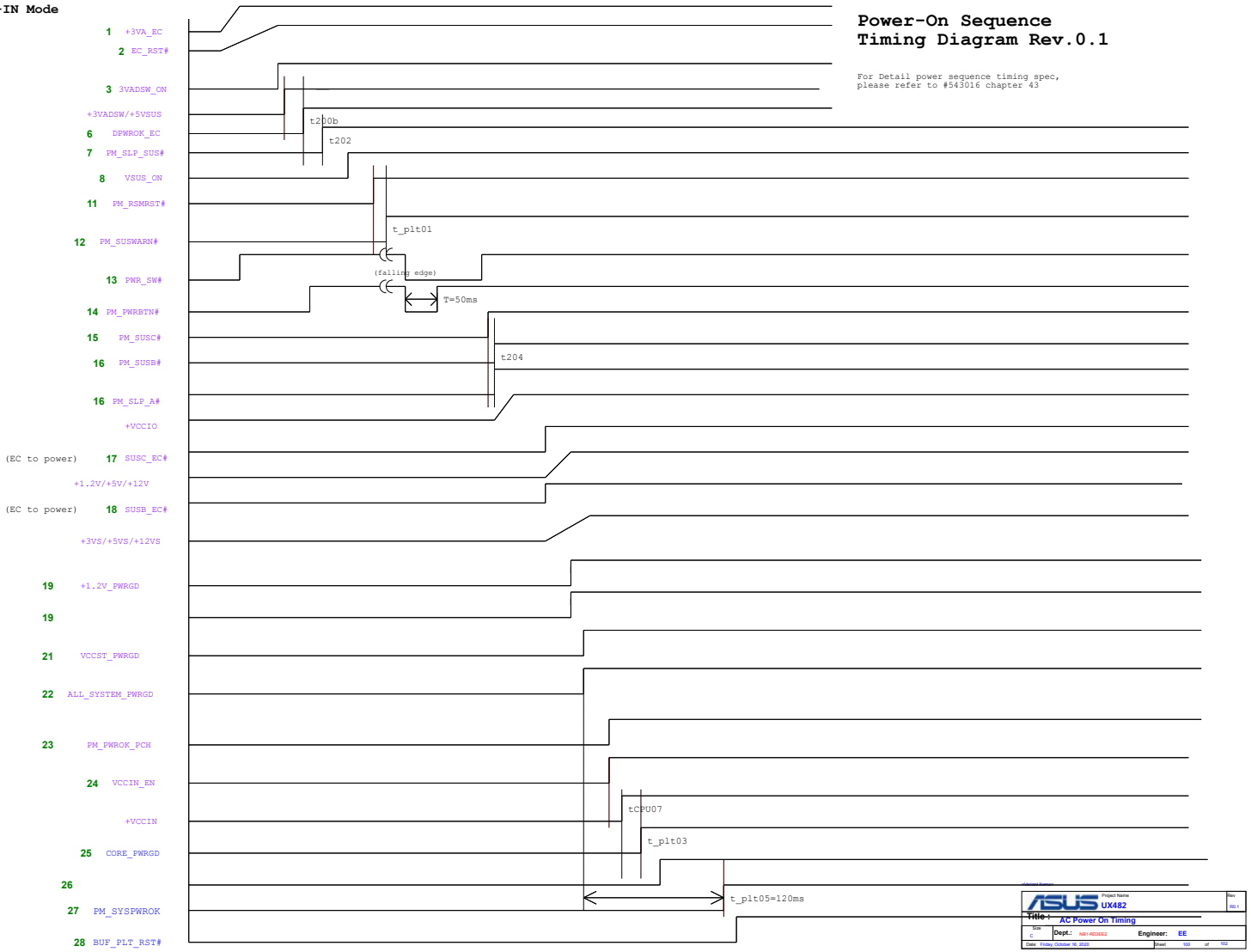
	PU9801	PR9805	PR9807	PC9803	PC9804	PC9805	PR9814	PR9855	PR9822
GN20	NCP45495XMNTWG 06129-00220000	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	@	@	0 Ohm 10G212000004030	0 Ohm 10G212000004030	0 Ohm 10G212000004030
N18P-G1	UP9026QQKI 06129-00110100	75KOhm 10G212750214010	75KOhm 10G212750214010	1000PF/50V 11G232110214321	1000PF/50V 11G232110214321	0.015UF/16V 11G232115311360	357Ohm 10G212357014010	@	49.9Ohm 10G21249R914010

	PC9810	PR9860	PR9809	PR9810	PR9834	PR9863	PR9859	PC9809	PR9808
GN20	@	@	@	10KOhm 10G212100214010	31.6KOhm 10G212316214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	@
N18P-G1	1000PF/16V 11G232110211030	0 Ohm 10G212000004030	360KOhm 10G212364004010	680KOhm 10G212680314010	324KOhm 10G212324314010	@	@	0.015UF/16V 11G232115311360	487Ohm 10G212487014010

	PR9806	PR9861	PR9864	PR9857	PR9801	PR9853	PR9817	PR9844/PR9845	PR9846/PR9847
GN20	@	0 Ohm 10G212000004030	@	10KOhm 10G212100214010	0 Ohm 10G212000004030	0 Ohm 10G212000004030	@	0 Ohm 10G212000004030	@
N18P-G1	487Ohm 10G212487014010	@	0Ohm 10G212000004030	@	100Ohm 10G212100014010	49.9Ohm 10G21249R914010	357Ohm 10G212357014010	@	0 Ohm 10G212000004030


AID_DOCK_IN
CM15059HAC
PSA2SB8A
SN28678UYR
AC_BAT_SYS
BAT
DCSRV
ACSRV
SMB_DAT
SMB_CLK
ACOK
PSA2SB8A
AC_BAT_SYS
RTS249GCGQW
+3VAO
+3VA
+3VA_EC
+5VSUSO
+5VSUS
+5VSUS_PWR
+5VS
+5VS_PWR
+3VADSWO
+3VA_DSW
+3VSUS
+3VS
+1.8VSUSO
+1.8VSUS
+1.8VS
+2.5VO
+2.5V
+12VSUS
+12V
+12VS
ATK1604ACGQW
+VCCCORE
+VCCGT
+VCCSA
+1.0VSUSO
+1.0VSUS
+VCCST
+VCCIO
RTS2548AGQW
+1.2VO
+1.2V
+VCCPLL_OC
+VTT
RTS8208AGQW
+NVVDD
RTS8208AGQW
+FBVDDQ
Controller
Converter
LDO
MOSFET

AC-IN Mode



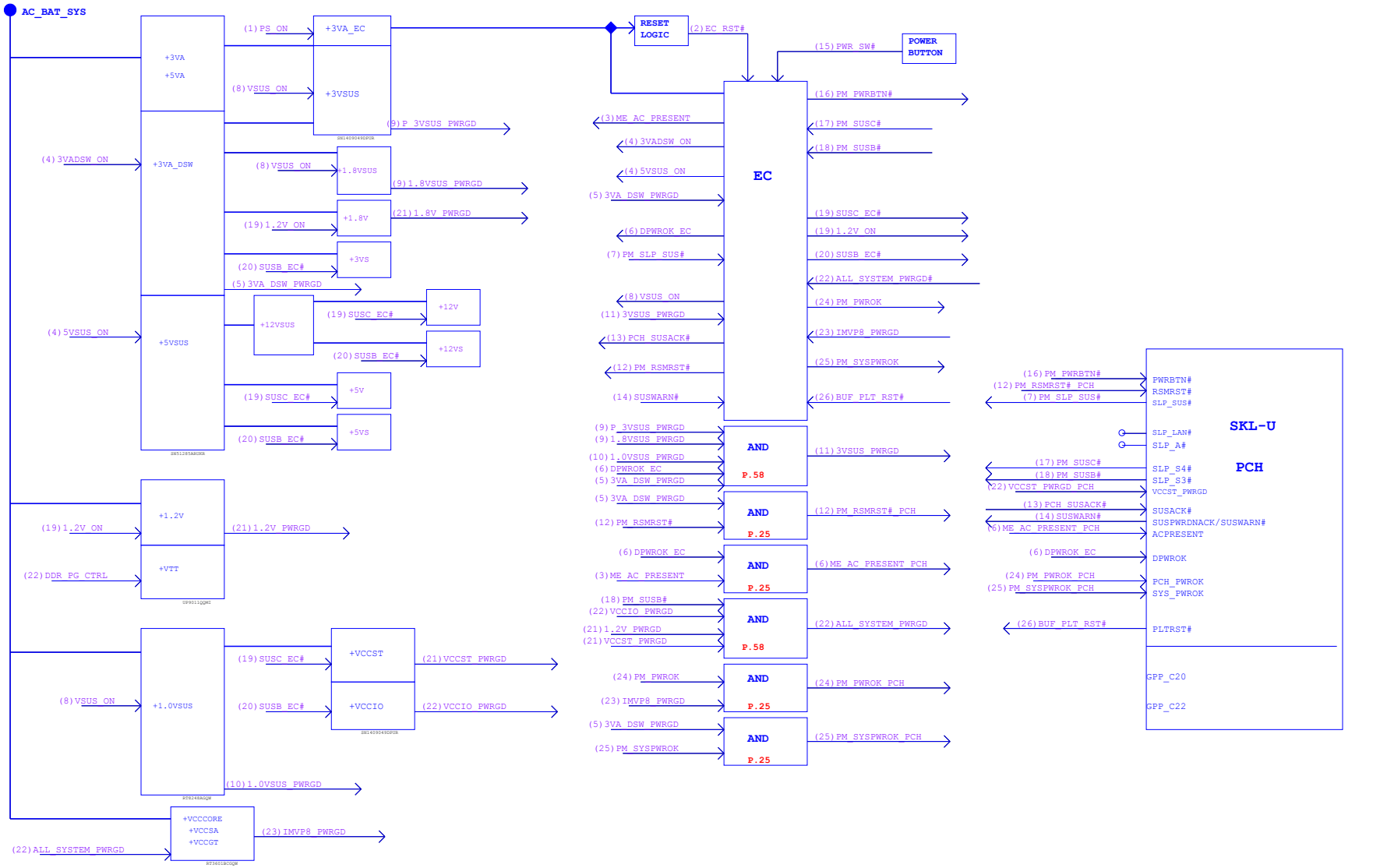
Power-On Sequence Timing Diagram Rev.0.1

For Detail power sequence timing spec, please refer to #543016 chapter 43

Project Name: UX482		Rev: R0.1
Title: AC Power On Timing		
Size: C	Dept.: NB1-RDSE2	Engineer: EE
Date: Friday, October 16, 2020	Sheet 100 of 102	

AC-IN Mode

Power On Sequence Diagram Rev.2.0



<Variant Name>

ASUS	Project Name: UX482	Rev: 152.1
Title :		
Size: A2	Dept.: NB1-RD3EE2	Engineer: EE
Date: Friday, October 16, 2020	Sheet 101 of 102	