DMS-SA30 *Rev.1.2*

Intel Skylake-S

CPU:

Intel SKL-S CPU (LGA1151)
Max. TDP: 35W

System Chipset:

Intel 100 series
Q170/H110

Main Memory:

DDR4-1866/2133 SO-DIMM x2 (1DPC, Max:32GB)

On Board Chip:

HDMI to LVDS - TSUMU58DC2-1
DP to VGA - CH7517A
Super I/O - NCT6106D
Audio - Realtek Codec ALC898 + Amplifier TPA2008D2
LAN - Intel Jacksonville i219LM(Q170) / V(H110)
BIOS - SPI Flash ROM 128MB(Q170) / 64MB(H110)
TPM 2.0/1.2 - SLB9665/9660 (Q170 Sku)
GL850G - USB2.0 HUB (H110 Sku)

VRM Controller:

IMVP8-ISL95855(VCCP/VCCGT/VCCSA)
ISL8016(VCCIO)
NCP1589L(VCC_DDR) + UP1727(VPP_DDR)
NCP1589L(PCH_1VSB)
NCP1589A(+12VSB)
TPS40210DGQ(+24VSB)
TPS51125RGER(SYS_PWR)

Expansion Slots:

SATA Riser Connector (2* SATA ports)
Mini-PCIE *2
Expension Board (RS232*2, USB*1 ...)

Others :

Cash Drawer
Power USB

How to distinguish different Sku

BLUE Color for all models
Orange Color for Q170 SKU
Purple Color for H110 SKU

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Title: Cover page		
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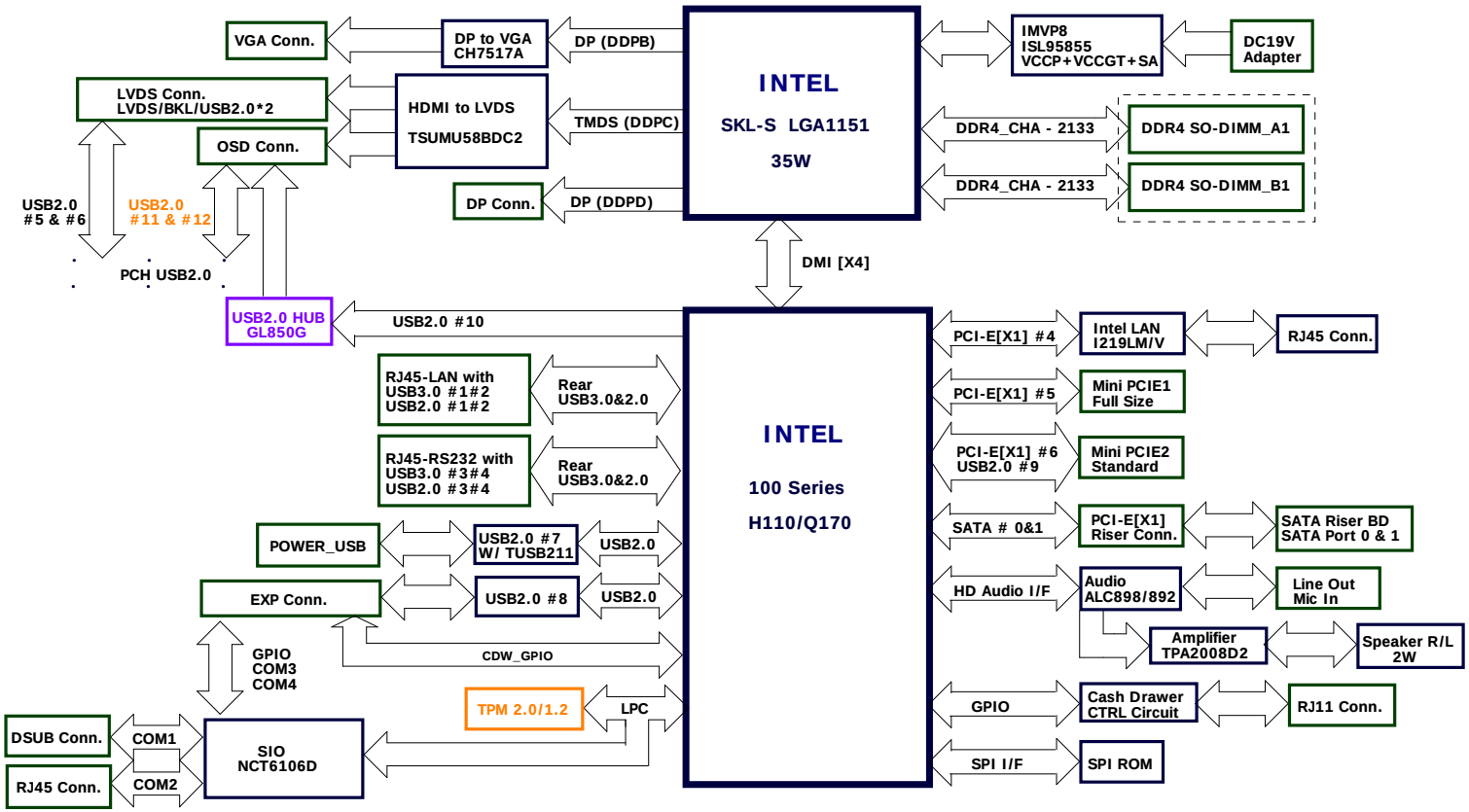
Block Diagram



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Title: Block Diagram		
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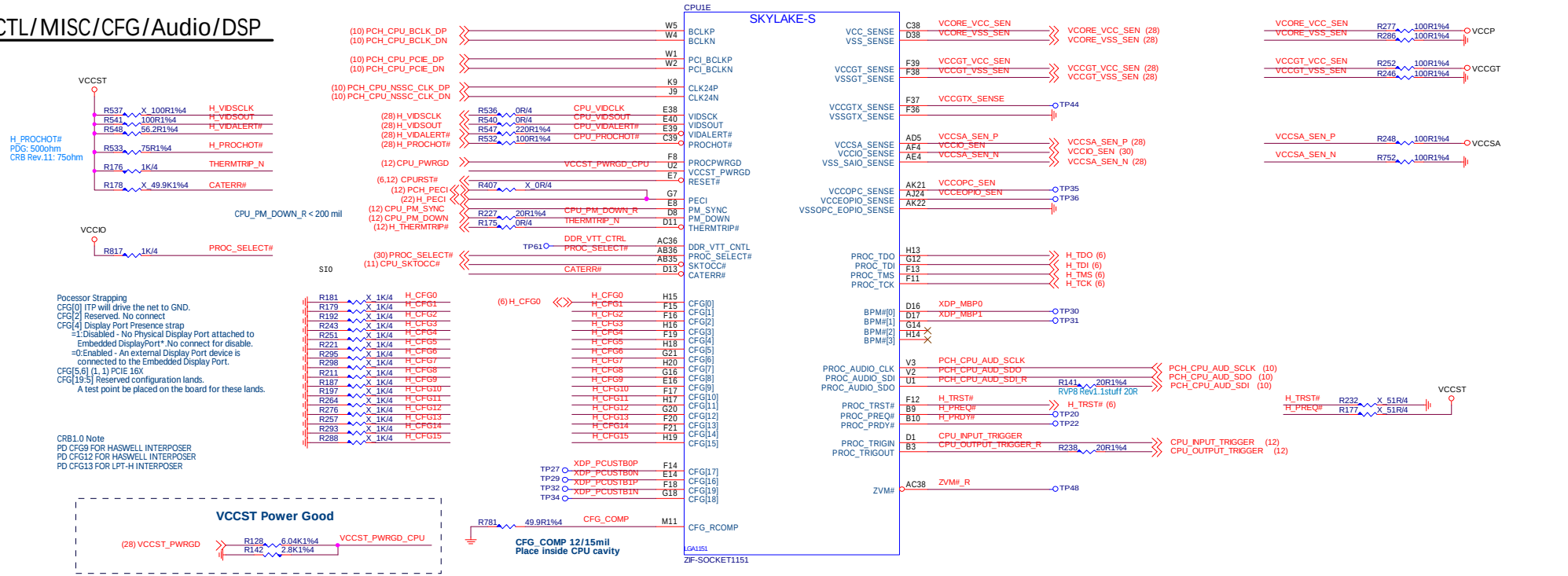
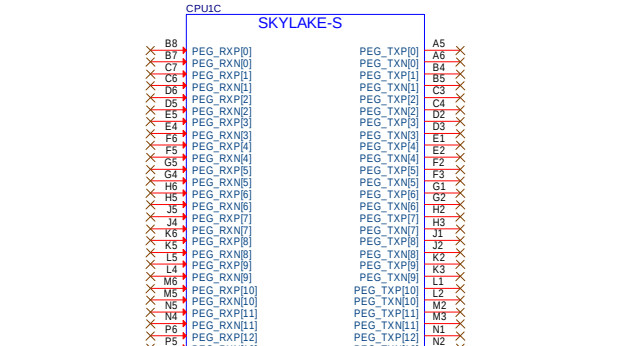
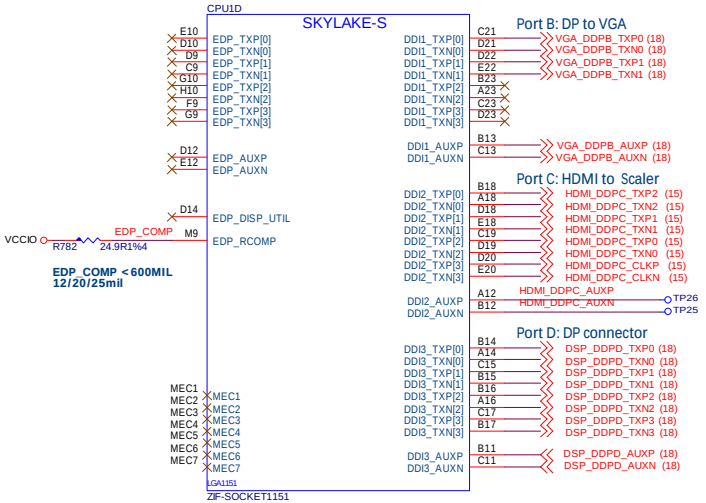
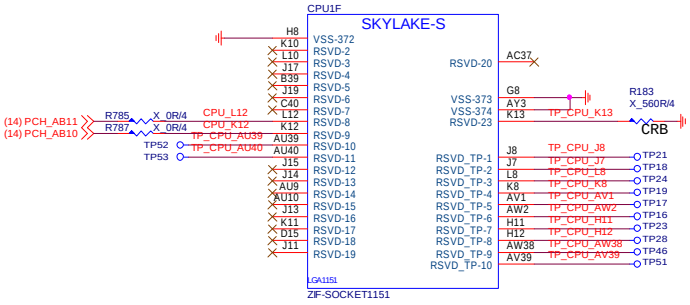
CPU-CTL/MISC/CFG/Audio/DSP









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Title	CPU-CTL/MISC/CFG/Audio/DSP		
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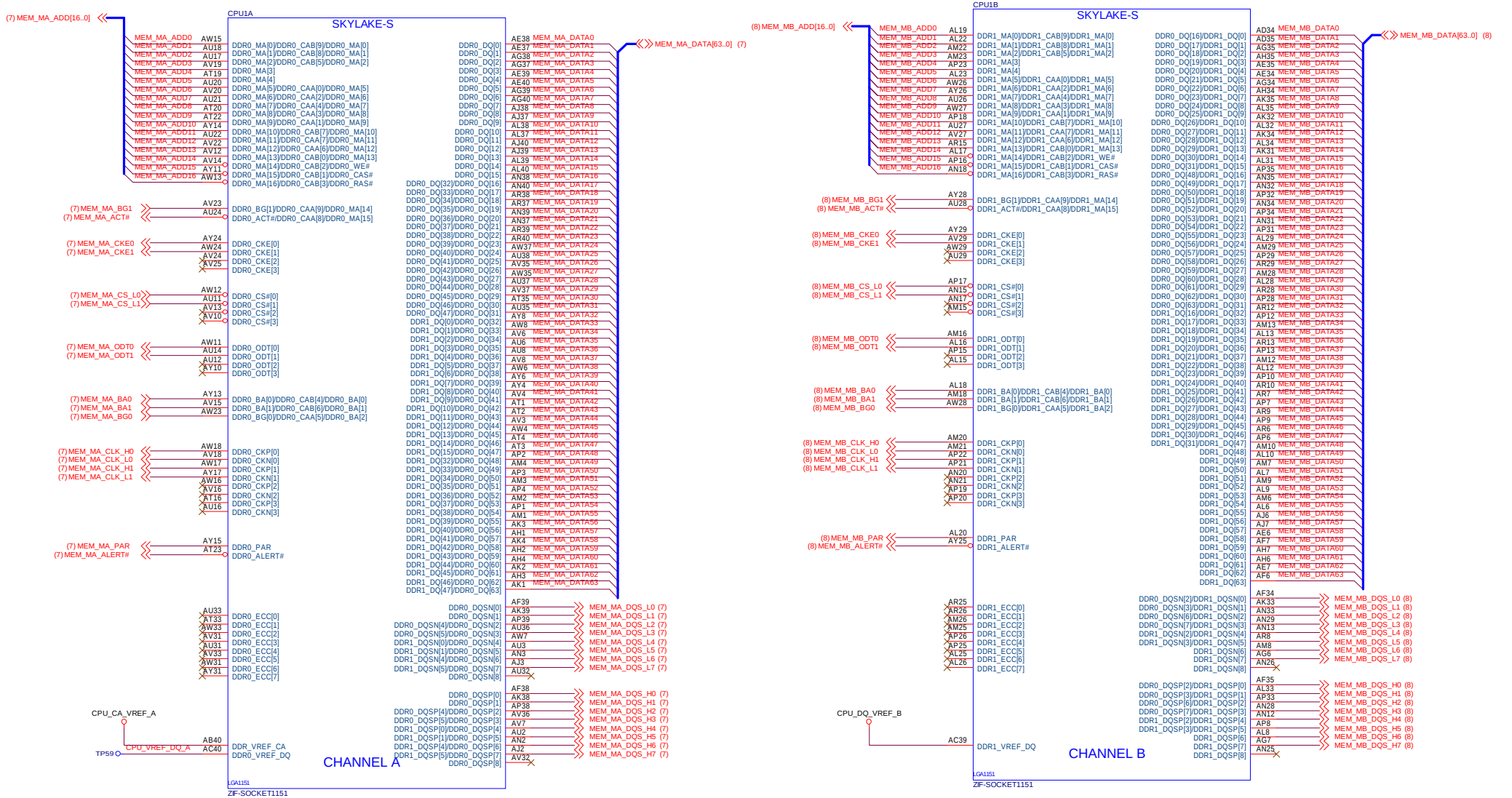
CPU-Memory



SOCKET PN N12-151A010-L06

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Title: CPU-Memory			
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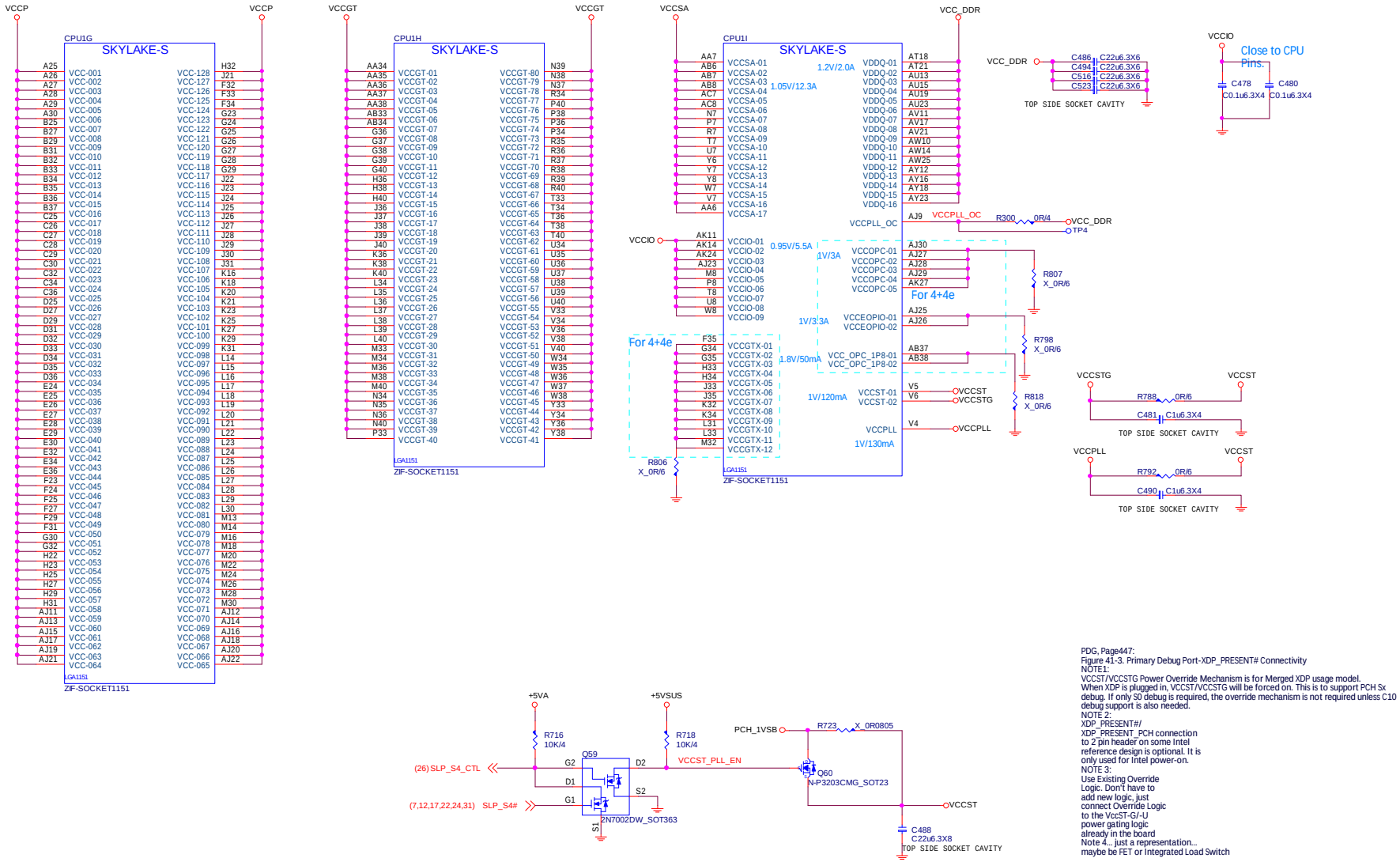
CPU-Power



PDG, Page447:
Figure 41-3. Primary Debug Port-XDP_PRESENT# Connectivity
NOTE1:
VCCST/VCCSTG Power Override Mechanism is for Merged XDP usage model.
When XDP is plugged in, VCCST/VCCSTG will be forced on. This is to support PCH Sx debug. If only S0 debug is required, the override mechanism is not required unless C10 debug support is also needed.
NOTE 2:
XDP_PRESENT#/
XDP_PRESENT_PCH connection to 2 pin header on some Intel reference design is optional. It is only used for Intel power-on.
NOTE 3:
Use Existing Override Logic. Don't have to add new logic, just connect Override Logic to the VccST-G/-U power gating logic already in the board
Note 4... just a representation... maybe be FET or Integrated Load Switch

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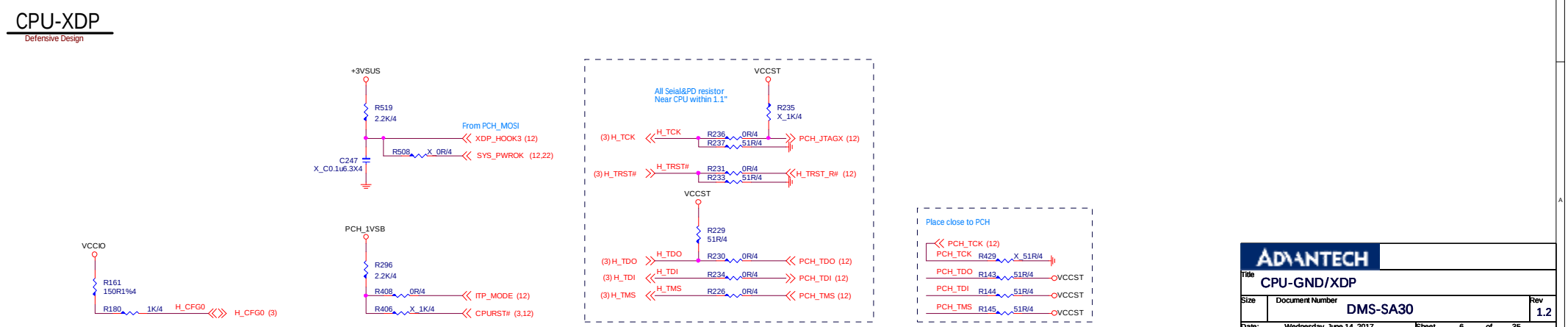

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Title	CPU-GND/XDP	
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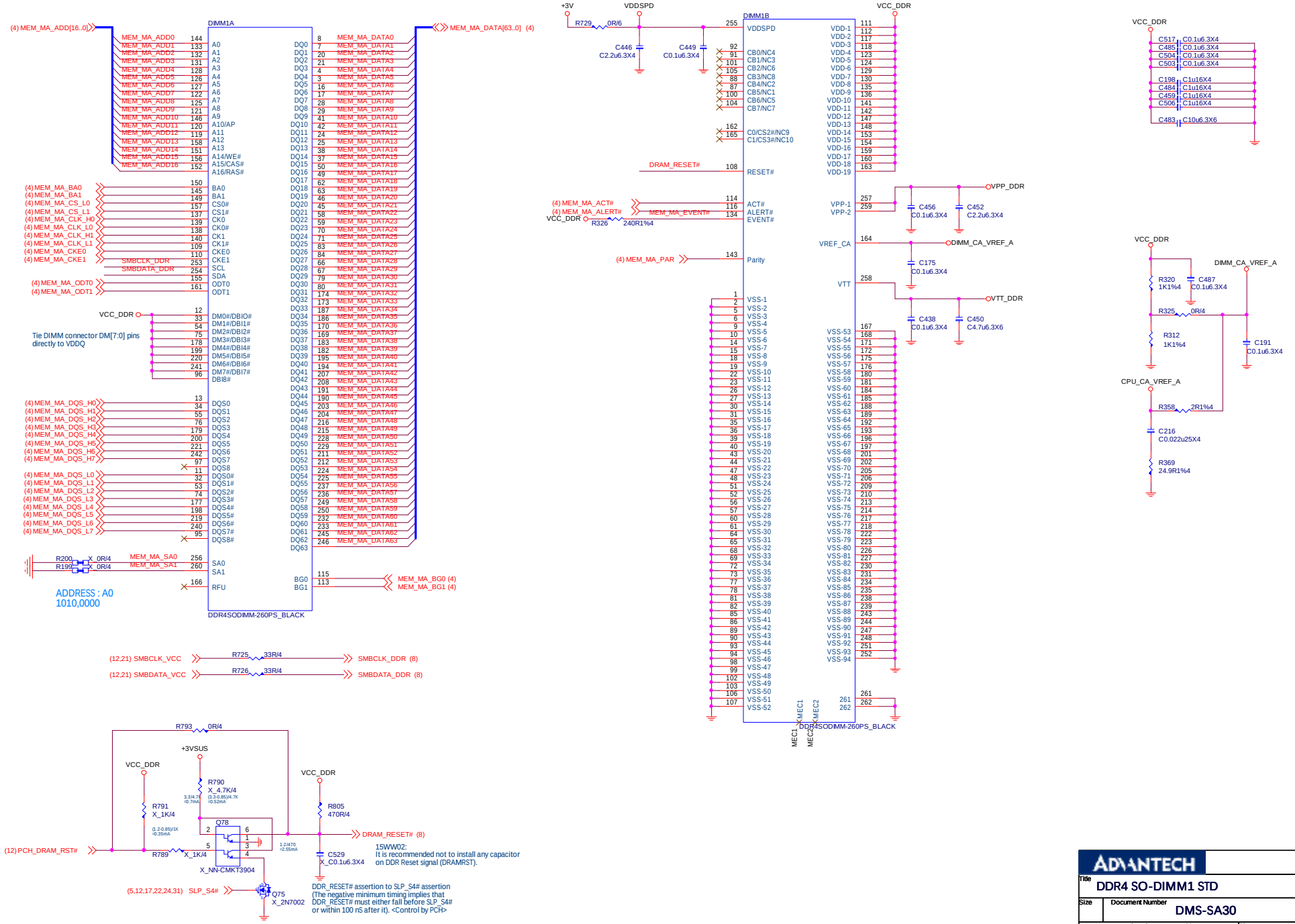
DDR4 SO-DIMM DIMM1

Channel A (W/O ECC)



Title	DDR4 SO-DIMM1 STD		
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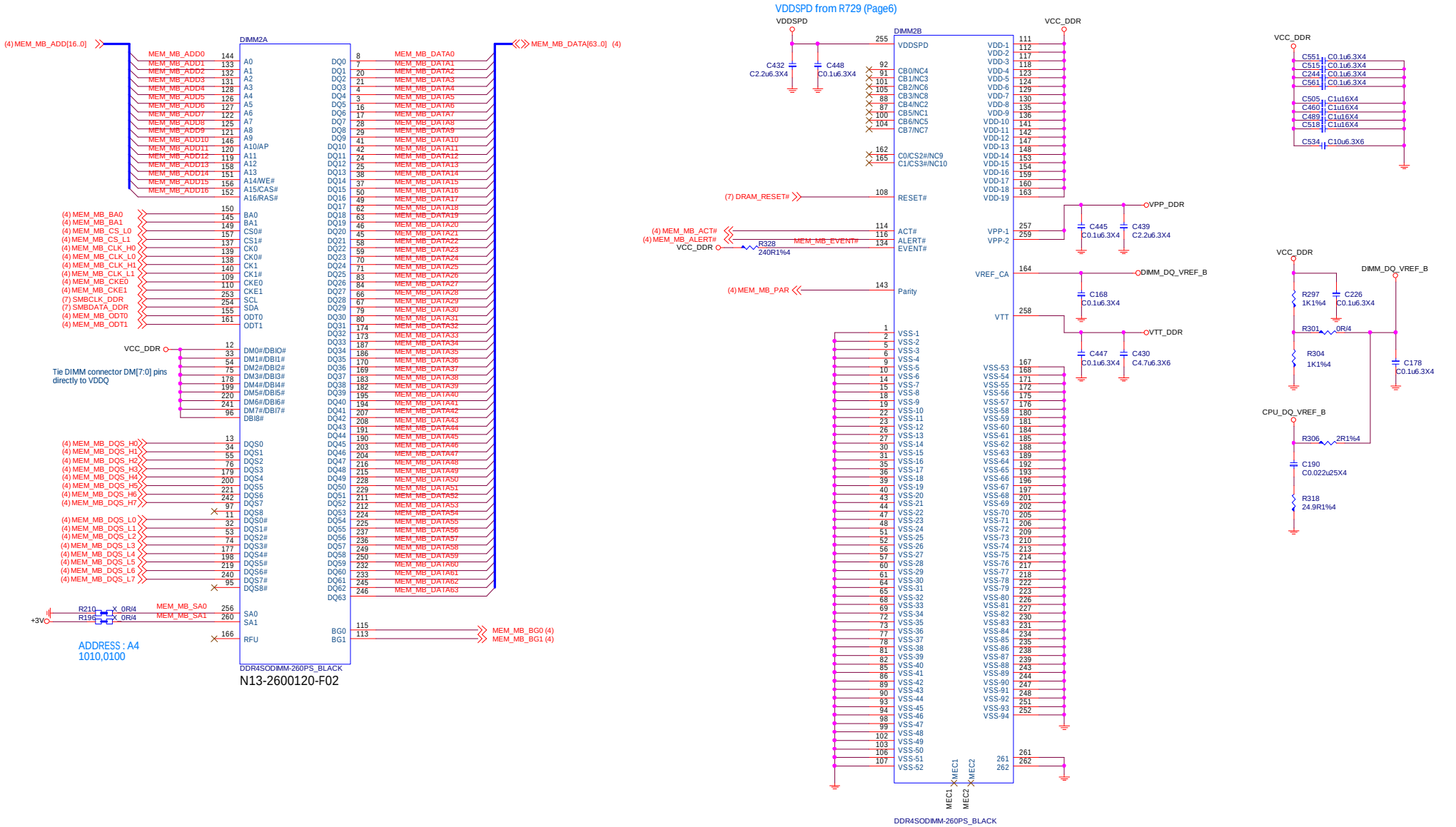
DDR4 SO-DIMM DIMM2

Channel B (W/O ECC)



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Title	DDR4 SO-DIMM2 STD	
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PCH-USB/PCIE/DMI/SATA

USB1~2 for Rear USB3.0(LAN_USB1)
USB3~4 for Rear USB3.0(COM_USB1)

PCH1A

SPT-H_PCH

(19) USB3_TX1P
(19) USB3_TX1N
(19) USB3_TX2P
(19) USB3_TX2N
(23) USB3_TX3P
(23) USB3_TX3N
(23) USB3_TX4P
(23) USB3_TX4N

B11 USB3_1_TXP
C11 USB3_1_TXN
A12 USB3_2_TXP/SSIC_1_TXP
B12 USB3_2_TXN/SSIC_1_TXN
D13 USB3_3_TXP/SSIC_2_TXP
C13 USB3_3_TXN/SSIC_2_TXN
B13 USB3_4_TXP
A14 USB3_4_TXN
C14 USB3_5_TXP
B14 USB3_5_TXN
C15 USB3_6_TXP
B15 USB3_6_TXN

The xHCI controller provides a USB 3.0 debug port capability on all SuperSpeed ports.

(19) USB3_RX1P
(19) USB3_RX1N
(19) USB3_RX2P
(19) USB3_RX2N
(23) USB3_RX3P
(23) USB3_RX3N
(23) USB3_RX4P
(23) USB3_RX4N

A7 USB3_1_RXP
B7 USB3_1_RXN
B8 USB3_2_RXP/SSIC_1_RXP
C8 USB3_2_RXN/SSIC_1_RXN
A9 USB3_3_RXP/SSIC_2_RXP
B10 USB3_3_RXN/SSIC_2_RXN
G11 USB3_4_RXP
E11 USB3_4_RXN
H13 USB3_5_RXP
G13 USB3_5_RXN
K13 USB3_6_RXP
K15 USB3_6_RXN

USB 3.0

USB5~9 & PCI-E1~3
No functtion for H110

USB 2.0

USB11~16 :
No function for H110

AG7 USB2P_1
AF5 USB2N_1
AD7 USB2P_2
AD5 USB2N_2
AG10 USB2P_3
AG8 USB2N_3
AE2 USB2P_4
AE1 USB2N_4
AC3 USB2P_5
AC2 USB2N_5
AF3 USB2P_6
AF2 USB2N_6
AB2 USB2P_7
AB3 USB2N_7
AL7 USB2P_8
AL8 USB2N_8
AA2 USB2P_9
AA1 USB2N_9
AJ7 USB2P_10
AJ8 USB2N_10
W3 USB2P_11
W2 USB2N_11
AD2 USB2P_12
AD3 USB2N_12
V1 USB2P_13
V2 USB2N_13
AJ13 USB2P_14
AJ11 USB2N_14

USB1+ (19) — USB1~2 for Rear USB3.0(LAN_USB1) (OC#0)
USB1- (19)
USB2+ (19)
USB2- (19) — USB3~4 for Rear USB3.0(COM_USB1) (OC#1)
USB3+ (23)
USB3- (23)
USB4+ (23)
USB4- (23)
USB5+ (16) — USB5~6 for LVDS Conn. (OC#2)
USB5- (16)
USB6+ (16)
USB6- (16) — USB7 for PUSB (OC#3)
USB7+ (24)
USB7- (24) — USB8 for EXP. BD. (OC#4)
USB8+ (23)
USB8- (23) — USB9 for Mini PCI-E2
USB9+ (21)
USB9- (21) — USB10 for GL-850G USB2.0 HUB
USB10+ (17)
USB10- (17) — USB11~12 for OSD BD (Normal_PWR) (OC#6)
USB11+ (17)
USB11- (17) — USB13~14 for OSD BD (BIOS_PWR) (OC#7)
USB12+ (17)
USB12- (17)
USB13+ (17)
USB13- (17)
USB14+ (17)
USB14- (17)

USB2_COMP<500mil

AG3 USB2_COMP — R386 113R1%4
AD10 USB2_VBUSSENSE — R375 1K/4
AG2 USB2_ID — R385 1K/4

USB2_COMP
USB2_VBUSSENSE
USB2_ID

PCIe/USB 3

(19) PE4_LAN_TXP
(19) PE4_LAN_TXN

G15 PCIE1_TXP/USB3_7_TXP
H15 PCIE1_TXN/USB3_7_TXN
G17 PCIE2_TXP/USB3_8_TXP
E17 PCIE2_TXN/USB3_8_TXN
K17 PCIE3_TXP/USB3_9_TXP
L17 PCIE3_TXN/USB3_9_TXN
G19 PCIE4_TXP/USB3_10_TXP
E20 PCIE4_TXN/USB3_10_TXN

(19) PE4_LAN_RXP
(19) PE4_LAN_RXN

B16 PCIE1_RXP/USB3_7_RXP
A16 PCIE1_RXN/USB3_7_RXN
C19 PCIE2_RXP/USB3_8_RXP
B19 PCIE2_RXN/USB3_8_RXN
C20 PCIE3_RXP/USB3_9_RXP
B20 PCIE3_RXN/USB3_9_RXN
A21 PCIE4_RXP/USB3_10_RXP
B21 PCIE4_RXN/USB3_10_RXN

PCIe

(21) PE5_PCIE_TXP
(21) PE5_PCIE_TXN
(21) PE6_PCIE_TXP
(21) PE6_PCIE_TXN

C22 PCIE5_TXP
D22 PCIE5_TXN
A23 PCIE6_TXP
B22 PCIE6_TXN
B23 PCIE7_TXP
C23 PCIE7_TXN
B24 PCIE8_TXP
C24 PCIE8_TXN

(21) PE5_PCIE_RXP
(21) PE5_PCIE_RXN
(21) PE6_PCIE_RXP
(21) PE6_PCIE_RXN

L19 PCIE5_RXP
K19 PCIE5_RXN
E22 PCIE6_RXP
G22 PCIE6_RXN
K22 PCIE7_RXP
L22 PCIE7_RXN
L24 PCIE8_RXP
K24 PCIE8_RXN

DMI

B27 DMI_RXP0
C27 DMI_RXN0
A28 DMI_RXP1
B28 DMI_RXN1
C29 DMI_RXP2
B29 DMI_RXN2
A30 DMI_RXP3
B30 DMI_RXN3

DMI_TXP0 — DMI_RXP0 (3)
DMI_TXN0 — DMI_RXN0 (3)
DMI_TXP1 — DMI_RXP1 (3)
DMI_TXN1 — DMI_RXN1 (3)
DMI_TXP2 — DMI_RXP2 (3)
DMI_TXN2 — DMI_RXN2 (3)
DMI_TXP3 — DMI_RXP3 (3)
DMI_TXN3 — DMI_RXN3 (3)

N27 DMI_TXP0
L27 DMI_TXN0
G24 DMI_TXP1
E24 DMI_TXN1
E26 DMI_TXP2
G27 DMI_TXN2
K29 DMI_TXP3
L29 DMI_TXN3

DMI_RXP0 — DMI_TXP0 (3)
DMI_RXN0 — DMI_TXN0 (3)
DMI_RXP1 — DMI_TXP1 (3)
DMI_RXN1 — DMI_TXN1 (3)
DMI_RXP2 — DMI_TXP2 (3)
DMI_RXN2 — DMI_TXN2 (3)
DMI_RXP3 — DMI_TXP3 (3)
DMI_RXN3 — DMI_TXN3 (3)

PCIECOMP_P — C17
PCIECOMP_N — B18
R314 100R1%4

PCIE_RCOMPP
PCIE_RCOMPN

PCIE_RCOMP 12/15mil
RCOMPP&RCOMPN
Miss-match<1%

1 OF 12

SPT-H

Lane11 of H110 is N/A and lane 12 only can be used for LAN only.

PCH1B

SPT-H_PCH

B31 PCIE9_TXP/SATA0A_TXP
C31 PCIE9_TXN/SATA0A_TXN
B32 PCIE10_TXP/SATA1A_TXP
C32 PCIE10_TXN/SATA1A_TXN
B33 PCIE11_TXP
C33 PCIE11_TXN
A35 PCIE12_TXP
B35 PCIE12_TXN

PCIE9_RXP/SATA0A_RXP — H31
PCIE9_RXN/SATA0A_RXN — G31
PCIE10_RXP/SATA1A_RXP — E29
PCIE10_RXN/SATA1A_RXN — G29
PCIE11_RXP — K31
PCIE11_RXN — L31
PCIE12_RXP — H33
PCIE12_RXN — G33

Sku15&16 only support PCIe/GbE for H110

SATA Port 0/1 can be configured to PCIe Ports 9/10 or 13/14

SATA0B_TXP
SATA0B_TXN
SATA1B_TXP
SATA1B_TXN

B36 PCIE13_TXP/SATA0B_TXP
C36 PCIE13_TXN/SATA0B_TXN
C38 PCIE14_TXP/SATA1B_TXP
B38 PCIE14_TXN/SATA1B_TXN
A39 PCIE15_TXP/SATA2_TXP
B39 PCIE15_TXN/SATA2_TXN
A40 PCIE16_TXP/SATA3_TXP
A41 PCIE16_TXN/SATA3_TXN

PCIe/SATA

PCIE13_RXP/SATA0B_RXP — E35 — SATA0B_RXP
PCIE13_RXN/SATA0B_RXN — G35 — SATA0B_RXN
PCIE14_RXP/SATA1B_RXP — E37 — SATA1B_RXP
PCIE14_RXN/SATA1B_RXN — D39 — SATA1B_RXN
PCIE15_RXP/SATA2_RXP — E41
PCIE15_RXN/SATA2_RXN — F41
PCIE16_RXP/SATA3_RXP — E42
PCIE16_RXN/SATA3_RXN — D43

F45 PCIE17_TXP/SATA4_TXP
E45 PCIE17_TXN/SATA4_TXN
G44 PCIE18_TXP/SATA5_TXP
G45 PCIE18_TXN/SATA5_TXN
H44 PCIE19_TXP
H43 PCIE19_TXN
J45 PCIE20_TXP
K44 PCIE20_TXN

PCIE17_RXP/SATA4_RXP — H40
PCIE17_RXN/SATA4_RXN — H42
PCIE18_RXP/SATA5_RXP — G37
PCIE18_RXN/SATA5_RXN — K37
PCIE19_RXP — L39
PCIE19_RXN — L37
PCIE20_RXP — N38
PCIE20_RXN — N39

2 OF 10

GPP_E8/SATALED# — AD44 — PCH_SATA_LED# — R393 X_10K/4 — +3V

SPT-H

PLTRST# Buffer

+3VA
R323 10K1%4
(12) PLTRST# — R307 10K1%4 — Q32 N-MMBT3904
+3VA — C278 C0.1u6.3X4
U24A NC7WZ14P6X_SC70
RSTOUT0# — R319 33R1%4 — RST_SIO# (22)
R316 33R1%4 — RST_LAN# (19)
R311 33R1%4 — RST_CH7517# (18)
R324 33R1%4 — RST_TPM# (21)
+3VA
U24B
RSTOUT1# — R308 33R1%4 — RST_PCIE1# (21)
R309 33R1%4 — RST_PCIE2# (21)
R310 33R1%4 — RST_JTPM# (21)
R925 X_33R1%4 — RST_GL850# (17)

SATA Riser Connector

SATA1
+5V — 1A — L11 80L6A-30/8 — SATA_5V
C107 C10u10Y8
C97 C0.1u6.3X4

B1 12V
B2 12V
B3 12V
B4 GND
B5 SMCLK
B6 SMDATA
B7 GND
B8 3.3V
B9 3.3V
B10 JTAG1
B11 3.3VAUX
WAKE_#
B12 RSVD
B13 GND
B14 HSOP0+
B15 HSOP0-
B16 GND
B17 PRSNT2_#
B18 GND

A1 PRSNT1_#
A2 12V
A3 12V
A4 GND
A5 JTAG2
A6 JTAG3
A7 JTAG4
A8 JTAG5
A9 3.3V
A10 3.3V
A11 PWRGD
X1
A12 GND
A13 REFCLK+
A14 REFCLK-
A15 GND
A16 HSIP0+
A17 HSIP0-
A18 GND
X2

ST_RXN1
ST_RXP1
ST_TXP1
ST_TXN1
ST_RXN0
ST_RXP0
ST_TXP0
ST_TXN0

SLOT-PCIG6P-2PITCH

0.1uf caps placed on riser BD.

SATA0B_TXP — R188 0R/4 — ST_TXP0
SATA0B_TXN — R191 0R/4 — ST_TXN0
SATA0B_RXN — R162 0R/4 — ST_RXN0
SATA0B_RXP — R184 0R/4 — ST_RXP0

SATA-0B

SATA1B_TXP — R116 0R/4 — ST_TXP1
SATA1B_TXN — R122 0R/4 — ST_TXN1
SATA1B_RXN — R106 0R/4 — ST_RXN1
SATA1B_RXP — R108 0R/4 — ST_RXP1

SATA-1B

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Title	PCH-USB/PCIE/DMI/SATA	
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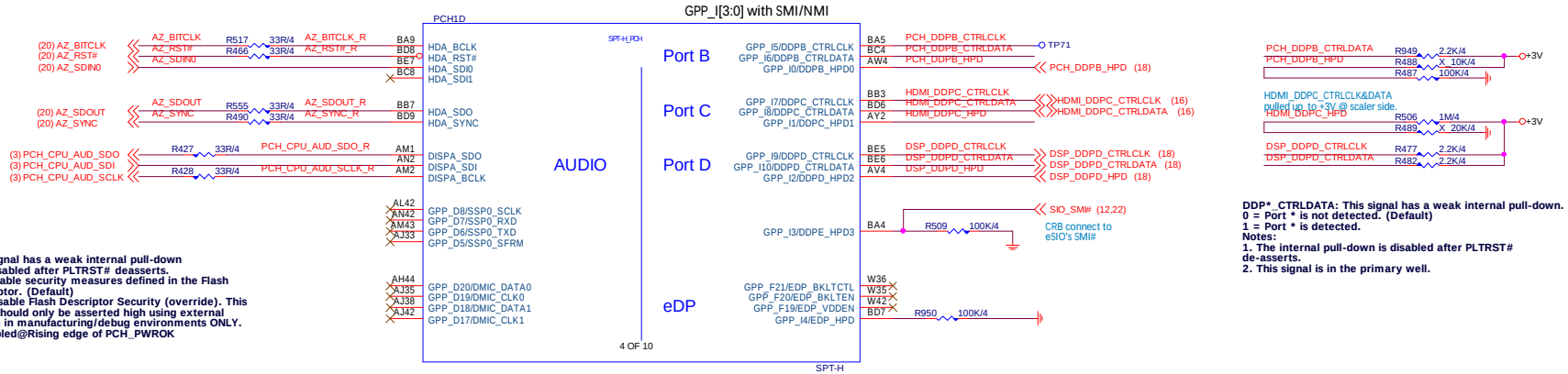
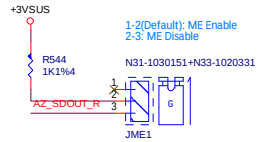
PCH-Audio & Display



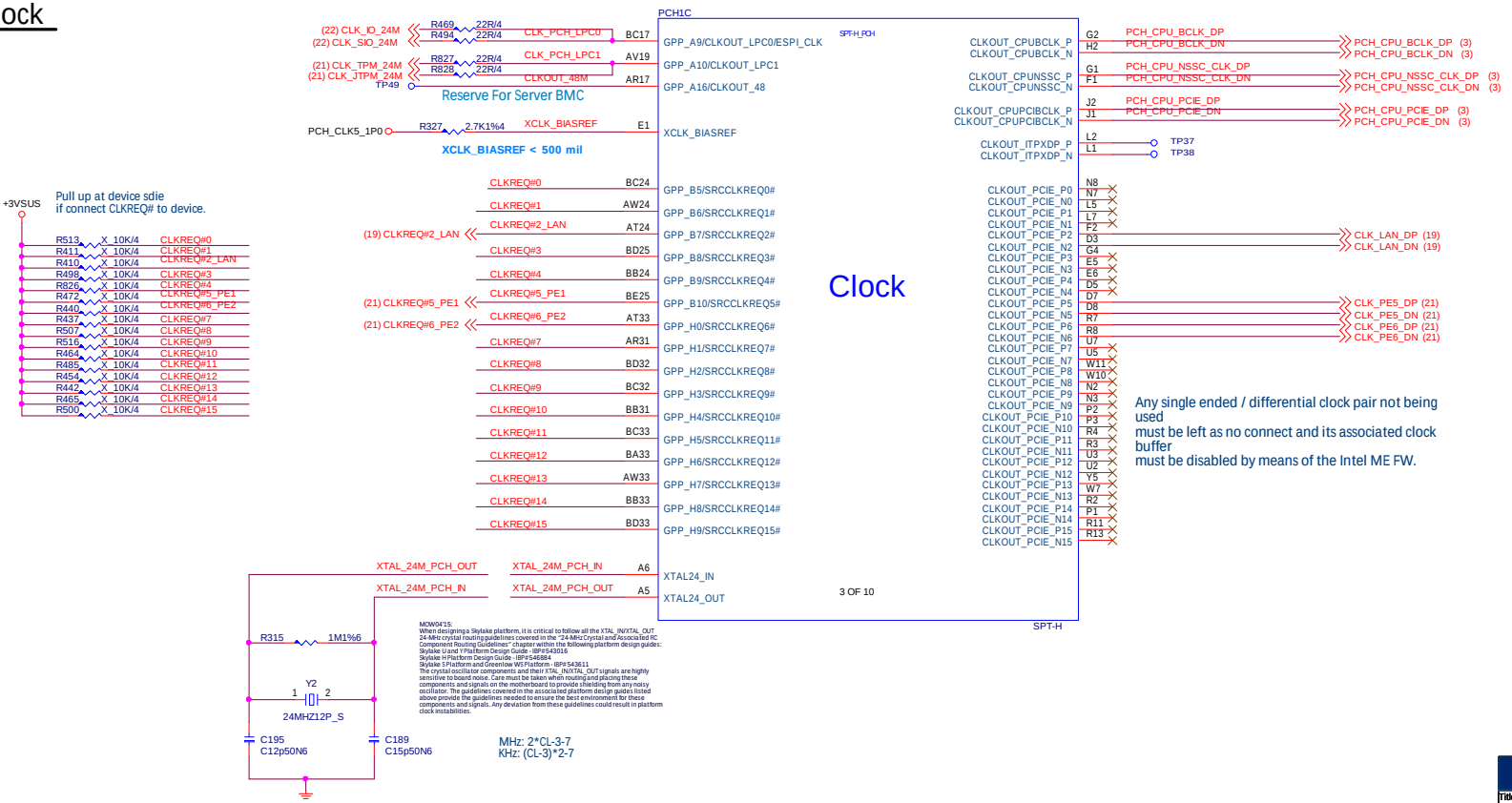
Flash Descriptor Security Override



This signal has a weak internal pull-down and disabled after PLTRST# deasserts.
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
***Sampled@Rising edge of PCH_PWROK**

DDP*_CTRLDATA: This signal has a weak internal pull-down.
0 = Port * is not detected. (Default)
1 = Port * is detected.
Notes:
1. The internal pull-down is disabled after PLTRST# de-asserts.
2. This signal is in the primary well.

PCH-Clock



Title	PCH-Audio/Display/Clock		
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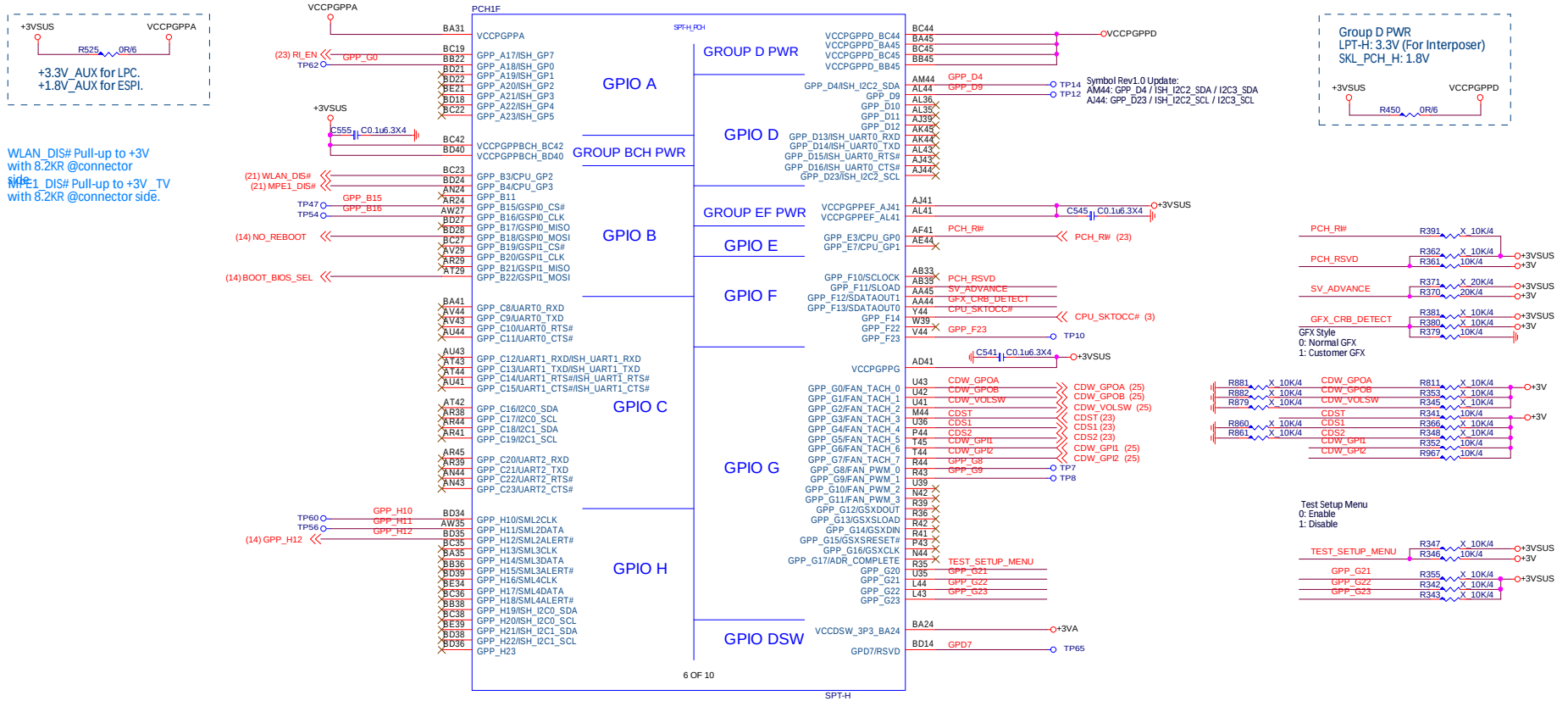
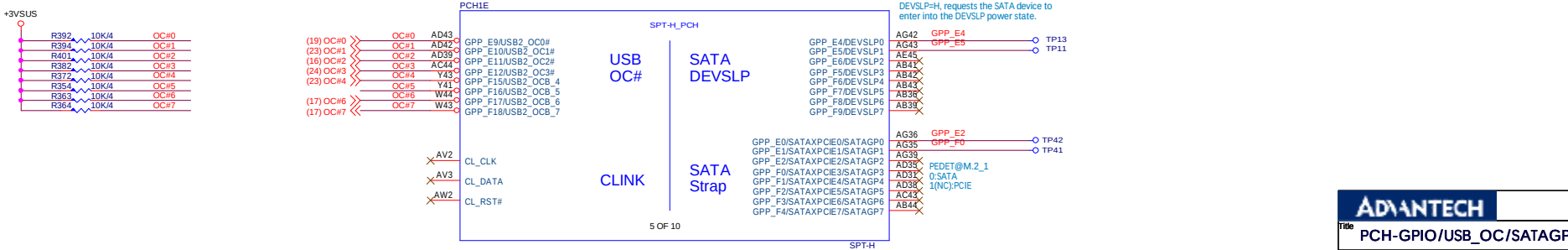
PCH-GPIO



PCH-USB_OC & SATAGP



Title	PCH-GPIO/USB_OC/SATAGP
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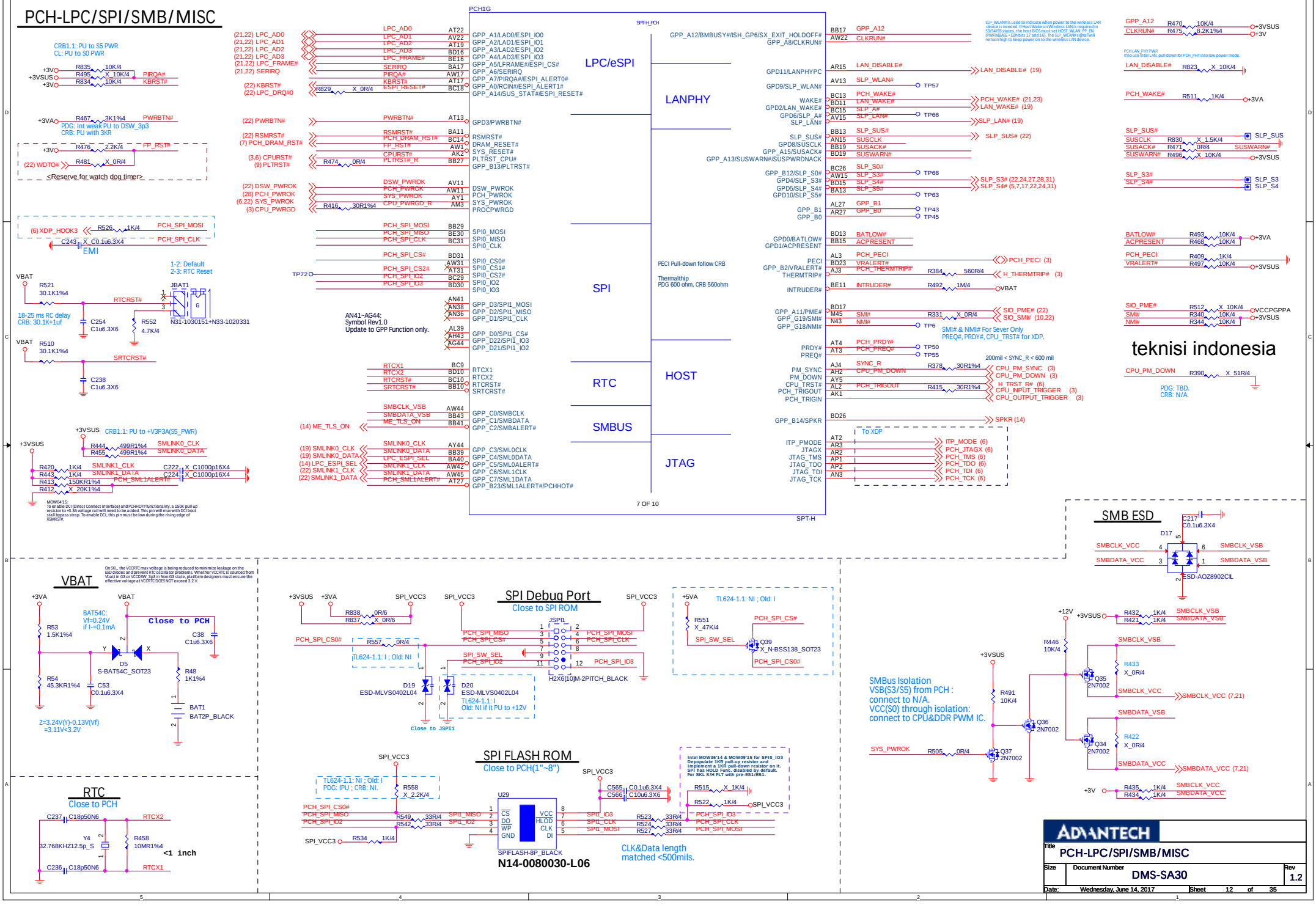
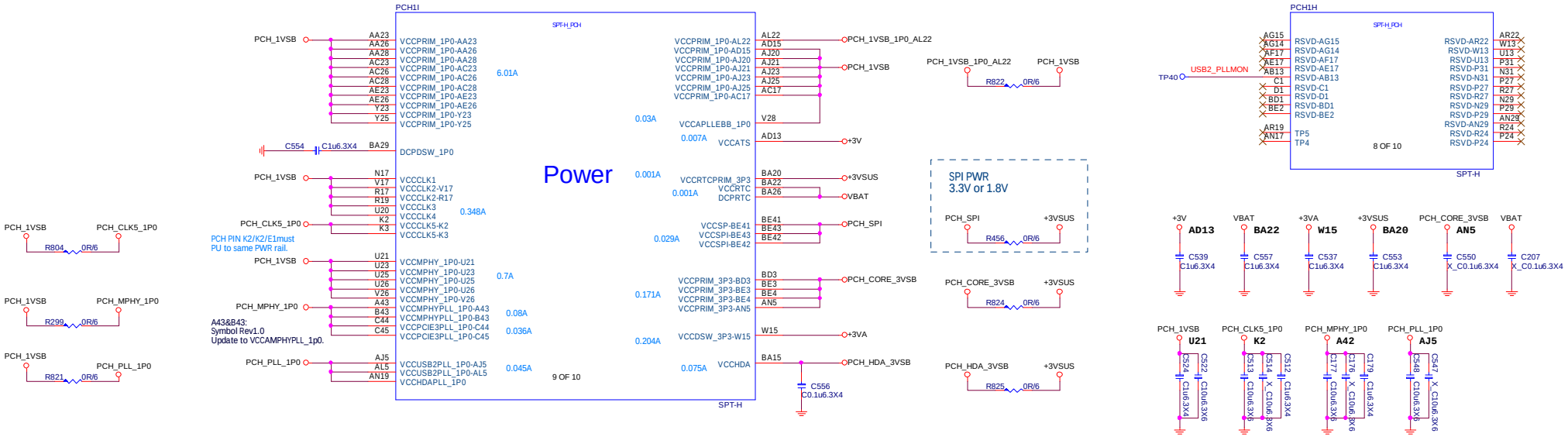
PCH-LPC/SPI/SMB/MISC



PCH-Power



TPM - SLB9670VQ2.0 (SPI I/F)

<Reserve>

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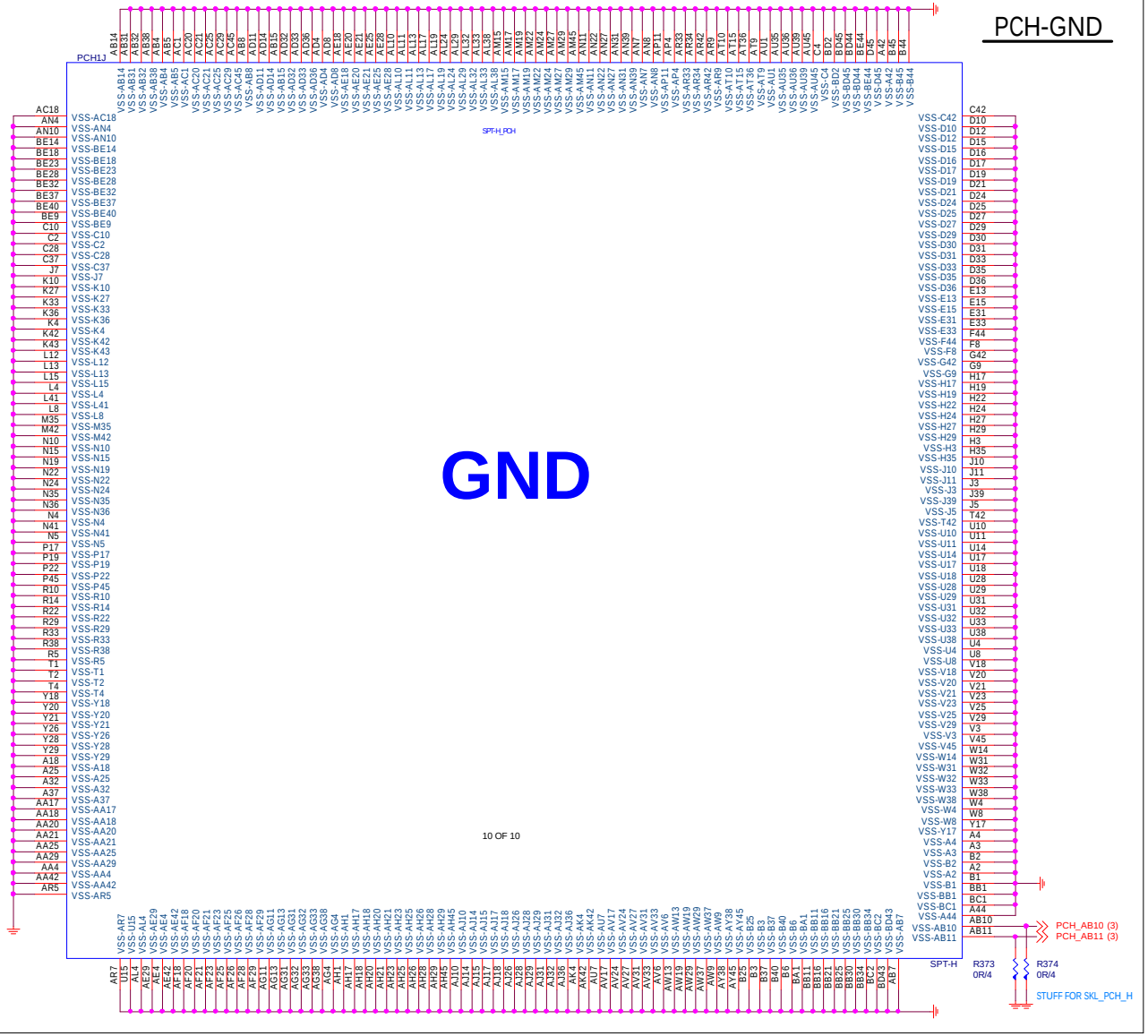
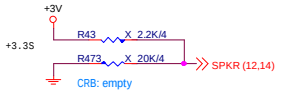
PCH-GND



PCH-Strap

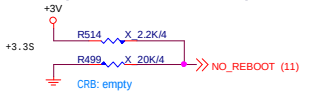
For Strapping pull-up resistor
CRB1.1: 4.7KR
PDG2.1: 1~2.2KR

Top Swap(SPKR/GPP_B14)



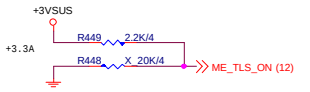
This signal has an integrated weak pull-down resistor (20 KΩ nominal) to disable Top-Block Sway by default.
To enable Top-Block Swap, this signal should be pulled up to V3.3S through a 1k to 2.2 KΩ ±5% resistor.

No Reboot(GSPI0_MOSI/GPP_B18)



This signal has an integrated weak pull-down resistor (20 KΩ nominal) to disable the no reboot strap functionality by default.
To enable no reboot on TCO Timer expiration, this signal should be pulled-up to V3.3S through a 1k to 2.2 KΩ ±5% resistor.

Intel ME Crypto Transport Layer Security (TLS-SMBALERT#/GPP_C2)

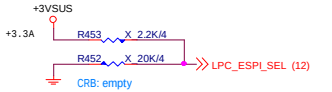


This signal has an integrated weak pull-down resistor (20 KΩ nominal) to disable IntelR ME Cryptographic Transport Layer Security (TLS) cipher suite (no confidentiality).
To enable IntelR ME Cryptographic Transport Layer Security (TLS) cipher suite with confidentiality, this signal should be pulled up to V3.3A through a 1k to 2.2 KΩ ±5% resistor.

Boot BIOS Strap Bit (GSPI1_MOSI/GPP_B22)

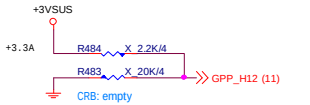
This signal has an integrated weak pull-down resistor (20 KΩ nominal) to default boot from SPI.
To enable boot to LPC, this signal should be pulled up to V3.3S through a 1k to 2.2 KΩ ±5% resistor.

ESPI/LPC SEL Strap(SML0ALERT#/GPP_C5)



This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

ESPI Flash Sharing Mode(GPP_H12)



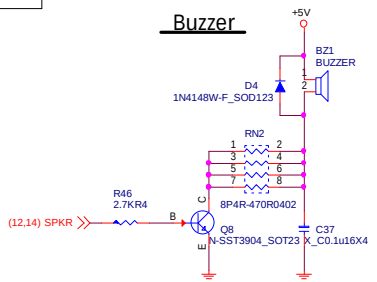
This signal has a weak internal pull-down.
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
Note: The pull-down resistor is disabled after RSMRST# de-asserts

SPI0_MOSI & SPI0_MISO:
This signal has an internal pull-up.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling(RSMRST#).

SML1ALERT# /PCHHOT#/GPP_B23:
This signal has an internal pull-down.
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling(RSMRST#).

SPI0_IO2 & SPI0_IO3:
This signal has an internal pull-up.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling(RSMRST#).

Buzzer



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Title	PCH-GND/Strap	
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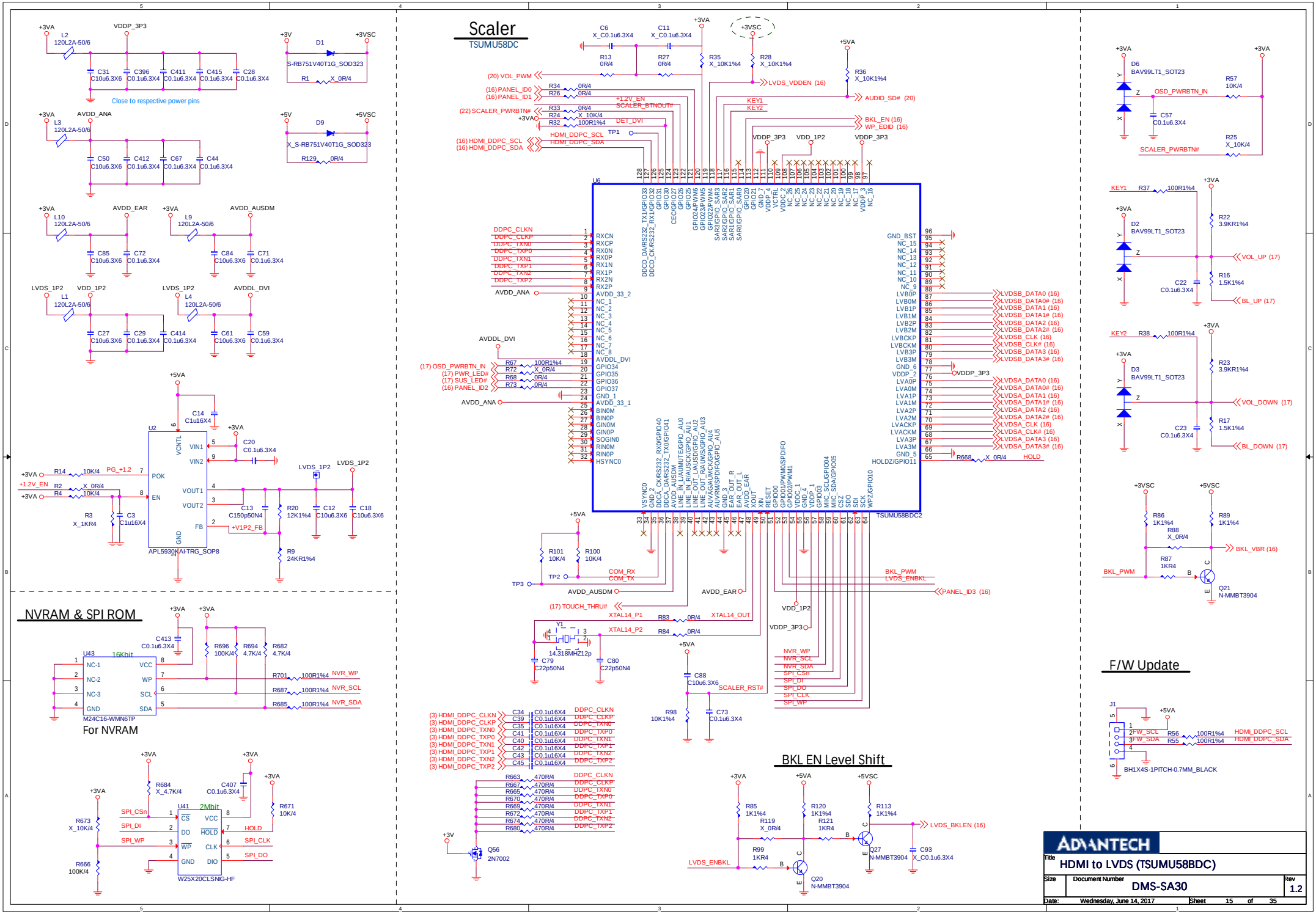
Scaler
TSUMU58DC
NVRAM & SPI ROM
For NVRAM
F/W Update
BKL EN Level Shift
Close to respective power pins
TSUMU58BDC2
APL5930KAI-TRG_SOP8
M24C16-WMN6TP
W25X20CLSNIG-HF
BH1X4S-1PITCH-0.7MM_BLACK
ADVANTECH
Title
HDMI to LVDS (TSUMU58BDC)
Size
Document Number
DMS-SA30
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1.2
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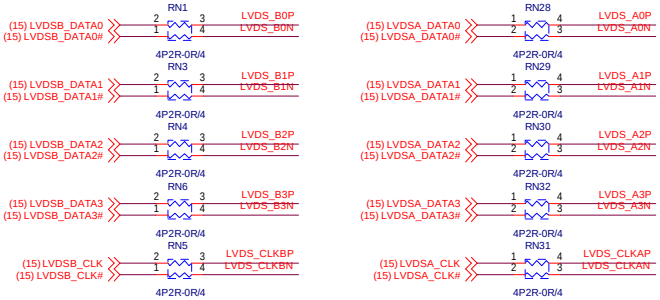
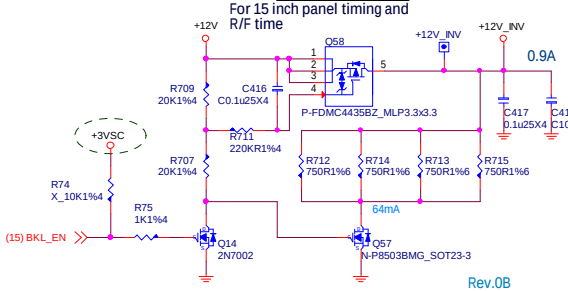
LVDS Output

R3C-0000012-W08 Co-layout with L12-9008090-M09
Note. The pin's definition between R&L are difference.



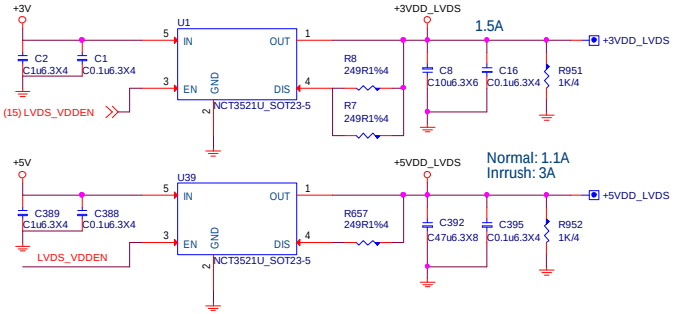
+12V For BL

For 15 inch panel timing and R/F time



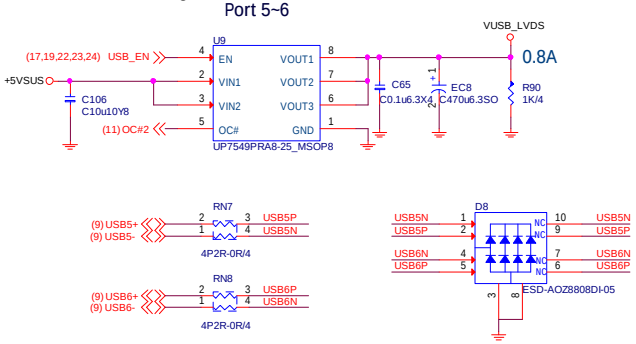
Rev.0B
C16&C395 stuff 1KR to discharge VDD_LVDSunder G3

+3V&+5V For LVDS

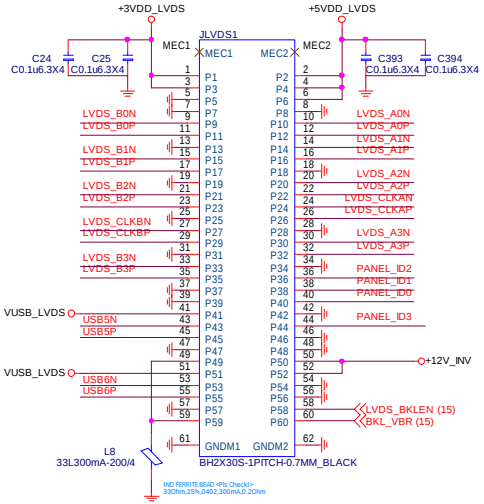


USB Signal & PWR For LVDS Conn.

Port 5~6

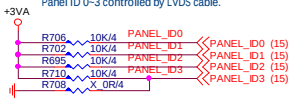


LVDS & BL & USB2.0*2 Conn.



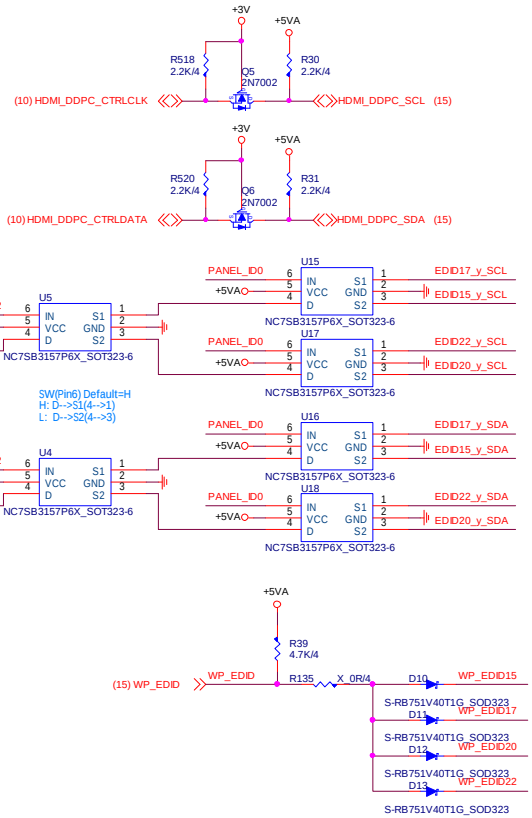
Pannel ID

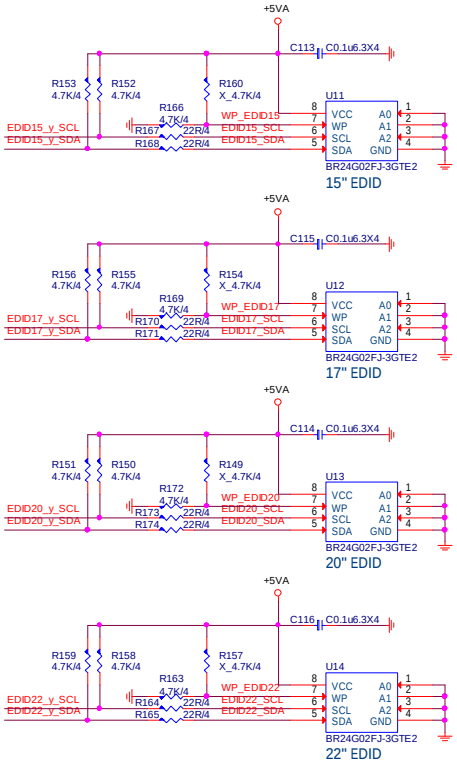
Panel ID 0~3 controlled by LVDS cable.



170109
ID 0~2 PD to GND by LVDS cable for 20" monitor.

EDID Switch





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Title	LVDS Output & EDID Switch & USB2.0*2	
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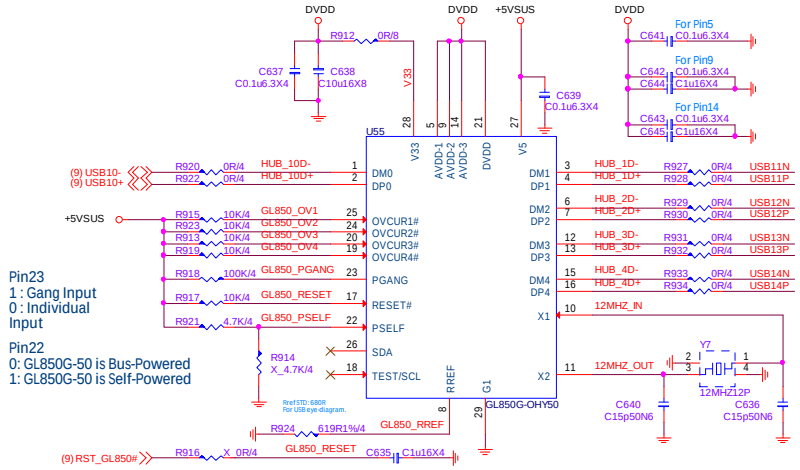
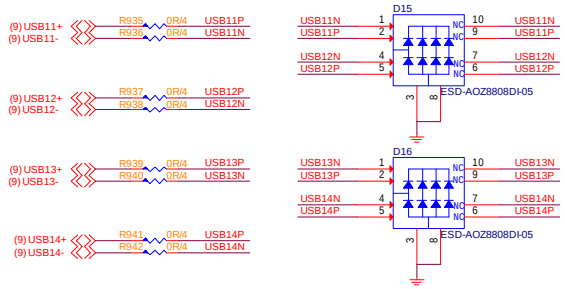
GL850G - USB2.0 HUB

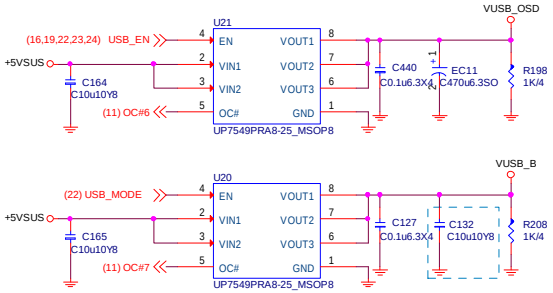
USB Port 10 For H110 Sku



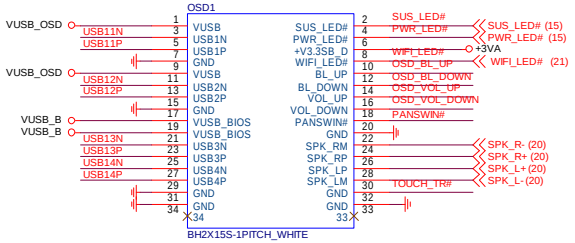
USB Signal & PWR For OSD Conn.

USB Port 11~14 For Q170 Sku

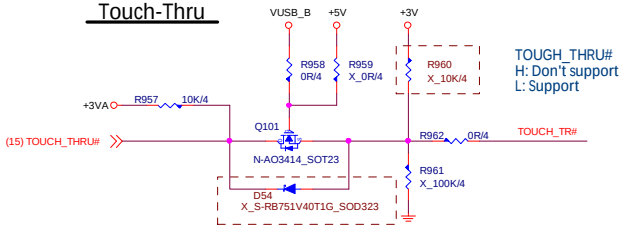




OSD & LED & SPK & USB2.0*4 Conn.

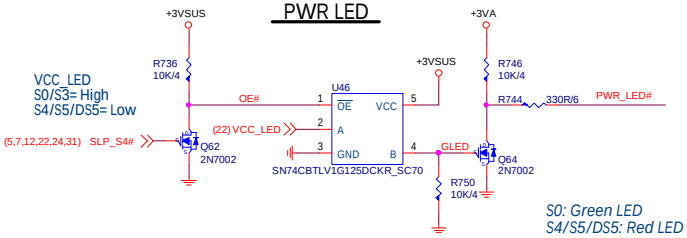


Touch-Thru

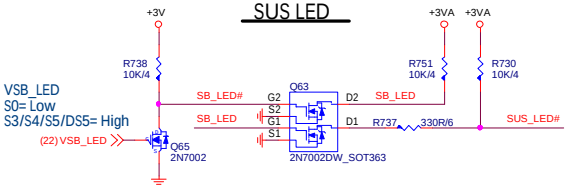


Touch-thru feature. Typical functionality is:
1. After pressing the "Volume Down" and "Brightness Up" buttons together for 3 seconds, the Touch-thru control status will display as long as the two buttons are pressed.
2. Pressing the "Volume Down" and "Brightness Up" buttons together for ANOTHER 3 seconds toggles the Touch-thru control status between OFF and ON.
3. The Touch-thru feature is "OFF" as default setting.

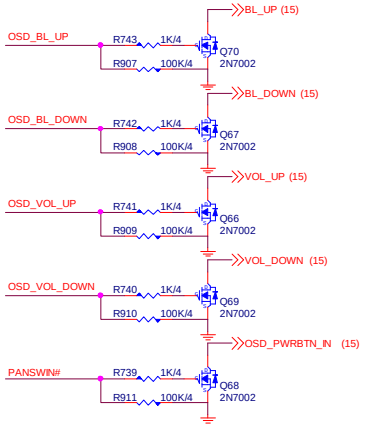
PWR LED

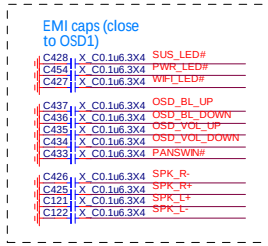


SUS LED



BL & VOL Control





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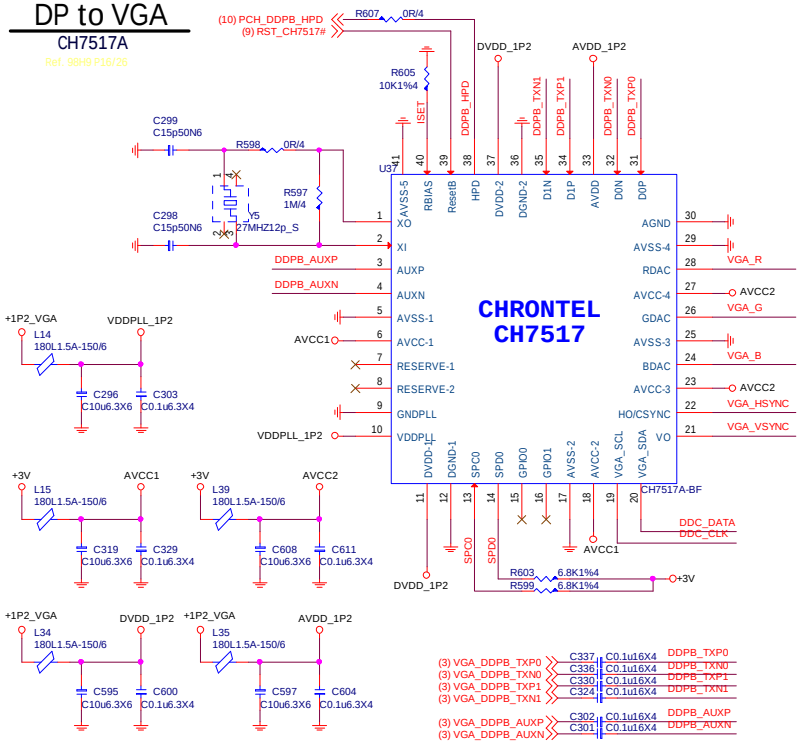
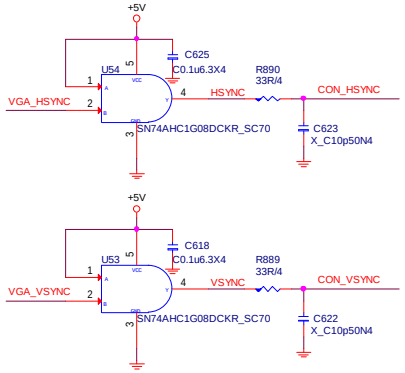
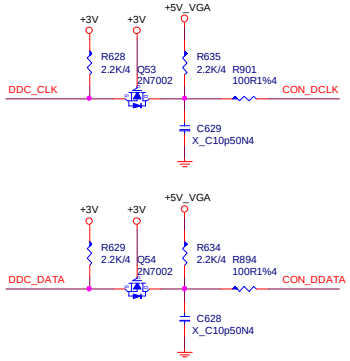
DP to VGA

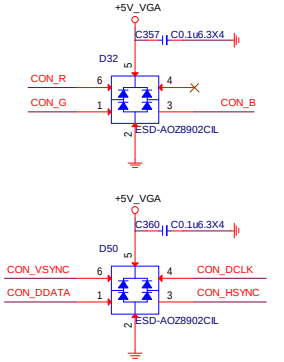
CH7517A

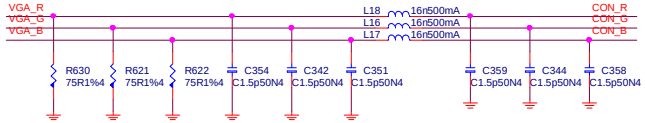
Ref: 98H9 P16/26



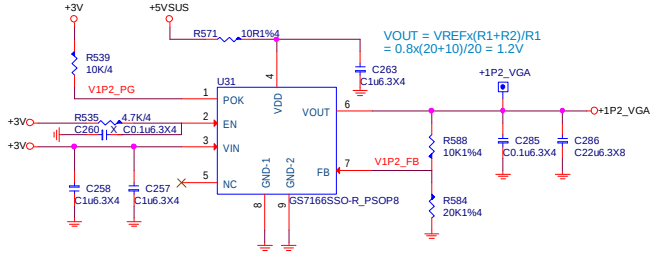


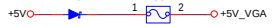


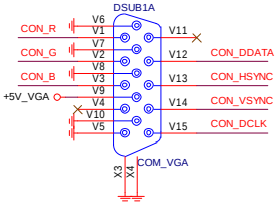




VGA_1P2

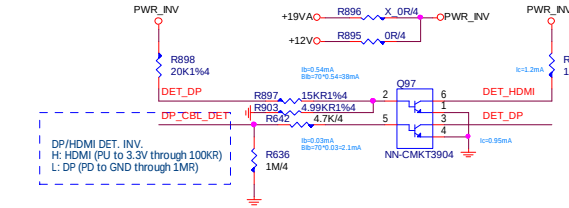


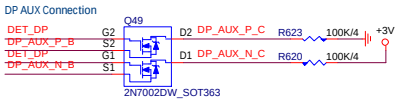


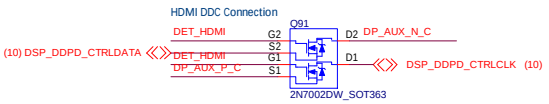


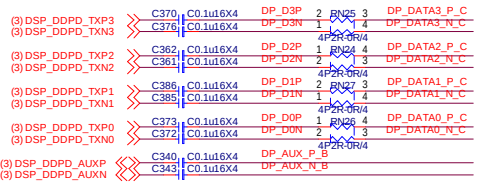
DP Connector

DisplayPort Auxiliary Channel Dual Mode Support Protection Circuit

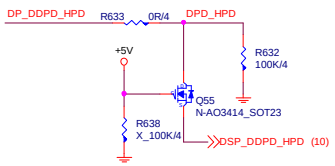


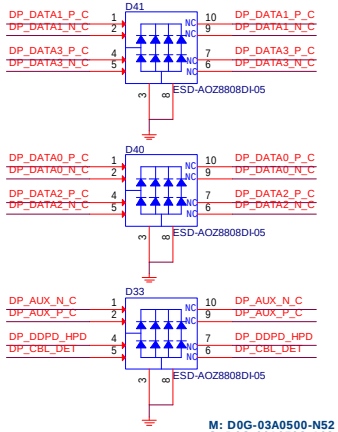




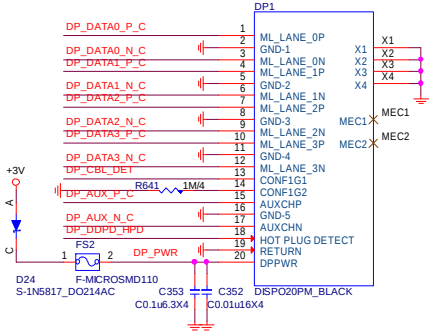


HPD Inversion for DP





M: D0G-03A0500-N52
S: D0G-06A050C-A68
S: D0G-05A0300-I14



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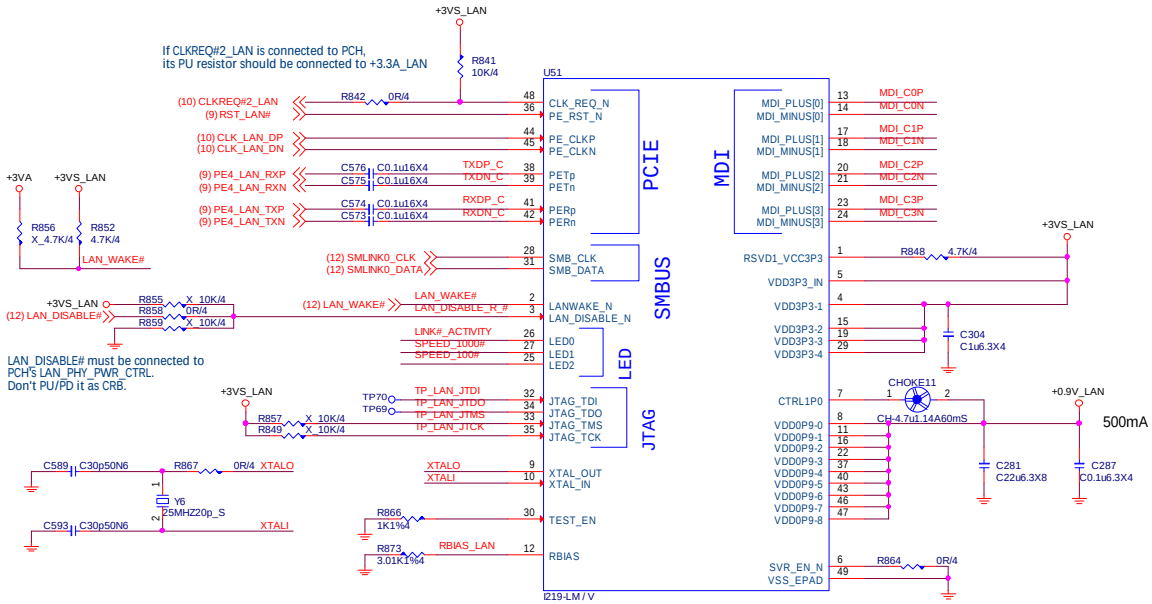
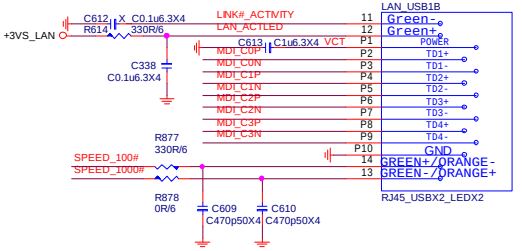
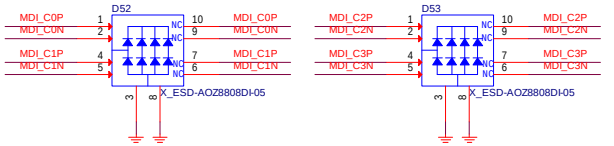
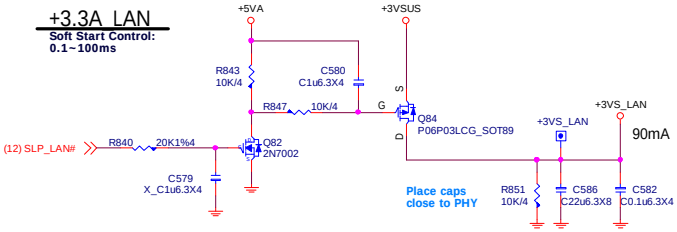
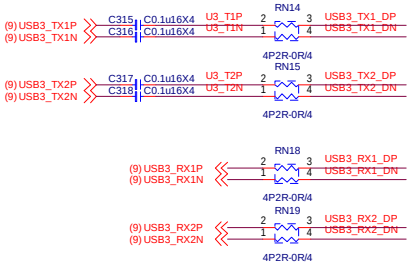
Intel LAN I219-V/LM

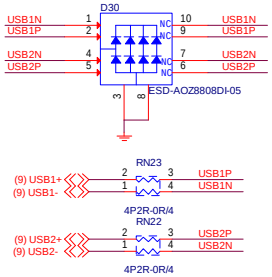


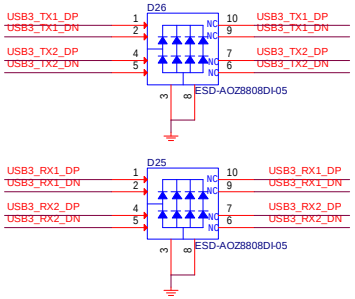


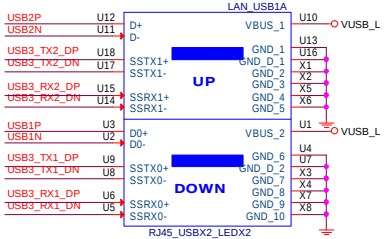


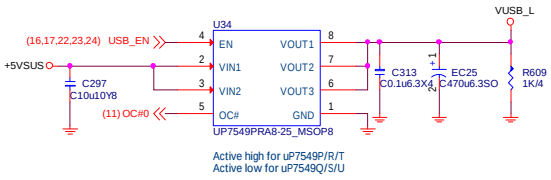












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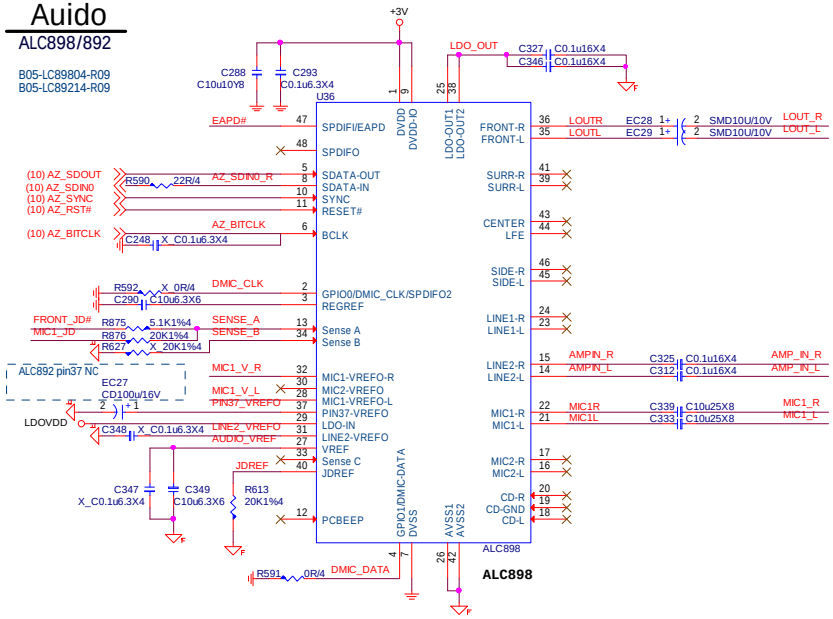
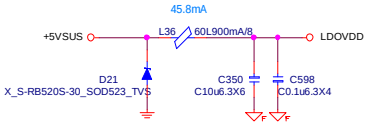
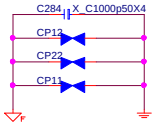
Auido

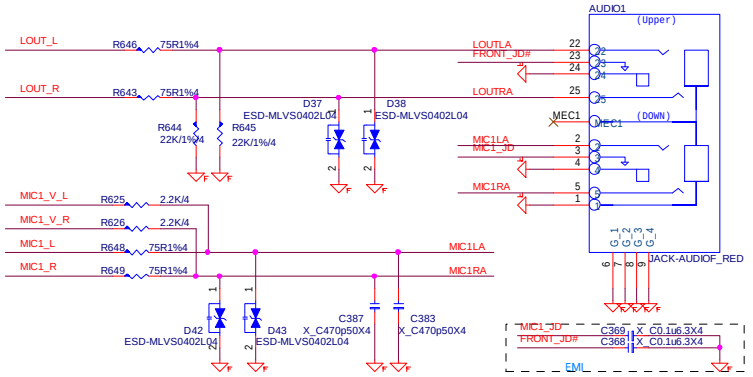
ALC898/892

B05-LC89804-R09
B05-LC89214-R09

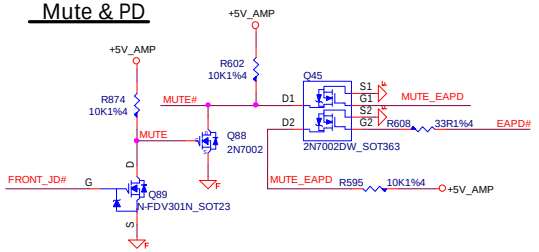




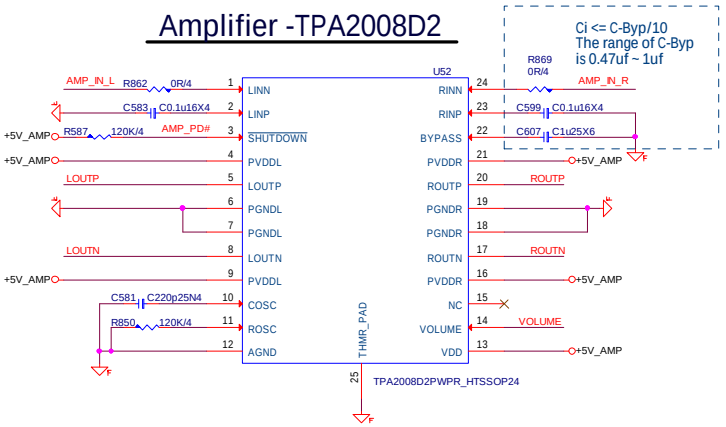


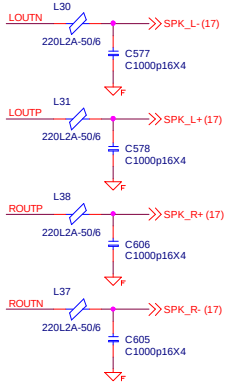


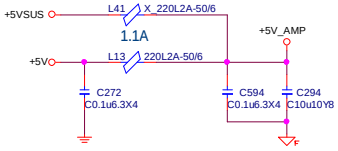
Mute & PD

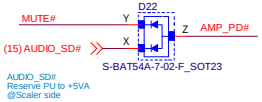


Amplifier -TPA2008D2

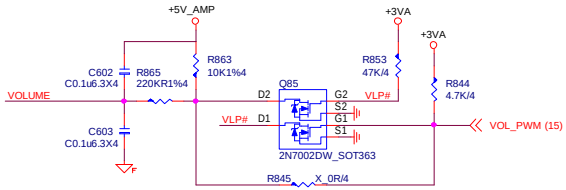








VOL_PWM Level Shift



ADVANTECH		
Title: Audio Codec ALC898/AMP		
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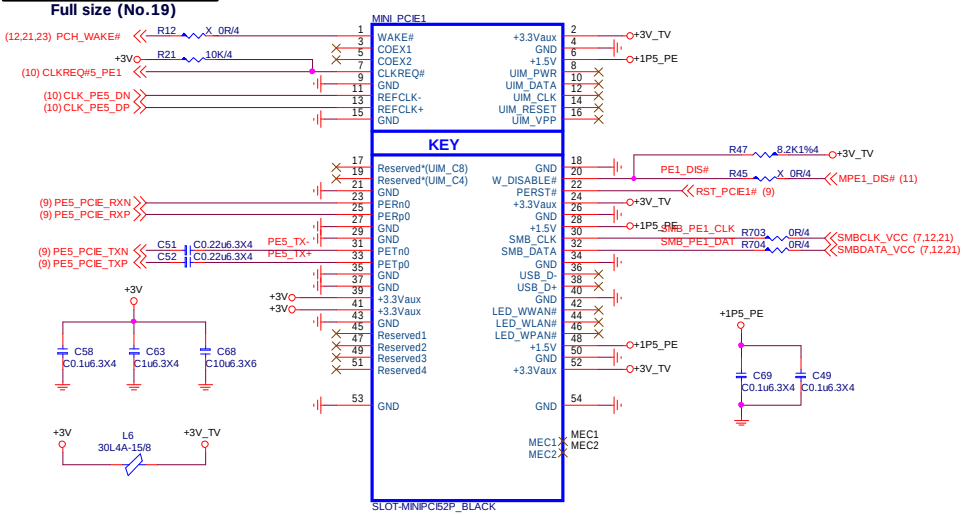
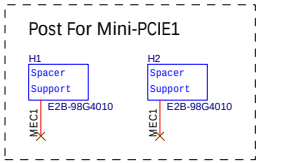
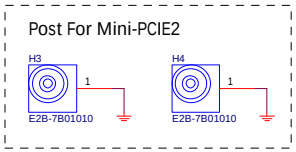
Mini PCI-E Slot

Full size (No.19)

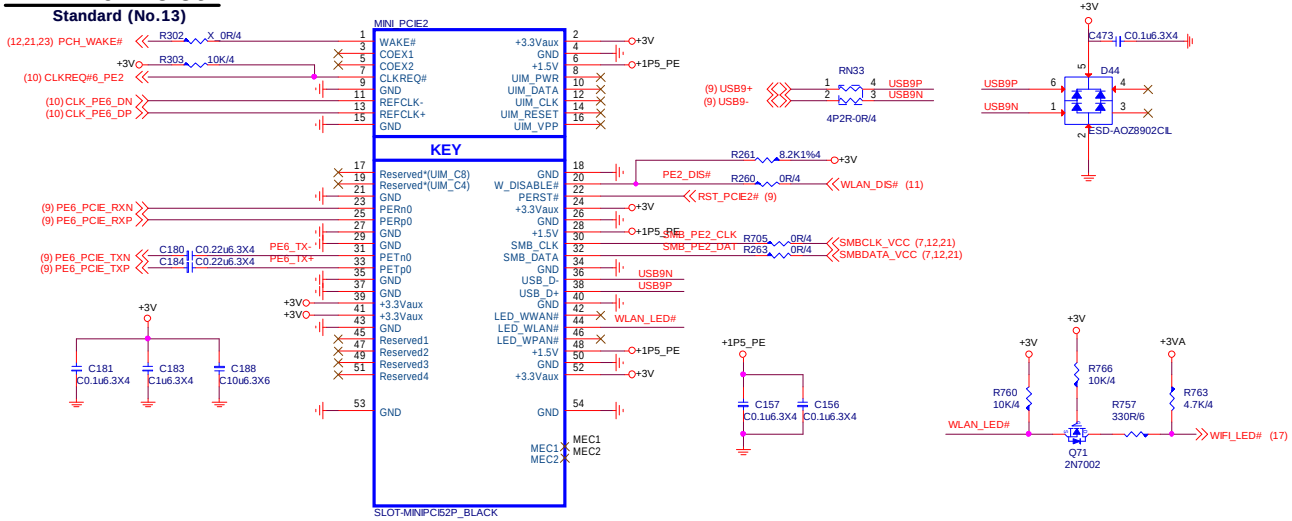






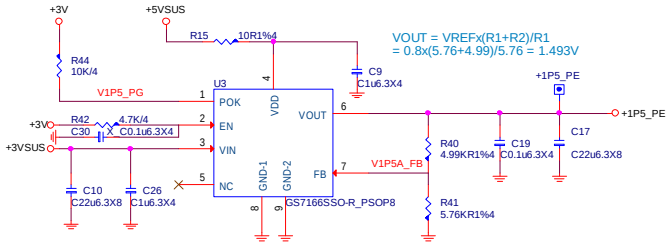
Mini PCI-E Slot

Standard (No.13)



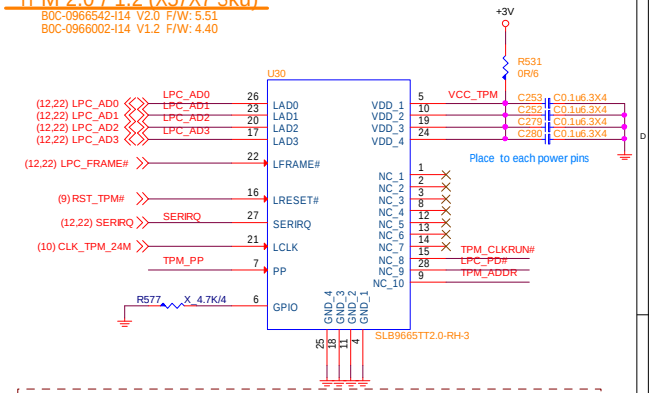
+1P5 For Mini PCI-E Slot *2

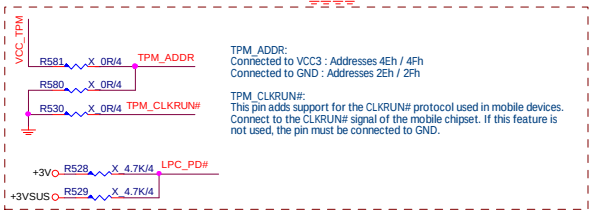
1A



TPM 2.0 / 1.2 (X5/X7 Sku)

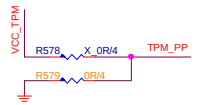
B0C-0966542-I14 V2.0 F/W: 5.51
B0C-0966002-I14 V1.2 F/W: 4.40





TPM_ADDR:
Connected to VCC3 : Addresses 4Eh / 4Fh
Connected to GND : Addresses 2Eh / 2Fh

TPM_CLKRUN#:
This pin adds support for the CLKRUN# protocol used in mobile devices. Connect to the CLKRUN# signal of the mobile chipset. If this feature is not used, the pin must be connected to GND.

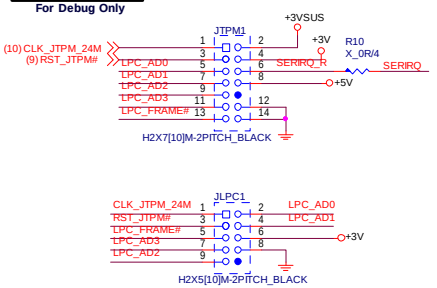


TPM_PP:
Physical presence
This pin indicates physical presence; for usage of this signal, please refer to the TCG specification v1.2. The TPM 2.0 device does not use this functionality.
For compatibility reasons (downgrade capability to a TPM 1.2), the pin should be connected to a jumper. The standard position of the jumper should connect the pin to GND. If the pin is connected to VDD, some special commands are enabled for a TPM 1.2.
This pin does not have an internal pull-up or pulldown resistor and must not be left floating.

NC_9:
Not Connected
This pin may be connected to the Reset signal (for backward compatibility) or may be left floating.

JTPM & JLPC

For Debug Only



EMI

C558 X_C0.1u6.3X4 CLK_TPM_24M
C7 X_C0.1u6.3X4 CLK_JTPM_24M

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Title: Mini PCI-E & TPM & JTPM/JLPC & USB2.0*1

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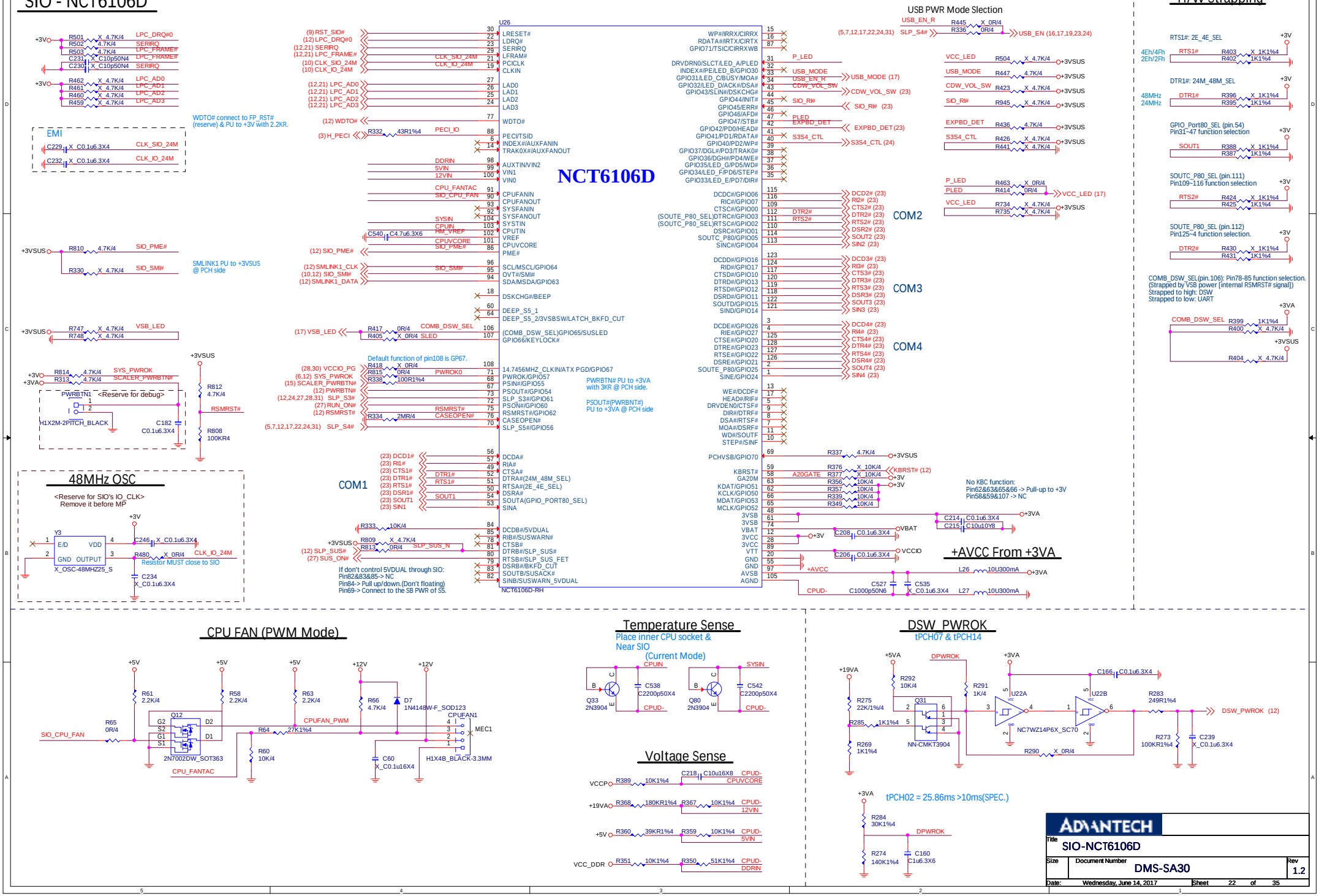
SIO - NCT6106D



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Title	SIO-NCT6106D	
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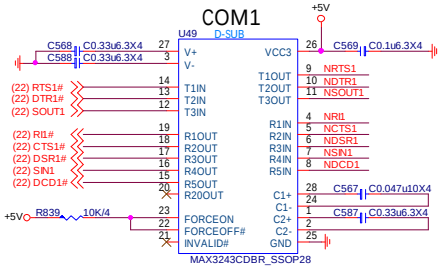
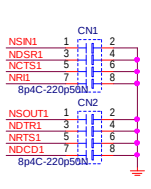
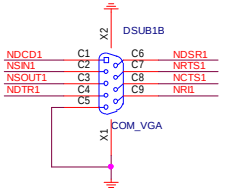
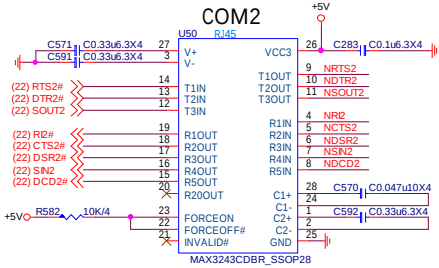
COM 1&2

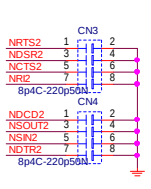
MAX3243CDBR

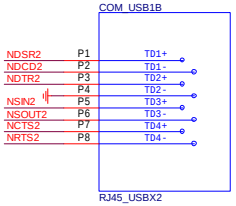


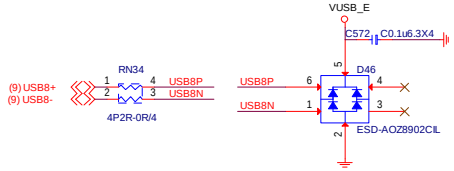


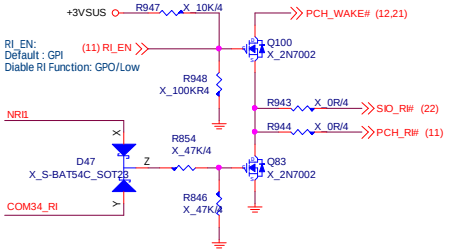


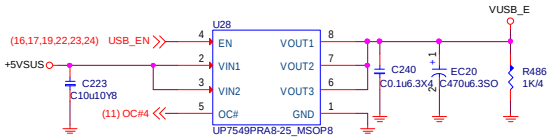






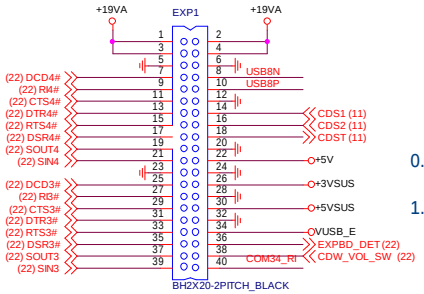






Expansion BD Conn.

COM3&4



0.3A

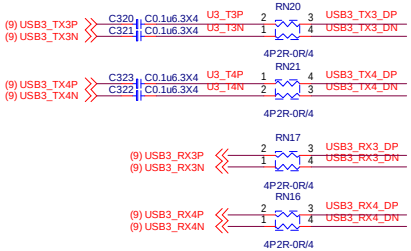
1.5A

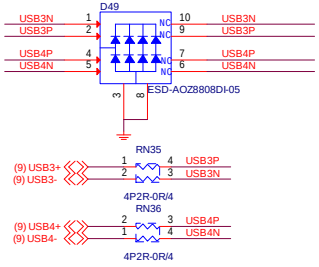
CDS1 & CDS2 :
Cash drawer GPIO output to expansion BD.
Default=Low, this GPIO controlled by AP.

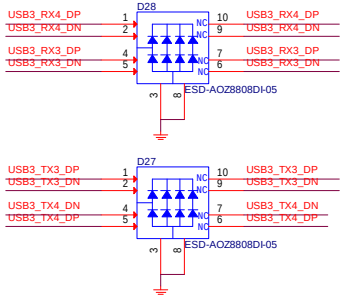
CDST :
Cash drawer status input from expansion BD.
Default=H (Drawer open=Low ; close=High)

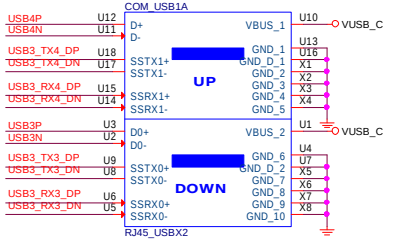
EXPBD_DET
No EXP. BD.= High -> Disable COM3&COM4
Insert EXP. BD.= Low -> Enable COM3&COM4

CDW_VOL_SW
+24VSB/+12VSB selection output for expansion BD.
Default=H, It controlled by BIOS setup manual

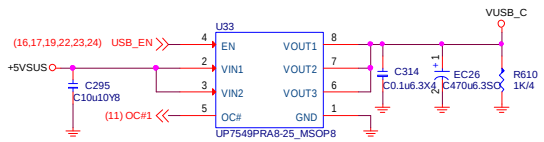








RJ45(COM+USB)
USB3.0: N58-26F0031-S42
USB2.0: N58-16F0291-S42



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Title	COM & Exp BD & USB3.0	
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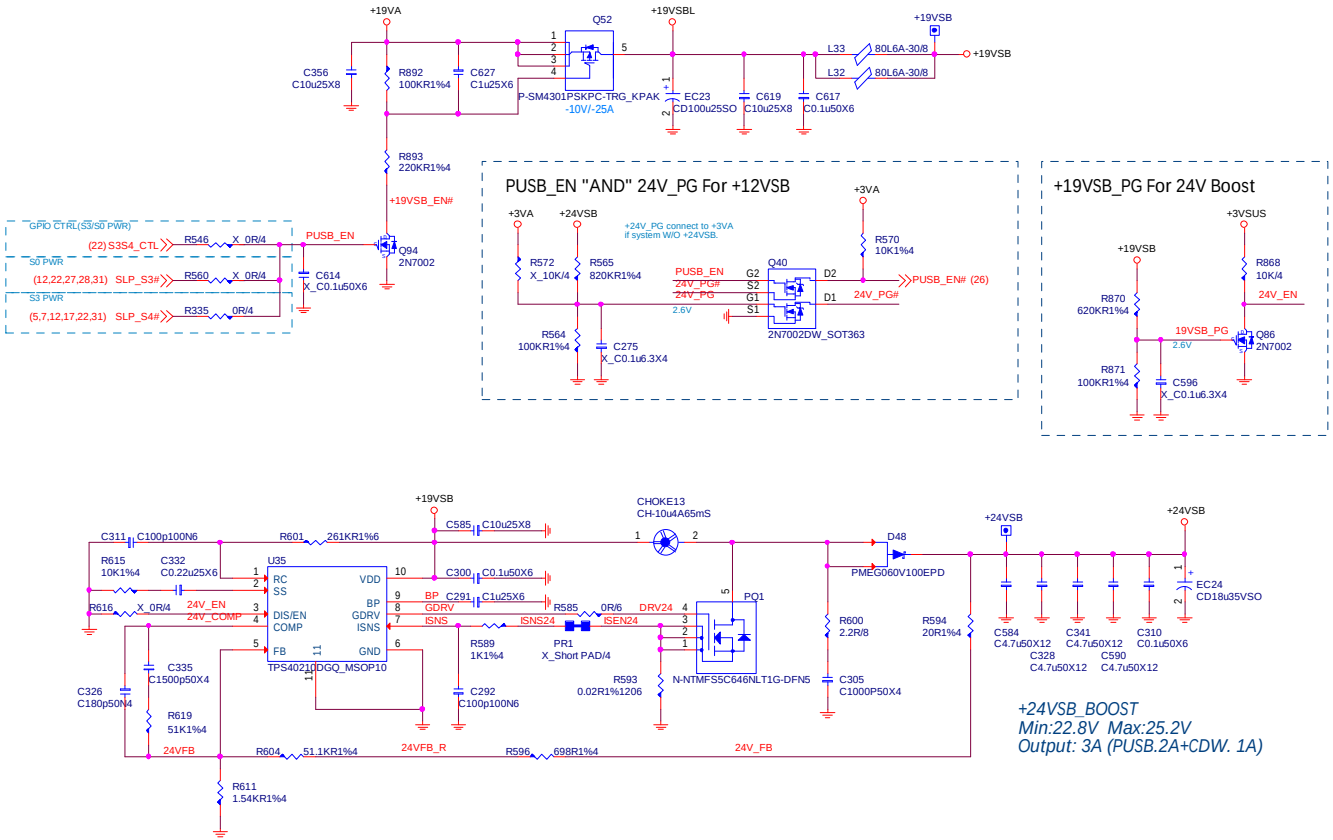
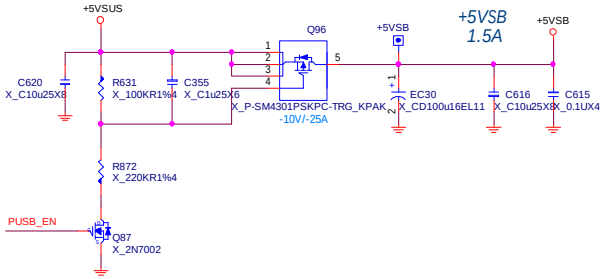
+24V Boost (S3/S0 PWR)

TPS40210



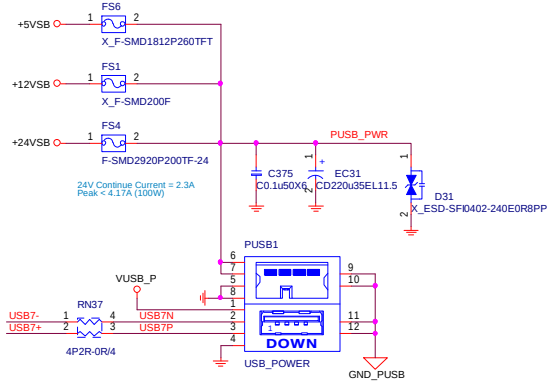
+5VSB (S3/S0 PWR)

Reserve for FS6 of PUSB



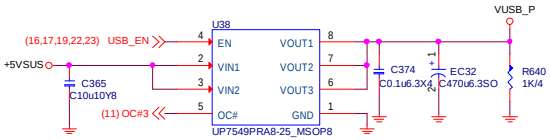
Power USB

The default spec would stay with +24PUSB spec as VS defined,
and reserve the +12V/+5V PUSB EE design on MB for option reuirement.



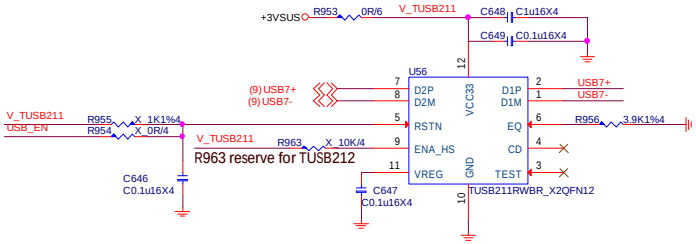
USB Signal & PWR For PWR USB

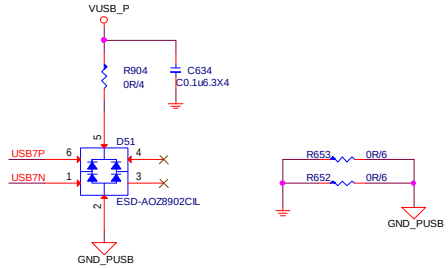
Port 13



TUSB211 USB 2.0 HS Signal Conditioner

Reserve for 5M Certificated USB Cable





ADVANTECH

Title	+24V Boost & +5VSB & Power USB(U2*1)	
Size	Document Number: DMS-SA30	Rev: 1.2
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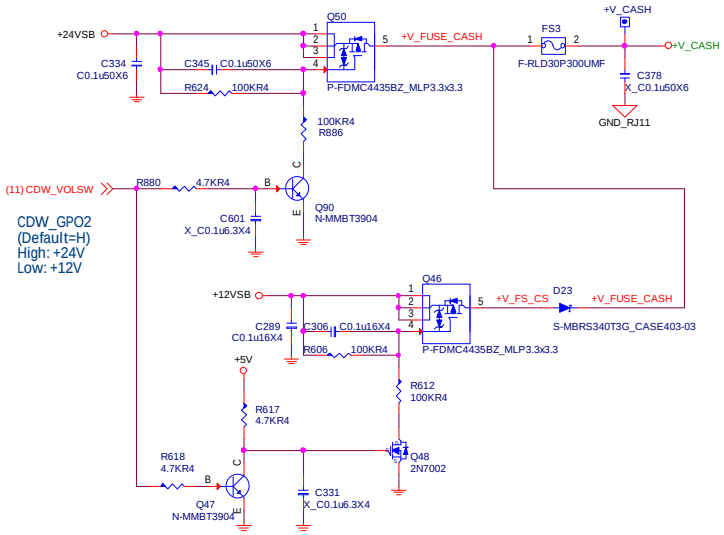
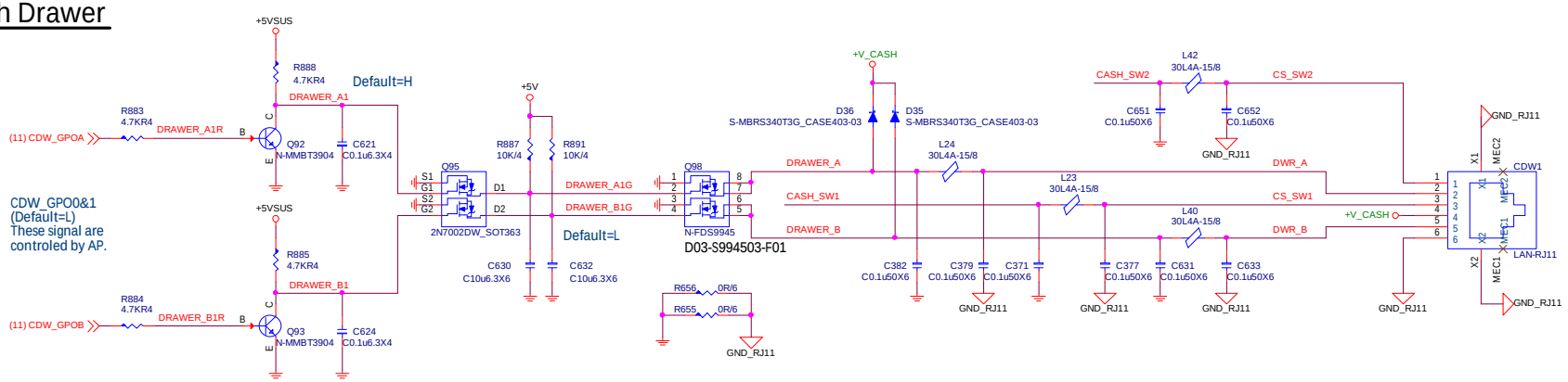
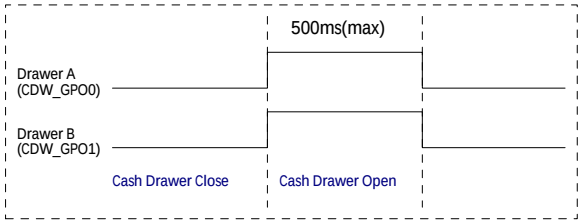
+V_CASH Power Selection

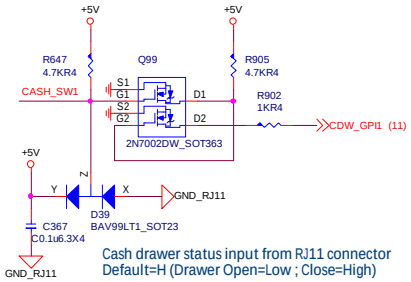
+24VSB / +12VSB

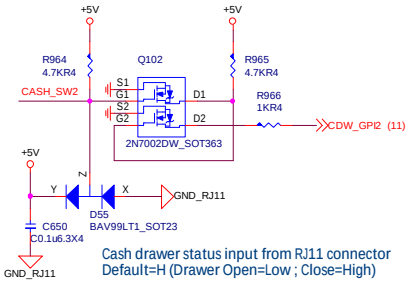


Cash Drawer









ADVANTECH

Title: Cash Drawer		
Size	Document Number: DMS-SA30	Rev: 1.2
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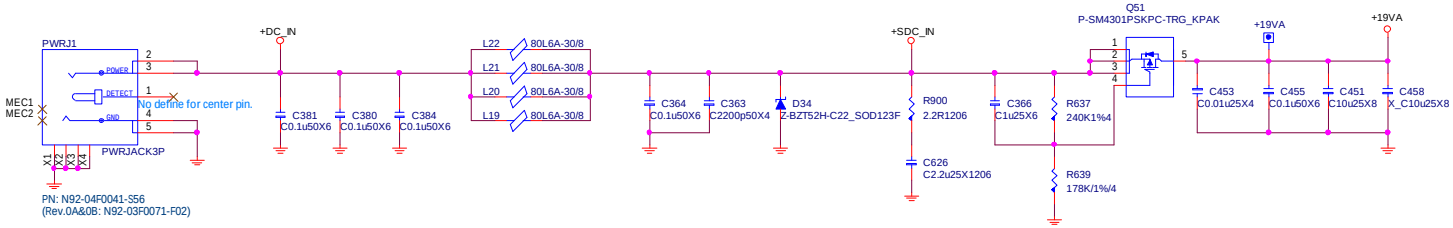
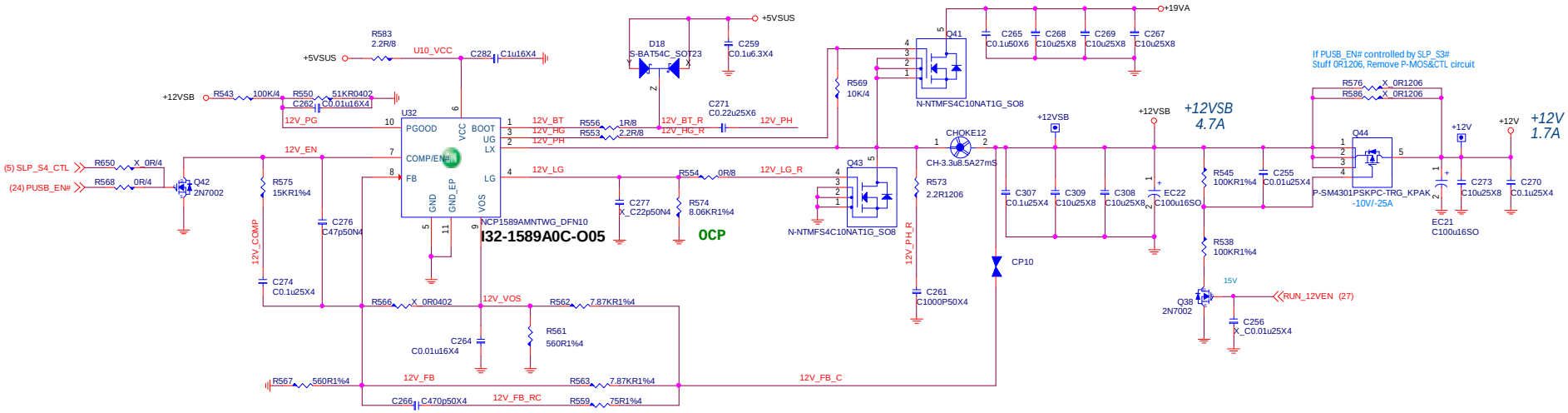
PWR JACK & +19VA

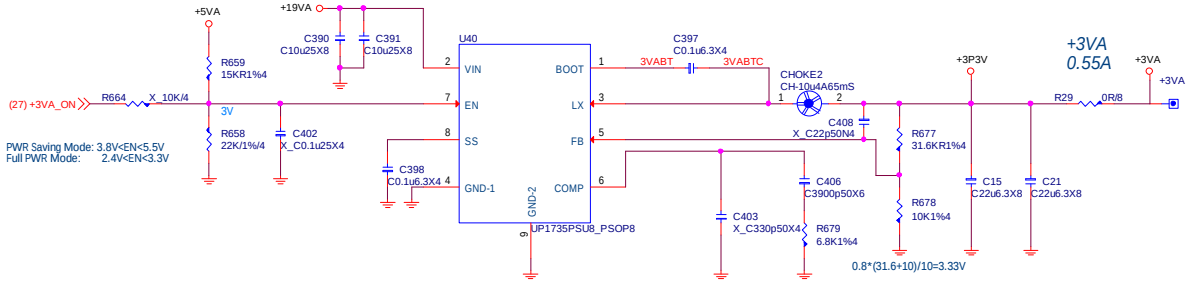


+12VSB (S3/S0 PWR)



+3VA

Provide DSW_3.3V PWR
For Scaler/SIO/SPI ROM



ADVANTECH

Title	PWR_SRC/+12VSB/+12V/+3.3A	
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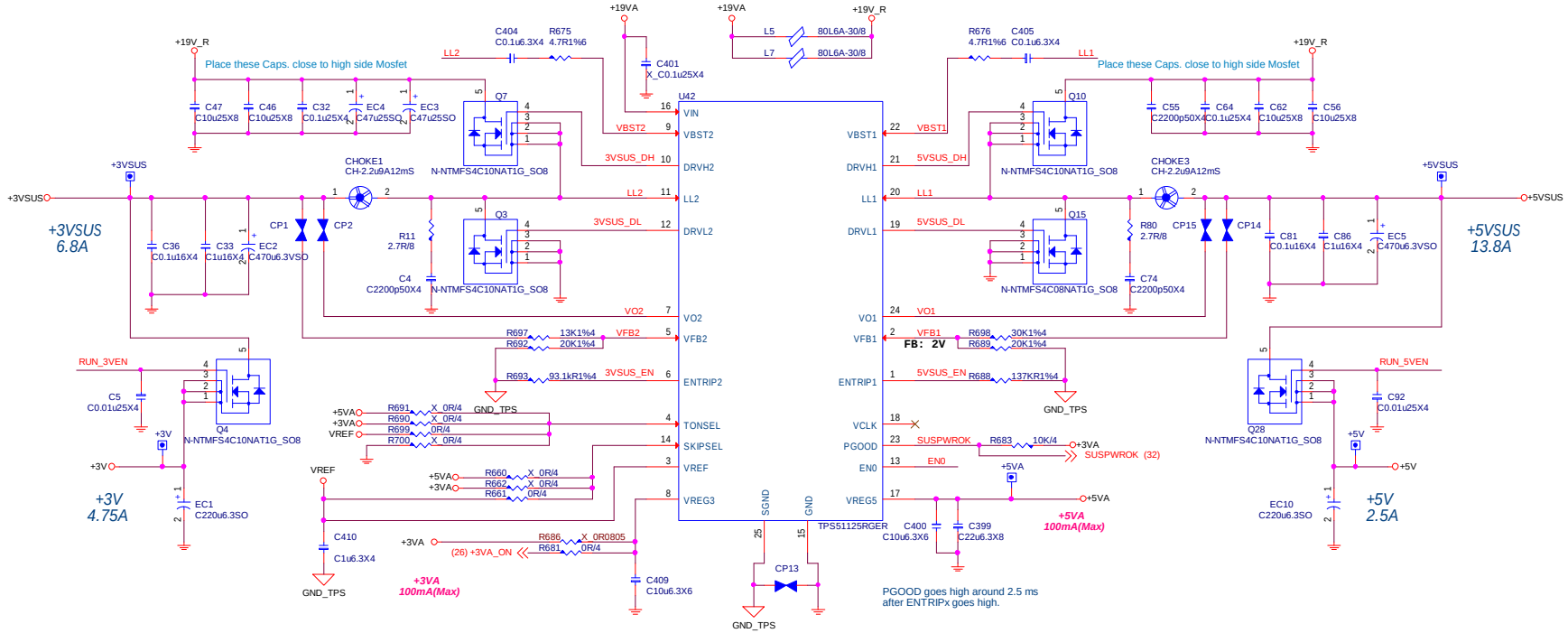
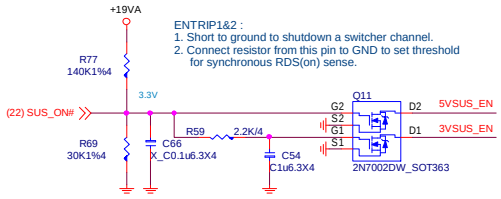
System Power

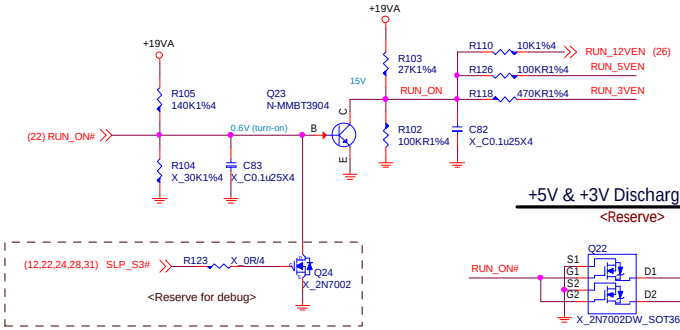
+5VSUS/+3VSUS/+5V/+3V



+5VSUS & +3VSUS Eanble



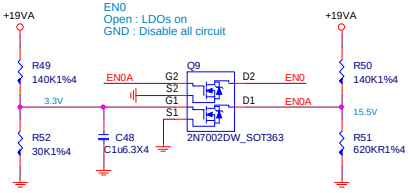
+5V & +3V Eanble



+5V & +3V Discharge Circuit

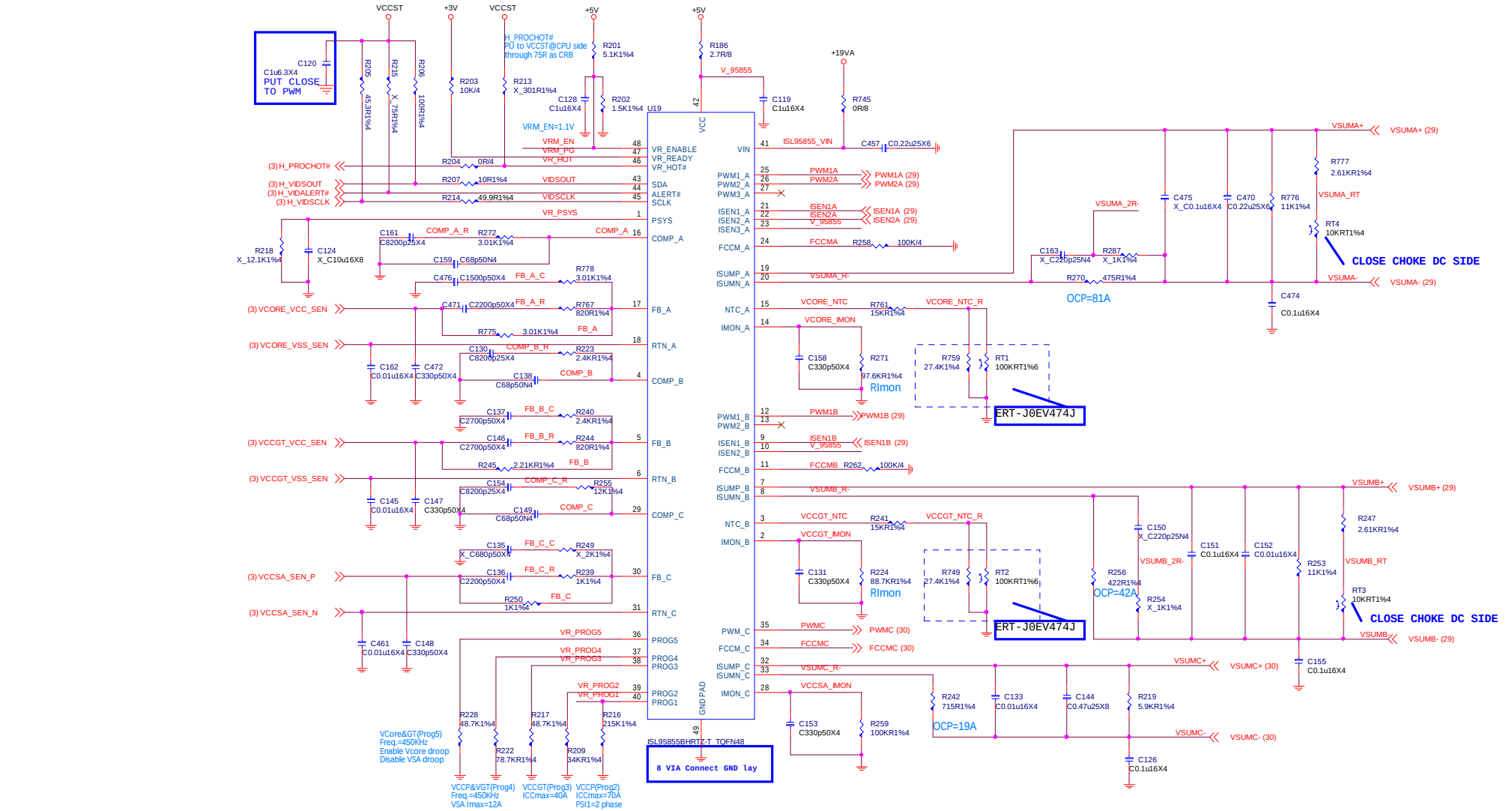
<Reserve>

EN0 delay to wait PWR_SRC ready



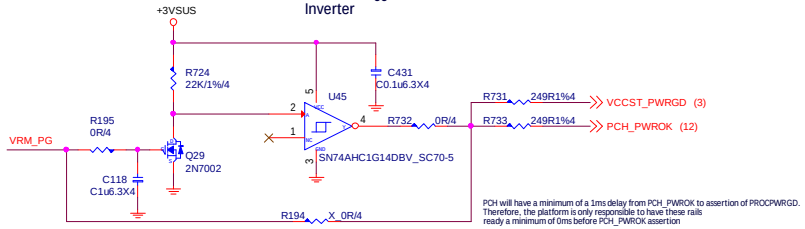
ADVANTECH		
Title: System Power		
Size	Document Number: DMS-SA30	Rev: 1.2
Date: Wednesday, June 14, 2017	Sheet 27 of 35	

SKL S-line 35W (ISL95855B)



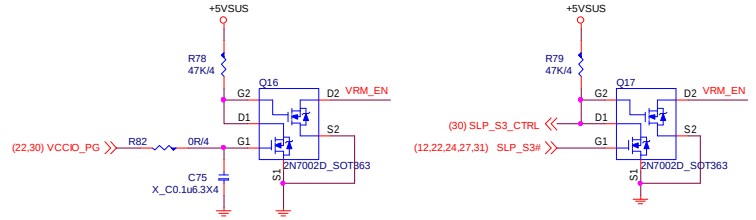
PCH_PWROK

Schmitt-Trigger Inverter



VRM_EN Sequence Control

VCCIO_PG & SLP_S3#



ADVANTECH		
Title: IMVP8-ISL95855(VCCP/VGT/VSA)		
Size	Document Number: DMS-SA30	Rev: 1.2
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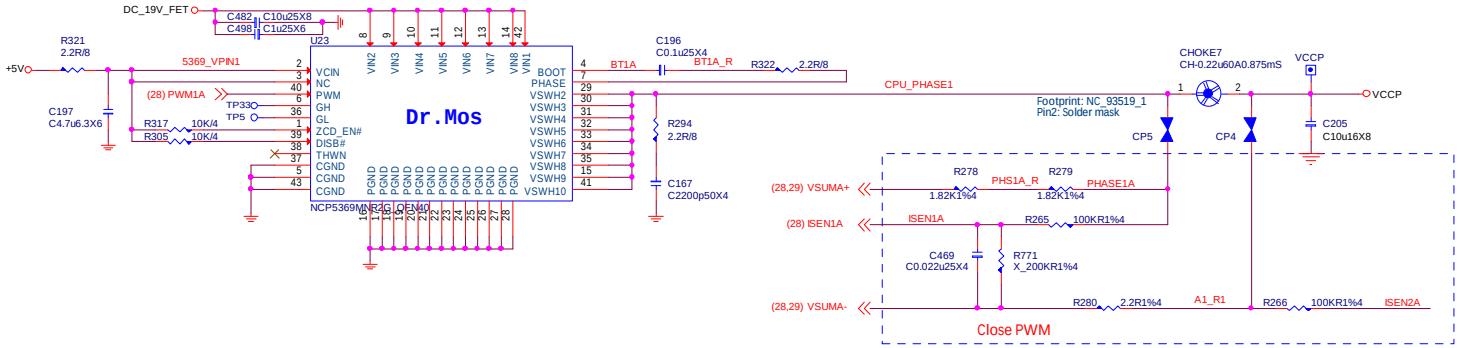
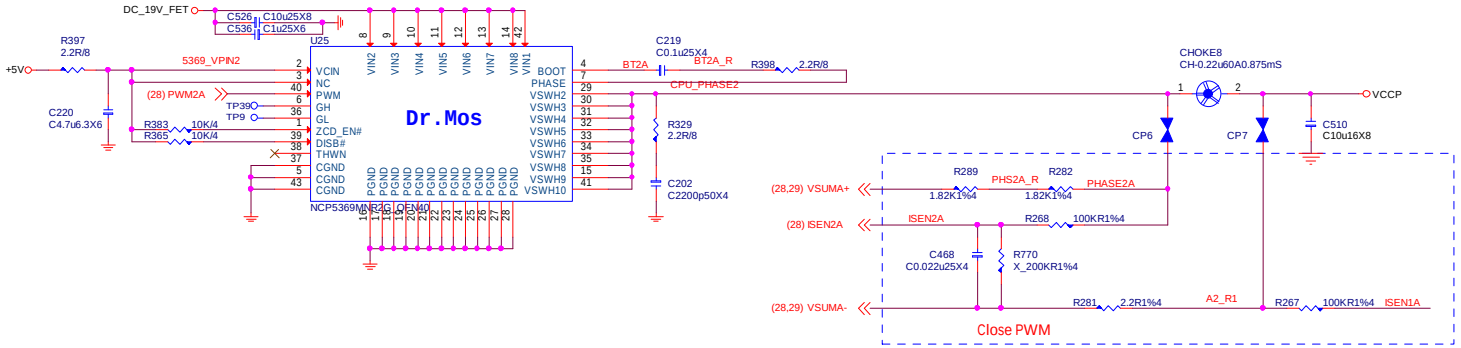
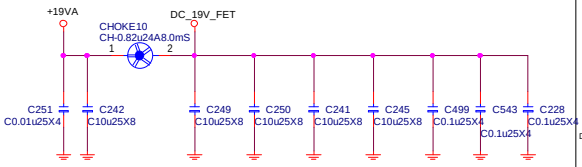
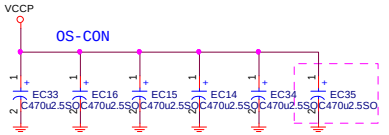
VCCP

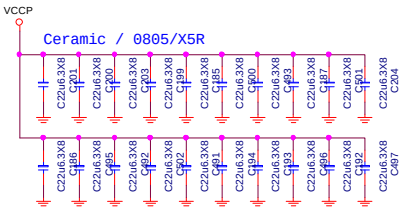
0.55V~1.52V output range
TDC=45A
EDC=66A





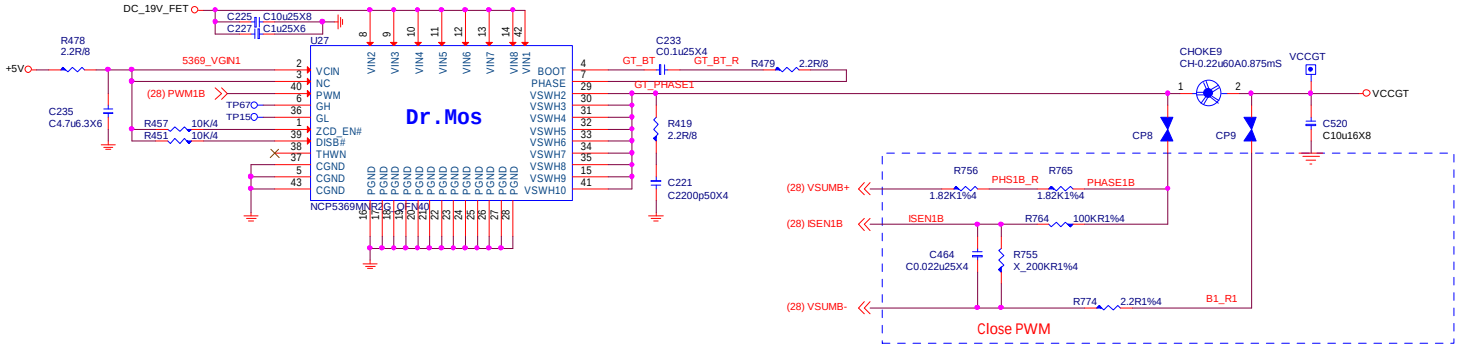


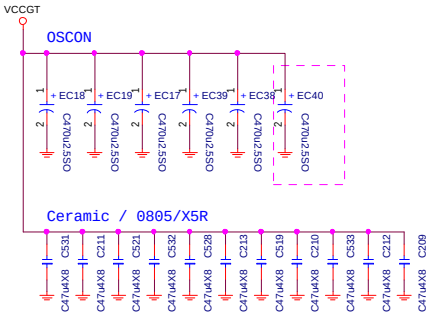




VCCGT

0.55V~1.5V output range
TDC=25A
EDC=35A





ADVANTECH

Title	VCORE&VCCGT	
Size	Document Number: DMS-SA30	Rev: 1.2
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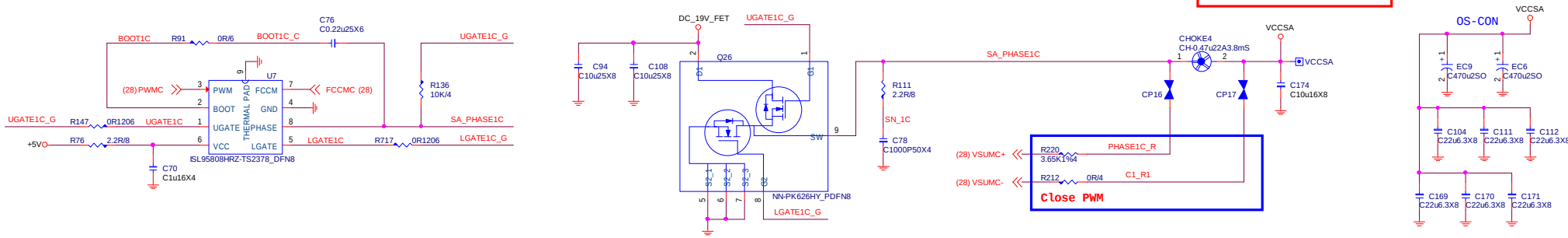
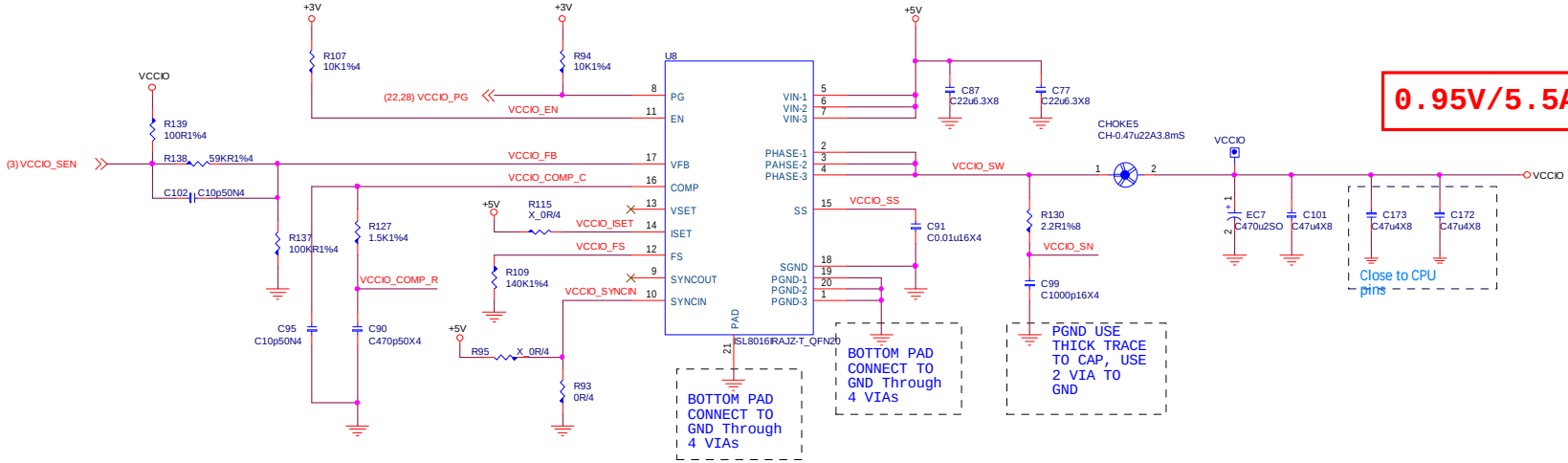
VCCSA

1.05V/11.1A



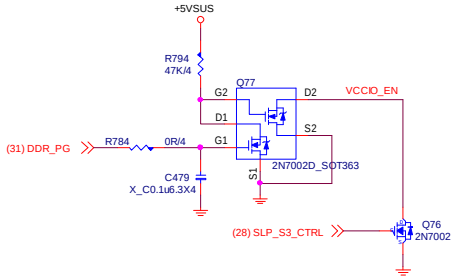
VCCIO

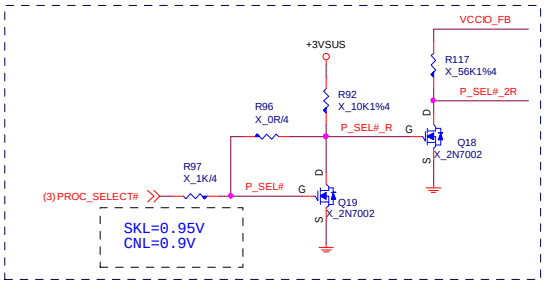
0.95V/5.5A



VCCIO_EN Sequence Control

DDR_PG & SLP_S3#





ADVANTECH

Title	VCCSA & VCCIO	
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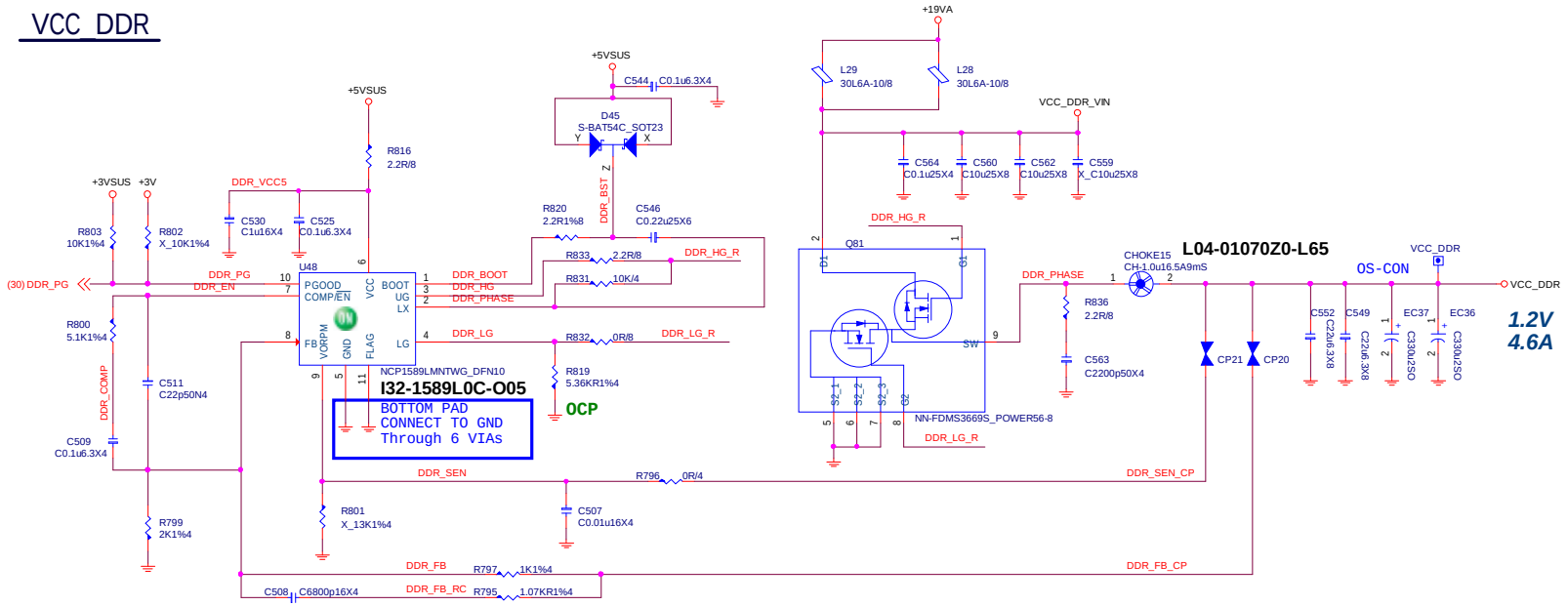
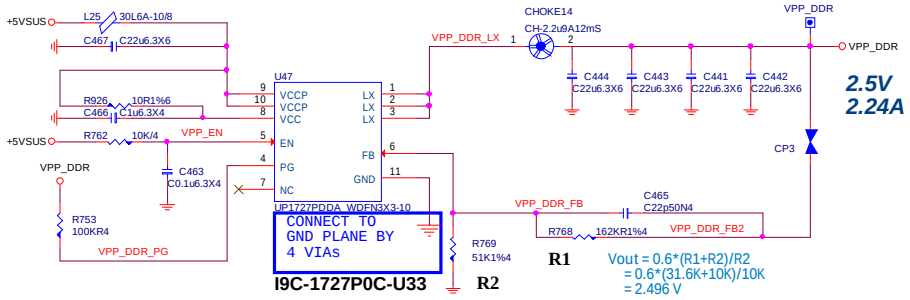
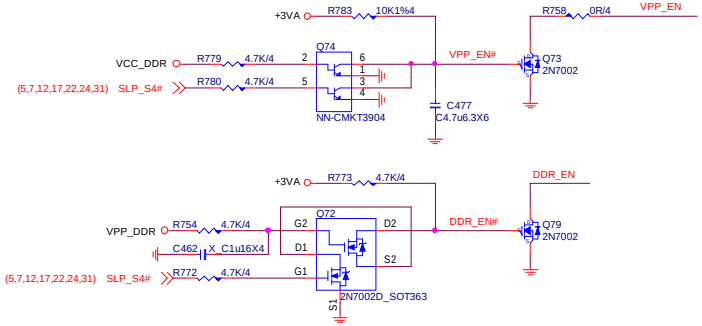
VCC_DDR



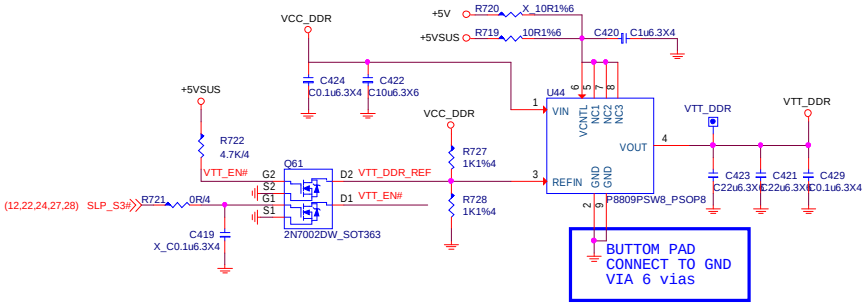
VPP_DDR



VPP_DDR & VCC_DDR Enable Control



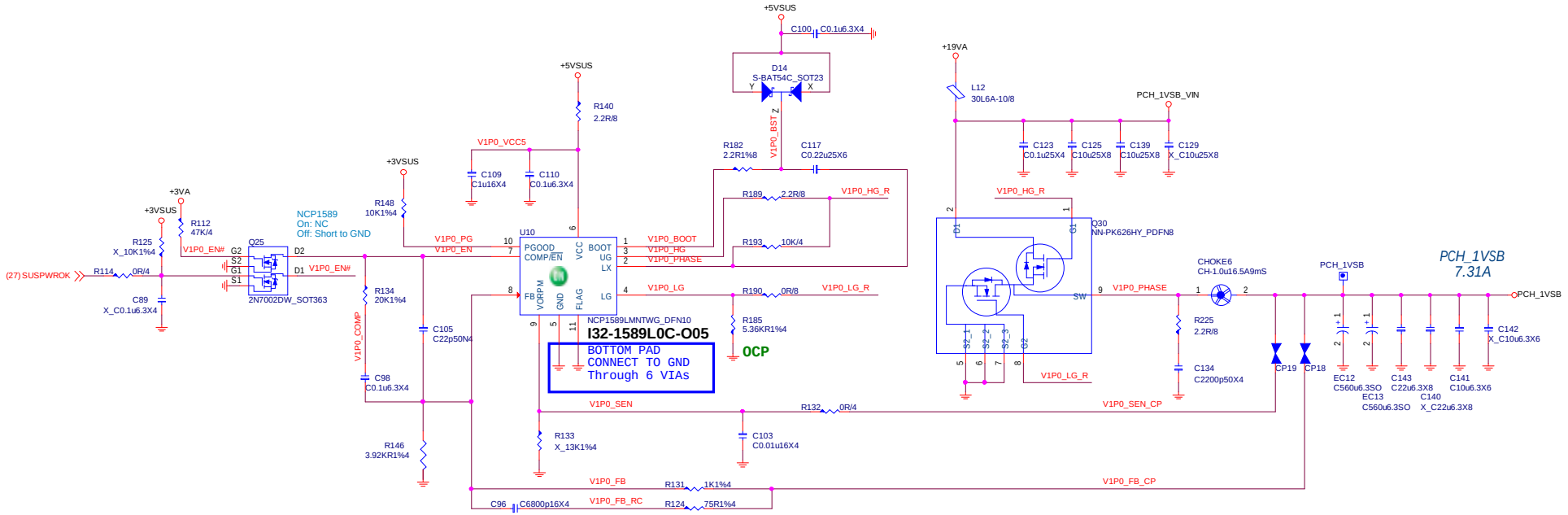
VTT_DDR



ADVANTECH

Title	DDR4 POWER	
Size	Document Number: DMS-SA30	Rev: 1.2
Date: Wednesday, June 14, 2017	Sheet 31 of 35	

PCH_1VSB



ADVANTECH		
Title: PCH Power-PCH_1VSB		
Size	Document Number: DMS-SA30	Rev: 1.2
Date: Wednesday, June 14, 2017	Sheet 32 of 35	

CPU Socket

ILM+BP

CPU_LM1

CPU_LM1
E21-AC71010-L06

CPU_BP1

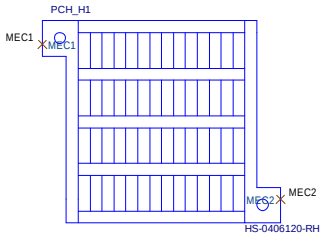
CPU_BP1
E93-0000089-H06

PCB

PCB1

7B01-11
P30-07B0111-E48

PCH Heatsink



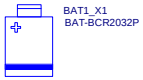
SPI ROM

BIOS1 is a 60-level option part.
<Reserve it if stuff SPI-ROM socket on U29>

BIOS Label

AMI-UEFI_BIOS-LABEL
G51-M1SPXXA-A09

Battery



Option Parts

PCH Option

PCH_Q170

X_SKL-Q170
B01-0Q17025-I06

PCH_H110

X_SKL-H110
B01-0H11005-I06

LAN Chip Option

LAN_LM

X_I219LM
B06-0I2191C-I06

LAN_V

X_I219V
B06-0I2190C-I06

COM_USB1 Option

COMUSB_Q

X_RJ45/USB3.0
N58-26F0031-S42

COMUSB_H

X_RJ45/USB2.0
N58-16F0291-S42

SPI ROM Option

BIOS_Q

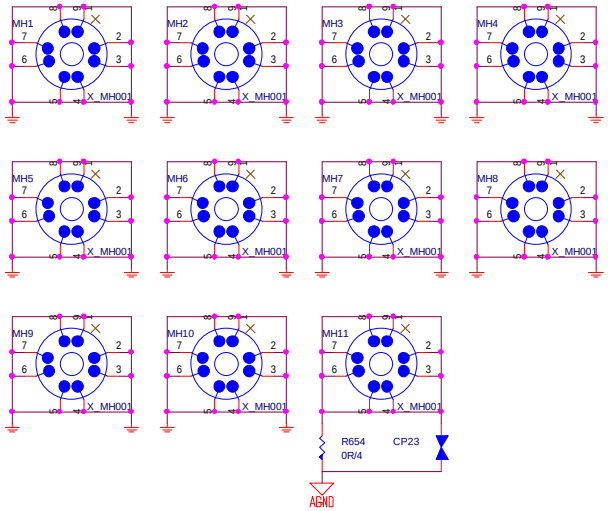
X_MX25L12873FM2I-10G
M31-2512832-M24

BIOS_H

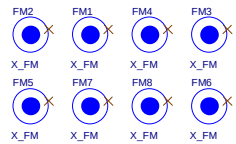
X_W25Q64JVSSIQ
M31-25Q64A3-W03

BIOS 8M (H110) : M31-25Q6443-W03
BIOS 16M (H170/Q170) :
M31-2512832-M24 & M31-2512893-W03

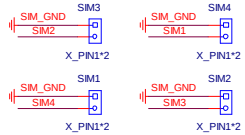
Mounting Holes



Optical Fiducial Marks-120

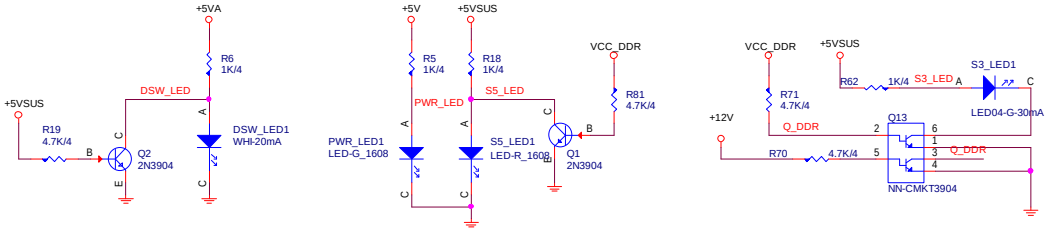


Simulation



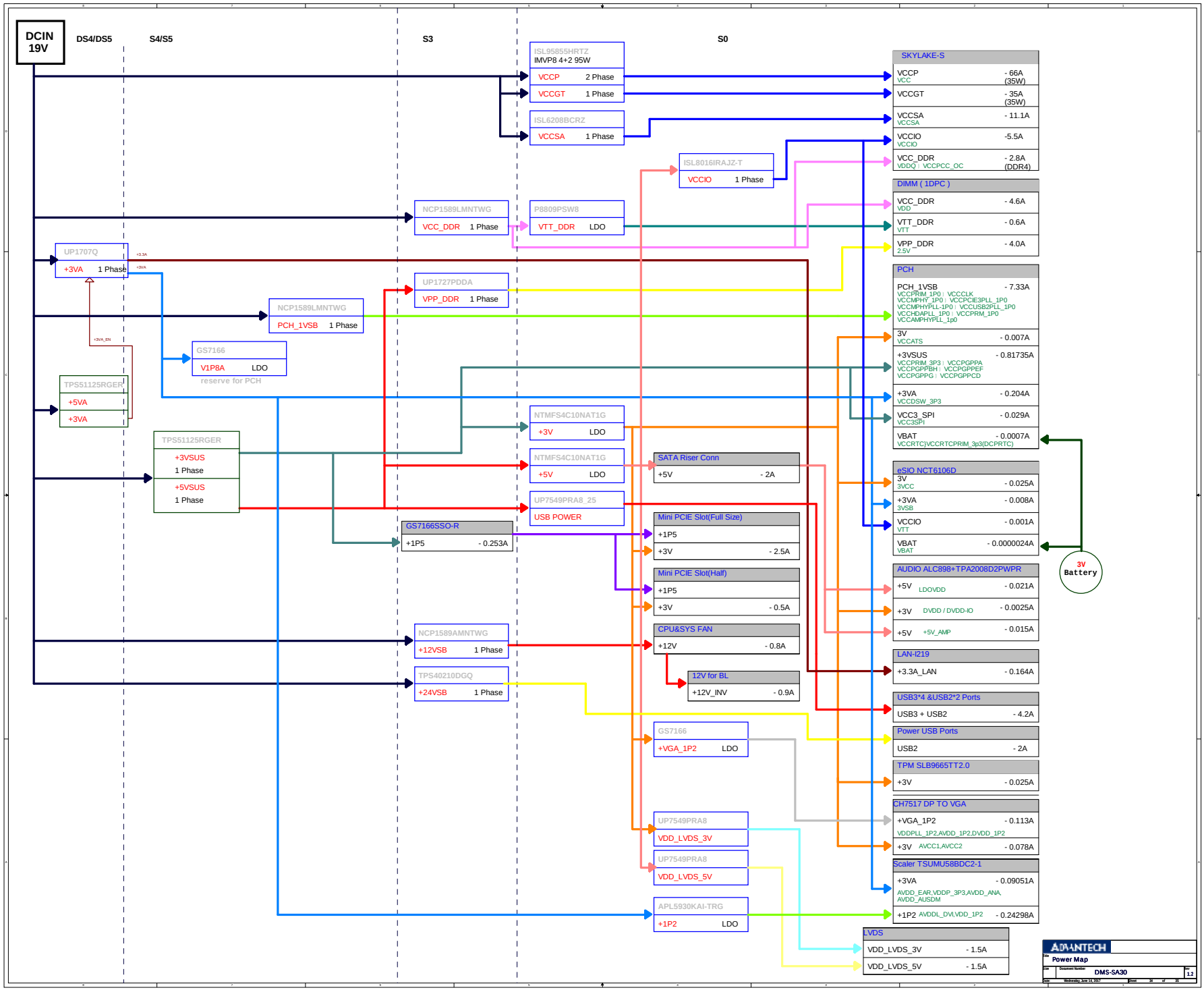
Power status LEDs

<Debug only, remove it before MP>



ADVANTECH

Title: Manual Parts		
Size	Document Number: DMS-SA30	Rev: 1.2
Date: Wednesday, June 14, 2017	Sheet 33 of 35	


DCIN 19V
DS4/DS5
S4/S5
S3
S0
ISL95855HRTZ
IMVP8 4+2 95W
VCCP 2 Phase
VCCGT 1 Phase
ISL6208BCRZ
VCCSA 1 Phase
ISL8016IRAJZ-T
VCCIO 1 Phase
NCP1589LMNTWG
VCC_DDR 1 Phase
P8809PSW8
VTT_DDR LDO
UP1707Q
+3VA 1 Phase
UP1727PDDA
VPP_DDR 1 Phase
NCP1589LMNTWG
PCH_1VSB 1 Phase
GS7166
V1P8A LDO
reserve for PCH
TPS51125RGER
+5VA
+3VA
TPS51125RGER
+3VSUS
1 Phase
+5VSUS
1 Phase
NTMFS4C10NAT1G
+3V LDO
NTMFS4C10NAT1G
+5V LDO
UP7549PRA8_25
USB POWER
GS7166SSO-R
+1P5 - 0.253A
NCP1589AMNTWG
+12VSB 1 Phase
TPS40210DGQ
+24VSB 1 Phase
GS7166
+VGA_1P2 LDO
UP7549PRA8
VDD_LVDS_3V
UP7549PRA8
VDD_LVDS_5V
APL5930KAI-TRG
+1P2 LDO
SATA Riser Conn
+5V - 2A
Mini PCIE Slot(Full Size)
+1P5
+3V - 2.5A
Mini PCIE Slot(Half)
+1P5
+3V - 0.5A
CPU&SYS FAN
+12V - 0.8A
12V for BL
+12V_INV - 0.9A
SKYLAKE-S
VCCP - 66A (35W)
VCC
VCCGT - 35A (35W)
VCCSA - 11.1A
VCCSA
VCCIO -5.5A
VCCIO
VCC_DDR - 2.8A (DDR4)
VDDQ VCCPCC_OC
DIMM (1DPC)
VCC_DDR - 4.6A
VDD
VTT_DDR - 0.6A
VTT
VPP_DDR - 4.0A
2.5V
PCH
PCH_1VSB - 7.33A
VCCPRIM_1P0 VCCCLK
VCCMPHY_1P0 VCCPCIE3PLL_1P0
VCCMPHYPLL-1P0 VCCUSB2PLL_1P0
VCCHDAPLL_1P0 VCCPRM_1P0
VCCAMPHYPLL_1p0
3V - 0.007A
VCCATS
+3VSUS - 0.81735A
VCCPRIM_3P3 VCCPGPPA
VCCPGPPBH VCCPGPPEF
VCCPGPPG VCCPGPPCD
+3VA - 0.204A
VCCDSW_3P3
VCC3_SPI - 0.029A
VCC3SPI
VBAT - 0.0007A
VCCRTC)VCCRTCPRIM_3p3(DCPRTC)
eSIO NCT6106D
3V - 0.025A
3VCC
+3VA - 0.008A
3VSB
VCCIO - 0.001A
VTT
VBAT - 0.0000024A
VBAT
3V Battery
AUDIO ALC898+TPA2008D2PWPR
+5V LDOVDD - 0.021A
+3V DVDD / DVDD-IO - 0.0025A
+5V +5V_AMP - 0.015A
LAN-I219
+3.3A_LAN - 0.164A
USB3*4 &USB2*2 Ports
USB3 + USB2 - 4.2A
Power USB Ports
USB2 - 2A
TPM SLB9665TT2.0
+3V - 0.025A
CH7517 DP TO VGA
+VGA_1P2 - 0.113A
VDDPLL_1P2,AVDD_1P2,DVDD_1P2
+3V AVCC1,AVCC2 - 0.078A
Scaler TSUMU58BDC2-1
+3VA - 0.09051A
AVDD_EAR,VDDP_3P3,AVDD_ANA,
AVDD_AUSDM
+1P2 AVDDL_DVI,VDD_1P2 - 0.24298A
LVDS
VDD_LVDS_3V - 1.5A
VDD_LVDS_5V - 1.5A
ADVANTECH
Power Map
DMS-SA30
1.2
Wednesday, June 14, 2017

DMS-SA30 Rev.0A : (161226)
DMS-SA30 Rev.0B : (170313)

Page 3:
* The connection of CH7517 (VGA) change from eDP(Port-A) to DP(Port-B) to prevent some limitation of eDP.
Page 5:
* Reserved SLP_S4_CTL from Q59.D1 for the option of turn on timing of +12VSB&+12V.
Page 9:
* Reserve R925 (RST_GL850#) for GL-850 USB HUB.
* Change/Swap configuration of USB2.0 Port 7~14.
* SATA connection change from SATA2B&3B to SATA0B&1B to same as the display of DMS-SA20's BIOS Setup Manual.
Page 10:
* C195 change from 22P50N4 to 12P50N6 and C189 change from 22P50N4 to 15P50N6 by crystal matching test report.
Page 11:
* Change/Swap configuration of USB2.0 OC#3~7.
* No stuff the pull up resister R391 of PCH_RI# because this function change to SIO by BIOS request.
Page 12:
* C236&C237 change from 12P50N6 to 18P50N6 by crystal matching test report.
* R54 change from 78.7K1%4 to 45.3K1%4 to same as CRB design.
Page 15:
* Y1 change from 14.318M20P(D04-0103000-F07) to 14.318M12P(D04-0103700-F07) by crystal matching test report.
* No stuff D9 and stuff R129 to solve noise from BKL_VBR.(170322)
Page 16:
* C392 change from 10uf6.3X6 to 47u6.3X8 for the inrrush current of +5VDD_LVDS.
* C16&C392 stuff 1KR4 to discharge *VDD_LVDS under G3.(170322)
Page 17:
* Add R907~R911 for the gates of Q66~Q70 to prevent gate floating problem.
* Add U55 (GL850 USB2.0 HUB) and related components for H110 Sku.
* Remove RN10~13 ; Add R935~942 for Q170 Sku.
Page 18:
* The connection of CH7517 (VGA) change from eDP (Port-A) to DP (Port-B) to prevent some limitation of eDP.
* F/W version of CH7517 change from 3.1.0.7 (B07-7517A1C-C25) to B000.05.01.13 (B07-7517A4C-C25).
* C299&C298 change from 18P50N4 to 15P50N6 by crystal matching test report.
* Swap D32&D50's connection by layout requst.
* L16~L18 change from 82nf300mA to 16nf500mA ; C354/C342/C351/C359/C344/C358 change from 10pf50N4 to 1.5pf50N4 for R/F time and Over/Under shoot adjustment.
Page 19:
* LAN_USB1 change footprint from IOA_RJ45_USB2_LED2_32_1 to IOA_RJ45_USB2_LED2_32.
* C589&C593 change from 22P50N4 to 30P50N6 by crystal matching test report.
* Reserve D52&D53(ESD diode) by EMI request.
Page 20:
* C325&C312 change from 1u16X4 to 0.1u16X4 because Ci must be 10 times smaller than C-Bypass, the value range of C-Bypass is 0.47uf to 1uf.
* C607 change from 1u16X4(X5R) to 1u25X6(X7R) for low-ESR requirement of BYPASS(pin22).
* Change the power source of L36(LDOVDD) from +5V to +5VSUS for S3 wake up noise issue.
* Reserve L41 to add a power source from +5VSUS for +5V_AMP.
Page 21:
* No stuff R10(SERIRQ) because not support TPM card for JTPM1.
Page 22:
* Reserve a connection(SIO_RI#) between U26.45(GP45) and Q83.D by BIOS request.
* Modify Hardware Monitor(Voltage Sense) of +12V change to +19VA and R368 change from 110K1%4 to 180K1%4.
* No stuff Y3&C246 because it only for defensive design.(170322)
Page 23
* C567&C570 change from 0.1u6.3X4 to 0.047u10X4 ; C568&C588&C587&C571&C591&C592 change from 0.1u6.3X4 to 0.33u6.3X4 to meet the requirement of MAX3243 datasheet.
* Reserve R943&R944 for the signal of RI# by BIOS request.
* Add Q100 and R947 to change the connection from PCH_GPIO to PCH_WAKE# by BIOS request.
Page 24:
* R593 change from 0.01R1%XTRA to 0.02R1%1206 for OCP adjustment.
* FS4 change from RUEF300K to SMD2920P200-24 for safety.
Page 25:
* FS3 change from FUSE-4A to RLD30P300 to same as EXP BD.
Page 26:
* Remove R650 because without current sense feature.
* Reserved R650 (SLP_S4_CTL) for the option of turn on timing of +12VSB&+12V.
* EC22 change from 220uf/16V/Solid DIP (C71-2211610-N07) to 100uf/16V/Solid SMD (C71-1011680-N07) for ME limitation.
* EC21 change from 100uf/16V/EL_DIP (C94-1011621-N07) to 100uf/16V/Solid SMD (C71-1011680-N07) for ME limitation.
* C274 change from 0.047uf10X4 to 0.1uf25X4 & C266 stuff 470pf50X4 & R559 stuff 75R1%4 12V_COMP&FB.
Page 27:
* R51 change from 30K1% to 620K1% to solve +3VA&+5VA abnormal turn on issue.
* The pulled-up PWR source of SUS_ON# change from +3VA to +19VA and
  R77 change from 10K1% to 140K1% and
  R69 change from 100K1% to 30K1% to solve +3VSUS&+5VSUS abnormal turn on issue.
Page 28:
* No stuff C475 and C470 change from 0.1uf16X4 to 0.22uf25X6 for ISUM_A.
* C152 change from 0.012uf16X4 to 0.01uf16X4 for ISUM_B.
* R224 change from 93.1KR1% to 88.7KR1% for I-mon.
* R242 change from 1.54K1% to 715R1% to adjust OCP=19A.
* C137 change from 2200pf50X4 to 2700pf50X4 and R245 change from 2.4KR1% to 2.1KR1% for FB_B.
Page 31:
* R800 change from 20KR1% to 5.1KR1% for DDR_COMP.
* Add R926 (10R1%6) and modify circuit to same as the demo circuit of UP1727 (U47)'s datasheet.
Page 33:
* PCB1 change from Rev.0A(P30-07B010A-E48) to Rev.0B(P30-07B010B-E48).
* Remove R651 and change it to CP23(copper) by process request.

Others:
* D20&D37&D38&D42&D43 change from D0G-2950500-SI0 to D0G-2710510-I05 by purchase request.
* C190&C216&C464&C468&C469 change from 0.22uf16X4 (C11-2232022-W08) to 0.22uf25X4 (C11-2232022-W08) by purchase request.
* C146 change from 2700pf25X4 (C11-2722022-W08) to 2700pf50X4 (C11-2722822-W08/C11-2722012-S02) by purchase request.
* BIOS_X3 change from W25Q64FVSSIQ (M31-25Q6443-W03) to W25Q64JVSSIQ (M31-25Q64A3-W03) by purchase request.
* All of the net name of PWR_SRC change to +19VA.

DMS-SA30 Rev.10 : (170331)

Page 6:
* Stuff R143&R144&R145 by schematic checklist of XDP.
Page 10:
* DDPC_CTRLDATE pull up to +3V through R949(2.2KR4) to enable DDI Port- B and reserve TP71.
* Add R950 to disable DDI Port-A(eDP).
* R509 change from 10KR4 to 100KR4 for DDPD_HPD3.
Page 12
* No stuff R551 for TL-624-1.1.
* Add TP72 (PCH_SPI_CS2#) for debug.
Page 16
* Add discharge resistors R951&R952(1KR4) for +3VDD&+5VDD_LVDS power plane.
* C16&C392 stuff 0.1uf6.3X4.
Page 22:
* No stuff R330 because no SMI# requirement.
Page 23:
* No stuff R947/R854/R846/D47/Q83/Q100 because no need support WOR function. (170410)
Page 29:
* PWRJ1 change from N92-03F0071-F02 to N92-04F0041-S56 by customer request. (170410)
Page 33:
* PCB1 change from Rev.0B(P30-07B010B-E48) to Rev.10(P30-07B0110-E48).

DMS-SA30 Rev.11 : (170508)

Page 10:
* No stuff R513/R411/R498/R826/R437/R507/R516/R464/R485/R454/R442/R465/R500 because un-used related SRCCLK signals.
Page 12:
No stuff SPI-ROM socket on U29 and mount SPI-ROM on U29 directly.
Page 15&17:
* Add a connection (TOUCH_THRU#) from U6.39 to OSD1.30 ; Add Q101/R957/R958/R962 and related circuit by customer request.
Page 18:
* No stuff C622 & C623 to solve the glitch of H/VSYNC between 0.5V~2V.
Page 18&23:
* DSUB1 change from N58-24F0251-F02(with screw) to "N59-24M0031-H06"(W/O screw) by customer request.
Page 22:
* No stuff PWRBTN1 because it reserve for debug only.
Page 24:
* Add U56 (TUSB211RWBR) and related components by customer request.
* No stuff Q96/EC30/C616/C615/C355/R631/R872/Q87/C620 if W/O FS6.
* D48 change from S-PDS560-13(D01-PDS5600-D07) to PMEG060V100EPD(D01-60V100-N78) by purchase request.
Page 27:
* No stuff Q24, it cause Drain Current issue because gate floating.
* Q23 change from 2N7002 to N-3904 ; R105 change from 470KR1% to 140KR1% ; R103 change from 47KR4 to 27KR1% ; R102 change from 178KR1% to 100KR1% and no stuff C82 and R104 for S5 to G3 turn-off timing adjustment.
Page 33:
* R6 change from 680R0603 to 1KR0402 for power saving under DS mode.
* PCB change from Rev.10 to Rev.11.

DMS-SA30 Rev.12 : (170616)

Page 3:
* No stuff R251 because no DP port attached to eDP.
Page 11:
* Add CDW_GPI2(GPP_G7) and pull-up it through R967(10KR) for cash drawer by customer request.
Page 12:
* Add L42/C651/C652/Q102/R964/R965/R966/D55/C650 for CDW_GPI2 by customer request.
Page 19:
* CHOKE11 change from L04-47A7210-T36(4.7u1.14A72mS) to L04-47A71B0-L65(4.7u1.14A60mS) by purchase request.
Page 22:
* Stuff PWRBTN1 by QA team request.

ADVANTECH

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