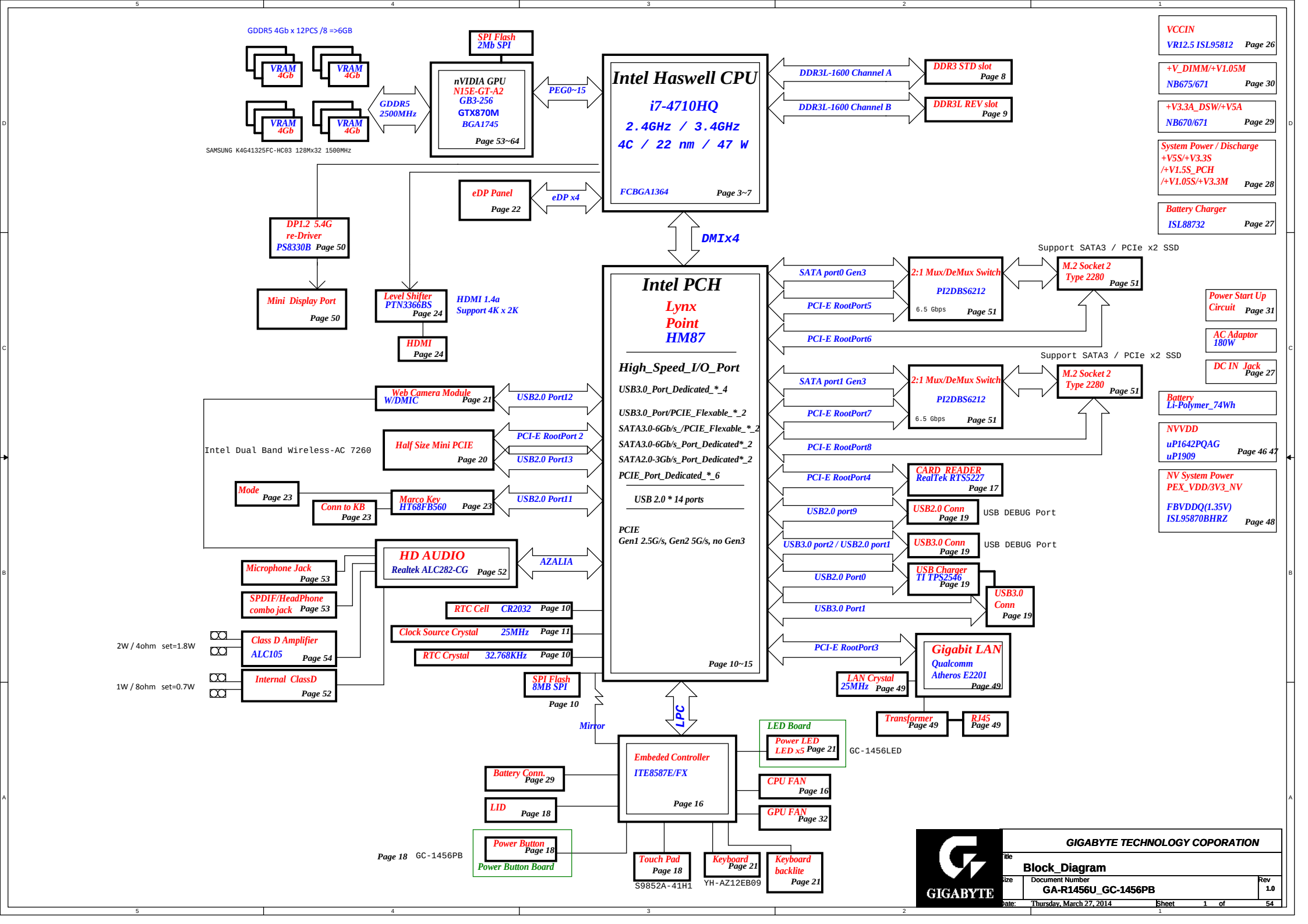
Technical Information Release Notice

單據編號	Ans000002769232				
Doc Type	Schematic		Date	2014/03/26	
Project Code	R13010-0		Customer	N/A	
Project Name	R1456		Revision	old：N/A	
Model Name	GC-1456PB;GA-R1456U;			new：1.0	
P/N			IT Doc No	DR143015	
PCB Rev.	1.0		Check Sum	N/A	
P/N Description			Effected Class	○R ●N ○M	
				●A ○B ○C ○D ○E ○F	
				○A ●B	
Description	GC-1456PB and GA-R1456U 1.0 schematic first release.				
Remark	GC-1456PB and GA-R1456U 1.0 schematic first release.				
Approved By	969033 /林意能	2014/03/26 18:47:25	Applicant	TA110235 /謝勵志	2014/03/26 18:24:24
Research Management	975003 /金志潔	Validation Manager	/	Project Manager	/
	2014/03/27 13:40:25				

Emily.Chin **3/27/2014**


GDDR5 4Gb x 12PCS /8 =>6GB
VRAM 4Gb
VRAM 4Gb
VRAM 4Gb
VRAM 4Gb
SAMSUNG K4G41325FC-HC03 128Mx32 1500MHz
GDDR5 2500MHz
SPI Flash 2Mb SPI
nVIDIA GPU N15E-GT-A2 GB3-256 GTX870M BGA1745 Page 53~64
PEG0~15
Intel Haswell CPU
i7-4710HQ
2.4GHz / 3.4GHz
4C / 22 nm / 47 W
FCBGA1364 Page 3~7
DDR3L-1600 Channel A
DDR3L-1600 Channel B
DDR3 STD slot Page 8
DDR3L REV slot Page 9
eDP Panel Page 22
eDP x4
DP1.2 5.4G re-Driver PS8330B Page 50
Mini Display Port Page 50
Level Shifter PTN3366BS Page 24
HDMI 1.4a Support 4K x 2K
HDMI Page 24
DMIx4
Intel PCH
Lynx Point HM87
High_Speed_I/O_Port
USB3.0_Port_Dedicated_*_4
USB3.0_Port/PCIE_Flexable_*_2
SATA3.0-6Gb/s_/PCIE_Flexable_*_2
SATA3.0-6Gb/s_Port_Dedicated*_2
SATA2.0-3Gb/s_Port_Dedicated*_2
PCIE_Port_Dedicated_*_6
USB 2.0 * 14 ports
PCIE
Gen1 2.5G/s, Gen2 5G/s, no Gen3
Page 10~15
Support SATA3 / PCIe x2 SSD
SATA port0 Gen3
PCI-E RootPort5
PCI-E RootPort6
2:1 Mux/DeMux Switch PI2DBS6212 6.5 Gbps Page 51
M.2 Socket 2 Type 2280 Page 51
Support SATA3 / PCIe x2 SSD
SATA port1 Gen3
PCI-E RootPort7
PCI-E RootPort8
2:1 Mux/DeMux Switch PI2DBS6212 6.5 Gbps Page 51
M.2 Socket 2 Type 2280 Page 51
Web Camera Module W/DMIC Page 21
USB2.0 Port12
Intel Dual Band Wireless-AC 7260
Half Size Mini PCIE Page 20
PCI-E RootPort 2
USB2.0 Port13
Mode Page 23
Conn to KB Page 23
Marco Key HT68FB560 Page 23
USB2.0 Port11
PCI-E RootPort4
CARD_READER RealTek RTS5227 Page 17
USB2.0 port9
USB2.0 Conn Page 19
USB DEBUG Port
USB3.0 port2 / USB2.0 port1
USB3.0 Conn Page 19
USB DEBUG Port
USB2.0 Port0
USB Charger TI TPS2546 Page 19
USB3.0 Port1
USB3.0 Conn Page 19
HD AUDIO Realtek ALC282-CG Page 52
AZALIA
Microphone Jack Page 53
SPDIF/HeadPhone combo jack Page 53
RTC Cell CR2032 Page 10
Clock Source Crystal 25MHz Page 11
RTC Crystal 32.768KHz Page 10
SPI Flash 8MB SPI Page 10
PCI-E RootPort3
Gigabit LAN Qualcomm Atheros E2201 Page 49
LAN Crystal 25MHz Page 49
Transformer Page 49
RJ45 Page 49
2W / 4ohm set=1.8W
Class D Amplifier ALC105 Page 54
1W / 8ohm set=0.7W
Internal ClassD Page 52
LPC
Mirror
LED Board
Power LED LED x5 Page 21
GC-1456LED
Embeded Controller ITE8587E/FX Page 16
Battery Conn. Page 29
LID Page 18
CPU FAN Page 16
GPU FAN Page 32
Power Button Page 18
Power Button Board
Page 18 GC-1456PB
Touch Pad Page 18
S9852A-41H1
Keyboard Page 21
YH-AZ12EB09
Keyboard backlite Page 21
VCCIN VR12.5 ISL95812 Page 26
+V_DIMM/+V1.05M NB675/671 Page 30
+V3.3A_DSW/+V5A NB670/671 Page 29
System Power / Discharge +V5S/+V3.3S /+V1.5S_PCH /+V1.05S/+V3.3M Page 28
Battery Charger ISL88732 Page 27
Power Start Up Circuit Page 31
AC Adaptor 180W
DC IN Jack Page 27
Battery Li-Polymer_74Wh
NVVDD uP1642PQAG uP1909 Page 46 47
NV System Power PEX_VDD/3V3_NV FBVDDQ(1.35V) ISL95870BHRZ Page 48
GIGABYTE TECHNOLOGY COPORATION
Title Block_Diagram
Size
Document Number GA-R1456U_GC-1456PB
Rev 1.0
Date: Thursday, March 27, 2014
Sheet 1 of 54

Circuit or PCB layout change Note

Rev.	Page	Change Item	Reason	Layout
0.2	13	Add eDP X2 X4 select function (GPIO68)		
0.2	16	Add GPU FAN PWM & TACH Add +V1.35 voltage control GPIO. Add ALC282 PD signal to GPI1		
0.2	21	Add 0805 0 ohm (R460) for KB_BK adjust		
0.2	21	Change C2353 footprint from 0805 to B2		
0.2	24	Add DDPB_CTRLDATA DDPB_CTRLDATA pull up resistor (HDR3 HDR5)		
0.2	30	Change +V_DIMM & +V1.05M choke form 7A to 11A.		
0.2	44	Fix 3V3_MAIN & 3V3_AON net short		
0.2	45	Add PEX_VDD delay circuit.		
0.2	48	Add 3V3_MAIN discharg circuit.		
0.2	48	Add 1x 4935N for FBVDDQ low side.		
0.2	49	Modify LAX1 footprint		
0.2	50	Fix mDP circuit error		
0.2	51	Swap SATA RX signal		
0.2	53	Fix SPDIF_IN- connect mistake.		
0.3	48	change Csen cap vale from 8.2nF to 33nF. footprint from 0402 to 0602.		
0.3	13 48	Modify GPU power discharg circuit.		
0.3	27	change CHR1 from 10m/1206 to 10m/2512		
0.3	27	Remove CHC4 CHQ2 and CHQ9 for layout space.		
0.3	27	Change CHC6 CHc13 footprint from 0402 to 0602. rated voltage from 6.3V to 25V.		
0.3	16	Swap EC GPA2 GPE23.		
0.3	16	Modify CPU prochot circuit.		
0.3	16	Add IVT1 connect for LED driver board.		
0.3	23	Change Marco Key solution from CYPRESS CY7C64215 to Hotek HT68FB560		
0.4	23	Change Marco Key HT68FB560 footprint from IC48QFN to IC48LQFP		
1.0	18	Change power button from MPTCFG-T-Q-T/R to NTC311-EC1T-A220T by ME request.		
1.0	52	Remove reserve component including R446 R447 C375 C376 C378 C377.		

Rev.	Page	Change Item	Reason	Layout

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Title: Change_Note

Size | Document Number: GA-R1456U_GC-1456PB | Rev: 1.0

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PEG_COMP
Width/Spacing/Length
12/15/500 mils

+VCCIOA_OUT

RG17
24.9/4/1

U55A HASWELL_BGA_E

PEG_RXN[15:0] 32
PEG_RXP[15:0] 32
PEG_TXN[15:0] 32
PEG_TXP[15:0] 32

12 DMI_TXN[3:0]
DMI_TXN0 AB2
DMI_TXN1 AB3
DMI_TXN2 AC3
DMI_TXN3 AC1

12 DMI_TXP[3:0]
DMI_TXP0 AB1
DMI_TXP1 AB4
DMI_TXP2 AC4
DMI_TXP3 AC2

12 DMI_RXN[3:0]
DMI_RXN0 AF2
DMI_RXN1 AF4
DMI_RXN2 AG4
DMI_RXN3 AG2

12 DMI_RXP[3:0]
DMI_RXP0 AF1
DMI_RXP1 AF3
DMI_RXP2 AG3
DMI_RXP3 AG1

DMI_RXN0 DMI_RXN1 DMI_RXN2 DMI_RXN3
DMI_RXP0 DMI_RXP1 DMI_RXP2 DMI_RXP3
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3
DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3

DMI

12 PCH_FDI_CSYNC F11
12 FDI_INT F12
FDI_CSYNC
DISP_INT

FDI

PEG

AH6 PEG_COMP
PEG_RCOMP

E10	PEG_RXN15	C104	0.22u/4/X5R/10V/K	PEG_TXN15
C10	PEG_RXN14	C103	0.22u/4/X5R/10V/K	PEG_TXN14
B10	PEG_RXN13	C113	0.22u/4/X5R/10V/K	PEG_TXN13
E9	PEG_RXN12	C115	0.22u/4/X5R/10V/K	PEG_TXN12
D9	PEG_RXN11	C121	0.22u/4/X5R/10V/K	PEG_TXN11
B9	PEG_RXN10	C128	0.22u/4/X5R/10V/K	PEG_TXN10
L5	PEG_RXN9	C146	0.22u/4/X5R/10V/K	PEG_TXN9
L2	PEG_RXN8	C153	0.22u/4/X5R/10V/K	PEG_TXN8
M4	PEG_RXN7	C159	0.22u/4/X5R/10V/K	PEG_TXN7
L4	PEG_RXN6	C166	0.22u/4/X5R/10V/K	PEG_TXN6
M2	PEG_RXN5	C177	0.22u/4/X5R/10V/K	PEG_TXN5
V5	PEG_RXN4	C180	0.22u/4/X5R/10V/K	PEG_TXN4
V4	PEG_RXN3	C186	0.22u/4/X5R/10V/K	PEG_TXN3
V1	PEG_RXN2	C190	0.22u/4/X5R/10V/K	PEG_TXN2
Y3	PEG_RXN1	C165	0.22u/4/X5R/10V/K	PEG_TXN1
Y2	PEG_RXN0	C179	0.22u/4/X5R/10V/K	PEG_TXN0
F10	PEG_RXP15	C101	0.22u/4/X5R/10V/K	PEG_TXP15
D10	PEG_RXP14	C108	0.22u/4/X5R/10V/K	PEG_TXP14
A10	PEG_RXP13	C110	0.22u/4/X5R/10V/K	PEG_TXP13
F9	PEG_RXP12	C114	0.22u/4/X5R/10V/K	PEG_TXP12
C9	PEG_RXP11	C116	0.22u/4/X5R/10V/K	PEG_TXP11
A9	PEG_RXP10	C125	0.22u/4/X5R/10V/K	PEG_TXP10
M5	PEG_RXP9	C142	0.22u/4/X5R/10V/K	PEG_TXP9
L1	PEG_RXP8	C149	0.22u/4/X5R/10V/K	PEG_TXP8
M3	PEG_RXP7	C154	0.22u/4/X5R/10V/K	PEG_TXP7
L3	PEG_RXP6	C163	0.22u/4/X5R/10V/K	PEG_TXP6
M1	PEG_RXP5	C169	0.22u/4/X5R/10V/K	PEG_TXP5
Y5	PEG_RXP4	C178	0.22u/4/X5R/10V/K	PEG_TXP4
V3	PEG_RXP3	C183	0.22u/4/X5R/10V/K	PEG_TXP3
V2	PEG_RXP2	C187	0.22u/4/X5R/10V/K	PEG_TXP2
Y4	PEG_RXP1	C161	0.22u/4/X5R/10V/K	PEG_TXP1
Y1	PEG_RXP0	C173	0.22u/4/X5R/10V/K	PEG_TXP0

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U55B HASWELL_BGA_E

MISC
C51 PROC_DETECT
G50 CATERR
G51 PECI
16 H_PECI
16,26 H_PROCHOT-
13 PM_THRMTRIP-
R694 56/4
H_PROCHOT- R E50
D53 PROCHOT
THERMTRIP
THERMAL

12 H_PM_SYNC
13 H_CPUPWRGD
R1431 0/4 H_CPUPWRGD_R
VDDPWRGOOD AP48
D52 PM_SYNC
PWRGOOD
SM_DRAMPWROK
13 PCH_PLTRST_CPU
R6 0/4 CPU_RST-
L54 PLTRSTIN
PWR

11 CLK_DP_NONSSC_N
11 CLK_DP_NONSSC_P
11 CLK_DP_SSC_N
11 CLK_DP_SSC_P
11 CLK_EXP_N
11 CLK_EXP_P
CLK_DP_SSC_N
CLK_DP_SSC_P
AC6 DPLL_REF_CLKN
AE6 DPLL_REF_CLKP
V6 SSC_DPLL_REF_CLKN
Y6 SSC_DPLL_REF_CLKP
AB6 BCLKN
AA6 BCLKP
CLOCK

DDR3
SM_RCOMP0 BB51
SM_RCOMP1 BB53
SM_RCOMP2 BB52
SM_DRAMRST BE51
SM_RCOMP_0 RG18 100/4/1
SM_RCOMP_1 RG6 75/4/1
SM_RCOMP_2 RG7 100/4/1
CPUDRAMRST- 4

JTAG
PRDY N53
PREQ N52
TCK N54
TMS M51
TRST M53
TDI N49
TDO M49
DBR F53

BPM#0 R51
BPM#1 R50
BPM#2 P49
BPM#3 N50
BPM#4 R49
BPM#5 P53
BPM#6 U51
BPM#7 P51

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931920/S

Length < 500 mils

DDR3L COMPENSATION SIGNALS

Processor JTAG (TDI, TDO, TMS, TRST#, TCK) signals, PREQ# and PRDY# signals have adequate internal bias resistances to support the removal of the external pull up and pull down on the board when debug is no longer needed.

SSC CLOCK TERMINATION STUFF R & R ONLY WHEN SSC CLOCK NOT USED

+VCCIO_OUT
CLK_DP_SSC_P R1432 10K/4/X
CLK_DP_SSC_N R1433 10K/4/X

R177 10K/4 H_CPUPWRGD_R

+VCCIO_OUT
H_PROCHOT- R695 62/4
C1987
47p/4/NPO/50V/J/X

+V_VDDQS_CPU
VDDPWRGOOD=0.8V-->R753=1.54K,R1696=3.32K
Low Max=0.2025V
Hi Min=0.6075V;Max=1.0V
Shark Bay Mobile Power Sequence Specification:
in S3, the CPU SM_PWRGOOD=Hi

R753 1.54K/4/1
VDDPWRGOOD_D
R765 0/4
VDDPWRGOOD
S0=0.78V
S3=0.78V

+V3.3S
R776 10K/4
Q99
QN7002/SOT23/20pF/2
R5017 3.32K/4/1

VDDPWRGOOD=1.11V-->R753=1.00K,R1696=NA
VDDPWRGOOD=0.98V-->R753=1.82K,R1696=NA
VDDPWRGOOD=0.97V-->R753=2.00K,R1696=NA
VDDPWRGOOD=0.8V-->R753=1.54K,R1696=3.32K
VDDPWRGOOD=0.77V-->R753=1.69K,R1696=3.32K
VDDPWRGOOD=0.76V-->R753=1.74K,R1696=3.32K
VDDPWRGOOD=0.75V-->R753=1.82K,R1696=3.32K
VDDPWRGOOD=0.73V-->R753=2.00K,R1696=3.32K
VDDPWRGOOD=0.60V-->R753=3.09K,R1696=3.32K
Low Max=0.2025V
Hi Min=0.6075V;Max=1.0V

+V3.3A
S0=0V
S3=0V
Q99_G
Q103
S0T23
MMBT2222A/SOT23/600mA/40
R878 10K/4
S0=0.6V
S3=0.6V
Q103_B
Q102_D
PCH output is OpenDrain
R879 10K/4
440ms
240ms
S0=3.3V
S3=3.3V
+V3.3A
Q102
R592 200/4
QN7002/SOT23/20pF/2
12,30 PM_DRAM_PWRGD

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Title: CPU_1-PEG/DMI/JTAG/CLK

Size	Document Number	Rev
	GA-R1456U_GC-1456PB	1.0

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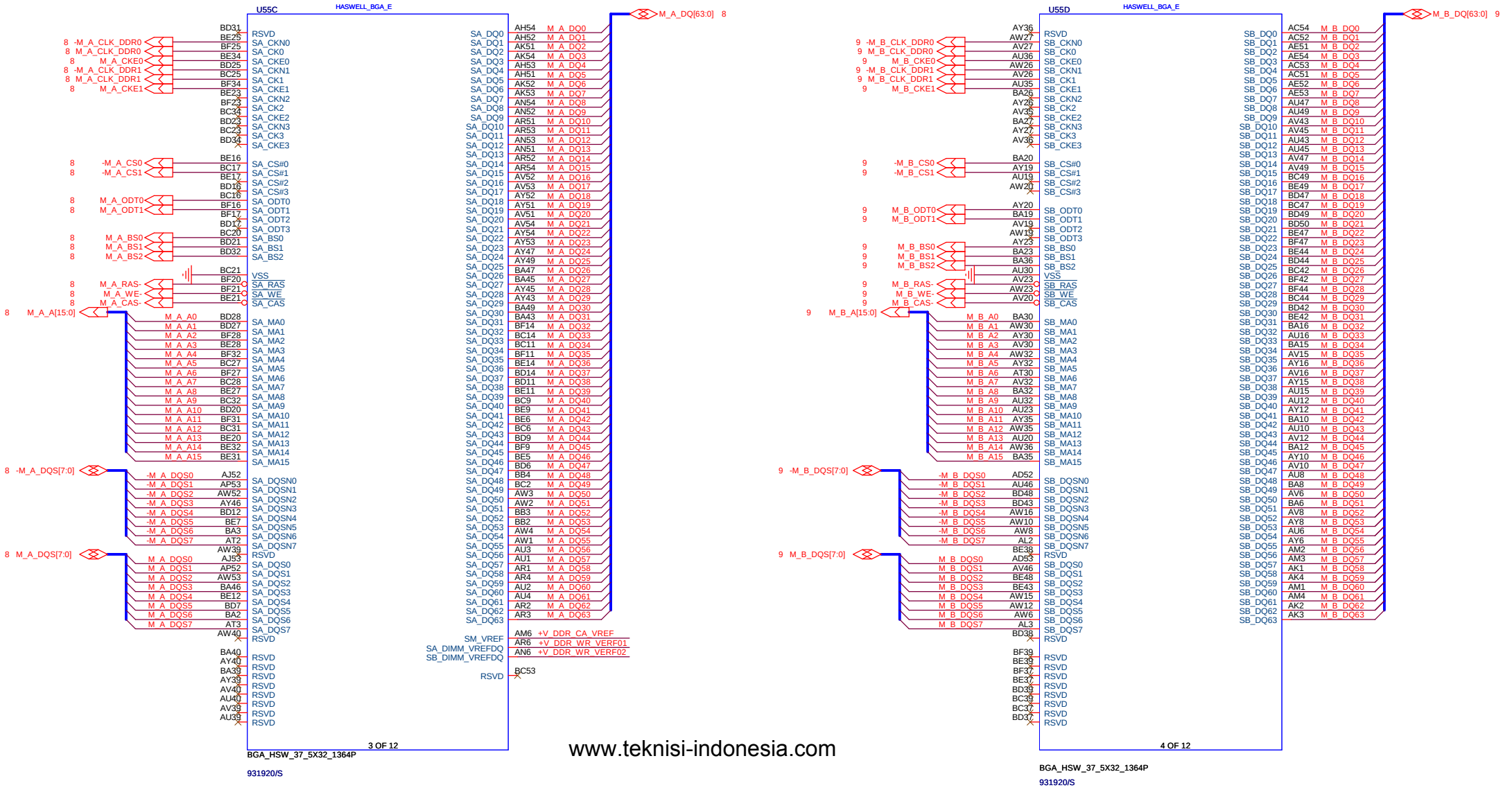

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Title: CPU_2-Memory_Controller

Size | Document Number: GA-R1456U_GC-1456PB | Rev: 1.0

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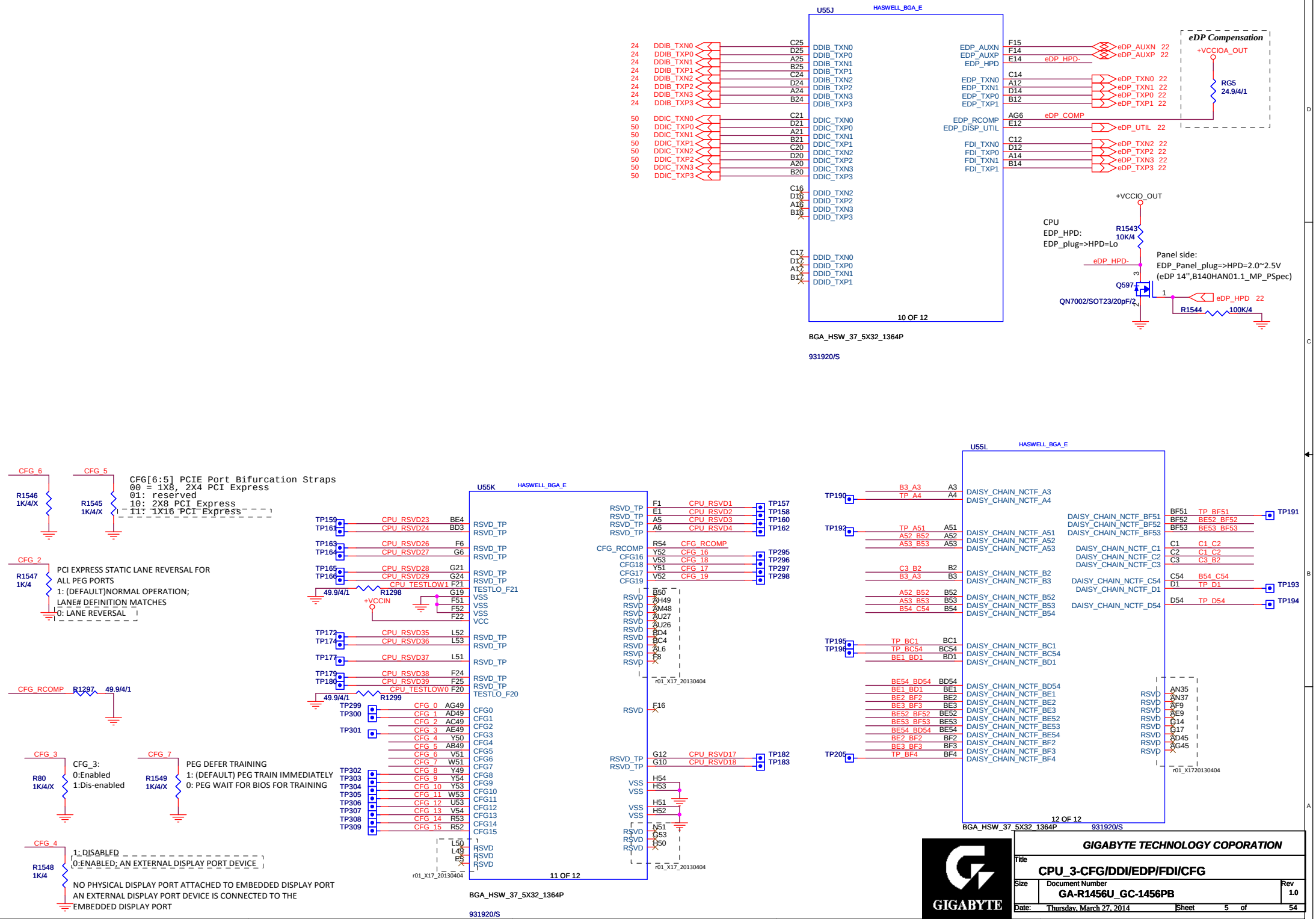
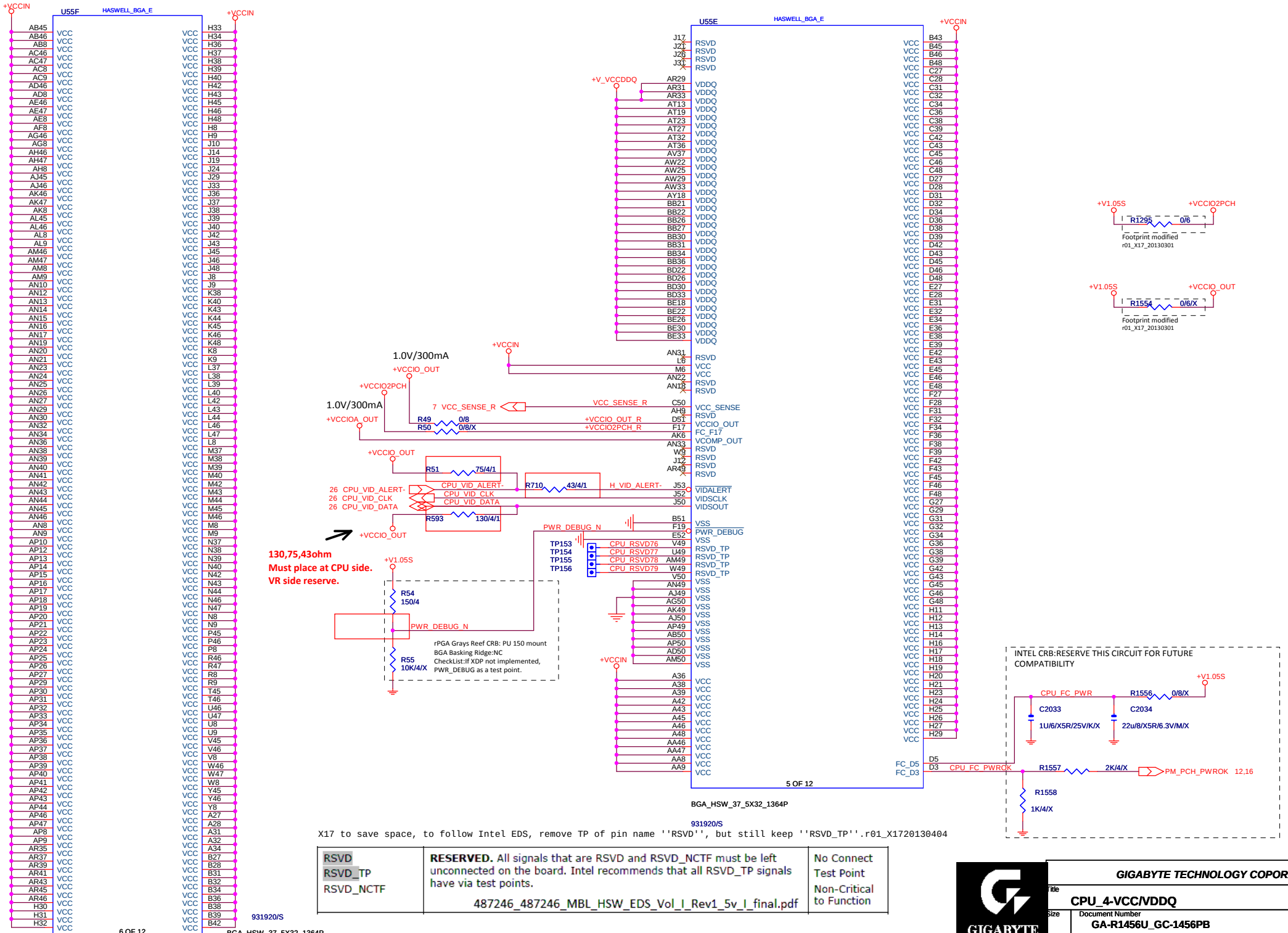
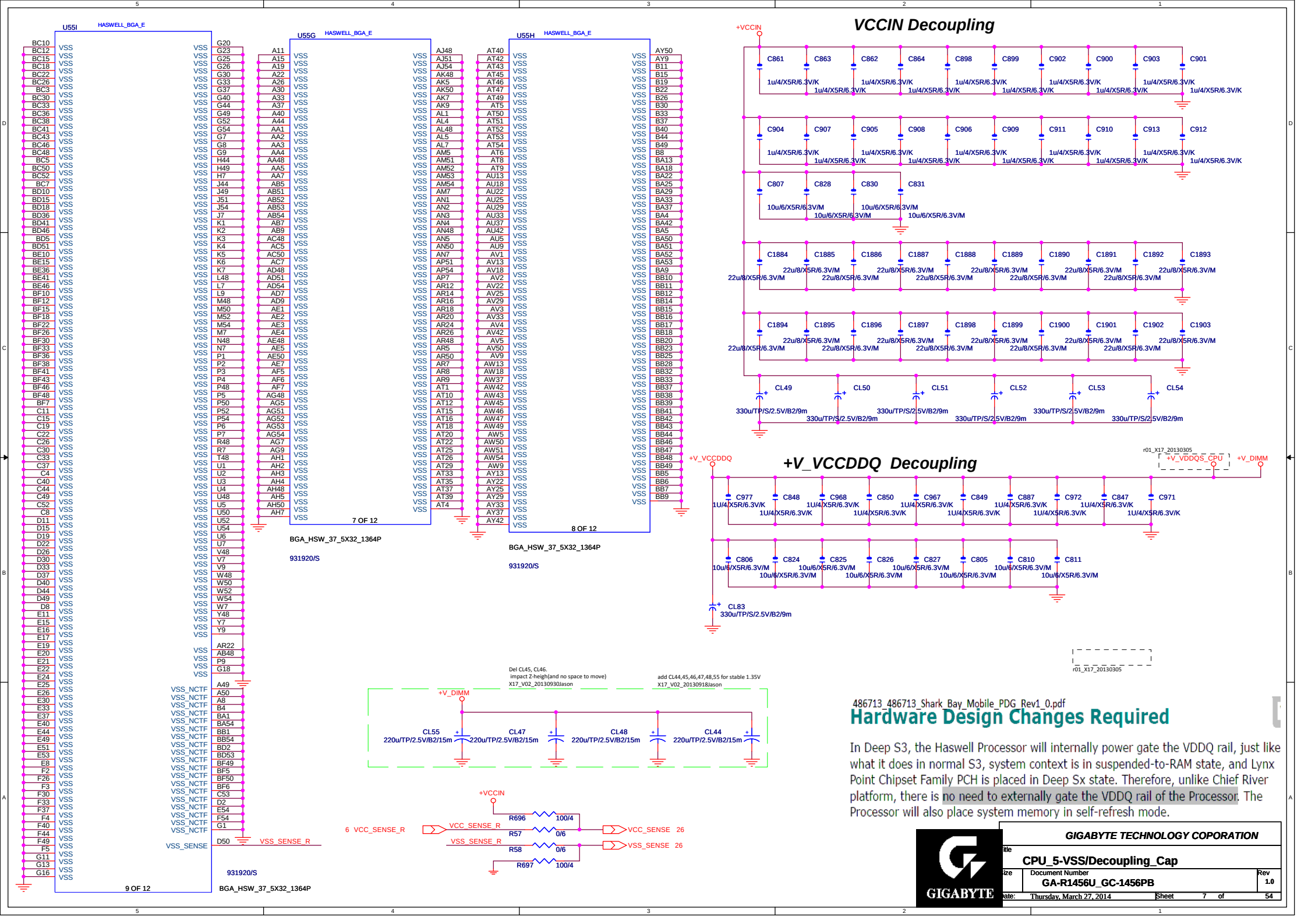

U55J
HASWELL_BGA_E
DDIB_TXN0
DDIB_TXP0
DDIB_TXN1
DDIB_TXP1
DDIB_TXN2
DDIB_TXP2
DDIB_TXN3
DDIB_TXP3
DDIC_TXN0
DDIC_TXP0
DDIC_TXN1
DDIC_TXP1
DDIC_TXN2
DDIC_TXP2
DDIC_TXN3
DDIC_TXP3
DDID_TXN2
DDID_TXP2
DDID_TXN3
DDID_TXP3
DDID_TXN0
DDID_TXP0
DDID_TXN1
DDID_TXP1
EDP_AUXN
EDP_AUXP
EDP_HPD
EDP_TXN0
EDP_TXN1
EDP_TXP0
EDP_TXP1
EDP_RCOMP
EDP_DISP_UTIL
FDI_TXN0
FDI_TXP0
FDI_TXN1
FDI_TXP1
eDP_AUXN 22
eDP_AUXP 22
eDP_HPD-
eDP_TXN0 22
eDP_TXN1 22
eDP_TXP0 22
eDP_TXP1 22
eDP_COMP
eDP_UTIL 22
eDP_TXN2 22
eDP_TXP2 22
eDP_TXN3 22
eDP_TXP3 22
eDP Compensation
+VCCIOA_OUT
RG5
24.9/4/1
10 OF 12
BGA_HSW_37_5X32_1364P
931920/S
+VCCIO_OUT
CPU
EDP_HPD:
EDP_plug=>HPD=Lo
R1543
10K/4
eDP_HPD-
Panel side:
EDP_Panel_plug=>HPD=2.0~2.5V
(eDP 14",B140HAN01.1_MP_PSpec)
Q597
QN7002/SOT23/20pF/2
eDP_HPD 22
R1544
100K/4
CFG_6
CFG_5
R1546
1K/4/X
R1545
1K/4/X
CFG[6:5] PCIE Port Bifurcation Straps
00 = 1X8, 2X4 PCI Express
01: reserved
10: 2X8 PCI Express
11: 1X16 PCI Express
CFG_2
R1547
1K/4
PCI EXPRESS STATIC LANE REVERSAL FOR
ALL PEG PORTS
1: (DEFAULT)NORMAL OPERATION;
LANE# DEFINITION MATCHES
0: LANE REVERSAL
CFG_RCOMP
R1297
49.9/4/1
CFG_3
R80
1K/4/X
CFG_3:
0:Enabled
1:Dis-enabled
CFG_7
R1549
1K/4/X
PEG DEFER TRAINING
1: (DEFAULT) PEG TRAIN IMMEDIATELY
0: PEG WAIT FOR BIOS FOR TRAINING
CFG_4
R1548
1K/4
1: DISABLED
0:ENABLED; AN EXTERNAL DISPLAY PORT DEVICE
NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT
AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE
EMBEDDED DISPLAY PORT
U55K
HASWELL_BGA_E
CPU_RSVD23
CPU_RSVD24
CPU_RSVD26
CPU_RSVD27
CPU_RSVD28
CPU_RSVD29
CPU_TESTLOW1
CPU_RSVD35
CPU_RSVD36
CPU_RSVD37
CPU_RSVD38
CPU_RSVD39
CPU_TESTLOW0
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
R1298
R1299
+VCCIN
CPU_RSVD1
CPU_RSVD2
CPU_RSVD3
CPU_RSVD4
CFG_RCOMP
CFG_16
CFG_18
CFG_17
CFG_19
CPU_RSVD17
CPU_RSVD18
r01_X17_20130404
11 OF 12
BGA_HSW_37_5X32_1364P
931920/S
U55L
HASWELL_BGA_E
DAISY_CHAIN_NCTF_A3
DAISY_CHAIN_NCTF_A4
DAISY_CHAIN_NCTF_A51
DAISY_CHAIN_NCTF_A52
DAISY_CHAIN_NCTF_A53
DAISY_CHAIN_NCTF_B2
DAISY_CHAIN_NCTF_B3
DAISY_CHAIN_NCTF_B52
DAISY_CHAIN_NCTF_B53
DAISY_CHAIN_NCTF_B54
DAISY_CHAIN_NCTF_BC1
DAISY_CHAIN_NCTF_BC54
DAISY_CHAIN_NCTF_BD1
DAISY_CHAIN_NCTF_BD54
DAISY_CHAIN_NCTF_BE1
DAISY_CHAIN_NCTF_BE2
DAISY_CHAIN_NCTF_BE3
DAISY_CHAIN_NCTF_BE52
DAISY_CHAIN_NCTF_BE53
DAISY_CHAIN_NCTF_BE54
DAISY_CHAIN_NCTF_BF2
DAISY_CHAIN_NCTF_BF3
DAISY_CHAIN_NCTF_BF4
DAISY_CHAIN_NCTF_BF51
DAISY_CHAIN_NCTF_BF52
DAISY_CHAIN_NCTF_BF53
DAISY_CHAIN_NCTF_C1
DAISY_CHAIN_NCTF_C2
DAISY_CHAIN_NCTF_C3
DAISY_CHAIN_NCTF_C54
DAISY_CHAIN_NCTF_D1
DAISY_CHAIN_NCTF_D54
TP_A4
TP_A51
A52_B52
A53_B53
C3_B2
B3_A3
TP_BC1
TP_BC54
BE1_BD1
BE54_BD54
BE2_BF2
BE3_BF3
TP_BF4
TP_BF51
BE52_BF52
BE53_BF53
C1_C2
C3_B2
TP_D1
TP_D54
B54_C54
r01_X1720130404
12 OF 12
BGA_HSW_37_5X32_1364P
931920/S
GIGABYTE TECHNOLOGY COPORATION
Title
CPU_3-CFG/DDI/EDP/FDI/CFG
Size
Document Number
GA-R1456U_GC-1456PB
Rev
1.0
Date: Thursday, March 27, 2014
Sheet 5 of 54



GIGABYTE TECHNOLOGY COPORATION	
Title	CPU_4-VCC/VDDQ
Size	Document Number: GA-R1456U_GC-1456PB; Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 6 of 54

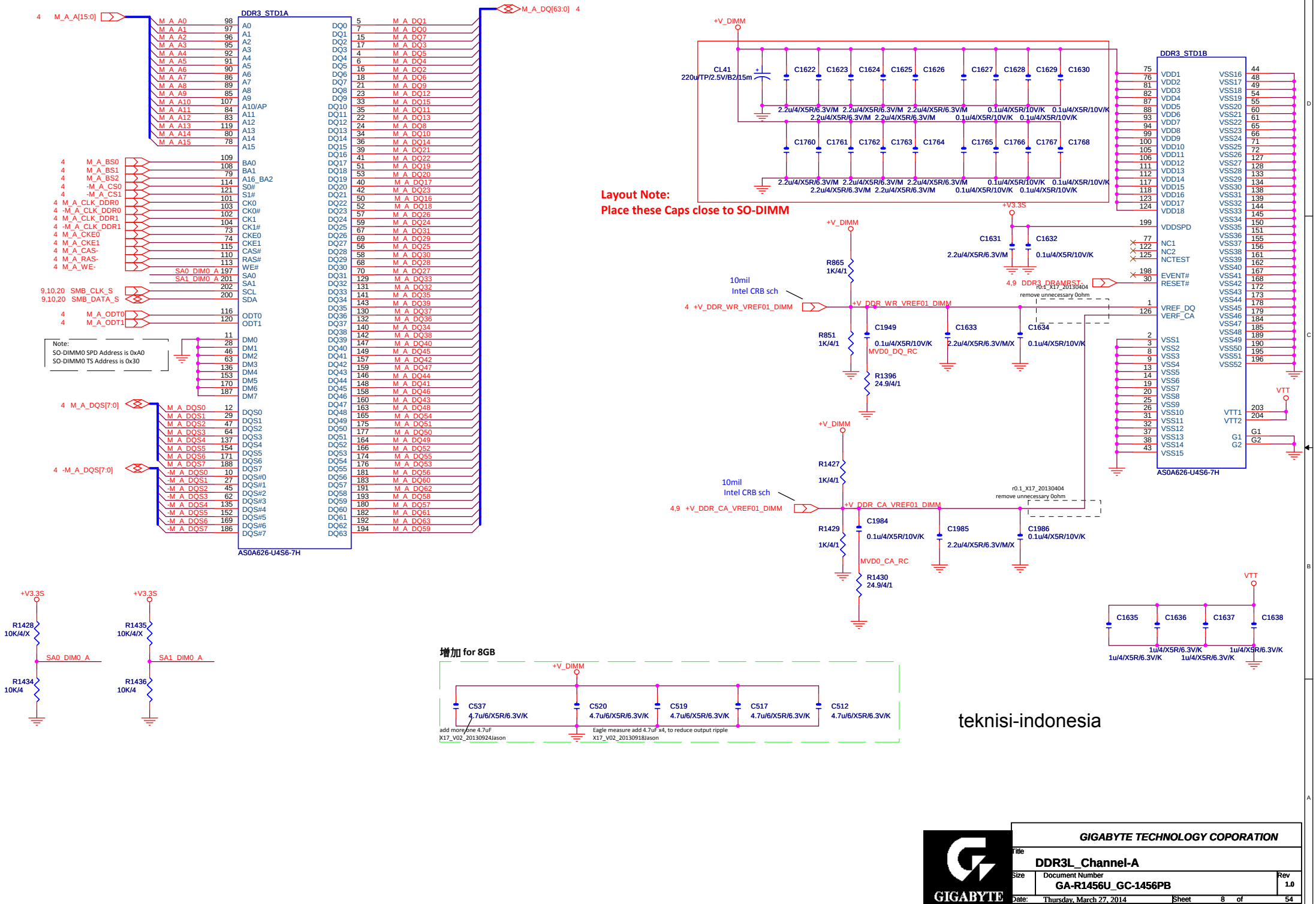


486713_486713_Shark_Bay_Mobile_PDG_Rev1_0.pdf

Hardware Design Changes Required

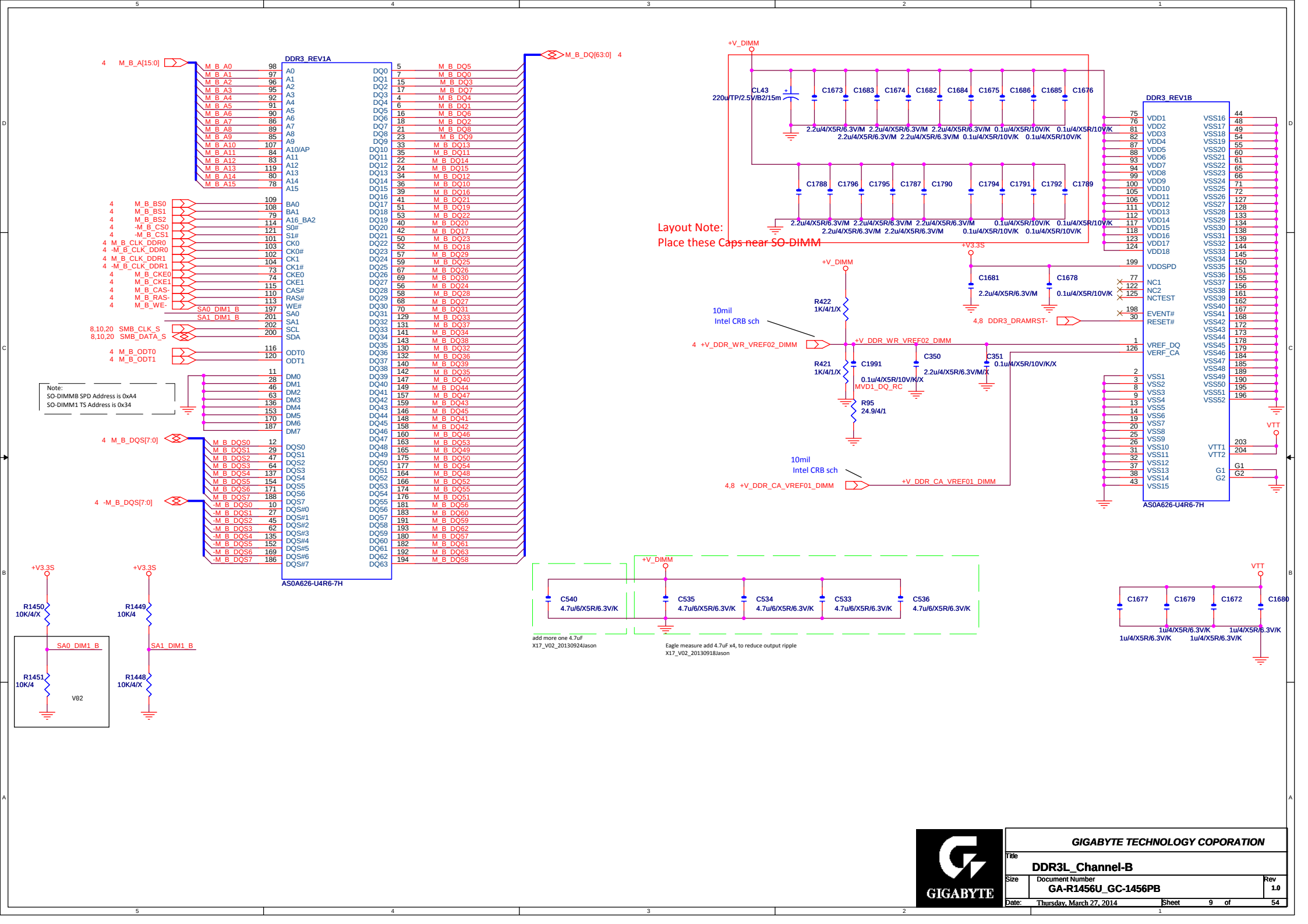
In Deep S3, the Haswell Processor will internally power gate the VDDQ rail, just like what it does in normal S3, system context is in suspended-to-RAM state, and Lynx Point Chipset Family PCH is placed in Deep Sx state. Therefore, unlike Chief River platform, there is no need to externally gate the VDDQ rail of the Processor. The Processor will also place system memory in self-refresh mode.

GIGABYTE	GIGABYTE TECHNOLOGY COPORATION	
Title	CPU_5-VSS/Decoupling_Cap	
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 7 of 54	



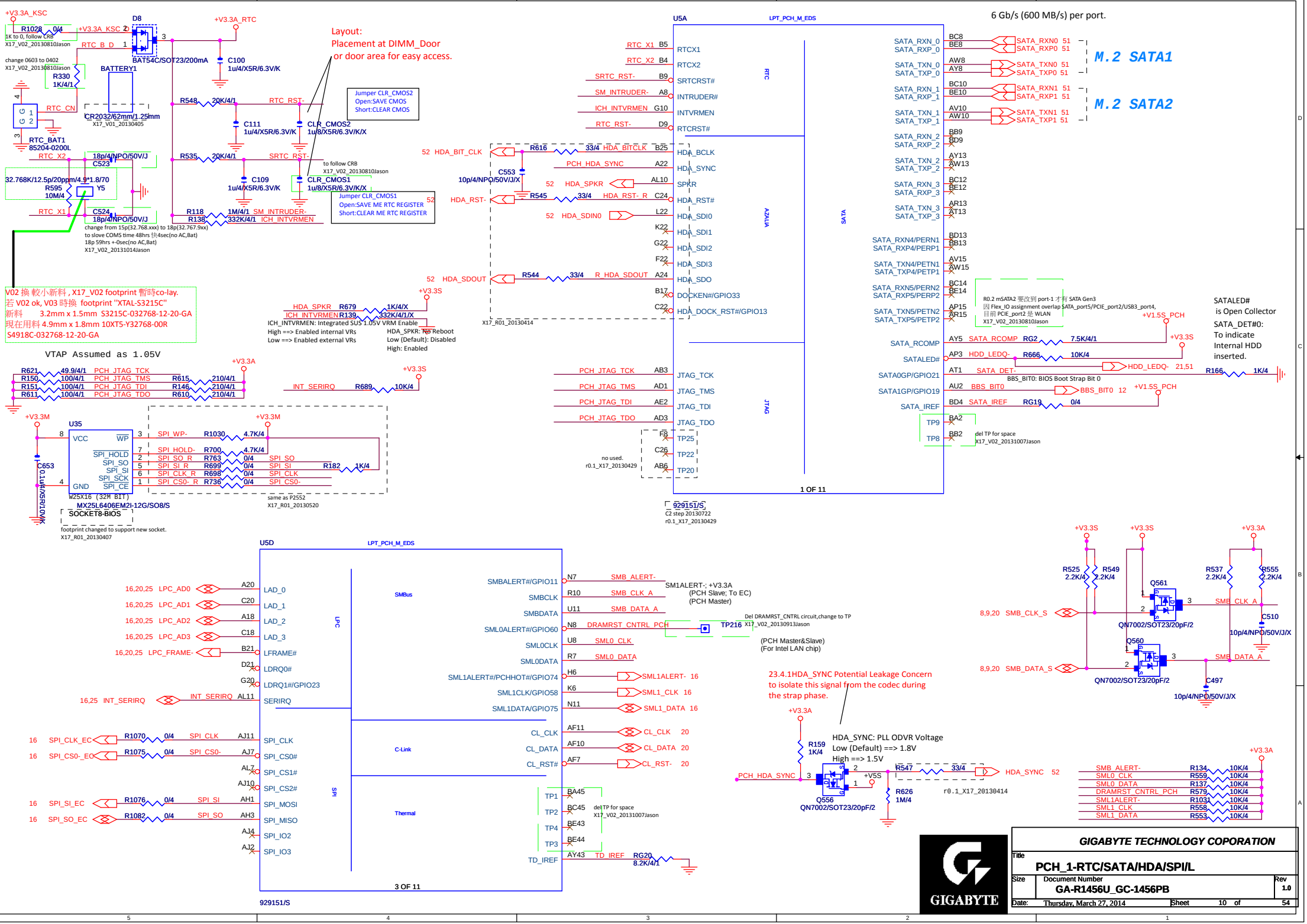
Title	DDR3L_Channel-A
Size	Document Number: GA-R1456U_GC-1456PB
Rev	1.0
Date:	Thursday, March 27, 2014
Sheet	8 of 54

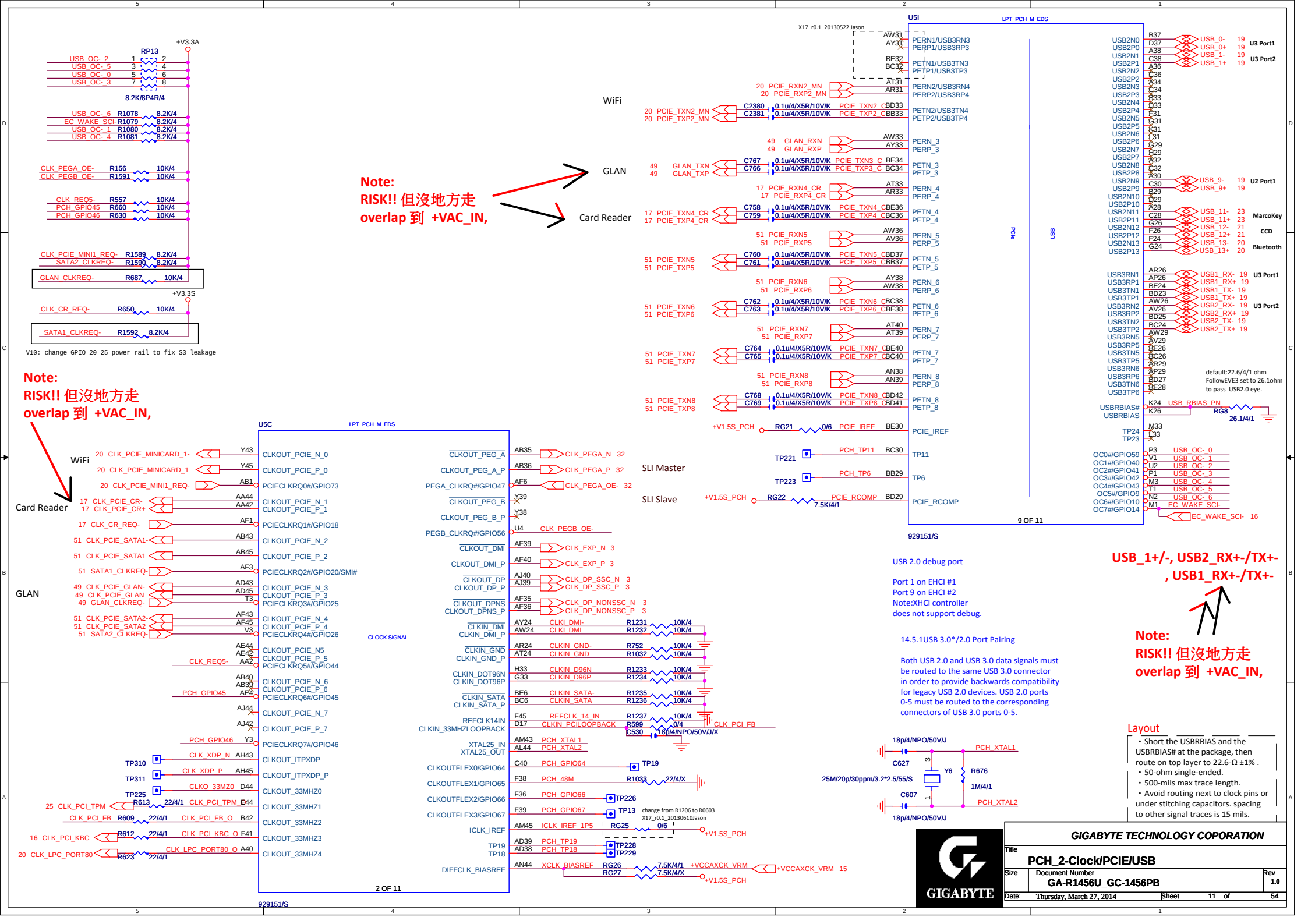
GIGABYTE TECHNOLOGY COPORATION

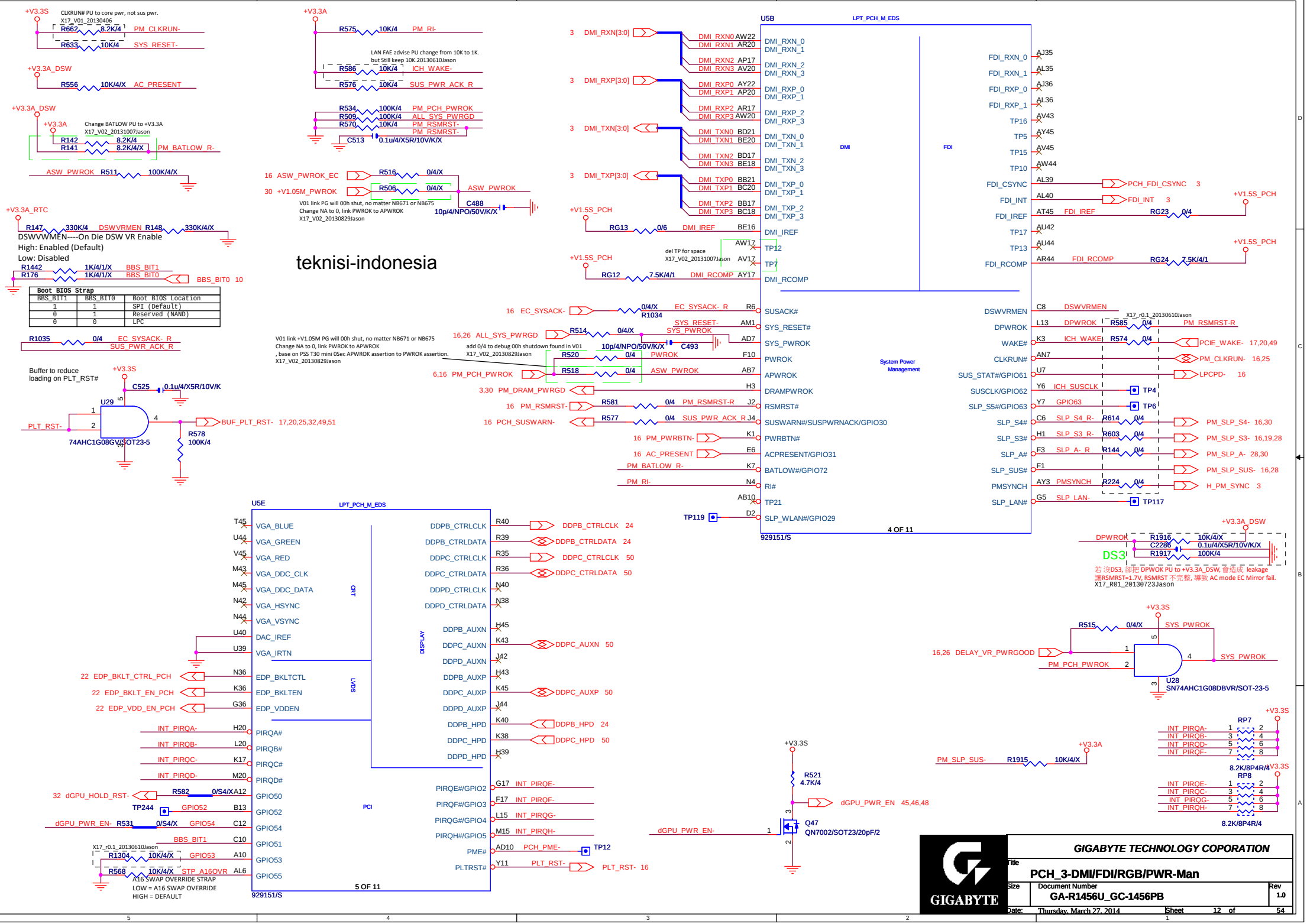


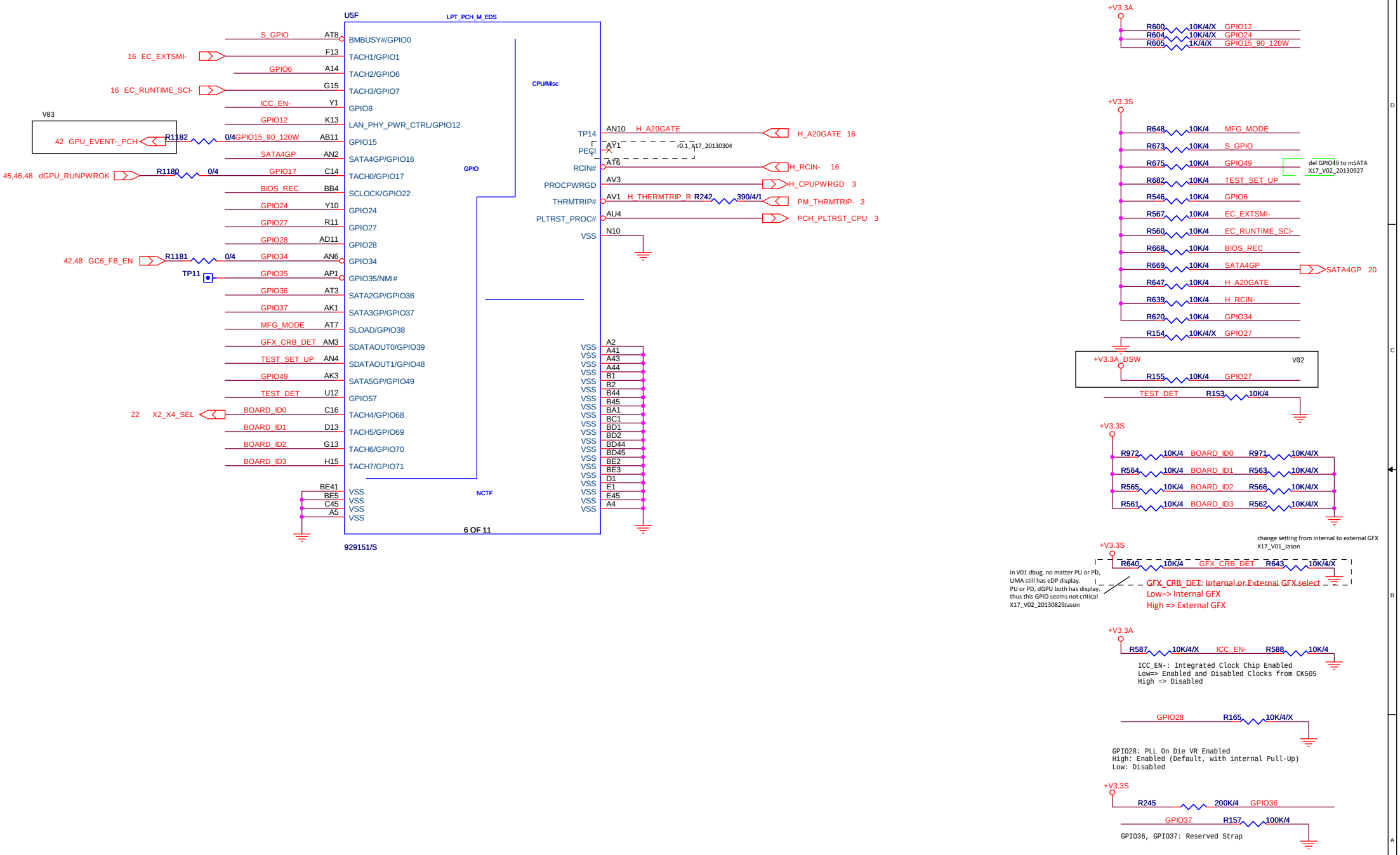
GIGABYTE TECHNOLOGY COPORATION

Title	DDR3L_Channel-B	
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 9 of 54	


6 Gb/s (600 MB/s) per port.
M.2 SATA1
M.2 SATA2
Layout:
Placement at DIMM_Door
or door area for easy access.
Jumper CLR_CMOS2
Open:SAVE CMOS
Short:CLEAR CMOS
Jumper CLR_CMOS1
Open:SAVE ME RTC REGISTER
Short:CLEAR ME RTC REGISTER
V02 換 較小新料 , X17_V02 footprint 暫時co-lay.
若 V02 ok, V03 時換 footprint "XTAL-S3215C"
新料 3.2mm x 1.5mm S3215C-032768-12-20-GA
現在用料 4.9mm x 1.8mm 10XT5-Y32768-00R
S4918C-032768-12-20-GA
VTAP Assumed as 1.05V
SATALED# is Open Collector
SATA_DET#0: To indicate Internal HDD inserted.
23.4.1HDA_SYNC Potential Leakage Concern to isolate this signal from the codec during the strap phase.
HDA_SYNC: PLL ODVR Voltage
Low (Default) ==> 1.8V
High ==> 1.5V
GIGABYTE TECHNOLOGY COPORATION
PCH_1-RTC/SATA/HDA/SPI/L
GA-R1456U_GC-1456PB
Rev 1.0
Date: Thursday, March 27, 2014
Sheet 10 of 54

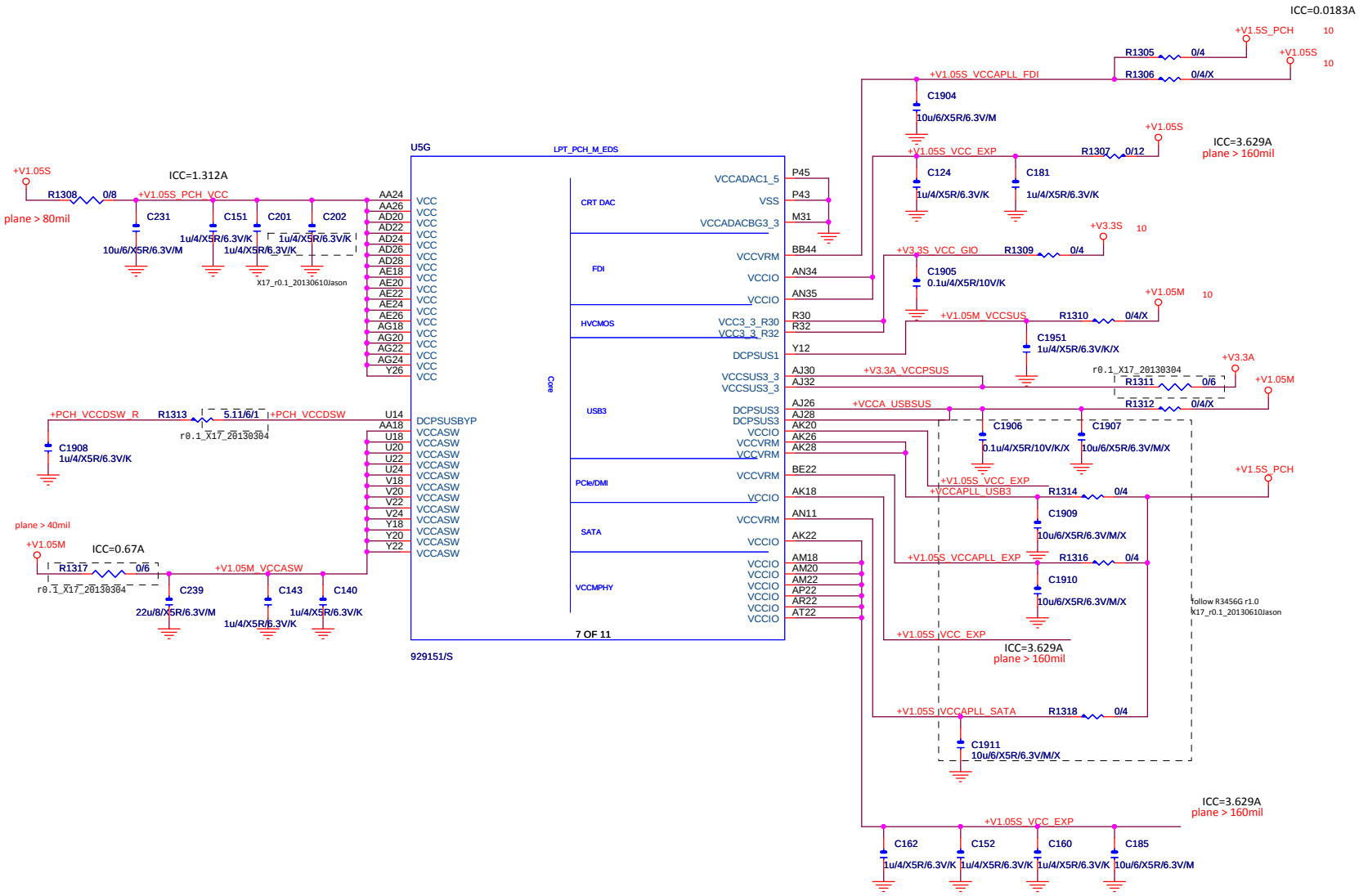

RP13
+V3.3A
USB_OC- 2
USB_OC- 5
USB_OC- 0
USB_OC- 3
8.2K/8P4R/4
USB_OC- 6 R1078 8.2K/4
EC_WAKE_SCI- R1079 8.2K/4
USB_OC- 1 R1080 8.2K/4
USB_OC- 4 R1081 8.2K/4
CLK_PEGA_OE- R156 10K/4
CLK_PEGB_OE- R1591 10K/4
CLK_REQ5- R557 10K/4
PCH_GPIO45 R660 10K/4
PCH_GPIO46 R630 10K/4
CLK_PCIE_MINI1_REQ- R1589 8.2K/4
SATA2_CLKREQ- R1590 8.2K/4
GLAN_CLKREQ- R687 10K/4
+V3.3S
CLK_CR_REQ- R650 10K/4
SATA1_CLKREQ- R1592 8.2K/4
V10: change GPIO 20 25 power rail to fix S3 leakage
Note:
RISK!! 但沒地方走
overlap 到 +VAC_IN,
WiFi
GLAN
Card Reader
U5I
LPT_PCH_M_EDS
X17_r0.1_20130522 Jason
PERN1/USB3RN3
PERP1/USB3RP3
PETN1/USB3TN3
PETP1/USB3TP3
PERN2/USB3RN4
PERP2/USB3RP4
PETN2/USB3TN4
PETP2/USB3TP4
PERN_3
PERP_3
PETN_3
PETP_3
PERN_4
PERP_4
PETN_4
PETP_4
PERN_5
PERP_5
PETN_5
PETP_5
PERN_6
PERP_6
PETN_6
PETP_6
PERN_7
PERP_7
PETN_7
PETP_7
PERN_8
PERP_8
PETN_8
PETP_8
PCIE_IREF
TP11
TP6
PCIE_RCOMP
PCIe
USB
USB2N0 USB2P0 USB2N1 USB2P1 USB2N2 USB2P2 USB2N3 USB2P3 USB2N4 USB2P4 USB2N5 USB2P5 USB2N6 USB2P6 USB2N7 USB2P7 USB2N8 USB2P8 USB2N9 USB2P9 USB2N10 USB2P10 USB2N11 USB2P11 USB2N12 USB2P12 USB2N13 USB2P13
USB_0- USB_0+ USB_1- USB_1+ U3 Port1 U3 Port2
USB_9- USB_9+ U2 Port1
USB_11- USB_11+ USB_12- USB_12+ USB_13- USB_13+ MarcoKey CCD Bluetooth
USB3RN1 USB3RP1 USB3TN1 USB3TP1 USB3RN2 USB3RP2 USB3TN2 USB3TP2 USB3RN5 USB3RP5 USB3TN5 USB3TP5 USB3RN6 USB3RP6 USB3TN6 USB3TP6
USB1_RX- USB1_RX+ USB1_TX- USB1_TX+ USB2_RX- USB2_RX+ USB2_TX- USB2_TX+ U3 Port1 U3 Port2
default:22.6/4/1 ohm
FollowEVE3 set to 26.1ohm
to pass USB2.0 eye.
USBRBIAS# USBRBIAS
USB_RBIAS_PN
RG8 26.1/4/1
OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO9 OC6#/GPIO10 OC7#/GPIO14
USB_OC- 0
USB_OC- 1
USB_OC- 2
USB_OC- 3
USB_OC- 4
USB_OC- 5
USB_OC- 6
EC_WAKE_SCI-
9 OF 11
929151/S
SLI Master
SLI Slave
RG21 0/6 PCIE_IREF
RG22 7.5K/4/1 PCIE_RCOMP
TP221
TP223
PCH_TP11
PCH_TP6
USB 2.0 debug port
Port 1 on EHCI #1
Port 9 on EHCI #2
Note:XHCI controller
does not support debug.
14.5.1USB 3.0*/2.0 Port Pairing
Both USB 2.0 and USB 3.0 data signals must
be routed to the same USB 3.0 connector
in order to provide backwards compatibility
for legacy USB 2.0 devices. USB 2.0 ports
0-5 must be routed to the corresponding
connectors of USB 3.0 ports 0-5.
USB_1+/-, USB2_RX+-/TX+-
, USB1_RX+-/TX+-
Note:
RISK!! 但沒地方走
overlap 到 +VAC_IN,
U5C
LPT_PCH_M_EDS
CLOCK SIGNAL
CLKOUT_PCIE_N_0
CLKOUT_PCIE_P_0
PCIECLKRQ0#/GPIO73
CLKOUT_PCIE_N_1
CLKOUT_PCIE_P_1
PCIECLKRQ1#/GPIO18
CLKOUT_PCIE_N_2
CLKOUT_PCIE_P_2
PCIECLKRQ2#/GPIO20/SMI#
CLKOUT_PCIE_N_3
CLKOUT_PCIE_P_3
PCIECLKRQ3#/GPIO25
CLKOUT_PCIE_N_4
CLKOUT_PCIE_P_4
PCIECLKRQ4#/GPIO26
CLKOUT_PCIE_N5
CLKOUT_PCIE_P_5
PCIECLKRQ5#/GPIO44
CLKOUT_PCIE_N_6
CLKOUT_PCIE_P_6
PCIECLKRQ6#/GPIO45
CLKOUT_PCIE_N_7
CLKOUT_PCIE_P_7
PCIECLKRQ7#/GPIO46
CLKOUT_ITPXDP
CLKOUT_ITPXDP_P
CLKOUT_33MHZ0
CLKOUT_33MHZ1
CLKOUT_33MHZ2
CLKOUT_33MHZ3
CLKOUT_33MHZ4
CLKOUT_PEG_A
CLKOUT_PEG_A_P
PEGA_CLKRQ#/GPIO47
CLKOUT_PEG_B
CLKOUT_PEG_B_P
PEGB_CLKRQ#/GPIO56
CLKOUT_DMI
CLKOUT_DMI_P
CLKOUT_DP
CLKOUT_DP_P
CLKOUT_DPNS
CLKOUT_DPNS_P
CLKIN_DMI
CLKIN_DMI_P
CLKIN_GND
CLKIN_GND_P
CLKIN_DOT96N
CLKIN_DOT96P
CLKIN_SATA
CLKIN_SATA_P
REFCLK14IN
CLKIN_33MHZLOOPBACK
XTAL25_IN
XTAL25_OUT
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
ICLK_IREF
TP19
TP18
DIFFCLK_BIASREF
2 OF 11
929151/S
WiFi
GLAN
Card Reader
CLK_PCIE_MINICARD_1-
CLK_PCIE_MINICARD_1
CLK_PCIE_MINI1_REQ-
CLK_PCIE_CR-
CLK_PCIE_CR+
CLK_CR_REQ-
CLK_PCIE_SATA1-
CLK_PCIE_SATA1
SATA1_CLKREQ-
CLK_PCIE_GLAN-
CLK_PCIE_GLAN
GLAN_CLKREQ-
CLK_PCIE_SATA2-
CLK_PCIE_SATA2
SATA2_CLKREQ-
CLK_REQ5-
PCH_GPIO45
PCH_GPIO46
CLK_XDP_N
CLK_XDP_P
CLKO_33MZ0
CLK_PCI_TPM
CLK_PCI_FB
CLK_PCI_FB_O
CLK_PCI_KBC
CLK_PCI_KBC_O
CLK_LPC_PORT80
CLK_LPC_PORT80_O
TP310
TP311
TP225
R613 22/4/1
R609 22/4/1
R612 22/4/1
R623 22/4/1
CLK_PEGA_N 32
CLK_PEGA_P 32
CLK_PEGA_OE- 32
CLK_EXP_N 3
CLK_EXP_P 3
CLK_DP_SSC_N 3
CLK_DP_SSC_P 3
CLK_DP_NONSSC_N 3
CLK_DP_NONSSC_P 3
CLKI_DMI- R1231 10K/4
CLKI_DMI R1232 10K/4
CLKIN_GND- R752 10K/4
CLKIN_GND R1032 10K/4
CLKIN_D96N R1233 10K/4
CLKIN_D96P R1234 10K/4
CLKIN_SATA- R1235 10K/4
CLKIN_SATA R1236 10K/4
REFCLK_14_IN R1237 10K/4
CLKIN_PCILOOPBACK R599 0/4
C530 18p/4/NPO/50V/J/X
CLK_PCI_FB
PCH_XTAL1
PCH_XTAL2
PCH_GPIO64
PCH_48M
PCH_GPIO66
PCH_GPIO67
ICLK_IREF_1P5
PCH_TP19
PCH_TP18
XCLK_BIASREF
TP19
R1033 22/4/X
TP226
TP13
change from R1206 to R0603
X17_r0.1_20130610Jason
RG25 0/6
TP228
TP229
RG26 7.5K/4/1
RG27 7.5K/4/X
+VCCAXCK_VRM
+VCCAXCK_VRM 15
+V1.5S_PCH
18p/4/NPO/50V/J
C627
Y6
R676 1M/4/1
25M/20p/30ppm/3.2*2.5/5S/S
C607
Layout
• Short the USBRBIAS and the USBRBIAS# at the package, then route on top layer to 22.6-Ω ±1% .
• 50-ohm single-ended.
• 500-mils max trace length.
• Avoid routing next to clock pins or under stitching capacitors. spacing to other signal traces is 15 mils.
GIGABYTE TECHNOLOGY COPORATION
Title
PCH_2-Clock/PCIE/USB
Size
Document Number
GA-R1456U_GC-1456PB
Rev
1.0
Date: Thursday, March 27, 2014
Sheet 11 of 54
GIGABYTE


+V3.3S
CLKRUN# PU to core pwr, not sus pwr.
X17_V01_20130406
R662 8.2K/4
R633 10K/4
PM_CLKRUN-
SYS_RESET-
+V3.3A_DSW
R556 10K/4/X AC_PRESENT
+V3.3A_DSW
+V3.3A
Change BATLOW PU to +V3.3A
X17_V02_20131007Jason
R142 8.2K/4
R141 8.2K/4/X
PM_BATLOW_R-
ASW_PWROK R511 100K/4/X
+V3.3A_RTC
R147 330K/4 DSWVRMEN R148 330K/4/X
DSWVWMEN----On Die DSW VR Enable
High: Enabled (Default)
Low: Disabled
R1442 1K/4/1/X BBS_BIT1
R176 1K/4/1/X BBS_BIT0
BBS_BIT0 10
Boot BIOS Strap
BBS_BIT1 | BBS_BIT0 | Boot BIOS Location
1 | 1 | SPI (Default)
0 | 1 | Reserved (NAND)
0 | 0 | LPC
R1035 0/4 EC_SYSACK- R
SUS_PWR_ACK_R
Buffer to reduce loading on PLT_RST#
+V3.3S
C525 0.1u/4/X5R/10V/K
U29
PLT_RST-
BUF_PLT_RST- 17,20,25,32,49,51
R578 100K/4
74AHC1G08GV/SOT23-5
+V3.3A
R575 10K/4 PM_RI-
LAN FAE advise PU change from 10K to 1K.
but Still keep 10K.20130610Jason
R586 10K/4 ICH_WAKE-
R576 10K/4 SUS_PWR_ACK_R
R534 100K/4 PM_PCH_PWROK
R509 100K/4 ALL_SYS_PWRGD
R570 10K/4 PM_RSMRST-
PM_RSMRST-
C513 0.1u/4/X5R/10V/K/X
16 ASW_PWROK_EC
30 +V1.05M_PWROK
R516 0/4/X
R506 0/4/X
ASW_PWROK
C488 10p/4/NPO/50V/K/X
V01 link PG will 00h shut, no matter NB671 or NB675
Change NA to 0, link PWROK to APWROK
X17_V02_20130829Jason
teknisi-indonesia
U5B
LPT_PCH_M_EDS
3 DMI_RXN[3:0]
DMI_RXN0 AW22
DMI_RXN1 AR20
DMI_RXN2 AP17
DMI_RXN3 AV20
3 DMI_RXP[3:0]
DMI_RXP0 AY22
DMI_RXP1 AP20
DMI_RXP2 AR17
DMI_RXP3 AW20
3 DMI_TXN[3:0]
DMI_TXN0 BD21
DMI_TXN1 BE20
DMI_TXN2 BD17
DMI_TXN3 BE18
3 DMI_TXP[3:0]
DMI_TXP0 BB21
DMI_TXP1 BC20
DMI_TXP2 BB17
DMI_TXP3 BC18
+V1.5S_PCH
RG13 0/6 DMI_IREF BE16
DMI_IREF
AW17 TP12
del TP for space
X17_V02_20131007Jason
AV17 TP7
+V1.5S_PCH
RG12 7.5K/4/1 DMI_RCOMP AY17
DMI_RCOMP
DMI
FDI
FDI_RXN_0 AJ35
FDI_RXN_1 AL35
FDI_RXP_0 AJ36
FDI_RXP_1 AL36
TP16 AV43
TP5 AY45
TP15 AV45
TP10 AW44
FDI_CSYNC AL39
PCH_FDI_CSYNC 3
FDI_INT AL40
FDI_INT 3
+V1.5S_PCH
FDI_IREF AT45
FDI_IREF RG23 0/4
TP17 AU42
TP13 AU44
+V1.5S_PCH
FDI_RCOMP AR44
FDI_RCOMP RG24 7.5K/4/1
16 EC_SYSACK-
0/4/X EC_SYSACK- R R6
R1034
SUSACK#
SYS_RESET- AM1
SYS_RESET#
16,26 ALL_SYS_PWRGD
R514 0/4/X
SYS_PWROK
C493 10p/4/NPO/50V/K/X
SYS_PWROK AD7
V01 link +V1.05M PG will 00h shut, no matter NB671 or NB675
Change NA to 0, link PWROK to APWROK
, base on PSS T30 mini 0Sec APWROK assertion to PWROK assertion.
X17_V02_20130829Jason
add 0/4 to debug 00h shutdown found in V01
X17_V02_20130829Jason
R520 0/4 PWROK F10
PWROK
6,16 PM_PCH_PWROK
R518 0/4 ASW_PWROK AB7
APWROK
System Power Management
3,30 PM_DRAM_PWRGD
H3
DRAMPWROK
16 PM_RSMRST-
R581 0/4 PM_RSMRST-R J2
RSMRST#
16 PCH_SUSWARN-
R577 0/4 SUS_PWR_ACK_R J4
SUSWARN#/SUSPWRNACK/GPIO30
16 PM_PWRBTN-
K1
PWRBTN#
16 AC_PRESENT
E6
ACPRESENT/GPIO31
PM_BATLOW_R-
K7
BATLOW#/GPIO72
PM_RI-
N4
RI#
AB10 TP21
TP119
D2
SLP_WLAN#/GPIO29
4 OF 11
929151/S
DSWVRMEN C8 DSWVRMEN
DPWROK L13 DPWROK R585 0/4 PM_RSMRST-R
X17_r0.1_20130610Jason
WAKE# K3 ICH_WAKE# R574 0/4 PCIE_WAKE- 17,20,49
CLKRUN# AN7 PM_CLKRUN- 16,25
SUS_STAT#/GPIO61 U7 LPCPD- 16
SUSCLK/GPIO62 Y6 ICH_SUSCLK TP4
SLP_S5#/GPIO63 Y7 GPIO63 TP6
SLP_S4# C6 SLP_S4_R- R614 0/4 PM_SLP_S4- 16,30
SLP_S3# H1 SLP_S3_R- R603 0/4 PM_SLP_S3- 16,19,28
SLP_A# F3 SLP_A-_R R144 0/4 PM_SLP_A- 28,30
SLP_SUS# F1 PM_SLP_SUS- 16,28
PMSYNCH AY3 PMSYNCH R224 0/4 H_PM_SYNC 3
SLP_LAN# G5 SLP_LAN- TP117
+V3.3A_DSW
DPWROK R1916 10K/4/X
C2286 0.1u/4/X5R/10V/K/X
R1917 100K/4
DS3
若沒DS3, 卻把 DPWOK PU to +V3.3A_DSW, 會造成 leakage
讓RSMRST=1.7V, RSMRST 不完整, 導致 AC mode EC Mirror fail.
X17_R01_20130723Jason
U5E
LPT_PCH_M_EDS
CRT
VGA_BLUE T45
VGA_GREEN U44
VGA_RED V45
VGA_DDC_CLK M43
VGA_DDC_DATA M45
VGA_HSYNC N42
VGA_VSYNC N44
DAC_IREF U40
VGA_IRTN U39
DISPLAY
DDPB_CTRLCLK R40 DDPB_CTRLCLK 24
DDPB_CTRLDATA R39 DDPB_CTRLDATA 24
DDPC_CTRLCLK R35 DDPC_CTRLCLK 50
DDPC_CTRLDATA R36 DDPC_CTRLDATA 50
DDPD_CTRLCLK N40
DDPD_CTRLDATA N38
DDPB_AUXN H45
DDPC_AUXN K43 DDPC_AUXN 50
DDPD_AUXN J42
DDPB_AUXP H43
DDPC_AUXP K45 DDPC_AUXP 50
DDPD_AUXP J44
DDPB_HPD K40 DDPB_HPD 24
DDPC_HPD K38 DDPC_HPD 50
DDPD_HPD H39
LVDS
22 EDP_BKLT_CTRL_PCH
EDP_BKLTCTL N36
22 EDP_BKLT_EN_PCH
EDP_BKLTEN K36
22 EDP_VDD_EN_PCH
EDP_VDDEN G36
INT_PIRQA- PIRQA# H20
INT_PIRQB- PIRQB# L20
INT_PIRQC- PIRQC# K17
INT_PIRQD- PIRQD# M20
PCI
32 dGPU_HOLD_RST-
R582 0/S4/X
GPIO50 A12
TP244
GPIO52 B13
dGPU_PWR_EN- R531 0/S4/X
GPIO54 C12
BBS_BIT1 C10
GPIO51
X17_r0.1_20130610Jason
R1304 10K/4/X GPIO53 A10
R568 10K/4/X STP_A16OVR AL6
A16 SWAP OVERRIDE STRAP
LOW = A16 SWAP OVERRIDE
HIGH = DEFAULT
GPIO55
PIRQE#/GPIO2 G17 INT_PIRQE-
PIRQF#/GPIO3 F17 INT_PIRQF-
PIRQG#/GPIO4 L15 INT_PIRQG-
PIRQH#/GPIO5 M15 INT_PIRQH-
PME# AD10 PCH_PME- TP12
PLTRST# Y11 PLT_RST- PLT_RST- 16
5 OF 11
929151/S
+V3.3S
R515 0/4/X SYS_PWROK
16,26 DELAY_VR_PWRGOOD
PM_PCH_PWROK
U28
SN74AHC1G08DBVR/SOT-23-5
+V3.3S
R521 4.7K/4
dGPU_PWR_EN 45,46,48
dGPU_PWR_EN-
Q47
QN7002/SOT23/20pF/2
PM_SLP_SUS- R1915 10K/4/X
+V3.3A
+V3.3S
RP7
INT_PIRQA-
INT_PIRQB-
INT_PIRQD-
INT_PIRQF-
8.2K/8P4R/4
+V3.3S
RP8
INT_PIRQE-
INT_PIRQC-
INT_PIRQG-
INT_PIRQH-
8.2K/8P4R/4
GIGABYTE TECHNOLOGY COPORATION
Title
PCH_3-DMI/FDI/RGB/PWR-Man
Size
Document Number
GA-R1456U_GC-1456PB
Rev
1.0
Date: Thursday, March 27, 2014
Sheet 12 of 54

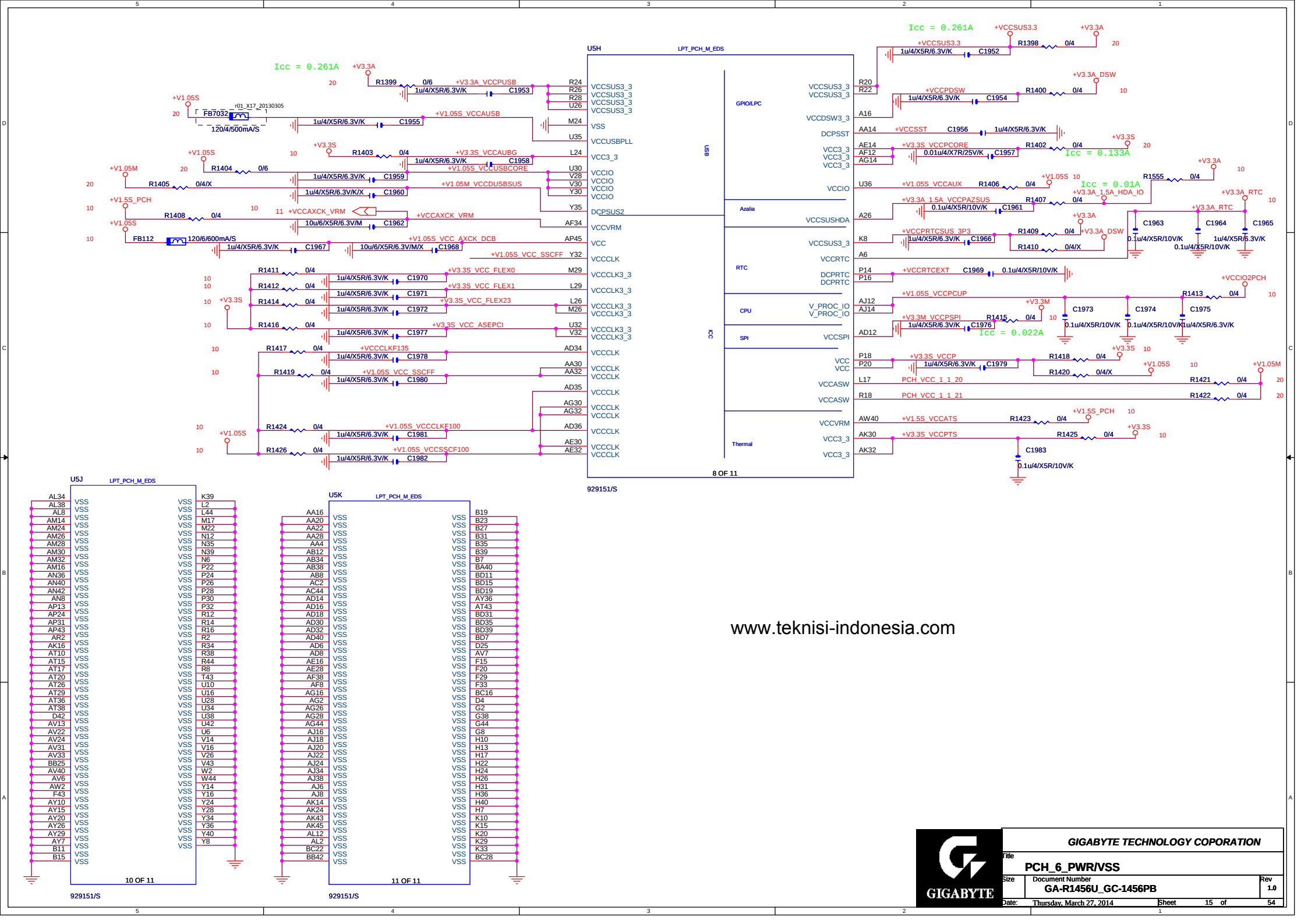


GIGABYTE TECHNOLOGY COPORATION

Title	PCH_4-GPIO/MISC	
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 13 of 54	



GIGABYTE	GIGABYTE TECHNOLOGY COPORATION		
	Title: PCH_5-PWR		
	Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
	Date: Thursday, March 27, 2014	Sheet 14 of 54	



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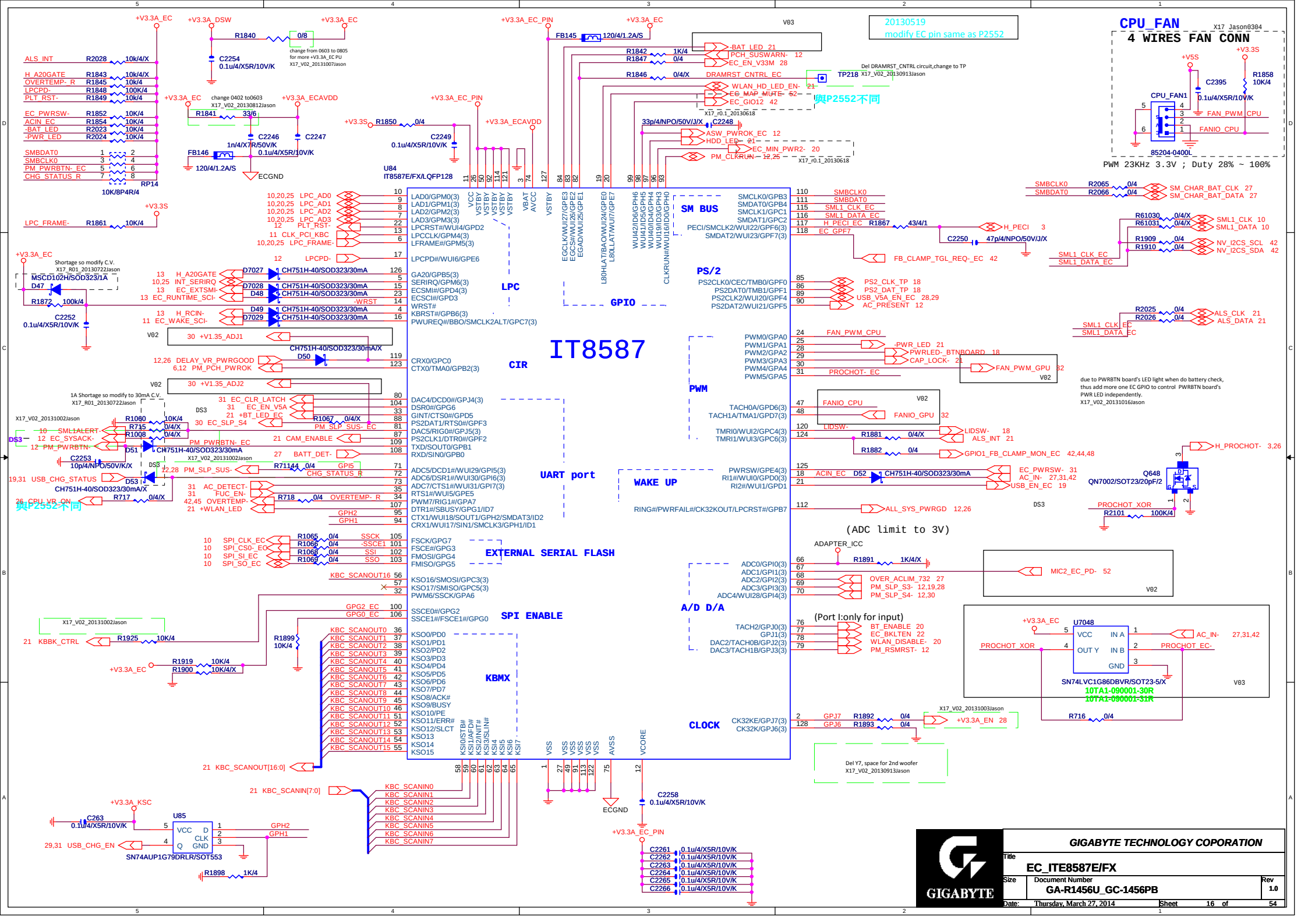
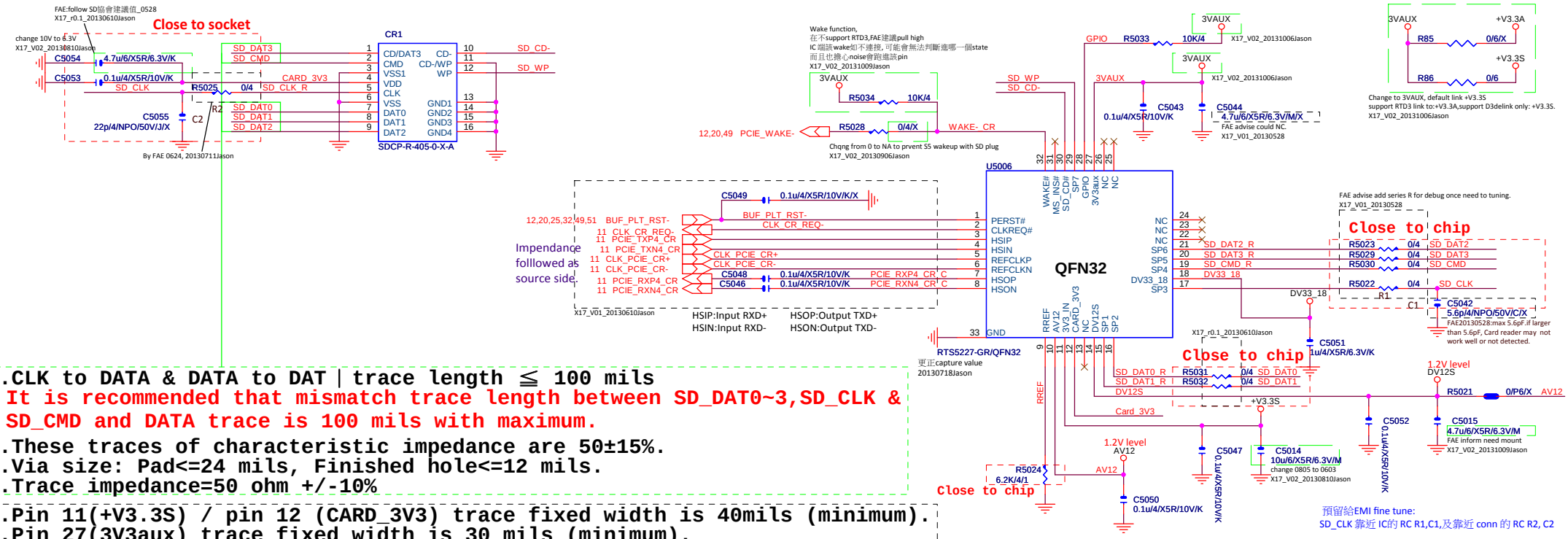
Title	PCH_6_PWR/VSS	
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 15 of 54	


IT8587
SM BUS
PS/2
LPC
GPIO
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
20130519
modify EC pin same as P2552
CPU_FAN
4 WIRES FAN CONN
PWM 23KHz 3.3V ; Duty 28% ~ 100%
(ADC limit to 3V)
(Port I:only for input)
GIGABYTE TECHNOLOGY COPORATION
EC_ITE8587E/FX
GA-R1456U_GC-1456PB
Thursday, March 27, 2014



1. CLK to DATA & DATA to DAT | trace length ≦ 100 mils
   It is recommended that mismatch trace length between SD_DAT0~3,SD_CLK & SD_CMD and DATA trace is 100 mils with maximum.
2. These traces of characteristic impedance are 50±15%.
3. Via size: Pad<=24 mils, Finished hole<=12 mils.
4. Trace impedance=50 ohm +/-10%

1. Pin 11(+V3.3S) / pin 12 (CARD_3V3) trace fixed width is 40mils (minimum).
2. Pin 27(3V3aux) trace fixed width is 30 mils (minimum).
3. Pin 10(AV12), pin 14(DV12S), pin 18 (DV33_18) trace fixed width is 20 mils(minimum). Keep the trace routing lengths is limit to 200mils.
4. Pin 9 (RREF) trace fixed width is 12 mils (minimum).
   Keep the trace routing lengths is limit to 200mils.
5. Via size: Pad>=28 mils, Finished hole>=16 mils.

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Title	Card_Reader_RTS5227	
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
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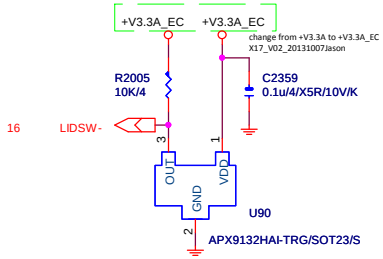
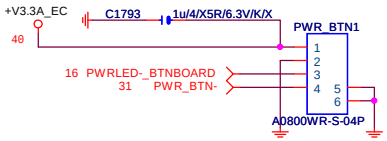
Hall Effect Micro Switch IC



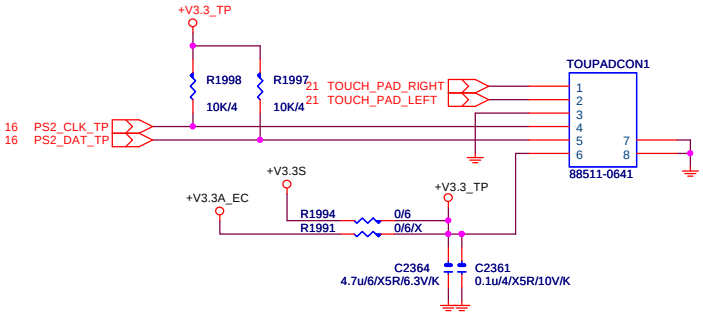
Power_Button_Cnn



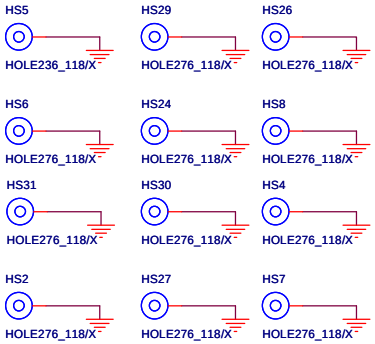
Touch_Pad

S9852A-41H1 Pin Assignment

PIN#	1	2	3	4	5	6
SIGNAL	Right	Left	GND	CLK	DATA	VCC

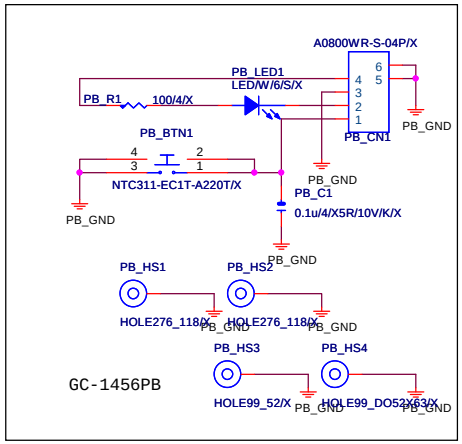


HOLE276_118 x 12

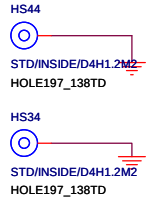


PCB

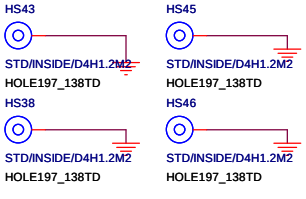
V10: change power button from MPTCFG-T-Q-T/R to NTC311-EC1T-A220T



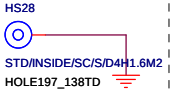
GPU
M2.0 x H1.2mm stand off



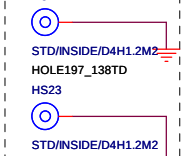
CPU
M2.0 x H1.2mm stand off



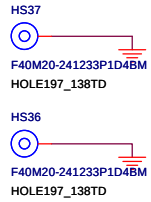
For WiFi card
M2.0 x 1.6mm stand off



For PCH heatsink
M2.0 x H1.2mm stand off



For NGFF card
M2.0 x H2.4mm stand off



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Title: TouchPad/MouseKey/PWRBTN/ScrewHole

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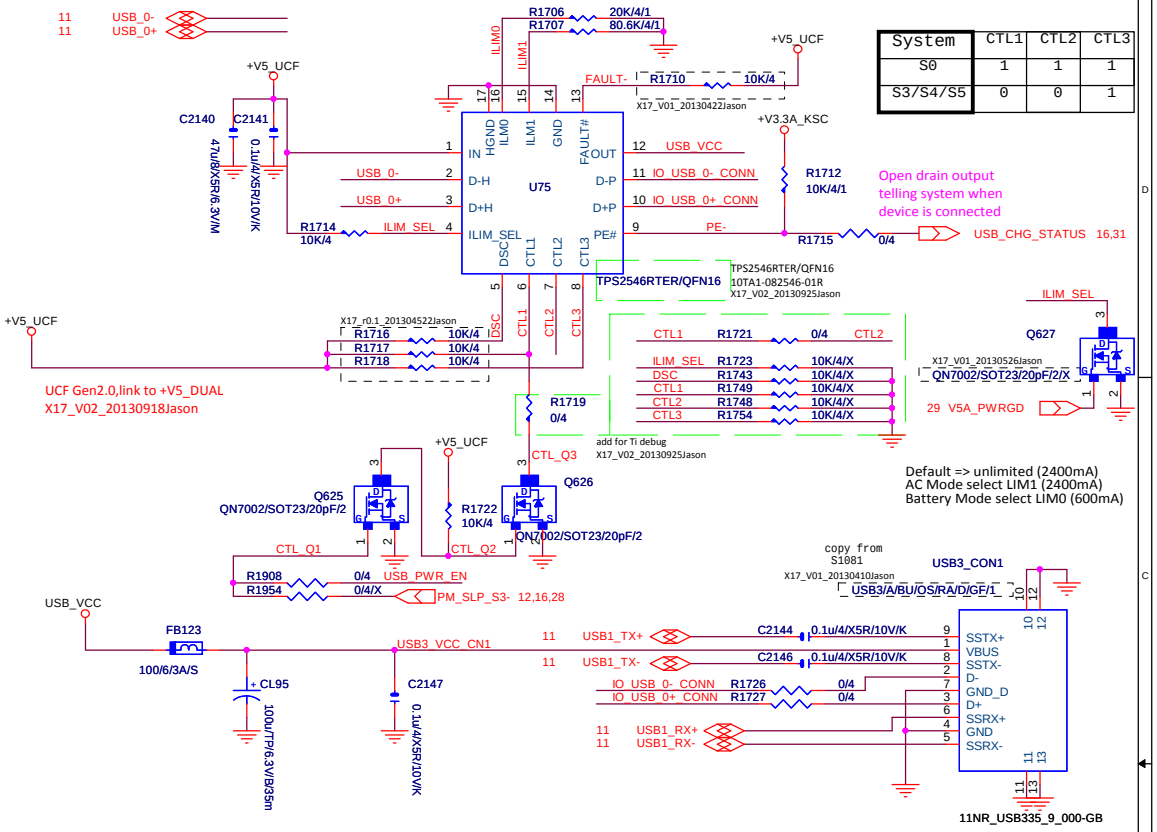
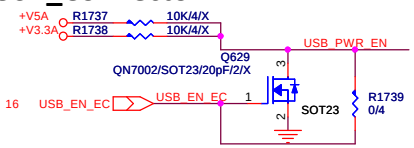
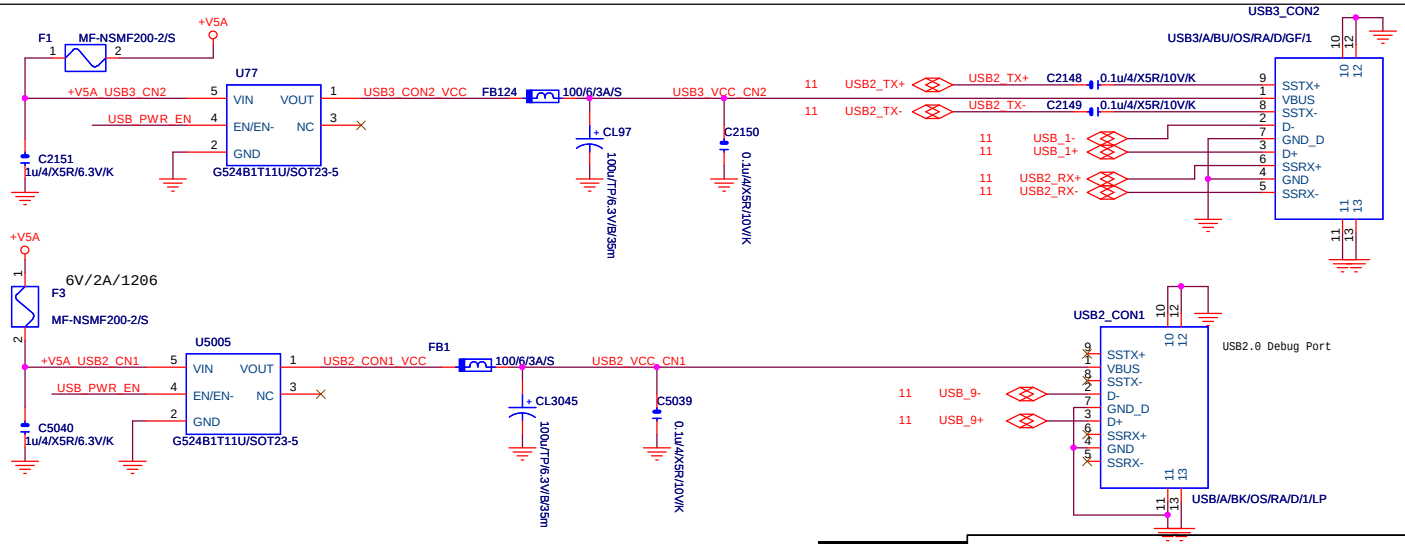
USB_Charging_Function



USB_Connector





GIGABYTE TECHNOLOGY COPORATION

Title: USB2.0/USB3.0/UCF

Size: | Document Number: GA-R1456U_GC-1456PB | Rev: 1.0

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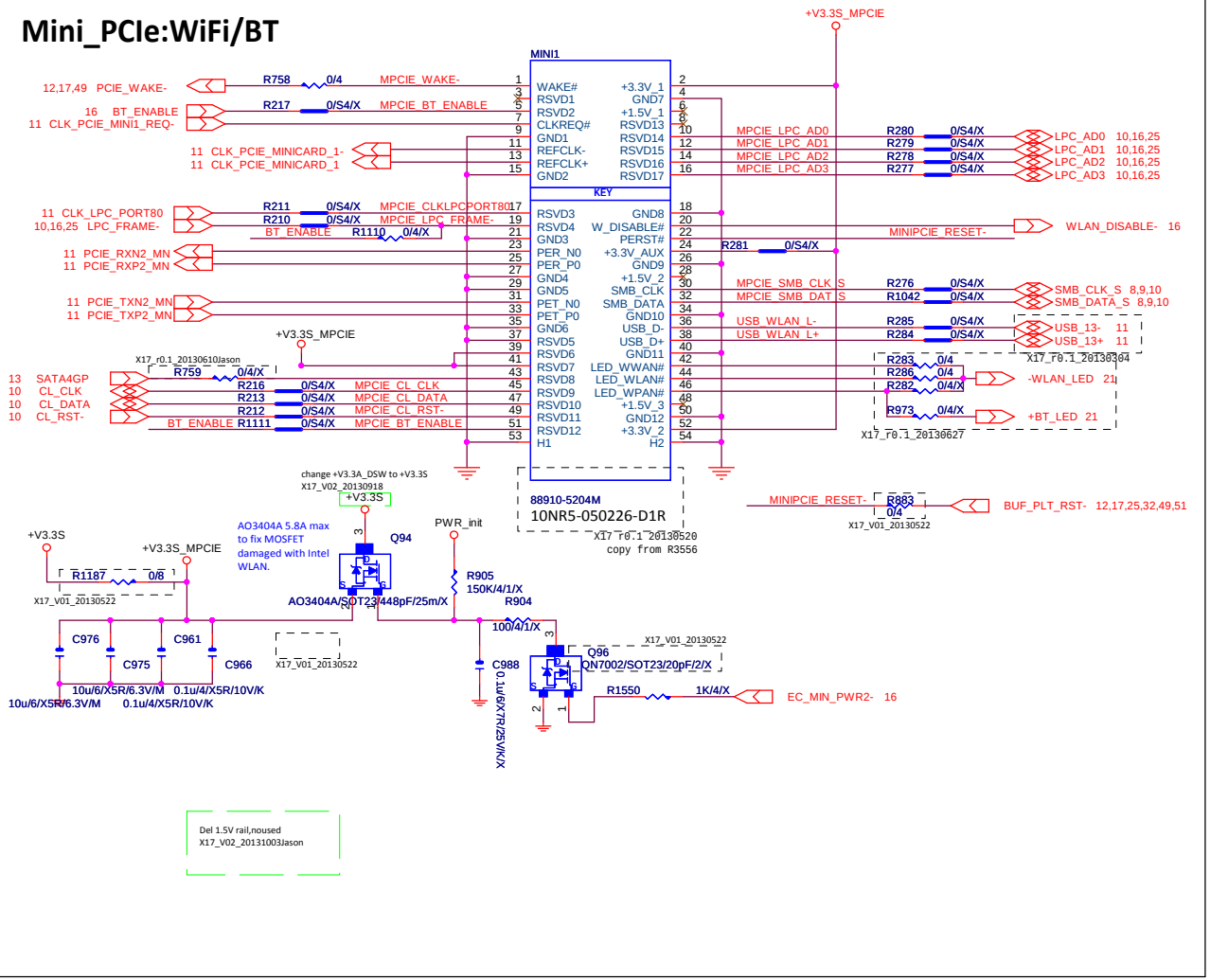
Mini_PCIe:WiFi/BT



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GIGABYTE TECHNOLOGY COPORATION

Title: MiniPCIE/mSATA/WiFiBT/HDD/re-Driver

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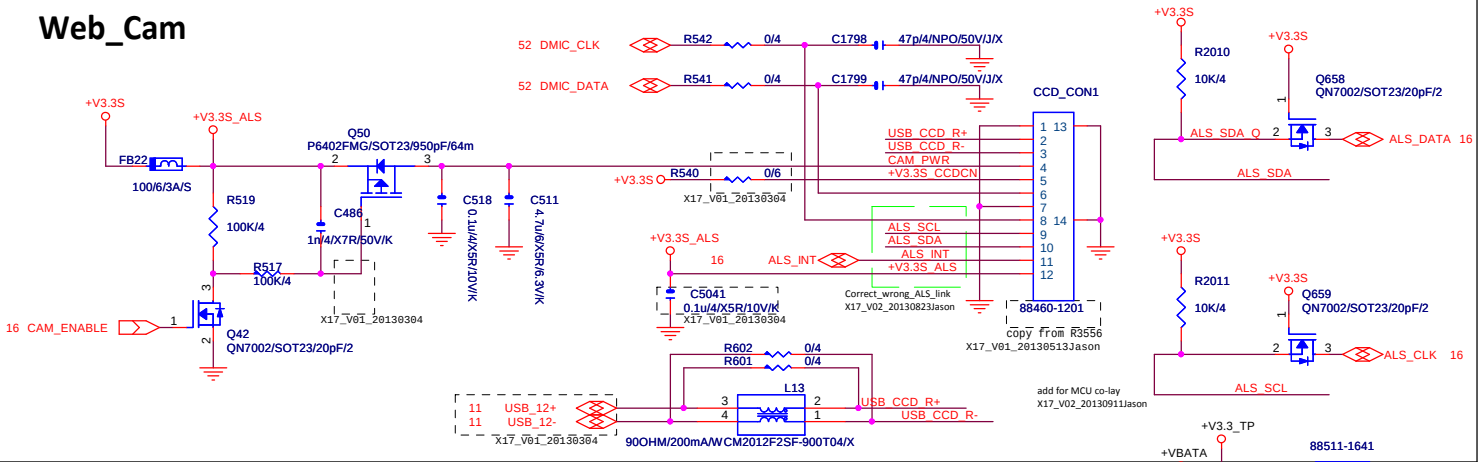
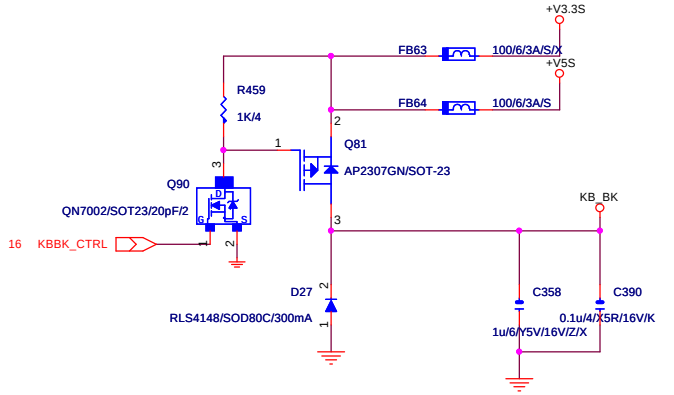
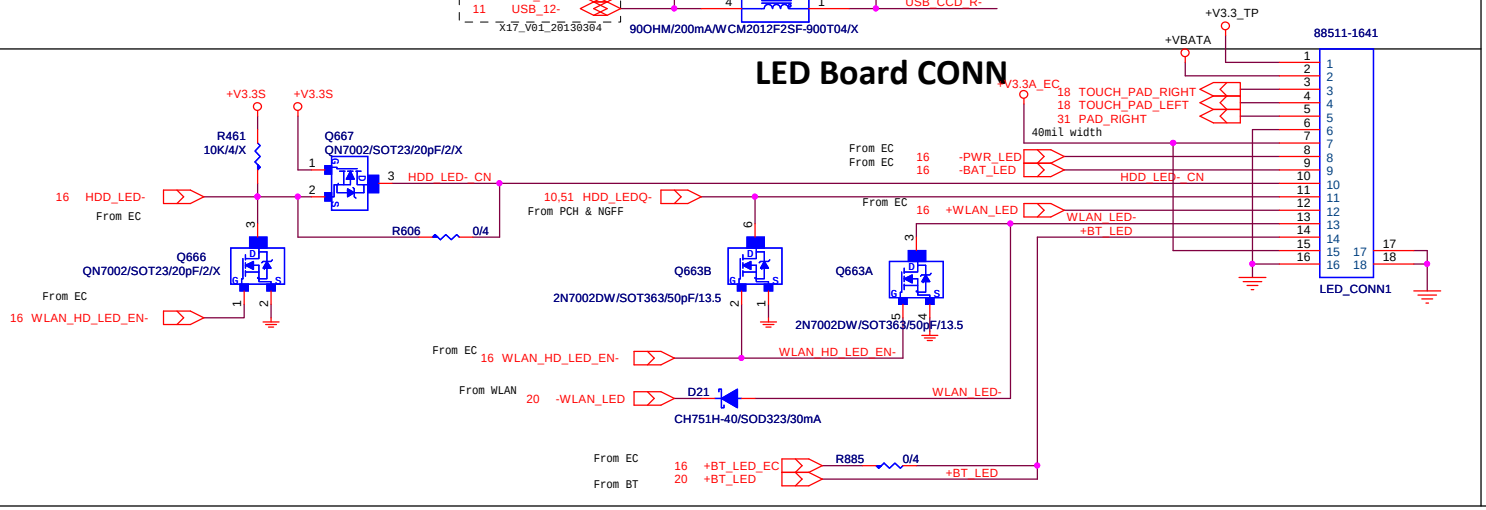
Web_Cam



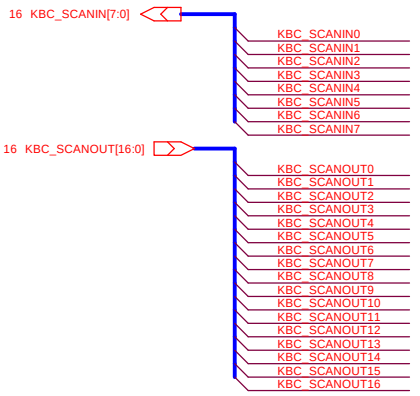


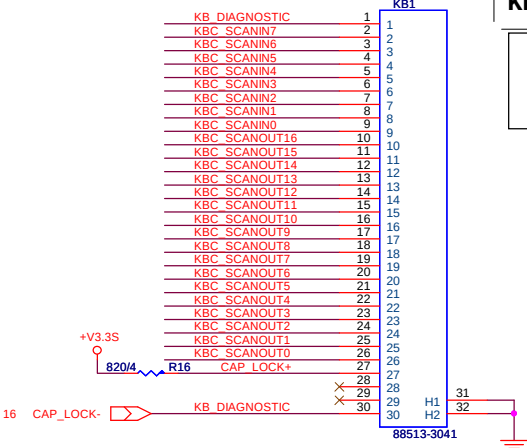
KB power consumption as below, 3.3V => 0.15A ; 4V => 0.3A ; 5V => 0.5A

LED Board CONN

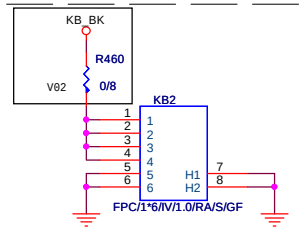


KEYBOARD_CONNECTOR





KEYBOARD CONNECTOR



KB2 for keyboard back light.

KB LED Power 2.5V~5V

GIGABYTE TECHNOLOGY COPORATION

Title: Board_Connectors/MCU_for_ALS

Size | Document Number: GA-R1456U_GC-1456PB | Rev: 1.0

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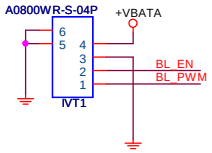
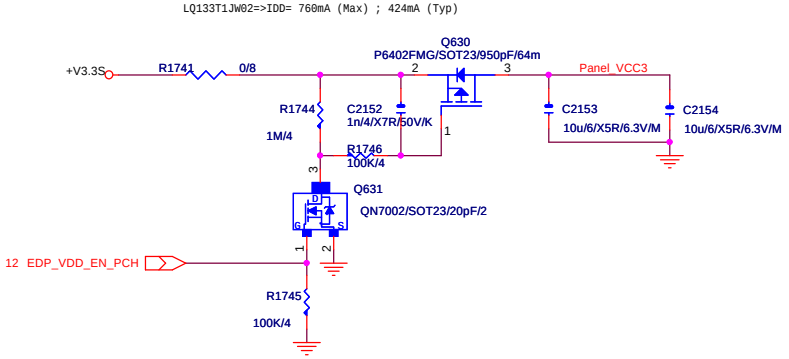
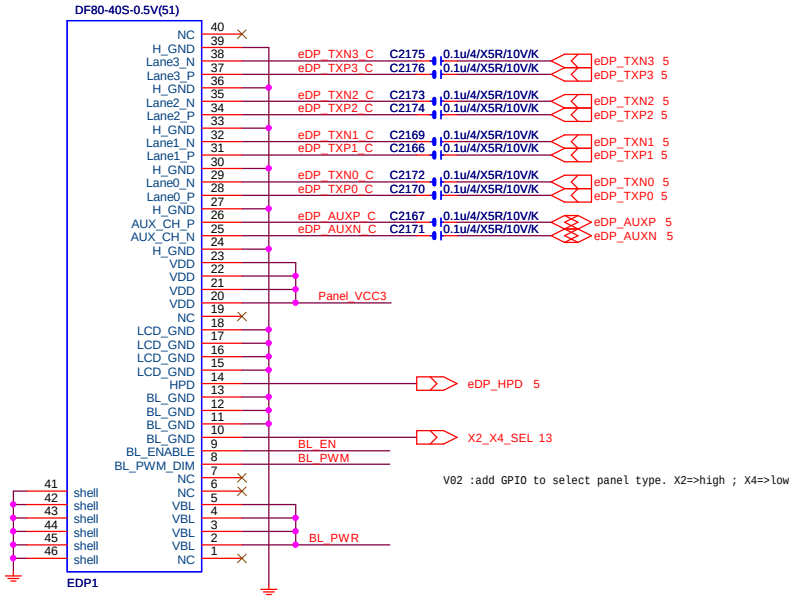
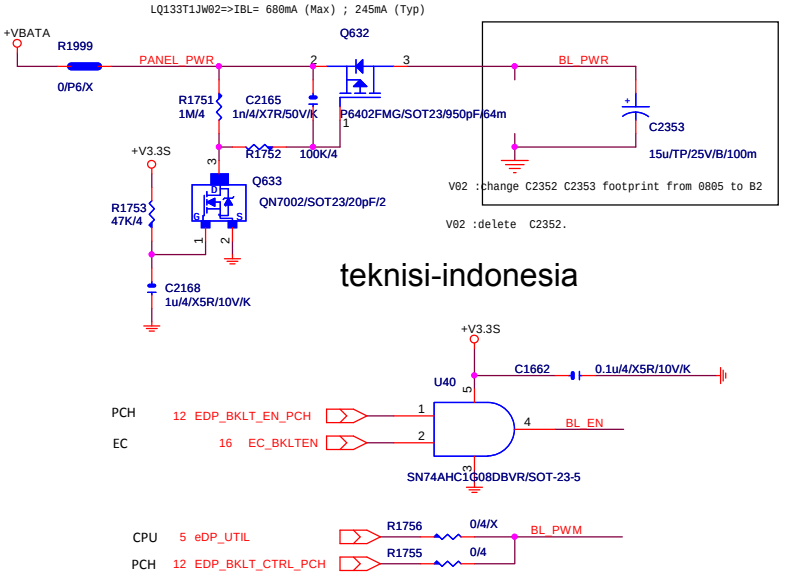




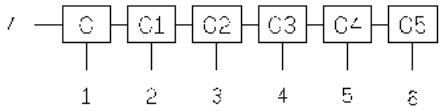
V02 :change eDP connector by SI

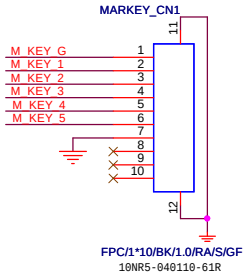


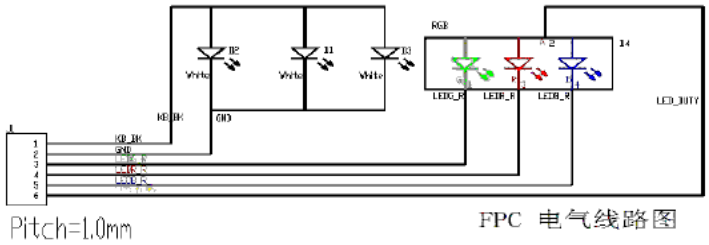
V02 :add GPIO to select panel type. X2=>high ; X4=>low

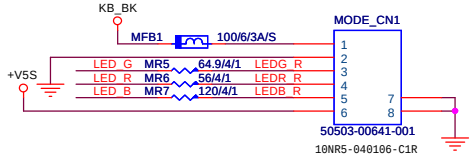


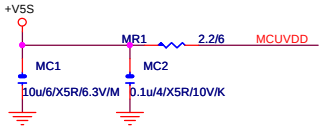
GIGABYTE	GIGABYTE TECHNOLOGY COPORATION	
	Title: eDP	
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 22 of 54	

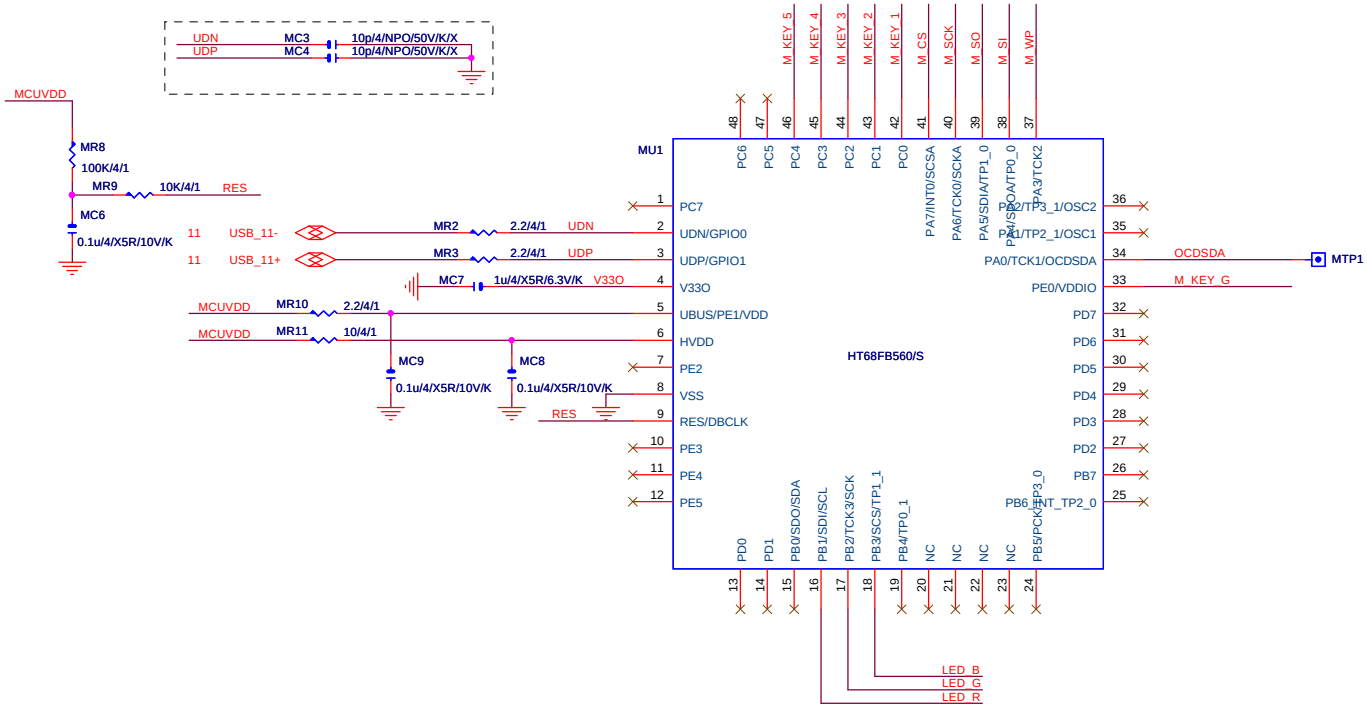


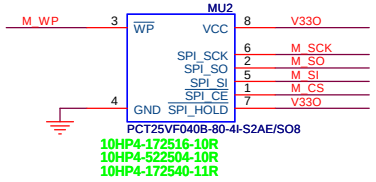












GIGABYTE TECHNOLOGY COPORATION

Title	Marco_Key_HT68FB560		
Size	Document Number GA-R1456U_GC-1456PB		Rev 1.0
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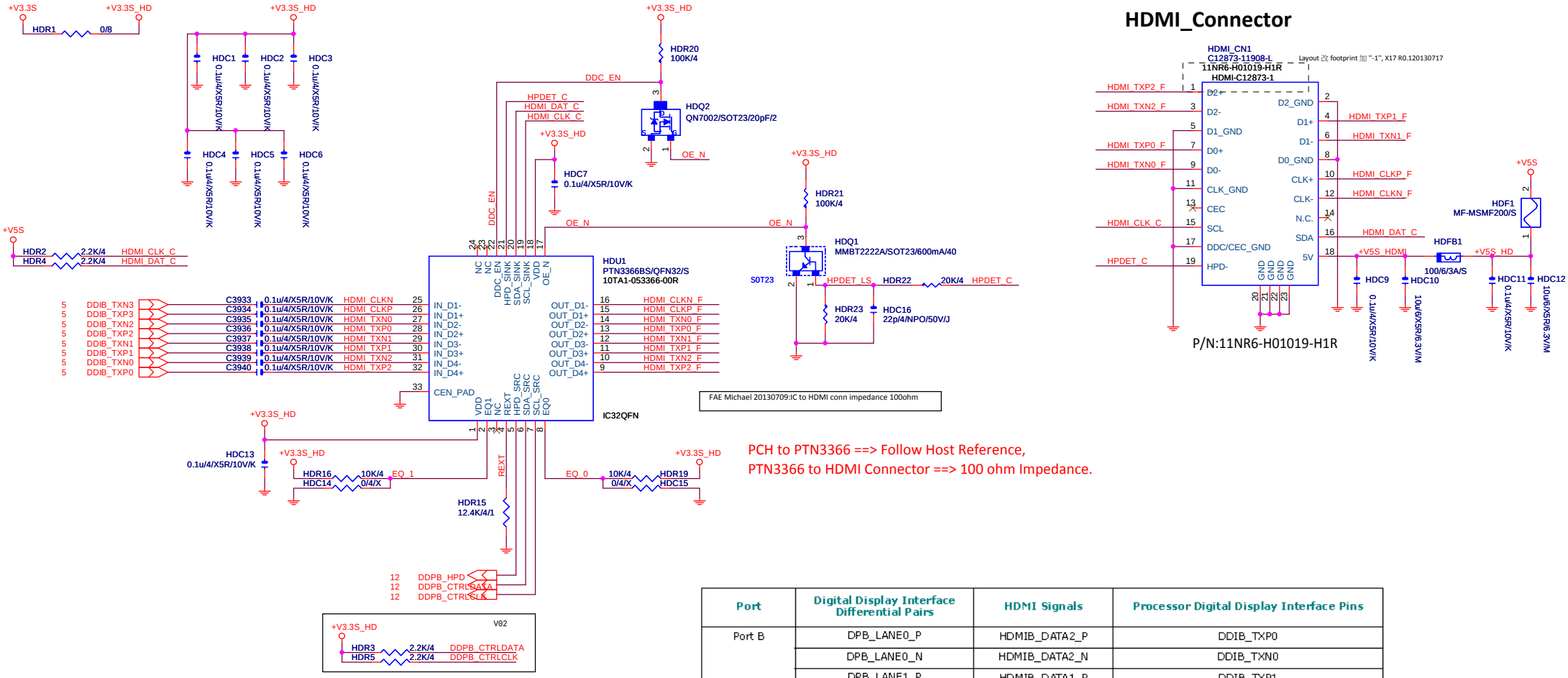

Port	Digital Display Interface Differential Pairs	HDMI Signals	Processor Digital Display Interface Pins
Port B	DPB_LANE0_P	HDMIB_DATA2_P	DDIB_TXP0
	DPB_LANE0_N	HDMIB_DATA2_N	DDIB_TXN0
	DPB_LANE1_P	HDMIB_DATA1_P	DDIB_TXP1
	DPB_LANE1_N	HDMIB_DATA1_N	DDIB_TXBN1
	DPB_LANE2_P	HDMIB_DATA0_P	DDIB_TXBP2
	DPB_LANE2_N	HDMIB_DATA0_N	DDIB_TXBN2
	DPB_LANE3_P	HDMIB_CK_P	DDIB_TXBP3
	DPB_LANE3_N	HDMIB_CK_N	DDIB_TXBN3
	DDPB_HPD	DDSP_1_HPD0	Hot plug detect used by HDMI Port B
	DDPB_CTRLCLK	DPB_CTRL_CK	HDMI DDC lines for Port B
	DDPB_CTRLDATA	DPB_CTRL_DATA	

7.7 Power management

PTN3366 implements innovative power management scheme whereby it achieves very low power consumption in both active and standby modes. Based on OE_N, DDC_EN, HPD_SNK, the PTN3366 intelligently optimizes the power consumption and disables outputs (OUT_Dx). Refer to Table 5.

Table 5. Power management schemes

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	don't care	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

GIGABYTE TECHNOLOGY COPORATION

Title: HDMI_Level_Shifter/Conn_1st

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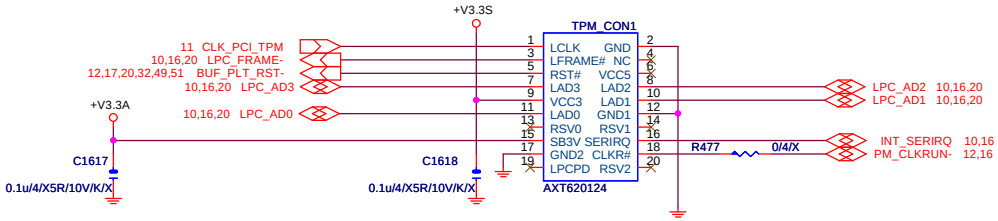
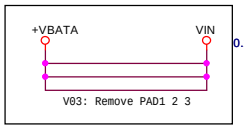
TPM Module



GIGABYTE TECHNOLOGY COPORATION

Title: TPM		
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 25 of 54	

ISL95812 3 Phase
VRM12.5 solution



put CPU side. put VR side.

U60 ISL95812HRZ-T/QFN32 ic32qfn-4x4P04

BOTTOM PAD CONNECT TO GND Through 8 VIAs

CLOSE TO Vcore LowSide MOSFET

Close PWM

CLOSE TO CHOKE

U61 ISL6208BCRZ/DFN8

CSD87350Q5D/SON8/S

Note:
X17
47W
Imax 85A, OCP
142.5Amp

Note:
1. V01_X17_20130410
use new choke
10LC4-30360C-03R 0.36uH/30A/S/H3 Chilisin
10.1*11.6*3mm DCR=1.6mOHM
2. V02_X17_20130830
Thermal test 4mm can low 5degreeC than 3mm, ask change Part, thus change from 3mm to 4mm heigh
1st:10LC4-30360C-02R CORE 0.36uH 30A PANASONIC
SMD 11.7*10 DCR 0.76mOHM~0.82mOhm
2nd: 10LC4-30360C-01R CORE 0.36uH 30A CYNTEC
SMD PCMC104T-R36MN DCR 1.05mOhm~1.2mOhm

GIGABYTE TECHNOLOGY COPORATION		
Title: VR12.5-ISL95812HRZ_T		
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
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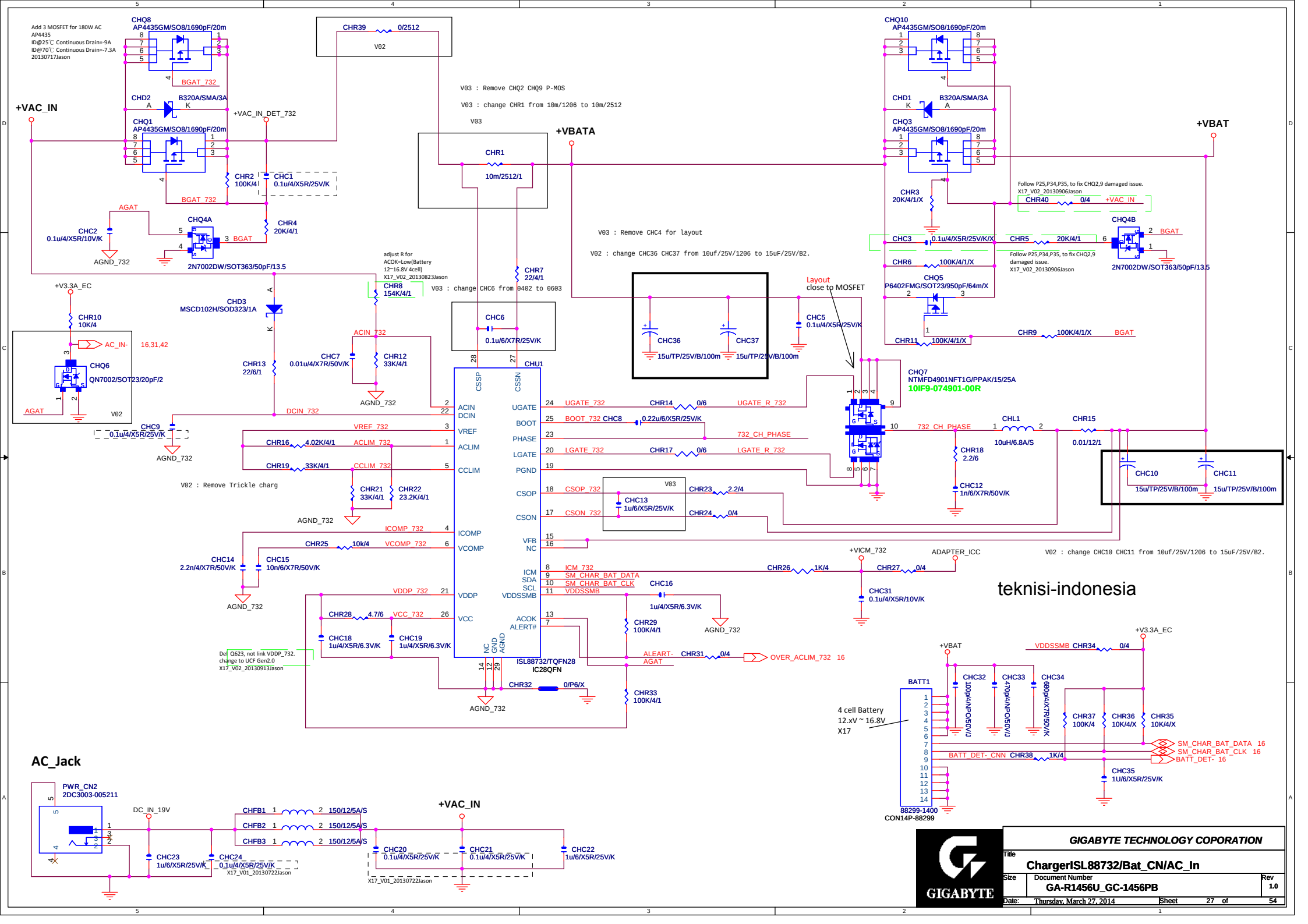
Add 3 MOSFET for 180W AC
AP4435
ID@25℃ Continuous Drain=-9A
ID@70℃ Continuous Drain=-7.3A
20130717Jason
CHQ8 AP4435GM/SO8/1690pF/20m
CHR39 0/2512
V02
V03 : Remove CHQ2 CHQ9 P-MOS
V03 : change CHR1 from 10m/1206 to 10m/2512
V03
CHQ10 AP4435GM/SO8/1690pF/20m
+VAC_IN
CHD2 B320A/SMA/3A
+VAC_IN_DET_732
CHQ1 AP4435GM/SO8/1690pF/20m
BGAT_732
CHR1 10m/2512/1
+VBATA
CHD1 B320A/SMA/3A
CHQ3 AP4435GM/SO8/1690pF/20m
+VBAT
CHR2 100K/4/1
CHC1 0.1u/4/X5R/25V/K
CHR3 20K/4/1/X
Follow P25,P34,P35, to fix CHQ2,9 damaged issue.
X17_V02_20130906Jason
CHR40 0/4 +VAC_IN
AGAT
CHC2 0.1u/4/X5R/10V/K
CHQ4A
CHR4 20K/4/1
2N7002DW/SOT363/50pF/13.5
V03 : Remove CHC4 for layout
V02 : change CHC36 CHC37 from 10uf/25V/1206 to 15uF/25V/B2.
CHC3 0.1u/4/X5R/25V/K/X
CHR5 20K/4/1
CHQ4B
CHR6 100K/4/1/X
CHQ5 P6402FMG/SOT23/950pF/64m/X
CHR11 100K/4/1/X
CHR9 100K/4/1/X
BGAT
adjust R for ACOK=Low(Battery 12~16.8V 4cell)
X17_V02_20130823Jason
CHR8 154K/4/1
V03 : change CHC6 from 0402 to 0603
CHR7 22/4/1
CHC6 0.1u/6/X7R/25V/K
CHC36 15u/TP/25V/B/100m
CHC37 15u/TP/25V/B/100m
CHC5 0.1u/4/X5R/25V/K
Layout close to MOSFET
+V3.3A_EC
CHR10 10K/4
AC_IN-
16,31,42
CHQ6 QN7002/SOT23/20pF/2
CHD3 MSCD102H/SOD323/1A
CHR13 22/6/1
CHC7 0.01u/4/X7R/50V/K
CHR12 33K/4/1
ACIN_732
DCIN_732
CHC9 0.1u/4/X5R/25V/K
CHU1
CSSP
CSSN
ACIN
DCIN
VREF
ACLIM
CCLIM
ICOMP
VCOMP
VDDP
VCC
UGATE
BOOT
PHASE
LGATE
PGND
CSOP
CSON
VFB
NC
ICM
SDA
SCL
VDDSSMB
ACOK
ALERT#
NC
GND
AGND
ISL88732/TQFN28
IC28QFN
UGATE_732
BOOT_732
LGATE_732
CSOP_732
CSON_732
VREF_732
ACLIM_732
CCLIM_732
ICOMP_732
VCOMP_732
VDDP_732
VCC_732
CHR14 0/6
CHR17 0/6
CHC8 0.22u/6/X5R/25V/K
732_CH_PHASE
UGATE_R_732
LGATE_R_732
CHQ7 NTMFD4901NFT1G/PPAK/15/25A
10IF9-074901-00R
CHL1 10uH/6.8A/S
CHR15 0.01/12/1
CHR18 2.2/6
CHC12 1n/6/X7R/50V/K
CHC10 15u/TP/25V/B/100m
CHC11 15u/TP/25V/B/100m
V02 : Remove Trickle charg
CHR16 4.02K/4/1
CHR19 33K/4/1
CHR21 33K/4/1
CHR22 23.2K/4/1
V03
CHC13 1u/6/X5R/25V/K
CHR23 2.2/4
CHR24 0/4
CHC14 2.2n/4/X7R/50V/K
CHC15 10n/6/X7R/50V/K
CHR25 10k/4
V02 : change CHC10 CHC11 from 10uf/25V/1206 to 15uF/25V/B2.
+VICM_732
ADAPTER_ICC
CHR26 1K/4
CHR27 0/4
CHC31 0.1u/4/X5R/10V/K
ICM_732
SM_CHAR_BAT_DATA
SM_CHAR_BAT_CLK
VDDSSMB
CHC16 1u/4/X5R/6.3V/K
CHR28 4.7/6
CHC18 1u/4/X5R/6.3V/K
CHC19 1u/4/X5R/6.3V/K
CHR29 100K/4/1
Del Q623, not link VDDP_732. change to UCF Gen2.0
X17_V02_20130913Jason
ALEART-
AGAT
CHR31 0/4
OVER_ACLIM_732 16
CHR32 0/P6/X
CHR33 100K/4/1
teknisi-indonesia
+V3.3A_EC
+VBAT
VDDSSMB CHR34 0/4
BATT1
CHC32 100p/4/NPO/50V/J
CHC33 470p/4/NPO/50V/J
CHC34 680p/4/X7R/50V/K
CHR37 100K/4
CHR36 10K/4/X
CHR35 10K/4/X
SM_CHAR_BAT_DATA 16
SM_CHAR_BAT_CLK 16
BATT_DET- 16
BATT_DET- CNN CHR38 1K/4
CHC35 1U/6/X5R/25V/K
4 cell Battery
12.xV ~ 16.8V
X17
88299-1400
CON14P-88299
AC_Jack
PWR_CN2
2DC3003-005211
DC_IN_19V
CHFB1 150/12/5A/S
CHFB2 150/12/5A/S
CHFB3 150/12/5A/S
CHC23 1u/6/X5R/25V/K
CHC24 0.1u/4/X5R/25V/K
X17_V01_20130722Jason
+VAC_IN
CHC20 0.1u/4/X5R/25V/K
CHC21 0.1u/4/X5R/25V/K
CHC22 1u/6/X5R/25V/K
x17_V01_20130722Jason
GIGABYTE TECHNOLOGY COPORATION
Title
ChargerISL88732/Bat_CN/AC_In
Size
Document Number
GA-R1456U_GC-1456PB
Rev
1.0
Date: Thursday, March 27, 2014
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change from +V5A to +V5A_MAP
X17_V02_20131003Jason

+V5A_MPS

Q34

AP4435GM/SO8/1690pF/20m

+V5S

+V5S

+ CL72

100u/TP/6.3V/B/35m

PWR_init

R347

100k/4

C1853

1u/4/X5R/6.3V/K

C306

0.1u/6/X7R/25V/K

PS_S3CNTRL

R348

1K/4

Q30

QN7002/SOT23/20pF/2

R353

1M/4

12,16,19 PM_SLP_S3-

change from +V5A to +V5A_MAP
X17_V02_20131003Jason

+V5A_MPS

C1861

10u/6/X5R/6.3V/M

C1860

2.2u/4/X5R/6.3V/M

C1859

0.1u/4/Y5V/25V/Z

change from +V3.3A to +V3.3A_DSW
X17_V02_20131003Jason

+V3.3A_DSW

change from AP0903 to 3707 small size
X17_V02_20131003Jason

+V3.3M

Q17

ic8pqfn

10IF9-072800-00R

10IF9-073702-00R

IRFH3707PBF/QFN3*3/755pF/12.4m

PWR_init

R271

100K/4/1

R1905

0/4

C2371

0.1u/6/X7R/25V/K/X

C214

0.1u/6/X7R/25V/K/X

PWR_init

R270

100K/4/1

Q15A

2N7002DW/SOT363/50pF/13.5

EC_EN_V33M_R

R2054

0/4

Q15B

2N7002DW/SOT363/50pF/13.5

Q668

QN7002/SOT23/20pF/2

12,30 PM_SLP_A-

+V3.3A_KSC

R272

100K/4

16 EC_EN_V33M

預留給 Mirror時 EC status
unknow, 無法來開 +V3.3M.
X17_V01_20130716

UCF Gen2.0
X17_V02_20130918Jason

+V5A_MPS

+V5A

Q652

PWR_init

C2289

1u/4/X5R/6.3V/K

NTMFS4935N/N/3.2mm/PPAKSO8

PWR_init

R1944

100K/4

R1942

0/4

C2245

0.1u/4/X5R/16V/K

R1945

100K/4

Q7100A

2N7002DW/SOT363/50pF/13.5

C2290

0.1u/6/X7R/25V/K

Q7100B

2N7002DW/SOT363/50pF/13.5

R1943

0/4

16,29 USB_V5A_EN_EC

PWR_init

R256

200K/4/1

+V3.3A

Q14

AP0903GM/SO8/600pF/8.5m

+V3.3S

+V3.3S

+ CL73

100u/TP/6.3V/B/35m

C1852

1u/4/X5R/6.3V/K

R263

1K/4

C226

0.1u/6/X7R/25V/K

Q16

QN7002/SOT23/20pF/2

PS_S3CNTRL

+V1.05M

PWR_init

220uF x 2(1of2 on PWM) for
+V1.05M to fix softatrt issue.

CL75

220u/TP/2.5V/B2/15m

C1850

1u/4/X5R/6.3V/K

Q35

+V1.05S

NTMFS4935N/N/3.2mm/PPAKSO8

+V1.05S

R333

200K/4/1

R340

10K/4

C312

C305

C310

0.1u/4/Y5V/25V/Z

C294

0.1u/6/X7R/25V/K

Q29

QN7002/SOT23/20pF/2

PS_S3CNTRL

Discharge

rename +VCC_CORE to +VCCIN
X17_V02_20131015Jason

+VCCIN

PWR_init

R30

100K/4/X

PM_SLP_S3

Q22

PM_SLP_S3- 1

QN7002/SOT23/20pF/2/X

R27

1M/4/X

C1057

0.1u/4/Y5V/25V/Z/X

+V1.5S_PCH

+V5S

R444

120/6/X

Q124

QN7002/SOT23/20pF/2/X

R2002

120/6/X

Q656

QN7002/SOT23/20pF/2/X

R445

180/6/X

Q98

QN7002/SOT23/20pF/2/X

+V1.05S

+V3.3M

+V3.3S

R32

120/6/X

Q65

QN7002/SOT23/20pF/2/X

R672

120/6/X

Q97

QN7002/SOT23/20pF/2/X

R443

120/6/X

Q123

QN7002/SOT23/20pF/2/X

All NA
X17_V02_20130926Jason

D3

+V3.3A_DSW

X17_V02_20131016Jason

+V3.3A

PWR_init

R1949

0/12/X

R1920

0/12/X

R1921

100K/4

C2287

1u/4/X5R/6.3V/K

Q649

NTMFS4935N/N/3.2mm/PPAKSO8

R1922

0/4

Q649_G

PWR_init

C2288

0.1u/6/X7R/25V/K

R1923

100K/4

Q650A

rename Q7099S to Q650A
X17_V02_20131008Jason

2N7002DW/SOT363/50pF/13.5

Q650B_D

Q650B

2N7002DW/SOT363/50pF/13.5

R1929

10K/4

X17_V02_20131003Jason

16 +V3.3A_EN

R1928

0/4

+V3.3A_EN_R

12,16 PM_SLP_SUS-

R1924

0/4/X

+V3.3S

+V1.5S_PCH

+V1.5S_PCH

U39

RT9018B-18GSP/SO8/3A

R1132

1K/4

R1131

1K/4

GD_9018

EN_9018

+V3.3S

PGD

EN

VIN

VDD

GND

ADJ

VOUT

NC

ADJ_9018

+V5S

C1731

10u/6/X5R/6.3V/M

C1730

0.1u/4/Y5V/25V/Z/X

C1802

10u/6/X5R/6.3V/M

C1801

0.1u/4/Y5V/25V/Z/X

R823

9.1K/4/1

R822

10K/4/1

+V1.5S_PCH

C1733

C1734

C1735

C1736

10u/6/X5R/6.3V/M

0.1u/4/Y5V/25V/Z

0.1u/4/Y5V/25V/Z

V01 reserve 0.1u x 4, PWR_init to GND
no need, del them
X17_V02_20130829Jason

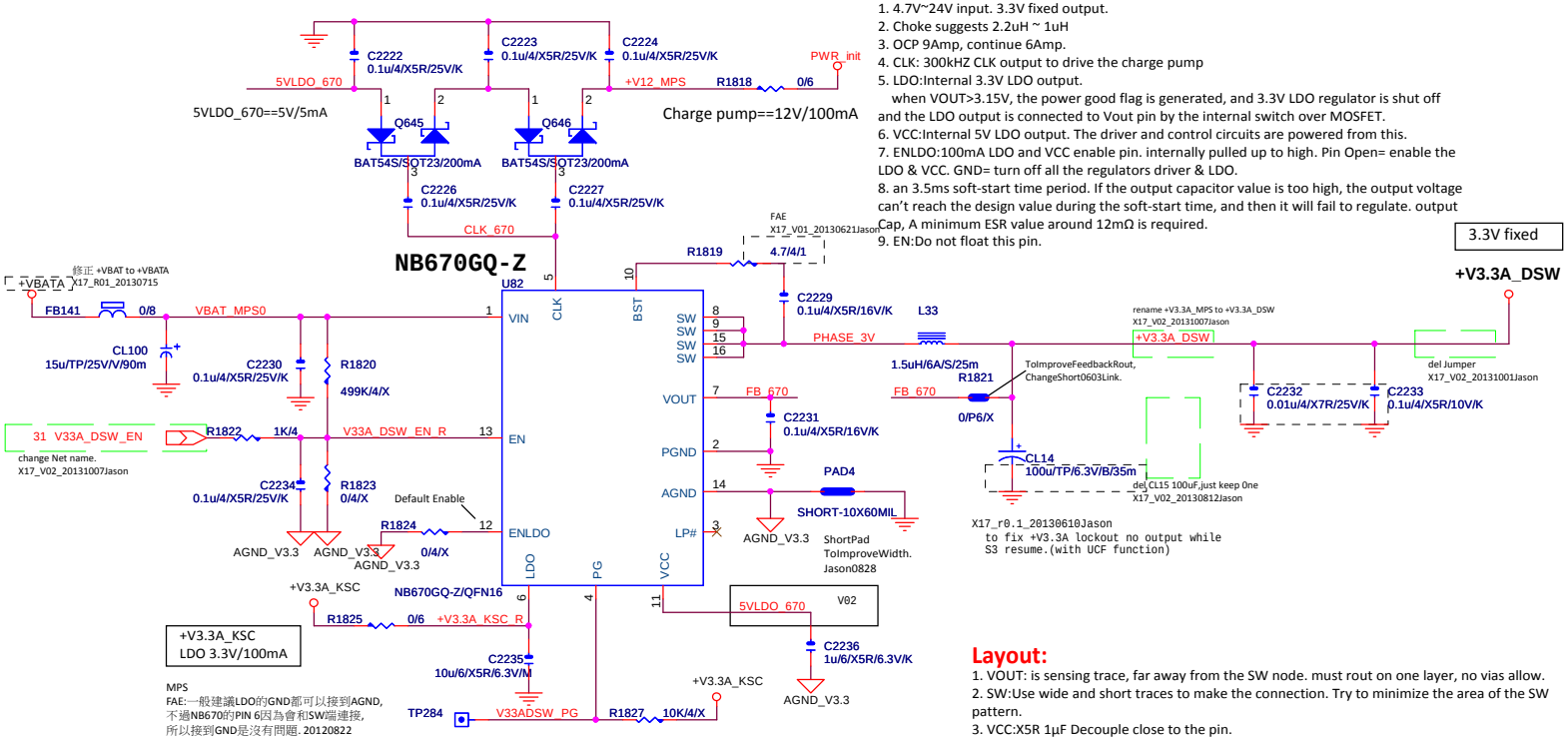
GIGABYTE

GIGABYTE TECHNOLOGY COPORATION

Title: System_Power/Discharge/+V1.5S_PCH

Size: | Document Number: GA-R1456U_GC-1456PB | Rev: 1.0

Date: Thursday, March 27, 2014 | Sheet 28 of 54

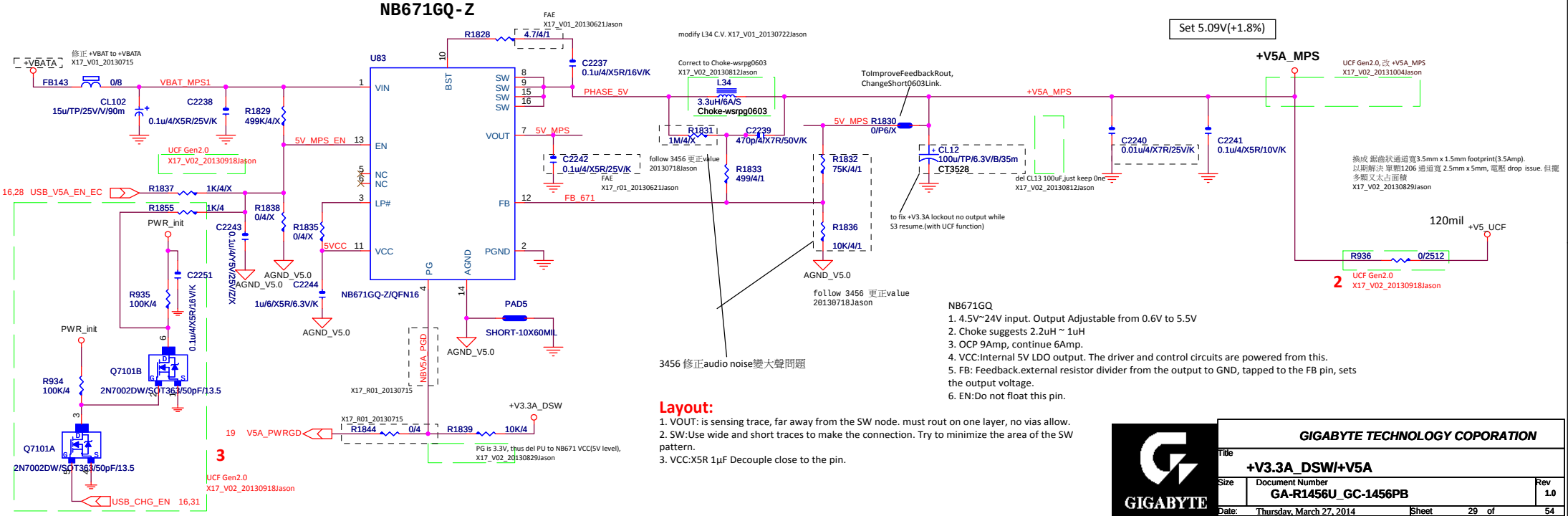


NB670GQ

1. 4.7V~24V input. 3.3V fixed output.
2. Choke suggests 2.2uH ~ 1uH
3. OCP 9Amp, continue 6Amp.
4. CLK: 300kHZ CLK output to drive the charge pump
5. LDO:Internal 3.3V LDO output.
   when VOUT>3.15V, the power good flag is generated, and 3.3V LDO regulator is shut off and the LDO output is connected to Vout pin by the internal switch over MOSFET.
6. VCC:Internal 5V LDO output. The driver and control circuits are powered from this.
7. ENLDO:100mA LDO and VCC enable pin. internally pulled up to high. Pin Open= enable the LDO & VCC. GND= turn off all the regulators driver & LDO.
8. an 3.5ms soft-start time period. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. output cap, A minimum ESR value around 12mΩ is required.
9. EN:Do not float this pin.

Layout:

1. VOUT: is sensing trace, far away from the SW node. must rout on one layer, no vias allow.
2. SW:Use wide and short traces to make the connection. Try to minimize the area of the SW pattern.
3. VCC:X5R 1μF Decouple close to the pin.



NB671GQ

1. 4.5V~24V input. Output Adjustable from 0.6V to 5.5V
2. Choke suggests 2.2uH ~ 1uH
3. OCP 9Amp, continue 6Amp.
4. VCC:Internal 5V LDO output. The driver and control circuits are powered from this.
5. FB: Feedback.external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
6. EN:Do not float this pin.

Layout:

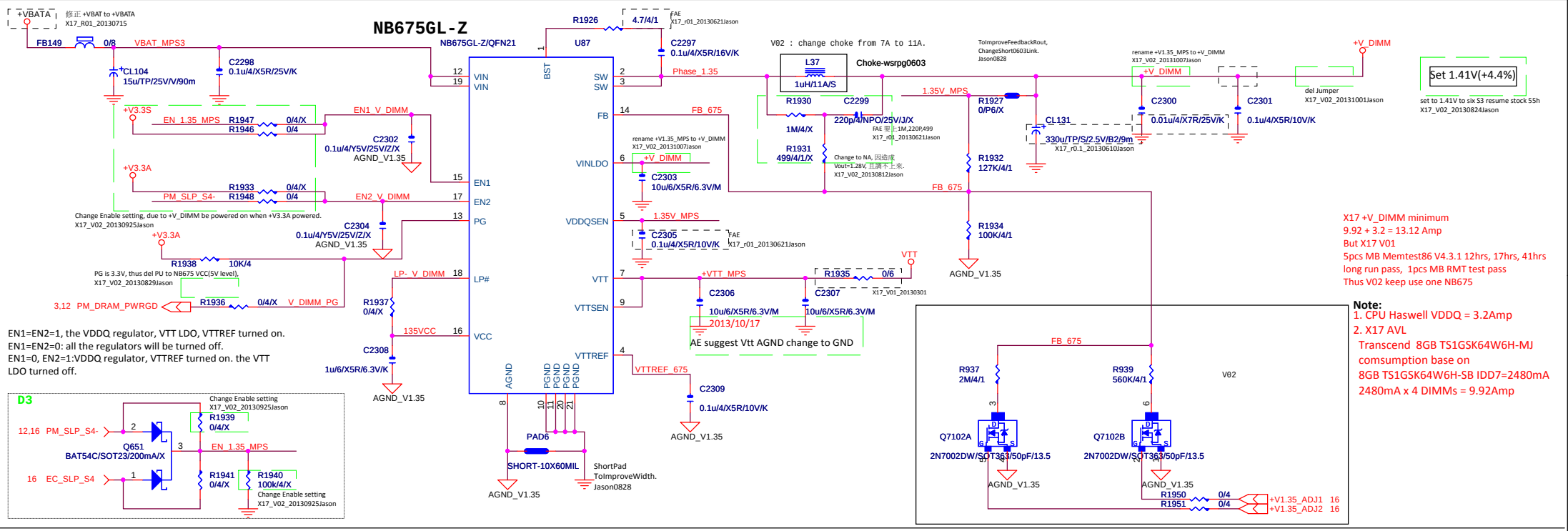
1. VOUT: is sensing trace, far away from the SW node. must rout on one layer, no vias allow.
2. SW:Use wide and short traces to make the connection. Try to minimize the area of the SW pattern.
3. VCC:X5R 1μF Decouple close to the pin.

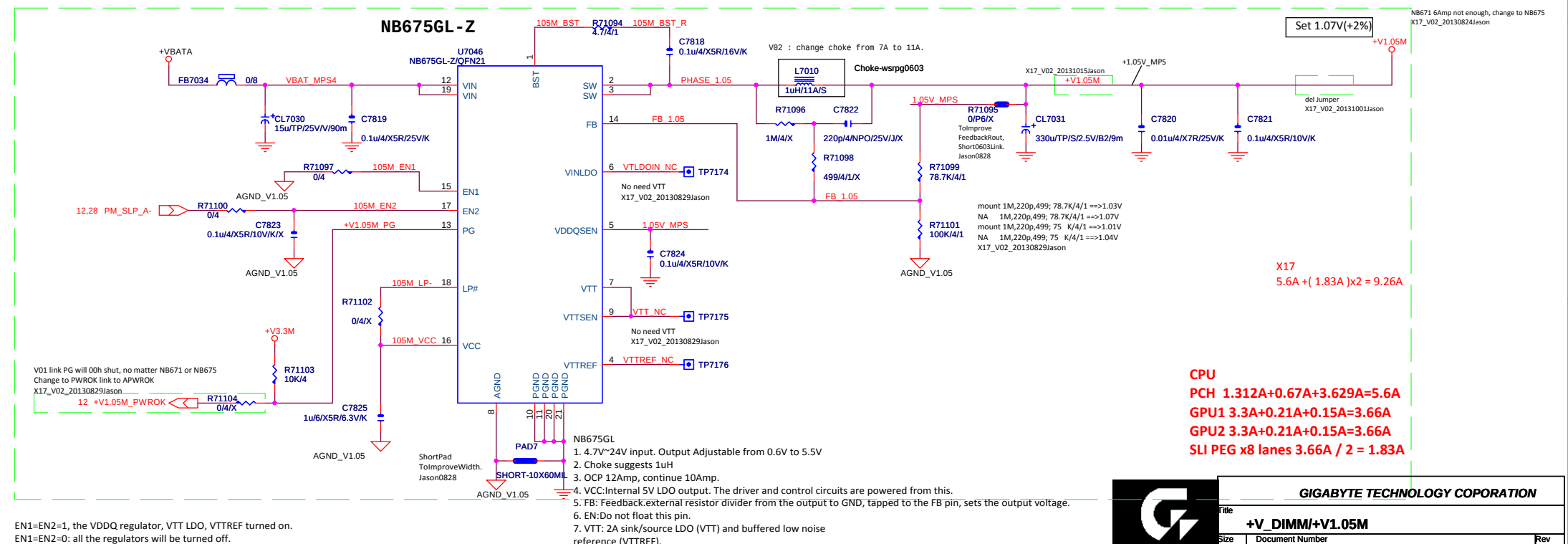
GIGABYTE TECHNOLOGY COPORATION

Title: +V3.3A_DSW/+V5A

Size	Document Number	Rev
	GA-R1456U_GC-1456PB	1.0

Date: Thursday, March 27, 2014 Sheet 29 of 54





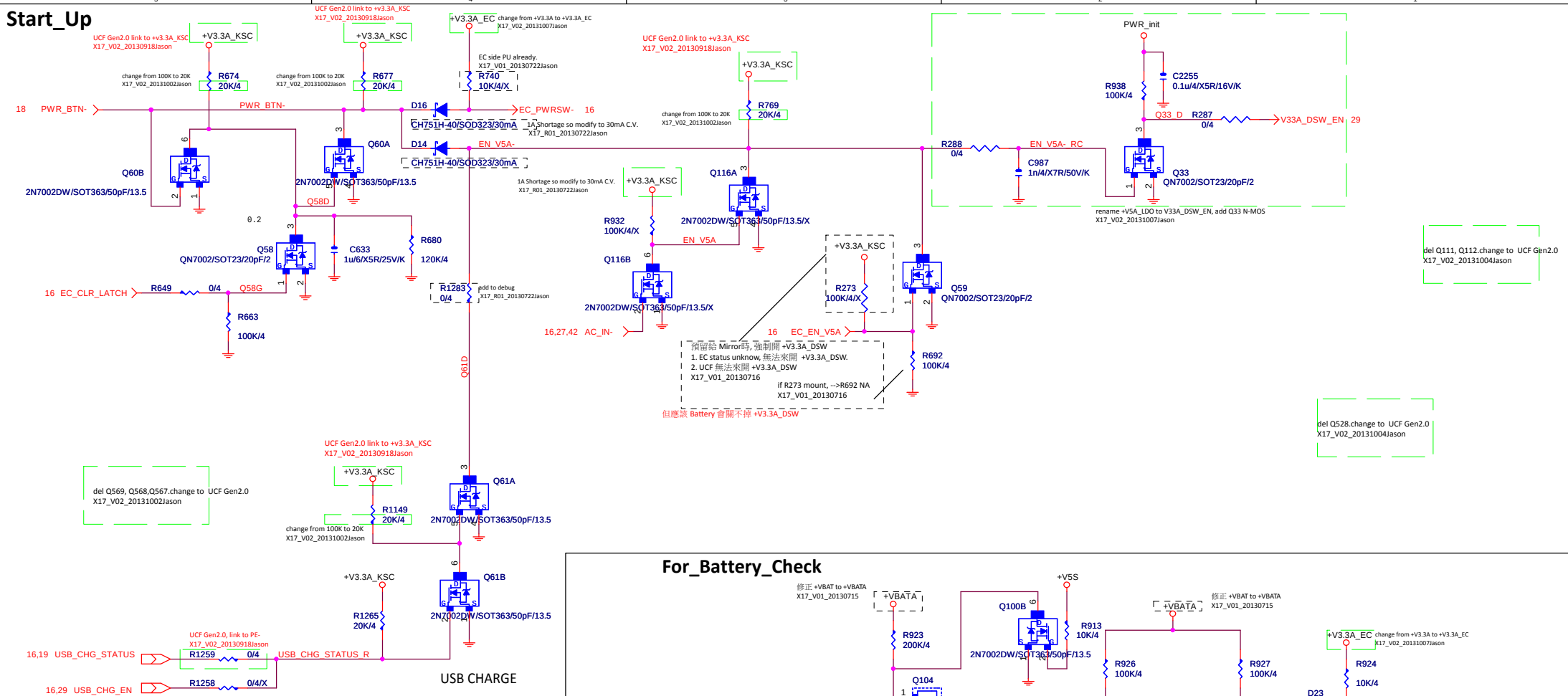
NB675GL
1. 4.7V~24V input. Output Adjustable from 0.6V to 5.5V
2. Choke suggests 1uH
3. OCP 12Amp, continue 10Amp.
4. VCC:Internal 5V LDO output. The driver and control circuits are powered from this.
5. FB: Feedback.external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage.
6. EN:Do not float this pin.
7. VTT: 2A sink/source LDO (VTT) and buffered low noise reference (VTTREF).
8. VINLDO:VTT LDO regulator input.Connect to VDDQ.
9. VDDQSEN:Buck regulator output voltage sense. Connect this pin to the output capacitor of the regulator directly

EN1=EN2=1, the VDDQ regulator, VTT LDO, VTTREF turned on.
EN1=EN2=0: all the regulators will be turned off.
EN1=0, EN2=1:VDDQ regulator, VTTREF turned on. the VTT LDO turned off.

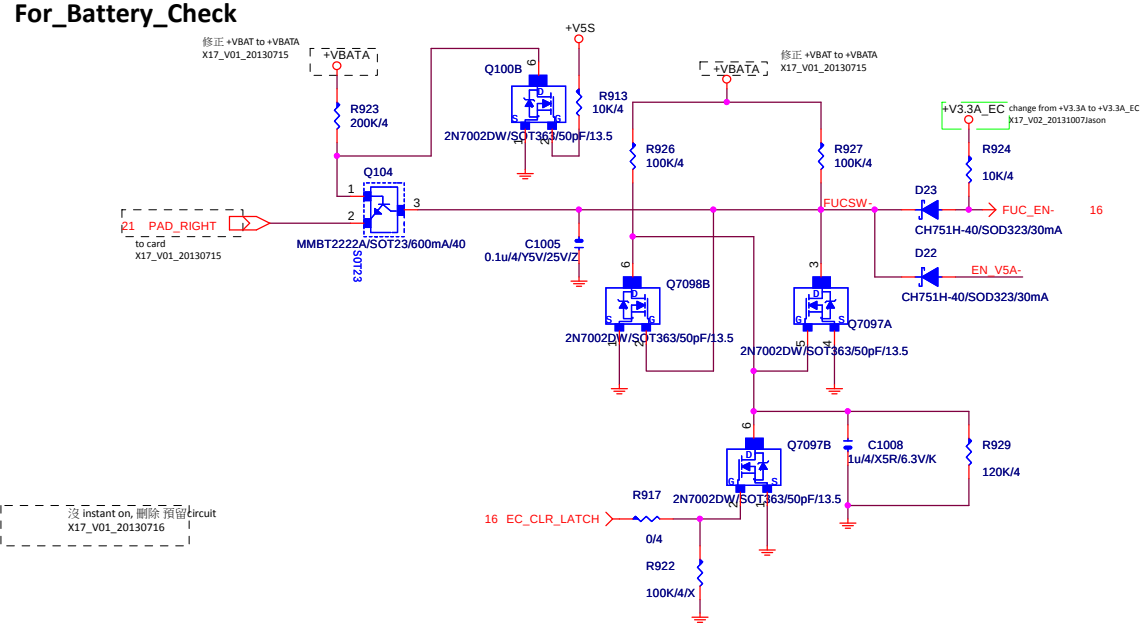
GIGABYTE TECHNOLOGY COPORATION

Title	+V_DIMM/+V1.05M	
Size	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
Date: Thursday, March 27, 2014	Sheet 30 of 54	

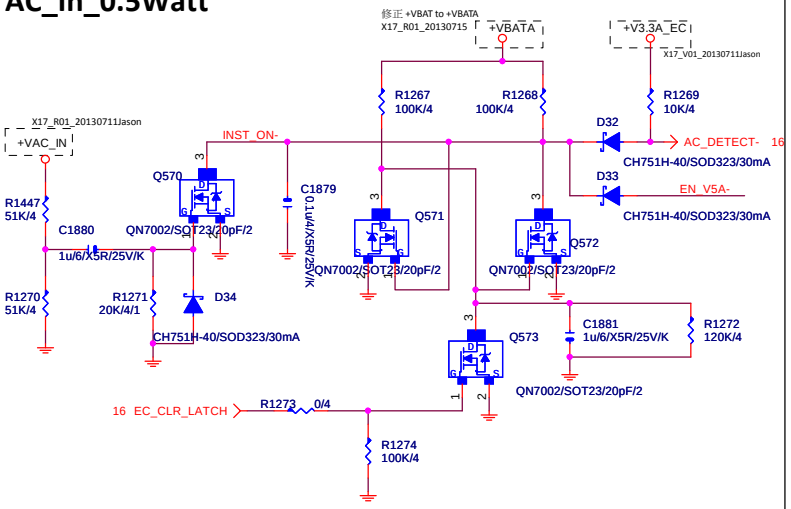
Start_Up

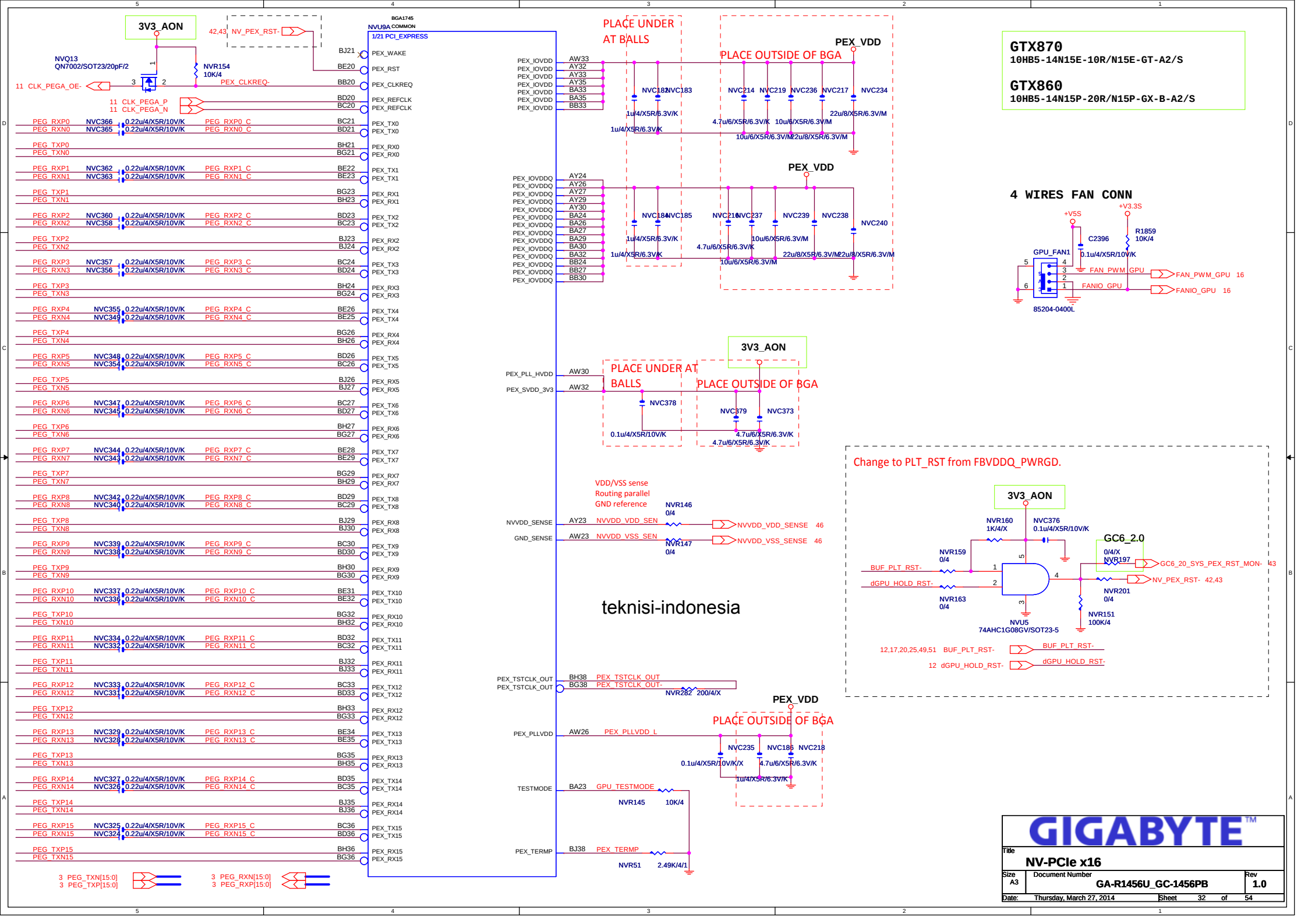


For_Battery_Check



AC_In_0.5Watt




3V3_AON
NVQ13
QN7002/SOT23/20pF/2
NVR154
10K/4
11 CLK_PEGA_OE-
42,43 NV_PEX_RST-
PEX_CLKREQ-
11 CLK_PEGA_P
11 CLK_PEGA_N
BGA1745
NVU9A COMMON
1/21 PCI_EXPRESS
PEX_WAKE
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_REFCLK
PEG_RXP0 NVC366 0.22u/4/X5R/10V/K PEG_RXP0_C
PEG_RXN0 NVC365 0.22u/4/X5R/10V/K PEG_RXN0_C
PEG_TXP0
PEG_TXN0
PEG_RXP1 NVC362 0.22u/4/X5R/10V/K PEG_RXP1_C
PEG_RXN1 NVC363 0.22u/4/X5R/10V/K PEG_RXN1_C
PEG_TXP1
PEG_TXN1
PEG_RXP2 NVC360 0.22u/4/X5R/10V/K PEG_RXP2_C
PEG_RXN2 NVC358 0.22u/4/X5R/10V/K PEG_RXN2_C
PEG_TXP2
PEG_TXN2
PEG_RXP3 NVC357 0.22u/4/X5R/10V/K PEG_RXP3_C
PEG_RXN3 NVC356 0.22u/4/X5R/10V/K PEG_RXN3_C
PEG_TXP3
PEG_TXN3
PEG_RXP4 NVC355 0.22u/4/X5R/10V/K PEG_RXP4_C
PEG_RXN4 NVC349 0.22u/4/X5R/10V/K PEG_RXN4_C
PEG_TXP4
PEG_TXN4
PEG_RXP5 NVC348 0.22u/4/X5R/10V/K PEG_RXP5_C
PEG_RXN5 NVC354 0.22u/4/X5R/10V/K PEG_RXN5_C
PEG_TXP5
PEG_TXN5
PEG_RXP6 NVC347 0.22u/4/X5R/10V/K PEG_RXP6_C
PEG_RXN6 NVC345 0.22u/4/X5R/10V/K PEG_RXN6_C
PEG_TXP6
PEG_TXN6
PEG_RXP7 NVC344 0.22u/4/X5R/10V/K PEG_RXP7_C
PEG_RXN7 NVC343 0.22u/4/X5R/10V/K PEG_RXN7_C
PEG_TXP7
PEG_TXN7
PEG_RXP8 NVC342 0.22u/4/X5R/10V/K PEG_RXP8_C
PEG_RXN8 NVC340 0.22u/4/X5R/10V/K PEG_RXN8_C
PEG_TXP8
PEG_TXN8
PEG_RXP9 NVC339 0.22u/4/X5R/10V/K PEG_RXP9_C
PEG_RXN9 NVC338 0.22u/4/X5R/10V/K PEG_RXN9_C
PEG_TXP9
PEG_TXN9
PEG_RXP10 NVC337 0.22u/4/X5R/10V/K PEG_RXP10_C
PEG_RXN10 NVC336 0.22u/4/X5R/10V/K PEG_RXN10_C
PEG_TXP10
PEG_TXN10
PEG_RXP11 NVC334 0.22u/4/X5R/10V/K PEG_RXP11_C
PEG_RXN11 NVC332 0.22u/4/X5R/10V/K PEG_RXN11_C
PEG_TXP11
PEG_TXN11
PEG_RXP12 NVC333 0.22u/4/X5R/10V/K PEG_RXP12_C
PEG_RXN12 NVC331 0.22u/4/X5R/10V/K PEG_RXN12_C
PEG_TXP12
PEG_TXN12
PEG_RXP13 NVC329 0.22u/4/X5R/10V/K PEG_RXP13_C
PEG_RXN13 NVC328 0.22u/4/X5R/10V/K PEG_RXN13_C
PEG_TXP13
PEG_TXN13
PEG_RXP14 NVC327 0.22u/4/X5R/10V/K PEG_RXP14_C
PEG_RXN14 NVC326 0.22u/4/X5R/10V/K PEG_RXN14_C
PEG_TXP14
PEG_TXN14
PEG_RXP15 NVC325 0.22u/4/X5R/10V/K PEG_RXP15_C
PEG_RXN15 NVC324 0.22u/4/X5R/10V/K PEG_RXN15_C
PEG_TXP15
PEG_TXN15
PEX_TX0
PEX_TX0
PEX_RX0
PEX_RX0
PEX_TX1
PEX_TX1
PEX_RX1
PEX_RX1
PEX_TX2
PEX_TX2
PEX_RX2
PEX_RX2
PEX_TX3
PEX_TX3
PEX_RX3
PEX_RX3
PEX_TX4
PEX_TX4
PEX_RX4
PEX_RX4
PEX_TX5
PEX_TX5
PEX_RX5
PEX_RX5
PEX_TX6
PEX_TX6
PEX_RX6
PEX_RX6
PEX_TX7
PEX_TX7
PEX_RX7
PEX_RX7
PEX_TX8
PEX_TX8
PEX_RX8
PEX_RX8
PEX_TX9
PEX_TX9
PEX_RX9
PEX_RX9
PEX_TX10
PEX_TX10
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PEX_TX12
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PEX_RX13
PEX_RX13
PEX_TX14
PEX_TX14
PEX_RX14
PEX_RX14
PEX_TX15
PEX_TX15
PEX_RX15
PEX_RX15
3 PEG_TXN[15:0]
3 PEG_TXP[15:0]
3 PEG_RXN[15:0]
3 PEG_RXP[15:0]
PLACE UNDER AT BALLS
PLACE OUTSIDE OF BGA
PEX_VDD
PEX_IOVDD
AW33
AY32
AY33
AY35
BA33
BA35
BB33
NVC182 NVC183
1u/4/X5R/6.3V/K
NVC214 NVC219 NVC236 NVC217 NVC234
4.7u/6/X5R/6.3V/K
10u/6/X5R/6.3V/M
22u/8/X5R/6.3V/M
PEX_IOVDDQ
AY24
AY26
AY27
AY29
AY30
BA24
BA26
BA27
BA29
BA30
BA32
BB24
BB27
BB30
NVC184 NVC185
NVC216 NVC237 NVC239 NVC238
NVC240
PEX_PLL_HVDD
AW30
PEX_SVDD_3V3
AW32
3V3_AON
NVC378
NVC379 NVC373
0.1u/4/X5R/10V/K
4.7u/6/X5R/6.3V/K
VDD/VSS sense
Routing parallel
GND reference
NVVDD_SENSE
AY23 NVVDD_VDD_SEN
NVR146
0/4
NVVDD_VDD_SENSE 46
GND_SENSE
AW23 NVVDD_VSS_SEN
NVR147
0/4
NVVDD_VSS_SENSE 46
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PEX_TSTCLK_OUT
BH38 PEX_TSTCLK_OUT
PEX_TSTCLK_OUT-
BG38 PEX_TSTCLK_OUT-
NVR282 200/4/X
PEX_PLLVDD
AW26 PEX_PLLVDD_L
NVC235 NVC186 NVC218
0.1u/4/X5R/10V/K/X
4.7u/6/X5R/6.3V/K
1u/4/X5R/6.3V/K
TESTMODE
BA23 GPU_TESTMODE
NVR145 10K/4
PEX_TERMP
BJ38 PEX_TERMP
NVR51 2.49K/4/1
GTX870
10HB5-14N15E-10R/N15E-GT-A2/S
GTX860
10HB5-14N15P-20R/N15P-GX-B-A2/S
4 WIRES FAN CONN
+V5S
+V3.3S
C2396
0.1u/4/X5R/10V/K
R1859
10K/4
GPU_FAN1
FAN_PWM_GPU
FANIO_GPU
FAN_PWM_GPU 16
FANIO_GPU 16
85204-0400L
Change to PLT_RST from FBVDDQ_PWRGD.
3V3_AON
NVR160
1K/4/X
NVC376
0.1u/4/X5R/10V/K
GC6_2.0
0/4/X
NVR197
BUF_PLT_RST-
dGPU_HOLD_RST-
NVR159
0/4
NVR163
0/4
GC6_20_SYS_PEX_RST_MON- 43
NV_PEX_RST- 42,43
NVR201
0/4
NVR151
100K/4
NVU5
74AHC1G08GV/SOT23-5
12,17,20,25,49,51 BUF_PLT_RST-
12 dGPU_HOLD_RST-
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NV-PCIe x16
Size A3
Document Number
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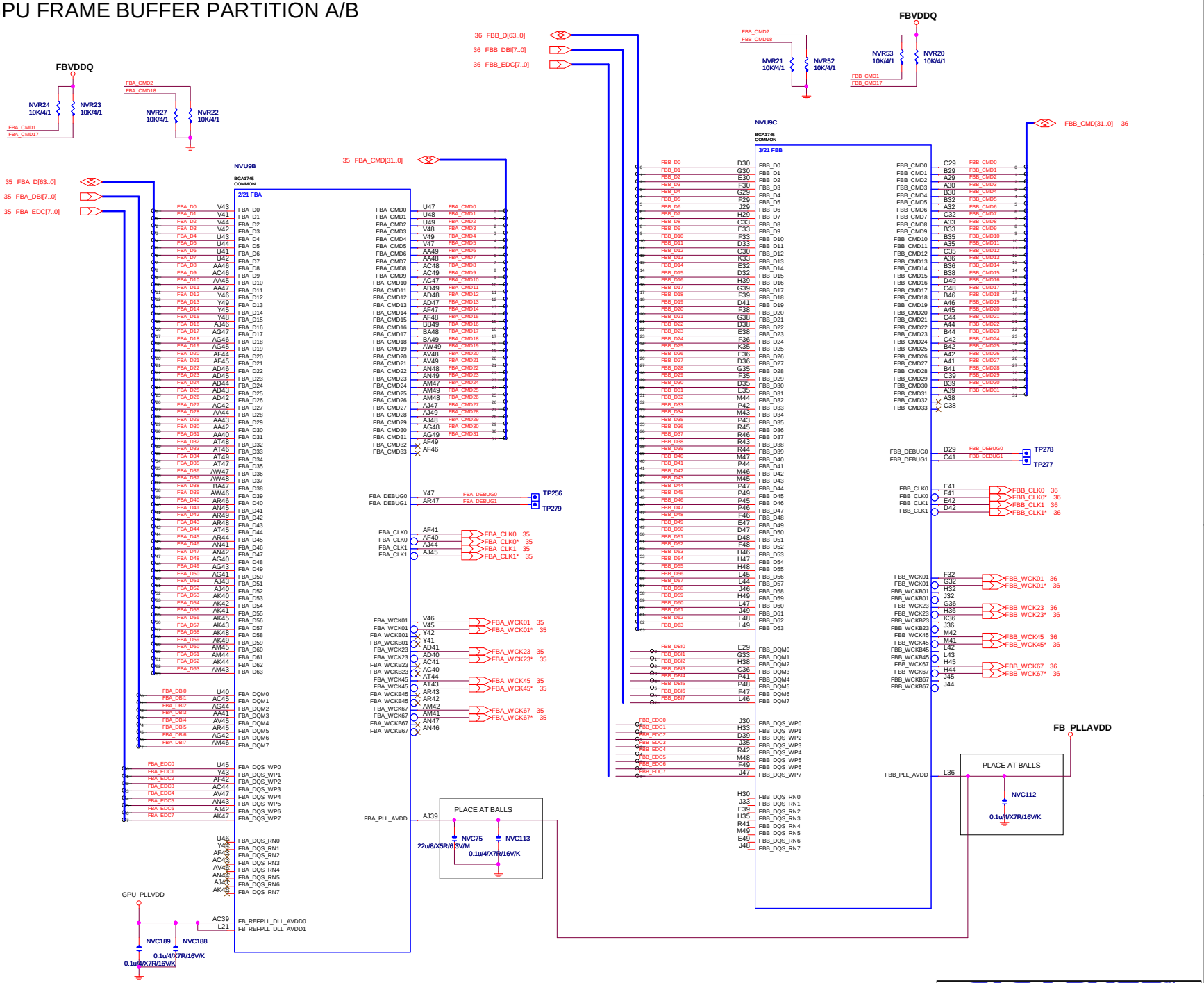
GPU FRAME BUFFER PARTITION A/B



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Title	NV-FB Partit A/B	
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GPU FRAME BUFFER PARTITION C

	0..31	32..63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

For GTX870 Design,the FB_PLL_AVDD not need power input for partition D.

NVR287,NVC422 no insert.

Title	NV-FB Partit C		
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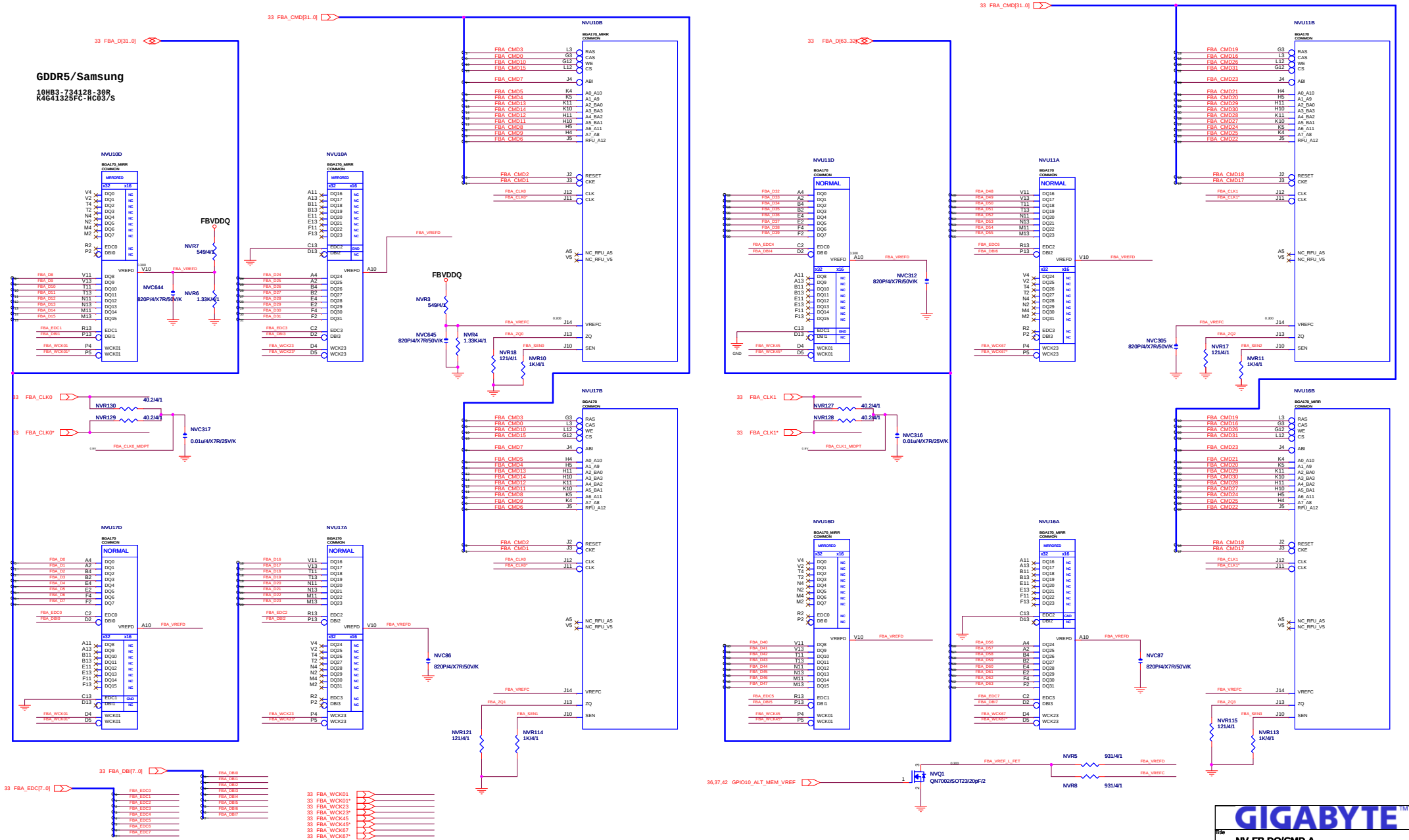
PAGE4: FRAME BUFFER PARTITION A



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Title	NV-FB DQ/CMD A	
Size: Custom	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
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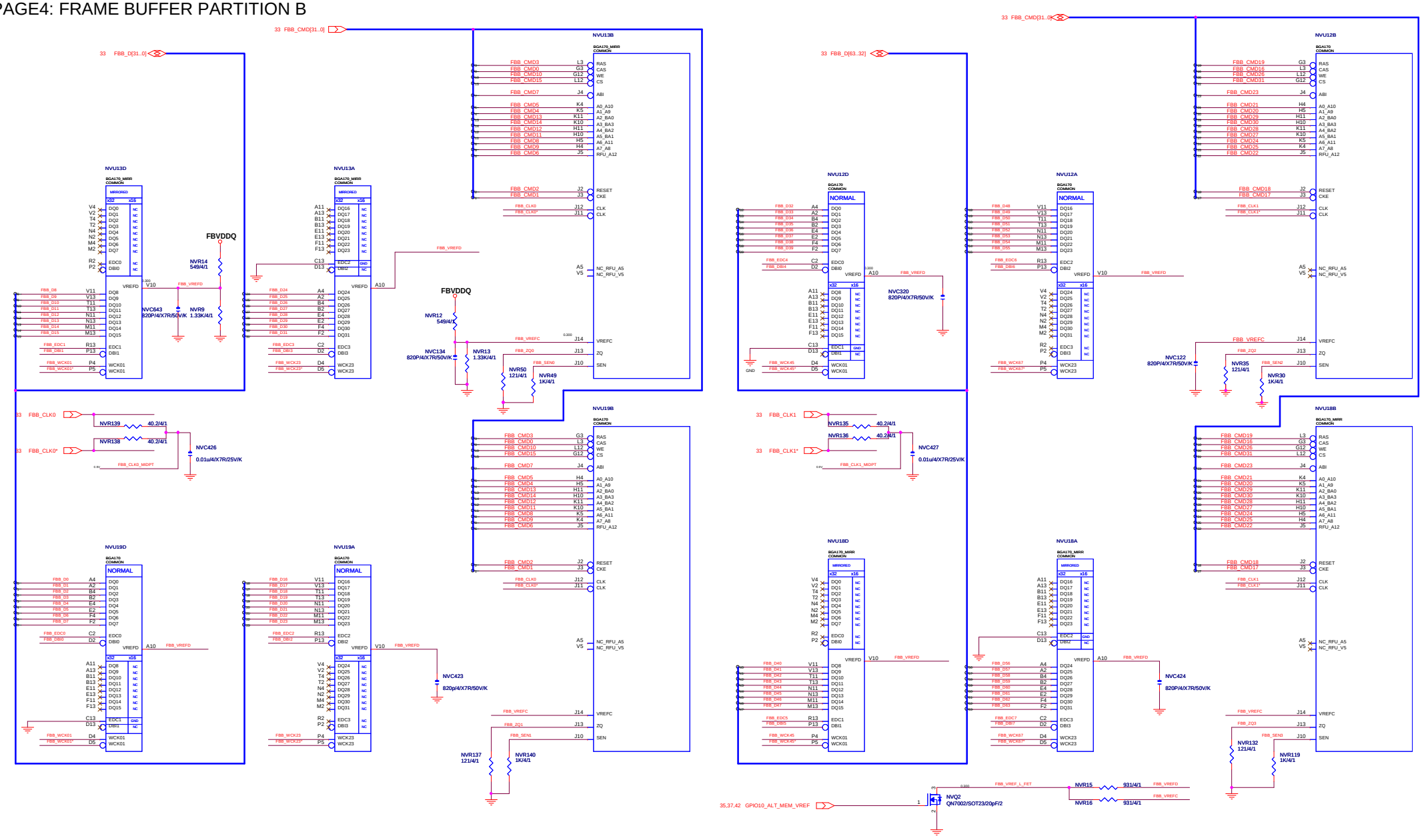
PAGE4: FRAME BUFFER PARTITION B



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Title	NV-FB DQ/CMD B		
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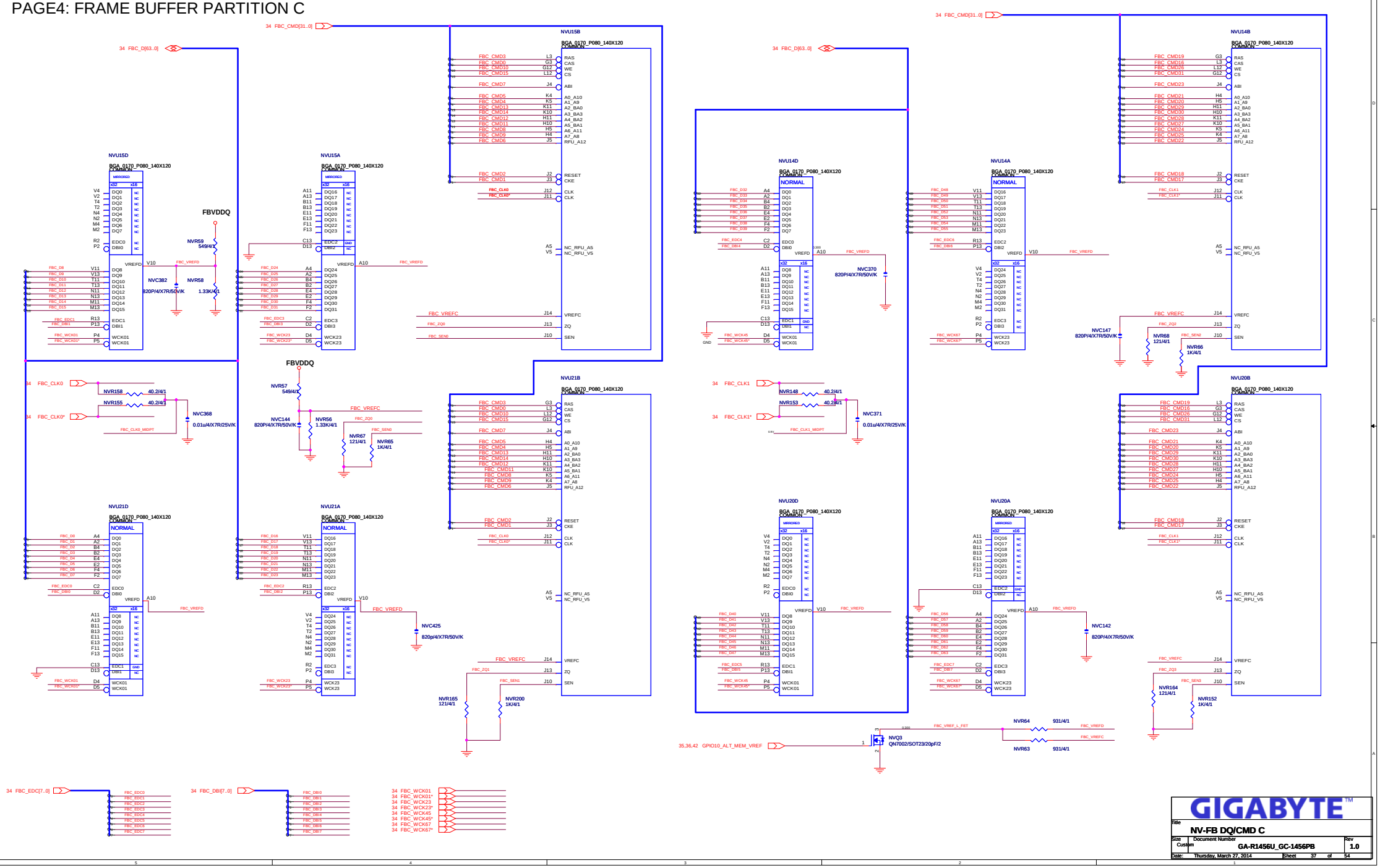
PAGE4: FRAME BUFFER PARTITION C



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Title	NV-FB DQ/CMD C	
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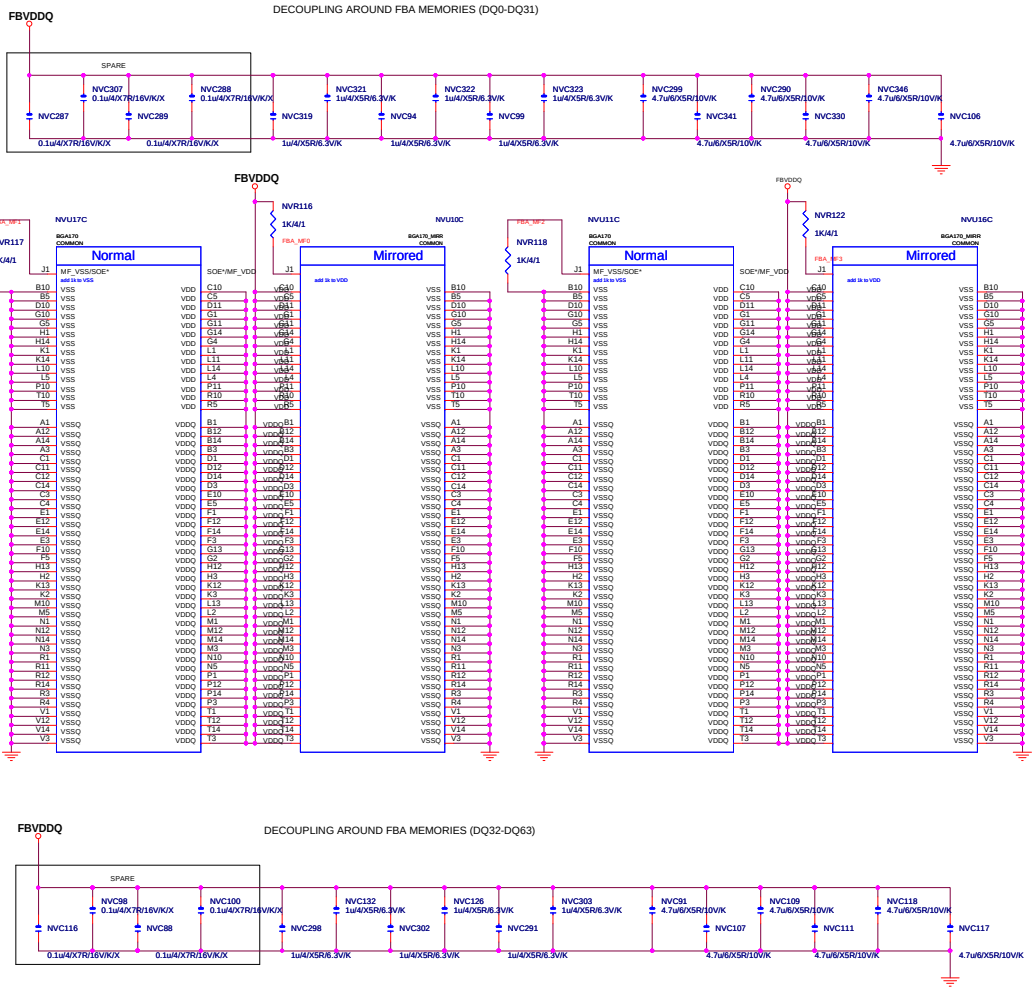
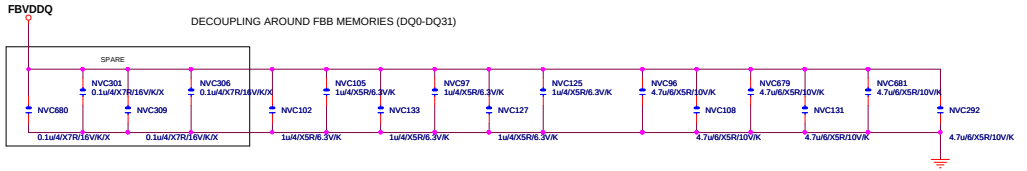
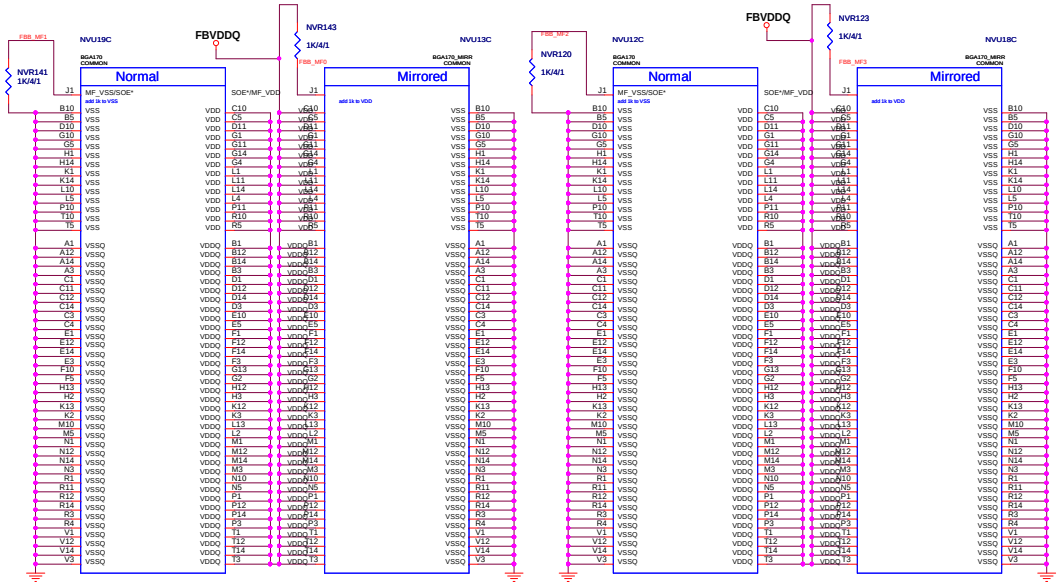
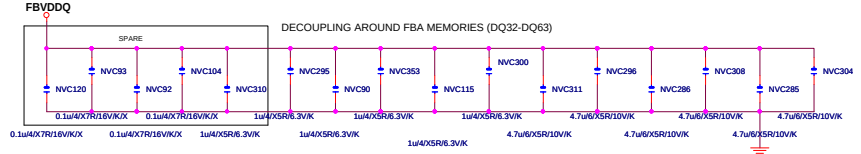
PAGE6: FRAME BUFFER PARTITION A/B DECOUPLING









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Title	NV-FB A+B PWR Decoupling	
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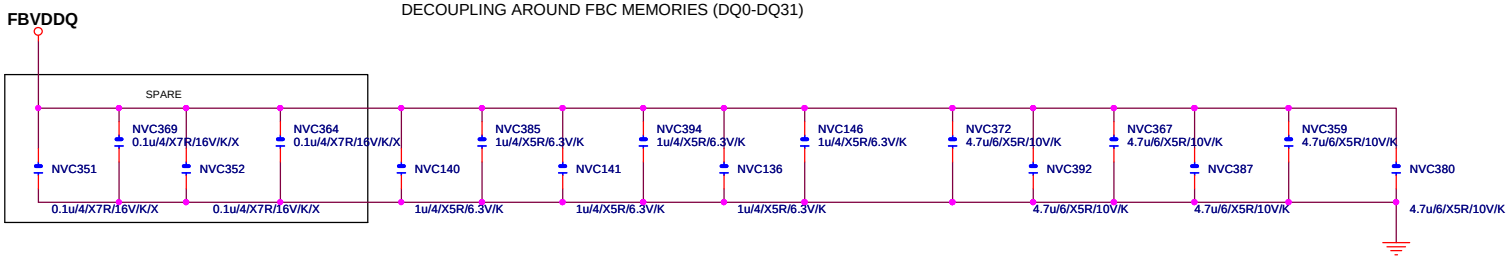
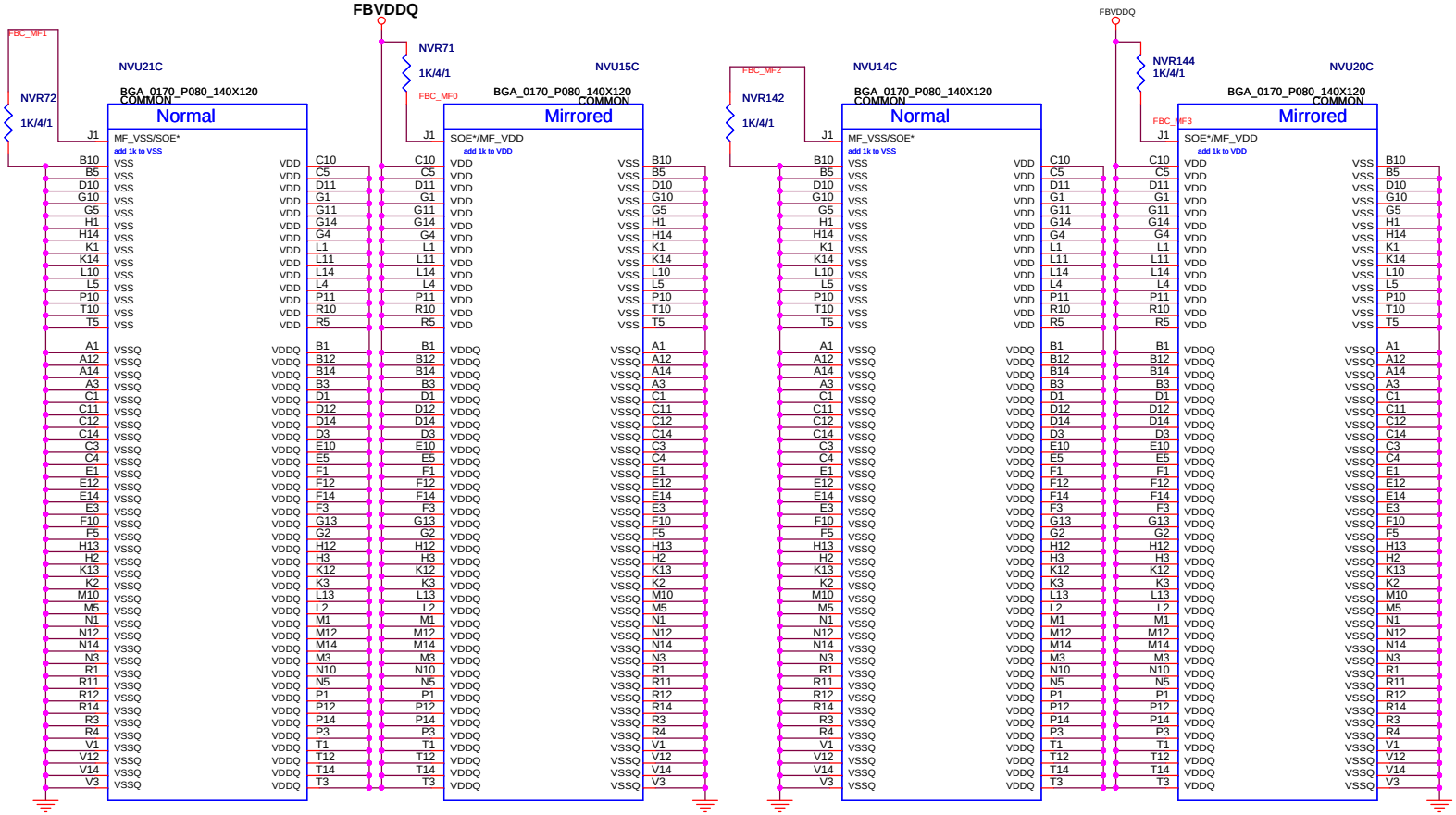
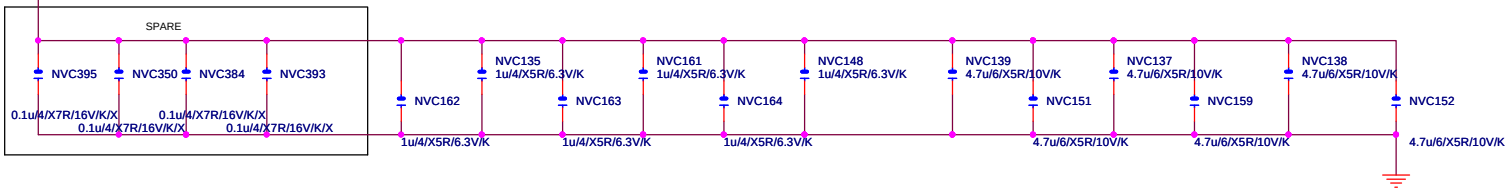
PAGE6: FRAME BUFFER PARTITION C DECOUPLING

DECOUPLING AROUND FBC MEMORIES (DQ0-DQ31)





DECOUPLING AROUND FBA MEMORIES (DQ32-DQ63)



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Title: NV-FB C PWR Decoupling		
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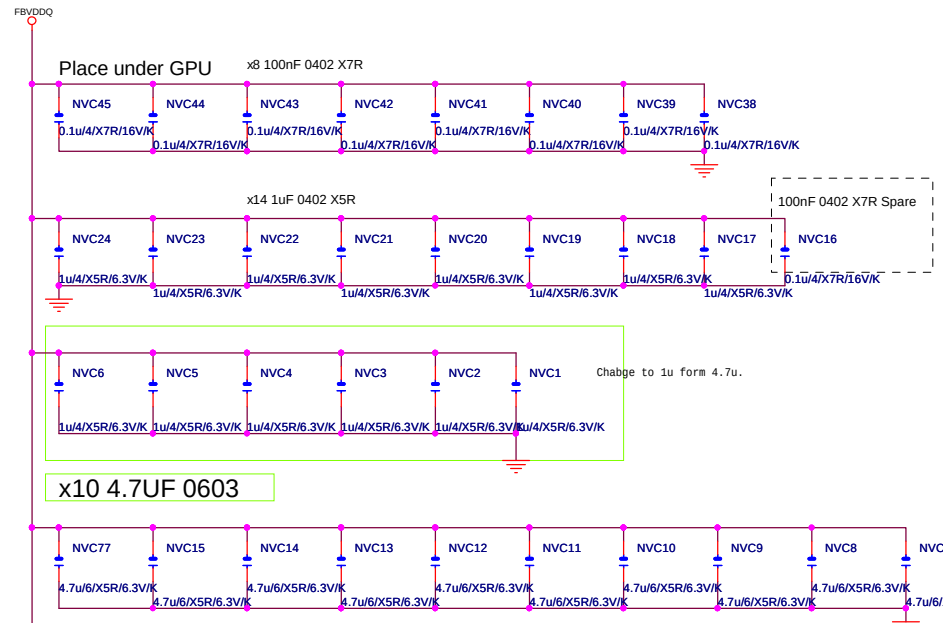
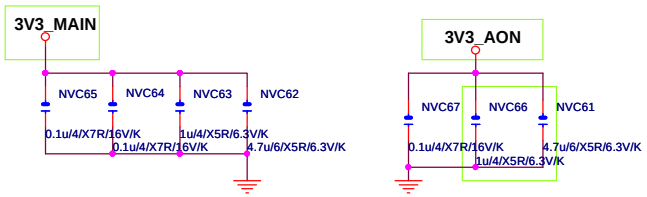
PAGE11: GPU DECOUPLING
FBVDDQ

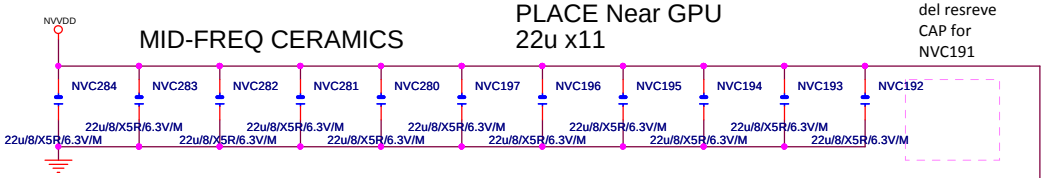


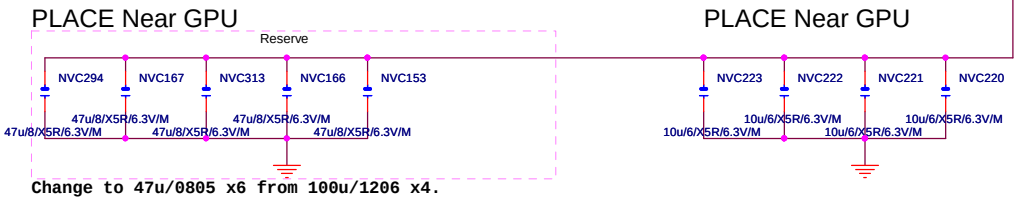


3.3V Power Rail Decoupling

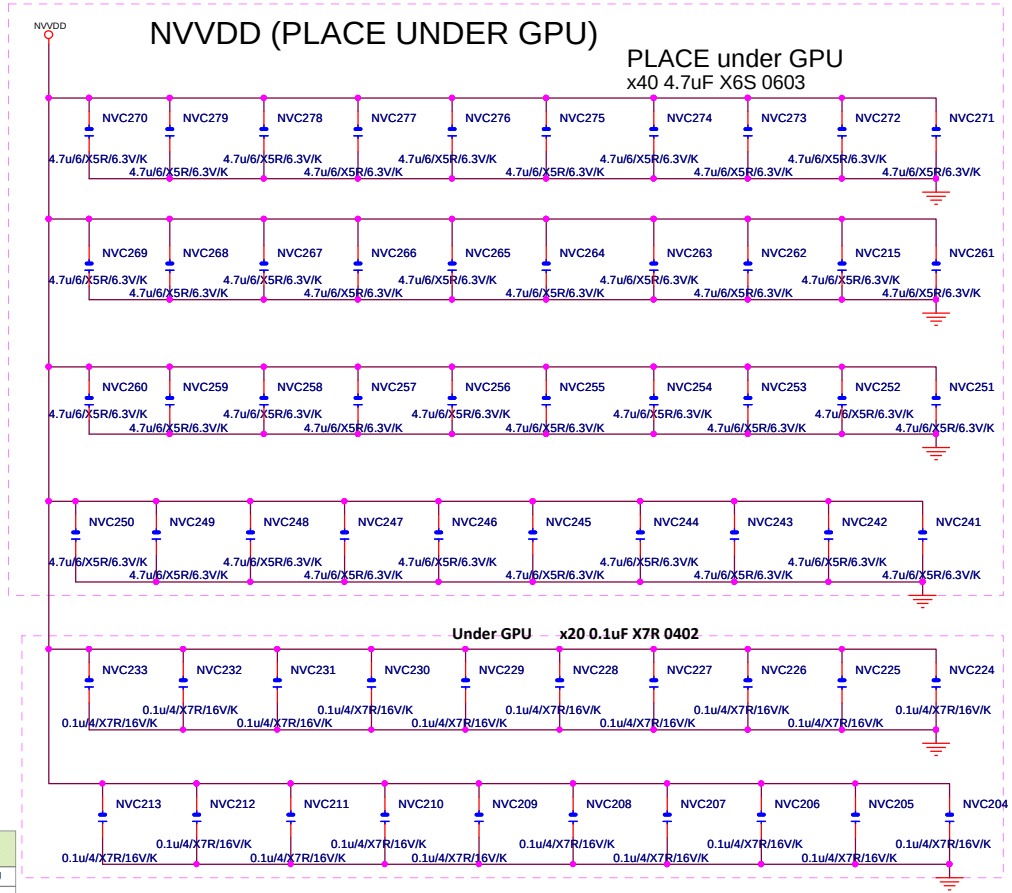
GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.





Change to 47u/0805 x6 from 100u/1206 x4.



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Title: NV-GPU PWR Decoupling		
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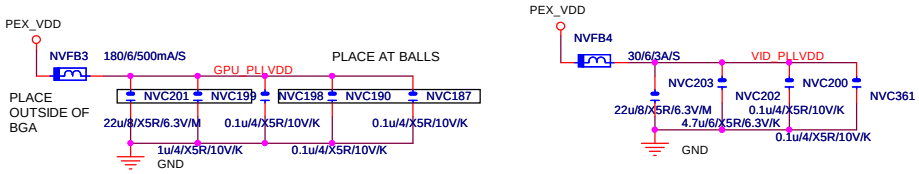
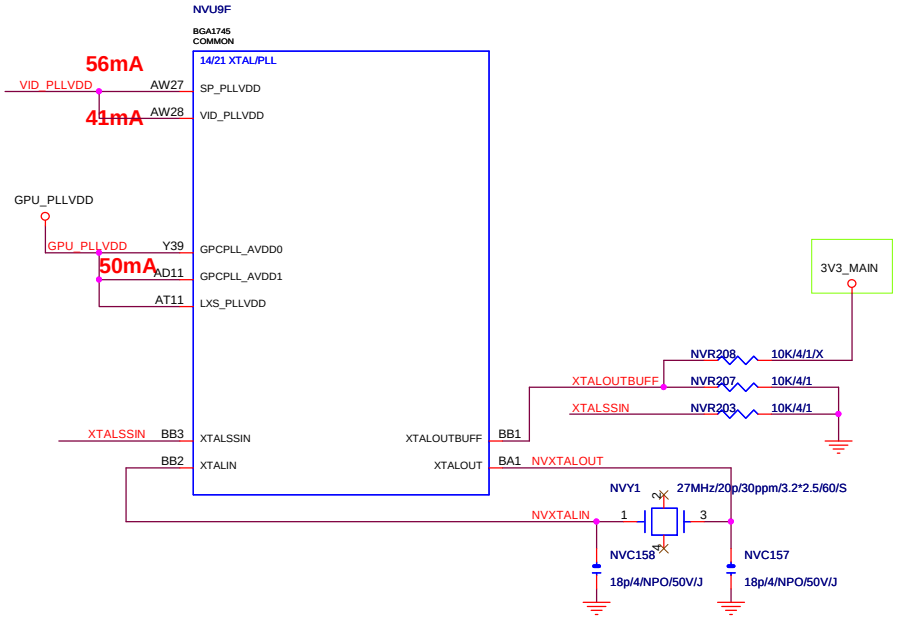
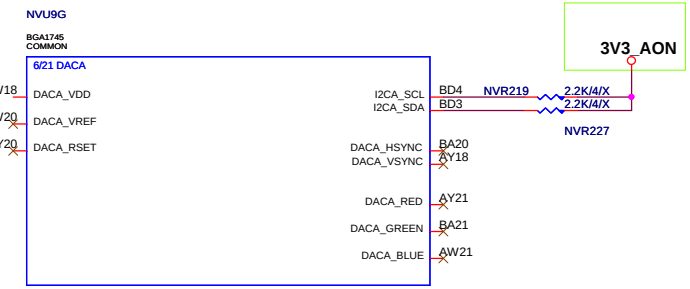
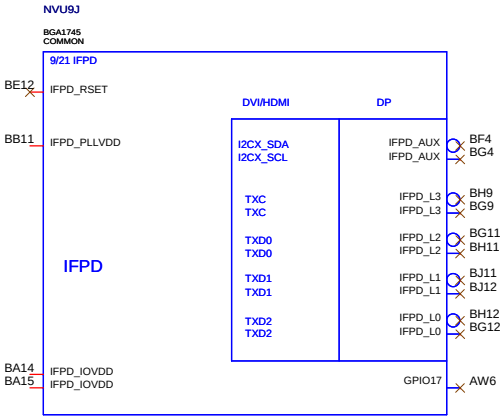
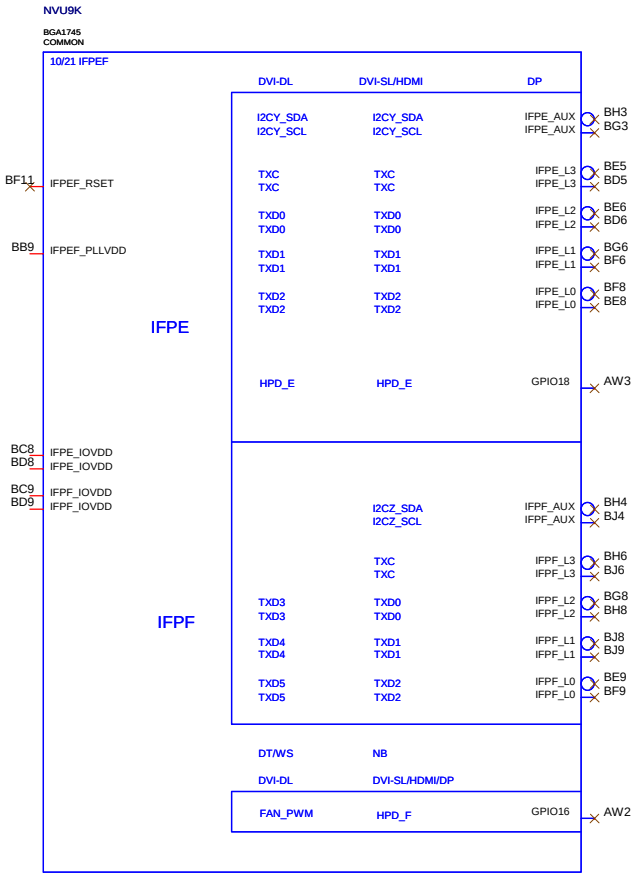
DACA/IFPX:NC

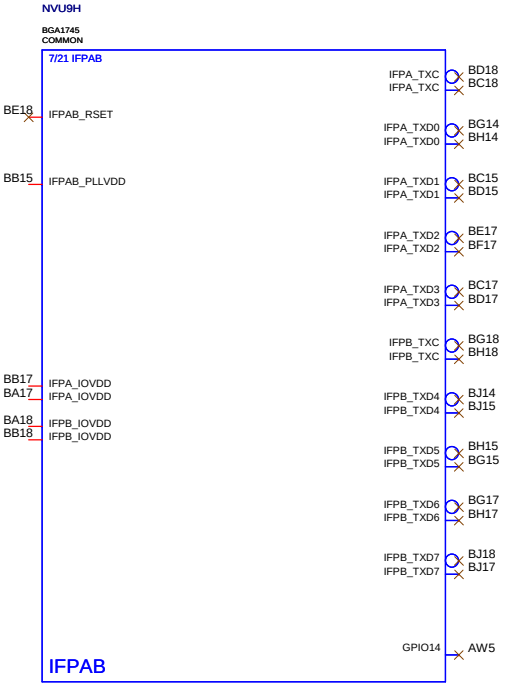


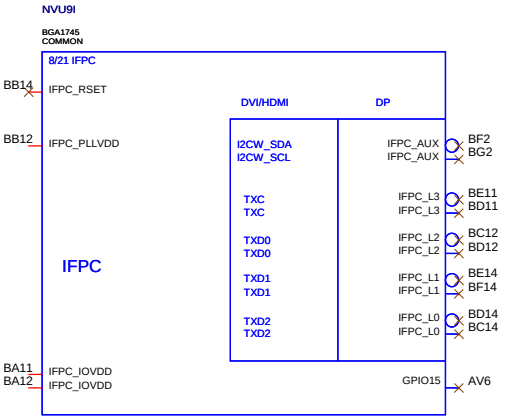












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Title	NV-DACA/XTAL/PLL/IFPX GROUP	
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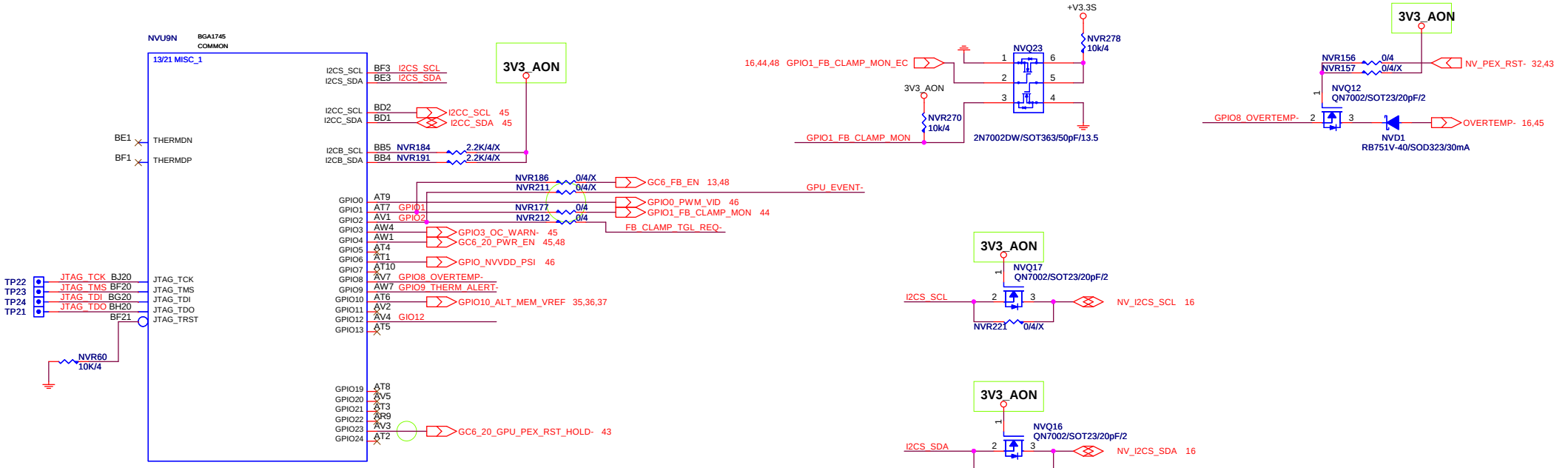
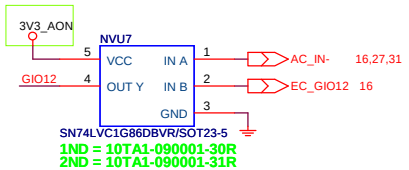
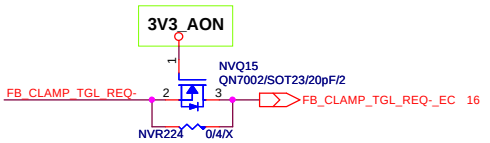


GPIO(1,2,4,23),CEC Assignment

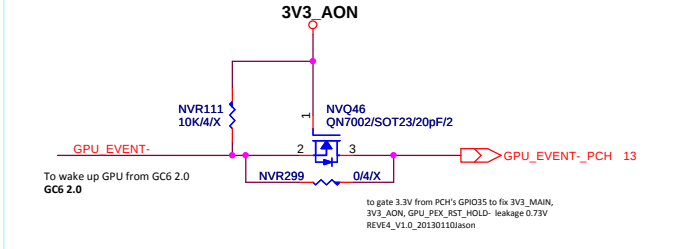
	GC6 1.0 Control Signal	GC6 2.0 Control Signal
GPIO 1	FB_CLAMP_MOM	GC6_FB_EN
GPIO 2	FBCLAMP_TGL_REQ#	GPU_EVENT#
GPIO 4	Reserve	PWR_EN
GPIO 23	Reserve	GPU_PEX_RST_HOLD#
CEC	NC	SYS_PEX_RST_MON#

	NVR(186,211,2,86), NVU6,NVD5,	NVR(177,212)
GC6 1.0	No Insert	STUFF
GC6 2.0	STUFF	No Insert





V03



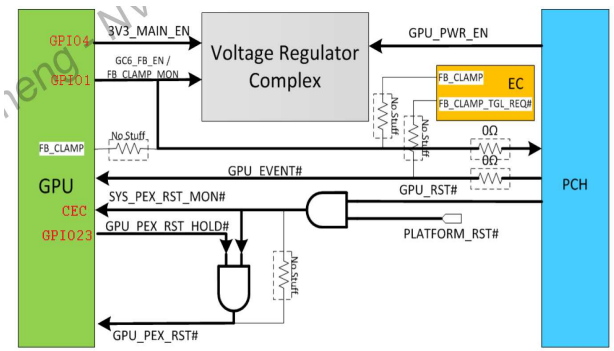
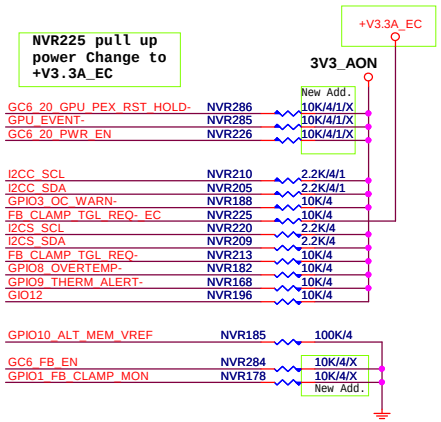


Figure 18-12. GC6 2.0 Implementation with GC6 1.0 Compatibility



Title	NV-GPIO/SPI/FAN/JTAG	
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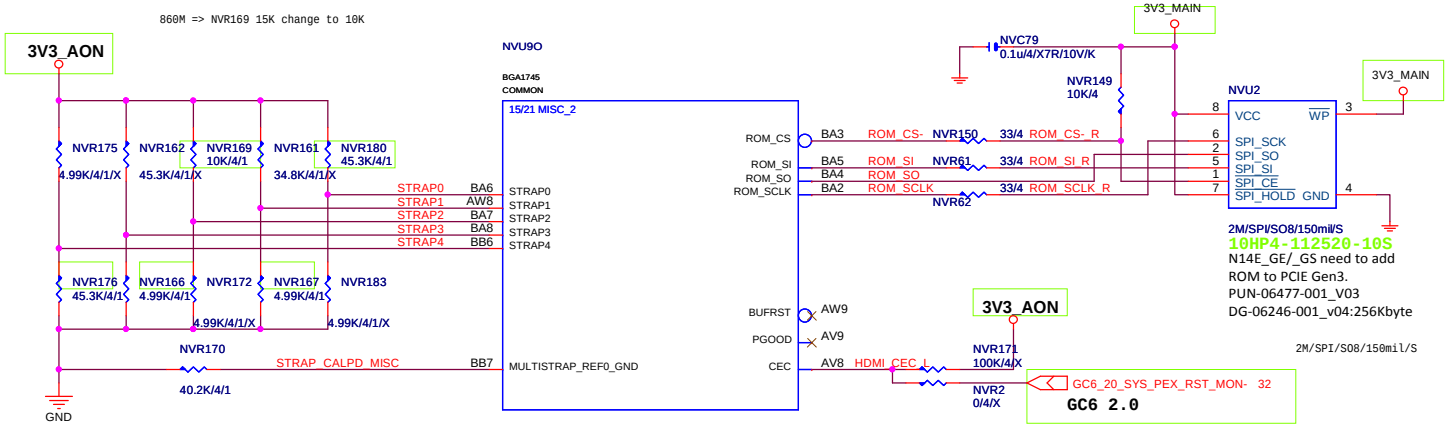

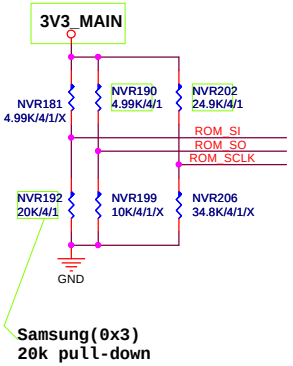

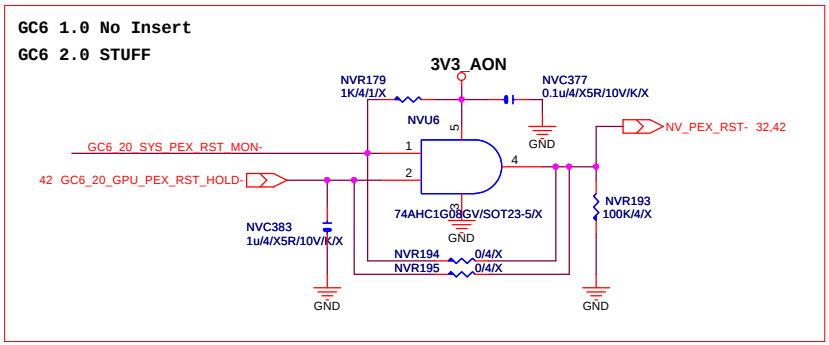

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Title: TPM 1.2		
Size: A3	Document Number: GA-R1456U_GC-1456PB	Rev: 1.0
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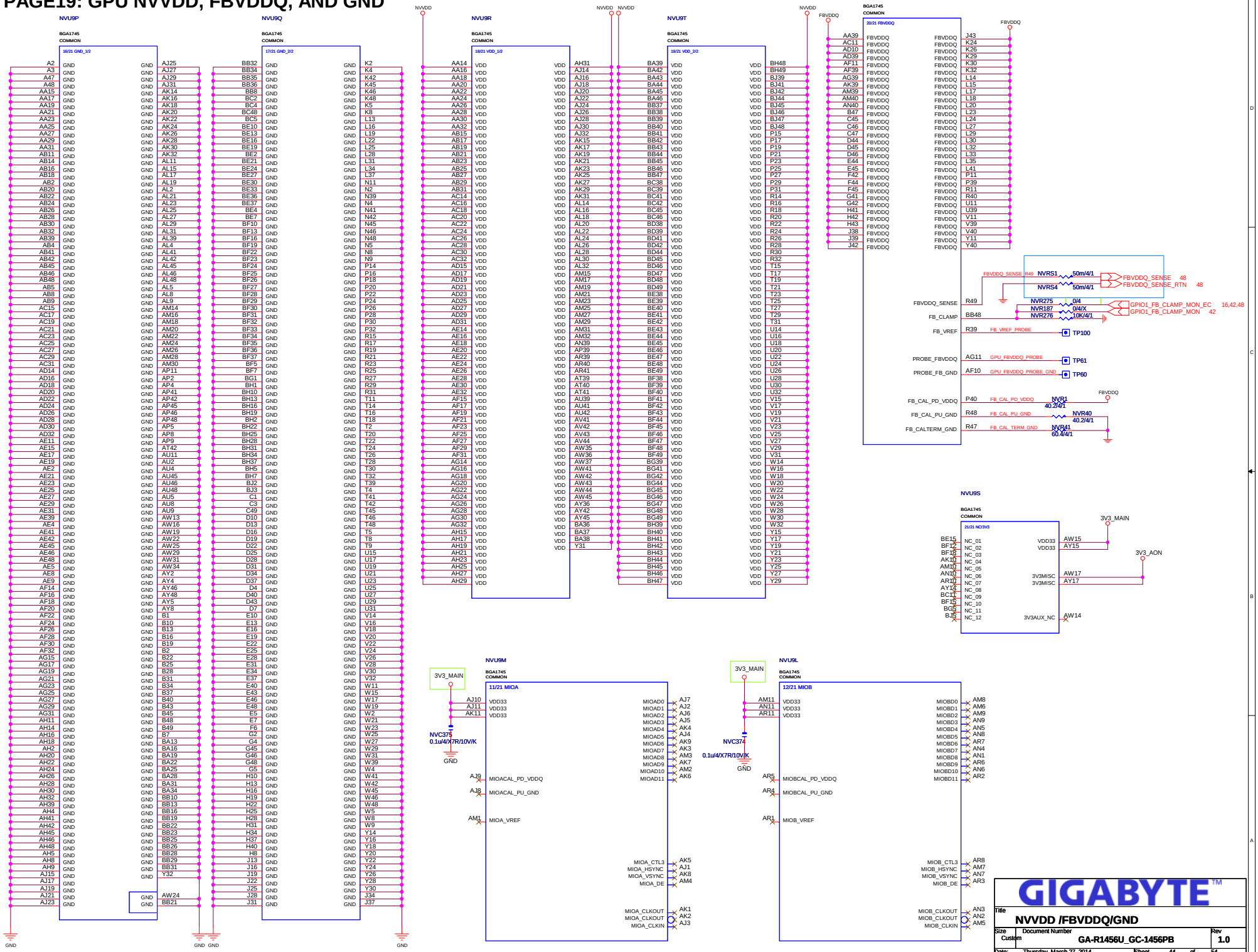
PAGE19: GPU NVVDD, FBVDDQ, AND GND



Title	NVVDD /FBVDDQ/GND
Size	Custom
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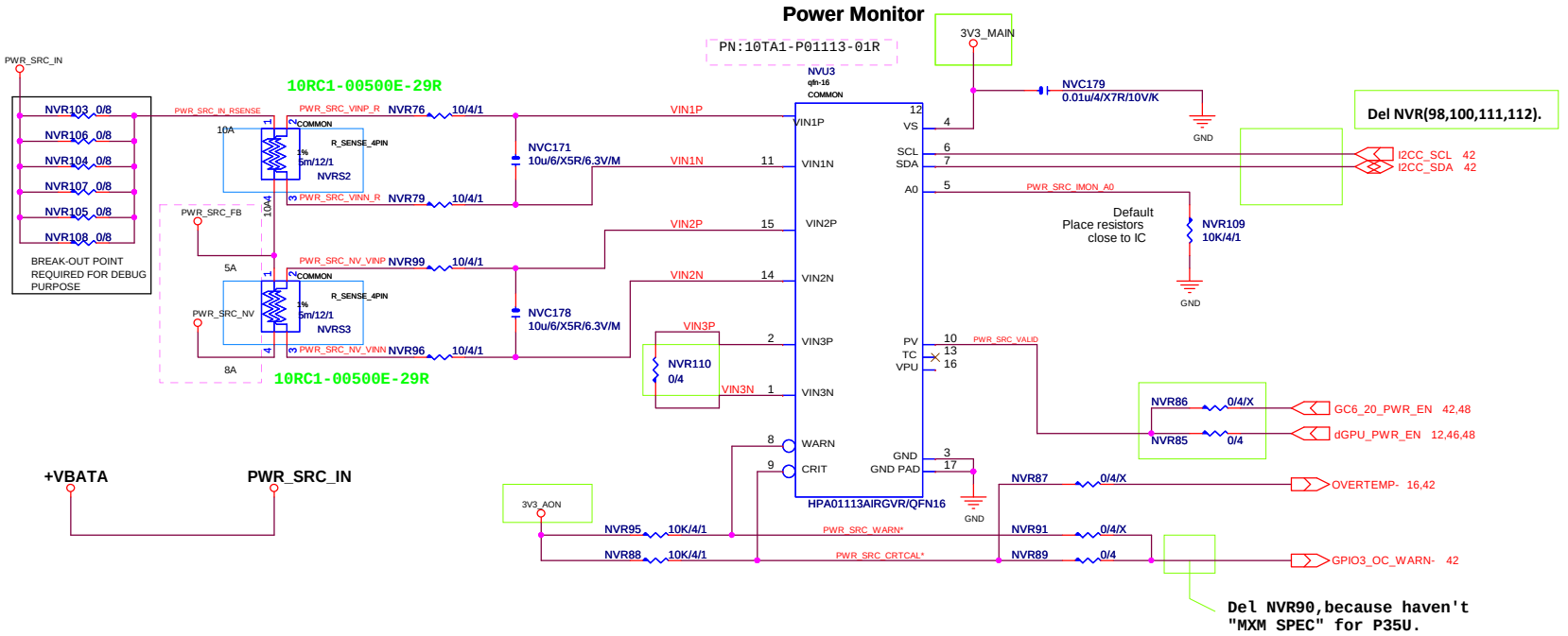
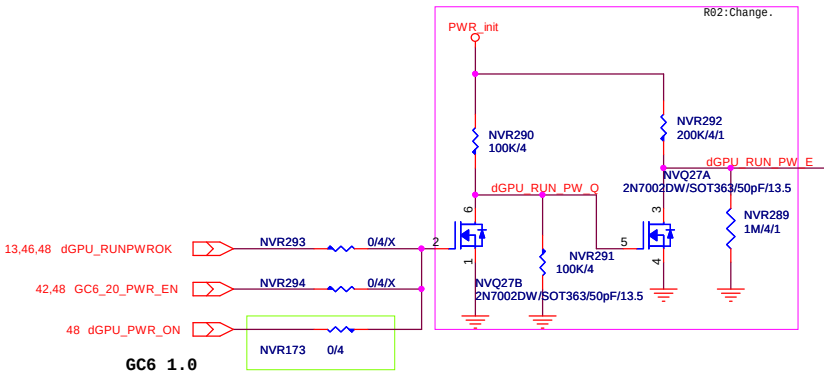
INPUT POWER CAPPING



	NVR(86)	NVR(85)
GC6 1.0	No Insert	STUFF
GC6 2.0	STUFF	No Insert

PEX_VDD_PG



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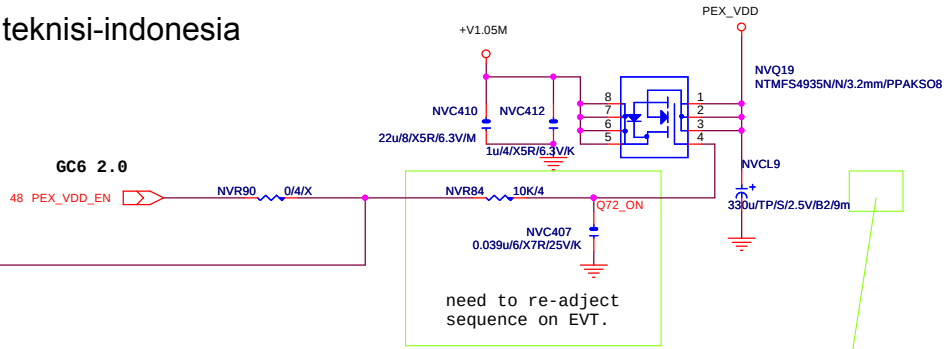

PEX_VDD_PG BOM Assignment

	NVR173	NVR90
GC6 1.0	STUFF	No Insert
GC6 2.0	No Insert	STUFF

Del NVC401,NVC396,NVC390

N15E-GT
1.05V EDP Continuous=1.01A.
Peak=2.76A.

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Title	NV IPC/PEX_VDD POWER	
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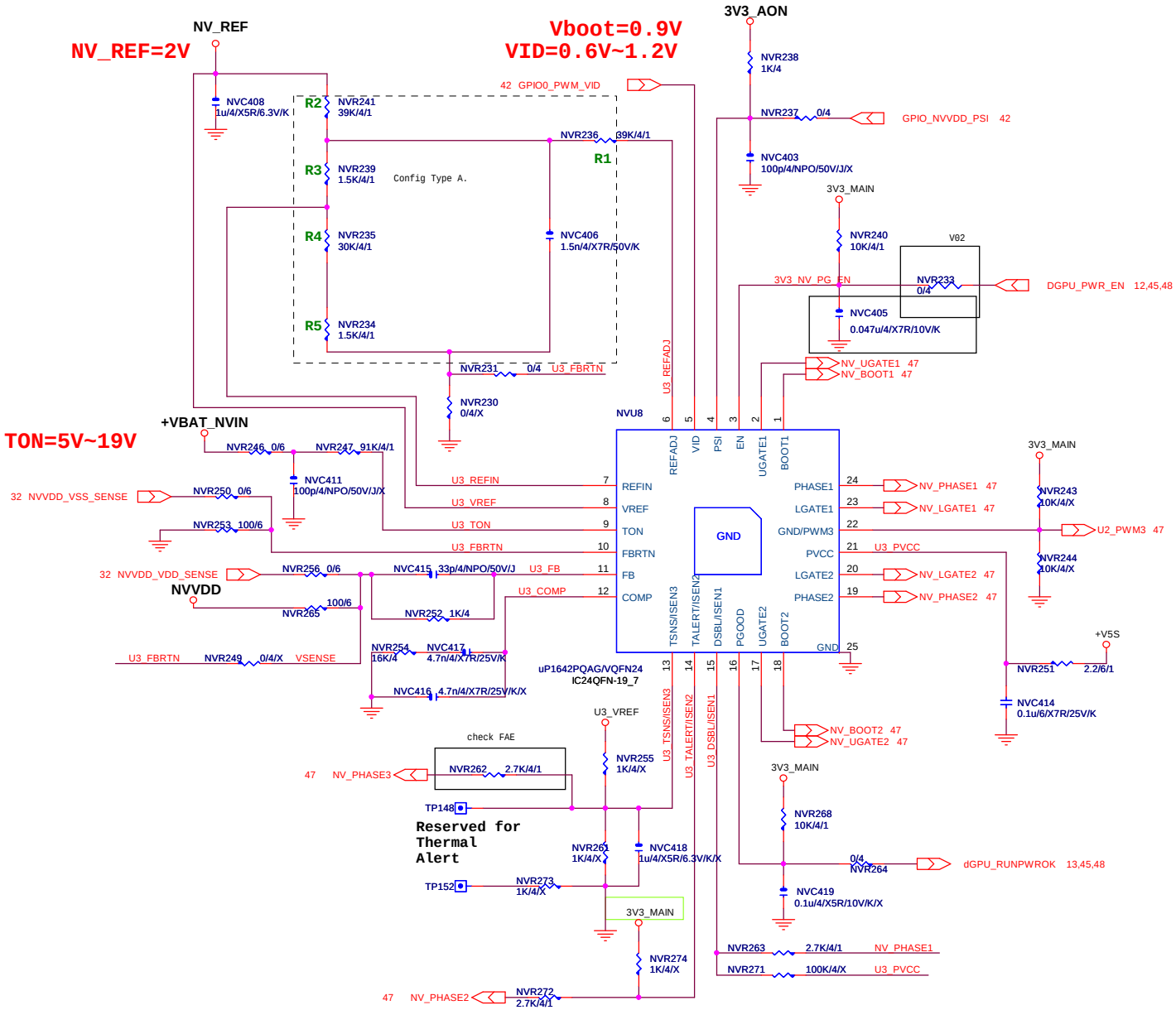

Table 1. OpenVReg Configurations

Products	OpenVR Config
N15E-GX /-GT	A

Table 1. PWM-VID Spec and Component Values

PWM-VID Specification		Config A	Config B	Config C	Config D
Vmin	V	0.6	0.6	0.65	0.9
Vmax	V	1.2	1.2	1.15	1.15
Vboot	V	0.875	0.9	0.9	1.028
Voltage Step Vstep	mV	6.25	6.25	25	12.5
Number of Voltage Levels N	level	96	96	20	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74	74
VID Transient Time T	us	<100	<100	<100	<100
Component Value					
R1 (1%)	KΩ	39	20	39	27
R2 (1%)	KΩ	39	20	30	7.5
R3 (1%)	KΩ	1.5	2	3	0
R4 (1%)	KΩ	30	18	24	6.2
R5 (1%)	KΩ	1.5	0	3	1.74
C	nF	1.5	2.7	1.8	5.6

GIGABYTE™

Title	NV CORE POWER-1	
Size A3	Document Number GA-R1456U_GC-1456PB	Rev 1.0
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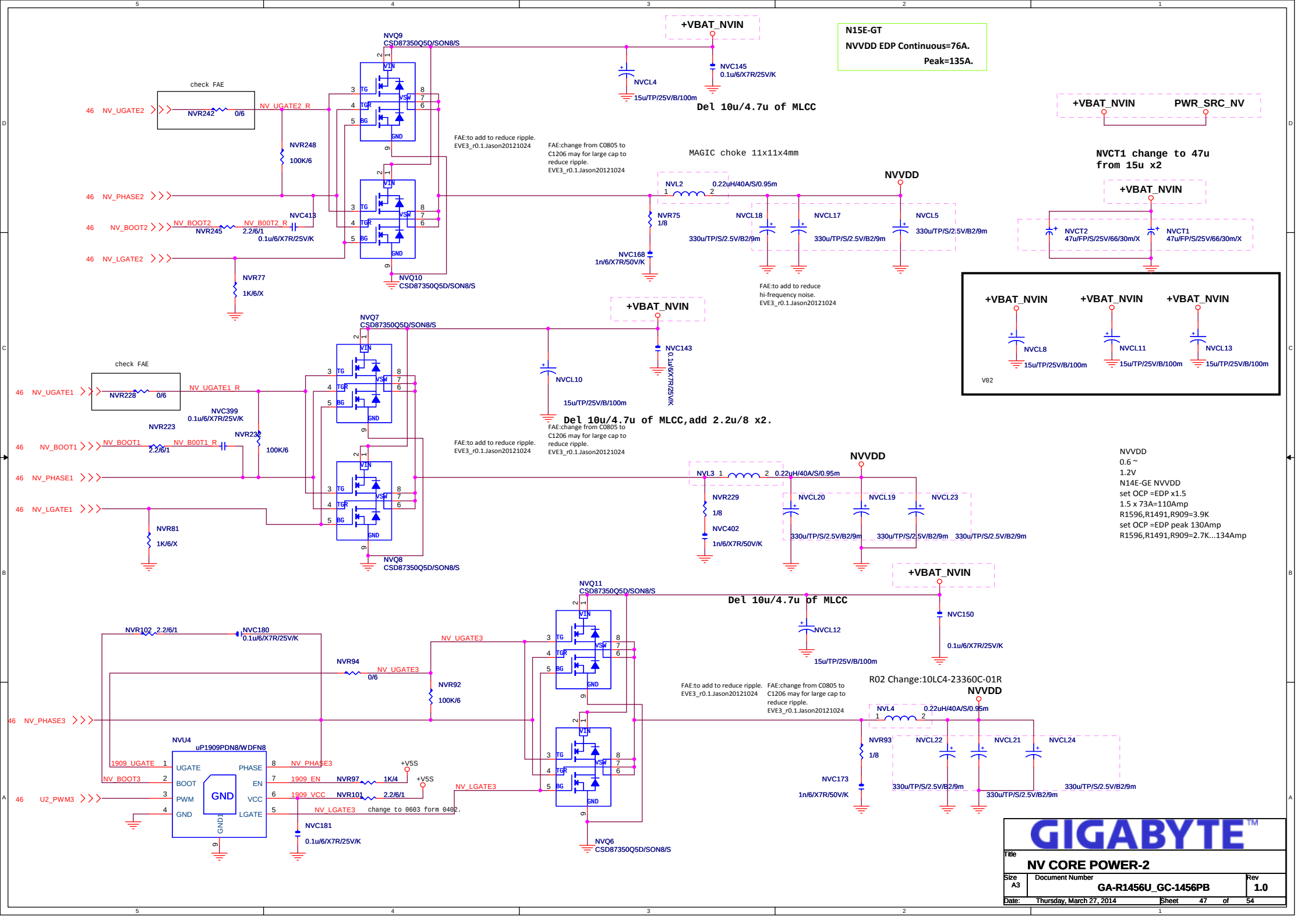
N15E-GT
NVVDD EDP Continuous=76A.
Peak=135A.
+VBAT_NVIN
NVQ9
CSD87350Q5D/SON8/S
NVCL4
15u/TP/25V/B/100m
NVC145
0.1u/6/X7R/25V/K
Del 10u/4.7u of MLCC
check FAE
46 NV_UGATE2
NVR242 0/6
NV_UGATE2_R
NVR248
100K/6
46 NV_PHASE2
46 NV_BOOT2
NV_BOOT2
NVR245
NV_B00T2_R
2.2/6/1
NVC413
0.1u/6/X7R/25V/K
46 NV_LGATE2
NVR77
1K/6/X
NVQ10
CSD87350Q5D/SON8/S
FAE:to add to reduce ripple.
EVE3_r0.1.Jason20121024
FAE:change from C0805 to
C1206 may for large cap to
reduce ripple.
EVE3_r0.1.Jason20121024
MAGIC choke 11x11x4mm
NVL2
0.22uH/40A/S/0.95m
NVVDD
NVR75
1/8
NVC168
1n/6/X7R/50V/K
NVCL18
NVCL17
NVCL5
330u/TP/S/2.5V/B2/9m
FAE:to add to reduce
hi-frequency noise.
EVE3_r0.1.Jason20121024
+VBAT_NVIN
PWR_SRC_NV
NVCT1 change to 47u
from 15u x2
NVCT2
47u/FP/S/25V/66/30m/X
NVCT1
47u/FP/S/25V/66/30m/X
+VBAT_NVIN
+VBAT_NVIN
+VBAT_NVIN
NVCL8
NVCL11
NVCL13
15u/TP/25V/B/100m
V02
NVQ7
CSD87350Q5D/SON8/S
NVC143
0.1u/6/X7R/25V/K
NVCL10
15u/TP/25V/B/100m
Del 10u/4.7u of MLCC,add 2.2u/8 x2.
check FAE
46 NV_UGATE1
NVR228 0/6
NV_UGATE1_R
NVC399
0.1u/6/X7R/25V/K
NVR223
46 NV_BOOT1
NV_BOOT1
2.2/6/1
NV_B00T1_R
NVR232
100K/6
46 NV_PHASE1
46 NV_LGATE1
NVR81
1K/6/X
NVQ8
CSD87350Q5D/SON8/S
NVL3
0.22uH/40A/S/0.95m
NVVDD
NVR229
1/8
NVC402
1n/6/X7R/50V/K
NVCL20
NVCL19
NVCL23
330u/TP/S/2.5V/B2/9m
NVVDD
0.6 ~
1.2V
N14E-GE NVVDD
set OCP =EDP x1.5
1.5 x 73A=110Amp
R1596,R1491,R909=3.9K
set OCP =EDP peak 130Amp
R1596,R1491,R909=2.7K...134Amp
NVQ11
CSD87350Q5D/SON8/S
Del 10u/4.7u of MLCC
NVC150
0.1u/6/X7R/25V/K
NVCL12
15u/TP/25V/B/100m
NVR102 2.2/6/1
NVC180
0.1u/6/X7R/25V/K
NV_UGATE3
NVR94
0/6
NVR92
100K/6
46 NV_PHASE3
NVU4
uP1909PDN8/WDFN8
1909_UGATE
NV_BOOT3
46 U2_PWM3
UGATE
BOOT
PWM
GND
PHASE
EN
VCC
LGATE
NV_PHASE3
1909_EN
1909_VCC
NVR97 1K/4
NVR101 2.2/6/1
+V5S
NV_LGATE3
change to 0603 form 0402.
NVC181
0.1u/6/X7R/25V/K
NVQ6
CSD87350Q5D/SON8/S
FAE:to add to reduce ripple.
EVE3_r0.1.Jason20121024
FAE:change from C0805 to
C1206 may for large cap to
reduce ripple.
EVE3_r0.1.Jason20121024
R02 Change:10LC4-23360C-01R
NVVDD
NVL4
0.22uH/40A/S/0.95m
NVR93
1/8
NVC173
1n/6/X7R/50V/K
NVCL22
NVCL21
NVCL24
330u/TP/S/2.5V/B2/9m
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Title
NV CORE POWER-2
Size A3
Document Number
GA-R1456U_GC-1456PB
Rev 1.0
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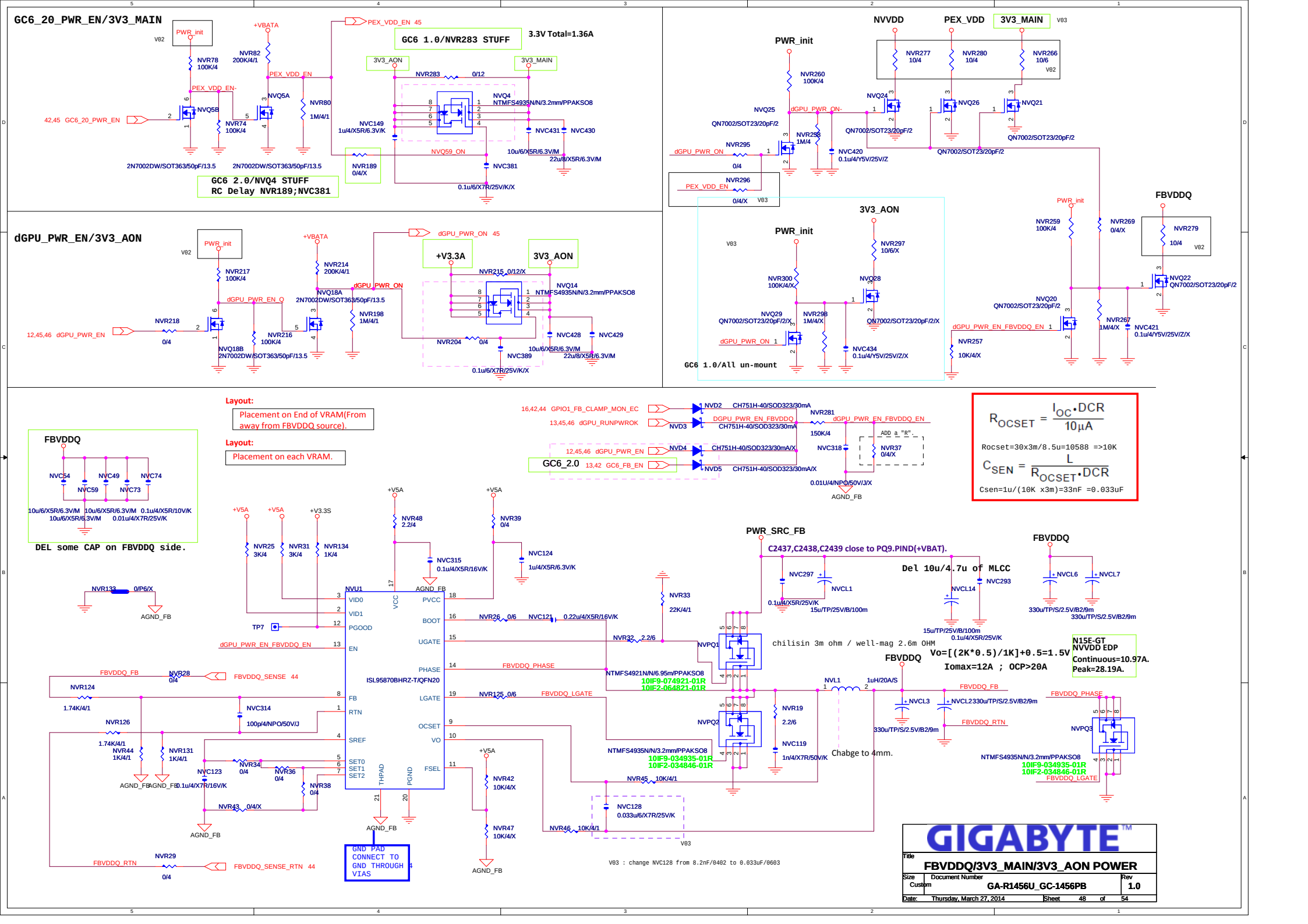
GC6_20_PWR_EN/3V3_MAIN
GC6 1.0/NVR283 STUFF
3.3V Total=1.36A
GC6 2.0/NVQ4 STUFF
RC Delay NVR189;NVC381
dGPU_PWR_EN/3V3_AON
GC6 1.0/All un-mount
Layout:
Placement on End of VRAM(From away from FBVDDQ source).
Layout:
Placement on each VRAM.
DEL some CAP on FBVDDQ side.
C2437,C2438,C2439 close to PQ9.PIND(+VBAT).
Del 10u/4.7u of MLCC
chilisin 3m ohm / well-mag 2.6m OHM
Vo=[(2K*0.5)/1K]+0.5=1.5V
Iomax=12A ; OCP>20A
N15E-GT
NVVDD EDP
Continuous=10.97A.
Peak=28.19A.
Chabge to 4mm.
GND PAD CONNECT TO GND THROUGH 4 VIAS
V03 : change NVC128 from 8.2nF/0402 to 0.033uF/0603
GIGABYTE
FBVDDQ/3V3_MAIN/3V3_AON POWER
GA-R1456U_GC-1456PB
1.0
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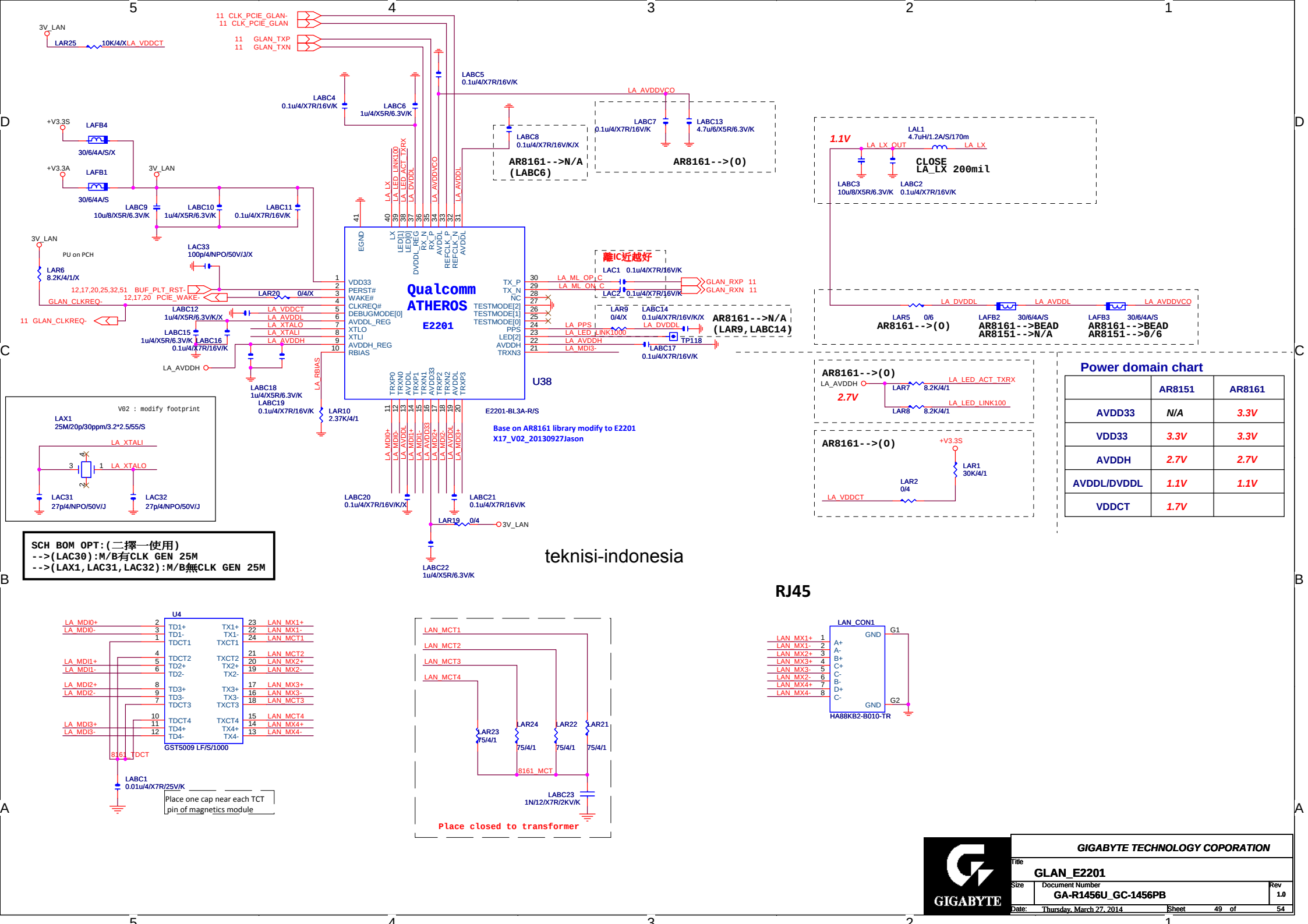
Qualcomm ATHEROS E2201
U38
E2201-BL3A-R/S
Base on AR8161 library modify to E2201
X17_V02_20130927Jason
teknisi-indonesia
SCH BOM OPT:(二擇一使用)
-->(LAC30):M/B有CLK GEN 25M
-->(LAX1,LAC31,LAC32):M/B無CLK GEN 25M
Power domain chart
AR8151
AR8161
AVDD33 N/A 3.3V
VDD33 3.3V 3.3V
AVDDH 2.7V 2.7V
AVDDL/DVDDL 1.1V 1.1V
VDDCT 1.7V
RJ45
GST5009 LF/S/1000
HA88KB2-B010-TR
Place one cap near each TCT pin of magnetics module
Place closed to transformer
GIGABYTE TECHNOLOGY COPORATION
GLAN_E2201
GA-R1456U_GC-1456PB
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DP Source Connector

Config1 用途:
for Dual-Mode [HDMI(DP-to-HMDI dongle) / DP]
若沒支援 Dual mode, 可不接.

MDP1 — mDP — MAR2C-20K1200

OUT0p	DPC1	0.1u/4/X5R/10V/K	ML_L0P	ML0(p)	3
OUT0n	DPC2	0.1u/4/X5R/10V/K	ML_L0N	ML0(n)	5
OUT1p	DPC3	0.1u/4/X5R/10V/K	ML_L1P	ML1(p)	9
OUT1n	DPC4	0.1u/4/X5R/10V/K	ML_L1N	ML1(n)	11
OUT2p	DPC5	0.1u/4/X5R/10V/K	ML_L2P	ML2(p)	15
OUT2n	DPC6	0.1u/4/X5R/10V/K	ML_L2N	ML2(n)	17
OUT3p	DPC7	0.1u/4/X5R/10V/K	ML_L3P	ML3(p)	10
OUT3n	DPC8	0.1u/4/X5R/10V/K	ML_L3N	ML3(n)	12
AUX_SNKp_83				AUX(p)	16
AUX_SNKn_83				AUX(n)	18
CAD_SNK_83				CONFIG1	4
				CONFIG2	6
HPD_SNK_83				HPD	2
				RETN	19

mDP: PWR 20; P1 1; P7 7; GND 8, 13, 14; G1, G2, G3, G4

+V3.3S_MDP — R1190 0/8 — C242 22u/8/X5R/6.3V/M — C243 22u/8/X5R/6.3V/M

+V3.3S_DP — DPR32 100K/4 — DPR33 100K/4 (V02)

R83 5.1M/4

DDPC / HPD

12 DDPC_AUXP	DPC9	0.1u/4/X5R/10V/K	AUX_SRCp	
12 DDPC_AUXN	DPC10	0.1u/4/X5R/10V/K	AUX_SRCn	
12 DDPC_CTRLCLK	DPR9	0/4	SCL_DDC	
12 DDPC_CTRLDATA	DPR10	0/4	SDA_DDC	
12 DDPC_HPD	HPD_SRC_83	DPR24	100K/4	V02

+V3.3S_DP +V3.3S_DP — DPR34 2.2K/4 — DPR35 2.2K/4

+V3.3S_DP — DPR14 10K/4/1 — RST-_83 — DPC13 2.2u/8/X7R/10V/K (2.2uF X7R only find 0805 Size in HWtool)

TP199 — CAD_SRC_83

FAE:
Cable Adaptor DETection , 若
NV 也沒使用, 則可不接.
X17_V02_20130930Jason

+V3.3S_DP — DPC15 0.1u/4/X5R/10V/K — DPC14 0.01u/4/X7R/10V/K

+V3.3S_DP — DPR31 0/8 — +V3.3S

DPU1

Parade
PS8330B
3.3V power
Dual_Mode DP V1.2 5.4Gbps

PS8330BQFN48GTR2/S
7mm x 7mm QFN48 pin

Library created by JasonWu
X17_V02_20130929

5 DDIC_TXP0	IN0p	37	NC	
5 DDIC_TXN0	IN0n	38	IN0p	
	CFG1_83	39	IN0n	
5 DDIC_TXP1	IN1p	40	CFG1	
5 DDIC_TXN1	IN1n	41	IN1p	
		42	IN1n	
5 DDIC_TXP2	IN2p	43	NC	
5 DDIC_TXN2	IN2n	44	IN2p	
		45	IN2n	
5 DDIC_TXP3	IN3p	46	NC	
5 DDIC_TXN3	IN3n	47	IN3p	
		48	IN3n	
		49	EAPD	

		24	GND	
OUT0p		23	OUT0p	
OUT0n		22	OUT0n	
		21	NC	
OUT1p		20	OUT1p	
OUT1n		19	OUT1n	
		18	GND	
OUT2p		17	OUT2p	
OUT2n		16	OUT2n	
		15	NC	
OUT3p		14	OUT3p	
OUT3n		13	OUT3n	

+V3.3S_DP — DPC17 2.2u/4/X5R/6.3V/M — DPR29 4.99K/4/1 — DPR30 1M/4

AE 建議做 Pin control mode
直接以 H/W strape PEQ & CFG0 對 EQ 做 設定.
若採 I2C control mode, 一樣是用來做 EQ 設定
I2C (SCL_CTL, SDA_CTL) 就拉 給 EC.

CFG0_83	DPR22 / DPR23	4.7K/4/X	Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150k ohm, 3.3V I/O. L: default, automatic EQ enable & AUX interception enable H: automatic EQ disable & AUX interception enable M: automatic EQ disable & AUX interception disable, no pre-emphasis, 600mVpp swing
CFG1_83	DPR26 / DPR27	4.7K/4/X	Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K H: default, auto test disable & input offset cancellation enable L: auto test enable & input offset cancellation enable M: auto test disable & input offset cancellation disable
PEQ_83	DPR20 / DPR21	4.7K/4/X	Programmable input equalization levels; Internal pull down at ~150k ohm, 3.3V I/O. L: default, LEQ, compensate channel loss up to 12dB @ HBR2 H: HEQ, compensate channel loss up to 15dB @ HBR2 M: LLEQ, compensate channel loss up to 5dB @ HBR2
I2CADDR_83	DPR28	0/4	I2C control enable and address. Internal pull down at ~150k ohm. 3.3V I/O L: pin control mode H: I2C Control is selected with default I2C address 42/43 M: I2C Control is selected with alternative I2C address C2/C3

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Title	Mini_DP/DP_Re-Driver	
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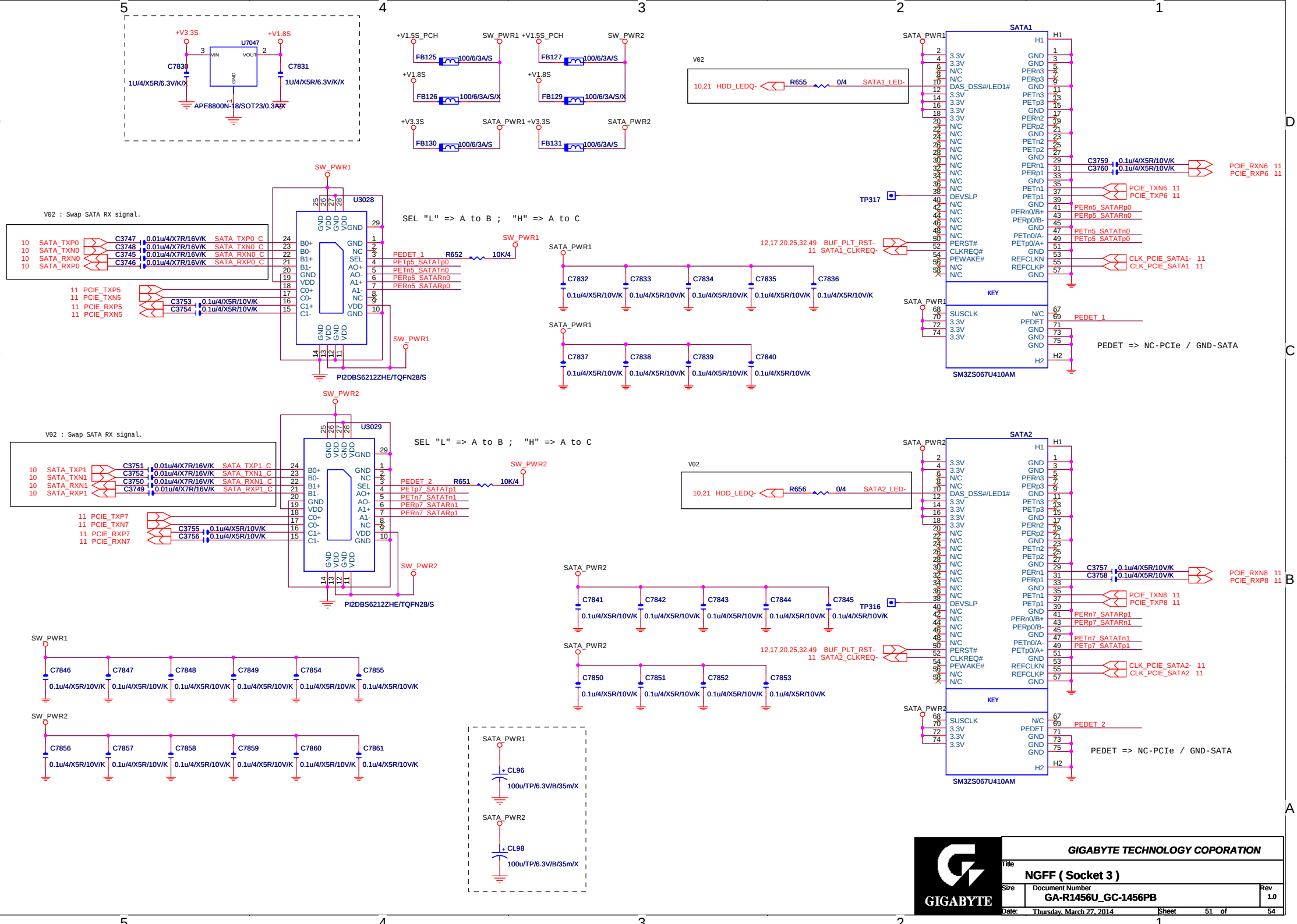

Title	NGFF (Socket 3)
Size	
Document Number	GA-R1456U_GC-1456PB
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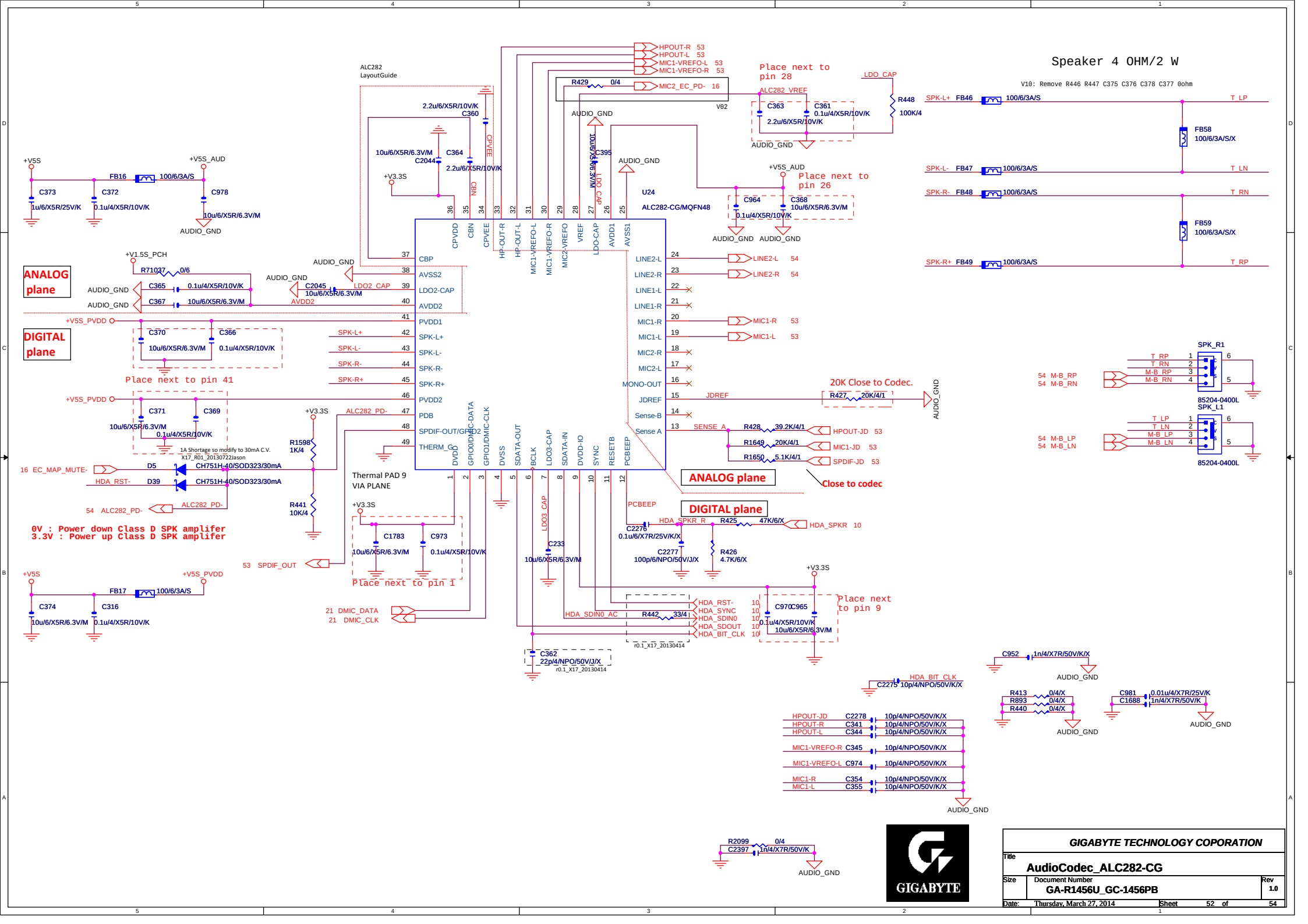
Speaker 4 OHM/2 W
V10: Remove R446 R447 C375 C376 C378 C377 0ohm
ALC282 LayoutGuide
U24
ALC282-CG/MQFN48
ANALOG plane
DIGITAL plane
Place next to pin 28
Place next to pin 26
Place next to pin 41
Place next to pin 1
Place next to pin 9
20K Close to Codec.
Close to codec
Thermal PAD 9 VIA PLANE
0V : Power down Class D SPK amplifer
3.3V : Power up Class D SPK amplifer
1A Shortage so modify to 30mA C.V. X17_R01_20130722Jason
r0.1_X17_20130414
SPK_R1
SPK_L1
85204-0400L
HPOUT-R 53
HPOUT-L 53
MIC1-VREFO-L 53
MIC1-VREFO-R 53
MIC2_EC_PD- 16
LINE2-L 54
LINE2-R 54
MIC1-R 53
MIC1-L 53
HPOUT-JD 53
MIC1-JD 53
SPDIF-JD 53
HDA_SPKR 10
HDA_RST- 10
HDA_SYNC 10
HDA_SDIN0 10
HDA_SDOUT 10
HDA_BIT_CLK 10
SPDIF_OUT 53
ALC282_PD- 54
DMIC_DATA 21
DMIC_CLK 21
EC_MAP_MUTE- 16
GIGABYTE TECHNOLOGY COPORATION
AudioCodec_ALC282-CG
GA-R1456U_GC-1456PB
Rev 1.0
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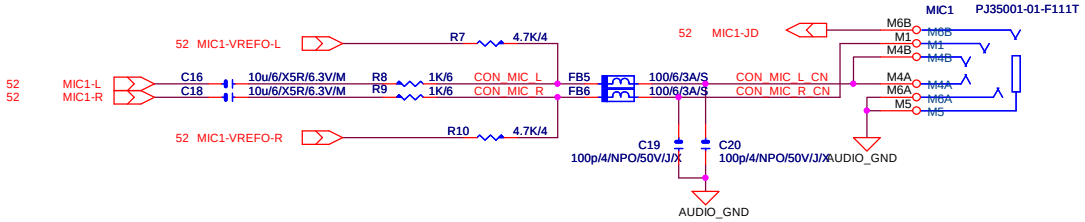
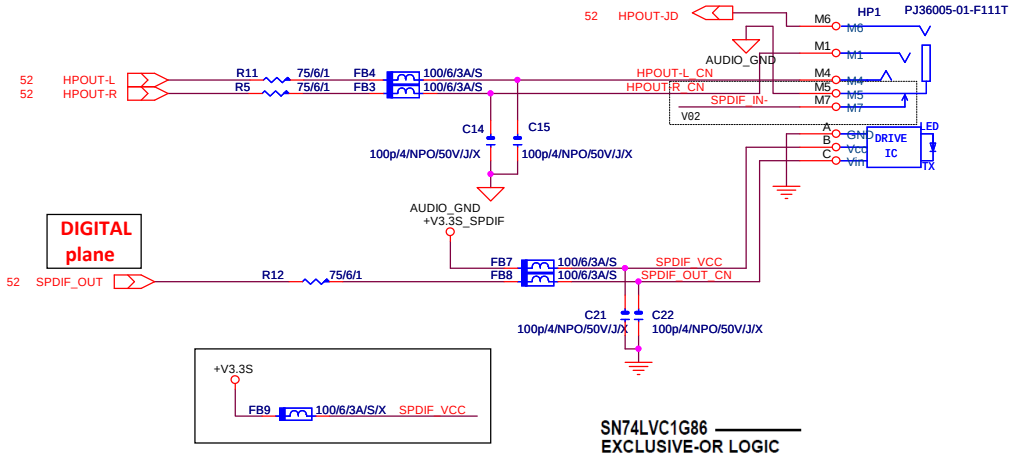
Audio Jack

Description: iPhone headphone jack adapter

4 pin 3.5mm (2.5mm) plug connector

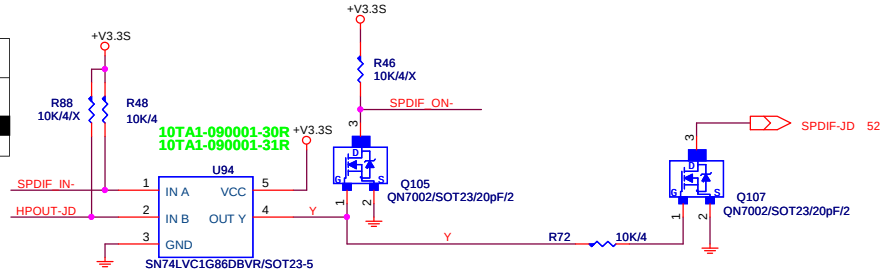
Pin Number	Pin Name	Description
1	Tip	Left audio
2	Ring	Right audio
3	Ring	Common/Ground
4	Sleeve	Microphone



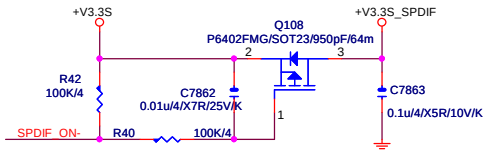


SN74LVC1G86
EXCLUSIVE-OR LOGIC
FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	L
L	H	H
H	H	L



Turn off SPDIF Power while no SPDIF plug.



GIGABYTE TECHNOLOGY COPORATION

Title: Phone Jack

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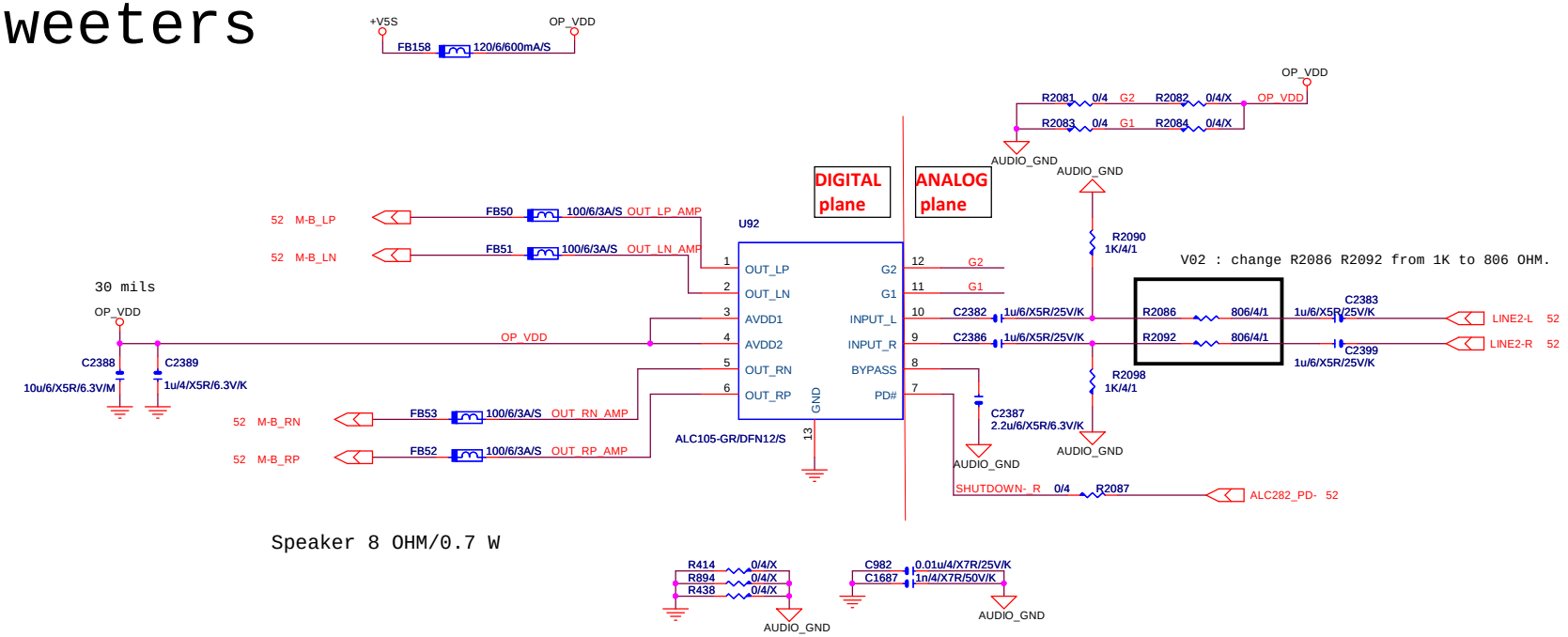
tweeters



Speaker 8 OHM/0.7 W

G1 and G2 are used to configure the input-to-output gain ratio.

Table 6. Amplifier Gain

G1	G2	Single-End Output Gain (OUT-LP/OUT-LN) (OUT-RP/OUT-RN)	Differential Output Gain (OUT-LP/OUT-LN) (OUT-RP/OUT-RN)
GND	GND	5dB	11dB
PVDD1	GND	8dB	14dB
GND	PVDD1	13dB	19dB
PVDD1	PVDD1	19dB	25dB

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Title: ALC105	
Size	Document Number: GA-R1456U_GC-1456PB — Rev: 1.0
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