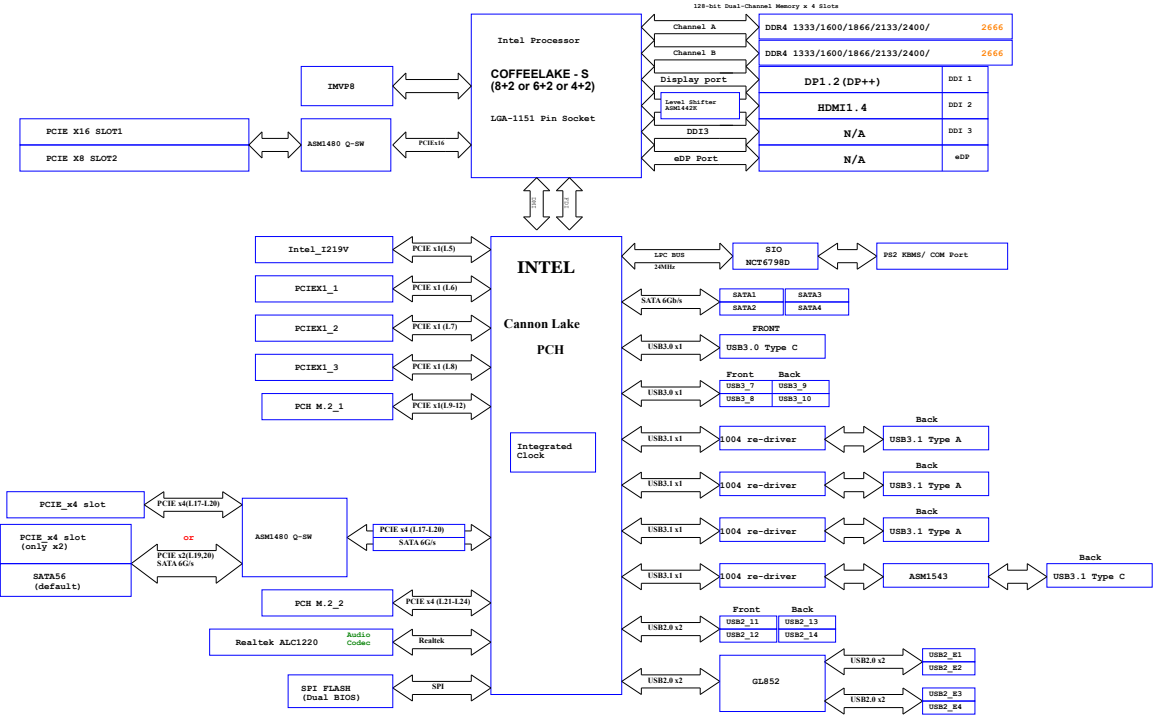
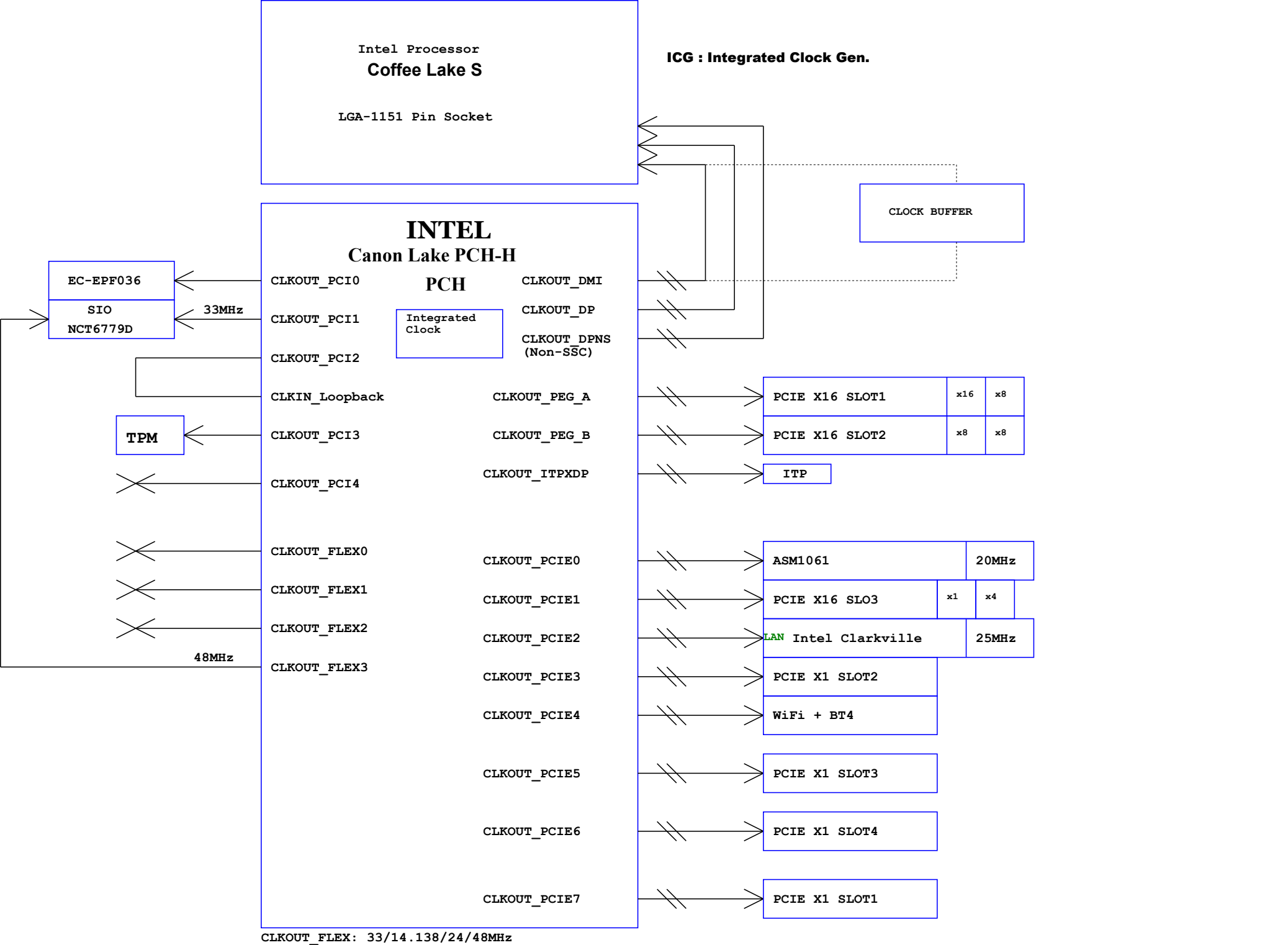
PRIME Z390-A board

Rev 1.00

2018.05





CLKOUT_FLEX: 33/14.138/24/48MHz

<Variant Name>

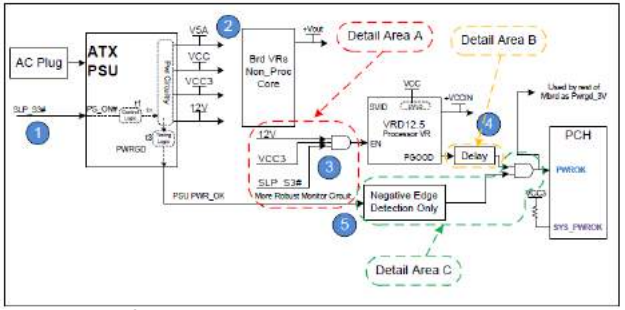
ASUSTek COMPUTER INC.

Title : Clock Distribution

Engineer: Aaron_Su

Size	Project Name	Rev
A3	Z390 Golden board	R1.00

Date: Tuesday, July 24, 2018 Sheet 2 of 139



PCH

LYNX POINT

SIO

NCT6779D

PCI_Express x 16_1 — PWRGD — <19>O_PCIRST#_PCIEX16_1

PCI_Express x 16_2 — PWRGD — <19>O_PCIRST#_PCIEX16_2

PCI_Express x 1_1,2 & x16_3 — PWRGD — <19>O_PCIRST#_PCIEX16_3

POWER_SWITCH — PWRBTN — <5>O_PWRBTN#IN

POWER SUPPLY — Main PWR — VSB — PSON# — PWROK

<2>AC Power Switch On

<10>12V,5V,3V

<3>+5VSB, +3VSB

<9>O_PSON#

<11>B_ATX_PWROK

PS_IN# — PSON# *1 — ATXPGD *2 — PWROK

PCIRST1# — PCIRST2# — PCIRST3# — LRESET# — KBRST# — RSMRST# — PS_OUT# — SUSC# — SUSB#

<18>S_PLTRST# *8

O_KB_RST#

<4>O_RSMRST#

<6>O_PWRBTN#

<4.1> / <8>S_SLPS4#

<4.2> / <9>S_SLPS3#

<7>S_SLP_A#

<7.1>S_SLP_LAN#

HDA_RST# — PLTRST# — RCIN# — RSMRST# — PWRBTN# — SLP_S5# — SLP_S4# *4 — SLP_S3# *5 — SLP_A# *3 — SLP_LAN# — SYS_PWROK — PCH_PWROK — PLTRST_PROC# — DRAMPWROK — RTCRST# — SRTCRST# — PROCPUPWRGD — DPWROK — MEPWROK

AZ_RST#

RESET# AUDIO ALC898

SYS_RESET#

<1>RTCRST#

<1>SRTCRST#

BATTERY

<3.1>S_DPWROK

Non-AMT

AMT

<12>O_PWROK

ME_POWER — +1.05ME — +3V_DUAL_LAN/EPW

<7.2>S_MEPWROK

RESET_SWITCH — SYS_RESET#

XDP — DBR# — RESET# — OBSDATA

SYS_RESET#

H_CPURST#

PROCESSOR HASWELL — DBR# — RESET# — SM_DRAMPWROK — CFG — PWRGOOD — SVID — VCORE

SYS_RESET# *9

<18>H_CPURST# *5

<13>S_DRAMPWRGD

<14>H_CPUPWRGD *7

<15>VRM_SVID

<16>VCORE

Vcore Controller — SVID — VCORE — VR_ON — PGOOD — ISL95818

<17>VRMPWRGD

*6 S_SLPS3# — +12V — +3V

CHIP

SOCKET or SLOT

*1 PSON# is inverted by SLP_S3#, but gated and delayed by PWRBTN#

*2 PWROK will assert when +3V arrives at +2.1V then delay 300ms~500ms and gated by ATXPGD

*3 If support AMT, SLP_A# could already be high before sequence begins. If not support AMT, SLP_A# will come with SLP_S3

*4 SLP_S4# controls +1.5VDual and +VTTDDR

*5 Come with 1.5VDUAL

*6 Come with +3V,+12V and gated by SLP_S3#

*7 CPUPWRGD= After PWROK

*8 PLTRST# = PCH PWROK AND PCH SYS_PWROK

*9 PLTRST_PROC#=PLTRST#, voltage=1V, directly connect to CPU

<Variant Name>

ASUSTeK COMPUTER INC.

Title : Signal & Reset map

Engineer: Aaron_Su

Size: A3 | Project Name: Z390 Golden board | Rev: R1.00

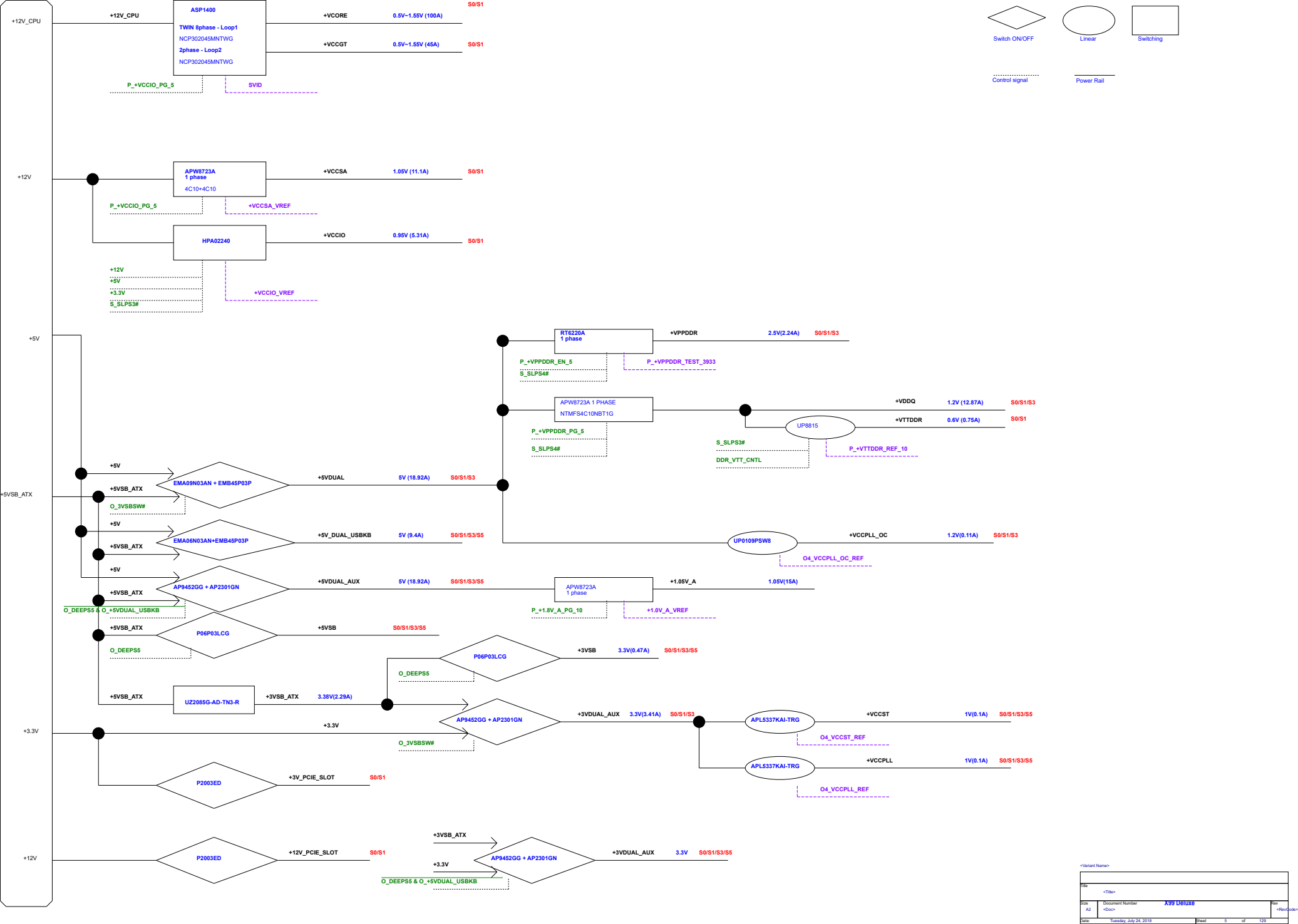
Date: Tuesday, July 24, 2018 | Sheet 3 of 139

Title :

Engineer:

Size	Project Name	Rev
A3		R1.00

Date:	Tuesday, July 24, 2018	Sheet	4	of	139


+12V_CPU
+12V_CPU
ASP1400
TWIN 8phase - Loop1
NCP302045MNTWG
2phase - Loop2
NCP302045MNTWG
+VCORE
0.5V~1.55V (100A)
S0/S1
+VCCGT
0.5V~1.55V (45A)
S0/S1
P_+VCCIO_PG_5
SVID
Switch ON/OFF
Linear
Switching
Control signal
Power Rail
+12V
APW8723A
1 phase
4C10+4C10
+VCCSA
1.05V (11.1A)
S0/S1
P_+VCCIO_PG_5
+VCCSA_VREF
HPA02240
+VCCIO
0.95V (5.31A)
S0/S1
+12V
+5V
+3.3V
S_SLPS3#
+VCCIO_VREF
+5V
RT6220A
1 phase
+VPPDDR
2.5V(2.24A)
S0/S1/S3
P_+VPPDDR_EN_5
S_SLPS4#
P_+VPPDDR_TEST_3933
APW8723A 1 PHASE
NTMFS4C10NBT1G
+VDDQ
1.2V (12.87A)
S0/S1/S3
+VTTDDR
0.6V (0.75A)
S0/S1
UP8815
P_+VPPDDR_PG_5
S_SLPS4#
S_SLPS3#
DDR_VTT_CNTL
P_+VTTDDR_REF_10
+5VSB_ATX
+5V
+5VSB_ATX
O_3VSBSW#
EMA09N03AN + EMB45P03P
+5VDUAL
5V (18.92A)
S0/S1/S3
+5V
+5VSB_ATX
EMA06N03AN+EMB45P03P
+5V_DUAL_USBKB
5V (9.4A)
S0/S1/S3/S5
UP0109PSW8
+VCCPLL_OC
1.2V(0.11A)
S0/S1/S3
O4_VCCPLL_OC_REF
+5V
+5VSB_ATX
O_DEEPS5 & O_+5VDUAL_USBKB
AP9452GG + AP2301GN
+5VDUAL_AUX
5V (18.92A)
S0/S1/S3/S5
APW8723A
1 phase
+1.05V_A
1.05V(15A)
P_+1.8V_A_PG_10
+1.0V_A_VREF
+5VSB_ATX
O_DEEPS5
P06P03LCG
+5VSB
S0/S1/S3/S5
P06P03LCG
+3VSB
3.3V(0.47A)
S0/S1/S3/S5
O_DEEPS5
+5VSB_ATX
UZ2085G-AD-TN3-R
+3VSB_ATX
3.38V(2.29A)
+3.3V
O_3VSBSW#
AP9452GG + AP2301GN
+3VDUAL_AUX
3.3V(3.41A)
S0/S1/S3
APL5337KAI-TRG
+VCCST
1V(0.1A)
S0/S1/S3/S5
O4_VCCST_REF
APL5337KAI-TRG
+VCCPLL
1V(0.1A)
S0/S1/S3/S5
O4_VCCPLL_REF
+3.3V
P2003ED
+3V_PCIE_SLOT
S0/S1
+12V
P2003ED
+12V_PCIE_SLOT
S0/S1
+3VSB_ATX
+3.3V
O_DEEPS5 & O_+5VDUAL_USBKB
AP9452GG + AP2301GN
+3VDUAL_AUX
3.3V
S0/S1/S3/S5
<Variant Name>
Title
<Title>
Size
A2
Document Number
<Doc>
X99 Deluxe
Rev
<RevCode>
Date:
Tuesday, July 24, 2018
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5
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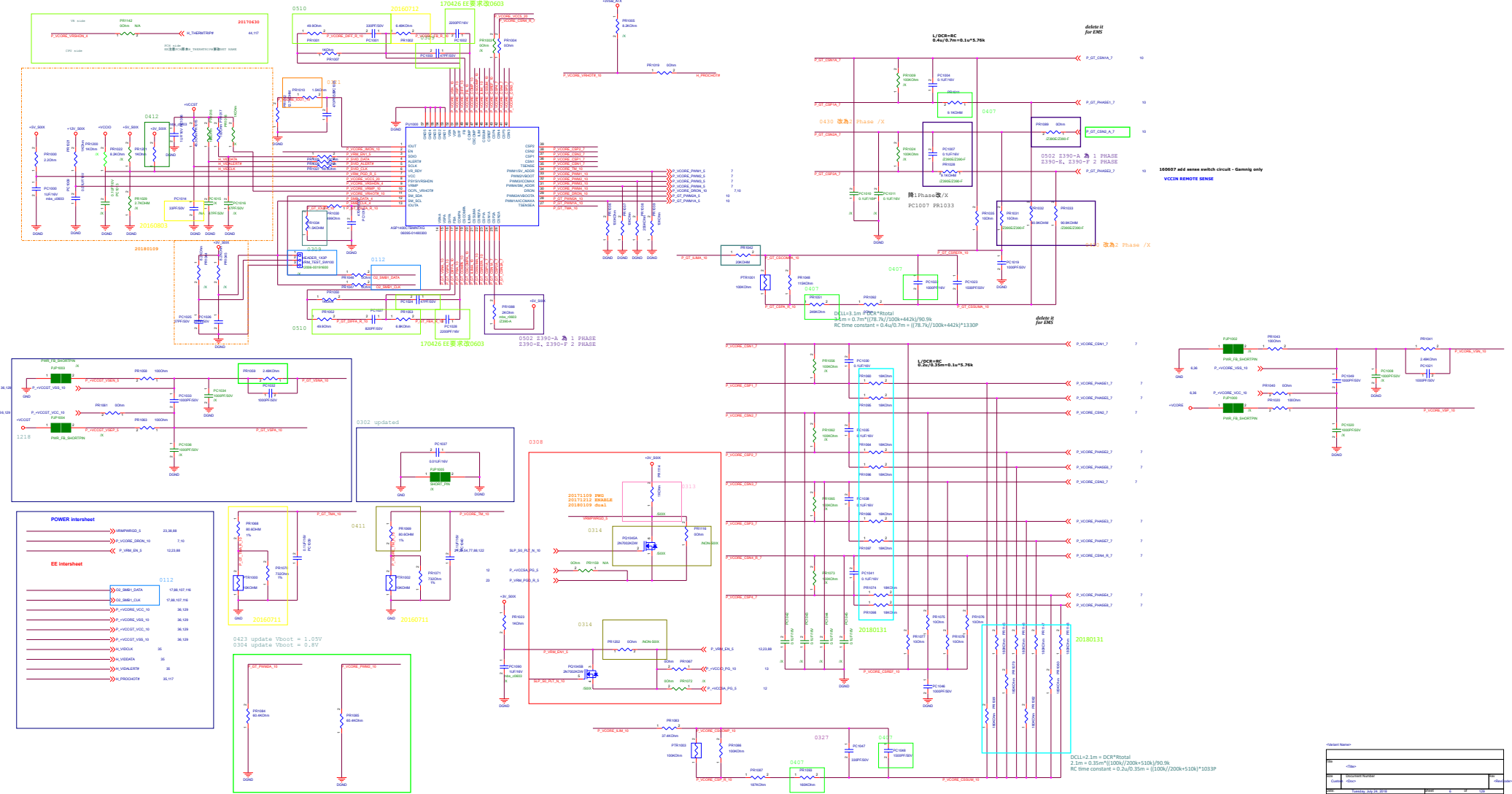
129


20170630
20160712
170426 EE要求改0603
20160803
20180109
0502 Z390-A 為 1 PHASE
Z390-I, Z390-F 2 PHASE
0423 update Vboot = 1.05V
0304 update Vboot = 0.8V
20160711
20180131
160607 add sense switch circuit - Gamnig only
VCCIN REMOTE SENSE
delete it for EMS
L/DCR=RC
0.4u/0.7m=0.1u*5.76k
0.2u/0.35m=0.1u*5.76k
降1Phase/X
PC1007 PR1033
DCLL=3.1m = DCR*Rtotal
3.1 m = 0.7m*[(78.7k//100k+442k)/90.9k
RC time constant = 0.4u/0.7m = ((78.7k//100k+442k)*1330P
DCLL=2.1m = DCR*Rtotal
2.1m = 0.35m*[(100k//200k+510k)/90.9k
RC time constant = 0.2u/0.35m = ((100k//200k+510k)*1033P
POWER intersheet
EE intersheet

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
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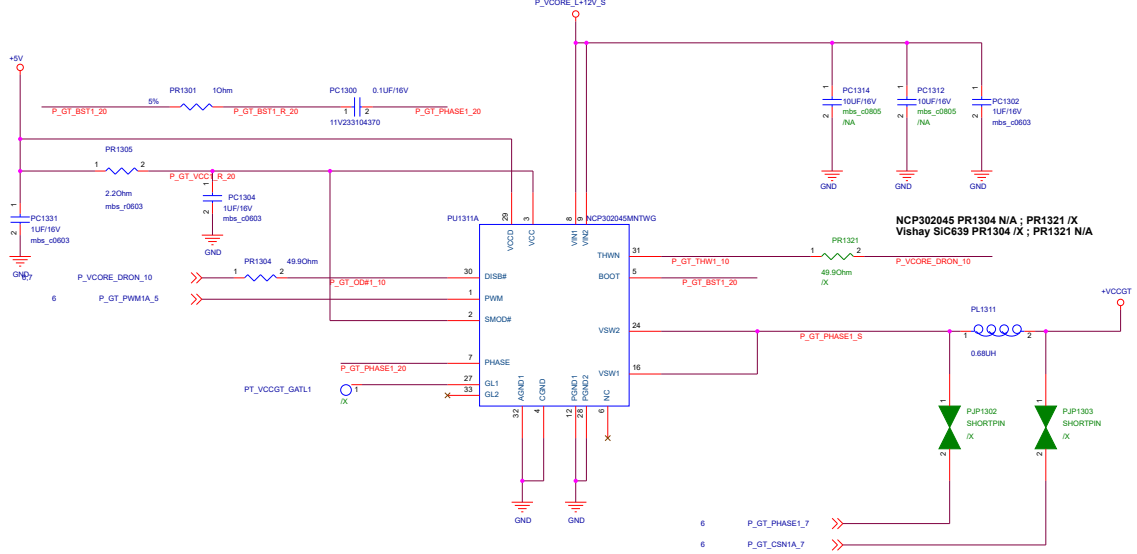
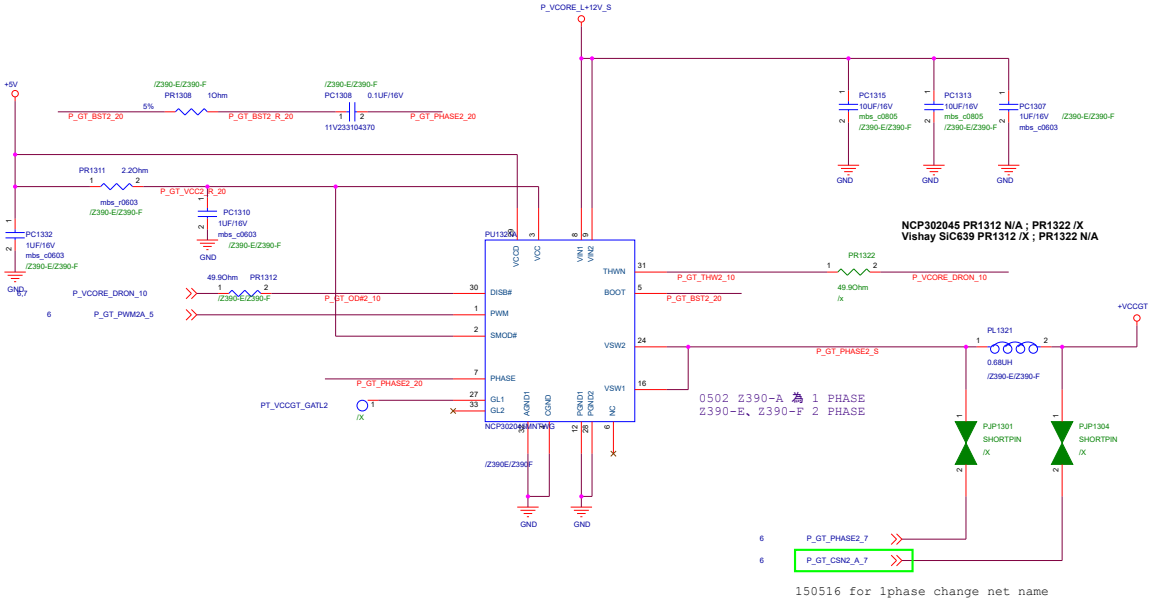
<Variant Name>

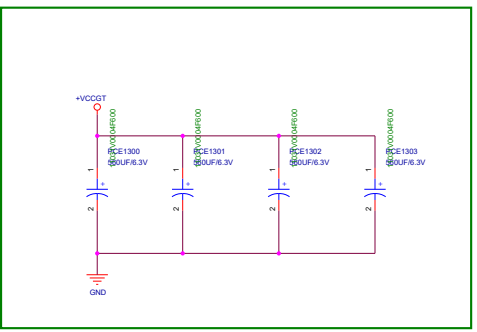
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, July 24, 2018	Sheet 9 of 129	



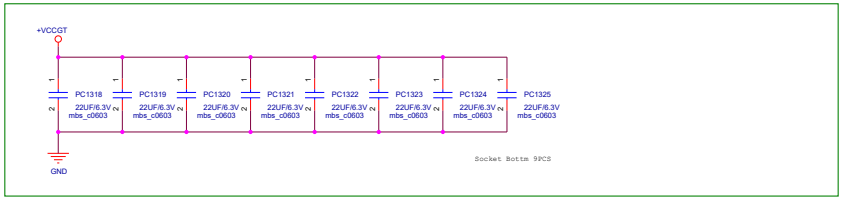


150516 for 1phase change net name

20160426 change to MS footprint



2015.03.25 Remove PC7004, PC7005, PC7007, PC7008, PC7011, PCB7033 for layout routing

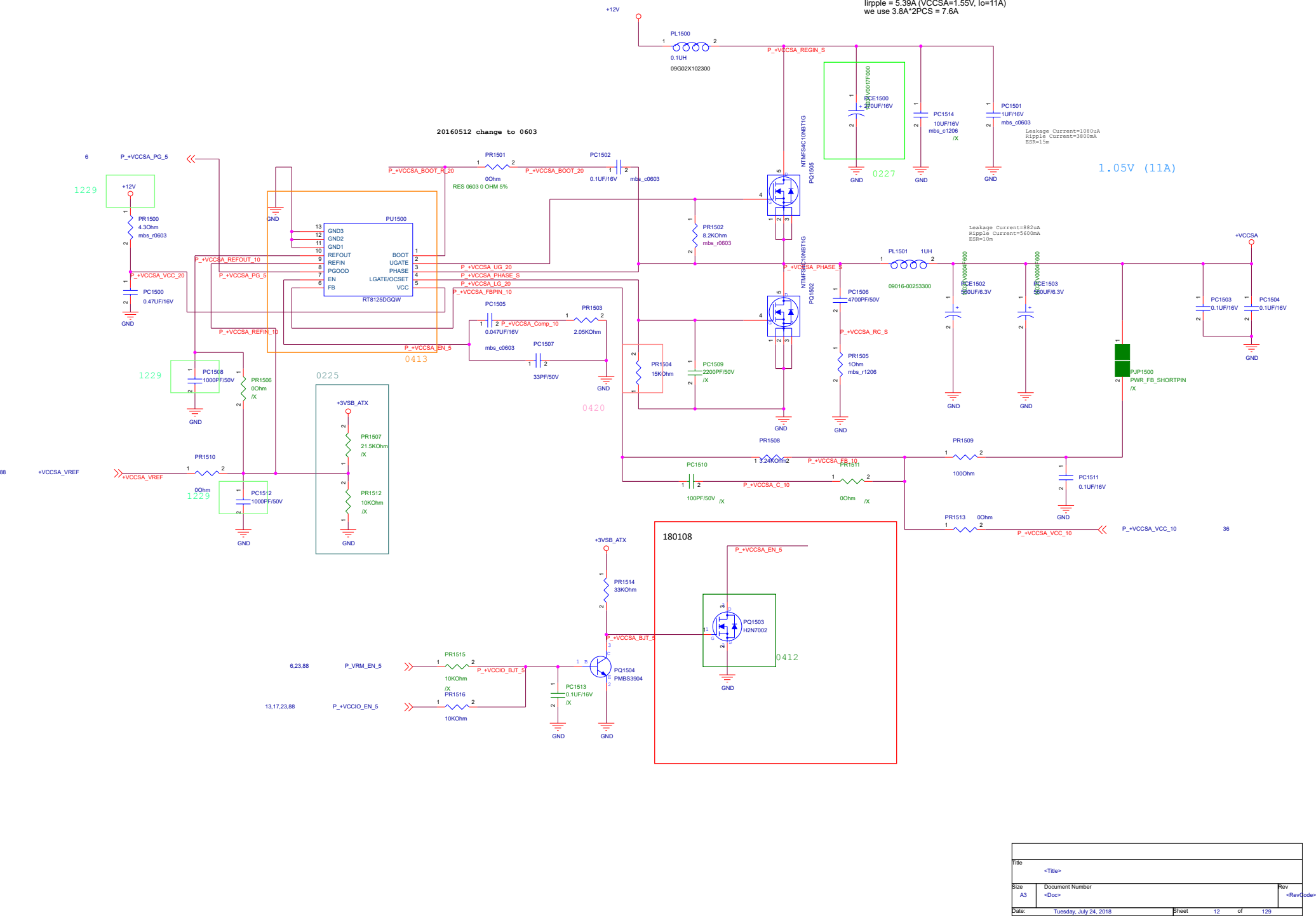


<Variant Name>

ASUSTek COMPUTER INC.	Title : VCCGT DRIVER	
	Engineer: RAY	
Size: A2	Project Name: SkyLake VC	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 10 of 129	

<Variant Name>

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, July 24, 2018	Sheet 11 of 129	



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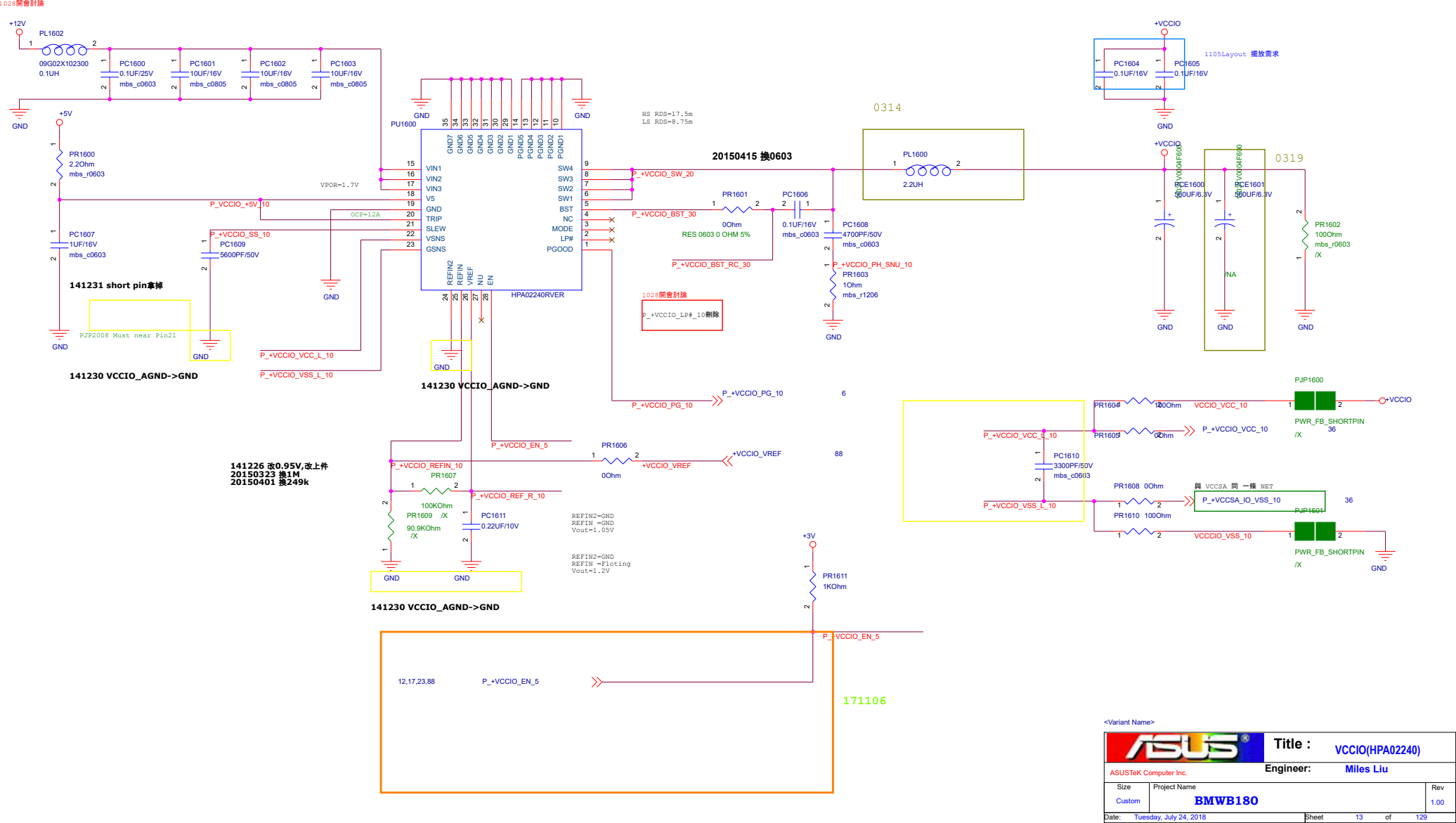
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, July 24, 2018	Sheet 12 of 129	


1028開會討論
+12V
PL1602
09G02X102300
0.1UH
PC1600
0.1UF/25V
mbs_c0603
PC1601
10UF/16V
mbs_c0805
PC1602
10UF/16V
mbs_c0805
PC1603
10UF/16V
mbs_c0805
GND
+5V
PR1600
2.2Ohm
mbs_r0603
PC1607
1UF/16V
mbs_c0603
141231 short pin拿掉
PJP2008 Must near Pin21
141230 VCCIO_AGND->GND
PU1600
HPA02240RVER
VIN1
VIN2
VIN3
V5
GND
TRIP
SLEW
VSNS
GSNS
SW4
SW3
SW2
SW1
BST
NC
MODE
LP#
PGOOD
REFIN2
REFIN
VREF
NU
EN
VPOR=1.7V
OCP=12A
P_+VCCIO_+5V_10
P_+VCCIO_SS_10
PC1609
5600PF/50V
P_+VCCIO_VCC_L_10
P_+VCCIO_VSS_L_10
HS RDS=17.5m
LS RDS=8.75m
20150415 換0603
P_+VCCIO_SW_20
P_+VCCIO_BST_30
PR1601
0Ohm
RES 0603 0 OHM 5%
PC1606
0.1UF/16V
mbs_c0603
PC1608
4700PF/50V
mbs_c0603
P_+VCCIO_BST_RC_30
P_+VCCIO_PH_SNU_10
PR1603
1Ohm
mbs_r1206
1028開會討論
P_+VCCIO_LP#_10刪除
0314
PL1600
2.2UH
+VCCIO
PC1604
0.1UF/16V
PC1605
0.1UF/16V
1105Layout 擺放需求
PCE1600
330UF/6.3V
PCE1601
330UF/6.3V
0319
PR1602
100Ohm
mbs_r0603
/X
NA
P_+VCCIO_PG_10
P_+VCCIO_PG_10
P_+VCCIO_EN_5
PR1606
0Ohm
+VCCIO_VREF
P_+VCCIO_REFIN_10
PR1607
100KOhm
PR1609 /X
90.9KOhm
/X
P_+VCCIO_REF_R_10
PC1611
0.22UF/10V
REFIN2=GND
REFIN =GND
Vout=1.05V
REFIN2=GND
REFIN =Floting
Vout=1.2V
141226 改0.95V,改上件
20150323 換1M
20150401 換249k
141230 VCCIO_AGND->GND
+3V
PR1611
1KOhm
P_+VCCIO_EN_5
12,17,23,88
P_+VCCIO_EN_5
171106
PJP1600
PR1604
120Ohm
VCCIO_VCC_10
PWR_FB_SHORTPIN
/X
PR1605
0Ohm
P_+VCCIO_VCC_10
PC1610
3300PF/50V
mbs_c0603
PR1608 0Ohm
與 VCCSA 同 一條 NET
P_+VCCSA_IO_VSS_10
PJP1601
PR1610 100Ohm
VCCIO_VSS_10
PWR_FB_SHORTPIN
/X
<Variant Name>
Title : VCCIO(HPA02240)
Engineer: Miles Liu
ASUSTeK Computer Inc.
Size Custom
Project Name BMWB180
Rev 1.00
Date: Tuesday, July 24, 2018
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<Variant Name>

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
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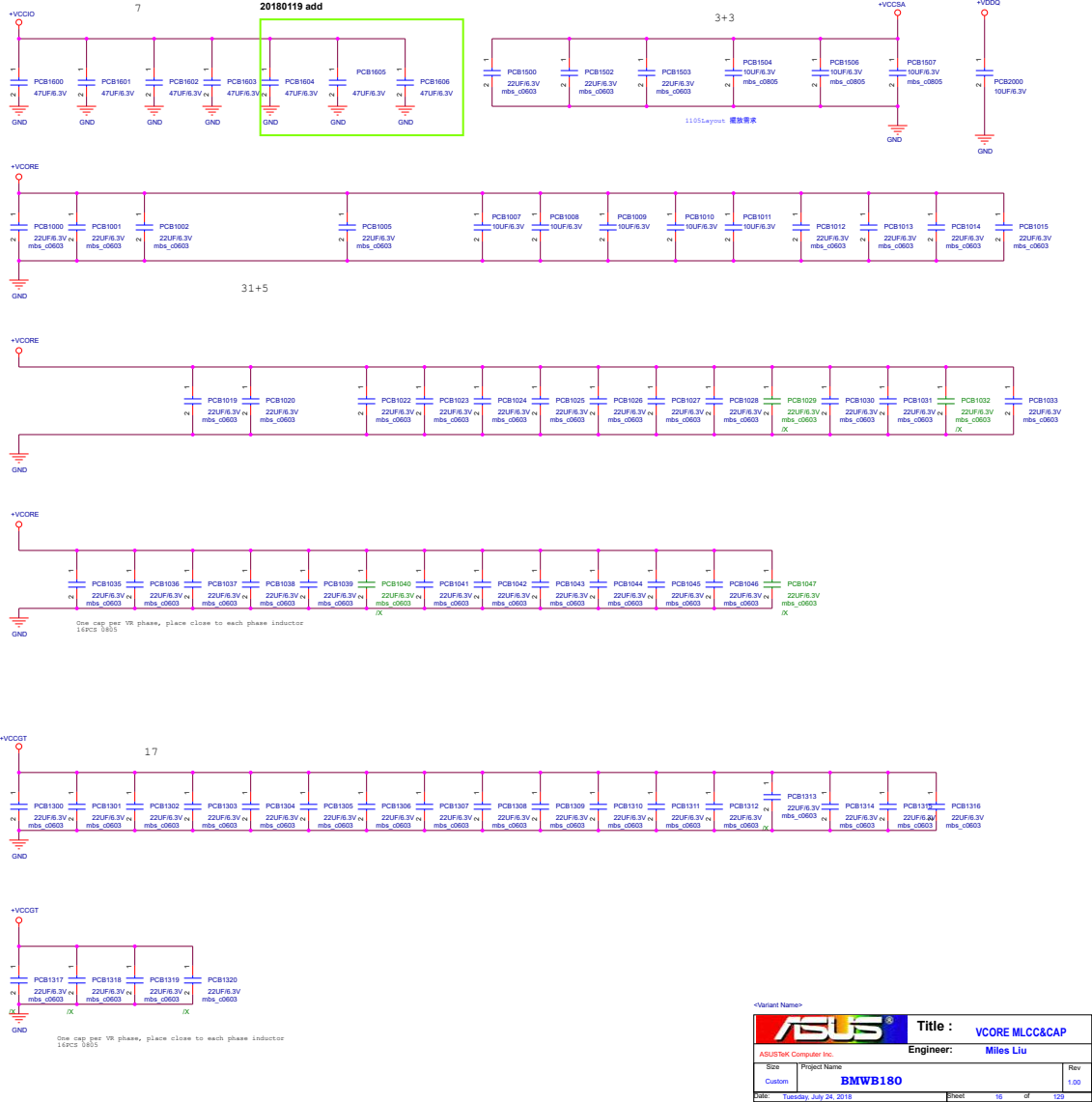
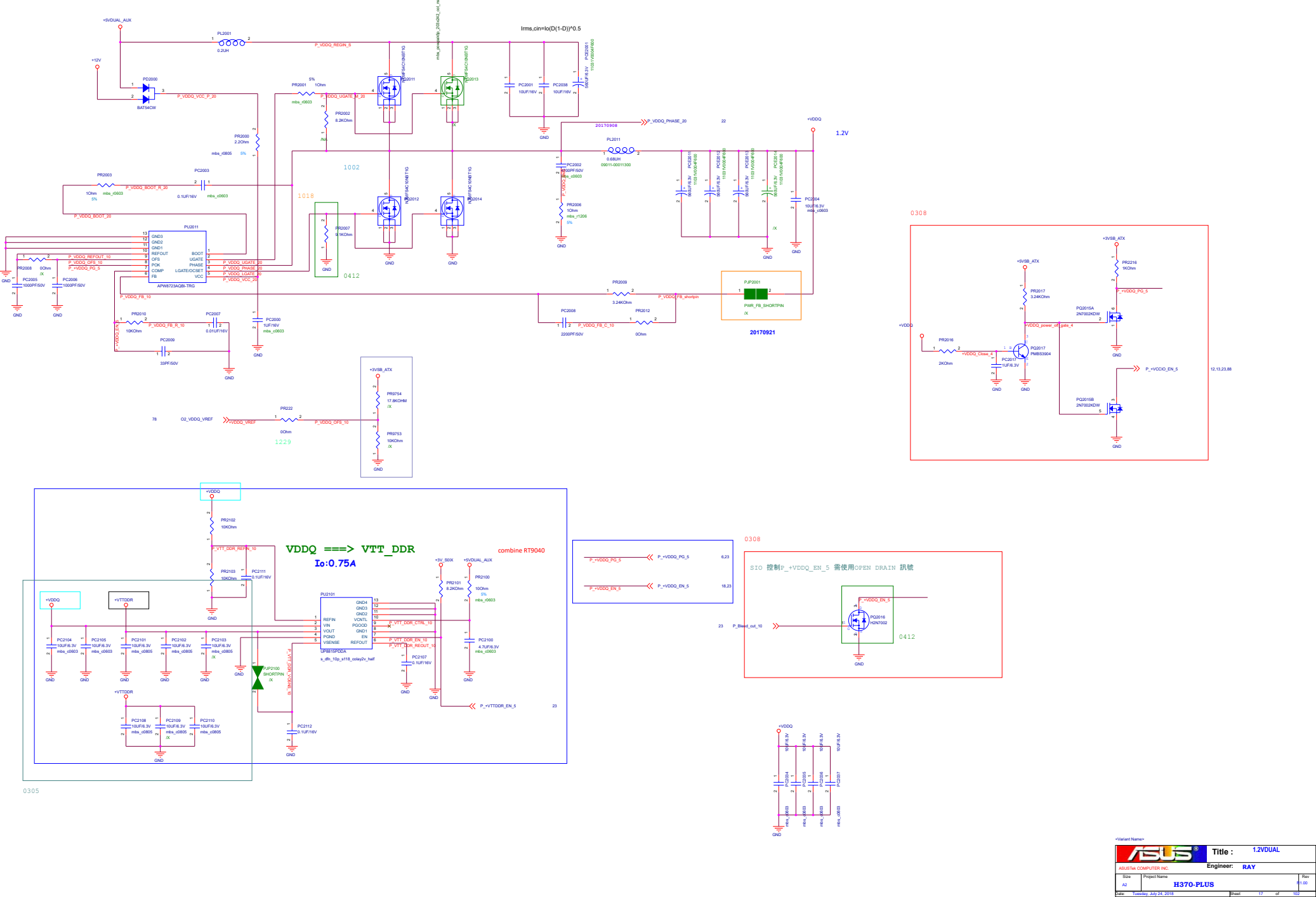
<Variant Name>

Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, July 24, 2018	Sheet 15 of 129	



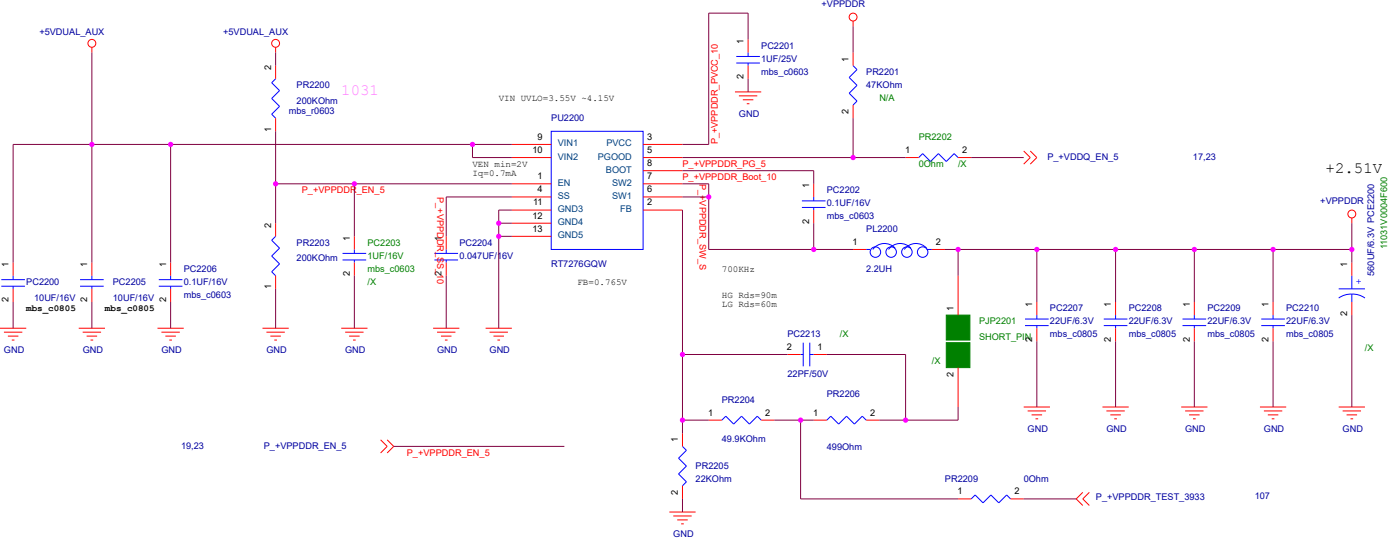
<Variant Name>

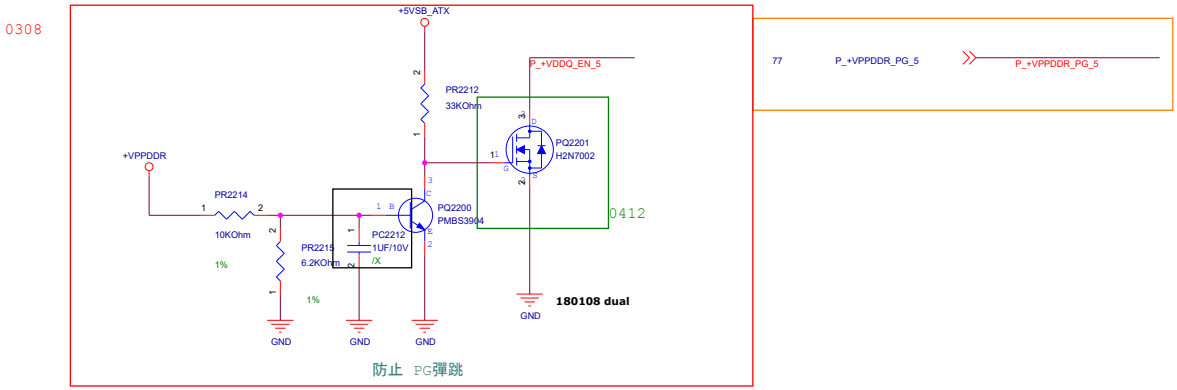
ASUSTeK Computer Inc.	Title :	VCORE MLCC&CAP
	Engineer:	Miles Liu
Size: Custom	Project Name: BMWB180	Rev: 1.00
Date: Tuesday, July 24, 2018	Sheet 16 of 129	



<Variant Name>

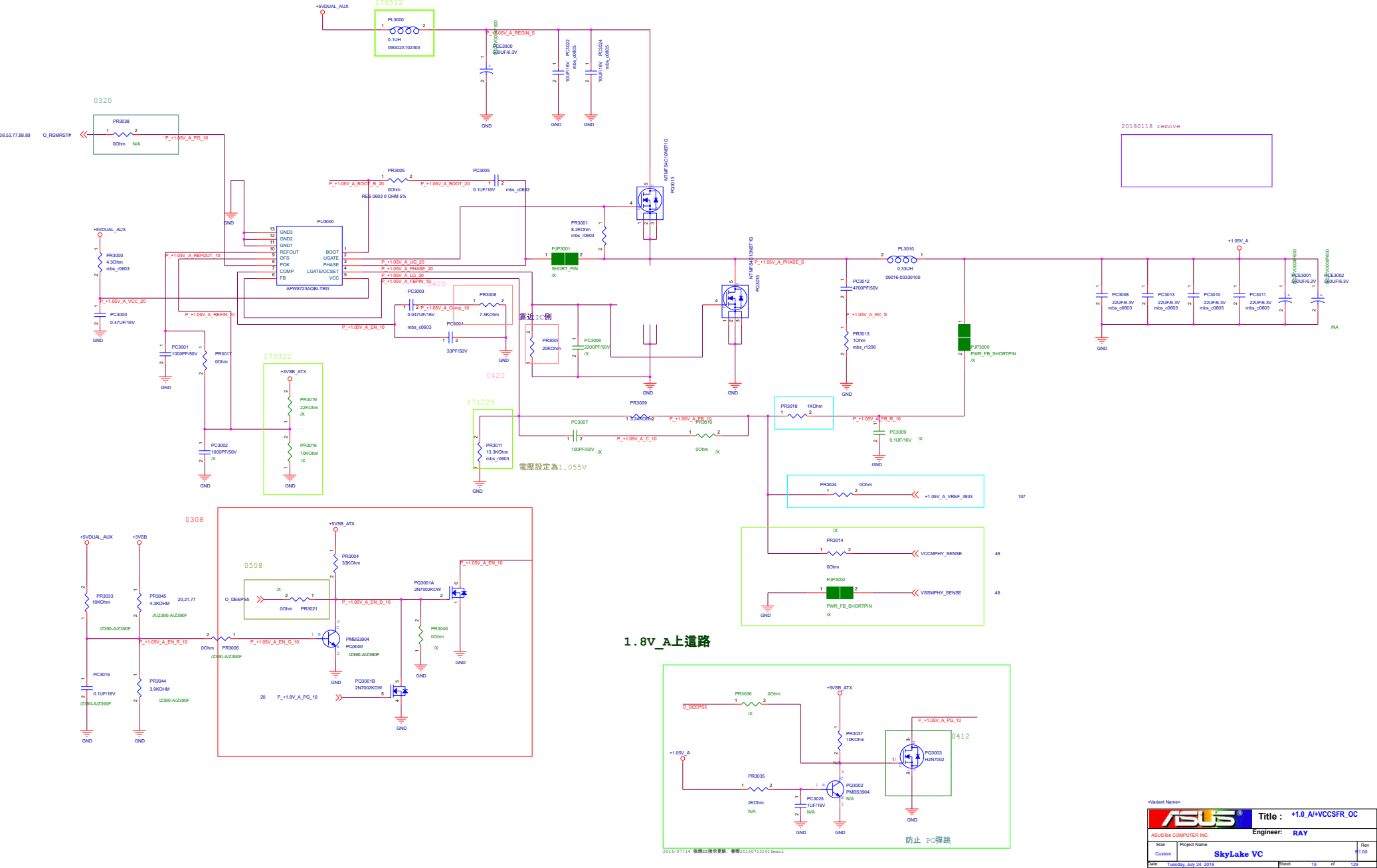
ASUSTek COMPUTER INC.	Title : 1.2VDUAL	
	Engineer: RAY	
Size: A2	Project Name: H370-PLUS	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet: 17 of 102	



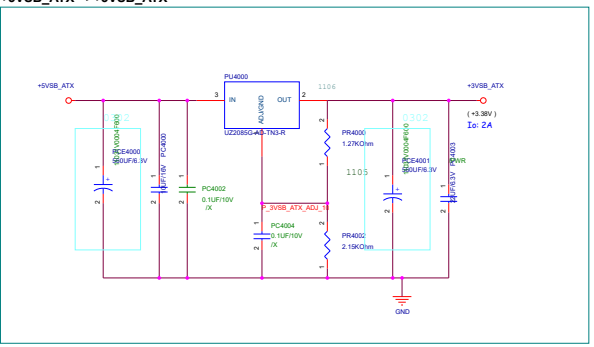


<Variant Name>

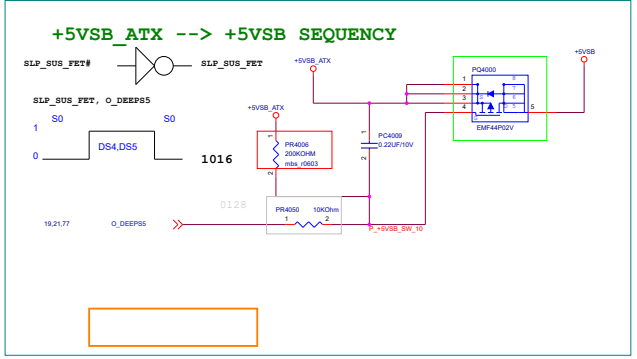
ASUSTek Computer Inc.	Title :	+VPPDDR(TR8125D)	
	Engineer:	Miles Liu	
Size: A3	Project Name: BMWB180		Rev: 1.01
Date: Tuesday, July 24, 2018	Sheet 18 of 129		


170512
PL3000
0.1UH
09G02X102300
PCE3000
560UF/6.3V
PC3022
100UF/16V
mbs_c0805
PC3024
10UF/16V
mbs_c0805
GND
0320
PR3038
0Ohm N/A
P_+1.05V_A_PG_10
O_RSMRST#
20180118 remove
PR3005
0Ohm
RES 0603 0 OHM 5%
PC3005
0.1UF/16V
mbs_c0603
NTMFS4C10NBT1G
PQ3013
PR3001
8.2KOhm
mbs_r0603
PJP3001
SHORT_PIN
/X
PU3000
APW8723AQBI-TRG
GND3
GND2
GND1
REFOUT
OFS
POK
COMP
FB
BOOT
UGATE
PHASE
LGATE/OCSET
VCC
+5VDUAL_AUX
PR3000
4.3Ohm
mbs_r0603
PC3000
0.47UF/16V
P_+1.05V_A_REFOUT_10
P_+1.05V_A_VCC_20
P_+1.05V_A_REFIN_10
P_+1.05V_A_UG_20
P_+1.05V_A_PHASE_20
P_+1.05V_A_LG_30
P_+1.05V_A_FBPIN_10
0420
PC3003
0.047UF/16V
PR3008
7.5KOhm
PC3004
33PF/50V
P_+1.05V_A_Comp_10
P_+1.05V_A_EN_10
靠近IC側
PR3007
20KOhm
PC3006
2200PF/50V
/X
PC3001
1000PF/50V
PR3017
0Ohm
PC3002
1000PF/50V
/X
170322
+3VSB_ATX
PR3019
22KOhm
/X
PR3016
10KOhm
/X
0420
171229
PR3011
13.3KOhm
mbs_r0603
電壓設定為1.055V
PR3009
1.24KOhm/2
PC3007
100PF/50V
/X
PR3010
0Ohm
/X
P_+1.05V_A_C_10
P_+1.05V_A_FB_10
P_+1.05V_A_FB_R_10
PR3018
1KOhm
PC3009
0.1UF/16V
/X
PR3024
0Ohm
+1.05V_A_VREF_3933
107
/X
PR3014
0Ohm
VCCMPHY_SENSE
48
PJP3002
PWR_FB_SHORTPIN
/X
VSSMPHY_SENSE
48
NTMFS4C10NBT1G
PQ3015
P_+1.05V_A_PHASE_S
PL3010
0.33UH
09016-00330100
PC3012
4700PF/50V
P_+1.05V_A_RC_S
PR3013
1Ohm
mbs_r1206
PJP3000
PWR_FB_SHORTPIN
/X
+1.05V_A
PCE3001
560UF/6.3V
PCE3002
560UF/6.3V
PC3008
22UF/6.3V
mbs_c0603
PC3013
22UF/6.3V
mbs_c0603
PC3010
22UF/6.3V
mbs_c0603
PC3011
22UF/6.3V
mbs_c0603
/NA
0308
+5VDUAL_AUX
+3VSB
+5VSB_ATX
PR3033
10KOhm
/Z390-A/Z390F
PR3045
4.3KOHM
20,21,77
/X/Z390-A/Z390F
PR3044
3.9KOHM
/Z390-A/Z390F
PC3016
0.1UF/16V
/Z390-A/Z390F
0508
O_DEEPSS
/X
0Ohm
PR3021
PR3004
33KOhm
P_+1.05V_A_EN_10
P_+1.05V_A_EN_D_10
PQ3001A
2N7002KDW
PR3046
0Ohm
/X
P_+1.05V_A_EN_R_10
P_+1.05V_A_EN_G_10
0Ohm
PR3006
/Z390-A/Z390F
PMBS3904
PQ3000
/Z390-A/Z390F
PQ3001B
2N7002KDW
20
P_+1.8V_A_PG_10
1.8V_A上這路
PR3036
0Ohm
O_DEEPSS
/X
PR3037
10KOhm
N/A
PQ3003
H2N7002
0412
PR3035
2KOhm
N/A
PQ3002
PMBS3904
N/A
PC3025
1UF/16V
N/A
P_+1.05V_A_PG_10
+1.05V_A
防止 PG彈跳
2016/07/14 依照ECR指示更新, 參照20160713191 6mail
<Variant Name>
ASUSTek COMPUTER INC.
Title : +1.0_A/+VCCSFR_OC
Engineer: RAY
Size
Custom
Project Name
SkyLake VC
Rev
R1.00
Date: Tuesday, July 24, 2018
Sheet 19 of 129

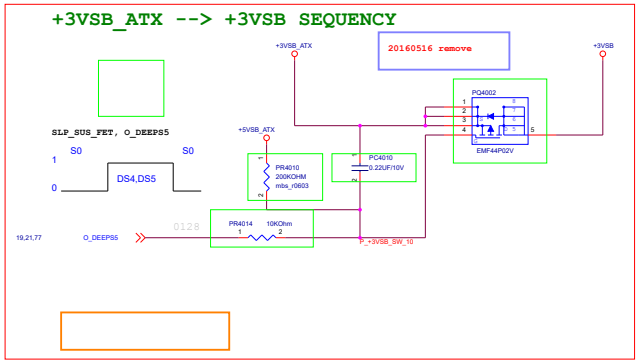
+5VSB_ATX =>+3VSB_ATX



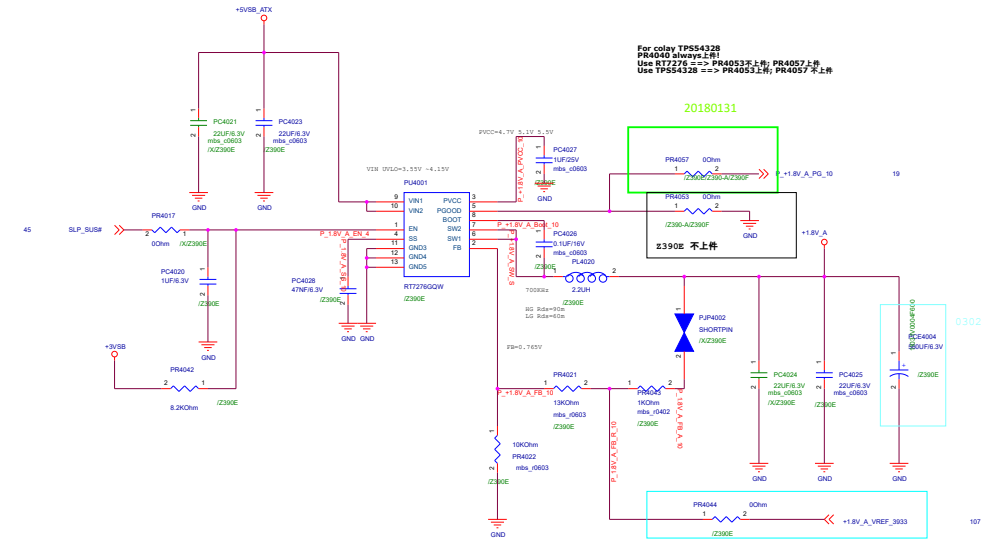
+5VSB_ATX --> +5VSB SEQUENCY

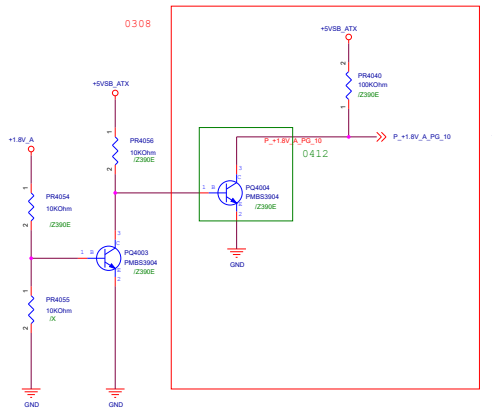


+3VSB_ATX --> +3VSB SEQUENCY



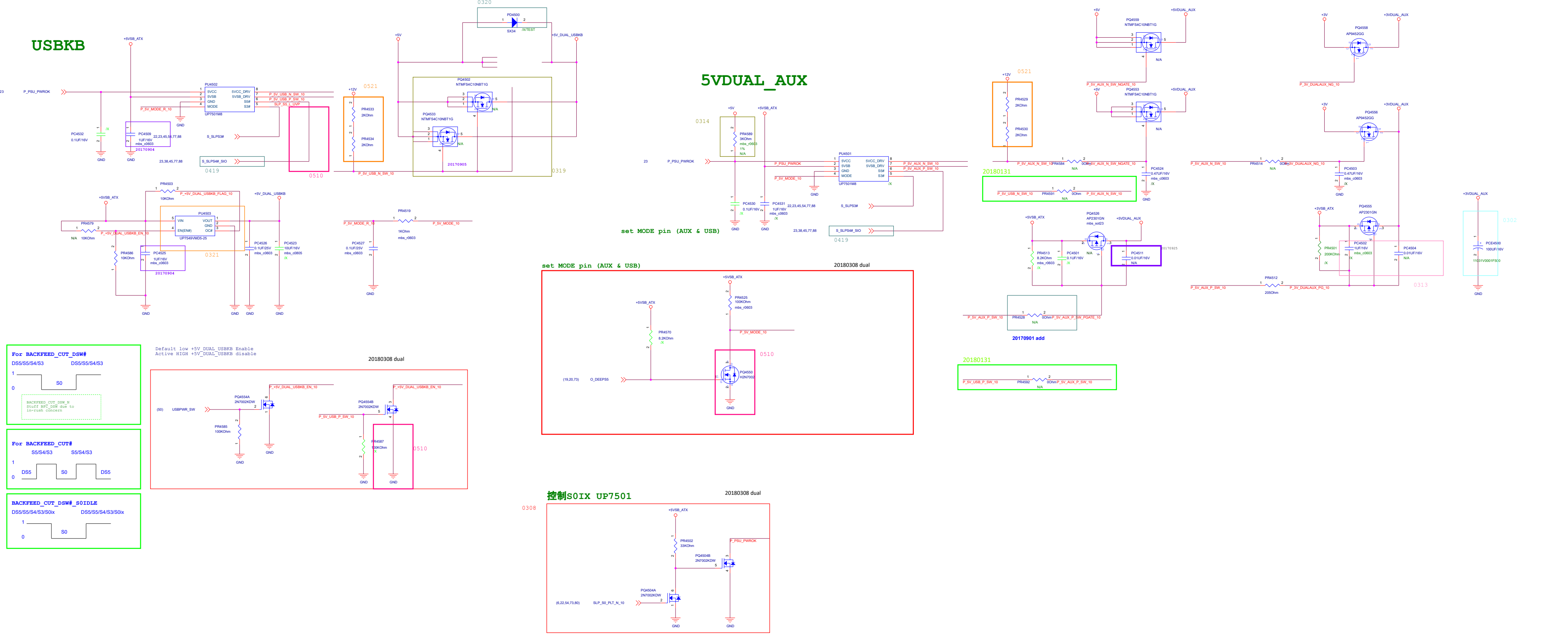
+1.8V_A



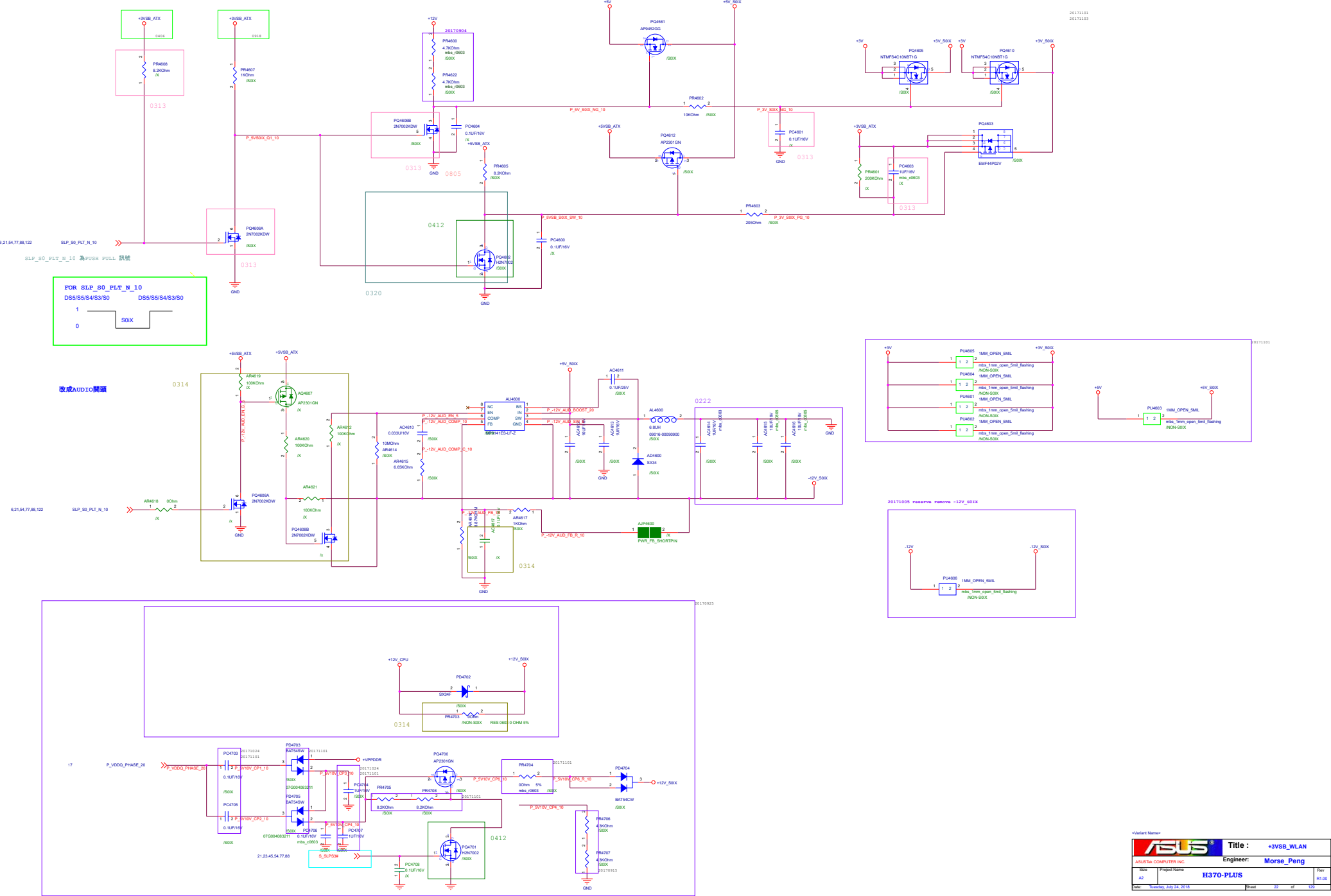


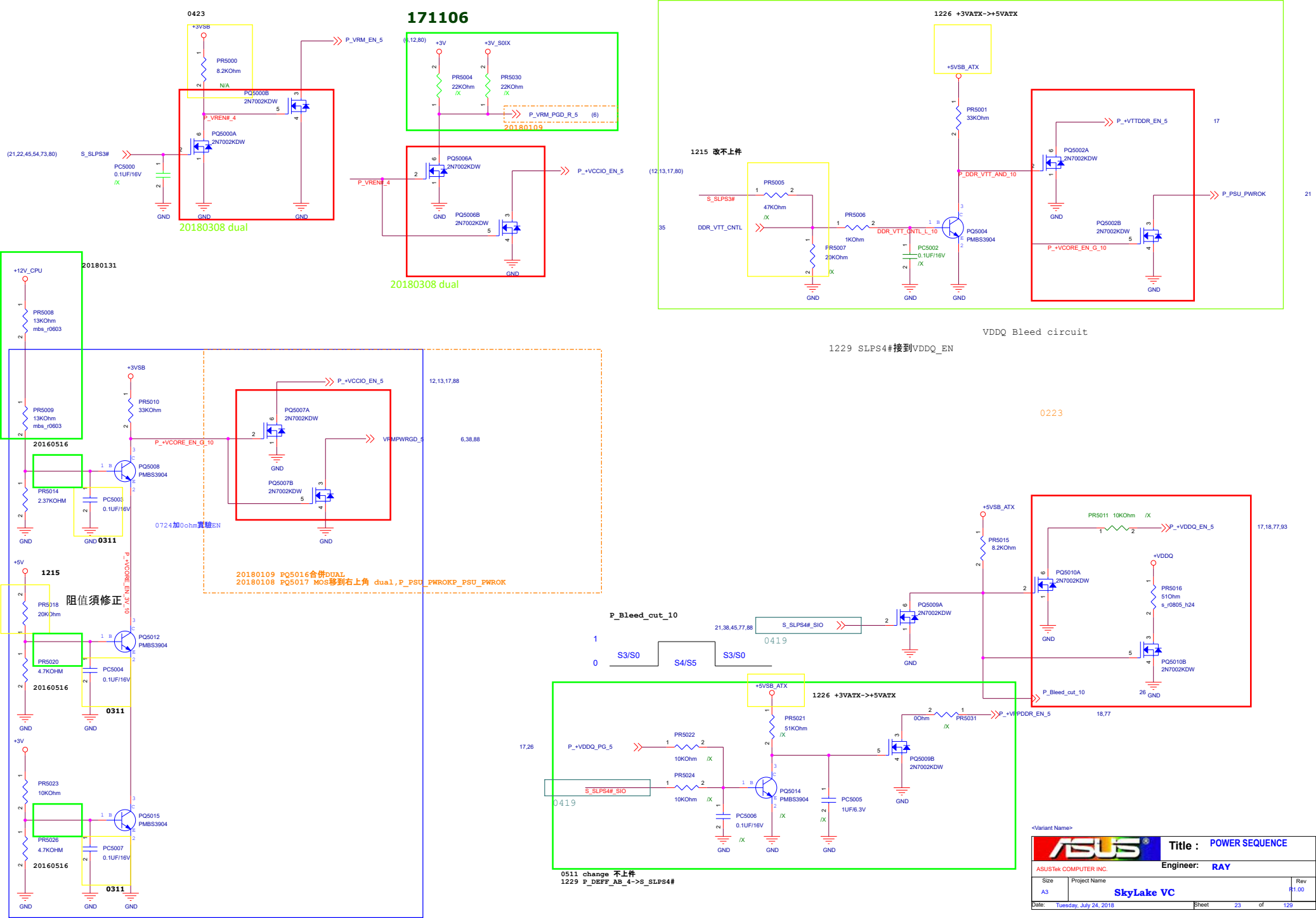
<Variant Name>

ASUSTek Computer Inc.	Title :	+VPPDDR(TR8125D)
	Engineer:	Miles Liu
Size: A2	Project Name: BMWB180	Rev: 1.01
Date: Tuesday, July 24, 2018	Sheet: 20 of 129	



Title: <Title>
Size: D
Document Number: <Doc>
Rev: <RevCode>
Date: Tuesday, July 24, 2018
Sheet 21 of 129


+3VSB_ATX
PR4608 8.2KOhm /X
PR4607 1KOhm /S0IX
+12V
20170904
PR4600 4.7KOhm mba_r0603 /S0IX
PR4622 4.7KOhm mba_r0603 /S0IX
PQ4606B 2N7002KDW
PC4604 0.1UF/16V /X
P_5VS0IX_Q1_10
PQ4606A 2N7002KDW
SLP_S0_PLT_N_10
SLP_S0_PLT_N_10 為PUSH PULL 訊號
FOR SLP_S0_PLT_N_10
DS5/S5/S4/S3/S0
S0IX
PR4605 8.2KOhm /S0IX
PQ4602 H2N7002
PC4600 0.1UF/16V /X
P_5VSB_S0IX_SW_10
PQ4561 AP9452GG
+5V_S0IX
PR4602 10KOhm /S0IX
P_5V_S0IX_NG_10
P_3V_S0IX_NG_10
PQ4605 NTMFS4C10NBT1G
PQ4610 NTMFS4C10NBT1G
PQ4612 AP2301GN
PC4601 0.1UF/16V /X
PQ4603 EMF44P02V
PR4601 200KOhm /X
PC4603 1UF/16V mba_c0603 /X
PR4603 205Ohm /S0IX
P_3V_S0IX_PG_10
改成AUDIO開頭
AR4619 100KOhm /X
AQ4607 AP2301GN /X
AR4620 100KOhm /X
AR4621 100KOhm /X
AR4622 100KOhm /X
AR4618 0Ohm /X
PQ4608A 2N7002KDW
PQ4608B 2N7002KDW
P_-12V_AUD_EN_S
P_-12V_AUD_COMP_10
P_-12V_AUD_COMP_C_10
AC4610 0.033UF/16V /S0IX
10MOhm
AR4614 /S0IX
AR4615 6.65KOhm /S0IX
AU4600 APW7141ES-LF-Z
P_-12V_AUD_BOOST_20
AC4611 0.1UF/25V /S0IX
AL4600 6.8UH 09016-80090900 /S0IX
AD4600 SX34 /S0IX
-12V_S0IX
P_-12V_AUD_FB_10
AR4617 1KOhm /S0IX
AJP4600 PWR_FB_SHORTPIN
20171005 reserve remove -12V_S0IX
PU4605 1MM_OPEN_SMIL
PU4604 1MM_OPEN_SMIL
PU4601 1MM_OPEN_SMIL
PU4602 1MM_OPEN_SMIL
PU4603 1MM_OPEN_SMIL
PU4606 1MM_OPEN_SMIL
mba_1mm_open_5mil_flashing /NON-S0IX
PD4702 SX34F
PR4703 /S0IX
PR4704 0Ohm 5% mba_r0603 /S0IX
PD4704 BAT54CW /S0IX
PD4703 BAT54SW
PC4703 0.1UF/16V /S0IX
PC4705 0.1UF/16V /S0IX
PC4706 0.1UF/16V /S0IX
PC4707 1UF/16V /S0IX
PC4708 0.1UF/16V /X
PQ4700 AP2301GN
PR4705 8.2KOhm /S0IX
PR4706 4.3KOhm /S0IX
PR4707 4.3KOhm /S0IX
PQ4701 H2N7002
P_5V10V_CP1_10
P_5V10V_CP2_10
P_5V10V_CP3_10
P_5V10V_CP4_10
P_VDDQ_PHASE_20
+VPPDDR
+12V_CPU
+12V_S0IX
S_SLPS3#
07G004083211
07G004083211
RES 0603 0 OHM 5%
/NON-S0IX
0313
0320
0412
0805
0314
0222
GND
+3V
+3V_S0IX
+5VSB_ATX
+5V_S0IX
+12V_S0IX
+12V_CPU
+VPPDDR
+8V
-12V
-12V_S0IX
P_VDDQ_PHASE_20
SLP_S0_PLT_N_10
S_SLPS3#
20171101
20171103
20170925
20171024
20171101
ASUSTeK COMPUTER INC.
Title : +3VSB_WLAN
Engineer: Morse_Peng
Size A2
Project Name H370-PLUS
Rev R1.00
Date: Tuesday, July 24, 2018
Sheet 22 of 120


0423
171106
+3VSB
PR5000
8.2KOhm
N/A
PQ5000B
2N7002KDW
P_VREN#_4
PQ5000A
2N7002KDW
S_SLPS3#
PC5000
0.1UF/16V
/X
GND
P_VRM_EN_5
20180308 dual
(6,12,80)
+3V
+3V_S0IX
PR5004
22KOhm
/X
PR5030
22KOhm
/X
P_VRM_PGD_R_5
(6)
20180109
PQ5006A
2N7002KDW
PQ5006B
2N7002KDW
P_+VCCIO_EN_5
20180308 dual
1226 +3VATX->+5VATX
+5VSB_ATX
PR5001
33KOhm
P_DDR_VTT_AND_10
1215 改不上件
(12,13,17,80)
PR5005
47KOhm
/X
S_SLPS3#
DDR_VTT_CNTL
35
PR5006
1KOhm
DDR_VTT_CNTL_L_10
PQ5004
PMBS3904
FR5007
20KOhm
/X
PC5002
0.1UF/16V
/X
PQ5002A
2N7002KDW
PQ5002B
2N7002KDW
P_+VTTDDR_EN_5
17
P_PSU_PWROK
21
P_+VCORE_EN_G_10
VDDQ Bleed circuit
1229 SLPS4#接到VDDQ_EN
20180131
+12V_CPU
PR5008
13KOhm
mbs_r0603
PR5009
13KOhm
mbs_r0603
20160516
+3VSB
PR5010
33KOhm
P_+VCORE_EN_G_10
PQ5007A
2N7002KDW
PQ5007B
2N7002KDW
P_+VCCIO_EN_5
12,13,17,88
VRMPWRGD_5
6,38,88
PQ5008
PMBS3904
PR5014
2.37KOHM
PC5003
0.1UF/16V
GND
0311
0724加0ohm實驗EN
20180109 PQ5016合併DUAL
20180108 PQ5017 MOS移到右上角 dual,P_PSU_PWROKP_PSU_PWROK
0223
+5V
1215
阻值須修正
PR5018
20KOhm
PR5020
4.7KOHM
20160516
PQ5012
PMBS3904
PC5004
0.1UF/16V
0311
P_+VCORE_EN_3V_10
+3V
PR5023
10KOhm
PR5026
4.7KOHM
20160516
PQ5015
PMBS3904
PC5007
0.1UF/16V
0311
P_Bleed_cut_10
1
0
S3/S0
S4/S5
S3/S0
21,38,45,77,88
S_SLPS4#_SIO
0419
PQ5009A
2N7002KDW
+5VSB_ATX
PR5015
8.2KOhm
PR5011 10KOhm /X
P_+VDDQ_EN_5
17,18,77,93
PQ5010A
2N7002KDW
+VDDQ
PR5016
51Ohm
s_r0805_h24
PQ5010B
2N7002KDW
26
P_Bleed_cut_10
1226 +3VATX->+5VATX
PR5021
51KOhm
/X
PR5031
0Ohm
/X
P_+VPPDDR_EN_5
18,77
17,26
P_+VDDQ_PG_5
PR5022
10KOhm
/X
PR5024
10KOhm
/X
S_SLPS4#_SIO
0419
PQ5014
PMBS3904
PC5006
0.1UF/16V
/X
PC5005
1UF/6.3V
/X
PQ5009B
2N7002KDW
0511 change 不上件
1229 P_DEFF_AB_4->S_SLPS4#
<Variant Name>
Title : POWER SEQUENCE
ASUSTek COMPUTER INC.
Engineer: RAY
Size A3
Project Name SkyLake VC
Rev R1.00
Date: Tuesday, July 24, 2018
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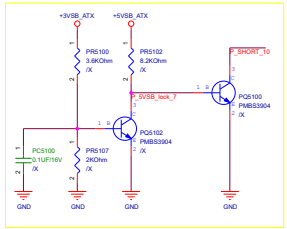
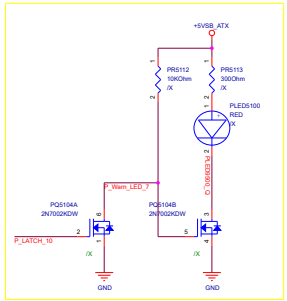
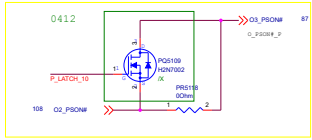
All Gaming only

20150715

Default unstuff vcore OVP circuit

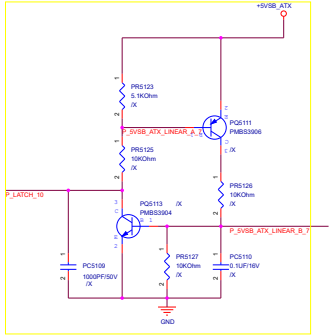


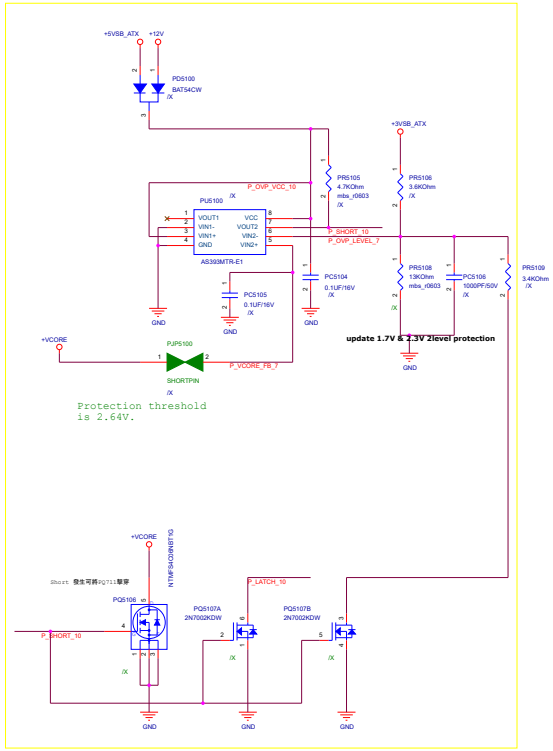




GND

141106 拿掉RC,C,換1000P





20160602 update /Test
0210 update form Z170-A

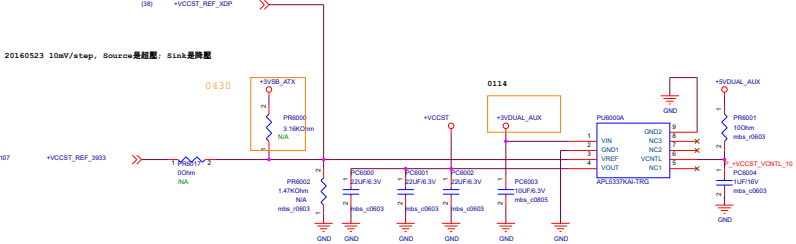
20160520 follow Strix Z270

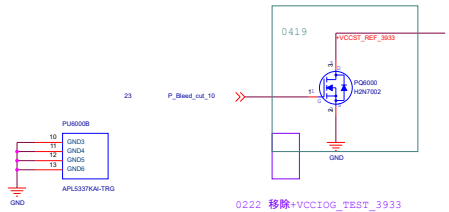
20180116 remove

0222 移除+5VSB_AUD

<Variant Name>

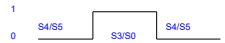
Title	<Title>	
Size: Custom	Document Number: <Doc>	Rev: <RevCode>
Date: Tuesday, July 24, 2018	Sheet 25 of 129	





0222 移除+VCCIOG_TEST_3933

P_Bleed_cut_10



Reserved VCCPLL & VCCST Merge 0ohm

0225移除+VCCPLL_OC與+VCCPLL

+VDDQ Power Monitor

+5V Power Monitor

+VCORE Power Monitor

+VCCIO Power Monitor

+5VSB_ATX Power Monitor

+3VSB_ATX Power Monitor

+VCCGT Power Monitor

+VCCSA Power Monitor

+1.05V_A Power Monitor

A1	A0	Address	
Gnd	Gnd	1000000 ; 40	
Gnd	Vcc	1000001 ; 41	
Gnd	SDA	1000010 ; 42	
Gnd	SCL	1000011 ; 43	
Vcc	Gnd	1000100 ; 44	+5VSB
Vcc	Vcc	1000101 ; 45	
Vcc	SDA	1000110 ; 46	
Vcc	SCL	1000111 ; 47	
SDA	Gnd	1001000 ; 48	
SDA	Vcc	1001001 ; 49	
SDA	SDA	1001010 ; 4A	
SDA	SCL	1001011 ; 4B	
SCL	Gnd	1001100 ; 4C	+5V
SCL	Vcc	1001101 ; 4D	+3V
SCL	SDA	1001110 ; 4E	
SCL	SCL	1001111 ; 4F	

<Variant Name>

ASUSTek COMPUTER INC.

Title : Power monitor-1

Engineer: RAY

Size	Project Name	Rev
A2	SkyLake VC	R1.00

Date: Tuesday, July 24, 2018 Sheet 27 of 139

+3V Power Monitor

+12V Power Monitor

<Variant Name>

Title : Power monitor-2

ASUSTek COMPUTER INC.

Engineer: RAY

Size	Project Name	Rev
A2	SkyLake VC	0.1.00

Date: Tuesday, July 24, 2018 Sheet 28 of 139

+VDDQ Power Monitor

+5V Power Monitor

+VCORE Power Monitor

+VCCIO Power Monitor

+5VSB_ATX Power Monitor

+3VSB_ATX Power Monitor

+VCCGT Power Monitor

+VCCSA Power Monitor

+1.05V_A Power Monitor

A1	A0	Address	
Gnd	Gnd	1000000 ; 40	
Gnd	Vcc	1000001 ; 41	
Gnd	SDA	1000010 ; 42	
Gnd	SCL	1000011 ; 43	
Vcc	Gnd	1000100 ; 44	+5VSB
Vcc	Vcc	1000101 ; 45	
Vcc	SDA	1000110 ; 46	
Vcc	SCL	1000111 ; 47	
SDA	Gnd	1001000 ; 48	
SDA	Vcc	1001001 ; 49	
SDA	SDA	1001010 ; 4A	
SDA	SCL	1001011 ; 4B	
SCL	Gnd	1001100 ; 4C	+5V
SCL	Vcc	1001101 ; 4D	+3V
SCL	SDA	1001110 ; 4E	
SCL	SCL	1001111 ; 4F	

<Variant Name>

ASUSTek COMPUTER INC.

Title : Power monitor-1

Engineer: RAY

Size	Project Name	Rev
A2	SkyLake VC	R1.00

Date: Tuesday, July 24, 2018 Sheet 29 of 139

Remove XMP/EPU/TPU

<Variant Name>

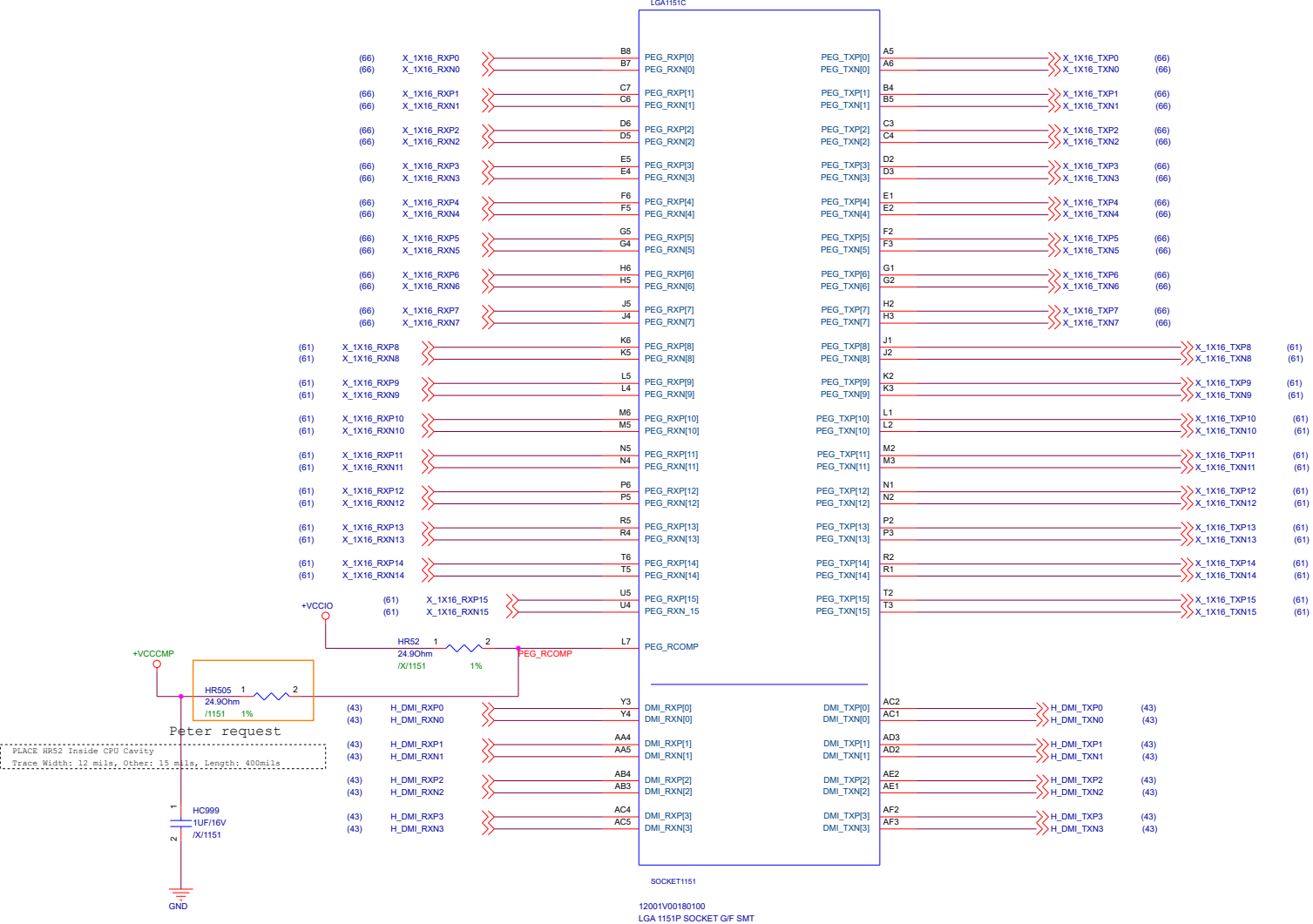
Title : TPU,EPU,TPM,XMP

ASUSTek Computer Inc.

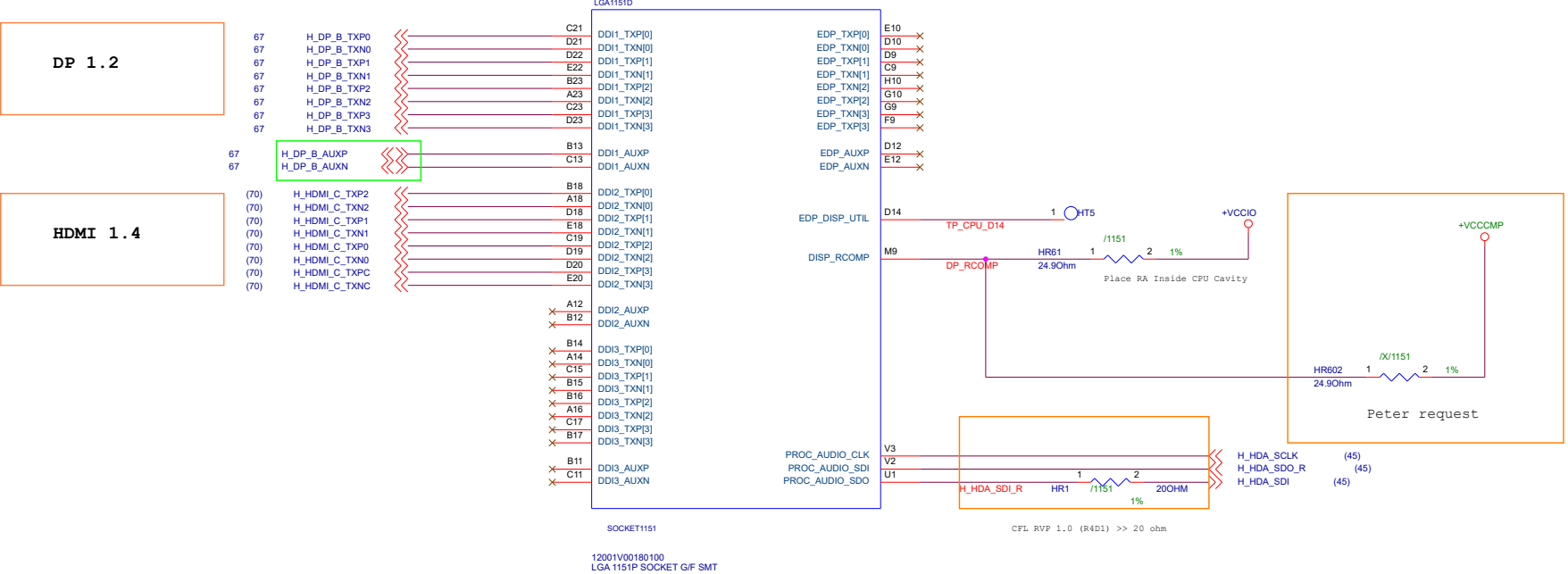
Engineer: Aaron_Su

Size	Project Name	Rev
A2	Z390 Golden board	R1.00

Date: Tuesday, July 24, 2018 Sheet 30 of 139



ASUSTek Computer Inc.	Title : LGA1151 (DMI/PEG)	
	Engineer: Aaron_Su	
Size: A3	Project Name: Z390 Golden board	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 31 of 139	



Title :	LGA1151 (FDI/DISPLAY)
ASUSTek Computer Inc.	Engineer: Aaron_Su
Size: A3	Project Name: Z390 Golden board
Rev: R1.00	
Date: Tuesday, July 24, 2018	Sheet 32 of 139

Channel A
8 Layer routing

(39) D4_DQ_A[0:63]

LGA1151A

AE38		DDR0_DQ[0]
AE37	D4_DQ_A5	DDR0_DQ[1]
AG38	D4_DQ_A1	DDR0_DQ[2]
AG37	D4_DQ_A2	DDR0_DQ[3]
AE39	D4_DQ_A3	DDR0_DQ[4]
AE40	D4_DQ_A4	DDR0_DQ[5]
AG39	D4_DQ_A0	DDR0_DQ[6]
AG40	D4_DQ_A6	DDR0_DQ[7]
AJ38	D4_DQ_A7	DDR0_DQ[8]
AJ37	D4_DQ_A13	DDR0_DQ[9]
AL38	D4_DQ_A9	DDR0_DQ[10]
AL37	D4_DQ_A10	DDR0_DQ[11]
AJ40	D4_DQ_A11	DDR0_DQ[12]
AJ39	D4_DQ_A8	DDR0_DQ[13]
AL39	D4_DQ_A12	DDR0_DQ[14]
AL40	D4_DQ_A14	DDR0_DQ[15]
AN38	D4_DQ_A15	DDR0_DQ[16]/DDR0_DQ[32]
AN40	D4_DQ_A21	DDR0_DQ[17]/DDR0_DQ[33]
AR38	D4_DQ_A16	DDR0_DQ[18]/DDR0_DQ[34]
AR37	D4_DQ_A18	DDR0_DQ[19]/DDR0_DQ[35]
AN39	D4_DQ_A19	DDR0_DQ[20]/DDR0_DQ[36]
AN37	D4_DQ_A20	DDR0_DQ[21]/DDR0_DQ[37]
AR39	D4_DQ_A17	DDR0_DQ[22]/DDR0_DQ[38]
AR40	D4_DQ_A22	DDR0_DQ[23]/DDR0_DQ[39]
AW37	D4_DQ_A23	DDR0_DQ[24]/DDR0_DQ[40]
AU38	D4_DQ_A25	DDR0_DQ[25]/DDR0_DQ[41]
AV35	D4_DQ_A28	DDR0_DQ[26]/DDR0_DQ[42]
AW35	D4_DQ_A27	DDR0_DQ[27]/DDR0_DQ[43]
AU37	D4_DQ_A31	DDR0_DQ[28]/DDR0_DQ[44]
AV37	D4_DQ_A29	DDR0_DQ[29]/DDR0_DQ[45]
AT35	D4_DQ_A24	DDR0_DQ[30]/DDR0_DQ[46]
AU35	D4_DQ_A30	DDR0_DQ[31]/DDR0_DQ[47]
AY8	D4_DQ_A26	DDR0_DQ[32]/DDR1_DQ[0]
AW8	D4_DQ_A32	DDR0_DQ[33]/DDR1_DQ[1]
AV6	D4_DQ_A36	DDR0_DQ[34]/DDR1_DQ[2]
AU6	D4_DQ_A34	DDR0_DQ[35]/DDR1_DQ[3]
AU8	D4_DQ_A35	DDR0_DQ[36]/DDR1_DQ[4]
AV8	D4_DQ_A33	DDR0_DQ[37]/DDR1_DQ[5]
AW6	D4_DQ_A37	DDR0_DQ[38]/DDR1_DQ[6]
AY6	D4_DQ_A39	DDR0_DQ[39]/DDR1_DQ[7]
AY4	D4_DQ_A38	DDR0_DQ[40]/DDR1_DQ[8]
AV4	D4_DQ_A44	DDR0_DQ[41]/DDR1_DQ[9]
AT1	D4_DQ_A40	DDR0_DQ[42]/DDR1_DQ[10]
AT2	D4_DQ_A47	DDR0_DQ[43]/DDR1_DQ[11]
AV3	D4_DQ_A43	DDR0_DQ[44]/DDR1_DQ[12]
AW4	D4_DQ_A41	DDR0_DQ[45]/DDR1_DQ[13]
AT4	D4_DQ_A45	DDR0_DQ[46]/DDR1_DQ[14]
AT3	D4_DQ_A46	DDR0_DQ[47]/DDR1_DQ[15]
AP2	D4_DQ_A42	DDR0_DQ[48]/DDR1_DQ[32]
AM4	D4_DQ_A49	DDR0_DQ[49]/DDR1_DQ[33]
AP3	D4_DQ_A54	DDR0_DQ[50]/DDR1_DQ[34]
AM3	D4_DQ_A53	DDR0_DQ[51]/DDR1_DQ[35]
AP4	D4_DQ_A50	DDR0_DQ[52]/DDR1_DQ[36]
AM2	D4_DQ_A52	DDR0_DQ[53]/DDR1_DQ[37]
AP1	D4_DQ_A51	DDR0_DQ[54]/DDR1_DQ[38]
AM1	D4_DQ_A48	DDR0_DQ[55]/DDR1_DQ[39]
AK3	D4_DQ_A55	DDR0_DQ[56]/DDR1_DQ[40]
AH1	D4_DQ_A61	DDR0_DQ[57]/DDR1_DQ[41]
AK4	D4_DQ_A63	DDR0_DQ[58]/DDR1_DQ[42]
AH2	D4_DQ_A60	DDR0_DQ[59]/DDR1_DQ[43]
AH4	D4_DQ_A59	DDR0_DQ[60]/DDR1_DQ[44]
AK2	D4_DQ_A62	DDR0_DQ[61]/DDR1_DQ[45]
AH3	D4_DQ_A57	DDR0_DQ[62]/DDR1_DQ[46]
AK1	D4_DQ_A58	DDR0_DQ[63]/DDR1_DQ[47]
	D4_DQ_A56	

(39) D4_MCB_A[0:7]

AU33		DDR0_ECC[0]
AT33	D4_MCB_A5	DDR0_ECC[1]
AW33	D4_MCB_A4	DDR0_ECC[2]
AV31	D4_MCB_A0	DDR0_ECC[3]
AU31	D4_MCB_A3	DDR0_ECC[4]
AV33	D4_MCB_A2	DDR0_ECC[5]
AW31	D4_MCB_A1	DDR0_ECC[6]
AY31	D4_MCB_A6	DDR0_ECC[7]
	D4_MCB_A7	

DDR0_CKP[0]	AW18	D4_MA_CLK0	(39)
DDR0_CKN[0]	AV18	D4_MA_CLK#0	(39)
DDR0_CKP[1]	AW17	D4_MA_CLK1	(39)
DDR0_CKN[1]	AY17	D4_MA_CLK#1	(39)
DDR0_CKP[2]	AW16	D4_MA_CLK2	(39)
DDR0_CKN[2]	AV16	D4_MA_CLK#2	(39)
DDR0_CKP[3]	AT16	D4_MA_CLK3	(39)
DDR0_CKN[3]	AU16	D4_MA_CLK#3	(39)
DDR0_CKE[0]	AY24	D4_CKE_A0	(39)
DDR0_CKE[1]	AW24	D4_CKE_A1	(39)
DDR0_CKE[2]	AV24	D4_CKE_A2	(39)
DDR0_CKE[3]	AV25	D4_CKE_A3	(39)
DDR0_CS#[0]	AW12	D4_CS_A#0	(39)
DDR0_CS#[1]	AU11	D4_CS_A#1	(39)
DDR0_CS#[2]	AV13	D4_CS_A#2	(39)
DDR0_CS#[3]	AV10	D4_CS_A#3	(39)
DDR0_ODT[0]	AW11	D4_ODT_A0	(39)
DDR0_ODT[1]	AU14	D4_ODT_A1	(39)
DDR0_ODT[2]	AU12	D4_ODT_A2	(39)
DDR0_ODT[3]	AY10	D4_ODT_A3	(39)
DDR0_BA[0]	AY13	D4_BAA0	(39)
DDR0_BA[1]	AV15	D4_BAA1	(39)
DDR0_BG[0]	AW23	D4_BGA0	(39)

D4_MAA[0:16] (39)

DDR0_MA[16]	AW13	
DDR0_MA[14]	AV14	D4_MAA16
DDR0_MA[15]	AY11	D4_MAA14
		D4_MAA15
DDR0_MA[0]	AW15	
DDR0_MA[1]	AU18	D4_MAA0
DDR0_MA[2]	AU17	D4_MAA1
DDR0_MA[3]	AV19	D4_MAA2
DDR0_MA[4]	AT19	D4_MAA3
DDR0_MA[5]	AU20	D4_MAA4
DDR0_MA[6]	AV20	D4_MAA5
DDR0_MA[7]	AU21	D4_MAA6
DDR0_MA[8]	AT20	D4_MAA7
DDR0_MA[9]	AT22	D4_MAA8
DDR0_MA[10]	AY14	D4_MAA9
DDR0_MA[11]	AU22	D4_MAA10
DDR0_MA[12]	AV22	D4_MAA11
DDR0_MA[13]	AV12	D4_MAA12
DDR0_BG[1]	AV23	D4_MAA13
DDR0_ACT#	AU24	D4_BGA1 (39) / D4_A_ACT# (39)
DDR0_PAR	AY15	D4_A_PAR (39)
DDR0_ALERT#	AT23	D4_A_ALERT# (39)

DDR0_DQSN[0]	AF39		
DDR0_DQSN[1]	AK39	D4_DQS_A#0	D4_DQS_A#0 (39)
DDR0_DQSN[2]/DDR0_DQSN[4]	AP39	D4_DQS_A#1	D4_DQS_A#1 (39)
DDR0_DQSN[3]/DDR0_DQSN[5]	AU36	D4_DQS_A#2	D4_DQS_A#2 (39)
DDR0_DQSN[4]/DDR1_DQSN[0]	AW7	D4_DQS_A#3	D4_DQS_A#3 (39)
DDR0_DQSN[5]/DDR1_DQSN[1]	AU3	D4_DQS_A#4	D4_DQS_A#4 (39)
DDR0_DQSN[6]/DDR1_DQSN[4]	AN3	D4_DQS_A#5	D4_DQS_A#5 (39)
DDR0_DQSN[7]/DDR1_DQSN[5]	AJ3	D4_DQS_A#6	D4_DQS_A#6 (39)
		D4_DQS_A#7	D4_DQS_A#7 (39)
DDR0_DQSP[0]	AF38		
DDR0_DQSP[1]	AK38	D4_DQS_A0	D4_DQS_A0 (39)
DDR0_DQSP[2]/DDR0_DQSP[4]	AP38	D4_DQS_A1	D4_DQS_A1 (39)
DDR0_DQSP[3]/DDR0_DQSP[5]	AV36	D4_DQS_A2	D4_DQS_A2 (39)
DDR0_DQSP[4]/DDR1_DQSP[0]	AV7	D4_DQS_A3	D4_DQS_A3 (39)
DDR0_DQSP[5]/DDR1_DQSP[1]	AU2	D4_DQS_A4	D4_DQS_A4 (39)
DDR0_DQSP[6]/DDR1_DQSP[4]	AN2	D4_DQS_A5	D4_DQS_A5 (39)
DDR0_DQSP[7]/DDR1_DQSP[5]	AJ2	D4_DQS_A6	D4_DQS_A6 (39)
		D4_DQS_A7	D4_DQS_A7 (39)
DDR0_DQSP[8]	AV32		
DDR0_DQSN[8]	AU32	D4_DQS_A8	D4_DQS_A8 (39)
		D4_DQS_A#8	D4_DQS_A#8 (39)

SOCKET1151

12001V00180100
LGA 1151P SOCKET G/F SMT

ASUSTek Computer Inc.	Title : LGA1151 (DDR4_A Control)	
	Engineer: Aaron_Su	
Size: A3	Project Name: Z390 Golden board	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 33 of 139	

Follow CRB

Channel B
8 Layer routing

(40) D4_DQ_B[0:63]

LGA1151B

AD34	D4_DQ_B4	DDR1_DQ[0]/DDR0_DQ[16]
AD35	D4_DQ_B5	DDR1_DQ[1]/DDR0_DQ[17]
AG35	D4_DQ_B7	DDR1_DQ[2]/DDR0_DQ[18]
AH35	D4_DQ_B3	DDR1_DQ[3]/DDR0_DQ[19]
AE35	D4_DQ_B1	DDR1_DQ[4]/DDR0_DQ[20]
AE34	D4_DQ_B0	DDR1_DQ[5]/DDR0_DQ[21]
AG34	D4_DQ_B6	DDR1_DQ[6]/DDR0_DQ[22]
AH34	D4_DQ_B2	DDR1_DQ[7]/DDR0_DQ[23]
AK35	D4_DQ_B13	DDR1_DQ[8]/DDR0_DQ[24]
AL35	D4_DQ_B9	DDR1_DQ[9]/DDR0_DQ[25]
AK32	D4_DQ_B14	DDR1_DQ[10]/DDR0_DQ[26]
AL32	D4_DQ_B15	DDR1_DQ[11]/DDR0_DQ[27]
AK34	D4_DQ_B12	DDR1_DQ[12]/DDR0_DQ[28]
AL34	D4_DQ_B8	DDR1_DQ[13]/DDR0_DQ[29]
AK31	D4_DQ_B10	DDR1_DQ[14]/DDR0_DQ[30]
AL31	D4_DQ_B11	DDR1_DQ[15]/DDR0_DQ[31]
AP35	D4_DQ_B16	DDR1_DQ[16]/DDR0_DQ[48]
AN35	D4_DQ_B20	DDR1_DQ[17]/DDR0_DQ[49]
AN32	D4_DQ_B22	DDR1_DQ[18]/DDR0_DQ[50]
AP32	D4_DQ_B23	DDR1_DQ[19]/DDR0_DQ[51]
AN34	D4_DQ_B17	DDR1_DQ[20]/DDR0_DQ[52]
AP34	D4_DQ_B21	DDR1_DQ[21]/DDR0_DQ[53]
AN31	D4_DQ_B18	DDR1_DQ[22]/DDR0_DQ[54]
AP31	D4_DQ_B19	DDR1_DQ[23]/DDR0_DQ[55]
AL29	D4_DQ_B28	DDR1_DQ[24]/DDR0_DQ[56]
AM29	D4_DQ_B24	DDR1_DQ[25]/DDR0_DQ[57]
AP29	D4_DQ_B30	DDR1_DQ[26]/DDR0_DQ[58]
AR29	D4_DQ_B26	DDR1_DQ[27]/DDR0_DQ[59]
AM28	D4_DQ_B25	DDR1_DQ[28]/DDR0_DQ[60]
AL28	D4_DQ_B29	DDR1_DQ[29]/DDR0_DQ[61]
AR28	D4_DQ_B27	DDR1_DQ[30]/DDR0_DQ[62]
AP28	D4_DQ_B31	DDR1_DQ[31]/DDR0_DQ[63]
AR12	D4_DQ_B32	DDR1_DQ[32]/DDR1_DQ[16]
AP12	D4_DQ_B33	DDR1_DQ[33]/DDR1_DQ[17]
AM13	D4_DQ_B38	DDR1_DQ[34]/DDR1_DQ[18]
AL13	D4_DQ_B34	DDR1_DQ[35]/DDR1_DQ[19]
AR13	D4_DQ_B36	DDR1_DQ[36]/DDR1_DQ[20]
AP13	D4_DQ_B37	DDR1_DQ[37]/DDR1_DQ[21]
AM12	D4_DQ_B39	DDR1_DQ[38]/DDR1_DQ[22]
AL12	D4_DQ_B35	DDR1_DQ[39]/DDR1_DQ[23]
AP10	D4_DQ_B44	DDR1_DQ[40]/DDR1_DQ[24]
AR10	D4_DQ_B45	DDR1_DQ[41]/DDR1_DQ[25]
AR7	D4_DQ_B46	DDR1_DQ[42]/DDR1_DQ[26]
AP7	D4_DQ_B42	DDR1_DQ[43]/DDR1_DQ[27]
AR9	D4_DQ_B41	DDR1_DQ[44]/DDR1_DQ[28]
AP9	D4_DQ_B40	DDR1_DQ[45]/DDR1_DQ[29]
AR6	D4_DQ_B47	DDR1_DQ[46]/DDR1_DQ[30]
AP6	D4_DQ_B43	DDR1_DQ[47]/DDR1_DQ[31]
AM10	D4_DQ_B52	DDR1_DQ[48]
AL10	D4_DQ_B53	DDR1_DQ[49]
AM7	D4_DQ_B55	DDR1_DQ[50]
AL7	D4_DQ_B51	DDR1_DQ[51]
AM9	D4_DQ_B48	DDR1_DQ[52]
AL9	D4_DQ_B49	DDR1_DQ[53]
AM6	D4_DQ_B54	DDR1_DQ[54]
AL6	D4_DQ_B50	DDR1_DQ[55]
AJ6	D4_DQ_B61	DDR1_DQ[56]
AJ7	D4_DQ_B56	DDR1_DQ[57]
AE6	D4_DQ_B63	DDR1_DQ[58]
AF7	D4_DQ_B58	DDR1_DQ[59]
AH7	D4_DQ_B60	DDR1_DQ[60]
AH6	D4_DQ_B57	DDR1_DQ[61]
AE7	D4_DQ_B59	DDR1_DQ[62]
AF6	D4_DQ_B62	DDR1_DQ[63]

(40) D4_MCB_B[0:7]

AR25	D4_MCB_B2	DDR1_ECC[0]
AR26	D4_MCB_B6	DDR1_ECC[1]
AM26	D4_MCB_B5	DDR1_ECC[2]
AM25	D4_MCB_B1	DDR1_ECC[3]
AP26	D4_MCB_B3	DDR1_ECC[4]
AP25	D4_MCB_B7	DDR1_ECC[5]
AL25	D4_MCB_B0	DDR1_ECC[6]
AL26	D4_MCB_B4	DDR1_ECC[7]

AM20	DDR1_CKP[0]	D4_MB_CLK0 (40)
AM21	DDR1_CKN[0]	D4_MB_CLK#0 (40)
AP22	DDR1_CKP[1]	D4_MB_CLK1 (40)
AP21	DDR1_CKN[1]	D4_MB_CLK#1 (40)
AN20	DDR1_CKP[2]	D4_MB_CLK2 (40)
AN21	DDR1_CKN[2]	D4_MB_CLK#2 (40)
AP19	DDR1_CKP[3]	D4_MB_CLK3 (40)
AP20	DDR1_CKN[3]	D4_MB_CLK#3 (40)
AY29	DDR1_CKE[0]	D4_CKE_B0 (40)
AV29	DDR1_CKE[1]	D4_CKE_B1 (40)
AW29	DDR1_CKE[2]	D4_CKE_B2 (40)
AU29	DDR1_CKE[3]	D4_CKE_B3 (40)
AP17	DDR1_CS#_0	D4_CS_B#0 (40)
AN15	DDR1_CS#_1	D4_CS_B#1 (40)
AN17	DDR1_CS#_2	D4_CS_B#2 (40)
AM15	DDR1_CS#_3	D4_CS_B#3 (40)
AM16	DDR1_ODT[0]	D4_ODT_B0 (40)
AL16	DDR1_ODT[1]	D4_ODT_B1 (40)
AP15	DDR1_ODT[2]	D4_ODT_B2 (40)
AL15	DDR1_ODT[3]	D4_ODT_B3 (40)
AN18	DDR1_MA[16]	D4_MAB16
AL17	DDR1_MA[14]	D4_MAB14
AP16	DDR1_MA[15]	D4_MAB15
AL18	DDR1_BA[0]	D4_BAB0 (40)
AM18	DDR1_BA[1]	D4_BAB1 (40)
AW28	DDR1_BG[0]	D4_BGB0 (40)
AL19	DDR1_MA[0]	D4_MAB0
AL22	DDR1_MA[1]	D4_MAB1
AM22	DDR1_MA[2]	D4_MAB2
AM23	DDR1_MA[3]	D4_MAB3
AP23	DDR1_MA[4]	D4_MAB4
AL23	DDR1_MA[5]	D4_MAB5
AW26	DDR1_MA[6]	D4_MAB6
AY26	DDR1_MA[7]	D4_MAB7
AU26	DDR1_MA[8]	D4_MAB8
AW27	DDR1_MA[9]	D4_MAB9
AP18	DDR1_MA[10]	D4_MAB10
AU27	DDR1_MA[11]	D4_MAB11
AV27	DDR1_MA[12]	D4_MAB12
AR15	DDR1_MA[13]	D4_MAB13
AY28	DDR1_BG[1]	D4_BGB1 (40)
AU28	DDR1_ACT#	D4_B_ACT# (40)
AL20	DDR1_PAR	D4_B_PAR (40)
AY25	DDR1_ALERT#	D4_B_ALERT# (40)

D4_MAB[0:16] (40)

AF34	DDR1_DQSN[0]/DDR0_DQSN[2]	D4_DQS_B#0 (40)
AK33	DDR1_DQSN[1]/DDR0_DQSN[3]	D4_DQS_B#1 (40)
AN33	DDR1_DQSN[2]/DDR0_DQSN[6]	D4_DQS_B#2 (40)
AN29	DDR1_DQSN[3]/DDR0_DQSN[7]	D4_DQS_B#3 (40)
AN13	DDR1_DQSN[4]/DDR1_DQSN[2]	D4_DQS_B#4 (40)
AR8	DDR1_DQSN[5]/DDR1_DQSN[3]	D4_DQS_B#5 (40)
AM8	DDR1_DQSN[6]	D4_DQS_B#6 (40)
AG6	DDR1_DQSN[7]	D4_DQS_B#7 (40)
AF35	DDR1_DQSP[0]/DDR0_DQSP[2]	D4_DQS_B0 (40)
AL33	DDR1_DQSP[1]/DDR0_DQSP[3]	D4_DQS_B1 (40)
AP33	DDR1_DQSP[2]/DDR0_DQSP[6]	D4_DQS_B2 (40)
AN28	DDR1_DQSP[3]/DDR0_DQSP[7]	D4_DQS_B3 (40)
AN12	DDR1_DQSP[4]/DDR1_DQSP[2]	D4_DQS_B4 (40)
AP8	DDR1_DQSP[5]/DDR1_DQSP[3]	D4_DQS_B5 (40)
AL8	DDR1_DQSP[6]	D4_DQS_B6 (40)
AG7	DDR1_DQSP[7]	D4_DQS_B7 (40)
AN25	DDR1_DQSP[8]	D4_DQS_B8 (40)
AN26	DDR1_DQSN[8]	D4_DQS_B#8 (40)

AB40	DDR_VREF_CA	
AC40	DDR0_VREF_DQ	H_D4_VREFCA_A 1 HT10
AC39	DDR1_VREF_DQ	H_D3A_VREFDQ_R
		H_D4_VREFCA_B

SOCKET1151

12001V00180100
LGA 1151P SOCKET G/F SMT

H_D4_VREFCA_A
D3R111 1 2 2Ohm
D4_VREFCA_A (41)
D3C48 0.022UF/16V
D3R23 24.9Ohm
GND
High frequency termination, can absorb any high frequency noise coming from CPU/board crosstalk.

H_D4_VREFCA_B
D3R110 1 2 2Ohm
D4_VREFCA_B (41)
VREF control form CPU
D3C47 0.022UF/16V
D3R22 24.9Ohm
close B channel
GND
High frequency termination, can absorb any high frequency noise coming from CPU/board crosstalk.

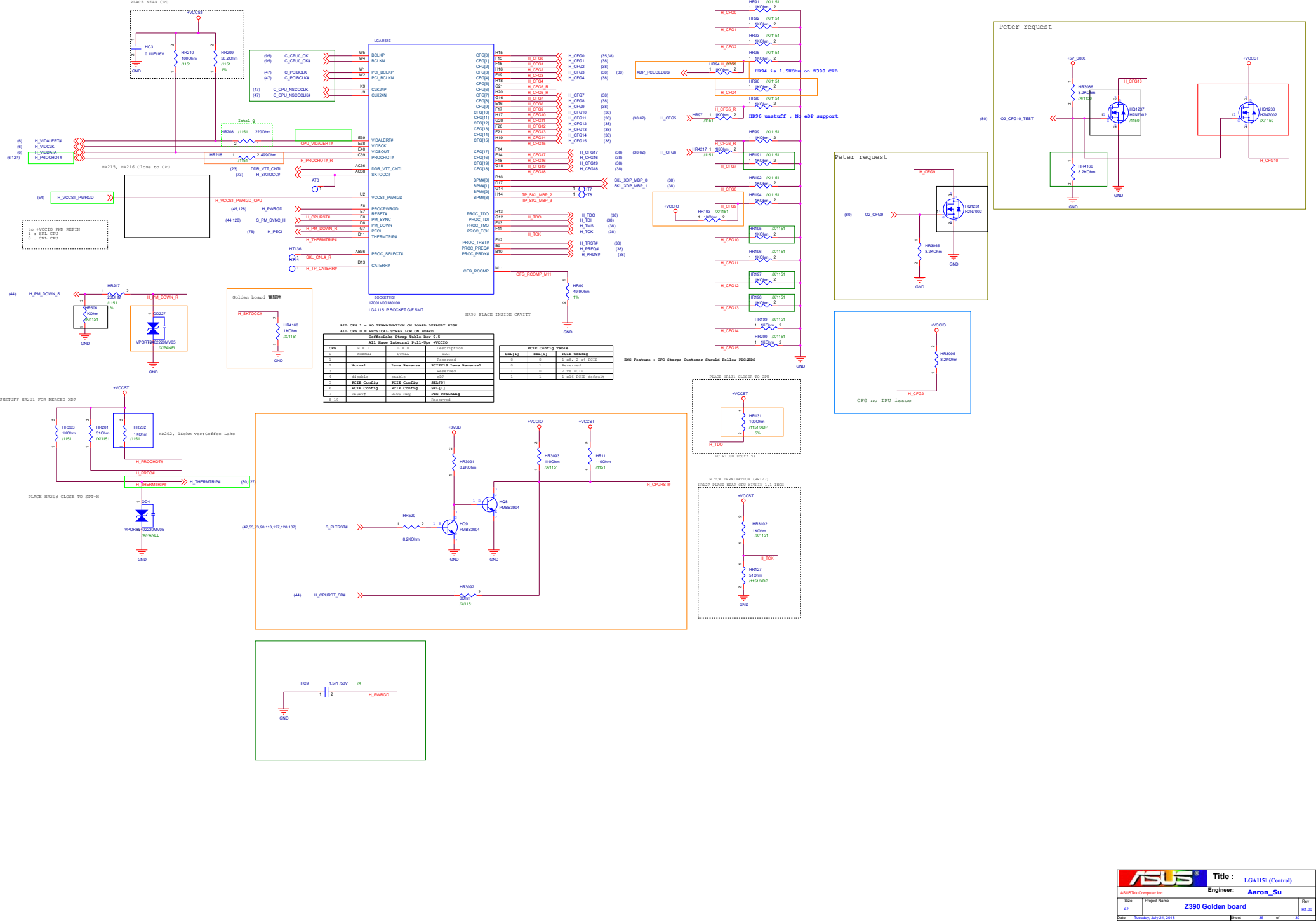
ASUSTek Computer Inc.

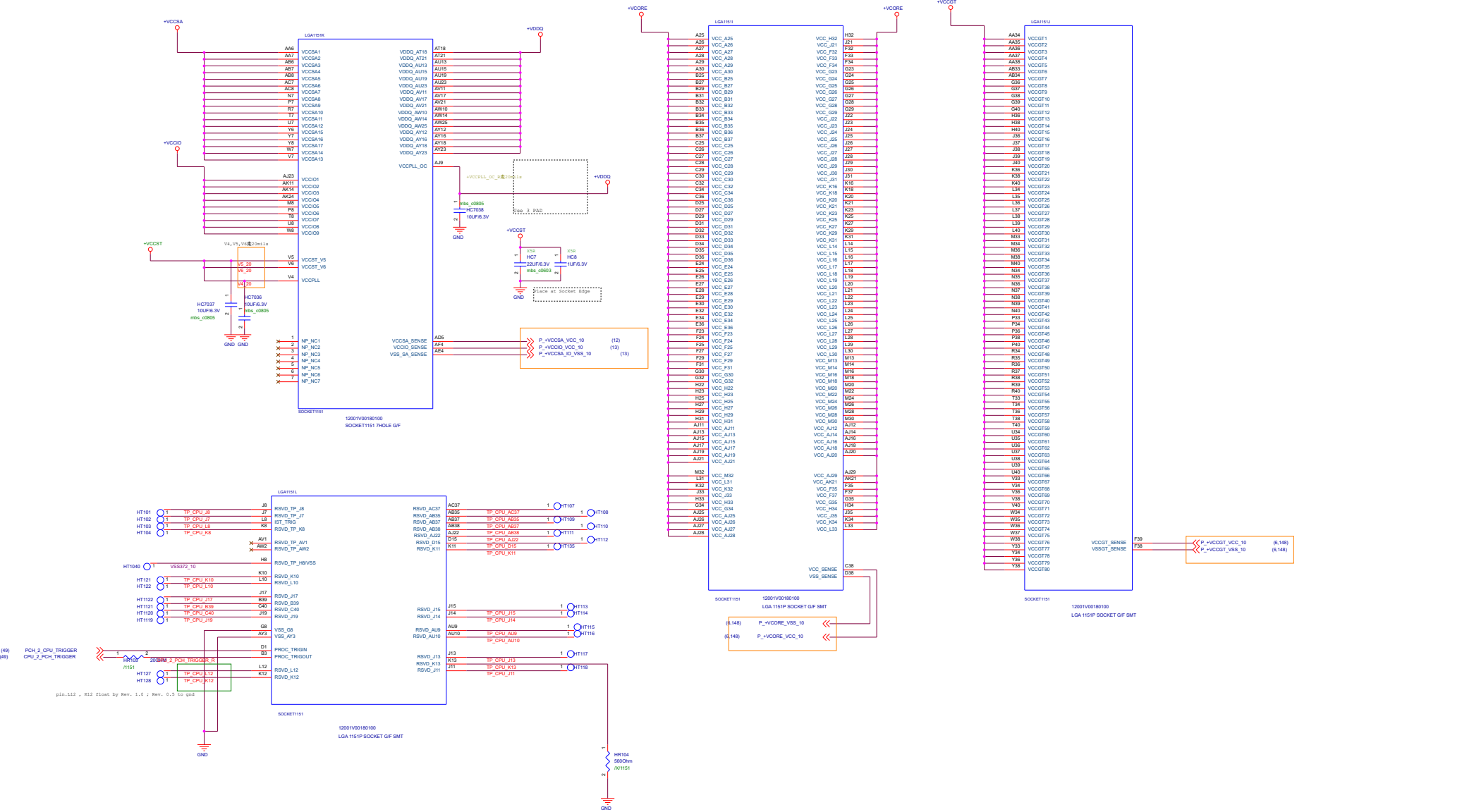
Title : LGA1151 (DDR4_B Control)

Engineer: Aaron_Su

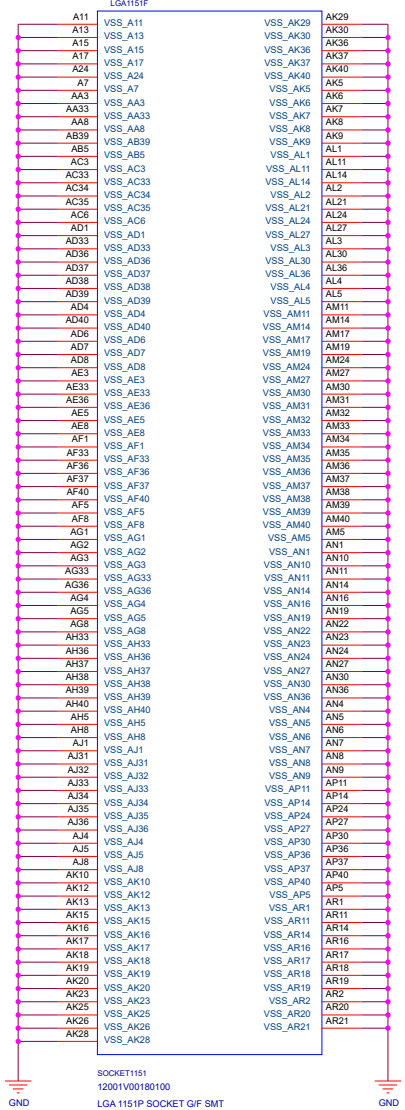
Size	Project Name	Rev
A3	Z390 Golden board	R1.00

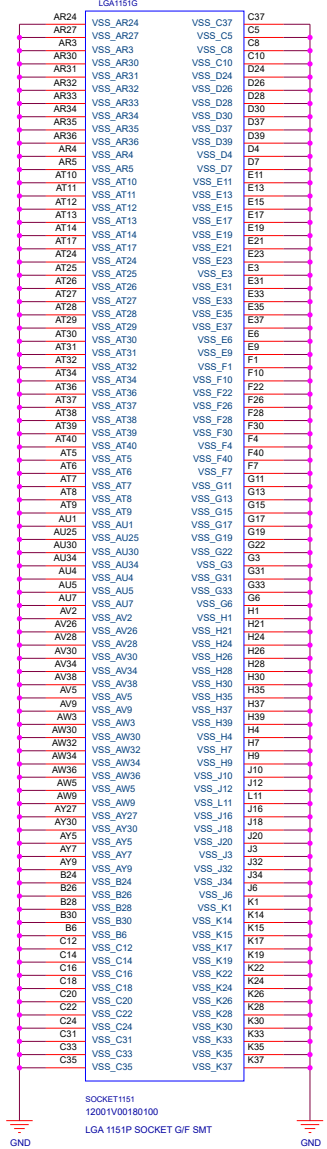
Date: Tuesday, July 24, 2018 Sheet 34 of 139

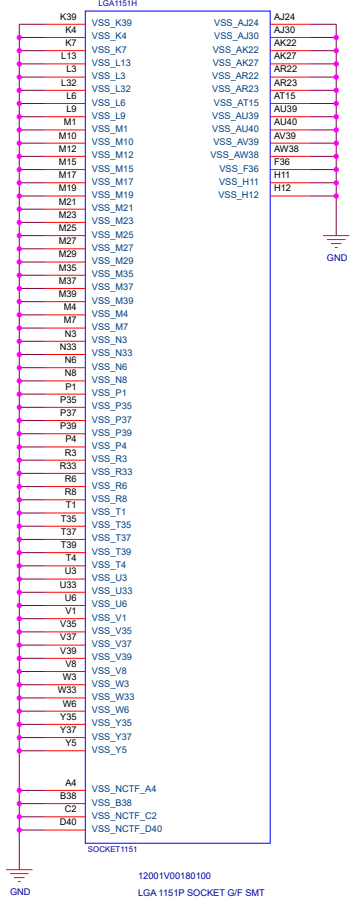

PLACE NEAR CPU
HC3 0.1UF/16V
HR210 100Ohm /1151
HR209 56.2Ohm /1151 1%
GND
LGA1151E
BCLKP
BCLKN
PCI_BCLKP
PCI_BCLKN
CLK24P
CLK24N
C_CPU0_CK
C_CPU0_CK#
C_PCIBCLK
C_PCIBCLK#
C_CPU_NSCCCLK
C_CPU_NSCCCLK#
VIDALERT#
VIDSCK
VIDSOUT
PROCHOT#
DDR_VTT_CNTL
SKTOCC#
VCCST_PWRGD
PROCPWRGD
RESET#
PM_SYNC
PM_DOWN
PECI
THERMTRIP#
PROC_SELECT#
CATERR#
PROC_TDO
PROC_TMS
PROC_TCK
PROC_TRST#
PROC_PREQ#
PROC_PRDY#
CFG_RCOMP
CFG_RCOMP_M11
HR90 49.9Ohm 1%
HR90 PLACE INSIDE CAVITY
SOCKET1151
1200IV0018D100
LGA 1151P SOCKET G/F SMT
HR208 /1151 220Ohm
HR218 /1151 2.49KOhm
HR215, HR216 Close to CPU
H_VIDALERT#
H_VIDCLK
H_MEDATA
H_PROCHOT#
CPU_VIDALERT#
H_PROCHOT#_R
H_SKTOCC#
H_VCCST_PWRGD
H_VCCST_PWRGD_CPU
H_PWRGD
H_CPURST#
S_PM_SYNC_H
H_PM_DOWN_R
H_PECI
H_THERMTRIP#
SKL_CNL#_R
H_TP_CATERR#
to +VCCIO PWR REFIN
1 : SKL CPU
0 : CNL CPU
H_PM_DOWN_S
HR217 200Ohm /1151 1%
HR506 ROhm /X1151
DD227 VPORT0402220MV05 /XPANEL
Golden board 實驗用
H_SKTOCC#
HR4168 1KOhm /X1151
ALL CFG 1 = NO TERMINATION ON BOARD DEFAULT HIGH
ALL CFG 0 = PHYSICAL STRAP LOW ON BOARD
Coffeelake Strap Table Rev 0.5
All Have Internal Pull-Ups +VCCIO
CFG | H = 1 | L = 0 | Description
0 | Normal | STALL | EAR
1 | | | Reserved
2 | Normal | Lane Reverse | PCIEX16 Lane Reversal
3 | | | Reserved
4 | disable | enable | eDP
5 | PCIE Config | PCIE Config | SEL[0]
6 | PCIE Config | PCIE Config | SEL[1]
7 | RESET# | BIOS REQ | PEG Training
8-19 | | | Reserved
PCIE Config Table
SEL[1] | SEL[0] | PCIE Config
0 | 0 | 1 x8, 2 x4 PCIE
0 | 1 | Reserved
1 | 0 | 2 x8 PCIE
1 | 1 | 1 x16 PCIE default
ENG Feature : CPG Starps Customer Should Follow PDG&EDS
HR91 /X1151 H_CFG0
HR92 /X1151 H_CFG1
HR93 /X1151 H_CFG2
HR95 /X1151 H_CFG3
HR96 /X1151 H_CFG4
HR98 /X1151 H_CFG5_R
HR99 /X1151 H_CFG6_R
HR191 /X1151 H_CFG7
HR192 /X1151 H_CFG8
HR194 /X1151 H_CFG9
HR195 /X1151 H_CFG10
HR196 /X1151 H_CFG11
HR197 /X1151 H_CFG12
HR198 /X1151 H_CFG13
HR199 /X1151 H_CFG14
HR200 /X1151 H_CFG15
XDP_PCUDEBUG
HR94 is 1.5KOhm on Z390 CRB
HR96 unstuff , No eDP support
HR4217 /1151
HR193 /X1151
+VCCIO
Peter request
O2_CFG9
O2_CFG10_TEST
HR3086 8.2KOhm /X1151
HR4166 8.2KOhm
HR3065 8.2KOhm
HQ1237 HZN7002 /1150
HQ1238 HZN7002 /X1150
HQ1231 HZN7002
CFG no IPU issue
HR3095 8.2KOhm
H_CFG2
UNSTUFF HR201 FOR MERGED XDP
HR203 1KOhm /1151
HR201 51Ohm /X1151
HR202 1KOhm /1151
HR202, 1Kohm ver:Coffee Lake
H_PROCHOT#
H_PREQ#
H_THERMTRIP#
PLACE HR203 CLOSE TO SPT-H
DD4 VPORT0402220MV05 /XPANEL
PLACE HR131 CLOSER TO CPU
HR131 100Ohm /1151/XDP 5%
VC R1.00 stuff 5%
H_TDO
R_TCK TERMINATION (HR127)
SPLIT PLANE NEAR CPU WITHIN 1 INCH
HR3102 1KOhm /X1151
HR127 51Ohm /1151/XDP
H_TCK
+3VSB
HR3091 8.2KOhm
HR3093 110Ohm /X1151
HR11 110Ohm /1151
H_CPURST#
HR320 8.2KOhm
HQ9 PMBS3904
HQ8 PMBS3904
S_PLTRST#
HR3002 0Ohm /X1151
H_CPURST_SB#
HC9 1.5PF/50V /X
H_PWRGD
Title : LGA1151 (Control)
Engineer: Aaron_Su
ASUSTek Computer Inc.
Size: A2
Project Name: Z390 Golden board
Rev: R1.00
Date: Tuesday, July 24, 2018
Sheet 35 of 130

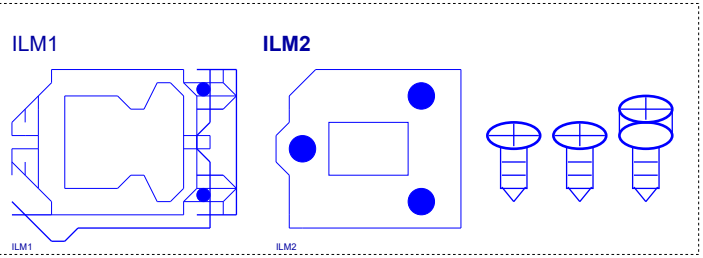


ASUSTek Computer Inc.	Title :	LGA1151 (POWER)	
	Engineer:	Aaron_Su	
Size: A2	Project Name: Z390 Golden board		Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 36 of 139		



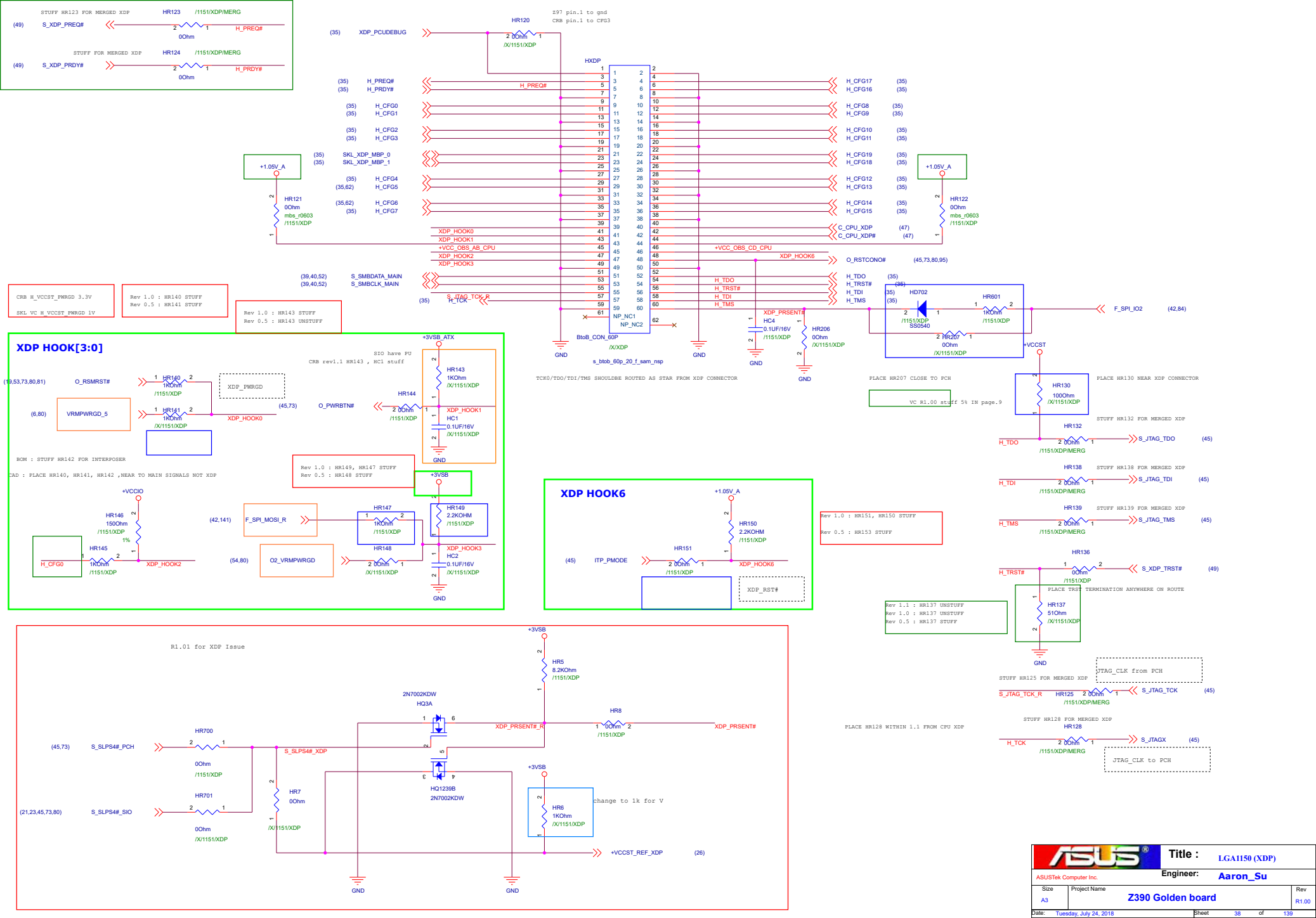




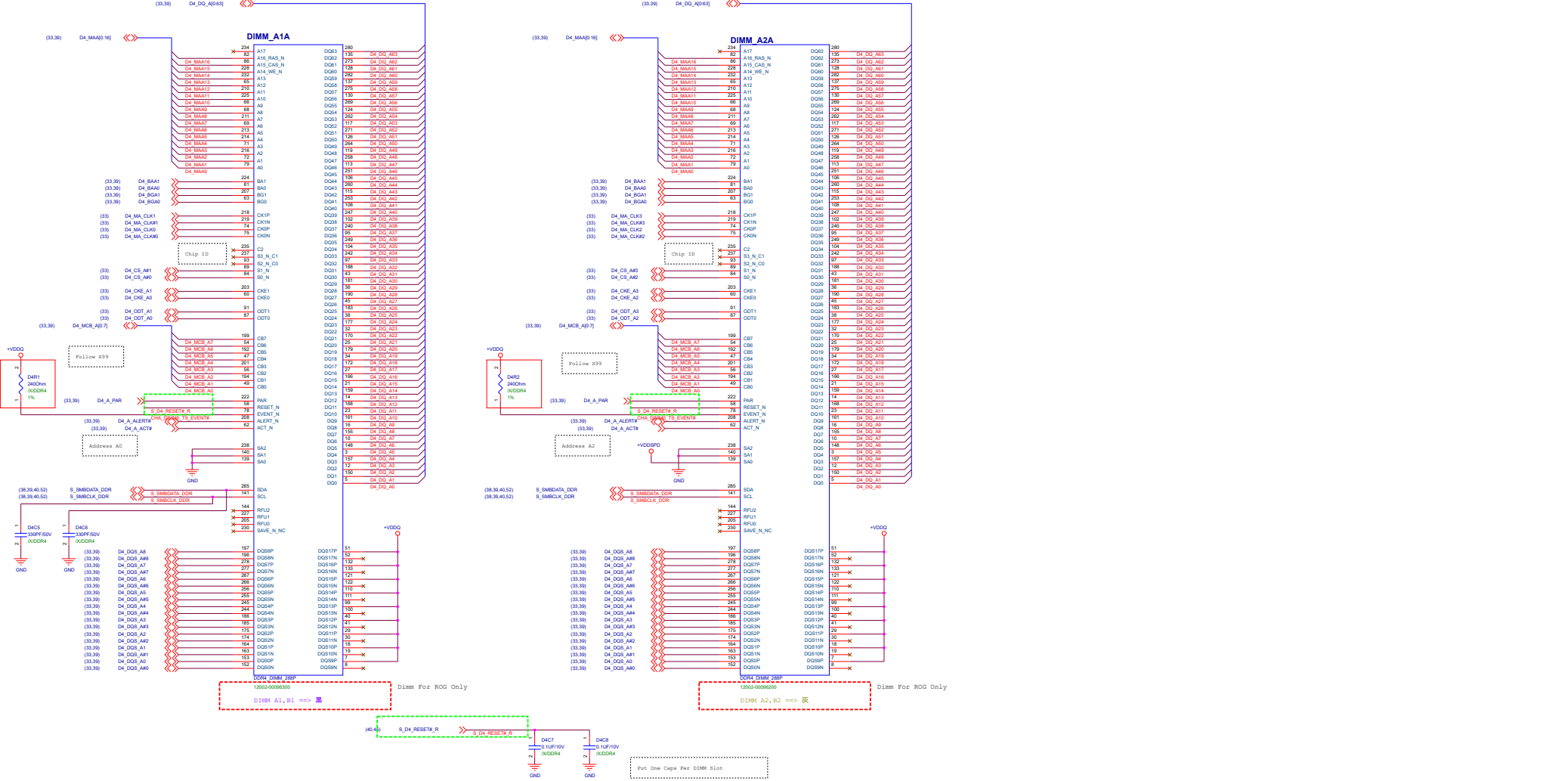


Change BOM (R1.02)
1. ILM + COVER P/N : 13020-00061900
2. BACKPLATE P/N : 13020-00062000 (替代料 13020-00061300)
各別加入 BOM 內, Location 皆為 ILM1 , ILM2

ASUSTek Computer Inc.	Title :	LGA1151 (GND)
	Engineer:	Aaron Su
Size: A3	Project Name: Z390 Golden board	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 37 of 139	



ASUSTek Computer Inc.	Title :	LGA1150 (XDP)	
	Engineer:	Aaron_Su	
Size: A3	Project Name: Z390 Golden board		Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 38 of 139		



<Variant Name>

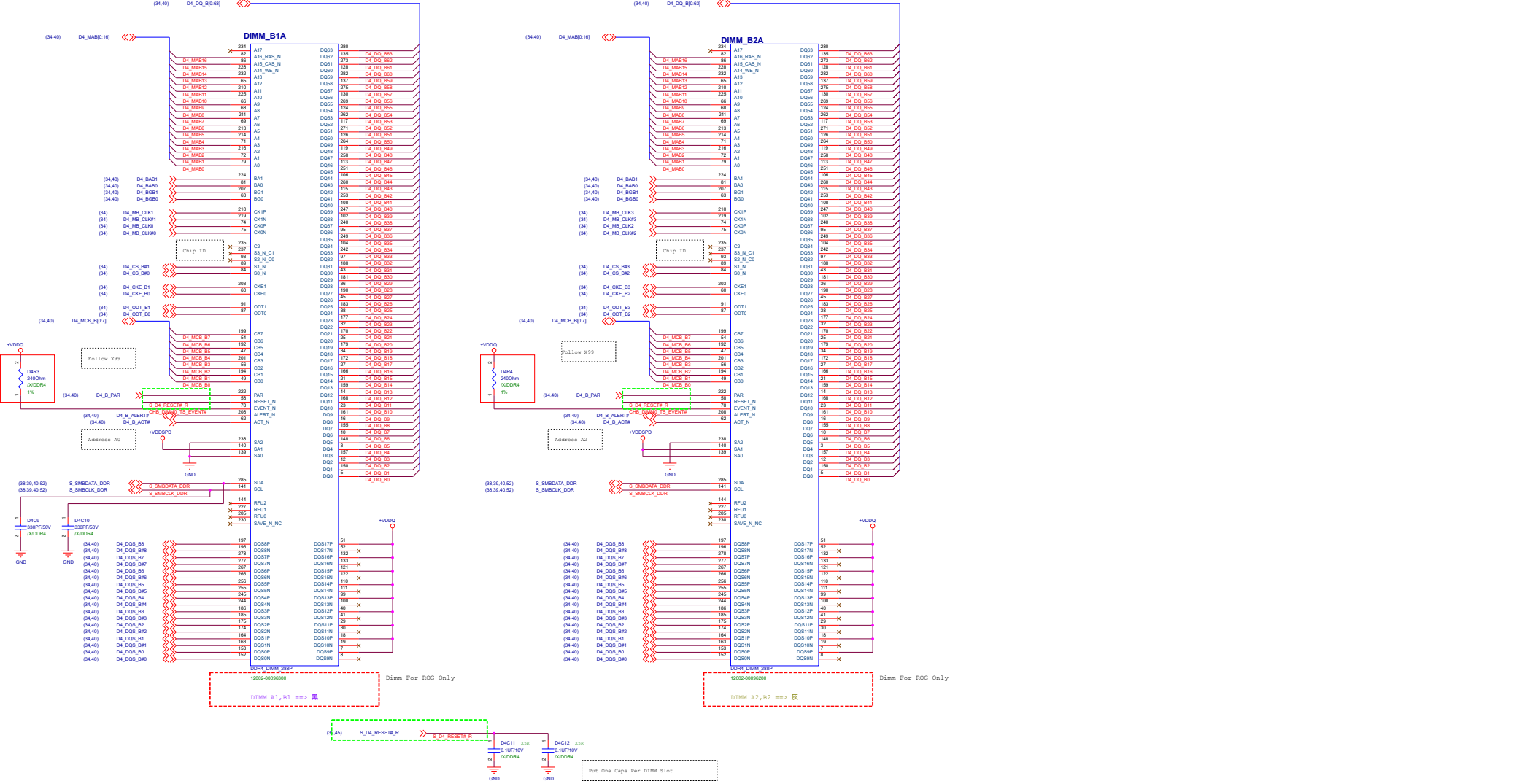
ASUS TeK Computer INC

Title : DDR4 Channel A

Engineer: Aaron_Su

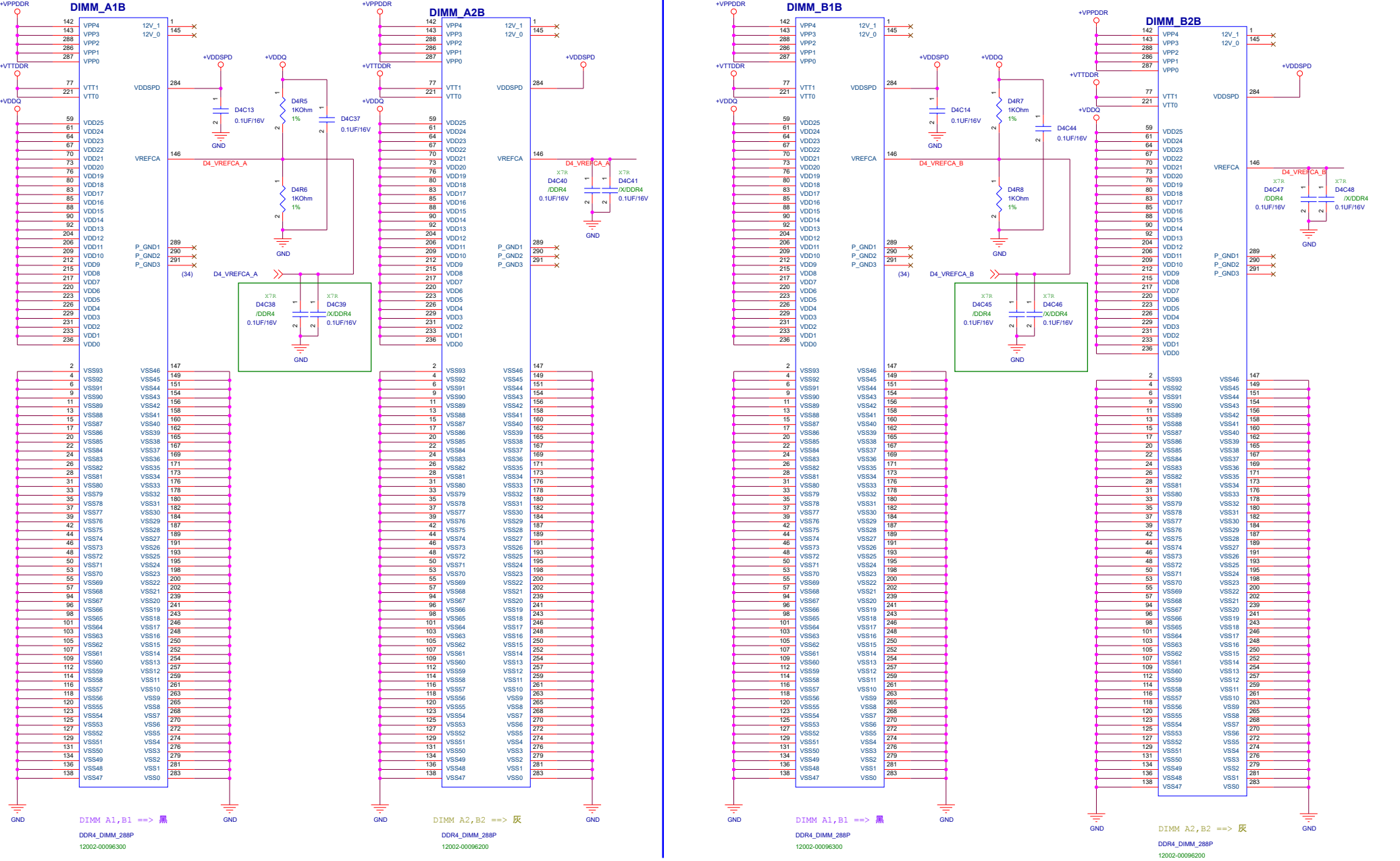
Size	Project Name	Rev
A2	Z390 Golden board	R1.00

Date: Tuesday, July 24, 2018 Sheet 39 of 139



<Variant Name>

ASUS TeK Computer INC	Title :	DDR4 Channel B
	Engineer:	Aaron_Su
Size: A2	Project Name:	Z390 Golden board
Rev: R1.00		
Date: Tuesday, July 24, 2018	Sheet: 40 of 130	



<variant_name>

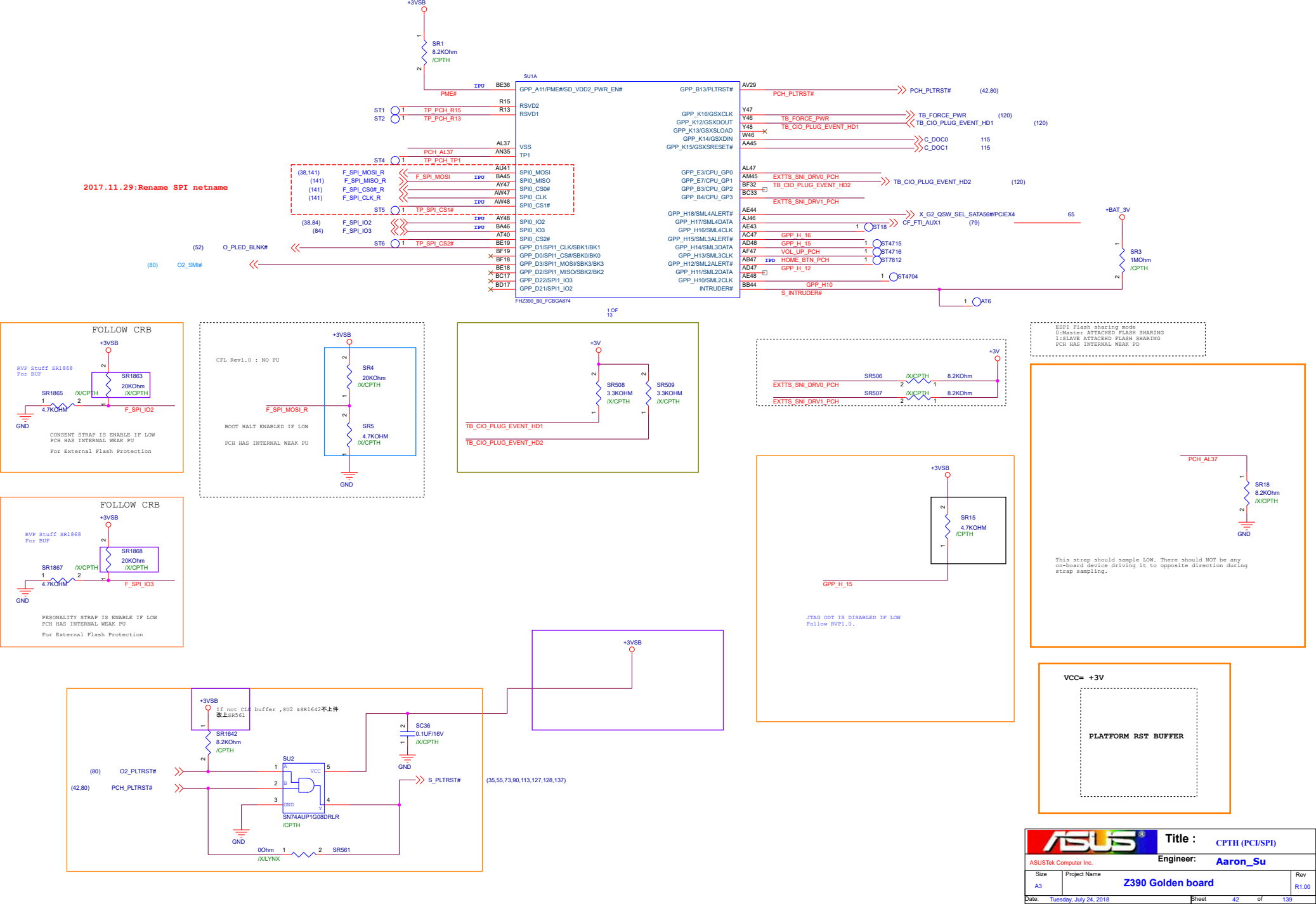
ASUS TeK Computer INC

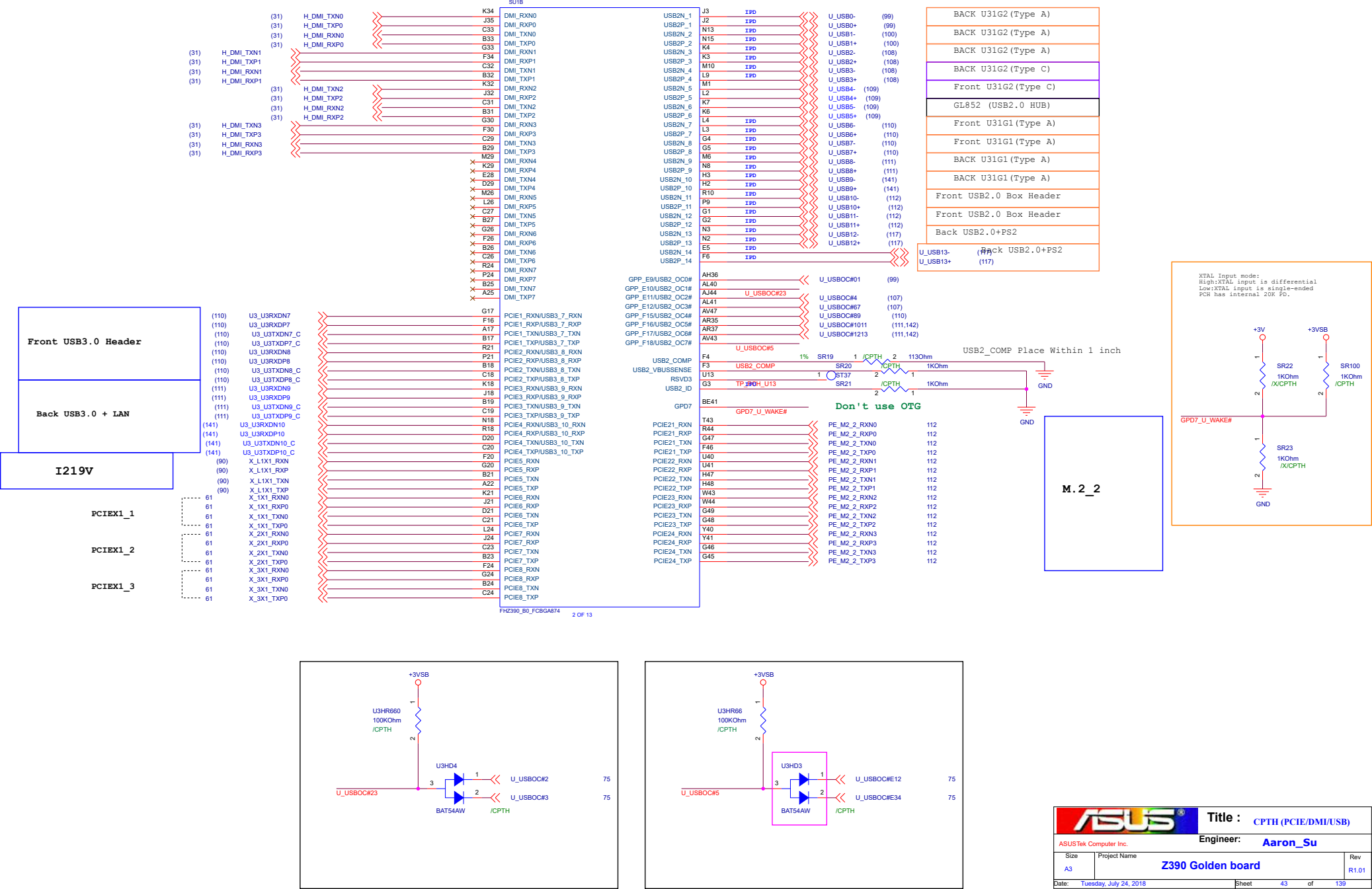
Title : DDR4 (Power)

Engineer: Aaron_Su

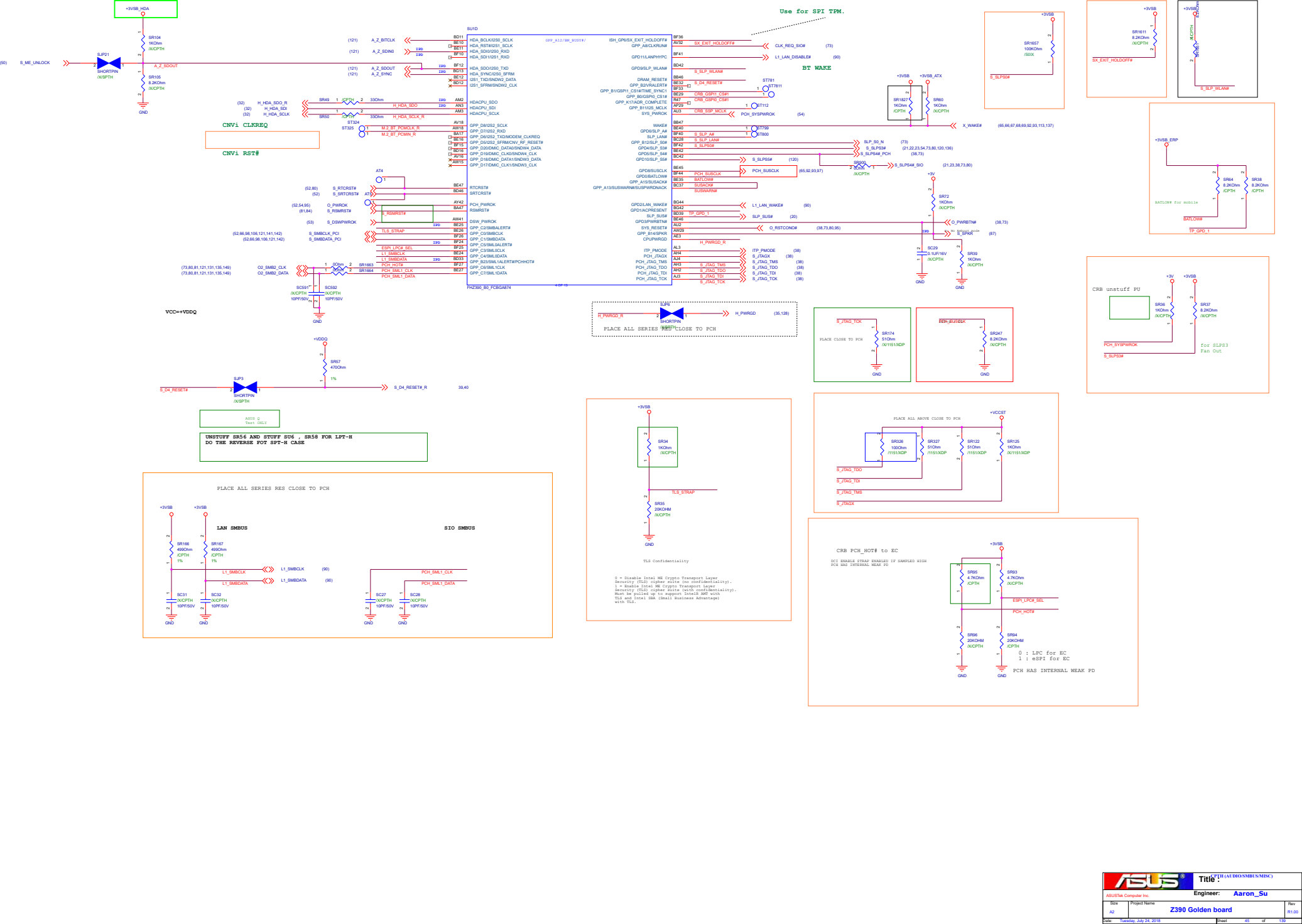
Size	Project Name	Rev
A3	Z390 Golden board	R1.00

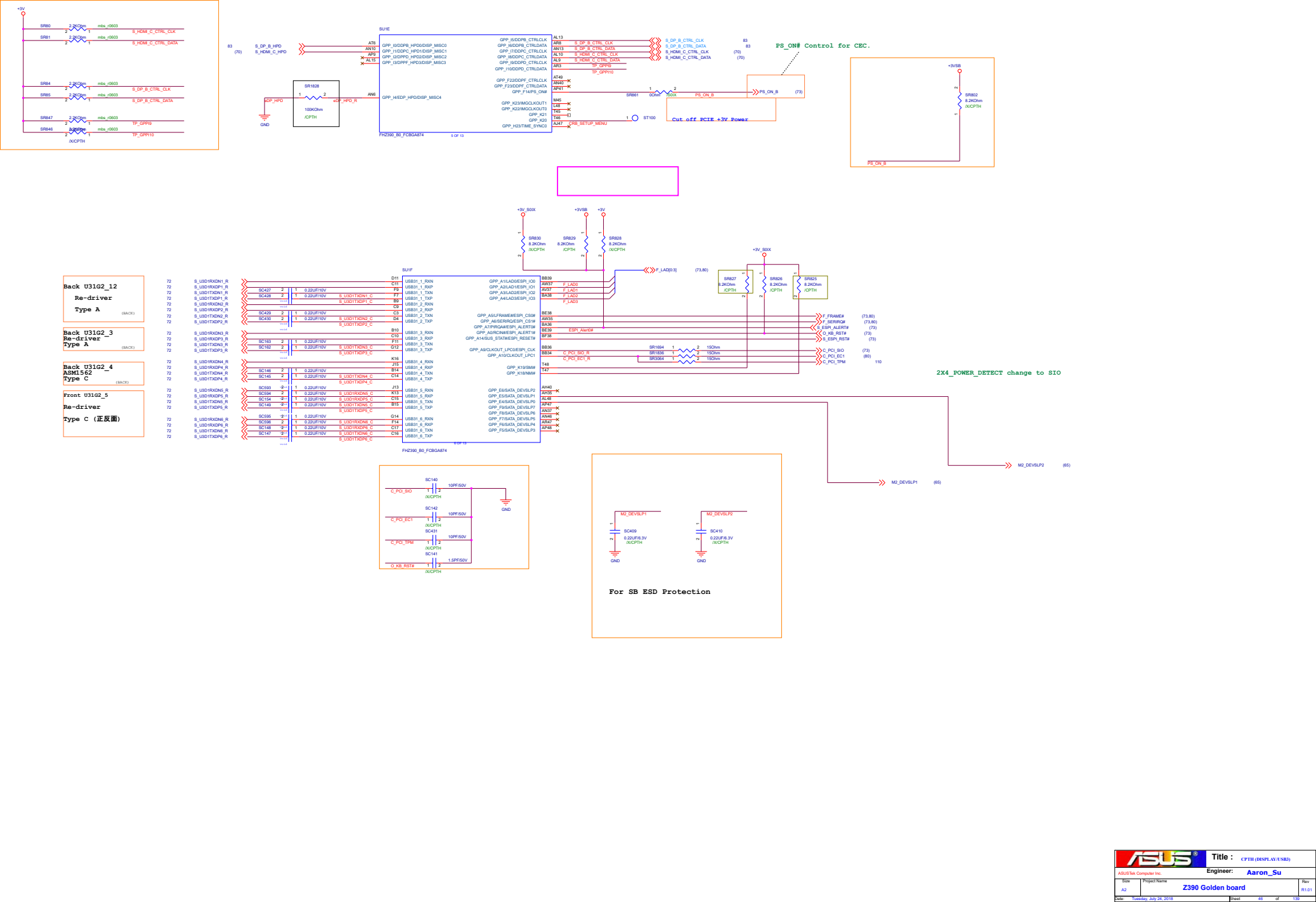
Date: Tuesday, July 24, 2018 Sheet 41 of 139


2017.11.29:Rename SPI netname
SU1A
FHZ390_B0_FCBGA874
1 OF 13
FOLLOW CRB
RVP Stuff SR1868 For BUF
CONSENT STRAP IS ENABLE IF LOW
PCH HAS INTERNAL WEAK PU
For External Flash Protection
CFL Rev1.0 : NO PU
BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU
ESPI Flash sharing mode
0:Master ATTACHED FLASH SHARING
1:SLAVE ATTACEHD FLASH SHARING
PCH HAS INTERNAL WEAK PD
FOLLOW CRB
RVP Stuff SR1868 For BUF
PESONALITY STRAP IS ENABLE IF LOW
PCH HAS INTERNAL WEAK PU
For External Flash Protection
JTAG ODT IS DISABLED IF LOW
Follow RVP1.0.
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
If not CLK buffer ,SU2 &SR1642不上件
改上SR561
SN74AUP1G08DRLR
VCC= +3V
PLATFORM RST BUFFER
Title : CPTH (PCI/SPI)
ASUSTek Computer Inc.
Engineer: Aaron_Su
Size A3
Project Name Z390 Golden board
Rev R1.00
Date: Tuesday, July 24, 2018
Sheet 42 of 139



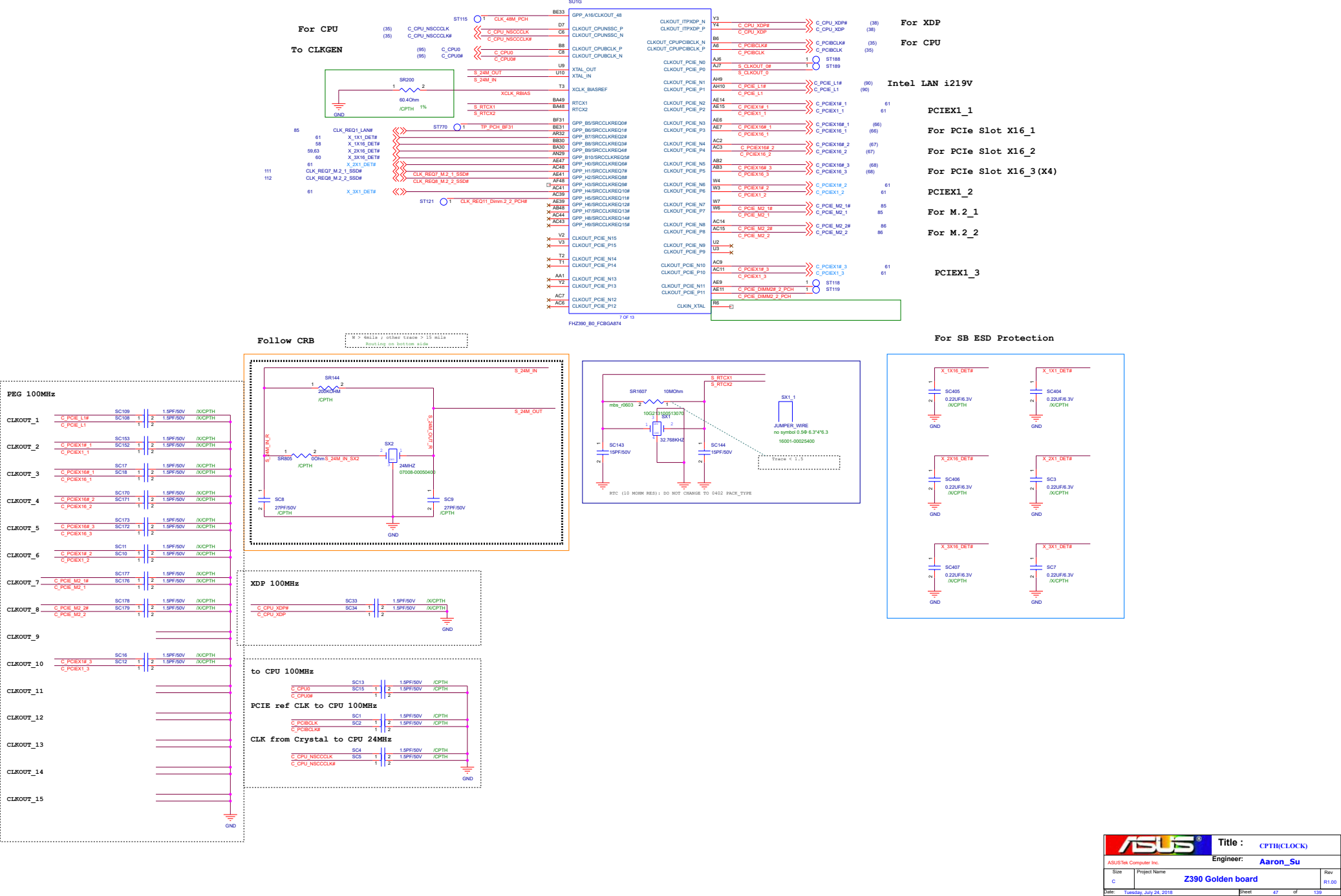
ASUSTek Computer Inc.	Title :	CPTH (PCIE/DMI/USB)	
	Engineer:	Aaron_Su	
Size: A3	Project Name: Z390 Golden board		Rev: R1.01
Date: Tuesday, July 24, 2018	Sheet 43 of 139		


Use for SPI TPM.
BT WAKE
SUID
CNVi CLKREQ
CNVi RST#
VCC=+VDDQ
UNSTUFF SR56 AND STUFF SU6 , SR58 FOR LPT-H
DO THE REVERSE FOT SPT-H CASE
PLACE ALL SERIES RES CLOSE TO PCH
LAN SMBUS
SIO SMBUS
PLACE ALL SERIES RES CLOSE TO PCH
PLACE ALL ABOVE CLOSE TO PCH
CRB unstuff PU
for SLPS3
Fan Out
CRB PCH_HOT# to EC
PCH HAS INTERNAL WEAK PD
0 : LPC for EC
1 : eSPI for EC
TLS Confidentiality
Title : LPTH (AUDIO/SMBUS/MISC)
Engineer: Aaron_Su
ASUSTek Computer Inc.
Z390 Golden board
Rev R1.00
Tuesday, July 24, 2018
Sheet 45 of 130

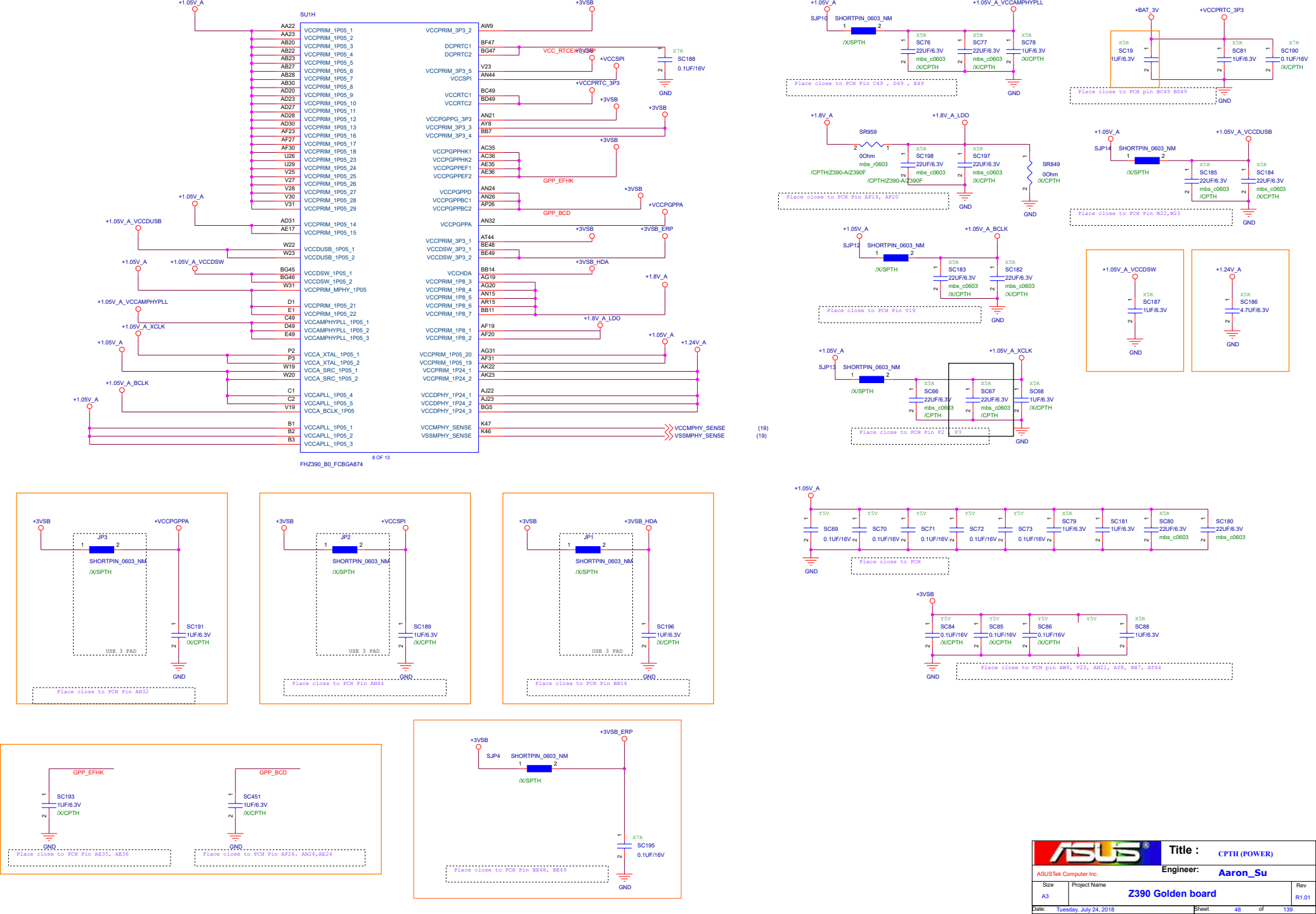


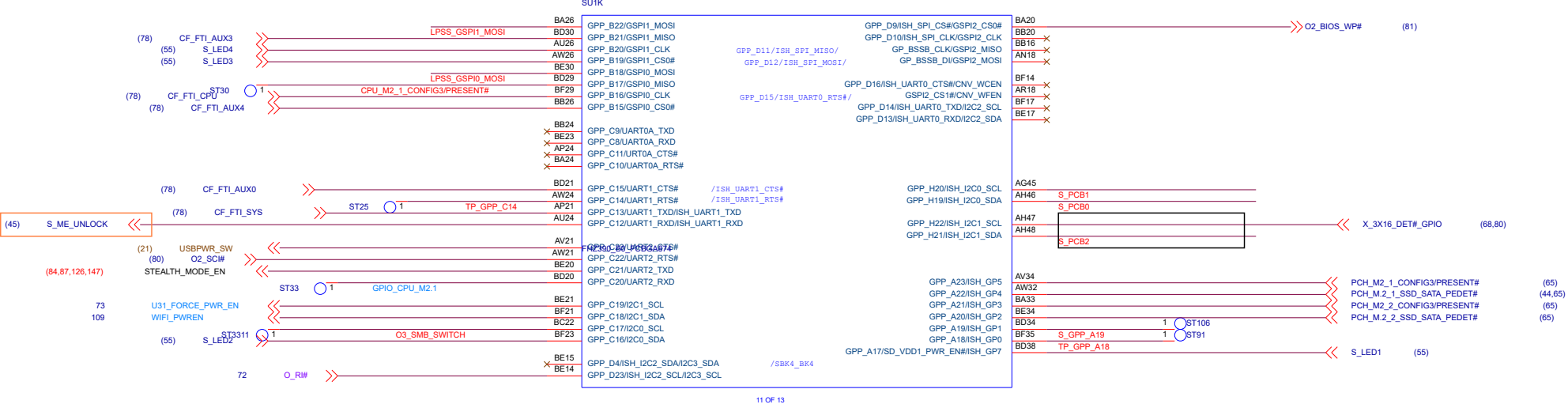
Title :	CPTH (DISPLAY/USB3)
Engineer:	Aaron_Su
Size	A2
Project Name	Z390 Golden board
Rev	R1.01
Date:	Tuesday, July 24, 2018
Sheet	46 of 139

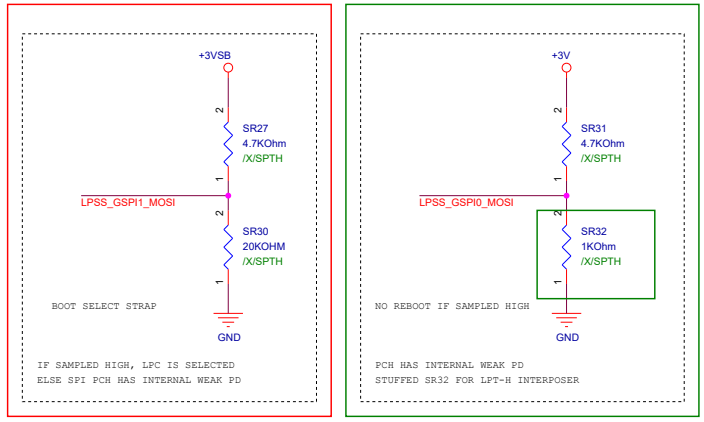
ASUSTek Computer Inc.

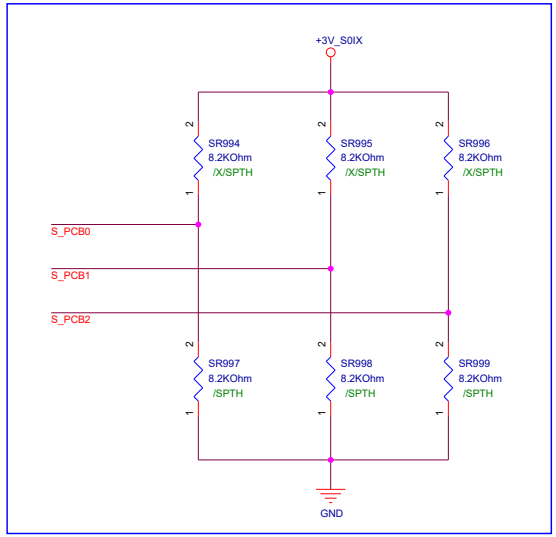


ASUSTek Computer Inc.	Title : CPTH(CLOCK)
	Engineer: Aaron_Su
Size: C	Project Name: Z390 Golden board
	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 47 of 139


SU1H
FHZ390_B0_FCBGA874
8 OF 13
+1.05V_A
+3VSB
+VCCSPI
+VCCPRTC_3P3
+VCCPGPPA
+3VSB_ERP
+3VSB_HDA
+1.8V_A
+1.8V_A_LDO
+1.05V_A_VCCDSUSB
+1.05V_A_VCCDSW
+1.05V_A_VCCAMPHYPLL
+1.05V_A_XCLK
+1.05V_A_BCLK
+1.24V_A
+BAT_3V
+1.05V_A_VCCAMPHYPLL
+1.05V_A_VCCDSUSB
+1.05V_A_VCCDSW
+1.05V_A_BCLK
+1.05V_A_XCLK
SHORTPIN_0603_NM
/X/SPTH
/X/CPTH
GND
Place close to PCH Pin C49 , D49 , E49
Place close to PCH pin BC49 BD49
Place close to PCH Pin AF19, AF20
Place close to PCH Pin W22,W23
Place close to PCH Pin V19
Place close to PCH Pin P2 P3
Place close to PCH Pin AN32
Place close to PCH Pin AN44
Place close to PCH Pin BB14
Place close to PCH
Place close to PCH pin AN9, V23, AN21, AY8, BB7, AT44
Place close to PCH Pin AE35, AE36
Place close to PCH Pin AP26, AN26,AE24
Place close to PCH Pin BE48, BE49
GPP_EFHK
GPP_BCD
VCC_RTCEXTVSS
VCCMPHY_SENSE
VSSMPHY_SENSE
(19)
(19)
Title :
CPTH (POWER)
Engineer:
Aaron_Su
ASUSTek Computer Inc.
Size
A3
Project Name
Z390 Golden board
Rev
R1.01
Date:
Tuesday, July 24, 2018
Sheet
48
of
139





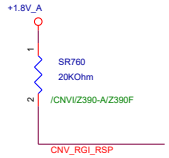


ASUSTek Computer Inc.	Title : CPTH (GPIO)		
	Engineer: Aaron_Su		
Size: A3	Project Name: Z390 Golden board		Rev: R1.01
Date: Tuesday, July 24, 2018	Sheet 50 of 139		

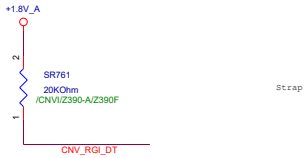
If use CNVi => SR354 Remove/ WR315 stuff
If don't use CNVi =>SR354 stuff

XTAL FREQUENCY SELECTION
1 = 24MHZ
0 = 38.4/19.2MHZ
PCH HAS INTERNAL 20K PD

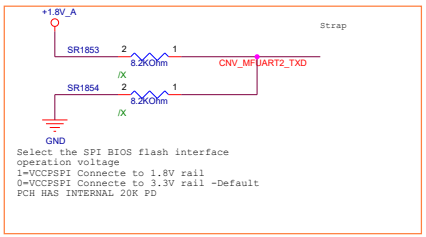
If use CNVi => SR760 Remove/ SR313 stuff
If don't use CNVi =>SR760 stuff



If use CNVi => SR761 Remove/ WR314 stuff
If don't use CNVi =>SR761 stuff

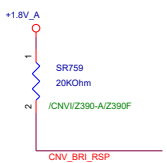


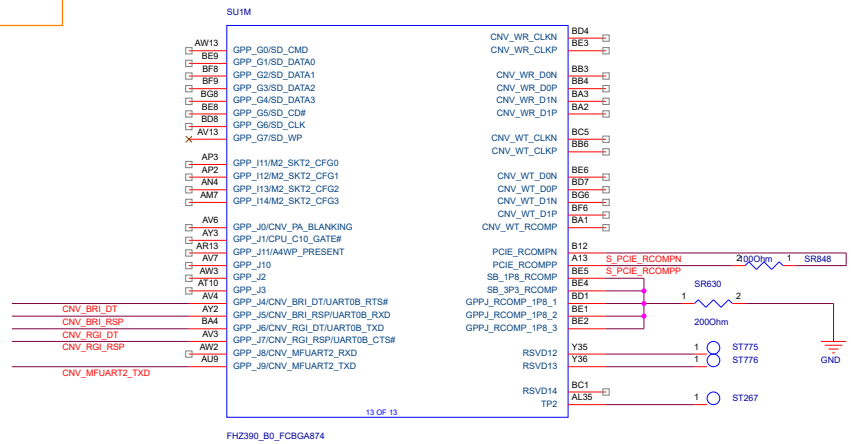
1 = Integrated CNVi disable
0 =Integrated CNVi enable
PCH HAS INTERNAL weak PU.



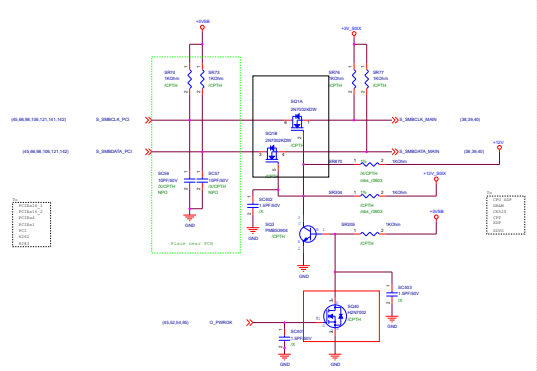
Select the SPI BIOS flash interface
operation voltage
1=VCCPSPI Connecte to 1.8V rail
0=VCCPSPI Connecte to 3.3V rail -Default
PCH HAS INTERNAL 20K PD

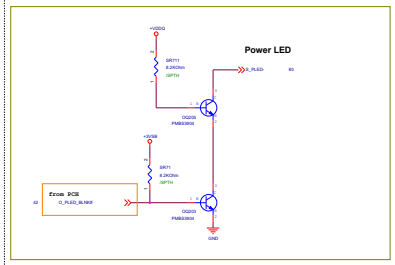
If use CNVi => SR759 Remove/ SR312 stuff
If don't CNVi =>SR759 stuff



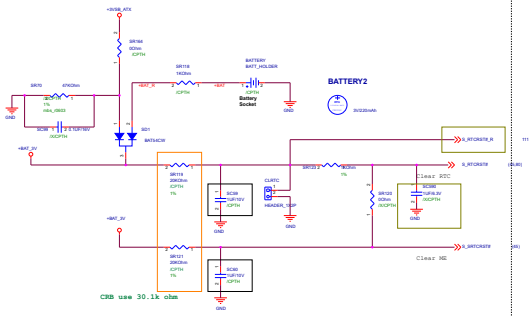


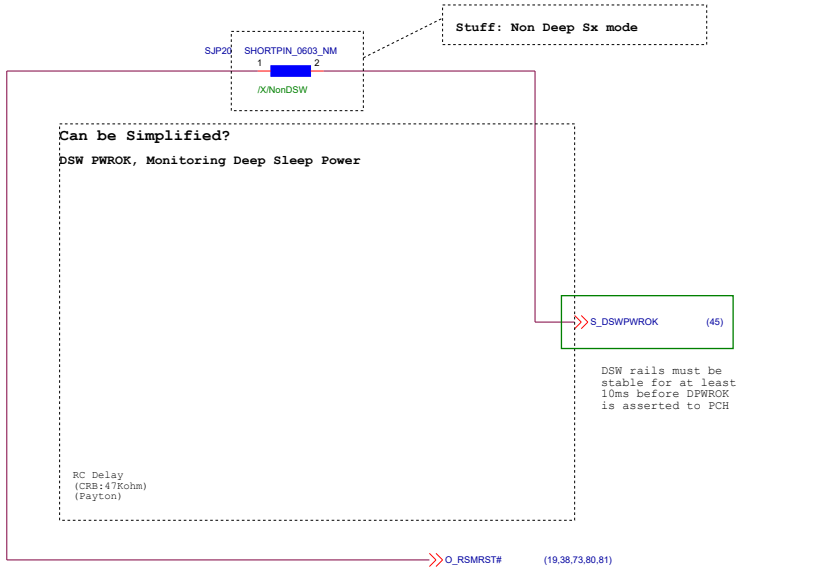
ASUSTek Computer Inc.	Title :	CPTH (CNVi)	
	Engineer:	Aaron_Su	
Size: A3	Project Name: Z390 Golden board		Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 51 of 139		





6/15 simplized for channel boards
6/18 connect with GP2025 for led work immediately
when power on





BackFeed Cut DSW & Backfeed Cut Logic

ASUSTek Computer Inc.

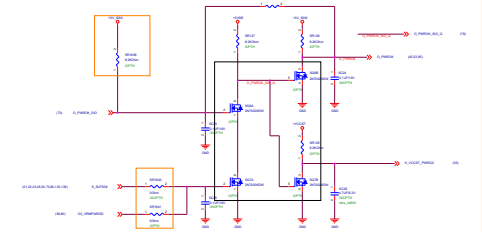
Title : CPTH (DSW SEQUENCE)

Engineer: Aaron_Su

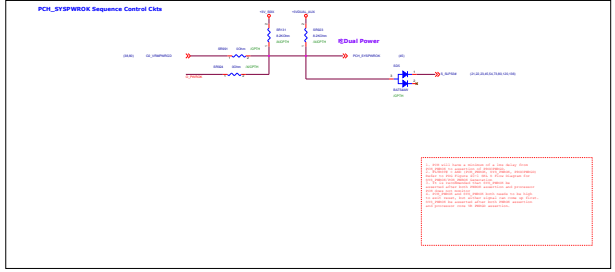
Size	Project Name	Rev
A3	Z390 Golden board	R1.00

Date: Tuesday, July 24, 2018 Sheet 53 of 139

PCH_PWROK Sequence Control Ckts



PCH_SYSPWROK Sequence Control Ckts



VCCST_PWRGD Sequence Control Ckts

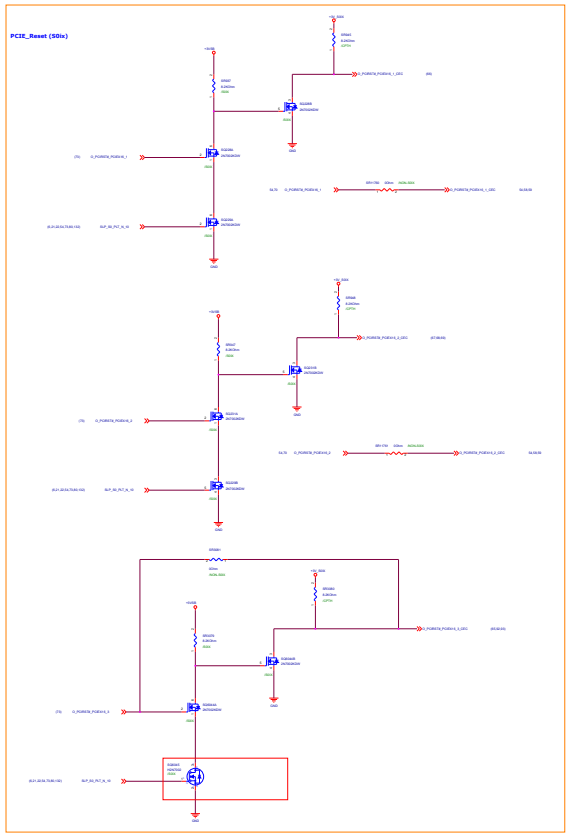
BATX Sequence Control Ckts

S0ix Sequence Control Ckts

S0ix:
PS_ON_B = 1
SLP_S0_B = 1
SLP_S0_PLT_N_10 = 0

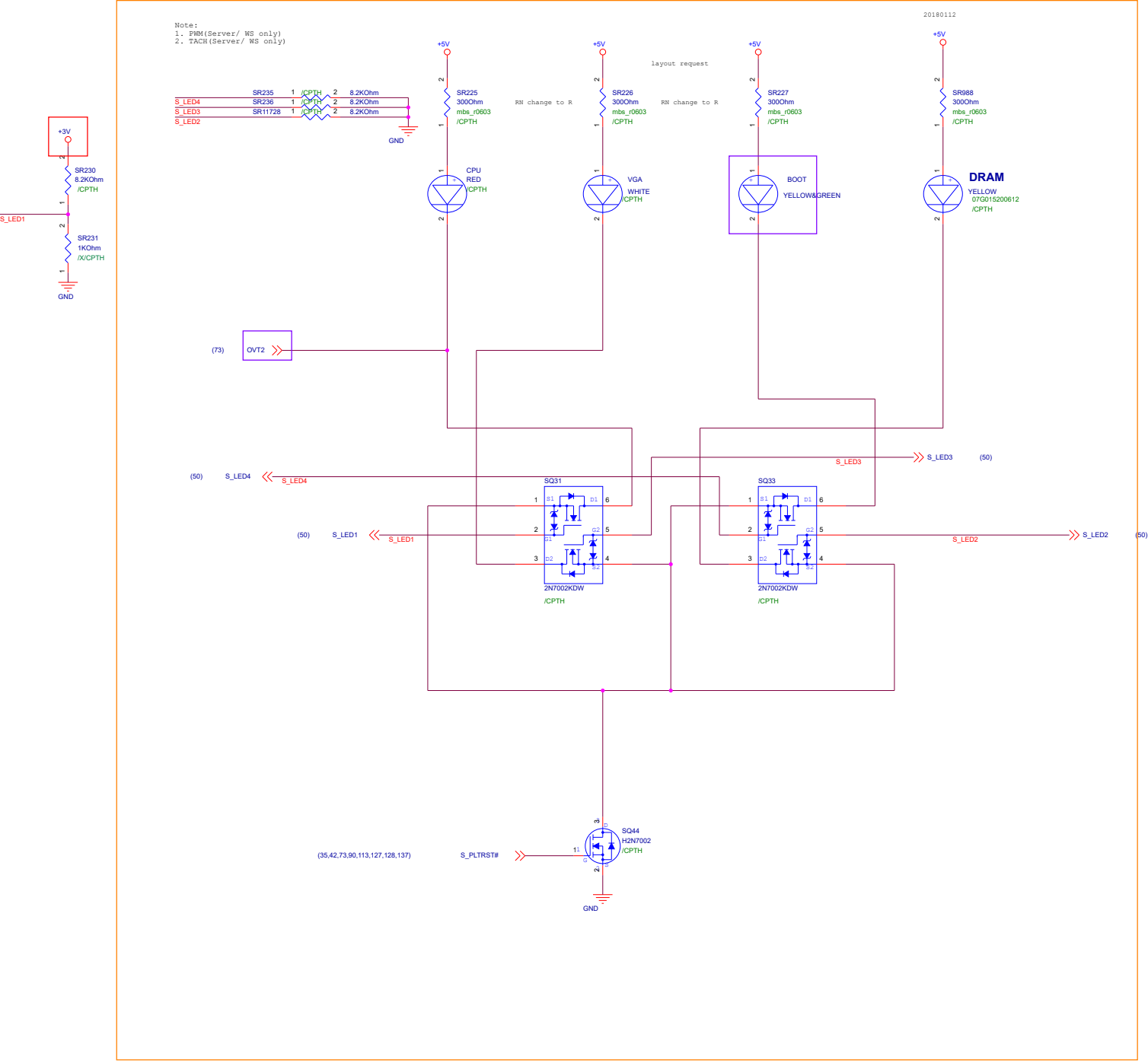
PS_ON# Logic

PCIE_Reset (S0ix)



Engineer: Aaron_Su

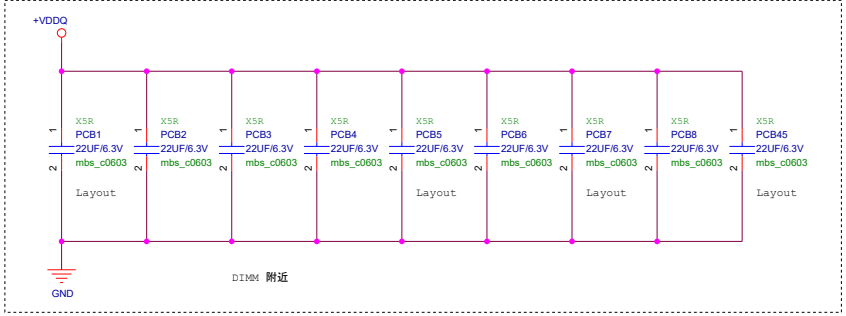
Z390 Golden board

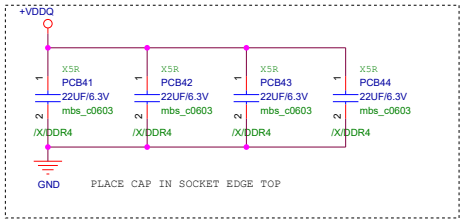


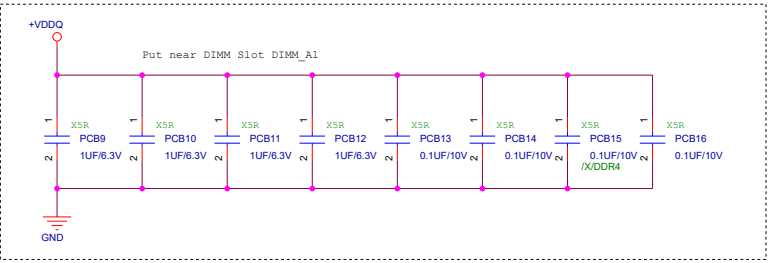
<Variant Name>

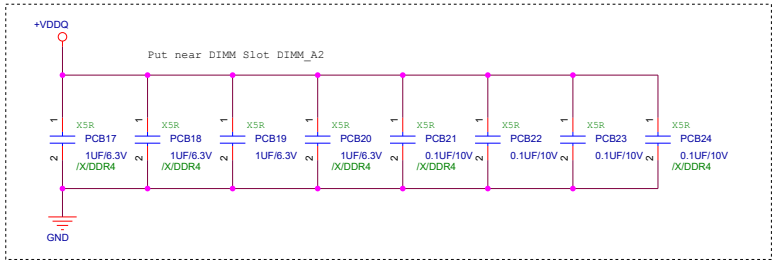
ASUSTeK COMPUTER INC	Title: CPTH EUP/LED Control	
	Engineer: Aaron_Su	
Size: A3	Project Name: Z390 Golden board	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 55 of 139	

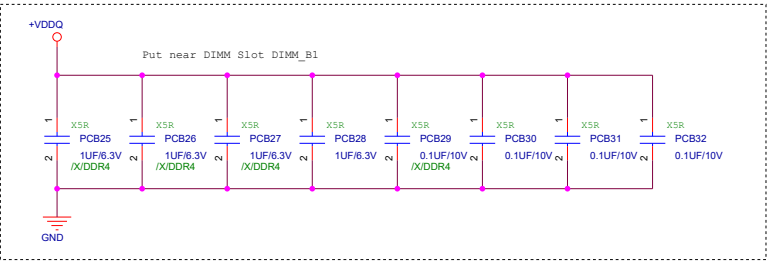
Layout to 0603

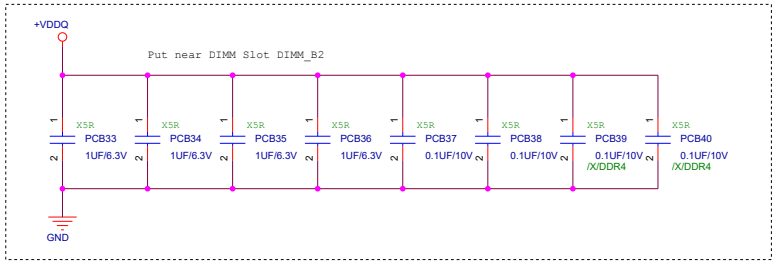


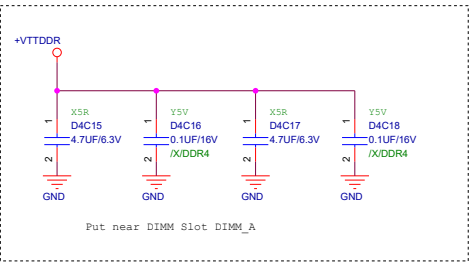


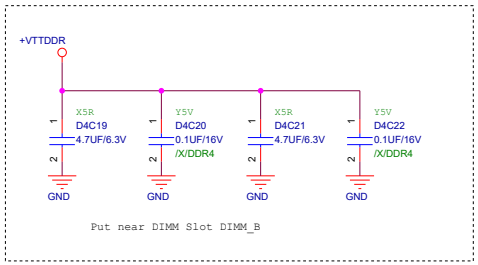


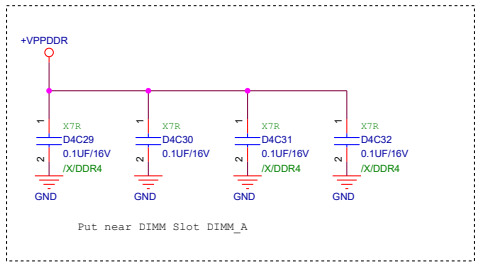


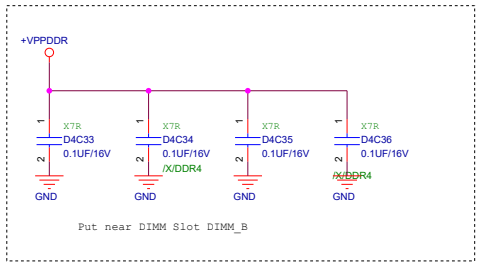












<Variant Name>

ASUSTek Computer Inc.	Title : DDR4 (Power CAPs)	
	Engineer: Aaron_Su	
Size: A3	Project Name: Z390 Golden board	Rev: 1.01
Date: Tuesday, July 24, 2018	Sheet 56 of 139	

DRAM SMBUS From PCH (Thru Level Shift)

<Variant Name>

ASUSTeK Computer Inc.

Title : DDR4 (SMBUS/SPD)

Engineer: Eason

Size	Project Name	Rev
A3	Z390 Golden board	1.00

Date: Tuesday, July 24, 2018 Sheet 57 of 139

Support Gen3

X_WAKE#

需在SB端Pull-high

Near Connector (Void)

Near Connector (Void)

Z390-A請用12003-00036000

PRSNT# PIN	Netname修改
使用此功能（請確認SB端是否要Pull-high）	請將PIN B17,B31,B48,B81 netname 改為X_1X16PRSNT#.
不使用此功能,且不support SLOT WARN & SDVO線路（請確認SB端是否要Pull-high or Pull-down）	請將PIN B17,B31,B48,B81 netname 改為GND.
Only support SDVO線路	PIN B17 --> X_SDVO_CLK PIN B31 --> X_SDVO_DATA PIN B48 --> X_EXP_SM

	SLOT 顏色
PCIEX16_1	LIGHT GRAY

<Variant Name>

ASUSTek Computer Inc.

Title : PCIEX16_1(LIGHT GRAY)

Engineer: Aaron_Su

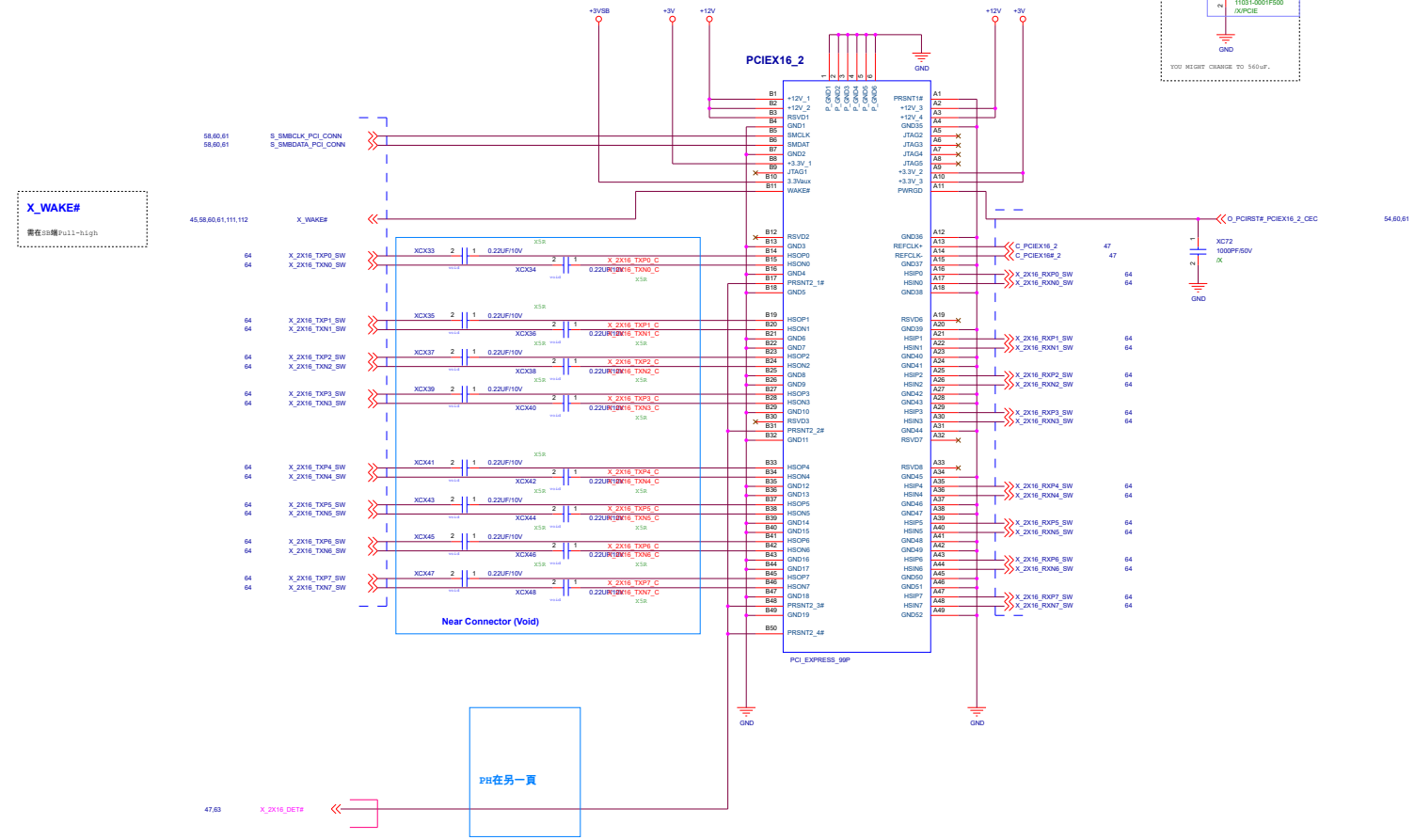
Size: A2 | Project Name: Z390 Golden board | Rev: 3.1

Date: Tuesday, July 24, 2018 | Sheet 58 of 129

Support Gen3

X_WAKE#

需在SB端Pull-high



	SLOT 顏色
PCIEX8_2	CHARCOAL_炭黑

PRSNT# PIN	Netname修改
使用此功能（請確認SB端是否要Pull-high）	請將PIN B17,B31,B48,B50 netname 改為X_2X16PRSNT#.
不使用此功能,且不support SLOT_WARN（請確認SB端是否要Pull-high or Pull-down）	請將PIN B17,B31,B48,B50 netname 改為GND.
Only support SLOT_WARN線路	請維持線路default netname.

<Variant Name>

ASUSTeK Computer Inc.

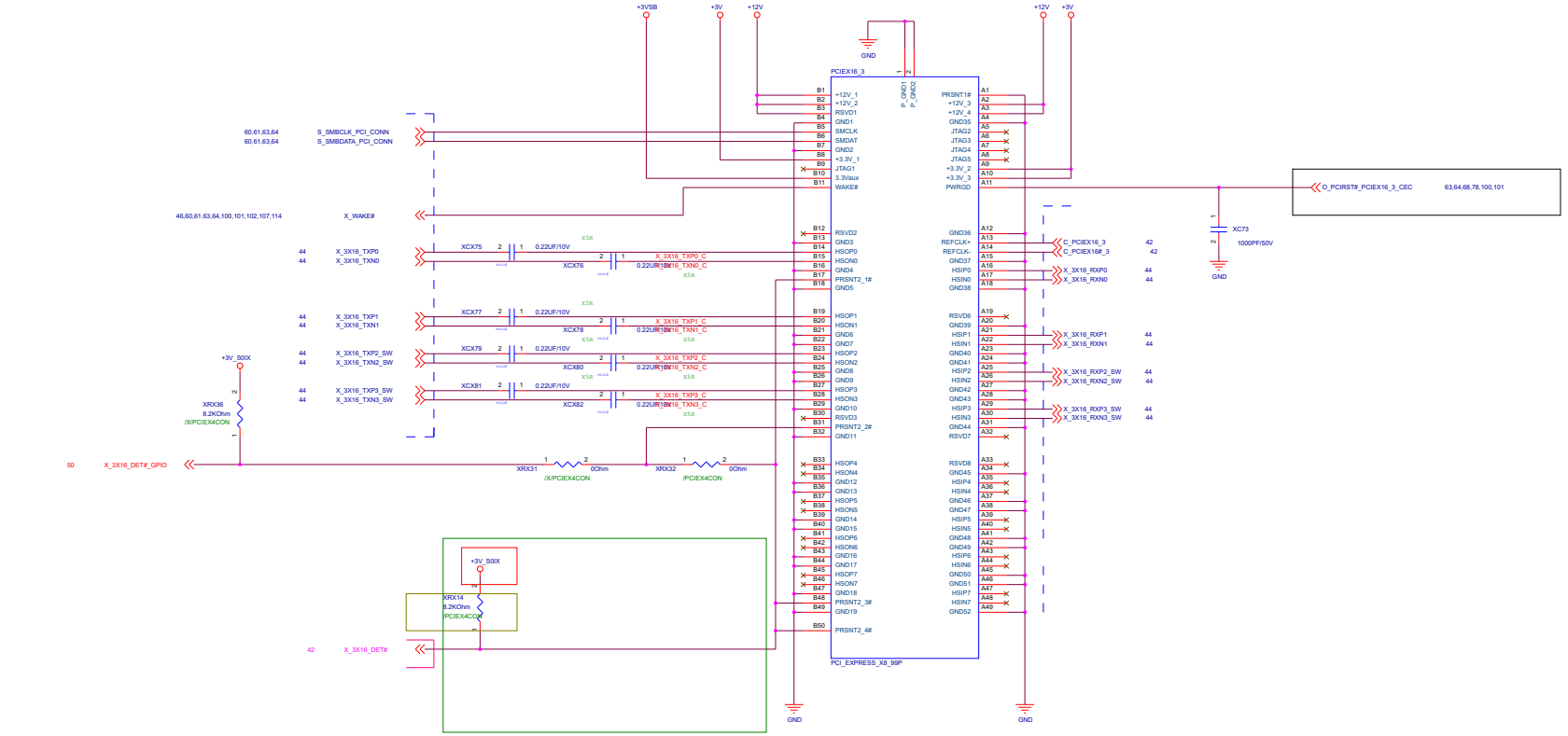
Title : PCIEX8_2(CHARCOAL_炭黑)

Engineer: Aaron_Su

Size	Project Name	Rev
A0	Z390 Golden board	3.1

Date: Tuesday, July 24, 2018 Sheet 59 of 129

Support Gen3



PRSNT# PIN	Netname修改
使用此功能（請確認SB端是否要Pull-high）	請將PIN B17,B31,B48,B50 netname 改為X_2X16PRSNT#.
不使用此功能,且不support SLOT_WARN（請確認SB端是否要Pull-high or Pull-down）	請將PIN B17,B31,B48,B50 netname 改為GND.
Only support SLOT_WARN線路	請維持線路default netname.

	SLOT 顏色
PCIEX4_3	BLACK_黑

X_WAKE#

需在SB端Pull-high

<Variant Name>

ASUSTek Computer Inc.

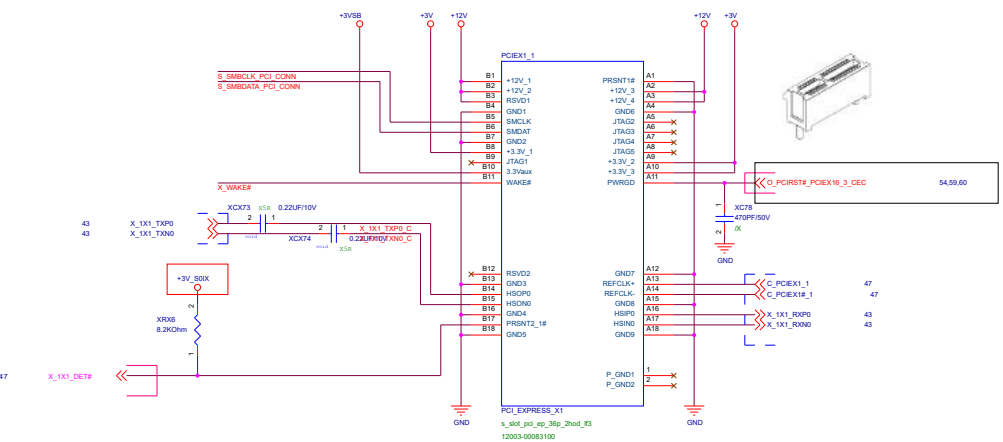
Title : PCIEX4_3(BLACK_黑)

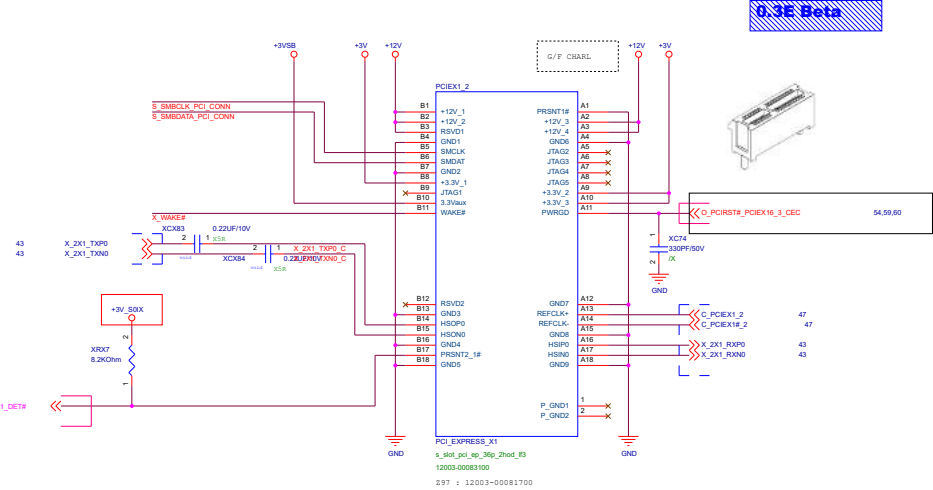
Engineer: Aaron_Su

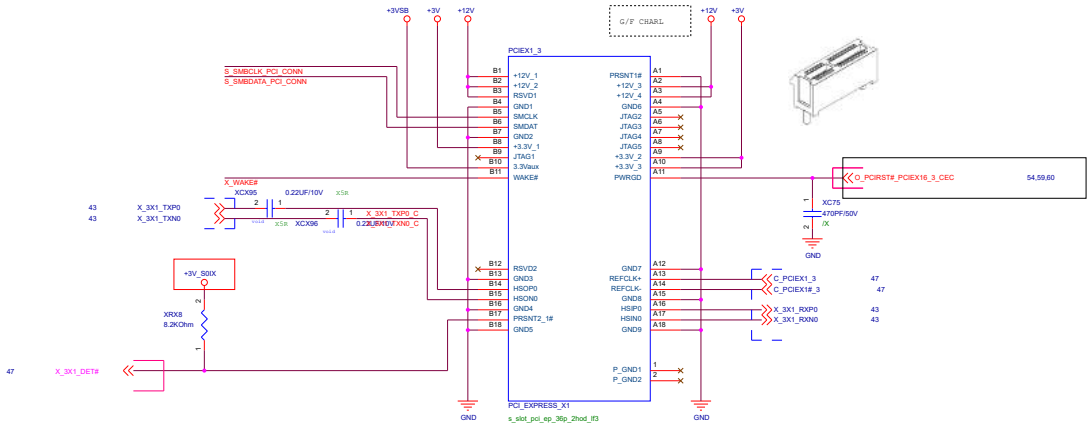
Size	Project Name	Rev
A2	Z390 Golden board	3.1

Date: Tuesday, July 24, 2018 Sheet 60 of 129

0.3E Beta







S_SMBCLK_PCI & S_SMBDATA_PCI

需接至SB SMBus(吃standby power)

58,59,60 S_SMBCLK_PCI_CONN
58,59,60 S_SMBDATA_PCI_CONN

45,58,59,60,111,112 X_WAKE#

X_WAKE#

需在SB端Pull-high

PRSNT# PIN	Netname修改
使用此功能（請確認SB端是否要Pull-high）	請維持線路default netname.
不使用此功能（請確認SB端是否要Pull-high or Pull-down）	請將PIN B17 netname 改為GND.

<Variant Name>

ASUSTek COMPUTER INC.

Title : PCIEX1_1

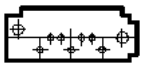
Engineer: Eason

Size	Project Name	Rev
A2	Z170-DELUXE	R1.02A

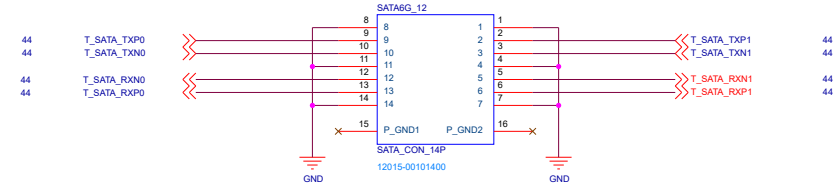
Date: Tuesday, July 24, 2018 Sheet 61 of 129

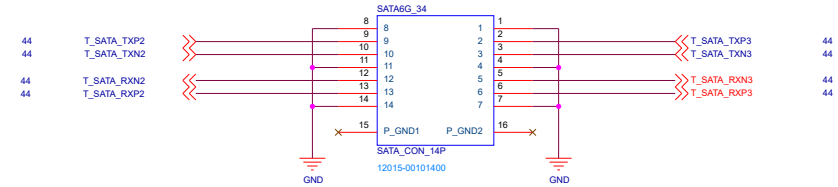
	Connector 顏色
SATA6G_123456	LIGHT GRAY
	BROWN

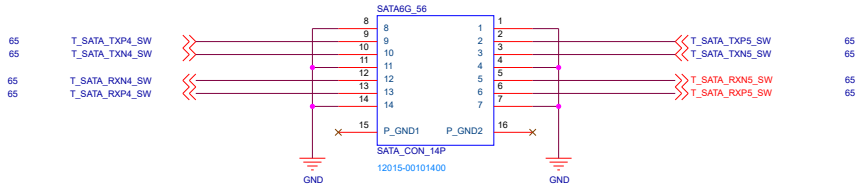
R/A Connector擺放與板端切齊，
如上圖黑色箭頭處.

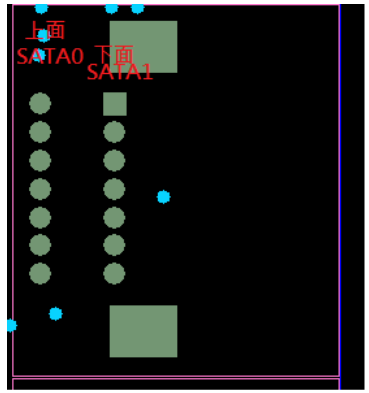


	Connector 顏色
SATA6G_123456	LIGHT GRAY
	NAVY BLUE



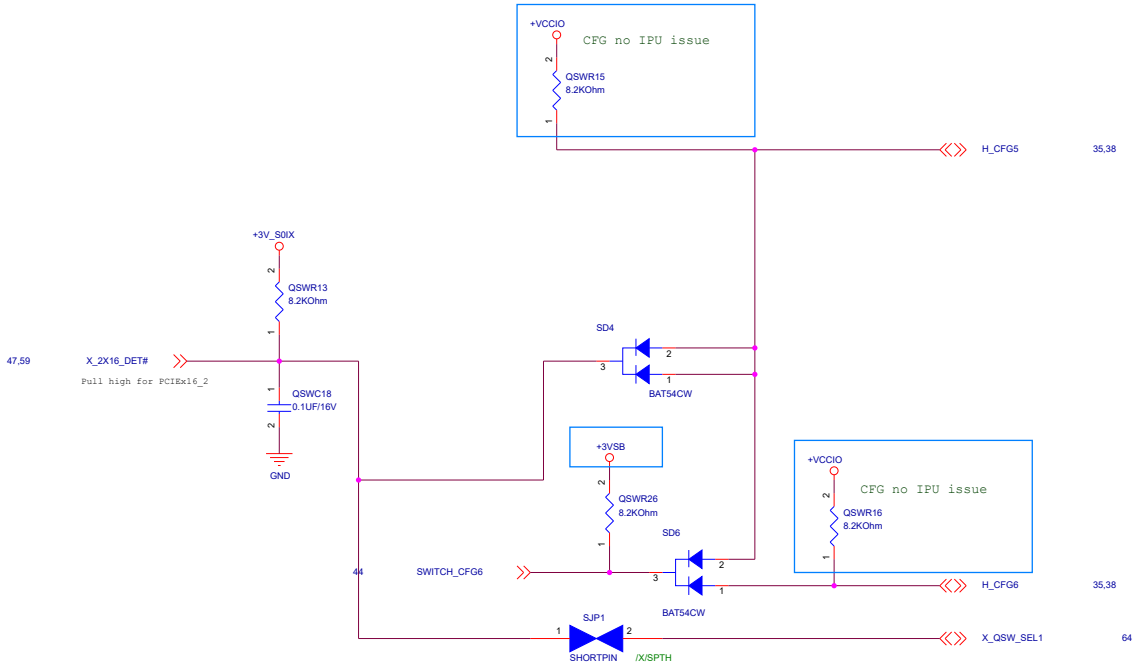






ASUSTek Computer Inc.	Title : SATA6G_1-8 Connector	
	Engineer: Scott2_Lin	
Size: A3	Project Name: X299-Golden Board	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 62 of 129	

For add-in card only in X16_1 & X16_2



ALL CFG 1 = NO TERMAINATION ON BOARD DEFAULT HIGH
ALL CFG 0 = PHYSICAL STRAP LOW ON BOARD

CoffeeLake Strap Table Rev 0.5			
All Have Internal Pull-Ups +VCCIO			
CFG	H = 1	L = 0	Description
0	Normal	STALL	EAR
1			Reserved
2	**Normal**	**Lane Reverse**	**PCIEX16 Lane Reversal**
3			Reserved
4	disable	enable	eDP
5	**PCIE Config**	**PCIE Config**	**SEL[0]**
6	**PCIE Config**	**PCIE Config**	**SEL[1]**
7	RESET#	BIOS REQ	**PEG Training**
8-19			Reserved

CFG[6:5]: PCI Express* Bifurcation
- 00 = 1 x8, 2 x4 PCI Express*
- 01 = reserved
- 10 = 2 x8 PCI Express*
- 11 = 1 x16 PCI Express*

<Variant Name>

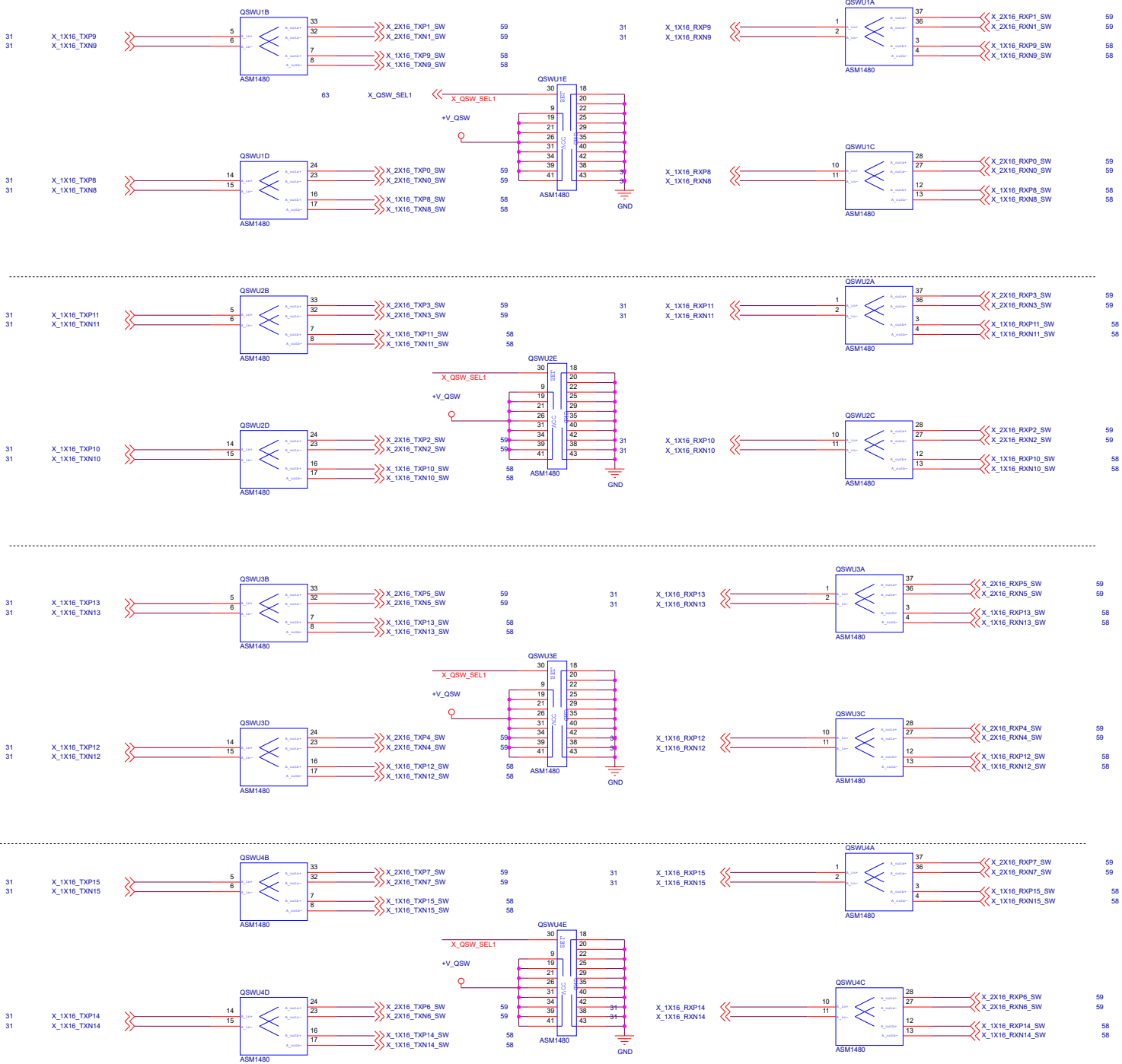
ASUSTek COMPUTER INC.

Title : QUICK SWITCH(PCIEX16)

Engineer: Eason

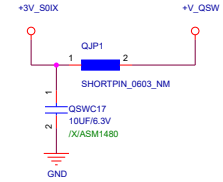
Size	Project Name	Rev
A3	Z170-DELUXE	R1.02A

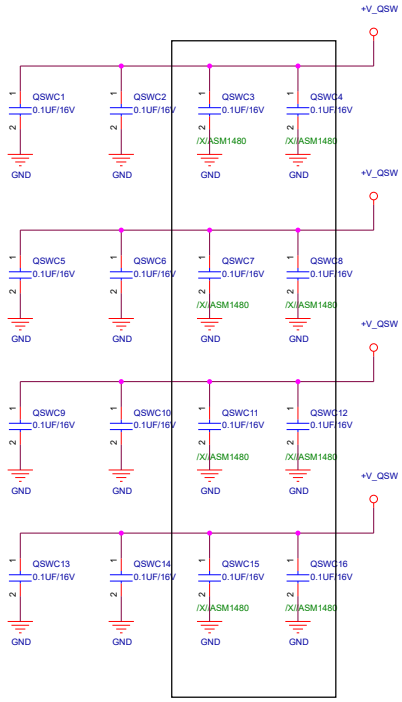
Date: Tuesday, July 24, 2018 Sheet 63 of 129



Sel Pin	Function	
L	N_in to N_outa	PCIEX16_2
H	N_in to N_outb	PCIEX16_1

3.3V for 1440 new version
1.8V for 1440 old version





<Variant Name>

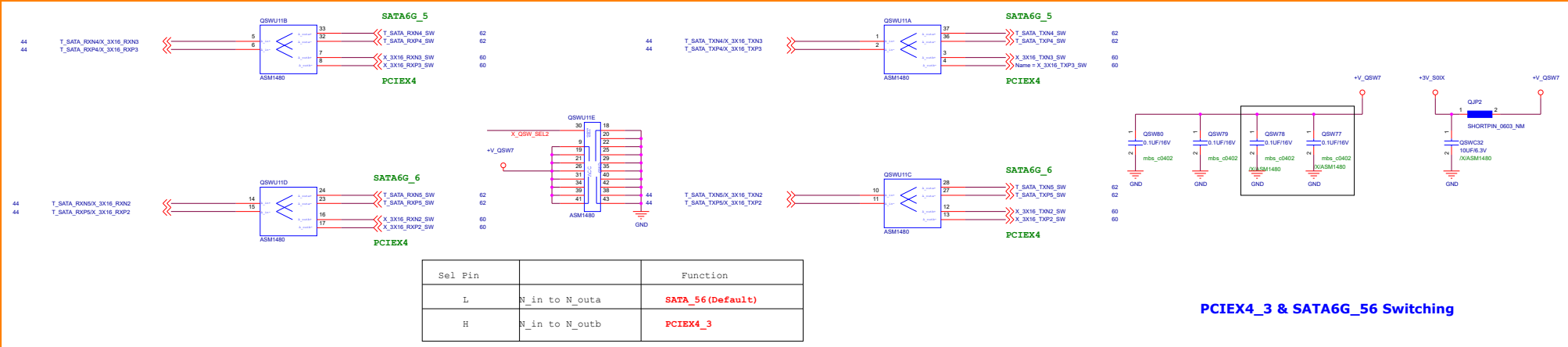
ASUSTek COMPUTER INC.

Title : Switch 1440

Engineer: KENNY_CHEN

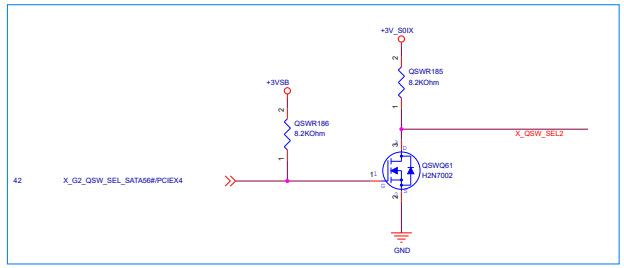
Size	Project Name	Rev
A3	Z87-PRO	R1.02A

Date: Tuesday, July 24, 2018 Sheet 64 of 129



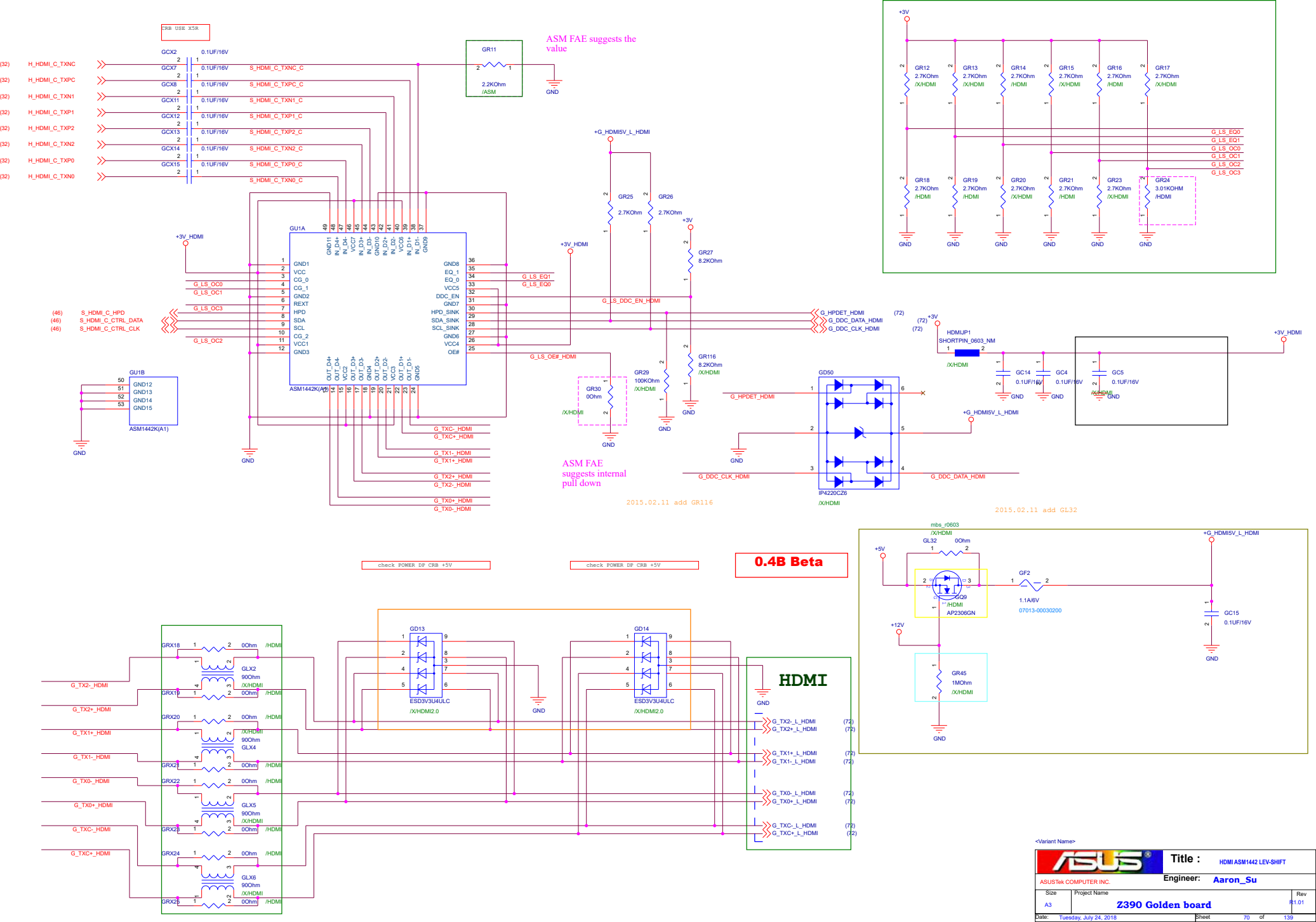
Sel Pin		Function
L	N_in to N_outa	**SATA_56(Default)**
H	N_in to N_outb	**PCIEX4_3**

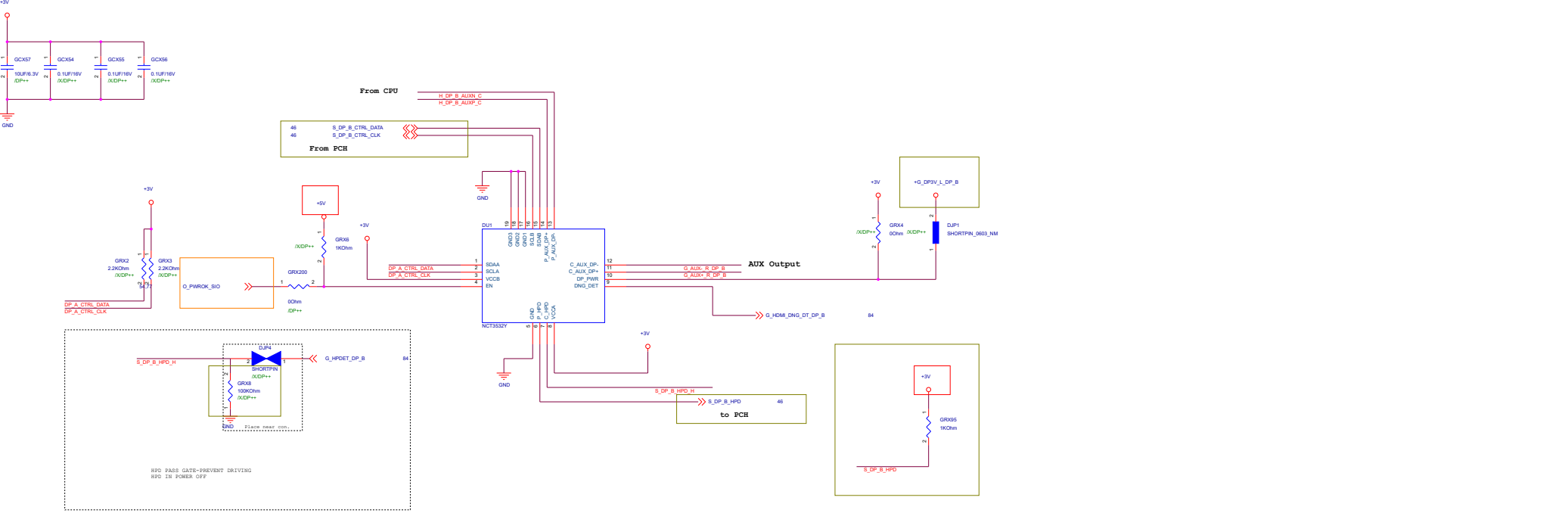
PCIEX4_3 & SATA6G_56 Switching



<Variant Name>

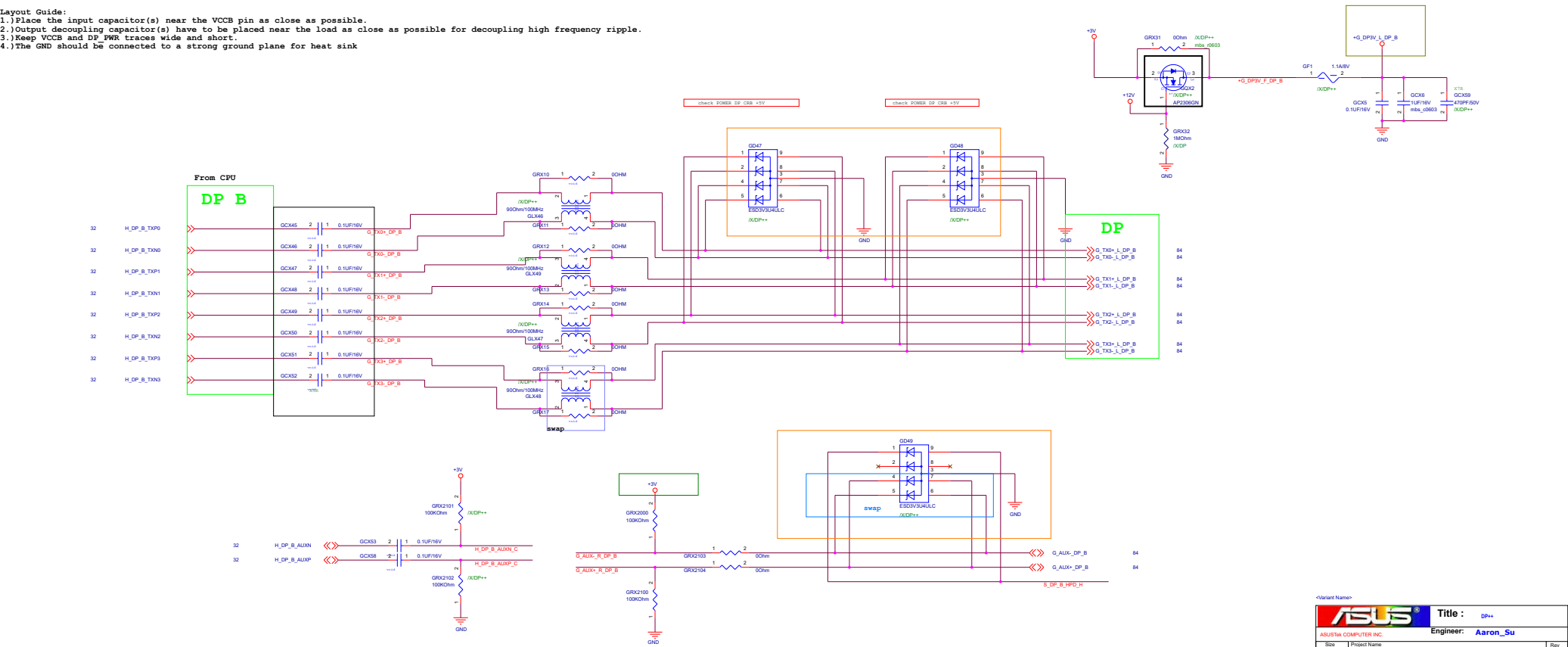
ASUSTek COMPUTER INC.	Title : Q-SW PCIE&SATA_56)	
	Engineer: Aaron_Su	
Size: C	Project Name: Z390 Golden board	Rev: R1.00
Date: Tuesday, July 24, 2018	Sheet 65 of 129	


CRB USE X5R
ASM FAE suggests the value
GR11
2.2KOhm /ASM
GCX2 0.1UF/16V S_HDMI_C_TXNC_C
GCX7 0.1UF/16V S_HDMI_C_TXPC_C
GCX8 0.1UF/16V S_HDMI_C_TXN1_C
GCX11 0.1UF/16V S_HDMI_C_TXP1_C
GCX12 0.1UF/16V S_HDMI_C_TXP2_C
GCX13 0.1UF/16V S_HDMI_C_TXN2_C
GCX14 0.1UF/16V S_HDMI_C_TXP0_C
GCX15 0.1UF/16V S_HDMI_C_TXN0_C
(32) H_HDMI_C_TXNC
(32) H_HDMI_C_TXPC
(32) H_HDMI_C_TXN1
(32) H_HDMI_C_TXP1
(32) H_HDMI_C_TXP2
(32) H_HDMI_C_TXN2
(32) H_HDMI_C_TXP0
(32) H_HDMI_C_TXN0
GU1A
ASM1442K(A1)
GU1B
ASM1442K(A1)
+3V_HDMI
+G_HDMI5V_L_HDMI
GR25 2.7KOhm
GR26 2.7KOhm
GR27 8.2KOhm
GR116 8.2KOhm /X/HDMI
GR29 100KOhm /X/HDMI
GR30 0Ohm /X/HDMI
G_LS_DDC_EN_HDMI
G_LS_EQ1
G_LS_EQ0
G_LS_OE#_HDMI
G_LS_OC0
G_LS_OC1
G_LS_OC3
G_LS_OC2
(46) S_HDMI_C_HPD
(46) S_HDMI_C_CTRL_DATA
(46) S_HDMI_C_CTRL_CLK
G_HPDET_HDMI
G_DDC_DATA_HDMI
G_DDC_CLK_HDMI
GD50
IP4220CZ6 /X/HDMI
HDMIJP1 SHORTPIN_0603_NM /X/HDMI
GC14 0.1UF/16V
GC4 0.1UF/16V
GC5 0.1UF/16V /X/HDMI
GR12 2.7KOhm /X/HDMI
GR13 2.7KOhm /X/HDMI
GR14 2.7KOhm /HDMI
GR15 2.7KOhm /X/HDMI
GR16 2.7KOhm /HDMI
GR17 2.7KOhm /X/HDMI
GR18 2.7KOhm /HDMI
GR19 2.7KOhm /HDMI
GR20 2.7KOhm /X/HDMI
GR21 2.7KOhm /HDMI
GR23 2.7KOhm /X/HDMI
GR24 3.01KOHM /HDMI
G_LS_EQ0
G_LS_EQ1
G_LS_OC0
G_LS_OC1
G_LS_OC2
G_LS_OC3
ASM FAE suggests internal pull down
2015.02.11 add GR116
2015.02.11 add GL32
check POWER DP CRB +5V
check POWER DP CRB +5V
0.4B Beta
GRX18 0Ohm /HDMI
GRX19 0Ohm /HDMI
GRX20 0Ohm /HDMI
GRX21 0Ohm /HDMI
GRX22 0Ohm /HDMI
GRX23 0Ohm /HDMI
GRX24 0Ohm /HDMI
GRX25 0Ohm /HDMI
GLX2 90Ohm /X/HDMI
GLX4 90Ohm /X/HDMI
GLX5 90Ohm /X/HDMI
GLX6 90Ohm /X/HDMI
GD13 ESD3V3U4ULC /X/HDMI2.0
GD14 ESD3V3U4ULC /X/HDMI2.0
HDMI
G_TX2-_HDMI
G_TX2+_HDMI
G_TX1+_HDMI
G_TX1-_HDMI
G_TX0-_HDMI
G_TX0+_HDMI
G_TXC-_HDMI
G_TXC+_HDMI
G_TX2-_L_HDMI
G_TX2+_L_HDMI
G_TX1+_L_HDMI
G_TX1-_L_HDMI
G_TX0-_L_HDMI
G_TX0+_L_HDMI
G_TXC-_L_HDMI
G_TXC+_L_HDMI
mbs_r0603 /X/HDMI
GL32 0Ohm
GQ9 /HDMI AP2306GN
GF2 1.1A/6V 07013-00030200
GR45 1MOhm /X/HDMI
GC15 0.1UF/16V
+5V
+12V
GND
<Variant Name>
ASUSTek COMPUTER INC.
Title : HDMI ASM1442 LEV-SHIFT
Engineer: Aaron_Su
Size A3
Project Name Z390 Golden board
Rev R1.01
Date: Tuesday, July 24, 2018
Sheet 70 of 139



Layout Guide:

1.)Place the input capacitor(s) near the VCCB pin as close as possible.
2.)Output decoupling capacitor(s) have to be placed near the load as close as possible for decoupling high frequency ripple.
3.)Keep VCCB and DP_PWR traces wide and short.
4.)The GND should be connected to a strong ground plane for heat sink



<Variant Name>

ASUSTek COMPUTER INC.

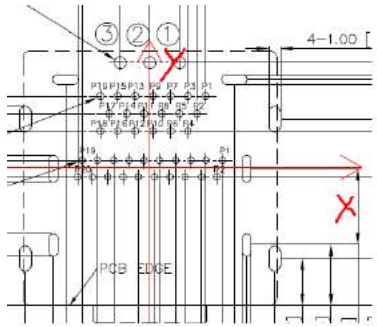
Title : DP++

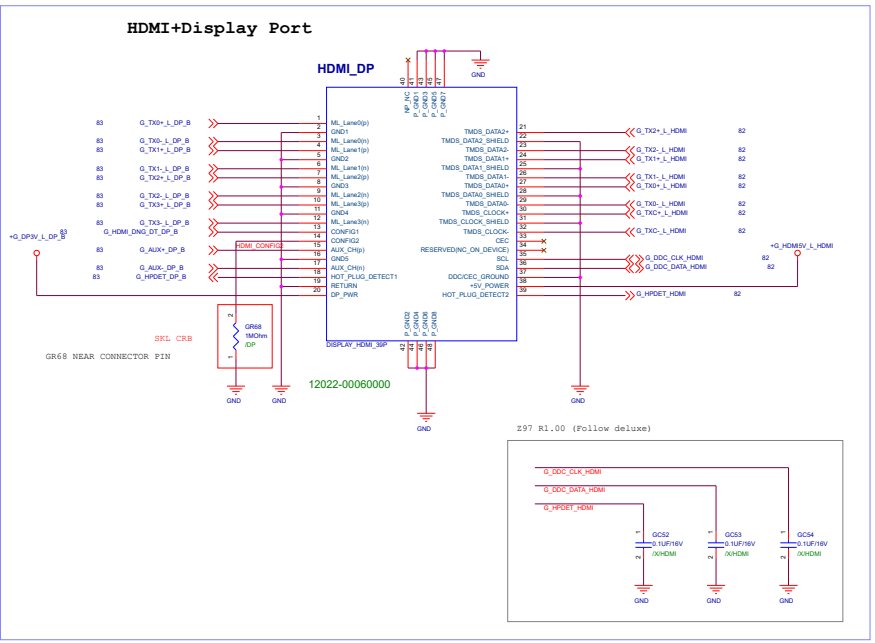
Engineer: Aaron_Su

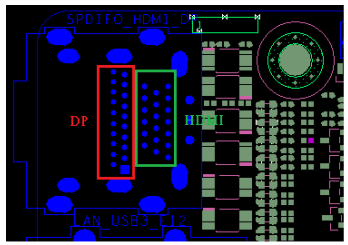
Size: A2 | Project Name: CoffeeLake VC | Rev: 81.00

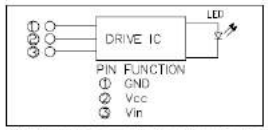
Date: Tuesday, July 24, 2018 | Sheet 83 of 129

2016.03.30 Remove VGA Connector





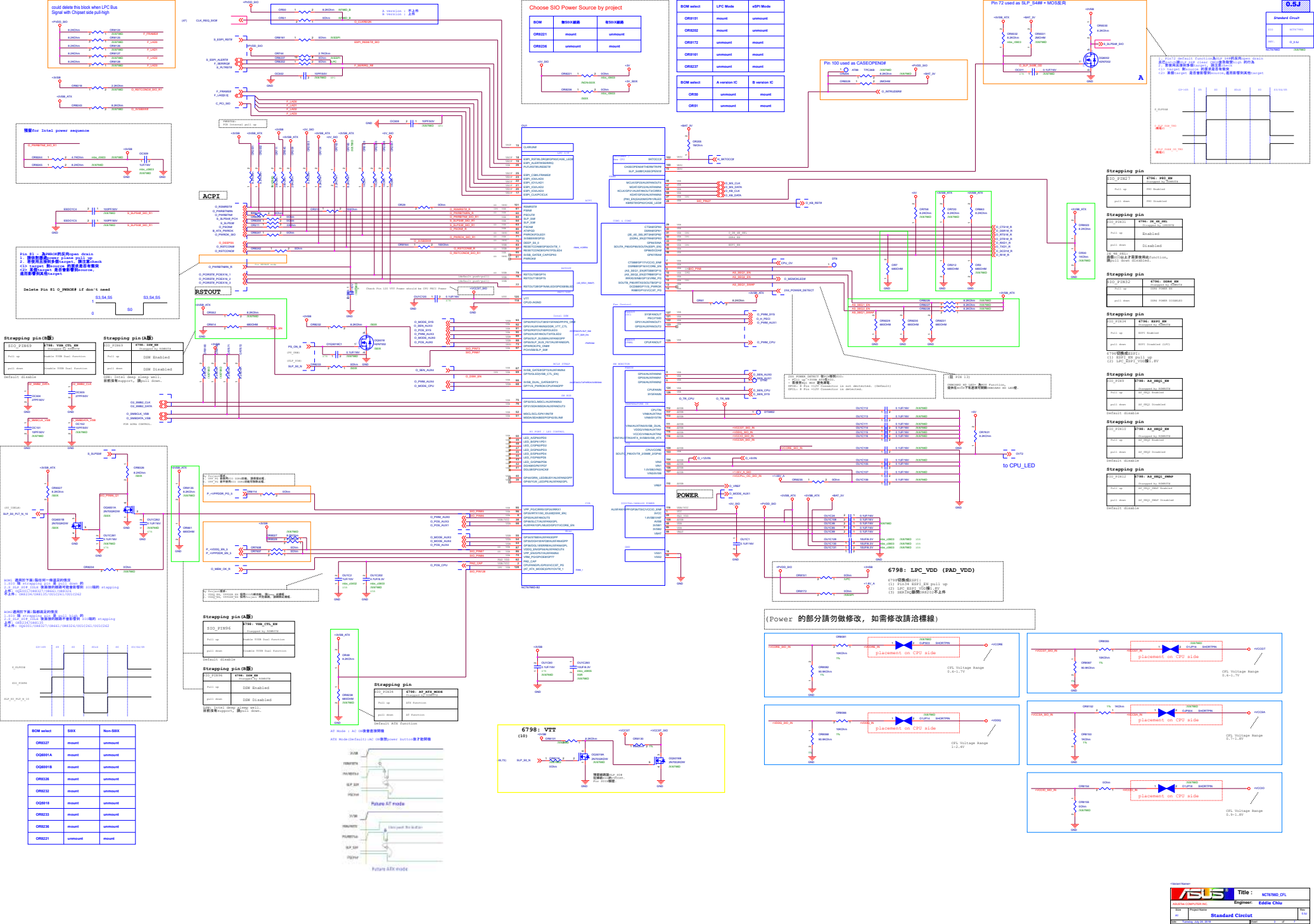




7. HDMI AND DP PIN ASSIGNMENTS:

HDMI			
PIN NO.	SIGNAL ASSIGNMENT	PIN NO.	SIGNAL ASSIGNMENT
P1	TMDS DATA2+	P2	TMDS DATA2 SHIELD
P3	TMDS DATA2-	P4	TMDS DATA1+
P5	TMDS DATA1 SHIELD	P6	TMDS DATA1-
P7	TMDS DATA0+	P8	TMDS DATA0 SHIELD
P9	TMDS DATA0-	P10	TMDS CLOCK+
P11	TMDS CLOCK SHIELD	P12	TMDS CLOCK-
P13	CEC	P14	RESERVED (N.C. ON DEVICE)
P15	SCL	P16	SDA
P17	DDC/CEC GROUND	P18	+5V POWER
P19	HOT PLUG DETECT		

DISPLAYPORT		
PIN NUMBER	SOURCE-SIDE PIN ASSIGNMENT	SINK-SIDE PIN ASSIGNMENT
P1	ML_Lane 0(p)	ML_Lane 3(n)
P2	GND	GND
P3	ML_Lane 0(n)	ML_Lane 3(p)
P4	ML_Lane 1(p)	ML_Lane 2(n)
P5	GND	GND
P6	ML_Lane 1(n)	ML_Lane 2(p)
P7	ML_Lane 2(p)	ML_Lane 1(n)
P8	GND	GND
P9	ML_Lane 2(n)	ML_Lane 1(p)
P10	ML_Lane 3(p)	ML_Lane 0(n)
P11	GND	GND
P12	ML_Lane 3(n)	ML_Lane 0(p)
P13	CONFIG1	CONFIG1
P14	CONFIG2	CONFIG2
P15	AUX CH (p)	AUX CH (p)
P16	GND	GND
P17	AUX CH (n)	AUX CH (n)
P18	HOT PLUG DETECT	HOT PLUG DETECT
P19	RETURN	RETURN
P20	DP PWR	DP PWR


could delete this block when LPC Bus Signal with Chipset side pull-high
Choose SIO Power Source by project
BOM | 無SIO裝機 | 有SIO裝機
OR8221 | mount | unmount
OR8236 | unmount | mount
BOM select | LPC Mode | eSPI Mode
OR8101 | mount | unmount
OR8202 | mount | unmount
OR8172 | unmount | mount
OR8161 | unmount | mount
OR8237 | unmount | mount
BOM select | A version IC | B version IC
OR50 | unmount | mount
OR51 | unmount | mount
Pin 72 used as SLP_S4## + MOS反向
Pin 100 used as CASEOPEN#
0.5J
Standard Circuit
預留for Intel power sequence
ACPI
RSTOUT
Pin 81 = 為PWROK的反向open drain
Delete Pin 81 O_PWROK# if don't need
Strapping pin(B版)
SIO_PIN69 | 6798: VSB_CTL_EN
Strapping pin(A版)
SIO_PIN69 | 6798: DSW_EN
Strapping pin(A版)
SIO_PIN96 | 6798: VSB_CTL_EN
Strapping pin(B版)
SIO_PIN96 | 6798: DSW_EN
Strapping pin
SIO_PIN24 | 6798: AT_ATX_MODE
Future AT mode
Future ATX mode
6798: VTT
(10)
6798: LPC_VDD (PAD_VDD)
(Power 的部分請勿做修改, 如需修改請洽標籤)
placement on CPU side
CFL Voltage Range 0.4-1.7V
CFL Voltage Range 1-2.4V
CFL Voltage Range 0.7-1.8V
CFL Voltage Range 0.8-1.8V
BOM select | S0IX | Non-S0IX
OR8327 | mount | unmount
OQ8501A | mount | unmount
OQ8501B | mount | unmount
OR8326 | mount | unmount
OR8232 | mount | unmount
OQ8518 | mount | unmount
OR8233 | mount | unmount
OR8236 | mount | unmount
OR8221 | unmount | mount
Strapping pin
SIO_PIN27 | 6796: PSO_EN
SIO_PIN31 | 6796: DS_OC_SEL
SIO_PIN72 | 6796: DDR4_EN
SIO_PIN34 | 6796: ESPI_EN
SIO_PIN5 | 6796: AZ_SDO2_EN
SIO_PIN15 | 6796: AZ_SDO2_EN
SIO_PIN12 | 6796: AZ_SDO1_SNAP
to CPU_LED
Standard AC LED 為ACC Function, 請將此ACC下拉並且預留0ohm reserved AC LED電阻.
Title : NCT6796D_CFL
Engineer: Eddie Chiu
Standard Circuit
Tuesday, July 24, 2018

0.5F

Connect to Connector

(A)

Dual Power

+O_KBMS_5V_L
+O_KBMS_5V_F
+5V_DUAL_USBKB
OJP3
SHORTPIN_0603_NM
/X/6798D
OF1
1.1A/6V
OC36
0.1UF/16V
EMI REQUEST.
GND

+O_KBMS_5V_F
OR2024
4.7KOhm
OJP4
33Ohm
O_KB_CLK_L
O_KB_CLK_R
SHORTPIN_0603_NM
/X/6798D
OR2028
O_KB_CLK
77
76 O_KB_CLK_L
76 O_KB_DATA_L
OC37
150PF/50V
NPO
ESD issue
GND

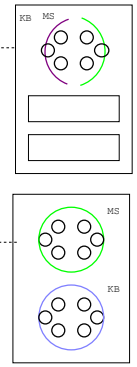
+O_KBMS_5V_F
OR2025
4.7KOhm
OJP5
33Ohm
O_KB_DATA_L
O_KB_DATA_R
SHORTPIN_0603_NM
/X/6798D
OR2029
O_KB_DATA
77
OC38
150PF/50V
NPO
ESD issue
GND

OD1
O_KB_DATA_L
O_KB_CLK_L
+O_KBMS_5V_L
GND
IP4220CZ6

+O_KBMS_5V_F
+O_KBMS_5V_F
OR2027
4.7KOhm
OR2026
4.7KOhm
O_MS_CLK
77
O_MS_DATA
77

(B)

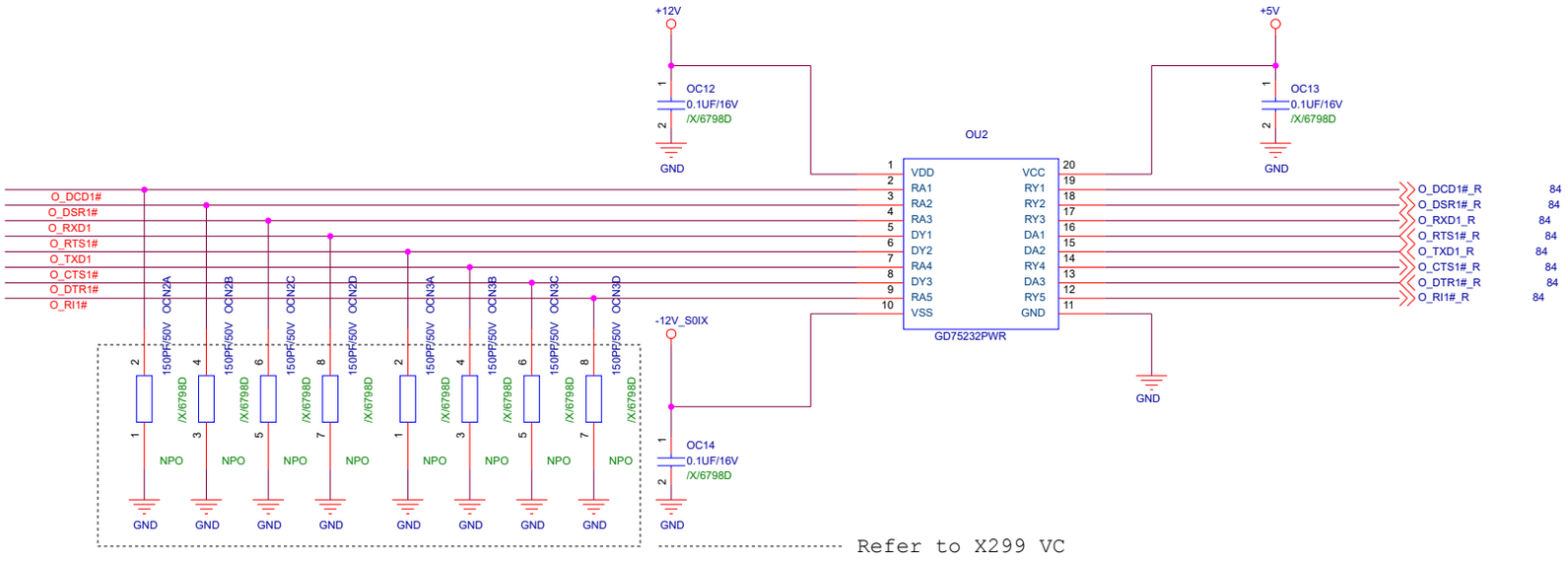
3擇1, By Project 需求:
1. 如無Onboard KBMS connector , 請保留(C)框, 刪除(A)(B)框.
2. 如connector只有一個KBMS孔 請留(A)框, 刪除(B)(C)框.
3. 如connector分別各有一個KB, 一個MOS孔, 請留(A)(B)框, 刪除(C)框.



(C)

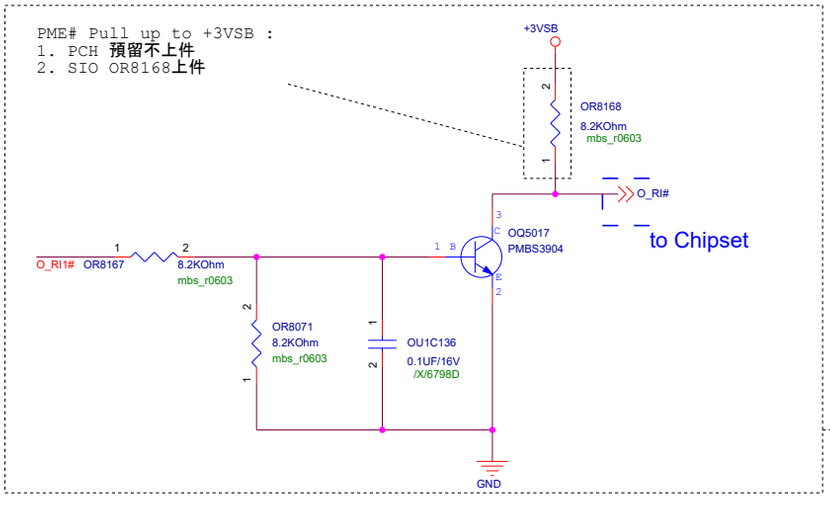
<Variant Name>

ASUSTek COMPUTER INC.	Title : NCT6798D_CFL-2	
	Engineer: Eddie Chiu	
Size: A3	Project Name: Standard Circiut	Rev: 0.5F
Date: Tuesday, July 24, 2018	Sheet 78 of 129	



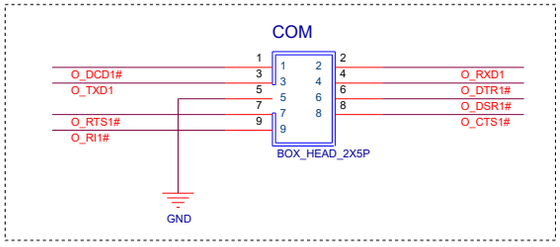
RING Function

PME# Pull up to +3VSB :
1. PCH 預留不上件
2. SIO OR8168上件



COM

Box Header



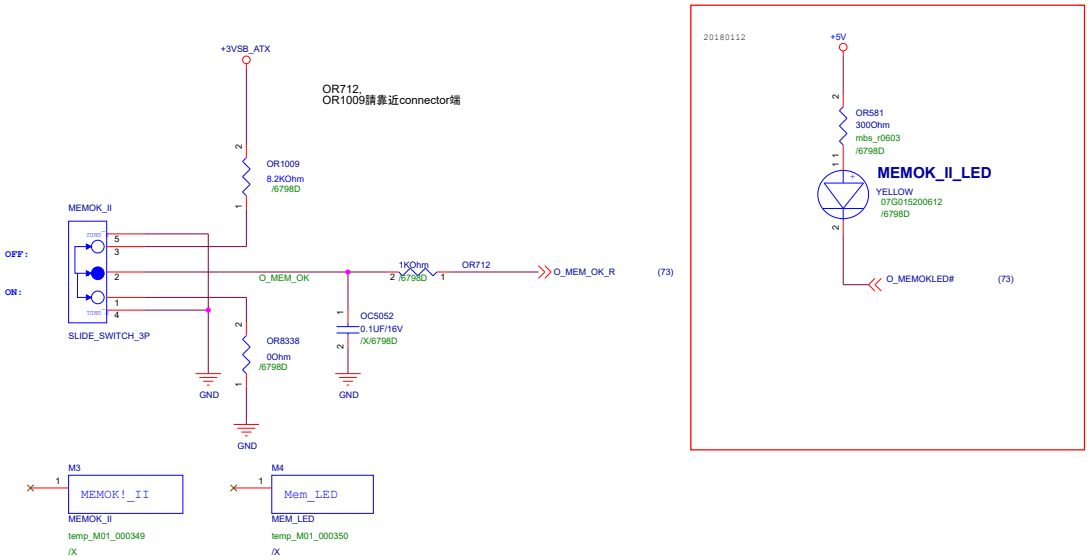
有COM PORT Header的Model需上此線路,
避免關機時PME#意外被觸發的issue.

<Variant Name>

ASUSTeK COMPUTER INC	Title : NCT6798D_CFL-3	
	Engineer: Eddie Chiu	
Size: A3	Project Name: Standard Circuit	Rev: 0.5F
Date: Tuesday, July 24, 2018	Sheet 5 of 7	

0.5F

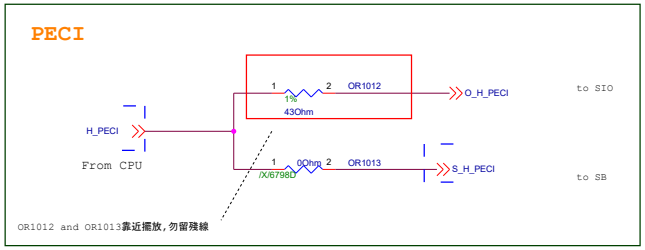
MemOK II Circuit



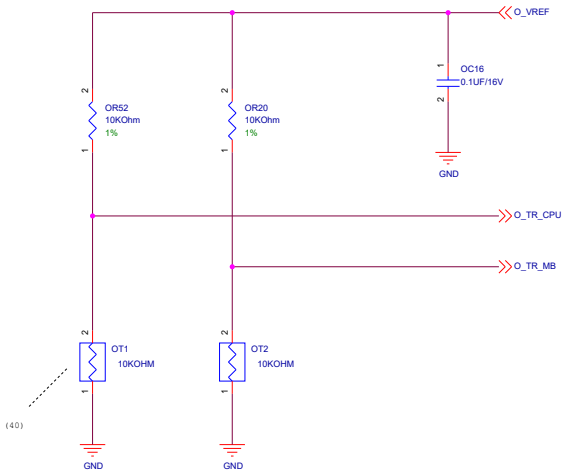
6/12 revised the circuits to two 0 ohm style

SKL PDG CRB CPU PECI to EC PECI have 43 ohm

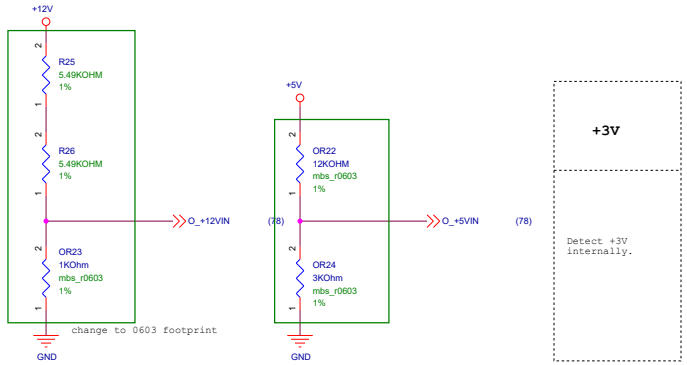
Z97 OR1012 0 ohm



Hardware Monitor for Temperature



Hardware Monitor for VIN



<Variant Name>

ASUSTeK COMPUTER INC	Title : NCT6798D_CFL-4	
	Engineer: Eddie Chiu	
Size: A3	Project Name: Standard Circiut	Rev: 0.5F
Date: Tuesday, July 24, 2018	Sheet 6 of 7	

Port 80 (7 Segment). SIO is common athode.

1.1

Q_CODE_High byte

Q_CODE_low byte

<Variant Name>

Title : NCT6796D_BF-5

ASUSTek COMPUTER INC.

Engineer: Eagle

Size	Project Name	Rev
A3	Standard Circiut	1.1

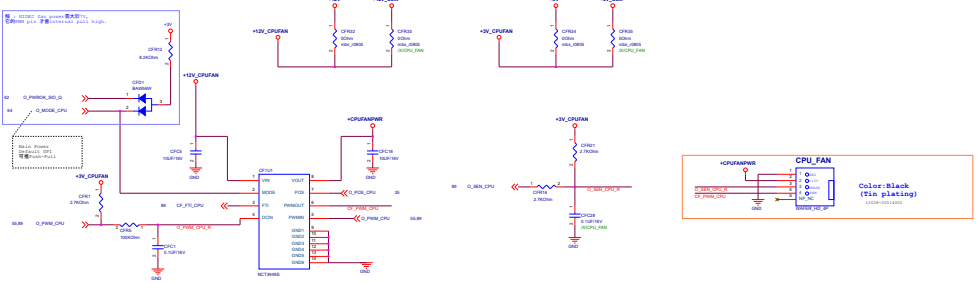
Date: Tuesday, July 24, 2018 Sheet 77 of 139

O_MODE_CPU	Mode
GPOH	PWM mode
GPOL	DC Mode
GPI (Floating) (Default)	Auto-detection

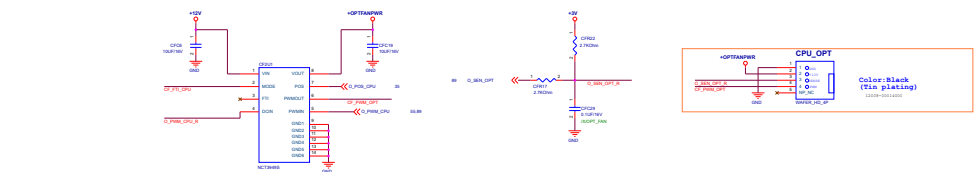
CF_FTI_CPU	Mode
H	PWM Mode
L	DC Mode

O_BOS_CPU (O_CPU_FANQUIET_CTRL)	Mode
GPI (H) (3949 internal pull-high)	PWMOUT follows PWMIN
GPOL	PWMOUT outputs 0V (extreme quite mode)

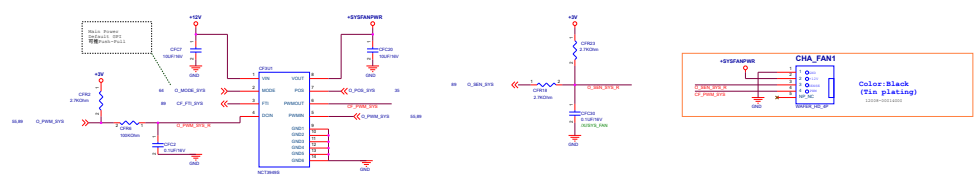
CPU_FAN



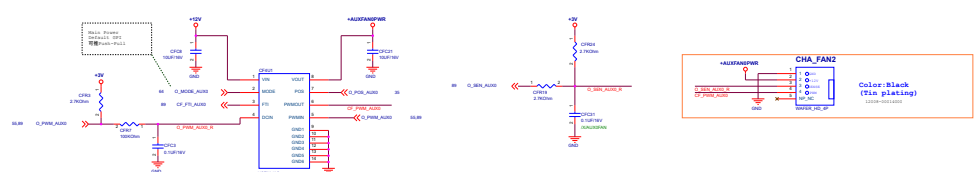
CPU_OPT FAN



CHA_FAN1

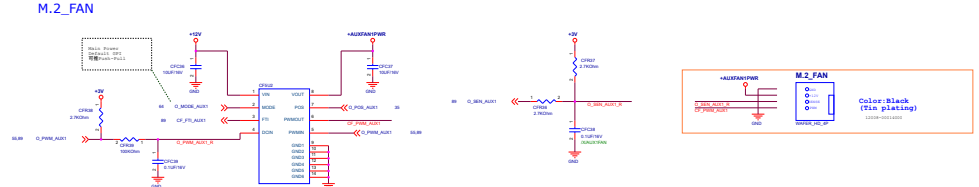


CHA_FAN2



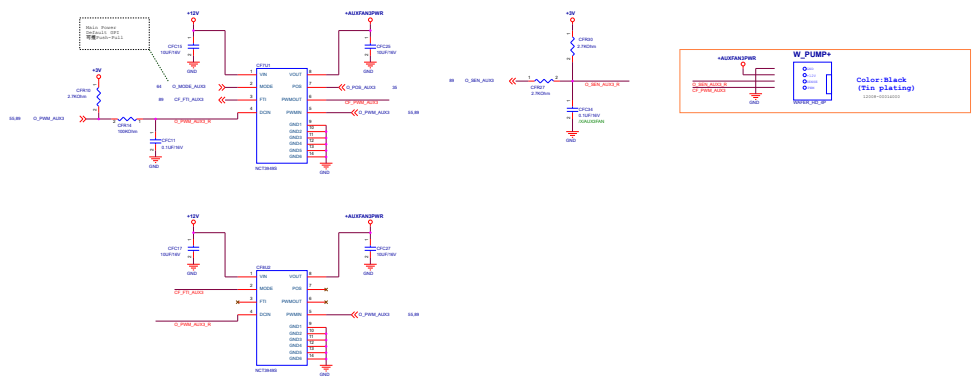
CHA_FAN3 / M.2_FAN 二擇一

M.2_FAN

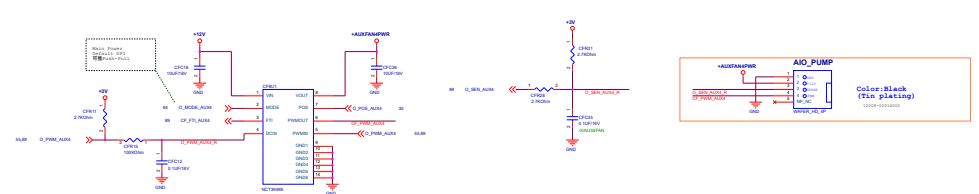


H_AMP FAN

W_PUMP+

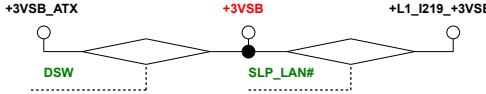


AIO_PUMP

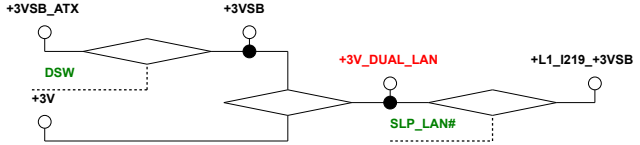


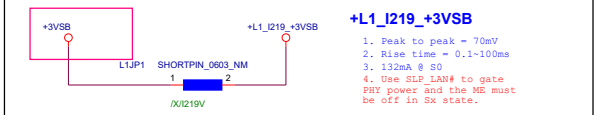
若platform只有一個LAN controller,可以直接使用+3VSB
power;若platform同時有兩個LAN controller,請改用+3V_DUAL power.

Single LAN Power Flow



DUAL LAN Power Flow





0.5E

PCIE IF

GbE can only be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13

L1_SMBCLK & L1_SMBDATA

Connect to PCH SML0DATA / GPP_C4 and SML0CLK / GPP_C3 and need to pull-up 499ohm resistors to at PCH +3VSB side.The PHY SMBus address is 0XC8

L1_LAN_DISABLE#

Connect to PCH LANPHYPC / GPD11 and LANPHYPC can only be driven low if SLP_LAN# is deasserted.

CLK_REQ_N

1. 需要與PCIE CLK為同一組
2. Pull up power well需要與PCH相同

Internal SVR

Maximum voltage ripple = 50mV
BW is 20MHz
110mA @ S0

L1_CTRLP

請注意灰框net為Switching power noise較大的地方
1. 所有訊號需距離灰框net至少30 mil
2. 所有訊號請勿reference誤power plane
3. 誤power net請reference GND plane並與其他GND切割,follow switching power phase的做法
4. L1L1元件中間請勿走線
5. L1_CTRLP長度勿超過100mil,越短越好

MDI differential impedance = 100ohmit15%
Maximum trace length = 8 inch

L1X1,L1C7,L1C8

Placement rule:
1.Place close to L1U1
2.Trace length <1inch

L1_LAN_WAKE# pull-up power well

請確認I219V 與 PCH LAN_WAKE# /GPD2 必須要同時有電同時沒電

L1_LAN_WAKE#

Must be connected to PCH LAN_WAKE# / GPD2

Table 20-4. Power Plane and States for Input Signals

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5	Deep Sx
LAN_WAKE# / GPD2	DSW	Undriven	Undriven	Undriven	Undriven/ Internal Pull-Down[2]

Notes:
1. Configurable
2. Configurable based on PMC configuration bit.
'1' (pin will be driven by platform in Deep Sx) -> Undriven;
'0' (pin will NOT be driven by platform in Deep Sx) -> Internal pull-down (15k-40k) enabled

Standard Circuit

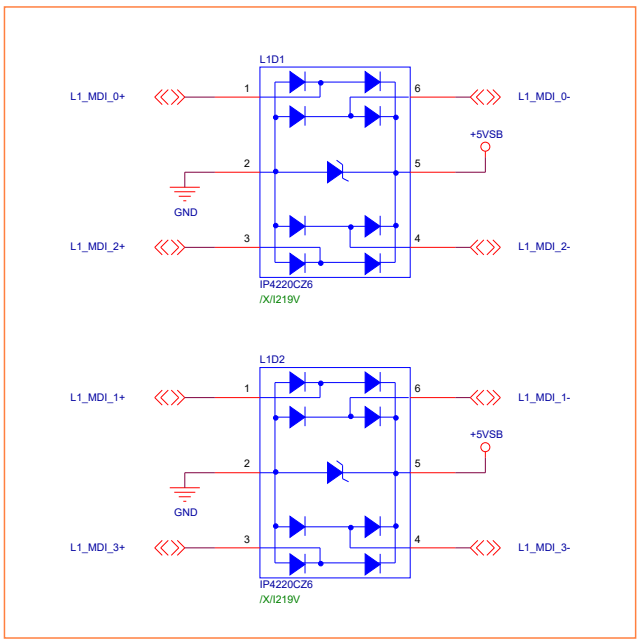
LAN	I219V
REV.	L1_0.5E

LAN_I219V

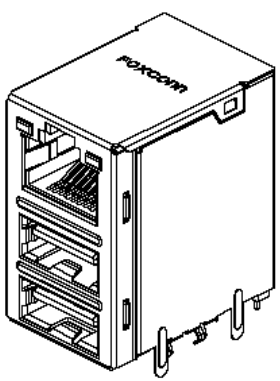
<Core Design>

Title :	I219V-1
Engineer:	Ben Hsieh
ASUSTek Computer Inc.	
Size: A3	Project Name: Standard Circiut
Rev: 0.5E	
Date: Tuesday, July 24, 2018	Sheet 3 of 4

MD0 and MD1 不共用 ESD part ,follow Intel 建議



Choose a proper LAN Connector in page Back I/O Connector

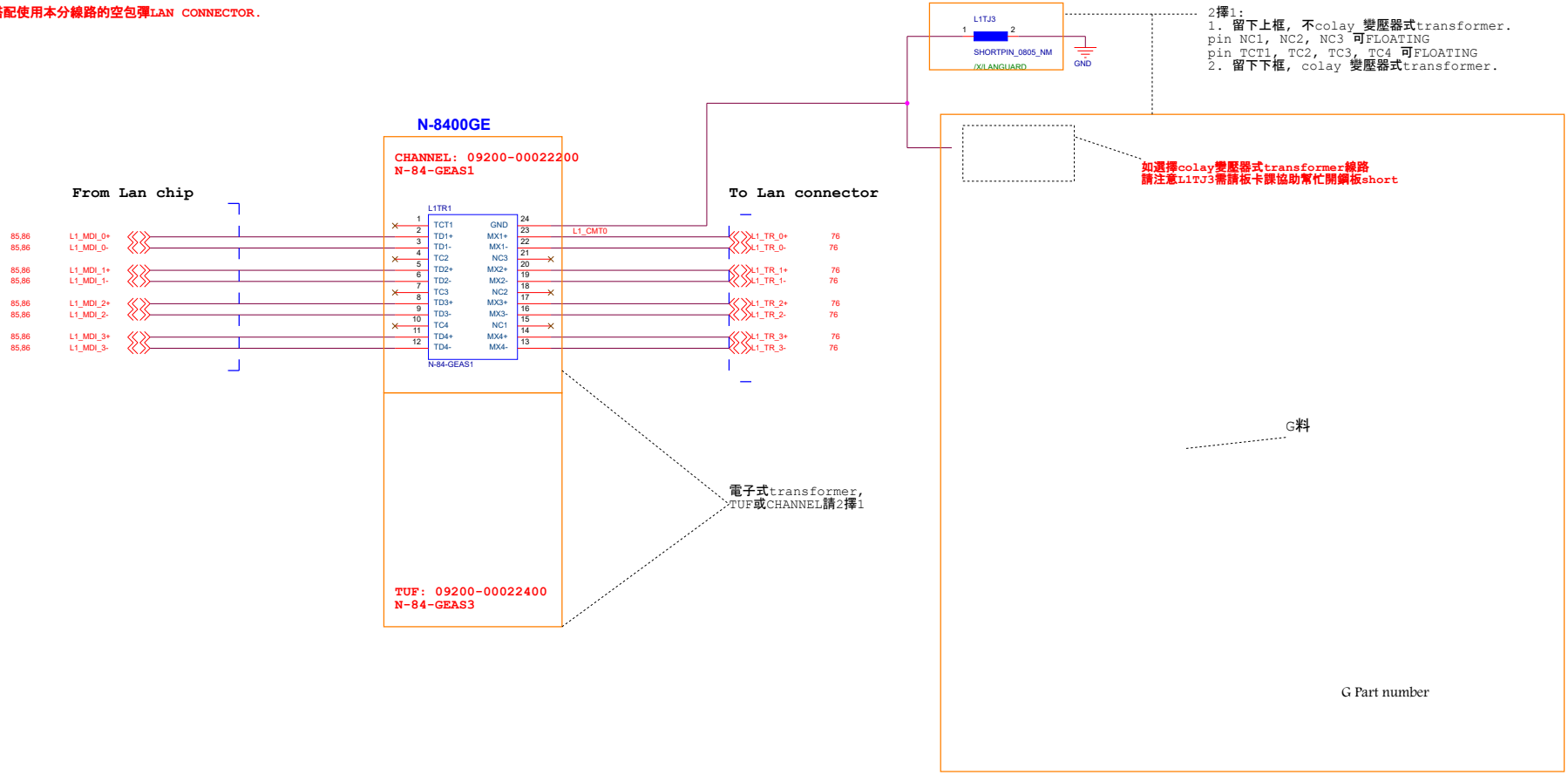


L1_ACTLEDP
L1_ACTLEDN
L1_GND
L1_MDI_3-
L1_MDI_3+
L1_MDI_2-
L1_MDI_2+
L1_MDI_1-
L1_MDI_1+
L1_MDI_0-
L1_MDI_0+
L1_LINK1000#
L1_LINK100#

<Variant Name>

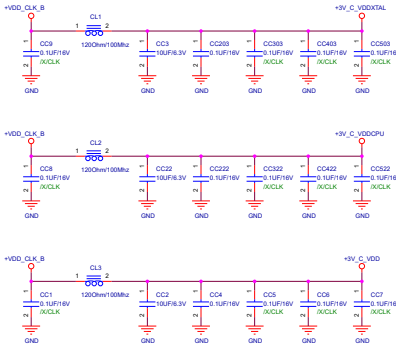
ASUSTek Computer Inc.	Title : I219V-2	
	Engineer: Scherzer Lu	
Size: A3	Project Name: Standard Circiut	Rev: 0.5B
Date: Tuesday, July 24, 2018	Sheet 86 of 129	

請務必搭配使用本分線路的空包彈LAN CONNECTOR.



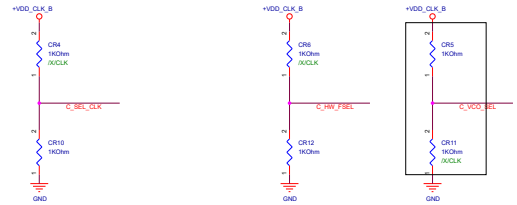
<Variant Name>

ASUSTek Computer Inc.	Title : TRANSFORMER1	
	Engineer: Ben Hsieh	
Size: A3	Project Name: Standard Circiut	Rev: 1.4
Date: Tuesday, July 24, 2018	Sheet 87 of 129	



H/W Strapping

PWR&PWRGD Ready後，1.8mS內會完成所有Latch H/W Strapping



SEL_CLK Function Select Table

SEL_CLK	X1/CLKIN	X2/CLKINB
0	X1	X2
1	CLKIN	CLKINB

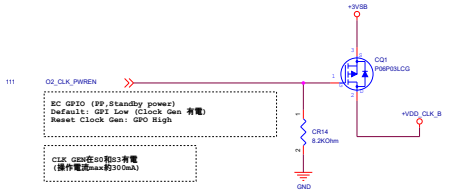
CPU Frequency Selection Table

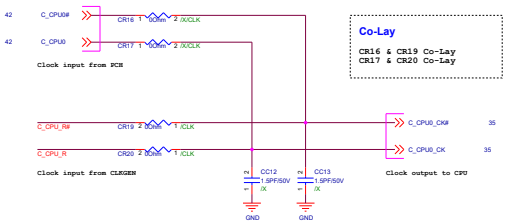
HW_FSEL	VCO_SEL	VCO(MHz)	CPU Divider	CPU(MHz)
0	0	400	4	100
0	1	1000	10	100
1	0	412	4	103
1	1	1030	10	103

*Default by hardware latch

Note:

橘紅框可改netname和tune 值
橘框可選option



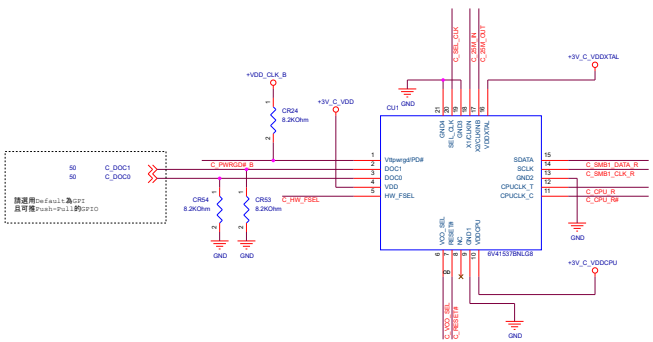


Co-Lay

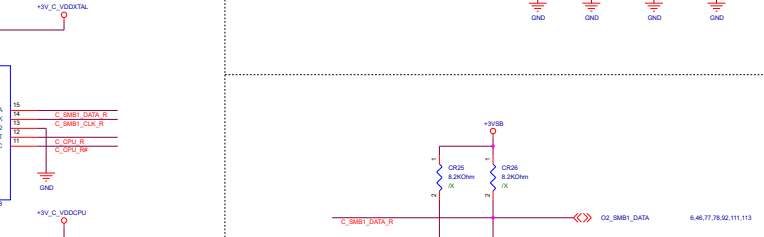
CR16 & CR19 Co-Lay
CR17 & CR20 Co-Lay

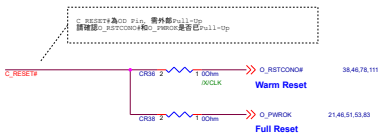
Sequency

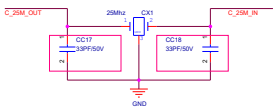
若需改由PCH提供Clock Input需額外考慮時序因素：
開機時序：+VDD_CLK_B → CLK Input → PWRGD
關機時序：PWRGD → CLK Input → +VDD_CLK_B



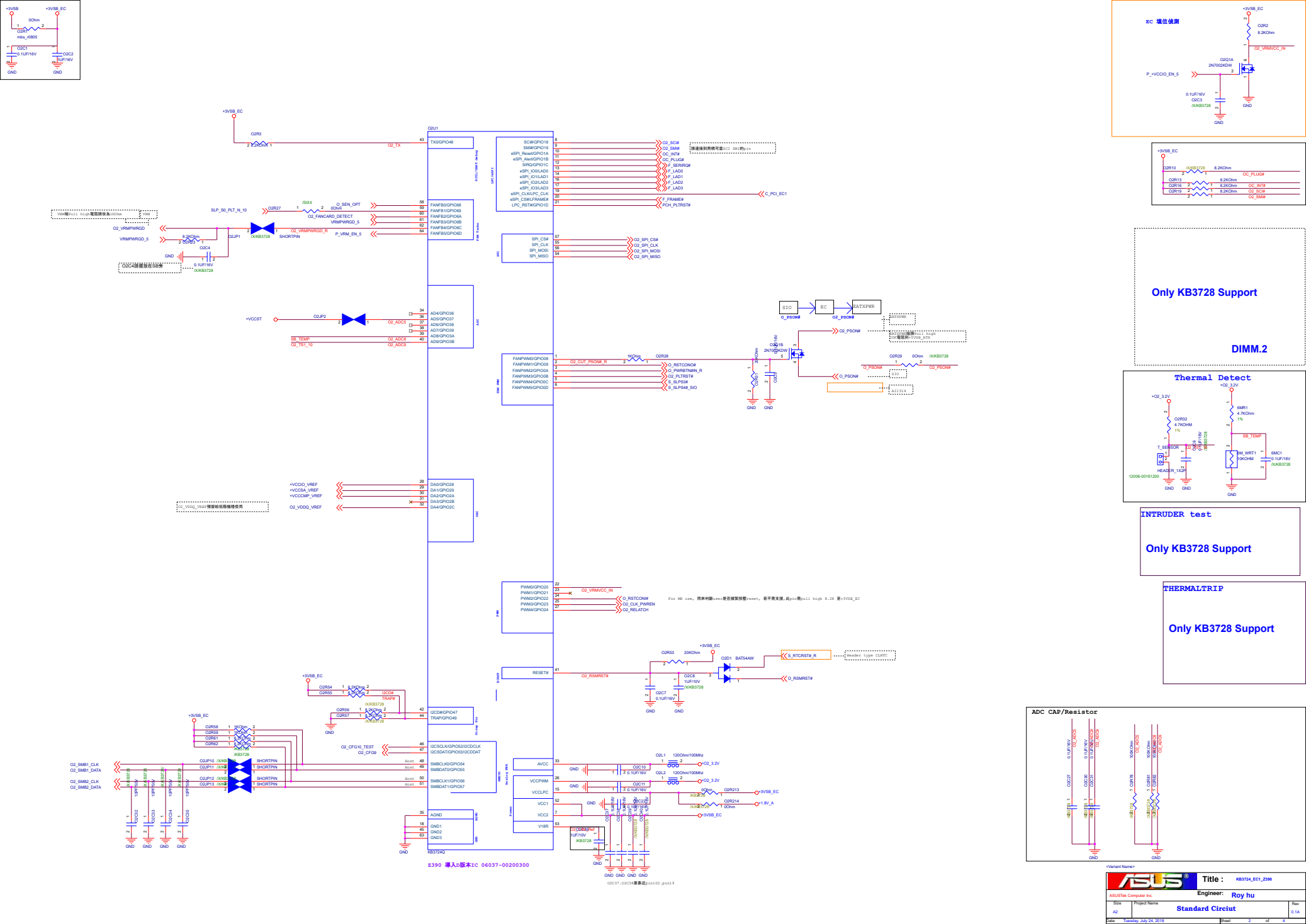
Device Slave Address: 0xD2

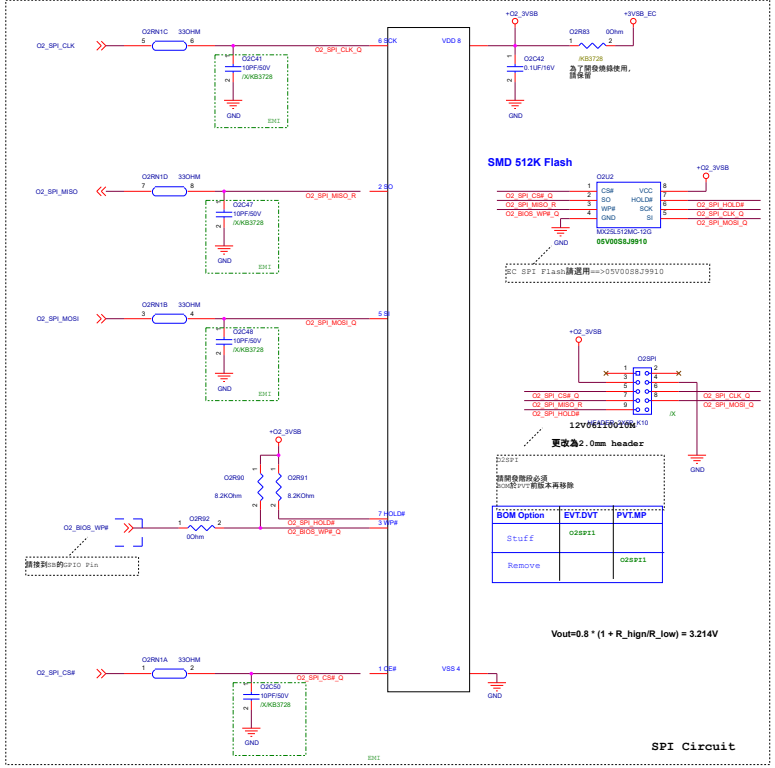


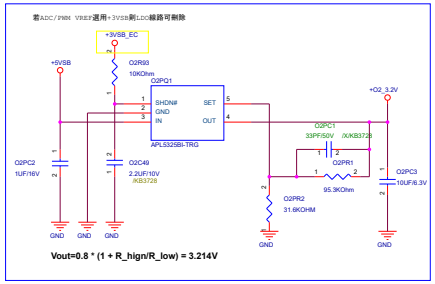


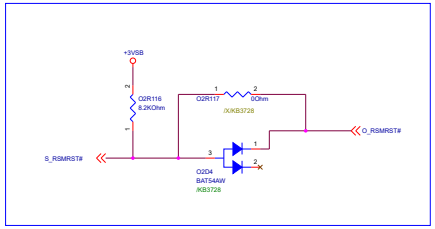


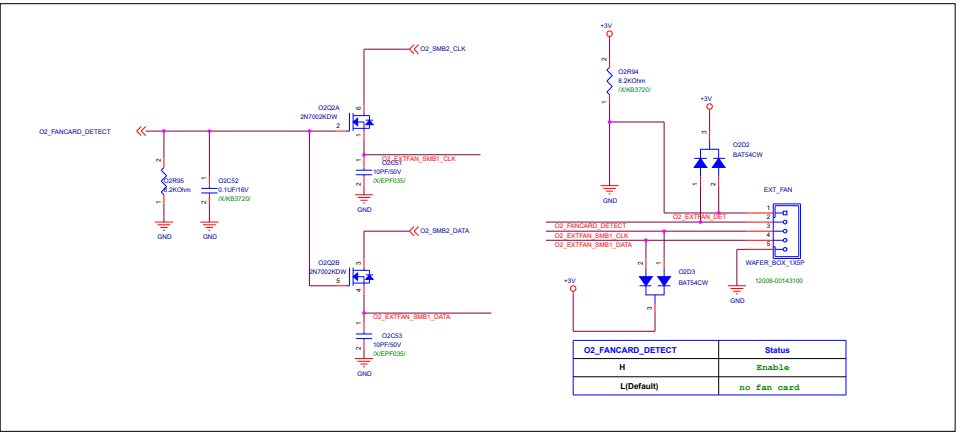
ASUSTeK Computer Inc.	Title :	CLKGEN_IDT6V41537	
	Engineer:	Scott2_Lin	
Size: A2	Project Name: KABYLAKE		Rev: 0.1B
Date: Tuesday, July 24, 2018	Sheet 115 of 123		

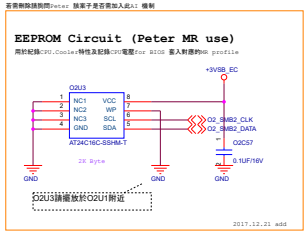

EC 填位偵測
Only KB3728 Support
DIMM.2
Thermal Detect
INTRUDER test
Only KB3728 Support
THERMALTRIP
Only KB3728 Support
ADC CAP/Resistor
Z390 導入D版本IC 06037-00200300
Title : KB3724_EC1_Z390
Engineer: Roy hu
Standard Circiut











<Variant Name>
ASUSTek Computer Inc.
Title : KB3724_EC1_Z390
Engineer: Roy hu
Size: A2
Project Name: Standard Circiut
Rev: 0.1A
Date: Tuesday, July 24, 2018
Sheet 3 of 4

僅一組Waterflow機種

Water Block(WB)一體式水冷

Only KB3728 Support

漏水偵測

Only KB3728 Support

<Variant Name>

Title : KB3724_EC1_Z390

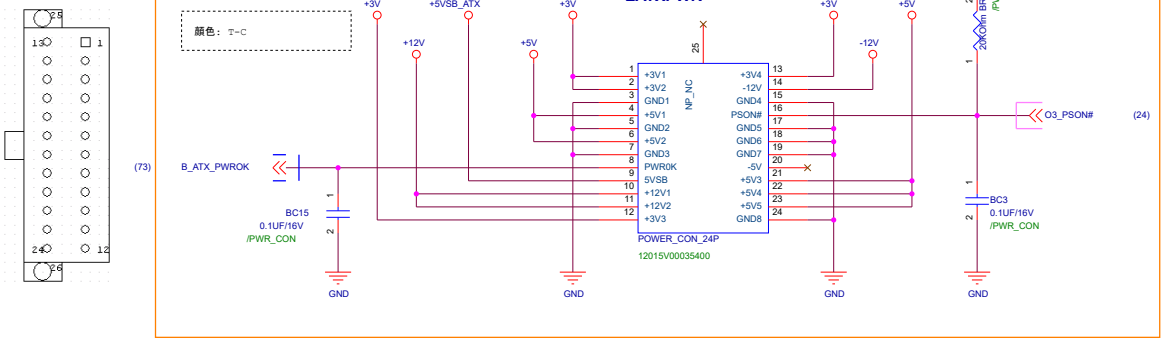
Engineer: Roy hu

ASUSTek Computer Inc.

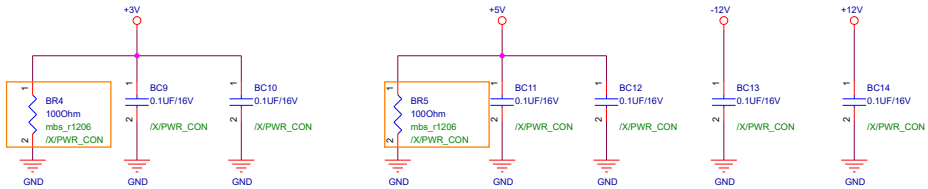
Size: A2 | Project Name: Standard Circiut | Rev: 0.1A

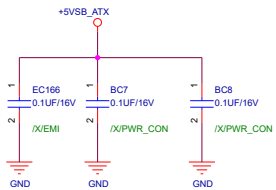
Date: Tuesday, July 24, 2018 | Sheet 4 of 4

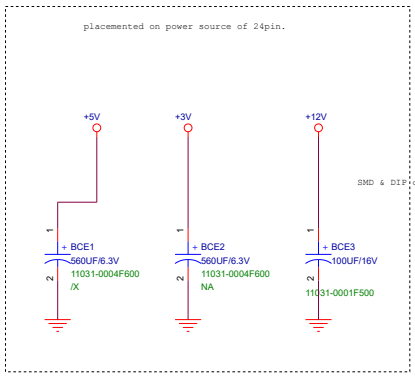
24 Pin ATX Connector



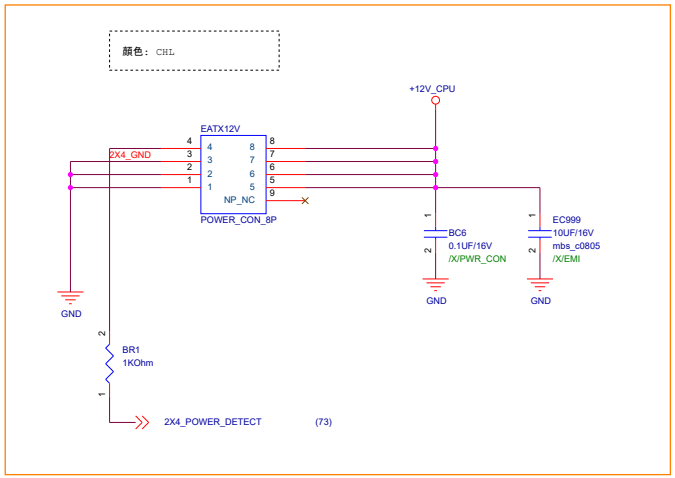
Bypass/EMI Capacitor





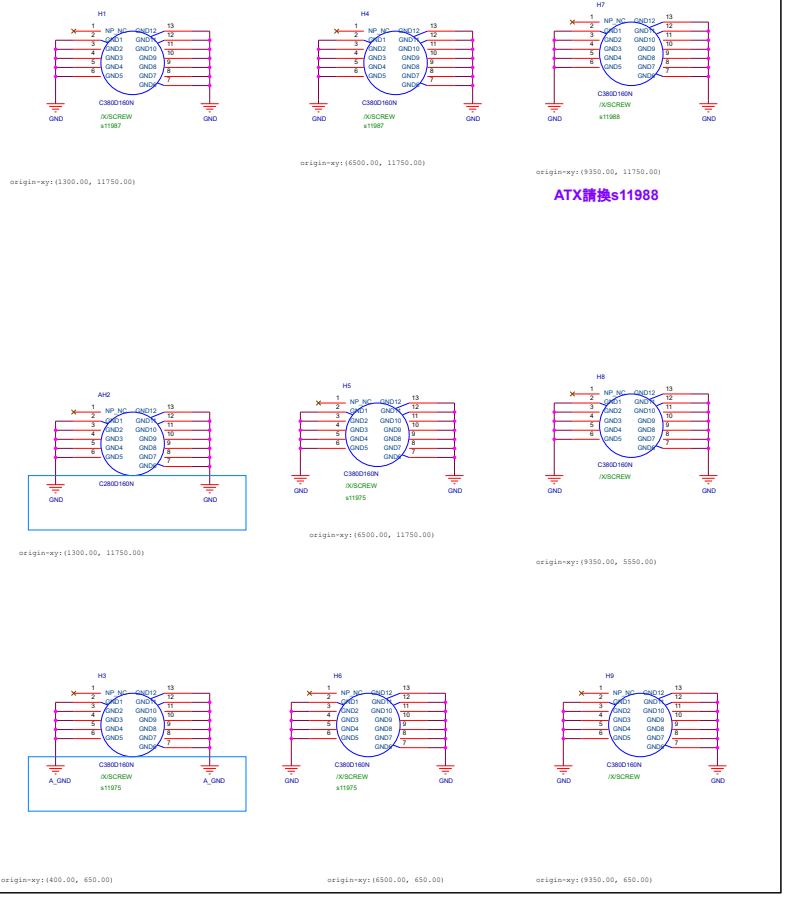


8 Pin +12V Connector



USED TO DETECT 2X4 PRESENCE

Screw Hole



ATX請換s11988

12 inch

(X,Y)=(0,0)

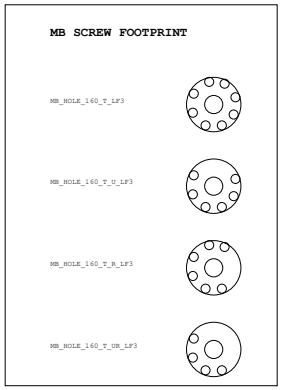
<9.6 inch

9.6 inch

Screw Select

	Standard (12 x 9.6)	scale down (12 x <9.6)
H1	V	V
H2	V	V
H3	V	V
H4	V	V
H5	V	V
H6	V	V
H7	V	X
H8	V	X
H9	V	X

MB SCREW FOOTPRINT



Fiducial Mask (光學點)

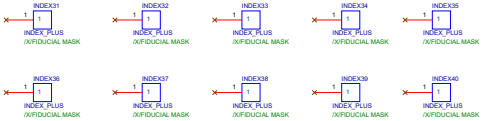
光學點需要10顆，
LayoutRD會依空間大小及版本需求
盡致所需的光學點
所以四種光學點都需畫入線路中，
最後再做刪除.

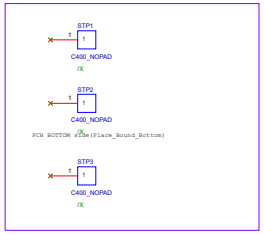
大顆光學點

小顆光學點

大顆十字光學點

小顆十字光學點





<Variant Name>

Title : ATX Screw Hole/Fiducial Mask

ASUS TeK Computer INC

Engineer: Ben Hsieh

Size	Project Name	Rev
A2	Standard Circuit	1.15

Date: Tuesday, July 24, 2018 Sheet 106 of 129

Standard Circuit	
BIOS	SPI
REV.	F1_0.5B

SPI /X/SPI_SMD

F1C8 close to Pin 8 VDD.

+F1_SPI_PWR

F1C8 0.1UF/16V

GND

92 F_SPI_CLK_R — F1R12 15Ohm — F_SPI_CLK_L — 6 SCK — VDD 8

92 F_SPI_MISO_R — F1R13 15Ohm — F_SPI_MISO_L — 2 SO

38,92 F_SPI_MOSI_R — F1R14 15Ohm — F_SPI_MOSI_L — 5 SI

+F1_SPI_PWR

F1R10 1KOhm

F1R11 1KOhm

42 F_SPI_IO3 — F1R5 15Ohm — F_SPI_HOLD# — 7 HOLD#

38,42 F_SPI_IO2 — F1R6 15Ohm — F_SPI_WP# — 3 WP#

F1R16 1.2KOhm 1% /X/SPI_SMD

F1R15 1.2KOhm 1% /X/SPI_SMD

GND GND

92 F_SPI_CS0#_R — 1 CE# — VSS 4

GND

+3V main power

+3VSB power

+3V_SPI

F1JP1 SHORTPIN /X/SPI_SMD

+3VSB +3V_SPI

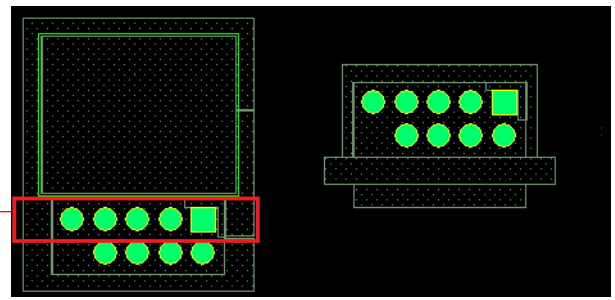
F1D2 BAT54CW

F1R20 0Ohm /X/SPI_SMD

Using
+3VSB,
+3V,
+1.8VSB,
+1.8V
depends on project spec.

12V06110010M for 水平插入SPI CARD
mbs_hd_2x5p_79_k10_pin_lf3

12006V00023300 for 垂直插入SPI CARD
mbs_hd_2x5p_79_k10_ls_lf3



5-Pin 這一面靠近SMD BIOS.
使Header限制區剛好在SMD BIOS上方.

SMT FLASH

+F1_SPI_PWR

F1U1

F_SPI_CS0#_R	1 CS#	VCC 8	+F1_SPI_PWR
F_SPI_MISO_L	2 DO(IO1)	HOLD#/RESET(IO3) 7	F_SPI_HOLD#
F_SPI_WP#	3 WP#(IO2)	CLK 6	F_SPI_CLK_L
	4 GND	DI(IO0) 5	F_SPI_MOSI_L

W25Q128FVSIQ

GND

KABALAKE:
05006-00090400 128M SPI
05006-00091900 128M SPI
AMD:
05006-00092200 128M SPI
05006-00092400 128M SPI

CS1 no need for single BIOS

+F1_SPI_PWR

SPI

F_SPI_WP# F_SPI_CS0#_R F_SPI_MISO_L F_SPI_HOLD# F_SPI_CLK_L F_SPI_MOSI_L

HEADER_2X5P_K10

GND

12V06110010M

SPI Flash Header Pin Define

HOLD#	SO	CS0#	VCC	NC for single BIOS CS1# for dual BIOS
9	7	5	3	1
8	6	4	2	
SI	CLK	GND	WP#	

2x5 Pin Header
12006-00021100
12G06110010M

<Variant Name>

ASUSTek COMPUTER INC.

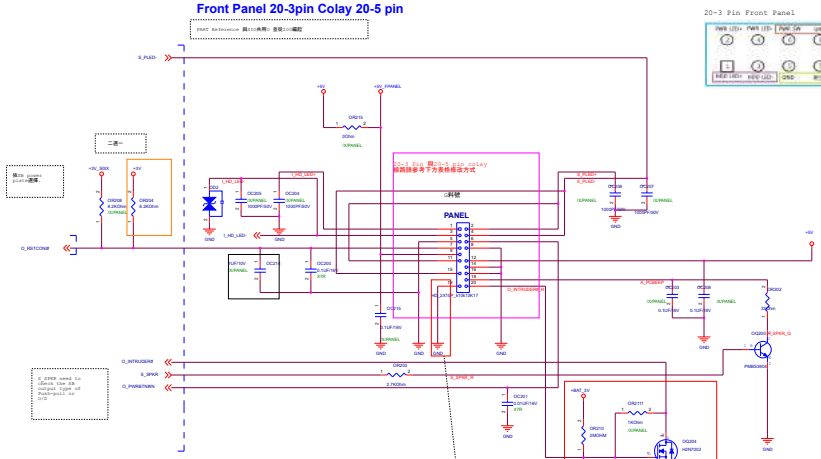
Title : SINGLE BIOS_SPI SMD-1

Engineer: Eagle Liu

Size	Project Name	Rev
A3	Standard Circuit	0.5B

Date: Tuesday, July 24, 2018 Sheet 104 of 129

Front Panel 20-3pin Colay 20-5 pin

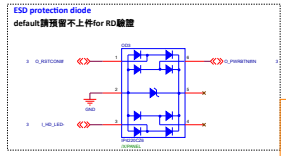


Chassis intruder support	Footprint P/N	實際上料 Front Panel P/N	BOM option
支援	20-3 Pin 12006-00201700	20-3 Pin 12006-00201700	紅框內線路全上件
不支援 (預留不上)	20-3 Pin 12006-00201700	20-5 Pin 12006-00202000	紅框內線路為 X 預留不上
不支援	20-5 Pin 12006-00202000	20-5 Pin 12006-00202000	移除紅框內線路

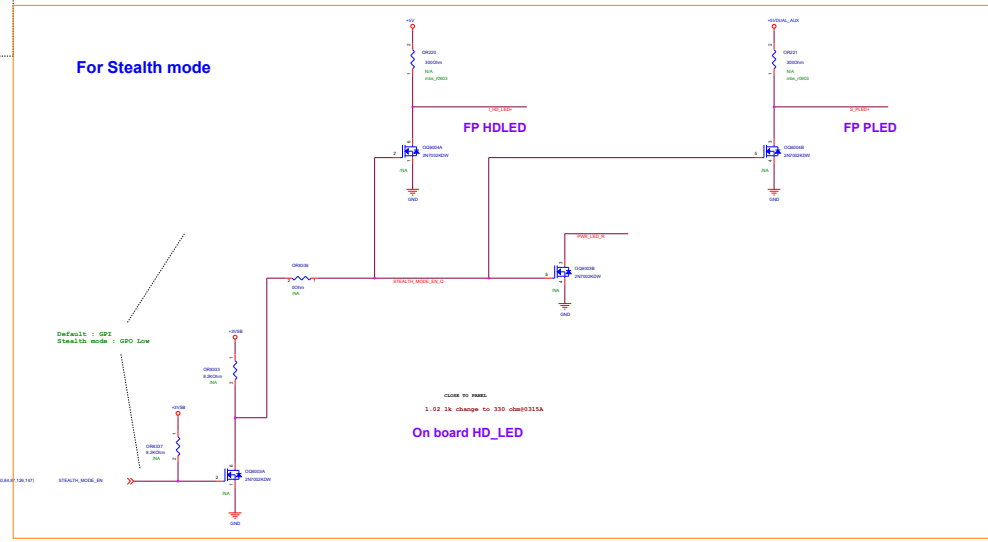
20-3 Pin Front Panel

20-5 Pin Front Panel

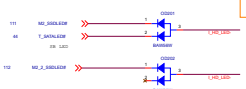
ESD protection diode
default請預留不上件for RD驗證



For Stealth mode

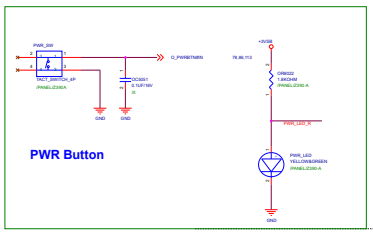


HD_LED

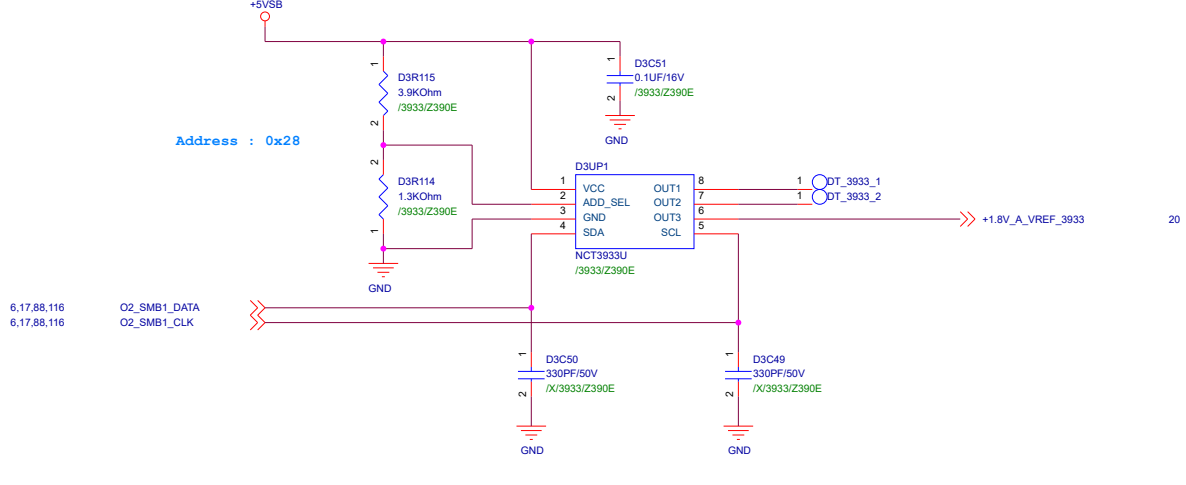


RST Button

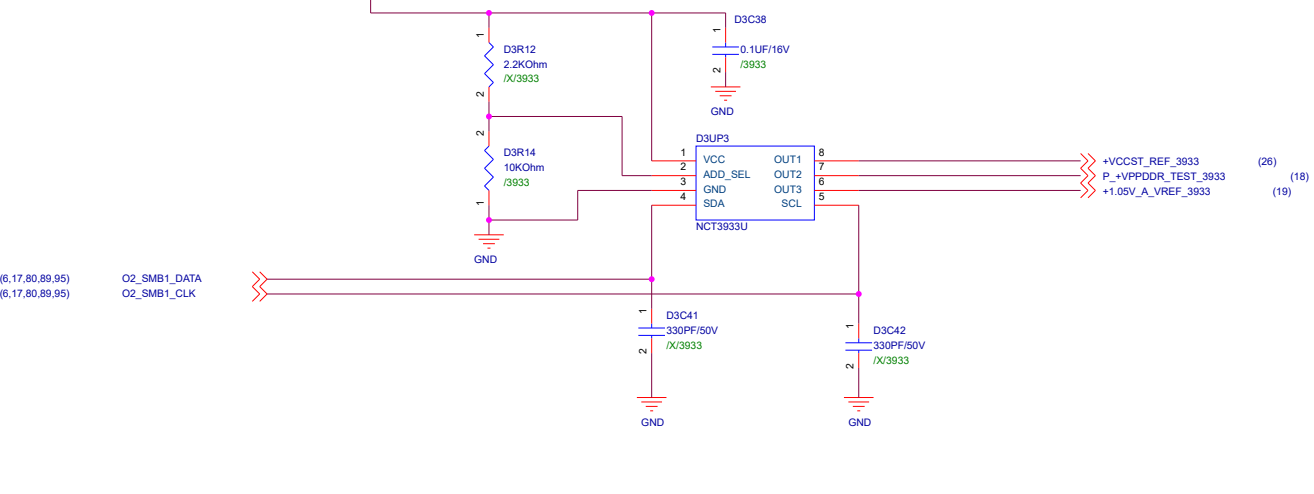
PWR Button



Title :	Panel&HotStart		
Engineer:	Ben Hsieh		
Size: A2	Project Name: Standard Circuit		Rev: 1.15
Date: Tuesday, July 24, 2018	Sheet 4 of 7		



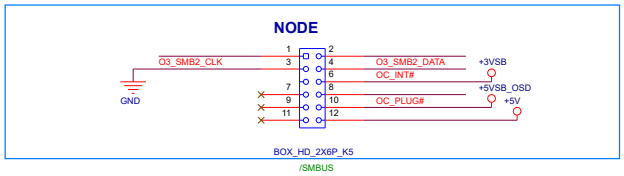
Address : 0x2A



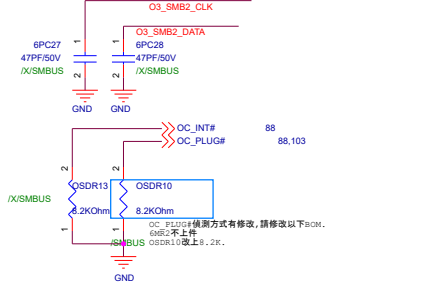
<Variant Name>

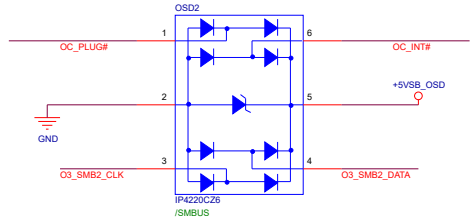
ASUSTek COMPUTER INC.	Title : NCT3933	
	Engineer: Aaron_Su	
Size: A3	Project Name: Z390 Golden board	Rev: R1.02A
Date: Tuesday, July 24, 2018	Sheet 89 of 139	

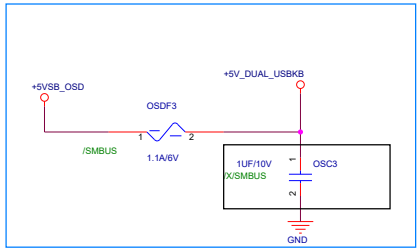
M8E 1.01@20150308:(Stanley)5VSB短路的話,M8版端的poly 1.6A/6V並不會跳開保護.
OSDF3更換為(建議使用替代料: 07G01411041L)



Add兩個獨立connector(9/25)





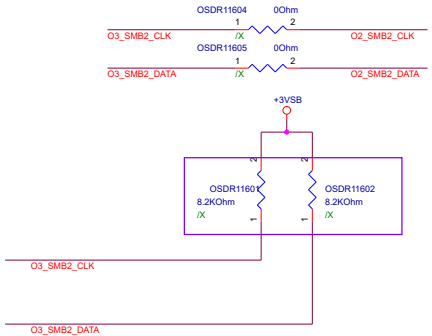


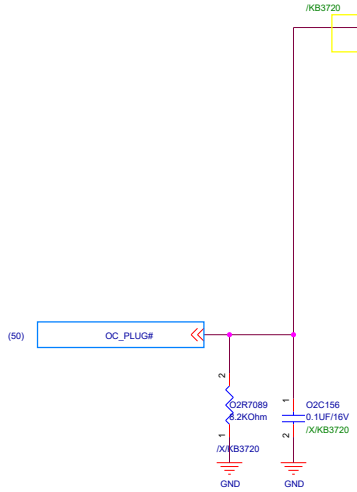
2015.03.23 OSDF3 Change to 1.1A

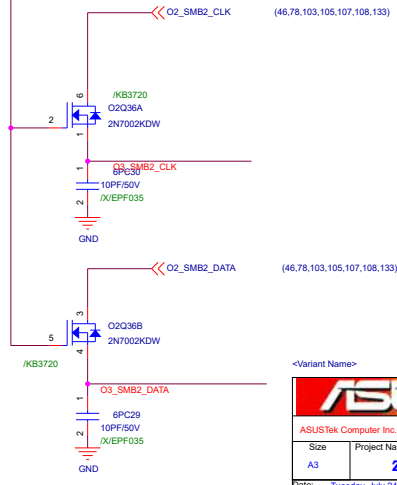
2015.03.23 Change ROG_EXT part.

M6E 1.01@1209:C_PANEL_X申請Symbol 只留文字面
料號：temp_TX15127_0002
PCB Footprint：hd_2x9p_100_k17_nopad(新建)

OC_PANEL_X
定位用,不上件







<Variant Name>

ASUSTek Computer Inc.	Title : OC_PANEL	
	Engineer: Aaron_Su	
Size: A3	Project Name: Z390 golden board	Rev: 1.2
Date: Tuesday, July 24, 2018	Sheet 103 of 129	

Thermal Pad

M2_M_HOLD_80 — TC217BC176D146 — GND

M2_M_HOLD_60 — TC217BC176D146 — GND

M2_M_HOLD_42 — TC217BC176D146 — GND

M.2_1(SOCKET3)

+3V_S0IX

XC17 0.01UF/16V /X/M.2 — XC16 0.01UF/16V /X/M.2 — XC15 0.1UF/16V — XC22 10UF/6.3V mbs_c0805

C CLOSE TO M.2(SOCKET3) pin 2 , 4

GND

M2_LED-

XC20 0.01UF/16V /X/M.2 — XC19 0.1UF/16V /X/M.2 — XC21 10UF/6.3V mbs_c0805

C CLOSE TO M.2(SOCKET3) pin 12, 14, 16 , 18

GND

+3V_S0IX

XR16 2 /M.2 1 8.2KOhm

46 M2_DEVSLP1

M2JP1 SHORTPIN /X/M.2

54,112 O_PCIRST#_PCIEX16_3_CEC

47 CLK_REQ7_M.2_1_SSD#

45,58,59,60,61,112 X_WAKE#

M2_PE_RST#

Require No Stub

45,108,112 PCH_SUSCLK — XR46 33Ohm /X/M.2 — M2_M_SUSCLK

XC13 0.01UF/16V /X/M.2 — XC12 0.01UF/16V /X/M.2 — XC11 0.1UF/16V — XC10 10UF/6.3V mbs_c0805

C CLOSE TO M2_TYPE_M pin 70, 72, 74

GND

MINI_PCI_75P

XR40 1 100Ohm 2 1%

PCH_M2_1_CONFIG3/PRESENT# 50

PE_M2_RXN3 44 / PE_M2_RXP3 44

XC9 X5R 0.22UF/10V — PE_M2_TXN3_C — XC8 0.22UF/10V X5R — PE_M2_TXP3_C

PE_M2_TXN3 44 / PE_M2_TXP3 44

PE_M2_RXN2 44 / PE_M2_RXP2 44

XC7 X5R 0.22UF/10V — PE_M2_TXN2_C — XC6 0.22UF/10V X5R — PE_M2_TXP2_C

PE_M2_TXN2 44 / PE_M2_TXP2 44

PE_M2_RXN1 44 / PE_M2_RXP1 44

XC5 X5R 0.22UF/10V — PE_M2_TXN1_C — XC4 0.22UF/10V X5R — PE_M2_TXP1_C

PE_M2_TXN1 44 / PE_M2_TXP1 44

PE_M2_RXP0/SA 44 / PE_M2_RXN0/SA 44

XC3 X5R 0.22UF/10V — PE_M2_TXN0_C — XC2 0.22UF/10V X5R — PE_M2_TXP0_C

PE_M2_TXN0/SA 44 / PE_M2_TXP0/SA 44

C_PCIE_M2_1# 47 / C_PCIE_M2_1 47

M.2_1_SSD_SATA_PEDET#

GND

M2_CONFIG3/PRESENT#	
0	M.2 Present
1	M.2 Unplug

+3V_S0IX — XR17 8.2KOhm — PCH_M2_1_CONFIG3/PRESENT#

M2_CONFIG0/WWAN_SSD# M2_CONFIG2/WWAN_SSD#	
0	SATA & PCIE
1	HYPERKIT

+5V — XR14 8.2KOhm mbs_r0603 — M2_SSDLED# 101

+3V — XQ49 H2N7002 — M2_LED-

+3V_S0IX — XR711 8.2KOhm — XJP1 SHORTPIN_0603_NM /X/M.2_2

M.2_1_SSD_SATA_PEDET# — PCH_M.2_1_SSD_SATA_PEDET# 50

M.2_1_SSD_PEDET	
0	M.2 SATA Mode
1	M.2 PCIe Mode

PCIE and SATA Mode

P8Z77-V DELUXE R1.00

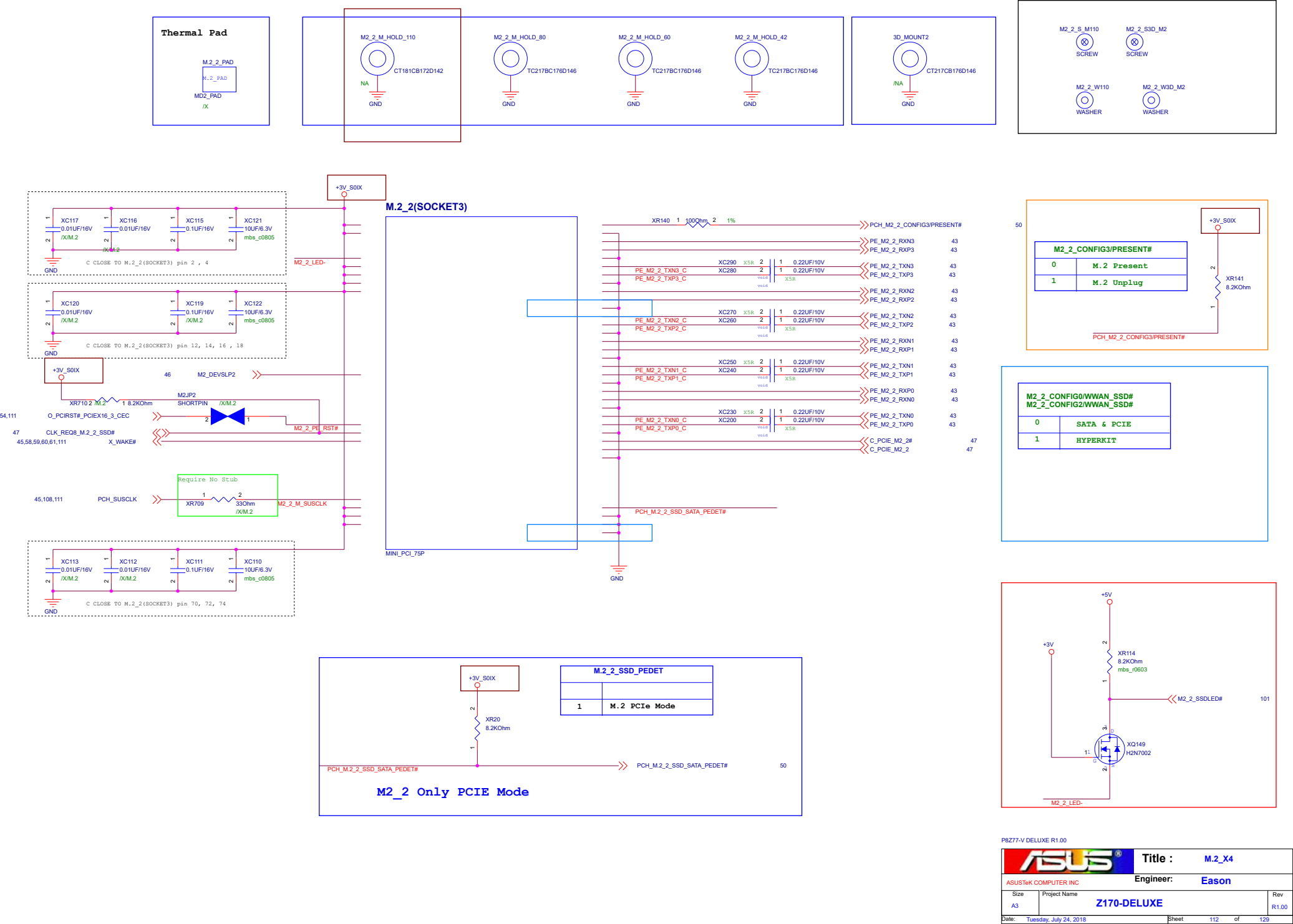
ASUSTeK COMPUTER INC

Title : M.2_X4

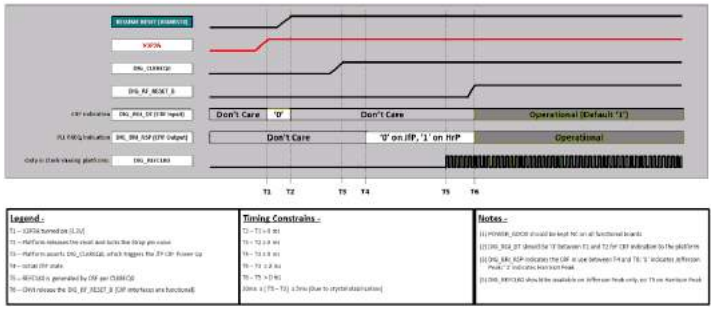
Engineer: Eason

Size	Project Name	Rev
A3	Z170-DELUXE	R1.00

Date: Tuesday, July 24, 2018 Sheet 111 of 129


Thermal Pad
M.2_PAD
M2_2_PAD
M.2_PAD
MD2_PAD
/X
M2_2_M_HOLD_110
CT181CB172D142
NA
GND
M2_2_M_HOLD_80
TC217BC176D146
GND
M2_2_M_HOLD_60
TC217BC176D146
GND
M2_2_M_HOLD_42
TC217BC176D146
GND
3D_MOUNT2
CT217CB176D146
/NA
GND
M2_2_S_M110
SCREW
M2_2_S3D_M2
SCREW
M2_2_W110
WASHER
M2_2_W3D_M2
WASHER
+3V_S0IX
M.2_2(SOCKET3)
XC117 0.01UF/16V /X/M.2
XC116 0.01UF/16V /X/M.2
XC115 0.1UF/16V /X/M.2
XC121 10UF/6.3V mbs_c0805
C CLOSE TO M.2_2(SOCKET3) pin 2 , 4
GND
M2_2_LED-
XC120 0.01UF/16V /X/M.2
XC119 0.1UF/16V /X/M.2
XC122 10UF/6.3V mbs_c0805
C CLOSE TO M.2_2(SOCKET3) pin 12, 14, 16 , 18
GND
+3V_S0IX
46 M2_DEVSLP2
XR710 2 /M.2 1 8.2KOhm
M2JP2
SHORTPIN /X/M.2
54,111 O_PCIRST#_PCIEX16_3_CEC
M2_2_PE_RST#
47 CLK_REQ8_M.2_2_SSD#
45,58,59,60,61,111 X_WAKE#
Require No Stub
45,108,111 PCH_SUSCLK
XR709 1 2 33Ohm /X/M.2
M2_2_M_SUSCLK
XC113 0.01UF/16V /X/M.2
XC112 0.01UF/16V /X/M.2
XC111 0.1UF/16V /X/M.2
XC110 10UF/6.3V mbs_c0805
C CLOSE TO M.2_2(SOCKET3) pin 70, 72, 74
GND
MINI_PCI_75P
XR140 1 100Ohm 2 1%
PCH_M2_2_CONFIG3/PRESENT#
PE_M2_2_RXN3 43
PE_M2_2_RXP3 43
XC290 X5R 0.22UF/10V
XC280 0.22UF/10V
PE_M2_2_TXN3_C
PE_M2_2_TXP3_C
PE_M2_2_TXN3 43
PE_M2_2_TXP3 43
PE_M2_2_RXN2 43
PE_M2_2_RXP2 43
XC270 X5R 0.22UF/10V
XC260 0.22UF/10V
PE_M2_2_TXN2_C
PE_M2_2_TXP2_C
PE_M2_2_TXN2 43
PE_M2_2_TXP2 43
PE_M2_2_RXN1 43
PE_M2_2_RXP1 43
XC250 X5R 0.22UF/10V
XC240 0.22UF/10V
PE_M2_2_TXN1_C
PE_M2_2_TXP1_C
PE_M2_2_TXN1 43
PE_M2_2_TXP1 43
PE_M2_2_RXP0 43
PE_M2_2_RXN0 43
XC230 X5R 0.22UF/10V
XC200 0.22UF/10V
PE_M2_2_TXN0_C
PE_M2_2_TXP0_C
PE_M2_2_TXN0 43
PE_M2_2_TXP0 43
C_PCIE_M2_2# 47
C_PCIE_M2_2 47
PCH_M.2_2_SSD_SATA_PEDET#
GND
50
M2_2_CONFIG3/PRESENT#
0 M.2 Present
1 M.2 Unplug
+3V_S0IX
XR141 8.2KOhm
PCH_M2_2_CONFIG3/PRESENT#
M2_2_CONFIG0/WWAN_SSD#
M2_2_CONFIG2/WWAN_SSD#
0 SATA & PCIE
1 HYPERKIT
+3V_S0IX
M2_2_SSD_PEDET
1 M.2 PCIe Mode
XR20 8.2KOhm
PCH_M.2_2_SSD_SATA_PEDET#
PCH_M.2_2_SSD_SATA_PEDET# 50
M2_2 Only PCIE Mode
+5V
+3V
XR114 8.2KOhm mbs_r0603
M2_2_SSDLED# 101
XQ149 H2N7002
M2_2_LED-
P8Z77-V DELUXE R1.00
Title : M.2_X4
ASUSTeK COMPUTER INC
Engineer: Eason
Size A3
Project Name Z170-DELUXE
Rev R1.00
Date: Tuesday, July 24, 2018
Sheet 112 of 129

請注意所選用的PWR rail需follow CNVI sequence需求，+3VSB_WIFI_BT2需ready後，RSMRST#才能ready



Legend -

T1 – XDP26 turned on (1.2V)

T2 – Platform releases the reset and locks the strap pin value

T3 – Platform asserts DIG_CLKREQB, which triggers the ZP CRF Power Up

T4 – Initial CRF state

T5 – RSTCLKO is generated by CRF per CLKREQB

T6 – CNVi releases the DIG_RF_RESET_B (CRF interfaces are functional)

Timing Constrains -

T2 – T1 = 0 ms

T3 – T2 ≥ 0 ms

T4 – T3 ≥ 0 ms

T5 – T3 ≥ 0 ms

T5 – T4 = 0 ms

30ms ≤ (T5 – T2) ≤ 5ms (Due to crystal stabilization)

Notes -

(1) POWER_GOOD should be kept ‘hi’ on all functional boards

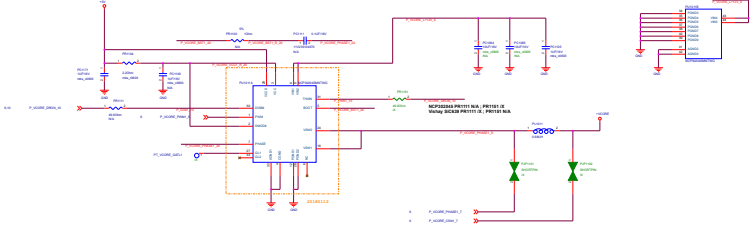
(2) CNV_RGI_DT should be ‘0’ between T1 and T2 for CRF indication to the platform

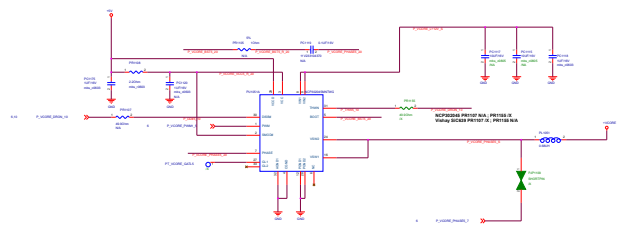
(3) CNV_BRI_RSP indicates the CRF in use between T4 and T6. ‘1’ indicates Jefferson Peak; ‘2’ indicates Harrison Peak

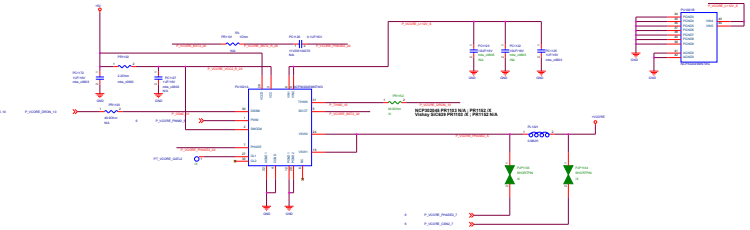
(4) CNV_RSTCLKO should be available on Jefferson Peak only, on T5 on Harrison Peak

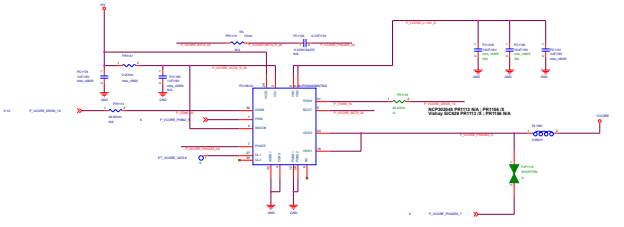
<Variant Name>

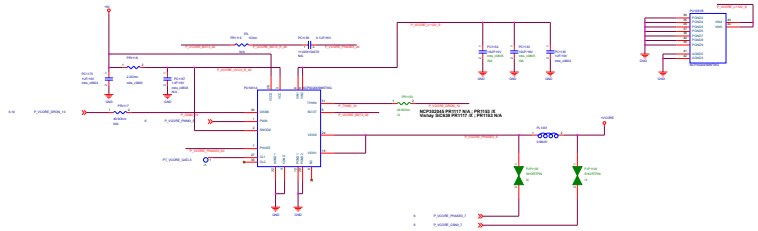
ASUSTeK COMPUTER INC	Title :	intel_CNVi
	Engineer:	Ben Hsieh
Size: A2	Project Name: Standard Circuit	Rev: 0.5F
Date: Tuesday, July 24, 2018	Sheet 3 of 3	

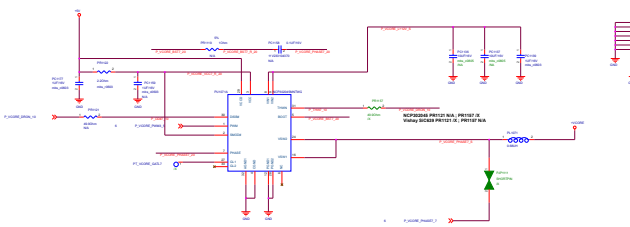




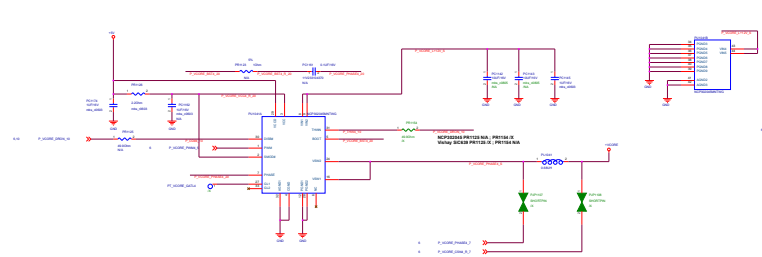


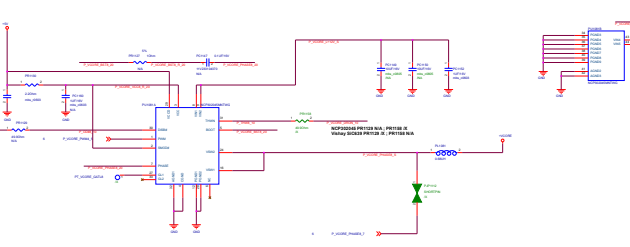






20170420 remove +VSD name
20180711 L82 mode remove +VSD
20180814 Add +VSD





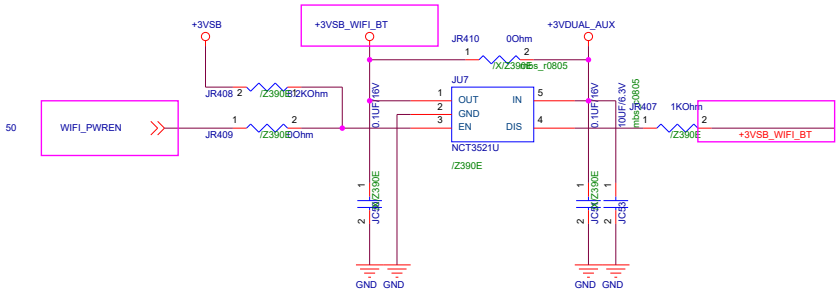
Water Vias 8 X16 Combination

Ripple = 4.75/0.1A (Vcore=1.52V, fs=115K)
set use 3.9A*3PCS=11.7A/4.5PCS = 13.24A

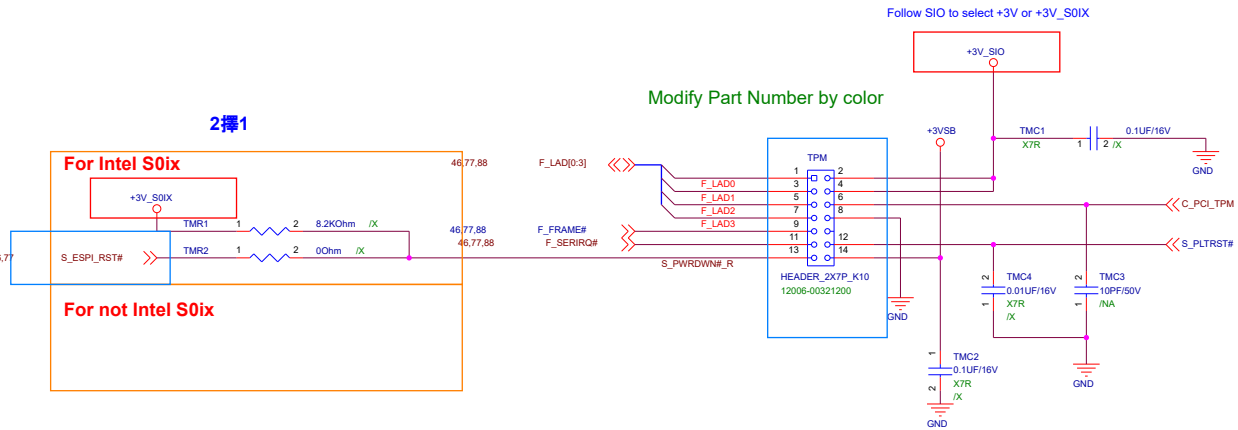
20180117 change 0603

Title :	VCORE DRIVER		
Size:	Document Number:		Rev:
Date:	Sheet of		
File:	C:\Users\...\VCORE_DRIVER.SchDoc	Drawn By:	

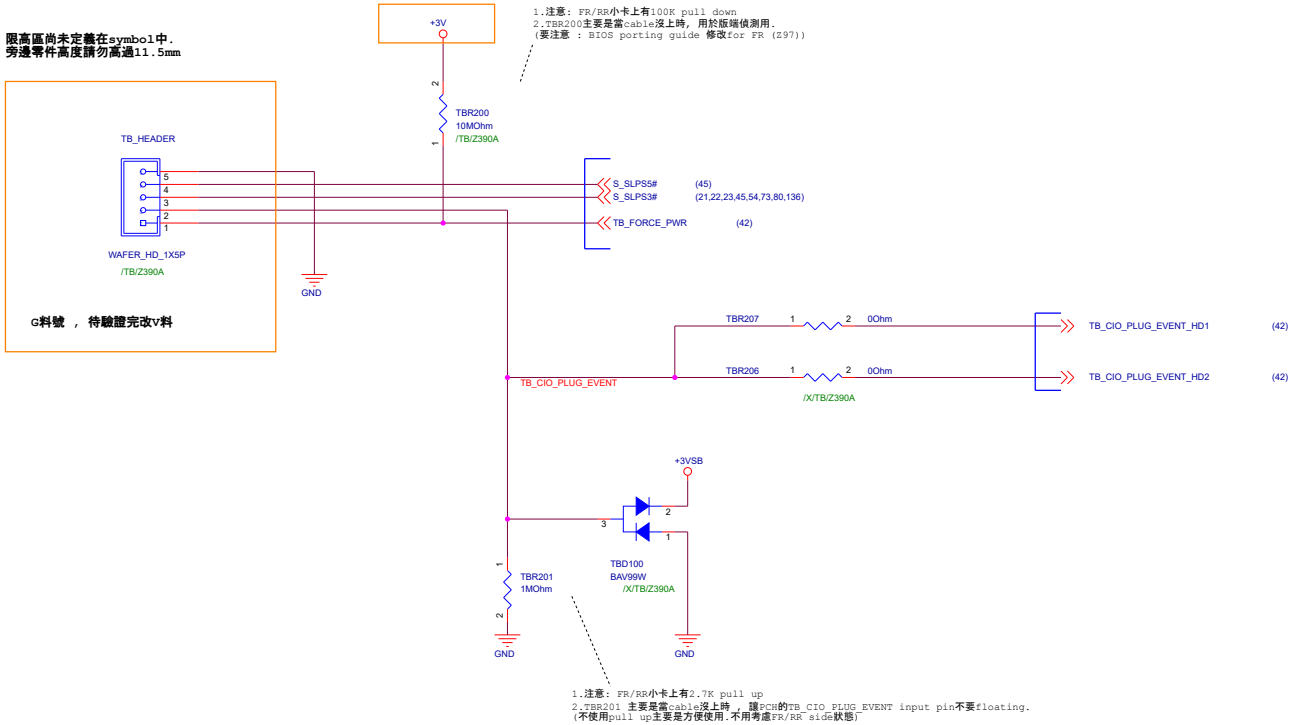
WIFI


+3VSB
+3VSB_WIFI_BT
+3VDUAL_AUX
JR410 0Ohm
/X/Z390E_r0805
JR408 2 /Z390E 2KOhm
JU7
OUT IN
GND
EN DIS
NCT3521U
/Z390E
0.1UF/16V
10UF/6.3V
m/s/Z0805
JR407 1KOhm
/Z390E
50
WIFI_PWREN
JR409 /Z390E 0Ohm
+3VSB_WIFI_BT
JC54 /Z390E
JC53
GND GND GND GND

2x7 Pin TPM Header



BOM	TPM Header	Onboard TPM
N/A	mount	mount
/X	unmount	unmount
/TPM HEADER	mount	unmount
/TPM IC	unmount	mount



NOTE:

TB_Header	TB	SIO 6791D mapping	Function
Pin1	TB_FORCE_PWR	GP11	1.Security level setting 2.TBR200 for 當沒插cable時用於detect 為High level 沒插device . for BIOS detect TBT AIC 用.

TB_Header	TB	Z97 / X99 PCH mapping	Function
Pin2	TB_CIO_PLUG_EVENT	connector to GPIO11 and GPIO0 . 請使用0 ohm for option , default option is GPIO0	Hot plug event
Pin3	S_SLPS3#	connect to PCH SLP_S3#	Sx Entry/Exit Flow for RR/FR Host
Pin4	S_SLPS5#	connect to PCH SLP_S5#	for +TB_VCC3V3 power enable /disable
Pin5	GND	N/A	1.GND 2.For AIC卡與TB Header接上時將AIC 上 Warning LED#拉掉

<Variant Name>

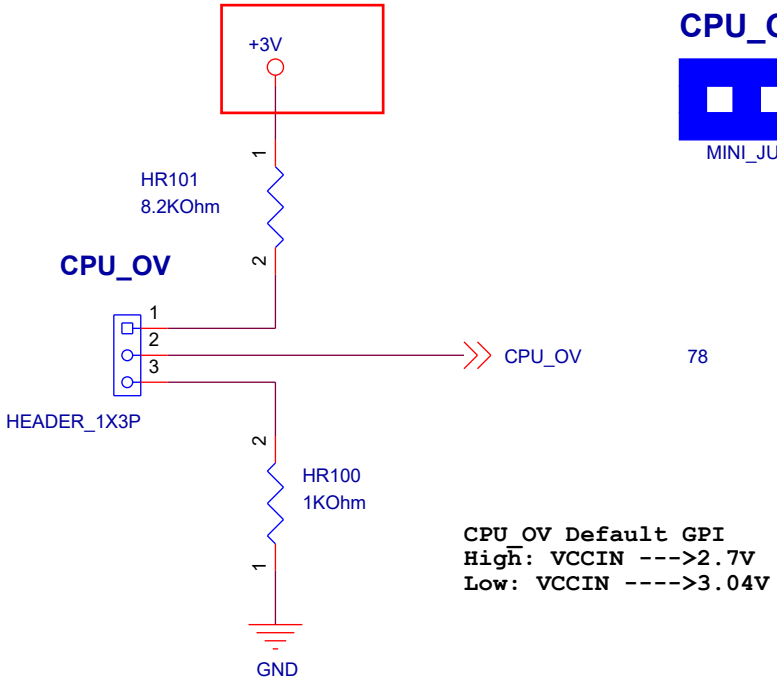
ASUSTek Computer Inc.

Title : TB_Header

Engineer: Aaron_Su

Size	Project Name	Rev
A3	Z390 Golden board	0.5A

Date: Tuesday, July 24, 2018 Sheet 120 of 139



CPU_OV_12

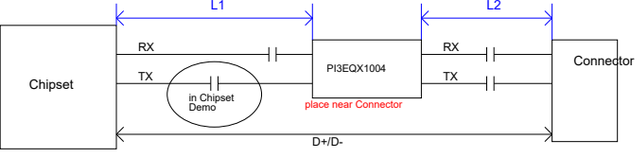
MINI_JUMPER

CPU_OV Default GPI
High: VCCIN --->2.7V
Low: VCCIN ---->3.04V

Z97_R1.01

<Variant Name>

ASUSTek Computer Inc.	Title : CPU_OV	
	Engineer: Eason	
Size: A	Project Name: Z270-STRIX	Rev: 1.02
Date: Tuesday, July 24, 2018	Sheet 117 of 123	



Net	Impedance/Width	Space	Length
TX/RX L1	follow USB 3.1 Controller Rule	30 mils	< 10", prefer 5" - 9"
TX/RX L2		30 mils	< 2.5", prefer 0.5" - 1.5"
+3V_RDP2	>= PI3EQX1004 IC Count *20 mils		
Other Power Net	>= 20 mils		

USB 3.1 Re-Driver PI3EQX1004 Circuit

A. Delete the Re-Driver IC which is not needed by Project

B. Modify Input USB 3.1 TX/RX Signal Net Name by Project

C. Modify Output USB 3.1 TX/RX Signal Net Name by Project

D. Choose PI3EQX1004 Power Solution by PI3EQX1004 count

E. If UU41 TXA output signals send to ASM1543, UU41C34 & UU41C35 change from 11V232222416150 to 11V232334150 & mount UU41R34, UU41R35, otherwise could delete UU41R34, UU41R35

F. If UU41 TXB output signals send to ASM1543, UU41C26 & UU41C27 change from 11V232222416150 to 11V232334150 & mount UU41R26, UU41R27, otherwise could delete UU41R26, UU41R27

G. If UU42 TXA output signals send to ASM1543, UU42C34 & UU42C35 change from 11V232222416150 to 11V232334150 & mount UU42R34, UU42R35, otherwise could delete UU42R34, UU42R35

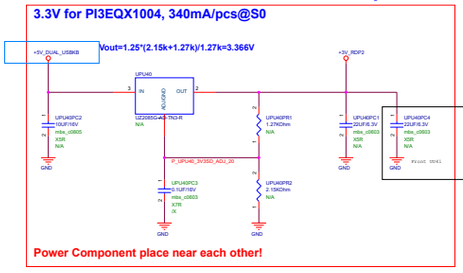
H. If UU42 TXB output signals send to ASM1543, UU42C26 & UU42C27 change from 11V232222416150 to 11V232334150 & mount UU42R26, UU42R27, otherwise could delete UU42R26, UU42R27

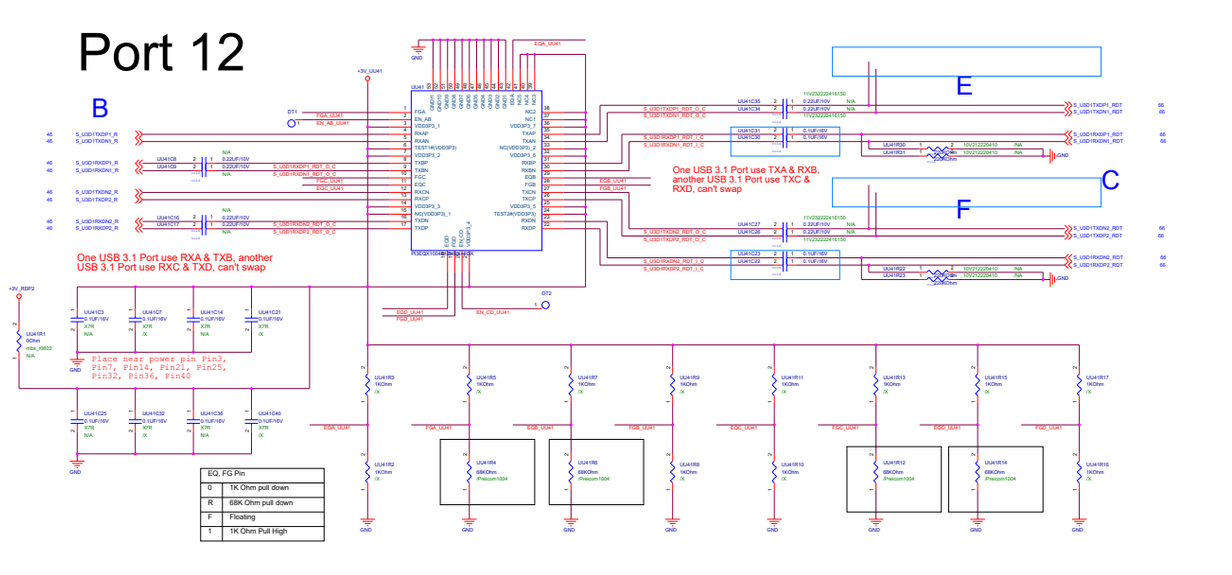
I. If UU43 TXA output signals send to ASM1543, UU43C34 & UU43C35 change from 11V232222416150 to 11V232334150 & mount UU43R34, UU43R35, otherwise could delete UU43R34, UU43R35

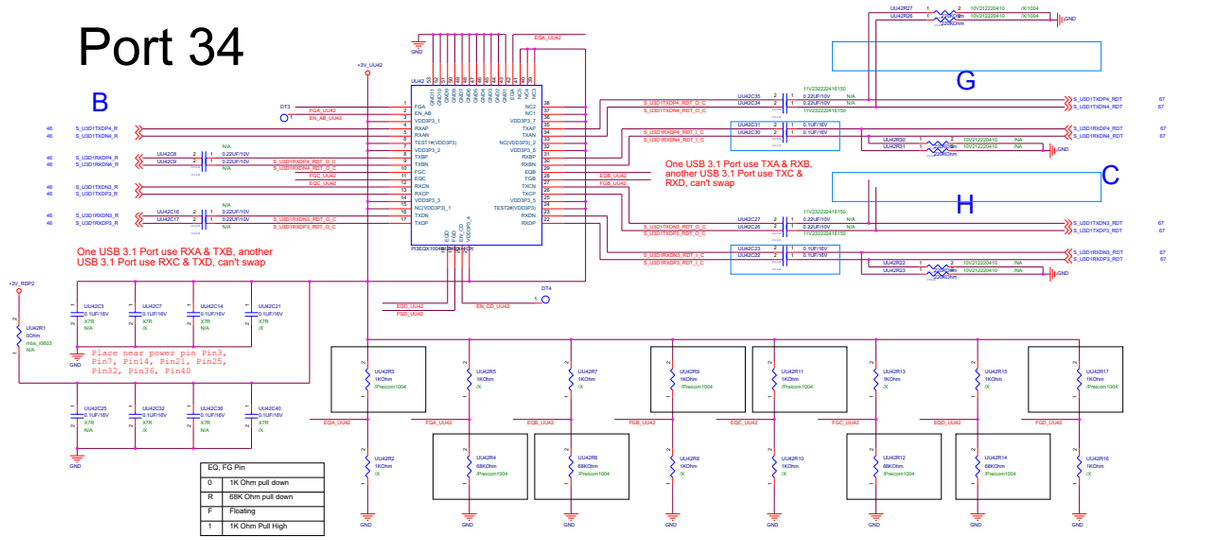
J. If UU43 TXB output signals send to ASM1543, UU43C26 & UU43C27 change from 11V232222416150 to 11V232334150 & mount UU43R26, UU43R27, otherwise could delete UU43R26, UU43R27

D.2

Power Solution for PI3EQX1004 *2/3pcs







請確認是否為 USB3.1GEN1 或GEN2
1.GEN1請選擇2.6A/GEN2請選擇3.5A
2. 兩個port共用一組OC# & VBUS PWR
3. 確認connector VBUS PWR
netname是否一致

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

Connect to Chipset

Connect to Connector

Connect to Redriver or Retimer

USB1

Connect to Redriver or Retimer

USB2

Reserve for EMI

ASUS PIN ESD SPEC
Back I/O : +/- 8KV
Front I/O : +/- 10KV

ESD橋框選擇方式:

組合 \ 橋框	A	B	C
Front I/O	Keep	Keep	Delete
Back I/O layout空間夠	Keep	Keep	Delete
Back I/O layout空間不夠	Keep	Delete	Delete
Back I/O layout空間不夠 且Pin ESD打不過8KV	Delete	Delete	Keep

Port 1,2

A

B

C

U31 GEN2 & GEN1 PIN ESD 橋框選擇方式:

組合 \ 橋框	A	B
U31 GEN 2 PIN ESD	Keep	Delete
U31 GEN 1 PIN ESD	Delete	Keep

A

U31GEN2 PIN ESD

B

U31GEN1 PIN ESD

Port 1

A

U31GEN2 PIN ESD

B

U31GEN1 PIN ESD

Port 2

USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題

<Variant Name>

ASUSTeK COMPUTER INC

Title : CHIPSET U31_Port1,2

Engineer: Brian Hsieh

Size: A2 | Project Name: Standard Circiut | Rev: 2.1

Date: Tuesday, July 24, 2018 | Sheet 9 of 13

請確認是否為 USB3.1GEN1 或GEN2
1.GEN1請選擇2.6A/GEN2請選擇3.5A
2. 兩個port共用一組OC# & VBUS PWR
3. 確認connector VBUS PWR
netname是否一致

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

Connect to Chipset

Connect to Redriver or Retimer

Connect to Connector

USB3

USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題

U31 GEN2 & GEN1 PIN ESD 橋框選擇方式:

組合 \ 橋框	A	B
U31 GEN 2 PIN ESD	Keep	Delete
U31 GEN 1 PIN ESD	Delete	Keep

A

B

U31GEN2 PIN ESD

Port 3

ESD橋框選擇方式:

組合 \ 橋框	A	B	C
Front I/O	Keep	Keep	Delete
Back I/O layout空間夠	Keep	Keep	Delete
Back I/O layout空間不夠	Keep	Delete	Delete
Back I/O layout空間不夠 且Pin ESD打不過4KV	Delete	Delete	Keep

A

Port 3,4

<Variant Name>

ASUSTeK COMPUTER INC

Title : CHIPSET U31_Port3,4

Engineer: Brian Hsieh

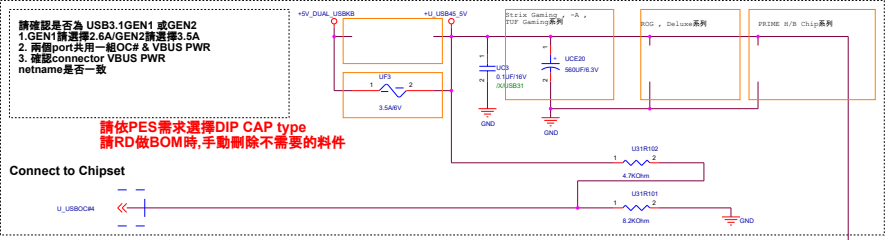
Size: A2 | Project Name: Standard Circuit | Rev: 2.1

Date: Tuesday, July 24, 2018 | Sheet 10 of 13

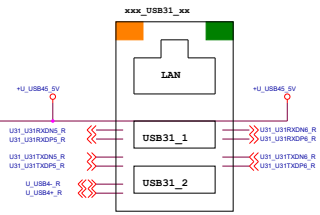
請確認是否為 USB3.1GEN1 或GEN2
1.GEN1請選擇2.6A/GEN2請選擇3.5A
2. 兩個port共用一組OC# & VBUS PWR
3. 確認connector VBUS PWR
netname是否一致

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

Connect to Chipset



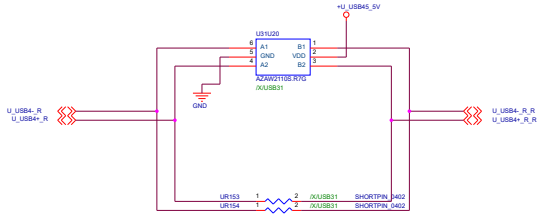
Connect to Connector



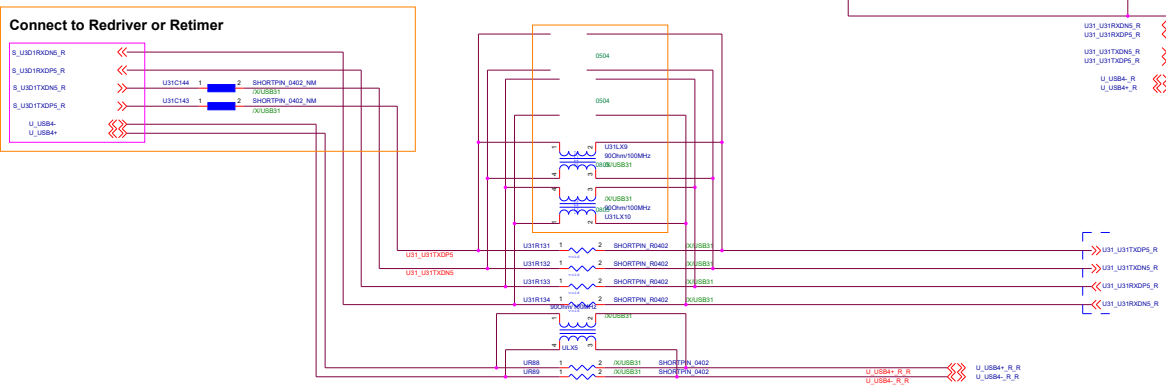
USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題

UR88~UR91 U31R131~U31R138
UR151~UR154

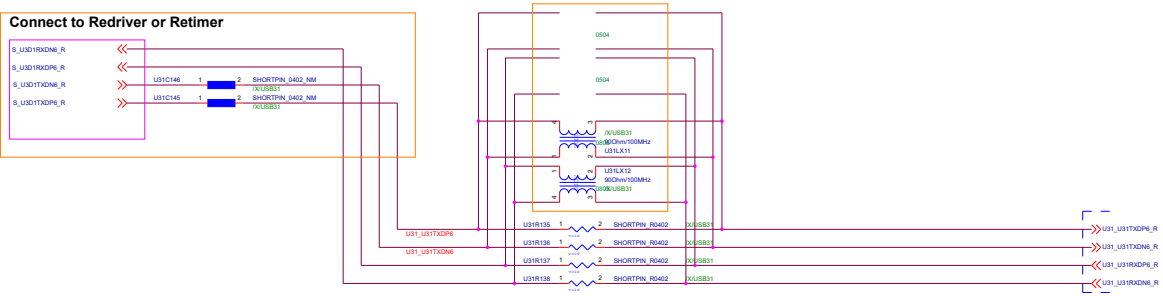


Connect to Redriver or Retimer



USB5

Connect to Redriver or Retimer



USB6

U31 GEN2 & GEN1 PIN ESD 橋框選擇方式:

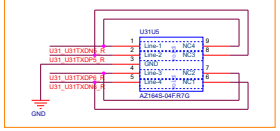
組合 \ 橋框	A	B
U31 GEN 2 PIN ESD	Keep	Delete
U31 GEN 1 PIN ESD	Delete	Keep

Port 5

A

U31GEN2 PIN ESD

B

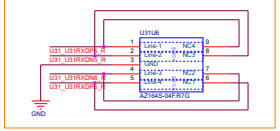


Port 6

A

U31GEN2 PIN ESD

B

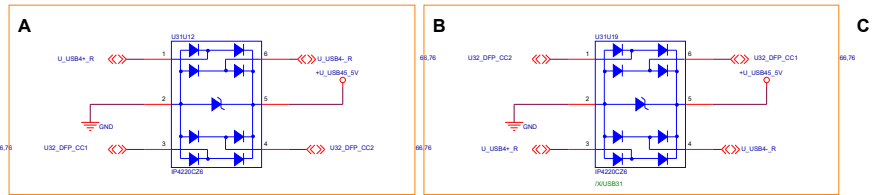


ASUS PIN ESD SPEC
Back I/O : +/- 8KV
Front I/O : +/- 10KV

ESD橋框選擇方式:

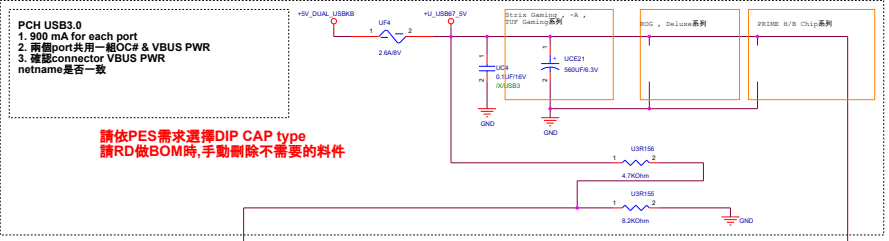
組合 \ 橋框	A	B	C
Front I/O	Keep	Keep	Delete
Back I/O layout空間夠	Keep	Keep	Delete
Back I/O layout空間不夠	Keep	Delete	Delete
Back I/O layout空間不夠 且Pin ESD打不過8KV	Delete	Delete	Keep

Port 5,6

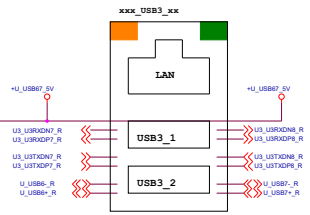


PCH USB3.0
1. 900 mA for each port
2. 兩個port共用一組OC# & VBUS PWR
3. 確認connector VBUS PWR
netname是否一致

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

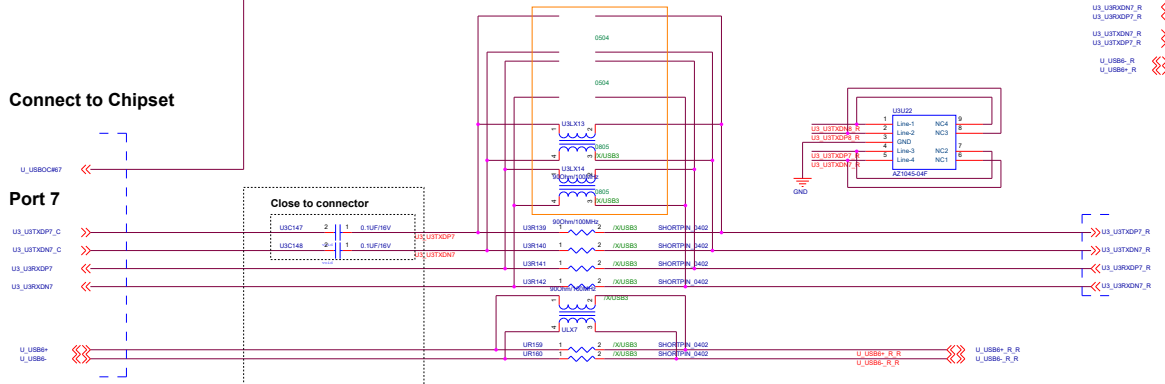


Connect to Connector



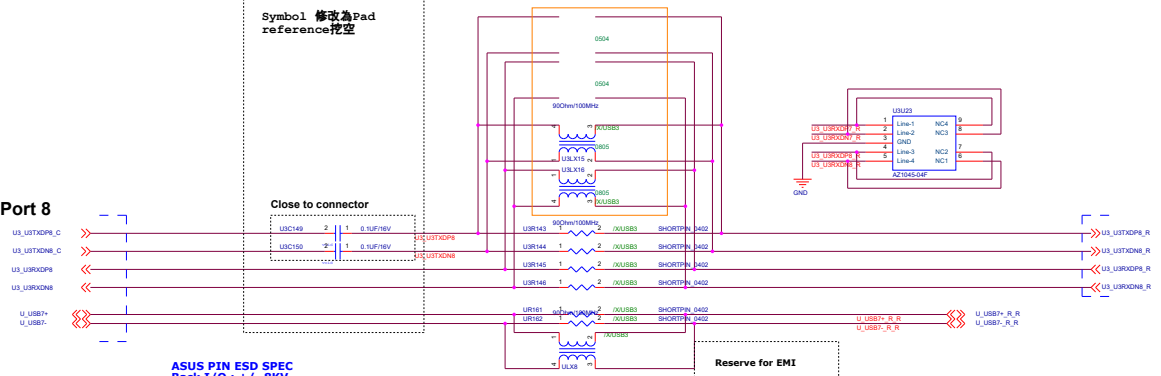
Connect to Chipset

Port 7



Symbol 修改為Pad reference挖空

Port 8



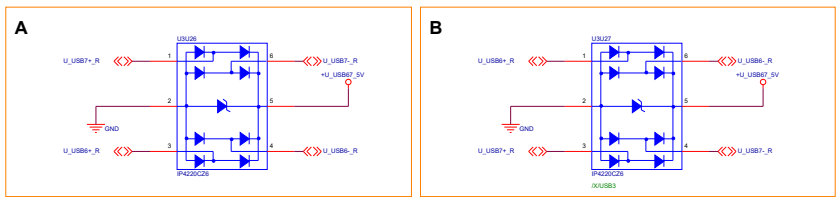
Reserve for EMI

ASUS PIN ESD SPEC
Back I/O : +/- 8KV
Front I/O : +/- 10KV

ESD橋框選擇方式:

組合 \ 橋框	A	B	C
Front I/O	Keep	Keep	Delete
Back I/O layout空間夠	Keep	Keep	Delete
Back I/O layout空間不夠	Keep	Delete	Delete
Back I/O layout空間不夠 且Pin ESD打不過8KV	Delete	Delete	Keep

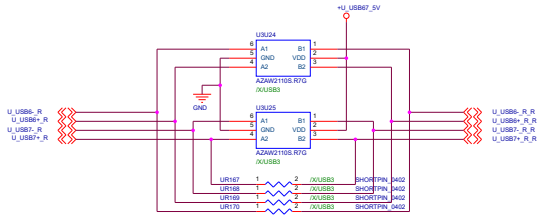
Port 7,8



UR159-UR162 U3R139-U3R146
UR167-UR170

USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題



<Variant Name>

ASUSTeK COMPUTER INC.

Title : CHIPSET U3_Port7,8
Engineer: Brian Hsieh
Size: A2
Project Name: Standard Circiut
Rev: 2.1
Date: Tuesday, July 24, 2018
Sheet 12 of 13

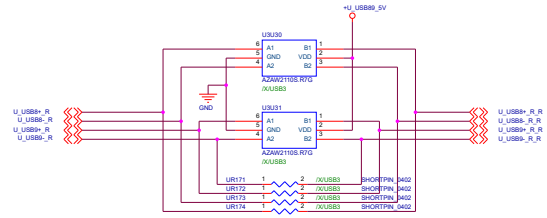
PCH USB3.0
1. 900 mA for each port
2. 兩個port共用一組OC# & VBUS PWR
3. 確認connector VBUS PWR
netname是否一致

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

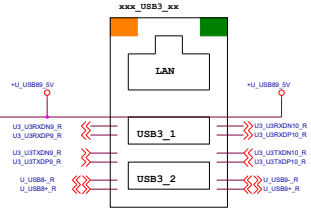
UR163-UR166 U3R147-U3R154
UR171-UR174

USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題

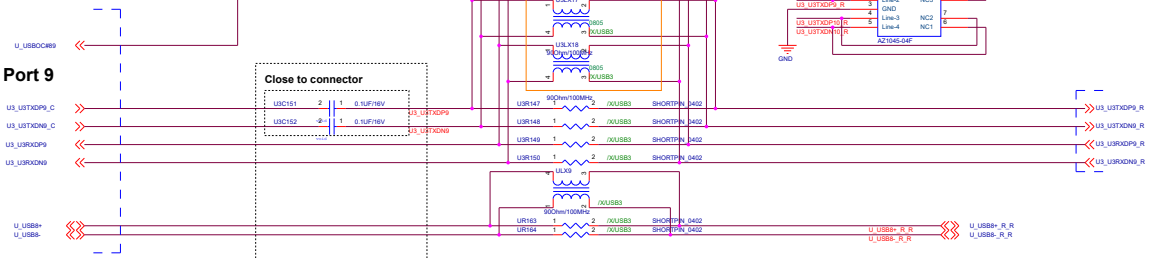


Connect to Connector

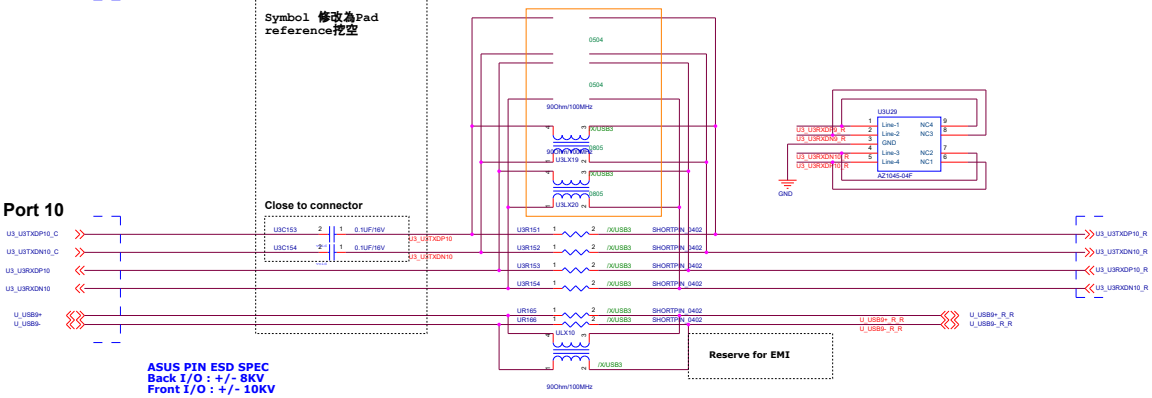


Connect to Chipset

Port 9



Port 10



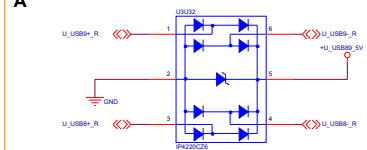
ASUS PIN ESD SPEC
Back I/O : +/- 8KV
Front I/O : +/- 10KV

ESD橋框選擇方式:

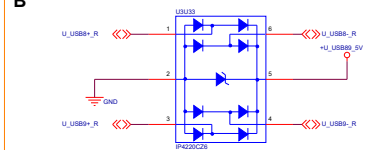
橋框 / 組合	A	B	C
Front I/O	Keep	Keep	Delete
Back I/O layout空間夠	Keep	Keep	Delete
Back I/O layout空間不夠	Keep	Delete	Delete
Back I/O layout空間不夠 且Pin ESD打不過8KV	Delete	Delete	Keep

Port 9,10

A



B



C

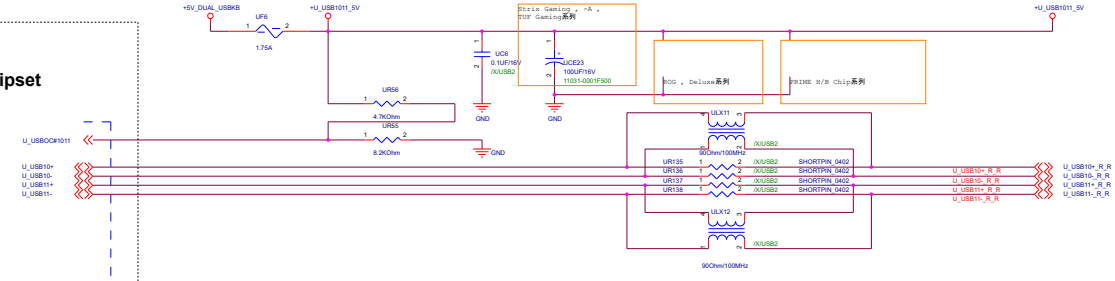
請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

Connect to Connector

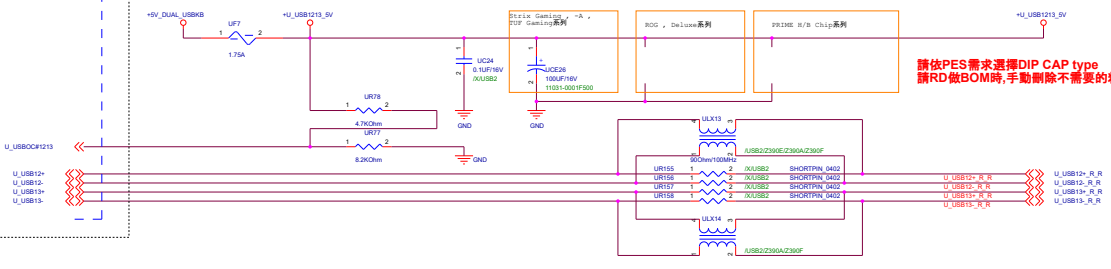
UR127~UR130 UR135~UR142 UR155~UR158

Connect to Chipset

Port 11,12



Port 13,14

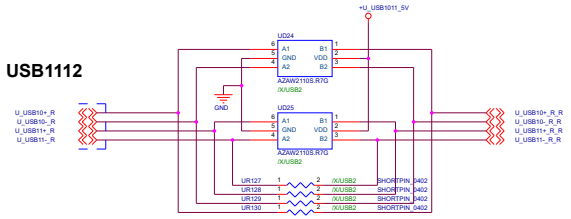


請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

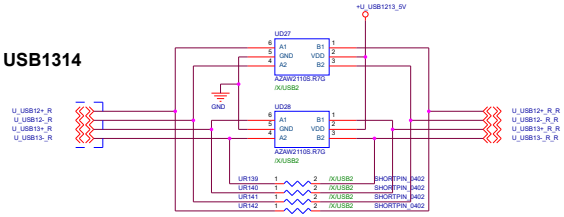
USB2.0 Guard

預防PCH USB2 Signal被Device高壓damaged問題

USB1112



USB1314

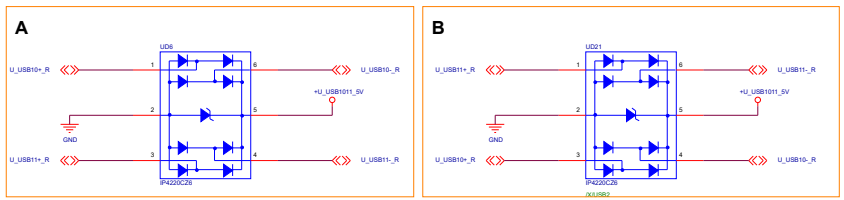


ASUS PIN ESD SPEC
Back I/O : +/- 8KV
Front I/O : +/- 10KV

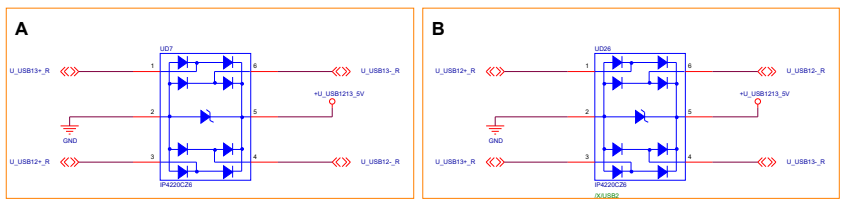
ESD橋框選擇方式:

橋框 / 組合	A	B	C
Front I/O	Keep	Keep	Delete
Back I/O layout空間夠	Keep	Keep	Delete
Back I/O layout空間不夠	Keep	Delete	Delete
Back I/O layout空間不夠且Pin ESD打不過8KV	Delete	Delete	Keep

Port 11,12



Port 13,14



<Variant Name>

ASUSTeK COMPUTER INC

Title : CHIPSET U2_Port13,14

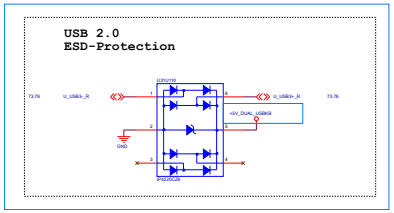
Engineer: Brian Hsieh

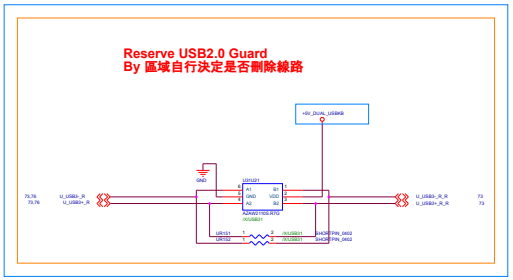
Size: A2 | Project Name: Standard Circiut | Rev: 2.1

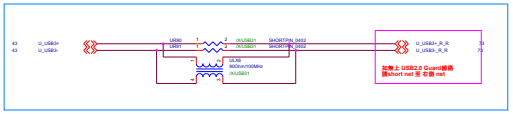
Date: Tuesday, July 24, 2018 | Sheet 8 of 13

Port A : Type C Connector

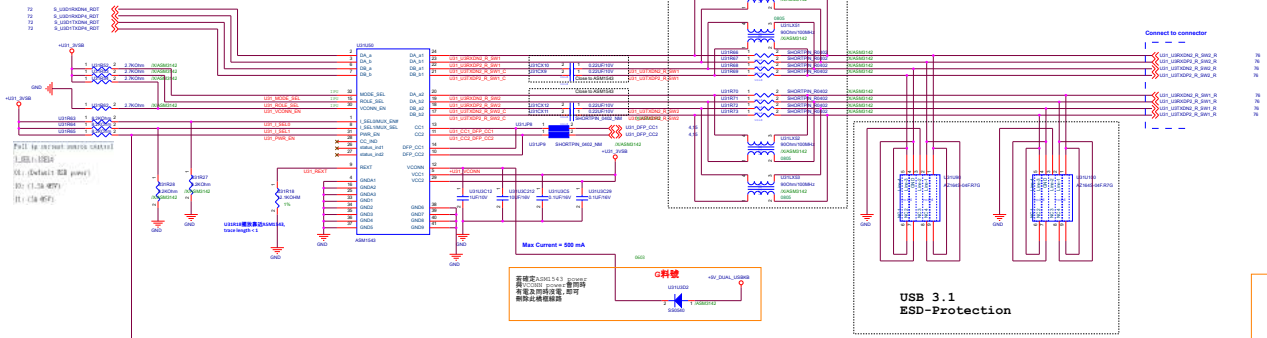
USB2.0
EMI-Protection

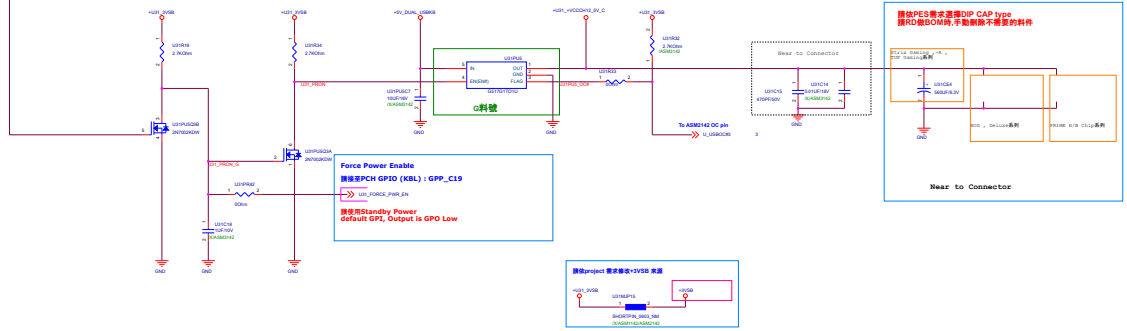


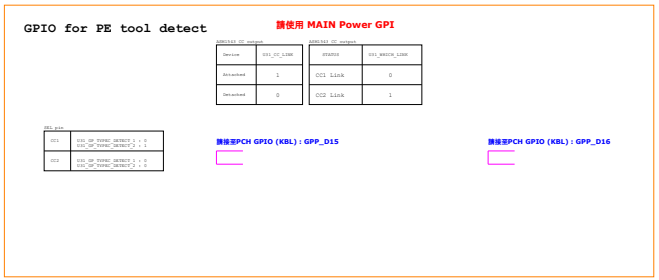


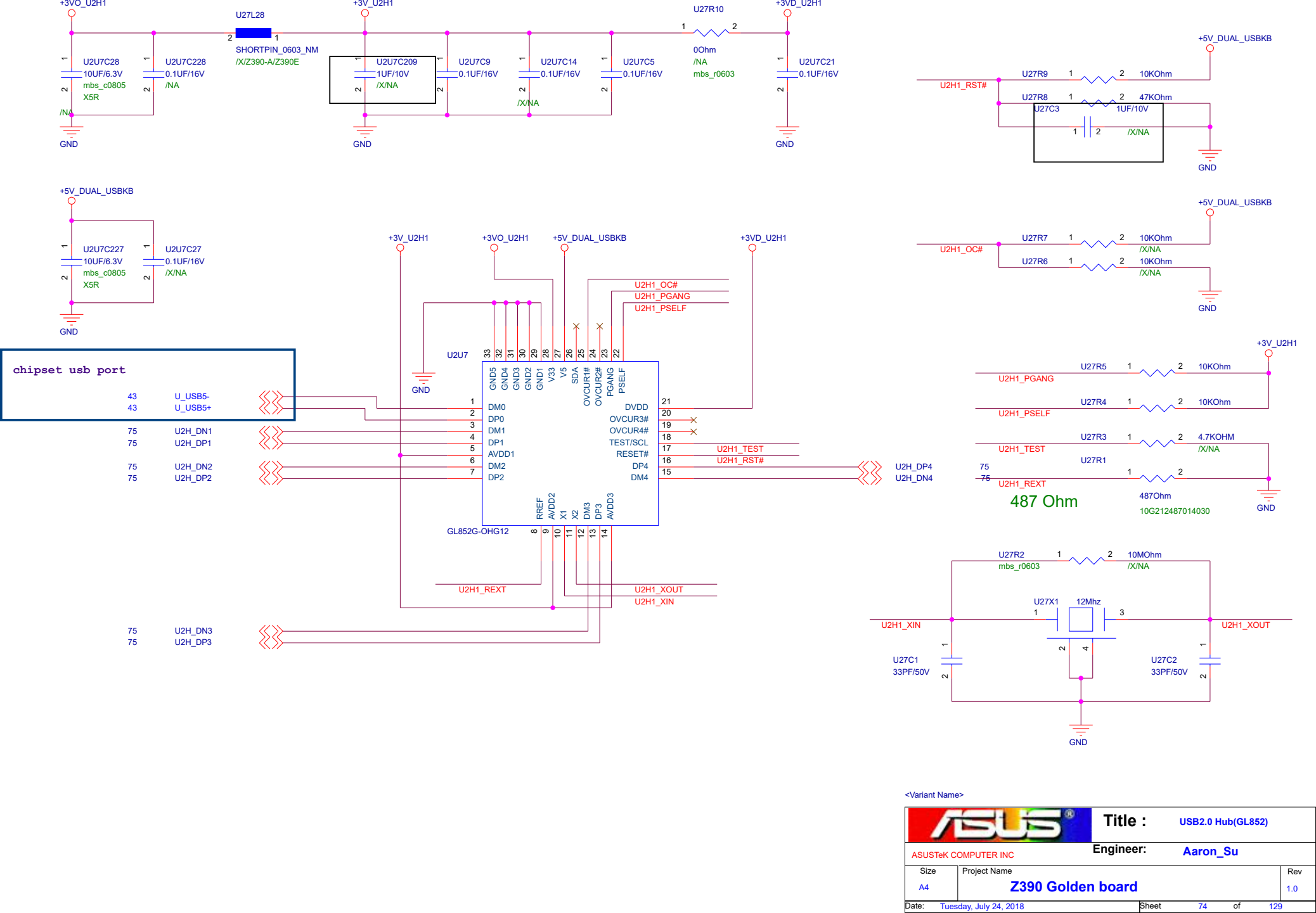


USB3.1
EMI-Protection









<Variant Name>

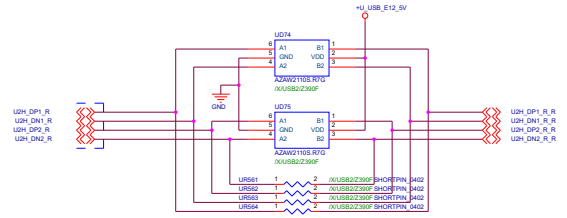
ASUSTeK COMPUTER INC	Title : USB2.0 Hub(GL852)	
	Engineer: Aaron_Su	
Size: A4	Project Name: Z390 Golden board	Rev: 1.0
Date: Tuesday, July 24, 2018	Sheet 74 of 129	

若chipset 只有12port,
請整頁刪除

請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

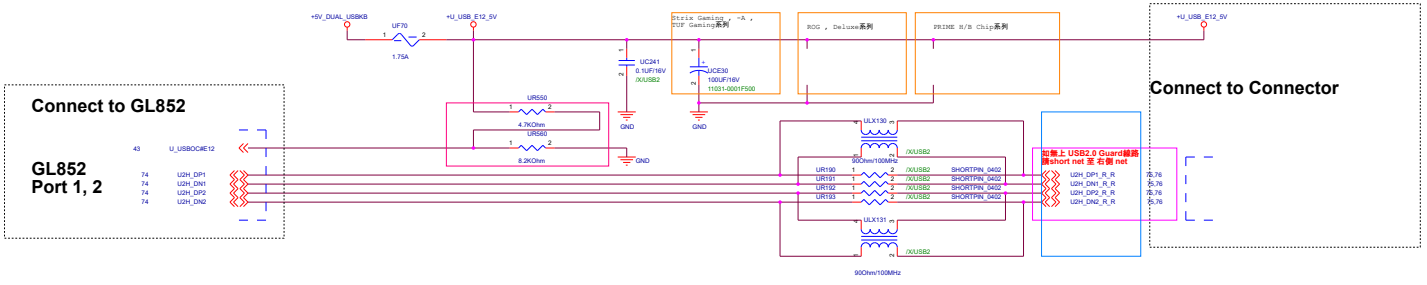
UR139~UR142
UR155~UR158

Reserve USB2.0 Guard
By 區域自行決定是否刪除線路



Connect to GL852

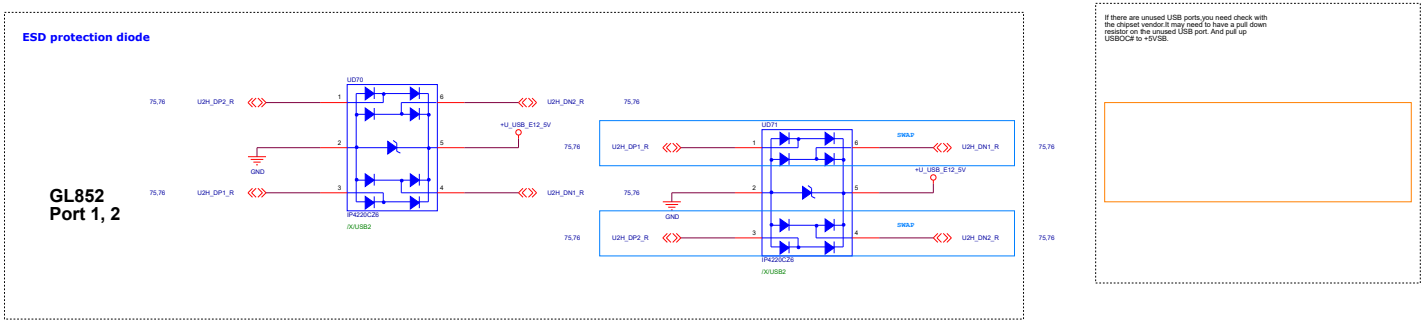
GL852
Port 1, 2



Connect to Connector

ESD protection diode

GL852
Port 1, 2



If there are unused USB ports,you need check with the chipset vendor.It may need to have a pull down resistor on the unused USB port. And pull up USBOC# to +5VSB.

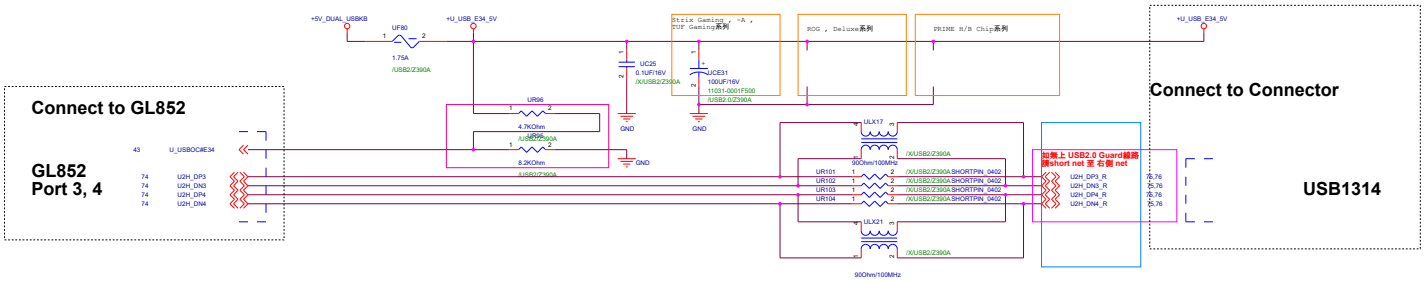
請依PES需求選擇DIP CAP type
請RD做BOM時,手動刪除不需要的料件

UR139~UR142
UR155~UR158

Reserve USB2.0 Guard
By 區域自行決定是否刪除線路

Connect to GL852

GL852
Port 3, 4

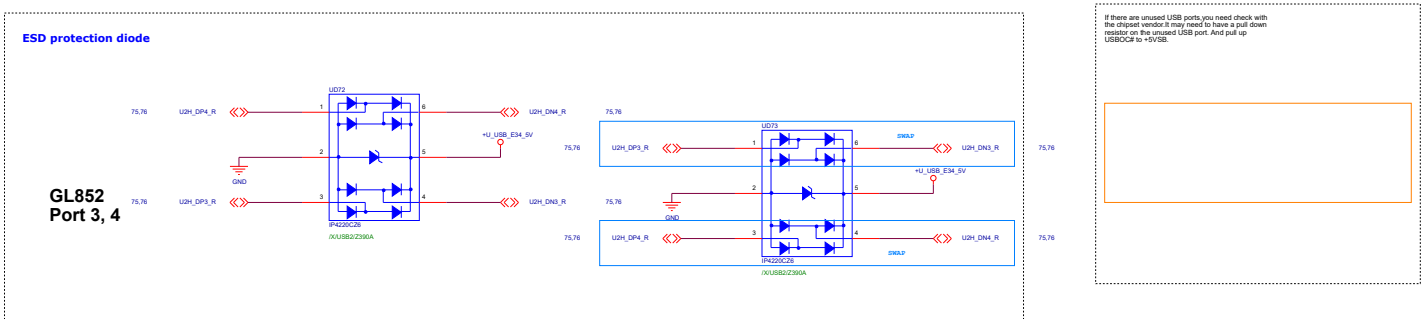


Connect to Connector

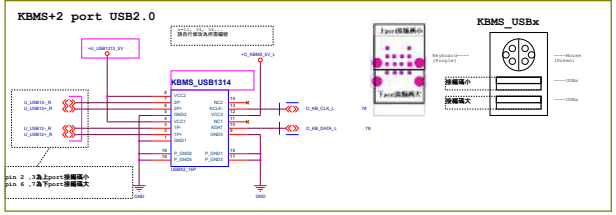
USB1314

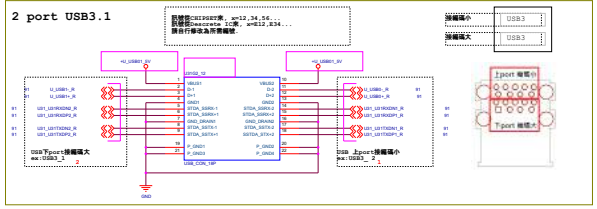
ESD protection diode

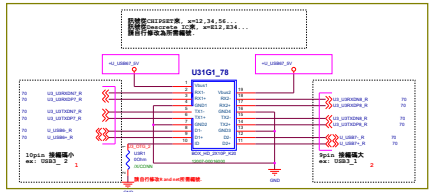
GL852
Port 3, 4

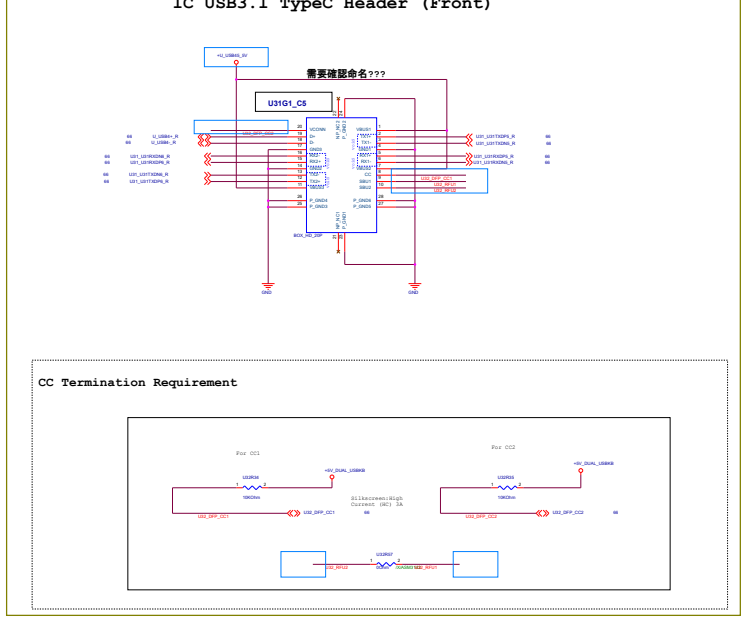


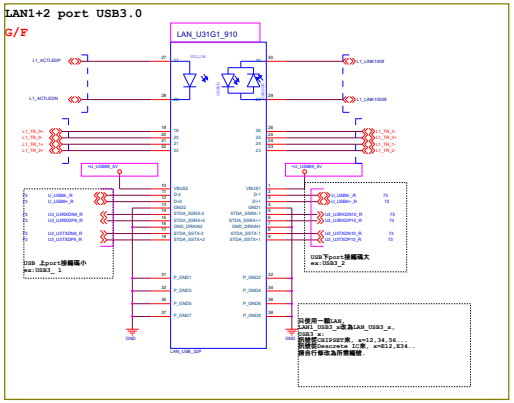
If there are unused USB ports,you need check with the chipset vendor.It may need to have a pull down resistor on the unused USB port. And pull up USBOC# to +5VSB.

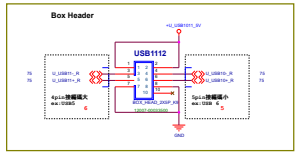


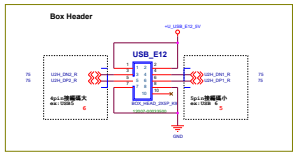


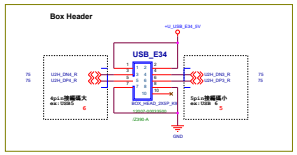


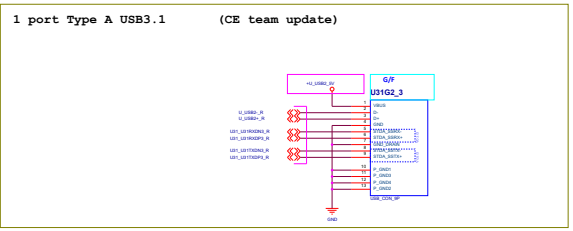


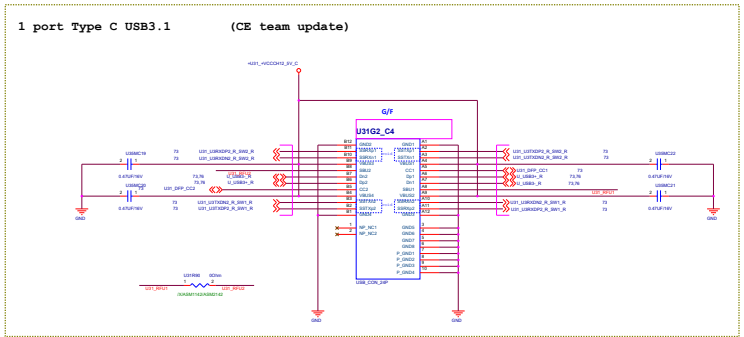




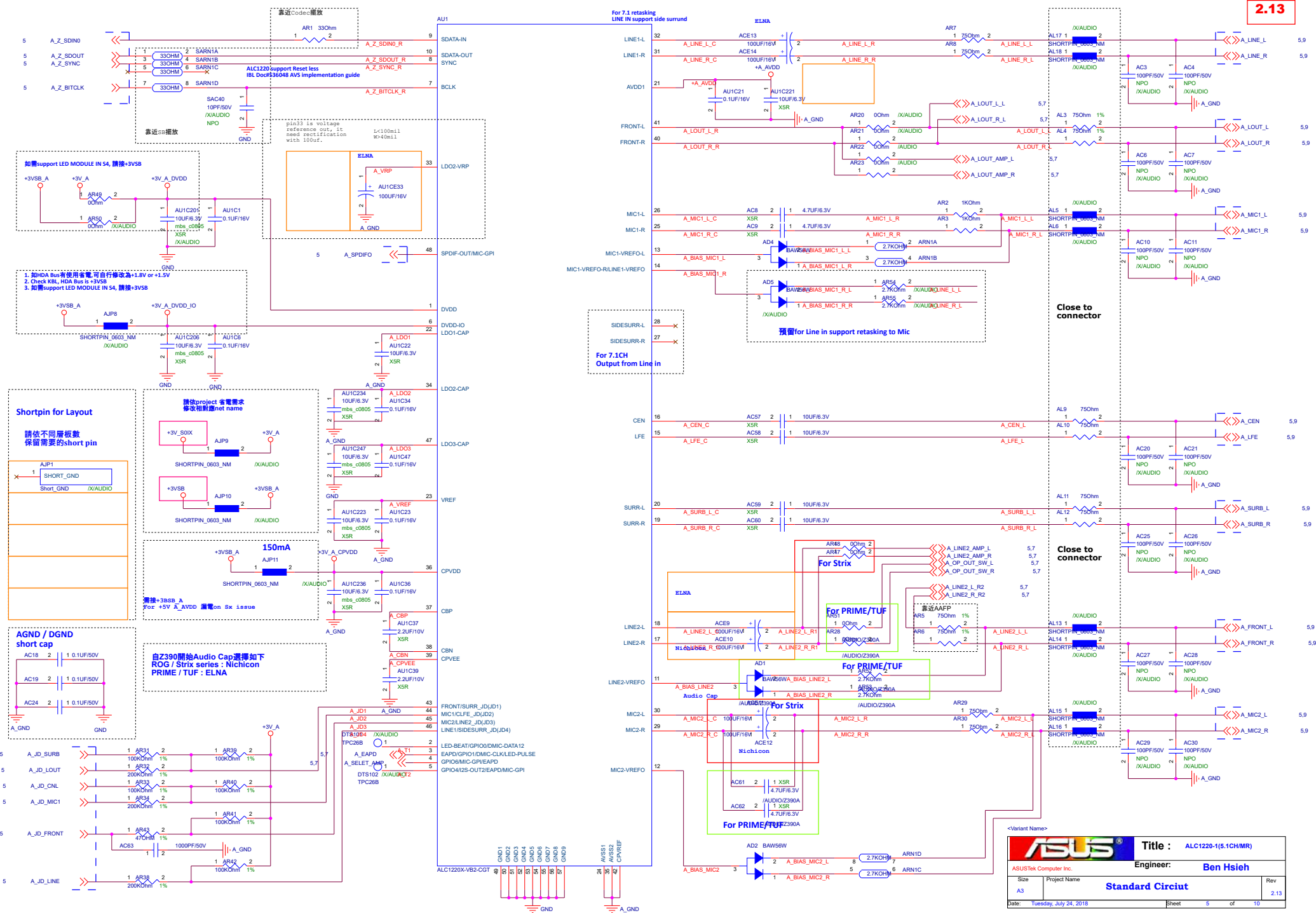








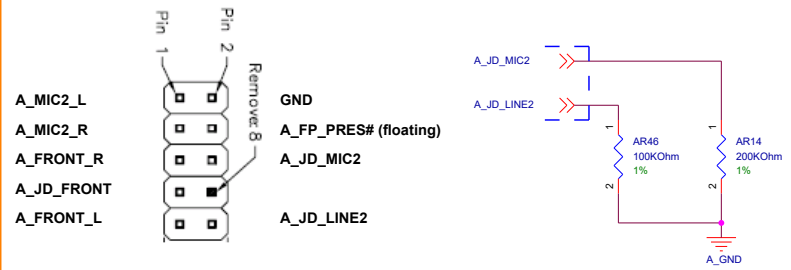
<Variant Name>			
Title :	Front Back IO_USB3.0		
Engineer:	Aaron_Su		
Size: A1	Project Name: CoffeeLake VC		Rev: V0.00
Date: Tuesday, July 24, 2018		Sheet 78 of 130	


靠近Codec擺放
ALC1220 support Reset less
IBL Doc#536048 AVS implementation guide
靠近SB擺放
pin33 is voltage reference out, it need rectification with 100uf.
如需support LED MODULE IN S4, 請接+3VSB
1. 如HDA Bus有使用省電,可自行修改為+1.8V or +1.5V
2. Check KBL, HDA Bus is +3VSB
3. 如需support LED MODULE IN S4, 請接+3VSB
Shortpin for Layout
請依不同層板數
保留需要的short pin
請依project 省電需求
修改相對應net name
150mA
AGND / DGND
short cap
自Z390開始Audio Cap選擇如下
ROG / Strix series : Nichicon
PRIME / TUF : ELNA
For 7.1 retasking
LINE IN support side surrund
For 7.1CH
Output from Line in
預留for Line in support retasking to Mic
Close to connector
For Strix
For PRIME/TUF
Audio Cap
Nichicon
ELNA
靠近AAFP
ALC1220-VB2-CGT
Title : ALC1220-1(5.1CH/MR)
ASUSTek Computer Inc.
Engineer: Ben Hsieh
Standard Circiut
Size A3
Date: Tuesday, July 24, 2018
Sheet 5 of 10
Rev 2.13

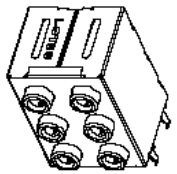
Standard Circuit	
AUDIO	ALC1220
REV.	A_2.13

ALC1220 /X/AUDIO

Front Panel

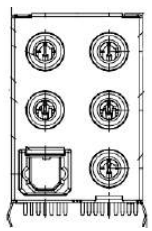


Back Panel
7.1 Channel Connector(示意圖)



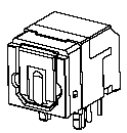
橘	●	●	藍
黑	●	●	綠
灰	●	●	粉紅

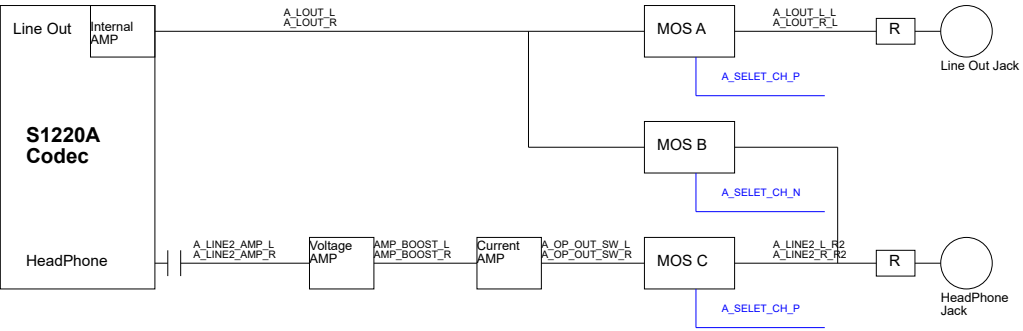
Back Panel
5.1Channel Connector
+SPDIF OUT(Optical)(示意圖)



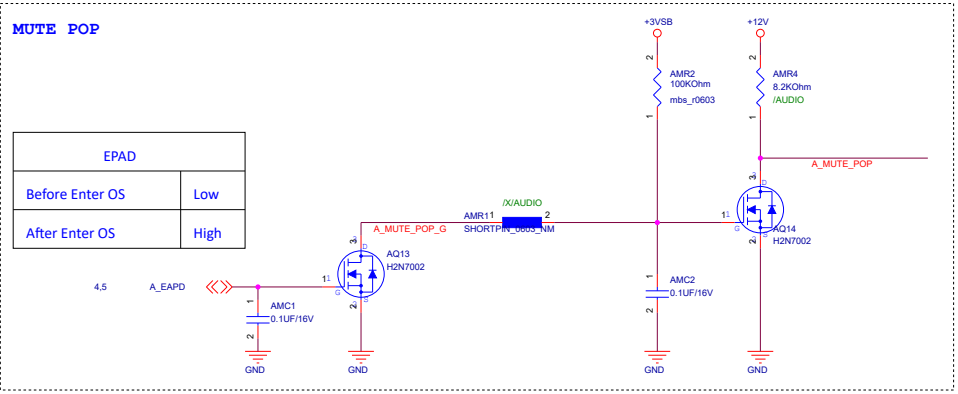
橘	●	●	藍
黑	●	●	綠
SPDIF OUT (Optical)	▭	●	粉紅

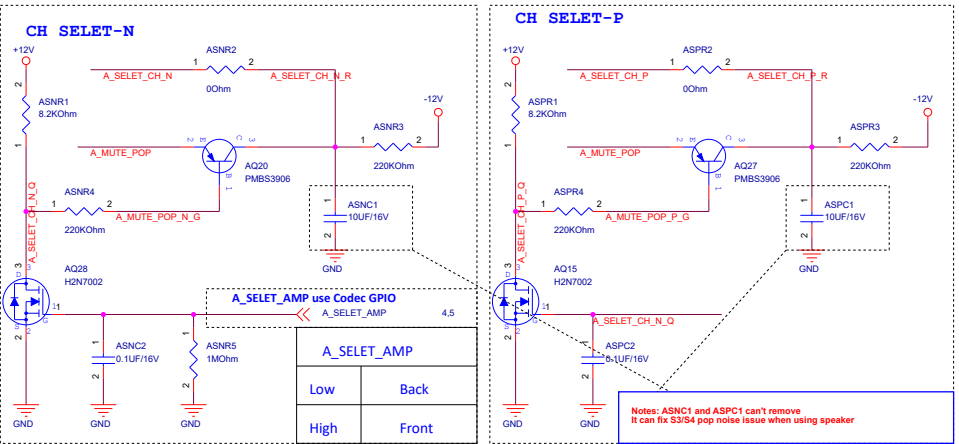
SPDIF OUT (Optical)(示意圖)



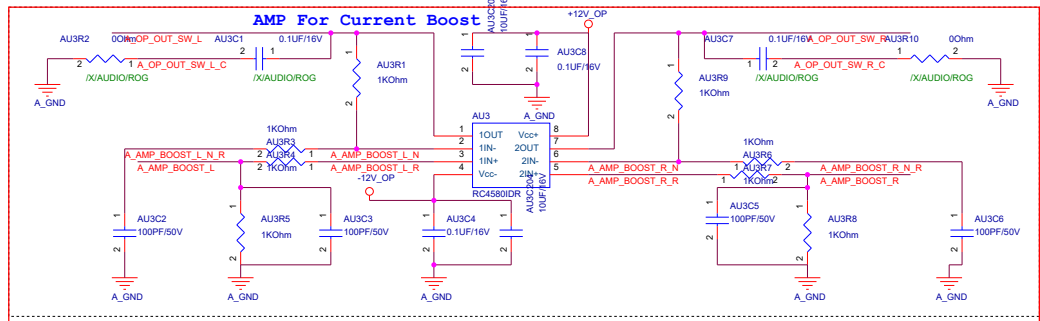


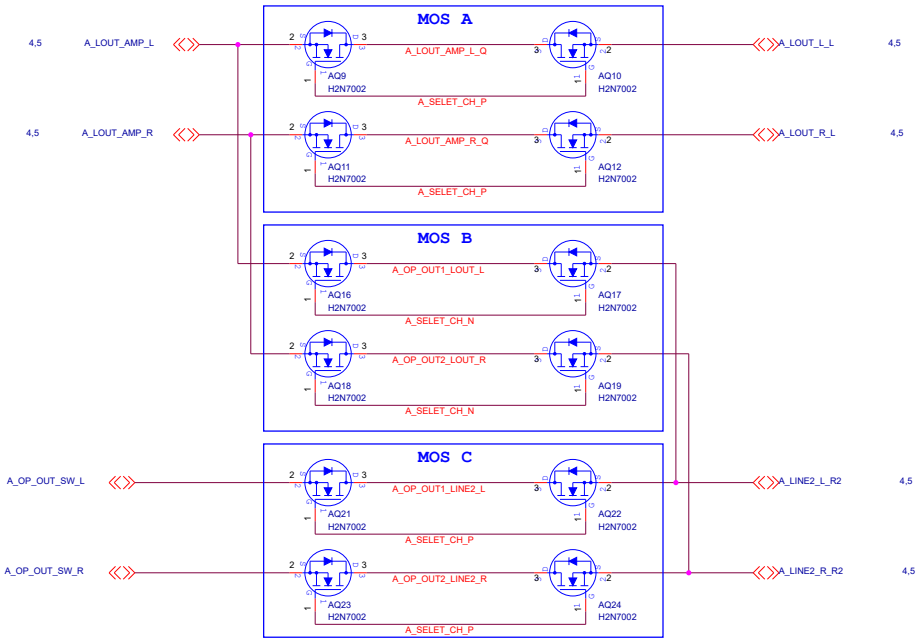
SELET_CH_P	SELET_CH_N	MOS A&C	MOS B	
-12V	-12V	Off	Off	De-POP for Power On & Power Off
+12V	-12V	On	Off	Impedance sensing for Lout Jack
-12V	+12V	Off	On	Impedance sensing for HP Jack
+12V	+12V	On	On	Not Allowed



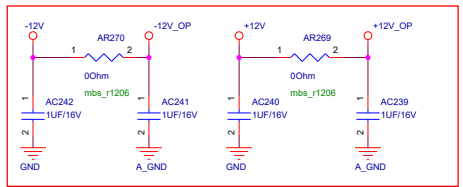


For Strix





For Strix



<Core Design>

ASUSTek Computer Inc.

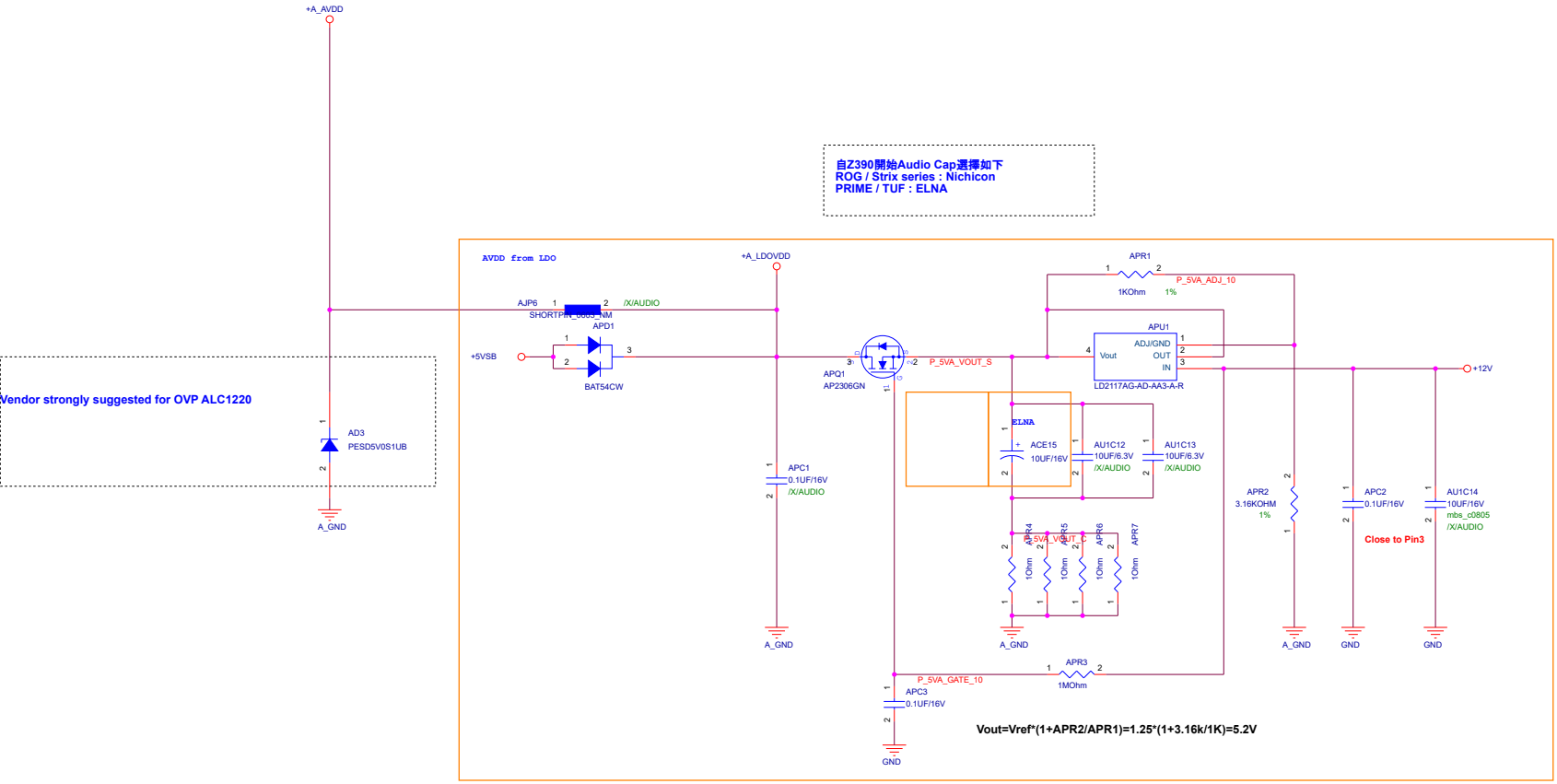
Title : ALC1220-3 (AMP)

Engineer: Ben Hsieh

Size	Project Name	Rev
A3	Standard Circuit	2.13

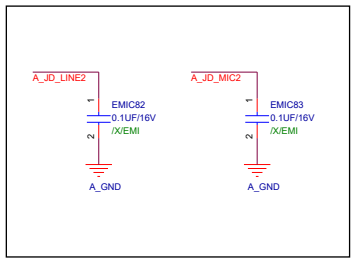
Date: Tuesday, July 24, 2018 Sheet 8 of 10

請依PES是否有上LDO 選擇相對應線路

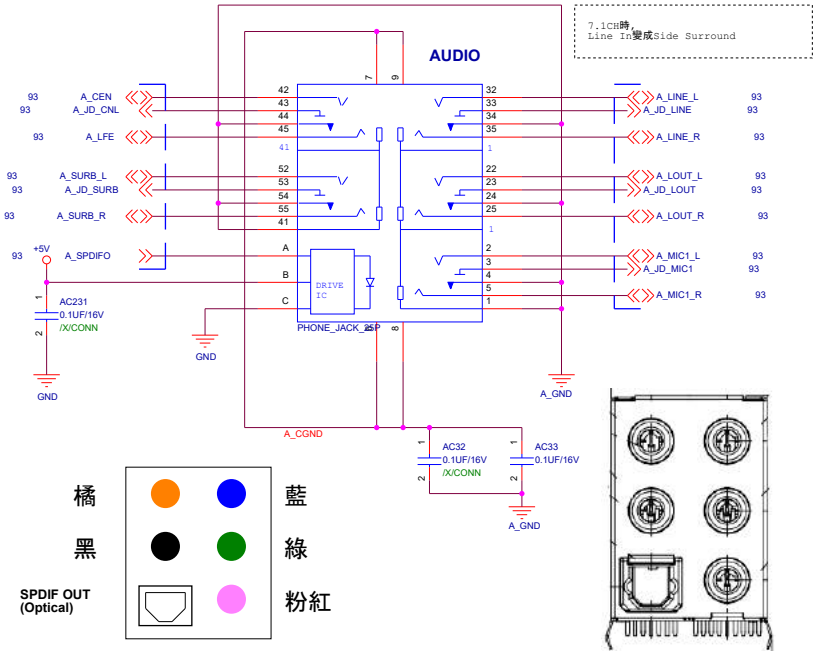


<Variant Name>

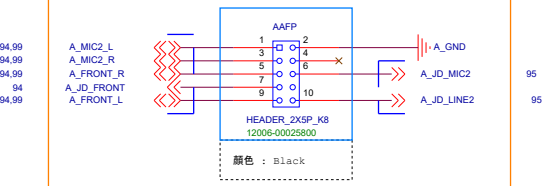
ASUSTek Computer Inc.	Title : ALC1220-5 (LDO)	
	Engineer: Ben Hsieh	
Size: A3	Project Name: Standard Circiut	Rev: 2.13
Date: Tuesday, July 24, 2018	Sheet 9 of 10	



Back Panel 5.1Channel Connector +SPDIF OUT(Optical)



Front Panel

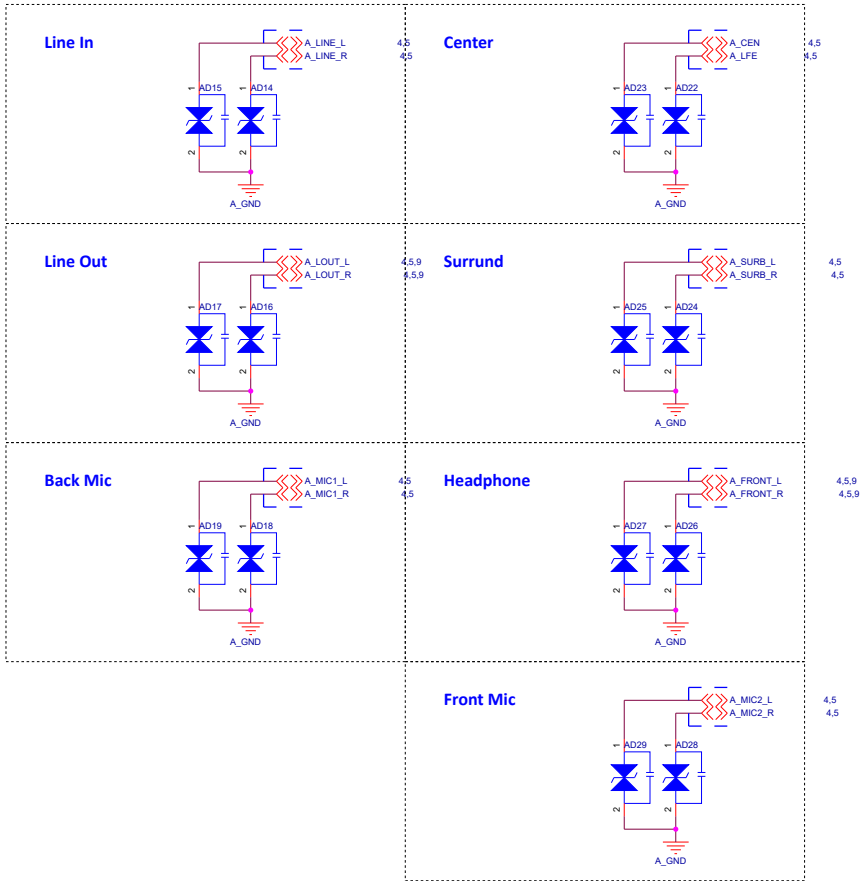


VARISTOR

Pin ESD spec (自Z370起spec)

Line Out	Headphone	Center	Surrund	Front Mic	Line In	Back Mic
5KV	5KV	4.5KV	4.5KV	5KV	4.5KV	5KV

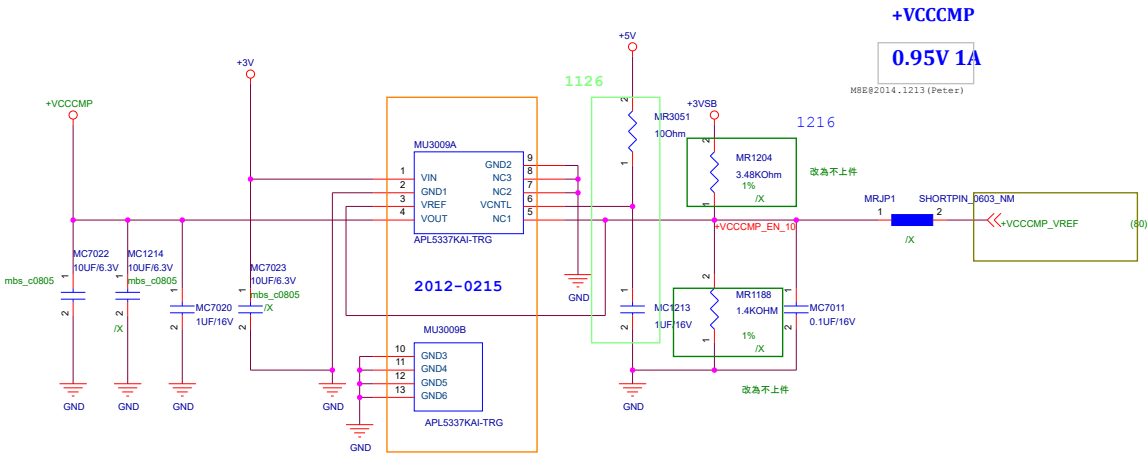
For ALC1220 B2：所有Varistor皆需上件



<Variant Name>

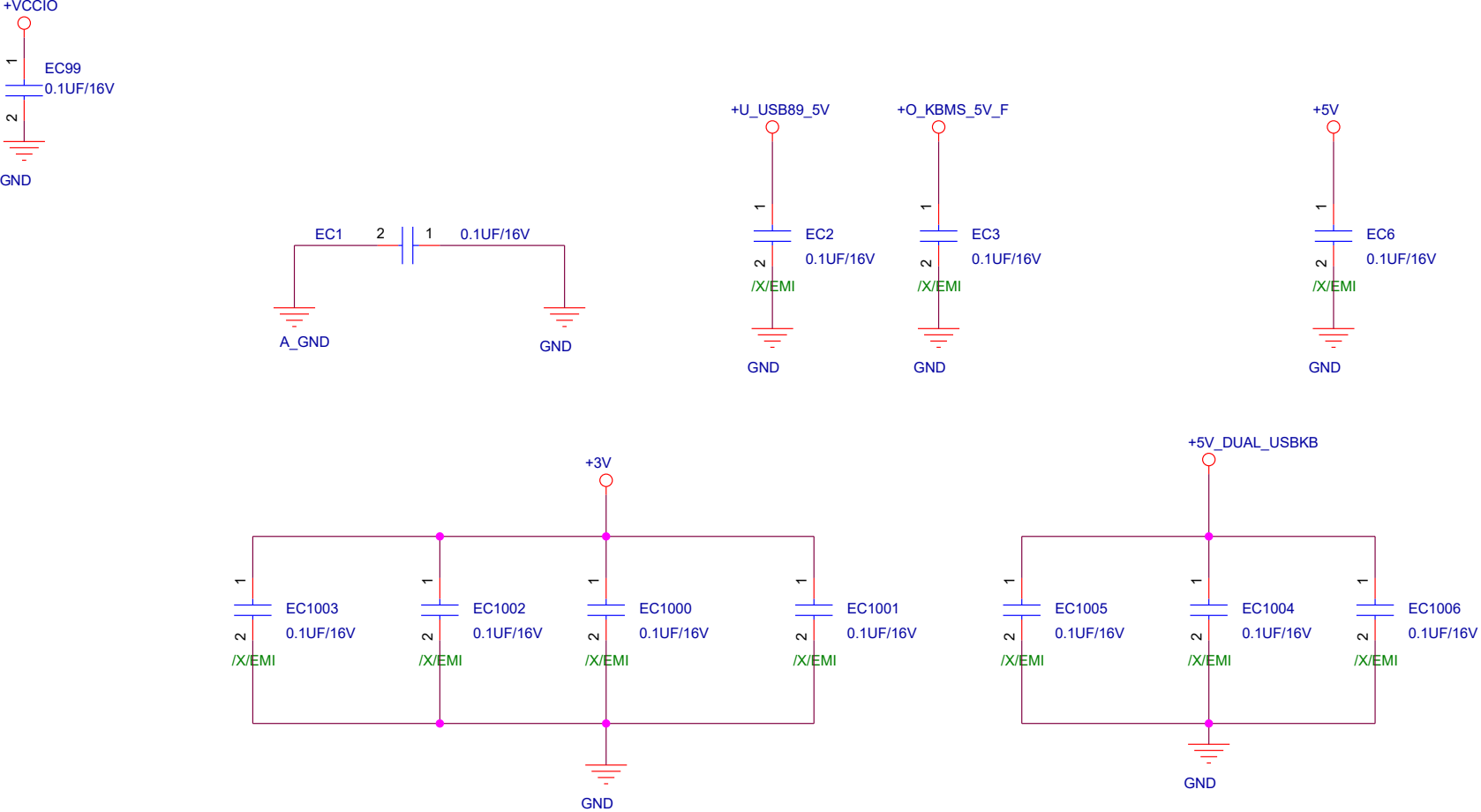
ASUSTek Computer Inc.	Title : ALC1220-6 (VARISTOR)	
	Engineer: Ben Hsieh	
Size: A3	Project Name: Standard Circiut	Rev: 2.13
Date: Tuesday, July 24, 2018	Sheet 10 of 10	

10 mil



<Variant Name>

ASUSTEK COMPUTER INC	Title : +VCCCMP/+VCCIO_G	
	Engineer: Aaron_Su	
Size: A3	Project Name: Z390 Golden board	Rev: 0.1A
Date: Tuesday, July 24, 2018	Sheet 134 of 139	



Title	<Title>	
Size: A	Document Number: Z390 Golden board	Rev: <RevCode>
Date: Tuesday, July 24, 2018	Sheet 144 of 139	

ASUS PCB Logo

PCB MADE IN CHINA

LOGO20
NODE
NODE
/X

LOGO7
PCB MADE IN CHINA
PCB_MADE_IN_CHINA
/X

LOGO5
WEEE_LOGO
WEEE_LOGO
/X

LOGO30
SFIS LABEL
SFIS_LABEL
/X

LOGO8
VCCI
VCCI
/X

因應歐盟針對無線指令的修改,有Wi-Fi機種也請選用CE

LOGO6
CE
CE
/X

無Wi-Fi機種請選用CE

LOGO2
FCC
FCC
/X

LOGO3
RCM
RCM
/X

LOGO1
EMI_D33005_H
EMI_D33005_H
/X

文字在右方

文字在下方

LOGO9
CAN ICES-3(B)/NMB-3(B)
CAN_ICES_3B_NMB_3B
/X

CAN ICES-3 (B)/NMB-3(B)

ASUS Logo

LOGO28
ASUS
ASUS
/X

M/B Default請選擇此Symbol (5.5mm)

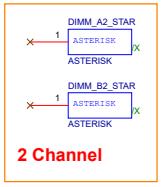
<Variant Name>

ASUSTEK COMPUTER INC	Title :	PCB Logo	
	Engineer:	Kell_Huang	
Size: A3	Project Name: Silkscreen		Rev: 0.2G
Date: Tuesday, July 24, 2018	Sheet 114 of 129		

ASUS PCB Logo

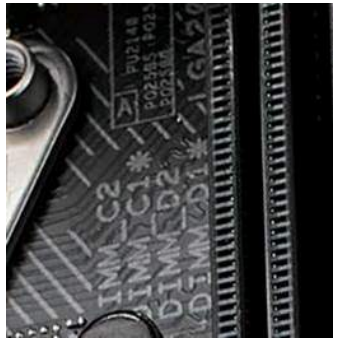
DRAM Slot Naming Rule

DIMM slot '*' 命名方式, 若 MR team 建議先插
1. DIMM_x1 就叫做 DIMM_A1_STAR, DIMM_B1_STAR … 以此類推
2. DIMM_x2 就叫做 DIMM_A2_STAR, DIMM_B2_STAR … 以此類推
3.RD請與MR確認後提Modify給Layout確認'*'擺放位置



2 Channel

4 Channel



KCC Logo

無Wi-Fi機種使用

10mm for主板使用

無Wi-Fi機種使用

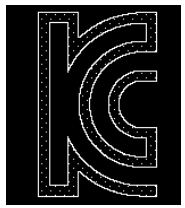
6.8mm for小卡使用

有Wi-Fi機種使用

10mm for主板使用

有Wi-Fi機種使用

6.8mm for小卡使用



**出圖前請與SPM確認KCC LOGO和FCC LOGO已更新到最新版本

烏克蘭LOGO

無Wi-Fi機種使用

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X4	V	V	temp_M01_000320

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X2	V	V	temp_T_001453

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X4	X	V	temp_T_001454

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X2	X	V	temp_T_001455

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X4	X	X	temp_T_001456

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X2	X	X	temp_T_001457

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X	V	X	temp_T_001458

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X4	V	X	temp_T_001486

PCIE	SATA	IRST	料號
"X4" or "X2"	"V" or "X"	"V" or "X"	
X2	V	X	temp_T_001487

請依PES選擇相對應文字框及修改流水號

M.2_1

PCIE	SATA	IRST
X4	V	V

M2_1

/X

M.2_2

PCIE	SATA	IRST
X4	X	V

M.2_3

/X

<Variant Name>

ASUSTEK COMPUTER INC

Title : M2_TEXT

Engineer: Grace Wu

Size	Project Name	Rev
A3	Silkscreen	0.2F

Date: Tuesday, July 24, 2018 Sheet 113 of 129

有支援addressable線路, 第6頁請刪除

IC在主板上的情境使用, 右邊線路請移除

SMBUS 請依平台選擇SMBUS, 不要的請刪除

由SIO的SMBUS來猜錄及控制

Intel：接SIO Pin51,52

SMBUS net 命名請依板子為主, 有不同請自行修改

請放置在IC的SMBUS附近

Net名稱：請依照順序命名

SMBUS2：接至ST072xx

要放置在IC的SMBUS附近

Location

A~C組PWM可Sink 50mA

D~H組PWM可Sink 20mA

請參考P.5~P.12

請依照區域命名

PCH(Z390-A)

RGB HEADER(A & E)

RGB HEADER (A & E)

若有外接MOS,請註解

Back IO(A&E)

Back IO(A&E)

Back IO(A&E)

IC Power

IDD=5mA

Isink=320mA

請將LED1C57擺放至Pin8附近

ACPI 支援開/關機特效

進sleep S0時, 關閉LED燈

SLP_S0_PLT_N_10

High：開燈

Low：關燈

(進入S0ix時, 關閉LED特效)

SMBUS Address:9C

若有使用2顆6K582, 請由右至左定義address

IC或LED燈在燈板上的情境使用(左邊線路請移除)

Net name ：請依需求自行規劃

Pin define ：請注意Pin順序是否與燈卡

Ver 1.2

Cable list(請與機構確認cable長度需求)：

8Pin

14011-00700100 115mm 醋酸膠布；
w to b 8pin (R/A) 12017-00800100通用
14011-00700200 70mm 醋酸膠布
14011-00700300 110mm 醋酸膠布

13pin

w to b 13pin (S/T) 12017-00960100

13Pin

14011-02620200 50mm 醋酸膠布
14011-02620100 370mm 醋酸膠布
14011-02620300 60mm 醋酸膠布
14011-02620000 130mm 醋酸膠布

Title：	6K582(ADD LED)
Engineer：	Kaizer_Luo
Size	Custom
Project Name	LED Standard Circuit
Rev	1.2
Date	Tuesday, July 23, 2019
Sheet	6 of 10

沒有支援OLED，請選則本頁線路，第1、2頁請刪除

Ver 1.3

<Variant Name>

Title : ST072CB(No OLED)

ASUSTek Computer Inc.

Engineer: Kaizer_Luo

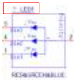
Size: Custom | Project Name: LED Standard Circiut | Rev: 1.3

Date: Tuesday, July 24, 2018 | Sheet 3 of 13

1.LED燈數 < 4顆 的接線方式

(請依需求選擇LED燈類型及顆數，不需要部分請刪除)

LED燈零件命名



LED零件命名規則：

請參照以下方式命名

位置	命名
0: CPU	0: CPU_LED
1: VRM	1: VRM_LED
2: NB	2: NB_LED
3: PCH	3: PCH_LED
4: Audio	4: AUD_LED
5: Back IO	5: BAKIO_LED
6: Back Plate	6: BAP_LED
7: PCIE	7: PCIE_LED
8: PCB Surround	8: MB_LED
9: M.2	9: M.2_LED
10:Start/retry Button	10: STN_LED
11:Light Bar	11: LB_LED

2.LED燈數大於4顆，但不超過20顆的接線方式

(請依需求選擇或刪減LED燈類型及顆數)

LED燈零件命名

LED零件命名規則：

請參照以下方式命名

位置	命名
0: CPU	0: CPU_LED
1: VRM	1: VRM_LED
2: NB	2: NB_LED
3: PCH	3: PCH_LED
4: Audio	4: AUD_LED
5: Back IO	5: BAKIO_LED
6: Back Plate	6: BAP_LED
7: PCIE	7: PCIE_LED
8: PCB Surround	8: MB_LED
9: M.2	9: M.2_LED
10:Start/retry Button	10: STN_LED
11:Light Bar	11: LB_LED

3.LED燈數大於20顆

(請依需求選擇LED燈類型及顆數，不需要部分請刪除)

LED燈零件命名

LED零件命名規則：

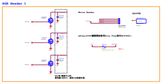
請參照以下方式命名

位置	命名
0: CPU	0: CPU_LED
1: VRM	1: VRM_LED
2: NB	2: NB_LED
3: PCH	3: PCH_LED
4: Audio	4: AUD_LED
5: Back IO	5: BAKIO_LED
6: Back Plate	6: BAP_LED
7: PCIE	7: PCIE_LED
8: PCB Surround	8: MB_LED
9: M.2	9: M.2_LED
10:Start/retry Button	10: STN_LED
11:Light Bar	11: LB_LED

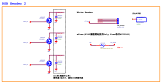
4.外接一組燈條的情境

5.兩組燈條以上的情境

RGB Header 1



RGB Header 2



6.外接LED燈板的情境

(5pin)

請確認燈板是否有接MOS至LED燈上

LED connector 命名規則：

請參照以下方式命名

位置	命名
0: CPU	0: CPU_CON
1: VRM	1: VRM_CON
2: NB	2: NB_CON
3: PCH	3: PCH_CON
4: Audio	4: AUD_CON
5: Back IO	5: BAKIO_CON
6: Back Plate	6: BAP_CON
7: PCIE	7: PCIE_CON
8: PCB Surround	8: MB_CON
9: M.2	9: M.2_CON
10:Start/retry Button	10: STN_CON
11:Light Bar	11: LB_CON

Connector 使用的 Cable料號 (5pin)

14011-00770100 96mm 黑色塑膠HD
14011-00770200 200mm 黑色塑膠HD
14011-00770300 160mm 醋酸膠布
14011-00770500 50mm 醋酸膠布
14011-00770400 130mm 醋酸膠布
14011-00770600 130mm 熱縮套管
14011-00770700 70mm 熱縮套管

1.LED個數 < 4個 的接線方式 (接線需求選擇LED個數及個數，不需要部分接線除)

Key Note LED個數接線與命名及說明
WARNING Note: Pins marked * are PWM

LED個數外命名

LED個數命名規則:

請參照以下方式命名

位置	命名
0. CPU	0. CPU_LED
1. VRM	1. VRM_LED
2. DRAM	2. DRAM_LED
3. PCH	3. PCH_LED
4. Audio	4. AUDIO_LED
5. Rear IO	5. REAR_IO_LED
6. Back Plate	6. BAK_LED
7. PCIE	7. PCIE_LED
8. PCH Surround	8. PCH_LED
9. M.2	9. M.2_LED
10. Start/setey Button	10. SSB_LED
11 Light Bar	11. LB_Tab

2.LED個數大於4個, 但不超過10顆的接線方式 (接線需求選擇或超過LED個數及個數)

3.LED個數大於10個 (接線需求選擇LED個數及個數，不需要部分接線除)

1.LED個數 < 4顆 的接線方式

(請依需求選擇LED個數及顏色，不需要部分接線跳)

LED個數命名

LED個數命名規則：

請參照以下方式命名

位置	命名
0. CPU	0. CPU_LED
1. VRM	1. VRM_LED
2. DRAM	2. DR_LED
3. PCH	3. PCH_LED
4. Audio	4. AUD_LED
5. Super IO	5. SIO_LED
6. Back Plate	6. BAP_LED
7. PCIE	7. PCIE_LED
8. PCH Surround	8. PCH_S_LED
9. Logo	9. MB_T_LED
10. Start/setup Button	10. STB_LED
11.Light Bar	11. LB_LED

2.LED個數大於4顆，但不超過20顆的接線方式

(請依需求選擇或跳過LED個數及顏色)

COVER_h1
1
C118D118N
/X

COVER_h3
1
C118D118N
/X

COVER_h2
1
C118D118N
/X

COVER_h4
1
C118D118N
/X

COVER_h5
1
C118D118N
/X

COVER_h6
1
C118D118N
/X

COVER_h7
1
C126D126N
/X

COVER_h10
1
O126X138DO126X138N
/X

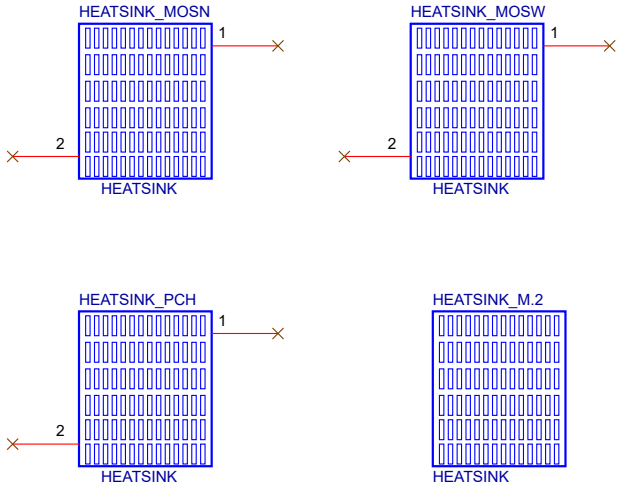
COVER_h8
1
C126D126N
/X

COVER_h11
1
O126X138DO126X138N
/X

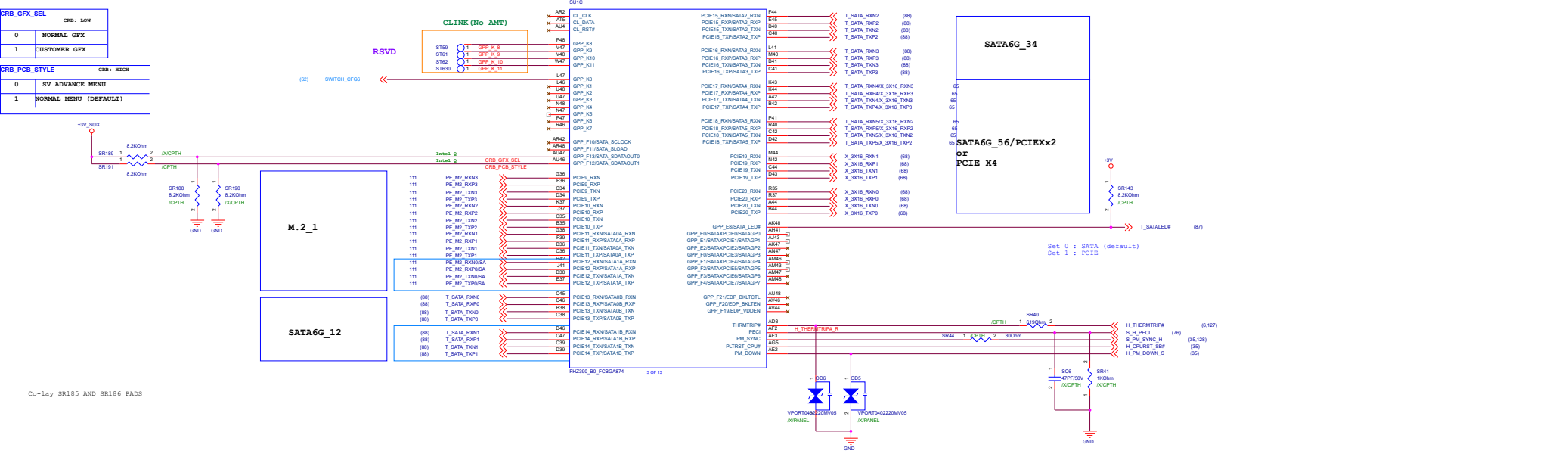
COVER_h9
1
C126D126N
/X

COVER_h12
1
O126X138DO126X138N
/X

Z390-A



Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, July 24, 2018	Sheet 1 of 1	



Title	CPTH (HOST/FAN/SATA)		
ASUSTek Computer Inc.	Engineer: Aaron_Su		
Size: A2	Project Name: Z390 Golden board		Rev: R1.01
Date: Tuesday, July 24, 2018	Sheet 44 of 130		