PCB Number: 15139-1
ECO# number: ?

PCB BOARD SIZE
4 Layers
170mm x200mm

Intel Apollo Lake Platform

LAN: RTL8111GA
AUDIO: ALC662
DP to VGA: RTD2166
ECIO: ITE8739E

BOM Configuration
(R_):Unmount
(PSU_): PSU SKU
(ADP_): ADP SKU
(1D8VS0_):1D8V_S0
(O_): OCP
(NOOCP_) : ADP & No OCP
(O6_) : 65W adapter OCP
(O9_) : 90W adapter OCP
(DEBUG_) : debug
(FUSB3_): Front USB3.0
(COM_): COM port function
(TPM_): TPM Header
(N_): RJ45 connector without surge
(S_): RJ45 connector with surge

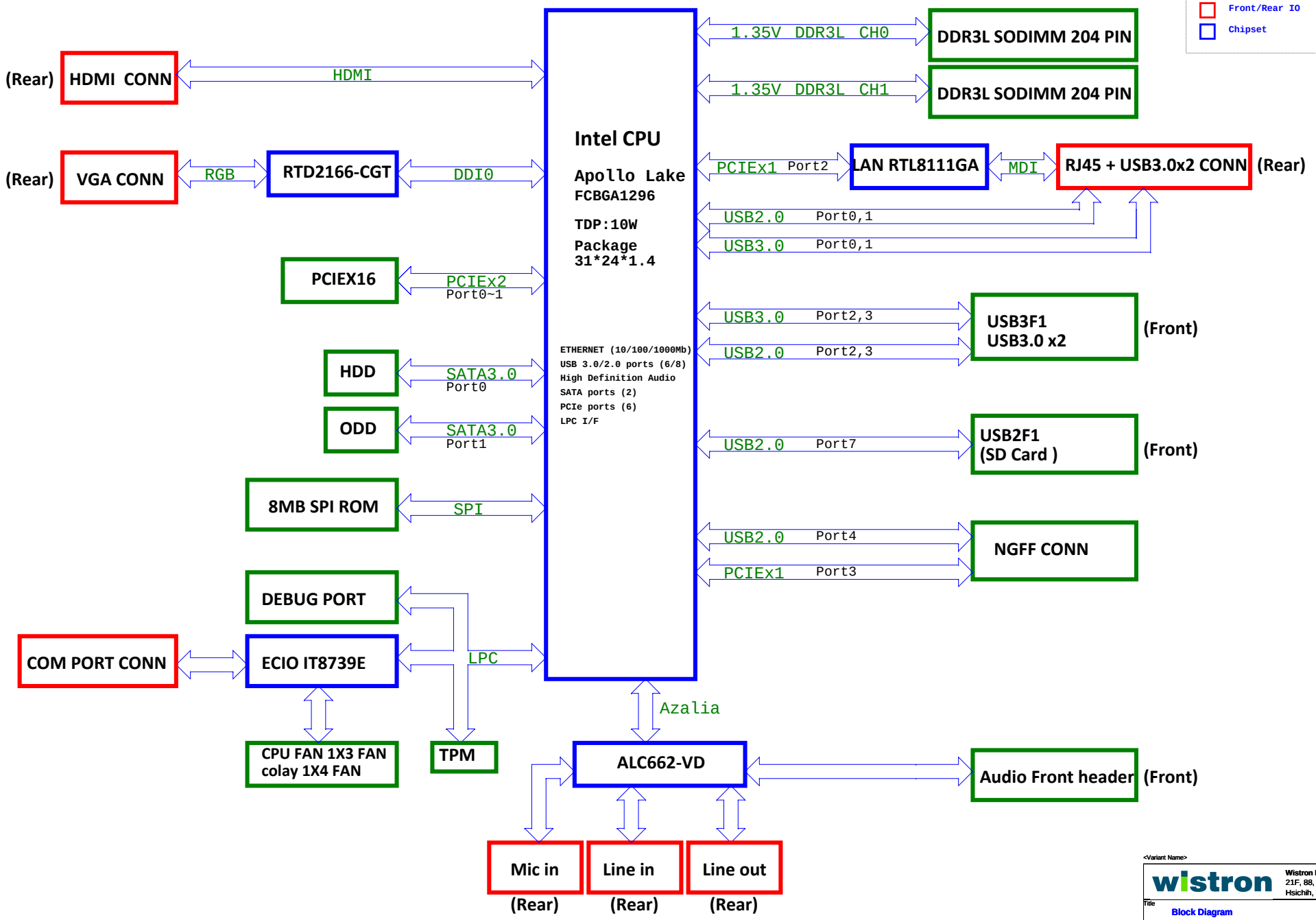
<Variant Name>

wistron
Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Cover Page
Size: Custom | Document Number: Adma_APL | Rev: SA
Date: Monday, August 08, 2016 | Sheet 1 of 105

Project Name: Adam
Project Code: 3PD06R010001
PCB Version: 1A
PCB Number:15139

PCB BOARD SIZE
4 Layer
Internal Slot/Header
Front/Rear IO
Chipset



<Variant Name>

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21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: Block Diagram
Size: C
Document Number: Adma_APL
Rev: SA
Date: Monday, August 08, 2016
Sheet 2 of 105

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Size	Document Number	Rev
A	Adma_APL	SA

Date: Monday, August 08, 2016 Sheet 4 of 105

SSID = CPU

Space/Width = 15/15 mils

CPU1A — 1 OF 22 — APL_SOC — APOLLO-LAKE-GP-U

M_A_DQ0	AY62	MEM_CH0_DQ0/MEM_CH0_DQA0	
M_A_DQ1	AY61	MEM_CH0_DQ1/MEM_CH0_DQA1	
M_A_DQ2	BE62	MEM_CH0_DQ2/MEM_CH0_DQA2	
M_A_DQ3	BG62	MEM_CH0_DQ3/MEM_CH0_DQA3	
M_A_DQ4	BD63	MEM_CH0_DQ4/MEM_CH0_DQA4	
M_A_DQ5	AW62	MEM_CH0_DQ5/MEM_CH0_DQA5	
M_A_DQ6	AW63	MEM_CH0_DQ6/MEM_CH0_DQA6	
M_A_DQ7	BD62	MEM_CH0_DQ7/MEM_CH0_DQA7	
M_A_DQ8	AY59	MEM_CH0_DQ8/MEM_CH0_DQA8	
M_A_DQ9	AU63	MEM_CH0_DQ9/MEM_CH0_DQA9	
M_A_DQ10	AU62	MEM_CH0_DQ10/MEM_CH0_DQA10	
M_A_DQ11	AV58	MEM_CH0_DQ11/MEM_CH0_DQA11	
M_A_DQ12	AV57	MEM_CH0_DQ12/MEM_CH0_DQA12	
M_A_DQ13	AT55	MEM_CH0_DQ13/MEM_CH0_DQA13	
M_A_DQ14	AT54	MEM_CH0_DQ14/MEM_CH0_DQA14	
M_A_DQ15	AY59	MEM_CH0_DQ15/MEM_CH0_DQA15	
M_A_DQ16	AV57	MEM_CH0_DQ16/MEM_CH0_DQA16	
M_A_DQ17	BB57	MEM_CH0_DQ17/MEM_CH0_DQA17	
M_A_DQ18	BD59	MEM_CH0_DQ18/MEM_CH0_DQA18	
M_A_DQ19	BF59	MEM_CH0_DQ19/MEM_CH0_DQA19	
M_A_DQ20	AV54	MEM_CH0_DQ20/MEM_CH0_DQA20	
M_A_DQ21	AY59	MEM_CH0_DQ21/MEM_CH0_DQA21	
M_A_DQ22	AV52	MEM_CH0_DQ22/MEM_CH0_DQA22	
M_A_DQ23	BD58	MEM_CH0_DQ23/MEM_CH0_DQA23	
M_A_DQ24	BE56	MEM_CH0_DQ24/MEM_CH0_DQA24	
M_A_DQ25	BD54	MEM_CH0_DQ25/MEM_CH0_DQA25	
M_A_DQ26	BF58	MEM_CH0_DQ26/MEM_CH0_DQA26	
M_A_DQ27	BE50	MEM_CH0_DQ27/MEM_CH0_DQA27	
M_A_DQ29	BB50	MEM_CH0_DQ29/MEM_CH0_DQA29	
M_A_DQ28	BD50	MEM_CH0_DQ28/MEM_CH0_DQA28	
M_A_DQ30	BA50	MEM_CH0_DQ30/MEM_CH0_DQA30	
M_A_DQ31	BB54	MEM_CH0_DQ31/MEM_CH0_DQA31	
		MEM_CH0_DQ32/MEM_CH0_DQB0	AR39 M_A_DQ32
		MEM_CH0_DQ33/MEM_CH0_DQB1	AV37 M_A_DQ33
		MEM_CH0_DQ34/MEM_CH0_DQB2	AW37 M_A_DQ34
		MEM_CH0_DQ35/MEM_CH0_DQB3	AR37 M_A_DQ35
		MEM_CH0_DQ36/MEM_CH0_DQB4	AT37 M_A_DQ36
		MEM_CH0_DQ37/MEM_CH0_DQB5	AT41 M_A_DQ37
		MEM_CH0_DQ38/MEM_CH0_DQB6	AR41 M_A_DQ38
		MEM_CH0_DQ39/MEM_CH0_DQB7	AW35 M_A_DQ39
		MEM_CH0_DQ40/MEM_CH0_DQB8	BJ44 M_A_DQ40
		MEM_CH0_DQ41/MEM_CH0_DQB9	BG39 M_A_DQ41
		MEM_CH0_DQ42/MEM_CH0_DQB10	BG40 M_A_DQ42
		MEM_CH0_DQ43/MEM_CH0_DQB11	BJ40 M_A_DQ43
		MEM_CH0_DQ44/MEM_CH0_DQB12	BG43 M_A_DQ44
		MEM_CH0_DQ45/MEM_CH0_DQB13	BG44 M_A_DQ45
		MEM_CH0_DQ46/MEM_CH0_DQB14	BH45 M_A_DQ46
		MEM_CH0_DQ47/MEM_CH0_DQB15	BH41 M_A_DQ47
		MEM_CH0_DQ48/MEM_CH0_DQB16	BA34 M_A_DQ48
		MEM_CH0_DQ49/MEM_CH0_DQB17	BE34 M_A_DQ49
		MEM_CH0_DQ50/MEM_CH0_DQB18	BD34 M_A_DQ50
		MEM_CH0_DQ51/MEM_CH0_DQB19	BD37 M_A_DQ51
		MEM_CH0_DQ52/MEM_CH0_DQB20	BB37 M_A_DQ52
		MEM_CH0_DQ53/MEM_CH0_DQB21	BE39 M_A_DQ53
		MEM_CH0_DQ54/MEM_CH0_DQB22	BD39 M_A_DQ54
		MEM_CH0_DQ55/MEM_CH0_DQB23	BB34 M_A_DQ55
		MEM_CH0_DQ56/MEM_CH0_DQB24	BJ38 M_A_DQ56
		MEM_CH0_DQ57/MEM_CH0_DQB25	BG34 M_A_DQ57
		MEM_CH0_DQ58/MEM_CH0_DQB26	BG33 M_A_DQ58
		MEM_CH0_DQ59/MEM_CH0_DQB27	BH33 M_A_DQ59
		MEM_CH0_DQ60/MEM_CH0_DQB28	BG38 M_A_DQ60
		MEM_CH0_DQ61/MEM_CH0_DQB29	BH37 M_A_DQ61
		MEM_CH0_DQ62/MEM_CH0_DQB30	BG37 M_A_DQ62
		MEM_CH0_DQ63/MEM_CH0_DQB31	BJ34 M_A_DQ63

M_A_DQ[63:0] 12

M_A_A[15:0] 12 — M_A_A5, M_A_A6, M_A_A7, M_A_A8, M_A_A9, M_A_A10, M_A_A11, M_A_A12, M_A_A13, M_A_A14, M_A_A15

M_A_DQS_DN[7:0] 12 — M_A_DQS_DN0, M_A_DQS_DN1, M_A_DQS_DN2, M_A_DQS_DN3, M_A_DQS_DN4, M_A_DQS_DN5, M_A_DQS_DN6, M_A_DQS_DN7

M_A_DQS_DP[7:0] 12 — M_A_DQS_DP0, M_A_DQS_DP1, M_A_DQS_DP2, M_A_DQS_DP3, M_A_DQS_DP4, M_A_DQS_DP5, M_A_DQS_DP6, M_A_DQS_DP7

CPU1B — 2 OF 22 — APL_SOC

M_A_DQS_DP0	BB63	MEM_CH0_DQSP0/MEM_CH0_DQSPA0	
M_A_DQS_DN0	BC62	MEM_CH0_DQSN0/MEM_CH0_DQSNA0	
M_A_DQS_DP1	AT59	MEM_CH0_DQSP1/MEM_CH0_DQSPA1	
M_A_DQS_DN1	AT58	MEM_CH0_DQSN1/MEM_CH0_DQSNA1	
M_A_DQS_DP2	BB59	MEM_CH0_DQSP2/MEM_CH0_DQSPA2	
M_A_DQS_DN2	BB58	MEM_CH0_DQSN2/MEM_CH0_DQSNA2	
M_A_DQS_DP3	BD57	MEM_CH0_DQSP3/MEM_CH0_DQSPA3	
M_A_DQS_DN3	BB52	MEM_CH0_DQSN3/MEM_CH0_DQSNA3	
M_A_DQS_DP4	AV39	MEM_CH0_DQSP4/MEM_CH0_DQSPB0	
M_A_DQS_DN4	AW39	MEM_CH0_DQSN4/MEM_CH0_DQSNB0	
M_A_DQS_DP5	BJ42	MEM_CH0_DQSP5/MEM_CH0_DQSPB1	
M_A_DQS_DN5	BG42	MEM_CH0_DQSN5/MEM_CH0_DQSNB1	
M_A_DQS_DP6	BB35	MEM_CH0_DQSP6/MEM_CH0_DQSPB2	
M_A_DQS_DN6	BD35	MEM_CH0_DQSN6/MEM_CH0_DQSNB2	
M_A_DQS_DP7	BG36	MEM_CH0_DQSP7/MEM_CH0_DQSPB3	
M_A_DQS_DN7	BH35	MEM_CH0_DQSN7/MEM_CH0_DQSNB3	
M_A_A0	BG50	MEM_CH0_MA0/MEM_CH0_CAB7	
M_A_A1	BG51	MEM_CH0_MA1/MEM_CH0_CAB9	
M_A_A2	BH51	MEM_CH0_MA2/MEM_CH0_CAB5	
M_A_A3	BD41	MEM_CH0_MA3/NCTF_22	
M_A_A4	BE41	MEM_CH0_MA4/NCTF_23	
M_A_A5	BJ52	MEM_CH0_MA5/MEM_CH0_CAA2	
M_A_A6	BG53	MEM_CH0_MA6/MEM_CH0_CAA0	
M_A_A7	BG55	MEM_CH0_MA7/MEM_CH0_CAA3	
M_A_A8	BH53	MEM_CH0_MA8/MEM_CH0_CAA1	
M_A_A9	BG52	MEM_CH0_MA9/MEM_CH0_CAA4	
M_A_A10	BH49	MEM_CH0_MA10/MEM_CH0_CAB6	
M_A_A11	BH55	MEM_CH0_MA11/MEM_CH0_CAA6	
M_A_A12	BG54	MEM_CH0_MA12/MEM_CH0_CAA5	
M_A_A13	BG46	MEM_CH0_MA13/MEM_CH0_CAB0	
M_A_A14	BG56	MEM_CH0_MA14/MEM_CH0_CAA8	
M_A_A15	BG57	MEM_CH0_MA15/MEM_CH0_CAA9	
		MEM_CH0_VREFCA	AR35
		MEM_CH0_VREFDQ	AT34
		MEM_CH0_BA0/MEM_CH0_CAB2	BJ48 M_A_BS0 12
		MEM_CH0_BA1/MEM_CH0_CAB3	BG49 M_A_BS1 12
		MEM_CH0_BA2/MEM_CH0_CAA7	BH57 M_A_BS2 12
		MEM_CH0_ODT0/MEM_CH0_ODTA	AW43 M_A_ODT0 12
		MEM_CH0_ODT1/MEM_CH0_ODTB	AW41 M_A_ODT1 12
		MEM_CH0_CAS#/MEM_CH0_CAB1	BH47 M_A_CAS# 12
		MEM_CH0_WE#/MEM_CH0_CAB4	BG48 M_A_WE# 12
		MEM_CH0_RAS#/MEM_CH0_CAB3	BG47 M_A_RAS# 12
		NCTF/MEM_CH0_CS1A#	AT43
		NCTF/MEM_CH0_CS0B#	BB41
		MEM_CH0_CS1#/MEM_CH0_CS1B#	BA41 M_A_CS#1 12
		MEM_CH0_CS0#/MEM_CH0_CS0A#	AR43 M_A_CS#0 12
		MEM_CH0_CLKP1/MEM_CH0_CLKP_A	BB48 M_A_CLK1 12
		MEM_CH0_CLKN1/MEM_CH0_CLKN_A	BD48 M_A_CLK#1 12
		MEM_CH0_CLKP0/MEM_CH0_CLKP_B	BD45 M_A_CLK0 12
		MEM_CH0_CLKN0/MEM_CH0_CLKN_B	BE45 M_A_CLK#0 12
		MEM_CH0_CKE0/MEM_CH0_CKE0A	BH61 M_A_CKE0 12
		MEM_CH0_CKE1/MEM_CH0_CKE1A	BH60 M_A_CKE1 12
		NCTF/MEM_CH0_CKE0B	BH58
		NCTF/MEM_CH0_CKE1B	BJ56
		MEM_CH1_RESET#/NCTF_33	AR30 M_B_DRAMRST# 13
		MEM_CH0_RESET#/NCTF_33	AR34 M_A_DRAMRST# 12
		MEM_CH0_DQSP8/NCTF_28	BD47
		MEM_CH0_DQSN8/NCTF_30	BB47
		MEM_CH0_CB7/NCTF_35	BA45
		MEM_CH0_CB6/NCTF_34	BD43
		MEM_CH0_CB5/NCTF_32	AY43
		MEM_CH0_CB4/NCTF_29	AY48
		MEM_CH0_CB3/NCTF_27	AW49
		MEM_CH0_CB2/NCTF_26	BB43
		MEM_CH0_CB1/NCTF_25	AW47
		MEM_CH0_CB0/NCTF_24	AW45

Space/Width = 15/15 mils

CPU1C — 2 OF 22 — APL_SOC — APOLLO-LAKE-GP-U

M_B_DQ0	BJ26	MEM_CH1_DQ0/MEM_CH1_DQA0	
M_B_DQ1	BG30	MEM_CH1_DQ1/MEM_CH1_DQA1	
M_B_DQ2	BH31	MEM_CH1_DQ2/MEM_CH1_DQA2	
M_B_DQ3	BG31	MEM_CH1_DQ3/MEM_CH1_DQA3	
M_B_DQ4	BH27	MEM_CH1_DQ4/MEM_CH1_DQA4	
M_B_DQ5	BG27	MEM_CH1_DQ5/MEM_CH1_DQA5	
M_B_DQ6	BG26	MEM_CH1_DQ6/MEM_CH1_DQA6	
M_B_DQ7	BJ30	MEM_CH1_DQ7/MEM_CH1_DQA7	
M_B_DQ8	BA30	MEM_CH1_DQ8/MEM_CH1_DQA8	
M_B_DQ9	BB30	MEM_CH1_DQ9/MEM_CH1_DQA9	
M_B_DQ10	BE30	MEM_CH1_DQ10/MEM_CH1_DQA10	
M_B_DQ11	BD30	MEM_CH1_DQ11/MEM_CH1_DQA11	
M_B_DQ12	BE25	MEM_CH1_DQ12/MEM_CH1_DQA12	
M_B_DQ13	BB27	MEM_CH1_DQ13/MEM_CH1_DQA13	
M_B_DQ14	BD25	MEM_CH1_DQ14/MEM_CH1_DQA14	
M_B_DQ15	BD27	MEM_CH1_DQ15/MEM_CH1_DQA15	
M_B_DQ16	BG24	MEM_CH1_DQ16/MEM_CH1_DQA16	
M_B_DQ17	BJ20	MEM_CH1_DQ17/MEM_CH1_DQA17	
M_B_DQ18	BH23	MEM_CH1_DQ18/MEM_CH1_DQA18	
M_B_DQ19	BJ24	MEM_CH1_DQ19/MEM_CH1_DQA19	
M_B_DQ20	BG20	MEM_CH1_DQ20/MEM_CH1_DQA20	
M_B_DQ21	BG21	MEM_CH1_DQ21/MEM_CH1_DQA21	
M_B_DQ22	BH19	MEM_CH1_DQ22/MEM_CH1_DQA22	
M_B_DQ23	BG25	MEM_CH1_DQ23/MEM_CH1_DQA23	
M_B_DQ24	AT27	MEM_CH1_DQ24/MEM_CH1_DQA24	
M_B_DQ25	AW29	MEM_CH1_DQ25/MEM_CH1_DQA25	
M_B_DQ26	AR27	MEM_CH1_DQ26/MEM_CH1_DQA26	
M_B_DQ27	AT23	MEM_CH1_DQ27/MEM_CH1_DQA27	
M_B_DQ28	AV27	MEM_CH1_DQ28/MEM_CH1_DQA28	
M_B_DQ29	AR25	MEM_CH1_DQ29/MEM_CH1_DQA29	
M_B_DQ30	AR23	MEM_CH1_DQ30/MEM_CH1_DQA30	
M_B_DQ31	AW27	MEM_CH1_DQ31/MEM_CH1_DQA31	
		MEM_CH1_DQ32/MEM_CH1_DQB0	BF6 M_B_DQ32
		MEM_CH1_DQ33/MEM_CH1_DQB1	BD10 M_B_DQ33
		MEM_CH1_DQ34/MEM_CH1_DQB2	BE14 M_B_DQ34
		MEM_CH1_DQ35/MEM_CH1_DQB3	BB10 M_B_DQ35
		MEM_CH1_DQ36/MEM_CH1_DQB4	BA14 M_B_DQ36
		MEM_CH1_DQ37/MEM_CH1_DQB5	BB14 M_B_DQ37
		MEM_CH1_DQ38/MEM_CH1_DQB6	BD14 M_B_DQ38
		MEM_CH1_DQ39/MEM_CH1_DQB7	BE8 M_B_DQ39
		MEM_CH1_DQ40/MEM_CH1_DQB8	AV12 M_B_DQ40
		MEM_CH1_DQ41/MEM_CH1_DQB9	BD6 M_B_DQ41
		MEM_CH1_DQ42/MEM_CH1_DQB10	BD5 M_B_DQ42
		MEM_CH1_DQ43/MEM_CH1_DQB11	BB7 M_B_DQ43
		MEM_CH1_DQ44/MEM_CH1_DQB12	AV10 M_B_DQ44
		MEM_CH1_DQ45/MEM_CH1_DQB13	AY9 M_B_DQ45
		MEM_CH1_DQ46/MEM_CH1_DQB14	AV7 M_B_DQ46
		MEM_CH1_DQ47/MEM_CH1_DQB15	BF5 M_B_DQ47
		MEM_CH1_DQ48/MEM_CH1_DQB16	AU2 M_B_DQ48
		MEM_CH1_DQ49/MEM_CH1_DQB17	AT10 M_B_DQ49
		MEM_CH1_DQ50/MEM_CH1_DQB18	AT9 M_B_DQ50
		MEM_CH1_DQ51/MEM_CH1_DQB19	AU5 M_B_DQS1
		MEM_CH1_DQ52/MEM_CH1_DQB20	AY5 M_B_DQ52
		MEM_CH1_DQ53/MEM_CH1_DQB21	AV5 M_B_DQ53
		MEM_CH1_DQ54/MEM_CH1_DQB22	AV6 M_B_DQ54
		MEM_CH1_DQ55/MEM_CH1_DQB23	AV7 M_B_DQ55
		MEM_CH1_DQ56/MEM_CH1_DQB24	AY2 M_B_DQ56
		MEM_CH1_DQ57/MEM_CH1_DQB25	BD2 M_B_DQ57
		MEM_CH1_DQ58/MEM_CH1_DQB26	BD1 M_B_DQ58
		MEM_CH1_DQ59/MEM_CH1_DQB27	BE2 M_B_DQ59
		MEM_CH1_DQ60/MEM_CH1_DQB28	AW1 M_B_DQ60
		MEM_CH1_DQ61/MEM_CH1_DQB29	AW2 M_B_DQS1
		MEM_CH1_DQ62/MEM_CH1_DQB30	AY3 M_B_DQ62
		MEM_CH1_DQ63/MEM_CH1_DQB31	BG2 M_B_DQ63

M_B_DQ[63:0] 13 (071.APOLL.0000)

M_B_A[15:0] 13 — M_B_A0, M_B_A1, M_B_A2, M_B_A3, M_B_A4, M_B_A5, M_B_A6, M_B_A7, M_B_A8, M_B_A9, M_B_A10, M_B_A11, M_B_A12, M_B_A13, M_B_A14, M_B_A15

M_B_DQS_DN[7:0] 13 — M_B_DQS_DN0, M_B_DQS_DN1, M_B_DQS_DN2, M_B_DQS_DN3, M_B_DQS_DN4, M_B_DQS_DN5, M_B_DQS_DN6, M_B_DQS_DN7

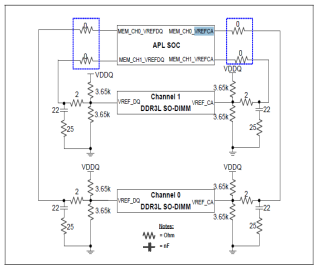
M_B_DQS_DP[7:0] 13 — M_B_DQS_DP0, M_B_DQS_DP1, M_B_DQS_DP2, M_B_DQS_DP3, M_B_DQS_DP4, M_B_DQS_DP5, M_B_DQS_DP6, M_B_DQS_DP7

CPU1D — 4 OF 23 — APL_SOC — APOLLO-LAKE-GP-U

M_B_DQS_DP0	BG28	MEM_CH1_DQSP0/MEM_CH1_DQSPA0	
M_B_DQS_DN0	BH29	MEM_CH1_DQSN0/MEM_CH1_DQSNA0	
M_B_DQS_DP1	BD29	MEM_CH1_DQSP1/MEM_CH1_DQSPA1	
M_B_DQS_DN1	BB29	MEM_CH1_DQSN1/MEM_CH1_DQSNA1	
M_B_DQS_DP2	BJ22	MEM_CH1_DQSP2/MEM_CH1_DQSPA2	
M_B_DQS_DN2	BG22	MEM_CH1_DQSN2/MEM_CH1_DQSNA2	
M_B_DQS_DP3	AY25	MEM_CH1_DQSP3/MEM_CH1_DQSPA3	
M_B_DQS_DN3	AW25	MEM_CH1_DQSN3/MEM_CH1_DQSNA3	
M_B_DQS_DP4	BB12	MEM_CH1_DQSP4/MEM_CH1_DQSPB0	
M_B_DQS_DN4	BD12	MEM_CH1_DQSN4/MEM_CH1_DQSNB0	
M_B_DQS_DP5	BB5	MEM_CH1_DQSP5/MEM_CH1_DQSPB1	
M_B_DQS_DN5	BB6	MEM_CH1_DQSN5/MEM_CH1_DQSNB1	
M_B_DQS_DP6	AT5	MEM_CH1_DQSP6/MEM_CH1_DQSPB2	
M_B_DQS_DN6	AT6	MEM_CH1_DQSN6/MEM_CH1_DQSNB2	
M_B_DQS_DP7	BC2	MEM_CH1_DQSP7/MEM_CH1_DQSPB3	
M_B_DQS_DN7	BB1	MEM_CH1_DQSN7/MEM_CH1_DQSNB3	
M_B_A0	BG9	MEM_CH1_MA0/MEM_CH1_CAB7	
M_B_A1	BG10	MEM_CH1_MA1/MEM_CH1_CAB9	
M_B_A2	BH9	MEM_CH1_MA2/MEM_CH1_CAB5	
M_B_A3	BD16	MEM_CH1_MA3/NCTF_1	
M_B_A4	BB16	MEM_CH1_MA4/NCTF_2	
M_B_A5	BG11	MEM_CH1_MA5/MEM_CH1_CAA2	
M_B_A6	BJ12	MEM_CH1_MA6/MEM_CH1_CAA0	
M_B_A7	BG14	MEM_CH1_MA7/MEM_CH1_CAA3	
M_B_A8	BG12	MEM_CH1_MA8/MEM_CH1_CAA1	
M_B_A9	BH11	MEM_CH1_MA9/MEM_CH1_CAA4	
M_B_A10	BG7	MEM_CH1_MA10/MEM_CH1_CAB6	
M_B_A11	BH13	MEM_CH1_MA11/MEM_CH1_CAA6	
M_B_A12	BG13	MEM_CH1_MA12/MEM_CH1_CAA5	
M_B_A13	BH3	MEM_CH1_MA13/MEM_CH1_CAB0	
M_B_A14	BG15	MEM_CH1_MA14/MEM_CH1_CAA8	
M_B_A15	BG16	MEM_CH1_MA15/MEM_CH1_CAA9	
		MEM_CH1_VREFDQ	AT35
		MEM_CH1_VREFCA	AR29
		MEM_CH1_BA0/MEM_CH1_CAB2	BH6 M_B_BS0 13
		MEM_CH1_BA1/MEM_CH1_CAB8	BG8 M_B_BS1 13
		MEM_CH1_BA2/MEM_CH1_CAA7	BH15 M_B_BS2 13
		MEM_CH1_RAS#/MEM_CH1_CAB3	BJ8 M_B_RAS# 13
		MEM_CH1_CAS#/MEM_CH1_CAB1	BH4 M_B_CAS# 13
		MEM_CH1_WE#/MEM_CH1_CAB4	BH7 M_B_WE# 13
		MEM_CH1_ODT0/MEM_CH1_ODTA	AW16 M_B_ODT0 13
		MEM_CH1_ODT1/MEM_CH1_ODTB	AV16 M_B_ODT1 13
		MEM_CH1_CLKP1/MEM_CH1_CLKP_A	BB21 M_B_CLK1 13
		MEM_CH1_CLKN1/MEM_CH1_CLKN_A	BD21 M_B_CLK#1 13
		MEM_CH1_CLKP0/MEM_CH1_CLKP_B	BD19 M_B_CLK0 13
		MEM_CH1_CLKN0/MEM_CH1_CLKN_B	BE19 M_B_CLK#0 13
		MEM_CH1_CKE0/MEM_CH1_CKE0A	BG18 M_B_CKE0 13
		MEM_CH1_CKE1/MEM_CH1_CKE1A	BG17 M_B_CKE1 13
		NCTF/MEM_CH1_CKE0B	BH17
		NCTF/MEM_CH1_CKE1B	BJ16
		MEM_CH1_CS0#/MEM_CH1_CS0A#	BD17 M_B_CS#0 13
		MEM_CH1_CS1#/MEM_CH1_CS1B#	AW17 M_B_CS#1 13
		NCTF/MEM_CH1_CS0B#	AV17
		NCTF/MEM_CH1_CS1A#	BB17
		MEM_CH1_DQSN8/NCTF_9	BE23
		MEM_CH1_DQSP8/NCTF_5	BD23
		MEM_CH1_CB0/NCTF_3	AR21
		MEM_CH1_CB1/NCTF_4	AT21
		MEM_CH1_CB6/NCTF_11	BA23
		MEM_CH1_CB3/NCTF_7	AW23
		MEM_CH1_CB4/NCTF_8	BA19
		MEM_CH1_CB5/NCTF_10	AW19
		MEM_CH1_CB7/NCTF_12	BB23
		MEM_CH1_CB2/NCTF_6	AW23

Follow MoW WW41

Figure 39. SODIMM DRAM_VREF Generation Example Circuit



NOTE: The 0 Ohm resistor should be un-stuffed by default.

<Variant Name>

wistron — Wistron Incorporated, 21F, 8B, Sec.1, Hsin Tai Wu Rd, Hsichih, Taipei Hsien

File: CPU_(DDR)

Size: A1 | Document Number: Adima_APL | Rev: 3A

Date: Monday, August 08, 2016 | Sheet 5 of 105

SSID = CPU

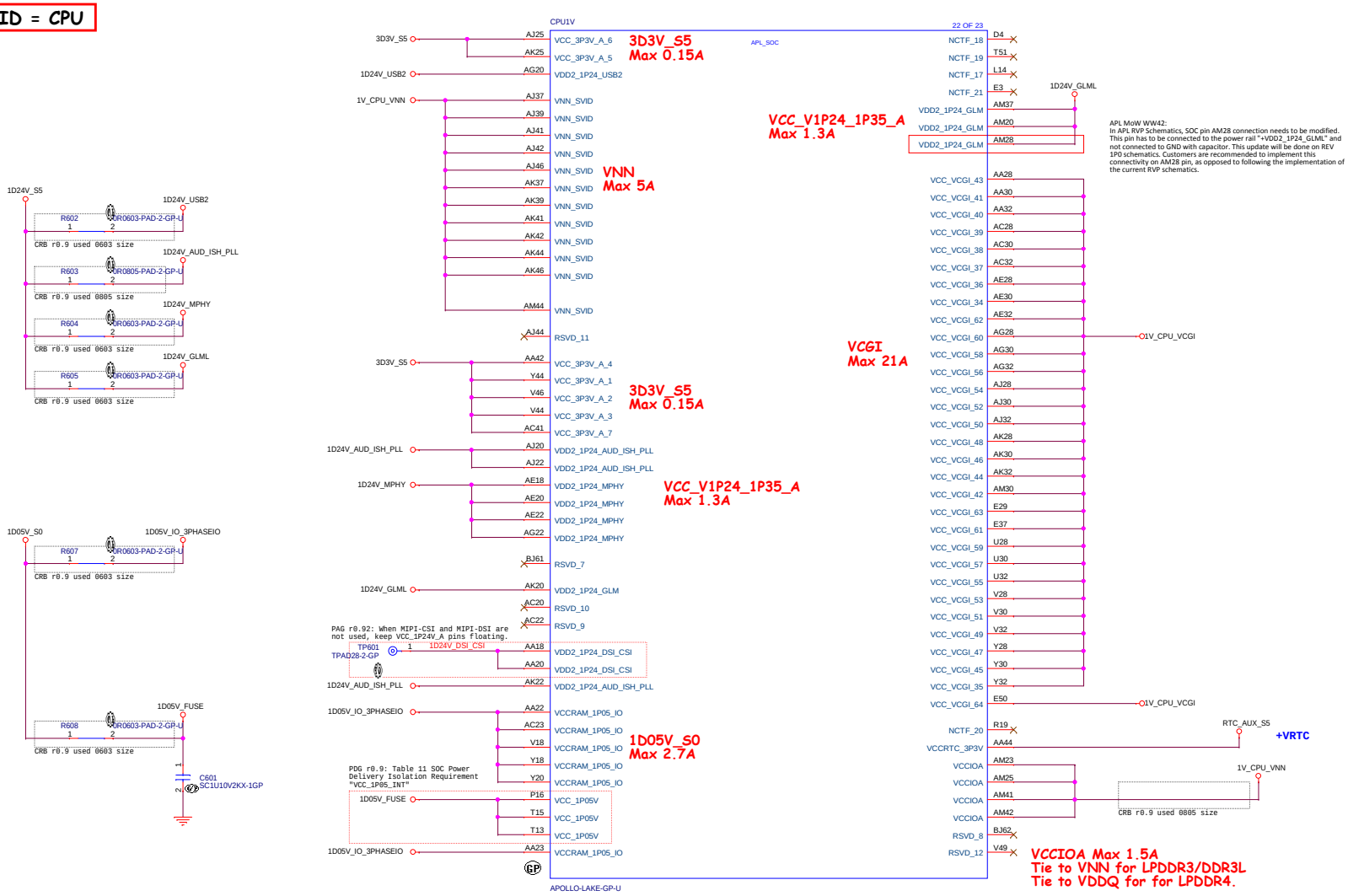


Table 5-3. Apollo Lake SoC Power Rail DC Specification and Iccmax

Power Type	Voltage Range (V)	Voltage Tolerance (AC+DC+Ripple)	Power Well Description	Iccmax (A)
VCC_VCGI	0.45–1.3	DC Load Line (DCLL) = TBD Ripple at Iccmax = +/-15mV TOB_Iccmax = +/-20mV Maximum overshoot voltage = 100mV Maximum overshoot duration = 50 µs	Variable voltage supply to CPU and Graphics Core and ISP logic	21
VNN	0.45–1.3	+/-50mV	Variable voltage supply to other (non core) logic	4.8
VCC_V1P05	1.05	+/-5%	Fixed voltage rail for SRAM and I/O Logic	2.7
VCC_V1P24_1P35_A	1.24V or 1.35V	+/- 5%	Fixed voltage rail for SoC L2, I/O Logic and PLLs **Note:** This rail must be 1.24V for Apollo Lake A0 step. Starting B-step, this rail can be 1.24V or 1.35V	1.3
VCC_V1P24_A	1.24	+/-5%	Fixed voltage rail for MIPI* I/Os	TBD
VCC_V1P8V_A	1.8	+/-5%	Fixed voltage rail for all GPIOs	0.4
VDDQ	1.35	+/-5%	Fixed voltage rail for DDR3L PHY	2.8 (excluding DRAM)
	1.24	+/-5%	Fixed voltage rail for LPDDR3 PHY	
VCC_3P3V_A	3.3	+/-5%	Fixed voltage rail for GPIO, I/O logic and USB2 PHY	0.15
VCC_RTC_3P3V	2–3.47	N/A	Fixed Voltage rail for RTC (Real Time Clock)	TBD

<Variant Name>

Wistron Incorporated
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Hsichih, Taipei Hsien

Title: CPU (VCCGI/VNN/Others)

Size: C | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 6 of 105

SSID = CPU

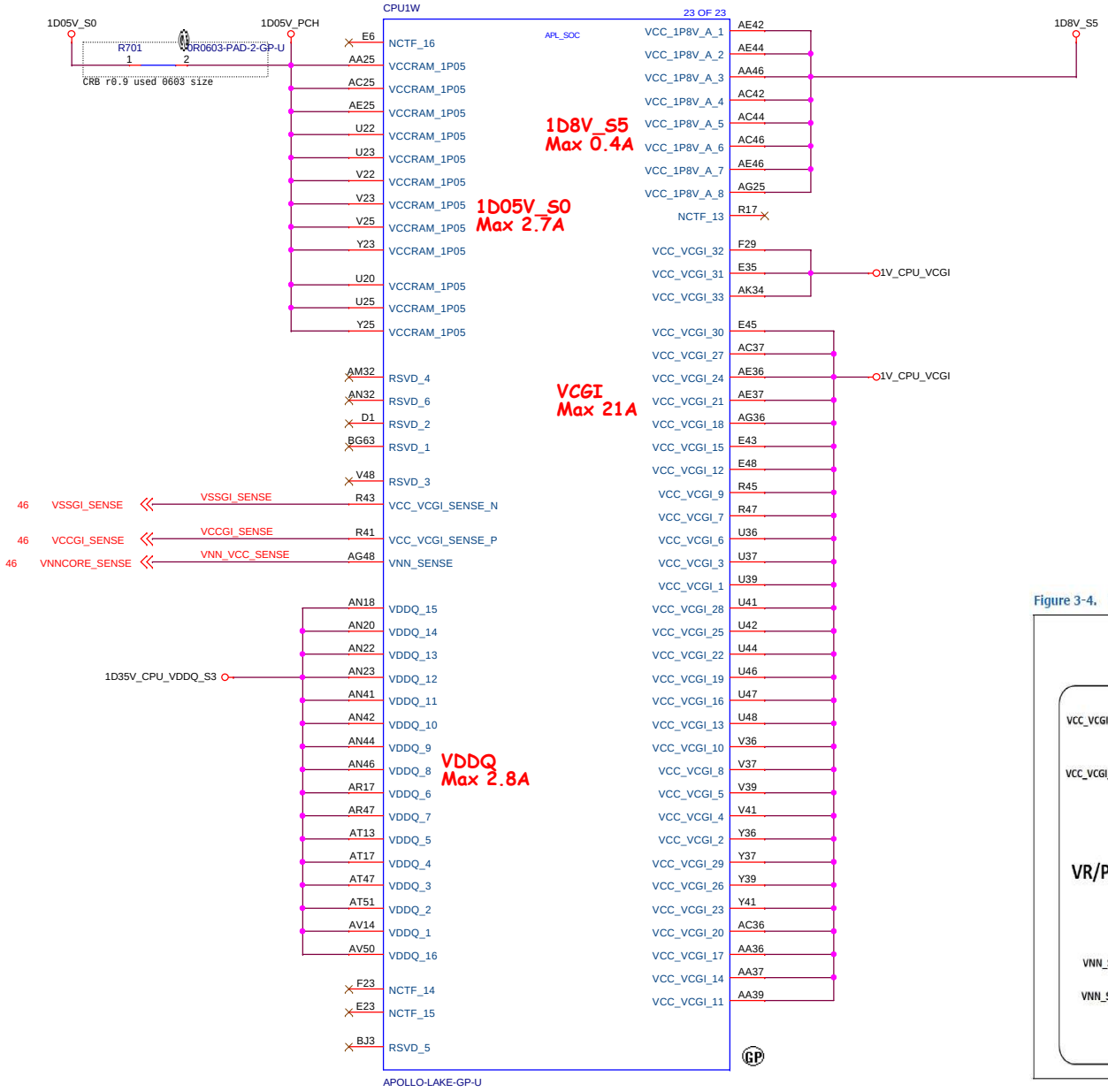
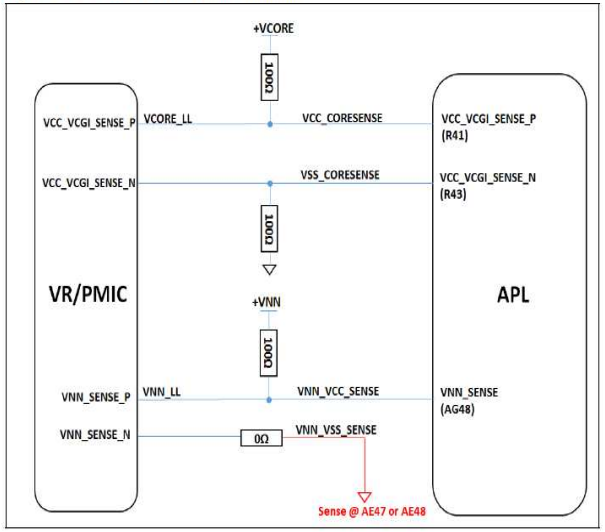
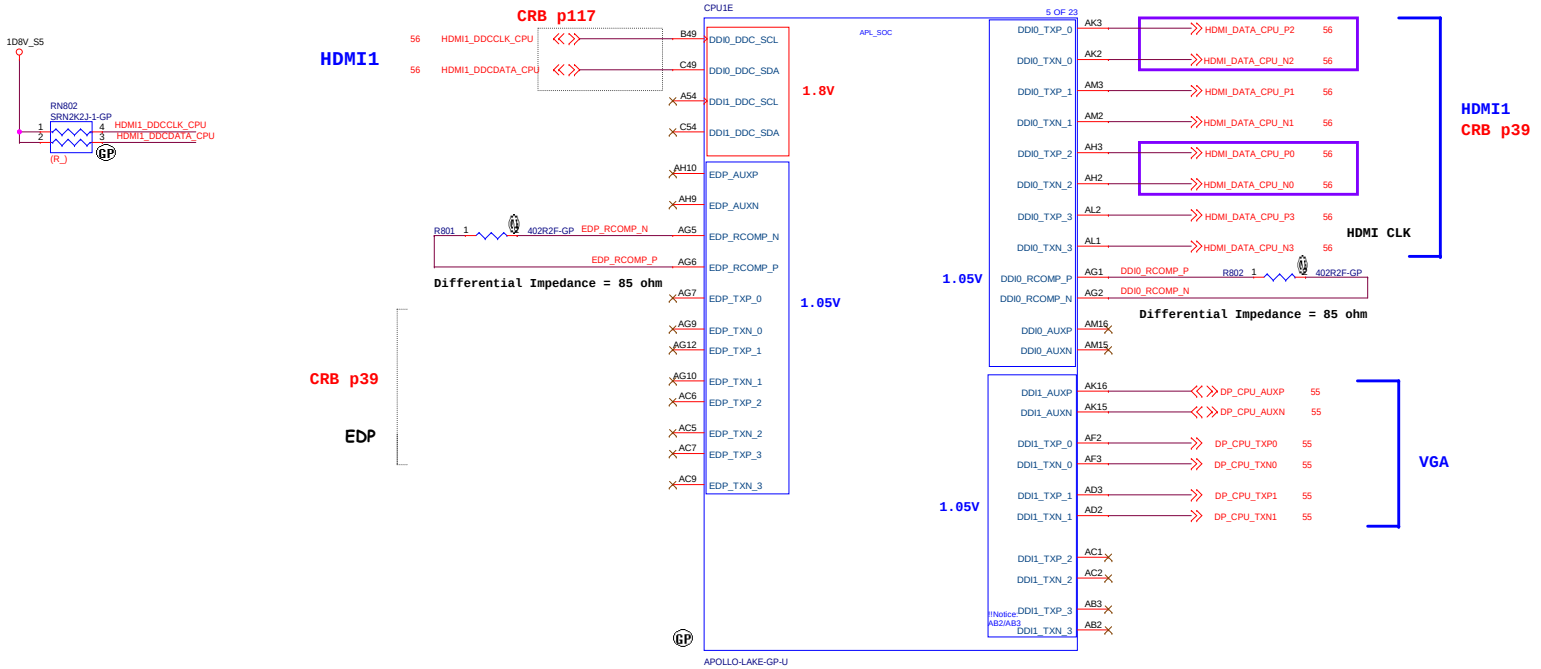


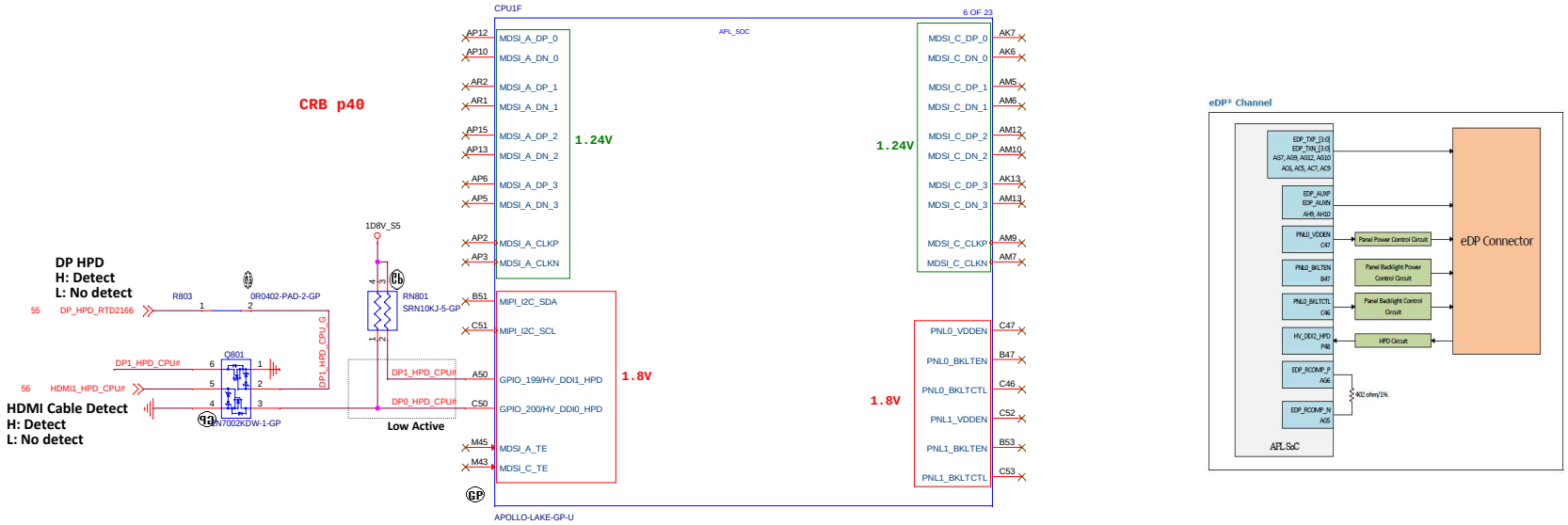
Figure 3-4. VCGI, VSS, VNN Sense Guideline



wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei		
Title: CPU (VCCGI/VDDQ/Others)			
Size: Custom	Document Number: Adma_APL		Rev: SA
Date: Monday, August 08, 2016	Sheet 7 of 105		

SSID = CPU





<Variant Name>

wistron

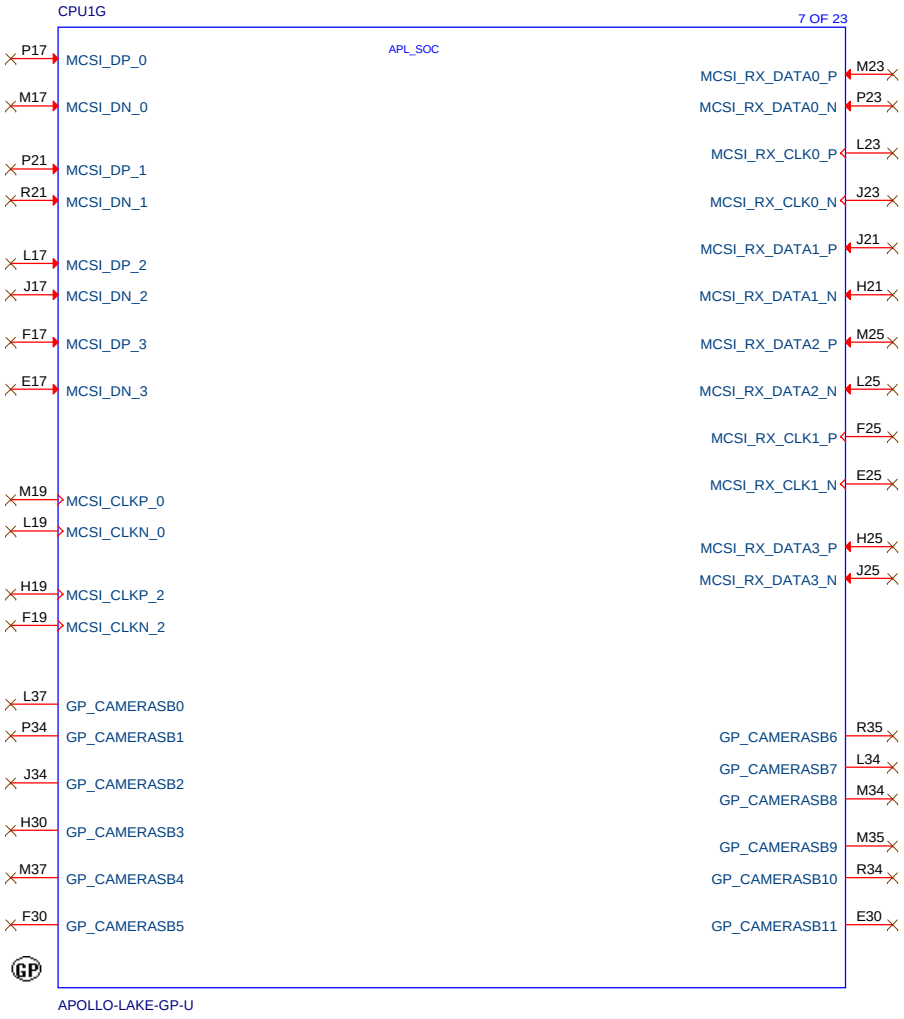
Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU (DDI/EDP/MDSI)

Size: C | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 8 of 105

SSID = CPU



wistron	Wistron Incorporated 12F, 88, Hsin Tai Wu Rd Hsichih, Taipei	
Title: CPU (MCSI/Camera)		
Size: Custom	Document Number: Adma_APL	Rev: SA
Date: Monday, August 08, 2016	Sheet 9 of 105	

SSID = CPU

VCCGI

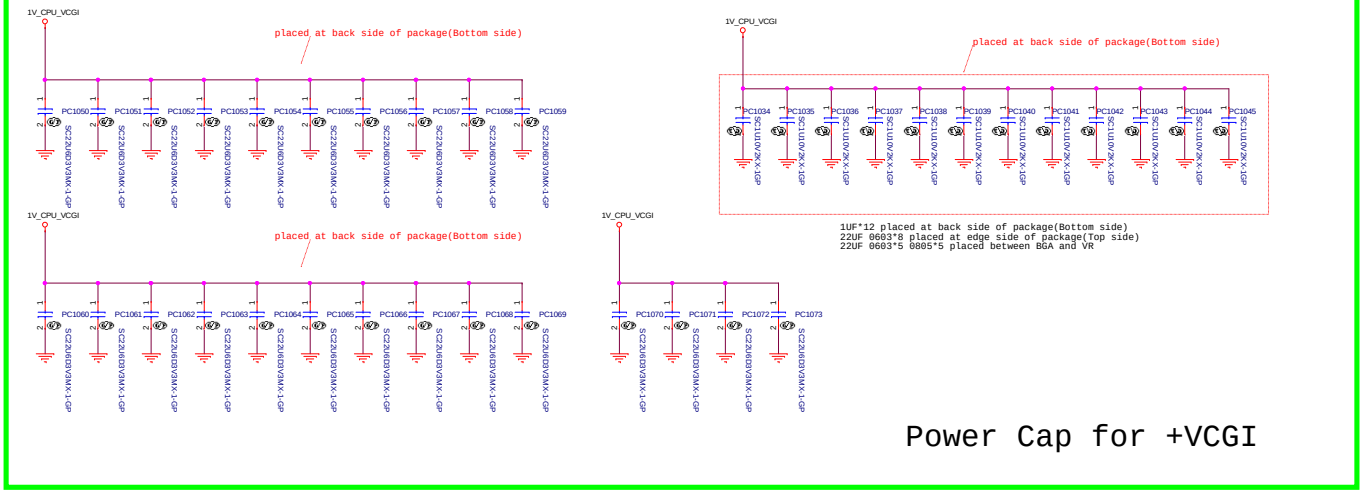
CRB p57, p58

CRB r0.9: 1U 0402 x 12, 22U 0603 x 8, 47U 0805 x 3, 47U 0805 x 9(EMPTY)
PDG r0.9: 1U 0402 x 12, 22U 0603 x 8, 47U 0805 x 3

IccMax = 21 A

1U 0402 x 12, 22U 0805 x 5, 22U 0603 x 13

follow power team



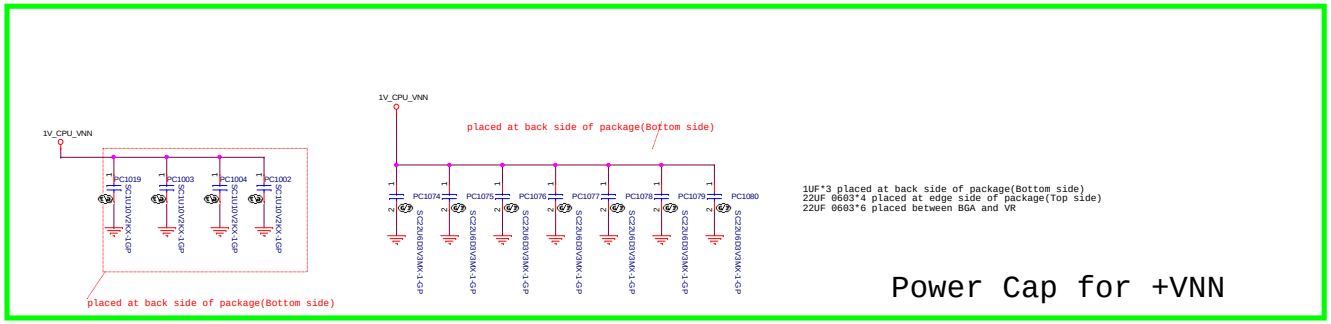
VNN

CRB p57

CRB r0.9: 1U 0402 x 3, 22U 0603 x 4, 47U 0805 x 7
PDG r0.9: 1U 0402 x 3, 22U 0603 x 4, 47U 0805 x 7

IccMax = 4.8 A

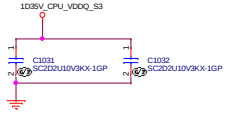
1U 0402 x3, 22U 0603 x 7, 22U 0603 x 3(EMPTY)



VDDQ follow CRB

CRB p57

22U 0603 x 8

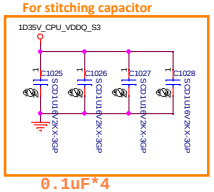


1UF*2. placed at edge side of package(Top side)
22UF*2 placed between BGA and VR

22UF capacitor move to Page.48

22UF*4 placed at edge side of package(Top side)
22UF*4 placed between BGA and VR

For stitching capacitor



0.1uF*4

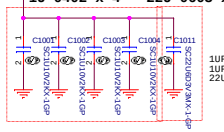
0.1UF*4 placed at back side of package(Bottom side)

VCCRAM_1P05_IO follow CRB

CRB p57

1D05V_IO_3PHASEIO

1U 0402 x 4 22U 0603 x 1



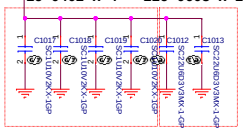
1UF*2 placed at back side of package(Bottom side)
1UF*2 placed at edge side of package(Top side)
22UF*1 placed between BGA and VR

VCCRAM_1P05 follow CRB

CRB p57

1D05V_PCH

1U 0402 x 4 22U 0603 x 2



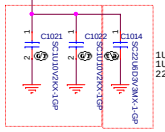
1UF*2 placed at back side of package(Bottom side)
1UF*2 placed at edge side of package(Top side)
22UF*2 placed between BGA and VR

VDD2_1P24_AUD_ISH_PLL follow CRB

CRB p57

1D24V_AUD_ISH_PLL

1U 0402 x 2 22U 0603 x 1



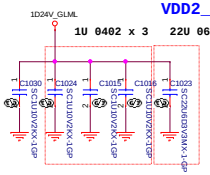
1UF*1 placed at back side of package(Bottom side)
1UF*1 placed at edge side of package(Top side)
22UF*1 placed between BGA and VR

VDD2_1P24_GLM follow CRB

CRB p57

1D24V_GLML

1U 0402 x 3 22U 0603 x 1



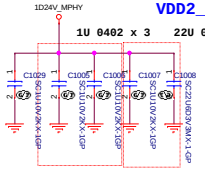
1UF*2 placed at back side of package(Bottom side)
1UF*1 placed at edge side of package(Top side)
22UF*1 placed between BGA and VR

VDD2_1P24_MPHY follow CRB

CRB p57

1D24V_MPHY

1U 0402 x 3 22U 0603 x1



1UF*2 placed at back side of package(Bottom side)
1UF*1 placed at edge side of package(Top side)
22UF*1 placed between BGA and VR

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Hsichih, Taipei

Title: CPU (Power CAP1)

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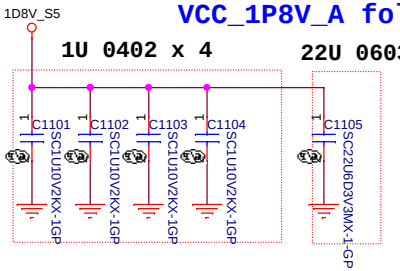
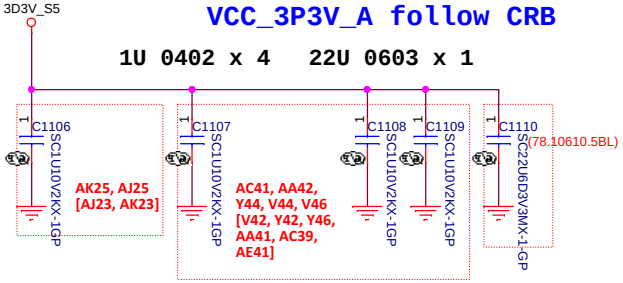
SSID = CPU CRB p58

VCC_1P8V_A follow CRB



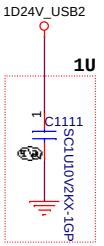
1UF*2 placed at back side of package(Bottom side)
1UF*2 placed at edge side of package(Top side)
22UF*1 placed between BGA and VR

VCC_3P3V_A follow CRB



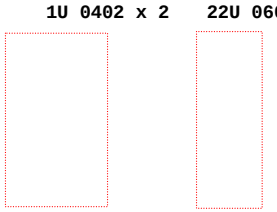
1UF*2 placed at back side of package(Bottom side)
1UF*2 placed at edge side of package(Top side)
22UF*1 placed between BGA and VR

VDD2_1P24_USB2 follow CRB



1UF*1 placed at back side of package(Bottom side)

VDD2_1P24_DSI_CSI follow CRB

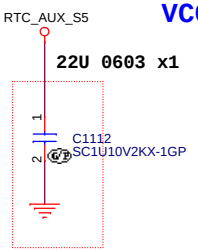


PAG r0.92: When MIPI-CSI and MIPI-DSI are not used, keep VCC_1P24V_A pins floating.

1UF*1 placed at back side of package(Bottom side)
1UF*1 placed at edge side of package(Top side)
22UF*1 placed between BGA and VR

VCCRTC_3P3V follow CRB

+VRTC



22UF*1 placed between BGA and VR

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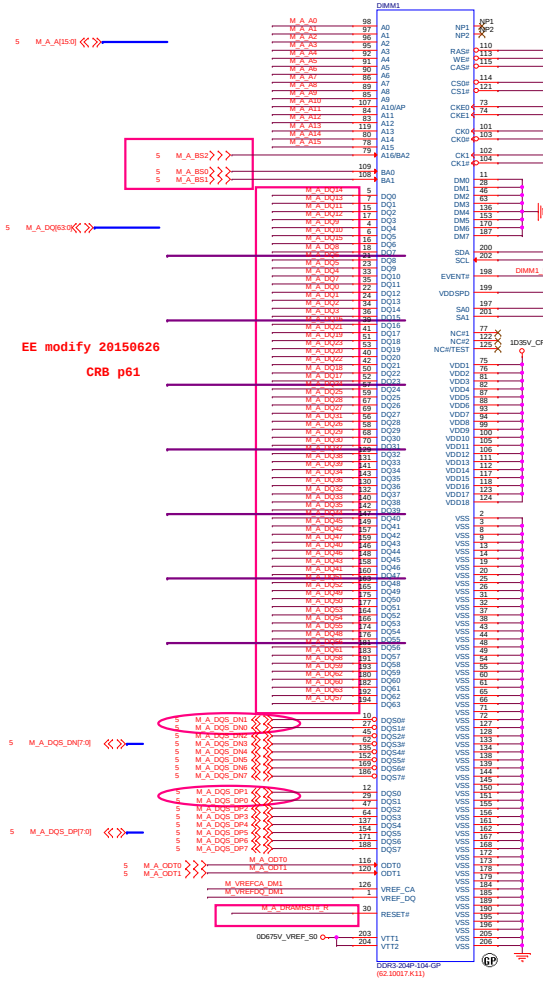
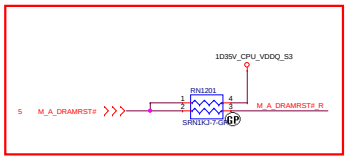
Title: CPU (Power CAP2)		
Size: B	Document Number: Adma_APL	Rev: SA
Date: Monday, August 08, 2016	Sheet 11 of 105	

SSID = DIMM1

DIMM1

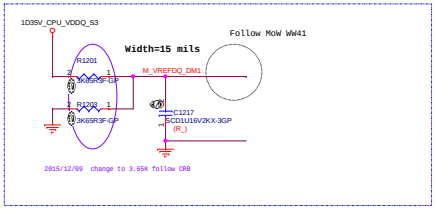


2nd source: 62.10024.M31

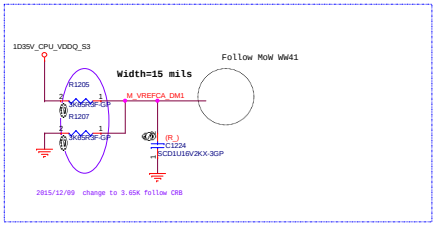


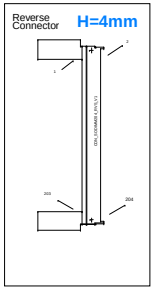
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

For Intel Recommend Close to DIMM1



For Intel Recommend Close to DIMM1

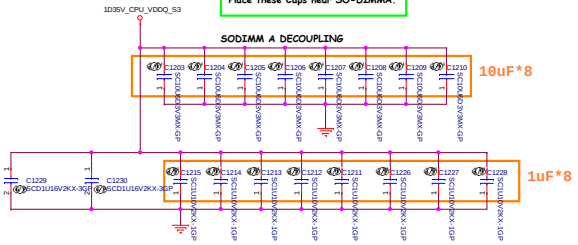


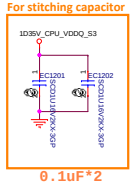


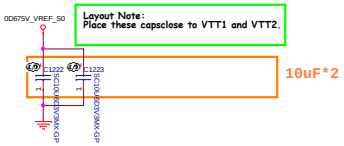
CRB r0.9 p61
VTT: 1U 0402 x 4, 10U 0603 x 2
VDD: 0.1U 0402 x 8, 10U 0603 x 8, 330U x 1

PDG r0.9
VTT: 10U 0603 x 2
VDD: 0.1U 0402 x 2, 10U 0603 x 8, 1U 0402 x 8

Layout Note:
Place these Caps near SO-DIMMA.







<Variant Name>
wistron
Wistron Incorporated
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Hsichih, Taipei Hsien

Title: DDR3_SODIMM1
Size: Custom | Document Number: Adma_APL | Rev: SA
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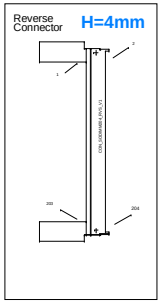
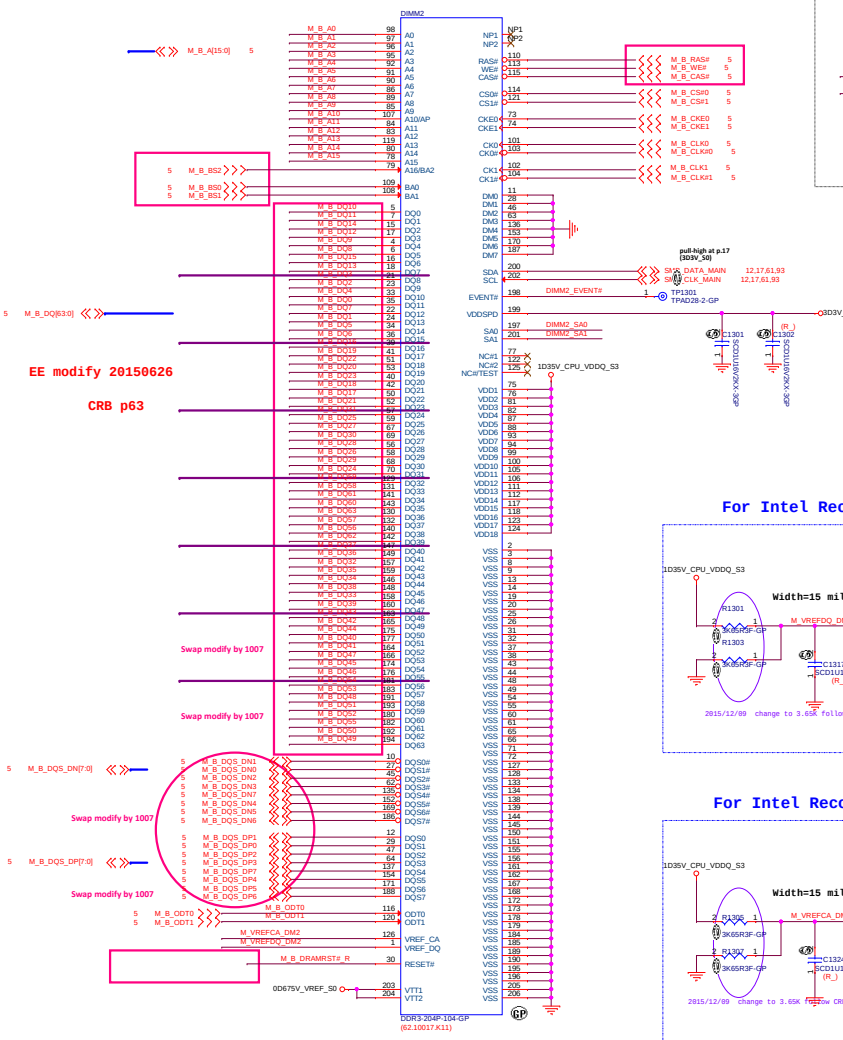
SSID = DIMM2

DIMM2

Reverse Connector **H=4mm**





EE modify 20150626

CRB p63

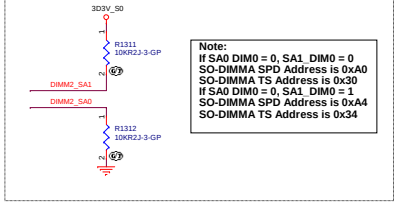
Swap modify by 1007

Swap modify by 1007

Swap modify by 1007

Swap modify by 1007

2nd source: 62.10024.M31

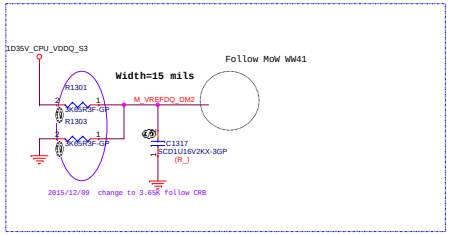


Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

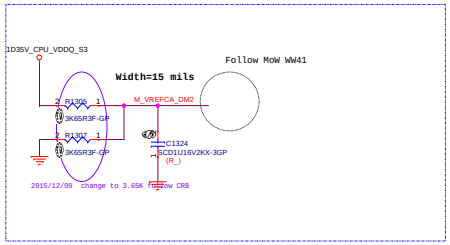
CRB r0.9 p63
VTT: 1U 0402 x 4, 10U 0603 x 2
VDD: 0.1U 0402 x 8, 10U 0603 x 8, 330U x 1

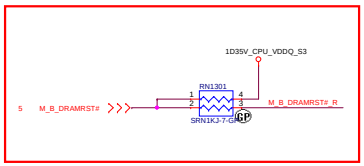
PDG r0.9
VTT: 10U 0603 x 2
VDD: 0.1U 0402 x 2, 10U 0603 x 8, 1U 0402 x 8

For Intel Recommend Close to DIMM2

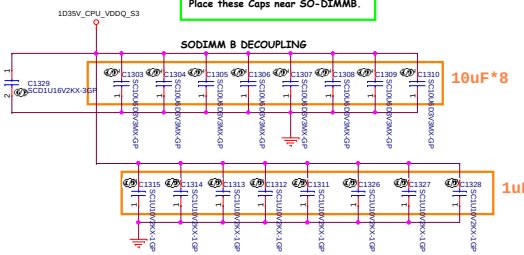


For Intel Recommend Close to DIMM2

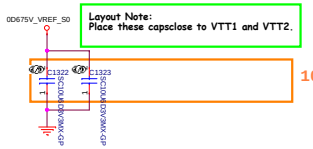




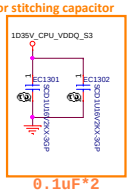
Layout Note:
Place these Caps near SO-DIMMB.



Layout Note:
Place these capsclose to VTT1 and VTT2.



For stitching capacitor



<Variant Name>

wistron Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: DDR3_SODIMM2

Size: Custom | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 13 of 105

Blanking

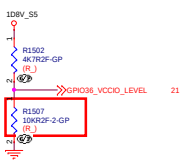
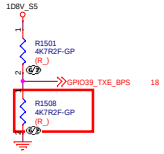
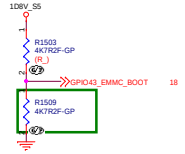
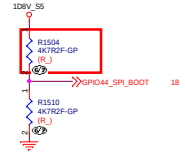
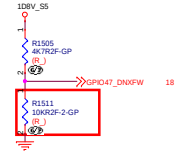
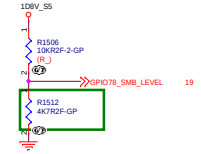
<Variant Name>

wistron	**Wistron Incorporated** 21F, 88, Sec.1, Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: **(Reserved)**		
Size: A	Document Number: **Adma_APL**	Rev: SA
Date: Monday, August 08, 2016	Sheet 14 of 105	

SSID = STRAP

STRAP RESISTORS SHOULD BE PLACED CLOSE TO SOC
SHOULD BE PLACED OUTSIDE KOZ AREA

EDS r0.7:
All the straps are sampled at Rising Edge of RSM_RST_N **CRB p61**

GPIO	GPIO_36	GPIO_39	GPIO_43	GPIO_44	GPIO_47	GPIO_78
Schematic						
High	VCC_1P24V_1P35V_A=1.35V	Enable CSE ROM Bypass enable	Allow eMMC as a boot source enable Weak internal pull-up	**Allow SPI as a boot source enable** Weak internal pull-up	Force DNX FW Load	SMBus 1.8V mode select Weak internal pull-up
Low	**VCC_1P24V_1P35V_A=1.24V (for A-step)** Weak internal pull-down	**Enable CSE ROM Bypass disable** Weak internal pull-down	**Allow eMMC as a boot source disable**	Allow SPI as a boot source disable	**Do not force DNX FW Load** Weak internal pull-down	**SMBus 3.3V mode select**

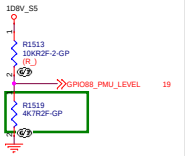
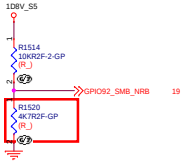
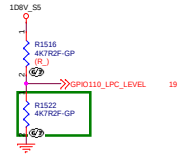
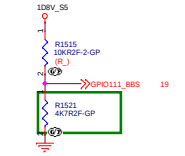
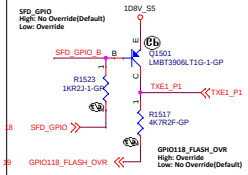
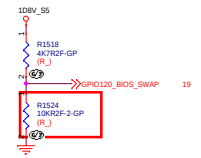
GPIO	GPIO_88	GPIO_92	GPIO_110	GPIO_111	GPIO_118	GPIO_120
Schematic						
High	PMU 1.8V mode select Weak internal pull-up	SMBus No Re-Boot enable	buffers set to 1.8V mode Weak internal pull-up	Do not boot from SPI Weak internal pull-up	Flash Descriptor Override	Top swap override enable
Low	**PMU 3.3V mode select**	**SMBus No Re-Boot disable** Weak internal pull-down	**buffers set to 3.3V mode**	**Boot from SPI**	**No Override(Normal Operation)** Weak internal pull-down	**Top swap override disable** Weak internal pull-down

Table 2-36. Hardware Straps

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_34	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_35	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_36	VCC_1P24V_1P35V_A voltage selection	20K PD	1 = 1.35V 0 = 1.24V (default) ***Note:*** This strap will only be used for B-step. For A-step this rails should only be set at 1.24V
GPIO_39	Enable CSE ROM Bypass	20K PD	1 = enable bypass 0 = disable bypass (default) ***Note:*** Apollo Lake supports TXE3.0 (this is also called CSE) ***Note:*** This strap tells CSE (TXE3.0) to bypass Read-Only Memory (ROM) that it has on SoC. If an issue occurs with the boot up code of CSE (TXE3.0) before the first patch point this strap enabled the platform tell CSE (TXE3.0) to bypass the ROM causing the issue and go to the patch space instead.
GPIO_40	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_43	Allow eMMC as a boot source	20K PU	1=enable (default) 0=disable
GPIO_44	Allow SPI as a boot source	20K PU	1=enable (default) 0=disable
GPIO_47	Force DNX FW Load	20K PD	1 = Force 0 = Do not force (default) ***Note:*** DnX: Download and Execute ***Note:*** This strap is a recovery strap for corrupted FW image. This strap will force CSE (TXE3.0) to execute a "Download and Execute" (DnX) flow, where it would fetch firmware from a USB stick and re-flash a USB. CSE (TXE3.0) can do it for BIOS part of FW, but if CSE FW itself is corrupted we need this strap.
GPIO_48	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_78	SMBus 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_82	RSVD	20K PD	Please ensure that this strap is always pulled low for normal platform operation.
GPIO_88	PMU (Power Management Unit) 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_92	SMBus No Re-Boot	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Platforms should strap this LOW. Functionality is handled by the PMC.

GPIO #	Purpose	Internal Termination	Pin Strap Usage/Description/Polarity
GPIO_104	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_105	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_106	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_111	Boot BIOS Strap (BBS)	20K PU	1 = Do not boot from SPI (default) 0 = Boot from SPI
GPIO_118	Flash Descriptor Override	20K PD	0 = No Override (Normal Operation) 1 = Override ***Note:*** This strap enables the platform to override security features in the SPI.
GPIO_110	LPC 1.8V/3.3V mode select	20K PU	1=buffers set to 1.8V mode (default) 0=buffers set to 3.3V mode
GPIO_117	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_123	RSVD	20K PU	Please ensure that this strap is pulled HIGH when RSM_RST_N de-asserts for normal platform operation.
GPIO_112	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_113	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.
GPIO_120	Top swap override	20K PD	1 = Enable 0 = Disable (default) ***Note:*** Within the SPI ROM there may be different locations where the boot code is stored. This strap enables platform to change where the core will look for BIOS code for a SPI boot only.
GPIO_121	RSVD	20K PD	Please ensure that this strap is pulled LOW when RSM_RST_N de-asserts for normal platform operation.

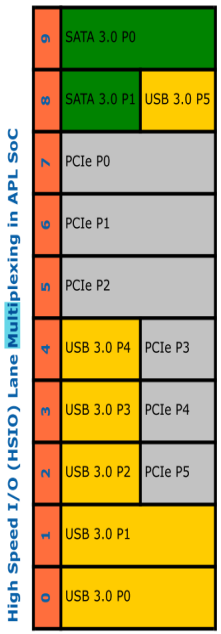
Note: All the straps are sampled at Rising Edge of RSM_RST_N

<Variant Name>

wistron Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU_(STRAP)
Size: Custom | Document Number: Adma_APL | Rev: SA
Date: Monday, August 08, 2016 | Sheet 15 of 105

SSID = CPU



The 10 HSIO lanes on APL SoC supports the following port configurations:

1. Up to 6 PCIe* lanes (multiplexed with USB 3.0 ports)

CRB p43

USB3.0 FRONT HEADER

NGFF

CPU1I

9 OF 23

APL_SOC

1.24V

1.24V

1.24V

1.8V

LAN

PCIE X16

NGFF

LAN

PCIE X16

CRB p44

Impedance / Space = 85R / 20 mils

APOLLO-LAKE-GP-U

Rear USB

USB3.0 port1

USB3.0 port0

CPU1J

10 OF 23

APL_SOC

CRB 66,68

ODD

HDD

1.8V

NGFF

LAN

PCIE X16

NGFF

LAN

PCIE X16

APOLLO-LAKE-GP-U

WLAN and LAN side are OD pin, so no need LS

<Variant Name>

wistron	Wistron Incorporated 21F, 88, Sec.1, Hsin Tai Wu Rd Hsichih, Taipei Hsien	
Title: CPU (USB3/PCIE/SATA/CLKOUT)		
Size: C	Document Number: Adma_APL	Rev: SA
Date: Monday, August 08, 2016	Sheet 16 of 105	

SSID = CPU

SVID0_DATA: CPU and VR side both PU 170R, and damping 20R close VR
SVID0_CLK: Only VR side PU 85R, and damping 95R close VR
SVID0_ALERT#: Only CPU side PU 68R,and damping 220R close CPU

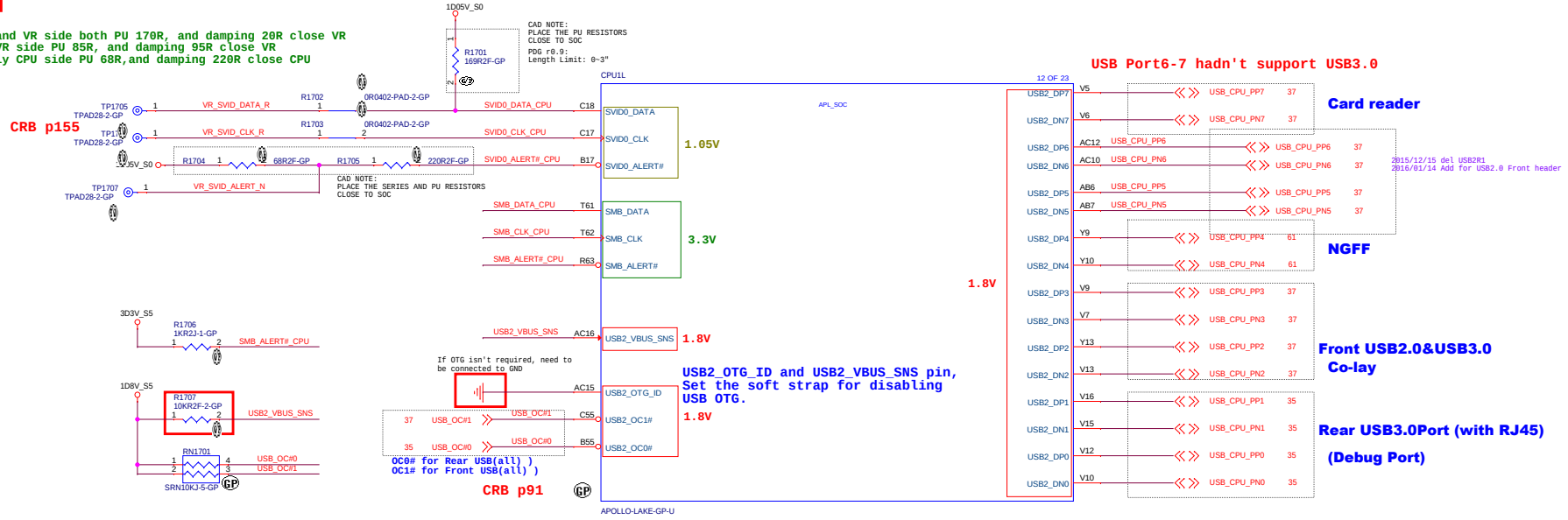
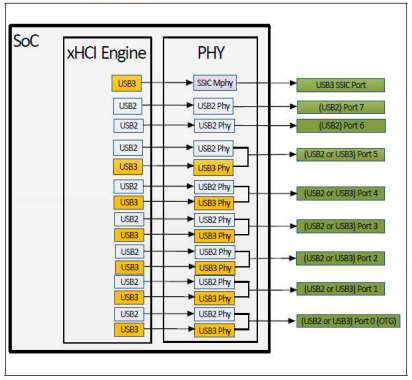


Figure 3-3. USB2 and USB3 Port Mapping



Notes: There are 8x USB Ports supported on Apollo Lake. USB Ports [5:0] can be used as USB2 and USB3 and are mutually exclusive. USB Port 6 and Port 7 can only be used as USB2.

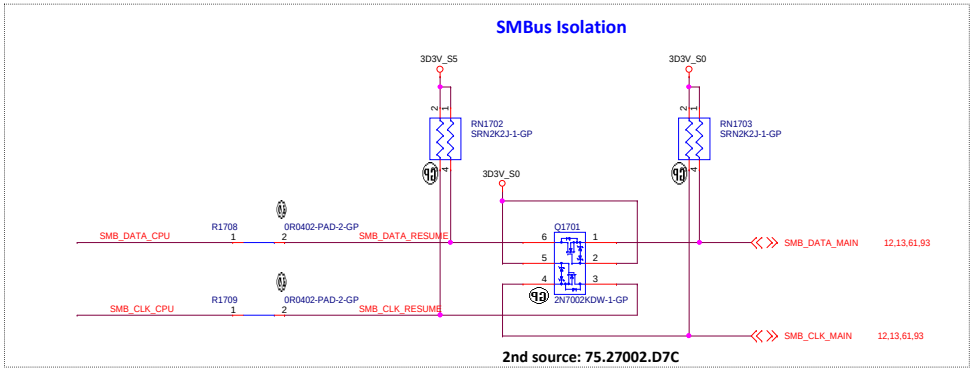


Table 61. Over current Pin Default Usage

Pin	Default Port Mapping
OC0#	Port 0
OC1#	Port 1-7

Table 62. Over current Pin Example Configuration

Location	Number of USB Ports	USB Ports Number	OC Pins Used
External Topology	1	0	OC0#
External Topology	4	1,2,3,4	OC1#

NOTE: All USB ports routed out of the package must have over current protection. It is the system BIOS responsibility to ensure all used ports have OC protection.

<Variant Name>

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Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU (USB2/SMB/SVID)

Size: C | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 17 of 105

SSID = PCH

Note:
- LPSS_UART0 and LPSS_UART3 are not POR for UART functionality.

These signals can be used as GPIOs.
- LPSS_UART1 should be dedicated for discrete GNSS
- LPSS_UART2 should be dedicated for Host OS Debug

CRB p48

EDS p34

EDS p34

EDS p35 to TPM

EDS p43

CRB p77

CRB p51

MIPI-60

CRB p50

PDG PH

RTC_RST# Circuit

RSMRST# CIRCUIT

XTAL 32.768KHz

CL=12.5P 20PPM

ESR=50K for PDG request

Table 2-30. Apollo Lake PM Interface Signals (Sheet 1 of 2)

Note: These signals are part of the GPIO. Please refer to Table 2-37 for more details.

Signal Name	Dir.	I/O Voltage	Type	Description
PMU_BATLOW_N	I/O	V1P8/V3P3	GPIO	**Battery Low:** This signal indicates that there is insufficient power to boot the system. Assertion will prevent wake from S3-S5 state. This signal can also be enabled to cause an SMI# when asserted.
PMU_PLTRST_N	I/O	V1P8/V3P3	GPIO	**Platform Reset:** This signal is used to reset devices on the platform (such as SIO, LAN, processor, and so forth.). This signal is asserted during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O port CF9h). The SoC drives PLTRST# active a minimum of 1 ms when initiated through the Reset Control register (I/O port CF9h)
PMU_PWRBTN_N	I/O	V1P8/V3P3	GPIO	**Power Button:** Power button input signal. Used to wake the SoC from power button press. The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S3- S4 states. This signal has an internal 16 ms de-bounce on the input.
PMU_RSTBTN_N	I/O	V1P8/V3P3	GPIO	**Reset Button:** Reset button input signal.
PMU_SLP_S0_N	I/O	V1P8/V3P3	GPIO	**S0 Sleep Control:** Controls power delivery subsystem. Asserted low in S0ix and G3 state.
PMU_SLP_S3_N	I/O	V1P8/V3P3	GPIO	**S3 Sleep Control:** Controls power delivery subsystem. Asserted low in S3 and lower
PMU_SLP_S4_N	I/O	V1P8/V3P3	GPIO	**S4 Sleep Control:** Controls power delivery subsystem. Asserted low in S4 and lower

Table 2-30. Apollo Lake PM Interface Signals (Sheet 2 of 2)

Note: These signals are part of the GPIO. Please refer to Table 2-37 for more details.

Signal Name	Dir.	I/O Voltage	Type	Description
PMU_SUSCLK	I/O	V1P8/V3P3	GPIO	**Suspend Clock:** Primary RTC clock output.
SUS_STAT_N		V1P8/V3P3	GPIO	**Suspend Status:** Asserted to indicate that the system will be entering a Sx state.
SUSPWRDNACK		V1P8/V3P3	GPIO	**Sus Power Down Ack:** Indicator from SoC that "always on" rails can be shut down.
SOC_PWROK	I	V1P8/V3P3	RTC	**SoC Power OK:** When asserted, this signal is an indication to the SoC that all of its core power rails have been stable for at least 5 ms. This signal can be driven asynchronously. Then this signal is negated, the SOC asserts PLTRST#.

Note: The I/O voltage selection is done by using Hardware Strap GPIO_88

Wistron Incorporated
21F, 8B, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

CPU (PMU/UART/JTAG/RTC/MSC)

Size: Custom | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 18 of 105

SSID = CPU

CPU1K

APL_SOC

11 OF 23

APOLLO-LAKE-GP-U

1.8V

3.3V /1.8V

1.8V

CRB p45

LPC

CRB p45

EDS p44

PDG p257

SPI

CPU1M

APL_SOC

13 OF 23

APOLLO-LAKE-GP-U

1.8V

1.8V

For XDP

14.4MHz for SCH5553

XTAL 19.2MHz

CL=7PF 10PPM

Table 150. I2C Mapping on CRB

Port	Usage
I2C0	Audio codec, MCSI camera
I2C1	NFC
I2C2	MCSI camera
I2C3	Touch panel
I2C4	Touch pad
I2C5	Sensors
I2C6	Sensors
I2C7	PSS, PCON, WWAN

Board ID Settings

MB Version	SKU_ID_S	BOARD1_DISP
SA(X00)	0	0
SB(X01)	0	1
-1A(X02)	1	0
-1(A00)	1	1

Board ID

Board ID (ECIO)

<Variant Name>

wistron

Wistron Incorporated
21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: CPU_(I2S/LPC/SPI/I2C/OSC)

Size: Custom | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 19 of 105

SSID = CPU

CRB p52

all S0 power rail ok (PCH_PWROK)
" delay 1D05V_S0 between 5~100ms")
(input pin)

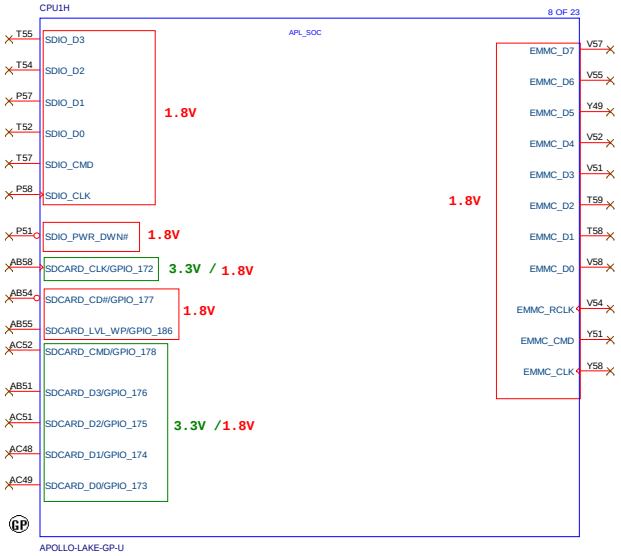
CRB: DELAY_ALL_SYS_PWRGD

SOC_PWROK_CPU 39

From SIO

R2010 100KR2J-1-GP

CRB p52
EDS p35



wistron
Wistron Incorporated
12F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: CPU (Storage/RCOMP)

Size: C | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 20 of 105

SSID = CPU

EDS p42

V1.8A

EDS p41

HDA

CPU1O

APL_SOC

15 OF 23

1.8V

HDA_SPKR — AK57 ISH_GPIO_9/SPKR

AM52 ISH_GPIO_8/MEMHOT#

AM55 ISH_GPIO_7/AVS_I2S5_SDO/LPSS_UART2_CTS#

AM57 ISH_GPIO_6/AVS_I2S5_SDI/LPSS_UART2_RTS#

AM49 ISH_GPIO_5/AVS_I2S5_WS_SYNC/LPSS_UART2_TXD

AM51 ISH_GPIO_4/AVS_I2S5_BCLK/LPSS_UART2_RXD

HDA_SDOUT_CODEC — R2101 33R2J-2-GP — HDA_SDOUT_CPU — AM54 ISH_GPIO_3/AVS_I2S6_SDO/AVS_HDA_SDO

HDA_SDIN0_CPU — AK51 ISH_GPIO_2/AVS_I2S6_SDI/AVS_HDA_SDI

HDA_SYNC_CODEC — R2103 33R2J-2-GP — HDA_SYNC_CPU — AK58 ISH_GPIO_1/AVS_I2S6_WS_SYNC/AVS_HDA_WS_SYNC

HDA_BITCLK_CODEC — R2105 33R2J-2-GP — HDA_BITCLK_CPU — AM48 ISH_GPIO_0/AVS_I2S6_BCLK/AVS_HDA_BCLK

HDA_SYNC_CODEC — R2106 249R2F-GP — HDA_SDIN0_CPU

R2108 1KR2J-1-GP

Sighting No.560733: un-stuff for QS sample

PMIC_IRQ_CPU — F34 GPIO_33/ISH_GPIO_15/SUS_CLK3

F35 GPIO_32/ISH_GPIO_14/SUS_CLK2

H34 GPIO_31/ISH_GPIO_13/SUS_CLK1

C37 GPIO_30/ISH_GPIO_12

H35 GPIO_29/ISH_GPIO_11

B37 GPIO_28/ISH_GPIO_10

C29 GPIO_27

64 CPU_SATA_LED_N — CPU_SATA_LED_N — OD — C31 GPIO_26/SATA_LED#

C27 GPIO_25/SATA_DEVSLP1

1.8V

GPIO_18 J39

GPIO_24/SATA_DEVSLP0 C25

GPIO_23/SATA_GP1 B25

GPIO_22/SATA_GP0 A26

GPIO_21 C26

GPIO_20 B27

GPIO_19 C33

GPIO_9 A30

GPIO_17 C35

GPIO_16 C36

GPIO_15 F39

GPIO_14 C38

GPIO_13 C30

GPIO_12 E39 SOC_WAKE_SCI#

GPIO_11 C34 SOC_RUNTIME_SCI# — SOC_RUNTIME_SCI# 24

GPIO_10 L39

GPIO_0 A36 DBG_PTI_CLK0_R — TP2103 TPAD28-2-GP

GPIO_8 B29 DBG_PTI_DATA_7_R — TP2104 TPAD28-2-GP

GPIO_7 H36 DBG_PTI_DATA_6_R — TP2105 TPAD28-2-GP

GPIO_6 B31 DBG_PTI_DATA5 — TP2106 TPAD28-2-GP

GPIO_5 A34 DBG_PTI_DATA4 — TP2107 TPAD28-2-GP

GPIO_4 B35 DBG_PTI_DATA3 — TP2108 TPAD28-2-GP

GPIO_3 B30 DBG_PTI_DATA2 — TP2109 TPAD28-2-GP

GPIO_2 C36 DBG_PTI_DATA1 — TP2110 TPAD28-2-GP

GPIO_1 B33 DBG_PTI_DATA0 — TP2111 TPAD28-2-GP

MIPI-60

EDS p29

1D8V_S5

SOC_WAKE_SCI# — R2102 10KR2F-2-GP

SOC_RUNTIME_SCI# — R2104 10KR2F-2-GP

1D8V_S5

R2110 10KR2J-3-GP

PME_R

SOC_WAKE_SCI# — Q2103 LMBT3904LT1G-GP — LPC_PME_N 24

2016/4/6 change PMIC_IRQ connect (follow 15265-Rocket)

1D8V_S5

R1834 1KR2J-1-GP

2016/6/21 Delete

PMIC_IRQ_CPU — PMIC_IRQ 46

CPU1Q

APL_SOC

17 OF 23

1.8V

M16 NCTF_59

L16 NCTF_60

F16 NCTF_63

E16 NCTF_54

J16 NCTF_66

H16 NCTF_58

H12 NCTF_68

F12 NCTF_56

M12 NCTF_65

M10 NCTF_62

F14 NCTF_57

H14 NCTF_55

GPIO_219 L30

GPIO_218 M30

GPIO_217 M29

GPIO_216 P30

NCTF_67 AP57

PWM3 E41 PW_CLEAR — GPI — TP2112 TPAD28-2-GP

PWM2 F41 GPIO36_VCCIO_LEVEL — STRAP, 20K PD — GPIO36_VCCIO_LEVEL 15

PWM1 C41 GPIO35_CPU — STRAP, 20K PD — TP2101 TPAD28-2-GP

PWM0 B41 GPIO34_CPU — STRAP, 20K PD — TP2102 TPAD28-2-GP

NCTF_64 C63

NCTF_61 E63

APOLLO-LAKE-GP-U

APOLLO-LAKE-GP-U

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Hsichih, Taipei

Title: CPU (HDA/ISH/GPIO/PWM)

Size: C | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 21 of 105

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<Variant Name>

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Hsichih, Taipei Hsien

Title
(Reserved)

Size	Document Number	Rev
A	Adma_APL	SA

Date: Monday, August 08, 2016 Sheet 22 of 105

SSID = CPU

CPU1S

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APL_SOC

AM36	VSS_394		VSS_1	A12	
AG42	VSS_190		VSS_4	A16	
AG44	VSS_193		VSS_7	A20	
AG46	VSS_196		VSS_10	A24	
AH15	VSS_199		VSS_13	A28	
AH16	VSS_202		VSS_16	A32	
AH48	VSS_205		VSS_19	A36	
AH5	VSS_208		VSS_22	A40	
AH52	VSS_211		VSS_25	A44	
AH54	VSS_214		VSS_28	A48	
AH55	VSS_217		VSS_31	A52	
AH57	VSS_220		VSS_380	A56	
AH58	VSS_223		VSS_34	A62	
AH59	VSS_226		VSS_382	A9	
AH6	VSS_229		VSS_37	AA1	
AH7	VSS_232		VSS_40	AA2	
AJ1	VSS_235		VSS_43	AA27	
AJ18	VSS_388		VSS_384	AA34	
AJ2	VSS_238		VSS_46	AA41	
AJ23	VSS_241		VSS_49	AA63	
AJ27	VSS_244		VSS_52	AB10	
AJ34	VSS_247		VSS_55	AB12	
AJ36	VSS_250		VSS_58	AB16	
AJ63	VSS_253		VSS_61	AB48	
AK10	VSS_256		VSS_64	AB5	
AK12	VSS_259		VSS_67	AB52	
AK18	VSS_262		VSS_70	AB57	
AK23	VSS_265		VSS_73	AB59	
AK27	VSS_268		VSS_76	AB9	
AK48	VSS_273		VSS_79	AC27	
AK5	VSS_276		VSS_82	AC34	
AK52	VSS_279		VSS_85	AC39	
AK59	VSS_282		VSS_88	AE1	
AK9	VSS_285		VSS_91	AE10	
AM18	VSS_288		VSS_386	AE11	
AM22	VSS_291		VSS_94	AE13	
AM27	VSS_294		VSS_97	AE14	
AM34	VSS_297		VSS_100	AE16	
AM39	VSS_300		VSS_103	AE17	
AM46	VSS_303		VSS_106	AE2	
AN1	VSS_306		VSS_109	AE23	
AN10	VSS_309		VSS_112	AE27	
AN11	VSS_312		VSS_115	AE34	
AN13	VSS_315		VSS_118	AE39	
AN14	VSS_318		VSS_121	AE4	
AN16	VSS_321		VSS_124	AE41	
AN17	VSS_324		VSS_127	AE47	
AN2	VSS_327		VSS_130	AE48	
AN25	VSS_330		VSS_133	AE5	
AN27	VSS_333		VSS_136	AE50	
AN28	VSS_336		VSS_139	AE51	
AN30	VSS_339		VSS_142	AE53	
AN34	VSS_342		VSS_145	AE54	
AN36	VSS_345		VSS_148	AE56	
AN37	VSS_348		VSS_151	AE57	
AN39	VSS_351		VSS_154	AE59	
AN47	VSS_354		VSS_157	AE63	
AN48	VSS_357		VSS_160	AE7	
AN5	VSS_360		VSS_163	AE8	
AN50	VSS_363		VSS_166	AG13	
AN51	VSS_366		VSS_169	AG18	
AN53	VSS_369		VSS_172	AG23	
B63	VSS_392		VSS_175	AG27	
A5	VSS_393		VSS_178	AG34	
AC18	VSS_391		VSS_181	AG37	
			VSS_184	AG39	
			VSS_187	AG41	

APOLLO-LAKE-GP-U

CPU1T

20 OF 23

APL_SOC

AR19	VSS_2	VSS_191	BB19
AR32	VSS_5	VSS_194	BB25
AR45	VSS_8	VSS_197	BB3
AT12	VSS_11	VSS_200	BB39
AT16	VSS_14	VSS_203	BB45
AT19	VSS_17	VSS_206	BB61
AT2	VSS_20	VSS_209	BC32
AT25	VSS_23	VSS_212	BD3
AT29	VSS_26	VSS_215	BD32
AT3	VSS_29	VSS_218	BD56
AT35	VSS_32	VSS_221	BD61
AT39	VSS_381	VSS_224	BD8
AT45	VSS_35	VSS_227	BE1
AT48	VSS_383	VSS_230	BE10
AT52	VSS_38	VSS_233	BE12
AT57	VSS_41	VSS_236	BE16
AT61	VSS_44	VSS_389	BE17
AT62	VSS_385	VSS_239	BE21
AT7	VSS_47	VSS_242	BE27
AU32	VSS_50	VSS_245	BE29
AV19	VSS_53	VSS_248	BE35
AV2	VSS_56	VSS_251	BE37
AV21	VSS_59	VSS_254	BE43
AV23	VSS_62	VSS_257	BE47
AV29	VSS_65	VSS_260	BE48
AV3	VSS_68	VSS_263	BE52
AV32	VSS_71	VSS_266	BE54
AV35	VSS_74	VSS_269	BE63
AV41	VSS_77	VSS_271	BF3
AV43	VSS_80	VSS_274	BF32
AV45	VSS_83	VSS_277	BF61
AV55	VSS_86	VSS_280	BG19
AV61	VSS_89	VSS_283	BG23
AV62	VSS_92	VSS_286	BG29
AV9	VSS_387	VSS_289	BG32
AW14	VSS_95	VSS_292	BG35
AW30	VSS_98	VSS_295	BG41
AW34	VSS_101	VSS_298	BG45
AW50	VSS_104	VSS_301	BH1
AY10	VSS_107	VSS_304	BH2
AY32	VSS_110	VSS_307	BH21
AY54	VSS_113	VSS_310	BH25
AY58	VSS_116	VSS_313	BH39
AY6	VSS_119	VSS_316	BH43
B2	VSS_122	VSS_319	BH62
B3	VSS_125	VSS_322	BH63
B62	VSS_128	VSS_325	BJ10
B9	VSS_131	VSS_328	BJ14
BA1	VSS_134	VSS_331	BJ18
BA12	VSS_137	VSS_334	BJ28
BA16	VSS_140	VSS_337	BJ32
BA17	VSS_143	VSS_340	BJ36
BA2	VSS_146	VSS_343	BJ4
BA21	VSS_149	VSS_346	BJ46
BA25	VSS_152	VSS_349	BJ50
BA27	VSS_155	VSS_352	BJ54
BA29	VSS_158	VSS_355	BJ56
BA32	VSS_161	VSS_358	BJ60
BA35	VSS_164	VSS_361	BJ8
BA37	VSS_167	VSS_364	C12
BA39	VSS_170	VSS_367	C16
BA43	VSS_173		
BA47	VSS_176		
BA48	VSS_179		
BA52	VSS_182		
BA62	VSS_185		
BA63	VSS_188		
AK36	VSS_390		

APOLLO-LAKE-GP-U

CPU1U

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APL_SOC

D6	VSS_21	VSS_222	P45
E12	VSS_24	VSS_225	P5
E14	VSS_27	VSS_228	P55
E19	VSS_30	VSS_231	P59
E27	VSS_33	VSS_234	P9
E4	VSS_36	VSS_237	R23
E54	VSS_39	VSS_240	R32
F10	VSS_42	VSS_243	T49
F21	VSS_45	VSS_246	U1
F3	VSS_48	VSS_249	U10
F32	VSS_51	VSS_252	U11
F37	VSS_54	VSS_255	U13
F43	VSS_57	VSS_258	U14
F45	VSS_60	VSS_261	U16
F50	VSS_63	VSS_264	U17
F56	VSS_66	VSS_267	U18
F59	VSS_69	VSS_270	U2
F63	VSS_72	VSS_272	U27
G1	VSS_75	VSS_275	U34
G32	VSS_78	VSS_278	U5
H17	VSS_81	VSS_281	U50
H23	VSS_84	VSS_284	U51
H29	VSS_87	VSS_287	U53
H3	VSS_90	VSS_290	U54
H37	VSS_93	VSS_293	U56
H47	VSS_96	VSS_296	U57
H61	VSS_99	VSS_299	U59
H7	VSS_102	VSS_302	U62
J12	VSS_105	VSS_305	U63
J14	VSS_108	VSS_308	U7
J19	VSS_111	VSS_311	U8
J27	VSS_114	VSS_314	V20
J30	VSS_117	VSS_317	V27
J32	VSS_120	VSS_320	V34
J35	VSS_123	VSS_323	V42
J37	VSS_126	VSS_326	Y12
J48	VSS_129	VSS_329	Y16
J63	VSS_132	VSS_332	Y22
K32	VSS_135	VSS_335	Y27
K5	VSS_138	VSS_338	Y34
K54	VSS_141	VSS_371	AP9
K57	VSS_144	VSS_372	AP55
K6	VSS_147	VSS_373	AN63
L21	VSS_150	VSS_374	AN7
L27	VSS_153	VSS_375	AN8
L29	VSS_156	VSS_376	AN54
L35	VSS_159	VSS_377	AN56
L43	VSS_162	VSS_378	AN57
L45	VSS_165	VSS_379	AN59
L50	VSS_168	VSS_341	Y42
M14	VSS_171	VSS_344	Y46
M21	VSS_174	VSS_347	Y48
M27	VSS_177	VSS_350	Y5
M3	VSS_180	VSS_353	Y52
M32	VSS_183	VSS_356	Y54
M50	VSS_186	VSS_359	Y55
M59	VSS_189	VSS_362	Y57
M9	VSS_192	VSS_365	Y59
N1	VSS_195	VSS_368	Y6
N32	VSS_198	VSS_370	Y7
N63	VSS_201	VSS_3	C28
P13	VSS_204	VSS_6	C32
P19	VSS_207	VSS_9	C40
P35	VSS_210	VSS_12	C48
P37	VSS_213	VSS_15	D32
		VSS_18	D58
		VSS_216	P41
		VSS_219	P43
R29	VSS_395		

APOLLO-LAKE-GP-U

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Hsichih, Taipei

Title: CPU (VSS)

Size: B | Document Number: Adma_APL | Rev: SA

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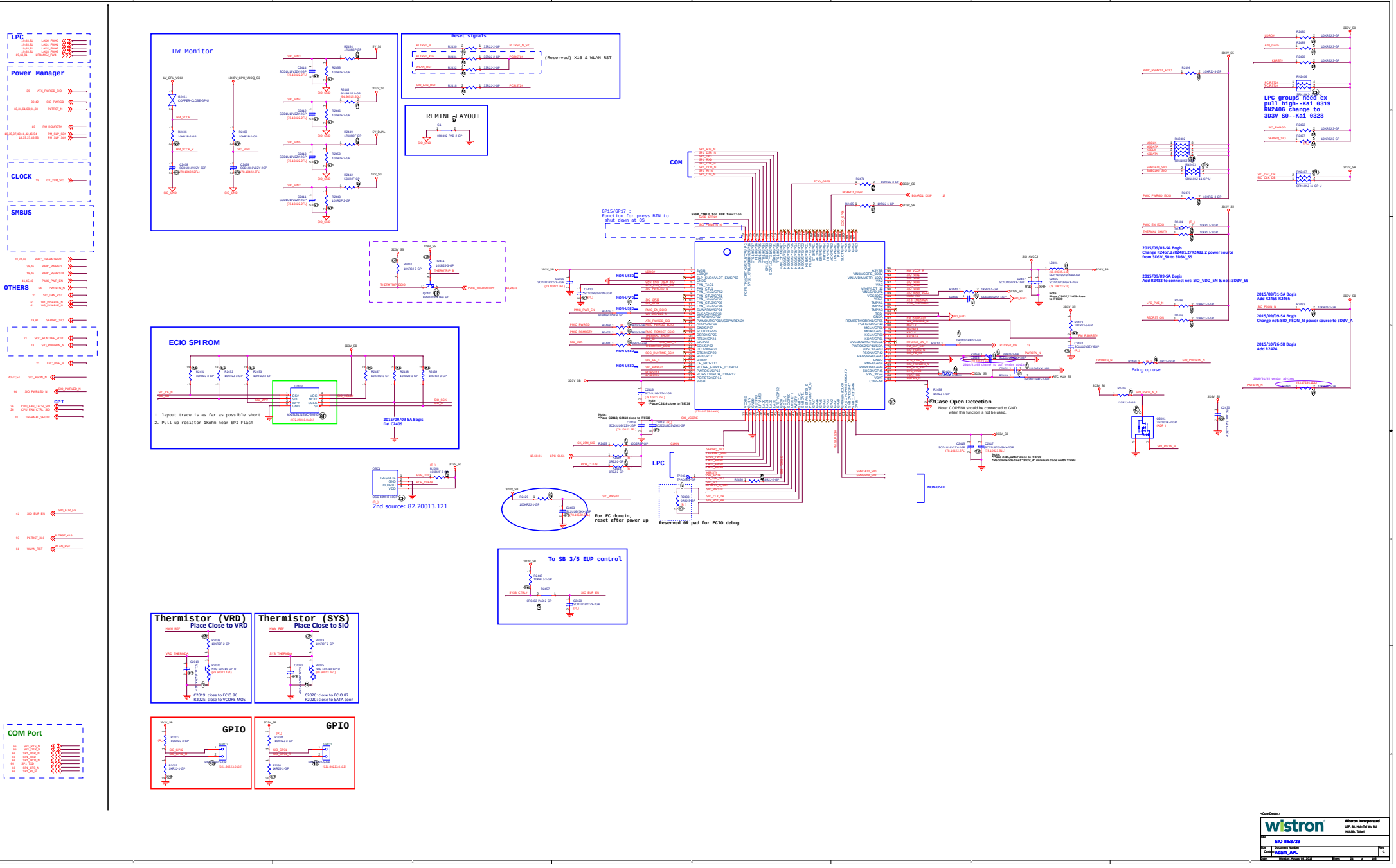
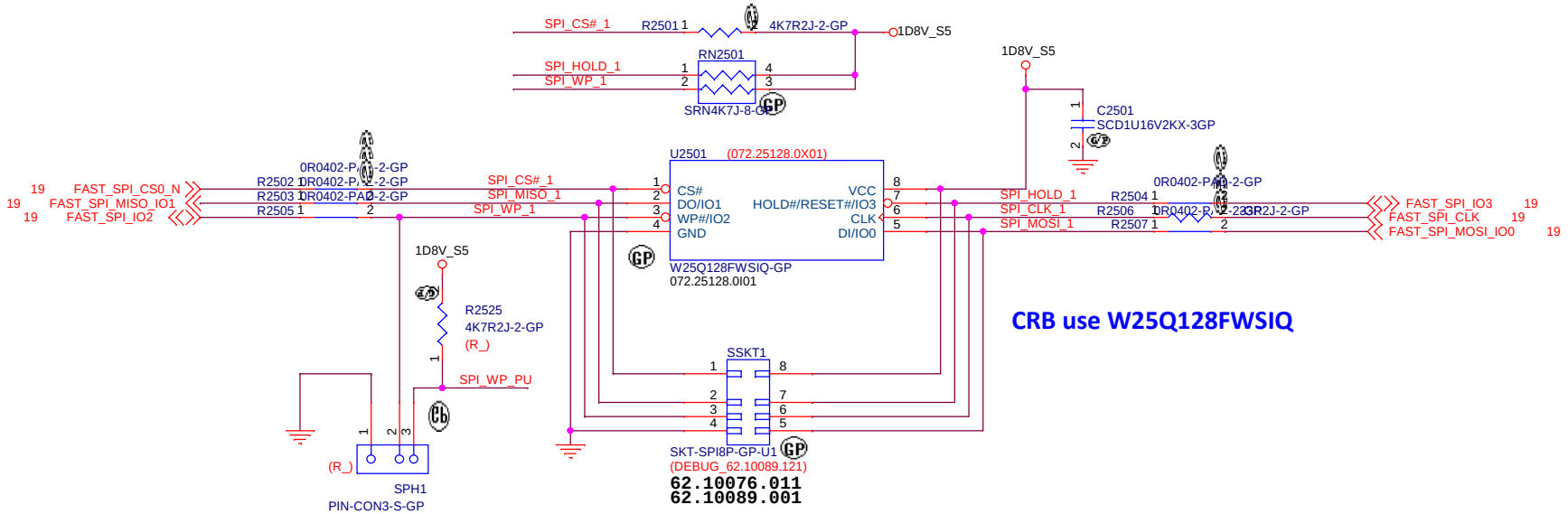

LPC
Power Manager
CLOCK
SMBUS
OTHERS
GPI
COM Port
HW Monitor
Reset Signals
(Reserved) X16 & WLAN RST
REMINE LAYOUT
ECIO SPI ROM
1. layout trace is as far as possible short
2. Pull-up resistor 1Kohm near SPI Flash
2015/09/09-5A Bogis
Del C2409
2nd source: 82.20013.121
COM
LPC
GP15/GP17 :
Function for press BTN to
shut down at OS
Case Open Detection
Note: COPEN# should be connected to GND
when this function is not be used.
For EC domain,
reset after power up
Reserved 0R pad for ECIO debug
NON-USED
To SB 3/5 EUP control
Thermistor (VRD)
Place Close to VRD
C2019: close to ECIO.86
R2025: close to VCORE MOS
Thermistor (SYS)
Place Close to SIO
C2020: close to ECIO.87
R2020: close to SATA conn
GPIO
GPIO
LPC groups need ex
pull high--Kai 0319
RN2406 change to
3D3V_S0--Kai 0328
2015/09/03-5A Bogis
Change R2467.2/R3481.2/R2482.2 power source
from 3D3V_S0 to 3D3V_S5
2015/09/09-5A Bogis
Add R2483 to connect net: SIO_VDD_EN & net: 3D3V_S5
2015/08/31-5A Bogis
Add R2465 R2466
2015/09/09-5A Bogis
Change net: SIO_PSON_N power source to 3D3V_S
2015/10/26-5B Bogis
Add R2474
Bring up use
SIO ITE8739
Adson_APL
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

SSID = Flash.ROM

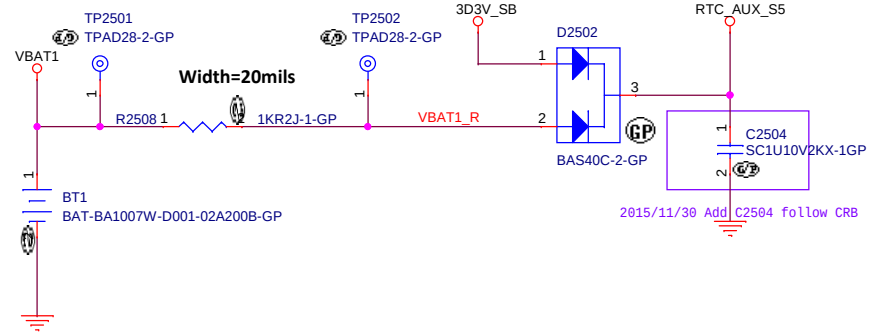
SPI ROM 16M Byte



CRB use W25Q128FWSIQ

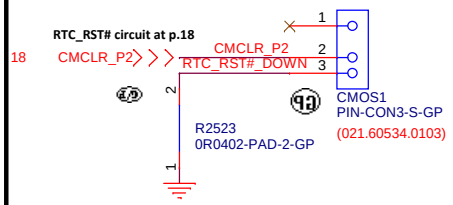
SPI ROM socket Co-Layout with U2501

SSID = RTC

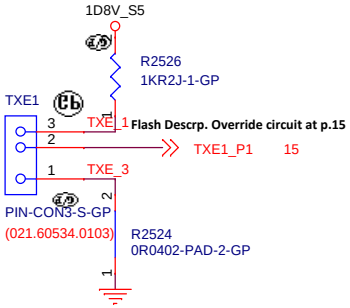


1-2: NORMAL

2-3: CMOS CLEAR



SFD_GPIO_B
1-2:Low: No Override(Default)
2-3:High: Override



<Variant Name>

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Hsichih, Taipei Hsien

Title: Flash ROM/RTC

Size	Document Number	Rev
Custom	Adma_APL	SA

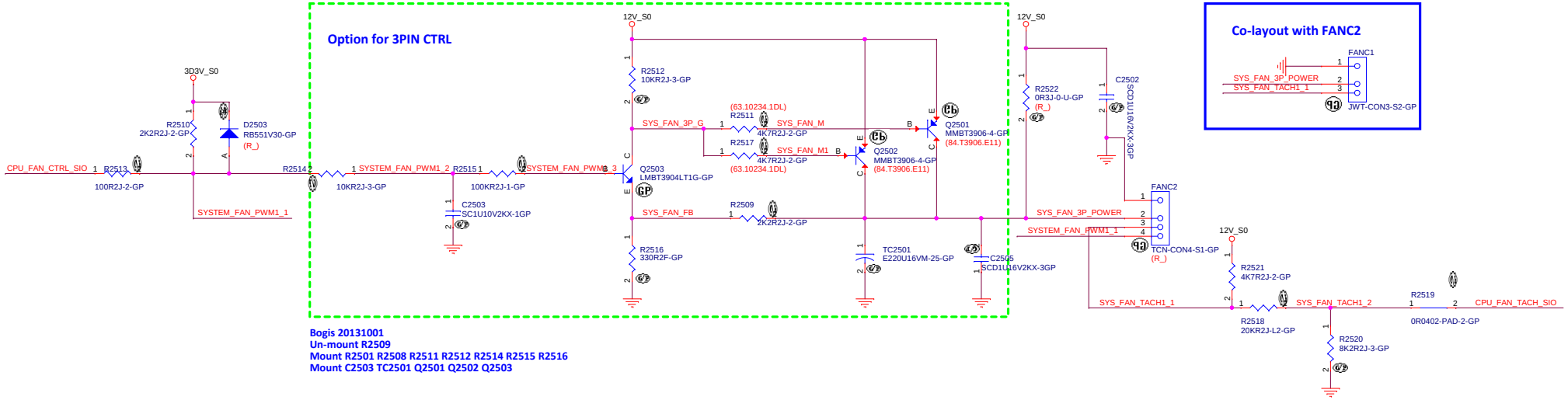
Date: Monday, August 08, 2016 Sheet 25 of 105

Fan Controller

24 CPU_FAN_TACH_SIO
24 CPU_FAN_CTRL_SIO

CPU FAN

SYS 3 PINS/4 PINS FAN CONTROL



Co-layout with FANC2

Bogis 20131001
Un-mount R2509
Mount R2501 R2508 R2511 R2512 R2514 R2515 R2516
Mount C2503 TC2501 Q2501 Q2502 Q2503

<Variant Name>

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Hsichih, Taipei Hsien

Title: FAN CIRCUITS/HOLE

Size: Custom | Document Number: Adma_APL | Rev: SA

Date: Monday, August 08, 2016 | Sheet 26 of 105

HD_LINK

21	HDA_SDIN0_CPU
21	HDA_SDOUT_CODEC
19,29	HDA_RST#_CODEC
21	HDA_SYNC_CODEC
21	HDA_BITCLK_CODEC

AUDIO PORT

29	AUD_IN_L
29	AUD_IN_R
29	AUD_MIC1_L
29	AUD_MIC1_R
29	MIC1_VREFO_R
29	MIC1_VREFO_L
29	AUDAMPIN_L
29	AUDAMPIN_R
29	MIC2_LL
29	MIC2_RR
29	FP_OUTR_LL
29	FP_OUTR_RR

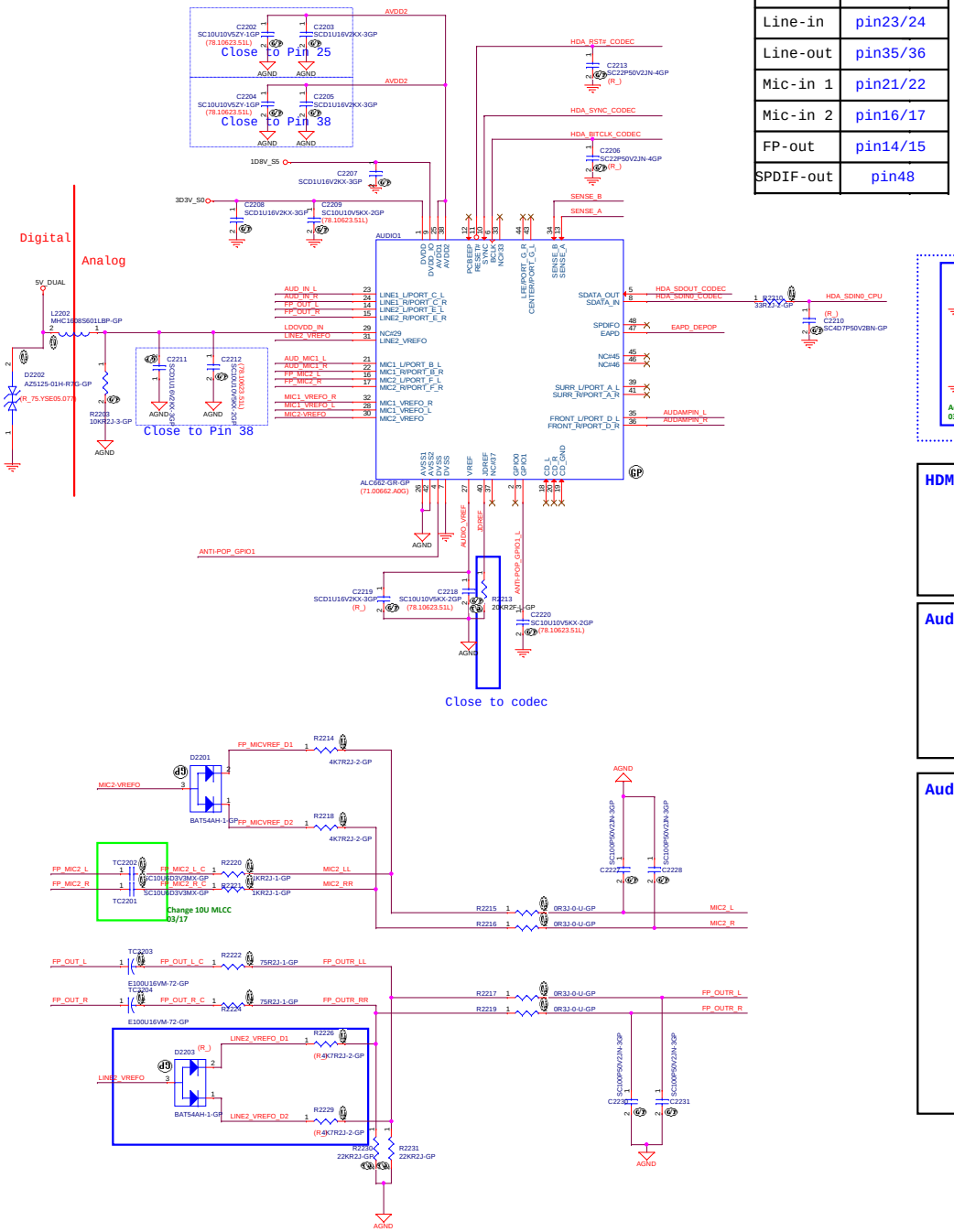
MISC

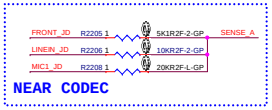
29	FRONT_JD
29	LINEIN_JD
29	MIC1_JD
29	EAPD_DEPOP

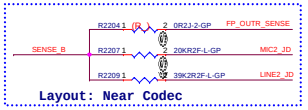
GPIO

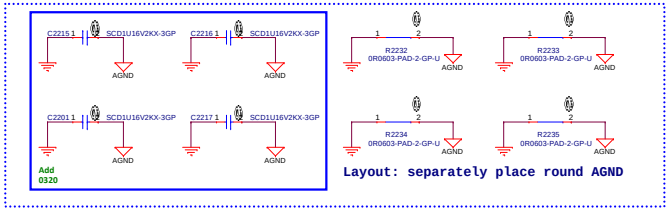
29	ANTI-POP_GPIO1

	ALC662-VC\VD
Line-in	pin23/24
Line-out	pin35/36
Mic-in 1	pin21/22
Mic-in 2	pin16/17
FP-out	pin14/15
SPDIF-out	pin48









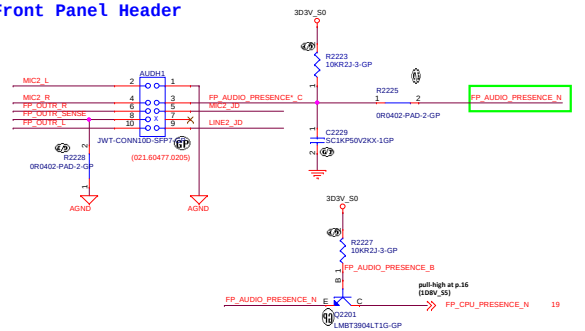
HDMI SPDIF HEADER

20140708 David
Removed

Audio Internal Speaker Header

20140708 David
Removed

Audio Front Panel Header



wistron Wistron Incorporated
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Title: AUDIO CODEC (ALC662-VD)

Size: Custom | Document Number: Adma_APL | Rev: SA

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<Variant Name>

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Hsichih, Taipei Hsien

Title
(Reserved)

Size	Document Number	Rev
A	Adma_APL	SA

Date:	Monday, August 08, 2016	Sheet	28	of	105

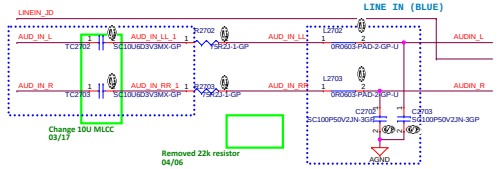
AUDIO PORT

27 FP_OUTR_LL
27 FP_OUTR_RR
27 MIC2_LL
27 MIC2_RR
27 AUD_IN_L
27 AUD_IN_R
27 MIC1_VREFO_L
27 AUD_MIC1_L
27 AUD_MIC1_R
27 MIC1_VREFO_R
27 AUDAMPIN_L
27 AUDAMPIN_R

MISC

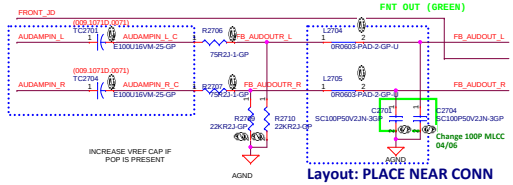
27 LINEIN_JD
27 FRONT_JD
27 MIC1_JD
19,27 HDA_RST#_CODEC
27 ANTI-POP_GPIO1
27 EAPD_DEPOP

The cap need to close codec on layout.



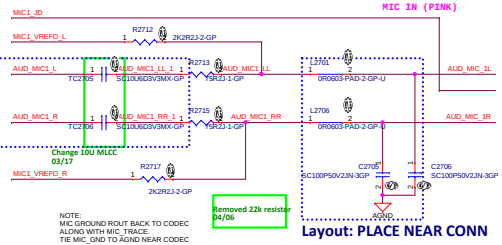
Layout: PLACE NEAR CONN

The cap need to close codec on layout.

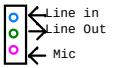


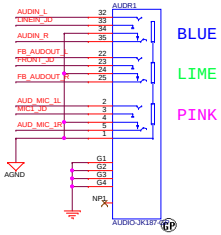
Layout: PLACE NEAR CONN

The cap need to close codec on layout.



Layout: PLACE NEAR CONN

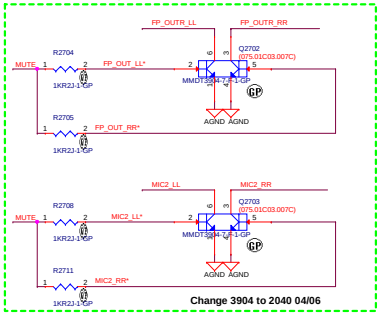




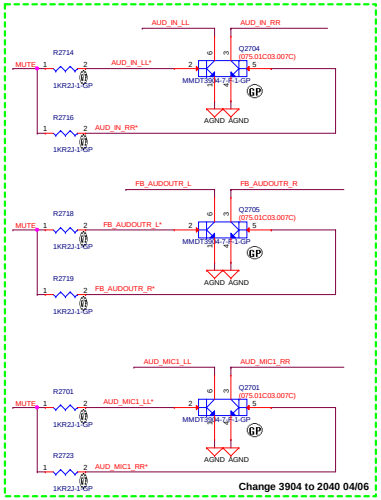
2010/10/19
USE Lingyang 22.10270.691 Audio Jack

Bogis 20130826
Connect AUDR1.G1/G2/G3/G4 from ESDGND to GND

Front Audio Port De-Pop Circuit

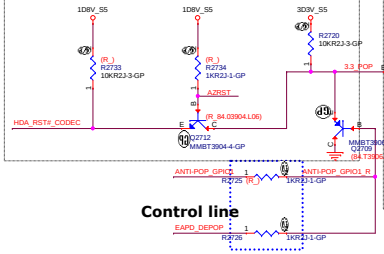


Rear Audio Port De-Pop Circuit



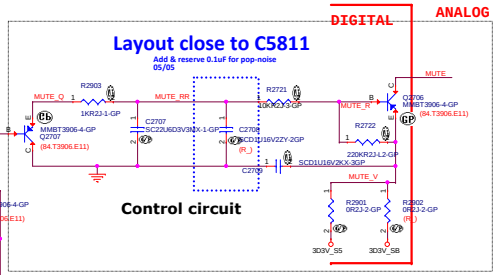
POP Circuit *Rear*

Control by software driver and CODEC GPIO.
GPIO driving low at:
1).Initial state
2).Suspend to S1
3).Resume from S1.



Control line

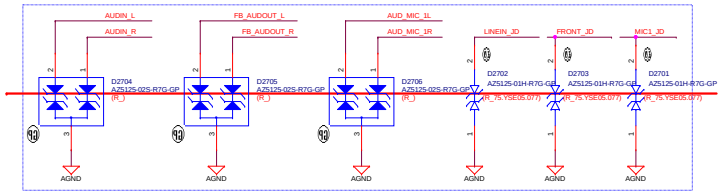
Unmount R2725, Mount R2726



Control circuit

MUTE

AZ_RST_N	EAPD_DEPOP	MUTE
0	0	0
0	1	0
1	0	0
1	1	1



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Title: AUDIO JACK
Size: Custom
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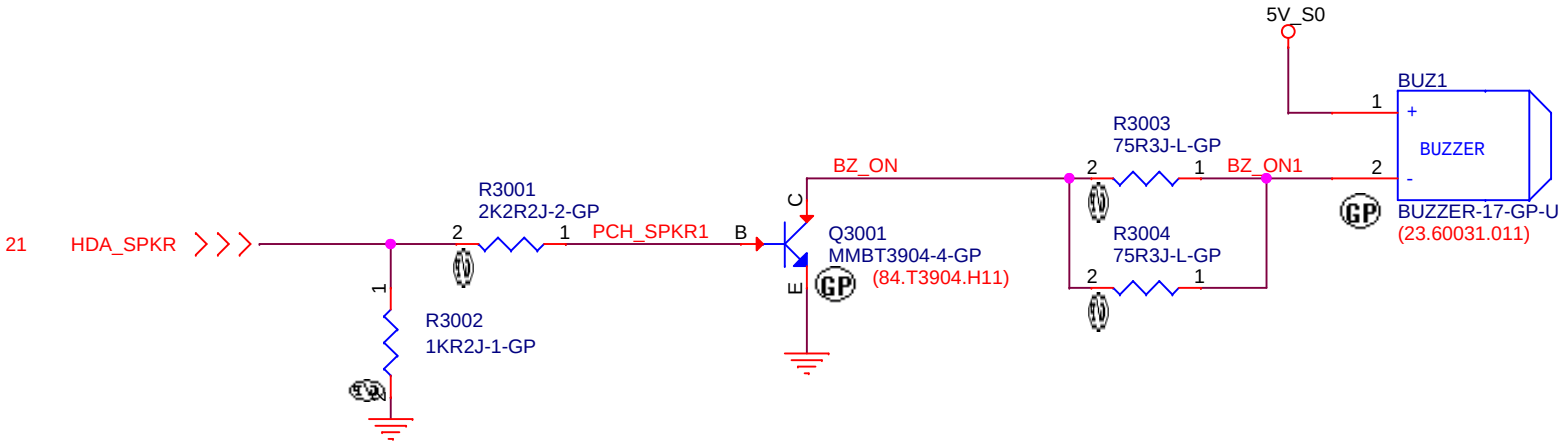
BUZZER



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Title: BUZZER		
Size: A	Document Number: Adma_APL	Rev: SA
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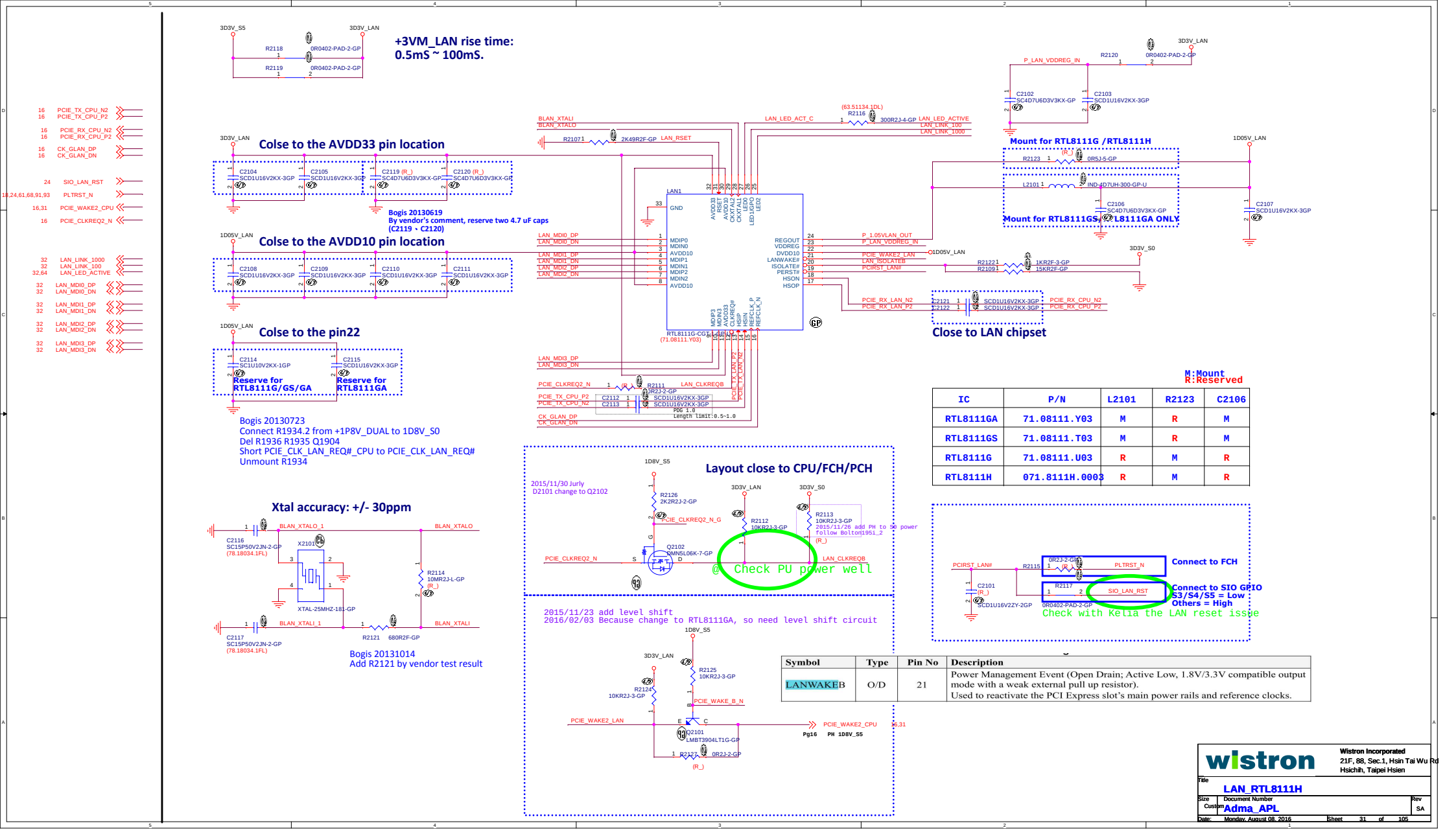

IC	P/N	L2101	R2123	C2106
RTL8111GA	71.08111.Y03	M	R	M
RTL8111GS	71.08111.T03	M	R	M
RTL8111G	71.08111.U03	R	M	R
RTL8111H	071.8111H.0003	R	M	R

Symbol	Type	Pin No	Description
LANWAKEB	O/D	21	Power Management Event (Open Drain; Active Low, 1.8V/3.3V compatible output mode with a weak external pull up resistor). Used to reactivate the PCI Express slot's main power rails and reference clocks.

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Title: LAN_RTL8111H
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LAN common choke

31 LAN_MDI0_DN → EC3201 (R_) SC1D5P50V2CN-1GP → EL3201 → LAN_MDI0_DN_C
31 LAN_MDI0_DP → EC3202 (R_) SC1D5P50V2CN-1GP → EL3201 → LAN_MDI0_DP_C
COIL-90OHM-100MHZ-5-GP (66.R0036.04L)

31 LAN_MDI2_DN → EC3205 (R_) SC1D5P50V2CN-1GP → EL3203 → LAN_MDI2_DN_C
31 LAN_MDI2_DP → EC3206 (R_) SC1D5P50V2CN-1GP → EL3203 → LAN_MDI2_DP_C
COIL-90OHM-100MHZ-5-GP (66.R0036.04L)

31 LAN_MDI1_DN → EC3203 (R_) SC1D5P50V2CN-1GP → EL3202 → LAN_MDI1_DN_C
31 LAN_MDI1_DP → EC3204 (R_) SC1D5P50V2CN-1GP → EL3202 → LAN_MDI1_DP_C
COIL-90OHM-100MHZ-5-GP (66.R0036.04L)

31 LAN_MDI3_DN → EC3207 (R_) SC1D5P50V2CN-1GP → EL3204 → LAN_MDI3_DN_C
31 LAN_MDI3_DP → EC3208 (R_) SC1D5P50V2CN-1GP → EL3204 → LAN_MDI3_DP_C
COIL-90OHM-100MHZ-5-GP (66.R0036.04L)

ED3201 AZC099-04S-2-GP
LAN_MDI3_DN_C / LAN_MDI2_DP_C → I/O1 / I/O2
GND, VDD → 3D3V_LAN
I/O4 → LAN_MDI3_DP_C
I/O3 → LAN_MDI2_DN_C

U2/LAN/DMIC TVS suggestion part
1st :075.09904.0A7C Amazing
2nd :075.02304.0C7C INPAQ
3rd :075.01256.007C Liteonsemi

ED3202 AZC099-04S-2-GP
LAN_MDI1_DN_C / LAN_MDI0_DP_C → I/O1 / I/O2
GND, VDD → 3D3V_LAN
I/O4 → LAN_MDI1_DP_C
I/O3 → LAN_MDI0_DN_C

ED3203 AZC099-04S-2-GP
LAN_LED_ACTIVE / LAN_LINK_100 → I/O1 / I/O2
GND, VDD → 3D3V_LAN
I/O4 → LAN_LINK_1000
I/O3 → (NC)

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

USB3.0+RJ45

USB30_VCCA_0 → TC3201 E220U16VM-25-GP
U3RJ1 SKT-RJ45-USB-83-GP (N_022.10001.0E61,S_022.10001.0I31)
Normal parts (N_)
022.10001.0E61 UDE
022.10001.0C51 Speedtech
With surge protection (S_)
022.10001.0I31 UDE (6k only)
022.10001.0I41 Speedtech (6k only)

35	USB30_TX_REAR_P0	
35	USB30_TX_REAR_P1	
35	USB30_TX_REAR_N0	
35	USB30_TX_REAR_N1	
35	USB30_RX_REAR_P1	
35	USB30_RX_REAR_N1	
35	USB30_RX_REAR_N0	
35	USB_RJ45_PN0	
35	USB_RJ45_PN1	
35	USB_RJ45_PP1	
35	USB_RJ45_PP0	
35	USB30_RX_REAR_P0	

LAN_CONN_GND
LAN_LED_ACT
LAN_LED_ACTIVE 31,64
LAN_MDI3_DN_C
LAN_MDI3_DP_C
LAN_MDI2_DN_C
LAN_MDI2_DP_C
LAN_MDI1_DN_C
LAN_MDI1_DP_C
LAN_MDI0_DN_C
LAN_MDI0_DP_C
LAN_LINK_100_R
LAN_LINK_1000_R
LAN_CONN_CVT

3D3V_LAN
R3201 200R2J-L1-GP (63.18134.1DL)
20150629 David
v/f Brian need add
front LAN LED
C3201 SCD1U16V2ZY-2GP
C3202 SCD1U16V2ZY-2GP
C3203 SCD1U16V2KX-3GP
C3207 SCD1U16V2ZY-2GP
R3202 330R2J-3-GP
R3203 330R2J-3-GP
R2813 330R2J-2-GP → LAN_LINK_100 31
R2814 330R2J-2-GP → LAN_LINK_1000 31

reserved for ESD
5V_DUAL, 3D3V_S5
ED3204 AZ5725-01FDR7G-GP
ED3205 AZ5725-01FDR7G-GP

UP - Port 0
DOWN - Port 1

<Variant Name>

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Title: RJ45+USB2.0
Size: Custom
Document Number: Adma_APL
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Title
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Size B | Document Number Adma_APL | Rev SA

Date: Monday, August 08, 2016 | Sheet 33 of 105

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<Variant Name>

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Title
(Reserved)

Size	Document Number	Rev
B	Adma_APL	SA

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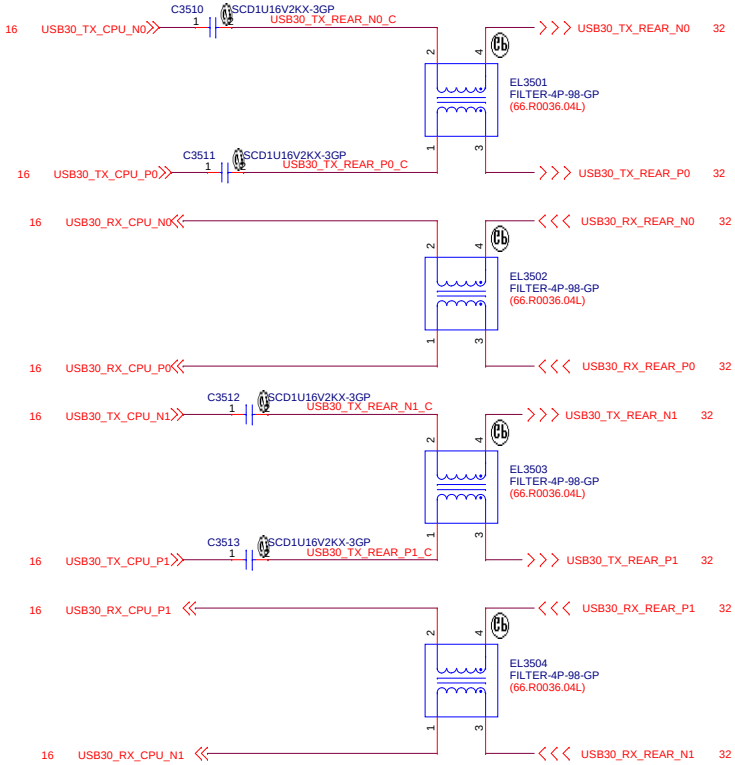
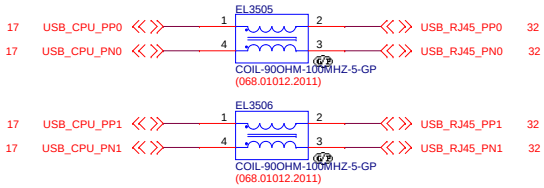
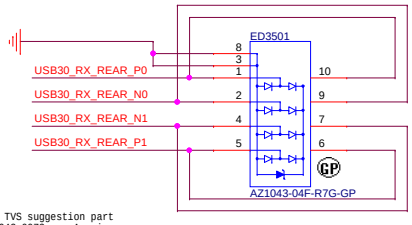
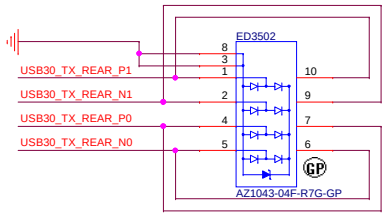
USB 3.0 Rear Port

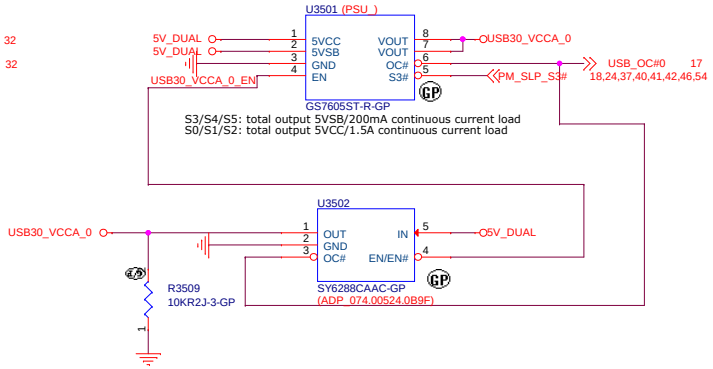


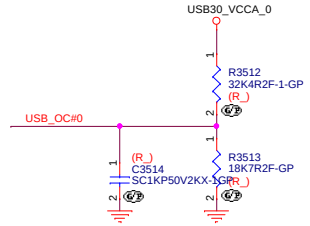


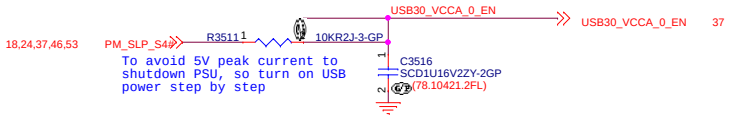


U3/HDMI/DVI TVS suggestion part
1st :075.01043.0073 Amazing
2nd :75.08808.073 AOS
3rd :075.00550.0071 Liteonsemi

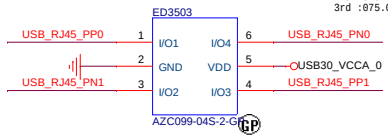








U2/LAN/DMIC TVS suggestion part
1st :075.00904.0A7C Amazing
2nd :075.02304.0C7C INPAQ
3rd :075.01256.007C Liteonsemi



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Title: USB3.0 CONN(FRONT)

Size: Custom | Document Number: Adma_APL | Rev: SA

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<Variant Name>

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Size	Document Number	Rev
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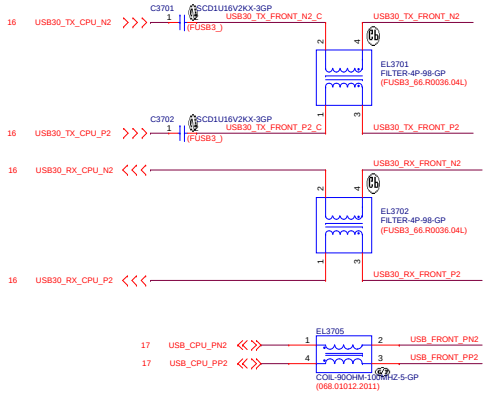
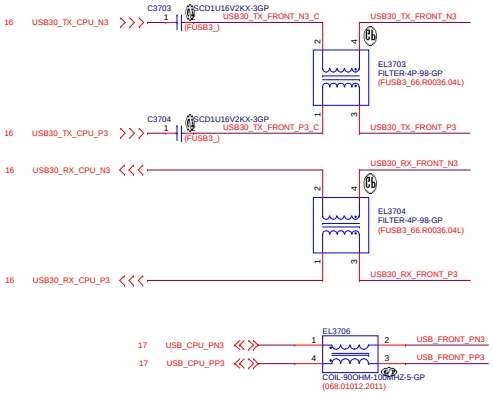
USB3F1 Front Port





U3/HDMI/DVI TVS suggestion part
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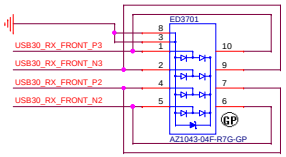
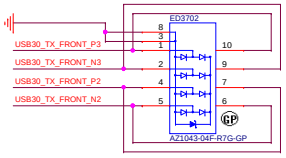
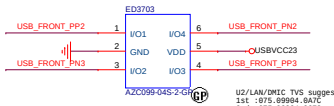
2nd :75.08808.073 ADS
3rd :075.00550.0071 Liteonsemi

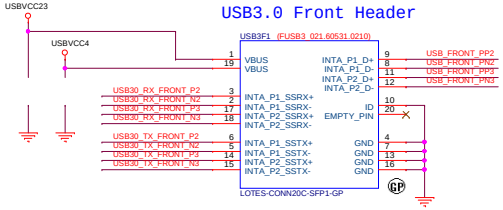




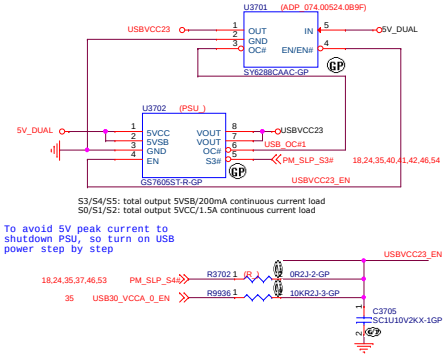


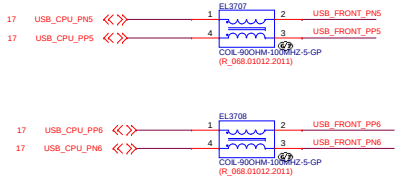
U2/LAN/DMIC TVS suggestion part
1st :075.09904.0A7C Amazing
2nd :075.02384.0C7C INPAQ
3rd :075.01256.007C Liteonsemi

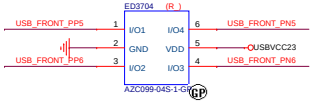
USB3.0 Front Header



USB2F2 Front Port







USB2.0 Front Header

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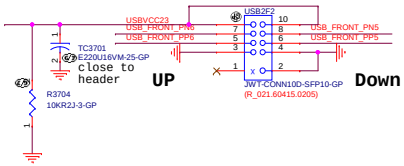
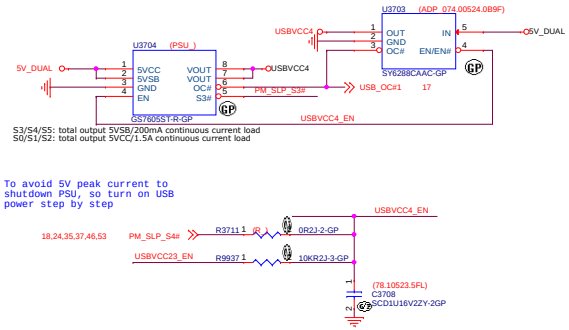
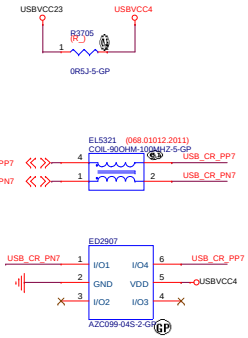


USB2F1 (Card Reader)





U2/LAN/DMIC TVS suggestion part
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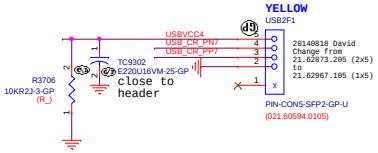
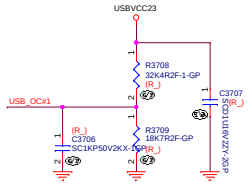
2nd :075.02384.0C7C INPAQ
3rd :075.01256.007C Liteonsemi

USB2.0 Front Header

YELLOW





<Variant Name>

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Title: (Reserved)

Size: Custom | Document Number: Adma_APL | Rev: SA

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<Variant Name>

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Hsichih, Taipei Hsien

Title
(Reserved)

Size	Document Number	Rev
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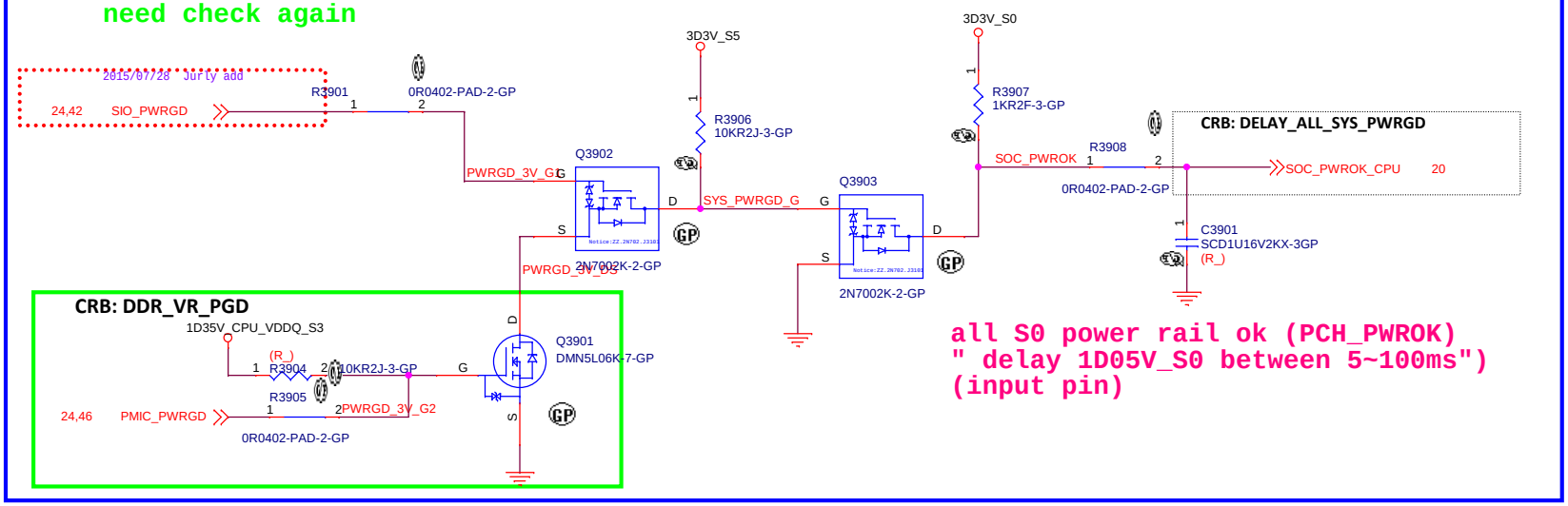
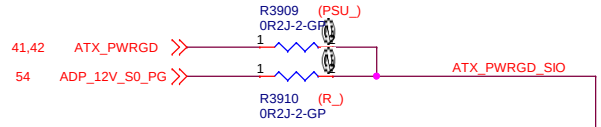
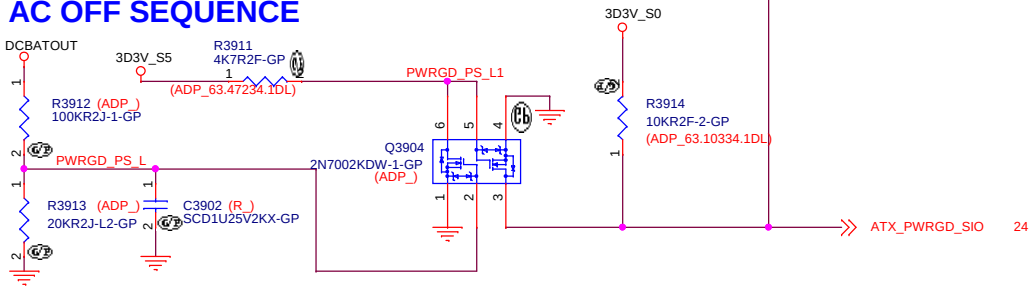
need check again





For AC OFF SEQUENCE



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Title	(Reserved)	
Size B	Document Number Adma_APL	Rev SA
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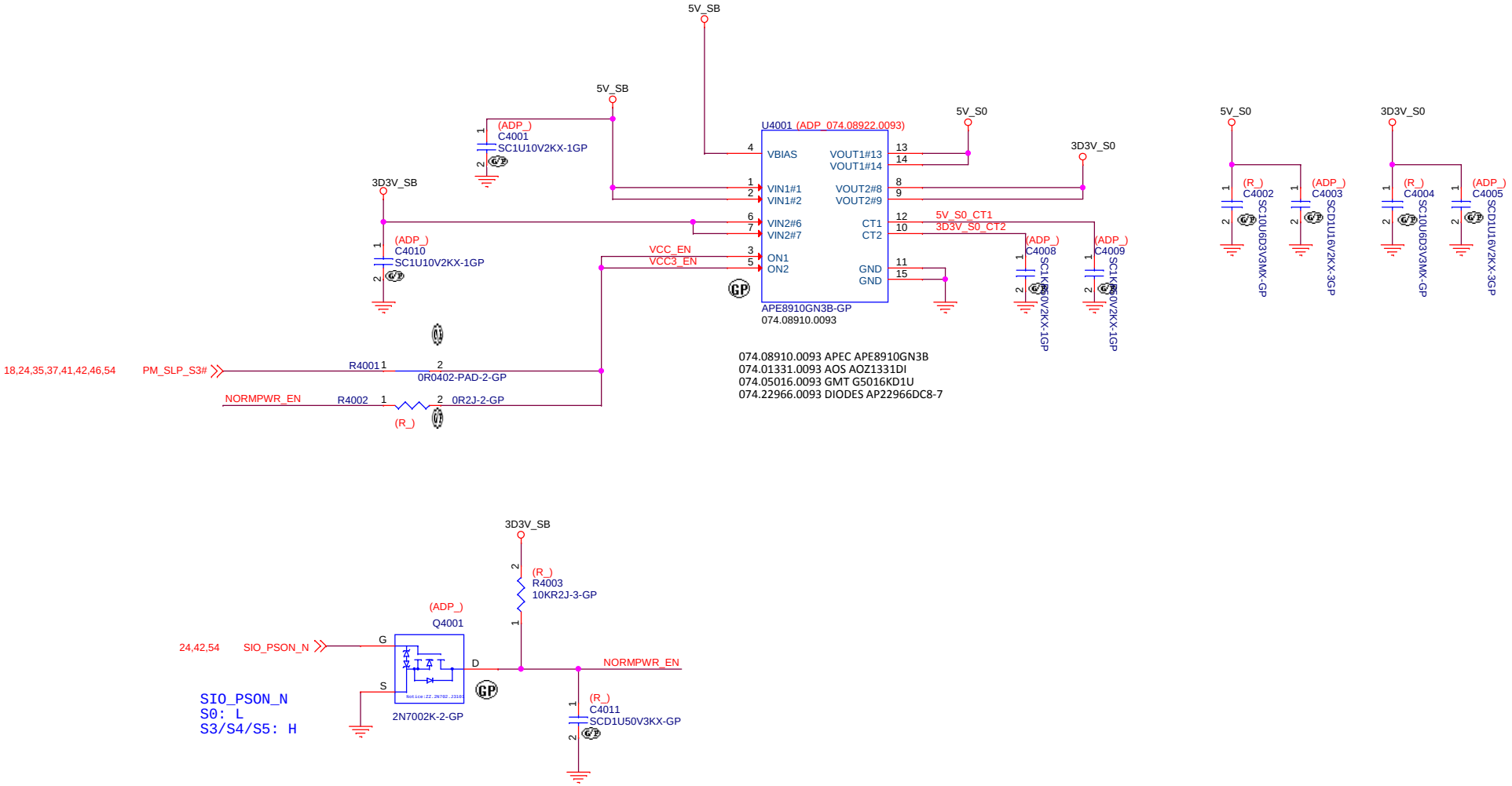
Run Power(5V_S0 & 3D3V_S0)



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Hsichih, Taipei Hsien

Title: 3D3V_S0/5V_S0		
Size: B	Document Number: Adma_APL	Rev: SA
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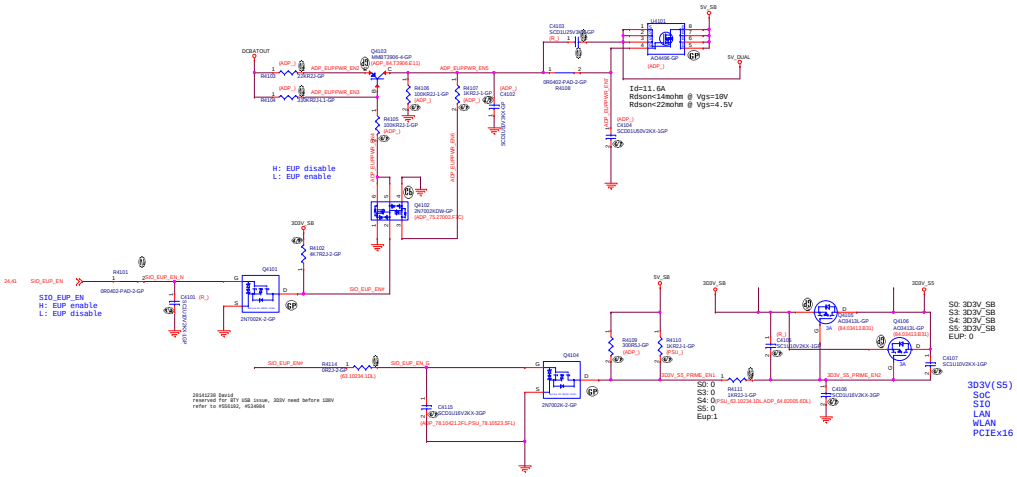
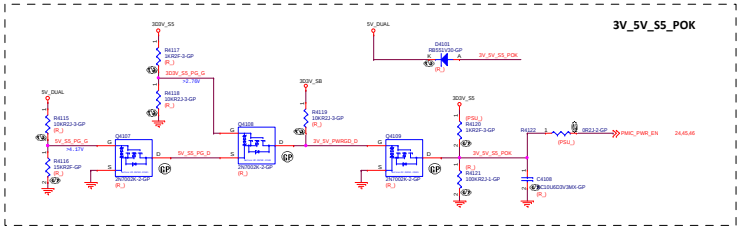
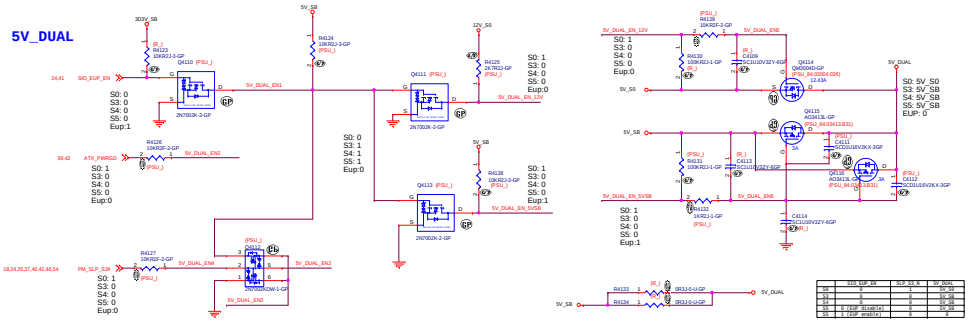
ADP Eup Power Control





PSU Eup Power Control



SIO_EUP_EN	SUP_S5_N	5V_DUAL
0	0	5V_S0
1	0	5V_S0
0	1	5V_SB
1 (EUP enable)	1	5V_SB

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Title	3D3V_S5/5V_S5
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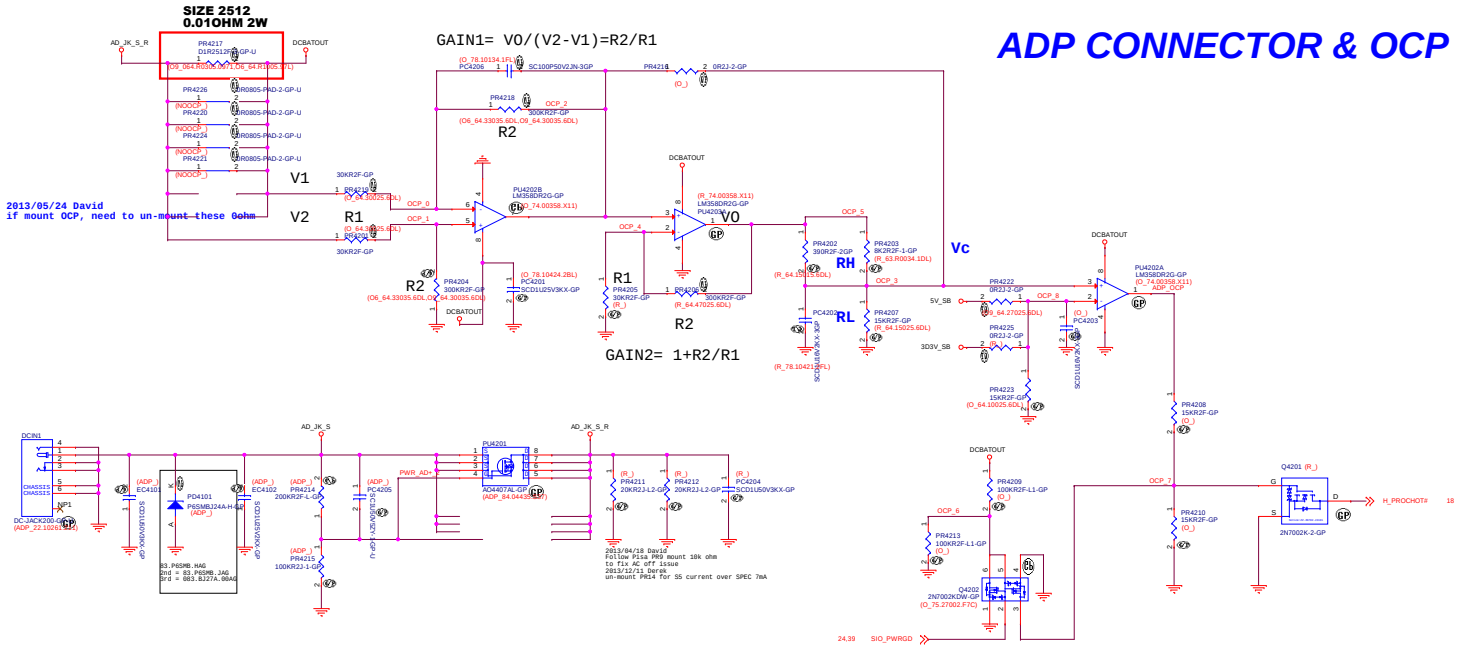
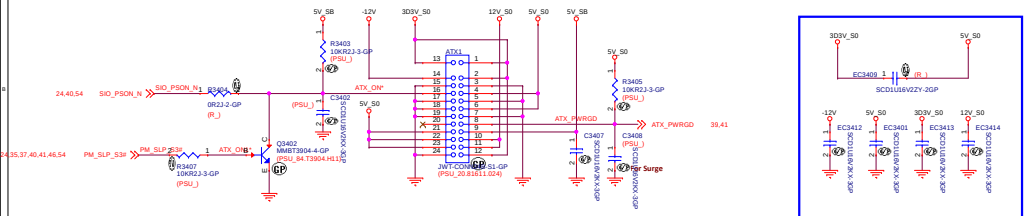
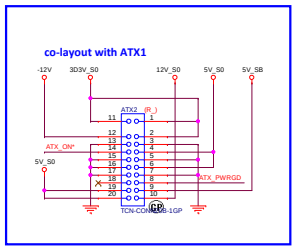
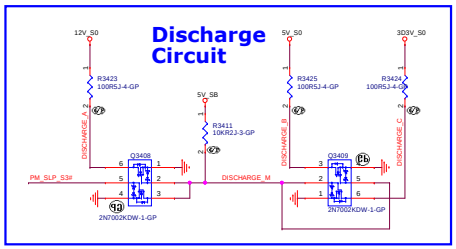
ADP CONNECTOR & OCP



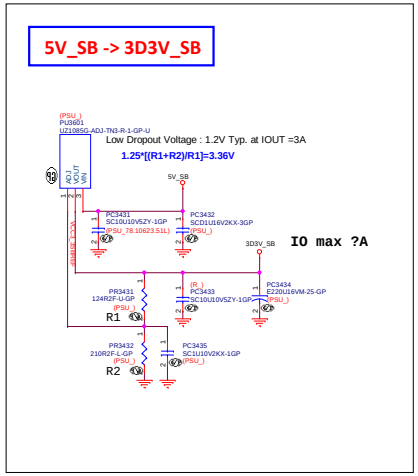
ATX CONNECTOR







20160424
ADP sku add discharge circuit



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Title: DCIN JACK	
Size: Custom	Document Number: Adma_APL
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Title
PWR_12V_(NCP1589A)

Size	Document Number	Rev
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Title
3D3V/5V_(RT6575D)

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V_5P0_A

V_3P3_A

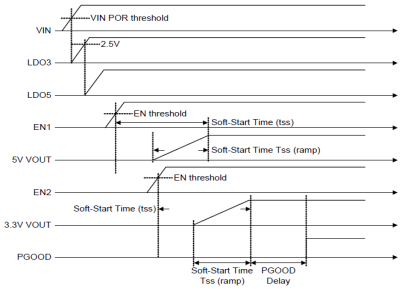

Figure 6. RT6575B Timing

3.3V Imax=5A
Iocp=7.5A

5V Imax=6.5A
Iocp=9.75A

2016/07/11
To solve PMIC_RSMRST will have a short high pulse when AC OFF at OS issue : RTC time fail.

2016/02/01 Modify

5V/3V ENABLE CONTROL

5V_S5_EN 45

3V_S5_EN 45

5V/3V POWER GOOD

3V_5V_PWRGD

PMIC_PWR_EN

PMIC_PWR_EN 24,41,46

Need EE confirm

2016/01/12
PR4431 PIN1 change connect to 5VLDO,Base on FAE suggest

EN pin
VIH=1.6V(min)
>4V

EN pin
VIH=1.6V(min)
>17.6V

<Variant Name>

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Title: CPU_IMVP8_NCP81266MN

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CPU CORE ENABLE CONTROL

24,41,45,46 PMIC_PWR_EN

CPU CORE POWER GOOD

24,39 PMIC_PWRGD

Others

18,46 PMIC_I2C_SDA
18,46 PMIC_I2C_SCL
18,24,35,37,46,53 PM_SLP_S4#
18,46 PM_SLP_SD#
18,24,35,37,40,41,45,46,54 PM_SLP_S3#
18,24,46 PMIC_RSMRST#
18,24,46 PMIC_THERMTRIP#
21,46 PMIC_IRQ
7,46 VCCGI_SENSE
7,46 VSSGI_SENSE
7,46 VNNCORE_SENSE

20151101 PWR modify

20151110 PWR modify

20151110 PWR modify

20151110 PWR modify

20151110 PWR modify

PMIC output for 1D8V_S0

SSID = CPU.Regulator

DDR_SEL Pin State	Buck6 Nominal Output Voltage
H	1.35V
L	1.2V

Cyntec 10*11.15*3.8mm DCR:3~3.3mOhm Irms : 18A , Isat : 28A

TDC=3A Fs=800Khz

Chilisin 2.5 x 2.0 x 1.2mm DCR:45~59mOhm Irms : 3.0~3.5A , Isat : 4.0~5.0A

TDC=1.5A

Chilisin 2.5 x 2.0 x 1.2mm DCR:102~115mOhm Irms : 2.0~2.3A , Isat : 3.3~3.8A

TDC=1.5A

2016/06/21 Delete PMIC_PWRGD

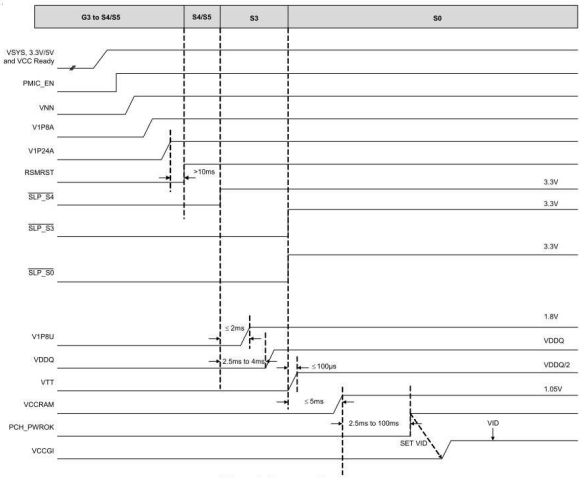

Figure 3. Power on Sequence

<Variant Name>

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Title: CPU_VCGI

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Main Func = CPU_VNN

For ADP sku, use "DCBATOUT" to input "PWR_DCBATOUT_VCCGI"
But
For PSU sku, use same trace as
"12V_S0" input "PWR_DCBATOUT_VCCGI"

DCBATOUT
PWR_DCBATOUT_VCCGI
PL4702 1 MHC1608S800QBP-GP
PL4703 1 MHC1608S800QBP-GP
12V_S0

Reserved for test (system stable)
If test pass with 3 MLCC, we can unmount
PC4708/PC4709/PC4710

PWR_DCBATOUT_VCCGI
PC4704 SC10U25V5KX-GP
PC4705 SC10U25V5KX-GP
PC4707 SC10U25V5KX-GP
PC4708 SC10U25V5KX-GP
PC4709 SC10U25V5KX-GP
PC4710 SE47U25VM-24-GP

5V_DUAL
PR4701 2D2R3J-2-GP
PC4701 SC1U10V2KX-1GP

PR4705 0R0603-PAD-1-GP-U
PWR_VCCGI_BOOT
PWR_VCCGI_BOOT_A
PC4706 SCD1U50V3KX-GP

PU4702 FDMS3600-02-RJK0215-COLAY-GP (075.07321.0073)

PU4701 RT9610BZQW-GP
VCC BOOT
EN UGATE
PWM PHASE
GND LGATE
GND

46 PWR_VCCGI_EN
46 PWR_VCCGI_PWM
PWR_VCCGI_VCC
PWR_VCCGI_HG
PWR_VCCGI_PH
PWR_VCCGI_LG

46 PWR_VCCGI_PHA
PG4702 GAP-CLOSE-PWR-3-GP

Mag 11.15 x 10 x 4.0mm
DCR : 0.86mOhm+/-7%
Idc : 35A , Isat :68A

Iccmax=21A

1V_CPU_VCGI
PL4701 IND-D22UH-47-GP
Fs=400KHz
22U 6.3V 0805 x 14
Place in Page 10 need check EE

(R_) PC4702 SC1KP50V2KX-1GP
PR4706 2K94R2F-GP
PC4703 SCD1U50V3KX-GP
PT4701 E820U2D5VM-19-GP
PWR_VCCGI_SNUB
(R_) PR4702 2D2R5F-2-GP
DY

PR4707 820R2F-GP
PR4704 562R2F-GP
(ADP_64.10015.6DL,PSU_64.82005.2DL)
2016/01/25 change R value
PR4707 499 -> 226 ohm
PR4704 825 -> 562 ohm
2016/06/13 change R value
PR4707 226 -> 820 ohm (PSU)
PR4707 226 -> 1K ohm (ADP)

PR4703 NTC-10K-GP (69.60013.161)
PR4708 0R0402-PAD-1-GP

46 PWR_ISENSEP2
46 PWR_ISENSEN2

PG4701 GAP-CLOSE-PWR-3-GP
46 FBL_VCCGI

<Variant Name>

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Title	V_SM/VTT_(RT8231A)	
Size A	Document Number Adma_APL	Rev SA
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Title
Reserved

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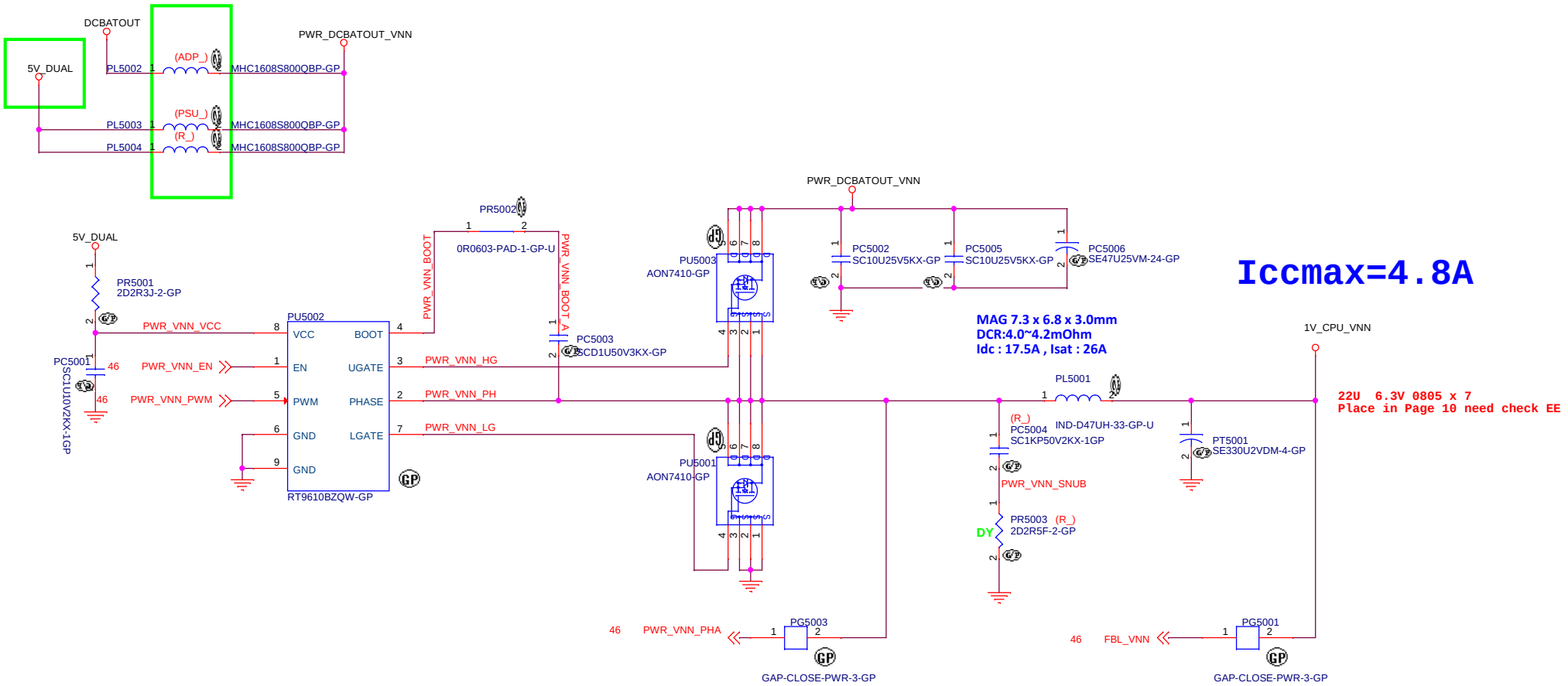
1V_CPU_VNN



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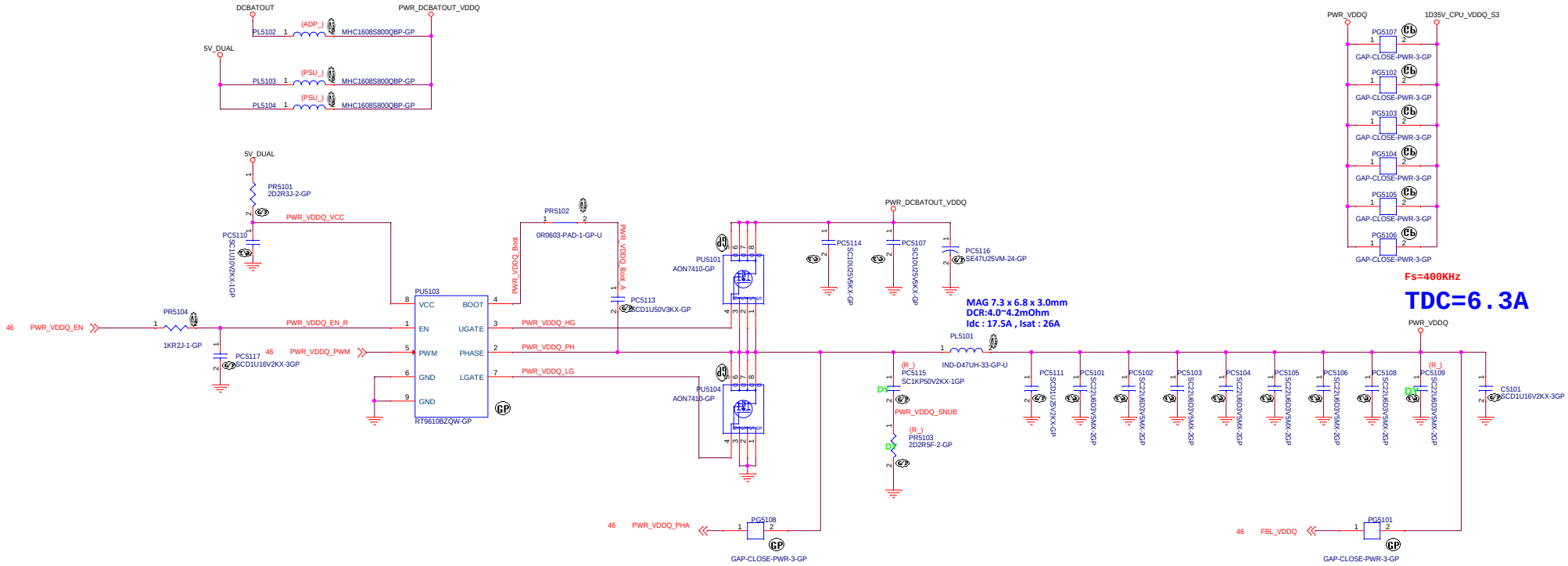
VDDQ



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Size	Document Number	Rev
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Title
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Size	Document Number	Rev
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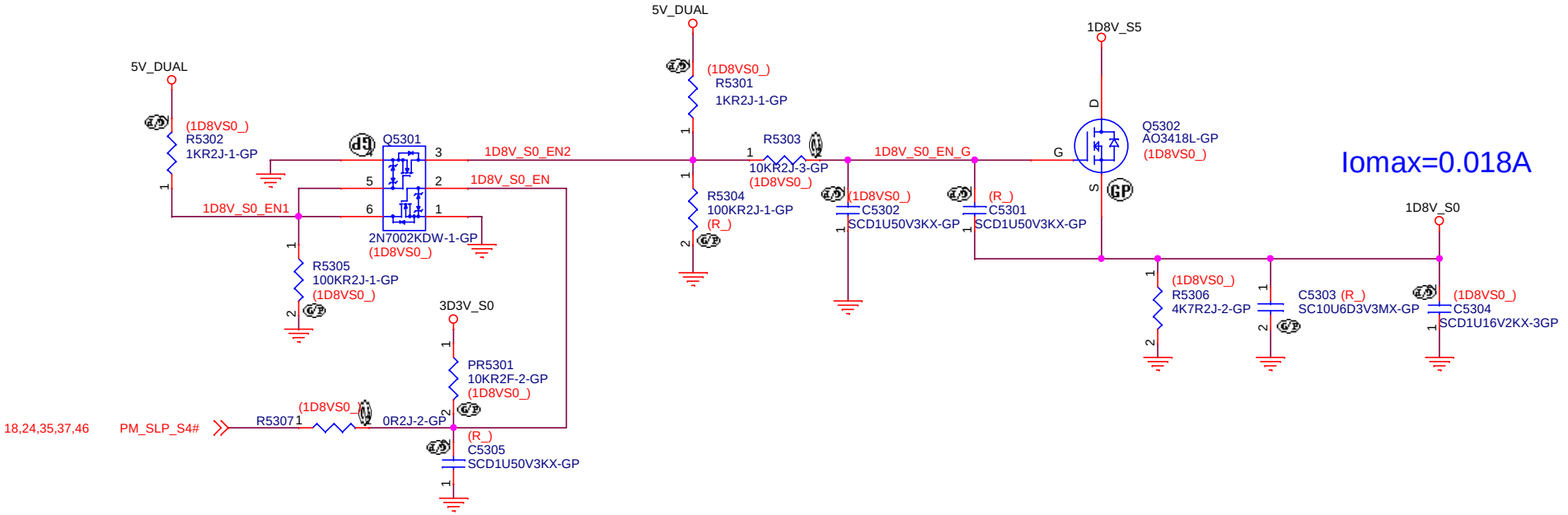
1.8V_S0



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Title: **1D8V_S0**		
Size: Custom	Document Number: **Adma_APL**	Rev: SA
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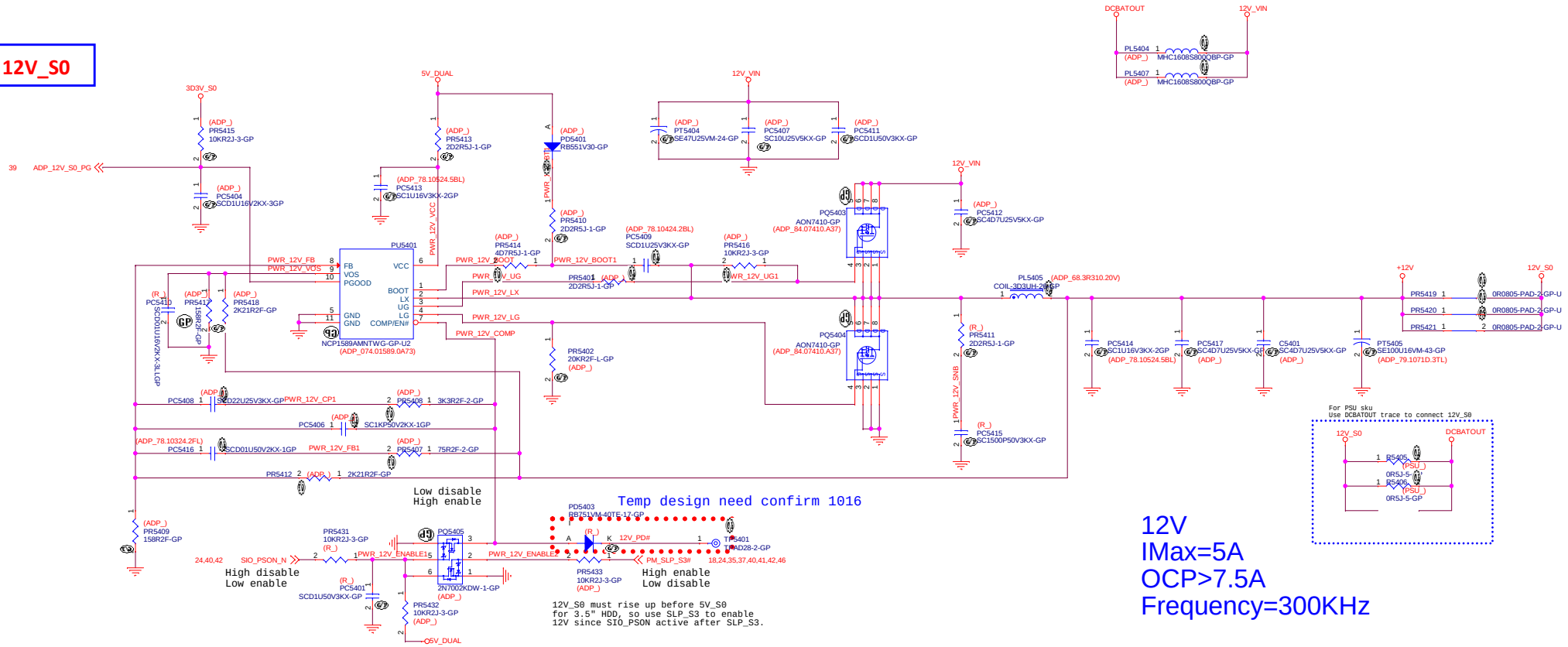
19V_A -> 12V_S0



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DP to RTD2166

For Debug

RTD2166 Slave Address:
0x64/0x65, 0x68/0x69

pull-high at p.17 (3D3V_S0)

Operation Mode Selection Table(Power on latch)

		POL1_SPICEB(PIN10)	
		0	1
POL2(PIN9)	0	Not use, for Internal Test Purpose	Not use, for Internal Test Purpose
	1	ROM MODE	External Flash Mode

ROM Mode:
PIN29/30 pull high, connect to SMB_SDA/SMB_SCL(PCH)
PIN10 pull down, PIN9 pull high

External Flash Mode:
PIN29/30 pull high, connect to SMB_SDA/SMB_SCL(PCH)
PIN9 pull high
PIN10 pull high, connect to SPI FLASH
PIN11/12/13 connect to SPI FLASH

Close pin25

20 mils

6 via on Body PAD

To SOC HPD

VGA cable
un-Plug: Low
Plug: High

20140708 David
vendor suggest from
33 to 0ohm

<Variant Name>

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Title: DP to VGA_(RTD2166)

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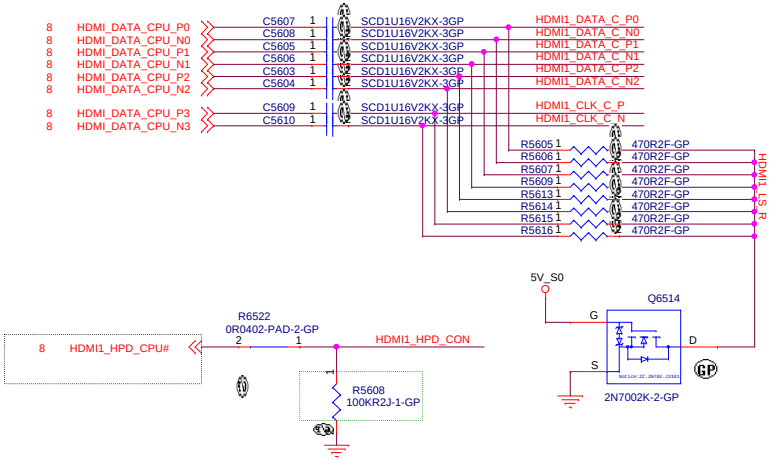

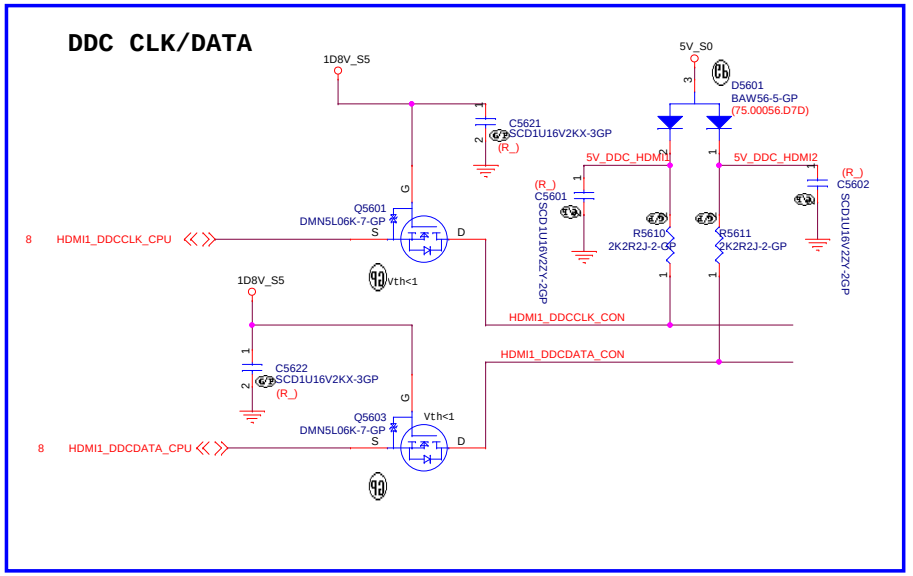

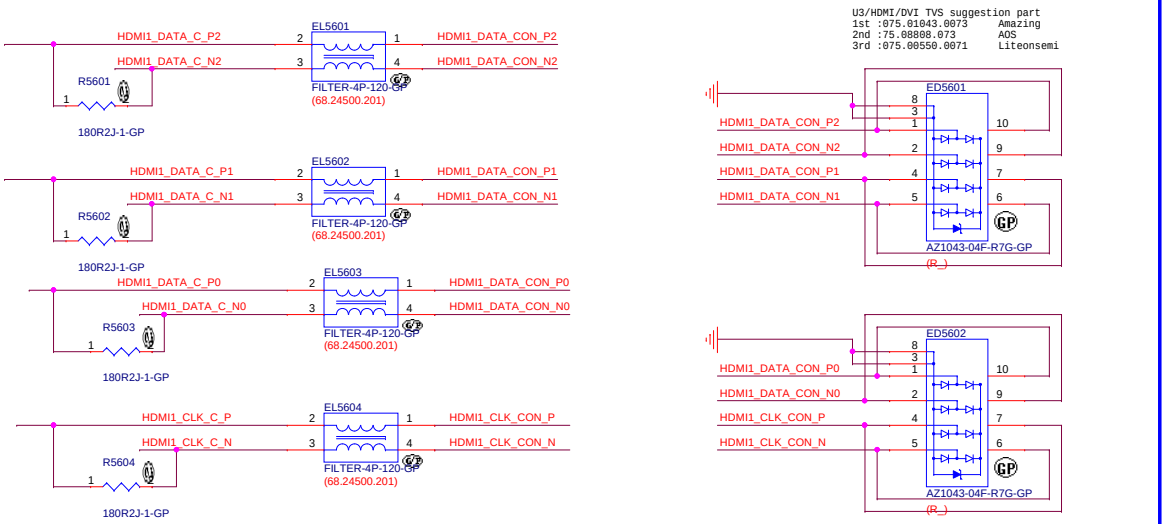

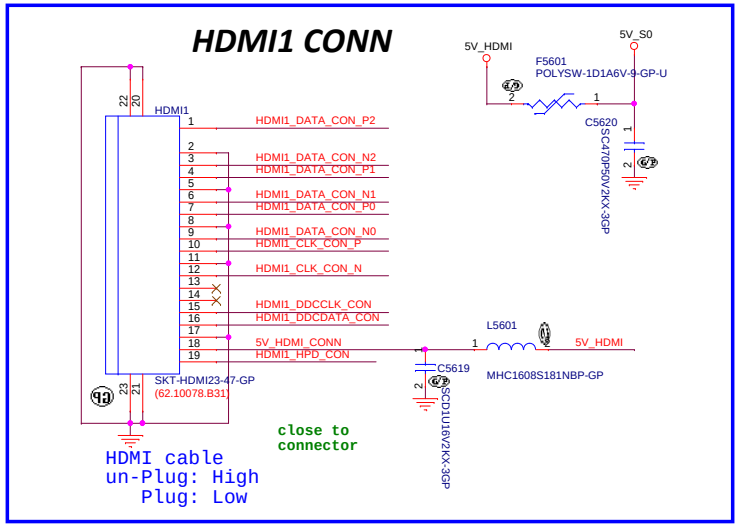

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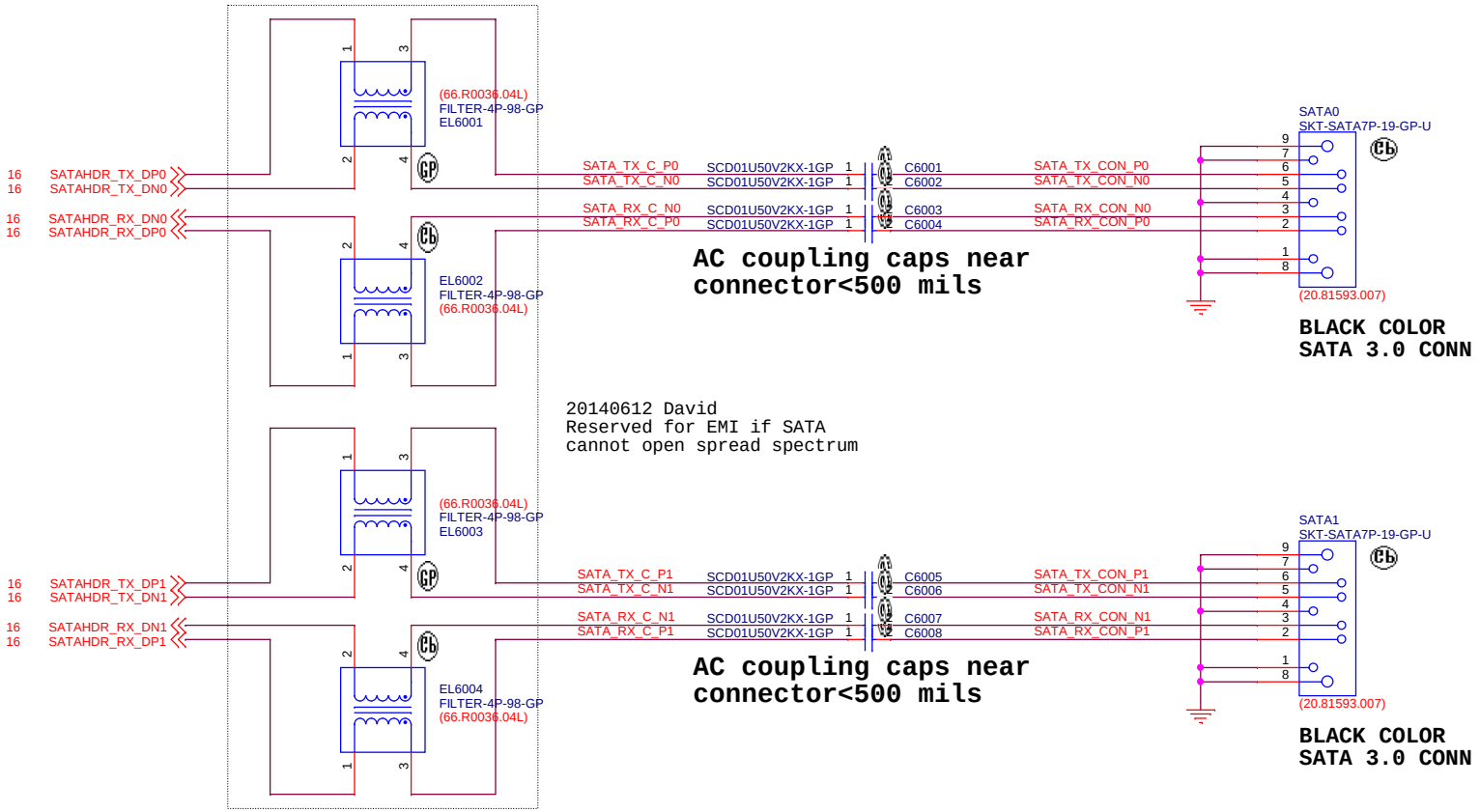
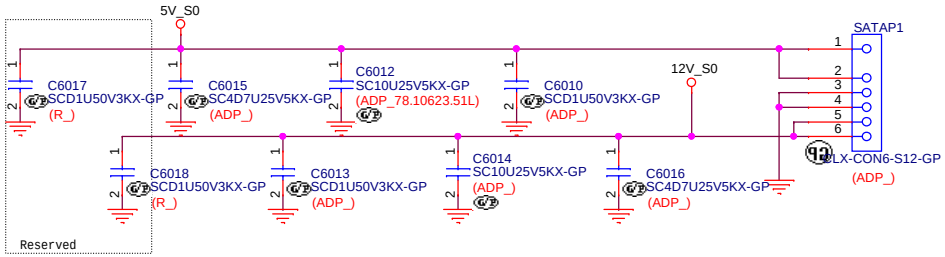
SSID = HDD/ODD



20140612 David
Reserved for EMI if SATA
cannot open spread spectrum



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Title: HDD/ODD		
Size: B	Document Number: Adma_APL	Rev: SA
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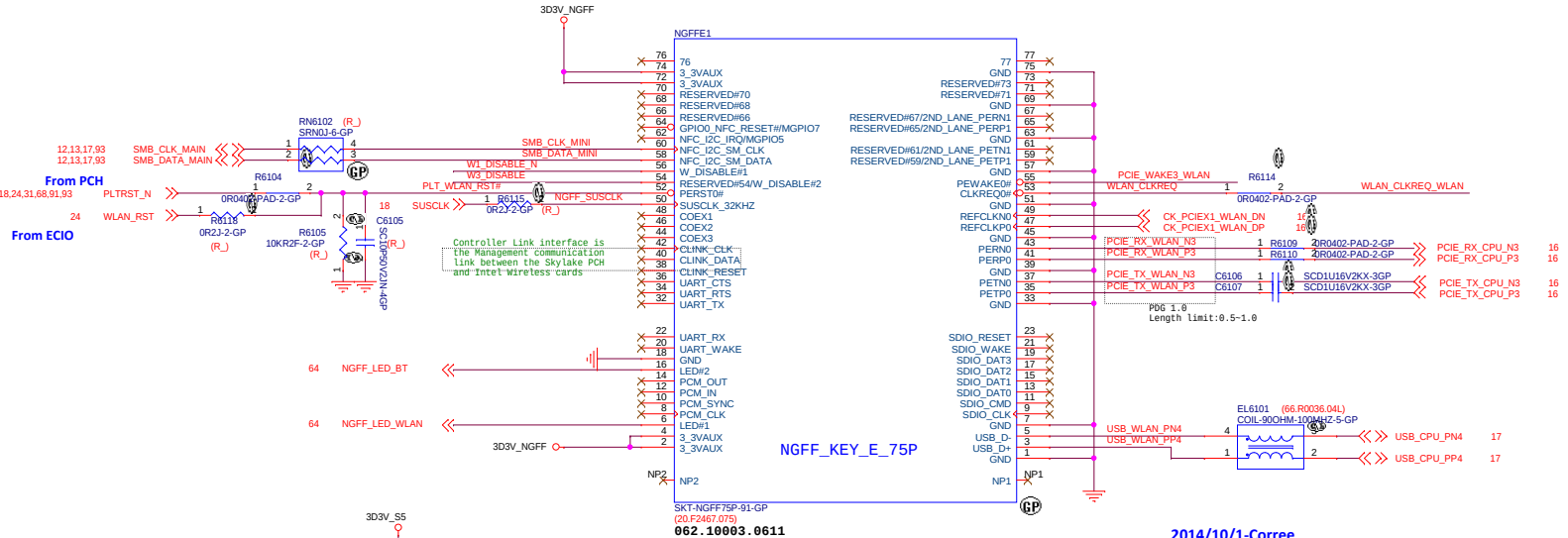
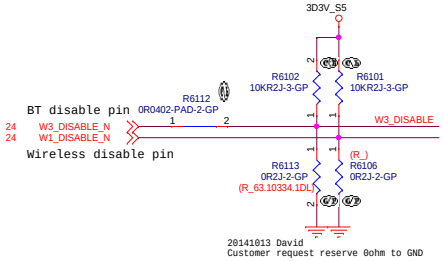
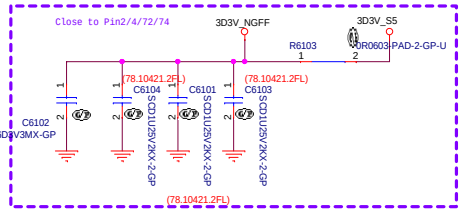
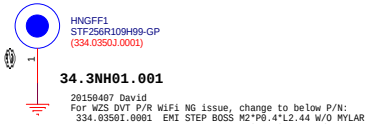
M.2 2230 / 1630 Key E Type (Wireless LAN+BT)

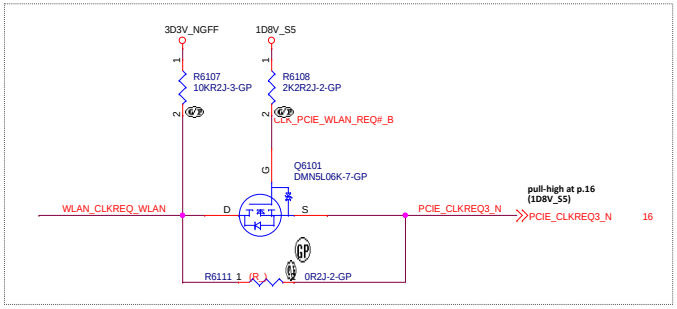


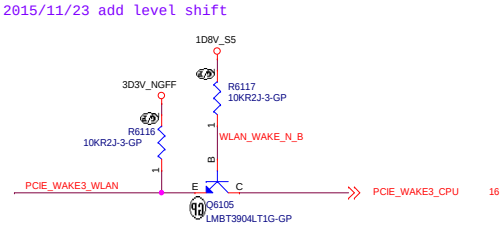




2014/10/1-Corree
Change to 34.3NH01.001 that follow Sqwerty







PCIEx1 wake

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21F, 88, Sec.1, Hsin Tai Wu Rd
Hsichih, Taipei Hsien

Title: NGFF CONN

Size: Custom | Document Number: Adma_APL | Rev: SA

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Title
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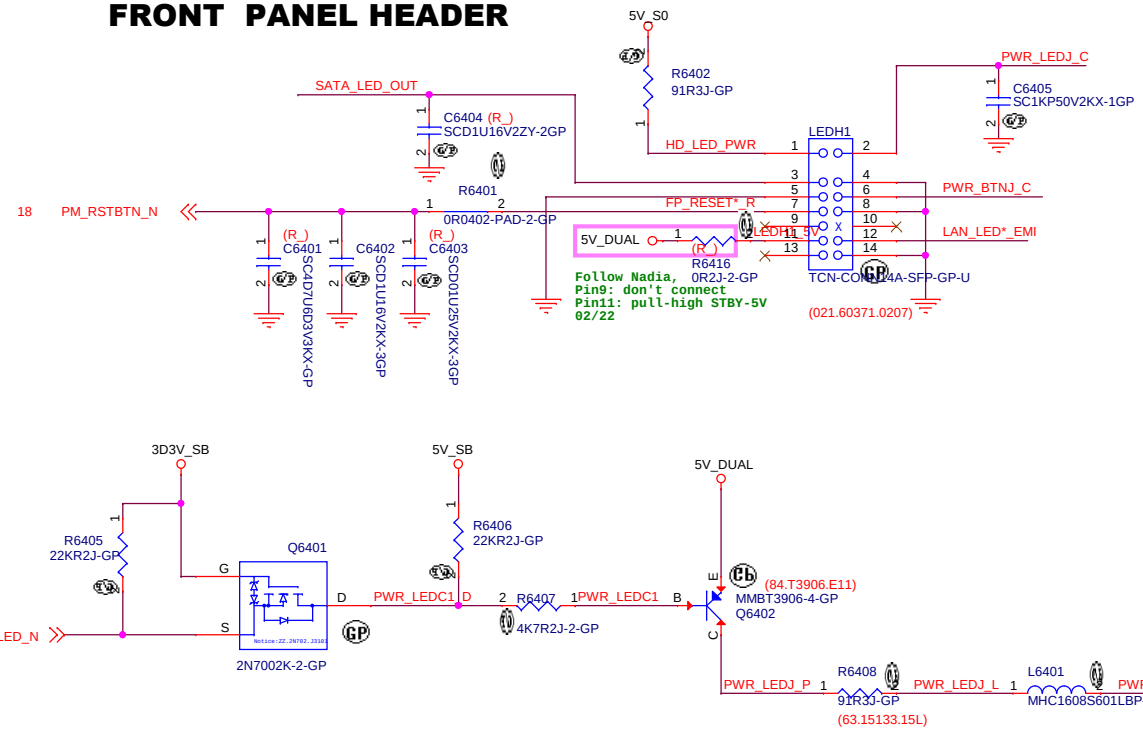
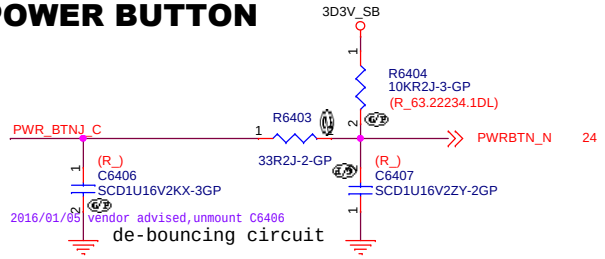
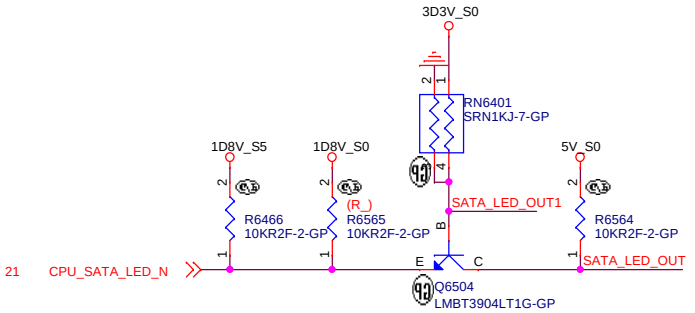
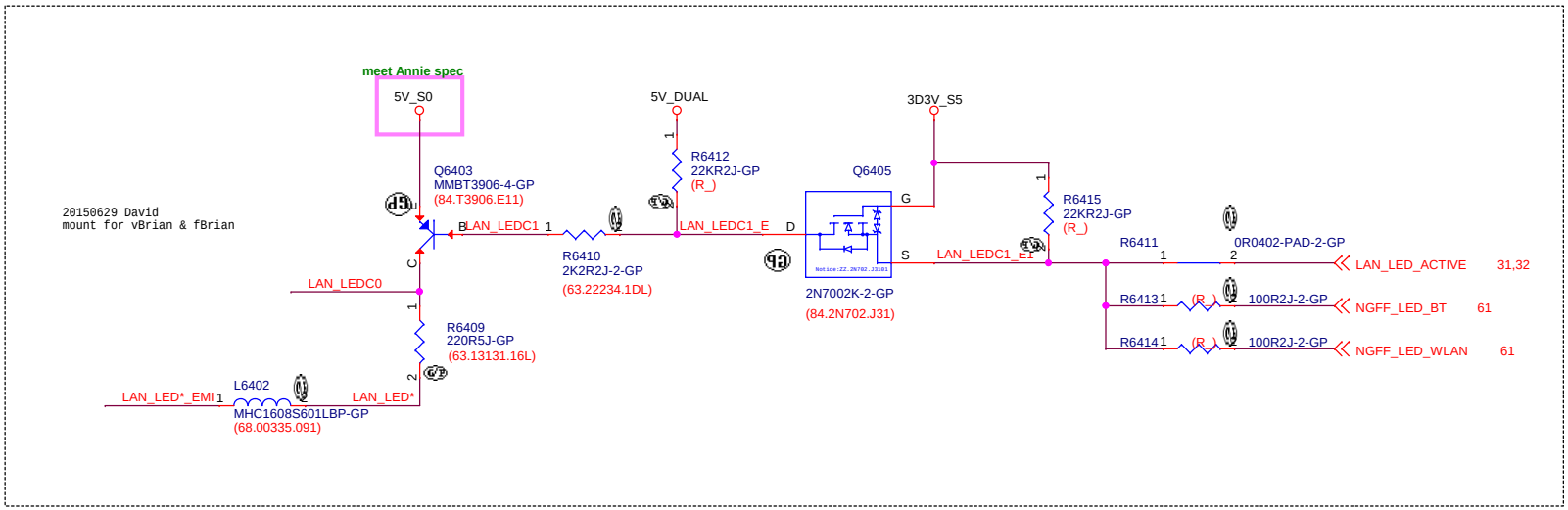
FRONT PANEL HEADER



POWER BUTTON







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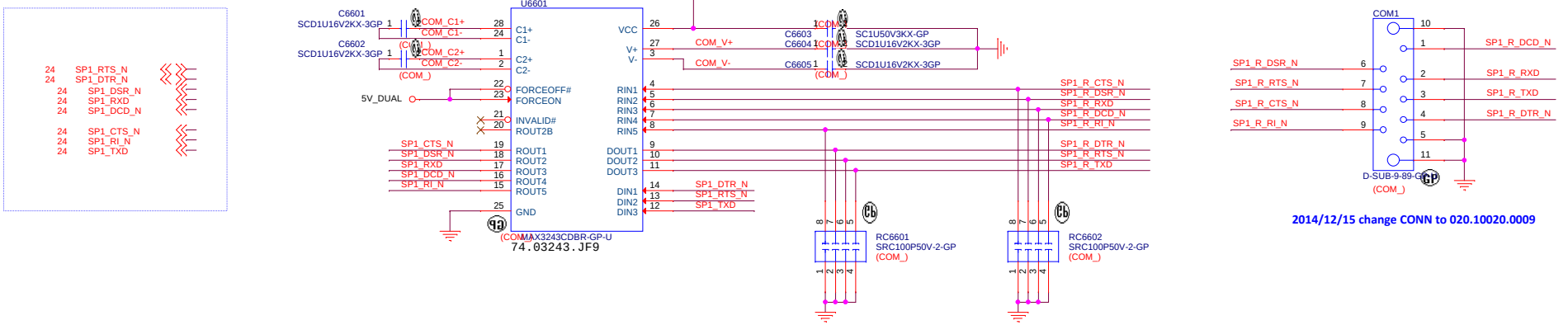
COM1

2014/9/30-SA Vita
change COM2 power to +5V_AUX2

SERIAL PORT



2014/12/15 change CONN to 020.10020.0009

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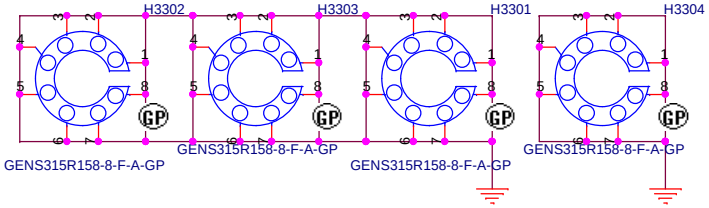
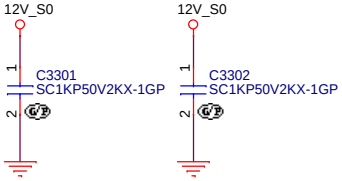
Scre Hole (PCB New type MOUNTING HOLES)



Bogis 20130826
Del R3301
Connect H3304 from ESDGND to GND



LABEL

LBL1
LABEL
(40.3BZ24.011)

LBL2
LABEL
(R_45.41101.011)

LBL3
LABEL
(R_40.3KP03.001)

```
45.41107.011 (一般的紙，70x8mm過完高溫reflow之後會變的偏黃)
45.41101.001 (一般的紙，35x15mm，過完高溫reflow之後會變的偏黃)
40.3KP03.001 (高溫貼紙，35x15mm，過完高溫reflow之後紙還是很白)

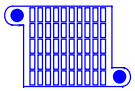
2015/02/02 WZS's request
35x15 (40.3KP03.011)
30x15 (40.3BZ24.011)
70x8  (45.41107.021)
```

Battery Symbol

BAT2
BATTERY CR2032
(23.20068.001)

23.20068.001 KTS BBBCR2032BX
23.20023.311 MITSUBISHI CR2032 MITSUBISHI
23.22063.001 JHT CR2032 JHT

HeatSink Symbol



CPUHS1
HEATSINK
(360.06R02.0001)

```
2016/06/06  Adam change
1st  360.06R02.0001
2nd  360.06R02.0011
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SSID = DEBUG PORT

LPC DEBUG PORT

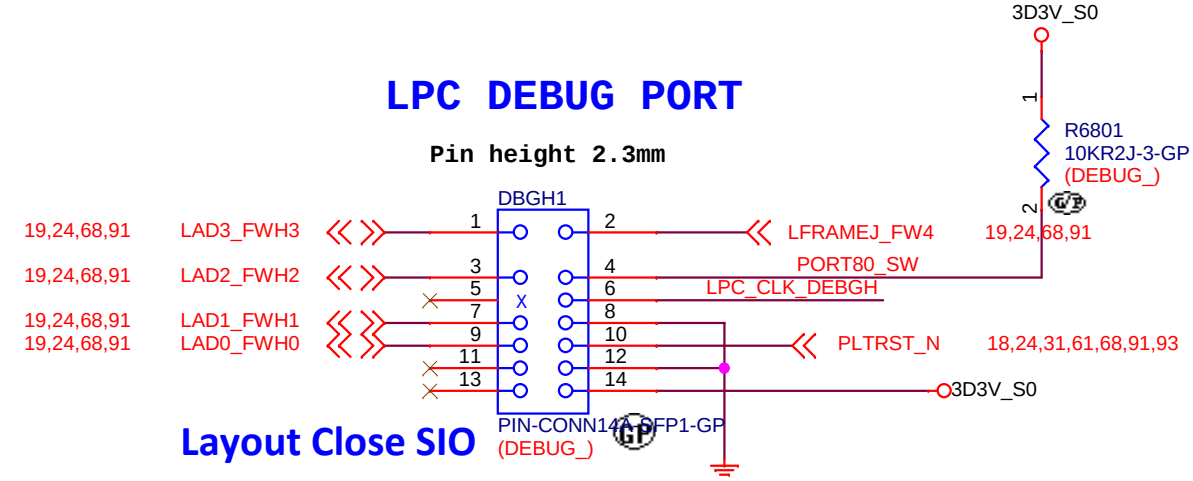
19,24,68,91 LAD0_FWH0
19,24,68,91 LAD1_FWH1
19,24,68,91 LAD2_FWH2
19,24,68,91 LAD3_FWH3
19,24,68,91 LFRAMEJ_FW4

19,24,91 LPC_CLK1

18,24,31,61,68,91,93 PLTRST_N

LPC DEBUG PORT

Pin height 2.3mm



Layout Close SIO

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Title: DEBUG CONNECTOR

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19,24,68 LAD0_FWH0
19,24,68 LAD1_FWH1
19,24,68 LAD2_FWH2
19,24,68 LAD3_FWH3
19,24,68 LFRAMEJ_FW4

19,24,68 LPC_CLK1

18,24,31,61,68,93 PLTRST_N

18 PM_SUS_STAT#

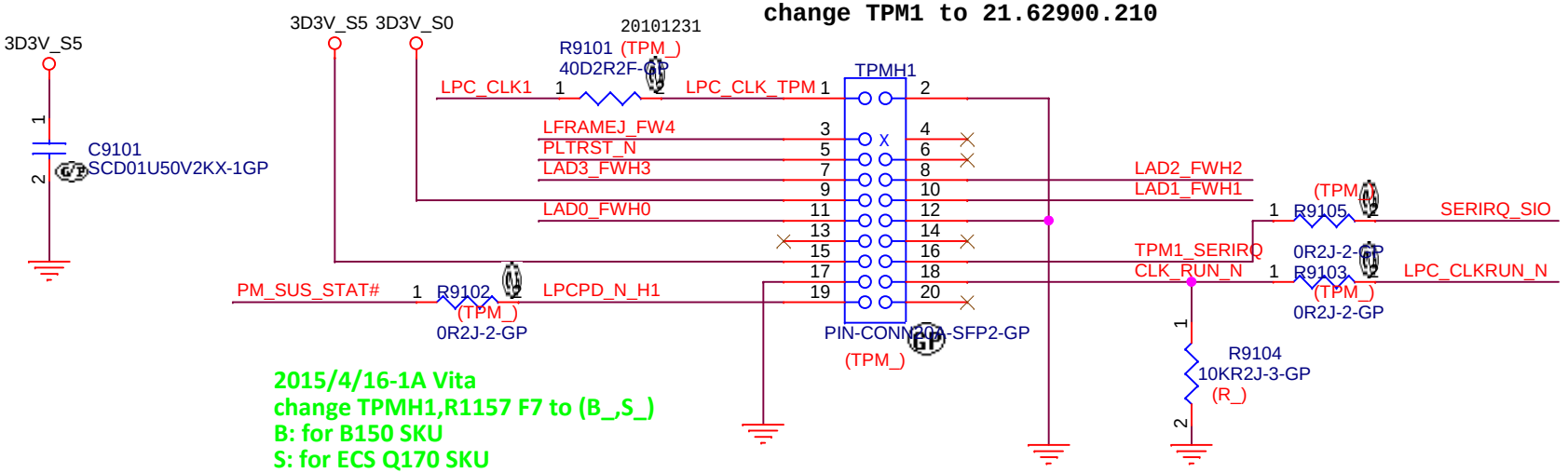
19 LPC_CLKRUN_N

19,24 SERIRQ_SIO

2014/8/1
need check pin define
2014/8/3-Corree
Change to DT TPM design

TPM 2.54 pitch Header

2014/8/7
change TPM1 to 21.62900.210



2015/4/16-1A Vita
change TPMH1,R1157 F7 to (B_,S_)
B: for B150 SKU
S: for ECS Q170 SKU

<Variant Name>

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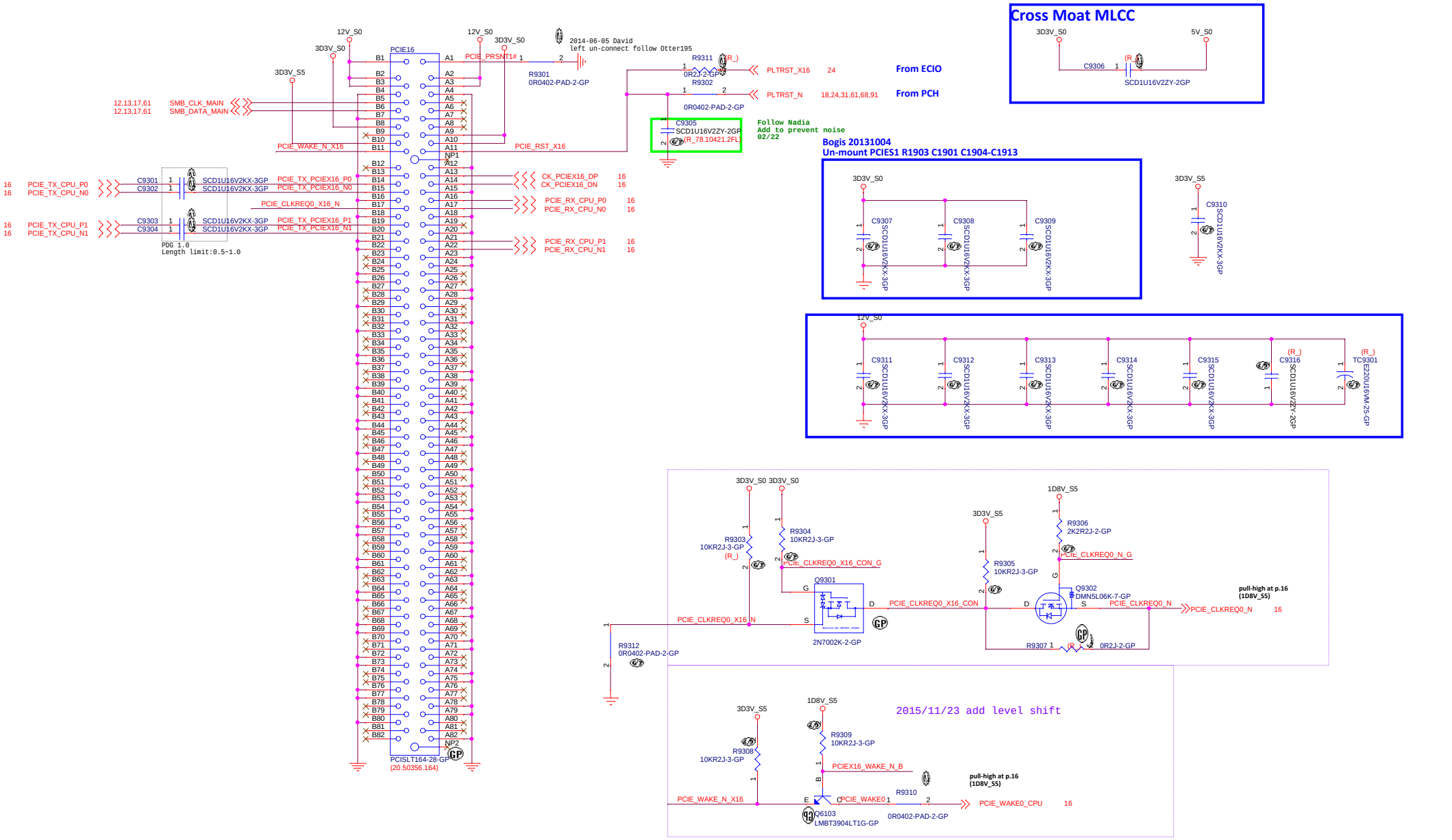
PCIEx16 CONN

PCIEx16 Power Estimation for 75W Card
12V_S0 @ 5.5A
3D3V_S0 @ 3A
3D3V_S5 @ 0.375A



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21F, 88, Sec.1, Hsin Tai Wu Rd
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Title: Express Card

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MIPI-60 Connector Pinout
Samtec QSH-030-01-L-D-A
CRB p159

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Source	Destination	Signal
RTC Battery	CPU/SIO	RTC_VCC
RTC Battery	CPU/SIO	RTC_TEST# RTC_RST#
Adaptor	MB	DCBATOUT
VRs	CPU/SIO	V_3P3_A V_5P0_A
Power Button	SIO	PWRBTN_N
SIO	VRs	SIO_EUP_EN#
VRs	MB	VNN
VRs	MB	1D05V_S5
VRs	MB	1D15V_S5
VRs	MB	1D24V_S5
VRs	MB	1D8V_S5
VRs	MB	SB3V/SB5V
SIO	CPU	RSMRST_N
SIO	CPU	PMC_PWBTN_N
CPU	SIO / VRs	SLP_S4#
VRs	MB	DDR_VDDQ
MB	CPU	DDR3_DRAM_PWROK
CPU	SIO / VRs	SLP_S3#
SIO	VRs	SIO_PSON#
VRs	MB	1D5V_S0
VRs	MB	VCC3 VCCS
VRs	CPU	VGG
VRs	MB	VCC0/1
VRs	MB	MEM_VTT
VRs	MB	1D8V_S0
SIO	MB	PWRGD_3V
SIO	CPU	PMC_CORE_PWROK
SIO	CPU	DDR3_VCCA_PWROK
CPU	MB	PMC_PLTRST#

RTC Power Well Timing Diagrams

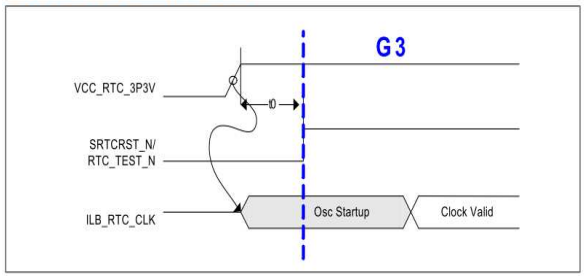


Figure 4-2. Apollo Lake G3 Cold Boot Power-Up

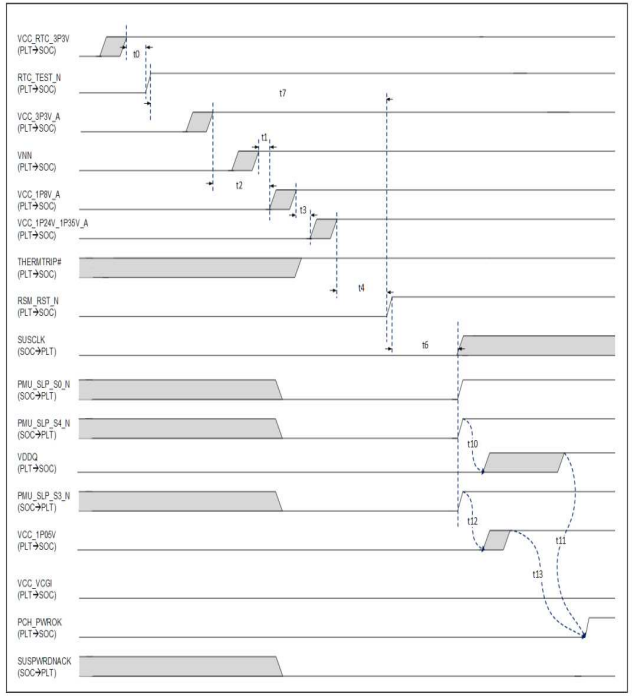
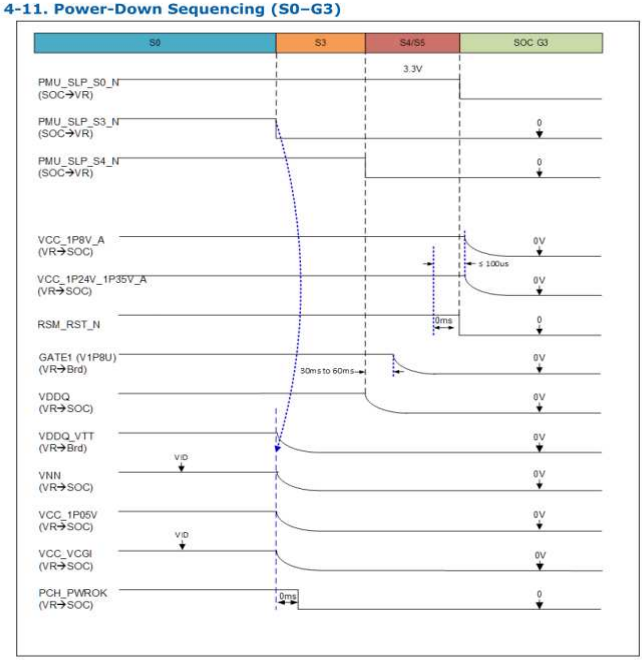
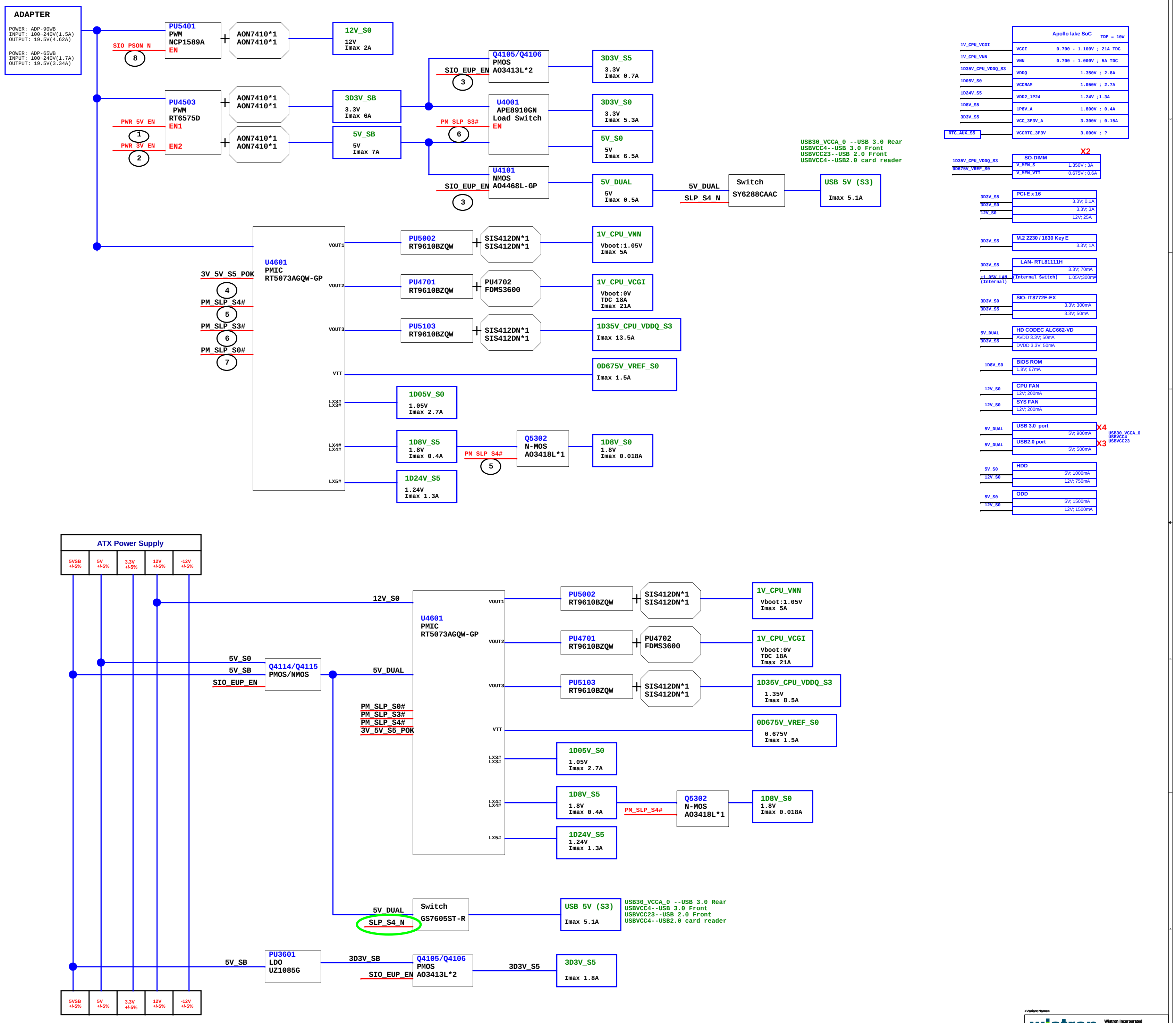
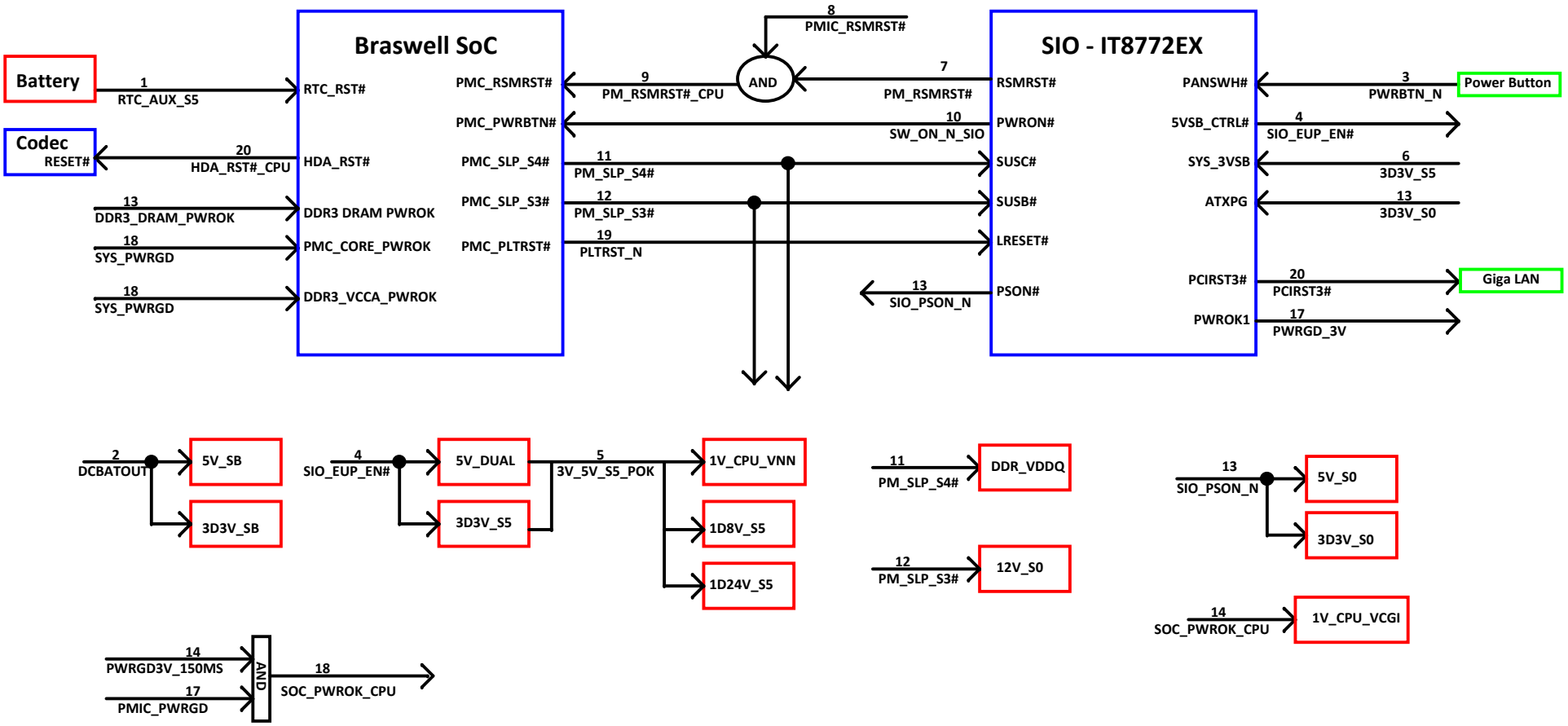


Figure 4-11. Power-Down Sequencing (S0–G3)




ADAPTER
POWER: ADP-90WB
INPUT: 100~240V(1.5A)
OUTPUT: 19.5V(4.62A)
POWER: ADP-65WB
INPUT: 100~240V(1.7A)
OUTPUT: 19.5V(3.34A)
PU5401 PWM NCP1589A EN
SIO_PSON_N
AON7410*1 AON7410*1
12V_S0 12V Imax 2A
PU4503 PWM RT6575D EN1 EN2
PWR_5V_EN
PWR_3V_EN
3D3V_SB 3.3V Imax 6A
5V_SB 5V Imax 7A
Q4105/Q4106 PMOS AO3413L*2
SIO_EUP_EN
3D3V_S5 3.3V Imax 0.7A
U4001 APE8910GN Load Switch EN
PM_SLP_S3#
3D3V_S0 3.3V Imax 5.3A
5V_S0 5V Imax 6.5A
U4101 NMOS AO4468L-GP
5V_DUAL 5V Imax 0.5A
SLP_S4_N
Switch SY6288CAAC
USB 5V (S3) Imax 5.1A
USB30_VCCA_0 --USB 3.0 Rear
USBVCC4--USB 3.0 Front
USBVCC23--USB 2.0 Front
USBVCC4--USB2.0 card reader
U4601 PMIC RT5073AGQW-GP
3V_5V_S5_POK
PM_SLP_S4#
PM_SLP_S3#
PM_SLP_S0#
VOUT1 VOUT2 VOUT3 VTT LX3# LX4# LX5#
PU5002 RT9610BZQW
SIS412DN*1 SIS412DN*1
1V_CPU_VNN Vboot:1.05V Imax 5A
PU4701 RT9610BZQW
PU4702 FDMS3600
1V_CPU_VCGI Vboot:0V TDC 18A Imax 21A
PU5103 RT9610BZQW
1D35V_CPU_VDDQ_S3 Imax 13.5A
0D675V_VREF_S0 Imax 1.5A
1D05V_S0 1.05V Imax 2.7A
1D8V_S5 1.8V Imax 0.4A
Q5302 N-MOS AO3418L*1
1D8V_S0 1.8V Imax 0.018A
1D24V_S5 1.24V Imax 1.3A
Apollo lake SoC TDP = 10W
VCGI 0.700 - 1.100V ; 21A TDC
VNN 0.700 - 1.000V ; 5A TDC
VDDQ 1.350V ; 2.8A
VCCRAM 1.050V ; 2.7A
VDD2_1P24 1.24V ;1.3A
1P8V_A 1.800V ; 0.4A
VCC_3P3V_A 3.300V ; 0.15A
VCCRTC_3P3V 3.000V ; ?
1V_CPU_VCGI 1V_CPU_VNN 1D35V_CPU_VDDQ_S3 1D05V_S0 1D24V_S5 1D8V_S5 3D3V_S5 RTC_AUX_S5
SO-DIMM X2
V_MEM_S 1.350V ; 3A
V_MEM_VTT 0.675V ; 0.6A
PCI-E x 16 3.3V; 0.1A 3.3V; 3A 12V; 25A
M.2 2230 / 1630 Key E 3.3V; 1A
LAN- RTL8111H 3.3V; 70mA (Internal Switch) 1.05V;300mA
SIO- IT8772E-EX 3.3V; 300mA 3.3V; 50mA
HD CODEC ALC662-VD AVDD 3.3V; 50mA DVDD 3.3V; 50mA
BIOS ROM 1.8V; 67mA
CPU FAN 12V; 200mA
SYS FAN 12V; 200mA
USB 3.0 port 5V; 900mA X4
USB2.0 port 5V; 500mA X3
USB30_VCCA_0 USBVCC4 USBVCC23
HDD 5V; 1000mA 12V; 750mA
ODD 5V; 1500mA 12V; 1500mA
ATX Power Supply
5VSB +/-5% 5V +/-5% 3.3V +/-5% 12V +/-5% -12V +/-5%
12V_S0
5V_S0
5V_SB
SIO_EUP_EN
Q4114/Q4115 PMOS/NMOS
5V_DUAL
1D35V_CPU_VDDQ_S3 1.35V Imax 8.5A
0D675V_VREF_S0 0.675V Imax 1.5A
Switch GS7605ST-R
SLP_S4_N
PU3601 LDO UZ1085G
3D3V_SB
3D3V_S5 Imax 1.8A



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Hsichih, Taipei Hsien

Title: Power Good & Reset Diagram

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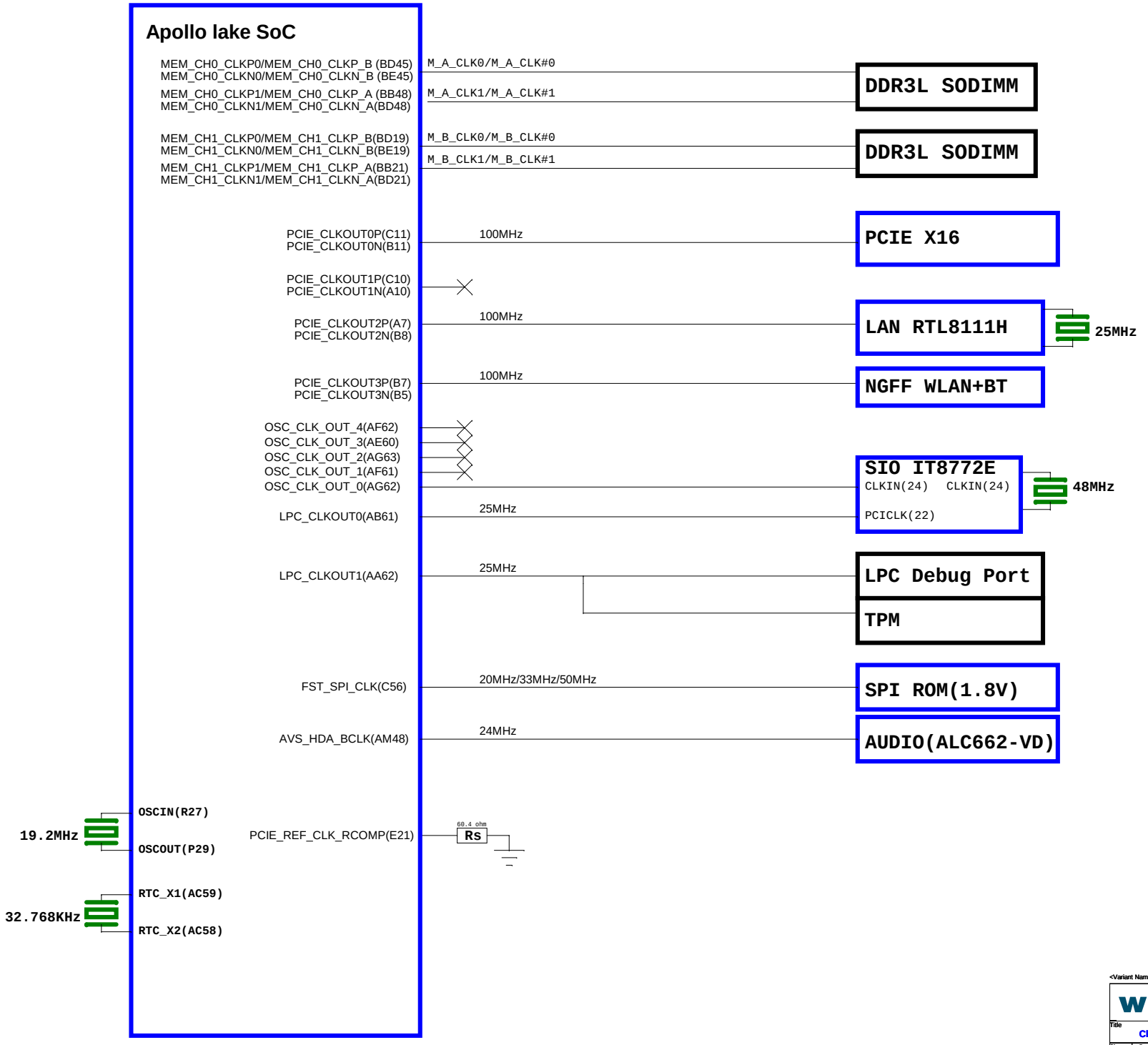

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Title: Clock Diagram

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