Model: Mission Hills/Sawgrass
PCB Ver: A00
PCB Number: 10097-1
SCH Ver: 06
PCBA:

PAGE	TITLE	Quantity
01	Cover Page	
02	BLOCK DIAGRAM	
03	Power Delivery	
04	POWER GOOD AND RESET DIAGRAM	
05	CLOCKS DIAGRAM	
06	Power Sequence	
07	POWER Map	
08	GPIO	
09	CLOCK GEN - CK505	
10	CPU LGA 1155_1	
11	CPU LGA 1155_2	
12	CPU LGA 1155_3	
13	CPU LGA 1155_4	
14	XDP/80 PORT HEADER	
15	DDR3 CHA DIMM 0	
16	TBD	
17	DDR3 CHB DIMM 0	
18	TBD	
19	PCH_Cougar_AUDIO/GPIO/SPI	
20	PCH_Cougar_CLK/FDI/ONFI	
21	PCH_Cougar_SATA/FAN/DP	
22	PCH_Cougar_PCI/PCIE/DMI/USB	
23	PCH_Cougar_GND/STRAPS	
24	PCH_Cougar_POWER	
25	SATA Port	
26	PCIEX16 CONNECTOR	
27	VGA Port	
28	HDMI Port	
29	TBD	
30	FRONT USB	
31	USB+RJ45 / REAR USB	
32	Gb LAN RTL8151ED	
33	AUDIO CX20641/CX20651	
34	AUDIO CODEC JACKS	
35	DSW	
36	SIO SCH5514E	
37	KeyBoard and MouSe	
38	Serial & Parallel port	
39	FAN CIRCUITS/HOLE	
40	TBD	
41	PCIEX1 CONNECTOR	
42	TBD	
43	TBD	
44	TBD	
45	PWR/FNT PNL	
46	DUAL POWER	
47	DDR POWER	
48	SYSTEM POWER	
49	CPU_VTT & CPU_SA	
50	CPU_VRD 12-1 & CPU_AXG	
51	CPU_VRD 12-2	

PCB BOARD SIZE
4 Layers
244mmX 218mm

BOM Configuration
Unmount:(R)
Unmount after MP (X)

SB BUILD

Sugar Bay :

LGA1155 : Sandy Brighe

Chipset : Cougar Point H61

LAN : Gb LAN RTL8151ED

<Variant Name>

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PCB BOARD SIZE
244mmX 218mm
4 Layer

Internal Slot/Header
Front/Rear IO
Chipset

VRM 12
(3 Phase 95W)

PCIE_X16

PCI EXPRESS Gen2

INTEL
Sandy Bridge
SOCKET FCLGA LGA1155
(95W)
0.9144mmX0.9144mm

Channel A
64 bit
1066/1333MHZ

DDR3 DIMM
Unbuffered 4GB

Channel B
64 bit
1066/1333MHZ

DDR3 DIMM
Unbuffered 4GB

100MHz
100MHz

FDI
DMI

PECI
Wait for change

14.318MHz
33MHz
24MHz or 48MHz
100 MHz
120 MHz
133 MHz

PCH
CLOCK
Buffer

25M

D-SUB PORT
RGB

HDMI PORT
Port D

INTEL PCH
Sugar Bay

FCBGA 942PIN
27mm X 27mm

PCIE Gen1 Interface
PCIE X1

PCIE Gen1 Interface
PCIE X1

PCIE Gen1 Interface
PCIE X1

PCIE Gen1 Interface
Realtek LAN
RTL8111E-VL

RJ45

25M

ATX-24PIN PWR CONN

CPU-4PIN CONN

USB2.0X2 FRONT HEADER
USB2.0X2 FRONT HEADER
USB2.0x2 REAR (+RJ45)
USB2.0x2 REAR
USB2.0x2 REAR

USB 2.0 *10
480Mb/S

SPI Flash ROM
4MB/2MB
SPI BUS

SATA *4
SATA2.0 BUS

133MHz
100MHz
96MHz
14.318MHz
32.768KHz
32.7K

REAR
Line - IN
REAR
Line - Out
REAR
MIC -IN
FRONT
MIC -IN
FRONT
HP - OUT

HDA CODEC
CX20641/20651
High Definition Audio

LPC BUS

SIO SCH5514E

FAN CNTL

CPU 1X4 FAN

SYS 1X3 FAN
(For MT)

SYS 1X3 FAN
(For ST/DT)

COM + PS/2 KBMS
REAR HEADER

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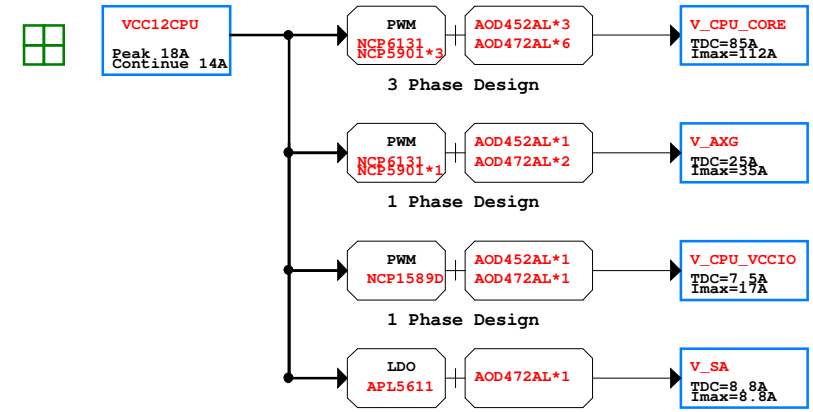
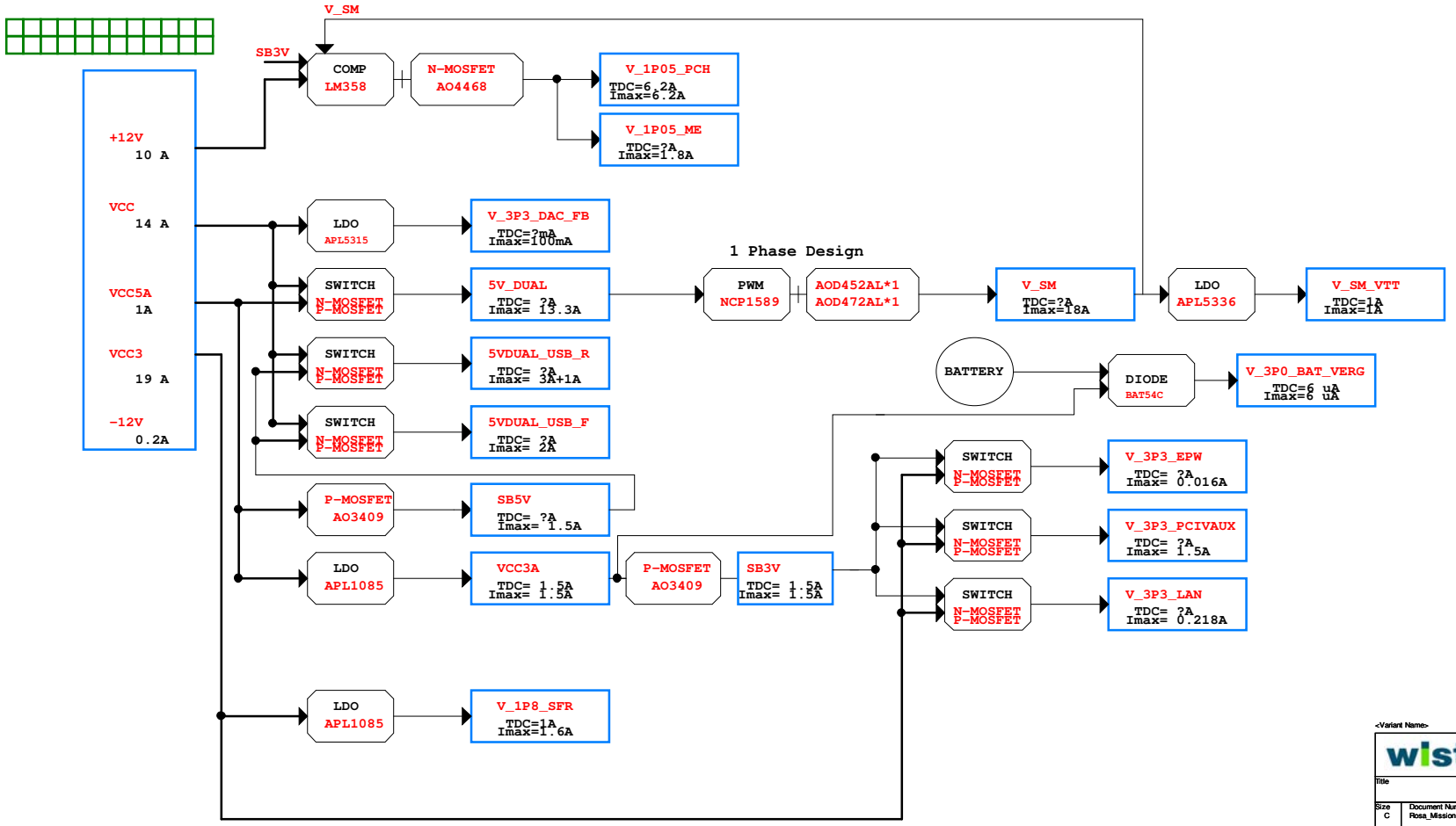
CPU 2X2 POWER CONN



ATX 2X12 POWER CONN



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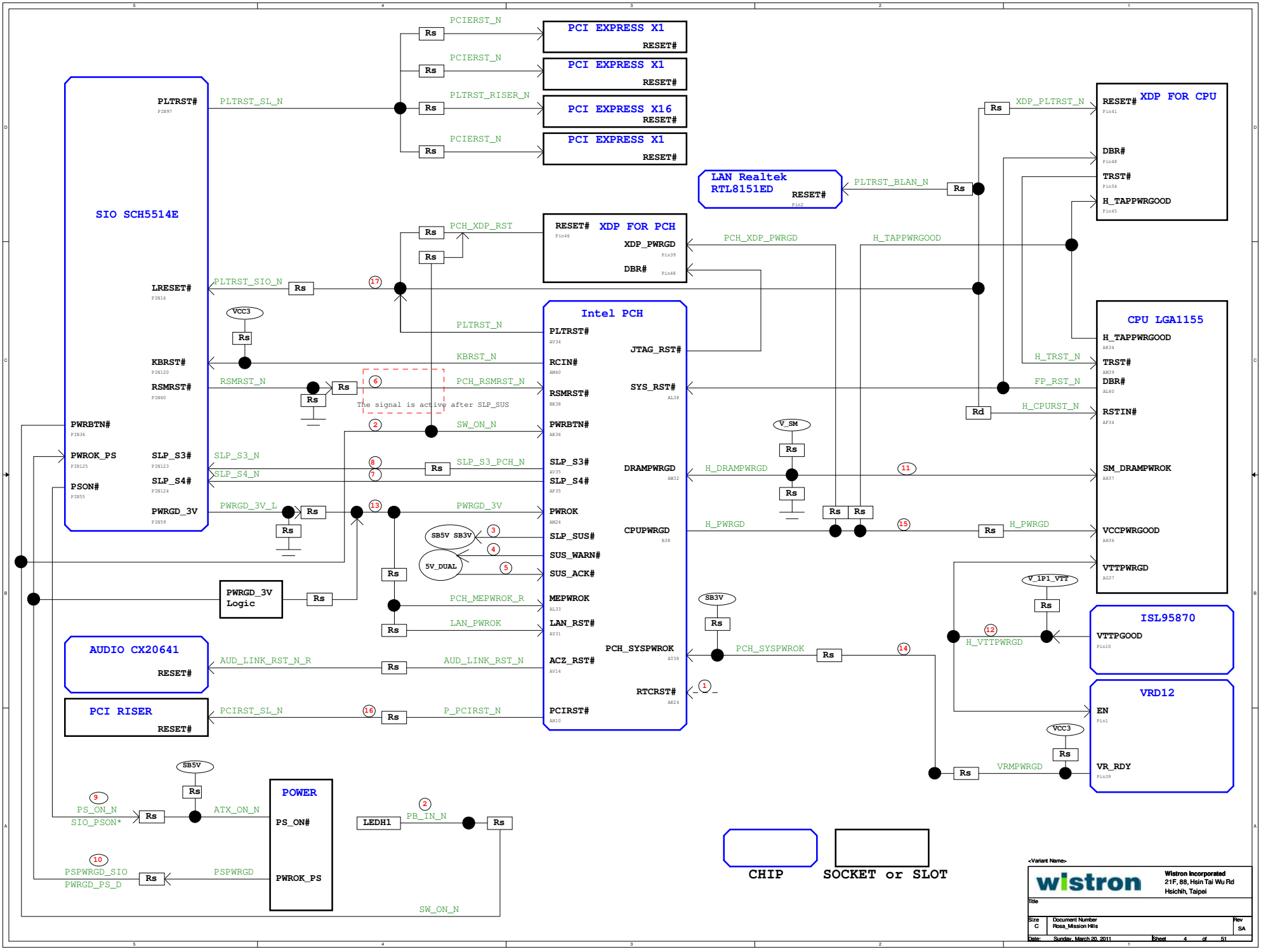

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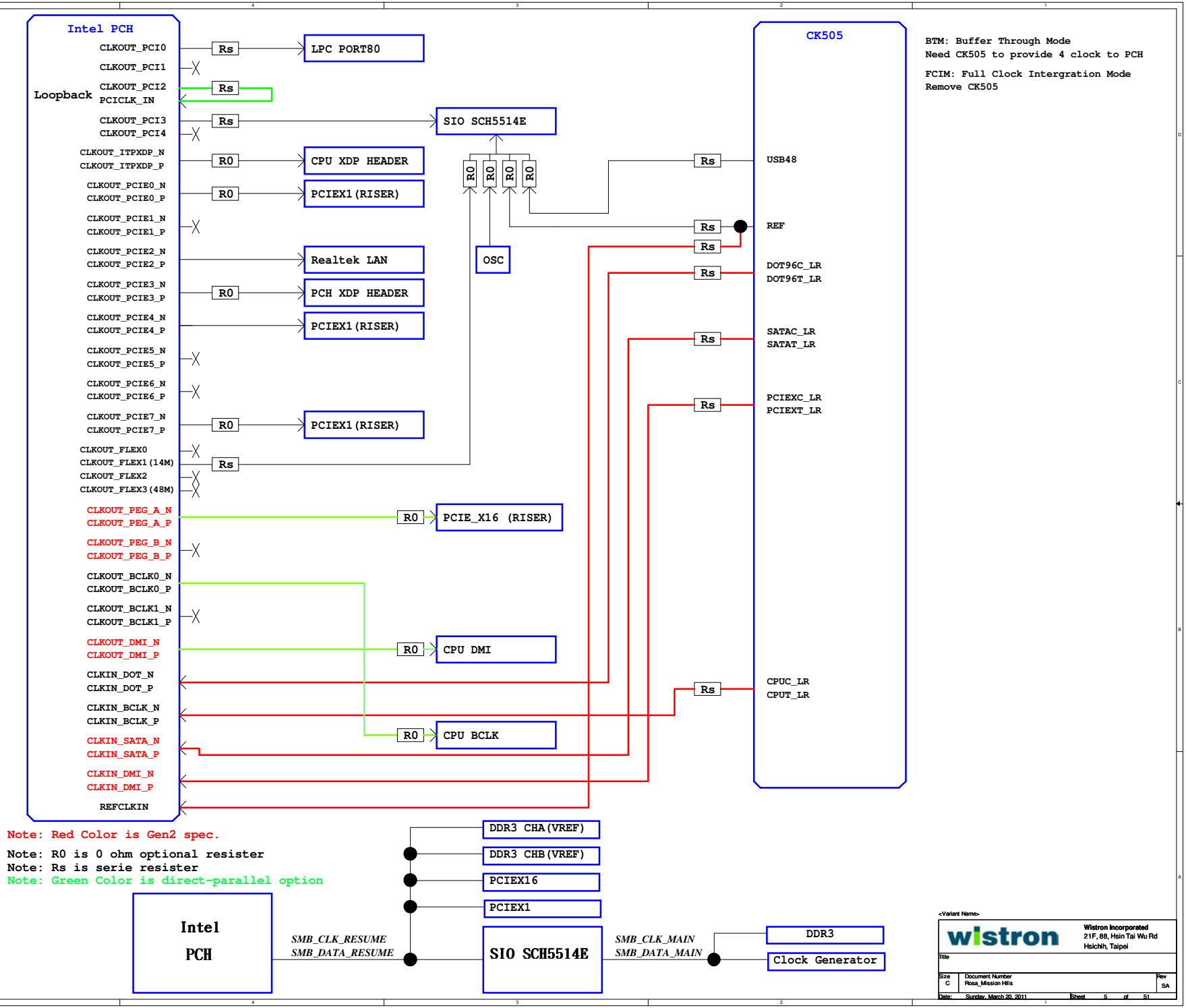

<Variant Name>

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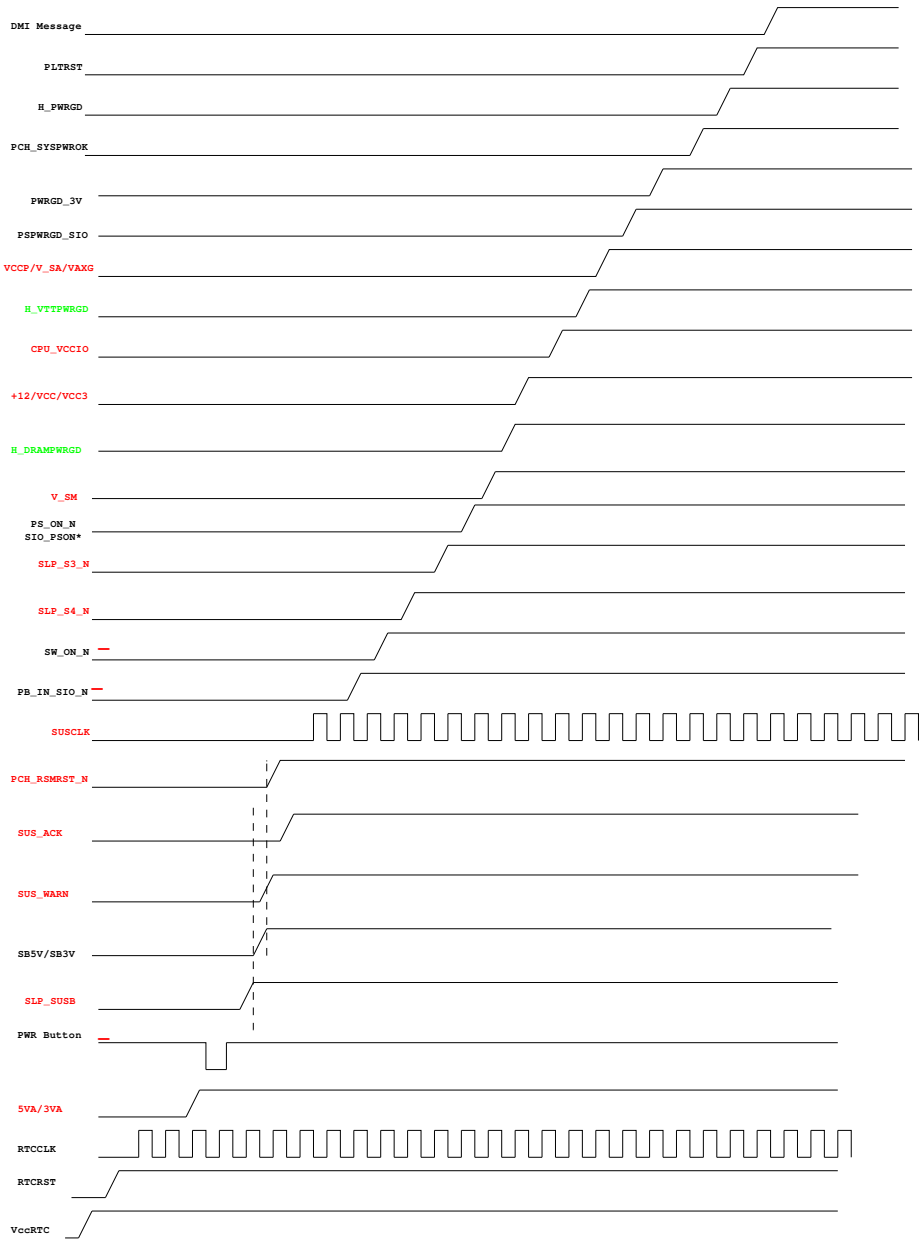
POWER ON SEQUENCE



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D	Ross_Mission Hills	SA

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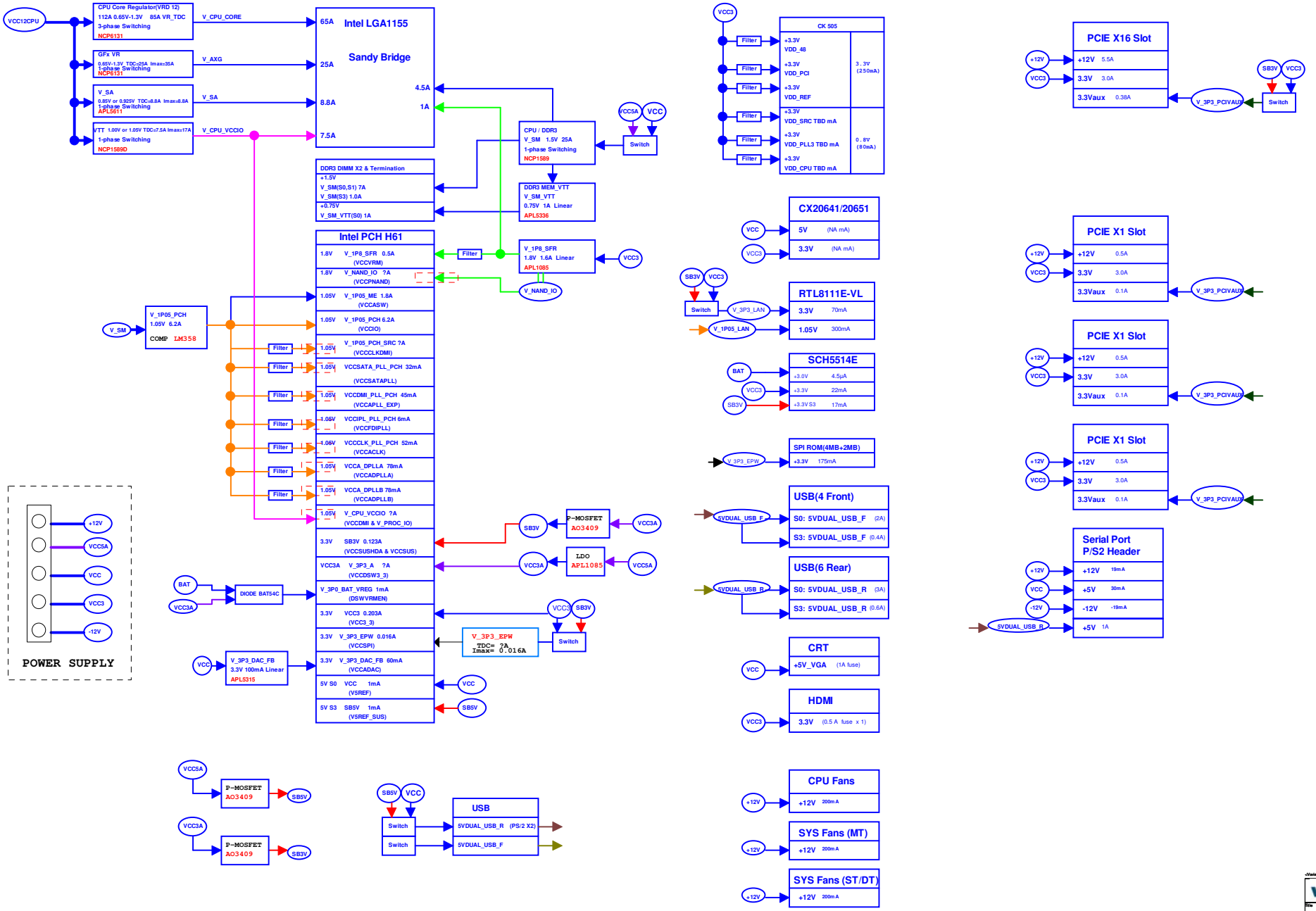

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PCH (H61)

PIN NAME	PIN#	POWER WELL	USAGE	BIOS Post Value	Defult Type	Notes
GPIO0	AW55	MAIN	PECI_REQ_N	GPI (No use)	GPI	10K P/U to VCC3 MAIN
GPIO1	BR19	MAIN	HDMI_DETECT	GPI (Low: NO HDMI, High: HDMI detect)	GPI	I P/U-20K
GPIO2	BN9	MAIN	P_INTE_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO3	AV9	MAIN	P_INTF_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO4	BT15	MAIN	P_INTG_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO5	BR4	MAIN	P_INTH_N	GPI (No Use)	GPI	Unused,8.2K P/U to VCC3 MAIN
GPIO6	BA22	MAIN	TACH2	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN,I P/U-20K
GPIO7	BR16	MAIN	TACH3	GPI (No Use)	GPI	Unused,10K P/U to VCC3 MAIN,I P/U-20K
GPIO8	BP51	RESUME	IO_SMI_N	GPI (IO_SMI_N)	GPO	10K P/U to SB3V
GPIO9	BJ41	RESUME	USB_OC5_R_N	NATIVE	Native	USB OVER CURRENT
GPIO10	BT45	RESUME	USB_OC6_R_N	NATIVE	Native	10K P/U to SB3V
GPIO11	BN49	RESUME	LPC_PME_N	GPI (LPC_PME_N)	Native	LPC_PME_N,10K P/U to SB3V
GPIO12	BK50	RESUME	PCH_HEATSINK_DETECT (Reserved)	GPI (Low: PCH Heatsink detected, High: No PCH Heatsink)	Native	10K P/U to SB3V
GPIO13	BA25	RESUME	PW_CLEAR	GPI (High: Normal, Low: Clear Password)	GPI	10K P/U to SB3V,With a Jumper to GND
GPIO14	BM45	RESUME	USB_OC7_R_N	NATIVE	Native	10K P/U to SB3V
GPIO15	BM55	RESUME	TLS_EN	GPO (Unused)	GPO	I P/D-20K (Strapping)
GPIO16	AU56	MAIN	FB_USBF2_DET	GPI (Low: Front USB detected, High: No Front USB)	GPI	10K P/U to VCC3 MAIN
GPIO17	BT17	MAIN	TACH0	GPI (No use)	GPI	Unused,10K P/U to VCC3 MAIN
GPIO19	AY52	MAIN	SATA1GP	GPO (No use)	GPI	Unused,10K P/U to VCC3 MAIN (Strapping)
GPIO20	AV43	MAIN	BOARD_ID_0	GPI(Reference Board ID Table)	Native	10K P/U to VCC3 MAIN,10K (R) P/D to GND
GPIO21	BC54	MAIN	FB_USBF1_DET	GPI (Low: Card Reader detected, High: No Card Reader)	GPI	FB_USBF1_DET,10K P/U to VCC3 MAIN
GPIO22	BA53	MAIN	BIOS_RCY_GP22	GPI (No use)	GPI	BIOS_RCY_GP22,10K P/U to VCC3 MAIN
GPIO23	BA20	MAIN	LPC_DRQ1_N	GPI (Dell request for test)	Native	Unused, I P/U-20K
GPIO24	BP53	RESUME	H_SKTOCC_R_N	GPI (Low: CPU detected, Floating: No CPU)	GPO	H_SKTOCC_R_N,1K(R) P/U to +3P3V_AUX,10K(R) P/D to GND
GPIO27	BJ43	ep Sleep Power W	PCH_GP27_PU	GPI (Unused)	GPI	10K P/U to V_3P3_A
GPIO28	BJ55	RESUME	PCH_GP28_PU	GPO (Unused)	GPO	10K(R) P/U to V_3P3_A
GPIO29	BH49	RESUME	SLP_LAN_N	GPO (S0/S5 Low, S3 High) S5 Low to turn off LAN power in S5	Native	LAN Enable/Disable
GPIO30	BU46	RESUME	SUS_WARNB	Native	GPI	Function Pin
GPIO31	BG43	ep Sleep Power W	PCH_GP31_PU	GPI (Unused)	GPI	10K P/U to V_3P3_A
GPIO32	BC56	MAIN	EXT_MUTE#	GPO (S0 High, S3/S5 Low) S3/S5 Low to mute all port	GPO	External Mute 10K P/U to VCC3_MAIN
GPIO33	BC25	MAIN	SOP_ENABLE_GP33	Unused (GPO)	GPO	10K(R) P/U to VCC3 MAIN,I P/U-20K
GPIO34	BL56	MAIN	SPK_DETECT	GPI (Low: Speaker detected, High: No Speaker)	GPI	SPK_DETECT,10K P/U to VCC3 MAIN
GPIO35	BJ57	MAIN	SPK_MUTE#	GPO (S0 High, S3/S5 Low) S3/S5 Low to mute external speaker	GPO	SPK_MUTE#,10K P/U to VCC3 MAIN
GPIO36	BB55	MAIN	SATA2GP	GPI (Unused)	GPI	Unused,10K(R) P/U to VCC3 MAIN
GPIO37	BG53	MAIN	SATA3GP	GPI (Unused)	GPI	Unused,10K P/U to VCC3 MAIN
GPIO38	BE54	MAIN	CHASSIS_ID_0	GPI (Pls refer to Chassis ID table)	GPI	CHASSIS_ID_0,10K P/U to VCC3 MAIN
GPIO39	BF55	MAIN	CHASSIS_ID_1	GPI (Pls refer to Chassis ID table)	GPI	CHASSIS_ID_1,10K P/U to VCC3 MAIN
GPIO40	BD41	RESUME	USB_OC1_R_N	Native (OC1#)	Native	USB OVER CURRENT
GPIO41	BG41	RESUME	USB_OC2_R_N	Native (OC2#)	Native	USB OVER CURRENT
GPIO42	BK43	RESUME	USB_OC3_R_N	Native (Unused)	Native	10K P/U to SB3V
GPIO43	BP43	RESUME	USB_OC4_R_N	Native (OC4#)	Native	USB OVER CURRENT
GPIO44	BL54	RESUME	LAN_EN	GPO (High: LAN enable,Low: LAN disable) S0/S3 :High ,S5/DSLP: Low S5/WOL: High	Native	10K P/U to SB3V,10K(R) P/D To GND
GPIO45	AV44	RESUME	1_WATT_CTRL_1	GPO (S0/S5 High, S3 Low) S5 High to turn off PCIAUX 3.3V	Native	1_WATT_CTRL_1,10K P/U to SB3V,10K(R) P/D To GND
GPIO46	BP55	RESUME	INTRU_DET	GPI (Low: Intruder Cable detected, High: No cable)	Native	INTRU_DET,10K P/U to SB3V,1K(R) P/D to GND
GPIO48	AW53	MAIN	MTST_ID	GPI (High: Slim Tower, Low: Mini Tower) (Pls refer to Chassis ID table)	GPI	MTST_ID,10K P/U to VCC3 MAIN
GPIO49	BA56	MAIN	VGA_DET	GPI (High: VGA detected, Low: No VGA)	GPI	VGA_DET,10K P/U to VCC3 MAIN
GPIO50	BT5	MAIN	P_REQ_N1	Native (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO51	AV8	MAIN	P_GNT_N1	Native (Unused)	Native	Strap Pin,1K(R) P/D GND ,I P/U 20K
GPIO52	BK8	MAIN	P_REQ_N2	Native (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO53	BU12	MAIN	P_GNT_N2	Native (Unused)	Native	Strap Pin,1K(R) P/D GND ,I P/U 20K
GPIO54	AV11	MAIN	P_REQ_N3	Native (Unused)	Native	Function Pin,8.2K P/U to VCC3 MAIN
GPIO55	BE2	MAIN	P_GNT_N3	Native (Unused)	Native	Strap Pin,1K(R)P/D GND ,I P/U 20K
GPIO57	BT53	RESUME	ME_CNTL	GPO (High: Enable ME, Low: Disable ME)	GPI	Unused,10K(R) P/U to SB3V,47K P/D GND
GPIO58	BJ46	RESUME	SMLICLK_PCH	Native (Unused)	Native	SMLICLK_PCH,10K P/U to SB3V
GPIO59	BM43	RESUME	USB_OC0_R_N	Native	Native	USB OVER CURRENT
GPIO60	BU49	RESUME	SMLALERT_PCH	Native (Unused)	Native	SMLALERT_PCH,2.2K P/U to SB3V
GPIO61	BN54	RESUME	SUS_STAT_N	Native	Native	W_DISABLE_N,10K P/U (R)to SB3V
GPIO62	BA47	RESUME	SUSCLK	Native	Native	Unused, TP
GPIO63	BH50	RESUME	SLP_S5_N	Native	Native	Unused, TP
GPIO64	AT9	MAIN	Test point(CLKOUTFLEX0)	GPO (Unused)	Native	Unused,I P/D 20K
GPIO65	BA5	MAIN	CK_14M_FLEX	Native (14.318MHz CLK)	Native	14.318MHz CLK for SIO,I P/D 20K
GPIO66	AW5	MAIN	Test point (CLKOUTFLEX2)	GPO (Unused)	Native	Unused,I P/D 20K
GPIO67	BA2	MAIN	BOARD_ID_1	GPI(Reference Board ID Table)	Native	P/D 20K
GPIO68	BU16	MAIN	FP_DETECT (Palm Beach MT/DT Only)	GPI(Low: PWR cable detected, High: No PWR cable)	TBD	10K P/U to VCC3 MAIN
GPIO69	BM18	MAIN	TACH5	Unused	TBD	Unused,10K P/U to VCC3 MAIN
GPIO70	BN17	MAIN	SERIAL_DETECT	GPI (Low: COM Port/KBMS detected, High: No COM/KBMS)	GPI	SERIAL_DETECT,10K P/U to VCC3 MAIN
GPIO71	BP15	MAIN	FP_AUD_DETECT	GPI (Low: Front Audio detected, High: No Front Audio)	GPI	FP_AUD_DETECT,10K P/U to VCC3 MAIN
GPIO72	AV46	RESUME	USB_PWR_CRL1	GPO (S0/S3 High, S5 Low)if board ID is 11 S3 High to turn on USB 5V, S5 Low to turn off USB 5V GPO (S0/S3 Low, S5 High)if board ID is 00 S3 Low to turn on USB 5V, S5 High to turn off USB 5V	GPO	USB_PWR_CRL1,10K P/U to SB3V
GPIO74	BR46	RESUME	SML1ALERT_PCH	Native (Unused)	Native	SML1ALERT_PCH,10K P/U to SB3V
GPIO75	BK46	RESUME	SMLIDATA_PCH	Native (Unused)	Native	SMLIDATA_PCH,10K P/U to SB3V

SCH5514E

GPIO#	Mux Function	GPIO Function	BIOS Post Value		BIOS Default value	BIOS output type	Pull up/down
GP8051_1	DDC_DATA_2P5V	DIAG_LED1	GPO	Unuse, follow original function	GPIO	Open Drain	Pull up to VCC3 on I/O Modul
GP8051_2	DDC_CLK_5V	DIAG_LED2	GPO	Unuse, follow original function	GPIO	Open Drain	Pull up to VCC3 on I/O Modul
GP8051_3	DDC_DATA_5V	DIAG_LED3	GPO	Unuse, follow original function	GPIO	Open Drain	Pull up to VCC3 on I/O Modul
GP8051_4	DDC_CLK_2P5V	DIAG_LED4	GPO	Unuse, follow original function	GPIO	Open Drain	Pull up to VCC3 on I/O Modul
GP8051_5	PWRBTN#	Unuse	Native	follow original function	Native	Push Pull	PCH Internal PH to V_3P3_A
GP8051_6	RI2#	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP8051_7	CTS2#	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP8051_8	DSR2#	SMLIDATA_PCH_SIO	GPO (H)	Unuse,set as "GPO" to prevent floating	GPIO	Push Pull	
GP8051_9	DCD2#	SMLICLK_PCH_SIO	GPO (H)	Unuse,set as "GPO" to prevent floating	GPIO	Push Pull	
GP8051_10	DCD1#	Unuse	Native	follow original function	Native	Input	Pull up to VCC3
GP8051_11	DSR1#	Unuse	Native	follow original function	Native	Input	Pull up to VCC3
GP8051_12	RXD1	Unuse	Native	follow original function	Native	Input	Pull up to VCC3
GP8051_14	TXD1	Unuse	Native	follow original function	Native	Push Pull	Pull up to VCC3
GP8051_15	CTS1#	Unuse	Native	follow original function	Native	Input	
GP8051_16	DTR1#	Unuse	Native	follow original function	Native	Push Pull	Pull up to VCC3
GP8051_17	RI1#	Unuse	Native	follow original function	Native	Input	Pull up to VCC3
GP10	SLP_S3#	Unuse	Native	follow original function	Native	Push Pull	
GP11	SLP_S5#	Unuse	Native	follow original function	Native	Push Pull	
GP14	HD_LED#	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP21	P16/DS1#	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP22	P12/MRT1#/SCS1#	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP23	LATCHED_BF_CUT	Unuse	Native	follow original function	Native	Push Pull	
GP25	SCLK	Unuse	Native	follow original function	Native	Open Drain	Pull up to VCC3
GP26	SCLK_1	Unuse	Native	follow original function	Native	Open Drain	Pull up to SB3V
GP31	SECONDARY_HD#	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP33	PRIMARY_HD#	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP35	SDAT/LED1	Unuse	Native	follow original function	Native	Open Drain	Pull up to VCC3
GP36	KBDRST#	Unuse	Native	follow original function	Native	Open Drain	Pull up to VCC3
GP37	A20GATE	Unuse	Native	follow original function	Native	Open Drain	Pull up to VCC3
GP40	DRVDEN0	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP41	IO_PME#	Unuse	Native	follow original function	GPIO	Open Drain	Pull up to SB3V
GP42	SDAT_1/IO_SMI#	Unuse	Native	follow original function	Native	Open Drain	Pull up to SB3V
GP52	RXD2	SLOTOCC_N	Native	reserve, follow original function	GPIO	Push Pull	
GP53	TXD2	COPEN_N	Native	reserve, follow original function	GPIO	Push Pull	
GP55	RTS2#/DDRC	CPURST_IN	Native	reserve, follow original function	GPIO	Push Pull	
GP57	DTR2#	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP60	YELLOW	Unuse	Native	follow Power LED behavior function S0/S1: High S3: Low S4/S5: High boot failure(No-Post): Low boot failure(Post):Blinking	Native	Open Drain	Pull up to SB3V
GP61	GREEN	Unuse	Native	follow Power LED behavior function S0/S1: Low S3: High S4/S5: High boot failure(No-Post): High boot failure(Post): High	Native	Open Drain	Pull up to SB3V
GP75	DE_RSTDRV#	IO_SMI_N	GPO (IO_SMI)	set as "GPO" for SMI function	Native	Open Drain	Pull up to SB3V
GP76	PCI_RST_SYS#	Unuse	Native	follow original function	Native	Push Pull	
GP77	PCI_RST_SLOTS#	Unuse	Native	follow original function	Native	Push Pull	
GP80	PS_ON#	Unuse	Native	follow original function	Native	Open Drain	Pull up to V_5P0_A
GP81	BACKFEED_CUT#	Unuse	Native	follow original function	Native	Open Drain	Pull up to SB5V
GP82	None	Unuse	GPO (H)	set as "GPO" to prevent floating	GPIO	Push Pull	
GP83	PWR_GOOD_3V	Unuse	Native	follow original function	Native	Push Pull	
GP84	RSMRST#	Unuse	Native	follow original function	Native	Push Pull	

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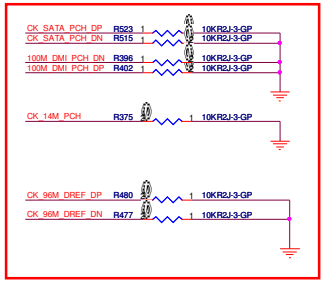
PCH Buffer CLOCK

22 CK_96M_DREF_DP
22 CK_96M_DREF_DN
21 CK_SATA_PCH_DP
21 CK_SATA_PCH_DN
22 100M_DMI_PCH_DP
22 100M_DMI_PCH_DN

14M CLOCK

20 CK_14M_PCH



Terminate PCH CLK Inputs

Remove CLK GEN
Use PCH Internal CLK

<Variant Name>

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CLOCK
20 CK_PE_100M_MCP_DP
20 CK_PE_100M_MCP_DN

CPU_SA
49 VCCSA_VID
49 VCCSA_SENSE

CPU_VTT
49 VCCIO_SEL
49 VCCTT_SENSE
49 VSSTT_SENSE

CPU_AXG
50 VCCAXG_SENSE
50 VSSAXG_SENSE

CPU_VCORE
50 VCC_SENSE
50 VSS_SENSE
50 H_VIDSCK_VR
50 H_VIDSOUT_VR
50 H_VIDALERT_N_VR

ITP
14 H_TDO
14 H_TDI
14 H_TCK
14 H_TMS
14 H_TRST_N
14 H_PRDY_N
14 H_PREQ_N
14 XDP_DBRESET_N
14 CK_XDP_S_DN
14 CK_XDP_S_DP
14 H_BPM#0
14 H_BPM#1
14 H_BPM#2
14 H_BPM#3
14 H_BPM#4
14 H_BPM#5
14 H_BPM#6
14 H_BPM#7
14,36 H_CPURST_N

OTHER
14,19,36 PLTRST_N
14,19 H_PWRGD
19 FP_RST_DBR_N
19,46 H_DRAMPWRGD
21,36 H_PECI
36,50 H_PROCHOT_N
21 H_THERMTRIP_N
21 H_PM_SYNC_0
19,36 H_SKTOCC_N
14,36 H_CPURST_N
23 H_SNB_N
19,26,32,36,41 SMB_CLK_RESUME
19,26,32,36,41 SMB_DATA_RESUME
14 TPEV_SNB_PCUDEBUG_0
03/21:follow CRB1.0 rout the CFG[0] to XDP !

MINIMIZE STUB BETWEEN THESE AND RESISTORS AT SINK PAGE
PLACE IN CRB AREA
H_VIDSCK_VR R355 0R0402-PAD-2-GP H_VIDSCK
H_VIDSOUT_VR R350 0R0402-PAD-2-GP H_VIDSOUT
H_VIDALERT_N_VR R329 0R0402-PAD-2-GP H_VIDALERT_N

Defensive Design

V_CPU_VCCIO
R335 75R2F-2-GP
R353 110R2F-GP
R351 (R) 90D9R2F-1-GP

PLTRST_N
R349 1K3R2F-1-GP (R)
R365 665R2F-2-GP (R)
C567 SCD1U16V2ZY-2GP 2010/12/20 Add EMI Cap
R330 43R2J-GP
SB3V
R341 100KR2J-1-GP
R339 75R2J-1-GP
PLTRST_CPU_N2
PLTRST_CPU_N1
(84.27002.E3F) 2N7002DW-1-GP U25
PLTRST_N 1 R336 2 PLTRST_CPU_N 0R0402-PAD-2-GP
(R) C301 SC100P50V2JN-3GP
C472 SCD1U16V2ZY-2GP 2010/12/20 Add EMI Cap

V_SM
R494 1 200R2F-L-GP H_DRAMPWRGD

V_CPU_VCCIO
R372 1 (R) 1KR2J-1-GP H_PECI
R342 1 (R) 1KR2J-1-GP H_CATERR_N
R338 1 51R2J-2-GP H_PROCHOT_R_N
R334 1 (R) 51R2J-2-GP CPU_THERMTRIP_N
R348 1 51R2J-2-GP H_PWRGD
R352 1 1KR2J-1-GP
C460 SCD1U16V2ZY-2GP
C449 SCD1U16V2ZY-2GP 2010/12/20 Add EMI Cap

SB3V
R606 1 (R) 220R5J-GP FP_RST_DBR_N
H_PROCHOT_N R343 1 0R0402-PAD-2-GP H_PROCHOT_R_N
H_THERMTRIP_N R333 1 0R0402-PAD-2-GP CPU_THERMTRIP_N

H_VIDSCK
H_VIDSOUT
H_VIDALERT_N
R322 2 100R2F-2-GP (R)
R323 1 44D2R2F-GP H_VIDALERT_N_1
H_DRAMPWRGD R491 2 120R2F-GP
H_PWRGD
H_DRAMPWRGD_CPU
H_CPURST_N
H_PM_SYNC_0
H_PECI
H_CATERR_N
H_PROCHOT_R_N
CPU_THERMTRIP_N
H_SKTOCC_N
H_SNB_N
SNB_DDR_VREF

03/21:follow CRB1.0 rout the CFG[0] to XDP !
TPEV_SNB_PCUDEBUG_0
TPAD28 TP88 1 TPEV_SNB_PCUDEBUG_1 H36
TPAD28 TP89 1 TPEV_SNB_PCUDEBUG_2 J36
R381 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_3 J37
TPAD28 TP90 1 TPEV_SNB_PCUDEBUG_4 K36
TPAD28 TP91 1 TPEV_SNB_PCUDEBUG_5 L36
R383 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_6 N35
R415 1 (R) 1KR2J-1-GP TPEV_SNB_PCUDEBUG_7 L37
TPAD28 TP92 1 TPEV_SNB_PCUDEBUG_8 M36
TPAD28 TP93 1 TPEV_SNB_PCUDEBUG_9 R8
TPAD28 TP94 1 TPEV_SNB_PCUDEBUG_10 L35
TPAD28 TP95 1 TPEV_SNB_PCUDEBUG_11 M38
TPAD28 TP96 1 TPEV_SNB_PCUDEBUG_12 N36
TPAD28 TP97 1 TPEV_SNB_PCUDEBUG_13 N38
TPAD28 TP98 1 TPEV_SNB_PCUDEBUG_14 N39
TPAD28 TP99 1 TPEV_SNB_PCUDEBUG_15 N37
TPAD28 TP100 1 TPEV_SNB_PCUSTB_0 N40
TPAD28 TP101 1 TPEV_SNB_PCUSTB_1 G37
TPAD28 TP102 1 G36

PEG CONFIG TABLE Default is X16

CFG	H	L	DESCRIPTION
0	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED
2	NORM	RESERVE	PEG REVERSAL[0]
3,4,7-17	RESERVED	RESERVED	RESERVED

CFG5/SEL0	CFG6/SEL1	PCIE CONFIG
1	1	1 X 16
0	1	1 X 8

* NOA[6:5] 11:DEFAULT X16; 10:2X8; 01:RESERVED; 00:X8,X4,X4 *

U27E 5 OF 11
BCLK_0 W2
BCLK#_0 W1
VIDSCLK C37
VIDSOUT B37
VIDALERT# A37
UNCOREPWRGOOD J40
SM_DRAMPWROK A19
RESET# F36
PM_SYNC J38
PECI B35
CATERR# E37
PROCHOT# H34
THERMTRIP# G35
SKTOCC# A33
PROC_SEL K32
SM_VREF A22
CFG_0 H36
CFG_1 J36
CFG_2 J37
CFG_3 K36
CFG_4 L36
CFG_5 N35
CFG_6 L37
CFG_7 M36
CFG_8 R8
CFG_9 L35
CFG_10 M38
CFG_11 N36
CFG_12 N38
CFG_13 N39
CFG_14 N37
CFG_15 N40
CFG_16 G37
CFG_17 G36
RSVD#AT14 AT14
RSVD#AY3 AY3
RSVD#H7 H7
RSVD#H8 H8
VCCP_SELECT P33
VCCSA_VID P34
VCCSA_SENSE T2
VCC_SENSE A36
VSS_SENSE B36
VCCIO_SENSE AB4
VSSIO_SENSE AB3
VCCAXG_SENSE L32
VSSAXG_SENSE M32
TDO L39
TDI L40
TCK M40
TMS L38
TRST# J39
PRDY# K38
PREQ# K40
DBR# E39
RSVD#C40 C40
RSVD#D40 D40
BPM#_0 H40
BPM#_1 H38
BPM#_2 G38
BPM#_3 G40
BPM#_4 G39
BPM#_5 F38
BPM#_6 E40
BPM#_7 F40
RSVD#B39 B39
RSVD#J33 J33
RSVD#L34 L34
RSVD#L33 L33
RSVD#K34 K34
RSVD#N33 N33
RSVD#M34 M34
RSVD#AV1 AV1
RSVD#AW2 AW2
RSVD#L9 L9
RSVD#J9 J9
RSVD#K9 K9
RSVD#L31 L31
RSVD#J31 J31
RSVD#K31 K31
RSVD#AD34 AD34
RSVD#AD35 AD35
ITP_CLKINP C39
ITP_CLKINN D39
SAN-1U2NF (62.10055.441)

VCC
R429 10KR2J-3-GP
R421 4K7R2J-2-GP

12/23 JACK
XDP_DBRESET_N
R427 1 0R0402-PAD-2-GP FP_RST_DBR_N
R430 1 (R) 0R2J-2-GP CK_XDP_S_DP
R432 1 (R) 0R2J-2-GP CK_XDP_S_DN

V_SM
R500 100R2F-L1-GP-U
SNB_DDR_VREF
R493 100R2F-L1-GP-U
C406 SCD1U16V2ZY-2GP

Remove Potentiometer

<Variant Name>

wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title

Size	Document Number	Rev
C	Rosa_Mission Hills	SA

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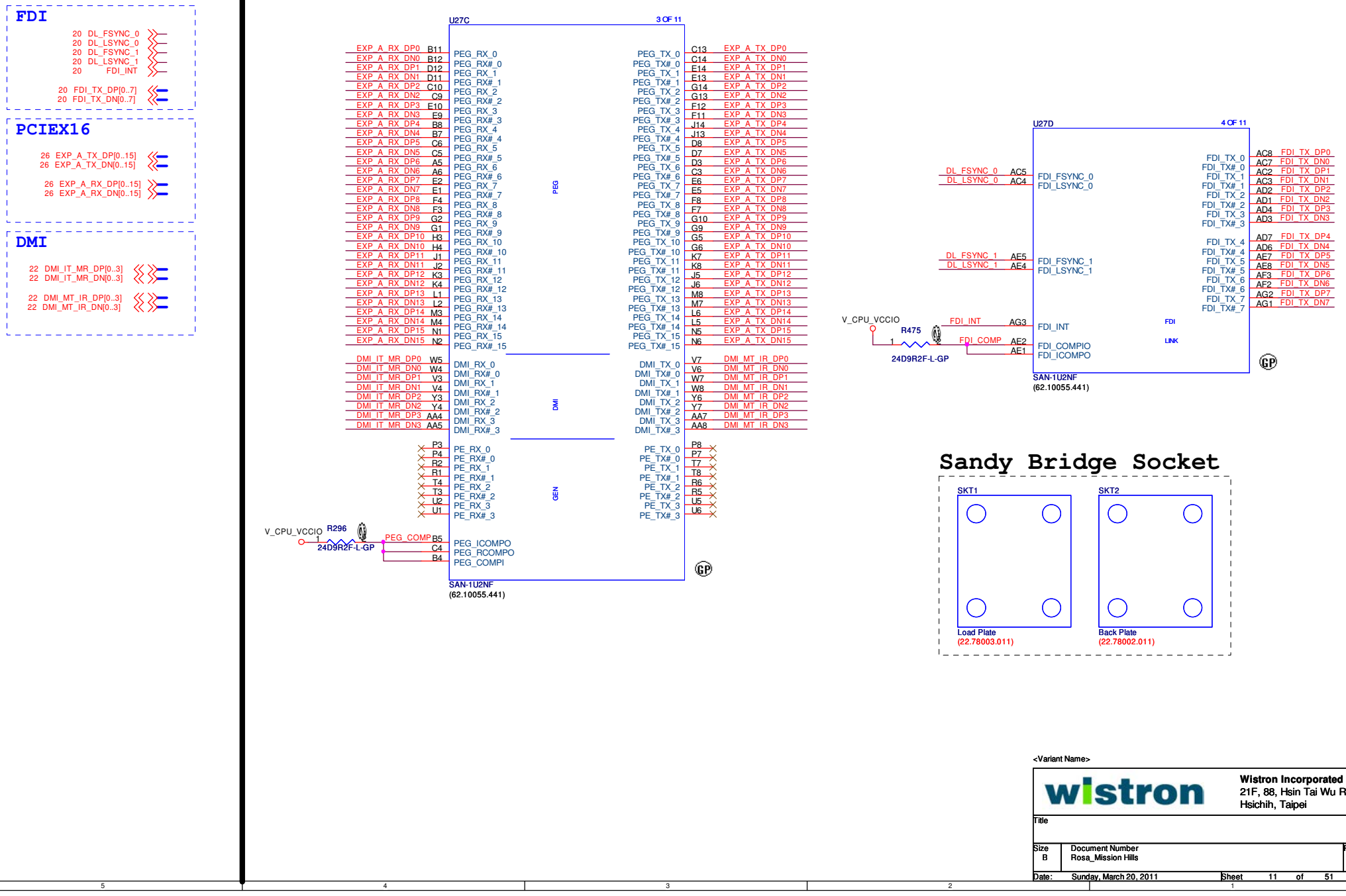
FDI
20 DL_FSYNC_0
20 DL_LSYNC_0
20 DL_FSYNC_1
20 DL_LSYNC_1
20 FDI_INT
20 FDI_TX_DP[0..7]
20 FDI_TX_DN[0..7]
PCIEX16
26 EXP_A_TX_DP[0..15]
26 EXP_A_TX_DN[0..15]
26 EXP_A_RX_DP[0..15]
26 EXP_A_RX_DN[0..15]
DMI
22 DMI_IT_MR_DP[0..3]
22 DMI_IT_MR_DN[0..3]
22 DMI_MT_IR_DP[0..3]
22 DMI_MT_IR_DN[0..3]
U27C
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PEG
DMI
GEN
SAN-1U2NF
(62.10055.441)
V_CPU_VCCIO
R296
24D9R2F-L-GP
PEG_COMP
PEG_ICOMPO
PEG_RCOMPO
PEG_COMPI
U27D
4 OF 11
FDI
LINK
R475
FDI_COMPIO
FDI_ICOMPO
Sandy Bridge Socket
SKT1
SKT2
Load Plate
(22.78003.011)
Back Plate
(22.78002.011)
<Variant Name>
wistron
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei
Title
Size
B
Document Number
Rosa_Mission Hills
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SA
Date:
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DDR DATA

15 M_DATA_A[0..63]
17 M_DATA_B[0..63]

15 M_DQS_A_DP[0..8]
15 M_DQS_A_DN[0..8]

17 M_DQS_B_DP[0..8]
17 M_DQS_B_DN[0..8]

15 M_DATA_A_CB[0..7]
17 M_DATA_B_CB[0..7]

DDR CMD/ADD

15 M_MAA_A[0..15]
17 M_MAA_B[0..15]

15 M_WE_A_N
15 M_CAS_A_N
15 M_RAS_A_N
15 M_SBS_A0
15 M_SBS_A1
15 M_SBS_A2

17 M_WE_B_N
17 M_CAS_B_N
17 M_RAS_B_N
17 M_SBS_B0
17 M_SBS_B1
17 M_SBS_B2

DDR CTRL

15 M_SCS_A_N0
15 M_SCS_A_N1
15 M_SCKE_A0
15 M_SCKE_A1
15 M_ODT_A0
15 M_ODT_A1

17 M_SCS_B_N0
17 M_SCS_B_N1
17 M_SCKE_B0
17 M_SCKE_B1
17 M_ODT_B0
17 M_ODT_B1

DDR CLOCK

15 CK_M_DDR0_A_DP
15 CK_M_DDR0_A_DN
15 CK_M_DDR1_A_DP
15 CK_M_DDR1_A_DN

17 CK_M_DDR0_B_DP
17 CK_M_DDR0_B_DN
17 CK_M_DDR1_B_DP
17 CK_M_DDR1_B_DN

DDR OTHERS

15,17 DDR3_DRAMRST_N

U27A — 1 OF 11

M_MAA_A0	AV27	SA_MA_0	SA_DQ_0	AJ3	M_DATA_A0
M_MAA_A1	AY24	SA_MA_1	SA_DQ_1	AJ4	M_DATA_A1
M_MAA_A2	AW24	SA_MA_2	SA_DQ_2	AL3	M_DATA_A2
M_MAA_A3	AW23	SA_MA_3	SA_DQ_3	AL4	M_DATA_A3
M_MAA_A4	AY23	SA_MA_4	SA_DQ_4	AJ2	M_DATA_A4
M_MAA_A5	AT24	SA_MA_5	SA_DQ_5	AJ1	M_DATA_A5
M_MAA_A6	AT23	SA_MA_6	SA_DQ_6	AL2	M_DATA_A6
M_MAA_A7	AU22	SA_MA_7	SA_DQ_7	AL1	M_DATA_A7
M_MAA_A8	AV22	SA_MA_8	SA_DQ_8	AN1	M_DATA_A8
M_MAA_A9	AT22	SA_MA_9	SA_DQ_9	AN4	M_DATA_A9
M_MAA_A10	AY28	SA_MA_10	SA_DQ_10	AR3	M_DATA_A10
M_MAA_A11	AU21	SA_MA_11	SA_DQ_11	AR4	M_DATA_A11
M_MAA_A12	AT21	SA_MA_12	SA_DQ_12	AN2	M_DATA_A12
M_MAA_A13	AW22	SA_MA_13	SA_DQ_13	AN3	M_DATA_A13
M_MAA_A14	AU20	SA_MA_14	SA_DQ_14	AR2	M_DATA_A14
M_MAA_A15	AT20	SA_MA_15	SA_DQ_15	AR1	M_DATA_A15
			SA_DQ_16	AV2	M_DATA_A16
M_WE_A_N	AW29	SA_WE#	SA_DQ_17	AW3	M_DATA_A17
M_CAS_A_N	AV30	SA_CAS#	SA_DQ_18	AV5	M_DATA_A18
M_RAS_A_N	AU28	SA_RAS#	SA_DQ_19	AW5	M_DATA_A19
			SA_DQ_20	AU2	M_DATA_A20
M_SBS_A0	AY29	SA_BS_0	SA_DQ_21	AU3	M_DATA_A21
M_SBS_A1	AW28	SA_BS_1	SA_DQ_22	AU5	M_DATA_A22
M_SBS_A2	AV20	SA_BS_2	SA_DQ_23	AY5	M_DATA_A23
			SA_DQ_24	AY7	M_DATA_A24
M_SCS_A_N0	AU29	SA_CS#_0	SA_DQ_25	AU7	M_DATA_A25
M_SCS_A_N1	AV32	SA_CS#_1	SA_DQ_26	AV9	M_DATA_A26
	AW30	SA_CS#_2	SA_DQ_27	AU9	M_DATA_A27
	AU33	SA_CS#_3	SA_DQ_28	AV7	M_DATA_A28
			SA_DQ_29	AW7	M_DATA_A29
M_SCKE_A0	AV19	SA_CKE_0	SA_DQ_30	AW9	M_DATA_A30
M_SCKE_A1	AT19	SA_CKE_1	SA_DQ_31	AY9	M_DATA_A31
	AU18	SA_CKE_2	SA_DQ_32	AU35	M_DATA_A32
	AV18	SA_CKE_3	SA_DQ_33	AW37	M_DATA_A33
			SA_DQ_34	AU39	M_DATA_A34
M_ODT_A0	AV31	SA_ODT_0	SA_DQ_35	AU36	M_DATA_A35
M_ODT_A1	AU32	SA_ODT_1	SA_DQ_36	AW35	M_DATA_A36
	AU30	SA_ODT_2	SA_DQ_37	AY36	M_DATA_A37
	AW33	SA_ODT_3	SA_DQ_38	AU38	M_DATA_A38
			SA_DQ_39	AU37	M_DATA_A39
			SA_DQ_40	AR40	M_DATA_A40
			SA_DQ_41	AR37	M_DATA_A41
			SA_DQ_42	AN38	M_DATA_A42
			SA_DQ_43	AN37	M_DATA_A43
CK_M_DDR0_A_DP	AY25	SA_CK_0	SA_DQ_44	AR39	M_DATA_A44
CK_M_DDR0_A_DN	AW25	SA_CK#_0	SA_DQ_45	AR38	M_DATA_A45
CK_M_DDR1_A_DP	AU24	SA_CK_1	SA_DQ_46	AN39	M_DATA_A46
CK_M_DDR1_A_DN	AU25	SA_CK#_1	SA_DQ_47	AN40	M_DATA_A47
	AW27	SA_CK_2	SA_DQ_48	AL40	M_DATA_A48
	AY27	SA_CK#_2	SA_DQ_49	AL37	M_DATA_A49
	AY26	SA_CK_3	SA_DQ_50	AJ38	M_DATA_A50
	AW26	SA_CK#_3	SA_DQ_51	AJ37	M_DATA_A51
			SA_DQ_52	AL39	M_DATA_A52
			SA_DQ_53	AL38	M_DATA_A53
			SA_DQ_54	AJ39	M_DATA_A54
			SA_DQ_55	AJ40	M_DATA_A55
			SA_DQ_56	AG40	M_DATA_A56
			SA_DQ_57	AG37	M_DATA_A57
			SA_DQ_58	AE38	M_DATA_A58
			SA_DQ_59	AE37	M_DATA_A59
			SA_DQ_60	AG39	M_DATA_A60
			SA_DQ_61	AG38	M_DATA_A61
			SA_DQ_62	AE39	M_DATA_A62
			SA_DQ_63	AE40	M_DATA_A63
DDR3_DRAMRST_N	AW18	SM_DRAMRST#			
M_DQS_A_DP8	AV13	SA_DQS_8	SA_DQS_0	AK3	M_DQS_A_DP0
M_DQS_A_DN8	AV12	SA_DQS#_8	SA_DQS_1	AP3	M_DQS_A_DP1
			SA_DQS_2	AW4	M_DQS_A_DP2
M_DATA_A_CB0	AU12	SA_ECC_CB_0	SA_DQS_3	AV8	M_DQS_A_DP3
M_DATA_A_CB1	AU14	SA_ECC_CB_1	SA_DQS_4	AV37	M_DQS_A_DP4
M_DATA_A_CB2	AW13	SA_ECC_CB_2	SA_DQS_5	AP38	M_DQS_A_DP5
M_DATA_A_CB3	AY13	SA_ECC_CB_3	SA_DQS_6	AK38	M_DQS_A_DP6
M_DATA_A_CB4	AU13	SA_ECC_CB_4	SA_DQS_7	AF38	M_DQS_A_DP7
M_DATA_A_CB5	AU11	SA_ECC_CB_5			
M_DATA_A_CB6	AY12	SA_ECC_CB_6	SA_DQS#_0	AK2	M_DQS_A_DN0
M_DATA_A_CB7	AW12	SA_ECC_CB_7	SA_DQS#_1	AP2	M_DQS_A_DN1
			SA_DQS#_2	AV4	M_DQS_A_DN2
			SA_DQS#_3	AW8	M_DQS_A_DN3
			SA_DQS#_4	AV36	M_DQS_A_DN4
			SA_DQS#_5	AP39	M_DQS_A_DN5
			SA_DQS#_6	AK39	M_DQS_A_DN6
			SA_DQS#_7	AF39	M_DQS_A_DN7

DDR3_DRAMRST_N — 1 — R637 — 2 — DDR3_DRAMRST_N-1
0R0402-PAD-2-GP

(R) C474
SCD1U10V2KX-4GP

Can be left as no connects if no support ECC.

DDR_0

SAN-1U2NF
(62.10055.441)

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M_MAA_B0	AK24	SB_MA_0	SB_DQ_0	AG7	M_DATA_B0
M_MAA_B1	AM20	SB_MA_1	SB_DQ_1	AG8	M_DATA_B1
M_MAA_B2	AM19	SB_MA_2	SB_DQ_2	AJ9	M_DATA_B2
M_MAA_B3	AK18	SB_MA_3	SB_DQ_3	AJ8	M_DATA_B3
M_MAA_B4	AP19	SB_MA_4	SB_DQ_4	AG5	M_DATA_B4
M_MAA_B5	AP18	SB_MA_5	SB_DQ_5	AG6	M_DATA_B5
M_MAA_B6	AM18	SB_MA_6	SB_DQ_6	AJ6	M_DATA_B6
M_MAA_B7	AL18	SB_MA_7	SB_DQ_7	AJ7	M_DATA_B7
M_MAA_B8	AN18	SB_MA_8	SB_DQ_8	AL7	M_DATA_B8
M_MAA_B9	AY17	SB_MA_9	SB_DQ_9	AM7	M_DATA_B9
M_MAA_B10	AN23	SB_MA_10	SB_DQ_10	AM10	M_DATA_B10
M_MAA_B11	AU17	SB_MA_11	SB_DQ_11	AL10	M_DATA_B11
M_MAA_B12	AT18	SB_MA_12	SB_DQ_12	AL6	M_DATA_B12
M_MAA_B13	AP26	SB_MA_13	SB_DQ_13	AM6	M_DATA_B13
M_MAA_B14	AY16	SB_MA_14	SB_DQ_14	AL9	M_DATA_B14
M_MAA_B15	AV16	SB_MA_15	SB_DQ_15	AM9	M_DATA_B15
			SB_DQ_16	AP7	M_DATA_B16
M_WE_B_N	AR25	SB_WE#	SB_DQ_17	AR7	M_DATA_B17
M_CAS_B_N	AK25	SB_CAS#	SB_DQ_18	AP10	M_DATA_B18
M_RAS_B_N	AP24	SB_RAS#	SB_DQ_19	AR10	M_DATA_B19
			SB_DQ_20	AP6	M_DATA_B20
M_SBS_B0	AP23	SB_BS_0	SB_DQ_21	AR6	M_DATA_B21
M_SBS_B1	AM24	SB_BS_1	SB_DQ_22	AP9	M_DATA_B22
M_SBS_B2	AW17	SB_BS_2	SB_DQ_23	AR9	M_DATA_B23
			SB_DQ_24	AM12	M_DATA_B24
M_SCS_B_N0	AN25	SB_CS#_0	SB_DQ_25	AM13	M_DATA_B25
M_SCS_B_N1	AN26	SB_CS#_1	SB_DQ_26	AR13	M_DATA_B26
	AL25	SB_CS#_2	SB_DQ_27	AP13	M_DATA_B27
	AT26	SB_CS#_3	SB_DQ_28	AL12	M_DATA_B28
			SB_DQ_29	AL13	M_DATA_B29
M_SCKE_B0	AU16	SB_CKE_0	SB_DQ_30	AR12	M_DATA_B30
M_SCKE_B1	AY15	SB_CKE_1	SB_DQ_31	AP12	M_DATA_B31
	AW15	SB_CKE_2	SB_DQ_32	AR28	M_DATA_B32
	AY15	SB_CKE_3	SB_DQ_33	AR29	M_DATA_B33
			SB_DQ_34	AL28	M_DATA_B34
M_ODT_B0	AL26	SB_ODT_0	SB_DQ_35	AL29	M_DATA_B35
M_ODT_B1	AP26	SB_ODT_1	SB_DQ_36	AP28	M_DATA_B36
	AM26	SB_ODT_2	SB_DQ_37	AP29	M_DATA_B37
	AK26	SB_ODT_3	SB_DQ_38	AM28	M_DATA_B38
			SB_DQ_39	AM29	M_DATA_B39
			SB_DQ_40	AP32	M_DATA_B40
			SB_DQ_41	AP31	M_DATA_B41
			SB_DQ_42	AP35	M_DATA_B42
			SB_DQ_43	AP34	M_DATA_B43
CK_M_DDR0_B_DP	AL21	SB_CK_0	SB_DQ_44	AR32	M_DATA_B44
CK_M_DDR0_B_DN	AL22	SB_CK#_0	SB_DQ_45	AR31	M_DATA_B45
CK_M_DDR1_B_DP	AL20	SB_CK_1	SB_DQ_46	AR35	M_DATA_B46
CK_M_DDR1_B_DN	AK20	SB_CK#_1	SB_DQ_47	AR34	M_DATA_B47
	AL23	SB_CK_2	SB_DQ_48	AM32	M_DATA_B48
	AM22	SB_CK#_2	SB_DQ_49	AM31	M_DATA_B49
	AP21	SB_CK_3	SB_DQ_50	AL35	M_DATA_B50
	AN21	SB_CK#_3	SB_DQ_51	AL32	M_DATA_B51
			SB_DQ_52	AM34	M_DATA_B52
			SB_DQ_53	AL31	M_DATA_B53
			SB_DQ_54	AM35	M_DATA_B54
			SB_DQ_55	AL34	M_DATA_B55
			SB_DQ_56	AR35	M_DATA_B56
			SB_DQ_57	AR34	M_DATA_B57
			SB_DQ_58	AE34	M_DATA_B58
			SB_DQ_59	AE35	M_DATA_B59
			SB_DQ_60	AJ35	M_DATA_B60
			SB_DQ_61	AJ34	M_DATA_B61
			SB_DQ_62	AF33	M_DATA_B62
			SB_DQ_63	AF35	M_DATA_B63
M_DQS_B_DP8	AN16	SB_DQS_8	SB_DQS_0	AH7	M_DQS_B_DP0
M_DQS_B_DN8	AN15	SB_DQS#_8	SB_DQS_1	AM8	M_DQS_B_DP1
			SB_DQS_2	AR8	M_DQS_B_DP2
M_DATA_B_CB0	AL16	SB_ECC_CB_0	SB_DQS_3	AN13	M_DQS_B_DP3
M_DATA_B_CB1	AM16	SB_ECC_CB_1	SB_DQS_4	AN29	M_DQS_B_DP4
M_DATA_B_CB2	AP16	SB_ECC_CB_2	SB_DQS_5	AP33	M_DQS_B_DP5
M_DATA_B_CB3	AR16	SB_ECC_CB_3	SB_DQS_6	AL33	M_DQS_B_DP6
M_DATA_B_CB4	AL15	SB_ECC_CB_4	SB_DQS_7	AG35	M_DQS_B_DP7
M_DATA_B_CB5	AM15	SB_ECC_CB_5			
M_DATA_B_CB6	AR15	SB_ECC_CB_6	SB_DQS#_0	AH6	M_DQS_B_DN0
M_DATA_B_CB7	AP15	SB_ECC_CB_7	SB_DQS#_1	AL8	M_DQS_B_DN1
			SB_DQS#_2	AP8	M_DQS_B_DN2
			SB_DQS#_3	AN12	M_DQS_B_DN3
			SB_DQS#_4	AN28	M_DQS_B_DN4
			SB_DQS#_5	AR33	M_DQS_B_DN5
			SB_DQS#_6	AM33	M_DQS_B_DN6
			SB_DQS#_7	AG34	M_DQS_B_DN7

Can be left as no connects if no support ECC.

DDR_1

SAN-1U2NF
(62.10055.441)

<Variant Name>

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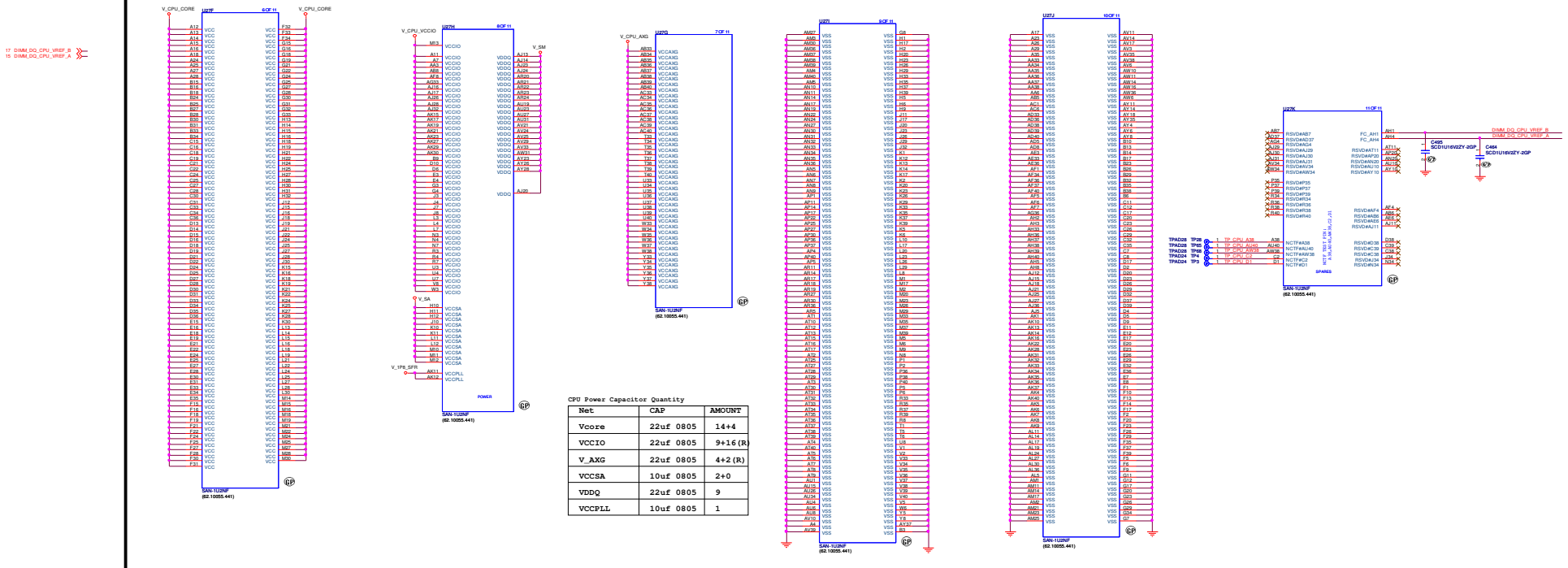
Title

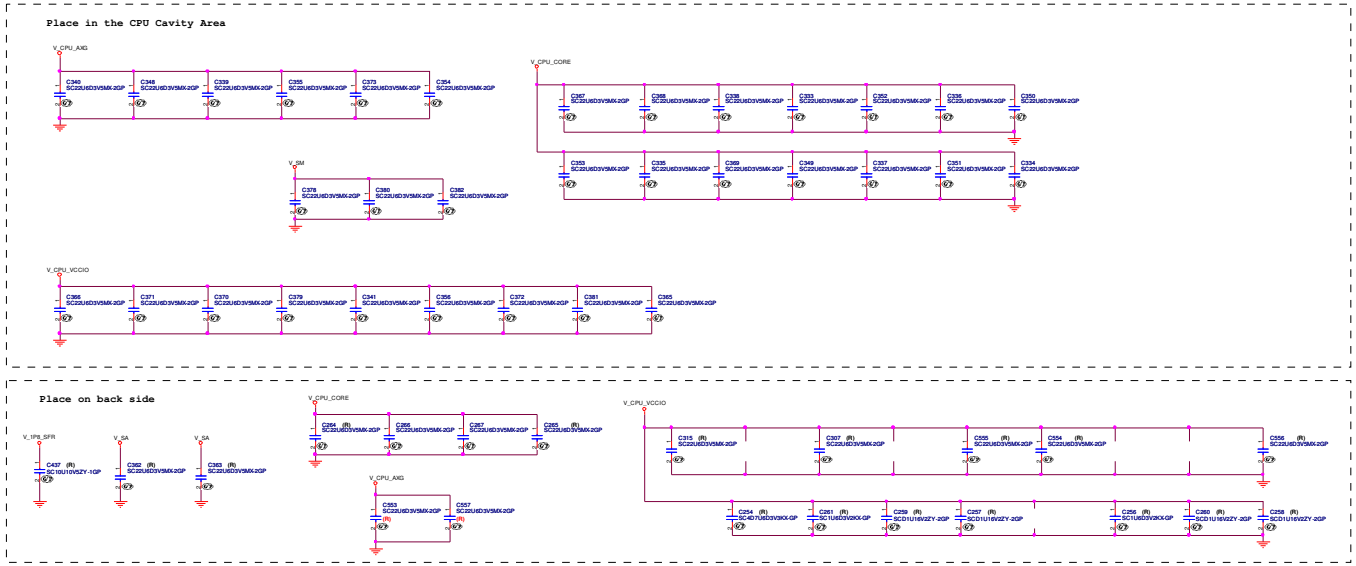
Size	Document Number	Rev
C	Rosa_Mission Hills	SA

Date: Sunday, March 20, 2011 Sheet 12 of 51



CPU Power Capacitor Quantity

Net	CAP	AMOUNT
Vcore	22uf 0805	14+4
VCCIO	22uf 0805	9+16 (R)
V_AXG	22uf 0805	4+2 (R)
VCCSA	10uf 0805	2+0
VDDQ	22uf 0805	9
VCCPLL	10uf 0805	1



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Size	Document Number	Rev
D	Ross_Mission Hills	SA

Date: Sunday, March 20, 2011 Sheet 13 of 51

XDP(ITP) for CPU

10 H_TDO
10 H_TDI
10 H_TMS
10 H_TCK
10 H_TRST_N
10,36 H_CPURST_N
10 H_PREQ_N
10 H_PRDY_N

10,19 H_PWRGD
10,19,36 PLTRST_N

15,17,36 SMB_DATA_MAIN
15,17,36 SMB_CLK_MAIN

10 XDP_DBRESET_N

10 H_BPM#0
10 H_BPM#1
10 H_BPM#2
10 H_BPM#3
10 H_BPM#4
10 H_BPM#5
10 H_BPM#6
10 H_BPM#7

20 CK_100M_CPU_XDP_DN
20 CK_100M_CPU_XDP_DP

10 CK_XDP_S_DP
10 CK_XDP_S_DN

XDP(ITP) for PCH

19 PCH_JTAG_RST_R
19,35 PCH_DPWROK
19 PCH_JTAG_TDO
19 PCH_JTAG_TDI
19 PCH_JTAG_TMS
19 PCH_JTAG_TCK
19,45 FP_RST_N
SW_ON_N

19,21,36 PWRGD_3V
20 CK_XDPG_PCH_100M_DP
20 CK_XDPG_PCH_100M_DN
22 USB_OC0_R_N
22 USB_OC1_R_N
22 USB_OC2_R_N
22 USB_OC3_R_N
22 USB_OC4_R_N
22 USB_OC5_R_N
22 USB_OC6_R_N
22 USB_OC7_R_N

LPC DEBUG PORT

19,36 L_AD0
19,36 L_AD1
19,36 L_AD2
19,36 L_AD3
19,36 L_FRAME_N
20 CK_P_33M_LPCP80

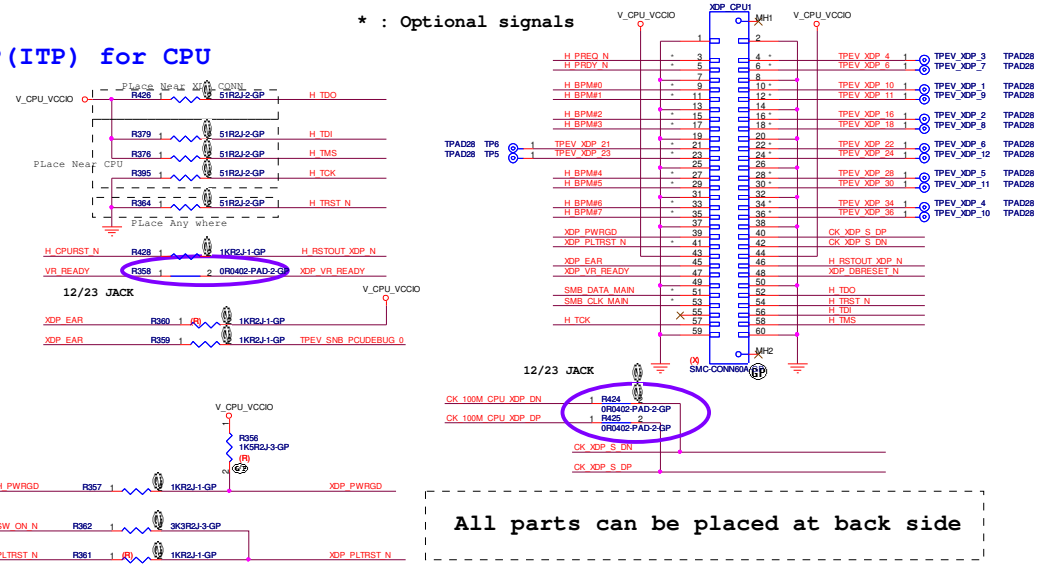
26,36 PLTRST_SL_N

10 TPEV_SNB_PCUDEBUG_0

19,50 VR_READY

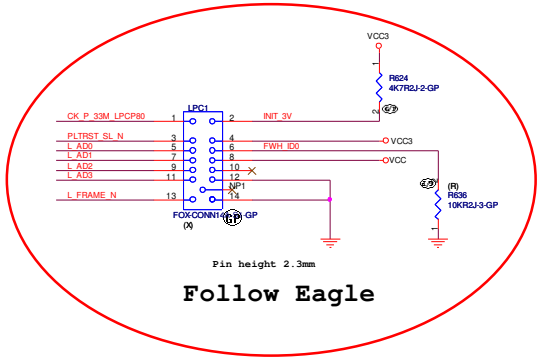
* : Optional signals

XDP(ITP) for CPU



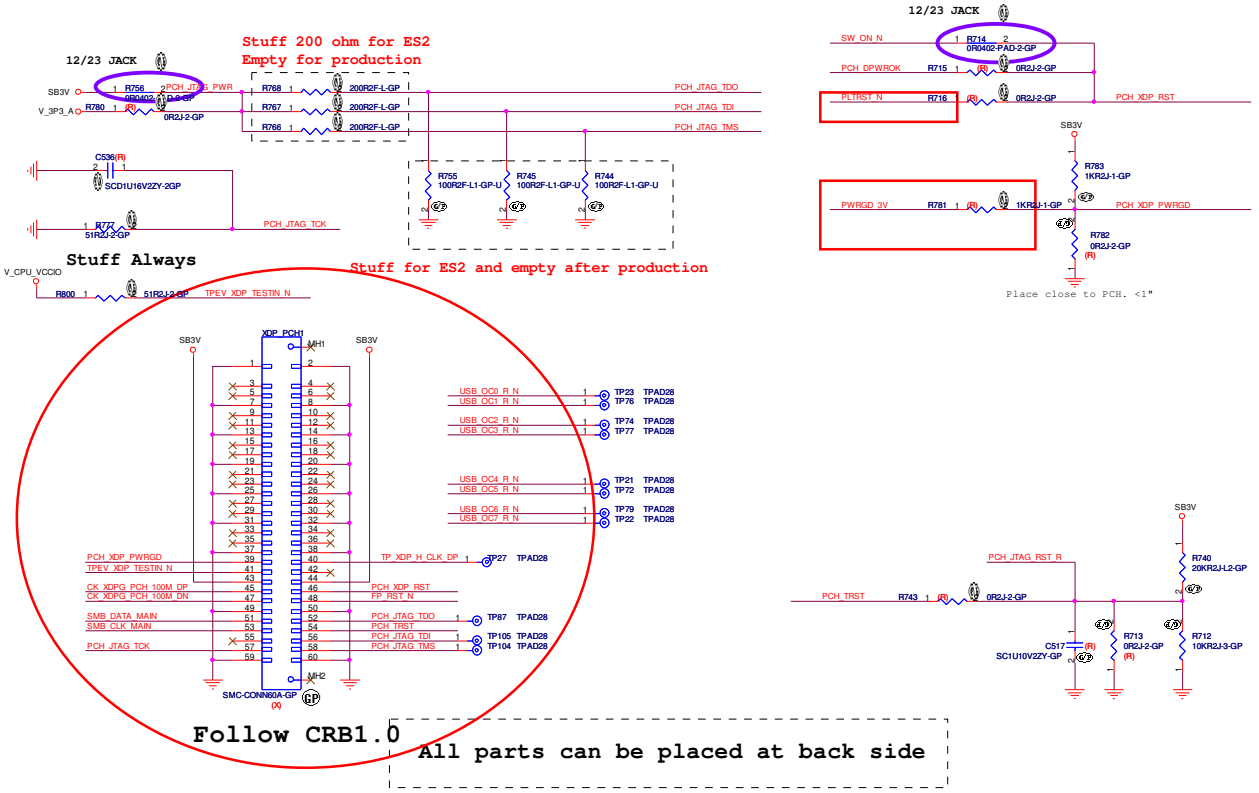
All parts can be placed at back side

LPC DEBUG PORT



Follow Eagle

XDP(ITP) for PCH



Follow CRB1.0

All parts can be placed at back side

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Title

Size	Document Number	Rev
C	Rosa_Mission Hills	SA

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DDR DATA

12 M_DATA_A[0..63]
12 M_DQS_A_DP[0..8]
12 M_DQS_A_DN[0..8]
12 M_DATA_A_CB[0..7]

DDR CMD/ADD

12 M_MAA_A[0..15]
12 M_WE_A_N
12 M_CAS_A_N
12 M_RAS_A_N
12 M_SBS_A0
12 M_SBS_A1
12 M_SBS_A2

DDR CTRL

12 M_SCS_A_N0
12 M_SCS_A_N1
12 M_SCKE_A0
12 M_SCKE_A1
12 M_ODT_A0
12 M_ODT_A1

DDR CLOCK

12 CK_M_DDR0_A_DP
12 CK_M_DDR0_A_DN
12 CK_M_DDR1_A_DP
12 CK_M_DDR1_A_DN

DDR OTHERS

12,17 DDR3_DRAMRST_N
14,17,36 SMB_DATA_MAIN
14,17,36 SMB_CLK_MAIN
19,26,32,36,41 SMB_CLK_RESUME
19,26,32,36,41 SMB_DATA_RESUME

13 DIMM_DQ_CPU_VREF_A

DIMM1A 1 OF 3

M_DATA_A0	3	DQ0	
M_DATA_A1	4	DQ1	
M_DATA_A2	9	DQ2	
M_DATA_A3	10	DQ3	
M_DATA_A4	122	DQ4	
M_DATA_A5	123	DQ5	
M_DATA_A6	128	DQ6	
M_DATA_A7	129	DQ7	
M_DATA_A8	12	DQ8	
M_DATA_A9	13	DQ9	
M_DATA_A10	18	DQ10	
M_DATA_A11	19	DQ11	
M_DATA_A12	131	DQ12	
M_DATA_A13	132	DQ13	
M_DATA_A14	137	DQ14	
M_DATA_A15	138	DQ15	
M_DATA_A16	21	DQ16	
M_DATA_A17	22	DQ17	
M_DATA_A18	27	DQ18	
M_DATA_A19	28	DQ19	
M_DATA_A20	140	DQ20	
M_DATA_A21	141	DQ21	
M_DATA_A22	146	DQ22	
M_DATA_A23	147	DQ23	
M_DATA_A24	30	DQ24	
M_DATA_A25	31	DQ25	
M_DATA_A26	36	DQ26	
M_DATA_A27	37	DQ27	
M_DATA_A28	149	DQ28	
M_DATA_A29	150	DQ29	
M_DATA_A30	155	DQ30	
M_DATA_A31	156	DQ31	
M_DATA_A32	81	DQ32	
M_DATA_A33	82	DQ33	
M_DATA_A34	87	DQ34	
M_DATA_A35	88	DQ35	
M_DATA_A36	200	DQ36	
M_DATA_A37	201	DQ37	
M_DATA_A38	206	DQ38	
M_DATA_A39	207	DQ39	
M_DATA_A40	90	DQ40	
M_DATA_A41	91	DQ41	
M_DATA_A42	96	DQ42	
M_DATA_A43	97	DQ43	
M_DATA_A44	209	DQ44	
M_DATA_A45	210	DQ45	
M_DATA_A46	215	DQ46	
M_DATA_A47	216	DQ47	
M_DATA_A48	99	DQ48	
M_DATA_A49	100	DQ49	
M_DATA_A50	105	DQ50	
M_DATA_A51	106	DQ51	
M_DATA_A52	218	DQ52	
M_DATA_A53	219	DQ53	
M_DATA_A54	224	DQ54	
M_DATA_A55	225	DQ55	
M_DATA_A56	108	DQ56	
M_DATA_A57	109	DQ57	
M_DATA_A58	114	DQ58	
M_DATA_A59	115	DQ59	
M_DATA_A60	227	DQ60	
M_DATA_A61	228	DQ61	
M_DATA_A62	233	DQ62	
M_DATA_A63	234	DQ63	

A0	188	M_MAA_A0	
A1	181	M_MAA_A1	
A2	61	M_MAA_A2	
A3	180	M_MAA_A3	
A4	59	M_MAA_A4	
A5	58	M_MAA_A5	
A6	178	M_MAA_A6	
A7	56	M_MAA_A7	
A8	177	M_MAA_A8	
A9	175	M_MAA_A9	
A10_AP	70	M_MAA_A10	
A11	55	M_MAA_A11	
A12_BC#	174	M_MAA_A12	
A13	196	M_MAA_A13	
A14	172	M_MAA_A14	
A15_NC	171	M_MAA_A15	
BA0	71	M_SBS_A0	
BA1	190	M_SBS_A1	
BA2	52	M_SBS_A2	
CK0	184	CK_M_DDR0_A_DP	
CK0#	185	CK_M_DDR0_A_DN	
CK1_NC	63	CK_M_DDR1_A_DP	
CK1#_NC	64	CK_M_DDR1_A_DN	
S0#	193	M_SCS_A_N0	
S1#_NC	76	M_SCS_A_N1	
S2#_NC	79		
S3#_NC	198		
CKE0	50	M_SCKE_A0	
CKE1_NC	169	M_SCKE_A1	
WE#	73	M_WE_A_N	
RAS#	192	M_RAS_A_N	
CAS#	74	M_CAS_A_N	
ODT0	195	M_ODT_A0	
ODT1_NC	77	M_ODT_A1	
PAR_IN_NC	68		
ERR_OUT#_NC	53		
CB0_NC	39	M_DATA_A_CB0	
CB1_NC	40	M_DATA_A_CB1	
CB2_NC	45	M_DATA_A_CB2	
CB3_NC	46	M_DATA_A_CB3	
CB4_NC	158	M_DATA_A_CB4	
CB5_NC	159	M_DATA_A_CB5	
CB6_NC	164	M_DATA_A_CB6	
CB7_NC	165	M_DATA_A_CB7	
RESET#	168	DDR3_DRAMRST_N	
VDDSPD	236	VCC3	
SA0	117		
SA1	237		
SA2	119		
SDA	238	SMB_DATA_MAIN	
SCL	118	SMB_CLK_MAIN	
VREFDQ	1	DIMM_DQ_VREF_A	
VREFCA	67	DIMM_CA_VREF_A	

DDR3-240P-4-GP
(22.10244.S21)
Black color
Pin Height is 2.7mm

Trace: 12/12 mils

DIMM1C 3 OF 3

M_DQS_A_DP0	7	DQS0	
M_DQS_A_DN0	6	DQS0#	
M_DQS_A_DP1	16	DQS1	
M_DQS_A_DN1	15	DQS1#	
M_DQS_A_DP2	25	DQS2	
M_DQS_A_DN2	24	DQS2#	
M_DQS_A_DP3	34	DQS3	
M_DQS_A_DN3	33	DQS3#	
M_DQS_A_DP4	85	DQS4	
M_DQS_A_DN4	84	DQS4#	
M_DQS_A_DP5	94	DQS5	
M_DQS_A_DN5	93	DQS5#	
M_DQS_A_DP6	103	DQS6	
M_DQS_A_DN6	102	DQS6#	
M_DQS_A_DP7	112	DQS7	
M_DQS_A_DN7	111	DQS7#	
M_DQS_A_DP8	43	DQS8	
M_DQS_A_DN8	42	DQS8#	
	125	DQS9_DM0	
	126	DQS9#_NC	
	134	DQS10_DM1	
	135	DQS10#_NC	
	143	DQS11_DM2	
	144	DQS11#_NC	
	152	DQS12_DM3	
	153	DQS12#_NC	
	203	DQS13_DM4	
	204	DQS13#_NC	
	212	DQS14_DM5	
	213	DQS14#_NC	
	221	DQS15_DM6	
	222	DQS15#_NC	
	230	DQS16_DM7	
	231	DQS16#_NC	
	161	DQS17_DM8	
	162	DQS17#_NC	
NP1		NP1	

DM8 must connect to GND

DDR3-240P-4-GP
(22.10244.S21)

DIMM1B 2 OF 3

V_SM

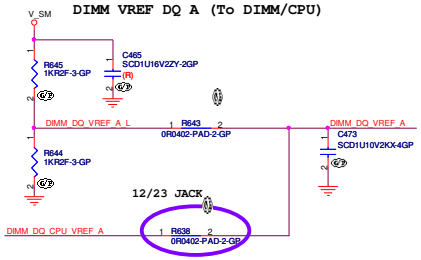
	2	VSS	
	5	VSS	
	8	VSS	
	11	VSS	
	14	VSS	
	17	VSS	
	20	VSS	
	23	VSS	
	26	VSS	
	29	VSS	
	32	VSS	
	35	VSS	
	38	VSS	
	41	VSS	
	44	VSS	
	47	VSS	
	80	VSS	
	83	VSS	
	86	VSS	
	89	VSS	
	92	VSS	
	95	VSS	
	98	VSS	
	101	VSS	
	104	VSS	
	107	VSS	
	110	VSS	
	113	VSS	
	116	VSS	
	121	VSS	
	124	VSS	
	127	VSS	
	130	VSS	
	133	VSS	
	136	VSS	
	139	VSS	
	142	VSS	
	145	VSS	
	148	VSS	
	151	VSS	
	154	VSS	
	157	VSS	
	160	VSS	
	163	VSS	
	166	VSS	
	199	VSS	
	202	VSS	
	205	VSS	
	208	VSS	
	211	VSS	
	214	VSS	
	217	VSS	
	220	VSS	
	223	VSS	
	226	VSS	
	229	VSS	
	232	VSS	
	235	VSS	
	239	VSS	
	51	VDD	
	54	VDD	
	57	VDD	
	60	VDD	
	62	VDD	
	65	VDD	
	66	VDD	
	69	VDD	
	72	VDD	
	75	VDD	
	78	VDD	
	170	VDD	
	173	VDD	
	176	VDD	
	179	VDD	
	182	VDD	
	183	VDD	
	186	VDD	
	189	VDD	
	191	VDD	
	194	VDD	
	197	VDD	
VTT_48_NC	48		
VTT_49_NC	49		
VTT	120	V_SM_VTT	
VTT	240		
EVENT#_NC	187		
NC_TEST	167		

DDR3-240P-4-GP
(22.10244.S21)

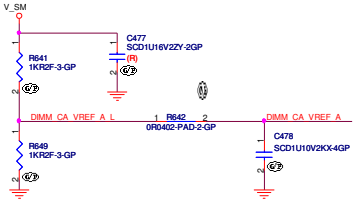
CHANNEL A DIMM1

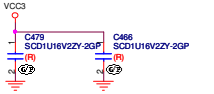
SMB ADDRESS: 000
SPD R/W: 0*A1, 0*A0

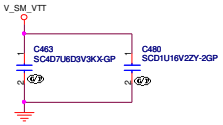
DIMM VREF DQ A (To DIMM/CPU)

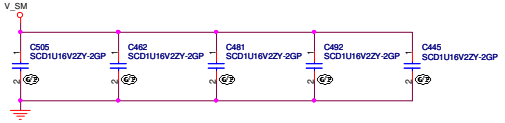


DIMM VREF CA A (To DIMM)









Place Near Power Pin

Net	CAP	AMOUNT
V_SM	1uf 0603 X5R	4
V_SM_VTT	4.7uf 0603 X5R	1
V_SM_VTT	0.1uf 0402 Y5V	1

<Variant Name>

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Title

Size	Document Number	Rev
C	Rosa_Mission Hills	SA

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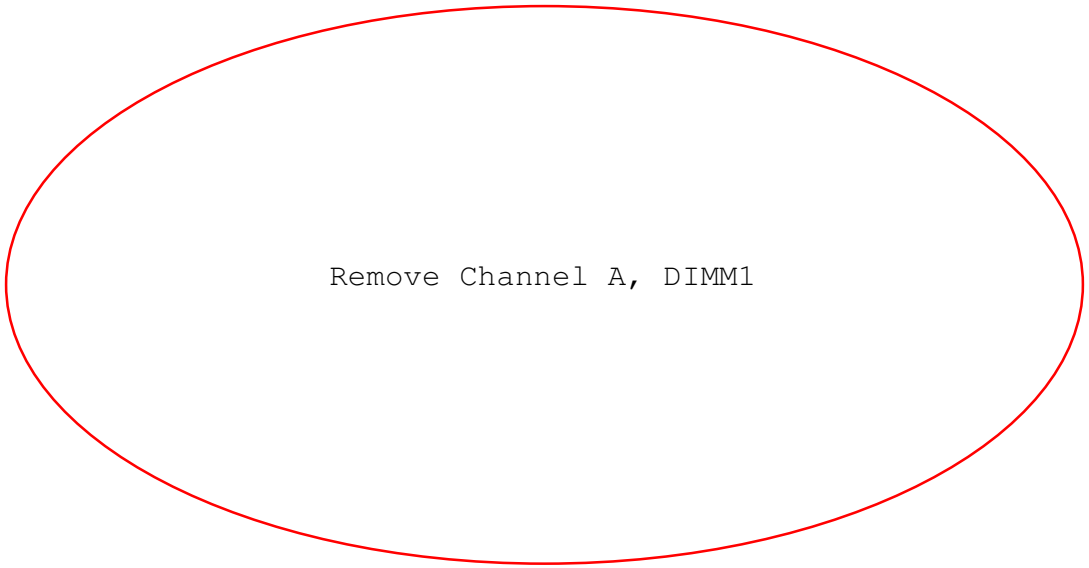

<Variant Name>

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Title

Size	Document Number	Rev
C	Rosa_Mission Hills	SA

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DDR DATA

12 M_DATA_B[0..63]
12 M_DQS_B_DP[0..8]
12 M_DQS_B_DN[0..8]
12 M_DATA_B_CB[0..7]

DDR CMD/ADD

12 M_MAA_B[0..15]
12 M_WE_B_N
12 M_CAS_B_N
12 M_RAS_B_N
12 M_SBS_B0
12 M_SBS_B1
12 M_SBS_B2

DDR CTRL

12 M_SCS_B_N0
12 M_SCS_B_N1
12 M_SCKE_B0
12 M_SCKE_B1
12 M_ODT_B0
12 M_ODT_B1

DDR CLOCK

12 CK_M_DDR0_B_DP
12 CK_M_DDR0_B_DN
12 CK_M_DDR1_B_DP
12 CK_M_DDR1_B_DN

DDR OTHERS

12,15 DDR3_DRAMRST_N
14,15,36 SMB_DATA_MAIN
14,15,36 SMB_CLK_MAIN
19,26,32,36,41 SMB_CLK_RESUME
19,26,32,36,41 SMB_DATA_RESUME

13 DIMM_DQ_CPU_VREF_B

DIMM2A 1 OF 3

M_DATA_B0	3	DQ0	A0	188	M_MAA_B0
M_DATA_B1	4	DQ1	A1	181	M_MAA_B1
M_DATA_B2	9	DQ2	A2	61	M_MAA_B2
M_DATA_B3	10	DQ3	A3	180	M_MAA_B3
M_DATA_B4	122	DQ4	A4	59	M_MAA_B4
M_DATA_B5	123	DQ5	A5	58	M_MAA_B5
M_DATA_B6	128	DQ6	A6	178	M_MAA_B6
M_DATA_B7	129	DQ7	A7	56	M_MAA_B7
M_DATA_B8	12	DQ8	A8	177	M_MAA_B8
M_DATA_B9	13	DQ9	A9	175	M_MAA_B9
M_DATA_B10	18	DQ10	A10_AP	70	M_MAA_B10
M_DATA_B11	19	DQ11	A11	55	M_MAA_B11
M_DATA_B12	131	DQ12	A12_BC#	174	M_MAA_B12
M_DATA_B13	132	DQ13	A13	196	M_MAA_B13
M_DATA_B14	137	DQ14	A14	172	M_MAA_B14
M_DATA_B15	138	DQ15	A15_NC	171	M_MAA_B15
M_DATA_B16	21	DQ16	BA0	71	M_SBS_B0
M_DATA_B17	22	DQ17	BA1	190	M_SBS_B1
M_DATA_B18	27	DQ18	BA2	52	M_SBS_B2
M_DATA_B19	28	DQ19			
M_DATA_B20	140	DQ20	CK0	184	CK_M_DDR0_B_DP
M_DATA_B21	141	DQ21	CK0#	185	CK_M_DDR0_B_DN
M_DATA_B22	146	DQ22	CK1_NC	63	CK_M_DDR1_B_DP
M_DATA_B23	147	DQ23	CK1#_NC	64	CK_M_DDR1_B_DN
M_DATA_B24	30	DQ24			
M_DATA_B25	31	DQ25	S0#	193	M_SCS_B_N0
M_DATA_B26	36	DQ26	S1#_NC	76	M_SCS_B_N1
M_DATA_B27	37	DQ27	S2#_NC	79	
M_DATA_B28	149	DQ28	S3#_NC	198	
M_DATA_B29	150	DQ29			
M_DATA_B30	155	DQ30	CKE0	50	M_SCKE_B0
M_DATA_B31	156	DQ31	CKE1_NC	169	M_SCKE_B1
M_DATA_B32	81	DQ32			
M_DATA_B33	82	DQ33	WE#	73	M_WE_B_N
M_DATA_B34	87	DQ34	RAS#	192	M_RAS_B_N
M_DATA_B35	88	DQ35	CAS#	74	M_CAS_B_N
M_DATA_B36	200	DQ36			
M_DATA_B37	201	DQ37	ODT0	195	M_ODT_B0
M_DATA_B38	206	DQ38	ODT1_NC	77	M_ODT_B1
M_DATA_B39	207	DQ39			
M_DATA_B40	90	DQ40	PAR_IN_NC	68	
M_DATA_B41	91	DQ41	ERR_OUT#_NC	53	
M_DATA_B42	96	DQ42			
M_DATA_B43	97	DQ43	CB0_NC	39	M_DATA_B_CB0
M_DATA_B44	209	DQ44	CB1_NC	40	M_DATA_B_CB1
M_DATA_B45	210	DQ45	CB2_NC	45	M_DATA_B_CB2
M_DATA_B46	215	DQ46	CB3_NC	46	M_DATA_B_CB3
M_DATA_B47	216	DQ47	CB4_NC	158	M_DATA_B_CB4
M_DATA_B48	99	DQ48	CB5_NC	159	M_DATA_B_CB5
M_DATA_B49	100	DQ49	CB6_NC	164	M_DATA_B_CB6
M_DATA_B50	105	DQ50	CB7_NC	165	M_DATA_B_CB7
M_DATA_B51	106	DQ51			
M_DATA_B52	218	DQ52	RESET#	168	DDR3_DRAMRST_N
M_DATA_B53	219	DQ53			
M_DATA_B54	224	DQ54	VDDSPD	236	VCC3
M_DATA_B55	225	DQ55	SA0	117	
M_DATA_B56	108	DQ56	SA1	237	
M_DATA_B57	109	DQ57	SA2	119	
M_DATA_B58	114	DQ58	SDA	238	SMB_DATA_MAIN
M_DATA_B59	115	DQ59	SCL	118	SMB_CLK_MAIN
M_DATA_B60	227	DQ60			
M_DATA_B61	228	DQ61	VREFDQ	1	DIMM_DQ_VREF_B
M_DATA_B62	233	DQ62	VREFCA	67	DIMM_CA_VREF_B
M_DATA_B63	234	DQ63			

DDR3-240P-4-GP
(22.10244.S21)
Black color
Pin Height is 2.7mm

Trace: 12/12 mils

DIMM2C 3 OF 3

M_DQS_B_DP0	7	DQS0	
M_DQS_B_DN0	6	DQS0#	
M_DQS_B_DP1	16	DQS1	
M_DQS_B_DN1	15	DQS1#	
M_DQS_B_DP2	25	DQS2	
M_DQS_B_DN2	24	DQS2#	
M_DQS_B_DP3	34	DQS3	
M_DQS_B_DN3	33	DQS3#	
M_DQS_B_DP4	85	DQS4	
M_DQS_B_DN4	84	DQS4#	
M_DQS_B_DP5	94	DQS5	
M_DQS_B_DN5	93	DQS5#	
M_DQS_B_DP6	103	DQS6	
M_DQS_B_DN6	102	DQS6#	
M_DQS_B_DP7	112	DQS7	
M_DQS_B_DN7	111	DQS7#	
M_DQS_B_DP8	43	DQS8	
M_DQS_B_DN8	42	DQS8#	
	125	DQS9_DM0	
	126	DQS9#_NC	
	134	DQS10_DM1	
	135	DQS10#_NC	
	143	DQS11_DM2	
	144	DQS11#_NC	
	152	DQS12_DM3	
	153	DQS12#_NC	
	203	DQS13_DM4	
	204	DQS13#_NC	
	212	DQS14_DM5	
	213	DQS14#_NC	
	221	DQS15_DM6	
	222	DQS15#_NC	
	230	DQS16_DM7	
	231	DQS16#_NC	
	161	DQS17_DM8	
	162	DQS17#_NC	
	195	NP1	

DM8 must connect to GND

DDR3-240P-4-GP
(22.10244.S21)

DIMM2B 2 OF 3

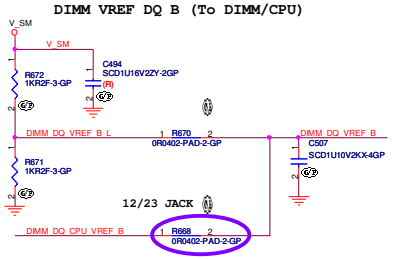
	2	VSS	VDD	51	
	5	VSS	VDD	54	
	8	VSS	VDD	57	
	11	VSS	VDD	60	
	14	VSS	VDD	62	
	17	VSS	VDD	65	
	20	VSS	VDD	66	
	23	VSS	VDD	69	
	26	VSS	VDD	72	
	29	VSS	VDD	75	
	32	VSS	VDD	78	
	35	VSS	VDD	170	
	38	VSS	VDD	173	
	41	VSS	VDD	176	
	44	VSS	VDD	179	
	47	VSS	VDD	182	
	80	VSS	VDD	183	
	83	VSS	VDD	186	
	86	VSS	VDD	189	
	89	VSS	VDD	191	
	92	VSS	VDD	194	
	95	VSS	VDD	197	
	98	VSS			
	101	VSS	VTT_48_NC	48	
	104	VSS	VTT_49_NC	49	
	107	VSS	VTT	120	V_SM_VTT
	110	VSS	VTT	240	
	113	VSS			
	116	VSS	EVENT#_NC	187	
	121	VSS	NC_TEST	167	
	124	VSS			
	127	VSS			
	130	VSS			
	133	VSS			
	136	VSS			
	139	VSS			
	142	VSS			
	145	VSS			
	148	VSS			
	151	VSS			
	154	VSS			
	157	VSS			
	160	VSS			
	163	VSS			
	166	VSS			
	199	VSS			
	202	VSS			
	205	VSS			
	208	VSS			
	211	VSS			
	214	VSS			
	217	VSS			
	220	VSS			
	223	VSS			
	226	VSS			
	229	VSS			
	232	VSS			
	235	VSS			
	239	VSS			

DDR3-240P-4-GP
(22.10244.S21)

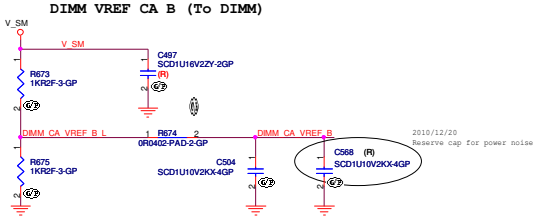
CHANNEL B DIMM1

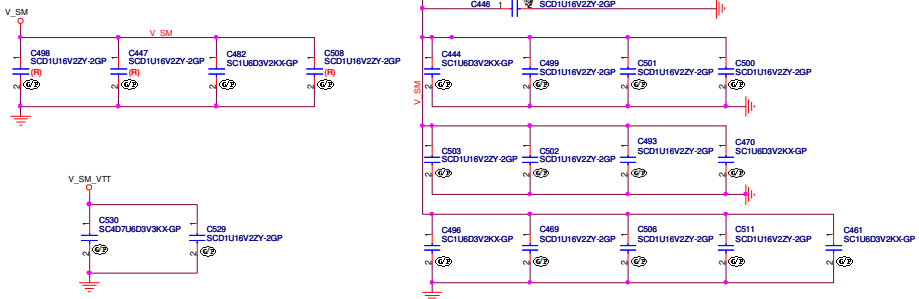
SMB ADDRESS: 010
SPD R/W: 0*A5, 0*A4

DIMM VREF DQ B (To DIMM/CPU)



DIMM VREF CA B (To DIMM)





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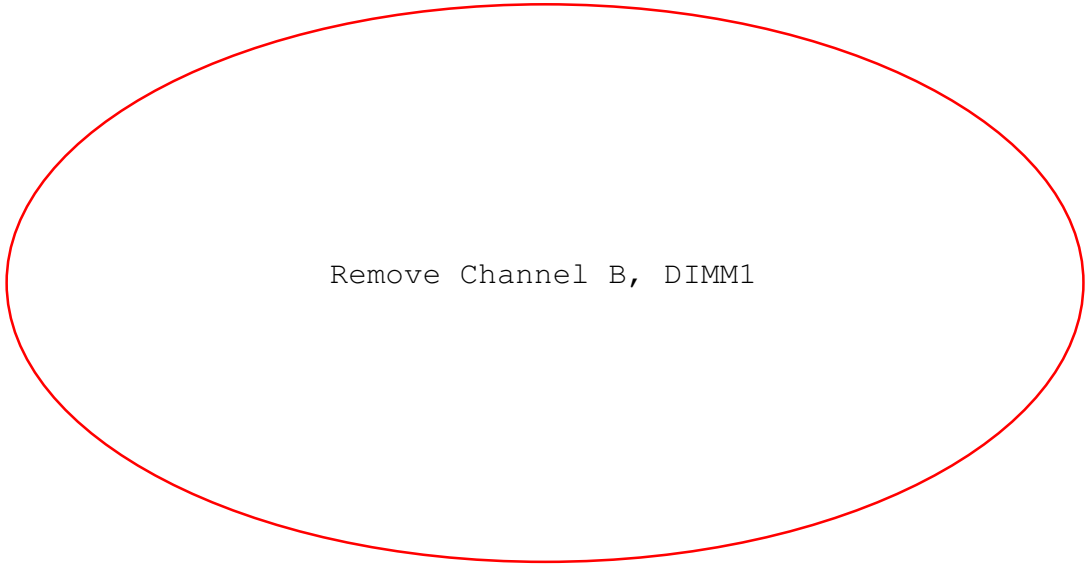
Size	Document Number	Rev
C	Rosa_Mission Hills	SA

Date: Sunday, March 20, 2011 Sheet 17 of 51



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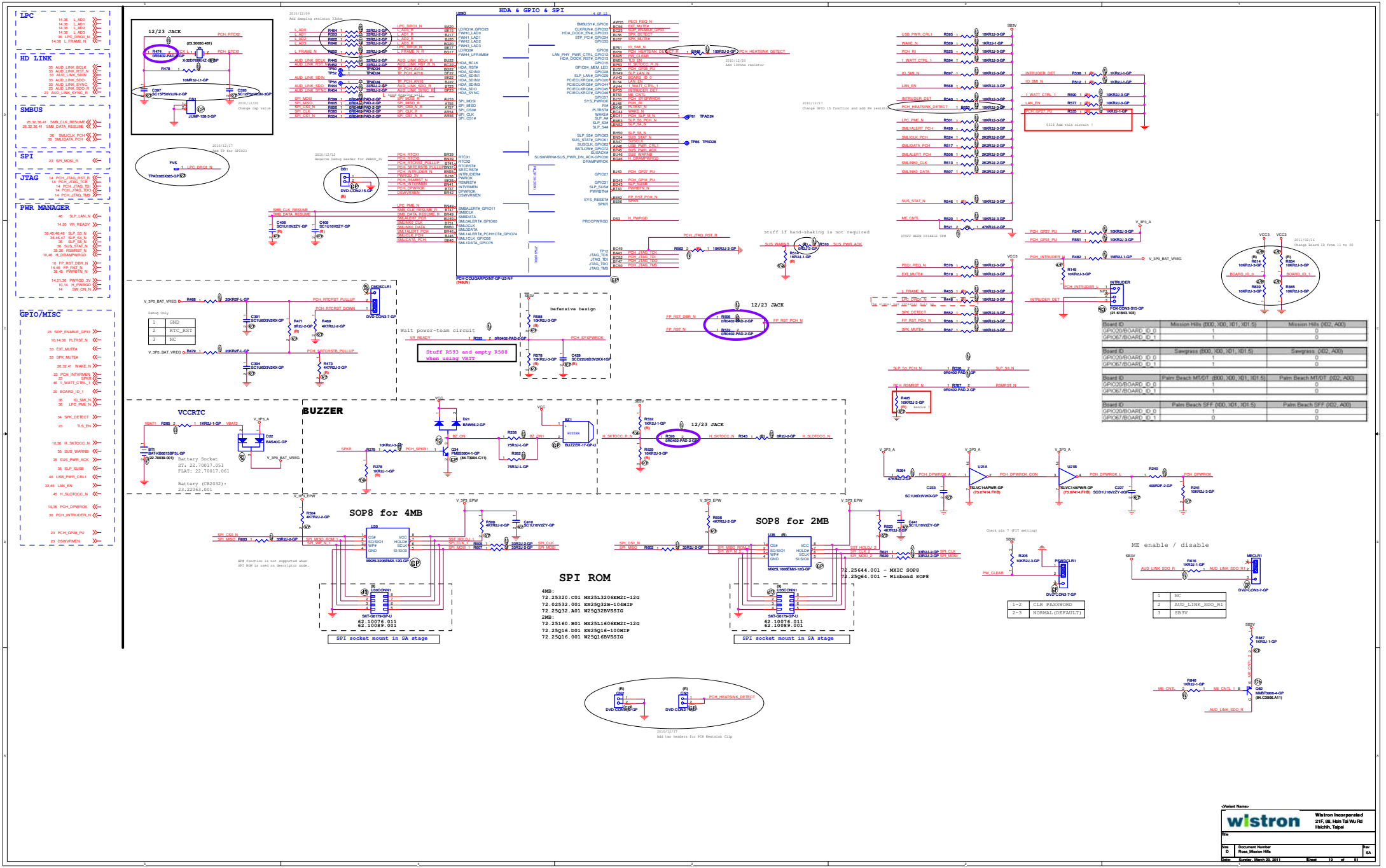
Date: Sunday, March 20, 2011 Sheet 18 of 51


LPC
HD LINK
SMBUS
SPI
JTAG
PWR MANAGER
GPIO/MISC
HDA & GPIO & SPI
12/23 JACK
BUZZER
VCCRTC
SOP8 for 4MB
SOP8 for 2MB
SPI ROM
4MB:
72.25320.C01 MX25L3206EM2I-12G
72.02532.001 EN25Q32B-104HIP
72.25Q32.A01 W25Q32BVSSIG
2MB:
72.25160.B01 MX25L1606EM2I-12G
72.25Q16.D01 EN25Q16-100HIP
72.25Q16.001 W25Q16BVSSIG
72.25644.001 - MXIC SOP8
72.25Q64.001 - Winbond SOP8
SPI socket mount in SA stage
SPI socket mount in SA stage
Defensive Design
Wait power-team circuit
Stuff R593 and empty R588 when using VR5T
Stuff if hand-shaking is not required
ME enable / disable
Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

CPU CLOCK

14 CK_100M_CPU_XDP_DN
14 CK_100M_CPU_XDP_DP

PCI CLOCK

36 CK_P_33M_SIO
22 CK_PCH_33M_FB
14 CK_P_33M_LPCP80

PCIE CLOCK

26 CK_PE_100M_16PORT_DP
26 CK_PE_100M_16PORT_DN
10 CK_PE_100M_MCP_DN
10 CK_PE_100M_MCP_DP
14 CK_XDPG_PCH_100M_DP
14 CK_XDPG_PCH_100M_DN
41 CK_PCIE_1PCIEX1_DN
41 CK_PCIE_1PCIEX1_DP
41 CK_PCIE_2PCIEX1_DN
41 CK_PCIE_2PCIEX1_DP
41 CK_PCIE_3PCIEX1_DN
41 CK_PCIE_3PCIEX1_DP
32 CK_GLAN_DN
32 CK_GLAN_DP

14M CLOCK

9 CK_14M_PCH
36 CK_14M_SIO2
19 BOARD_ID_1

FDI

11 FDI_TX_DN[0..7]
11 FDI_TX_DP[0..7]
11 DL_FSYNC_0
11 DL_LSYNC_0
11 DL_FSYNC_1
11 DL_LSYNC_1
11 FDI_INT

NVRAM

23 NVR_CLE

U29H — 8 OF 12 — PCH-COUGARPOINT-GP-U2-NF (749JN)

To LPC P80 Debug — CK_P_33M_LPCP80 — R354 22R2J-2-GP — CK_33M_PCI0 — AT11 CLKOUT_PCI0
TPAD24 TP34 — CK_33M_PCI1 — AN14 CLKOUT_PCI1
LOOPBACK CLK — CK_PCH_33M_FB — R388 22R2J-2-GP — CK_33M_PCI2 — AT12 CLKOUT_PCI2
To SIO — CK_P_33M_SIO — R406 22R2J-2-GP — CK_33M_PCI3 — AT17 CLKOUT_PCI3
TPAD24 TP40 — CK_33M_PCI4 — AT14 CLKOUT_PCI4

To SIO — TPAD24 TP32 — CLKOUTFLEX0 — AT9 CLKOUTFLEX0_GPIO64
To SIO — CK_14M_SIO2 — R399 22R2J-2-GP — CK_14M_FLEX — BA5 CLKOUTFLEX1_GPIO65
BOARD_ID_1 — AW5 CLKOUTFLEX2_GPIO66
BA2 CLKOUTFLEX3_GPIO67
2011/01/31 Remove TP
V_1P05_PCH — R392 90D9R2F-1-GP — XCLK_RCOMP — AL2 XCLK_RCOMP
CK_14M_PCH — AN8 REFCLK14IN

CLKIN_GND1_N/P — R27 CK_100M_CPHY_PCH_IN_DN — R418 10KR2J-3-GP; P27 CK_100M_CPHY_PCH_IN_DP — R414 10KR2J-3-GP
CLKIN_GND0_N/P — W53 CK_CSI_PCH_IN_DN — R530 10KR2J-3-GP; V52 CK_CSI_PCH_IN_DP — R531 10KR2J-3-GP
CLKOUT_ITPXDP_N/P — R52 CK_100M_CPU_XDP_DN; N52 CK_100M_CPU_XDP_DP — 12/23 JACK — CLK OUT TO XDP
CLKOUT_PCIE7N/P — AE2 CK_PCIEX1_DN — R202 0R0402-PAD-2-GP — CK_PCIE_1PCIEX1_DN; AF1 CK_PCIEX1_DP — R201 0R0402-PAD-2-GP — CK_PCIE_1PCIEX1_DP — CLK OUT TO PCIEX1
CLKOUT_DMI_N/P — P31 CK_PE_100M_DMI_DN — R462 0R0402-PAD-2-GP — CK_PE_100M_MCP_DN; R31 CK_PE_100M_DMI_DP — R466 0R0402-PAD-2-GP — CK_PE_100M_MCP_DP — CLK OUT TO CPU for DMI
CLKOUT_DP_N/P — N56 CLKOUT_DP_N — TP25 TPAD28; M55 CLKOUT_DP_P — TP24 TPAD28 — CLK OUT TO CPU??
CLKOUT_PCIE6N/P — AE6 CLKOUT_PCIE6N — R194 0R0402-PAD-2-GP — CK_PCIE_2PCIEX1_DN; AC6 CLKOUT_PCIE6P — R193 0R0402-PAD-2-GP — CK_PCIE_2PCIEX1_DP — CLK OUT TO PCIEX1
CLKOUT_PCIE1N/P — AA5 CK_PE1_R_DN — TP7 TPAD28; W5 CK_PE1_R_DP — TP11 TPAD28 — 12/23 JACK
CLKOUT_PCIE2N/P — AB12 CK_GLAN_DN; AB14 CK_GLAN_DP — CLK OUT TO PCIEX1 for LAN
CLKOUT_PCIE3N/P — AB9 CLKOUT_PCIE3N — R408 0R0402-PAD-2-GP — CK_XDPG_PCH_100M_DN; AB8 CLKOUT_PCIE3P — R407 0R0402-PAD-2-GP — CK_XDPG_PCH_100M_DP — CLK OUT TO PCH-XDP
CLKOUT_PCIE4N/P — Y9 CLKOUT_PCIE4N — R196 0R0402-PAD-2-GP — CK_PCIE_3PCIEX1_DN; Y8 CLKOUT_PCIE4P — R188 0R0402-PAD-2-GP — CK_PCIE_3PCIEX1_DP — CLK OUT TO PCIEX1
CLKOUT_PCIE5N/P — AF3, AG2 — 2011/01/31 Remove TP — 12/23 JACK
CLKOUT_PCIE6N/P — AR3 CLKOUT_PCIE6N — TP9 TPAD28; AA2 CLKOUT_PCIE6P — TP13 TPAD28 — CLK OUT TO PCIEX1 for LAN
CLKOUT_PEG_A_N/P — AG8 CK_PE_16PORT_PCH_DN — R197 0R0402-PAD-2-GP — CK_PE_100M_16PORT_DN; AG9 CK_PE_16PORT_PCH_DP — R195 0R0402-PAD-2-GP — CK_PE_100M_16PORT_DP — CLK OUT TO CPU for X16 Graphic
CLKOUT_PEG_B_N/P — AE12 CK_PCIEX4_DN — TP35 TPAD24; AE11 CK_PCIEX4_DP — TP33 TPAD24 — 12/23 JACK

NOTE:The 1Mohm Damping Resistor
Use 0603 and Can't change to 0402!

XTAL_25M_PCH_OUT — AJ5 XTAL25_OUT
R383 1MR3F-GP
XTAL_25M_PCH_IN — AJ3 XTAL25_IN
X2 XTAL-25MHZ-32GP DIP +- 20ppm CL:12P
C322 SC15P50V2JN-2-GP
C321 SC12P50V2JN-3GP
When support FCIM need to stuff.
XTAL_IN should be pulled to GND via a 0-Ω resistor by default.
Intel reliability concerns

WHEN USING 25MHZ EXTERNAL REFERENCE FROM SINAI CMV:
REMOVE R63CK, Y5LB, C56LB
REPLACE C37LB WITH 500HM RES 0402 PACKAGE

DUAL CHANNEL NAND INTERFACE

U29E — 5 OF 12 — PCH-COUGARPOINT-GP-U2-NF (749JN)

NVR_CLE — M48 NV_ALE; R47 NV_CLE; Y41 NV_RB#; M50 NV_RE#_WRB0; M49 NV_RE#_WRB1; U43 NV_WE#_CK0; J57 NV_WE#_CK1

NV_DQ0_NV_IO0 AB59; NV_DQ1_NV_IO1 Y50; NV_DQ2_NV_IO2 AB45; NV_DQ3_NV_IO3 AB44; NV_DQ4_NV_IO4 U49; NV_DQ5_NV_IO5 R44; NV_DQ6_NV_IO6 U50; NV_DQ7_NV_IO7 U46; NV_DQ8_NV_IO8 U44; NV_DQ9_NV_IO9 H50; NV_DQ10_NV_IO10 K46; NV_DQ11_NV_IO11 L56; NV_DQ12_NV_IO12 J55; NV_DQ13_NV_IO13 F53; NV_DQ14_NV_IO14 H52; NV_DQ15_NV_IO15 E52

NV_CE#0 K50; NV_CE#1 K49; NV_CE#2 AB46; NV_CE#3 G56
NV_DQS0 Y44; NV_DQS1 L53
NV_RCOMP — R50 PCH_NV_RCOMP — (R) R518 32D4R2F-GP

U29G — 7 OF 12 — FDILINK — PCH-COUGARPOINT-GP-U2-NF (749JN)

TPAD24 TP63 — TP21 H31 — FDI_RXN0 C42 — FDI_TX_DN0
TPAD24 TP62 — TP25 J31 — FDI_RXP0 B43 — FDI_TX_DP0
TPAD28 TP20 — TP29 C29 — FDI_RXN1 F45 — FDI_TX_DN1
TPAD24 TP19 — TP33 E29 — FDI_RXP1 F43 — FDI_TX_DP1
FDI_RXN2 H41 — FDI_TX_DN2
TPAD24 TP61 — TP22 J27 — FDI_RXP2 J41 — FDI_TX_DP2
TPAD24 TP57 — TP26 L27 — FDI_RXN3 C46 — FDI_TX_DN3
TPAD24 TP18 — TP30 F28 — FDI_RXP3 D47 — FDI_TX_DP3
TPAD28 TP16 — TP34 E27 — FDI_RXN4 B45 — FDI_TX_DN4
FDI_RXP4 A46 — FDI_TX_DP4
TPAD24 TP58 — TP23 J25 — FDI_RXN5 B47 — FDI_TX_DN5
TPAD24 TP55 — TP27 L25 — FDI_RXP5 C49 — FDI_TX_DP5
TPAD28 TP15 — TP31 C26 — FDI_RXN6 J43 — FDI_TX_DN6
TPAD24 TP14 — TP35 B27 — FDI_RXP6 H43 — FDI_TX_DP6
FDI_RXN7 M43 — FDI_TX_DN7
TPAD24 TP51 — TP24 L22 — FDI_RXP7 P43 — FDI_TX_DP7
TPAD24 TP49 — TP28 J22
TPAD24 TP53 — TP32 B25 — FDI_FSYNC0 B51 — DL_FSYNC_0
TPAD28 TP17 — TP36 D25 — FDI_LSYNC0 E49 — DL_LSYNC_0
FDI_FSYNC1 C52 — DL_FSYNC_1
FDI_LSYNC1 D51 — DL_LSYNC_1
FDI_INT H46 — FDI_INT

If want to disable FDI function:
1.Connect FDI_FSYNC and FDI_LSYNC and FDI_INT to GND
2.Float FDI TX and RX

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Title

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C	Rosa_Mission Hills	SA

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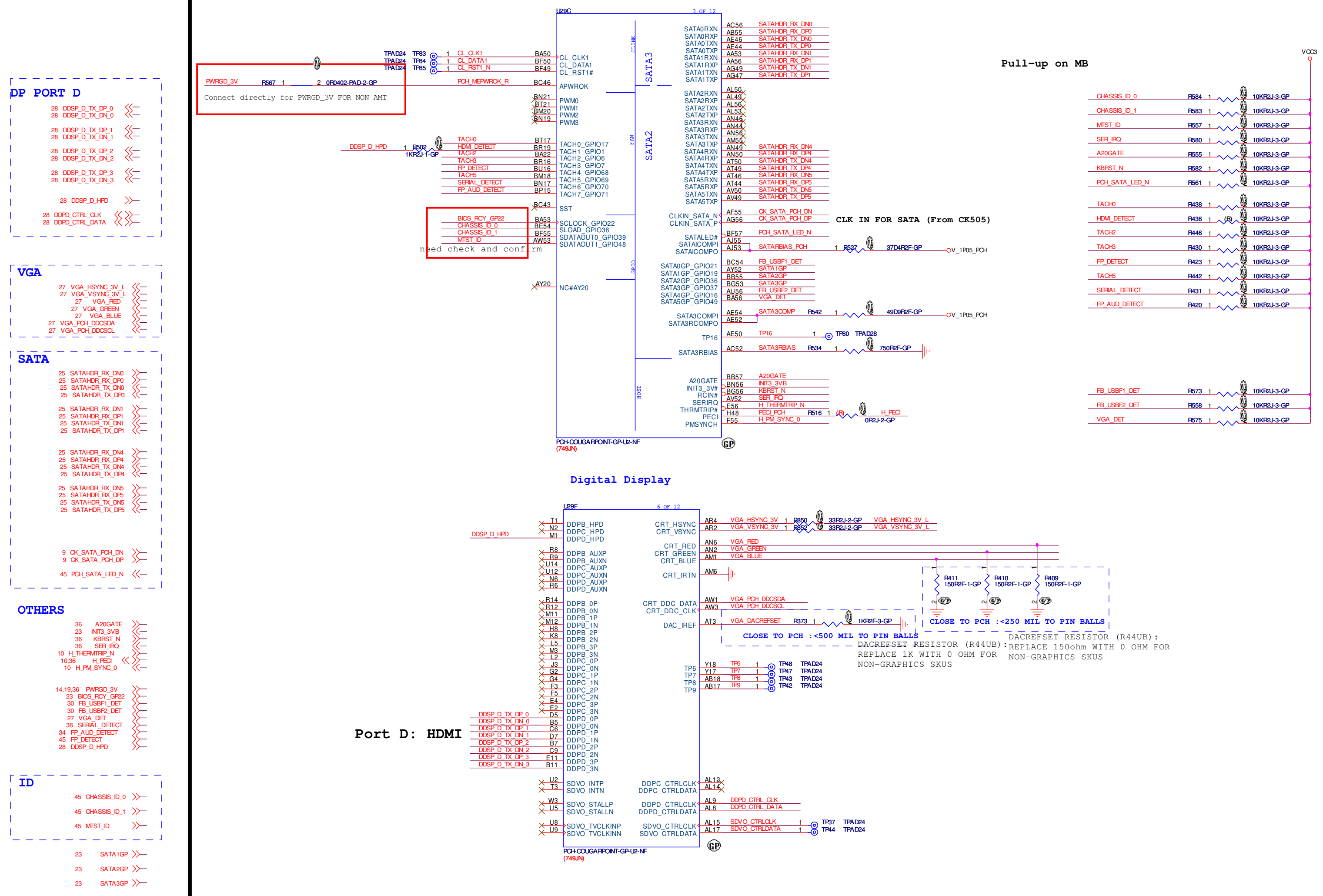

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Date: Sunday, March 20, 2011 Sheet 21 of 51

PCI

20 CK_PCH_33M_FB

23 P_GNT_N0
23 P_GNT_N1
23 P_GNT_N2
23 P_GNT_N3

DMI

11 DMI_MT_IR_DN[0..3]
11 DMI_MT_IR_DP[0..3]
11 DMI_IT_MR_DN[0..3]
11 DMI_IT_MR_DP[0..3]

9 100M_DMI_PCH_DN
9 100M_DMI_PCH_DP

PCIE

32 HSI_LAN_DN1
32 HSI_LAN_DP1
32 HSO_C_LAN_DN1
32 HSO_C_LAN_DP1

41 HSI_DN2
41 HSI_DP2
41 HSO_C_DN2
41 HSO_C_DP2

41 HSI_DN3
41 HSI_DP3
41 HSO_C_DN3
41 HSO_C_DP3

41 HSI_DN4
41 HSI_DP4
41 HSO_C_DN4
41 HSO_C_DP4

USB

30 USB_PCH_DN0
30 USB_PCH_DP0
30 USB_PCH_DN1
30 USB_PCH_DP1
30 USB_PCH_DN2
30 USB_PCH_DP2
30 USB_PCH_DN3
30 USB_PCH_DP3

31 USB_PCH_DN4
31 USB_PCH_DP4
31 USB_PCH_DN5
31 USB_PCH_DP5

31 USB_PCH_DN8
31 USB_PCH_DP8

31 USB_PCH_DN9
31 USB_PCH_DP9

31 USB_PCH_DN10
31 USB_PCH_DP10
31 USB_PCH_DN11
31 USB_PCH_DP11

30 USB_OC_01*
30 USB_OC_23*

31 USB_OC_1011*
31 USB_OC_89*
31 USB_OC_45*

VGA CLK

9 CK_96M_DREF_DN
9 CK_96M_DREF_DP

OTHERS

14 USB_OC0_R_N
14 USB_OC1_R_N
14 USB_OC2_R_N
14 USB_OC3_R_N
14 USB_OC4_R_N
14 USB_OC5_R_N
14 USB_OC6_R_N
14 USB_OC7_R_N

PCI

U29A 1 OF 12

TPAD24 TP31 — TP_BH8 — BH8
P_DEVSEL_N — BH9
CK_PCH_33M_FB — BD15
TPAD24 TP38 — P_PCIRST_N — AV14
P_IRDY_N — BF11
TPAD24 TP45 — P_PME_N — AV15
P_SERR_N — BR6
P_STOP_N — BC12
P_PLOCK_N — BA12
P_TRDY_N — BC8
P_PERR_N — BM3
P_FRAME_N — BC11

This pin have internal pull up

PAR, DEVSEL#, CLKIN_PCILOOPBACK, PCIRST#, IRDY#, PME#, SERR#, STOP#, PLOCK#, TRDY#, PERR#, FRAME#

P_GNT_N0 — BA15 — GNT0#
P_GNT_N1 — AV8 — GNT1#_GPIO51
P_GNT_N2 — BU12 — GNT2#_GPIO53
P_GNT_N3 — BE2 — GNT3#_GPIO55

P_REQ_N0 — BG5 — REQ0#
P_REQ_N1 — BT5 — REQ1#_GPIO50
P_REQ_N2 — BK6 — REQ2#_GPIO52
P_REQ_N3 — AV11 — REQ3#_GPIO54

P_INTA_N — BK10 — PIRQA#
P_INTB_N — BJ5 — PIRQB#
P_INTC_N — BM15 — PIRQC#
P_INTD_N — BP5 — PIRQD#
P_INTE_N — BN5 — PIRQE#_GPIO2
P_INTF_N — AV9 — PIRQF#_GPIO3
P_INTG_N — BT15 — PIRQG#_GPIO4
P_INTH_N — BR4 — PIRQH#_GPIO5

AD0–AD31, C_BE0#–C_BE3#

PCH-COUGARPOINT-GP-U2-NF (749JIN)

RN5 SRN8K2-4-GP: P_SERR_N, P_REQ_N1, P_REQ_N2, P_INTH_N
RN6 SRN8K2-4-GP: P_INTD_N, P_PERR_N, P_INTB_N, P_REQ_N0
RN2 SRN8K2-4-GP: P_PLOCK_N, P_STOP_N, P_IRDY_N, P_DEVSEL_N
RN3 SRN8K2-4-GP: P_FRAME_N, P_TRDY_N, P_REQ_N3, P_INTF_N
RN4 SRN8K2-4-GP: P_INTG_N, P_INTC_N, P_INTA_N, P_INTE_N

VCC3

USB & DMI & PCIE

U29B 2 OF 12

DMI_MT_IR_DN0 — D33 — DMI0RXN
DMI_MT_IR_DP0 — B33 — DMI0RXP
DMI_IT_MR_DN0 — J36 — DMI0TXN
DMI_IT_MR_DP0 — H36 — DMI0TXP
DMI_MT_IR_DN1 — A36 — DMI1RXN
DMI_MT_IR_DP1 — B35 — DMI1RXP
DMI_IT_MR_DN1 — P38 — DMI1TXN
DMI_IT_MR_DP1 — R38 — DMI1TXP
DMI_MT_IR_DN2 — B37 — DMI2RXN
DMI_MT_IR_DP2 — C36 — DMI2RXP
DMI_IT_MR_DN2 — H38 — DMI2TXN
DMI_IT_MR_DP2 — J38 — DMI2TXP
DMI_MT_IR_DN3 — E37 — DMI3RXN
DMI_MT_IR_DP3 — F38 — DMI3RXP
DMI_IT_MR_DN3 — M41 — DMI3TXN
DMI_IT_MR_DP3 — P41 — DMI3TXP
R31 — DMI_IRCOMP
E31 — DMI_ZCOMP

DMICOMP
4mil width / 8mil spacing
<500mils
V_1P05_PCH — R472 49D9R2F-GP — DMICOMP

CLK From CK505
100M_DMI_PCH_DN — P33 — CLKIN_DMI_N
100M_DMI_PCH_DP — R33 — CLKIN_DMI_P

USB:
USBP0N — BF36 — USB_PCH_DN0 — FOR Front USB
USBP0P — BD36 — USB_PCH_DP0 — FOR Front USB
USBP1N — BC33 — USB_PCH_DN1 — FOR Internal USB
USBP1P — BA33 — USB_PCH_DP1 — FOR Internal USB
USBP2N — BM33 — USB_PCH_DN2 — FOR Rear USB+LAN
USBP2P — BM35 — USB_PCH_DP2 — FOR Rear USB+LAN
USBP3N — BT33 — USB_PCH_DN3
USBP3P — BU32 — USB_PCH_DP3
USBP4N — BR32 — USB_PCH_DN4
USBP4P — BT31 — USB_PCH_DP4
USBP5N — BN29 — USB_PCH_DN5
USBP5P — BM30 — USB_PCH_DP5
USBP6N — BK33
USBP6P — BJ33
USBP7N — BF33
USBP7P — BD31
USBP8N — BN27 — USB_PCH_DN8
USBP8P — BR29 — USB_PCH_DP8
USBP9N — BR26 — USB_PCH_DN9
USBP9P — BT27 — USB_PCH_DP9
USBP10N — BK25 — USB_PCH_DN10
USBP10P — BJ25 — USB_PCH_DP10
USBP11N — BJ31 — USB_PCH_DN11
USBP11P — BK31 — USB_PCH_DP11
USBP12P — BD27
USBP12N — BF27
USBP13P — BK27
USBP13N — BJ27

OC0#_GPIO59 — BM43 — USB_OC0_R_N — R490 0R0402-PAD-2-GP — USB_OC_01*
OC1#_GPIO40 — BD41 — USB_OC1_R_N — R496 0R0402-PAD-2-GP — USB_OC_23*
OC2#_GPIO41 — BG41 — USB_OC2_R_N — R487 0R0402-PAD-2-GP — USB_OC_45*
OC3#_GPIO42 — BK43 — USB_OC3_R_N — R528 10KR2J-3-GP — USB_OC_67*
OC4#_GPIO43 — BP43 — USB_OC4_R_N — R489 0R0402-PAD-2-GP — USB_OC_89*
OC5#_GPIO9 — BJ41 — USB_OC5_R_N — R483 0R0402-PAD-2-GP — USB_OC_1011* — (R) R491 10KR2J-3-GP
OC6#_GPIO10 — BT45 — USB_OC6_R_N — R492 10KR2J-3-GP — USB_OC_1213*
OC7#_GPIO14 — BM45 — USB_OC7_R_N — R488 10KR2J-3-GP — +3V

OC[0..3] for Ports 0-7
OC[4..7] for Ports 8-13

USBRBIAS — BP25 — USBRBIAS_PCH — R465 22D6R2F-L1-GP
BM25

USBRBIAS (R63LB): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

CLKIN_DOT_96N — BD38 — CK_96M_DREF_DN
CLKIN_DOT_96P — BF38 — CK_96M_DREF_DP

DMI2RBIAS — A32 — RBIAS_CPY — R476 750R2F-GP

RBIAS_PHY (R211LB): TIE TRACES TOGETHER CLOSE TO PINS, WITH LENGTH NO LONGER THAN 450 MILS TO RESISTOR

PCIE:
HSI_DN2 — J20 — PERN1
HSI_DP2 — L20 — PERP1
HSO_DN2 — F25 — PETN1
HSO_DP2 — F23 — PETP1
HSI_DN3 — P20 — PERN2
HSI_DP3 — R20 — PERP2
HSO_DN3 — C22 — PETN2
HSO_DP3 — A22 — PETP2
HSI_DN4 — H17 — PERN3
HSI_DP4 — J17 — PERP3
HSO_DN4 — E21 — PETN3
HSO_DP4 — B21 — PETP3
HSI_LAN_DN1 — P17 — PERN4
HSI_LAN_DP1 — M17 — PERP4
HSO_LAN_DN1 — F18 — PETN4
HSO_LAN_DP1 — E17 — PETP4
N15 — PERN5
M15 — PERP5
B17 — PETN5
C16 — PETP5
J15 — PERN6
L15 — PERP6
A16 — PETN6
B15 — PETP6
J12 — PERN7
H12 — PERP7
F15 — PETN7
E13 — PETP7
H10 — PERN8
J10 — PERP8
B13 — PETN8
D13 — PETP8

FOR PCIEX1: HSO_C_DN2 C219 — HSO_C_DP2 C220 — SCD1U10V2KX-4GP
FOR PCIEX1: HSO_C_DN3 C205 — HSO_C_DP3 C206 — SCD1U10V2KX-4GP
FOR PCIEX1: HSO_C_DN4 C211 — HSO_C_DP4 C210 — SCD1U10V2KX-4GP
FOR LAN: HSO_C_LAN_DN1 C143 — HSO_C_LAN_DP1 C141 — SCD1U10V2KX-4GP

2010/09/28
Change LAN from PCIE Port1 to PCIE Port5
due to disable PCIE Port 1 will also disable all ports

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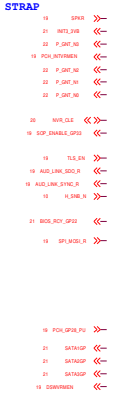
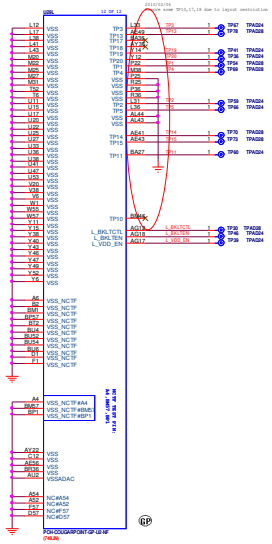
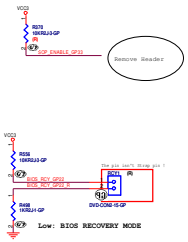
STRAP

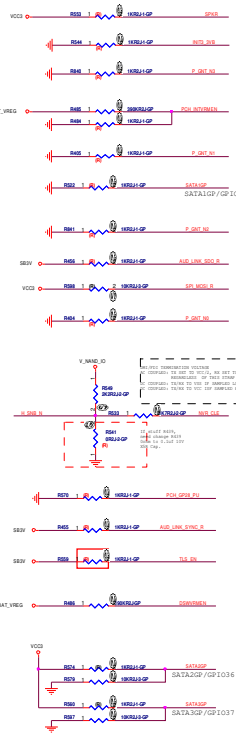




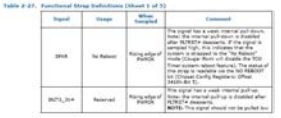


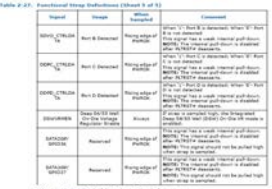
PCH Functional Straps

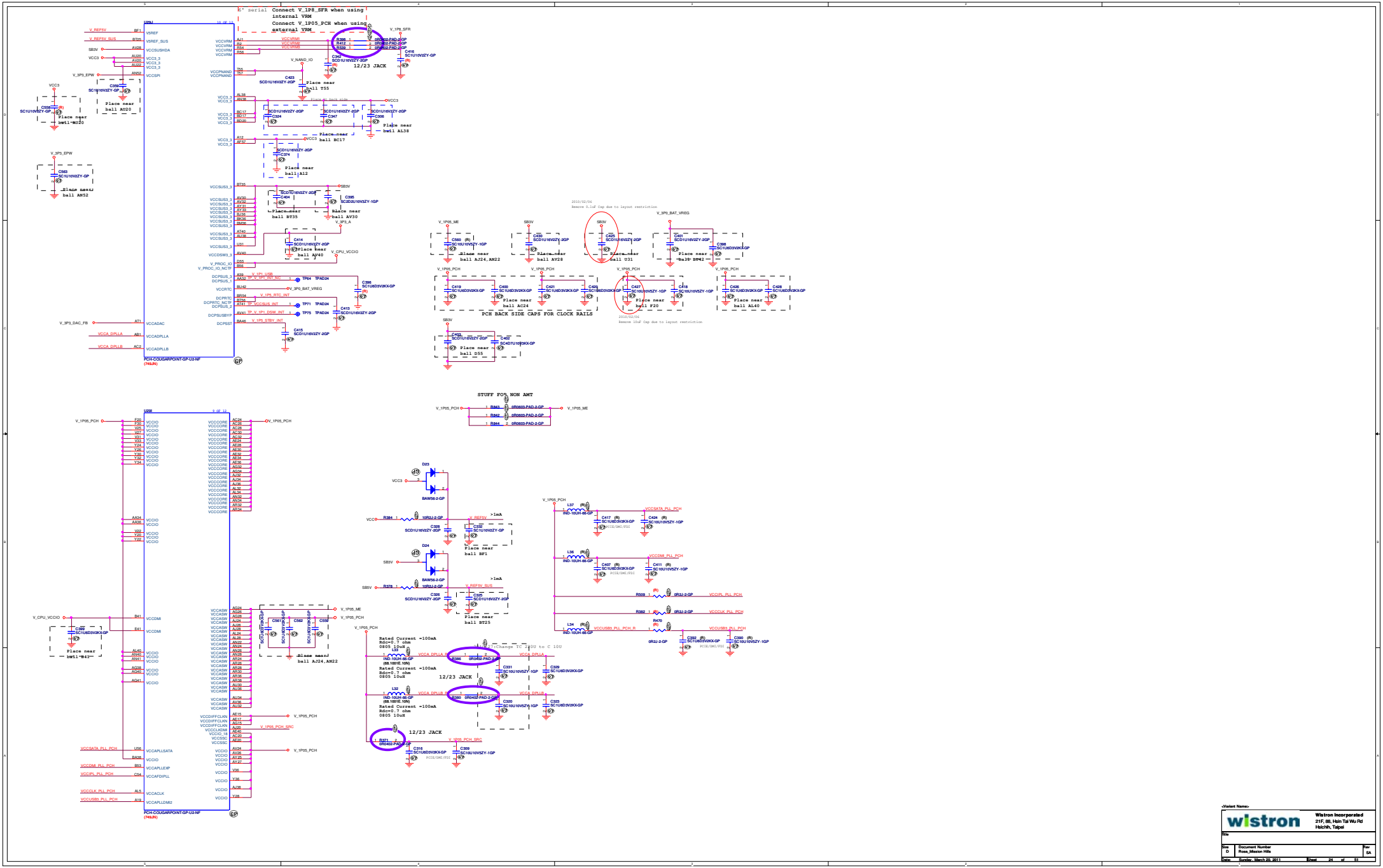
BOOT DEVICE	GNT1	SATA1GP /GPIO19
SPI	1	1
PCI	1	0
FWH	0	0



6' serial straping define







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SATA

21 SATAHDR_RX_DP0
21 SATAHDR_RX_DN0

21 SATAHDR_TX_DN0
21 SATAHDR_TX_DP0

21 SATAHDR_RX_DP1
21 SATAHDR_RX_DN1

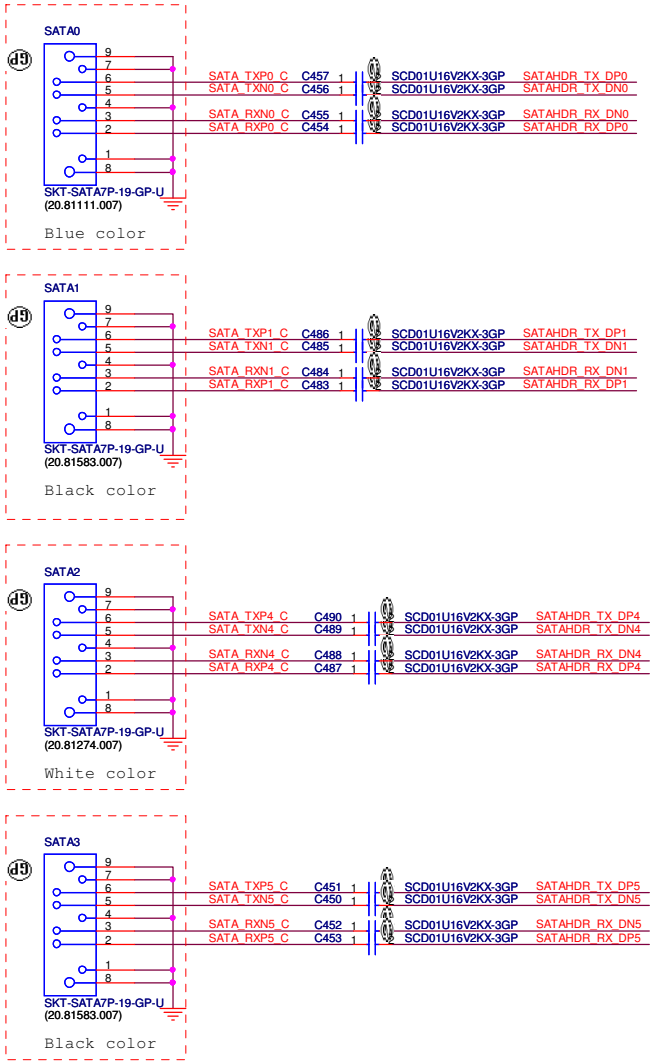
21 SATAHDR_TX_DN1
21 SATAHDR_TX_DP1

21 SATAHDR_RX_DP4
21 SATAHDR_RX_DN4

21 SATAHDR_TX_DN4
21 SATAHDR_TX_DP4

21 SATAHDR_RX_DP5
21 SATAHDR_RX_DN5

21 SATAHDR_TX_DN5
21 SATAHDR_TX_DP5



NOTE:
PCH only port 0&1 support SATA 3.0

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PCIEX16

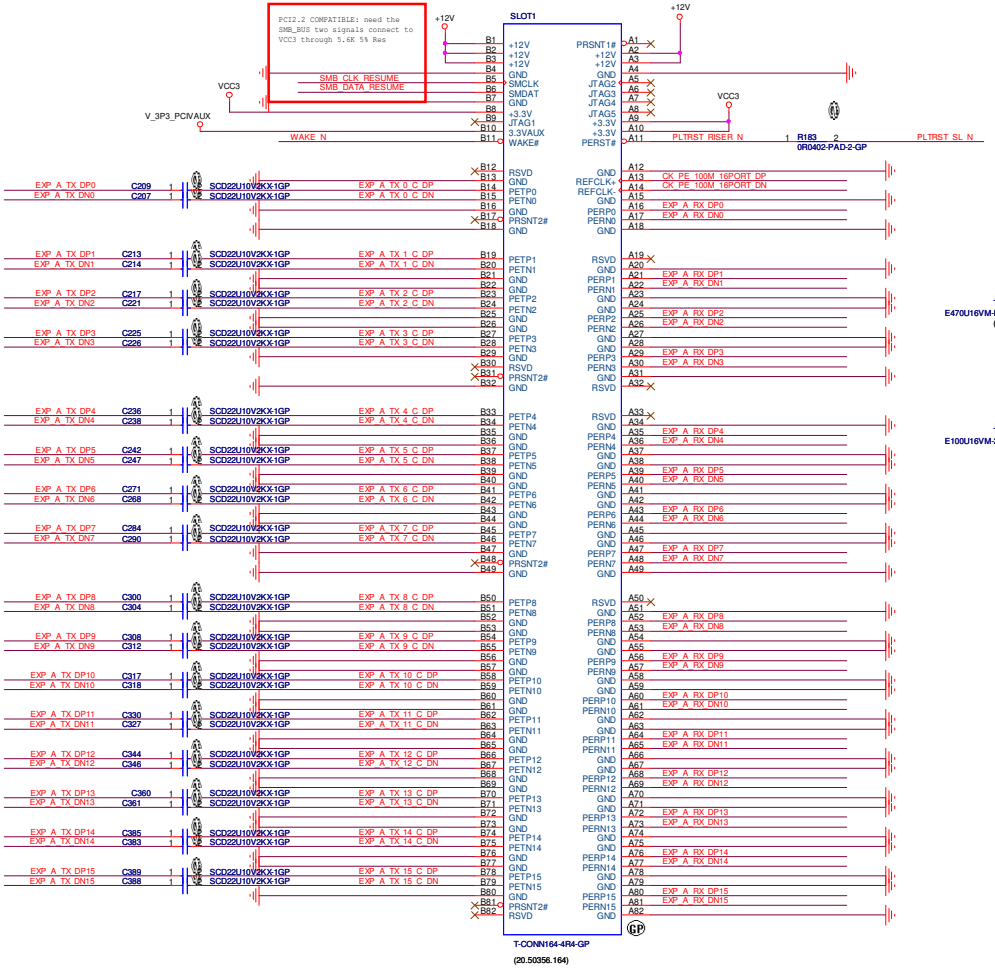
11 EXP_A_RX_DN[0..15]
11 EXP_A_RX_DP[0..15]
11 EXP_A_TX_DP[0..15]
11 EXP_A_TX_DN[0..15]
20 CK_PE_100M_16PORT_DP
20 CK_PE_100M_16PORT_DN
14,36 PLTRST_SL_N

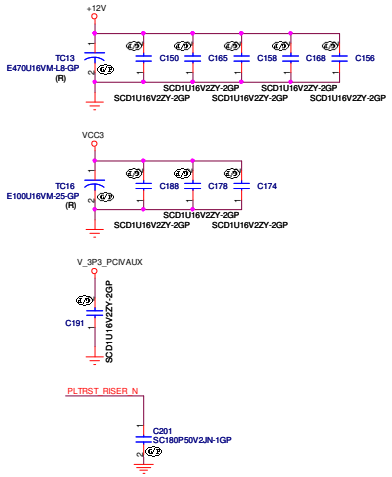
OTHERS

19,32,36,41 SMB_CLK_RESUME
19,32,36,41 SMB_DATA_RESUME
19,32,41 WAKE_N

w/o Latch: 20.50352.164
with Latch: 20.50512.164, 20.50356.164

PCIEx16 CONN may need LATCH if supporting 75W GFX Card





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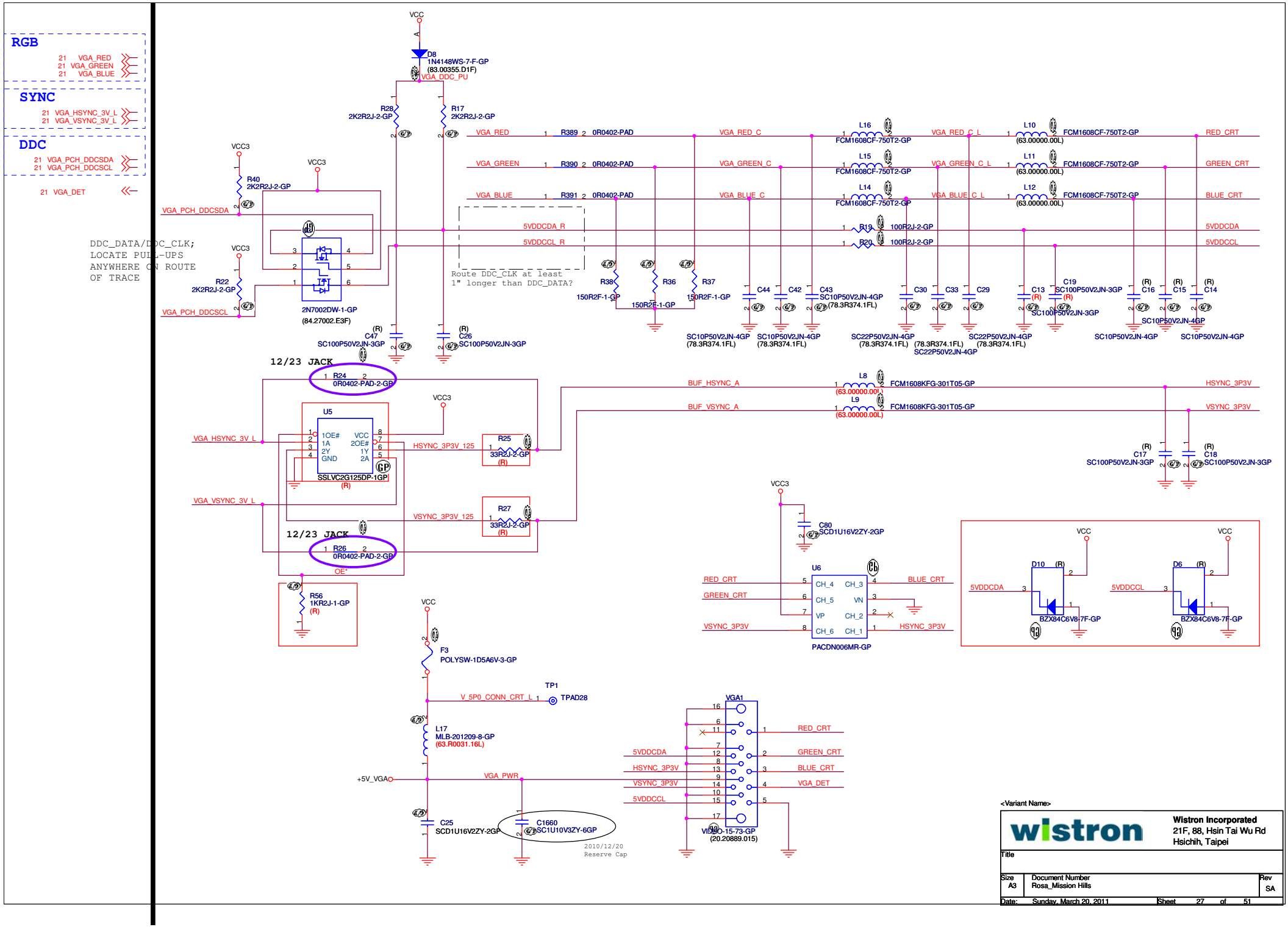
RGB
21 VGA_RED
21 VGA_GREEN
21 VGA_BLUE
SYNC
21 VGA_HSYNC_3V_L
21 VGA_VSYNC_3V_L
DDC
21 VGA_PCH_DDCSDA
21 VGA_PCH_DDCSCL
21 VGA_DET
DDC_DATA/DDC_CLK;
LOCATE PULL-UPS
ANYWHERE ON ROUTE
OF TRACE
VCC
D8
1N4148WS-7-F-GP
(83.00355.D1F)
VGA_DDC_PU
R28
2K2R2J-2-GP
R17
2K2R2J-2-GP
VGA_RED
R389 0R0402-PAD
VGA_GREEN
R390 0R0402-PAD
VGA_BLUE
R391 0R0402-PAD
VGA_RED_C
VGA_GREEN_C
VGA_BLUE_C
L16
FCM1608CF-750T2-GP
L15
FCM1608CF-750T2-GP
L14
FCM1608CF-750T2-GP
VGA_RED_C_L
VGA_GREEN_C_L
VGA_BLUE_C_L
L10
FCM1608CF-750T2-GP
(63.00000.00L)
L11
FCM1608CF-750T2-GP
(63.00000.00L)
L12
FCM1608CF-750T2-GP
(63.00000.00L)
RED_CRT
GREEN_CRT
BLUE_CRT
VCC3
R40
2K2R2J-2-GP
VGA_PCH_DDCSDA
VGA_PCH_DDCSCL
R22
2K2R2J-2-GP
2N7002DW-1-GP
(84.27002.E3F)
5VDDCDA_R
5VDDCCL_R
R19 100R2J-2-GP
R20 100R2J-2-GP
5VDDCDA
5VDDCCL
Route DDC_CLK at least
1" longer than DDC_DATA?
R38
150R2F-1-GP
R36
150R2F-1-GP
R37
150R2F-1-GP
C47
SC100P50V2JN-3GP
C26
SC100P50V2JN-3GP
C44
SC10P50V2JN-4GP
(78.3R374.1FL)
C42
SC10P50V2JN-4GP
(78.3R374.1FL)
C43
SC10P50V2JN-4GP
(78.3R374.1FL)
C30
SC22P50V2JN-4GP
(78.3R374.1FL)
C33
SC22P50V2JN-4GP
(78.3R374.1FL)
C29
SC22P50V2JN-4GP
(78.3R374.1FL)
C13
SC100P50V2JN-3GP
C19
SC100P50V2JN-3GP
C16
SC10P50V2JN-4GP
C15
SC10P50V2JN-4GP
C14
SC10P50V2JN-4GP
12/23 JACK
R24
0R0402-PAD-2-GP
U5
1OE#
1A
2Y
GND
VCC
2OE#
1Y
2A
SSLVC2G125DP-1GP
VGA_HSYNC_3V_L
VGA_VSYNC_3V_L
HSYNC_3P3V_125
VSYNC_3P3V_125
R25
33R2J-2-GP
R27
33R2J-2-GP
12/23 JACK
R26
0R0402-PAD-2-GP
OE*
R56
1KR2J-1-GP
BUF_HSYNC_A
BUF_VSYNC_A
L8
FCM1608KFG-301T05-GP
(63.00000.00L)
L9
FCM1608KFG-301T05-GP
(63.00000.00L)
HSYNC_3P3V
VSYNC_3P3V
C17
SC100P50V2JN-3GP
C18
SC100P50V2JN-3GP
C80
SCD1U16V2ZY-2GP
U6
CH_4
CH_5
VP
CH_6
CH_3
VN
CH_2
CH_1
PACDN006MR-GP
RED_CRT
GREEN_CRT
VSYNC_3P3V
BLUE_CRT
HSYNC_3P3V
D10
BZX84C6V8-7F-GP
D6
BZX84C6V8-7F-GP
5VDDCDA
5VDDCCL
F3
POLYSW-1D5A6V-3-GP
TP1
TPAD28
V_5P0_CONN_CRT_L
L17
MLB-201209-8-GP
(63.R0031.16L)
+5V_VGA
VGA_PWR
C25
SCD1U16V2ZY-2GP
C1660
SC1U10V3ZY-6GP
2010/12/20
Reserve Cap
VGA1
VIDEO-15-73-GP
(20.20889.015)
VGA_DET
<Variant Name>
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DVI PORT

21 DDSP_D_TX DP_0
21 DDSP_D_TX DN_0
21 DDSP_D_TX DP_1
21 DDSP_D_TX DN_1
21 DDSP_D_TX DP_2
21 DDSP_D_TX DN_2
21 DDSP_D_TX DP_3
21 DDSP_D_TX DN_3
21 DDPD_CTRL_CLK
21 DDPD_CTRL_DATA
21 DDSP_D_HPD

PCH PORT D Place near HDMI Connector

DDSP_D_TX DP_0 — C90 — SCD1U10V2KX-4GP — HDMI LANE0_DP_C
DDSP_D_TX DN_0 — C91 — SCD1U10V2KX-4GP — HDMI LANE0_DN_C
DDSP_D_TX DP_1 — C84 — SCD1U10V2KX-4GP — HDMI LANE1_DP_C
DDSP_D_TX DN_1 — C95 — SCD1U10V2KX-4GP — HDMI LANE1_DN_C
DDSP_D_TX DP_2 — C88 — SCD1U10V2KX-4GP — HDMI LANE2_DP_C
DDSP_D_TX DN_2 — C89 — SCD1U10V2KX-4GP — HDMI LANE2_DN_C
DDSP_D_TX DP_3 — C92 — SCD1U10V2KX-4GP — HDMI LANE3_DP_C
DDSP_D_TX DN_3 — C93 — SCD1U10V2KX-4GP — HDMI LANE3_DN_C

R73 680R2J-3-GP — R74 680R2J-3-GP — R78 680R2J-3-GP — R79 680R2J-3-GP — R72 680R2J-3-GP — R75 680R2J-3-GP — R76 680R2J-3-GP — R77 680R2J-3-GP

DDSP_D_TX_N1 — R39 0R0805-PAD — DDSP_D_TX_N0

12/23 JACK

VCC3 — R66 100KR2J-1-GP — DDSP_D_TX_N2 — Q2 2N7002-11-GP (84.2N702.E31)

ESD

VCC — D11 1N4148WS-7-F-GP (R)

U3 (R) IP4220CZ6-GP
HDMI_LANE2_DN — ESD I/O4 — ESD I/O1 — HDMI_LANE2_DP
HDMI_ESD_PWR — VP — GND
HDMI_LANE3_DP — ESD I/O3 — ESD I/O2 — HDMI_LANE3_DN
C50 SCD1U16V2ZY-2GP (R)

U9 (R) IP4220CZ6-GP
DDPD_CTRL_CLK_CONN — ESD I/O4 — ESD I/O1 — DDPD_CTRL_DATA_CONN
HDMI_ESD_PWR — VP — GND
ESD I/O3 — ESD I/O2 — DDSP_D_HPD_CONN
C74 SCD1U16V2ZY-2GP (R)

U4 (R) IP4220CZ6-GP
HDMI_LANE0_DN — ESD I/O4 — ESD I/O1 — HDMI_LANE0_DP
HDMI_ESD_PWR — VP — GND
HDMI_LANE1_DP — ESD I/O3 — ESD I/O2 — HDMI_LANE1_DN
C36 SCD1U16V2ZY-2GP (R)

AOS 83.08900.0AE
NXP 83.42236.0AE
ON 83.04201.AA0

VCC3 — R102 2K2R2J-2-GP — R89 2K2R2J-2-GP — DDPD_CTRL_CLK
VCC3 — DDPD_CTRL_DATA
U11 2N7002DW-1-GP (84.27002.E3F)

VCC — D13 1N4148WS-7-F-GP (83.00355.D1F) — VCC5_DDC_HDMI
R101 2K2R2J-2-GP — R96 2K2R2J-2-GP — C118 SCD1U16V2ZY-2GP
For HDMI Logo Test

DDPD_CTRL_CLK_CONN
DDPD_CTRL_DATA_CONN
Route DDC_DATA at least 1" longer than DDC_CLK

C81 SC470P50V2KX-3GP (R)
C108 SC470P50V2KX-3GP (R)

VCC3 — R91 1MR2J-1-GP (R) — BSS138-8-GP — Q6 — DDSP_D_HPD — DDSP_D_HPD_CONN — R30 20KR2J-L2-GP

EMI

HDMI_LANE0_DP — C67 SC3D3P50V2CN-GP (R) — HDMI_LANE0_DN — C68 SC3D3P50V2CN-GP (R)
HDMI_LANE1_DP — C65 SC3D3P50V2CN-GP (R) — HDMI_LANE1_DN — C66 SC3D3P50V2CN-GP (R)
HDMI_LANE2_DP — C69 SC3D3P50V2CN-GP (R) — HDMI_LANE2_DN — C70 SC3D3P50V2CN-GP (R)
HDMI_LANE3_DP — C71 SC3D3P50V2CN-GP (R) — HDMI_LANE3_DN — C72 SC3D3P50V2CN-GP (R)

VCC — Need Check Fuse value ? — F2 PCLYSW-1D5A6V-2-GP — V_5P0_HDMI_CONN_L — L5 0R0805-PAD — C49 SCD1U16V2ZY-2GP — C3 SCD1U16V2ZY-2GP
2011/01/23 Change to 0ohm Pad

HDMI1 SKT-HDMI19P-4GP-U1 (62.10078.641)
HDMI_LANE0_DP — 1
HDMI_LANE0_DN — 2
HDMI_LANE1_DP — 4
HDMI_LANE1_DN — 5
HDMI_LANE2_DP — 7
HDMI_LANE2_DN — 8
HDMI_LANE3_DP — 10
HDMI_LANE3_DN — 11
DDPD_CTRL_CLK_CONN — 14
DDPD_CTRL_DATA_CONN — 15
V_5P0_HDMI_CONN — 18
DDSP_D_HPD_CONN — 19
20, 21, 22, 23

w Screw: 62.10078.101
w/o Screw: 62.10078.641

R61 0R2J-2-GP-DUMMY (R) — HDMI_LANE2_DP_C — HDMI_LANE2_DP
TR3 ACM2012H-900-GP-DUMMY (69.10103.071)
HDMI_LANE2_DN_C — HDMI_LANE2_DN
R62 0R2J-2-GP-DUMMY (R)

R59 0R2J-2-GP-DUMMY (R) — HDMI_LANE1_DP_C — HDMI_LANE1_DP
TR2 ACM2012H-900-GP-DUMMY (69.10103.071)
HDMI_LANE1_DN_C — HDMI_LANE1_DN
R60 0R2J-2-GP-DUMMY (R)

R58 0R2J-2-GP-DUMMY (R) — HDMI_LANE0_DP_C — HDMI_LANE0_DP
TR1 ACM2012H-900-GP-DUMMY (69.10103.071)
HDMI_LANE0_DN_C — HDMI_LANE0_DN
R57 0R2J-2-GP-DUMMY (R)

R64 0R2J-2-GP-DUMMY (R) — HDMI_LANE3_DP_C — HDMI_LANE3_DP
TR4 ACM2012H-900-GP-DUMMY (69.10103.071)
HDMI_LANE3_DN_C — HDMI_LANE3_DN
R65 0R2J-2-GP-DUMMY (R)

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DISPLAY PORT

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Title

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FRONT USB

22 USB_PCH_DP0
22 USB_PCH_DN0
22 USB_PCH_DP1
22 USB_PCH_DN1

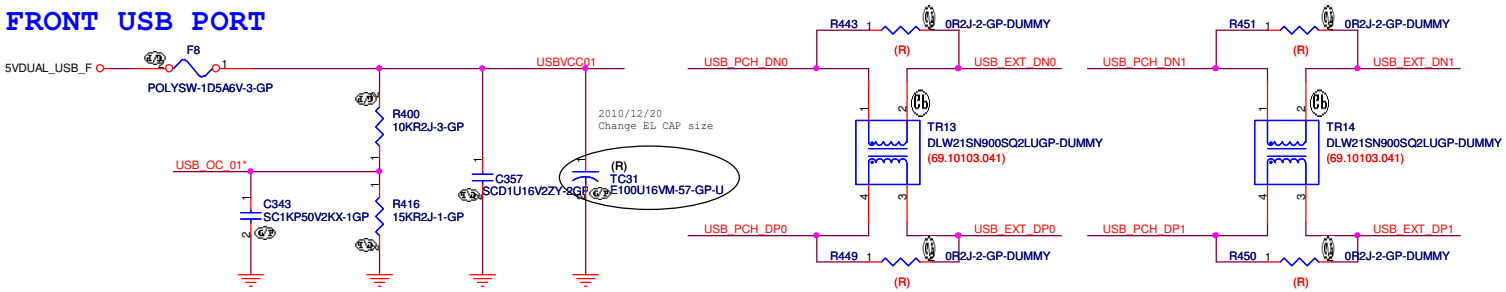
22 USB_OC_01*
21 FB_USBF1_DET

22 USB_PCH_DP2
22 USB_PCH_DN2
22 USB_PCH_DP3
22 USB_PCH_DN3

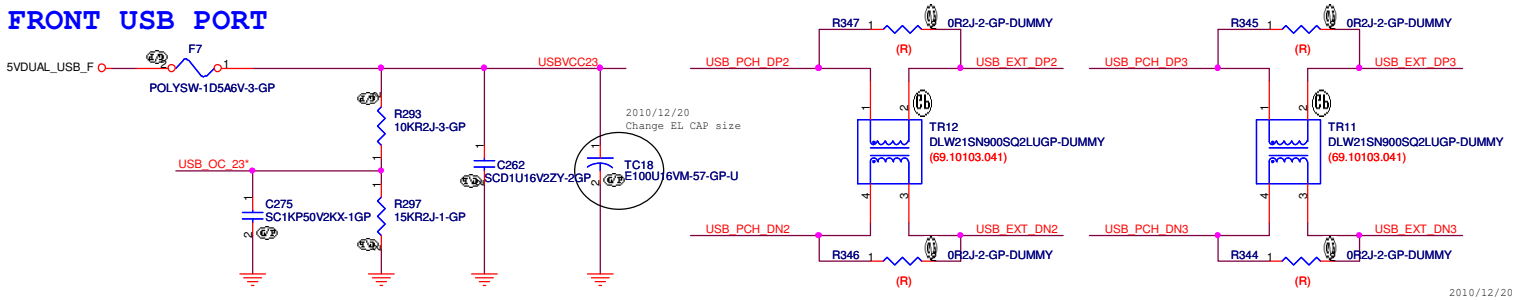
22 USB_OC_23*
21 FB_USBF2_DET

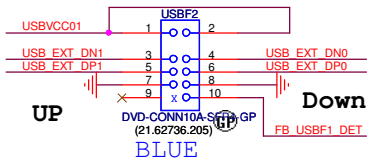
22,31 USB_PCH_DN10
22,31 USB_PCH_DP10
22,31 USB_PCH_DN11
22,31 USB_PCH_DP11

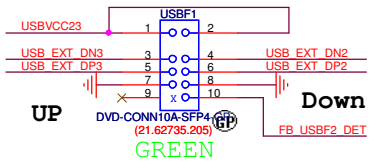
FRONT USB PORT

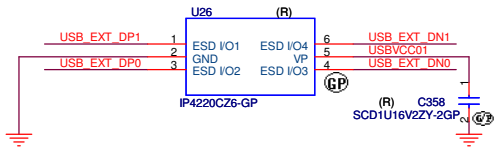


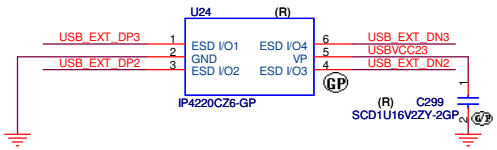
FRONT USB PORT

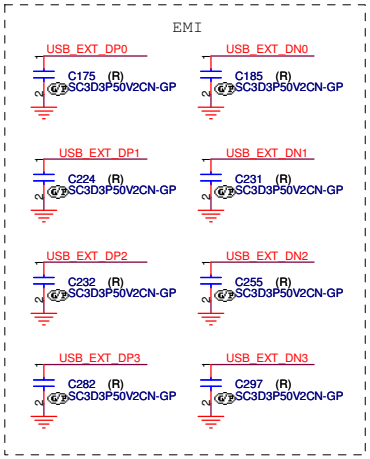












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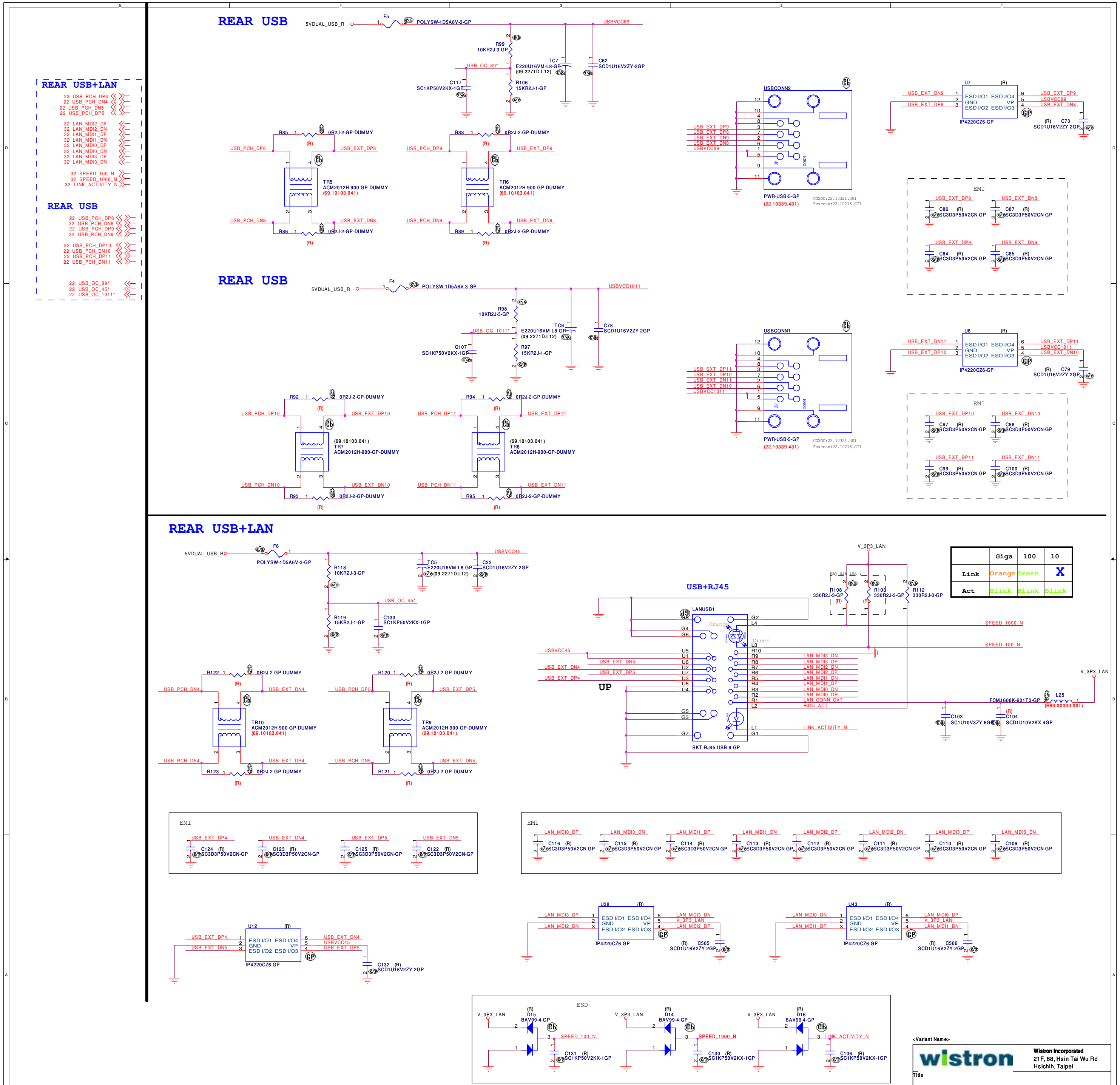

	Giga	100	10
Link	Orange	Green	X
Act	Blink	Blink	Blink

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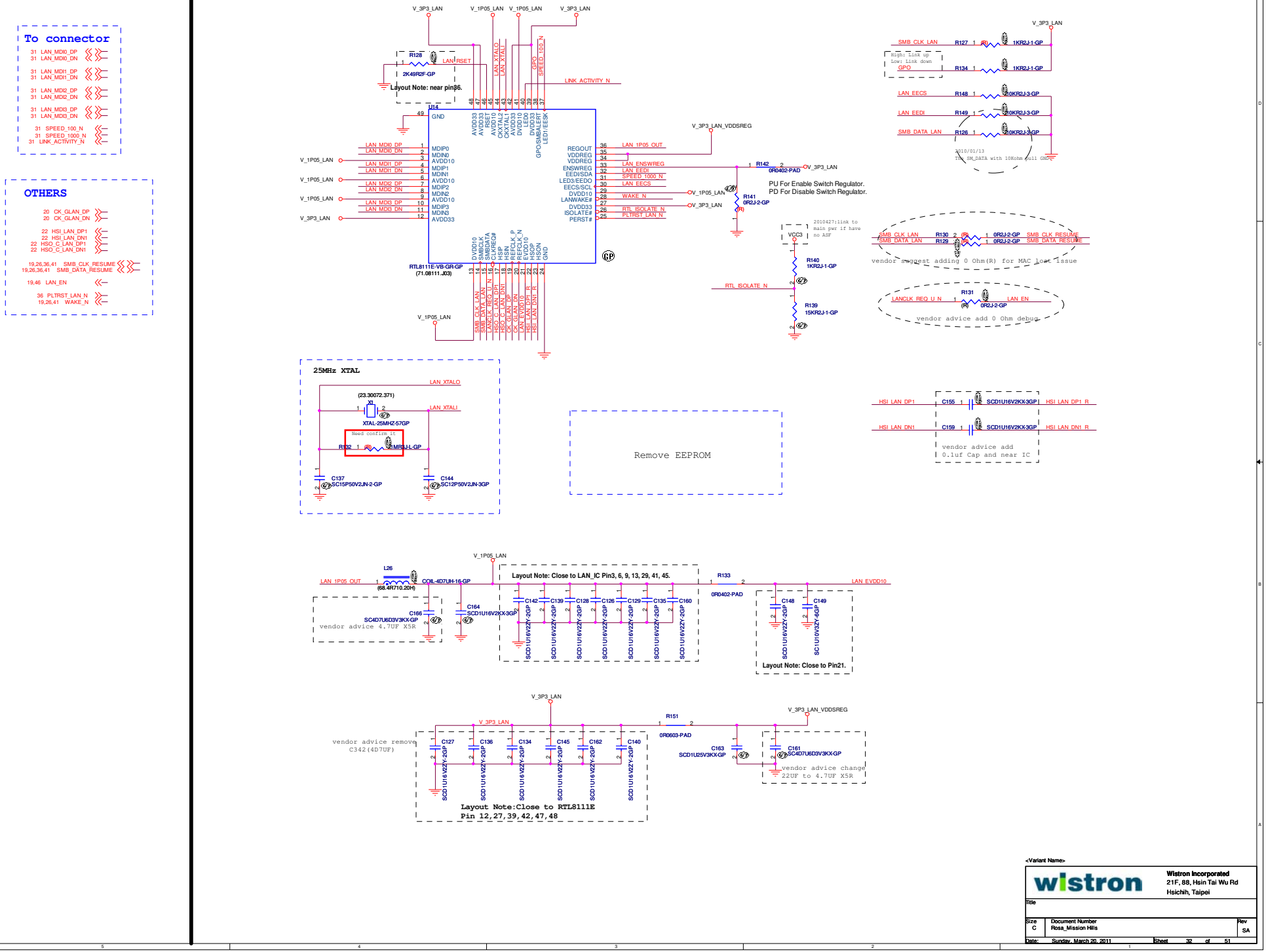
To connector
31 LAN_MDI0_DP
31 LAN_MDI0_DN
31 LAN_MDI1_DP
31 LAN_MDI1_DN
31 LAN_MDI2_DP
31 LAN_MDI2_DN
31 LAN_MDI3_DP
31 LAN_MDI3_DN
31 SPEED_100_N
31 SPEED_1000_N
31 LINK_ACTIVITY_N
OTHERS
20 CK_GLAN_DP
20 CK_GLAN_DN
22 HSI_LAN_DP1
22 HSI_LAN_DN1
22 HSO_C_LAN_DP1
22 HSO_C_LAN_DN1
19,26,36,41 SMB_CLK_RESUME
19,26,36,41 SMB_DATA_RESUME
19,46 LAN_EN
36 PLTRST_LAN_N
19,26,41 WAKE_N
V_3P3_LAN
V_1P05_LAN
V_3P3_LAN_VDDSREG
R128 2K49R2F-GP
Layout Note: near pin36.
U14
RTL8111E-VB-GR-GP
(71.08111.J03)
LINK_ACTIVITY_N
LAN_1P05_OUT
LAN_ENSWREG
LAN_EEDI
SPEED_1000_N
LAN_EECS
WAKE_N
RTL_ISOLATE_N
PLTRST_LAN_N
R142 0R0402-PAD
R141 0R2J-2-GP
PU For Enable Switch Regulator.
PD For Disable Switch Regulator.
2010427:link to main pwr if have no ASF
VCC3
R140 1KR2J-1-GP
R139 15KR2J-1-GP
SMB_CLK_LAN
SMB_DATA_LAN
R127 1KR2J-1-GP
R134 1KR2J-1-GP
High: Link up
Low: Link down
GPO
R148 10KR2J-3-GP
R149 10KR2J-3-GP
R126 10KR2J-3-GP
2010/01/13
TIE SM_DATA with 10Kohm pull GND
R130 0R2J-2-GP
R129 0R2J-2-GP
SMB_CLK_RESUME
SMB_DATA_RESUME
vendor suggest adding 0 Ohm(R) for MAC lost issue
LANCLK_REQ_U_N
R131 0R2J-2-GP
LAN_EN
vendor advice add 0 Ohm debug
25MHz XTAL
(23.30072.371)
XTAL-25MHZ-57GP
Need confirm it
R132 1MR0J-1-GP
C137 SC15P50V2JN-2-GP
C144 SC12P50V2JN-3GP
LAN_XTALO
LAN_XTALI
Remove EEPROM
HSI_LAN_DP1
HSI_LAN_DN1
C155 SCD1U16V2KX-3GP
C159 SCD1U16V2KX-3GP
HSI_LAN_DP1_R
HSI_LAN_DN1_R
vendor advice add 0.1uf Cap and near IC
L26 COIL-4D7UH-16-GP
(68.4R710.20H)
LAN_1P05_OUT
Layout Note: Close to LAN_IC Pin3, 6, 9, 13, 29, 41, 45.
C142 C139 C128 C126 C129 C135 C160
C166 SC4D7U6D3V3KX-GP
vendor advice 4.7UF X5R
C164 SCD1U16V2KX-3GP
R133 0R0402-PAD
LAN_EVDD10
C148 C149
Layout Note: Close to Pin21.
R151 0R0603-PAD
C127 C136 C134 C145 C162 C140
vendor advice remove C342(4D7UF)
C163 SCD1U25V3KX-GP
C161 SC4D7U6D3V3KX-GP
vendor advice change 22UF to 4.7UF X5R
Layout Note:Close to RTL8111E Pin 12,27,39,42,47,48
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HD_LINK

19 AUD_LINK_SDIN
19 AUD_LINK_SDO
19 AUD_LINK_RST_N
19 AUD_LINK_SYNC
19 AUD_LINK_BCLK

Rear I/O

LINE-OUT

34 LOUT_R
34 LOUT_L
34 LOUT_JD

LINE-IN

34 LIN_R
34 LIN_L
34 LIN_JD

MIC-IN

34 MIC_IN_R
34 MIC_IN_L
34 MIC_JD
34 MIC1_VREFO

Front I/O

HP-OUT

34 FP_OUT_L
34 FP_OUT_R
34 LINE2_JD

MIC-IN

34 FP_MIC2_R
34 FP_MIC2_L
34 MIC2_JD
34 MIC2_VREFO

Internal Speaker

34 SPK_D-
34 SPK_D+

Others

34 AUD_FRONT_SENSE
19 EXT_MUTE#
19 SPK_MUTE#

Pin 3: Digital Supply Voltage 3.3V

Pin 22: Charge Pump Input 3.3V

Pin 18: Class-D Supply 3.3V

To support Wake-On-Jack Functionality, DVDD_3.3 and VDD_IO should be powered from a power supply that is never removed

	CX20641/CX20651	
Line-in	pin34/35	Port E
Line-out	pin28/29	Port D
Mic-in-R	pin36/37	Port C
Mic-in-F	pin40/41	Port B
HP-out	pin26/27	Port A

	CX20641	CX20651
PIN 13	SPKR+	NC
PIN 15	SPKR-	NC
PIN 21	NC	PORT I

Connect GND and AGND under Codec

12/23 JACK

NEAR CODEC

NEAR CODEC

For EMI

Remove De-Pop Circuit

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Rear I/O

LINE-OUT
- 33 LOUT_R
- 33 LOUT_L
- 33 LOUT_JD

LINE-IN
- 33 LIN_R
- 33 LIN_L
- 33 LIN_JD

MIC-IN
- 33 MIC_IN_R
- 33 MIC_IN_L
- 33 MIC_JD
- 33 MIC1_VREFO

Front I/O

HP-OUT
- 33 FP_OUT_R
- 33 FP_OUT_L
- 33 LINE2_JD

MIC-IN
- 33 FP_MIC2_R
- 33 FP_MIC2_L
- 33 MIC2_JD
- 33 MIC2_VREFO

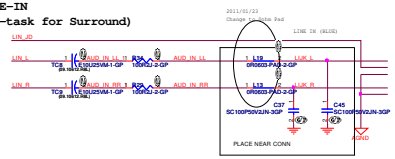
SPEAKER

- 33 SPK_D-
- 33 SPK_D+
- 19 SPK_DETECT

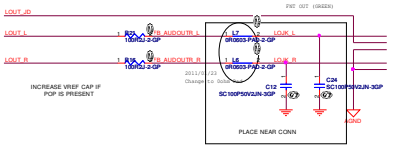
Others

- 33 AUD_FRONT_SENSE
- 21 FP_AUD_DETECT

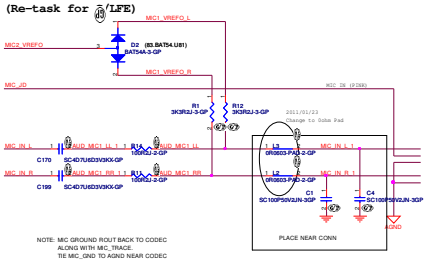
LINE-IN (Re-task for Surround)

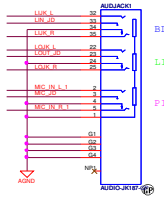


LINE-OUT



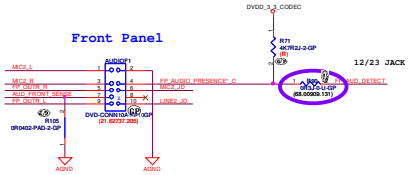
MIC-IN (Re-task for Mic/LFE)



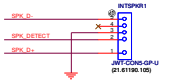


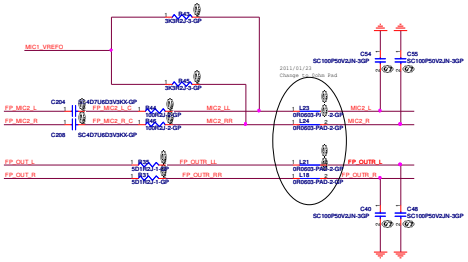
Line in (Surround)
Line Out
Mic (C/LFE)

Front Panel



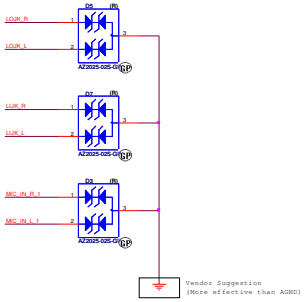
Internal Speaker





Remove Mute Circuit

ESD



<Variant Name>

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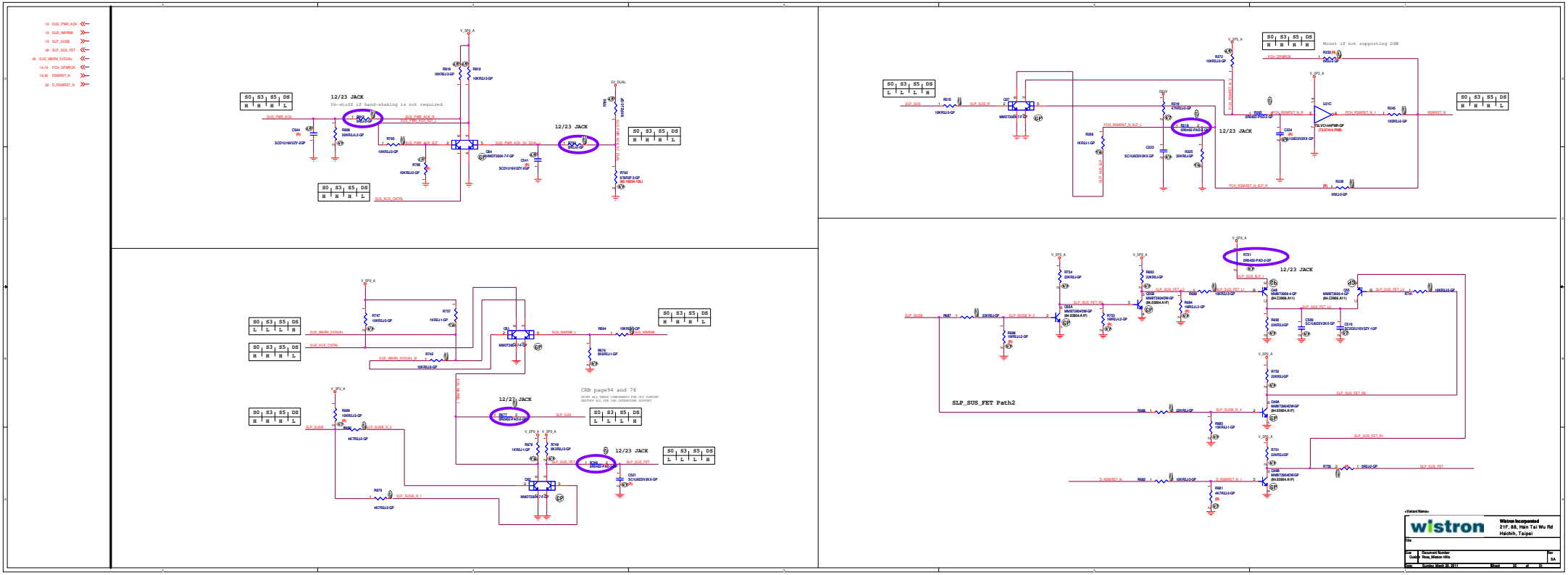

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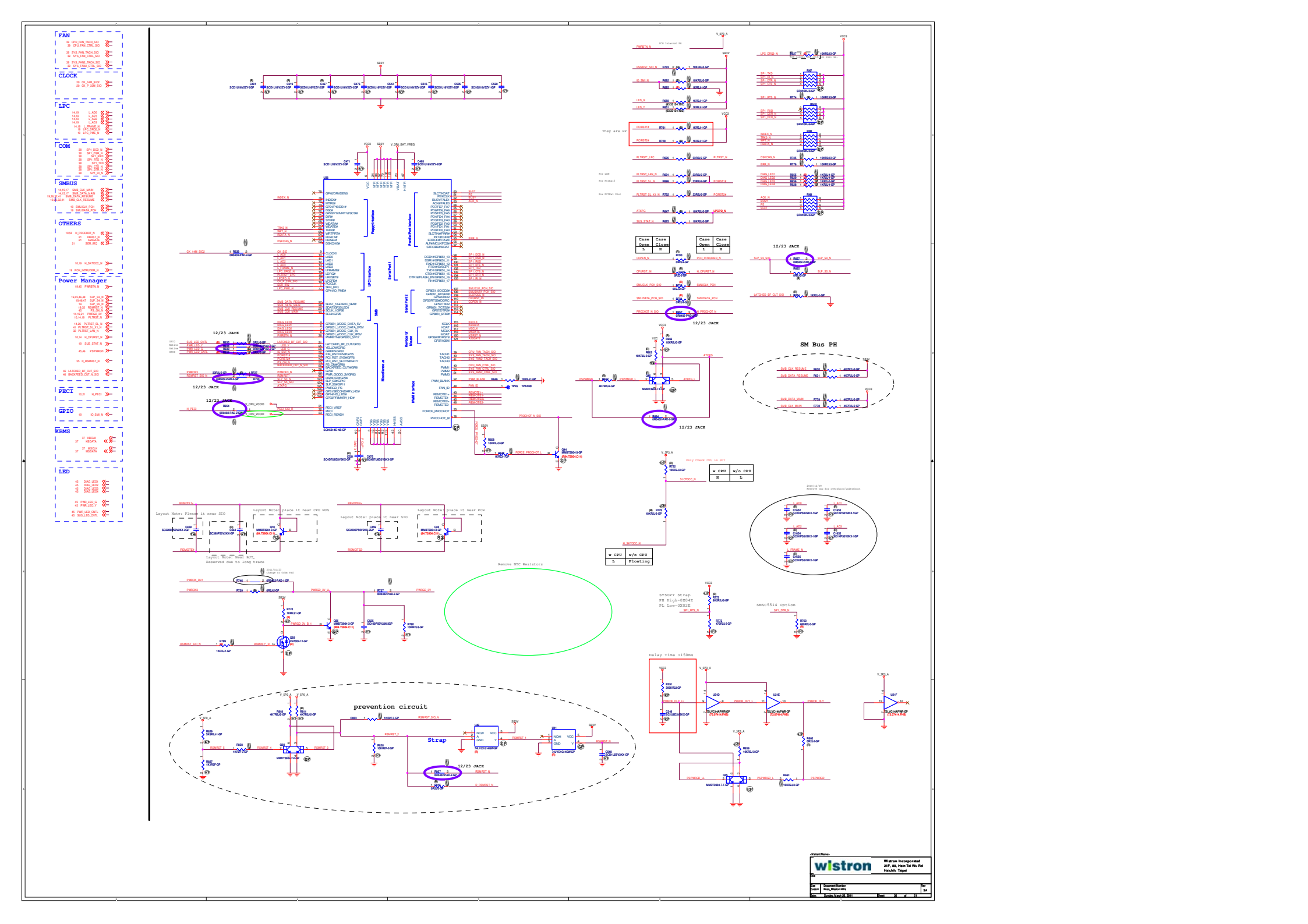
FAN
CLOCK
LPC
COM
SMBUS
OTHERS
Power Manager
PECI
GPIO
KBMS
LED
SCH5514E-NS-GP
prevention circuit
Strap
Delay Time >150ms
SM Bus PH
Remove NTC Resistors
SYSOPY Strap
PH High=0X04E
PL Low=0X02E
SMSC5514 Option
Only Check CPU in S0?
Layout Note: Place it near SIO
Layout Note: Place it near CPU MOS
Layout Note: Place it near PCH
Layout Note: Must BJT, Reserved due to long trace
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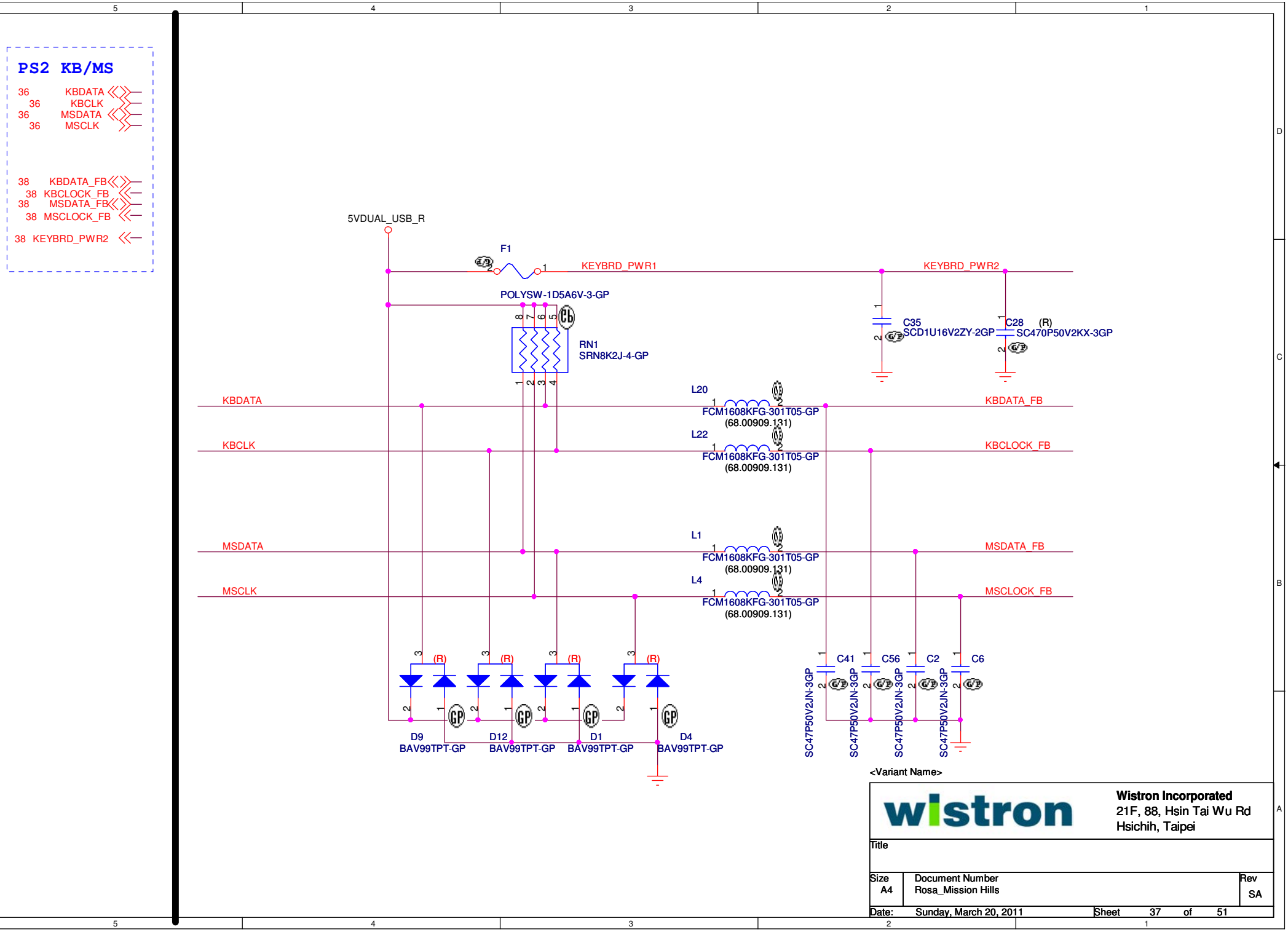
PS2 KB/MS
36 KBDATA
36 KBCLK
36 MSDATA
36 MSCLK
38 KBDATA_FB
38 KBCLOCK_FB
38 MSDATA_FB
38 MSCLOCK_FB
38 KEYBRD_PWR2
5VDUAL_USB_R
F1
POLYSW-1D5A6V-3-GP
KEYBRD_PWR1
KEYBRD_PWR2
RN1
SRN8K2J-4-GP
C35
SCD1U16V2ZY-2GP
C28 (R)
SC470P50V2KX-3GP
KBDATA
KBCLK
MSDATA
MSCLK
L20
FCM1608KFG-301T05-GP
(68.00909.131)
L22
FCM1608KFG-301T05-GP
(68.00909.131)
L1
FCM1608KFG-301T05-GP
(68.00909.131)
L4
FCM1608KFG-301T05-GP
(68.00909.131)
KBDATA_FB
KBCLOCK_FB
MSDATA_FB
MSCLOCK_FB
D9
BAV99TPT-GP
D12
BAV99TPT-GP
D1
BAV99TPT-GP
D4
BAV99TPT-GP
C41
C56
C2
C6
SC47P50V2JN-3GP
<Variant Name>
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COM Port

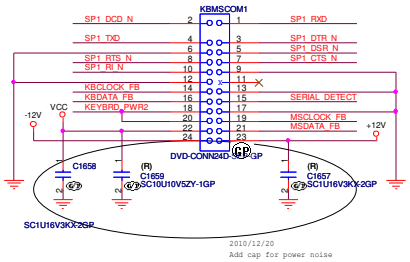
36 SP1_RTS_N
36 SP1_DTR_N
36 SP1_DSR_N
36 SP1_RXD
36 SP1_DCD_N
36 SP1_TXD
36 SP1_CTS_N
36 SP1_RI_N

21 SERIAL_DETECT

KB/MS

37 KBDATA_FB
37 KBCLOCK_FB
37 MSDATA_FB
37 MSCLOCK_FB

37 KEYBRD_PWR2



2010/12/20
Add cap for power noise

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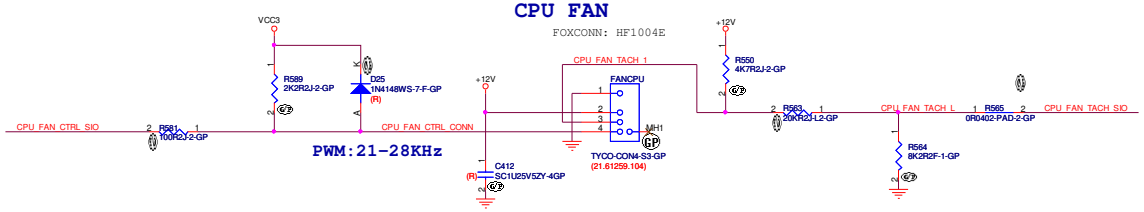
SIO FAN CONTROL

36 CPU_FAN_CTRL_SIO
36 CPU_FAN_TACH_SIO
36 SYS_FAN_CTRL_SIO
36 SYS_FAN_TACH_SIO
36 SYS_FAN2_CTRL_SIO
36 SYS_FAN2_TACH_SIO

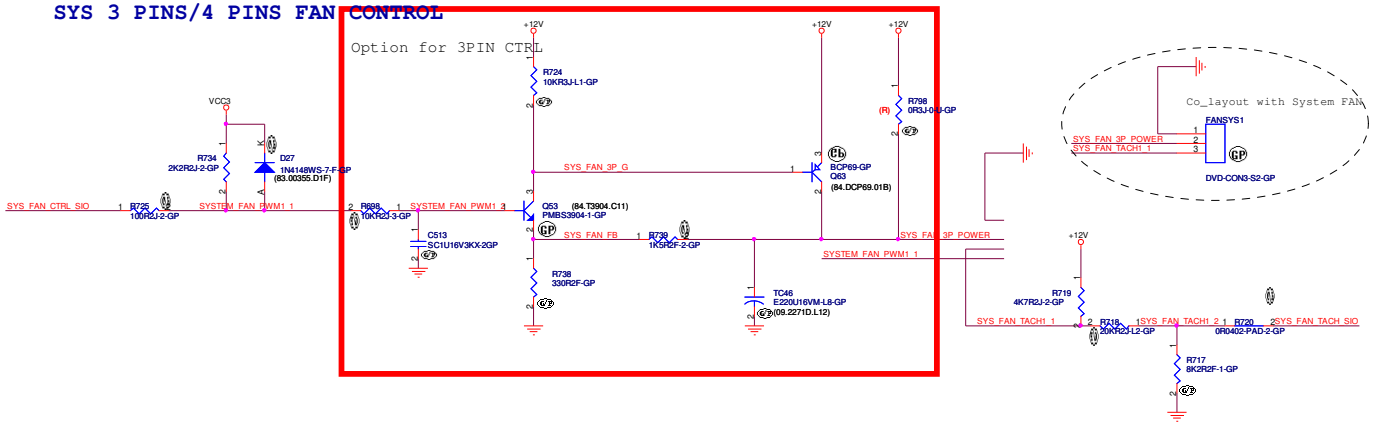
CPU FAN

FOXCONN: HF1004E



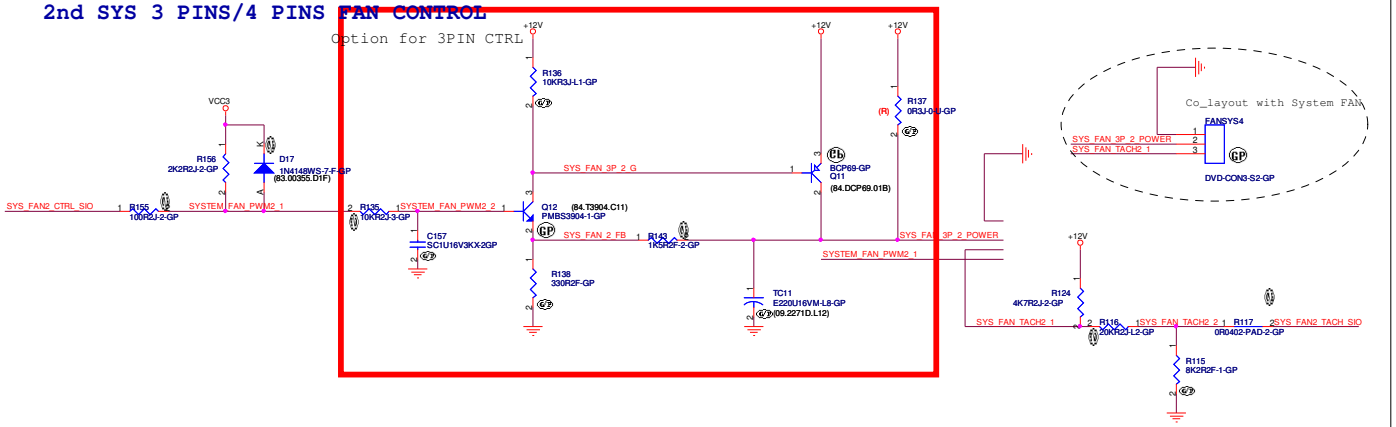
SYS 3 PINS/4 PINS FAN CONTROL

Option for 3PIN CTRL



2nd SYS 3 PINS/4 PINS FAN CONTROL

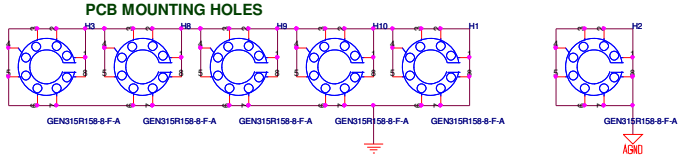
Option for 3PIN CTRL



PCB MOUNTING HOLES

Remove CPU Heatsink Screw Holes

CPU Heatsink screw hole.



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RESERVED

<Variant Name>

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ONFI

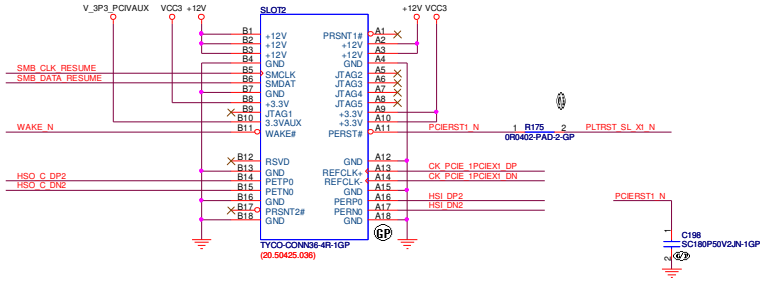
PCIEX1
22 HSO_C_DP2
22 HSO_C_DN2
22 HSI_DP2
22 HSI_DN2
20 CK_PCIE_1PCIEX1_DP
20 CK_PCIE_1PCIEX1_DN

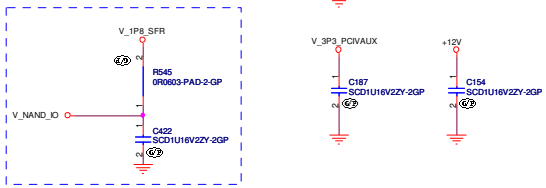
PCIEX1
22 HSO_C_DP3
22 HSO_C_DN3
22 HSI_DP3
22 HSI_DN3
20 CK_PCIE_2PCIEX1_DP
20 CK_PCIE_2PCIEX1_DN

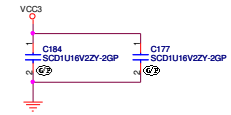
PCIEX1
22 HSO_C_DP4
22 HSO_C_DN4
22 HSI_DP4
22 HSI_DN4
20 CK_PCIE_3PCIEX1_DP
20 CK_PCIE_3PCIEX1_DN

Others
36 PLTRST_SL_X1_N
19,26,32,36 SMB_CLK_RESUME
19,26,32,36 SMB_DATA_RESUME
19,26,32 WAKE_N

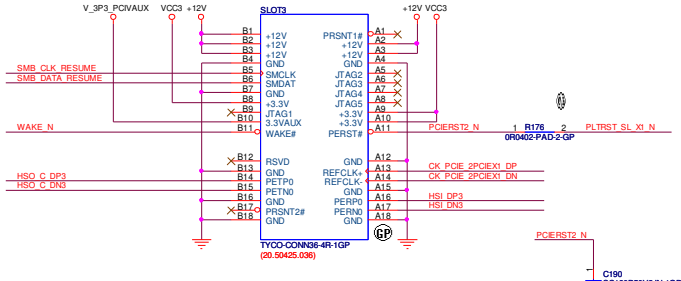
PCIEX1 CONN

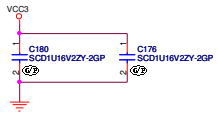


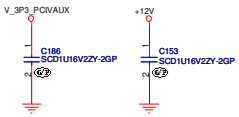




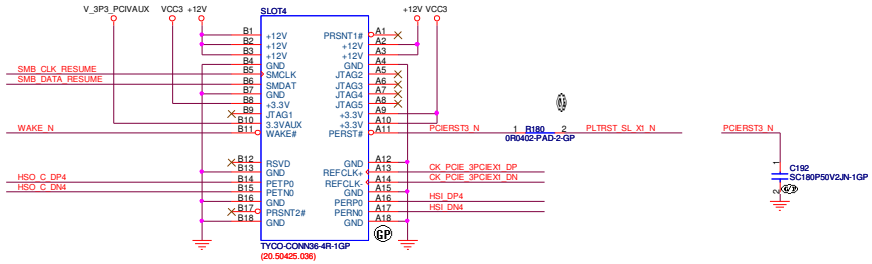
PCIEX1 CONN

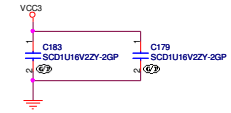


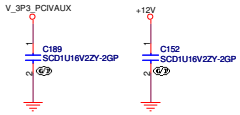




PCIEX1 CONN







<Variant Name>

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RESERVED

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RESERVED

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RESERVED

36 PS_ON_N
19,36,46,48 SLP_S3_N

21 PCH_SATA_LED_N
36,46 PSPWRGD
14,19 FP_RST_N
19,36 PWRBTN_N

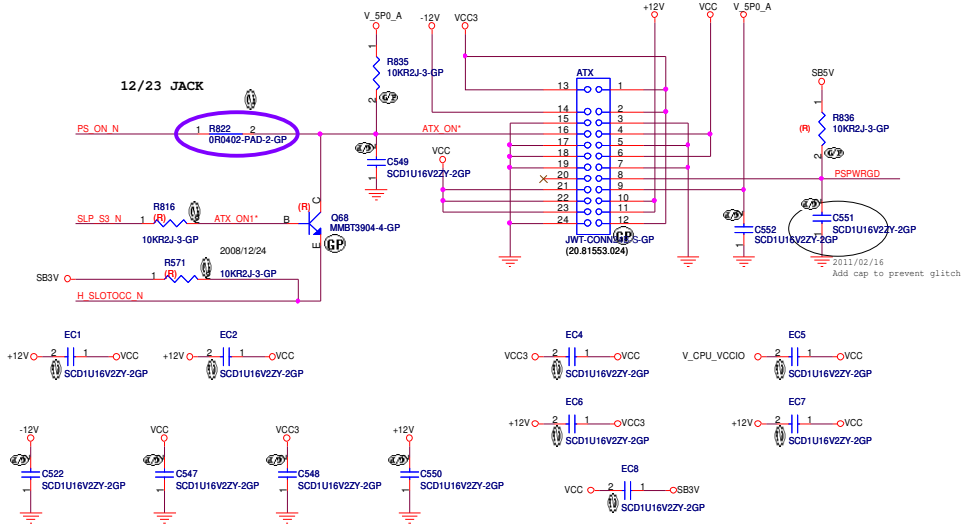
19 H_SLOTOCC_N
21 CHASSIS_ID_0
21 CHASSIS_ID_0
21 CHASSIS_ID_1
21 MTST_ID
21 FP_DETECT

36 PWR_LED_G
36 PWR_LED_Y

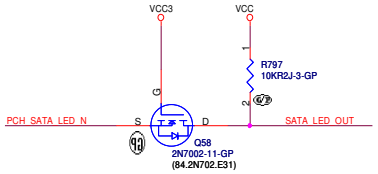
36 PWR_LED_CNTL
36 SUS_LED_CNTL

36 DIAG_LED1
36 DIAG_LED2
36 DIAG_LED3
36 DIAG_LED4

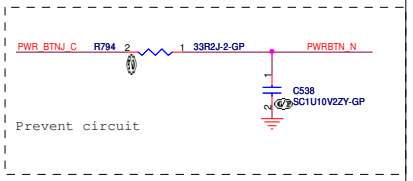
ATX CONNECTOR



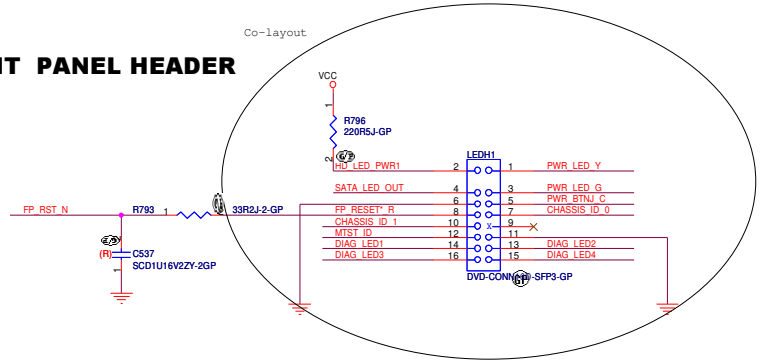
HDD LED

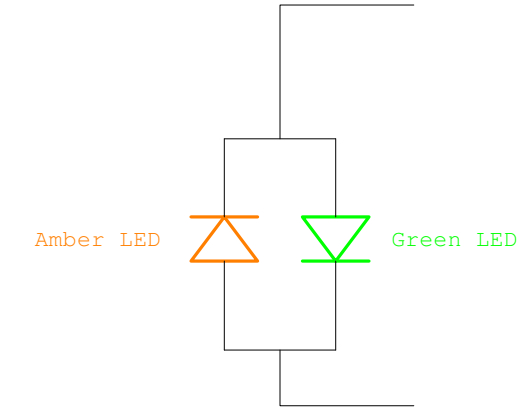


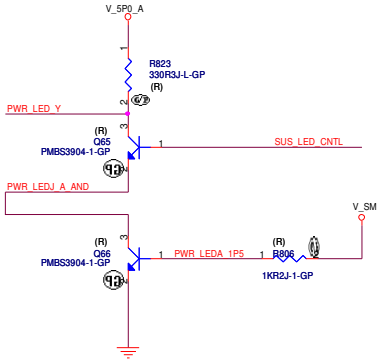
POWER BUTTON



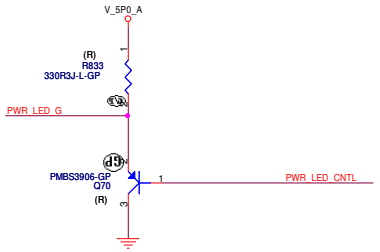
FRONT PANEL HEADER





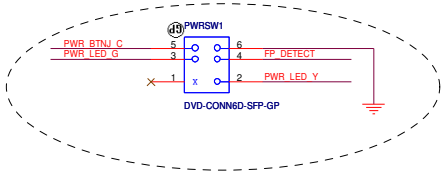


BIOS: Open-Drain
Default High, Output

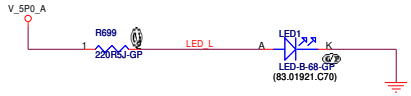


BIOS: Open-Drain
Default High, Output

2010/10/21
delete D29 diode



2010/10/28
Add PWRSW1 for Palm Beach



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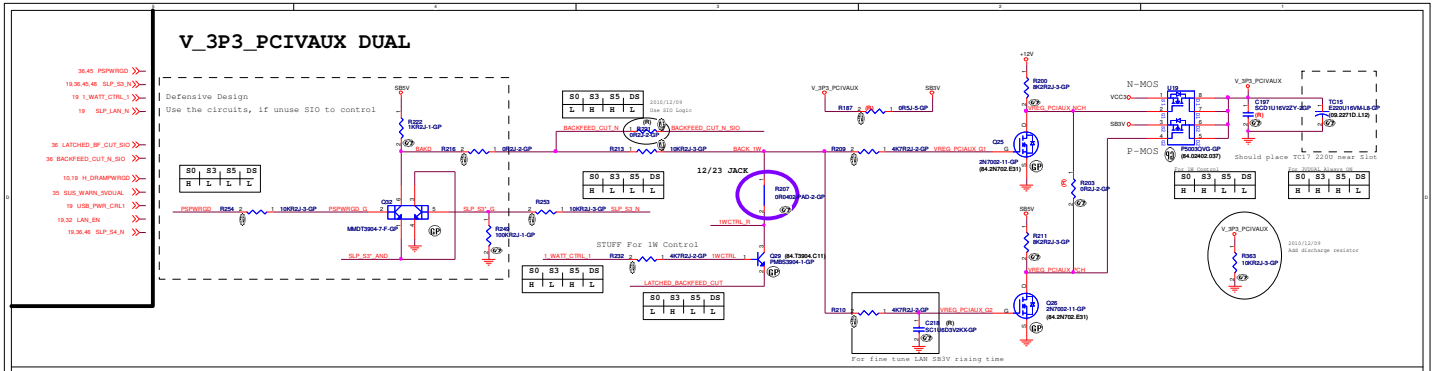
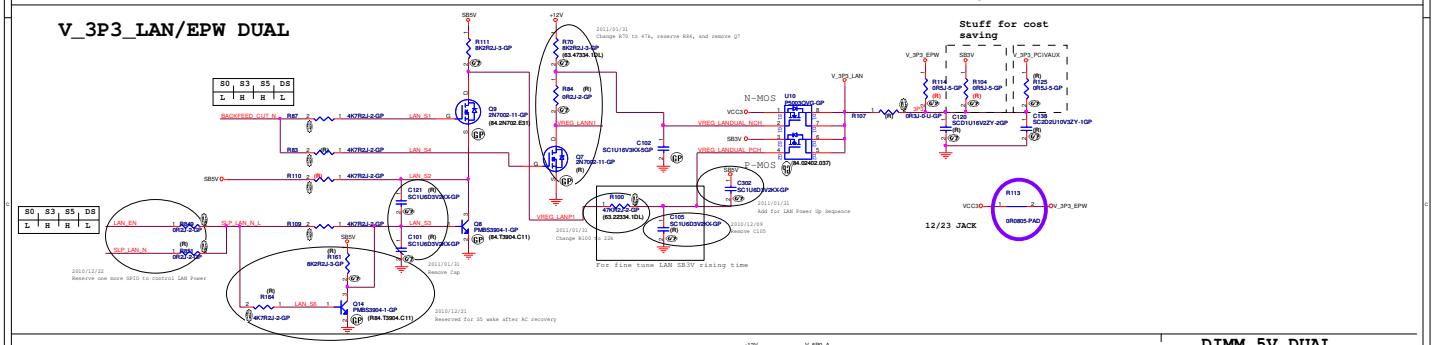
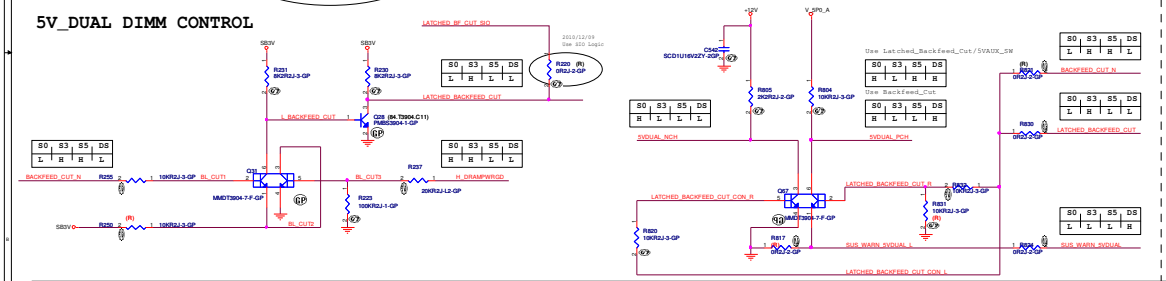
V_3P3_PCIVAUX DUAL



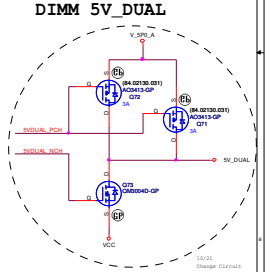
V_3P3_LAN/EPW DUAL



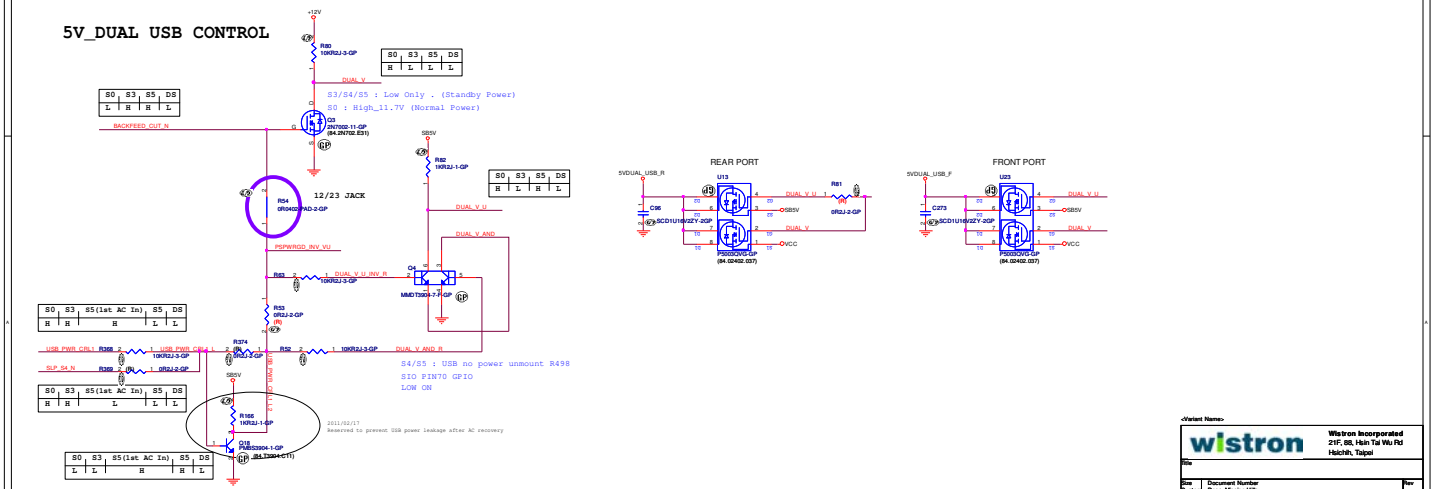
5V_DUAL DIMM CONTROL



DIMM 5V_DUAL



5V_DUAL USB CONTROL



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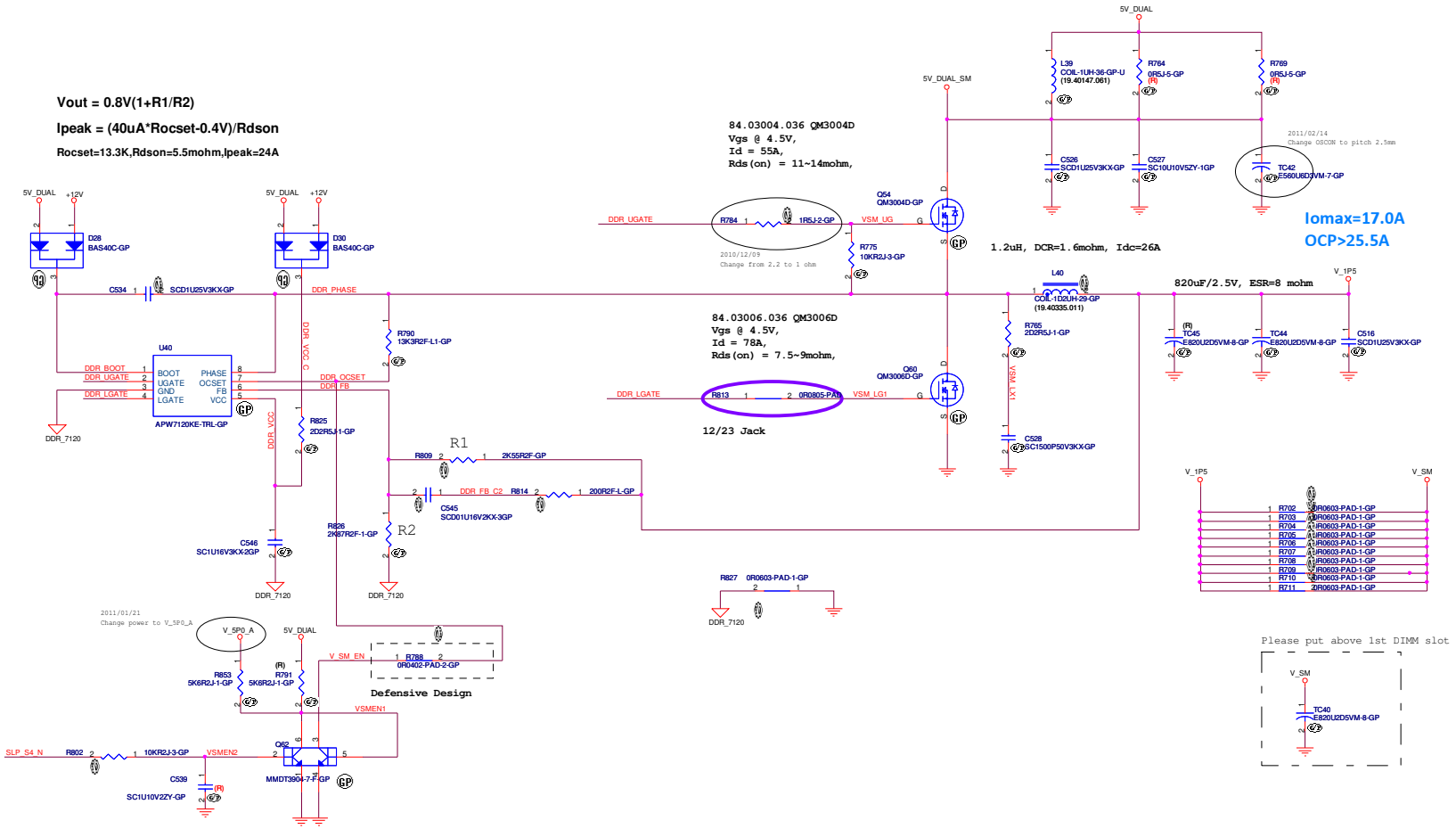
19,36,46 SLP_S4_N
19,36,45,46,48 SLP_S3_N

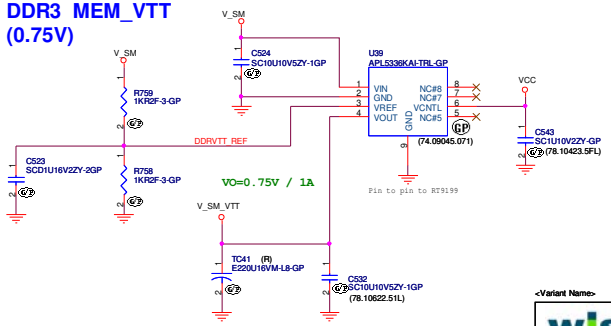
Vout = 0.8V(1+R1/R2)

Ipeak = (40uA*Rocset-0.4V)/Rdson

Rocset=13.3K,Rdson=5.5mohm,Ipeak=24A



DDR3 MEM_VTT (0.75V)



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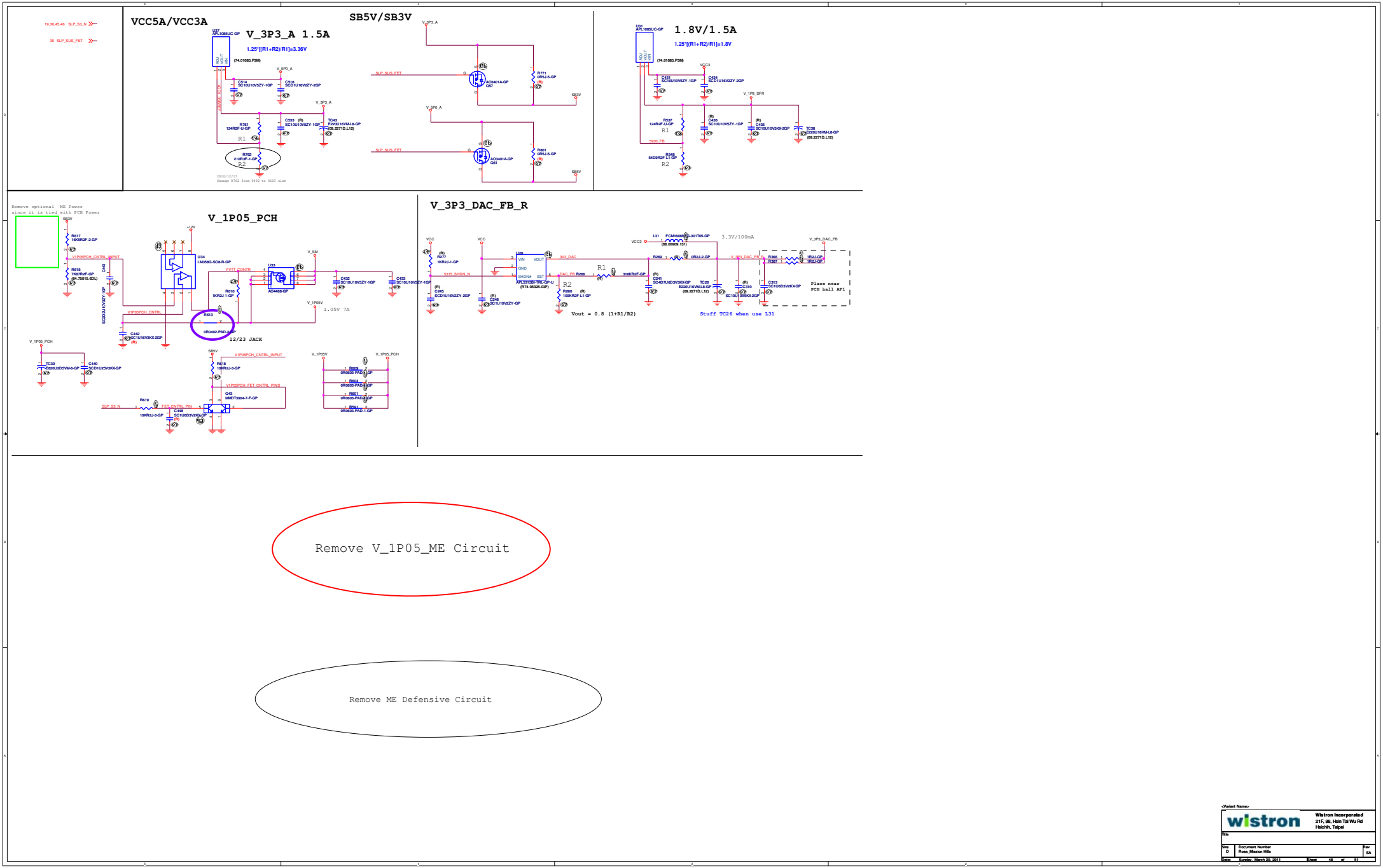
VCC5A/VCC3A
V_3P3_A 1.5A
1.25*[(R1+R2)/R1]=3.36V
SB5V/SB3V
1.8V/1.5A
1.25*[(R1+R2)/R1]=1.8V
V_1P05_PCH
V_3P3_DAC_FB_R
3.3V/100mA
Vout = 0.8 (1+R1/2)
Stuff TC26 when use L31
Place near PCH ball AF1
12/23 JACK
1.05V 7A
Remove optional ME Power since it is tied with PCH Power
Remove V_1P05_ME Circuit
Remove ME Defensive Circuit
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CPU VTT POWER

PCH

CPU SA POWER

CPU VTT POWER

Ipeak = (8.5uA*Rocset)/(DCR*K)

Rocset=6.49K,DCR=1.6mohm,K=1.3,Ipeak=26.5A

84.03004.036 QM3004D
Vgs @ 4.5V,
Id = 53A,
Rds(on) = 11~14mohm,

84.03006.036 QM3006D
Vgs @ 4.5V,
Id = 78A,
Rds(on) = 7.5~9mohm,

1.2uH, DCR=1.6mohm, Idc=26A

V_CPU_VCCIO 1.05V/1.00V Max=17A

820uF/2.5V, ESR=8 mohm

Place at bottom side

Vout=0.8*(R1+R2)/R2

DVT1

DVT2

VCCIO_SEL	V_CPU_VTT
1	1.05V
0	1.00V

Defensive Design

CPU SA POWER

12/23 JACK

Iomax=8.8A

Vout=0.8*(R1+R2)/R2

VCCSA_VID	V_SA
0	0.925V
1	0.85V

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CPU VCORE POWER

CPU AXG POWER

HOT

VCC_CORE

VCC_AXG

VCC_AXG

PWM ADDRESS		
Resistor value	SVID address for Vcore rail	SVID address for VCC_AXG rail
10K	0000	0001
25K	0010	0011
45K	0100	0101
70K	0110	0111
95K	1000	1001
124K	1010	1011
165K	1100	1101

3 Phase option

BOOT VOLTAGE	
Resistor value	Boot Voltage
10K	0V
25K	0.85V
45K	0.9V
70K	0.95V
95K	1V
124K	1.1V
165K	1.5V

VCORE VBOOT SET AT 1.1V

VCORE IMAX SET AT 112A

PWM ADDRESS

VCC_AXG IMAX SET AT 35A

Option: Disalbe VCC_AXG

12/23 JACK

Put colse to VCC_AXG hot spot

Work F=270Khz

Bottom PAD connect to GND Through 4 Vias

Put colse to VCORE hot spot

84.03004.036 QM3004D
Vgs @ 4.5V,
Id = 55A,
Rds(on) = 11~14mohm,

84.03006.036 QM3006D
Vgs @ 4.5V,
Id = 78A,
Rds(on) = 7.5~9mohm,

0.5uH, DCR=0.78 mohm, Idc=31A

820uF/2.5V, ESR=8 mohm

0.65V~1.3V/35A, TDC=25A

Bottom PAD connect to GND through 4 Vias

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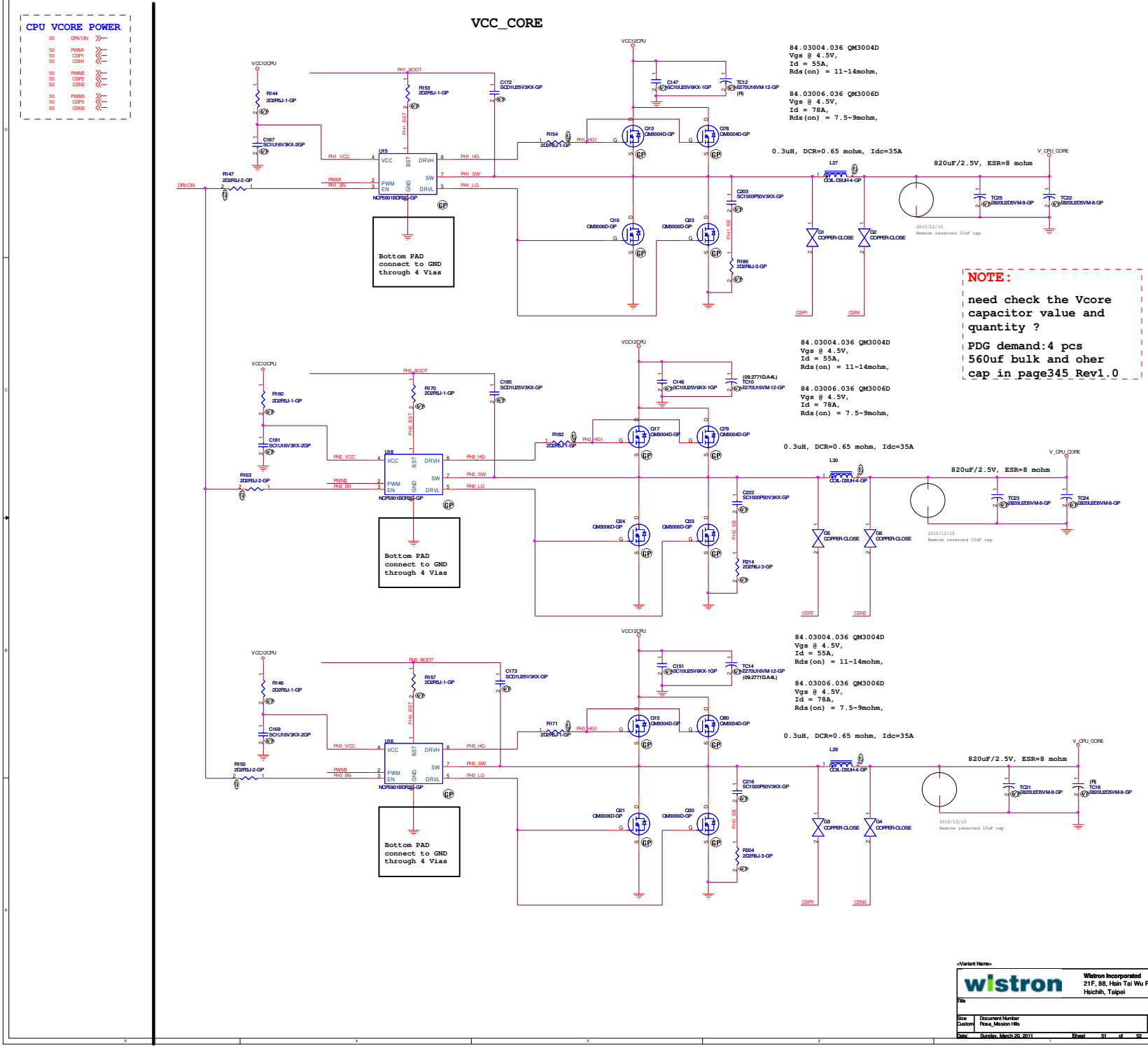
VCC_CORE


CPU VCORE POWER
50 DRVON
50 PWM1
50 CSP1
50 CSN1
50 PWM2
50 CSP2
50 CSN2
50 PWM3
50 CSP3
50 CSN3
VCC12CPU
PH1_BOOT
R144 2D2R5J-1-GP
R153 2D2R5J-1-GP
C172 SCD1U25V3KX-GP
C167 SC1U16V3KX-2GP
PH1_BST
PH1_VCC
U15
VCC
BST
DRVH
SW
GND
DRVL
PWM
EN
NCP5901BDR2G-GP
PWM1
PH1_EN
PH1_HG
PH1_SW
PH1_LG
R147 2D2R5J-2-GP
DRVON
R154 2D2R5J-1-GP
PH1_HG1
Q13 QM3004D-GP
Q78 QM3004D-GP
Q16 QM3006D-GP
Q23 QM3006D-GP
C147 SC10U25V6KX-1GP
TC12 E270U16VM-12-GP (R)
C203 SC1500P50V3KX-GP
PH1_SB
R186 2D2R5J-3-GP
Bottom PAD connect to GND through 4 Vias
84.03004.036 QM3004D
Vgs @ 4.5V,
Id = 55A,
Rds(on) = 11~14mohm,
84.03006.036 QM3006D
Vgs @ 4.5V,
Id = 78A,
Rds(on) = 7.5~9mohm,
0.3uH, DCR=0.65 mohm, Idc=35A
820uF/2.5V, ESR=8 mohm
L27 COIL-D3UH-4-GP
G1 COPPER-CLOSE
G2 COPPER-CLOSE
V_CPU_CORE
TC25 E820LD5VM-8-GP
TC22 E820LD5VM-8-GP
2010/12/15
Remove reserved 10uF cap
CSP1
CSN1
NOTE:
need check the Vcore capacitor value and quantity ?
PDG demand:4 pcs 560uf bulk and oher cap in page345 Rev1.0
PH2_BOOT
R160 2D2R5J-1-GP
R170 2D2R5J-1-GP
C195 SCD1U25V3KX-GP
C181 SC1U16V3KX-2GP
PH2_BST
PH2_VCC
U18
PH2_HG
PH2_SW
PH2_LG
R163 2D2R5J-2-GP
PWM2
PH2_EN
R182 2D2R5J-1-GP
PH2_HG1
Q17 QM3004D-GP
Q79 QM3004D-GP
Q24 QM3006D-GP
Q83 QM3006D-GP
C146 SC10U25V6KX-1GP
(09.2771DA4L) TC10 E270U16VM-12-GP
C222 SC1500P50V3KX-GP
PH2_SB
R214 2D2R5J-3-GP
L30 COIL-D3UH-4-GP
Q5 COPPER-CLOSE
Q6 COPPER-CLOSE
TC23 E820LD5VM-8-GP
TC24 E820LD5VM-8-GP
CSP2
CSN2
PH3_BOOT
R146 2D2R5J-1-GP
R157 2D2R5J-1-GP
C173 SCD1U25V3KX-GP
C169 SC1U16V3KX-2GP
PH3_BST
PH3_VCC
U16
PH3_HG
PH3_SW
PH3_LG
R150 2D2R5J-2-GP
PWM3
PH3_EN
R171 2D2R5J-1-GP
PH3_HG1
Q15 QM3004D-GP
Q80 QM3004D-GP
Q21 QM3006D-GP
Q30 QM3006D-GP
C151 SC10U25V6KX-1GP
TC14 E270U16VM-12-GP (09.2771DA4L)
C216 SC1500P50V3KX-GP
PH3_SB
R204 2D2R5J-3-GP
L29 COIL-D3UH-4-GP
G3 COPPER-CLOSE
G4 COPPER-CLOSE
TC21 E820LD5VM-8-GP
TC19 E820LD5VM-8-GP
CSP3
CSN3
<Variant Name>
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