Model Name:GA-P41T-D3 *Revision 1.4*

SHEET	TITLE
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B,D
06	P4_LGA775_C
07	P4_LGA775_E,F,G,H
08	Eaglelake HOST
09	Eaglelake DDR
10	Eaglelake PCI_EXP_16,DMI
11	Eaglelake VGA
12	Eaglelake GND
13	Eaglelake PWR
14	PCI EXPRESS*16 SLOT
15	DDRII CHANNEL A
16	DDRII CHANNEL B
17	DDRII TERMINATION
18	ICH7 PCI, USB, DMI, LAN
19	ICH7 IDE, GPIO, SATA, CTRL
20	ICH7 VCC, GND
21	CK505 CLOCK.
22	PCI SLOT 1,2,PCIE*1
23	IDE/FLOPPY
24	ITE 8718 GB/HX
25	COM_LPT
26	CI,HWM,KB/MS,DUAL BIOS
27	ALC888

SHEET	TITLE
28	REAR AUDIO JACK
29	DISCRETE POWER
30	VCORE PWM_ISL6312
31	ATX, OTHERS POWER
32	FRONT PANEL
33	REALTEK RTL8111D
34	PCI SLOT3,PCIE*2,3

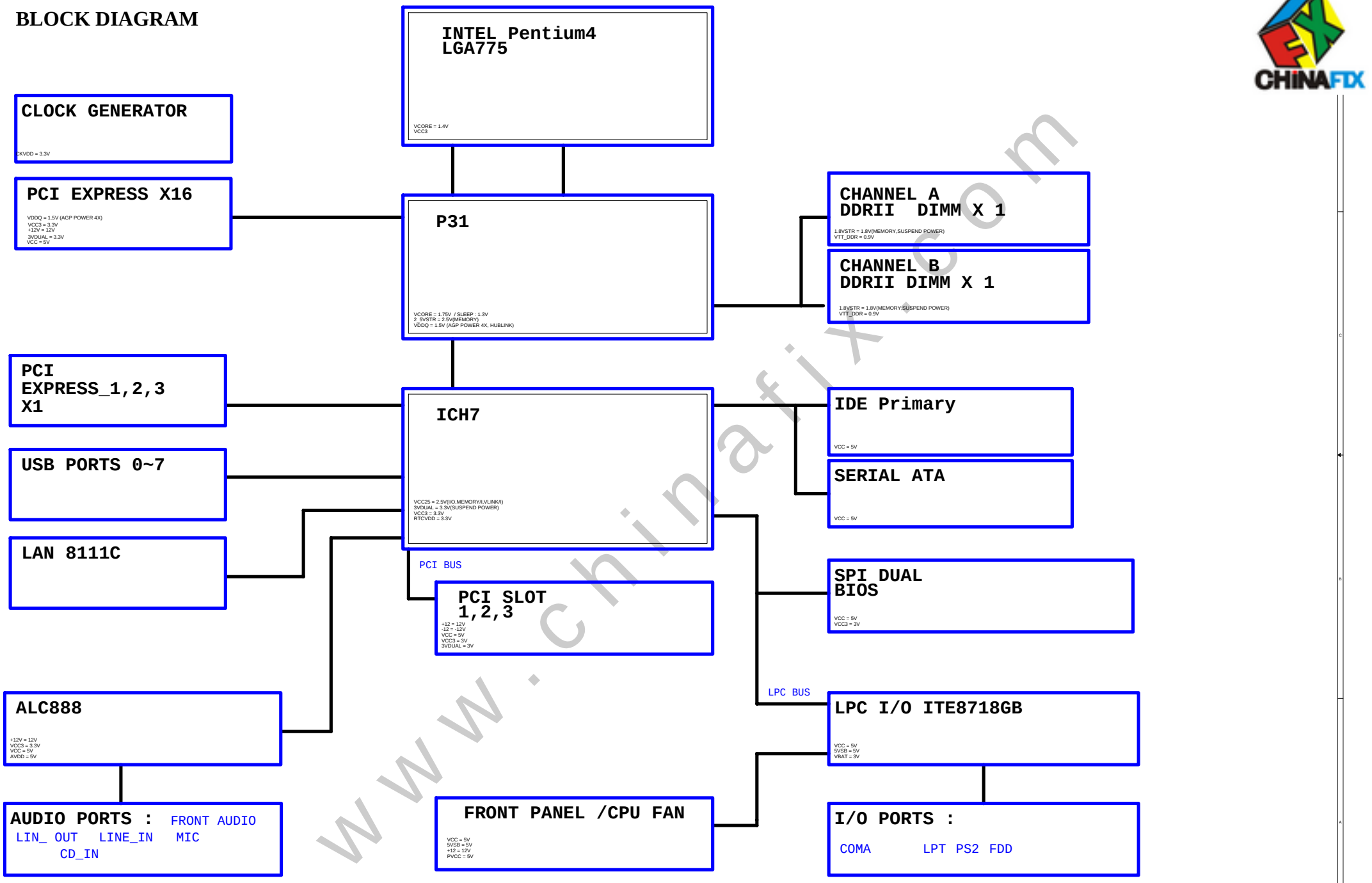
Gigabyte Technology

Title: Cover Sheet

Size: Custom | Document Number: GA-P41T-D3 | Rev: 1.4

Date: Friday, July 16, 2010 | Sheet 1 of 34

BLOCK DIAGRAM



Gigabyte Technology		
Title: BOM & PCB MODIFY HISTORY		
Size: Custom	Document Number: GA-P41T-D3	Rev: 1.4
Date: Friday, July 16, 2010	Sheet 2 of 34	

Model Name:GA-P41T-D3

Version: 1.4

Component value change history

2007/08/02

Data	Change Item	Reason
2007/08/03		EBOM:9MG31MS2L-00-10B
2007/08/22 EBOM:10A	1.G31 CHIP -->P31 CHIP, remove VGA function,add comb port	
	2.ADD 1 PCI SLOT,2 PCIE SLOT	
2007/09/10 PBOM:10A	1.R375 8.2K-->1K ,R1951 1K-->8.2K	
	2.R327 2.67K-->649 ,R325 8.45K-->1M,DR37 1.4K-->1.54K,DR30 330-->365	
	3.R2913 1.18K-->2.21K,R2914 360-->931	
2008/05/14 PBOM:11A	1.ADD DES LITE ,FERRITE CHOKE	
	2.B0 CHIP , SMD POLY FUSE	
2008/06/26 EBOM:20B	1.20A BOM爲 PCB2.0使用,故以20B FOR PCB:2.01	
	2.修改爲RTM587 CLOCK GEN,RTL8111C,ALC883,DUAL BIOS,FORNT USB ADD PROTECT DIODE	
2008/07/21 PBOM:10A	1.ALC883--->888; DR30 316-->365 ;BC747 0.1U\Y5V-->X7R;IDE red--->green	
	2.ADD C1908 10PF / R1896 1K-->330 ohm add c1908 22pf ,22ohm--->0ohm for bios CS0 glitch issue	
	3.DEL R2935, ADD R2936 FOR MAIN POWER BIOS---rechard 說的	
2008/07/31 PBOM:10B	1.DQ13 2N7002--->MMBT2222A FOR CPU FSB LATCH ERROR ISSUE	
2008/08/21 PBOM:10C	1.CLOCK GEN POWER CAP 0.1U/Y5V---->0.1U/X7R FOR CPU INFORMATION FAIL ISSUE	
	2.ADD PCB CR ,CL	
P41T-ES3G-10A	1. SC1~SC8轉背板	
P41T-ES3G-13A	2. F4,F5 10FP1-06160B-C1R -> 10FP1-06350B-10R	

Circuit or PCB layout change for next version

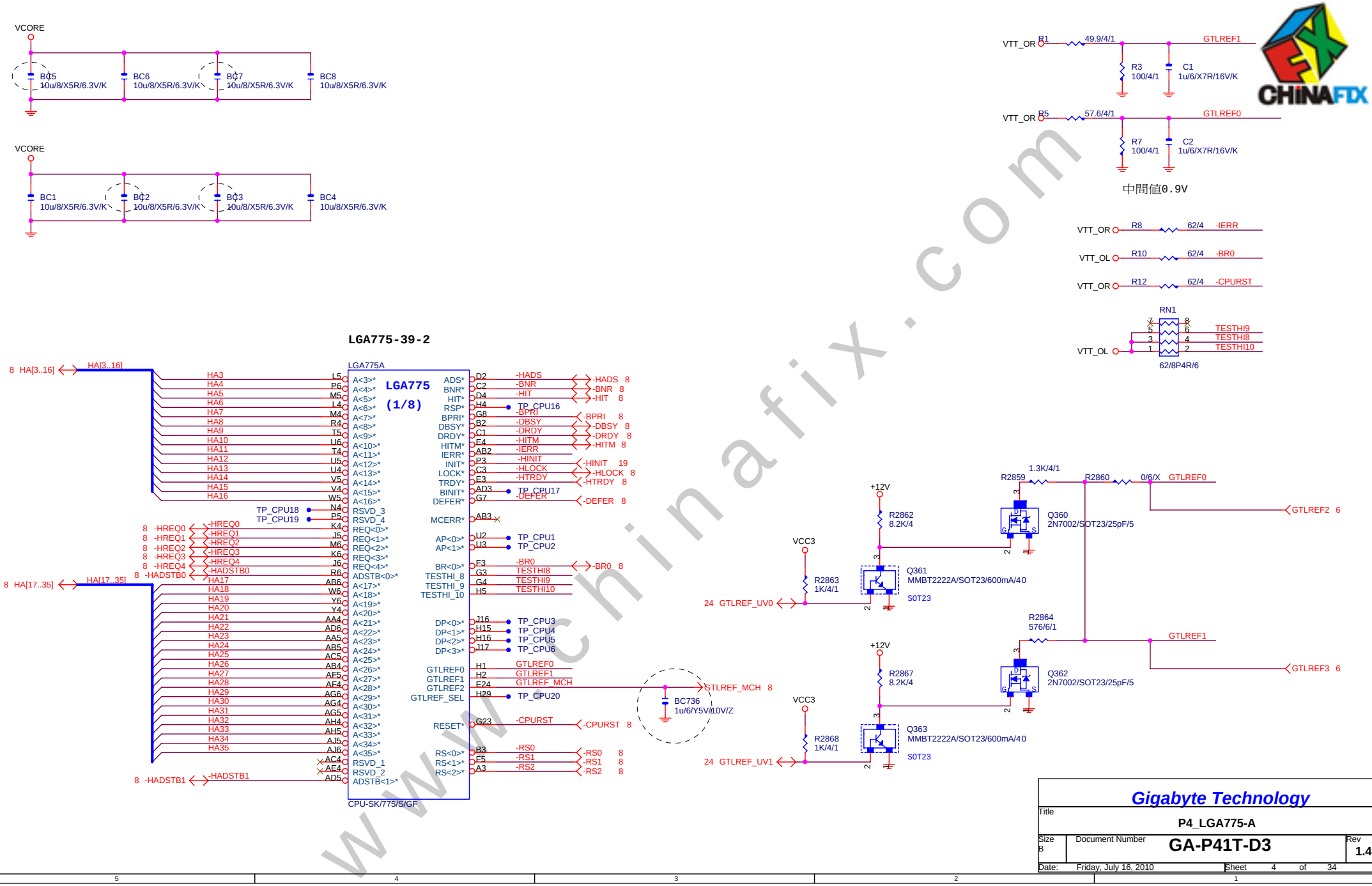
DATE	Change Item	Reason
2007/08/08 PCB:1.0	1.由GA-G31M-S2L-1.01修改	
	2.ADD 1 PCI SLOT,2 PCIE SLOT	
2007/09/07 PCB:1.0	1.由GA-P31-S3E-1.0 rename GA-P31-S3G-1.0	
2008/05/14 PCB:1.1	1.由 GA-P31-S3G-1.0修改,ADD DES LITE ,FERRITE CHOKE	
2008/06/12 PCB:2.01	1.由 GA-P31-S3G-1.1修改	
	2.ALC662--->ALC883,ADD RCA IN REAR-->ALC888;RTL8111C	
	3.DUAL BIOS 4M;DUAL BIOS	
	4.SUPPORT CPU FSB 1600	
2008/07/18 PCB:1.0	1.由 GA-P31-S3G-2.01 rename GA-P31-ES3G 1.0	
	2.移除EASY SAVER文字面	
2009/08/27 PCB:1.0	1.由 GA-P31-ES3G 1.0改成P41-ES3G-1.0,更換北橋	
2009/10/01 PCB:1.1	1.ADD EUP FUNCTION	
	2.更換螺孔FOOTPRINT	
	3.更換DDR18V_OV2 GPIO PIN	
P41T-ES3G 0.1	1. EVT Release	
	2. DDR3 1333+ --> DDR3 1333 OC	
P41T-ES3G 1.0	1. PVT Release	
P41T-ES3G 1.3	1. 文字面Rev1.0 --> Rev1.3 for USB 3X Power	
P41T-ES3G 1.4	1. RTL8111D --> RTL8111E 2. R2985~R2988 Short Wire --> 0/4 ohm 3. SATA2_0~SATA2_3 Update footprint "H1X7-SATA2- HS-MASK" 4. Add Prochot control circuit (GPO21:MB_ID , ICH7_GPO0 prochot) 5. 定位孔移除	

Gigabyte Technology

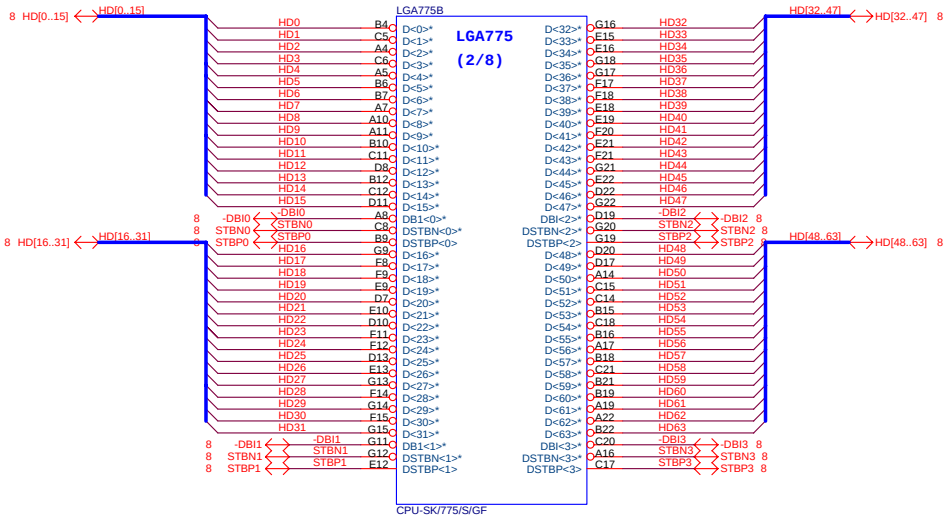
Title: BOM & PCB MODIFY HISTORY

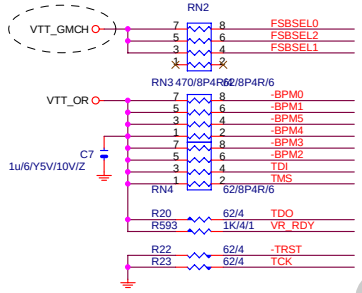
Size: Custom | Document Number: GA-P41T-D3 | Rev: 1.4

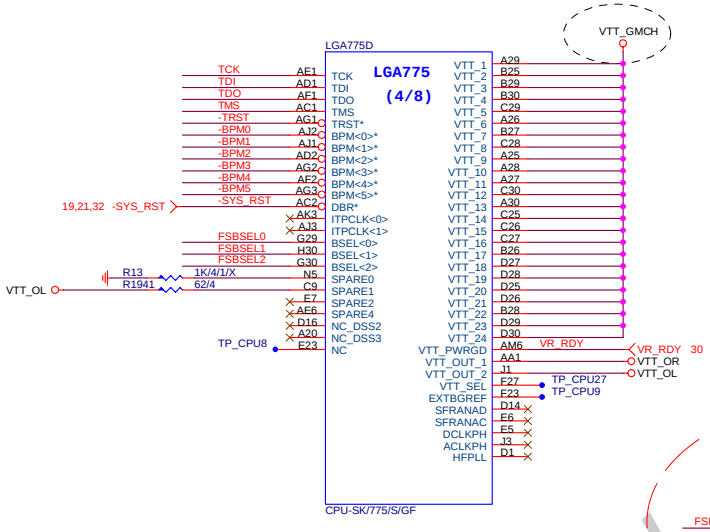
Date: Friday, July 16, 2010 | Sheet 3 of 34



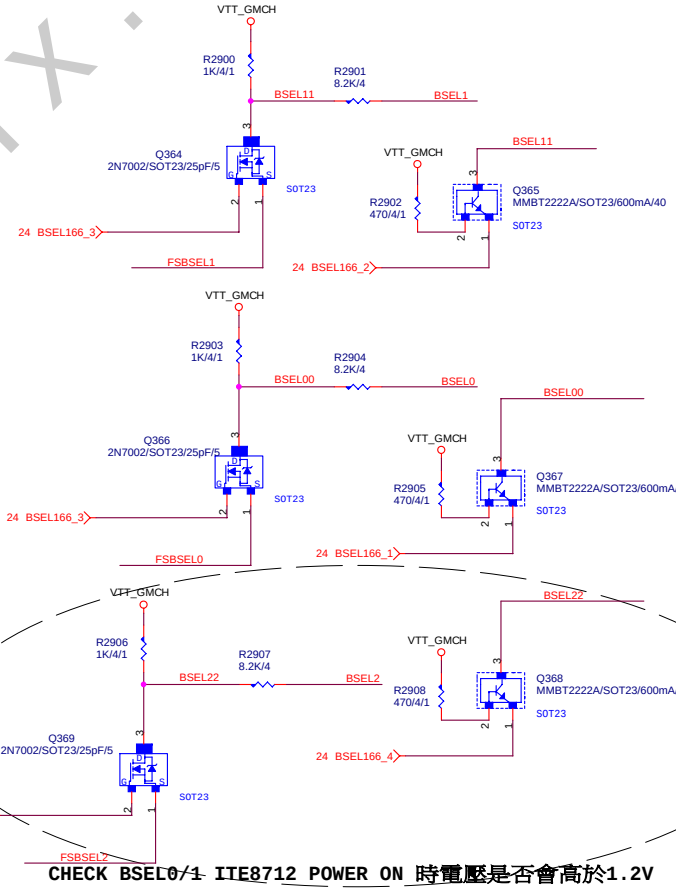
Gigabyte Technology		
Title	P4_LGA775-A	
Size B	Document Number GA-P41T-D3	Rev 1.4
Date: Friday, July 16, 2010	Sheet 4 of 34	

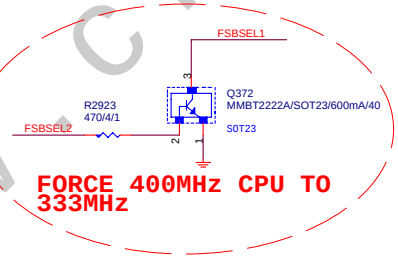






FOR ALL DDR CLK RATIO





FORCE 400MHz CPU TO 333MHz

FSA	FSB	FSC			
FSBSEL0	FSBSEL1	FSBSEL2	Clock		
?	1	0	1	100MHz	
?	1	0	0	133MHz	3/4
G31	0	1	0	200MHz	2/2.66/3.33/4
G31	0	0	0	266MHz	2/2.5/3/4
G31	0	0	1	333MHz	2/2.4
	0	1	1	400MHz	

400/533
400/533/667/800
533/667/800/1066
667/800

CHECK BSEL0/1 IIE8712 POWER ON 時電壓是否會高於1.2V

Gigabyte Technology	
Title	P4_LGA775-B,D
Size: Custom	Document Number: GA-P41T-D3
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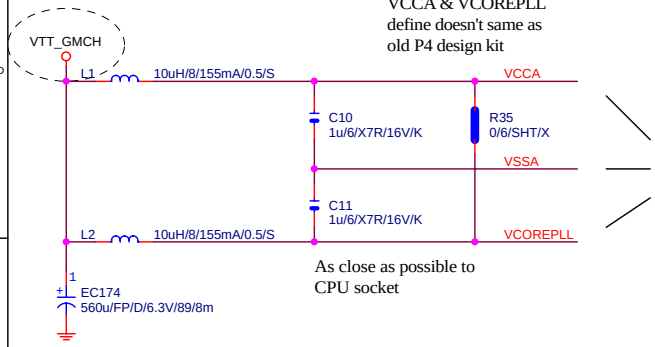
Date: Friday, July 16, 2010	Sheet 5 of 34

Note:

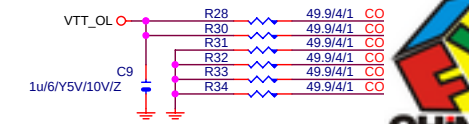
VCCA & VCOREPLL define doesn't same as old P4 design kit

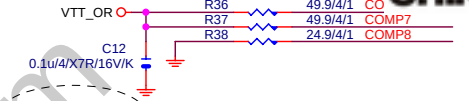


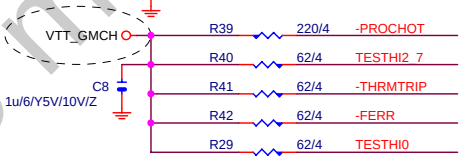
Trace width doesn't less than 12 Mil

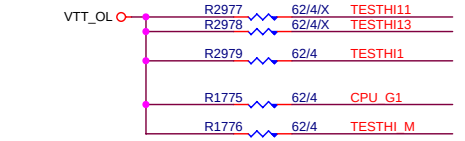
As close as possible to CPU socket

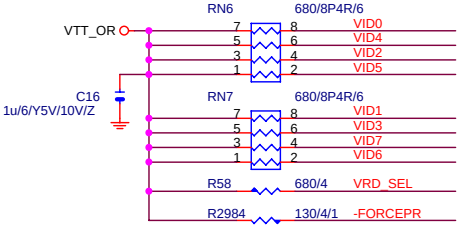
Place outside of CPU socke

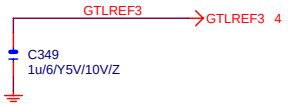


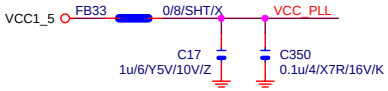


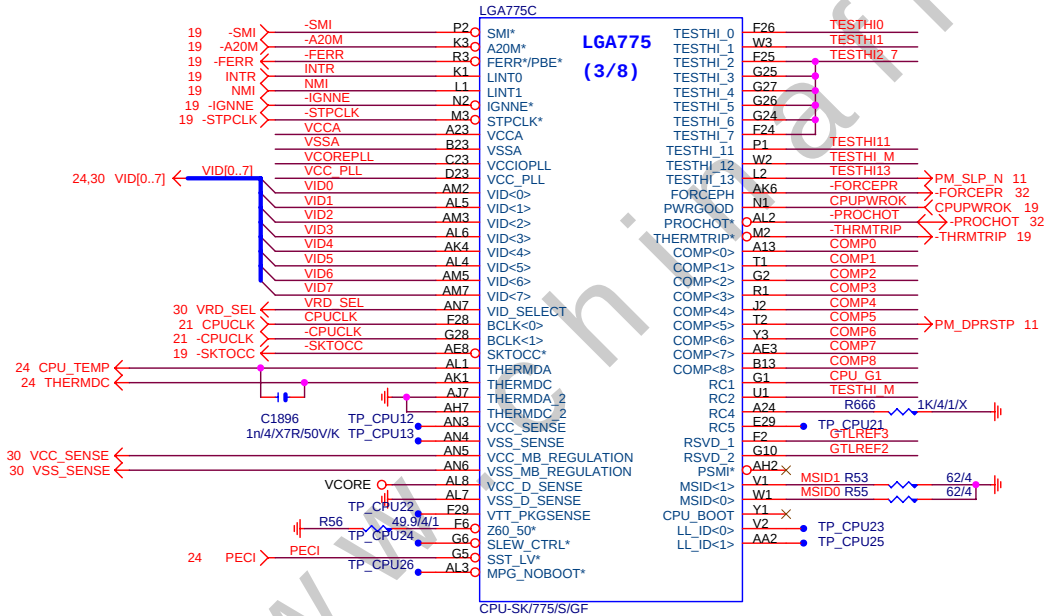






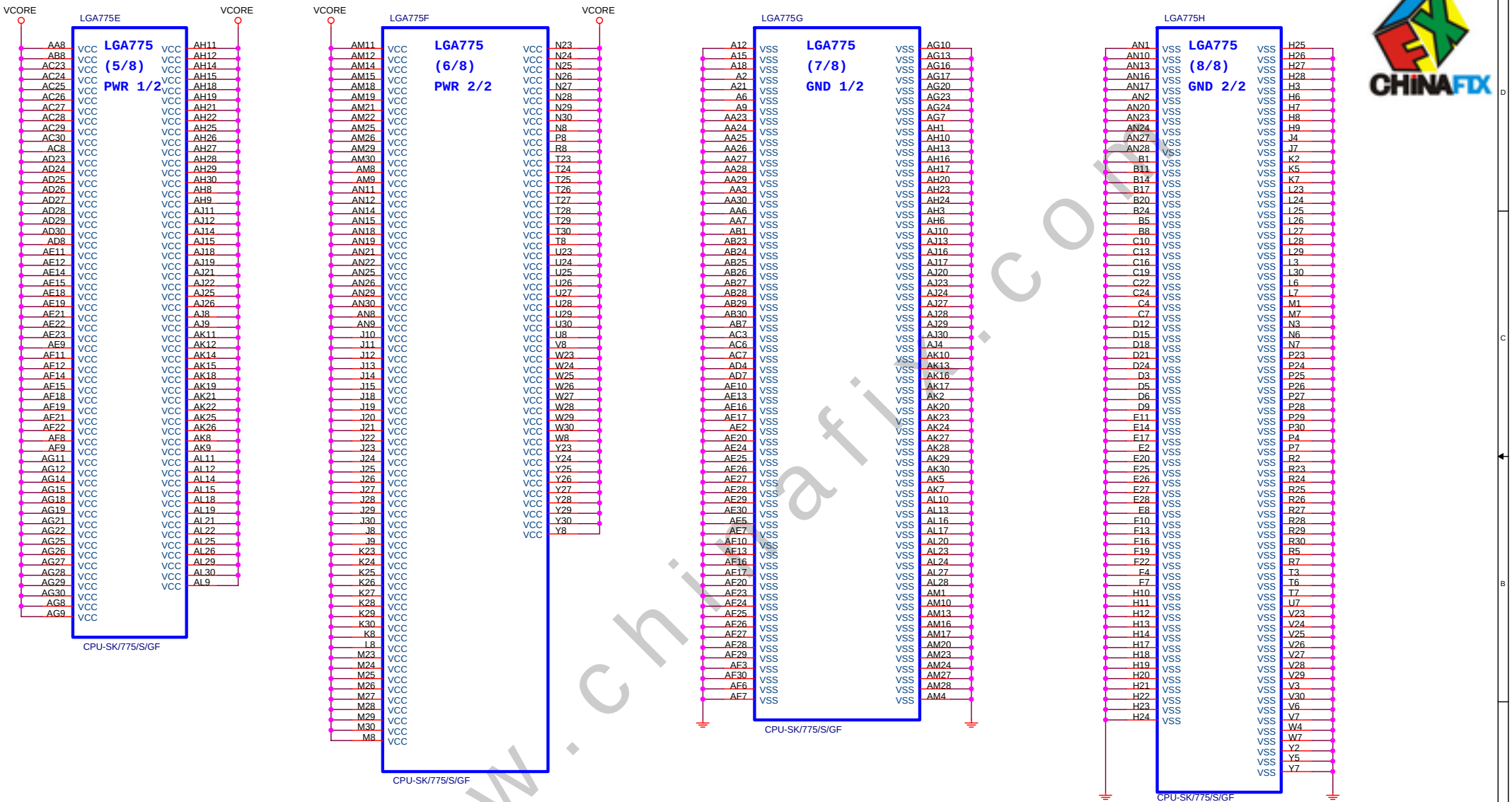




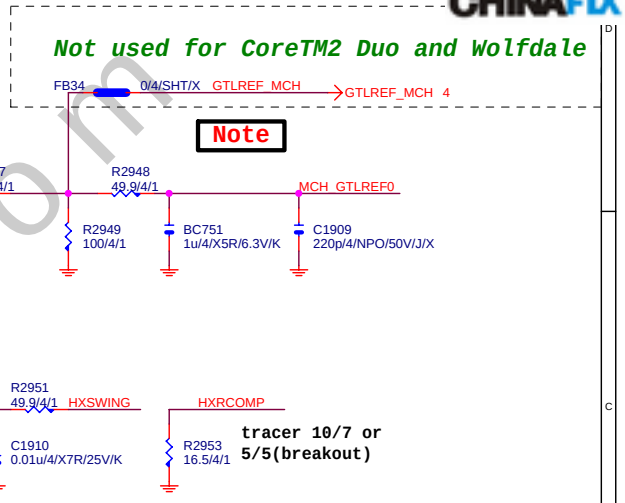


PECI:Platform Environment Control Interface

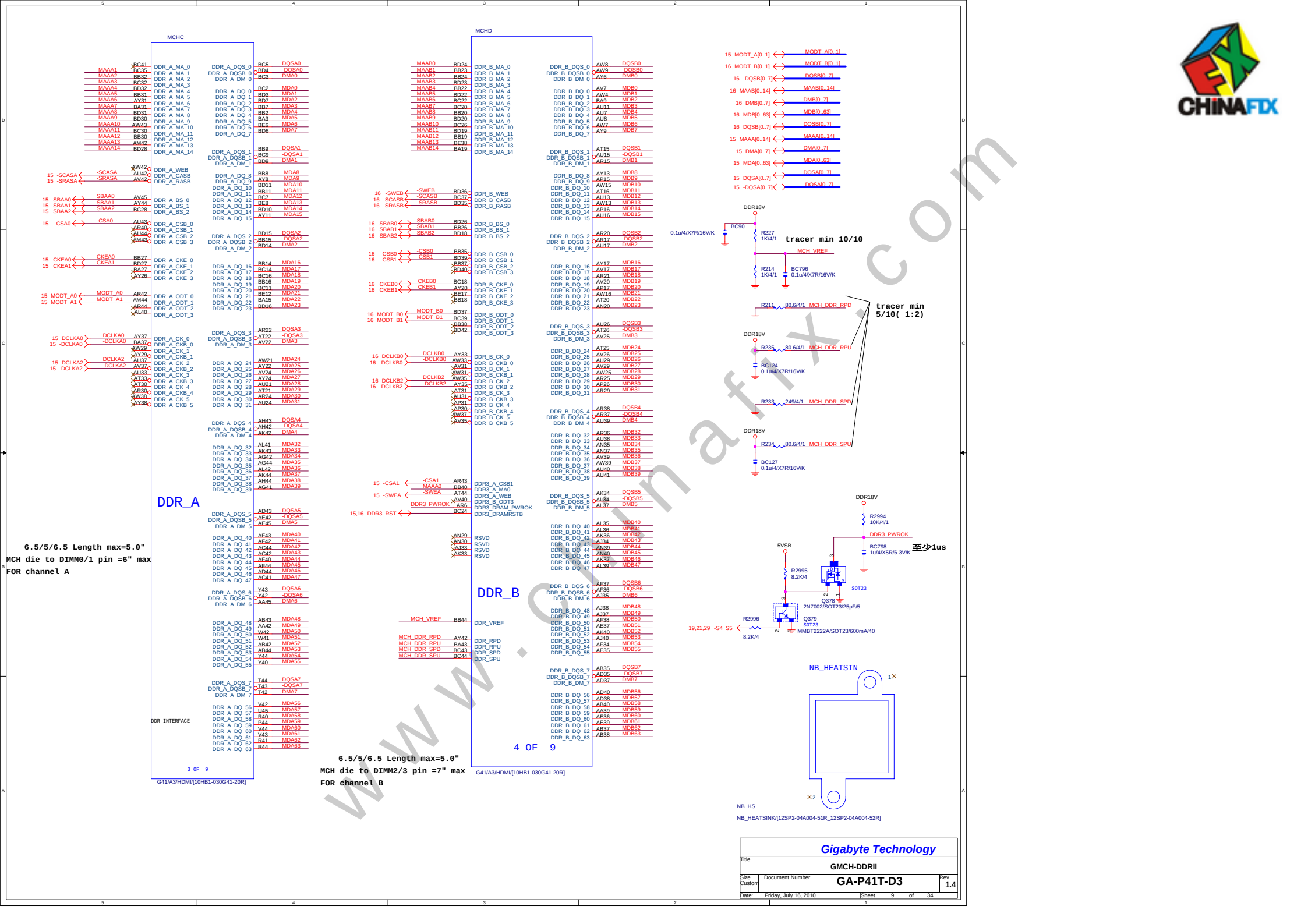
Gigabyte Technology		
Title: P4_LGA775-C		
Size: B	Document Number: GA-P41T-D3	Rev: 1.4
Date: Friday, July 16, 2010	Sheet 6 of 34	



Gigabyte Technology		
Title: P4_LGA775-E,F,G,H		
Size: B	Document Number: GA-P41T-D3	Rev: 1.4
Date: Friday, July 16, 2010	Sheet 7 of 34	



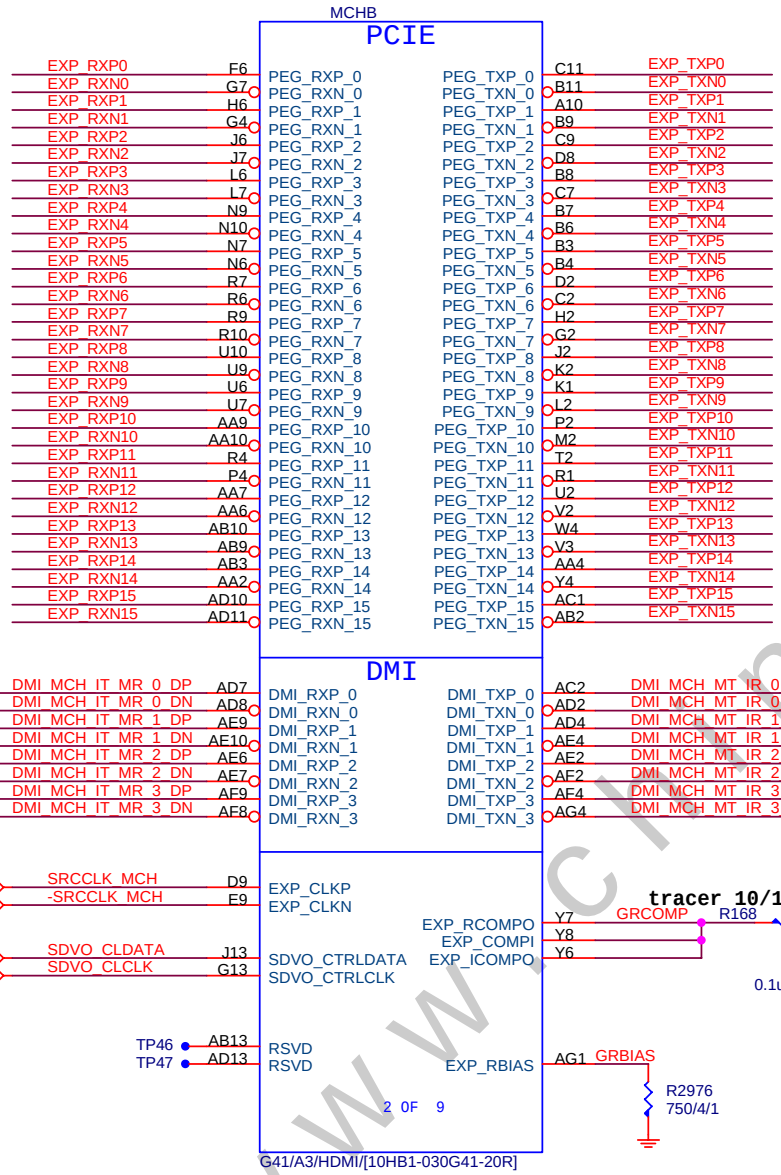
Gigabyte Technology			
Title: GMCH-HOST			
Size: Custom	Document Number: GA-P41T-D3		Rev: 1.4
Date: Friday, July 16, 2010		Sheet 8 of 34	

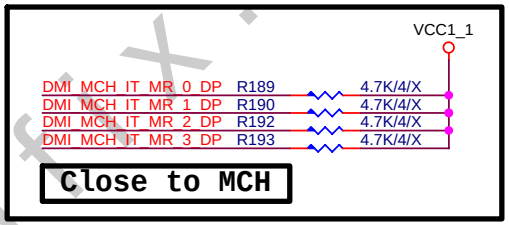


Gigabyte Technology			
Title: GMCH-DDRII			
Size: Custom	Document Number: GA-P41T-D3		Rev: 1.4
Date: Friday, July 16, 2010	Sheet 9 of 34		

PCIEX16:16/5/5/5/16(breakout min 8/4/5/4/8)

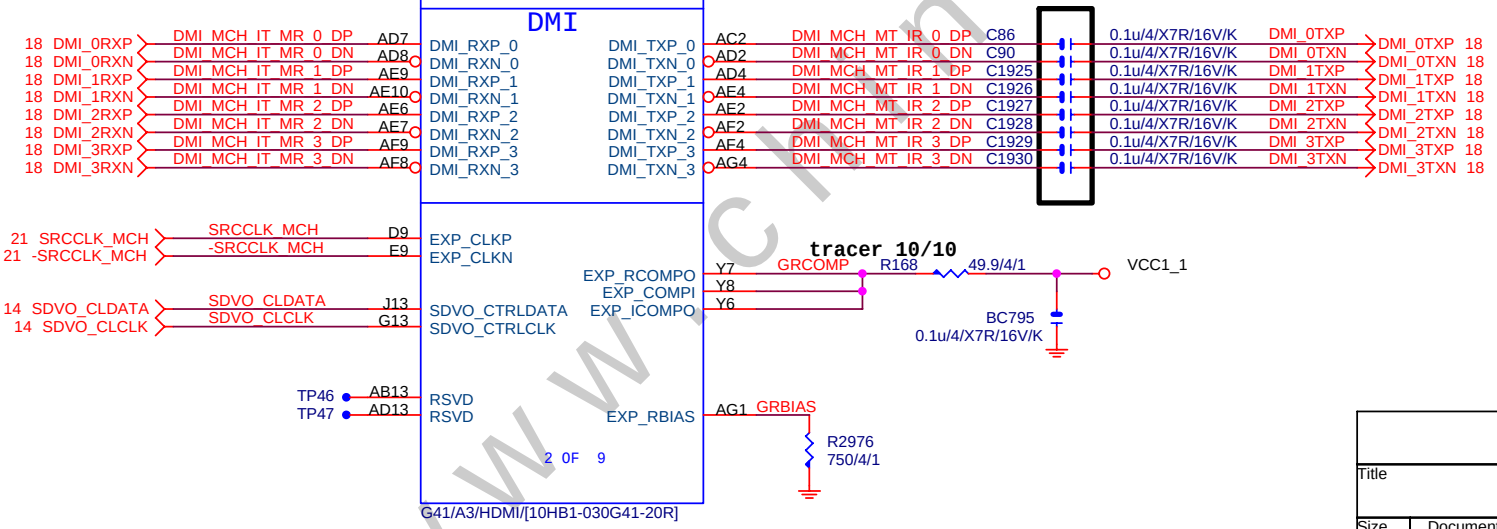
Impedance=85 +- 17.5%





DMI:12/4/8/4/12

Impedance=95 +- 17.5%



Gigabyte Technology

Title: GMCH-PCI E & DMI

Size: Custom | Document Number: GA-P41T-D3 | Rev: 1.4

Date: Friday, July 16, 2010 | Sheet 10 of 34

EXP_SM
0:SDVO OR PCIE
1:BOTH SDVO AND PCIE
EXP_SLR:
0:BTX PCIE are reversed
1:ATX PCIE normal

MCHE

4/10//15<500 MILS

1th RGB:7.5/6 < 300 MILS 2th RGB:4/20 <5"~8" inch

VGA

ON-BOARD VGA 75ohm
non-ON-BOARD VGA 0ohm

4/6//12

ON-BOARD VGA 1.02k
non-ON-BOARD VGA 0ohm

MISC

BW+ICH8 不要上(SAMPLE)
BW+ICH7 要上

CL_VREF:4/10

0.349V

ITPM:
0:ENABLE ITPM
1:DISABLE ITPM

CEN:
0:DISABLE TLS
1:ENABLE TLS

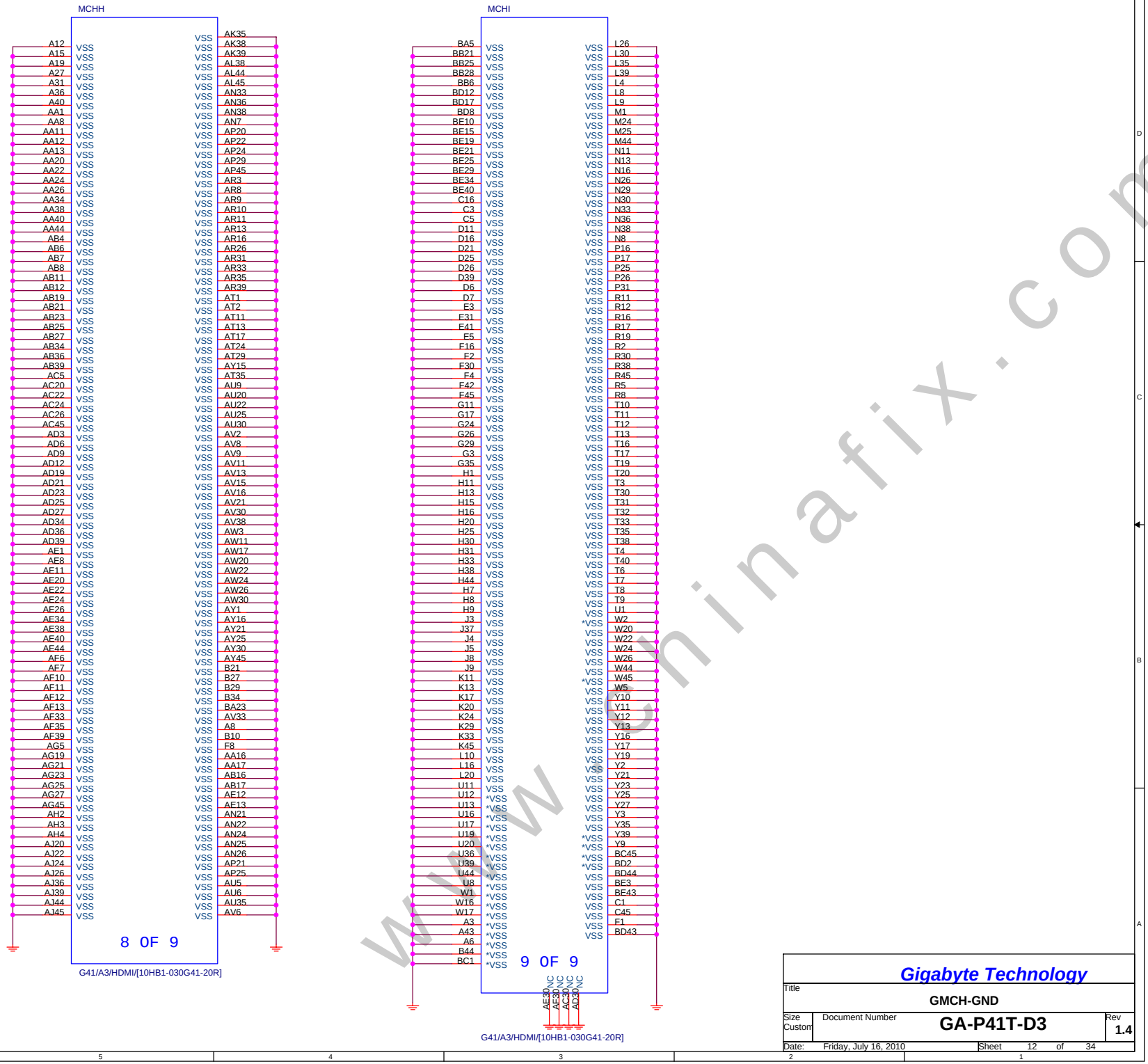
DualX8_Enable:
0 = 2x8 PCI Express Ports
1 = 1x16 PCI Express Port

G41CHIP 都要上

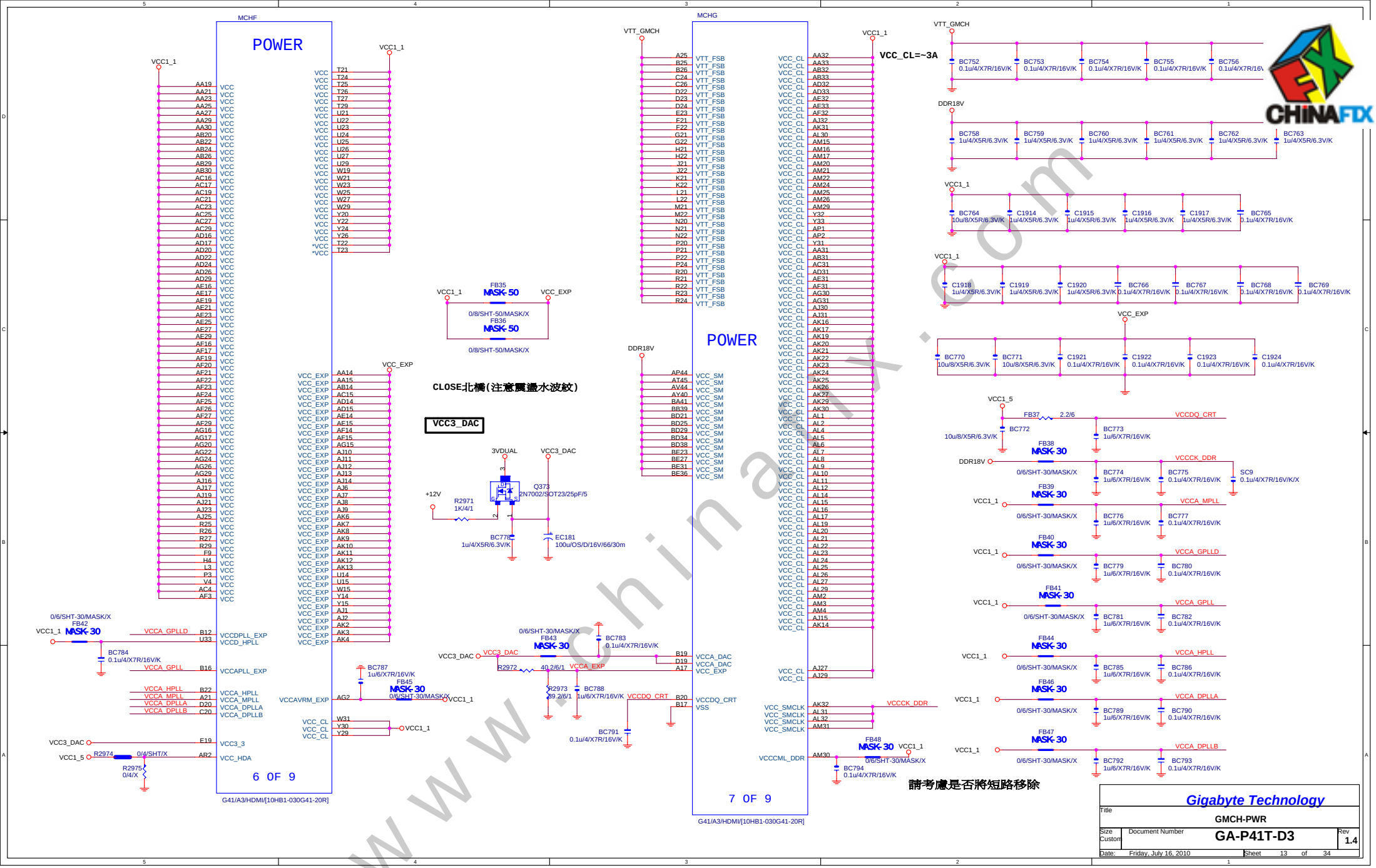
5 OF 9

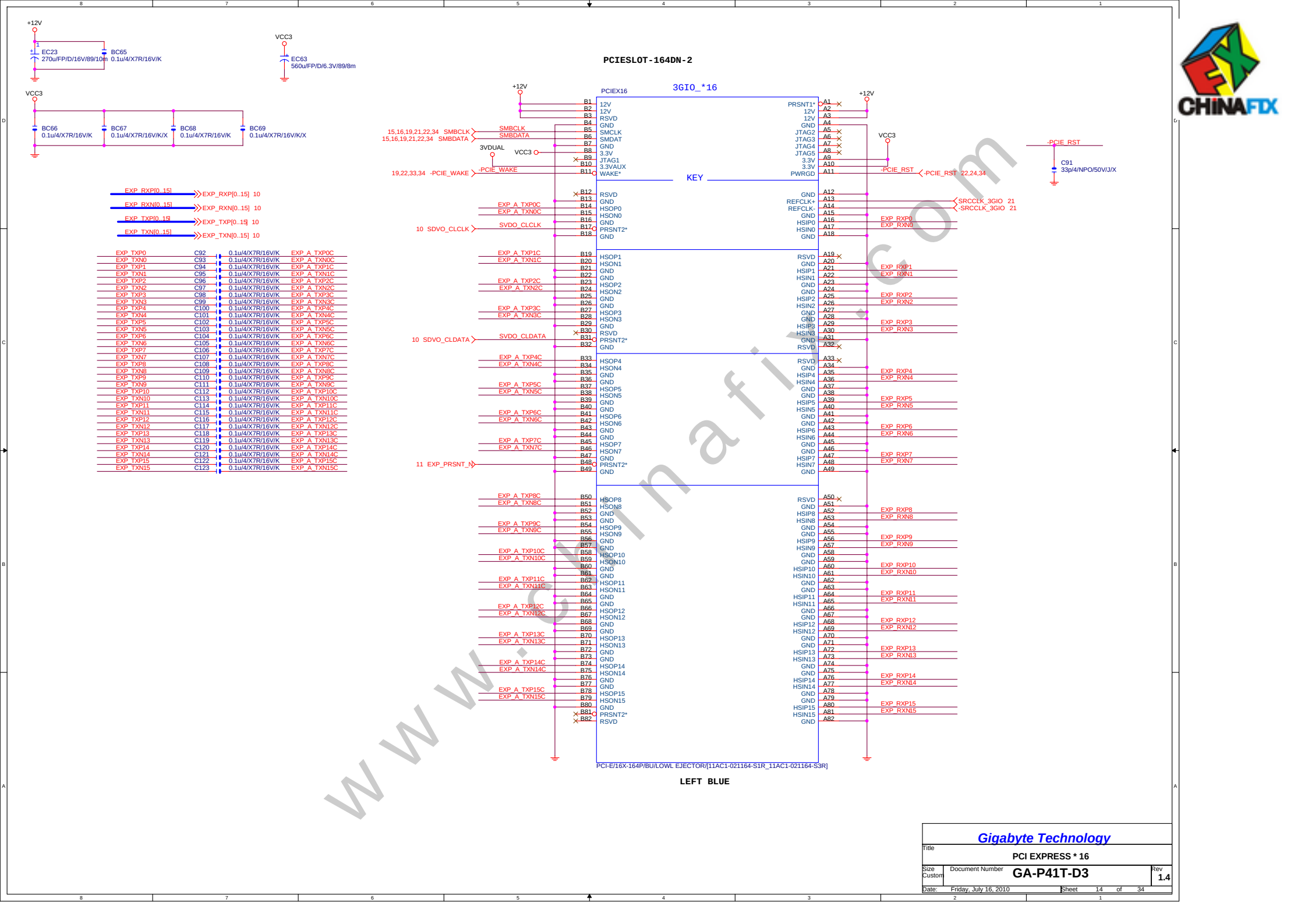
G41/A3/HDMI/[10HB1-030G41-20R]

Gigabyte Technology			
Title: GMCH-INTERNAL VGA			
Size: B	Document Number: GA-P41T-D3		Rev: 1.4
Date: Friday, July 16, 2010	Sheet 11 of 34		

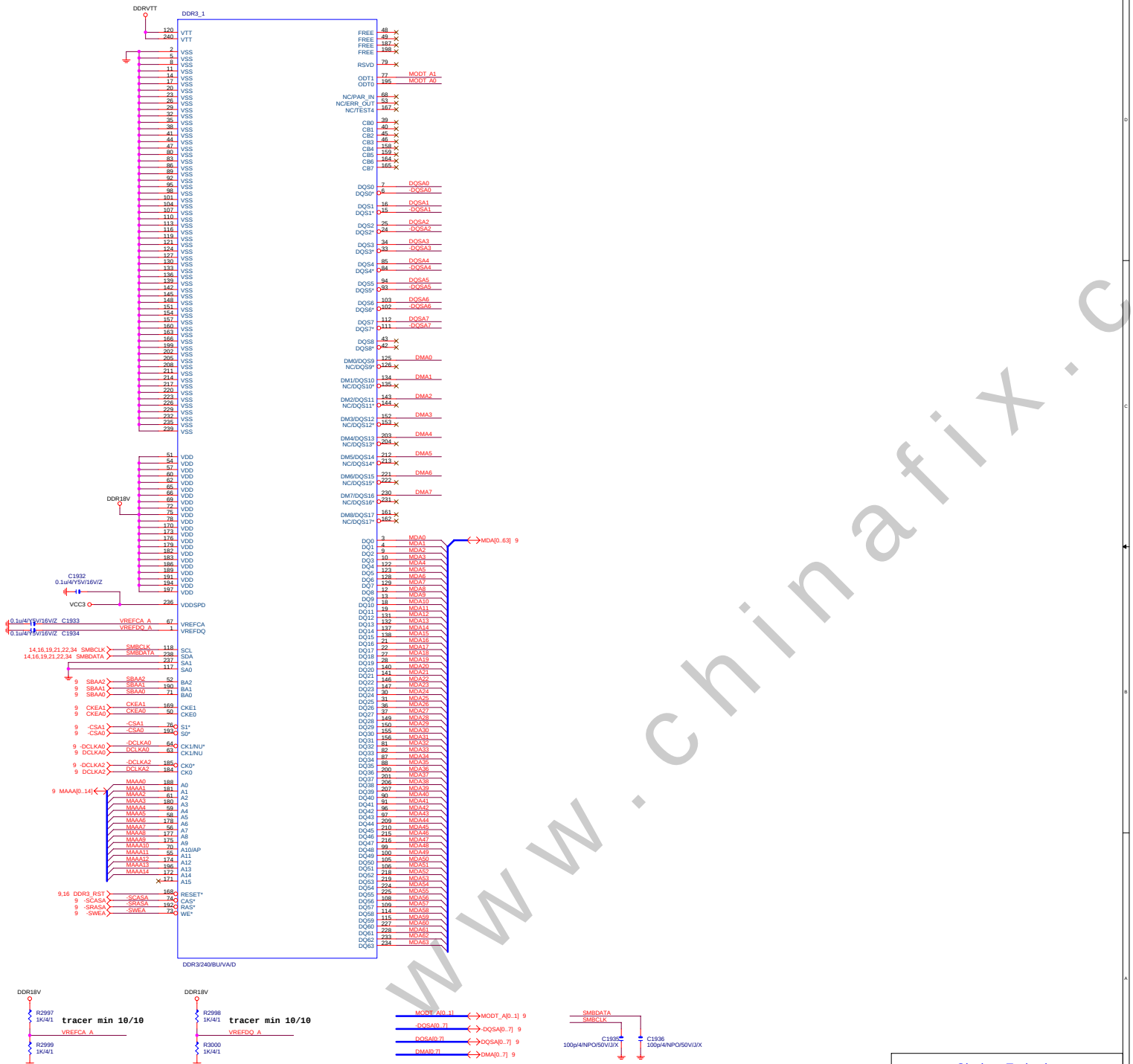


Gigabyte Technology		
Title: GMCH-GND		
Size: Custom	Document Number: GA-P41T-D3	Rev: 1.4
Date: Friday, July 16, 2010	Sheet 12 of 34	

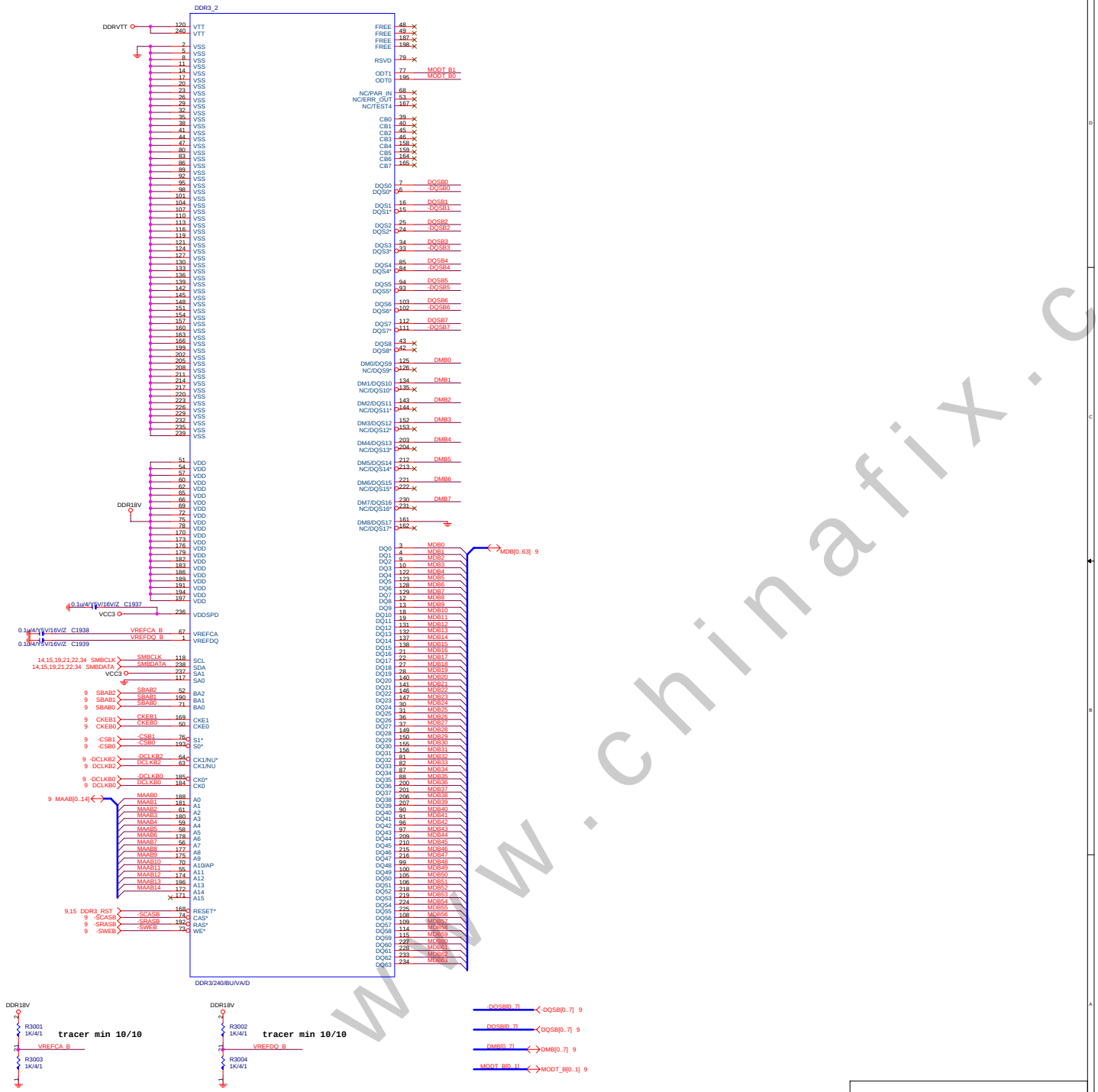




Gigabyte Technology			
Title: PCI EXPRESS * 16			
Size: Custom	Document Number: GA-P41T-D3		Rev: 1.4
Date: Friday, July 16, 2010	Sheet 14 of 34		



Title	Gigabyte Technology
	DDR3 CHANNEL A
Size: Custom	Document Number: GA-P41T-D3
Rev	1.4
Date:	Sheet 15 of 34

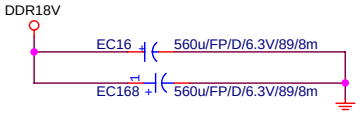


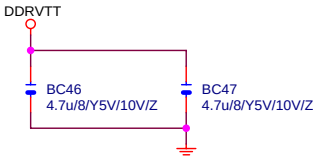
Title	DDR3 CHANNEL B
Size	Custom
Document Number	GA-P41T-D3
Rev	1.4
Date:	Sheet 16 of 34

Gigabyte Technology

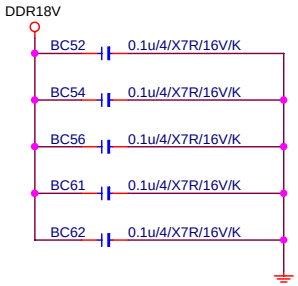
DDR TERMINATION CHANNEL A

DDRVTT Decouple

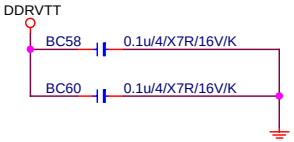




DDR18V Decouple

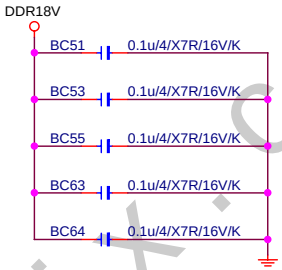


DDRVTT Decouple

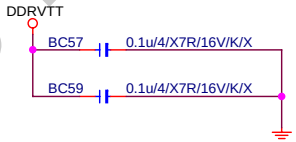


DDR TERMINATION CHANNEL B

DDR18V Decouple



DDRVTT Decouple



Gigabyte Technology		
Title: DDRII TERMINATOR		
Size: Custom	Document Number: GA-P41T-D3	Rev: 1.4
Date: Friday, July 16, 2010	Sheet 17 of 34	

FOR ICH7R POWER ON 瞬間會HIGH 到1.8V 之後0V,必須PULL DOWN 1K/6

H/W RESET

24 -RST_BTN
Q371 MMBT2222A/SOT23/600mA/40
Q370 MMBT2222A/SOT23/600mA/40
S0T23
S0T23
19 GPO16
R2915 100K/4/1
R2916 1K/4/1
BC744 1u/6/Y5V/10V/Z
BC745 1U/6/Y/10V/X/X

A_D[0..31] 22,34

U9A

PAR E10
-DEVSEL A12
ICH33 A9
R171 22/4
-IRDY A7
-PCIPME B19
-SERR B10
-STOP F15
-PLOCK E11
-TRDY F14
-PERR C9
-FRAME F16
PAR
DEVSEL#
PCICLK
PCIRST#
IRDY#
PME#
SERR#
STOP#
TRDY#
PERR#
FRAME#
22,34 PAR
22,34 -DEVSEL
21 ICH33
22,34 -PCIRST
22,34 -IRDY
22,34 -PCIPME
22,34 -SERR
22,34 -STOP
22,34 -PLOCK
22,34 -TRDY
22,34 -PERR
22,34 -FRAME
C124 100p/4/NPO/50V/J/X

-GNT0 E7
-GNT1 D16
-GNT2 D17
-GNT4 A14
-GNT5 D8
GNT0#
GNT1#
GNT2#
GNT3#
GNT4#_GPIO48
GPIO17/GNT5#
22 -GNT0
22 -GNT1
34 -GNT2
-GNT4

-REQ0 D7
-REQ1 C16
-REQ2 C17
-REQ3 E13
-REQ4 A13
-REQ5 C8
REQ0#
REQ1#
REQ2#
REQ3#
REQ4#/GPIO22
GPIO1/REQ5#
22 -REQ0
22 -REQ1
22,34 -REQ2
22 -REQ3
22 -REQ4
22 -REQ5

-PIRQA A3
-PIRQB B4
-PIRQC C5
-PIRQD B5
-PIRQE G8
-PIRQF F7
-PIRQG F8
-PIRQH G7
PIRQA#
PIRQB#
PIRQC#
PIRQD#
GPIO2/PIRQE#
GPIO3/PIRQF#
GPIO4/PIRQG#
GPIO5/PIRQH#
22,34 -PIRQA
22 -PIRQB
22,34 -PIRQC
22,34 -PIRQD
22,34 -PIRQE
22 -PIRQF
22 -PIRQG
22 -PIRQH

AD_0 E18 A_D0
AD_1 C18 A_D1
AD_2 A16 A_D2
AD_3 F18 A_D3
AD_4 E16 A_D4
AD_5 A18 A_D5
AD_6 F17 A_D6
AD_7 A17 A_D7
AD_8 A15 A_D8
AD_9 C14 A_D9
AD_10 E14 A_D10
AD_11 D14 A_D11
AD_12 B12 A_D12
AD_13 C13 A_D13
AD_14 G15 A_D14
AD_15 G13 A_D15
AD_16 E12 A_D16
AD_17 C11 A_D17
AD_18 D11 A_D18
AD_19 A11 A_D19
AD_20 A10 A_D20
AD_21 F11 A_D21
AD_22 F10 A_D22
AD_23 E9 A_D23
AD_24 D9 A_D24
AD_25 B9 A_D25
AD_26 A8 A_D26
AD_27 A6 A_D27
AD_28 C7 A_D28
AD_29 B6 A_D29
AD_30 E6 A_D30
AD_31 D6 A_D31

C/BE0# B15 -C_BE0
C/BE1# C12 -C_BE1
C/BE2# D12 -C_BE2
C/BE3# C15 -C_BE3
-C_BE0 22,34
-C_BE1 22,34
-C_BE2 22,34
-C_BE3 22,34

ICH7/A1/[10HB1-032801-N2R]

Pb-Free

SB_HEATSIN
1
2
SB_HS/[12SP2-030005-42R_12SP2-030005-43R]
SB_HS
NEW SB_HS 對邊

01=SPI
10=PCI
11=LPC(DEFAULT)
-GNT4 R1744 1K/4/1/X
-GNT5 R1745 1K/4/1

Close to ICH
as short as possible

U9B

10 DMI_0TXN DMI_0TXN V26
10 DMI_0TXP DMI_0TXP V25
10 DMI_0RXN DMI_0RXN C1863 0.1u/4/X7R/16V/K
10 DMI_0RXP DMI_0RXP C1864 0.1u/4/X7R/16V/K
DMI_ICH_IT_MR_0_DN U28
DMI_ICH_IT_MR_0_DP U27
10 DMI_1TXN DMI_1TXN Y26
10 DMI_1TXP DMI_1TXP Y25
10 DMI_1RXN DMI_1RXN C1865 0.1u/4/X7R/16V/K
10 DMI_1RXP DMI_1RXP C1866 0.1u/4/X7R/16V/K
DMI_ICH_IT_MR_1_DN W28
DMI_ICH_IT_MR_1_DP W27
10 DMI_2TXN DMI_2TXN AB26
10 DMI_2TXP DMI_2TXP AB25
10 DMI_2RXN DMI_2RXN C1867 0.1u/4/X7R/16V/K
10 DMI_2RXP DMI_2RXP C1868 0.1u/4/X7R/16V/K
DMI_ICH_IT_MR_2_DN AA28
DMI_ICH_IT_MR_2_DP AA27
10 DMI_3TXN DMI_3TXN AD25
10 DMI_3TXP DMI_3TXP AD24
10 DMI_3RXN DMI_3RXN C1869 0.1u/4/X7R/16V/K
10 DMI_3RXP DMI_3RXP C1870 0.1u/4/X7R/16V/K
DMI_ICH_IT_MR_3_DN AC28
DMI_ICH_IT_MR_3_DP AC27

DMI_0RXN
DMI_0RXP
DMI_0TXN
DMI_0TXP
DMI_1RXN
DMI_1RXP
DMI_1TXN
DMI_1TXP
DMI_2RXN
DMI_2RXP
DMI_2TXN
DMI_2TXP
DMI_3RXN
DMI_3RXP
DMI_3TXN
DMI_3TXP

22 PCIE_IN0 F26
22 PCIE_IP0 F25
22 PCIE_ON0 C1874 0.1u/4/X7R/16V/K E28
22 PCIE_OP0 C1875 0.1u/4/X7R/16V/K E27
33 ML_IN H26
33 ML_IP H25
33 ML_ON C1894 0.1u/4/X7R/16V/K G28
33 ML_OP C1895 0.1u/4/X7R/16V/K G27
34 PCIE_IN1 K26
34 PCIE_IP1 K25
34 PCIE_ON1 C1897 0.1u/4/X7R/16V/K J28
34 PCIE_OP1 C1898 0.1u/4/X7R/16V/K J27
34 PCIE_IN2 M26
34 PCIE_IP2 M25
34 PCIE_ON2 C1899 0.1u/4/X7R/16V/K L28
34 PCIE_OP2 C1900 0.1u/4/X7R/16V/K L27
P26
P25
N28
N27
T25
T24
R28
R27

PE0RXN
PE0RXP
PE0TXN
PE0TXP
PE1RXN
PE1RXP
PE1TXN
PE1TXP
PE2RXN
PE2RXP
PE2TXN
PE2TXP
PE3RXN
PE3RXP
PE3TXN
PE3TXP
PE4RXN
PE4RXP
PE4TXN
PE4TXP
PE5RXN
PE5RXP
PE5TXN
PE5TXP

ICH7 ONLY 4 LANE

VCC1_5 R173 24.9/4/1
C25 DMI_ZCOMP
D25 DMI_IRCOMP

21 -SRCCLK_ICH -SRCCLK_ICH AE28
21 SRCCLK_ICH SRCCLK_ICH AE27
DMICLKN
DMICLKP

USBP_0N F1 -USBP0 -USBP0 23
USBP_0P F2 +USBP0 +USBP0 23
USBP_1N G4 -USBP1 -USBP1 23
USBP_1P G3 +USBP1 +USBP1 23
USBP_2N H1 -USBP2 -USBP2 23
USBP_2P H2 +USBP2 +USBP2 23
USBP_3N J4 -USBP3 -USBP3 23
USBP_3P J3 +USBP3 +USBP3 23
USBP_4N K1 -USBP4 -USBP4 33
USBP_4P K2 +USBP4 +USBP4 33
USBP_5N L4 -USBP5 -USBP5 33
USBP_5P L5 +USBP5 +USBP5 33
USBP_6N M1 -USBP6 -USBP6 23
USBP_6P M2 +USBP6 +USBP6 23
USBP_7N N4 -USBP7 -USBP7 23
USBP_7P N3 +USBP7 +USBP7 23

OC_0# D3 -USBOC_F 23
OC_1# C4
OC_2# D5
OC_3# D4
OC_4# E5 -USBOC_R 33
GPIO29_OC_5# C3
GPIO30_OC_6# A2
GPIO31_OC_7# B3

USBRBIAS D1 R172 22.6/6/1
USBRBIAS# D2
CLK48 B2 USBCLK48 USBCLK48 21

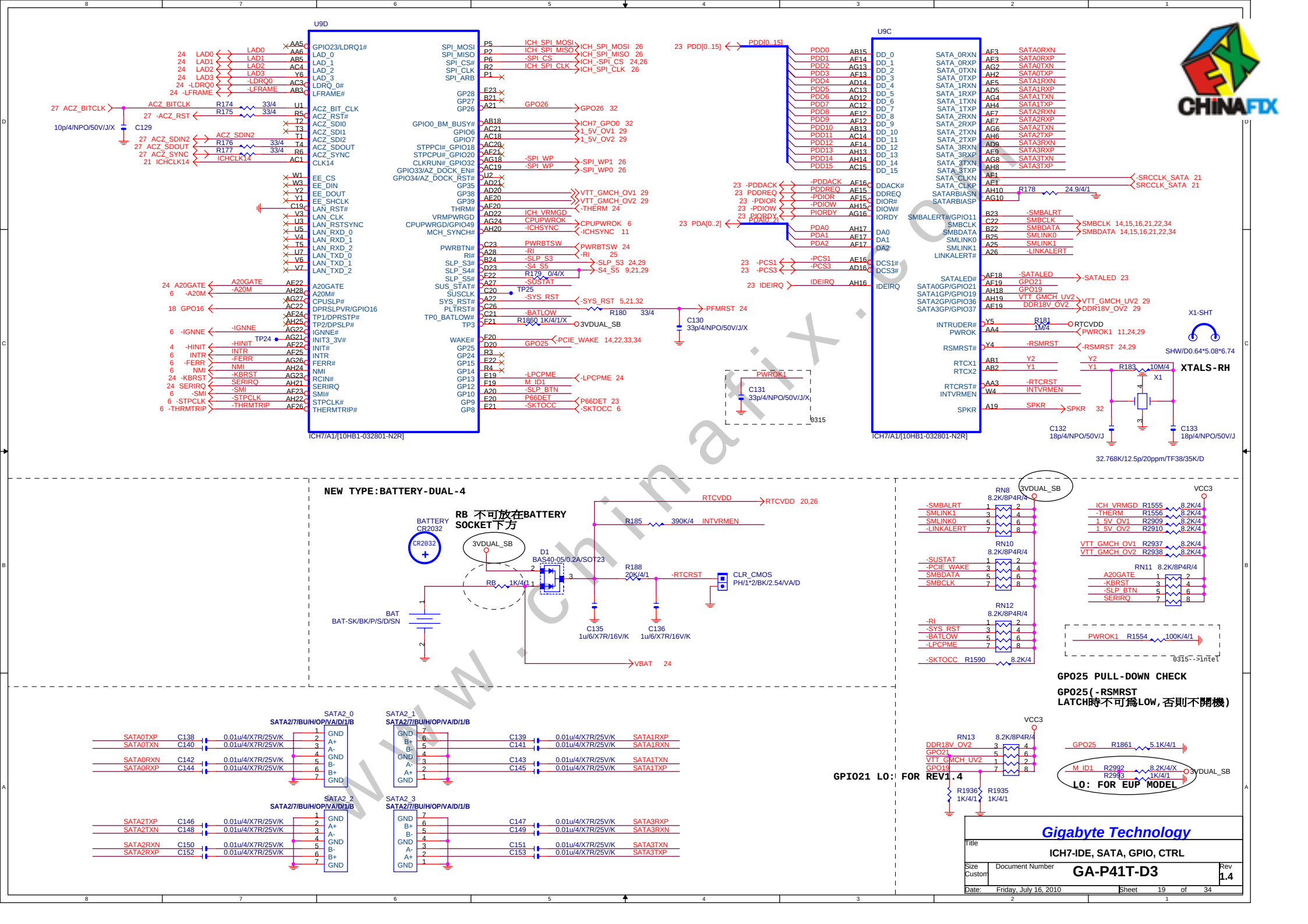
ICH7/A1/[10HB1-032801-N2R]

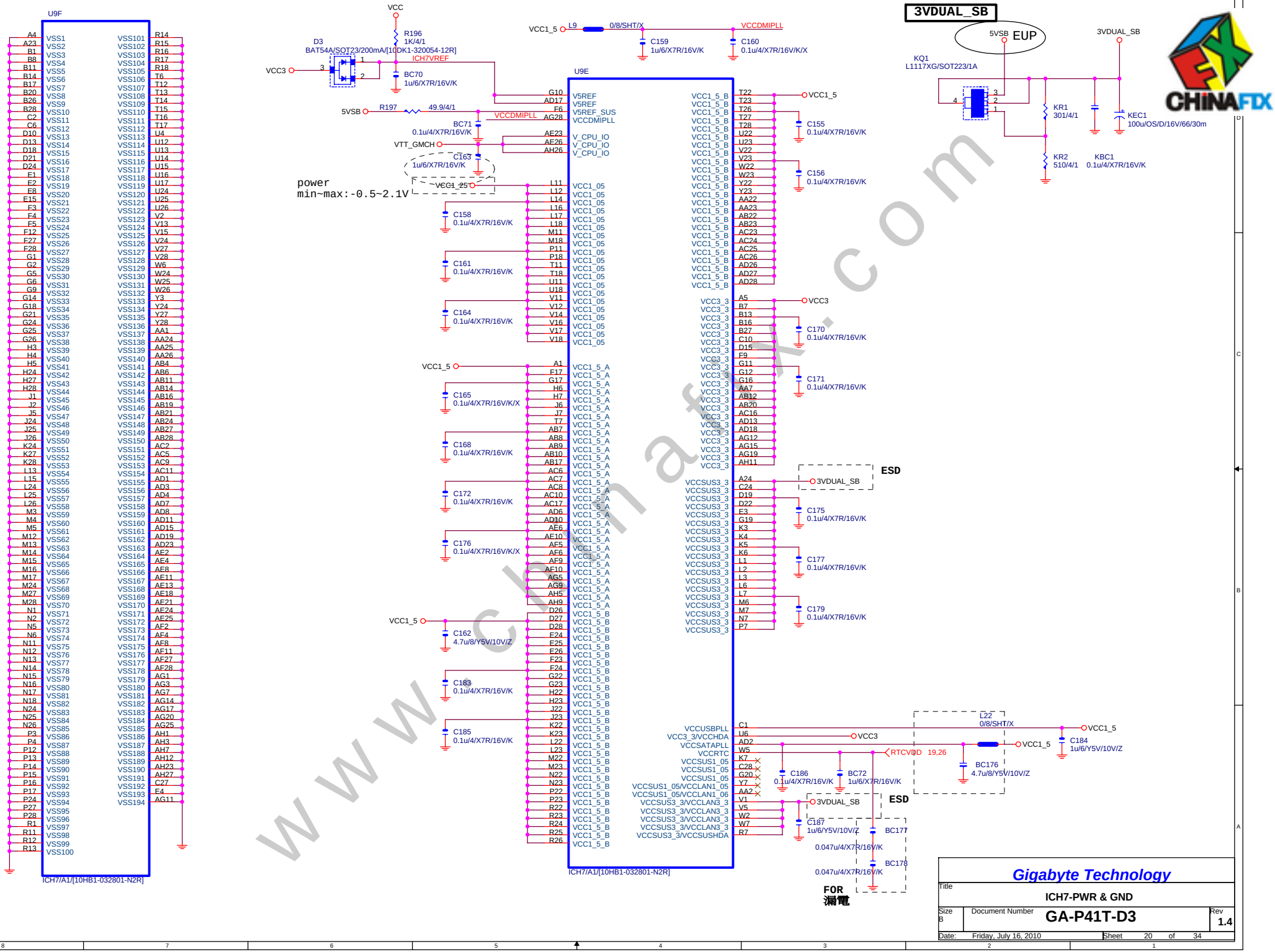
Gigabyte Technology

Title: ICH7-PCI, DMI, LAN, USB

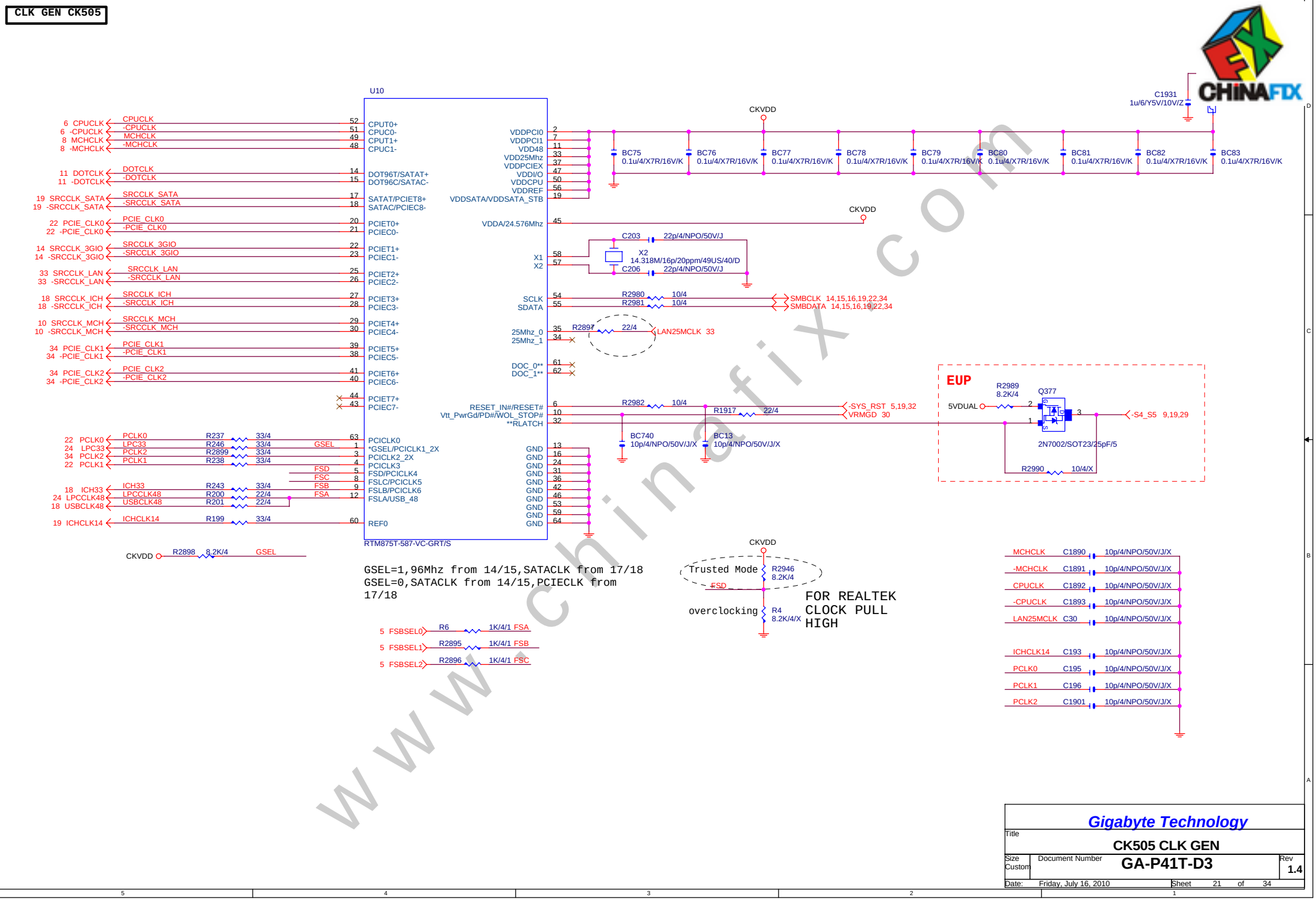
Size: B | Document Number: GA-P41T-D3 | Rev: 1.4

Date: Friday, July 16, 2010 | Sheet 18 of 34


U9D
ICH7/A1/[10HB1-032801-N2R]
U9C
ICH7/A1/[10HB1-032801-N2R]
NEW TYPE:BATTERY-DUAL-4
RB 不可放在BATTERY SOCKET下方
BATTERY CR2032
3VDUAL_SB
D1 BAS40-05/0.2A/SOT23
CLR_CMOS PH/1*2/BK/2.54/VA/D
BAT BAT-SK/BK/P/S/D/SN
RTCVDD
VBAT
SATA2_0 SATA2/7/BU/H/OP/VA/D/1/B
SATA2_1 SATA2/7/BU/H/OP/VA/D/1/B
SATA2_2 SATA2/7/BU/H/OP/VA/D/1/B
SATA2_3 SATA2/7/BU/H/OP/VA/D/1/B
GPIO21 LO: FOR REV1.4
GPO25 PULL-DOWN CHECK
GPO25(-RSMRST LATCH時不可爲LOW,否則不開機)
LO: FOR EUP MODEL
XTALS-RH
X1-SHT
32.768K/12.5p/20ppm/TF38/35K/D
Gigabyte Technology
ICH7-IDE, SATA, GPIO, CTRL
GA-P41T-D3
Rev 1.4
Friday, July 16, 2010
Sheet 19 of 34

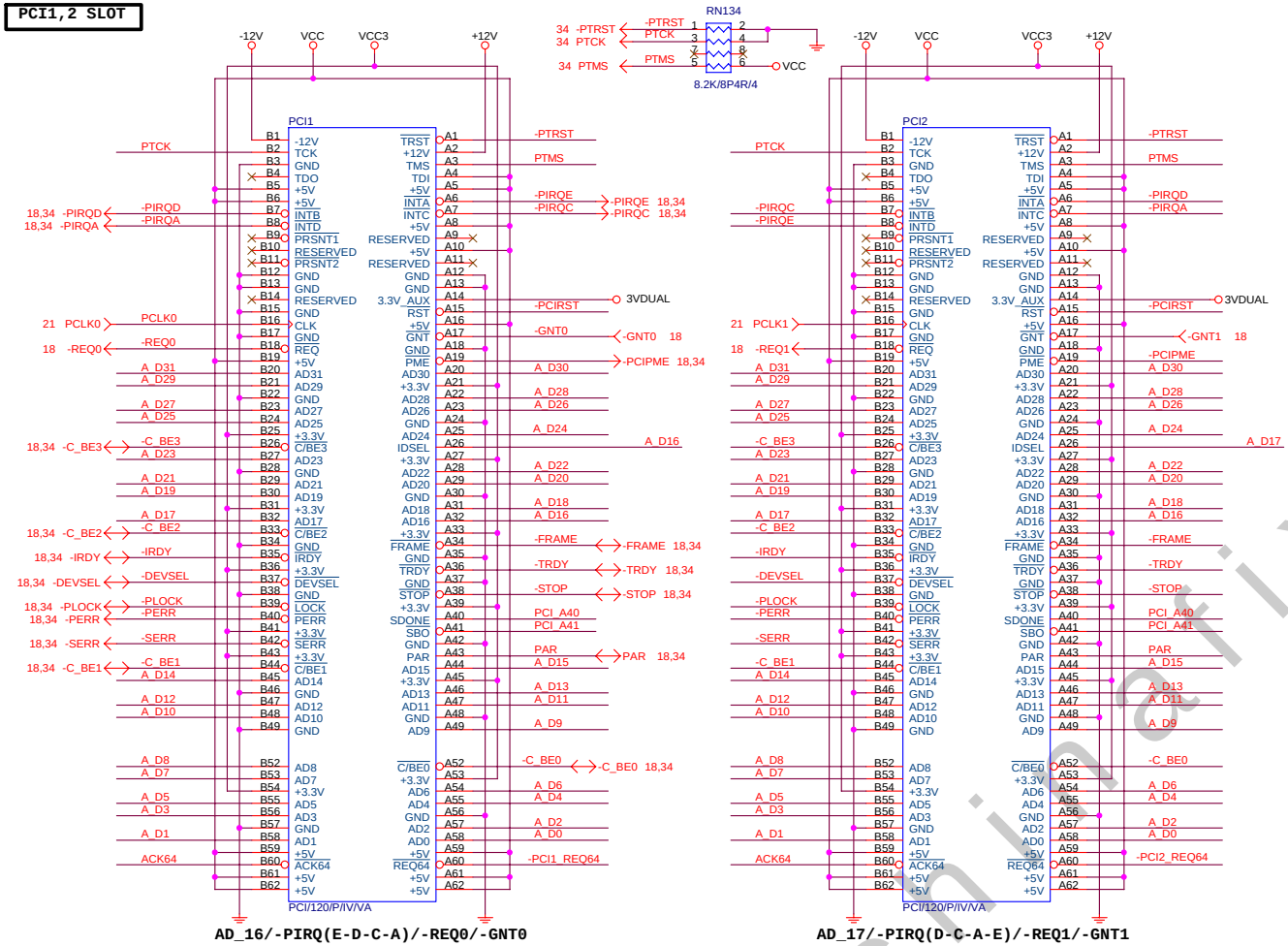


CLK GEN CK505



Gigabyte Technology		
Title: CK505 CLK GEN		
Size: Custom	Document Number: GA-P41T-D3	Rev: 1.4
Date: Friday, July 16, 2010	Sheet 21 of 34	

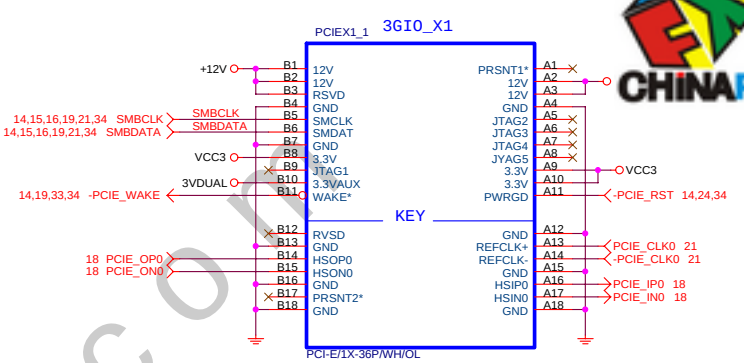
PCI1,2 SLOT

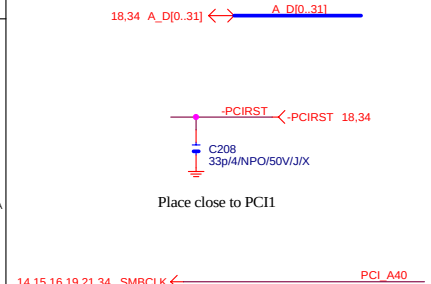


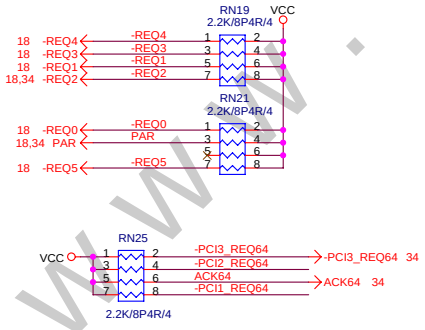
AD_16/-PIRQ(E-D-C-A)/-REQ0/-GNT0

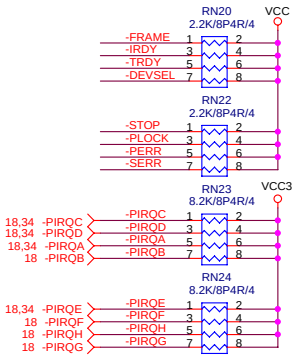
AD_17/-PIRQ(D-C-A-E)/-REQ1/-GNT1

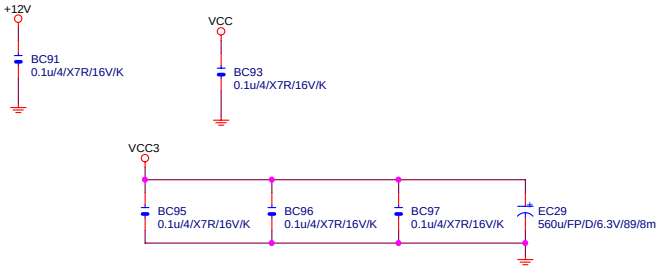
PCIE*1





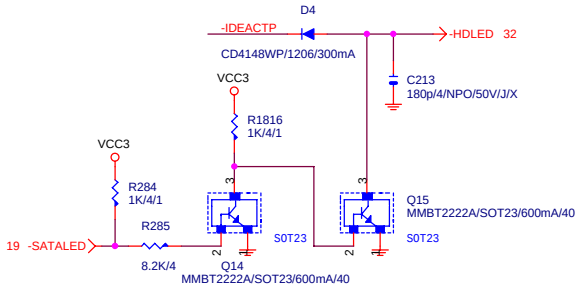




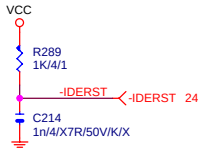


Gigabyte Technology			
Title	PCI SLOT 1, 2/PCIEX1		
Size: Custom	Document Number: GA-P41T-D3		Rev: 1.4
Date: Friday, July 16, 2010	Sheet 22 of 34		

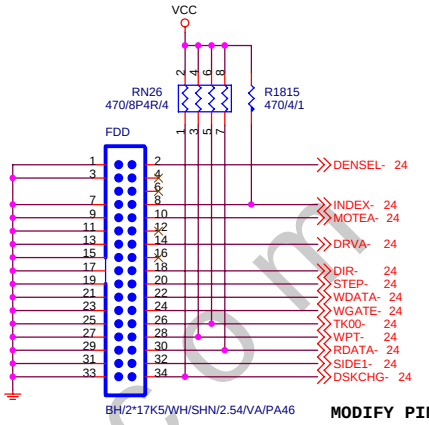
IDE/SATA LED



IDE RESET

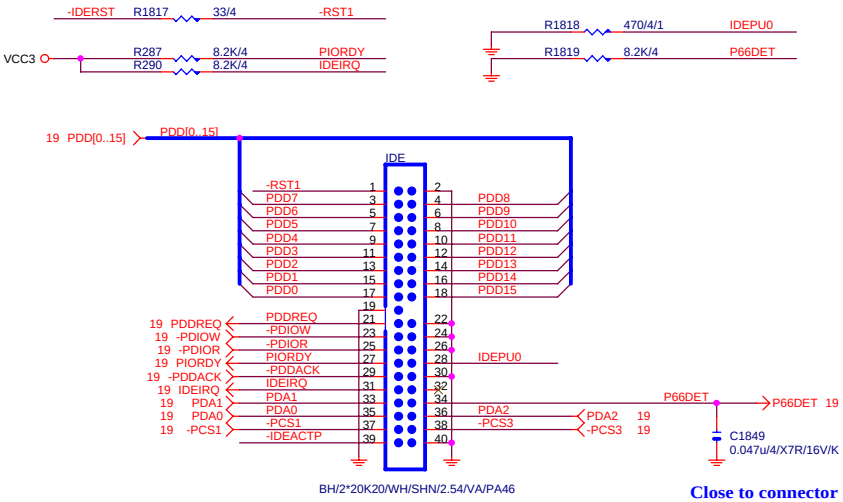


FLOPPY



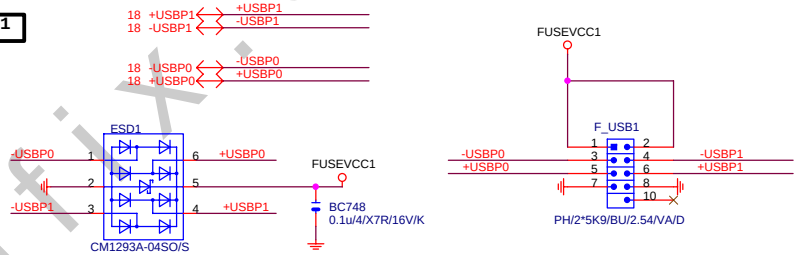
MODIFY PIN HEADER

IDE

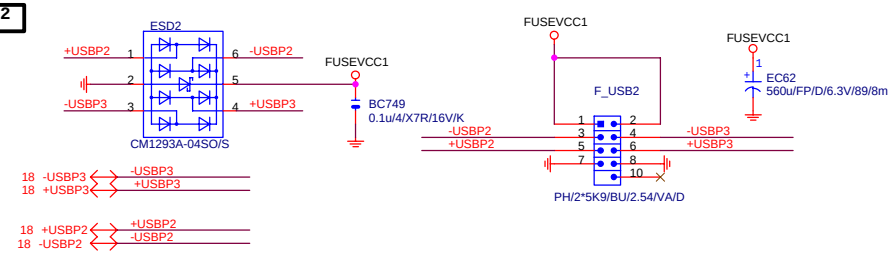


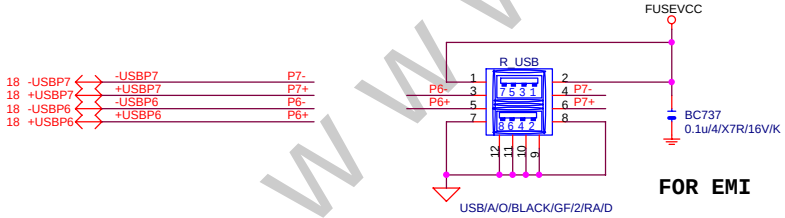
Close to connector

FRONT USB1

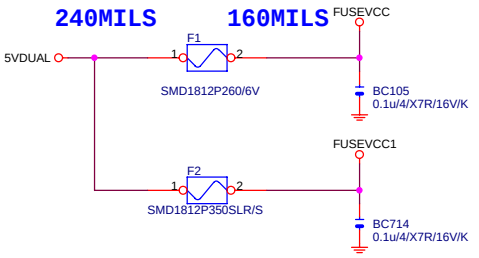


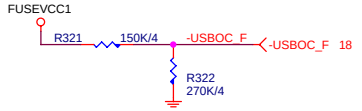
FRONT USB2





FOR EMI





Gigabyte Technology		
Title: IDE,FDD,F_USB		
Size: B	Document Number: GA-P41T-D3	Rev: 1.4
Date: Friday, July 16, 2010	Sheet 23 of 34	

RTS2- ==LOW CPU FAN 50%
==HIGH 100%
DEFAULT 50%

VCC R1561 8.2K/4/X DTR2- R1562 8.2K/4/X RTS2- R1587 680/4 0302-UP

SOUT2		
	1	VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8V
	0	VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4V

PUSH-PULL D68 BAT54A/SOT23/200mA/[10DK1-320054-12R]/X VCC R2920 1K/4/1/X DTR2- RTS2-
33 GP64
R347 680/4 DTR2- R348 680/4 TXD2 FOR LAN 8111C TXD2
29 DDR18V_OV3 32 FANIO1 32 FANIO2 32 FANIO3 32 FANPWM3 30 IO_VID5 30 IO_VID4 30 IO_VID3 30 IO_VID2 30 IO_VID1 30 IO_VID0 4 GTLREF_UV0 4 GTLREF_UV1 32 FANIO4 5 BSEL166_3 29 EUP_N 29 DDR18V_OV1 29 VTT_GMCH_UV1 5 BSEL166_4 30 IO_VIDO6

IT8712F/[IT8718F]

VCC R1896 220/6 -RST_BT 19,26 ICH_-SPI_CS
18 -RST_BTN
14,22,34 -PCIE_RST 11,19,29 PWROK1 11,33 -PFMRST1 -PCIE_RST_F ITE_PWROK -PFMRST1_F -PFMRST2_F
VCC VCC3 19 -PFMRST 19 -LDRQ0 -PFMRST -LDRQ0
R1565 8.2K/4 VCC3
BC731 1u/6/Y5V/10V/Z
19 SERIRQ 19 -LFRAME LAD[0..3] 19 LAD[0..3]
19 -KBRST 19 A20GATE 21 LPC33 21 LPCCLK48
C230 10p/4/NPO/50V/J/X
-PFMRST -PFMRST 19
BC121 100p/4/NPO/50V/J/X

VCC3 RN140 2 4 6 8 1 3 5 7 -PFMRST2_F -PCIE_RST_F ITE_PWROK -PFMRST1_F 1K/8P4R/4

Pop to disable Dual BIOS
-SIO_SPI_CS0 R2926 0/4/X ICH_-SPI_CS
26 -SIO_SPI_CS1 R2927 22/4 CEB_N
26 -SIO_SPI_CS0 R2928 0/4/SHT/X -RST_BT

Dual BIOS:
GB logo :Pin 61 (GP15/CSA)
GB logo :Pin 59 (GP17/CSB)

Pin 59 Dual BIOS ,Power On Strapping:
H ==>Dual BIOS function Enable
L ==>Dual BIOS function Disable

1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接3.3V
LPCPD#=VIDVCC

25 DCD1- 25 RI1- 25 CTS1- 25 DTR1- 25 RTS1- 25 DSR1- 25 TXD1 25 RXD1 19 -THERM 29 1_1V_OV1 29 1_1V_OV2
PD[0..7] PD[0..7] 25
STB- AFD- ERR- INIT- SLIN- ACK- STB- 25 AFD- 25 ERR- 25 INIT- 25 SLIN- 25 ACK- 25

U15
BUSY PE SLCT VCC/[AVCC] VIN0 VIN1 VIN2 VIN3/ATXPG VIN4 VIN5/[VID7] VIN6/[VID6] VIN7/PCIRSTIN# VREF TMPIN1 TMPIN2 TMPIN3/[SO1] GNDA RSMRST#/CIRRX/GP55 PCIRST4#/SCRPRES#/GP10 MCLK/[GP56] MDAT/[GP57] KCLK/[GP60] KDAT/[GP61] 3VSBSW#/GP40 PWROK2/GP41 RING#/GP53/SUSC# PSON#/GP42 PANSWH#/GP43 GNDD PME#/GP54 PWRON#GP44 PSIN/GP45/SUSB# IRRX/GP46 VBAT COPEN# VCCH IRTX/GP47/CEB_N/JP7 for dual DB DSKCHG#
BUSY 25 PE 25 SLCT 25 VCC PWOK VIN0 26 VIN1 26 VIN2 26 PWOK 31 VIN4 26 VID7 6 VID6 6 VIN7 26 VREF 26 SYS_TEMP 26 PWM_TEMP 26
BC717 1u/6/Y5V/10V/Z FIX TEMP RANDOM
PWOK C228 1n/4/X7R/50V/K/X
CPU_TEMP 6 THERMDC 6
R1821 33/4 -RSMRST 19,29 -IDERST 23 MCLK 26 MDAT 26 KCLK 26 KDAT 26 BSEL166_1 5 BSEL166_2 5
R1913 0/6/SHT/X BC117 2.2n/4/X7R/50V/K 5VSB
R352 8.2K/4
R2890 33/4 -PWRBTSW 32 -PSON 29,31
-LPCPME 19 PWRBTSW 19
-SLP_S3 19,29 BEEP- 32
R1916 10/4 -CASEOPEN 26,32 5VSB VBAT 19 C229 1u/6/Y5V/10V/Z R359 8.2K/4 3VDUAL_SB
BC118 BC119 BC730 1u/6/Y5V/10V/Z 4.7u/8/Y5V/10V/Z 0.047u/4/X7R/16V/K
DSKCHG- 23
IT8718F-S/LX(GB)/S/[10HP2-118718-E0R_10HP2-118718-C0R] VCC3
CEB_N R2925 220/6
R1909 1K/4/1/X

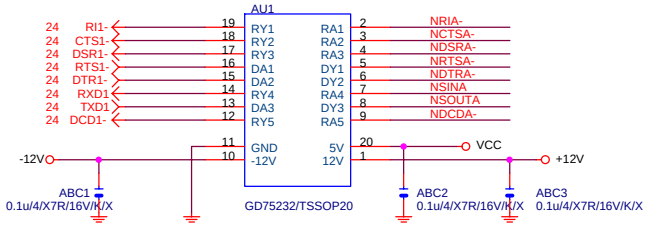
JP7 : HIGH DUAL BIOS ENABLE
LOW DUAL BIOS
DISABLE

WPT- 23 INDEX- 23 TK00- 23 RDATA- 23 WGATE- 23 SIDE1- 23 STEP- 23 DIR- 23 WDATA- 23 PECI 6 DRVA- 23
MOTEA- 23 DENSEL- 23 IO_VIDO7 30

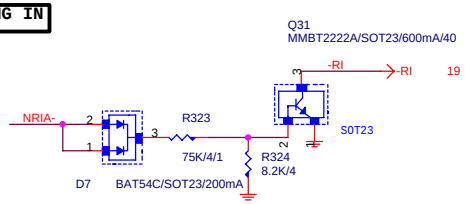
如果BSEL0/1 直接拉TO N/B,R264/R265 不上
5VSB RN163 8.2K/8P4R/4 1 3 5 7 2 4 6 8 BSEL166_3 BSEL166_2 BSEL166_4 BSEL166_1

Gigabyte Technology
Title: ITE 8718 LPC IO
Size B | Document Number: GA-P41T-D3 | Rev 1.4
Date: Friday, July 16, 2010 | Sheet 24 of 34

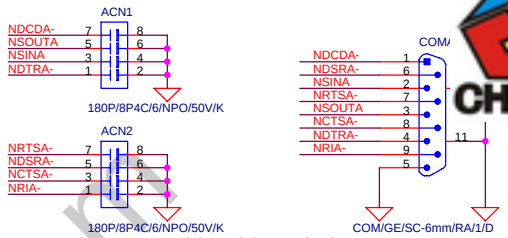
COMA



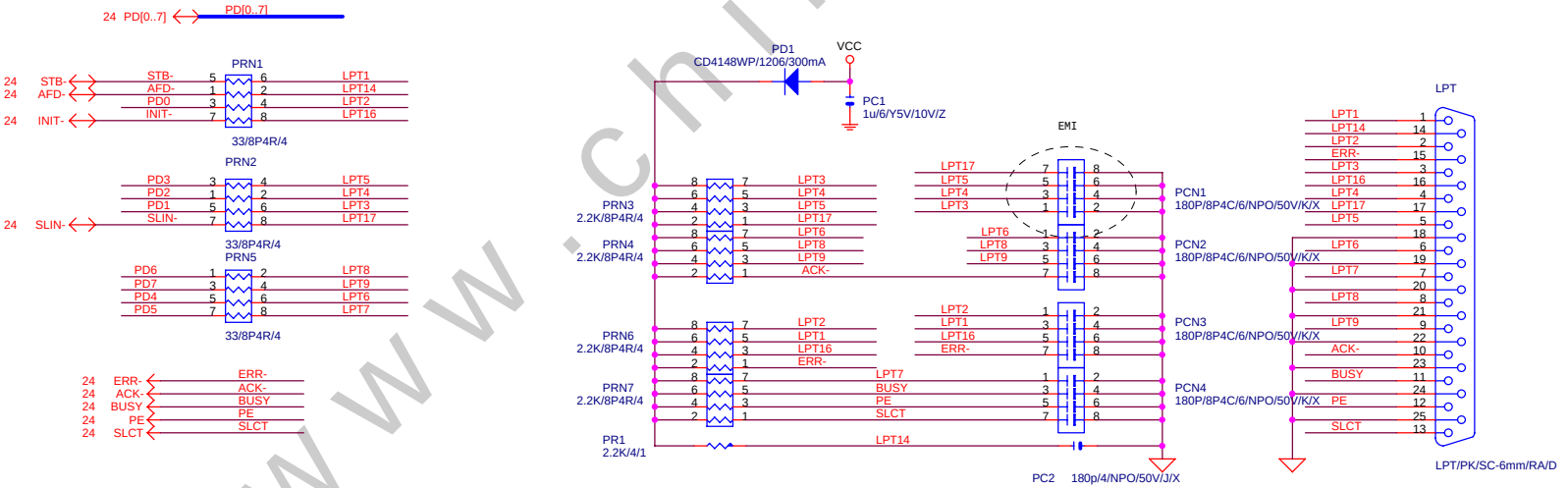
RING IN



EXTERNAL COMA

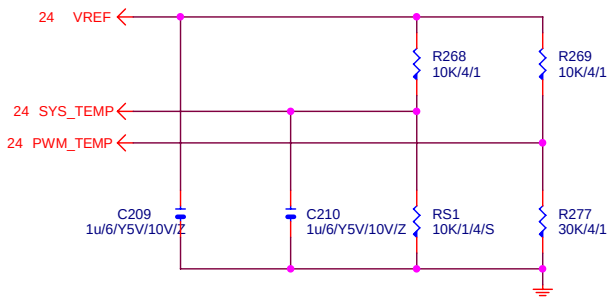


LPT PORT

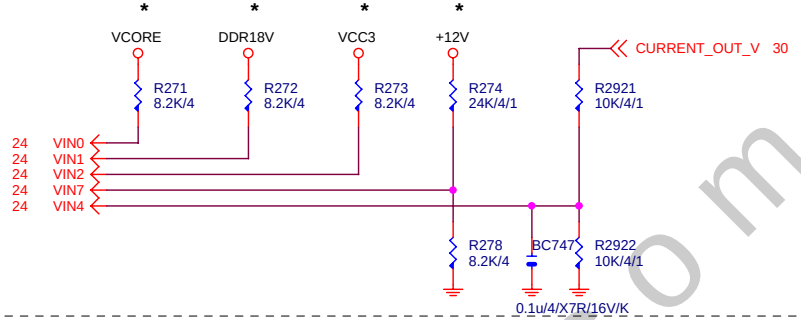


Gigabyte Technology		
Title: COM & LPT PORT		
Size: B	Document Number: GA-P41T-D3	Rev: 1.4
Date: Friday, July 16, 2010	Sheet 25 of 34	

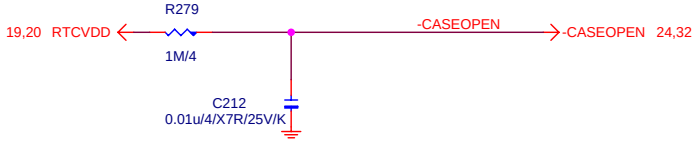
TEMP H/W MONITOR



VOLTAGE-- H/W MONITOR

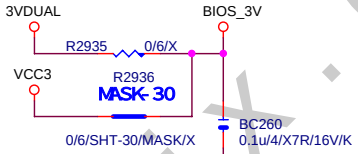


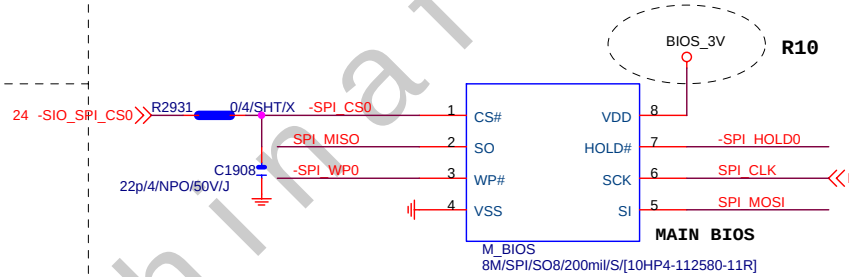
CASE OPEN

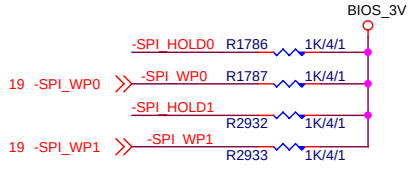


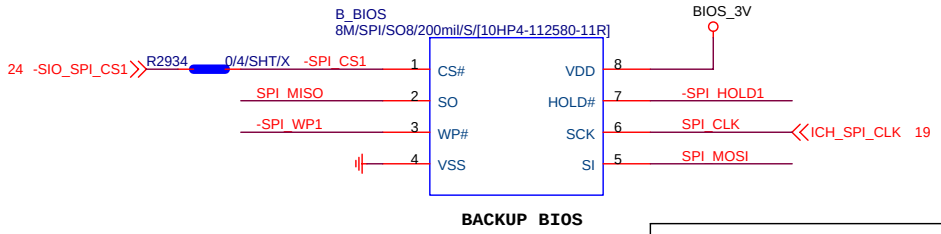
Case Open Circuits

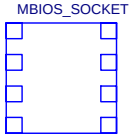
DUAL BIOS



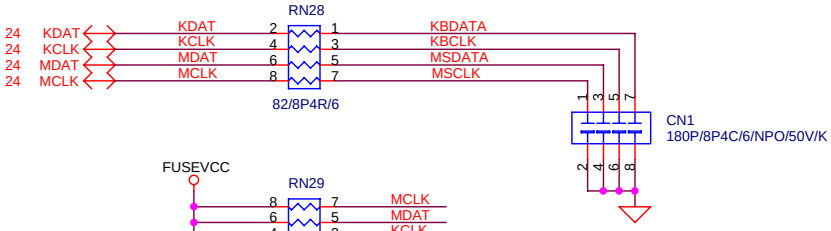


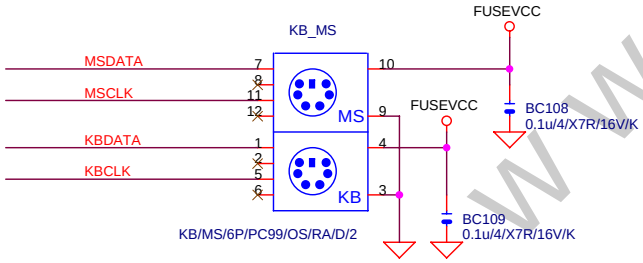






KB/MS





Gigabyte Technology		
Title: HW-MONITOR/CI/KB/MS/BIOS		
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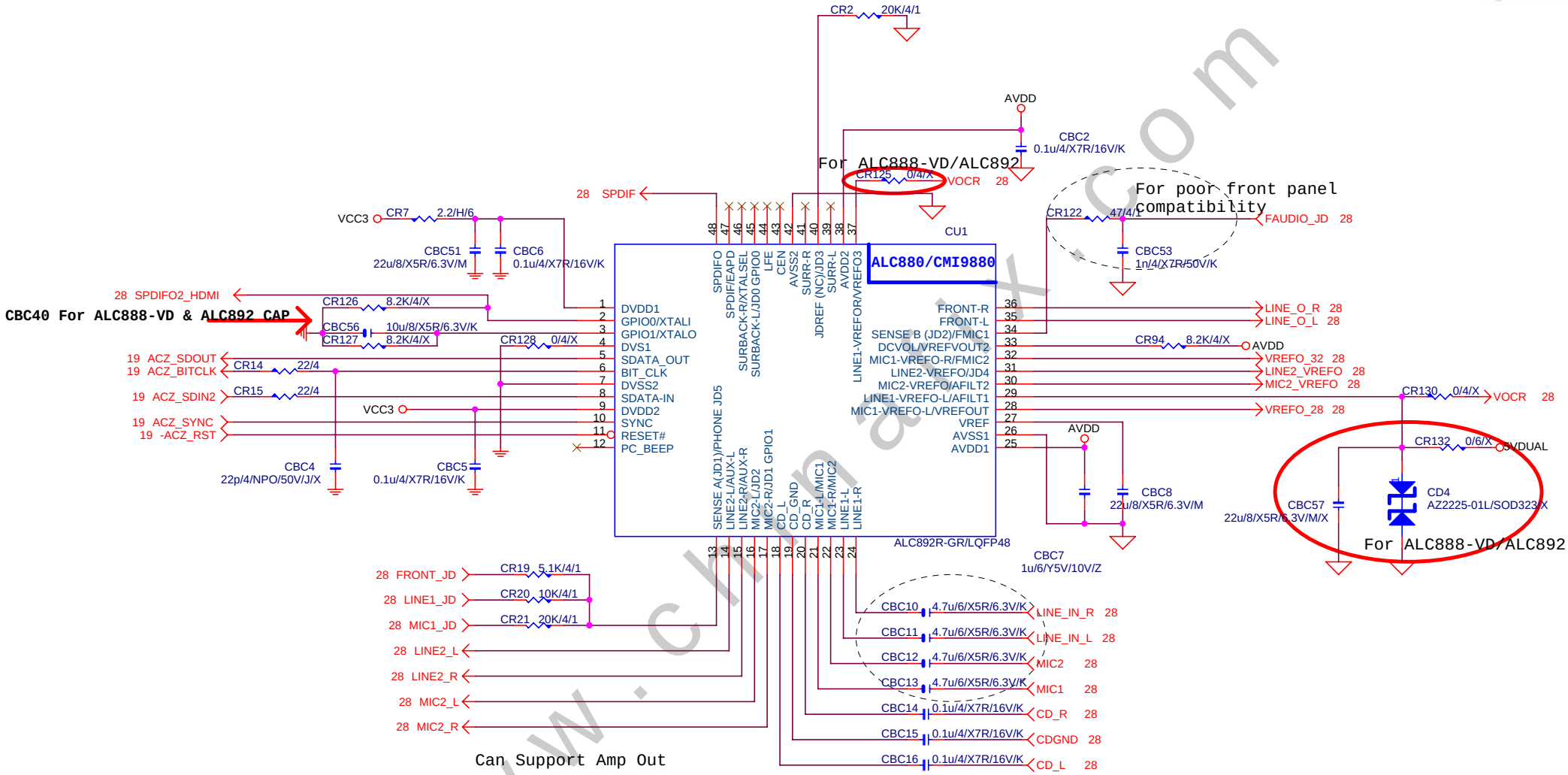
AZALIA CODEC



Gigabyte Technology		
Title: AZALIA ALC888		
Size: Custom	Document Number: GA-P41T-D3	Rev: 1.4
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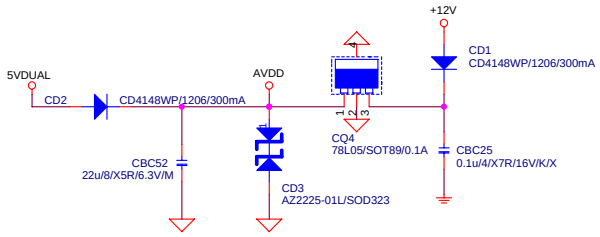
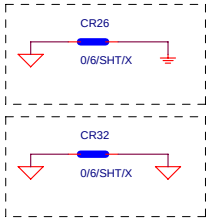
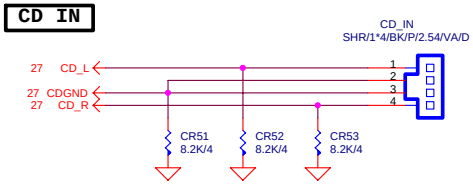
CODEC POWER/EMI PAD

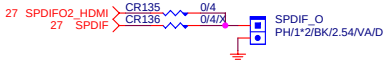




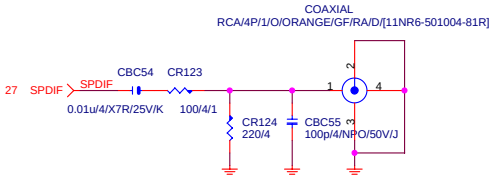
CD IN



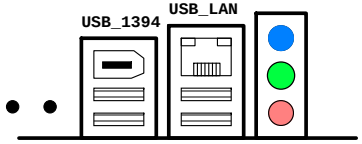
SPDIF

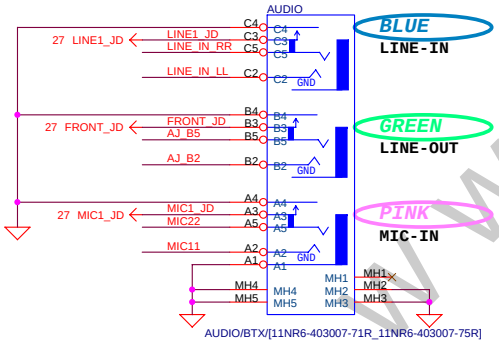


PIN HEADER 1X2

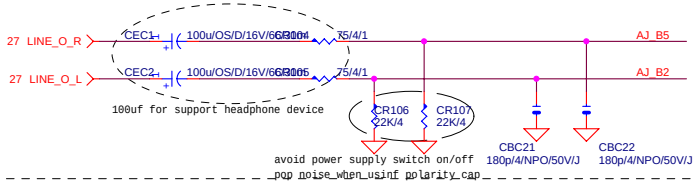


AZALIA JACK





LINE-OUT



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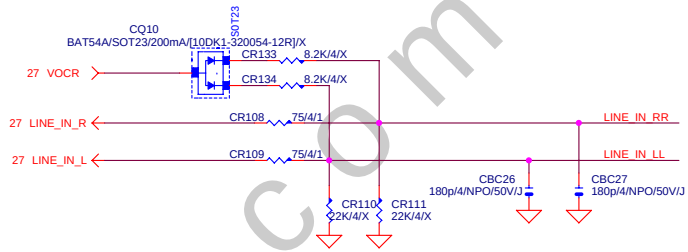
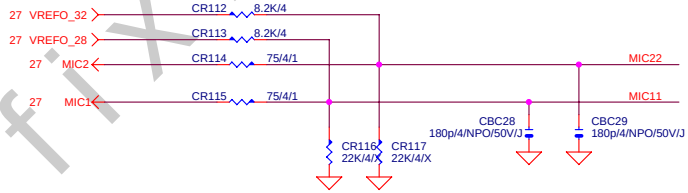
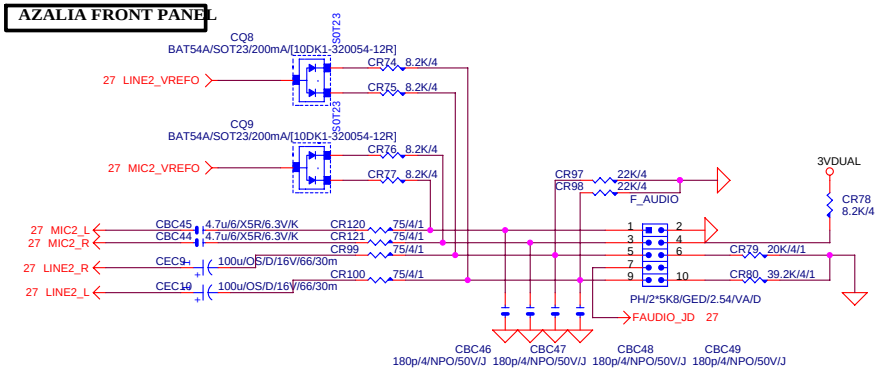


MIC-IN



AZALIA FRONT PANEL



Gigabyte Technology

Title	AUDIO JACK	
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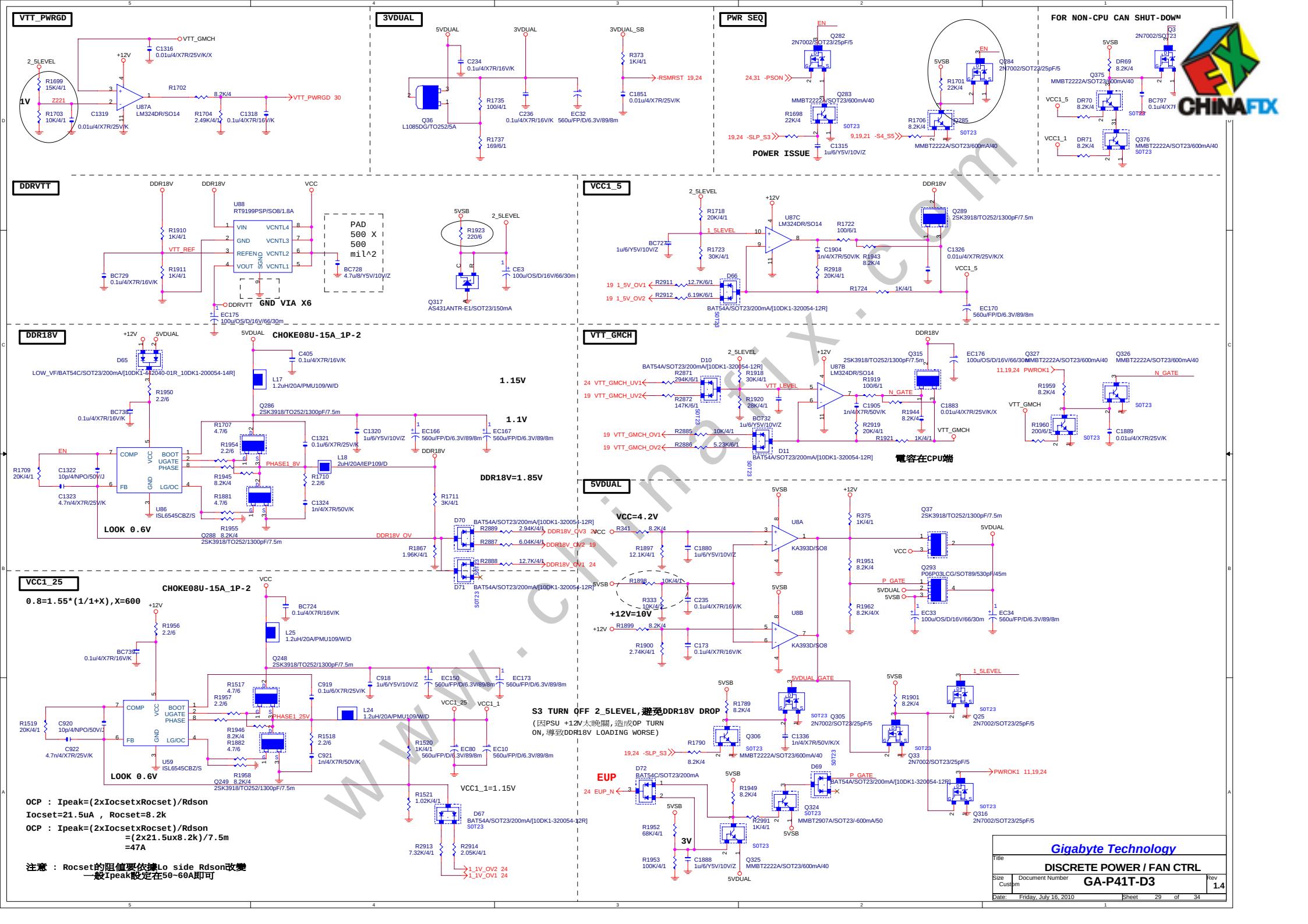

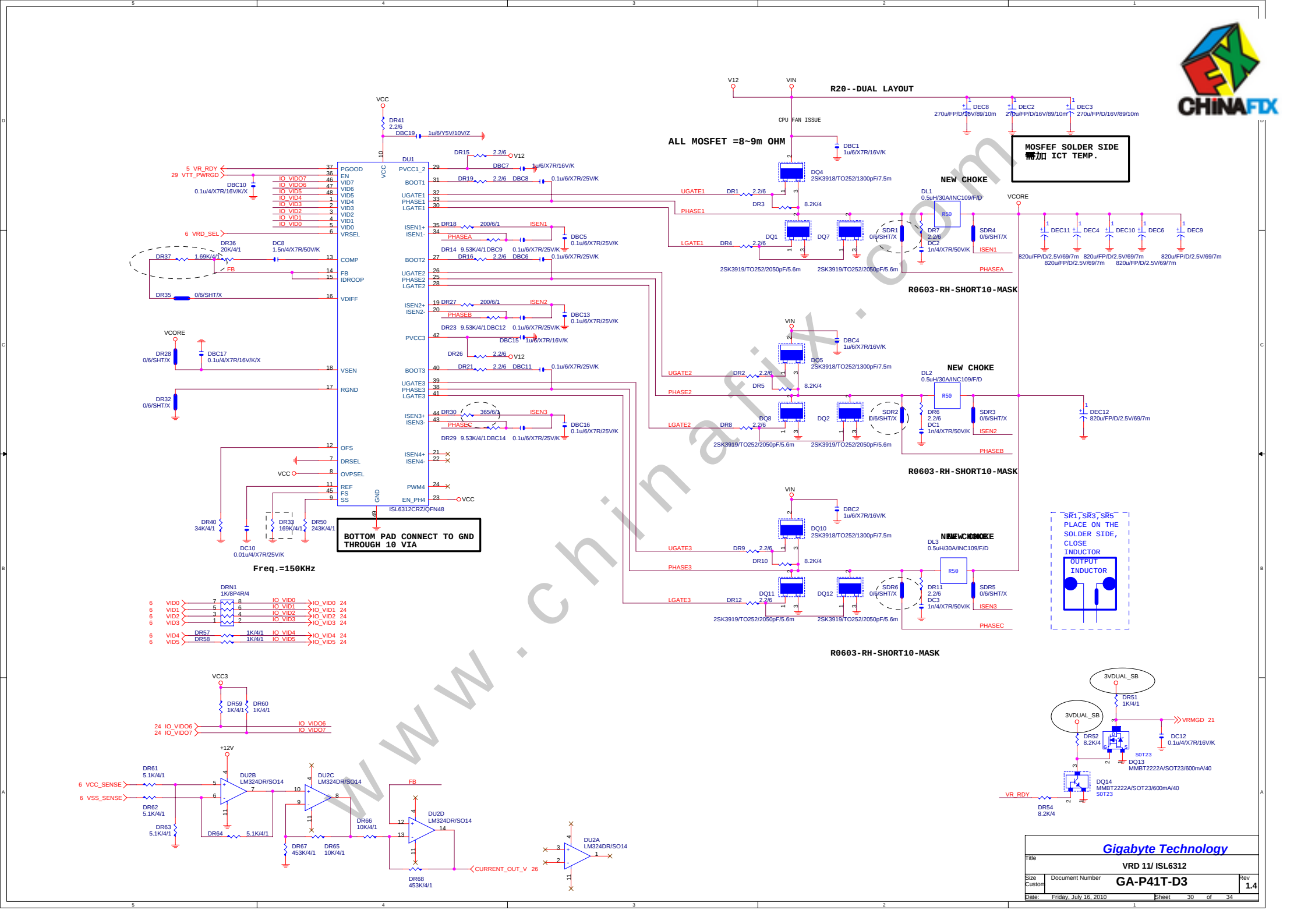
R20--DUAL LAYOUT
ALL MOSFET =8~9m OHM
MOSFEF SOLDER SIDE 靠加 ICT TEMP.
NEW CHOKE
R0603-RH-SHORT10-MASK
BOTTOM PAD CONNECT TO GND THROUGH 10 VIA
Freq.=150KHz
SR1,SR3,SR5 PLACE ON THE SOLDER SIDE, CLOSE INDUCTOR
OUTPUT INDUCTOR
ISL6312CRZ/QFN48
Gigabyte Technology
VRD 11/ ISL6312
GA-P41T-D3
Rev 1.4
Friday, July 16, 2010
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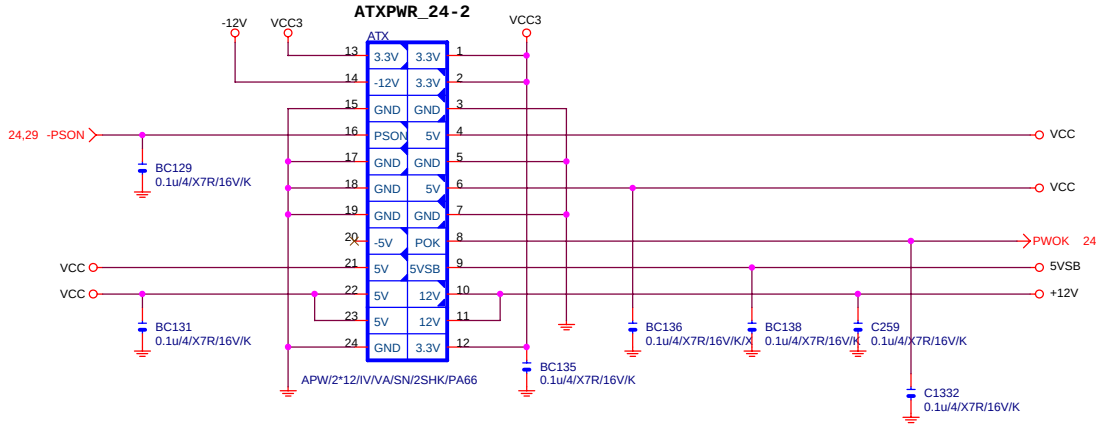
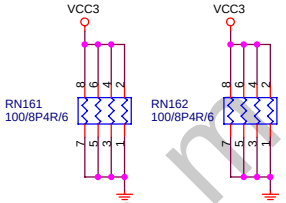
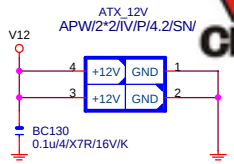
ATX POWER CONNECTOR

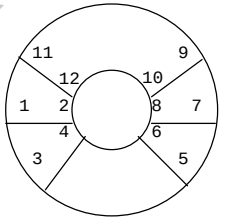


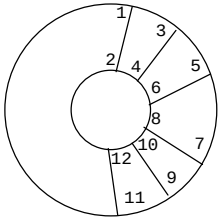
FIX PWR AcBel(ATX-400C-A2ADB)

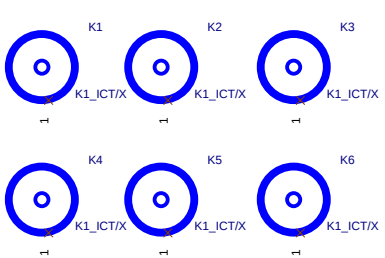


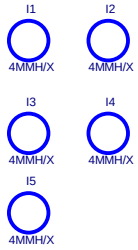


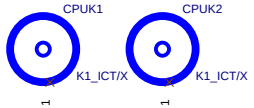
ATX_4-1

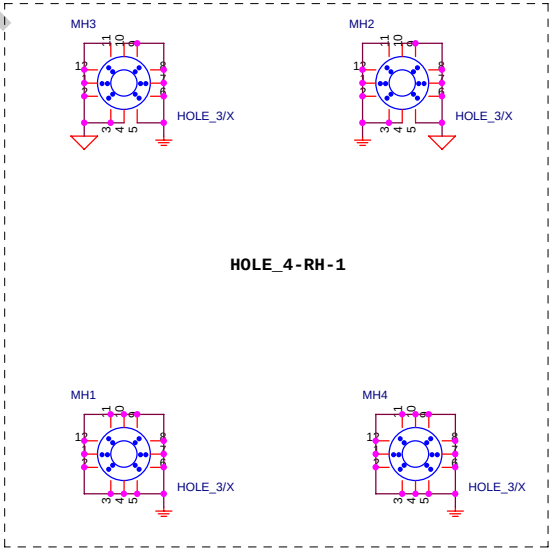




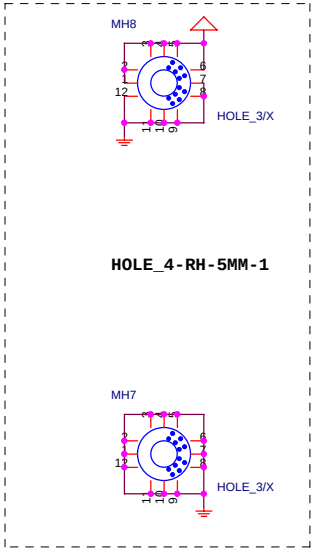




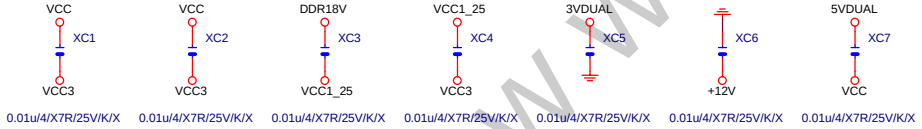




HOLE_4-RH-1



HOLE_4-RH-5MM-1



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Title: ATX POWER CONNECTOR		
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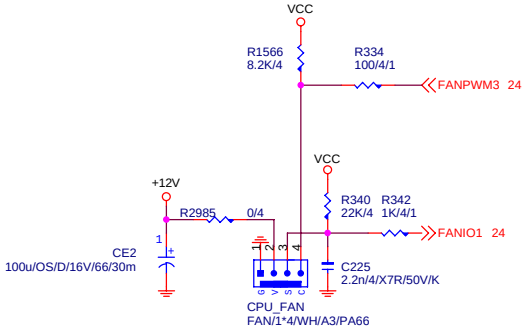
CPU SMART FAN

SMART FAN

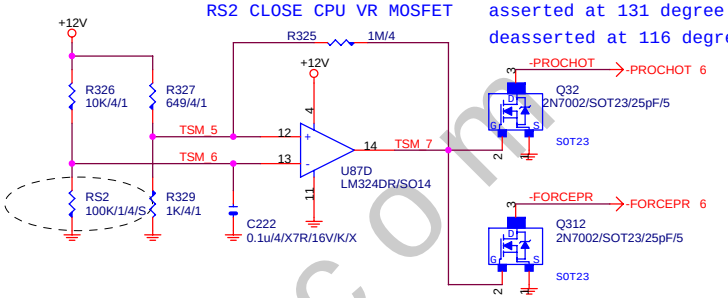


PROCESSOR HOT

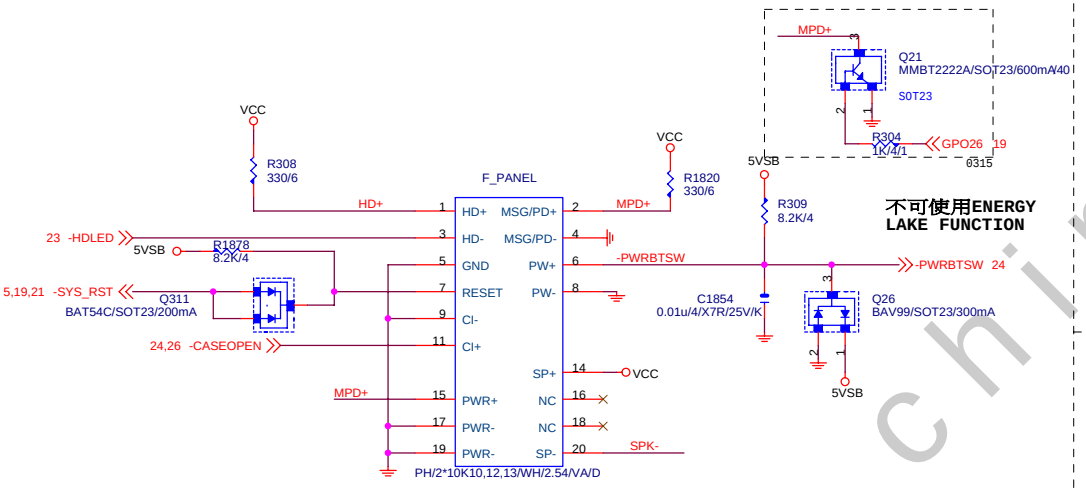
RS2 CLOSE CPU VR MOSFET

asserted at 131 degree

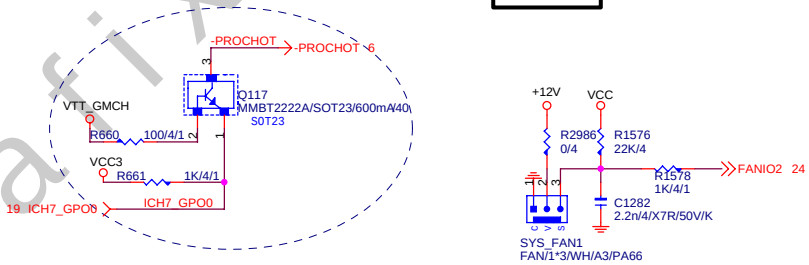
deasserted at 116 degree



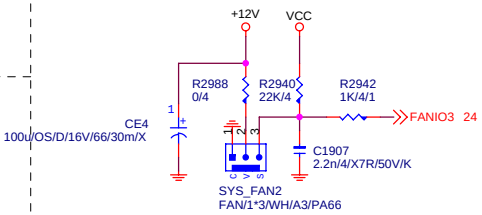
INTEL FRONT PANEL



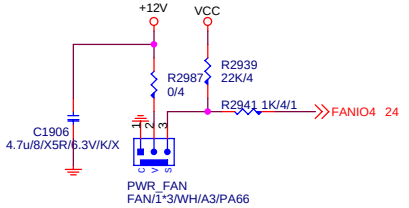
SYS_FAN1



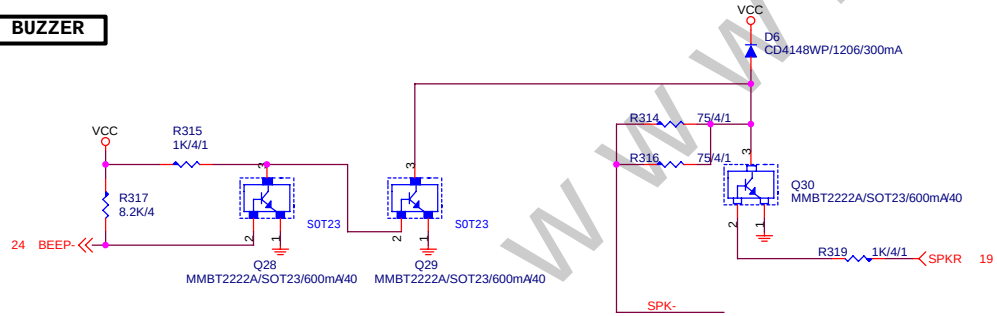
SYS_FAN2



PWR FAN



BUZZER



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Title: FRONT PANEL / FAN CTRL

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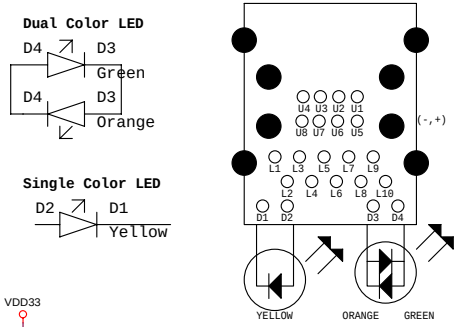
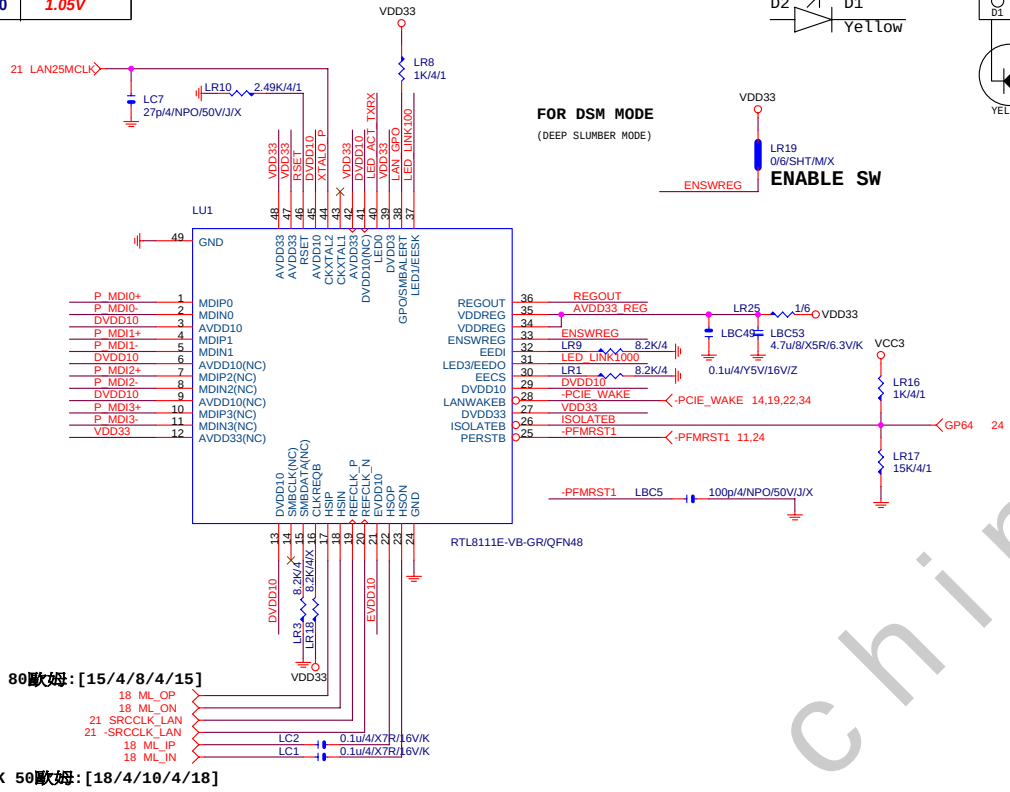
PCIE-1G LAN

Power domain chart

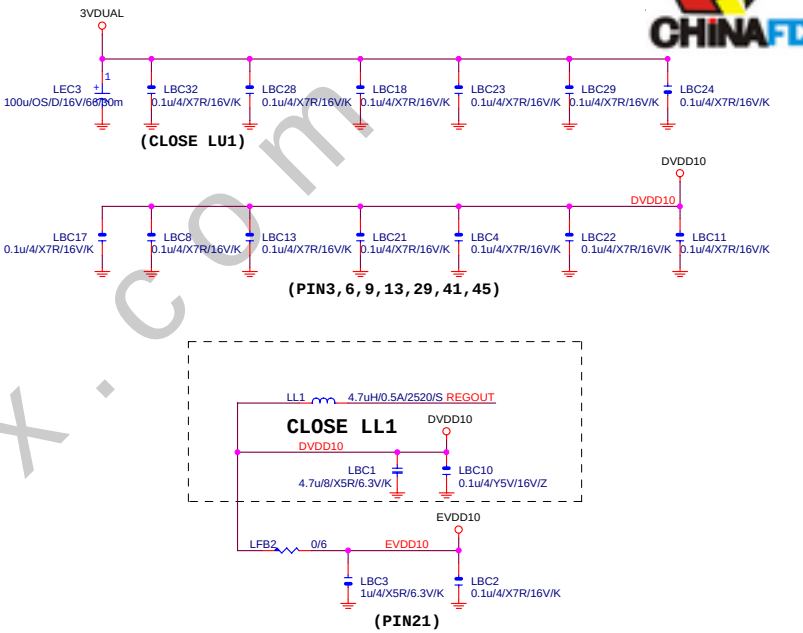
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V





FOR DSM MODE

(DEEP SLUMBER MODE)



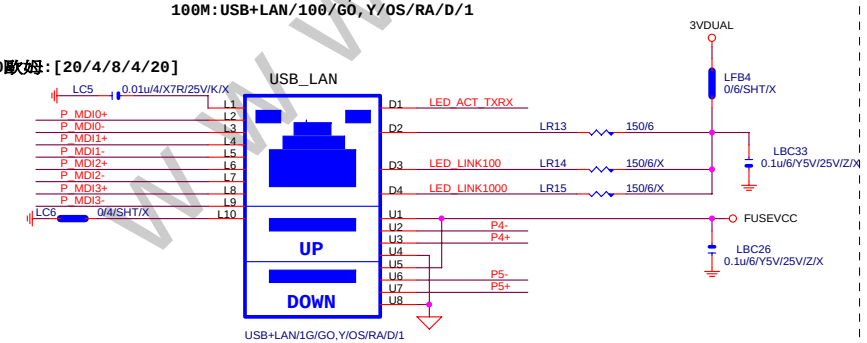
USB_LAN CONNECTOR

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

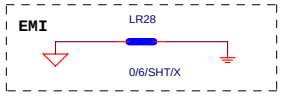
1G :USB+LAN/1G/GO,Y/OS/RA/D/1

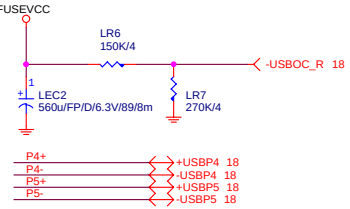
100M:USB+LAN/100/GO,Y/OS/RA/D/1

100歐姆:[20/4/8/4/20]



USB_LAN





Gigabyte Technology

Title: REALTEK RTL8111E

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