Starlord KBL_Refresh Schematics
KabyLake-R

2017-05-25
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Cover Page*		
Size: A3	Document Number: Starlord KBL-R	Rev: A00
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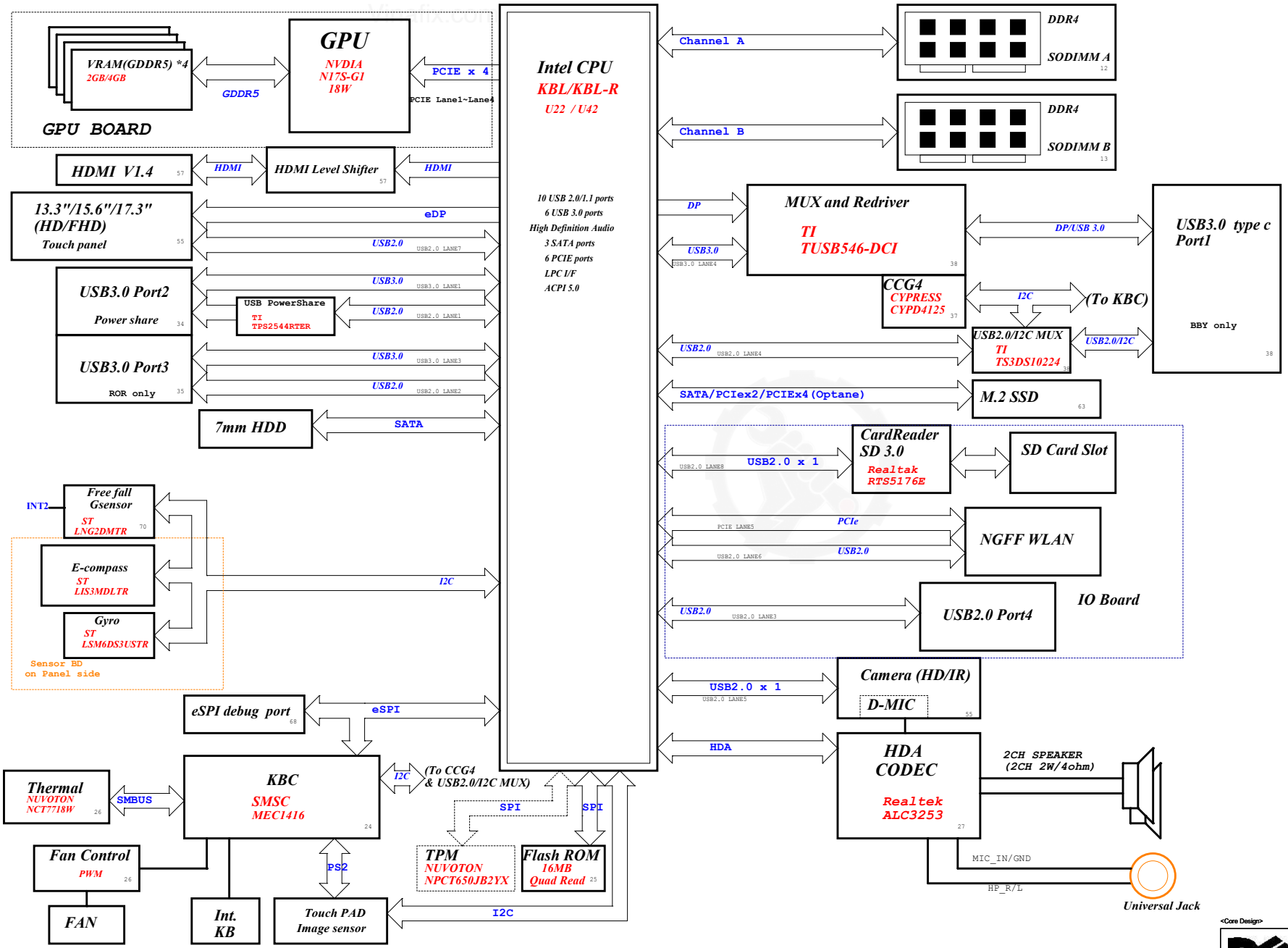
Project code: 4PD0CF010001(SL13_R)
4PD0CG010001(SL15_R)
4PD0CH010001(SL17_B)

Star lord KBL Block Diagram

PCB P/N: 16888
Revision: A00

	SENSOR	IO	MB
ROR	17A18-SA	17A17-SA	17810-1
BBY	17A18-SA	17A16-SA	16888-1



CHARGER — ISL88739 — 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC — SY8288CRAC-GP — 45

INPUTS	OUTPUTS
DCBATOUT	PWR_5V 5V_S5 5V_AUX_S5

CPU Core Power — NCP81208MNTXG-GP 46~50, NCP81382MNTXG-1-GP, NCP81382MNTXG-1-GP, NCP81253MNTBG-GP

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCSA_VR

DDR4 — SY8288RAC-GP, APL5338XAI-TRG-GP — 51

INPUTS	OUTPUTS
DCBATOUT	1D2V_S3 0D675V_S0

CPU DCDC-V1D00A — AOZ1268QI-02-GP — 52

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D5V — S-1339D15-M5001-GP — 54

INPUTS	OUTPUTS
3D3V_S5	1D5V_S0

LDO-V1D8V — APL5930KAI-TRG-GP — 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0 — G5016KD1U — 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

VCCSTG — M5938ARD1U-GP-U — 40

INPUTS	OUTPUTS
1D0V_S5	+VCCSTG

VCCST — TPS22965DSGR-GP-U — 40

INPUTS	OUTPUTS
1D0V_S5	+V1.00U_CPU

SYSTEM DC/DC — TPS51225RUKR-GP — 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 PWR_3D3V

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Title: Block Diagram
Size: C | Document Number: Starlord KBL-R | Rev: A00
Date: Monday, August 28, 2017 | Sheet 2 of 106

SSID = CPU

(Blanking)

<Core Design>

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Title: *(Reserved)*		
Size: A3	Document Number: *Starlord KBL-R*	Rev: *A00*
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SSID = CPU

#544669 CRB Rev0.52

+VCCSTG = 1.0 V

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

Vince,20170106
[24] H_PECI_CPU
[24,44,45] H_PROCHOT#

Vince,20161107

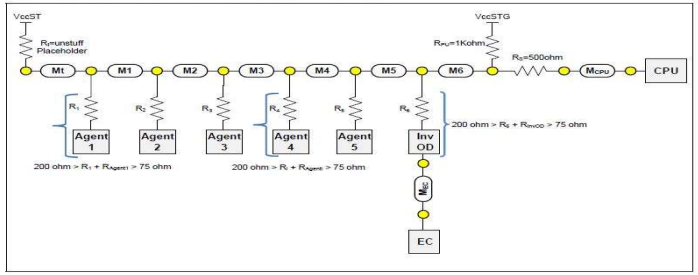
Vince,20161031

Vince,20161031
65] TP_WAKE_KBC#

Add resistor by NON DS3 function

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

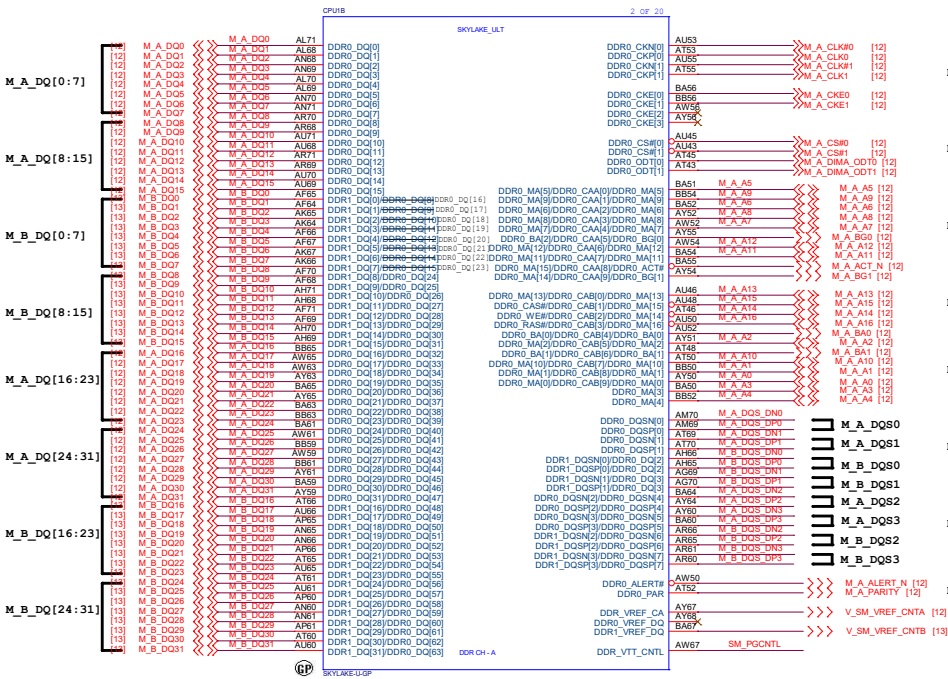
Title: CPU_(JTAG/CPU SIDE BAND)

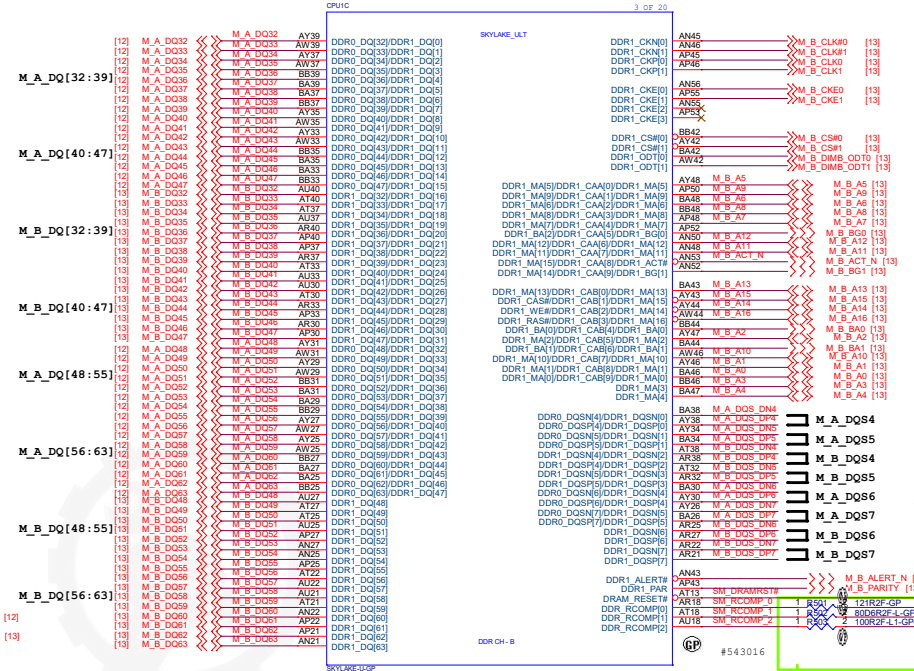
Size	Document Number	Rev
A3	Starlord KBL-R	A00

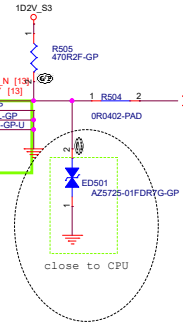
Date: Friday, December 08, 2017 Sheet 4 of 106

SSID = CPU

DDR4 ball type: Interleaved Type



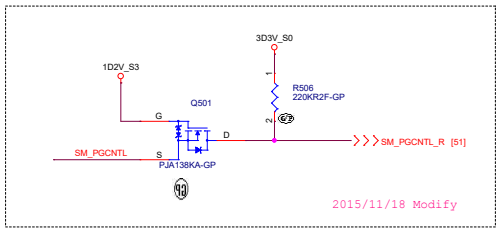


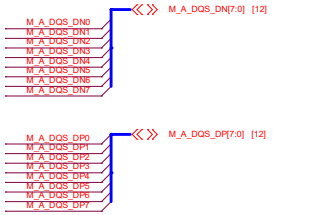


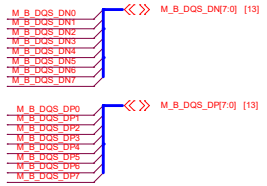
Layout Note:

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.







PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT . Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3)
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z)
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(DDR)

Size	Document Number	Rev
A2	Starlord KBL-R	A00

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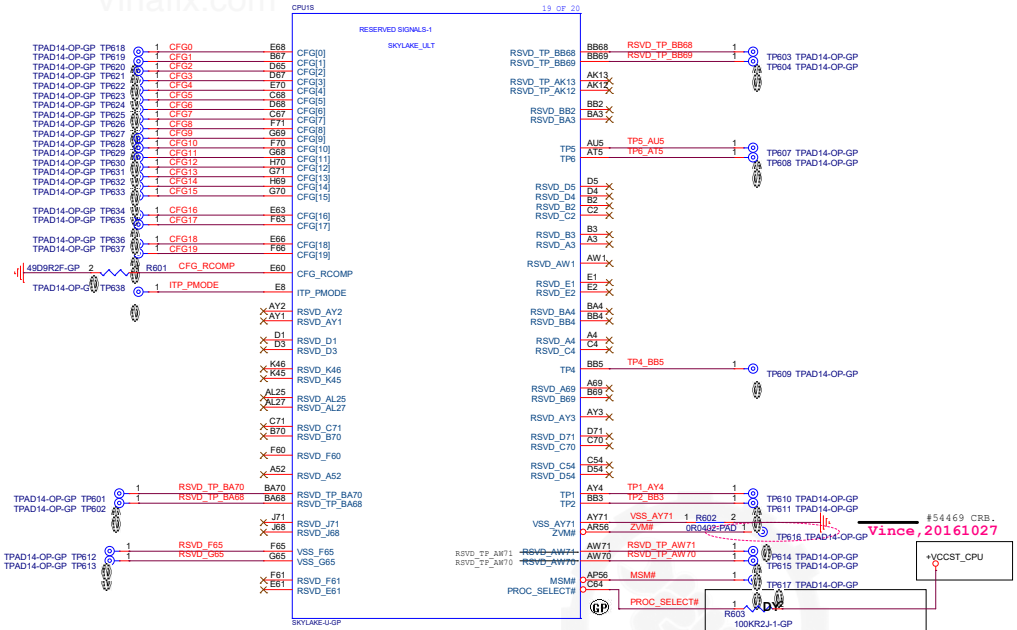
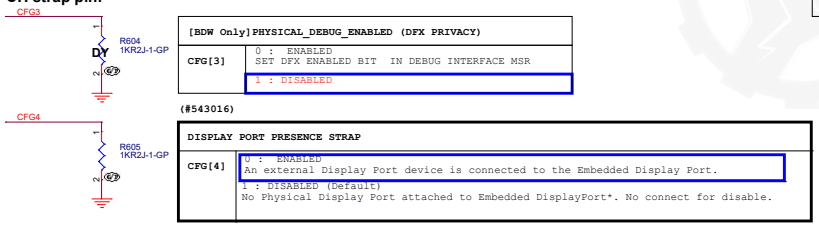
Main Func = CPU

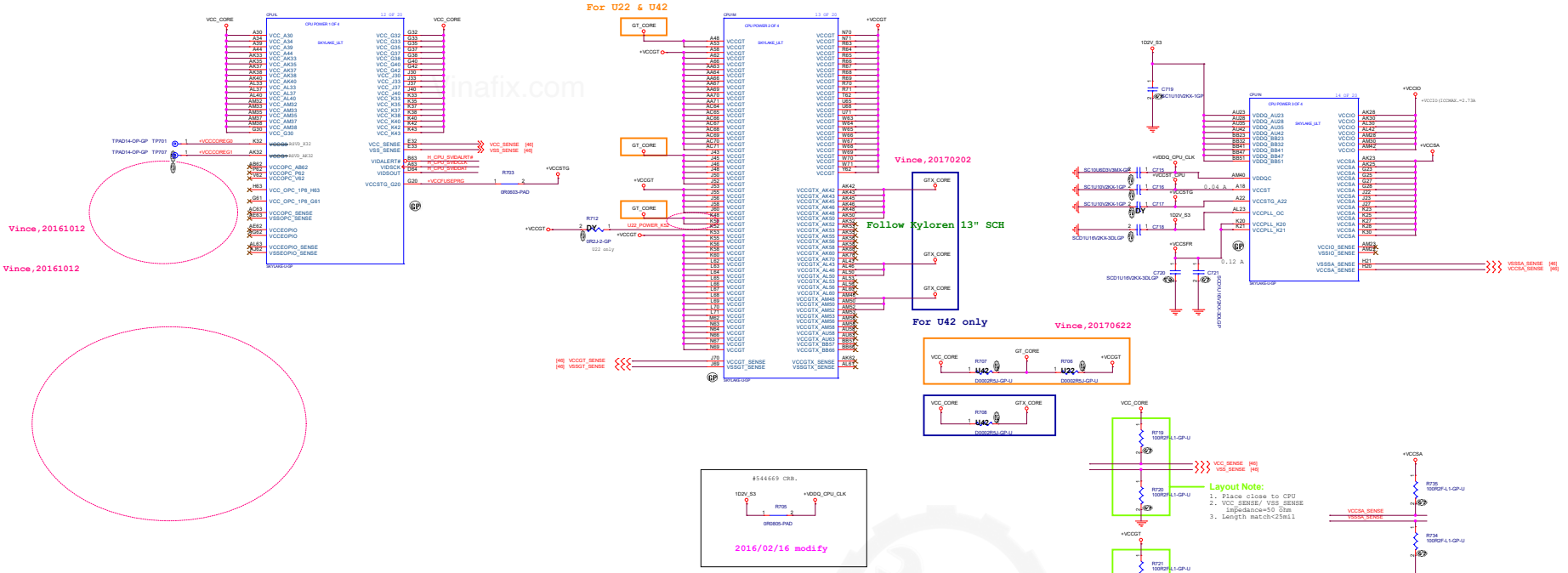


PCH strap pin:



SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

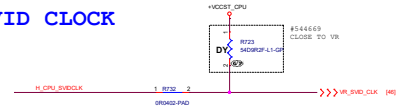
SSID = CPU

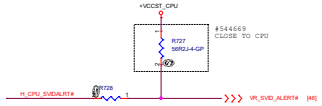


SVID DATA

Layout Note:
The total length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID CLOCK





SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

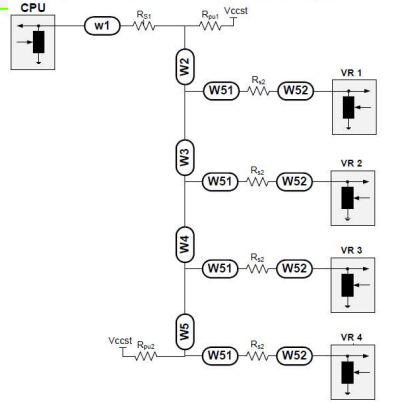


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	WS1 [inches]	WS2 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{S1} [Ω]	R_{S2} [Ω]	V_{CCST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(VCC_CORE)

Size: M | Document Number: Starlord KBL-R | Rev: A00

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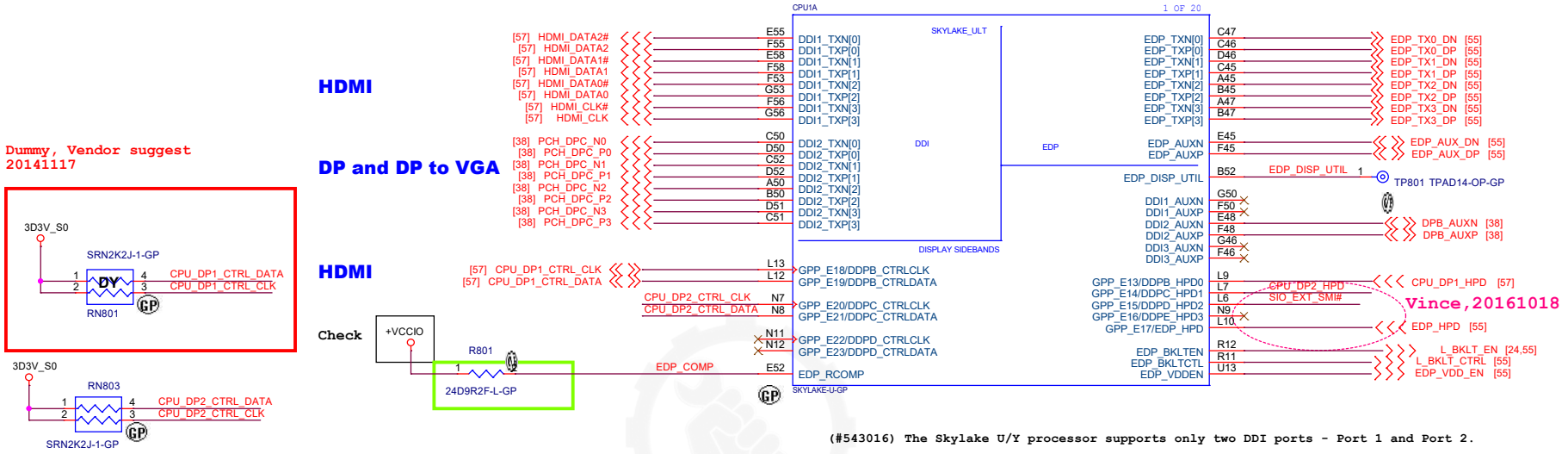
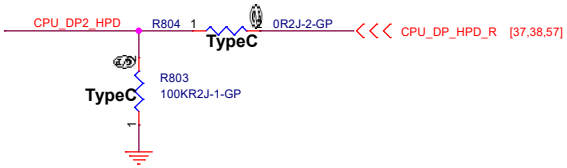
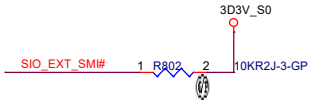
SSID = CPU



(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.





(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.

<Core Design>

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Title: CPU_(DISPLAY)

Size: A3 | Document Number: Starlord KBL-R | Rev: A00

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Main Func = CPU

(Blanking)

<Core Design>

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Title: *(Reserved)*

Size: A3 | Document Number: *Starlord KBL-R* | Rev: *A00*

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SSID = CPU

(#543016 PDG)

20140814 DAVID

CORE

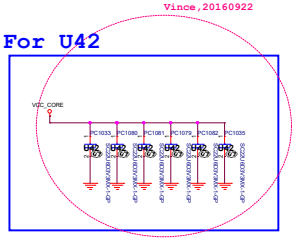
U-line 23e 28W
IccMax current-10ms max = 34 A

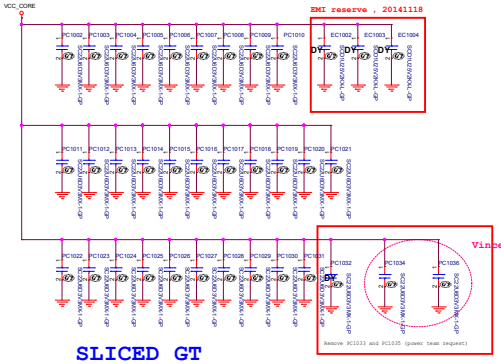
22U 0603 x 35(5 DY)

EMI reserve , 20141118

Vince,20160922

For U42



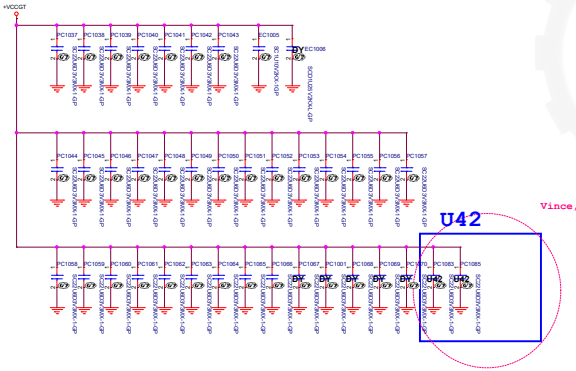


SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

22U 0603 x35 (5 DY)

Vince,20160922



VCCSA

22U 0603 x13 (5 DY)

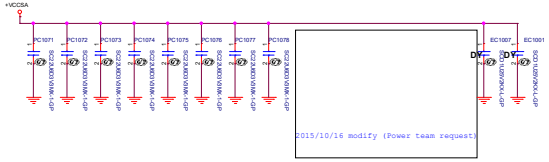


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Additional components needed when supporting 23e
VCCGTx Power Plane at VR output	1x 220uF (@4.5mO ESR)	Placed at primary side near to VR output Only needed when supporting 23e
VCCIO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

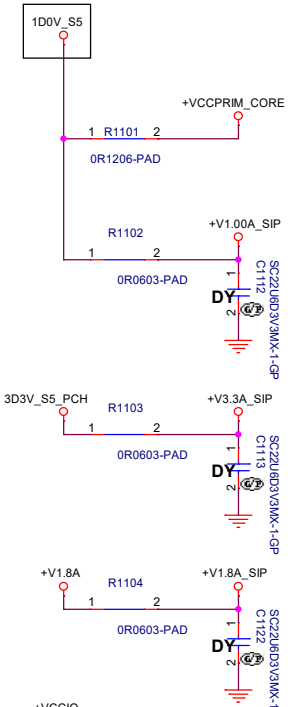
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603		Place on secondary side, underneath the package
	7x 10uF 0402		
	15x 1uF 0201		
		8x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
	12x 1uF 0201		
		3x 47uF 0805 (6.3V)[1]	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible Additional components needed when supporting 23e
		5x 22uF 0603	
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
	7x 1uF 0201		
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402		Place on secondary side, underneath the package
	4x 1uF 0201		
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL		1x 1uF 0402	Place as close to the package as possible
VCCST		1x 1uF 0402	Place as close to the package as possible

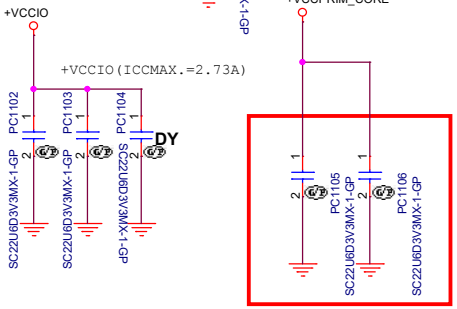
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCEOPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0201		

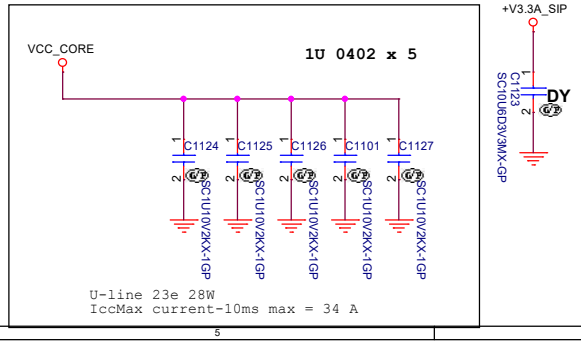
Main Func = CPU

PCH DERIVED RAILS

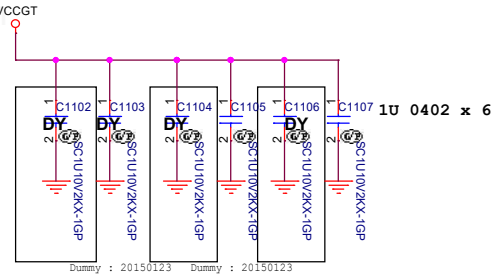




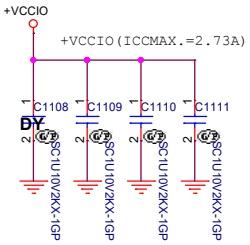
Size:0805 change to 0603
20141117

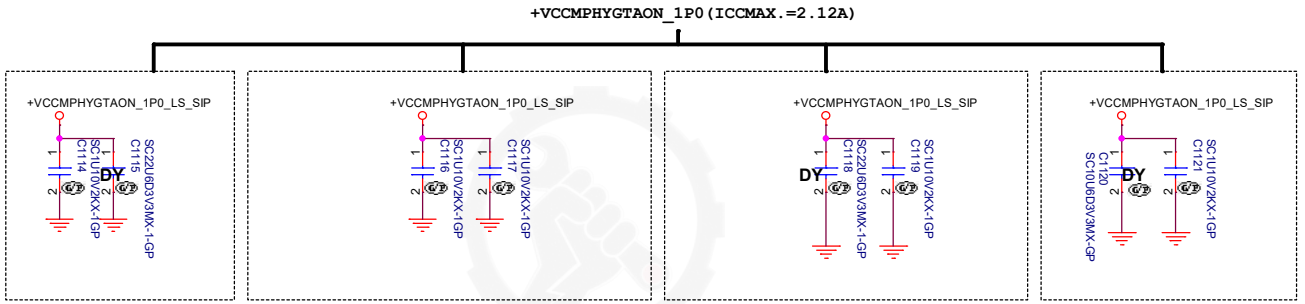


UNSLICED GT



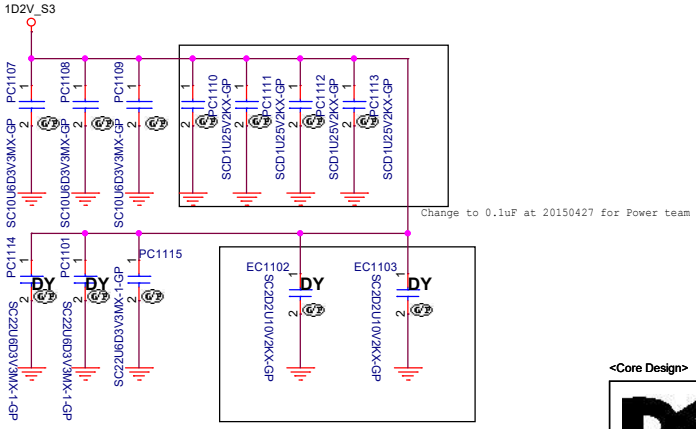
VCCIO





Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

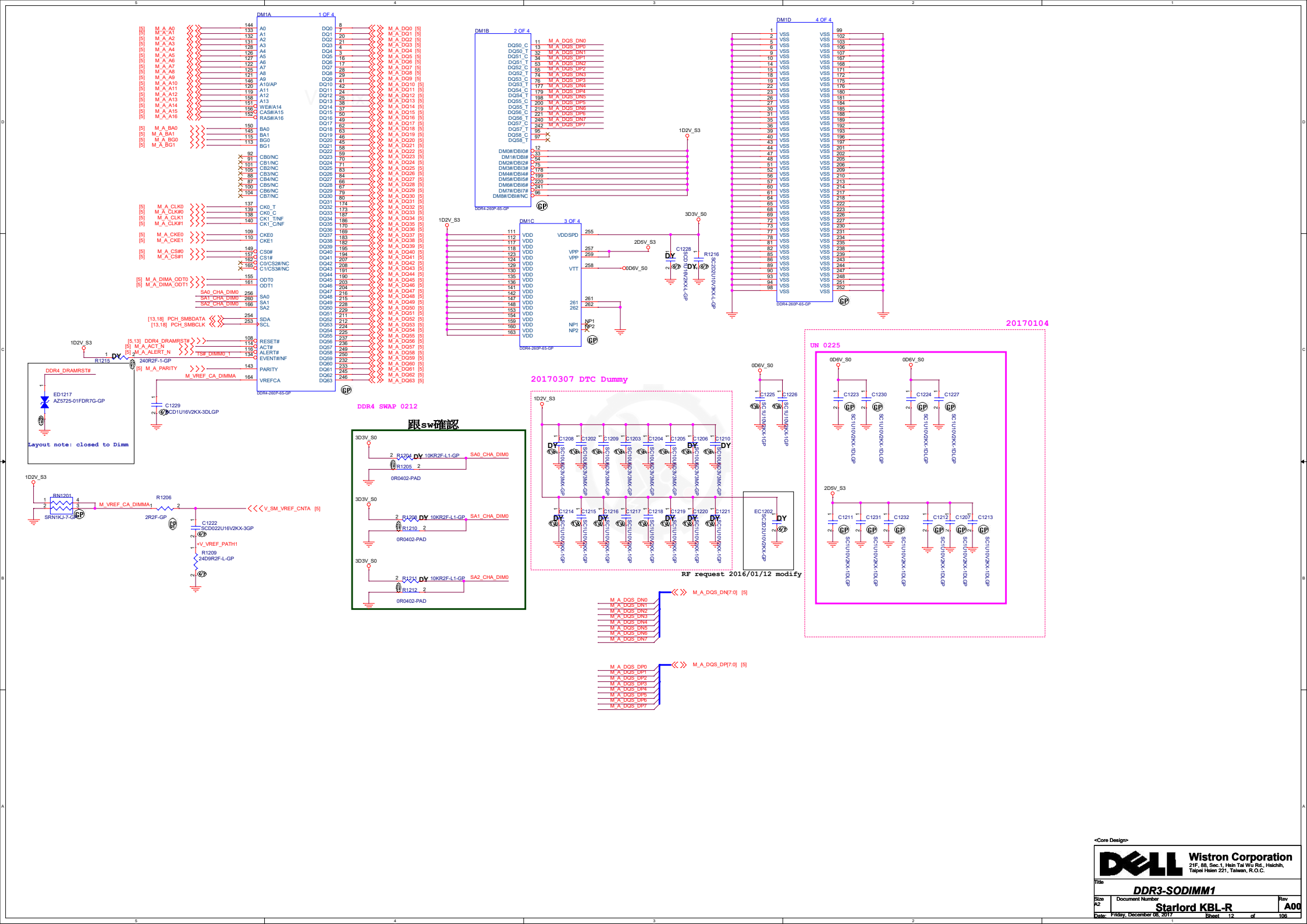


RF request 2016/01/12 modify

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(Power CAP2)	
Size: A3	Document Number: Starlord KBL-R	Rev: A00
Date: Friday, December 08, 2017	Sheet 11 of 106	


DM1A
1 OF 4
DM1B
2 OF 4
DM1C
3 OF 4
DM1D
4 OF 4
DDR4-260P-65-GP
DDR4 SWAP 0212
跟sw確認
20170307 DTC Dummy
RF request 2016/01/12 modify
20170104
UN 0225
Layout note: closed to Dimm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DDR3-SODIMM1
Starlord KBL-R
A00
Friday, December 08, 2017
12
106

By layou modify 20150916

By layou modify 20150916

DDR4 SWAP 0212

跟sw確認

20170307 DTC Dummy

UN 0225

20170104

RF request 2016/01/12 modify

RF request 2016/01/12 modify

Layout note: closed to Dimm

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size: A2 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 13 of 106

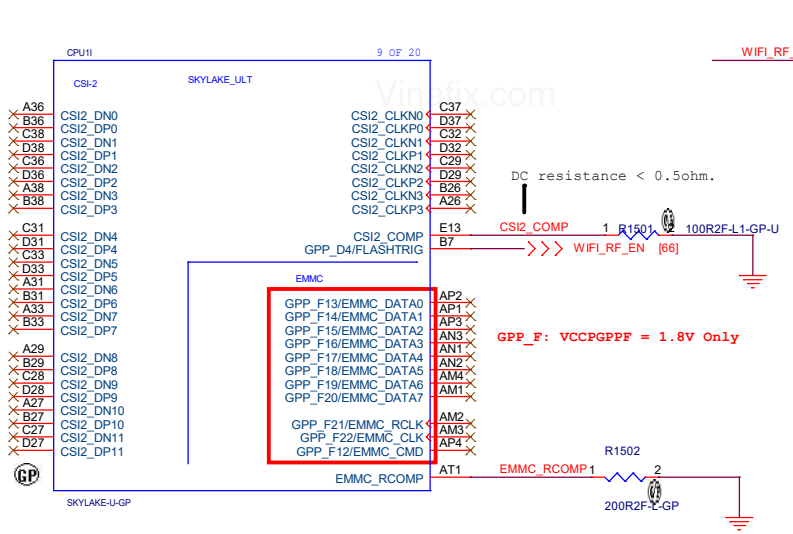
(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)_SODIMM _SODIMM4*		
Size: A4	Document Number: *Starlord KBL-R*	Rev: *A00*
Date: Monday, August 28, 2017	Sheet 14 of 106	

Main Func = PCH



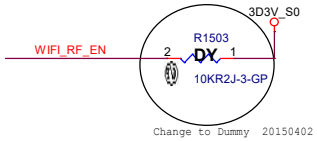


Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

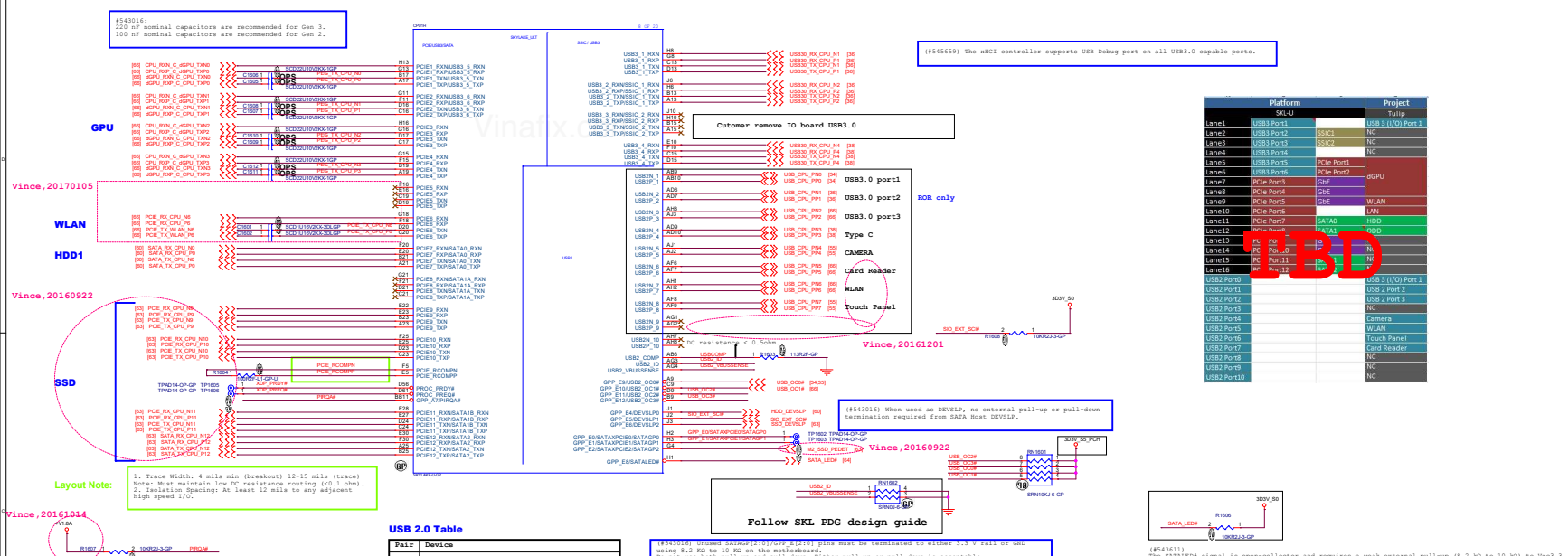
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CS-2/EMMC)

Size: A3 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 15 of 106

SSID = PCH



(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

(#543016) When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

(#543611)
The SATALED# signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc3_3.

1. Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2 (Debug Port/IOBD)
2	USB3.0 Port3 (IOBD)
3	Sensor HUB
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader

Table 12-7. PCIe* Configuration Lane Reversal Mapping

PCIe* Configuration	PCI Express* Lanes			
	PCIe* Controller #1	PCIe* Controller #3	PCIe* Controller #3 (KBL-U PCH-LP Only)	PCI Express* Down Device or Connector Lanes
1x4	1	5	9	3
	2	6	10	2
	3	7	11	1
	4	8	12	0
2x1+1x2	1	5	9	0
	2	6	10	0
	3	7	11	1
	4	8	12	0

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

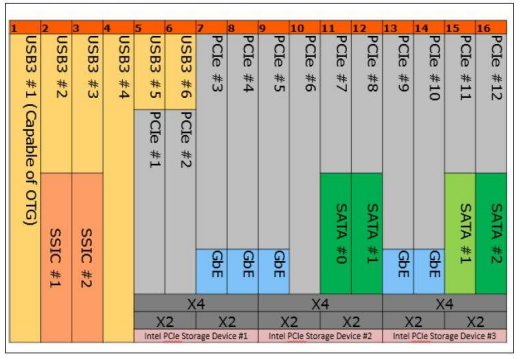


Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Dell_CY17_CSB_HSIO_Port_Assignment_Rev0.7_2016-10-18_Release (Wistron)_DELL

	PCH-U HSIO Ports															
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	USB3 #1 (capable of OTG)	USB3 #2	USB3 #3	USB3 #4	USB3 #5 (Premium-U only)	USB3 #6 (Premium-U only)	PCIe #3	PCIe #4	PCIe #5	PCIe #6	PCIe #7 (Premium-U only)	PCIe #8 (Premium-U only)	PCIe #9	PCIe #10	PCIe #11	PCIe #12
		SSIC			PCIe #1	PCIe #2	GbE	GbE	GbE		SATA #0	SATA #1A	GbE	GbE	SATA #1B (Premium-U only)	SATA #2 (Premium-U only)
					X4				X4 (Intel RST for PCIe storage device #1)				X4 (Intel RST for PCIe storage device #2)			
					X2		X2		X2		X2		X2		X2	
CY17 Port Mapping	External Port /Type-C #1	External Port /Type-C #2 or WWAN SSIC	External Port /Type-C #3	External Port /Type-C #4 3D CAM	dGPU (x4)				LOM	WLAN	HDD (2.5")	ODD (2SP) SSD (1SP)	Thunderbolt Gen3x2 (Alpine Ridge SP/LP)		Optane SSD/NVMe PCIe Gen3x2	
Starlord KBL_Refresh	USB3.0 #1 (USB2)	USB3.0 #2_ROR (USB3)	N/A	Type-C #1 (USB1)	dGPU (x4)				WLAN	N/A	HDD1 (2.5")	N/A	Optane SSD/NVMe PCIe Gen3x4			
													M.2 SSD PCIe x4			

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/SATA/USB)

Size: A1 | Document Number | Rev: A00

Starlord KBL-R

Date: Friday, December 08, 2017 | Sheet 18 of 106

Main Func = PCH

Remove Power rail +V3.3A_SIP and R1712(DY), 20141118

R1709,R1723,R1703,R1724 merge to RN1704

RN1704 SRN10KJ-6-GP

AC_PRESENT
PCH_WAKE#
PCH_BATLOW#
GPD11/LANPHYPC

2PD11 pull high by Intel PDG1.3 request

3D3V_S5 R1711 0R0603-PAD +VCCPDSW_3P3

Layout note: 3 PAD SHARING

RTC_AUX_S5 R1730 330KR2J-L1-GP SM_INTRUDER#

#544669 (CRB): 330k.

+V3.3A_SIP R1731 20KR2J-L2-GP EXT_PWR_GATE#

[#543016 Rev0.7]
EXT_PWR_GATE#: Due to a bug on A0, a temporary pull-up resistor will be required to overcome the internal 20k pull-down that is active during the early portion of the power up sequence

#544669 Rev0.52 CRB:
No PL resistor on THERMTRIP#.

H_CPUPWRGD R1714 10KR2J-3-GP DY ED1701 AZ5725-01FDRTG-GP DY

EMI DVT1 0210

RN1703 SRN10KJ-GP
PM_RSMRST#
PM_PCH_PWROK
R1717 100KR2J-1-GP DY SYS_PWROK

[24] LANWAKE# R1732 0R2J-2-GP DY GPD2/LAN_WAKE#

Vince,20161107

+V1.8A R1739 10KR2J-3-GP DY ME_SUS_PWR_ACK_R

AOZ Power switch, P/N: 074.01334.0093
Low Rds(on)= 5m Ohm
Turn on rise time = 10us

+V3.3A_SIP R1701 10KR2J-3-GP

TP1709 TPAD14-OP-GP PCH_PLTRST#
TP1705 TPAD14-OP-GP H_CPUPWRGD
H_VCCST_PWRGD

[24] SYS_PWROK
[24,26] RESET_OUT#
PM_RSMRST# R1706 2 0R0402-PAD R1704 2 0R0402-PAD
SYS_PWROK
PCH_PWROK
DSW_PWROK
ME_SUS_PWR_ACK_R
SUSACK#_R
PCH_WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC

+VCCPDSW_3P3 R1707 10KR2J-3-GP

(PDG#543016)
WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

CPU1K 11 OF 20
SYSTEM POWER MANAGEMENT
SKYLAKE_ULT
SKYLAKE-U-GP

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/ISS2_WAKEOUT#

GPP_B12/SLP_S0#
GPD4/SLP_S3#
GPD5/SLP_S4#
GPD10/SLP_S5#
SLP_SUS#
SLP_LAN#
GPD9/SLP_WLAN#
GPD6/SLP_A#
GPD3/PWRBTN#
GPD1/ACPRESENT
GPD0/BATLOW#
GPP_A11/PME#
INTRUDER#
GPP_B11/EXT_PWR_GATE#
GPP_B2/VRALERT#

SIO_SLP_S0# [24,40,60,91]
SIO_SLP_S3# [27,40,51,54]
SIO_SLP_S4# [40,54]
SIO_SLP_S5#
TP1703 TPAD14-OP-GP

Vince,20161031
SLP_SUS#
SLP_LAN#
AUX_EN_WOWL
SIO_SLP_A#
TP1711 TPAD14-OP-GP
TP1704 TPAD14-OP-GP
TP1710 TPAD14-OP-GP
TP1706 TPAD14-OP-GP

SIO_PWRBTN# [24]
AC_PRESENT
PCH_BATLOW#
PME#
SM_INTRUDER#
TP1707 TPAD14-OP-GP
EXT_PWR_GATE#
VRALERT#
TP1708 TPAD14-OP-GP

BATLOW#:
Pull-up required even if not implemented.

AC_PRESENT EC1707 SCD1U16V2KX-3GP DY

Vince,20161121

[24,40] RUNPWROK R1716 100KR2F-L1-GP DY R1719 47KR2F-GP

H_VCCST_PWRGD SCD01U50V2KX-1GP DY ED1708 AZ5725-01FDRTG-GP DY

EMI DVT1 0210

R1722 & EC1708 modify to 100k and 0.01uF at DVT1

Vince,20161017

[63,66,91] PLT_RST# R1715 100KR2J-1-GP DY DY R1713 2 0R0402-PAD PCH_PLTRST#
C1701 SC220P50V2KX-3GP

3D3V_S5 EC1713 SCD01U10V2KX-GP DY

RF request 2016/01/12 modify

Vince,20161121

+VCCMPHYGTAON_1P0
SKL: 1.0V
+VCCMPHYGTAON_1P0(ICCMAX.=2.12A)

1D0V_S5 EC1710 SCD1U10V2KX-GP DY R1724 0R6J-L-GP +VCCMPHYGTAON_1P0_LS_SIP C1704 SC10U6D3V3MX-GP

RF request 2016/01/12 modify

#543016 Rev0.7
1. VCCST_PWRGD is only 1.0 V tolerant.
2. VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST

XDP_DBRESET#
SYS_PWROK
PLT_RST#
RESET_OUT#
3V_5V_POK

EC1705 SCKP50V2KX-1GP DY
ED1702 ED1703 ED1704 ED1705 AZ5725-01FDRTG-GP DY

EMI DVT1 0210

D1701 RB751V-40H-GP
ACOK_IN_M [43,44]

3D3V_AUX_S5 R1737 100KR2J-1-GP PM_RSMRST#_M
Q1702 2N7002KDW-1-GP
PM_RSMRST#_R 1 R1720 2 0R0402-PAD PM_RSMRST#
AC_PRESENT

Reserve by NON DS3 function 20150413

DS3 BOM Option

Vince,20161017

PCH_DPWROK R1761 DY 0R2J-2-GP 3V_5V_POK [40,45,52,54]

Change dummy property from DS3 to DY

ED1711 AZ5725-01FDRTG-GP

Change location to net PCH_DPWROK

Vince,20170307

ME_SUS_PWR_ACK_R 1 R1708 2 SUSACK#_R 0R0402-PAD

3D3V_AUX_S5 R1727 100KR2J-GP R1726 10KR2J-3-GP

Q1701 PJT138KA-GP

PM_RSMRST# 1 R1702 1KR2J-1-GP PM_RSMRST# [24]
3V_5V_POK# 5
3V_5V_POK_C 1 R1728 2 0R0402-PAD
3V_5V_POK [40,45,52,54]

Vince,20161031

C1710 SCD47U10V2KX-GP DY

Dummy C1710 by it's useless

EC1712 SCD1U16V2KX-3GP DY

EC1711 modify to 100k and 0.01uF at DVT1 20150203

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)
Size: A2 | Document Number: Starlord KBL-R | Rev: A00
Date: Friday, December 08, 2017 | Sheet 17 of 106

SSID = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

R1835 and R1834 merge to RN1802
2015/10/06 modify

R1806,R1807,R1808,R1809 merge to RN1803
2015/10/06 modify

SERIRQ PH:
PDG: 8.2k
CRB: 10k

RCIN#:
Frequency to Avoid: 33 MHz

Pin	Connection
#1,#3	X'tal
#2,#4	GND

Vinafix.com

Vince,20161013
Vince,20170106
Vince,20161017
Vince DVT2,20170511
Vince,20161027
Vince,20170117
Vince,20170120 common part request
Vince,20170110
Vince,20161026
Vince,20170328
Vince,20161223
Vince,20170203
Vince,20161027

WLAN
SSD

Layout: Place at the open door area.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(LPC/SPI/SMBUS/CL/CLK)
Size: A2 | Document Number: Starlord KBL-R | Rev: A00
Date: Friday, December 08, 2017 | Sheet 18 of 106

SSID = PCH

Strap pin:

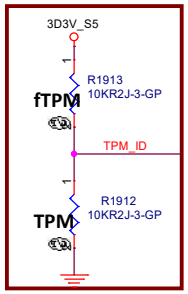
Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

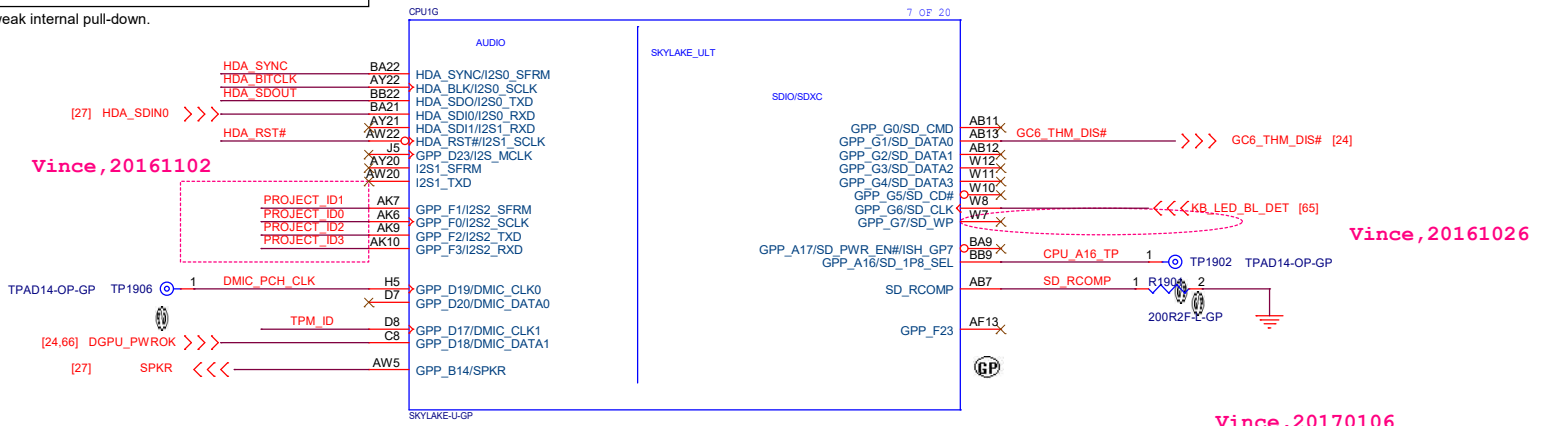
These two signals have weak internal pull-down.

Vince,20161107

fTPM: SW TPM

TPM:HW TPM





PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default High = Enable *

The internal pull-down is disabled after PLTRST# deasserts

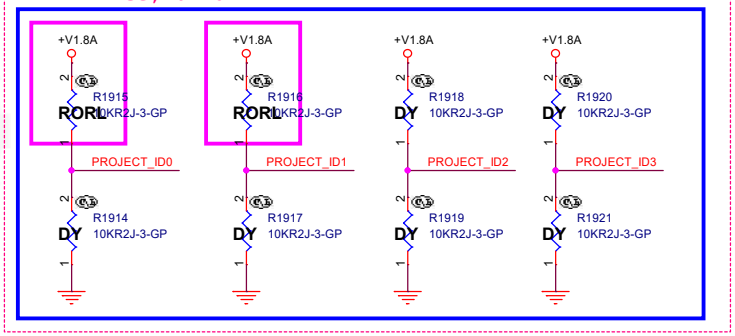
PCH strap pin:

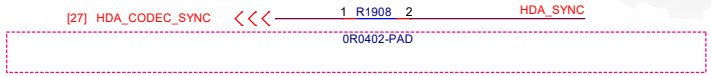
NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts

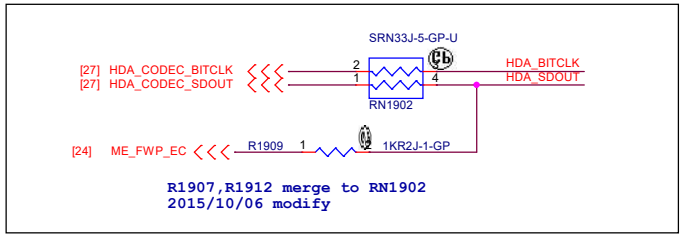
Vince,20170721

Vince,20170106





Vince,20170106



<Core Design>

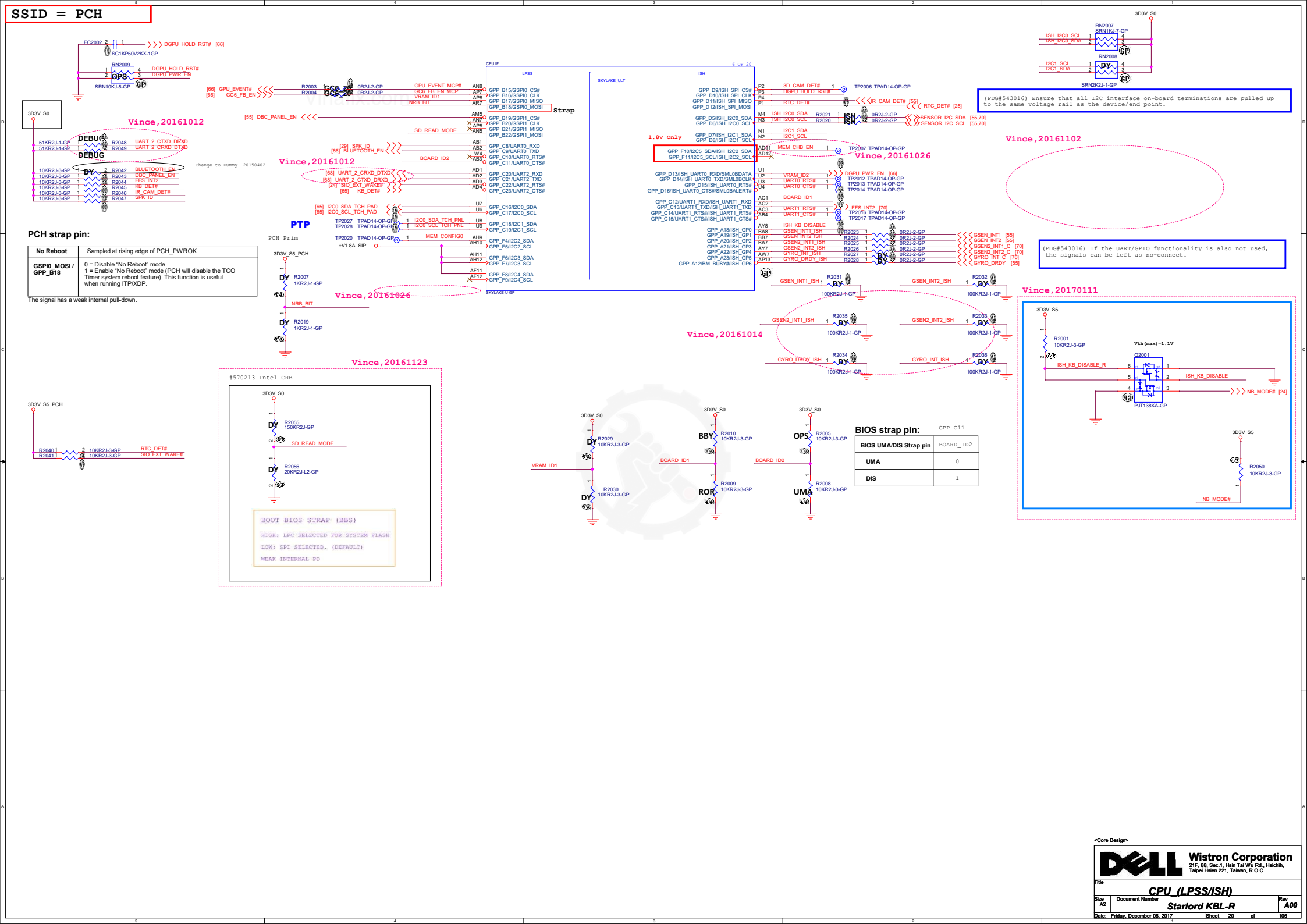
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(AUDIO/SDIO/SDXC)

Size	Document Number	Rev
A3	Starlord KBL-R	A00

Date: Friday, December 08, 2017 Sheet 19 of 106

SSID = PCH



PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

BIOS strap pin: GPP_C11

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

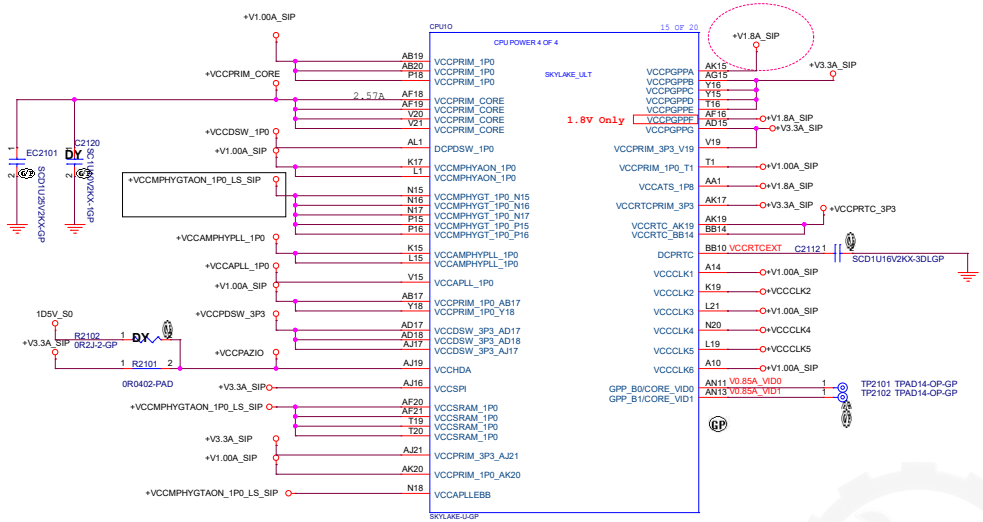
Title: CPU_(LPSS/ISH)

Size	Document Number	Rev
A2	Starlord KBL-R	A00

Date: Friday, December 08, 2017 Sheet 20 of 106

Main Func = PCH

Vince,20161013



+VCCPRTC_3P3

C2118 SC1U10V2KX-1GP

C2117 SCD1U16V2KX-3DLGP

Layout Note:

0.1uF:
C2118 near AK19
1uF:
C2117 near Ak19

RTC_AUX_S5 — R2106 — +VCCPRTC_3P3 — 0R0603-PAD

+VCCMPHYGTAON_1P0_LS_SIP — R2107 — +VCCAMPHYPLL_1P0 — 0R0603-PAD

+V1.00A_SIP — R2108 — +VCCAPLL_1P0 — 0R0603-PAD

+V1.00A_SIP — R2109 — +VCCCLK2 — 0R0603-PAD

+V1.00A_SIP — R2110 — +VCCCLK4 — 0R0603-PAD

+V1.00A_SIP — R2111 — +VCCCLK5 — 0R0603-PAD

+V3.3A_SIP

C2105 SC1U10V2KX-1GP
C2106 SC1U10V2KX-1GP
C2107 SC1U10V2KX-1GP
C2109 SC1U10V2KX-1GP
C2110 SC1U10V2KX-1GP
C2111 SCD1U16V2KX-3DLGP

Layout Note:

1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
C2110 near T16
C2111 near AJ19

+V1.8A_SIP +VCCPRIM_CORE +VCCDSW_1P0

C2108 SC1U10V2KX-1GP
C2102 SC1U10V2KX-1GP
C2103 SC1U10V2KX-1GP

+V1.00A_SIP

C2101 SC1U10V2KX-1GP
C2104 SC1U10V2KX-1GP
C2116 SC1U10V2KX-1GP
C2121 SC1U10V2KX-1GP

Layout Note:

1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1

+VCCAMPHYPLL_1P0

C2113 SC22UF6D3V3MX-1GP

Layout Note:

22uF:
C2113 near K15

+VCCAPLL_1P0

C2114 SC22UF6D3V3MX-1GP

Layout Note:

22uF:
C2113 near K15

+V1.00A_SIP +VCCCLK2 +VCCCLK4 +VCCCLK5

C2116 SC1U10V2KX-1GP
C2115 SC22UF6D3V3MX-1GP
C2119 SC22UF6D3V3MX-1GP
C2122 SC22UF6D3V3MX-1GP

Layout Note:

1uF:
C2116 near A10
22uF:
C2115 near K19
C2119 near N20
C2122 near L19

<Core Design>

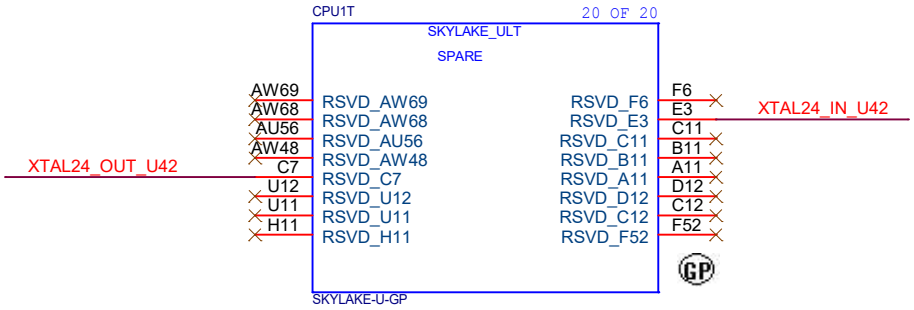
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER1)

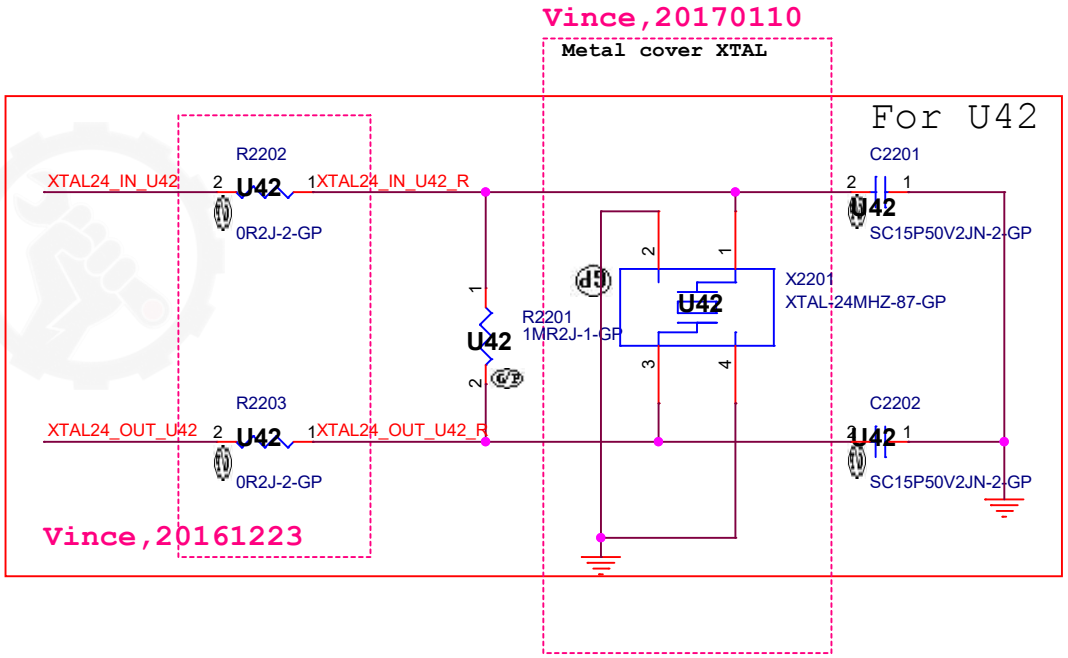
Size: A2 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 21 of 106

Main Func = PCH



Pin	Connection
#1,#3	X'tal
#2,#4	GND



<Core Design>

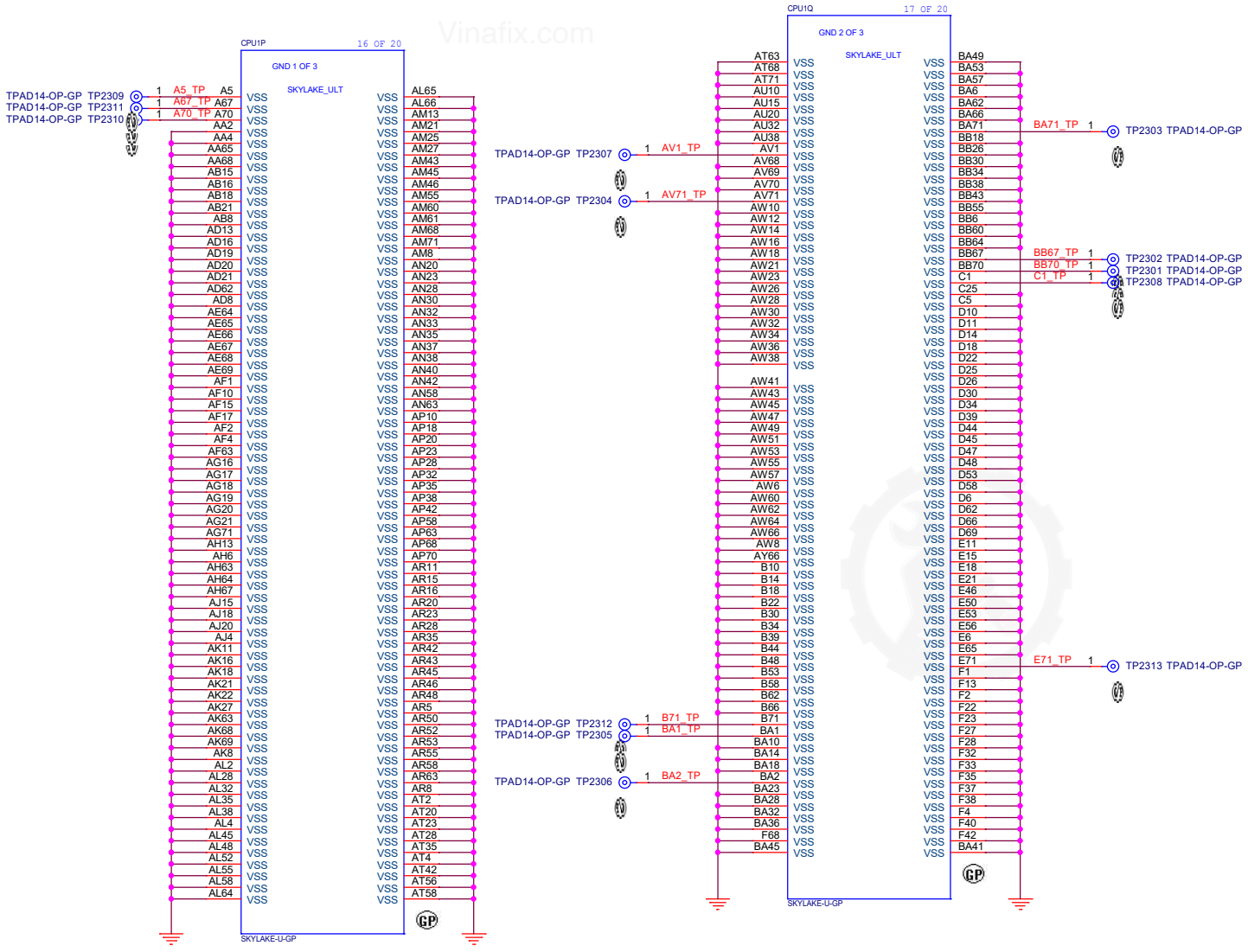
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU_(RSVD)**

Size	Document Number	Rev
A4	Starlord KBL-R	A00

Date: Friday, December 08, 2017 Sheet 22 of 106

Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size: A3 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 23 of 106

Main Func = KBC

Vince,20161013

Vince,20170525

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

Vince,20170721

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1		100.0K	10.0K	3
2	Starlord_13/15"_ROB_UMA	100.0K	17.8K(64.17825.6DL)	2.801
3	StarlordR-L[KBL-U]	100.0K	27.0K	2.598
4	Starlord_17"_BBY_UMA	100.0K	37.4K(064.37425.06DS)	2.402
5		100.0K	49.9K	2.201
6	Starlord_17"_BBY_DIS	100.0K	64.9K(64.64925.6DL)	2.001
7		100.0K	82.5K	1.808
8	StarlordR-L[KBL-R]	100.0K	107K	1.594
9		100.0K	154K	1.299
10	StarlordR-L[SKL-U]	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

Just for Starload placement 2015/09/23 modify

Layout Note: Need very close to EC

Just for Starload placement 2015/09/23 modify

If don't need RTC alarm wake up, can change to 3V3_AUX_S5

Vince,20161013

Vince,20161018

For Typec SMBUS

Change symbol part number, because origin symbol is DELL OBS part

Vince,20161114

Vince,20161012

Vince,20170206

eDP backlight Control from PCH

Vince,20161018

Q2412 and Q2413 merge 24014/12/23 modify

Vince,20160926

Vince,20161013

Vince,20161018

Need very close to EC, PDG: <0.5 inches.

Vince,20161018

Vince,20160929

Vince,20161018

For Typec charge detect modfy 2016/01/04

ALL_SYS_PWRGD assert, delay 1ms; PCH PWROK assert.

Vince,20161101

Vince,20170203

Vince,20161031

For eSPI

GPIO102 (CR_STRAP) GPIO123 (BSS_STRAP)

Already pull low on CPU side

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
1	1	Use 3.3V Shared SPI

Vince,2017328 common part request

Microchip: Use CL=9p Xtal-Tr=7p

Layout Note: Connect GND and AGND planes via either 0R resistor or connect directly.

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

Vince,20160929

Move schematic, 20141118

Vince,20170105

Layout Note: Need very close to EC

Need very close to EC

Vince,20170203

Reserve by NON DS3 function 20150413

2015/09/22 modify

Vince,20161107

Touch Panel_PN internally.

R2498,R2499 merge to RN2407 2015/10/06 modify

Just for Starload placement 2015/09/23 modify

Change symbol part number, because origin symbol is DELL OBS part 20150116 2040

Vince,20161107

Vince,20161123

Power Switch Logic(PSL)

Vince,20170516

Vince,20161013

Vince,20161031

Vince,20161018

Just for Starload placement 2015/09/23 modify

EC Debug

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

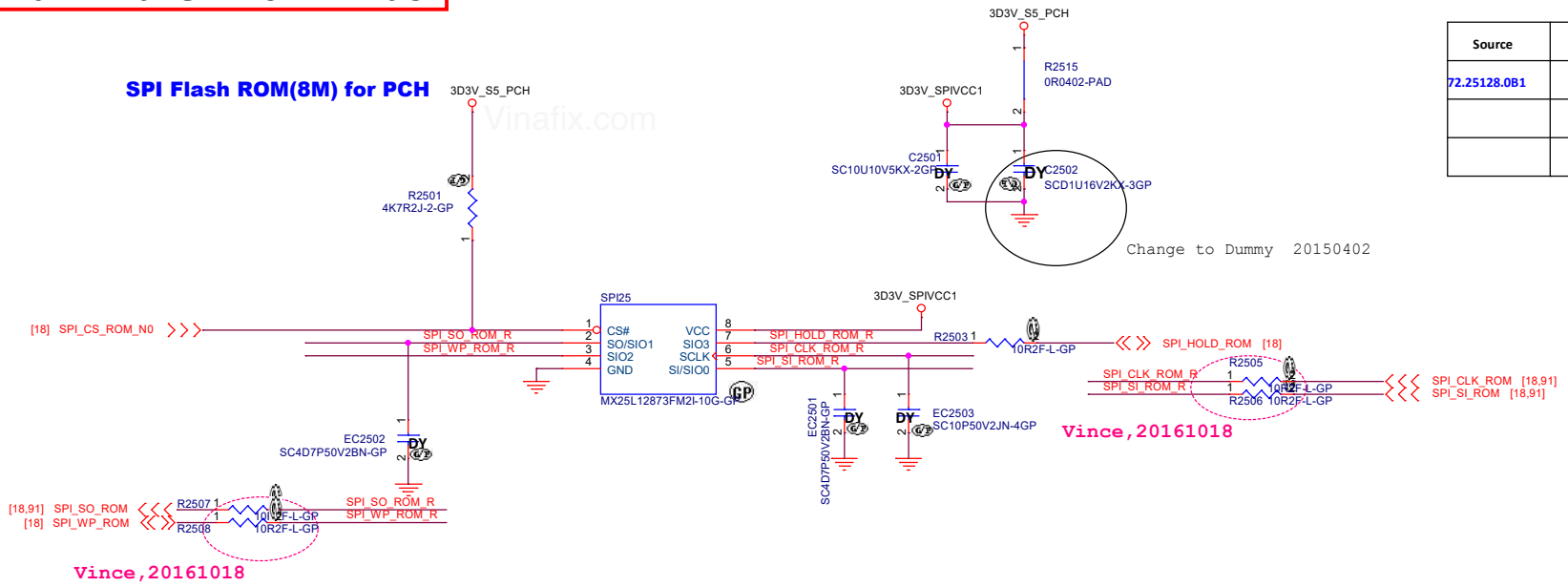
KBC Nuvoton NPCE285PA0DX

Size: A1 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 09, 2016 | Sheet 24 of 55

Main Func = SPI Flash

SPI Flash ROM(8M) for PCH

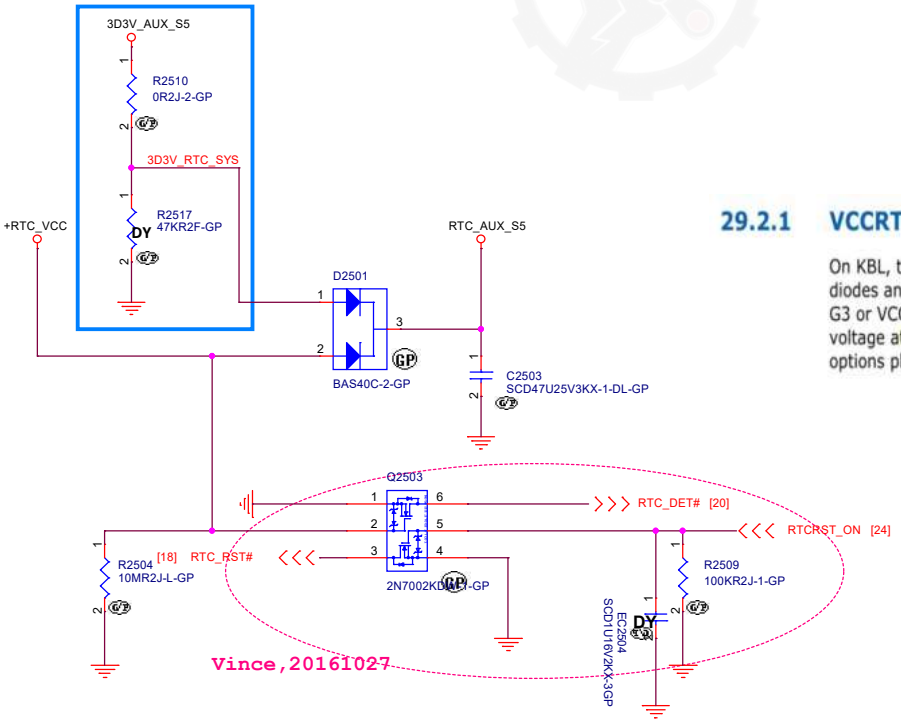


Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25128.0B1	O	O	O
	O	O	O
	O	O	O

Main Func = RTC

Delivery Voltage 3.19V

(when R2510 1K6 ohm)



29.2.1 VCCRTC External Circuit

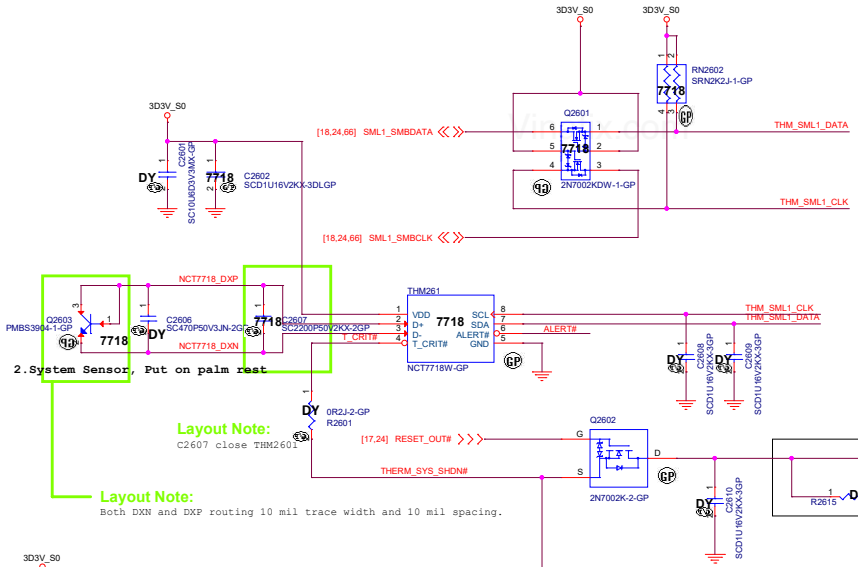
On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

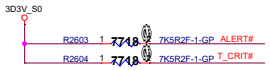
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC		
Size: A3	Document Number: Starlord KBL-R	Rev: A00
Date: Friday, December 08, 2017	Sheet 25 of 106	

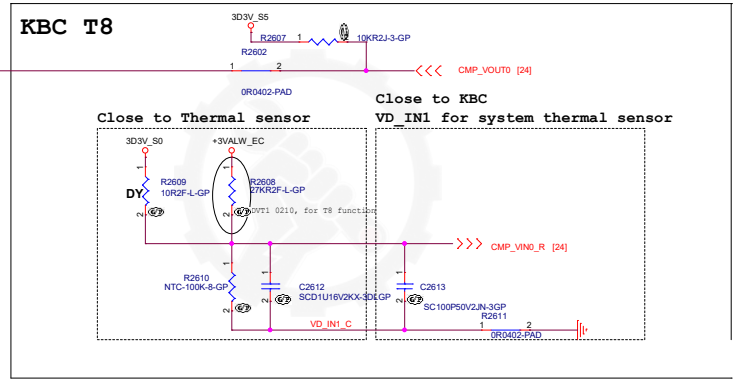
Main Func = Thermal Sensor



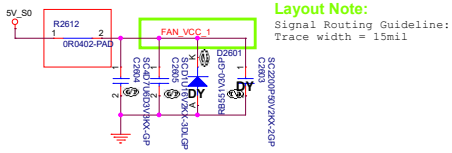


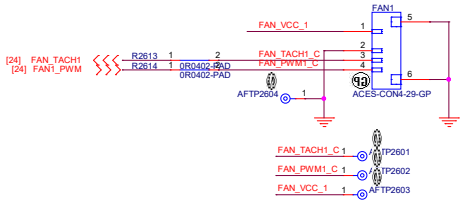
TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

KBC T8



PWM FAN1





<Core Design>
Wistron Corporation
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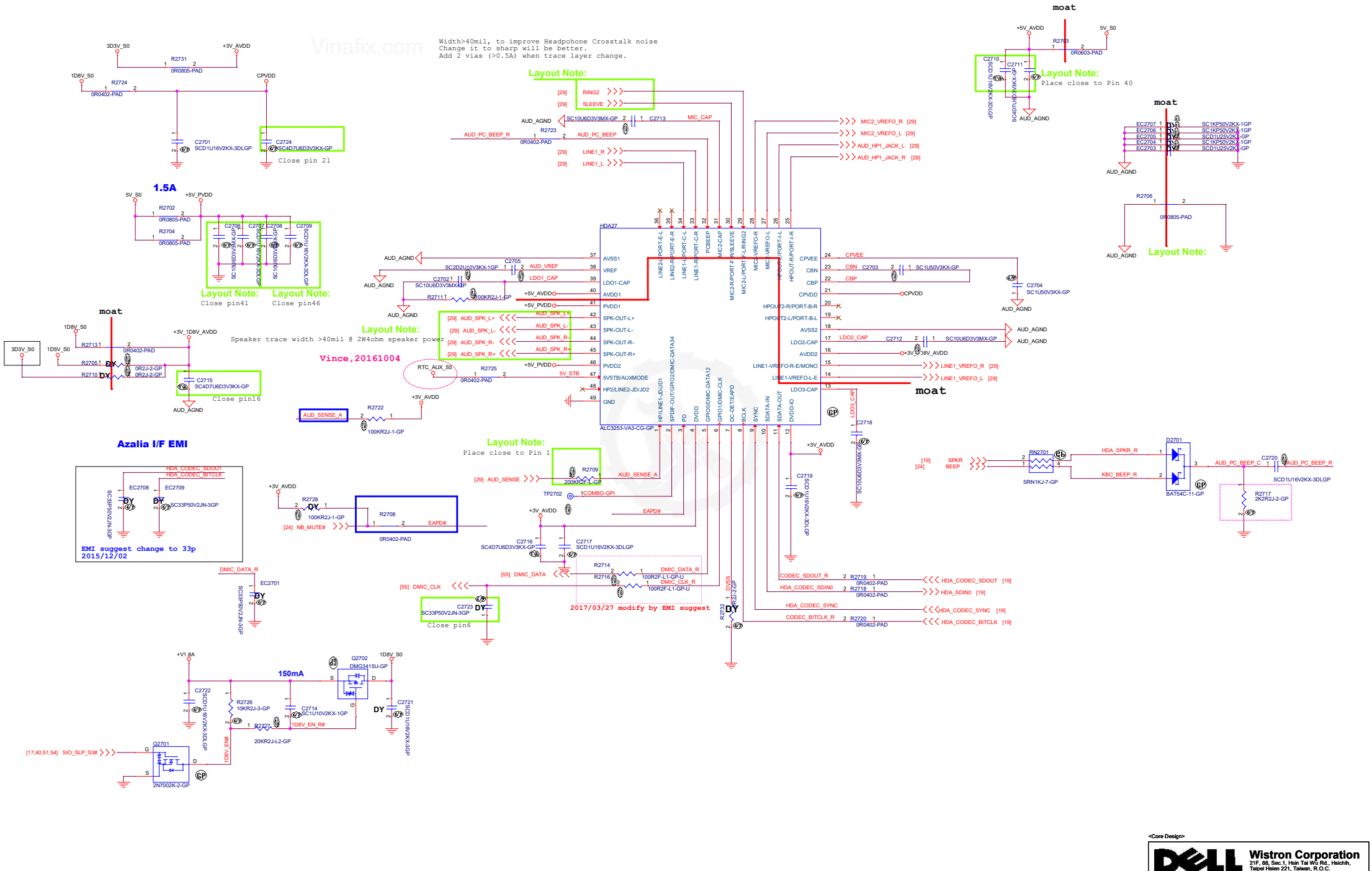
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan
Size: A2
Document Number: Starlord KBL-R
Rev: A00
Date: Friday, December 08, 2017
Sheet 26 of 106

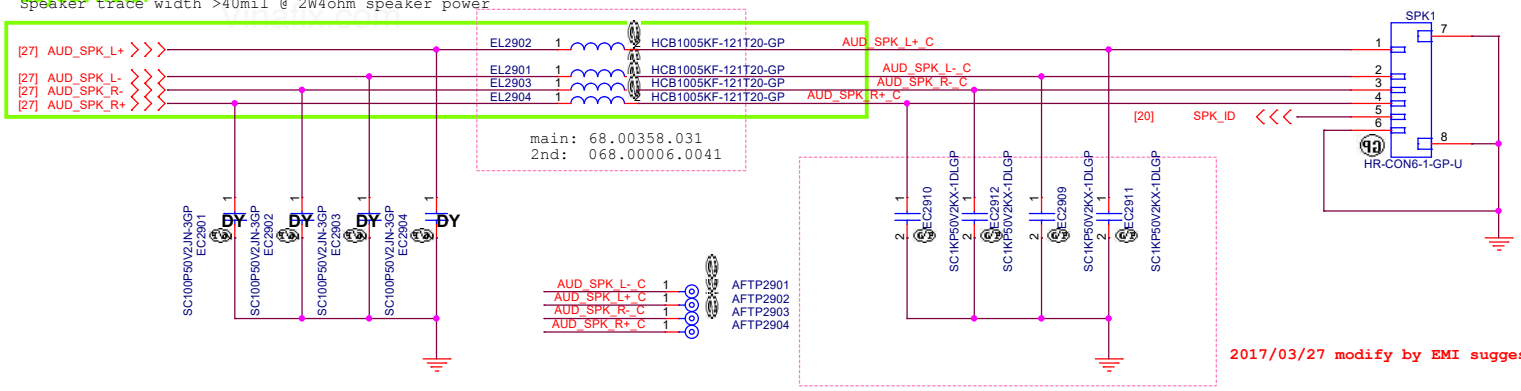
Main Func = Audio



SSID = Audio

Speaker

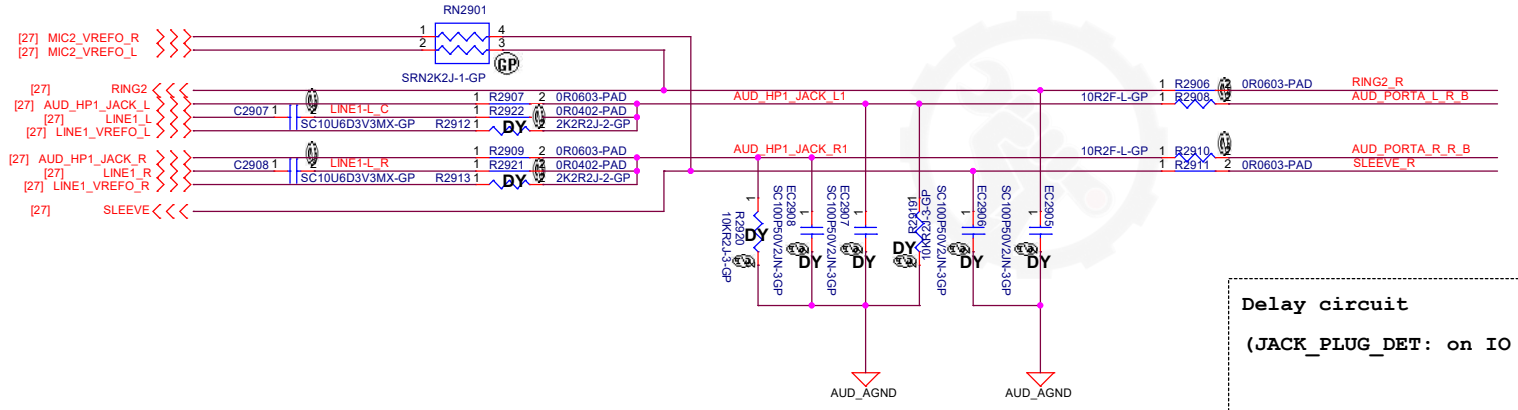
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

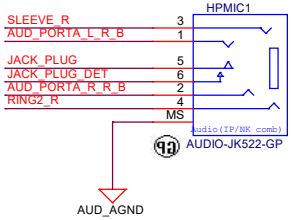


CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

2017/03/27 modify by EMI suggest

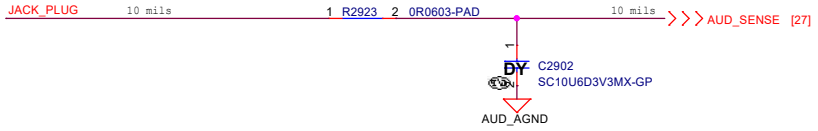
Universal Jack (Moved to I/O Board)

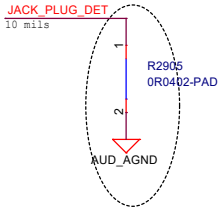




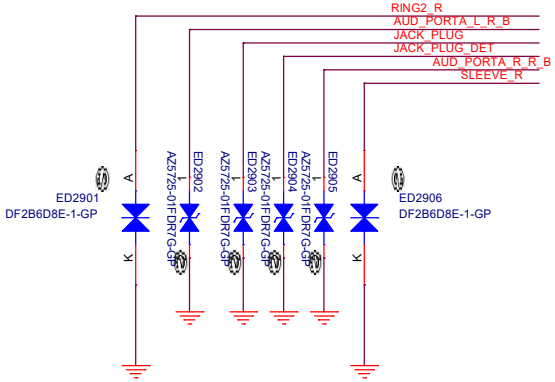
Delay circuit

(JACK_PLUG_DET: on IO Board)





CLOSS TO HPMIC1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio IO
Size: A3
Document Number: Starlord KBL-R
Rev: A00
Date: Friday, December 08, 2017
Sheet 29 of 106

Main Func = Audio

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

(Reserved)

Size	Document Number	Rev
A4	Starlord KBL-R	A00

Date: Monday, August 28, 2017 Sheet 30 of 106

Main Func = LAN

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN RTL8106

Size	Document Number	Rev
A2	Starlord KBL-R	A00

Date: Monday, August 28, 2017 Sheet 31 of 106

SSID = LAN

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XFOM&RJ45

Size: A3 | Document Number: Starlord KBL-R | Rev: A00

Date: Monday, August 28, 2017 | Sheet 32 of 106

Main Func = Card Reader

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

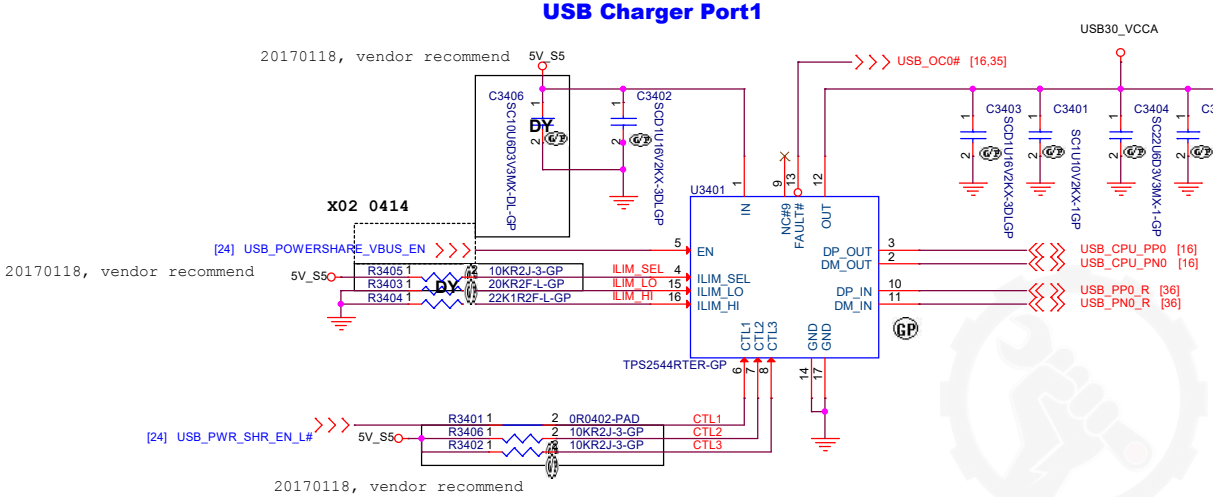
Title: Card Reader-RTS5170

Size	Document Number	Rev
A2	Starlord KBL-R	A00

Date: Monday, August 28, 2017 Sheet 33 of 106

Main Func = USB3.0 Port1

USB Charger Port1



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

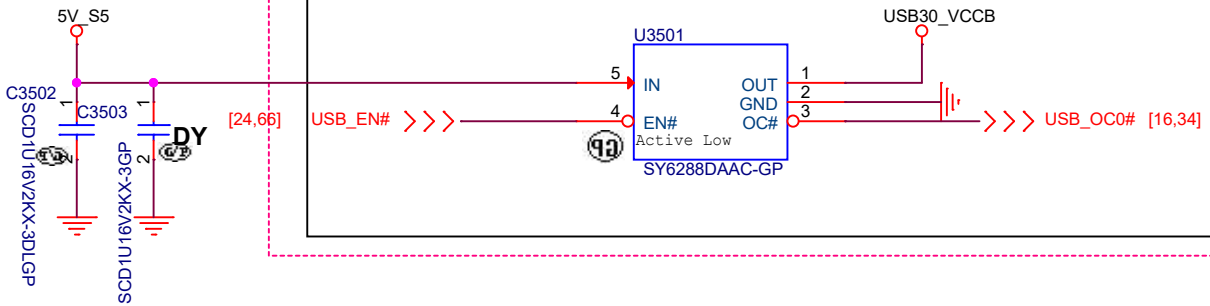
<Core Design>

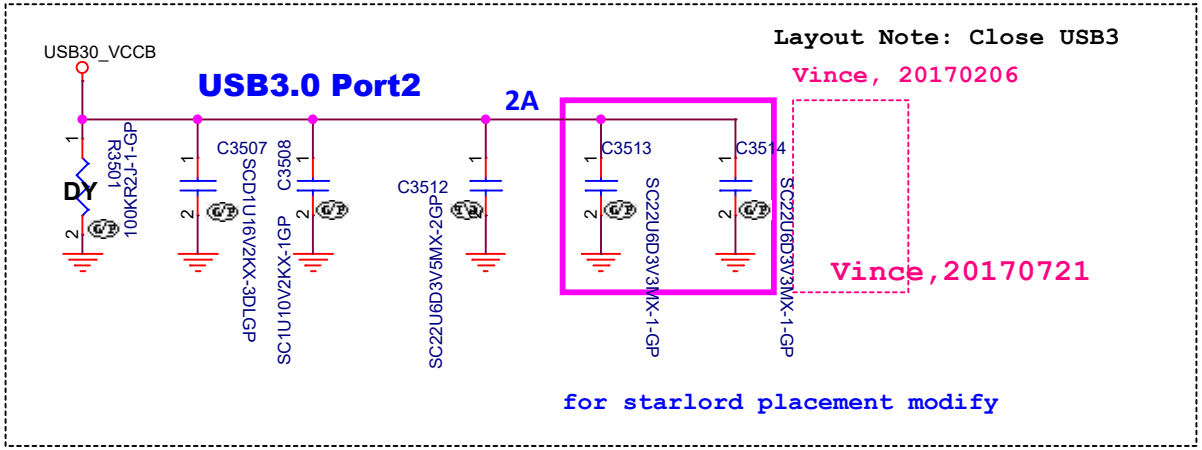
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
(Reserved)		
Size: A3	Document Number: Starlord KBL-R	Rev: A00
Date: Friday, December 08, 2017	Sheet 34 of 106	

Main Func = USB3.0 Port1

Vince, 20170206





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB switch

Size	Document Number	Rev
	Starlord KBL-R	A00

Date: Friday, December 08, 2017 Sheet 35 of 106

SSD = USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1

[16] USB30_TX_CPU_N1 → C3601 SCD1U16V2KX-3DLGP → USB30_TXDN1_R → R3605 0R0402-PAD → USB30_TXDN1_C

[16] USB30_RX_CPU_N1 → R3609 0R0402-PAD → USB30_RXDN1_C

[16] USB30_TX_CPU_P1 → C3602 SCD1U16V2KX-3DLGP → USB30_TXDP1_R → R3606 0R0402-PAD → USB30_TXDP1_C

[16] USB30_RX_CPU_P1 → R3610 0R0402-PAD → USB30_RXDP1_C

ED3601 L05ESDL5V0NA-4-GP

USB30_RXDN1_C 1 → 10 USB30_RXDN1_C
USB30_RXDP1_C 2 → 9 USB30_RXDP1_C
3 → 8
USB30_TXDN1_C 4 → 7 USB30_TXDN1_C
USB30_TXDP1_C 5 → 6 USB30_TXDP1_C

Vince, 20170206

USB30_VCCA

ED3602 AZC099-04S-1-GP

USB20_DN0_C 1 I/O1 I/O4 6 USB20_DP0_C
2 GND VDD 5
USB20_DN1_C 3 I/O2 I/O3 4 USB20_DP1_C

[34] USB_PP0_R → COIL-90OHM-100MHZ-5-GP EL3605 → USB20_DP0_C

[34] USB_PN0_R → USB20_DN0_C

Vince,20161121

BOM change

USB30_VCCA

USB2 SKT-USB13-221-GP

1 VBUS
D- 2 → USB20_DN0_C
D+ 3 → USB20_DP0_C
USB30_RXDN1_C 5 STDA_SSRX-
USB30_RXDP1_C 6 STDA_SSRX+
GND_DRAIN 7
USB30_TXDN1_C 8 STDA_SSTX-
USB30_TXDP1_C 9 STDA_SSTX+
GND 10
GND 11
GND 4
12 CHASSIS#12
13 CHASSIS#13

USB 3.0 Connector Pin definition		
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB3.0 Port2

[16] USB30_TX_CPU_N2 → C3603 SCD1U16V2KX-3DLGP → USB30_TXDN2_R → R3611 0R0402-PAD → USB30_TXDN2_C

[16] USB30_RX_CPU_N2 → R3612 0R0402-PAD → USB30_RXDN2_C

ED3603 L05ESDL5V0NA-4-GP

USB30_RXDN2_C 1 → 10 USB30_RXDN2_C
USB30_RXDP2_C 2 → 9 USB30_RXDP2_C
3 → 8
USB30_TXDN2_C 4 → 7 USB30_TXDN2_C
USB30_TXDP2_C 5 → 6 USB30_TXDP2_C

Vince,20170206

[16] USB30_TX_CPU_P2 → C3604 SCD1U16V2KX-3DLGP → USB30_TXDP2_R → R3614 0R0402-PAD → USB30_TXDP2_C

[16] USB30_RX_CPU_P2 → R3613 0R0402-PAD → USB30_RXDP2_C

[16] USB_CPU_PP1 → COIL-90OHM-100MHZ-5-GP EL3606 → USB20_DP1_C

[16] USB_CPU_PN1 → USB20_DN1_C

BOM change

USB30_VCCB

USB3 SKT-USB13-221-GP

1 VBUS
D- 2 → USB20_DN1_C
D+ 3 → USB20_DP1_C
USB30_RXDN2_C 5 STDA_SSRX-
USB30_RXDP2_C 6 STDA_SSRX+
GND_DRAIN 7
USB30_TXDN2_C 8 STDA_SSTX-
USB30_TXDP2_C 9 STDA_SSTX+
GND 10
GND 11
GND 4
12 CHASSIS#12
13 CHASSIS#13

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB30

Size	Document Number	Rev
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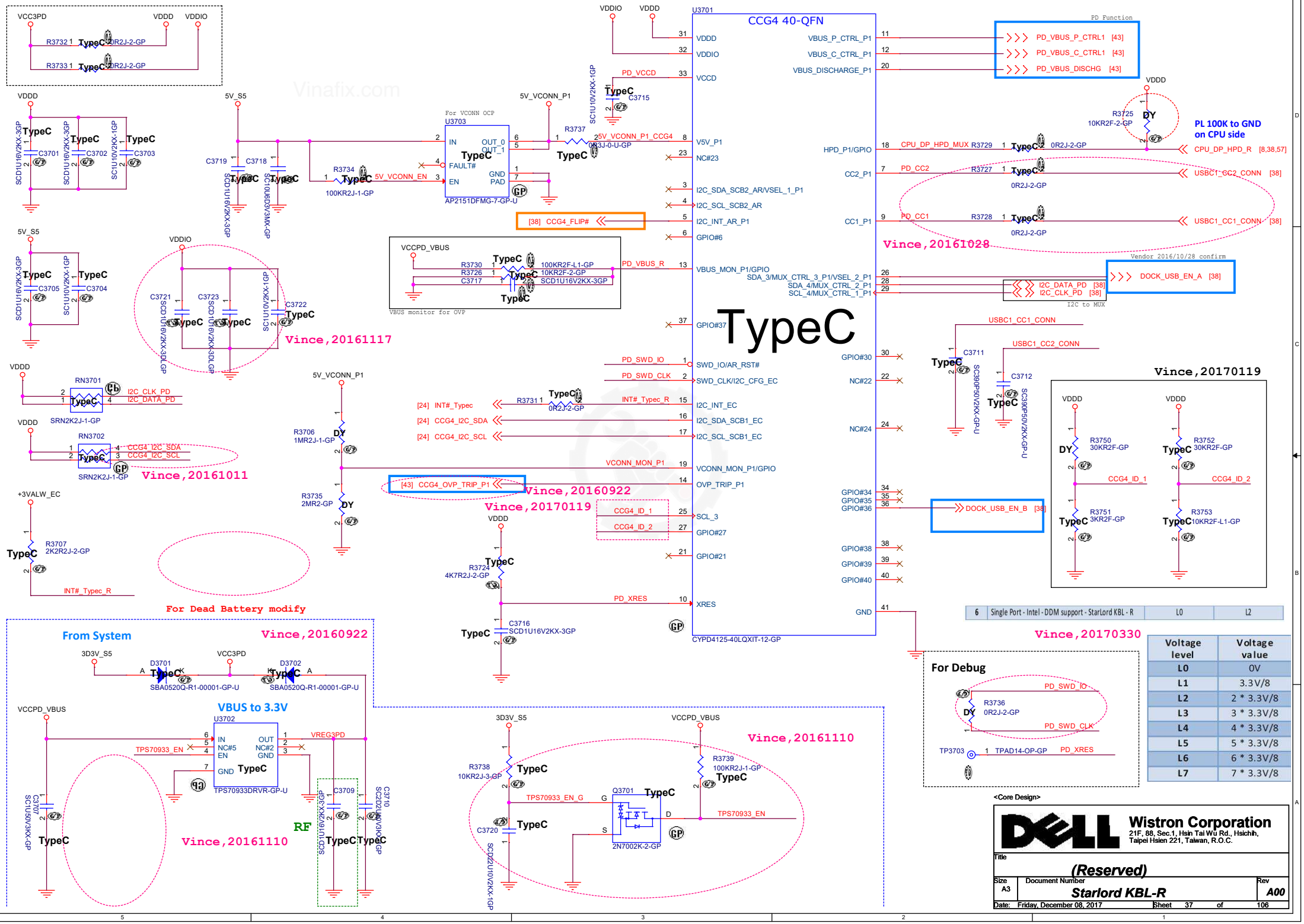
TypeC
CCG4 40-QFN
U3701
CYPD4125-40LQXIT-12-GP
VCC3PD
VDDD
VDDIO
R3732 0R2J-2-GP
R3733 0R2J-2-GP
5V_S5
U3703
AP2151DFMG-7-GP-U
5V_VCONN_P1
5V_VCONN_EN
5V_VCONN_P1_CCG4
R3737 0R3J-0-U-GP
R3734 100KR2J-1-GP
VCCPD_VBUS
VBUS monitor for OVP
R3730 100KR2F-L1-GP
R3726 10KR2F-2-GP
C3717 SCD1U16V2KX-3GP
PD_VBUS_R
[38] CCG4_FLIP#
I2C_SDA_SCB2_AR/VSEL_1_P1
I2C_SCL_SCB2_AR
I2C_INT_AR_P1
GPIO#6
GPIO#37
VBUS_MON_P1/GPIO
SDA_3/MUX_CTRL_3_P1/VSEL_2_P1
SDA_4/MUX_CTRL_2_P1
SCL_4/MUX_CTRL_1_P1
VBUS_P_CTRL_P1
VBUS_C_CTRL_P1
VBUS_DISCHARGE_P1
PD_VBUS_P_CTRL1 [43]
PD_VBUS_C_CTRL1 [43]
PD_VBUS_DISCHG [43]
PD Function
HPD_P1/GPIO
CPU_DP_HPD_MUX R3729 0R2J-2-GP
CPU_DP_HPD_R [8,38,57]
CC2_P1
PD_CC2 R3727 0R2J-2-GP
USBC1_CC2_CONN [38]
CC1_P1
PD_CC1 R3728 0R2J-2-GP
USBC1_CC1_CONN [38]
R3725 10KR2F-2-GP
PL 100K to GND on CPU side
Vince,20161028
Vendor 2016/10/28 confirm
DOCK_USB_EN_A [38]
I2C_DATA_PD [38]
I2C_CLK_PD [38]
I2C to MUX
USBC1_CC1_CONN
USBC1_CC2_CONN
C3711 SC390P50V2KX-GP-U
C3712 SC390P50V2KX-GP-U
Vince,20170119
R3750 30KR2F-GP
R3752 30KR2F-GP
CCG4_ID_1
CCG4_ID_2
R3751 3KR2F-GP
R3753 10KR2F-L1-GP
DOCK_USB_EN_B [38]
PD_SWD_IO
PD_SWD_CLK
SWD_IO/AR_RST#
SWD_CLK/I2C_CFG_EC
INT#_Typec_R
I2C_INT_EC
[24] INT#_Typec
[24] CCG4_I2C_SDA
[24] CCG4_I2C_SCL
I2C_SDA_SCB1_EC
I2C_SCL_SCB1_EC
VCONN_MON_P1
VCONN_MON_P1/GPIO
[43] CCG4_OVP_TRIP_P1
OVP_TRIP_P1
Vince,20160922
Vince,20170119
SCL_3
GPIO#27
GPIO#21
PD_XRES
XRES
GND
GPIO#30
GPIO#34
GPIO#35
GPIO#36
GPIO#38
GPIO#39
GPIO#40
NC#22
NC#24
RN3701 SRN2K2J-1-GP
RN3702 SRN2K2J-1-GP
Vince,20161011
R3706 1MR2J-1-GP
R3735 2MR2-GP
+3VALW_EC
R3707 2K2R2J-2-GP
INT#_Typec_R
Vince,20161117
For Dead Battery modify
From System
Vince,20160922
3D3V_S5
VCC3PD
D3701 SBA0520Q-R1-00001-GP-U
D3702 SBA0520Q-R1-00001-GP-U
VBUS to 3.3V
U3702
TPS70933DRVR-GP-U
TPS70933_EN
VREG3PD
RF
Vince,20161110
R3724 4K7R2J-2-GP
C3716 SCD1U16V2KX-3GP
Vince,20161110
R3738 10KR2J-3-GP
R3739 100KR2J-1-GP
Q3701 2N7002K-2-GP
TPS70933_EN_G
TPS70933_EN
C3720 SCD2U10V3KX-GP
For Debug
R3736 0R2J-2-GP
PD_SWD_IO
PD_SWD_CLK
TP3703 TPAD14-OP-GP
PD_XRES
Vince,20170330
6 Single Port - Intel - DDM support - StarLord KBL - R L0 L2
Voltage level | Voltage value
L0 | 0V
L1 | 3.3V/8
L2 | 2 * 3.3V/8
L3 | 3 * 3.3V/8
L4 | 4 * 3.3V/8
L5 | 5 * 3.3V/8
L6 | 6 * 3.3V/8
L7 | 7 * 3.3V/8
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
(Reserved)
Size A3
Document Number
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Rev A00
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Main Func = TYPEC MUX

Vince,20161012

DisplayPort Source

USB HOST

U3801 TUSB546-DCIRNQR-GP

Vince,20161026

Vince,20170721

Vince,20170721

FLIP POL	CTL0 AMSEL	CTL1 EN	Mux Operation
X	LOW	LOW	POWER DOWN
LOW	LOW	HIGH	4-lane Orientation 1
HIGH	LOW	HIGH	4-lane Orientation 2
LOW	HIGH	HIGH	2-lane Orientation 1
HIGH	HIGH	HIGH	2-lane Orientation 2
LOW	HIGH	LOW	USB3.1 only Orientation 1
HIGH	HIGH	LOW	USB3.1 only Orientation 2

	DCI	Non DCI
23 CTL1/HPDIN	DP ENABLE in GPIO mode HPD in I2C mode	DP Enable in GPIO mode/ Unused in I2C mode
29 CAD_SNK/DCI_DAT	AUX Snoop EN in GPIO mode DCI_DAT in I2C mode	AUX Snoop EN in GPIO mode EN in I2C mode
32 DCI_CLK	HPD in GPIO mode DCI_CLK in I2C mode	HPD

Vince,20160922

USB1 SKT-USB34-21-GP-U

Vince,20170517

U3802 TS3DS10224RUKR-GP

Vince,20161004

Vince,20160929

Vince,20161028

FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

Size	Document Number	Rev
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Main Func = USB3.0 Port1

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

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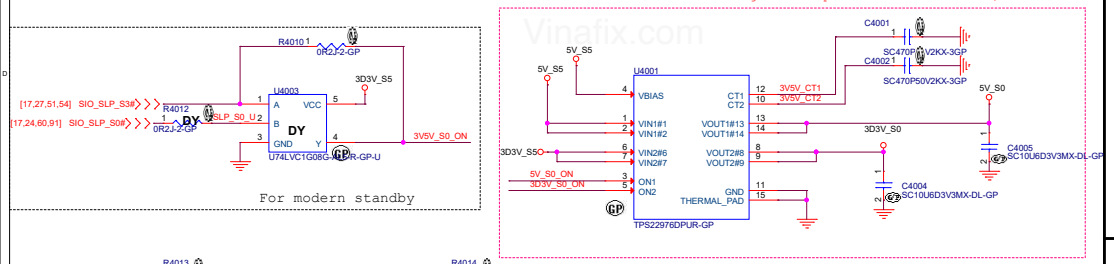
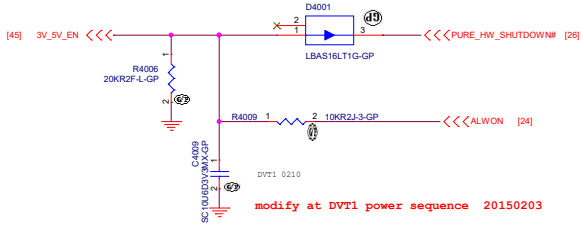
SSID = Power Plane & Sequence

ROSA Run Power

change common part PN:074.05027.0093, 20170110





modify at DVT1 power sequence 20150203

20150116 2032

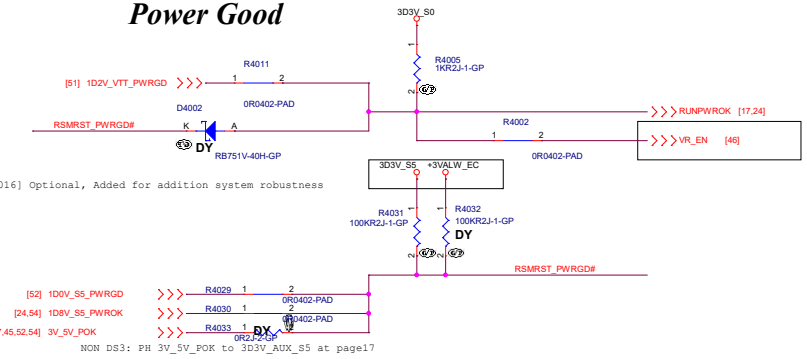
5V_S0

5V_S0 Comsumption
Peak current 5A

3D3V_S0

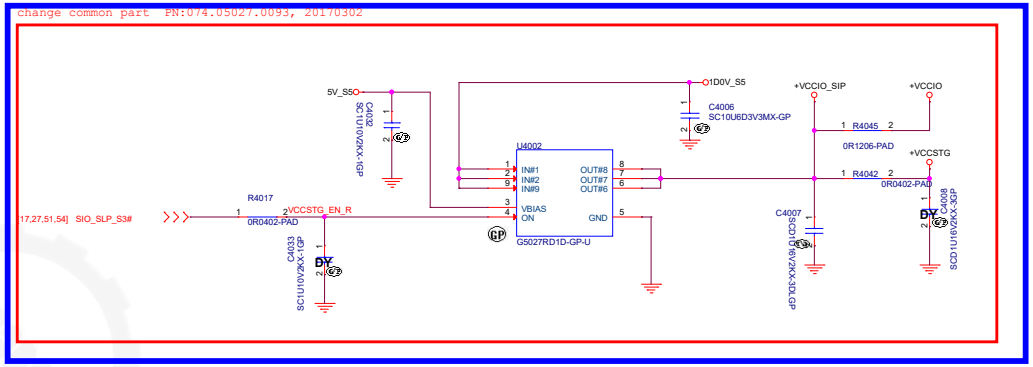
3D3V_S0 Comsumption
Peak current 2.5A

Power Good



VCCIO and VCCSTG

change common part PN:074.05027.0093, 20170302



EOPIO and EDRAM

Vince,20161012

Vince,20161027

Vince,20161012

Vince,20161012

Vince,20161012

+V_EDRAM_VR

Imax = 6 A
Rds on = 4.65mohm

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

Vince,20161012

V1.8S

Vince,20161012

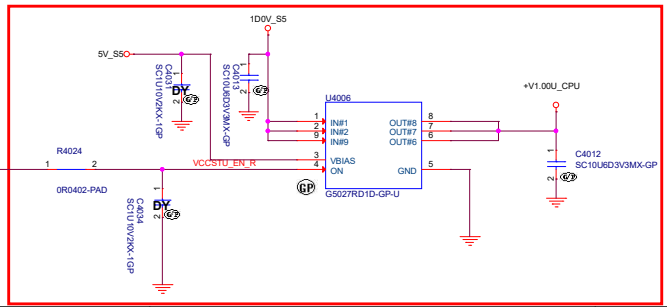
MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST

Vince,20161031

change common part PN:074.05027.0093, 20170110



<Core Design>

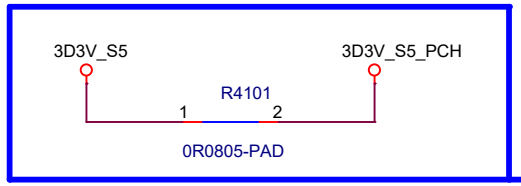
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size: A2 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 40 of 106

Main Func = Power Plane & Sequence



Reserve by NON DS3 function 20150413

Vince,20161031

DS3

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Connected_Standby(1/2)+DS3		
Size: A4	Document Number: Starlord KBL-R	Rev: A00
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Main Func = DIMM1

Main Func = DIMM2

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Connected_Standby(2/2)*

Size: A3 | Document Number: Starlord KBL-R | Rev: A00

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SSID = ADT Input

Layout Note:
PSID Layout width > 25mil

Pin Definition: TBD

60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

20170623 Reserve

2016/01/07 mofiy

Vince,20161110

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

PD_VBUS_C_CTRL1 = 1 (Consumer Path OFF)
PD_VBUS_C_CTRL1 = 0/Z (Consumer Path ON)

If=0.3A

20170622 Reserve

Vince,20170519

VBUS_C_CTRL = 1 (Consumer Path ON)
VBUS_C_CTRL = 0/Z (Consumer Path OFF)

Vince,20161004

VBUS overvoltage output indicator (active LOW)

PD_VBUS_DISCHG = 1 (VBUS Discharging)
PD_VBUS_DISCHG = 0/Z (VBUS not discharging)

PD_VBUS_P_CTRL1 = 1 (Provider Path ON)
PD_VBUS_P_CTRL1 = 0/Z (Provider Path OFF)

Id=115mA

SSID = M-BAT Input

Batt Connecter

Placement: Close to Batt Connector

Vince,20161013

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN
Size: A2
Document Number: Starlord KBL-R
Rev: A00
Date: Friday, December 08, 2017
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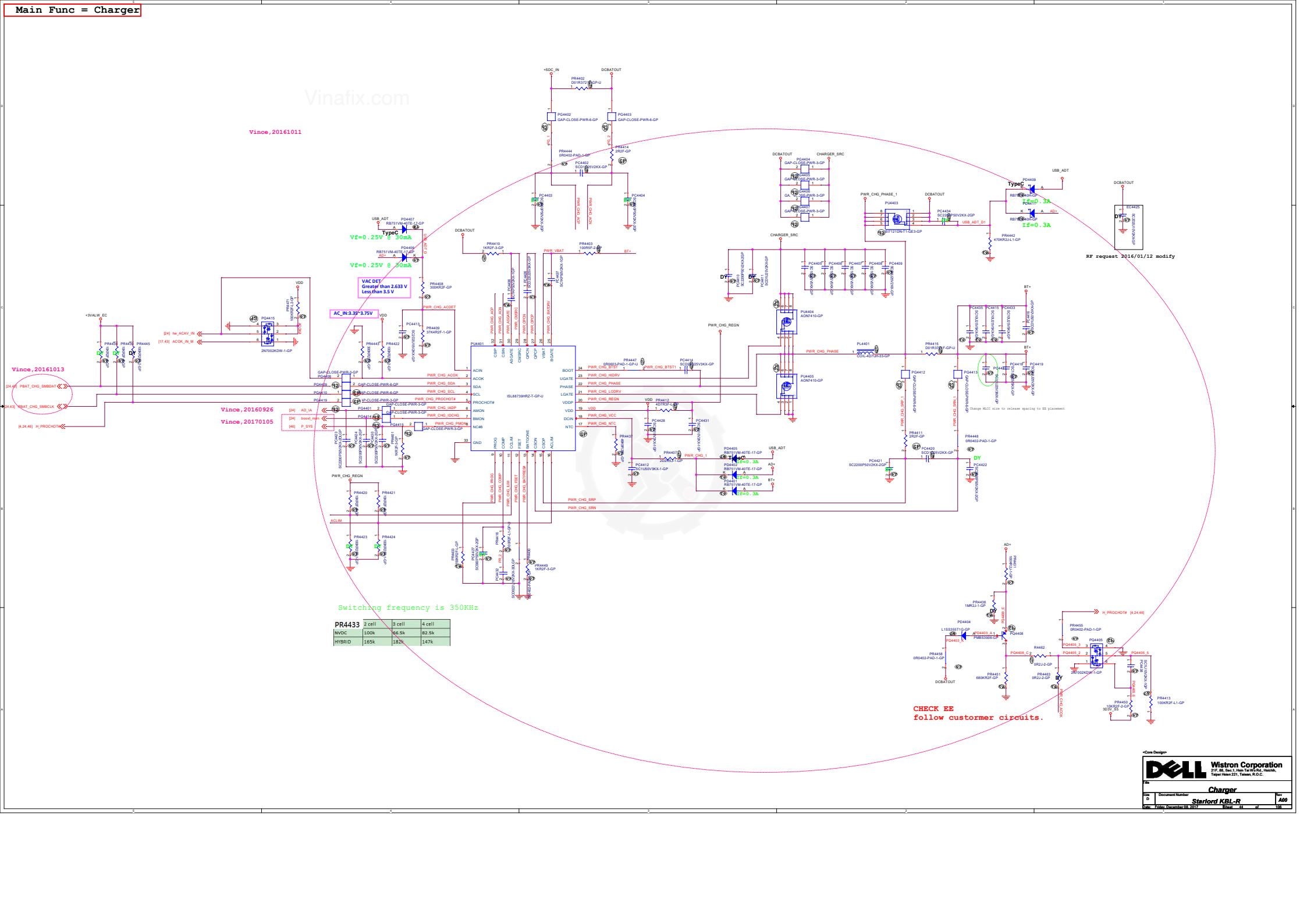
Main Func = Charger



PR4433	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger

Size	Document Number	Rev
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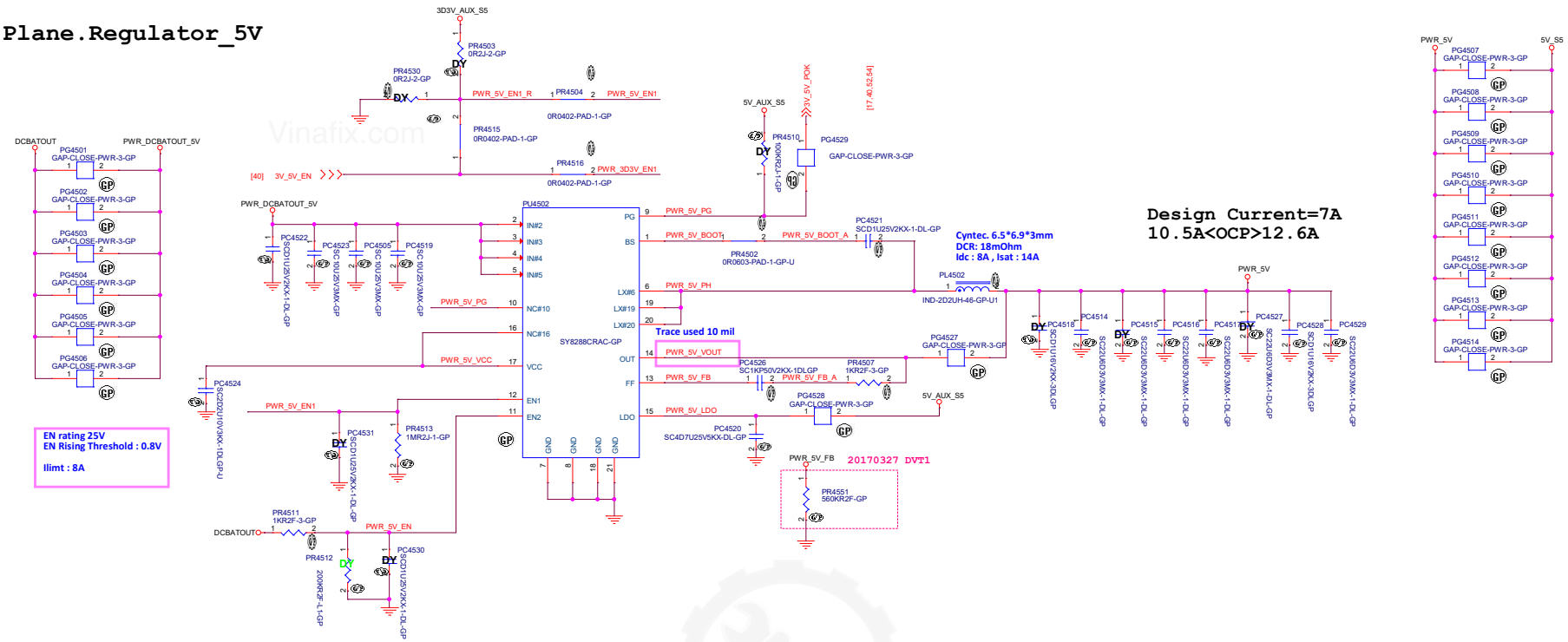
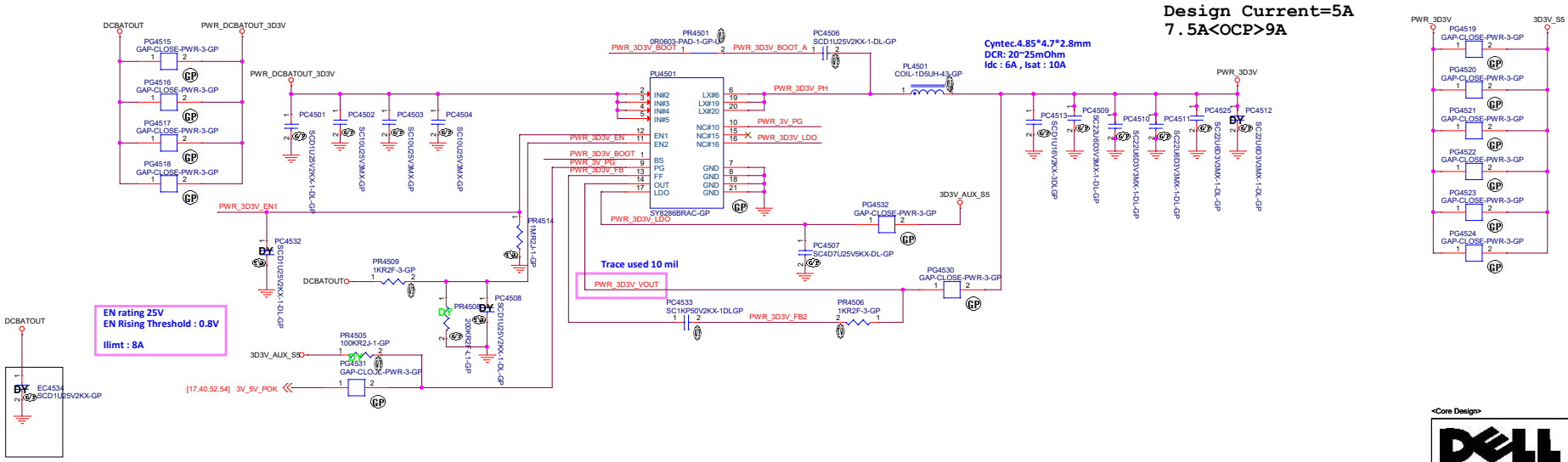
SSID = PWR.Plane.Regulator_5V

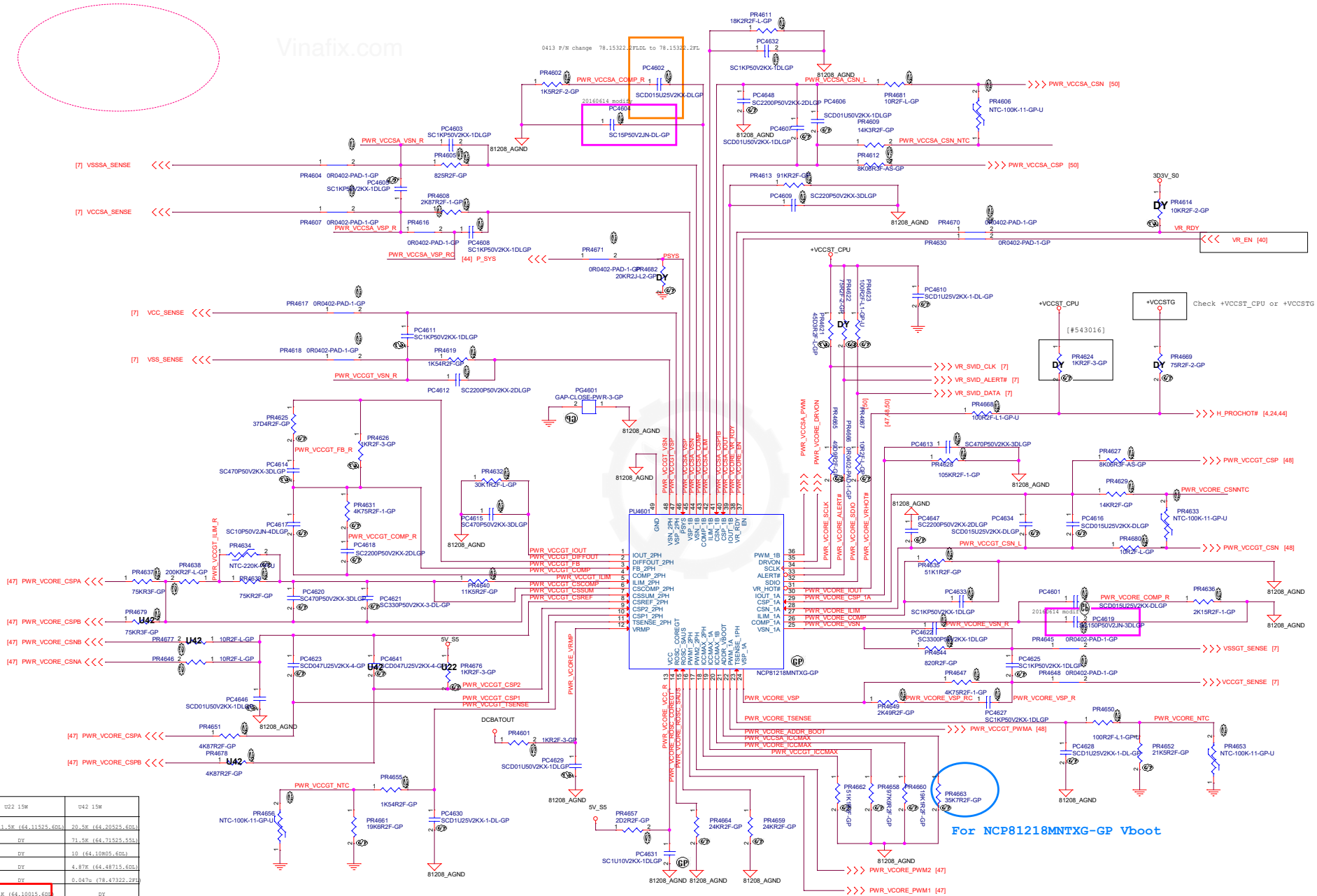


SSID = PWR.Plane.Regulator_3D3V



SSID = CPU_CORE

Vince,20160922



	U22 15W	U42 15W
PR4640	11.5K (64.11525.6DL)	20.5K (64.20525.6DL)
PR4679	DY	71.5K (64.71525.55L)
PR4677	DY	10 (64.10R05.6DL)
PR4678	DY	4.87K (64.48715.6DL)
PC4641	DY	0.047u (78.47322.2FL)
PR4676	1K (64.10015.6DL)	DY
PR4662	51.1K (64.51125.6DL)	100K (64.10035.6DL)
PR4658	97.6K (64.97625.6DL)	97.6K (64.97625.6DL)
PR4635	51.1K (64.51125.6DL)	51.1K (64.51125.6DL)
PR4628	105K (64.10535.6DLL)	105K (64.10535.6DLL)
PR4632	30.1K (64.30125.6DL)	26.1K (64.26125.6DL)

20170208

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81208MN_CPU_VCORE(1/3)

Size: A2 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 46 of 105

Main Func = CPU_CORE

Vince,20161020

1020 EMI add

For acoustic noice

Vince,20160922

EVT1_20160901

EVT1_20160810

EVT1_20160829

330uF/2V,
ESR=9mohm,
Ripple current=3000mA

Confirm with EE:
22uF/0805 total 32pcs (DY 5 pcs)

0.15uH,
DCR=0.66mohm,
Idc=36A, Isat=45A

TDC=42A
Iomax=64A
OCP>80A

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCORE(2/3)

Size: A2 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 47 of 105

Main Func = CPU_CORE

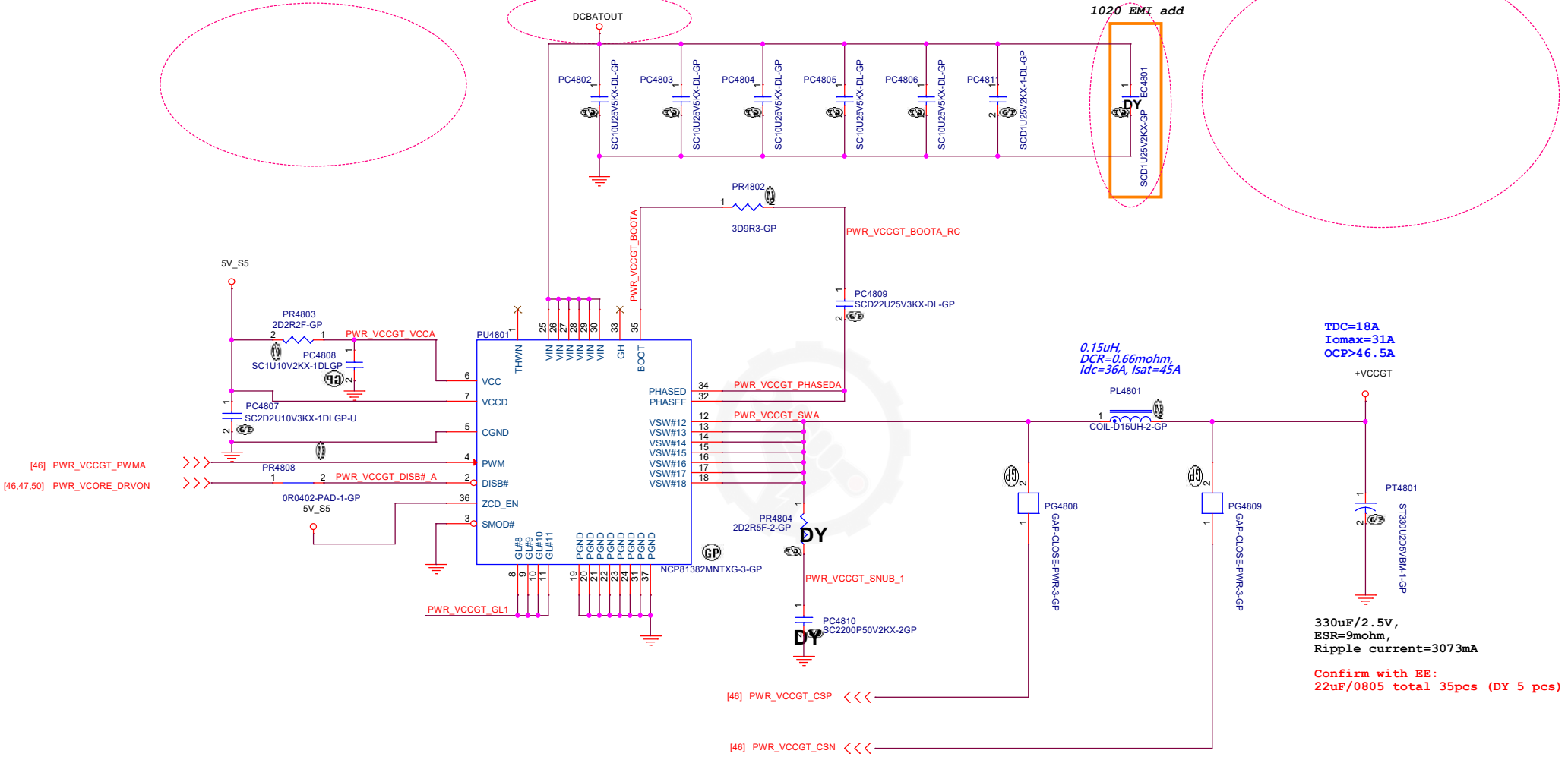
Vince,20160922

Vince,20160929

Vince,20161020

Vince,20160929

1020 EMI add



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81382MN_CPU_VCCGT(3/3)

Size: A3 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 48 of 105

Main Func = CPU_CORE

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP81210MN_CPU_VCCGTUS

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A4	Starlord KBL-R	A00

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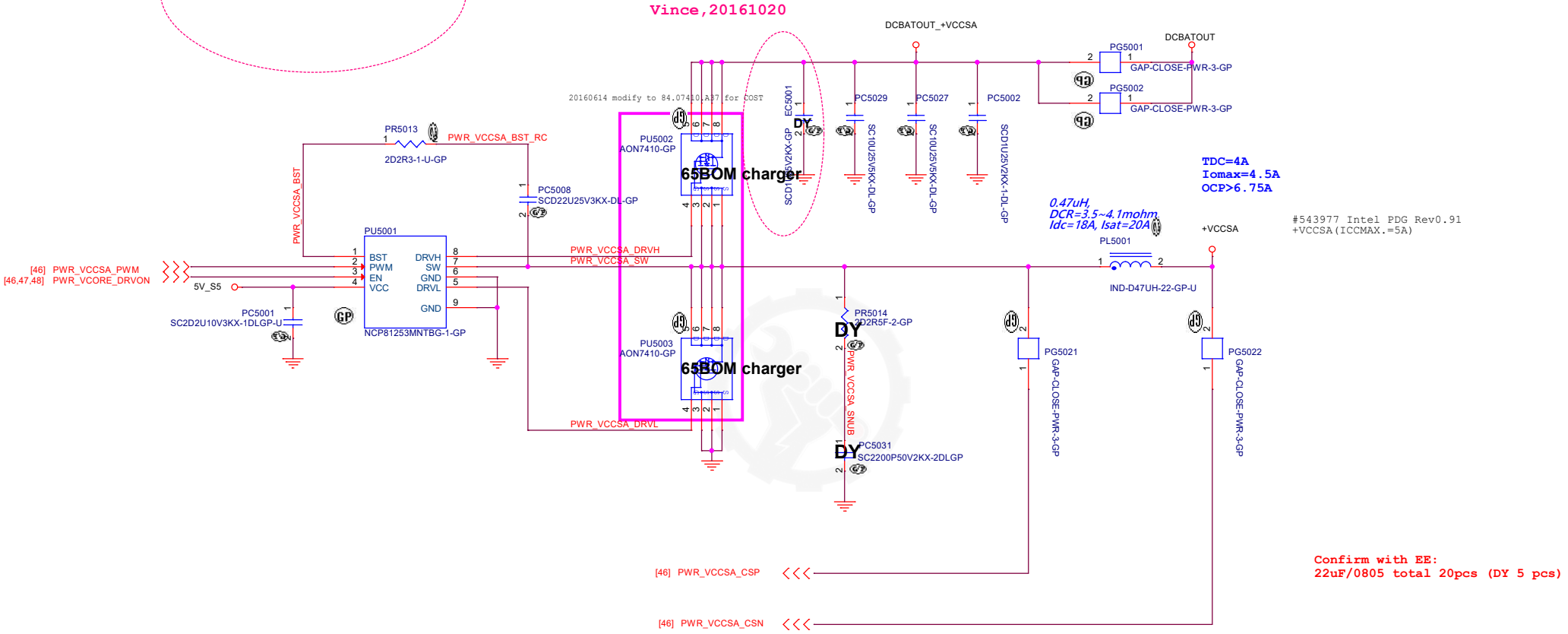
Main Func = CPU_CORE

Vince,20160922

Vince,20161020



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81253MN_CPU_VCCSA	
Size: A3	Document Number: Starlord KBL-R	Rev: A00
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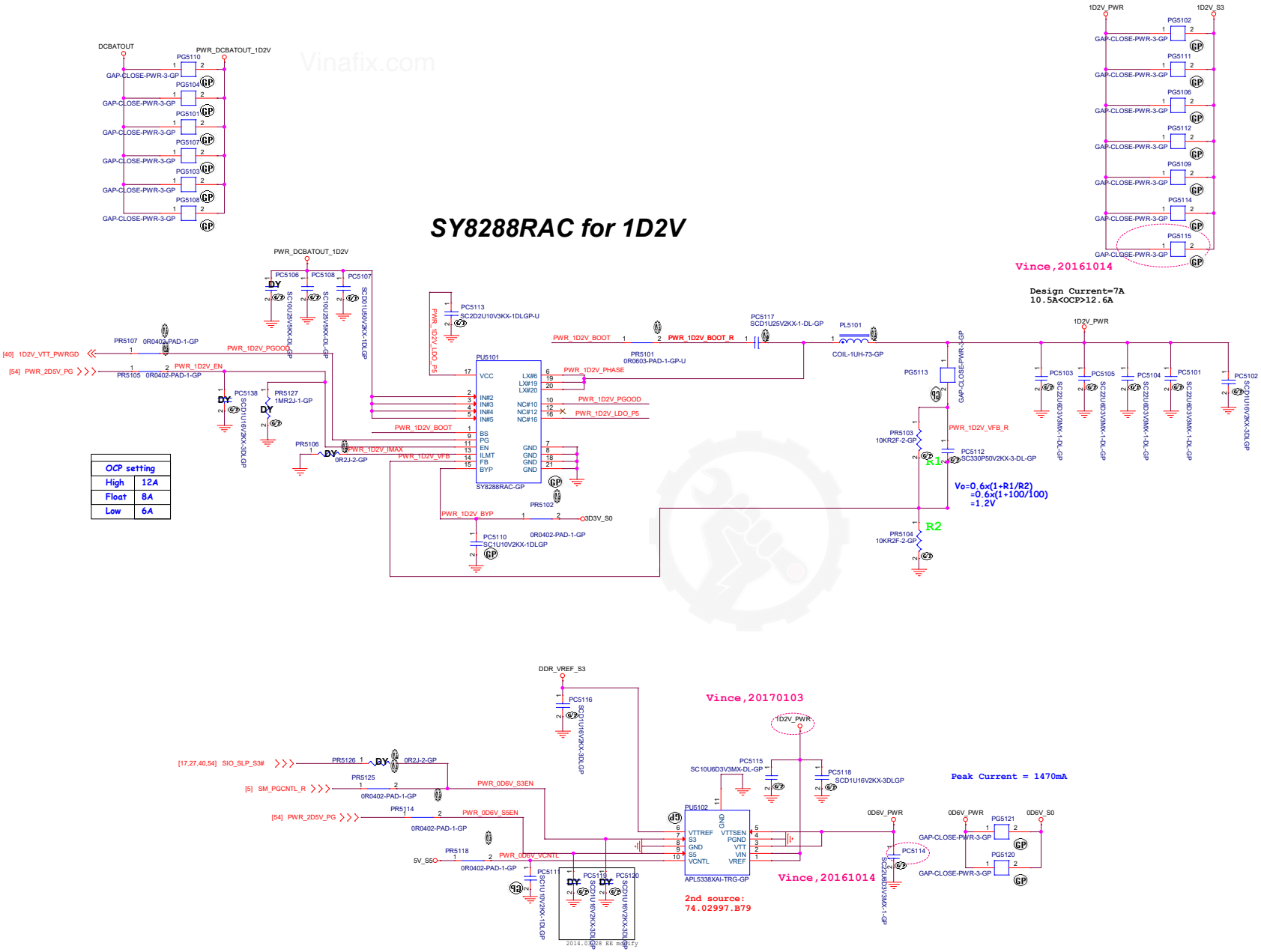
SSID = PWR.Plane.Regulator_1p2v

SY8288RAC for 1D2V



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

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A2	Starlord KBL-R	A00

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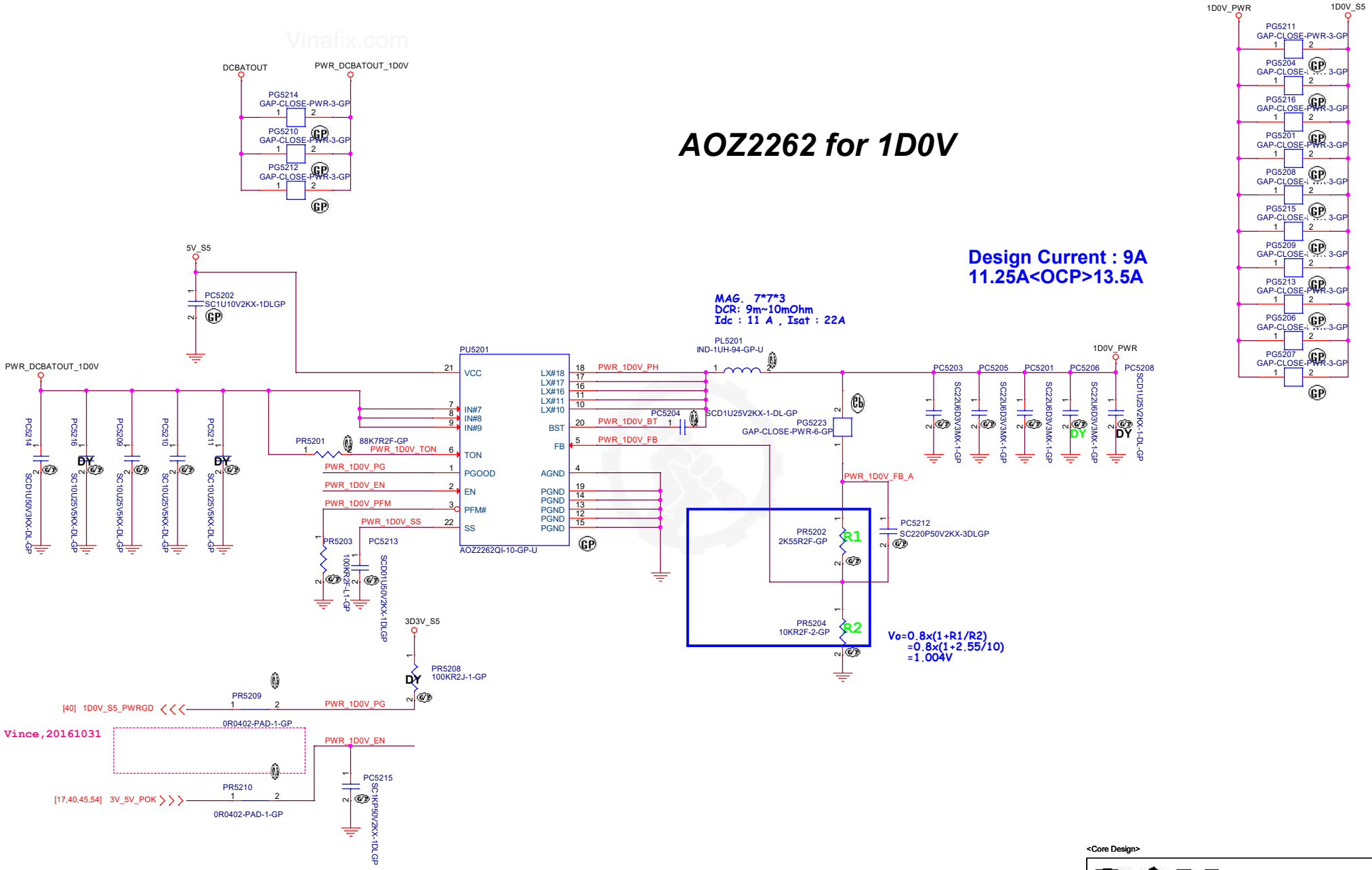
SSID = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D0V

Design Current : 9A
11.25A<OCP>13.5A



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: (Reserved)

Size	Document Number	Rev
A3	Starlord KBL-R	A00

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size	Document Number	Rev
A3	*Starlord KBL-R*	*A00*

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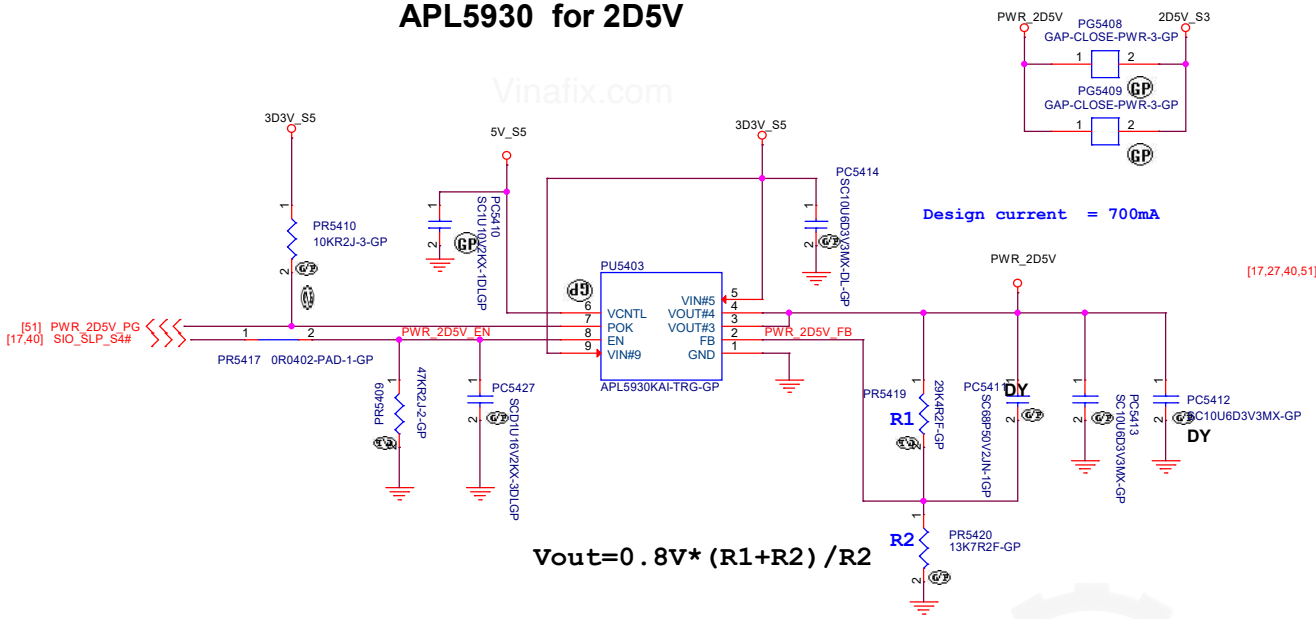
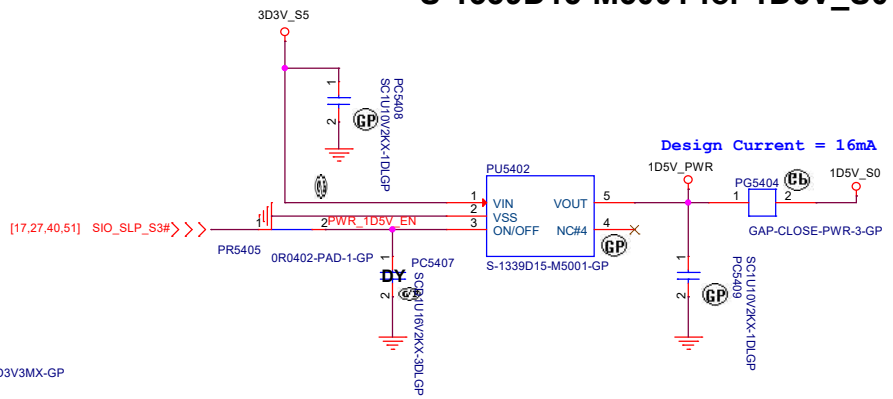
SSID = 1D5V

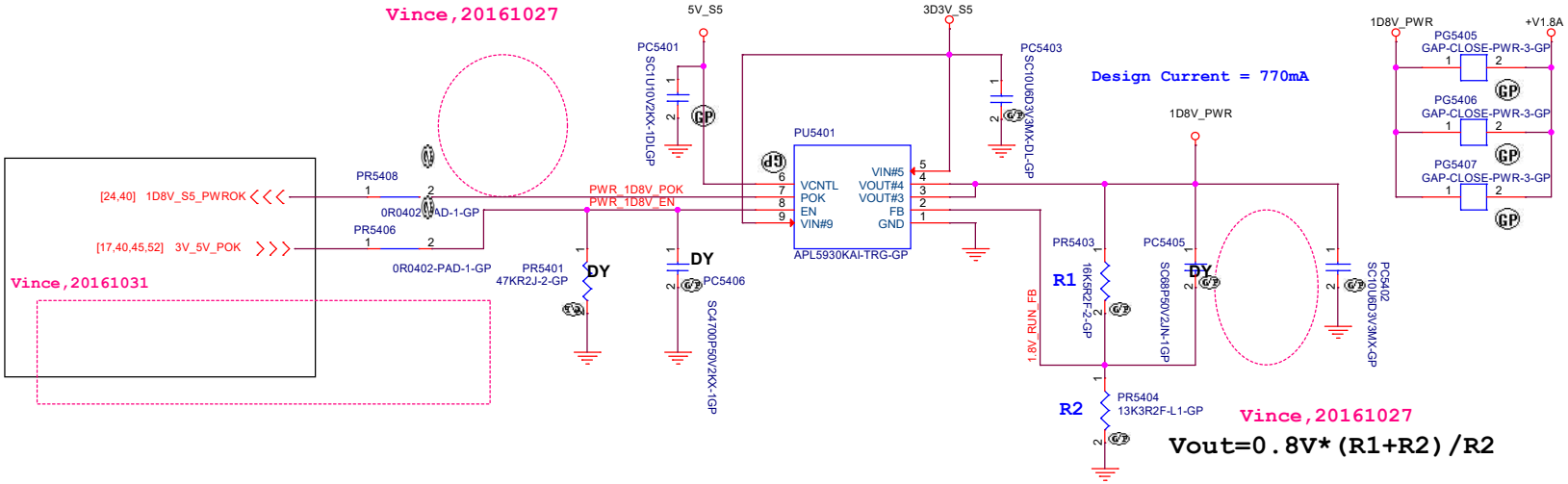
APL5930 for 2D5V



S-1339D15-M5001 for 1D5V_S0



APL5930 for 1D8V_S5



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (Reserved)

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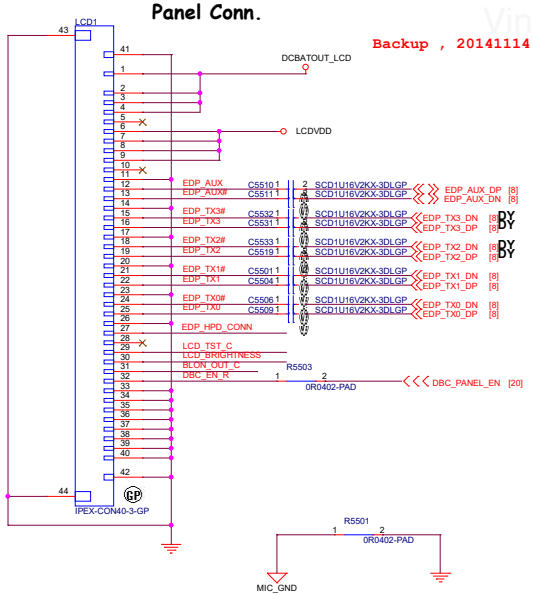
SSID = LCD

Panel Conn.

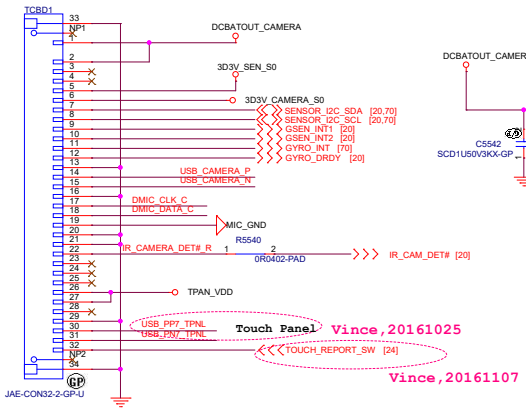
Backup , 20141114



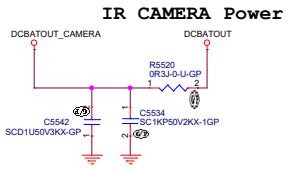
Power Pin Count : 7
GND Pin Count : 9

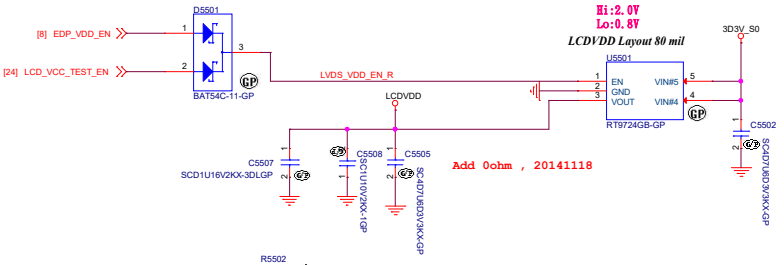
HSYNC

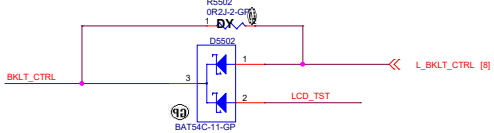
Remove HSYNC schematic
201511276

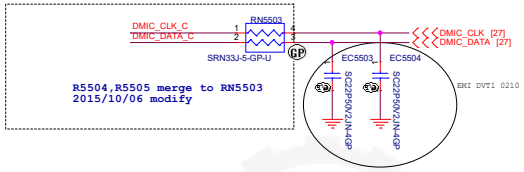


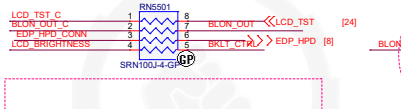
IR CAMERA Power



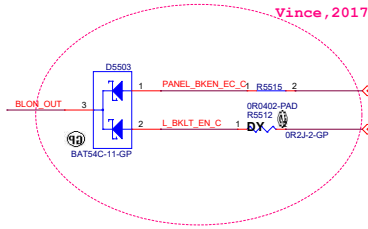




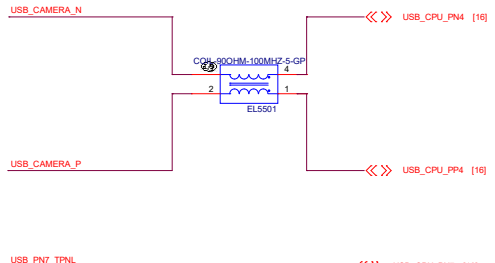




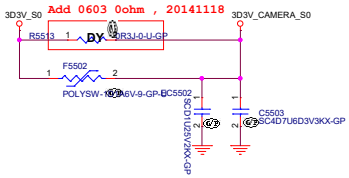
Vince,20170202



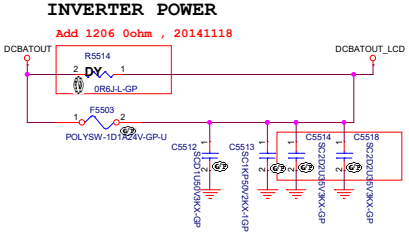
Vince,20161202



CAMERA POWER

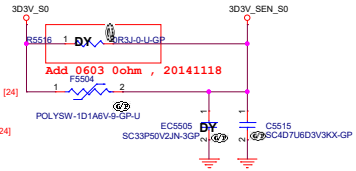


INVERTER POWER

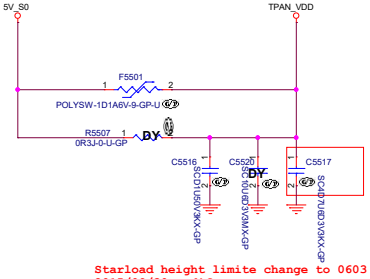


Starload height limite change to 0603 package
2015/09/24 modify

SENSOR POWER



TOUCH PANEL POWER



Starload height limite change to 0603 package
2015/09/30 modify

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Title: LCD&CAM&DMC&Touch
Size: A2
Document Number: Starlord KBL-R
Rev: A00
Date: Friday, December 08, 2017
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Title: CRT

Size	Document Number	Rev
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SSID = HDMI

vince 20170516 EMI request

260mA

change common part PN:71.08201.G03, 20170110

Exchange 0603 0ohm , 20141118

change to 180 for HDMI signal quality 2016/01/05

vince 20170516 EMI request

Change to 4.12k 20170327

vince 20170315

HDMI CONN

X01 0227

For DIODE in case of leakage from HDMI1

Remove DUMMY-HDMI , 20141118

Vince,20161101

20170622 Type-c HPD close window

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Title: HDMI

Size: A3 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 57 of 106

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Title: *(Reserved)*		
Size: A3	Document Number: *Starlord KBL-R*	Rev: *A00*
Date: Monday, August 28, 2017	Sheet 58 of 106	

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Title: *(Reserved)*

Size	Document Number	Rev
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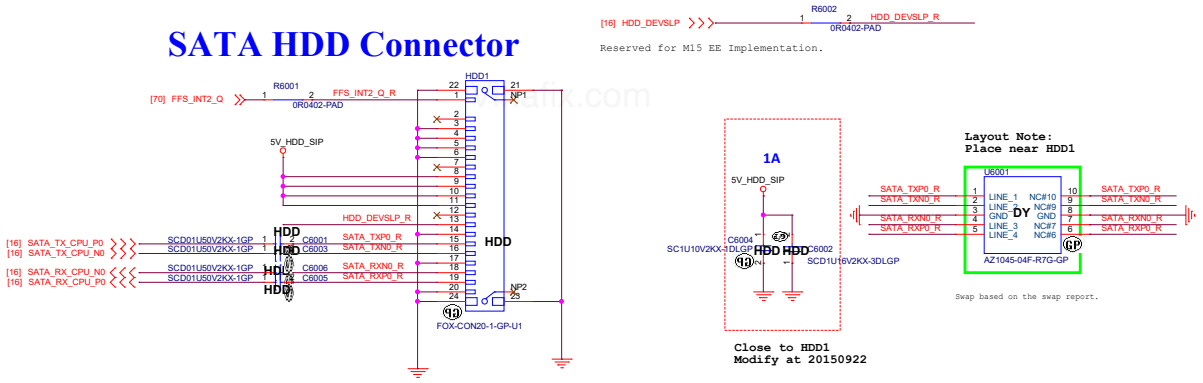
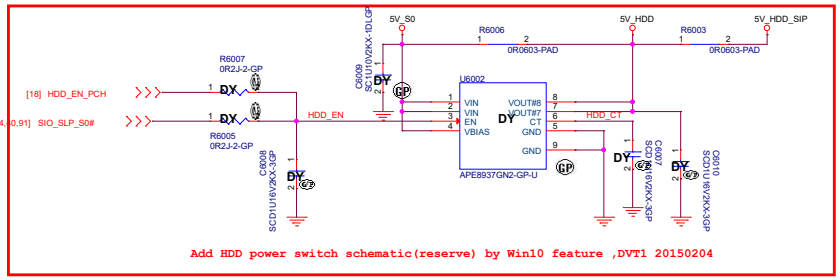
Date: Monday, August 28, 2017 Sheet 59 of 106

SSID = HDD

SATA HDD Connector





Main Func = ODD

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Title: SATA IF_HDD/ODD

Size: A2 | Document Number: Starlord KBL-R | Rev: A00

Date: Friday, December 08, 2017 | Sheet 60 of 106

Main Func = WLAN

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF_WLAN CONN

Size	Document Number	Rev
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Date: Monday, August 28, 2017 Sheet 61 of 106

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<Core Design>

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Title

Reserved

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SSD = M.2

Vince,20160929

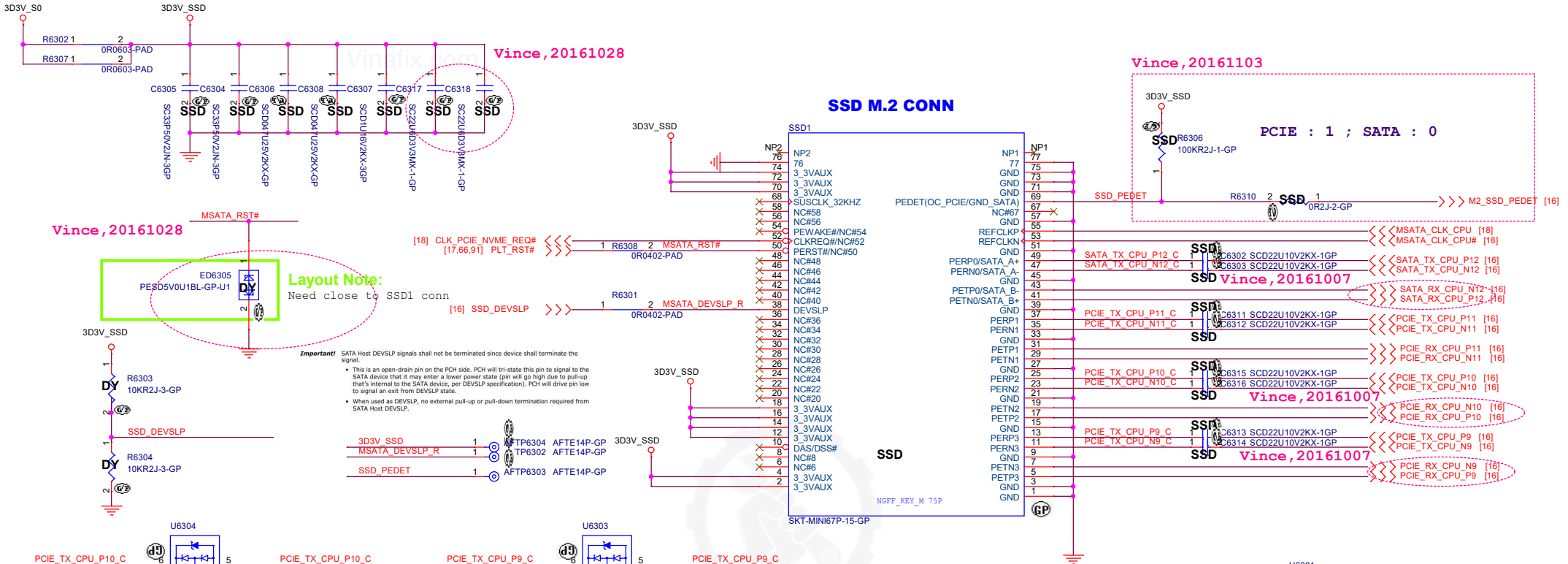

Table 13-12. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, please refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines"" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

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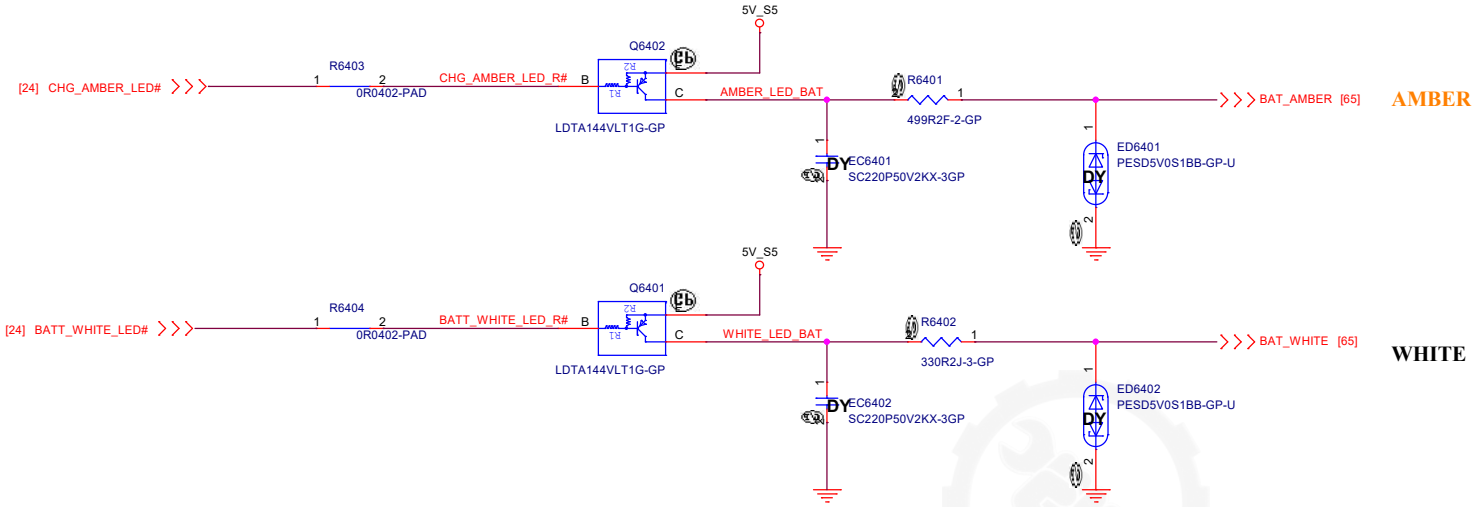
A3	*Starlord KBL-R*	*A00*

Date: Friday, December 08, 2017 Sheet 63 of 106

SSID = Power BTN

Battery LED1 (AMBER_LED)

Low actived from KBC GPIO

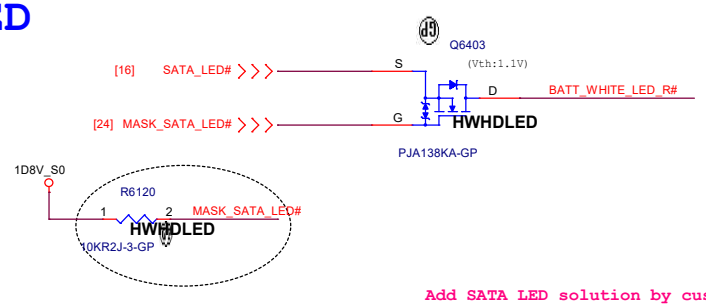


Battery LED2 (WHITE_LED)

Low actived from KBC GPIO

Vince, 20170116

SATA LED



Add SATA LED solution by customer request 2016/02/03

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Title	LED Board&Power Button	
Size A3	Document Number Starlord KBL-R	Rev A00
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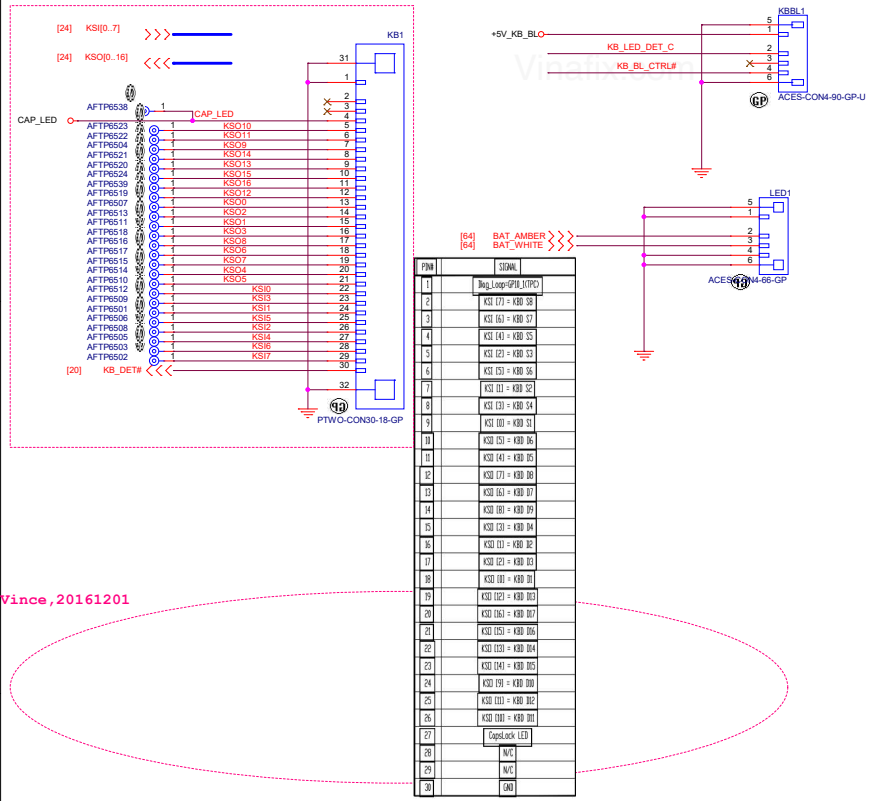
SSID = KB

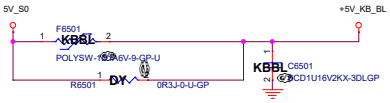
Keyboard

Vince,20170208

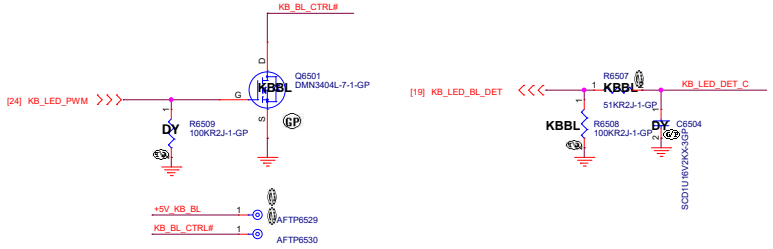


PIN#	SIGNAL
1	Reg_Loop=GPI8_1(TPC)
2	KSI (7) = KBD S8
3	KSI (6) = KBD S7
4	KSI (4) = KBD S5
5	KSI (2) = KBD S3
6	KSI (5) = KBD S6
7	KSI (1) = KBD S2
8	KSI (3) = KBD S4
9	KSI (0) = KBD S1
10	KSO (5) = KBD D6
11	KSO (4) = KBD D5
12	KSO (7) = KBD D8
13	KSO (6) = KBD D7
14	KSO (8) = KBD D9
15	KSO (3) = KBD D4
16	KSO (1) = KBD D2
17	KSO (2) = KBD D3
18	KSO (0) = KBD D1
19	KSO (12) = KBD D13
20	KSO (16) = KBD D17
21	KSO (15) = KBD D16
22	KSO (13) = KBD D14
23	KSO (14) = KBD D15
24	KSO (9) = KBD D10
25	KSO (11) = KBD D12
26	KSO (10) = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND

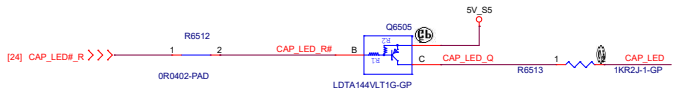
Vince,20161201



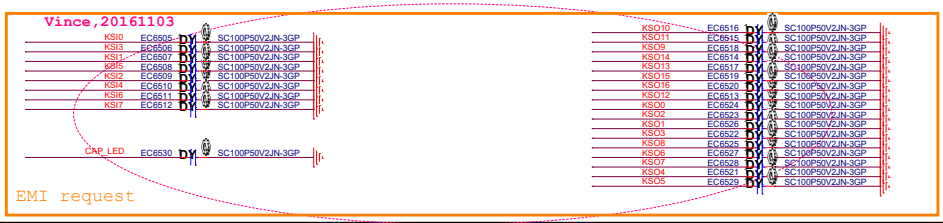
KB Backlight Power Consumption: 285mA max.



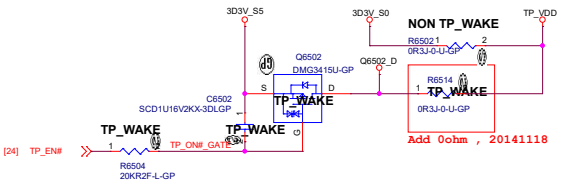
CAP LED Control
LOW actived from KBC GPIO



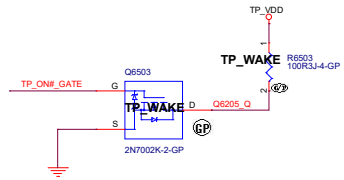
Vince,20161103

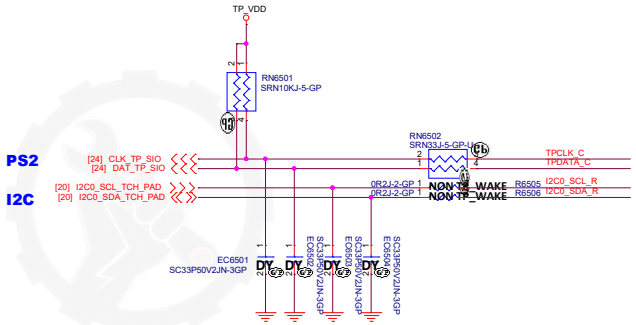


Main Func = TPAD

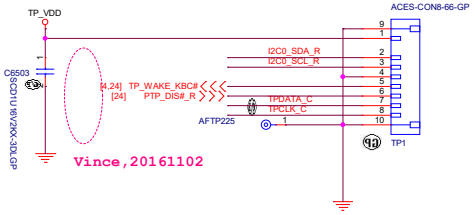


TP_VDD Discharge Circuit



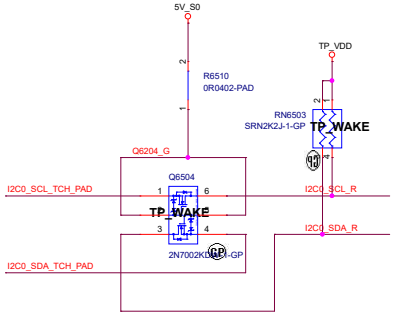


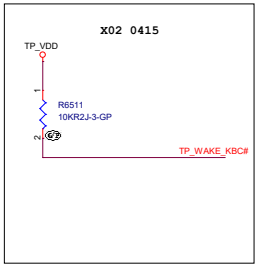
GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)



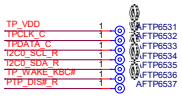
Change pindefine DVT1 0210 1330

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.





Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)



<Core Design>

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Title: Key Board&Touch Pad

Size	Document Number	Rev
A2	Starlord KBL-R	A00

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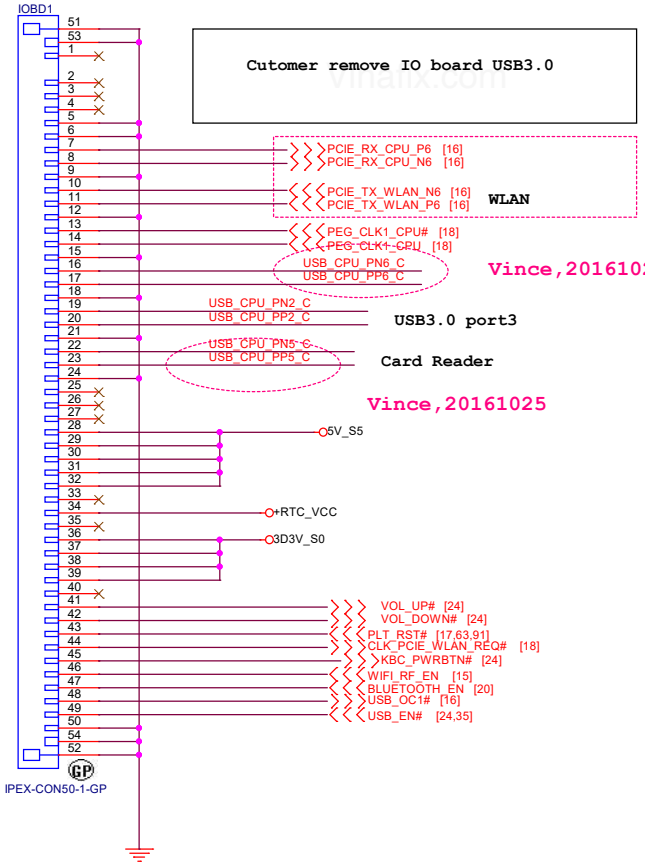
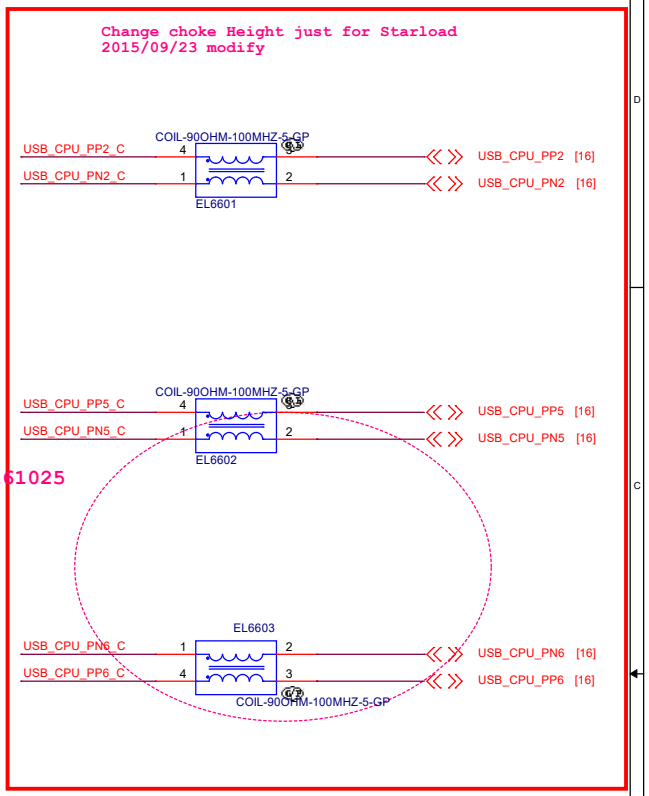
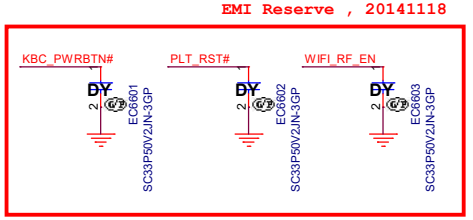
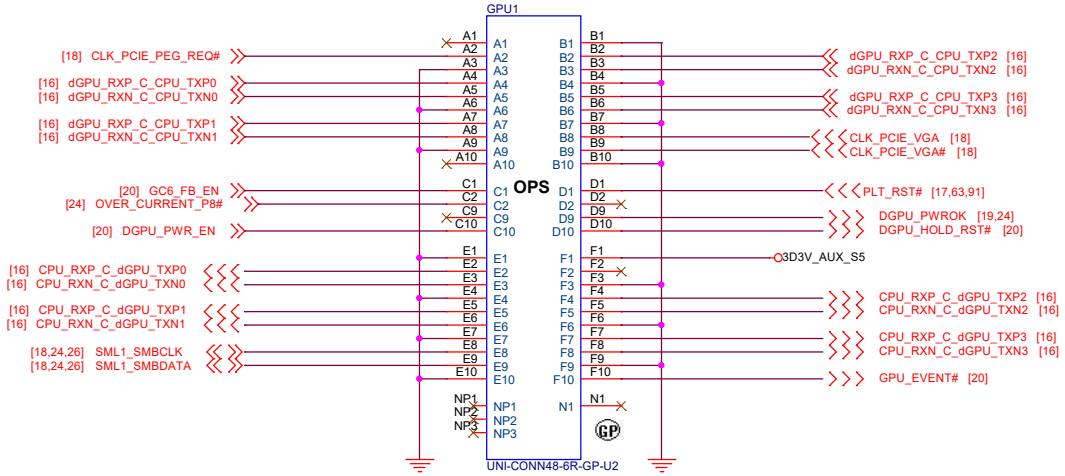
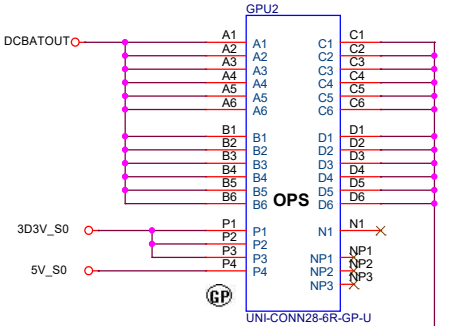
SSID = IO Connector











<Core Design>

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Title: IO Board Connector

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<Core Design>

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Title	*Reserved*	
Size: A3	Document Number: *Starlord KBL-R*	Rev: *A00*
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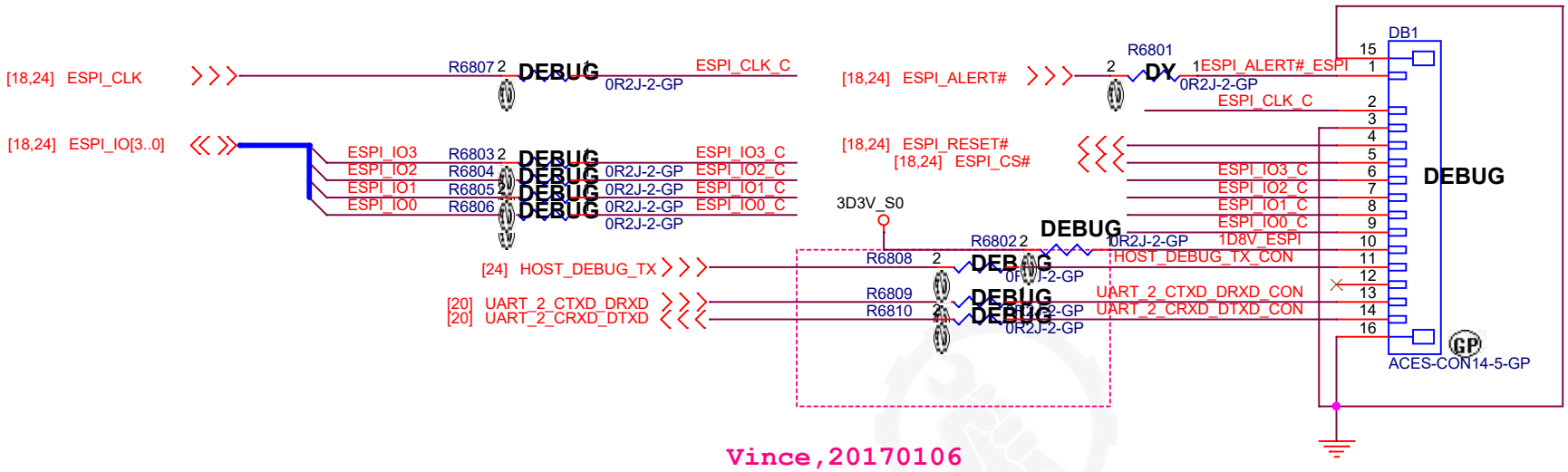
SSID = Debug

Debug Connector



Vince,20170106

<Core Design>

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Title: ***Dubug connector***

Size	Document Number	Rev
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<Core Design>

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Title

Reserved

Size	Document Number	Rev
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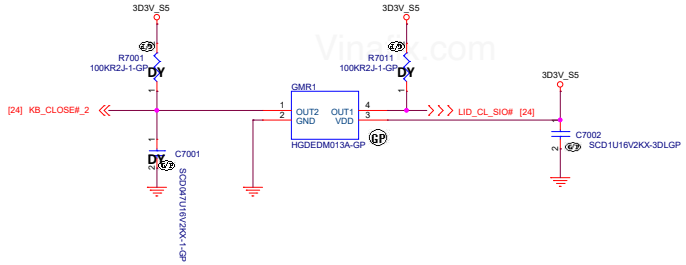
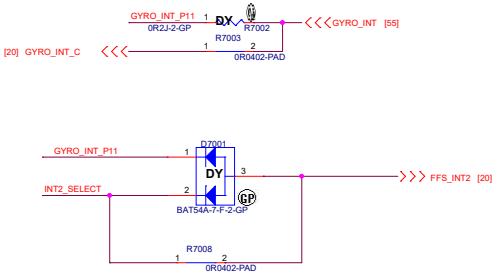
Main Func = Hall Sensor

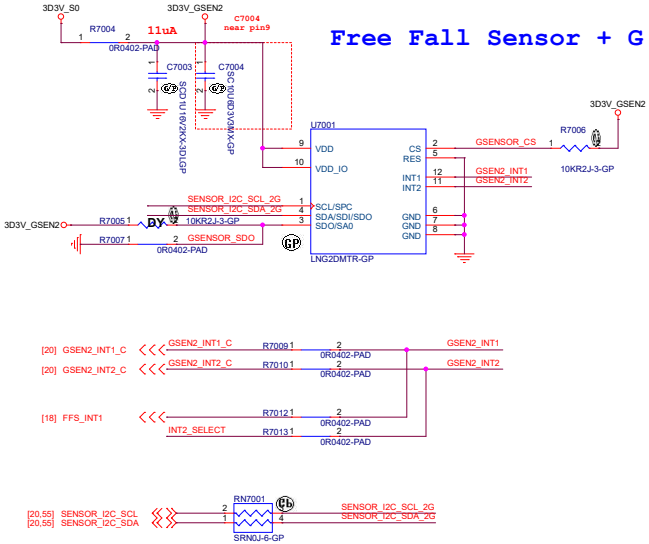
LID sensoe



combine G

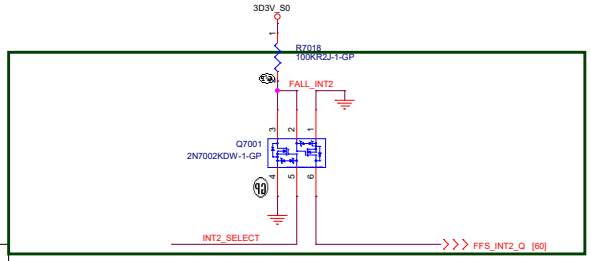


Free Fall Sensor + G Sensor



Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Main Func = dGPU

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Title: GPU(1/5)PEG

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Main Func = dGPU

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Title: GPU(2/5)DIGITALOUT

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Main Func = dGPU

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File:

GPU(3/5)VRAM/F

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Main Func = dGPU

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Title: GPU(4/5)GPIO/STRAP

Size	Document Number	Rev
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Main Func = dGPU

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Title: *GPU(5/5)PWR/GND*

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Main Func = dGPU

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Title: *GPU-VRAM1,2 (1/4)*

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Main Func = dGPU

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Title: *GPU-VRAM3,4 (2/4)*

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Main Func = dGPU

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Title: *GPU-VRAM5,6 (3/4)*

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Main Func = dGPU

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Title: *GPU-VRAM7,8 (4/4)*

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Main Func = dGFX_CORE

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Main Func = dGPU

<Core Design>

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Title: *GPU Discrete Power*

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SSID = UnusedParts

34.4YW18.001

SPR3 SPRING-171-GP
SPR4 SPRING-171-GP
SPR2 SPRING-171-GP
SPR1 SPRING-171-GP

ZZ.00PAD.7F1

H2 HOLE335R178-GP
H4 HOLE335R178-GP
H7 HOLE335R178-GP
H8 HOLE335R178-GP
H9 HOLE335R178-GP
H10 HOLE335R178-GP

ZZ.00PAD.7G1

H5 HOLE335R229-GP
H3 HOLE335R229-GP
H6 HOLE335R229-GP

HS1 STF217R115H101-2-GP
STFSR158R113H62-GP HS2 OPS NP1
STFSR158R113H62-GP HS3 OPS NP1

SSID = EMI

Mind the voltage rating of the caps.

AUD_AGND
EC8901 SCD1U25V2KX-GP
EC8902 SC1KP50V2KX-1GP DY
EC8903 SCD1U25V2KX-GP
EC8904 SC1KP50V2KX-1GP DY

DCBATOUT
EC8905 SC1U50V3KX-GP DY
EC8906 SC2200P50V2KX-2GP DY
EC8907 SCD1U25V2KX-GP DY
EC8908 SCD1U25V2KX-GP

Vince,20161111
EC8930 EC8931 EC8932 EC8939 EC8940 EC8941 EC8942 EC8943 EC8944 EC8945 SCD1U25V2KX-GP DY
EC8952 EC8951 EC8955 EC8947 EC8949 EC8950 EC8953 EC8954 EC8946 EC8948 SCD1U25V2KX-GP DY

5V_S5
EC8914 SCD1U25V2KX-GP DY
EC8915 SCD1U25V2KX-GP DY

5V_S0
EC8916 SCD1U25V2KX-GP DY
EC8917 SCD1U25V2KX-GP DY

1D2V_S3
EC8918 SC1KP50V2KX-1GP
EC8919 SCD1U25V2KX-GP
Change to 0.1uF at 20150427 for EMI

3D3V_S0
EC8909 SCD1U25V2KX-GP DY
EC8910 SCD1U25V2KX-GP DY
EC8911 SCD1U25V2KX-GP DY

3D3V_S5
EC8912 SCD1U25V2KX-GP

+DC_IN
EC8913 SCD1U25V2KX-GP

SSID = RF

1D2V_S3
EC8920 EC8921 EC8922 EC8923 EC8924 EC8925 SCD1U25V2KX-GP
Change to 0.1uF at 20150427 for EMI

1D2V_S3
EC8933 SC2200P50V2KX-2GP DY
EC8934 SC2200P50V2KX-2GP DY
EC8935 SC2200P50V2KX-2GP DY
EC8936 SCD1U25V2KX-GP
EC8937 SCD1U25V2KX-GP
EC8938 SCD1U25V2KX-GP
Change to 0.1uF at 20150427 for EMI

DCBATOUT
EC8927 SC1U50V3KX-GP
EC8928 SC1U50V3KX-GP
EC8929 SC1U50V3KX-GP

Remove EC8931,EC8932,EC8926,EC8930for placement

DCBATOUT
EC8926 SC2D2U10V2KX-GP DY

RF request 2016/01/12 modify

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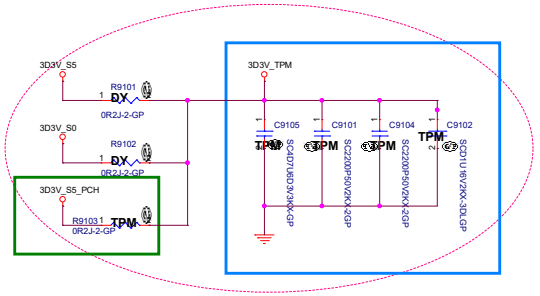
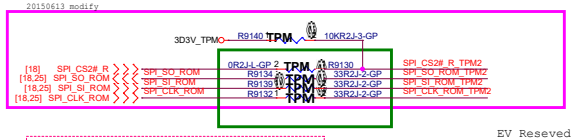
Vince,20161123





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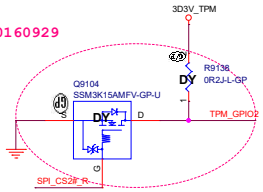

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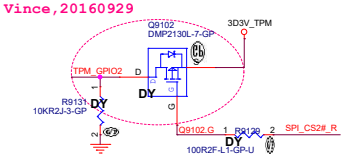
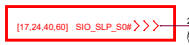
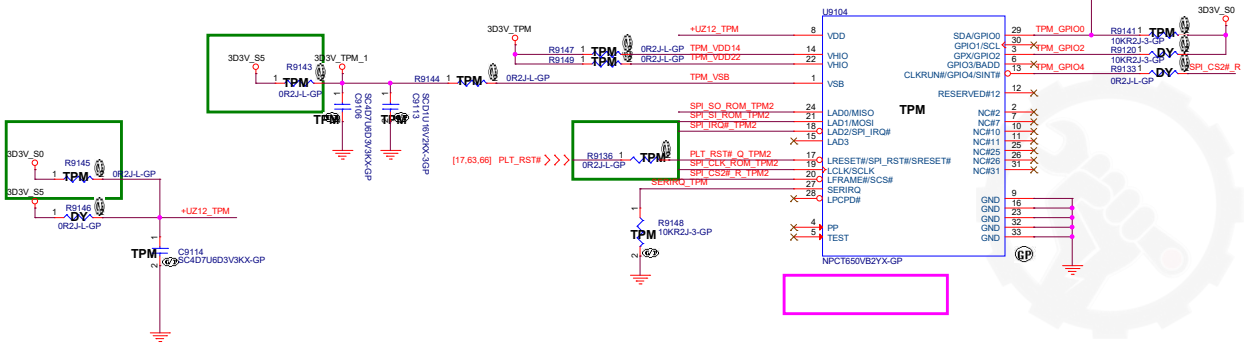


EV Reseved for modern stanby



Vince DVT2,20170511



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Title: *LVDS_Switch*

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Title: CRT_Switch

Size	Document Number	Rev
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Main Func = Debug

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Title: CPU_XDP;PCH_XDP

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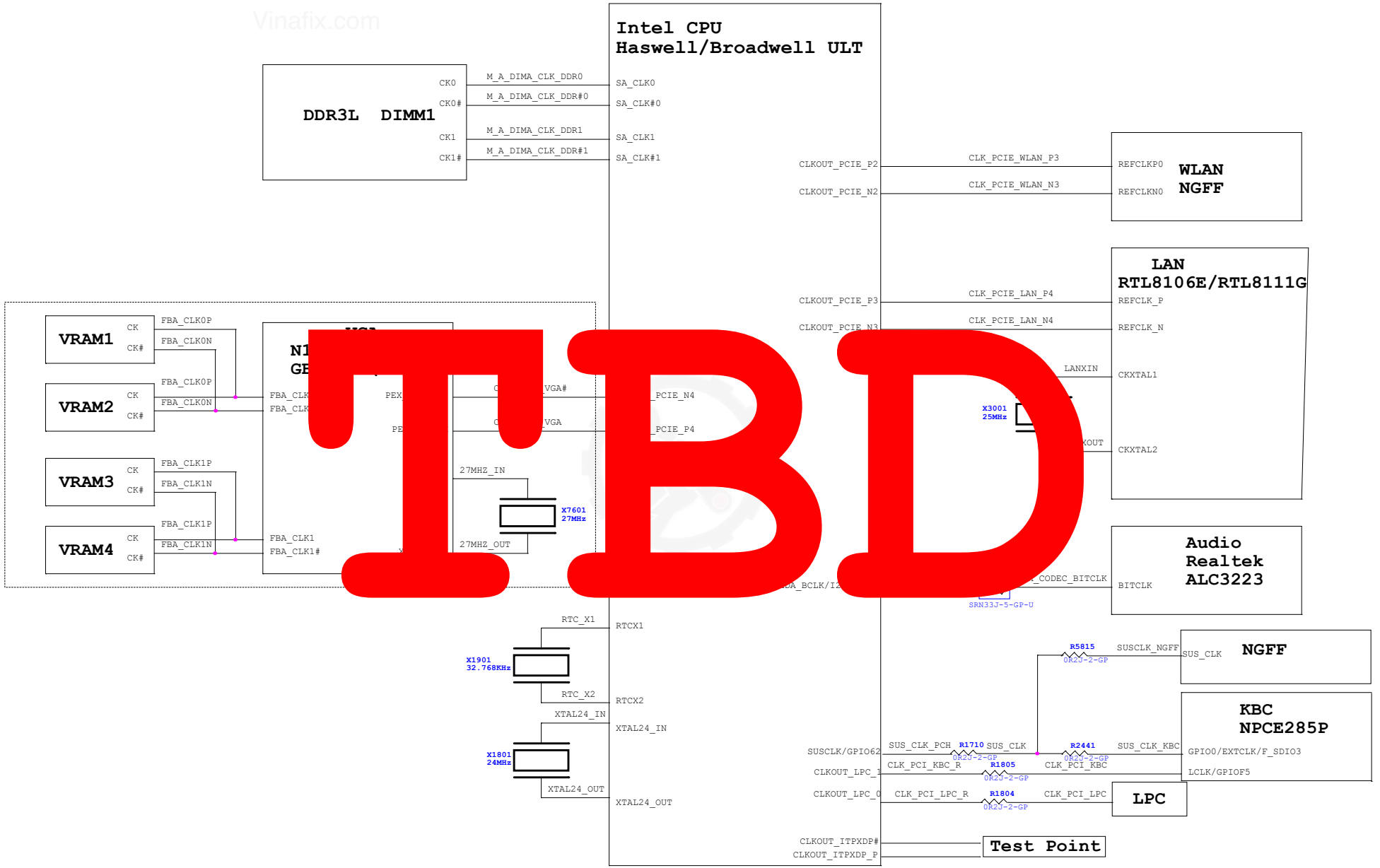
CLK Block Diagram



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Title: CLK Block Diagram

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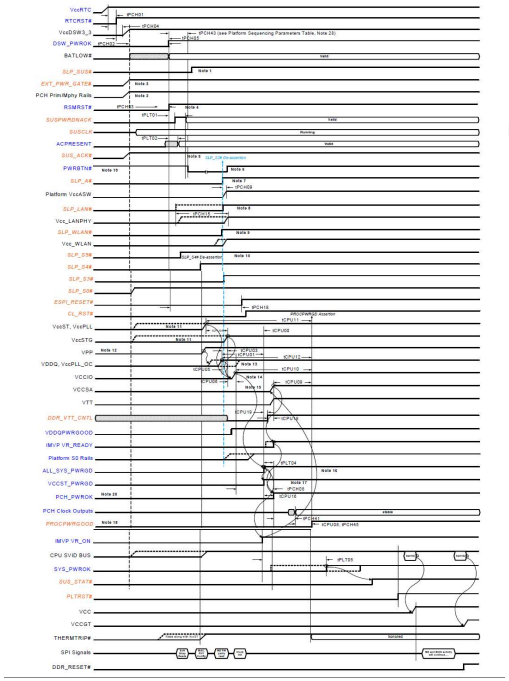
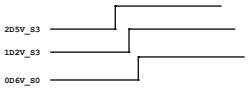
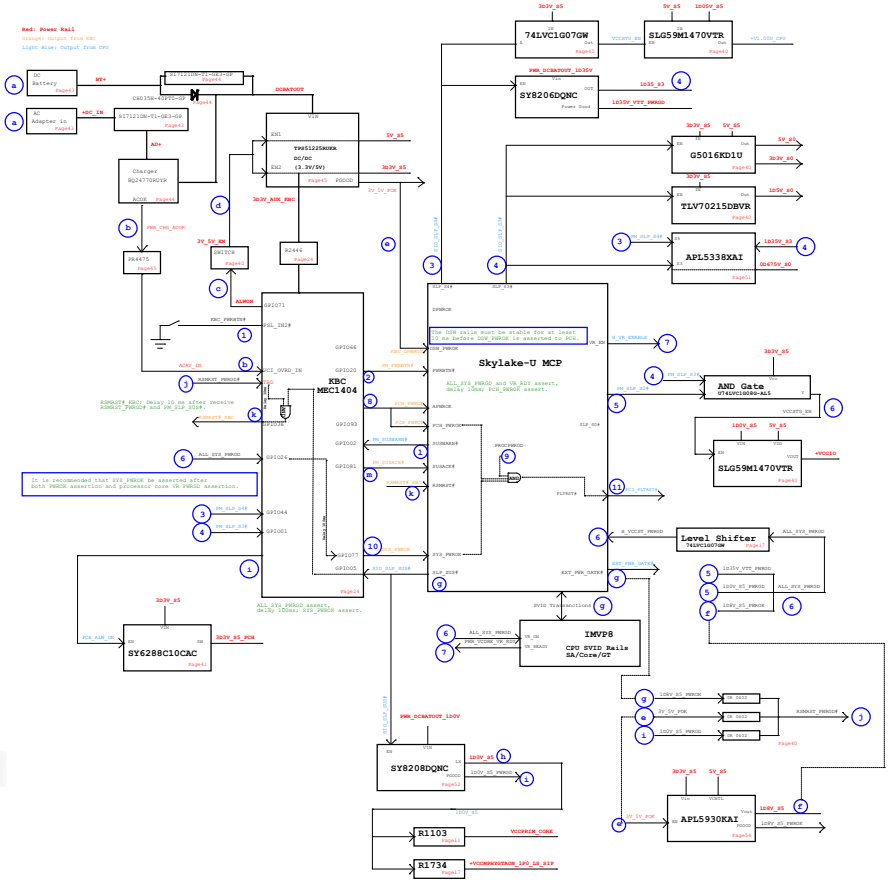
SKL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]

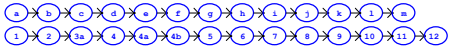


For DDR4 power sequence

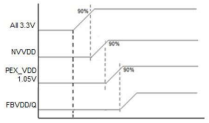


Tulip Skylake POWER UP SEQUENCE DIAGRAM (Deep Sx Platform)





[dGPU] N16x Power-Up/Down Sequence



Notes: - All 3.3V includes all rails powered at 3.3V
- PEX_VDD 1.05V includes all rails that are shared

> **Note:**
> - The ramp time for any rail must be more than 40 us and is recommended to be less than 2ms.
> - The ramp up overshoot should not exceed the silicon reliability limit voltage.
> - The previous power rail must ramp up to 90% before the next power rail can start ramping up.
> - No signal should be applied to the GPU before the power rails are fully ramped
> - Refer to the JEDEC Memory Specification for memory related power sequencing.
> - The order of NVVDD and PEX_VDD ramp-up can be reversed during GC6 exit when there is a back-to-back GC6 entry/exit and/or when PEX_VDD takes longer to ramp down during GC6 entry.

3.10.2.2 Power-Down Sequence

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

18.3.2.3 GC6 2.0 Entry/Exit Timing

The following timing diagram in Figure 18-12 and Table 18-3 describes the GC6 2.0 en and exit sequence and timing requirements.

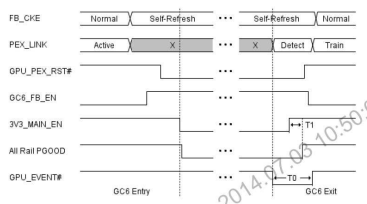


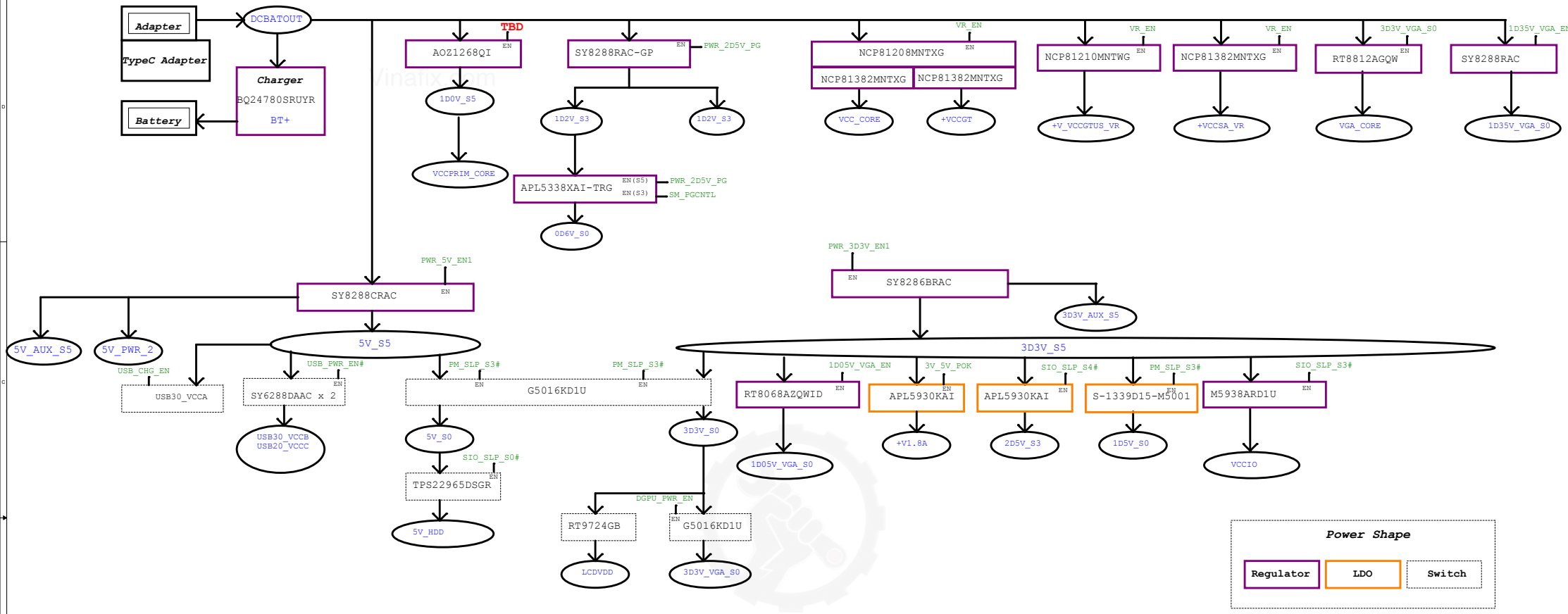
Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram

Table 18-2. GC6 2.0 Entry/Exit Sequence Timing Parameters

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

> **Note:**
> - ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
> - During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
> - All delays should be minimized to increase time spent in GC6 for maximum power saving.
> - The entire entry/exit sequence must complete within 200 ms.

Dell Wistron Corporation — Power Sequence — Starlord KBL-R



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Title: Power Block Diagram

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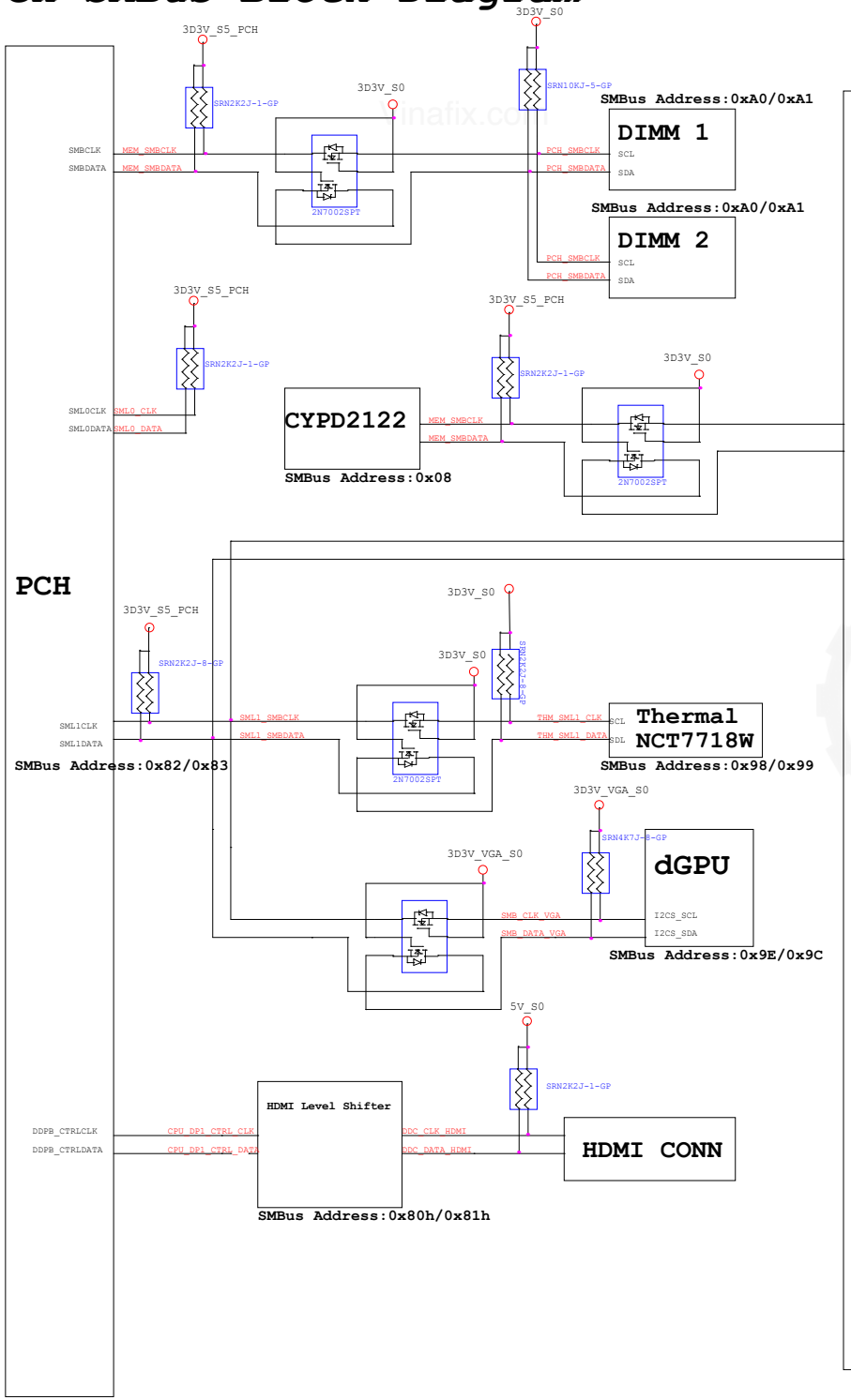
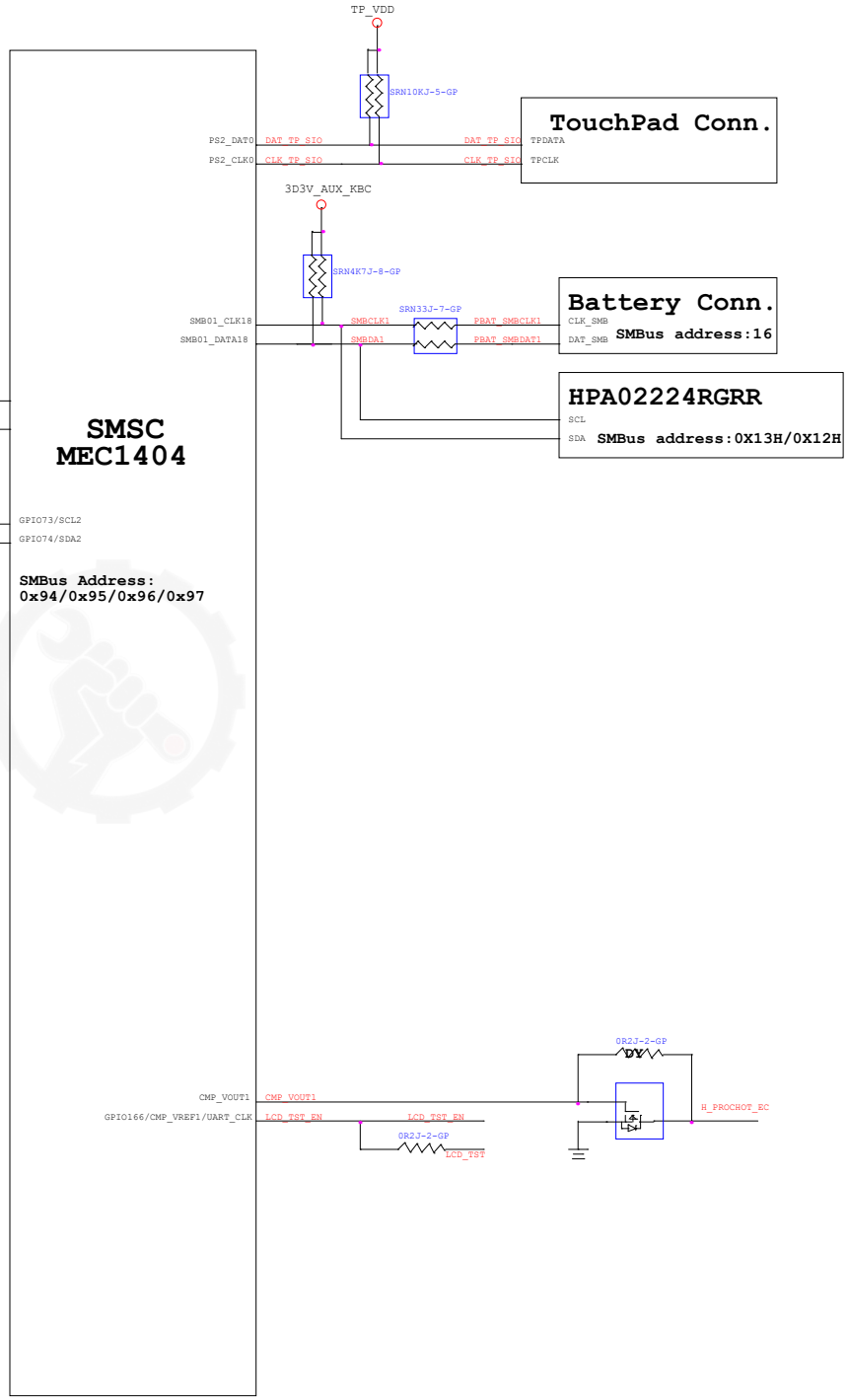
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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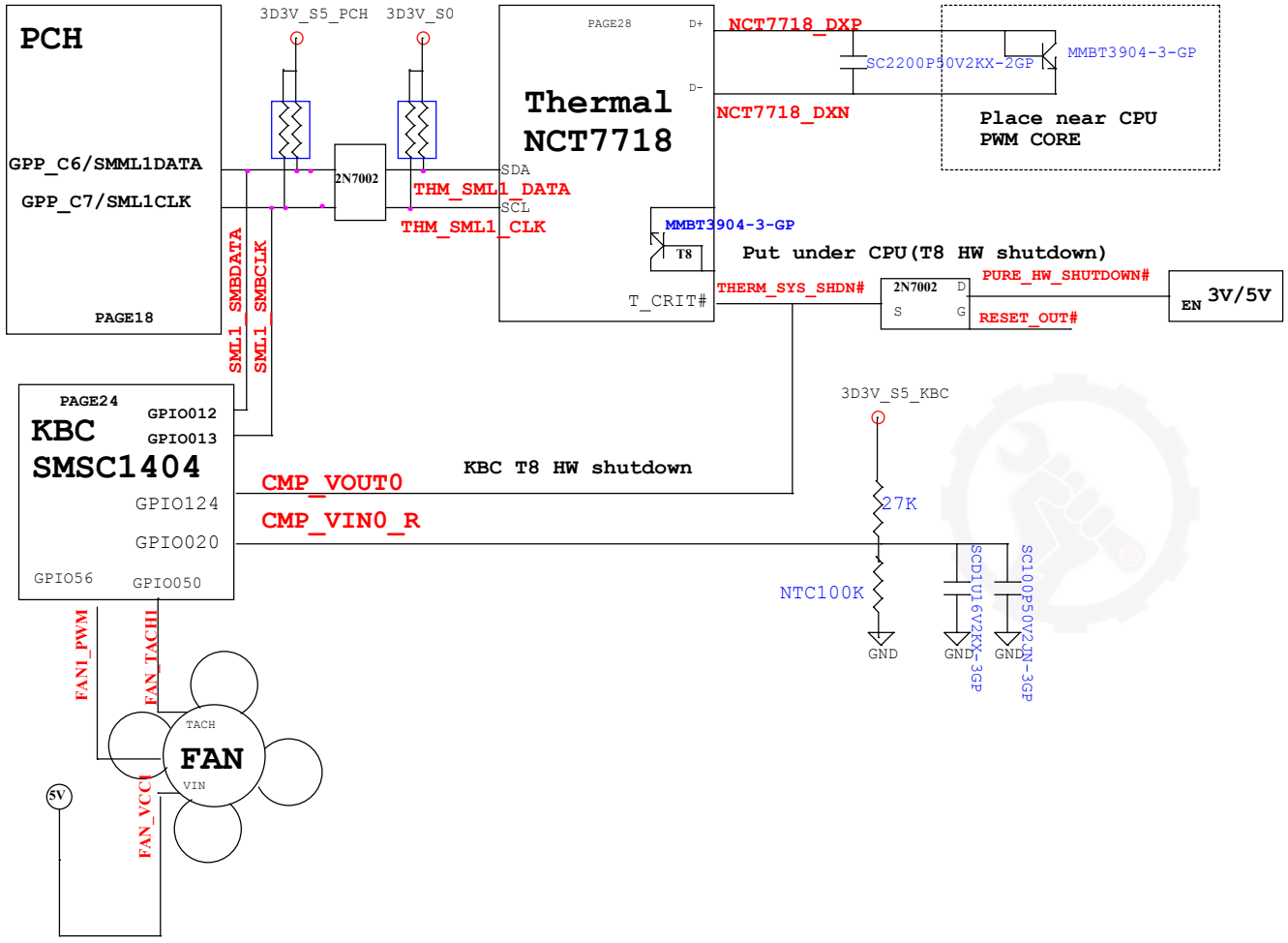
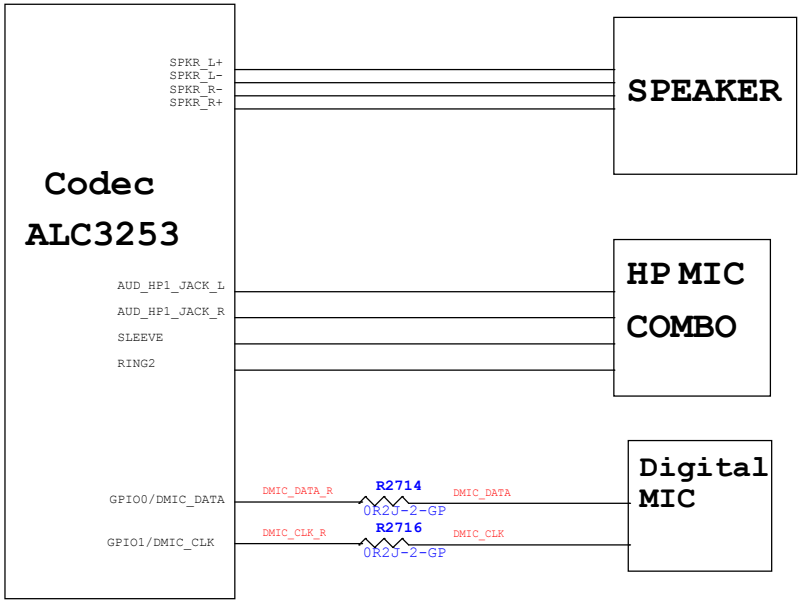
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Title

SIP connector

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