MS-7C82

uATX

Ver: 1.0

Intel -CML-S plamform

CPU:

Comet lake S 65W

PWM:

IMVP8 -RT3609BE

Onboard Chip:

HD Audio Codec:ALC1200
LAN- RTL8125B
SIO:NTC6687
Flash ROM: SPI 128 MB X1

Main Memory:

*DDRIV (2933MHz) * 4 (Dual Channel)*

ACPI:

LDO

Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 1*
*M.2 Slot * 2*

System Chipset:

B460 PCH_V

Display Output:

HDMI Port

DP Port

MSI MICRO-STAR INT'L CO.,LTD.

Title: Cover Sheet

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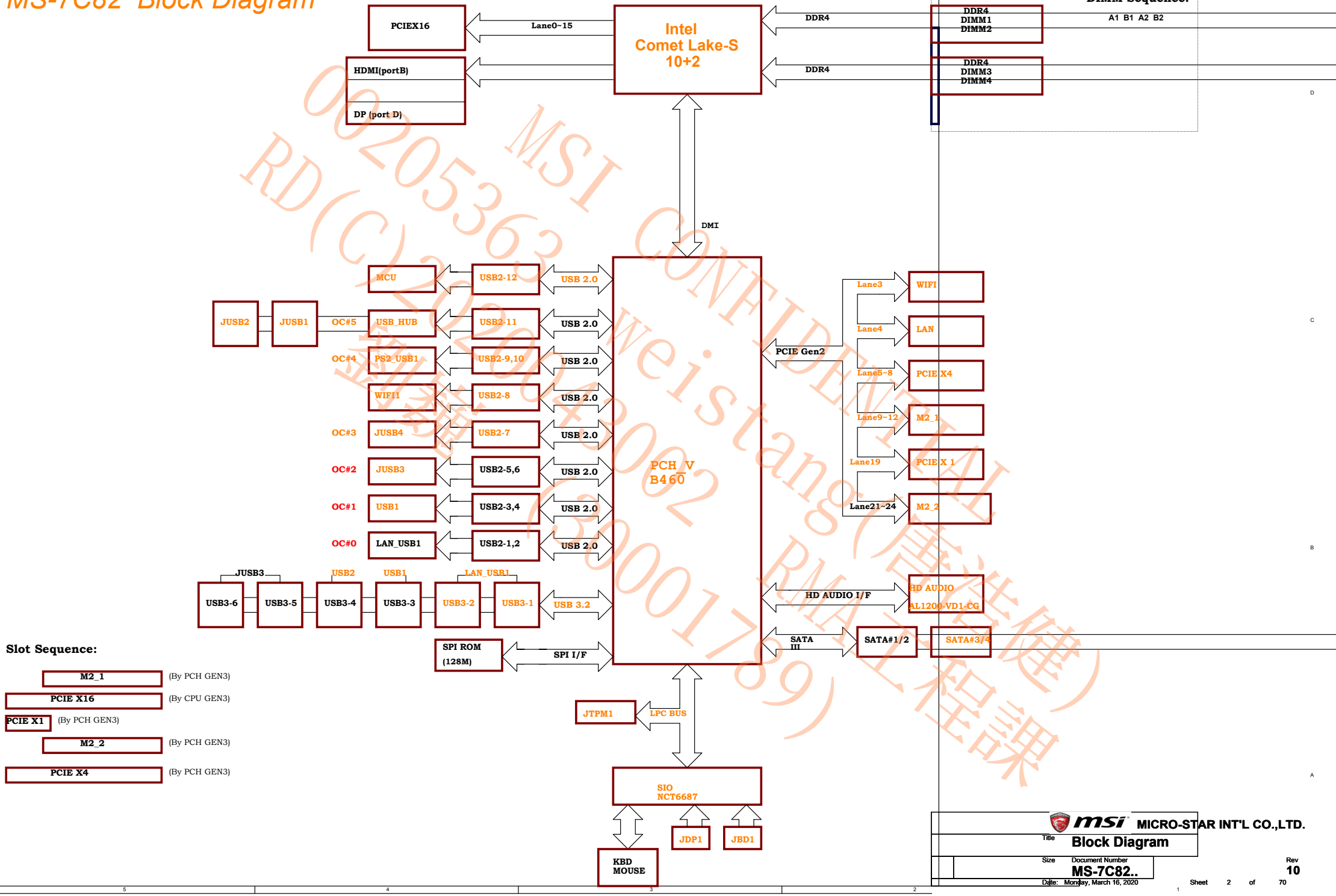
MS-7C82 Block Diagram



Slot Sequence:

- M2_1 (By PCH GEN3)
- PCIE X16 (By CPU GEN3)
- PCIE X1 (By PCH GEN3)
- M2_2 (By PCH GEN3)
- PCIE X4 (By PCH GEN3)

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Title: Block Diagram

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2019/11/1
R140 is changed from 10Kohm to 49.9ohm by PDG/CRB r1.0

2020/2/13
RN4 is changed from R31-0103012-W08 to R31-0103032-W08 by Robert's comment

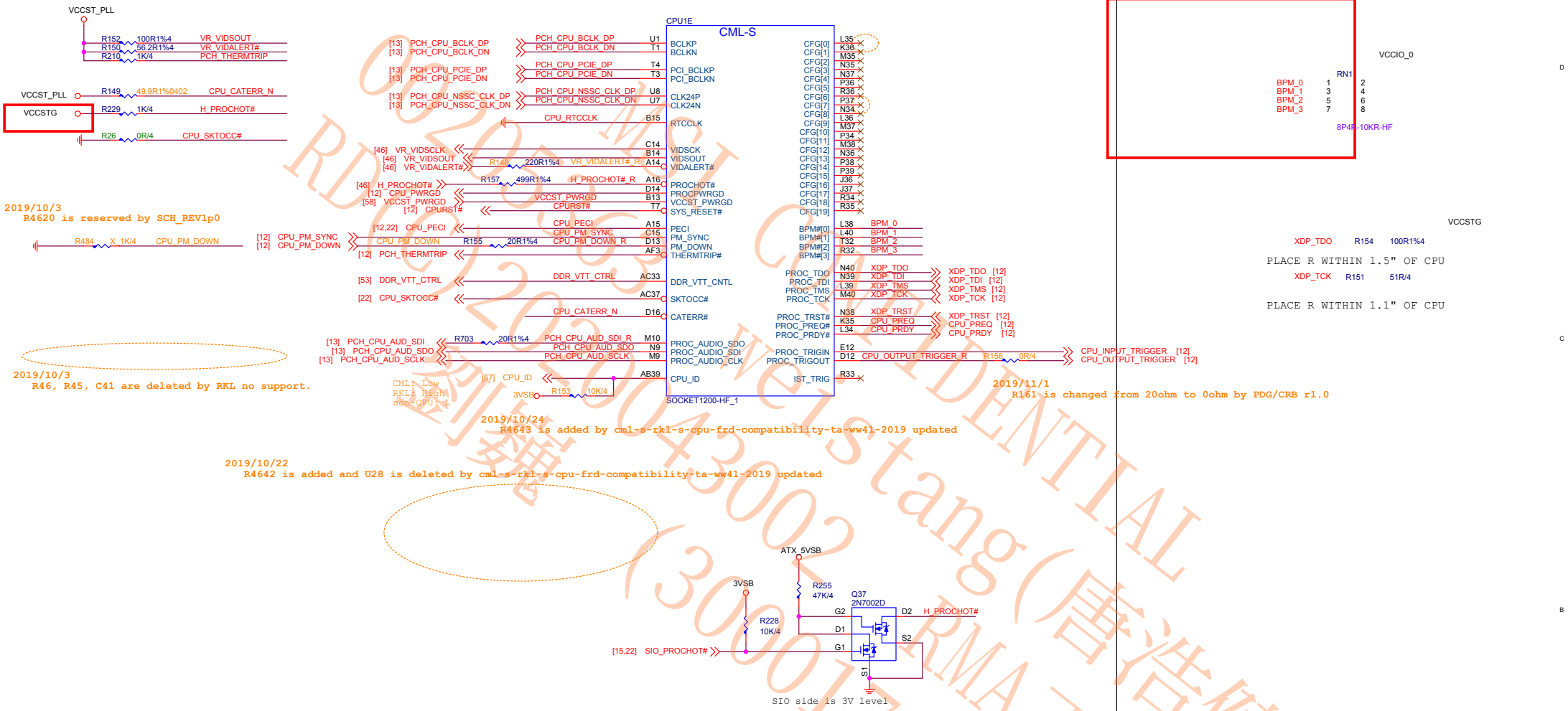
2019/10/3
R4620 is reserved by SCH_REV1p0

2019/10/3
R46, R45, C41 are deleted by RKL no support.

2019/10/24
R4643 is added by cml-s-rkl-s-cpu-frd-compatibility-ta-ww41-2019 updated

2019/10/22
R4642 is added and U28 is deleted by cml-s-rkl-s-cpu-frd-compatibility-ta-ww41-2019 updated

2019/11/1
R161 is changed from 20ohm to 0ohm by PDG/CRB r1.0



CFG Strap

CFG Table

	HIGH	LOW	DESCRIPTION
0	No stall	Stall	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5			PCIE Bifurcation
6			PCIE Bifurcation
7	Follow RESET#	Wait for BIOS	PEG TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

CFG5	CFG6			
ENABLE#		SLOT	SLOT	SLOT
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	RSVD	RSVD	RSVD
1	1	X16	X0	X0

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Title: CPU-Control/MISC/CFG
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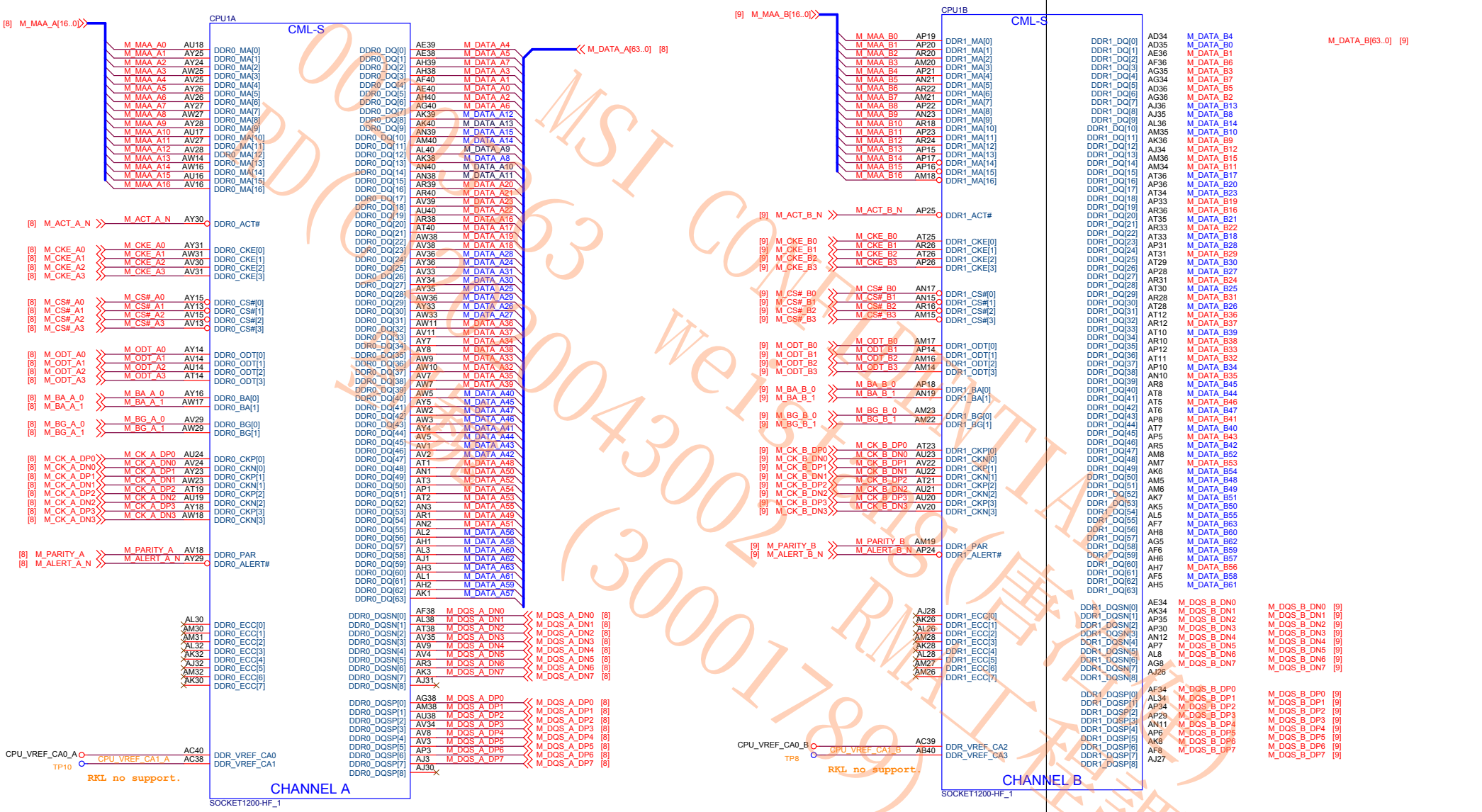

MICRO-STAR INT'L CO.,LTD.

Title: CPU-Memory

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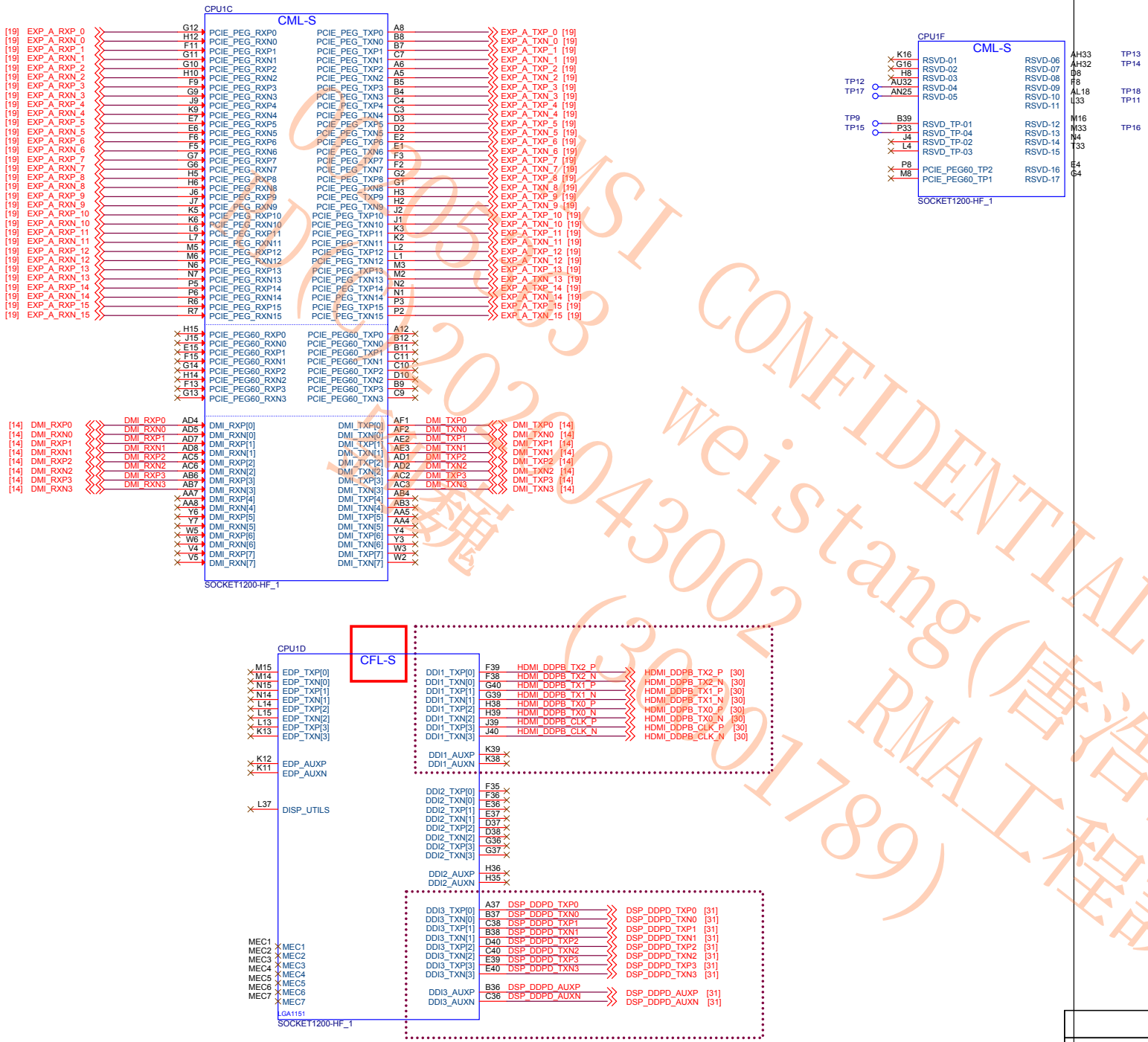

MICRO-STAR INT'L CO.,LTD.

Title: CPU-PEG/Display/RSD

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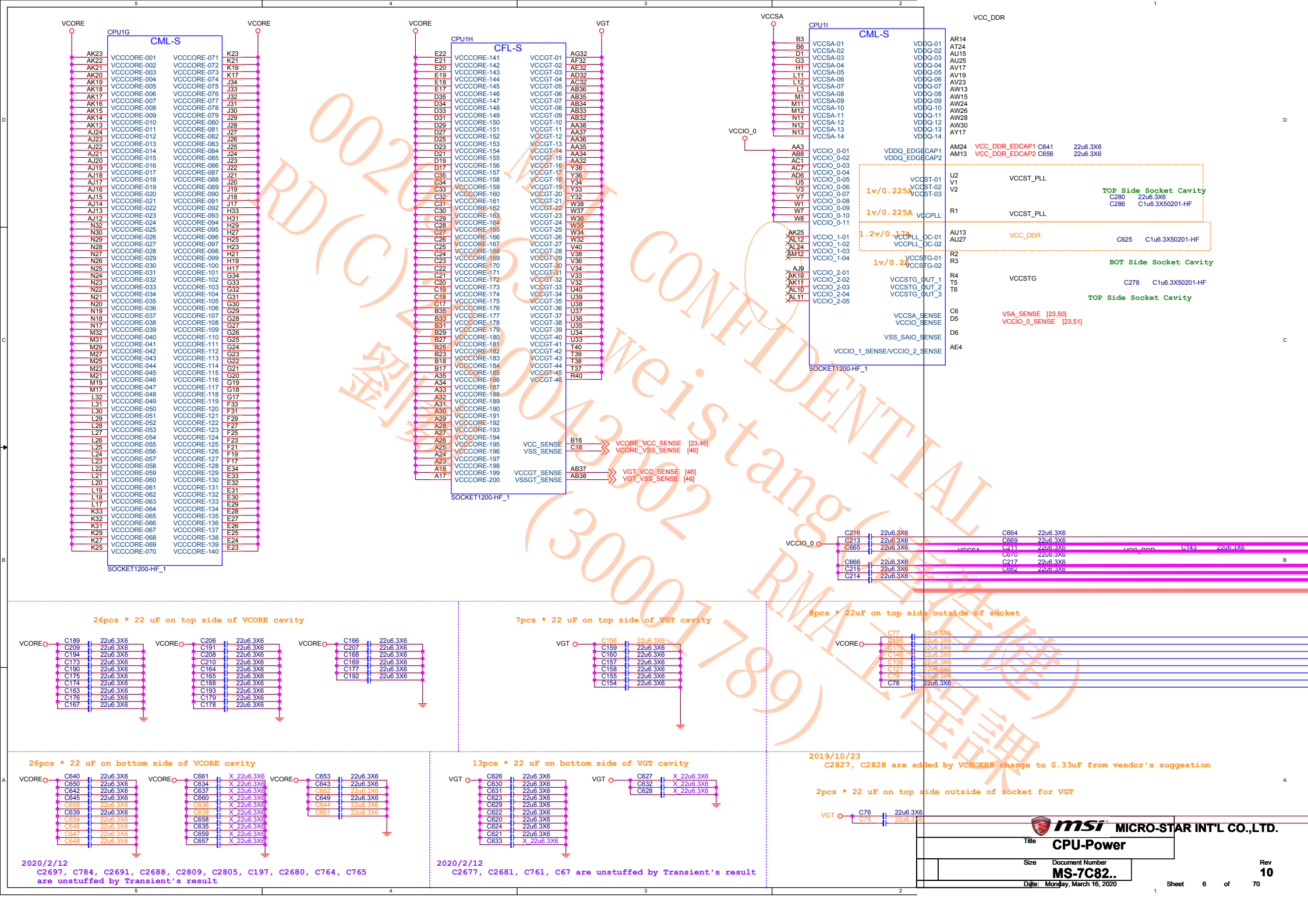
CPU1G
CML-S
SOCKET1200-HF_1
CPU1H
CFL-S
SOCKET1200-HF_1
CPU1I
CML-S
SOCKET1200-HF_1
VCORE_VCC_SENSE [23,46]
VCORE_VSS_SENSE [46]
VGT_VCC_SENSE [46]
VGT_VSS_SENSE [46]
VCC_DDR
VCCST_PLL
VCC_DDR
VCCSTG
VSA_SENSE [23,50]
VCCIO_0_SENSE [23,51]
TOP Side Socket Cavity
BOT Side Socket Cavity
TOP Side Socket Cavity
26pcs * 22 uF on top side of VCORE cavity
7pcs * 22 uF on top side of VGT cavity
8pcs * 22uF on top side outside of socket
26pcs * 22 uF on bottom side of VCORE cavity
13pcs * 22 uF on bottom side of VGT cavity
2019/10/23
C2827, C2828 are added by VCHOKE8 change to 0.33uF from vendor's suggestion
2pcs * 22 uF on top side outside of socket for VGT
2020/2/12
C2697, C784, C2691, C2688, C2809, C2805, C197, C2680, C764, C765
are unstuffed by Transient's result
2020/2/12
C2677, C2681, C761, C67 are unstuffed by Transient's result
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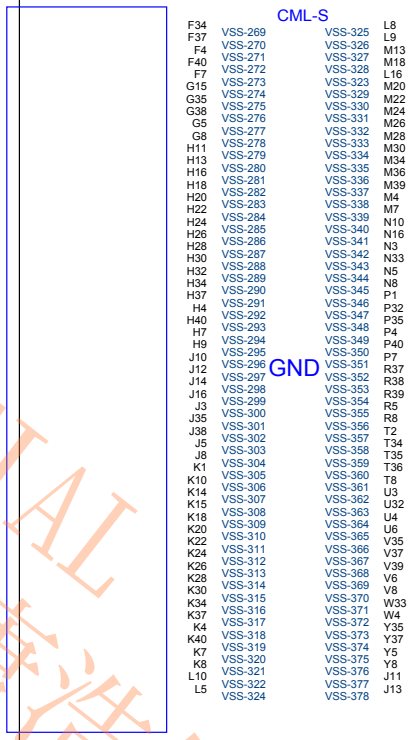

MICRO-STAR INT'L CO.,LTD.

Title: CPU-GND

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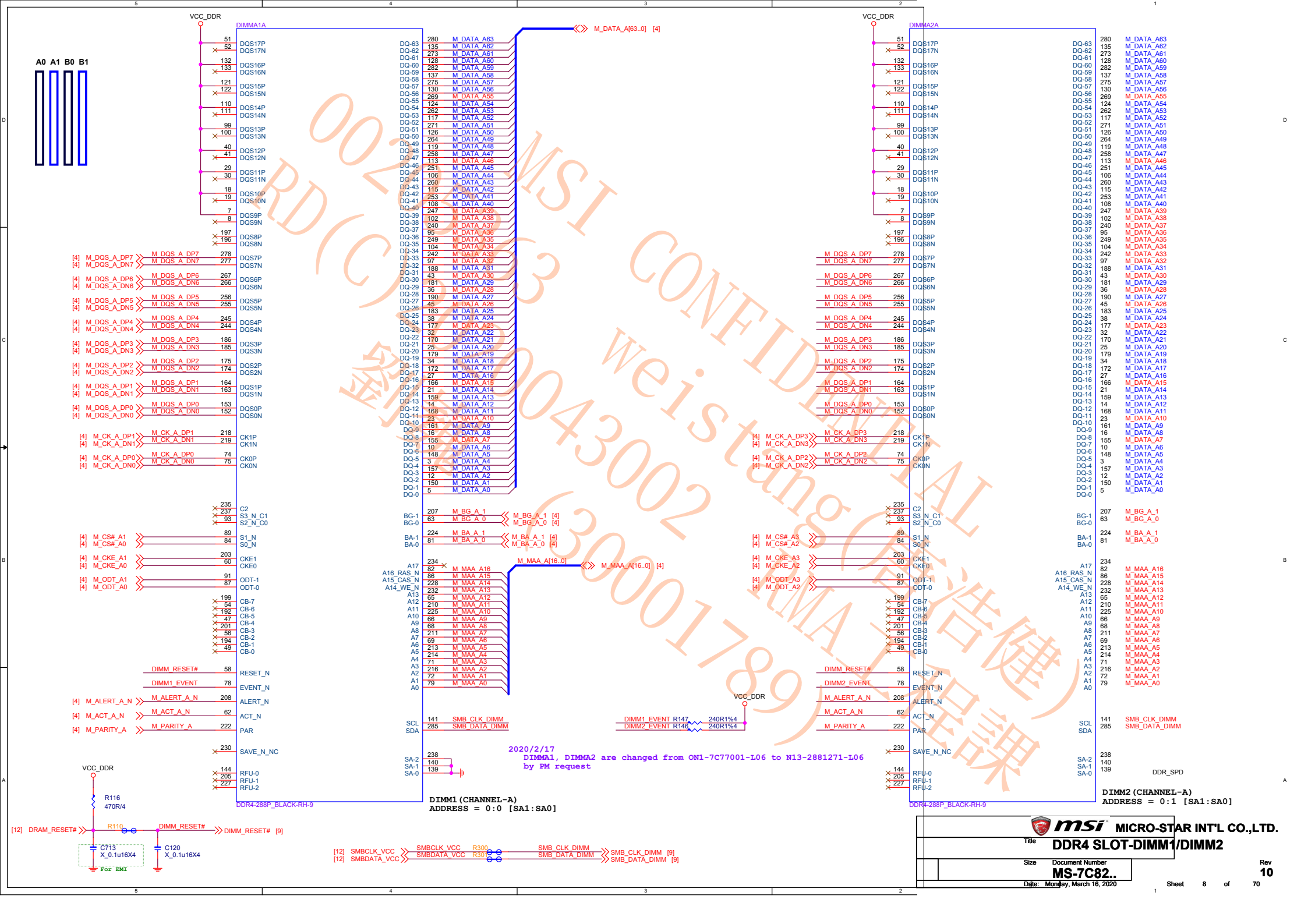

MICRO-STAR INT'L CO.,LTD.

Title: DDR4 SLOT-DIMM1/DIMM2

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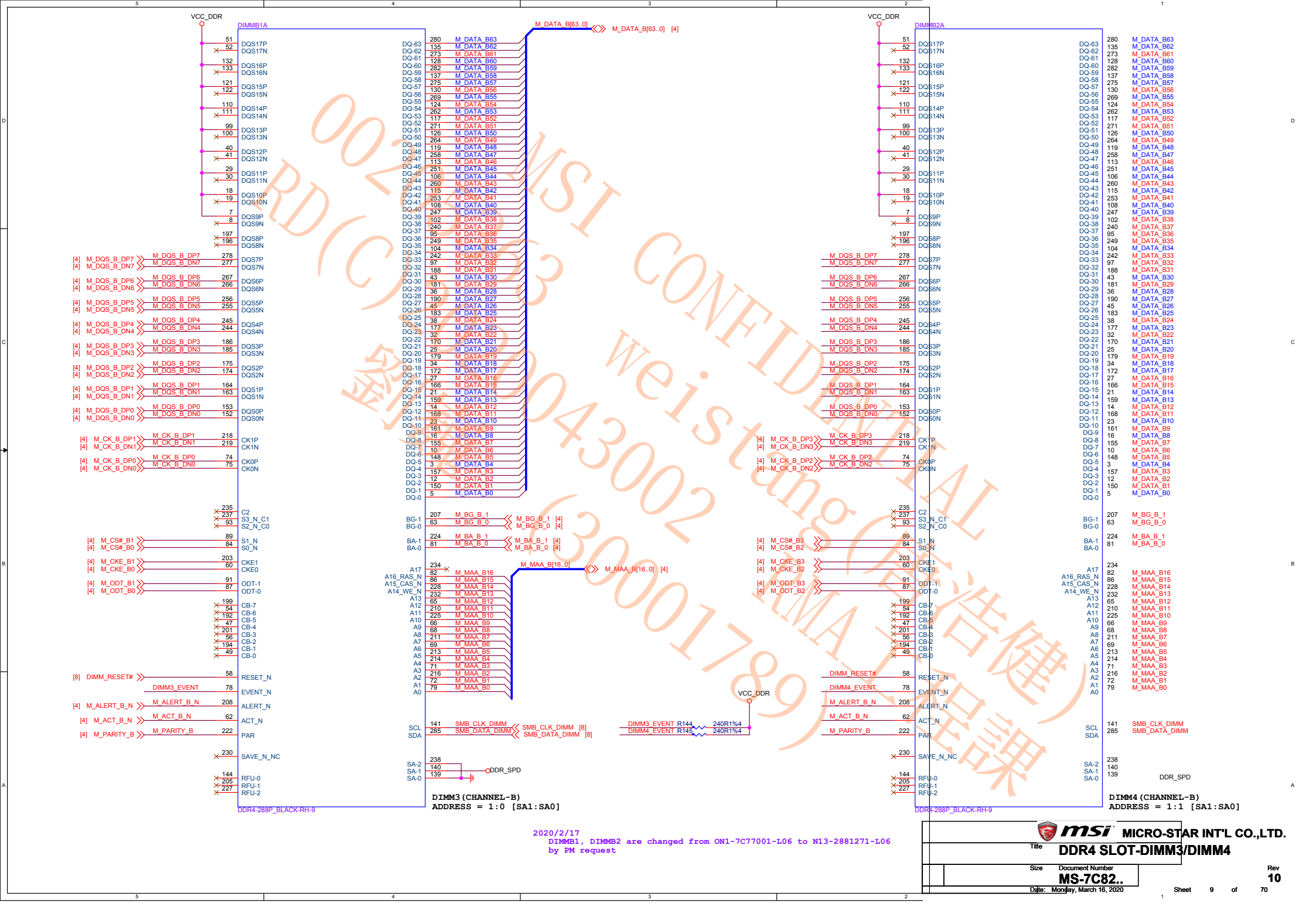

2020/2/17
DIMMB1, DIMMB2 are changed from ON1-7C77001-L06 to N13-2881271-L06 by PM request

MICRO-STAR INT'L CO.,LTD.

Title: DDR4 SLOT-DIMM3/DIMM4

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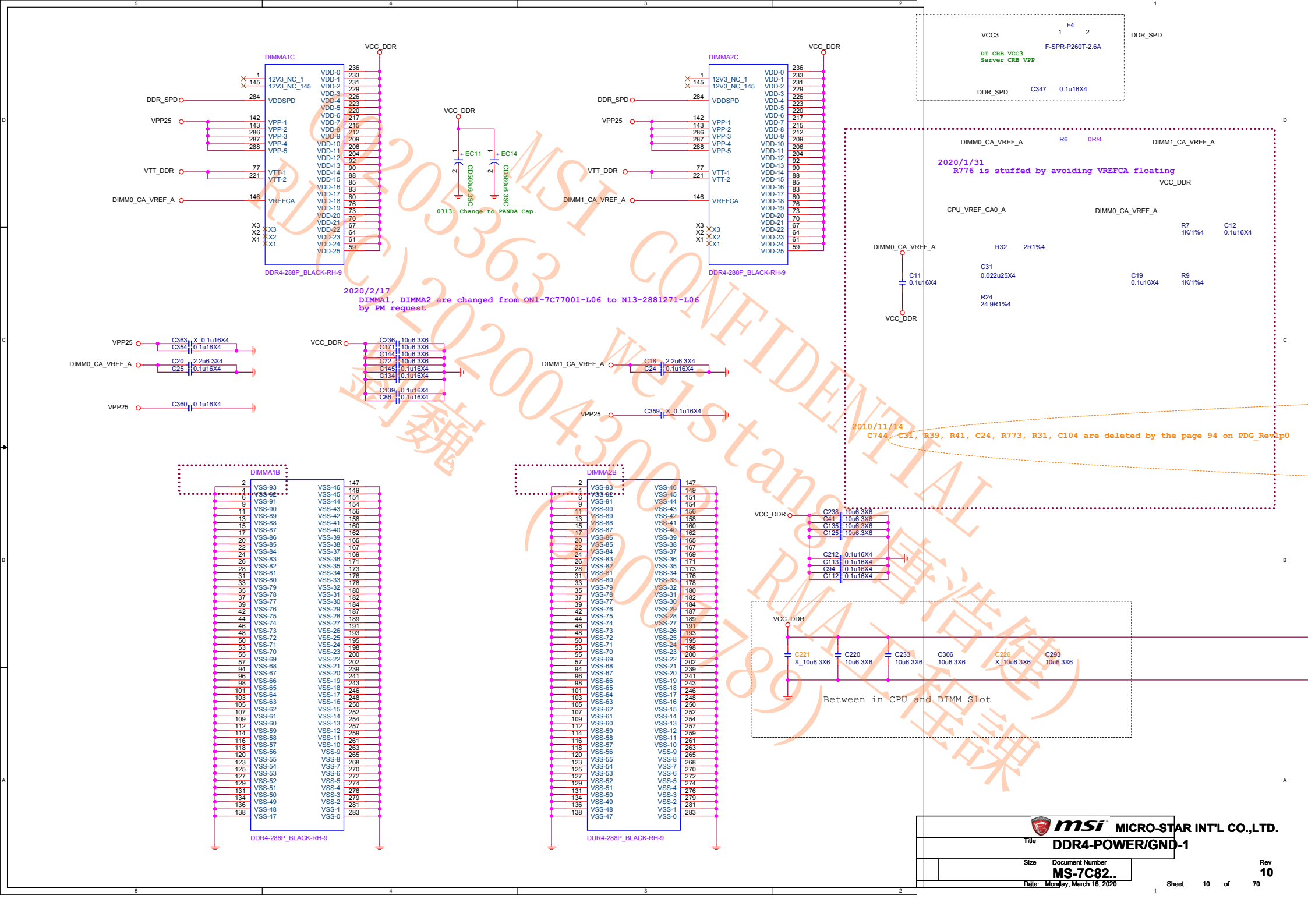

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Title	DDR4-POWER/GND-1	
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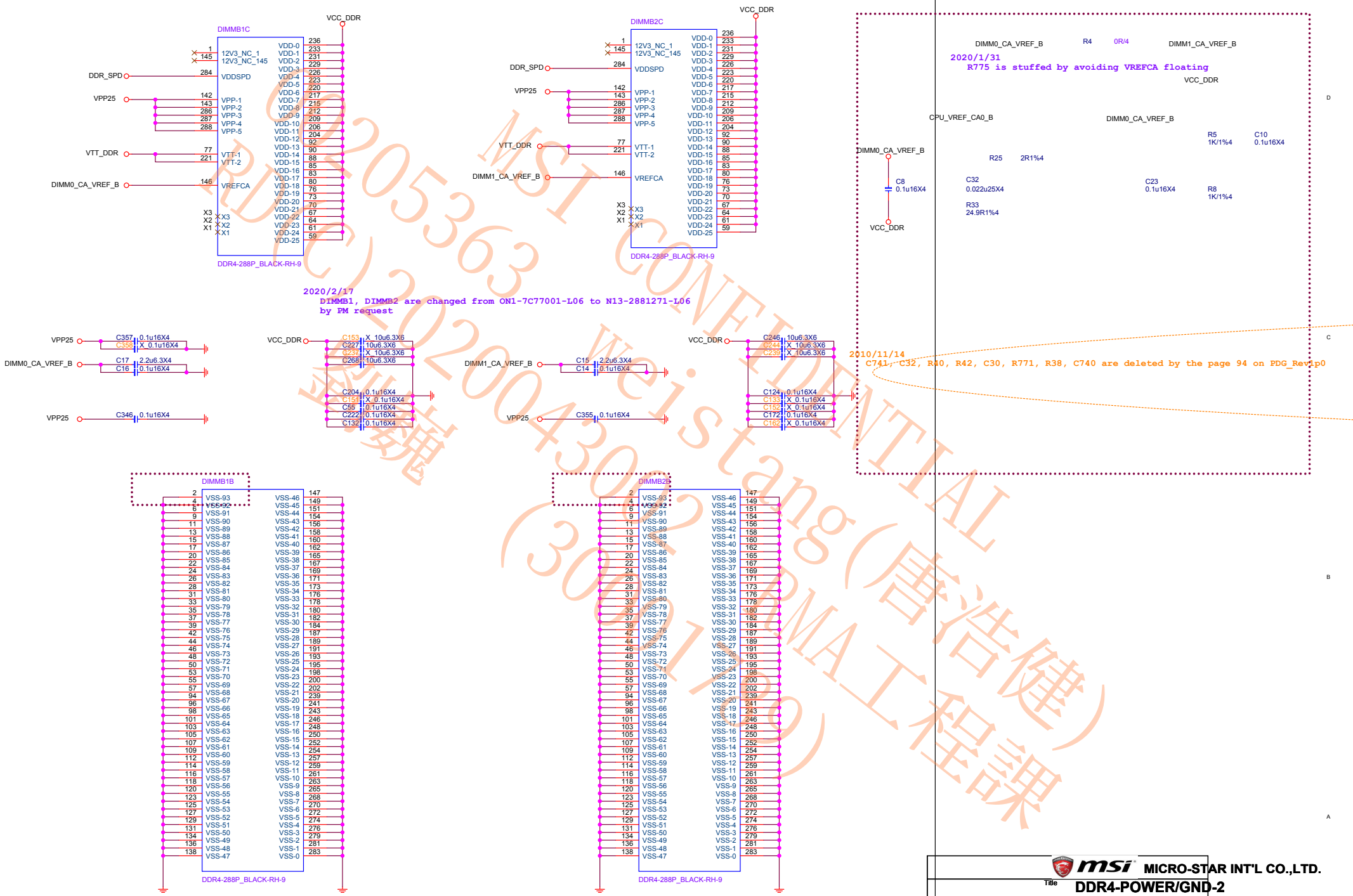

MICRO-STAR INT'L CO.,LTD.

Title: DDR4-POWER/GND-2

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2019/11/1
R830, R823, R824, R822 are changed from 15ohm to 33ohm by PDG/CRB r1.0

2019/11/27
R830, R823, R824, R822 are changed from 33ohm to 0ohm; R836 is unstuffed and then R844 is stuffed; by LPC seleted

2019/10/23
R583, R584 were stuffed by ESIO controled

2019/11/27
R583, R584 are unstuffed and
R591, R592 are stuffed by LPC mode

2020/2/20
R547 is unstuffed by KBRST# avoided floating when S5

2019/10/17
R579 is deleted by PDG_Rev0p7 & CRB Rev1p0

2019/10/17
C832, C833, C834, C828 were deleted because of lack of space

2020/1/31
R581 is stuffed by CRB Rev1p0

2020/1/31
R564 is changed from short-pad to 0ohm by CRB Rev1p0

2019/10/17
R474, R582, R494, R477, R498, R424, R500, R545, R4517, R502 are deleted by PDG_Rev0p7 & CRB Rev1p0

2020/3/4
R480 is stuffed by module circuit updated from Robert

2019/10/3
R636, R1754 were deleted because of lack of space

2019/10/3
R4619 is added by SCH_REV1p0

2019/10/23
R446, R445 are deleted by page 58 combined

2020/2/17
PCH1 is changed from OB1-7C86002-I06 to B01-B460005-I06 by PM request

2020/2/24
PCH1 is changed from B01-B460005-I06 to OB1-7C86002-I06 by PM request

2019/10/3
The value of R4508, R834 are the same as PDG_Rev0p7

Chassis Intrusion

RTC

PCH1A

LPC
SMB
Power Management
STRAP
SPI
JTAG

INTEL-FH82B460-RH

Title	MICRO-STAR INT'L CO.,LTD.		
	PCH-LPC/SPI/SMBUS/MISC		
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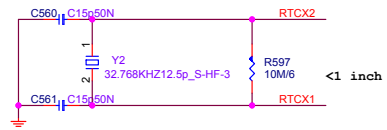
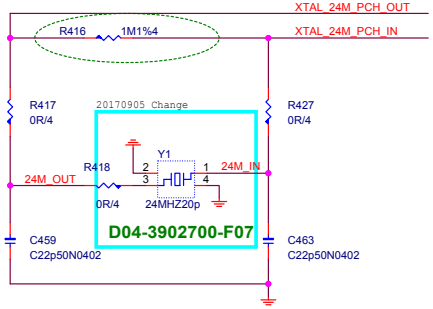
PCH_CLK

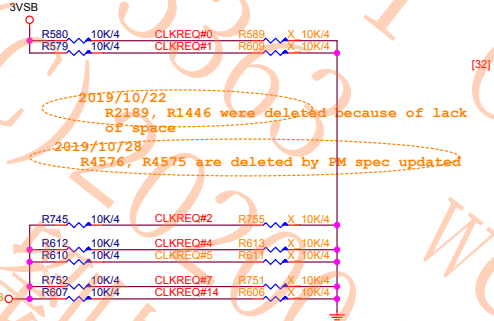
2019/10/2
R966 is changed from 22ohm to 33ohm by the page 41 from SCH_REV1p0

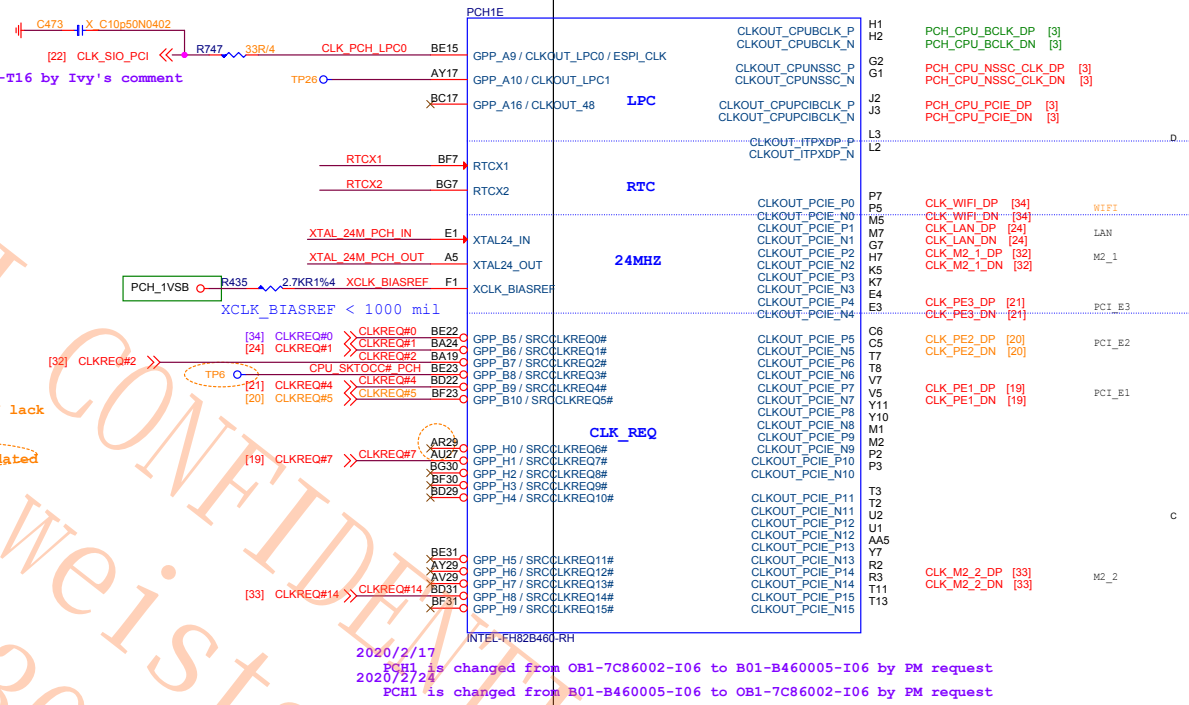
2019/10/7
Y3 is changed from D04-0305901-F07 to D04-0305500-SC6 by the lack of space

Close to PCH 2020/3/16
C560, C561 are changed from 12pF to 15pF and Y2 is changed from D04-0305500-SC6 to D04-0305500-T16 by Ivy's comment









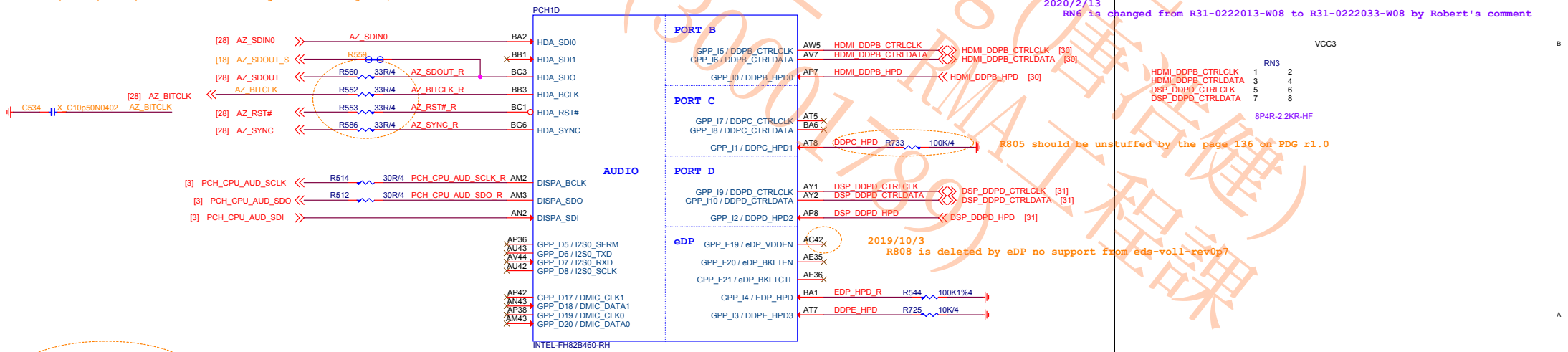
2020/2/17
PCH1 is changed from OB1-7C86002-I06 to B01-B460005-I06 by PM request
2020/2/24
PCH1 is changed from B01-B460005-I06 to OB1-7C86002-I06 by PM request

PCH_AUDIO

2020/2/17
PCH1 is changed from OB1-7C86002-I06 to B01-B460005-I06 by PM request
2020/2/24
PCH1 is changed from B01-B460005-I06 to OB1-7C86002-I06 by PM request

2019/11/15
R835, R512, R489, R513 should be changed to 47ohm by PDG/CRB r1.0

2020/2/13
RN6 is changed from R31-0222013-W08 to R31-0222033-W08 by Robert's comment



2019/10/17
R483, R482 are deleted by PDG_Rev0p7 & CRB Rev1p0R474

MICRO-STAR INT'L CO.,LTD.

Title: PCH-Clock/Audio

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USB3_9, USB3_10 were not function
except for PCIE3, PCIE4 by B460

SATA6, SATA7 were not function
except for PCIE19, PCIE20 by B460

PCH1B

DMI

PCIE

INTEL-FH82B460-RH

PCH1C

USB3

USB2

INTEL-FH82B460-RH

USB2_COMP <1000 mil

R1307, R769 are the same as CRB r0.7

2020/3/6
R1487 is changed from 1Kohm to 0ohm
by same as SCH_Rev_2p0

If USB On-The-Go is not supported
, USB2_ID pin should be grounded.

USB port13, 14 were not
function by B460 from Intel updated

2020/2/17
PCH1 is changed from OB1-7C86002-I06 to B01-B460005-I06 by PM request
2020/2/24
PCH1 is changed from B01-B460005-I06 to OB1-7C86002-I06 by PM request

R2653 is the same as CRB r0.7

PCIECOMP_P
PCIECOMP_N
Length Match < 5mil

請用GND包覆

2020/2/17
PCH1 is changed from OB1-7C86002-I06 to B01-B460005-I06 by PM request
2020/2/24
PCH1 is changed from B01-B460005-I06 to OB1-7C86002-I06 by PM request

R2649 is the same as CRB r0.7

2019/10/23
R1080, R2331, R2332, R2333, R2334, R4584 were deleted because of lack

2019/10/21
R2244, R2245, R2644, R2645, R2650, R2647, R2335, R2651, R2648, R2646 are deleted by 7C67-1.0's result

SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA

MICRO-STAR INT'L CO.,LTD.

Title: PCH-DMI/PCIE/USB/SATA

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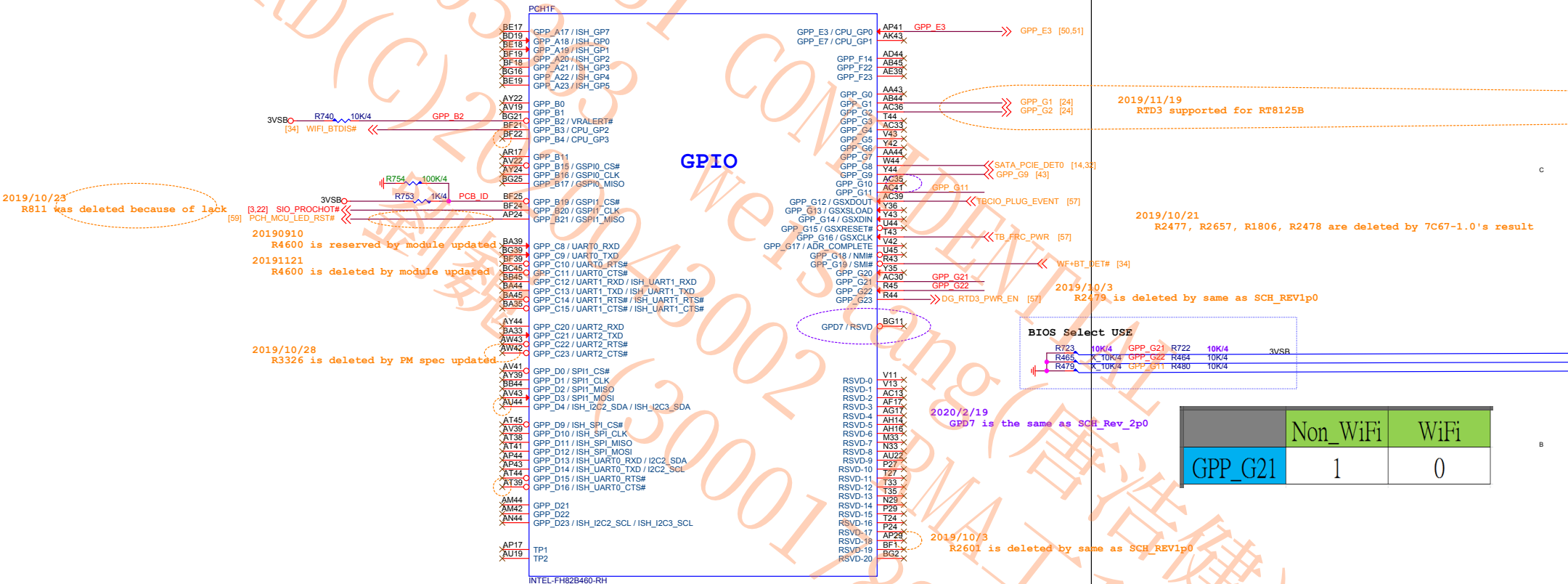
GPIO(SMI/NMI):
GPP_B14,GPP_B20,GPP_B23
GPP_C[23:22]
GPP_D[4:0]
GPP_E[8:0]
GPP_I[3:0]
GPP_G[7:0](Support SMI# only)

2020/2/17
PCH1 is changed from OB1-7C86002-I06 to B01-B460005-I06 by PM request
2020/2/24
PCH1 is changed from B01-B460005-I06 to OB1-7C86002-I06 by PM request



2019/10/23
R811 was deleted because of lack

20190910
R4600 is reserved by module updated

20191121
R4600 is deleted by module updated

2019/10/28
R3326 is deleted by PM spec updated

2019/11/19
RTD3 supported for RT8125B

2019/10/21
R2477, R2657, R1806, R2478 are deleted by 7C67-1.0's result

2019/10/3
R2479 is deleted by same as SCH_REV1p0

BIOS Select USE

2020/2/19
GPD7 is the same as SCH_Rev_2p0

2019/10/3
R2601 is deleted by same as SCH_REV1p0

	Non_WiFi	WiFi
GPP_G21	1	0

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Title: PCH-GPIO/RSVD
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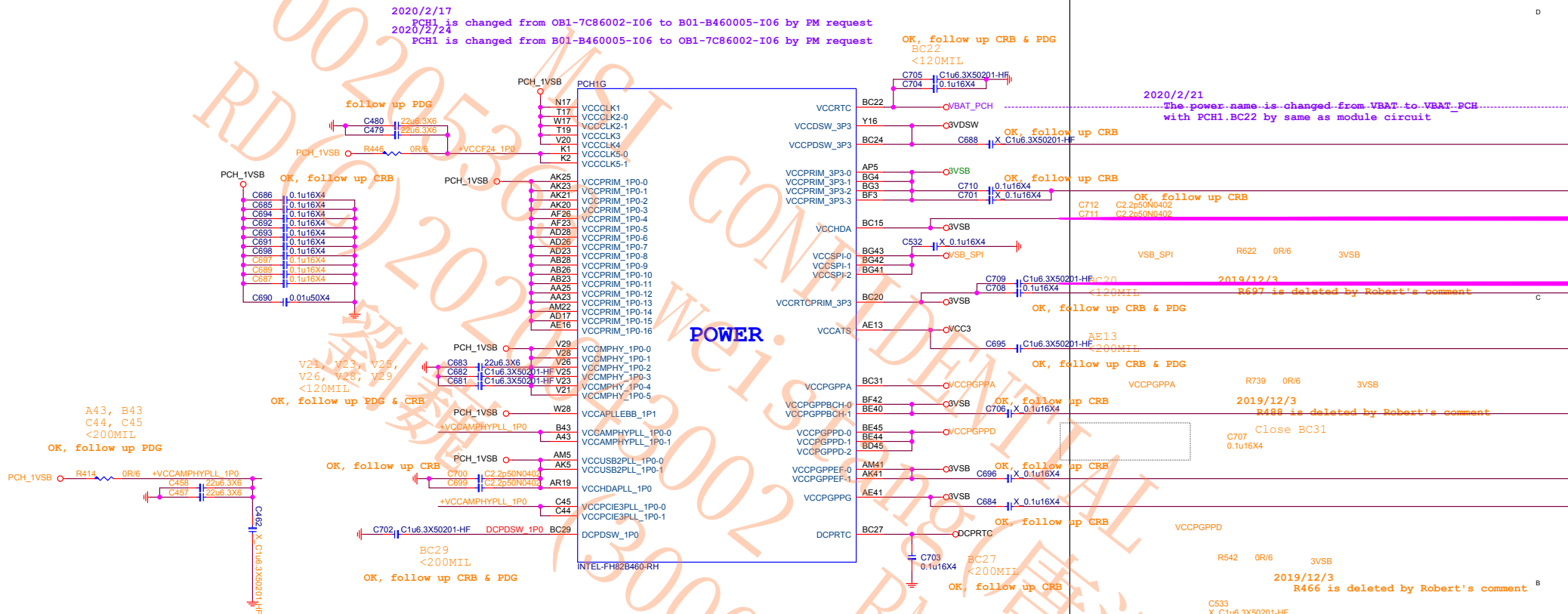

Title	PCH-Power
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MICRO-STAR INT'L CO.,LTD.

2020/2/17
PCH1 is changed from OB1-7C86002-I06 to B01-B460005-I06 by PM request
2020/2/24
PCH1 is changed from B01-B460005-I06 to OB1-7C86002-I06 by PM request

MICRO-STAR INT'L CO.,LTD.

Title: PCH-GND

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Top Swap Override

Here is the same as SCH_REV1p0

2019/10/23
R4513, R831 were deleted because of lack

0 : DISABLE (Default)
1 : ENABLE

Internal Pull-down is disabled after PCH_PWROK is high.

Reserved

Please see R734 on page 43
R734 is the same as SCH_REV1p0

No Reboot

Here is the same as SCH_REV1p0

2019/10/23
R503, R479 were deleted because of lack

0 : DISABLE (Default)
1 : ENABLE

Internal Pull-down is disabled after PCH_PWROK is high.

Reserved

Here is the same as SCH_REV1p0
R563 should be unstuffed by SCH_REV1p0

2019/10/23
R4514 was deleted because of lack

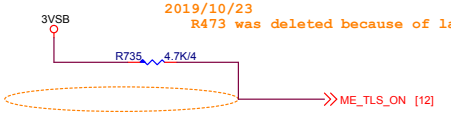
0 : DISABLE Intel DCI-OOB(Default)
1 : ENABLE intel DCI-OOB

Internal Pull-down is disabled after RSMRST# de-assert.

TLS Confidentiality

Here is the same as SCH_REV1p0

2019/10/23
R473 was deleted because of lack

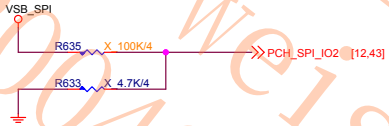


0 : DISABLE
1 : ENABLE (Default)

Internal Pull-down is disabled after RSMRST# de-assert.

Reserved

2019/10/3
INTERNAL 20K PU
R587 is unstuffed by eds-vol1-rev1p1 & SCH_REV1p0



Boot BIOS Strap Bit BBS

Here is the same as SCH_REV1p0

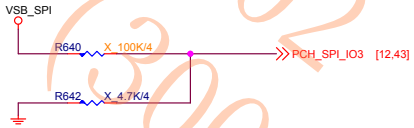
2019/10/23
R828, R815 were deleted because of lack

0 : SPI (Default)
1 : LPC

Internal Pull-down is disabled after PCH_PWROK is high.

Reserved

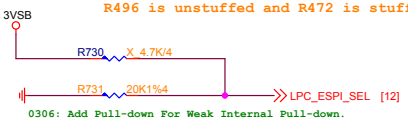
2019/10/3
INTERNAL 20K PU
R586 is unstuffed by eds-vol1-rev1p1 & SCH_REV1p0



eSPI or LPC

Here is the same as SCH_REV1p0
R472 should be unstuffed by SCH_REV1p0 + ug-rev1p2

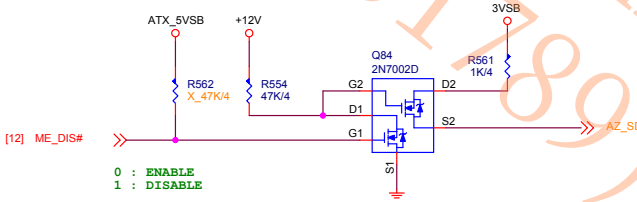
2019/11/27
R496 is unstuffed and R472 is stuffed by LPC seleted



0 : LPC (Default)
1 : eSPI

Internal Pull-down is disabled after RSMRST# de-assert.

Flash Descriptor Security Override



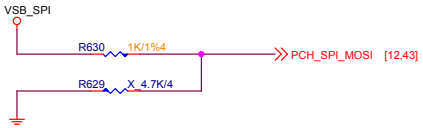
0 : ENABLE
1 : DISABLE

0 : Enable security measures defined in the Flash Descriptor. (Default)
1 : DISABLE:Flash Descritior Decurity(Override).

Internal Pull-down is disabled after PCH_PWROK is high.

Reserved

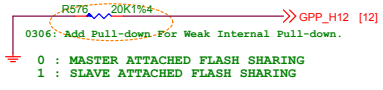
Here is the same as SCH_REV1p0



Reserved

R373 should be unstuffed by SCH_REV1p0

2019/10/23
R357 was deleted because of lack



0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal Pull-down is disabled after RSMRST# de-assert.

MSI MICRO-STAR INT'L CO.,LTD.

Title: PCH-Strap

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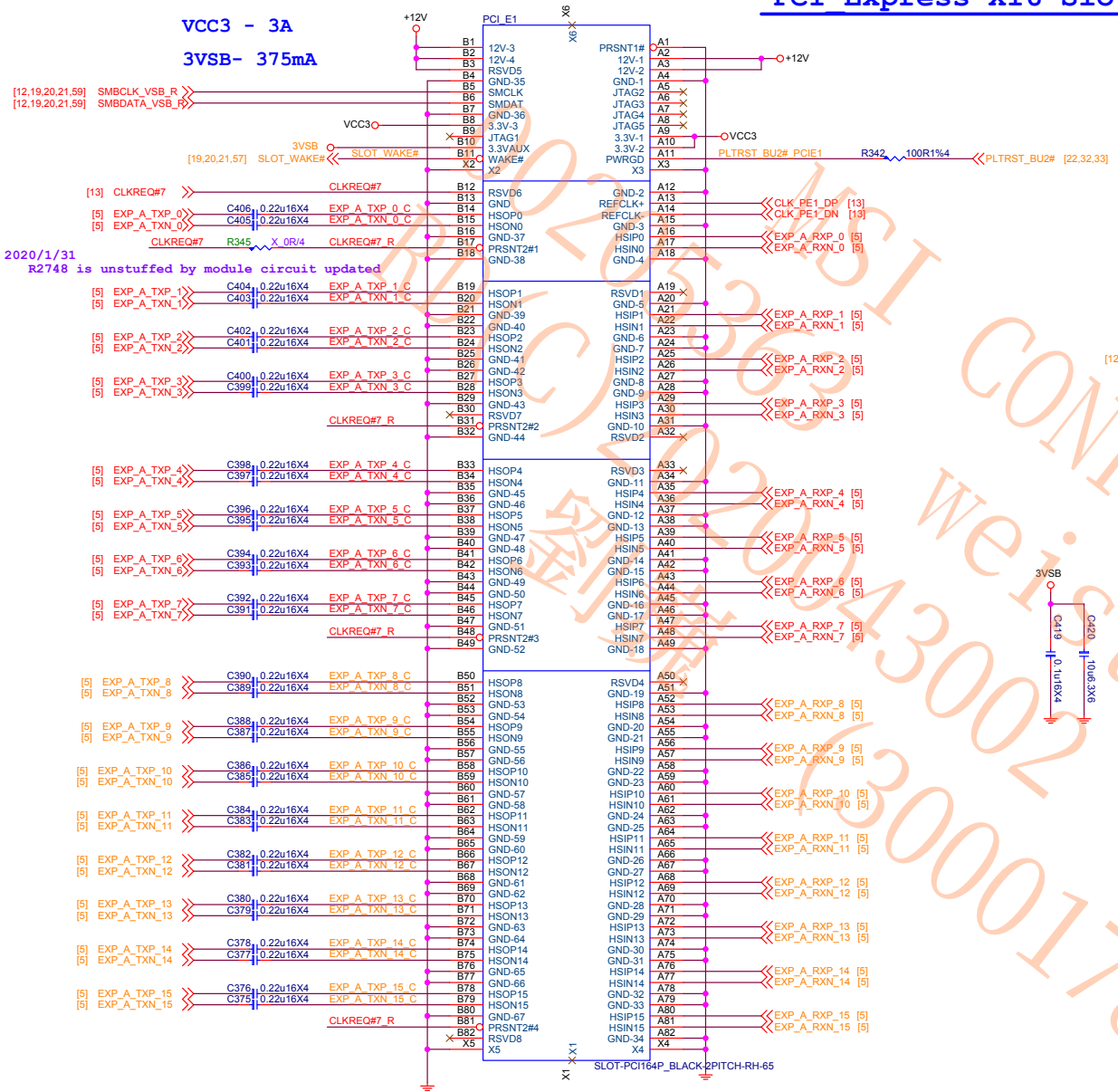
Date: Monday, March 16, 2020 Sheet 18 of 70

PCI Express X16 Slot

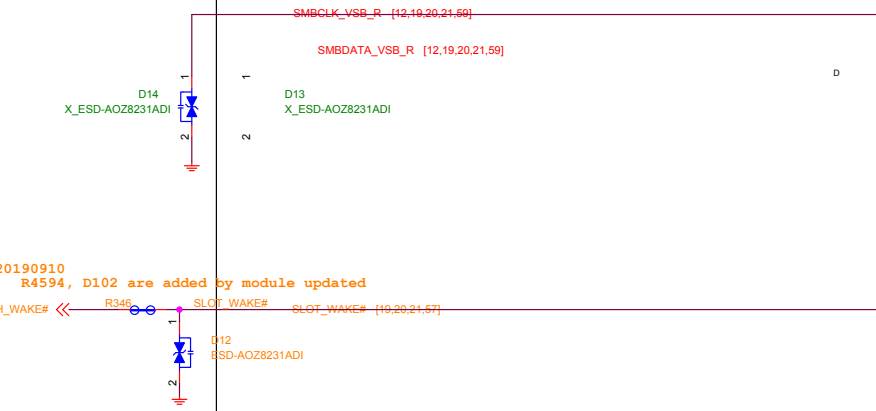
12V - 5.5A

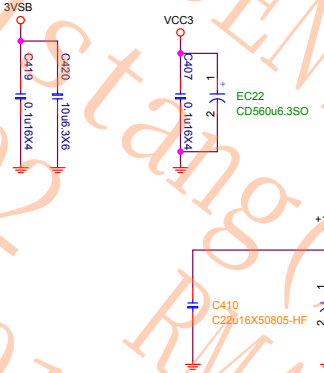
VCC3 - 3A

3VSB- 375mA

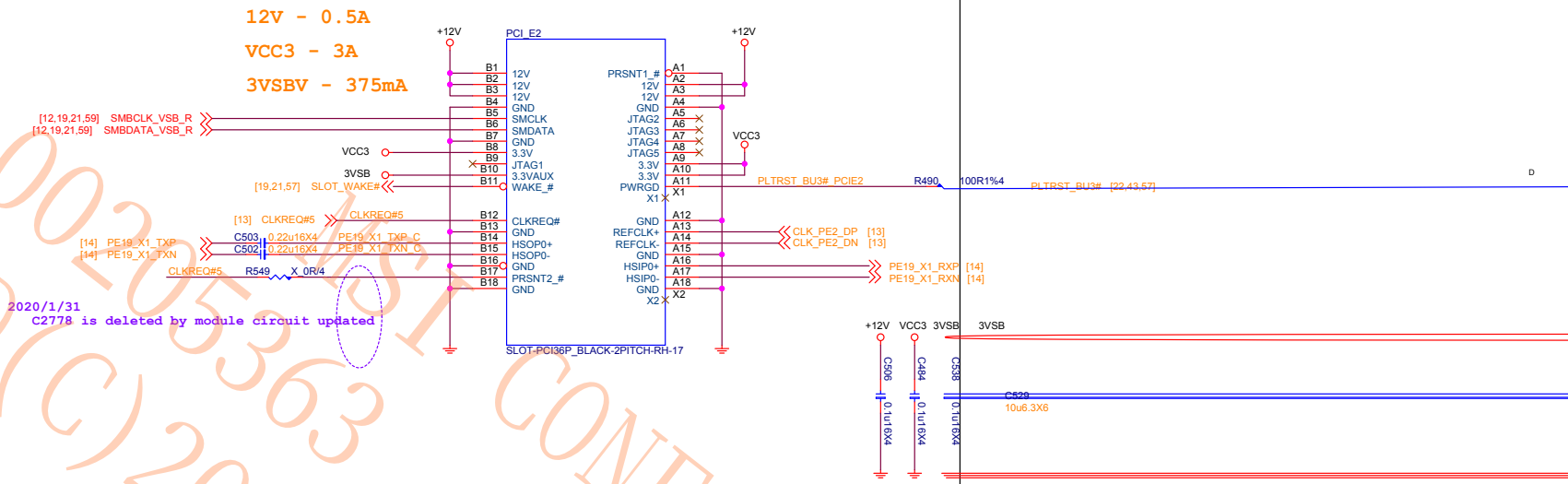


SMBus ESD





MICRO-STAR INT'L CO.,LTD.		
Title: PCIE SLOT X16		
Size	Document Number: MS-7C82..	Rev: 10
Date: Monday, March 16, 2020	Sheet 19 of 70	



MICRO-STAR INT'L CO.,LTD.		
Title: PCIE SLOT-PCH(X1)		
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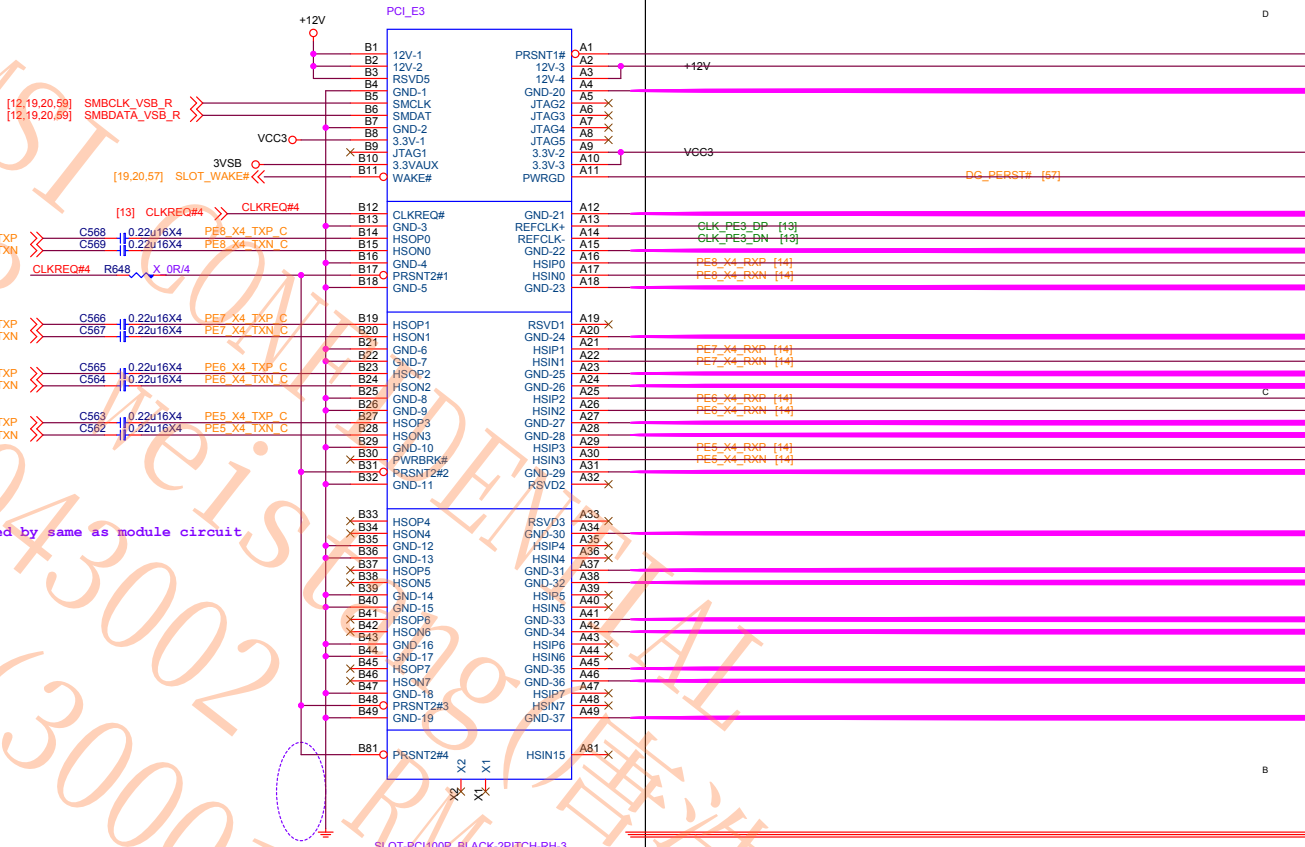
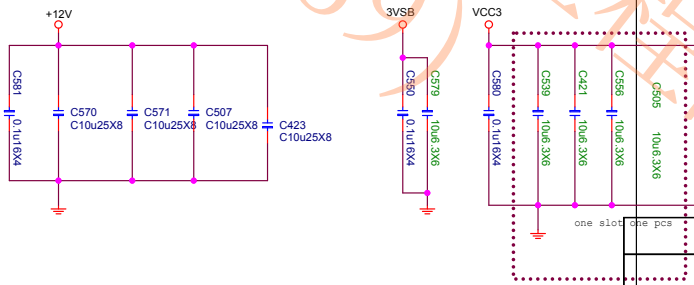
PCI Express X4 Slot

2.1A at +12V
3A at VCC3
375mA at 3VSB

2020/2/17
PCI_E3 is changed from N11-1000321-L06 to N11-1000151-L06 by PM request

2020/1/31
R597 is unstuffed and C2777 is deleted by same as module circuit





MICRO-STAR INT'L CO.,LTD.

Title: PCIE SLOT (X4)

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POWER ON STRAPPING PIN FOR NCT6687

PIN	NAME	Circuit NAME	0	1	Strap Point
27	ESPI_EN	KBRST#	LPC(VCC3)	ESPI(3VA)	VCC3 3VA
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789_EN disable	FAN789_EN enable	3VA

2020/3/16
R442 is changed from short-pad to 0ohm(unstffed) by same as CRB 2.0

2020/1/31
R327 is unstuffed by module circuit

2020/2/21
R2729 is changed to pull-up to VBAT_PCH from VBAT by same as module circuit

2019/10/8
R382 is unstuffed and R385 is stuffed by module updated

2020/2/19
R520 is changed from 7.68Kohm to 2.55Kohm and R522 is changed from 3.3Kohm to 1.1Kohm by module circuit updated from Robert's comment

2020/3/16
U29 is changed from OB2-7B51001-N62 to B02-6687D04-N62 by PM request

2020/2/25
GPIO32 is changed to GPIO31 and R4676 is reserved by module circuit updated from Robert's comment

2019/12/9
R530 is unstuffed and R2717 is stuffed by pin 7, 8, 13 unused

2019/12/9
R533 is unstuffed and R552 is stuffed by LPC mode default used ESIO

2019/11/6
R343, R342 are stuffed and R360, R359 are unstuffed by Robert's comment

2019/12/3
R550 is deleted by Robert's comment

2019/11/27
R549 is stuffed and R550 is unstuffed by LPC seleted

2020/1/31
R4671 is added by module circuit updated

20190910
Q392 is reserved by module updated

20191008
Q392 is stuffed by module updated

2019/12/6
U1014 is changed from 512k to 256k by module circuit same as 7C71

20191015
C2825, R4635 are addd and C2826 is reserved by module updated

Closed PIN119
Closed PIN110
Closed PIN99
Closed PIN46,85
Closed PIN1

3V Analog Power

DEBUG PORT for BIOS

Use JBD1 for BIOS Debug if no COM port or JTPM.

DEBUG PORT

SPI ROM

Title	SIO-NCT6687-1
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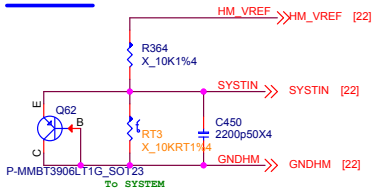
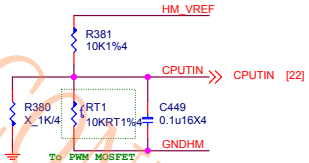
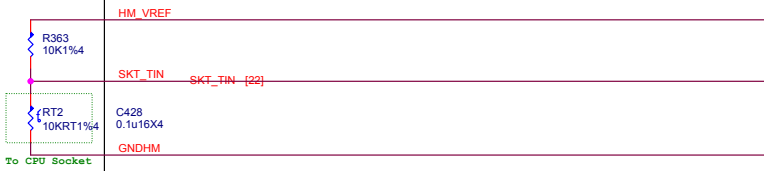
MICRO-STAR INT'L CO.,LTD.

Thermal

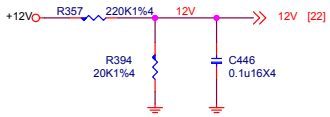


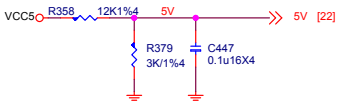




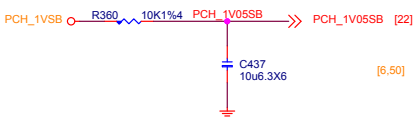
HW Monitor - Voltage

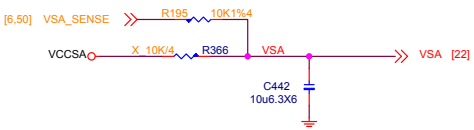
SIO HM Voltage Over 2V will Not Detect

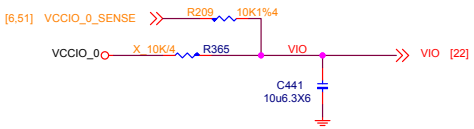




2019/10/22
R4636, R4638, R4640 are added and R4637, R4639, R4641 are reserved by robert's comment







MICRO-STAR INT'L CO.,LTD.

Title: SIO-NCT6687-2

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RTL8125B 10/100/1000/2.5G LAN Controller

2019/11/19
U1025, C2843, R4648, R4649, R4647 are added by RTD3 supported for RT8125B

For RTD3 Control ISOLATEB
ISOLATEB pull up Main Power,not aux power
check GPIO
if GPIO have power in S5/S4/S3 ->stuff RL32&RL34&QL457,RL33 NC

2020/2/26
RL24, RL8, RL11, RL15, RL14 are deleted; RL33, RL38, DL2 are added; RL32, RL34, Q457, RL37 are reserved;
RL13 is unstuffed by module circuit updated from Nick

Place RL6 Close to IC

2020/3/12
RL38 is unstffed and then RL37 is stuffed by circuit correctness

pull up voltage need same with PCH_WAKE#

if RL13 stuff->DL2&RL37&RL38 NC

2020/3/2
L2 is chnaged from L02-3308082-M26 to L02-3308102-T19
by module circuit updated from Nick

2020/2/26
CL27 is changed from 10uF to 22uF; CL43, CL10, CL39 are stuffed; CL7, CL44 are deleted; CL34 is changed type(2.2uF to 10uF) by module circuit updated from Nick

Pin49: 16 via from top layer to GND layer
and make the via at the center of IC.

2020/2/21
R4648 is changed to pull-up to 3VSB from VCC3; RL39 is reserved by module circuit
updated from Nick

ESD Protect
UL1&UL2 close to connector

UL4 ESD-UT148ZAD5A-HF

UL3 ESD-UT148ZAD5A-HF

Main:D0G-28B030C-U33
AVL:D0G-28B180C-I05

2019/10/21
CL1, CL2, CL4 are changed from 100pF to 22pF by vendor's suggestion

LED2_LINK#_R	CL2	C22p50N0402
LED1_2500#_R	CL3	C22p50N0402
LED0_1000#_R	CL4	C22p50N0402

Check with EMI

LAN Connector

RJ45_USBX2_LEDX2_TX-RH-111
N58-32F0891-F02

CHOKEL1 PN:
Main:L04-47B70N0-M09
AVL:L04-47B7930-M26

Layout needs to check with module circuit

2020/2/26
RL16 is chnaged from 33Kohm to 22.6Kohm; RL25 is changed from 174Kohm to 120Kohm;
CL26 is chnaged from 6800pF to 4700pF; CL20 is chnaged from 10uF to 22uF; CL33 is
changed from 2.2uF(unstuffed) to 22uF by module circuit updated from Nick

2020/2/26
CL5 is stuffed and D10 is unstuffed by module
circuit updated from Nick

0.95V / 0.65A

Title	LAN RTL8125B		
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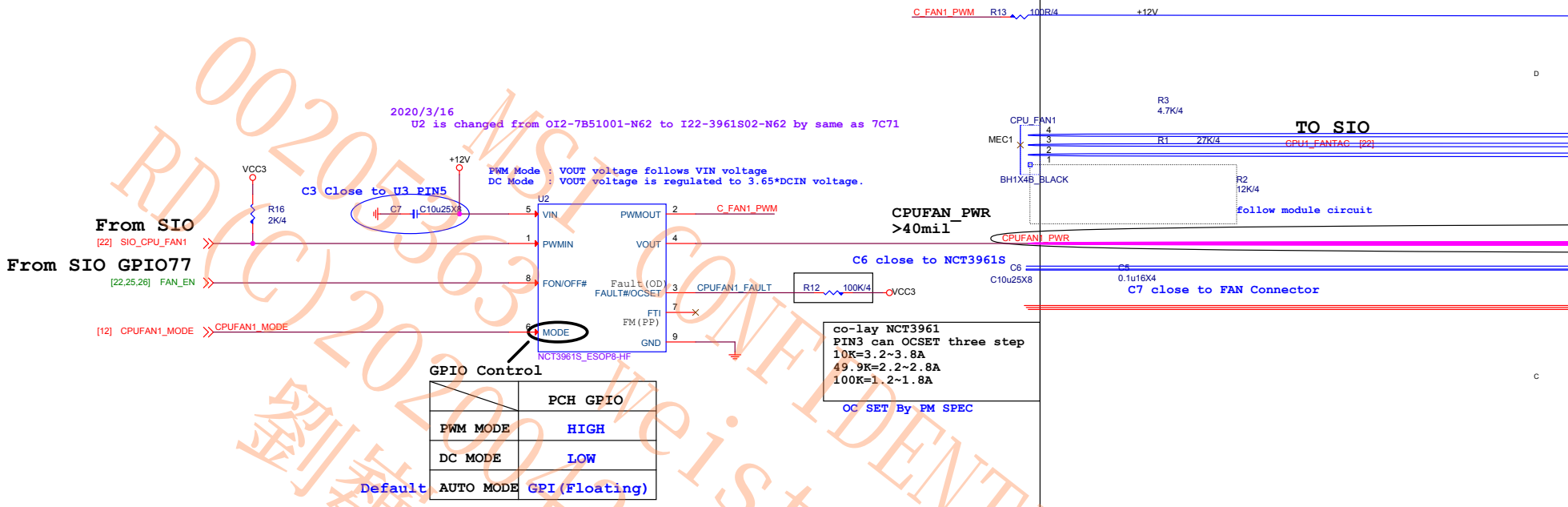
MICRO-STAR INT'L CO.,LTD.

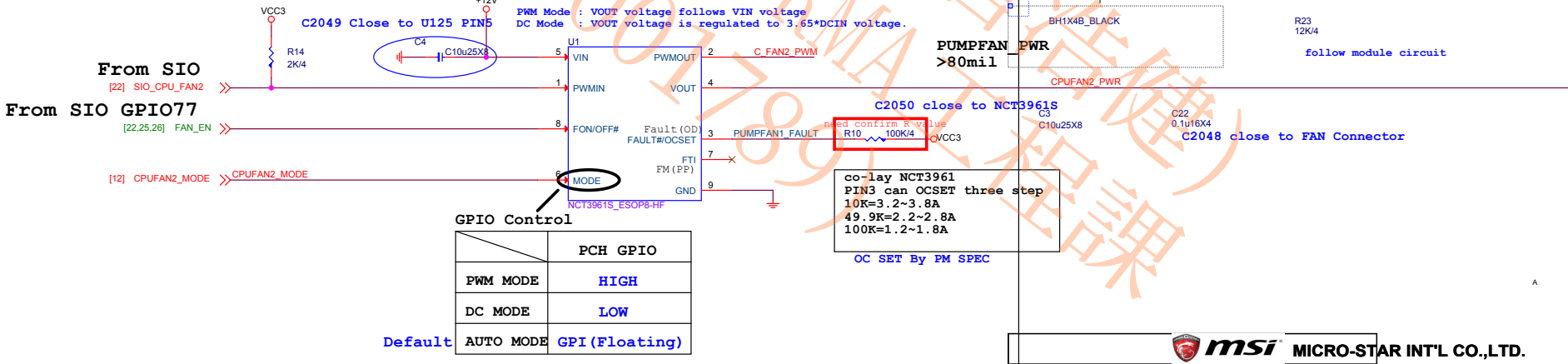
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



MICRO-STAR INT'L CO.,LTD.

Title: CPU and PUMP FAN

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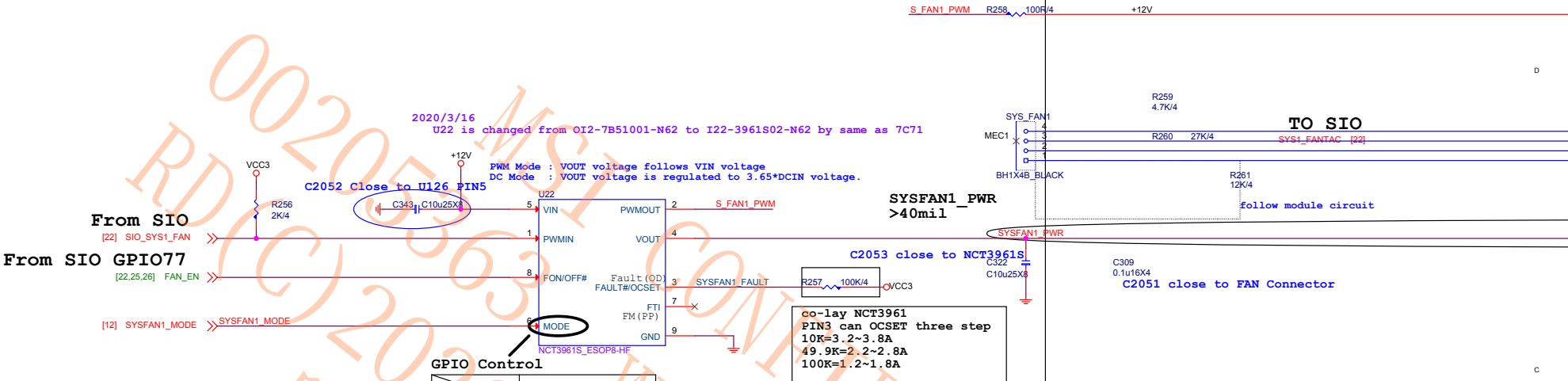
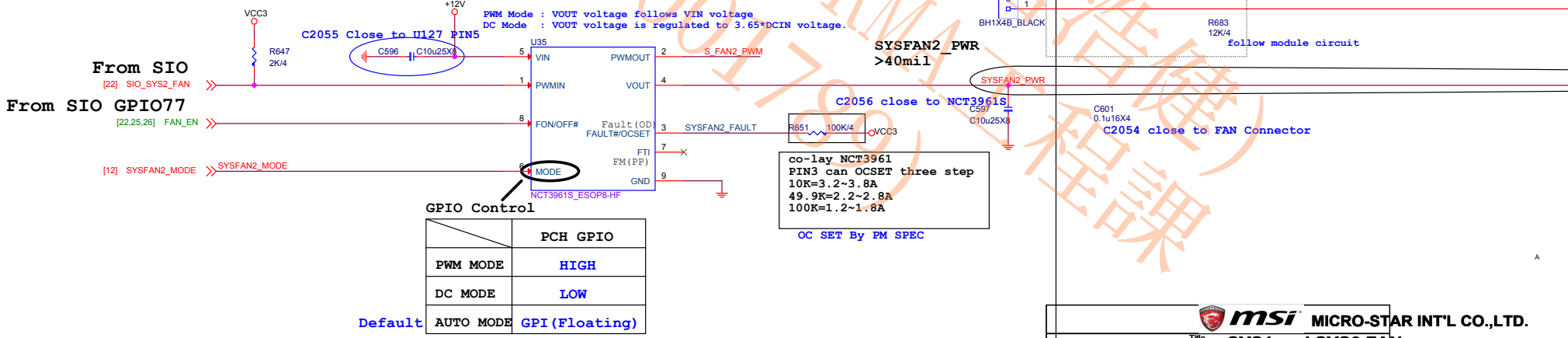
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

MICRO-STAR INT'L CO.,LTD.

Title: SYS1 and SYS2 FAN

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MICRO-STAR INT'L CO.,LTD.

Title

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ALC1200

follow PCH power well
need check

PIN 1~12, 47~49 reference GND,
others reference AGND

UA1
ALC1200-VD1-CG-RH
B05-012000C-R09

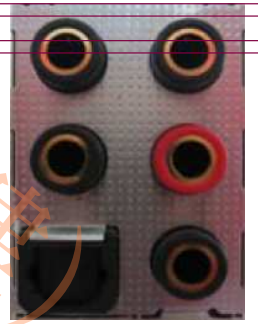
2020/2/18
CA15, CA16 are changed from C11-1067313-M09
to C11-1067614-M09 by audio percision

2020/3/13
ECA1, ECA2, ECA3, ECA4, ECA5 are changed from C91-1011041-P01 to C91-1011051-N07 by buyer request

Add CA14 and CA19 as close as possible to pin 24 at UA1

Closed PIN1
Closed PIN9
closed PIN43
closed PIN25
Closed Pin3
Closed Pin 27
close to codec
For EMI
Closed Codec

LIN_OUT
SURR
LIN_IN
CEN/BAS
MIC1



MICRO-STAR INT'L CO.,LTD.

Title	AUDIO-ALC1200-1	
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2019/9/27
DA8, RA54, RA55 are added by Robert's comment

DA3
[28] LINE2_VREFO
Z
Y
X
F_LINE_2L RA34 4.7K/4 F_LINE2L
F_LINE_2R RA33 4.7K/4 F_LINE2R
S-BAT54A

DA8
[28] MIC2_VREFO
Z
Y
X
F_MIC_2L RA48 4.7K/4 F_MIC2_L
F_MIC_2R RA44 4.7K/4 F_MIC2_R
S-BAT54A

F_LINE2L 2 1 DA4 ESD-MLVS0402L04-HF
F_LINE2R 2 1 DA5 ESD-MLVS0402L04-HF
F_MIC2_R 2 1 DA6 ESD-MLVS0402L04-HF
F_MIC2_L 2 1 DA7 ESD-MLVS0402L04-HF

F_MIC2_L RA47 22K/4
F_MIC2_R RA43 22K/4
F_LINE2L RA39 22K/4
F_LINE2R RA40 22K/4

Close to Front panel
ESD protect
D0G-2710510-I05
AVL:ODG-7C71001-T43

[28] MIC2_L MIC2_L RA49 75R/4 F_MIC2_L
[28] MIC2_R MIC2_R RA45 75R/4 F_MIC2_R
F_LINE2_R RA37 75R/4 F_LINE2R
[28] SENSE_C RA46 47R/4 HPON
F_LINE2_L RA35 75R/4 F_LINE2L

JAUD1
1 MIC
2 GND
3 MICPWR
4 PRESENCE#
5 FLINE OUTR
6 LINE NEXT R
7 HPON
8
9 FLINE OUTL
10 LINE NEXT L
H2X5[8]M
N31-2051411-H06

MIC2_JD
LINE2_JD

CA42 1000p50X/4
RA42 39.2K1%/4
RA41 20K1%4

Close to Front panel
For HDA/AC97 front cable.

De-POP circuit

2020/2/25
QA10, QA9, QA13, QA12, QA2, QA1, QA4, QA3, QA6, QA5, QA8, QA7, QA16, QA17, QA15, QA14, RA35, QA11, RA36, RA34, LA3, CA38 are deleted and RA32, RA33, RA20, RA21, RA28, RA30, RA39, RA38 are stuffed by PM request

RA21 0R/4
ALOUT_R Remove LOUT_R

RA25 0R/4
ACEN_OUT Remove CEN_OUT

RA20 0R/4
ALOUT_L Remove LOUT_L

RA24 0R/4
ABASS Remove BASS

RA22 0R/4
ASROUT_R Remove SROUT_R
LOUT_L [28]
LOUT_R [28]

RA23 0R/4
ASROUT_L Remove SROUT_L
SROUT_L [28]
SROUT_R [28]
CEN_OUT [28]
BASS [28]

RA38 0R/4
LINE2_R Remove F_LINE2_R
ALOUT_R [28]
ALOUT_L [28]
ASROUT_R [28]
ASROUT_L [28]
ACEN_OUT [28]
ABASS [28]

RA36 0R/4
LINE2_L Remove F_LINE2_L
LINE2_R [28]
LINE2_L [28]

MICRO-STAR INT'L CO.,LTD.
Title AUDIO-ALC1200-2
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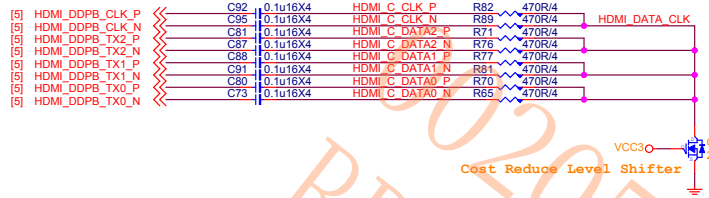
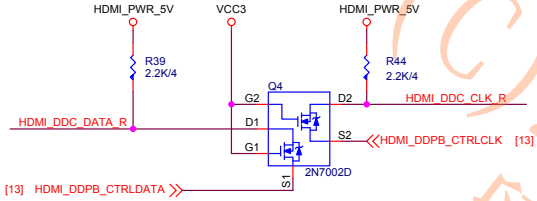
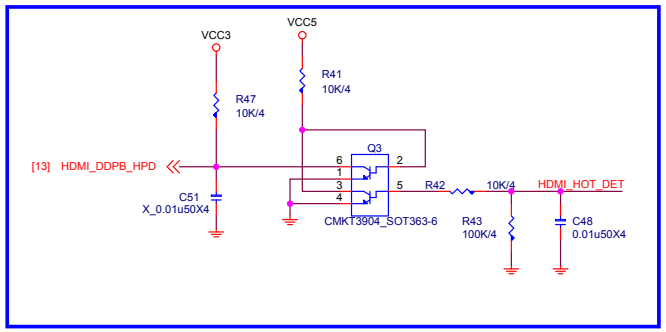
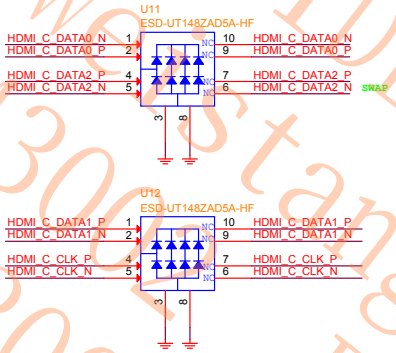
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

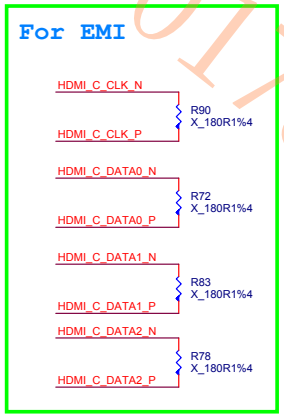




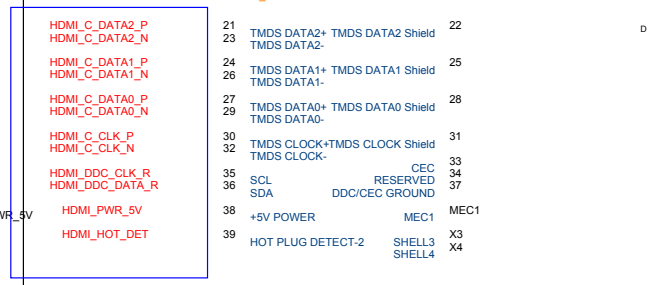
HPD

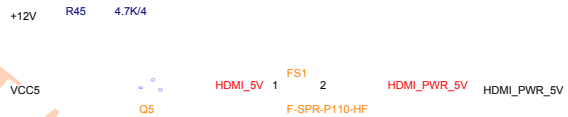




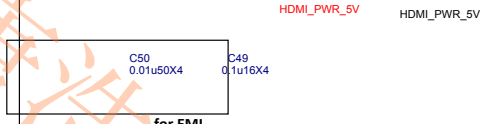


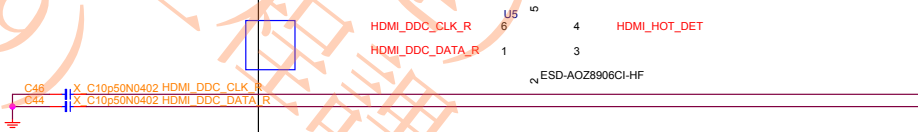
2020/3/16
DP_HDMI1 is changed from ON5-7C77001-F82 to N58-39M0111-F82 by PM request





2019/11/12
Q33 is changed from OD3-7C71001-ST8 to D03-2408N09-ST8 by Ivy's comment





2019/11/25
C2854, C2855 are reserved by EMI suggestion

MICRO-STAR INT'L CO.,LTD.

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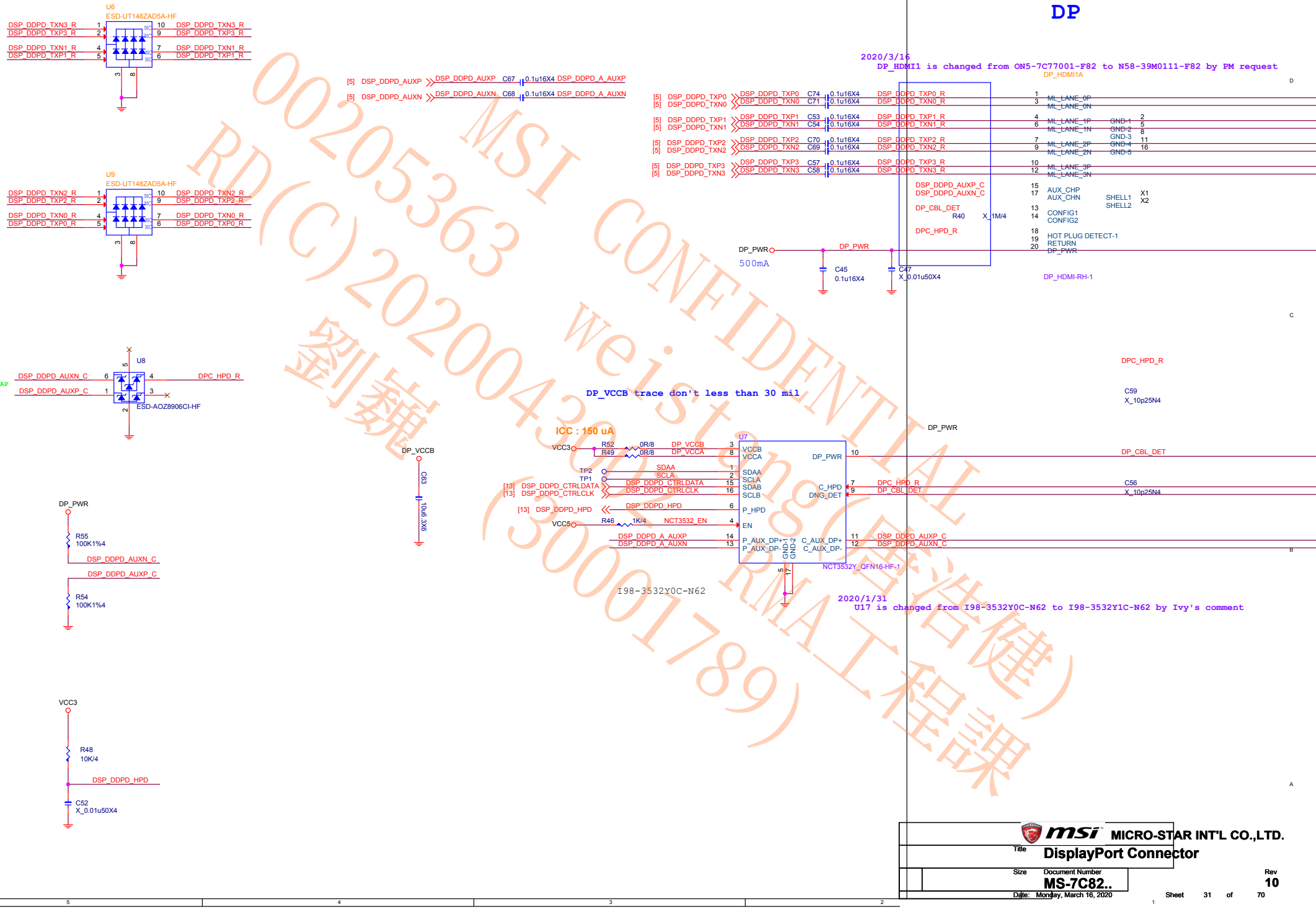
DP



MICRO-STAR INT'L CO.,LTD.		
Title: DisplayPort Connector		
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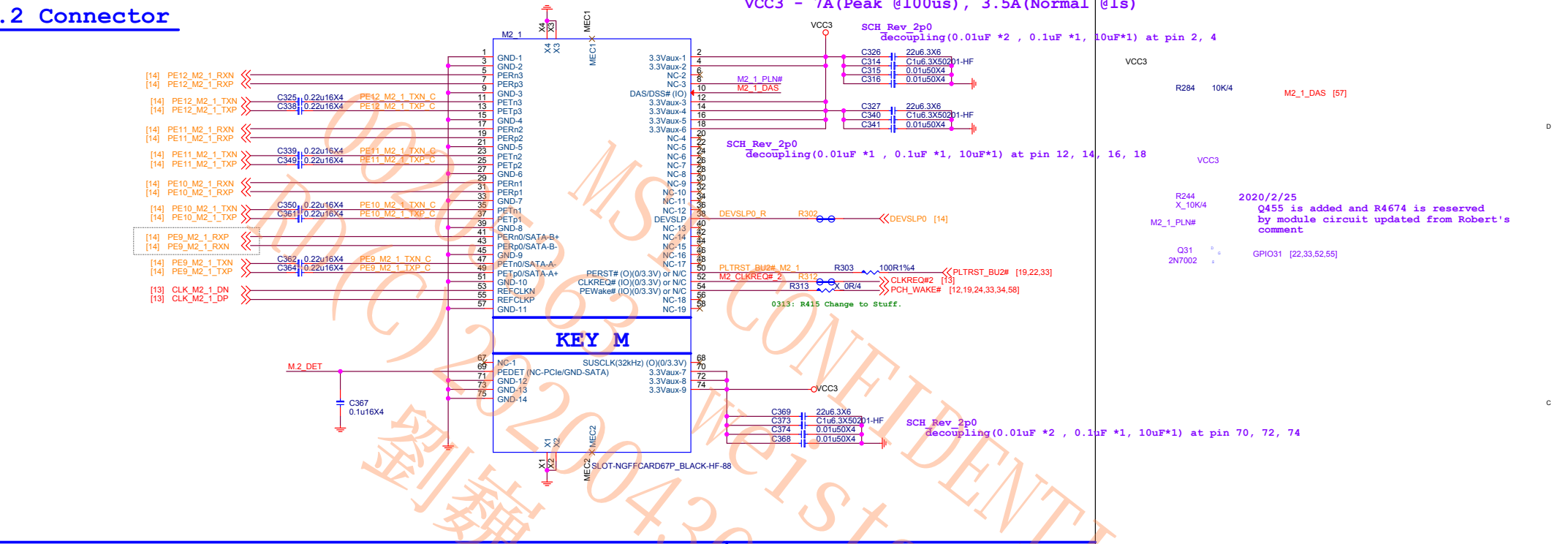
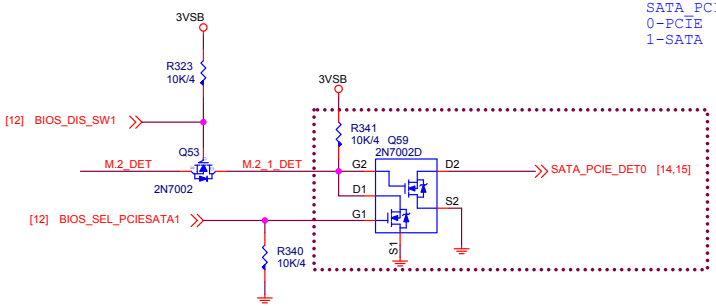
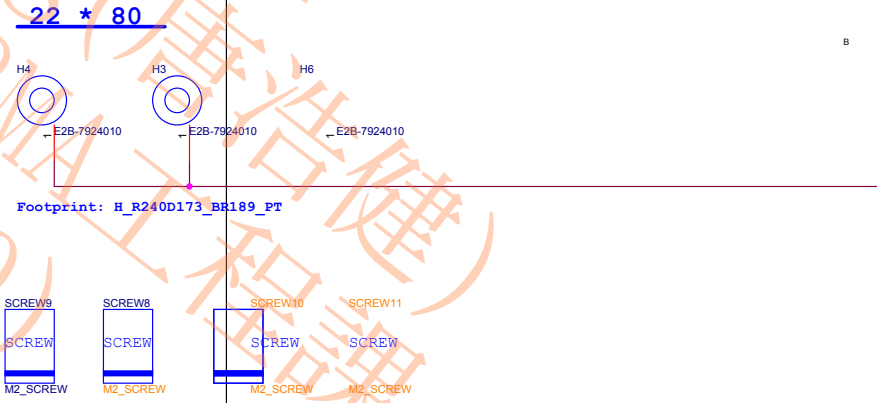
M.2 Connector







BIOS_MODE

BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

MICRO-STAR INT'L CO.,LTD.

Title: M.2-SLOT1

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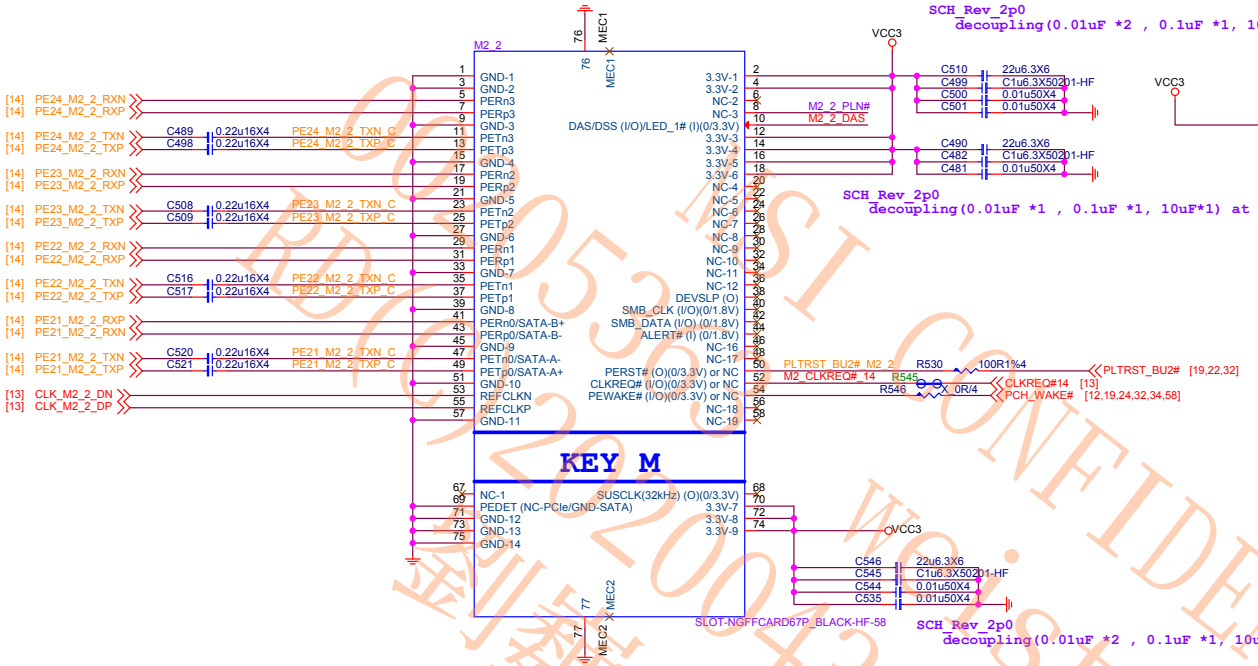
VCC3 - 7A(Peak @100us), 3.5A(Normal @1s)



SCH_Rev_2p0
decoupling(0.01uF *2 , 0.1uF *1, 10uF*1) at pin 2, 4

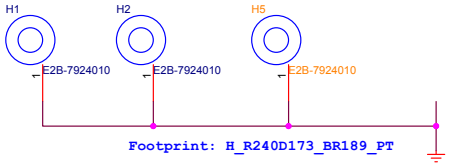
SCH_Rev_2p0
decoupling(0.01uF *1 , 0.1uF *1, 10uF*1) at pin 12, 14, 16, 18

SCH_Rev_2p0
decoupling(0.01uF *2 , 0.1uF *1, 10uF*1) at pin 70, 72, 74

2020/2/17
M2_2 is changed from N15-0670330-L06 to N15-0670820-L06 by PM request

2020/2/25
Q456 is added and R4675 is reserved
by module circuit updated from Robert's comment

22 * 80



Footprint: H_R240D173_BR189_PT

2019/10/28
H3, H7 are deleted by PM spec updated

2019/11/8
H3, H7 are added by PM spec updated

2019/11/18
H7 is added by PM spec updated

SCREW1 SCREW7
M2_SCREW M2_SCREW

MICRO-STAR INT'L CO.,LTD.

Title: M.2-SLOT2

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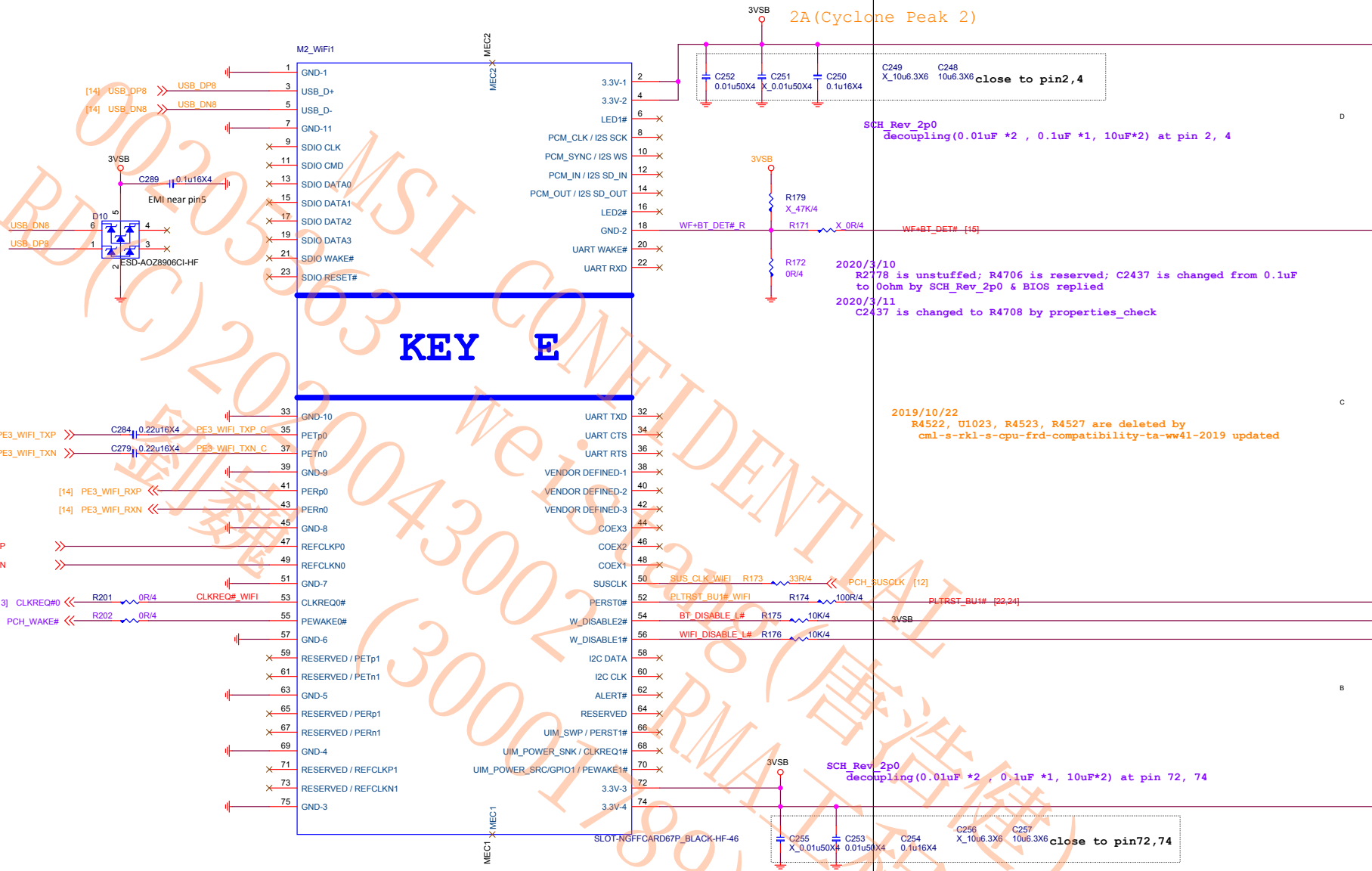
Option BOM

2A(Cyclone Peak 2)



SCH_Rev_2p0
decoupling(0.01uF *2 , 0.1uF *1, 10uF*2) at pin 2, 4

2020/3/10
R2778 is unstuffed; R4706 is reserved; C2437 is changed from 0.1uF to 0ohm by SCH_Rev_2p0 & BIOS replied

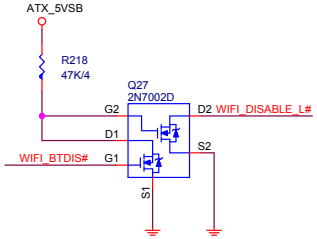
2020/3/11
C2437 is changed to R4708 by properties_check

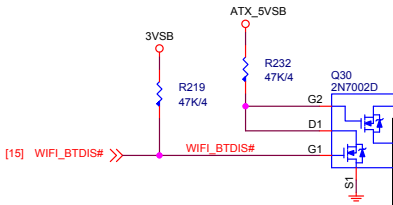
2019/10/22
R4522, U1023, R4523, R4527 are deleted by cml-s-rkl-s-cpu-frd-compatibility-ta-ww41-2019 updated

SCH_Rev_2p0
decoupling(0.01uF *2 , 0.1uF *1, 10uF*2) at pin 72, 74

2020/1/31
R2776 is changed from 10Kohm to 0ohm; R2776 is changed from pull up to 3VSB to CLKREQ#0; R4673 is added by circuit correctness

2020/3/12
SCREW5, SCREW6, Wireless1 are stuffed by PM request





MICRO-STAR INT'L CO.,LTD.

Title: M2_WIFI

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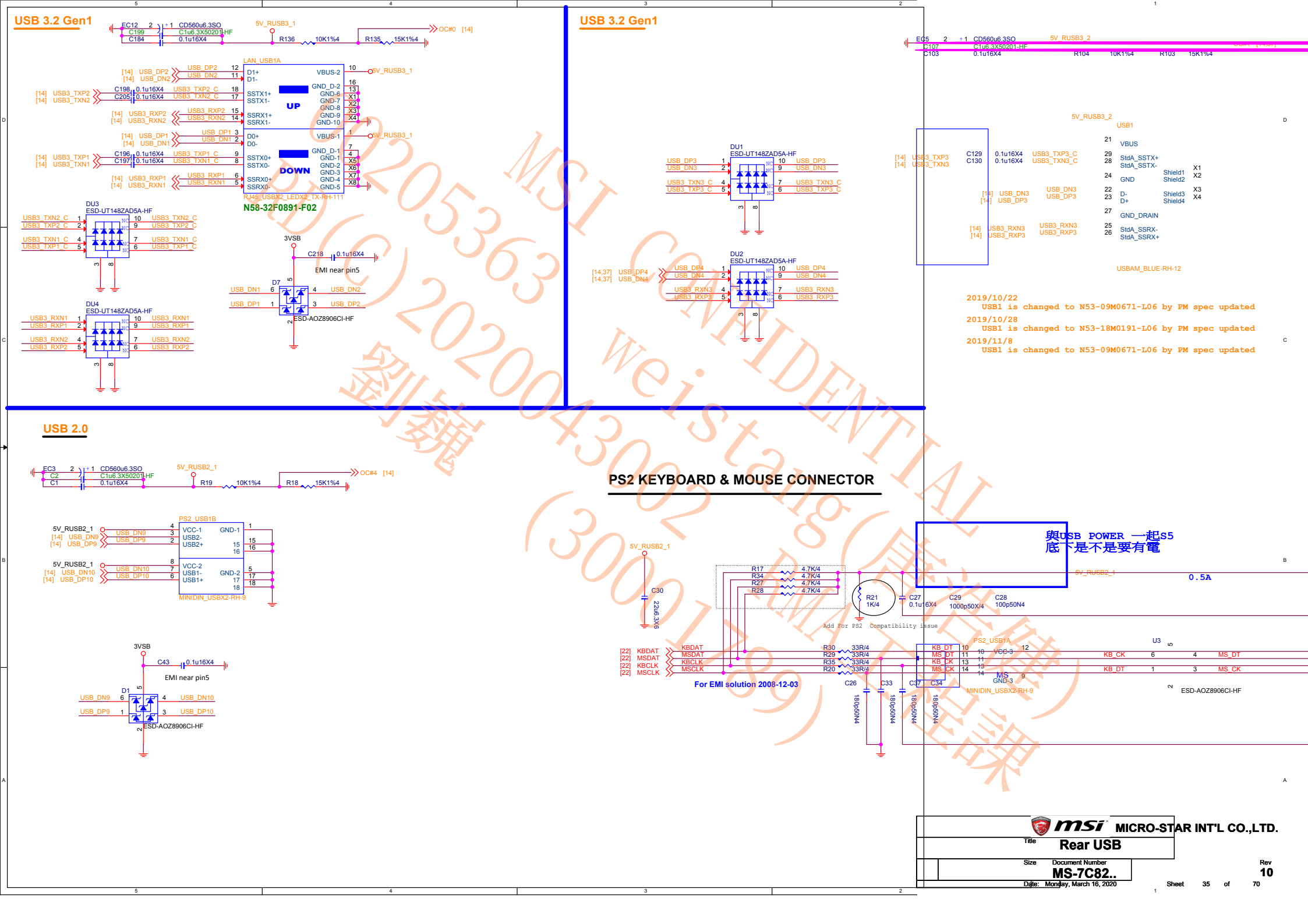
USB 3.2 Gen1
EC12 CD560u6.3SO
C199 C1u6.3X50201-HF
C184 0.1u16X4
5V_RUSB3_1
R136 10K1%4
R135 15K1%4
OC#0 [14]
LAN_USB1A
UP
DOWN
N58-32F0891-F02
RJ45_USBX2_LEDX2_TX-RH-111
DU3 ESD-UT148ZAD5A-HF
DU4 ESD-UT148ZAD5A-HF
3VSB
C218 0.1u16X4
EMI near pin5
D7
ESD-AOZ8906CI-HF
USB 3.2 Gen1
DU1 ESD-UT148ZAD5A-HF
DU2 ESD-UT148ZAD5A-HF
EC5 CD560u6.3SO
C107 C1u6.3X50201-HF
C103 0.1u16X4
5V_RUSB3_2
R104 10K1%4
R103 15K1%4
USB1
USBAM_BLUE-RH-12
2019/10/22
USB1 is changed to N53-09M0671-L06 by PM spec updated
2019/10/28
USB1 is changed to N53-18M0191-L06 by PM spec updated
2019/11/8
USB1 is changed to N53-09M0671-L06 by PM spec updated
USB 2.0
EC3 CD560u6.3SO
C2 C1u6.3X50201-HF
C1 0.1u16X4
5V_RUSB2_1
R19 10K1%4
R18 15K1%4
OC#4 [14]
PS2_USB1B
MINIDIN_USBX2-RH-9
PS2 KEYBOARD & MOUSE CONNECTOR
C30 22u6.3X6
R17 R34 R27 R28 4.7K/4
R21 1K/4
C27 0.1u16X4
C29 1000p50X/4
C28 100p50N4
Add for PS2 Compatibility issue
R30 R29 R35 R20 33R/4
C26 C33 C37 C34 180p50N4
For EMI solution 2008-12-03
與USB POWER 一起S5
底下是不是要有電
0.5A
PS2_USB1A
ESD-AOZ8906CI-HF
MICRO-STAR INT'L CO.,LTD.
Title
Rear USB
Size
Document Number
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MICRO-STAR INT'L CO.,LTD.

Title X

Size Document Number Rev
MS-7C82.. 10

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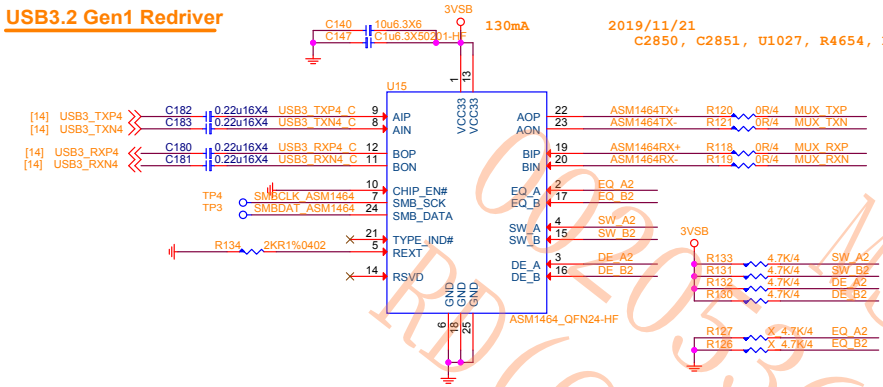
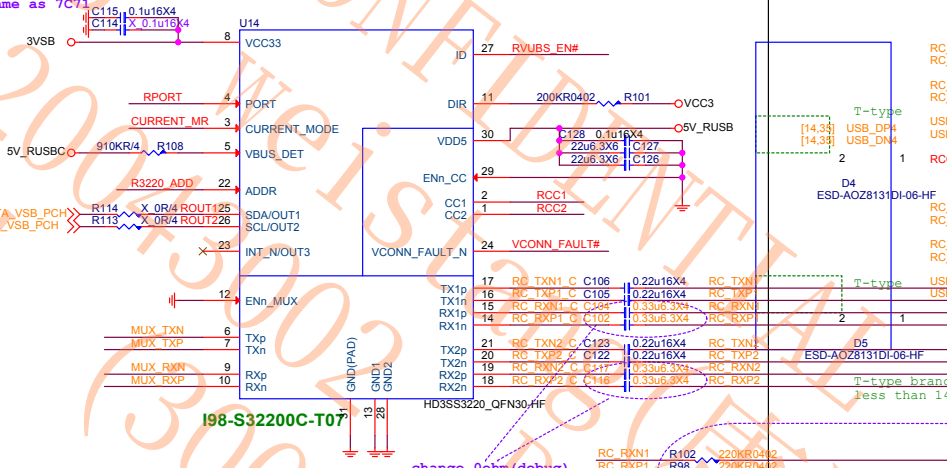
USB3.2 Gen1 Redriver

2019/11/21
C2850, C2851, U1027, R4654, R4655, R4656, R4657, R311, R4658, R4659, R4660, R4661, R4662, R4663 are added by traces length were over spec

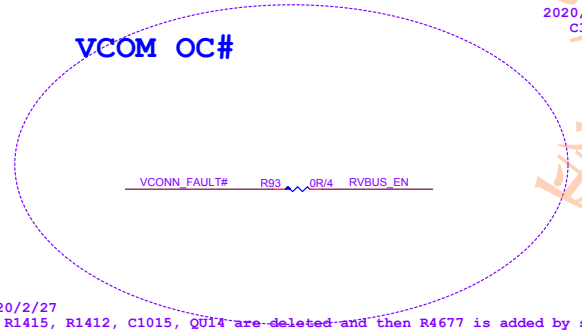


USB Type-C MUX with Configuration Channel (CC)

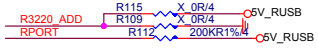


2020/2/27
C360 is unstuffed by same as 7C71

VCOM OC#

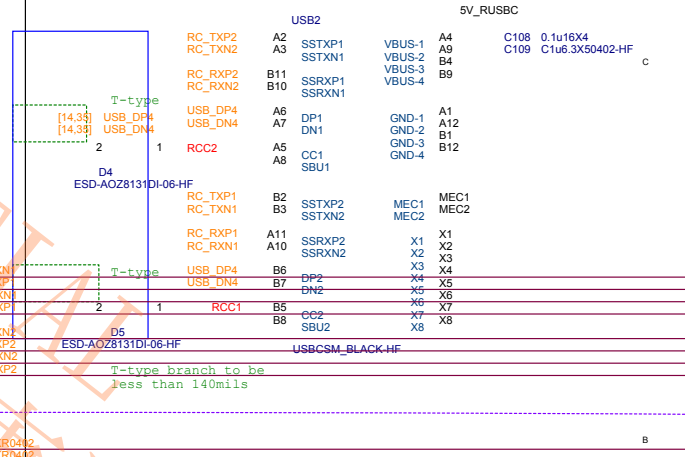


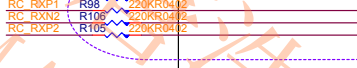
2020/2/27
R1415, R1412, C1015, QU14 are deleted and then R4677 is added by same as 7C71



change 0ohm(debug)

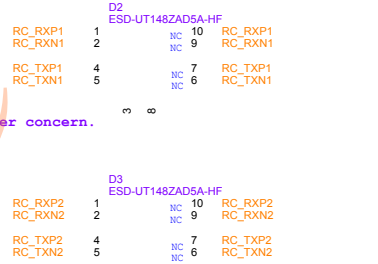
TYPE-C





ESD Protection
NEAR CONNECTOR

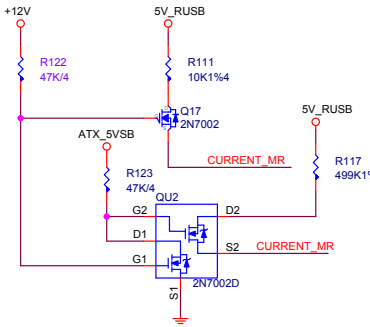
all remove(debug)



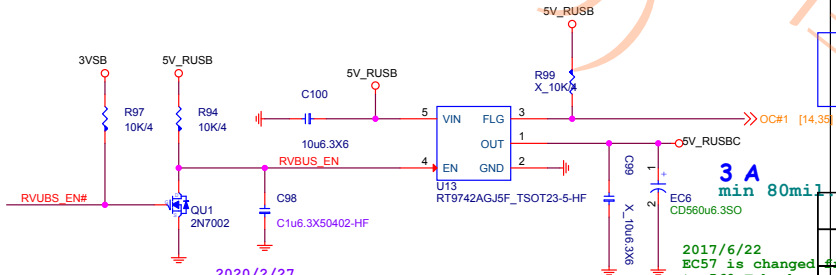
Current Mode

L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A

2020/2/27
R4678 is added by same as 7C71



2020/2/7
D105, D12 are changed from D0G-06A030C-A68 to D0G-28B030C-U33 by buyer concern.



2020/2/27
C2837 is stuffed by same as 7C71

2017/6/22
EC57 is changed from 470uF to 560uF by buyer request

MICRO-STAR INT'L CO.,LTD.			
Title: Rear USB 3.2 Gen1 Type C			
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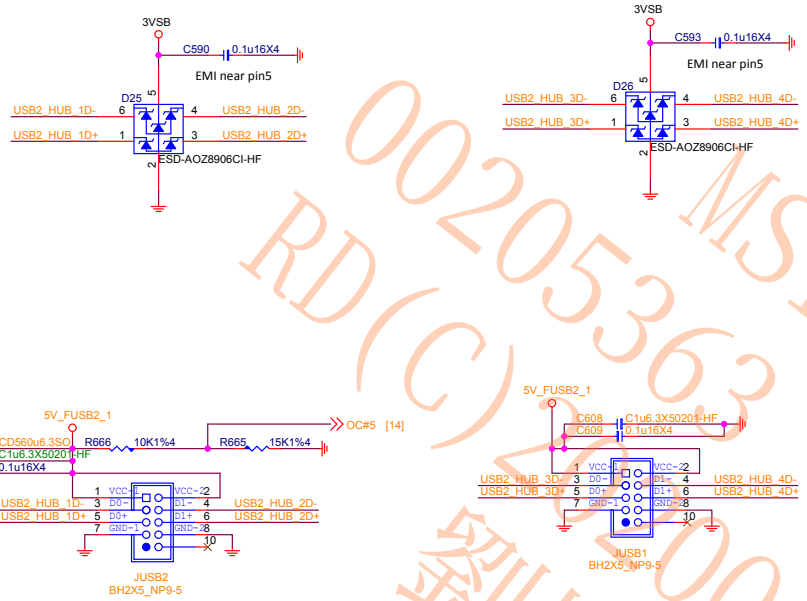
USB 2.0

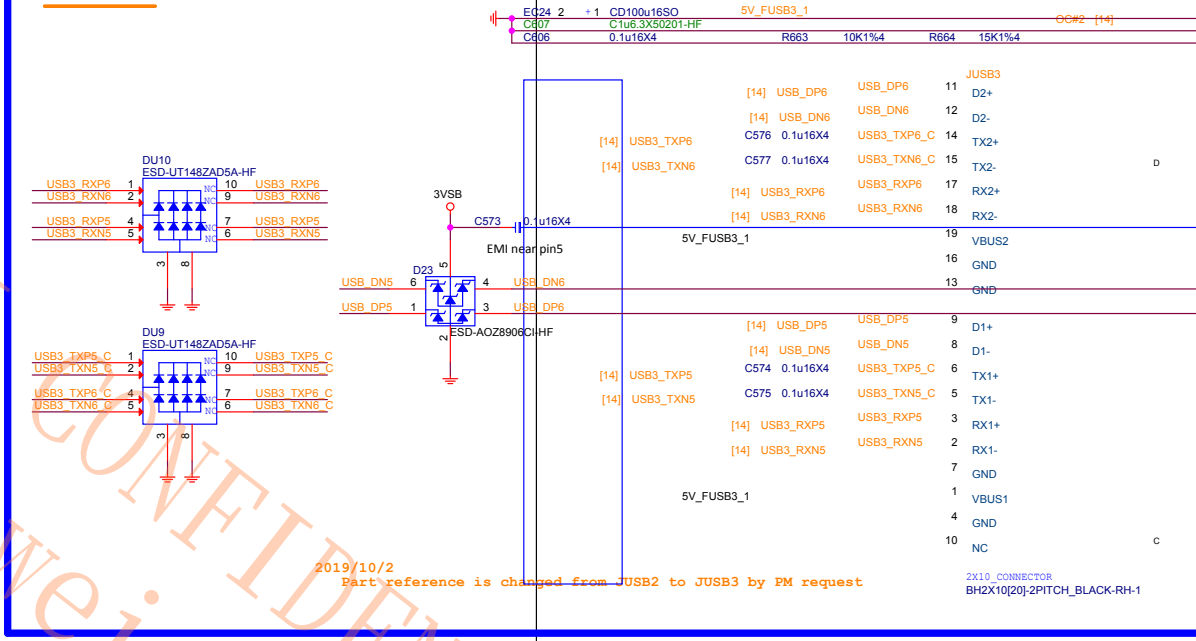


2019/10/2
Part reference is changed from JUSB1 to JUSB2 by PM request

2019/10/22
Part reference is changed from JUSB2 to JUSB1 by PM request

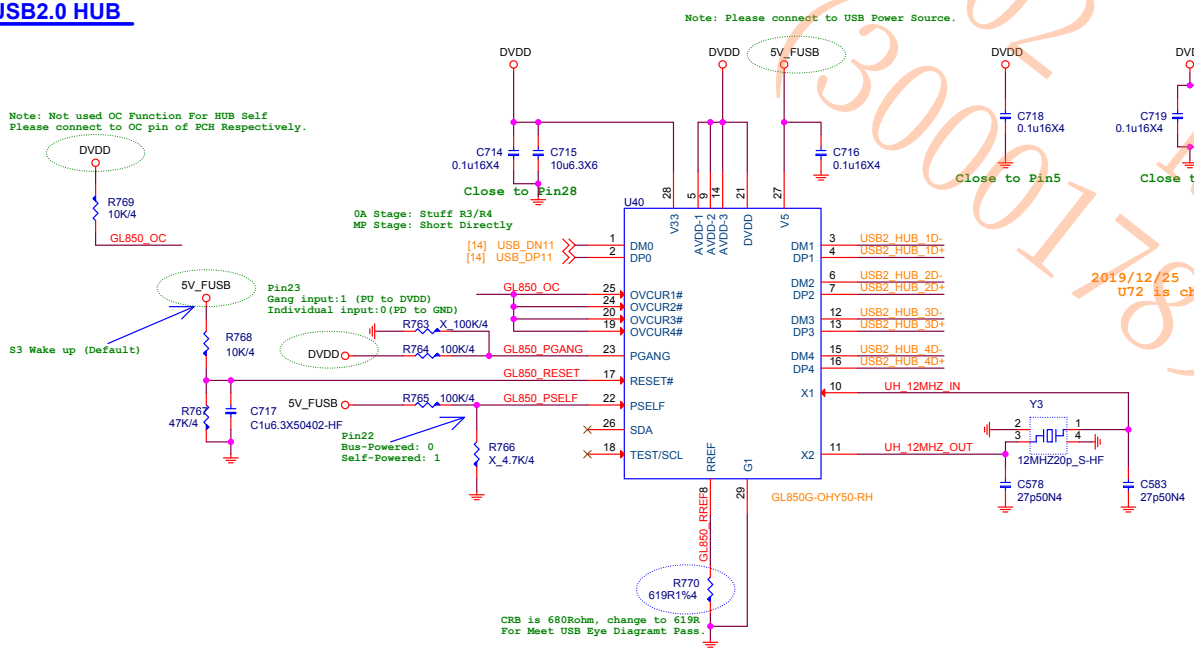
2019/10/2
Part reference is changed from JUSB4 to JUSB1 by PM request

USB 3.2 Gen1



2019/10/2
Part reference is changed from JUSB2 to JUSB3 by PM request

GL850G USB2.0 HUB



2019/12/25
U72 is changed from B07-GL8500C-G08 to B07-GL8501C-G08 by PM spec updated

MICRO-STAR INT'L CO.,LTD.		
Title: FUSB 3.2 G1/GL850 USB2.0 Hub		
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USB3.2 Gen1 Redriver

3VSB 130mA

C372 10u6.3X6
C353 C1u6.3X50201-HF

U24 ASM1464_QFN24-HF

[14] USB3_TXP8 CU6 0.22u16X4 USB3_TXP8_C
[14] USB3_TXN8 CU5 0.22u16X4 USB3_TXN8_C
[14] USB3_RXP8 CU7 0.22u16X4 USB3_RXP8_C
[14] USB3_RXN8 CU8 0.22u16X4 USB3_RXN8_C

AIP AIN BOP BON CHIP_EN# SMB_SCK SMB_DATA TYPE_IND# REXT RSVD
AOP AON BIP BIN EQ_A EQ_B SW_A SW_B DE_A DE_B
VCC33 GND

FASM1464TX+ R310 0R/4 F_MUX_TXP
FASM1464TX- R299 0R/4 F_MUX_TXN
FASM1464RX+ R322 0R/4 F_MUX_RXP
FASM1464RX- R311 0R/4 F_MUX_RXN

F_EQ_A2 F_EQ_B2 F_SW_A2 F_SW_B2 F_DE_A2 F_DE_B2

R293 2KR1%0402

3VSB
R292 4.7K/4 F_SW_A2
R333 4.7K/4 F_SW_B2
R291 4.7K/4 F_DE_A2
R332 4.7K/4 F_DE_B2
R290 X_4.7K/4 F_EQ_A2
R331 X_4.7K/4 F_EQ_B2

2020/3/9
U1028 is added and related parts are added by SA result from 7C81

2019/10/2
Part reference is changed from JUSB3 to JUSB4 by PM request

EC17 C275 C274 CD560u6.3SO C1u6.3X50201-HF 0.1u16X4
5V_FUSBC

JUSB4

FC_TXP1 FC_TXN1 FC_RXP1 FC_RXN1 FC_TXP2 FC_TXN2 FC_RXP2 FC_RXN2
TX1+ TX1- RX1+ RX1- TX2+ TX2- RX2+ RX2-
VBUS-1 VBUS-2 VBUS-3 GND-1 GND-2 GND-3
D+ D- SBU1 SBU2 CC1 VCONN
X1 X2 X3 X4 X5 X6 MEC1 MEC2

[14] USB_DP7 [14] USB_DN7 USB_DP7 USB_DN7
F_CC1 F_CC2

DU6 DU8 ESD-AOZ8131DI-06-HF FTYPEC_24P

FC_RXN1 R234 220KR0402
FC_RXP1 R233 220KR0402
FC_RXN2 R205 220KR0402
FC_RXP2 R203 220KR0402

U20

3VSB C332 0.1u16X4
VCC33 ID PORT DIR CURRENT_MODE VDD5 VBUS_DET ENn_CC ADDR CC1 CC2 SDA/OUT1 SCL/OUT2 INT_N/OUT3 VCONN_FAULT_N ENn_MUX TXp TXn RXp RXn TX1p TX1n RX1p RX1n TX2p TX2n RX2p RX2n GND(PAD) GND1 GND2

5V_FUSB R283 200KR1%/4 FPORT
FCURRENT_MR
5V_FUSBC R282 910KR/4
5V_FUSB X_0R/4 R271 X_0R/4 R262 F3220_ADD
F_MUX_TXN F_MUX_TXP F_MUX_RXN F_MUX_RXP

FVUBS_EN# 200KR0402 R270 VCC3
C334 0.1u16X4 22u6.3X6 C344 22u6.3X6 C333
F_CC1 F_CC2
FVCONN_FAULT#

FC_TXN1_C C290 FC_TXP1_C C291 FC_RXN1_C C305 FC_RXP1_C C304
FC_TXN2_C CU1 FC_TXP2_C CU2 FC_RXN2_C CU4 FC_RXP2_C CU3
0.22u16X4 0.33u6.3X4

HD3SS3220_QFN30-HF

I98-S32200C-T07

2019/10/9
R4445, R4447, R4448, R4450 are changed from 200Kohm to 220Kohm by PDG_Rev0p7

2020/3/6
The pin 4, 5, 6, 7 of DU16 & DU17 should be placed as closed as possible to JUSB4

DU7 ESD-UT148ZAD5A-HF
FC_TXN1 FC_TXP1 FC_RXP1 FC_RXN1

DU5 ESD-UT148ZAD5A-HF
FC_TXN2 FC_TXP2 FC_RXP2 FC_RXN2

2020/3/6
U39 is changed from I9E-0154100-AD0 to I98-S32200C-T07 and related parts are changed on page 39, 14 by DQA test result

Current Mode

L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A

+12V R338 47K/4
5V_FUSB R339 10K1%/4
Q58 2N7002
FCURRENT_MR
ATX_5VSB R336 47K/4
5V_FUSB R337 499K1%
Q56 G2 D2 D1 S2 G1 2N7002D

VBUS

3 A
min 80mil.

5V_FUSB R180 10K/4
FVCONN_FAULT# R181 0R/4 F_VBUS_EN
3VSB R191 10K/4 FVUBS_EN#
QU3 2N7002
C267 C1u6.3X50402-HF

5V_FUSB C260 10u6.3X6
U18 VIN FLG OUT EN GND RT9742AGJ5F_TSOT23-5-HF
F_VBUS_EN
OC#3 [14]
5V_FUSBC

3VSB C331 0.1u16X4
EMI near pin5
D11 ESD-AOZ8906CI-HF
USB_DN7 USB_DP7

MICRO-STAR INT'L CO.,LTD.
Title: Front USB 3.2 Gen 1 Type C
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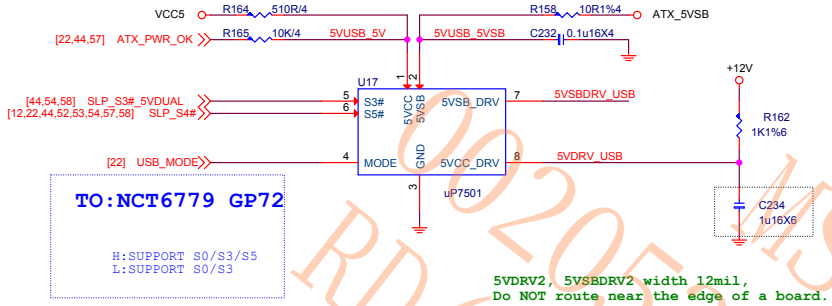
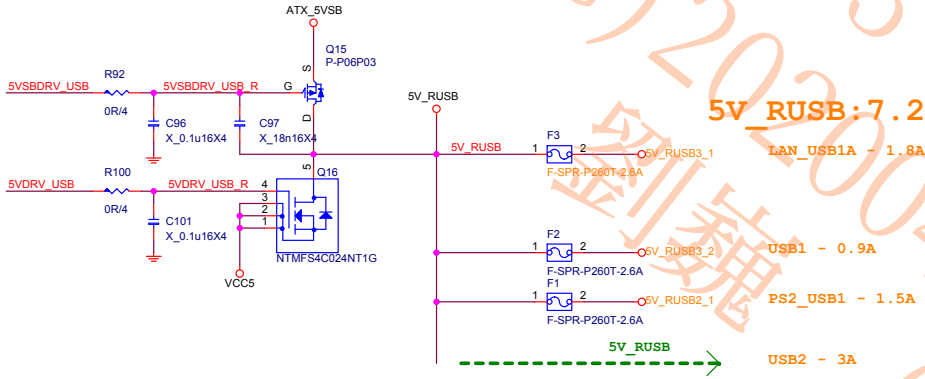
USB POWER



5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.

REAR USB PORT POWER



5V_RUSB:7.2A

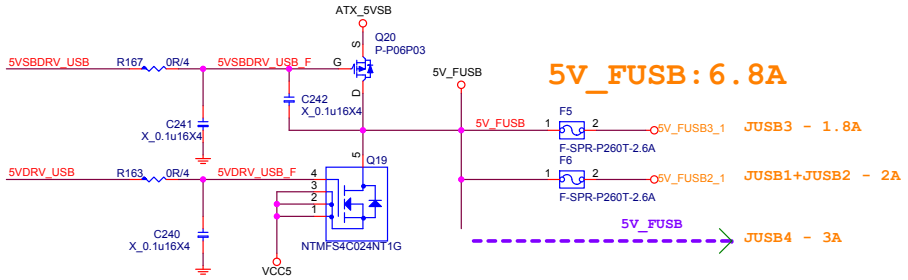
LAN_USB1A - 1.8A

USB1 - 0.9A

PS2_USB1 - 1.5A

USB2 - 3A

FRONT USB PORT POWER



5V_FUSB:6.8A

JUSB3 - 1.8A

JUSB1+JUSB2 - 2A

JUSB4 - 3A

2020/3/6
F9 is deleted by unnecessary circuit

MICRO-STAR INT'L CO.,LTD.

Title: USB /PS2 Power

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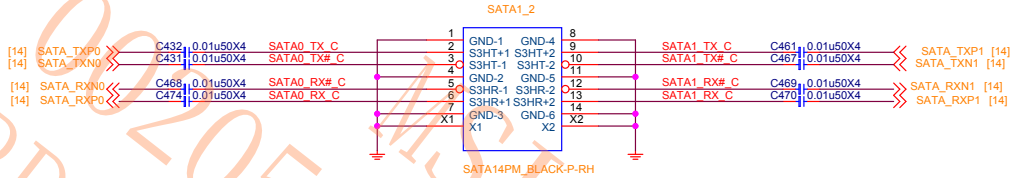
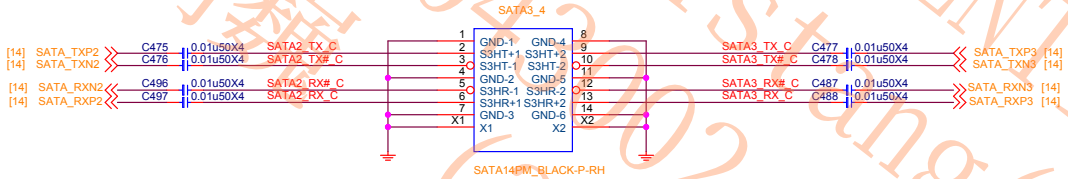
SATA PORT 0,1

Black 90 degree



SATA PORT 2,3

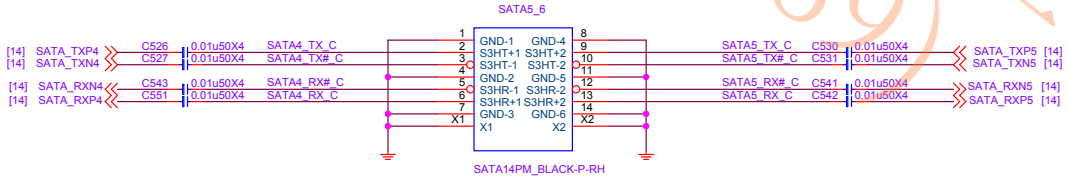
Black 90 degree



SATA PORT 4,5

Black 90 degree

2020/2/17
SATA5_6, C2861, C2862, C2863, C2864, C2865, C2866, C2867, C2860 are added by PM request



MICRO-STAR INT'L CO.,LTD.

Title: SATA connector

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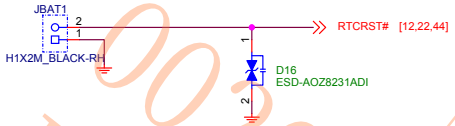
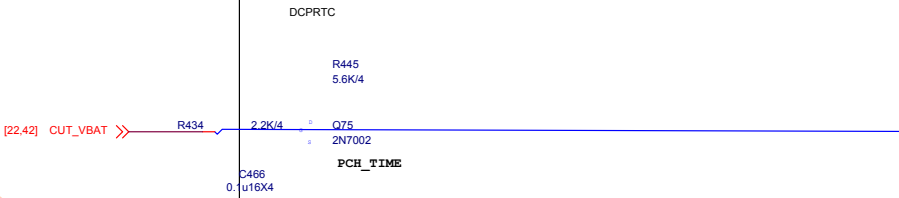
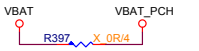
CUT_VBAT/CLR_CMOS

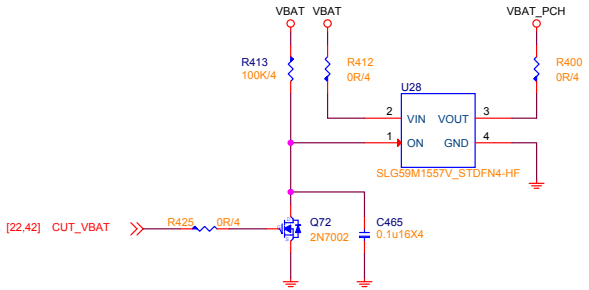


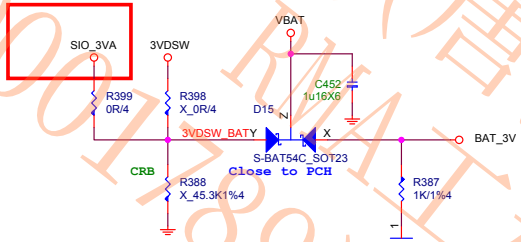
2020/1/31
R669, R454, R676 are stuffed by module circuit updated



VBAT







2019/9/25
R492 is unstuffed and R493, U42, R484, R467, C523, Q69, R443 are stuffed by Ivy's cooemt

2019/10/17
BAT1 is changed from N91-01F0151-H06 to N32-1020BF1-H06 by PM spec updated

2019/11/8
BAT1 is changed from N32-1020BF1-H06 to N91-01F0151-H06 by PM spec updated

MICRO-STAR INT'L CO.,LTD.

Title: VBAT Circuit

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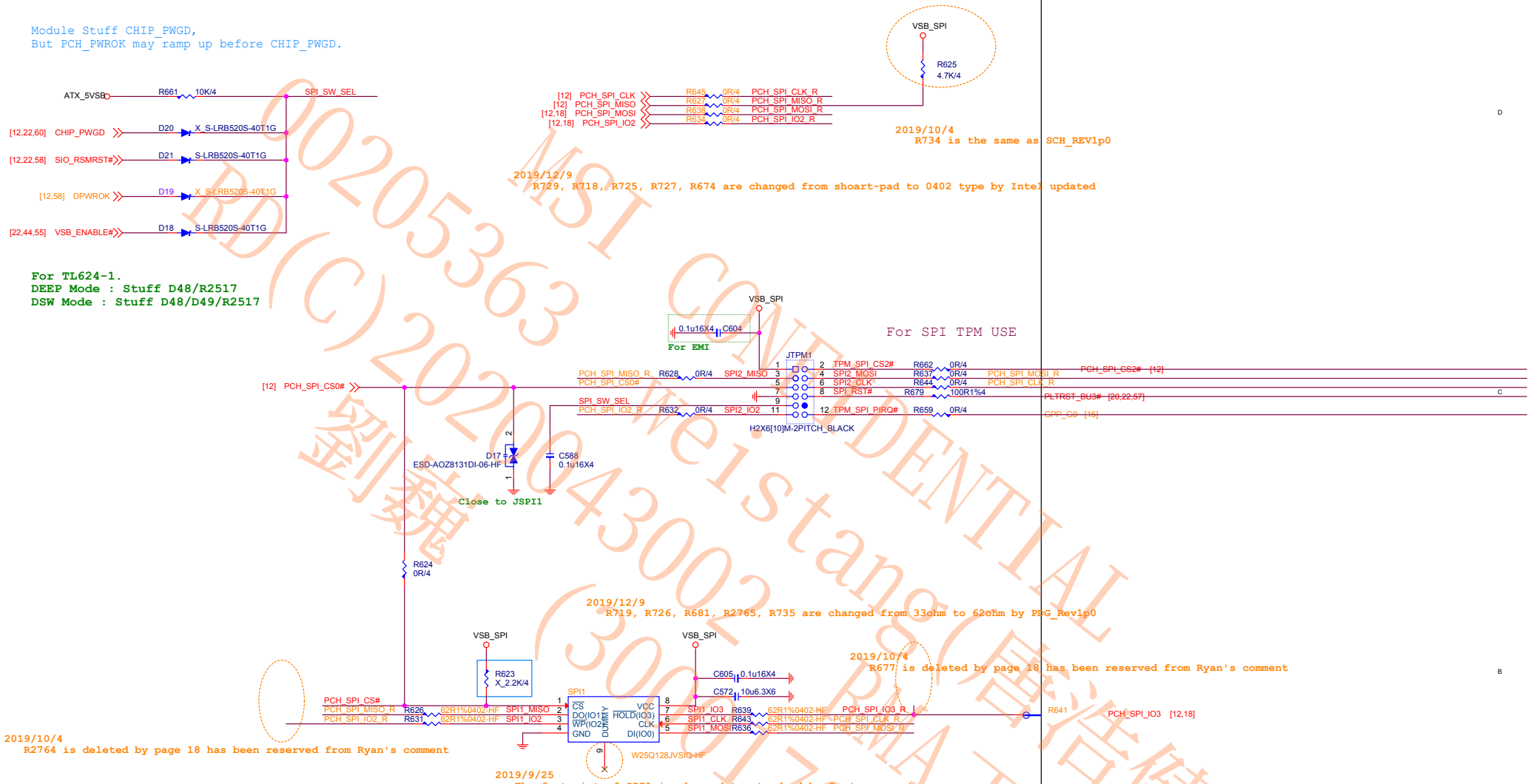

MICRO-STAR INT'L CO.,LTD.

Title: BIOS ROM

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5VDIMM FOR DDR

7.389A

VCC5 R37 510R/4 — R31 10R1%4 ATX_5VSB
[22,40,44,57] ATX_PWR_OK R36 10K1%4 5VDIMM_5V — 5VDIMM_5VSB C35 0.1u16X4
ATX_5VSB 5VDIMM
P-P06P03 Q1
U4 S3# S5# 5VCC 5VSB 5VSB_DRV DIMM_SBDRV C36 18n16X4
[40,44,54,58] SLP_S3#_5VDUAL
[12,22,40,44,52,53,54,57,58] SLP_S4#
MODE GND 5VCC_DRV DIMM_VCCDRV
uP7501
R38 1K1%6 C38 0.022u25X4 Q2 C40 0.1u16X4
+12V VCC5
N-SM4503NHKPC-TRG_DFN5x6-8-HF

2019/9/27
Q378 is changed to N-PK810BA by Ivy's comment
2019/12/17
Q378 is changed to SM4503NHKPC-TRG by Ivy's comment

5VDUAL

VCC5 R308 510R/4 5VCC_5V — 5VSB_5V R298 10R1%4 ATX_5VSB
[22,40,44,57] ATX_PWR_OK R297 10K1%4 — C352 0.1u16X4
Q57 P-P06P03
6.07A
5VDUAL
U26 S3# S5# 5VCC 5VSB 5VSB_DRV PCH_SBDRV C370 18n16X4
[40,44,54,58] SLP_S3#_5VDUAL
[12,22,40,44,52,53,54,57,58] SLP_S4#
ATX_5VSB R309 47K/4 S_MODE
MODE GND 5VCC_DRV PCH_VCCDRV
uP7501
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
[22,43,44,55] VSB_ENABLE# Q67 2N7002
R321 1K1%6 C366 0.022u25X4
+12V VCC5
Q55 C371 X_0.1u16X4 R373 1K/4 R374 1K/4
N-SM4503NHKPC-TRG_DFN5x6-8-HF

2019/9/27
Q93 is changed to N-PK810BA by Ivy's comment
2019/12/17
Q93 is changed to SM4503NHKPC-TRG by Ivy's comment
2019/10/7
Q59, R4626, C2821, R4627, C2822 are added and R4626 is reserved by Ryan's comment

ATX_5VSB R225 47K/4
C303 C1u6.3X50402-HF G2 D1 G1 Q40 D2 S2 S1 2N7002D 5VCC_5V
R266 47K/4 VCC3
R281 X_10K1%4 C320 C1u6.3X50402-HF

It's related to GS7133SO

3VDSW

0.204A

ATX_5VSB R587 10R1%4 3VDSW_CNTL C555 C1u6.3X50402-HF
U34 POK EN VIN NC VDD VOUT FB GND GND
R565 47K/4 3VDSW_EN
C548 10u6.3X6
C547 C10p50N0402 R564 31.6K1%4 3VDSW_FB
R563 10K1%4
3.333V 3VDSW
C553 X_10u6.3X6 C554 10u6.3X6 C429 0.1u16X4
GS7133SO_SOP8
Vout=0.8x(R1+R2)/R1
AVL:I31-3730S02-N62

3VDSW_EN Q83 2N7002 [22,43,44,55] VSB_ENABLE# C536 X_0.1u16X4
ATX_5VSB R555 47K/4 3VDSW_EN Q82 2N3904
SIO_3VA R547 0R/4 Q81 2N7002

2020/2/24
R693, Q103, R668, Q375 are stuffed by same as module circuit

3VSB cost down@3.3V

ATX_5VSB R344 10R/4 3VSB_CNTL C418 C1u6.3X50402-HF
U27 POK EN VIN NC VDD VOUT FB GND GND
3VSB_EN
5VDUAL C417 10u6.3X6
C443 C220p50X0402-RH
3VSB_FB
VFB=0.8
GS7133SO_SOP8
I31-7133S02-N03
PCH_VCCDRV
R386 30.9K1%4 R385 620K1%4 PCH_VCCDRV R384 10.2K1%4
C425 10u6.3X6 C426 0.1u16X4 EC21 CD100u16SO
一定要留下

2019/9/27
Q61 is changed to N-PK810BA by Ivy's comment
2019/12/17
Q61 is changed to SM4503NHKPC-TRG by Ivy's comment
VCC3
Q69
N-SM4503NHKPC-TRG_DFN5x6-8-HF
3.99A
3VSB

following formula: R2=(V_{OUT} /V_{REF} -1)*R1. Vout=Vref*(R2/R1+1)
=0.8*(30.9/10.2+1)
=3.2235v

Vout R2 FB R1 Coption Cout
Figure 3 Feedback Network
5VDUAL R371 47K/4 3VSB_EN
[22,43,44,55] VSB_ENABLE# Q63 PM514BA R372 100K/4 C430 C1u6.3X50402-HF

ATX_5VSB R353 47K/4 3VSB_EN Q64 2N3904
SIO_3VA R370 0R/4
3VDSW R369 X_0R/4 Q68 2N7002
Remove

for S5-G3 3VSB_EN ISSUE

2020/2/24
R4544 is unstuffed and R4543 is stuffed by same as module circuit
2020/2/24
R396, R4541 are deleted by unnecessary circuit

SIO_3VA

Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.04
=1.7*0.04
=0.068W

25mA+15mA=40mA

ATX_5VSB U33 GS7116S5-SOT23-5 VDD VOUT EN GND ADJ SIO_3VA
C549 1u16X4 R566 47K/4
C524 680p50X4 C528 10u6.3X6
3VA_FB R532 10K1%4 R531 3.16K1%4
[12,22,42] RTCRST# R621 X_0R/4 RTCRST#_D_SIO
C537 X_1u16X6

Vout = Vref*{(R661+R667)/R667}
= 0.8*{(10K+3.16K)/3.16K}
= 3.332V

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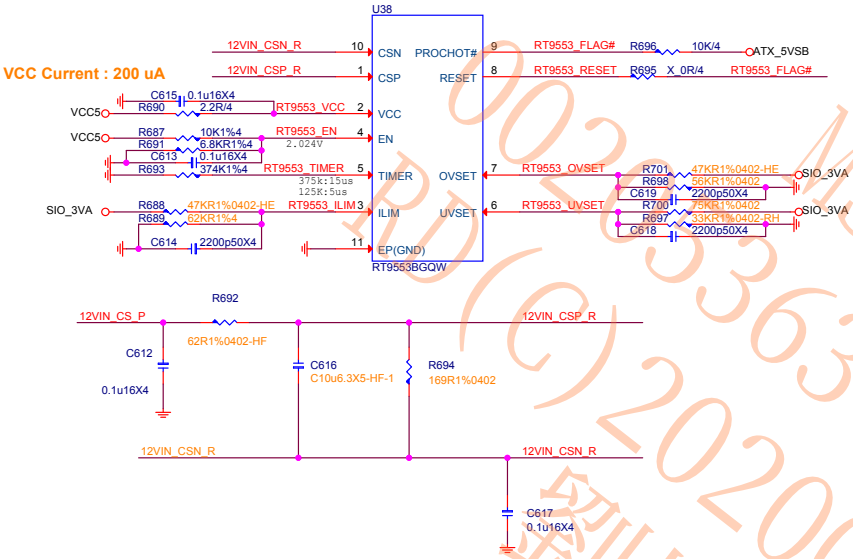
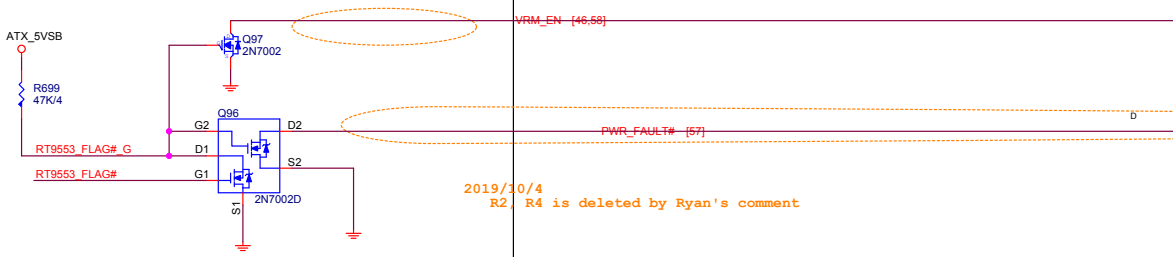
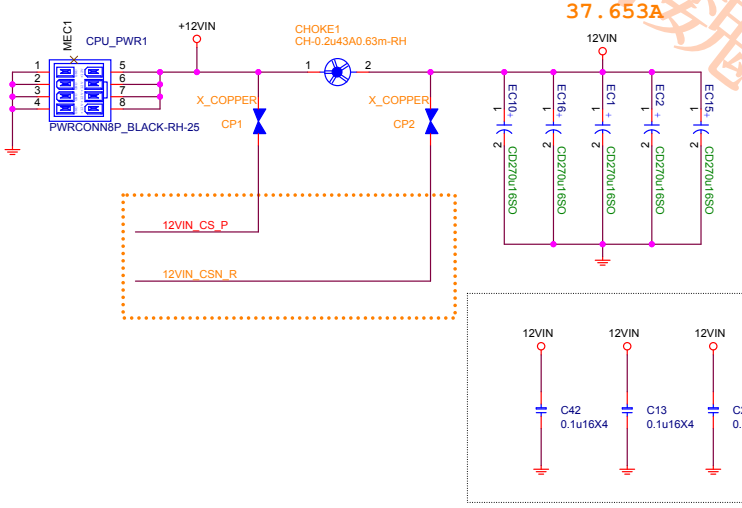
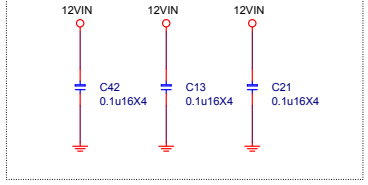
OCP: 45A For 10 core 210A Support





2019/10/4
R2, R4 is deleted by Ryan's comment





D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.52	> output Vcore
D	=	0.126667	

I o = Icore(max)*0.8			
I core(max)	=	210	> Vcore current
I avg.	=	168	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	12	phase
I ripple	=	4.656389	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	1	pcs.

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.52	> output Vcore
D	=	0.126667	

I o = Icore(max)*0.8			
I core(max)	=	35	> Vcore current
I avg.	=	28	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	1	phase
I ripple	=	9.312777	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	2	pcs.

D=Vout/Vin			
Vin	=	12	> input voltage
Vout	=	1.05	> output Vcore
D	=	0.0875	

I o = Icore(max)*0.8			
I core(max)	=	11.1	> Vcore current
I avg.	=	8.88	A

I ripple={ Io*√D*√(1-D)} / Phase			
Phase	=	1	phase
I ripple	=	2.509189	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	1	pcs.

2019/12/5
The footprint of CP3 & CP4 are changed from NC_93519 to NC_93519_1 by DFM request same as 7C59/7C60

MICRO-STAR INT'L CO.,LTD.
Title: 12VIN/CURRENT SENSE-RT9553
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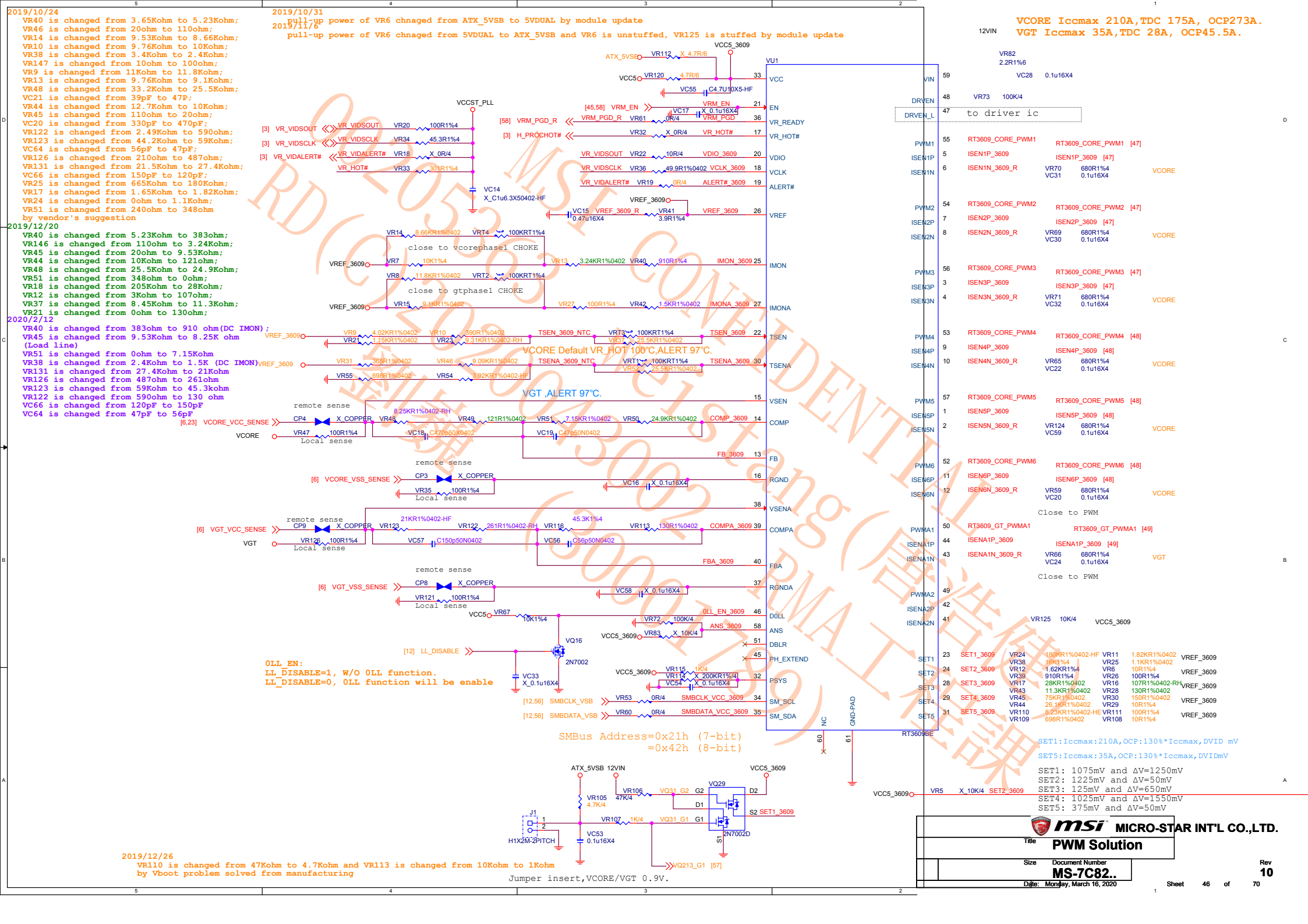
2019/10/24
VR40 is changed from 3.65Kohm to 5.23Kohm;
VR46 is changed from 20ohm to 110ohm;
VR14 is changed from 9.53Kohm to 8.66Kohm;
VR10 is changed from 9.76Kohm to 10Kohm;
VR38 is changed from 3.4Kohm to 2.4Kohm;
VR147 is changed from 10ohm to 100ohm;
VR9 is changed from 11Kohm to 11.8Kohm;
VR13 is changed from 9.76Kohm to 9.1Kohm;
VR48 is changed from 33.2Kohm to 25.5Kohm;
VC21 is changed from 39pF to 47P;
VR44 is changed from 12.7Kohm to 10Kohm;
VR45 is changed from 110ohm to 20ohm;
VC20 is changed from 330pF to 470pF;
VR122 is changed from 2.49Kohm to 590ohm;
VR123 is changed from 44.2Kohm to 59Kohm;
VC64 is changed from 56pF to 47pF;
VR126 is changed from 210ohm to 487ohm;
VR131 is changed from 21.5Kohm to 27.4Kohm;
VC66 is changed from 150pF to 120pF;
VR25 is changed from 665Kohm to 180Kohm;
VR17 is changed from 1.65Kohm to 1.82Kohm;
VR24 is changed from 0ohm to 1.1Kohm;
VR51 is changed from 240ohm to 348ohm
by vendor's suggestion

2019/12/20
VR40 is changed from 5.23Kohm to 383ohm;
VR146 is changed from 110ohm to 3.24Kohm;
VR45 is changed from 20ohm to 9.53Kohm;
VR44 is changed from 10Kohm to 121ohm;
VR48 is changed from 25.5Kohm to 24.9Kohm;
VR51 is changed from 348ohm to 0ohm;
VR18 is changed from 205Kohm to 28Kohm;
VR12 is changed from 3Kohm to 107ohm;
VR37 is changed from 8.45Kohm to 11.3Kohm;
VR21 is changed from 0ohm to 130ohm;

2020/2/12
VR40 is changed from 383ohm to 910 ohm(DC IMON);
VR45 is changed from 9.53Kohm to 8.25K ohm
(Load line)
VR51 is changed from 0ohm to 7.15Kohm
VR38 is changed from 2.4Kohm to 1.5K (DC IMON)
VR131 is changed from 27.4Kohm to 21Kohm
VR126 is changed from 487ohm to 261ohm
VR123 is changed from 59Kohm to 45.3kohm
VR122 is changed from 590ohm to 130 ohm
VC66 is changed from 120pF to 150pF
VC64 is changed from 47pF to 56pF

2019/10/31
pull-up power of VR6 chnaged from ATX_5VSB to 5VDUAL by module update
2019/11/6
pull-up power of VR6 chnaged from 5VDUAL to ATX_5VSB and VR6 is unstuffed, VR125 is stuffed by module update

VCORE Iccmax 210A,TDC 175A, OCP273A.
VGT Iccmax 35A,TDC 28A, OCP45.5A.



2019/12/26
VR110 is changed from 47Kohm to 4.7Kohm and VR113 is changed from 10Kohm to 1Kohm
by Vboot problem solved from manufacturing

MSI MICRO-STAR INT'L CO.,LTD.
Title: PWM Solution
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2019/10/15
VCHOKE12, VCHOKE11, VCHOKE10, VCHOKE9, VCHOKE13, VCHOKE14 are changed from 0.36uF to 0.33uF by Ivy's comment

2019/10/24
VR77, VR76, VR78 are changed from 2.15Kohm to 2.55Kohm by vendor's comment

2019/12/20
VR73, VR71, VR75 are changed from 2.1Kohm to 2.32Kohm

2020/2/12
VR77, VR76, VR78 are changed from 2.55Kohm to 2.05K ohm by AC IMON fine tune

2019/11/18
CP24, CP26, CP25, CP23, CP20, CP22, CP21, CP19, CP28, CP30, CP27, CP29 are deleted by Ivy's comment in 2019/11/7

2019/9/27
VQ22, VQ23, VQ19, VQ18, VQ26, VQ27 are changed to N-PK806BA; VQ21, VQ24, VQ17, VQ20, VQ28, VQ25 are changed to N-PK810BA by Ivy's comment

2019/12/17
VQ22, VQ23, VQ19, VQ18, VQ26, VQ27 are changed to SM4337NSKPC-TRG; VQ21, VQ24, VQ17, VQ20, VQ28, VQ25 are changed to SM4503NHKPC-TRG by Ivy's comment

Title	VCORE MOS-PHASE 1~3
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MICRO-STAR INT'L CO.,LTD.

2019/10/15
VCHOKE5, VCHOKE4, VCHOKE2, VCHOKE3, VCHOKE7, VCHOKE6 are changed from 0.36uF to 0.33uF by Ivy's comment

2019/10/24
VR58, VR127, VR54 are changed from 2.15Kohm to 2.55Kohm by vendor's comment

2019/12/20
VR59, VR128, VR55 are changed from 2.1Kohm to 2.32Kohm

2020/2/12
VR58 , VR127 , VR54 are changed from 2.55Kohm to 2.05K ohm by AC IMON fine tune

2019/11/21
VEC21, VEC22 are added by 7C75's result

2019/12/20
VEC16, VEC21 are unstuffed by 7C81's result

2019/9/27
VQ3, VQ4, VQ1, VQ2, VQ5, VQ6 are changed to N-PK806BA; VQ9, VQ13, VQ8, VQ12, VQ10, VQ14 are changed to N-PK810BA by Ivy's comment

2019/12/17
VQ3, VQ4, VQ1, VQ2, VQ5, VQ6 are changed to SM4337NSKPC-TRG; VQ9, VQ13, VQ8, VQ12, VQ10, VQ14 are changed to SM4503NHKPC-TRG by Ivy's comment

2019/11/18
CP6, CP42, CP14, CP15, CP39, CP40, CP12, CP13,CP7, CP41, CP16, CP17 are deleted by Ivy's comment in 2019/11/7

2020/3/10
VEC16, VEC21 are deleted by PCB rev1.0

Title	VCORE MOS-PHASE 4~6
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MICRO-STAR INT'L CO.,LTD.

2019/10/15
VCHOKE8 is changed from 0.2uFuF to 0.33uF by Ivy's comment

2020/2/12
VEC7 is unstuffed by Transient's result

2020/3/6
VEC7 is deleted by PCB rev1.0

2019/10/23
VEC20 is added by VCHOKE8 change to 0.33uF from vendor's suggestion

2019/9/27
VQ7 is changed to N-PK806BA and VQ15, VQ11 are changed to N-PK810BA by Ivy's comment

2019/12/17
VQ7 is changed to SM4337NSKPC-TRG and VQ15, VQ11 are changed to SM4503NHKPC-TRG by Ivy's comment

2019/10/24
VR64 is changed from 1.74Kohm to 2.55Kohm and VR61 is changed from 1.43Kohm to 2.1Kohm by vendor's suggestion

2019/11/18
CP9, CP18 are deleted by Ivy's comment in 2019/11/7

12VIN
VR93
2.2R/8
VC45
2.2u16X6
RT9624_GT_VCC1
VU2
VCC
PWM
NC
GND
GND-PAD
BOOT
UGATE
PHASE
LGATE
RT9624_GT_BOOTA1
RT9624_GT_UGA1
RT9624_GT_PHA1
RT9624_GT_LGA1
[46] RT3609_GT_PWMA1
RT9624F

Close to high MOS.
VC9
1u16X6
VC2
C10u25X8
VEC1
CD270u16SD
VC1
C10u25X8
VQ1
VQ9
VQ8
RT9624_GT_UGA1
RT9624_GT_BOOTA1
VR101
2.2R1%6
RT9624_GT_BOOTA1_R
VR97
X_10K/4
VC52
0.1u25X4
RT9624_GT_PHA1
RT9624_GT_LGA1
N-SM4337NSKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF
N-SM4503NHKPC-TRG_DFN5x6-8-HF

VEC4 CD560u6.3SO
VEC3 CD560u6.3SO
VEC2 CD560u6.3SO

VCHOKE1
CH-0.33u45A0.71mS-HF
VGT

VR1
2.2R1%8
VC10
1000p50X/4
VR75
2.55KR1%0402
ISENA1+_R
Close to IC
VR74
2.1KR1%0402-RH
VC29
0.1u16X4
VR68
X_0R/4
[46] ISENA1P_3609
VGT

MICRO-STAR INT'L CO.,LTD.
Title: VGT MOS-PHASE 1~2
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SA Power:1.05V,11.1A

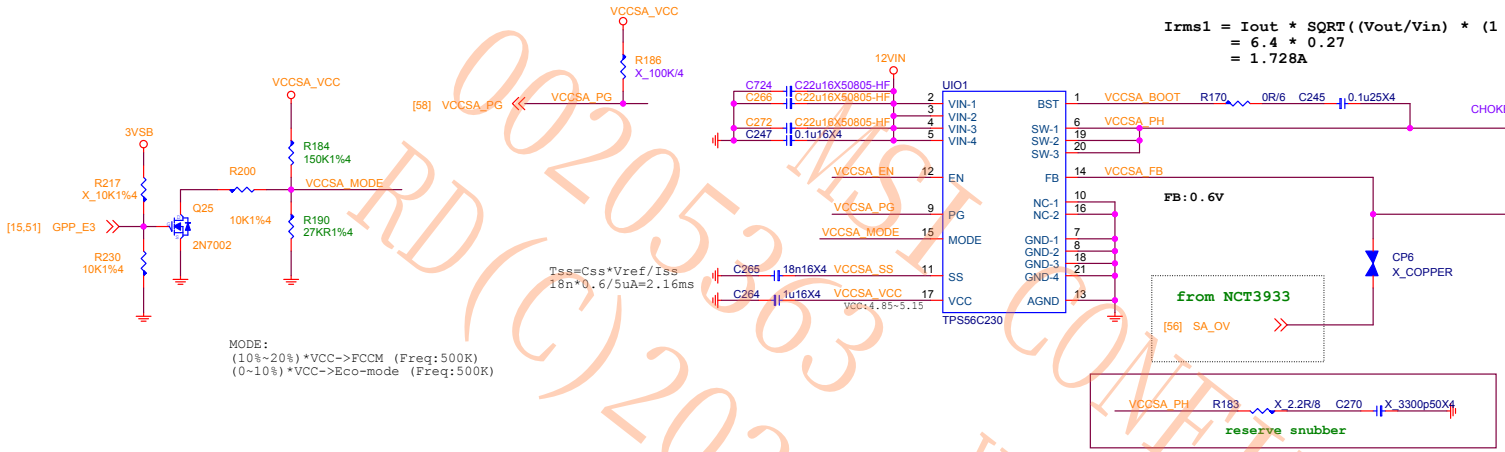
OCP 13-18A

2020/2/21
R193 is unstuffed by same as 7C71

2019/11/28
C2771 is deleted and C2768, C2770 are changed from 10uF to 22uF by lack of layout space

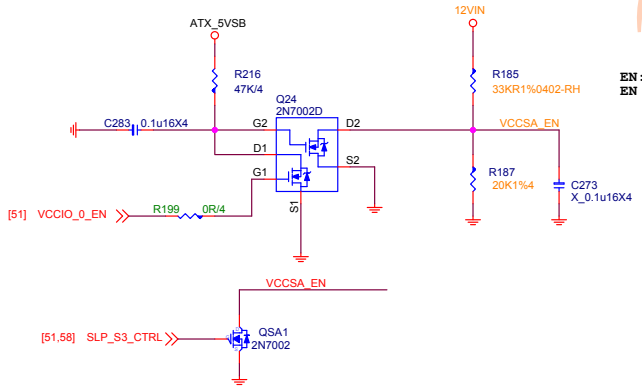
C667 0.1u16X4 | C663 22u6.3X6 | C668 22u6.3X6 | C723 22u6.3X6

Irms1 = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 6.4 * 0.27
= 1.728A

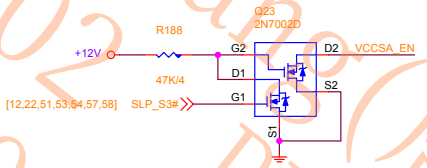


MODE:
(10%~20%)*VCC->FCCM (Freq:500K)
(0~10%)*VCC->Eco-mode (Freq:500K)

2020/3/12
CHOKE6 is changed from L04-68B7350-T15 to OL4-7C71008-T15 and C723, C724 are added by fine tune result



EN:VIH1.2~1.4V
EN pin Maximum:5.5V



2019/10/30
R4644, Q451 are added by avoiding bounce when S0 to G3 same as 300 series

2020/2/21
R4644 is changed to pull-up to +12V from 12VIN by same as 300 series

VCCSA

CHOKE6 CH-0.47u17.5A3.85mS

R196 10R1%4

R197 1K/1%4 | R189 0R/4 | VSA_SENSE [6,23]

C271 X_100p50N4

R198 1.33KR1%0402

$$V_{OUT} = 0.6 \times (1 + \frac{R_{UPPER}}{R_{LOWER}})$$

Vout = 0.6* (1 + Rupper/Rlower)
= 0.6 * (1 + 1/1.33)
= 1.051v

MICRO-STAR INT'L CO.,LTD.

Title: CPU VCCSA

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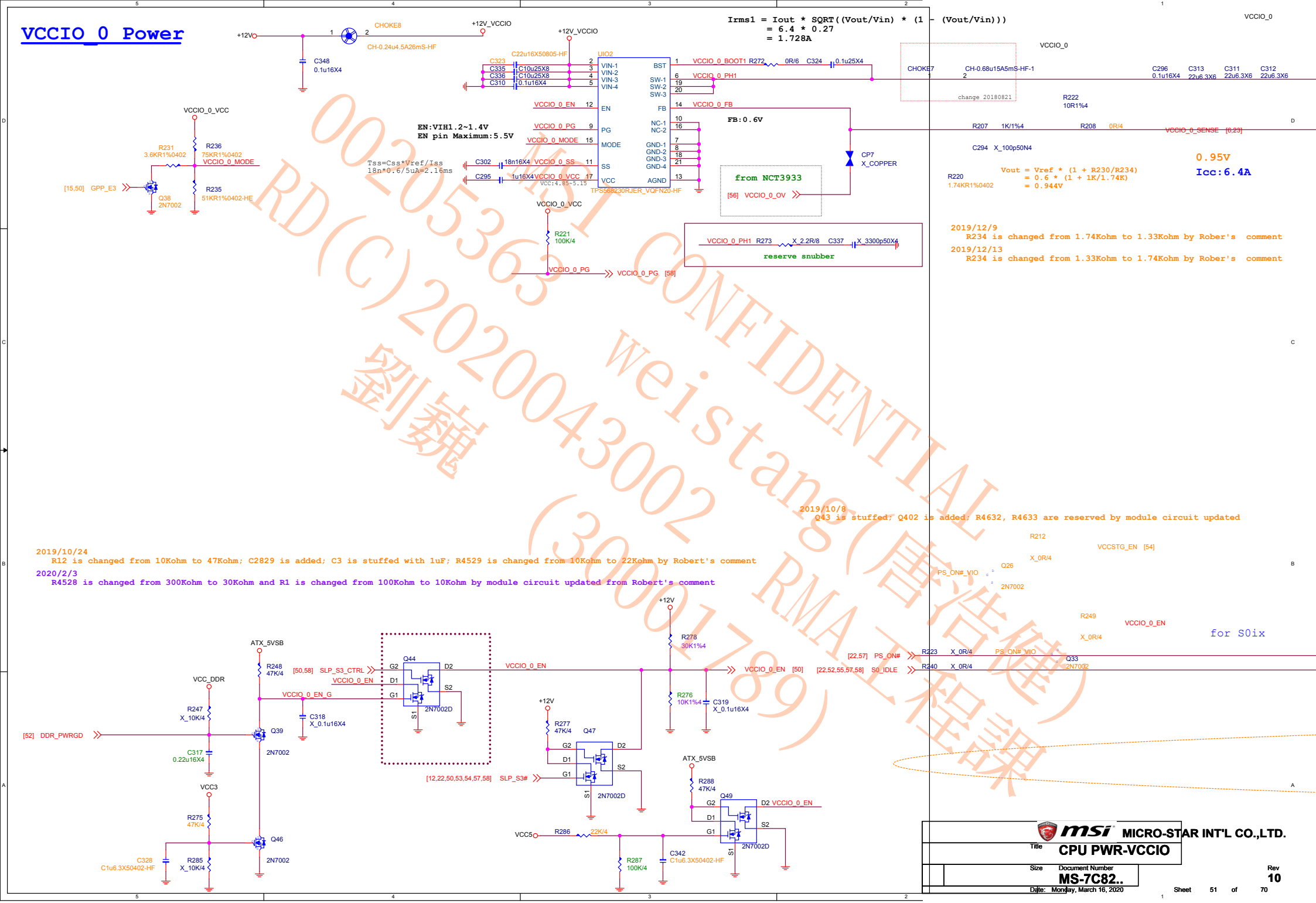
VCCIO_0 Power



Title	CPU PWR-VCCIO
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MICRO-STAR INT'L CO.,LTD.

DDR4 Power:1.2V,13.67A

3.7A For CPU
9.1A For 4DIMM
0.7A For DDR VTT
0.17A For VCCPLL_OC

Iout = 3.7+9.1+0.7+0.17=13.67A

Iocp=Rocset*Iocset/Rlgds(on)
=7.32K*10u/4.6m
=15.913A
Iocp=Rocset*Iocset/Rlgds(on)
=7.32K*10u/3m
=24.4A

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 16A		3	4.6	mΩ
		V_{GS} = 10V, I_D = 20A		2.1	3.3	

Table 1. States of EN_MODE Control Circuit

Q1	Q2	V_{EN_MODE} (V)	Mode
ON	OFF	2.37 2.1~2.7v	DEM
OFF	OFF	4.5 4.3~5v	FCCM
OFF	ON	0 <0.4v	Shutdown

20190910
R4590 is added and R4589 is reserved by module updated

Default:FCCM
L:FCCM
H:DEM

2020/2/25
GPIO32 is changed to GPIO31 by same as module circuit

need confirm select

2019/10/2
R4618 is added by same as 7C70

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 13.67 * SQRT(0.1824)
= 5.882A

CHOKE12, Idc=4.8A, Isat=6.7A

CHOKE2, Idc=16.5A, Isat=18A

$$V_{OUT} = \left[V_{REFOUT} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)\right] + \frac{\Delta V_{OUT}}{2}$$

Vout=Vrefout*(1+R1/R2)
=0.794x(1+1/1.96)
=1.1991v

ΔIL=(Vin-Vout)/(L*Fsw) * Vout/Vin
=(5-1.2)/(0.82u*300K)*(1.2/5)
=3.7073A

$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

Rocset = [(1.3* Iout) - (0.5 * ΔIL)]*Rds(on)/ Iocset
= [(1.3*13.67) -(0.5*3.7073)]* 3m / 10u
= 4.7752Kohm

Rocset = [(1.3*Iout) - (0.5 * ΔIL)]*Rds(on)/ Iocset
= ((1.3*13.67) - (0.5*3.7073)]* 4.6m / 10u
= 7.3219Kohm

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1.2) / (300K*0.2*13.67) * (1.2/5)
= 1.1119uH

L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1.2) / (300K*0.4*13.67) * (1.2/5)
= 0.55596uH

So L range = 0.55596uH ~ 1.1119uH

2019/9/27
Q18 is changed to N-PK806BA and Q21 is changed to N-PK810BA by Ivy's comment

2019/12/17
Q18 is changed to SM4337NSKPC-TRG and Q21 is changed to SM4503NHKPC-TRG by Ivy's comment

Title	DDR4 Power
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MICRO-STAR INT'L CO.,LTD.

VPP2.5V Power:2.5V,6A(for dimm LED)

IC OCP:7.6A(6.6A~8.6A)

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 6 * 0.5
     = 3A
```

20190910
CHOKE15 is added by module updated

L04-01074U0-T15

U16 TPS566235

Vout = Vref*{(R421+R1180)/R1180}
= 0.6*{(1K+0.316K)/0.316K}
= 2.499V

ENABLE HIGH:1.22~1.42V

need confirm select

try to chnage 2Kohm

try to chnage 3Kohm

try to mount 0.1uF

reserve snubber

Vmode(VPP25_MODE)	0~0.3V	0.3~1.2V	>1.2V
Rmode	0R	100K~150K	To VCC(recommend) or R>400K
Operating Mode	Eco-Mode	Out-Of-Audio	FCCM

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

0.3*4=1.2A

NCT3103S co-lay NCT3102S/UP0109

MICRO-STAR INT'L CO.,LTD.

Title: DDR PWR VPP25/VTT

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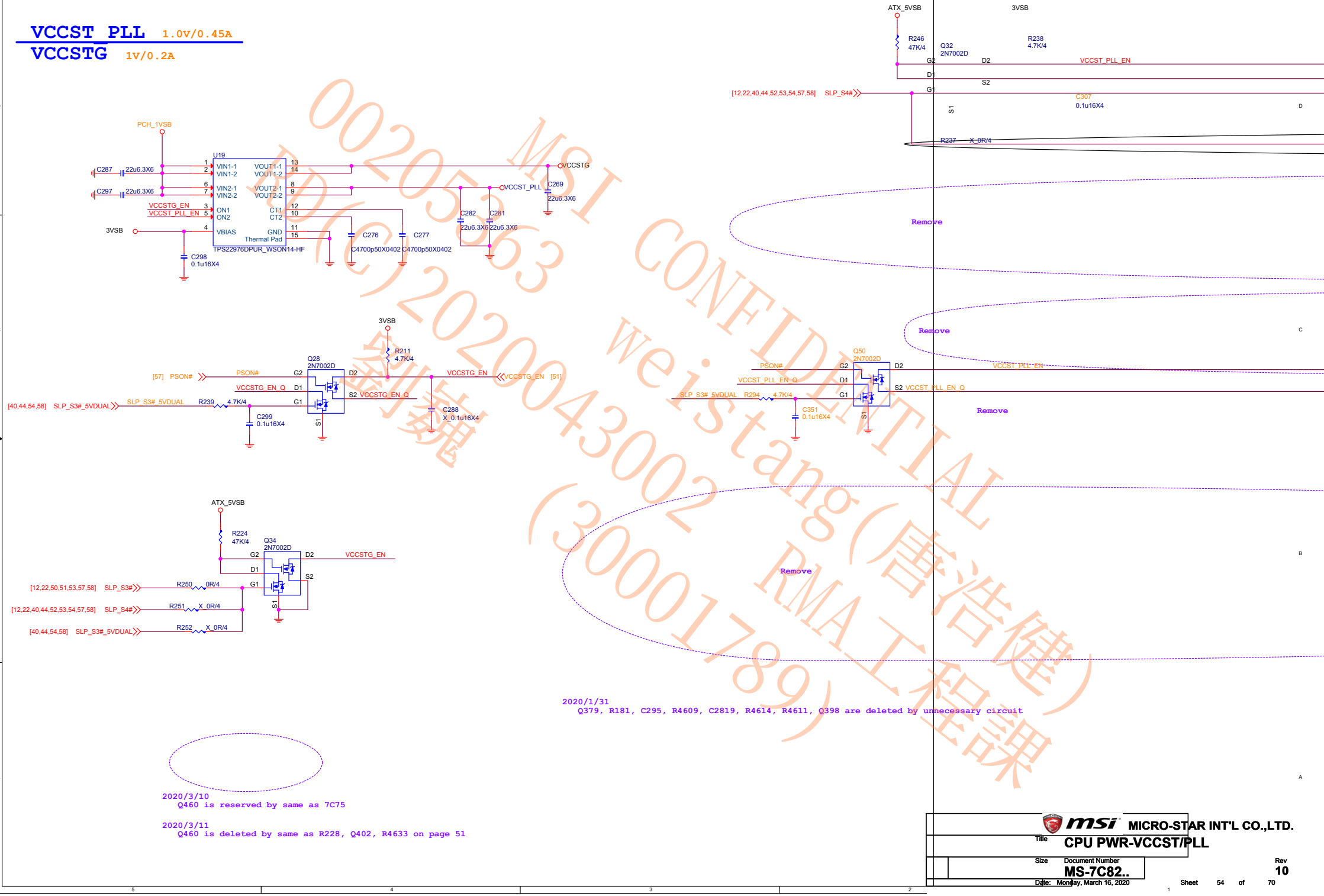
VCCST PLL 1.0V/0.45A
VCCSTG 1V/0.2A



2020/1/31
Q379, R181, C295, R4609, C2819, R4614, R4611, Q398 are deleted by unnecessary circuit

2020/3/10
Q460 is reserved by same as 7C75

2020/3/11
Q460 is deleted by same as R228, Q402, R4633 on page 51

MICRO-STAR INT'L CO.,LTD.

Title: CPU PWR-VCCST/PLL

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Date: Monday, March 16, 2020 Sheet 54 of 70

PCH_1P05_VSB Power:1.0V,11.258A

Iout = 11.258A

Iocp=Rocset*Iocset/Rlgds(on)
=5.76K*10u/4.6m
=12.5217A
Iocp=Rocset*Iocset/Rlgds(on)
=5.76K*10u/3m
=19.2A

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 4.5V, I_S = 16A		3	4.6	mΩ
		V_{GS} = 10V, I_S = 20A		2.1	3.3	

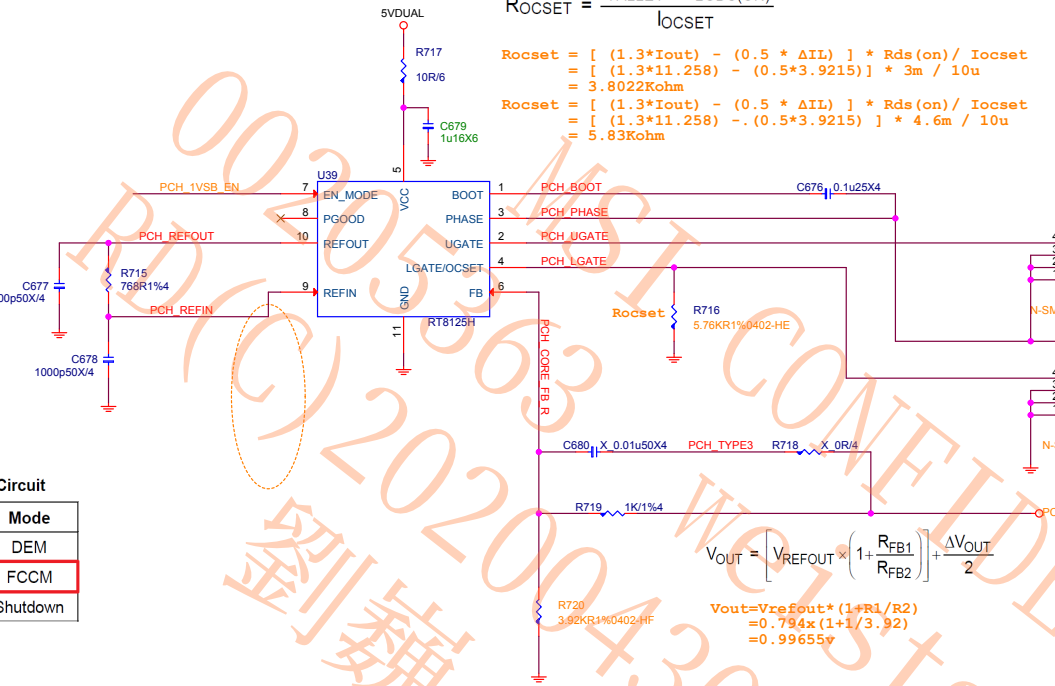
ΔIL=(Vin-Vout)/(L*Fsw) * Vout/Vin
=(5-1)/(0.68u*300K)*(1/5)
=3.9215A

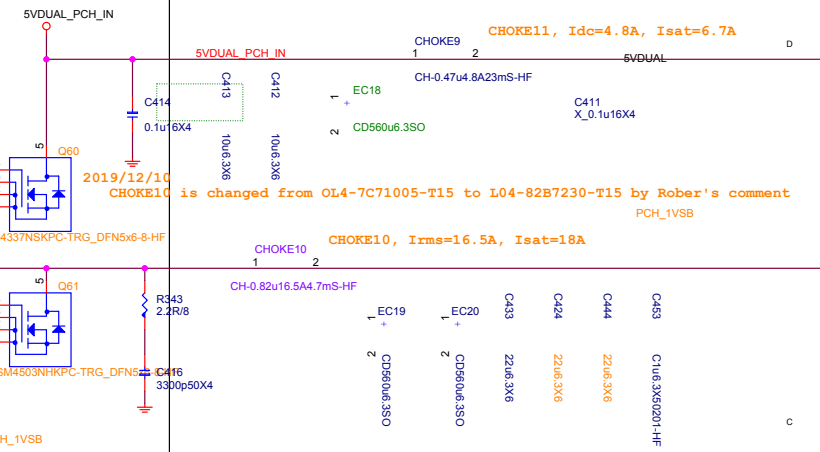
$$R_{OCSET} = \frac{I_{VALLEY} \times R_{LGDS(ON)}}{I_{OCSET}}$$

Rocset = [(1.3*Iout) - (0.5 * ΔIL)] * Rds(on)/ Iocset
= [(1.3*11.258) - (0.5*3.9215)] * 3m / 10u
= 3.8022Kohm
Rocset = [(1.3*Iout) - (0.5 * ΔIL)] * Rds(on)/ Iocset
= [(1.3*11.258) -.(0.5*3.9215)] * 4.6m / 10u
= 5.83Kohm

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
= 11.258 * 0.4
= 4.5032A





2020/1/31
The footprint of CHOKE10 is changed to CHK_S2_6_6X7_2_1 by properties_check

$$V_{OUT} = \left[V_{REFOUT} \times \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)\right] + \frac{\Delta V_{OUT}}{2}$$

Vout=Vrefout*(1+R1/R2)
=0.794x(1+1/3.92)
=0.99655v

$$L_{(MIN)} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_Full\ Load}} \times \frac{V_{OUT}}{V_{IN}}$$

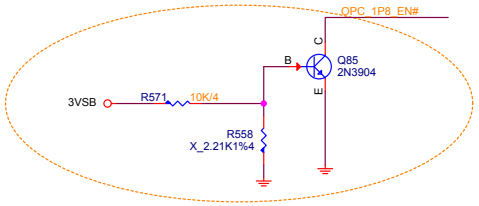
L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1) / (300K*0.2*11.258) * (1/5)
= 1.1843uH
L = (Vin - Vout) / (Fsw * K* Iout_full load) * (Vout/Vin)
= (5 - 1) / (300K*0.4*11.258) * (1/5)
= 0.5921uH

So L range = 0.5921uH ~ 1.1843uH

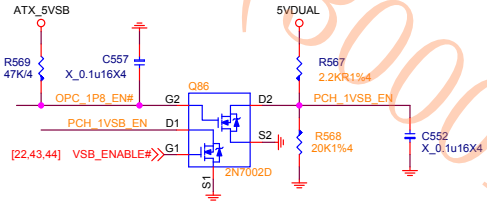
Table 1. States of EN_MODE Control Circuit

Q1	Q2	V_{EN_MODE} (V)	Mode
ON	OFF	2.37 2.1~2.7v	DEM
OFF	OFF	4.5 4.3~5v	FCCM
OFF	ON	0 <0.4v	Shutdown

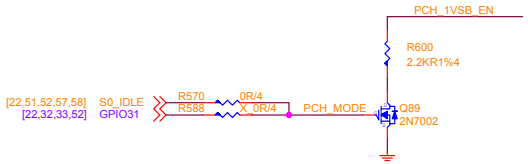
2019/12/3
R701 is stuffed and R700 is deleted by Rober's comment



It needs to confirm the timing for OPC_1P8_EN#



2019/10/22
Q99, Q100 are combined to Q99 by Ivy's comment



20190910
R4593, Q391, R4591 are added and R4592 is reserved by module updated

2020/2/25
GPIO32 is changed to GPIO31 by same as module circuit

2019/9/27
Q96 is changed to N-PK806BA and Q87 is changed to N-PK810BA by Ivy's comment

2019/12/17
Q96 is changed to SM4337NSKPC-TRG and Q87 is changed to SM4503NHKPC-TRG by Ivy's comment

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~~1P8_VSB Power:1.8V 0.16A~~

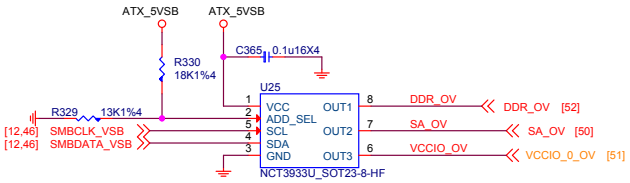
Power Loss=(Vin-Vou)*Iout
=(3.3-1.8)*0.21
=1.5*0.21
=0.315W

2019/11/27
C572, R589, Q80, C557, C556, U44, R578, C558, R598, R600, C572, C560 are unstuffed by LPC seleted

2019/12/3
C572, R589, Q80, C557, C556, U44, R578, C558, R598, R600, C572, C560, C561, C571 are deleted by Robert's comment

UPI VOLTAGE CONSOLE

0x26:RH=18K,RL=13K



MICRO-STAR INT'L CO.,LTD.

Title: PCH 1P8V -GS7133/OV

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ATX POWER CONNECTOR

JPWR1

ATX_PWR1

PWRCONN24P

0306: Follow Check List For D0G-0505

0313: Change to PANDA Cap.

上1K是解決新享200W(huntkey)power supply的問題,加1K是為了不讓ATX_5VSB空載而產生震盪

2019/10/15
C2823, C2824 are added by Eric's comment

FRONT PANNEL

JFP1

JFP2

H2X5[10]M_BLACK

H1X4M_BLACK

2020/2/13
RN9 is changed from R31-0151012-W08 to R31-0151042-W08 by Robert's comment

Thunderbolt card support

JTBT1

BH1X5_BLACK-RH-1

JRTD3

BH1X3_BLACK-RH-3

CRB use GPP_F2

CRB use GPP_H15
need confirm

default use PCIE Slot Wake#

Front Panel LED

2019/10/23
R740 was stuffed and R732 was unstffed because ESIO solved

Reserve pull high to 5VDIMM if PM don't want PLED light in deep mode.

SIO ver. LAA
Push pull pin, no need to stuff resisters.

CMKT3904_SOT363-6

Title	ATX Connector/F_Panel		
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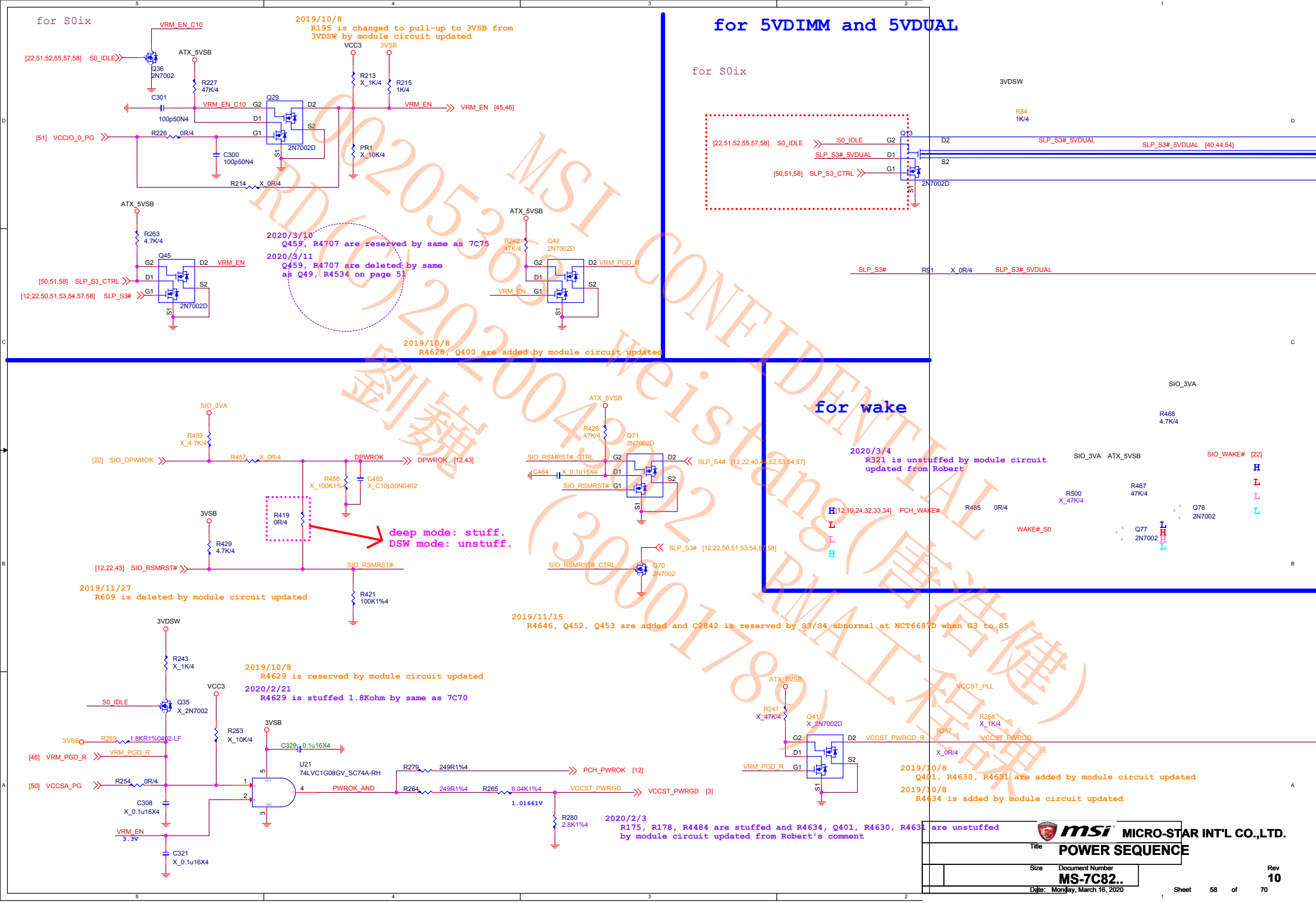
MSI MICRO-STAR INT'L CO.,LTD.


for S0ix
2019/10/8
R195 is changed to pull-up to 3VSB from 3VSDW by module circuit updated
for 5VDIMM and 5VDUAL
for S0ix
2020/3/10
Q459, R4707 are reserved by same as 7C75
2020/3/11
Q459, R4707 are deleted by same as Q49, R4534 on page 51
2019/10/8
R4628, Q400 are added by module circuit updated
for wake
2020/3/4
R321 is unstuffed by module circuit updated from Robert
deep mode: stuff.
DSW mode: unstuff.
2019/11/27
R609 is deleted by module circuit updated
2019/11/15
R4646, Q452, Q453 are added and C2842 is reserved by S3/S4 abnormal at NCT6687D when G3 to S5
2019/10/8
R4629 is reserved by module circuit updated
2020/2/21
R4629 is stuffed 1.8Kohm by same as 7C70
2019/10/8
Q401, R4630, R4631 are added by module circuit updated
2019/10/8
R4634 is added by module circuit updated
2020/2/3
R175, R178, R4484 are stuffed and R4634, Q401, R4630, R4631 are unstuffed by module circuit updated from Robert's comment
MICRO-STAR INT'L CO.,LTD.
POWER SEQUENCE
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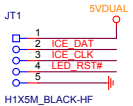
IF no JPWRLED1 & JPIPE_LED spec

MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.

JF1 for Factory test

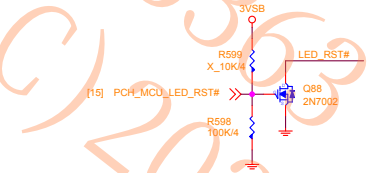
Check with LED model spec

JT1 for FW update



2019/11/22
R4664, Q455 are added by module curcuit updated from Robert's comment

2019/11/27
R4664, Q455 are deleted by module curcuit updated from Ryan's comment



2019/11/19
R4652, R4651, Q454 are added by MCU controlled

2019/11/25
R4652 is unstuffed and R4669 is added by Robert's comment

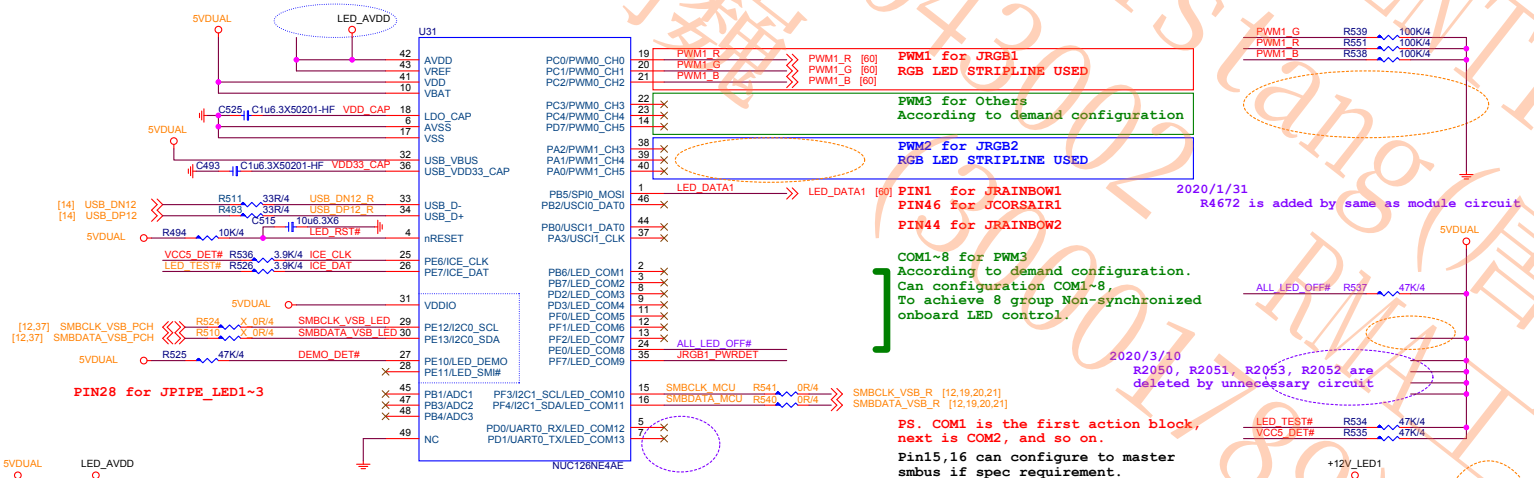
2019/11/25
R4651 is deleted and Q454 is changed from dual n-MOS to single n-MOS by Ryan's comment

LED SWITCH

2019/10/28
LED_SW1 , R4596, R4597, D103, C2779, R4599, R4598, Q393 are deleted by PM spec updated

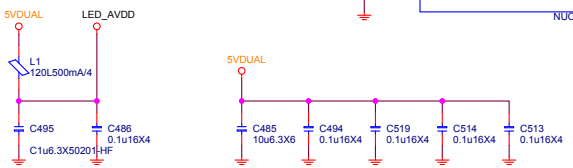
48 PIN LED MCU

If you use ADC function,need to separate VREF from AVDD and 4_09VREF stuff for VREF.

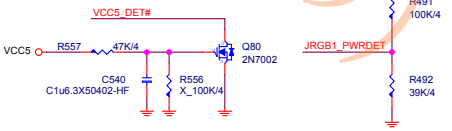


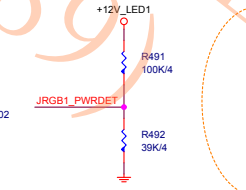
2020/1/31
R4672 is added by same as module circuit

2020/3/10
R2050, R2051, R2053, R2052 are deleted by unnecessary circuit



C1822 & C1823 near AVDD Pin. C1820 & C1821 near VDD Pin.
C1824 near VBAT Pin.
C1827 & C1828 near VDDIO & USB_VBUS Pin.





Control	Net Name	PWM USE
PCH	LED_DATA4	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_DATA1	No Use
JRAINBOW2	LED_DATA3	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~12	PWM2

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Title: LED MCU Control

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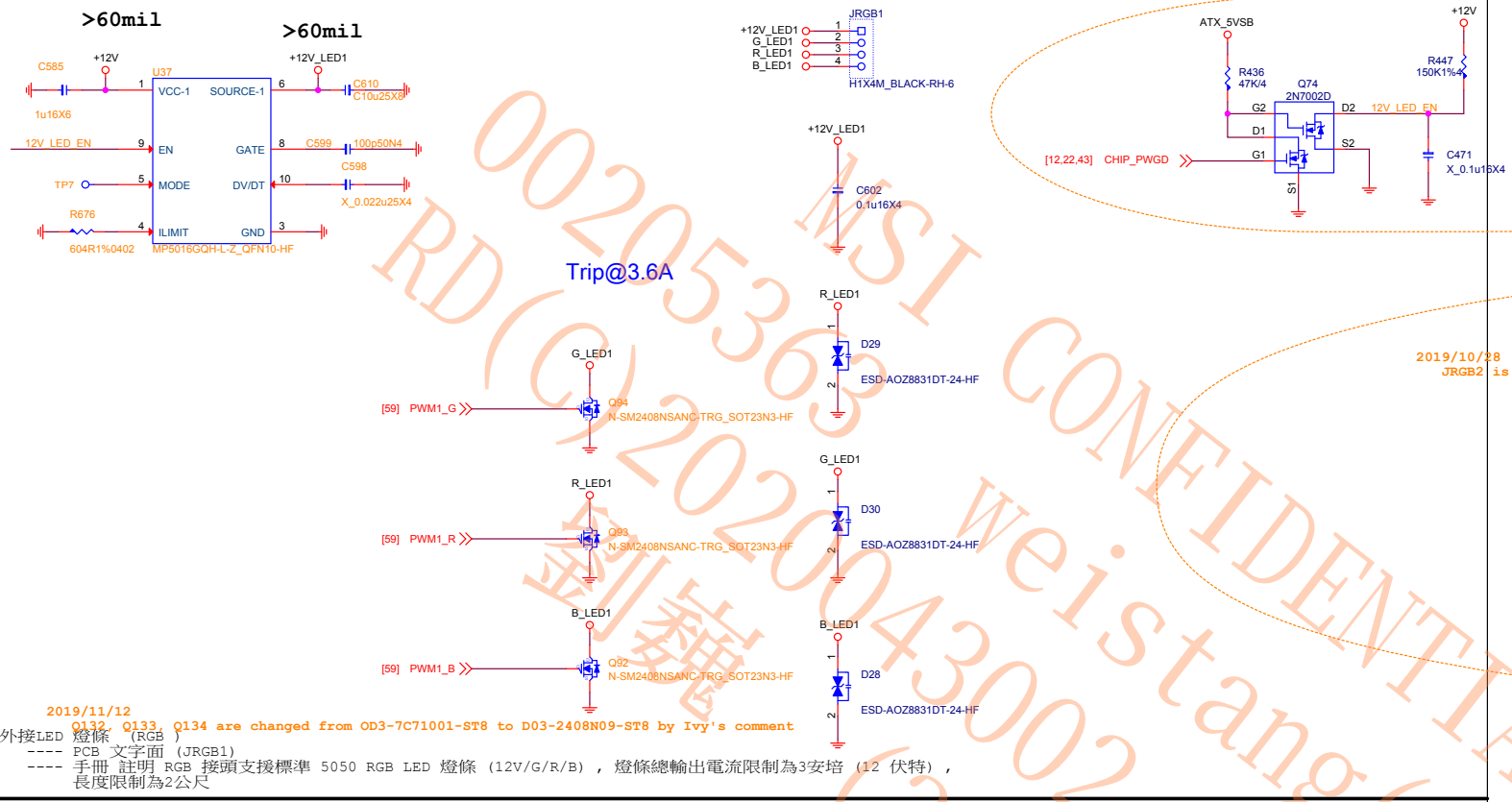
JRGB1

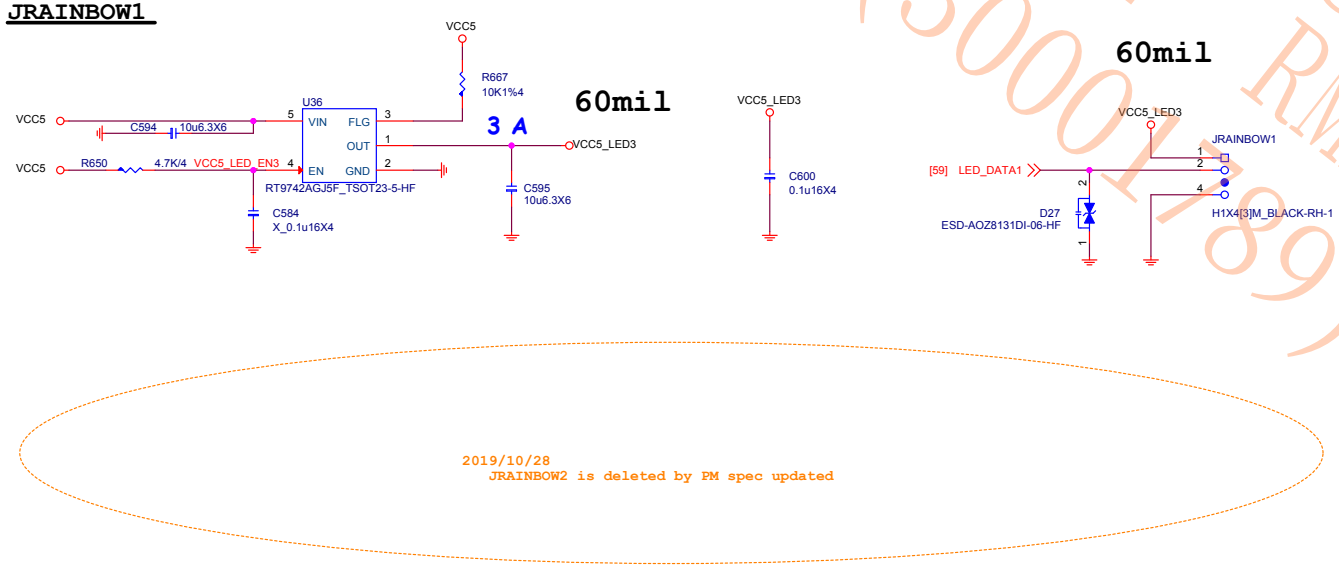


2019/10/28
JRGB2 is deleted by PM spec updated

2019/11/12
Q132, Q133, Q134 are changed from OD3-7C71001-ST8 to D03-2408N09-ST8 by Ivy's comment

外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B)，燈條總輸出電流限制為3安培 (12 伏特)，
長度限制為2公尺

JRAINBOW1



2019/10/28
JRAINBOW2 is deleted by PM spec updated

MICRO-STAR INT'L CO.,LTD.

Title: LED PIN HEADER

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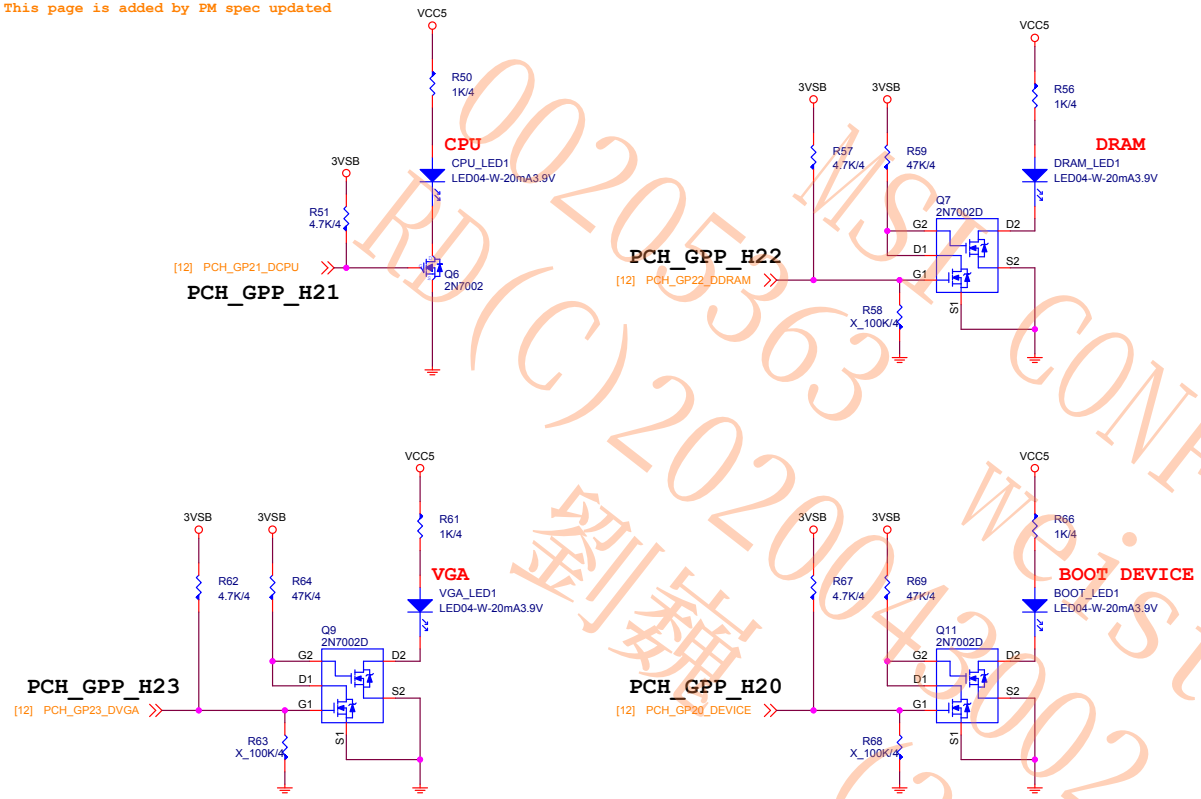
EZ DEBUG LED

2019/10/3
This page is added by PM spec updated



LED
紅 : D0C-040P100-H91
AVL: D0C-040S500-E07

LED
白 : D0C-040T200-H91
AVL: D0C-040S200-E07

GPIO / LED	GPP_H21	GPP_H22	GPP_H23	GPP_H20
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

關機斷電狀態下，4個LED先維持default全暗，開機通電後：
1. 首先進行CPU checkCPU LED 亮，check PASS後則CPU LED滅掉。
2. 接著依序進行Memory /memory LED亮check PASS後則memory LED滅掉。
3. VGA的check/VGA LED亮，check PASS後則VGA LED滅掉。
4. BOOT DEVICE的check/BOOT LED亮，check PASS後則BOOT LED滅掉。
5. 因此最後正常順利開機後，四個LED燈都是滅掉的。
（系統重啟或其他原因造成系統重開機，則LED仍按上述行為動作）

MICRO-STAR INT'L CO.,LTD.
Title: EZ DEBUG LED
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EMI CAP

MICRO-STAR INT'L CO.,LTD.

Title: X

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BAT1_X1

BAT-BCR2032P-RH

CPU_H1

CPU 鐵座

AZIF0208-P001C

BIOS_LA1

AMI

AMI

HDMI_LA1

HDMI_LABEL

CFOS_LA1

Y02-MU00170-CFO

PCB1

7C82_10

Main:PD0-07C8210-G37
AVL: PD0-07C8210-E48

2019/10/17
BAT1_X1 is changed to D06-0106501-K26 by PM spec updated

2019/10/17
HDMI_LA1 is added by PM spec updated

2019/11/8
BAT1_X1 is changed to D06-0100101-K26 by PM spec updated

2020/3/16
PCB1 is changed from PD0-07C820A-G37
to PD0-07C8210-G37 by G/O result

Optical Fiducial Marks-120

FM3 FM2 FM5 FM8

X_FM X_FM X_FM X_FM

FM1 FM4 FM6 FM7

X_FM X_FM X_FM X_FM

Simulation

SIM2 SIM1

SIM4 SIM3

X_PIN1*2 X_PIN1*2

Mounting Holes

MH1 MH3 MH5

MH2 MH7 MH4

MH6 MH8

X_MH001

CA34 0.1u16X4 CA29 0.1u16X4

C415 X_100p50N4

Audio layout guide

1.0 option - WiFi

MOS-N-HS-WIFI1

X_HS-0506730-RH

MOS-W-HS-WIFI1

X_HS-0506740-RH

PCH_HS_WIFI1

X_HS-0410510-RH

M2_1-COVER-WIFI1

X_0P10B08433

IO-SHIELDING-WIFI1

X_CSCZ-SHIELD252

MK_LA_WIFI1

X_G51-M1SPP96-Q13

2019/11/18
MK_LA1, MK_LA1_1 are added by PM spec updated

2019/11/18
MK_LA1, MK_LA1_1 are unstuffed by PM's comment

2020/3/12
MOS-N-HS-WIFI1 is changed to E31-0506730-A87;
MOS-W-HS-WIFI1 is changed to E31-0506740-A87;
PCH-HS-WIFI1 is changed to E31-0410510-A87;
M2_1-COVER-WIFI is added for E31-0002670-A87;
IO-SHIELDING-WIFI1 is added for E21-7C82010-A91
by PM request

2020/3/17
MK_LA_WIFI1 is changed to G51-M1SPP96-Q13 by
PM request

1.0 option - None WiFi

MEC1 MOS-N-HS1 MEC1 MOS-W-HS1 MEC1 PCH-HS1

HS-0506690-RH MEC2 HS-0506700-RH MEC2 HS-0410490-RH MEC2

M2_1-COVER1

0P10B08429

IO-SHIELDING1

CSCZ-SHIELD300

MK_LA1

G51-M1SPP77-Q13

2020/2/26
PCH-HS1 is changed from
OE3-7C82002-A87 to
OE3-7C82004-A87 by PM request

2020/3/12
MOS-N-HS1 is changed to E31-0506690-A87;
MOS-W-HS1 is changed to E31-0506700-A87;
PCH-HS1 is changed to E31-0410490-A87;
M2_1-COVER1 is added for E31-0002610-A87
by PM request

2020/3/13
MK_LA1 is changed to G51-M1SPP77-Q13 by
PM request

2020/3/16
IO-SHIELDING1 is added for E21-7C82020-A91
by PM request

MICRO-STAR INT'L CO.,LTD.

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