MS-7C81

ATX
Ver: 10

CML Platform

CPU:

Comet lake S 65W

System Chipset:

B460 PCH_V

Onboard Chip:

HD Audio Codec:ALC1200
LAN-Intel RTL8125B
SIO:NTC6687
Flash ROM: SPI 128 MB X1

VGA Output:

HDMI Port
DP Port

Main Memory:

*DDRIV (2666MHz) * 4 (Dual Channel)*

PWM:

IMVP8 -RT3609BE

ACPI:

LDO

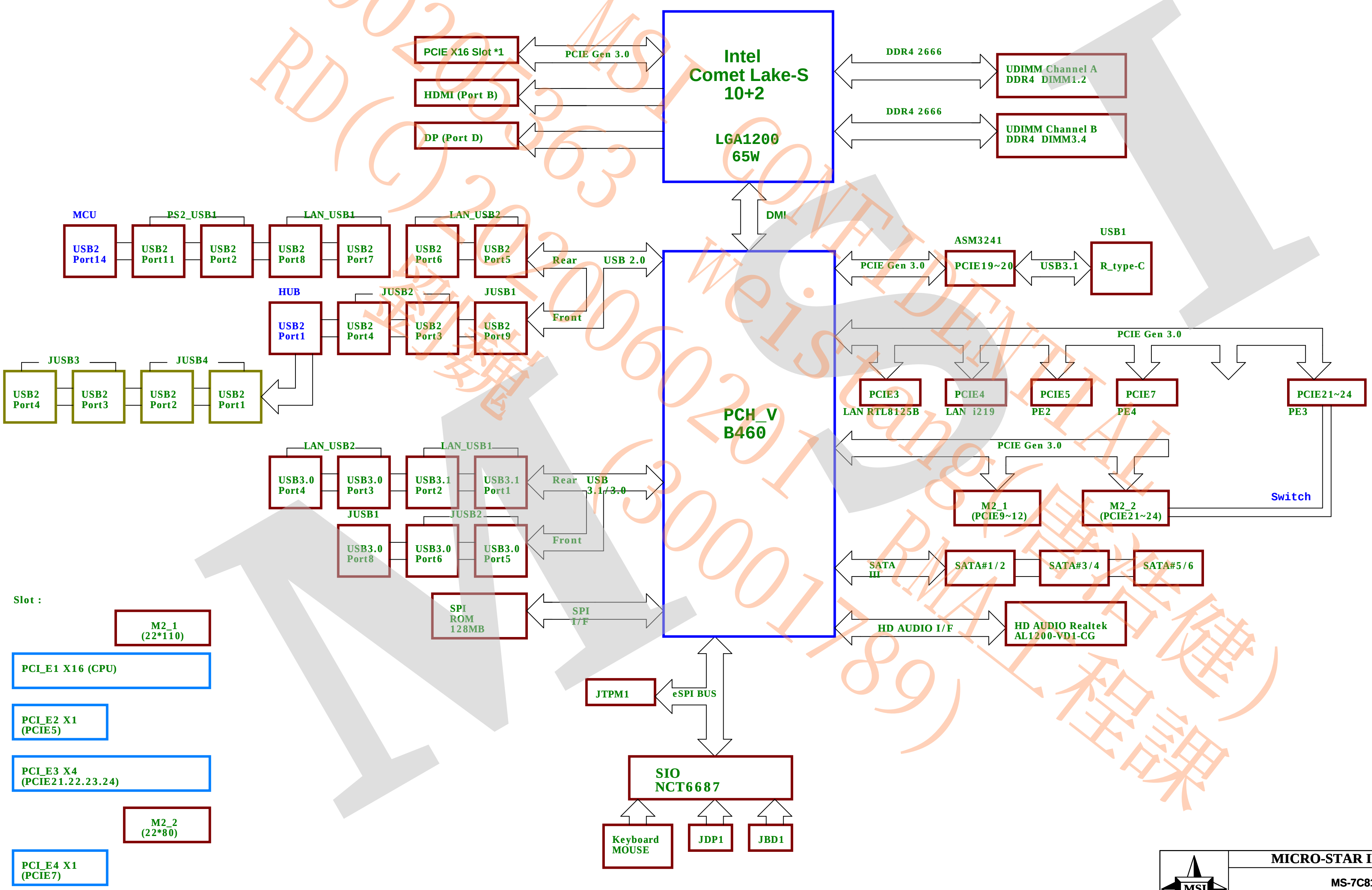
Expansion Slots:

*PCI Express (X16) Slot * 1*
*PCI Express (X4) Slot * 1*
*PCI Express (X1) Slot * 2*
*M.2 Slot * 2*

Other:

*SATA3.0 *6*
*USB2.0 *6*
REAL USB3.1 Gen2 Type A
REAL USB3.1 Gen2 x2 Type C
REAL USB3.1 Gen1 LAN_USB
FRONT USB3.1 GEN1 TypeC
*FRONT USB3.1 *2*

MS-7C81 Block Diagram



MICRO-STAR INT'L CO.,LTD			
MS-7C81			
Size: Custom	Document Description: Block Diagram		Rev: 10
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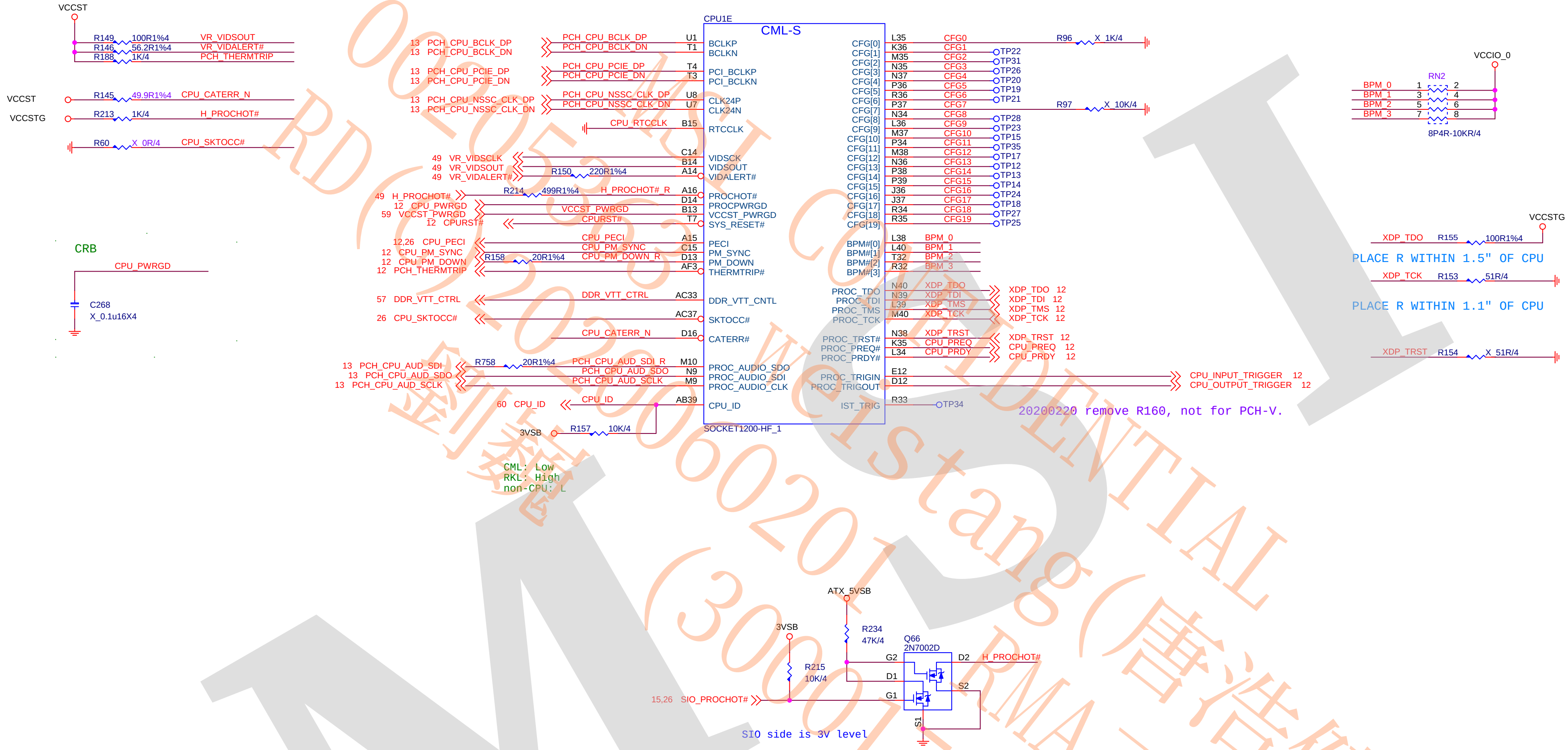

CFG Strap

CFG Table			
	HIGH	LOW	DESCRIPTION
0	No stall	Stall	PCU PLL lock
1			RSVD
2	NORM	REVERSE	PEG_LANE_REVERSAL
3			RSVD
4	DISABLE	ENABLE	eDP
5			PCIE Bifurcation
6			PCIE Bifurcation
7	Follow RESET#	Wait for BIOS	PEG_TRAINING
8			RSVD
9			RSVD
10			RSVD
11			RSVD
12			RSVD
13			RSVD
14			RSVD
15			RSVD
16			RSVD
17			RSVD
18			RSVD
19			RSVD

CFG5	CFG6			
ENABLE#		SLOT	SLOT	SLOT
X8	X4			
0	0	X8	X4	X4
0	1	X8	X8	X0
1	0	RSVD	RSVD	RSVD
1	1	X16	X0	X0

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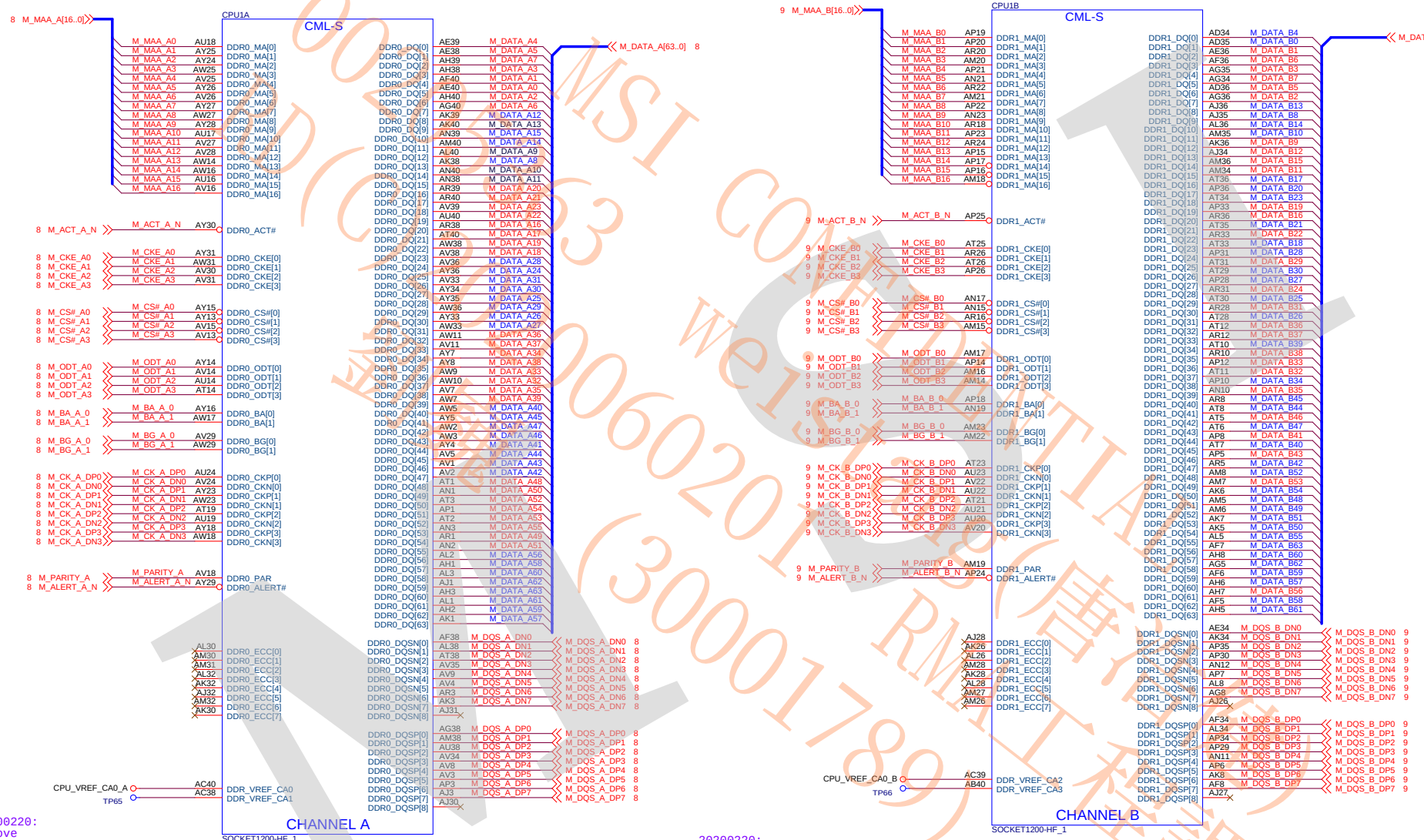

20200220:
remove
DIMM1_CA_VREF_A、CPU_VREF_CA1_A,
follow PDG.

20200220:
remove DIMM1_CA_VREF_B、CPU_VREF_CA1_B,
follow PDG.

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: CPU-Memory	Rev: 10
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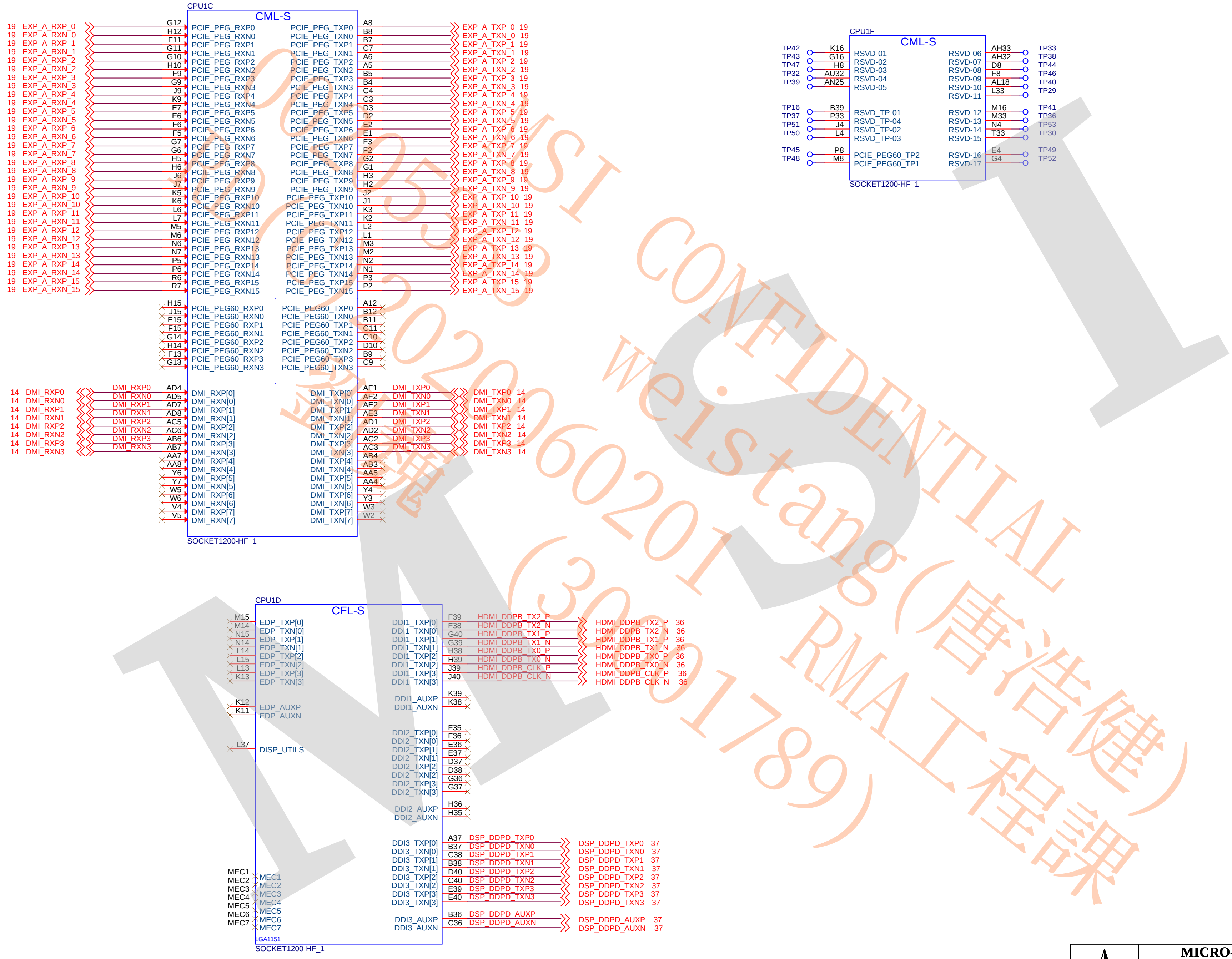

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Size	Document Description	Rev
Custom	CPU-PEG/Display/RSD	10

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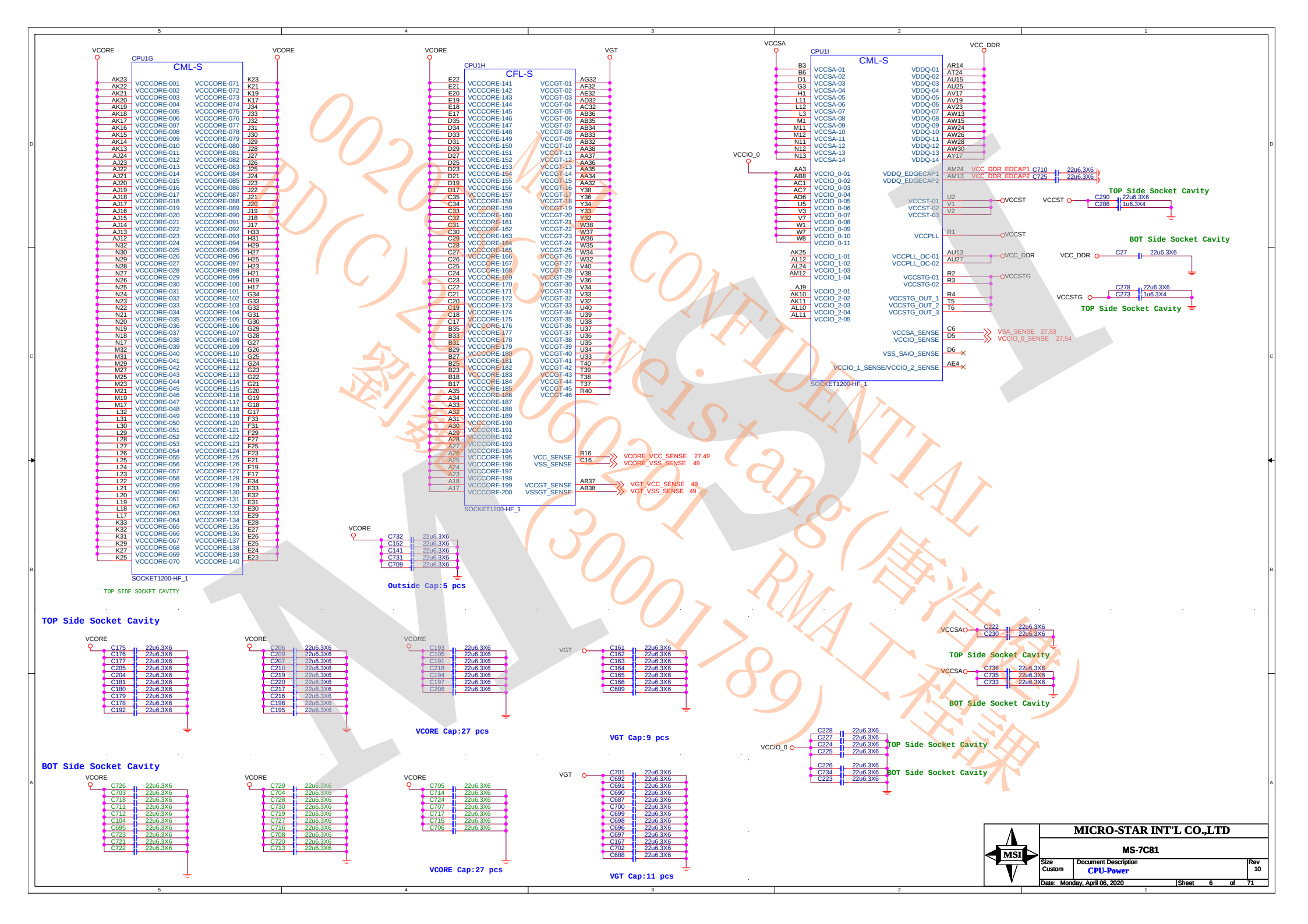
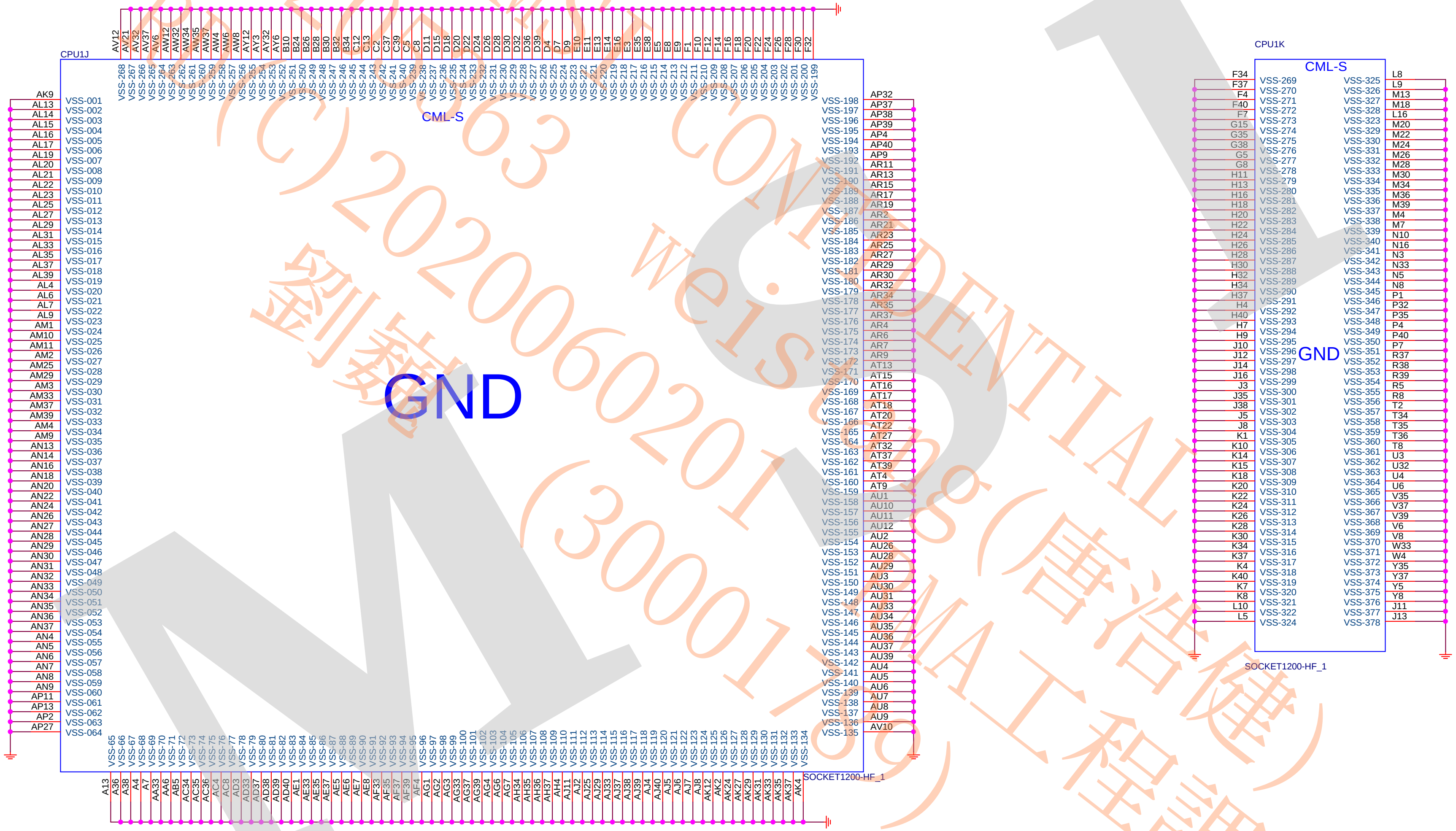

CPU1G
CML-S
SOCKET1200-HF_1
TOP SIDE SOCKET CAVITY
CPU1H
CFL-S
SOCKET1200-HF_1
CPU1I
CML-S
SOCKET1200-HF_1
Outside Cap:5 pcs
TOP Side Socket Cavity
BOT Side Socket Cavity
VCORE Cap:27 pcs
VGT Cap:9 pcs
VCORE Cap:27 pcs
VGT Cap:11 pcs
MICRO-STAR INT'L CO.,LTD
MS-7C81
CPU-Power
Monday, April 06, 2020



MICRO-STAR INT'L CO.,LTD		
MS-7C81		
Size Custom	Document Description CPU-GND	Rev 10
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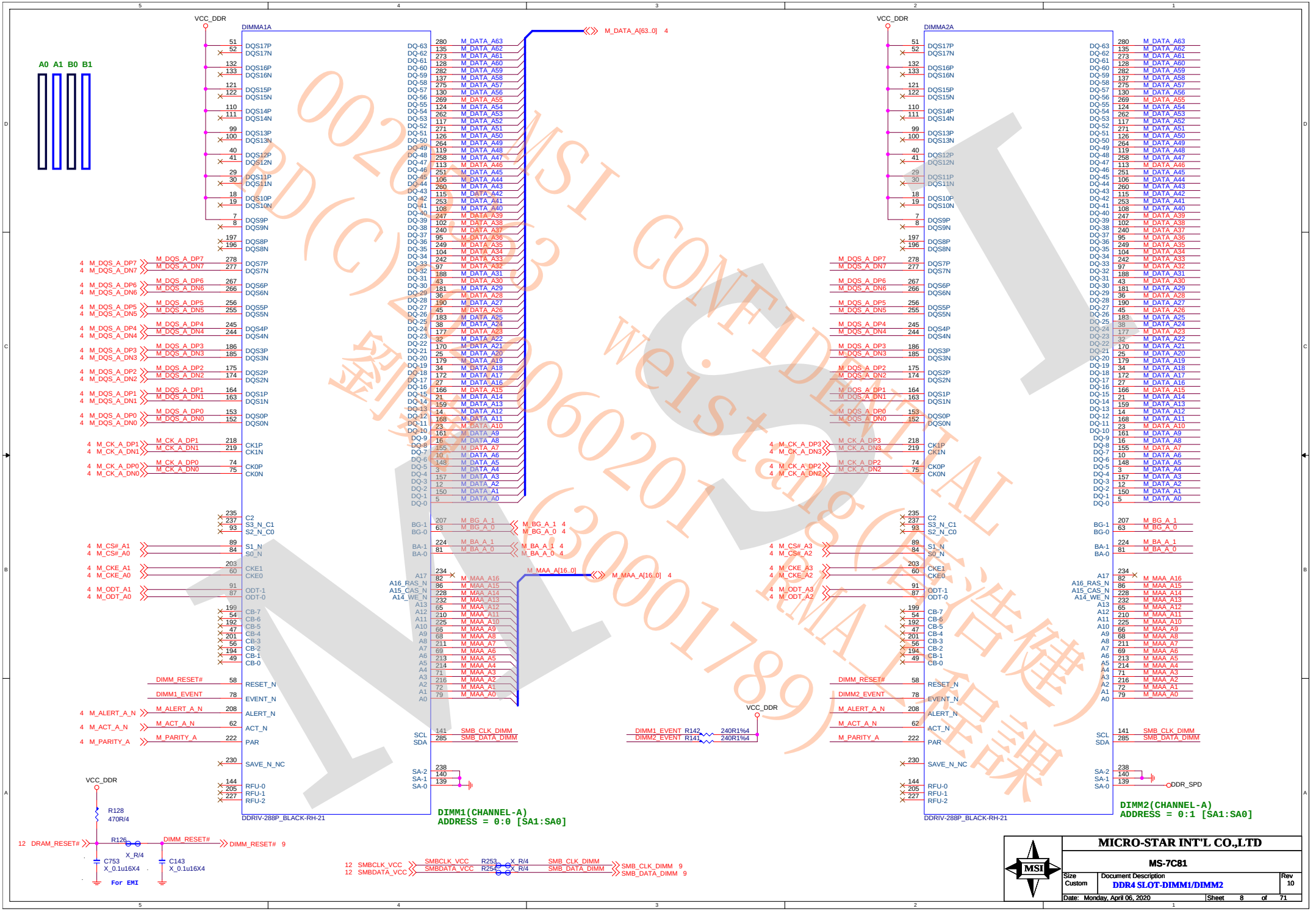
A0 A1 B0 B1
VCC_DDR
DIMMA1A
DDRIV-288P_BLACK-RH-21
DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]
M_DATA_A[63..0] 4
M_MAA_A[16..0]
M_MAA_A[16..0] 4
DIMM1_EVENT R142 240R1%4
DIMM2_EVENT R141 240R1%4
R128 470R/4
R126 X_R/4
C753 X_0.1u16X4
C143 X_0.1u16X4
For EMI
DRAM_RESET#
DIMM_RESET#
DIMM_RESET# 9
SMBCLK_VCC R253 X_R/4 SMB_CLK_DIMM
SMBDATA_VCC R254 X_R/4 SMB_DATA_DIMM
SMB_CLK_DIMM 9
SMB_DATA_DIMM 9
DIMMA2A
DDRIV-288P_BLACK-RH-21
DIMM2(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]
DDR_SPD
MICRO-STAR INT'L CO.,LTD
MS-7C81
Size Custom
Document Description
DDR4 SLOT-DIMM1/DIMM2
Rev 10
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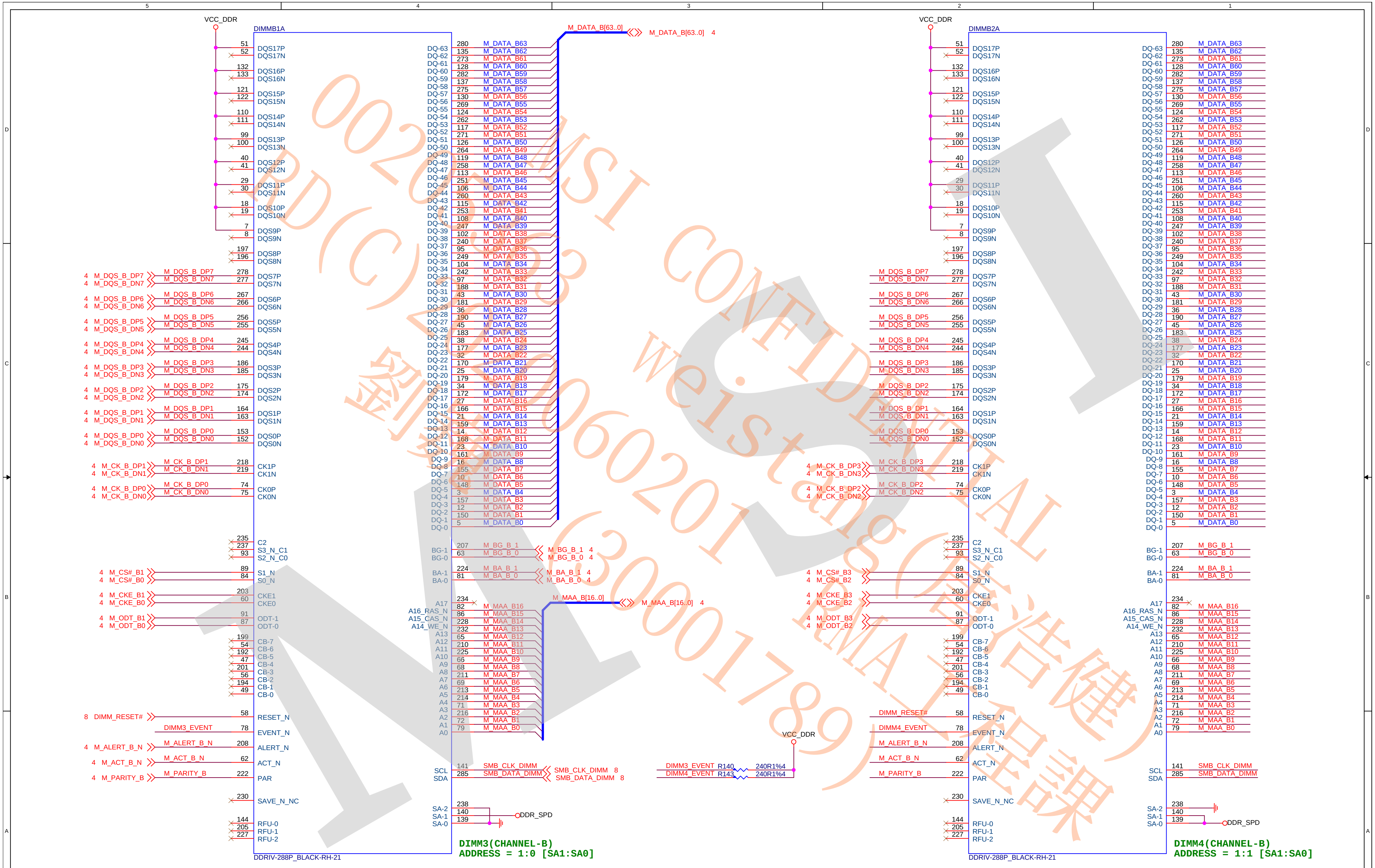

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Size	Document Description	Rev
Custom	DDR4 SLOT-DIMM3/DIMM4	10

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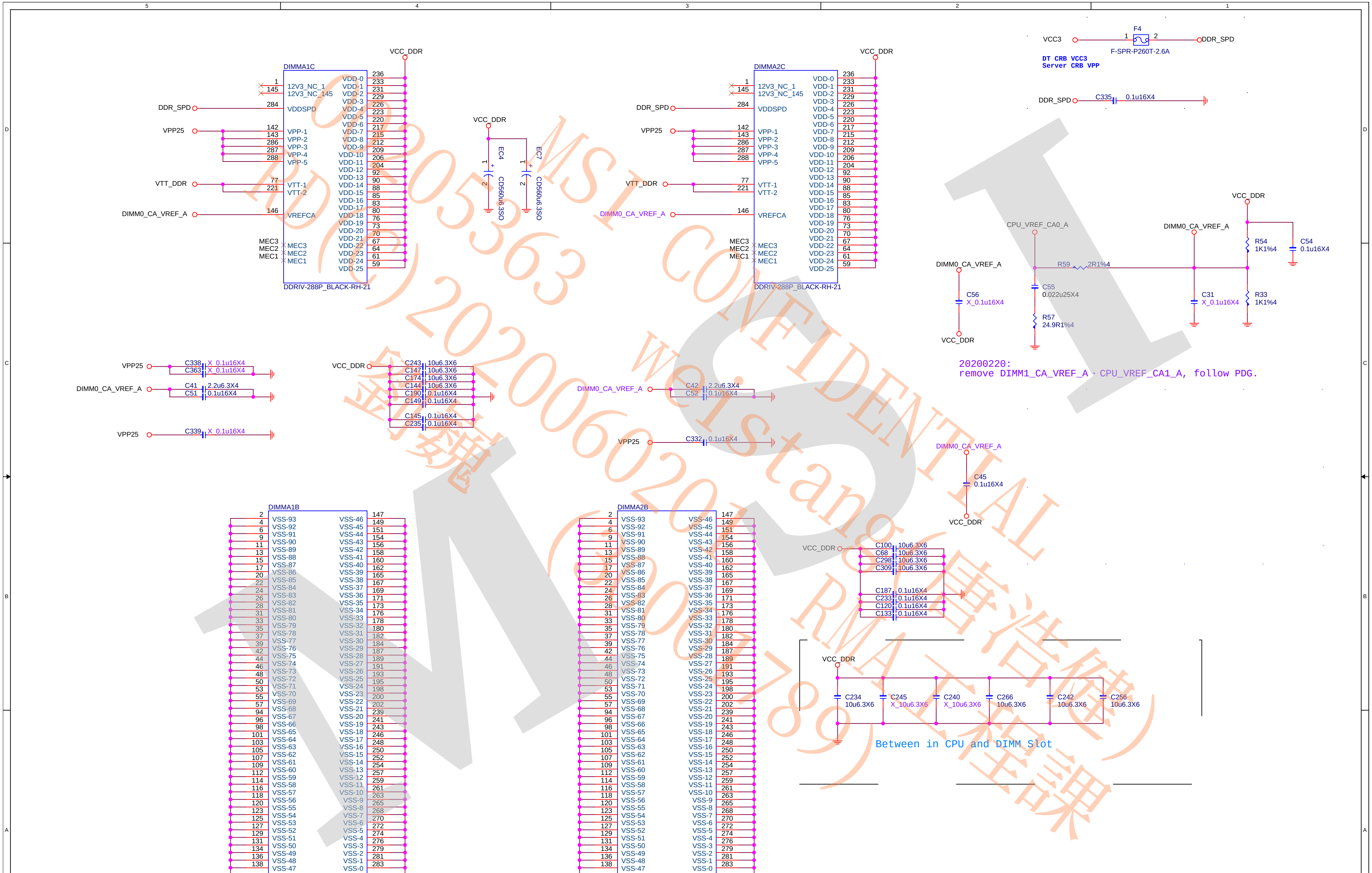

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Size	Document Description	Rev
Custom	DDR4-POWER/GND-1	10

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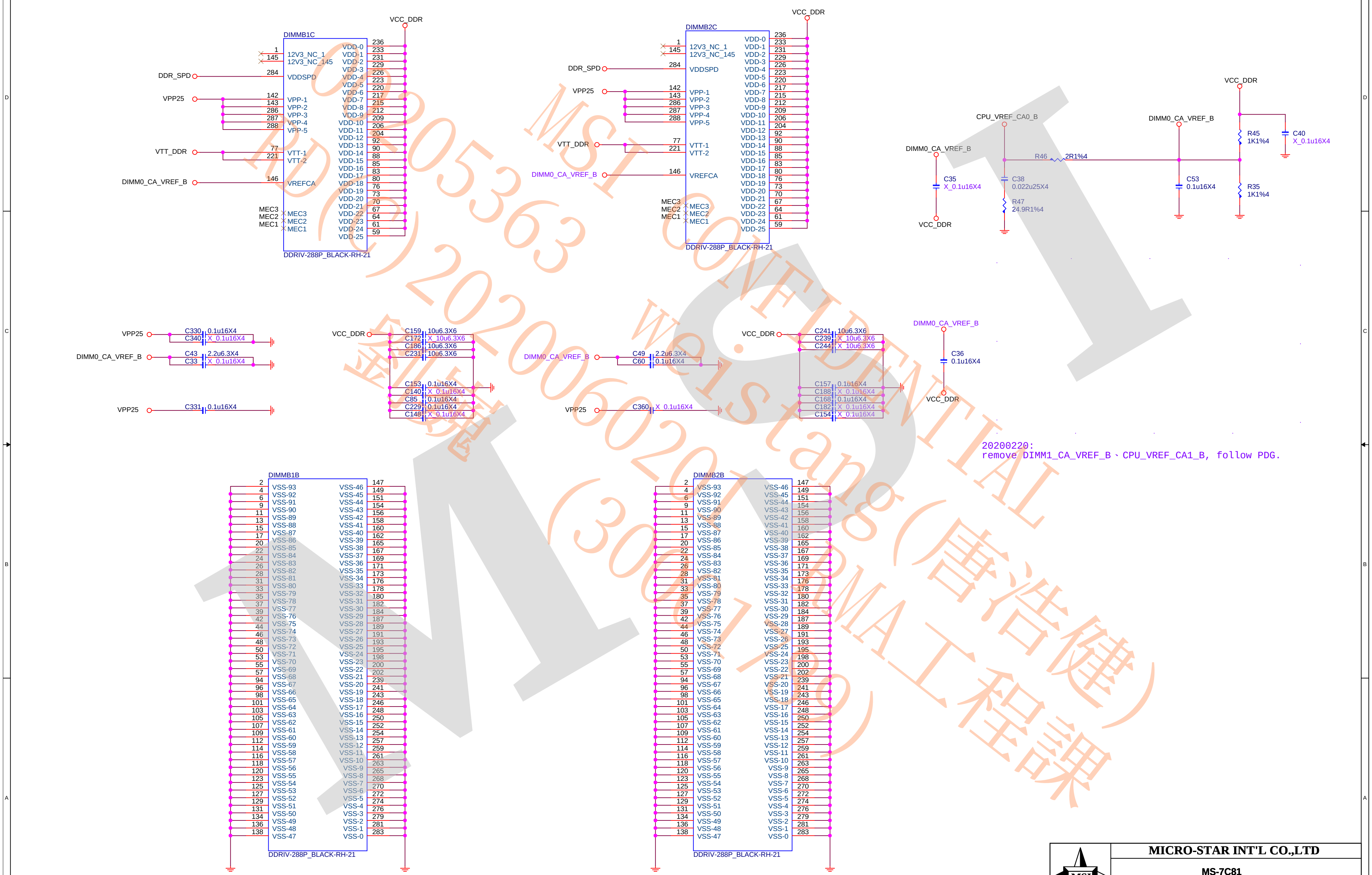

MICRO-STAR INT'L CO.,LTD

MS-7C81

Size	Document Description	Rev
Custom	DDR4-POWER/GND-2	10

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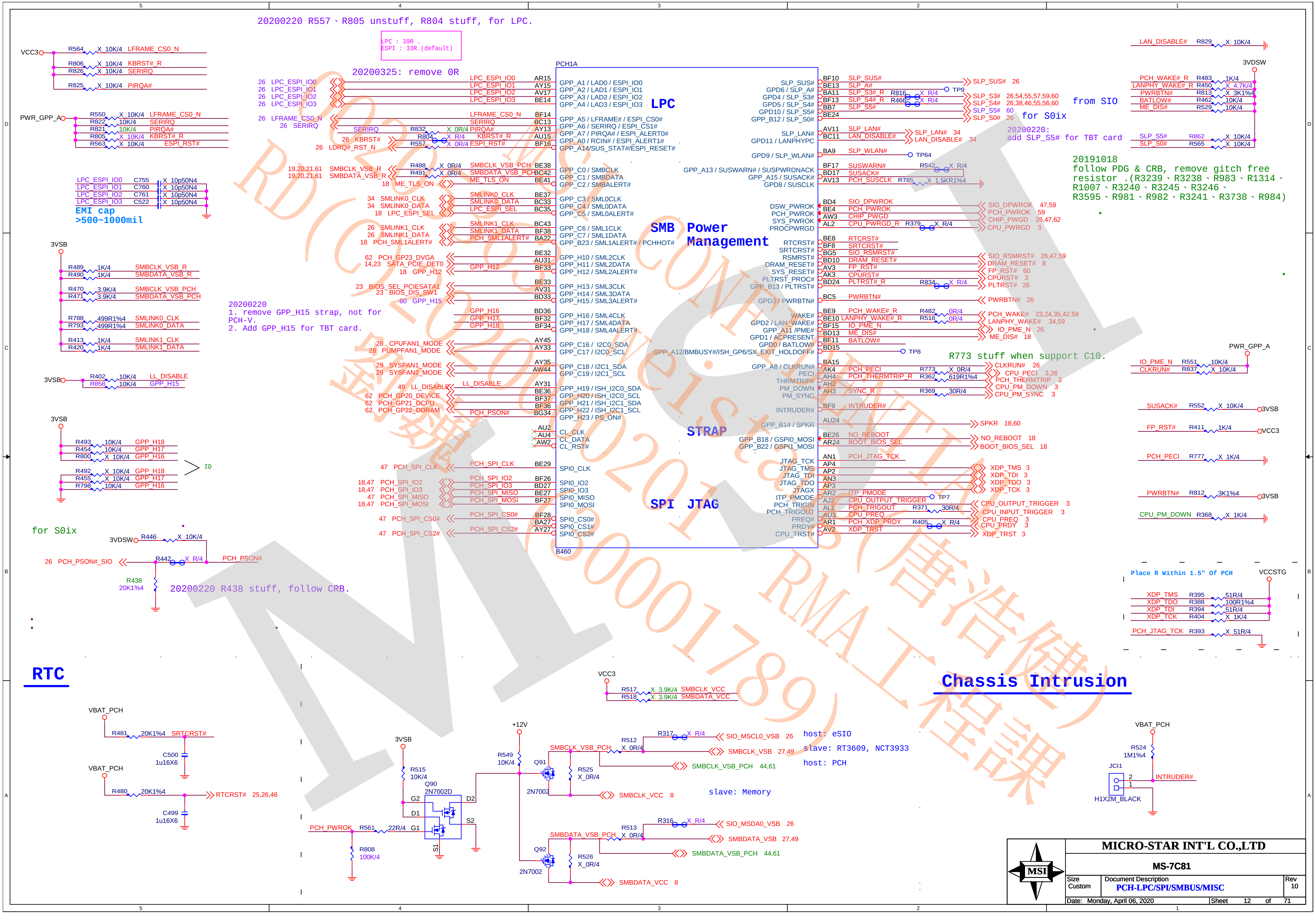

20200220 R557、R805 unstuff, R804 stuff, for LPC.
LPC : 39R .
ESPI : 33R.(default)
20200325: remove 0R
PCH1A
LPC
SMB
Power Management
STRAP
SPI
JTAG
B460
EMI cap
>500~1000mil
20200220
1. remove GPP_H15 strap, not for PCH-V.
2. Add GPP_H15 for TBT card.
for S0ix
20200220 R438 stuff, follow CRB.
from SIO
for S0ix
20200220:
add SLP_S5# for TBT card
20191018
follow PDG & CRB, remove gitch free resistor .(R3239、R3238、R983、R1314、R1007、R3240、R3245、R3246、R3595、R981、R982、R3241、R3738、R984)
R773 stuff when support C10.
Place R Within 1.5" Of PCH
RTC
Chassis Intrusion
host: eSIO
slave: RT3609, NCT3933
host: PCH
slave: Memory
VCC3
3VSB
3VDSW
PWR_GPP_A
VBAT_PCH
VCCSTG
+12V
SMBCLK_VSB_PCH
SMBDATA_VSB_PCH
SMBCLK_VCC
SMBDATA_VCC
SIO_MSCL0_VSB
SIO_MSDA0_VSB
INTRUDER#
JCI1
H1X2M_BLACK
Q90 2N7002D
Q91 2N7002
Q92 2N7002
MICRO-STAR INT'L CO.,LTD
MS-7C81
Size Custom
Document Description
PCH-LPC/SPI/SMBUS/MISC
Rev 10
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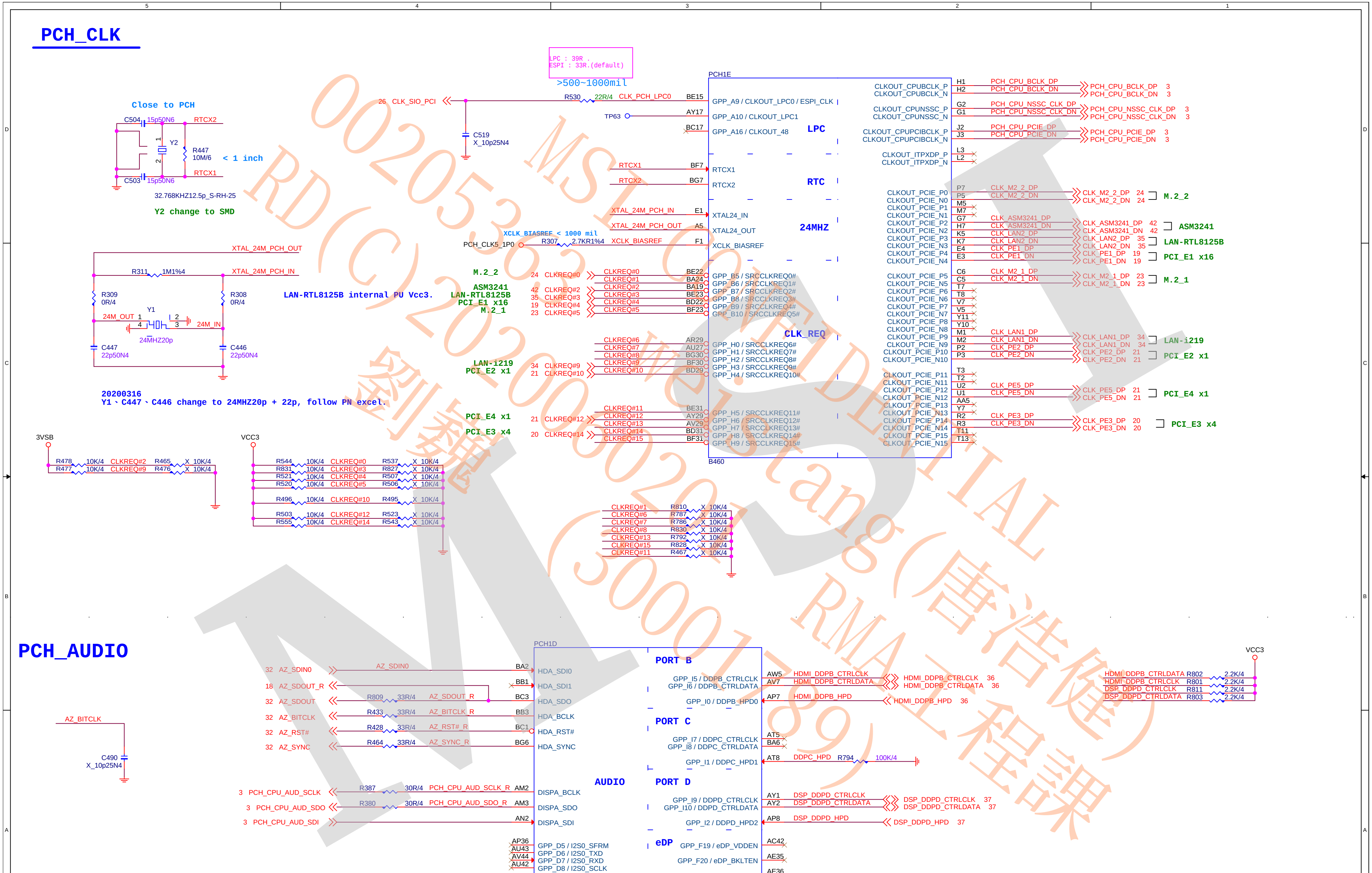

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Size	Document Description	Rev
Custom	PCH-Clock/Audio	10

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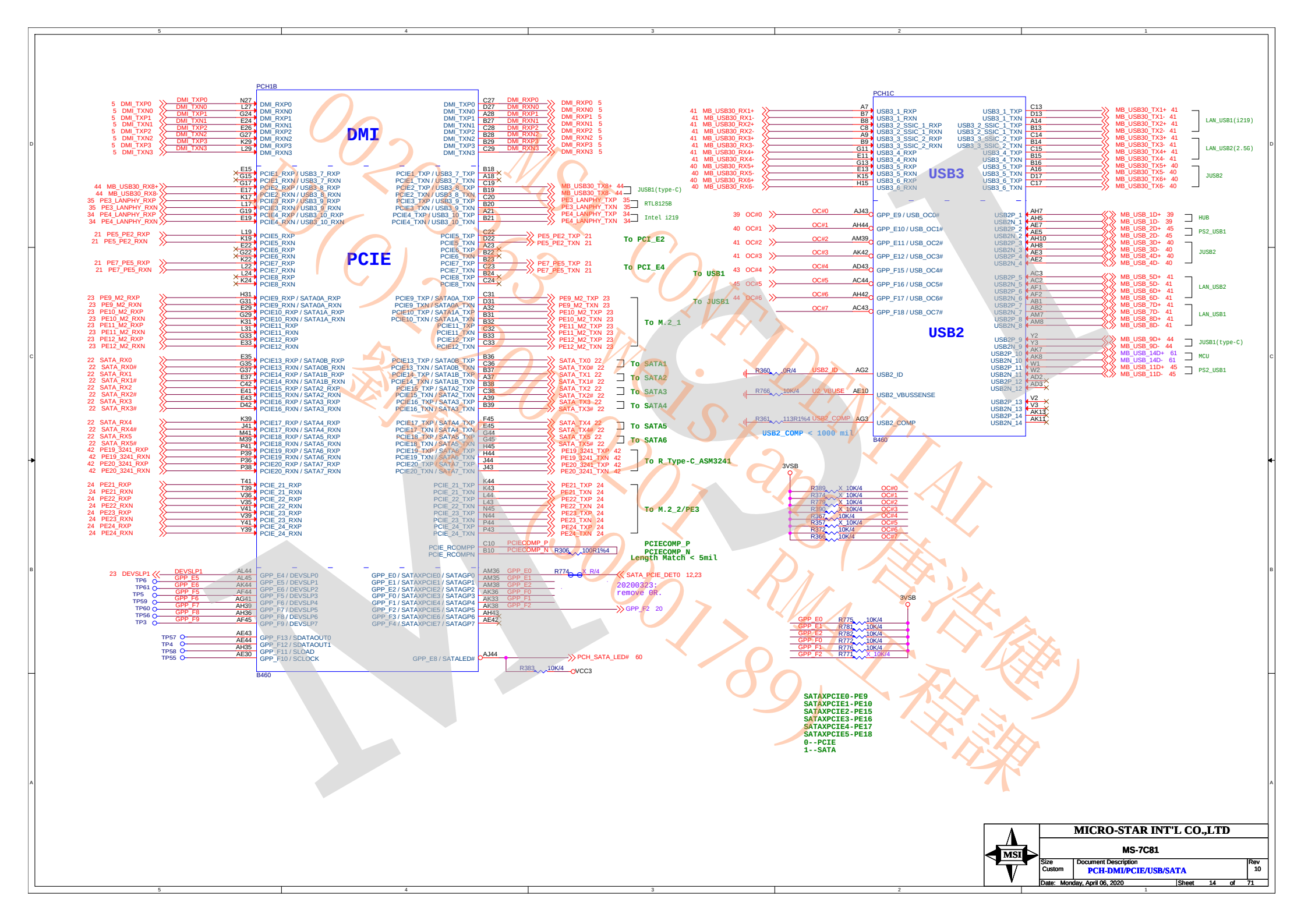
PCH1B
DMI
PCIE
B460
PCH1C
USB3
USB2
B460
To PCI_E2
To PCI_E4
To USB1
To JUSB1
To M.2_1
To SATA1
To SATA2
To SATA3
To SATA4
To SATA5
To SATA6
To R_Type-C_ASM3241
To M.2_2/PE3
PCIECOMP_P
PCIECOMP_N
Length Match < 5mil
USB2_COMP < 1000 mil
SATAXPCIE0-PE9
SATAXPCIE1-PE10
SATAXPCIE2-PE15
SATAXPCIE3-PE16
SATAXPCIE4-PE17
SATAXPCIE5-PE18
0--PCIE
1--SATA
20200323:
remove 0R.
LAN_USB1(i219)
LAN_USB2(2.5G)
JUSB2
JUSB1(type-C)
RTL8125B
Intel i219
HUB
PS2_USB1
MCU
3VSB
VCC3
MICRO-STAR INT'L CO.,LTD
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PCH-DMI/PCIE/USB/SATA
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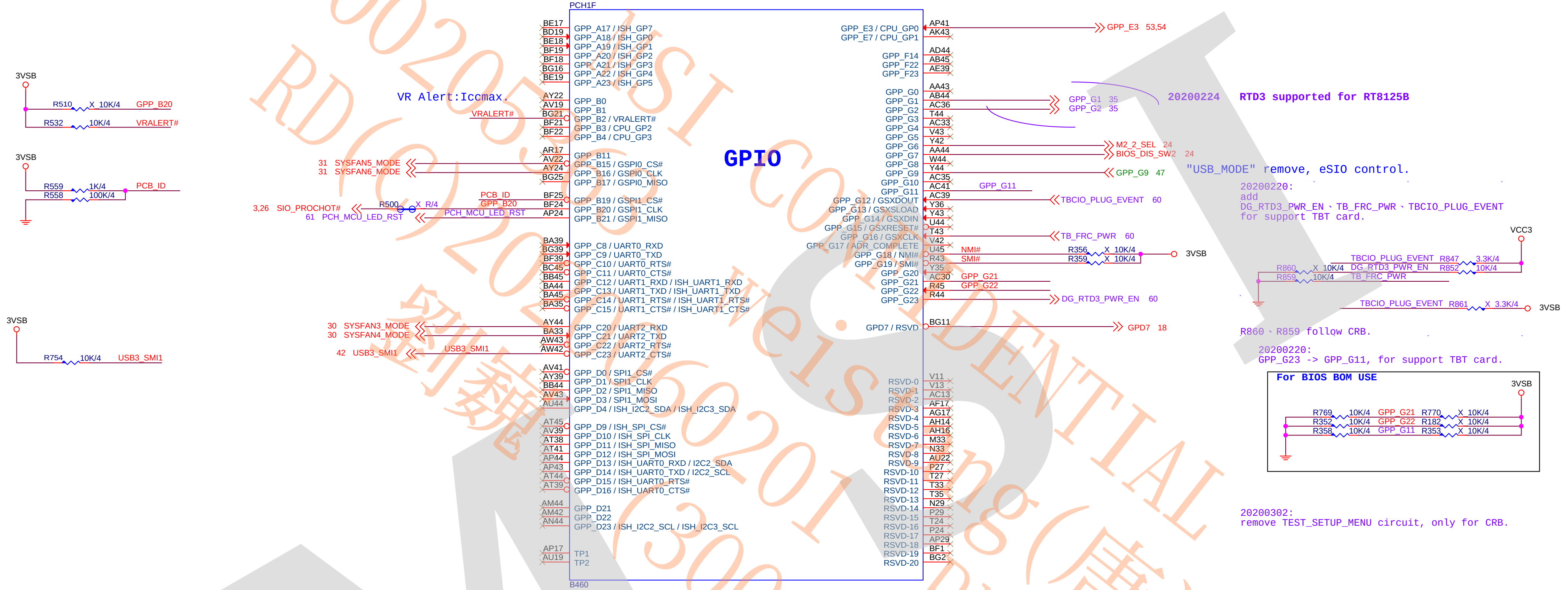

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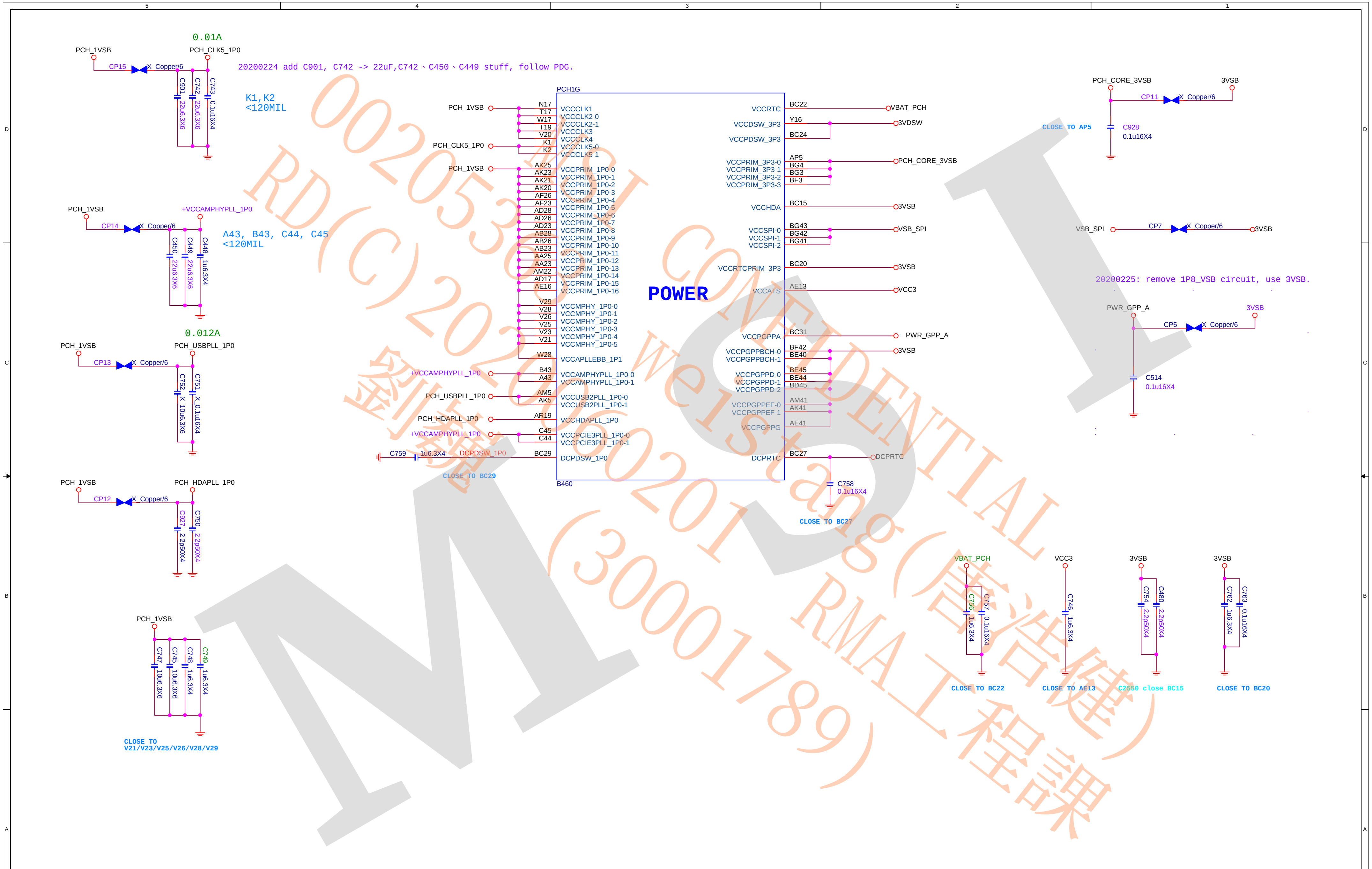

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Size	Document Description	Rev
Custom	PCH-Power	10

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Custom	PCH-GND	10

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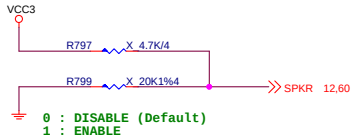
TOP Swap

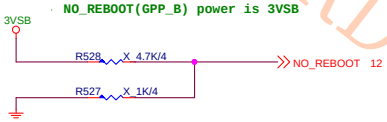


0 : DISABLE (Default)
1 : ENABLE

Internal Pull-down is disabled after PCH_PWROK is high.

No Reboot

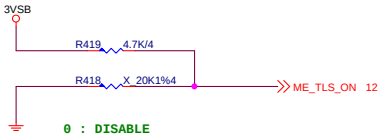
NO_REBOOT(GPP_B) power is 3VSB



0 : DISABLE (Default)
1 : ENABLE

Internal Pull-down is disabled after PCH_PWROK is high.

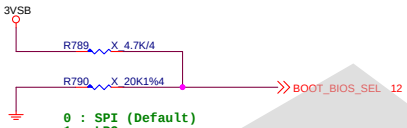
TLS confidentiality



0 : DISABLE
1 : ENABLE (Default)

Internal Pull-down is disabled after RSMRST# de-assert.

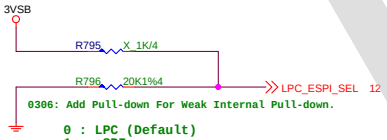
Boot BIOS



0 : SPI (Default)
1 : LPC

Internal Pull-down is disabled after PCH_PWROK is high.

LPC eSPI Mode

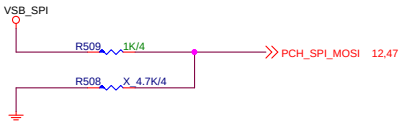


0306: Add Pull-down For Weak Internal Pull-down.

0 : LPC (Default)
1 : eSPI

Internal Pull-down is disabled after RSMRST# de-assert.

Reserved

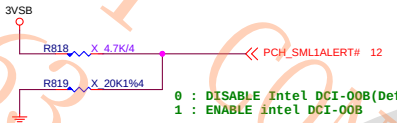


ODT Disable

20200220 remove GPP_H15 strap, not for PCH-V.

DCI Enable

20200302 unstuff, CRB.

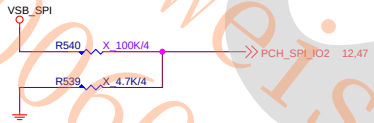


0 : DISABLE Intel DCI-OOB(Default)
1 : ENABLE intel DCI-OOB

Internal Pull-down is disabled after RSMRST# de-assert.

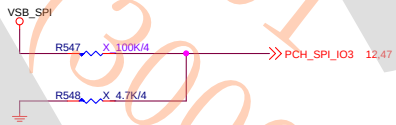
Reserved

20200302 unstuff, CRB.

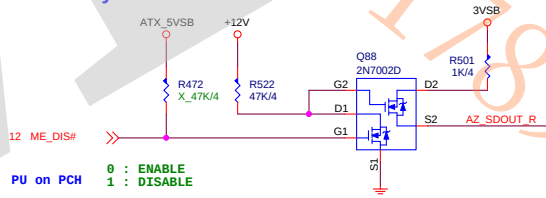


Reserved

20200302 unstuff, CRB.



Flash Descriptor Security Override



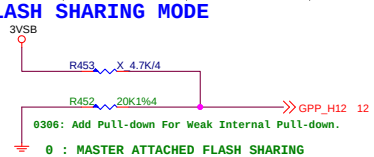
PU on PCH

0 : ENABLE
1 : DISABLE

0 : Enable security measures defined in the Flash Descriptor. (Default)
1 : DISABLE:Flash Descritior Decurity(Override).

Internal Pull-down is disabled after PCH_PWROK is high.

ESPI FLASH SHARING MODE



0306: Add Pull-down For Weak Internal Pull-down.

0 : MASTER ATTACHED FLASH SHARING
1 : SLAVE ATTACHED FLASH SHARING

Internal Pull-down is disabled after RSMRST# de-assert.

XTAL FREQUENCY SELECTION(CNV_BRI_DT)

This Signal has a Weak Internal Pull-down.
An External Pull-up is Required On this Strap Since 38.4 MHz XTAL is Not Supported On the PCH.
0 = 38.4 XTAL Frequency Selected. (Default)
1 = 24MHz XTAL Frequency Selected.

Modem Reference Clock Source Select(CNV_RGI_DT)

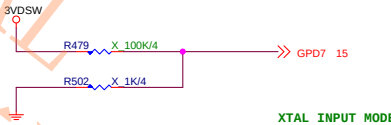
A Weak External Pull-up is Required.
0 = Integrated CNVi Enable.
1 = Integrated CNVi Disable.

Note: When a RF Companion Chip is Connected to The PCH CNVi Interface, The Device Internal Pull Down Resistor will Pull the Strap Load to Enable CNVi Interface.

1.8V VCCPSPI (GPP_J_9_CNV_MFUART2_TXD)

SELECT THE SPI BIOS FLASH INTERFACE OPERATING VOLTAGE
0 = VCCPSPI IS CONNECTED TO 3.3V RAIL - DEFAULT
1 = VCCPSPI IS CONNECTED TO 1.8V RAIL
PCH HAS INTERNAL 20K PD

Reserved



XTAL INPUT MODE??
0 = XTAL INPUT IS SINGLE-ENDED
1 = XTAL INPUT IS DIFFERENTIAL
PCH HAS INTERNAL 20K PD

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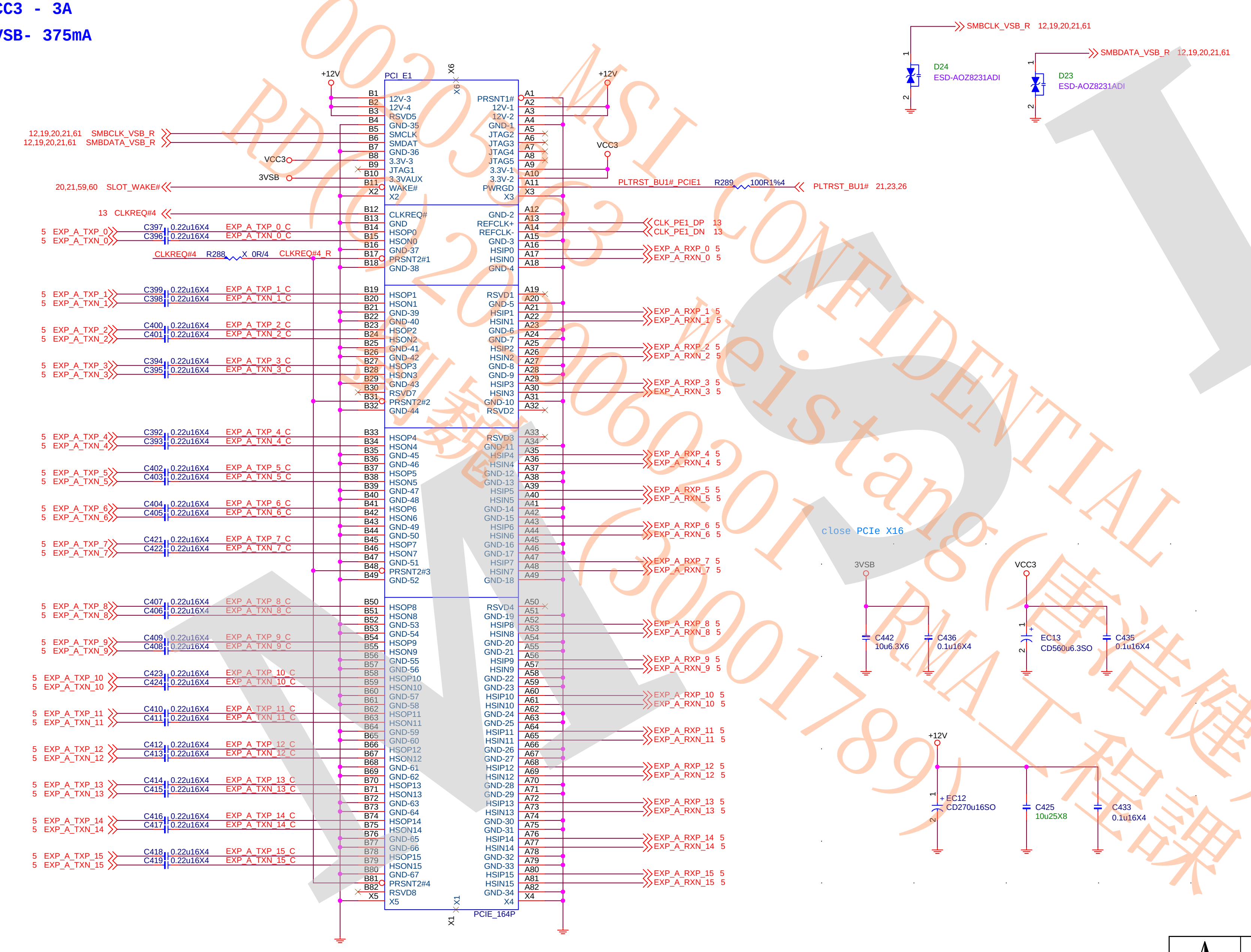
PCI_Express X16 Slot

12V - 5.5A

VCC3 - 3A

3VSB- 375mA

SMBus ESD



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PCIE SLOT (X16)	Rev: 10
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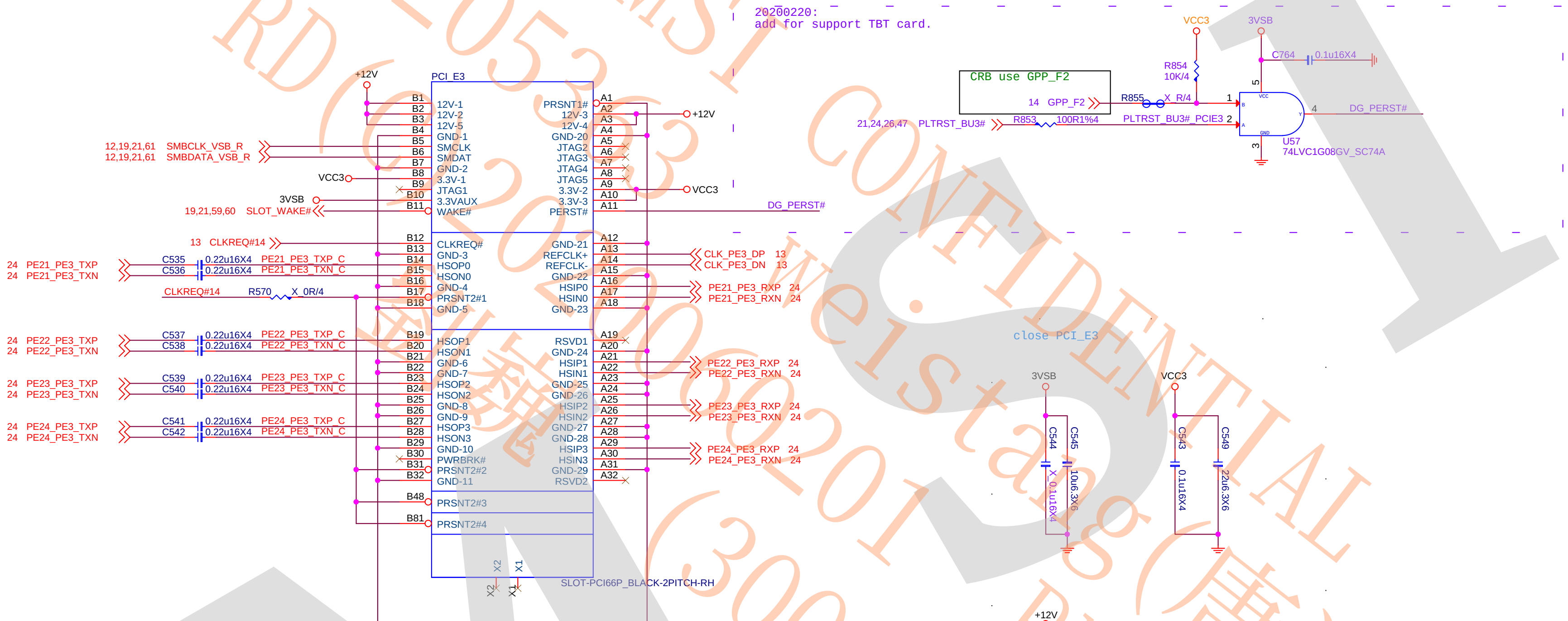
PCI_Express X4 Slot

12V - 2.1A

VCC3 - 3A

3VSB - 375mA

X8 無鐵殼
footprint配合AVL: N11-0660011-L06使用SLOT_PCIEXP66P.



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PCIE SLOT (X4)	Rev: 10
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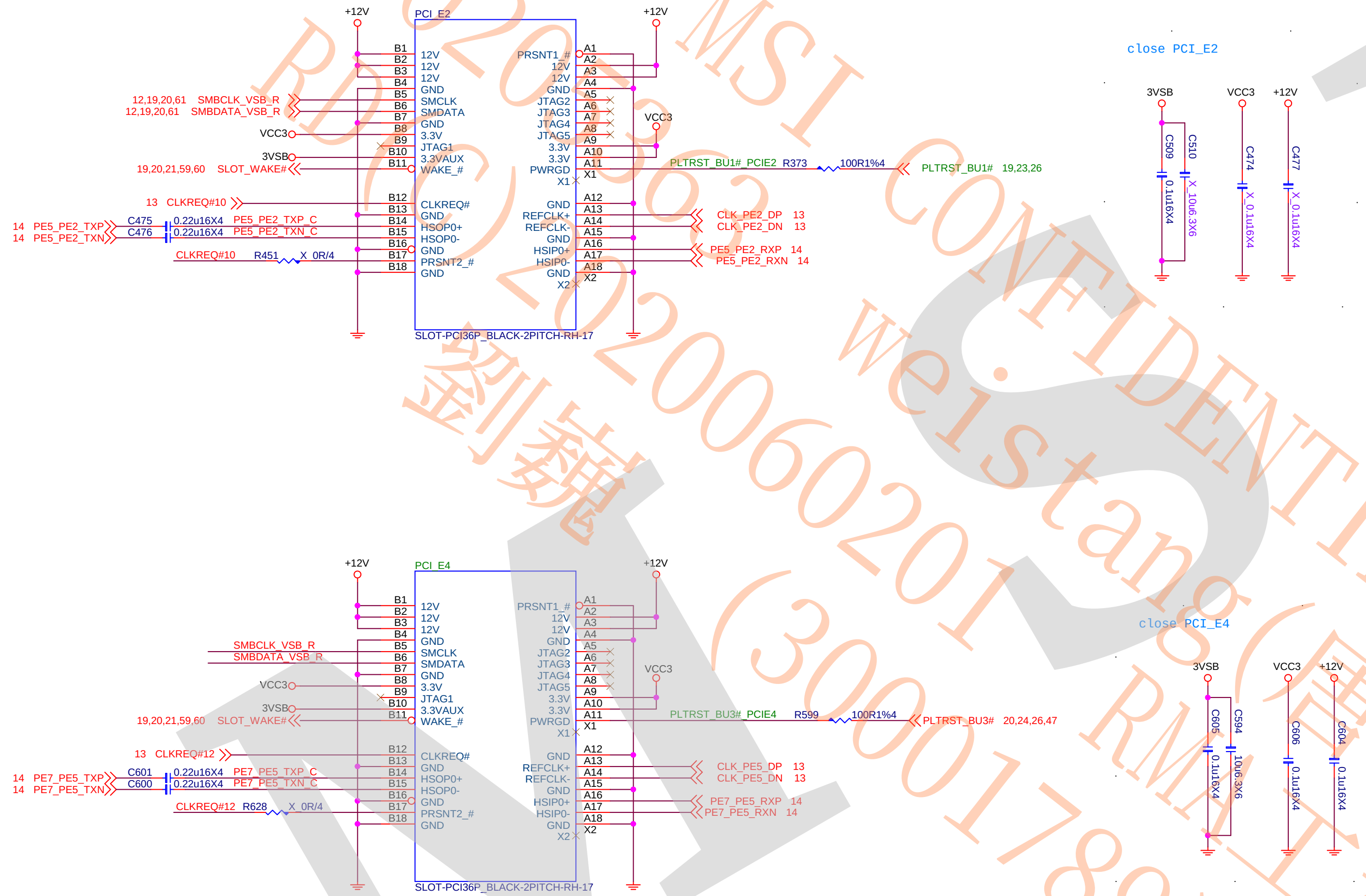
PCH PCIE X1 Slot

12V - 0.5A

VCC3 - 3A

3VSB - 375mA



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PCIE SLOT(X1)	Rev: 10
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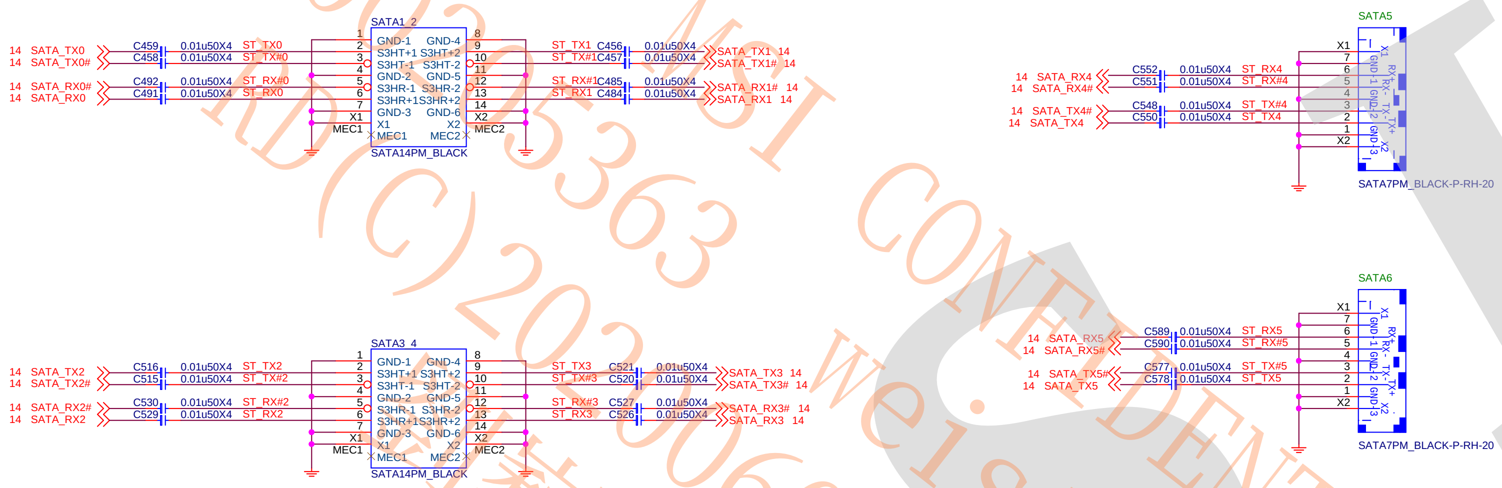
SATA Connector



MICRO-STAR INT'L CO.,LTD
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Size: Custom
Document Description: SATA Connector
Rev: 10
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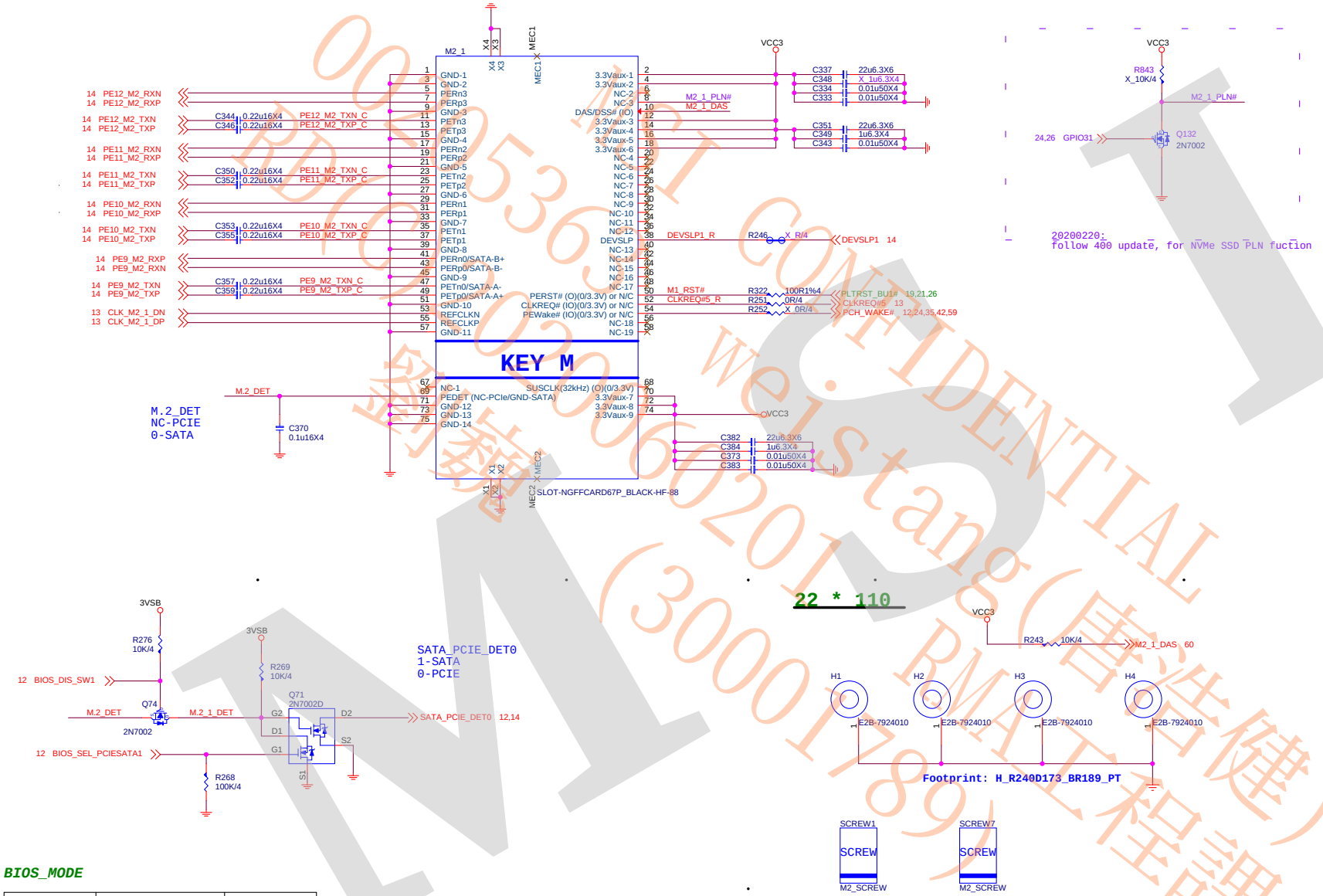
M.2 Connector



BIOS_MODE

BIOS_DIS_SW1	BIOS_SEL_PCIESATA1	Mode
0	1	M2-SATA
0	0	M2-PCIE
GPI	GPI	AUTO

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Size: Custom	Document Description: M.2-SLOT1	Rev: 10
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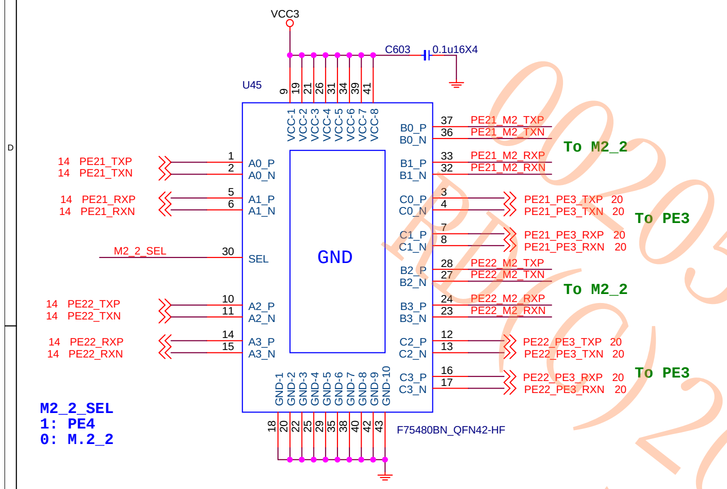
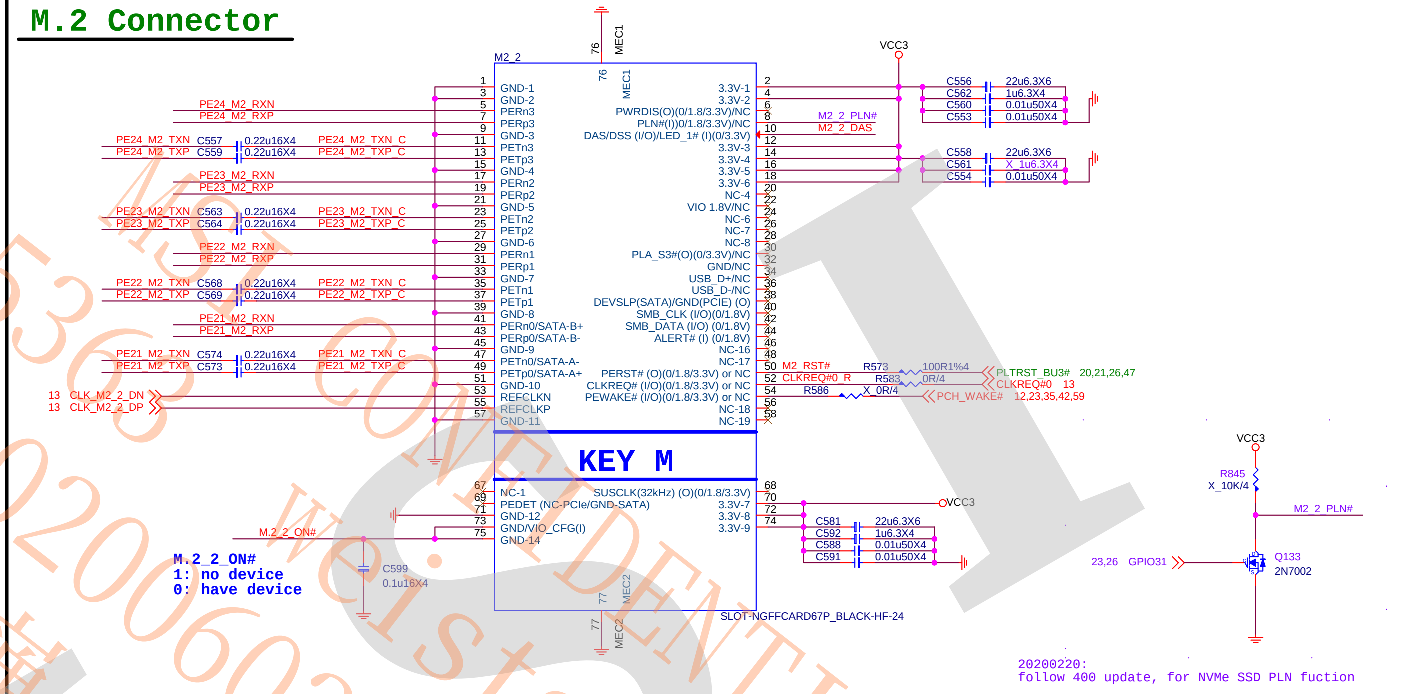
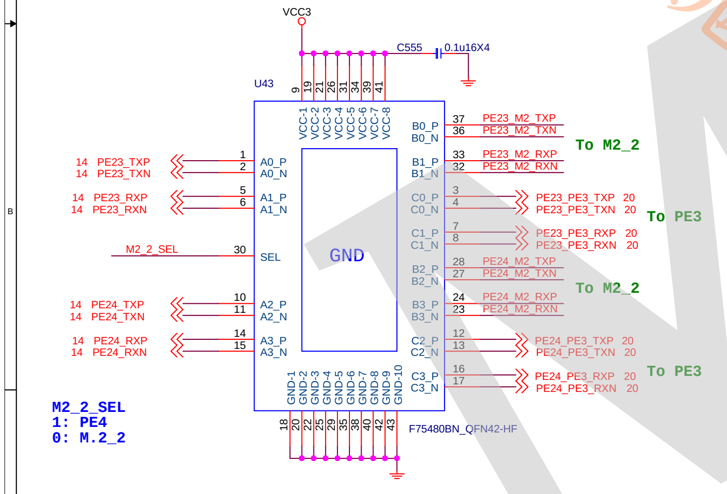
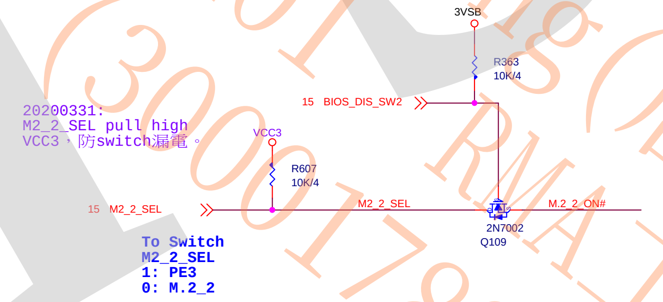
M.2 Connector

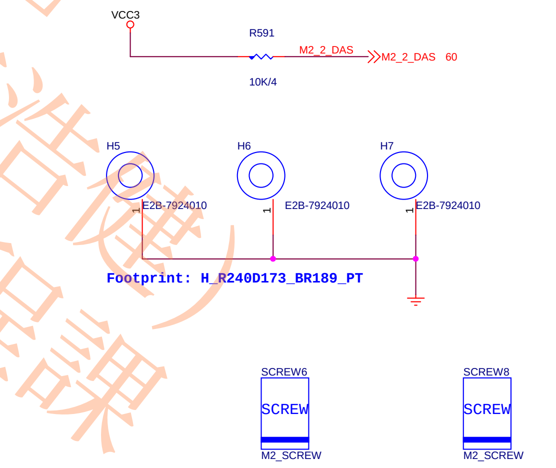








22 * 80



GPP_G7 GPP_G6

BIOS_DIS_SW2	M2_2_SEL	M.2_2_ON#	Mode
GPI(1)	GPI(1)	1	AUTO(PE43
GPI(1)	GPI(0)	0	AUTO(M.2_2)
0	1		PE3
0	0		M.2_2-PCIE

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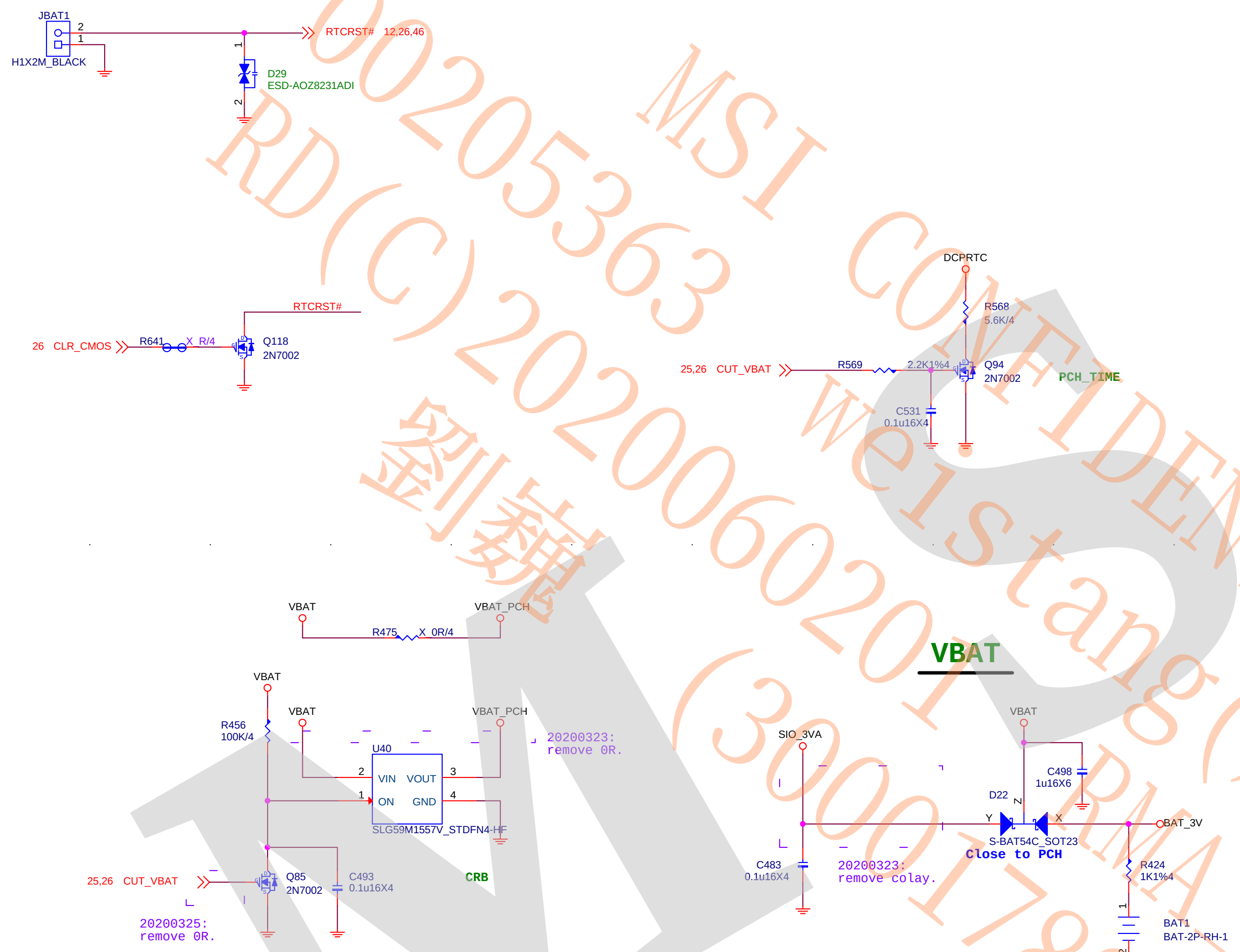

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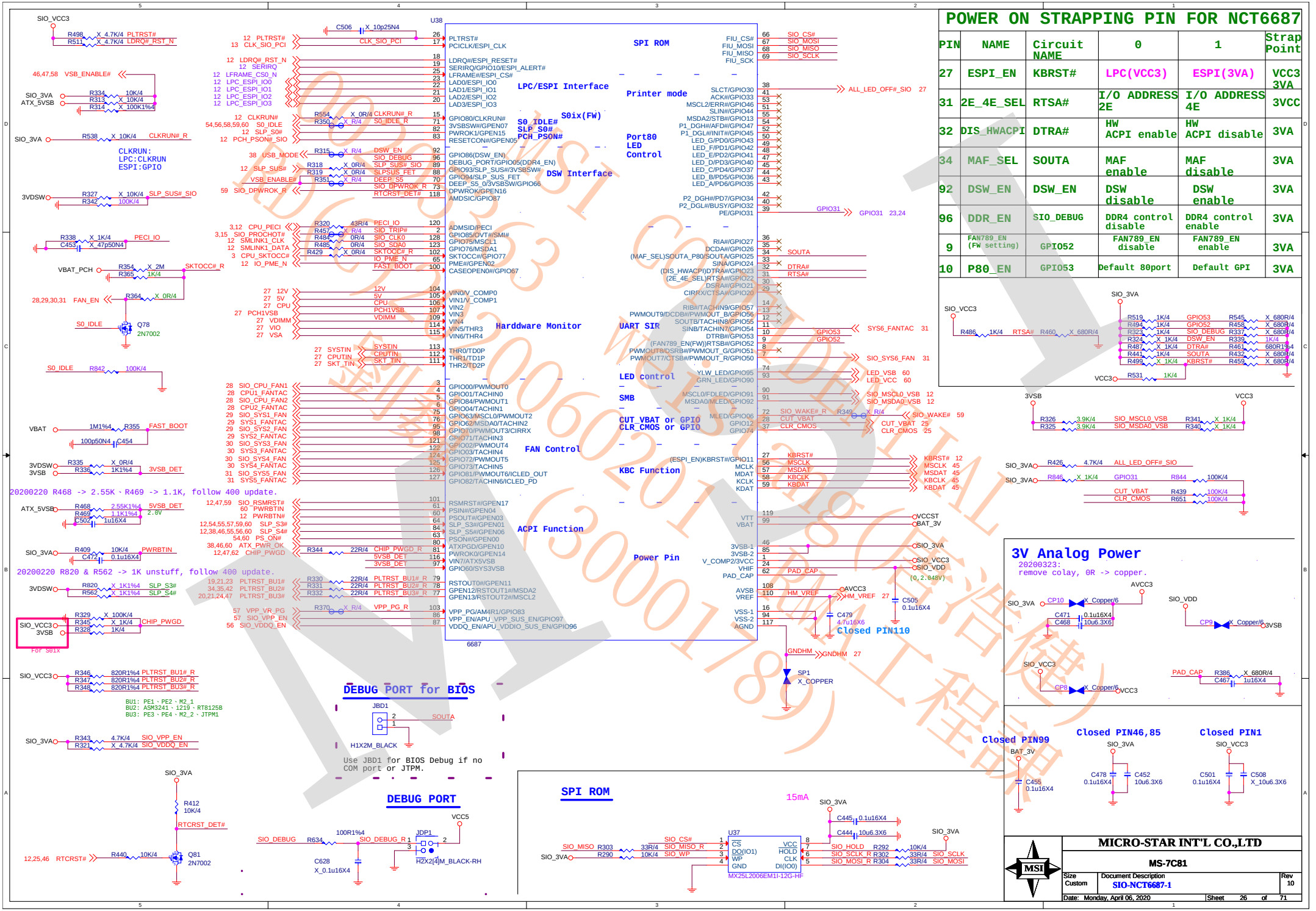
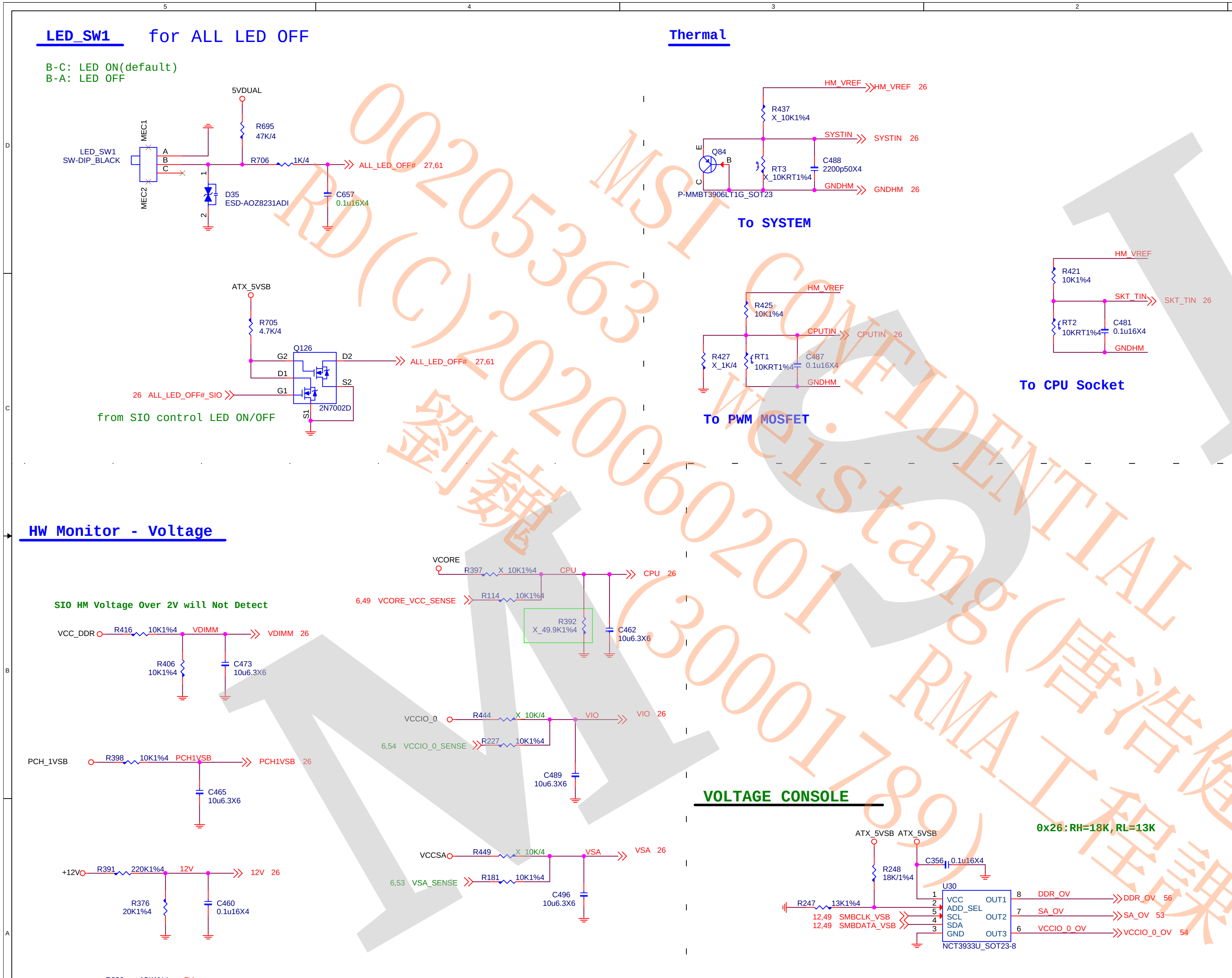


POWER ON STRAPPING PIN FOR NCT6687

PIN	NAME	Circuit NAME	0	1	Strap Point
27	ESPI_EN	KBRST#	LPC(VCC3)	ESPI(3VA)	VCC3 3VA
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	3VCC
32	DIS_HWACPI	DTRA#	HW ACPI enable	HW ACPI disable	3VA
34	MAF_SEL	SOUTA	MAF enable	MAF disable	3VA
92	DSW_EN	DSW_EN	DSW disable	DSW enable	3VA
96	DDR_EN	SIO_DEBUG	DDR4 control disable	DDR4 control enable	3VA
9	FAN789_EN (FW setting)	GPIO52	FAN789_EN disable	FAN789_EN enable	3VA
10	P80_EN	GPIO53	Default 80port	Default GPI	3VA



UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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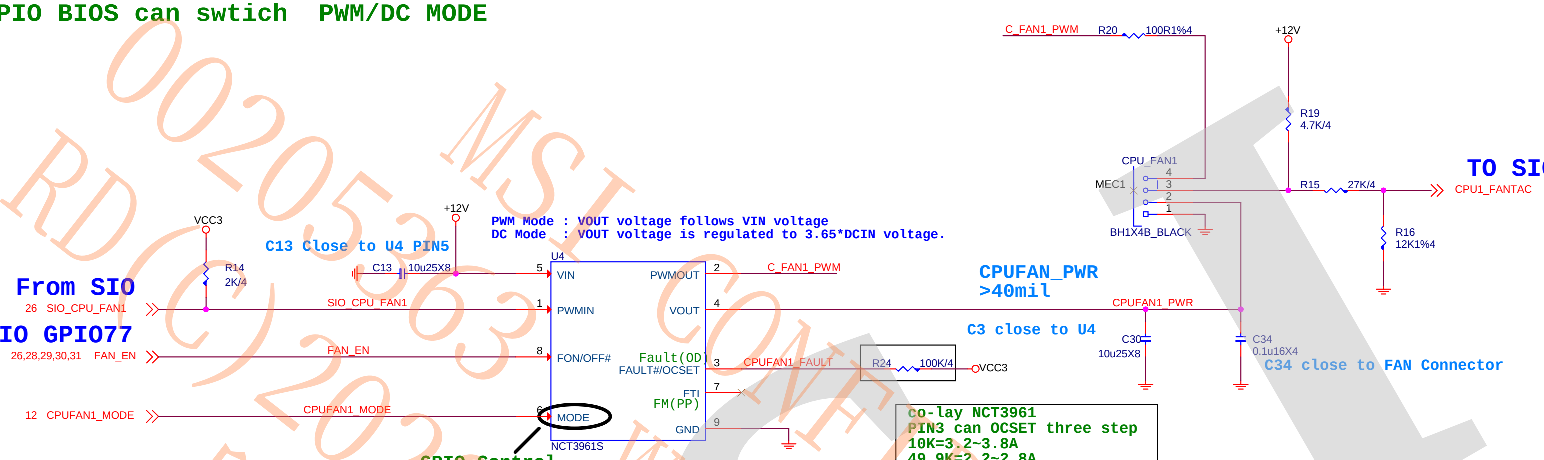
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

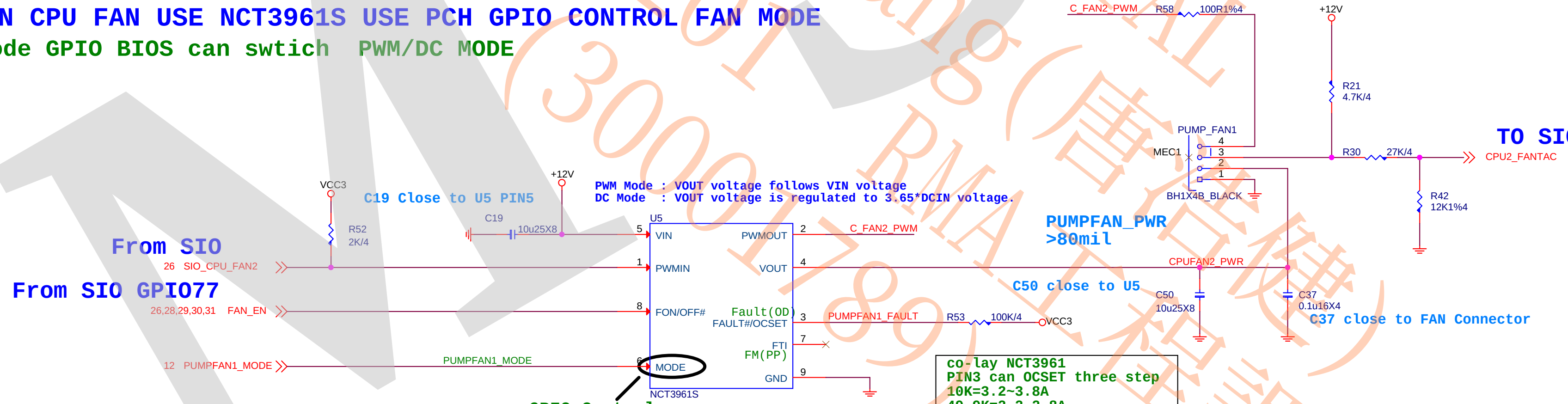


GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

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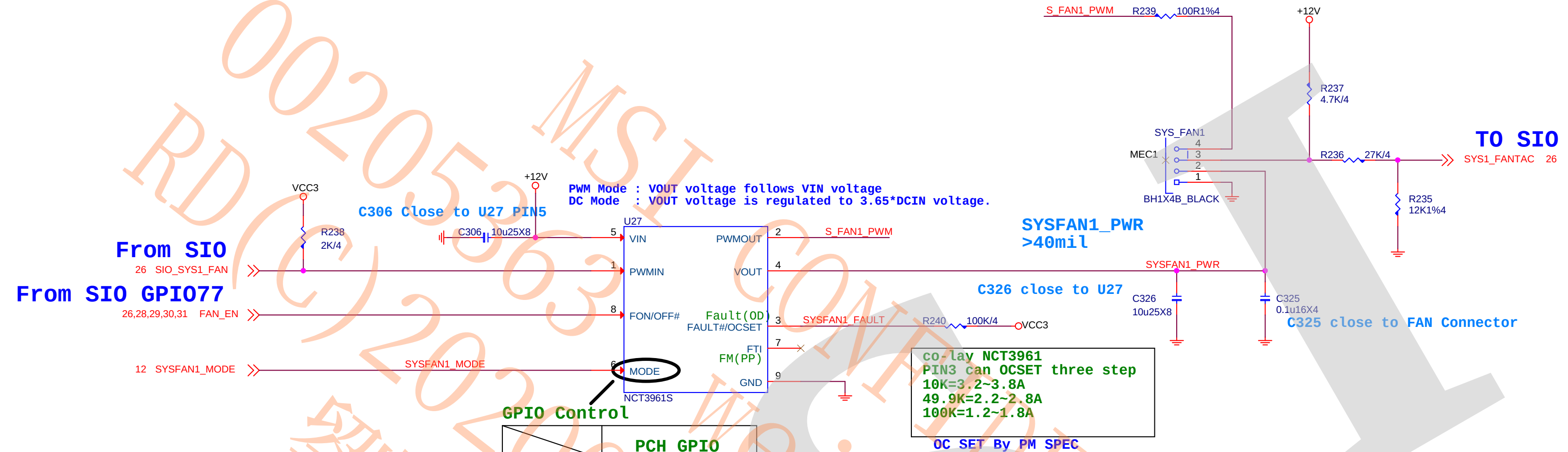
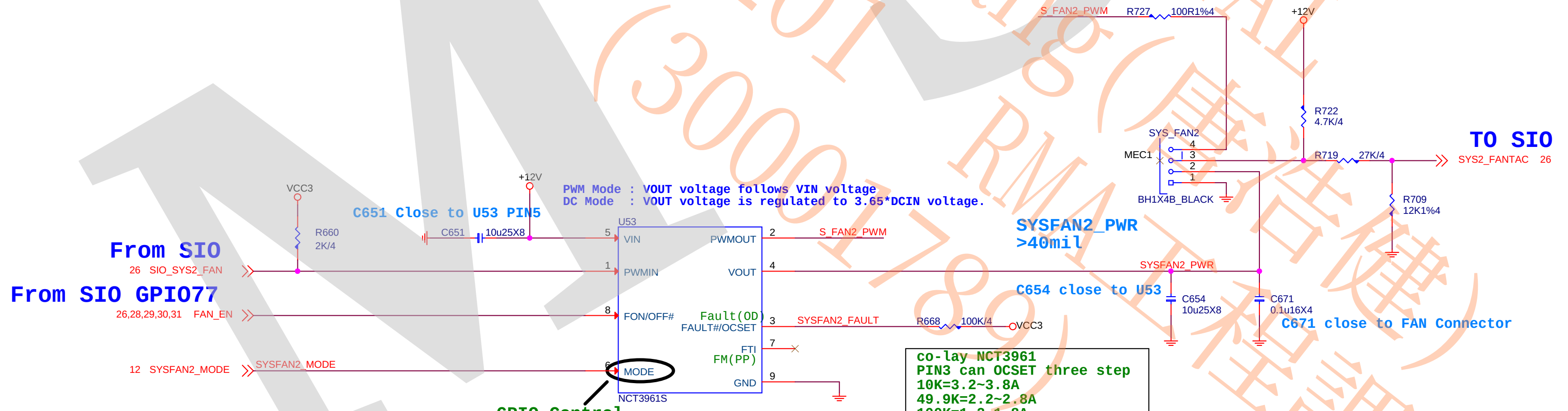
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

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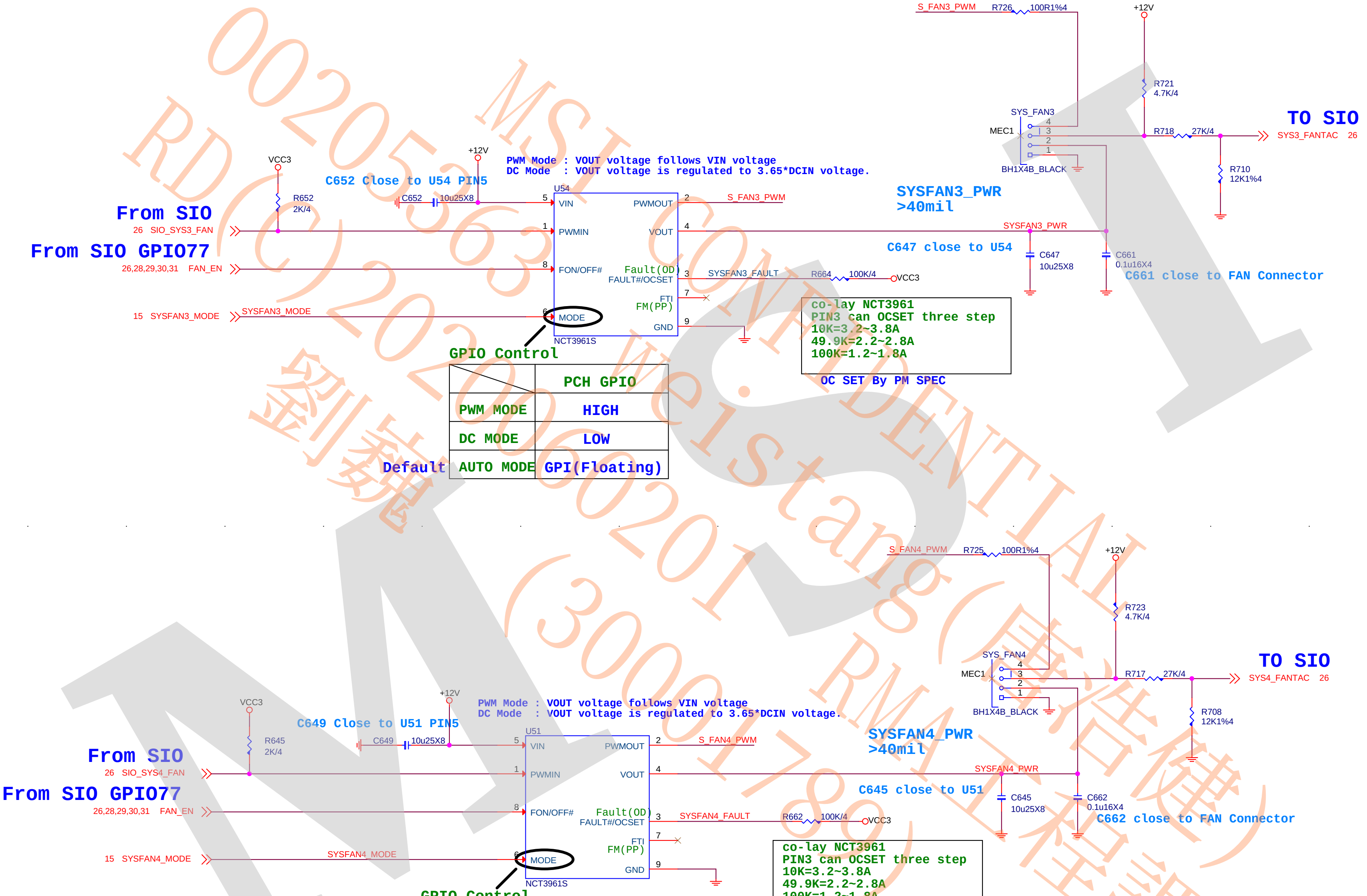
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



co-lay NCT3961
PIN3 can OCSET three step
10K=3.2~3.8A
49.9K=2.2~2.8A
100K=1.2~1.8A
OC SET By PM SPEC

GPIO Control

		PCH GPIO
	PWM MODE	HIGH
	DC MODE	LOW
Default	AUTO MODE	GPI(Floating)

co-lay NCT3961
PIN3 can OCSET three step
10K=3.2~3.8A
49.9K=2.2~2.8A
100K=1.2~1.8A
OC SET By PM SPEC

GPIO Control

		PCH GPIO
	PWM MODE	HIGH
	DC MODE	LOW
Default	AUTO MODE	GPI(Floating)

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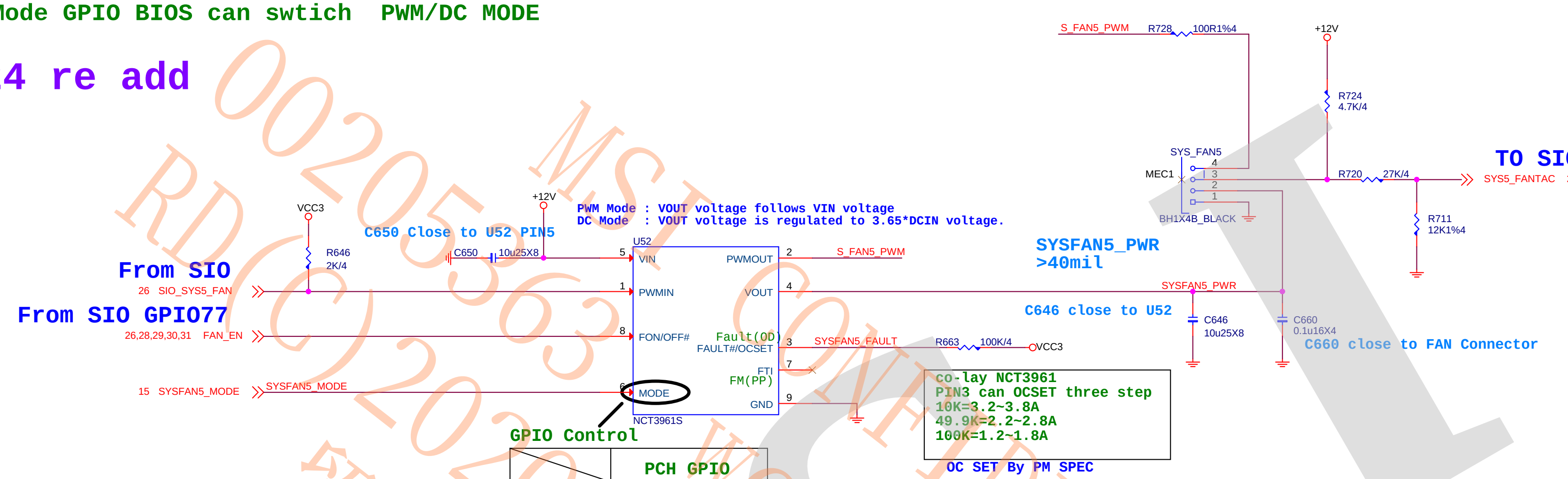
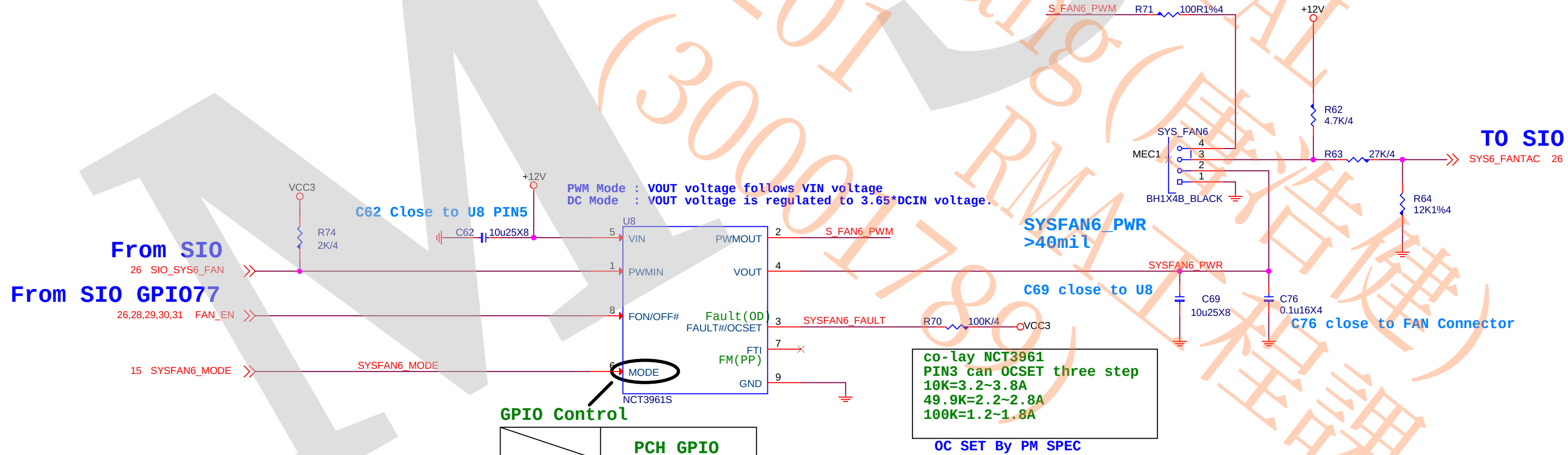
TYPE M : 4 PIN CPU FAN USE NCT3961S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

20200324 re add



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)



	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
Default AUTO MODE	GPI(Floating)

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Size: Custom | Document Description: SYS5 and SYS6 FAN | Rev: 10

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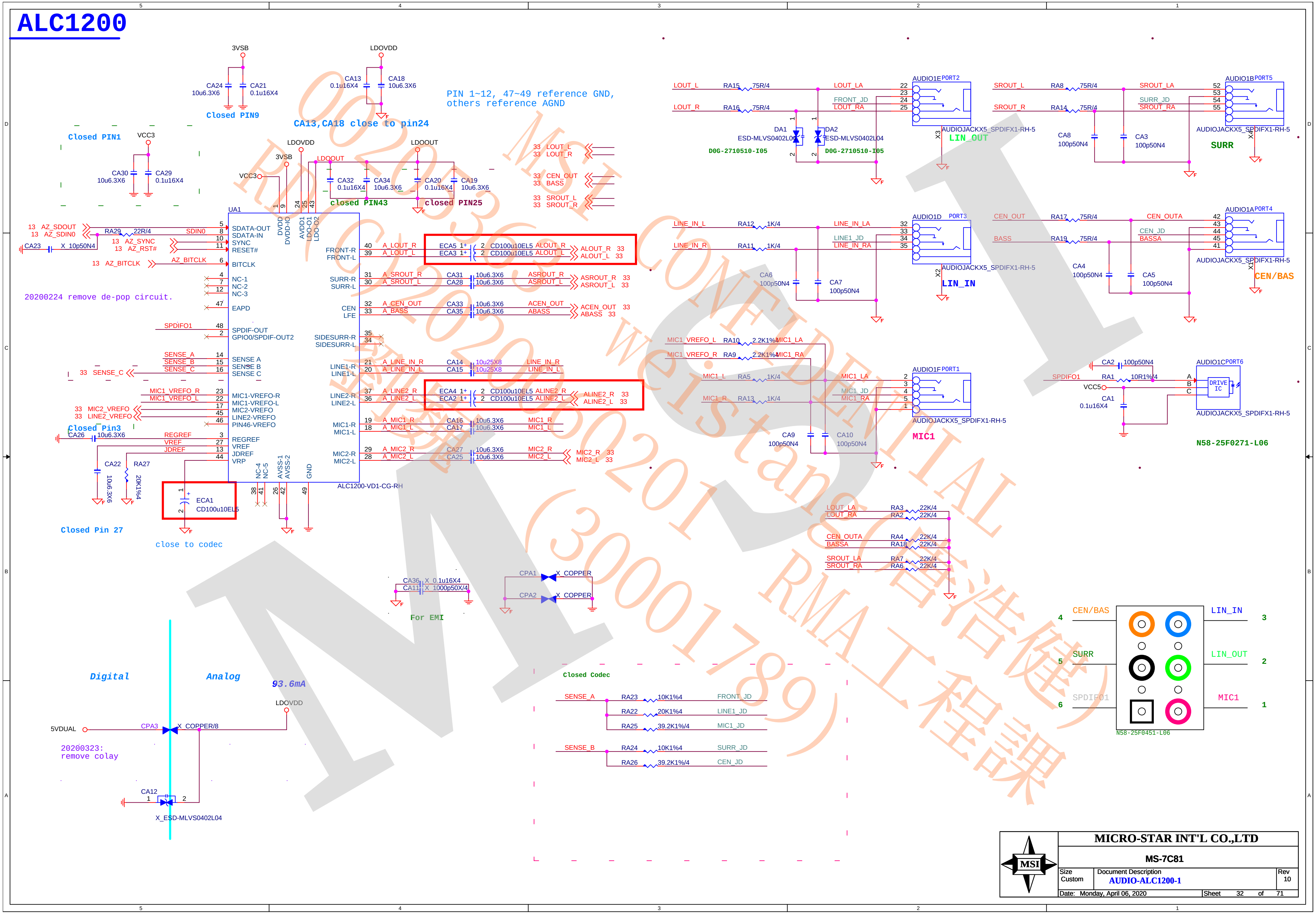
ALC1200
PIN 1~12, 47~49 reference GND, others reference AGND
CA13,CA18 close to pin24
Closed PIN1
Closed PIN9
closed PIN43
closed PIN25
20200224 remove de-pop circuit.
Closed Pin3
Closed Pin 27
close to codec
ALC1200-VD1-CG-RH
UA1
LIN_OUT
SURR
LIN_IN
CEN/BAS
MIC1
N58-25F0271-L06
D0G-2710510-I05
AUDIOJACKX5_SPDIFX1-RH-5
For EMI
Digital
Analog
93.6mA
5VDUAL
LDOVDD
20200323: remove colay
X_ESD-MLVS0402L04
Closed Codec
SENSE_A
SENSE_B
FRONT_JD
LINE1_JD
MIC1_JD
SURR_JD
CEN_JD
CEN/BAS
LIN_IN
SURR
LIN_OUT
SPDIFO1
MIC1
N58-25F0451-L06
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JAUD1
MIC
MICPWR
FLINE OUTR
HPON
FLINE OUTL
GND
PRESENCE#
LINE NEXT R
LINE NEXT L
H2X5[8]M
N31-2051411-H06
32 MIC2_L
32 MIC2_R
32 SENSE_C
MIC2_L
MIC2_R
LINE2_R
LINE2_L
RA40 75R/4
RA42 75R/4
RA46 75R/4
RA48 47R/4
RA50 75R/4
F_MIC2_L
F_MIC2_R
F_LINE2_R
F_LINE2_L
HPON
MIC2_JD
LINE2_JD
CA37
1000p50X/4
RA49
39.2K1%/4
RA47
20K1%/4
Close to Front panel
For HDA/AC97 front cable.
32 MIC2_VREFO
32 LINE2_VREFO
DA4
DA3
S-BAT54A
F_MIC_2L
F_MIC_2R
F_LINE_2L
F_LINE_2R
RA41 4.7K/4
RA43 4.7K/4
RA39 4.7K/4
RA38 4.7K/4
F_MIC2_L
F_MIC2_R
F_LINE2_L
F_LINE2_R
DA8
DA6
DA5
DA7
ESD-MLVS0402L04
D0G-2710510-I05
Close to Front panel
ESD protect
D0G-2710510-I05
AVL:D0G-2950500-SI0
RA51 22K/4
RA44 22K/4
RA52 22K/4
RA45 22K/4
De-POP circuit
20200224 remove de-pop circuit.
20200318 0R change to SPD.
32 ALOUT_R
32 ALOUT_L
32 ASROUT_R
32 ASROUT_L
32 ACEN_OUT
32 ABASS
32 ALINE2_R
32 ALINE2_L
RA31 X R/4
RA32 X R/4
RA28 X R/4
RA30 X R/4
RA20 X R/4
RA21 X R/4
RA37 X R/4
RA36 X R/4
LOUT_R 32
LOUT_L 32
SROUT_R 32
SROUT_L 32
CEN_OUT 32
BASS 32
LINE2_R
LINE2_L

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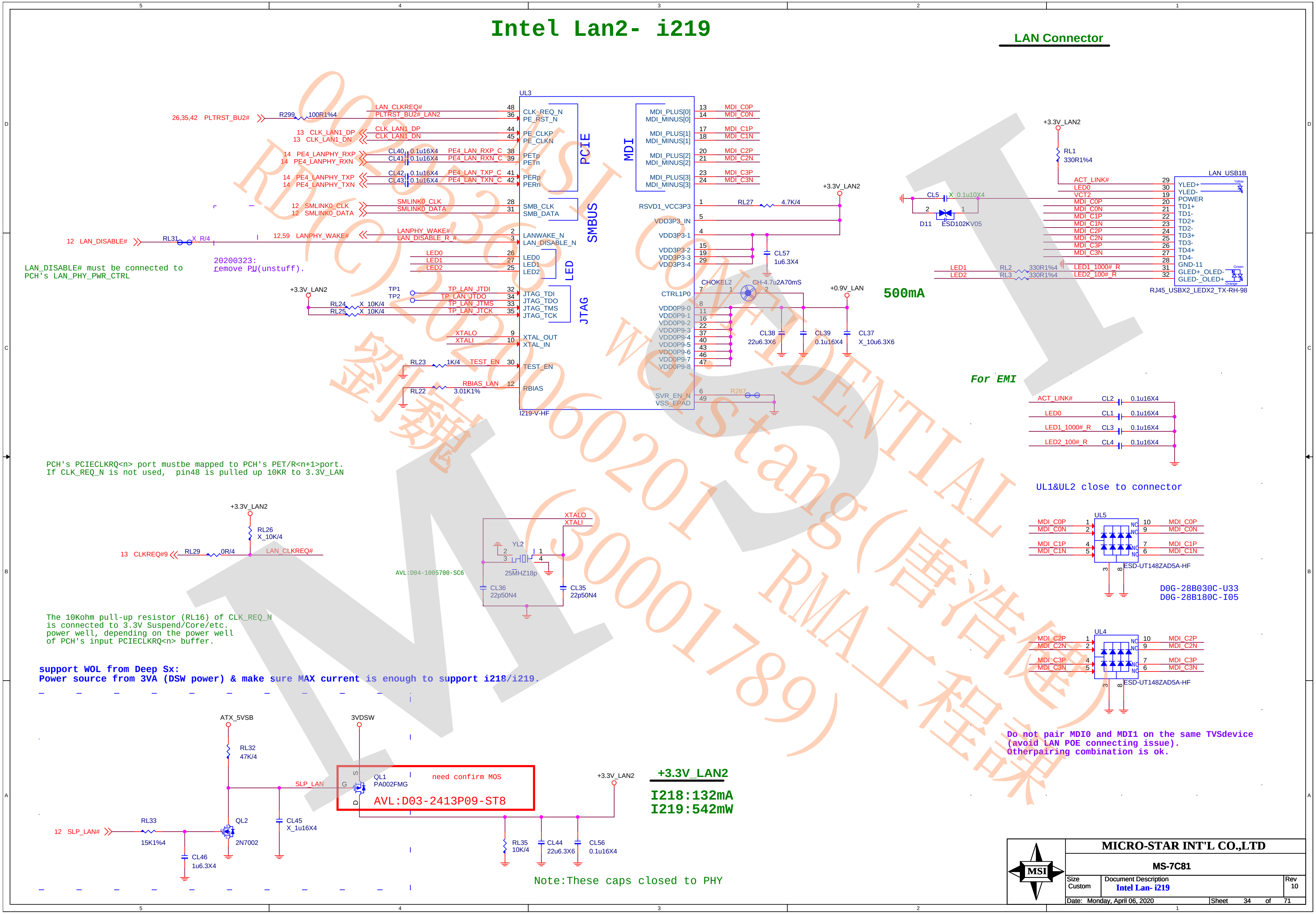
Intel Lan2- i219
LAN Connector
UL3
I219-V-HF
CLK_REQ_N
PE_RST_N
PE_CLKP
PE_CLKN
PETp
PETn
PERp
PERn
PCIE
MDI
MDI_PLUS[0]
MDI_MINUS[0]
MDI_PLUS[1]
MDI_MINUS[1]
MDI_PLUS[2]
MDI_MINUS[2]
MDI_PLUS[3]
MDI_MINUS[3]
SMB_CLK
SMB_DATA
SMBUS
LANWAKE_N
LAN_DISABLE_N
LED0
LED1
LED2
LED
JTAG_TDI
JTAG_TDO
JTAG_TMS
JTAG_TCK
JTAG
XTAL_OUT
XTAL_IN
TEST_EN
RBIAS
RSVD1_VCC3P3
VDD3P3_IN
VDD3P3-1
VDD3P3-2
VDD3P3-3
VDD3P3-4
CTRL1P0
VDD0P9-0
VDD0P9-1
VDD0P9-2
VDD0P9-3
VDD0P9-4
VDD0P9-5
VDD0P9-6
VDD0P9-7
VDD0P9-8
SVR_EN_N
VSS_EPAD
26,35,42 PLTRST_BU2#
R299 100R1%4
LAN_CLKREQ#
PLTRST_BU2#_LAN2
13 CLK_LAN1_DP
13 CLK_LAN1_DN
14 PE4_LANPHY_RXP
14 PE4_LANPHY_RXN
CL40 0.1u16X4
CL41 0.1u16X4
PE4_LAN_RXP_C
PE4_LAN_RXN_C
14 PE4_LANPHY_TXP
14 PE4_LANPHY_TXN
CL42 0.1u16X4
CL43 0.1u16X4
PE4_LAN_TXP_C
PE4_LAN_TXN_C
12 SMLINK0_CLK
12 SMLINK0_DATA
12 LAN_DISABLE#
RL31 X_R/4
12,59 LANPHY_WAKE#
LANPHY_WAKE#
LAN_DISABLE_R_#
LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL
20200323: remove PU(unstuff).
+3.3V_LAN2
TP1
TP2
RL24 X_10K/4
RL25 X_10K/4
TP_LAN_JTDI
TP_LAN_JTDO
TP_LAN_JTMS
TP_LAN_JTCK
XTALO
XTALI
RL23 1K/4 TEST_EN
RL22 3.01K1% RBIAS_LAN
MDI_C0P
MDI_C0N
MDI_C1P
MDI_C1N
MDI_C2P
MDI_C2N
MDI_C3P
MDI_C3N
RL27 4.7K/4
CL57 1u6.3X4
CHOKEL2 CH-4.7u2A70mS
+0.9V_LAN
500mA
CL38 22u6.3X6
CL39 0.1u16X4
CL37 X_10u6.3X6
R287
RL1 330R1%4
LAN_USB1B
CL5 X_0.1u10X4
D11 ESD102KV05
ACT_LINK#
VCT2
LED1
LED2
RL2 330R1%4
RL3 330R1%4
LED1_1000#_R
LED2_100#_R
YLED+
YLED-
POWER
TD1+
TD1-
TD2+
TD2-
TD3+
TD3-
TD4+
TD4-
GND-11
GLED+_OLED-
GLED-_OLED+
RJ45_USBX2_LEDX2_TX-RH-98
For EMI
CL2 0.1u16X4
CL1 0.1u16X4
CL3 0.1u16X4
CL4 0.1u16X4
UL1&UL2 close to connector
UL5
ESD-UT148ZAD5A-HF
D0G-28B030C-U33
D0G-28B180C-I05
UL4
ESD-UT148ZAD5A-HF
Do not pair MDI0 and MDI1 on the same TVSdevice (avoid LAN POE connecting issue). Otherpairing combination is ok.
PCH's PCIECLKRQ<n> port mustbe mapped to PCH's PET/R<n+1>port. If CLK_REQ_N is not used, pin48 is pulled up 10KR to 3.3V_LAN
RL26 X_10K/4
13 CLKREQ#9
RL29 0R/4
LAN_CLKREQ#
YL2
25MHZ18p
AVL:D04-1005700-SC6
CL36 22p50N4
CL35 22p50N4
The 10Kohm pull-up resistor (RL16) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.
support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.
ATX_5VSB
3VDSW
RL32 47K/4
QL1 PA002FMG
need confirm MOS
AVL:D03-2413P09-ST8
SLP_LAN
12 SLP_LAN#
RL33 15K1%4
QL2 2N7002
CL45 X_1u16X4
CL46 1u6.3X4
RL35 10K/4
CL44 22u6.3X6
CL56 0.1u16X4
+3.3V_LAN2
I218:132mA
I219:542mW
Note:These caps closed to PHY
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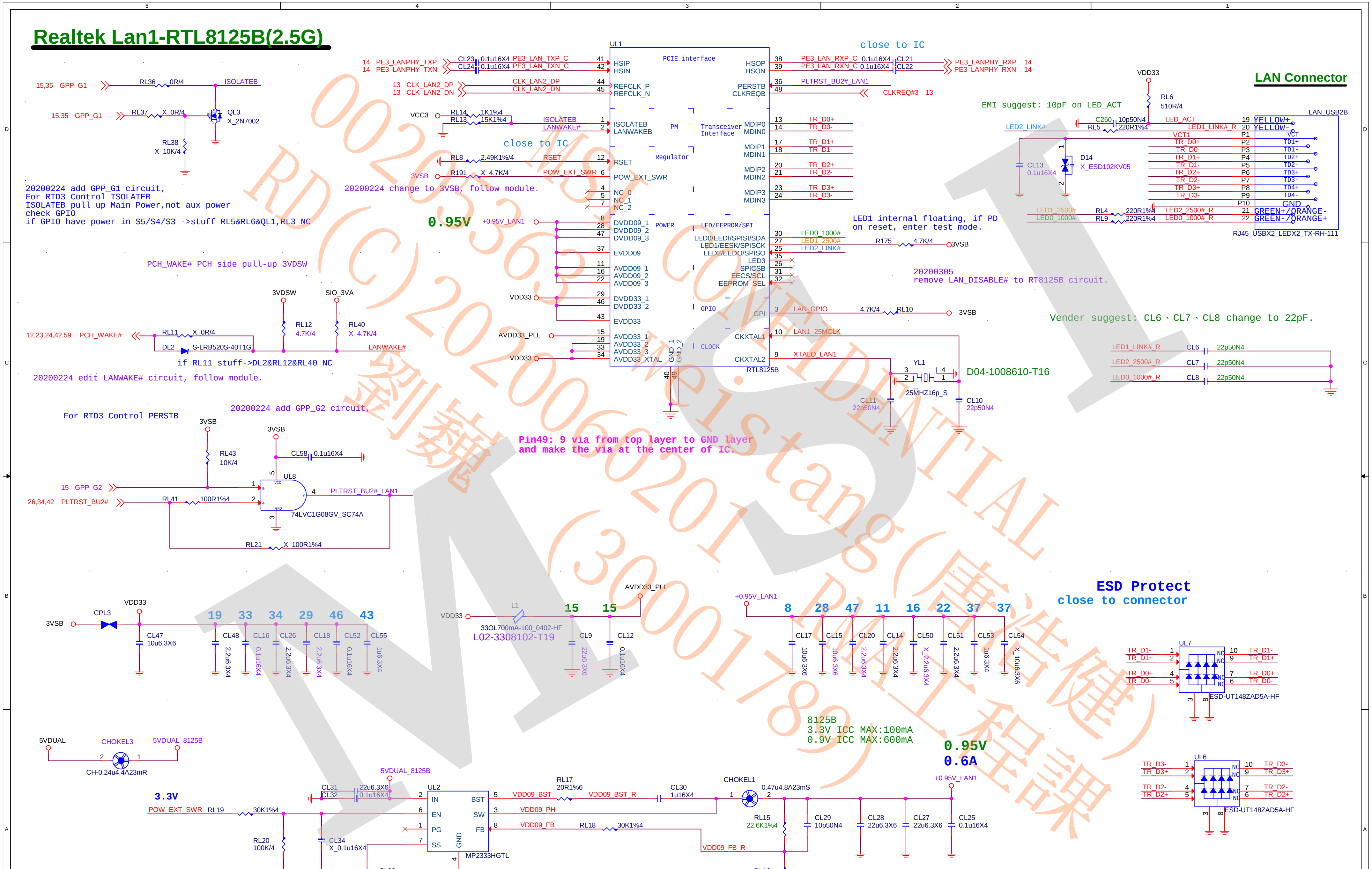
Realtek Lan1-RTL8125B(2.5G)



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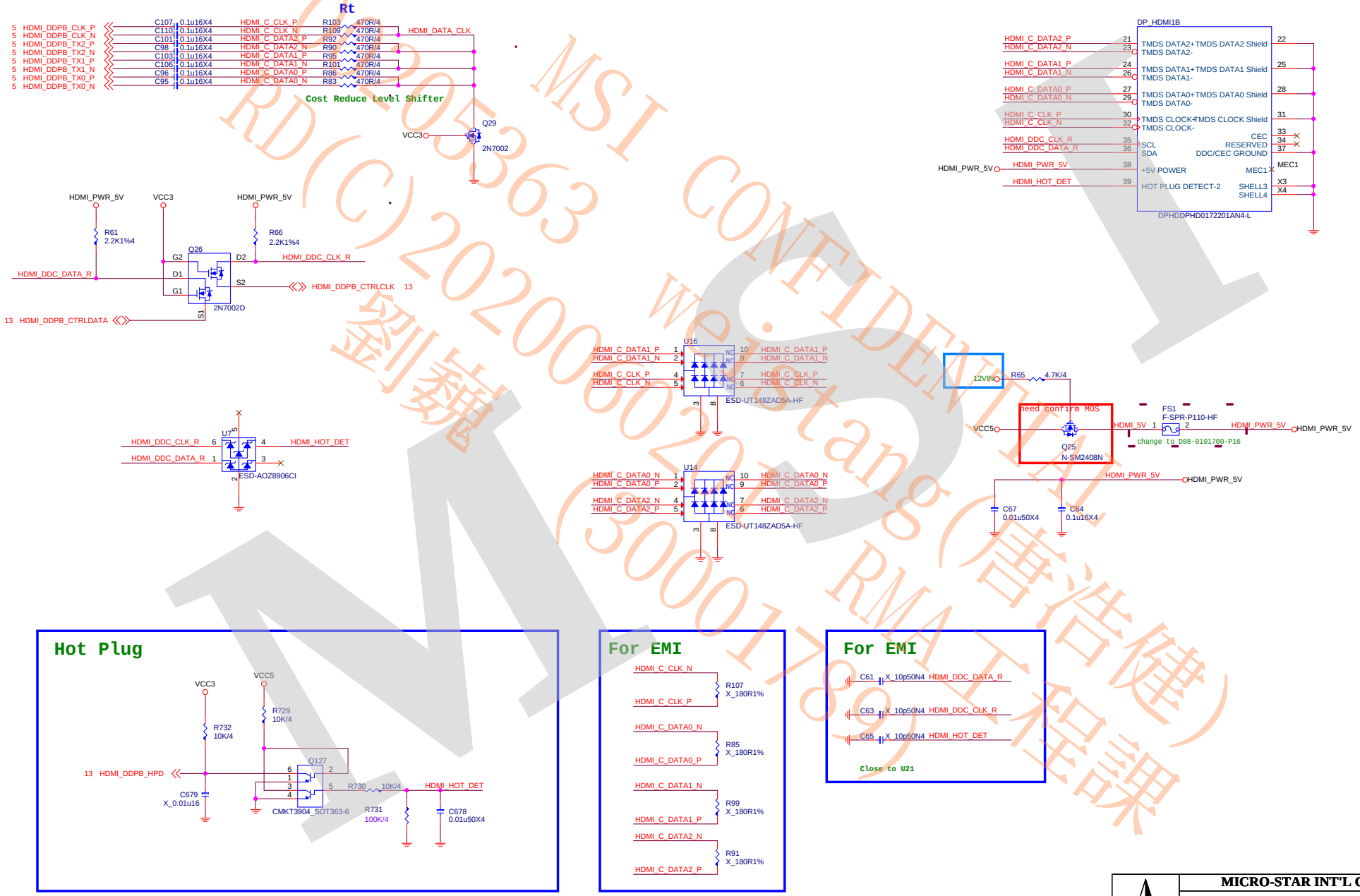
HDMI 1.4b

HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



0B版可以考慮是否刪除這4顆電阻

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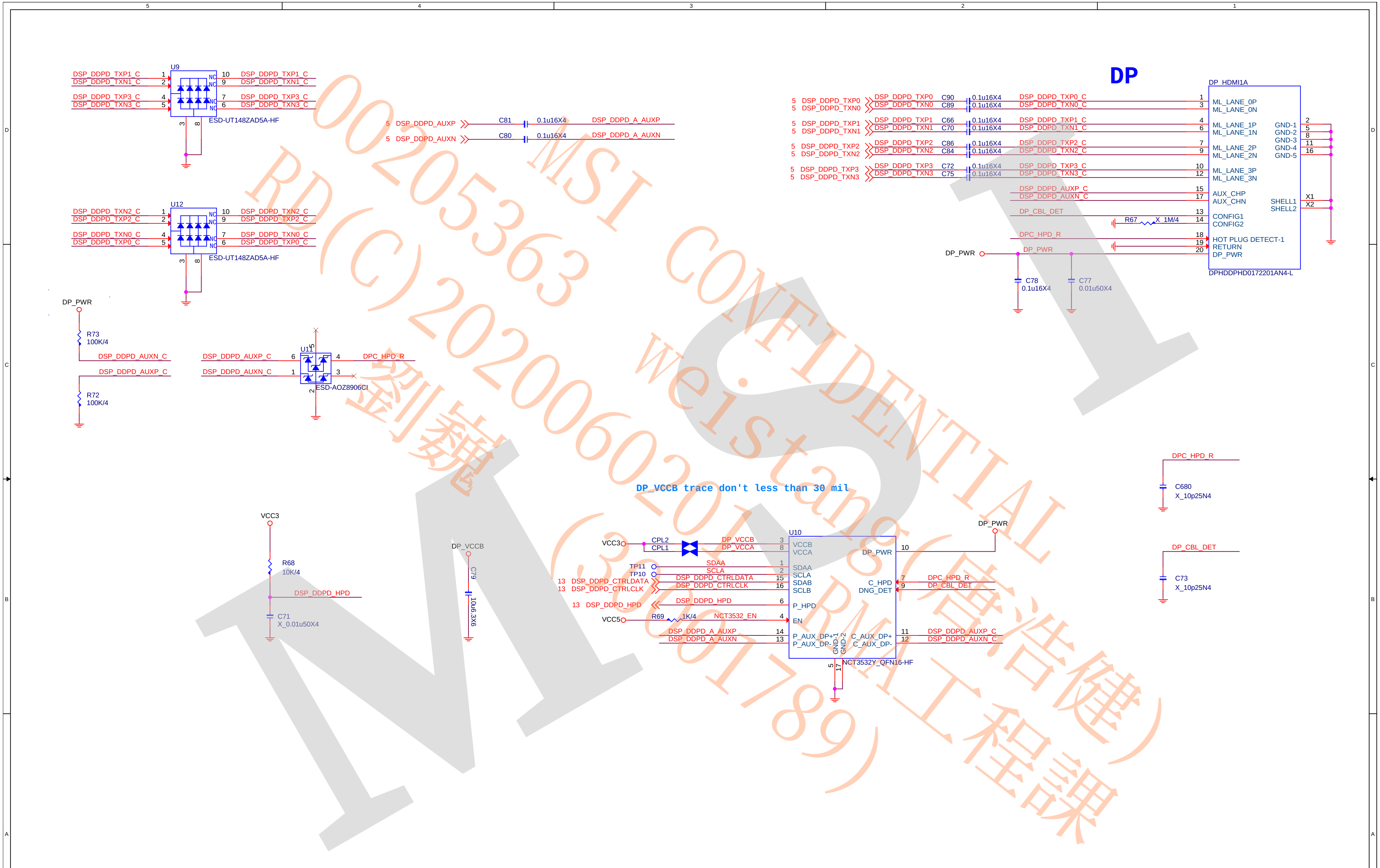

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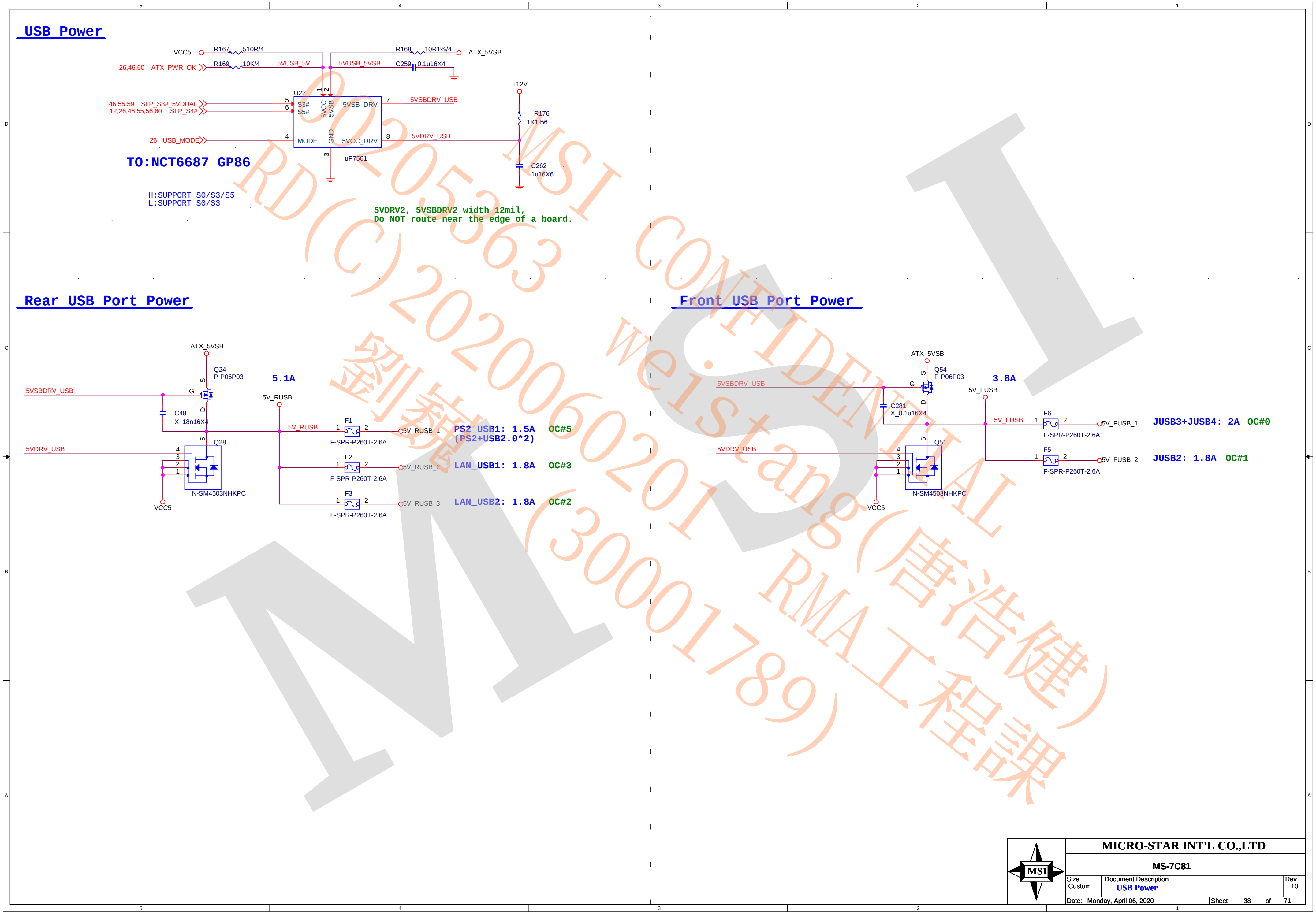
USB Power
VCC5
R167 510R/4
R168 10R1%/4
ATX_5VSB
26,46,60 ATX_PWR_OK
R169 10K/4
5VUSB_5V
5VUSB_5VSB
C259 0.1u16X4
+12V
U22
46,55,59 SLP_S3#_5VDUAL
12,26,46,55,56,60 SLP_S4#
S3#
S5#
5VCC
5VSB
5VSB_DRV
5VSBDRV_USB
R176
1K1%6
26 USB_MODE
MODE
GND
5VCC_DRV
5VDRV_USB
uP7501
C262
1u16X6
TO:NCT6687 GP86
H:SUPPORT S0/S3/S5
L:SUPPORT S0/S3
5VDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.
Rear USB Port Power
ATX_5VSB
Q24
P-P06P03
5.1A
5VSBDRV_USB
C48
X_18n16X4
5V_RUSB
Q28
5VDRV_USB
N-SM4503NHKPC
VCC5
F1
F-SPR-P260T-2.6A
5V_RUSB_1
PS2_USB1: 1.5A OC#5
(PS2+USB2.0*2)
F2
F-SPR-P260T-2.6A
5V_RUSB_2
LAN_USB1: 1.8A OC#3
F3
F-SPR-P260T-2.6A
5V_RUSB_3
LAN_USB2: 1.8A OC#2
Front USB Port Power
ATX_5VSB
Q54
P-P06P03
3.8A
5VSBDRV_USB
5V_FUSB
C281
X_0.1u16X4
F6
F-SPR-P260T-2.6A
5V_FUSB_1
JUSB3+JUSB4: 2A OC#0
Q51
5VDRV_USB
N-SM4503NHKPC
VCC5
F5
F-SPR-P260T-2.6A
5V_FUSB_2
JUSB2: 1.8A OC#1
MSI
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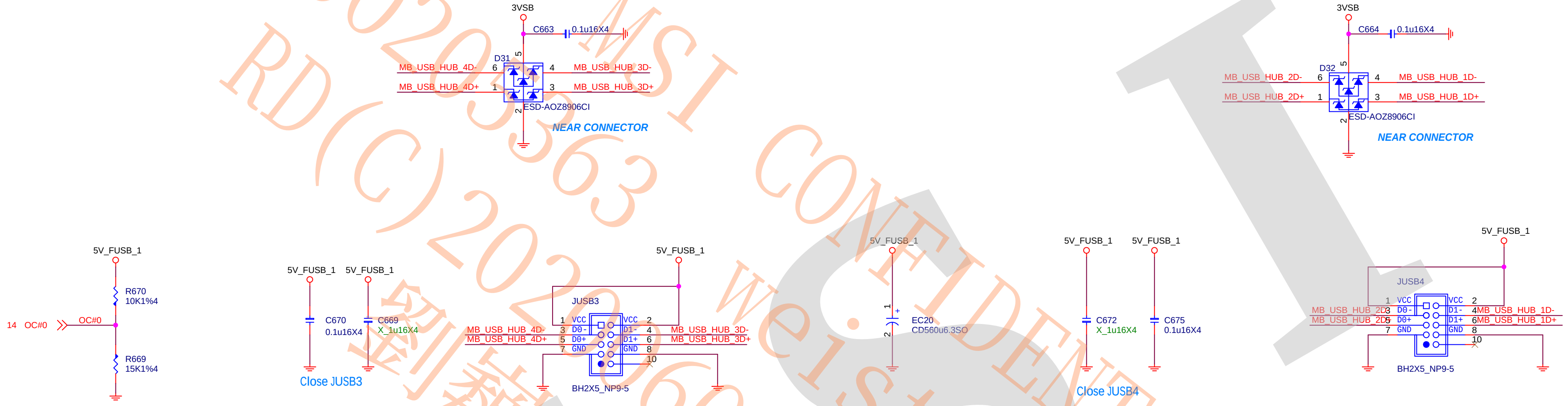
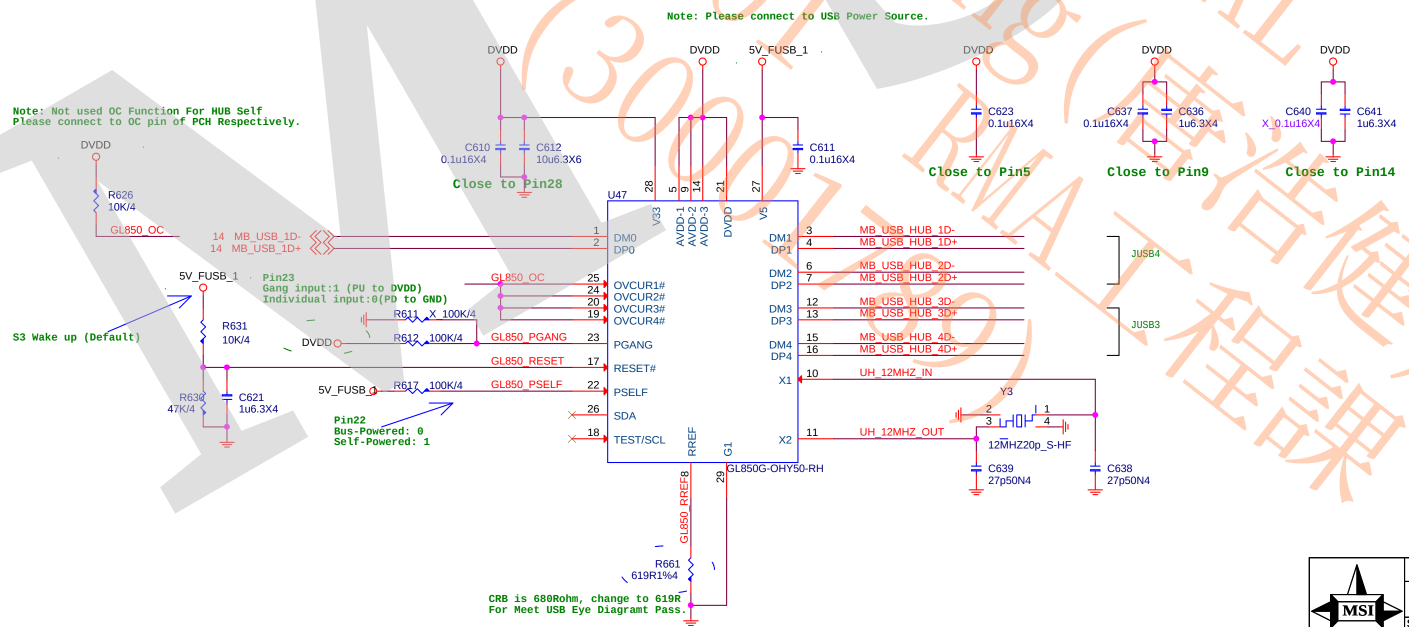
Front USB2.0



GL850G USB2.0 HUB



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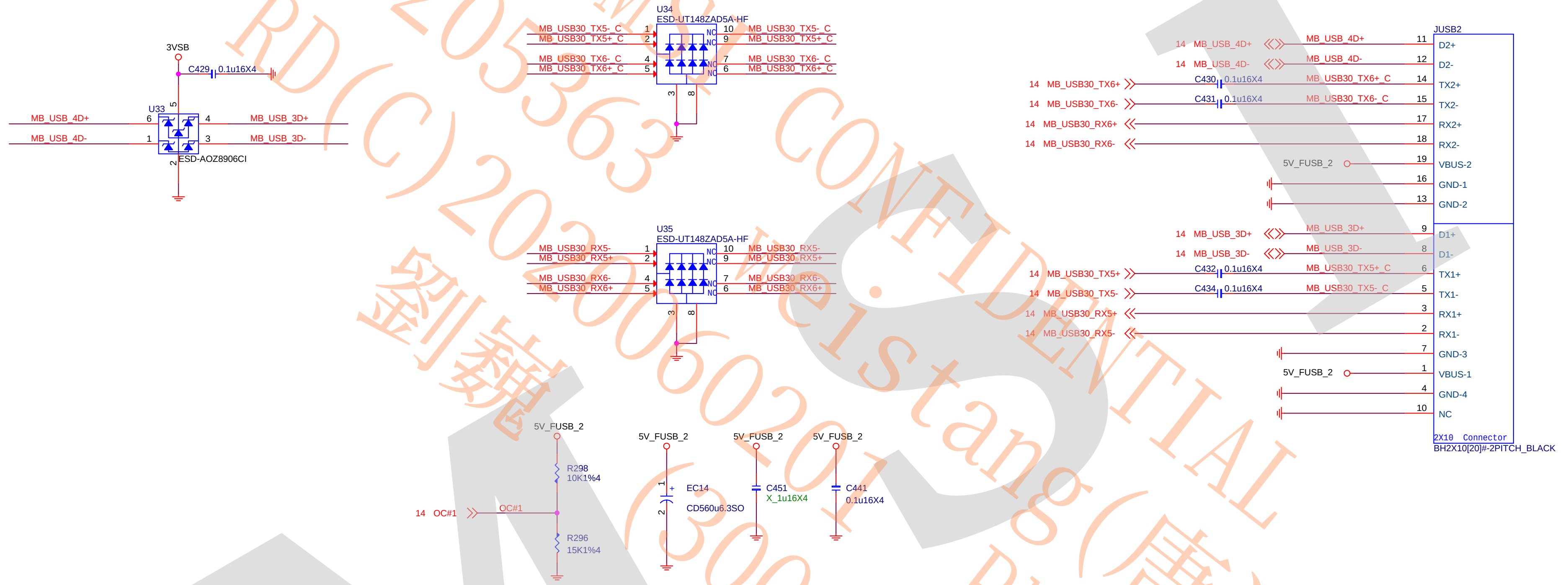
Front USB3.1 Gen1



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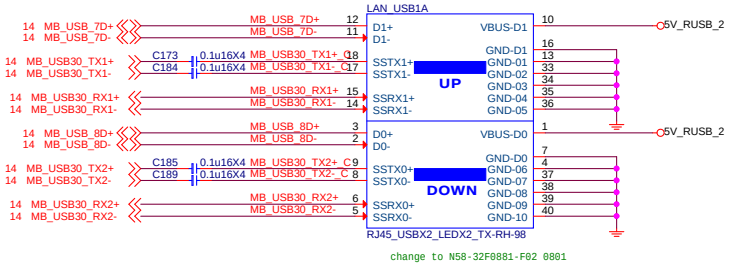
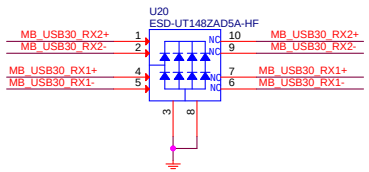
Rear LAN USB3.1 Gen2

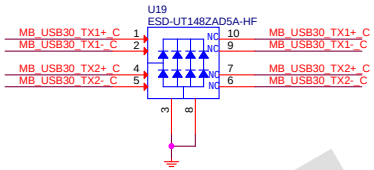
i219

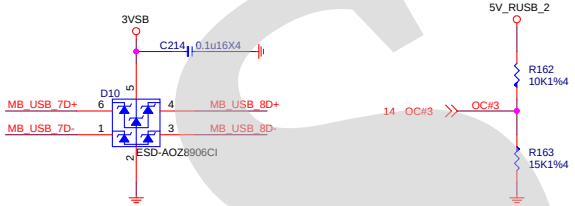
1.8A

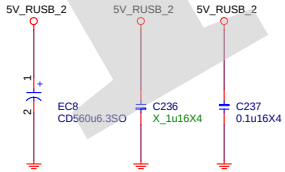


change to N58-32F0881-F02 0801



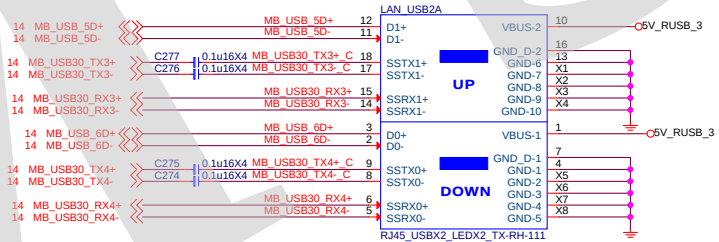


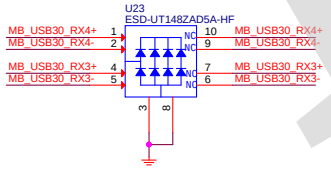


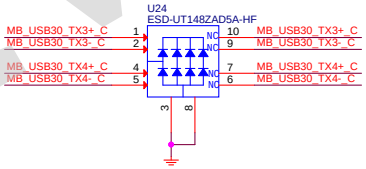


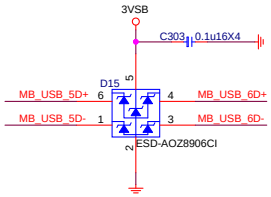
Rear LAN1 USB3.1 Gen1

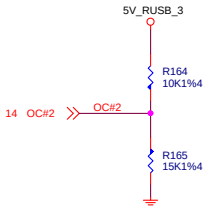
RTL8125B-2.5G

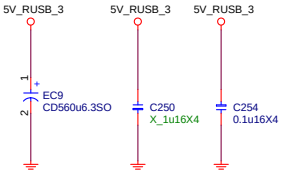












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Power On Sequence Timing Specification for Asynchronous mode

Symbols	Parameter	Min	Typ	Max	Unit	Remark
V_{TH_POR}	Threshold voltage for PORST# pins	1.38	1.6	1.8	V	Use 0.22uF cap for GEN3 , Gen2 use 0.1uf by Upstream SPEC
t_{OCI}	OCI# ready after Suspend Power Ready			12	ms	
t_{VSR}	Rising time for Suspend and normal Power Ready			10	ms	
t_{VNRDY}	Timing for all normal power Ready	50			ms	Note 1
t_{PORST1}	Timing for all normal Power Ready to Power On Reset (when suspend power domains are existed)	10		80	ms	
	Timing for all normal Power Ready to Power On Reset (when suspen powers connect to normal power directly)	60		80	ms	

CLK Rule (Follow SB PDG)

PCIE Rule (Follow SB PDG)

USB SS (80Ohm-Diff)
USB HS (90Ohm-Diff)

Layout Guide:
1.) USB3.1 to Connector Total Length < 1.5"
2.) VIA hole <2

LED function optional

SMD Crystal use 3225 size
M:D04-0900900-SC6
S:D04-0901100-T16
S:D04-0901200-F07

X0/XI (95hm-Diff,Spacing 30mil)

SMI connect to GPI which support smi function.
SB side pull high 10K ohm to 3VSB.
(Intel 8X & 9X series use GPIO10)
(Intel SKL use GPP_C23)
ASM_SMI has internal Pull-up to VCC
ASM_WAKE has internal Pull-up to VCCSUS

EEPROM

M:M31-25L1022-M24 (1M)
S:M31-25X2023-W03 (2M)

M:L01-0107118-M26
S:L01-0107108-C08

Power Consumption

	3.3V	3.3VSUS	2.5V	1.05V	1.05VSUS	Unit
ASM3241	10	10	400	850	20	mA

ASM3241 2.5v Analog Power

ASM3241 1.05v Suspend Power

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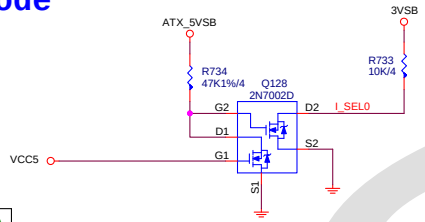
Current Mode

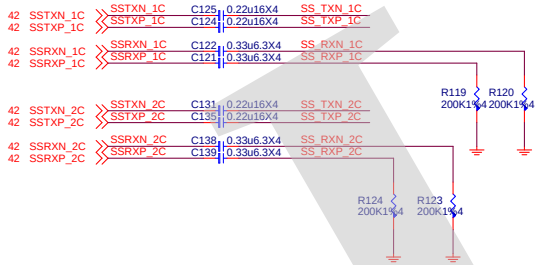
3A under S0 mode
1.5A under S3 mode



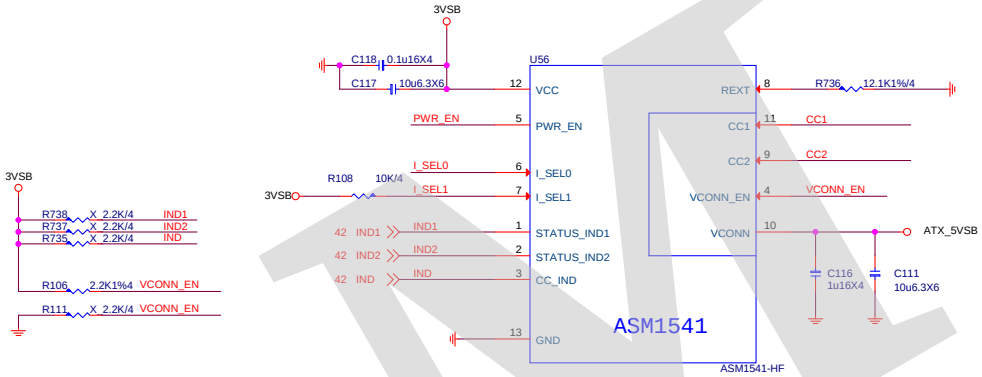
I_SEL0 : I_SEL1

X	0	~~Default for 900mA~~
0	1	1.5A @5V
1	1	3A @5V

1.5A under S3 mode
3A under S0 mode

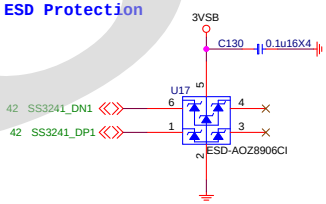


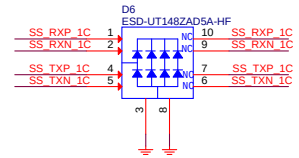
USB 3.2-Type-C

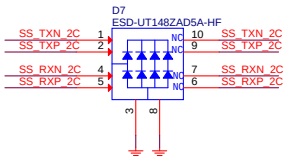


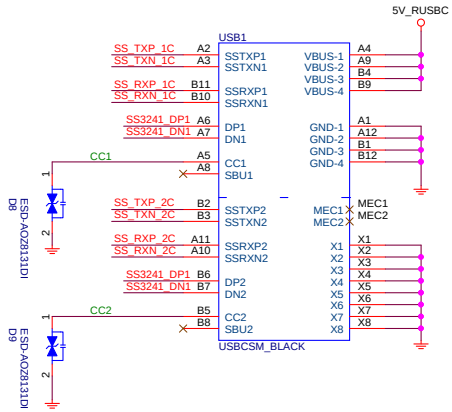
TYPE-C

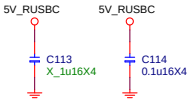
ESD Protection



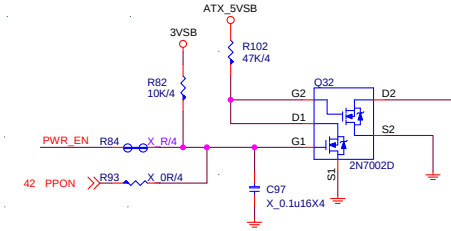




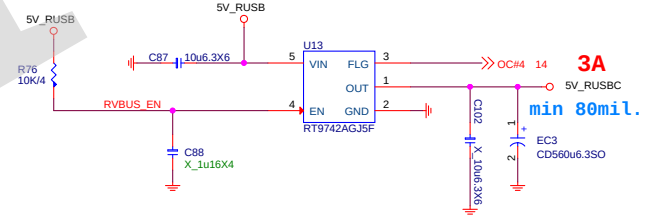




VCONN OC#



VBUS OC#



PPON internal PU 3.3V, change to PU 3VSB.

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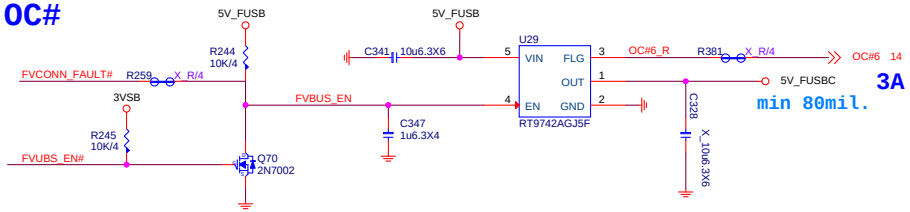
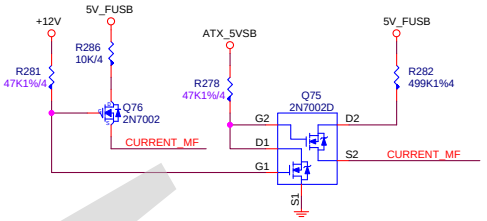
VCONN OC#



Current Mode

3A under S0 mode
1.5A under S3 mode



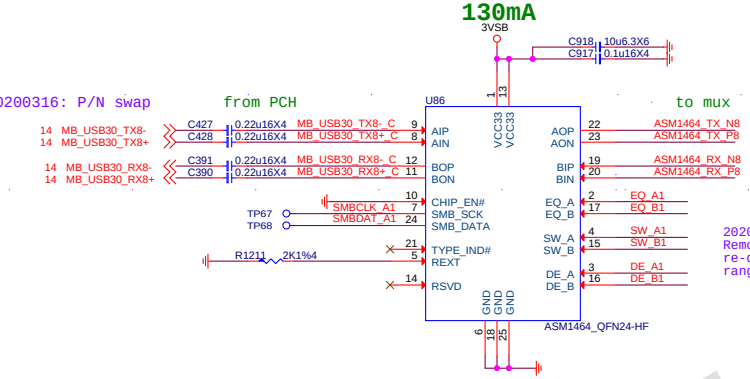
CURRENT_MF
L - Default for 900mA
M - Mid (500K) for 1.5A
H - High (10K) for 3A

Rear USB3.1 Redriver

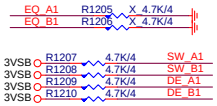
20200224 Add USB3.0 re-driver

130mA

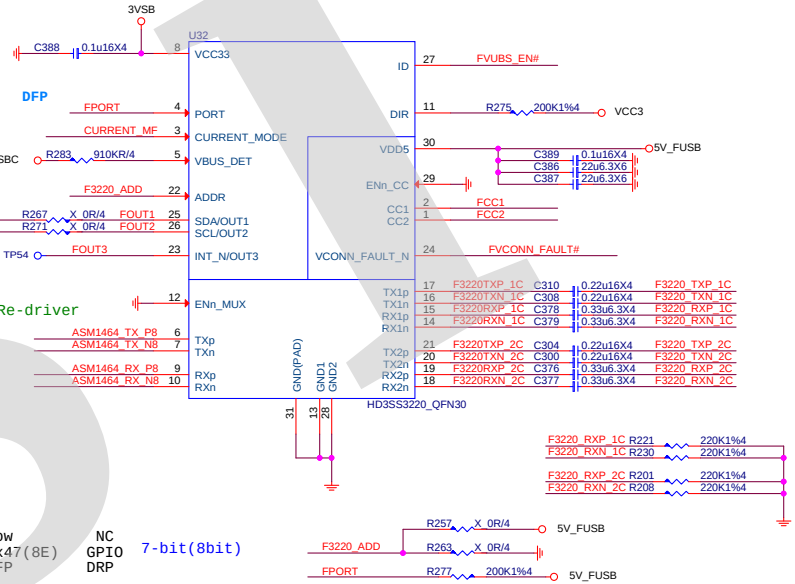
20200316: P/N swap



20200313:
Remove C919、C920、C921、C922, re-driver common voltage in mux range.

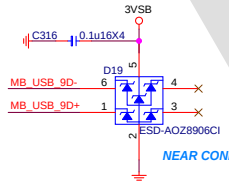


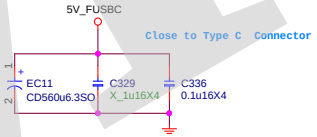
USB Type-C MUX with Configuration Channel (CC)

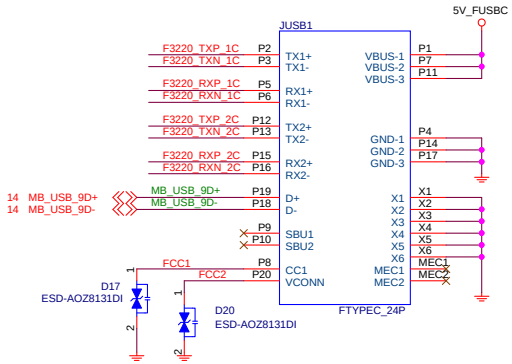


F3220_ ADD	High	Low	NC	7-bit(8bit)
FPORT	0x67(CE) DFP(V)	0x47(8E) UFP	GPIO DRP	

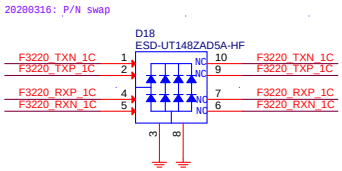
TYPE-C



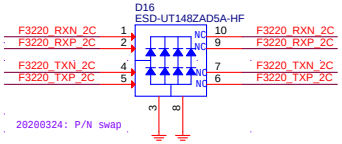




20200316: P/N swap



20200316: P/N swap



20200324: P/N swap

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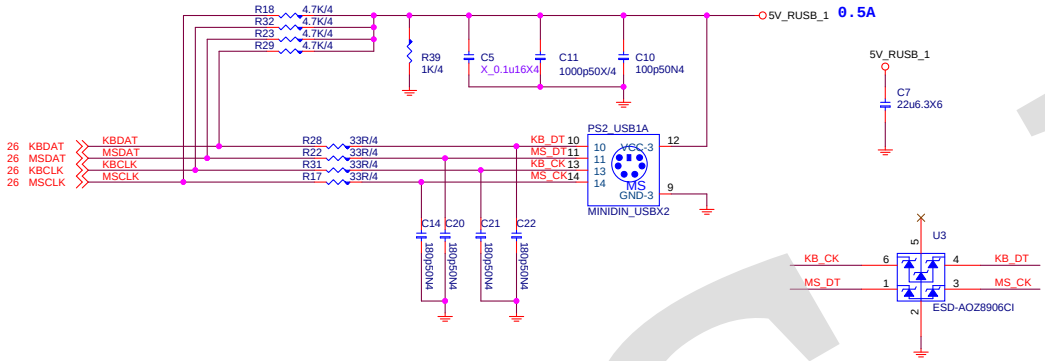
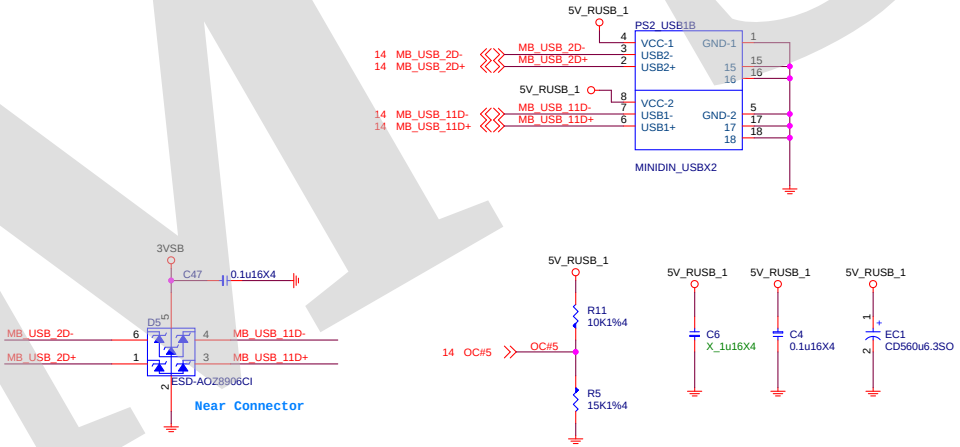
PS2 Keyboard & Mouse Connector



PS2 USB2.0



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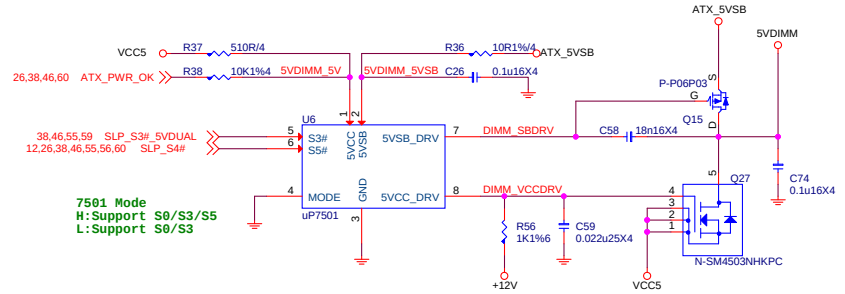
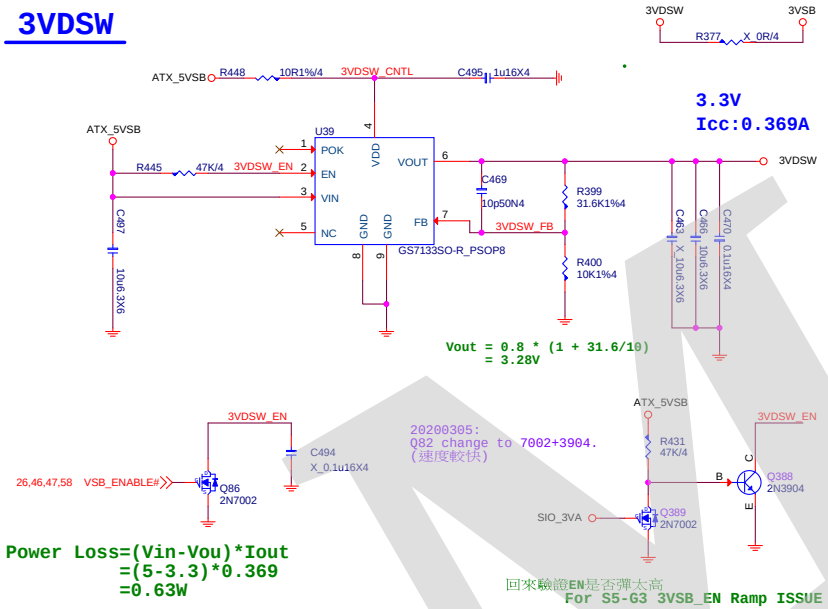
5VDIMM FOR DDR

9.831A



3VDSW

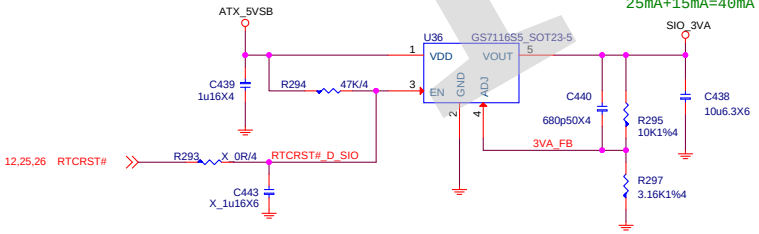


Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.369
=0.63W

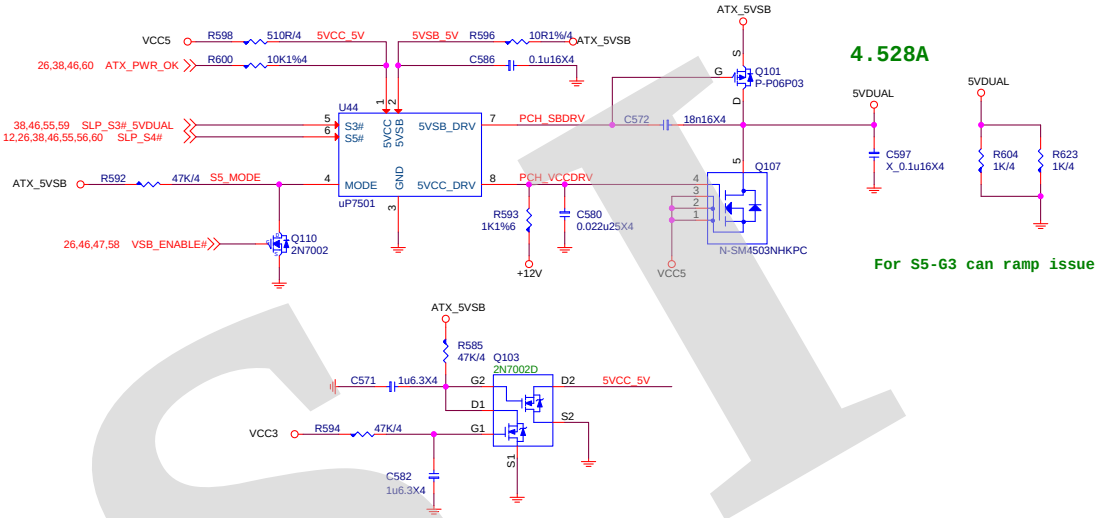
SIO_3VA

Power Loss=(Vin-Vou)*Iout
=(5-3.3)*0.04
=1.7*0.04
=0.068W

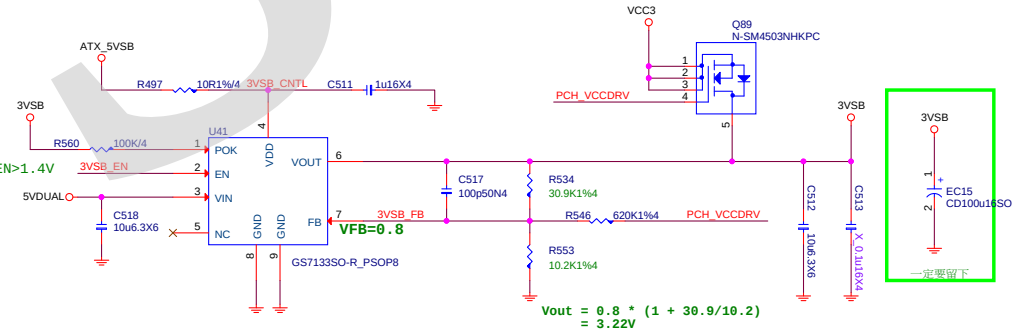
25mA+15mA=40mA

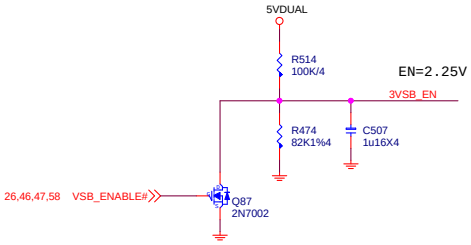


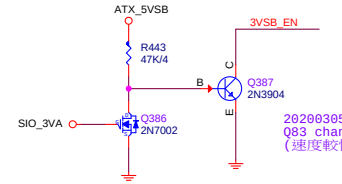
5VDUAL



3VSB







回來驗證EN是否彈太高

For S5-G3 3VSB_EN Ramp ISSUE

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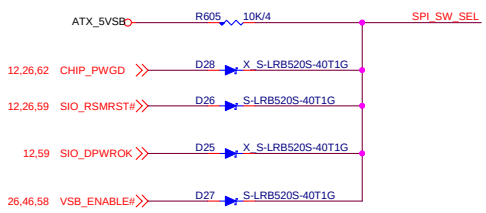
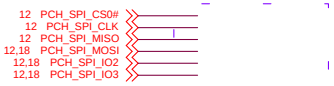
Module Stuff CHIP_PWGD,
But PCH_PWROK may ramp up before CHIP_PWGD.

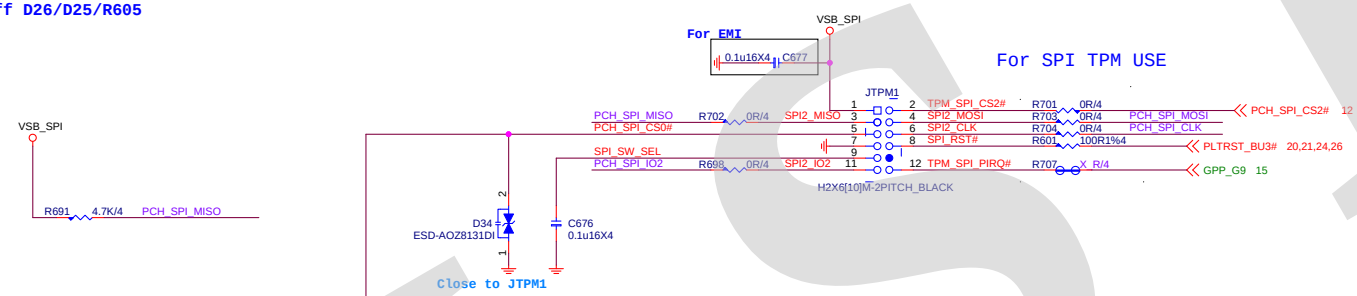


For TL624-1.
DEEP Mode : Stuff D26/R605
DSW Mode : Stuff D26/D25/R605



20200325: remove 0R

For SPI TPM USE



PDG: Serises resistor is 62 ohm for 3.3V.

Colay 32M footprint

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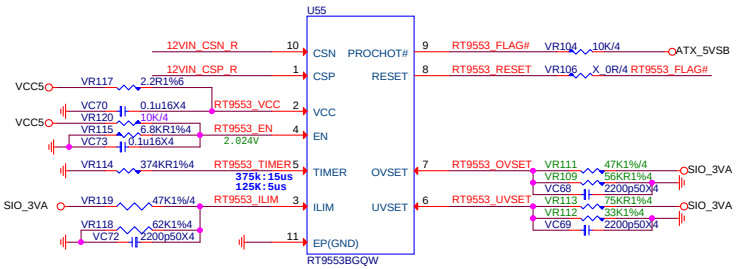
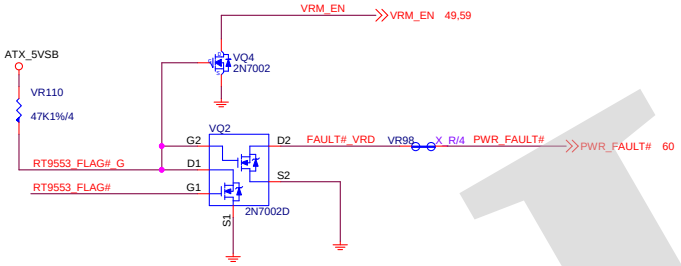
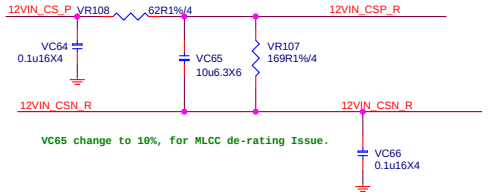
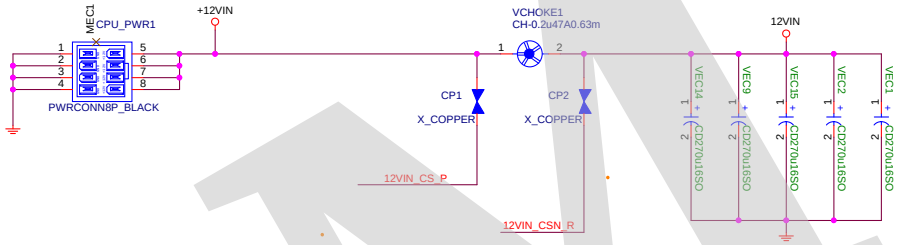
OCP: 45A For 10 core 210A Support








```
Vilim = 3.3V * 62KR / (62KR+47KR)
      =1.877V
Icsp = 0.43uA
OCP = [(62R + 169R) / 169R] * [1.877V / (100 * 0.63mR)] + [(0.43uA * 62R) / 0.63mR]
      = 45A
```



MICRO-STAR INT'L CO.,LTD		
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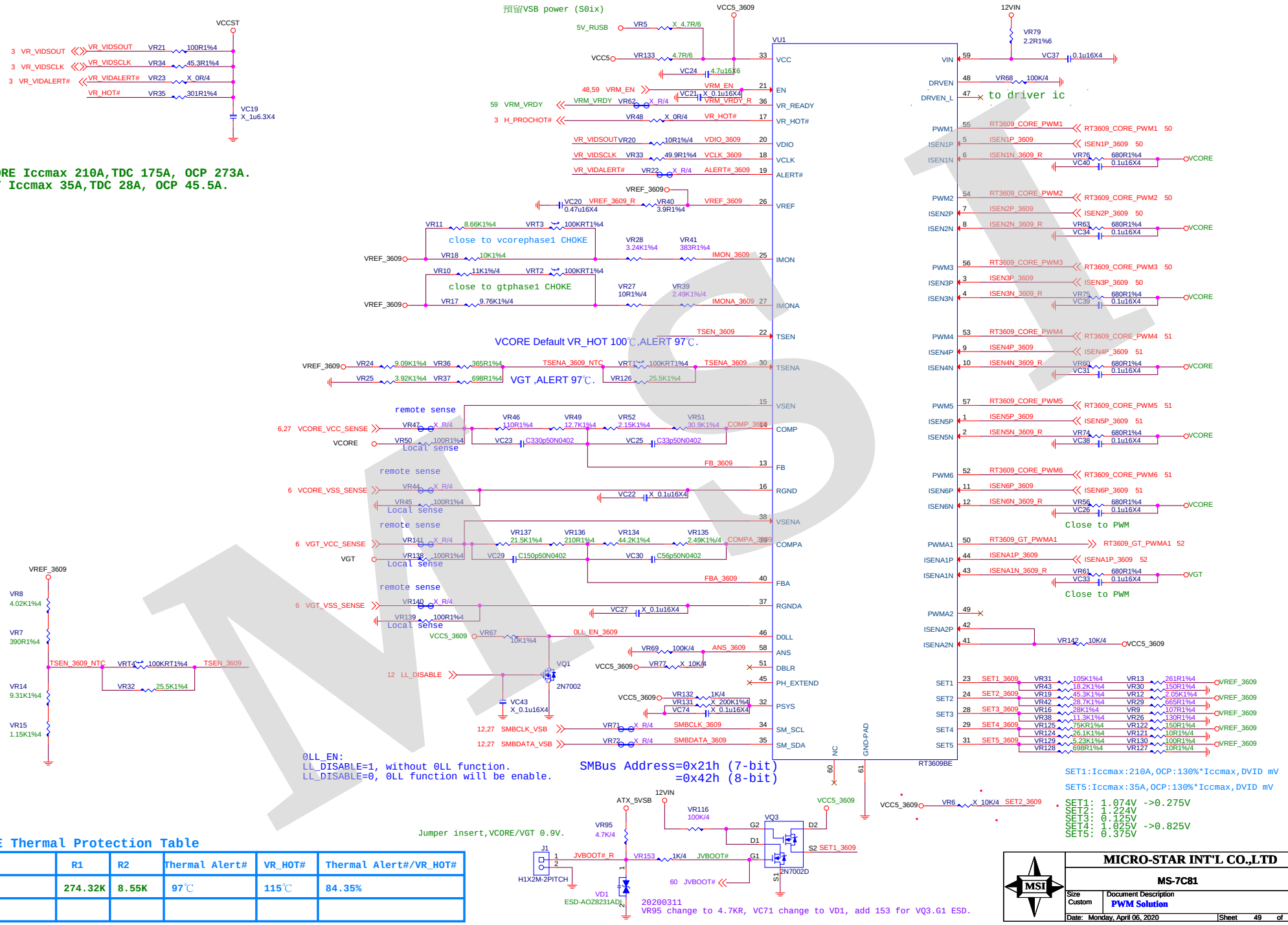

VCORE Thermal Protection Table

	R1	R2	Thermal Alert#	VR_HOT#	Thermal Alert#/VR_HOT#
	274.32K	8.55K	97℃	115℃	84.35%

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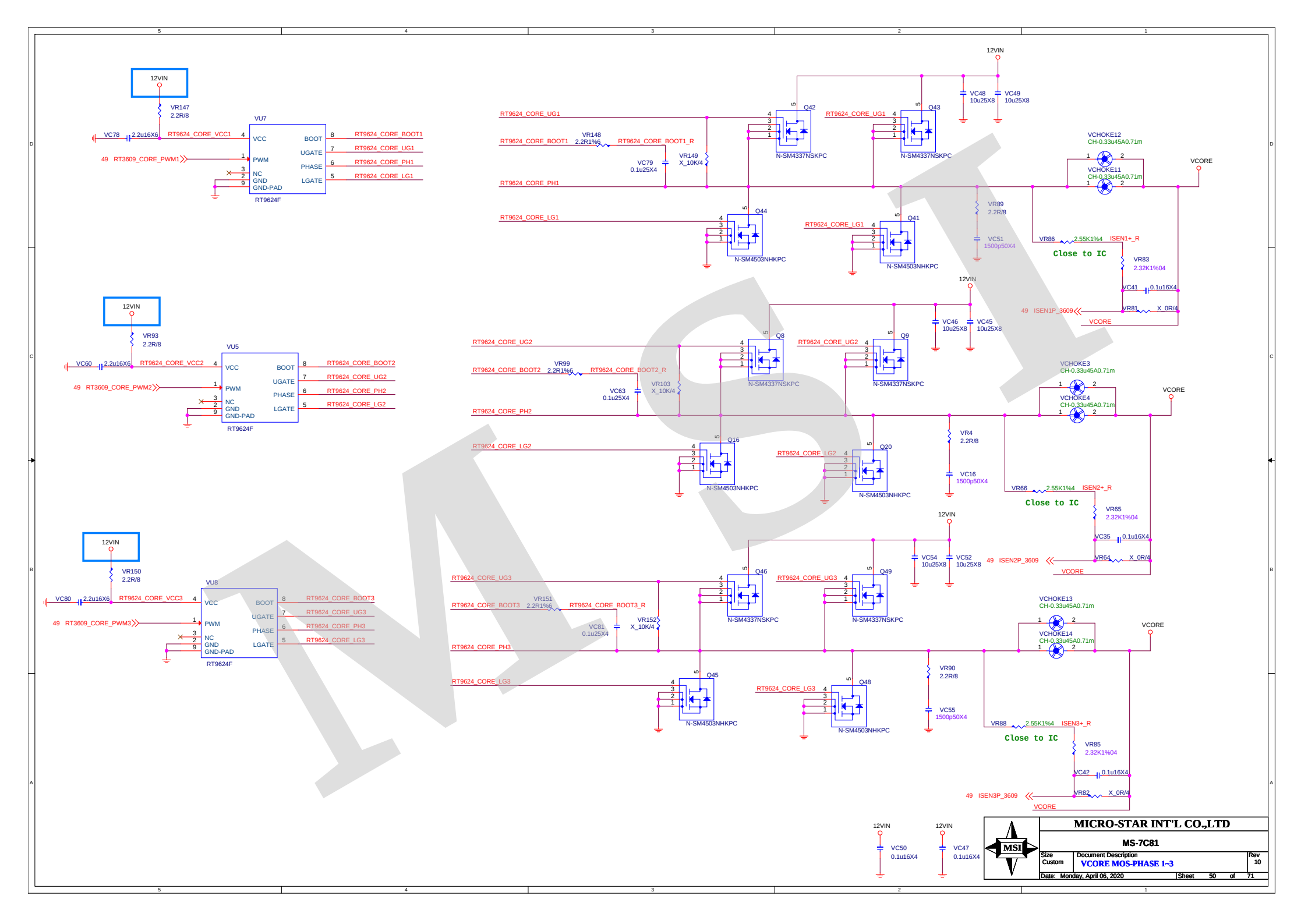
12VIN
VR147 2.2R/8
VC78 2.2u16X6
RT9624_CORE_VCC1
VU7
VCC
PWM
NC
GND
GND-PAD
BOOT
UGATE
PHASE
LGATE
RT9624F
49 RT3609_CORE_PWM1
RT9624_CORE_BOOT1
RT9624_CORE_UG1
RT9624_CORE_PH1
RT9624_CORE_LG1
VR148 2.2R1%6
RT9624_CORE_BOOT1_R
VC79 0.1u25X4
VR149 X_10K/4
Q42
Q43
Q44
Q41
N-SM4337NSKPC
N-SM4503NHKPC
VC48 10u25X8
VC49 10u25X8
VCHOKE12 CH-0.33u45A0.71m
VCHOKE11 CH-0.33u45A0.71m
VCORE
VR89 2.2R/8
VC51 1500p50X4
VR86 2.55K1%4
ISEN1+_R
Close to IC
VR83 2.32K1%04
VC41 0.1u16X4
VR81 X_0R/4
49 ISEN1P_3609
VR93 2.2R/8
VC60 2.2u16X6
RT9624_CORE_VCC2
VU5
RT9624_CORE_BOOT2
RT9624_CORE_UG2
RT9624_CORE_PH2
RT9624_CORE_LG2
49 RT3609_CORE_PWM2
VR99 2.2R1%6
RT9624_CORE_BOOT2_R
VC63 0.1u25X4
VR103 X_10K/4
Q8
Q9
Q16
Q20
VC46 10u25X8
VC45 10u25X8
VR4 2.2R/8
VC16 1500p50X4
VCHOKE3 CH-0.33u45A0.71m
VCHOKE4 CH-0.33u45A0.71m
VR66 2.55K1%4
ISEN2+_R
VR65 2.32K1%04
VC35 0.1u16X4
VR64 X_0R/4
49 ISEN2P_3609
VR150 2.2R/8
VC80 2.2u16X6
RT9624_CORE_VCC3
VU8
RT9624_CORE_BOOT3
RT9624_CORE_UG3
RT9624_CORE_PH3
RT9624_CORE_LG3
49 RT3609_CORE_PWM3
VR151 2.2R1%6
RT9624_CORE_BOOT3_R
VC81 0.1u25X4
VR152 X_10K/4
Q46
Q49
Q45
Q48
VC54 10u25X8
VC52 10u25X8
VR90 2.2R/8
VC55 1500p50X4
VCHOKE13 CH-0.33u45A0.71m
VCHOKE14 CH-0.33u45A0.71m
VR88 2.55K1%4
ISEN3+_R
VR85 2.32K1%04
VC42 0.1u16X4
VR82 X_0R/4
49 ISEN3P_3609
VC50 0.1u16X4
VC47 0.1u16X4
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Size Custom
Document Description
VCORE MOS-PHASE 1~3
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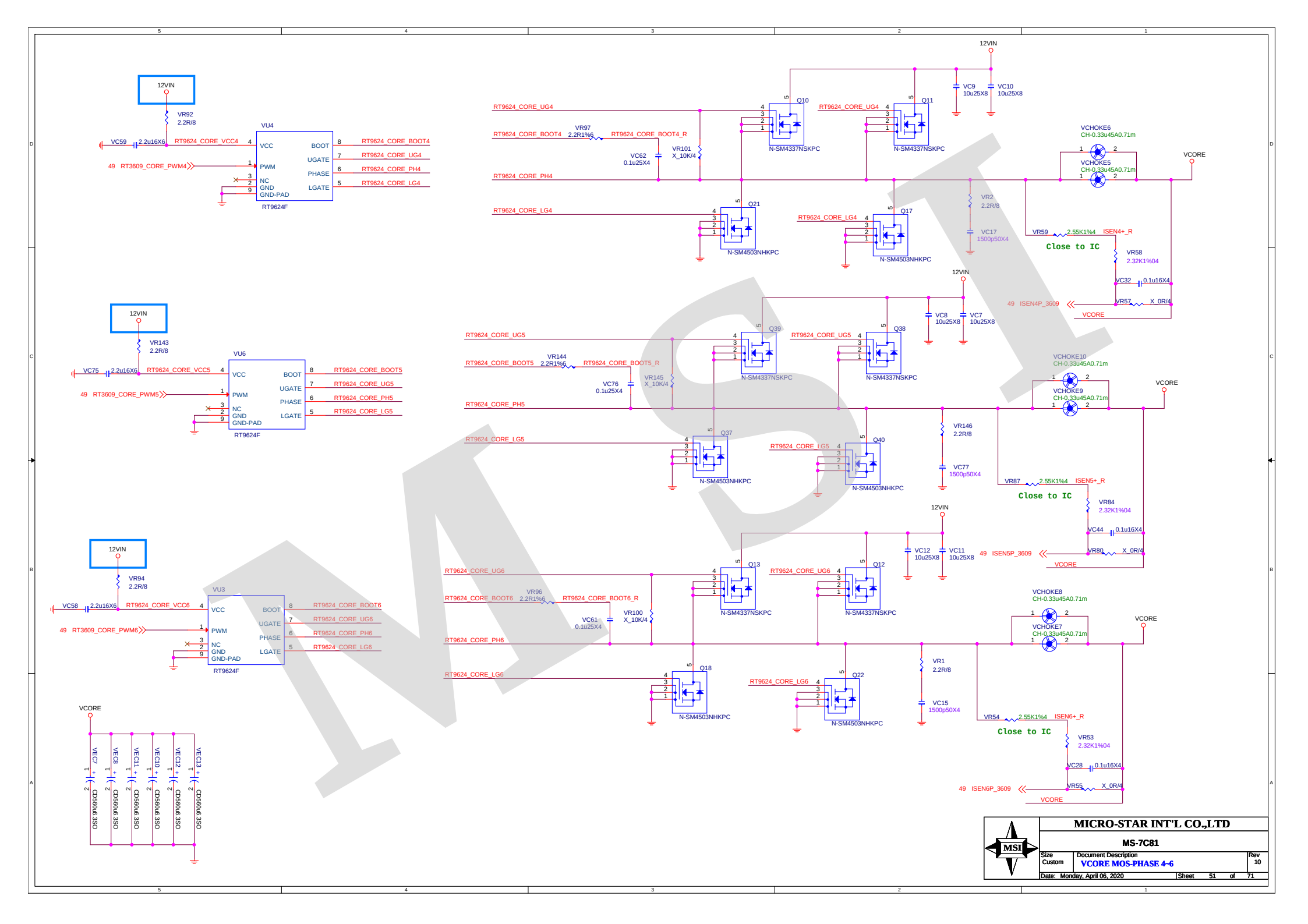
12VIN
VR92 2.2R/8
VU4
VC59 2.2u16X6
RT9624_CORE_VCC4
49 RT3609_CORE_PWM4
VCC
PWM
NC
GND
GND-PAD
BOOT
UGATE
PHASE
LGATE
RT9624_CORE_BOOT4
RT9624_CORE_UG4
RT9624_CORE_PH4
RT9624_CORE_LG4
RT9624F
VR143 2.2R/8
VU6
VC75 2.2u16X6
RT9624_CORE_VCC5
49 RT3609_CORE_PWM5
RT9624_CORE_BOOT5
RT9624_CORE_UG5
RT9624_CORE_PH5
RT9624_CORE_LG5
VR94 2.2R/8
VU3
VC58 2.2u16X6
RT9624_CORE_VCC6
49 RT3609_CORE_PWM6
RT9624_CORE_BOOT6
RT9624_CORE_UG6
RT9624_CORE_PH6
RT9624_CORE_LG6
VCORE
VEC7 CD560u6.3SO
VEC8 CD560u6.3SO
VEC11 CD560u6.3SO
VEC10 CD560u6.3SO
VEC12 CD560u6.3SO
VEC13 CD560u6.3SO
VR97 2.2R1%6
VR101 X_10K/4
VC62 0.1u25X4
Q10 N-SM4337NSKPC
Q11 N-SM4337NSKPC
Q21 N-SM4503NHKPC
Q17 N-SM4503NHKPC
VC9 10u25X8
VC10 10u25X8
VR2 2.2R/8
VC17 1500p50X4
VCHOKE6 CH-0.33u45A0.71m
VCHOKE5 CH-0.33u45A0.71m
VR59 2.55K1%4 ISEN4+_R
Close to IC
VR58 2.32K1%04
VC32 0.1u16X4
VR57 X_0R/4
49 ISEN4P_3609
VR144 2.2R1%6
VR145 X_10K/4
VC76 0.1u25X4
Q39 N-SM4337NSKPC
Q38 N-SM4337NSKPC
Q37 N-SM4503NHKPC
Q40 N-SM4503NHKPC
VC8 10u25X8
VC7 10u25X8
VCHOKE10 CH-0.33u45A0.71m
VCHOKE9 CH-0.33u45A0.71m
VR146 2.2R/8
VC77 1500p50X4
VR87 2.55K1%4 ISEN5+_R
VR84 2.32K1%04
VC44 0.1u16X4
VR80 X_0R/4
49 ISEN5P_3609
VR96 2.2R1%6
VR100 X_10K/4
VC61 0.1u25X4
Q13 N-SM4337NSKPC
Q12 N-SM4337NSKPC
Q18 N-SM4503NHKPC
Q22 N-SM4503NHKPC
VC12 10u25X8
VC11 10u25X8
VCHOKE8 CH-0.33u45A0.71m
VCHOKE7 CH-0.33u45A0.71m
VR1 2.2R/8
VC15 1500p50X4
VR54 2.55K1%4 ISEN6+_R
VR53 2.32K1%04
VC28 0.1u16X4
VR55 X_0R/4
49 ISEN6P_3609
MICRO-STAR INT'L CO.,LTD
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VCORE MOS-PHASE 4~6
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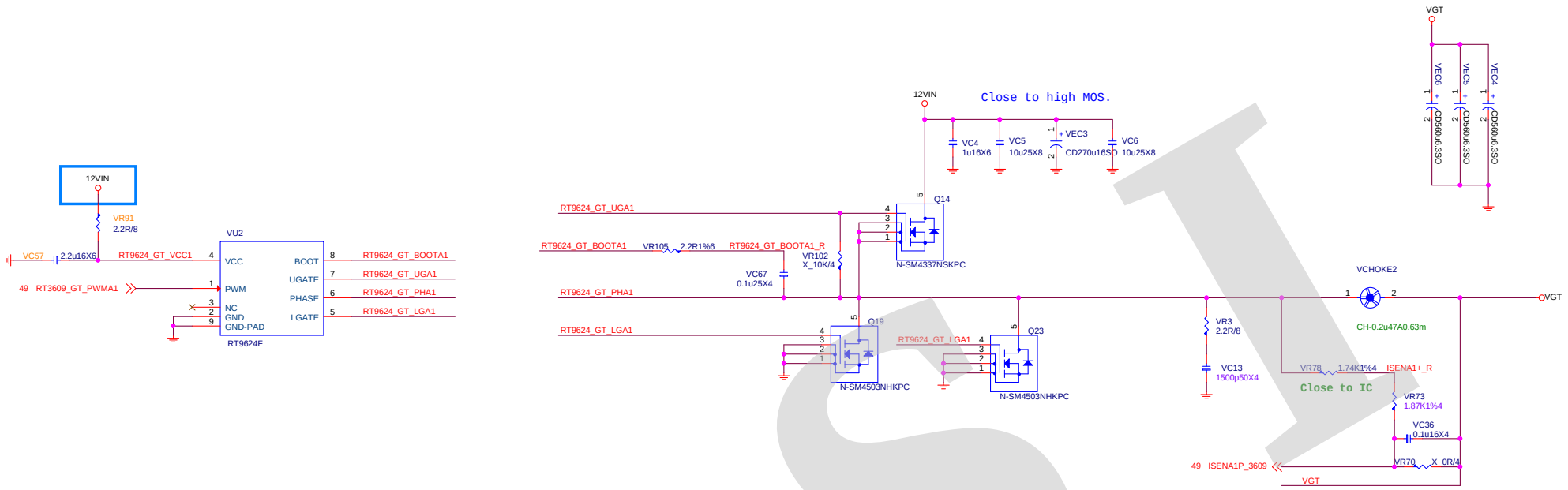

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7C81	
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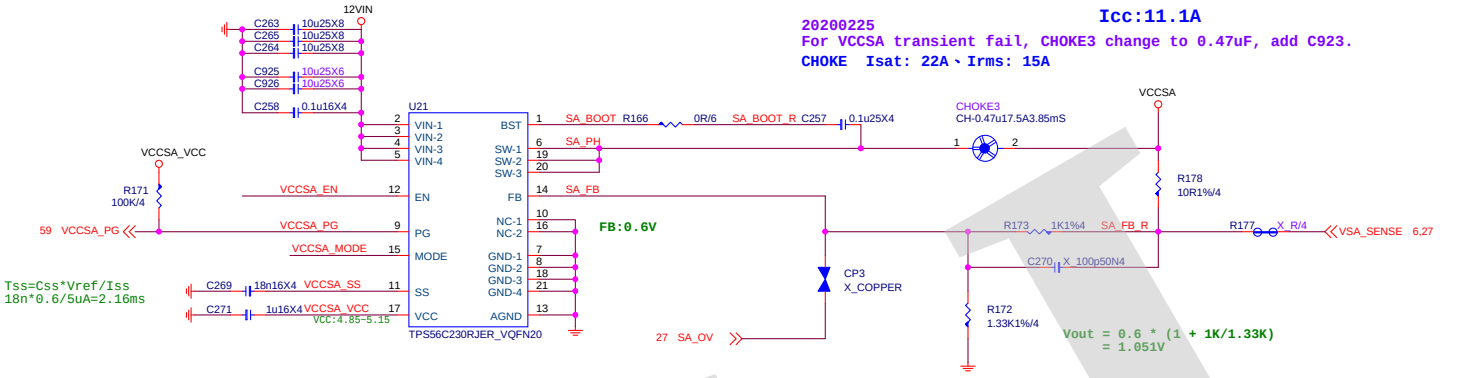
SA Power:1.05V,11.1A

Current limit: 13A~18A, TYP=15A

C925、C926 close U21, place under heatsink.

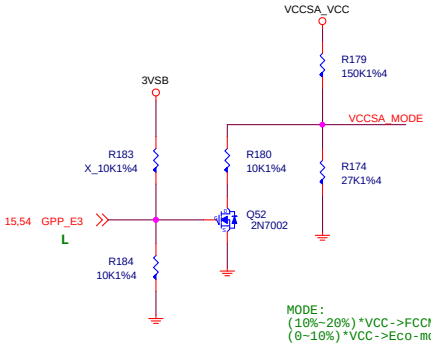
1.05V
Icc:11.1A

20200225
For VCCSA transient fail, CHOKE3 change to 0.47uF, add C923.
CHOKE Isat: 22A、Irms: 15A

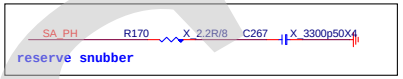


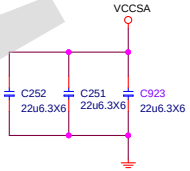
Tss=Css*Vref/Iss
18n*0.6/5uA=2.16ms

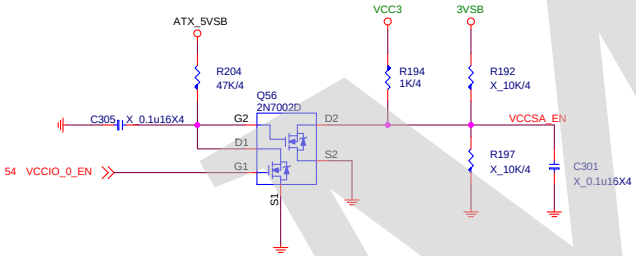
Vout = 0.6 * (1 + 1K/1.33K)
= 1.051V



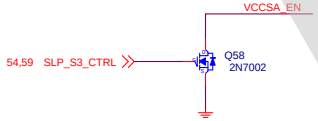
MODE:
(10%~20%)*VCC->FCCM (Freq:500K)
(0~10%)*VCC->Eco-mode (Freq:500K)







EN:VIH 1.2~1.4V
EN pin Maximum:5.5V



SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled max:1us

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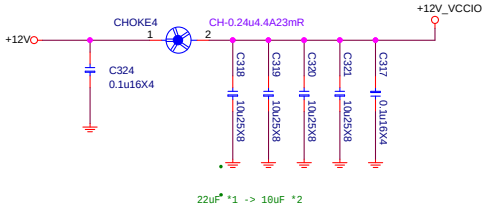
VCCIO_0 Power

1.05V Icc:6.4A

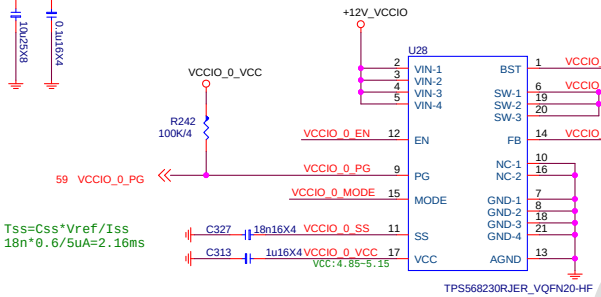
Current limit: 8.1A~12A, TYP=9.8A

```
Irms = Iout * SQRT[(Vout/Vin) * ((Vin-Vout)/Vin)]
     = 6.4 * SQRT[(0.95/12)*((12-0.95)/12)]
     = 1.73A
CHOKE  Isat: 5.05A、Irms: 4.5A
```



CHOKE Isat: 22A、Irms: 15A

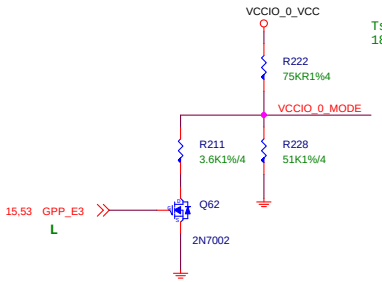
1.05V
Icc:6.4A




```
Vout = 0.6 * (1 + 1K/1.69K)
     = 0.955V
```

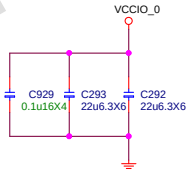
20200313:
R233 change to 1.69KR, VCCIO > 0.95V.

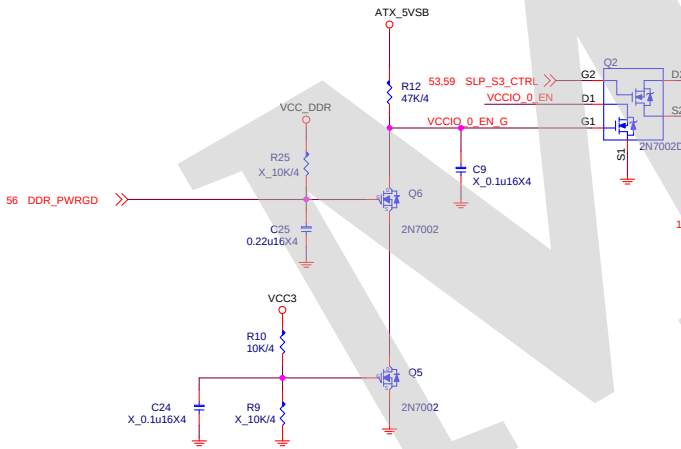
```
Tss=Css*Vref/Iss
18n*0.6/5uA=2.16ms
```

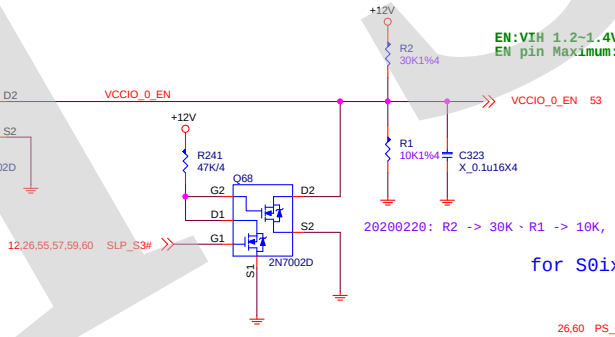



```
MODE:
RM_H:75K,RM_L:51K->FCCM (Freq:800K) 2V
RM_H:150K,RM_L:33K->OOA mode (Freq:800K) 0.9V
RM_H:330K,RM_L:15K->Eco-mode (Freq:800K) 0.22V
```

20200323
C929 for Vout return path.



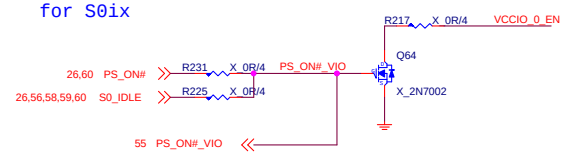


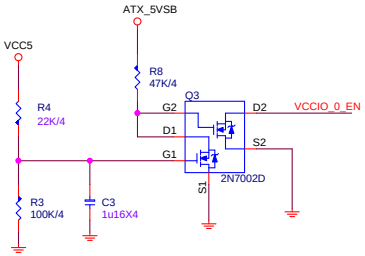


EN:VIH 1.2~1.4V
EN pin Maximum:3.6V

20200220: R2 -> 30K、R1 -> 10K, 400 update.

for S0ix





20200220: R4 change to 22KR, C3 change 1uF.(follow 7C82)

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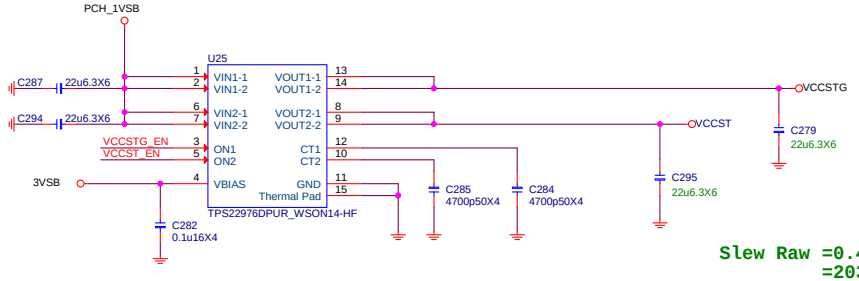
VCCST 1.0V; 0.45A

VCCSTG 1.0V; 0.2A

Power Loss1=(I*I)*Rds(on)
=(0.45*0.45))*0.027
=6.4*0.022
=5.5mW

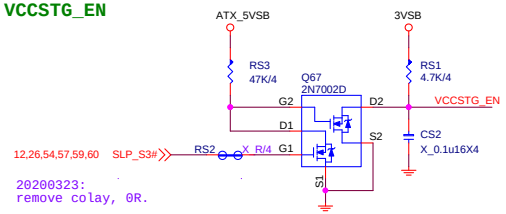
Power Loss2=(I*I)*Rds(on)
=(0.2*0.2)*0.027
=1mW



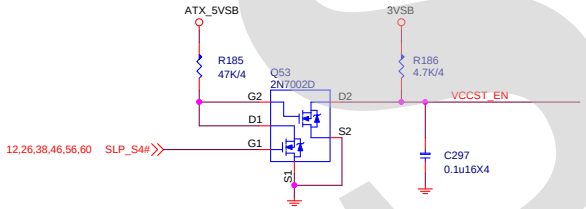
Slew Raw =0.42*4700p+56
=2030uS

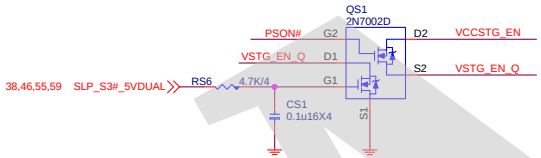
A CIN greater than CL is highly recommended.

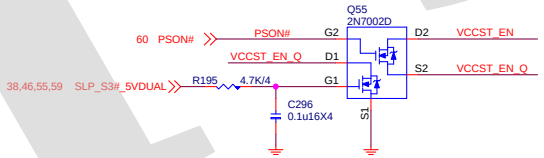
VCCSTG_EN

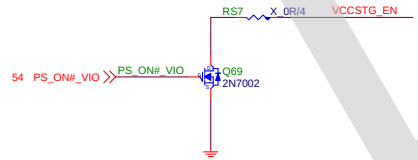


VCCST_EN









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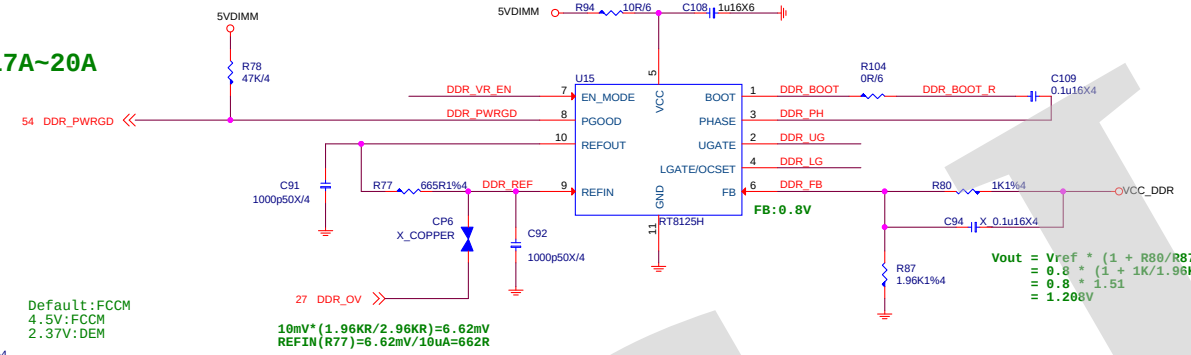
DDR4 Power:1.2V @ 13.67A

3.7A For CPU
9.1A For 4DIMM
0.7A For DDR VTT
0.17A For VCCPLL_OC

OCP = 16.2A~21.2A; Choke Isat=17A~20A

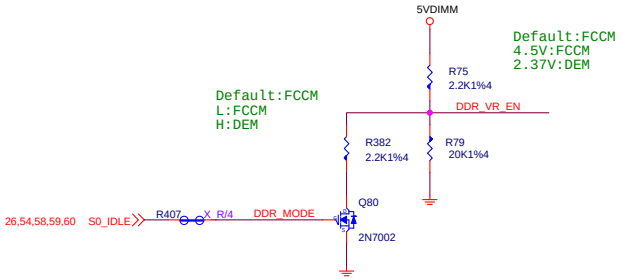
Iocp =Rocset* Iocset /Rdson(low)
=8.25K*10uA/3.9m
=21.2A
Iocp =Rocset* Iocset /Rdson(max)
=8.25K*10uA/5.1m
=16.2A

close IC

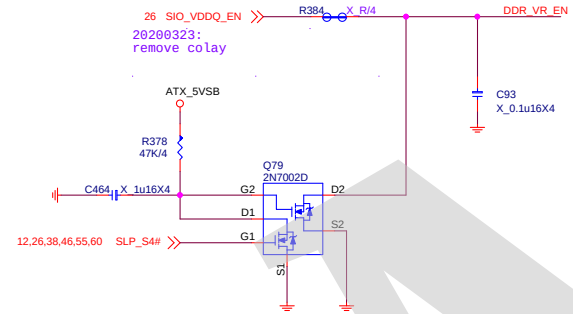


10mV*(1.96KR/2.96KR)=6.62mV
REFIN(R77)=6.62mV/10uA=662R

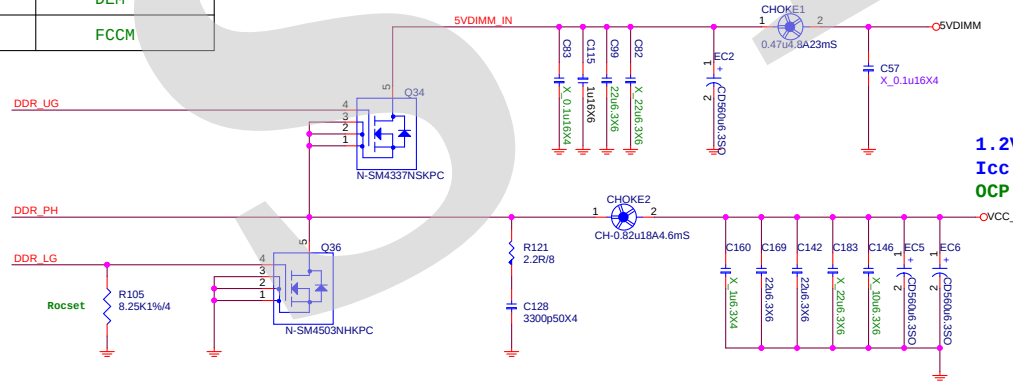
Vout = Vref * (1 + R80/R87)
= 0.8 * (1 + 1K/1.96K)
= 0.8 * 1.51
= 1.208V



EN_MODE Pin Voltage	IC Operate Mode
<0.4V	shut down
2.1~2.7V	DEM
4.3~5V	FCCM



Irms = Iout * SQRT[(Vout/Vin) * (1 - (Vout/Vin))]
= 13.67* SQRT[(1.2/5*(1-(1.2/5))]
= 5.84A
EC2 Irms: 1.8A/2.5A
CHOKE Isat: 6.7A、Irms: 4.8A



1.2V
Icc:13.67A
OCP: 16.2A~21.2A

Lout = [(Vin-Vout)/(Fsw*k*Iccmax)]*(Vout/Vin)
= [(5-1.2)/300K*0.3*13.67)]*(1.2/5)
= 0.74 uH
CHOKE Isat: 17A~20A、Irms: 16.5A

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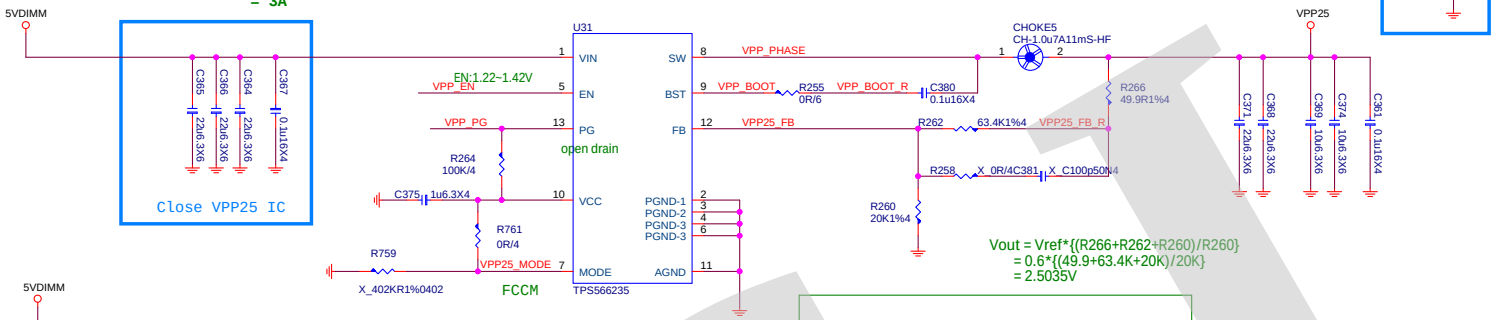
VPP2.5V Power:2.5V,6A(for dimm LED)

IC OCP:7.6A(6.6A~8.6A)

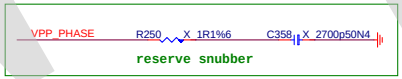
Isat(Lout)= 12A

```
Irms = Iout * SQRT((Vout/Vin) * (1 - (Vout/Vin)))
     = 6 * 0.5
     = 3A
```

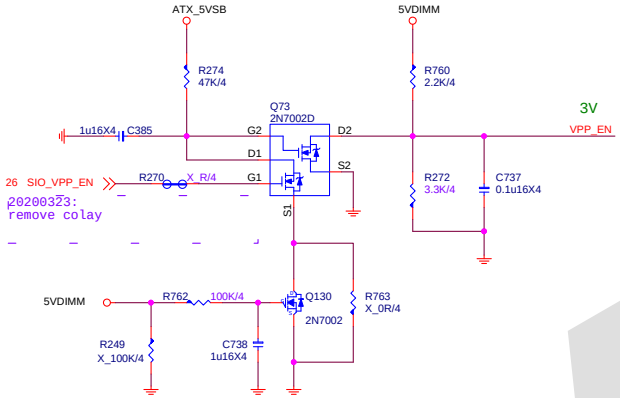


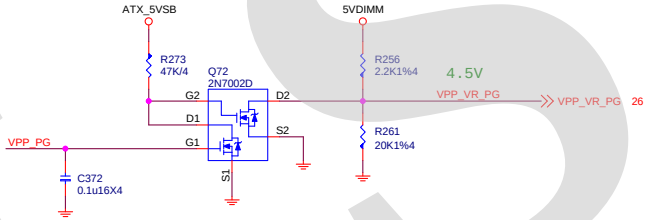

```
Vout = Vref*{(R266+R262+R260)/R260}
     = 0.6*{(49.9+63.4K+20K)/20K}
     = 2.5035V
```

```
source current 5uA at mode pin.
Rm to GND -> ECM
to VCC -> FCCM
```




```
Psnub = 1/2 x 2700p x 5^2 x 600K
      = 0.021W..... < 0.1W
```



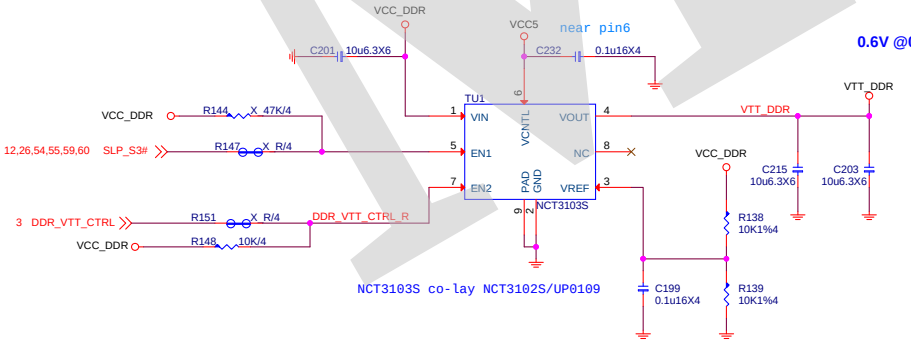


DDR VTT Power

IC OCP: 2.1A~4A

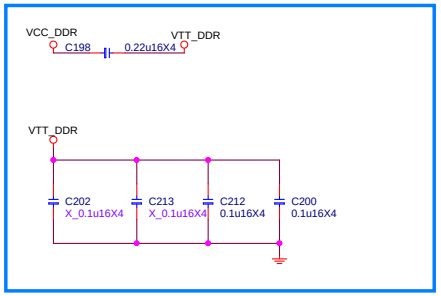
```
To CPU Copper trace width > 250mils , Fill
island behind DIMM > 400mils .
```

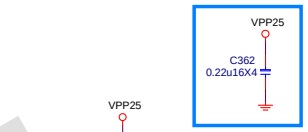
0.6V @0.7A



NCT3103S co-lay NCT3102S/UP0109

Close DIMM.





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PCH_1P05_VSB Power:1.0V,11.8A

OCP = 16.2A~21.2A

Iocp =Rocset* Iocset /Rdson(low)
=8.25K*10uA/3.9m
=21.2A
Iocp =Rocset* Iocset /Rdson(max)
=8.25K*10uA/5.1m
=16.2A

Irms = Iout * SQRT[(Vout/Vin) * (1 - (Vout/Vin))]
= 11.8* SQRT[(1/5*(1-(1/5))]
= 4.72A

CAP Irms: 1.8A/2.5A CHOKE Isat: 6.7A、Irms: 4.8A

1V
Icc:11.8A
OCP:18A

EN_MODE Pin Voltage	IC Operate Mode
<0.4V	shut down
2.1~2.7V	DEM
4.3~5V	FCCM

Vout = Vref * (1 + R610/R613)
= 0.8 * (1 + 1K/3.92K)
= 1.0V

Lout = [(Vin-Vout)/(Fsw*k*Iccmax)]*(Vout/Vin)
= [(5-1)/300K*0.3*11.8)]*(1/5)
= 0.75uH

CHOKE Isat: 17A~20A、Irms: 16.5A

20200225: use 3VSB.
20200323 remove 1P8_VSB

Default:FCCM
L:FCCM
H:DEM

1P8_VSB Power:1.8V, 0.082A

OCP = 3.8A

20191127
Change to LPC, unstuff.
1P8_VSB 改為3VSB

20200323
Remove 1P8_VSB

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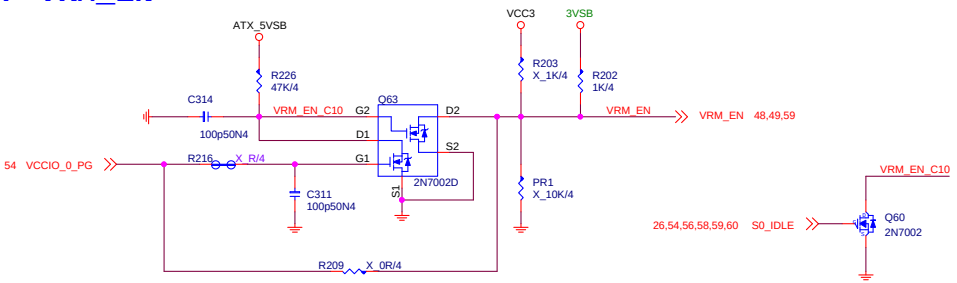
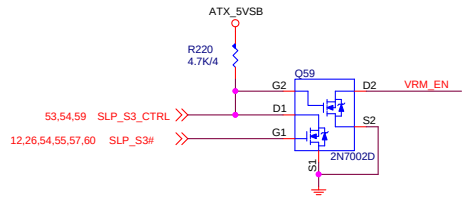
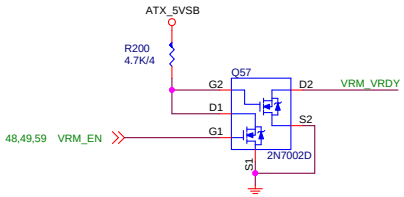
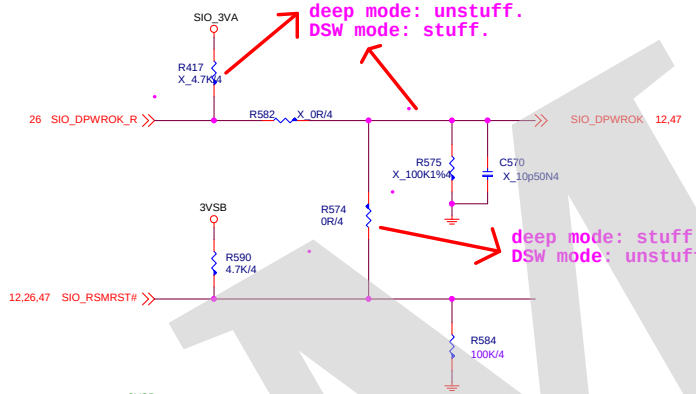
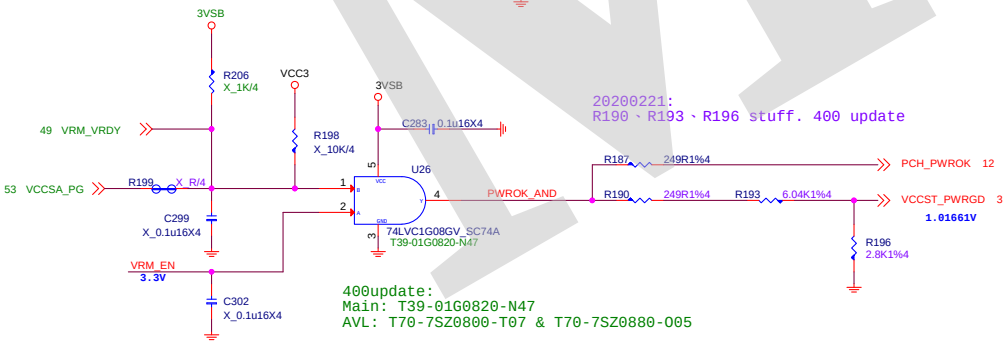
for VRM_EN









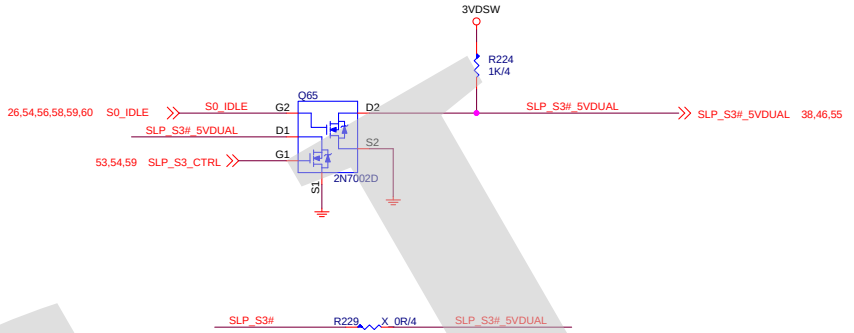


20200221:
R190、R193、R196 stuff. 400 update

400update:
Main: T39-01G0820-N47
AVL: T70-7SZ0800-T07 & T70-7SZ0880-O05

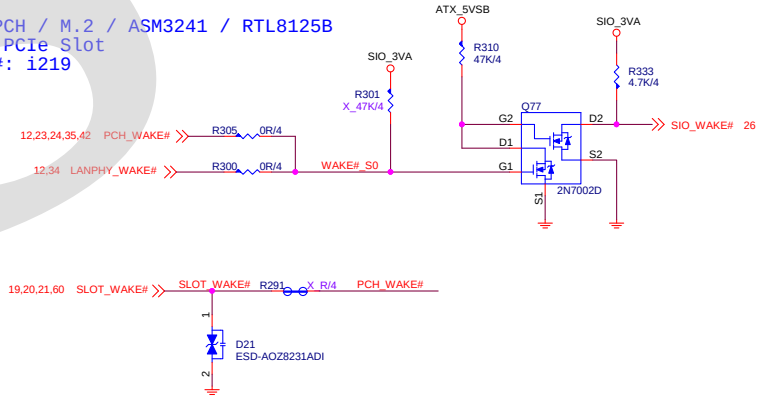
for 5VDIMM and 5VDUAL

for S0ix

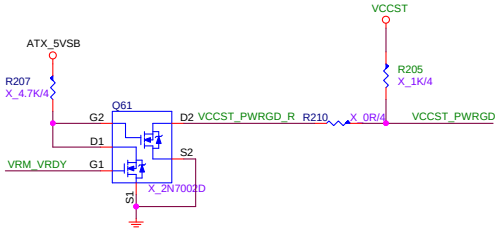


for wake

PCH_WAKE#: PCH / M.2 / ASM3241 / RTL8125B
SLOT_WAKE#: PCIe Slot
LANPHY_WAKE#: i219



20200221:
Q61、R207、R210、R205 unstuff. 400 update



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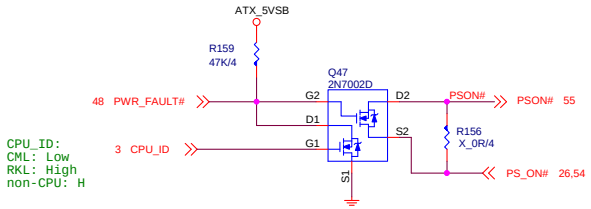
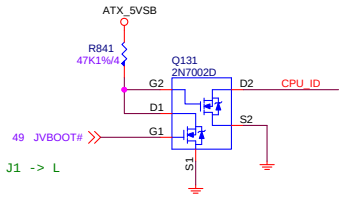
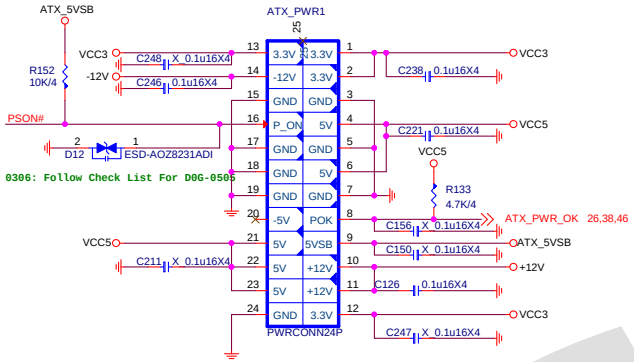
ATX POWER CONNECTOR



20200220 edit JVBOOT# circuit.

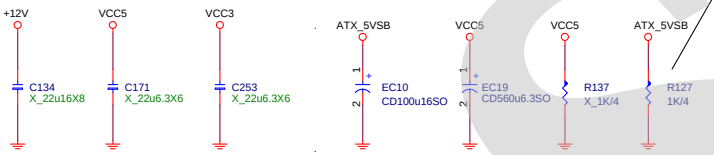


JPWR1

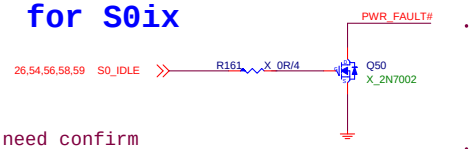


上1K是解決航嘉200W(huntkey)power supply的問題,加1K是為了不讓ATX_5VSB空載而產生震盪

close ATX_PWR1

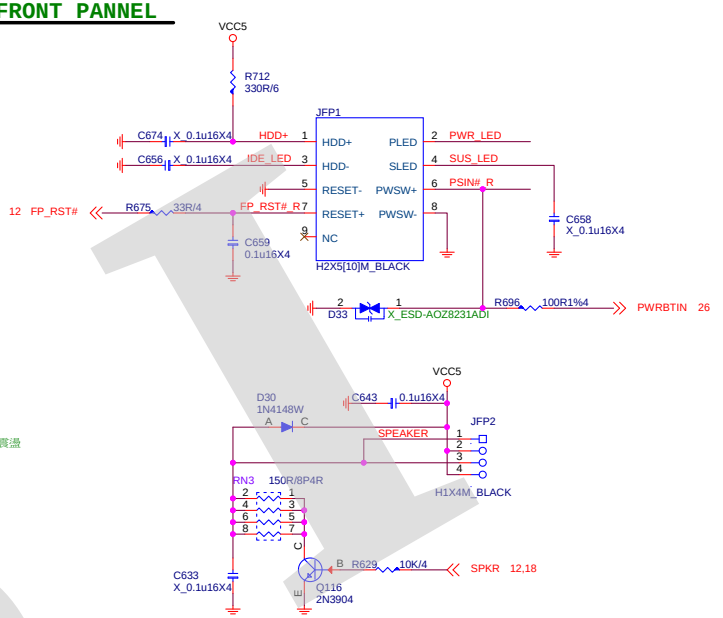


for S0ix

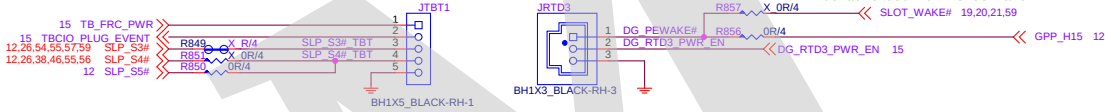


need confirm

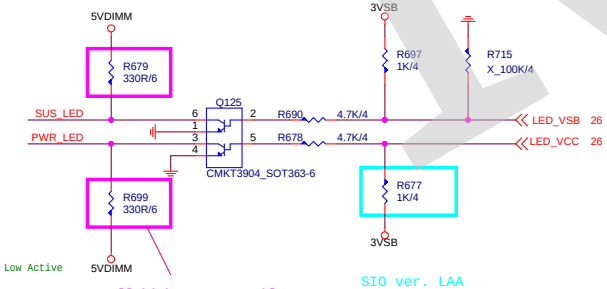
FRONT PANNEL

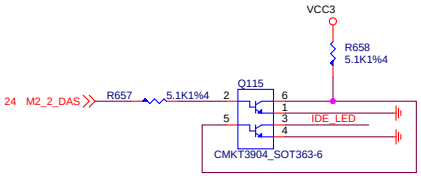


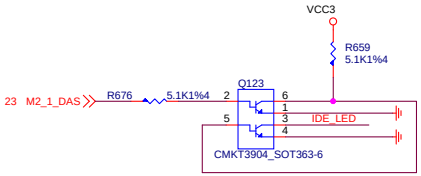
Thunderbolt card support

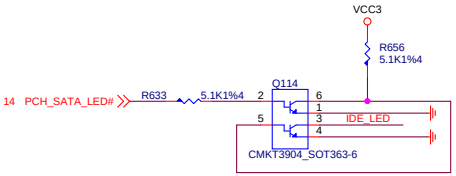


Front Panel LED









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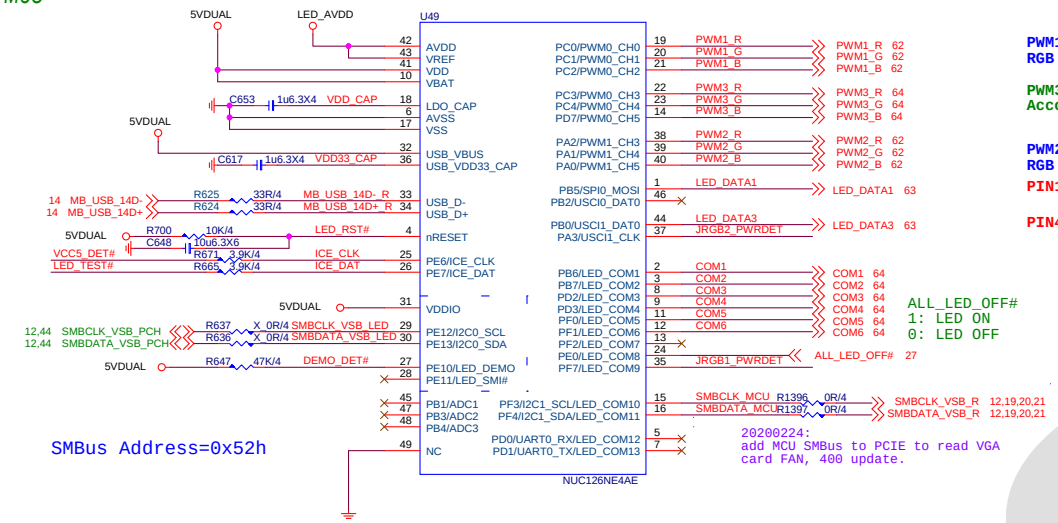
LED
MCU



SMBus Address=0x52h

ALL_LED_OFF#
1: LED ON
0: LED OFF

20200224:
add MCU SMBus to PCIE to read VGA card FAN, 400 update.

PWM1 for JRGB1
RGB LED STRIPLINE USED

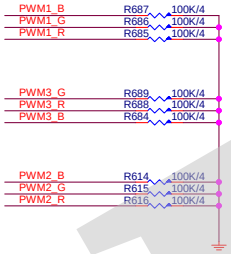
PWM3 for Others
According to demand configuration

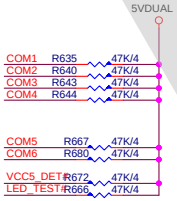
PWM2 for JRGB2
RGB LED STRIPLINE USED
PIN1 for JRAINBOW1

PIN44 for JRAINBOW2

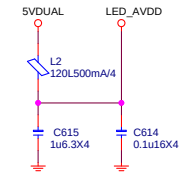
COM1~8 for PWM3
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized onboard LED control.

COM9~12 for PWM2
According to demand configuration.
If SPEC. don't have JRGB2,
Can configuration COM9~12,
To achieve 4 group Non-synchronized onboard LED control.
PS. COM1 is the first action block, next is COM2, and so on.
Pin15,16 can configure to master smbus if spec requirement.

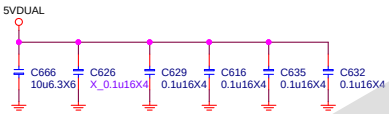




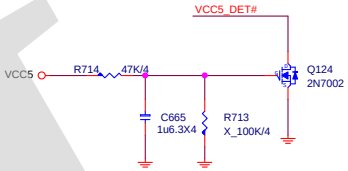
Control	Net Name	PWM USE
PCH	LED_DATA1	No Use
AUDIO Cover	LED_GPIO_01	No Use
MOS/IO cover	LED_GPIO_02	No Use
JRAINBOW1	LED_GPIO_03	No Use
JCORSAIR1	LED_DATA2	No Use
JRGB1/JRGB2	PWM1/ PWM2	PWM1/ PWM2
Board Side LED	COM 1~8	PWM3
Board Side LED	COM 9~16	PWM2

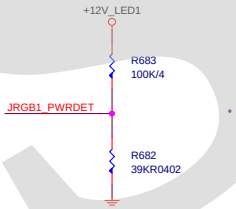


C615 & C614 near AVDD Pin.



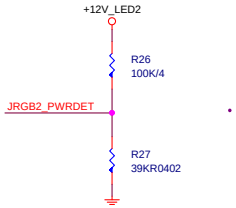
C666 & C626 near VDD_Pin.
C629 & C616 near VREF & VBAT Pin.
C635 & C632 near VDDIO & USB VBUS Pin.



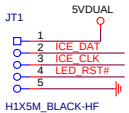


IF no JPWRLED1 & JPIPE_LED spec

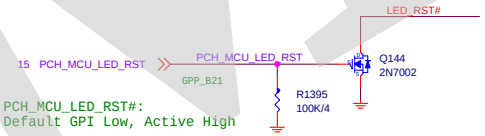
MCU can powered by 5VDUAL directly.
LED_VCC5 replace with 5VDUAL.



JT1 for FW update



20200224: add for HW Reset MCU



PCH_MCU_LED_RST#:
Default GPI Low, Active High

JF1 for Factory test

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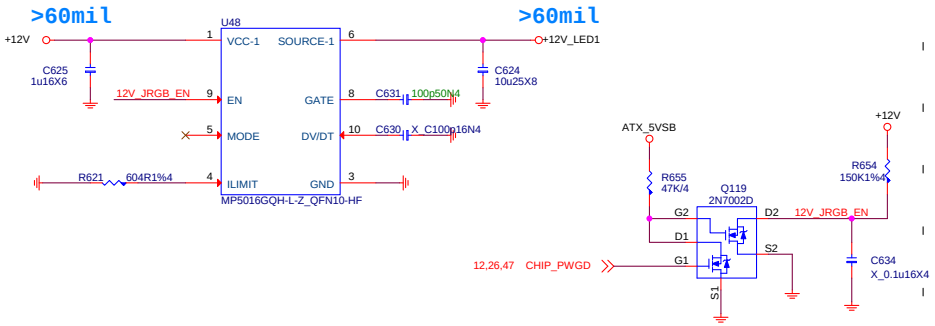
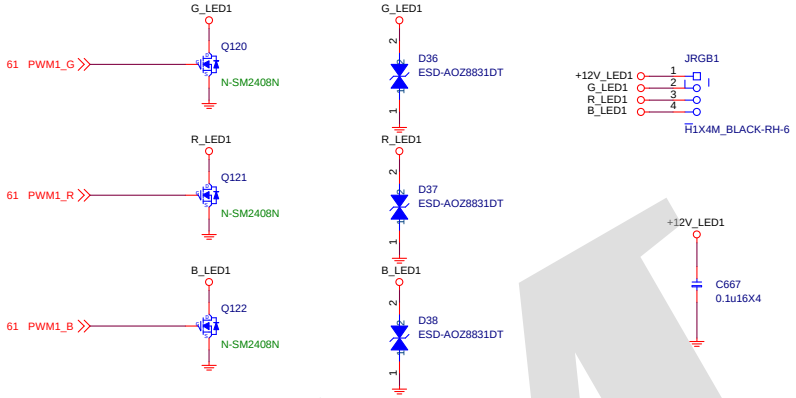
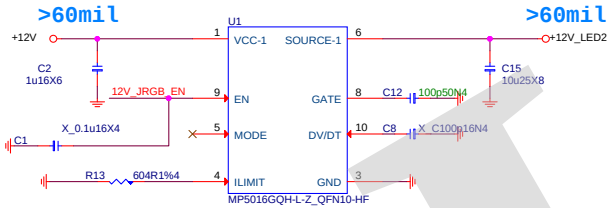
JRGB1

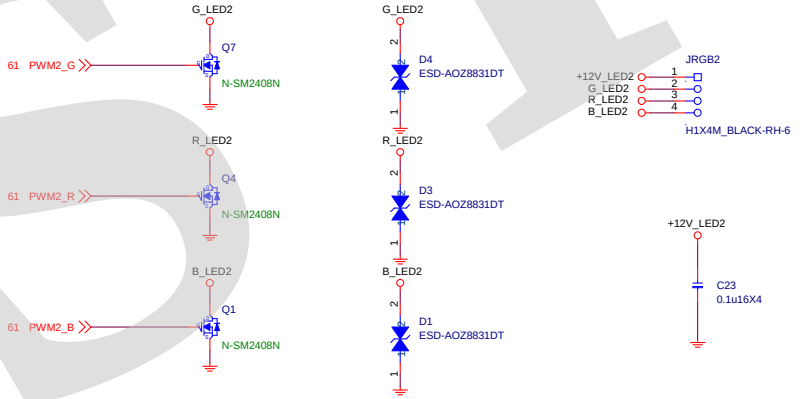




SM2408N為400系列新料，新製程較便宜，驗證OK將取代SM2306

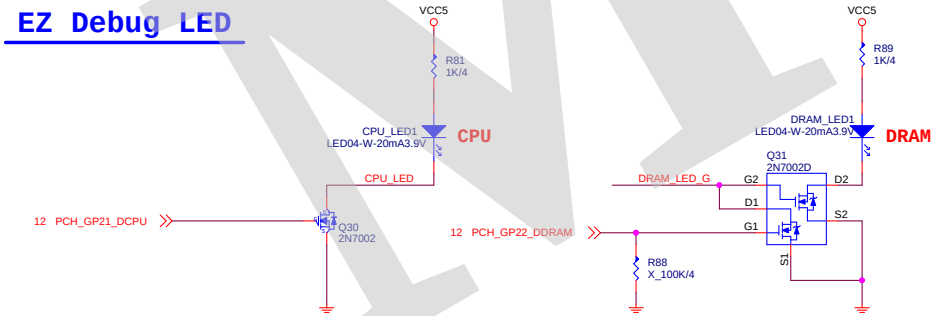
JRGB2

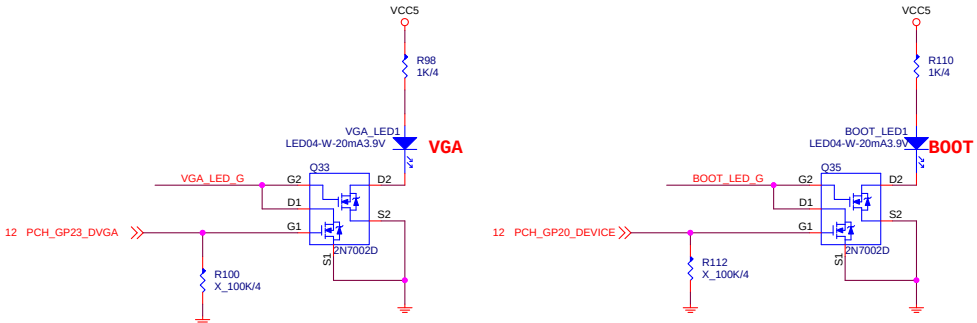




SM2408N為400系列新料，新製程較便宜，驗證OK將取代SM2306

EZ Debug LED





MSI	MICRO-STAR INT'L CO.,LTD	
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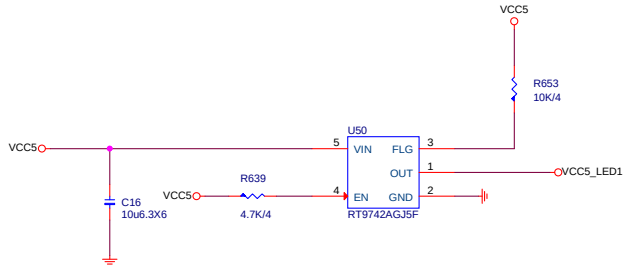
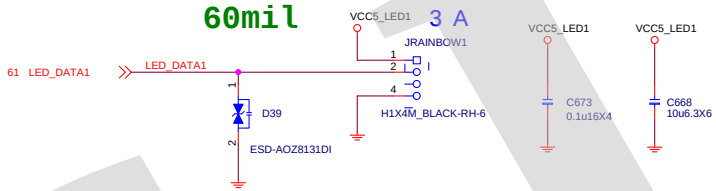
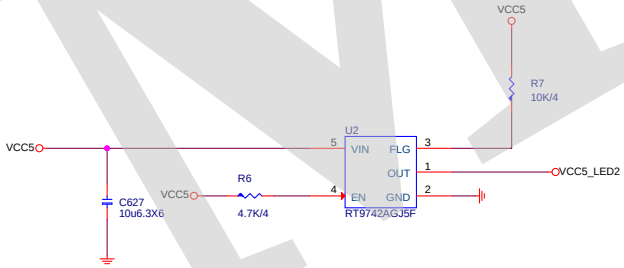
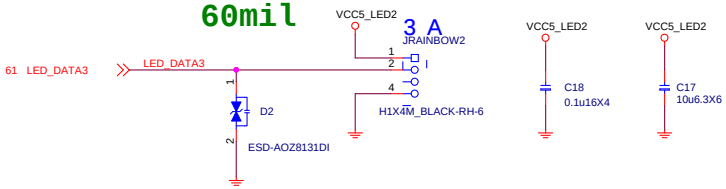


JRAINBOW1 LED





JRAINBOW2 LED



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Size: Custom	Document Description: JRAINBOW1_2 LED
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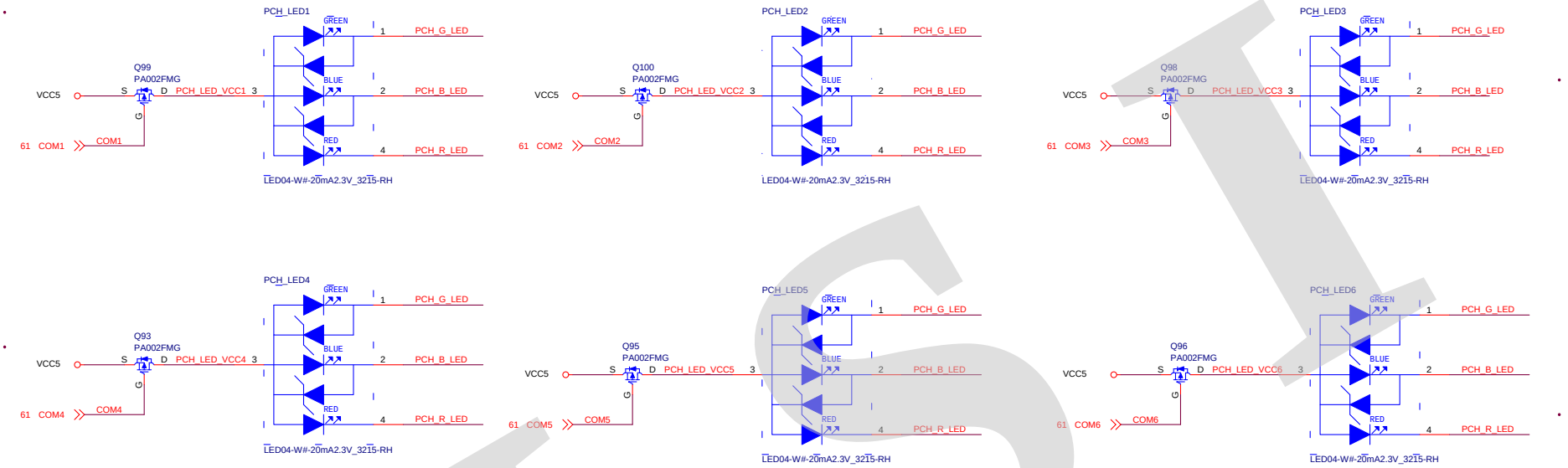
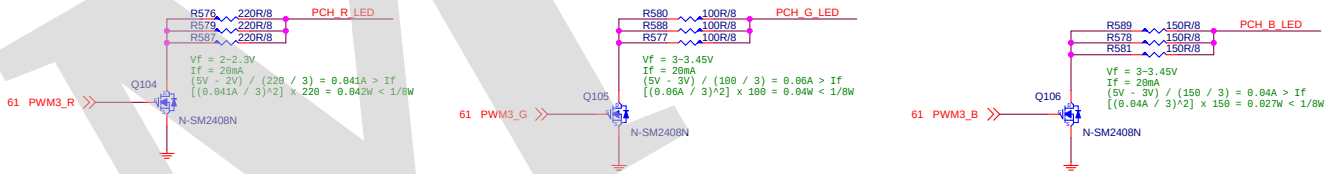
PCH_LED





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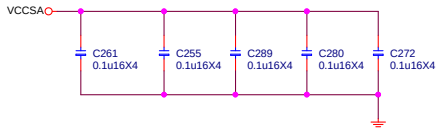
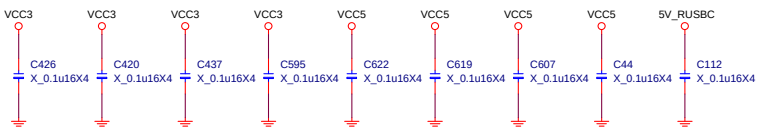
Return path cap

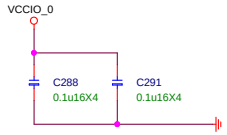
for VCCSA return path

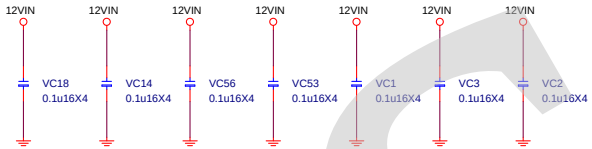


For EMC Request

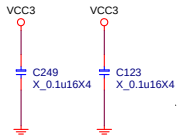


for DMI signals

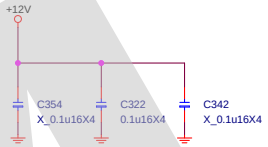




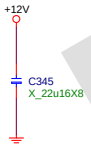
EMI



for +12V noise



reserve for GTX1650 VGA card



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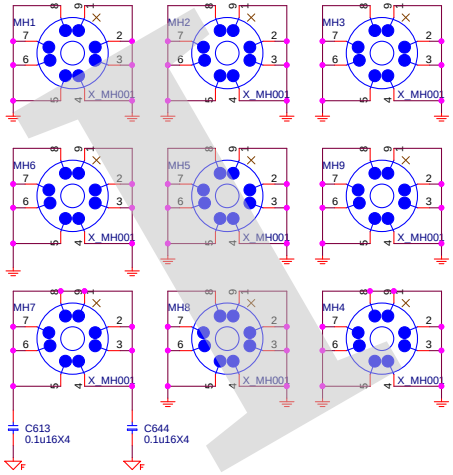
Mounting Holes



CPU_H1

CPU
鐵座

CPU_H1

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BAT1_X1

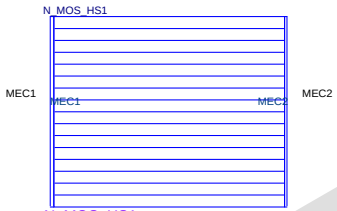
BAT-BCR2032P

PCB1

7C81-10

PD0-07C8110-E48

Heat Sink



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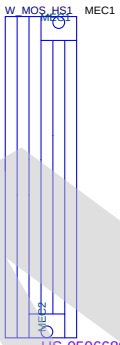

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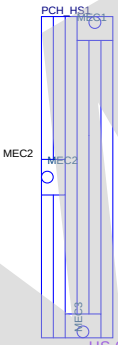

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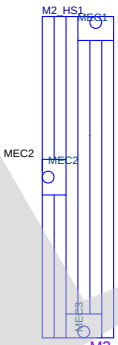

M2_HEATSINK

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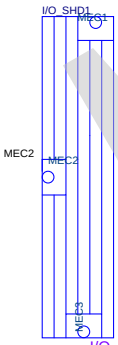

I/O_SHIELDING

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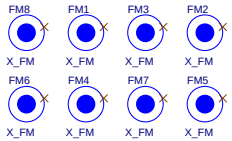
Simulation

Optical Fiducial Marks-120



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Custom	Manual Parts	10

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