LCFC Confidential

DG710 MB Schematics Document

Intel Skylake-U22/Kabylake-U22 with DDR4 + AMD R16M-M1-30 GPU

2016-02-25

REV:0.1

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Cover Page		
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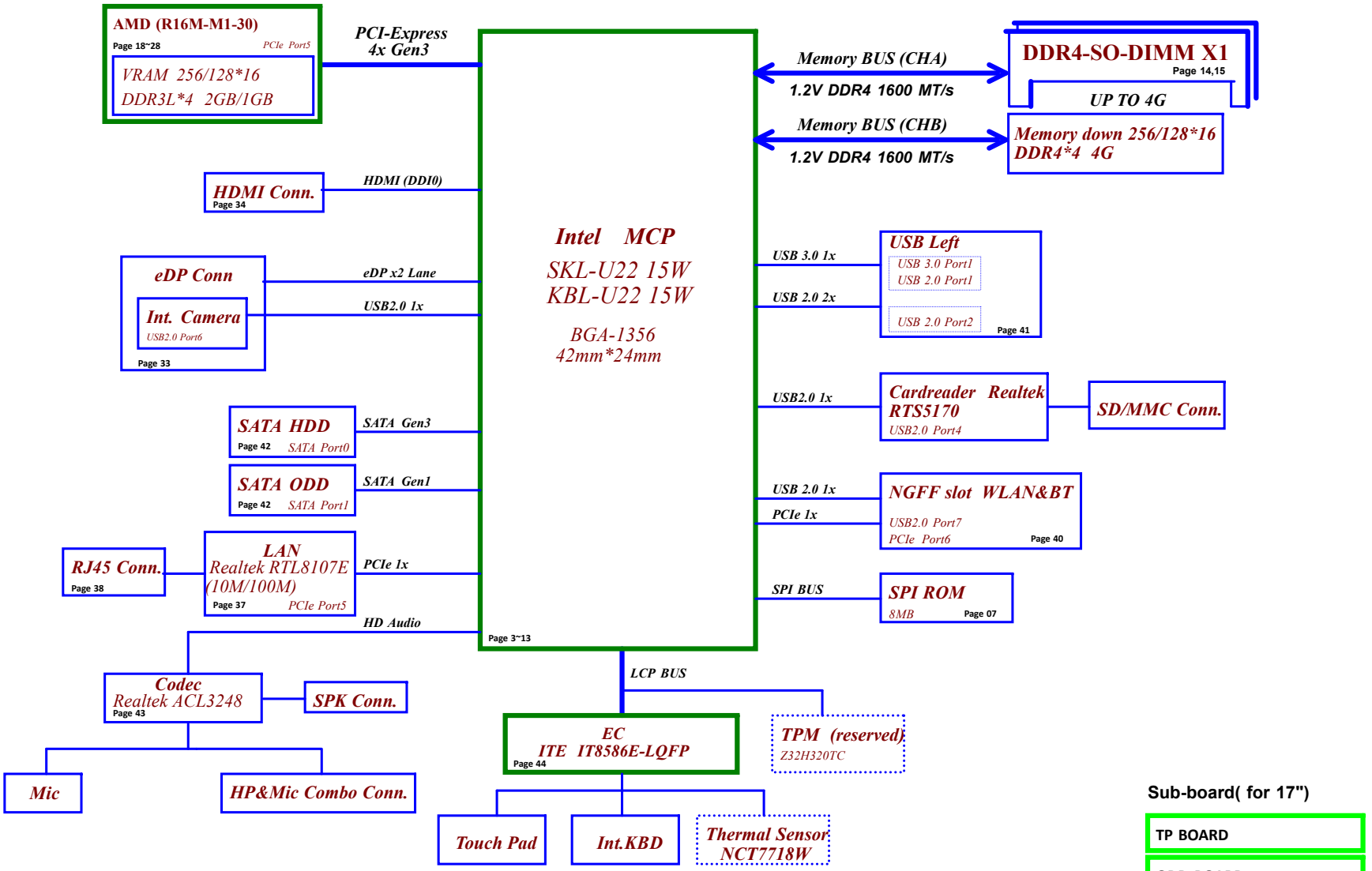

Sub-board(for 17")

TP BOARD

ODD BOARD

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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT		Function
USB3.0	1	USB3.0 Conn Left
	2	USB3.0 Conn Right(optional)
	3	3D Camera(optional)
	4	NC
	5	NC
	6	NC
USB2.0	1	USB3.0 Conn Left
	2	USB2.0 Conn1 Right
	3	USB2.0 Conn2 Right
	4	Camera
	5	Cardreader
	6	Touch Panel
	7	Bluetooth
	8	NC
	9	NC
	10	NC
PCIE	1	NC
	2	NC
	3	NC
	4	NC
	5	LAN
	6	WLAN
	7	used as SATA
	8	used as SATA
	9~12 X4 PCIE	DGPU
SATA	0	HDD
	1A	ODD
	1B	used as PCIE
	2	used as PCIE

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
14or15@	For 14" or 15" part
14or17@	For 14" or 17" part
Cannonlake@	For Cannonlake part
CD@	For C cost down
DUALMIC@	For Dual MIC part
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC nu-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ES@	For ES CPU
EXO@	For EXO GPU
ME@	For ME part
NTS@	For nu-touch part
PX@	For PX part
RANKA@	For VRAM rank A part
RANKB@	For VRAM rank B part
Realtek_SD@	For Realtek SD part
SINGLEMIC@	For single MIC part
SINGLERANK@	For single VRAN rank part
DUALRANK@	For dual VRAN rank part
TS@	For touch screen part
TPM@	For TPM part
UMA@	For UMA part

SMBUS Control Table

	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

EC SMBus1 address

Device	Address
Smart Battery	need to update
Charger	0001 0010 b

EC SMBus2 address

Device	Address
Thermal Sensor(NCT7718W)	1001_100xb
PCH	need to update
DGPU	need to update

EC SMBus3 address

Device	Address
PMIC	need to update

PCH SM Bus address

Device	Address
DDR4 SODIMM	need to update
Wlan	Reserved

Title: Notes List

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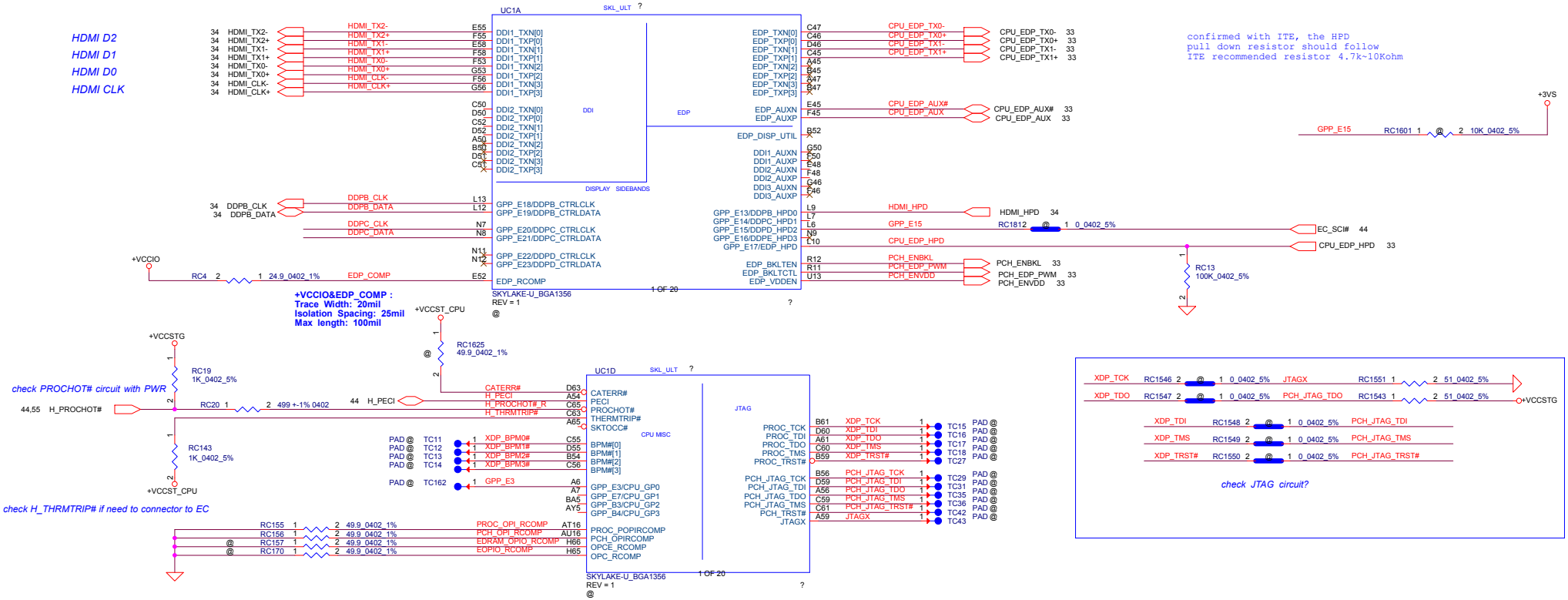

DDP*_CTRLDATA strapping sampled on the rising edge of PWROK

Port	Strap	Enable	Disable
Port 1	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC
Port 2	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2Kohm	NC

Title	MCP (DDI,EDP)	
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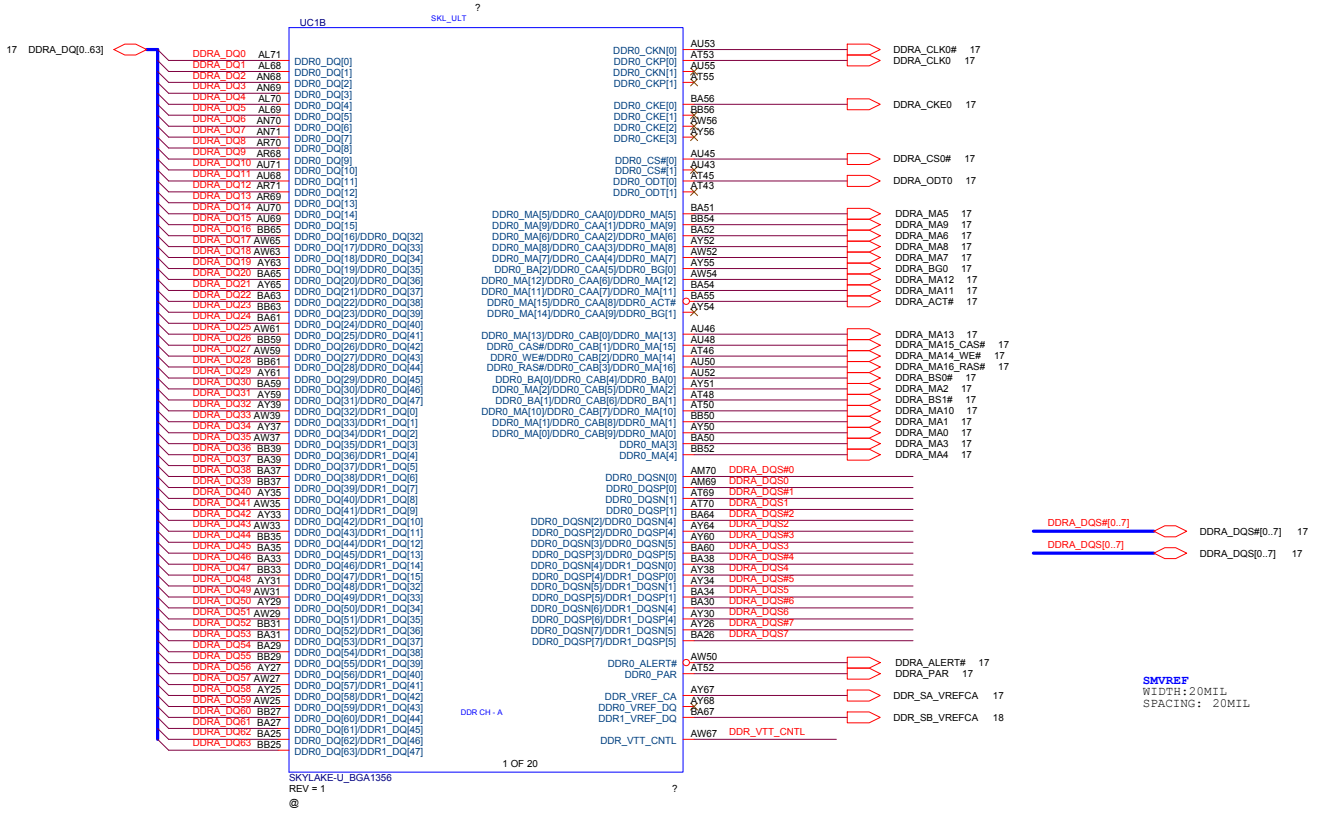

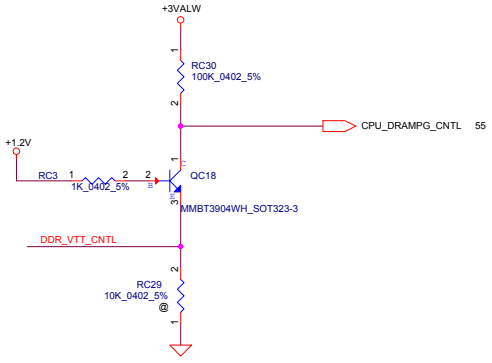

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (DDR4)**

Size: Custom	Document Number: DG710	Rev: 0.1
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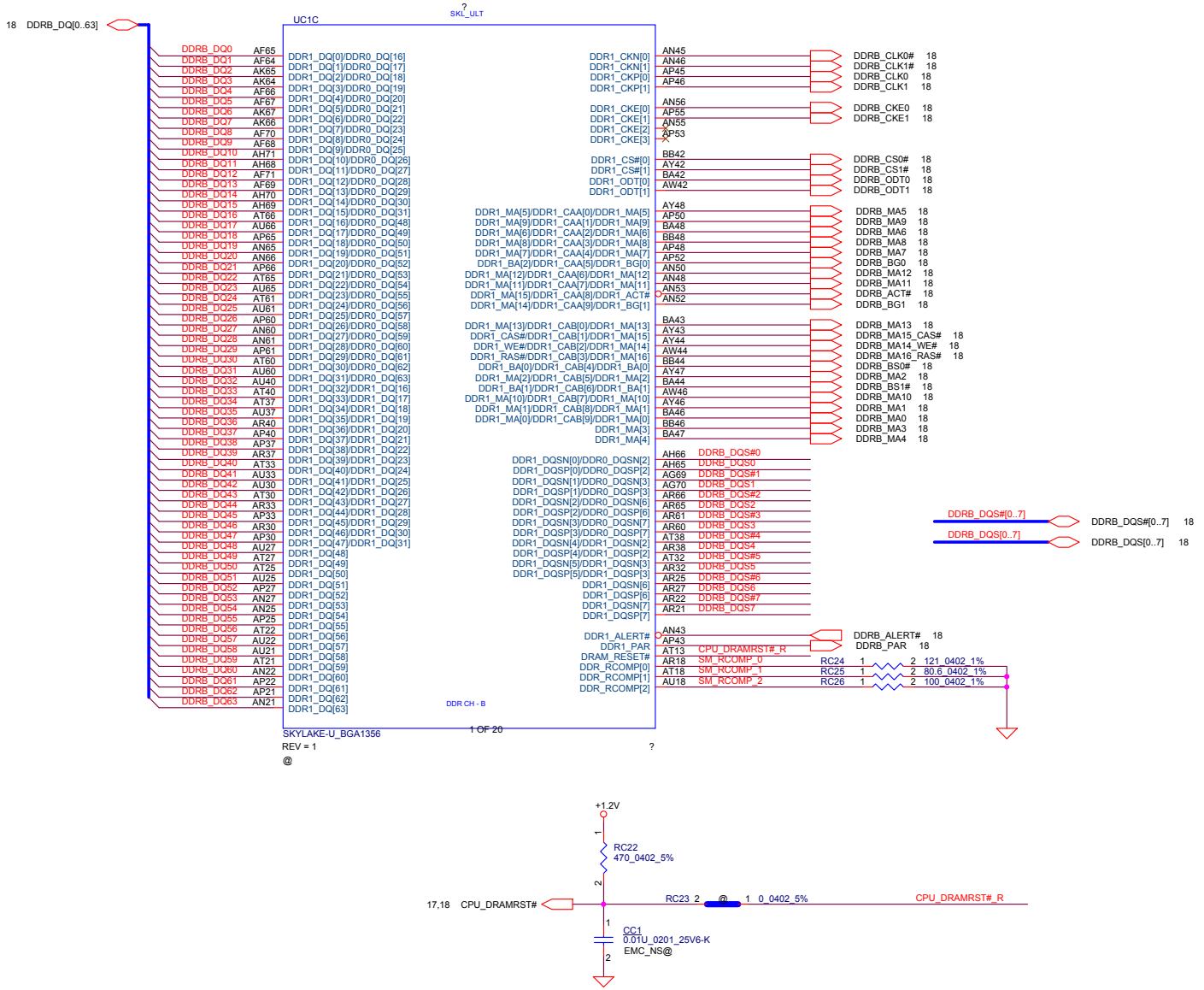

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (DDR4)

Size	Document Number	Rev
Custom	DG710	0.1

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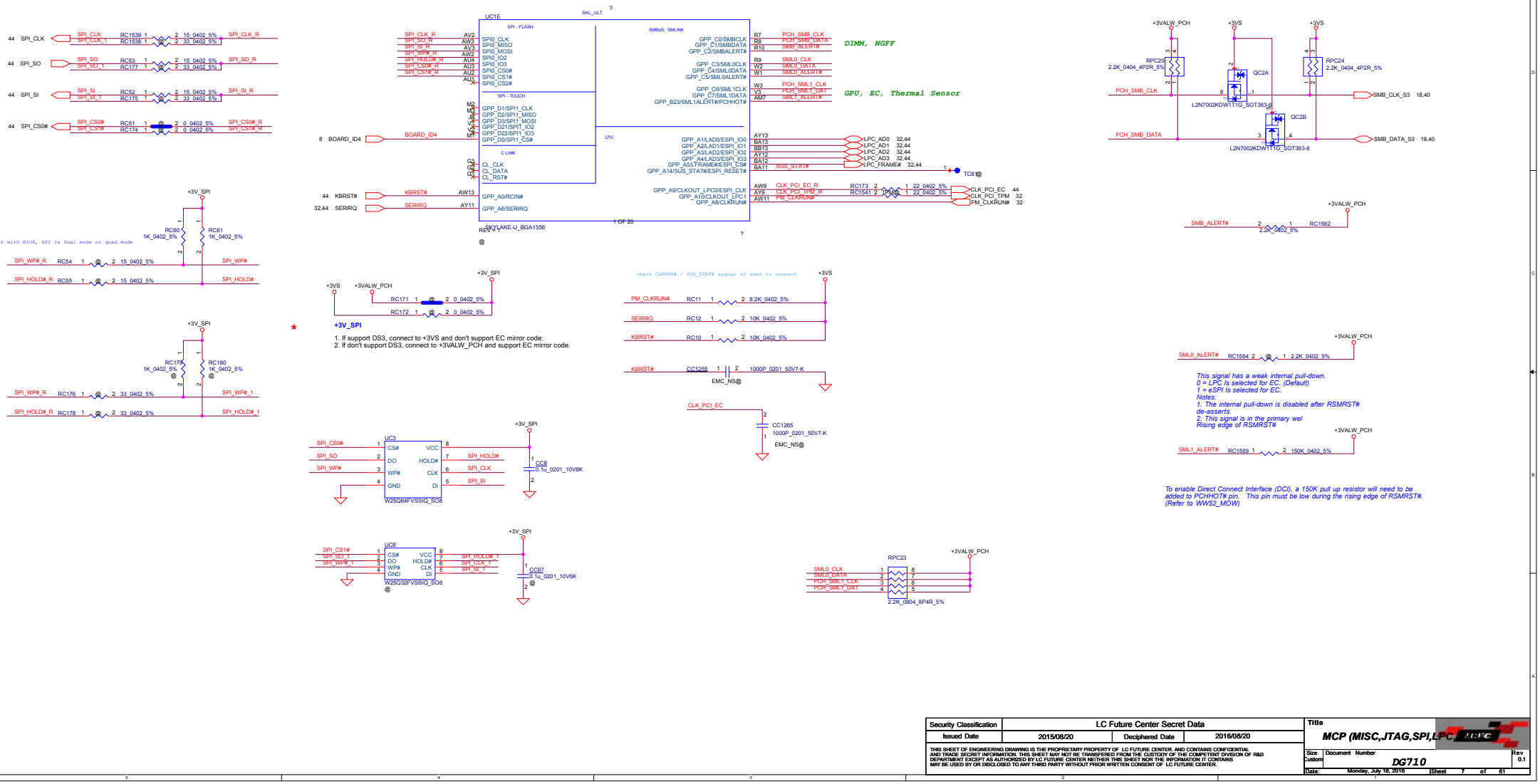

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

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Title	MCP (MISC,JTAG,SPI,LPC,...)		
Size: Custom	Document Number: DG710		Rev: 0.1
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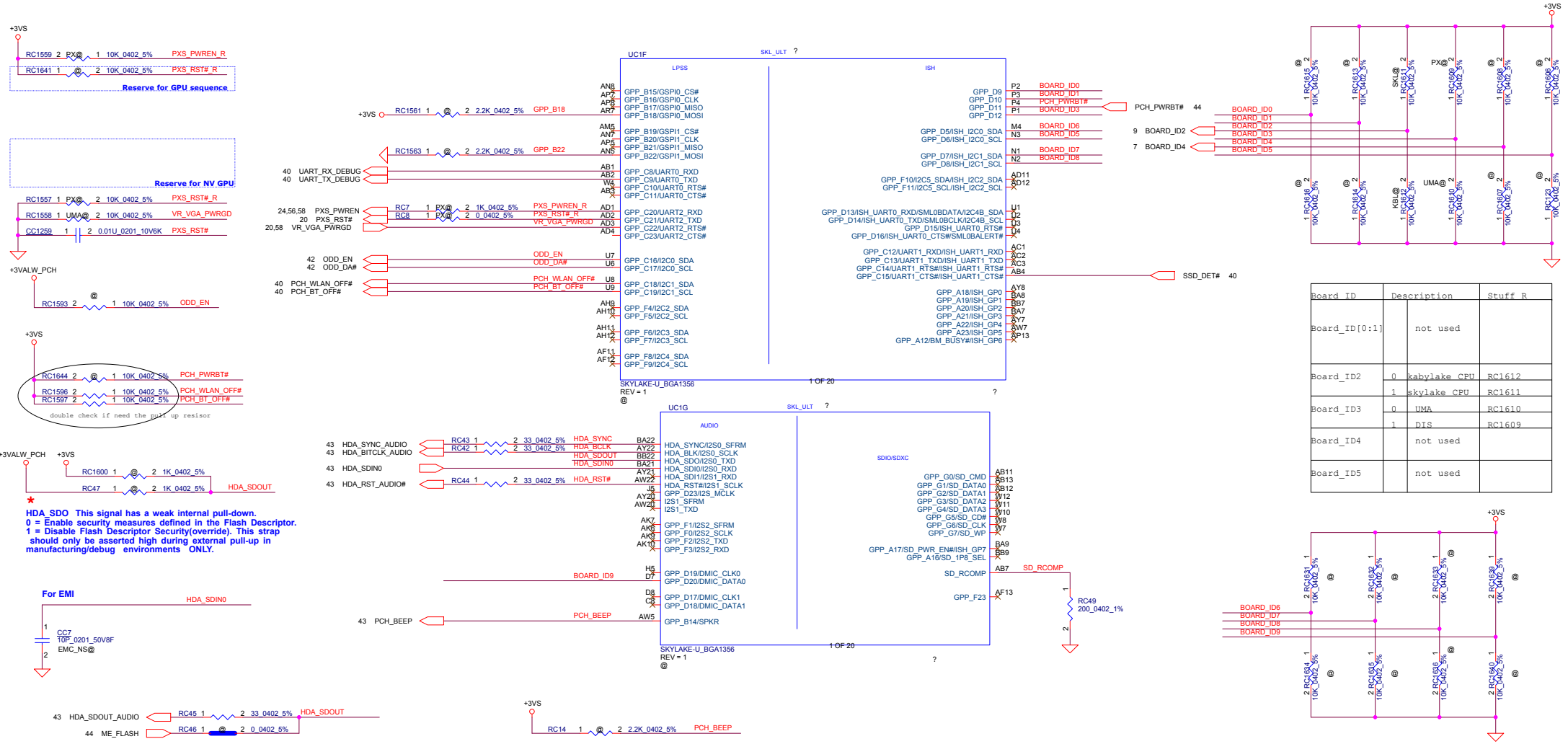

Board_ID		Description	Stuff R
Board_ID[0:1]		not used	
Board_ID2	0	kabylake CPU	RC1612
	1	skylake CPU	RC1611
Board_ID3	0	UMA	RC1610
	1	DIS	RC1609
Board_ID4		not used	
Board_ID5		not used	

Board_ID		Description	Stuff R
Board_ID [6,7,9]	000	Samsung 8Gb **2133 MT/s**	RC1634 RC1635 RC1640
	010	Hynix 8Gb **2133 MT/s**	RC1634 RC1632 RC1640
	100	Micron 8Gb **2133 MT/s**	RC1631 RC1635 RC1640
	110	Reserved	RC1631 RC1632 RC1640
	001	Samsung 8Gb **2400 MT/s**	RC1634 RC1635 RC1639
	011	Hynix 8Gb **2400 MT/s**	RC1634 RC1632 RC1639
	101	Micron 8Gb **2400 MT/s**	RC1631 RC1635 RC1639
	111	Reserved	RC1631 RC1632 RC1639
Board_ID8		not used	

Pin Name	Strap Description	Configuration	Default Value	When Sampled
SPKR / GPP_B14	Top Swap Override	Internal PD 0 = Disable " Top Swap" mode. (Default) ★ 1 = Enable " Top Swap" mode.	0	Rising edge of PCH_PWROK
GSPI0_MOSI /GPP_B18	No Reboot	Internal PD 0 = Disable " No Reboot" mode. (Default) ★ 1 = Enable " No Reboot" mode	0	Rising edge of PCH_PWROK
GSPI1_MOSI /GPP_B22	Boot BIOS Strap Bit BBS	Internal PD 0 = SPI (Default) 1 = LPC ★	0	Rising edge of PCH_PWROK

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Issued Date	2015/08/20	Deciphered Date	2016/08/20	

Title	MCP (LPSS,ISH,AUDIO,SDI		
Size Custom	Document Number DG710		Rev 0.1
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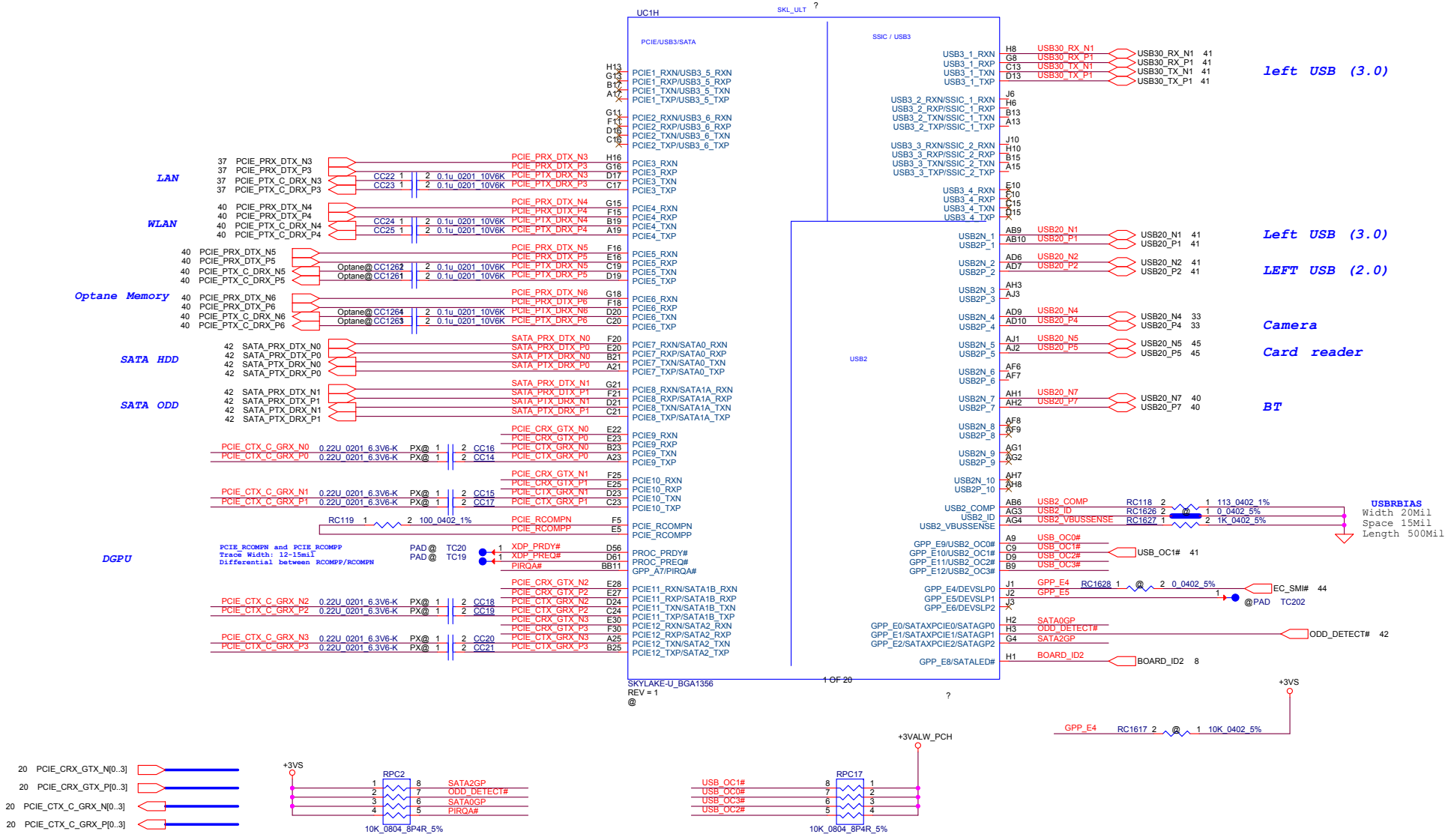

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (PCIE,SATA,USB3,US

Size	Document Number	Rev
Custom	DG710	0.1

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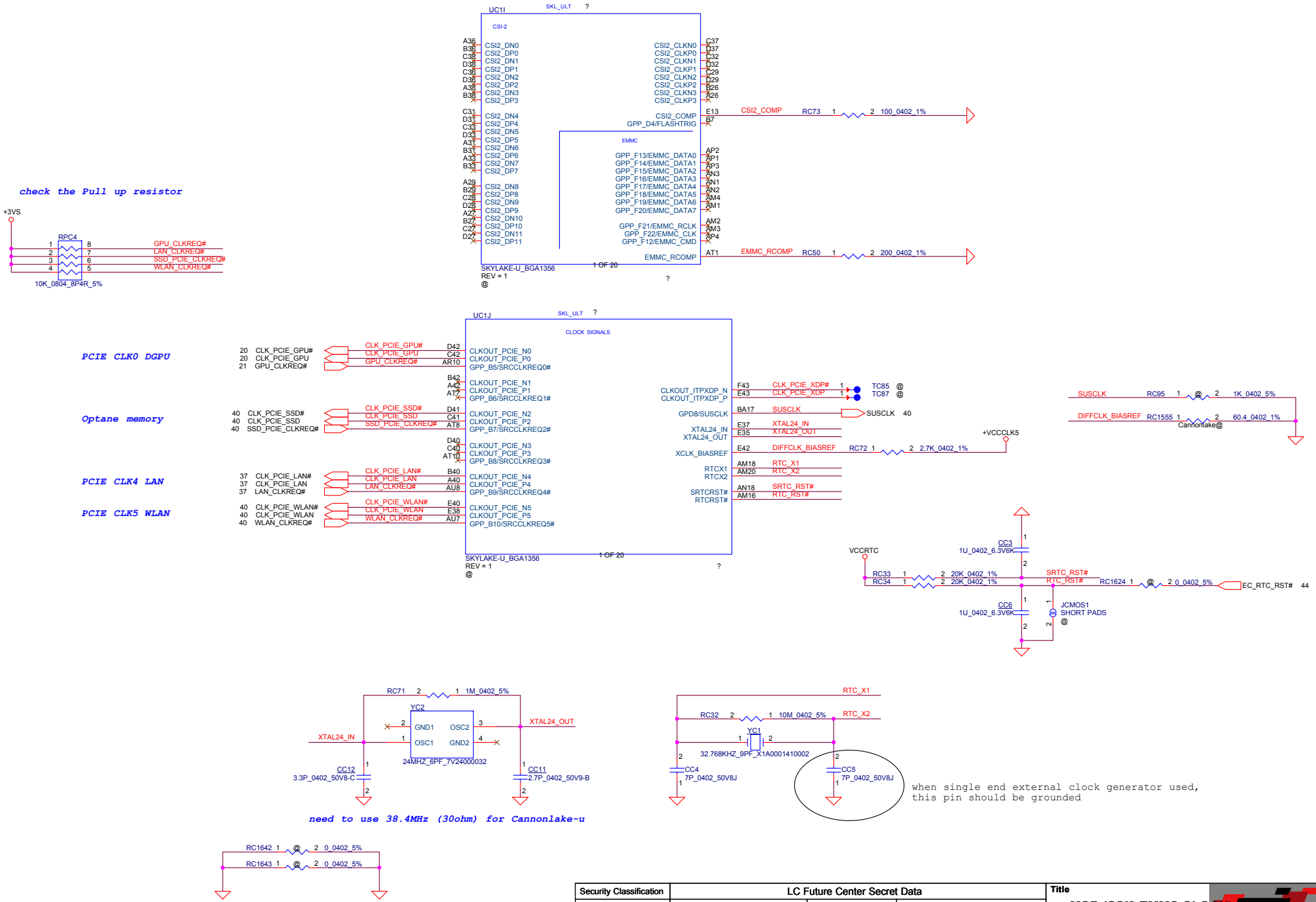

Title: MCP (CSI2,EMMC,CLOCK)

Size	Document Number	Rev
Custom	DG710	0.1

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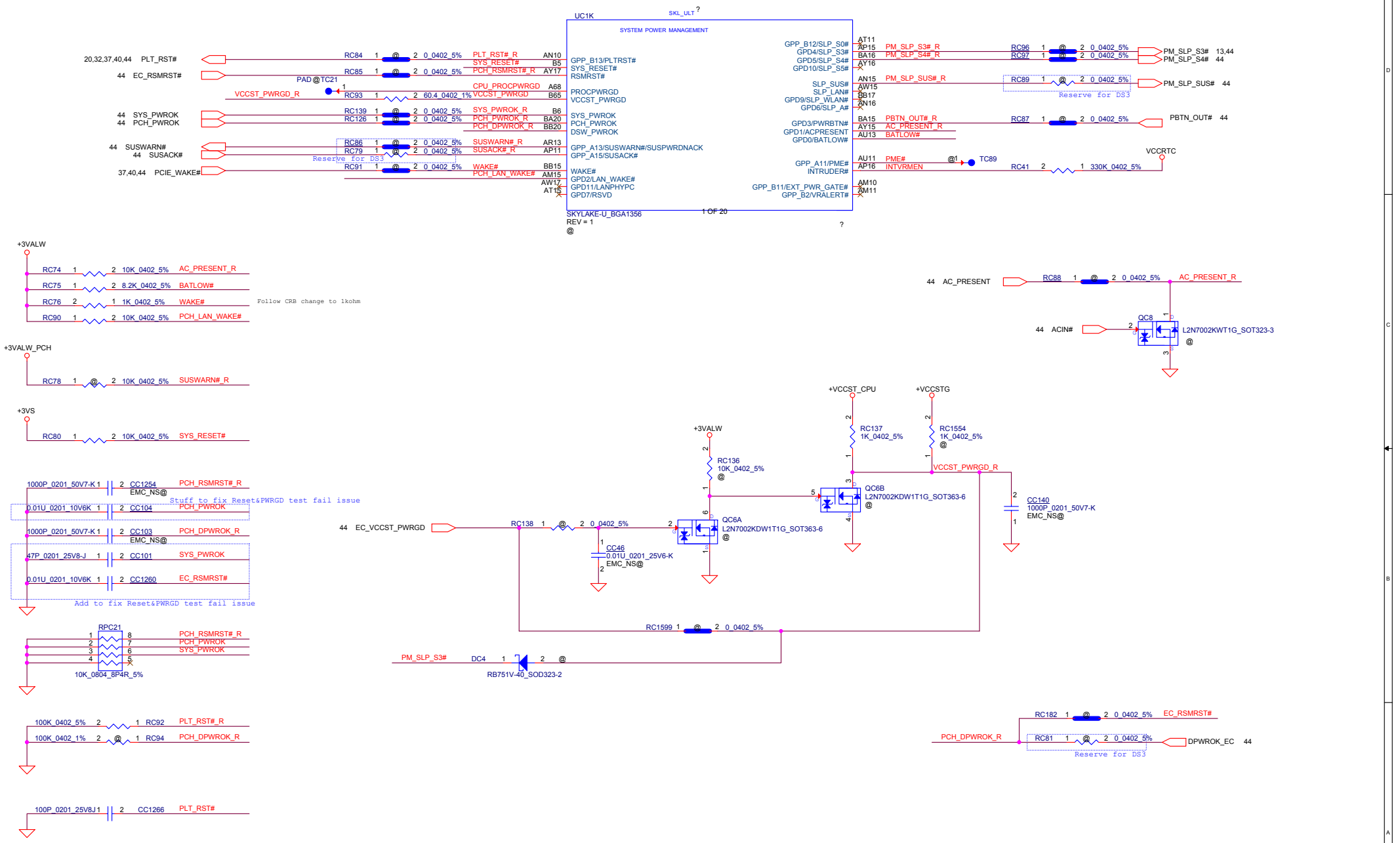

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (SYSTEM PWR MANAGEMENT)

Size	Document Number	Rev
Custom	DG710	0.1

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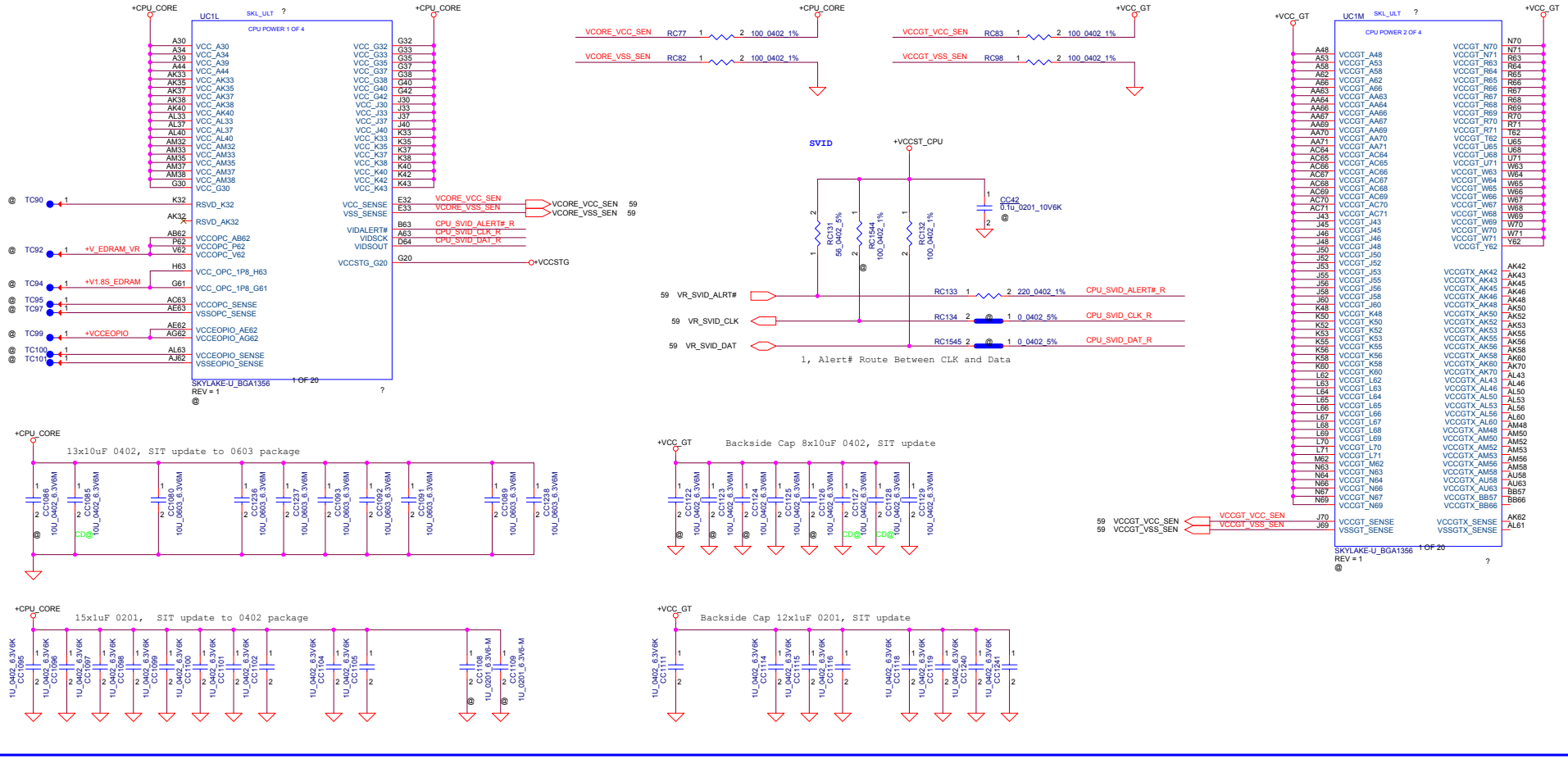

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (CPU PWR1)**

Size	Document Number	Rev
Custom	DG710	0.1

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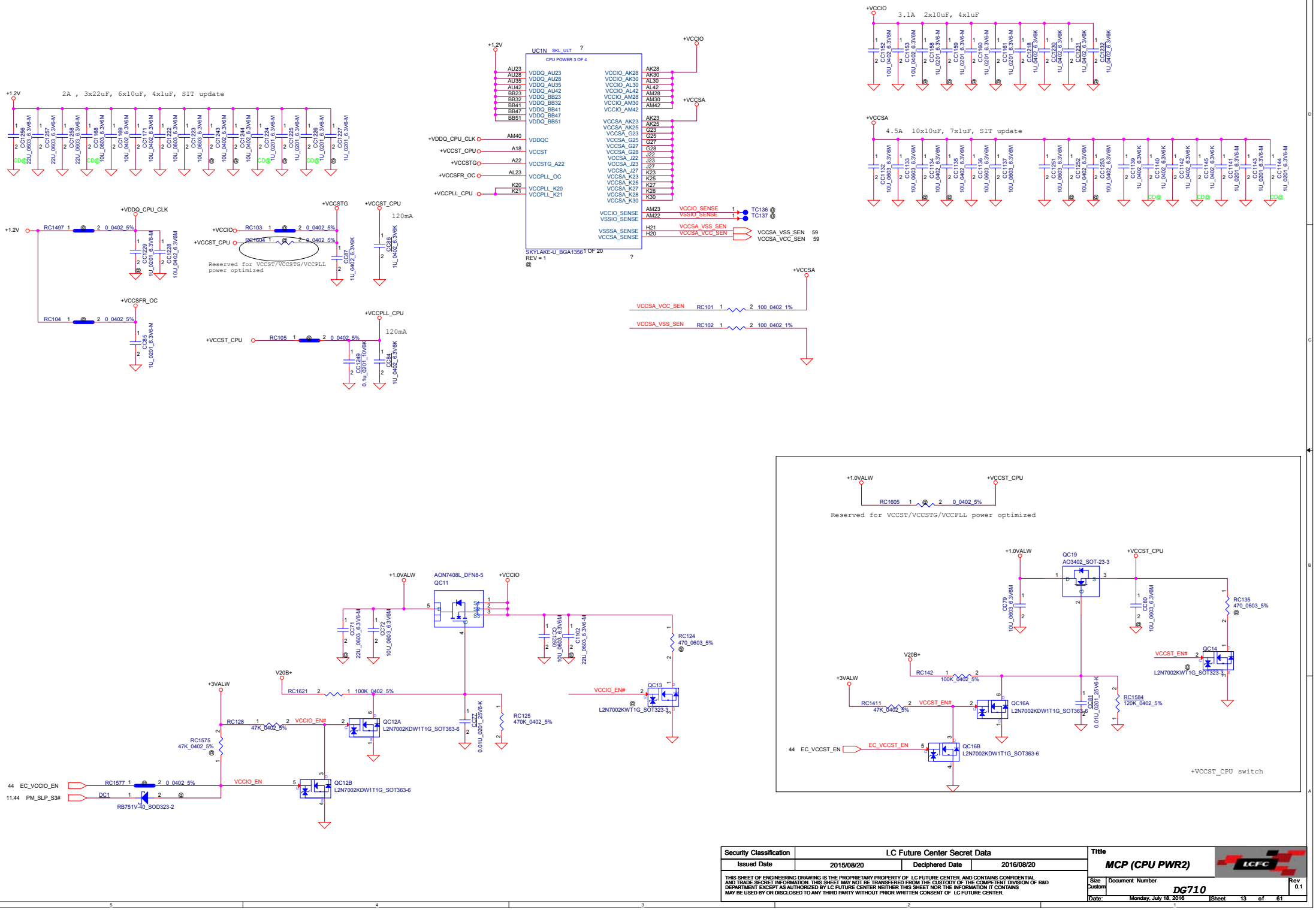

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (CPU PWR2)**

Size	Document Number	Rev
Custom	DG710	0.1

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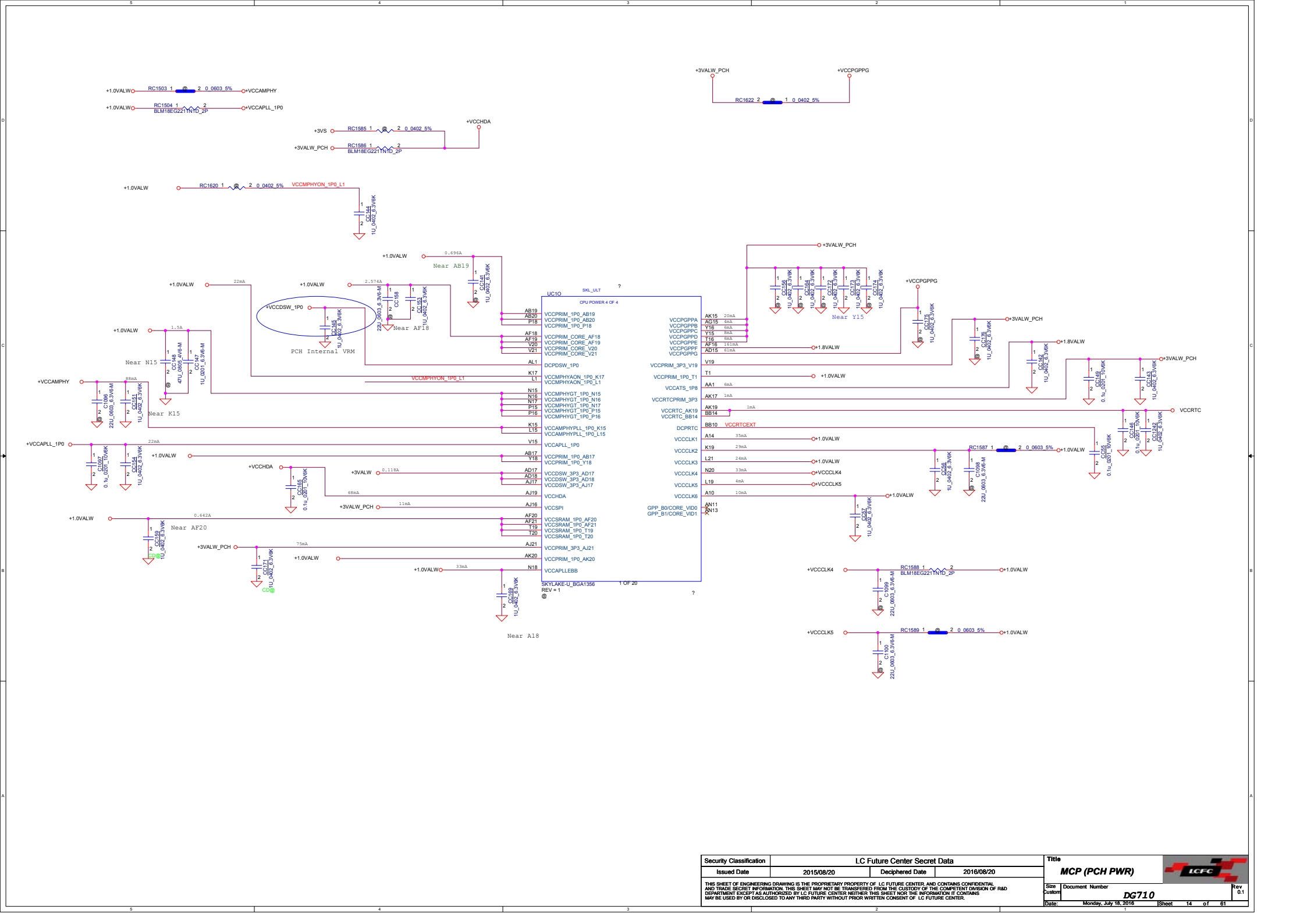

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Title: **MCP (PCH PWR)**

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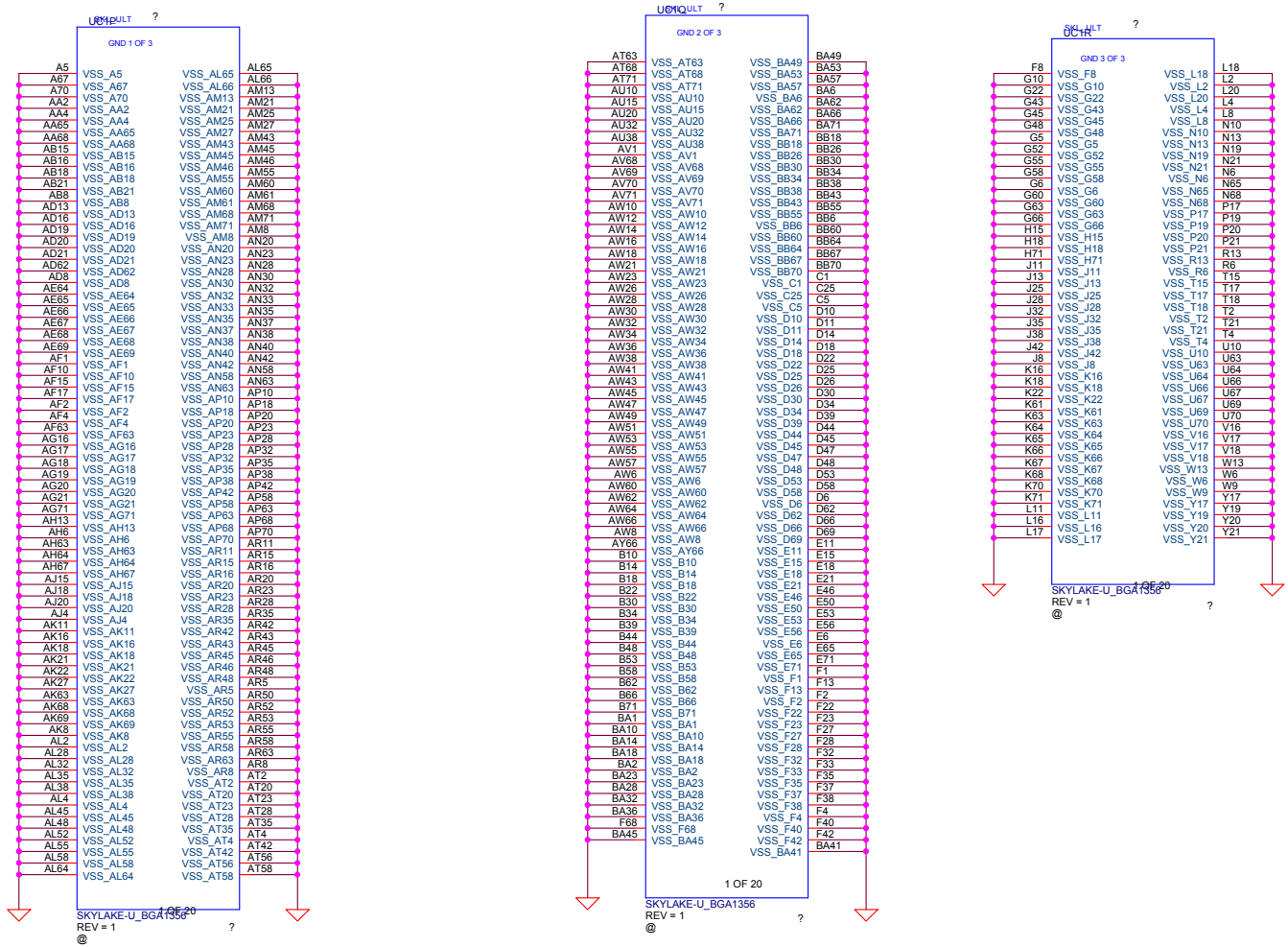

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **MCP (VSS)**

Size	Document Number	Rev
Custom	DG710	0.1

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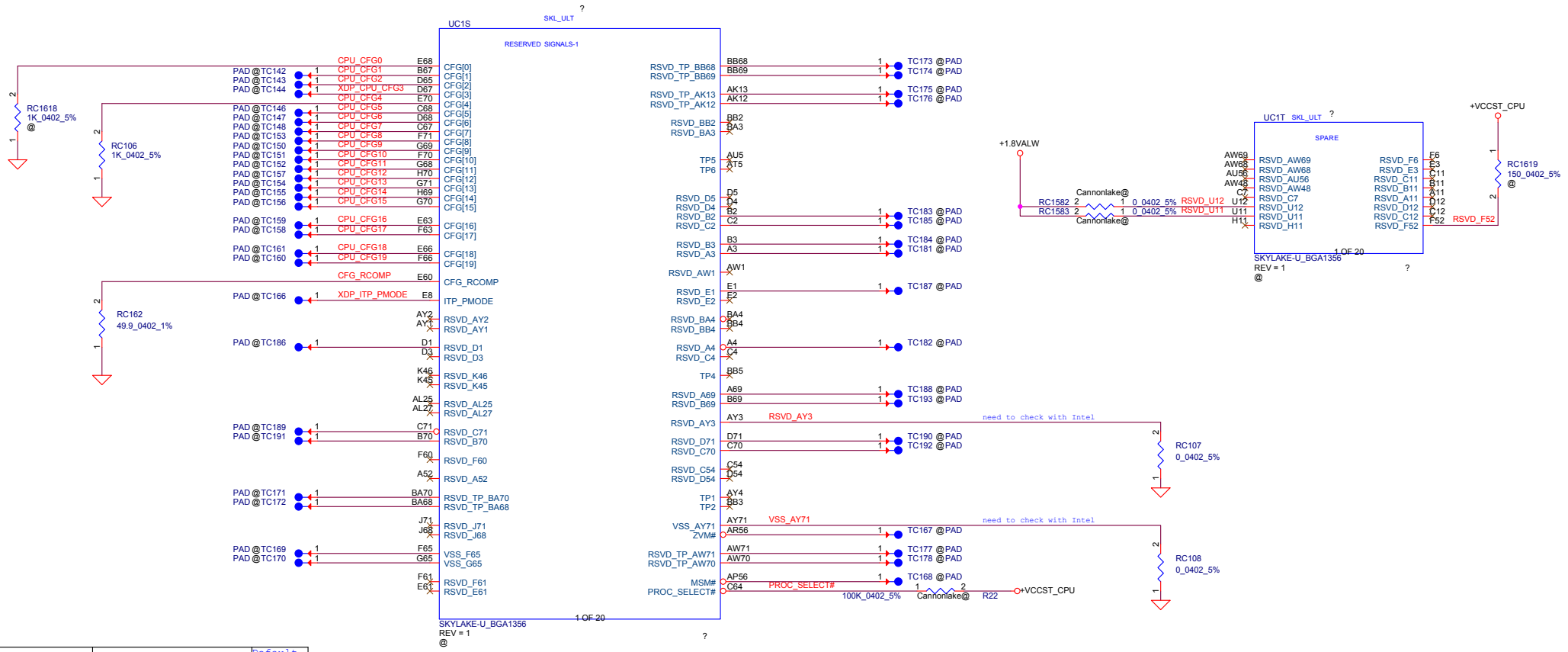

Pin Name	Strap Description	Configuration	Default Value
CFG[4]	Display Port Presence strap	– 1 = eDP Disabled – 0 = eDP Enabled*	1

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Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: MCP (CFG,RESERVED)

Size	Document Number	Rev
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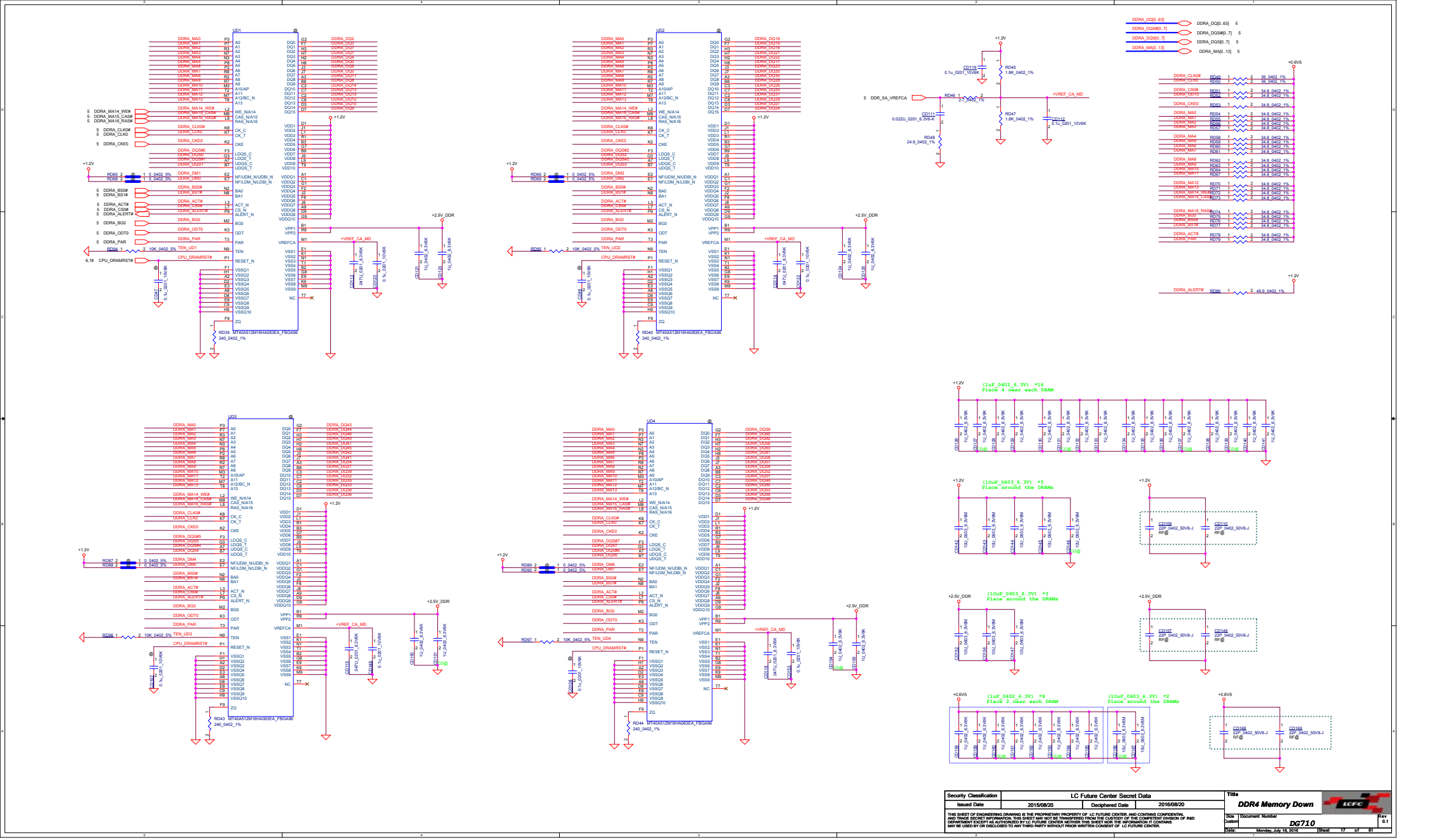

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Title: **DDR4 Memory Down**

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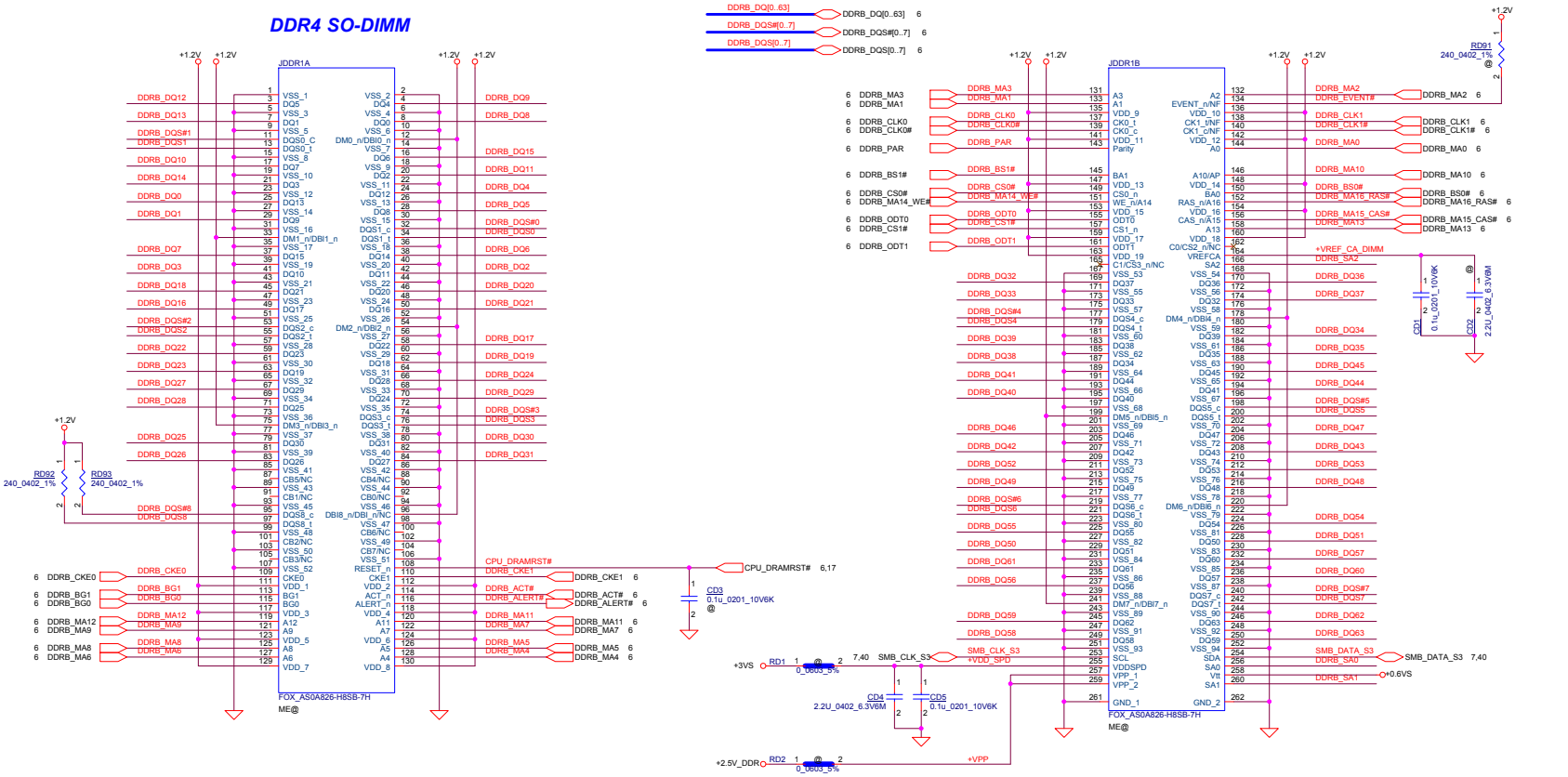
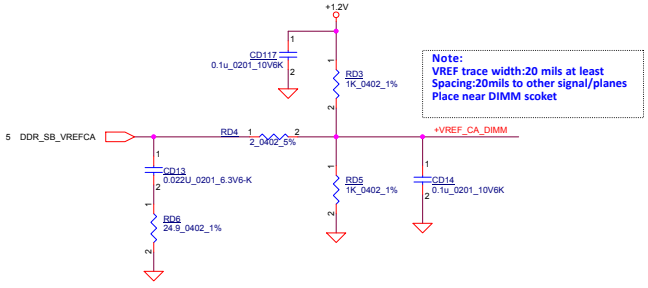
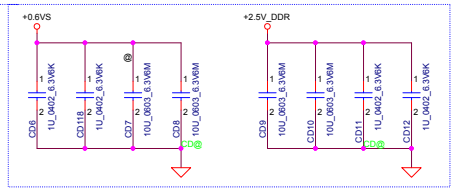
DDR4 SO-DIMM

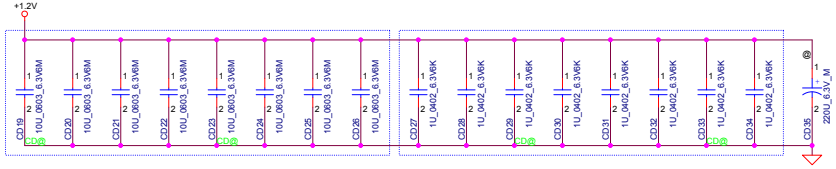


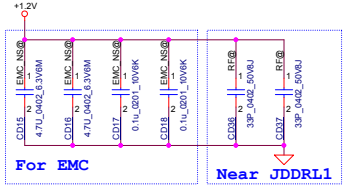


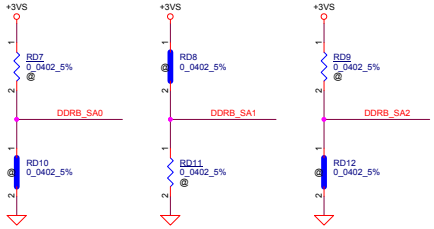
Note:
VREF trace width:20 mils at least
Spacing:20mils to other signal/planes
Place near DIMM scoket

Layout Note:
Place near DIMM









SPD Address = 2H

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Title	DDR4 SO-DIMM		
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Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

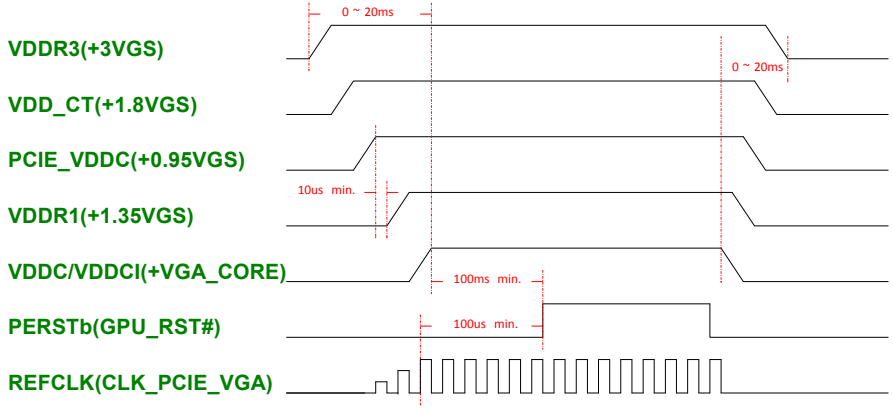
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 µ s before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/µ s).

For power down, reversing the ramp-up sequence is recommended.



VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

Title: VGA Notes List

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9 PCIE_CTX_C_GRX_P[3..0] → PCIE_CTX_C_GRX_P[3..0]
9 PCIE_CTX_C_GRX_N[3..0] → PCIE_CTX_C_GRX_N[3..0]

PCIE_CRX_GTX_P[3..0] → PCIE_CRX_GTX_P[3..0] 9
PCIE_CRX_GTX_N[3..0] → PCIE_CRX_GTX_N[3..0] 9

UV1A

PCIE_CTX_C_GRX_P0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PCIE_CRX_C_GTX_P0	CV1	PX@ 1	2	0.22U_0201_6.3V6-K	PCIE_CRX_GTX_P0
PCIE_CTX_C_GRX_N0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PCIE_CRX_C_GTX_N0	CV2	PX@ 1	2	0.22U_0201_6.3V6-K	PCIE_CRX_GTX_N0
PCIE_CTX_C_GRX_P1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PCIE_CRX_C_GTX_P1	CV3	PX@ 1	2	0.22U_0201_6.3V6-K	PCIE_CRX_GTX_P1
PCIE_CTX_C_GRX_N1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PCIE_CRX_C_GTX_N1	CV4	PX@ 1	2	0.22U_0201_6.3V6-K	PCIE_CRX_GTX_N1
PCIE_CTX_C_GRX_P2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PCIE_CRX_C_GTX_P2	CV5	PX@ 1	2	0.22U_0201_6.3V6-K	PCIE_CRX_GTX_P2
PCIE_CTX_C_GRX_N2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PCIE_CRX_C_GTX_N2	CV6	PX@ 1	2	0.22U_0201_6.3V6-K	PCIE_CRX_GTX_N2
PCIE_CTX_C_GRX_P3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PCIE_CRX_C_GTX_P3	CV7	PX@ 1	2	0.22U_0201_6.3V6-K	PCIE_CRX_GTX_P3
PCIE_CTX_C_GRX_N3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PCIE_CRX_C_GTX_N3	CV8	PX@ 1	2	0.22U_0201_6.3V6-K	PCIE_CRX_GTX_N3
	AB30	PCIE_RX4P	PCIE_TX4P	AC25						
	AA31	PCIE_RX4N	PCIE_TX4N	AB25						
	AA29	PCIE_RX5P	PCIE_TX5P	Y23						
	Y28	PCIE_RX5N	PCIE_TX5N	Y24						
	Y30	PCIE_RX6P	PCIE_TX6P	AB27						
	W31	PCIE_RX6N	PCIE_TX6N	AB26						
	W29	PCIE_RX7P	PCIE_TX7P	Y27						
	V28	PCIE_RX7N	PCIE_TX7N	Y26						
	V30	NC#V30	NC#W24	W24						
	U31	NC#U31	NC#W23	W23						
	U29	NC#U29	NC#V27	V27						
	T28	NC#T28	NC#U26	U26						
	T30	NC#T30	NC#U24	U24						
	R31	NC#R31	NC#U23	U23						
	R29	NC#R29	NC#T26	T26						
	P28	NC#P28	NC#T27	T27						
	P30	NC#P30	NC#T24	T24						
	N31	NC#N31	NC#T23	T23						
	N29	NC#N29	NC#P27	P27						
	M28	NC#M28	NC#P26	P26						
	M30	NC#M30	NC#P24	P24						
	L31	NC#L31	NC#P23	P23						
	L29	NC#L29	NC#M27	M27						
	K30	NC#K30	NC#N26	N26						

PCI EXPRESS INTERFACE

CLOCK

10 CLK_PCIE_GPU → CLK_PCIE_GPU AK30 PCIE_REFCLKP
10 CLK_PCIE_GPU# → CLK_PCIE_GPU# AK32 PCIE_REFCLKN

1K_0402_1% 1 PX@ 2 RV4 → N10 TEST_PG

21 GPU_RST# → GPU_RST# AL27 PERSTB

CALIBRATION

+0.95VGS
Y22 PCIE_CALR_TX — RV3 1 PX@ 2 1.69K_0402_1%
AA22 PCIE_CALR_RX — RV5 1 PX@ 2 1K_0402_1%

R16M-M1-30
EXO@

RV6 100K_0402_5% PX@

RV7 1 @ 2 0_0402_5%

+3VGS

UV2
MC74VHC1G08DFT2G_SC70-5
PX@

8 PXS_RST#
11|32,37,40,44 PLT_RST#
GPU_RST#

GPU_RST# → DV3 → VGA_PWROK → VGA_PWROK 58
8,58 VR_VGA_PWRGD → VR_VGA_PWRGD
LBAT54AWT1G_SOT323-3
PX@

with BOM strcture control, CV1--CV8 change to 0.22uf for CZ

change the GPU PN to AMD(EXO-S3 PRO), symbol check ok

11/4 change to PC sample SA000074V10

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Title: ATI_JET-LE_PCIE

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CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0. 100 = 256MB	x
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	x
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported. 0= Not support	x
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled. 1= Enable	x
PS_2[1]	N/A	Reserved.	NA
PS_2[2]	N/A	Reserved.	NA
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device. 0= Disable	x
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system' s VGA controller.	0
PS_2[5]	N/A	Reserved	NA
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 100 = Hynix 1G 000 = Hynix 2G 111 = Micron 1G 010 = Micron 2G 110 = Samsung 1G 001 = Samsung 2G	x
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 111= No usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	x

MLPS	Bit					BOM		
	5	4	3	2	1	R_pu ( )	R_pd ( )	C(nF)
PS_0[5:1]	1	1	0	0	1	RV71=8.45k	RV77=2K	CV15=NC
PS_1[5:1]	1	1	0	0	0	RV74=NC	RV77=4.75K	CV16=NC
PS_2[5:1]	1	1	0	0	0	RV60=NC	RV69=4.75K	CV18=NC
PS_3[5:1]	1	1	X	X	X	RV63=X76	RV70=X76	CV19=X76

with BOM strcture control,
RV63,RV70 change to different value to adjust VRAM config

with BOM strcture control,
when config PEG3
RV74 change to 8.45K,
RV80 change to 2K

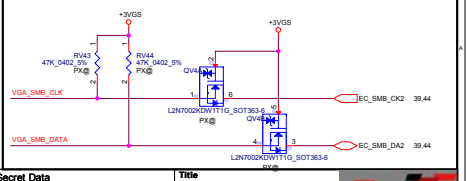
Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

SVC	SVD	Output Voltage (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Internal VGA Thermal Sensor



Connect GPIO_28 to 10K pull down to enable MLPS.

no symbol for 8pf cap, PLM has PN,change the PN

(1.8V@20mA TSVDD)

For Topaz, RV16/RV19 stuff 100ohm
for EXO, RV16/RV19 stuff 0hm.

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Title: ATI_JET-LE_Main_MSIC

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Title: ATI_JET-LE_TMDP

Size	Document Number	Rev
Custom	DG710	0.1

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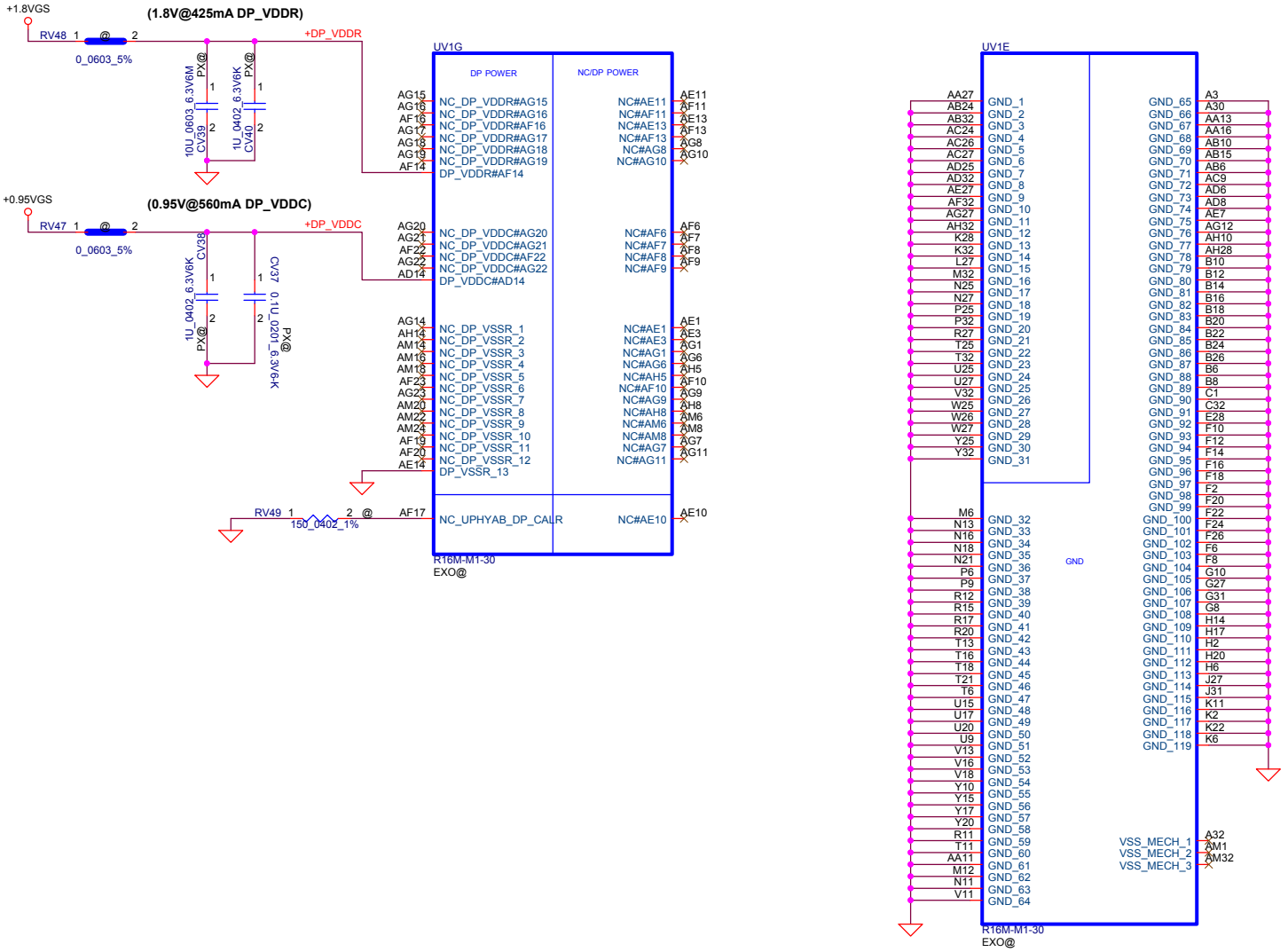

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_DP Power

Size	Document Number	Rev
Custom	DG710	0.1

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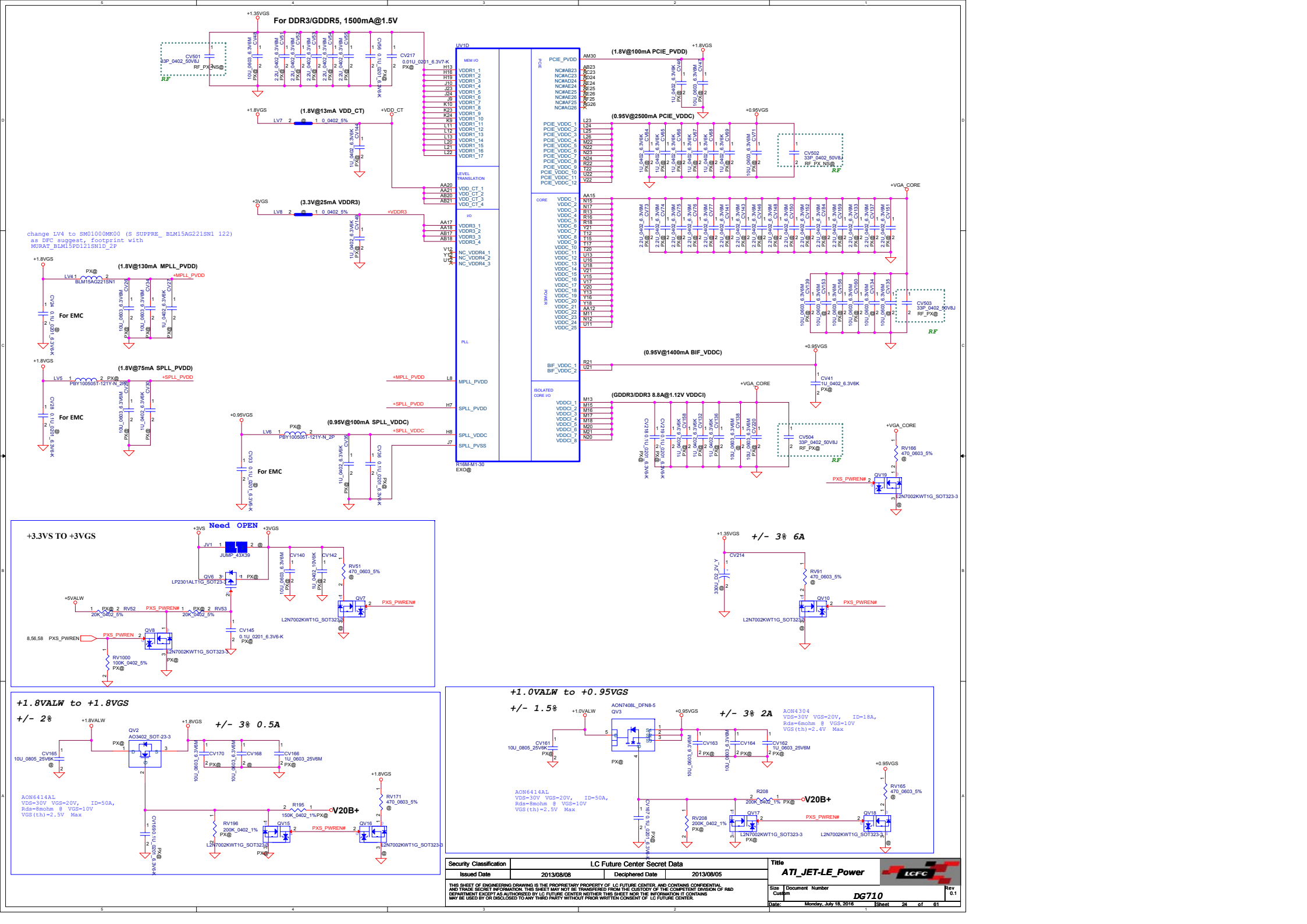
For DDR3/GDDR5, 1500mA@1.5V
change LV4 to SM01000MK00 (S SUPPRE_ BLM15AG221SN1 122)
as DFC suggest, footprint with
MURAT_BLM15PD121SN1D_2P
(1.8V@100mA PCIE_PVDD)
(0.95V@2500mA PCIE_VDDC)
(1.8V@13mA VDD_CT)
(3.3V@25mA VDDR3)
(1.8V@130mA MPLL_PVDD)
(1.8V@75mA SPLL_PVDD)
(0.95V@100mA SPLL_VDDC)
(0.95V@1400mA BIF_VDDC)
(GDDR3/DDR3 8.8A@1.12V VDDCI)
+VGA_CORE
For EMC
+3.3VS TO +3VGS
Need OPEN
+1.8VALW to +1.8VGS
+/- 2%
+/- 3% 0.5A
+/- 3% 6A
+1.0VALW to +0.95VGS
+/- 1.5%
+/- 3% 2A
AON6414AL
VDS=30V VGS=20V, ID=50A,
Rds=8mohm @ VGS=10V
VGS(th)=2.5V Max
AON7408L_DFN8-5
AON4304
VDS=30V VGS=20V, ID=18A,
Rds=6mohm @ VGS=10V
VGS(th)=2.4V Max
V20B+
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/08
Deciphered Date
2013/08/05
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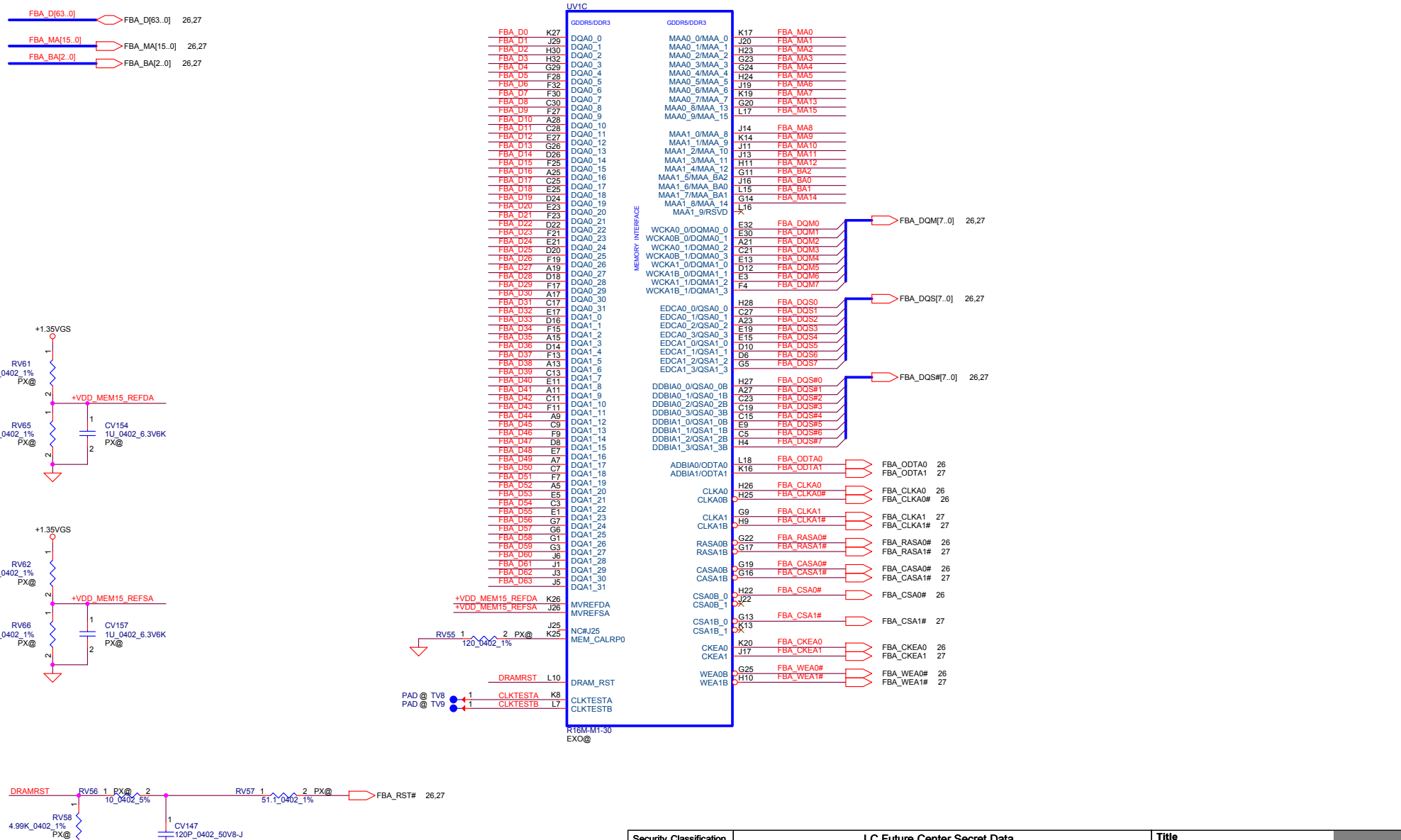

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Title: ATI_JET-LE_MEM IF

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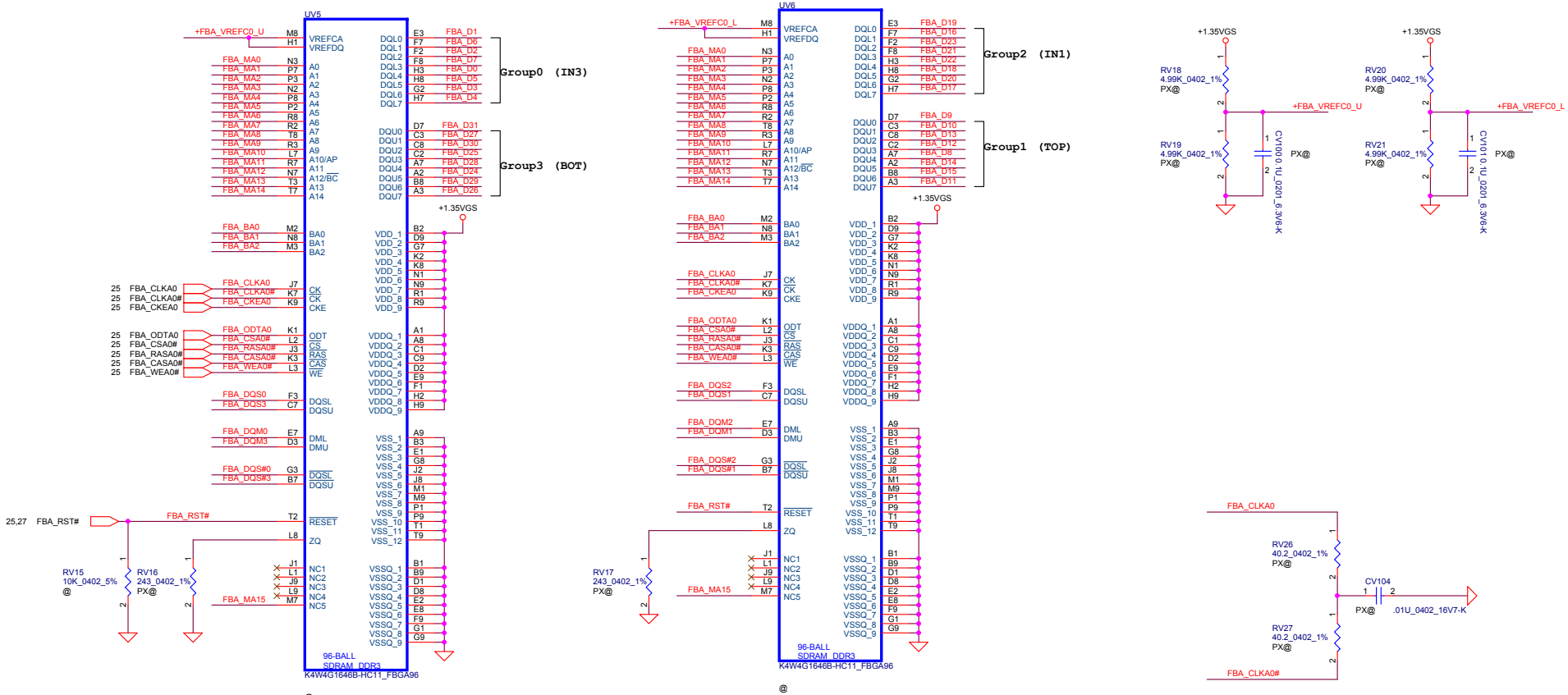
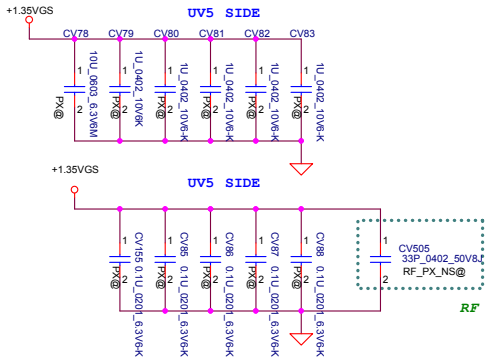
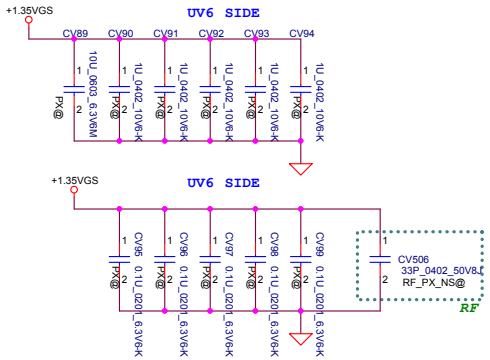
Memory Partition A - Lower 32 bits

FBA_MA[15..0] 25,27
FBA_BA[2..0] 25,27
FBA_DQS[3..0] 25
FBA_DQM[3..0] 25
FBA_DQS#[3..0] 25
FBA_D[31..0] 25







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: ATI_JET-LE_VRAM_A

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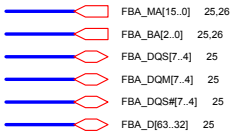
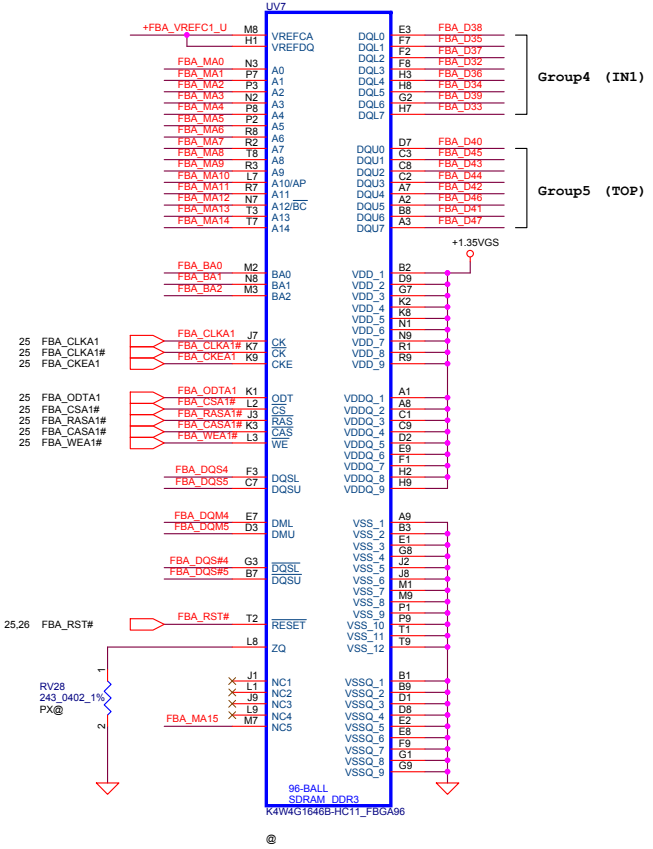
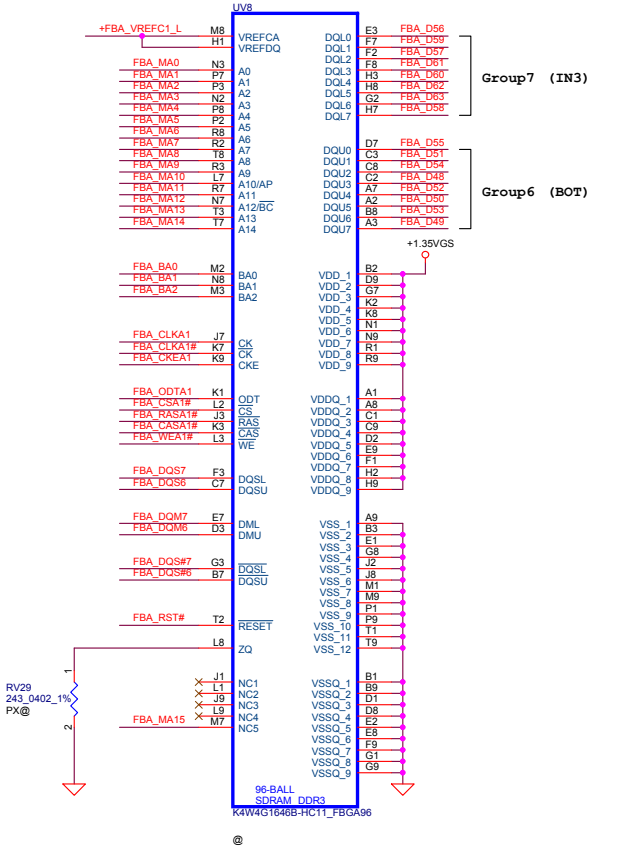
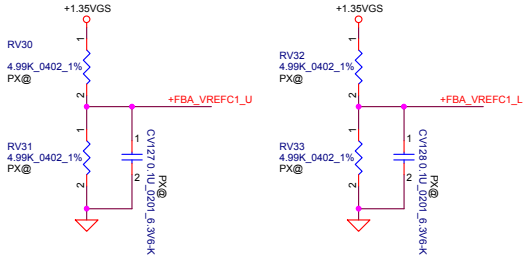
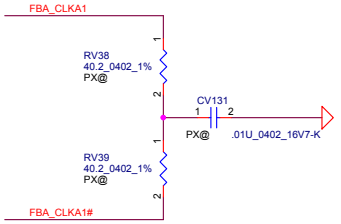
Memory Partition A - Upper 32 bits

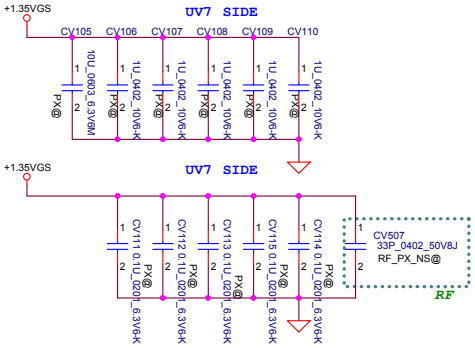


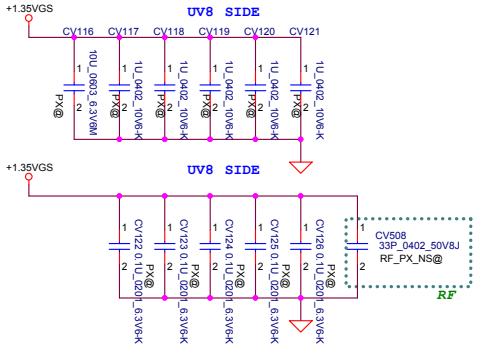












Title: ATI_JET-LE_VRAM_B

LCFC

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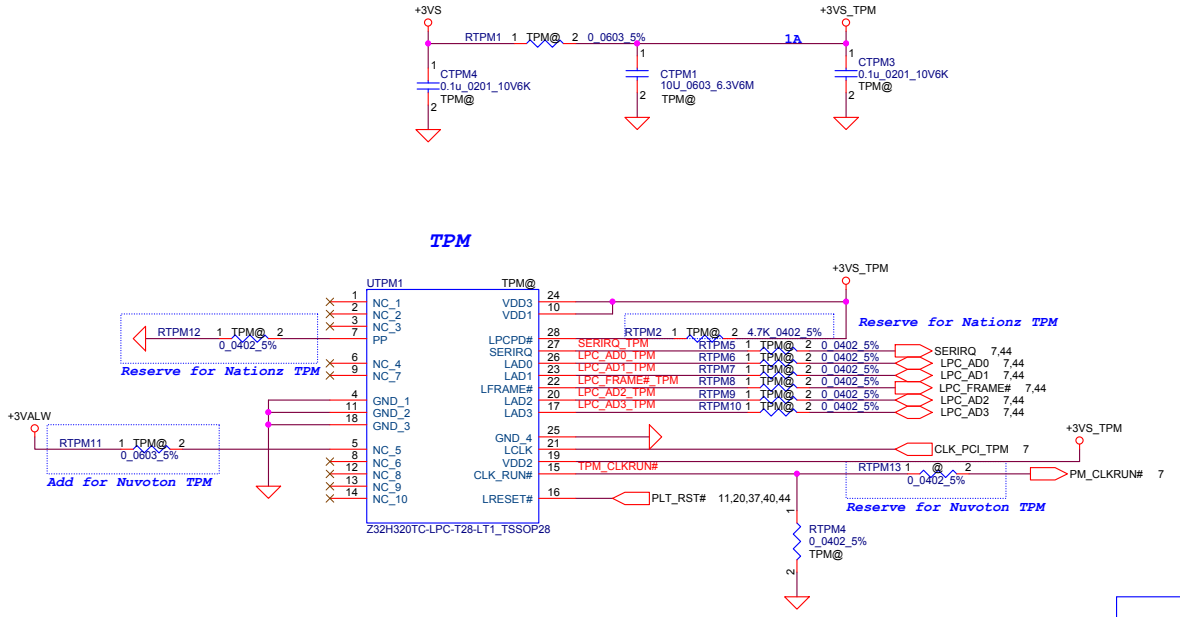

	Nationz TPM	Nuvoton TPM
RTPM2	Stuff	NC
RTPM12	Stuff	NC
RTPM11	NC	Stuff

Security Classification	LC Future Center Secret Data		
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Title: TPM

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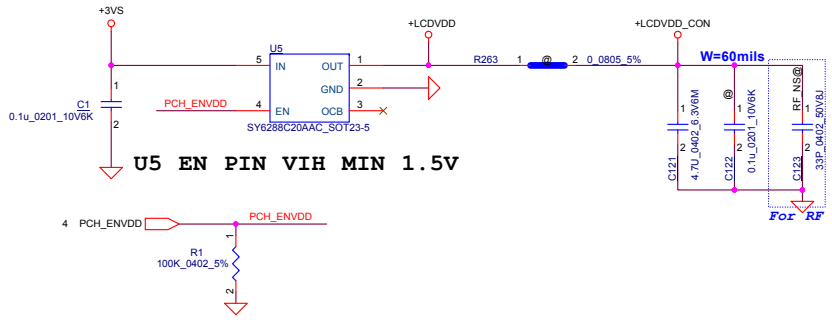
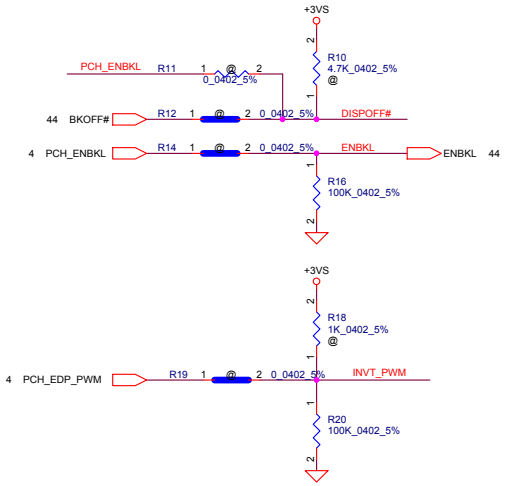
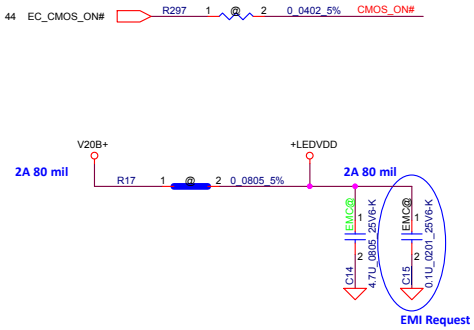
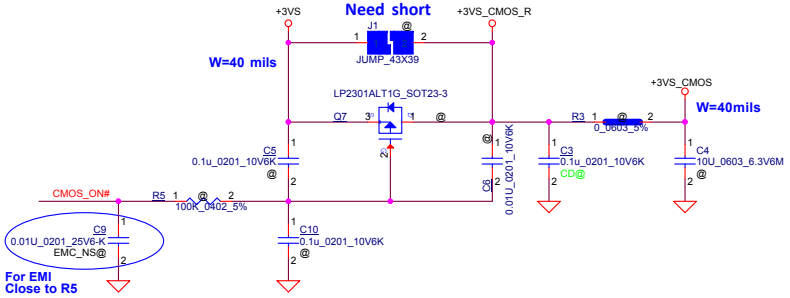
LCD POWER CIRCUIT

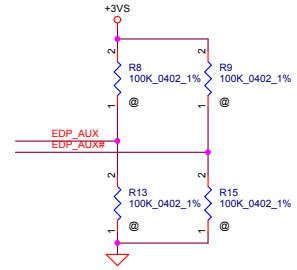


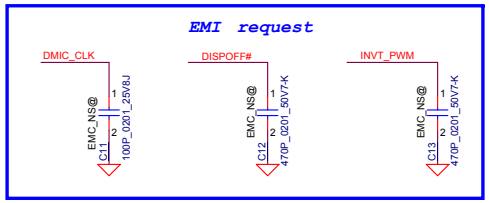


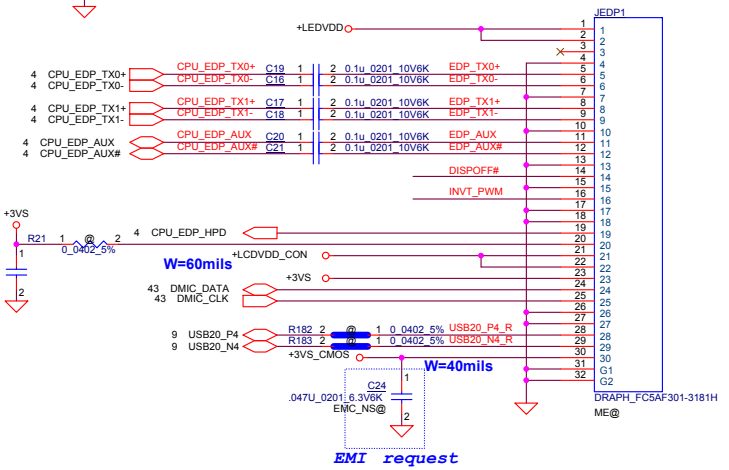


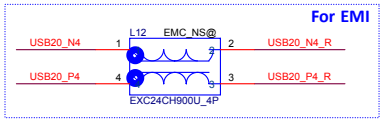
CMOS Camera











Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **eDP/CMOS**

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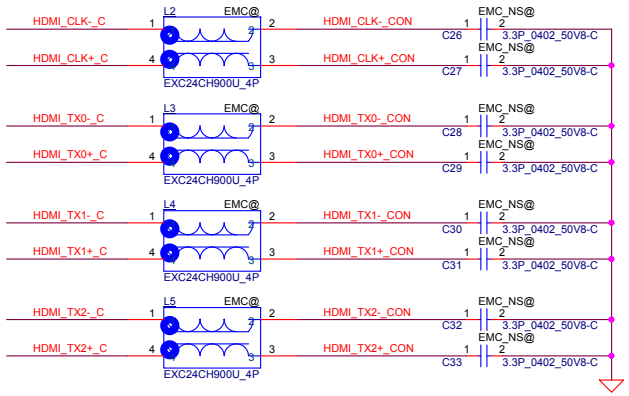
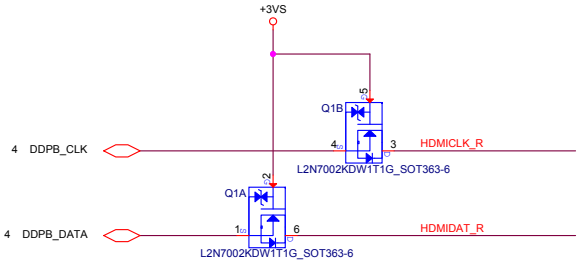
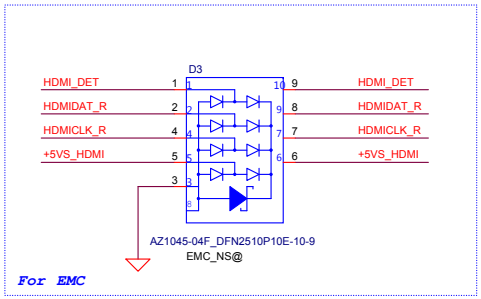
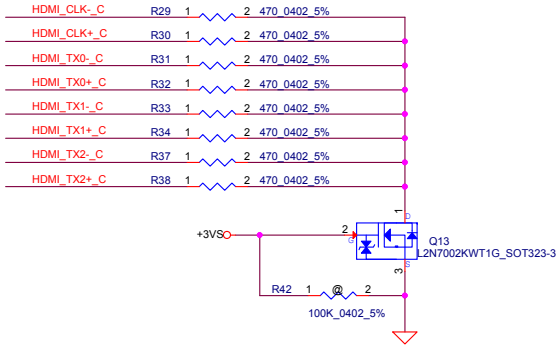


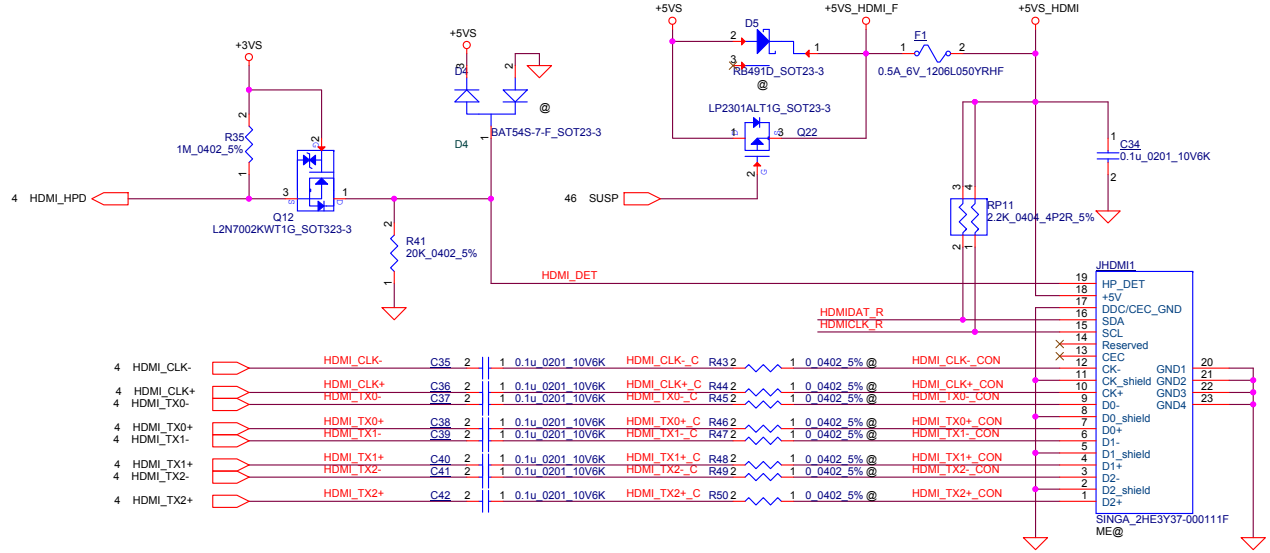
For EMC



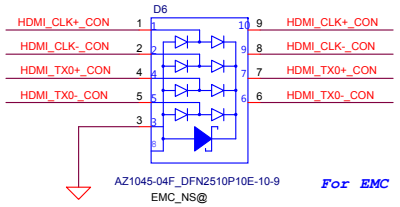


For EMC

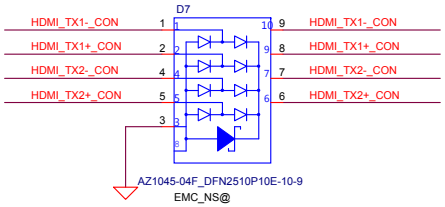




Close to JHDMI1



For EMC



Security Classification	LC Future Center Secret Data		
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Title: **HDMI_CONN**

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+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%)
0.5ms < spec < 10.0ms

+3VALW
Need short
+3VALW_LAN
JL1 1 2 @
JUMP_43X79
width : 40 mils

CL4 1 2 @ 4.7U_0603_6.3V6K
CL5 1 2 @ 4.7U_0603_6.3V6K
CL6 1 2 0.1U_0201_6.3V6-K
CL7 1 2 0.1U_0201_6.3V6-K

Close to Pin11
Close to Pin32
Close to Pin11
Close to Pin32

+3VALW_LAN
RL11 1 @ 2 0_0603_5%
+LAN_VDDREG
40mil
CL1 1 2 4700P_0603_50V7K
CL2 1 2 56P_0201_50V8-J

+3VALW_LAN
RL5 2 1 10K_0402_5% @
11,40,44 PCIE_WAKE#
40,44 LAN_WAKE#
RL7 1 @ 2 0_0402_5%
RL10 1 @ 2 0_0402_5%
PCIE_WAKE#_R

+3VALW_LAN
+3VS
RL4 2 1 10K_0402_5% @
LAN_CLKREQ#_R
QL1 L2N7002KWT1G_SOT323-3
RL18 1 @ 2 0_0402_5%
LAN_CLKREQ# 10

+3VS
RL9 1 2 1K_0402_1%
ISOLATE#
RL11 1 2 15K_0402_5% @

+3VALW_LAN
RL21 2 1 10K_0402_5% @
LAN_DISABLE#
PLT_RST#
CL34 1 2 0.1u_0201_10V6K EMC_NS@

UL1

	GND	33			
	AVDD33	32			
	RSET	31			
	AVDD10_1	30			
	CKXTAL2	29			
	CKXTAL1	28			
	LED0	27			
	GPO	26			
	LED1	25			
	NC_6	24			
	DVDD33	23			
	NC_5	22			
	LANWAKEB	21			
	ISOLATEB	20			
	PERSTB	19			
	HSON	18			
	HSOP	17			
REFCLK_N		16	CLK_PCIE_LAN#		CLK_PCIE_LAN# 10
REFCLK_P		15	CLK_PCIE_LAN		CLK_PCIE_LAN 10
HSIN		14	PCIE_PTX_C_DRX_N3		PCIE_PTX_C_DRX_N3 9
HSIP		13	PCIE_PTX_C_DRX_P3		PCIE_PTX_C_DRX_P3 9
CLKREQB		12	LAN_CLKREQ#_R		
NC_4		11	+3VALW_LAN		
NC_3		10	LAN_MDI3-		LAN_MDI3- 38
NC_2		9	LAN_MDI3+		LAN_MDI3+ 38
AVDD10_0		8	+LAN_VDD10		
NC_1		7	LAN_MDI2-		LAN_MDI2- 38
NC_0		6	LAN_MDI2+		LAN_MDI2+ 38
MDIN1		5	LAN_MDI1-		LAN_MDI1- 38
MDIP1		4	LAN_MDI1+		LAN_MDI1+ 38
NC_7		3	+LAN_VDD10		
MDIN0		2	LAN_MDI0-		LAN_MDI0- 38
MDIP0		1	LAN_MDI0+		LAN_MDI0+ 38

RTL8106E-CG_QFN32_4X4

RL8 1 2 2.49K_0402_1%
TL3 @ 1
TL4 @ 1

11,20,32,40,44 PLT_RST#
9 PCIE_PRX_DTX_N3
9 PCIE_PRX_DTX_P3
CL10 1 2 0.1U_0201_6.3V6-K
CL11 1 2 0.1U_0201_6.3V6-K

CL10 close to Pin18
CL11 close to Pin17

YL1
OSC1 GND2 4
GND1 OSC2 3
25MHZ_10PF_7V25000014
LAN_XTALI
LAN_XTALO
CL12 12P_0402_50V8-J
CL13 10P_0402_50V8J

For RTL8111H (LDO mode)

+LAN_REGOUT
CL33 1 2 0.1U_0201_6.3V6-K @
60mil
RL6 1 @ 2 0_0805_5%
LL1 1 @ 2 2.2UH_NLC252018T-2R2J-N_5%
60mil
CL15 4.7U_0603_6.3V6K @
CL16 0.1U_0201_6.3V6-K @

+LAN_VDD10
CL17 1U_0201_6.3V6-M
CL18 4700P_0201_25V7-K
CL19 0.1U_0201_6.3V6-K
CL20 0.1U_0201_6.3V6-K
@
Close to Pin3, 8, 22, 30

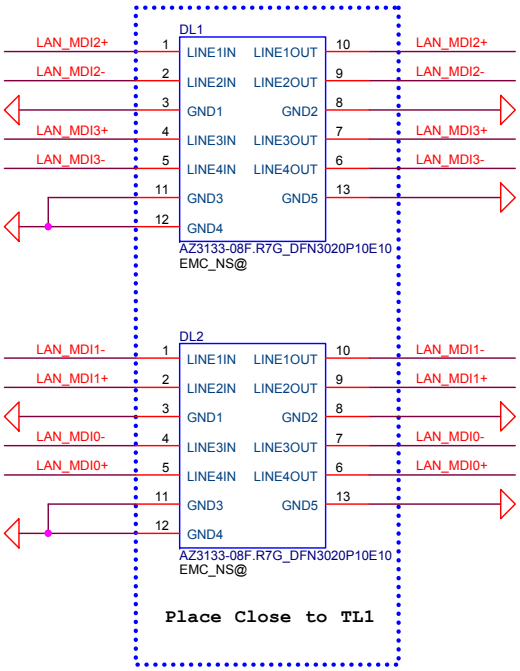
CL21 1U_0402_6.3V6K
CL22 0.1U_0201_6.3V6-K @
Close to Pin22(Reserved)

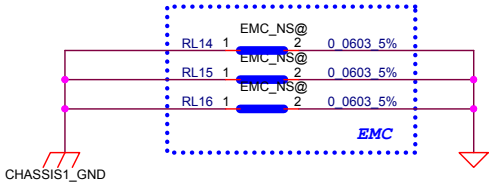
Layout Note: RL6,CL16 must be within 200mil to Pin36,
+LAN_REGOUT: Width =60mil

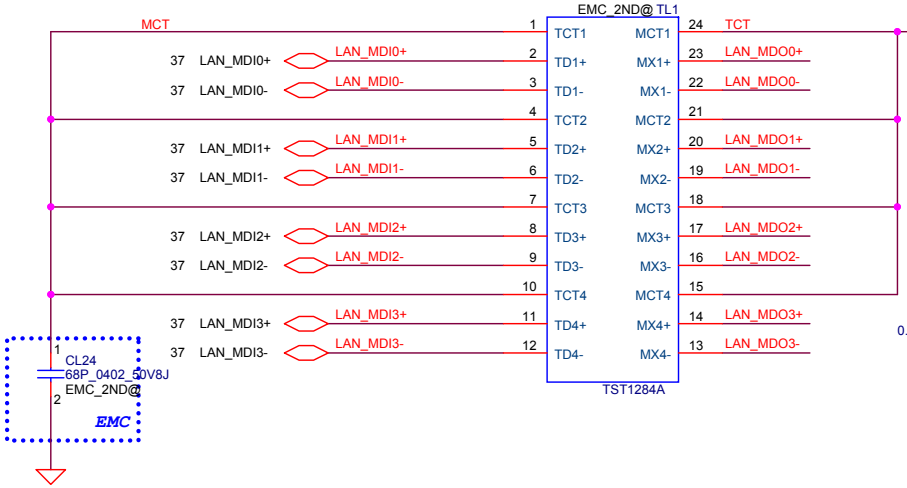
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

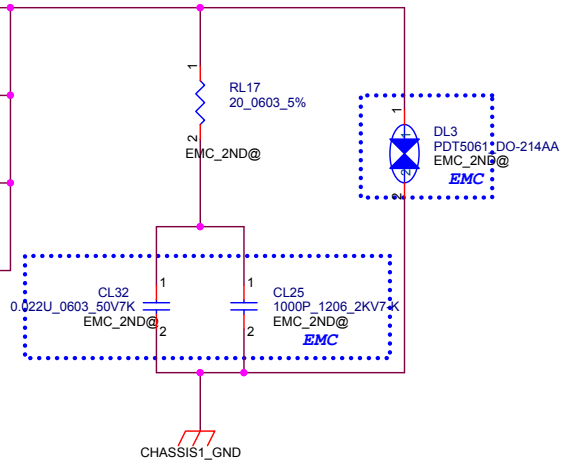
Title: LAN_RTL8106ECG
Size: Custom
Document Number: DG710
Rev: 0.1
Date: Monday, July 18, 2016
Sheet 37 of 61

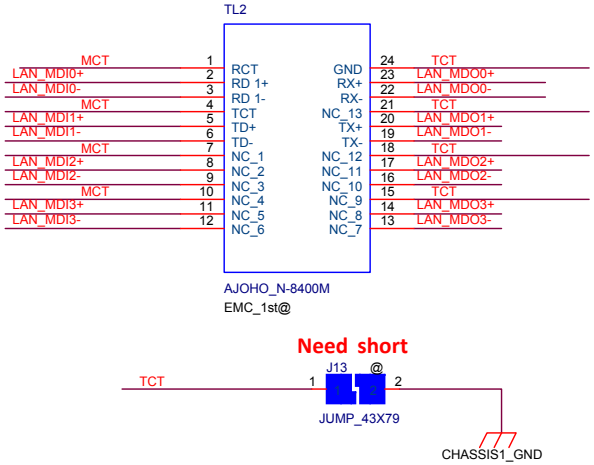
DL1/DL2
1'S PN:SC300003M00

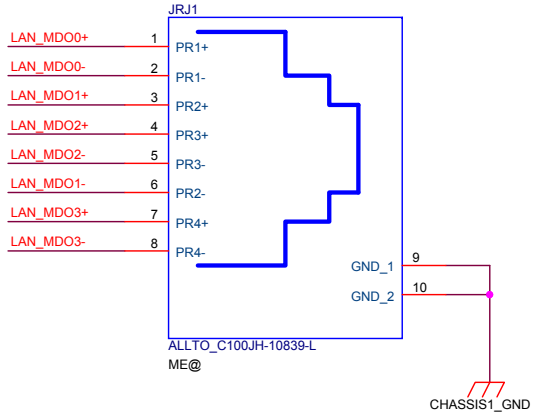






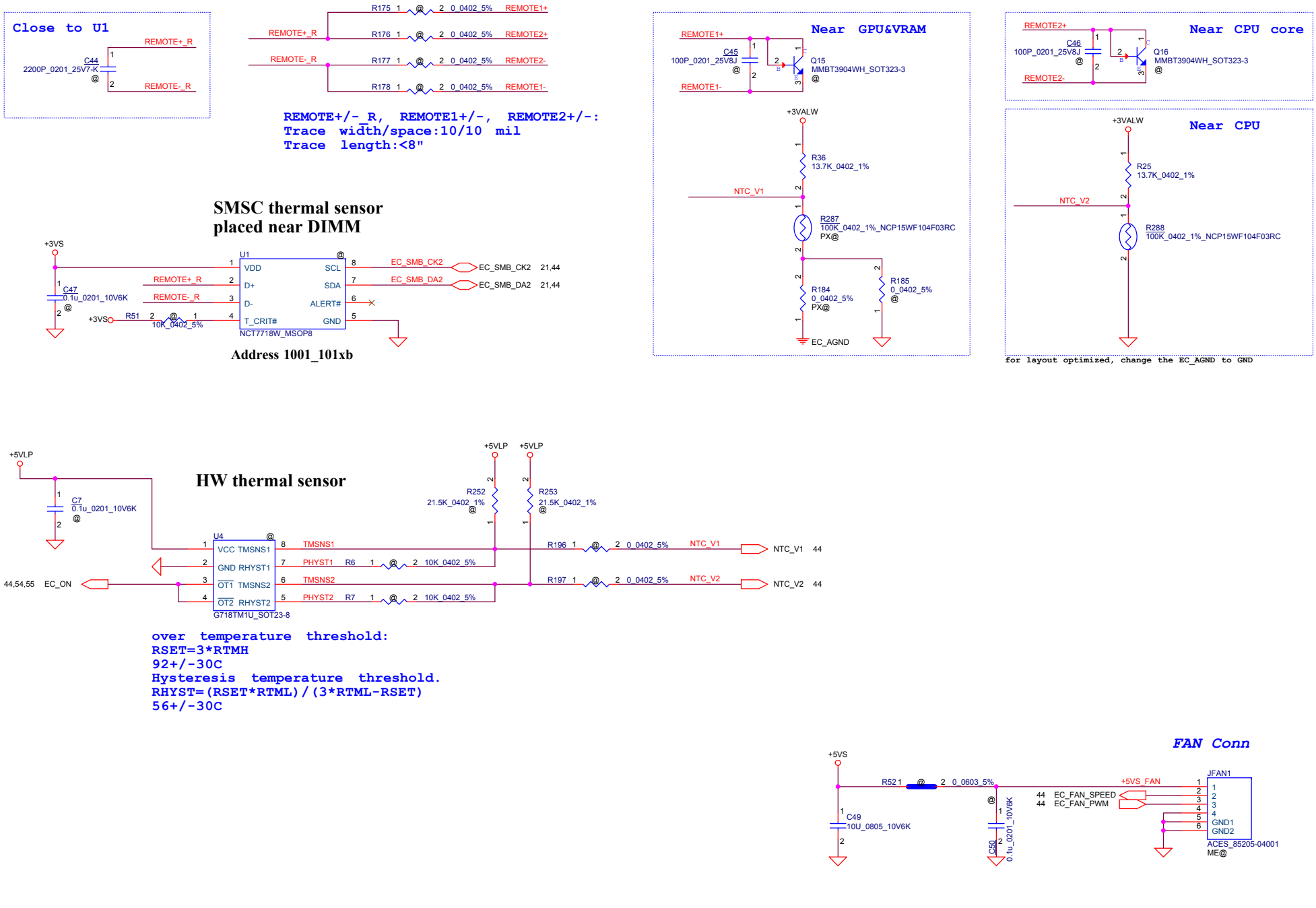






Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	LAN_Transformer		
Size B	Document Number DG710		Rev 0.1
Date: Monday, July 18, 2016	Sheet 38 of 61		



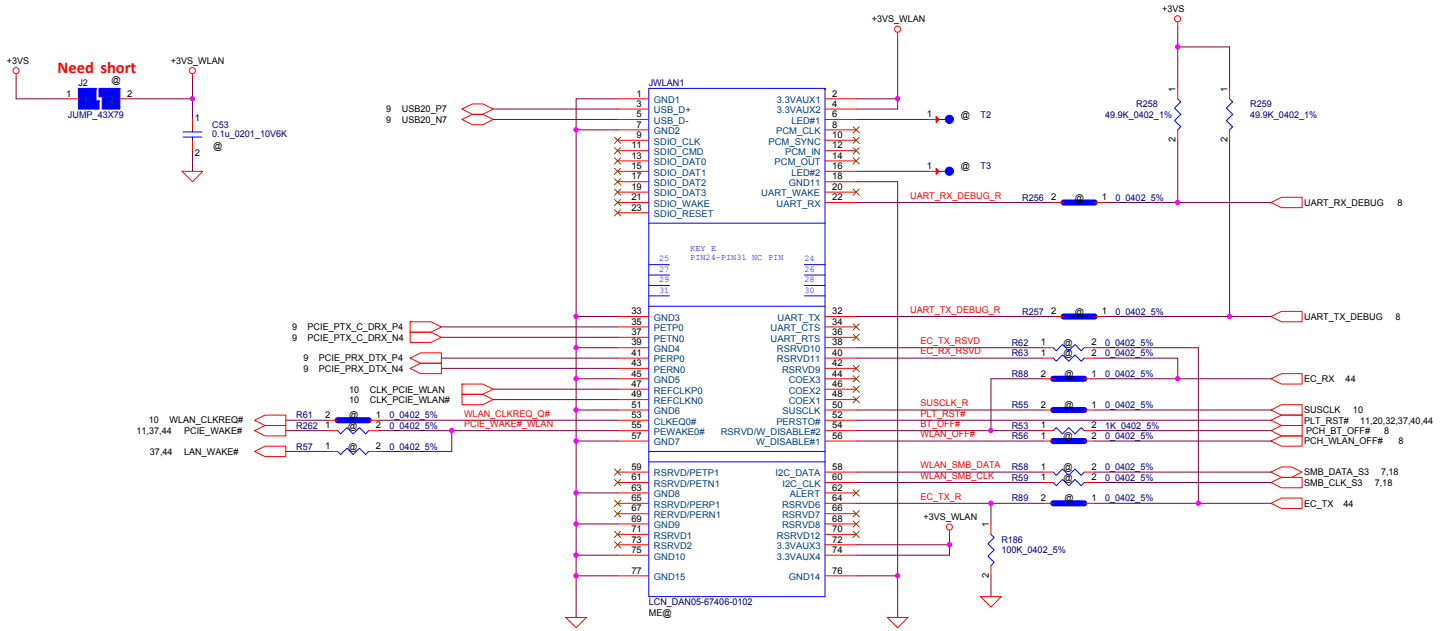
Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Thermal sensor/FAN CONN

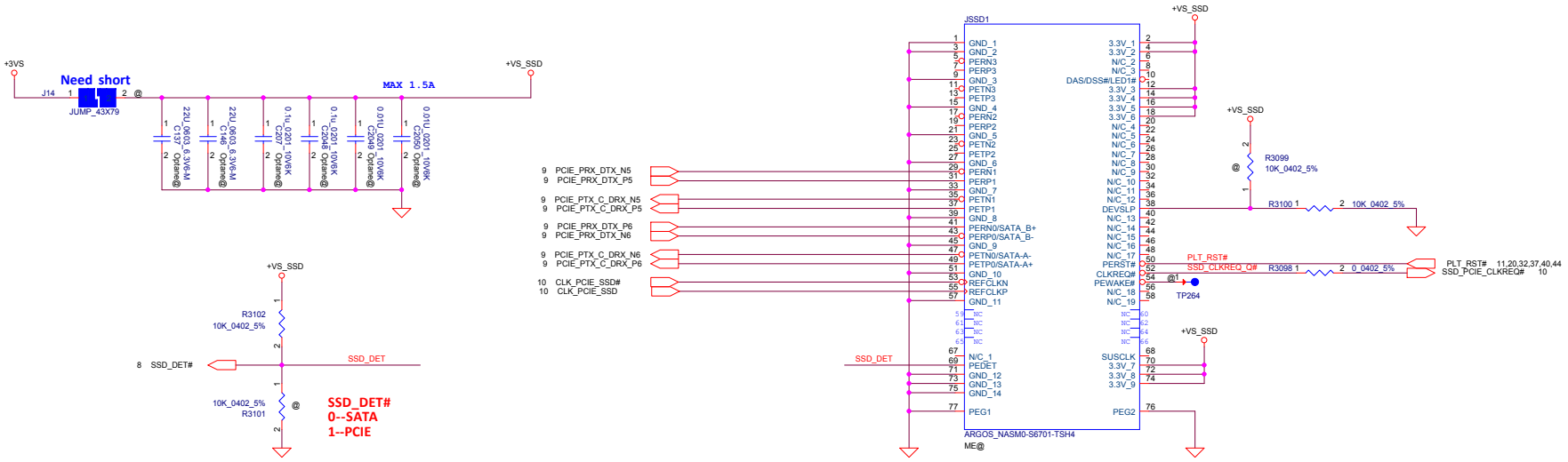
Size	Document Number	Rev
Custom	DG710	0.1

Date: Monday, July 18, 2016 Sheet 39 of 61

Mini-Express Card(WLAN/WiMAX)



Optane Memory



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	NGFF WLAN		
Size C	Document Number DG710		Rev 0.1
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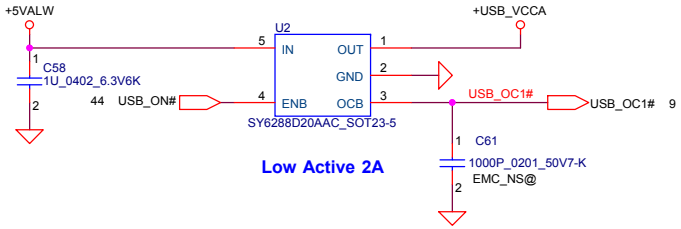
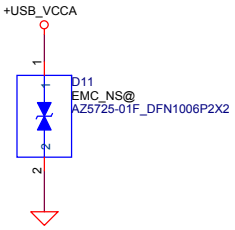
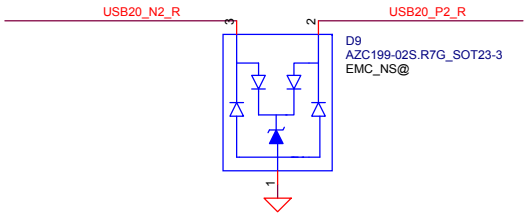
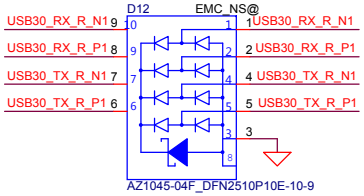
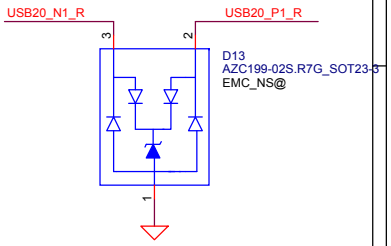
LEFT SIDE USB PORT X2



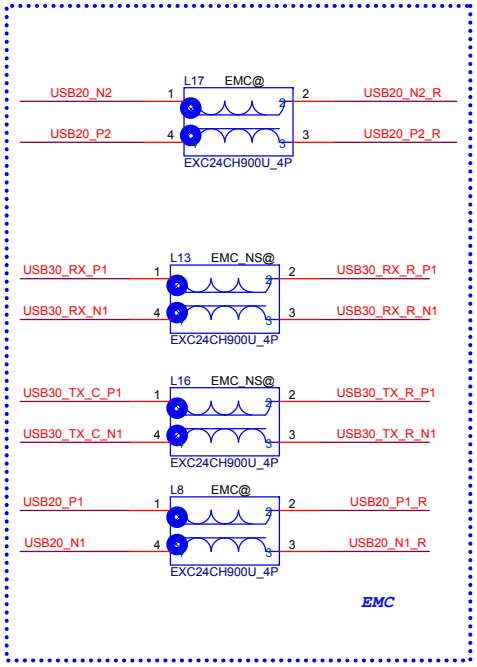


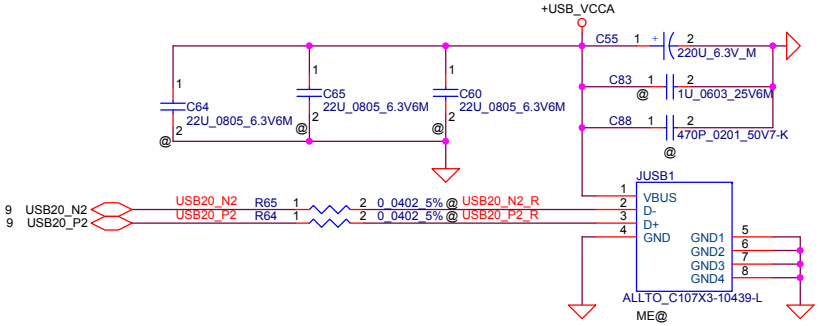


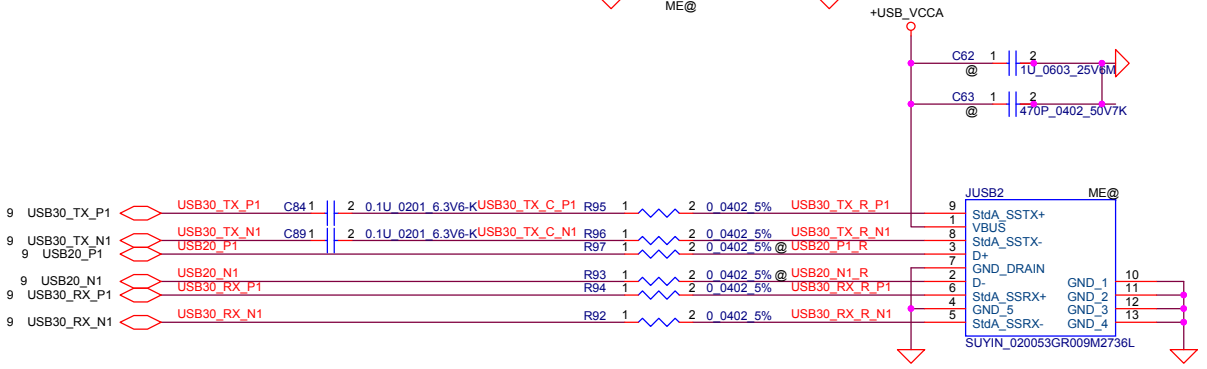




EMC solution need double check 1015







Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **USB PORT (LEFT)**

LCFC

Size	Document Number	Rev
Custom	DG710	0.1

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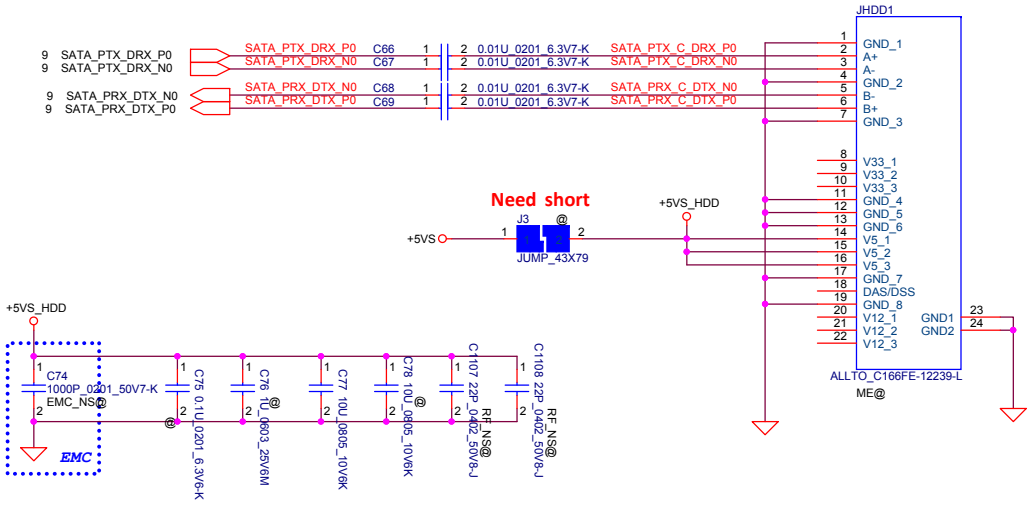
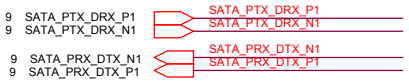
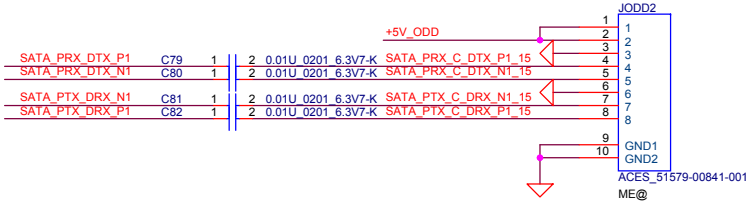
SATA HDD Conn.



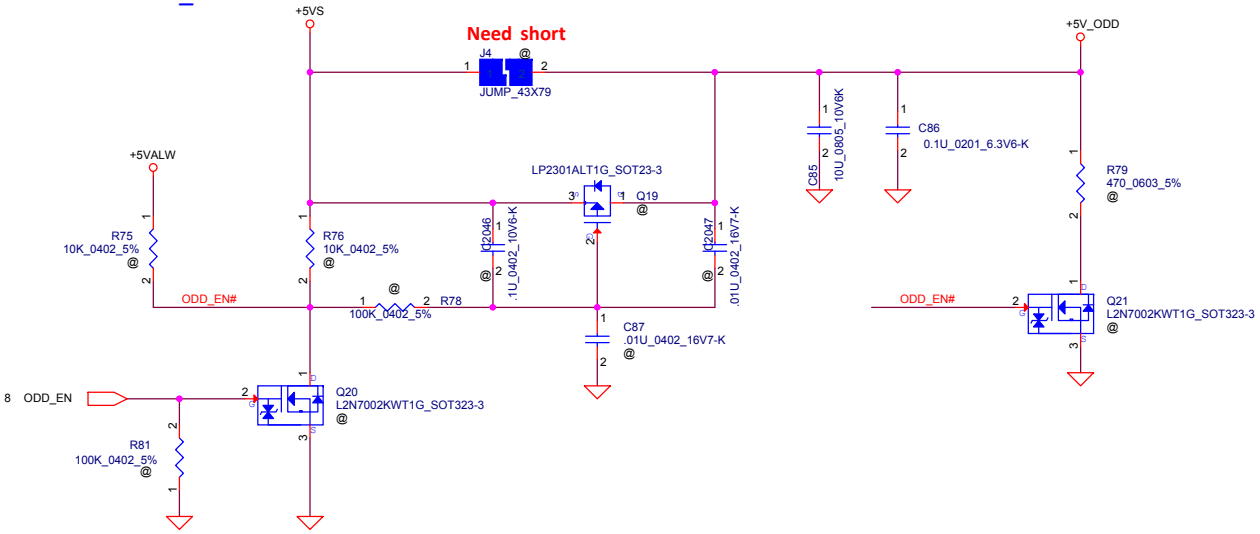
FOR 14"
SATA ODD Conn.

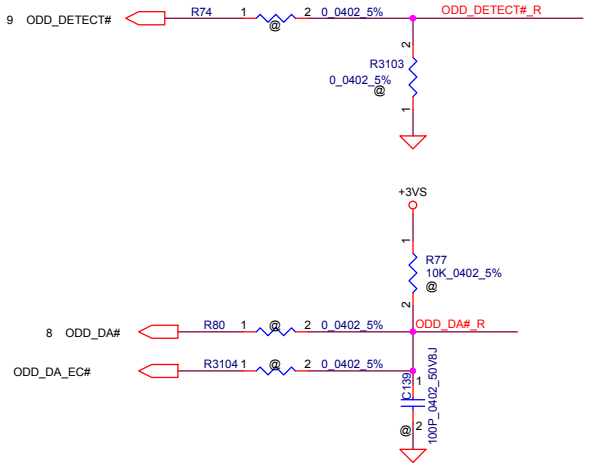


FOR 15"
SATA ODD FFC Conn



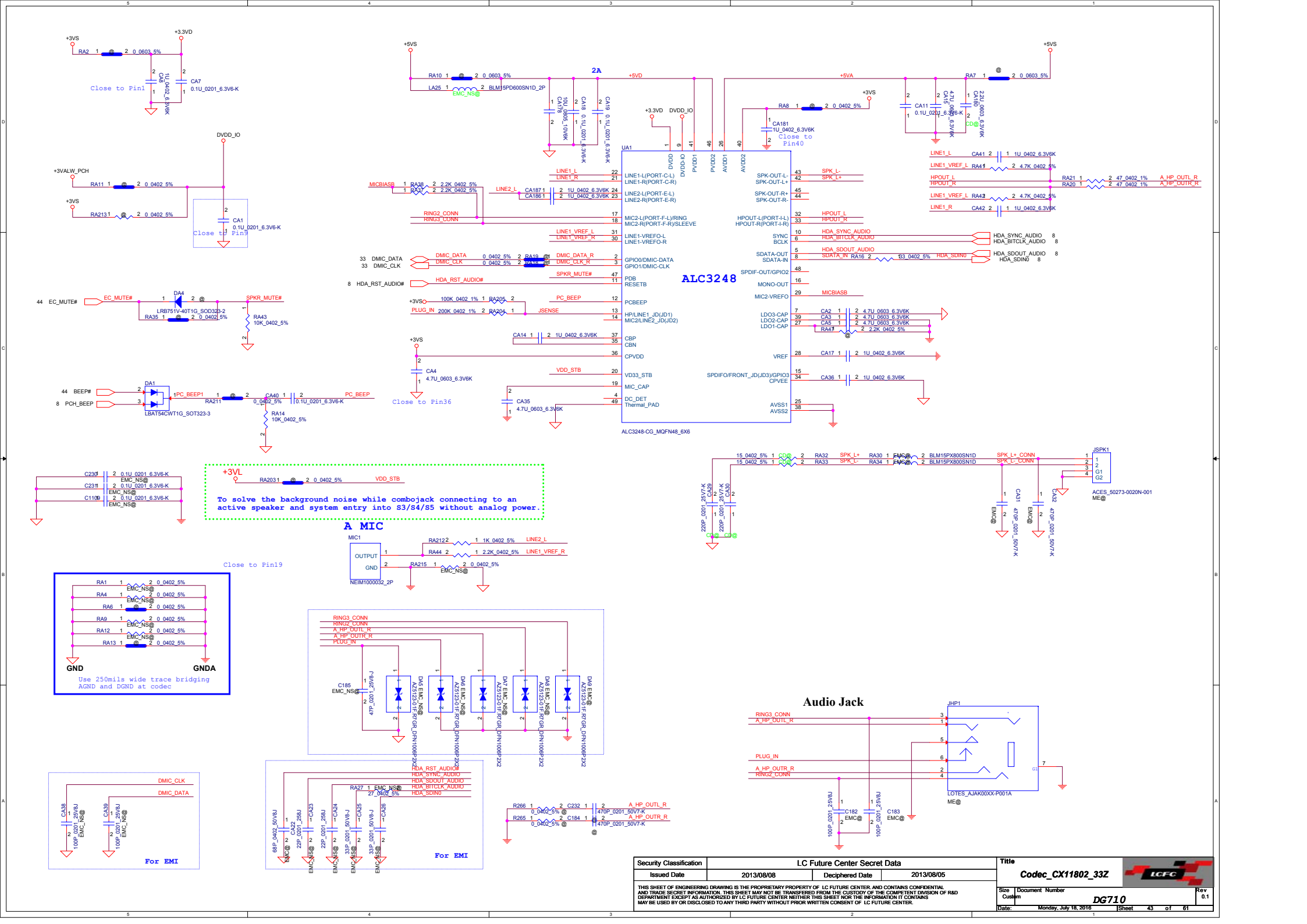
+5VS to +5V_ODD





Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title	HDD/ODD CONN		
Size	Document Number		Rev
Custom	DG710		0.1
Date:	Monday, July 18, 2016	Sheet	42 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

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Title: Codec_CX11802_33Z

Size	Document Number	Rev
Custom	DG710	0.1

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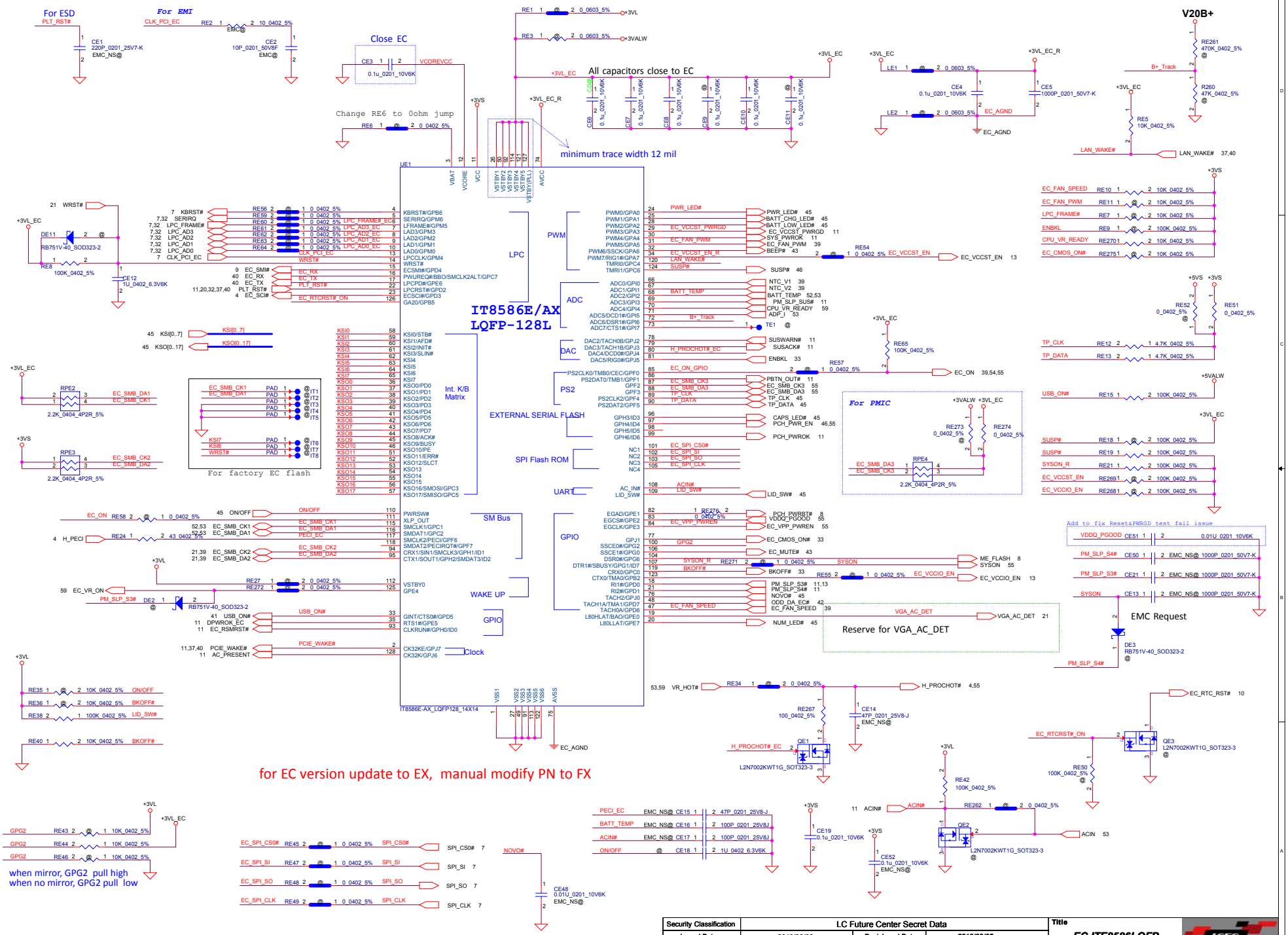
For ESD
For EMI
Close EC
All capacitors close to EC
minimum trace width 12 mil
Change RE6 to 0ohm jump
V20B+
IT8586E/AX
LQFP-128L
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
WAKE UP
GPIO
Clock
Int. K/B Matrix
For factory EC flash
For PMIC
Reserve for VGA_AC_DET
EMC Request
for EC version update to EX, manual modify PN to FX
when mirror, GPG2 pull high
when no mirror, GPG2 pull low
Add to fix Reset&PWRGD test fail issue
Security Classification
LC Future Center Secret Data
Issued Date
2013/08/08
Deciphered Date
2013/08/05
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Title
EC ITE8586LQFP
Size
Custom
Document Number
DG710
Rev
0.1
Date:
Monday, July 18, 2016
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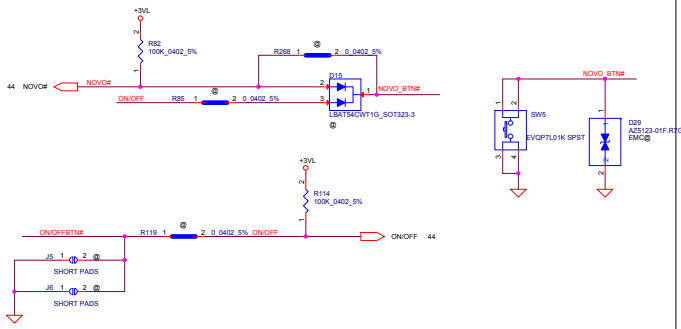
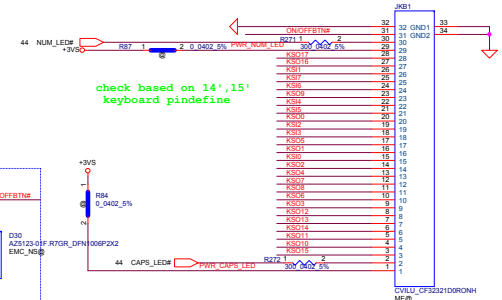
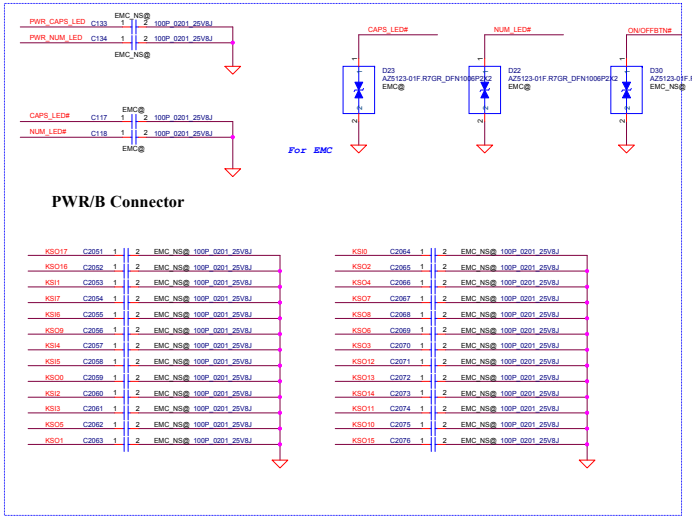
44
of
61

ON/OFF switch



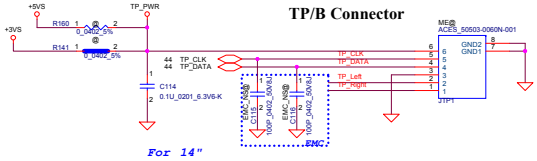
K/B Connector

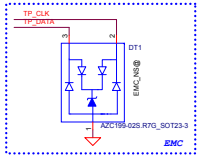


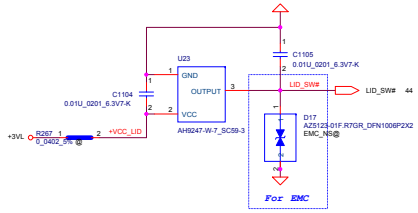


PWR/B Connector

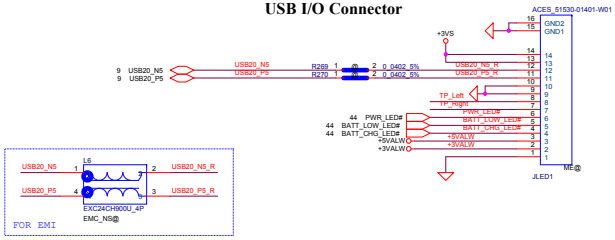
TP/B Connector







USB I/O Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: **KBD/PWR/IO/LED/TP Conn.**

Size: Custom | Document Number: **DG710** | Rev: 0.1

Date: Monday, July 18, 2016 | Sheet 45 of 61

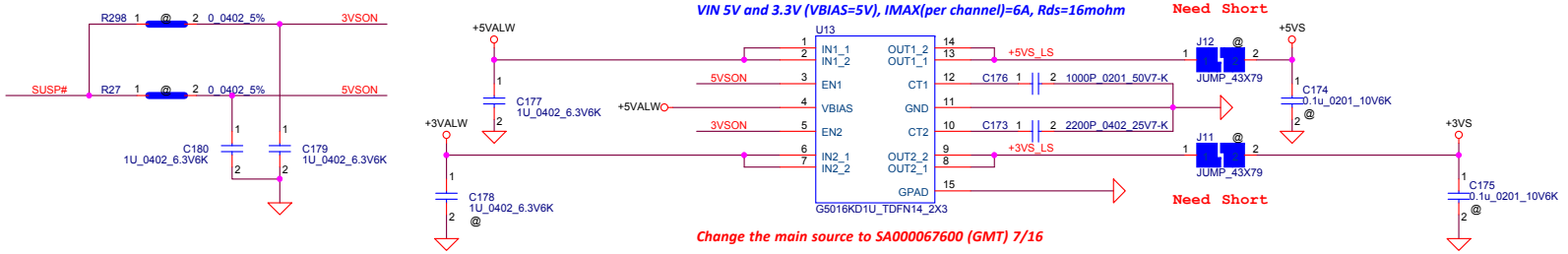
Load Switch

+5VALW To +5VS
+3VALW To +3VS

+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms

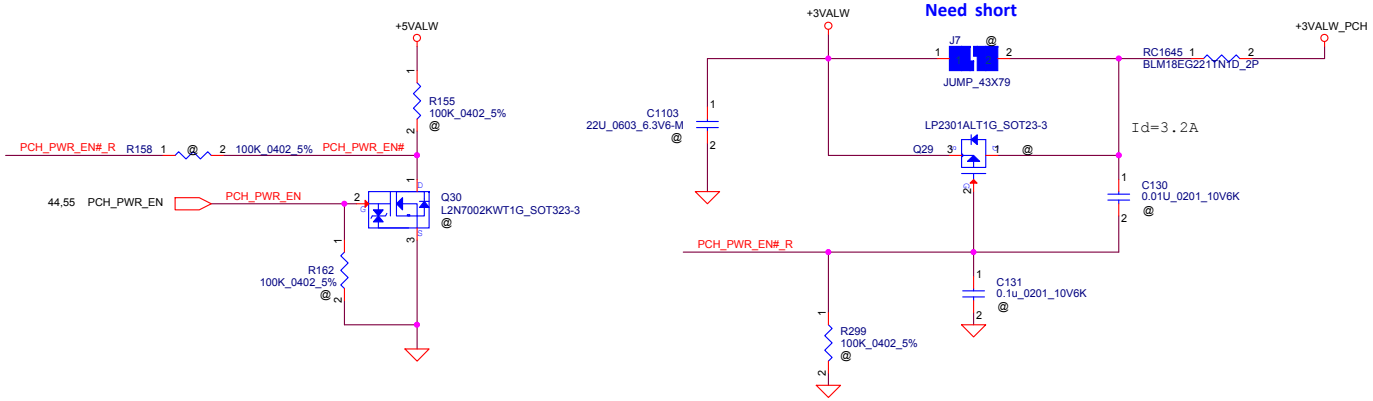
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm

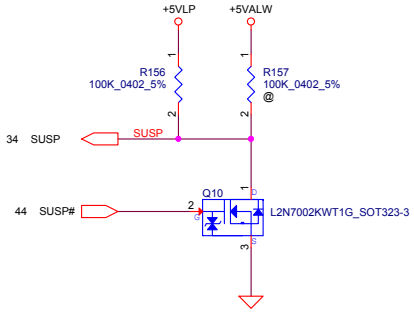
Need Short



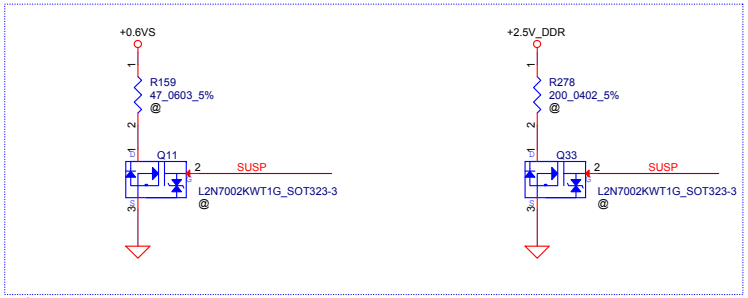
Need Short

Change the main source to SA000067600 (GMT) 7/16





For DisCharge



08/29: Need double check enable signal and the resistance

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: DC V TO VS INTERFACE

Size	Document Number	Rev
Custom	DG710	0.1

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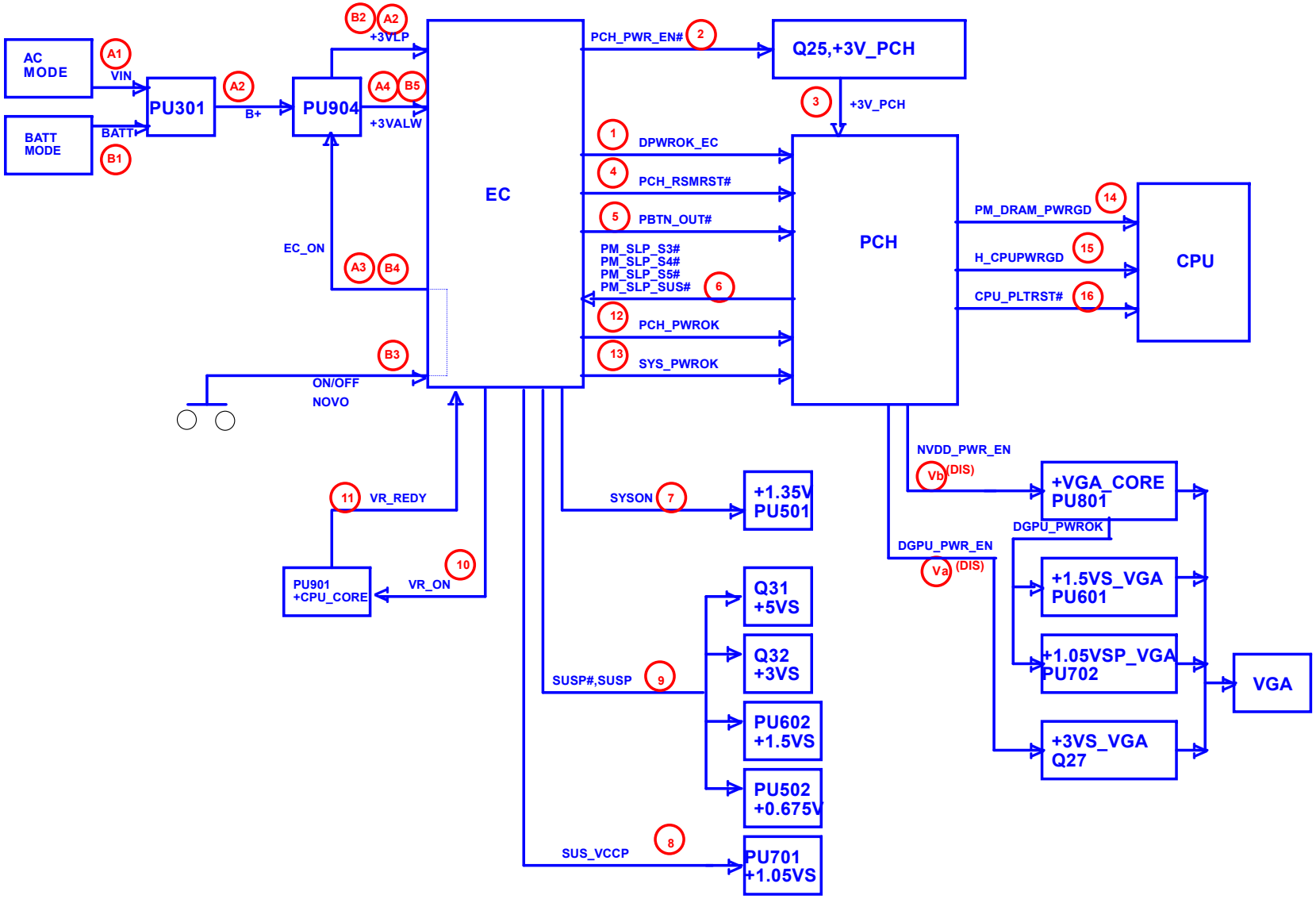

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Power sequence block**

Size	Document Number	Rev
Custom	DG710	0.1

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PCB ZZZ1
PCB PN
DAZ12G00100

HDMI ZZZ8 HDMI@
HDMI Logo
RO00000040J

CPU

UC1 7200U@ — KBL-U CPU — SA000080310
UC1 7500U@ — KBL-U CPU — SA000080410
UC1 7100U@ — KBL-U CPU — SA000080710
UC1 6006U@ — SKL-U CPU — SA000082E20

Add SKL-U CPU 6006U ------20161011

DRAM

ZZZ2 DRAM_S4G@ — Samsung — X7613712003
ZZZ3 DRAM_H4G@ — Hynix — X7613712004
ZZZ4 DRAM_M4G@ — Micron — X7613712005

2400MT/s DRAM X76 BOM

UD1 MD_S8Gb@ — K4A8G165WB-BCRC — SA00007TQ00
UD2 MD_S8Gb@ — K4A8G165WB-BCRC — SA00007TQ00
UD3 MD_S8Gb@ — K4A8G165WB-BCRC — SA00007TQ00
UD4 MD_S8Gb@ — K4A8G165WB-BCRC — SA00007TQ00
RC1634 MD_S8Gb@ — 10K_0402_5% — SD02B10028J
RC1635 MD_S8Gb@ — 10K_0402_5% — SD02B10028J
RC1639 MD_S8Gb@ — 10K_0402_5% — SD02B10028J

2400MT/s DRAM_Samsung 4G

UD1 MD_H8Gb@ — H5AN8G6NAFR-UHC — SA00007X200
UD2 MD_H8Gb@ — H5AN8G6NAFR-UHC — SA00007X200
UD3 MD_H8Gb@ — H5AN8G6NAFR-UHC — SA00007X200
UD4 MD_H8Gb@ — H5AN8G6NAFR-UHC — SA00007X200
RC1634 MD_H8Gb@ — 10K_0402_5% — SD02B10028J
RC1632 MD_H8Gb@ — 10K_0402_5% — SD02B10028J
RC1639 MD_H8Gb@ — 10K_0402_5% — SD02B10028J

2400MT/s DRAM_Hynix 4G

UD1 MD_M8Gb@ — MT40A512M16JY-083E:B — SA00007TS00
UD2 MD_M8Gb@ — MT40A512M16JY-083E:B — SA00007TS00
UD3 MD_M8Gb@ — MT40A512M16JY-083E:B — SA00007TS00
UD4 MD_M8Gb@ — MT40A512M16JY-083E:B — SA00007TS00
RC1631 MD_M8Gb@ — 10K_0402_5% — SD02B10028J
RC1635 MD_M8Gb@ — 10K_0402_5% — SD02B10028J
RC1639 MD_M8Gb@ — 10K_0402_5% — SD02B10028J

2400MT/s DRAM_Micron 4G

VRAM

ZZZ5 — Hynix H4GX4@ — X7614612001
ZZZ6 — Samsung S4GX4@ — X7613712001
ZZZ7 — MICRON M4GX4@ — X7613712002

UV5 H4G@ — H5TC4G63CFR-N0C 4Gb — SA00007DU10
UV6 H4G@ — H5TC4G63CFR-N0C 4Gb — SA00007DU10
UV7 H4G@ — H5TC4G63CFR-N0C 4Gb — SA00007DU10
UV8 H4G@ — H5TC4G63CFR-N0C 4Gb — SA00007DU10
RV70 H4G@ — 4.75K_0402_1% — SD03447518J

VRAM_Hynix_256M*16 000

UV5 M4G@ — MT41J256M16LY-091G:N — SA00007QJ00
UV6 M4G@ — MT41J256M16LY-091G:N — SA00007QJ00
UV7 M4G@ — MT41J256M16LY-091G:N — SA00007QJ00
UV8 M4G@ — MT41J256M16LY-091G:N — SA00007QJ00
RV63 M4G@ — 4.53K_0402_1% — SD03445318J
RV70 M4G@ — 2K_0402_1% — SD05420018J

VRAM_Micron_256M*16 010

UV5 S4G@ — K4W4G1646E-BC1A 4Gb — SA000063F20
UV6 S4G@ — K4W4G1646E-BC1A 4Gb — SA000063F20
UV7 S4G@ — K4W4G1646E-BC1A 4Gb — SA000063F20
UV8 S4G@ — K4W4G1646E-BC1A 4Gb — SA000063F20
RV63 S4G@ — 8.45K_0402_1% — SD00071R00
RV70 S4G@ — 2K_0402_1% — SD05420018J

VRAM_Samsung_256M*16 001

VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV63	PD resistor RV70
128Mx16	NA	100	4.53K	4.99K
	NA	111	4.75K	NC
	NA	110	3.4K	10K
256Mx16	Hynix H5TC4G63CFR-N0C 4Gb 900(1G)	000	NC	4.75K
	Micron MT41J256M16LY-091G:N 4Gb 900(1G)	010	4.53K	2K
	Samsung K4W4G1646E-BC1A 4Gb 900(1G)	001	8.45K	2K

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: Virtual symbol
Size: Custom
Document Number: DG710
Rev: 0.1
Date: Tuesday, October 11, 2016
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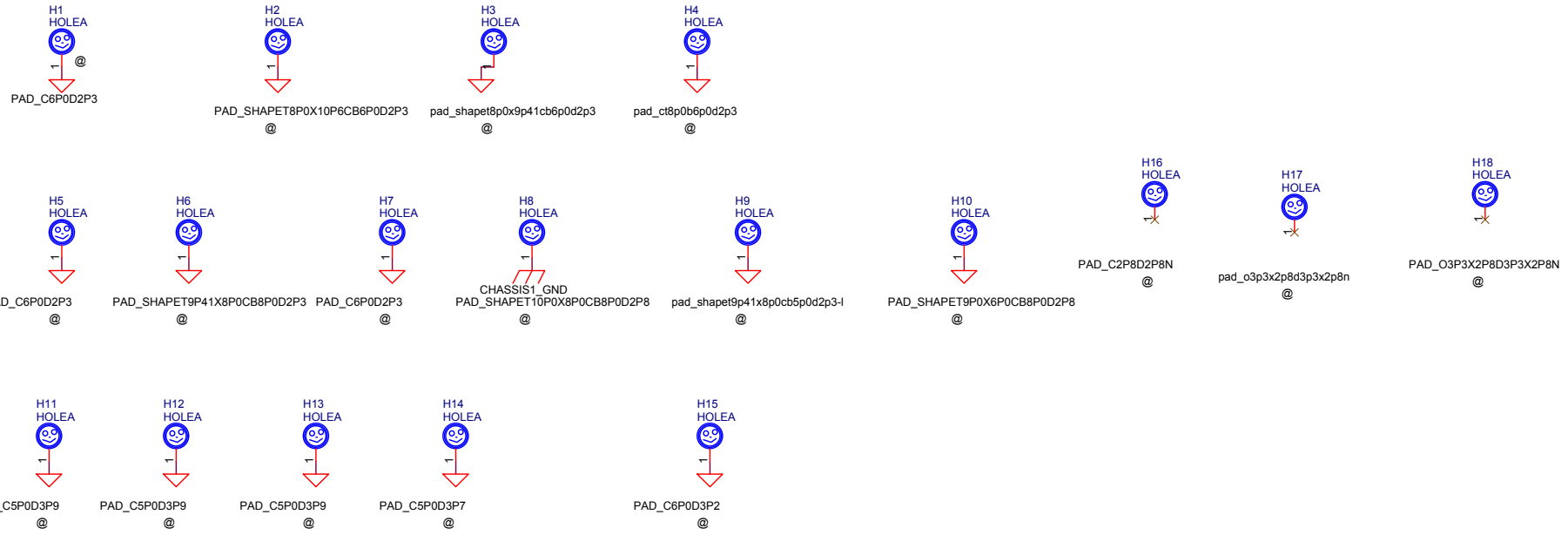
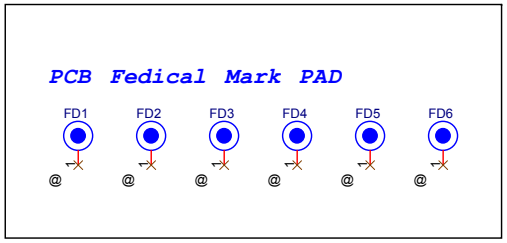
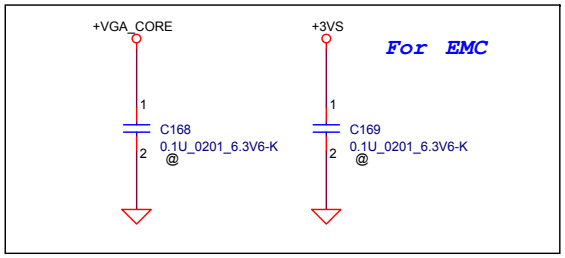




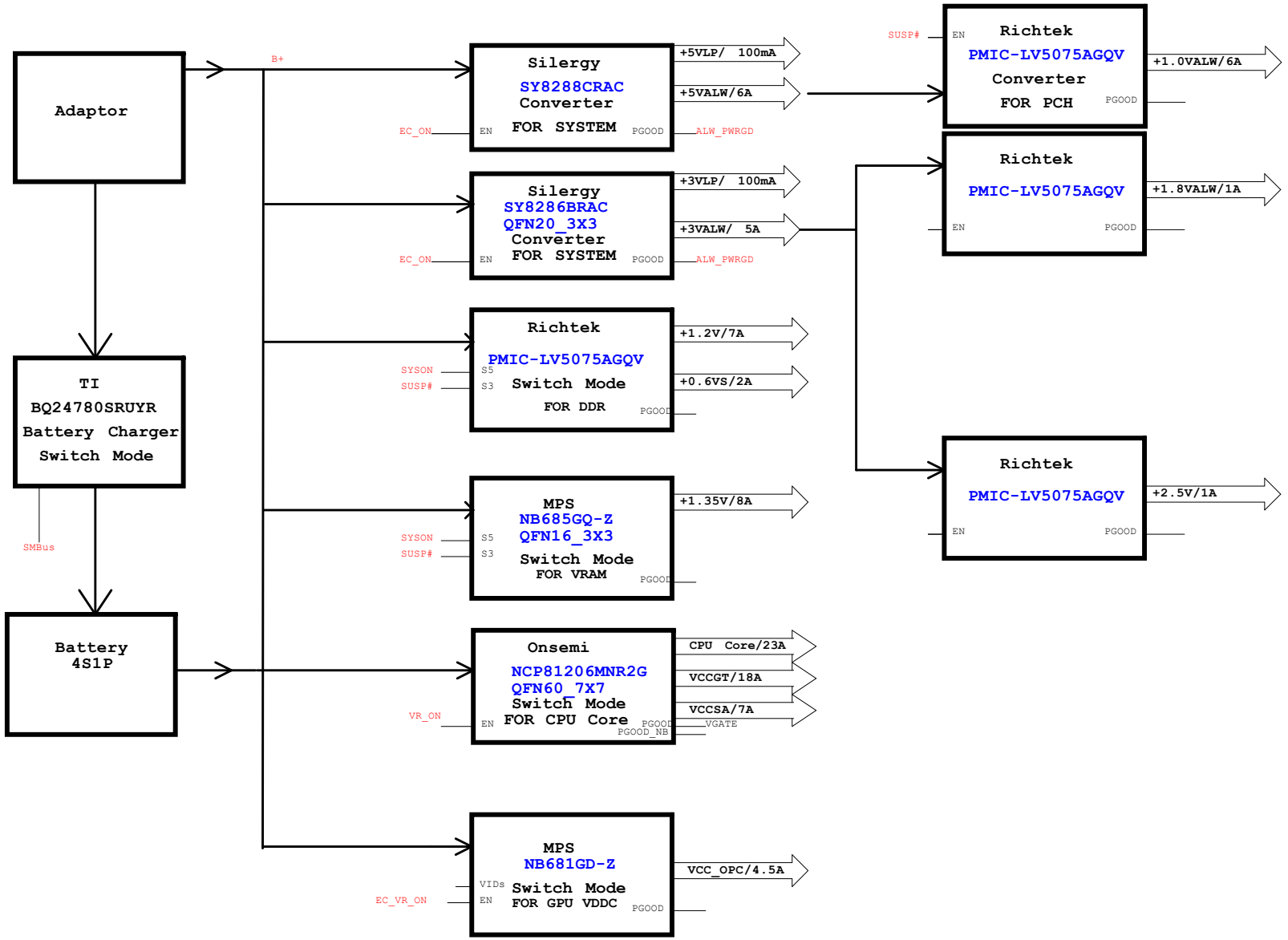


Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **Hole**

Size	Document Number	Rev
B	DG710	0.1

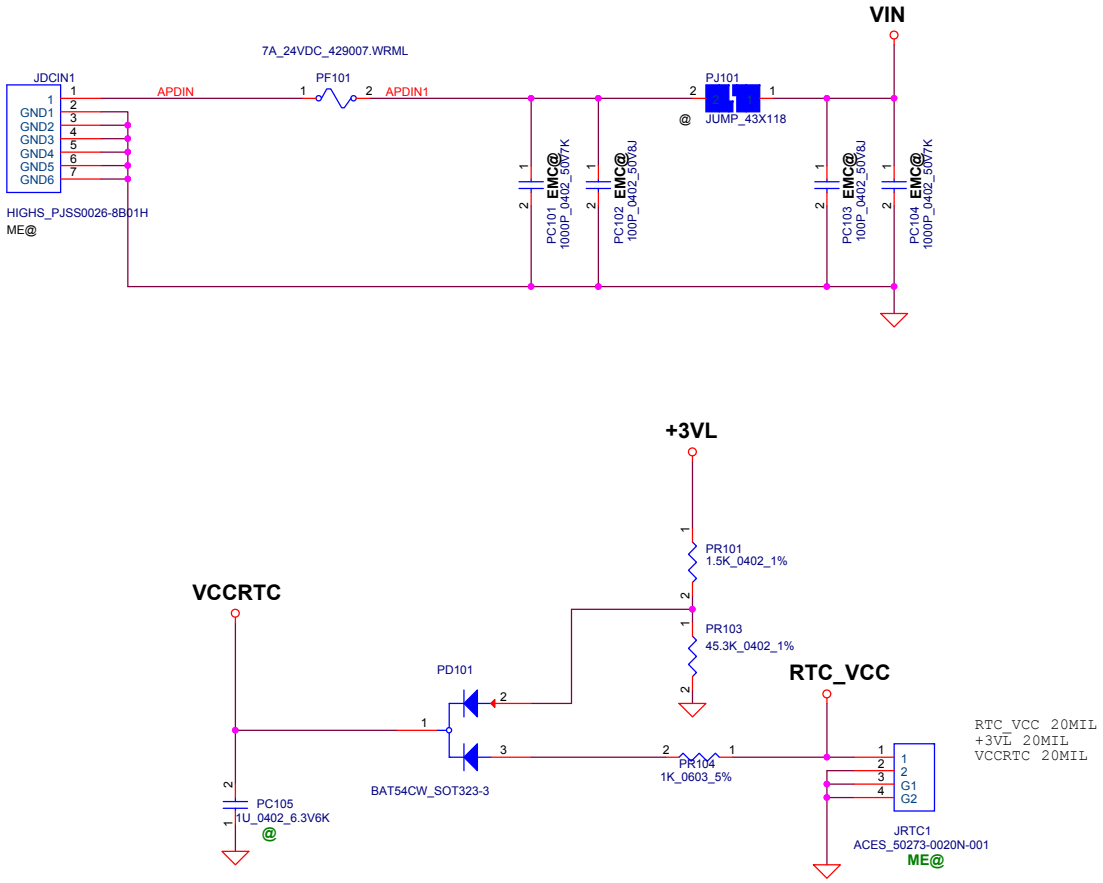
Date: Monday, July 18, 2016 Sheet 49 of 61



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-Power Diagram

Size: Custom	Document Number: DG710	Rev: 0.1
Date: Monday, July 18, 2016	Sheet 50 of 61	



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-DCIN / RTC charger

Size	Document Number	Rev
A3	DG710	0.1

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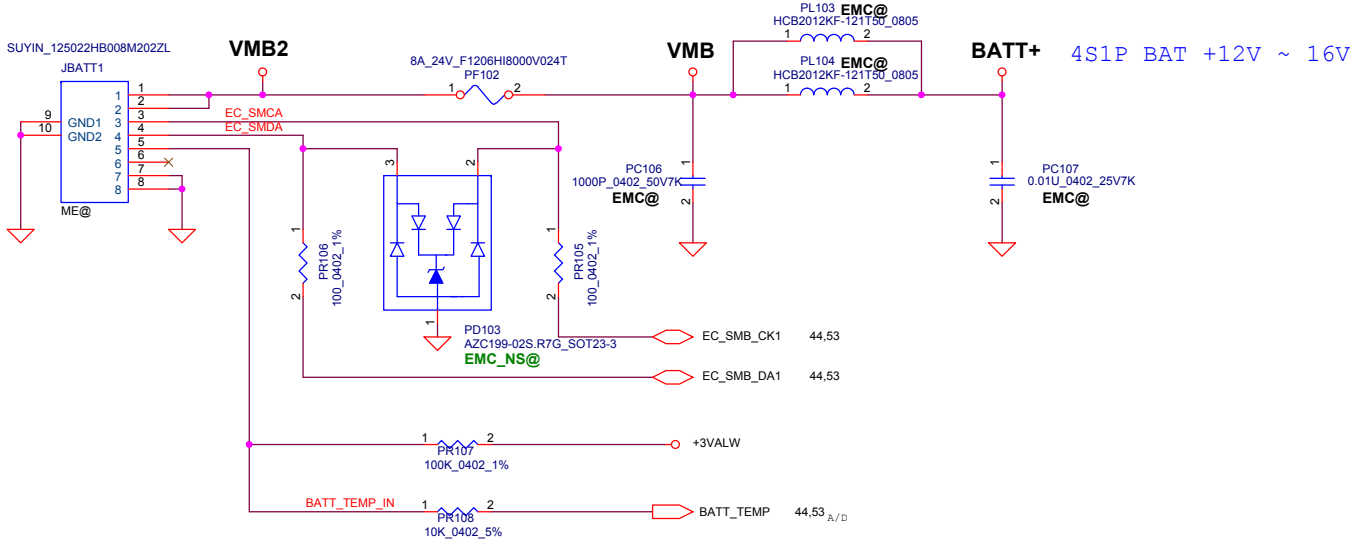

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR-BATTERY CONN/OTP

Size	Document Number	Rev
A3	DG710	0.1

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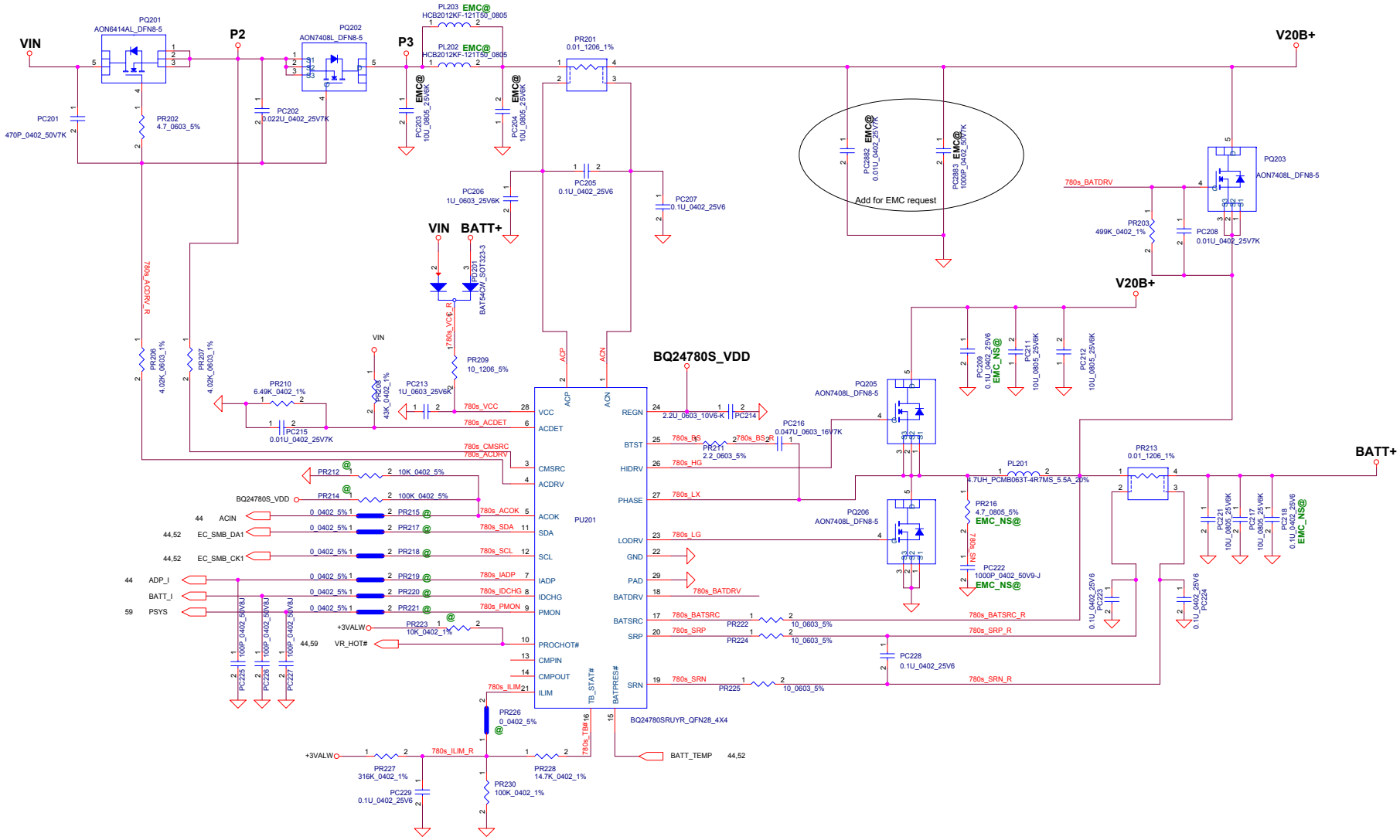

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: **PWR-CHARGER**

Size	Document Number	Rev
C	DG710	0.1

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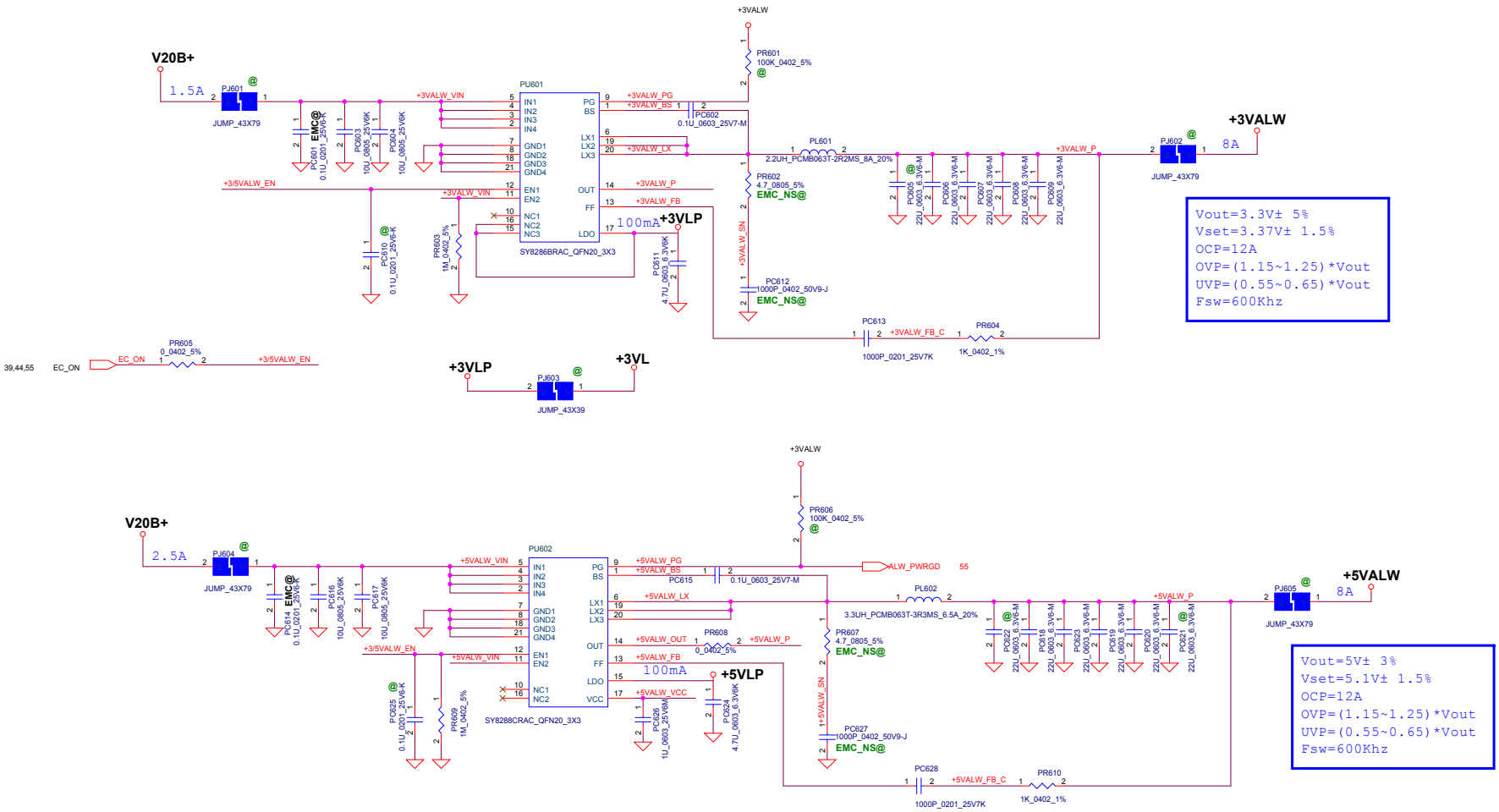

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PWR_3VALW/5VALW		
Size	Document Number		Rev
C	DG710		0.1
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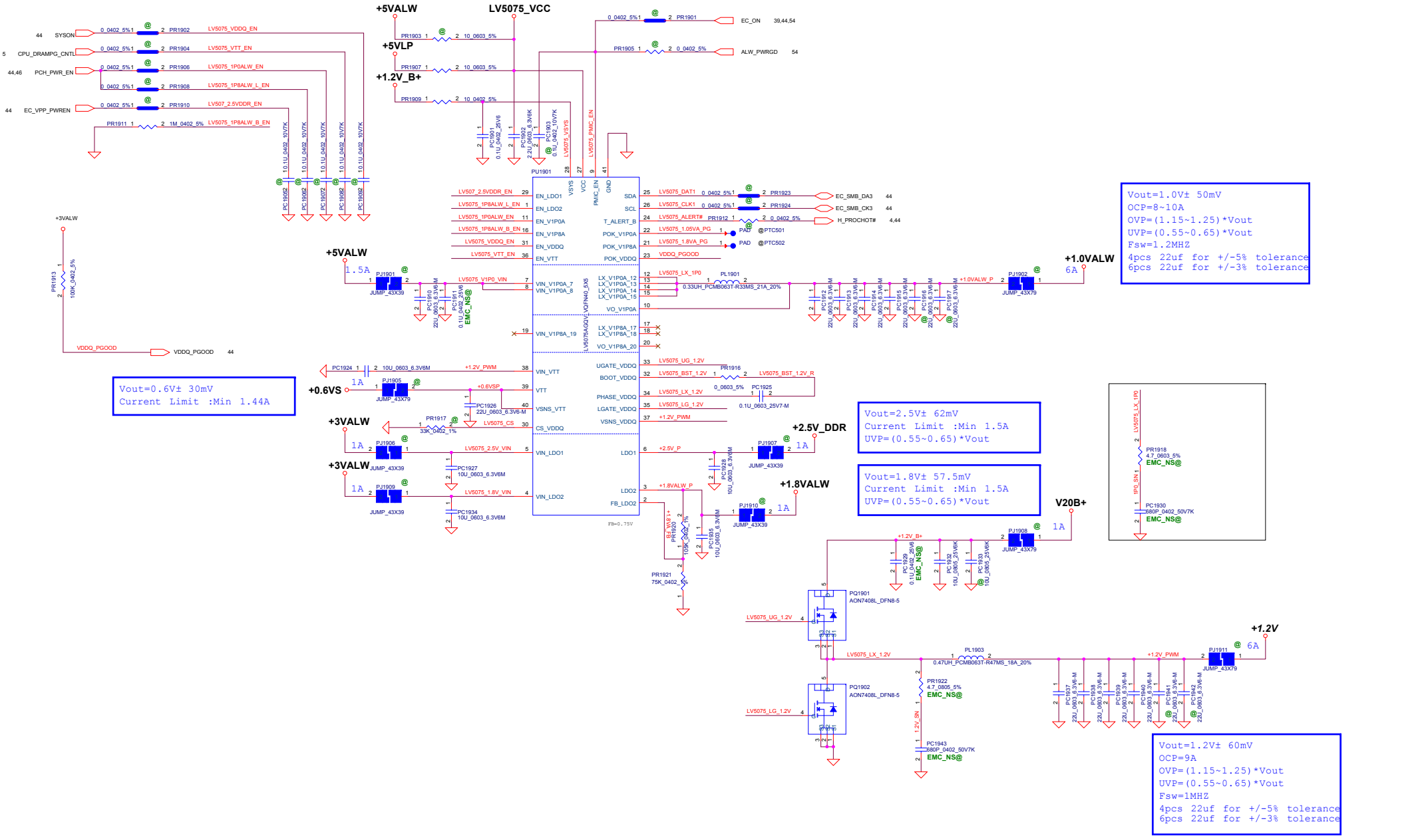

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR PMIC-DDR4/1.0ALW/1.2ALW

Size	Document Number	Rev
A2	DG710	0.1

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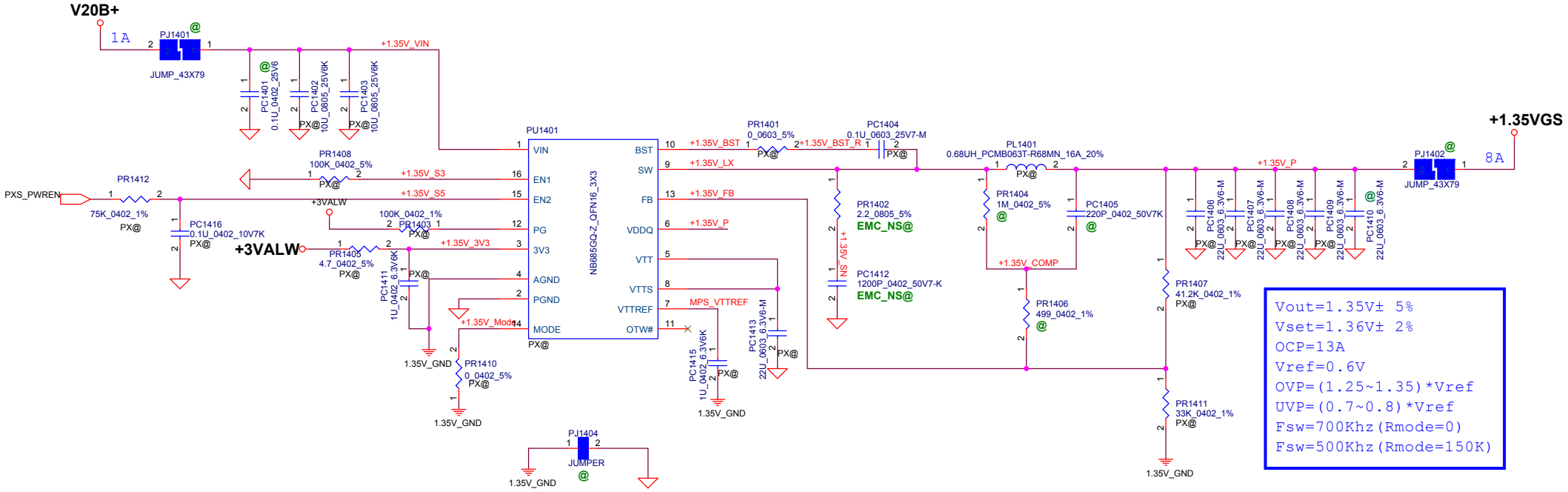

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR

Size	Document Number	Rev
A3	DG710	0.1

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Title

PWR-+VCCOPC

Size	Document Number	Rev
C	*DG710*	0.1

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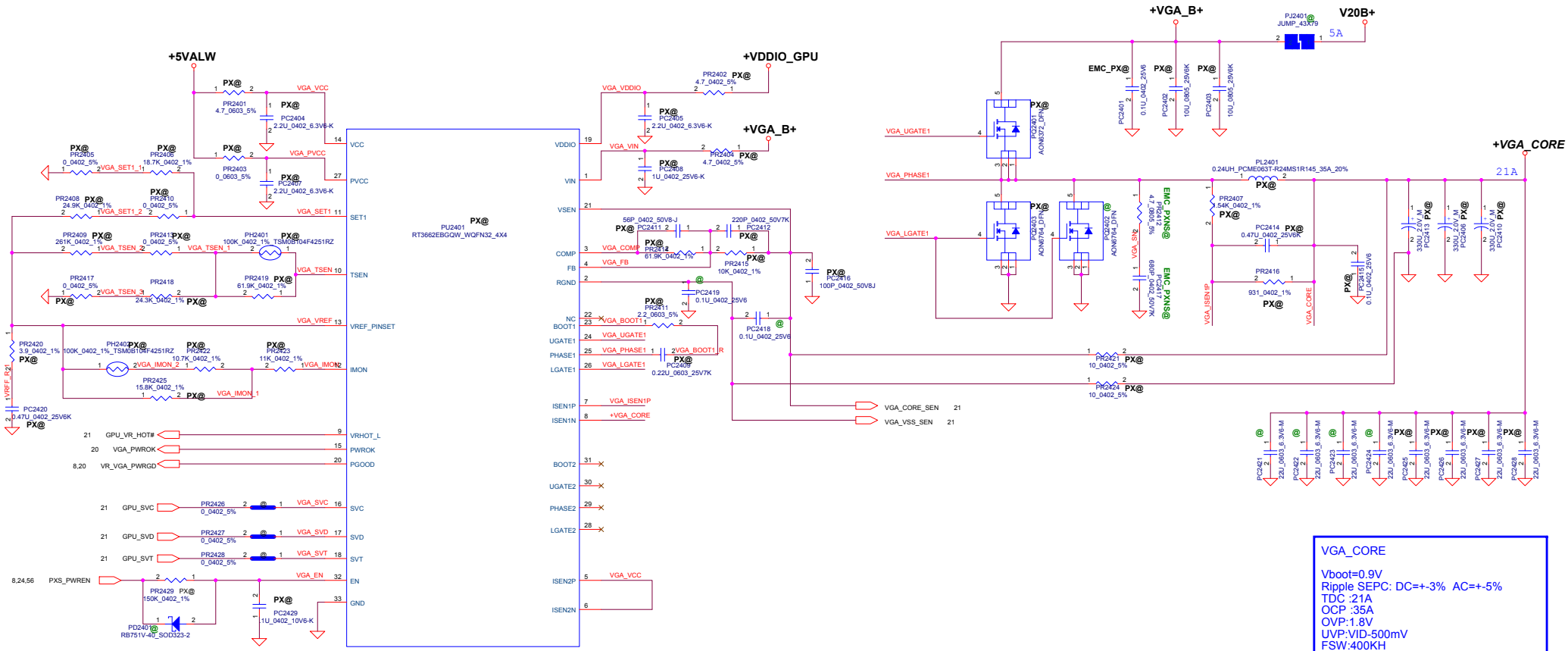

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title	PWR-VGA_CORE_AMD		
Size: Custom	Document Number: DG710		Rev: 0.1
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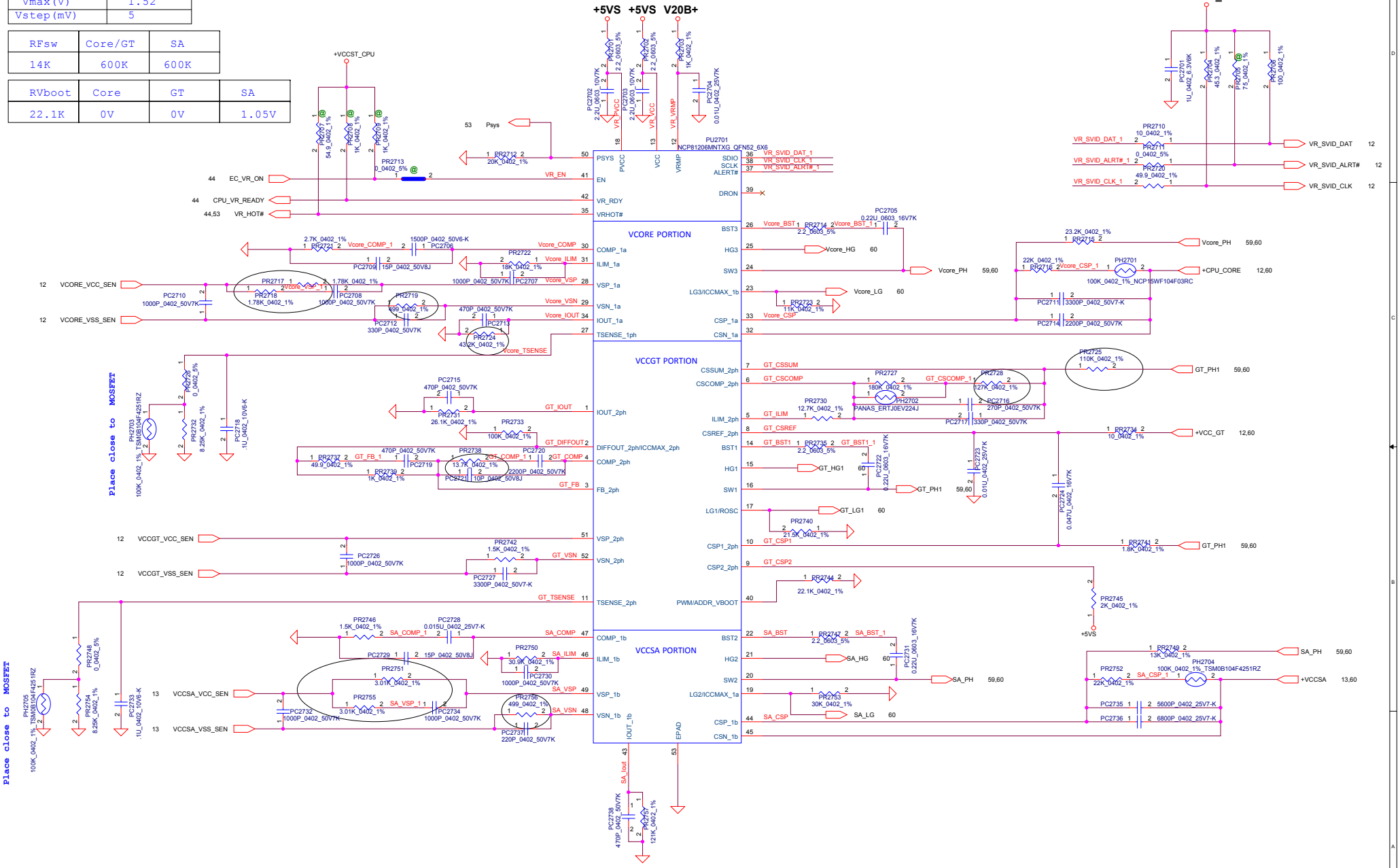
SVID Specification	
	Config
Vmin(V)	0
Vmax(V)	1.52
Vstep(mV)	5

RFsw	Core/GT	SA
14K	600K	600K

RVboot	Core	GT	SA
22.1K	0V	0V	1.05V



Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR_CPU_CORE1

Size	Document Number	Rev
C	DG710	0.1

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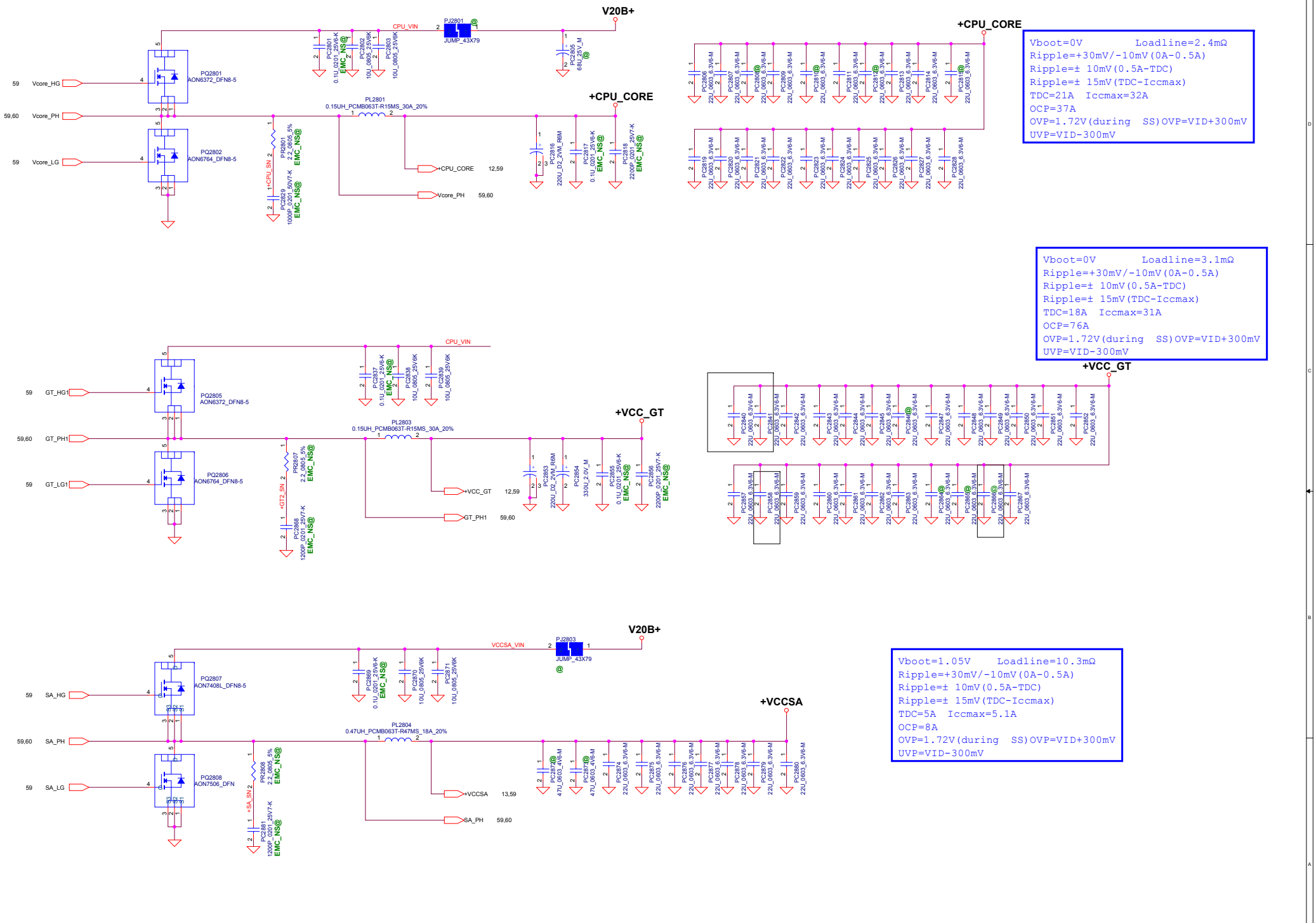

Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title: PWR_CPU_CORE2

Size	Document Number	Rev
C	DG710	0.1

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Security Classification	LC Future Center Secret Data		
Issued Date	2015/08/20	Deciphered Date	2016/08/20

Title

PWR-+VCCOPC

Size	Document Number	Rev
C	*DG710*	0.1

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