LCFC Confidential

ADL-P LCFC Griffin Schematics Document

Griffin / Roc M/B SCHEMATICS

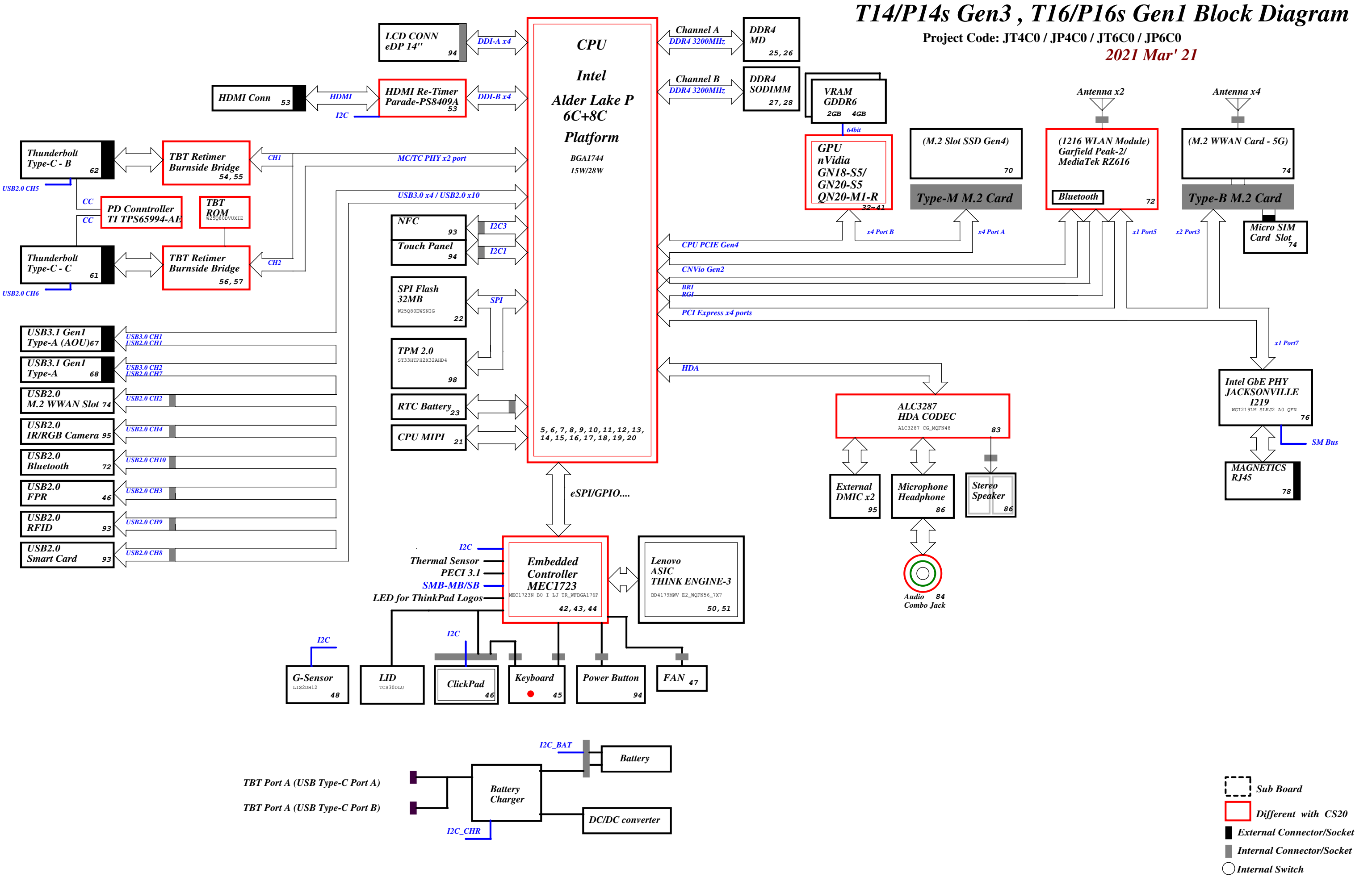
Intel AlderLake Processy with DDR4

REV:0.01

T14/P14s Gen3 , T16/P16s Gen1 Block Diagram

Project Code: JT4C0 / JP4C0 / JT6C0 / JP6C0

2021 Mar' 21



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EC HISTORY

627205_ADL P_PDG_Rev0p7

10.11.4 Power States

Table 760. System with M3 State Supported

Rails	SKUs	S0/M0[3]	C10[2]	S0ix/M-off[4]	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3[1]
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_3P3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VCCPRIM_3P3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_0P82	S	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P05	S	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
V1.8M[5]	All	ON	ON	OFF	ON[10]	OFF	ON[10]	OFF	OFF	No Power
VDD2	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VPP	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCC1P05_PROC	All	ON	ON	ON	ON [12, 13]	ON [12, 13]	ON [12, 13]	ON [12, 13]	OFF	No Power
VCCIN_AUX	All	ON	ON[14]/OFF[2]	ON[14]/OFF[2]	ON[14]/OFF	ON[14]/OFF	ON[14]/OFF	ON[14]/OFF	OFF	No Power
VCC1P8_PROC	All	ON	ON[15]/OFF[2]	ON[15]/OFF[2]	ON[15]/OFF	ON[15]/OFF	ON[15]/OFF	ON[15]/OFF	OFF	No Power
VCC_MIPILP[19]	P	ON	OFF[18]	OFF[18]	OFF	OFF	OFF	OFF	OFF	No Power
VCCCORE	All	ON	OFF[17]	OFF	OFF	OFF	OFF	OFF	OFF	No Power
VCCGT	All	ON	OFF[17]	OFF	OFF	OFF	OFF	OFF	OFF	No Power

continued...

Notes:
1. The state of the system without RTC well powered can also be considered G3.
2. VCCIN_AUX may turn off if the VIDs are low.
3. S0/M0 state includes all Package C-states from C0-C10
4. Assume SLP_S0# and CPU_C10_GATE# have asserted from the PCH
5. V3.3M and V1.8M are platform rails used by external devices which ME operates during Sx/M3 states. These rails are not used directly by the CPU/PCH, and are not present on non-M3 supported systems
6. NA
7. NA
8. NA
9. NA
10. For no M3 support on external devices, V3.3M/V1.8M will be OFF in Sx/M3
11. NA
12. If VCCIN_AUX is ON, VCC1P05_PROC needs to be ON
13. VCC1P05_PROC can be turned ON in S5 state through VCCST_OVERRIDE
14. VCCIN_AUX may be ON in these power states if required by the SOC.
15. For systems that use FIVR based PCH parts the processor requires that any time AUX is ON at a non-zero voltage that VCC1P8_PROC be powered as well. This means that the VCC1P8_PROC enable must use the AUX VIDs as part of the enable logic since AUX can be ON in Sx states with FIVR based PCH parts
16. NA
17. This supply is expected to be OFF during states where CPU_C10_GATE# is asserted. It may be left on during this condition but the Processor will not achieve it's lowest power consumption. Specific power up latencies apply when exiting this state.
18. If MIPI is not used, this power rail will be powered by VCC1P05_PROC and stays ON in S0ix. If MIPI is used with a LDO to make 1.24V its enable should be controlled by CPU_C10_GATE# to allow shutdown in S0ix.
19. VCC_MIPILP must ramp with or after VCC1P05_PROC. Recommend before IMVP for ease of implementation. While exiting from S0ix, must be ramped by the time STG timer expires in PCH (65us). No specific order required for discharge requirement.

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Griffin/Roc EVT Planar Logic Schematics

001.Project Name
002.Block diagram
003.EC list Or Component Tolence
004.Title Page
005.CPU(01/16):DDI/Type-C
006.CPU(02/16):DDR(1/2)
007.CPU(03/16):DDR(2/2)
008.CPU(04/16):MISC/JTAG
009.CPU(05/16):SPI/ESPI/SMB/CL
010.CPU(06/16):I2C/ISH/UART/GPIO
011.CPU(07/16):AUDIO
012.CPU(08/16):PCIE/USB/SATA
013.CPU(09/16):CSI-2/CNVI
014.CPU(10/16):CLOCK SIGNALS
015.CPU(11/16):SYSTEM PM
016.CPU(12/16):CPU Power (1/2)
017.CPU(13/16):CPU Power (2/2)
018.CPU(14/16):PCH Power
019.CPU(15/16):GND
020.CPU(16/16):CFG/RESERVED
021.MIPI60 DEBUG PORT
022.SPI FIASH
023.RTC BATTERY
024.BLANK
025.DDR4 SUB CHANNEL-A MD_1
026.DDR4 SUB CHANNEL-A MD_2
027.DDR4 SUB CHANNEL-B SODIMM_1
028.DDR4 SUB CHANNEL-B SODIMM_2
029.(BLANK)
030.(BLANK)
031.GN18/20-S5 OVR-M
032.GN18/20-S5(1/7) PEG I/F
033.GN18/20-S5(2/7) VRAM I/F
034.GN18/20-S5(3/7) DIGITA / XTAL
035.GN18/20-S5(4/7) STRAP / GPIO
036.GN18/20-S5(5/7) POWER
037.GN18/20-S5(6/7) POWER 2
038.GN18/20-S5(7/7) GND
039.GN18/20-S5 : GDDR6 VRAM CH_A
040.GN18/20-S5 : GDDR6 VRAM CH_A CAP
041.BLANK
042.MEC1723 (1/3)
043.MEC1723 (2/3)
044.MEC1723 (3/3)
045.Keyboard / Track point
046.TOUCH PAD/FPR POINT/PWR BTN
047.FAN
048.APS G-SENSOR
049.HPD G-SENSOR
050.Think Engine (1/2)
051.Think Engine (2/2)
052.BLANK
053.HDMI Retimer & Connector
054.Thunderbolt Retimer B (1/2)
055.Thunderbolt Retimer B(2/2)
056.Thunderbolt Retimer C(1/2)
057.Thunderbolt Retimer C(2/2)
058.(BLANK)
059.USB PD Controller
060.(BLANK)
061.Thunderbolt C Connector PORT C
062.Thunderbolt C Connector PORT B
063.(BLANK)
064.(BLANK)
065.TYPEC_DCIN
066.(BLANK)
067.USB TYPE-A CONNECTOR (AOU)
068.USB TYPE-A CONNECTOR
069.(BLANK)
070.M.2 Socket 3 Module I/F
071.(BLANK)
072.M.2 Type 1216 Module
073.(BLANK)
074.M.2 Socket 2 Module I/F
075.(BLANK)
076.GBE Jacksonville
077.(BLANK)
078.RJ45 Connector
079.(BLANK)
080.(BLANK)
081.(BLANK)
082.(BLANK)
083.Audio Codec (ALC3286)
084.Audio Connector
085.Audio Jack
086.Audio Speaker
087.Audio Beep
088.ENERGY ESTIMATION ENGINE
089.(BLANK)
090.(BLANK)
091.(BLANK)
092.(BLANK)
093.Smart Card Reader / NFC
094.LCD / Touch interface
095.LID / IR Camera / MIC
096.(BLANK)
097.(BLANK)
098.Discrete TPM 2.0
099.(BLANL)
100.(BLANK)
101.BATTERY INPUT
102.BATTERY CHARGER (BQ25710)
103.DC/DC VCC5M (NB690)
104.DC/DC VCC5M_PD (NB693GQ)
105.DC/DC VCC3M (TPS51393P)
106.DC/DC VCC1R065A/(NB705)
107.DC/DC VCC1R8_SUS (TPS56637R)
108.DC/DC ADL(MP2964
109.DC/DC_VCCCPUCORE(MP86971
110.DC/DC VCCCPUCORE_DE_CAP
111.DC/DC VCCGT(MP86943
112.DC/DC VCCPCHCORE(MP2961
113.DC/DC VCCPCHCORE DE_CAP
114.BLANK
115.DC/DC VCCGFXCORE_D (NCP8127)
116.DC/DC VCC1R2VIDEO(MP2941A)
117.DC/DC VCC1R8VIDEO (BD9B304)
118.Load SW VIDEO
119.DC/DC VCC1R0VIDEO(BD9B304)
120.LOAD SW VCC3_SUS
121.LOAD SW VCCST & VCCSTG
122.LOAD SW LAN
123.LOAD SW B
124.LOAD SW TOUCH PANEL
125.(BLANK)
126.(BLANK)
127.(BLANK)
128.System Power Tree
129.System Power Sequence
130.(BLANK)

TABLE: Chip Part Dimension

Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20	0402	01005
0.60 x 0.30	0603	0201
1.00 x 0.50	1005	0402
1.60 x 0.80	1608	0603
2.00 x 1.25	2125	0805
2.00 x 1.60	2016	0806
2.50 x 2.00	2520	1008
3.20 x 1.60	3216	1206
3.20 x 2.50	3225	1210
4.50 x 1.60	4516	1806
4.50 x 2.50	4525	1810
4.50 x 3.20	4532	1812
5.00 x 2.50	5025	2010
6.40 x 3.20	6432	2512

LOGIC

TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC -55 to 125degC	+/-30ppm/degC +/-30ppm/degC	NPO C0G
-55 to 125degC -55 to 105degC -55 to 85degC	+/-15% +/-22% +/-15%	X7R X6S X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.25pF +/-0.5pF	C D
+/-5% +/-10% +/-20% +80/-20%	J K M Z

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TABLE : Functional Strap

GPP_E19/DDP1_CTRLDATA/TBT_LSX0_RXD (DDP1 I2C / TBT_LSX0 Pin VCC Configuration)
GPP_E21/DDP2_CTRLDATA/TBT_LSX1_RXD (DDP2 I2C / TBT_LSX1 Pin VCC Configuration)
GPP_D10/DDP3_CTRLDATA/TBT_LSX2_RXD (DDP3 I2C / TBT_LSX2 Pin VCC Configuration)
GPP_D12/DDP4_CTRLDATA/TBT_LSX3_RXD (DDP4 I2C / TBT_LSX3 Pin VCC Configuration)

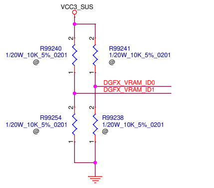
HIGH	3.3V for HDMI Display I2C (External Pull-Up Resistor Required)
LOW	1.8V for Thunderbolt LSX (Default)

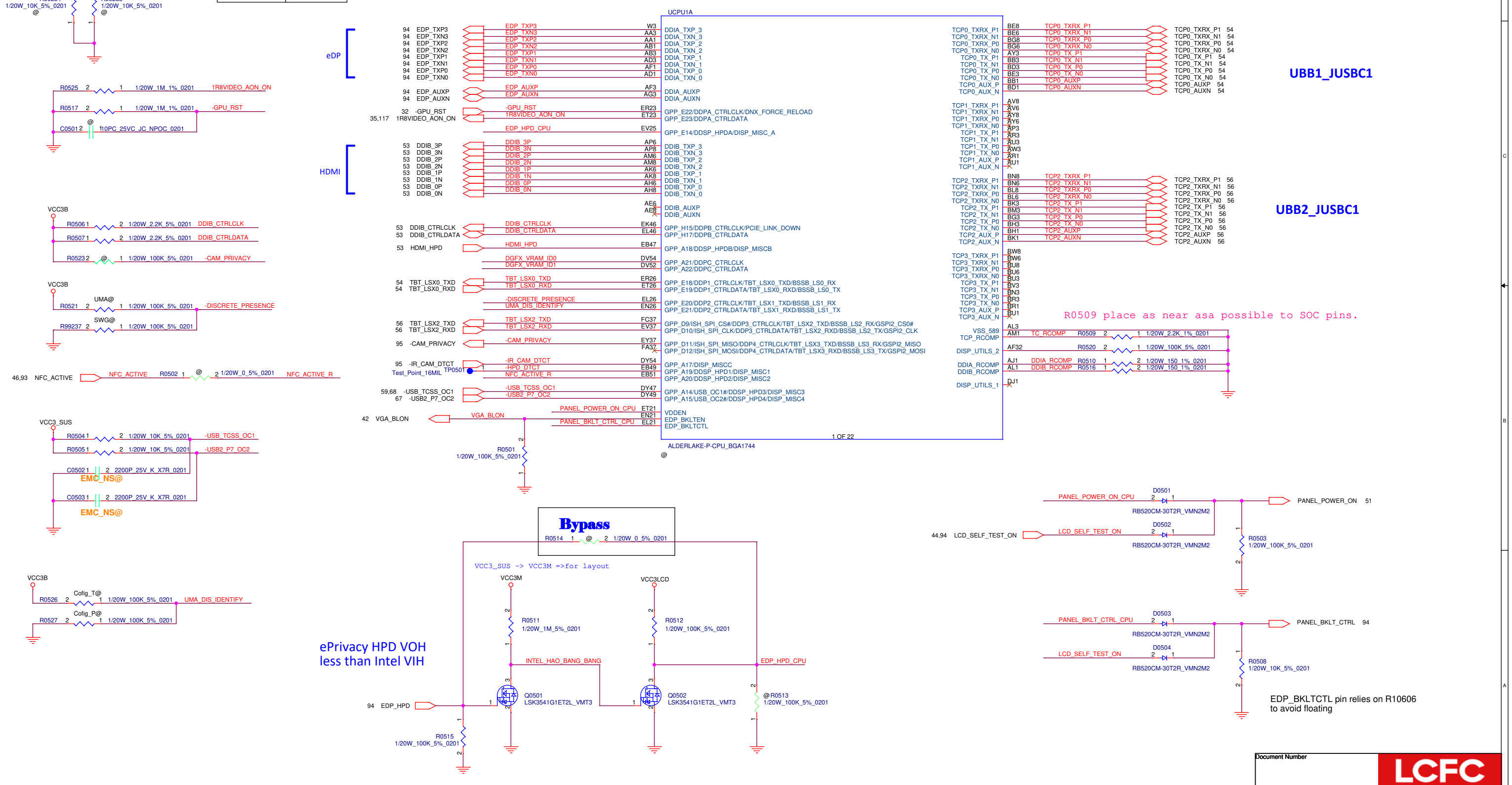
TABLE : DGFX_config

DFX_VRAM_ID[1..0]	
00B	GN18
01B	NA
10B	QN20
11B	UMA

TABLE : -DISCRETE_PRESENCE

Model	Part
SWG	R99237
UMA	R0521





Document Number	
Size: Custom	Title: 005_CPU(1/16): DDI/TYPE-C
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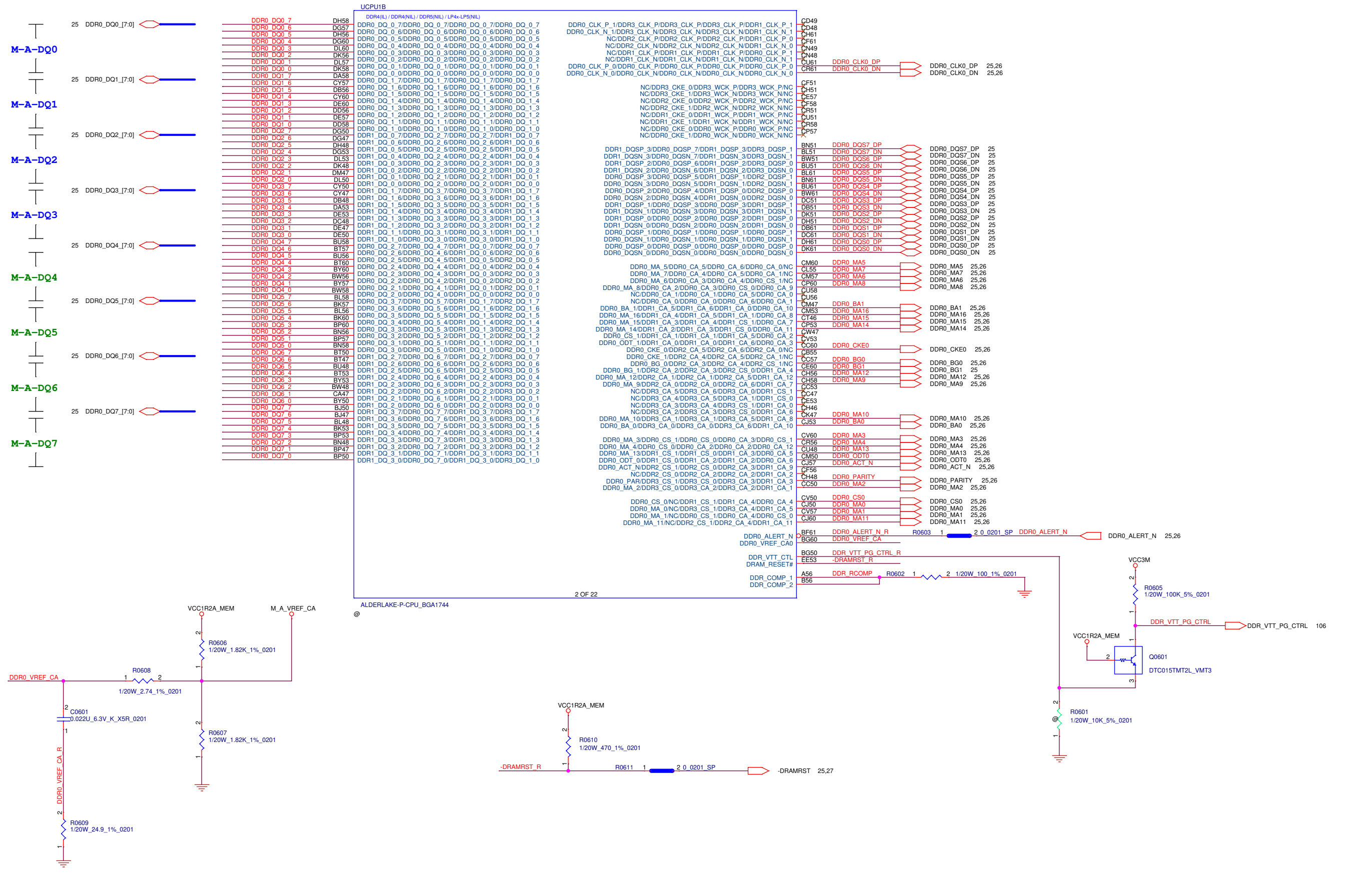

Document Number

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Size	Title	Rev
Custom	006_CPU(2/16): DDR (1/2)	0.01

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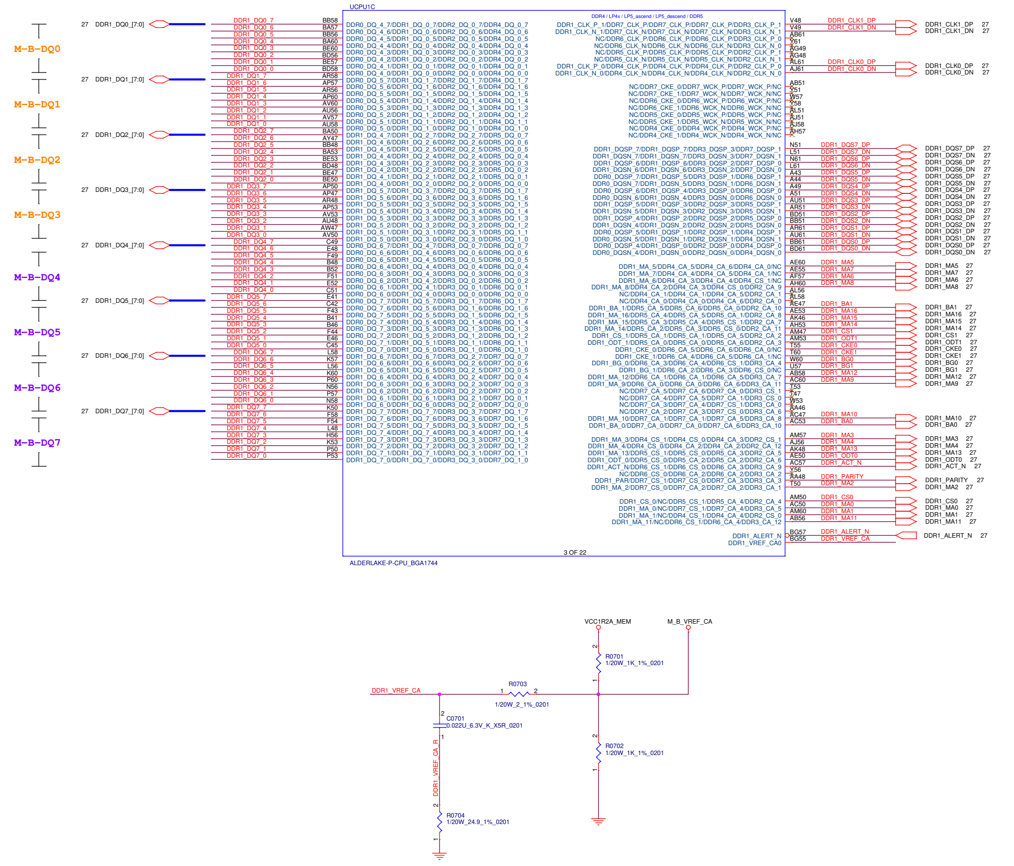

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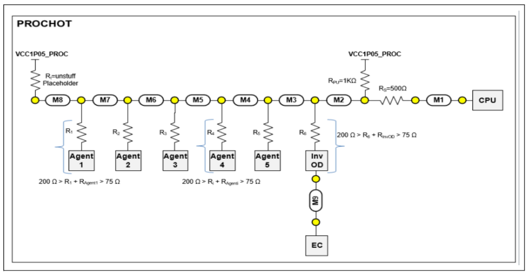
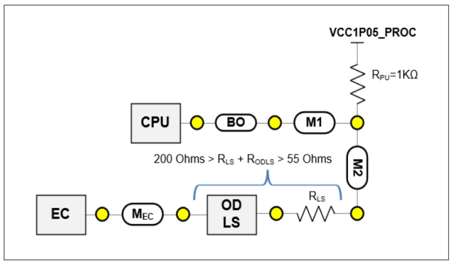
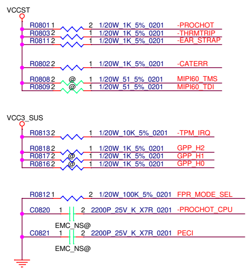
CPU Sideband - PROCHOT# Topology



CPU Sideband - THERMTRIP#





Part	MIPI60	DCI 2.0
R0808	ASM	NO_ASM
R0809	ASM	NO_ASM

need to series 43ohm and place within 500mil form EC.

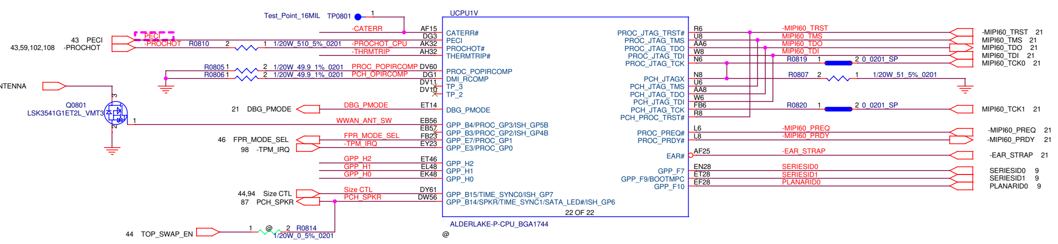


TABLE : Functional Strap

GPP_C5/SML0ALERT# (Boot Strap Bit 0)	
GPP_H0 (Boot Strap Bit 1)	
GPP_H1 (Boot Strap Bit 2)	
GPP_H2 (Boot Strap Bit 3)	
0000b	Master Attached Flash Configuration (Default)
0010b	Master Attached Flash Configuration eSPI is disable
0100b	BIOS on eSPI Peripheral Channel CSME on master attached device
1000b	Slave Attached Flash Configuration
1100b	BIOS on eSPI Peripheral Channel CSME on slave attached SPI

Top Swap Override	DFx Test Mode
GPP_B14/SPKR (Internal PD 20K)	DBG_PMODE (Internal PU 20K)
0 = Disable "Top Swap" mode (Default)	0 = DFx Test Mode Enabled
1 = Enable "Top Swap" mode	1 = DFx Test Mode Disabled (default)

TABLE : Functional Strap

GPP_F7 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

TABLE : Functional Strap

GPP_F10 (Reserved) - Should Sample LOW	
HIGH	
LOW	(Default)

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Boot Halt

SPI0_MOSI (External PU 4.7K)

0 = Enable

1 = Disable

VCC3_SUS

R0902 2 1 1/20W_4.7K_5%_0201 SPI_MOSI_IO0

Consent Strap

SPI0_MOSI (External PU 100K)

0 = Enable

1 = Disable

VCC3_SUS

R0903 2 1 1/20W_100K_5%_0201 SPI_IO2

A0 Personality Strap

SPI0_IO3 (External PU 100K)

0 = Enable

1 = Disable

VCC3_SUS

R0901 2 1 1/20W_100K_5%_0201 SPI_IO3

TLS Confidentiality

GPP_C2/SMBALERT# (Internal PD 20K)

0 = Disable ME Crypto TLS (Default)

1 = Enable ME Crypto TLS with Confidentiality

VCC3_SUS

R0904 2 1 1/20W_1K_5%_0201 GPP_C2

CPUNSSC Clock Frequency

GPP_B23/SML1ALERT#/PCHHOT# (Internal PD 20K)

0 = 38.4MHz Clock (Direct from Crystal) (Default)

1 = 19.2MHz Clock (Derived from 38.4MHz Crystal)

JTAG ODT Disable

GPP_E6/THC0_SPI1_RST# (External PU 100K)

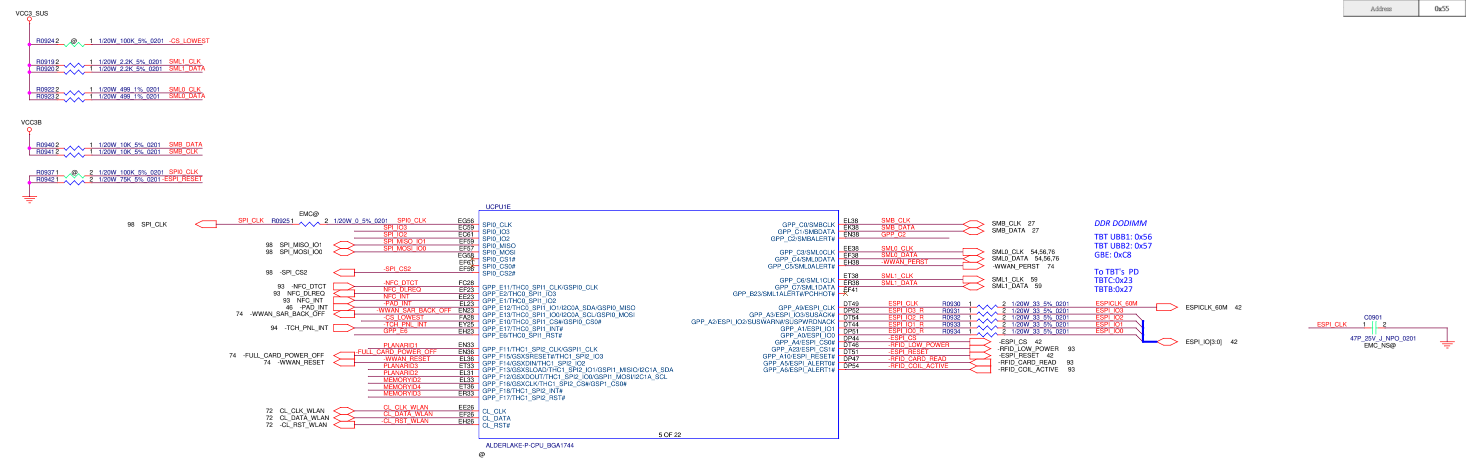
0 = JTAG ODT Disable

1 = JTAG ODT Enabled

VCC3_SUS

R0921 2 1 1/20W_100K_5%_0201 GPP_E6

Project	Griffin/Roc	
PD Controller	TPS65994AE	
Topology	PD port A	PD port B
	TCP2	TCP0
	TBT4	TBT4
net name	TBTC	TBTB
I2C1 SCL/SDA NetName	I2C1_CLK_PD	I2C1_DATA_PD
To where	EC	
Address	0x20	0x24
I2C2 SCL/SDA NetName	SML1_CLK	SML1_DATA
To where	PMC	
Address	0x23	0x27
I2C3 SCL/SDA NetName	I2C3_CLK_PD	I2C3_DATA_PD
To where	BB	
Address	0x57	0x56
PMC to BB's I2C	SML0_CLK	SML0_DATA
Address	0x55	0x56



TABLE

LEVEL	MEMORY ID		
	4	3	2
	R0910	R0911	R0912
1	NA	NA	NA
0	ASM	ASM	ASM

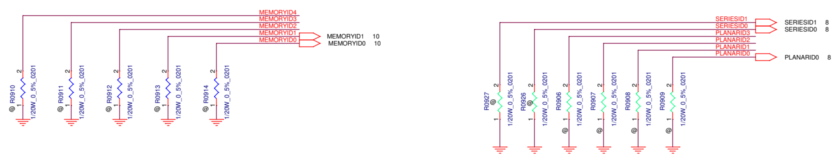


TABLE:

MEMORYID[4:2]	U2501,U2601,U2701,U2801				Total Memory	LCFC PN
	Supplier	Supplier's P/N	Capacity			
0h (000b)	Micron	MT40A1G16RC-062E:B	16Gb	SDP	8GB	SA0000A4K10
1h (001b)		MT40A2G16SKL-062E:B	32Gb	DDP	16GB	SA0000ADR00
2h (010b)	Samsung	K4AAG165WB-BCWE		SDP	8GB	SA0000C6N00
3h (011b)		K4ABG165WB-MCWE		DDP	16GB	SA0000C6P00
4h (100b)	Hynix	H5ANAG6NCJR-XNC		SDP	8GB	SA0000B5K00
5h (101b)		H5ANBG6NCMR-XNC		DDP	16GB	SA0000C6T00

TABLE

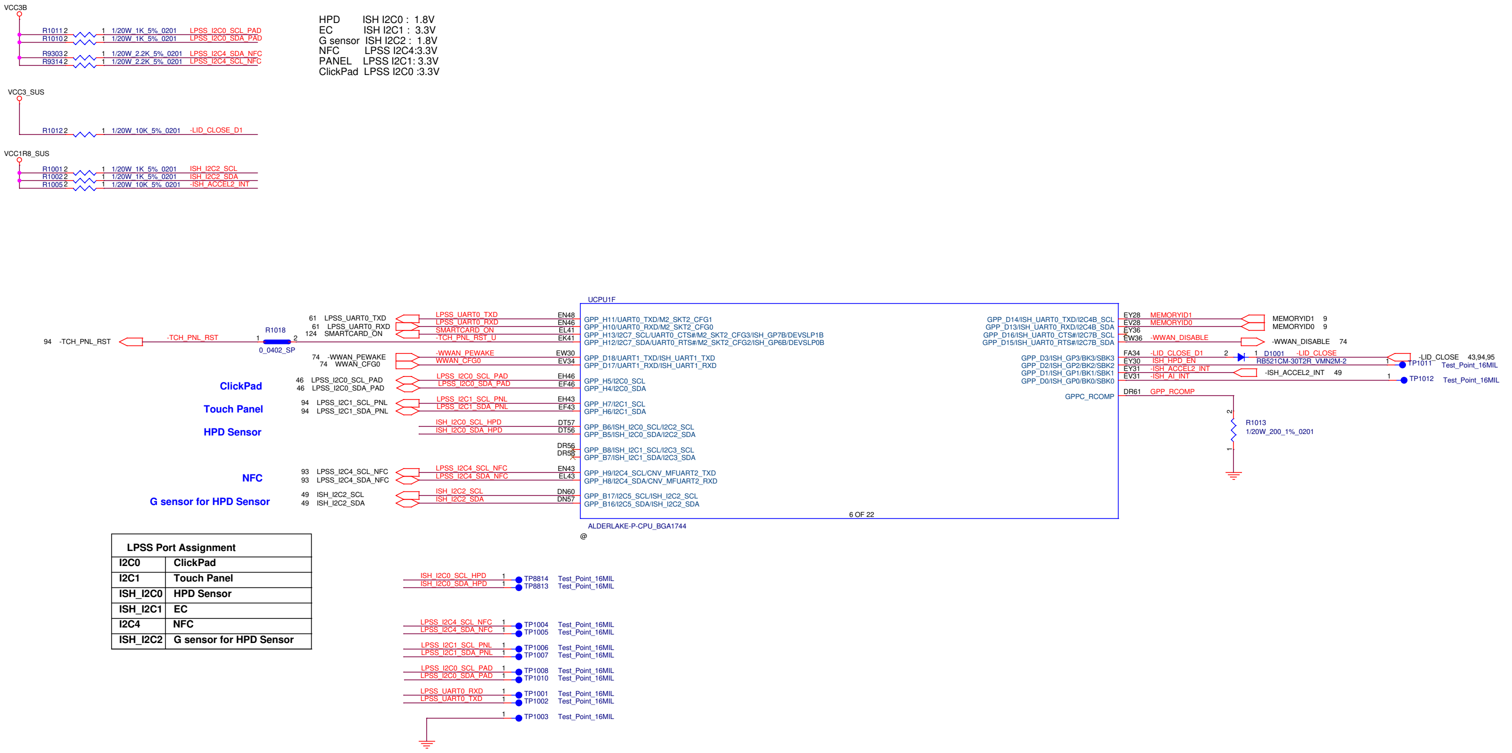
LEVEL	Series ID	
	1	0
	R0927	R0926
1	T	ThinkPAD
0	Ts/X	NEC

TABLE

LEVEL	PLANAR ID			
	3	2	1	0
	R0906	R0907	R0908	R0909
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

TABLE

LEVEL	PLANARID[3:0]
EVT	0000b
FVT	0001b
SIT	0100b
SVT	1111b



LPSS Port Assignment	
I2C0	ClickPad
I2C1	Touch Panel
ISH_I2C0	HPD Sensor
ISH_I2C1	EC
I2C4	NFC
ISH_I2C2	G sensor for HPD Sensor

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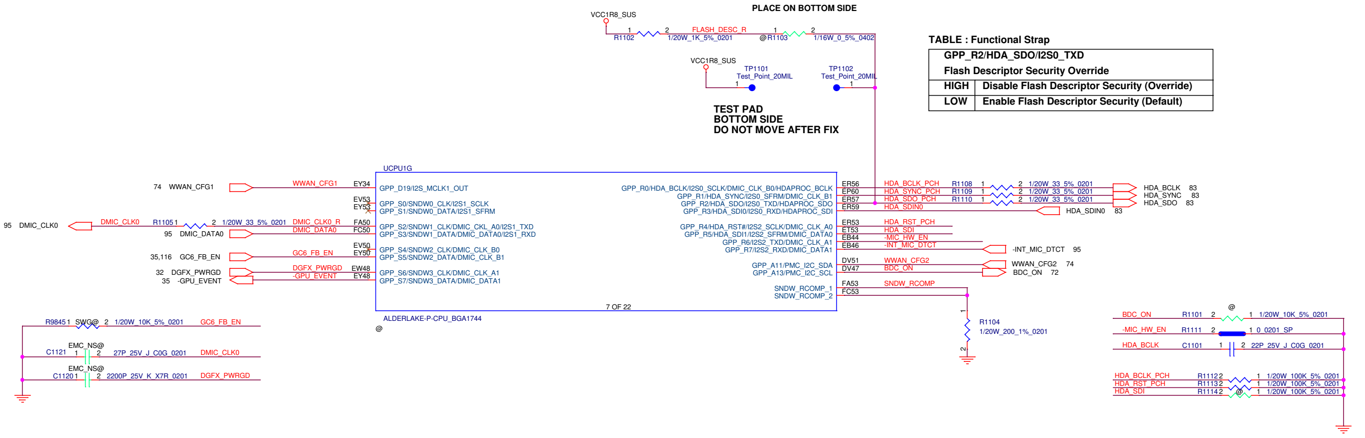


TABLE : Functional Strap

GPP_R2/HDA_SDO/I2S0_TXD Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

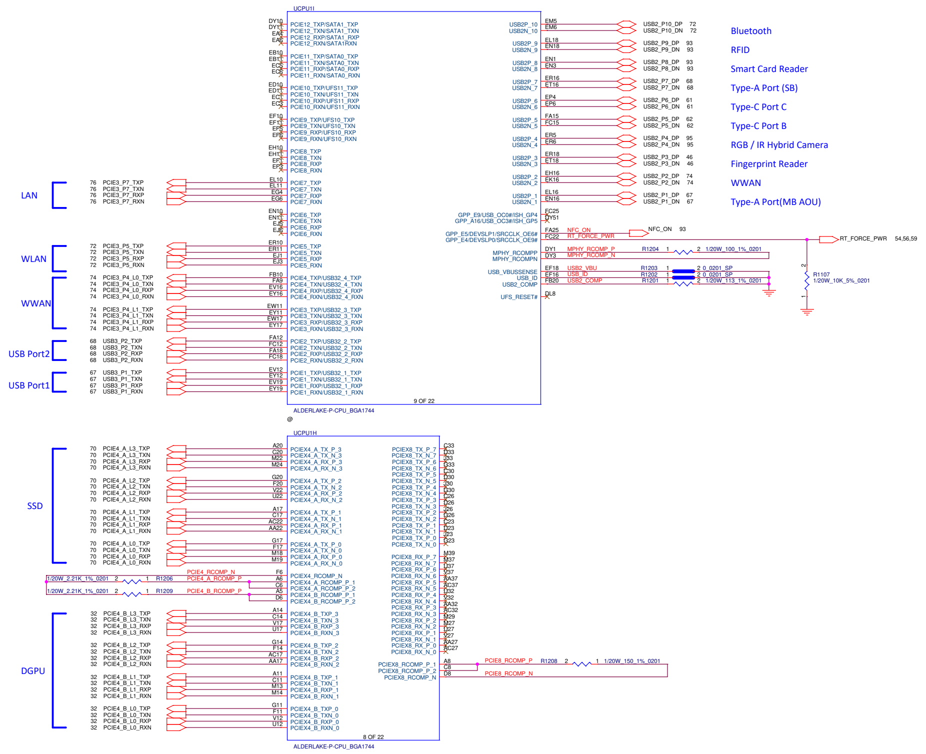
Flexible I/O Configuration								
HSIO Port	High Speed Signals	PCI Device	PCI Function	HSIO Configuration	Descriptor for PCIe	Net Name	PCI Device	PCI Function
PCH L0	USB 3.1 #1 / PCIe Gen3 #1	1Ch	0h	USB 3.1 #1	1x2, 2x1 Lane Reversal Enabled	N/A	14h	0h
PCH L1	USB 3.1 #2 / PCIe Gen3 #2		1h	USB 3.1 #2		USB3_P2		
PCH L2	USB 3.1 #3 / PCIe Gen3 #3		2h	PCIe Gen3 #3		PCIE3_P1_L1		
PCH L3	USB 3.1 #4 / PCIe Gen3 #4		3h	PCIe Gen3 #4		PCIE3_P1_L0	1Ch	0h
PCH L4	PCIe Gen3 #5	1Ch	4h	PCIe Gen3 #5	4x1 Lane Reversal Disabled	N/A	1Fh	6h
PCH L5	PCIe Gen3 #6		5h	PCIe Gen3 #6		N/A		
PCH L6	PCIe Gen3 #7 (GbE)		6h	PCIe Gen3 #7 (GbE)		PCIE3_P7		
PCH L7	PCIe Gen3 #8 (GbE)		7h	PCIe Gen3 #8		N/A		
PCH L8	PCIe Gen3 #9 (GbE)	1Dh	0h	PCIe Gen3 #9 (x4)	1x4 Lane Reversal Disabled	N/A		
PCH L9	PCIe Gen3 #10		1h	PCIe Gen3 #10 (x4)		N/A		
PCH L10	PCIe Gen3 #11 / SATA #0		2h	PCIe Gen3 #11 (x4)		N/A		
PCH L11	PCIe Gen3 #12 / SATA #1		3h	PCIe Gen3 #12 (x4)		N/A		
CPU_A L0	PCIe Gen4 x4Lane 0	06h	0h	PCIe Gen4 (x4) L0	1x4 Lane Reversal Disabled	PCIE4_L0	06h	0h
CPU_A L1	PCIe Gen4 x4Lane 1			PCIe Gen4 (x4) L1		PCIE4_L1		
CPU_A L2	PCIe Gen4 x4Lane 2			PCIe Gen4 (x4) L2		PCIE4_L2		
CPU_A L3	PCIe Gen4 x4Lane 3			PCIe Gen4 (x4) L3		PCIE4_L3		
CPU_B L0	PCIe Gen4 x4Lane 0			PCIe Gen4 (x4) L0	1x4 Lane Reversal Disabled	PCIE4_L0		
CPU_B L1	PCIe Gen4 x4Lane 1			PCIe Gen4 (x4) L1		PCIE4_L1		
CPU_B L2	PCIe Gen4 x4Lane 2			PCIe Gen4 (x4) L2		PCIE4_L2		
CPU_B L3	PCIe Gen4 x4Lane 3			PCIe Gen4 (x4) L3		PCIE4_L3		

PCIe Port Assignment	
PCIE3_P1	(USB3_P1)
PCIE3_P2	(USB3_P2)
PCIE3_P3	WWAN Lane 1
PCIE3_P4	WWAN Lane 0
PCIE3_P5	(WLAN)
PCIE3_P6	(Reserved)
PCIE3_P7	GbE
PCIE3_P8	(Reserved)
PCIE3_P9	(Reserved)
PCIE4 (x4)	NVMe SSD
PCIE4 (x4)	DGPU

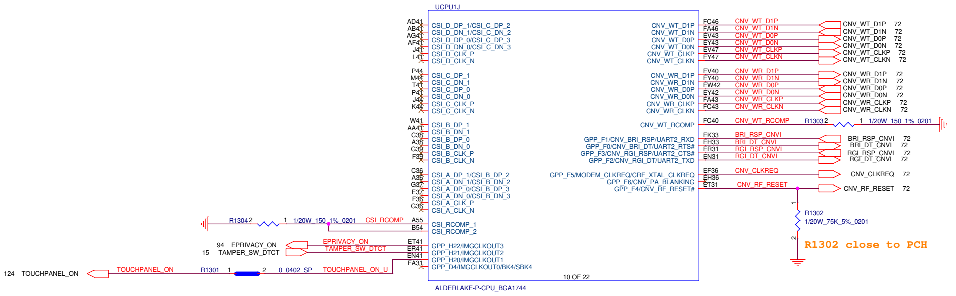
SATA Port Assignment	
SATA_P0	(PCIE3_P11)
SATA_P1	(PCIE3_P12)

USB 3.1 Port Assignment	
USB3_P1	Type-A Port (AOU)
USB3_P2	(Type-A Port)
USB3_P3	(PCIE3_P3)
USB3_P4	(PCIE3_P4)

USB 2.0 Port Assignment	
USB2_P1	Type-A Port (AOU)
USB2_P2	WWAN
USB2_P3	Fingerprint Reader
USB2_P4	RGB / IR Hybrid Camera
USB2_P5	Type-C Port B
USB2_P6	Type-C Port C
USB2_P7	(Type-A Port)
USB2_P8	(Smart Card Reader)
USB2_P9	(RFID)
USB2_P10	(Bluetooth)



Document Number	LCFC	
Size: Custom	Title: 012_CPU(8/16): PCIE/USB/SATA	Rev: 0.01
Date:	Friday, December 03, 2021	Sheet 12 of 130



M.2 CNVi Mode Selec

GPP_F2/CNV_RGI_DT (External PU 100K)

0 = Integrated CNVi Enabled

1 = Integrated CNVi Disabled

VCC1R8_SUS
R7216 1 2 1/20W_100K_5%_0201 RGI_DT_CNVI
R7220 1 @ 2 1/20W_4.7K_1%_0201

R7216 close to device

XTAL Frequency Selection

GPP_F0/CNV_BRI_DT (Internal PD 20K)

0 = 38.4MHz XTAL frequency selected (Default)

1 = 24MHz XTAL selected

VCC1R8_SUS
R7215 1 @ 2 1/20W_4.7K_1%_0201 BRI_DT_CNVI
R7219 1 @ 2 1/20W_20K_5%_0201

R7215, close to device

CNVi_WT_RCOMP

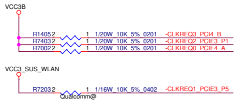
Interface	Ball Number	Pin Name	Board Rterm (Ohm)	Board DC resistance (ohms)	Board parasitic capacitance (pF)	Resistor Stuffing	Notes
PCH interface	FC40	CNV_WT_RCOMP	150 ohm +/-1 % pull-down to GND	<0.5	-	Mandatory	Pkg trace + Board trace <1pF should be sufficient

[Issue Symptom]
All PCIe device can't recognize

[Root cause]
GPP_F0 strap not correct setting.

[Solution]
GPIO need to set up "native" and can't have PU resistance.

PCIECLK and CLKREQ# Port Assignment		
Port 0	PCIe Gen4 A(x4)	NVMe SSD
Port 1	PCIe Gen3 P5	(M.2 WLAN)
Port 2	PCIe Gen3 P1	M.2 WWAN
Port 3	PCIe Gen4 B (x4)	(dGPU)
Port 4	PCIe Gen3 P7	GbE
Port 5	PCIe Gen3 P8	
Port 6	PCIe Gen3 P6	(Reserved)



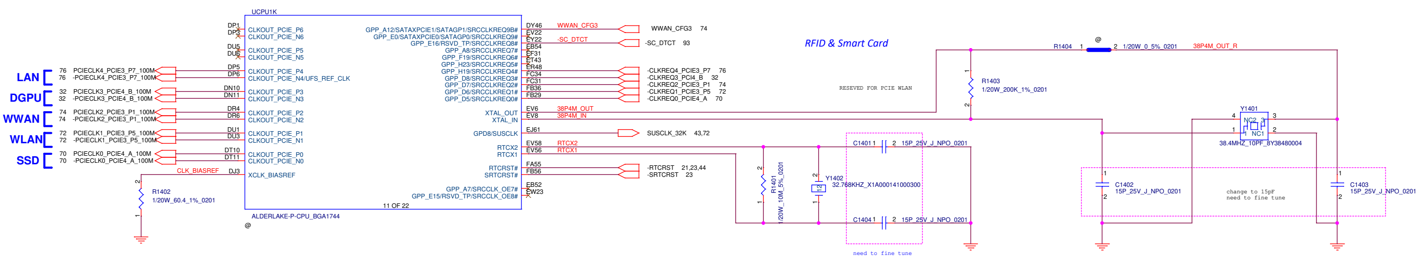


TABLE of Y1402		
Vendor	P/N	LCFC P/N
EPSON	X1A0001410003	SJ10000LM00
TXC	9H03280013	SJ100011T00
KDS	7BD03276A2S	SJ100011W00

TABLE of Y1401		
Vendor	P/N	LCFC P/N
TXC	8Y38480004	SJ10000SN00
KDS	7AF03840A04	SJ10000XG00
MURATA	XRCGB38M400F2T10R0	SJ100012100

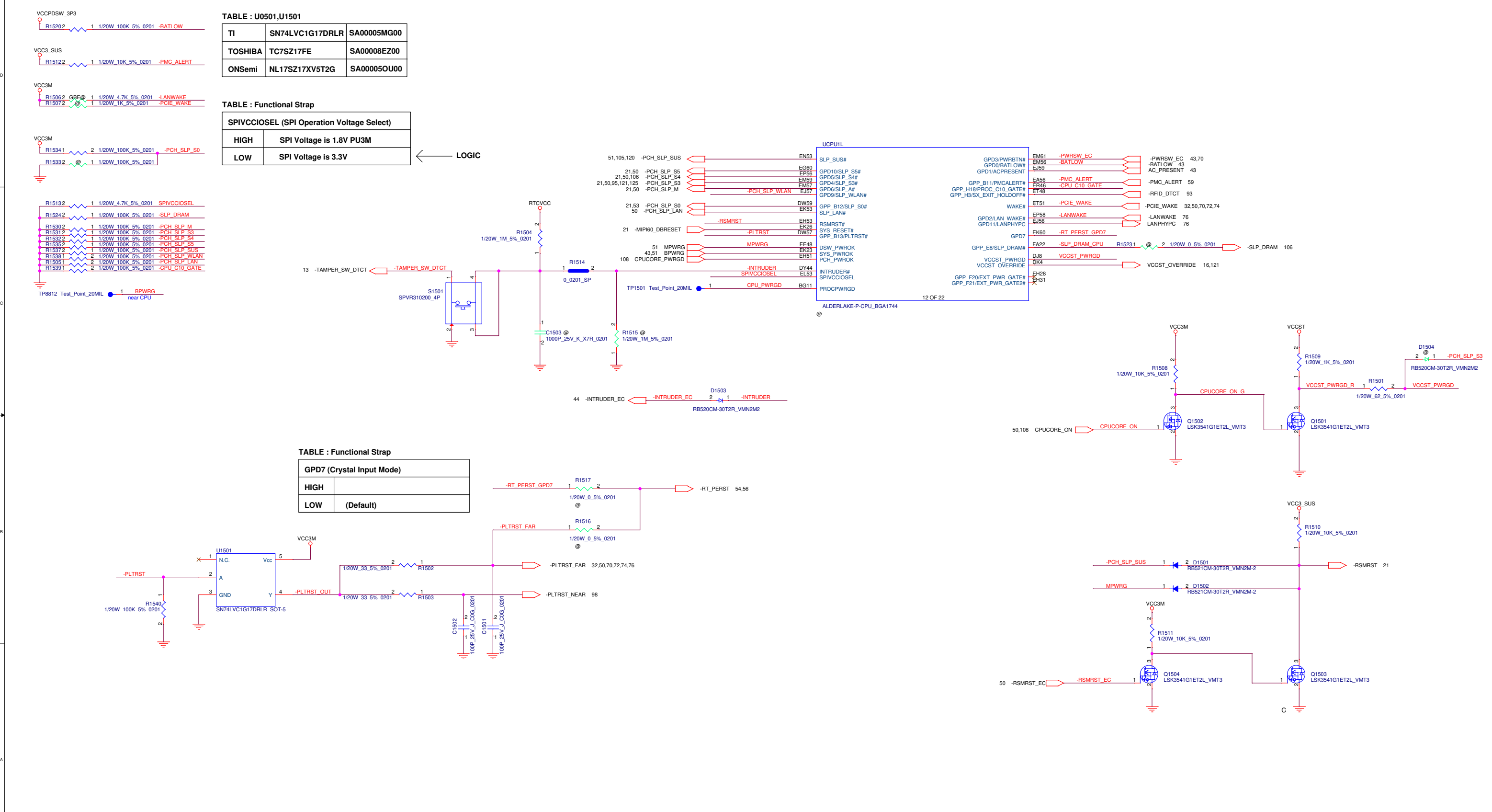


TABLE : U0501,U1501

TI	SN74LVC1G17DRLR	SA00005MG00
TOSHIBA	TC7SZ17FE	SA00008EZ00
ONSemi	NL17SZ17XV5T2G	SA00005OU00

TABLE : Functional Strap

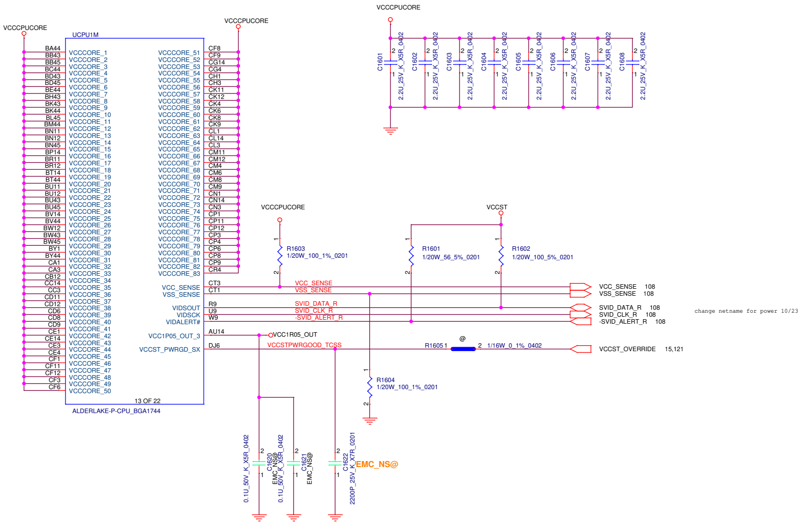
SPIVCCIOSEL (SPI Operation Voltage Select)	
HIGH	SPI Voltage is 1.8V PU3M
LOW	SPI Voltage is 3.3V

LOGIC

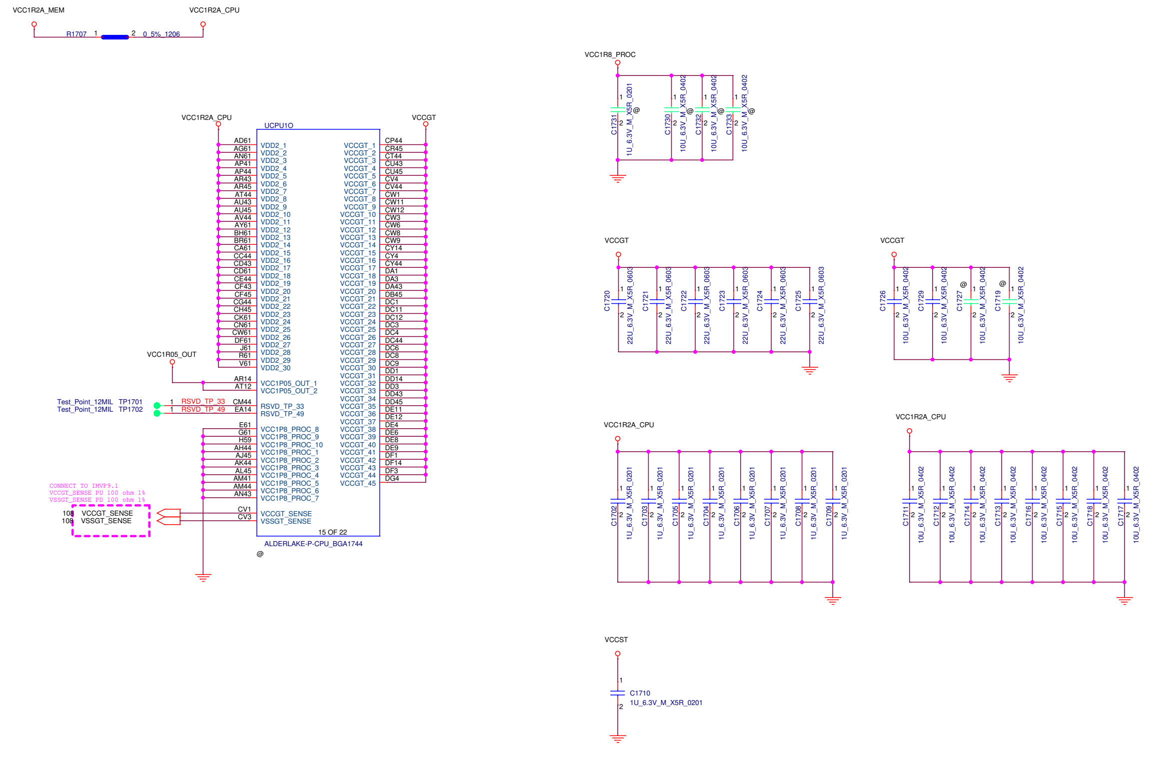
TABLE : Functional Strap

GPD7 (Crystal Input Mode)	
HIGH	
LOW	(Default)

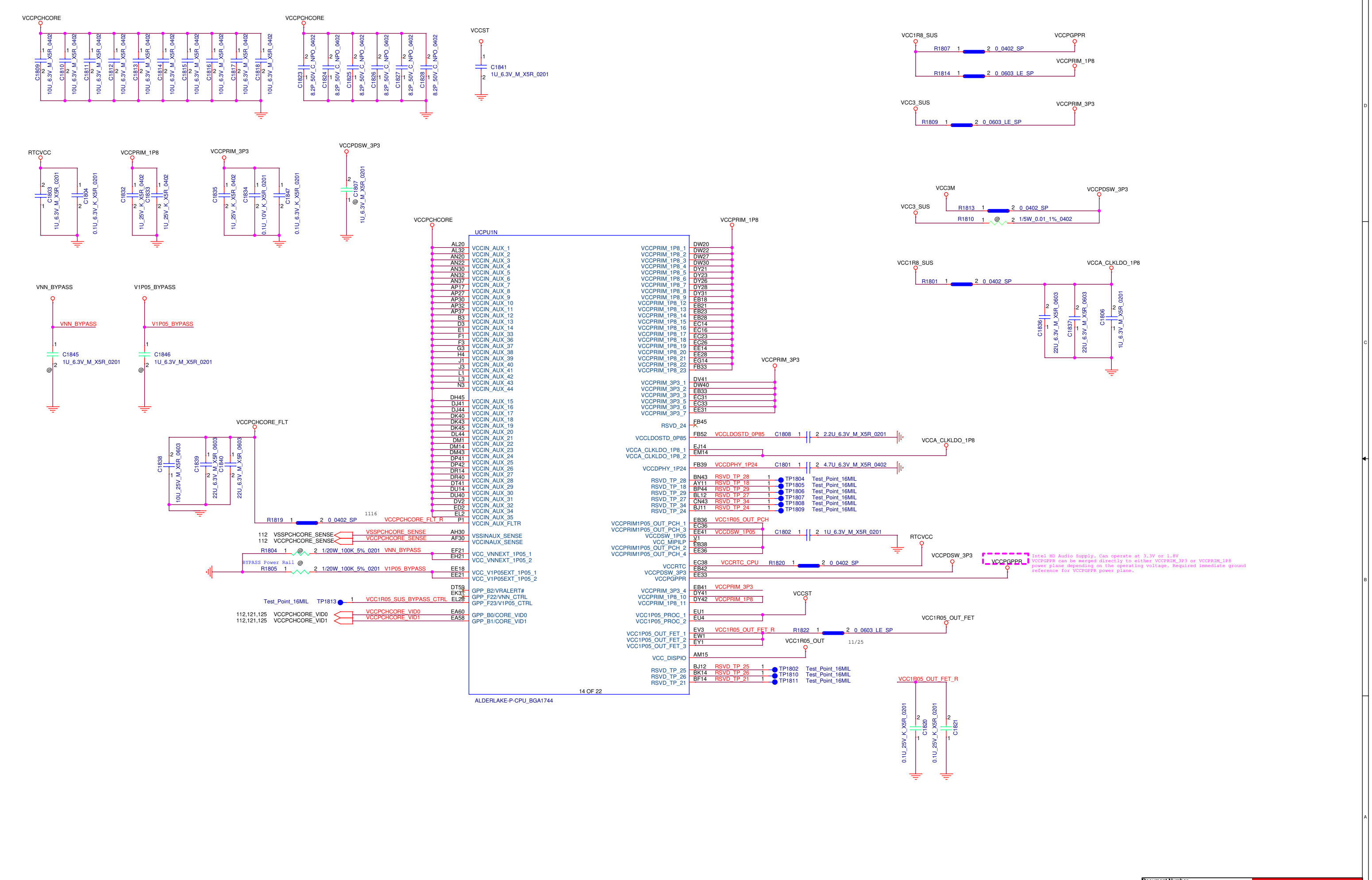
Document Number		LCFC
Size Custom	Title 015_CPU(11/16): SYSTEM PM	Rev 0.01
Date: Friday, December 03, 2021	Sheet 15 of 130	



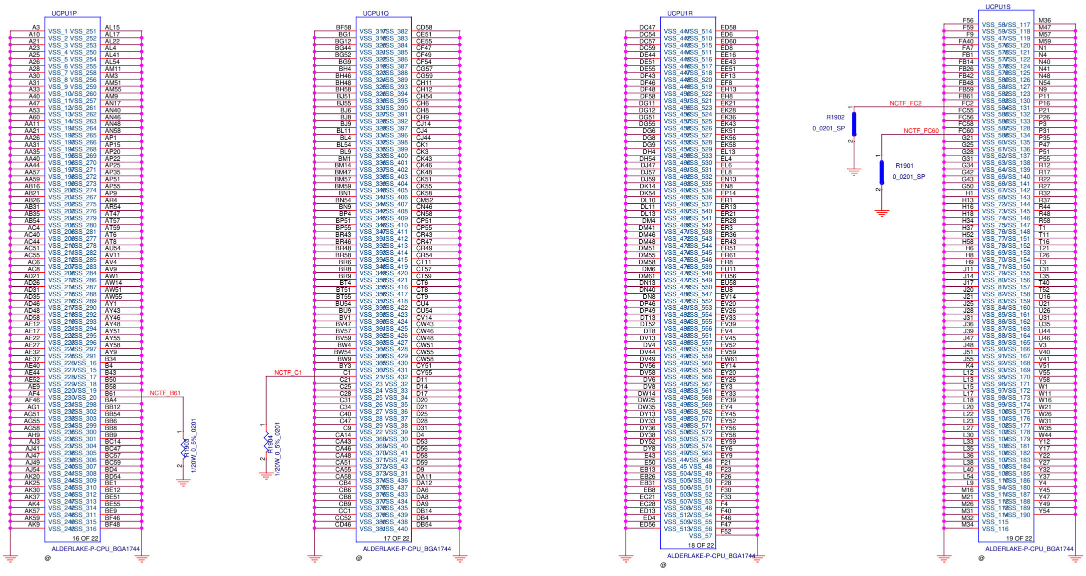
Document Number	LCFC	
Size: Custom	Title: 016_CPU(12/16): CPU POWER (1/2)	Rev
Date: Friday, December 03, 2021	Sheet 16 of 130	



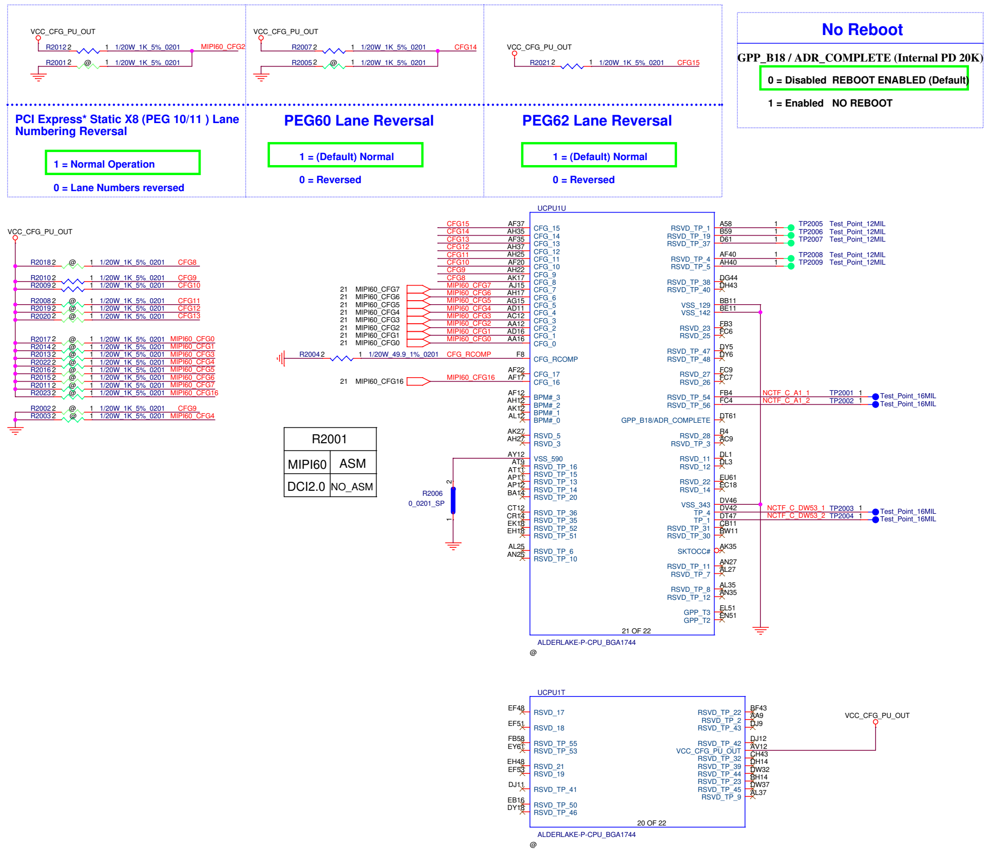
Document Number		LCFC
Size C	Title 017_CPU(13/16): CPU POWER(2/2)	Rev
Date: Friday, December 03, 2021	Sheet 17 of 130	



Document Number		
Size: Custom	Title: 018_CPU(14/16): PCH POWER	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 18 of 130	



Document Number		LCFC
Size Custom	Title **019_CPU(15/16): GND**	Rev 0.01
Date:	Friday, December 03, 2021	Sheet 19 of 130

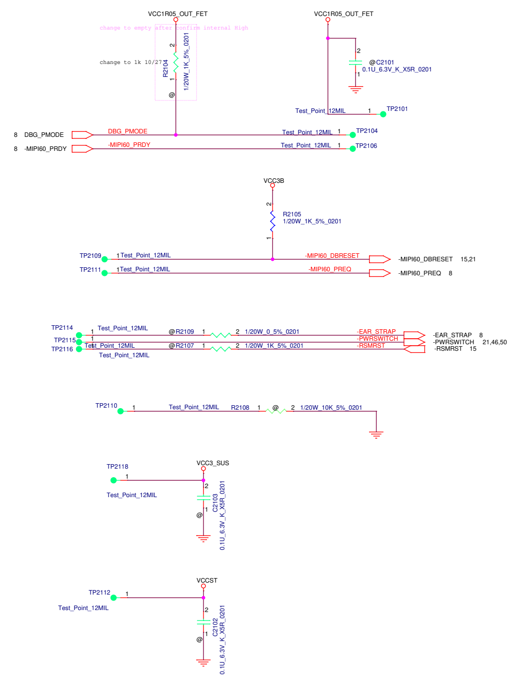


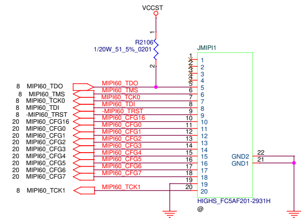
CFG Signals Functionality and Termination

CFG	Description	Termination	Resistor
EAR	Stall CPU reset sequence until de-asserted: - 1 = (Default) Normal Operation; No stall. - 0 = Stall	Pull -Up to VCC1P05_PROC	1K ohm
CFG[0]	RSVD	None	
CFG[1]	RSVD	None	

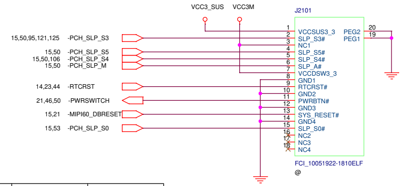
CFG	Description	Termination	Resistor
CFG[2]	PCI Express* Static X8 (PEG 10/11) Lane Numbering Reversal • 1:Normal Operation • 0: Lane Numbers reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[3]	RSVD	None	
CFG[4]	RSVD	None	
CFG[5]	RSVD	None	
CFG[6]	RSVD	NONE	
CFG[8:7]	RSVD	None	
CFG[10:9]	RSVD	Pull -Up to VCC_CFG_PU_OUT[1]	1K Ohm
CFG[13:11]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[15]	PEG62 Lane Reversal: • - 1 - (Default) Normal • - 0 - Reversed	Pull -Up to VCC_CFG_PU_OUT / Pull-down- Platform design dependent	1K ohm
CFG[17:16]	RSVD	None	

Note: 1.To ensure reliable boot across HVM.





APS/PETS Interface

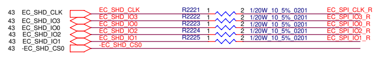


TABLE

Logic	Ref Des	MIPI60	DCI 2.0
Page8	R0808	ASM	NO_ASM
	R0809	ASM	NO_ASM
Page 20	R2001	ASM	NO_ASM
Page 21	J8	ASM	NO_ASM
	C2101	ASM	NO_ASM
	C2102	ASM	NO_ASM
	C2103	ASM	NO_ASM
	R2108	ASM	NO_ASM
	R2106	ASM	ASM
	R2105	ASM	ASM
	R2104	ASM	NO_ASM
	R2107	ASM	NO_ASM
	R2109	ASM	NO_ASM

LOGIC

Document Number
LCFC
Size: Custom
Title: 021_MIPI60 DEBUG PORT
Rev: 0.01
Date: Friday, December 03, 2021 Sheet 21 of 130



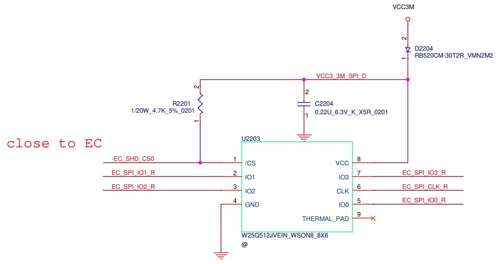
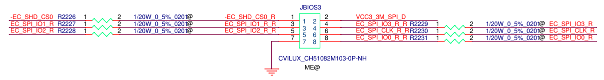
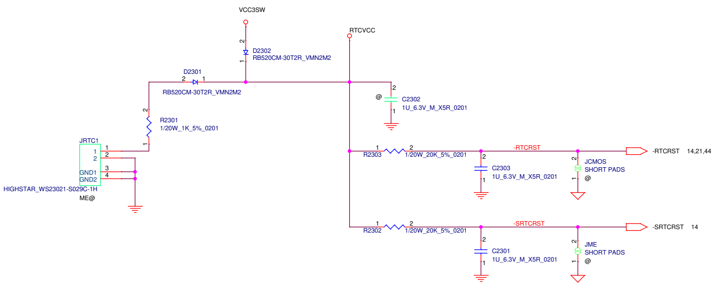


TABLE:U2203

64MB (512Mb) 8x6mm WSON		Part Number
Winbond	W25Q512JVEIN	SA0000BUN00
GigaDevie	GD25B512MEYIGR	SA0000BV300
Macronix	MX25L51273GZ4I-08G	SA0000CDT00



Document Number	LCFC	
Size: Custom	Title: 022_SPI FLASH	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 22 of 130	



Document Number		
Size: Custom	Title: 023_RTC BATTERY	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 23 of 130	

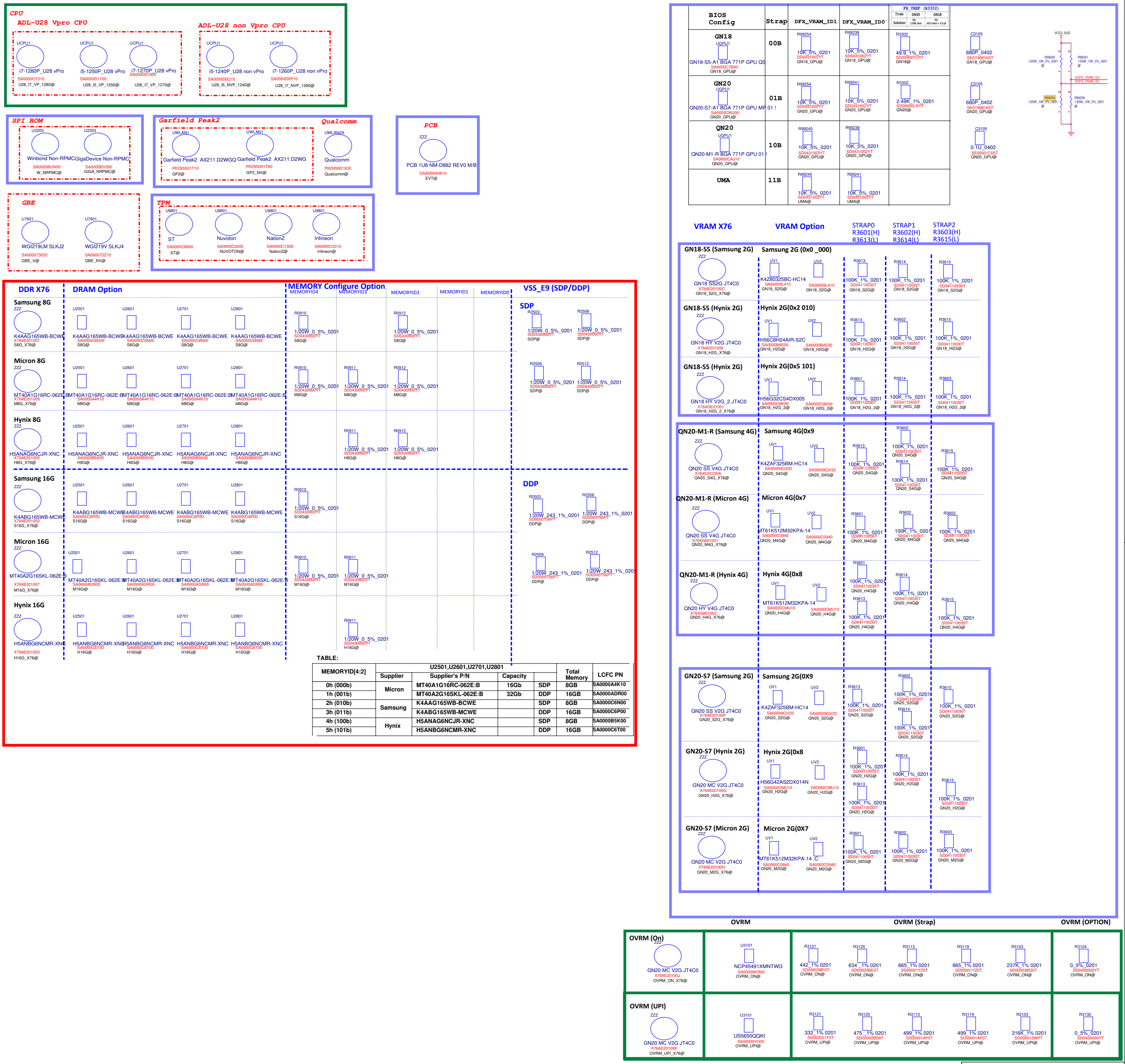
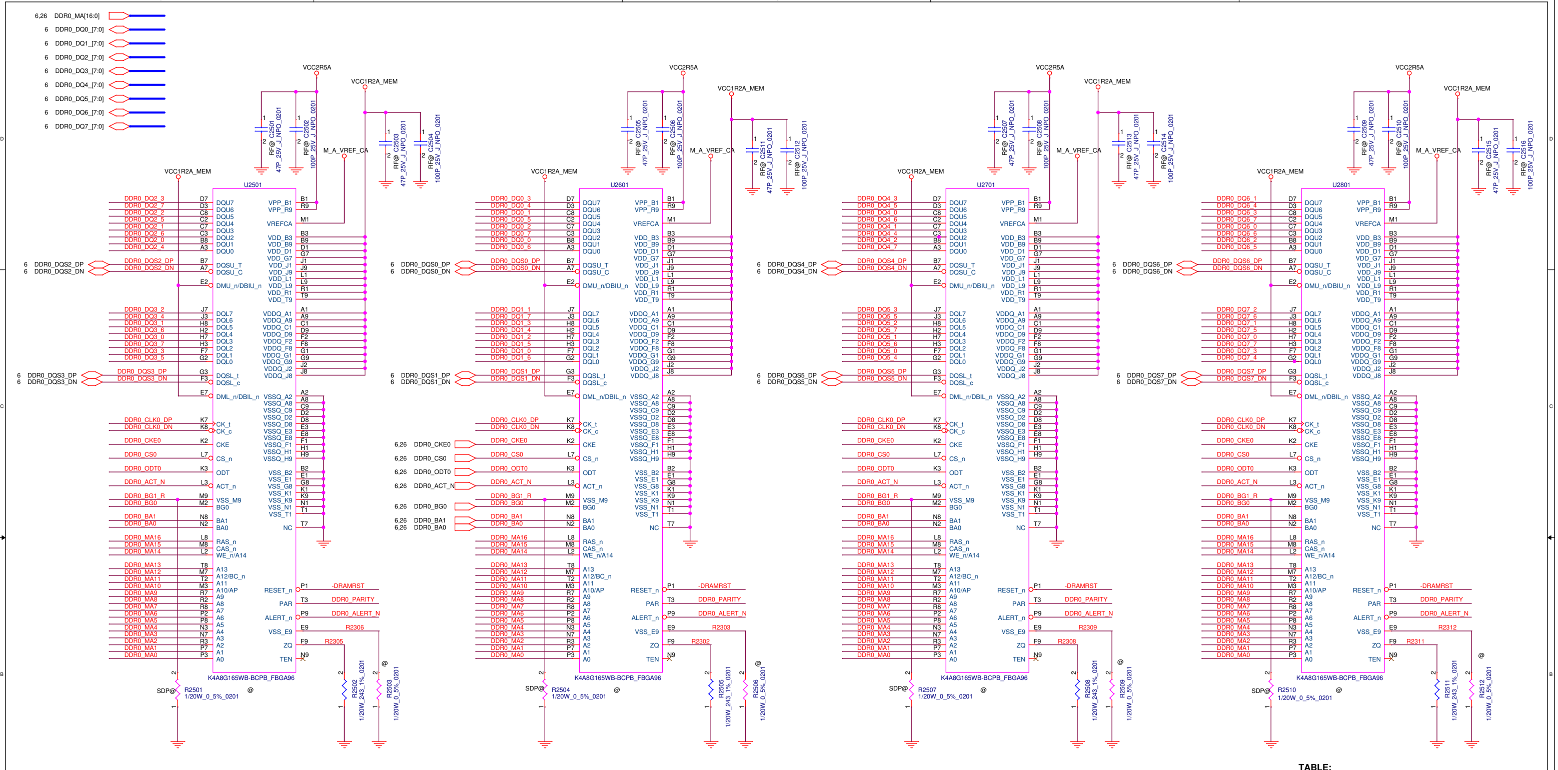
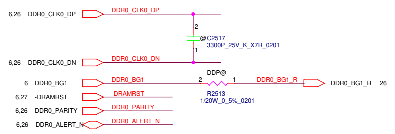


TABLE:

MEMORYID[4:2]	U2501,U2601,U2701,U2801				Total Memory	LCFC PN
	Supplier	Supplier's P/N	Capacity			
0h (000b)	Micron	MT40A1G16RC-062E:B	16Gb	SDP	8GB	SA0000A4K10
1h (001b)		MT40A2G16SKL-062E:B	32Gb	DDP	16GB	SA0000ADR00
2h (010b)	Samsung	K4AAG165WB-BCWE		SDP	8GB	SA0000C6N00
3h (011b)		K4ABG165WB-MCWE		DDP	16GB	SA0000C6P00
4h (100b)	Hynix	H5ANAG6NCJR-XNC		SDP	8GB	SA0000B5K00
5h (101b)		H5ANBG6NCMR-XNC		DDP	16GB	SA0000C6T00

Item	GN20	GN18
Solution	PD 2.49k ohm	PD 49.9 ohm + 3.9 pF






```
Original PN:SA00007DA00
Original Footprint : K4A8G165WB-BCPB_FBGA_96P
Temp Footprint : Samsung_memorydown_4G-XX
```

Supplier	Capacity	Supplier's P/N	Package Size		Die	Configuration	VSS_E9	BG1 / VSS	Ch. A	Ch. B
Micron	16Gbit	MT40A1G16KD-062E:E	10 x 13 mm	SDP	16Gb (1Gx16)	1 Rank x (1Gx16)	0_5%	BG1	8GB	SODIMM
	32Gbit	MT40A2G16SKL-062E:B	10.5 x 13.0 mm	DDP	32Gb (2Gx16)	1 Rank x (2Gx16)	243_1%	BG1	16GB	SODIMM
Samsung	16Gbit	K4AAG165WA-BCWE	9.5 x 13.3 mm	SDP	16Gb (1Gx16)	1 Rank x (1Gx16)	0_5%	BG1	8GB	SODIMM
	32Gbit	K4ABG165WA-MCWE	9.5 x 13.3 mm	DDP	32Gb (2Gx16)	1 Rank x (2Gx16)	243_1%	BG1	16GB	SODIMM
SK hynix	16Gbit	H5ANAG6NCJR-XNC	10 x 13.0 mm	SDP	16Gb (1Gx16)	1 Rank x (1Gx16)	0_5%	BG1	8GB	SODIMM
	32Gbit	H5ANBG6NCMR-XNC	10.5 x 13.0 mm	DDP	32Gb (2Gx16)	1 Rank x (2Gx16)	243_1%	BG1	16GB	SODIMM

TABLE:

	SDP	DDP
R2501	ASM	NA
R2504	ASM	NA
R2507	ASM	NA
R2510	ASM	NA
R2513	NA	ASM
R2618	NA	ASM
R2503	0_5%	243_1%
R2506	0_5%	243_1%
R2509	0_5%	243_1%
R2512	0_5%	243_1%

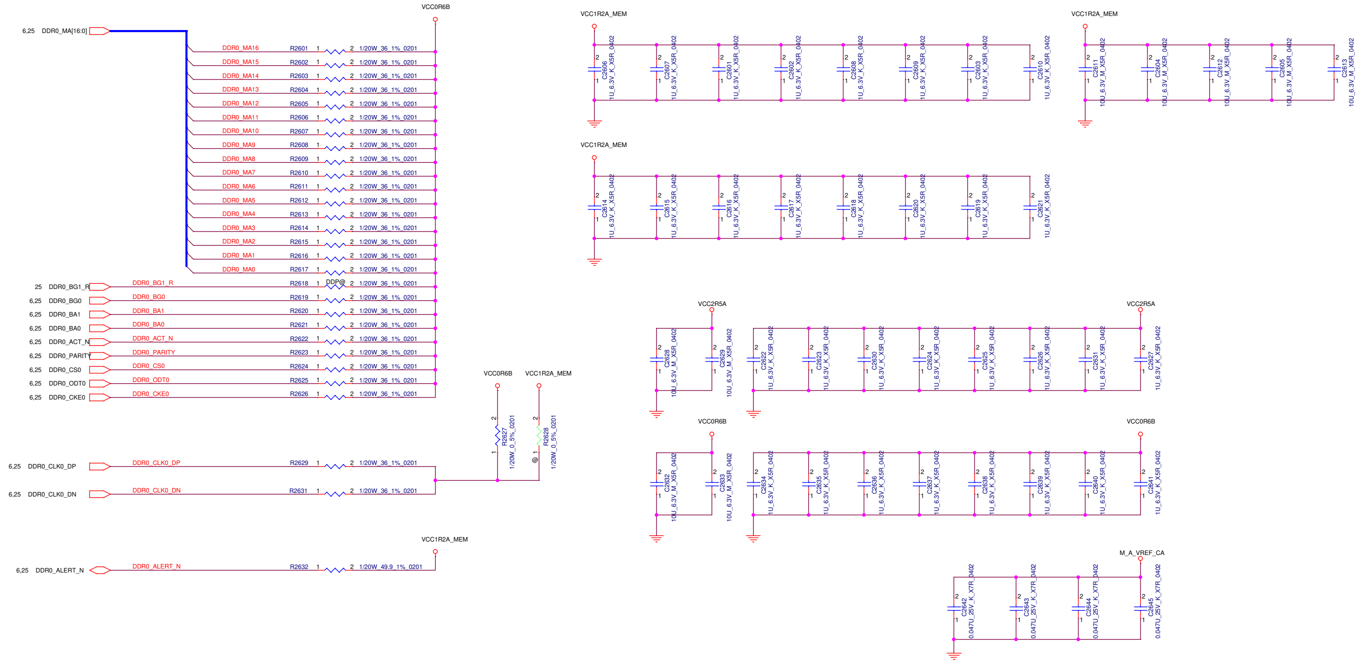
DRAM Configuration: X76@

Document Number		LCFC
Size: Custom	Title: **DDR4 SUB CHANNEL-A MD_1**	Rev: 0.01
Date:	Friday, December 03, 2021	Sheet 25 of 130

VCC1R2A	PDG	LCFC
1uF_0402	16	HW:16/PWR:0
10uF_0603	5	HW:5/PWR:0

VCC0R6B	PDG	LCFC
1uF_0402	8	HW:8/PWR:0
10uF_0603	2	HW:2/PWR:0

VCC2R5A	PDG	LCFC
1uF_0402	8	HW:8/PWR:0
10uF_0603	2	HW:2/PWR:0

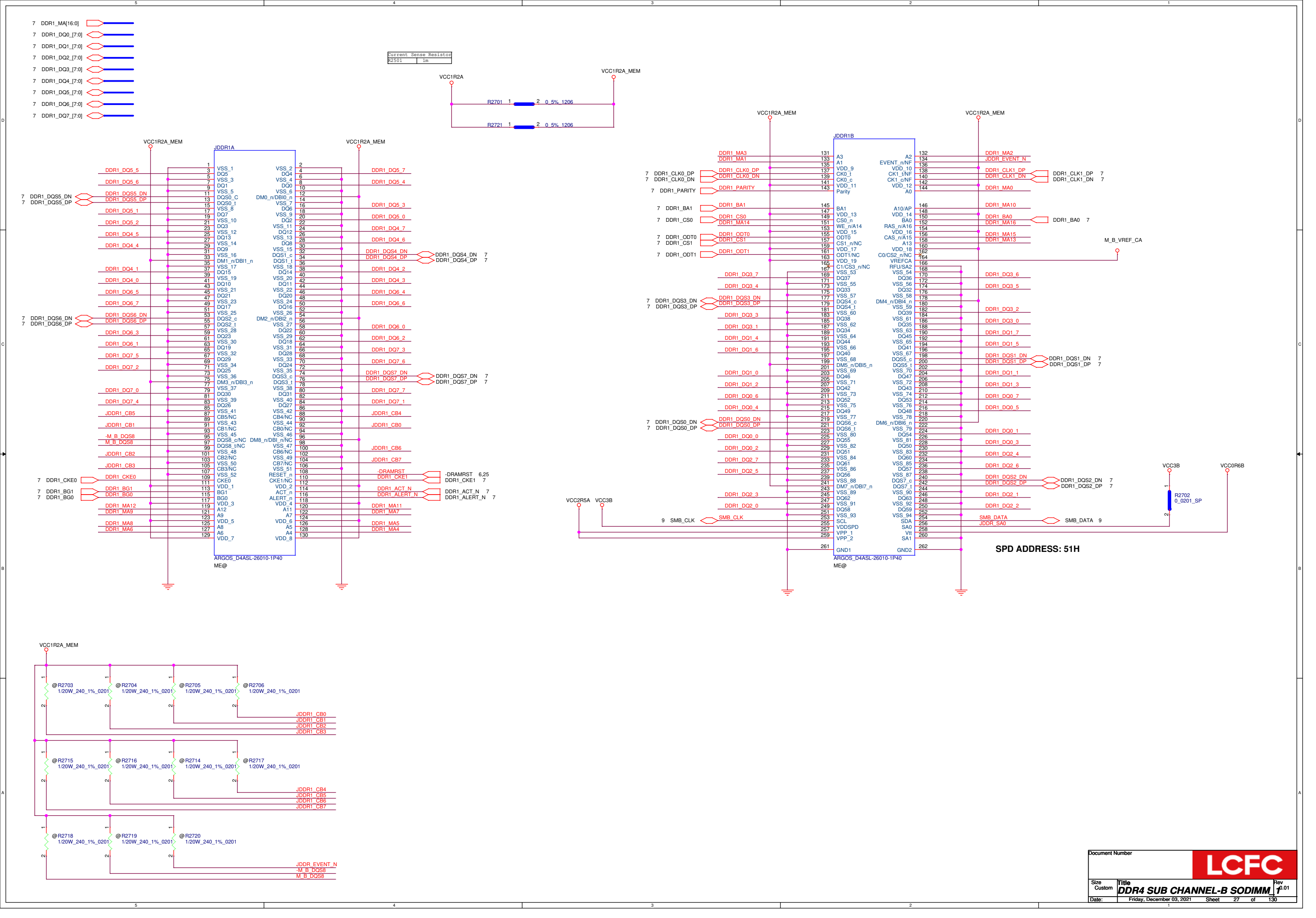


Document Number

LCFC

Size	Title	Rev
Custom	DDR4 SUB CHANNEL-A MD_2	0.01

Date: Friday, December 03, 2021 Sheet 26 of 130

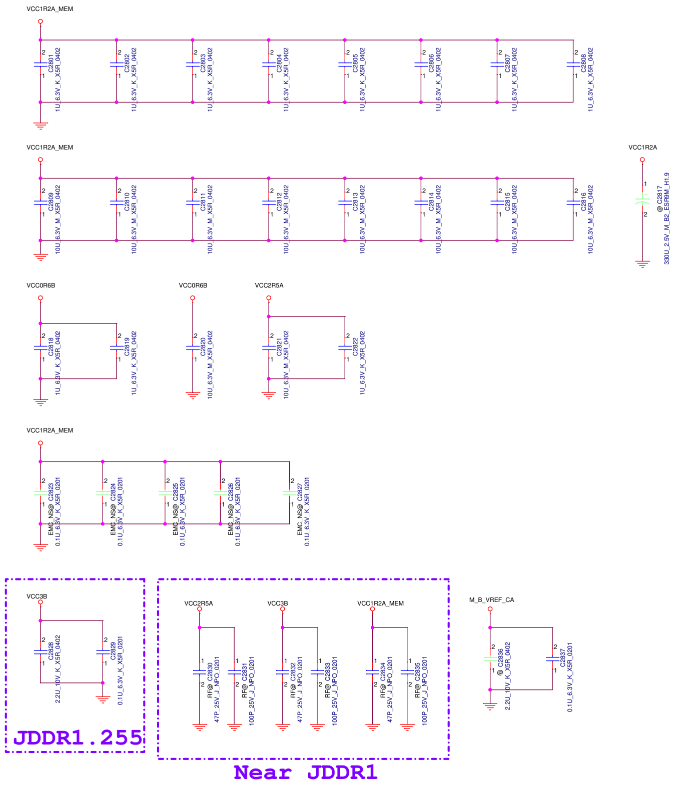

Current Sense Resistor
R2501 1m
VCC1R2A
VCC1R2A_MEM
R2701 0_5%_1206
R2721 0_5%_1206
JDDR1A
ARGOS_D4ASL-26010-1P40
ME@
JDDR1B
ARGOS_D4ASL-26010-1P40
ME@
M_B_VREF_CA
VCC3B
VCC2R5A
VCC0R6B
R2702 0_0201_SP
SMB_CLK
SMB_DATA
SPD ADDRESS: 51H
R2703 1/20W_240_1%_0201
R2704 1/20W_240_1%_0201
R2705 1/20W_240_1%_0201
R2706 1/20W_240_1%_0201
R2715 1/20W_240_1%_0201
R2716 1/20W_240_1%_0201
R2714 1/20W_240_1%_0201
R2717 1/20W_240_1%_0201
R2718 1/20W_240_1%_0201
R2719 1/20W_240_1%_0201
R2720 1/20W_240_1%_0201
LCFC
Document Number
Size Custom
Title
DDR4 SUB CHANNEL-B SODIMM_1
Rev 0.01
Date: Friday, December 03, 2021
Sheet 27 of 130

VCC1R2A	PDG	LCFC
1uF_0402	8	HW:8/PWR:0
10uF_0603	8	HW:8/PWR:0
330uF_B2	1	HW:0/PWR:0

JDDR1.255	PDG	LCFC
0.1uF_0402	1	HW:1/PWR:0
2.2uF_0402	1	HW:1/PWR:0

VCC0R6B	PDG	LCFC
1uF_0402	2	HW:2/PWR:0
10uF_0603	1	HW:1/PWR:0

VCC2R5A	PDG	LCFC
1uF_0402	1	HW:1/PWR:0
10uF_0603	1	HW:1/PWR:0



Document Number	
Size: Custom	Title: DDR4 SUB CHANNEL-B SODIMM_2
Rev: 0.01	
Date: Friday, December 03, 2021	Sheet 28 of 130

Document Number	LCFC
Size: Custom	Title: 029_BLANK	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 29 of 130

Netname	
SH_IN_N1/P1	Monitor NVVDD
SH_IN_N2/P2	Monitor FBVDD

OVR-M GEN1

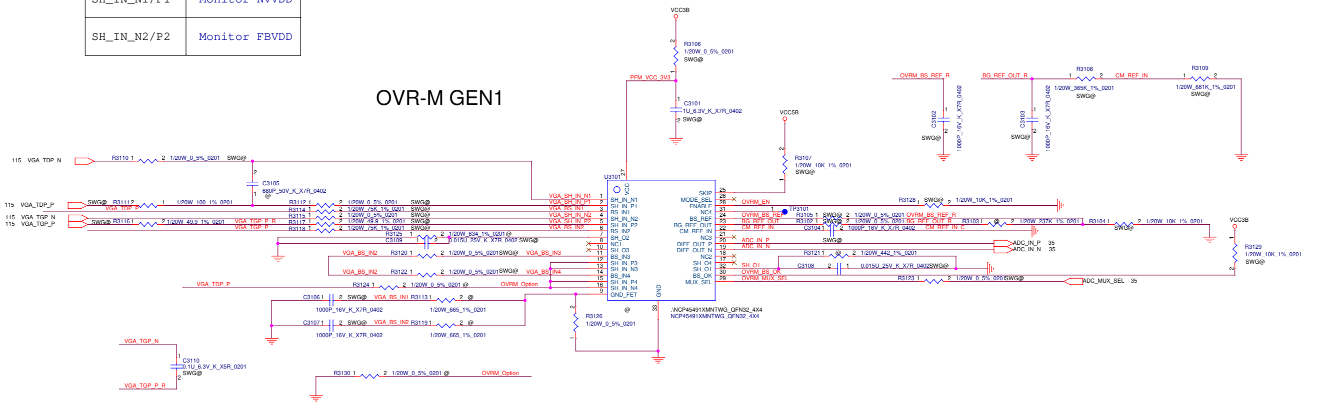
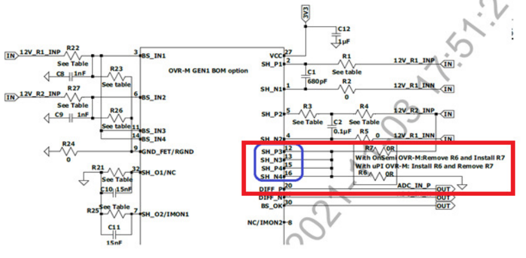
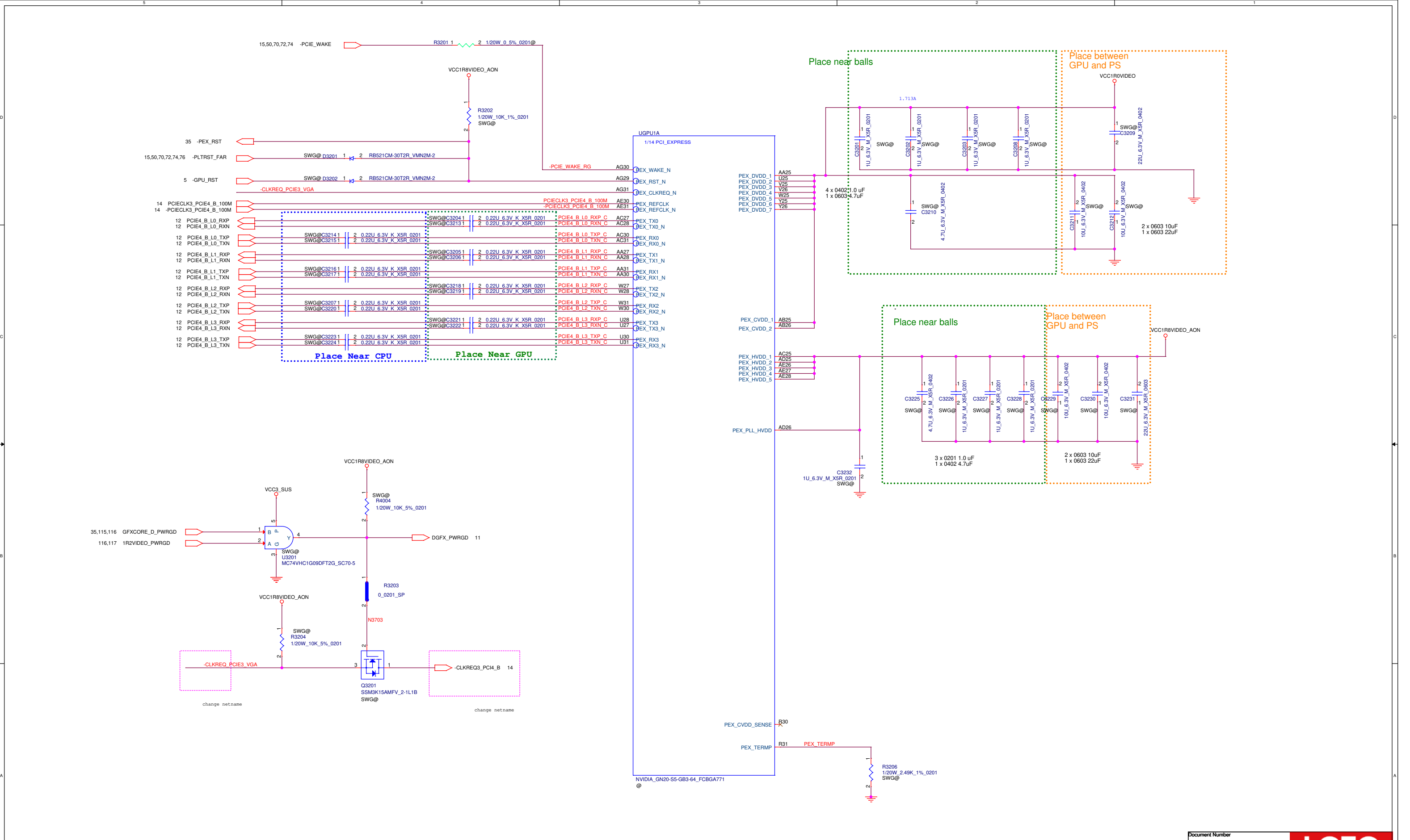


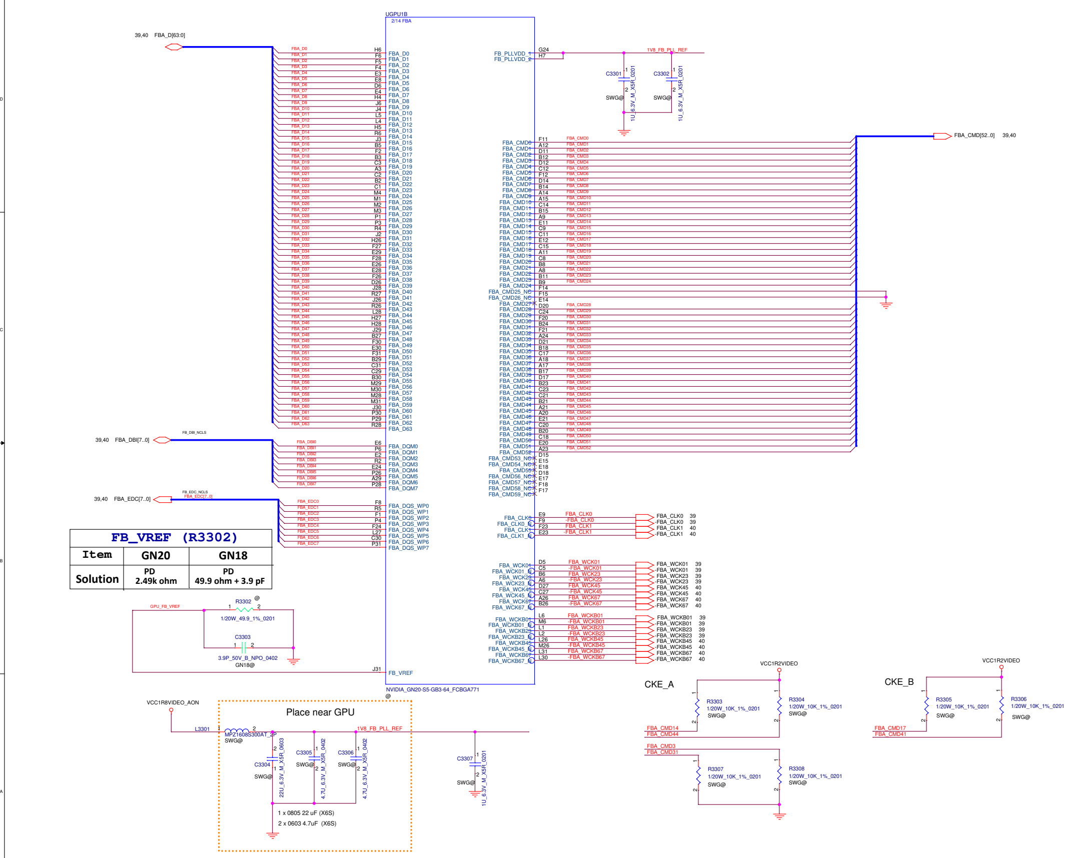
Figure 3.9 OVR-M GEN1 Reference Schematic



	OnSemi	UPI
R3121	442 Ω	332 Ω
R3125	634 Ω	475 Ω
R3113/R3119	665 Ω	499 Ω
R3103	237 KΩ	316 KΩ



Document Number		LCFC
Size: Custom	Title: 032_GN20-S5_PEG I/F	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 32 of 130	



FB_VREF (R3302)

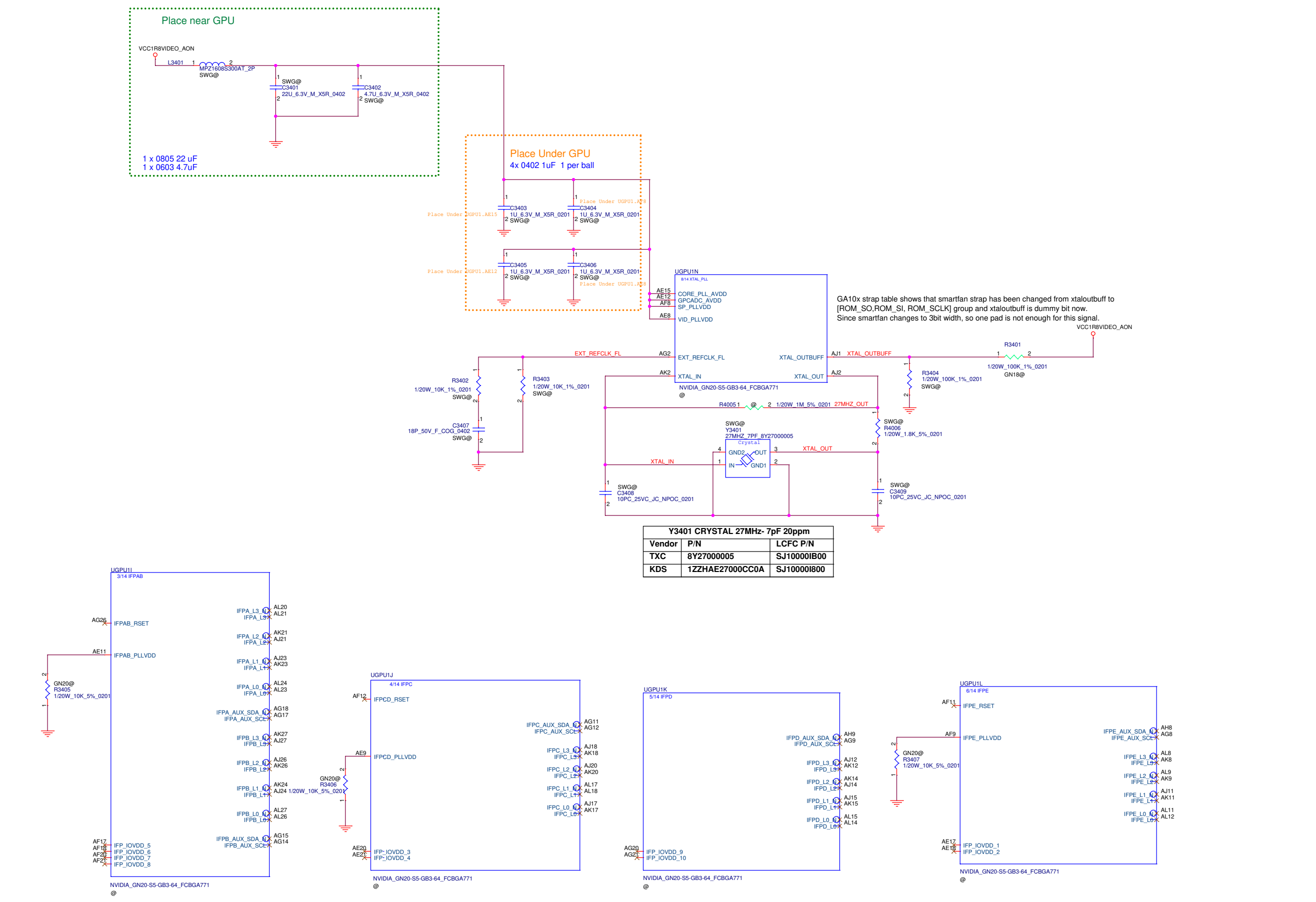
Item	GN20	GN18
Solution	PD 2.49k ohm	PD 49.9 ohm + 3.9 pF

GA1XX GDDR6 CMD Mapping

	Lower 0..31 DRAM1 CHA-Byte 0,1	Upper 32..63 DRAM2 CHA-Byte 4,5
CA0_A	CMD1	CMD33
CA1_A	CMD13	CMD45
CA2_A	CMD12	CMD35
CA3_A	CMD24	CMD46
CA4_A	CMD11	CMD36
CA5_A	CMD15	CMD43
CA6_A	CMD22	CMD48
CA7_A	CMD23	CMD47
CA8_A	CMD0	CMD34
CA9_A	CMD2	CMD32
CABI_A	CMD10	CMD37
CKE_A	CMD14	CMD44
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD5	CMD29
CA1_B	CMD18	CMD52
CA2_B	CMD7	CMD40
CA3_B	CMD20	CMD50
CA4_B	CMD8	CMD39
CA5_B	CMD16	CMD42
CA6_B	CMD21	CMD49
CA7_B	CMD19	CMD51
CA8_B	CMD6	CMD28
CA9_B	CMD4	CMD30
CABI_B	CMD9	CMD38
CKE_B	CMD17	CMD41
RESET*	CMD3	CMD31

LCFC

Document Number		
Size: Custom	Title: 033_GN20-S5 VRAM I/F	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 33 of 130	



Y3401 CRYSTAL 27MHz- 7pF 20ppm		
Vendor	P/N	LCFC P/N
TXC	8Y27000005	SJ10000IB00
KDS	1ZZHAE27000CC0A	SJ10000I800

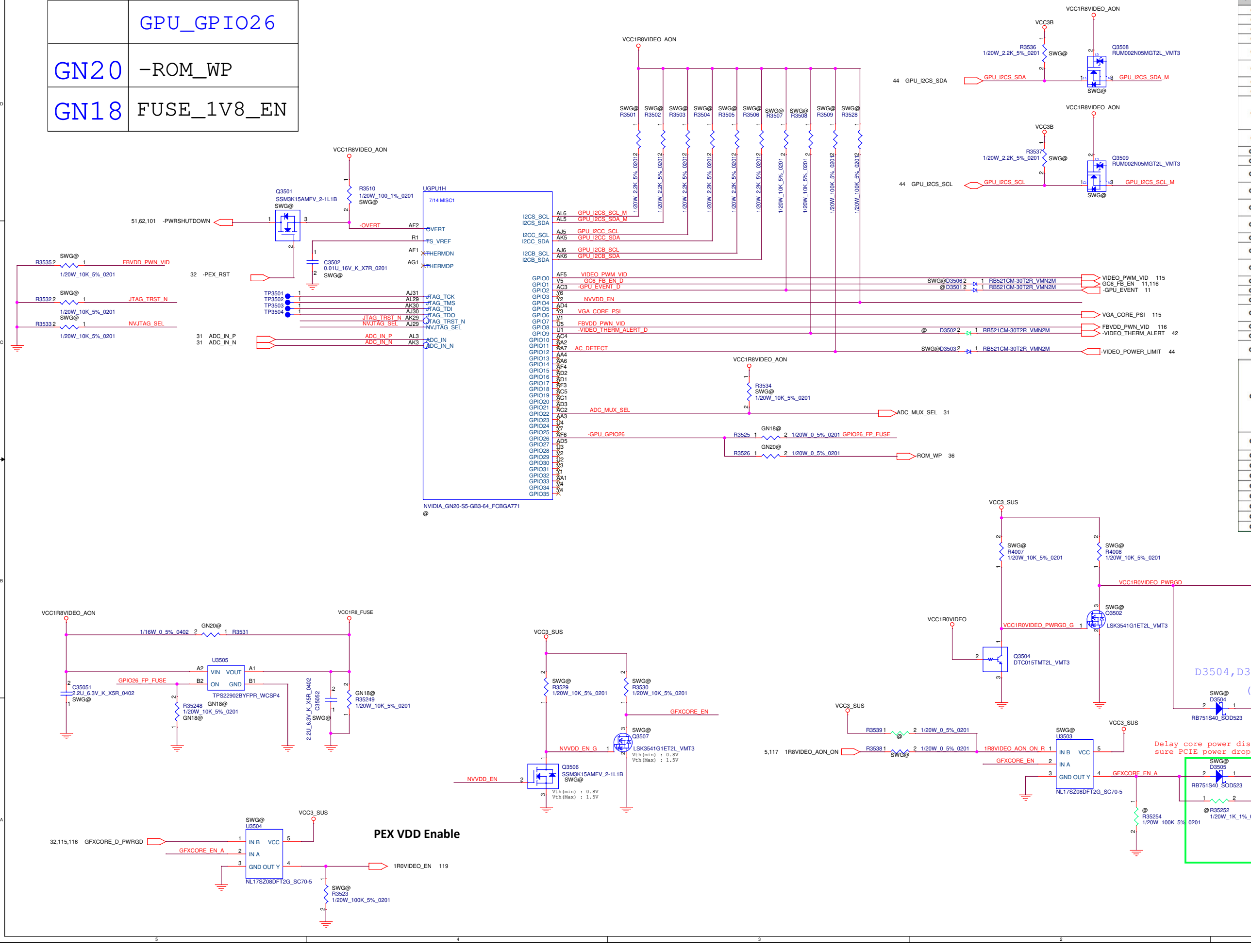
Document Number

LCFC

Size	Title	Rev
Custom	***034_GN20-S5 DIGITA / XTAL***	0.01
Date:	Wednesday, December 08, 2021 Sheet 34 of 130	

C

	GPU_GPIO26
GN20	-ROM_WP
GN18	FUSE_1V8_EN



Gpio Pin Name	GB3-64 GPIO Name	GB3B-64 GPIO Name
GPIO0	NVVDD_PWM_VID	NVVDD_PWM_VID
GPIO1	GC6_FB_EN	GC6_FB_EN
GPIO2	UNUSED	UNUSED
GPIO3	DISP_MUX_CNTL	DISP_MUX_CNTL
GPIO4	NVVDD_EN	NVVDD_EN
GPIO5	FRAME_LOCK*	FRAME_LOCK*
GPIO6	NVVDD_PSI*	NVVDD_PSI*
GPIO7	LCD_BL_PWM	LCD_BL_PWM
GPIO8	MEM_VDD_CTL	MEM_VDD_CTL
GPIO9	THERM_ALERT*	THERM_ALERT*
GPIO10	MEM_VREF_CTL	MEM_VREF_CTL
GPIO11	LCD_VDD	LCD_VDD
GPIO12	PWR_LEVEL	PWR_LEVEL
GPIO13	iGPU_BL_EN	iGPU_BL_EN
GPIO14	HPD_IFPA*	HPD_IFPA*
GPIO15	HPD_IFPB*	HPD_IFPB*
GPIO16	DISP_MUX_PWM_CNTL	DISP_MUX_PWM_CNTL
GPIO17	HPD_IFPD*	HPD_IFPD*
GPIO18	HPD_IFPE*	HPD_IFPE*
GPIO19	3D VISION/STEREO	3D VISION/STEREO
GPIO20	UNUSED	UNUSED
GPIO21	LCD_BLEN	LCD_BLEN
GPIO22	ADC_MUX_SEL	ADC_MUX_SEL
GPIO23	UNUSED	UNUSED
GPIO24	RESERVED	RESERVED
GPIO25	FBVDD_PSI*	FBVDD_PSI*
GPIO26	ROM_WP*	FP_FUSE
GPIO27	HPD_IFPC*	HPD_IFPC*
GPIO28	RESERVED	RESERVED
GPIO29	RESERVED	RESERVED
GPIO30	RESERVED	RESERVED
GPIO31	UNUSED	UNUSED
GPIO32	UNUSED	UNUSED
GPIO33	UNUSED	UNUSED
GPIO34	UNUSED	UNUSED
GPIO35	UNUSED	UNUSED

LCFC

Document Number

Title: 035_GN20-S5 GPIO

Size: Custom

Rev: 0.01

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Table 9.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

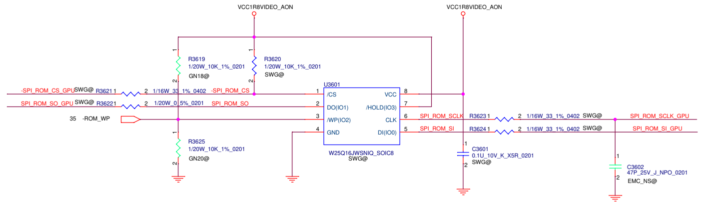
Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

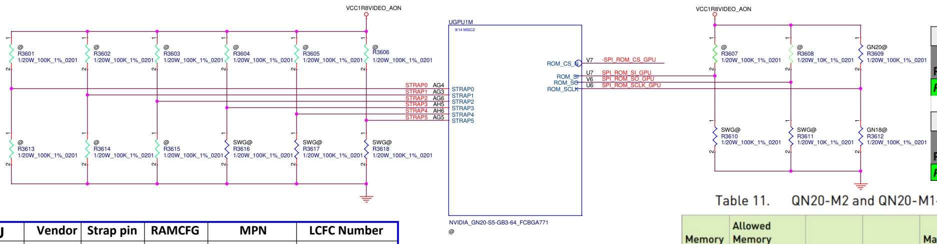
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



Provide VIA at ROM_SO close to GPU at bottom



GPU	Vendor	Strap pin	RAMCFG	MPN	LCFC Number
GN18-S5 GN20-S5	Samsung	0x0	000	K4Z80325BC-HC14	SA00009L410
	Hynix	0x2	010	H56C8H24AIR-S2C	SA0000B4E00
	Hynix	0x5	101	H56G32CS4DX005	SA0000C8K00
QN20	Samsung	0x9		K4ZAF325BM-HC14	SA00009QV20
	Hynix	TBD	TBD	TBD	TBD

Failsafe Over-Temperature Protection Strap (GB3-64/GN20-S5)				
Result	Strap Pins			FS_OVERT* Function
	ROM_SO	ROM_SI	ROM_SCLK	
Pass	L	L	H	FS_OVERT* Function ENABLE

Failsafe Over-Temperature Protection Strap (GB3B-64/GN18-S5)				
Result	Strap Pins			FS_OVERT* Function
	ROM_SO	ROM_SI	ROM_SCLK	
Pass	L	L	L	FS_OVERT* Function ENABLE

Table 11. QN20-M2 and QN20-M1-R GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
16 Gb	2Chx512Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4ZAF325BM-HC14	M-die	0x9	14 Gbps	2028	Full	Production candidate	ES or later
				TBD (new 1znm)	C-die	0xA	16 Gbps	N/A	Full	Post-production	TBD

Table 9.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)

Table 5. GN20-S5 and GN18-S5 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status	Supported GPU Milestone
8 Gb	2Chx256Mx16	1.35V 1.25V 1.2V[1]	Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001	Full	Production candidate	ES or later
			Hynix	H56C8H24AIR-S2C	A-die	0x2	14 Gbps	N/A	Full	Production candidate	QS or later
			Hynix	H56G32CS4DX005	C-die	0x5	16 Gbps	N/A	Full	Production candidate	PS or later

Notes:
[1] Refer to GN20-S and GN18-S GeForce GPU Product Spec for memory voltages and clocks.
For GN20-S5 and GN18-S5, the maximum allowable memory case temperature is 95 °C.

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Size: Custom	Title: 035_GN20-S5 GPIO	Rev: 0.01
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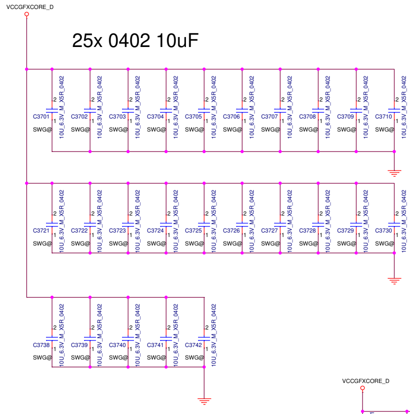
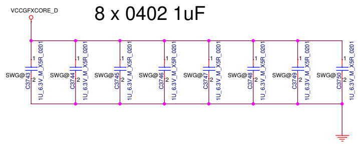
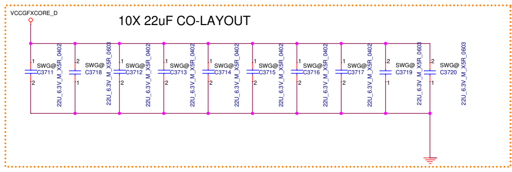
NVVDD

Under GPU





Near GPU



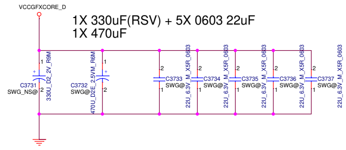
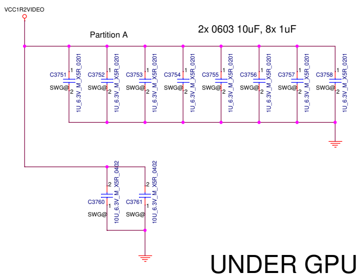


Table 3.11 GB3-64, GB3B-64 Power Rail Filtering

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU			Filtering near GPU		
			Footprint	BOM[1]	Value[2]	Footprint	BOM[1]	Value[2]
NVVDD + MSVDD (merged)	113	Varies	8 25	8 25	1uF 10uF	20 3	15 2	22uF 330uF

FBVDD

UNDER GPU



Close GPU

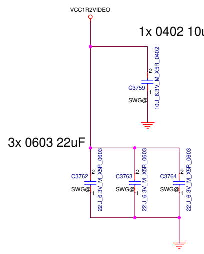
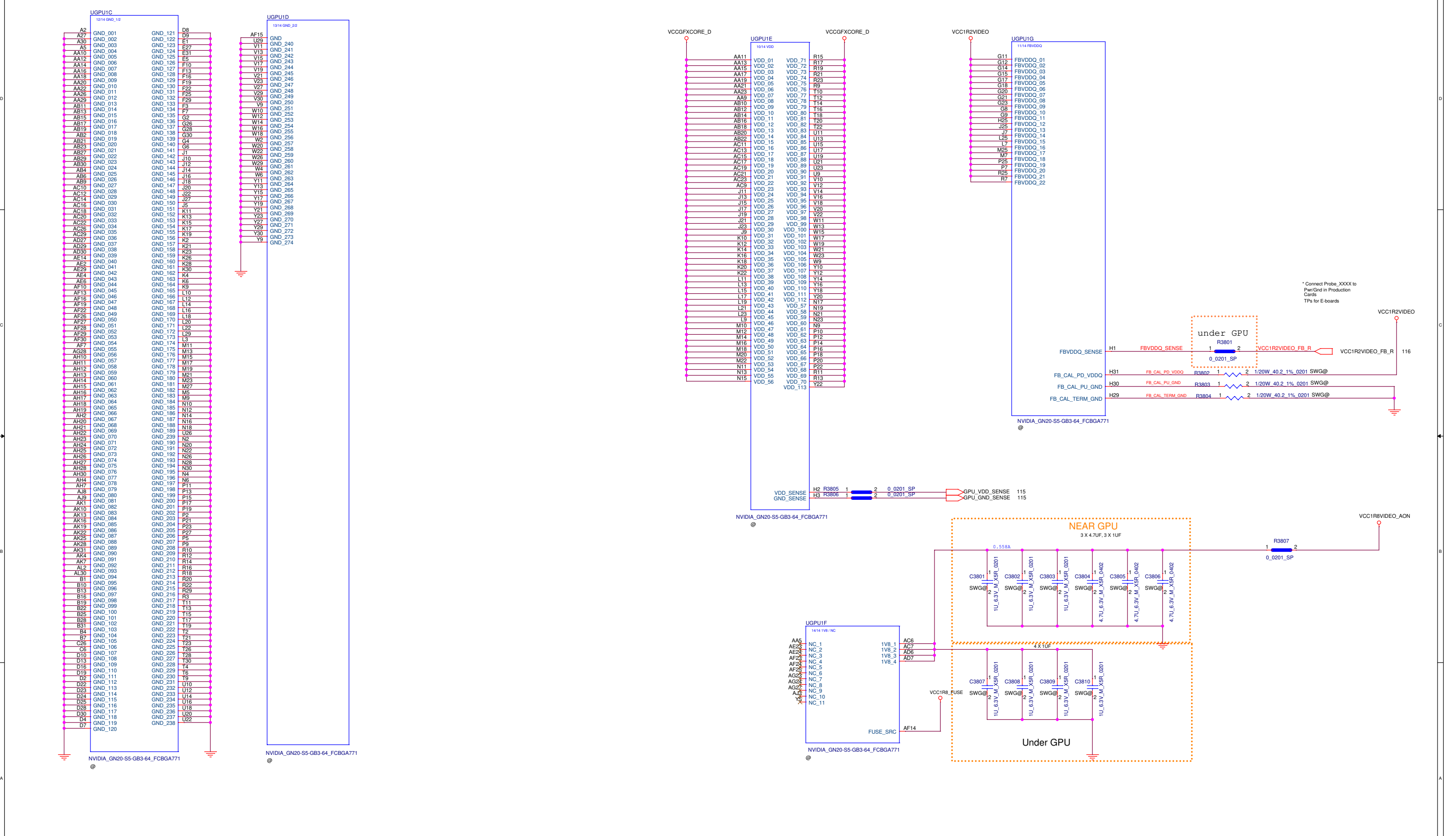


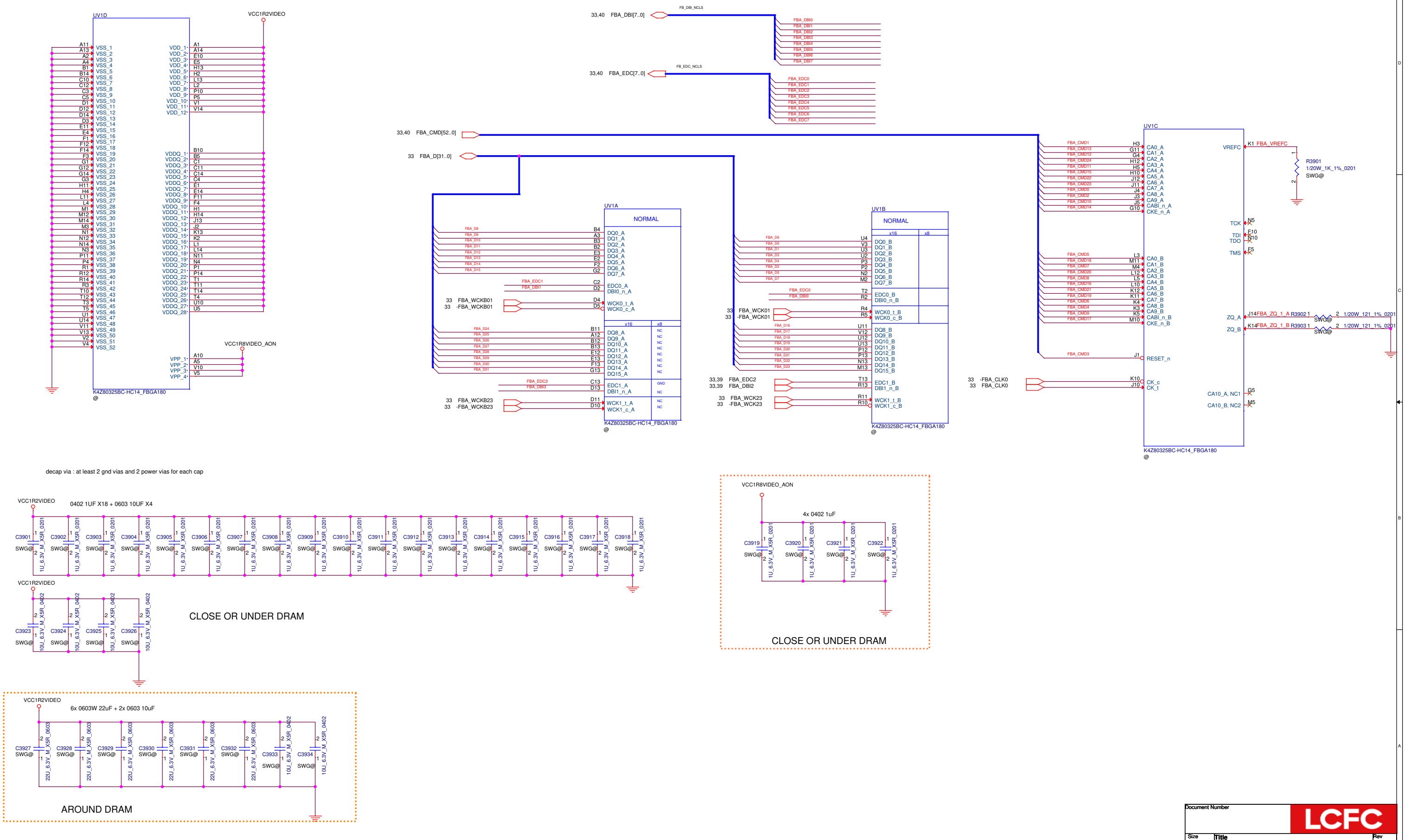
Table 3.11 GB3-64, GB3B-64 Power Rail Filtering

Rail (GPU Ball Name)	Balls	Voltage	Filtering under GPU			Filtering near GPU		
			Footprint	BOM[1]	Value[2]	Footprint	BOM[1]	Value[2]
FBVDDQ (GPU side)[1,3]	22	1.20V / 1.25V / 1.35V	8 2	8 2	1uF 10uF	1 3	1 3	10uF 22uF

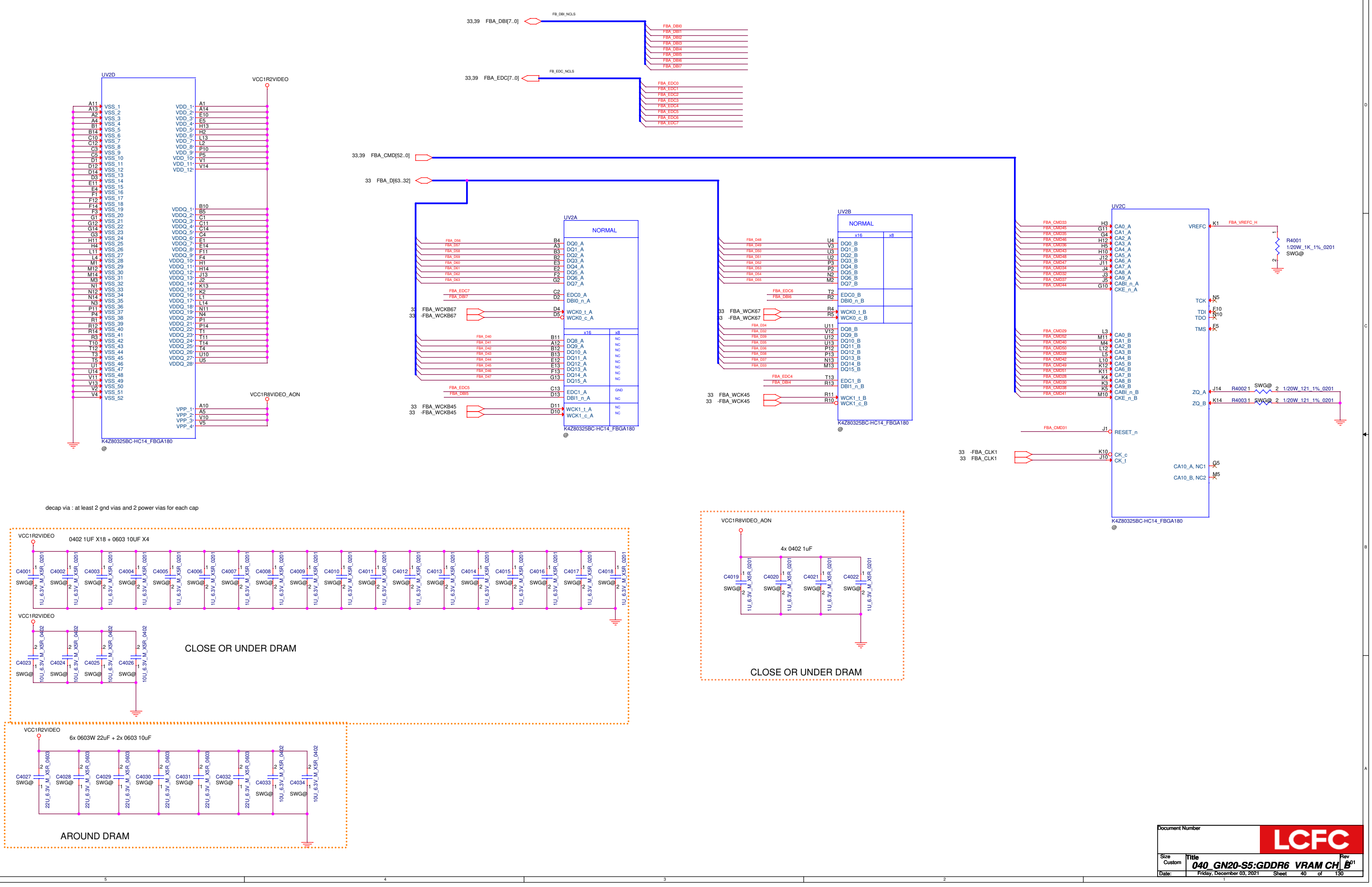
Document Number
LCFC
Title 037_GN20-S5 NVVDD & GFXCORE CAP
Size Custom
Date: Friday, December 03, 2021 Sheet 37 of 130



Document Number	LCFC
Size: Custom	Title: 038_GN20-S5 GND
Rev	0.01
Date: Friday, December 03, 2021	Sheet 38 of 130



Document Number			
Size Custom	Title 039_GN20-S5:GDDR6 VRAM CH_A		Rev 0.01
Date:	Friday, December 03, 2021	Sheet 39 of 130	



Document Number	LCFC
Size: Custom	Title: 040_GN20-S5:GDDR6 VRAM CH_B
Rev	0.01
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Document Number		LCFC
Size Custom	Title 041_BLANK	Rev 0.01
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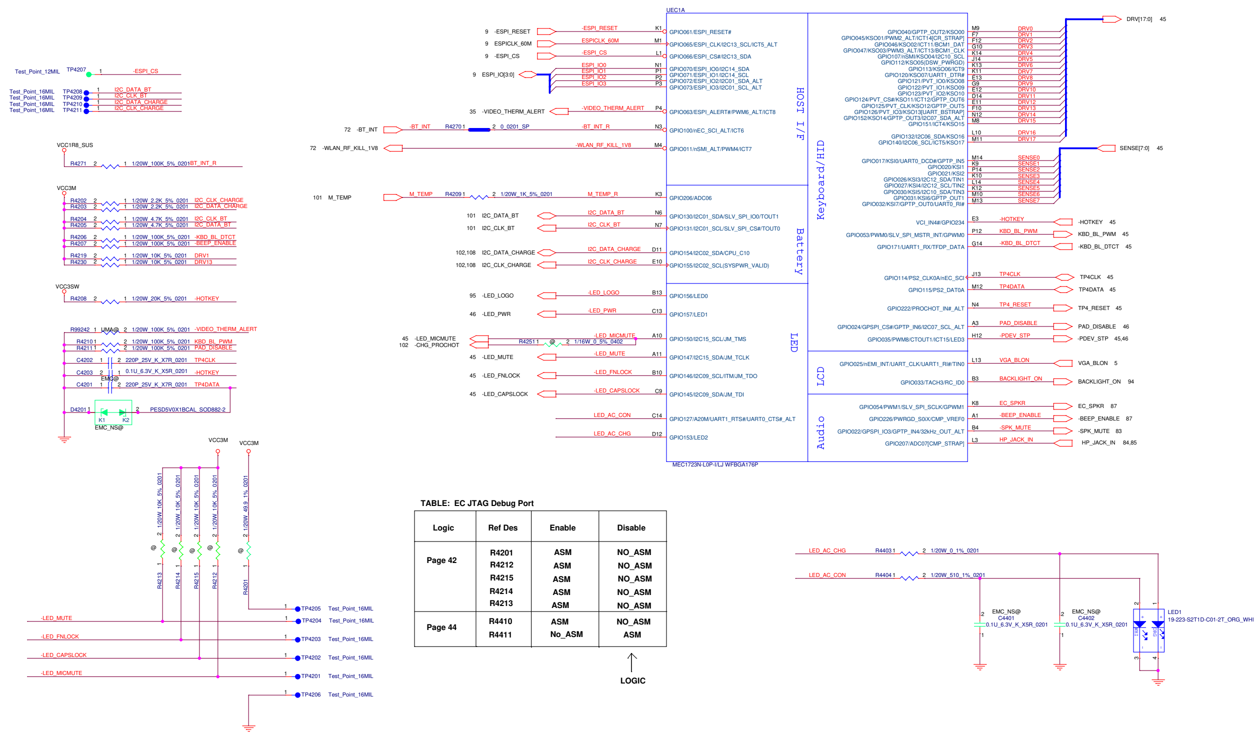

TABLE: EC JTAG Debug Port

Logic	Ref Des	Enable	Disable
Page 42	R4201	ASM	NO_ASM
	R4212	ASM	NO_ASM
	R4215	ASM	NO_ASM
	R4214	ASM	NO_ASM
	R4213	ASM	NO_ASM
Page 44	R4410	ASM	NO_ASM
	R4411	No_ASM	ASM

LOGIC

TABLE: Functional Strap

KSO01(Crisis Recovery over keyscan conn) CR STRAP	
HIGH	Normal Boot
LOW	Crash Recovery

LOGIC

KSO13(Crisis Recovery over UART) UARTB STRAP	
HIGH	Normal Operation
LOW	Use UARTinterface for Crisis recovery

LOGIC

GPIO207(Comparator 0 Strap pin) [only 144pin package] must be enabled in OTP. CMP STRAP	
HIGH	Comparator 0 Enabled.
LOW	Hardware Default (GPIO input)

LCFC

Document Number		
Size: Custom	Title: 042_MEC1723(1/3)	Rev: 0.01
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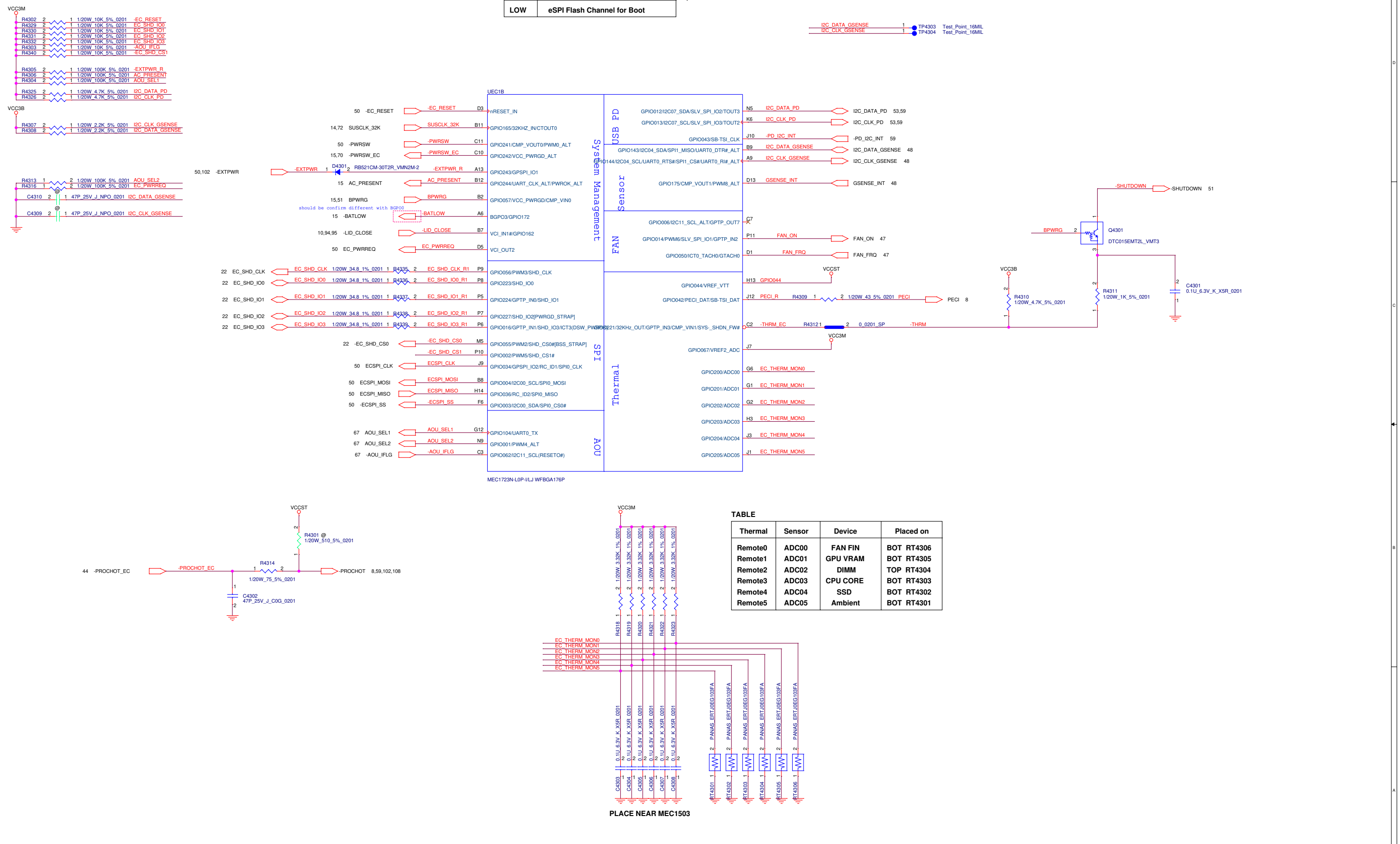
TABLE : Functional Strap

GPIO055 (Boot Source Select Starp)	
HIGH	Shared SPI pins for Boot
LOW	eSPI Flash Channel for Boot

LOGIC

GPIO227 (PWRGD Starp)



TABLE

Thermal	Sensor	Device	Placed on
Remote0	ADC00	FAN FIN	BOT RT4306
Remote1	ADC01	GPU VRAM	BOT RT4305
Remote2	ADC02	DIMM	TOP RT4304
Remote3	ADC03	CPU CORE	BOT RT4303
Remote4	ADC04	SSD	BOT RT4302
Remote5	ADC05	Ambient	BOT RT4301

Document Number			LCFC
Size Custom	Title 043_MEC1723(2/3)		Rev 0.01
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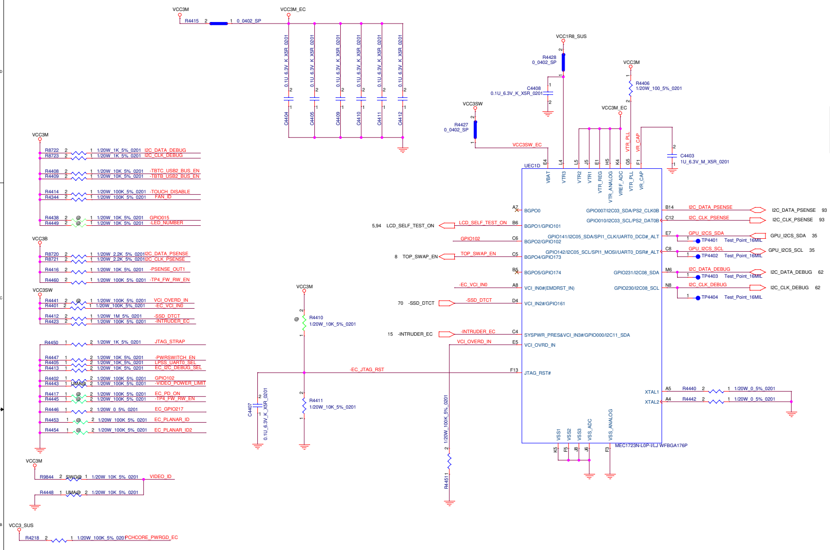


TABLE:EC PLANAR ID (GPIO111)

LEVEL	EC_PLANAR_ID
EVT,FVT	HIGH
SIT,and later	LOW

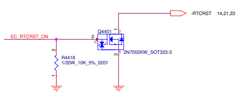
TABLE:EC PLANAR ID2 (GPIO211)

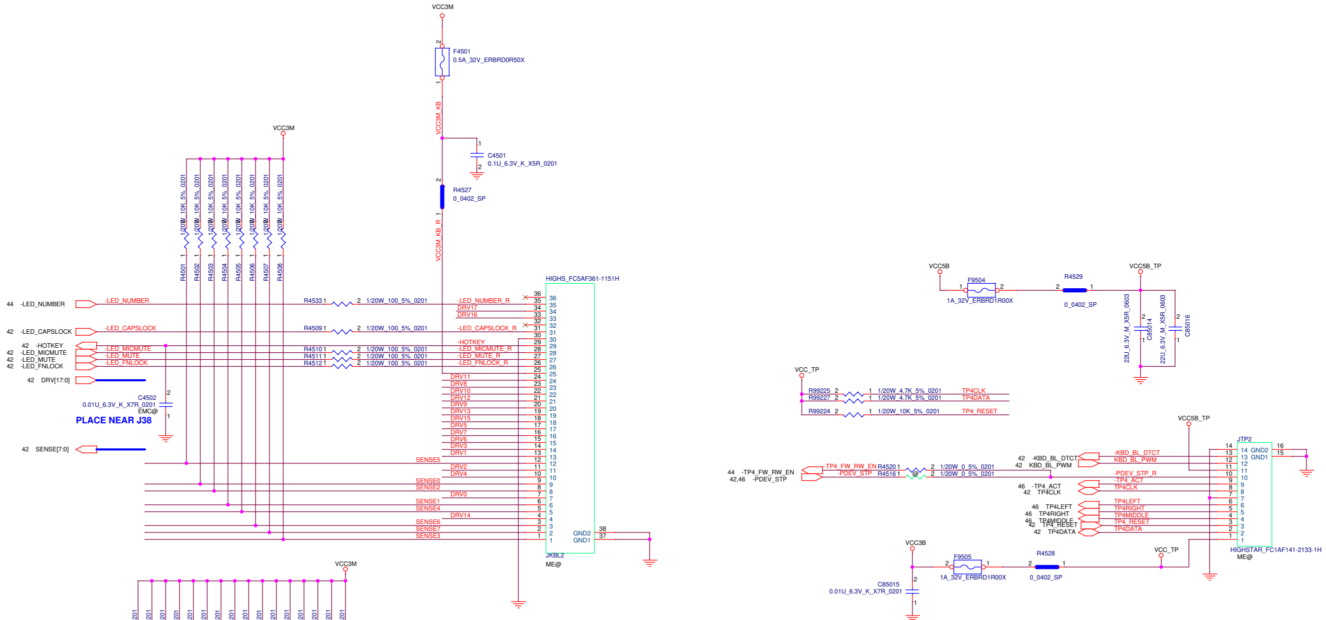
LEVEL	EC_PLANAR_ID2
EVT~SIT	HIGH
SIT-R and later	LOW

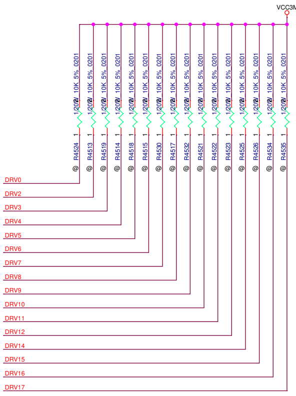
FAN_ID(GPIO207)

T14 Drift3.0	
Supplier	ID
AVC	High(2)_3.2v
Toshiba	Middle(1)_1.65v
DELTA	Low(0)_0v

Ironhide3.0	
Supplier	ID
AVC	High(2)_3.2v
Toshiba	Middle(1)_1.65v
DELTA	Low(0)_0v







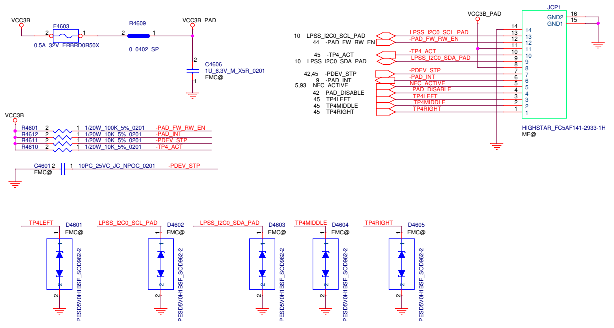
Num

Pin #	Case A
1	SENSE3
2	SENSE7
3	SENSE6
4	DRV14
5	SENSE4
6	SENSE1
7	DRV0
8	SENSE2
9	SENSE0
10	DRV4
11	DRV2
12	SENSE5
13	DRV1
14	DRV3
15	DRV6
16	DRV7
17	DRV5
18	DRV15
19	DRV13
20	DRV9
21	DRV12
22	DRV10
23	DRV8
24	DRV11
25	Vcc
26	LED1
27	LED2
28	LED3
29	HOTKEY
30	GND
31	LED4
32	NC
33	DRV16
34	DRV17
35	LED5
36	NC

Assign	Purpose
Vcc	Vcc 3V for LED
LED1	LED for Esc
LED2	LED for F1
LED3	LED for F4
LED4	LED for CapsLock
LED5	LED for NumLock

TrackPoint Cable Pin assignment

Pin #	Assign
1	VCC (3.3V)
2	IPD DATA
3	IPD RST
4	MIDDLE
5	RIGHT
6	LEFT
7	IPD GND
8	IPD CLK
9	-TP4_ACT
10	-TP4_FW_RW_EN
11	LED VCC5 (5V)
12	LED PWM
13	Backlight detection
14	LED GND



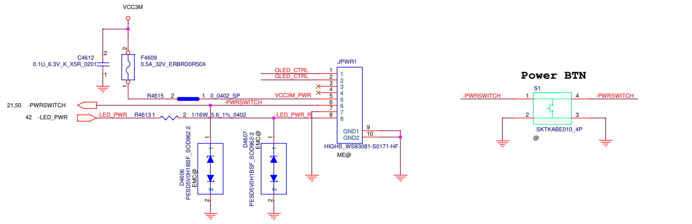
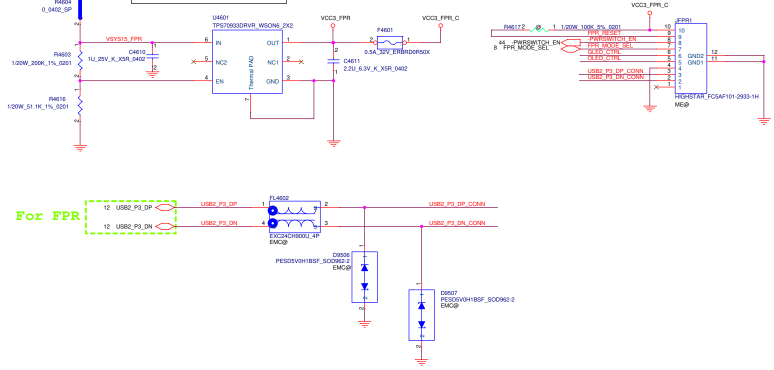


Table U4601

LDO_2 x 2mm WSON(6)	
TI	TPS70933DRVR
OnSemi	NCP730BMT330TBG



5/20 change pin define for click pad spec change

Connector to planer

Name	Pin#	Type	Function
GND	1	Power	Signal Ground
I2C_CLK	2	IN/OUT	I2C Clock to System I2C I/F on CPU/PCH
-PAD_FW_RW_EN	3	IN	Enable FW update.
VDDIO	4	Power	IO power.
-TP4_ACT	5	IN	TrackPoint Activity status. Please refer to “4.2.8”
I2C_DAT	6	IN/OUT	I2C Data to System I2C I/F on CPU/PCH
V_{DD}	7	Power	Supply power from system. Power is not supplied when system is in S3, S4, S5 and G5 state. (Refer to electrical requirement)
- PDEV_STP	8	IN	This signal is used to disable to report button status and finger status to system when system LCD lid is closed or is in Tent /Stand /Tablet modes (Yoga case). Please refer to “4.2.6-PDEV_STP”
-I2C_INT	9	OUT	Interrupt for I2C communication
NFC_Active	10	IN	This signal should use if NFC Antenna is implemented under touch pad PCBA. This signal should be NC or not be used in touch pad PCBA if NFC antenna is not implemented under touch pad PCBA. Please refer to “4.2.7 NFC_Active”
PAD_DISABLE	11	IN	This signal is used to disable touch pad. Please refer to “4.2.5 PAD_DISABLE”.
TP4LEFT	12	OUT	TrackPoint button signal
TP4MIDDLE	13	OUT	TrackPoint button signal
TP4RIGHT	14	OUT	TrackPoint button signal

Document Number

LCFC

Size: Custom

Title: 046_TOUCH PAD/FPR POINT/PWR BTN

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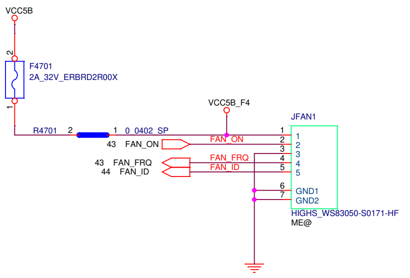

Document Number		LCFC
Size: Custom	Title: **047_FAN CONNECTOR**	Rev: 0.01
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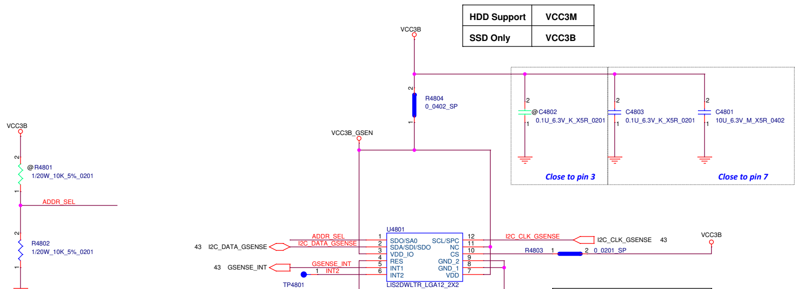
TABLE : G-Sensor Power

HDD Support	VCC3M
SSD Only	VCC3B



R4803				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

TABLE : U4801

P/N	ADDR_SEL	Address
LIS2DWLTR	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX022-1020	H L	
BMA422	H L	32h (W) & 33h (R) 30h (W) & 31h (R)

ST and Bosch I2C address is same but can be identified by Chip_ID

TABLE of G-Sensor (U4801)		
Vendor	P/N	LCFC P/N
ST	LIS2DWLTR	SA00009AQ00
Kionix	KX022-1020	SA000081E00
BOSCH	BMA422	SA0000C1V00

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Size Custom	Title 048_APS G-SENSOR	Rev 0.01
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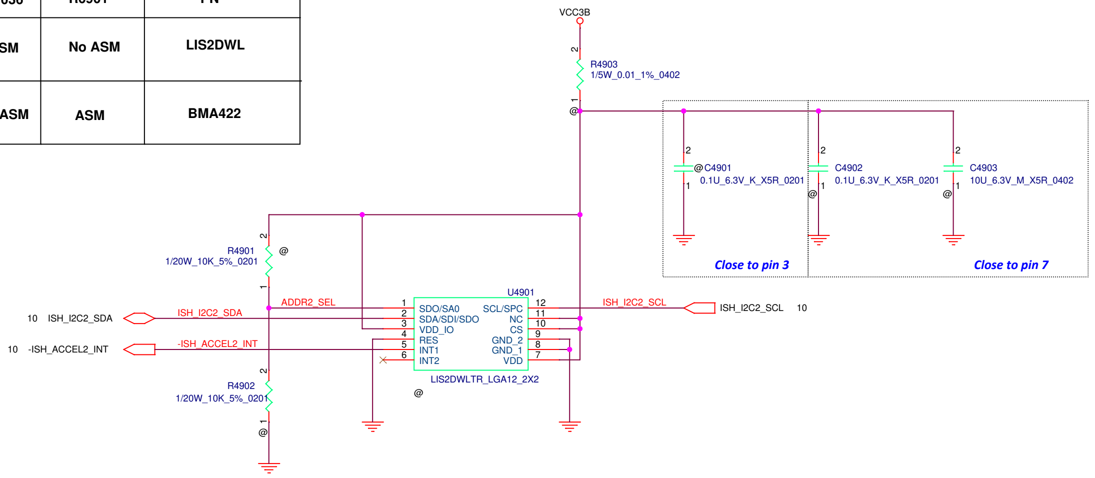
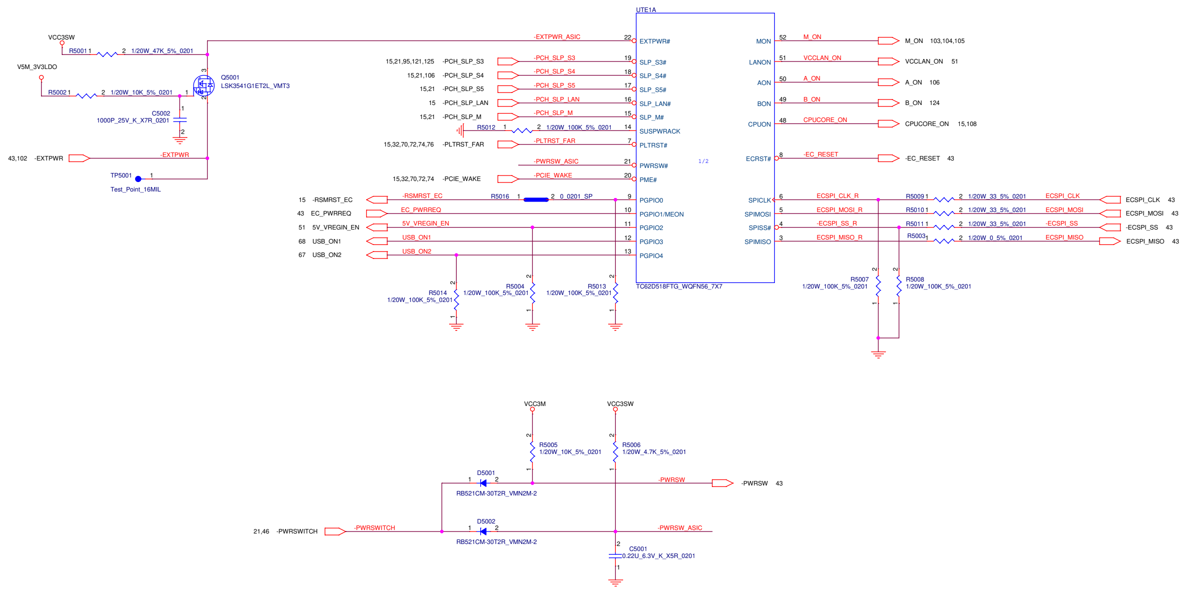
TABLE

SDO	I2C Address	R1036	R6901	PN
L	30h (W) & 31h (R)	ASM	No ASM	LIS2DWL
H	TBD	No ASM	ASM	BMA422



Document Number	LCFC
Size B	Title 049_HPD G-SENSOR	Rev 0.01
Date: Friday, December 03, 2021	Sheet 49 of 130



Document Number	
Size: Custom	Title: **050_THINK ENGINE-3(1/2)**
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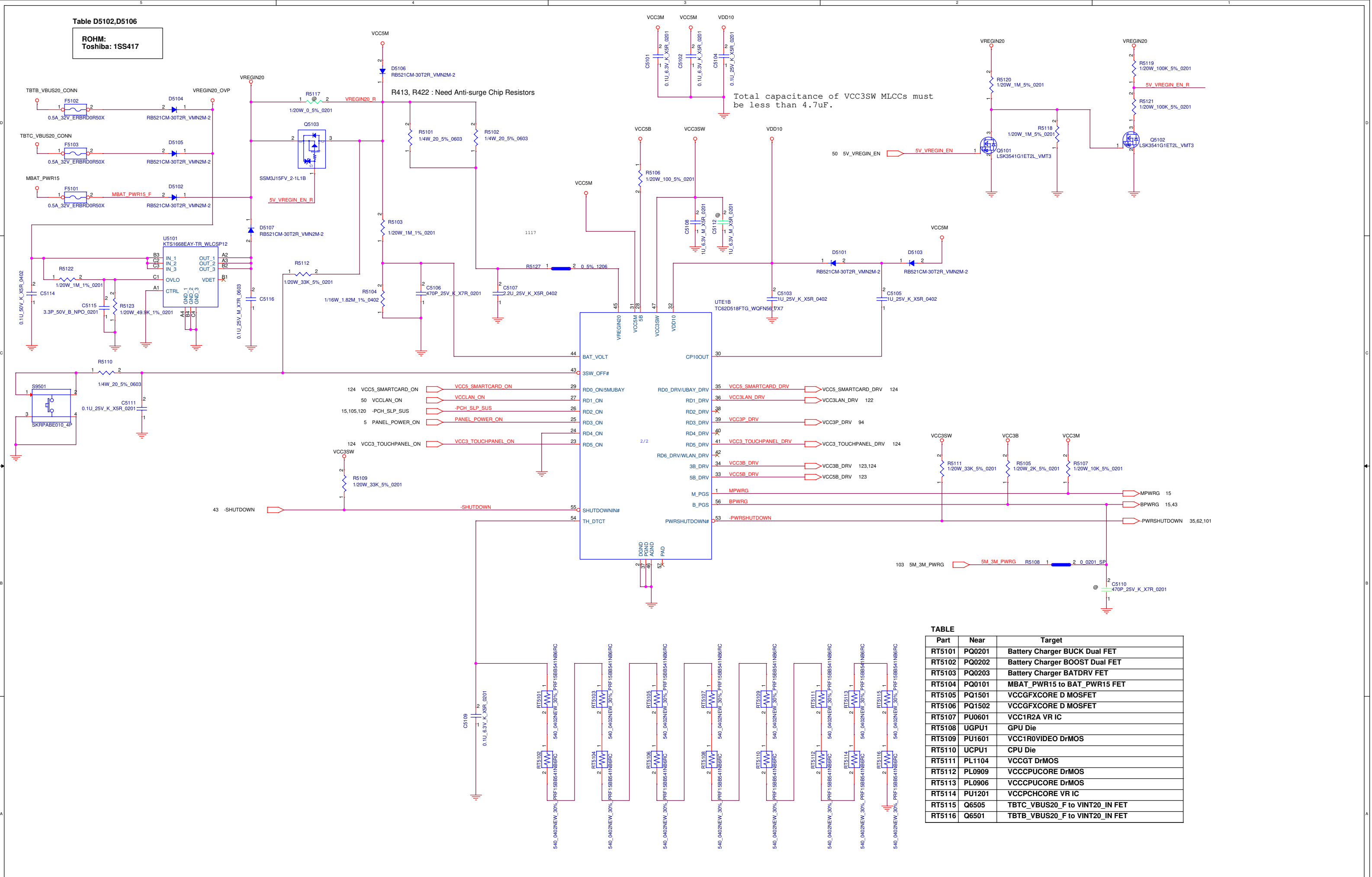
LCFC



TABLE

Part	Near	Target
RT5101	PQ0201	Battery Charger BUCK Dual FET
RT5102	PQ0202	Battery Charger BOOST Dual FET
RT5103	PQ0203	Battery Charger BATDRV FET
RT5104	PQ0101	MBAT_PWR15 to BAT_PWR15 FET
RT5105	PQ1501	VCCGFXCORE D MOSFET
RT5106	PQ1502	VCCGFXCORE D MOSFET
RT5107	PU0601	VCC1R2A VR IC
RT5108	UGPU1	GPU Die
RT5109	PU1601	VCC1R0VIDEO DrMOS
RT5110	UCPU1	CPU Die
RT5111	PL1104	VCCGT DrMOS
RT5112	PL0909	VCCCPUCORE DrMOS
RT5113	PL0906	VCCCPUCORE DrMOS
RT5114	PU1201	VCCPCHCORE VR IC
RT5115	Q6505	TBTC_VBUS20_F to VINT20_IN FET
RT5116	Q6501	TBTB_VBUS20_F to VINT20_IN FET

Document Number

LCFC

Size: Custom
Title: 051_ THINK ENGINE-3(2/2)
Rev: 0.01
Date: Wednesday, December 08, 2021 Sheet 51 of 130

Document Number		LCFC
Size Custom	Title 052_BLANK	Rev 0.01
Date:	Friday, December 03, 2021 Sheet 52 of 130	

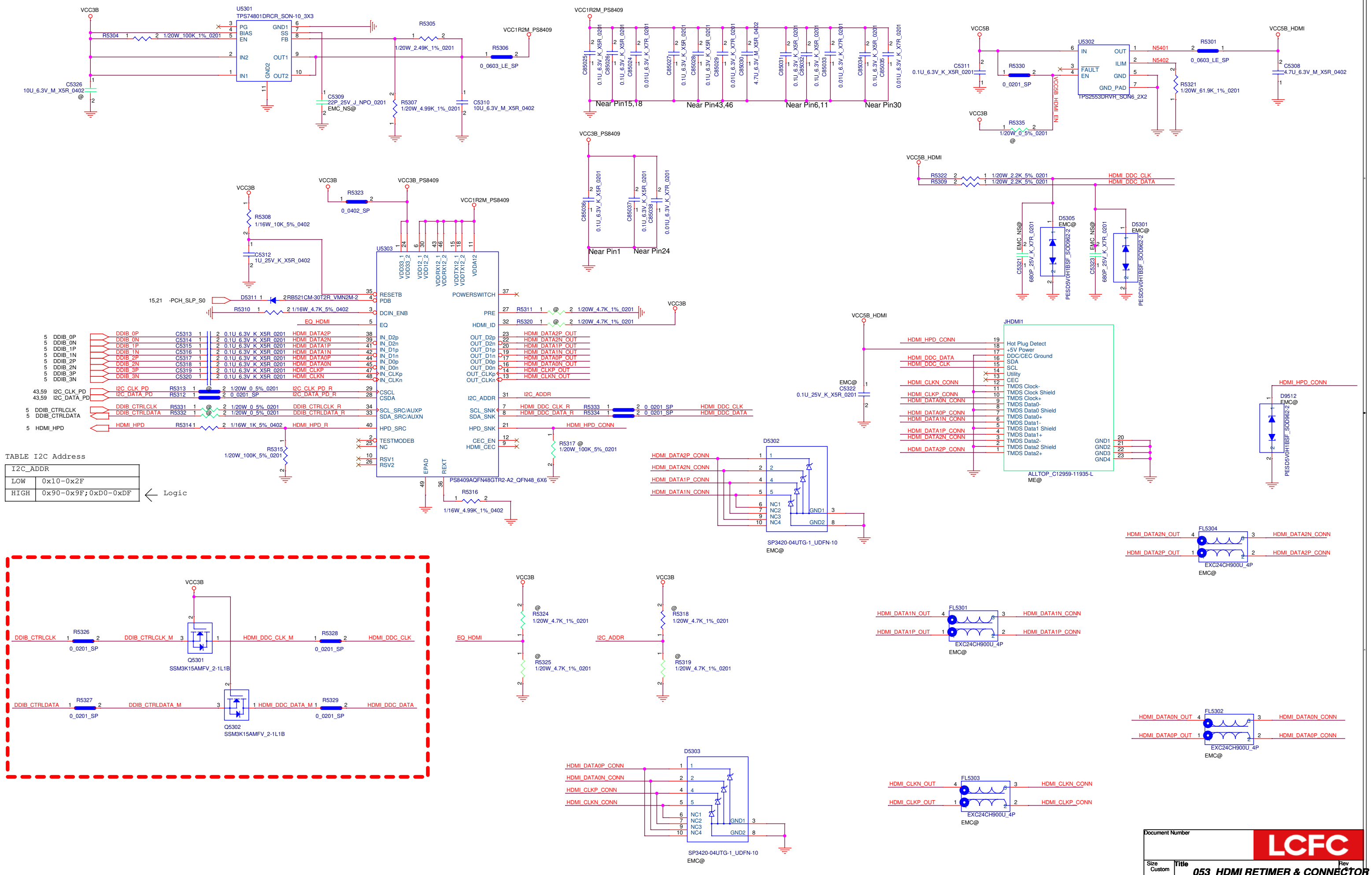


TABLE I2C Address

I2C_ADDR	
LOW	0x10-0x2F
HIGH	0x90-0x9F;0xD0-0xDF

Logic

Document Number

LCFC

Size Custom

Title 053_HDMI RETIMER & CONNECTOR

Rev

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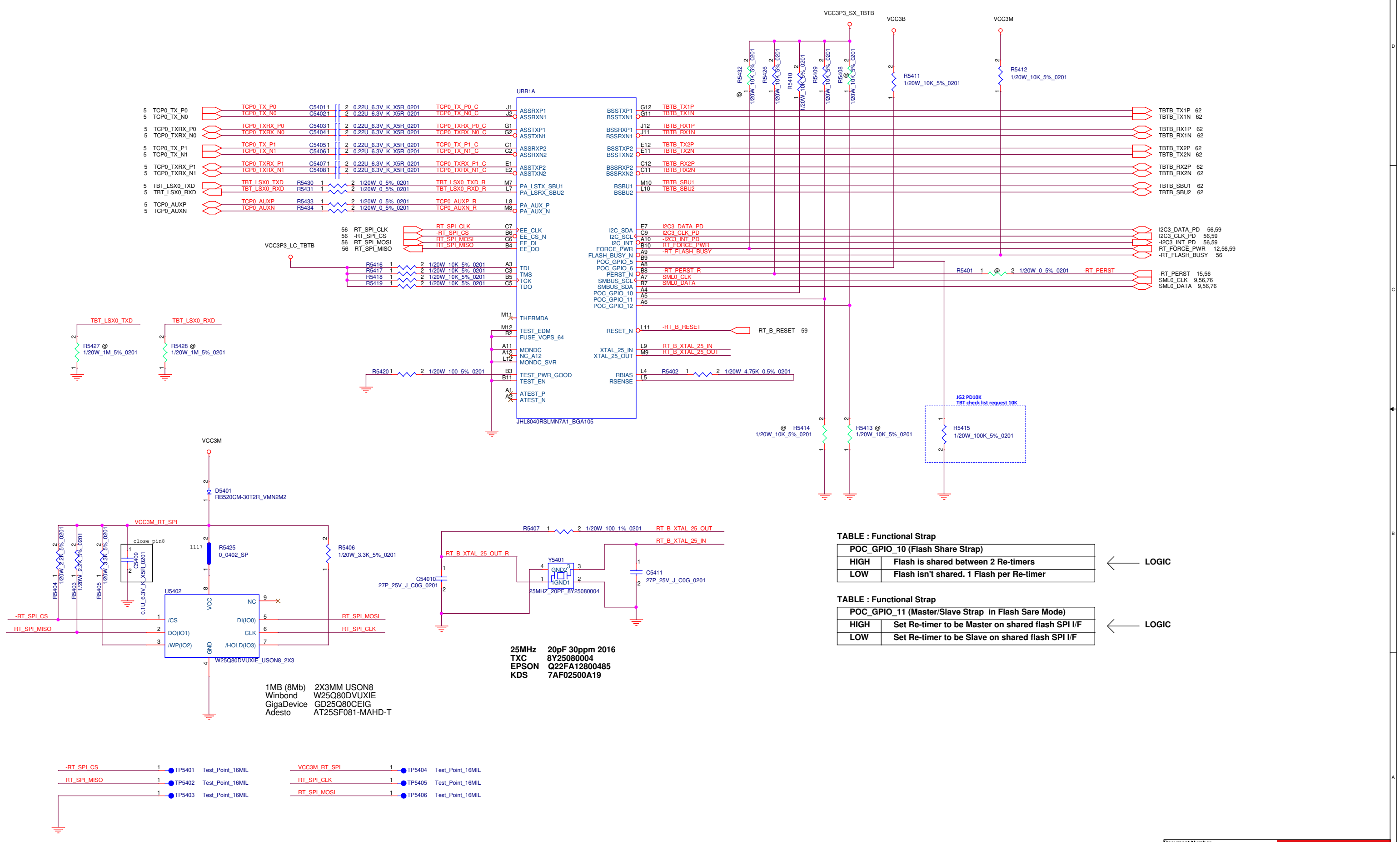

TABLE : Functional Strap

POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

LOGIC

Document Number

LCFC

Size Custom

Title **054_THUNDERBOLT RETIMER B (1/2)**

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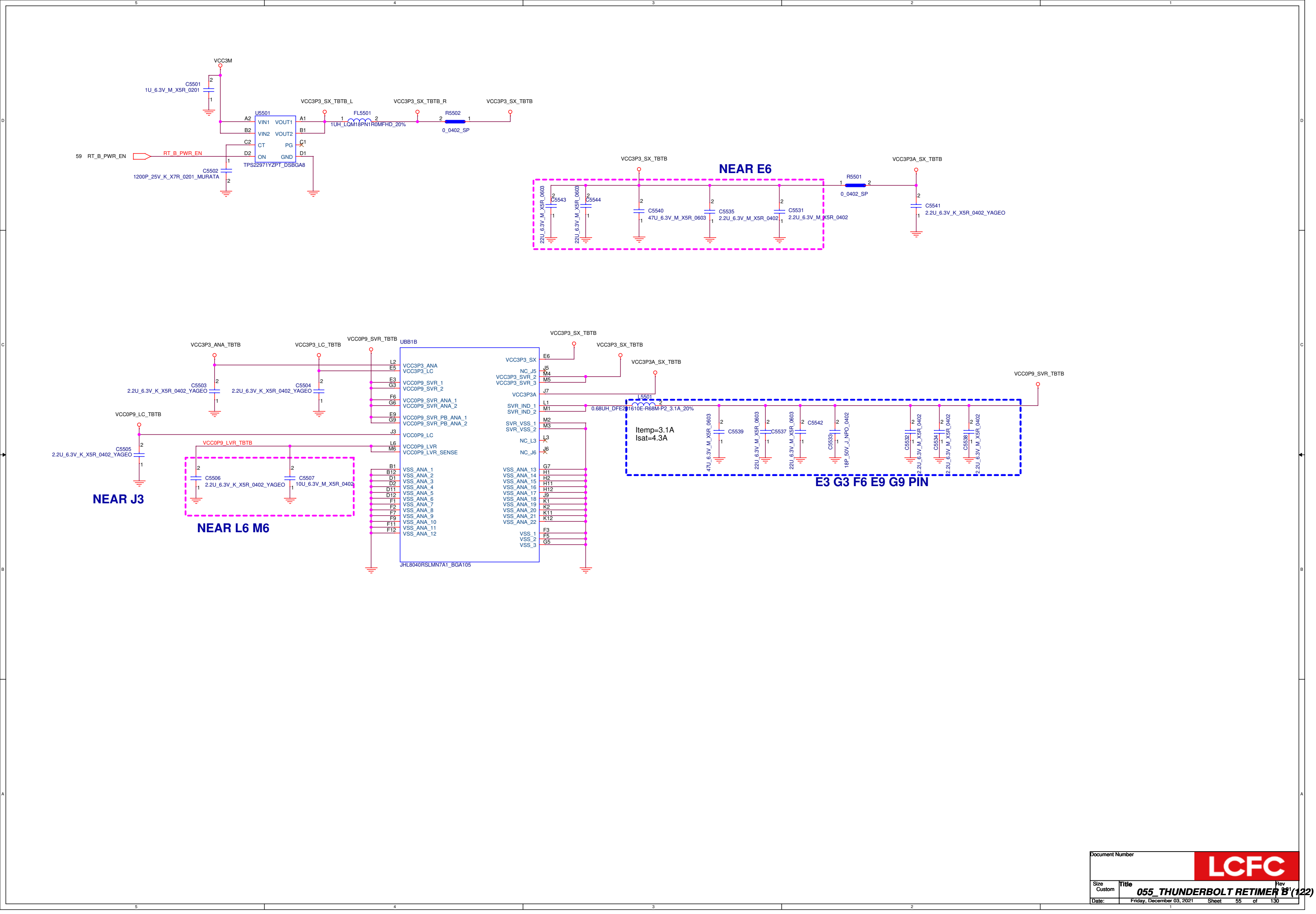
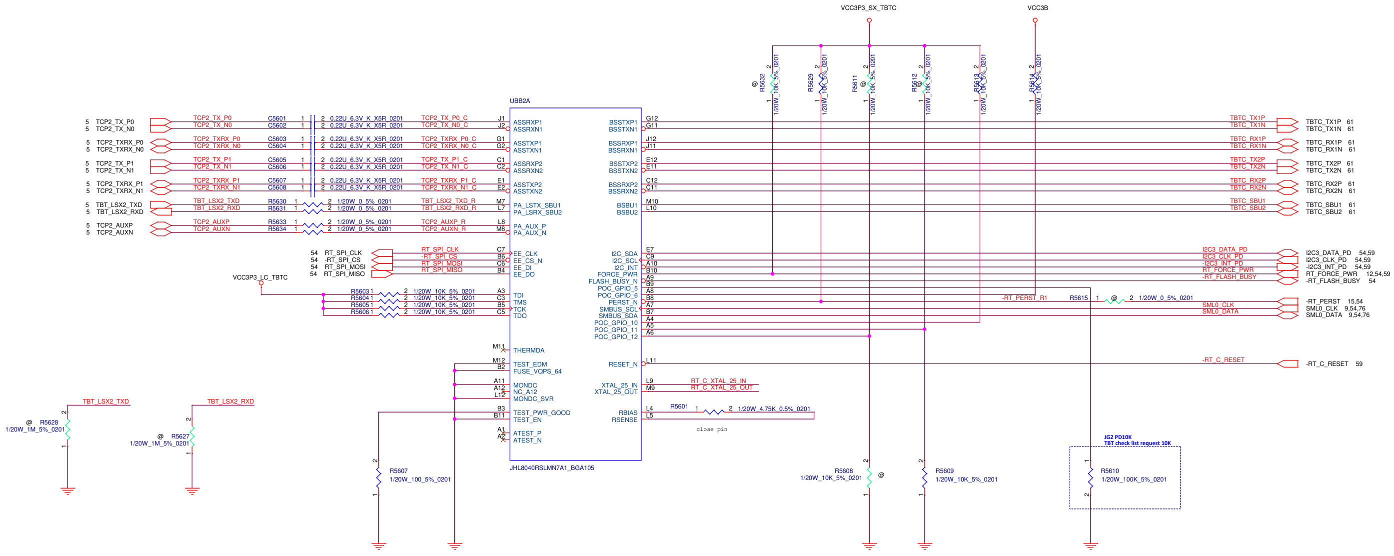
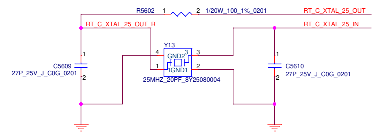

VCC3M
C5501
1U_6.3V_M_X5R_0201
U5501
VIN1
VIN2
CT
ON
VOUT1
VOUT2
PG
GND
TPS22971YZPT_DSBGA8
C5502
1200P_25V_K_X7R_0201_MURATA
59 RT_B_PWR_EN
RT_B_PWR_EN
VCC3P3_SX_TBTB_L
FL5501
1UH_LQM18PN1R0MFHD_20%
VCC3P3_SX_TBTB_R
R5502
0_0402_SP
VCC3P3_SX_TBTB
NEAR E6
C5543
C5544
22U_6.3V_M_X5R_0603
C5540
47U_6.3V_M_X5R_0603
C5535
2.2U_6.3V_M_X5R_0402
C5531
2.2U_6.3V_M_X5R_0402
R5501
0_0402_SP
VCC3P3A_SX_TBTB
C5541
2.2U_6.3V_K_X5R_0402_YAGEO
VCC3P3_ANA_TBTB
VCC3P3_LC_TBTB
VCC0P9_SVR_TBTB
C5503
2.2U_6.3V_K_X5R_0402_YAGEO
C5504
2.2U_6.3V_K_X5R_0402_YAGEO
VCC0P9_LC_TBTB
C5505
2.2U_6.3V_K_X5R_0402_YAGEO
VCC0P9_LVR_TBTB
C5506
2.2U_6.3V_K_X5R_0402_YAGEO
C5507
10U_6.3V_M_X5R_0402
NEAR J3
NEAR L6 M6
UBB1B
VCC3P3_ANA
VCC3P3_LC
VCC0P9_SVR_1
VCC0P9_SVR_2
VCC0P9_SVR_ANA_1
VCC0P9_SVR_ANA_2
VCC0P9_SVR_PB_ANA_1
VCC0P9_SVR_PB_ANA_2
VCC0P9_LC
VCC0P9_LVR
VCC0P9_LVR_SENSE
VSS_ANA_1 … VSS_ANA_12
VCC3P3_SX
NC_J5
VCC3P3_SVR_2
VCC3P3_SVR_3
VCC3P3A
SVR_IND_1
SVR_IND_2
SVR_VSS_1
SVR_VSS_2
NC_L3
NC_J6
VSS_ANA_13 … VSS_ANA_22
VSS_1
VSS_2
VSS_3
JHL8040RSLMN7A1_BGA105
L5501
0.68UH_DFE201610E-R68M-P2_3.1A_20%
Itemp=3.1A
Isat=4.3A
C5539
47U_6.3V_M_X5R_0603
C5537
22U_6.3V_M_X5R_0603
C5542
22U_6.3V_M_X5R_0603
C5533
18P_50V_J_NPO_0402
C5532
C5534
C5536
2.2U_6.3V_M_X5R_0402
VCC0P9_SVR_TBTB
E3 G3 F6 E9 G9 PIN
Document Number
LCFC
Size Custom
Title
055_THUNDERBOLT RETIMER B (122)
Rev
Date: Friday, December 03, 2021
Sheet 55 of 130





25MHz **20pF 30ppm 2016**
TXC **8Y25080004**
EPSON **Q22FA12800485**
KDS **7AF02500A19**

TABLE : Functional Strap

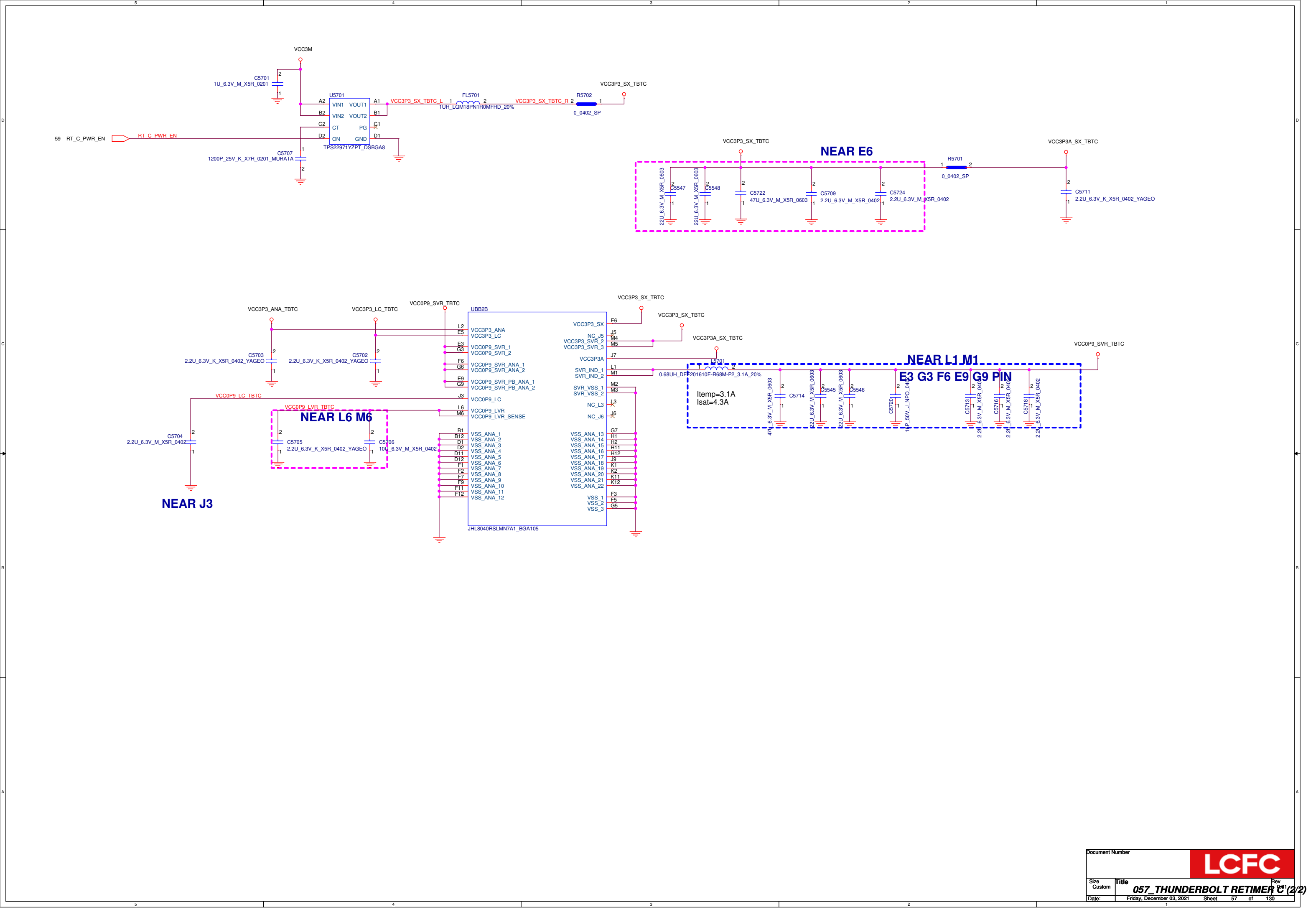
POC_GPIO_10 (Flash Share Strap)	
HIGH	Flash is shared between 2 Re-timers
LOW	Flash isn't shared. 1 Flash per Re-timer

LOGIC

TABLE : Functional Strap

POC_GPIO_11 (Master/Slave Strap in Flash Sare Mode)	
HIGH	Set Re-timer to be Master on shared flash SPI I/F
LOW	Set Re-timer to be Slave on shared flash SPI I/F

LOGIC


VCC3M
U5701
TPS22971YZPT_DSBGA8
FL5701
1UH_LQM18PN1R0MFHD_20%
R5702
0_0402_SP
VCC3P3_SX_TBTC
RT_C_PWR_EN
VCC3P3_SX_TBTC_L
VCC3P3_SX_TBTC_R
NEAR E6
R5701
VCC3P3A_SX_TBTC
UBB2B
JHL8040RSLMN7A1_BGA105
VCC3P3_ANA_TBTC
VCC3P3_LC_TBTC
VCC0P9_SVR_TBTC
VCC0P9_LC_TBTC
VCC0P9_LVR_TBTC
NEAR L6 M6
NEAR J3
L5701
0.68UH_DFE201610E-R68M-P2_3.1A_20%
Itemp=3.1A
Isat=4.3A
NEAR L1 M1
E3 G3 F6 E9 G9 PIN
LCFC
Document Number
Title
057_THUNDERBOLT RETIMER C (2/2)
Size Custom
Date: Friday, December 03, 2021
Sheet 57 of 130

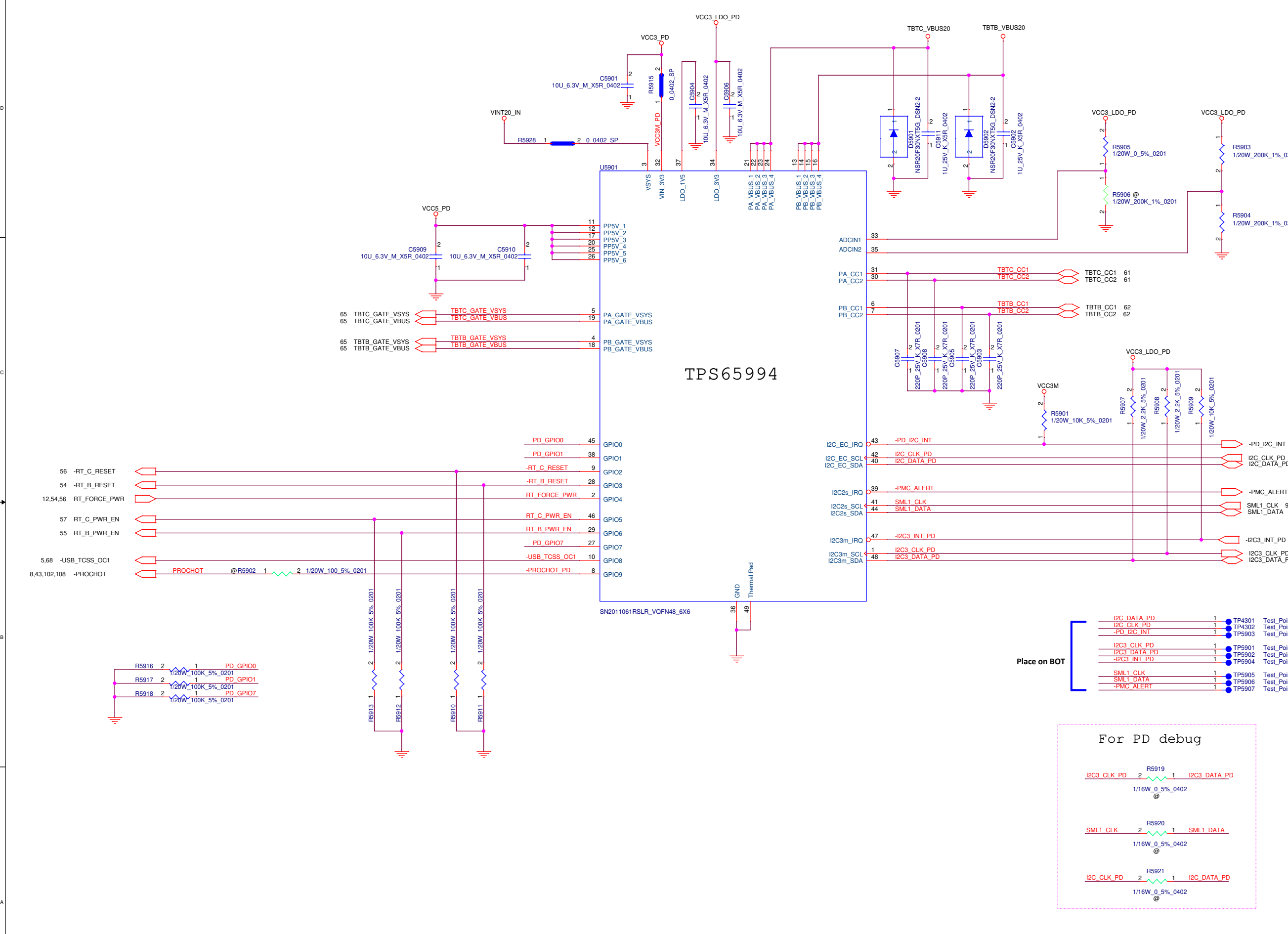


TABLE I2C Addressing

I2C1	Master: EC Slave: PD	TBTB PORT	0x24
		TBTC PORT	0x20
I2C2	Master: PMC Slave: PD	TBTB PORT	0x27
		TBTC PORT	0x23
I2C3	Master: PD Slave: RT	TBTB PORT	0x56
		TBTC PORT	0x57

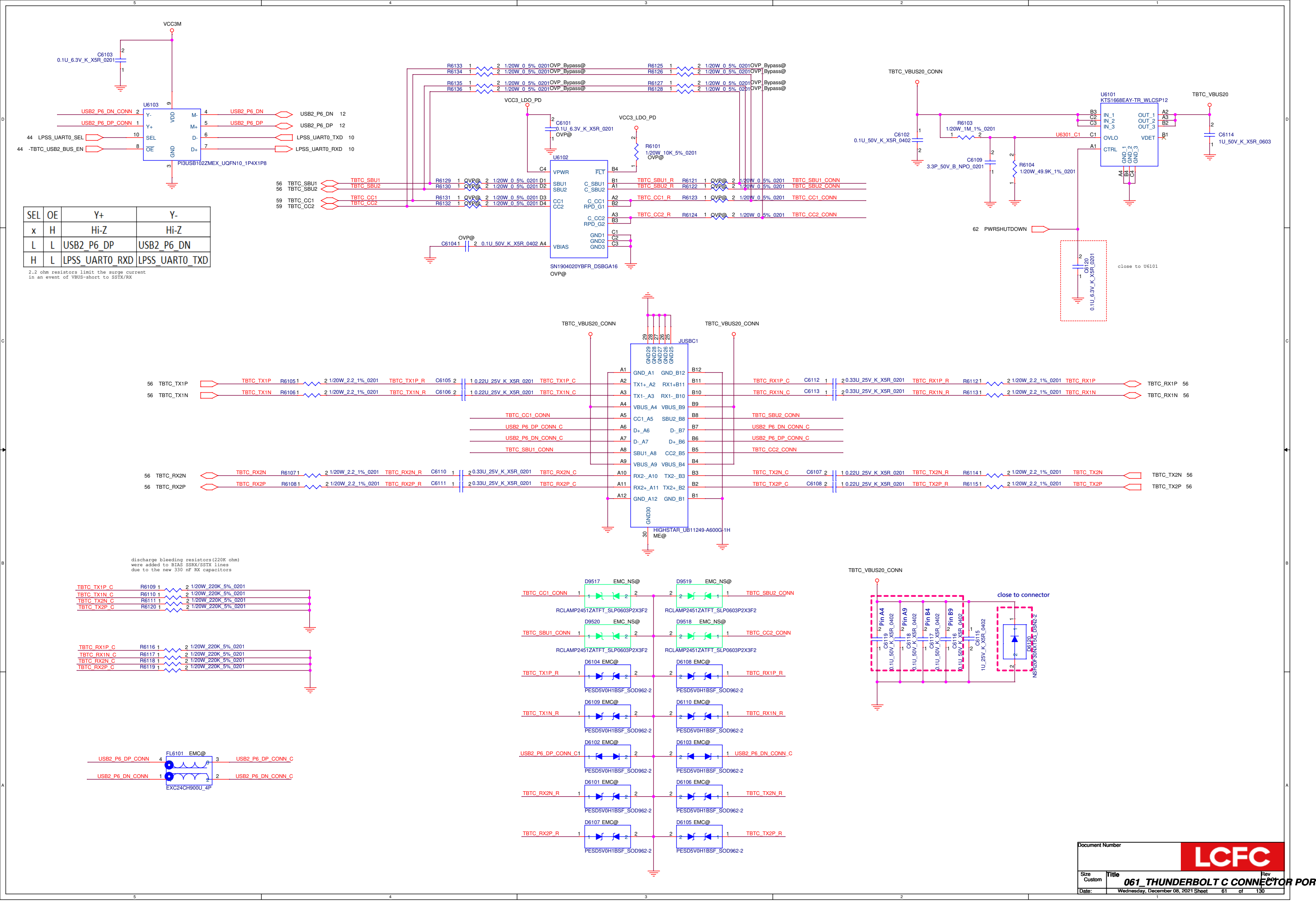
Document Number

LCFC

Size Custom | Title **059_USB PD CONTROLLER** | Rev 0.01

Date: Friday, December 03, 2021 Sheet 59 of 130

Document Number	LCFC		
Size A	Title **060_BLANK**		Rev 0.01
Date:	Friday, December 03, 2021	Sheet 60 of 130	



SEL	OE	Y+	Y-
x	H	Hi-Z	Hi-Z
L	L	USB2_P6_DP	USB2_P6_DN
H	L	LPSS_UART0_RXD	LPSS_UART0_TXD

Document Number

Size Custom

Title 061_THUNDERBOLT C CONNECTOR POR

Rev

Date: Wednesday, December 08, 2021 Sheet 61 of 130

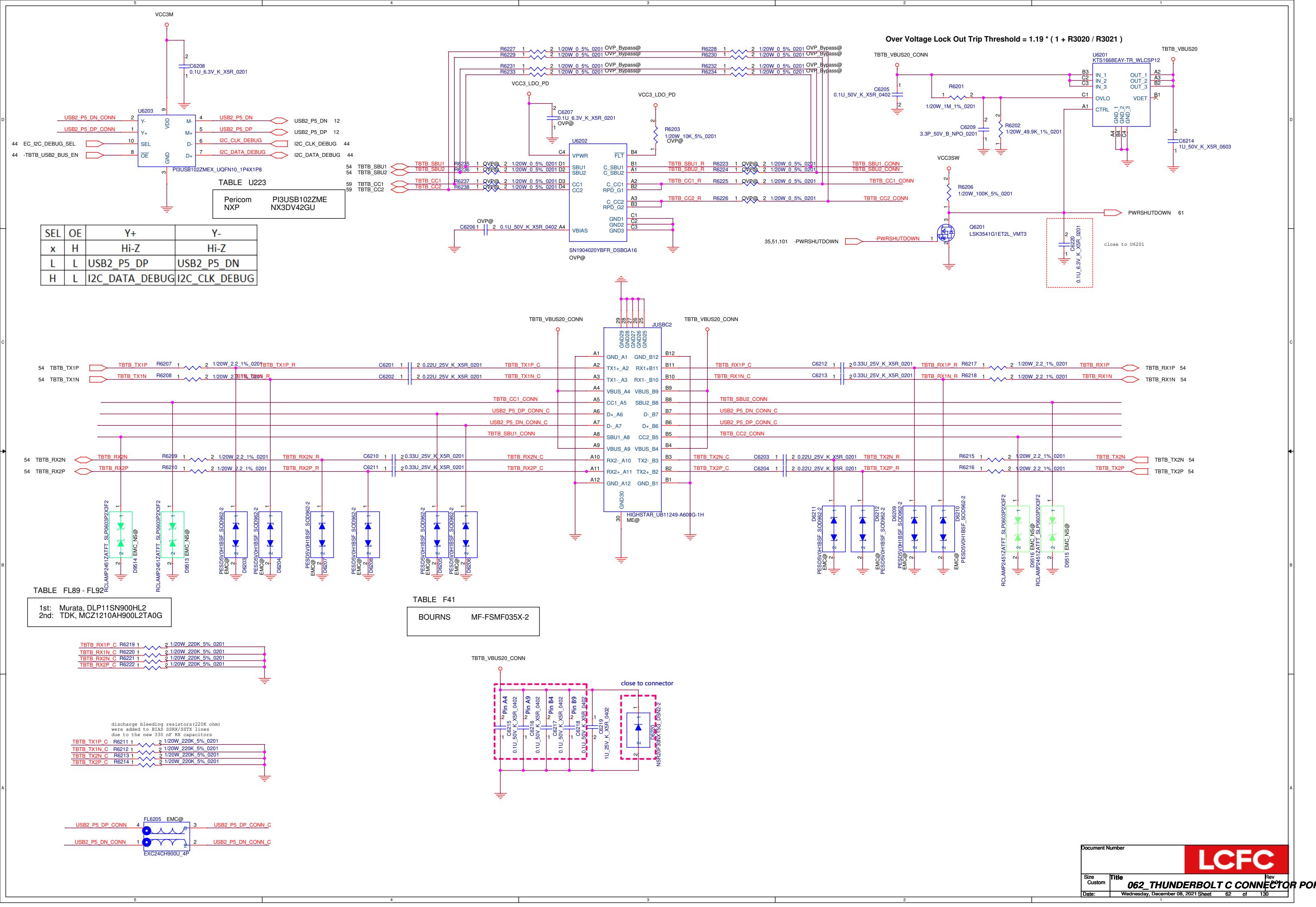


TABLE U223

Pericom	PI3USB102ZME
NXP	NX3DV42GU

SEL	OE	Y+	Y-
x	H	Hi-Z	Hi-Z
L	L	USB2_P5_DP	USB2_P5_DN
H	L	I2C_DATA_DEBUG	I2C_CLK_DEBUG

TABLE FL89 - FL92

1st: Murata, DLP11SN900HL2
2nd: TDK, MCZ1210AH900L2TA0G

TABLE F41

BOURNS	MF-FSMF035X-2

LCFC

Document Number

Size: Custom

Title: 062_THUNDERBOLT C CONNECTOR POR

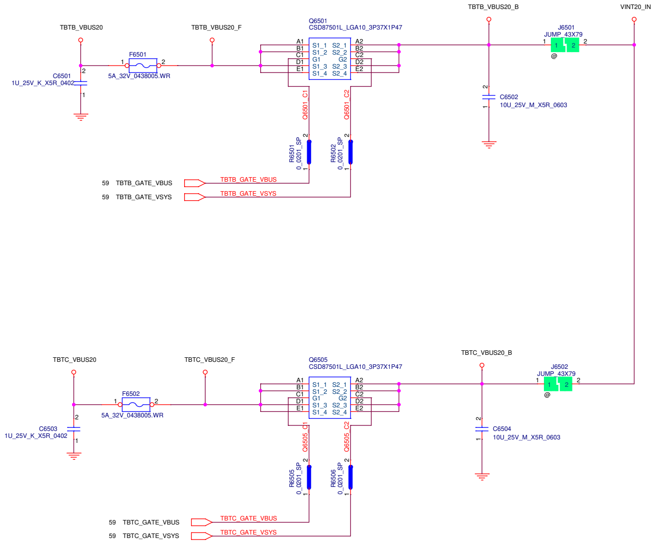
Date: Wednesday, December 08, 2021 Sheet 62 of 130

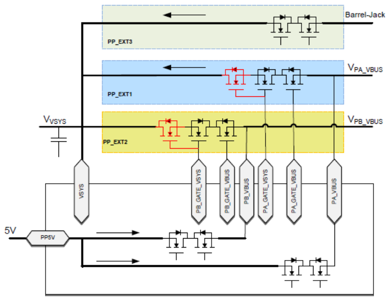
Document Number	LCFC	
Size Custom	Title 063_BLANK	Rev 0.01
Date:	Friday, December 03, 2021	Sheet 63 of 130

5 4 3 2 1

D C B A

Document Number		LCFC
Size: Custom	Title: **_064_BLANK_**	Rev: 0.01
Date:	Friday, December 03, 2021	Sheet 64 of 130





Document Number	LCFC	
Size: Custom	Title: 065_TYPEC_DCIN	Rev: 0.01
Date:	Friday, December 03, 2021	Sheet 65 of 130

Document Number		LCFC
Size Custom	Title **066_BLANK**	Rev 0.01
Date:	Friday, December 03, 2021	Sheet 66 of 130

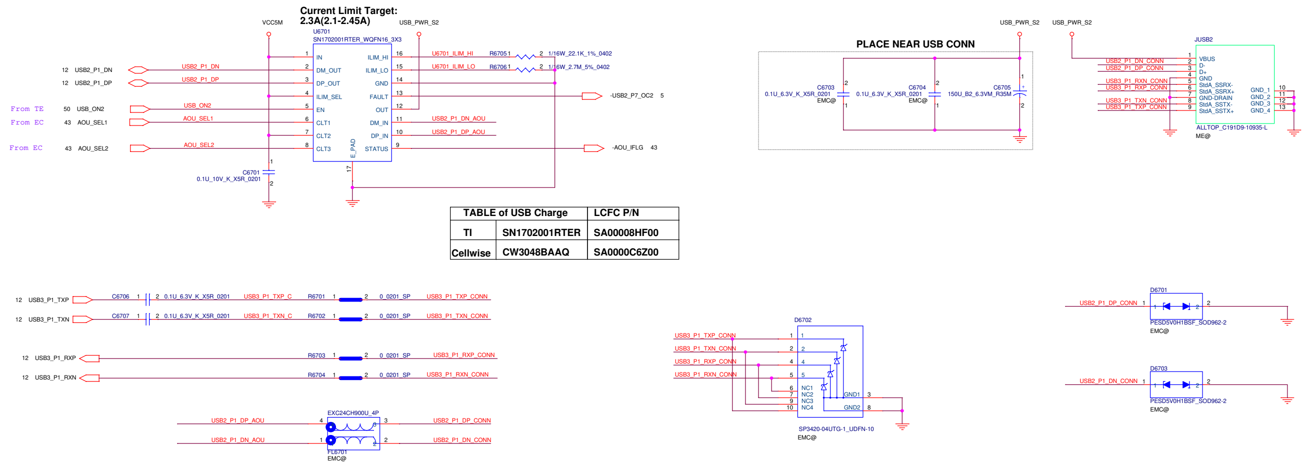
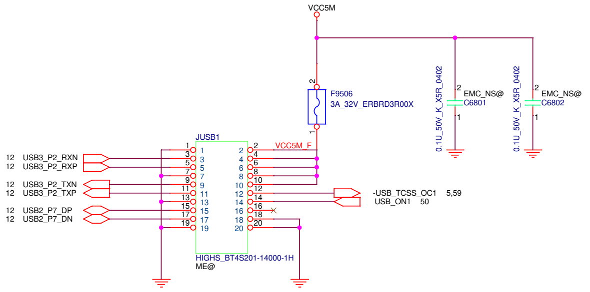


TABLE of USB Charge		LCFC P/N
TI	SN1702001RTER	SA00008HF00
Cellwise	CW3048BAAQ	SA0000C6Z00

Document Number	LCFC
Size: Custom	Title: 067_USB TYPE-A CONNECTOR PORT B — Rev 0.01
Date:	Friday, December 03, 2021 — Sheet 67 of 130



Document Number

LCFC

Size Custom

Title **068_USB TYPE-A CONNECTOR PORT A**

Rev

Date: Friday, December 03, 2021 Sheet 68 of 130

5 4 3 2 1

D

C

B

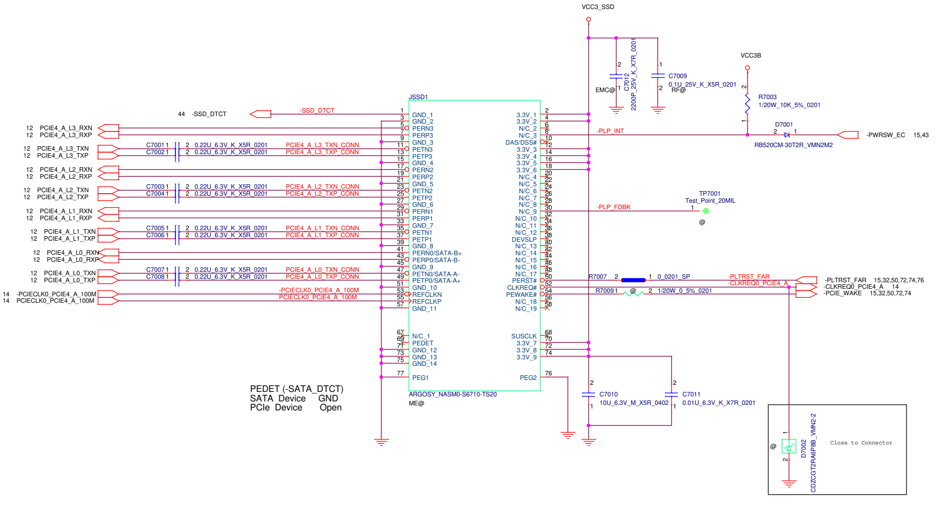
A

Document Number	
Size: CustomC	Title: **069_BLANK**	Rev: 0.01
Date:	Friday, December 03, 2021 Sheet 69 of 130

5 4 3 2 1

M.2 Socket 3 (Key-M) for 2280 S3 SSD

H=2.65mm Connector



PEDET (-SATA_DTCT)
SATA Device GND
PCIe Device Open

Document Number		LCFC
Size Custom	Title 070_M.2 SOCKET 3 MODULE I/F	Rev 0.1
Date: Friday, December 03, 2021	Sheet 70 of 130	

Document Number	LCFC	
Size: Custom	Title: 071_BLANK	Rev: 0.01
Date:	Friday, December 03, 2021	Sheet 71 of 130

M.2 Type 1216 Module for WLAN / Bluetooth

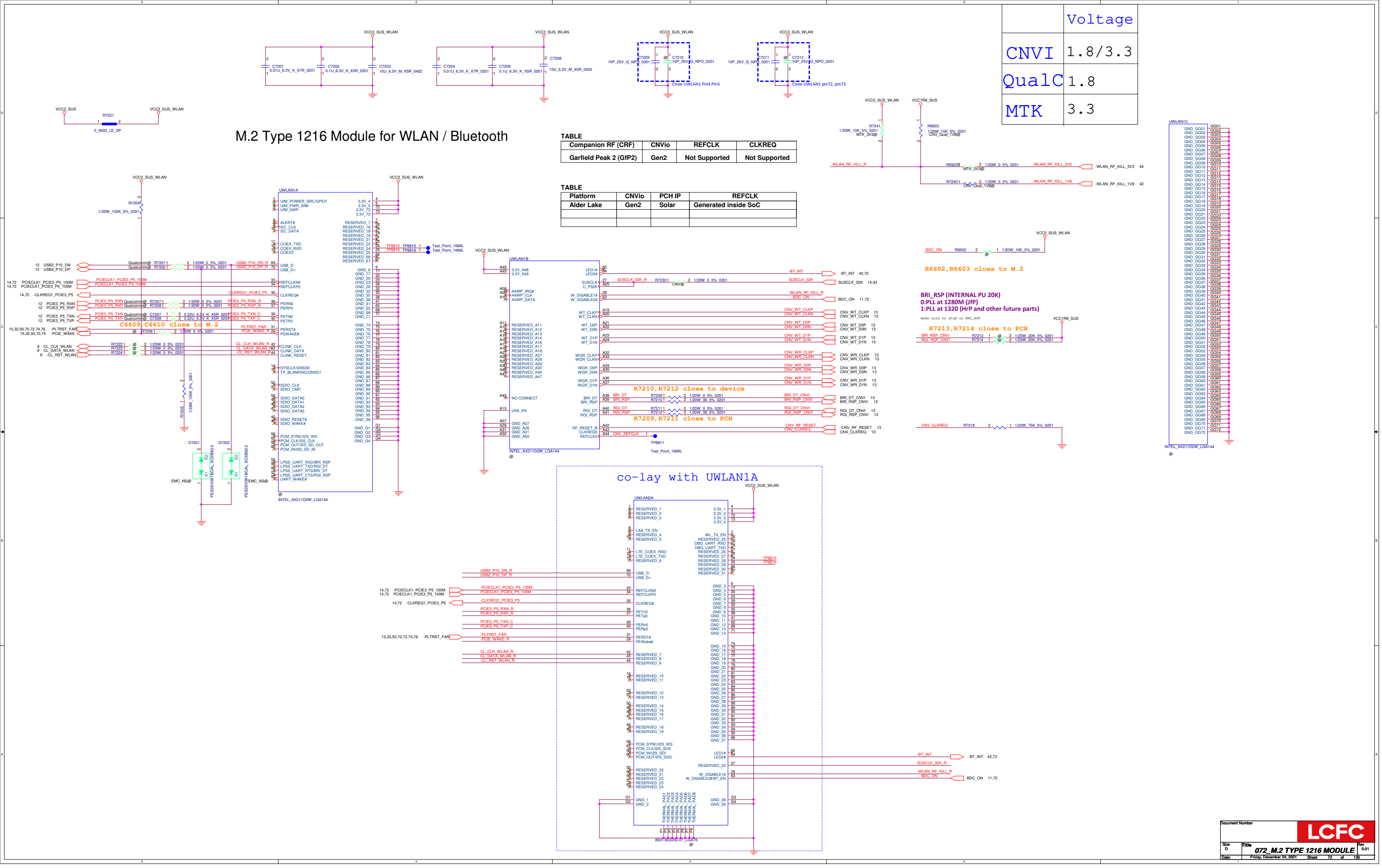
	Voltage
CNVI	1.8/3.3
QualC	1.8
MTK	3.3

TABLE

Companion RF (CRF)	CNVio	REFCLK	CLKREQ
Garfield Peak 2 (GfP2)	Gen2	Not Supported	Not Supported

TABLE

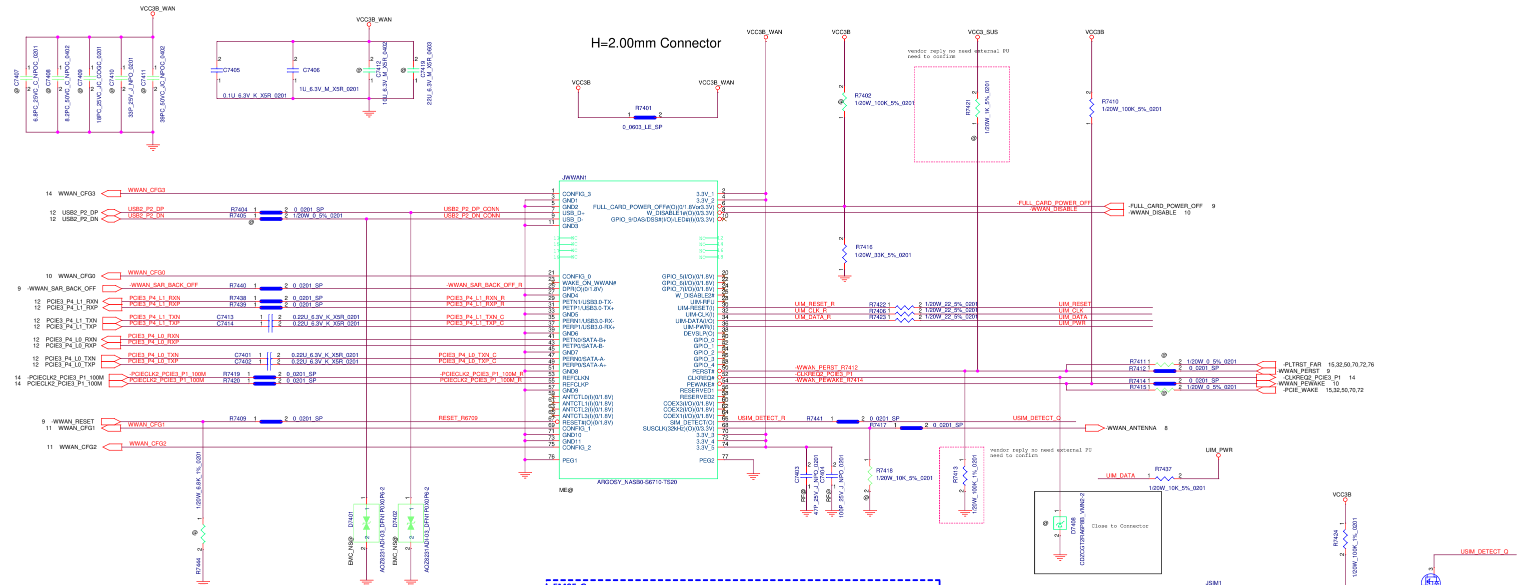
Platform	CNVio	PCH IP	REFCLK
Alder Lake	Gen2	Solar	Generated inside SoC



Document Number	
Size: D	Title: 072_M.2 TYPE 1216 MODULE	Rev: 0.01
Date:	Friday, December 24, 2021	Sheet 72 of 130

Document Number		LCFC
Size Custom	Title 073_BLANK	Rev 0.01
Date:	Friday, December 03, 2021 Sheet 73 of 130	

M.2 Socket 2 (Key-B) for 3042 S3 WWAN



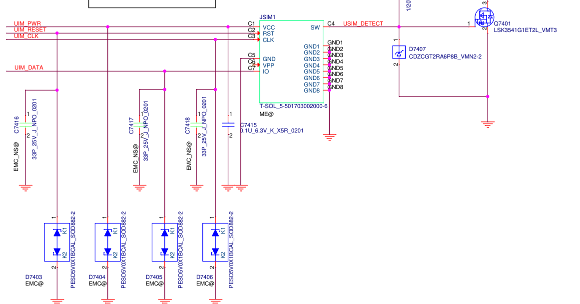


TABLE:

State #	Module Configuration Decodes CONFIG_0 (Pin 21)	CONFIG_3 (Pin 1)	CONFIG_2 (Pin 75)	CONFIG_1 (Pin 69)	Module Type and Main Host Interface	Port Configuration	Module
0	GND	GND	GND	GND	SSD - SATA	N/A	
1	GND	GND	GND	NC	SSD - PCIe	N/A	
2	GND	GND	NC	GND	WWAN - PCIe	0	
3	GND	GND	NC	NC	WWAN - PCIe	1	
4	GND	NC	GND	GND	WWAN - PCIe, USB 3.1 Gen1	0	
5	GND	NC	GND	NC	WWAN - PCIe, USB 3.1 Gen1	1	
6	GND	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	2	EM05-G
7	GND	NC	NC	NC	WWAN - PCIe, USB 3.1 Gen1	3	FM350-GL
8	NC	GND	GND	GND	WWAN - SSIC	0	EM05-CE
9	NC	GND	GND	NC	WWAN - SSIC	1	
10	NC	GND	NC	GND	WWAN - SSIC	2	
11	NC	GND	NC	NC	WWAN - SSIC	3	
12	NC	NC	GND	GND	WWAN - PCIe	2	
13	NC	NC	GND	NC	WWAN - PCIe	3	
14	NC	NC	NC	GND	WWAN - PCIe, USB 3.1 Gen1	Vendor Defined	L860 R+
15	NC	NC	NC	NC	No Module Present	N/A	

TABLE of WWAN (Pin68# ANT_CONFIG)		
M.2 module side	Description	MIMO mode
EM05-G	TBD	TBD
L860 R+	#68=NC/high	2
	#68=low level	4

EM05-G

EM05-G provides four configuration pins, which are defined as below.

Table 21: Configuration Pins List of M.2 Specification

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
GND	GND	NC	NC	Quectel defined	NA

EM05-CE

The 4 configuration pins on EM05-CE module are defined as below:

Table 18: List of Configuration Pins

Config_0 (Pin 21)	Config_1 (Pin 69)	Config_2 (Pin 75)	Config_3 (Pin 1)	Module Type and Main Host Interface	Port Configuration
NC	GND	GND	GND	WWAN-SSIC	0

L860 R+

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
NC	GND	NC	NC	WWAN - PCIe Gen2	Vendor defined

FM350-GL

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuration
GND	NC	NC	NC	WWAN–PCIe Gen3, USB3.1 Gen1	Vendor defined

Document Number	LCFC
Size: Custom	Title: 075_BLANK	Rev: 0.01
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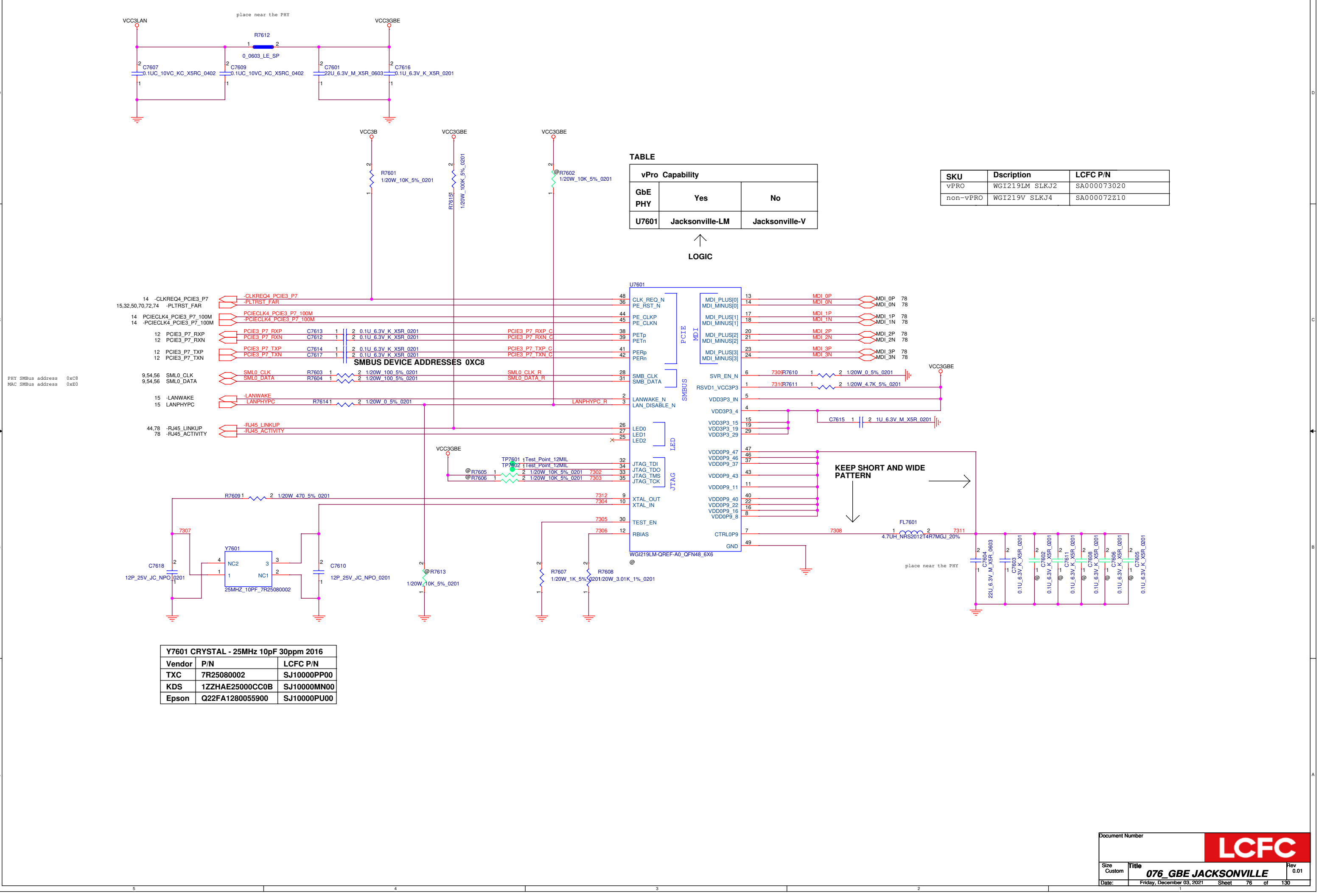


TABLE

vPro Capability		
GbE PHY	Yes	No
U7601	Jacksonville-LM	Jacksonville-V

SKU	Dscription	LCFC P/N
vPRO	WGI219LM SLKJ2	SA000073020
non-vPRO	WGI219V SLKJ4	SA000072Z10

Y7601 CRYSTAL - 25MHz 10pF 30ppm 2016		
Vendor	P/N	LCFC P/N
TXC	7R25080002	SJ10000PP00
KDS	1ZZHAE25000CC0B	SJ10000MN00
Epson	Q22FA1280055900	SJ10000PU00

Document Number

LCFC

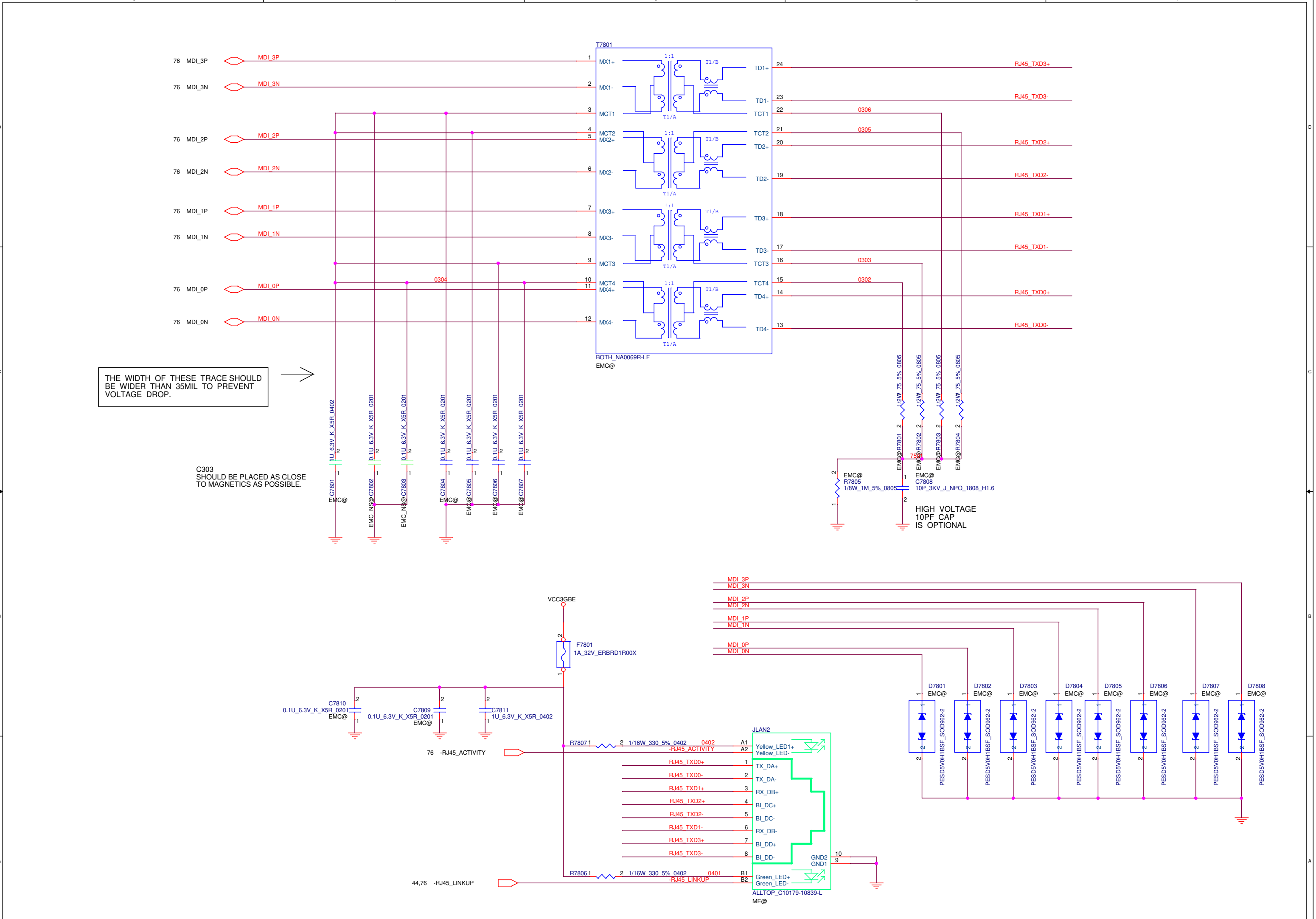
Size: Custom

Title: 076_GBE JACKSONVILLE

Rev: 0.01

Date: Friday, December 03, 2021 Sheet 76 of 130

Document Number		
Size Custom	Title **077_LAN SWITCH**	Rev 0.01
Date:	Friday, December 03, 2021 Sheet 77 of 130	



Document Number	
Size: C	Title: 078_LAN CONNECTOR
Rev: 0.01	
Date: Friday, December 03, 2021	Sheet 78 of 130

LCFC

Document Number	
	LCFC

Size	Title	Rev
A	079_BLANK	0.01
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Size: A	Title: 080_BLANK	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 80 of 130

Document Number			
Size B	Title **082_MEDIA CARD CONNECTOR**		Rev 0.01
Date:	Friday, December 03, 2021	Sheet 82 of 130	

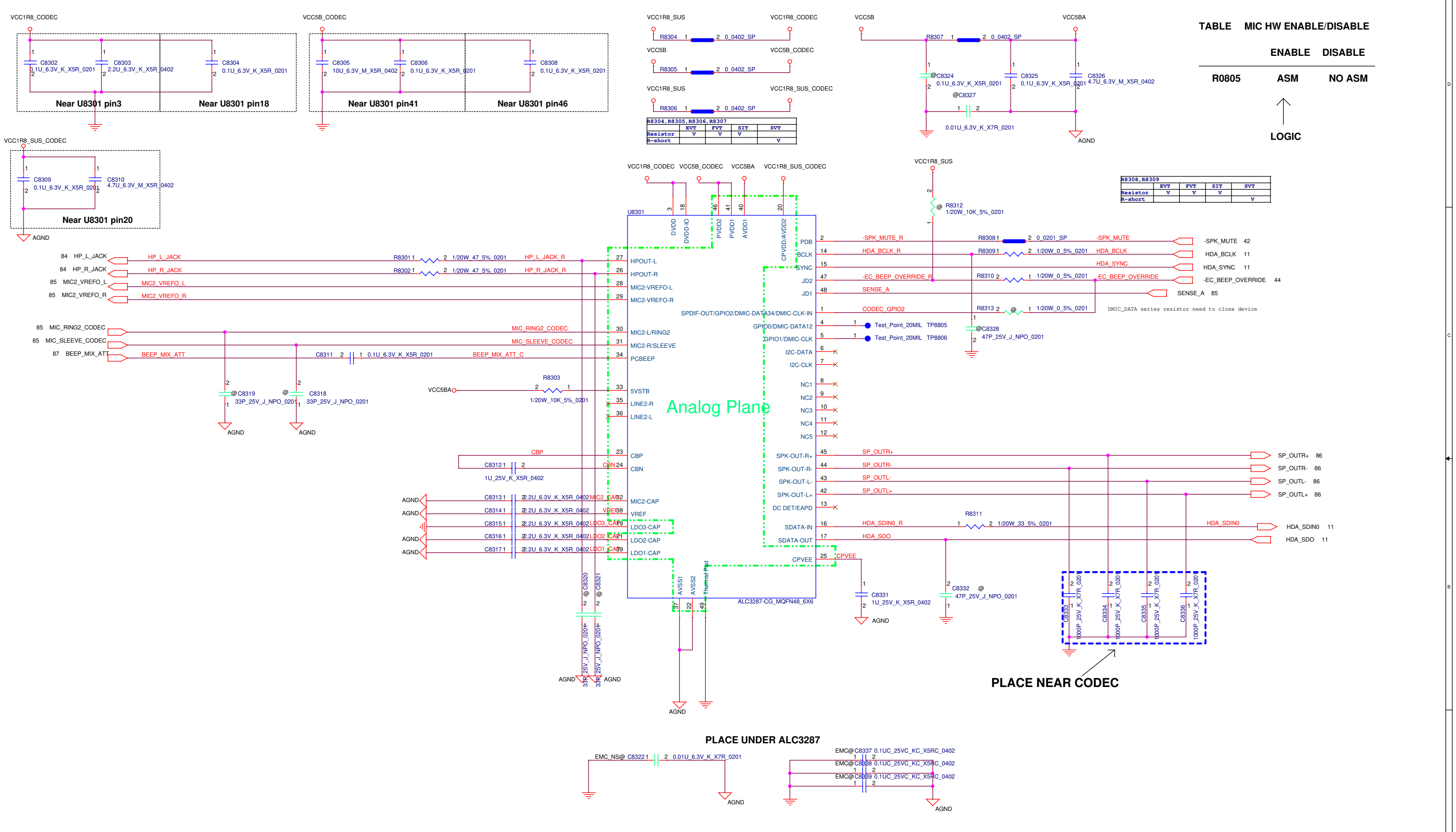


TABLE MIC HW ENABLE/DISABLE

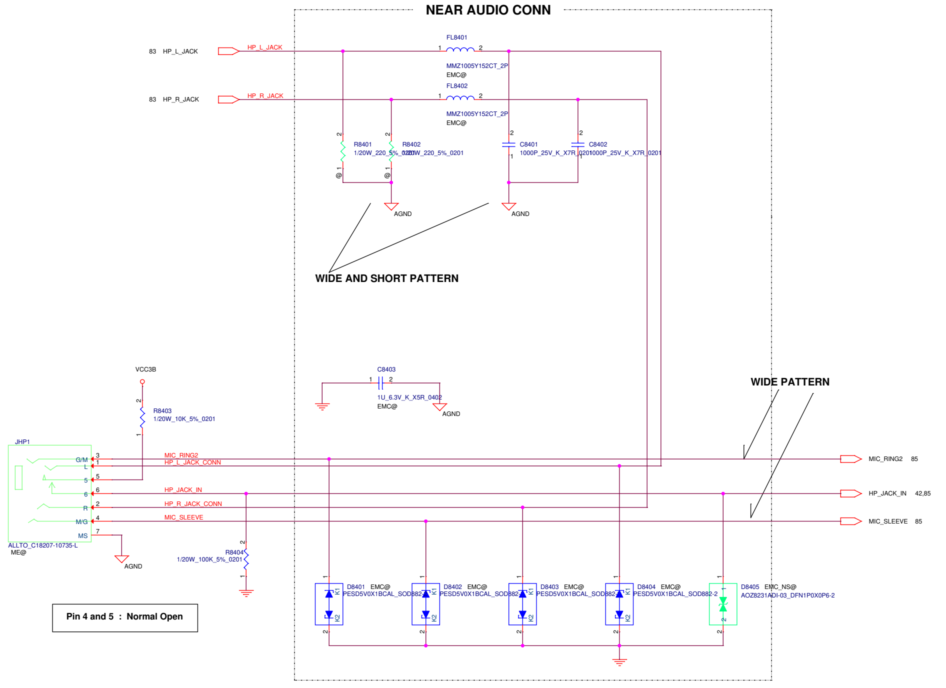
	ENABLE	DISABLE
R0805	ASM	NO ASM

LOGIC

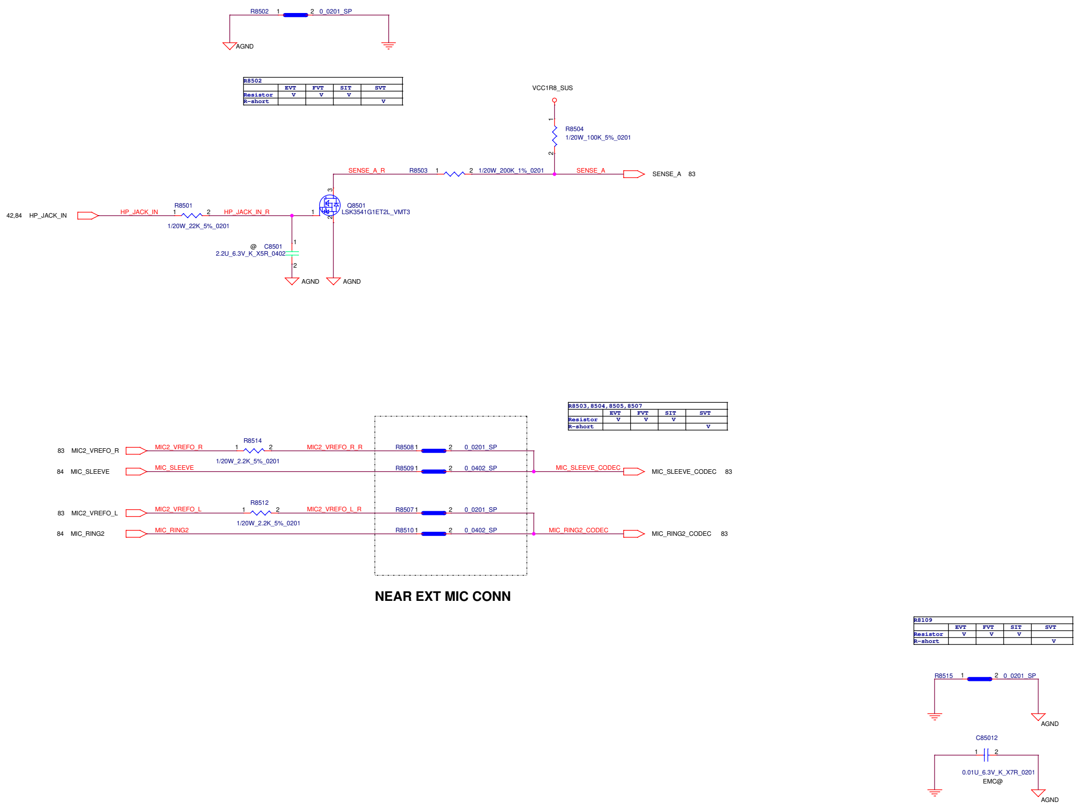
R8304,R8305,R8306,R8307	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

R8308,R8309	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

Document Number		
Size: Custom	Title: 083_AUDIO CODEC	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 83 of 130	



Document Number		LCFC
Size: Custom	Title: 084_AUDIO JACK	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 84 of 130	



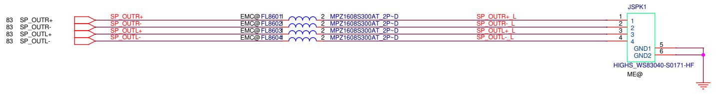
R8502				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

R8503,8504,8505,8507				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

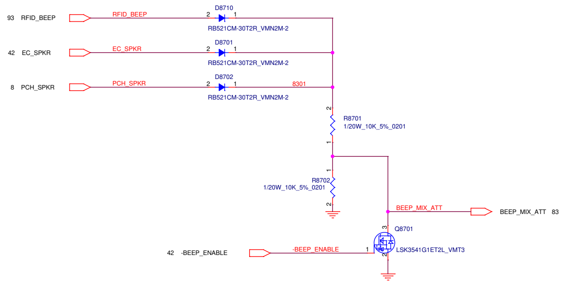
NEAR EXT MIC CONN

R8109				
	EVT	FVT	SIT	SVT
Resistor	V	V	V	
R-short				V

Document Number		LCFC
Size Custom	Title 085_AUDIO JACK SENSE_MIC_I/F	Rev 0.01
Date:	Friday, December 03, 2021	Sheet 85 of 130



Document Number			LCFC
Size Custom	Title **086_AUDIO SPEAKER**		Rev 0.01
Date:	Friday, December 03, 2021	Sheet 86 of 130	



Document Number	LCFC	
Size: Custom	Title: 087_AUDIO BEEP	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 87 of 130	

Document Number		LCFC
Size Custom	Title 088_BLANK	Rev 0.01
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Document Number		
Size A	Title **089_BLANK**	Rev 0.01
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Document Number	LCFC

Size	Title	Rev
A	090_BLANK	0.01
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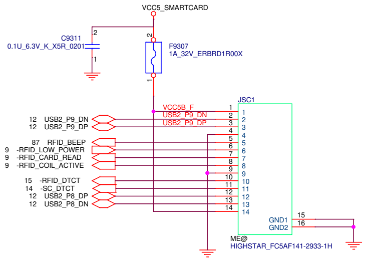
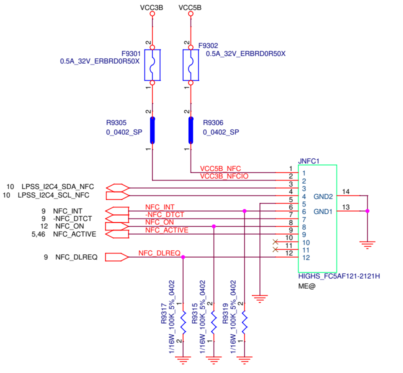
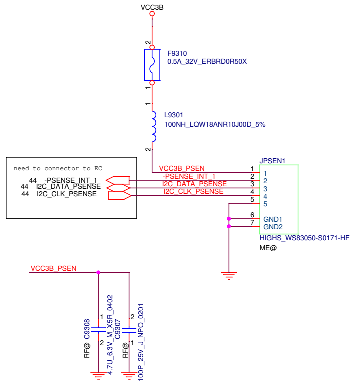
Document Number	
Size A	Title **091_BLANK**	Rev 0.01
Date: Friday, December 03, 2021	Sheet 91 of 130

Document Number			
Size A	Title **_092_BLANK_**		Rev 0.01
Date:	Friday, December 03, 2021	Sheet 92 of 130	



	RFID & Smart Card	NFC
Pin1	VBUS_5V	VBUS_5V_NFC
Pin2	USB_D-	VBUS_3V_NFC
Pin3	USB_D+	I2C0_DATA_NFC
Pin4	GND	I2C0_CLK_NFC
Pin5	BEEP	GND
Pin6	LOW POWER	NFC_INT
Pin7	CARD_READ	-NFC_DTCT
Pin8	COIL_ACTIVE	NFC_ON
Pin9	GND	NFC_ACTIVE
Pin10	-RFID_DTCT	NC
Pin11	-SC_DTCT	NC
Pin12	USB_D+	NFC_DLREQ
Pin13	USB_D-	
PIN14	VCC +5V	





P-sensor IC

WLCSP-9

(Channel 0)

Ping number	MB Net name	P-IC Net name
1	VCC3B_PSEN_3.3V	VDDHI
2	-PSENSE_INT_1	GPIO/RDY
3	I2C_DATA_PSENSE	SDA
4	I2C_CLK_PSENSE	SCL
5	GND	VSS

Document Number

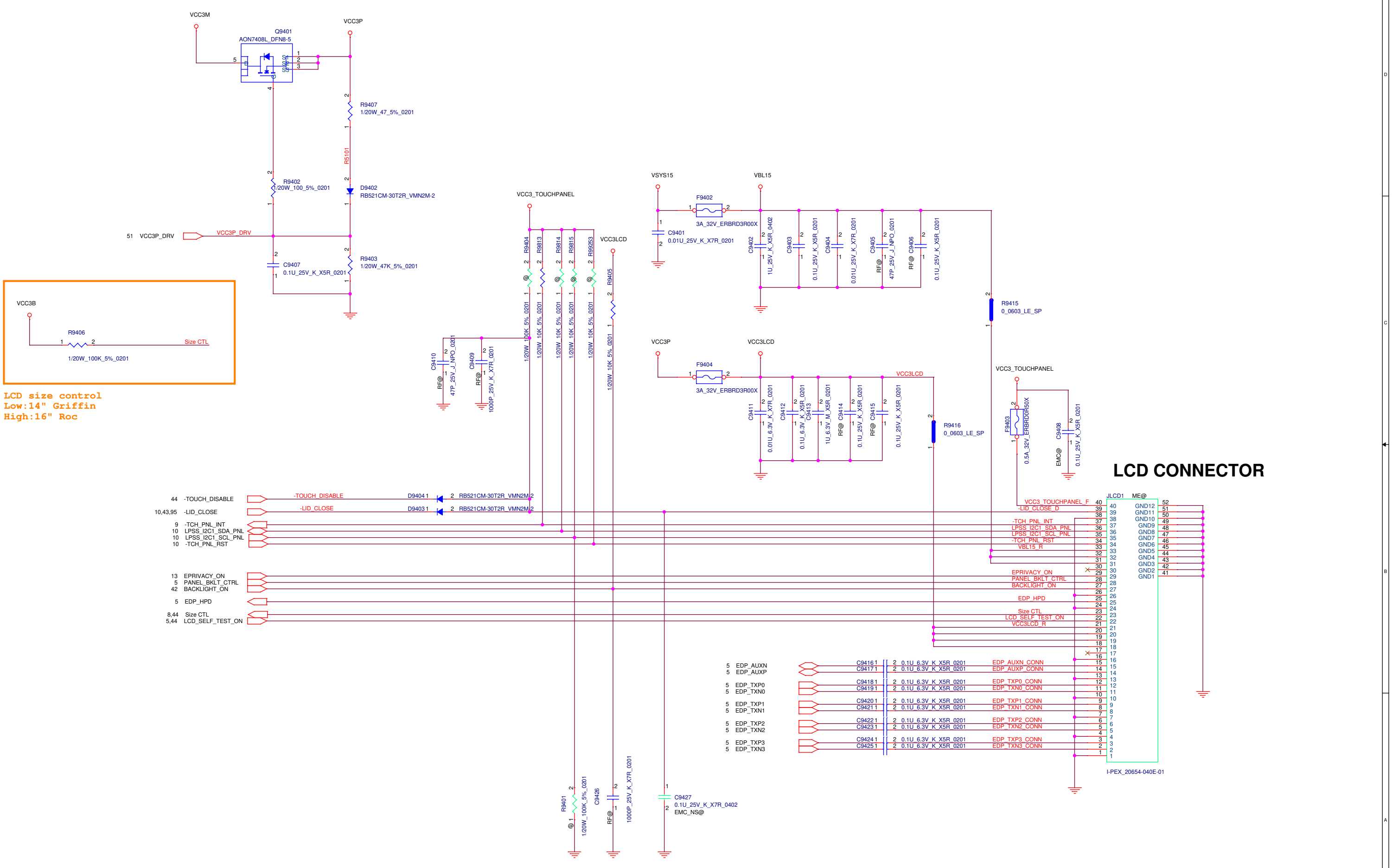
LCFC

Size: C

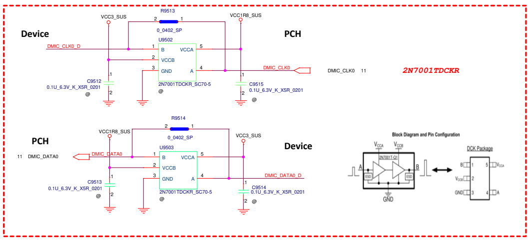
Title: 093_Smart Card Reader/NFC/P-Sensor

Rev: 0.01

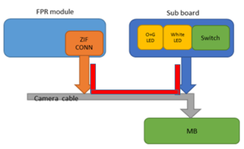
Date: Friday, December 03, 2021 Sheet 93 of 130



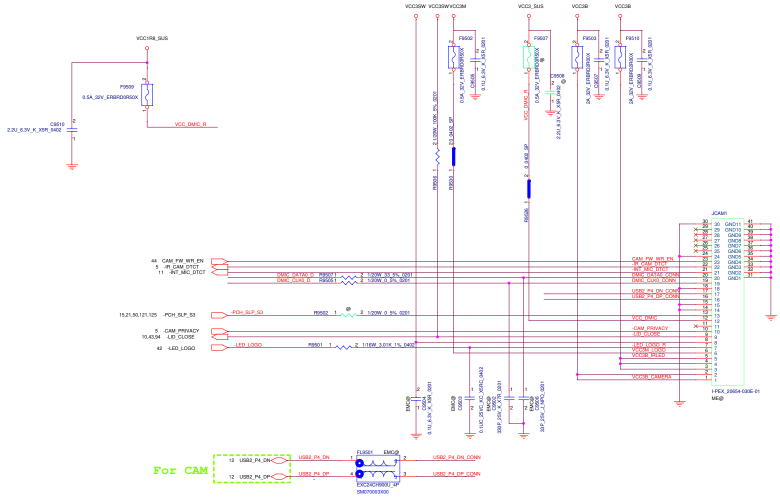
Document Number			LCFC
Size: Custom	Title: 094_LCD INTERFACE		Rev: 0.01
Date: Friday, December 03, 2021	Sheet 94 of 130		

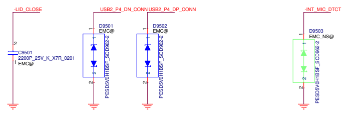


Case-1



WTB – Camera
 – FPR
 – PWR SUB BD
–Hall Sensor





For HPD

Pin assignment

No.		No.	
17	IR_VCC	18	IR_VCC
1	MIC_DET	16	MIC_VCC
2	•WP	15	MIC_CLK
3	NC	14	MIC_DATA
4	NC	13	NC
5	CAM_3V3	12	CAM_3V3
6	•Reverse	11	D+
7	MIC_GND	10	D-
8	DGND	9	DGND
19	IR_GND	20	IR_GND

For Hybrid & RGB

Pin assignment

No.		No.	
17	IR_VCC	18	IR_VCC
1	MIC_DET	16	MIC_VCC
2	•WP	15	MIC_CLK
3	NC	14	MIC_DATA
4	NC	13	NC
5	CAM_3V3	12	CAM_3V3
6	•Reverse	11	D+
7	MIC_GND	10	D-
8	DGND	9	DGND
19	IR_GND	20	IR_GND

PIN	State	
-PWRSWITCH_EN GPIO_AL0	High	Disable Power Button
	Low	Enable Power Button
FPR_MODE_SEL DELINK	High	S0/S0i3
	Low	S3/S4/S5

case1-connctor type — FPR

Connected to system

PIN	SIGNAL	
1	D3V3	3V3_B
2	Reset	reset pin for goodix
3	GPIO_AL0	GPIO for Power Button Suppression Indicate to host whether should suppress button press
4	DELINK	GPIO for OS stats
5	GLED_CTRL	Green LED
6	OLED_CTRL	Orange LED
7	GND	GND
8	USBDP	USB DP
9	USBDM	USB DN
10	NC	NC

FPR_PWR_SHIELD

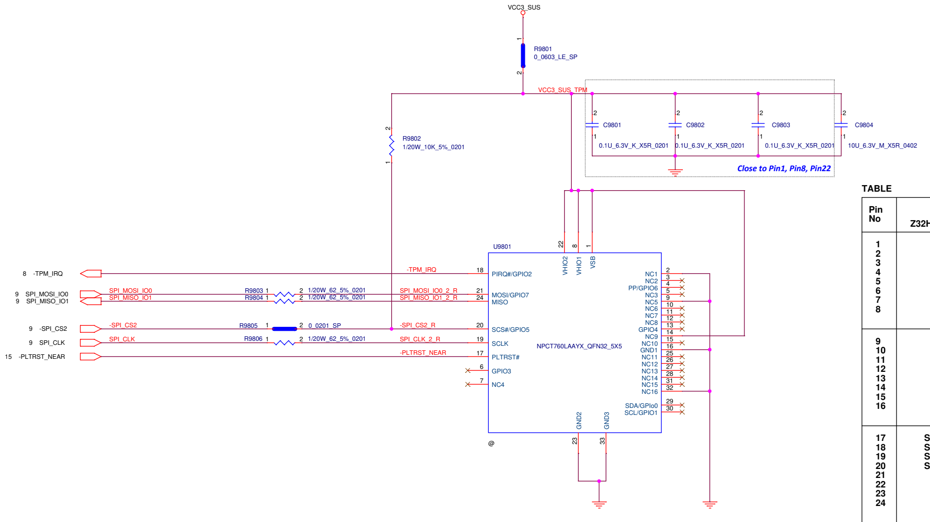
case1 — Subcard

O/G LED on sub card

White LED on sub card

PIN	SIGNAL	
1	OLED	Orange LED
2	GLED	Green LED
3	D5P0	VCC5B
4	NC	
5	D3P3	VCC3B
6	PRBTN-	Power botton out
7	GND	GND
8	PRLED-	White LED

Document Number		
Size: C	Title: 097_BLANK	Rev: 0.01
Date: Friday, December 03, 2021	Sheet 97 of 130	



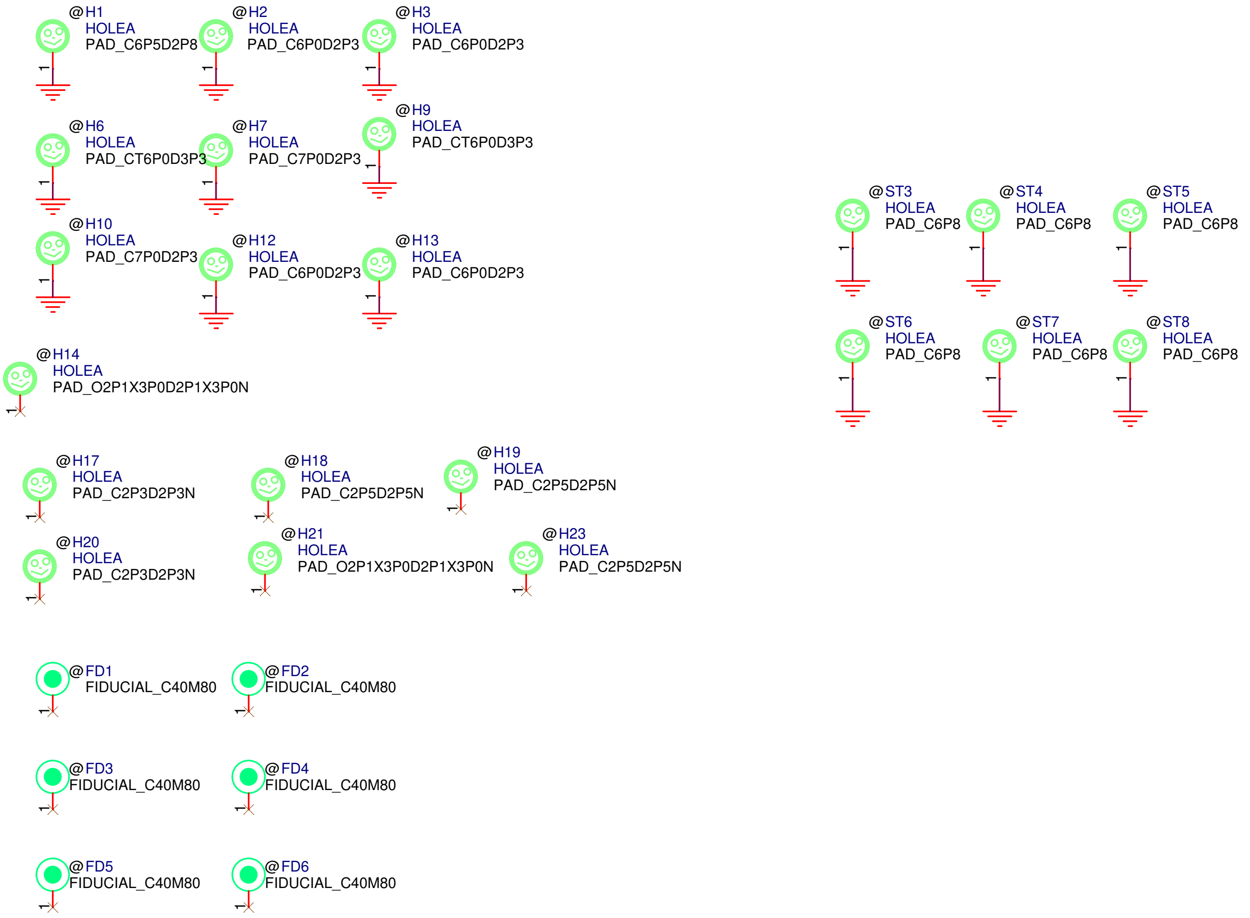
TABLE

Pin No	Nations Z32H330TC-SQN-L4	Nuvoton NPCT760LAAYX	ST Micro ST33HTPH2X32AHE0
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	NC	GPIO/PP	NC
5	NC	NC	NC
6	NC	GPIO3	GPIO_LP
7	PP	NC	GPIO_PP
8	VDD	VHIO	NC
9	GND	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	NC	GPIO4	NC
14	VDD	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	NC	SDA/GPIO0	NC
30	NC	SDA/GPIO1	NC
31	NC	NC	NC
32	GND	NC	NC

TABLE of TPM (U9801)

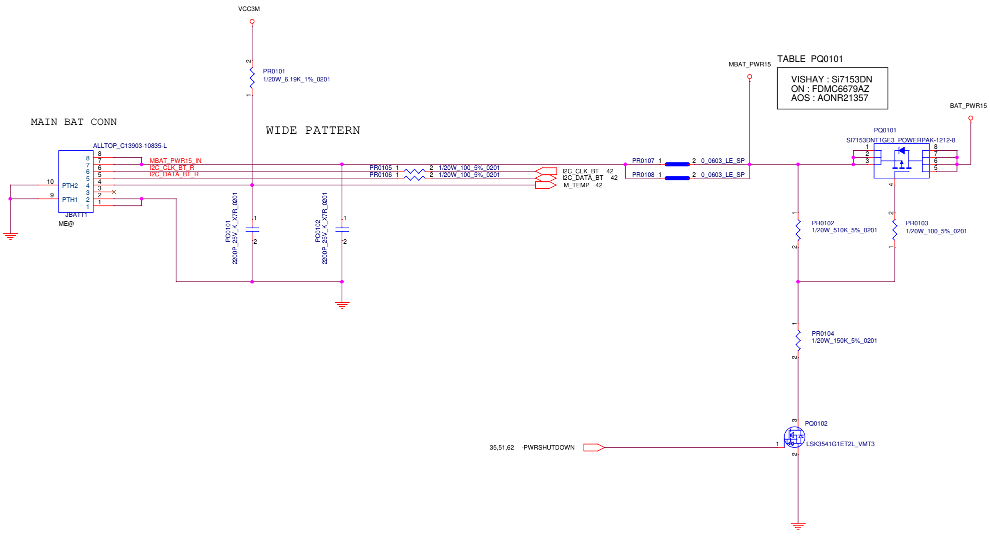
Vendor	P/N	LCFC P/N
ST Micro	ST33HTPH2X32AHE0	SA0000C8600
Nuvoton	NPCT760LAAYX	SA0000C3000
Nations	Z32H330TC-SQN-L4	SA0000C1S00

Document Number		LCFC
Size: Custom	Title: 098_DISCRETE TPM 2.0	Rev: 0.01
Date:	Friday, December 03, 2021	Sheet 98 of 130



Document Number		LCFC
Size A	Title **099_SCREW HOLES**	Rev 0.01
Date:	Friday, December 03, 2021	Sheet 99 of 130

Document Number	LCFC	
Size Custom	Title ***BLANK***	Rev 0.01
Date:	Tuesday, January 04, 2022	Sheet 100 of 130



Document Number	LCFC
Size: Custom	Title: **101_BATTERY INPUT** — Rev 0.01
Date: Tuesday, January 04, 2022	Sheet 101 of 130

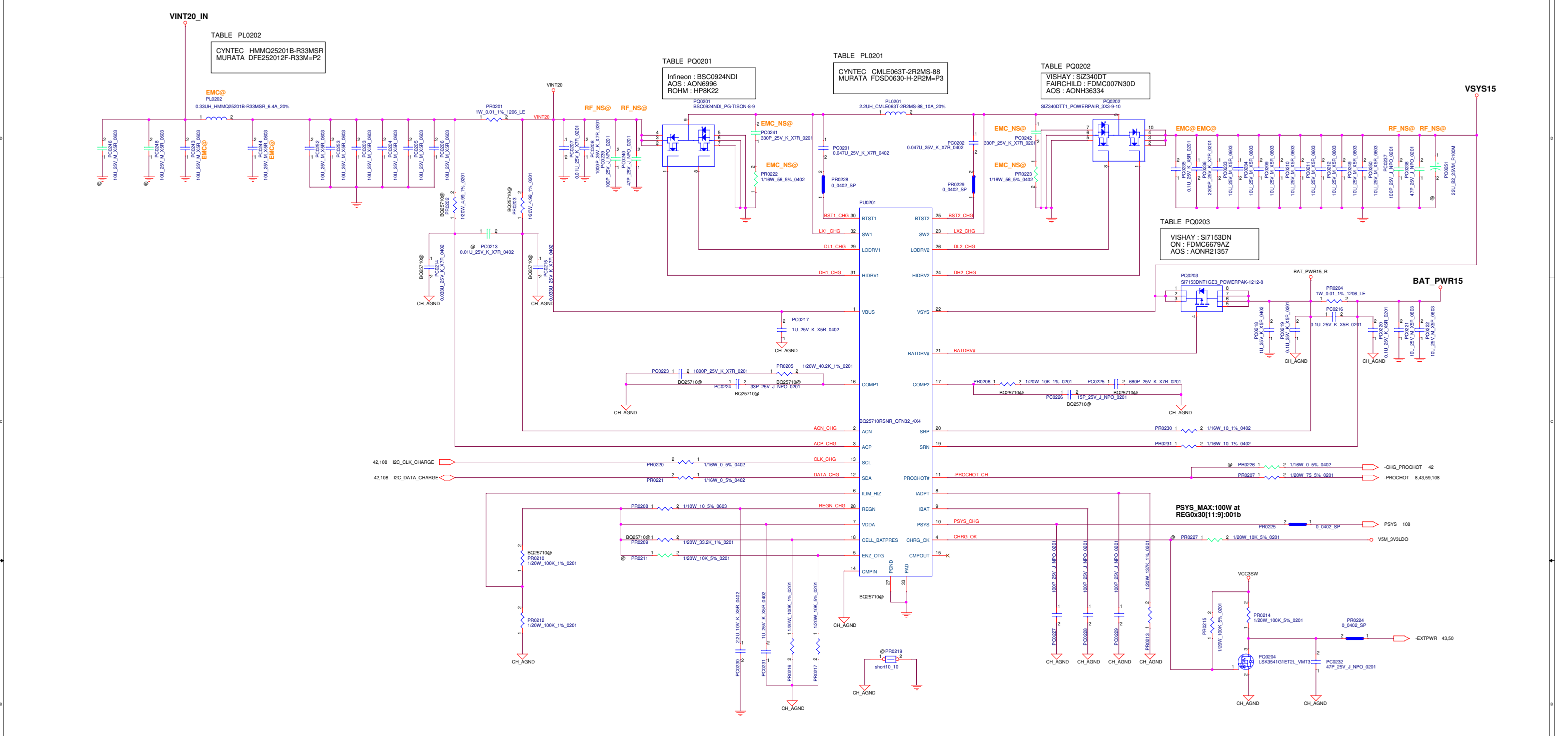


TABLE : ILIM_HIZ

IDPM	V (ILIM)	BQ25710RSNR	SC8885LQDER
500mA	1.2V		
1.0A	1.4V		
1.5A	1.6V		
2.0A	1.8V	237K	191K
3.0A	2.2V	174K	137K
3.25A	2.3V	162K	127K
4A	2.6V	131K	
5A	3V	100K	

W/ 65W adapter

W/ 100W adapter

TABLE : CELL_BATPRES (PR0209)

# of CELL	V (CELL_PRES)	BQ25710RSNR	SC8885LQDER
1-CELL	1.5V	301K	249K
2-CELL	2.5V	140K	110K
3-CELL	3.5V	71.5K	49.9K
4-CELL	4.5V	33.2K	16.5K

LOGIC

TABLE

Inductor	R(IADP)	fsw@POR
1.0uH	93kohm	800kHz
2.2uH	137kohm	800kHz
3.3uH	169kohm	800kHz

LOGIC

Charger BOM table

IC	U196	BQ25710RSNR	SC8885LQDER
ACP	PR0202	4.99ohm_1%_0201	10ohm_1%_0201
ACN	PR0203	4.99ohm_1%_0201	10ohm_1%_0201
ACP	PC0214	0.033uF_10%_25V_0402	NO_ASM
ACN	PC0215	0.033uF_10%_25V_0402	NO_ASM
COMP1	PR0205	40.2k_1%_0201	100k_1%_0201
COMP1	PC0223	1800pF_10%_25V_0201	1000pF_10%_25V_0201
COMP1	PC0224	33pF_5%_25V_0201	10pF_5%_25V_0201
COMP2	PR0206	10k_1%_0201	330k_1%_0201
COMP2	PC0225	680pF_10%_25V_0201	1000pF_10%_25V_0201
COMP2	PC0226	15pF_5%_25V_0201	220pF_10%_25V_0201
ILIM_HIZ	PR0210	174k_1%_0201	137k_1%_0201
CELL_BATPRESZ	PR0209	33.2k_1%_0201	16.5k_1%_0201

LOGIC

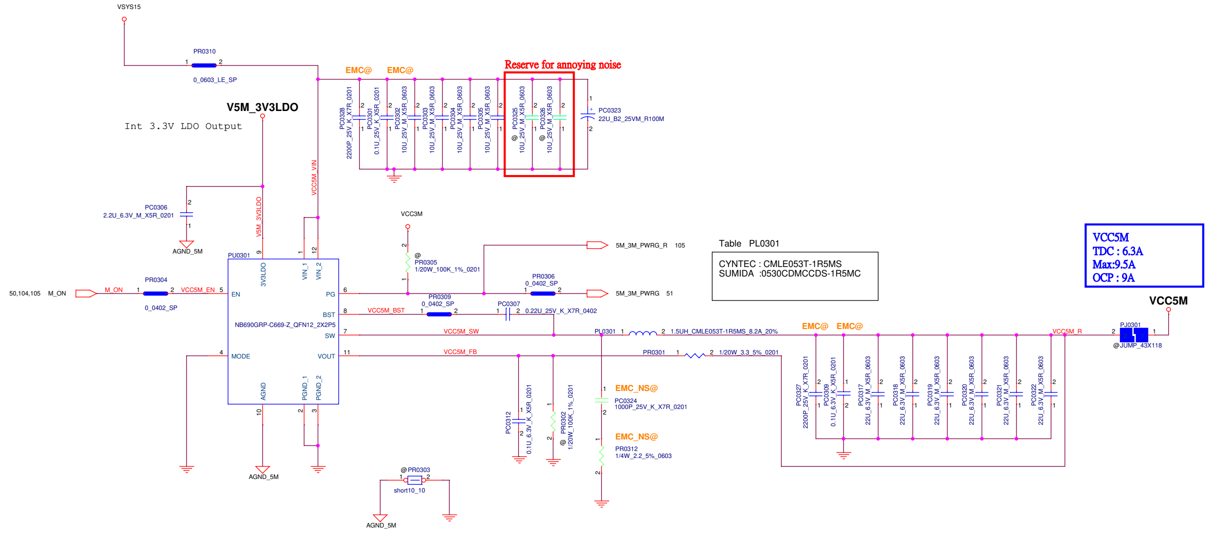


TABLE: NB690 Mode Control

RMode	MODE	VOUT	3V3LDO
0	Ceramic Cout	5.1V	3.3V
60K	POSCAP Cout	5.1V	3.3V
120K	Ceramic Cout	5V	3.3V
180K	POSCAP Cout	5V	3.3V
Floating	X	3.3V	3.3V

LOGIC

Document Number	LCFC
Size: Custom	Title: 103_DC/DC VCC5M (NB690) — Rev 0.01
Date: Tuesday, January 04, 2022	Sheet 103 of 130

TABLE1: NB693A CLM

Mode	CLM	Resister to GND
M1	7A	0
M2	10A	90K
M3	13A	150K
M4	16A	>230K or Float

LOGIC

TABLE 2: NB693A Mode 1 Control

Mode	VOUT	FS	Resister to GND
M1	Vo<3V, Vref=0.6V	700KHz	0
M2	Vo<3V, Vref=0.6V	1000KHz	90K
M3	Vo>=3V, Vref=1.8V	1000KHz	150K
M4	Vo>=3V, Vref=1.8V	700KHz	>230K or Float

LOGIC

VCC5_PD
TDC : 5.8A
OCP : 10A

Table PL0401

CYNTEC : CMLE053T-1R5MS
SUMIDA :0530CDMCCDS-1R5MC

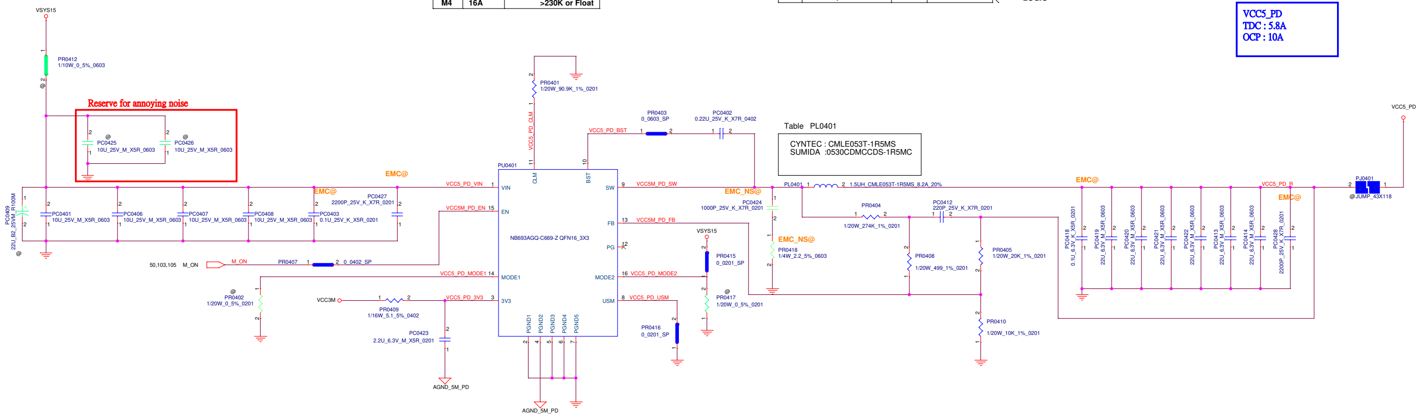


TABLE 3: NB693A MODE2 Selection

State	State	Mode2
M1	Internal Vcc	0
M2	External Vcc	Pull to VIN

LOGIC

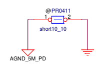
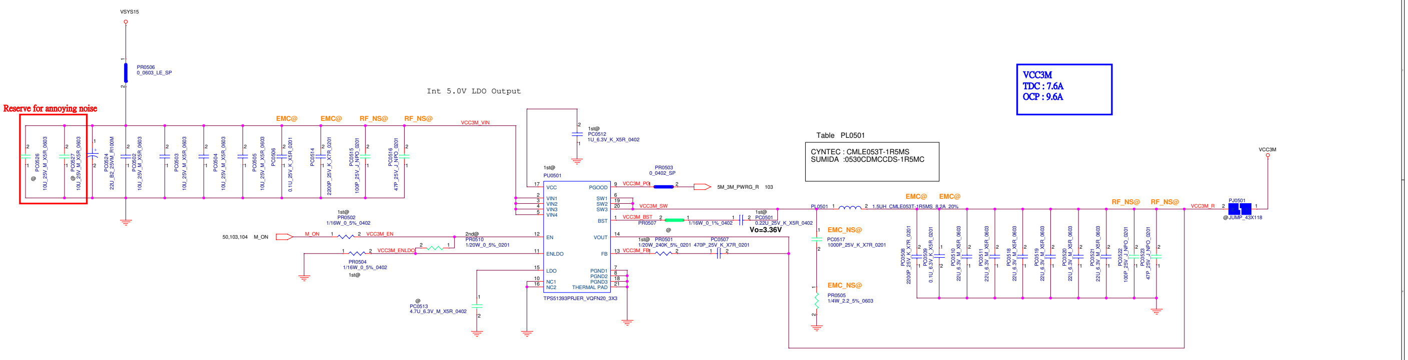


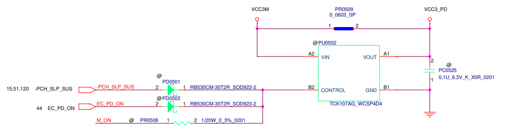
TABLE 4: USM Selection

State	USM	Resister to GND
M1	Y	0
M2	N	Floating

LOGIC

Document Number		LCFC
Size Custom	Title 104_DC/DC VCC5_PD (NB693AGQ)	Rev 0.01
Date:	Tuesday, January 04, 2022 Sheet 104 of 130	





VCC3M BOM table

IC	PU0501	**TPS51393P**	**SYV768BRAC**
EN	PR0502	0ohm_5%_0201	1k_5%_0201
EN-ENLDO	PR0510	NO_ASM	0ohm_5%_0201
ENLDO	PR0504	0ohm_5%_0201	NO_ASM
VCC	PC0512	1uF_6.3V_X5R_0201	2.2uF_6.3V_X5R_0201
BST	PC0501	0.22uF_25V_X5R_0402	0.1uF_25V_X5R_0402
FB	PR0501	240k_5%_0201	1k_5%_0201

LOGIC

Document Number

Size	Title	Rev
Custom	**105_DC/DC VCC3M (TPS51393P)**	0.01

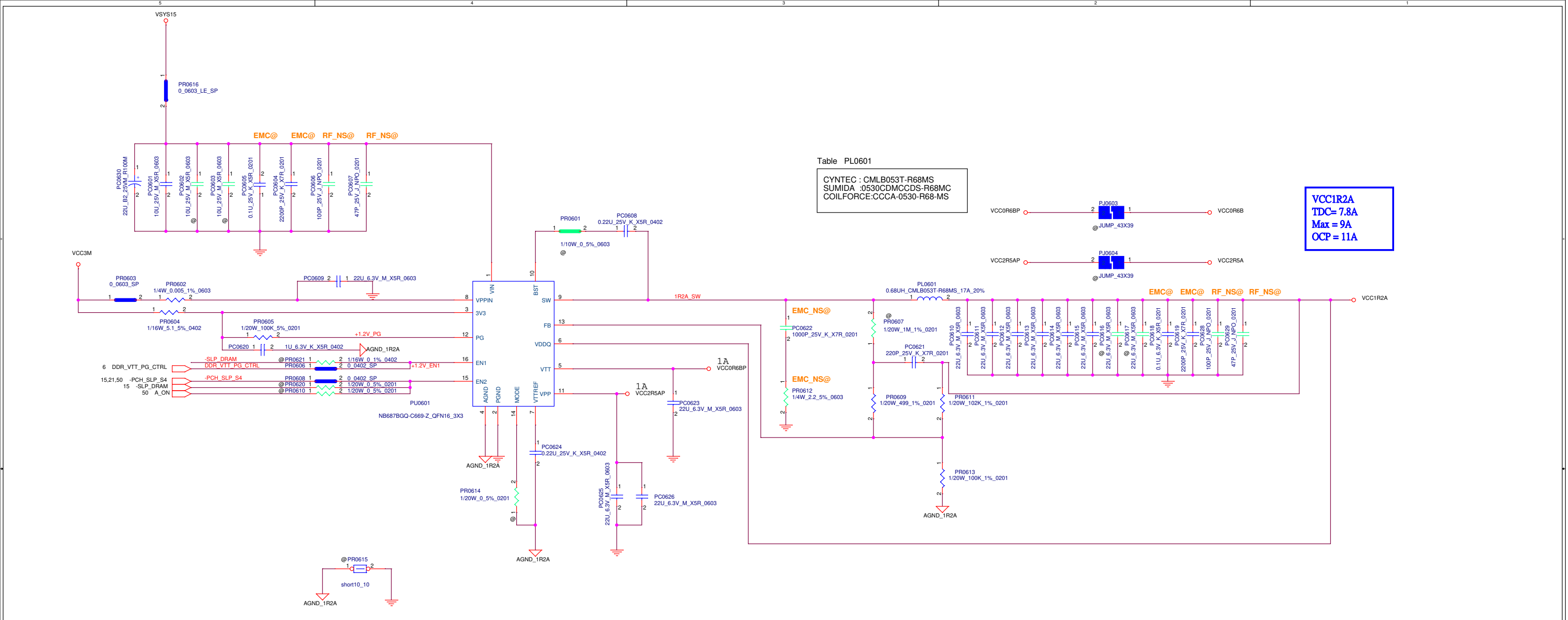


TABLE NB687GQ:EN1/EN2

State	EN1	EN2	VDDQ	VTTREF	VTT	VPP
S0	High	High	ON	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)	ON
S4/S5	Low	Low	OFF	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF	OFF

TABLE NB687GQ:MODE

State	USM	Fs	Resistor to GND
M1	NO	700KHz	0
M2	YES	700KHz	90K
M3	NO	500KHz	150K
M4	YES	500KHz	>230K or Float

Document Number

LCFC

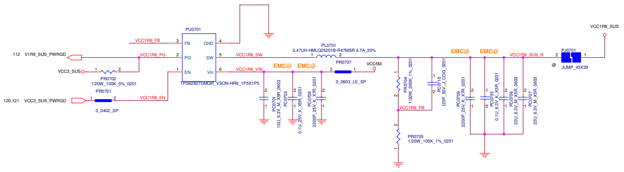
Size Custom | Title **106_DC/DC VCC1R2A/(NB687GQ-Z** | Rev 0.01

Date: Tuesday, January 04, 2022 | Sheet 106 of 130

Table PL0701

MURATA	: DFE252012F-R47M-P2
CYNTEC	: HMLQ25201B-R47MSR
SUMIDA	: 252012CDMCDDS-R47MC

VCC1R8_SUS
Imax= 3A



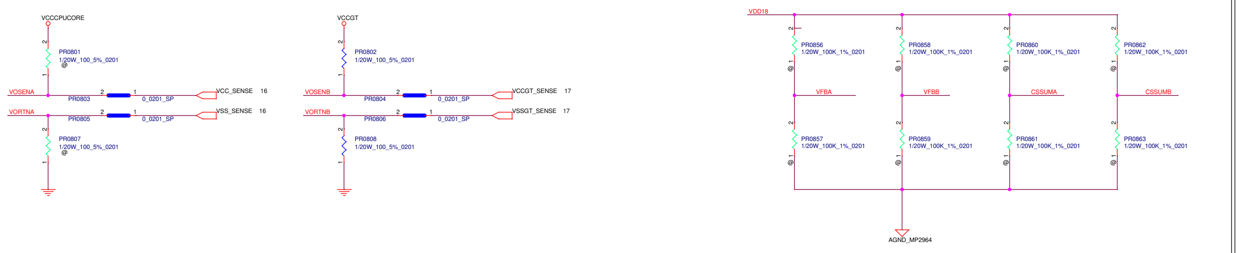
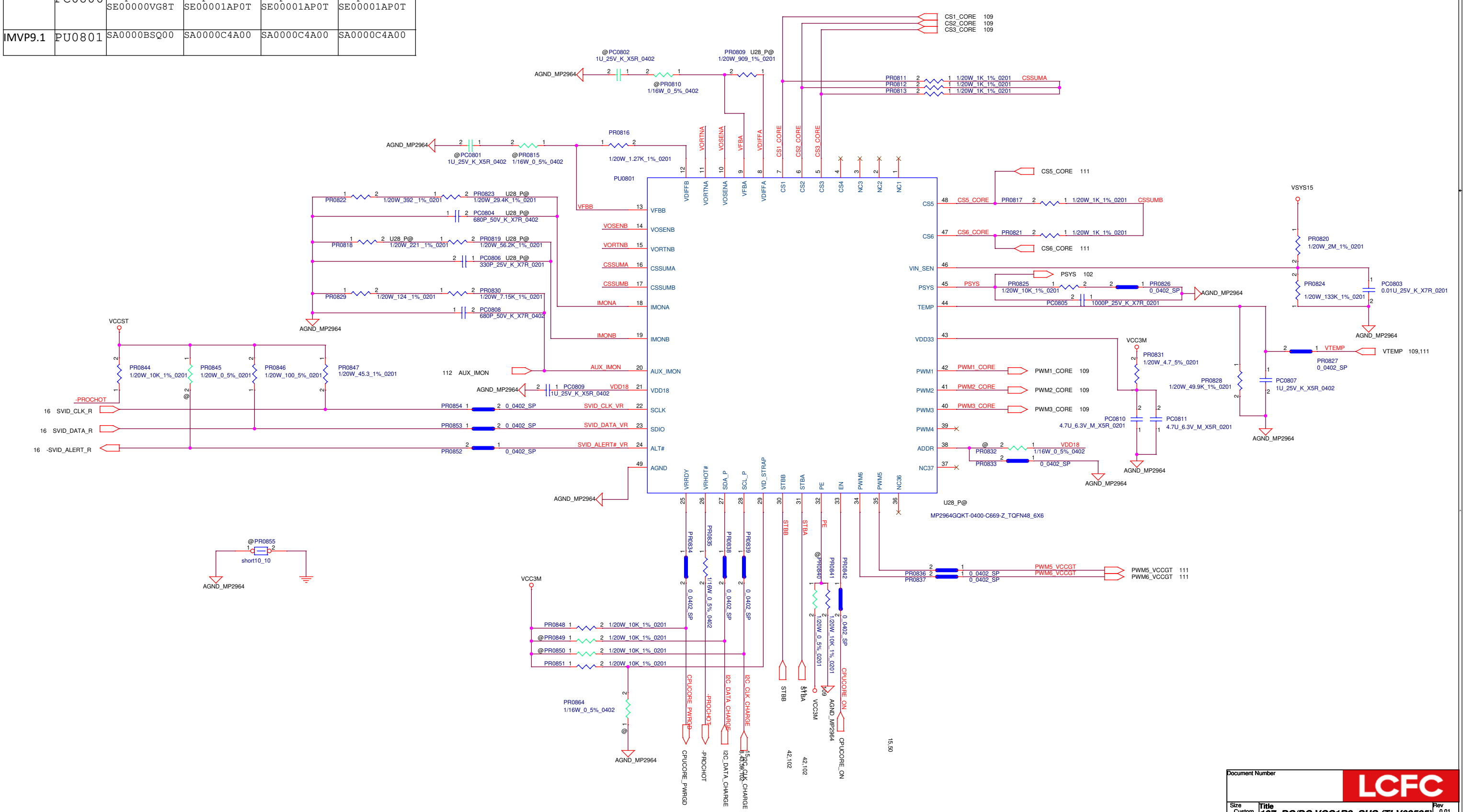


TABLE:MP2964 LL& IMON setting

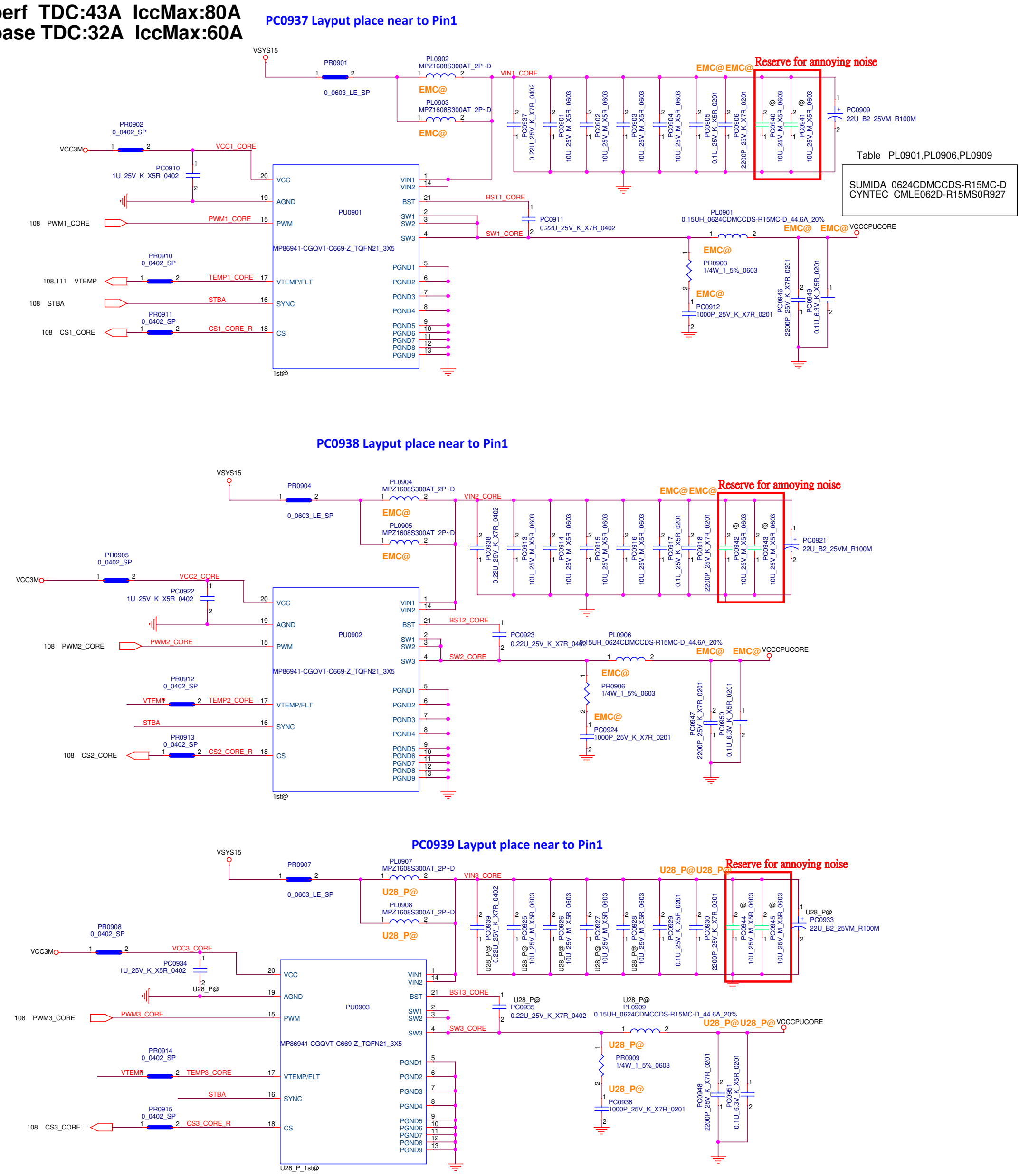
		28W Perf.	28W Base	15W Perf.	15W Base
VCORE LL	PR0809	887_1% SD00001B00T	887_1% SD00001B00T	1.1K_1% SD000018H0T	1.1K_1% SD000018H0T
VCORE IMON	PR0823 PR0822	29.8K_1%	38.8K_1% SD00001378T	38.8K_1% SD00001378T	38.8K_1% SD00001378T
	PC0804	680P SE074681K0T	680P SE074681K0T	680P SE074681K0T	680P SE074681K0T
VCCGT IMON	PR0819 PR0818	56.4K_1%	66.5K_1% SD00001MA0T	66.5K_1% SD00001MA0T	66.5K_1% SD00001MA0T
	PC0806	330p SE00000VG8T	270p SE00001AP0T	270p SE00001AP0T	270p SE00001AP0T
IMVP9.1	PU0801	SA0000BSQ00	SA0000C4A00	SA0000C4A00	SA0000C4A00



Document Number		LCFC
Size Custom	Title 107_DC/DC VCC1R8_SUS (TLV62585)	Rev 0.01
Date: Tuesday, January 04, 2022	Sheet 108 of 130	

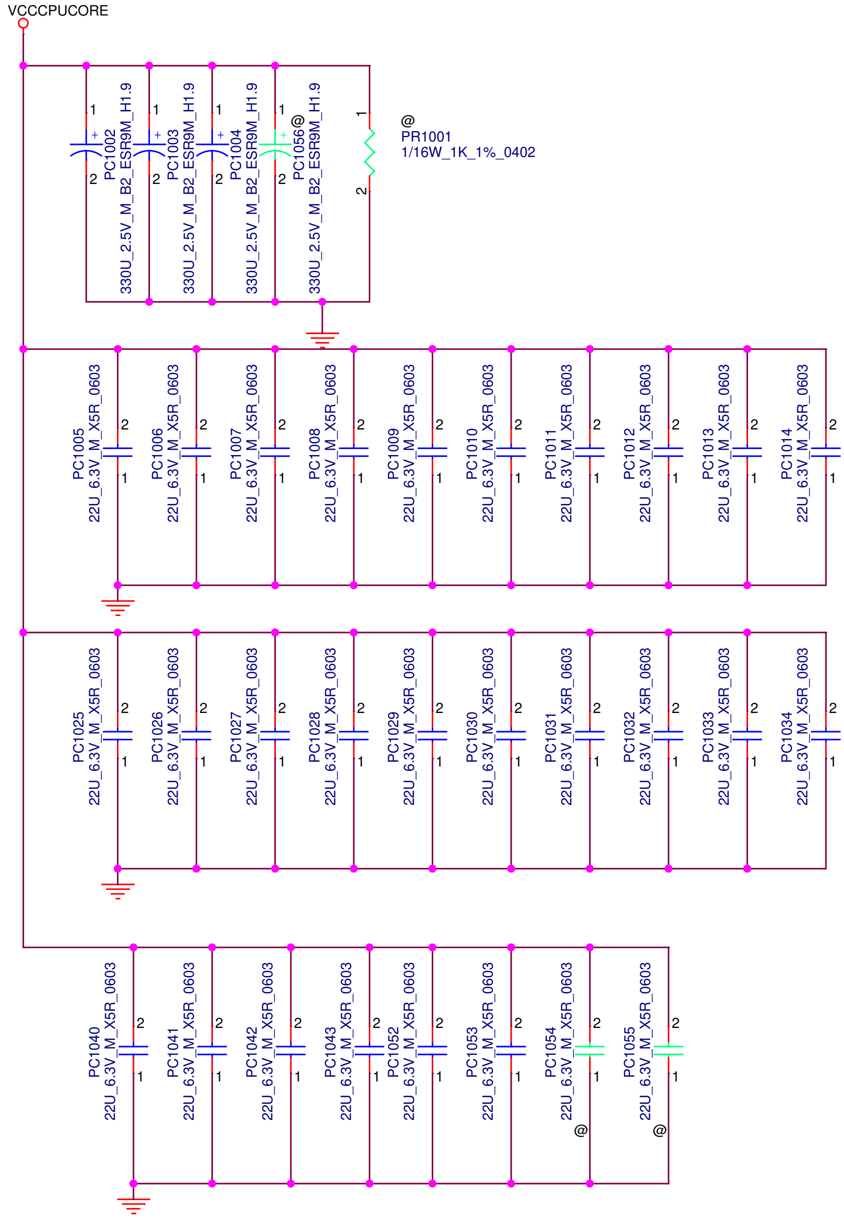
Vcore: PWM1/2/3

28W perf TDC:63A IccMax:109A
28W Base TDC:47A IccMax:80A
15W perf TDC:43A IccMax:80A
15W base TDC:32A IccMax:60A



Document Number		
Size: Custom	Title: 109_DC/DC_VCCCPUCORE(MP86971)	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 109 of 130	

LCFC

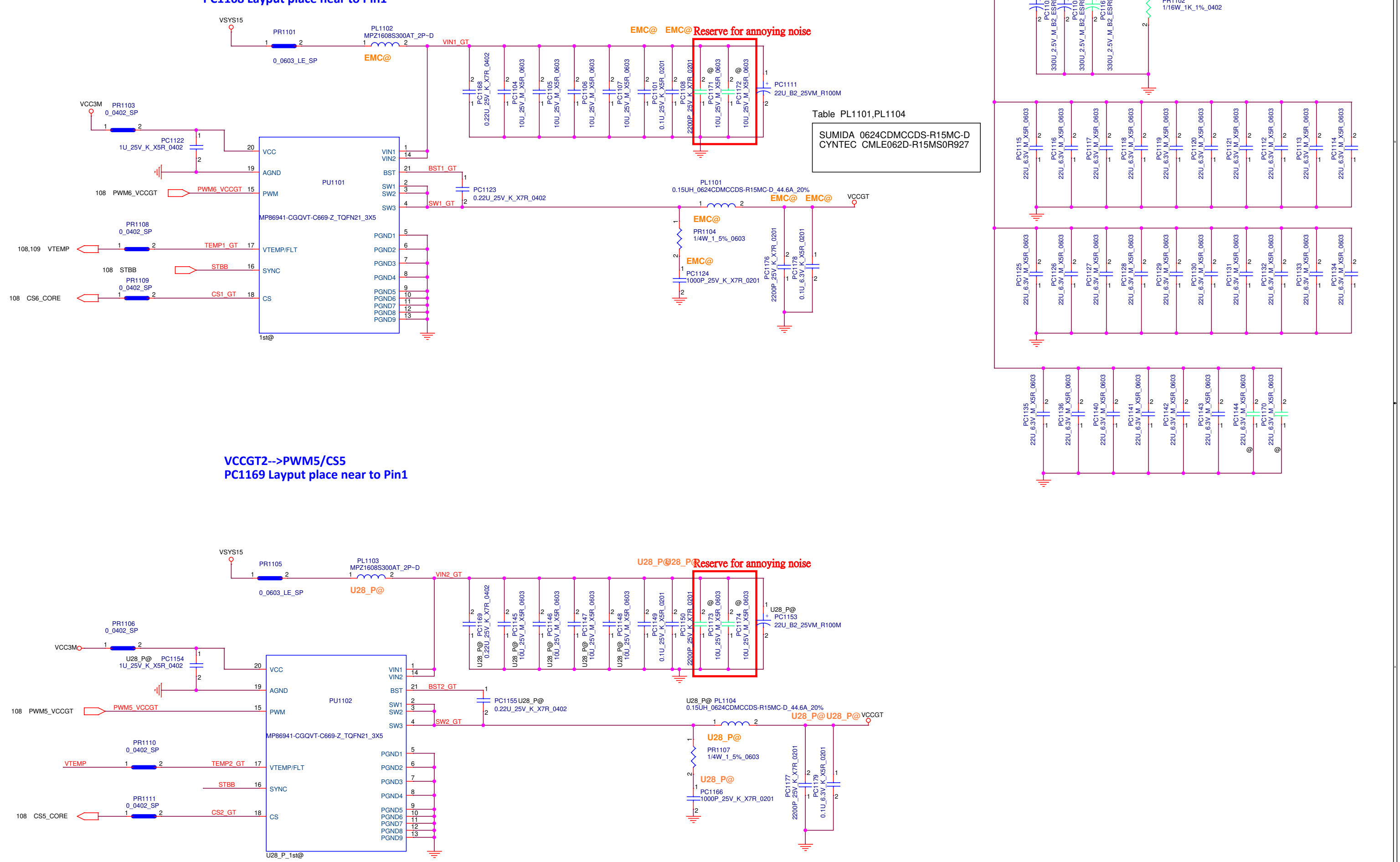


Document Number		LCFC
Size Custom	Title 110_DC/DC VCCCPUCORE_DE_CAP	Rev 0.01
Date:	Tuesday, January 04, 2022	Sheet 110 of 130

VccGT: PWM6/5
28W performance TDC:30A IccMax:50A
28W Base/15W performance/15W base TDC:23A IccMax:40A

VCCGT1-->PWM6/CS6
PC1168 Laypout place near to Pin1

VCCGT2-->PWM5/CS5
PC1169 Laypout place near to Pin1



Document Number	LCFC
Size: C	Title: 111_DC/DC VCCGT(MP86943
Rev	0.01
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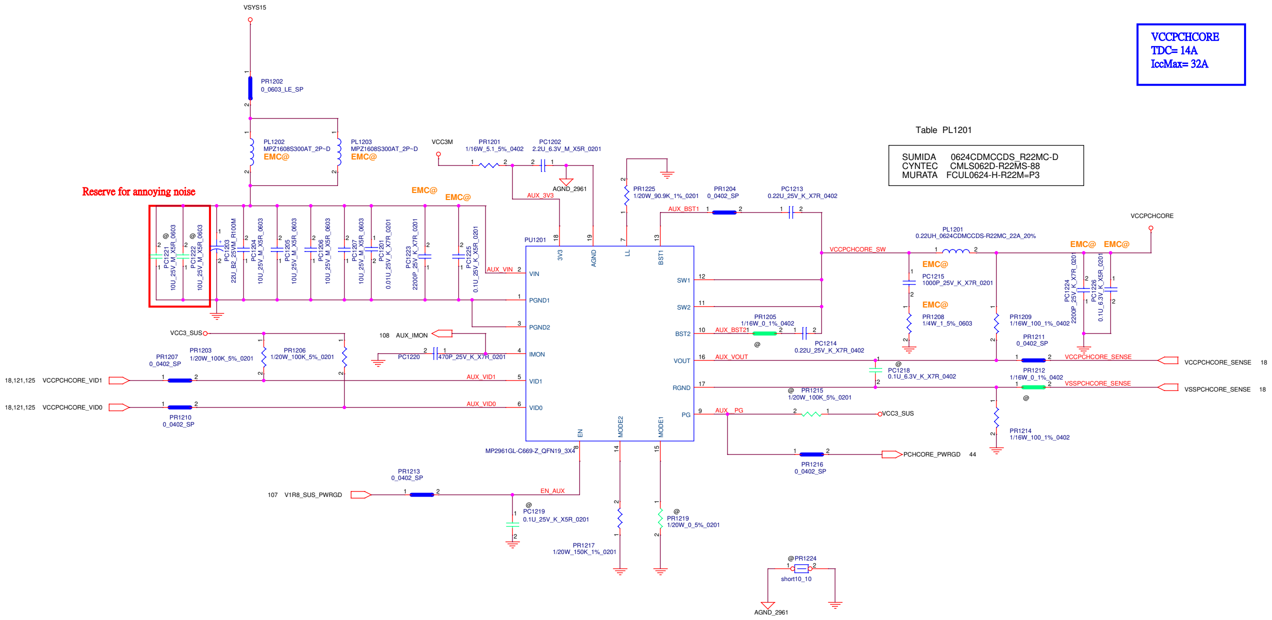

TABLE:MODE2 select

State	FS(KHz)	CLM	Resistor to GND
M1	800	12A	0
M2	1200	12A	90K
M3	800	17A	150K
M4	1200	17A	>230K or float

Logic →

TABLE:LL

State	Load Line	Resistor to GND
M1	1m	0
M2	1.5m	90K
M3	2m	150K
M4	2.5m	>230K or float

← Logic

TABLE:MODE1 select

State	Interleaving	VID Down option	Resistor to GND
M1	No	Slew down	0
M2	Yes	Slew down	90K
M3	Yes	Decay	150K
M4	No	Decay	>230K or float

Logic →

TABLE : VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Document Number	
Size: Custom	Title: 112_DC/DC VCCPCHCORE(MP2961
Rev	0.01
Date:	Tuesday, January 04, 2022
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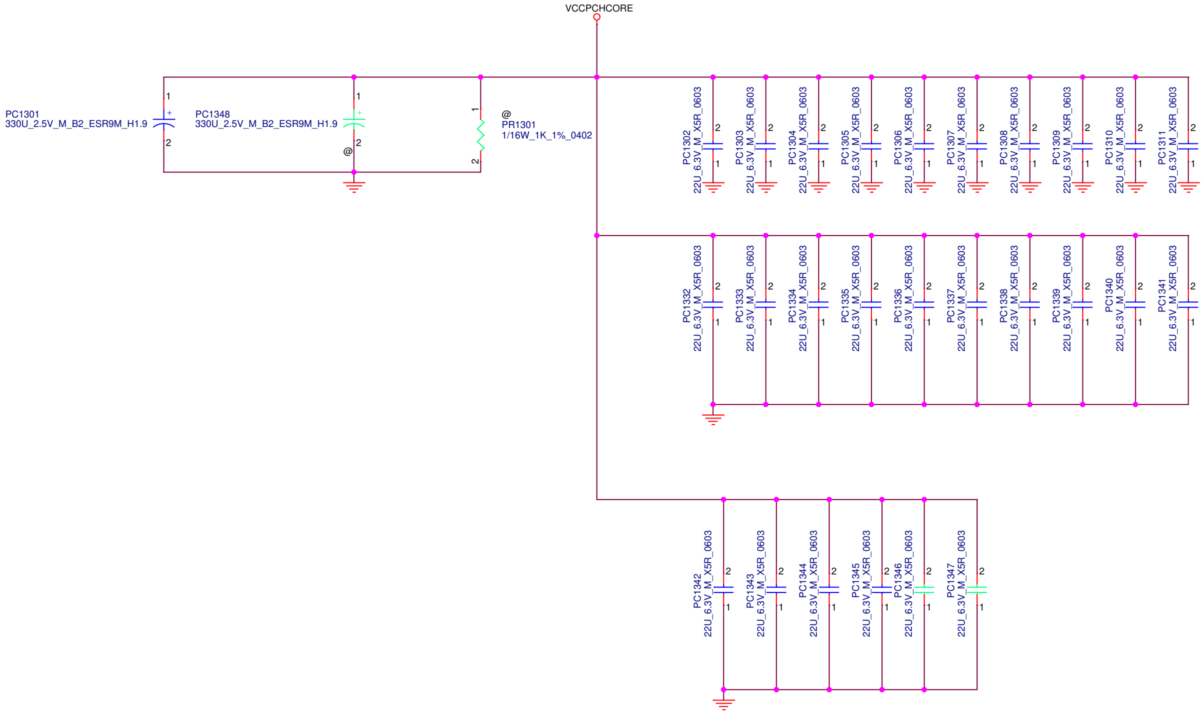

Document Number			LCFC
Size Custom	Title 113_DC/DC VCCPCHCORE DE_CAP		Rev 0.01
Date:	Tuesday, January 04, 2022	Sheet 113 of 130	

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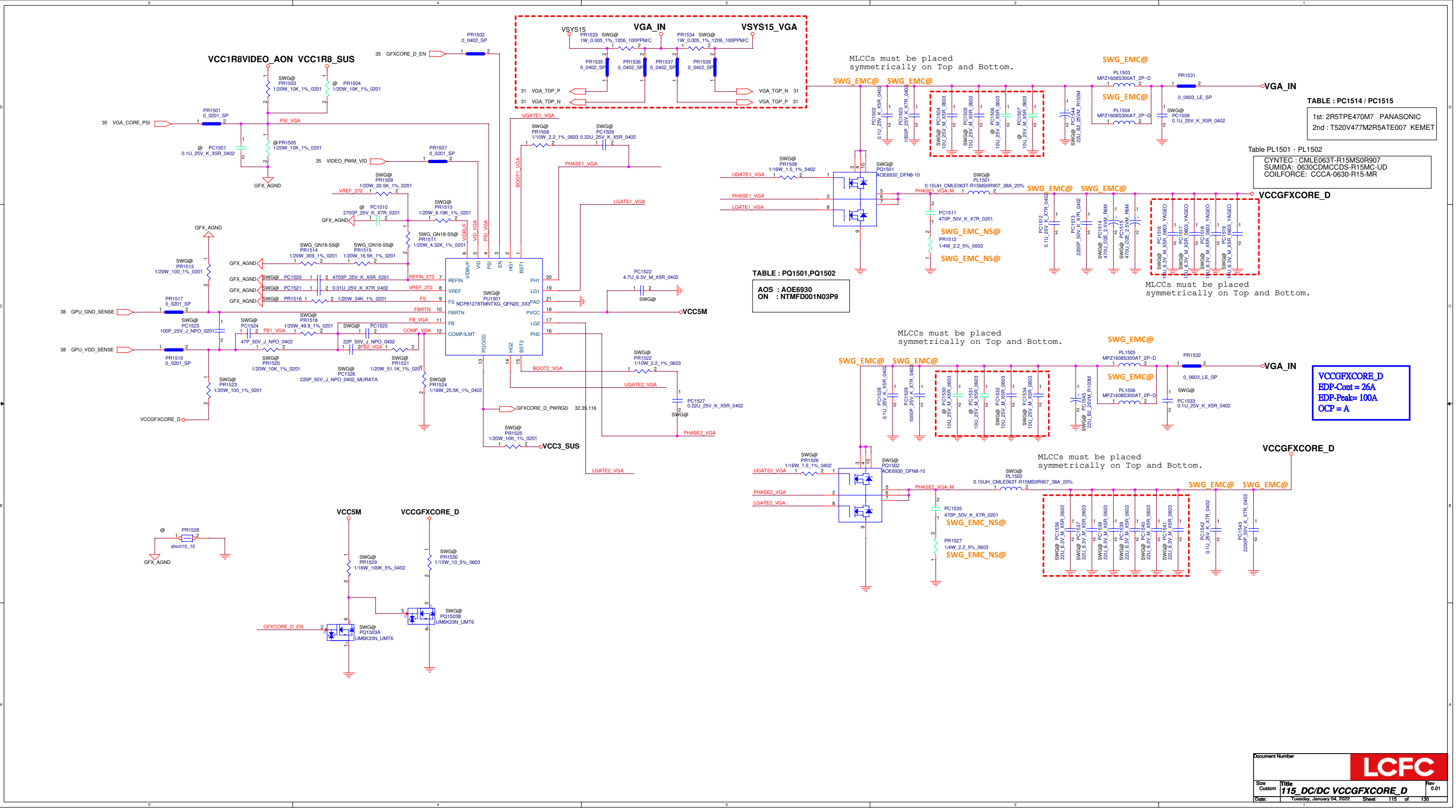
Document Number		LCFC
Size Custom	Title 114_BLANK	Rev 0.01
Date:	Tuesday, January 04, 2022	Sheet 114 of 130


VGA_IN
VSYS15_VGA
VSYS15
VCC1R8VIDEO_AON
VCC1R8_SUS
GFXCORE_D_EN
VGA_CORE_PSI
VIDEO_PWM_VID
GPU_GND_SENSE
GPU_VDD_SENSE
VCCGFXCORE_D
GFX_AGND
VCC5M
VCC3_SUS
GFXCORE_D_PWRGD
NCP81278TMNTXG_QFN20_3X3
MLCCs must be placed symmetrically on Top and Bottom.
SWG_EMC@
SWG_EMC_NS@
TABLE : PC1514 / PC1515
1st: 2R5TPE470M7 PANASONIC
2nd : T520V477M2R5ATE007 KEMET
Table PL1501 - PL1502
CYNTEC : CMLE063T-R15MS0R907
SUMIDA: 0630CDMCCDS-R15MC-UD
COILFORCE: CCCA-0630-R15-MR
TABLE : PQ1501,PQ1502
AOS : AOE6930
ON : NTMFD001N03P9
VCCGFXCORE_D
EDP-Cont = 26A
EDP-Peak= 100A
OCP = A
LCFC
Document Number
Title
115_DC/DC VCCGFXCORE_D
Size Custom
Rev 0.01
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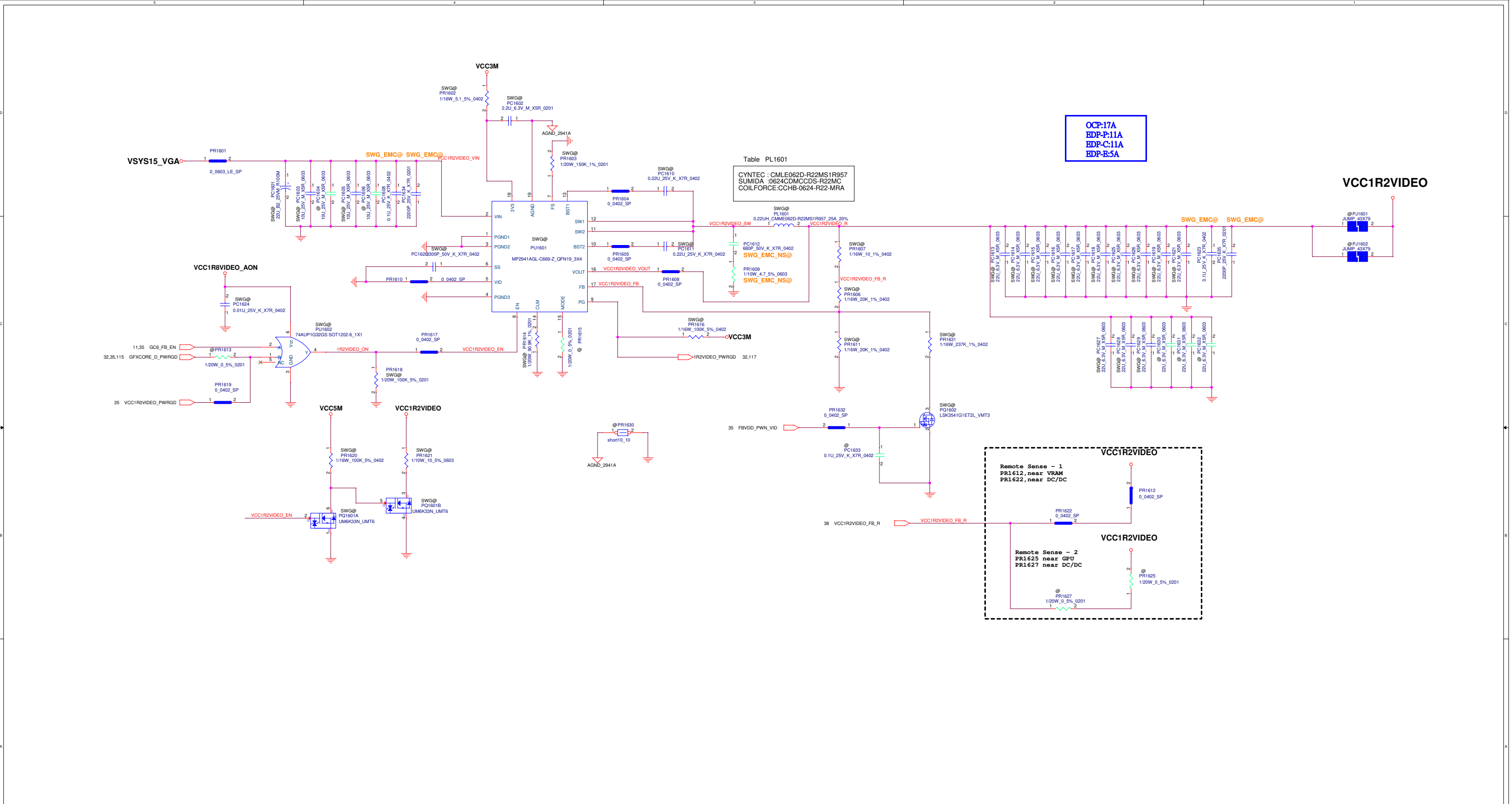


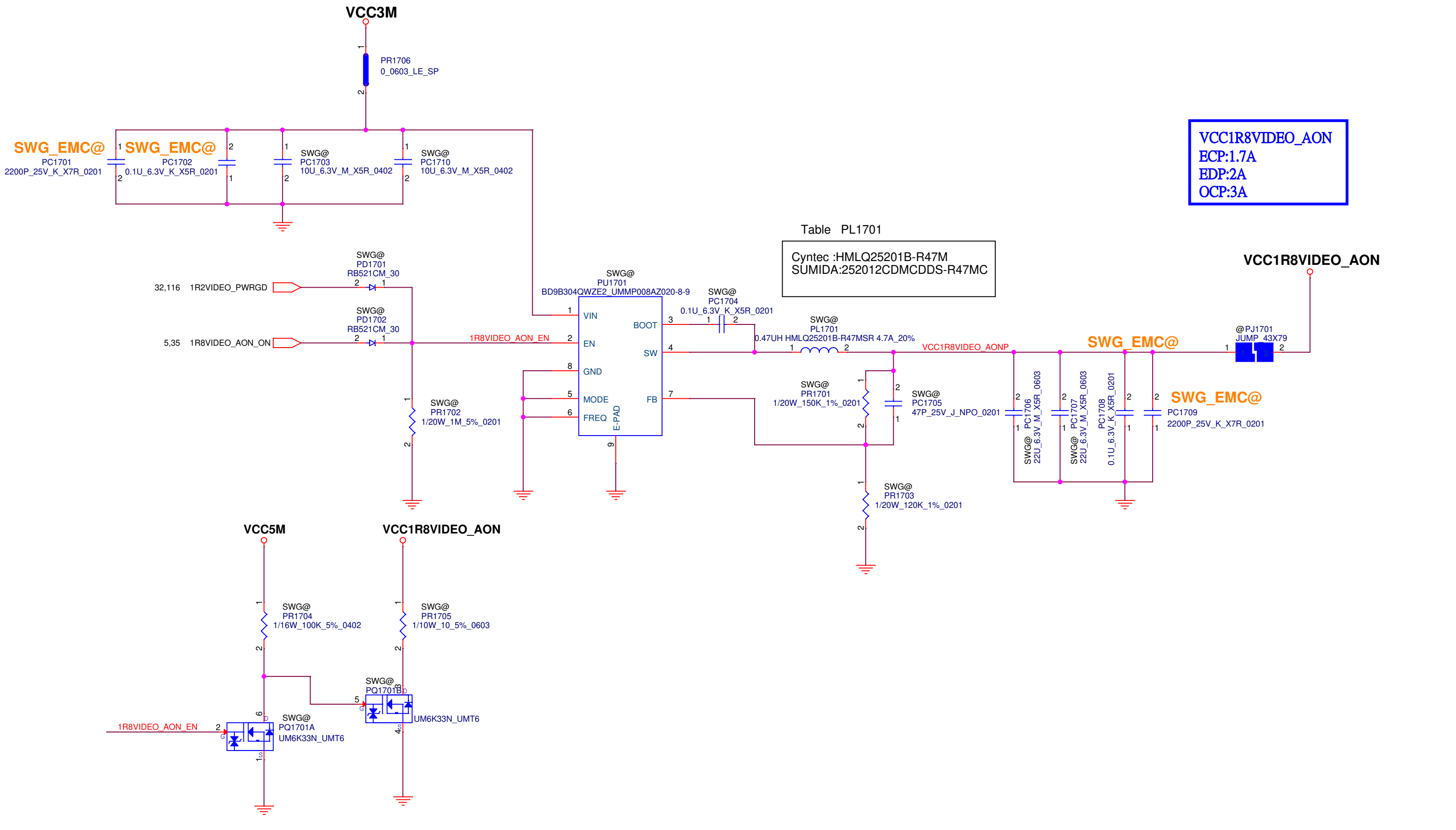
Document Number

LCFC

Title: 116_DC/DC VCC1R2VIDEO(MP2941A)

Size: Custom

Date: Tuesday, January 04, 2022 Sheet 116 of 130



Document Number		LCFC
Size Custom	Title 117_DC/DC VCC1R8VIDEO	Rev 0.01
Date: Tuesday, January 04, 2022	Sheet 117 of 130	

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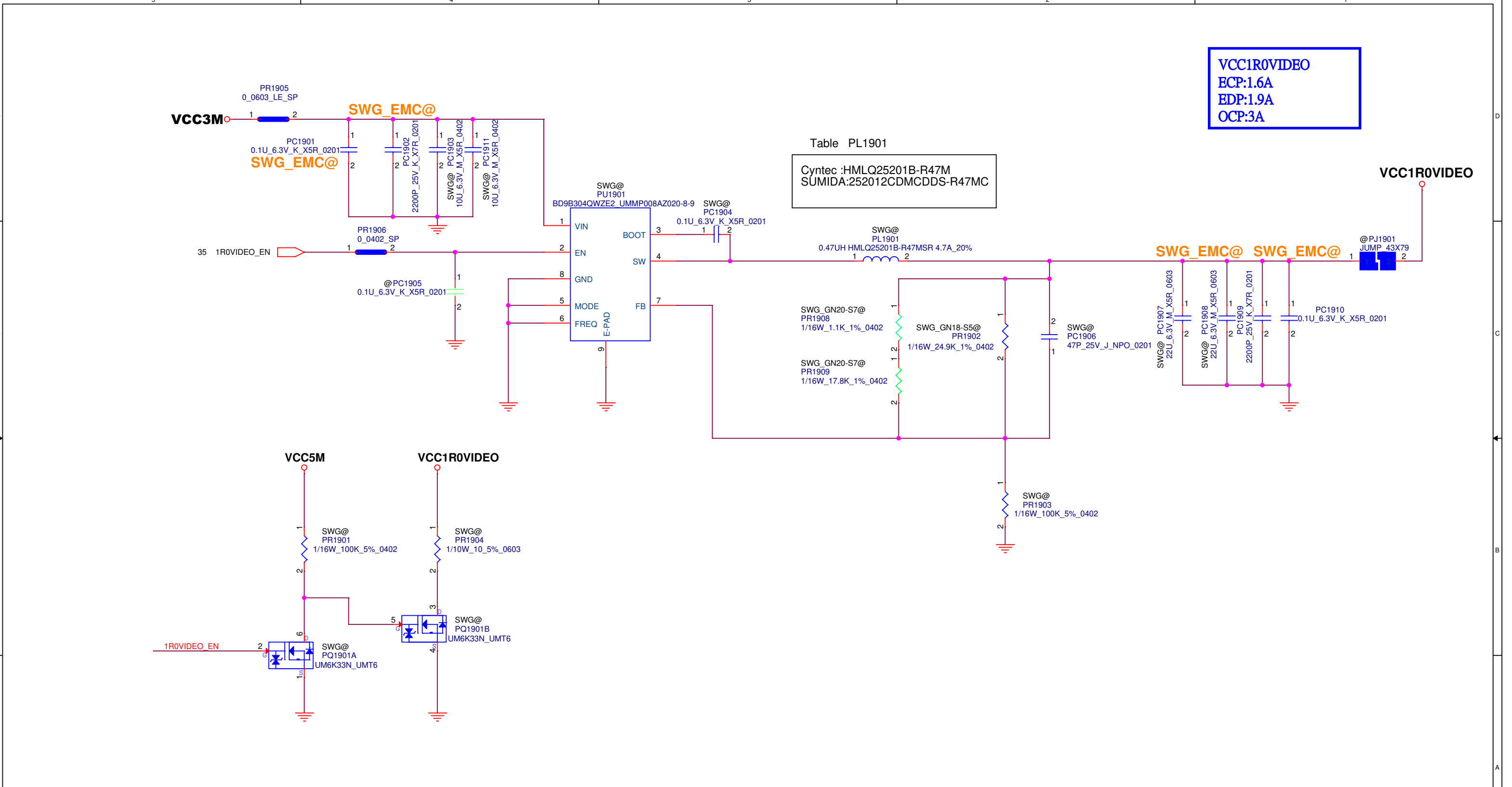
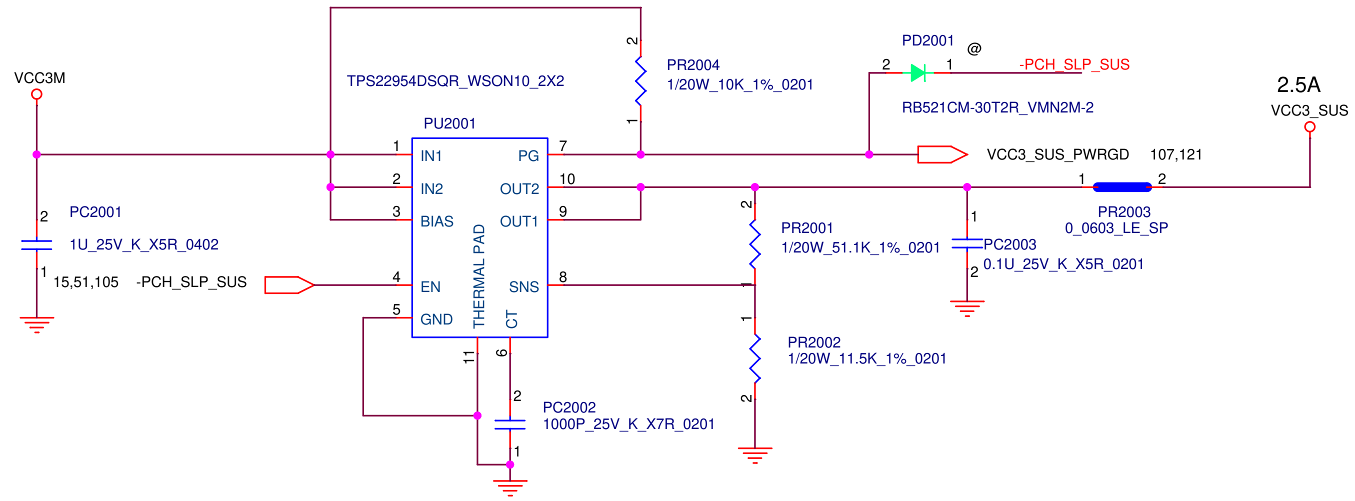
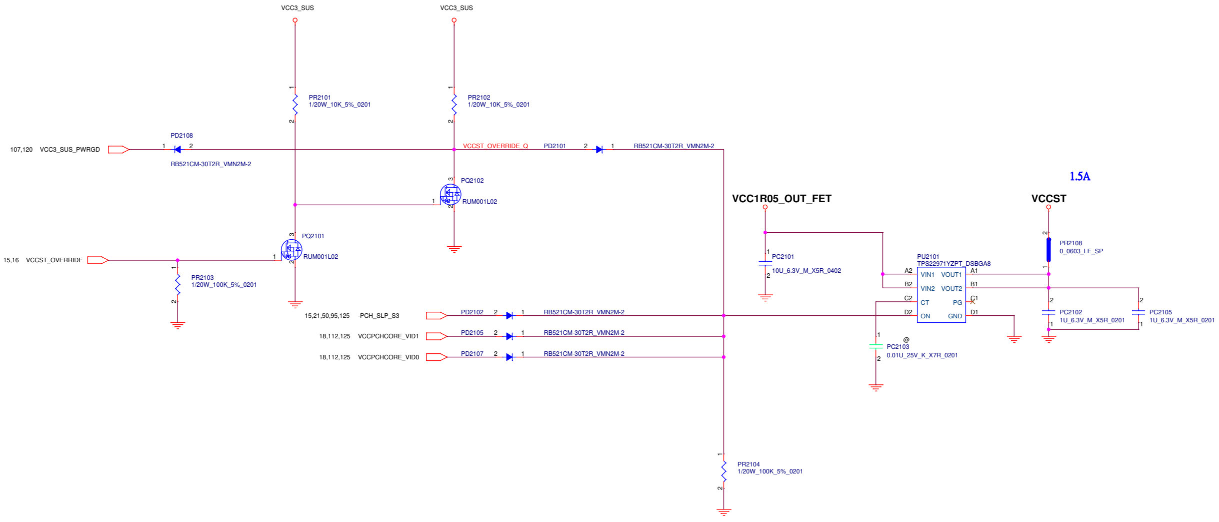
Document Number	
Size: A	Title: *118_BLANK*	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 118 of 130



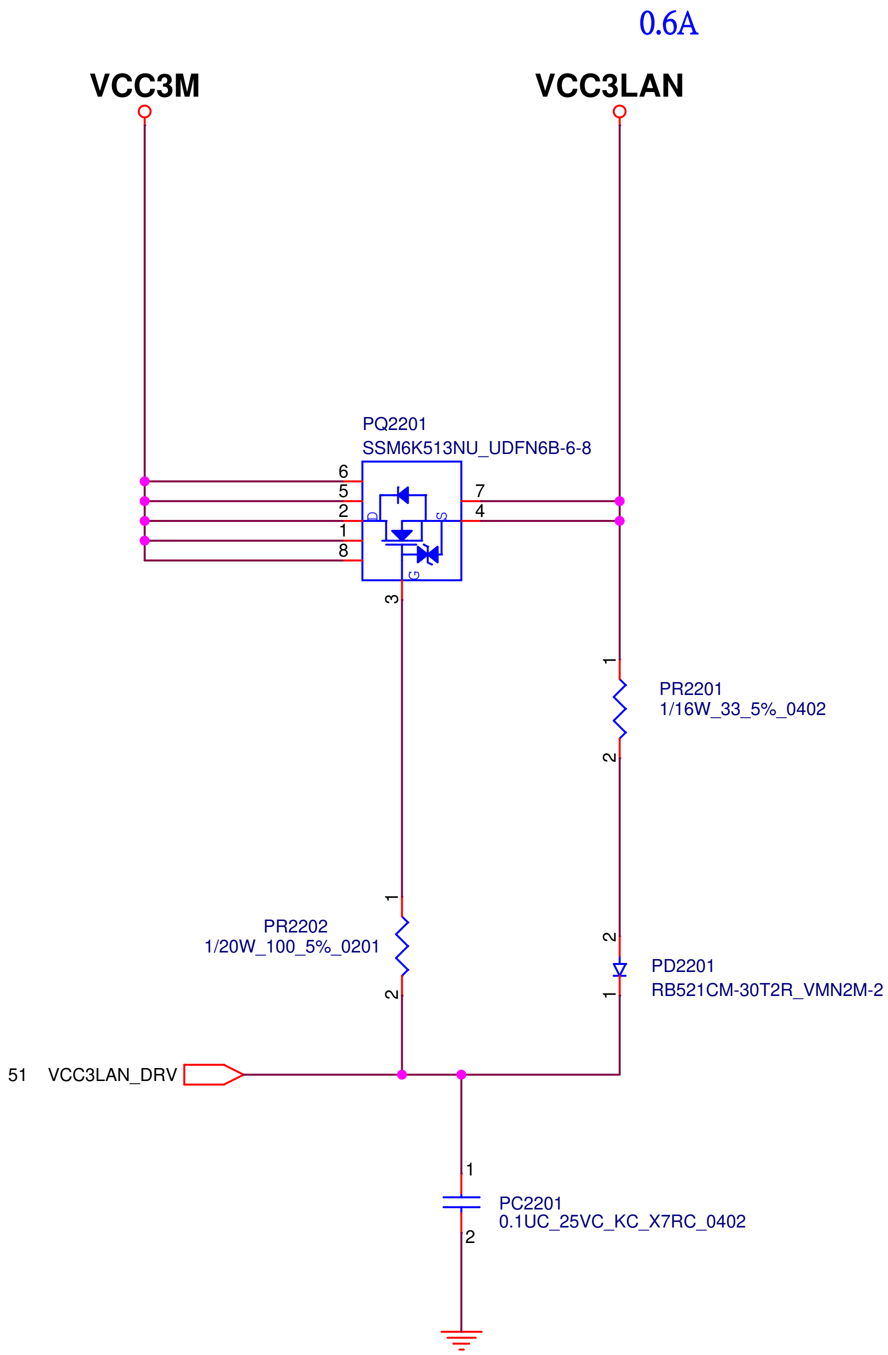
Document Number		LCFC
Size: Custom	Title: 119_DC/DC VCC1R0VIDEO	Rev: 0.01
Date: Tuesday, January 04, 2022	Sheet 119 of 130	



Document Number	LCFC	
Size A	Title **120_LOAD SW VIDEO**	Rev 0.01
Date:	Tuesday, January 04, 2022	Sheet 120 of 130



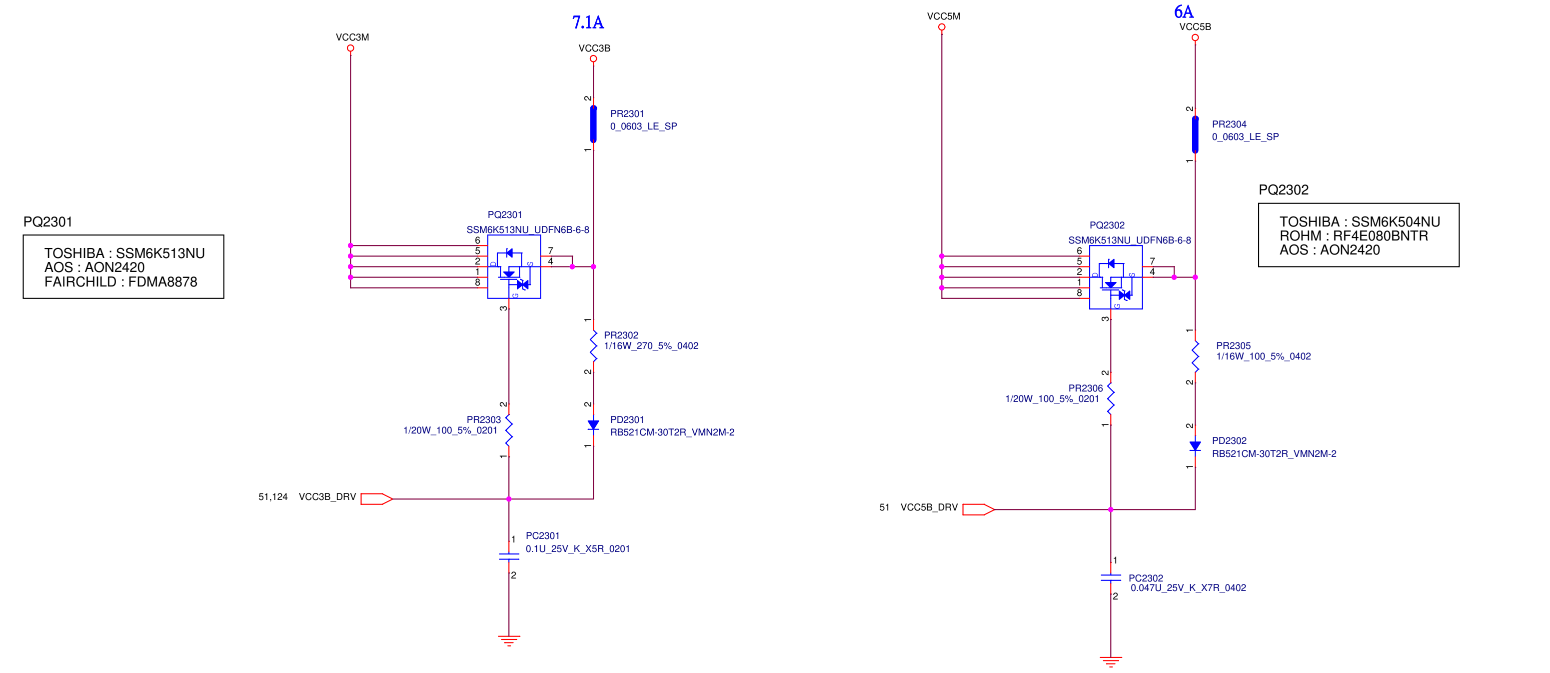
Document Number		LCFC	
Size Custom	Title 121_LOAD SW VCCST & VCCSTG		Rev 0.01
Date:	Tuesday, January 04, 2022	Sheet 121 of 130	



Document Number

LCFC

Size	Title	Rev
Custom	122_LOAD SW LAN	0.01
Date:	Tuesday, January 04, 2022	Sheet 122 of 130



Document Number	LCFC	
Size: Custom	Title: 123_LOAD SW B	Rev: 0.01
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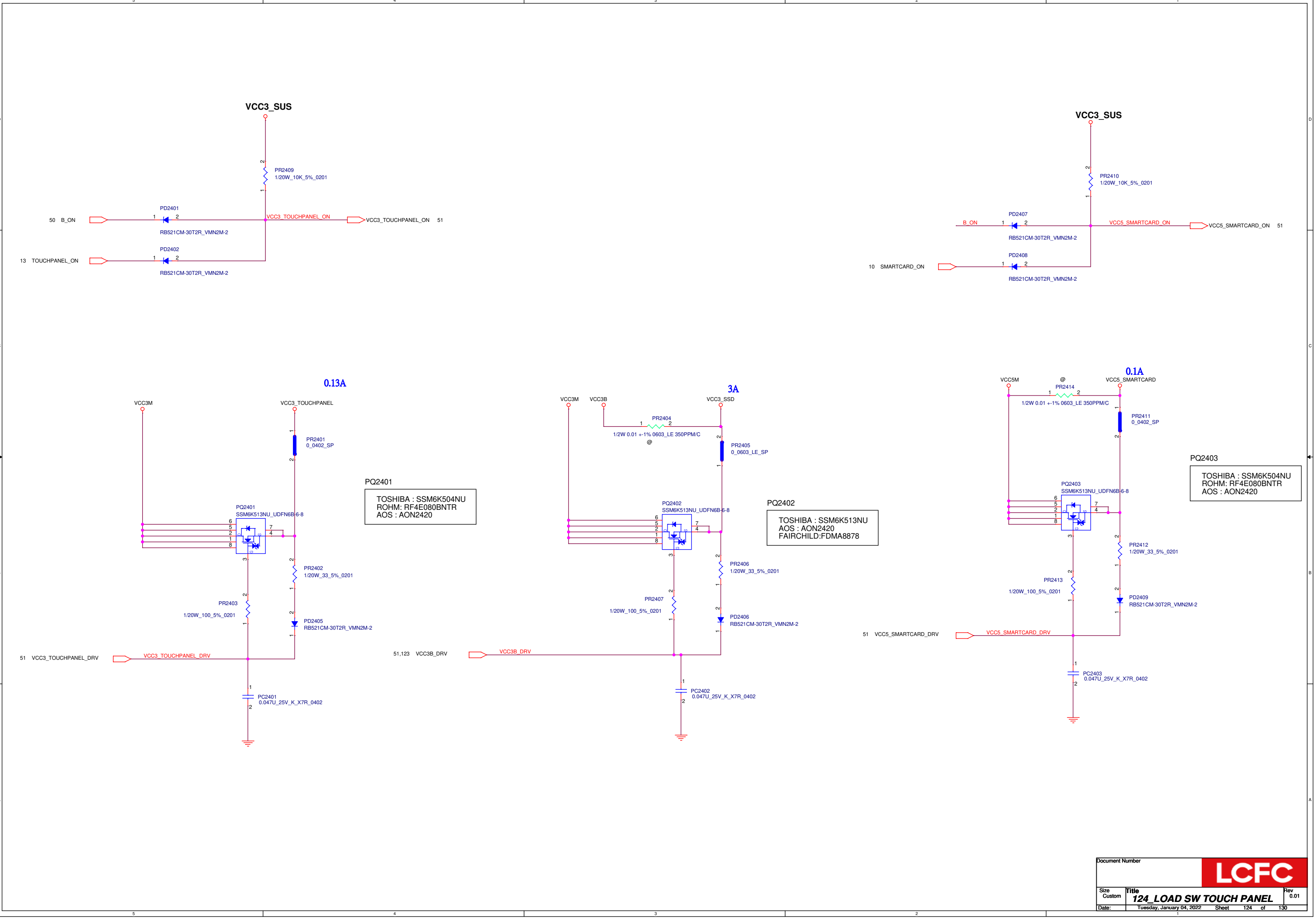

VCC3_SUS
PR2409
1/20W_10K_5%_0201
50 B_ON
PD2401
RB521CM-30T2R_VMN2M-2
VCC3_TOUCHPANEL_ON
VCC3_TOUCHPANEL_ON 51
13 TOUCHPANEL_ON
PD2402
RB521CM-30T2R_VMN2M-2
VCC3_SUS
PR2410
1/20W_10K_5%_0201
B_ON
PD2407
RB521CM-30T2R_VMN2M-2
VCC5_SMARTCARD_ON
VCC5_SMARTCARD_ON 51
10 SMARTCARD_ON
PD2408
RB521CM-30T2R_VMN2M-2
0.13A
VCC3M
VCC3_TOUCHPANEL
PR2401
0_0402_SP
PQ2401
TOSHIBA : SSM6K504NU
ROHM: RF4E080BNTR
AOS : AON2420
PQ2401
SSM6K513NU_UDFN6B-6-8
PR2402
1/20W_33_5%_0201
PR2403
1/20W_100_5%_0201
PD2405
RB521CM-30T2R_VMN2M-2
51 VCC3_TOUCHPANEL_DRV
VCC3_TOUCHPANEL_DRV
PC2401
0.047U_25V_K_X7R_0402
3A
VCC3M
VCC3B
VCC3_SSD
PR2404
1/2W 0.01 +-1% 0603_LE 350PPM/C
@
PR2405
0_0603_LE_SP
PQ2402
SSM6K513NU_UDFN6B-6-8
PQ2402
TOSHIBA : SSM6K513NU
AOS : AON2420
FAIRCHILD:FDMA8878
PR2406
1/20W_33_5%_0201
PR2407
1/20W_100_5%_0201
PD2406
RB521CM-30T2R_VMN2M-2
51,123 VCC3B_DRV
VCC3B_DRV
PC2402
0.047U_25V_K_X7R_0402
0.1A
VCC5M
@
PR2414
VCC5_SMARTCARD
1/2W 0.01 +-1% 0603_LE 350PPM/C
PR2411
0_0402_SP
PQ2403
TOSHIBA : SSM6K504NU
ROHM: RF4E080BNTR
AOS : AON2420
PQ2403
SSM6K513NU_UDFN6B-6-8
PR2412
1/20W_33_5%_0201
PR2413
1/20W_100_5%_0201
PD2409
RB521CM-30T2R_VMN2M-2
51 VCC5_SMARTCARD_DRV
VCC5_SMARTCARD_DRV
PC2403
0.047U_25V_K_X7R_0402
Document Number
LCFC
Size Custom
Title
124_LOAD SW TOUCH PANEL
Rev 0.01
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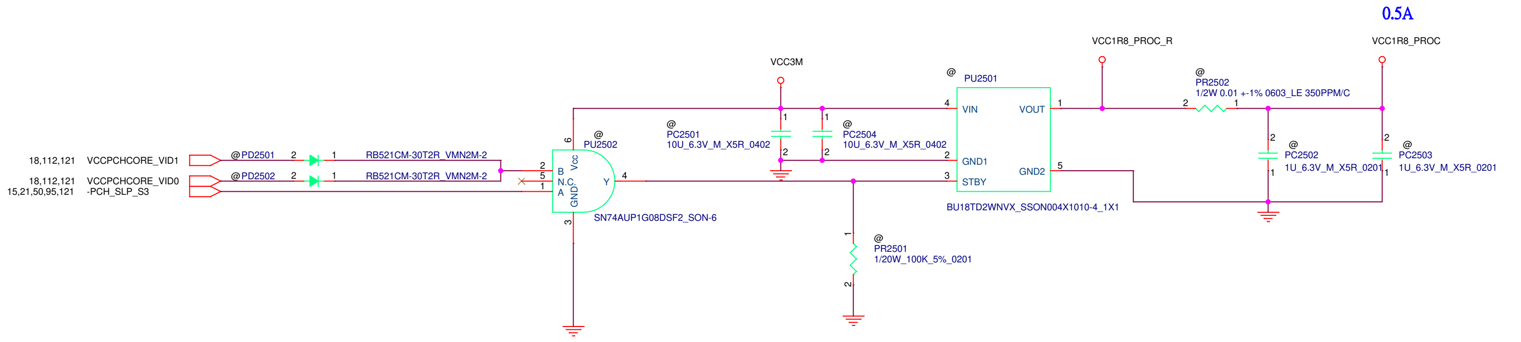

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Size: Custom	Title: **125_VCC1R8_PROC**		Rev: 0.01
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Document Number	
	LCFC

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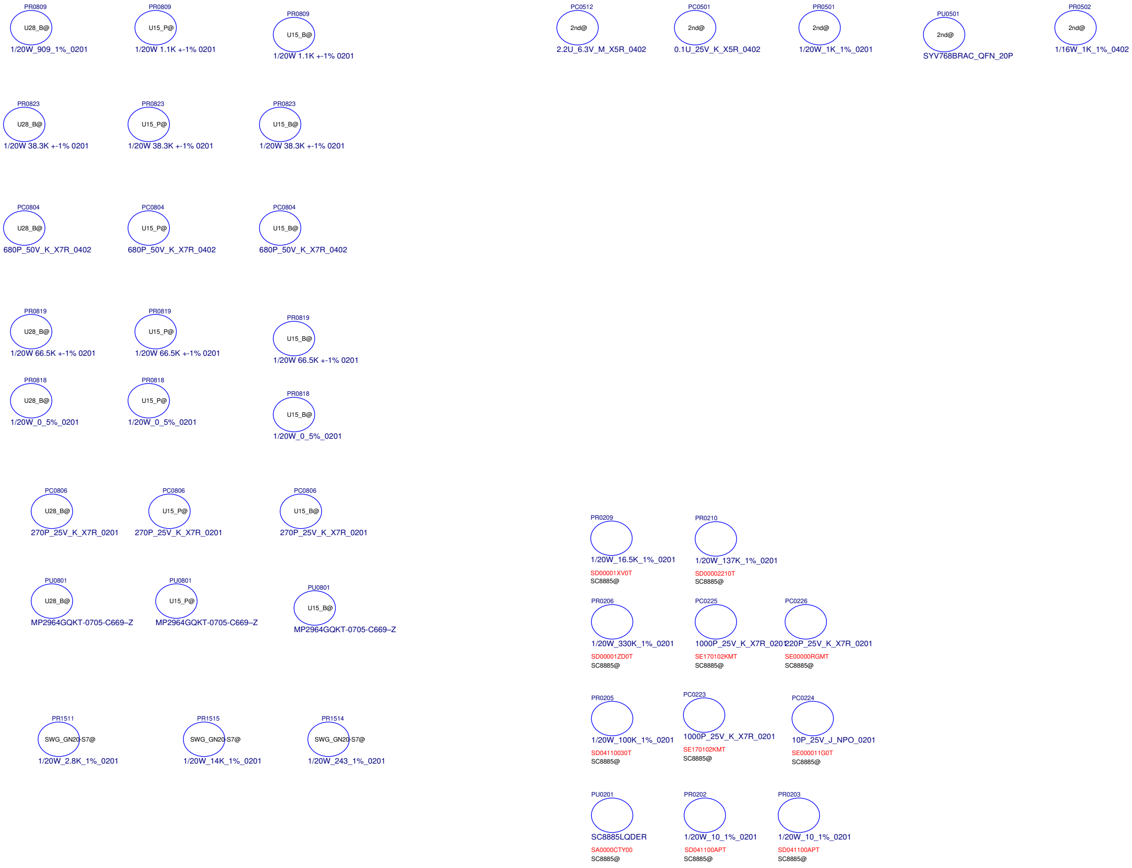

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Size Custom	Title **_127_BLANK_**	Rev 0.01
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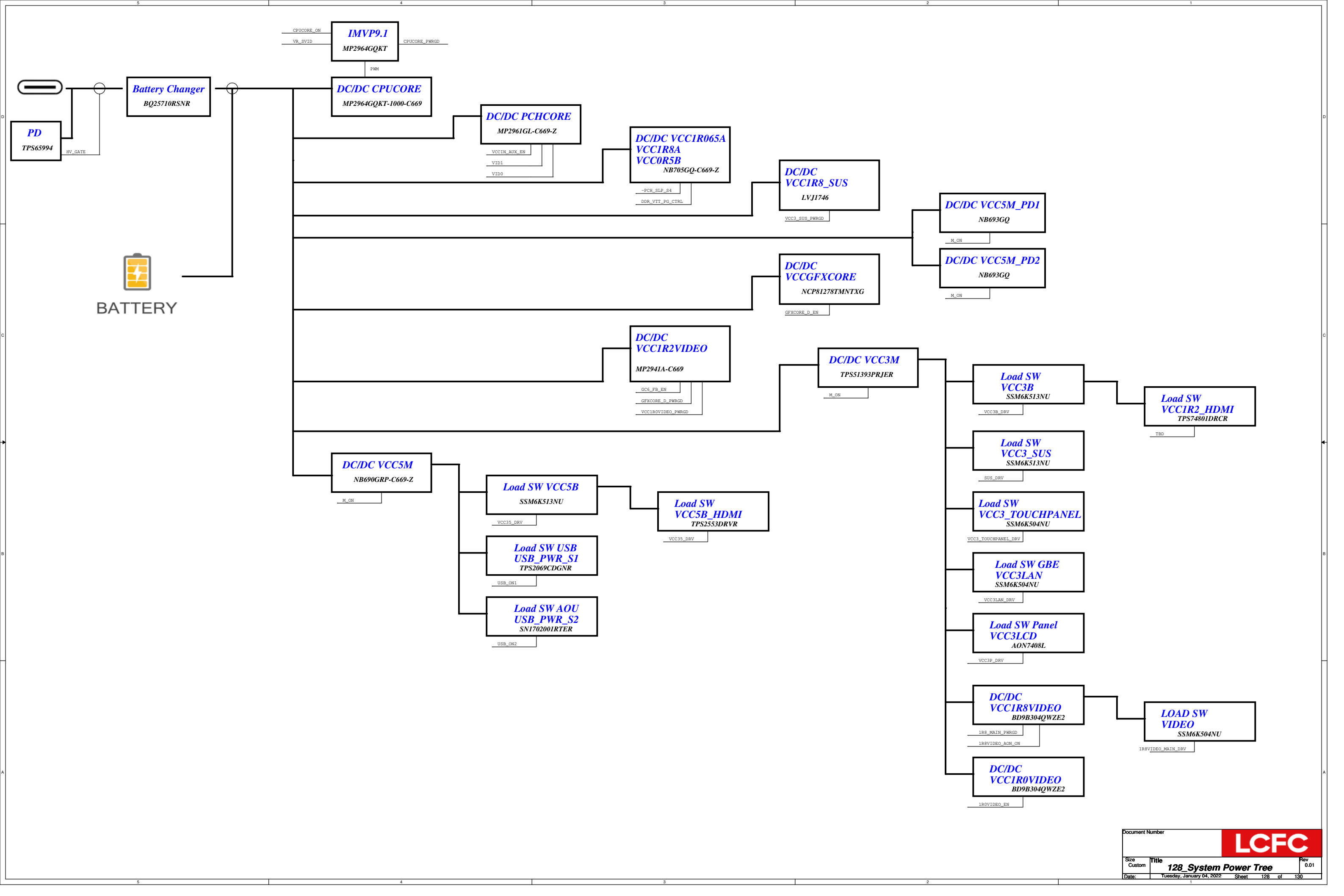
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MP2964GQKT
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VR_SVID
CPUCORE_PWRGD
PWM
PD
TPS65994
BV_GATE
Battery Changer
BQ25710RSNR
BATTERY
DC/DC CPUCORE
MP2964GQKT-1000-C669
DC/DC PCHCORE
MP2961GL-C669-Z
VCCIN_AUX_EN
VID1
VID0
DC/DC VCC1R065A
VCC1R8A
VCC0R5B
NB705GQ-C669-Z
~PCH_SLP_S4
DDR_VTT_PG_CTRL
DC/DC
VCC1R8_SUS
LVJ1746
VCC3_SUS_PWRGD
DC/DC VCC5M_PD1
NB693GQ
M_ON
DC/DC VCC5M_PD2
NB693GQ
M_ON
DC/DC
VCCGFXCORE
NCP81278TMNTXG
GFXCORE_D_EN
DC/DC
VCC1R2VIDEO
MP2941A-C669
GC6_FB_EN
GFXCORE_D_PWRGD
VCC1R0VIDEO_PWRGD
DC/DC VCC3M
TPS51393PRJER
M_ON
Load SW
VCC3B
SSM6K513NU
VCC3B_DRV
Load SW
VCC1R2_HDMI
TPS74801DRCR
TBD
Load SW
VCC3_SUS
SSM6K513NU
SUS_DRV
Load SW
VCC3_TOUCHPANEL
SSM6K504NU
VCC3_TOUCHPANEL_DRV
Load SW GBE
VCC3LAN
SSM6K504NU
VCC3LAN_DRV
Load SW Panel
VCC3LCD
AON7408L
VCC3P_DRV
DC/DC
VCC1R8VIDEO
BD9B304QWZE2
1R8_MAIN_PWRGD
1R8VIDEO_AON_ON
LOAD SW
VIDEO
SSM6K504NU
1R8VIDEO_MAIN_DRV
DC/DC
VCC1R0VIDEO
BD9B304QWZE2
1R0VIDEO_EN
DC/DC VCC5M
NB690GRP-C669-Z
M_ON
Load SW VCC5B
SSM6K513NU
VCC5S_DRV
Load SW
VCC5B_HDMI
TPS2553DRVR
VCC5S_DRV
Load SW USB
USB_PWR_S1
TPS2069CDGNR
USB_ON1
Load SW AOU
USB_PWR_S2
SN1702001RTER
USB_ON2
Document Number
LCFC
Size
Custom
Title
128_System Power Tree
Rev
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