B550M DS3H

Revision : 1.0

2015.12.30--B.L

GIGABYTE™

Title COVER SHEET		
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Model Name: B550M DS3H

Component value change history

Version: 1.0

Date	Change Item	Reason
2020.02.04	Update MA_L1 & MA_L2 Footprint	
	APU_STESYNC For HDMI AR22 PU 1K, AR21 N/A	
	Update USB Connector name	
2020.02.05	PCIEX16 Add IO_GP81 For 支援Bifurcation	
2020.02.06	Update strap table. page 9	
	LPC_CK0 Pull Down -> Up	
2020.02.07	Spec update ATX 24pin header改為空心pin	
	Add ATX -12V	
2020.02.18	Update BOM to 01A	
	Modify LED Header	
2020.03.06	Update to R0.2	
	IT5702 料號改為10HP2-NW5702-13R	
	Update LED 模組Add MCUR158,MCUR159	
2020.03.11	Q-Flash LED 改為3VDUAL	
	ADD PWM power sequence	
	Update CLK REQ & CLK 與PCIE Port 對應	
2020.03.18	IT5702 PIN7&11 Pull High 改為A_VDD18S5	
2020.03.23	Update PWM power sequence	
2020.03.27	PWM ADD SMB Switch	
	Add DAC9 close to DAQ2	
	Add DAR11,DAR12	
	Add AR130,AR131	
2020.04.08	Update to R1.0	
	ADD PCIEX16 A32 Bifurcation GPIO	
	ADD UC56	
2020.04.14	FIX Renoir APU CMOS 無法 clear issue	
	C92 & C225 改47u(0805)	
2020.04.16	FIX PWM VCCIO(PIN7) 漏電	
	FIX AUDIO 漏電 (Renoir Only)	
	Add IT5702 WTD	

Circuit or PCB layout change for next version

Date	Change Item	Reason
2020.04.20	移除PWM SMBUS switch	
2020.05.04	PCIEX16改GEN4 SLOT	
	OR40上件, For FAN ZERO	
2020.05.08	ADD ECD_Q4, DEL ECD_Q5	
2020.05.21	Update PWM 料號為10TA1-622904-08R	
2020.05.29	AR39, AR40 改為499 ohm	

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Title	BOM & PCB HISTORY	
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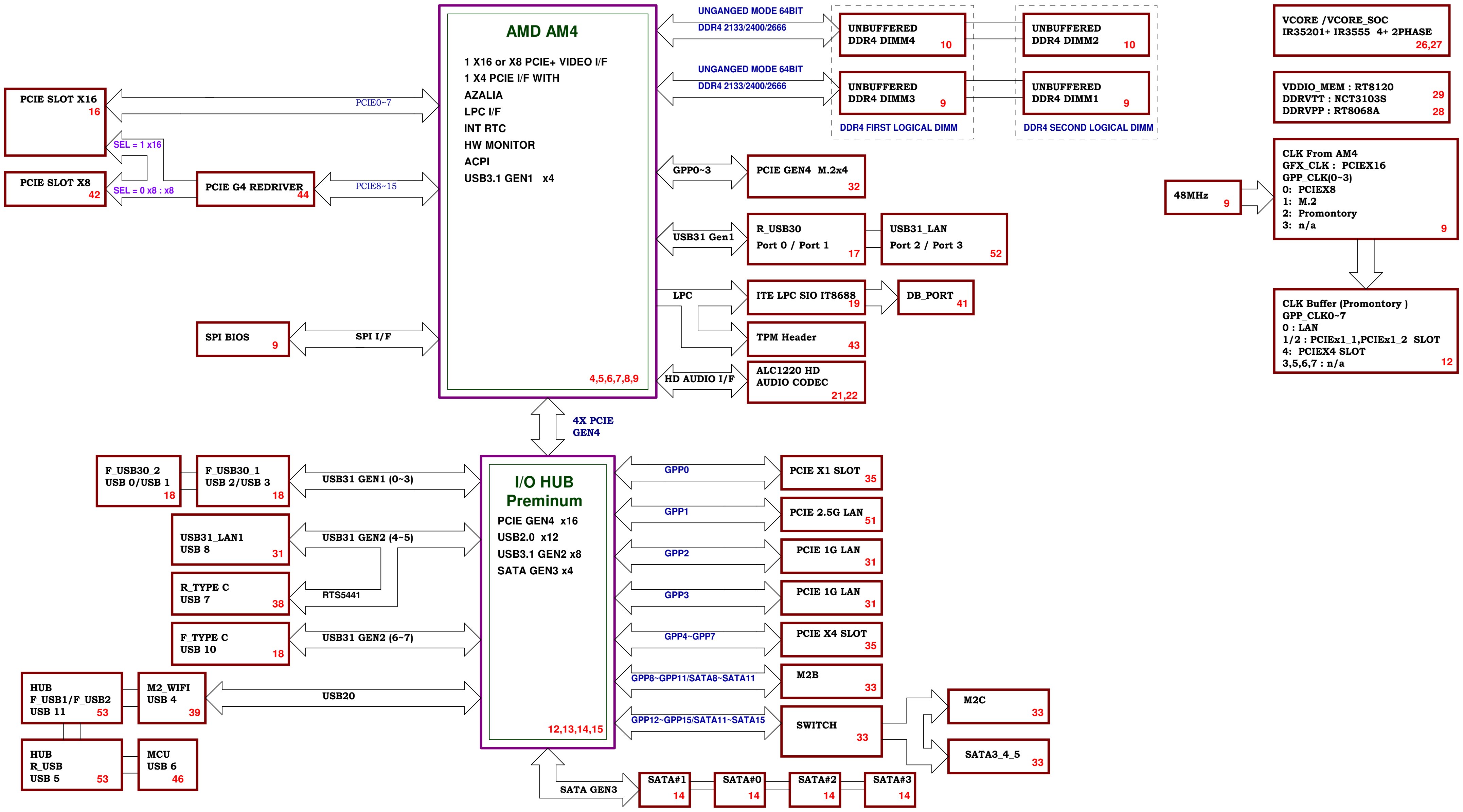

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Title
BLOCK DIAGRAM

Size	Document Number	Rev
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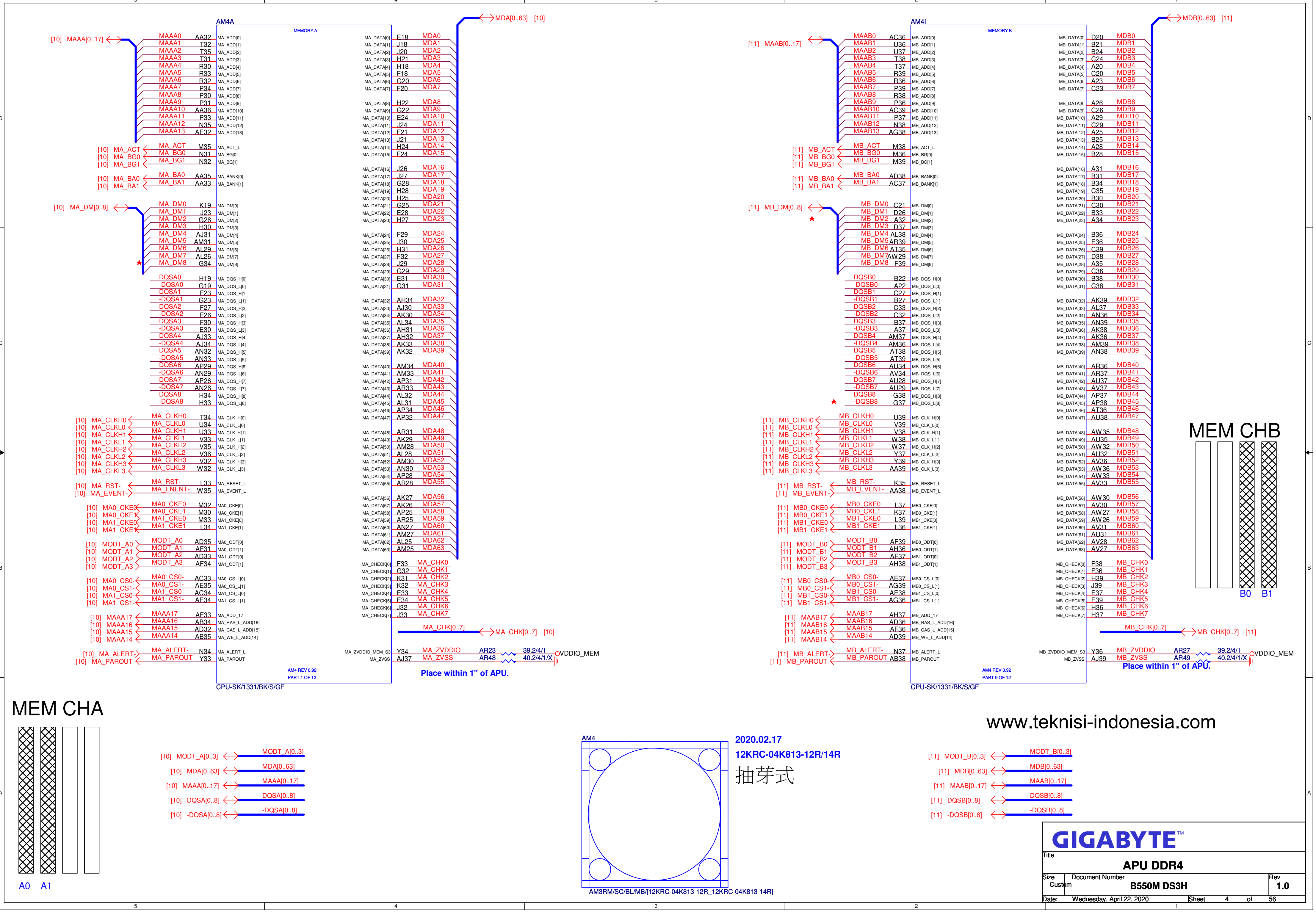

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Title	APU DDR4	
Size Custom	Document Number B550M DS3H	Rev 1.0
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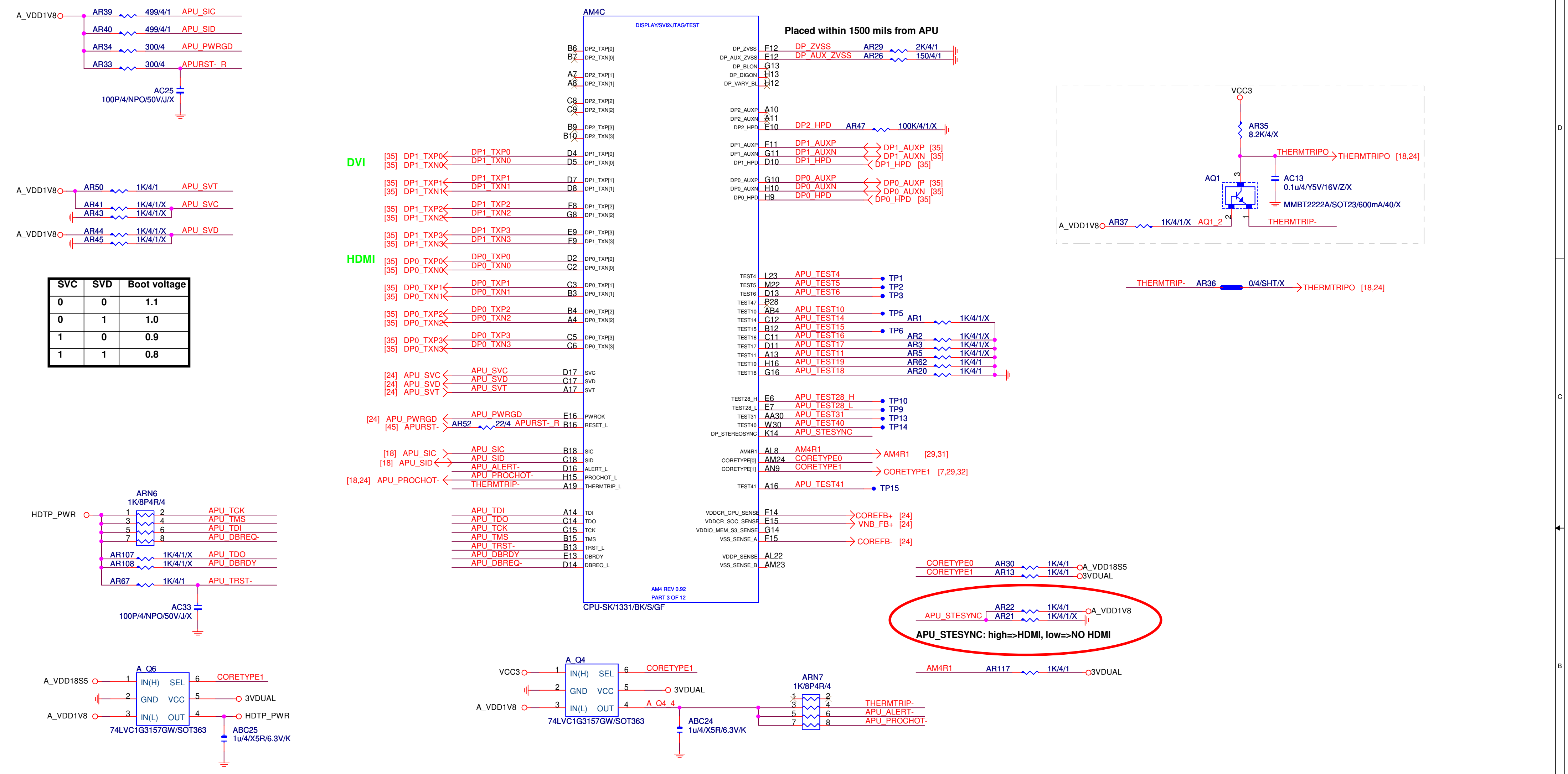

Placed within 1500 mils from APU

APU_STESYNC: high=>HDMI, low=>NO HDMI

SVC	SVD	Boot voltage
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

AM4 CPU CoreType

CORETYPE 1	CORETYPE 0	Family / Model Numbers	AM4 APU TYPE
0 BR	0	Family 15 h / Models 60 h- 6 Fh	TYPE 0
0 ST	1	Reserved	TYPE 1
1 ZP	0	Family 17 h / Models 00 h- 0 Fh	TYPE 2
1 RV	1	Family 17 h / Models 10 h- 1 Fh	TYPE 3

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Title
CPU CONTROL

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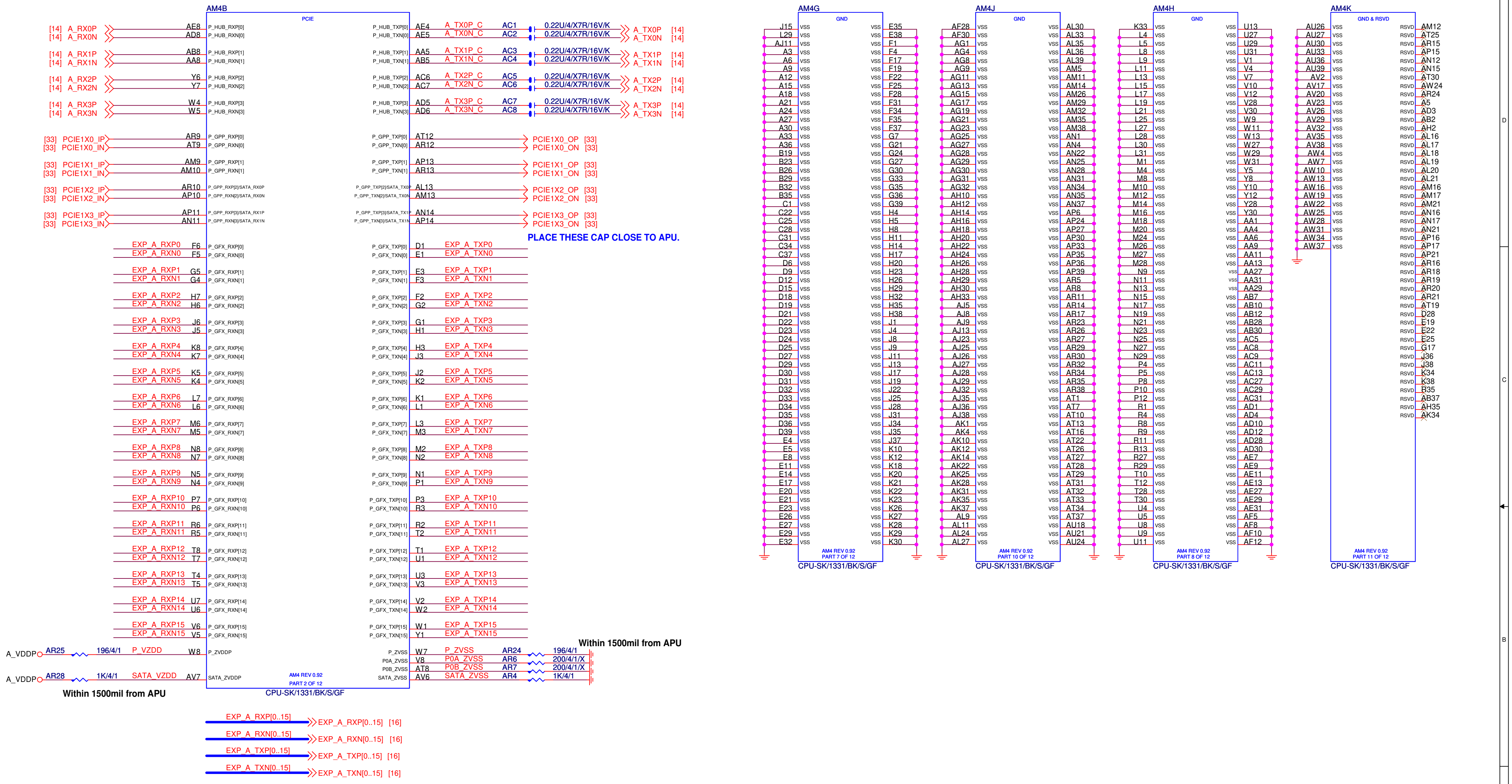

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Title
AM4_PCIE LINK, GND

Size	Document Number	Rev
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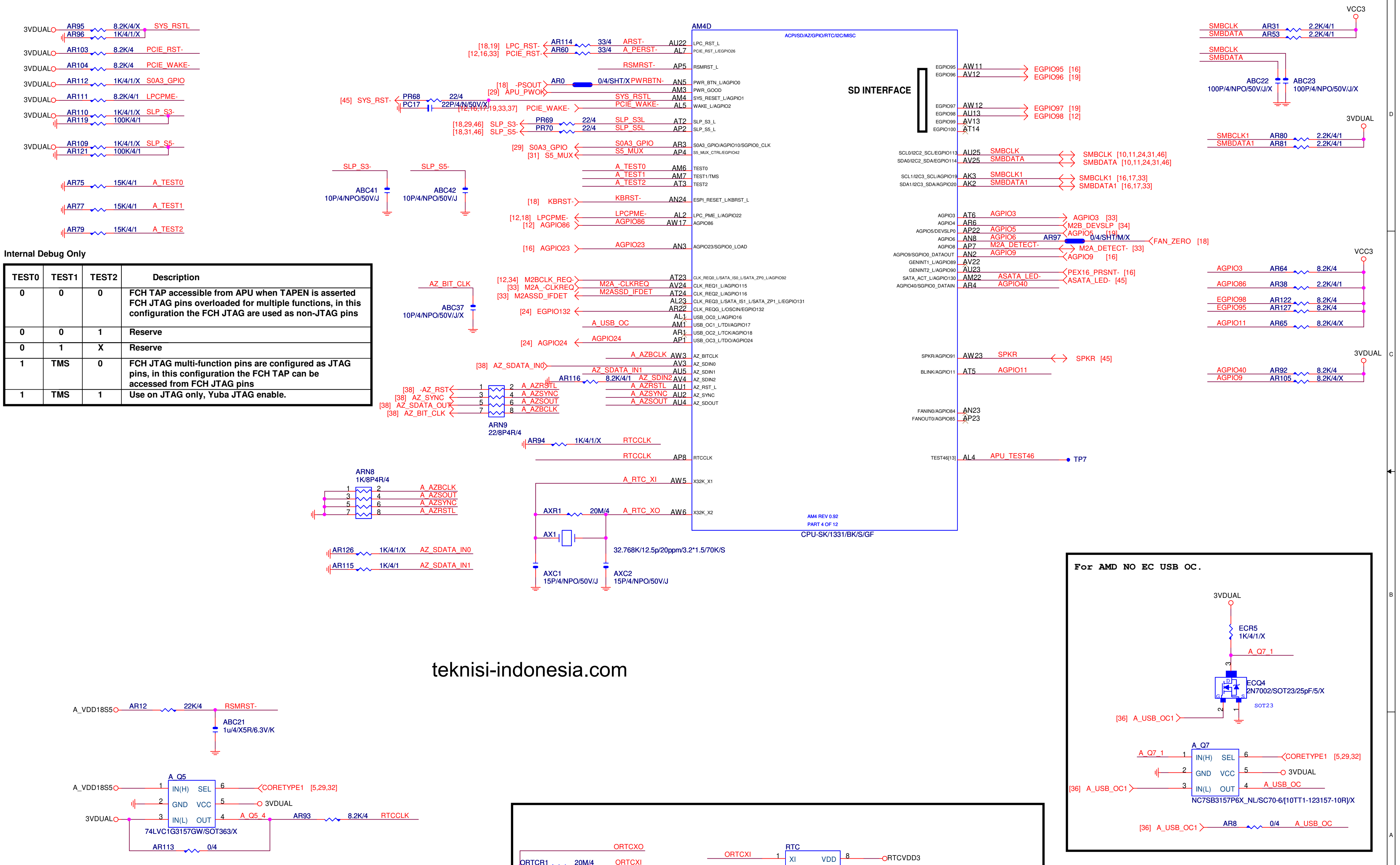

Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

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Title
AM4 MISC

Size Custom
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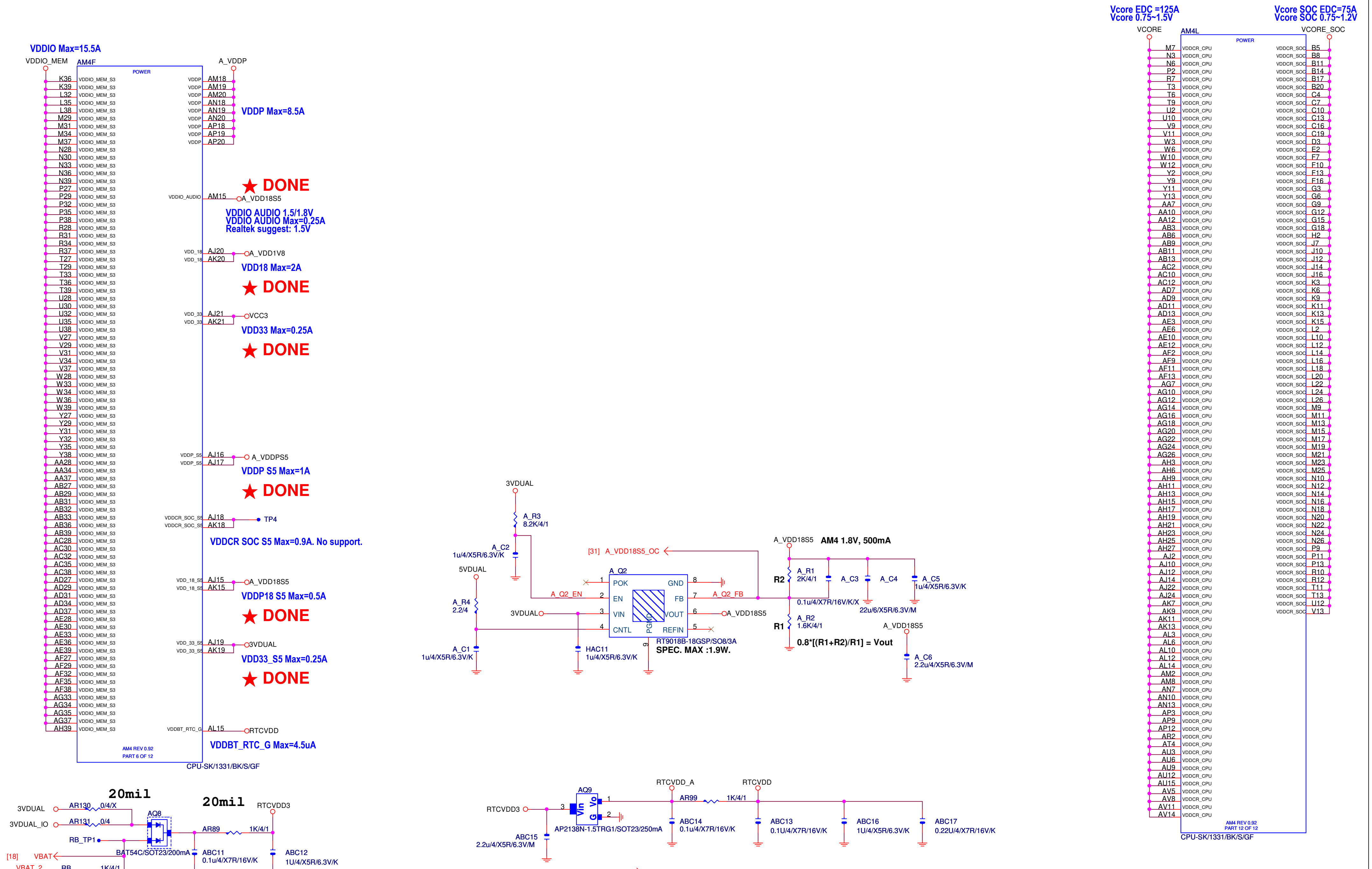

CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

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Title
CPU POWER & GND

Size Custom
Document Number B550M DS3H
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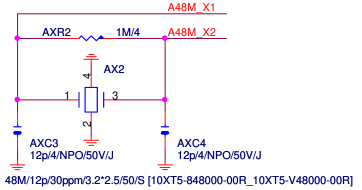
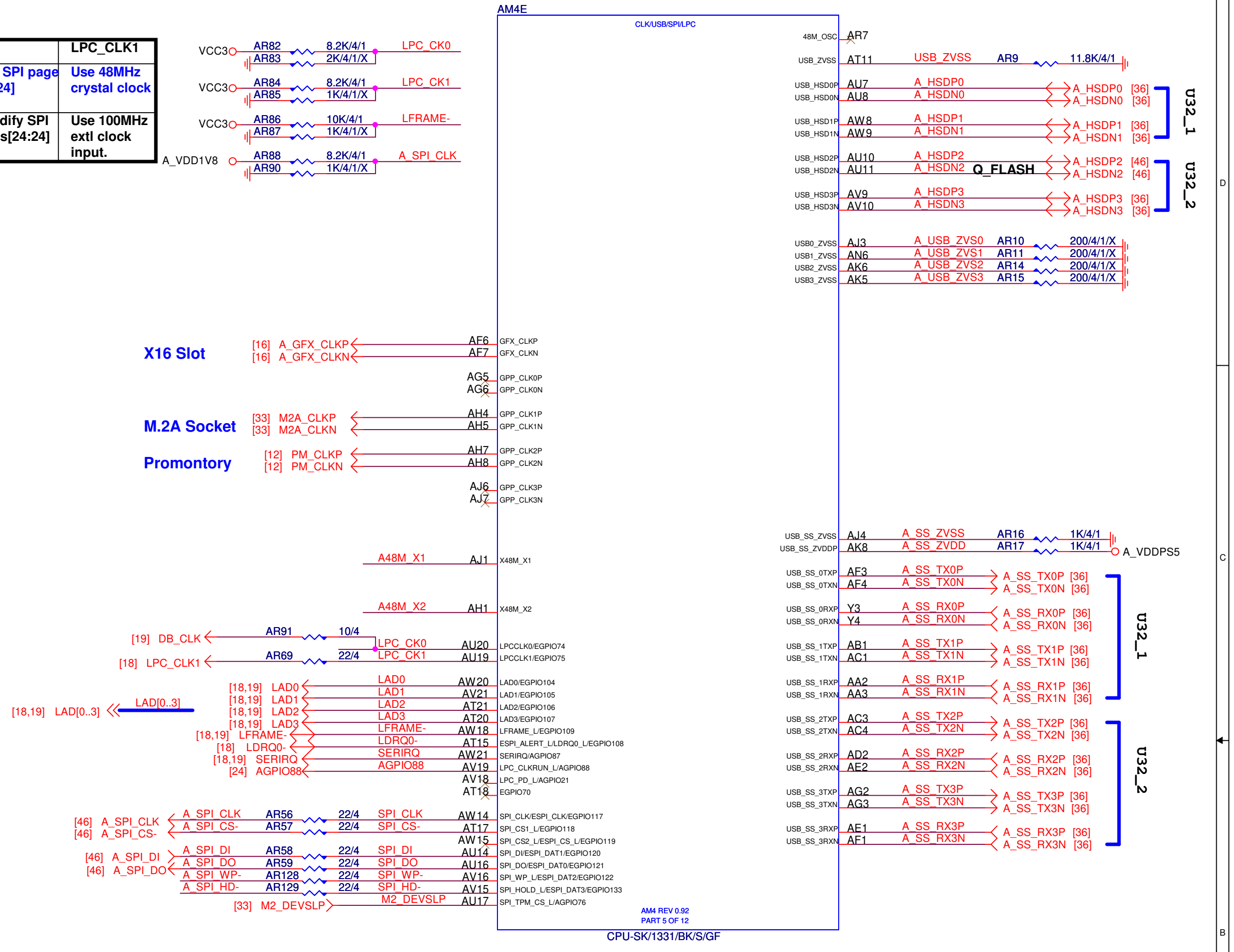


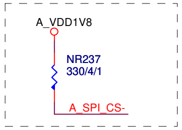
48M/12p/30ppm/3.2*2.5/50/S [10XT5-848000-00R_10XT5-V48000-00R]

AM4 STRAP

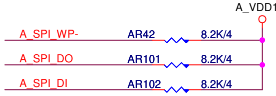
	SPI_CLK	LFRAME-	SYS_RST-	LPC_CLK0	LPC_CLK1
PULL HIGH	Internal clock mode	SPI ROM	Normal reset mode	PSP modify SPI page reg bits[24:24]	Use 48MHz crystal clock
PULL LOW	Extal clock mode	LPC ROM	Short reset mode	PSP not modify SPI page reg bits[24:24]	Use 100MHz extl clock input.

Bule: default

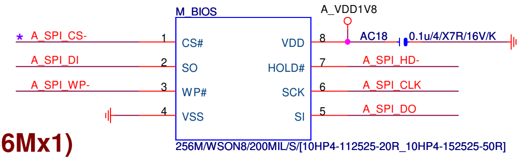




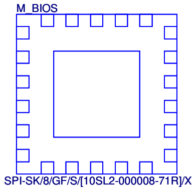
★1.8V SPI ROM USE



Fix flash BIOS fail Issue 1K to 330 ohm



★WSON8 BIOS Socket



Single (256Mx1)
Layout colay 128Mx1

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Title
APU USB, GPP

Size
Custom

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1.0

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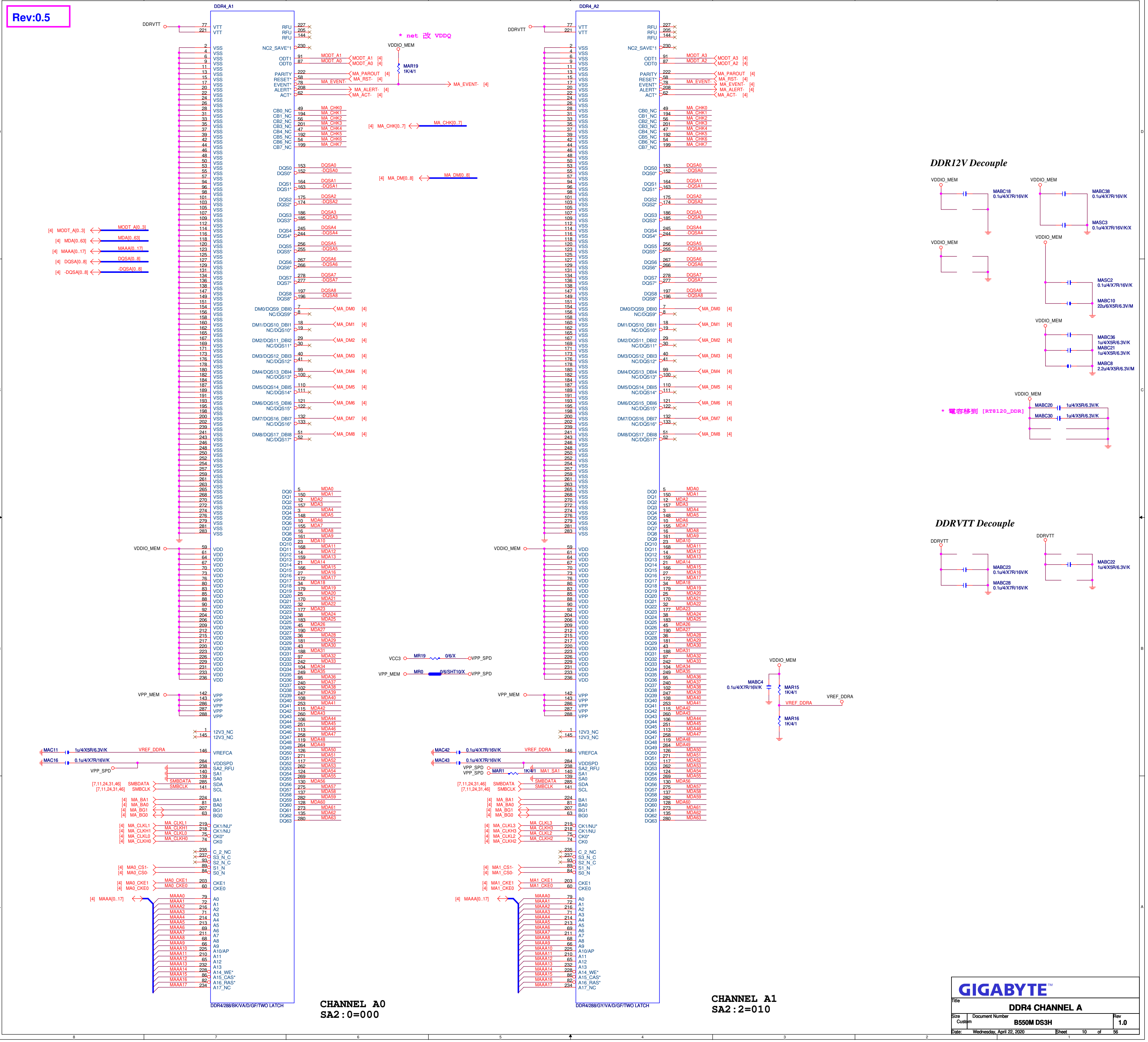

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Title
DDR4 CHANNEL A

Size: Custom
Document Number: **B550M DS3H**
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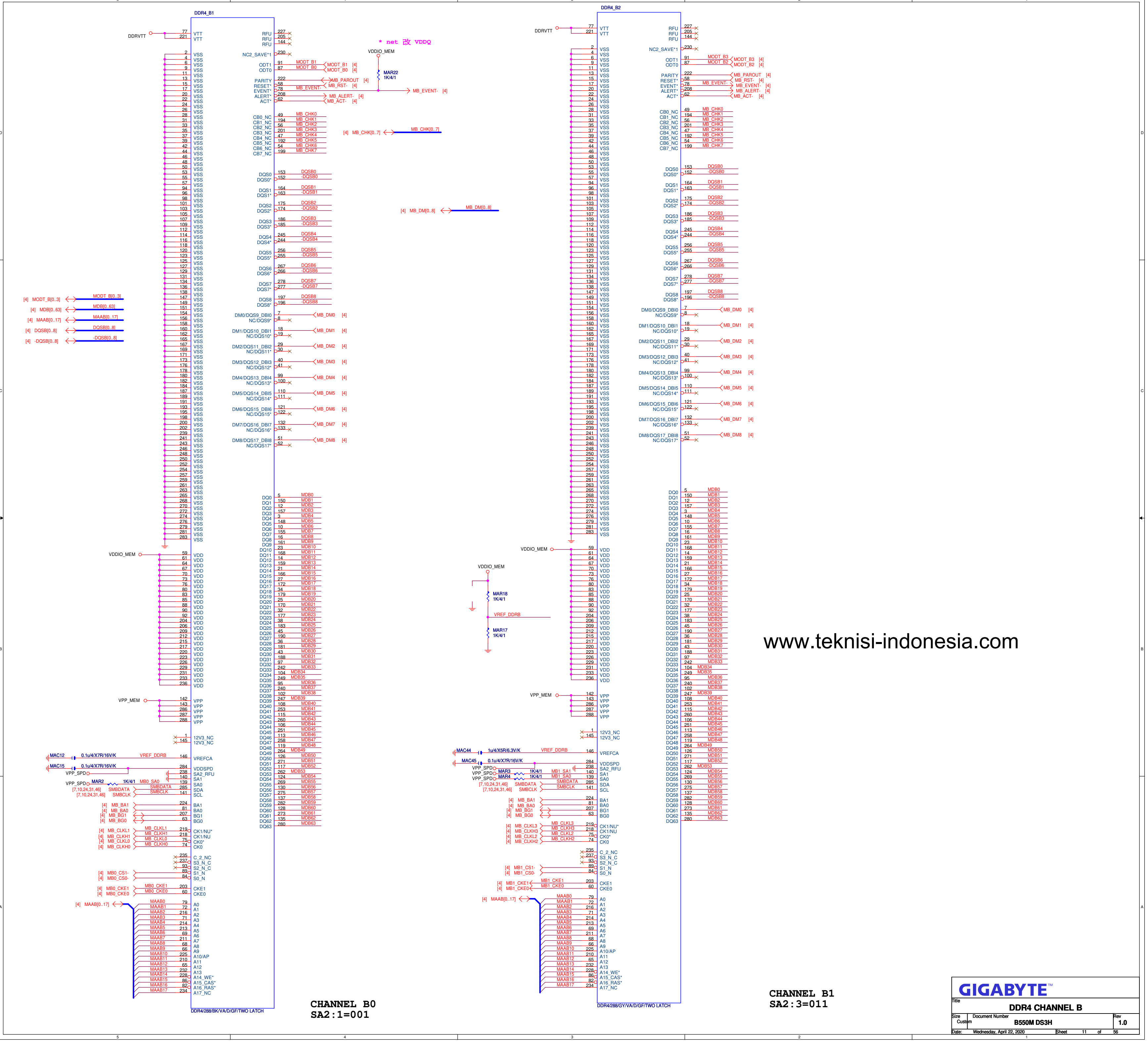

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Title
DDR4 CHANNEL B

Size	Document Number	Rev
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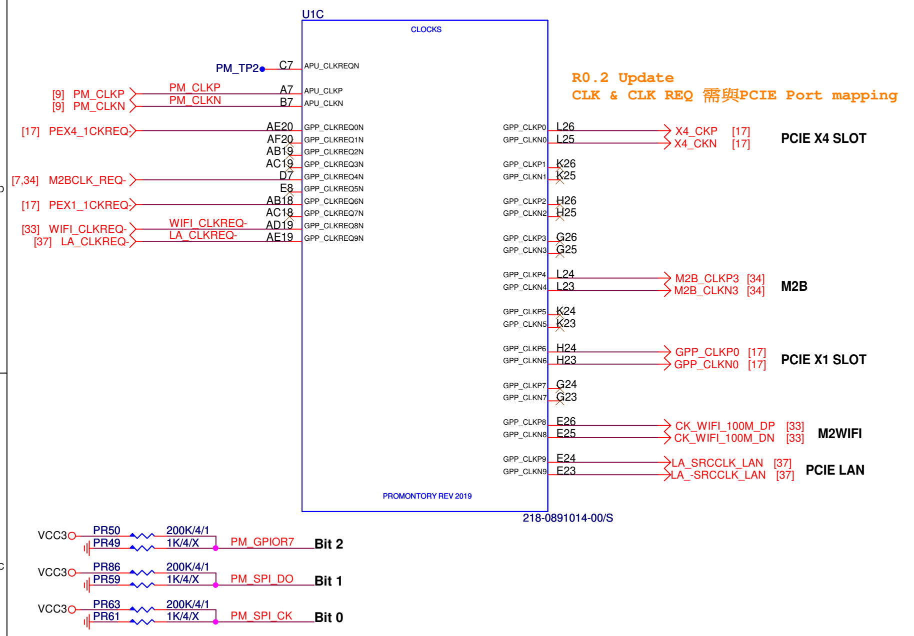
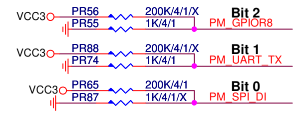


R0.2 Update
CLK & CLK REQ 需與PCIE Port mapping

Bit 2	Bit 1	Bit 0	GPP Group 0 (Lanes 3:0)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
			Others: Reserved

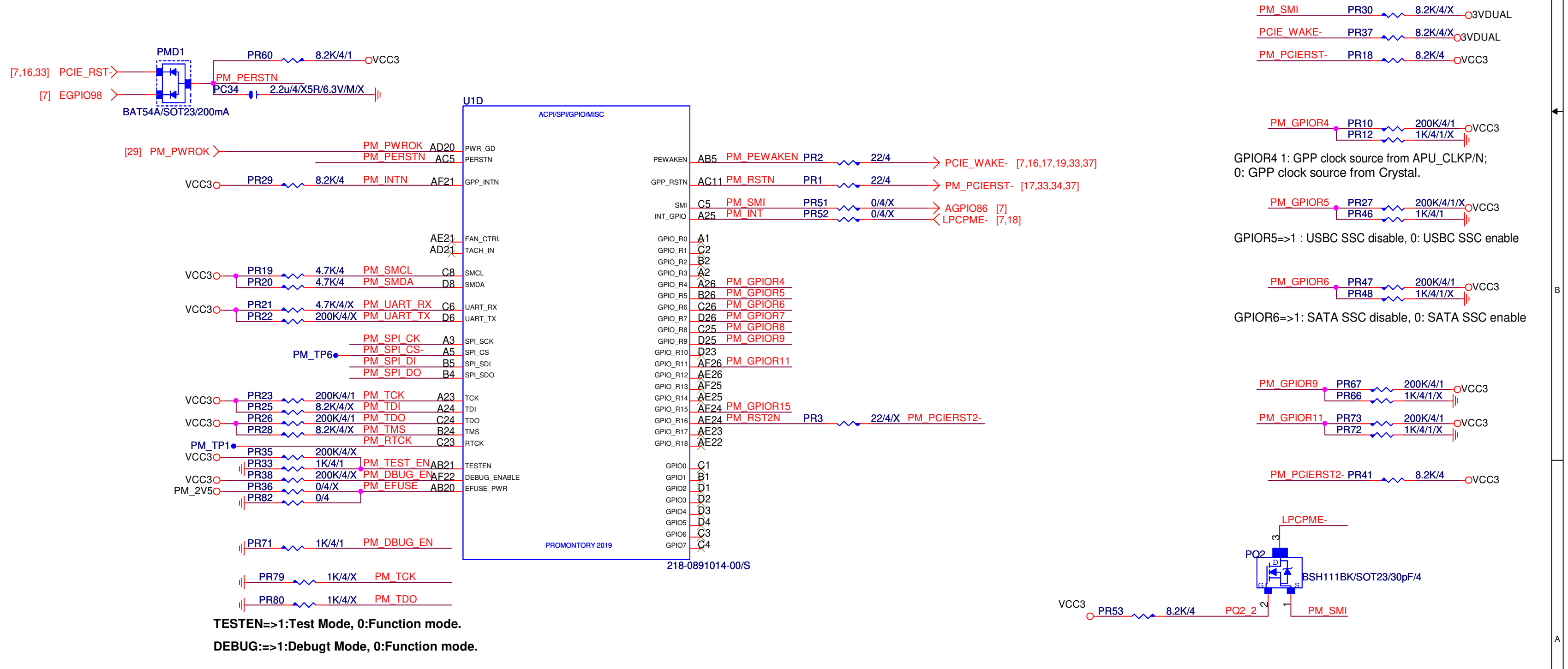
*



Bit 2	Bit 1	Bit 0	GPP Group 1(Lanes 7:4)
0	0	0	4 PCIe x1
0	0	1	2 PCIe x1 + 1 PCIe x2
0	1	0	1 PCIe x2 + 2 PCIe x1
0	1	1	1 PCIe x2 + 1 PCIe x2
1	1	1	1 PCIe x4
			Others: Reserved

*

GPP Group 2 (Lan 8:9)=>1: PCIe x2, 0: 2 PCIe x1



GPIOR4 1: GPP clock source from APU_CLKP/N;
0: GPP clock source from Crystal.

GPIOR5=>1 : USBC SSC disable, 0: USBC SSC enable

GPIOR6=>1: SATA SSC disable, 0: SATA SSC enable

TESTEN=>1:Test Mode, 0:Function mode.

DEBUG:=>1:Debugt Mode, 0:Function mode.

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Title	PREMIUM CPU/CLK/MISC		
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USB32G2	USB20	USB_OC
0	0	0
1	1	1
USB32G1		
0	2	2
1	3	3
	4	4
	5	5
	6	6
	7	7
	8	7
	9	7

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ANS 7955361

Title
PM USB

Size Custom
Document Number **B550M DS3H**
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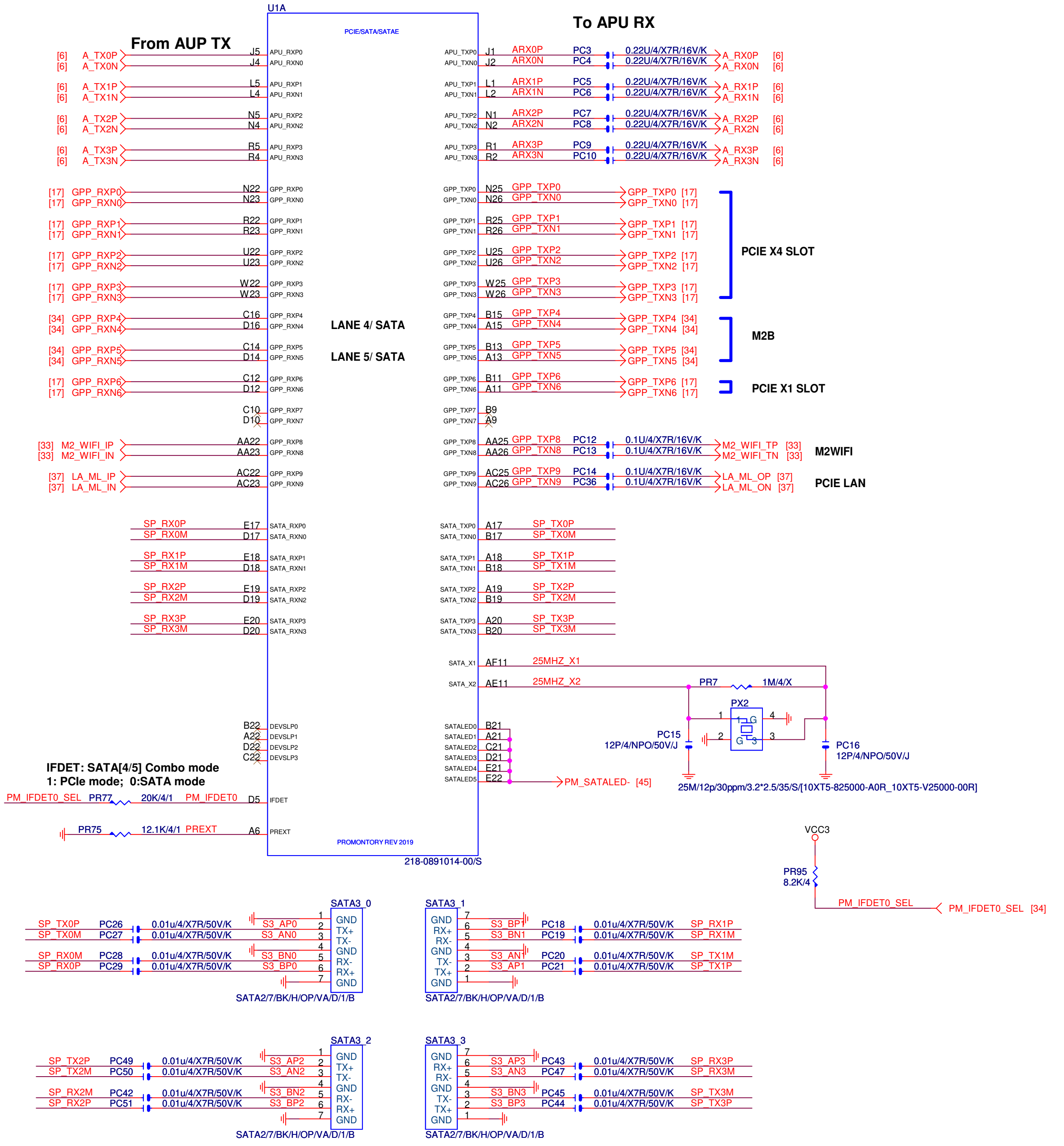

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ANS 7955361

Title		
PM SATA , PCIE		
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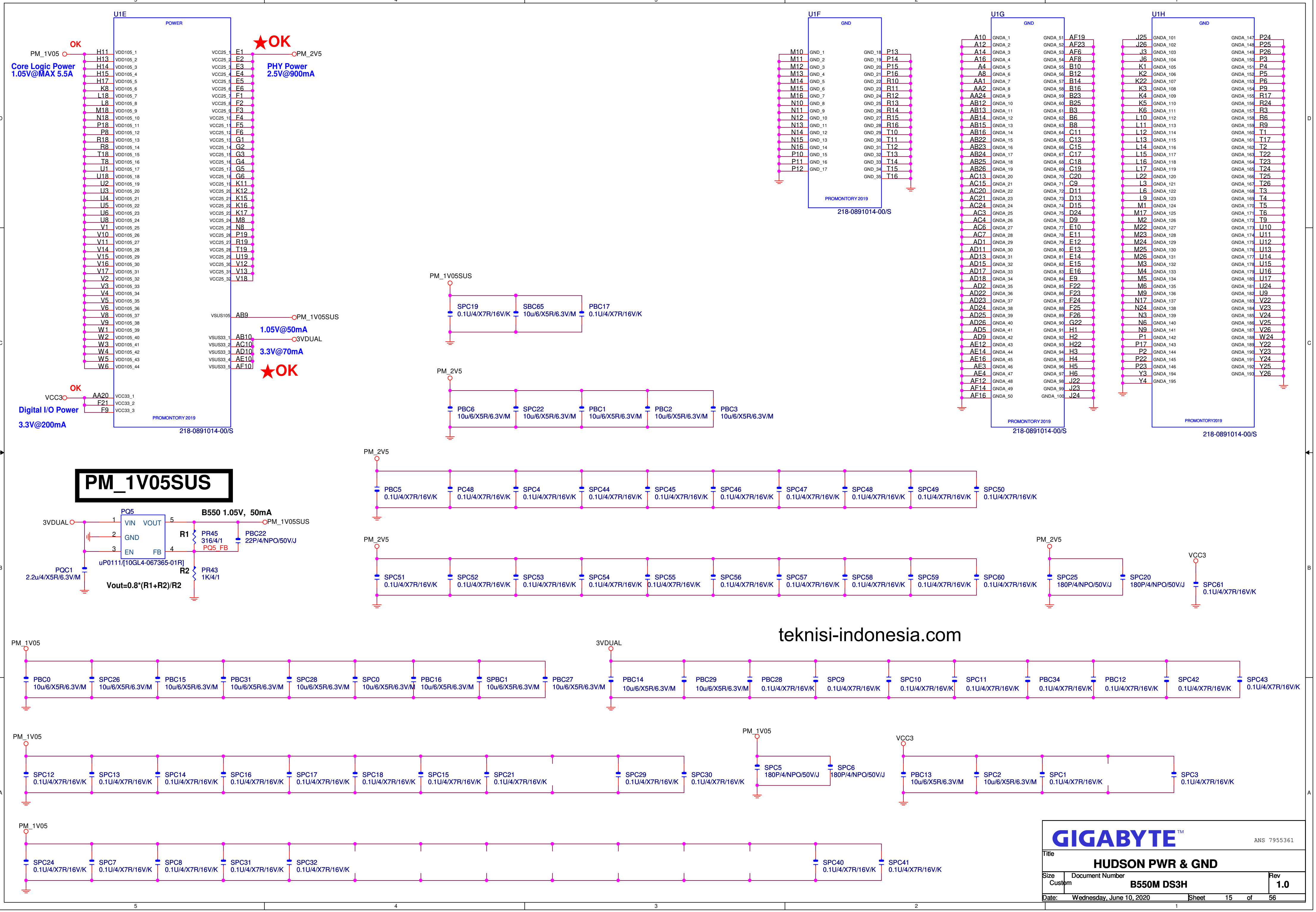

PM_1V05SUS

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ANS 7955361

Title
HUDSON PWR & GND

Size Custom
Document Number **B550M DS3H**
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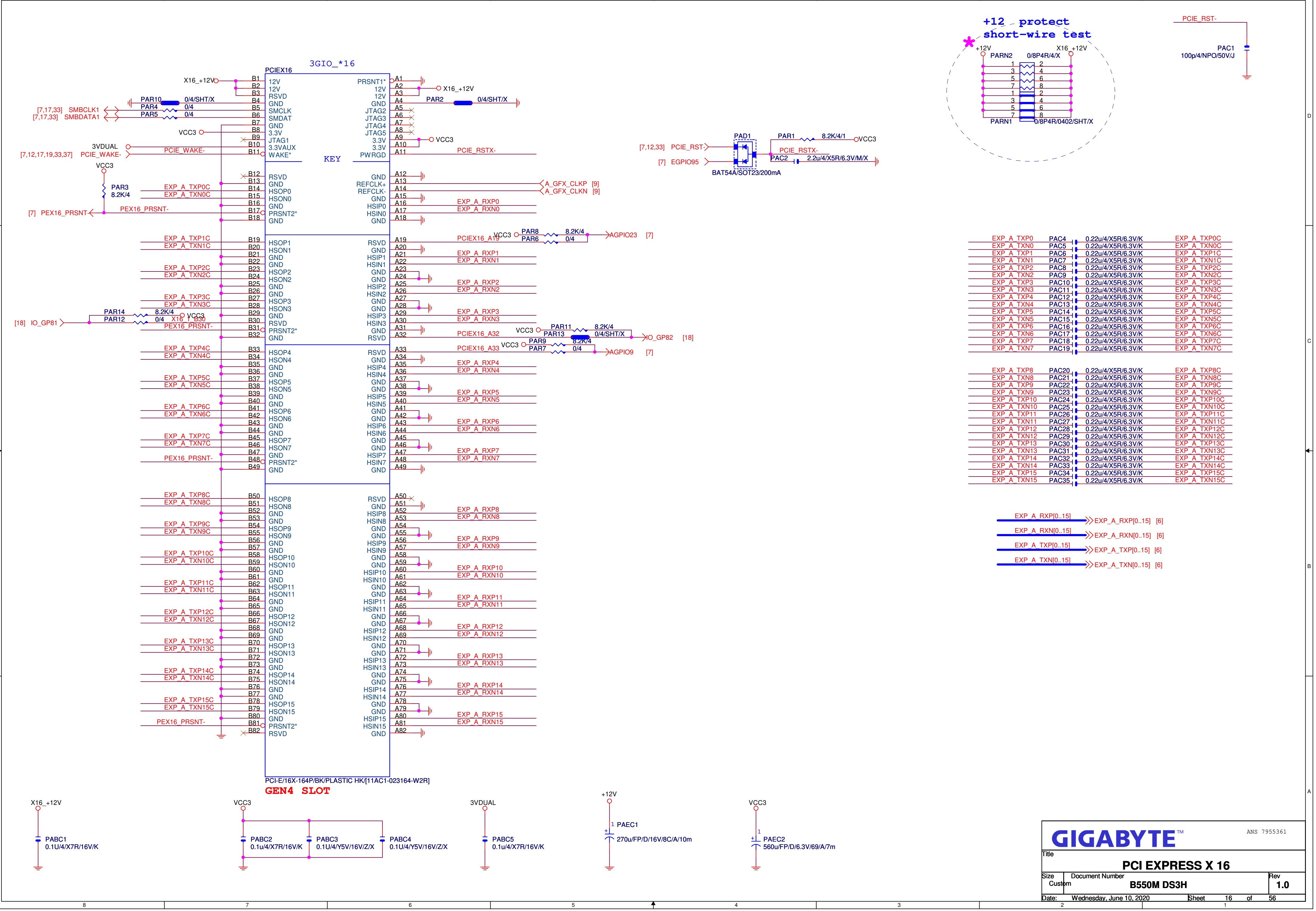

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ANS 7955361

Title
PCI EXPRESS X 16

Size	Document Number	Rev
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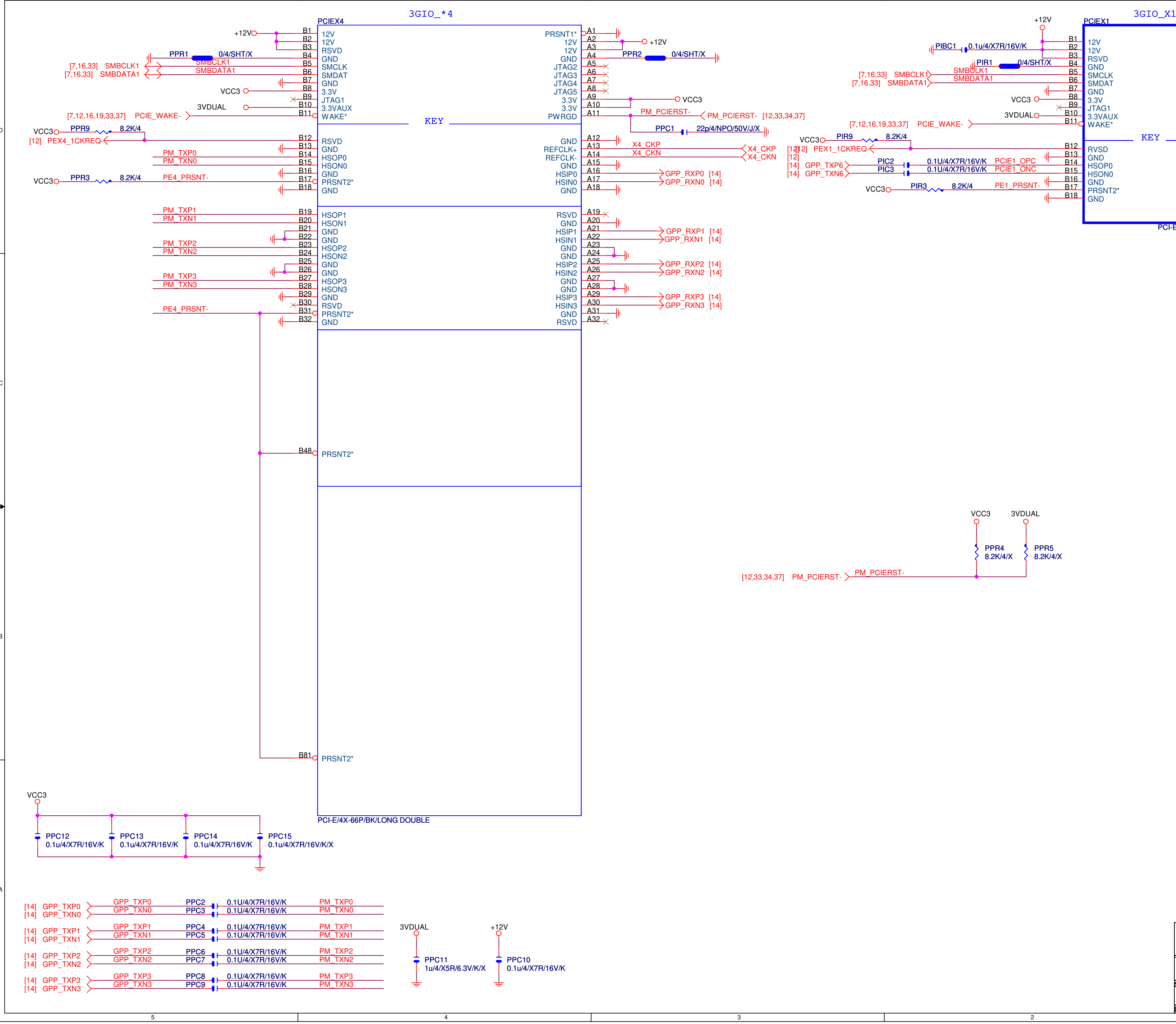

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ANS 7955361

Title
PCI_E X4

Size	Document Number	Rev
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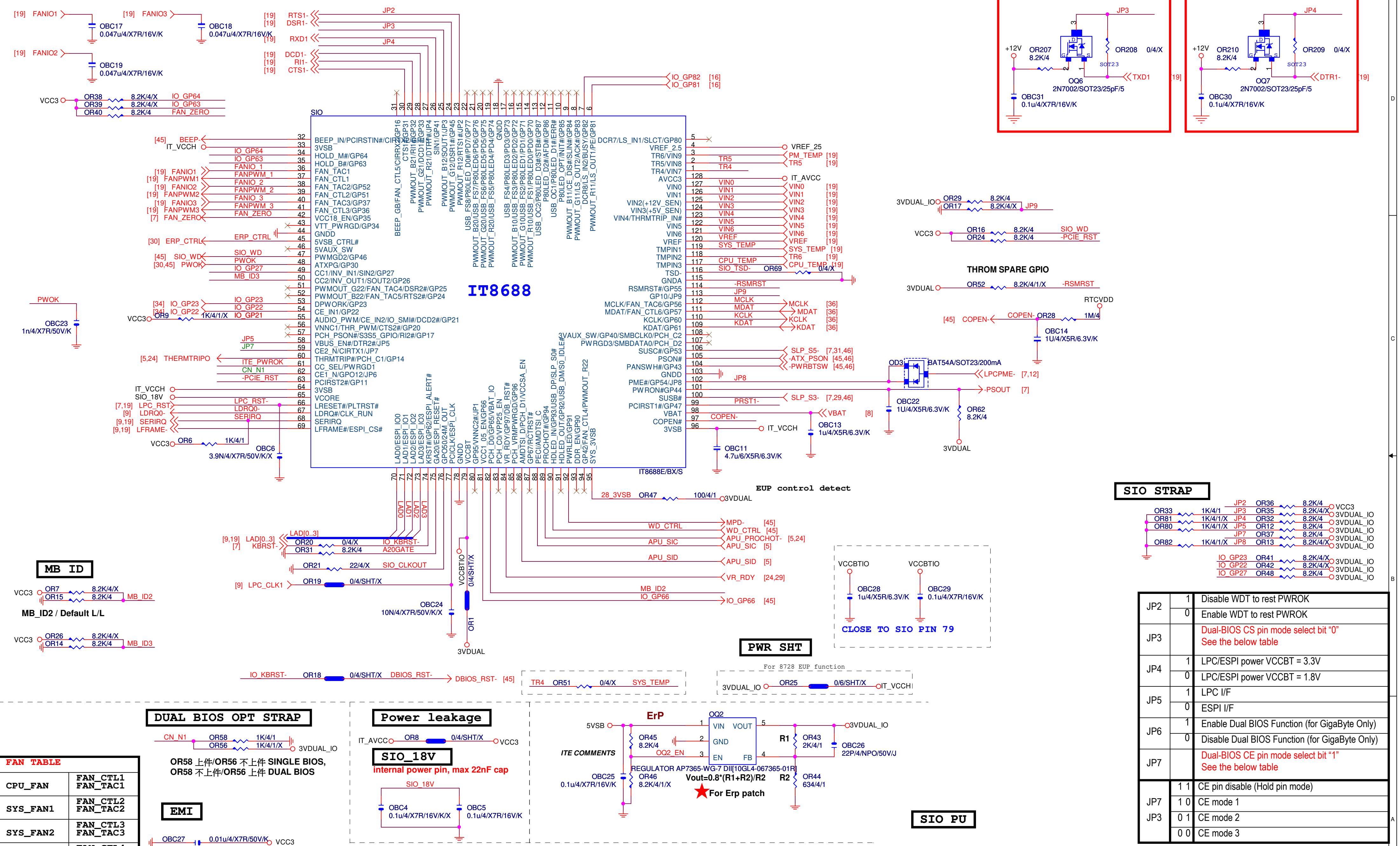
SIO IT8628CX REV:1.09



FAN TABLE

CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7 JP3	1 1	CE pin disable (Hold pin mode)
	1 0	CE mode 1
	0 1	CE mode 2
	0 0	CE mode 3

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Title: ITE 8686 LPC IO, TPM, KB/MS

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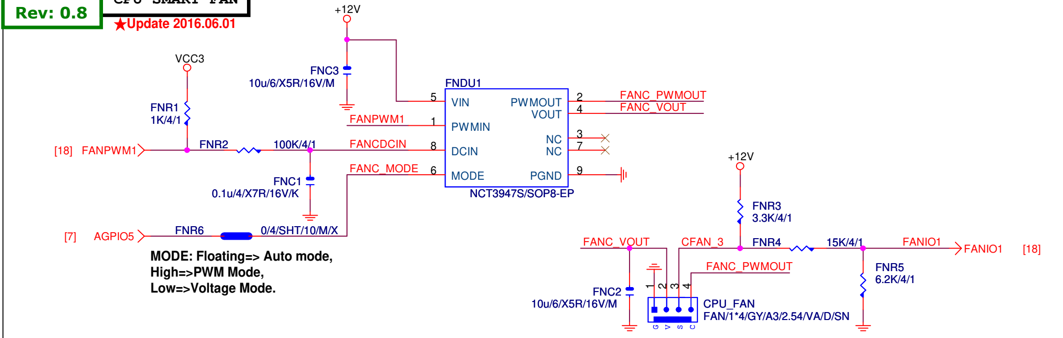
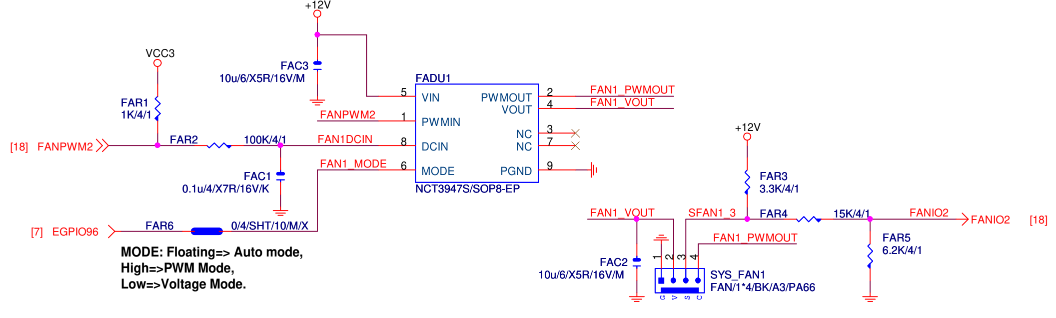
Rev: 0.8

CPU SMART FAN

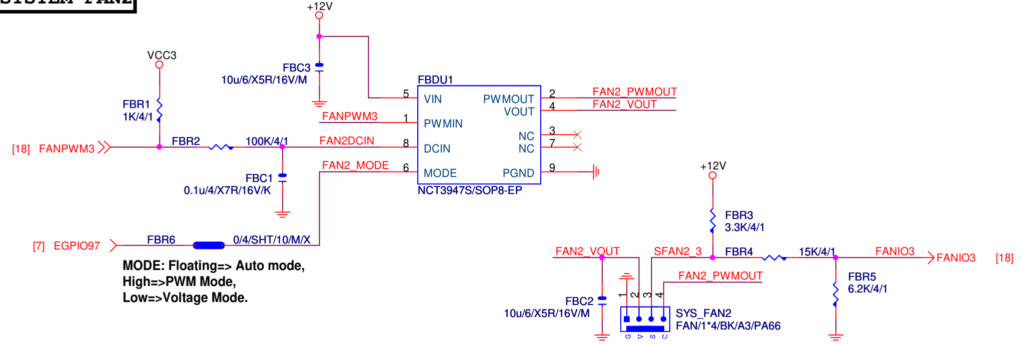
★Update 2016.06.01



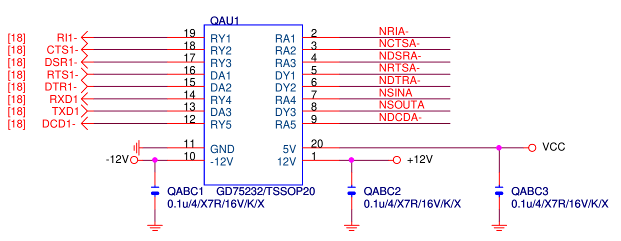
SYSTEM FAN1

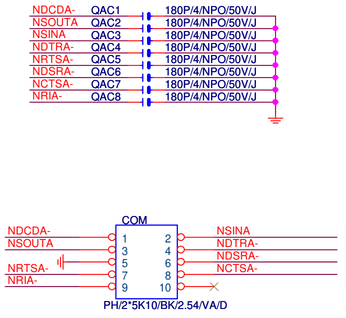


SYSTEM FAN2



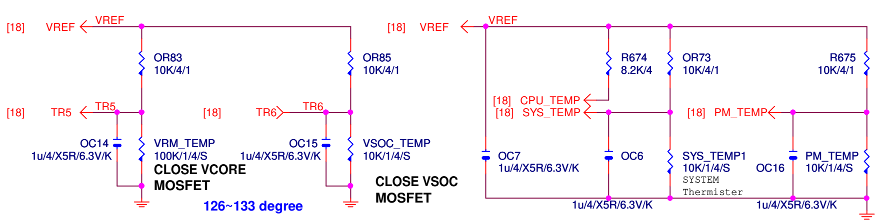
COM PORT





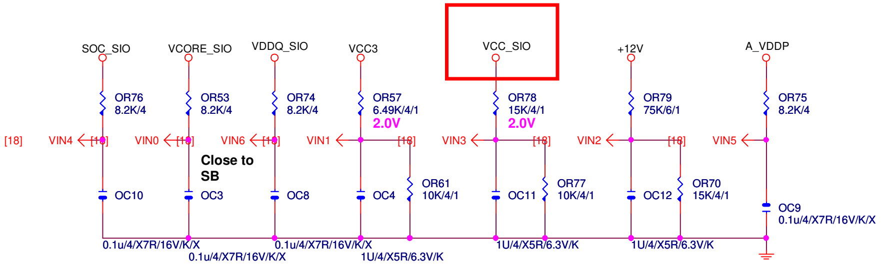
R&D技術通報151　有使用PRINT PORT的
MODEL，需使用新料號:10HP2-118728-72R 。(CHIP IT8728F/EX (GB) ITE/SMD
QFP128 PRINTPORT SORTING)料件。 串電阻33 ohm改為68 ohm。

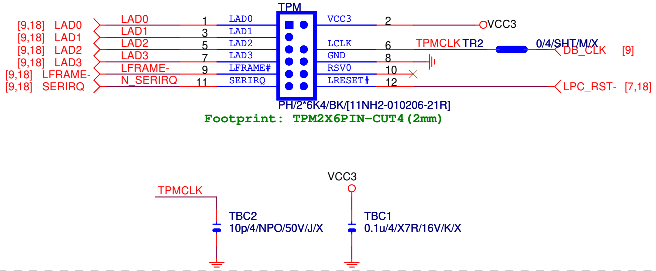
Hardware Monitor circuits - Tempature



Hardware Monitor circuits - VOLTAGE

Rev:0.6





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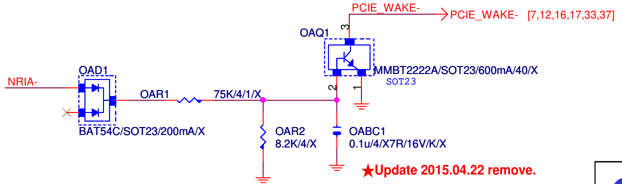

★Update 2015.04.22 remove.

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Title
CKG, HWM, TPM, THB

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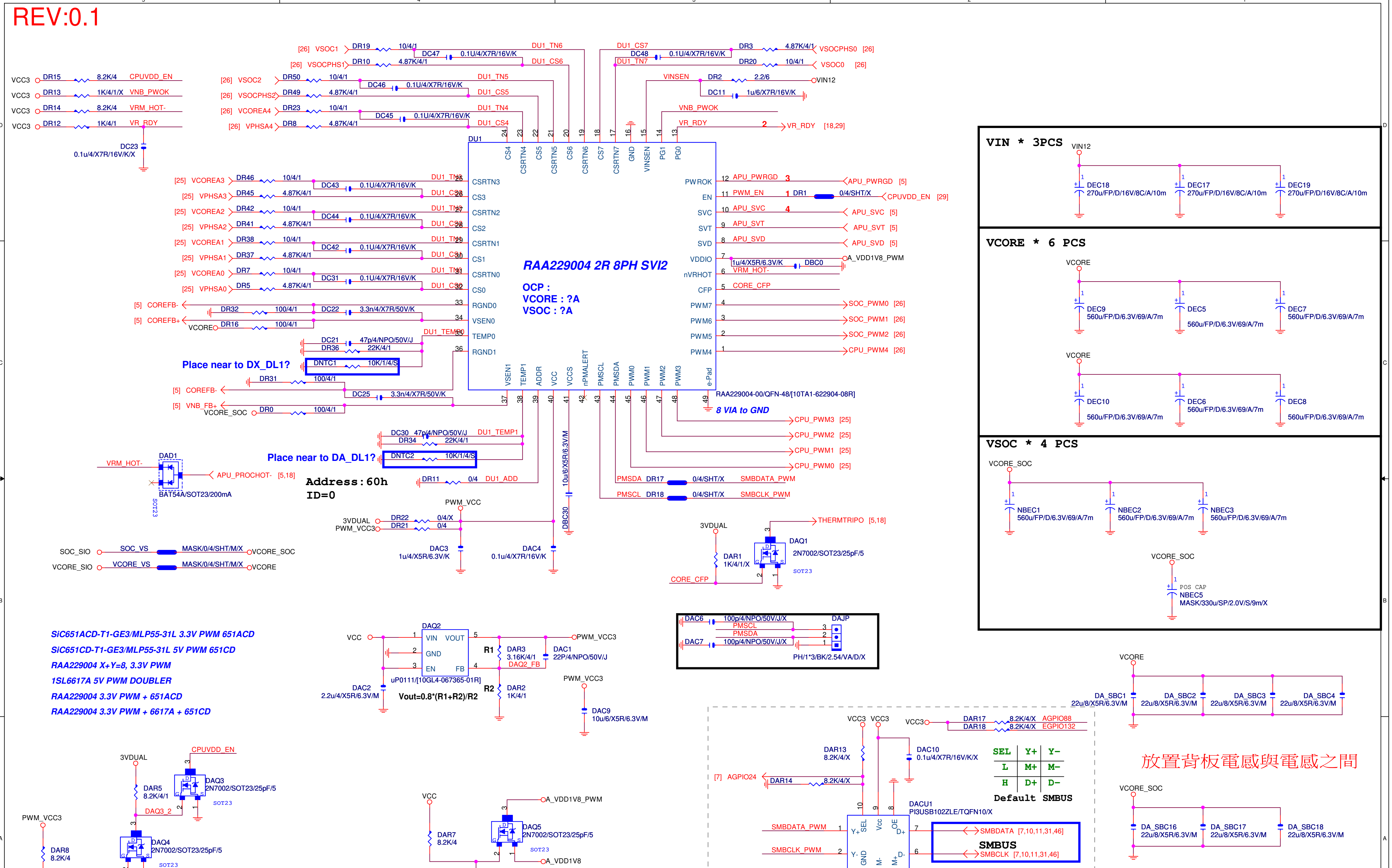
REV:0.1



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Title
PWM RAA229004

Size Custom
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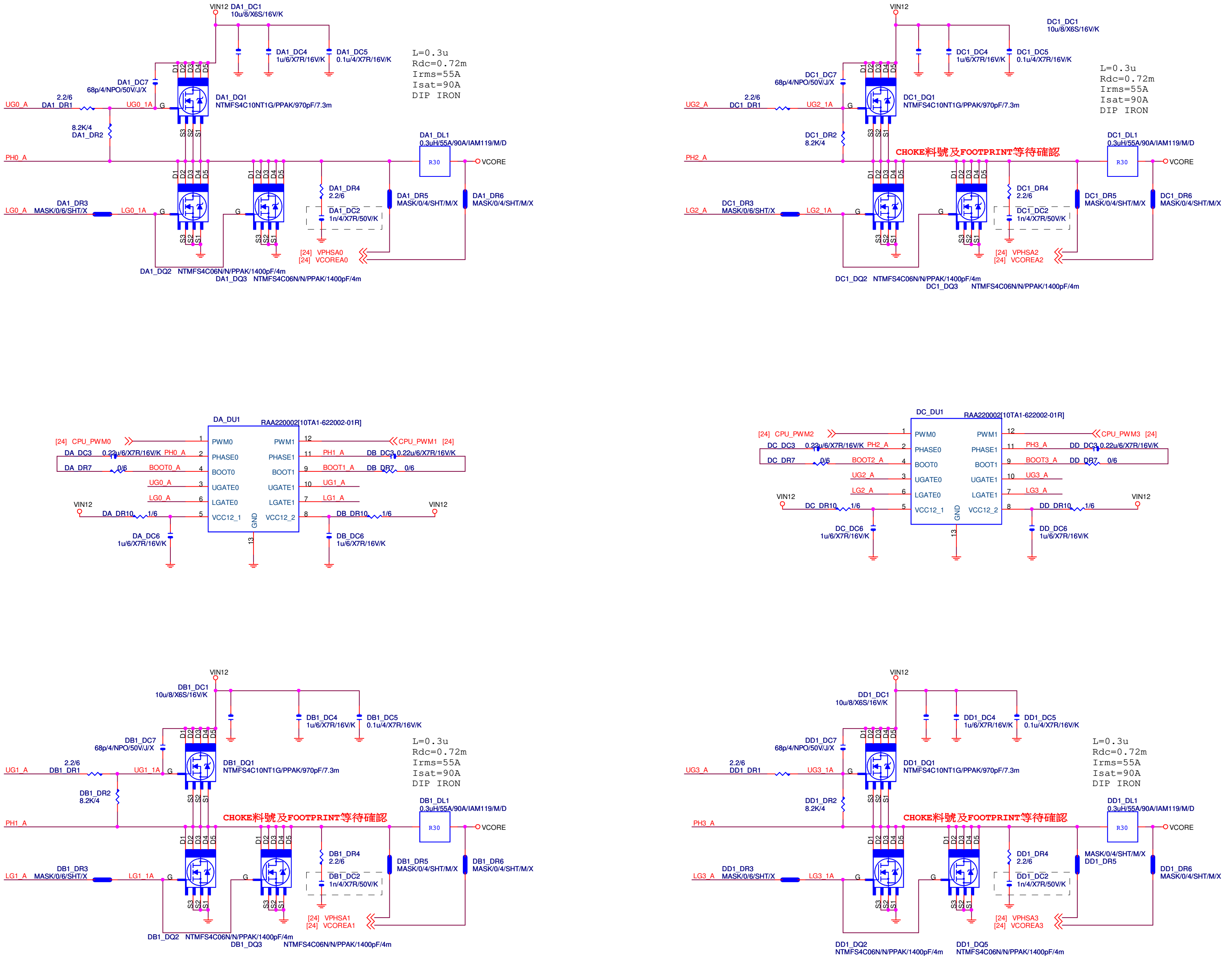
REV:0.1



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Title
PWM XDPE132G5C

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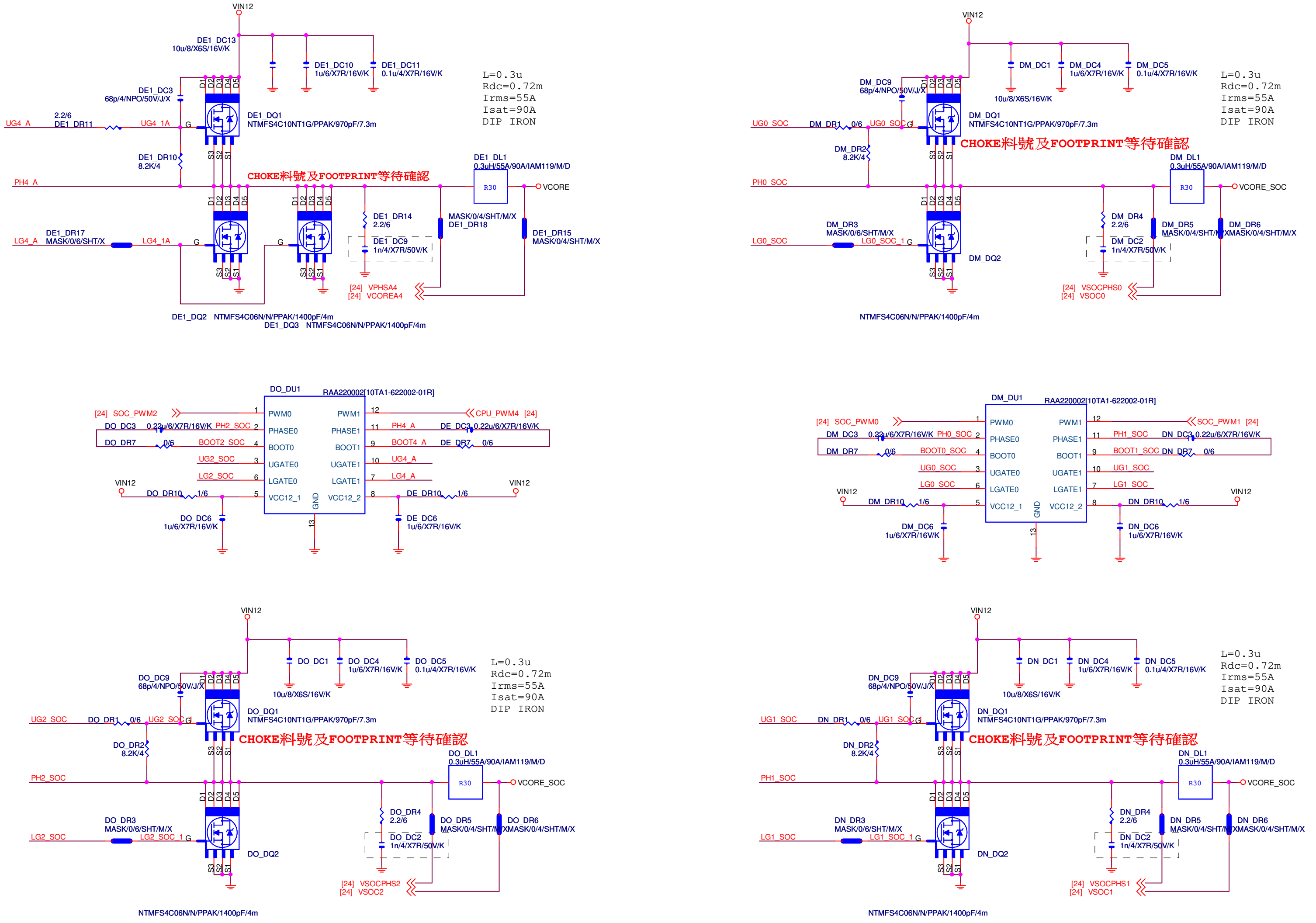
REV:0.1



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Title	IR3555_MOS-2	
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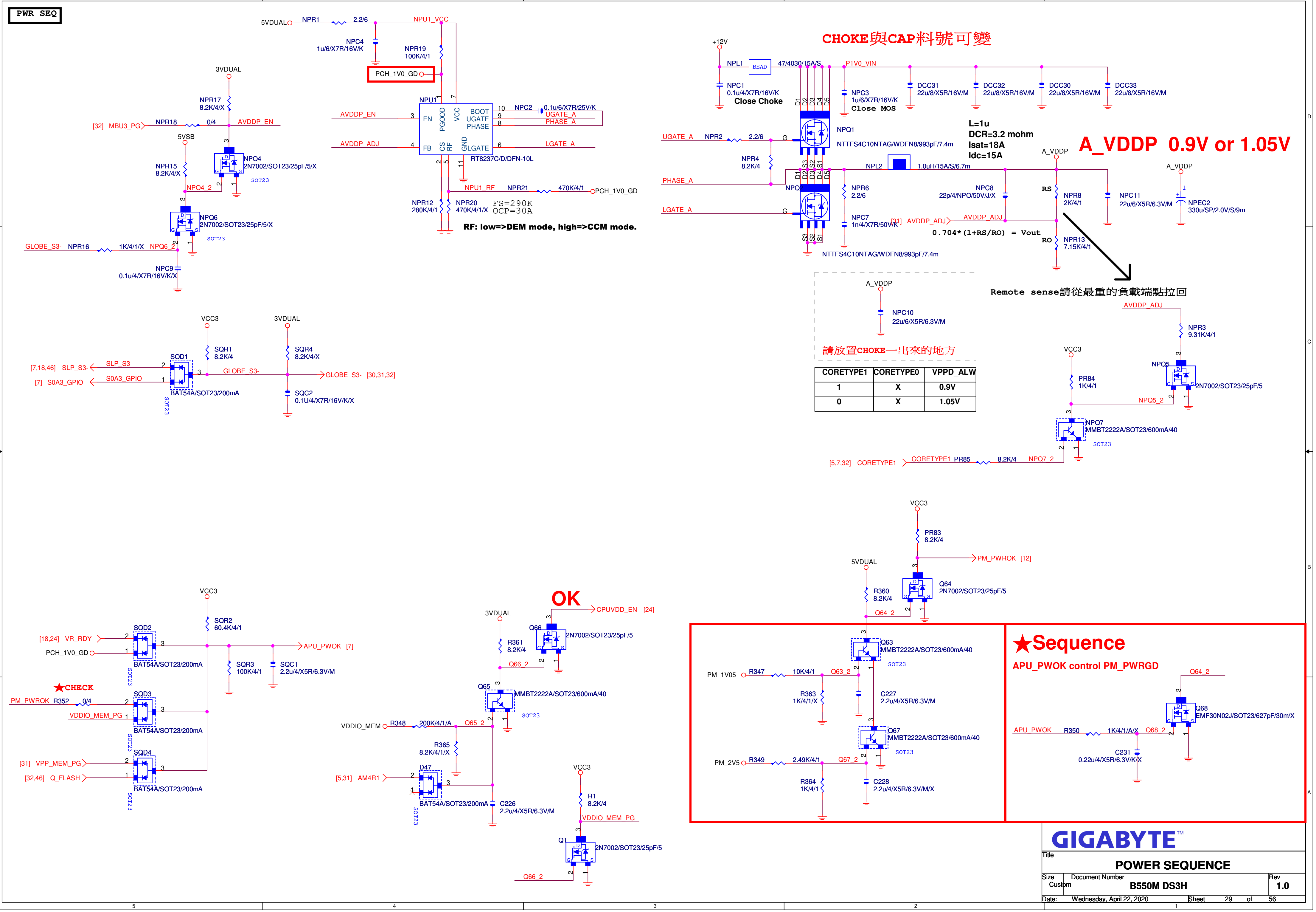

CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

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Title
POWER SEQUENCE

Size: Custom
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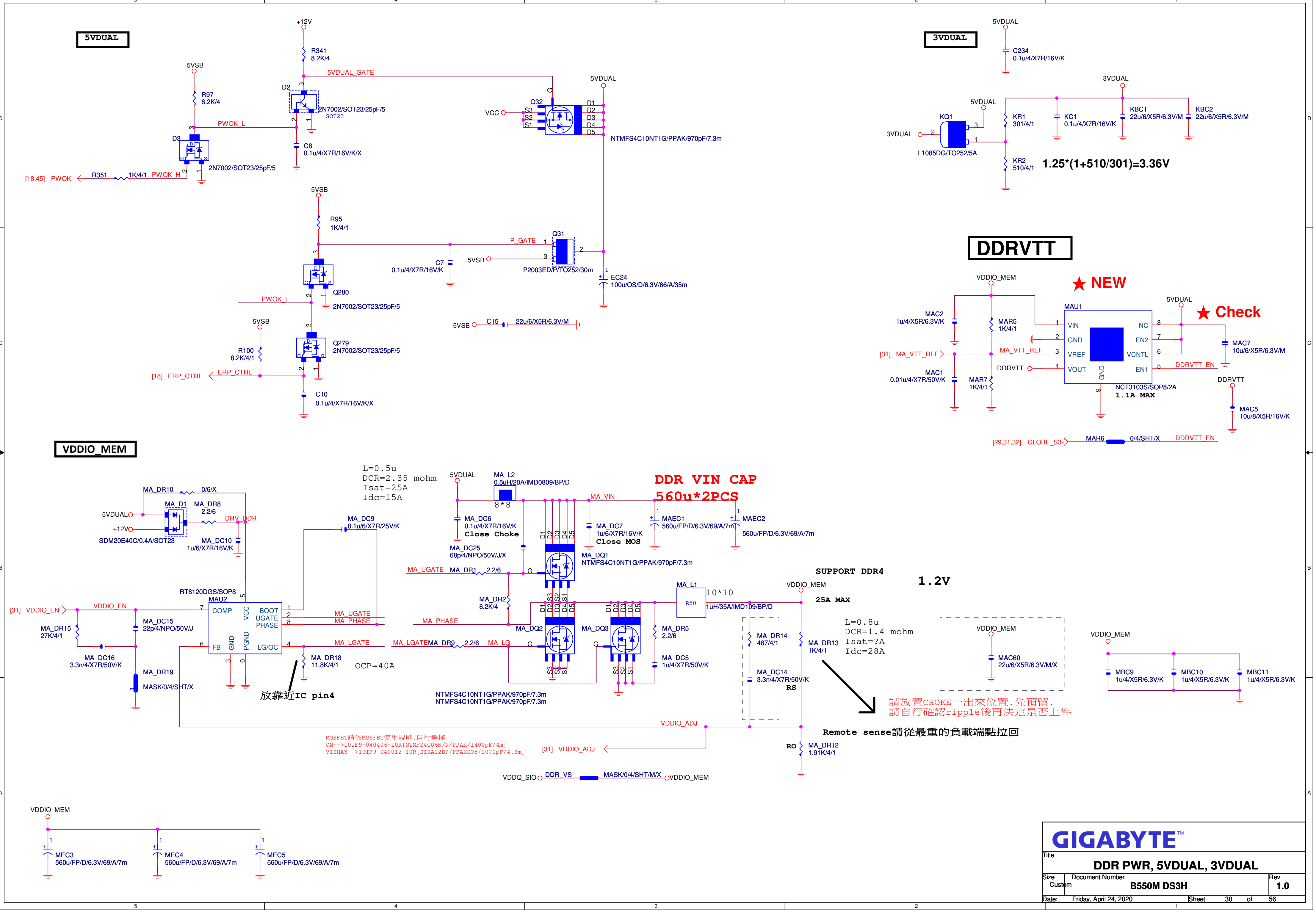

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Title
DDR PWR, 5VDUAL, 3VDUAL

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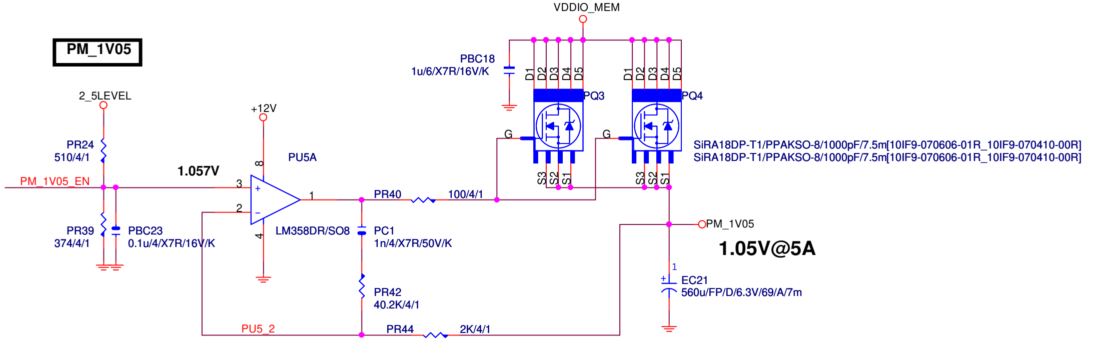
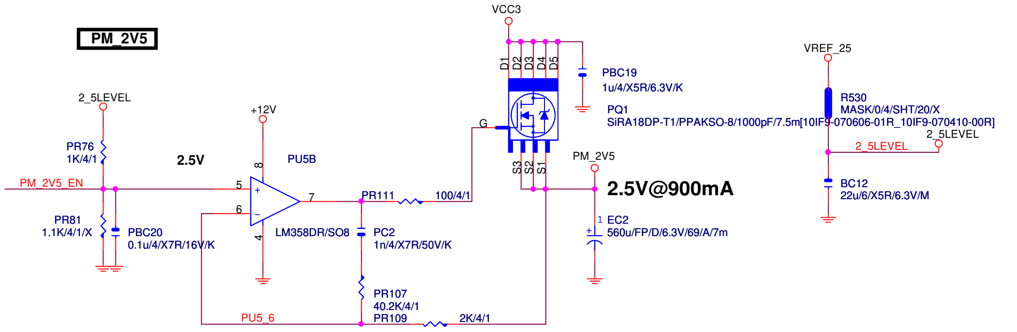
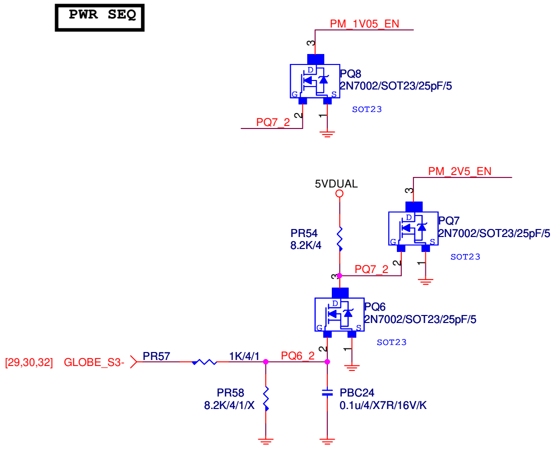
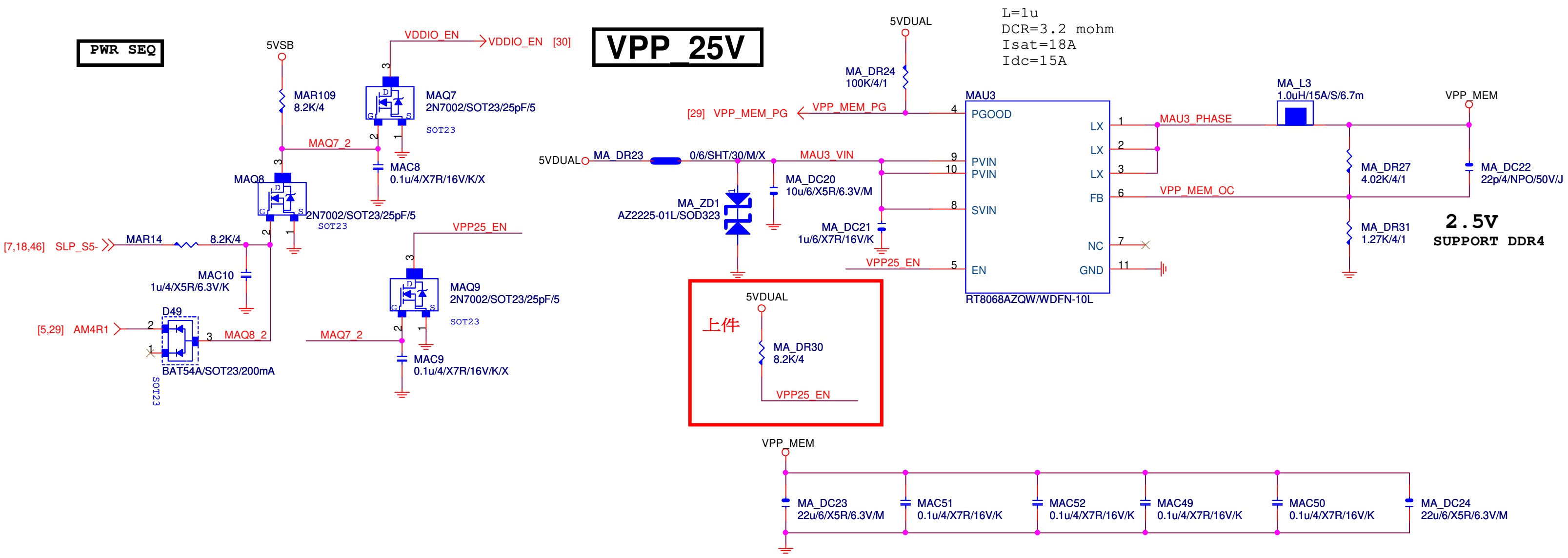
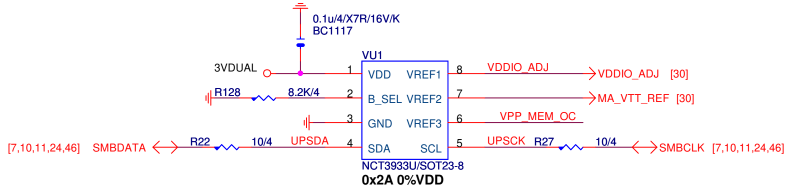
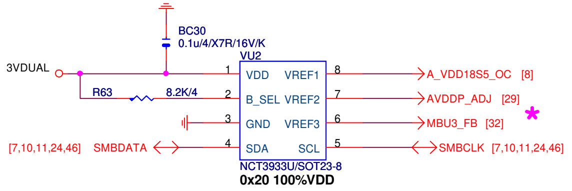






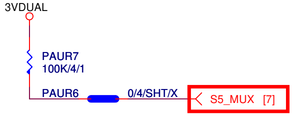






Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
ADD_SEL Voltage (% of VCC)	0	25	42	58	75	100

Table1. Recommended Slave Address Setting



GIGABYTE™

Title
VPP MEM

Size Custom
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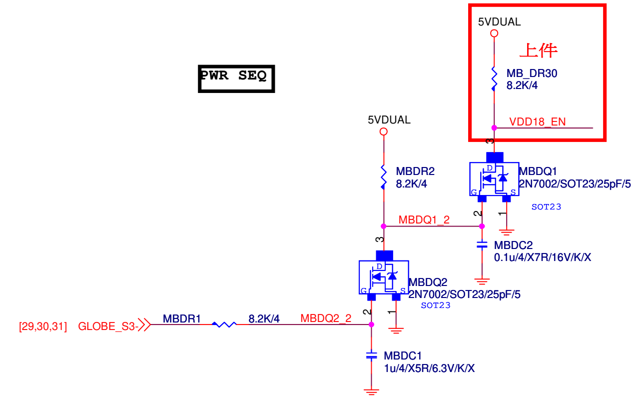
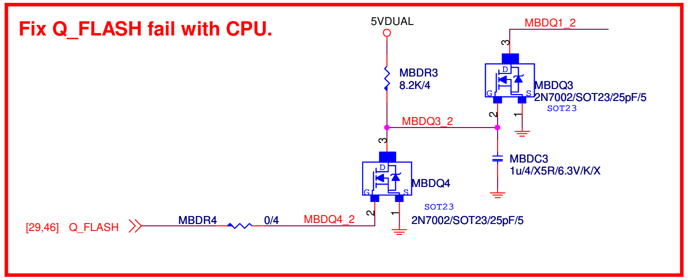
Rev 1.0

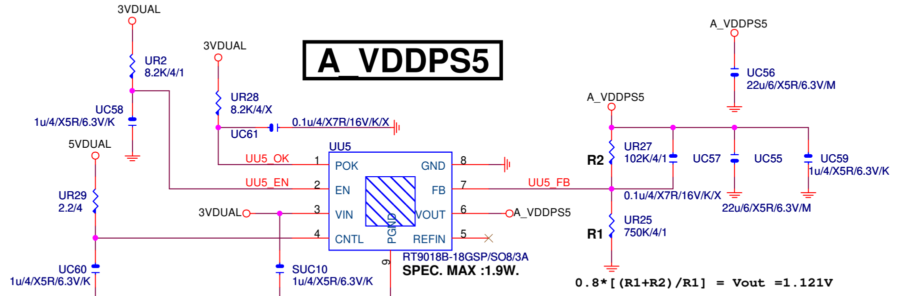
Date: Wednesday, April 22, 2020 Sheet 31 of 56



Fix Q_FLASH fail with CPU.

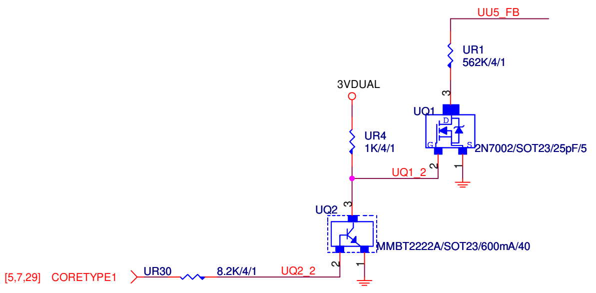


A_VDDPS5



0.8*[(R1+R2)/R1] = Vout =1.121V

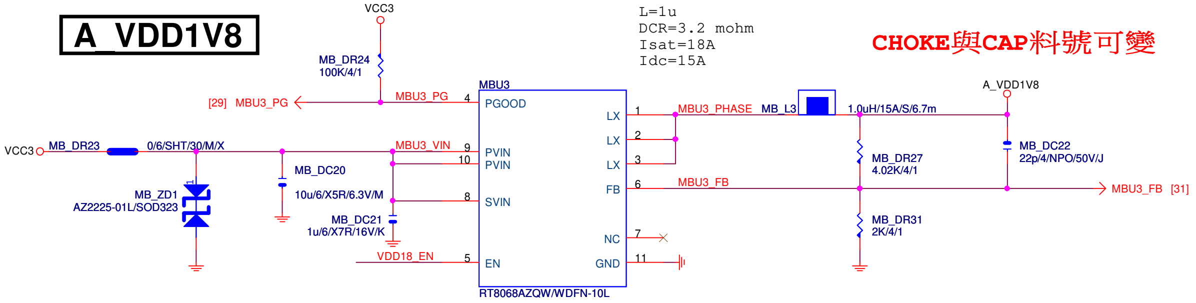
【技術通報R&D技術通報156】
RT9018(RICHTEK)與NCT3730(NUVOTON),
EM5103GE(EMC)做共用,針對PIN7(FB)分壓阻值部份
(R1/R2)須做修改為100K以上電阻值



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

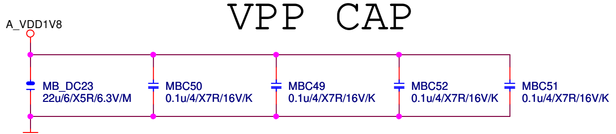
REV:0.4

A_VDD1V8



CHOKE與CAP料號可變

VPP CAP



22u*1PCS

GIGABYTE™
Title
FAN, A_VDD1V8
Size: Custom
Document Number: B550M DS3H
Rev: 1.0
Date: Monday, April 27, 2020
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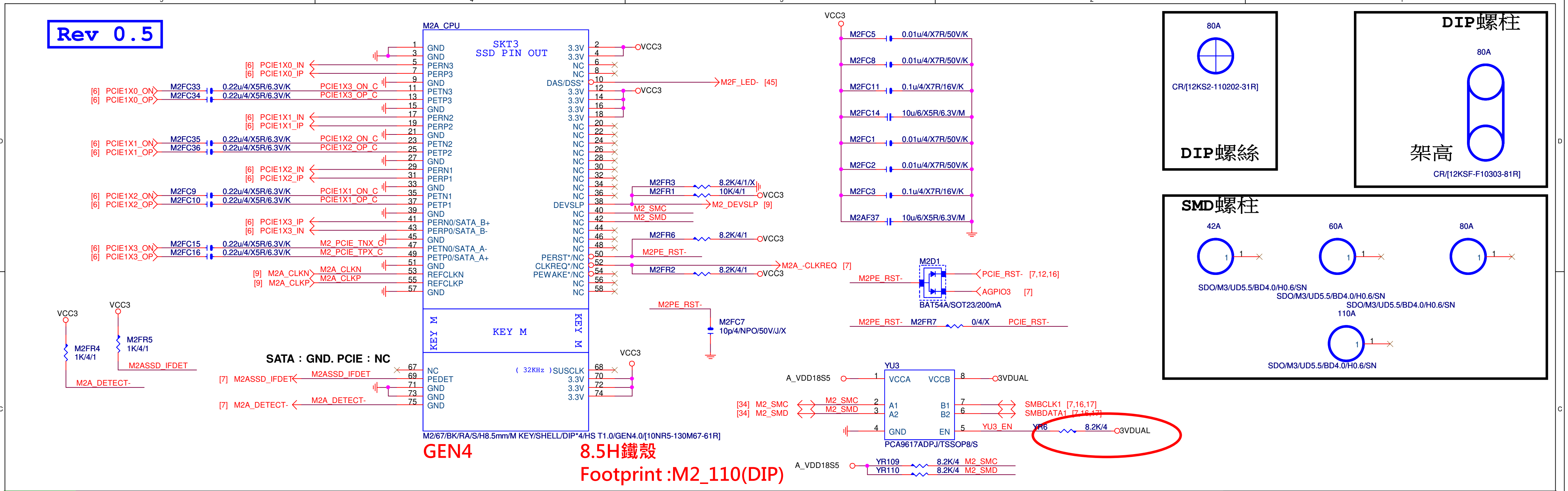

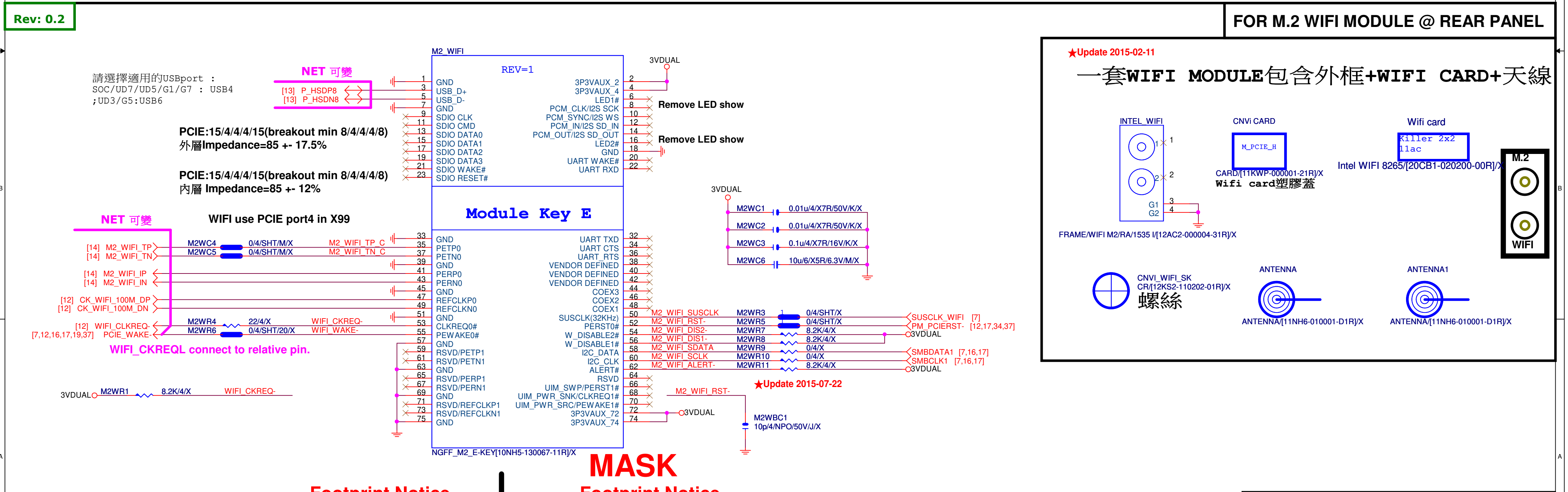

Footprint Notice.

★Update 2015-07-22

★Footprint for
直立式 SMD:
WIFI-EKEY

Footprint Notice.

★Update 2015-07-22

★Footprint for
橫躺式SMD: NGFF-E-75P-2

GIGABYTE™

Title	M.2 SOCKET
Size Custom	Document Number B550M DS3H
Rev	1.0
Date:	Wednesday, June 03, 2020
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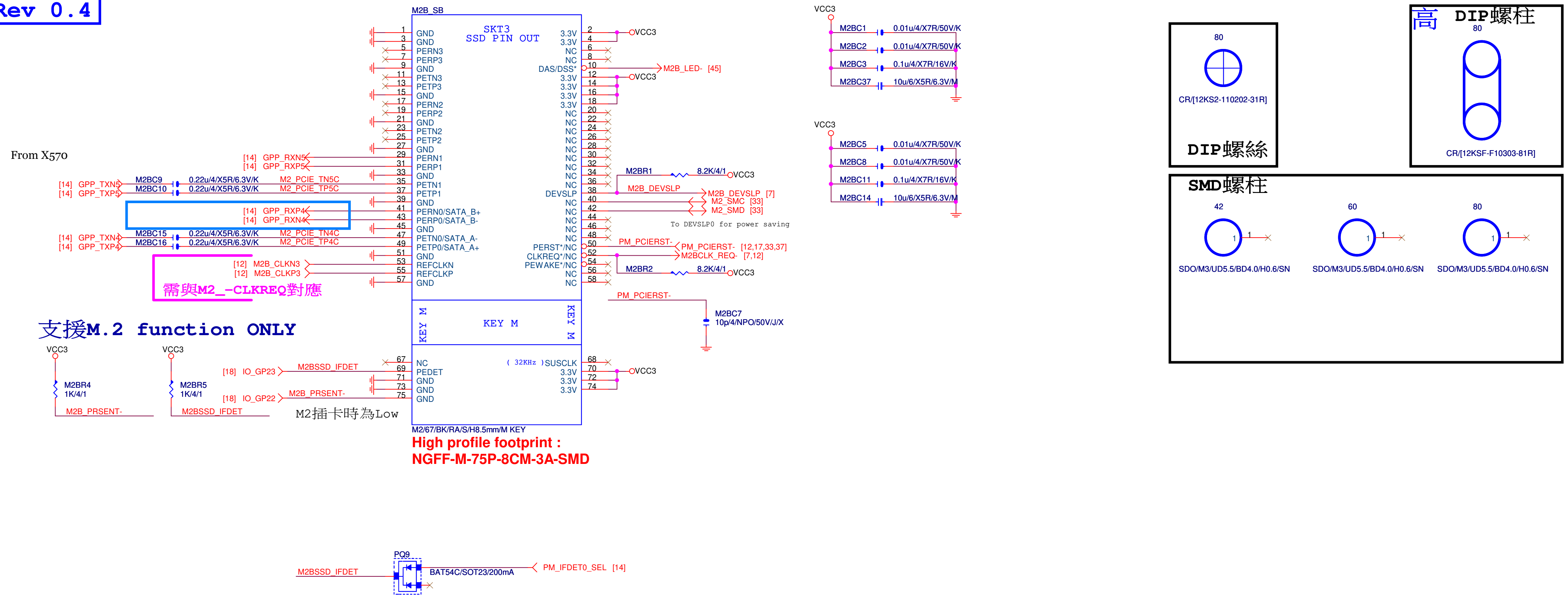
Rev 0.4



高 DIP螺柱

DIP螺絲

SMD螺柱

需與M2_-CLKREQ對應

支援M.2 function ONLY

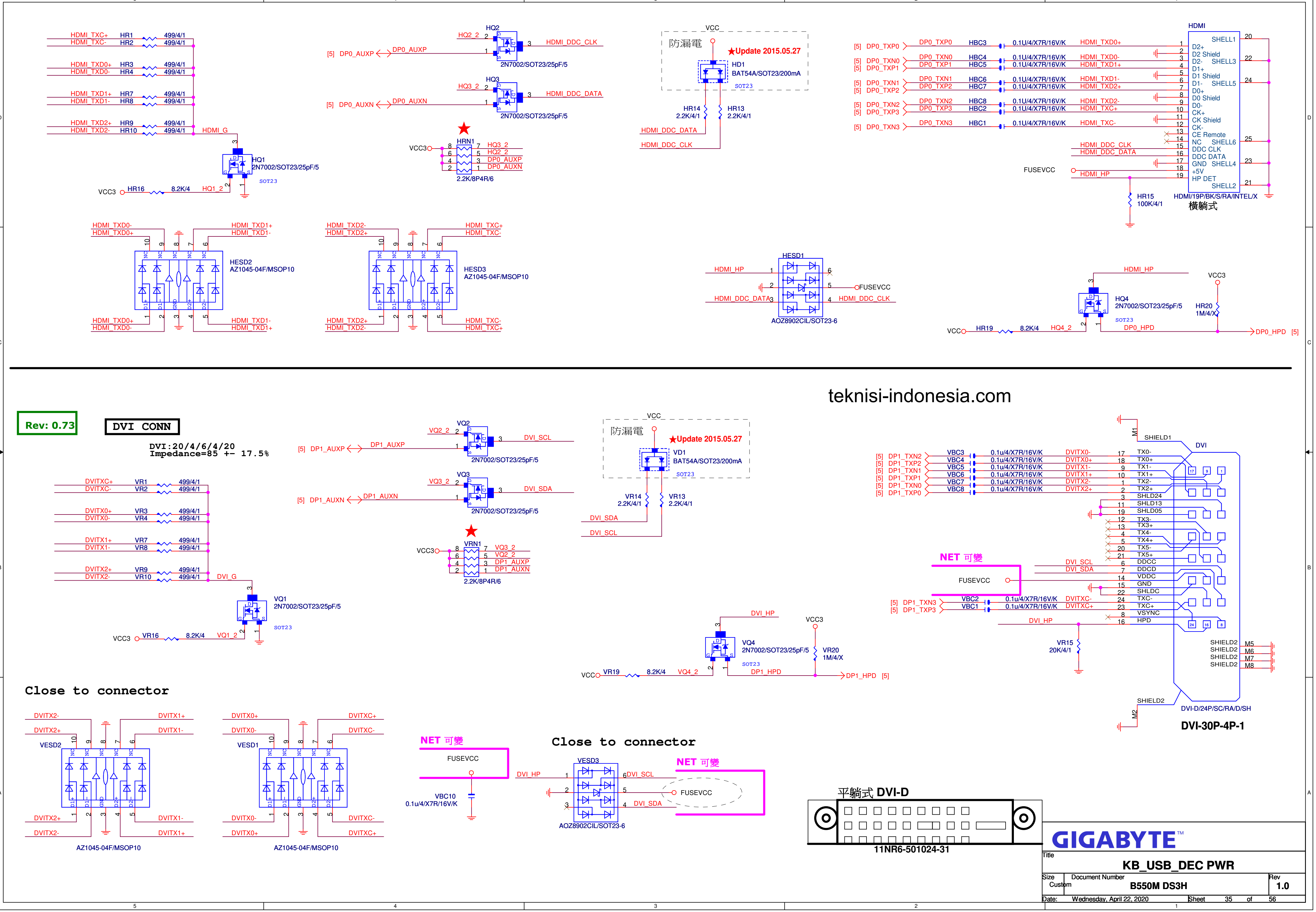
M2插卡時為Low

High profile footprint :
NGFF-M-75P-8CM-3A-SMD

刪除M2C_SOCKET & PU1

GIGABYTE™

Title	M.2 SLOT FROM PCH(B)	
Size Custom	Document Number B550M DS3H	Rev 1.0
Date: Wednesday, April 22, 2020	Sheet 34 of 45	



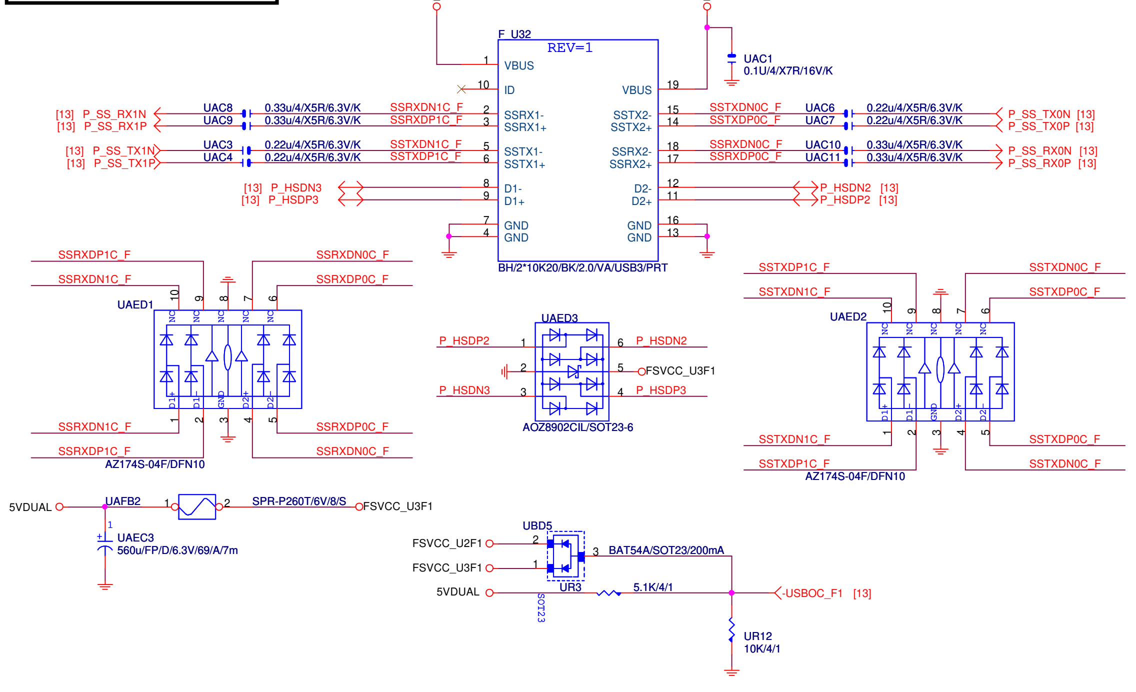
GIGABYTE™

Title: KB_USB_DEC PWR

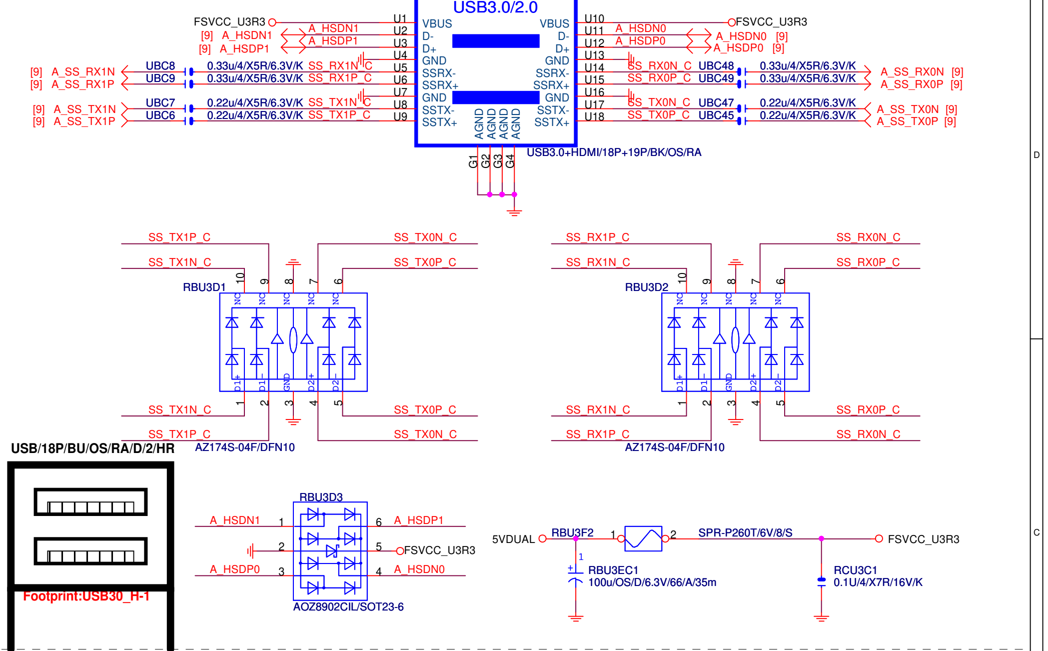
Size: Custom | Document Number: B550M DS3H | Rev: 1.0

Date: Wednesday, April 22, 2020 | Sheet 35 of 56

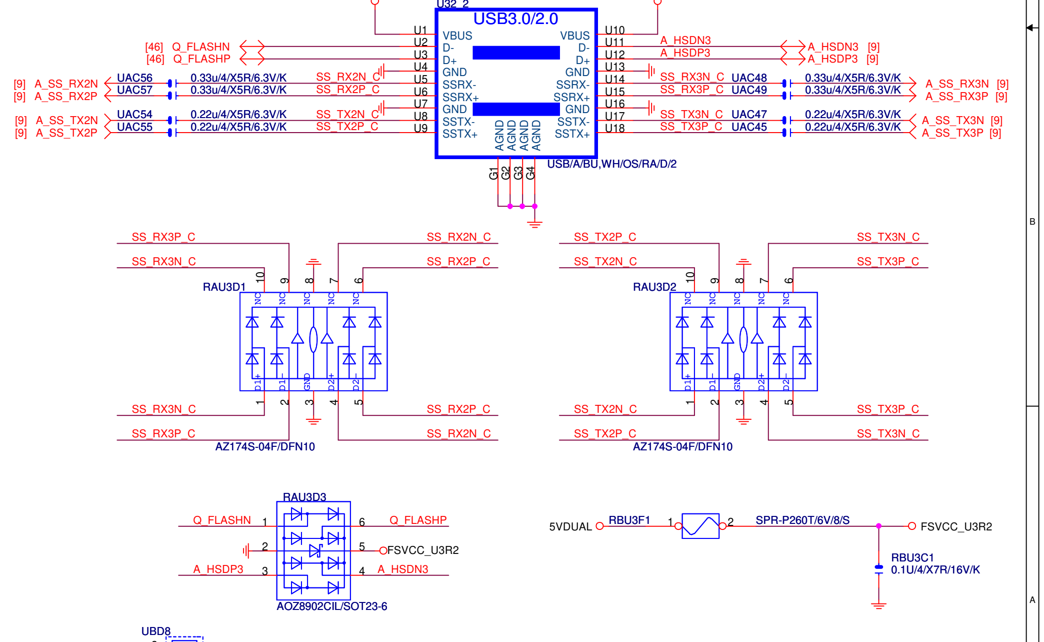
FRONT SIDE USB30



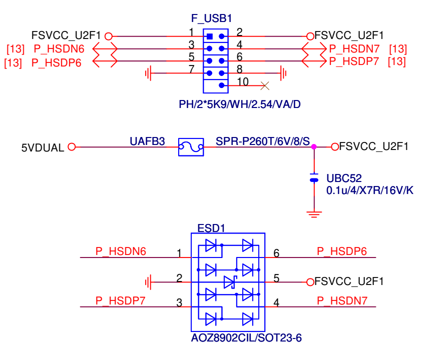
CPU SIDE



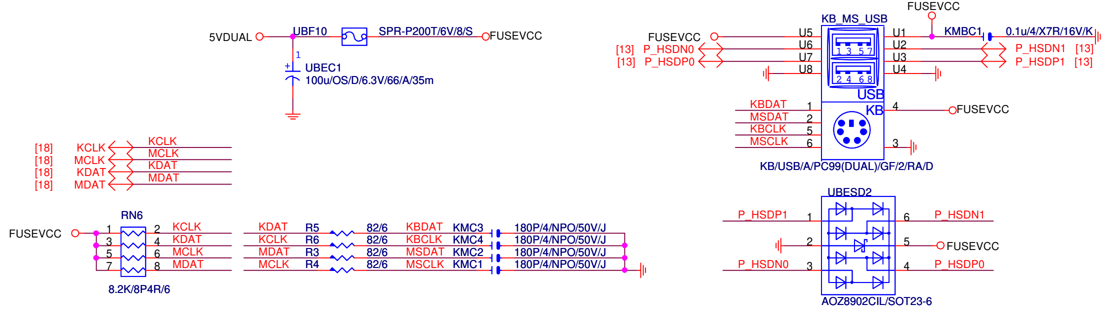
CPU SIDE

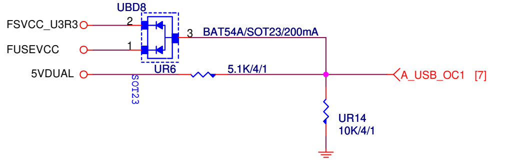


FRONT SIDE USB1



KB/MS & USB





GIGABYTE™

Title
F_USB ,F_USB30 ,R_USB30 , KB_MS_USB

Size	Document Number	Rev
Custom	B550M DS3H	1.0

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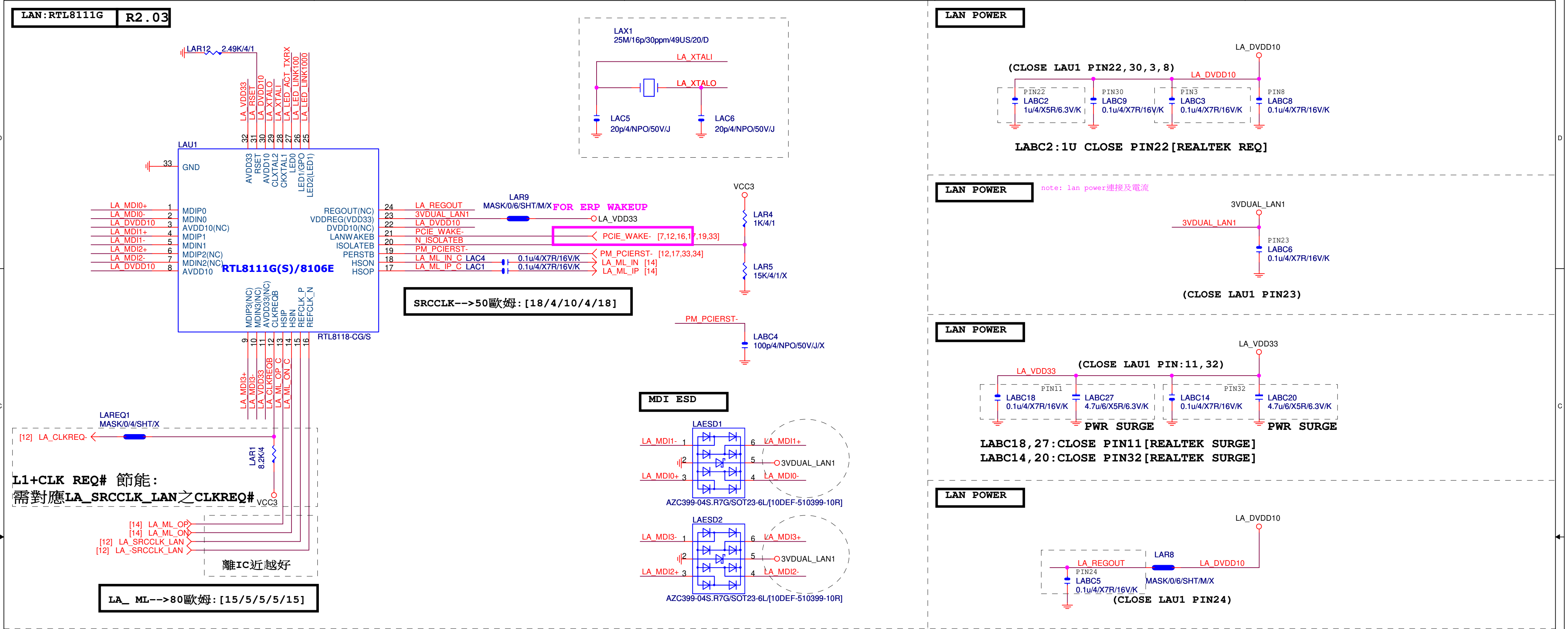

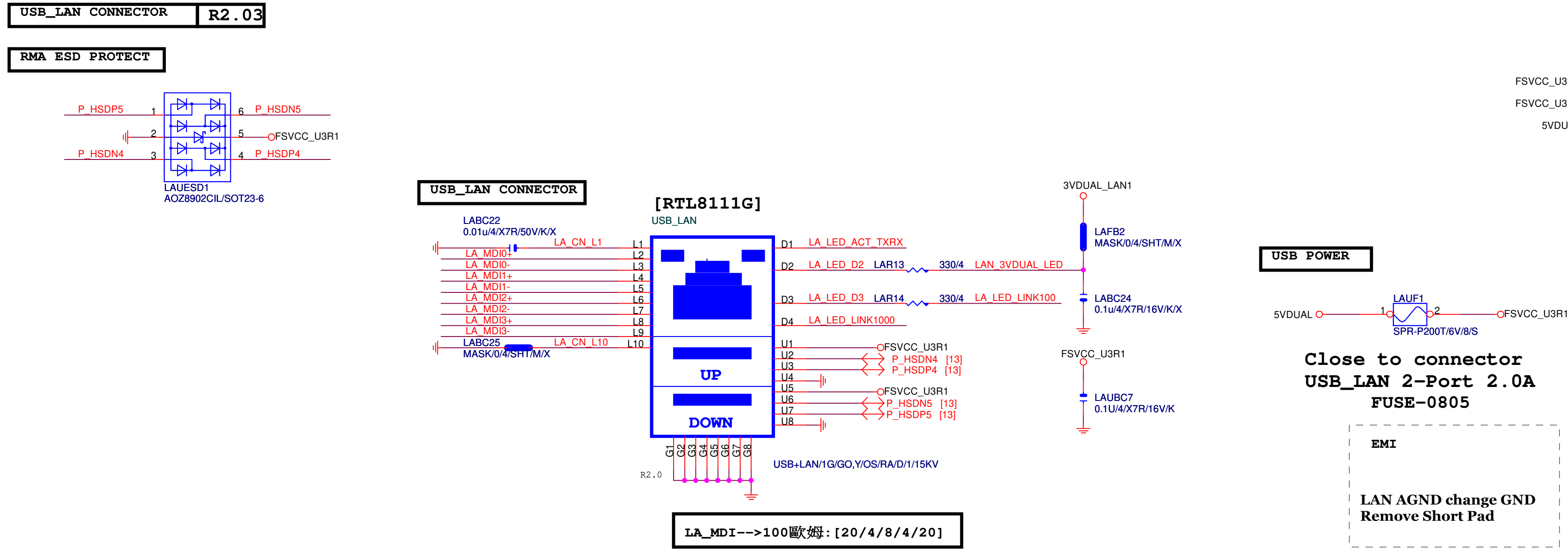

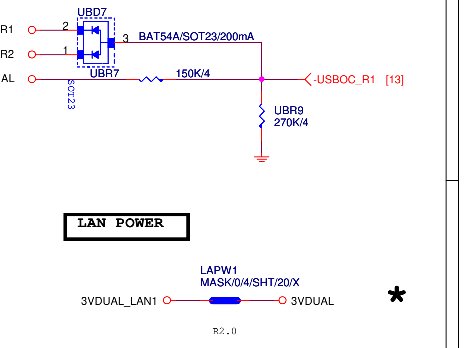

GIGABYTE™

Title
RTL8111G

Size: Custom
Document Number: B550M DS3H
Rev: 1.0

Date: Wednesday, April 22, 2020
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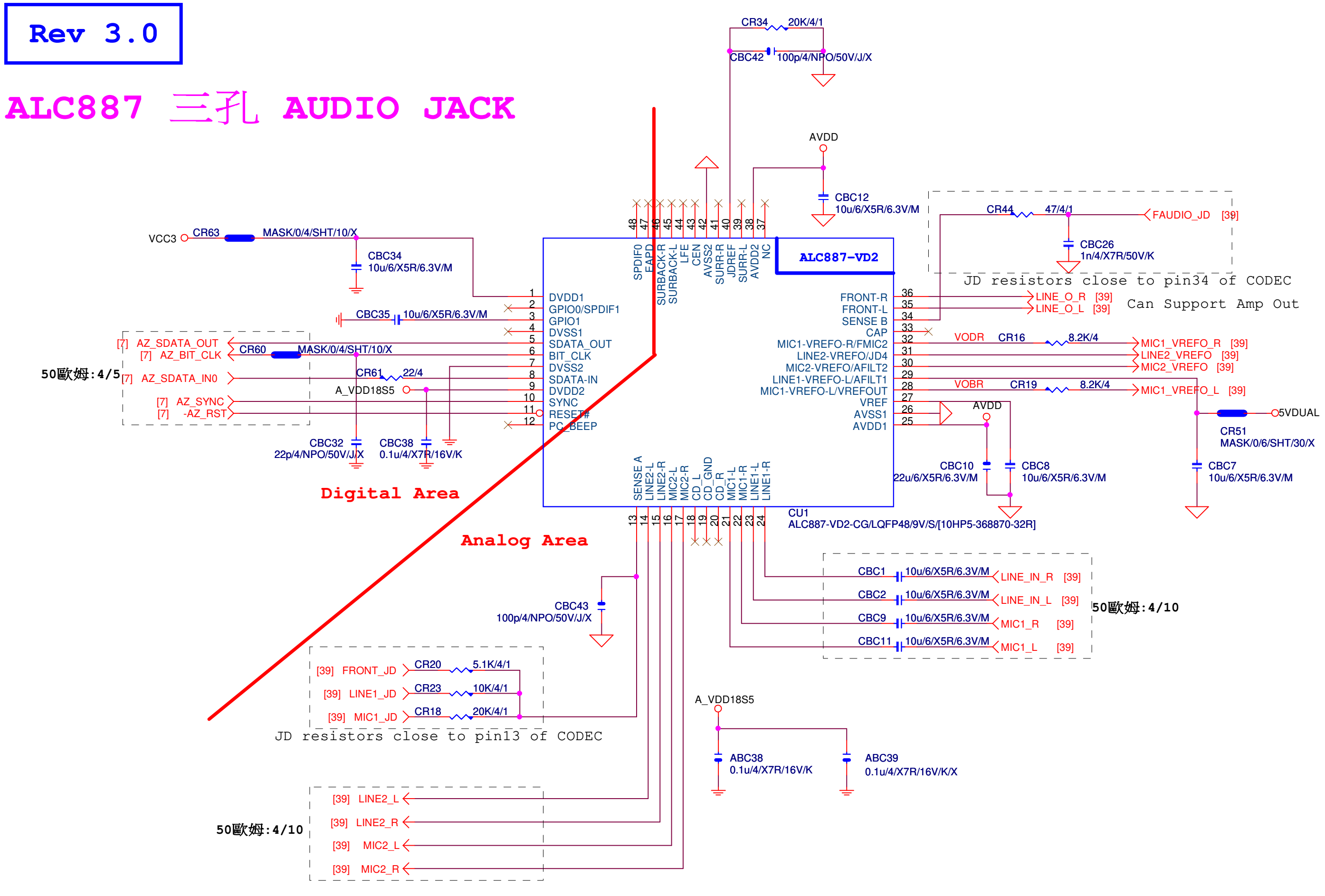
Rev 3.0

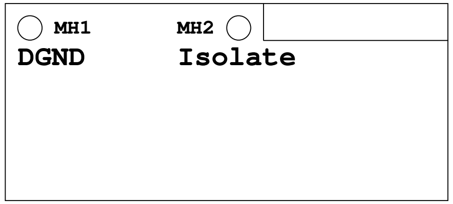
ALC887 三孔 AUDIO JACK



LAYOUT注意:螺絲孔下GND方式

1. MH1空間夠,下DGND
空間不夠,改為Isolate

2. MH2一律改為Isolate



GIGABYTE™

Title
ALC887 REAR

Size: Custom
Document Number: B550M DS3H
Rev: 1.0

Date: Wednesday, April 22, 2020
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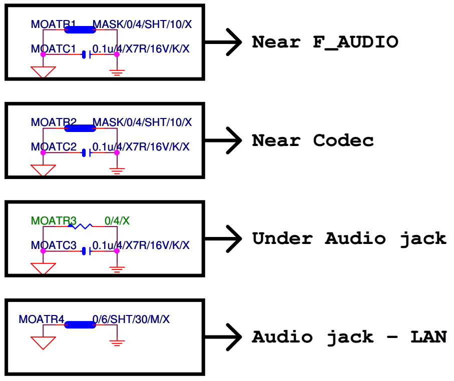
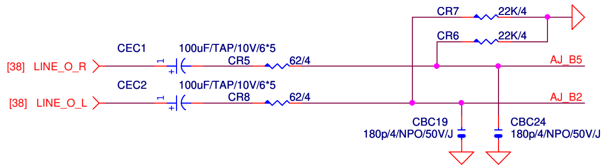
Rev 3.0

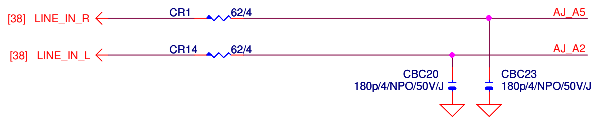


*量產前,0ohm改short pad

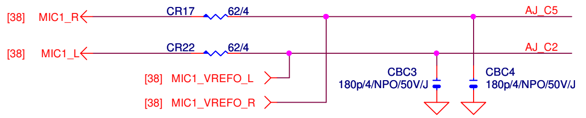
LINE-OUT



LINE-IN



MIC-IN



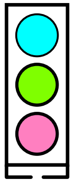
SURROUND

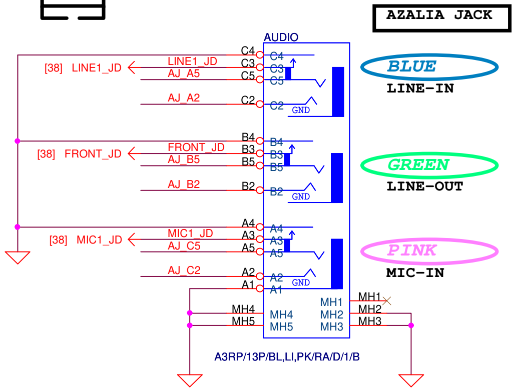
teknisi-indonesia.com

CEN/LFE

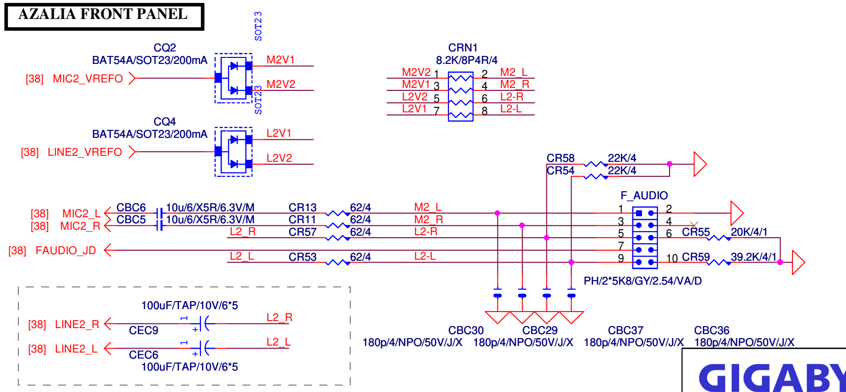
SURR BACK

AZALIA JACK





AZALIA FRONT PANEL



GIGABYTE™

Title
AUDIO JACK

Size	Document Number	Rev
Custom	B550M DS3H	1.0

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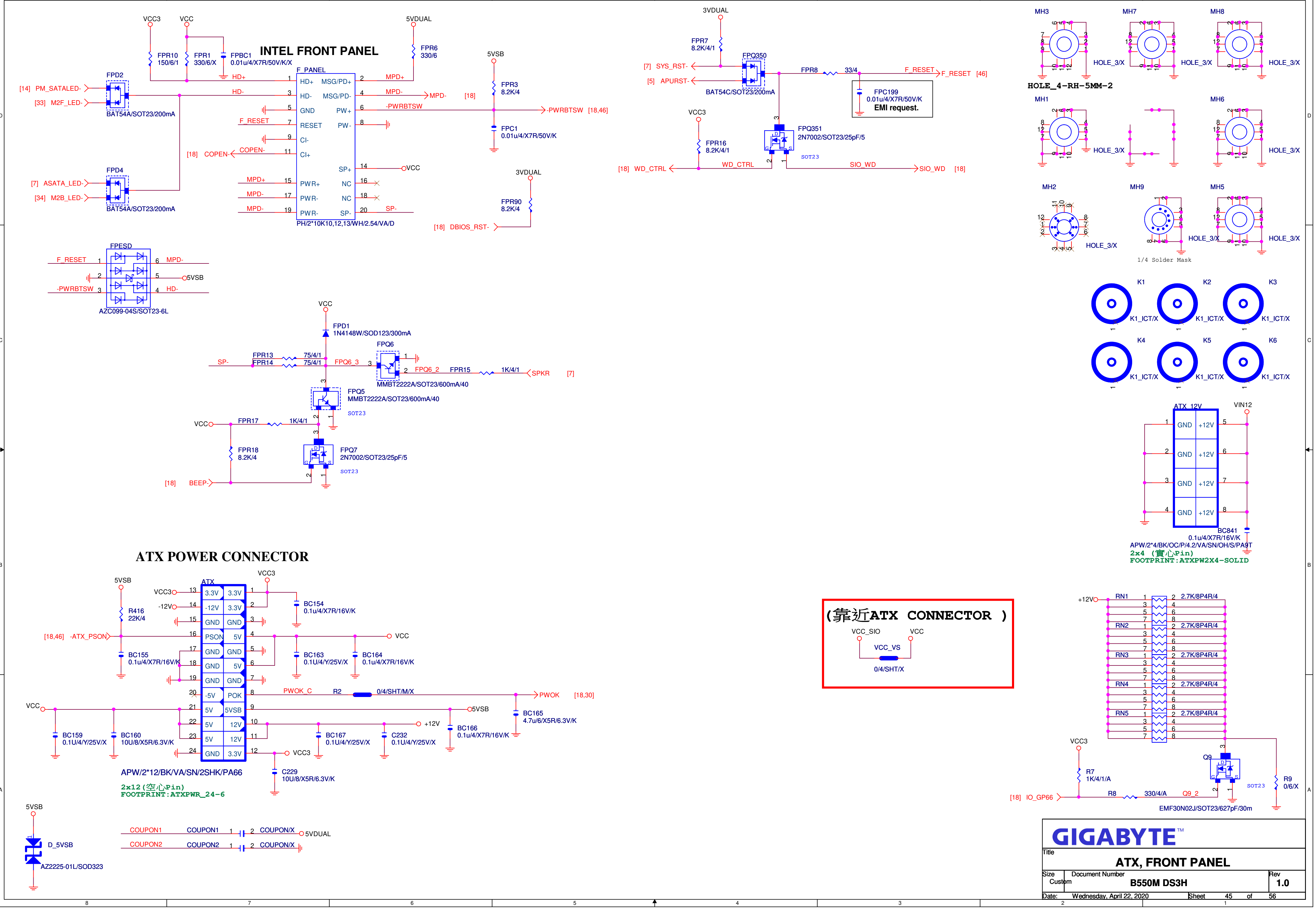

GIGABYTE

Title
ATX, FRONT PANEL

Size	Document Number	Rev
Custom	B550M DS3H	1.0

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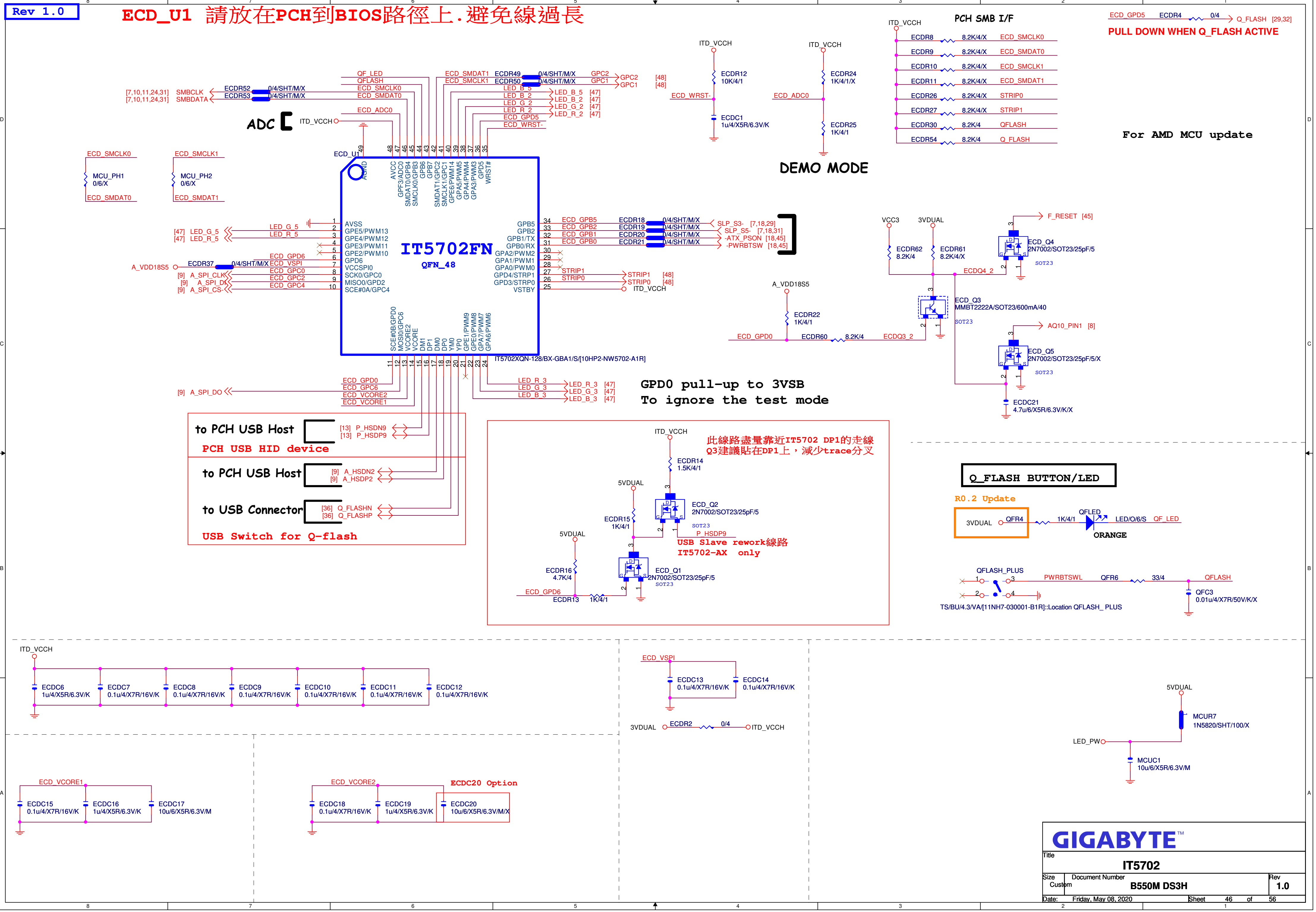

ECD_U1 請放在PCH到BIOS路徑上.避免線過長

PULL DOWN WHEN Q_FLASH ACTIVE

For AMD MCU update

DEMO MODE

GPD0 pull-up to 3VSB
To ignore the test mode

to PCH USB Host
PCH USB HID device

to PCH USB Host

to USB Connector
USB Switch for Q-flash

此線路盡量靠近IT5702 DP1的走線
Q3建議貼在DP1上，減少trace分叉

USB Slave rework線路
IT5702-AX only

Q_FLASH BUTTON/LED

R0.2 Update

ECDC20 Option

GIGABYTE™
Title
IT5702
Size Custom
Document Number B550M DS3H
Rev 1.0
Date: Friday, May 08, 2020
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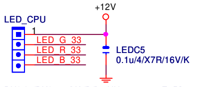
Rev 1.0

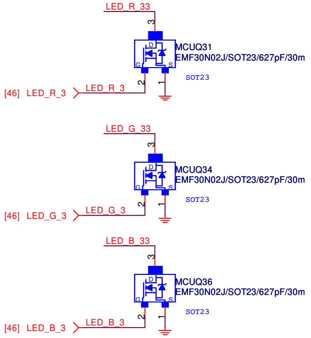
第三區 LED

燈條 LED (LED_CPU放在CPU附近位置)



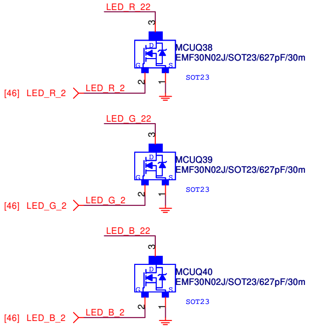
Footprint "PH1X4-FAN-AMD-L"

第三區 LED CONTROL

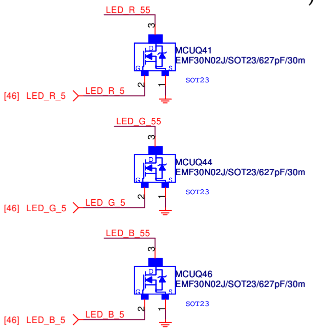


第五區 LED

第二區 LED CONTROL

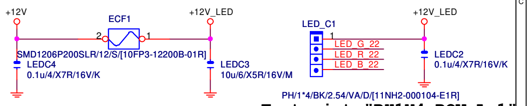


第五區 LED CONTROL

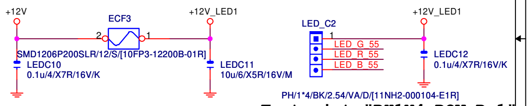


燈條 LED (LED_C1放在PCB左邊板邊位置)

燈條 LED (LED_C2放在PCB右邊板邊位置)



Footprint "PH1X4-ROW-L-1"



Footprint "PH1X4-ROW-R-1"

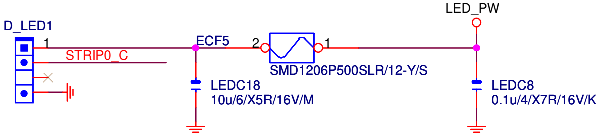
第四區 LED

GIGABYTE™		
Title CPU/AUDIO/LED_C		
Size Custom	Document Number B550M DS3H	Rev 1.0
Date: Wednesday, April 22, 2020	Sheet 47 of 56	

Rev 1.0

第六區 LED (靠近左上板邊位置)

Digital LED Strip1

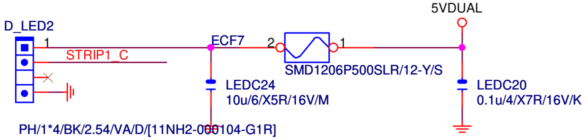


PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

Footprint PH1X4-CUT3-LED-L

第七區(靠近右下CPU板邊位置)

Digital LED Strip2

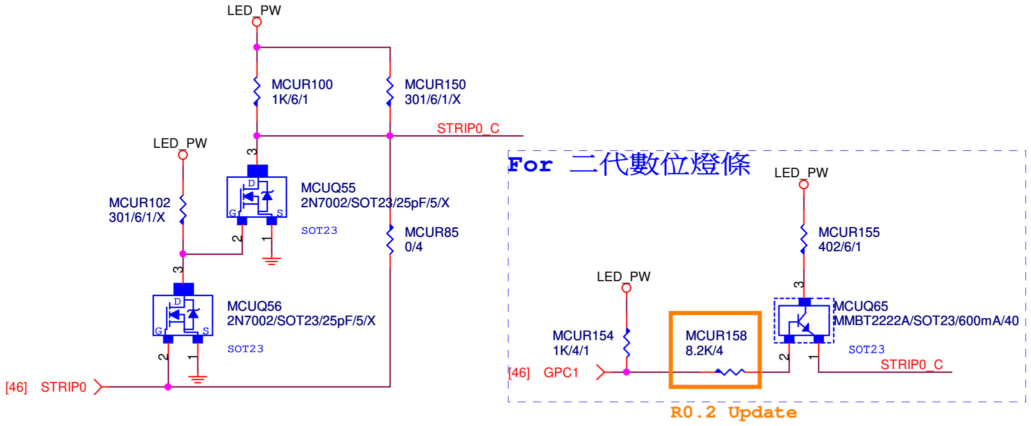


PH/1*4/BK/2.54/VA/D/[11NH2-000104-G1R]

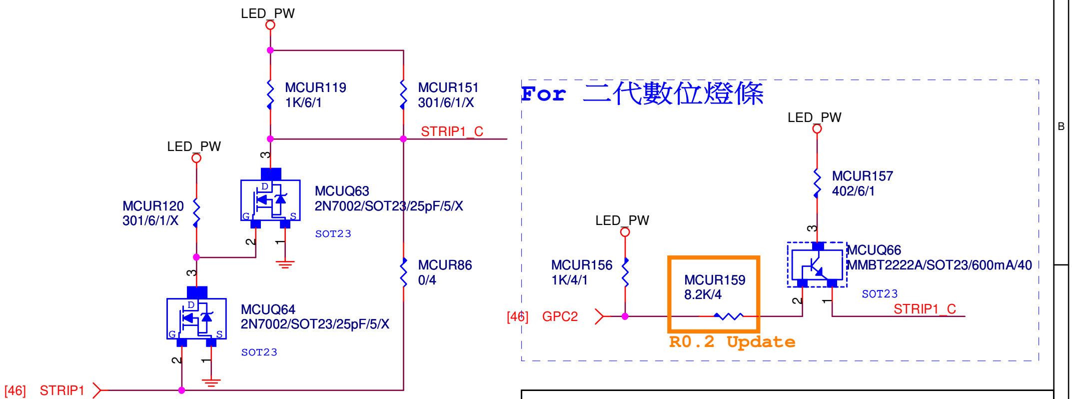
Footprint "PH1X4-CUT3-LED-R"

(for pin-name 與 model-name 同方向)

燈條 Level shift



燈條 Level shift



GIGABYTE™

Title	D_LED	
Size Custom	Document Number B550M DS3H	Rev 1.0
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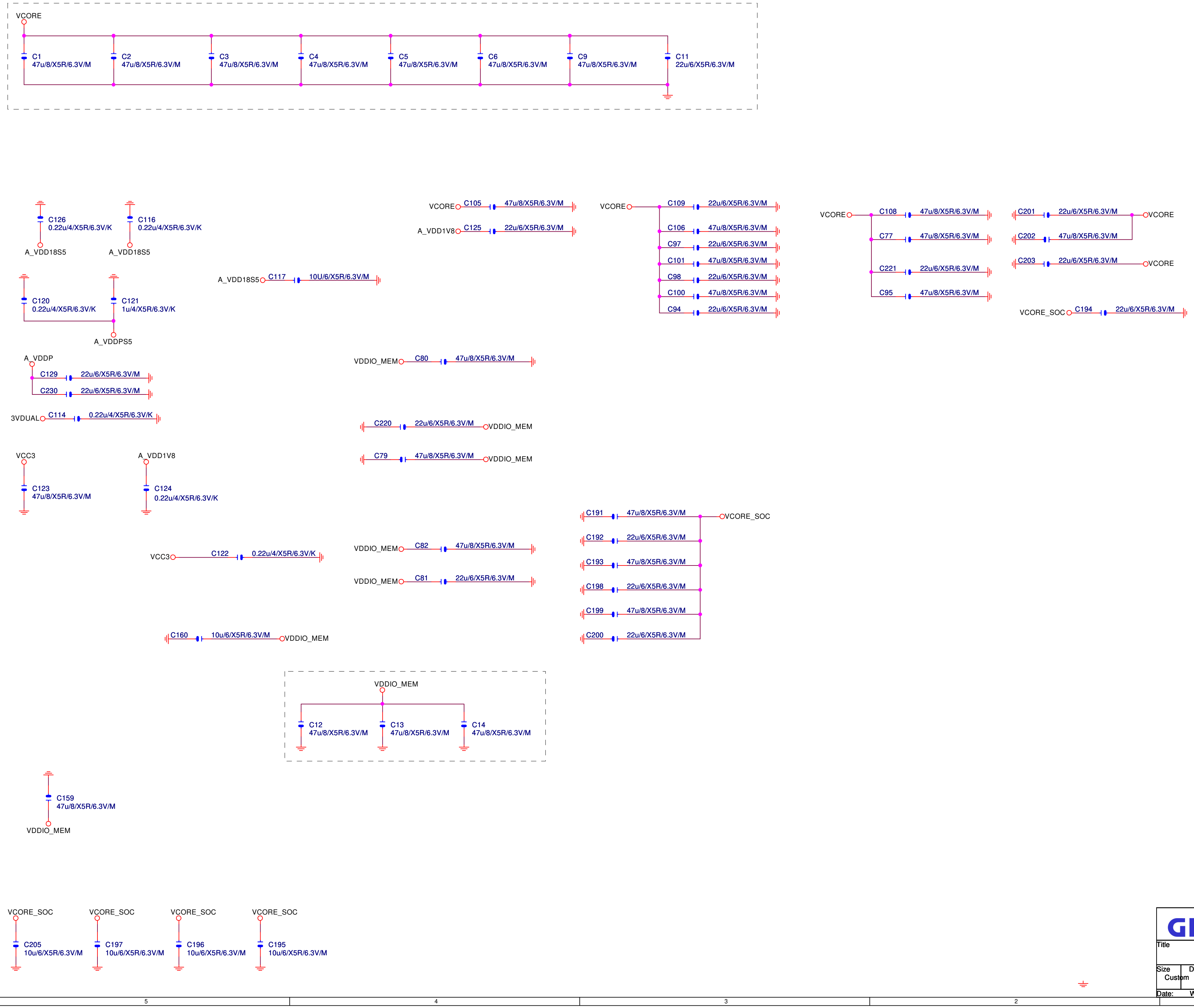

GIGABYTE™

Title
CPU BOTTOM CAP

Size	Document Number	Rev
Custom	B550M DS3H	1.0

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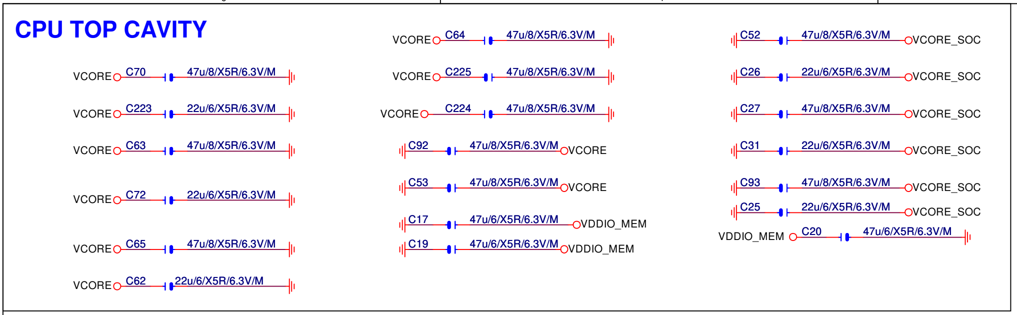

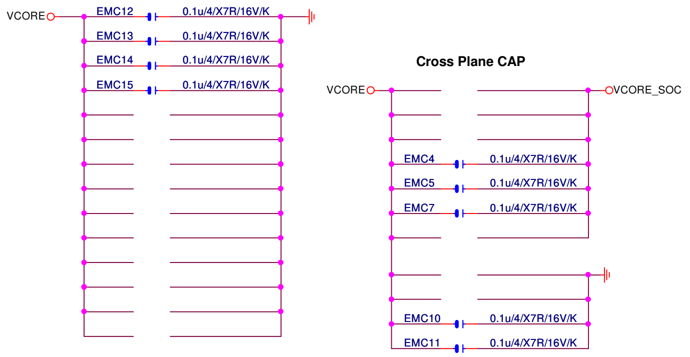

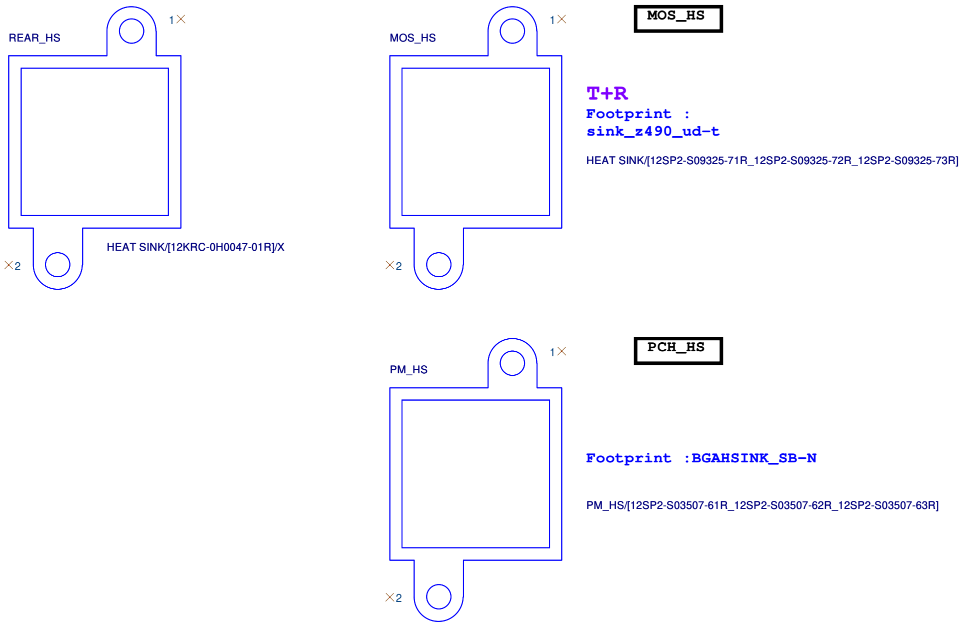

GIGABYTE™

Title
CPU TOP CAP

Size: Custom
Document Number: **B550M DS3H**
Rev: **1.0**

Date: Wednesday, April 22, 2020 Sheet 55 of 56