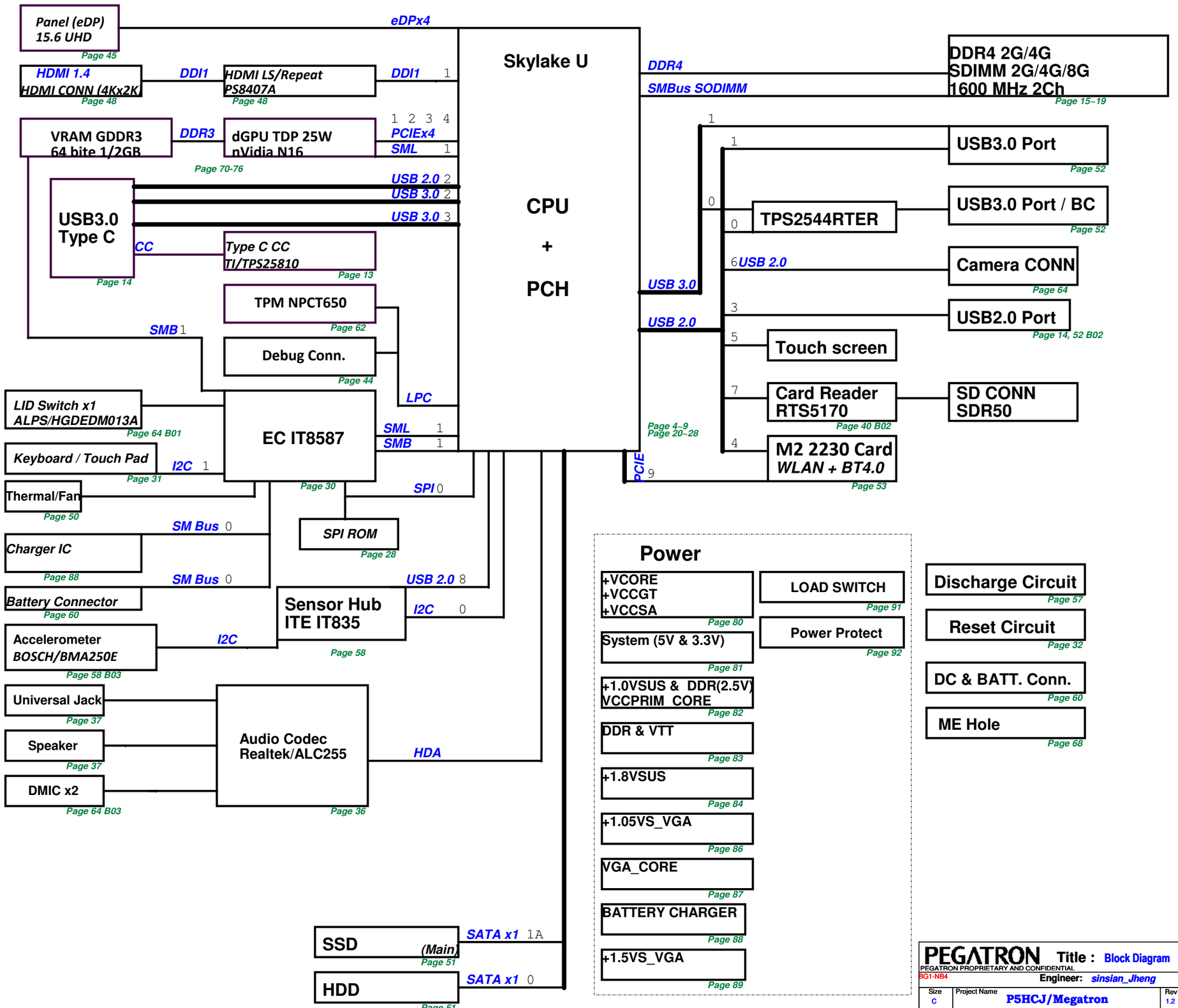
SYSTEM PAGE REF.

P5HCJ Block Diagram



PEGATRON Title : Block Diagram
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 1 of 96

Option

```
N/A   ---> Mount
/@    ---> Unmount
/RTL  ---> 10DN Support Array Mic
/ADSP ---> 08DN Support Stereo Mic
/Debug ---> Debug only
/TPM ---> Support TPM function
/NON-IOAC ---> Not support IOAC
/IOAC ---> Support IOAC
/SSD ---> Support SATA SSD
/HDD ---> Support HDD
/UMA ---> Support UMA
/VGA ---> Support VGA
/VGA_VRAM --> VRAM selection
/GC6 ---> Support GC6 function
/NGC6 ---> Not support GC6 function
/SEQS_EC
/BYPAS_EC
/E_SENSOR_HUB
/USBSLP
/EMI
```

PEGATRON Title : Option

<OrgName> Engineer: Ryen_Yen

Size	Project Name	Rev
C	P5HCJ_Megatron	1.2

Date: Friday, February 05, 2016 Sheet 2 of 96

03

CPU(1)_DDI_eDP

+VCCIO — +VCCIO 7,9,91
+VCCST_CPU — +VCCST_CPU 5,7,9,25,32
+VCCSTG — +VCCSTG 5,7
+3VS — +3VS 4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+3VSUS_ORG — +3VSUS_ORG 20,21,22,23,25,26

SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000

U0301A

DDI Port 1: HDMI

48 DDI1_TXN0 — DDI1_TXN0 E55 — DDI1_TXN[0]
48 DDI1_TXP0 — DDI1_TXP0 F55 — DDI1_TXP[0]
48 DDI1_TXN1 — DDI1_TXN1 E58 — DDI1_TXN[1]
48 DDI1_TXP1 — DDI1_TXP1 F58 — DDI1_TXP[1]
48 DDI1_TXN2 — DDI1_TXN2 F53 — DDI1_TXN[2]
48 DDI1_TXP2 — DDI1_TXP2 G53 — DDI1_TXP[2]
48 DDI1_TXN3 — DDI1_TXN3 F56 — DDI1_TXN[3]
48 DDI1_TXP3 — DDI1_TXP3 G56 — DDI1_TXP[3]

C50 — DDI2_TXN[0]
D50 — DDI2_TXP[0]
C52 — DDI2_TXN[1]
D52 — DDI2_TXP[1]
A50 — DDI2_TXN[2]
B50 — DDI2_TXP[2]
D51 — DDI2_TXN[3]
C51 — DDI2_TXP[3]

DDI

48 DDPB_CTRLCLK — DDPB_CTRLCLK L13 — GPP_E18/DDPB_CTRLCLK
48 DDPB_CTRLDATA — DDPB_CTRLDATA L12 — GPP_E19/DDPB_CTRLDATA
DDPC_CTRLCLK N7 — GPP_E20/DDPC_CTRLCLK
DDPC_CTRLDATA N8 — GPP_E21/DDPC_CTRLDATA
N11 — GPP_E22
N12 — GPP_E23

+VCCIO
R0301 2 1% 1 24.9Ohm — DP_COMP E52 — eDP_RCOMP

DISPLAY SIDEBANDS

EDP

EDP_TXN[0] — C47 EDP_TXN0 — EDP_TXN0 45
EDP_TXP[0] — C46 EDP_TXP0 — EDP_TXP0 45
EDP_TXN[1] — D46 EDP_TXN1 — EDP_TXN1 45
EDP_TXP[1] — C45 EDP_TXP1 — EDP_TXP1 45
EDP_TXN[2] — A45 EDP_TXN2 — EDP_TXN2 45
EDP_TXP[2] — B45 EDP_TXP2 — EDP_TXP2 45
EDP_TXN[3] — A47 EDP_TXN3 — EDP_TXN3 45
EDP_TXP[3] — B47 EDP_TXP3 — EDP_TXP3 45

eDP x 4
-- UHD 4 Lane
-- FHD 2 Lane

EDP_AUXN — E45 EDP_AUXN — EDP_AUXN 45
EDP_AUXP — F45 EDP_AUXP — EDP_AUXP 45

AUX For eDP

EDP_DISP_UTIL — B52

DDI1_AUXN — G50
DDI1_AUXP — F50
DDI2_AUXN — E48
DDI2_AUXP — F48
RSVD_1 — G46
RSVD_2 — F46

GPP_E13/DDPB_HPD0 — L9 DDI1_HPD — DDI1_HPD 48
GPP_E14/DDPC_HPD1 — L7 DDI2_HPD
GPP_E15/DDPD_HPD2 — L6 EXT_SMI#_R — R0302 1 2 0Ohm — EXT_SMI# — EXT_SMI# 30,44
GPP_E16/DDPE_HPD3 — N9 EXT_SCI#_R — R0303 1 2 0Ohm — EXT_SCI# — EXT_SCI# 30
GPP_E17/EDP_HPD — L10 eDP_HPD — eDP_HPD 45

eDP_BKLTEN — R12 LCD_BKLTEN_PCH — LCD_BKLTEN_PCH 21,45
eDP_BKLTCTL — R11 LCD_BL_PWM_PCH — LCD_BL_PWM_PCH 45
eDP_VDDEN — U13 EDP_VDD_EN — EDP_VDD_EN 45

940432 N/A
01V010000015

DDPB_CTRLDATA
DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
  1 : port is deteccted

+3VS
DDPB_CTRLDATA R0304 1 @ 2 2.2KOhm
DDPC_CTRLDATA R0305 1 @ 2 2.2KOhm
DDPB_CTRLCLK R0338 1 @ 2 2.2KOhm
DDPC_CTRLCLK R0340 1 @ 2 2.2KOhm

+3VS
EXT_SCI# R0307 1 2 10KOhm
EXT_SMI# R0308 1 2 10KOhm

DDPC_HPD
DP: 100Kohm pull down on PCH Side
HDMI: 20Kohm pull down
DDI2_HPD R0337 1 @ 2 100KOhm

+VCCST_CPU — R0311 1KOhm
+VCCSTG — R0312 1KOhm 5%
141024 follow PDG V1.0 Table 10-4
Rpu = 1K ohm 5%
Rs = 500 ohm 5%
Closeer EC
+VCCST_CPU — R0313 49.9Ohm 1% @

32 H_THRMTRIP# — H_PROCHOT# — R0314 1 2 499Ohm — 30 H_PECI_EC — R0315 1 2 43Ohm — SP0301 1 2 T0306 1 SKTOCC#

TP_CATERR#_R — D63 — CATERR#
H_PECI — A54 — PECI
H_PROCHOT#_R — C65 — PROCHOT#
H_THRMTRIP#_R — C63 — THERMTRIP#
SKTOCC# — A65

CPU MISC

C55 — BPM#[0]
D55 — BPM#[1]
B54 — BPM#[2]
C56 — BPM#[3]

T0311 1 CPU_GP0 — A6 — GPP_E3/CPU_GP0
T0312 1 CPU_GP1 — A7 — GPP_E7/CPU_GP1
T0313 1 CPU_GP2 — BA5 — GPP_B3/CPU_GP2
T0314 1 CPU_GP3 — AY5 — GPP_B4/CPU_GP3

R0316 1 2 49.9Ohm — CPU_POPIRCOMP — AT16 — PROC_POPIRCOMP
R0317 1 2 49.9Ohm — PCH_POPIRCOMP — AU16 — PCH_OPIRCOMP
R0318 1 2 49.9Ohm — EDRAM_OPIO_RCOMP — H66 — OPCE_RCOMP
R0319 1 2 49.9Ohm — EOPIO_RCOMP — H65 — OPC_RCOMP

JTAG

PROC_TCK — B61 XDP_TCLK
PROC_TDI — D60 XDP_TDI_CPU
PROC_TDO — A61 XDP_TDO_CPU
PROC_TMS — C60 XDP_TMS_CPU
PROC_TRST# — B59 XDP_TRST_CPU_N

PCH_JTAG_TCK — B56 PCH_JTAG_TCLK — 1 T0315
PCH_JTAG_TDI — D59 PCH_JTAG_TDI
PCH_JTAG_TDO — A56 PCH_JTAG_TDO
PCH_JTAG_TMS — C59 PCH_JTAG_TMS
PCH_TRST# — C61 PCH_TRST_CPU_N
JTAGX — A59 XDP_TCLK_JTAGX

Modify to XDP less

XDP Less Default Mount

+VCCSTG
PCH_JTAG_TDO XDP_TDO_CPU R0323 2 1 51Ohm
PCH_JTAG_TMS XDP_TMS_CPU — 1 T0316
PCH_TRST_CPU_N XDP_TRST_CPU_N — 1 T0317
PCH_JTAG_TDI XDP_TDI_CPU — 1 T0318
XDP_TCLK_JTAGX XDP_TCLK R0324 2 1 51Ohm

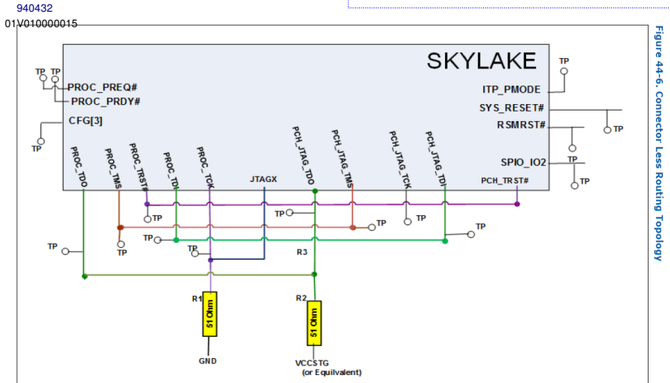
XDP Less Default Mount

940432
01V010000015

30 THRO_CPU — Q0301 2N7002 — R0341 2 3 1 0Ohm — H_PROCHOT#

R0341由EC control 觸發時的對地電阻也是要介於 70-200 ohm
(depends on under-shoot measurement result), 預留0ohm是調整空間

88 PROCHOT# — R0325 2 1 0Ohm
80 VR_HOT# — R0320 2 1 0Ohm



-- Stubs on JTAG nets should not more than 200ps
-- R1, R2 should be placed to within 200ps of PROC_TCK pin, PCH_JTAG_TDO, respectively
-- Place Test point pads on Secondary side
-- Route These Signals to Test Points: JTAG pins, ITP_PMODE, PROC_PREQ#, PROC_PRDY#, RSMRST#,SYS_RESET#, CFG[3], SPIO_IO2
VCCOPS_AB (PCH V1.0 A), GND pins (2)
-- TP should be placed to within 250ps of the respetive Skylake pins, and the distance between TP and termination (for JTAG, if any) must be within 200ps.
-- TP = Test Point Pad (size - 18 mil min, 25 mil preferred) The pad side must meet the industrial standard of Boundary Scan Test.

Figure 44-6. Connector Less Routing Topology

EMI 2015/10/12

+1.2V
C0301 0.1UF/25V @

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : CPU(1)_DDI_eDP

BG1-NB4

Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

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04

Memory bus_DDR4

+1.2V — +1.2V 3,7,15,16,17,18,19,57,83

+3VSUS — +3VSUS 21,24,25,26,28,30,31,51,53,62,63,81,92

+3VS — +3VS 3,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92

16,17 M_A_D[63:0]

U0301B

Used Interleave

Byte_0	M_A_D0	AL71	DDR0_DQ[0]	DDR0_CKN[0]	AU53	M_A_DIM0_CK_DDR0_DN	M_A_DIM0_CK_DDR0_DN 15,16,17
	M_A_D1	AL68	DDR0_DQ[1]	DDR0_CKP[0]	AT53	M_A_DIM0_CK_DDR0_DP	M_A_DIM0_CK_DDR0_DP 15,16,17
	M_A_D2	AN68	DDR0_DQ[2]	DDR0_CKN[1]	AU55		
	M_A_D3	AN69	DDR0_DQ[3]	DDR0_CKP[1]	AT55		
	M_A_D4	AL70	DDR0_DQ[4]	DDR0_CKE[0]	BA56	M_A_DIM0_CKE0	M_A_DIM0_CKE0 15,16,17
	M_A_D5	AL69	DDR0_DQ[5]	DDR0_CKE[1]	BB56		
	M_A_D6	AN70	DDR0_DQ[6]	DDR0_CKE[2]	AW56		
	M_A_D7	AN71	DDR0_DQ[7]	DDR0_CKE[3]	AY56		
	M_A_D8	AR70	DDR0_DQ[8]	DDR0_CS#[0]	AU45	M_A_DIM0_CS0_N	M_A_DIM0_CS0_N 15,16,17
	M_A_D9	AR68	DDR0_DQ[9]	DDR0_CS#[1]	AU43		
Byte_1	M_A_D10	AU71	DDR0_DQ[10]	DDR0_ODT[0]	AT45	M_A_DIM0_ODT0	M_A_DIM0_ODT0 15,16,17
	M_A_D11	AU68	DDR0_DQ[11]	DDR0_ODT[1]	AT43		
	M_A_D12	AR71	DDR0_DQ[12]		BA51	M_A_A5	M_A_A5 15,16,17
	M_A_D13	AR69	DDR0_DQ[13]	DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5]	BB54	M_A_A9	M_A_A9 15,16,17
	M_A_D14	AU70	DDR0_DQ[14]	DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9]	BD56	M_A_A6	M_A_A6 15,16,17
	M_A_D15	AU69	DDR0_DQ[15]	DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6]	AY52	M_A_A8	M_A_A8 15,16,17
Byte_2	M_A_D16	BB65	DDR0_DQ[16]/DDR0_DQ[32]	DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8]	AW52	M_A_A7	M_A_A7 15,16,17
	M_A_D17	AW65	DDR0_DQ[17]/DDR0_DQ[33]	DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7]	AY55	M_A_BG0	M_A_BG0 15,16,17
	M_A_D18	AW63	DDR0_DQ[18]/DDR0_DQ[34]	DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0]	AW54	M_A_A12	M_A_A12 15,16,17
	M_A_D19	AY63	DDR0_DQ[19]/DDR0_DQ[35]	DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12]	BA54	M_A_A11	M_A_A11 15,16,17
	M_A_D20	BA65	DDR0_DQ[20]/DDR0_DQ[36]	DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11]	BA55	M_A_ACT_N	M_A_ACT_N 15,16,17
	M_A_D21	AY65	DDR0_DQ[21]/DDR0_DQ[37]	DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT#	AY54		
	M_A_D22	BA63	DDR0_DQ[22]/DDR0_DQ[38]	DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1]			
	M_A_D23	BB63	DDR0_DQ[23]/DDR0_DQ[39]	DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13]	AU46	M_A_A13	M_A_A13 15,16,17
	M_A_D24	BA61	DDR0_DQ[24]/DDR0_DQ[40]	DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AU48	M_A_A15_CAS_N	M_A_A15_CAS_N 15,16,17
	M_A_D25	AW61	DDR0_DQ[25]/DDR0_DQ[41]	DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AT46	M_A_A14_WE_N	M_A_A14_WE_N 15,16,17
Byte_3	M_A_D26	BB59	DDR0_DQ[26]/DDR0_DQ[42]	DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16]	AU50	M_A_A16_RAS_N	M_A_A16_RAS_N 15,16,17
	M_A_D27	AW59	DDR0_DQ[27]/DDR0_DQ[43]	DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0]	AU52	M_A_BA0	M_A_BA0 15,16,17
	M_A_D28	BB61	DDR0_DQ[28]/DDR0_DQ[44]	DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2]	AY51	M_A_A2	M_A_A2 15,16,17
	M_A_D29	AY61	DDR0_DQ[29]/DDR0_DQ[45]	DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1]	AT48	M_A_BA1	M_A_BA1 15,16,17
	M_A_D30	BA59	DDR0_DQ[30]/DDR0_DQ[46]	DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10]	AT50	M_A_A10_AP	M_A_A10_AP 15,16,17
	M_A_D31	AY59	DDR0_DQ[31]/DDR0_DQ[47]	DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1]	BB50	M_A_A1	M_A_A1 15,16,17
	M_A_D32	AY39	DDR0_DQ[32]/DDR1_DQ[0]	DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0]	AY50	M_A_A0	M_A_A0 15,16,17
	M_A_D33	AW39	DDR0_DQ[33]/DDR1_DQ[1]	DDR0_MA[3]	BA50	M_A_A3	M_A_A3 15,16,17
	M_A_D34	AY37	DDR0_DQ[34]/DDR1_DQ[2]	DDR0_MA[4]	BB52	M_A_A4	M_A_A4 15,16,17
Byte_4	M_A_D35	AW37	DDR0_DQ[35]/DDR1_DQ[3]				
	M_A_D36	BB39	DDR0_DQ[36]/DDR1_DQ[4]	DDR0_DQSN[0]	AM70	M_A_DQS_DN0	M_A_DQS_DN0 16
	M_A_D37	BA39	DDR0_DQ[37]/DDR1_DQ[5]	DDR0_DQSP[0]	AM69	M_A_DQS_DP0	M_A_DQS_DP0 16
	M_A_D38	BA37	DDR0_DQ[38]/DDR1_DQ[6]	DDR0_DQSN[1]	AT69	M_A_DQS_DN1	M_A_DQS_DN1 16
	M_A_D39	BB37	DDR0_DQ[39]/DDR1_DQ[7]	DDR0_DQSP[1]	AT70	M_A_DQS_DP1	M_A_DQS_DP1 16
	M_A_D40	AY35	DDR0_DQ[40]/DDR1_DQ[8]	IL Channel A DQS[0..7]	BA64	M_A_DQS_DN2	M_A_DQS_DN2 16
	M_A_D41	AW35	DDR0_DQ[41]/DDR1_DQ[9]	DDR0_DQSN[2]/DDR0_DQSN[4]	AY64	M_A_DQS_DP2	M_A_DQS_DP2 16
	M_A_D42	AY33	DDR0_DQ[42]/DDR1_DQ[10]	DDR0_DQSP[2]/DDR0_DQSP[4]	AY60	M_A_DQS_DN3	M_A_DQS_DN3 16
Byte_5	M_A_D43	AW33	DDR0_DQ[43]/DDR1_DQ[11]	DDR0_DQSN[3]/DDR0_DQSP[5]	BA60	M_A_DQS_DP3	M_A_DQS_DP3 16
	M_A_D44	BB35	DDR0_DQ[44]/DDR1_DQ[12]	DDR0_DQSP[3]/DDR0_DQSN[5]	BB38	M_A_DQS_DN4	M_A_DQS_DN4 17
	M_A_D45	BA35	DDR0_DQ[45]/DDR1_DQ[13]	DDR0_DQSN[4]/DDR1_DQSN[0]	AY38	M_A_DQS_DP4	M_A_DQS_DP4 17
	M_A_D46	BA33	DDR0_DQ[46]/DDR1_DQ[14]	DDR0_DQSP[4]/DDR1_DQSP[0]	AY34	M_A_DQS_DN5	M_A_DQS_DN5 17
	M_A_D47	BB33	DDR0_DQ[47]/DDR1_DQ[15]	DDR0_DQSN[5]/DDR1_DQSN[1]	BA34	M_A_DQS_DP5	M_A_DQS_DP5 17
	M_A_D48	AY31	DDR0_DQ[48]/DDR1_DQ[32]	DDR0_DQSP[5]/DDR1_DQSP[1]	BA30	M_A_DQS_DN6	M_A_DQS_DN6 17
	M_A_D49	AW31	DDR0_DQ[49]/DDR1_DQ[33]	DDR0_DQSN[6]/DDR1_DQSN[4]	AY30	M_A_DQS_DP6	M_A_DQS_DP6 17
Byte_6	M_A_D50	AY29	DDR0_DQ[50]/DDR1_DQ[34]	DDR0_DQSP[6]/DDR1_DQSP[4]	AY26	M_A_DQS_DN7	M_A_DQS_DN7 17
	M_A_D51	AW29	DDR0_DQ[51]/DDR1_DQ[35]	DDR0_DQSN[7]/DDR1_DQSN[5]	BA26	M_A_DQS_DP7	M_A_DQS_DP7 17
	M_A_D52	BB31	DDR0_DQ[52]/DDR1_DQ[36]	DDR0_DQSP[7]/DDR1_DQSP[5]			
	M_A_D53	BA31	DDR0_DQ[53]/DDR1_DQ[37]		AW50	DDR0_A_ALERT_N	DDR0_A_ALERT_N 15,16,17
	M_A_D54	BA29	DDR0_DQ[54]/DDR1_DQ[38]	DDR0_ALERT#	AT52	DDR0_A_PARITY	DDR0_A_PARITY 15,16,17
	M_A_D55	BB29	DDR0_DQ[55]/DDR1_DQ[39]	DDR0_PAR			
Byte_7	M_A_D56	AY27	DDR0_DQ[56]/DDR1_DQ[40]	DDR_VREF_CA	AY67	+V_DDR_CA_VREF	+V_DDR_CA_VREF 19
	M_A_D57	AW27	DDR0_DQ[57]/DDR1_DQ[41]	DDR0_VREF_DQ	AY68		
	M_A_D58	AY25	DDR0_DQ[58]/DDR1_DQ[42]	DDR1_VREF_DQ	BA67	+V_DDR_VREFDQ02_CHB	+V_DDR_VREFDQ02_CHB 19
	M_A_D59	AW25	DDR0_DQ[59]/DDR1_DQ[43]	DDR_VTT_CNTL	AW67	DDR_VTT_CTRL	
	M_A_D60	BB27	DDR0_DQ[60]/DDR1_DQ[44]	DDR CH - A			
	M_A_D61	BA27	DDR0_DQ[61]/DDR1_DQ[45]				
	M_A_D62	BA25	DDR0_DQ[62]/DDR1_DQ[46]				
	M_A_D63	BB25	DDR0_DQ[63]/DDR1_DQ[47]				

940432

18 M_B_DQ[63:0]

SKL_ULT

U0301C

IL Channel B[0..63]

Byte_0	M_B_DQ0	AF65	DDR1_DQ[0]/DDR0_DQ[16]	DDR1_CKN[0]	AN45	M_B_DIM0_CK_DDR0_DN	M_B_DIM0_CK_DDR0_DN 18
	M_B_DQ1	AF64	DDR1_DQ[1]/DDR0_DQ[17]	DDR1_CKN[1]	AN46	M_B_DIM0_CK_DDR1_DN	M_B_DIM0_CK_DDR1_DN 18
	M_B_DQ2	AK65	DDR1_DQ[2]/DDR0_DQ[18]	DDR1_CKP[0]	AP45	M_B_DIM0_CK_DDR0_DP	M_B_DIM0_CK_DDR0_DP 18
	M_B_DQ3	AK64	DDR1_DQ[3]/DDR0_DQ[19]	DDR1_CKP[1]	AP46	M_B_DIM0_CK_DDR1_DP	M_B_DIM0_CK_DDR1_DP 18
	M_B_DQ4	AF66	DDR1_DQ[4]/DDR0_DQ[20]	DDR1_CKE[0]	AN56	M_B_DIM0_CKE0	
	M_B_DQ5	AF67	DDR1_DQ[5]/DDR0_DQ[21]	DDR1_CKE[1]	AP55	M_B_DIM0_CKE1	M_B_DIM0_CKE0 18
	M_B_DQ6	AK67	DDR1_DQ[6]/DDR0_DQ[22]	DDR1_CKE[2]	AN55		M_B_DIM0_CKE1 18
	M_B_DQ7	AK66	DDR1_DQ[7]/DDR0_DQ[23]	DDR1_CKE[3]	AP53		
	M_B_DQ8	AF70	DDR1_DQ[8]/DDR0_DQ[24]				
	M_B_DQ9	AF68	DDR1_DQ[9]/DDR0_DQ[25]	DDR1_CS#[0]	BB42	M_B_DIM0_CS0_N	
Byte_1	M_B_DQ10	AH71	DDR1_DQ[10]/DDR0_DQ[26]	DDR1_CS#[1]	AY42	M_B_DIM0_CS1_N	M_B_DIM0_CS0_N 18
	M_B_DQ11	AH68	DDR1_DQ[11]/DDR0_DQ[27]	DDR1_ODT[0]	BA42	M_B_DIM0_ODT0	M_B_DIM0_CS1_N 18
	M_B_DQ12	AF71	DDR1_DQ[12]/DDR0_DQ[28]	DDR1_ODT[1]	AW42	M_B_DIM0_ODT1	M_B_DIM0_ODT0 18
	M_B_DQ13	AF69	DDR1_DQ[13]/DDR0_DQ[29]				M_B_DIM0_ODT1 18
	M_B_DQ14	AH70	DDR1_DQ[14]/DDR0_DQ[30]		AY48	M_B_A5	
	M_B_DQ15	AH69	DDR1_DQ[15]/DDR0_DQ[31]	DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]	AP50	M_B_A9	M_B_A5 18
	M_B_DQ16	AT66	DDR1_DQ[16]/DDR0_DQ[48]	DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]	BA48	M_B_A6	M_B_A9 18
	M_B_DQ17	AU66	DDR1_DQ[17]/DDR0_DQ[49]	DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]	BB48	M_B_A8	M_B_A6 18
	M_B_DQ18	AP65	DDR1_DQ[18]/DDR0_DQ[50]	DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]	AP48	M_B_A7	M_B_A8 18
Byte_2	M_B_DQ19	AN65	DDR1_DQ[19]/DDR0_DQ[51]	DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]	AP52	M_B_BG0	M_B_A7 18
	M_B_DQ20	AN66	DDR1_DQ[20]/DDR0_DQ[52]	DDR1_BA[2]/DDR1_CAA[5]/DDR1_BG[0]	AN50	M_B_A12	M_B_BG0 18
	M_B_DQ21	AP66	DDR1_DQ[21]/DDR0_DQ[53]	DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]	AN48	M_B_A11	M_B_A12 18
	M_B_DQ22	AT65	DDR1_DQ[22]/DDR0_DQ[54]	DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]	AN53	M_B_ACT_N	M_B_A11 18
	M_B_DQ23	AU65	DDR1_DQ[23]/DDR0_DQ[55]	DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#	AN52	M_B_BG1	M_B_ACT_N 18
	M_B_DQ24	AT61	DDR1_DQ[24]/DDR0_DQ[56]	DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]			M_B_BG1 18
	M_B_DQ25	AU61	DDR1_DQ[25]/DDR0_DQ[57]		BA43	M_B_A13	
	M_B_DQ26	AP60	DDR1_DQ[26]/DDR0_DQ[58]	DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]	AY43	M_B_A15_CAS_N	M_B_A13 18
Byte_3	M_B_DQ27	AN60	DDR1_DQ[27]/DDR0_DQ[59]	DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AY44	M_B_A14_WE_N	M_B_A15_CAS_N 18
	M_B_DQ28	AN61	DDR1_DQ[28]/DDR0_DQ[60]	DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AW44	M_B_A16_RAS_N	M_B_A14_WE_N 18
	M_B_DQ29	AP61	DDR1_DQ[29]/DDR0_DQ[61]	DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]	BB44	M_B_BA0	M_B_A16_RAS_N 18
	M_B_DQ30	AT60	DDR1_DQ[30]/DDR0_DQ[62]	DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]	AY47	M_B_A2	M_B_BA0 18
	M_B_DQ31	AU60	DDR1_DQ[31]/DDR0_DQ[63]	DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]	BA44	M_B_BA1	M_B_A2 18
	M_B_DQ32	AU40	DDR1_DQ[32]/DDR1_DQ[16]	DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]	AW46	M_B_A10_AP	M_B_BA1 18
	M_B_DQ33	AT40	DDR1_DQ[33]/DDR1_DQ[17]	DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]	AY46	M_B_A1	M_B_A10_AP 18
	M_B_DQ34	AT37	DDR1_DQ[34]/DDR1_DQ[18]	DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]	BA46	M_B_A0	M_B_A1 18
Byte_4	M_B_DQ35	AU37	DDR1_DQ[35]/DDR1_DQ[19]	DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]	BB46	M_B_A3	M_B_A0 18
	M_B_DQ36	AR40	DDR1_DQ[36]/DDR1_DQ[20]	DDR1_MA[3]	BA47	M_B_A4	M_B_A3 18
	M_B_DQ37	AP40	DDR1_DQ[37]/DDR1_DQ[21]	DDR1_MA[4]			M_B_A4 18
	M_B_DQ38	AP37	DDR1_DQ[38]/DDR1_DQ[22]		AH66	M_B_DQS_DN0	
	M_B_DQ39	AR37	DDR1_DQ[39]/DDR1_DQ[23]	IL Channel B DQS[0..7]	AH65	M_B_DQS_DP0	M_B_DQS_DN0 18
	M_B_DQ40	AT33	DDR1_DQ[40]/DDR1_DQ[24]	DDR1_DQSN[0]/DDR0_DQSN[2]	AG69	M_B_DQS_DN1	M_B_DQS_DP0 18
	M_B_DQ41	AU33	DDR1_DQ[41]/DDR1_DQ[25]	DDR1_DQSP[0]/DDR0_DQSP[2]	AG70	M_B_DQS_DP1	M_B_DQS_DN1 18
	M_B_DQ42	AU30	DDR1_DQ[42]/DDR1_DQ[26]	DDR1_DQSN[1]/DDR0_DQSN[3]	AR66	M_B_DQS_DN2	M_B_DQS_DP1 18
Byte_5	M_B_DQ43	AT30	DDR1_DQ[43]/DDR1_DQ[27]	DDR1_DQSP[1]/DDR0_DQSP[3]	AR65	M_B_DQS_DP2	M_B_DQS_DN2 18
	M_B_DQ44	AR33	DDR1_DQ[44]/DDR1_DQ[28]	DDR1_DQSN[2]/DDR0_DQSN[6]	AR61	M_B_DQS_DN3	M_B_DQS_DP2 18
	M_B_DQ45	AP33	DDR1_DQ[45]/DDR1_DQ[29]	DDR1_DQSP[2]/DDR0_DQSP[6]	AR60	M_B_DQS_DP3	M_B_DQS_DN3 18
	M_B_DQ46	AR30	DDR1_DQ[46]/DDR1_DQ[30]	DDR1_DQSN[3]/DDR0_DQSN[7]	AT38	M_B_DQS_DN4	M_B_DQS_DP3 18
	M_B_DQ47	AP30	DDR1_DQ[47]/DDR1_DQ[31]	DDR1_DQSP[3]/DDR0_DQSP[7]	AR38	M_B_DQS_DP4	M_B_DQS_DN4 18
	M_B_DQ48	AU27	DDR1_DQ[48]	DDR1_DQSN[4]/DDR1_DQSN[2]	AT32	M_B_DQS_DN5	M_B_DQS_DP4 18
	M_B_DQ49	AT27	DDR1_DQ[49]	DDR1_DQSP[4]/DDR1_DQSP[2]	AR32	M_B_DQS_DP5	M_B_DQS_DN5 18
Byte_6	M_B_DQ50	AT25	DDR1_DQ[50]	DDR1_DQSN[5]/DDR1_DQSN[3]	AR25	M_B_DQS_DN6	M_B_DQS_DP5 18
	M_B_DQ51	AU25	DDR1_DQ[51]	DDR1_DQSP[5]/DDR1_DQSP[3]	AR27	M_B_DQS_DP6	M_B_DQS_DN6 18
	M_B_DQ52	AP27	DDR1_DQ[52]	DDR1_DQSN[6]	AR22	M_B_DQS_DP7	M_B_DQS_DP6 18
	M_B_DQ53	AN27	DDR1_DQ[53]	DDR1_DQSP[6]	AR21	M_B_DQS_DN7	M_B_DQS_DN7 18
	M_B_DQ54	AN25	DDR1_DQ[54]	DDR1_DQSN[7]			M_B_DQS_DP7 18
	M_B_DQ55	AP25	DDR1_DQ[55]	DDR1_DQSP[7]			
Byte_7	M_B_DQ56	AT22	DDR1_DQ[56]		AN43	DDR1_B_ALERT_N	
	M_B_DQ57	AU22	DDR1_DQ[57]	DDR1_ALERT#	AP43	DDR1_B_PARITY	DDR1_B_ALERT_N 18
	M_B_DQ58	AU21	DDR1_DQ[58]	DDR1_PAR	AT13	DDR4_DRAMRST_N	DDR1_B_PARITY 18
	M_B_DQ59	AT21	DDR1_DQ[59]	DRAM_RESET#	AR18	SM_RCOMP_0 R0402 1	2 121OHM
	M_B_DQ60	AN22	DDR1_DQ[60]	DDR_RCOMP[0]	AT18	SM_RCOMP_1 R0403 1	2 80.6Ohm
	M_B_DQ61	AP22	DDR1_DQ[61]	DDR_RCOMP[1]	AU18	SM_RCOMP_2 R0404 1	2 100Ohm
	M_B_DQ62	AP21	DDR1_DQ[62]	DDR_RCOMP[2]			
	M_B_DQ63	AN21	DDR1_DQ[63]	DDR CH - B			

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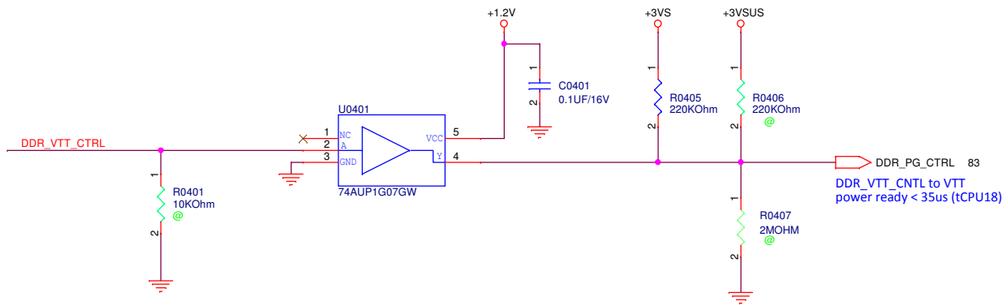

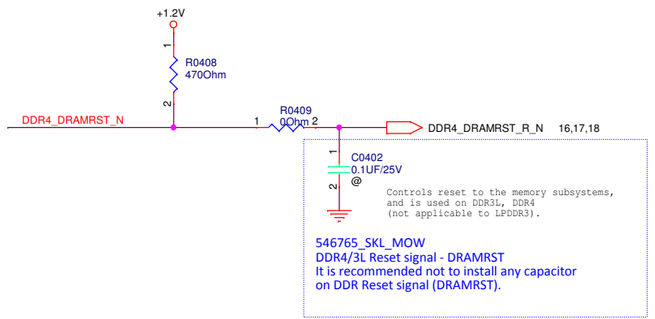

EMI 2015/10/12

Symbol U0301 B

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelA DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[0..15] DQS/DQS#[0,1]
BYTE 1		
BYTE 2		ChannelADQ[32..47] DQS/DQS#[4,5]
BYTE 3		
BYTE 4		ChannelB DQ[0..15] DQS/DQS#[0,1]
BYTE 5		
BYTE 6		ChannelB DQ[32..47] DQS/DQS#[4,5]
BYTE 7		

Symbol U0301 C

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelB DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[16..31] DQS/DQS#[2,3]
BYTE 1		
BYTE 2		ChannelADQ[48..63] DQS/DQS#[6,7]
BYTE 3		
BYTE 4		ChannelB DQ[16..31] DQS/DQS#[2,3]
BYTE 5		
BYTE 6		ChannelB DQ[48..63] DQS/DQS#[6,7]
BYTE 7		

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Title : Memory bus_DDR4

BG1-NB4

Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 4 of 96

05

CPU(3)_+VCCCORE

+VCCSTG → +VCCSTG 3,7
+VCCST_CPU → +VCCST_CPU 3,7,9,25,32
+VCORE → +VCORE 80
+1.8VSUS → +1.8VSUS 9,26,84

SKL 2+2, +V1.8VS_EDRAM / +V_EDRAM_VR / +V_EOPIO_VR
From Intel, SKL-U 2+2 reserve these pins PD to GND

+VCORE

U0301L
CPU POWER 1 OF 4

A30	VCC_1
A34	VCC_2
A39	VCC_3
A44	VCC_4
AK33	VCC_5
AK35	VCC_6
AK37	VCC_7
AK38	VCC_8
AK40	VCC_9
AL33	VCC_10
AL37	VCC_11
AL40	VCC_12
AM32	VCC_13
AM33	VCC_14
AM35	VCC_15
AM37	VCC_16
AM38	VCC_17
G30	VCC_18
K32	RSVD_3
AK32	RSVD_4
AB62	VCCOPC_1
P62	VCCOPC_2
V62	VCCOPC_3
H63	VCC_OPC_1P8_1
G61	VCC_OPC_1P8_2
AC63	VCCOPC_SENSE
AE63	VSSOPC_SENSE
AE62	VCCEOPIO_1
AG62	VCCEOPIO_2
AL63	VCCEOPIO_SENSE
AJ62	VSSEOPIO_SENSE

RSVD NC

R0528 1 2 0Ohm@
R0529 1 2 0Ohm
R0535 1 2 0Ohm
R0531 1 2 0Ohm
R0532 1 2 0Ohm
R0530 1 2 0Ohm
R0533 1 2 0Ohm
R0534 1 2 0Ohm

+VCORE

G32	VCC_19
G33	VCC_20
G35	VCC_21
G37	VCC_22
G38	VCC_23
G40	VCC_24
G42	VCC_25
J30	VCC_26
J33	VCC_27
J37	VCC_28
J40	VCC_29
K33	VCC_30
K35	VCC_31
K37	VCC_32
K38	VCC_33
K40	VCC_34
K42	VCC_35
K43	VCC_36
E32	VCC_SENSE
E33	VSS_SENSE
B63	VIDALERT#
A63	VIDSCK
D64	VIDSOUT
G20	VCCSTG

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Pull H/L near CPU side

R0536 1 1% 2 100Ohm → +VCORE
VCORE_VCCSENSE 80
VCORE_VSSSENSE 80
R0537 1 1% 2 100Ohm
VIDALERT# R0517 1 1% 2 220Ohm
VIDSCK R0518 1 2 0Ohm
VIDSOUT R0519 1 2 0Ohm
+VCCSTG
+VCCFUSEPRG SP0505 1 2
NB_R0402_20MIL_SMALL

CPU side | VR side

+VCCST_CPU
R0520 56Ohm 1%
VIDALERT#_R
VIDSCK_R
R0524 1 2 0Ohm → VR_SVID_ALERT# 80
R0522 45.3Ohm 1%
C0505 0.1UF/16V
R0525 1 1% 2 51Ohm → VR_SVID_CLK 80
R0521 100Ohm 1%
VIDSOUT_R
R0523 100Ohm 1%
R0526 1 1% 2 10Ohm → VR_SVID_DATA 80

PEGATRON
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BG1-NB4

Title: CPU(3)_+VCCCORE
Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 5 of 96

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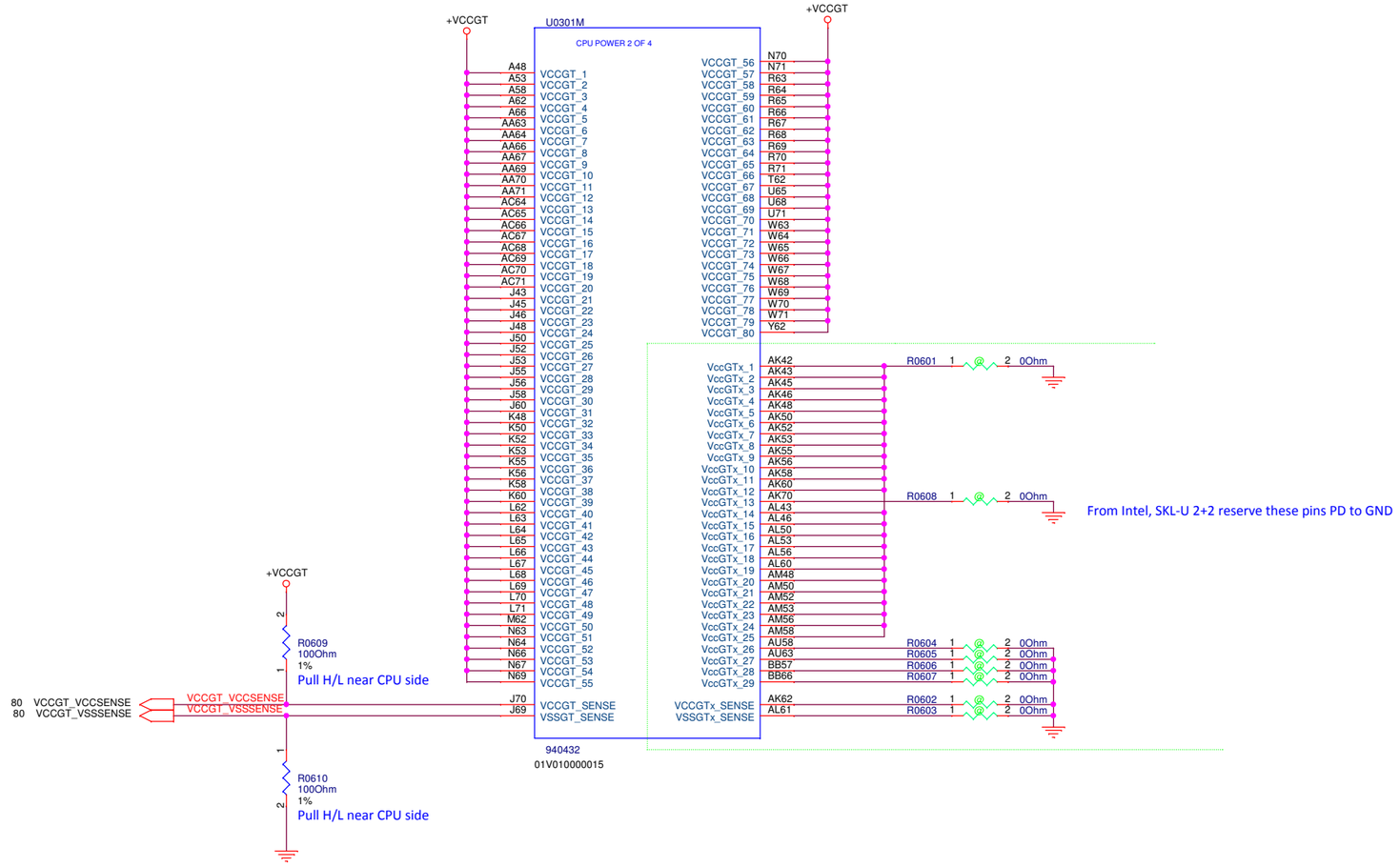
CPU(4)_+VCCGT

+VCCGT → +VCCGT 80



PEGATRON	Title : CPU(4)_+VCCGT	
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1-NB4	Engineer: sinsian_Jheng	
Size: C	Project Name: P5HCJ/Megatron	Rev: 1.2
Date: Friday, February 05, 2016	Sheet 6 of 96	

07

CPU(5)_+VDDQ/IO/SA

+1.2V +1.2V 3,4,15,16,17,18,19,57,83
+VCCST_CPU +VCCST_CPU 3,5,9,25,32
+VCCSTG +VCCSTG 3,5
+VCCIO +VCCIO 3,9,91
+VCCSA +VCCSA 80
+5VSUS +5VSUS 13,52,64,81
+12VSUS +12VSUS 28,81,91
+1.0VSUS +1.0VSUS 26,82
+1.0V +1.0V 57,91

+1.2V — JP0701 3MM_OPEN_5MIL — +VDDQ_CPU
JP0702 3MM_OPEN_5MIL

+VDDQ_CPU — R0701 0Ohm — +VDDQ_CPU_CLK

+1.2V — R0709 0Ohm — +VCCSFR_OC
Refer to CRB 0.53
141030 Merge Power PDDG0.91 Table5-1

+VDDQ_CPU
C0701 10UF/6.3V
C0702 10UF/6.3V
C0703 10UF/6.3V
C0704 10UF/6.3V
C0705 10UF/6.3V
C0706 10UF/6.3V
C0721 10UF/6.3V
C0722 10UF/6.3V
C0723 10UF/6.3V

C0701 - C0704 : Near by package
C0705 - C0710 : Underneath the package

+VDDQ_CPU
C0707 1UF/6.3V
C0708 1UF/6.3V
C0709 1UF/6.3V
C0710 1UF/6.3V

+1.0V — R0710 0Ohm — +VCCST_CPU
141127 65u sec full load ready

+1.0V — R0711 0Ohm — +VCCSFR

+VCCIO — R0713 0Ohm — +VCCSTG
141030 Merge Power PDDG0.91 Table5-1
141127 65u sec full load ready

+VDDQ_CPU
U0301N
CPU POWER 3 OF 4

AU23	VDDQ_1	VCCIO_1	AK28
AU28	VDDQ_2	VCCIO_2	AK30
AU35	VDDQ_3	VCCIO_3	AL30
AU42	VDDQ_4	VCCIO_4	AL42
BB23	VDDQ_5	VCCIO_5	AM28
BB32	VDDQ_6	VCCIO_6	AM30
BB41	VDDQ_7	VCCIO_7	AM42
BB47	VDDQ_8		
BB51	VDDQ_9		
AM40	VDDQC	VCCSA_1	AK23
A18	VCCST	VCCSA_2	AK25
A22	VCCSTG	VCCSA_3	G23
AL23	VCCPLL_OC	VCCSA_4	G25
K20	VccPLL_1	VCCSA_5	G27
K21	VccPLL_2	VCCSA_6	G28
		VCCSA_7	J22
		VCCSA_8	J23
		VCCSA_9	J27
		VCCSA_10	K23
		VCCSA_11	K25
		VCCSA_12	K27
		VCCSA_13	K28
		VCCSA_14	K30
		VCCIO_SENSE	AM23
		VSSIO_SENSE	AM22
		VSSSA_SENSE	H21
		VCCSA_SENSE	H20

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+VCCIO
C0717 1UF/6.3V
C0718 1UF/6.3V
C0719 1UF/6.3V
C0720 1UF/6.3V

+VCCSA

+VCCIO
R0714 1KOHM @
Reserved PH/PD
R0715 1KOHM @

VCCIO_VR_FB
VSSIO_VR_FB

VCCSA_VSSSENSE 80
R07021 1% 100Ohm
R07031 1% 100Ohm +VCCSA
VCCSA_VCCSENSE 80

Pull H/L near CPU side

+VDDQ_CPU_CLK
C0711 0.1UF/16V

+VCCST_CPU
C0712 1UF/6.3V

+VCCSTG
C0713 1UF/6.3V

+VCCSFR_OC
C0714 0.1UF/16V

+VCCSFR
C0715 0.1UF/16V
C0716 0.1UF/16V

Table 5-1. Power Rail Requirements — Volume Segment — U-Line

Load switch (LS)	LS ENABLE	Load/Rail name	Imax (A)
<= 65usec full load ready (Note 16)	SLP_S4#	Vcc_{ST}	0.04
		$Vcc_{PLL}(Vcc_{SFR})$	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VccIO	3.0
		Vcc_{STG}	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically Tcpu_04

reference 543977_543977_SKL_PDDG_Rev0_91

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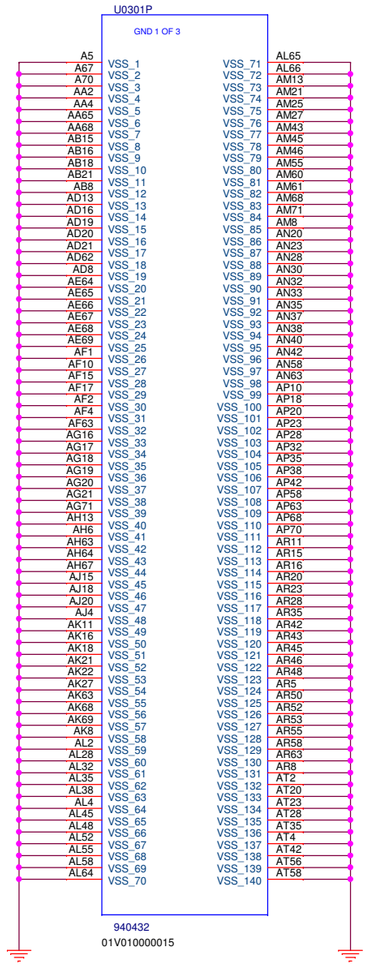
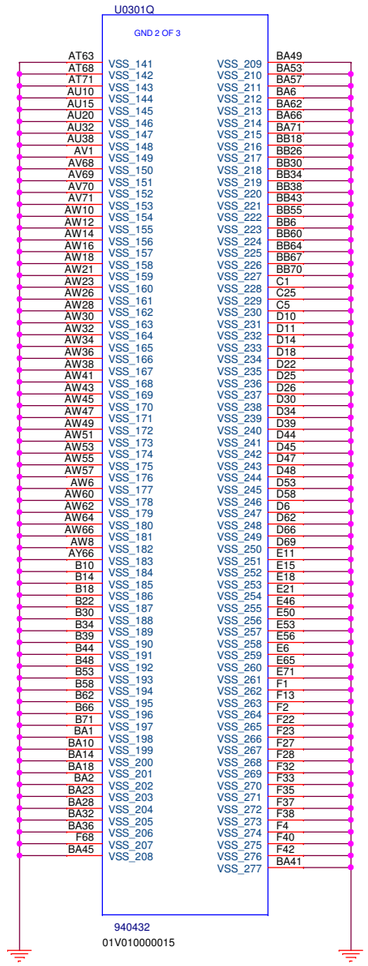
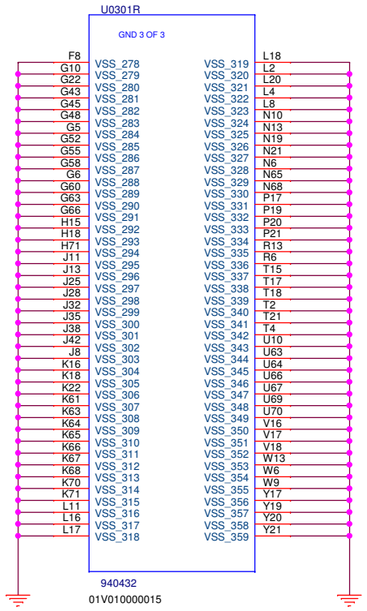
BG1-NB4
Title: CPU(5)_+VDDQ/IO/SA
Engineer: sinsian_Jheng
Size: C | Project Name: P5HCJ/Megatron | Rev: 1.2
Date: Friday, February 05, 2016 | Sheet 7 of 96

08

CPU(6)_CPU GND







PEGATRON

Title : CPU(6)_CPU GND

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BG1-NB4

Engineer: sinsian_Jheng

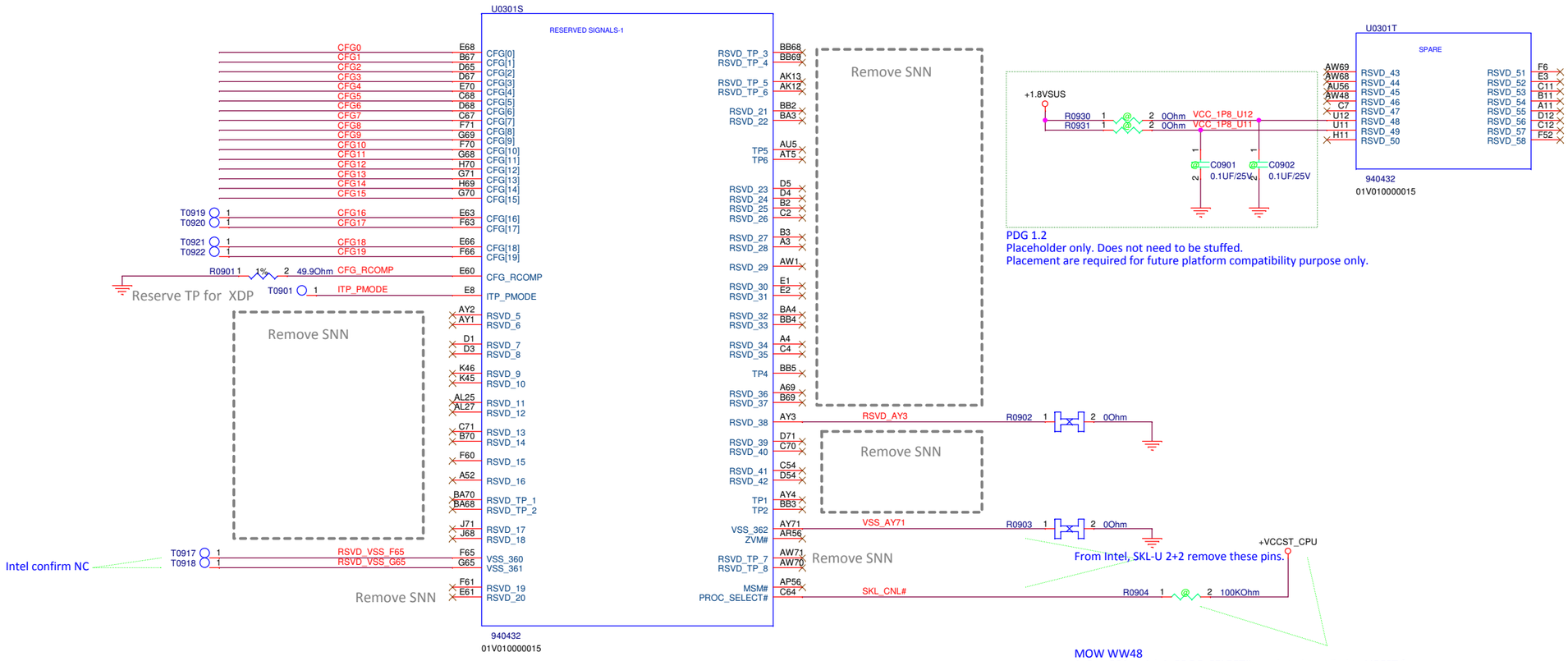
Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 8 of 96

09

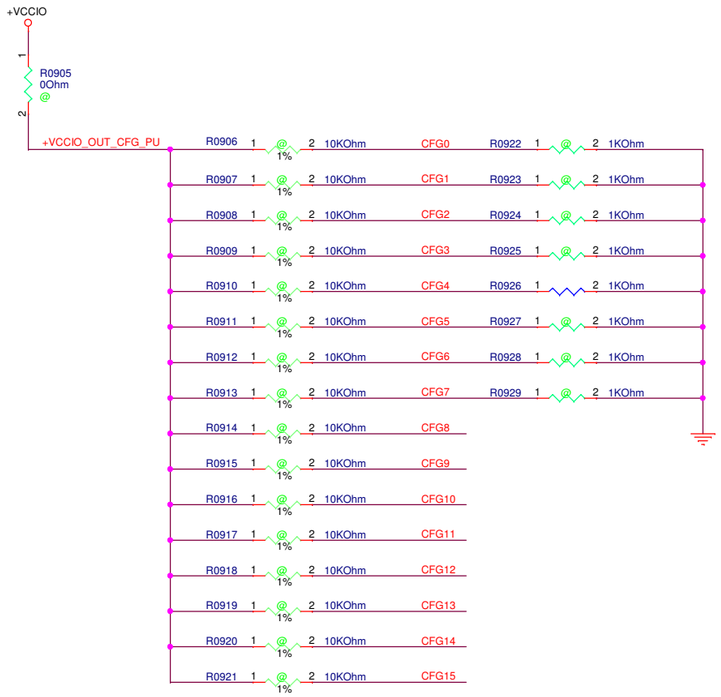
CPU(7)_CFG/RSVD

+VCCIO — +VCCIO 3,7,91
+VCCST_CPU — +VCCST_CPU 3,5,7,25,32
+1.8VSUS — +1.8VSUS 26,84



PDG 1.2
Placeholder only. Does not need to be stuffed.
Placement are required for future platform compatibility purpose only.

MOW WW48
1. Ball C64 which is PROC_SELECT# needs to be pulled to VCCST for Cannonlake support via 100K ohm resistor and with no resistor populated (floating pin) for Skylake.



6.4 Reset and Miscellaneous Signals

Table 6-8. Reset and Miscellaneous Signals

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I/O	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

13

Type_C_TPS25810

+5V_USB_I — +5V_USB_I 14

+5VSUS — +5VSUS 52,64,81

+5VBUS — R1305 10KOhm @ — EN

+5VBUS — R1306 10KOhm @ — CHG

+5VBUS — R1308 10KOhm @ — CHG_HI

R1304 10KOhm @

R1307 10KOhm @

R1309 10KOhm @

FAULTb pin is an open drain output that assert (active low) when device OUT current exceeds its programmed value and/or over temperature threshold is cressed.

23 USB_OC3#_PCH — R1326 0Ohm — FAULT#

+5VSUS — R1325 0Ohm — +5VBUS — 3.0A

R1301 0Ohm

C1301 10UF/6.3V

C1302 10UF/6.3V

C1304 10UF/6.3V

C1305 22UF/6.3V @

C1306 22UF/6.3V @

C1307 22UF/6.3V @

U1301 TPS25810RVC 06V500000016

LD_DET# UFP# POL# AUDIO#

GND2 DETb LD_DET# UFPb POLb AUDIOb

FAULTb IN1_1 IN1_2 IN2 AUX EN

DEBUGb OUT2 OUT1 CC2 GND1 CC1

DEBUG# — +5V_USB_I

SLG_CC2 14

SLG_CC1 14

+5V_USB_I — C1303 10UF/6.3V

CHG CHG_HI GND REF

30 TypeC_charge_EN — TypeC_charge_EN R1316 0Ohm

30 CHG_R — R1327 0Ohm

30 CHG_HI_R — R1328 0Ohm

R1302 100KOhm 1%

2016.02.03
R1.2
Support Type C charger function control by EC
Function request by 2016 customer BIOS spec

EMI 2015/10/19

+5VSUS — C1308 0.1UF/25V @

+5VBUS

R1310 10KOhm @ FAULT#

R1311 10KOhm LD_DET#

R1312 10KOhm UFP#

R1313 10KOhm POL#

R1314 10KOhm AUDIO#

R1315 10KOhm DEBUG#

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Type_C_TPS25810

BG1-NB4

Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 13 of 96

14

Type C CONN

+5V_USB_I 13 → +5V_USB_I

23 USB3_RXP3 → RNX1401B 0Ohm → USB3_RXP3_CON
23 USB3_RXN3 → RNX1401A 0Ohm → USB3_RXN3_CON
23 USB3_TXP3 → C1407 0.1UF/16V → USB3_TXP3_C → RNX1402A 0Ohm → USB3_TXP3_CON
23 USB3_TXN3 → C1408 0.1UF/16V → USB3_TXN3_C → RNX1402B 0Ohm → USB3_TXN3_CON
L1402 90Ohm 09V090000023
L1403 90Ohm 09V090000023

23 USB3_RXP4 → RNX1403B 0Ohm → USB3_RXP4_CON
23 USB3_RXN4 → RNX1403A 0Ohm → USB3_RXN4_CON
23 USB3_TXP4 → C1409 0.1UF/16V → USB3_TXP4_C → RNX1404A 0Ohm → USB3_TXP4_CON
23 USB3_TXN4 → C1410 0.1UF/16V → USB3_TXN4_C → RNX1404B 0Ohm → USB3_TXN4_CON
L1404 90Ohm 09V090000023
L1405 90Ohm 09V090000023

23 USB_PP3_PD → RNX1405A 0Ohm → C_USB2_PP3_CON
23 USB_PN3_PD → RNX1405B 0Ohm → C_USB2_PN3_CON
L1406 90Ohm/100MHz 09V090000001

USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

CON1401
USB_24P_12HD_LOTE
13 SLG_CC1 → A5 CC1
SLG_CC2 13 ← B5 CC2
USB3_TXP3_CON, USB3_TXN3_CON, +5V_USB_I, C_USB2_PP3_CON, C_USB2_PN3_CON, +5V_USB_I, USB3_RXN4_CON, USB3_RXP4_CON
USB3_RXP3_CON, USB3_RXN3_CON, +5V_USB_I, C_USB2_PN3_CON, +5V_USB_I, USB3_TXN4_CON, USB3_TXP4_CON

EMI 2015/10/08

U1404 PUSB3F96 07V220000032
USB3_TXN3_CON, USB3_TXP3_CON, USB3_RXP3_CON, USB3_RXN3_CON → USB3_TXN3_CON, USB3_TXP3_CON, USB3_RXP3_CON, USB3_RXN3_CON

U1405 PUSB3F96 07V220000032
USB3_TXN4_CON, USB3_TXP4_CON, USB3_RXP4_CON, USB3_RXN4_CON → USB3_TXN4_CON, USB3_TXP4_CON, USB3_RXP4_CON, USB3_RXN4_CON

C_USB2_PP3_CON, C_USB2_PN3_CON, SLG_CC1, SLG_CC2
D1402 AZ5425-01F 07V180000016
D1403 AZ5425-01F 07V180000016
D1406 AZ5725-01F /EMI 07V180000029
D1407 AZ5725-01F /EMI 07V180000029
+5V_USB_I → D1401 AZ5725-01F

2015.12.04
R1.1
EMI B build confirm

+5V_USB_I
C1401 22UF/6.3V, C1402 22UF/6.3V, C1403 22UF/6.3V, C1404 22UF/6.3V, C1405 22UF/6.3V, C1406 0.1UF/16V

2015.11.27
R1.1
採購建議用料 22UF/6.3V 0603

PEGATRON Title : Type C CONN
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

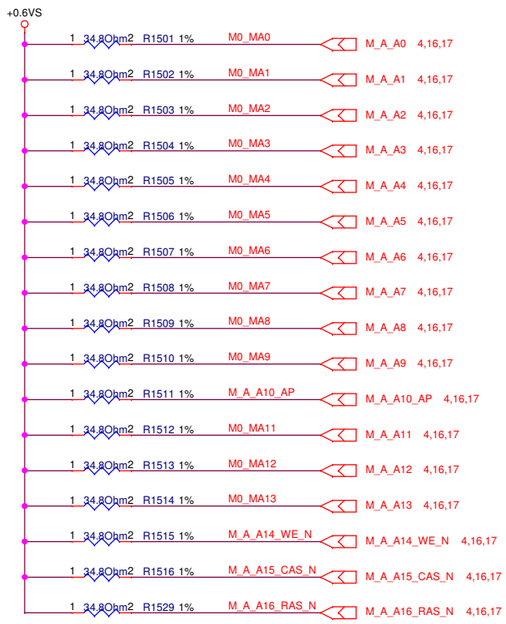
Date: Friday, February 05, 2016 Sheet 14 of 96

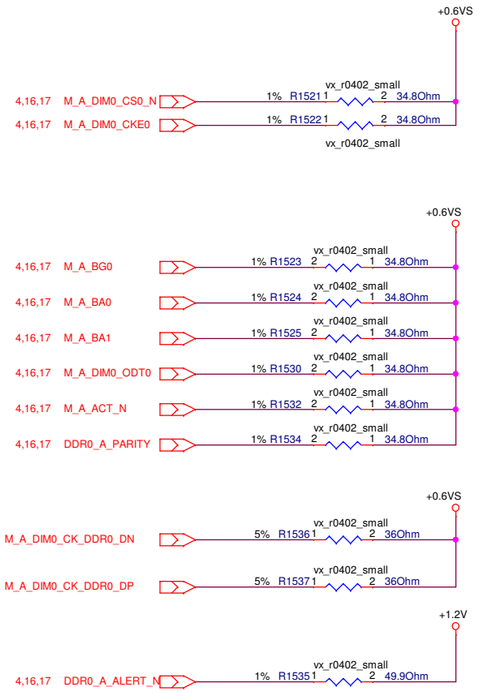
15

DDR4(0)_Termination

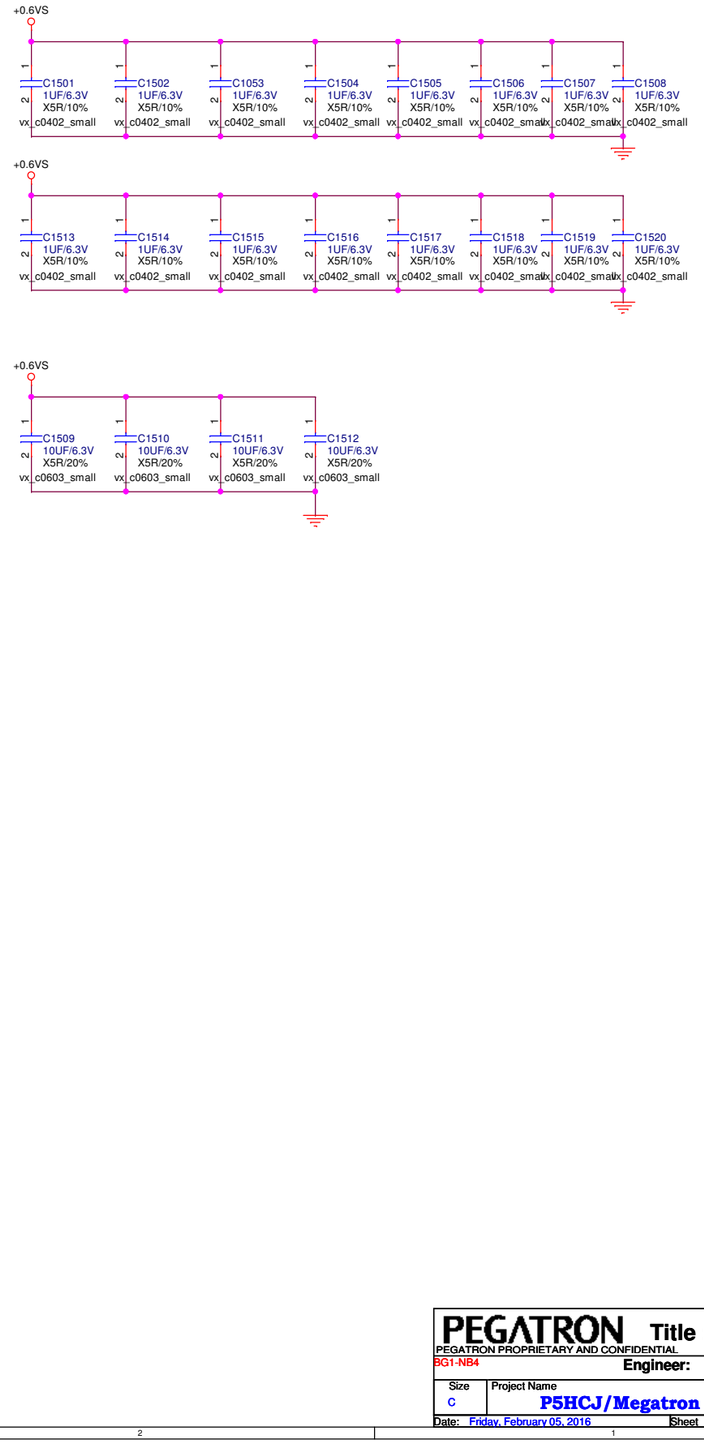
+0.6VS +0.6VS 18,57,83

+1.2V +1.2V 3,4,7,16,17,18,19,57,83





Average placed close to +VDDQ_VTT power plane



PEGATRON Title : DDR4(0)_Termination

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4 Engineer:

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 15 of 96

16

DDR4(1)_CH0

M_A_D[0:31] 4

+1.2V +1.2V 3,4,7,15,17,18,19,57,83

+V_DDR_VREFCA_CHA_DIMM +V_DDR_VREFCA_CHA_DIMM 17,19

+2.5V +2.5V 17,18,57,82

U1601

DDR4

256M x 16 (4Gbit)

4,15,17	M_A_A0	P3	A0	VDD_1	B3	+1.2V
4,15,17	M_A_A1	P7	A1	VDD_2	B9	
4,15,17	M_A_A2	R3	A2	VDD_3	D1	
4,15,17	M_A_A3	N7	A3	VDD_4	G7	
4,15,17	M_A_A4	N3	A4	VDD_5	J1	
4,15,17	M_A_A5	P8	A5	VDD_6	J9	
4,15,17	M_A_A6	P2	A6	VDD_7	L1	
4,15,17	M_A_A7	R8	A7	VDD_8	L9	
4,15,17	M_A_A8	R2	A8	VDD_9	R1	
4,15,17	M_A_A9	R7	A9	VDD_10	T9	
4,15,17	M_A_A10_AP	M3	A10/AP			
4,15,17	M_A_A11	T2	A11	VDDQ_1	A1	
4,15,17	M_A_A12	M7	A12/BC_n	VDDQ_2	A9	
4,15,17	M_A_A13	T8	A13	VDDQ_3	C1	
4,15,17	M_A_A14_WE_N	L2	WE_n/A14	VDDQ_4	D9	
4,15,17	M_A_A15_CAS_N	M8	CAS_n/A15	VDDQ_5	F2	
4,15,17	M_A_A16_RAS_N	L8	RAS_n/A16	VDDQ_6	F8	
4,15,17	M_A_ACT_N	L3	ACT_n	VDDQ_7	G1	
				VDDQ_8	G9	
4,15,17	M_A_BA0	N2	BA0	VDDQ_9	J2	
4,15,17	M_A_BA1	N8	BA1	VDDQ_10	J8	
4,15,17	M_A_BG0	M2	BG0			+2.5V
4,15,17	DDR0_A_PARITY	T3	PAR	VPP_1	B1	
4,15,17	M_A_DIM0_CS0_N	L7	CS_n	VPP_2	R9	
4,15,17	M_A_DIM0_ODT0	K3	ODT	VREFCA	M1	+V_DDR_VREFCA_CHA_DIMM
4,15,17	M_A_DIM0_CKE0	K2	CKE			
4,15,17	M_A_DIM0_CK_DDR0_DP	K7	CK_t	ZQ	F9	DDR3L_ZQ_01
4,15,17	M_A_DIM0_CK_DDR0_DN	K8	CK_c	TEN	N9	
4,15,17	DDR0_A_ALERT_N	P9	ALERT_n			
	M_A_D4	G2	DQL0	NC	T7	
	M_A_D6	F7	DQL1			
	M_A_D0	H3	DQL2			
	M_A_D7	H7	DQL3			
	M_A_D5	H2	DQL4			
	M_A_D2	H8	DQL5			
	M_A_D1	J3	DQL6			
	M_A_D3	J7	DQL7			
+1.2V		E7	DML_N/DBIL_N			
4	M_A_DQS_DP0	G3	DQSL_t			
4	M_A_DQS_DN0	F3	DQSL_c			
	M_A_D9	A3	DQU0	VSS_1	B2	
	M_A_D15	B8	DQU1	VSS_2	E1	
	M_A_D12	C3	DQU2	VSS_3	E9	
	M_A_D10	C7	DQU3	VSS_4	G8	
	M_A_D8	C2	DQU4	VSS_5	K1	
	M_A_D11	C8	DQU5	VSS_6	K9	
	M_A_D13	D3	DQU6	VSS_7	M9	
	M_A_D14	D7	DQU7	VSS_8	N1	
				VSS_9	T1	
+1.2V		E2	DMU_N/DBIU_N	VSSQ_1	A2	
4	M_A_DQS_DP1	B7	DQSU_t	VSSQ_2	A8	
4	M_A_DQS_DN1	A7	DQSU_c	VSSQ_3	C9	
				VSSQ_4	D2	
				VSSQ_5	D8	
				VSSQ_6	E3	
				VSSQ_7	E8	
				VSSQ_8	F1	
				VSSQ_9	H1	
4,17,18	DDR4_DRAMRST_R_N	P1	RESET_n	VSSQ_10	H9	

C1605 0.1UF/25V @

C1647 0.047UF/16V

R1602 240Ohm RES 240 OHM 1/16W (0402) 1%

K4A8G165WB-BCPB

03V150000088

U1602

DDR4

256M x 16 (4Gbit)

	M_A_A0	P3	A0	VDD_1	B3	+1.2V
	M_A_A1	P7	A1	VDD_2	B9	
	M_A_A2	R3	A2	VDD_3	D1	
	M_A_A3	N7	A3	VDD_4	G7	
	M_A_A4	N3	A4	VDD_5	J1	
	M_A_A5	P8	A5	VDD_6	J9	
	M_A_A6	P2	A6	VDD_7	L1	
	M_A_A7	R8	A7	VDD_8	L9	
	M_A_A8	R2	A8	VDD_9	R1	
	M_A_A9	R7	A9	VDD_10	T9	
	M_A_A10_AP	M3	A10/AP			
	M_A_A11	T2	A11	VDDQ_1	A1	
	M_A_A12	M7	A12/BC_n	VDDQ_2	A9	
	M_A_A13	T8	A13	VDDQ_3	C1	
	M_A_A14_WE_N	L2	WE_n/A14	VDDQ_4	D9	
	M_A_A15_CAS_N	M8	CAS_n/A15	VDDQ_5	F2	
	M_A_A16_RAS_N	L8	RAS_n/A16	VDDQ_6	F8	
	M_A_ACT_N	L3	ACT_n	VDDQ_7	G1	
				VDDQ_8	G9	
	M_A_BA0	N2	BA0	VDDQ_9	J2	
	M_A_BA1	N8	BA1	VDDQ_10	J8	
	M_A_BG0	M2	BG0			+2.5V
	DDR0_A_PARITY	T3	PAR	VPP_1	B1	
	M_A_DIM0_CS0_N	L7	CS_n	VPP_2	R9	
	M_A_DIM0_ODT0	K3	ODT	VREFCA	M1	+V_DDR_VREFCA_CHA_DIMM
	M_A_DIM0_CKE0	K2	CKE			
	M_A_DIM0_CK_DDR0_DP	K7	CK_t	ZQ	F9	DDR3L_ZQ_23
	M_A_DIM0_CK_DDR0_DN	K8	CK_c	TEN	N9	
	DDR0_A_ALERT_N	P9	ALERT_n			
	M_A_D16	G2	DQL0	NC	T7	
	M_A_D22	F7	DQL1			
	M_A_D20	H3	DQL2			
	M_A_D23	H7	DQL3			
	M_A_D17	H2	DQL4			
	M_A_D18	H8	DQL5			
	M_A_D21	J3	DQL6			
	M_A_D19	J7	DQL7			
+1.2V		E7	DML_N/DBIL_N			
4	M_A_DQS_DP2	G3	DQSL_t			
4	M_A_DQS_DN2	F3	DQSL_c			
	M_A_D28	A3	DQU0	VSS_1	B2	
	M_A_D27	B8	DQU1	VSS_2	E1	
	M_A_D29	C3	DQU2	VSS_3	E9	
	M_A_D26	C7	DQU3	VSS_4	G8	
	M_A_D25	C2	DQU4	VSS_5	K1	
	M_A_D31	C8	DQU5	VSS_6	K9	
	M_A_D24	D3	DQU6	VSS_7	M9	
	M_A_D30	D7	DQU7	VSS_8	N1	
				VSS_9	T1	
+1.2V		E2	DMU_N/DBIU_N	VSSQ_1	A2	
4	M_A_DQS_DP3	B7	DQSU_t	VSSQ_2	A8	
4	M_A_DQS_DN3	A7	DQSU_c	VSSQ_3	C9	
				VSSQ_4	D2	
				VSSQ_5	D8	
				VSSQ_6	E3	
				VSSQ_7	E8	
				VSSQ_8	F1	
				VSSQ_9	H1	
	DDR4_DRAMRST_R_N	P1	RESET_n	VSSQ_10	H9	

C1604 0.1UF/25V @

C1648 0.047UF/16V

R1603 240Ohm RES 240 OHM 1/16W (0402) 1%

K4A8G165WB-BCPB

03V150000088

2016.02.02
R1.2
Change 240 Ohm from 0201 to 0402

+1.2V

C1607 10UF/6.3V

C1608 10UF/6.3V

C1623 10UF/6.3V

+1.2V

C1611 1UF/6.3V

C1612 1UF/6.3V

C1613 1UF/6.3V

C1614 1UF/6.3V

C1615 1UF/6.3V

C1616 1UF/6.3V

C1624 1UF/6.3V

C1625 1UF/6.3V

+2.5V

C1626 10UF/6.3V

C1627 1UF/6.3V

C1628 1UF/6.3V

C1629 1UF/6.3V

C1630 1UF/6.3V

+1.2V

C1631 10UF/6.3V

C1632 10UF/6.3V

C1633 10UF/6.3V

+1.2V

C1634 1UF/6.3V

C1635 1UF/6.3V

C1636 1UF/6.3V

C1637 1UF/6.3V

C1638 1UF/6.3V

C1639 1UF/6.3V

C1640 1UF/6.3V

C1641 1UF/6.3V

+2.5V

C1642 10UF/6.3V

C1649 10UF/6.3V @

C1643 1UF/6.3V

C1644 1UF/6.3V

C1645 1UF/6.3V

C1646 1UF/6.3V

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4

Title : DDR4(1)_CH0

Engineer:

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 16 of 96

17

DDR4(2)_CH0

M_A_D[32:63] 4

+V_DDR_VREFCA_CHA_DIMM +V_DDR_VREFCA_CHA_DIMM 16,19
+1.2V +1.2V 3,4,7,15,16,18,19,57,83
+2.5V +2.5V 16,18,57,82

U1701 DDR4 256M x 16 (4Gbit)

4,15,16	M_A_A0	P3	A0	VDD_1	B3
4,15,16	M_A_A1	P7	A1	VDD_2	B9
4,15,16	M_A_A2	R3	A2	VDD_3	D1
4,15,16	M_A_A3	N7	A3	VDD_4	G7
4,15,16	M_A_A4	N3	A4	VDD_5	J1
4,15,16	M_A_A5	P8	A5	VDD_6	J9
4,15,16	M_A_A6	P2	A6	VDD_7	L1
4,15,16	M_A_A7	R8	A7	VDD_8	L9
4,15,16	M_A_A8	R2	A8	VDD_9	R1
4,15,16	M_A_A9	R7	A9	VDD_10	T9
4,15,16	M_A_A10_AP	M3	A10/AP		
4,15,16	M_A_A11	T2	A11	VDDQ_1	A1
4,15,16	M_A_A12	M7	A12/BC_n	VDDQ_2	A9
4,15,16	M_A_A13	T8	A13	VDDQ_3	C1
4,15,16	M_A_A14_WE_N	L2	WE_n/A14	VDDQ_4	D9
4,15,16	M_A_A15_CAS_N	M8	CAS_n/A15	VDDQ_5	F2
4,15,16	M_A_A16_RAS_N	L8	RAS_n/A16	VDDQ_6	F8
4,15,16	M_A_ACT_N	L3	ACT_n	VDDQ_7	G1
				VDDQ_8	G9
	M_A_BA0	N2	BA0	VDDQ_9	J2
4,15,16	M_A_BA1	N8	BA1	VDDQ_10	J8
4,15,16	M_A_BG0	M2	BG0		
				VPP_1	B1
4,15,16	DDR0_A_PARITY	T3	PAR	VPP_2	R9
4,15,16	M_A_DIM0_CS0_N	L7	CS_n		
4,15,16	M_A_DIM0_ODT0	K3	ODT	VREFCA	M1
4,15,16	M_A_DIM0_CKE0	K2	CKE		
4,15,16	M_A_DIM0_CK_DDR0_DP	K7	CK_t		
4,15,16	M_A_DIM0_CK_DDR0_DN	K8	CK_c	ZQ	F9
4,15,16	DDR0_A_ALERT_N	P9	ALERT_n	TEN	N9
	M_A_D53	G2	DQL0		
	M_A_D51	F7	DQL1		
	M_A_D52	H3	DQL2		
	M_A_D55	H7	DQL3		
	M_A_D48	H2	DQL4		
	M_A_D54	H8	DQL5		
	M_A_D49	J3	DQL6		
	M_A_D50	J7	DQL7	NC	T7
		E7	DML_N/DBIL_N		
4	M_A_DQS_DP6	G3	DQSL_t		
4	M_A_DQS_DN6	F3	DQSL_c		
				VSS_1	B2
				VSS_2	E1
				VSS_3	E9
	M_A_D57	A3	DQU0	VSS_4	G8
	M_A_D58	B8	DQU1	VSS_5	K1
	M_A_D60	C3	DQU2	VSS_6	K9
	M_A_D63	C7	DQU3	VSS_7	M9
	M_A_D61	C2	DQU4	VSS_8	N1
	M_A_D59	C8	DQU5	VSS_9	T1
	M_A_D56	D3	DQU6		
	M_A_D62	D7	DQU7	VSSQ_1	A2
				VSSQ_2	A8
		E2	DMU_N/DBIU_N	VSSQ_3	C9
				VSSQ_4	D2
4	M_A_DQS_DP7	B7	DQSU_t	VSSQ_5	D8
4	M_A_DQS_DN7	A7	DQSU_c	VSSQ_6	E3
				VSSQ_7	E8
				VSSQ_8	F1
				VSSQ_9	H1
4,16,18	DDR4_DRAMRST_R_N	P1	RESET_n	VSSQ_10	H9

K4A8G165WB-BCPB
03V150000088

+1.2V
+2.5V
+V_DDR_VREFCA_CHA_DIMM
C1739 0.047UF/16V
R1701 240Ohm
C1705 0.1UF/25V @

U1702 DDR4 256M x 16 (4Gbit)

	M_A_A0	P3	A0	VDD_1	B3
	M_A_A1	P7	A1	VDD_2	B9
	M_A_A2	R3	A2	VDD_3	D1
	M_A_A3	N7	A3	VDD_4	G7
	M_A_A4	N3	A4	VDD_5	J1
	M_A_A5	P8	A5	VDD_6	J9
	M_A_A6	P2	A6	VDD_7	L1
	M_A_A7	R8	A7	VDD_8	L9
	M_A_A8	R2	A8	VDD_9	R1
	M_A_A9	R7	A9	VDD_10	T9
	M_A_A10_AP	M3	A10/AP		
	M_A_A11	T2	A11	VDDQ_1	A1
	M_A_A12	M7	A12/BC_n	VDDQ_2	A9
	M_A_A13	T8	A13	VDDQ_3	C1
	M_A_A14_WE_N	L2	WE_n/A14	VDDQ_4	D9
	M_A_A15_CAS_N	M8	CAS_n/A15	VDDQ_5	F2
	M_A_A16_RAS_N	L8	RAS_n/A16	VDDQ_6	F8
	M_A_ACT_N	L3	ACT_n	VDDQ_7	G1
				VDDQ_8	G9
	M_A_BA0	N2	BA0	VDDQ_9	J2
	M_A_BA1	N8	BA1	VDDQ_10	J8
	M_A_BG0	M2	BG0		
				VPP_1	B1
	DDR0_A_PARITY	T3	PAR	VPP_2	R9
	M_A_DIM0_CS0_N	L7	CS_n		
	M_A_DIM0_ODT0	K3	ODT	VREFCA	M1
	M_A_DIM0_CKE0	K2	CKE		
	M_A_DIM0_CK_DDR0_DP	K7	CK_t		
	M_A_DIM0_CK_DDR0_DN	K8	CK_c	ZQ	F9
	DDR0_A_ALERT_N	P9	ALERT_n	TEN	N9
	M_A_D44	G2	DQL0		
	M_A_D47	F7	DQL1		
	M_A_D41	H3	DQL2		
	M_A_D46	H7	DQL3		
	M_A_D40	H2	DQL4		
	M_A_D42	H8	DQL5		
	M_A_D45	J3	DQL6		
	M_A_D43	J7	DQL7	NC	T7
		E7	DML_N/DBIL_N		
4	M_A_DQS_DP5	G3	DQSL_t		
4	M_A_DQS_DN5	F3	DQSL_c		
				VSS_1	B2
				VSS_2	E1
				VSS_3	E9
	M_A_D34	A3	DQU0	VSS_4	G8
	M_A_D33	B8	DQU1	VSS_5	K1
	M_A_D37	C3	DQU2	VSS_6	K9
	M_A_D38	C7	DQU3	VSS_7	M9
	M_A_D32	C2	DQU4	VSS_8	N1
	M_A_D39	C8	DQU5	VSS_9	T1
	M_A_D36	D3	DQU6		
	M_A_D35	D7	DQU7	VSSQ_1	A2
				VSSQ_2	A8
		E2	DMU_N/DBIU_N	VSSQ_3	C9
				VSSQ_4	D2
4	M_A_DQS_DP4	B7	DQSU_t	VSSQ_5	D8
4	M_A_DQS_DN4	A7	DQSU_c	VSSQ_6	E3
				VSSQ_7	E8
				VSSQ_8	F1
				VSSQ_9	H1
	DDR4_DRAMRST_R_N	P1	RESET_n	VSSQ_10	H9

K4A8G165WB-BCPB
03V150000088

+1.2V
+2.5V
+V_DDR_VREFCA_CHA_DIMM
C1740 0.047UF/16V
R1702 240Ohm RES 240 OHM 1/16W (0402) 1%

2016.02.02
R1.2
Change 240 Ohm from 0201 to 0402

C1706 0.1UF/25V @

+1.2V
C1707 10UF/6.3V
C1708 10UF/6.3V
C1727 10UF/6.3V

+1.2V
C1711 1UF/6.3V
C1712 1UF/6.3V
C1713 1UF/6.3V
C1714 1UF/6.3V
C1715 1UF/6.3V
C1716 1UF/6.3V
C1723 1UF/6.3V
C1724 1UF/6.3V

+2.5V
C1729 10UF/6.3V
C1730 10UF/6.3V
C1731 1UF/6.3V
C1732 1UF/6.3V
C1733 1UF/6.3V

+1.2V
C1709 10UF/6.3V
C1710 10UF/6.3V
C1728 10UF/6.3V

+1.2V
C1717 1UF/6.3V
C1718 1UF/6.3V
C1719 0.1UF/25V
C1720 0.1UF/25V
C1721 0.1UF/25V
C1722 0.1UF/25V
C1725 1UF/6.3V
C1726 1UF/6.3V

+2.5V
C1734 10UF/6.3V
C1735 1UF/6.3V
C1736 1UF/6.3V
C1737 1UF/6.3V
C1738 1UF/6.3V

PEGATRON Title : DDR4(2)_CH0
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer:

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 17 of 96

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DDR4(2)_SODIMM

+1.2V +1.2V 3,4,7,15,16,17,19,57,83
+0.6VS +0.6VS 15,57,83
+3VS +3VS 3,4,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+2.5V +2.5V 16,17,57,82

12V02GBSM007
DDR4_SO_260P

19 +V_DDR_VREFCA_CHB_DIMM
+V_DDR_VREFCA_CHB_DIMM 164 VREFCA
C1856 2.2UF/10V @
C1857 0.1UF/16V

28 SMB_CLK_S
28 SMB_DAT_S
SMB_CLK_S 253 SCL
SMB_DAT_S 254 SDA

+3VS
C1851 2.2UF/6.3V
C1853 0.1UF/25V

SA0 256 SA0
SA1 260 SA1
SA2 166 SA2
255 VDDSPD

+1.2V
R1809 240Ohm

4 M_B_ACT_N
4 DDR1_B_ALERT_N
M_B_ACT_N 114 ACT_n
DDR1_B_ALERT_N 116 ALERT_n
134 EVENT_n/NF

4,16,17 DDR4_DRAMRST_R_N
DDR4_DRAMRST_R_N 108 RESET_n
4 DDR1_B_PARITY
DDR1_B_PARITY 143 PARITY
C1872 0.1UF/25V @

M_B_CB0 92 CB0/NC
M_B_CB1 91 CB1/NC
M_B_CB2 101 CB2/NC
M_B_CB3 105 CB3/NC
M_B_CB4 88 CB4/NC
M_B_CB5 87 CB5/NC
M_B_CB6 100 CB6/NC
M_B_CB7 104 CB7/NC

4 M_B_DIM0_ODT0
4 M_B_DIM0_ODT1
M_B_DIM0_ODT0 155 ODT0
M_B_DIM0_ODT1 161 ODT1

4 M_B_DIM0_CKE0
4 M_B_DIM0_CKE1
M_B_DIM0_CKE0 109 CKE0
M_B_DIM0_CKE1 110 CKE1

4 M_B_DIM0_CS0_N
4 M_B_DIM0_CS1_N
M_B_DIM0_CS0_N 149 CS0_n
M_B_DIM0_CS1_N 157 CS1_n
162 C0/CS2_n/NC
165 C1/CS3_n/NC

4 M_B_DIM0_CK_DDR0_DN
4 M_B_DIM0_CK_DDR0_DP
4 M_B_DIM0_CK_DDR1_DN
4 M_B_DIM0_CK_DDR1_DP
M_B_DIM0_CK_DDR0_DN 139 CK0_c
M_B_DIM0_CK_DDR0_DP 137 CK0_t
M_B_DIM0_CK_DDR1_DN 140 CK1_c/NF
M_B_DIM0_CK_DDR1_DP 138 CK1_t/NF

4 M_B_BG0
4 M_B_BG1
M_B_BG0 115 BG0
M_B_BG1 113 BG1

4 M_B_BA0
4 M_B_BA1
M_B_BA0 150 BA0
M_B_BA1 145 BA1

4 M_B_A0
4 M_B_A1
4 M_B_A2
4 M_B_A3
4 M_B_A4
4 M_B_A5
4 M_B_A6
4 M_B_A7
4 M_B_A8
4 M_B_A9
4 M_B_A10_AP
4 M_B_A11
4 M_B_A12
4 M_B_A13
4 M_B_A14_WE_N
4 M_B_A15_CAS_N
4 M_B_A16_RAS_N
M_B_A0 144 A0
M_B_A1 133 A1
M_B_A2 132 A2
M_B_A3 131 A3
M_B_A4 128 A4
M_B_A5 126 A5
M_B_A6 127 A6
M_B_A7 122 A7
M_B_A8 125 A8
M_B_A9 121 A9
M_B_A10_AP 146 A10/AP
M_B_A11 120 A11
M_B_A12 119 A12
M_B_A13 158 A13
M_B_A14_WE_N 151 WE_n/A14
M_B_A15_CAS_N 156 CAS_n/A15
M_B_A16_RAS_N 152 RAS_n/A16

DQS0_c 11 M_B_DQS_DN1
DQS0_t 13 M_B_DQS_DP1
DQS1_c 32 M_B_DQS_DN0
DQS1_t 34 M_B_DQS_DP0
DQS2_c 53 M_B_DQS_DN2
DQS2_t 55 M_B_DQS_DP2
DQS3_c 74 M_B_DQS_DN3
DQS3_t 76 M_B_DQS_DP3
DQS4_c 177 M_B_DQS_DN4
DQS4_t 179 M_B_DQS_DP4
DQS5_c 198 M_B_DQS_DN5
DQS5_t 200 M_B_DQS_DP5
DQS6_c 219 M_B_DQS_DN6
DQS6_t 221 M_B_DQS_DP6
DQS7_c 240 M_B_DQS_DN7
DQS7_t 242 M_B_DQS_DP7
DQS8_c 95
DQS8_t 97

M_B_DQS_DN1 4
M_B_DQS_DP1 4
M_B_DQS_DN0 4
M_B_DQS_DP0 4
M_B_DQS_DN2 4
M_B_DQS_DP2 4
M_B_DQS_DN3 4
M_B_DQS_DP3 4
M_B_DQS_DN4 4
M_B_DQS_DP4 4
M_B_DQS_DN5 4
M_B_DQS_DP5 4
M_B_DQS_DN6 4
M_B_DQS_DP6 4
M_B_DQS_DN7 4
M_B_DQS_DP7 4

+1.2V
R1807 240Ohm
R1808 240Ohm

DM0_n/DBI0_n 12
DM1_n/DBI_n 33
DM2_n/DBI2_n 54
DM3_n/DBI3_n 75
DM4_n/DBI4_n 178
DM5_n/DBI5_n 199
DM6_n/DBI6_n 220
DM7_n/DBI7_n 241
DM8_n/DBI_n/NC 96

M_B_DQ[63:0] 4

DQ0 8 M_B_DQ13
DQ1 7 M_B_DQ12
DQ2 20 M_B_DQ15
DQ3 21 M_B_DQ11
DQ4 4 M_B_DQ9
DQ5 3 M_B_DQ8
DQ6 16 M_B_DQ14
DQ7 17 M_B_DQ10
DQ8 28 M_B_DQ5
DQ9 29 M_B_DQ0
DQ10 41 M_B_DQ2
DQ11 42 M_B_DQ6
DQ12 24 M_B_DQ1
DQ13 25 M_B_DQ4
DQ14 38 M_B_DQ3
DQ15 37 M_B_DQ7
DQ16 50 M_B_DQ21
DQ17 49 M_B_DQ19
DQ18 62 M_B_DQ16
DQ19 63 M_B_DQ22
DQ20 46 M_B_DQ18
DQ21 45 M_B_DQ20
DQ22 58 M_B_DQ23
DQ23 59 M_B_DQ17
DQ24 70 M_B_DQ28
DQ25 71 M_B_DQ25
DQ26 83 M_B_DQ31
DQ27 84 M_B_DQ26
DQ28 66 M_B_DQ29
DQ29 67 M_B_DQ24
DQ30 79 M_B_DQ30
DQ31 80 M_B_DQ27
DQ32 174 M_B_DQ36
DQ33 173 M_B_DQ33
DQ34 187 M_B_DQ35
DQ35 186 M_B_DQ39
DQ36 170 M_B_DQ37
DQ37 169 M_B_DQ32
DQ38 183 M_B_DQ34
DQ39 182 M_B_DQ38
DQ40 195 M_B_DQ44
DQ41 194 M_B_DQ41
DQ42 207 M_B_DQ46
DQ43 208 M_B_DQ43
DQ44 191 M_B_DQ45
DQ45 190 M_B_DQ40
DQ46 203 M_B_DQ47
DQ47 204 M_B_DQ42
DQ48 216 M_B_DQ52
DQ49 215 M_B_DQ48
DQ50 228 M_B_DQ50
DQ51 229 M_B_DQ54
DQ52 211 M_B_DQ49
DQ53 212 M_B_DQ53
DQ54 224 M_B_DQ51
DQ55 225 M_B_DQ55
DQ56 237 M_B_DQ60
DQ57 236 M_B_DQ56
DQ58 249 M_B_DQ62
DQ59 250 M_B_DQ59
DQ60 232 M_B_DQ57
DQ61 233 M_B_DQ61
DQ62 245 M_B_DQ63
DQ63 246 M_B_DQ58

Byte_1
Byte_0
Byte_2
Byte_3
Byte_4
Byte_5
Byte_6
Byte_7

0 1 2 3 4 5 6 7

CON1801A

+1.2V
CON1801B
DDR4_SO_260P
12V02GBSM007

VDD1 111
VDD2 112
VDD3 117
VDD4 118
VDD5 123
VDD6 124
VDD7 129
VDD8 130
VDD9 135
VDD10 136
VDD11 141
VDD12 142
VDD13 147
VDD14 148
VDD15 153
VDD16 154
VDD17 159
VDD18 160
VDD19 163

+0.6VS
VTT 258
+2.5V
VPP2 259
VPP1 257

VSS1 1
VSS2 2
VSS3 5
VSS4 6
VSS5 9
VSS6 10
VSS7 14
VSS8 15
VSS9 18
VSS10 19
VSS11 22
VSS12 23
VSS13 26
VSS14 27
VSS15 30
VSS16 31
VSS17 35
VSS18 36
VSS19 39
VSS20 40
VSS21 43
VSS22 44
VSS23 47
VSS24 48
VSS25 51
VSS26 52
VSS27 56
VSS28 57
VSS29 60
VSS30 61
VSS31 64
VSS32 65
VSS33 68
VSS34 69
VSS35 72
VSS36 73
VSS37 77
VSS38 78
VSS39 82
VSS40 85
VSS41 86
VSS42 89
VSS43 90
VSS44 93
VSS45 94
VSS46 98
VSS47

VSS48 99
VSS49 102
VSS50 103
VSS51 106
VSS52 107
VSS53 167
VSS54 168
VSS55 171
VSS56 172
VSS57 175
VSS58 176
VSS59 180
VSS60 181
VSS61 184
VSS62 185
VSS63 188
VSS64 189
VSS65 192
VSS66 193
VSS67 196
VSS68 197
VSS69 201
VSS70 202
VSS71 205
VSS72 206
VSS73 209
VSS74 210
VSS75 213
VSS76 214
VSS77 217
VSS78 218
VSS79 222
VSS80 223
VSS81 226
VSS82 227
VSS83 230
VSS84 231
VSS85 234
VSS86 235
VSS87 238
VSS88 239
VSS89 243
VSS90 244
VSS91 247
VSS92 248
VSS93 251
VSS94 252

SIDE2 264
SIDE1 263
NP_NC2 262
NP_NC1 261

+3VS
R1805 0Ohm @
R1802 0Ohm
R1804 0Ohm @
SPD Address
Read 0XA4
Write 0XA5
SA0
SA1
SA2
R1803 0Ohm
R1801 0Ohm @
R1806 0Ohm

+1.2V
R18182 240Ohm M_B_CB0
R18172 240Ohm M_B_CB1
R18162 240Ohm M_B_CB2
R18152 240Ohm M_B_CB3
R18142 240Ohm M_B_CB4
R18132 240Ohm M_B_CB5
R18122 240Ohm M_B_CB6
R18112 240Ohm M_B_CB7

2016.02.02
R1.2
Change 10 UF from 0805 to 0603

+1.2V
Layout Note: Place these caps near SODIMM
C1841 10UF/6.3V
C1842 10UF/6.3V
C1844 10UF/6.3V
C1845 10UF/6.3V
C1850 10UF/6.3V
C1849 10UF/6.3V
C1862 10UF/6.3V
C1863 10UF/6.3V
MLCC 10UF/6.3V (0603)X5R 20%

+1.2V
Layout Note: Place these caps near SODIMM
C1864 1UF/6.3V
C1865 1UF/6.3V
C1866 1UF/6.3V
C1867 1UF/6.3V
C1868 1UF/6.3V
C1869 1UF/6.3V
C1870 1UF/6.3V
C1871 1UF/6.3V

+1.2V
CE1801 330UF/2.5V @ vx_c3528_h79

+0.6VS
C1846 10UF/6.3V
C1843 10UF/6.3V @
MLCC 10UF/6.3V (0603)X5R 20%

+0.6VS
C1873 1UF/6.3V
C1874 1UF/6.3V
C1875 1UF/6.3V
C1876 1UF/6.3V

+2.5V
C1879 10UF/6.3V
C1880 10UF/6.3V
C1881 1UF/6.3V
C1882 1UF/6.3V
MLCC 10UF/6.3V (0603)X5R 20%

EMI 2015/10/12
+1.2V
C1883 0.1UF/25V @

PEGATRON
Title : DDR4(3)_CH1
BG1-NB4
Engineer: sinsian_Jheng
Size C
Project Name P5HCJ/Megatron
Rev 1.2
Date: Friday, February 05, 2016
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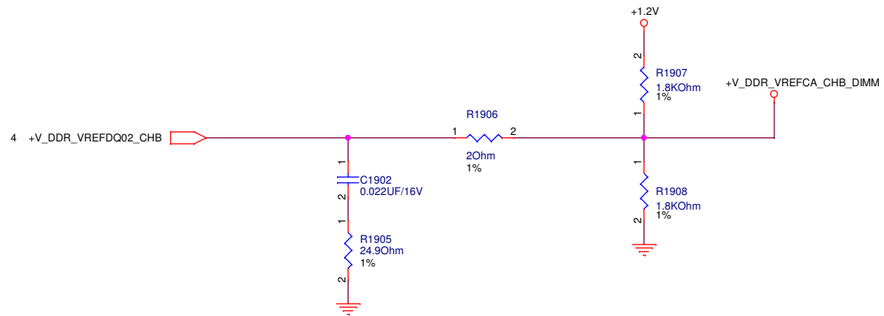
DDR4(3)_CA/DQ Voltage

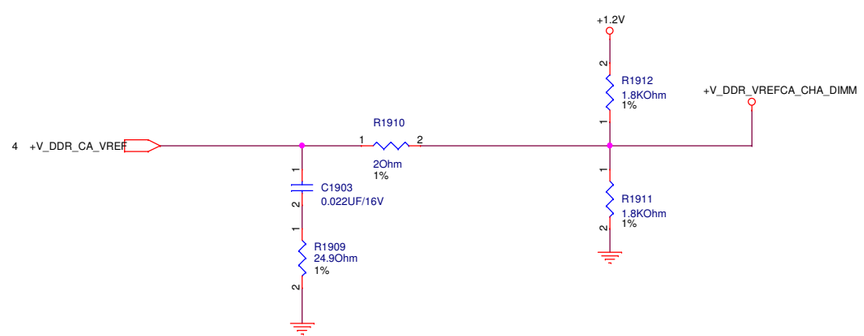
+1.2V → +1.2V 3,4,7,15,16,17,18,57,83

+V_DDR_VREFCA_CHB_DIMM → +V_DDR_VREFCA_CHB_DIMM 18

+V_DDR_VREFCA_CHA_DIMM → +V_DDR_VREFCA_CHA_DIMM 16,17

DDR4 Vref (Intel Schematic Review)





PEGATRON Title : DDR4(3)_CA/DQ Voltage

BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 19 of 96

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PCH(1)_SPI/LPC

+3VSUS_ORG — +3VSUS_ORG 21,22,23,25,26

+3VS — +3VS 3,4,18,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92

RF requirement

SPI_CLK — C2003 3.3PF/50V @ — near AV2

U0301E

SPI - FLASH

28 SPI_CLK	SPI_CLK	AV2	SPI0_CLK	
28 SPI_SO	SPI_SO	AW3	SPI0_MISO	
28 SPI_SI	SPI_SI	AV3	SPI0_MOSI	
28 SPI_WP#_IO2	SPI_WP#_IO2	AW2	SPI0_IO2	
28 SPI_HOLD#_IO3	SPI_HOLD#_IO3	AU4	SPI0_IO3	
28 SPI_CS#0	SPI_CS#0	AU3	SPI0_CS0#	
T2011 1	SPI_CS1#	AU2	SPI0_CS1#	
T2001 1	SPI_CS2#	AU1	SPI0_CS2#	

SPI - TOUCH

T2002 1	GPP_D1	M2	GPP_D1/SPI1_CLK
		M3	GPP_D2/SPI1_MISO
		J4	GPP_D3/SPI1_MOSI
		V1	GPP_D21/SPI1_IO2
		V2	GPP_D22/SPI1_IO3
T2007 1	GPP_D0	M1	GPP_D0/SPI1_CS#

C LINK

53 CL_CLK	CL_CLK	G3	CL_CLK
53 CL_DATA	CL_DATA	G2	CL_DATA
53 CL_RST#	CL_RST#	G1	CL_RST#

30 RCIN#	RCIN#	AW13	GPP_A0/RCIN#
30,44,62 INT_SERIRQ	INT_SERIRQ	AY11	GPP_A6/SERIRQ

940432

01V010000015

SMBUS, SMLINK

GPP_C0/SMBCLK	R7	SMB_CLK	SMB_CLK 28	SODIMM
GPP_C1/SMBDATA	R8	SMB_DAT	SMB_DAT 28	SODIMM
GPP_C2/SMBALERT#	R10	SMBALERT# 1 T2008		SODIMM
GPP_C3/SML0CLK	R9	SML0_CLK_NFC 1 T2003		PDG Reserve For NFC
GPP_C4/SML0DATA	W2	SML0_DAT_NFC 1 T2004		PDG Reserve For NFC
GPP_C5/SML0ALERT#	W1	SML0ALERT#		PDG Reserve For NFC
GPP_C6/SML1CLK	W3	SML1_CLK	SML1_CLK 28	To EC
GPP_C7/SML1DATA	V3	SML1_DAT	SML1_DAT 28	To EC
GPP_B23/SML1ALERT#/PCHHOT#	AM7	SML1ALERT# 1 T2010		To EC

LPC

GPP_A1/LAD0/ESPI_IO0	AY13	LPC_AD0	LPC_AD0 30,44,62
GPP_A2/LAD1/ESPI_IO1	BA13	LPC_AD1	LPC_AD1 30,44,62
GPP_A3/LAD2/ESPI_IO2	BB13	LPC_AD2	LPC_AD2 30,44,62
GPP_A4/LAD3/ESPI_IO3	AY12	LPC_AD3	LPC_AD3 30,44,62
GPP_A5/LFRAME#/ESPI_CS#	BA12	LPC_FRAME#	LPC_FRAME# 30,44,62
GPP_A14/SUS_STAT#/ESPI_RESET#	BA11	PM_SUS_STAT#	PM_SUS_STAT# 62

TPM

GPP_A9/CLKOUT_LPC0/ESPI_CLK	AW9	CLK_KBCPCI_PCH_R	R20001 1 2 22Ohm 1% — CLK_KBCPCI_PCH 30
GPP_A10/CLKOUT_LPC1	AY9	CLK_LPC1	R20021 2 22Ohm 1% — CLK_DEBUG 44
GPP_A8/CLKRUN#	AW11		R20141 2 22Ohm 1% — LPCCLK_TPM 62

C2001 10PF/50V @ — C2002 10PF/50V @

PM_CLKRUN# — PM_CLKRUN# 30,62

R2004 1 2 20KOhm SMBALERT# R2003 1 2 2.2KOhm — +3VSUS_ORG

SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable

CRB 0.53 reserve 150k ohm

R2006 1 2 20KOhm SML0ALERT# R2005 1 2 4.7KOhm — +3VSUS_ORG

SML0ALERT# - Internal weak pull down 20 kohm
0 : LPC EC (default)
1 : eSPI EC

CRB 0.53 reserve 150k ohm

R2008 1 2 20KOhm R2007 1 2 4.7KOhm — +3VSUS_ORG

BBS 21

BBS - Internal weak pull down 20k ohm
Boot BIOS Strap
0 : SPI destination (default)
1 : LPC destination

Unmount R2013,R2009
Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

+3VS

PM_CLKRUN# R2013 1 2 10KOhm

INT_SERIRQ R2009 1 2 10KOhm

+3VSUS_ORG

SMB_CLK RN2001B 3 2.2KOhm 4

SMB_DAT RN2001A 1 2.2KOhm 2

SML1_DAT RN2002B 3 2.2KOhm 4

SML1_CLK RN2002A 1 2.2KOhm 2

SML1ALERT# R2012 1 2 150KOhm

MOW WW52
To enable Direct Connect Interface (DCI),
a 150K pull up resistor will need to be added to PCHHOT#
pin. This pin must be low during the rising edge of RSMRST#.

PEGATRON Title : PCH(1)_SPI/LPC

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

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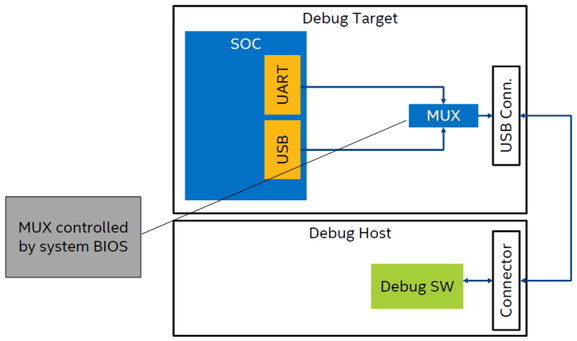
PCH(2)_ISH

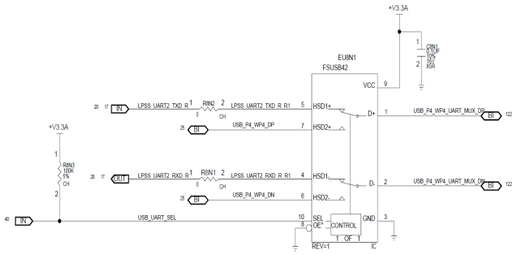
Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required



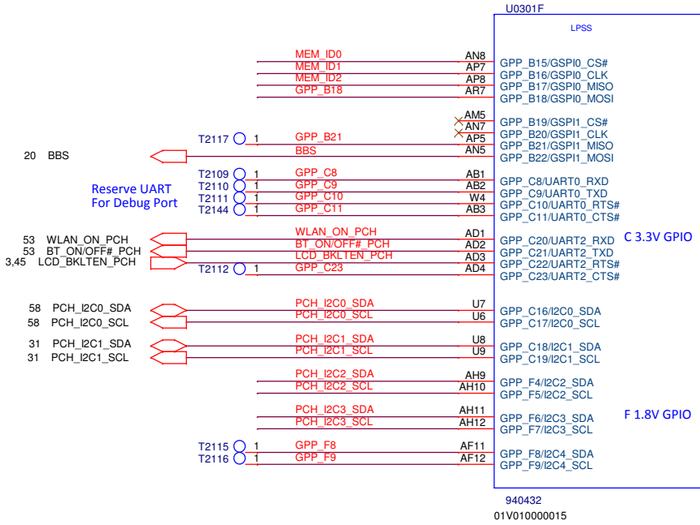
To implement UART for WIN7 WHCK requirement if need

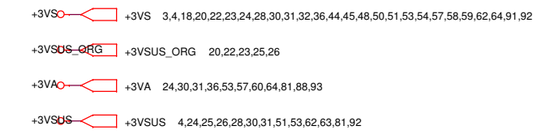
Please refer to Intel document #548689 - RVP5

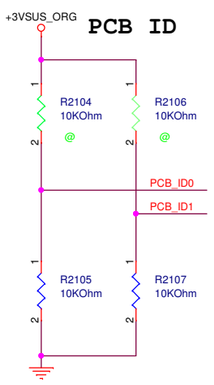


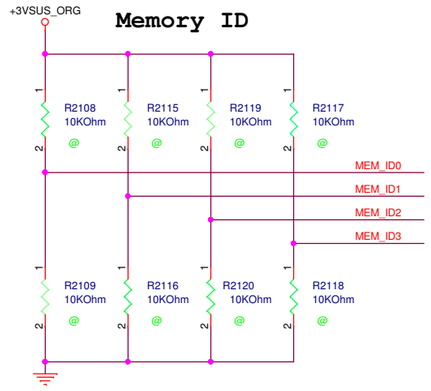
External SensorHub

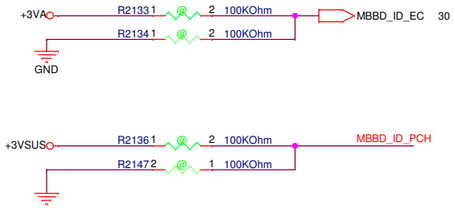
Touch Pad

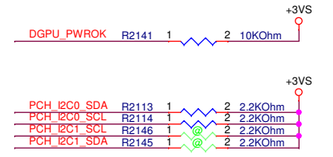




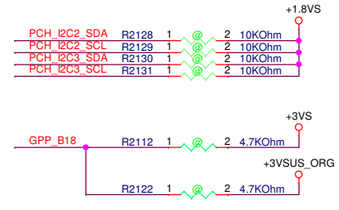








Change To 2.2Kohm PU side
Default PU +3V For S3 Resume by TP side



GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

Default is GPO, to reserve pull high to +3VSUS_ORG

	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R10	0	0
R11	0	1

	MEM_ID3 (GPP_C15)	MEM_ID2 (GPP_B17)	MEM_ID1 (GPP_B16)	MEM_ID0 (GPP_B15)
SAMSUNG K4A8G165WB-BCPB 2133MT 8Gb	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1

	MBBD_ID_PCH	location
UMA	0	R2147
DIS	1	R2136

PEGATRON Title : PCH(2)_ISH

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

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PCH(3)_HDA_SDIO

+VCCPAZIO — +VCCPAZIO 26
+3VS — +3VS 3,4,18,20,21,23,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+3VSUS_ORG — +3VSUS_ORG 20,21,23,25,26

RF requirement

HDA_BCLK
C2201 22PF/50V @

U0301G

AUDIO

36 HDA_SYNC	HDA_SYNC	SP2201 1 2	HDA_SYNC_R	BA22	HDA_SYNC/I2S0_SFRM	
36 HDA_BCLK	HDA_BCLK	SP2202 1 2	HDA_BCLK_R	AY22	HDA_BLK/I2S0_SCLK	
36 HDA_SDO	HDA_SDO	SP2203 1 2	HDA_SDO_R	BB22	HDA_SDO/I2S0_TXD	
36 HDA_SDI0	HDA_SDI0	SP2204 1 2	HDA_SDI0_R	BA21	HDA_SDI0/I2S0_RXD	
		T2201 1	HDA_SDI1	AY21	HDA_SDI1/I2S1_RXD	
36 HDA_RST#	HDA_RST#	SP2205 1 2	HDA_RST#_R	AW22	HDA_RST#/I2S1_SCLK	
		T2202 1	GPP_D23	J5	GPP_D23/I2S_MCLK	
				AY20	I2S1_SFRM	
				AW20	I2S1_TXD	
				AK7		
				AK6	GPP_F1/I2S2_SFRM	
				AK9	GPP_F0/I2S2_SCLK	
				AK10	GPP_F2/I2S2_TXD	
					GPP_F3/I2S2_RXD	
				H5		
				D7	GPP_D19/DMIC_CLK0	
					GPP_D20/DMIC_DATA0	
For Keyboard backlight Fn Key				D8		
58 KBBL_LV1	KBBL_LV1			C8	GPP_D17/DMIC_CLK1	
58 KBBL_LV0	KBBL_LV0				GPP_D18/DMIC_DATA1	
36 HDA_SPKR	HDA_SPKR	SP2208 1 2	SPKR	AW5	GPP_B14/SPKR	

SDIO/SDXC

GPP_G0/SD_CMD	AB11	LID_STAT0#_C	LID_STAT0#_C 58
GPP_G1/SD_DATA0	AB13	LID_STAT1#_C	LID_STAT1#_C 58
GPP_G2/SD_DATA1	AB12	LID_STAT2#_C	LID_STAT2#_C 58
GPP_G3/SD_DATA2	W12	KB_BL_INT#	KB_BL_INT# 58
GPP_G4/SD_DATA3	W11		
GPP_G5/SD_CD#	W10	SHB_RST#_CPU	SHB_RST#_CPU 58
GPP_G6/SD_CLK	W8	MODE INT#_C	MODE INT#_C 58
GPP_G7/SD_WP	W7	ESH_I2C_INT#	ESH_I2C_INT# 58
GPP_A17/SD_PWR_EN#/ISH_GP7	BA9		
GPP_A16/SD_1P8_SEL	BB9		
SD_RCOMP	AB7	SKL_SD_RCOMP	R2201 1 1% 2 200Ohm
GPP_F23	AF13	GPP_F23	1 T2224

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+3VS
R2202 1 @ 2 20KOhm SPKR R2209 1 @ 2 4.7KOhm
+3VSUS_ORG
GND
R2210 1 @ 2 4.7KOhm

SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS_ORG

+VCCPAZIO
CRB 0.53 reserve 150k ohm
R2203 4.7KOhm @
HDA_SDO_R — RB751V-40 2 1 D2201 — PCH_FLASH_DESCRIPTOR 30

HDA_SDO - Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRRIDE
0 : Enable security measure defined in the Flash Descriptor
1 : Disable Flash Descriptor Security

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PCH(3)_HDA/SDIO
BG1-NB4
Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 22 of 96

PCH(4)_USB/PCIE/SATA

+3VSUS_ORG — +3VSUS_ORG 20,21,22,25,26

+3VS — +3VS 3,4,18,20,21,22,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92

U0301H

PCIE/USB3/SATA

PCIE x 4 -dGPU

70 PCIENB_RXN1 — PCIENB_RXN1 — H13 — PCIE1_RXN/USB3_5_RXN
70 PCIENB_RXP1 — PCIENB_RXP1 — G13 — PCIE1_RXP/USB3_5_RXP
70 PCIECG_TXN1 — PCIECG_TXN1 /NGA C23041 2 0.22UF/10V PCIEG_TXN1_C — B17 — PCIE1_TXN/USB3_5_TXN
70 PCIECG_TXP1 — PCIECG_TXP1 /NGA C23031 2 0.22UF/10V PCIEG_TXP1_C — A17 — PCIE1_TXP/USB3_5_TXP

70 PCIENB_RXN2 — PCIENB_RXN2 — G11 — PCIE2_RXN/USB3_6_RXN
70 PCIENB_RXP2 — PCIENB_RXP2 — F11 — PCIE2_RXP/USB3_6_RXP
70 PCIECG_TXN2 — PCIECG_TXN2 /NGA C23101 2 0.22UF/10V PCIEG_TXN2_C — D16 — PCIE2_TXN/USB3_6_TXN
70 PCIECG_TXP2 — PCIECG_TXP2 /NGA C23091 2 0.22UF/10V PCIEG_TXP2_C — C16 — PCIE2_TXP/USB3_6_TXP

70 PCIENB_RXN3 — PCIENB_RXN3 — H16 — PCIE3_RXN
70 PCIENB_RXP3 — PCIENB_RXP3 — G16 — PCIE3_RXP
70 PCIECG_TXN3 — PCIECG_TXN3 /NGA C23081 2 0.22UF/10V PCIEG_TXN3_C — D17 — PCIE3_TXN
70 PCIECG_TXP3 — PCIECG_TXP3 /NGA C23071 2 0.22UF/10V PCIEG_TXP3_C — C17 — PCIE3_TXP

70 PCIENB_RXN4 — PCIENB_RXN4 — G15 — PCIE4_RXN
70 PCIENB_RXP4 — PCIENB_RXP4 — F15 — PCIE4_RXP
70 PCIECG_TXN4 — PCIECG_TXN4 /NGA C23061 2 0.22UF/10V PCIEG_TXN4_C — B19 — PCIE4_TXN
70 PCIECG_TXP4 — PCIECG_TXP4 /NGA C23051 2 0.22UF/10V PCIEG_TXP4_C — A19 — PCIE4_TXP

F16 — PCIE5_RXN
E16 — PCIE5_RXP
C19 — PCIE5_TXN
D19 — PCIE5_TXP

G18 — PCIE6_RXN
F18 — PCIE6_RXP
D20 — PCIE6_TXN
C20 — PCIE6_TXP

HDD

54 SATA_RXN0_HDD — SATA_RXN0_HDD — F20 — PCIE7_RXN/SATA0_RXN
54 SATA_RXP0_HDD — SATA_RXP0_HDD — E20 — PCIE7_RXP/SATA0_RXP
54 SATA_TXN0_HDD — SATA_TXN0_HDD — B21 — PCIE7_TXN/SATA0_TXN
54 SATA_TXP0_HDD — SATA_TXP0_HDD — A21 — PCIE7_TXP/SATA0_TXP

SATA_SSD

54 SATA_RXN1_SSD — SATA_RXN1_SSD — G21 — PCIE8_RXN/SATA1A_RXN
54 SATA_RXP1_SSD — SATA_RXP1_SSD — F21 — PCIE8_RXP/SATA1A_RXP
54 SATA_TXN1_SSD — SATA_TXN1_SSD — D21 — PCIE8_TXN/SATA1A_TXN
54 SATA_TXP1_SSD — SATA_TXP1_SSD — C21 — PCIE8_TXP/SATA1A_TXP

WLAN

53 PCIE_RXN9_WLAN — PCIE_RXN9_WLAN — E22 — PCIE9_RXN
53 PCIE_RXP9_WLAN — PCIE_RXP9_WLAN — E23 — PCIE9_RXP
53 PCIE_TXN9_WLAN — PCIE_TXN9_WLAN C23111 2 0.1UF/16V PCIE_TXN9_WLAN_C — B23 — PCIE9_TXN
53 PCIE_TXP9_WLAN — PCIE_TXP9_WLAN C23121 2 0.1UF/16V PCIE_TXP9_WLAN_C — A23 — PCIE9_TXP

F25 — PCIE10_RXN
E25 — PCIE10_RXP
D23 — PCIE10_TXN
C23 — PCIE10_TXP

PCIE_RCOMP PDG 0.9 need 100 ohm 0.1% / CRB 0.53 use 100 ohm +-1%

R2301 1 1% 2 100Ohm — PCIE_RCOMPN — F5 — PCIE_RCOMPN
PCIE_RCOMPP — E5 — PCIE_RCOMPP

Reserve TP for XDP

T2323 1 — PROC_PRDY# — D56 — PROC_PRDY#
T2324 1 — PROV_PREQ# — D61 — PROC_PREQ#
PIRQA# — BB11 — GPP_A7/PIRQA#

E28 — PCIE11_RXN/SATA1B_RXN
E27 — PCIE11_RXP/SATA1B_RXP
D24 — PCIE11_TXN/SATA1B_TXN
C24 — PCIE11_TXP/SATA1B_TXP
E30 — PCIE12_RXN/SATA2_RXN
F30 — PCIE12_RXP/SATA2_RXP
A25 — PCIE12_TXN/SATA2_TXN
B25 — PCIE12_TXP/SATA2_TXP

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SSIC / USB3

USB3_1_RXN — H8 — USB3_RXN1 — USB3_RXN1 52
USB3_1_RXP — G8 — USB3_RXP1 — USB3_RXP1 52
USB3_1_TXN — C13 — USB3_TXN1 — USB3_TXN1 52
USB3_1_TXP — D13 — USB3_TXP1 — USB3_TXP1 52

USB3_2_RXN/SSIC_RXN — J6 — USB3_RXN2 — USB3_RXN2 52
USB3_2_RXP/SSIC_RXP — H6 — USB3_RXP2 — USB3_RXP2 52
USB3_2_TXN/SSIC_TXN — B13 — USB3_TXN2 — USB3_TXN2 52
USB3_2_TXP/SSIC_TXP — A13 — USB3_TXP2 — USB3_TXP2 52

USB3_3_RXN — J10 — USB3_RXN3 — USB3_RXN3 14
USB3_3_RXP — H10 — USB3_RXP3 — USB3_RXP3 14
USB3_3_TXN — B15 — USB3_TXN3 — USB3_TXN3 14
USB3_3_TXP — A15 — USB3_TXP3 — USB3_TXP3 14

USB3_4_RXN — E10 — USB3_RXN4 — USB3_RXN4 14
USB3_4_RXP — F10 — USB3_RXP4 — USB3_RXP4 14
USB3_4_TXN — C15 — USB3_TXN4 — USB3_TXN4 14
USB3_4_TXP — D15 — USB3_TXP4 — USB3_TXP4 14

USB2

USB2N_1 — AB9 — USB_PN1_30 — USB_PN1_30 52
USB2P_1 — AB10 — USB_PP1_30 — USB_PP1_30 52

USB2N_2 — AD6 — USB_PN2_30 — USB_PN2_30 52
USB2P_2 — AD7 — USB_PP2_30 — USB_PP2_30 52

USB2N_3 — AH3 — USB_PN3_PD — USB_PN3_PD 14
USB2P_3 — AJ3 — USB_PP3_PD — USB_PP3_PD 14

USB2N_4 — AD9 — USB_PN4_20 — USB_PN4_20 64
USB2P_4 — AD10 — USB_PP4_20 — USB_PP4_20 64

USB2N_5 — AJ1 — USB_PN5_BT — USB_PN5_BT 53
USB2P_5 — AJ2 — USB_PP5_BT — USB_PP5_BT 53

USB2N_6 — AF6 — USB_PN6_TS — USB_PN6_TS 45
USB2P_6 — AF7 — USB_PP6_TS — USB_PP6_TS 45

USB2N_7 — AH1 — USB_PN7_CCD — USB_PN7_CCD 64
USB2P_7 — AH2 — USB_PP7_CCD — USB_PP7_CCD 64

USB2N_8 — AF8 — USB_PN8_CR — USB_PN8_CR 64
USB2P_8 — AF9 — USB_PP8_CR — USB_PP8_CR 64

USB2N_9 — AG1 — AG2
USB2P_9

USB2N_10 — AH7 — AH8
USB2P_10

USB2_COMP PDG 1.0 R=113 +-1%

USB2_COMP — AB6 — USBCOMP — R2302 1 1% 2 113Ohm
USB2_ID — AG3 — USB2_ID_OTG — R2319 1 2 1KOhm
USB2_VBUSSENSE — AG4 — USB2_VBUSSENSE_OTG — R2320 1 2 1KOhm

MOW 5.1.3 If the platform does not support Dual Role, then USB2_ID pin shall be connected directly to GND.

GPP_E9/USB2_OC0# — A9 — OC0# — R2321 1 2 0Ohm — USB_OC0#_PCH 52
GPP_E10/USB2_OC1# — C9 — OC1# — R2309 1 2 0Ohm — USB_OC1#_PCH 52
GPP_E11/USB2_OC2# — D9 — OC2# — R2310 1 2 0Ohm — USB_OC2#_PCH 64
GPP_E12/USB2_OC3# — B9 — OC3# — R9227 1 2 0Ohm — USB_OC3#_PCH 13

USB30 with USB Chager
USB30
USB20
Type C

{OD} GPP_E4/DEVSLP0 — J1
{OD} GPP_E5/DEVSLP1 — J2 — SATA_DEVSLP1 — SATA_DEVSLP1 51
{OD} GPP_E6/DEVSLP2 — J3

SATA SSD

GPP_E0/SATAXPCIE0/SATAGP0 — H2
GPP_E1/SATAXPCIE1/SATAGP1 — H3 — SATA_SSD1_PEDET — SATA_SSD1_PEDET 51
GPP_E2/SATAXPCIE2/SATAGP2 — G4 — SATA_SSD2_PEDET_R 1 — T2339

GPP_E8/SATALED# — H1 — SATA_LED# 1 — T2338

USB30 with USB Chager
USB30 with USB Chager
USB30
USB3 Type C
USB20
Bluetooth
Touch screen
Camera
Card reader

+3VSUS_ORG

OC0# — 10KOhm 3 — 4 RN2301B
OC1# — 10KOhm 7 — 8 RN2301D
OC2# — 10KOhm 1 — 2 RN2301A
OC3# — 10KOhm 5 — 6 RN2301C

+3VS

SATA_LED# — R2304 1 2 10KOhm
PIRQA# — R2318 1 2 10KOhm

Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

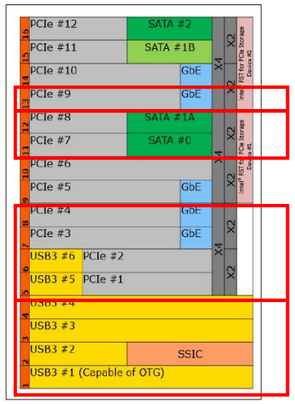

Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4

Title : PCH(4)_USB/PCIE/SATA

Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 23 of 96

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PCH(5)_CLK

SRCCLKREQ#[5:0] (PDG v1.3 Page 835)
Any un-used, disabled, must be left as no connects at the PCH side on the platform.
Any used, enabled, should connect to a PCIe* connector pin or a device down ball with a 10K Ohm ±10% external pull-up resistor to core rail.

CLK_REQ4_WLAN#_R — R2429 10KOhm +3VSUS; R2408 10KOhm +3VS; R2411 10KOhm

CLK_REQ5_LAN#_R — R2421 10KOhm +3VS; R2409 10KOhm +3VSUS; R2412 10KOhm

CLK_REQ0_PEG#_R — R2410 10KOhm +3VS; R2413 10KOhm

U0301I — CSI-2

A36	CSI2_DN0	CSI2_CLKN0	C37
B36	CSI2_DP0	CSI2_CLKP0	D37
C38	CSI2_DN1	CSI2_CLKN1	C32
D38	CSI2_DP1	CSI2_CLKP1	D32
C36	CSI2_DN2	CSI2_CLKN2	C29
D36	CSI2_DP2	CSI2_CLKP2	D29
A38	CSI2_DN3	CSI2_CLKN3	B26
B38	CSI2_DP3	CSI2_CLKP3	A26
C31	CSI2_DN4	CSI2_COMP	E13 — CSI2_COMP
D31	CSI2_DP4	GPD_4/FLASHTRIG	B7 — GPD_4 — T2417
C33	CSI2_DN5		
D33	CSI2_DP5	EMMC	
A31	CSI2_DN6		
B31	CSI2_DP6	GPP_F13/EMMC_DATA0	AP2
A33	CSI2_DN7	GPP_F14/EMMC_DATA1	AP1
B33	CSI2_DP7	GPP_F15/EMMC_DATA2	AP3
		GPP_F16/EMMC_DATA3	AN3
A29	CSI2_DN8	GPP_F17/EMMC_DATA4	AN1
B29	CSI2_DP8	GPP_F18/EMMC_DATA5	AN2
C28	CSI2_DN9	GPP_F19/EMMC_DATA6	AM4
D28	CSI2_DP9	GPP_F20/EMMC_DATA7	AM1
A27	CSI2_DN10		
B27	CSI2_DP10	GPP_F21/EMMC_RCLK	AM2
C27	CSI2_DN11	GPP_F22/EMMC_CLK	AM3
D27	CSI2_DP11	GPP_F12/EMMC_CMD	AP4
		EMMC_RCOMP	AT1 — EMMC_RCOMP

940432
01V010000015

R2418 100Ohm; R2419 200Ohm

+VCCF24NS_1P0 — +VCCF24NS_1P0 26
+RTCBAT — +RTCBAT 60
+VCC_RTC — +VCC_RTC 25,26,36
+3VA — +3VA 21,30,31,36,53,57,60,64,81,88,93
+3VS — +3VS 3,4,18,20,21,22,23,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+3VSUS — +3VSUS 4,21,25,26,28,30,31,51,53,62,63,81,92

+VCCDSW — +VCCDSW 25,26

+3VA
R2425 0Ohm; R2423 1.5KOhm 1%; R2424 45.3KOhm 1%
+RTC_AC
+VCC_RTC
R2420 1KOhm
D2401 RB751V-40 0.37V/30mA
D2402 RB751V-40 0.37V/30mA
C2407 1UF/6.3V
RTC_BAT R2405 1KOhm
+RTCBAT
12V17AISM001 WTOB_CON_2P
J2401 — SIDE1, SIDE2
P/N:1217-01EP000

VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V.

CLKOUT_PCIE_P/N[5:0] (PDG v1.3 Page420)
Any differential clock pair not being used must be left as no connect

U0301J — CLOCK SIGNALS

T2401 — SNN_CLKOUT_PCIE_N0 — D42 CLKOUT_PCIE_N0; C42 CLKOUT_PCIE_P0; AR10 GPP_B5/SRCCLKREQ0#
B42 CLKOUT_PCIE_N1; A42 CLKOUT_PCIE_P1; AT7 GPP_B6/SRCCLKREQ1#
T2403 — SNN_CLKOUT_PCIE_N2 — D41 CLKOUT_PCIE_N2; C41 CLKOUT_PCIE_P2; AT8 GPP_B7/SRCCLKREQ2#

70 CLK_PCIE_PEG#_PCH — CLK_PCIE_PEG#_PCH SP2415 — CLK_PCIE_PEG#_PCH_R — D40 CLKOUT_PCIE_N3
70 CLK_PCIE_PEG_PCH — CLK_PCIE_PEG_PCH SP2416 — CLK_PCIE_PEG_PCH_R — C40 CLKOUT_PCIE_P3
70 CLK_REQ0_PEG# — CLK_REQ0_PEG# SP2417 — CLK_REQ0_PEG#_R — AT10 GPP_B8/SRCCLKREQ3#

53 CLK_PCIE_WLAN#_PCH — CLK_PCIE_WLAN#_PCH SP2412 — CLK_PCIE_WLAN#_PCH_R — B40 CLKOUT_PCIE_N4
53 CLK_PCIE_WLAN_PCH — CLK_PCIE_WLAN_PCH SP2413 — CLK_PCIE_WLAN_PCH_R — A40 CLKOUT_PCIE_P4
53 CLK_REQ4_WLAN# — CLK_REQ4_WLAN# SP2414 — CLK_REQ4_WLAN#_R — AU8 GPP_B9/SRCCLKREQ4#

CLK_REQ5_LAN#_R — AU7 GPP_B10/SRCCLKREQ5#

E40 CLKOUT_PCIE_N5; E38 CLKOUT_PCIE_P5

CLKOUT_ITPXDP_N F43; CLKOUT_ITPXDP_P E43
GPD8/SUSCLK — BA17 SUSCLK_PCH
XTAL24_IN E37 XTAL_24M_IN; XTAL24_OUT E35 XTAL_24M_OUT
XCLK_BIASREF — E42 XCLK_BIASREF — R24171 2.7KOhm; R24221 60.4Ohm
RTCX1 AM18 XTAL_32K_X1; RTCX2 AM20 XTAL_32K_X2
SRTCRST# AN18 SRTC_RST#; RTCRST# AM16 HTC_RST#

940432
01V010000015

+VCCF24NS_1P0
+VCC_RTC
R2403 20KOhm; R2404 20KOhm
JRST2402 SGL_JUMP; C2405 1UF/6.3V
JRST2401 SGL_JUMP; C2406 1UF/6.3V
Q2401 2N7002
30 SW_RTCRST — R2406 0Ohm
R2407 10KOhm

2015.11.12
R1.1
545659_545659_SKL_PCH_EDS P.182
The SRCCLKREQ# signals can be configured to map to any of the PCH PCI Express* Root Ports while using any of the CLKOUT_PCIE_P/N differential pairs.

2015.04.06 YenPin
Add CLOCK Buffer Schematic (CRB Page123)

R2426~R2428 Close To U2401

SUSCLK is on the DSW well and is available earlier in the boot sequence.

+VCCDSW
C2408 0.01UF/50V
51 M_2_SSD1_SUSCLK — R2426 5% 33Ohm — M_2_SSD1_SUSCLK_R
U2401 — VDD, Q0, Q1, GND, OE, Q3, Q2, ICLK
ICS553MILFT
06V100000009
SUSCLK_PCH_R — R2428 5% 33Ohm — SUSCLK_PCH

XTAL_24M_IN / XTAL_24M_OUT
R2401 1MOhm
SP2401 NB_R0402_5MIL_SMALL
X2401 24MHZ
XTAL_24M_OUT_R
C2402 10PF/50V; C2401 10PF/50V

XTAL_32K_X1 / XTAL_32K_X2
R2402 10MOhm
SP2402 NB_R0402_5MIL_SMALL
X2402 32.768KHZ 07V080000075 +/-20ppm/9PF
XTAL_32K_X1_R
C2404 7PF/50V; C2403 7PF/50V

2015.11.23
R1.1
Vendor suggestion 7PF

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Title :PCH(5)_CLK
Engineer: sinsian_Jheng
Size C | Project Name P5HCJ/Megatron | Rev 1.2
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N/A

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PCH(6)_POWER MANAGE

+3VSUS_ORG — +3VSUS_ORG 20,21,22,23,26
+VCC_RTC — +VCC_RTC 24,26,36
+VCCDSW — +VCCDSW 24,26
+VCCST_CPU — +VCCST_CPU 3,5,7,9,32
+3V — +3V 31,57,58,64,91
+3VSUS — +3VSUS 4,21,24,26,28,30,31,51,53,62,63,81,92

U0301K
SYSTEM POWER MANAGEMENT
940432
01V010000015

30 PM_RSMRST# — SP2501 — PLT_RST# AN10 — PM_SYS_RESET#_R B5 — PM_RSMRST_R AY17
T2501 — H_CPUPWRGD_TP — R2503 1KOhm — H_CPUPWRGD A68 — H_VCCST_PWRGD_MCP B65
ALL_SYS_PWRGD delay 99 ms from EC
30,63 SYS_PWROK — R2504 0Ohm — SYS_PWROK_R B6
PM_PWROK — R2505 0Ohm — PM_PCH_PWROK_R BA20
PM_RSMRST_R — R2506 0Ohm — PCH_DPWROK BB20
DSW function / non-AMT
30 SUSWARN#/SUSPWRDNACK — R2508 0Ohm — SUS_PWR_ACK_R AR13
SUS_PWR_ACK_R — R2509 0Ohm — SUSACK#_R AP11
30 SUSACK# — R2510 0Ohm
53 WAKE_PCIE# — BB15
LAN_WAKE# AM15
T2502 — GPD11 AW17
T2508 — GPD7 AT15

GPP_B13/PLTRST# — SYS_RESET# — RSMRST#
PROCPWRGD — VCCST_PWRGD
SYS_PWROK — PCH_PWROK — DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK — GPP_A15/SUSACK#
WAKE# — GPD2/LAN_WAKE# — GPD11/LANPHYPC — GPD7/RSVD

GPP_B12/SLP_S0# — AT11 SLP_S0# — T2503
GPD4/SLP_S3# — AP15 SLP_S3#_R — SP2502 — PM_SUSB# 30,63
GPD5/SLP_S4# — BA16 SLP_S4#_R — SP2503 — PM_SUSC# 30,63
GPD10/SLP_S5# — AY16 GPD10 — T2504
SLP_SUS# — AN15 SLP_SUS# — T2510
SLP_LAN# — AW15 SLP_LAN# — T2505
GPD9/SLP_WLAN# — BB17 SLP_WLAN# — T2506
GPD6/SLP_A# — AN16 ME_PM_SLP_M#_PCH — T2507
If Deep Sx is not implemented on the platform, this signal may be left as no connect
GPD3/PWRBTN# — BA15
GPD1/ACPRESENT — AY15 AC_PRESENT_R — R2532 0Ohm — PM_PWRBTN# 30 — ME_AC_PRESENT 30
GPD0/BATLOW# — AU13 BATLOW#
GPP_A11/PME# — AU11 PME#
INTRUDER# — AP16 SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# — AM10 MPHY_EXT_PWR_GATEB_R — T2509
GPP_B2/VRALERT# — AM11 VR_ALERT#
internal pull high

2016.02.05
R1.2
ME concern. Remove U2501.

PLT_RST# — R2515 0Ohm — BUF_PLT_RST# 30,32,53,62,70
C2502 100PF/50V @ — GND
C2503 100PF/50V @ — R2516 10KOhm

+VCCDSW
BATLOW# — R2522 10KOhm
LAN_WAKE# — R2523 10KOhm
GPD7 — R2524 10KOhm
WAKE_PCIE# — R2525 1KOhm
AC_PRESENT_R — R2526 10KOhm
PM_PWRBTN# — R2533 10KOhm
R1.0 PCH internal pull high
R1.1 1111 Change Option Mount
for weak voltage at beginning of AC plug-in
+VCC_RTC
SM_INTRUDER# — R2513 1MOhm
+3VSUS_ORG
internal pull high
PME# — R2527 10KOhm
Set to GPI
VR_ALERT# — R2528 10KOhm
PM_SYS_RESET#_R — R2501 3KOhm

+3VSUS — +VCCST_CPU
U2503
DELAY_ALL_SYSTEM_PWRGD — R2529 0Ohm
ALL_SYSTEM_PWRGD — R2530 0Ohm
EC delay ALL_SYSTEM_PWRGD 2ms
H_VCCST_PWRGD_L — NC A GND VCC Y — H_VCCST_PWRGD_R
74AUP1G07GW
06V030000021
C2504 0.1UF/16V
R2520 1KOhm
C2505 0.1UF/16V
R2521 1% 60.4Ohm — H_VCCST_PWRGD_MCP
+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms

+3VSUS
30,92 ALL_SYSTEM_PWRGD — R2531 0Ohm
30 DELAY_ALL_SYSTEM_PWRGD — SP2506 — ALL_SYSTEM_PWRGD_PMOK
80,92 VRM_PWRGD — SP2507 — VR_READY_PMOK
U2502 A B GND VCC Y
Vcc=2~5.5
PM_PWROK
R2517 0Ohm
R2519 10KOhm
GND

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Title : PCH(6)_POWER MANAGE
Engineer: sinsian_Jheng
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PCH(7)_POWER

+VCCPRIM_CORE +VCCPRIM_CORE 82
+1.0VSUS +1.0VSUS 82
+VCCMPHYGTAON_1P0_LS_SIP +VCCMPHYGTAON_1P0_LS_SIP 82
+VCCDSW +VCCDSW 24,25
+3VSUS_ORG +3VSUS_ORG 20,21,22,23,25
+1.8VSUS +1.8VSUS 9,84
+VCCPAZIO +VCCPAZIO 22
+VCC_RTC +VCC_RTC 24,25,36
+VCCF24NS_1P0 +VCCF24NS_1P0 24
+VCCMPHYGTAON_1P0_LS +VCCMPHYGTAON_1P0_LS 82
+3VSUS +3VSUS 4,21,24,25,28,30,31,51,53,62,63,81,92

+3VSUS_ORG/+1.8VSUS to +1.0VSUS >200us (tPCH06)

+3VSUS JP2601 +3VSUS_ORG
2MM_OPEN_5MIL

w/o DSW
+3VSUS_ORG R2633 0Ohm +VCCDSW

+1.0VSUS 4A +VCCMPHYGTAON_1P0_LS +VCCMPHYGTAON_1P0_LS_SIP 2A +VCCSRAM_1P0
R2637 0Ohm 0.642A +VCCAMPHYPLL_1P0
R2638 0Ohm 0.088A +VCCAPLLEBB_1P0
R2639 0Ohm 0.033A

Table 10-5. SKL U / SKL Y PCH-LP
VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

SATA Gen3 Port X 2
PCIe Gen3 Lane X 5
USB3 Port X 3
All HSIO disabled (basic comsunption)
=0.154x5+0.132x2+0.132x3 = 1.43A

+1.0VSUS R2601 0Ohm C2601 1UF/10V @ near AB19
+VCCPRIM_CORE R2602 0Ohm C2602 1UF/10V @ near AF18
+1.0VSUS R2603 0Ohm near K17 C2603 1UF/10V

+VCCPRIM_1P0 0.696A AB19 AB20 P18 VCCPRIM_1P0_1 VCCPRIM_1P0_2 VCCPRIM_1P0_3
2.574A AF18 AF19 V20 V21 VCCPRIM_CORE_1 VCCPRIM_CORE_2 VCCPRIM_CORE_3 VCCPRIM_CORE_4
Decoupling cap for internal power
+VCCDSW_1P0 C2604 2 1UF/10V near AL1 AL1 DCPDSW_1p0
+VCCMPHYAON_1P0 0.022A K17 L1 VCCMPHYAON_1P0_1 VCCMPHYAON_1P0_2
+VCCMPHYGTAON_1P0_LS_SIP C2605 47UF/6.3V @ near N15 C2606 1UF/10V @ N/A near N15
+VCCAMPHYPLL_1P0 1.01A N15 N16 N17 P15 P16 VCCMPHYGT_1P0_1 VCCMPHYGT_1P0_2 VCCMPHYGT_1P0_3 VCCMPHYGT_1P0_4 VCCMPHYGT_1P0_5
+VCCAPLL_1P0 C2607 1UF/10V @ near K15 0.088A K15 L15 VCCAMPHYPLL_1P0_1 VCCAMPHYPLL_1P0_2
+1.0VSUS R2604 0Ohm C2608 47UF/6.3V C2648 0.1UF/16V @ near V15 2015.11.18 R1.1 RF: Change to 0 ohm
+1.0VSUS R2605 0Ohm +V1.00A_SIP 0.026A V15 VCCAPLL_1P0
+VCCPDSW_3P3 0.696A AB17 Y18 VCCPRIM_1P0_4 VCCPRIM_1P0_5
+3VSUS_ORG R2607 0Ohm C2609 1UF/10V near AJ19 C2649 0.1UF/16V +VCCDSW_3P3 0.118A AD17 AD18 AJ17 VCCDSW_3p3_1 VCCDSW_3p3_2 VCCDSW_3p3_3
+3VSUS_ORG R26101 0Ohm +VCCPAZIO +VCCPSPI 0.068A AJ19 VCCHDA
+3VSUS_ORG R26111 0Ohm near V19 C2611 1UF/10V +1.0VSUS R2612 0Ohm +VCCFHV +VCCAPLLEBB_1P0 +VCCSRAM_1P0 0.011A AJ16 VCCSPI
C26101 2 1UF/10V near AF20 +VCCPRIM_3P3 0.642A AF20 AF21 T19 T20 VCCSRAM_1P0_1 VCCSRAM_1P0_2 VCCSRAM_1P0_3 VCCSRAM_1P0_4
0.075A AJ21 VCCPRIM_3p3_1
0.696A AK20 VCCPRIM_1P0_6
0.033A N18 VCCAPLLEBB_1P0
C2612 1UF/10V near N18

U0301O
CPU POWER 4 OF 4
940432
01V010000015

0.02A +VCCPGPPA 0.004A +VCCPGPPB 0.006A +VCCPGPPC 0.008A +VCCPGPPD 0.006A +VCCPGPPE 0.161A +VCCPGPPF 0.056A +VCCPGPPG
AK15 AG15 Y16 Y15 T16 AF16 AD15 VCCPGPPA VCCPGPPB VCCPGPPC VCCPGPPD VCCPGPPE VCCPGPPF VCCPGPPG
V19 0.075A VCCPRIM_3p3_2
T1 0.696A VCCPRIM_1P0_7
AA1 0.006A VCCATS_1p8
AK17 0.001A VCCRTCPRIM_3p3
AK19 BB14 VCCRTC_1 VCCRTC_2
BB10 VCCRTCEXT C2620 2 0.1UF/16V near BB10 DCPRTC
A14 0.035A VCCCLK1
K19 0.029A VCCCLK2
L21 0.024A VCCCLK3
N20 0.033A VCCCLK4
L19 0.004A VCCCLK5
A10 0.01A VCCCLK6
AN11 AN13 GPP_B0/CORE_VID0 GPP_B1/CORE_VID1
R2646 1KOhm R2647 1KOhm
Intel confirm pull down 1k

+3VSUS_ORG R2613 0Ohm
C26351 2 1UF/10V @ near AG15
C26131 2 1UF/10V @ near Y16
C26141 2 1UF/10V @ near T16
+1.8VSUS 0Ohm 2 1 R2620
+VCCPRIM_3P3 +VCCDTS_1P0 +V1.8A_SIP +VCCPRTCPRIM_3P3
+1.0VSUS R2623 0Ohm +1.8VSUS R2624 0Ohm C2615 1UF/10V near AA1
+3VSUS_ORG R2625 0Ohm C2618 1UF/10V near AK17 C2625 0.1UF/16V near AK17 C2617 0.1UF/16V near AK17
GND C26341 2 0.1UF/16V near AK19 +VCCPRTC_3P3 R2626 0Ohm C2619 2 1UF/10V +VCC_RTC GND near AK19
+VCC19P2_1P0 R2627 0Ohm +1.0VSUS
+VCCF100_1P0 R2628 0Ohm +1.0VSUS
+VCCF135_1P0 R2629 0Ohm +1.0VSUS
+VCCF100OC_1P0 R2630 0Ohm +1.0VSUS
+VCCF24NS_1P0 R2631 0Ohm +1.0VSUS
+VCC24TBT_1P0 R2632 0Ohm +1.0VSUS
near A10 C2624 1UF/10V @

R2636 2 0Ohm
+VCCDSW Q2601 SI2301CDS-T1-GE3 +VCCPDSW_3P3
Q2602 BC856BS @ R2635 100KOhm @
R2634 100KOhm @

2016.01.07
R1.2
Armani 2016 project for USB D+/D- short lesson learn solution (EC)

PEGATRON Title :PCH(7)_POWER
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BG1-NB4 Engineer: sinsian_Jheng
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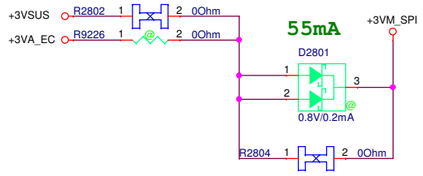
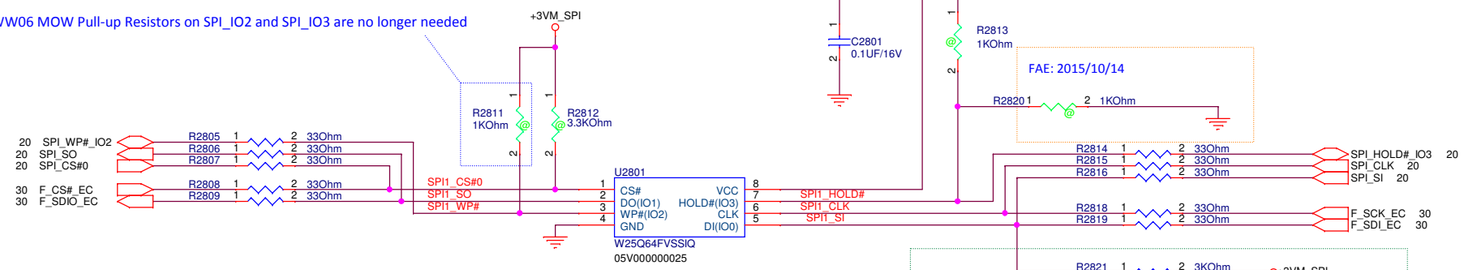
PCH(9)_SPI_SMB

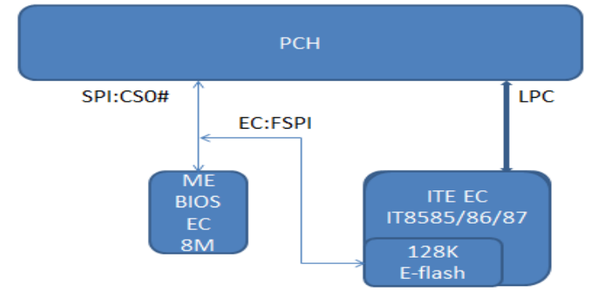
+3VS 3,4,18,20,21,22,23,24,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+12VS 31,48,57,91
+3VSUS 4,21,24,25,26,30,31,51,53,62,63,81,92
+3VA_EC 30,32
+12VSUS 81,91



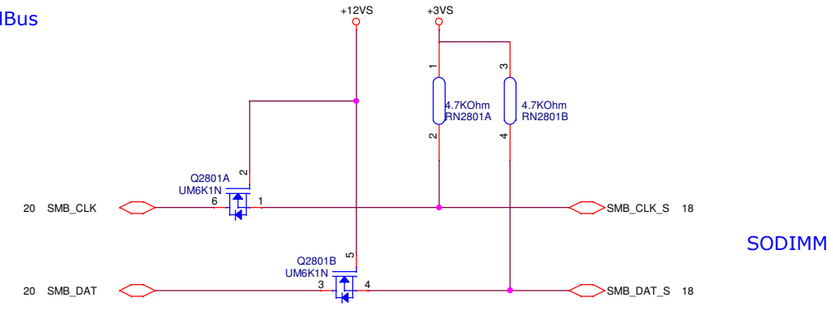
15WW06 MOW Pull-up Resistors on SPI_IO2 and SPI_IO3 are no longer needed

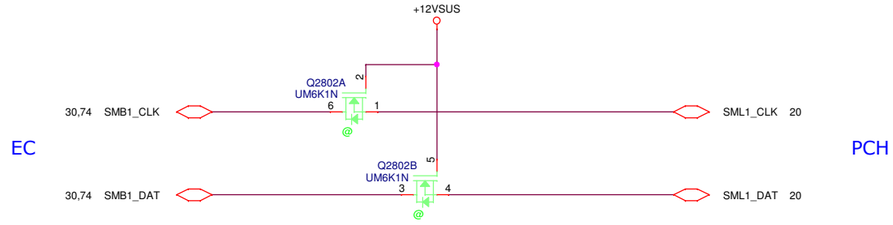


WW48MOW(ES Sample)
In Skylake Platform Design Guides (PDG) under "Platform Debug & Test Hooks" chapter, HOOK[3] pin from XDP/CMC header needs to be routed to PCH SPI0_MOSI pin. The termination resistor can be a value from 1K to 3K ohm pull up to Always rail (not Core rail) with voltage value from 0.8V to 3.3V. This will ensure PCH hardware straps are not overridden unintentionally and cause boot issues.



PCH SMBus





PEGATRON Title : PCH(9)_SPI_SMB
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4
Engineer: sinsian_Jheng
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EC_IT8587E/FX

+3VA_EC +3VA_EC 28,32
+3VS +3VS 3,4,18,20,21,22,23,24,28,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+3VSUS +3VSUS 4,21,24,25,26,28,31,51,53,62,63,81,92
+3VA +3VA 21,24,31,36,53,57,60,64,81,88,93
+1.8VSUS +1.8VSUS 9,26,84
+VCCDSW +VCCDSW 24,25,26

For EC Power

+3VA — 6mA — B3001 1 2 120Ohm/100Mhz — +3VA_EC
C3001 10UF/6.3V, C3002 0.1UF/16V, C3003 0.1UF/16V — GND
+3VS — C3006 0.1UF/16V — GND

+3VA_EC — C3004 10UF/6.3V — GND
SP3012 1 2 NB_R0402_20MIL_SMALL — +3VAPLL — C3005 0.1UF/16V — GND
For +3VPLL Nearby pin 127
SP3013 1 2 NB_R0402_20MIL_SMALL — +3VACC — C3007 0.1UF/16V
SP3011 1 2 NB_R0402_20MIL_SMALL — EC_AGND

IT8528, IT8587 Pin3 is VBAT, should pull down
IT8991 Pin 3 is GPH7, should NC

+3VA_EC — R3021 1 @ 2 0Ohm — R3022 1 2 0Ohm — GND — VBAT_PIN3 3 — VBAT

U3001

+3VAPLL — 127 VSTBY(PLL)
121 VSTBY5
114 VSTBY4
92 VSTBY3
50 VSTBY2
+3VA_EC — 26 VSTBY1

IT8528, IT8587 connect to +3VS
+3VACC — 74 AVCC
+3VS — R3023 1 2 0Ohm — EC_VCC — 11 VCC

20,44,62 LPC_AD0	SP3001	LAD0	10	LAD0/GPM0
20,44,62 LPC_AD1	SP3002	LAD1	9	LAD1/GPM1
20,44,62 LPC_AD2	SP3003	LAD2	8	LAD2/GPM2
20,44,62 LPC_AD3	SP3004	LAD3	7	LAD3/GPM3
20 CLK_KBCPCI_PCH	SP3005	CLK_KBCPCI_EC	13	LPCCLK/GPM4
20,44,62 LPC_FRAME#		LPC_FRAME#	6	LFRAME#/GPM5
25,32,53,62,70 BUF_PLT_RST#	R3026 0Ohm	PCRST#_EC	22	LPCRST#/GPD2
20,44,62 INT_SERIRQ		INT_SERIRQ	5	SERIRQ/GPM6
3,44 EXT_SMI#	SP3006	EXT_SMI#_EC	15	ECSMI#/GPD4
3 EXT_SCI#	SP3007	EXT_SCI#_EC	23	ECSCI#/GPD3
T3001		A20GATE	126	GA20/GPB5
20 RCIN#		RCIN#	4	KBRST#/GPB6
32 EC_RST#		EC_RST#	14	WRST#

31 KSI0	KSI0	58 KSI0/STB#
31 KSI1	KSI1	59 KSI1/AFD#
31 KSI2	KSI2	60 KSI2/INIT#
31 KSI3	KSI3	61 KSI3/SLIN#
31 KSI4	KSI4	62 KSI4
31 KSI5	KSI5	63 KSI5
31 KSI6	KSI6	64 KSI6
31 KSI7	KSI7	65 KSI7
31 KSO0	KSO0	36 KSO0/PD0
31 KSO1	KSO1	37 KSO1/PD1
31 KSO2	KSO2	38 KSO2/PD2
31 KSO3	KSO3	39 KSO3/PD3
31 KSO4	KSO4	40 KSO4/PD4
31 KSO5	KSO5	41 KSO5/PD5
31 KSO6	KSO6	42 KSO6/PD6
31 KSO7	KSO7	43 KSO7/PD7
31 KSO8	KSO8	44 KSO8/ACK#
31 KSO9	KSO9	45 KSO9/BUSY
31 KSO10	KSO10	46 KSO10/PE
31 KSO11	KSO11	51 KSO11/ERR#
31 KSO12	KSO12	52 KSO12/SLCT
31 KSO13	KSO13	53 KSO13
31 KSO14	KSO14	54 KSO14
31 KSO15	KSO15	55 KSO15

25 SUSWARN#/SUSPWRDNACK	R3029 @ 0Ohm		119	CRX0/GPC0
3 THRO_CPU		THRO_CPU	123	CTX0/TMA0/GPB2
88 BAT_LEARN		BAT_LEARN	85	PS2CLK0/TMB0/CEC/GPF0
53 WLAN_RST#_EC		WLAN_RST#_EC	86	PS2DAT0/TMB1/GPF1
25 PM_PWRBTN#		PM_PWRBTN#	87	PS2CLK1/DTR0#/GPF2
25 SUSACK#	R3072 @ 0Ohm, R3073 @ 0Ohm		88	PS2DAT1/RTS0#/GPF3
31 TP_PS2_CLK		TP_PS2_CLK	89	PS2CLK2/GPF4
31 TP_PS2_DAT		TP_PS2_DAT	90	PS2DAT2/GPF5
Battery / Charger 60,88 SMB0_CLK		SMB0_CLK	110	SMCLK0/GPB3
60,88 SMB0_DAT		SMB0_DAT	111	SMDAT0/GPB4
PCH/dGPU 28,74 SMB1_CLK		SMB1_CLK	115	SMCLK1/GPC1
28,74 SMB1_DAT		SMB1_DAT	116	SMDAT1/GPC2
3 H_PECI_EC		H_PECI_EC	117	SMCLK2/PECI/GPF6
45 LCD_BKLTEN_EC		LCD_BKLTEN_EC	118	SMDAT2/PECIRQT#/GPF7
T3027		CTL_FAN	81	DAC5/RIG0#/GPJ5
52,64 USBP01_EN		USBP01_EN	80	DAC4/DCD0#/GPJ4
52,81 USB_CPW_EN		USB_CPW_EN	79	DAC3/TACH1B/GPJ3
53 IOAC_EN		IOAC_EN	78	DAC2/TACH0B/GPJ2
64 VOL_DOWN#_EC		VOL_DOWN#_EC	77	GPJ1
64 VOL_UP#_EC		VOL_UP#_EC	76	TACH2/GPJ0
24 SW_RTCRST		SW_RTCRST	128	CK32K/GPJ6
22 PCH_FLASH_DESCRIPTOR		PCH_FLASH_DESCRIPTOR	2	CK32KE/GPJ7
28 F_CS#_EC		F_CS#_EC	101	FCSE#/GPG3
28 F_SCK_EC		F_SCK_EC	105	FSCK/GPG7
28 F_SDI_EC		F_SDI_EC	102	FMOSI/GPG4
28 F_SDIO_EC		F_SDIO_EC	103	FMISO/GPG5

C3008 10PF/50V @ — GND

IT8587E/FX
06V380000021

ADC0/GPI0	66 AD_IINP		AD_IINP 88
ADC1/GPI1	67 SUS_PWRGD		SUS_PWRGD 81,92
ADC2/GPI2	68 ALL_SYSTEM_PWRGD		ALL_SYSTEM_PWRGD 25,92
ADC3/GPI3	69 WCT_DET#		
ADC4/GPI4	70 WCT_PWRGD_EC		
ADC5/DCD1#/GPI5	71 USBPD_DET#		
ADC6/DSR1#/GPI6	72 WLAN_WAKE#		WLAN_WAKE# 53
ADC7/CTS1#/GPI7	73 AC_DET#		
PWM0/GPA0	24 PWR_BLUE_LED#		PWR_BLUE_LED# 64
PWM1/GPA1	25 CHG_BLUE_LED#		CHG_BLUE_LED# 64
PWM2/GPA2	28 CHG_ORG_LED#		CHG_ORG_LED# 64
PWM3/GPA3	29 PWR_ORG_LED#		PWR_ORG_LED# 64
PWM4/GPA4	30 FAN0_PWM		FAN0_PWM 50
PWM5/GPA5	31 FAN1_PWM		FAN1_PWM 50
PWM6/SSCK/GPA6	32 EC_SPKR		EC_SPKR 36
PWM7/RIG1#/GPA7	34 KEYBOARD_LED#		KEYBOARD_LED# 31
RXD/SIN0/GPB0	108 LID_SW#_GMR		LID_SW#_GMR 31,58,64
TXD/SOUT0/PB1	109 BT_ON/OFF#_EC		BT_ON/OFF#_EC 53
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7	112 PM_RSMRST#		PM_RSMRST# 25
KSO16/SMOSI/GPC3	56 KSO16		KSO16 31
TMRI0/GPC4	120 AC_IN_OC_EC	SP3008 1 2 AC_IN_OC	AC_IN_OC 74,88
KSO17/SMISO/GPC5	57 KSO17		KSO17 31
TMRI1/GPC6	124 BAT1_IN_OC#		BAT1_IN_OC# 93
PWUREQ#/BBO/SMCLK2ALT/GPC7	16 ME_AC_PRESENT		ME_AC_PRESENT 25
			PM_SUSB# 25,63
			PM_SUSC# 25,63
RI1#/GPD0	18 PM_SUSB#		
RI2#/GPD1	21 PM_SUSC#	R3067 /SEQS_EC 0Ohm	
GINT/CTS0#/GPD5	33 SYS_PWROK_EC_R	SP3010 2 SYS_PWROK_EC	SYS_PWROK 25,63
TACHOA/GPD6	47 FAN0_TACH		SYS_PWROK_EC 63
TACH1A/TMA1/GPD7	48 FAN1_TACH		FAN0_TACH 50
		SP3009 2 VSUS_ON	FAN1_TACH 50
		R3063 /SEQS_EC 0Ohm	VSUS_ON 81,82,84,93
	19 VSUS_ON_EC	R3064 /SYS_EC 0Ohm	SUSC_EC# 57,63,91
L80HLAT/BAO/GPE0	82 SUSC_EC#_EC	R3079 /BYPAS_EC 0Ohm	SUSB_EC# 57,63,91,92
EGAD/GPE1	83 SUSB_EC#_EC		DE_ALL_SYS_PGD_EC 63
EGCS#/GPE2	84 DE_ALL_SYS_PGD_EC_R	R3065 /SEQS_EC 0Ohm	DELAY_ALL_SYSTEM_PWRGD 25
EGCLK/GPE3	125	R3066 BYPAS_EC 0Ohm	CPU_VRON 80
PWRSW/GPE4	35 ILIM_SEL	R3034 2 0Ohm	DE_ALL_SYS_PGD_HW 63
RTS1#/GPE5	17 EC_PIN17		PWR_SW# 64
LPCPD#/GPE6	20 GPE7		ILIM_SEL 52
L80LLAT/GPE7	T3002		LID_SW#_BL 31,45,58,64
		R3048 2 0Ohm	
		R3049 2 0Ohm	
SSCE1#/GPG0	106 WLAN_ON_EC		WLAN_ON_EC 53
DTR1#/SBUSY/GPG1/ID7	107 TP_IRQ#_EC	R3076 @ 0Ohm	TP_IRQ# 21,31
SSCE0#/GPG2	100 TP_OFF#_EC		TP_OFF#_EC 31
DSR0#/GPG6	104 PTP_PWR_EN		PTP_PWR_EN 31
CLKRUN#/GPH0/ID0	93 PM_CLKRUN#		PM_CLKRUN# 20,62
CRX1/SIN1/SMCLK3/GPH1/ID1	94 CHGCB0		CHGCB0 52
CTX1/SOUT1/GPH2/SMDAT3/ID2	95 CHGCB1		CHGCB1 52
GPH3/ID3	96 CHG_R		CHG_R 13
GPH4/ID4	97 CHG_HI_R		CHG_HI_R 13
GPH5/ID5	98 MBBD_ID_EC		MBBD_ID_EC 21
GPH6/ID6	99 TypeC_charge_EN		TypeC_charge_EN 13

2016.02.03
R1.2
Support Type C charger function control by EC
Function request by 2016 customer BIOS spec

C3012 0.1UF/16V
VSS1 12, VCORE 27, VSS2 49, VSS3 91, VSS4 113, VSS5 122, VSS6, AVSS 75 — GND
EC_AGND

For PU / PD

+3VA_EC
R3001 1 2 100KOhm BAT1_IN_OC#
R3002 1 @ 2 10KOhm AC_IN_OC
R3078 1 @ 2 100KOhm TypeC_charge_EN

+3VA_EC
RN3001A 1 2 4.7KOhm SMB1_DAT
RN3001B 3 4 4.7KOhm SMB1_CLK
RN3001D 7 8 4.7KOhm SMB0_CLK
RN3001C 5 6 4.7KOhm SMB0_DAT

+3VA_EC
R3015 1 2 10KOhm PWR_SW#
R3074 1 2 10KOhm LID_SW#_BL
R3075 1 2 10KOhm LID_SW#_GMR
R3039 1 2 10KOhm AC_DET#
R3040 1 @ 2 10KOhm USBPD_DET#
R3041 1 @ 2 10KOhm WCT_DET#

150416 Multi Power detect OD source

+3VS
R3017 1 @ 2 10KOhm A20GATE
R3018 1 2 10KOhm RCIN#
R3019 1 2 10KOhm FAN0_TACH
R3035 1 2 10KOhm FAN1_TACH
R3009 1 2 10KOhm VOL_DOWN#_EC
R3016 1 2 10KOhm VOL_UP#_EC

RN3003A 1 /SEQS_EC 2 4.7KOhm SUSC_EC#
RN3003B 3 /SEQS_EC 4 4.7KOhm SUSB_EC#
GND

Reserved for IT8587E/FX

AD_IINP	R3055	1 @ 2	0Ohm
SUS_PWRGD	R3056	1 @ 2	0Ohm
ALL_SYSTEM_PWRGD	R3057	1 @ 2	0Ohm
WCT_DET#	R3058	1 @ 2	0Ohm
WCT_PWRGD_EC	R3059	1 @ 2	100KOhm
USBPD_DET#	R3060	1 @ 2	0Ohm
WLAN_WAKE#	R3061	1 @ 2	0Ohm
AC_DET#	R3062	1 @ 2	0Ohm

GND

PM_SUSB# R3003 1 2 100KOhm
PM_SUSC# R3004 1 2 100KOhm
150416Remove Pull-D 100K to SLPSUS
PM_RSMRST# R3006 1 2 10KOhm
150416Remove Pull-D 10K to PCH_DPWRK_DSW
BAT1_IN_OC# R3050 1 @ 2 100KOhm
TypeC_charge_EN R3077 1 @ 2 100KOhm
GND

141112 Remove Pull-D 10K to F_SDI_EC
(F Version problem has be solved)
TP_OFF#_EC R3010 1 @ 2 10KOhm — GND
+3VA_EC — R3011 1 2 10KOhm VSUS_ON
R3012 1 2 10KOhm TP_OFF#_EC
+3VSUS — R3013 1 @ 2 100KOhm VSUS_ON

PEGATRON Title : EC_IT8587E/FX
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 30 of 96

N/A

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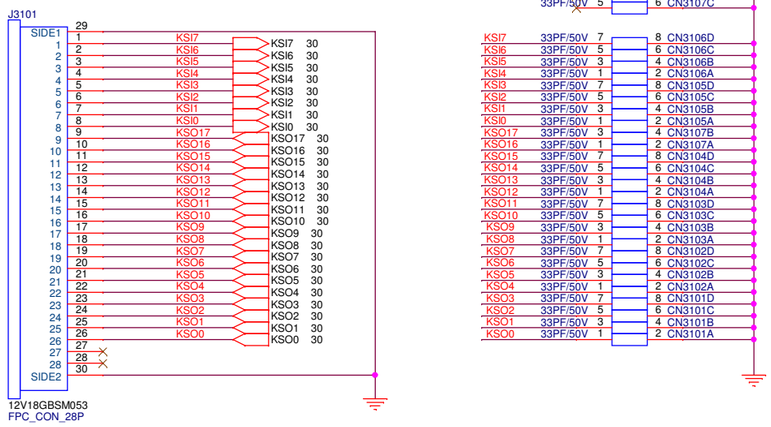
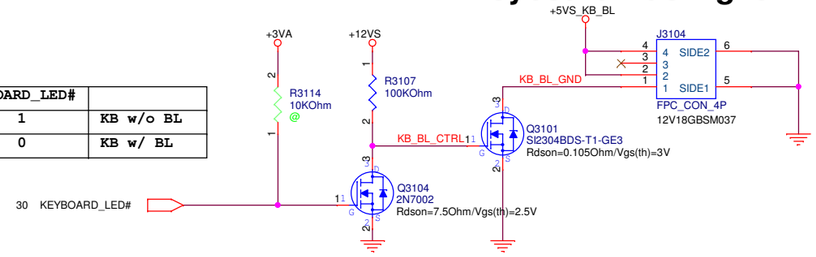
KB_TP

Keyboard



+3VS +3VS 3,4,18,20,21,22,23,24,28,30,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+3VSUS +3VSUS 4,21,24,25,26,28,30,51,53,62,63,81,92
+3V +3V 57,58,64,91
+3VA +3VA 21,24,30,36,53,57,60,64,81,88,93
+12VS +12VS 28,48,57,91
+5VS +5VS 36,45,48,50,51,57,80,87,91

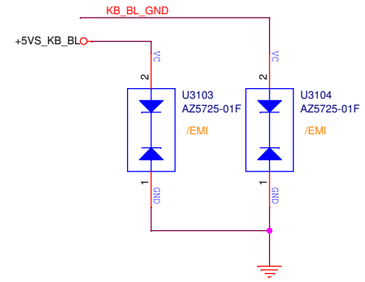
Keyboard Backlight



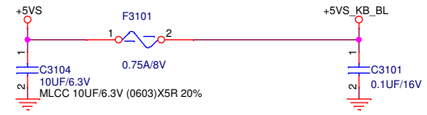
KEYBOARD_LED#	
1	KB w/o BL
0	KB w/ BL

2015.11.24
R1.1
Remove P1-VCC

2015.12.07
R1.1
EMI Unmount

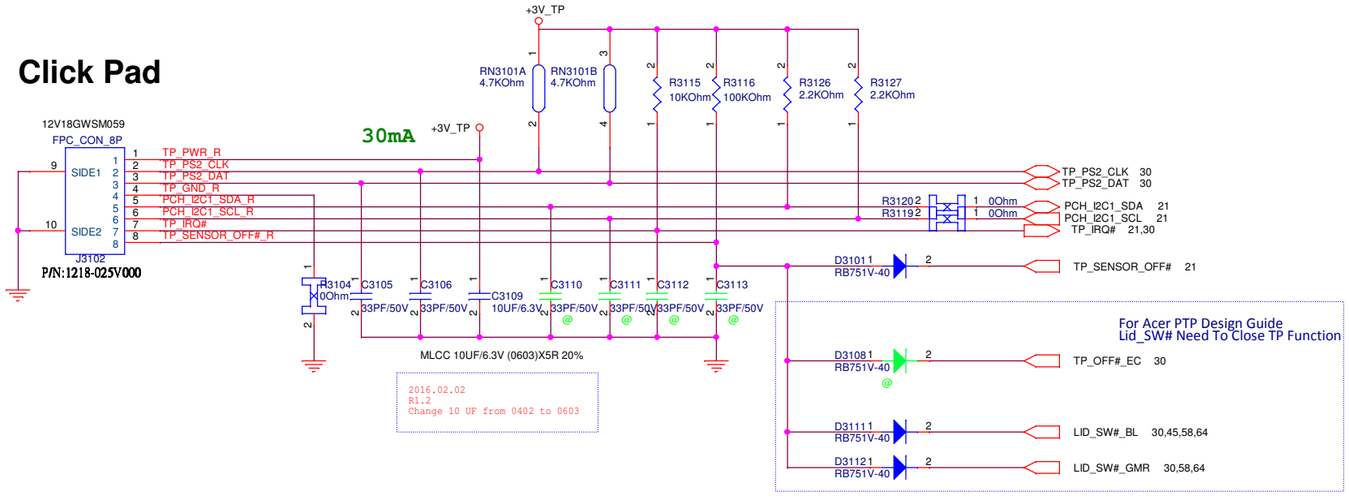


+5VS_KB_BL trace >20mils



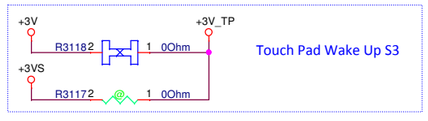
2016.02.02
R1.2
Change 10 UF from 0805 to 0603

Click Pad

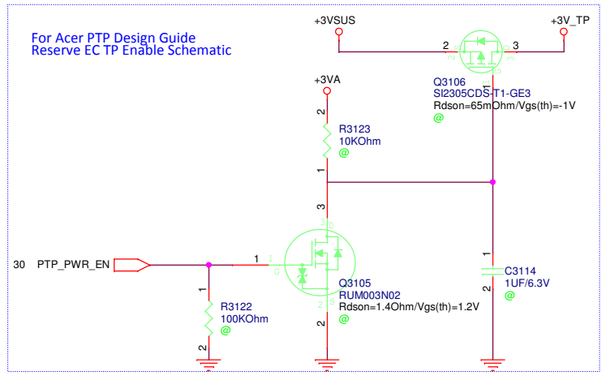


2016.02.02
R1.2
Change 10 UF from 0402 to 0603

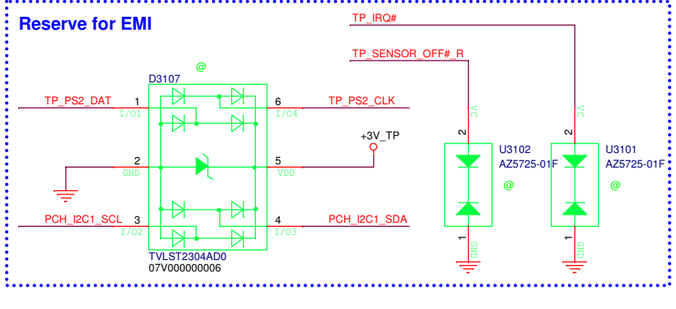
For Acer PTP Design Guide
Lid_SW# Need To Close TP Function



For Acer PTP Design Guide
Reserve EC TP Enable Schematic



Reserve for EMI



PEGATRON	Title :	KB_TP	
BG1-NB4	Engineer:	sinsian_Jheng	
Size: C	Project Name: P5HCJ/Megatron		Rev: 1.2
Date: Friday, February 05, 2016	Sheet 31 of 96		

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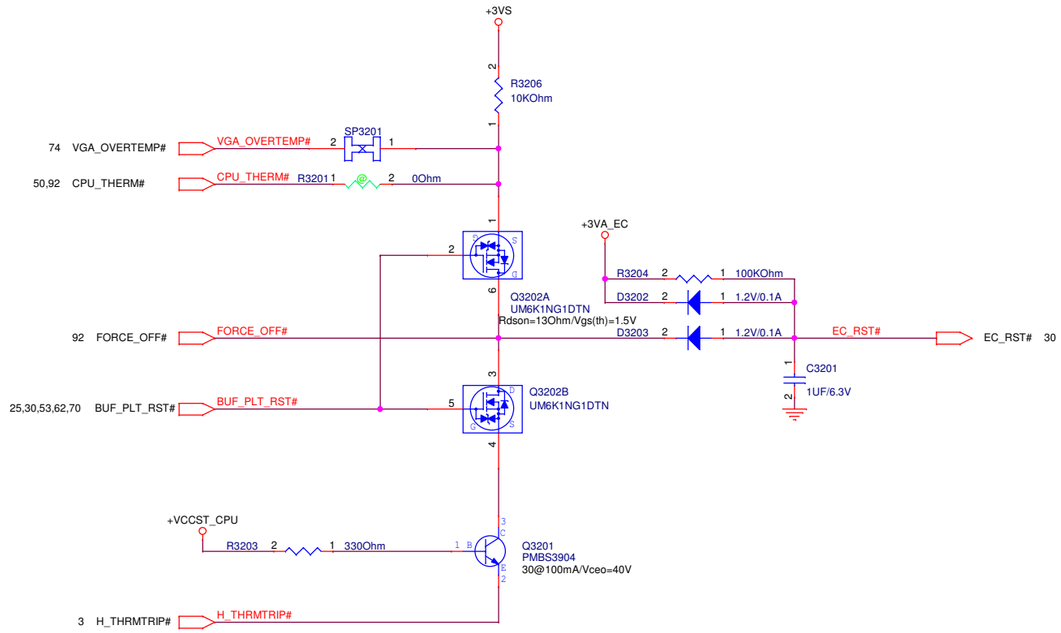
RST_Reset Circuit

+VCCST_CPU — +VCCST_CPU 3,5,7,9,25
+3VA_EC — +3VA_EC 28,30
+3VS — +3VS 3,4,18,20,21,22,23,24,28,30,31,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92



PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : RST_Reset Circuit

BG1-NB4

Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 32 of 96

AUD_ALC255

+1.8VS → +1.8VS 21,57,91
+3VS → +3VS 3,4,18,20,21,22,23,24,28,30,31,32,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+5VS → +5VS 31,45,48,50,51,57,80,87,91

Analog
Digital

+1.8VS — L3601 1 2 120Ohm/100Mhz — C3612 10UF/6.3V
+5VS_PVDD_AVD — C3611 10UF/6.3V

U3601A ALC255-CG

AC_HP_R → AC_HP_R 37
AC_HP_L → AC_HP_L 37
LINE1_VREFO_L → LINE1_VREFO_L 37
LINE1_VREFO_R → LINE1_VREFO_R 37
MIC2_VREFO → MIC2_VREFO 37

+3VS_AUDIO — C3638 10UF/6.3V — C3617 1UF/6.3V — C3616 1UF/6.3V — C3615 2.2UF/6.3V — C3609 10UF/6.3V — R3635 100KOhm
+5VS_AUDIO — C3604 0.1UF/16V — C3637 10UF/6.3V
Place close to Pin 26

CPVDD CBN CPVEE HPOUT-R(PORT-I-R) HPOUT-L(PORT-I-L) LINE1-VREFO-L LINE1-VREFO-R MIC2-VREFO VREF LDO1-CAP AVDD1 AVSS1

CBP AVSS2 LDO2-CAP AVDD2 PVDD1 SPK-OUT-L+ SPK-OUT-L- SPK-OUT-R- SPK-OUT-R+ PVDD2 PDB SPDIF-OUT/GPIO2 GND

37 H_SPKL+ — H_SPKL+ 42
37 H_SPKL- — H_SPKL- 43
37 H_SPKR- — H_SPKR- 44
37 H_SPKR+ — H_SPKR+ 45
PDB 47

LINE2-L(PORT-E-L) LINE2-R(PORT-E-R) LINE1-L(PORT-C-L) LINE1-R(PORT-C-R) VD33_STB MIC_CAP MIC2-R(PORT-F-R)/SLEEVE MIC2-L(PORT-F-L)/RING MONO-OUT SPDIFO/FRONT_JD(JD3)/GPIO3 MIC2/LINE2_JD(JD2) HP/LINE1_JD(JD1)

LINE1_L — LINE1_L 37
LINE1_R — LINE1_R 37
C3614 10UF/6.3V
SLEEVE — SLEEVE 37
RING2 — RING2 37
R3604 100KOhm — R3603 200KOhm — HP_JD# 37
+3VS_AUDIO
GND_AUDIO

+3VA — R3637 0Ohm
Digital
Analog

PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

Place close audio codec

DVDD GPIO0/DMIC-DATA GPIO1/DMIC-CLK DC_DET SDATA-OUT BCLK SYNC LDO3-CAP SDATA-IN DVDD-IO SYNC RESETB PCBEEP

+3VS_AUDIO — C3605 10UF/6.3V — C3606 0.1UF/16V
Place close to pin 1

Analog
Digital

PC_BEEP
HDA_RST# 22
HDA_SYNC 22
HDA_SDI0 22
HDA_BCLK 22
HDA_SDO 22

+3VS_AUDIO — C3607 10UF/6.3V — C3608 0.1UF/16V
R3621 22Ohm
R3620 22Ohm
C3613 22PF/50V
MLCC 22PF/50V (0402) NPO 5%
C3618 0.1UF/16V — C3625 10UF/6.3V

64 DMIC_DAT_P4 — DMIC_DAT_P4 — R3614 0Ohm
64 DMIC_CLK_P4 — DMIC_CLK_P4 — R3615 22Ohm
C3629 33PF/50V — C3624 33PF/50V

2016.02.04
R1.2
EMC/Ricky changes 10 pF to 33 pF

2016.02.02
R1.2
Change 22 pF from 0201 to 0402

+3VS_AUDIO — R3650 0Ohm — D3601 1V/0.1A — R3652 1KOhm — R3651 10KOhm — C3639 1UF/6.3V — PDB
21 OP_SD# → D3601
HDA_RST# → D3601
30 OP_SD#_EC — D3604 RB751V-40

PC_BEEP — C3602 0.1UF/16V — PCBEEP — R3605 22KOhm — C3626 100PF/50V — R3618 4.7KOhm
R3638 0Ohm — D3603 1V/0.2A — HDA_SPKR 22
R3639 0Ohm — EC_SPKR 30

U3601B
50 GND1
51 GND2
52 GND3
53 GND4
ALC255-CG
02V0J0000065

+3VS — R3636 5mA — +3VS_AUDIO

1.05A
+5VS — Digital — Analog — +5VS_AUDIO
VC
L3603 120Ohm/100Mhz
D3602 AZ5725-01F /EMI
GND
Moat
C3628 10UF/6.3V — GND_AUDIO

In order to prevent the built-in LDO damaged from over-voltage on +5VSYS or Standby power line, we suggested using this Voltage suppressing device.

2015.12.07
R1.1
EMI build confirm

Add this Filter to avoid other components/chips be influenced

+5VS — L3602 600Ohm/100Mhz — +5VS_PVDD_AVD
C3622 0.1UF/16V — C3623 10UF/6.3V
C3619 10UF/6.3V — C3601 0.1UF/16V
Close PIN 41
C3620 10UF/6.3V — C3603 0.1UF/16V
Close PIN 46

<<Attention>>
For power_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :
1. If you want the system make warning signal after power on , please let EC_MUTE# High.
2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

Grounding circuit for combo jack SLEEVE pin

+3VS_AUDIO — R3634 100KOhm — Q3601 2N7002 — SLEEVE
+VCC_RTC — R3633 100KOhm — Q3603 2N7002 — GND_AUDIO
+3VA — R3631 100KOhm — Q3602 2N7002 — RING2 — GND_AUDIO
HDA_RST# — R3619 0Ohm — C3627 1UF/6.3V

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

2015.09.10 Edison
EMI 建議Audio moat 預留TVS

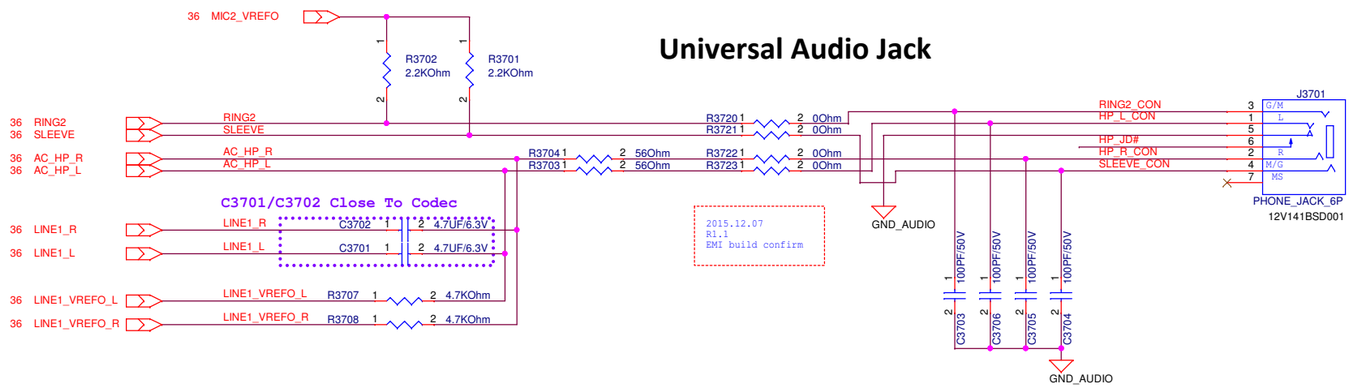
U3602 AZ5725-01F 07V180000029 /EMI
GND 1 — 2 VC
R3625 0Ohm
R3624 0Ohm
R3623 0Ohm
C3635 100PF/50V
R3622 0Ohm
C3633 1000PF/50V
C3634 1000PF/50V
GND — GND_AUDIO

2015.12.07
R1.1
EMI B build confirm

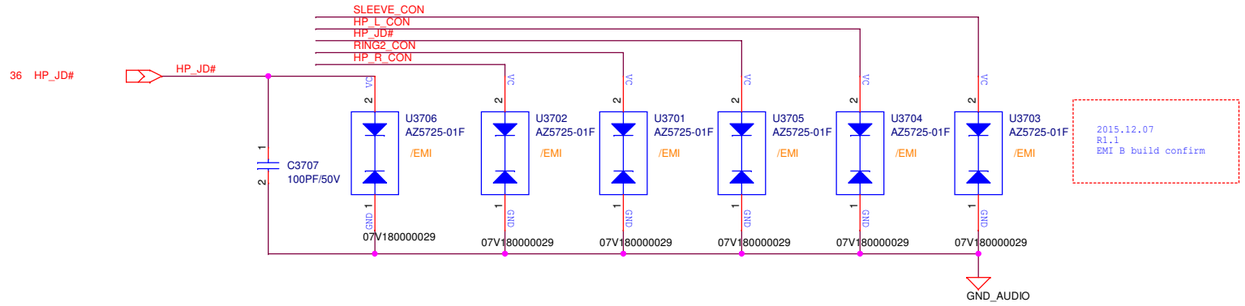
PEGATRON	Title : AUD_ALC255	
BG1-NB4	Engineer: sinsian_Jheng	
Size: C	Project Name: P5HCJ/Megatron	Rev: 1.2
Date: Friday, February 05, 2016	Sheet 36 of 96	

AUD_HP/DMIC/SPK

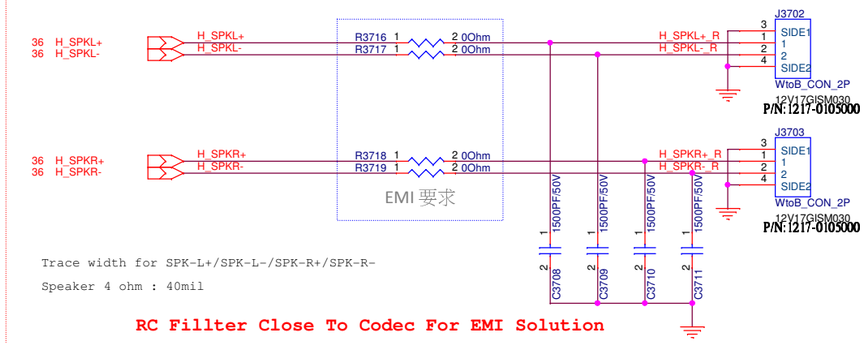
Universal Audio Jack



2015.04.08 YenPin
EMI 建議料號07V180000029
HP_JD# 請同樣預留bypass電容



Internal Speaker



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-

Speaker 4 ohm : 40mil

RC Fillter Close To Codec For EMI Solution

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4

Title : AUD_HP/DMIC/SPK

Engineer: sinsian_Jheng

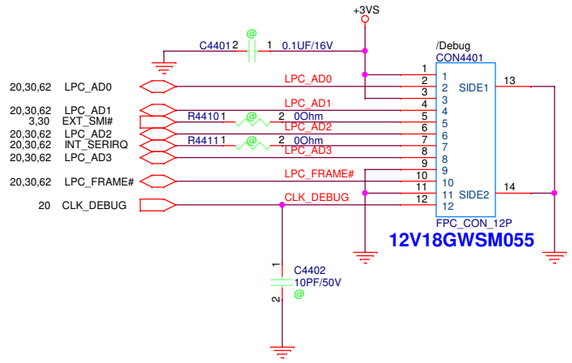
Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 37 of 96

44

DEBUG CONN

+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,45,48,50,51,53,54,57,58,59,62,64,91,92



PEGATRON Title : DEBUG CONN.

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

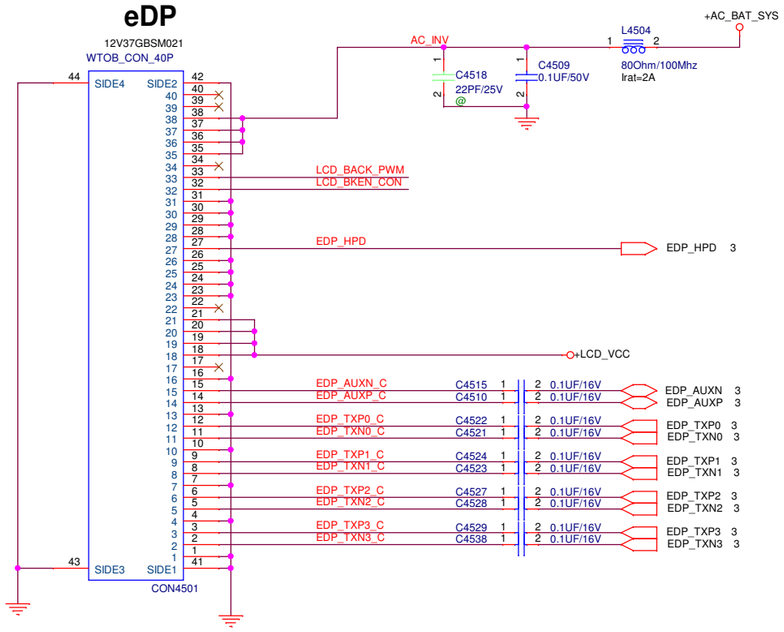
Date: Friday, February 05, 2016 Sheet 44 of 96

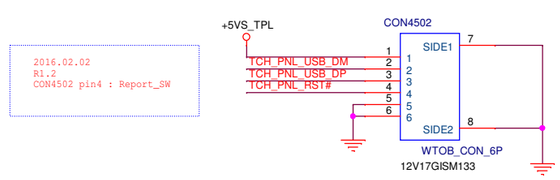
45

Panel_EDP_Touch

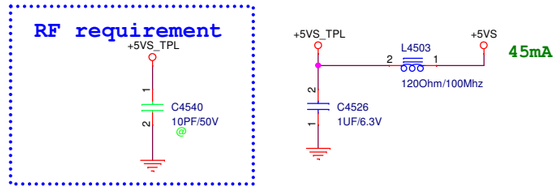
+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,48,50,51,53,54,57,58,59,62,64,91,92
+5VS +5VS 31,36,48,50,51,57,80,87,91
+AC_BAT_SYS +AC_BAT_SYS 80,81,82,83,87,88,89

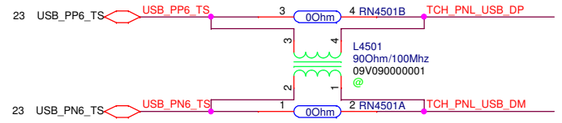
eDP

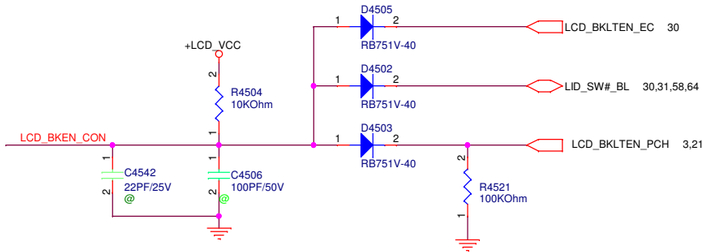


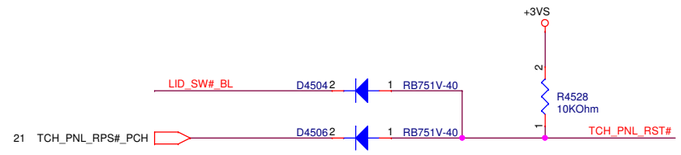


Touch

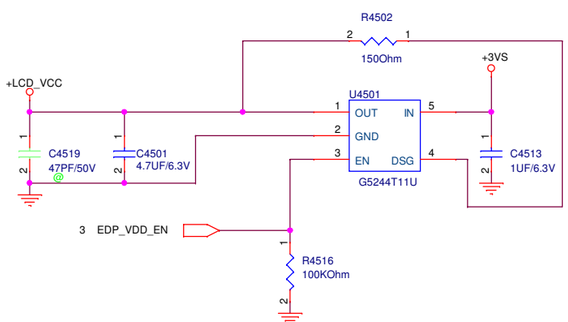


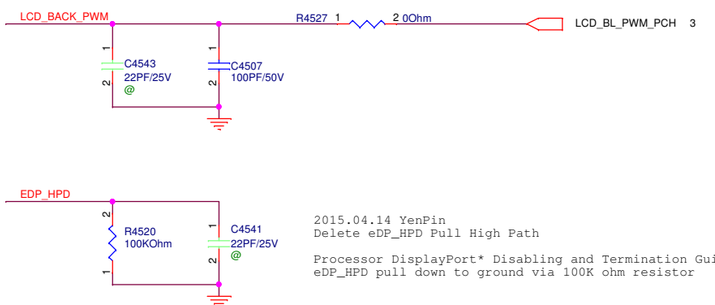






LCD_VCC

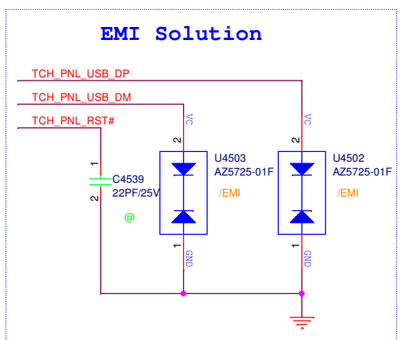




2015.04.14 YenPin
Delete eDP_HPD Pull High Path

Processor DisplayPort* Disabling and Termination Guidelines Checklist
eDP_HPD pull down to ground via 100K ohm resistor

2015.12.07
R1.1
EMI Unmount



PEGATRON Title : Panel_EDP_Touch
BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 45 of 96

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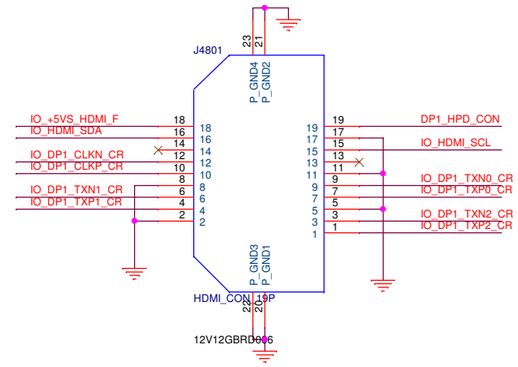
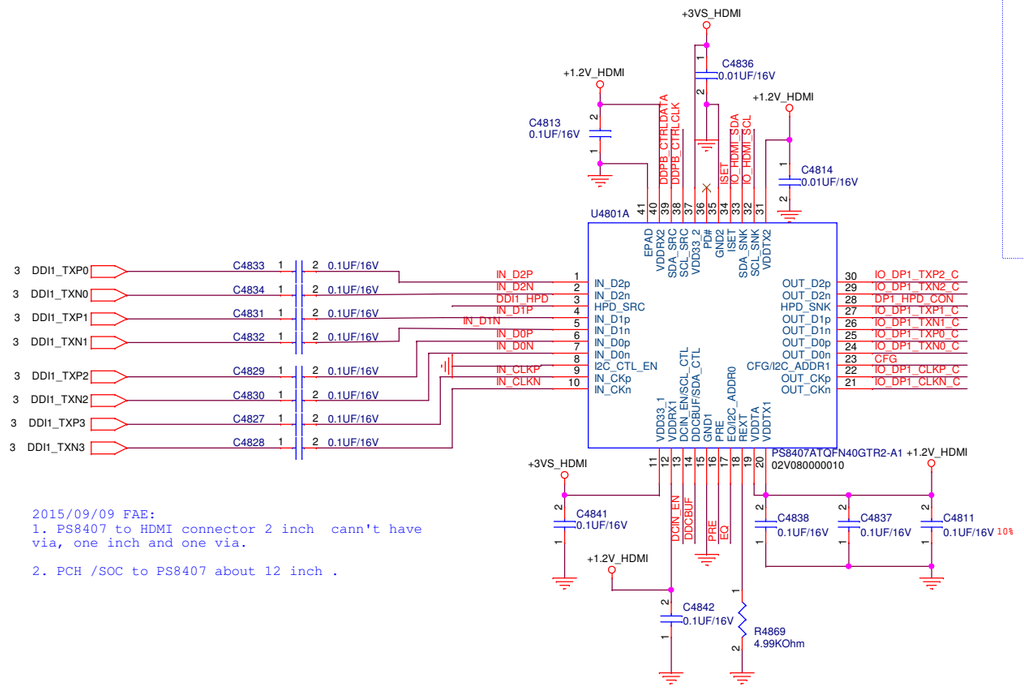
HDMI_4K2K

+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,50,51,53,54,57,58,59,62,64,91,92
+5VS +5VS 31,36,45,50,51,57,80,87,91
+12VS +12VS 28,31,57,91



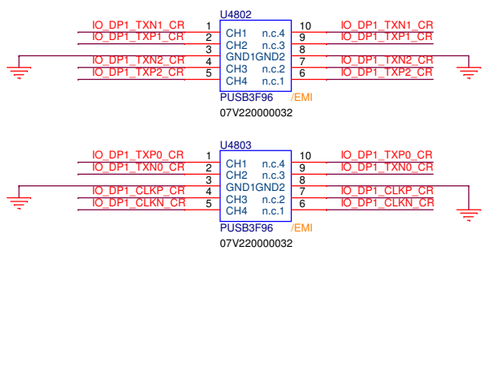


2015/09/09 FAE:
1. PS8407 to HDMI connector 2 inch cann't have via, one inch and one via.

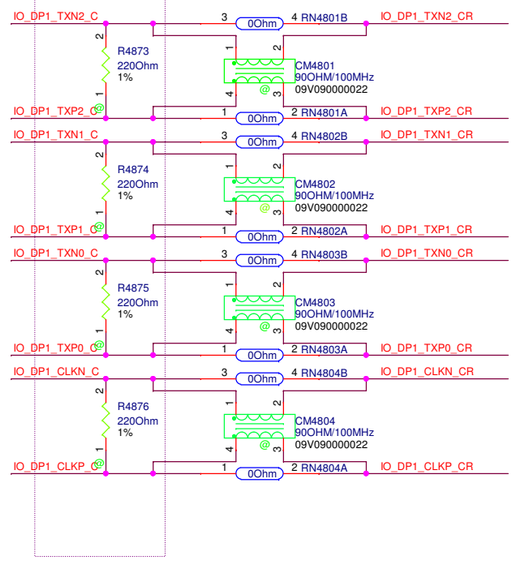
2. PCH /SOC to PS8407 about 12 inch .

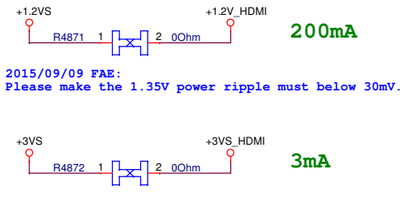
EMI 2015/12/04

2015.12.07
R1.1
EMI Unmount



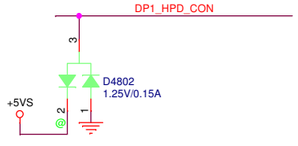
EMI 2015/10/08



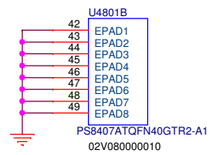


2015/09/09 FAE:
Please make the 1.35V power ripple must below 30mV.

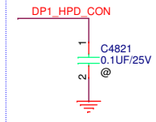
3.3V tolerent to HPD

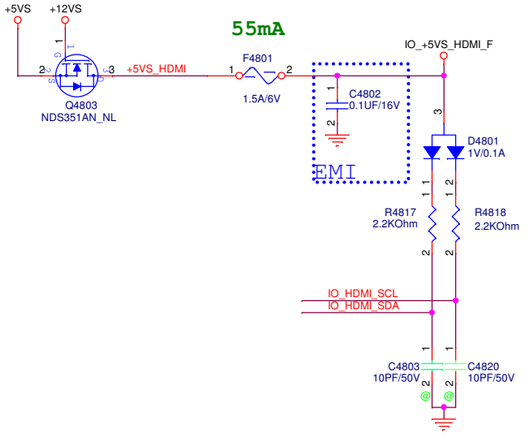


Vendor Suggestion
pin 28 : PS8408/ PS8201 have internal pull down resister, reserve D4802

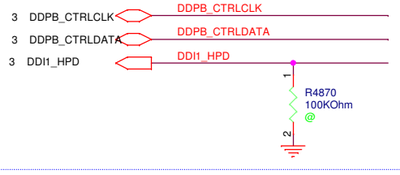


EMI 2015/10/12

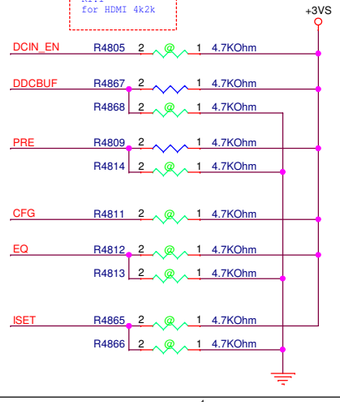




2015/09/09 FAE:
1. Pin 3: PS8407 have internal pull down resister, so you can remove R4870.



2015.12.04
R1.1
for HDMI 4k2k



DCIN_EN	PD
DDCBUF	PU
PRE	PU
CFG	PD
EQ	PD
ISET	PD

DCIN_EN : DC cou;ing enable; Internal pull down at ~150k文, 3.3V I/O.
L: default, AC coupling input
H: DC coupling input
DDCBUF : Enable active DDC buffer; Internal pull down at ~150K文, 3.3V I/O
L: default, passive DDC pass-through
H: active DDC buffer with default threshold
M: active DDC buffer without internal pull up resistor
PRE : Output pre-emphasis setting; Internal pull down at ~150k文, 3.3V I/O.
L: no pre-emphasis
H: 1.6dB pre-emphasis
M: 2.5dB pre-emphasis
CFG : Configuration pin, 3.3V IO, internal pull down at ~150k文. 3.3V I/O.
L: HDMI ID disable
H: HDMI ID enable
EQ : Receiver equalization setting; Internal pull down at ~150k文, 3.3V I/O.
L: programmable EQ for channel loss up to 6.5dB @ 3Gbps
H: programmable EQ for channel loss up to 9.5dB @ 3Gbps
M: programmable EQ for channel loss up to 3dB @ 3Gbps
ISET : TMDS output swing adjustment; Internal pull down at ~150k文, 3.3V I/O.
L: default
H: increase +13%
M: reduce -13%

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : HDMI_4K2K

BG1-NB4

Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 48 of 96

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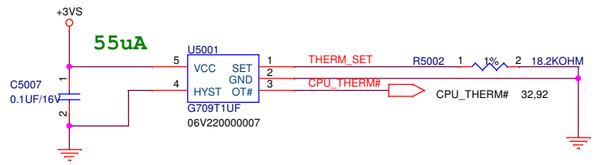
Thermal_Fan

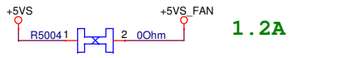
+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,51,53,54,57,58,59,62,64,91,92

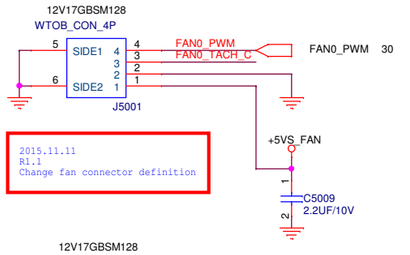
+5VS +5VS 31,36,45,48,51,57,80,87,91

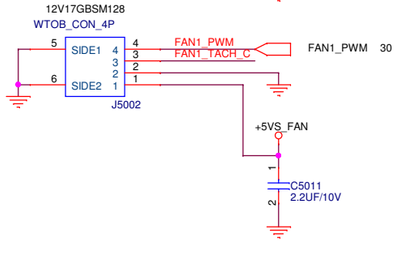
G709Thermal Sensor

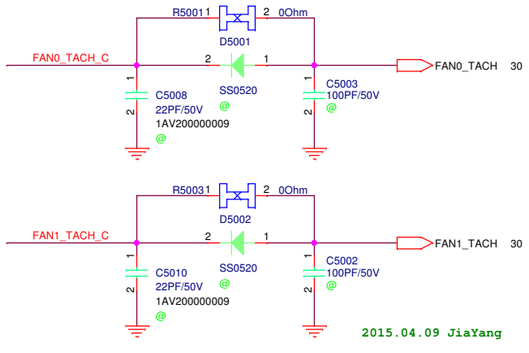


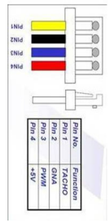
PWM FAN

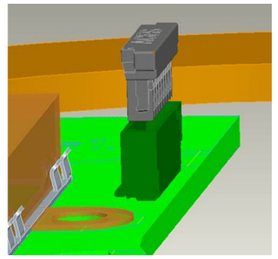












PEGATRON	Title : Thermal_Fan	
BG1-NB4	Engineer: sinsian_Jheng	
Size: C	Project Name: P5HCJ/Megatron	Rev: 1.2
Date: Friday, February 05, 2016	Sheet 50 of 96	

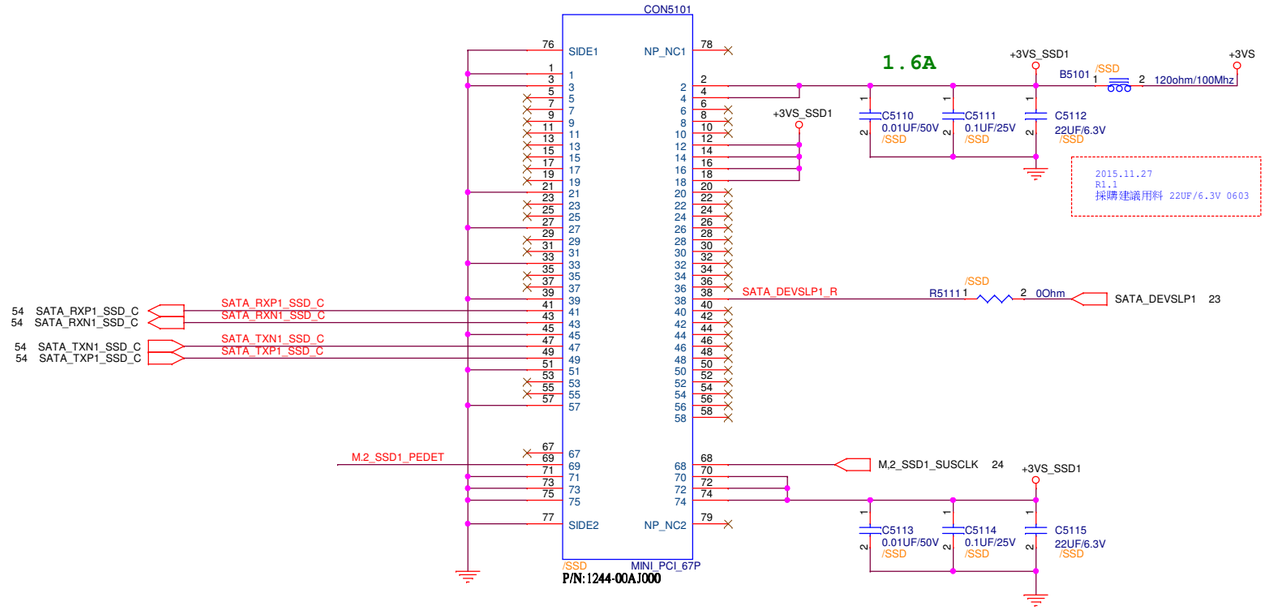
51 NGFF socket B -- SSD (Main)

SATA SSD_HDD

2015.12.10
R1.1
Remove +5VS_HDD

2015.11.12
R1.1
Support PCIE_SSD

2016.01.21
R1.2
Remove PCIE_SSD



PCIe_M.2_Electromechanical_Spec_Rev_0.9-3_07312013_RS_Clean

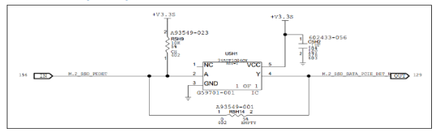
Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75)	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

36.3.2.3 PEDET Guidelines

PEDET is the interface detect used by PCH to determine the communication protocol that the M.2 card uses; PCIe* signaling (high) or SATA signaling (low) in conjunction with a platform located pull-up resistor.

Figure 36-6. PEDET Circuitry Example



For Skylake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the interface detect signaling from the M.2 device.

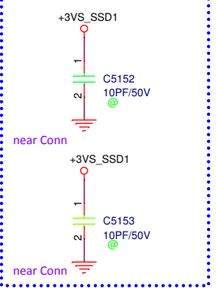
8.1.2 Pin Assignment

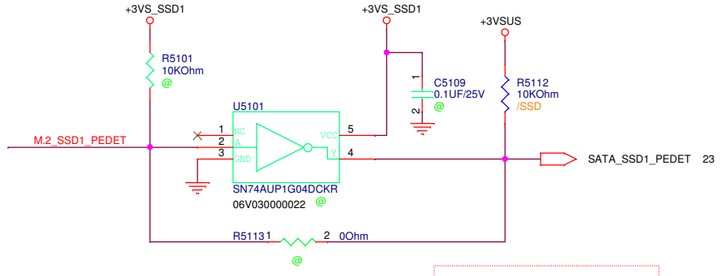
The following table describes all pins on the Edge Card connection.

Table 8-1 Pin Assignment

Pin #	Name	Description	Pin #	Name	Description
1	CONFIG_3	Defines module type(low)	2	+3.3V	3.3V Source
3	GND	GND	4	+3.3V	3.3V Source
5	Reserved	NC	6	Reserved	NC
7	Reserved	NC	8	Reserved	NC
9	Reserved	NC	10	DAS/DSS	Drive Activity Signal /
11	Reserved	NC			
Notch			Notch		
			20	Reserved	NC
21	CONFIG_0	Defines module type(low)	22	Reserved	NC
23	Reserved	NC	24	Reserved	NC
25	Reserved	NC	26	Reserved	NC
27	GND	GND	28	Reserved	NC
29	Reserved	NC	30	Reserved	NC
31	Reserved	NC	32	Reserved	NC
33	GND	GND	34	Reserved	NC
35	Reserved	NC	36	Reserved	NC
37	Reserved	NC	38	DEVSLP	DEVSLP signal
39	GND	GND	40	Reserved	NC
41	B+	Host Receiver Differential Signal Pair	42	Reserved	NC
43	B-		44	Reserved	NC
45	GND	GND	46	Reserved	NC
47	A-	Host Transmitter Differential Signal Pair	48	Reserved	NC
49	A+		50	Reserved	NC
51	GND	GND	52	Reserved	NC
53	Reserved	NC	54	Reserved	NC
55	Reserved	NC	56	MFG1	Manufacturing pin. Must be a no-connect on the host board.
57	GND	GND	58	MFG2	
Notch			Notch		
67	Reserved	NC	68	Reserved	NC
69	CONFIG_1	Defines module type(low)	70	+3.3V	3.3V Source
71	GND	GND	72	+3.3V	3.3V Source
73	GND	GND	74	+3.3V	3.3V Source
75	CONFIG_2	Defines module type(low)			

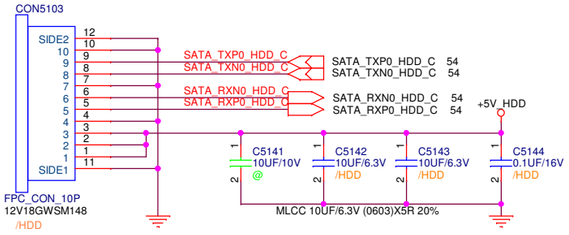
RF requirement

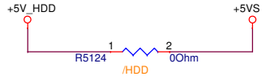




2016.01.07
R1.2
Revise the configuration for SSD

HDD





2016.02.02
R1.2
Change 10 UF from 0805 to 0603

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4

Title : SATA SSD_HDD
Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 51 of 96

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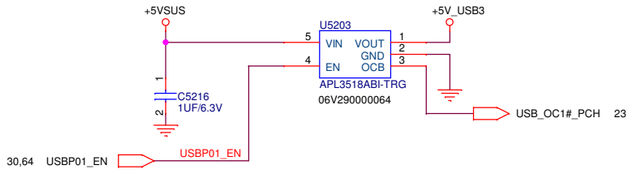
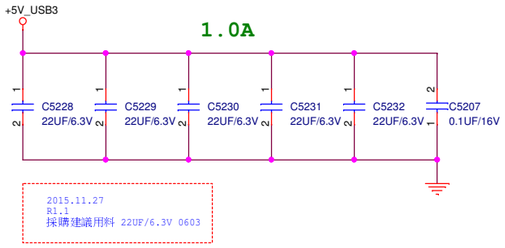
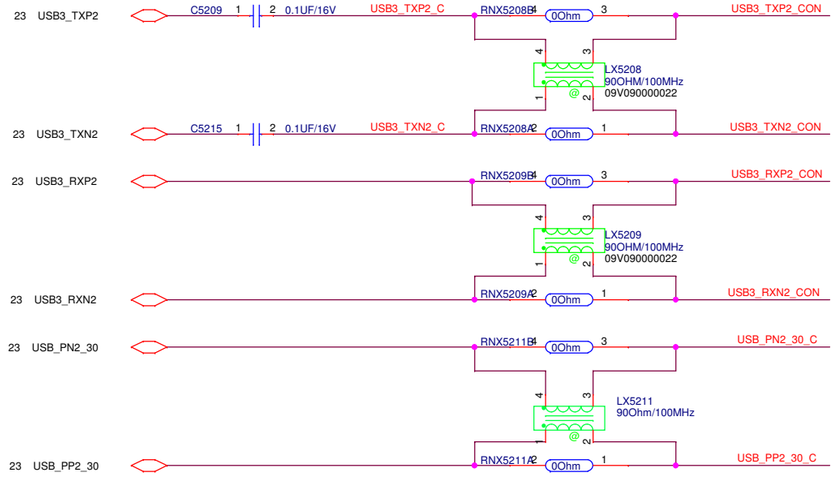
USB3.0_Charge IC

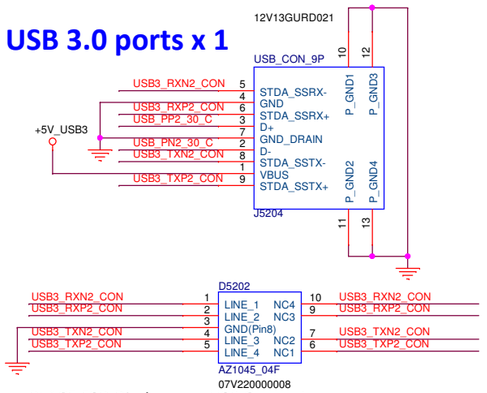
+5VSUS → +5VSUS 13,64,81



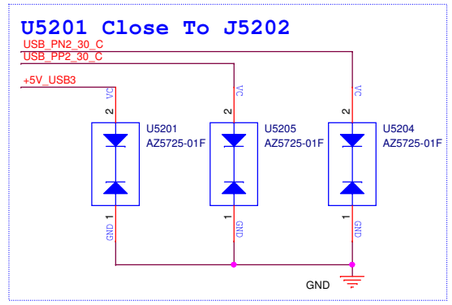




USB 3.0 ports x 1



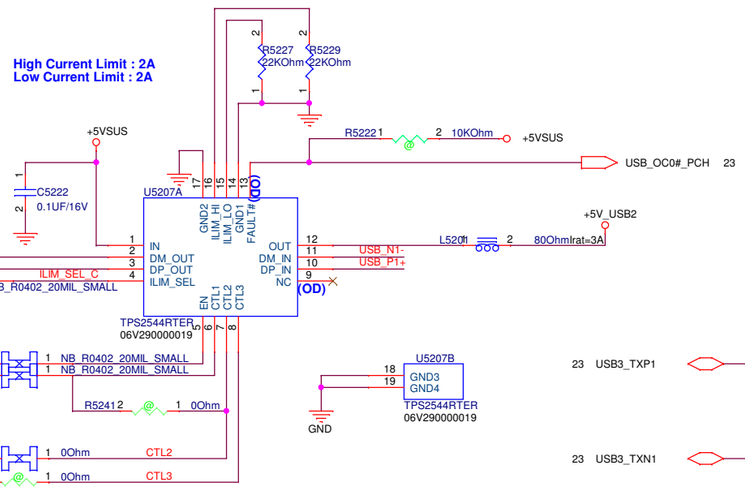
PLACE ESD Diodes near USB Connector

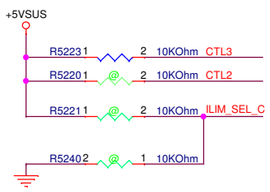


USB 3.0 ports x 1 with Sleep & Charge Left_Down

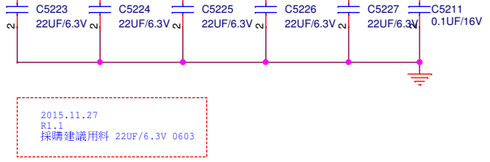
Device	Pega No.	VX No.
TPS2544RTER	0629-00CU000	06V290000019 (Default)

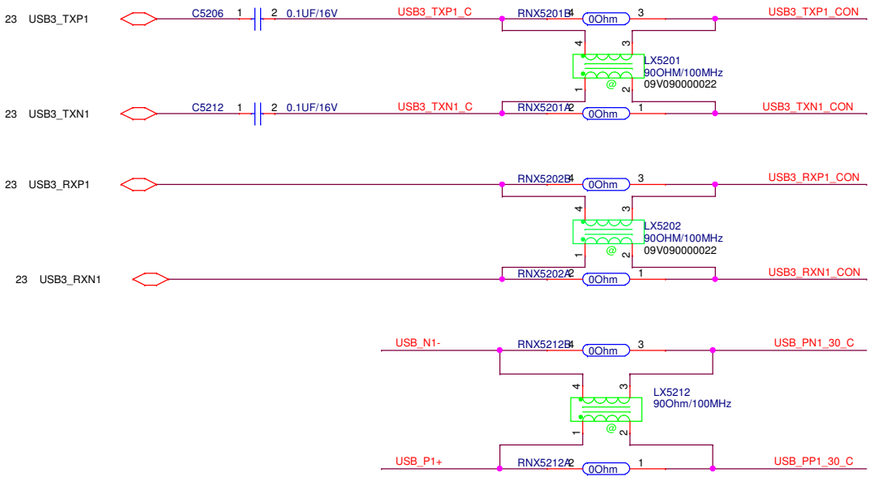
High Current Limit : 2A
Low Current Limit : 2A



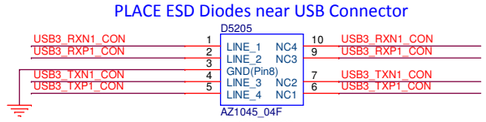


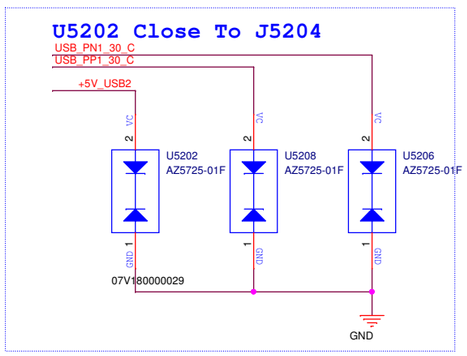
System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

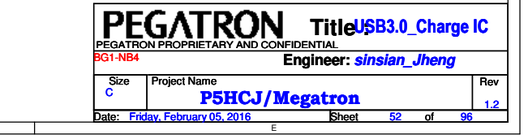




PLACE ESD Diodes near USB Connector







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4

Title: USB3.0_Charge IC
Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 52 of 96

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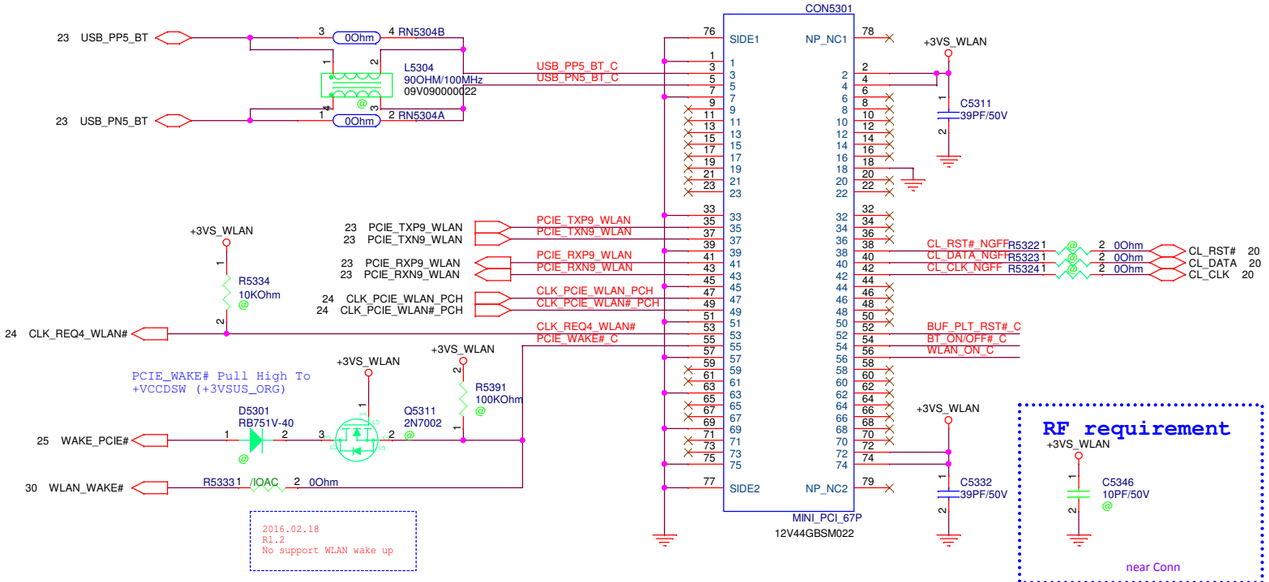
PCIE_WLAN_BT

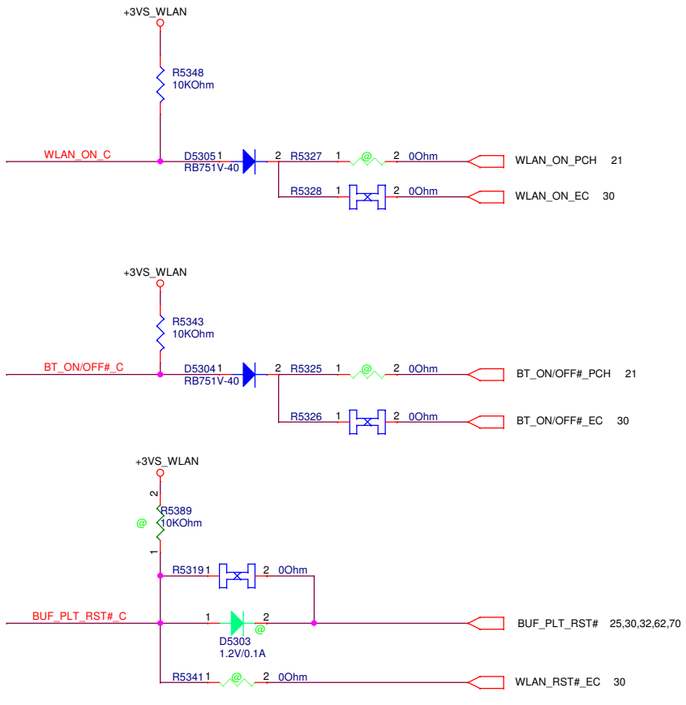
+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,54,57,58,59,62,64,91,92

+3VSUS +3VSUS 4,21,24,25,26,28,30,31,51,62,63,81,92

+3VA +3VA 21,24,30,31,36,57,60,64,81,88,93



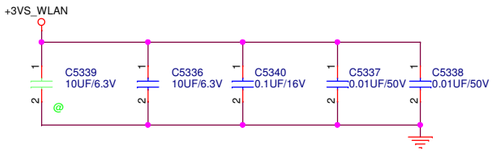
WLAN/BT with NGFF socket E



+3V_WLAN_WP1 bypass capactor:

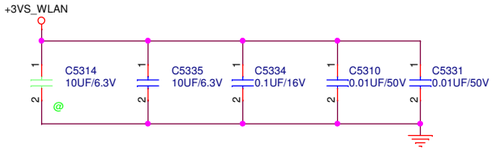
Place 0.1UF near pin 2,4

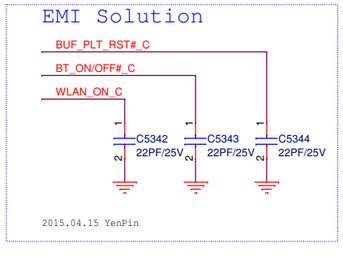
Place 10UF near +3V_WLAN_WP1 source side.

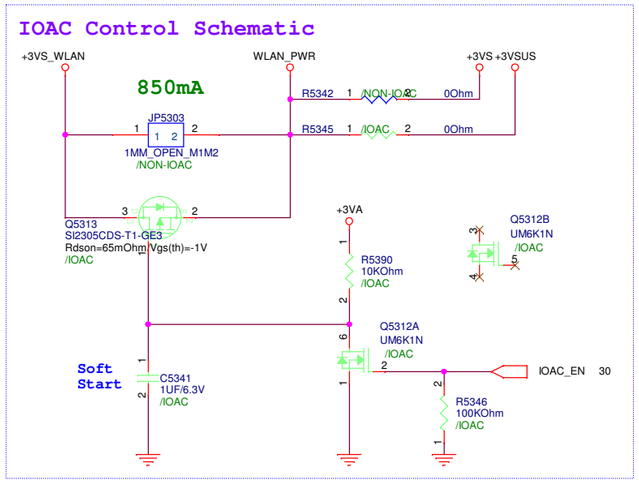


Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.







PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4

Title : PCIE_WLAN_BT

Engineer: sinsian_Jheng

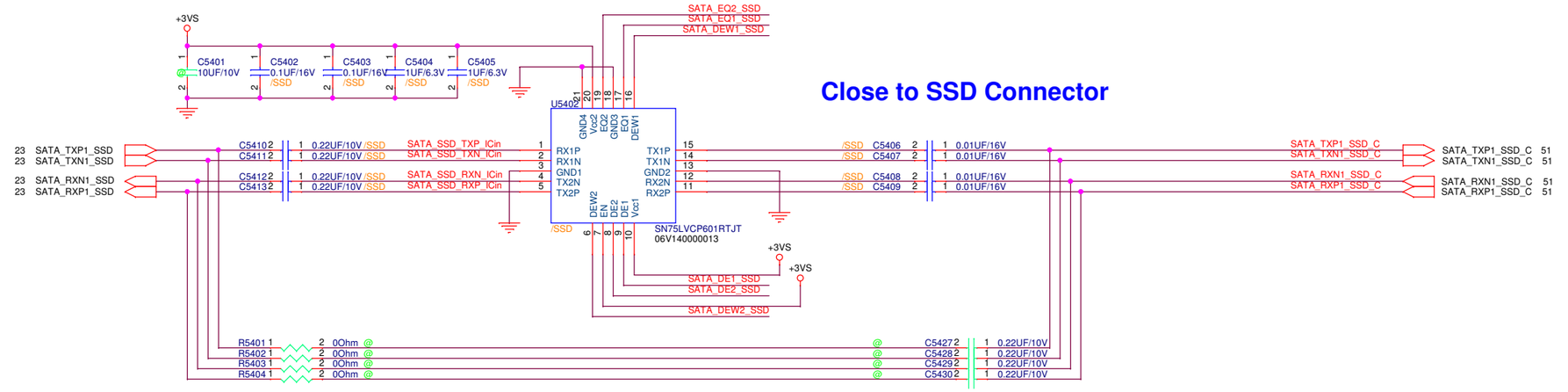
Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 19, 2016 Sheet 53 of 96

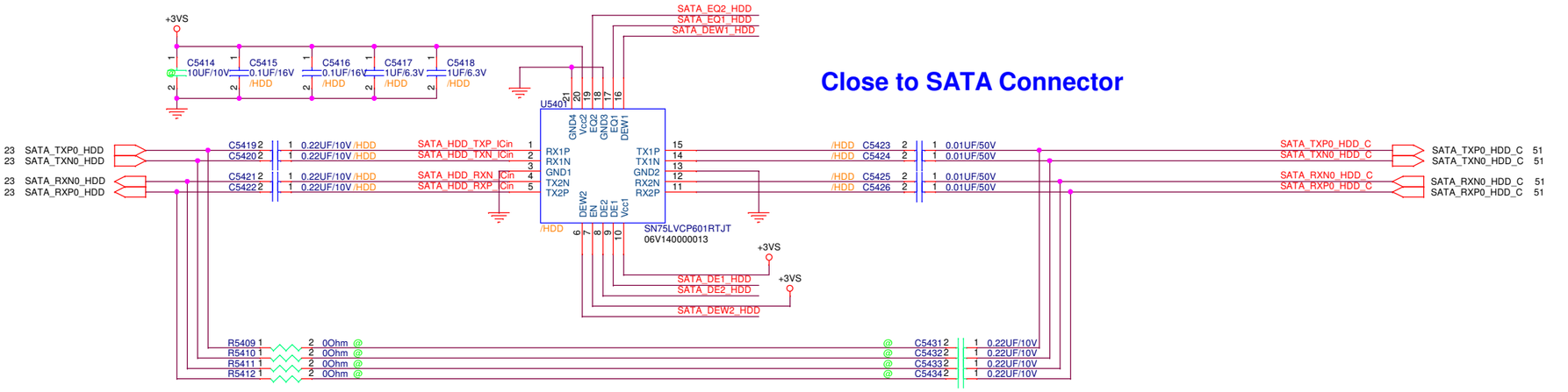
SATA Repeater

+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,57,58,59,62,64,91,92

SSD Redriver



HDD Redriver



EQ1	Resistor
0 dB	NC
7 dB	PD
14 dB	PU

EQ2	Resistor
0 dB	NC
7 dB	PD
14 dB	PU

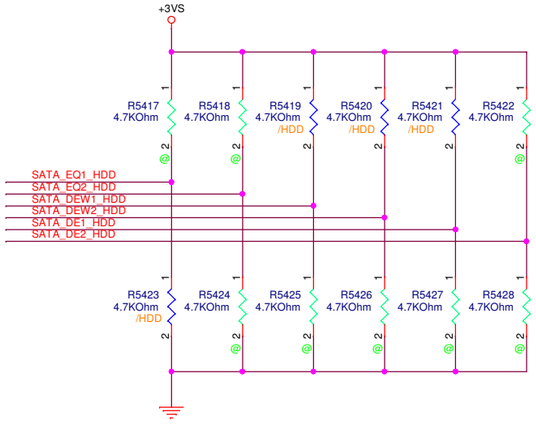
DE1	Resistor
0 dB	PD
-2 dB	PU
-4 dB	NC

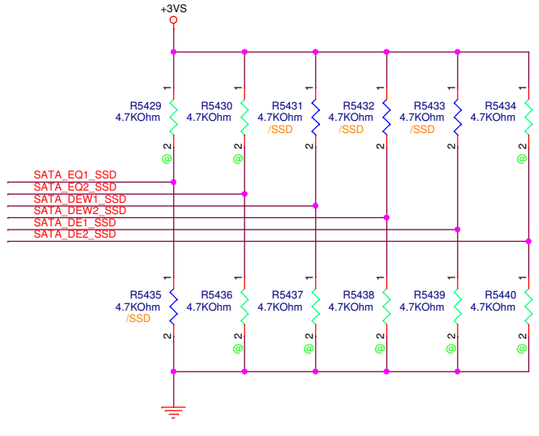
DE2	Resistor
0 dB	PD
-2 dB	PU
-4 dB	NC

DEW1	Resistor
Short	PD
Long	PU

DEW2	Resistor
Short	PD
Long	PU

EN	Resistor
Standby	PD
Normal	PU





PEGATRON Title : SATA Repeater

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName> Engineer: Ryan_Yen

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 54 of 99

DISCHARGE

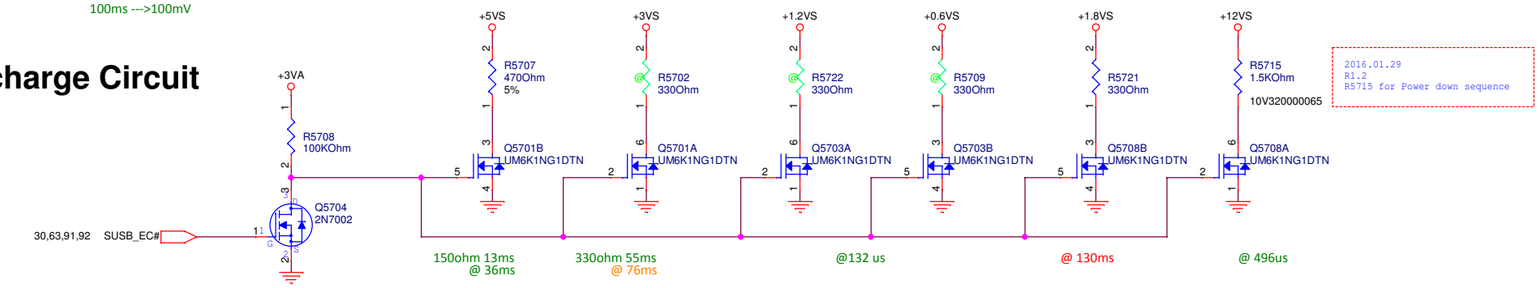
+3VA +3VA 21,24,30,31,36,53,60,64,81,88,93
+5VS +5VS 31,36,45,48,50,51,80,87,91
+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,54,58,59,62,64,91,92
+1.2V +1.2V 3,4,7,15,16,17,18,19,83
+1.8VS +1.8VS 21,36,91
+12VS +12VS 28,31,48,91
+0.6VS +0.6VS 15,18,83
+12V +12V 91
+3V +3V 31,58,64,91

+1.0V +1.0V 7,91
+VGA_VCORE +VGA_VCORE 75,87
+3VS_VGA +3VS_VGA 74,75,86,87,91
+1.05VS_VGA +1.05VS_VGA 70,71,72,86
+1.5VS_VGA +1.5VS_VGA 71,75,76,89
+3VS_AON_VGA +3VS_AON_VGA 70,72,74,75,91

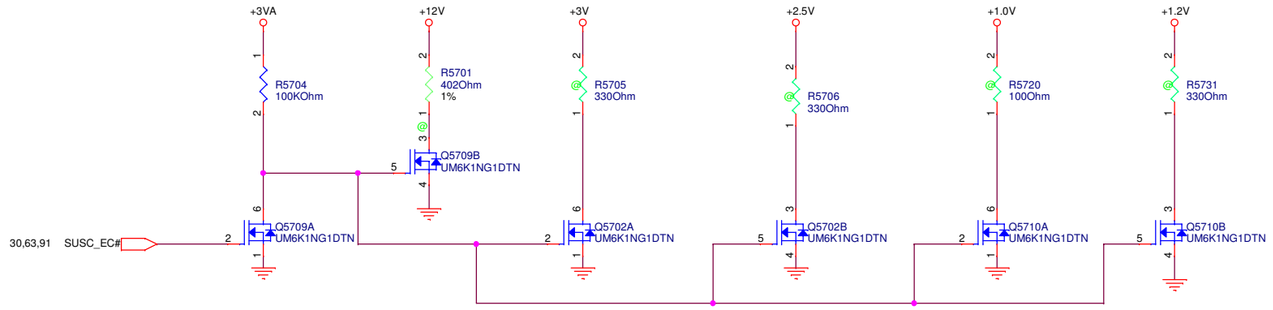
0402 1/16W min. resister
5V 400 OHM
3V 144 OHM
12V 2304 OHN

100ms --->100mV

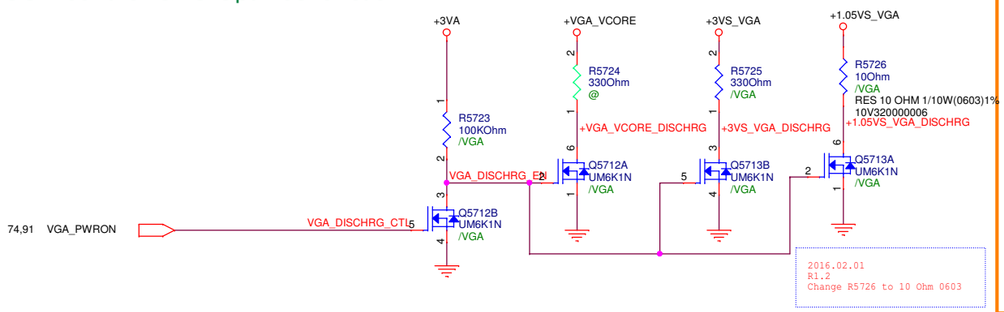
Discharge Circuit



2016.01.29
R1.2
R5715 for Power down sequence

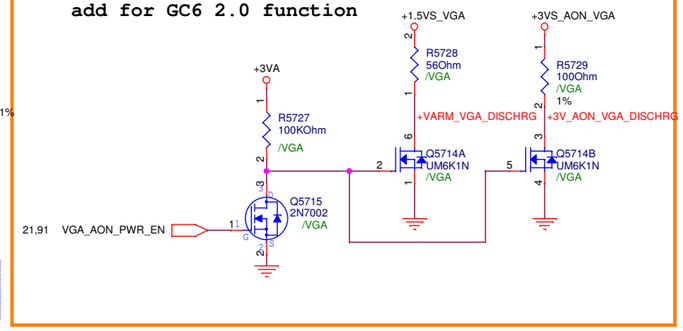


all MOS mount for GPU Optimus function



2016.02.01
R1.2
Change R5726 to 10 Ohm 0603

add for GC6 2.0 function



PEGATRON Title : DISCHARGE
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 57 of 96

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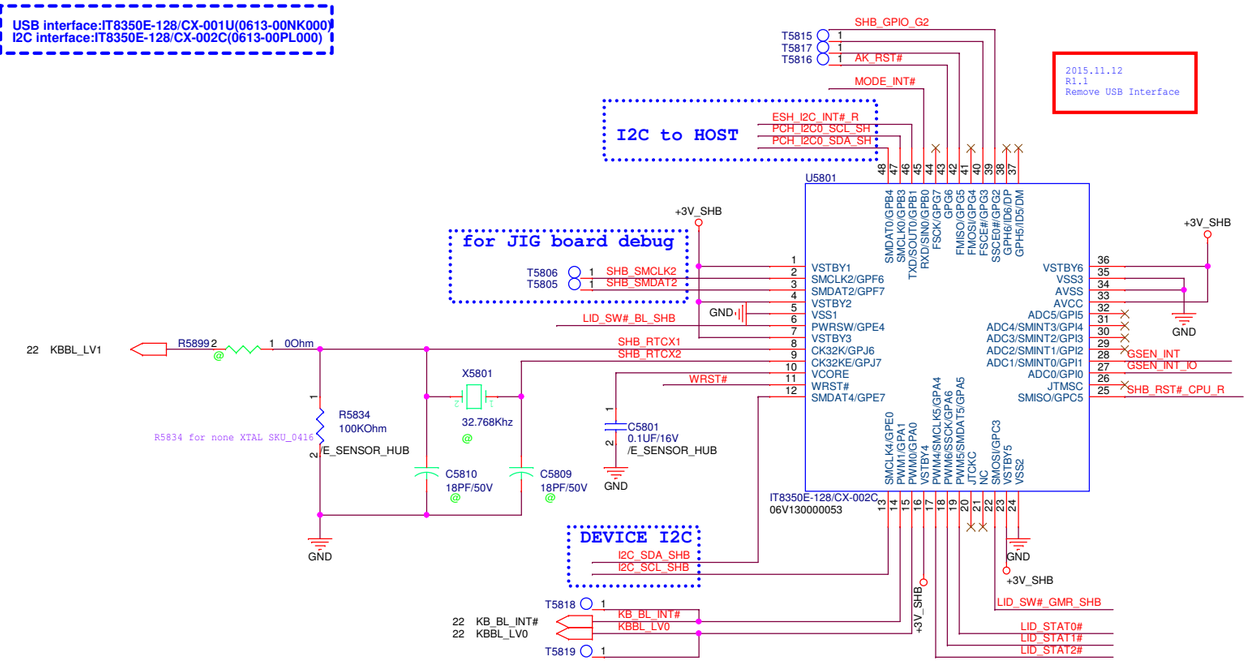
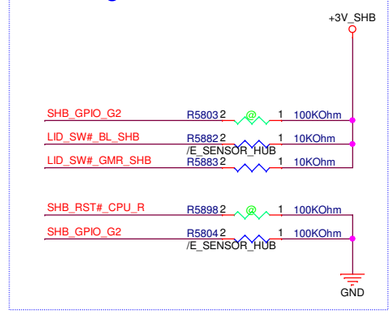
Sensor Hub

USB interface:IT8350E-128/CX-001U(0613-00NK000)
I2C interface:IT8350E-128/CX-002C(0613-00PL000)

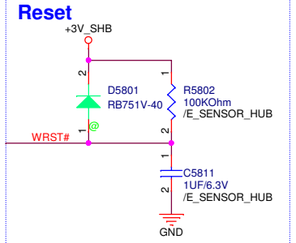
2015.11.12
R1.1
Remove USB Interface

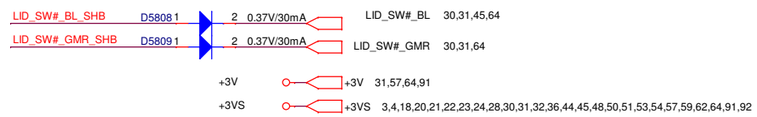


Pull High/ Pull Down

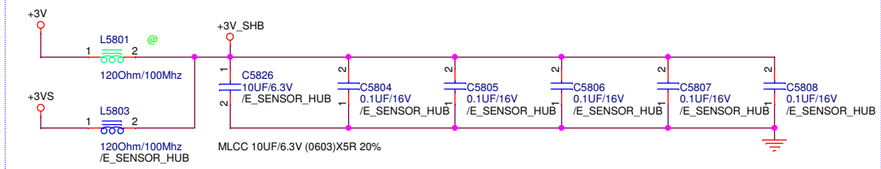


Reset



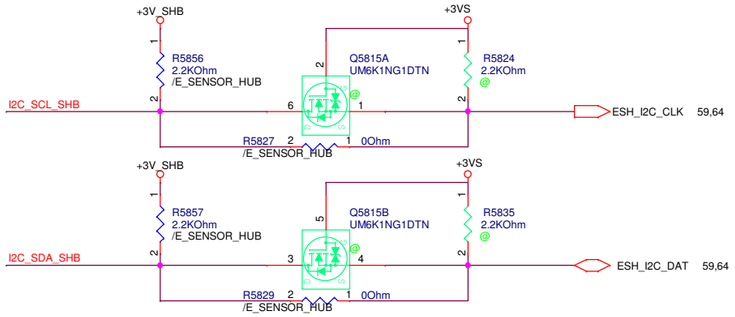


Sensor HUB Power Decouple

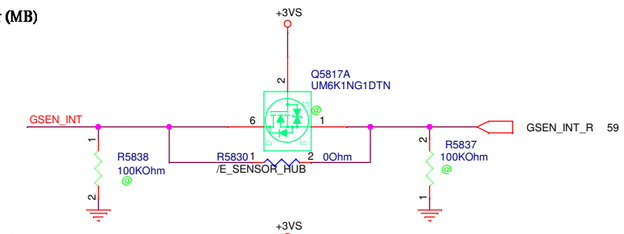


2016.02.02
R1.2
Change 10 UF from 0402 to 0603

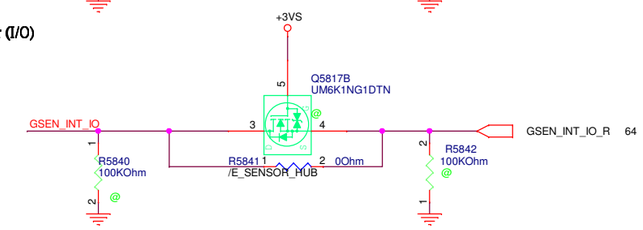
DEVICE I2C



G-Sensor (MB)

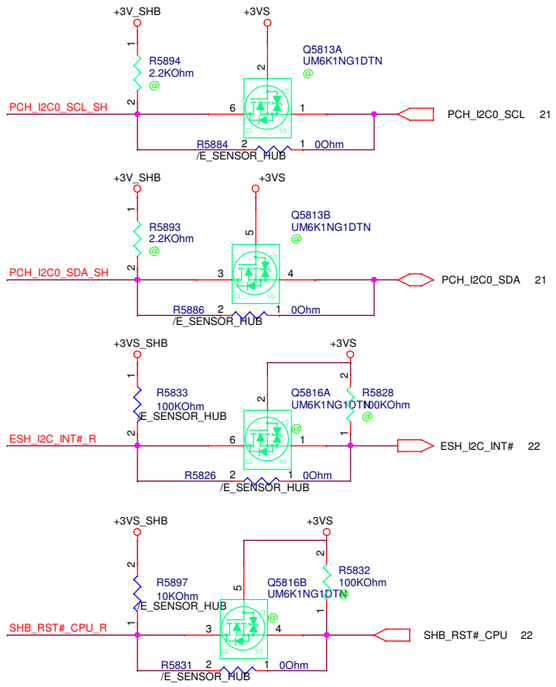


G-Sensor (I/O)



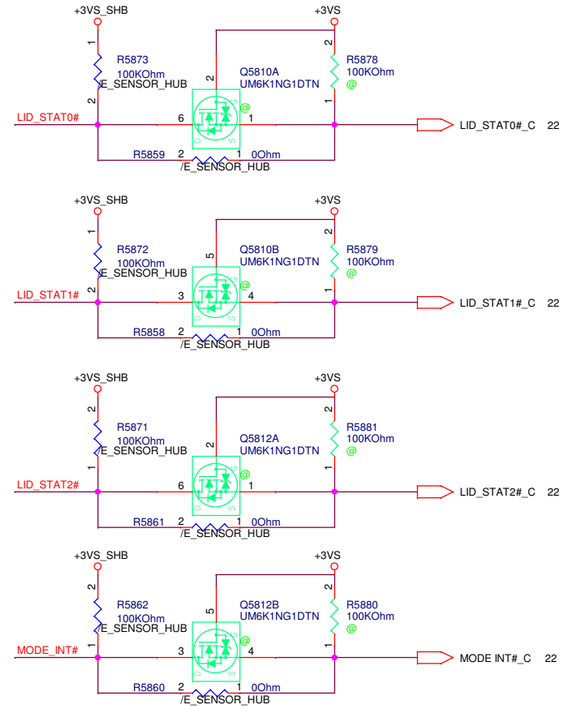
HOST I2C

HOST I2C to SHB



MODE GPIO & INT

Report To PCH



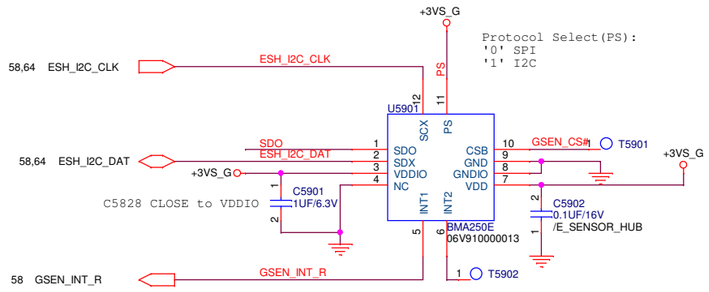
PEGATRON Title : Sensor Hub
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: sinsian_Jheng

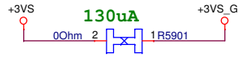
Size	Project Name	Rev
Custom	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 58 of 96

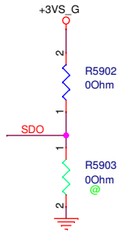
G Sensor

+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,62,64,91,92





U5806.1 Pull Up V	Slave Address(7-bits): 0x19 (W: 0x32, R: 0x33)
U5806.1 Pull Down	Slave Address(7-bits): 0x18 (W: 0x30, R: 0x31)



FAE
1. Left INT2 Floating
2.SDO use 0 ohm as option
3.INT PUD R UNMOUNT

N/A

N/A

PEGATRON Title : G Sensor
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 59 of 96

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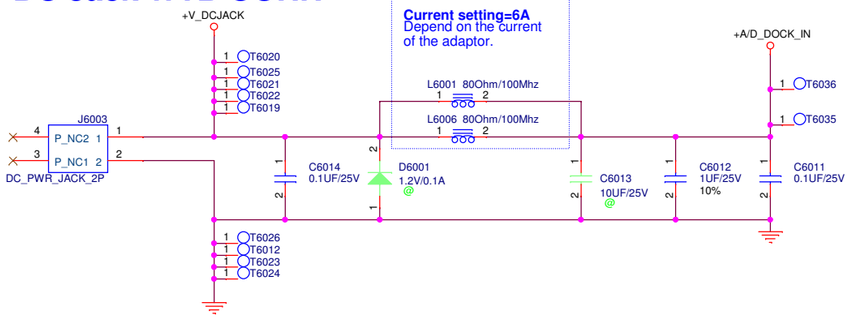
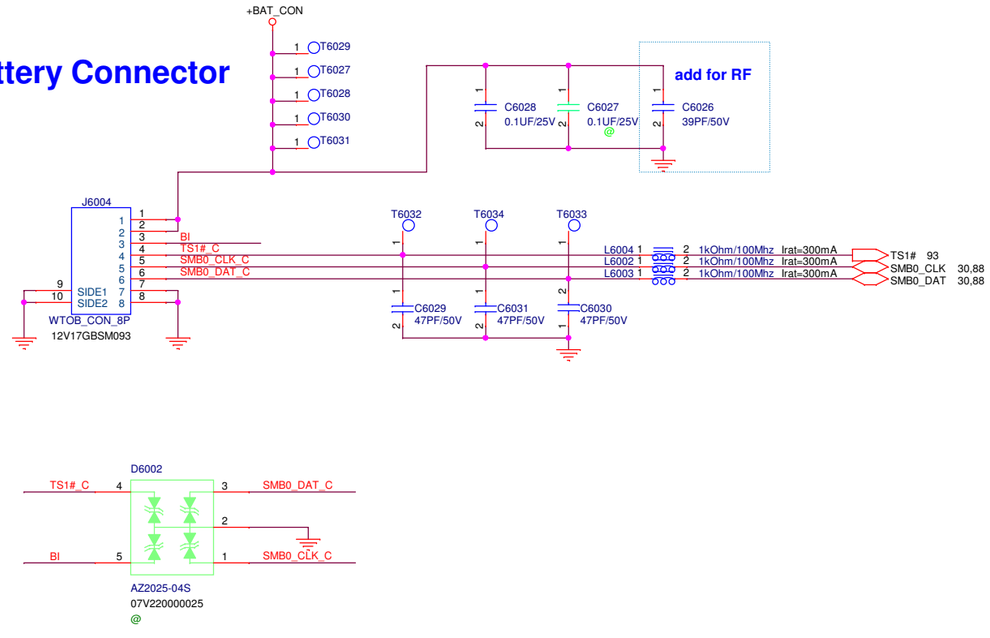
DC_BAT_CONN

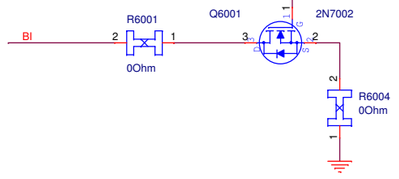
DC Jack WTB CONN



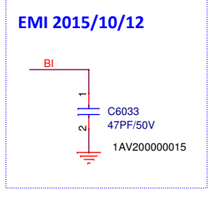
Battery Connector



客戶EE提出的原因是因為若有100OHM可能會造成分壓而導致BI pin無法拉到low，故改為0ohm



2015.11.12
R1.1
Remove SW6002



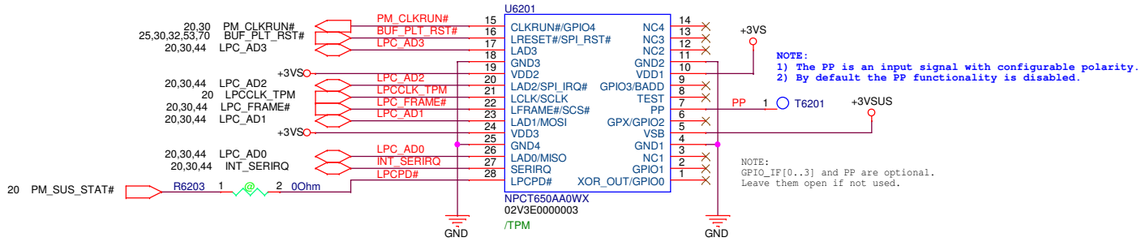
+VCC_RTC +VCC_RTC 24,25,26,36
+3VA_EC +3VA_EC 28,30,32
+3VA +3VA 21,24,30,31,36,53,57,64,81,88,93
+5VA +5VA 64,81
+1.0VSUS +1.0VSUS 26,82
+1.8VSUS +1.8VSUS 9,26,84
+3VSUS +3VSUS 4,21,24,25,26,28,30,31,51,53,62,63,81,92
+5VSUS +5VSUS 13,52,64,81
+12VSUS +12VSUS 28,81,91
+3V +3V 31,57,58,64,91
+12V +12V 57,91
+1.8VS +1.8VS 21,36,57,91
+3VS +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,62,64,91,92
+5VS +5VS 31,36,45,48,50,51,57,80,87,91
+12VS +12VS 28,31,48,57,91
+AC_BAT_SYS +AC_BAT_SYS 45,80,81,82,83,87,88,89
+A/D_DOCK_IN +A/D_DOCK_IN 88
+BAT_CON +BAT_CON 88
+VCORE +VCORE 5,80
+VCCGT +VCCGT 6,80
+VCCSA +VCCSA 7,80
+VCCIO +VCCIO 3,7,9,91
+RTCBAT +RTCBAT 24

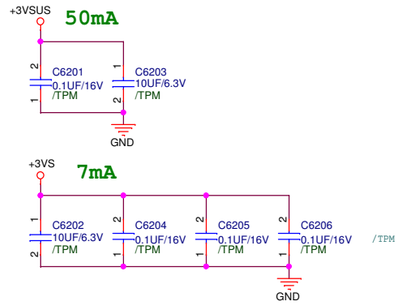
PEGATRON Title : DC_BAT_CONN
BG1-NB4 Engineer: sinsian_Jheng
Size C | Project Name P5HCJ/Megatron | Rev 1.2
Date: Friday, February 05, 2016 | Sheet 60 of 96

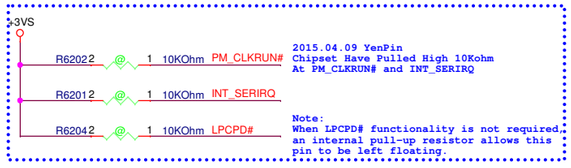
TPM NPCT650

+3VSUS ⟶ +3VSUS 4,21,24,25,26,28,30,31,51,53,63,81,92

+3VS ⟶ +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,54,57,58,59,64,91,92

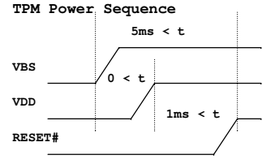






TPM VDD: Power the I/O buffers of the GPIO ports and the Host Interface
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

TPM Power Sequence



NOTE: RESET# is LRESET#, SPI_RST# or SRESET#.

NOTE:
1) For TPM 1.2:
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
2) For TPM 2.0:
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
4) RESET# must be asserted for at least 5 msec after VSB power-up.
5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

PEGATRON	Title : TPM NPCT650	
BG1-NB4	Engineer: sinsian_Jheng	
Size: C	Project Name: P5HCJ/Megatron	Rev: 1.2
Date: Friday, February 05, 2016	Sheet 62 of 96	

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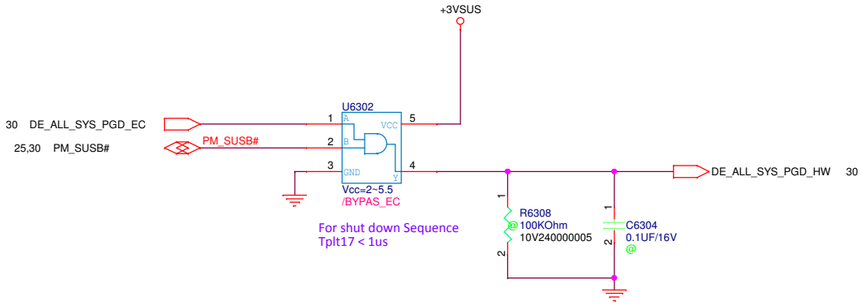
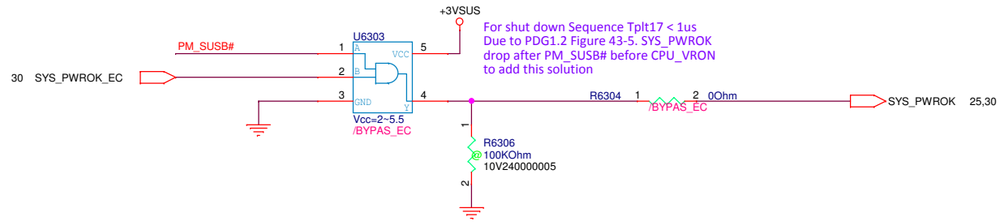
BYPASS EC SEQUENCE

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms

Delay By EC(2ms+ EC processing time (3ms~33ms)



For shut down Sequence
Tplt17 < 1us



PEGATRON Title : BYPASS EC SEQUENCE

BG1-NB4 Engineer: sinsian_Jheng

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 63 of 96

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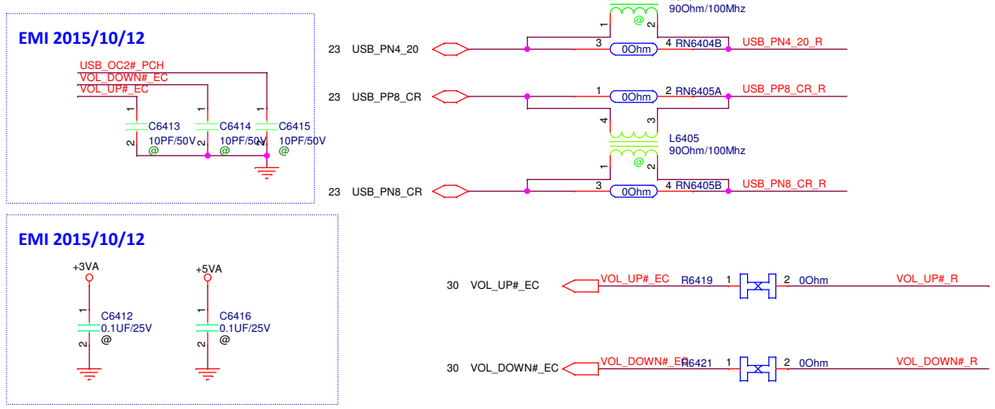
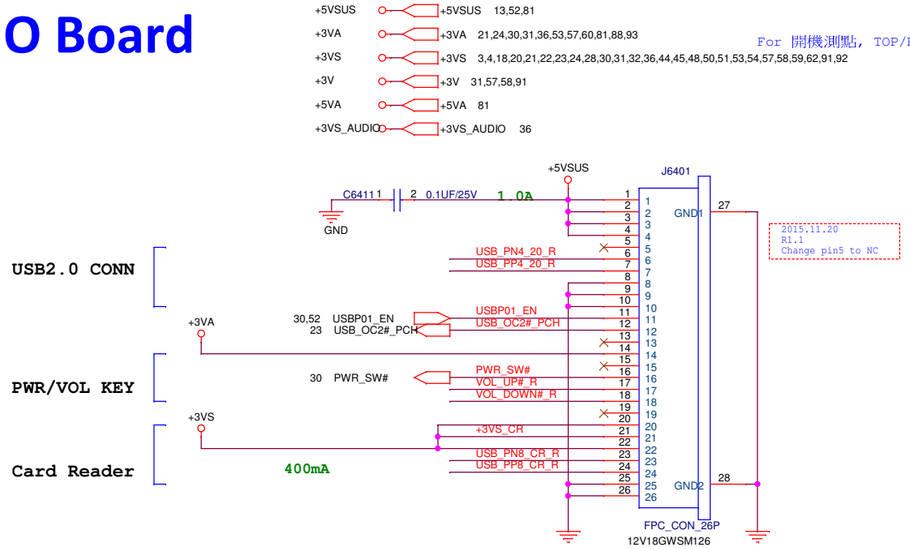
IO Board

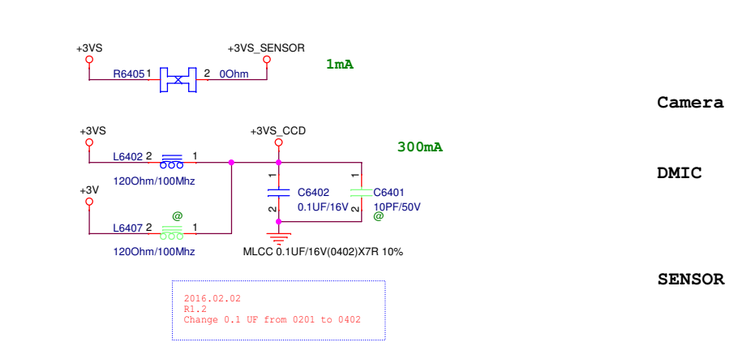


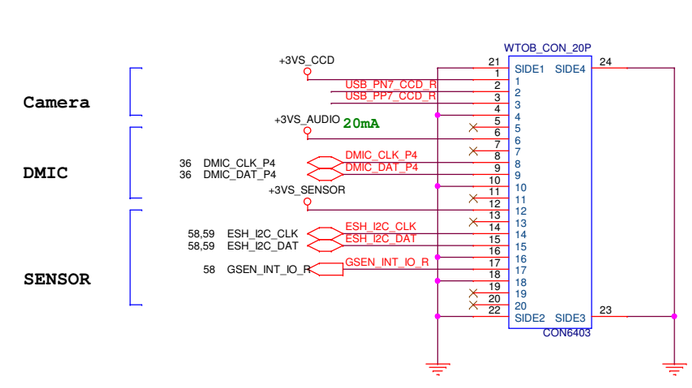


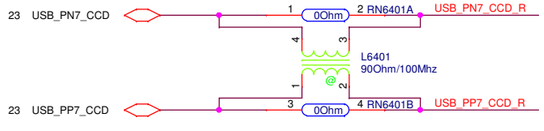
MB Connector Pin Define

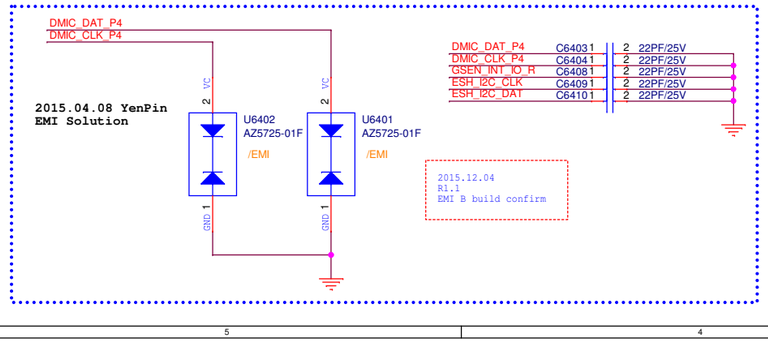
	R15
1	+5VSUS
2	+5VSUS
3	+5VSUS
4	+5VSUS
5	NC
6	USB_PN4_20_R
7	USB_PP4_20_R
8	GND
9	GND
10	GND
11	USBP01_EN
12	USB_OC2#_PCH
13	NC
14	+3VA
15	NC
16	PWR_SW#
17	VOL_UP#
18	VOL_DOWN#
19	NC
20	+3VS
21	+3VS
22	+3VS
23	USB_PN8_CR
24	USB_PP8_CR
25	GND
26	GND

Sensor Board Conn









MB Connector Pin Define

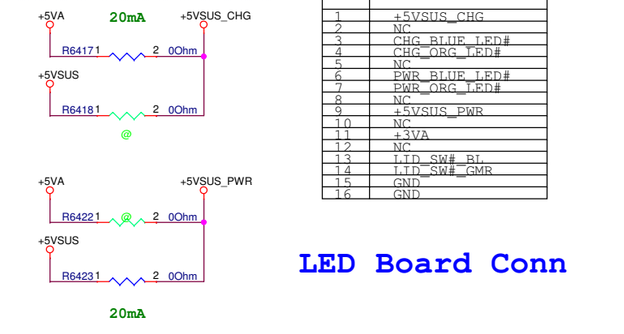
	R15
1	+3VS_CCD
2	USB_PN7_CCD_R
3	USB_PP7_CCD_R
4	GND
5	NC
6	+3VS_AUDIO
7	NC
8	DMIC_CLK_P4
9	DMIC_DAT_P4
10	GND
11	NC
12	+3VS_SENSOR
13	NC
14	ESH_I2C_CLK
15	ESH_I2C_DAT
16	GND
17	GSEN_INT_IO_R
18	GND
19	NC
20	NC

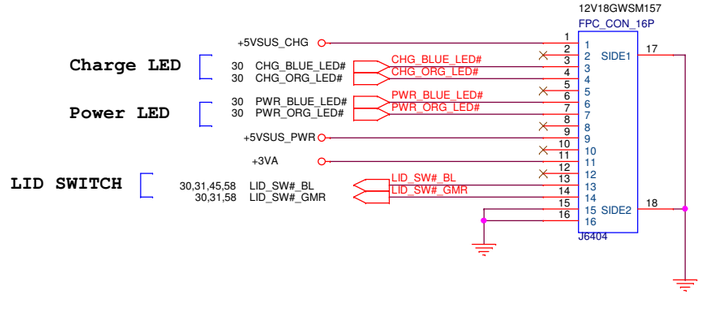
2016.02.03
R1.2
By 客戶BIOS/Erik回覆，當Battery電量<= 3%時，
若在S4/S5下按下Power button需要Flash charging LED並禁止system power on
請將Charge LED的power plan修改至+5VA power plan

MB Connector Pin Define

	R15
1	+5VSUS_CHG
2	NC
3	CHG_BLUE_LED#
4	CHG_ORG_LED#
5	NC
6	PWR_BLUE_LED#
7	PWR_ORG_LED#
8	NC
9	+5VSUS_PWR
10	NC
11	+3VA
12	NC
13	LID_SW#_BL
14	LID_SW#_GMR
15	GND
16	GND

LED Board Conn





PEGATRON	Title : IO Board		
BG1-NB4	Engineer: sinsian_Jheng		
Size: C	Project Name: P5HCJ/Megatron		Rev: 1.2
Date: Friday, February 05, 2016	Sheet 64 of 96		

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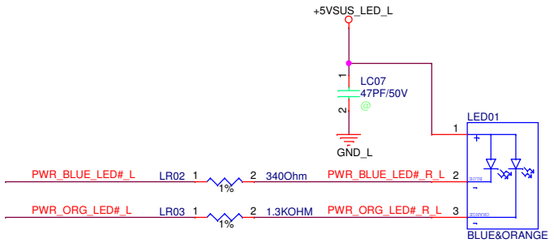
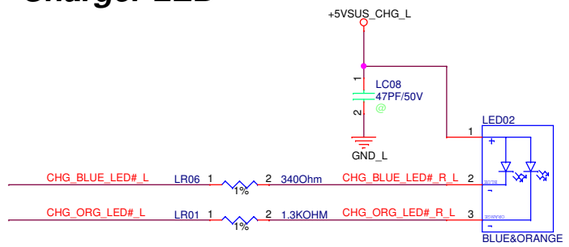
LED Board

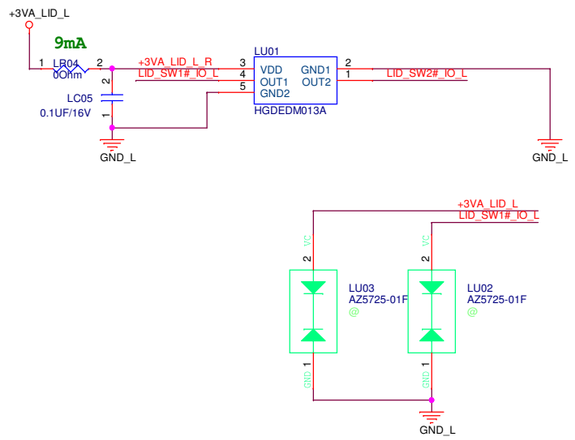
POWER LED

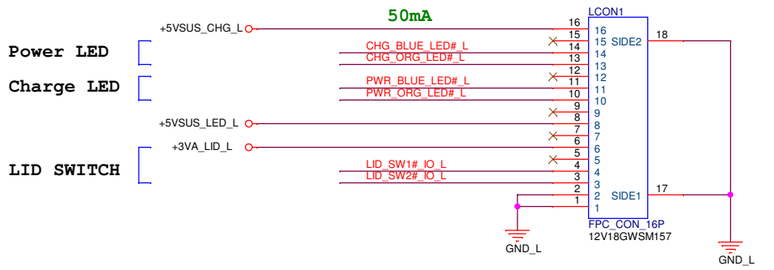


Charger LED



LID Switch





ME

Screw Hole A PTH

LH1
C276D98
GND_L

Tooling Hole C NPTH

LH3
O98X79DO98X79N

Tooling Hole B NPTH

LH2
C79D79N

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LED Board

BG1/HW4

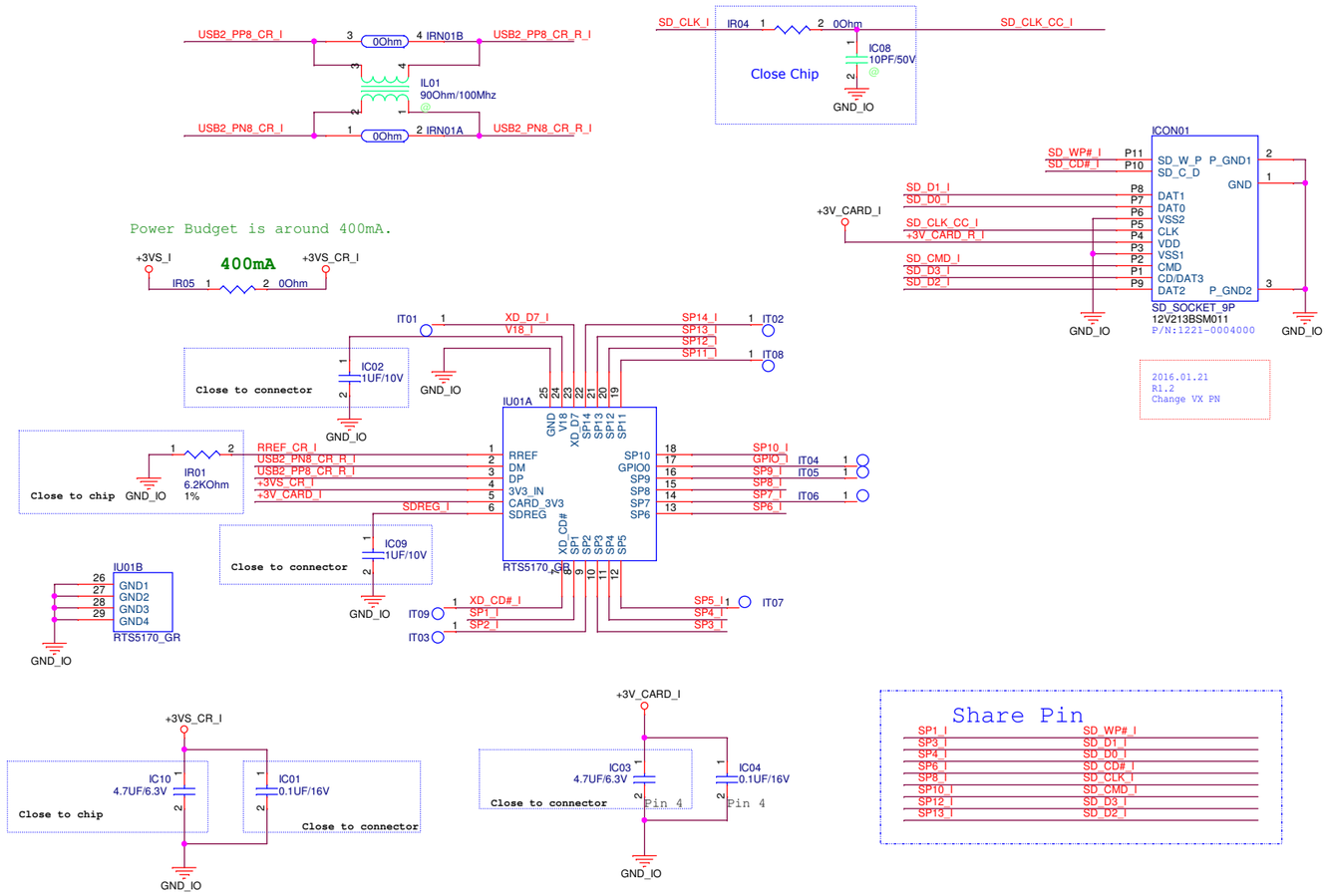
Engineer: Ryan_Yen

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

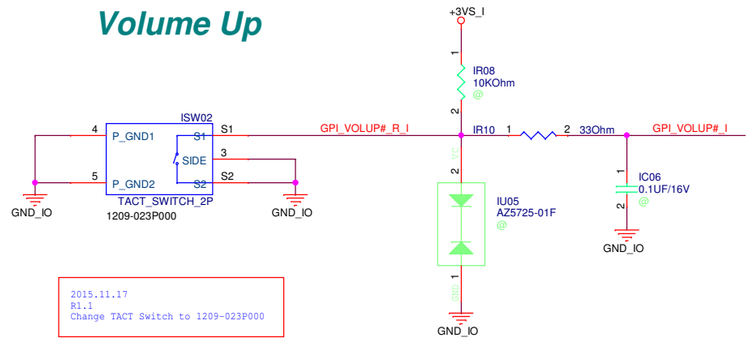
Date: Friday, February 05, 2016 Sheet 65 of 110

IO Board

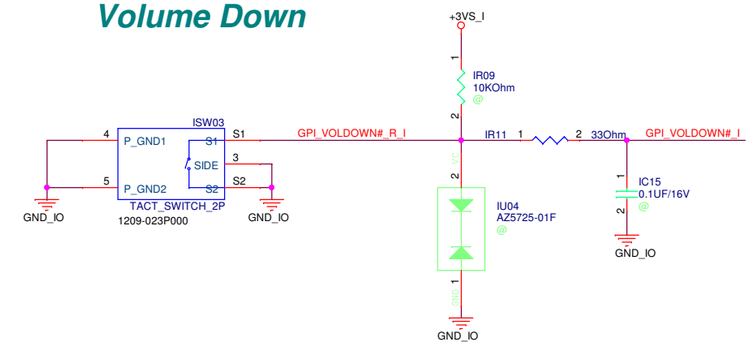
Card Reader



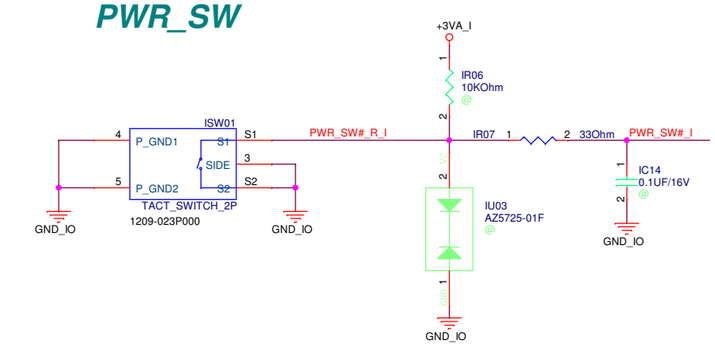
Volume Up



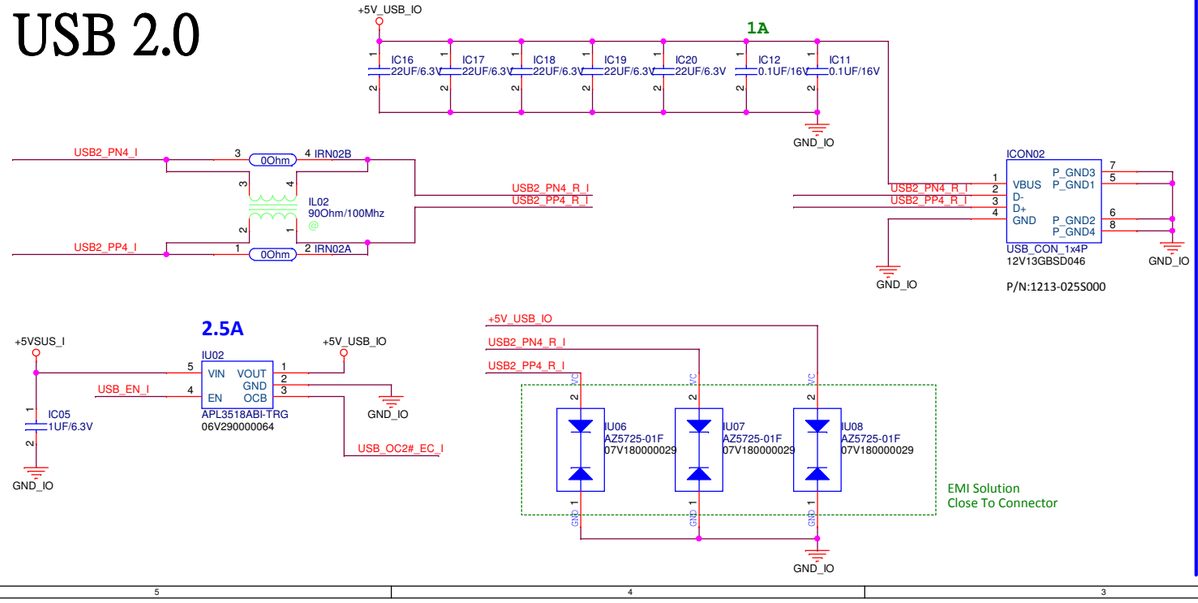
Volume Down



PWR_SW



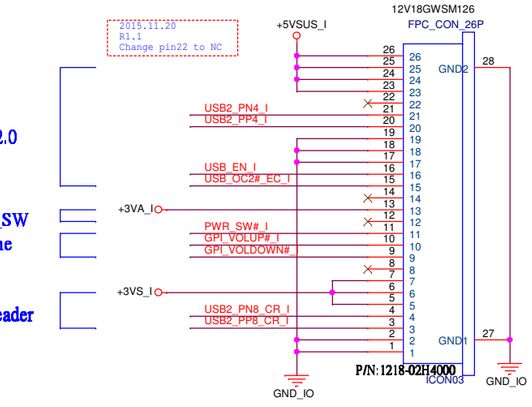
USB 2.0



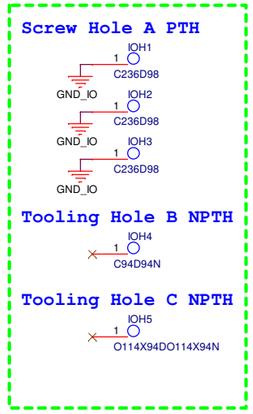
Connector

IO Connector Pin Define

R15	
26	+5VSUS
25	+5VSUS
24	+5VSUS
23	+5VSUS
22	NC
21	USB_PN4_20_R
20	USB_PP4_20_R
19	GND
18	GND
17	GND
16	USBP01_EN
15	USB_OC2#_PCH
14	NC
13	+3VA
12	NC
11	PWR_SW#
10	VOL_UP#
9	VOL_DOWN#
8	NC
7	+3VS
6	+3VS
5	+3VS
4	USB_PN8_CR_
3	USB_PP8_CR_
2	GND
1	GND



ME



PEGATRON Title : IO Board

PEGATRON PROPRIETARY AND CONFIDENTIAL

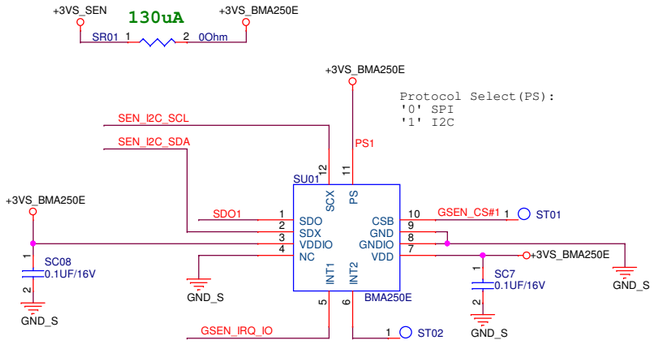
BG1/HW4 Engineer: Ryan_Yen

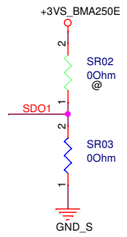
Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 66 of 110

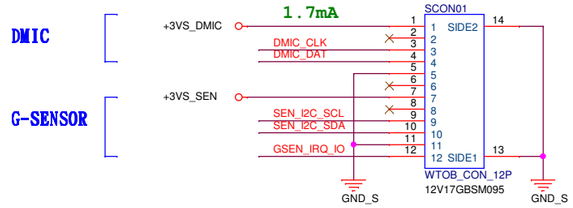
Sensor Board

G-Sensor

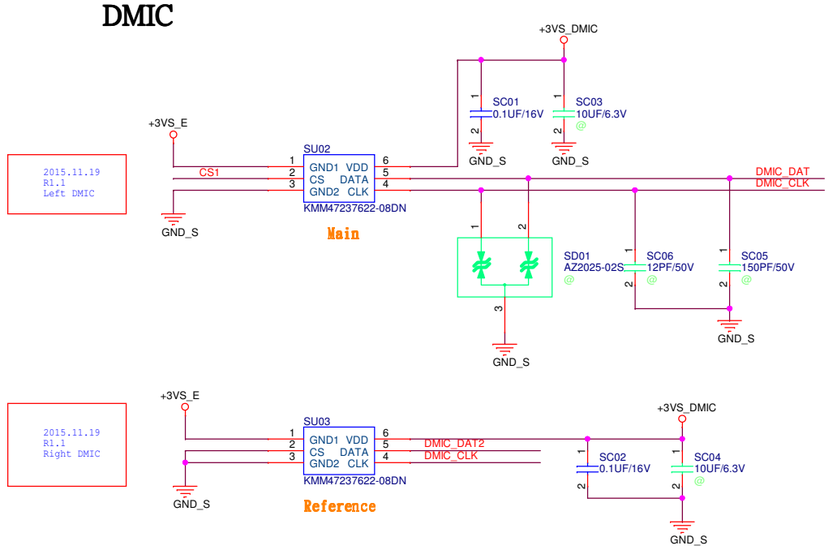


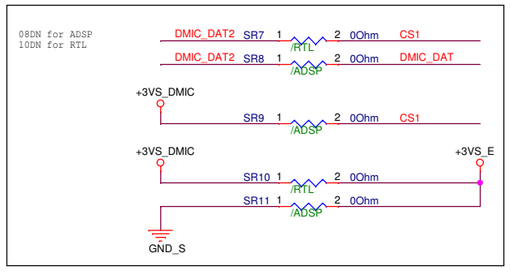


SU01.1 Pull Up	Slave Address(7-bits): 0x19 (W: 0x32, R: 0x33)
SU01.1 Pull Down V	Slave Address(7-bits): 0x18 (W: 0x30, R: 0x31)



DMIC





ME

Tooling Hole B NPTH

SH1
1
C91D91N

Tooling Hole C NPTH

SH2
1
O110X91DO110X91N

PEGATRON Title : Sensor Board

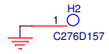
BG1/HW4 Engineer: Ryan_Yen

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

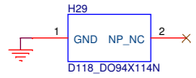
Date: Tuesday, February 23, 2016 Sheet 67 of 110

ME Hole

Screw Hole A PTH

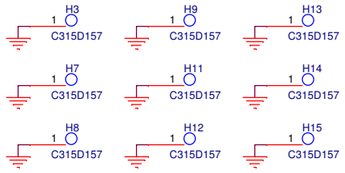


Screw Hole K/M/N PTH



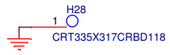
Tooling Hole H NPTH

Screw Hole B/C/D PTH



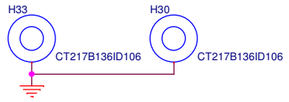
Tooling Hole O NPTH

Screw Hole E/L PTH

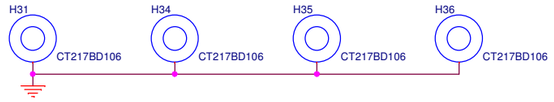


Screw Hole F PTH

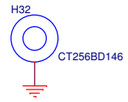
GPU NUT



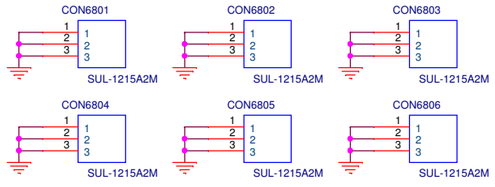
CPU NUT



WLAN NUT



Clip



PEGATRON Title : ME Hole

PEGATRON PROPRIETARY AND CONFIDENTIAL

<OrgName> Engineer: Ryan Yen

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

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VGA_PCIE

+3VS_AON_VGA → +3VS_AON_VGA 57,72,74,75,91
+1.05VS_VGA → +1.05VS_VGA 57,71,72,86

2015.12.07
R1.1
NVIDIA suggests to mount R7014
Unmount R7013

+3VS_AON_VGA
R70142 /VGA 1 0Ohm
21,86,87,89 DGPU_PWROK
R70132 @ 1 0Ohm
Q7001 2N7002 /VGA
24 CLK_REQ0_PEG#
+3VS_AON_VGA
R7005 10KOhm /VGA
CLKREQ_PEG#_R

U7001A
1/14 PCI_EXPRESS

	AB6	NC138
PEX_RST#	AC7	PEX_RST_N
CLKREQ_PEG#_R	AC6	PEX_CLKREQ_N
24 CLK_PCIE_PEG_PCH	AE8	PEX_REFCLK
24 CLK_PCIE_PEG#_PCH	AD8	PEX_REFCLK_N
23 PCIENB_RXP1 — PCIENB_RXP1 C70171 2 0.22UF/10V PCIENB_RXP1_C	AC9	PEX_TX0
23 PCIENB_RXN1 — PCIENB_RXN1 C70081 2 0.22UF/10V PCIENB_RXN1_C	AB9	PEX_TX0_N
23 PCIEG_TXP1	AG6	PEX_RX0
23 PCIEG_TXN1	AG7	PEX_RX0_N
23 PCIENB_RXP2 — PCIENB_RXP2 C70181 2 0.22UF/10V PCIENB_RXP2_C	AB10	PEX_TX1
23 PCIENB_RXN2 — PCIENB_RXN2 C70091 2 0.22UF/10V PCIENB_RXN2_C	AC10	PEX_TX1_N
23 PCIEG_TXP2	AF7	PEX_RX1
23 PCIEG_TXN2	AE7	PEX_RX1_N
23 PCIENB_RXP3 — PCIENB_RXP3 C70191 2 0.22UF/10V PCIENB_RXP3_C	AD11	PEX_TX2
23 PCIENB_RXN3 — PCIENB_RXN3 C70101 2 0.22UF/10V PCIENB_RXN3_C	AC11	PEX_TX2_N
23 PCIEG_TXP3	AE9	PEX_RX2
23 PCIEG_TXN3	AF9	PEX_RX2_N
23 PCIENB_RXP4 — PCIENB_RXP4 C70201 2 0.22UF/10V PCIENB_RXP4_C	AC12	PEX_TX3
23 PCIENB_RXN4 — PCIENB_RXN4 C70111 2 0.22UF/10V PCIENB_RXN4_C	AB12	PEX_TX3_N
23 PCIEG_TXP4	AG9	PEX_RX3
23 PCIEG_TXN4	AG10	PEX_RX3_N
	AB13	NC126
	AC13	NC127
	AF10	NC102
	AE10	NC103
	AD14	NC128
	AC14	NC129
	AE12	NC104
	AF12	NC105
	AC15	NC130
	AB15	NC131
	AG12	NC106
	AG13	NC107
	AB16	NC132
	AC16	NC133
	AF13	NC108
	AE13	NC109
	AD17	NC134
	AC17	NC135
	AE15	NC110
	AF15	NC111
	AC18	NC136
	AB18	NC137
	AG15	NC112
	AG16	NC113
	AB19	NC114
	AC19	NC115
	AF16	NC90
	AE16	NC91
	AD20	NC116
	AC20	NC117
	AE18	NC92
	AF18	NC93
	AC21	NC118
	AB21	NC119
	AG18	NC94
	AG19	NC95
	AD23	NC120
	AE23	NC121
	AF19	NC96
	AE19	NC97
	AF24	NC122
	AE24	NC123
	AE21	NC98
	AF21	NC99
	AG24	NC124
	AG25	NC125
	AG21	NC100
	AG22	NC101

PCIEG => From CPU
PCIENB : to CPU

PEX_IOVDD_1 PEX_IOVDD_2 PEX_IOVDD_3 PEX_IOVDD_4 PEX_IOVDD_5 PEX_IOVDD_6	AA22 PEX_IOVDD; AB23; AC24; AD25; AE26; AE27	C7001 1UF/6.3V /VGA; C7002 1UF/6.3V @; C7003 4.7UF/6.3V @; C7007 10UF/6.3V /VGA; C7012 10UF/6.3V @; C7052 22UF/6.3V @
PEX_IOVDDQ_01 PEX_IOVDDQ_02 PEX_IOVDDQ_03 PEX_IOVDDQ_04 PEX_IOVDDQ_05 PEX_IOVDDQ_06 PEX_IOVDDQ_07 PEX_IOVDDQ_08 PEX_IOVDDQ_09 PEX_IOVDDQ_10 PEX_IOVDDQ_11 PEX_IOVDDQ_12 PEX_IOVDDQ_13 PEX_IOVDDQ_14	AA10 PEX_IOVDDQ; AA12; AA13; AA16; AA18; AA19; AA20; AA21; AB22; AC23; AD24; AE25; AF26; AF27	C7004 1UF/6.3V @; C7005 1UF/6.3V @; C7006 4.7UF/6.3V /VGA; C7015 10UF/6.3V @; C7051 10UF/6.3V @; C7053 22UF/6.3V /VGA
PEX_PLL_HVDD_1 PEX_PLL_HVDD_2	AA8; AA9	C7062 0.1UF/16V /VGA; C7054 4.7UF/6.3V /VGA; C7013 4.7UF/6.3V /VGA
PEX_SVDD_3V3	AB8	
VDD_SENSE	F2 → NVDD_SENSE 87	
GND_SENSE	F1 → NVDD_GND_SENSE 87	
PEX_TSTCLK PEX_TSTCLK_N	AF22 PEX_TSTCLK+ R7002 1 @ 2 200Ohm; AE22 PEX_TSTCLK-	
PEX_PLLVDD_1 PEX_PLLVDD_2	AA14 PEX_PLLVDD; AA15	C7061 0.1UF/16V /VGA; C7044 1UF/6.3V /VGA; C7045 4.7UF/6.3V /VGA; L7001 1 @ 2 120Ohm/100Mhz; R7001 1 /VGA 2 0Ohm; C7014 1UF/6.3V @
TESTMODE	AD9 GPU_TESTMODE R70041 /VGA 2 10KOhm	
PEX_TERMP	AF25 PEX_TERMP R70031 /VGA 2 2.49KOhm 1%	

PLACE BETWEEN GPU AND POWER SUPPLY
PLACE UNDER GPU
PLACE NEAR GPU
PLACE NEAR GPU +3VS_AON_VGA
+1.05VS_VGA

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74 GPU_PEX_RST_HOLD#
+3VS_AON_VGA +3VS_AON_VGA
U7002 SN74LVC1G08DCKR
GPU_PEX_RST_HOLD# SYS_PEX_RST_MON# PEX_RST# → PEX_RST# 74
R7010 10KOhm /VGA
R7009 100KOhm @
D7001 /VGA 1V/0.1A

From PCH GPIO_D12 21 DGPU_HOLD_RST#
25,30,32,53,62 From PLTRST# BUF_PLT_RST#
+3VS_AON_VGA +3VS_AON_VGA
U7003 SN74LVC1G08DCKR @
DGPU_HOLD_RST# BUF_PLT_RST# SYS_PEX_RST_MON# → SYS_PEX_RST_MON# 74
R7012 10KOhm /VGA
R7011 10KOhm @
D7002 /VGA 1V/0.1A

Title :	VGA_PCIE
PEGATRON PROPRIETARY AND CONFIDENTIAL	
BG1-NB4	Engineer: Ryan_Yen
Size C	Project Name P5HCJ/Megatron
Rev 1.2	
Date: Friday, February 05, 2016	Sheet 70 of 96

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VGA_FRAME BUFFER

76 FBAD[0..63]
76 FBADQM[0..7]
76 FBADQS_WP[0..7]
76 FBADQS_RN[0..7]

76 FBA_A[0..14]
76 FBA_ODT[0..1]
76 FBA_CKE[0..1]
76 FBA_CS#[0..1]
76 FBA_BA[0..2]

76 FBA_WE#
76 FBA_CAS#
76 FBA_RAS#

+1.5VS_VGA → +1.5VS_VGA 57,75,76,89
+1.05VS_VGA → +1.05VS_VGA 57,70,72,86
+3VS_VGA → +3VS_VGA 57,74,75,86,87,91

U7001B
2/14 FBA

FBAD0	E18	FBA_D0
FBAD1	F18	FBA_D1
FBAD2	E16	FBA_D2
FBAD3	F17	FBA_D3
FBAD4	D20	FBA_D4
FBAD5	D21	FBA_D5
FBAD6	F20	FBA_D6
FBAD7	E21	FBA_D7
FBAD8	E15	FBA_D8
FBAD9	D15	FBA_D9
FBAD10	F15	FBA_D10
FBAD11	F13	FBA_D11
FBAD12	C13	FBA_D12
FBAD13	B13	FBA_D13
FBAD14	E13	FBA_D14
FBAD15	D13	FBA_D15
FBAD16	B15	FBA_D16
FBAD17	C16	FBA_D17
FBAD18	A13	FBA_D18
FBAD19	A15	FBA_D19
FBAD20	B18	FBA_D20
FBAD21	A18	FBA_D21
FBAD22	A19	FBA_D22
FBAD23	C19	FBA_D23
FBAD24	B24	FBA_D24
FBAD25	C23	FBA_D25
FBAD26	A25	FBA_D26
FBAD27	A24	FBA_D27
FBAD28	A21	FBA_D28
FBAD29	B21	FBA_D29
FBAD30	C20	FBA_D30
FBAD31	C21	FBA_D31
FBAD32	R22	FBA_D32
FBAD33	R24	FBA_D33
FBAD34	T22	FBA_D34
FBAD35	R23	FBA_D35
FBAD36	N25	FBA_D36
FBAD37	N26	FBA_D37
FBAD38	N23	FBA_D38
FBAD39	N24	FBA_D39
FBAD40	V23	FBA_D40
FBAD41	V22	FBA_D41
FBAD42	T23	FBA_D42
FBAD43	U22	FBA_D43
FBAD44	Y24	FBA_D44
FBAD45	AA24	FBA_D45
FBAD46	Y22	FBA_D46
FBAD47	AA23	FBA_D47
FBAD48	AD27	FBA_D48
FBAD49	AB25	FBA_D49
FBAD50	AD26	FBA_D50
FBAD51	AC25	FBA_D51
FBAD52	AA27	FBA_D52
FBAD53	AA26	FBA_D53
FBAD54	W26	FBA_D54
FBAD55	Y25	FBA_D55
FBAD56	R26	FBA_D56
FBAD57	T25	FBA_D57
FBAD58	N27	FBA_D58
FBAD59	R27	FBA_D59
FBAD60	V26	FBA_D60
FBAD61	V27	FBA_D61
FBAD62	W27	FBA_D62
FBAD63	W25	FBA_D63

FBADQM0	D19	FBA_DQM0
FBADQM1	D14	FBA_DQM1
FBADQM2	C17	FBA_DQM2
FBADQM3	C22	FBA_DQM3
FBADQM4	P24	FBA_DQM4
FBADQM5	W24	FBA_DQM5
FBADQM6	AA25	FBA_DQM6
FBADQM7	U25	FBA_DQM7

FBADQS_WP0	E19	FBA_DQS_WP0
FBADQS_WP1	C15	FBA_DQS_WP1
FBADQS_WP2	B16	FBA_DQS_WP2
FBADQS_WP3	B22	FBA_DQS_WP3
FBADQS_WP4	R25	FBA_DQS_WP4
FBADQS_WP5	W23	FBA_DQS_WP5
FBADQS_WP6	AB26	FBA_DQS_WP6
FBADQS_WP7	T26	FBA_DQS_WP7

FBADQS_RN0	F19	FBA_DQS_RN0
FBADQS_RN1	C14	FBA_DQS_RN1
FBADQS_RN2	A16	FBA_DQS_RN2
FBADQS_RN3	A22	FBA_DQS_RN3
FBADQS_RN4	P25	FBA_DQS_RN4
FBADQS_RN5	W22	FBA_DQS_RN5
FBADQS_RN6	AB27	FBA_DQS_RN6
FBADQS_RN7	T27	FBA_DQS_RN7

T7101
1 FB_VREF D23 → FB_VREF

GPU_FB_CLAMP_R R7107 2 1 0Ohm GC6_FB_EN → GC6_FB_EN 21,74,89
FB_CLAMP F3 → R7106 2 1 10KOhm /VGA

35 mA

FBA_CMD0	C27	FBA_CS#0
FBA_CMD1	C26	
FBA_CMD2	E24	FBA_ODT0
FBA_CMD3	F24	FBA_CKE0
FBA_CMD4	D27	FBA_A14
FBA_CMD5	D26	FBA_RST#
FBA_CMD6	F25	FBA_A9
FBA_CMD7	F26	FBA_A7
FBA_CMD8	F23	FBA_A2
FBA_CMD9	G22	FBA_A0
FBA_CMD10	G23	FBA_A4
FBA_CMD11	G24	FBA_A1
FBA_CMD12	F27	FBA_BA0
FBA_CMD13	G25	FBA_WE#
FBA_CMD14	G27	
FBA_CMD15	G26	FBA_CAS#
FBA_CMD16	M24	FBA_CS#1
FBA_CMD17	M23	
FBA_CMD18	K24	FBA_ODT1
FBA_CMD19	K23	FBA_CKE1
FBA_CMD20	M27	FBA_A13
FBA_CMD21	M26	FBA_A8
FBA_CMD22	M25	FBA_A6
FBA_CMD23	K26	FBA_A11
FBA_CMD24	K22	FBA_A5
FBA_CMD25	J23	FBA_A3
FBA_CMD26	J25	FBA_BA2
FBA_CMD27	J24	FBA_BA1
FBA_CMD28	K27	FBA_A12
FBA_CMD29	K25	FBA_A10
FBA_CMD30	J27	FBA_RAS#
FBA_CMD31	J26	

NVIDIA Design Guide
DG-07158-001_v05 P.92
Table 6-3

	LOWER 0..31	UPPER 32..63
CMD0	CS#	N/A
CMD1	N/A	N/A
CMD2	ODT	N/A
CMD3	CKE	N/A
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE#	WE#
CMD14	A15	A15
CMD15	CAS#	CAS#
CMD16	N/A	CS#
CMD17	N/A	N/A
CMD18	N/A	ODT
CMD19	N/A	CKE
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS#	RAS#

For test/Debug only
B19 → FBA_CMD32
FBA_CMD34 / FBA_CMD35 ← F22 / J22
R7101 1 @ 2 60.4Ohm 1% +1.5VS_VGA
R7102 1 @ 2 60.4Ohm 1%

FBA_CLK0	D24	FBA_CLK0 76
FBA_CLK0_N	D25	FBA_CLK0# 76
FBA_CLK1	N22	FBA_CLK1 76
FBA_CLK1_N	M22	FBA_CLK1# 76

FBA_WCK01	D18	
FBA_WCK01_N	C18	
FBA_WCK23	D17	
FBA_WCK23_N	D16	
FBA_WCK45	T24	
FBA_WCK45_N	U24	
FBA_WCK67	V24	
FBA_WCK67_N	V25	

FB_PLL_AVDD_1 F16
FB_PLL_AVDD_2 P22
FB_DLL_AVDD H22
1.05V+-3% 790 mA
+FB_PLL_AVDD
C7118 @ 0.1UF/16V
/VGA C7104 0.1UF/16V
/VGA C7101 0.1UF/16V
Place UNDER GPU
+1.05VS_VGA
/VGA C7103 22UF/6.3V
B7101 30Ohm/100Mhz /VGA
Place NEAR GPU

N16S-GTR-S-A2 /VGA
02V0A0000038

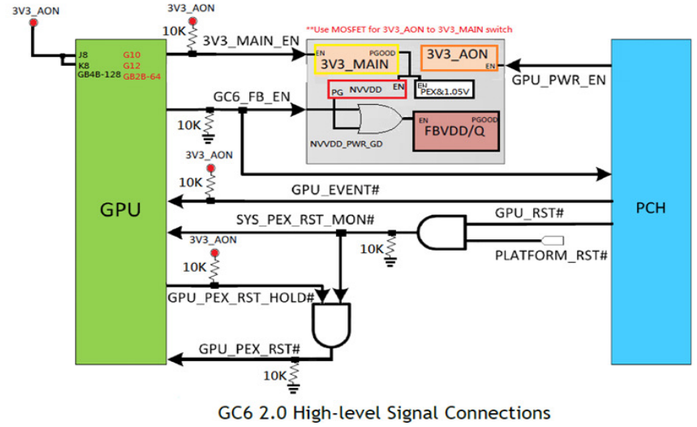
2015.11.27
R1.1
採購建議用料 22UF/6.3V 0603

GC6 RST

+1.5VS_VGA
R7124 100KOhm @
FBA_RST# → FBA_RST# 76
R7153 10KOhm /GC6

FBA_ODT_L FBA_ODT0 R7103 2 /VGA 1 10KOhm
FBA_ODT_H FBA_ODT1 R7104 2 /VGA 1 10KOhm
FBA_CKE_L FBA_CKE0 R7154 2 /VGA 1 10KOhm
FBA_CKE_H FBA_CKE1 R7108 2 /VGA 1 10KOhm

VR Complex



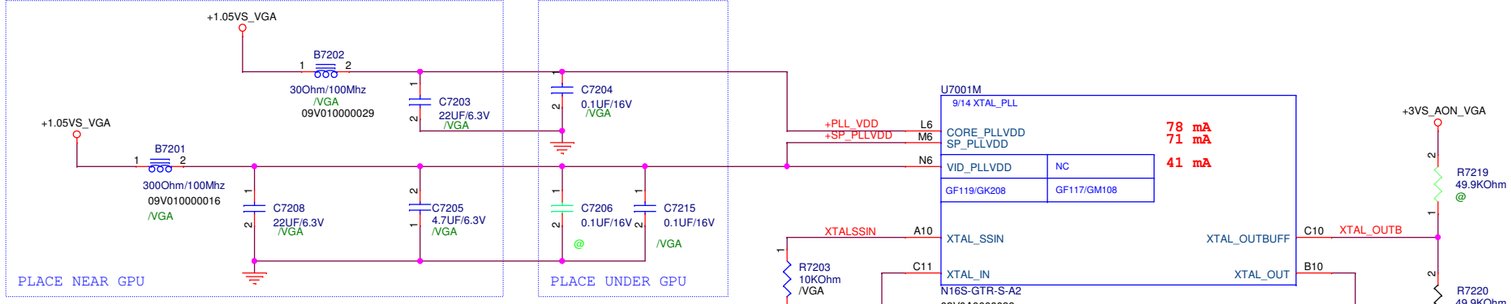
GC6 2.0 High-level Signal Connections

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : VGA_FRAME BUFFER
BG1-NB4
Engineer: Ryan_Yen
Size C | Project Name P5HCJ/Megatron | Rev 1.2
Date: Friday, February 05, 2016 | Sheet 71 of 96

VGA_XTAL

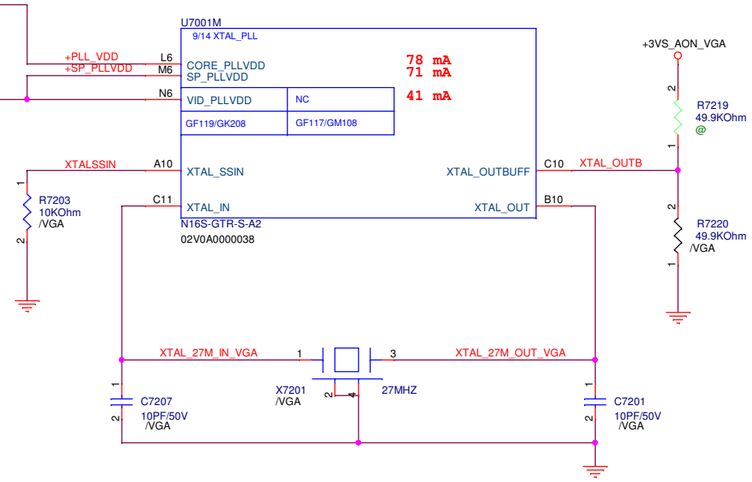
+1.05VS_VGA ⟶ +1.05VS_VGA 57,70,71,86
+3VS_AON_VGA ⟶ +3VS_AON_VGA 57,70,74,75,91

2015.11.27
R1.1
採購建議用料 22UF/6.3V 0603



N16x series B7201==> 300ohm bead.

2015.11.27
R1.1
採購建議用料 22UF/6.3V 0603



2016.02.23
R1.2
Change Xtal capacitance to 10PF.
Improve Driver level and Frequency tolerance

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : VGA_XTAL
BG1-NB4
Engineer: Ryan_Yen

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

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VGA_DISPLAY

LVDS

U7001G
4/14 IFPAB

		NC3	AC4
		NC2	AC3
AA6	NC14	NC5	Y3
		NC4	Y4
V7	NC12	NC7	AA2
W7	NC13	NC6	AA3
		NC9	AA1
		NC8	AB1
		NC11	AA5
		NC10	AA4
		NC17	AB4
		NC16	AB5
W6	NC1	NC19	AB2
Y6	NC15	NC18	AB3
		NC21	AD2
		NC20	AD3
		NC23	AD1
		NC22	AE1
		NC25	AD5
		NC24	AD4
		GPIO14	B3

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02V0A0000038

U7001J
7/14 IFPEF

		NC55	J3
		NC54	J2
J7	NC65	NC64	J1
		NC63	K1
K7	NC66	NC62	K3
		NC61	K2
K6	NC67	NC60	M3
		NC59	M2
		NC58	M1
		NC57	N1
		GPIO18	C2
H6	NC56	NC69	H4
J6	NC70	NC68	H3
		NC78	J5
		NC77	J4
		NC76	K5
		NC75	K4
		NC74	L4
		NC73	L3
		NC72	M5
		NC71	M4
		GPIO19	F7

N16S-GTR-S-A2
02V0A0000038

U7001H
5/14 IFPC

T6	NC39		
M7	NC37	NC27	N5
N7	NC38	NC26	N4
		NC36	N3
		NC35	N2
		NC34	R3
		NC33	R2
		NC32	R1
		NC31	T1
		NC30	T3
		NC29	T2
P6	NC28	GPIO15	C3

N16S-GTR-S-A2
02V0A0000038

U7001I
6/14 IFPD

U6	NC53		
T7	NC52	NC41	P4
R7	NC51	NC40	P3
		NC50	R5
		NC49	R4
		NC48	T5
		NC47	T4
		NC46	U4
		NC45	U3
		NC44	V4
		NC43	V3
R6	NC42	GPIO17	D4

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U7001K
3/14 DACA

	GF117/GM108	GF117	GM108/GK208				
W5	NC87	NC	NC	I2CA_SCL	B7	R7301 1	2 1.8KOHM /VGA
AE2	NC79	TSEN_VREF	NC	I2CA_SDA	A7	R7302 1	2 1.8KOHM /VGA
AF2	NC82	NC	NC	NC80	AE3		
			NC	NC81	AE4		
			NC	NC85	AG3		
			NC	NC84	AF4		
			NC	NC83	AF3		
		GM108 GF117	GK208				

N16S-GTR-S-A2
02V0A0000038

PEGATRON Title : VGA_DISPLAY
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4
Engineer: Ryan_Yen

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

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VGA_GPIO_STRAP

+3VS_VGA → +3VS_VGA 57,75,86,87,91

+3VS_AON_VGA → +3VS_AON_VGA 57,70,72,75,91

GPU DEVICE ID

N16V-GM	N16S-GTR
	0x134D

VRAM CFG--ROM_SI

	256Mx16
SAMSUNG	0x4
HYNIX	0x5

N16S-GT-R Strap Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

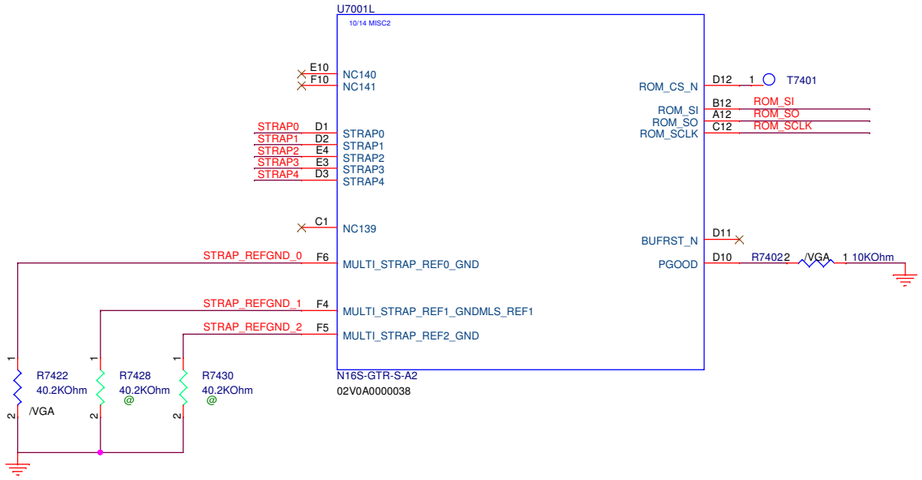
N16S-GTR Multi-Level Mode Strapping

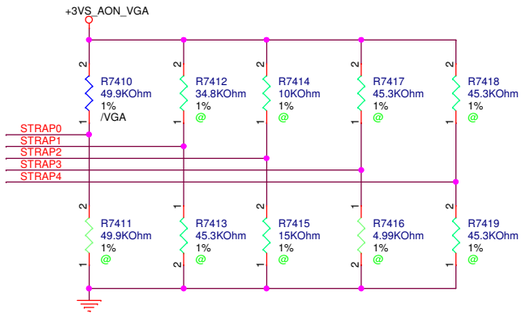
Resistor Values	Bit3	Bit2	Bit1	Bit0
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kohm pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff. /VGA			
STRAP2				
STRAP3				
STRAP4				
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE

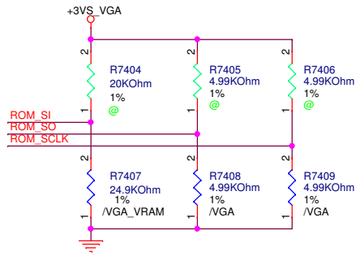
B build GB2B-64(N16V-GM/N16S-GTR)	Hynix	Samsung
DEVICE ID	0x5	0x4
STRAP0	49.9K PU	49.9K PU
STRAP1	Reserved	Reserved
STRAP2	Reserved	Reserved
STRAP3	Reserved	Reserved
STRAP4	Reserved	Reserved
ROM_SCLK	4.99K PD	4.99K PD
ROM_SI	30K PD	24.9K PD
ROM_SO	4.99K PD	4.99K PD

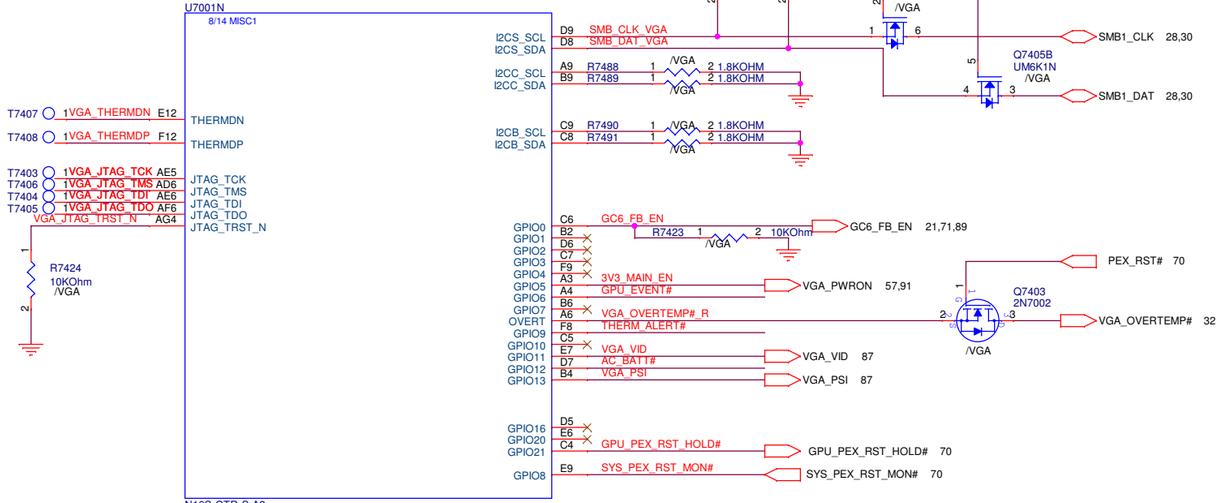
GPIO Definition

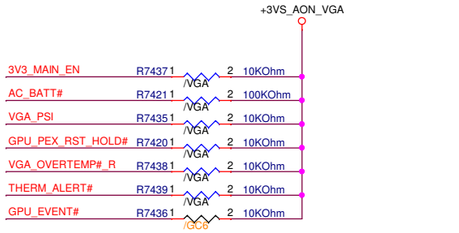
	NV SPEC Standard mode DG_07158_001_V05	P5HCJ
GPIO0	GC6_FB_EN	FB_CLAMP_MON
GPIO1	MEM_VDD_CTL	NC
GPIO2	LCD_BL_PWM	NC
GPIO3	LCD_VCC	NC
GPIO4	LCD_BLEN	NC
GPIO5	3V3_MAIN_EN	GPIO5_PWM_VID_BOOT_EN
GPIO6	GPU_EVENT#	FB_CLAMP_TGL_REQ#
GPIO7	3DVision	NC
GPIO8	SYS_PEX_RST_MON#	VGA_OVERTEMP#
GPIO9	THERM_ALERT	VGA_THERM_ALERT#
GPIO10	MEM_VREF_CTL	NC
GPIO11	PWM_VID	VGA_VID
GPIO12	PWR_LEVEL	AC_BATT#
GPIO13	PSI	VGA_PSI#
GPIO14	HPD_A	
GPIO15	HPD_C	
GPIO16	FRAME_LOCK#	NC
GPIO17	HPD_D	
GPIO18	HPD_E	
GPIO19	HPD_F or HPD_B	
GPIO20	Reserved	NC
GPIO21	GPU_PEX_RST_HOLD#	NC
OVERT	OVERT	

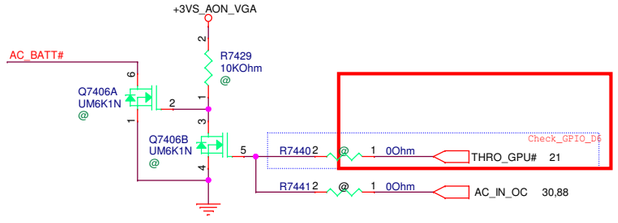


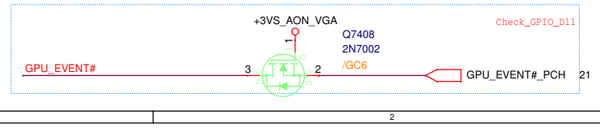












PEGATRON

Title : VGA_GPIO,STRAP

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4

Engineer: Ryan_Yen

Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 74 of 96

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VGA_Power

+3VS_VGA — +3VS_VGA 57,74,86,87,91
+3VS_AON_VGA — +3VS_AON_VGA 57,70,72,74,91
+VGA_VCORE — +VGA_VCORE 57,87
+1.5VS_VGA — +1.5VS_VGA 57,71,76,89

26A

+VGA_VCORE

U7001E
11/14 NVVDD
K10 VDD_01
K12 VDD_02
K14 VDD_03
K16 VDD_04
K18 VDD_05
L11 VDD_06
L13 VDD_07
L15 VDD_08
L17 VDD_09
M10 VDD_10
M12 VDD_11
M14 VDD_12
M16 VDD_13
M18 VDD_14
N11 VDD_15
N13 VDD_16
N15 VDD_17
N17 VDD_18
P10 VDD_19
P12 VDD_20
P14 VDD_21
P16 VDD_22
P18 VDD_23
R11 VDD_24
R13 VDD_25
R15 VDD_26
R17 VDD_27
T10 VDD_28
T12 VDD_29
T14 VDD_30
T16 VDD_31
T18 VDD_32
U11 VDD_33
U13 VDD_34
U15 VDD_35
U17 VDD_36
V10 VDD_37
V12 VDD_38
V14 VDD_39
V16 VDD_40
V18 VDD_41
N16S-GTR-S-A2
02V0A0000038

+VGA_VCORE

C7506 1UF/10V /VGA
C7505 1UF/10V /VGA
C7509 1UF/10V /VGA
C7508 1UF/10V /VGA
GND

C7510 22UF/6.3V /VGA
C7511 22UF/6.3V /VGA
C7512 22UF/6.3V /VGA
C7513 22UF/6.3V /VGA
C7515 22UF/6.3V /VGA
GND

C7523 4.7UF/6.3V /VGA
C7520 4.7UF/6.3V /VGA
C7521 4.7UF/6.3V /VGA
C7524 4.7UF/6.3V /VGA
C7525 4.7UF/6.3V /VGA
C7514 4.7UF/6.3V /VGA
C7516 4.7UF/6.3V /VGA
C7522 4.7UF/6.3V /VGA
C7517 4.7UF/6.3V /VGA
C7518 4.7UF/6.3V /VGA
GND

PLACE UNDER GPU

C7553 22UF/6.3V /VGA
C7552 22UF/6.3V /VGA
C7527 22UF/6.3V /VGA
C7543 4.7UF/16V /VGA
C7544 4.7UF/16V /VGA
C7545 4.7UF/16V /VGA
C7546 4.7UF/16V /VGA
C7547 4.7UF/16V /VGA
CE7501 330UF/2.5V @ vx_c3528_h79
GND

Option caps PLACE NEAR BGA

2016.02.02
R1.2
Change 47 UF x1 to 22 UF x2

2015.11.27
R1.1
採購建議用料 22UF/6.3V 0603

EMI

+VGA_VCORE

C7548 0.1UF/25V /VGA
C7549 0.1UF/25V /VGA
C7550 0.1UF/25V /VGA
C7551 0.1UF/25V /VGA
GND

U7001F
13/14 GND
A2 GND_001 M13
AB17 GND_005 M15
AB20 GND_006 M17
AB24 GND_007 N10
AC2 GND_008 N12
AC22 GND_009 N14
AC26 GND_010 N16
AC5 GND_011 N18
AC8 GND_012 P11
AD12 GND_013 P13
AD13 GND_014 P15
A26 GND_002 P17
AD15 GND_015 P2
AD16 GND_016 P23
AD18 GND_017 P26
AD19 GND_018 P5
AD21 GND_019 R10
AD22 GND_020 R12
AE11 GND_021 R14
AE14 GND_022 R16
AE17 GND_023 R18
AE20 GND_024 T11
AB11 GND_003 T13
AF1 GND_025 T15
AF11 GND_026 T17
AF14 GND_027 U10
AF17 GND_028 U12
AF20 GND_029 U14
AF23 GND_030 U16
AF5 GND_031 U18
AF8 GND_032 U2
AG2 GND_033 U23
AG26 GND_034 U26
AB14 GND_004 U5
B1 GND_035 V11
B11 GND_036 V13
B14 GND_037 V15
B17 GND_038 V17
B20 GND_039 Y2
B23 GND_040 Y23
B27 GND_041 Y26
B5 GND_042 Y5
B8 GND_043
E11 GND_044
E14 GND_045
E17 GND_046
E2 GND_047
E20 GND_048
E22 GND_049
E25 GND_050
E5 GND_051
E8 GND_052
H2 GND_053
H23 GND_054
H25 GND_055
H5 GND_056
K11 GND_057
K13 GND_058
K15 GND_059
K17 GND_060
L10 GND_061
L12 GND_062
L14 GND_063
L16 GND_064
L18 GND_065
L2 GND_066
L23 GND_067
L25 GND_068
L5 GND_069 AA7
M11 GND_070 GND_113 AB7
GND_114
N16S-GTR-S-A2
02V0A0000038
GND GND

1.4A

+1.5VS_VGA

U7001D
12/14 FBVDDQ
B26 FBVDDQ_01
C25 FBVDDQ_02
E23 FBVDDQ_03
E26 FBVDDQ_04
F14 FBVDDQ_05
F21 FBVDDQ_06
G13 FBVDDQ_07
G14 FBVDDQ_08
G15 FBVDDQ_09
G16 FBVDDQ_10
G18 FBVDDQ_11
G19 FBVDDQ_12
G20 FBVDDQ_13
G21 FBVDDQ_14
L22 FBVDDQ_19 FBVDDQ_AON
L24 FBVDDQ_20 FBVDDQ_AON
L26 FBVDDQ_21 FBVDDQ_AON
M21 FBVDDQ_22 FBVDDQ_AON
N21 FBVDDQ_23
R21 FBVDDQ_24
T21 FBVDDQ_25
V21 FBVDDQ_26
W21 FBVDDQ_27

GF117 GF119 GK208
H24 FBVDDQ_AON_1 FBVDDQ
H26 FBVDDQ_AON_2 FBVDDQ
J21 FBVDDQ_AON_3 FBVDDQ
K21 FBVDDQ_AON_4 FBVDDQ

N16S-GTR-S-A2
02V0A0000038

+1.5VS_VGA

C7532 1UF/6.3V /VGA
C7531 1UF/6.3V /VGA
C7526 0.1UF/16V /VGA
C7530 0.1UF/16V /VGA
GND

C7533 4.7UF/6.3V /VGA
C7534 22UF/6.3V /VGA
C7541 4.7UF/6.3V /VGA
GND

PLACE UNDER GPU

C7529 22UF/6.3V @
C7540 100UF/6.3V @
C7542 10UF/6.3V /VGA MLCC 10UF/6.3V (0603)X5R 20%
GND

PLACE NEAR BGA

2016.02.02
R1.2
Change 10 UF from 0805 to 0603

U7001C
14/14 XVDD/VDD33
AD10 NC88 — 3V3_MAIN1 G8
AD7 NC89 — 3V3_MAIN2 G9
GM108: 3V3_AON — 3V3_AON1 G10; 3V3_AON — 3V3_AON2 G12
F11 NC86 FBA_CMD32
V5 FERMI_RSVD1
V6 FERMI_RSVD2

CONFIGURABLE POWER CHANNELS
* nc on substrate

G1 NC142
G2 NC143
G3 NC144
G4 NC145
G5 NC146
G6 NC147
G7 NC148
V1 NC149
V2 NC150
W1 NC151
W2 NC152
W3 NC153
W4 NC154

N16S-GTR-S-A2
02V0A0000038

0.06A

C7507 0.1UF/16V @
C7501 0.1UF/16V /VGA
C7504 0.1UF/16V @
C7502 1UF/6.3V /VGA
C7503 4.7UF/6.3V /VGA
GND

PLACE UNDER GPU
PLACE NEAR GPU

R75012 0Ohm /GC6 — +3VS_VGA
R7530 0Ohm /NGC6

C7538 0.1UF/16V /VGA
C7519 0.1UF/16V @
C7537 0.1UF/16V /VGA
C7539 1UF/6.3V /VGA
C7536 4.7UF/6.3V /VGA
GND

PLACE UNDER GPU
PLACE NEAR GPU

R75052 0Ohm /VGA — +3VS_AON_VGA

FB_CAL_VDDQ — D22 +FB_CAL_PD_VDDQ — R7504 1 /VGA 2 40.2Ohm 1%
FB_CAL_GND — C24 +FB_CAL_PU_GND — R7503 1 /VGA 2 42.2Ohm 1%
FB_CAL_TERM — B25 +FB_CAL_TERM_GND — R7502 1 /VGA 2 51.1Ohm 1%
+1.5VS_VGA
GND
PLACE CLOSE TO GPU BALLS

Function / Feature Reserve	Component mount & un-mount	Verified or not	Note
N16V-GM without GC6 2.0	Mount: R7530 Un-mount: /N16S-GT_GC6	Basic function ok	Power BOM: Un-mount +3VS_VGA load switch schematic
N16S-GT with GC6 2.0	Mount: /N16S-GT_GC6 Un-mount: R7530	Not verify	Power BOM: Mount +3VS_VGA load switch schematic

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : VGA_Power
BG1-NB4
Engineer: Ryan_Yen
Size C | Project Name P5HCJ/Megatron | Rev 1.2
Date: Friday, February 05, 2016 | Sheet 75 of 96

VGA_FBA_DDR3

+1.5VS_VGA → +1.5VS_VGA 57,71,75,89

71 FBAD[0..63]
71 FBADQM[0..7]
71 FBADQS_WP[0..7]
71 FBADQS_RN[0..7]

71 FBA_A[0..14]
71 FBA_ODT[0..1]
71 FBA_CKE[0..1]
71 FBA_CS#[0..1]
71 FBA_BA[0..2]

M2

U7601 — H5TC4G63CFR-N0C — 03V150000089

+1.5VS_VGA — R76011 2 1KOhm /VGA — PLACE NEAR VRAM — C7601 0.01UF/16V /VGA — R7602 1KOhm /VGA

FBA_VREF_CA0 FBA_VREF_DQ0 — VREFCA VREFDQ

FBA_A0 FBA_A1 FBA_A2 FBA_A3 FBA_A4 FBA_A5 FBA_A6 FBA_A7 FBA_A8 FBA_A9 FBA_A10 FBA_A11 FBA_A12 FBA_A13 FBA_A14 — A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14

FBA_BA0 FBA_BA1 FBA_BA2 — BA0 BA1 BA2

71 FBA_CLK0 — CK
71 FBA_CLK0# — CK#
FBA_CKE0 — CKE

FBA_ODT0 — ODT
FBA_CS#0 — CS#
FBA_RAS# — RAS#
FBA_CAS# — CAS#
FBA_WE# — WE#

FBADQS_WP0 — DQSL
FBADQS_WP2 — DQSU

FBADQM0 — DML
FBADQM2 — DMU

FBADQS_RN0 — DQSL#
FBADQS_RN2 — DQSU#

FBA_RST# — RESET#

ZQ — R7605 243Ohm /VGA 1%

NC1 NC2 NC3 NC4 NC5 — J1 L1 J9 L9 M7

DQ0–DQ31 — FBAD3 FBAD5 FBAD2 FBAD7 FBAD0 FBAD6 FBAD1 FBAD4 FBAD16 FBAD21 FBAD17 FBAD20 FBAD22 FBAD19 FBAD23 FBAD18

Byte 0 **Byte 2**

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 — N1 R1 B2 K2 G7 K8 D9 N9 R9

C7604 C7605 0.1UF/16V /VGA

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 — A1 C1 F1 D2 H2 A8 C9 E9 H9

C7610 C7611 C7612 C7613 1UF/6.3V /VGA

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 — E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9

VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 — B1 D1 G1 E2 D8 E8 B9 F9 G9

PLACE NEAR U7601

R7608 2 162Ohm 1 /VGA — R7619 80.6KOhm @ — R7620 80.6KOhm @ — C7639 10NF/25V @ — PLACE NEAR VRAM

M1

U7602 — H5TC4G63CFR-N0C — 03V150000089

+1.5VS_VGA — R76031 2 1KOhm /VGA — PLACE NEAR VRAM — C7602 0.01UF/16V /VGA — R7604 1KOhm /VGA

FBA_VREF_CA0 FBA_VREF_DQ0 — VREFCA VREFDQ

FBA_A0 FBA_A1 FBA_A2 FBA_A3 FBA_A4 FBA_A5 FBA_A6 FBA_A7 FBA_A8 FBA_A9 FBA_A10 FBA_A11 FBA_A12 FBA_A13 FBA_A14 — A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14

FBA_BA0 FBA_BA1 FBA_BA2 — BA0 BA1 BA2

FBA_CLK0 FBA_CLK0# — CK CK#
FBA_CKE0 — CKE

FBA_ODT0 — ODT
71 FBA_RAS# — CS# RAS#
71 FBA_CAS# — CAS#
71 FBA_WE# — WE#

FBADQS_WP1 — DQSL
FBADQS_WP3 — DQSU

FBADQM1 — DML
FBADQM3 — DMU

FBADQS_RN1 — DQSL#
FBADQS_RN3 — DQSU#

71 FBA_RST# — RESET#

ZQ — R7606 243Ohm /VGA 1%

NC1 NC2 NC3 NC4 NC5 — J1 L1 J9 L9 M7

DQ0–DQ31 — FBAD8 FBAD13 FBAD11 FBAD14 FBAD9 FBAD15 FBAD10 FBAD12 FBAD29 FBAD27 FBAD30 FBAD25 FBAD28 FBAD26 FBAD31 FBAD24

Byte 1 **Byte 3**

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 — N1 R1 B2 K2 G7 K8 D9 N9 R9

C7606 C7607 0.1UF/16V /VGA

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 — A1 C1 F1 D2 H2 A8 C9 E9 H9

C7608 C7609 C7614 C7615 1UF/6.3V /VGA

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 — E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9

VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 — B1 D1 G1 E2 D8 E8 B9 F9 G9

PLACE NEAR U7602

M4

U7603 — H5TC4G63CFR-N0C — 03V150000089

+1.5VS_VGA — R76131 2 1KOhm /VGA — PLACE NEAR VRAM — C7625 0.01UF/16V /VGA — R7614 1KOhm /VGA

FBA_VREF_CA1 FBA_VREF_DQ1 — VREFCA VREFDQ

FBA_A0 FBA_A1 FBA_A2 FBA_A3 FBA_A4 FBA_A5 FBA_A6 FBA_A7 FBA_A8 FBA_A9 FBA_A10 FBA_A11 FBA_A12 FBA_A13 FBA_A14 — A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14

FBA_BA0 FBA_BA1 FBA_BA2 — BA0 BA1 BA2

71 FBA_CLK1 — CK
71 FBA_CLK1# — CK#
FBA_CKE1 — CKE

FBA_ODT1 — ODT
FBA_CS#1 — CS#
FBA_RAS# — RAS#
FBA_CAS# — CAS#
FBA_WE# — WE#

FBADQS_WP5 — DQSL
FBADQS_WP4 — DQSU

FBADQM5 — DML
FBADQM4 — DMU

FBADQS_RN5 — DQSL#
FBADQS_RN4 — DQSU#

FBA_RST# — RESET#

ZQ — R7617 243Ohm /VGA 1%

NC1 NC2 NC3 NC4 NC5 — J1 L1 J9 L9 M7

DQ0–DQ31 — FBAD41 FBAD44 FBAD40 FBAD45 FBAD42 FBAD47 FBAD43 FBAD46 FBAD32 FBAD36 FBAD34 FBAD37 FBAD33 FBAD38 FBAD35 FBAD39

Byte 5 **Byte 4**

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 — N1 R1 B2 K2 G7 K8 D9 N9 R9

C7636 C7627 0.1UF/16V /VGA

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 — A1 C1 F1 D2 H2 A8 C9 E9 H9

C7630 C7637 C7633 C7634 1UF/6.3V /VGA

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 — E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9

VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 — B1 D1 G1 E2 D8 E8 B9 F9 G9

PLACE NEAR U7603

R7611 2 162Ohm 1 /VGA — R7621 80.6KOhm @ — R7622 80.6KOhm @ — C7640 10NF/25V @ — PLACE NEAR VRAM

M3

U7604 — H5TC4G63CFR-N0C — 03V150000089

+1.5VS_VGA — R76151 2 1KOhm /VGA — PLACE NEAR VRAM — C7626 0.01UF/16V /VGA — R7616 1KOhm /VGA

FBA_VREF_CA1 FBA_VREF_DQ1 — VREFCA VREFDQ

FBA_A0 FBA_A1 FBA_A2 FBA_A3 FBA_A4 FBA_A5 FBA_A6 FBA_A7 FBA_A8 FBA_A9 FBA_A10 FBA_A11 FBA_A12 FBA_A13 FBA_A14 — A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC# A13 A14

FBA_BA0 FBA_BA1 FBA_BA2 — BA0 BA1 BA2

FBA_CLK1 FBA_CLK1# — CK CK#
FBA_CKE1 — CKE

FBA_ODT1 — ODT
FBA_CS#1 — CS#
FBA_RAS# — RAS#
FBA_CAS# — CAS#
FBA_WE# — WE#

FBADQS_WP6 — DQSL
FBADQS_WP7 — DQSU

FBADQM6 — DML
FBADQM7 — DMU

FBADQS_RN6 — DQSL#
FBADQS_RN7 — DQSU#

FBA_RST# — RESET#

ZQ — R7618 243Ohm /VGA 1%

NC1 NC2 NC3 NC4 NC5 — J1 L1 J9 L9 M7

DQ0–DQ31 — FBAD48 FBAD53 FBAD49 FBAD55 FBAD50 FBAD54 FBAD51 FBAD52 FBAD59 FBAD61 FBAD58 FBAD60 FBAD57 FBAD63 FBAD56 FBAD62

Byte 6 **Byte 7**

VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 — N1 R1 B2 K2 G7 K8 D9 N9 R9

C7628 C7629 0.1UF/16V /VGA

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 — A1 C1 F1 D2 H2 A8 C9 E9 H9

C7631 C7632 C7635 C7638 1UF/6.3V /VGA

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 — E1 M1 P1 T1 J2 B3 G8 J8 A9 M9 P9 T9

VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9 — B1 D1 G1 E2 D8 E8 B9 F9 G9

PLACE NEAR U7604

Title : VGA_FBA_DDR3

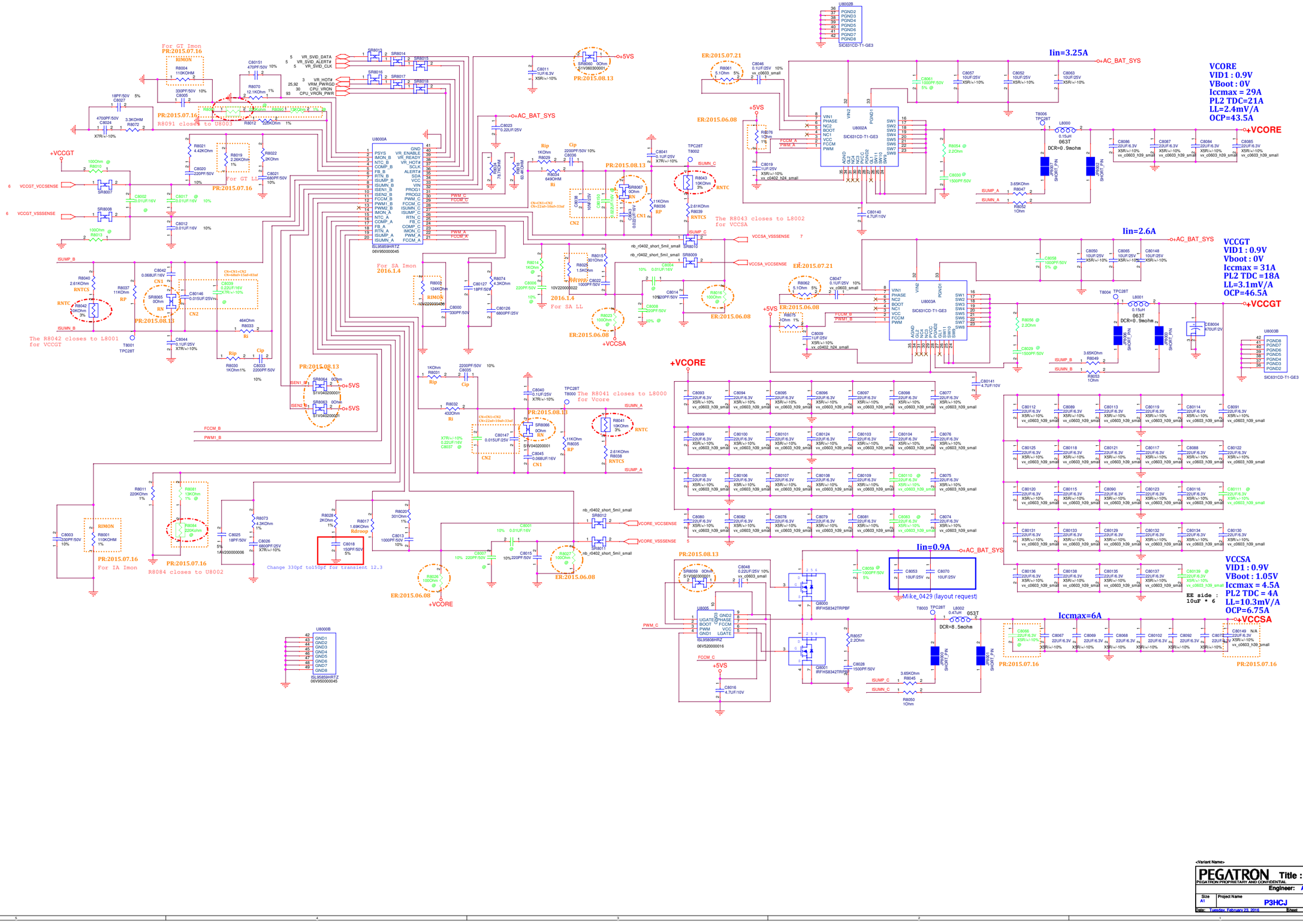
BG1-NB4

Engineer: Ryan_Yen

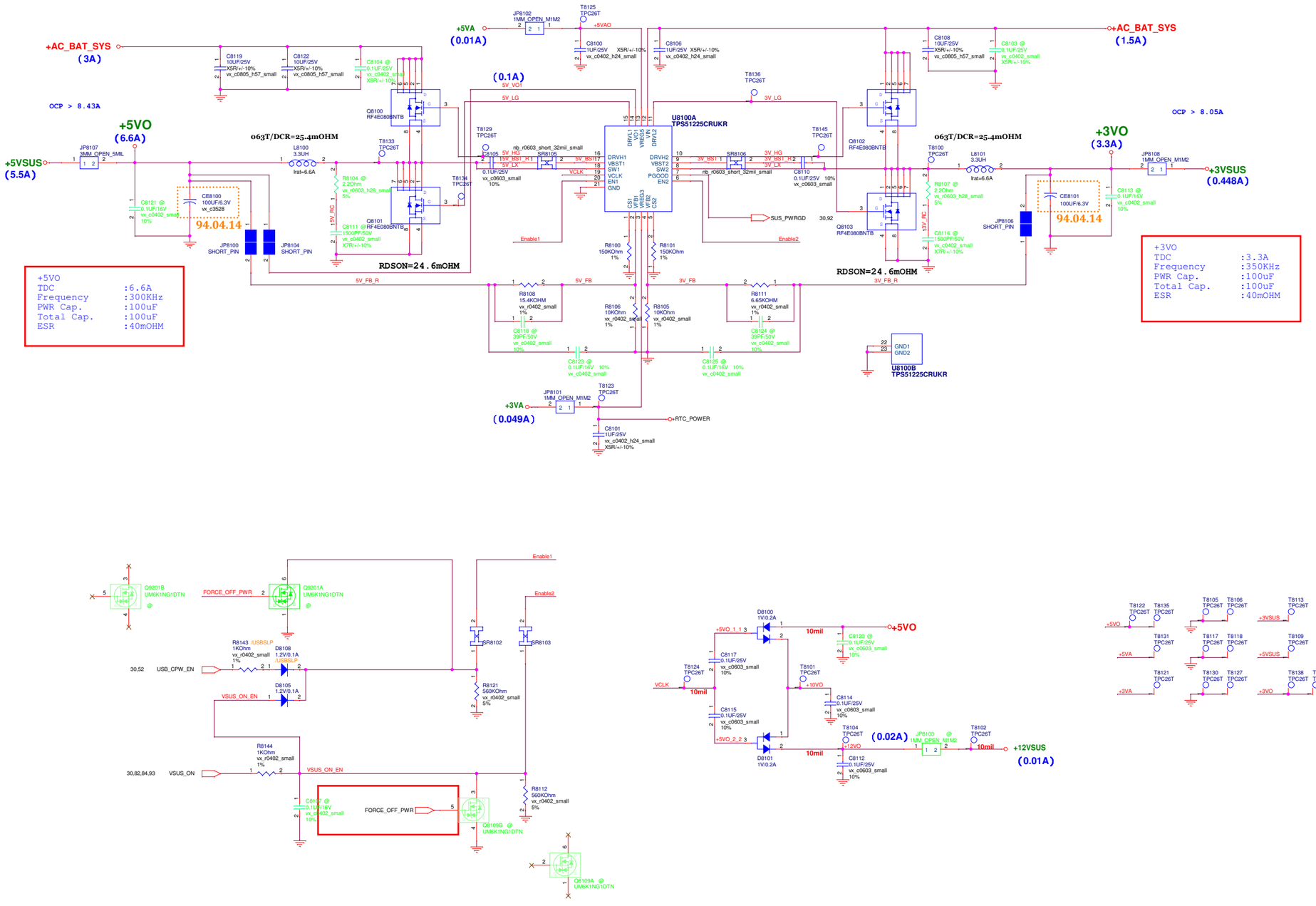
Size	Project Name	Rev
C	P5HCJ/Megatron	1.2

Date: Friday, February 05, 2016 Sheet 76 of 96

Vcore Power Supply



+5VO & +3VO POWER SUPPLY



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_SYSTEM

Engineer: Benson Lin

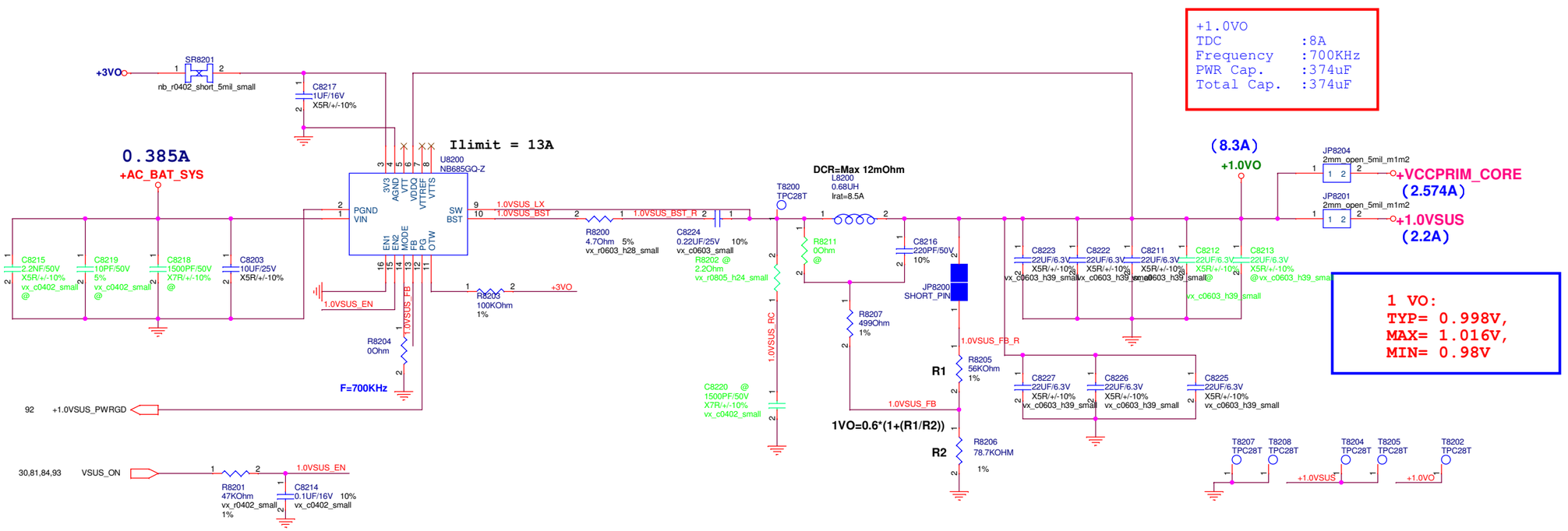
BG1-POWER

Size	Project Name	Rev
Custom	P5HCJ	2.0

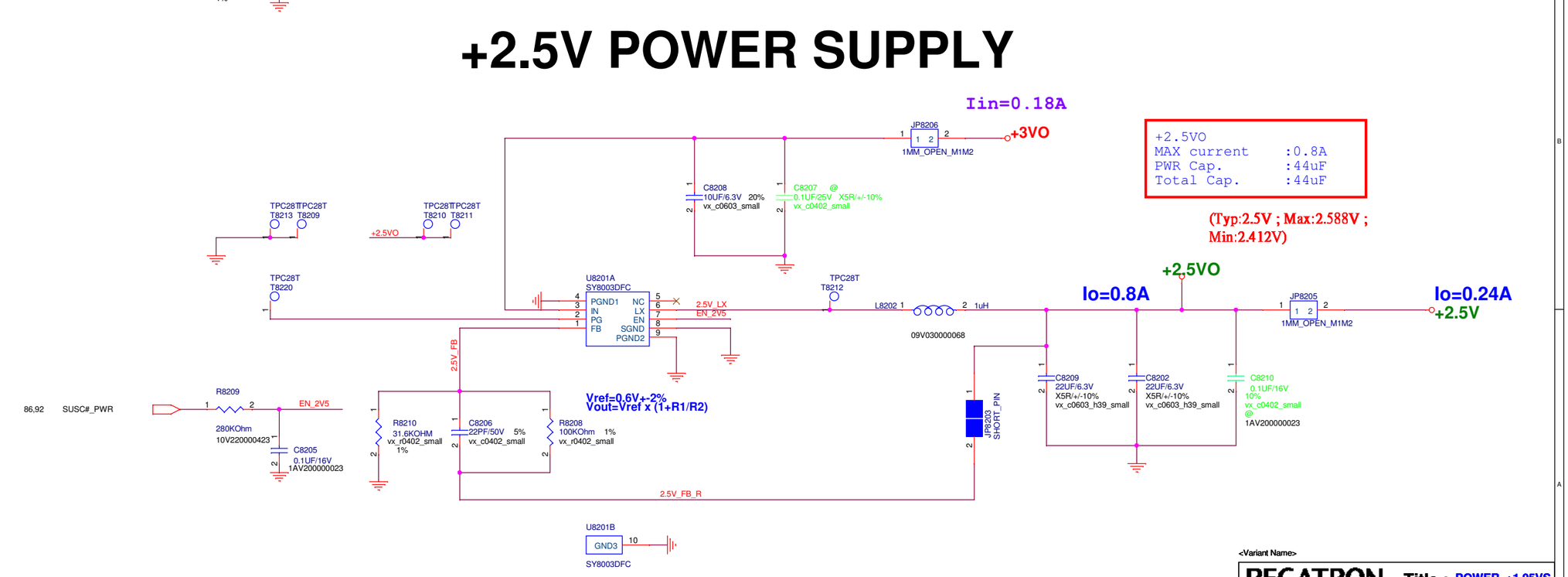
Date: Tuesday, February 23, 2016 Sheet 81 of 94

82

+1.0VSUS POWER SUPPLY



+2.5V POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_+1.05VS

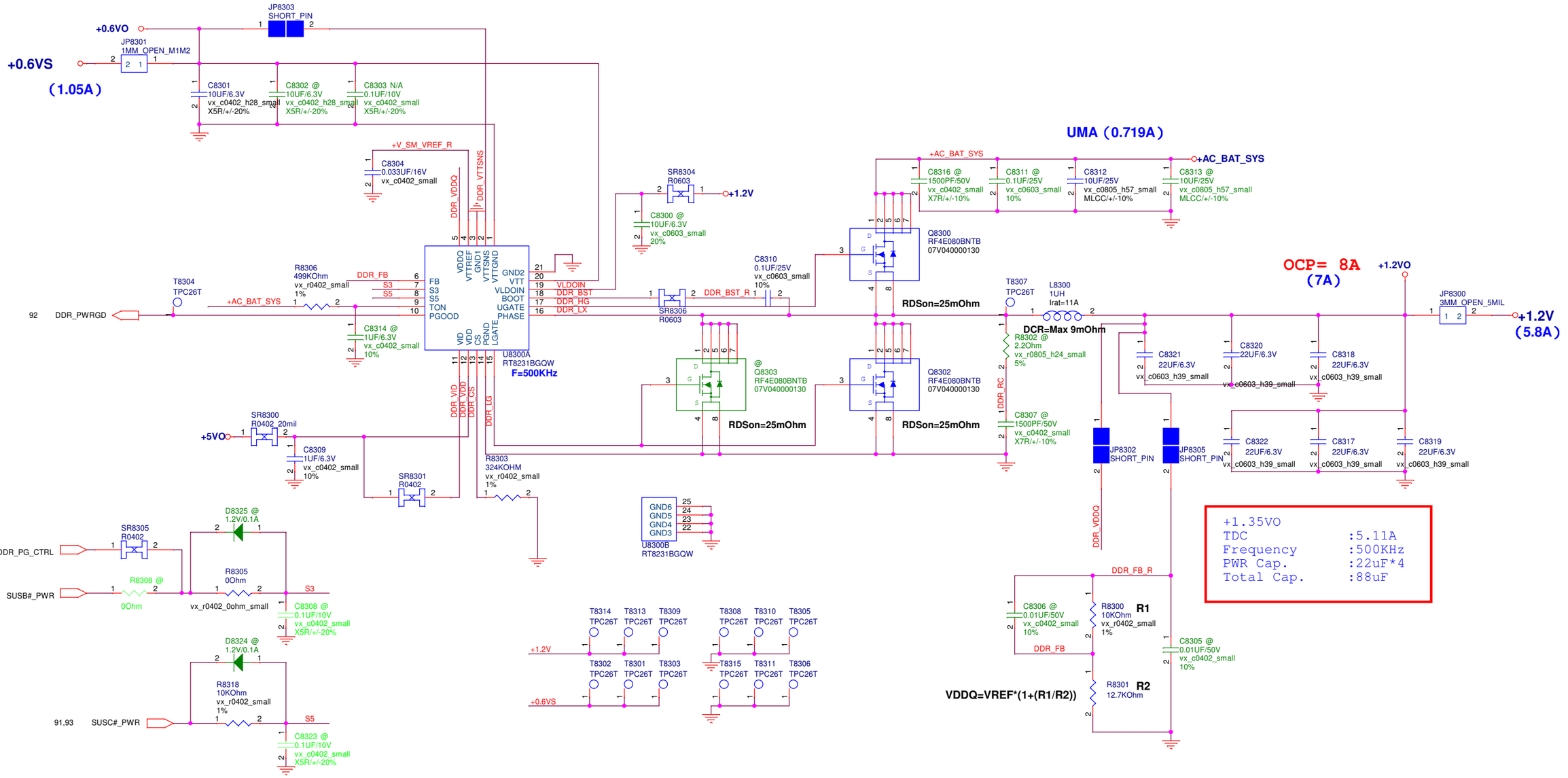
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	P5HCJ	1.0

Date: Tuesday, February 23, 2016 Sheet 82 of 96

DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_DDR & VTT

Engineer: Benson Lin

BG1-POWER

Size	Project Name	Rev
Custom	P5HCJ	2.0

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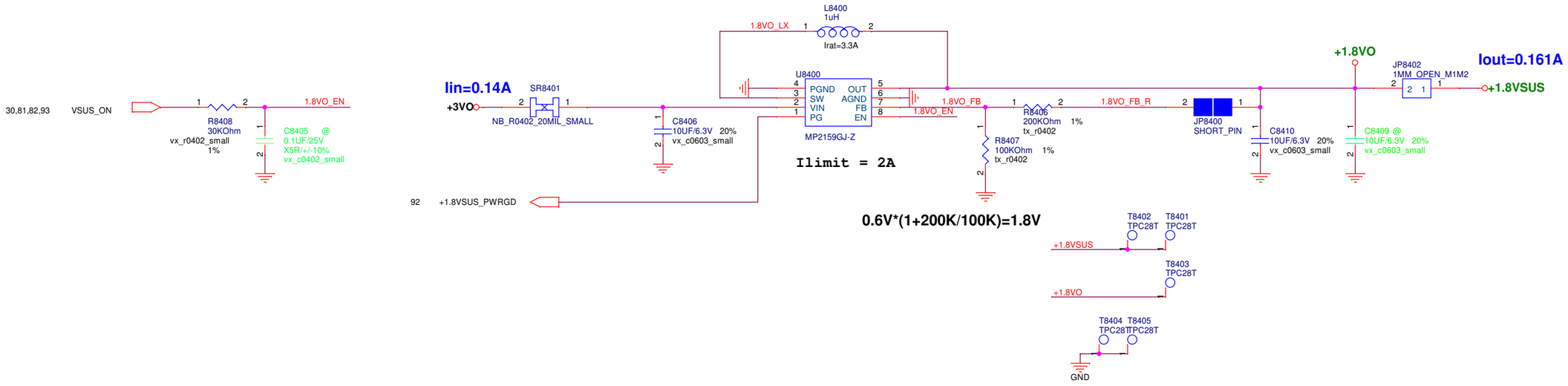
84

1.8VSUS POWER SUPPLY



<Variant Name>

PEGATRON Title : PAGE 84 POWER 1

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Neil_Lin

Size	Project Name	Rev
Custom	P5HCJ	1.0

Date: Tuesday, February 23, 2016 Sheet 84 of 96

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+1.05VS_VGA POWER SUPPLY

+1.05VS_VGA
DC Tolerance :+-30mV
Transient noise tolerance: 100mV pk-pk within 20MHz BW

+3VS_VGA

R8604 /VGA
10KOhm 1%
vx_r0402_small

89 1.05VS_VGA_PWRGD

12.11 上:DIODE, 加速en low

D8601
1.2V/0.1A
/VGA

R2.0

87,89,91 DGPU_EN_PWR

SR8600
nb_r0402_0ohm_short_5mil_small
/VGA

R8601 /VGA
100KOhm
vx_r0402_small

1V05_EN

R8602 @
0Ohm
vx_r0402_0ohm_small

21,87,89 DGPU_PWROK

C8612 /VGA
0.033UF/16V
vx_c0402_small
10%

SR8601
nb_r0603_short_32mil_small

+3VO

(0.3A)

C8622 /VGA
10UF/6.3V
vx_c0603_small
20%

C8608 @ /VGA
0.1UF/16V
vx_c0402_small
10%

2520/DCR_MAX:43mOhm

1V05_VIN
1V05_FB
1V05_LX
1V05_EN

U8600A/VGA
SY8003DFC

PGND1 NC
IN LX
PG EN
FB SGND
PGND2

U8600B/VGA
SY8003DFC
GND3

R8606 /VGA
100KOhm
vx_r0402_small
1%

C8618 /VGA
22PF/50V
vx_c0402_small
5%

R8610 /VGA
75KOhm 1%
vx_r0402_small

1V05_FB_R

Vout=FB * (1+ (R8610 / R8606))
VFB=0.6V;T=2%

T8613
TPC28T

L8600 /VGA
1uH
Irat=3.3A

R8603 @
2.2Ohm
vx_r0603_h28_small
5%

1V05_RC1

C8603 @
1500PF/50V
vx_c0402_small
MLCC/+/-10%

JP8602
SHORT_PIN
/VGA

+1.05VO_VGA
(0.8A)

C8617 /VGA
22UF/6.3V
vx_c0603_h39_small
X5R/+/-10%

C8600 /VGA
22UF/6.3V
vx_c0603_h39_small
X5R/+/-10%

C8601 @
22UF/6.3V
vx_c0603_h39_small
X5R/+/-10%

C8610 @
0.1UF/16V
vx_c0402_small
10%

JP8601
1MM_OPEN_M1M2
/VGA

+1.05VS_VGA
(0.8A)

+1.05VA_VGA
TDC :0.79A / 1.48A
Dyn :2.11A
EDC :2.09A / 1.74A

+1.05VA_VGA
TDC :0.79A
Frequency :1MHz
PWR Cap. :44uF
EE Cap :
Total Cap. :44uF

TPC28T T8617
+1.05VO_VGA
/VGA

TPC28T T8610
+1.05VS_VGA
/VGA

TPC28T T8616
TPC28T T8615
/VGA /VGA

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : +1.05VS_VGA

Engineer: Adams Lin

Size	Project Name	Rev
Custom	P5HCJ	2.1

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87

VGA_CORE POWER SUPPLY

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

	N16	N16S_GT
R8723	39K	20K
R8721	39K	20K
R8716	1.5K	2K
R8713	31.5K	18K
C8720	>1.8nF	2.7nF
Vstep	6.25mV	6.25mV
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.875V	0.9V
openVR Config	A	B

+VGA_VCORE(Package type:N16VS-GT)
DC Tolerance :+-20mV

Overshoot/undershoot
Transient noise tolerance: -10% ~ +20% within 20MHz BW
High frequency noise: 400mV pk-pk within 1GHz BW

VID:0.6V ~ 1.2V
Number of programmable Volt: 96 levels
Programmable volt steps: 6.25mV
Settling Time: < 100us for rising, no restriction on falling

+VGA_VCORE (2 Phase)
TDC :30A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

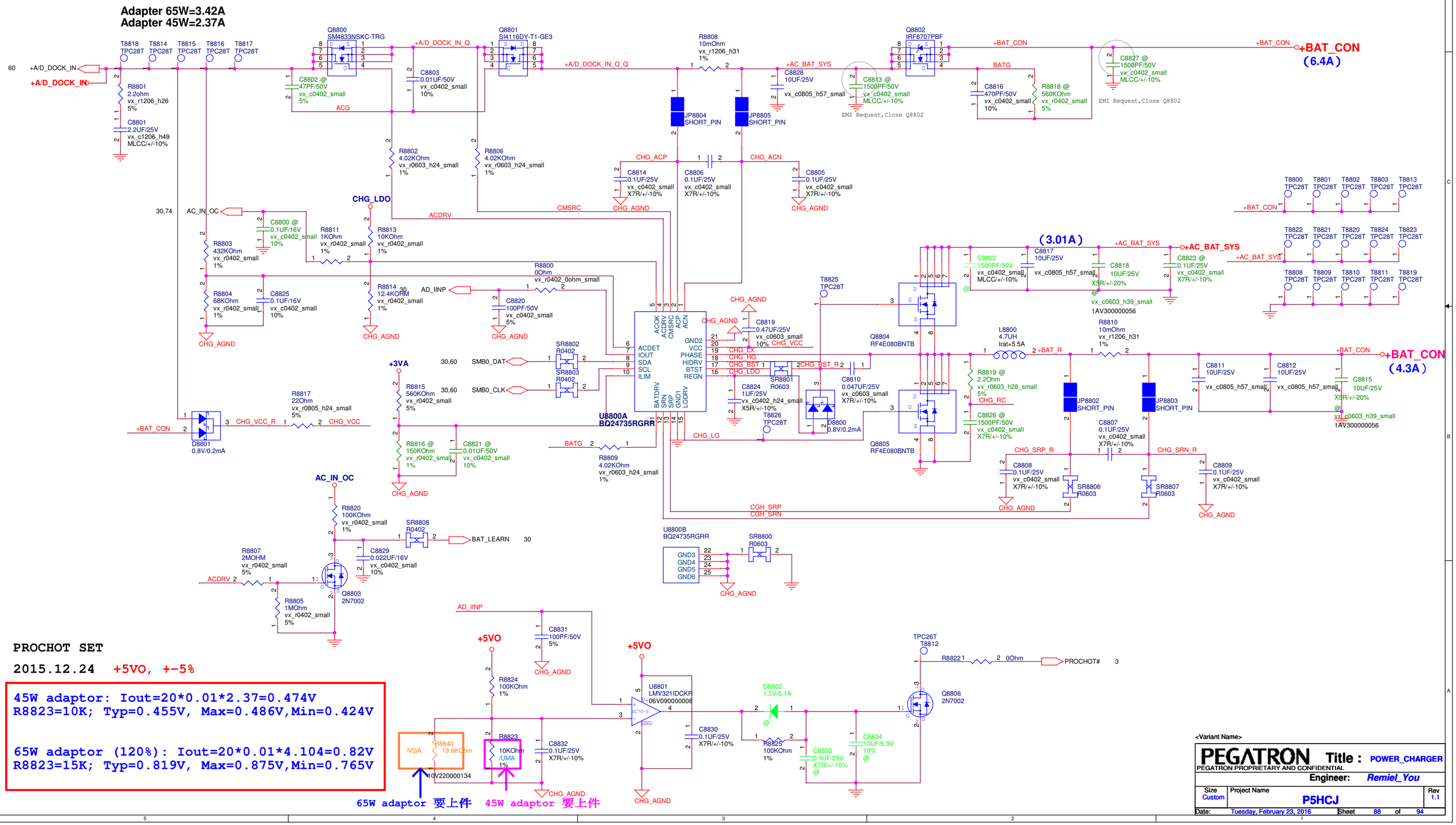
2 PHASE 25W
N16S-GT
EDP=51A
TDC=26A
DYN= A
OCP:62A

EE side pull high OHM check

<Variant Name>

PEGATRON Title : +VGA_VCORE
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: Remiel_You
Size: Custom | Project Name: P5HCJ | Rev: 2.1
Date: Tuesday, February 23, 2016 | Sheet 87 of 99

BATTERY CHARGER



PROCHOT SET

2015.12.24 +5VO, +-5%

45W adaptor: Iout=20*0.01*2.37=0.474V
R8823=10K; Typ=0.455V, Max=0.486V,Min=0.424V

65W adaptor (120%): Iout=20*0.01*4.104=0.82V
R8823=15K; Typ=0.819V, Max=0.875V,Min=0.765V

65W adaptor 要上件 45W adaptor 要上件

<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_CHARGER
Engineer: Remiel_You

Size	Project Name	Rev
Custom	P5HCJ	1.1

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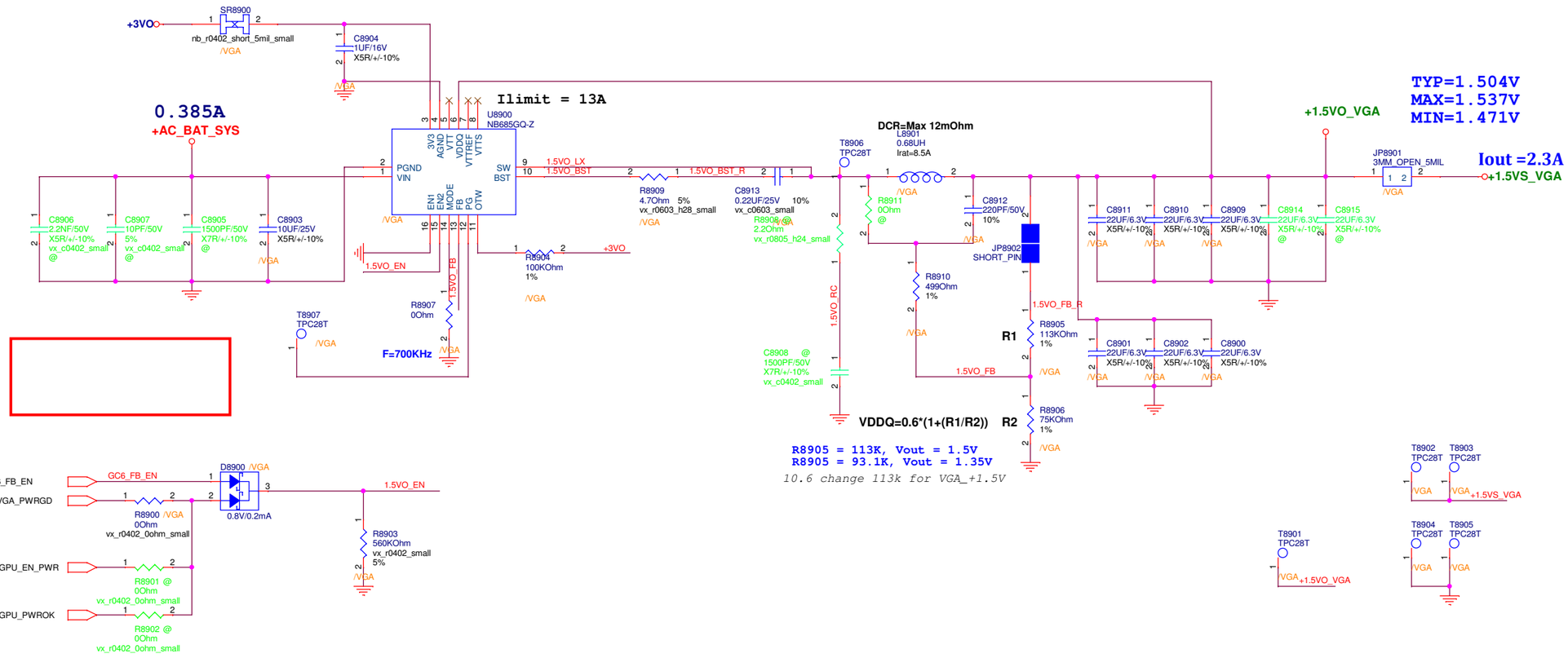
+1.5VS_VGA POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_+1.05VS

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Remiel_You

Size	Project Name	Rev
Custom	P5HCJ	1.2

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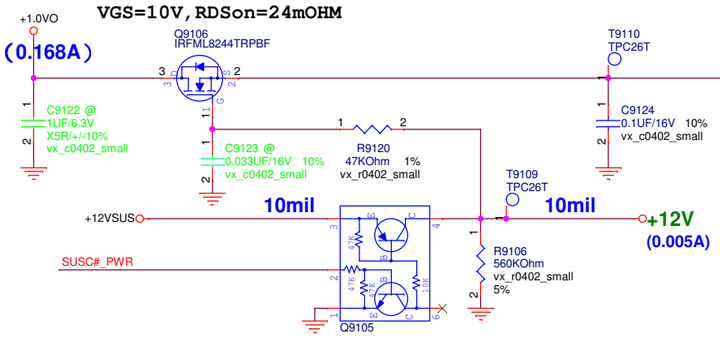
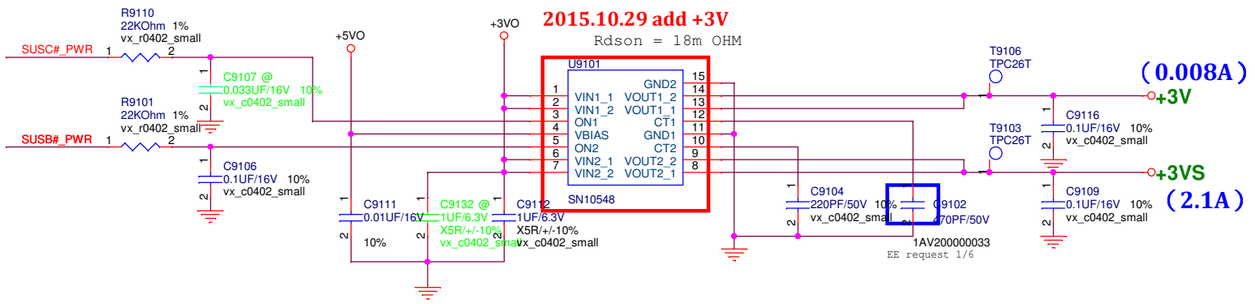
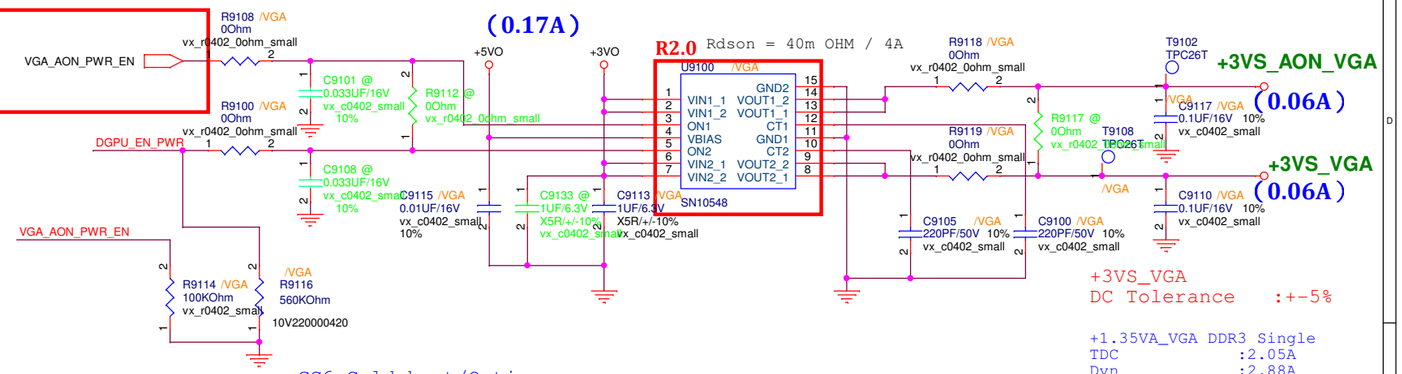
SUSC#_PWR POWER

SUSB#_PWR POWER







+3VS_VGA
DC Tolerance :+-5%

+1.35VA_VGA DDR3 Single
TDC :2.05A
Dyn :2.88A
EDC :3.62A

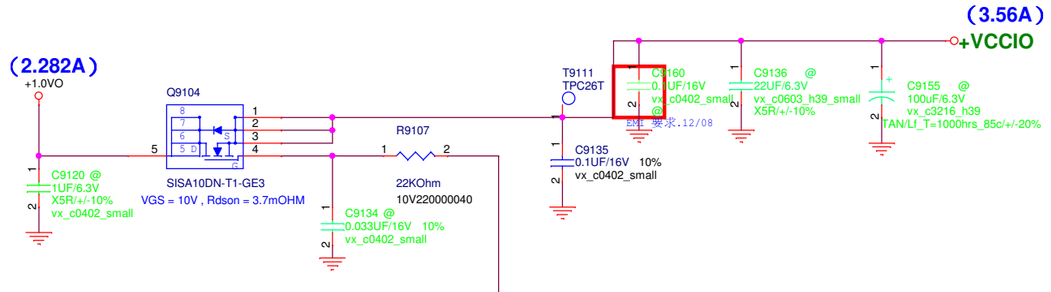
+1.35VA_VGA DDR3 Dual
TDC :2.75A
Dyn :4.14A
EDC :4.22A

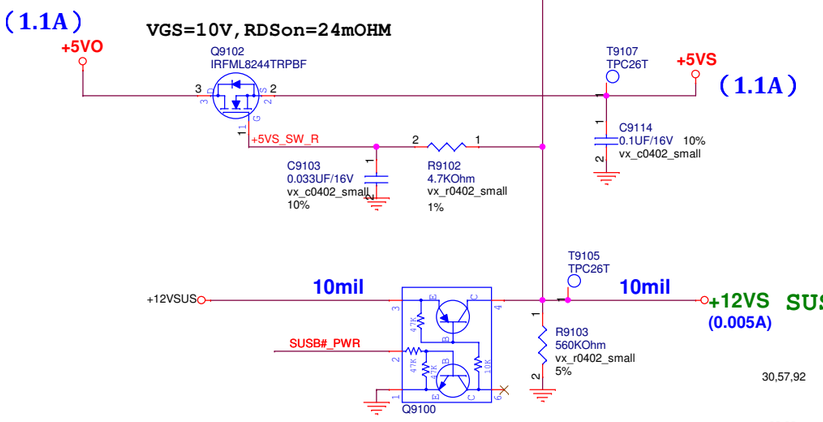
GC6 Cold boot/Optimus:
3V3_AON & 3V3_MAIN --> NVVDD --> PEX_VDD --> FBVDD/Q

GC6 2.0 Exit:
3V3_MAIN --> NVVDD --> PEX_VDD

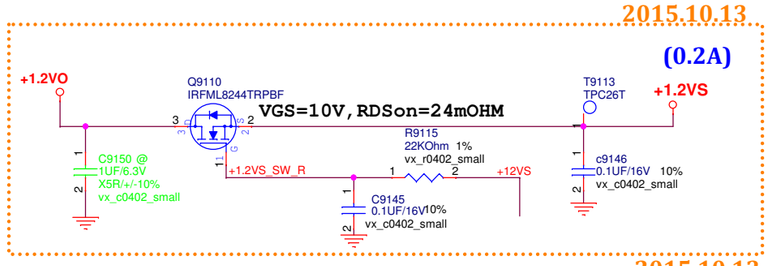
Power up Sequencing
1.The ramp time for any rail must be more 40us and
is recommended to be less than 2ms
2.The previous power rail must ramp up to 90%
before the next power rail can start ramping up

Power down Sequencing
1.There is no specific power down sequence
2.Residual voltage from power down must not violate ther power up sequence
when back to back GPU power down and power up event take place

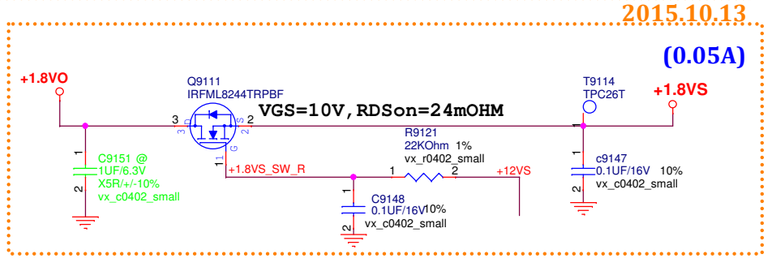




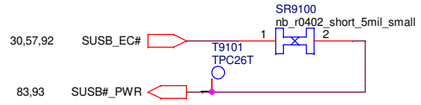
2015.10.13



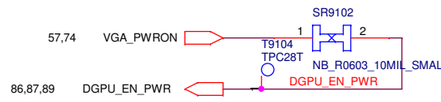
2015.10.13



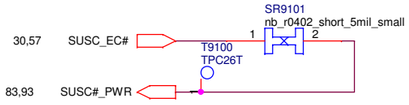
SUSB#_PWR POWER Control



DSC_VGA_PWR POWER Control



SUSC#_PWR POWER Control



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Remiel_You

Size	Project Name	Rev
Custom	P5HCJ	1.2

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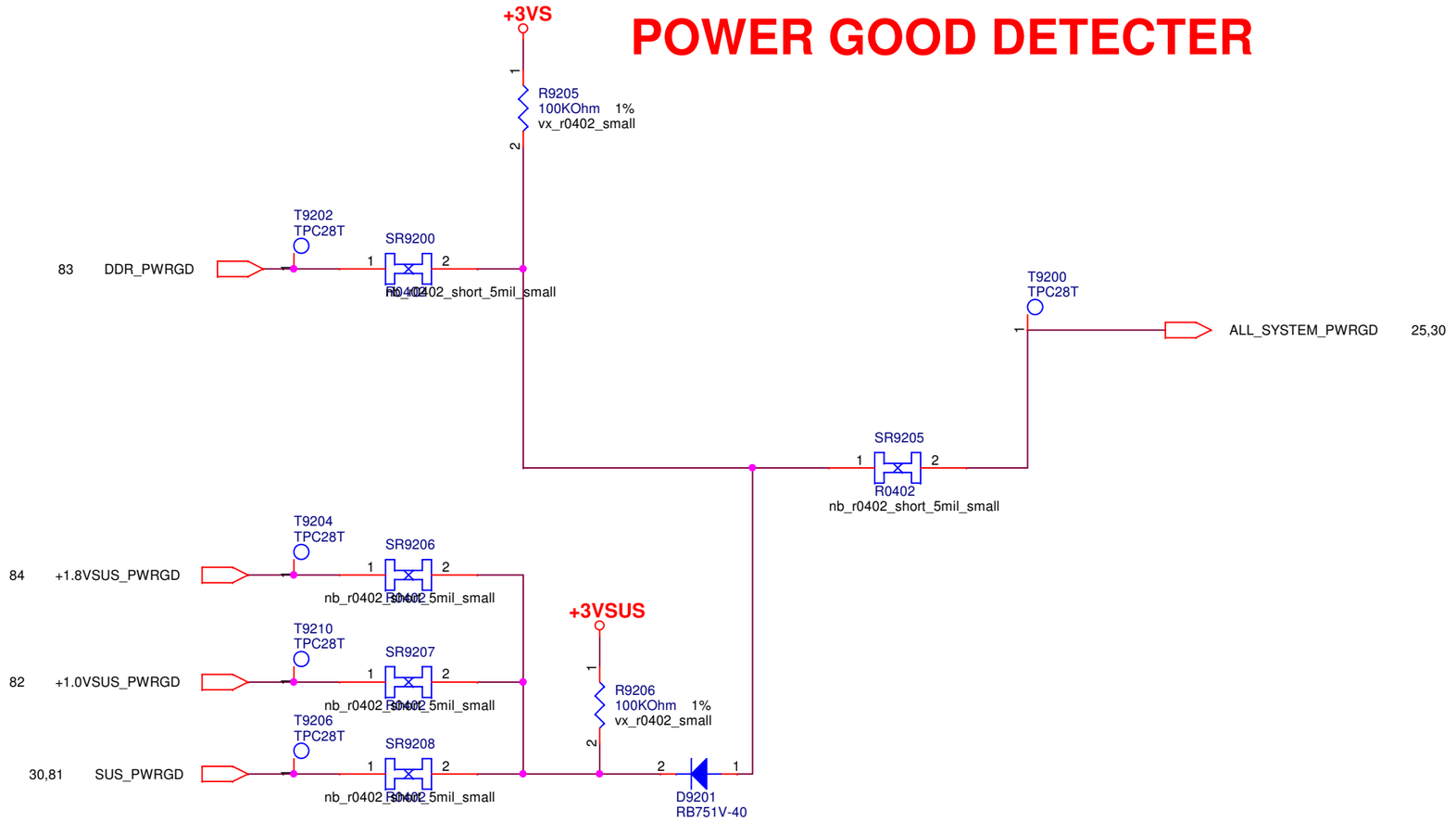
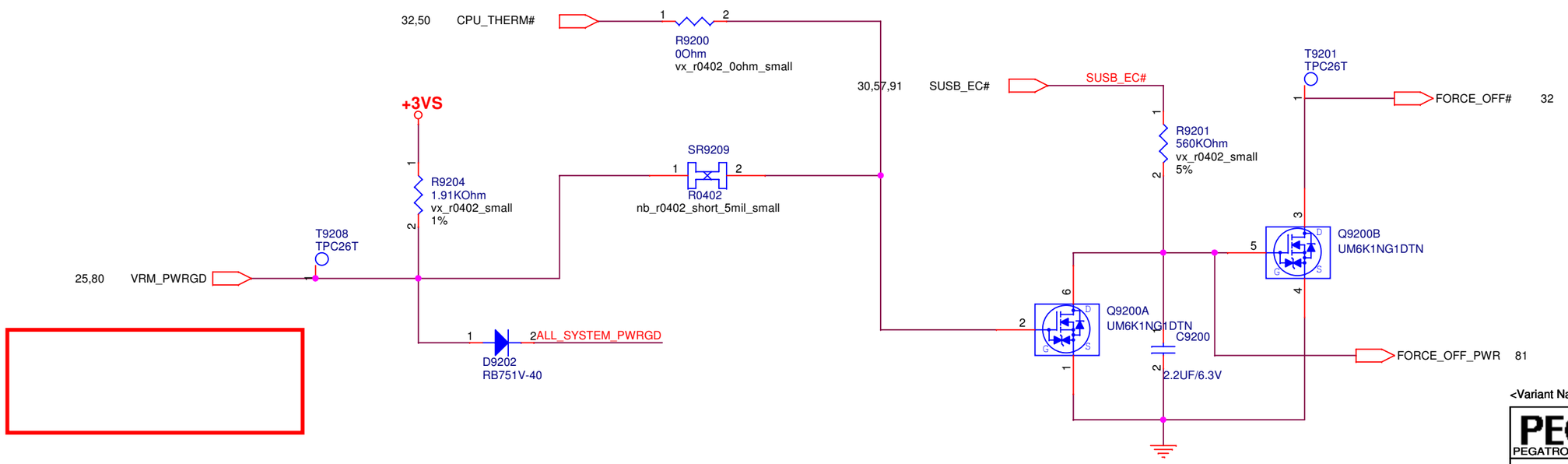
POWER GOOD DETECTER





<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: Remiel_You

Size	Project Name	Rev
Custom	P5HCJ	1.0

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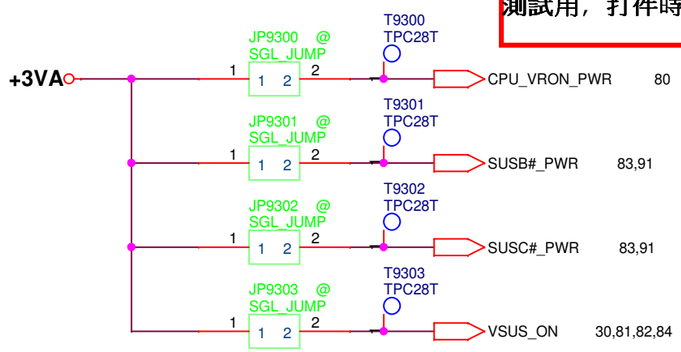
+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,87,88,89

+BAT_CON → +BAT_CON 60,88
+RTC_POWER → +RTC_POWER 81
+5VA → +5VA 64,81
+3VA → +3VA 21,24,30,31,36,53,57,60,64,81,88
+5VO → +5VO 81,83,88,91
+3VO → +3VO 81,82,84,86,89,91
+1.8VO → +1.8VO 84,91
+1.5VO_VGA → +1.5VO_VGA 89
+1.2VO → +1.2VO 83
+1.0VO → +1.0VO 82,91
+0.6VO → +0.6VO 83
+12VSUS → +12VSUS 28,81,91
+5VSUS → +5VSUS 13,52,64,81
+3VSUS → +3VSUS 4,21,24,25,26,28,30,31,51,53,62,81,92
+1.8VSUS → +1.8VSUS 9,26,84
+1.0VSUS → +1.0VSUS 26,82
+12V → +12V 57,91
+3V → +3V 25,31,57,58,64,91
+1.2V → +1.2V 4,7,16,17,18,19,57,83
+1.0V → +1.0V 7,57,91
+12VS → +12VS 28,31,48,57,91
+5VS → +5VS 31,36,45,48,50,51,57,80,87,91
+3VS → +3VS 3,4,18,20,21,22,23,24,28,30,31,32,36,44,45,48,50,51,53,57,58,59,62,64,91,92
+1.8VS → +1.8VS 21,36,57,91
+1.5VS_VGA → +1.5VS_VGA 57,71,75,76,89

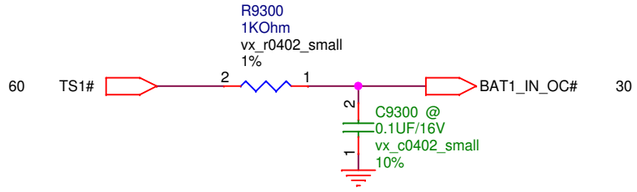
+0.6VS → +0.6VS 15,18,57,83
+VCORE → +VCORE 5,80
+VCCGT → +VCCGT 6,80
+VCCIO → +VCCIO 3,7,9,91
+VCCSA → +VCCSA 7,80
+VCCPRIM_CORE → +VCCPRIM_CORE 26,82

FOR POWER TEST

測試用，打件時 JUMP 不要用錫短路



BATTERY IN DETECT



PEGATRON PROPRIETARY AND CONFIDENTIAL

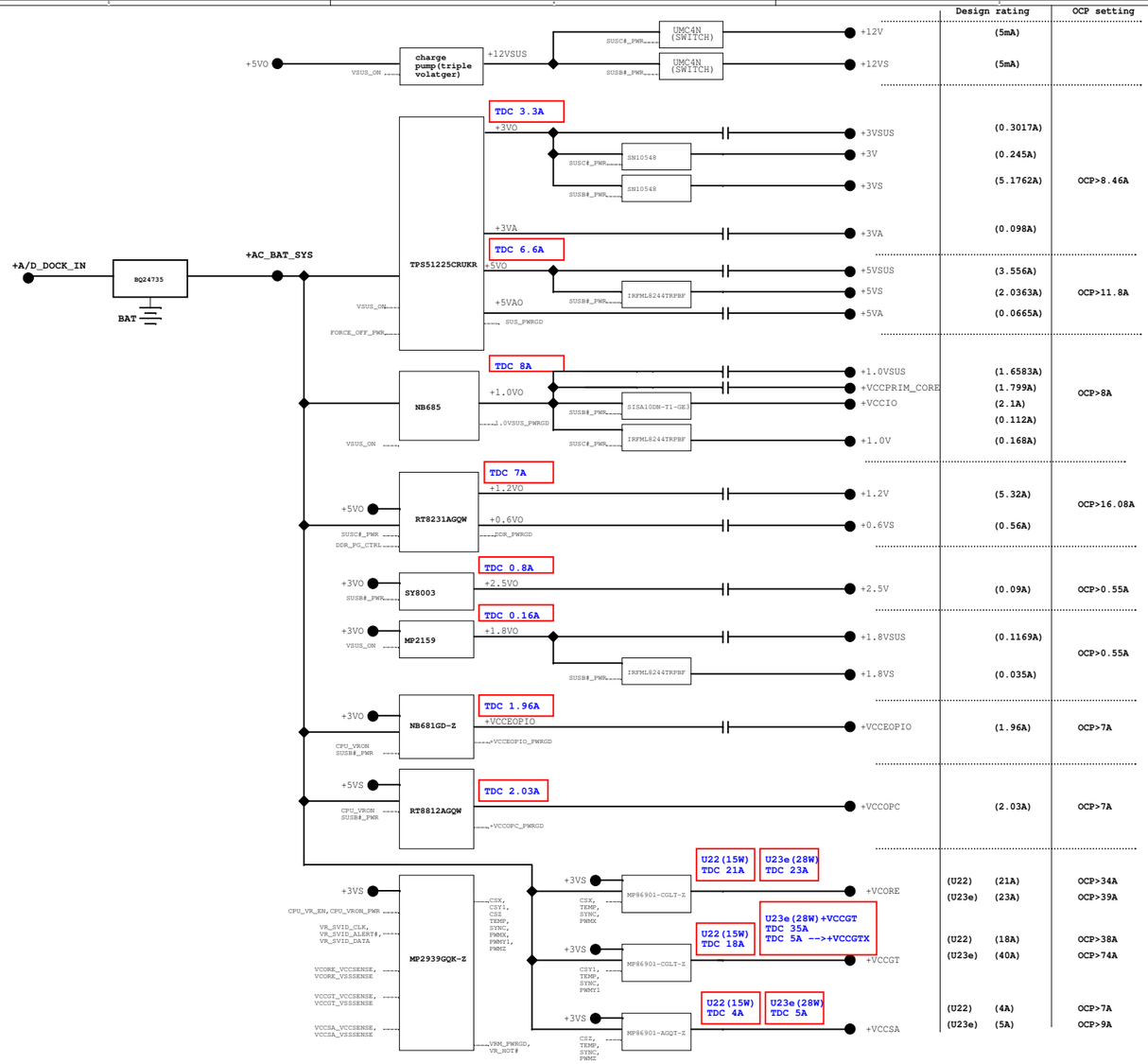
Title : POWER_SIGNAL

BG1-POWER

Engineer: Mike_Ke

Size	Project Name	Rev
B	P5HCJ	1.0

Date: Tuesday, February 23, 2016 Sheet 93 of 94



	Design rating		OCP setting
+12V	(5mA)		
+12VS	(5mA)		
+3VSUS	(0.3017A)		
+3V	(0.245A)		
+3VS	(5.1762A)		OCP>8.46A
+3VA	(0.098A)		
+5VSUS	(3.556A)		
+5VS	(2.0363A)		OCP>11.8A
+5VA	(0.0665A)		
+1.0VSUS	(1.6583A)		
+VCCPRIM_CORE	(1.799A)		OCP>8A
+VCCIO	(2.1A)		
	(0.112A)		
+1.0V	(0.168A)		
+1.2V	(5.32A)		OCP>16.08A
+0.6VS	(0.56A)		
+2.5V	(0.09A)		OCP>0.55A
+1.8VSUS	(0.1169A)		OCP>0.55A
+1.8VS	(0.035A)		
+VCCEOPIO	(1.96A)		OCP>7A
+VCCOPC	(2.03A)		OCP>7A
+VCORE	(U22)	(21A)	OCP>34A
	(U23e)	(23A)	OCP>39A
+VCCGT	(U22)	(18A)	OCP>38A
	(U23e)	(40A)	OCP>74A
+VCCSA	(U22)	(4A)	OCP>7A
	(U23e)	(5A)	OCP>9A

modify notice

Version	Date	Description
	2015/0626	Change all Jumper back (from Rsense) Remove 1.8VSUS snubber

<Variant Name>

PEGATRON
PEGATRON TECHNOLOGY (HK) CO.,LIMITED

Title : POWER_History

Engineer: Remiel_You

Size	Project Name	Rev
Custom	PSHCJ	1.0

Date: Monday, February 24, 2014 Sheet 35 of 36