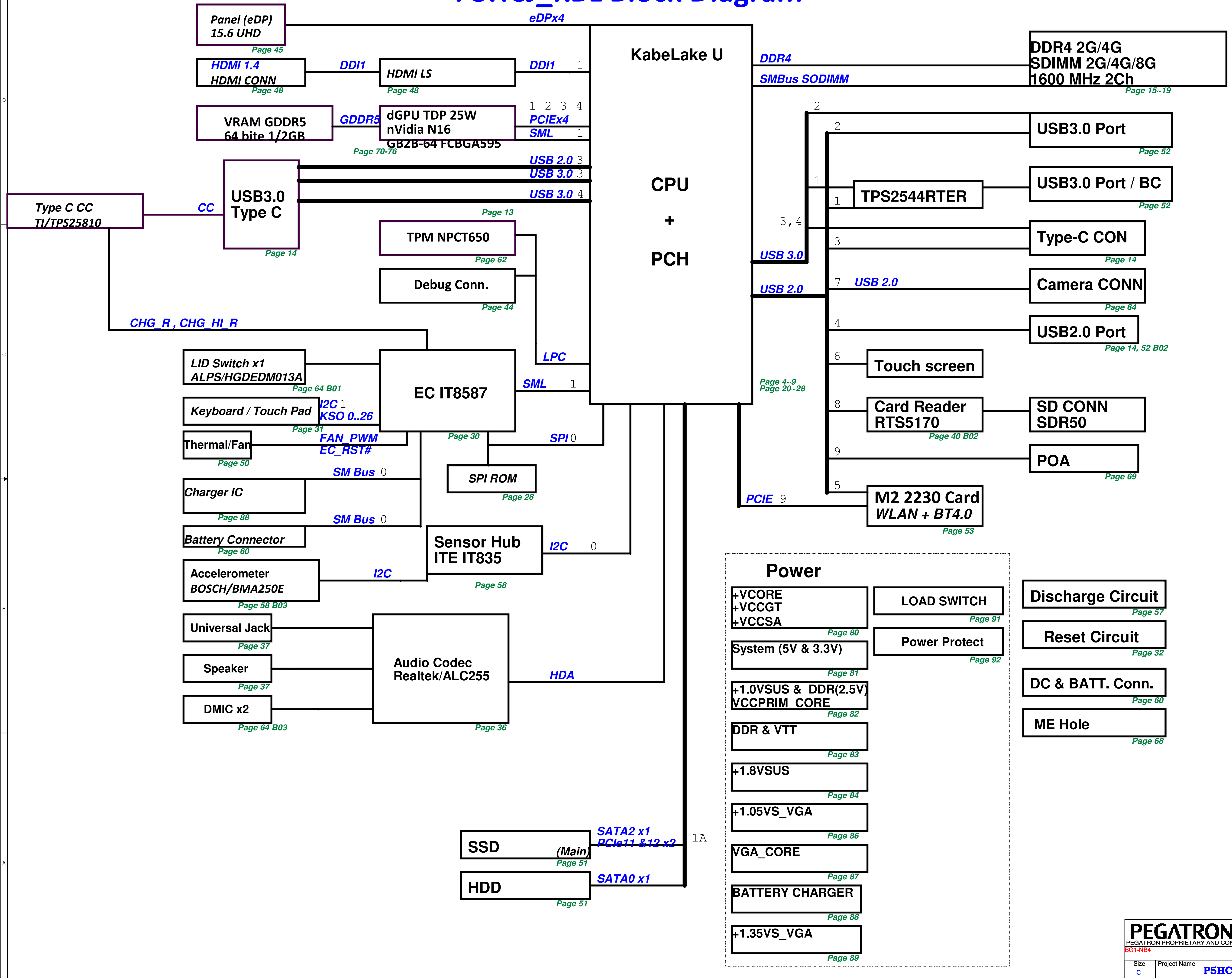
P5HCJ_KBL Block Diagram



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4

Title :	Block Diagram		
Engineer:	Leo_Zhang		
Size C	Project Name P5HCJ_KBL		Rev 1.2
Date: Monday, June 20, 2016	Sheet 1	of	96

Option

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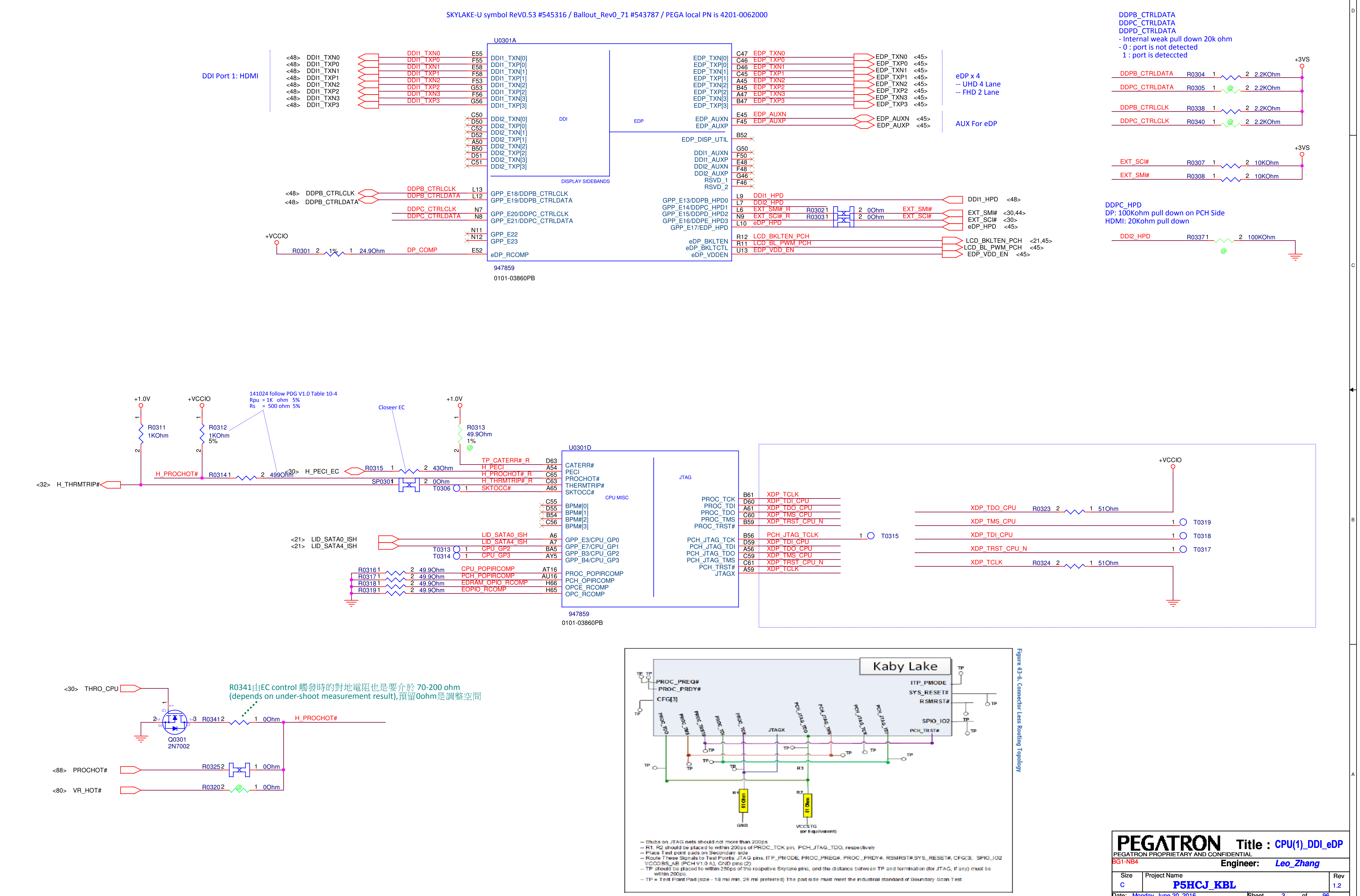
Optional	Stage								
	SR		ER		PR		MP		
	UMA	DIS	UMA	DIS	UMA	DIS	UMA	DIS	Remark
N/A	POP	POP							Mount
/@	NC	NC							Ummount
/Debug	POP	POP							Debug only
/TPM	NC	NC							Support TPM function
/NON-IOAC	POP	POP							Not support IOAC
/IOAC	NC	NC							Support IOAC
/HDD	POP	POP							Support HDD
/UMA	POP	POP							Support UMA
/VGA	NC	POP							Support VGA
/VGA_VRAM	NC	POP							VRAM selection
/GC6	NC	POP							Support GC6 function
/NGC6	NC	NC							Not support GC6 function
/USBSLP	POP	POP							Support USB wake up
/EMI	NC	NC							Reserved EMI part
/SSD	POP	POP							Support SATA SSD
/SSD_PCIe	POP	POP							Support PCIe SSD
/HDD_PROT	POP	POP							Support HDD portect
/POA	POP	POP							Support POA
/RTL									10DN Support Array Mic
/ADSP									08DN Support Stereo Mic

03

CPU(1)_DDI_eDP



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BG1-NB4

Title : CPU(1)_DDI_eDP

Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

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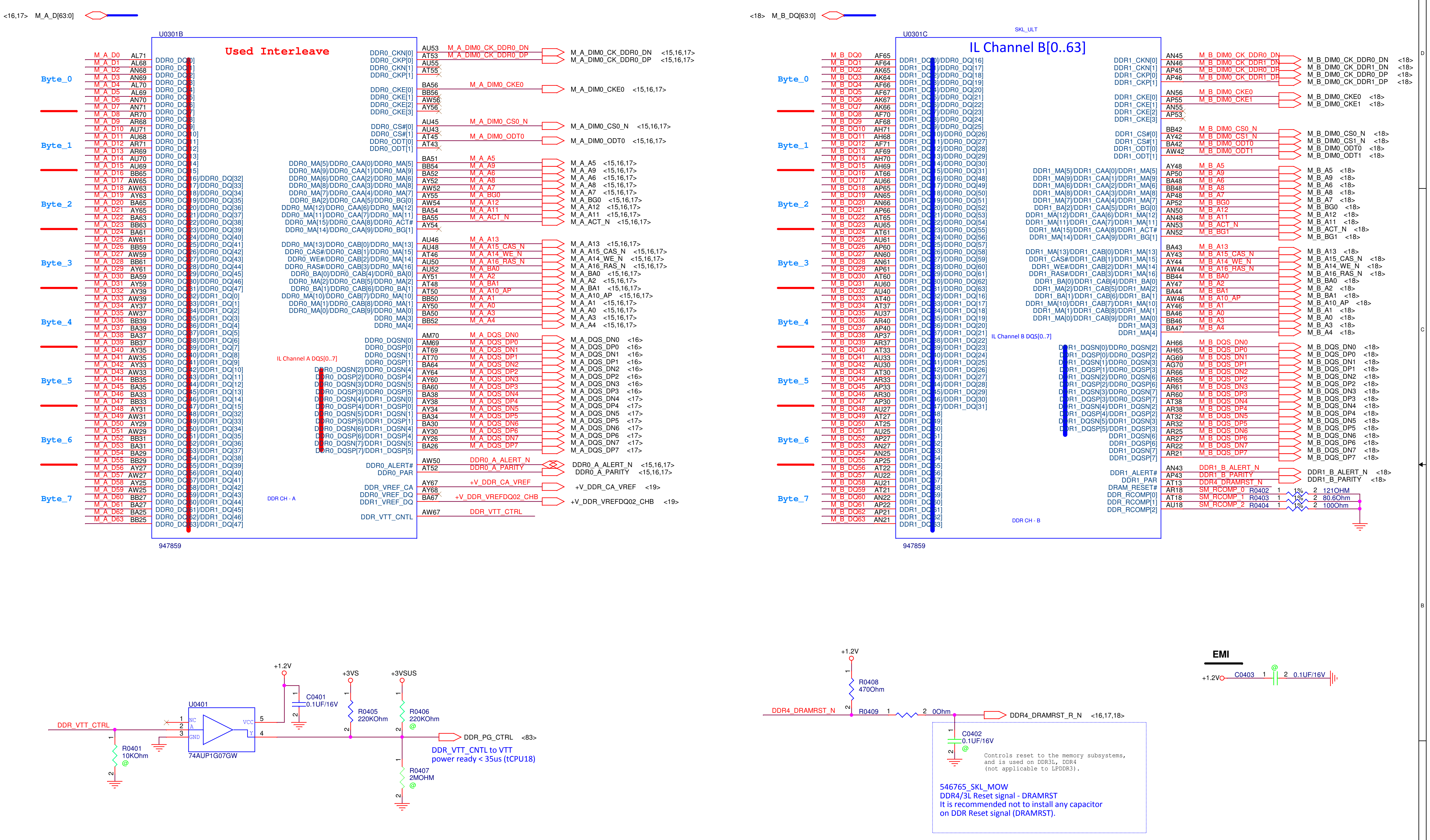
04 Memory bus_DDR4



Symbol U0301 B

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelA DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[0..15] DQS/DQS#[0,1]
BYTE 1		
BYTE 2		ChannelADQ[32..47] DQS/DQS#[4,5]
BYTE 3		
BYTE 4		ChannelB DQ[0..15] DQS/DQS#[0,1]
BYTE 5		
BYTE 6		ChannelB DQ[32..47] DQS/DQS#[4,5]
BYTE 7		

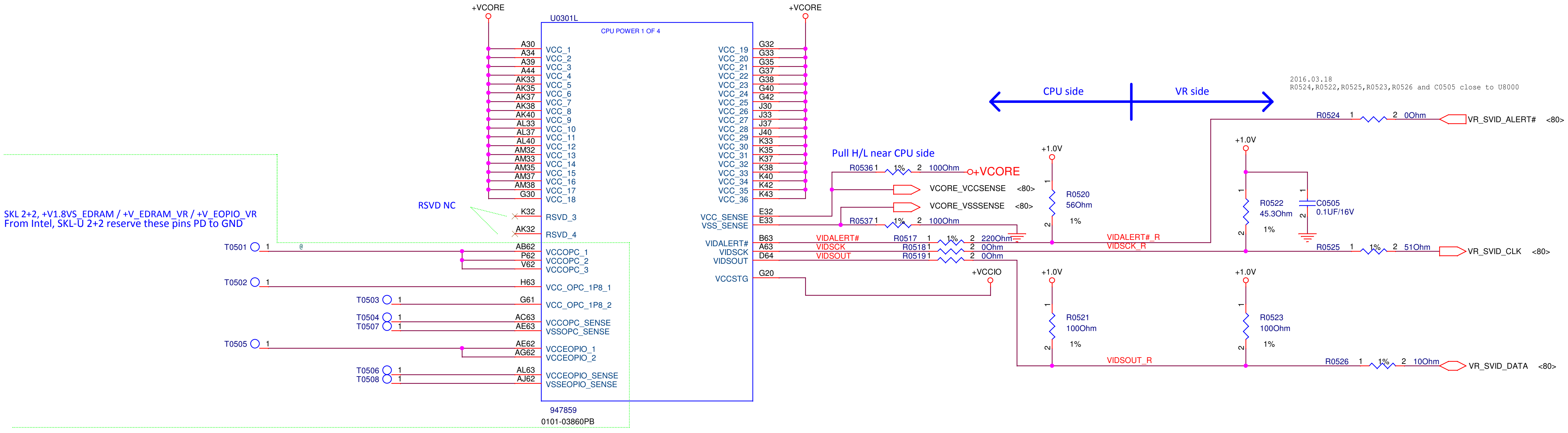
Symbol U0301 C

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelB DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[16..31] DQS/DQS#[2,3]
BYTE 1		
BYTE 2		ChannelADQ[48..63] DQS/DQS#[6,7]
BYTE 3		
BYTE 4		ChannelB DQ[16..31] DQS/DQS#[2,3]
BYTE 5		
BYTE 6		ChannelB DQ[48..63] DQS/DQS#[6,7]
BYTE 7		

PEGATRON Title : Memory bus_DDR4
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4
Engineer: Leo_Zhang
Size C | Project Name P5HCJ_KBL | Rev 1.2
Date: Monday, June 20, 2016 Sheet 4 of 96

05

CPU(3)_+VCCCORE



PEGATRON
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BG1-NB4

Title	CPU(3)_+VCCCORE
Engineer:	Leo_Zhang
Size	C
Project Name	P5HCJ_KBL
Rev	1.2
Date:	Monday, June 20, 2016
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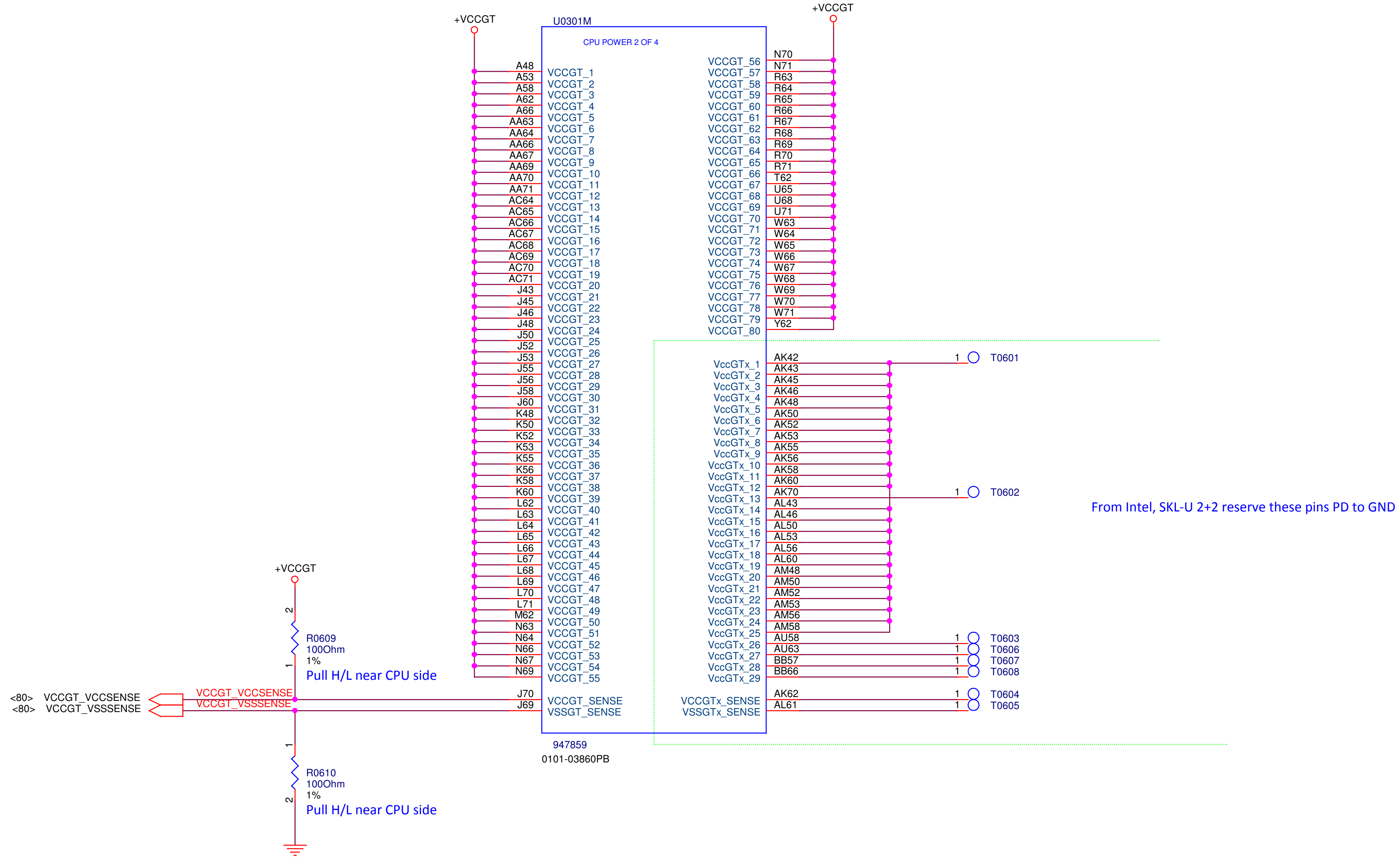
06

CPU(4)_+VCCGT



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4
Title : CPU(4)_+VCCGT
Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

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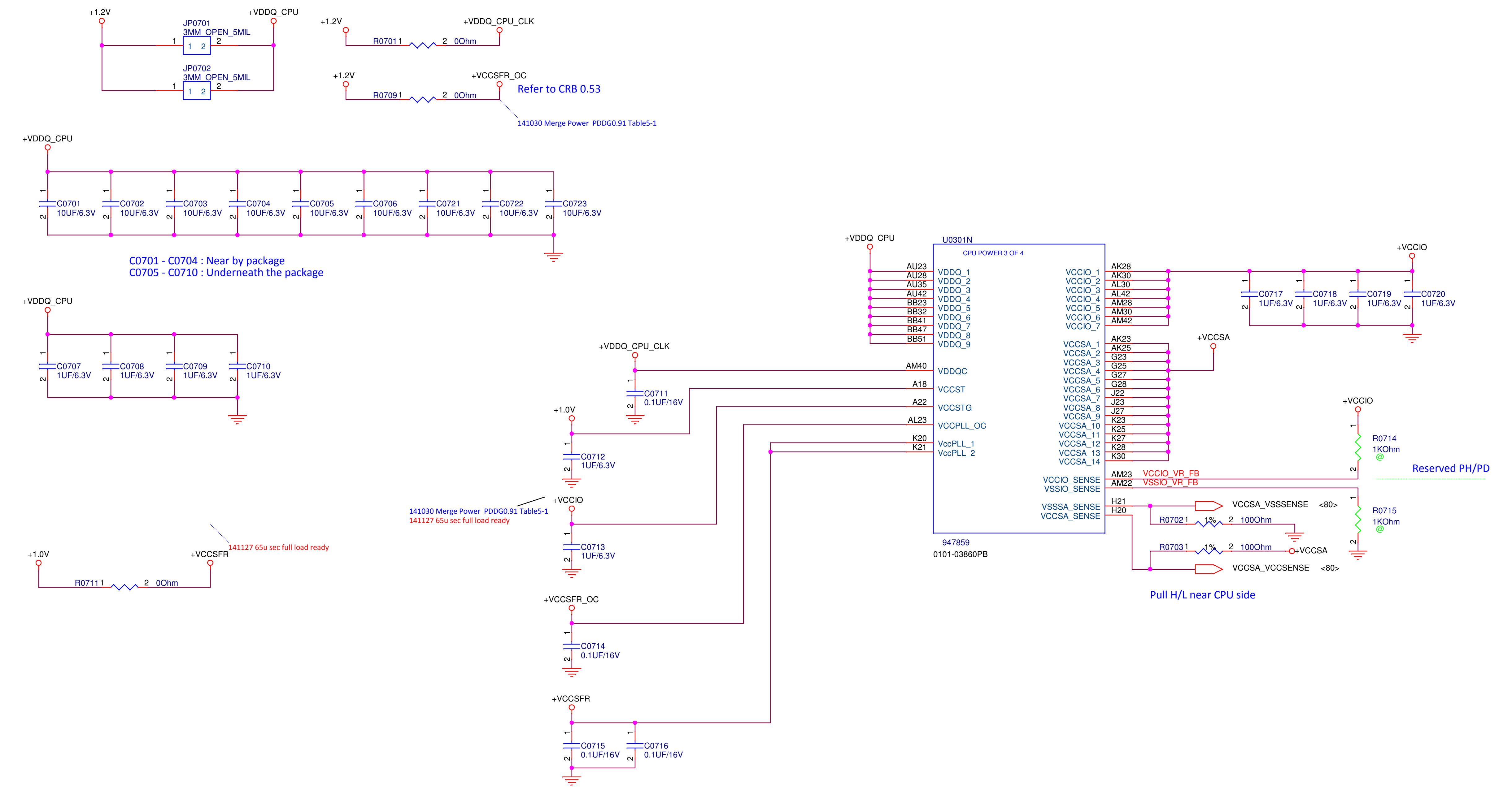
07

CPU(5)_+VDDQ/IO/SA



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4

Title: CPU(5)_+VDDQ/IO/SA

Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

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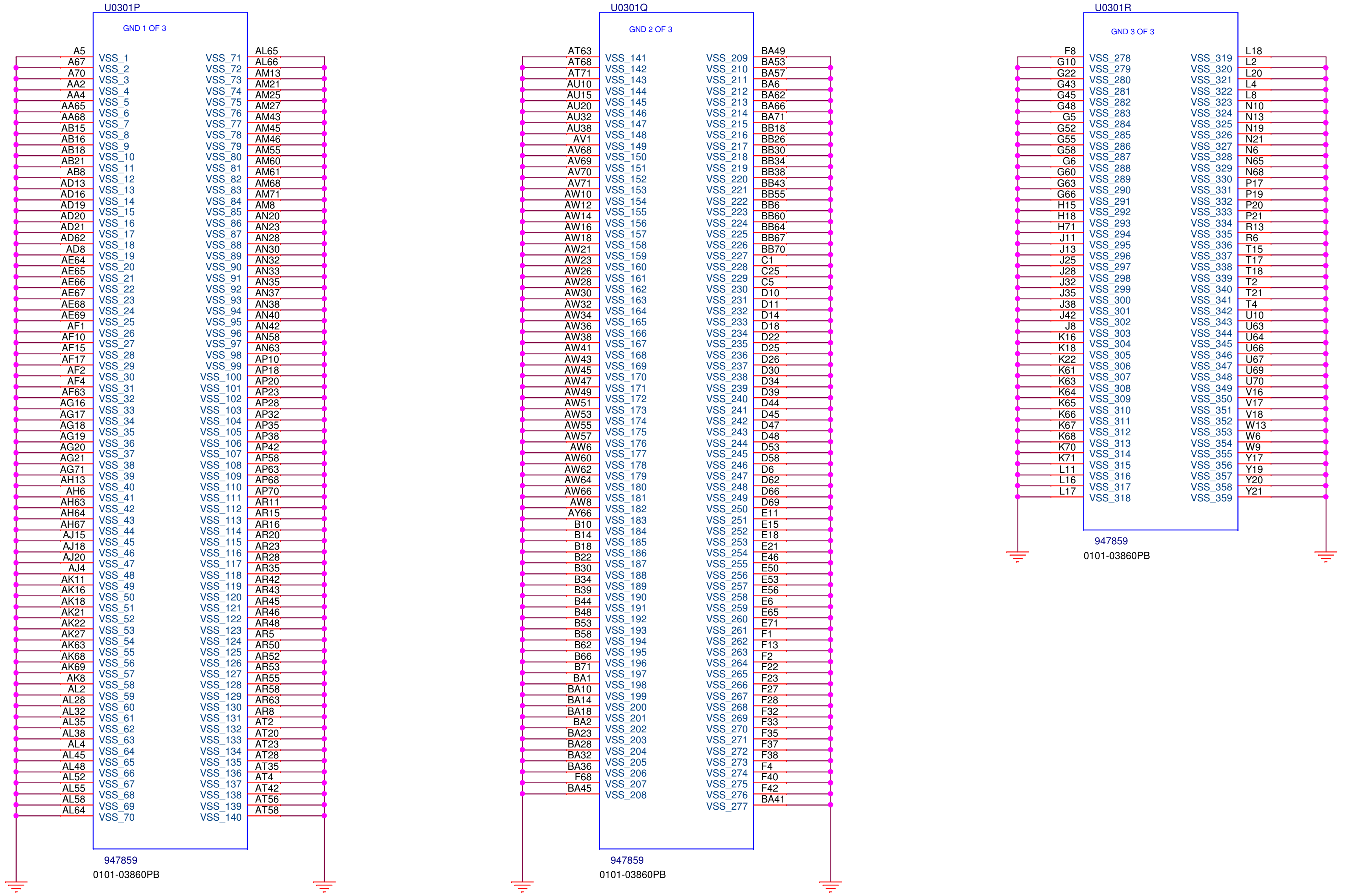
08

CPU(6)_CPU GND



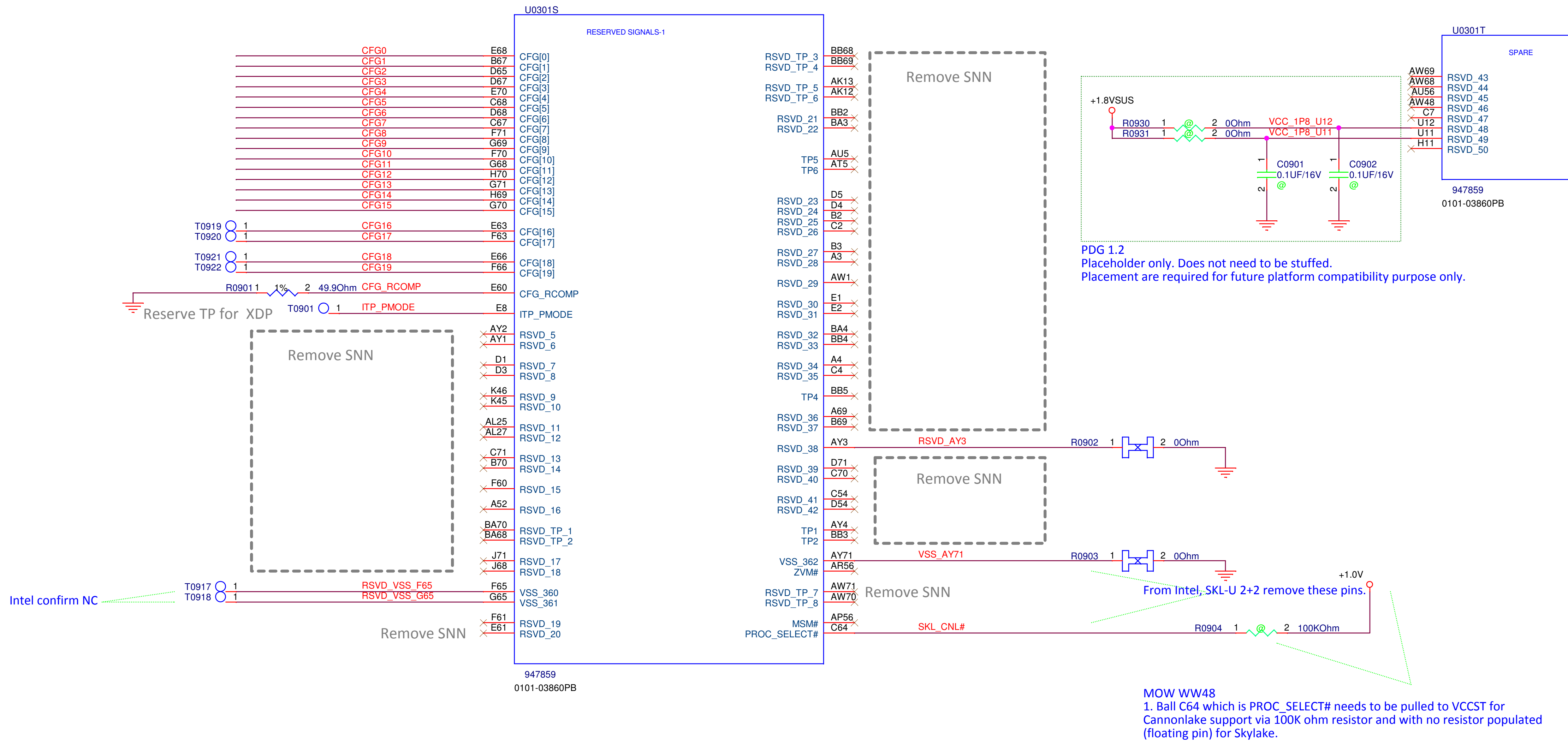
PEGATRON Title : CPU(6)_CPU GND

BG1-NB4 Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 8 of 96

CPU(7)_CFG/RSVD



The CFG signals have a default value of '1' if not terminated on the board.

*All processor lines.
CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them

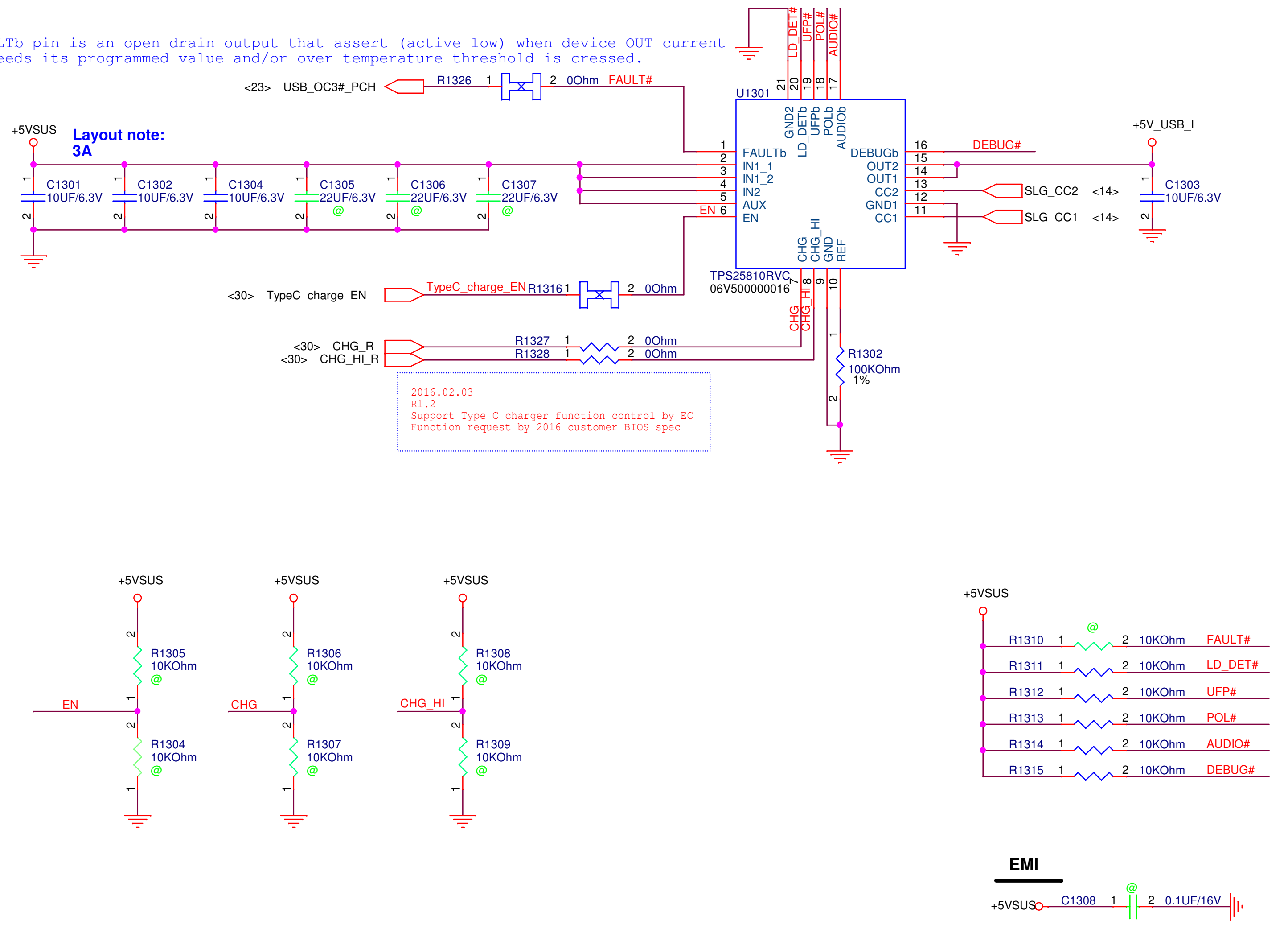
Name	P5HCJ_KBL	Description
CFG0	1	1 = (Default) Normal Operation; No stall 0 = Stall
CFG1	1	Reserved configuration lane
CFG2	1	PCI Express* Static x16 Lane Numbering Reversal 1 = Normal operation 0 = Lane numbers reversed
CFG3	1	Reserved configuration lane
CFG4	0	CFG[4]: eDP* enable: 1 = Disabled. 0 = Enabled
CFG5 CFG6	1	CFG[6:5]: PCI Express* Bifurcation 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
CFG7	1	CFG[7]: PEG Training: 1 = (default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.
CFG[19:8]	1	Reserved configuration lane

From EDS_Intel_CPU(Kabylake.UY)_Vol1_559100_Rev0p91 Page.123

13

Type_C_TPS25810

FAULTb pin is an open drain output that assert (active low) when device OUT current exceeds its programmed value and/or over temperature threshold is cressed.



PEGATRON
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BG1-NB4

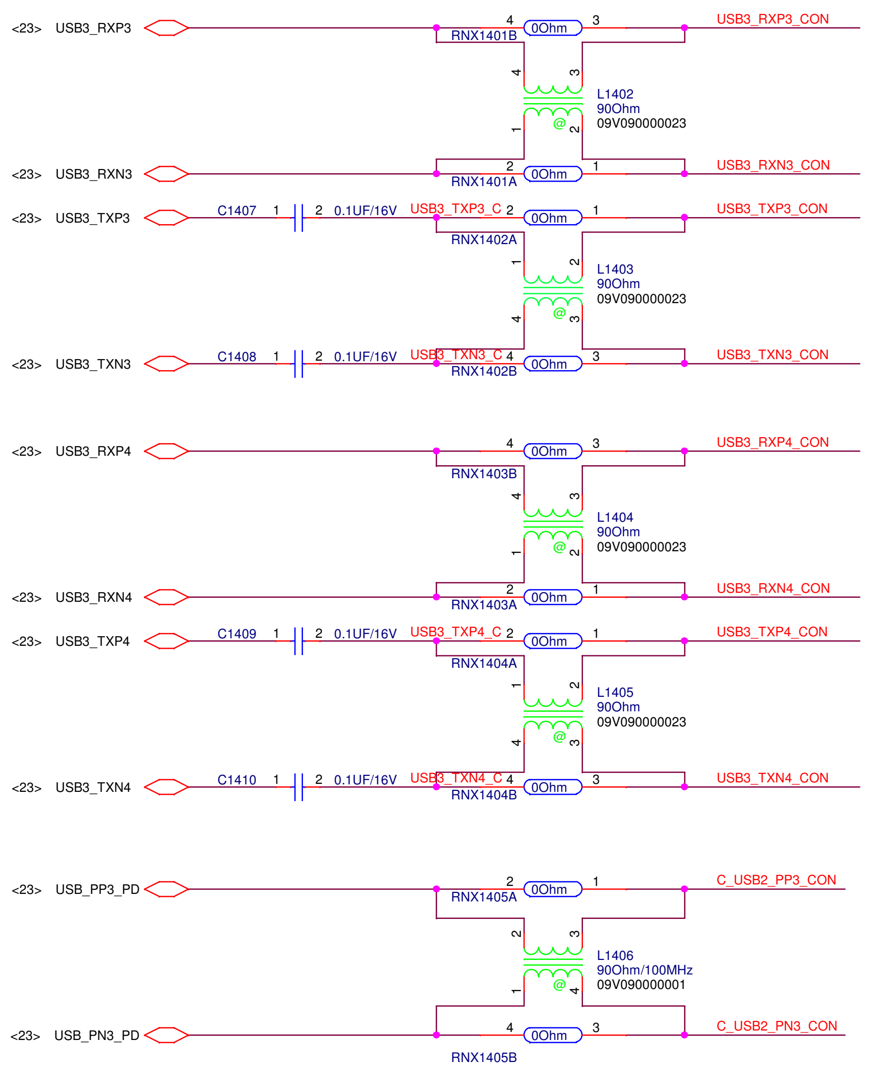
Title : Type_C_TPS25810

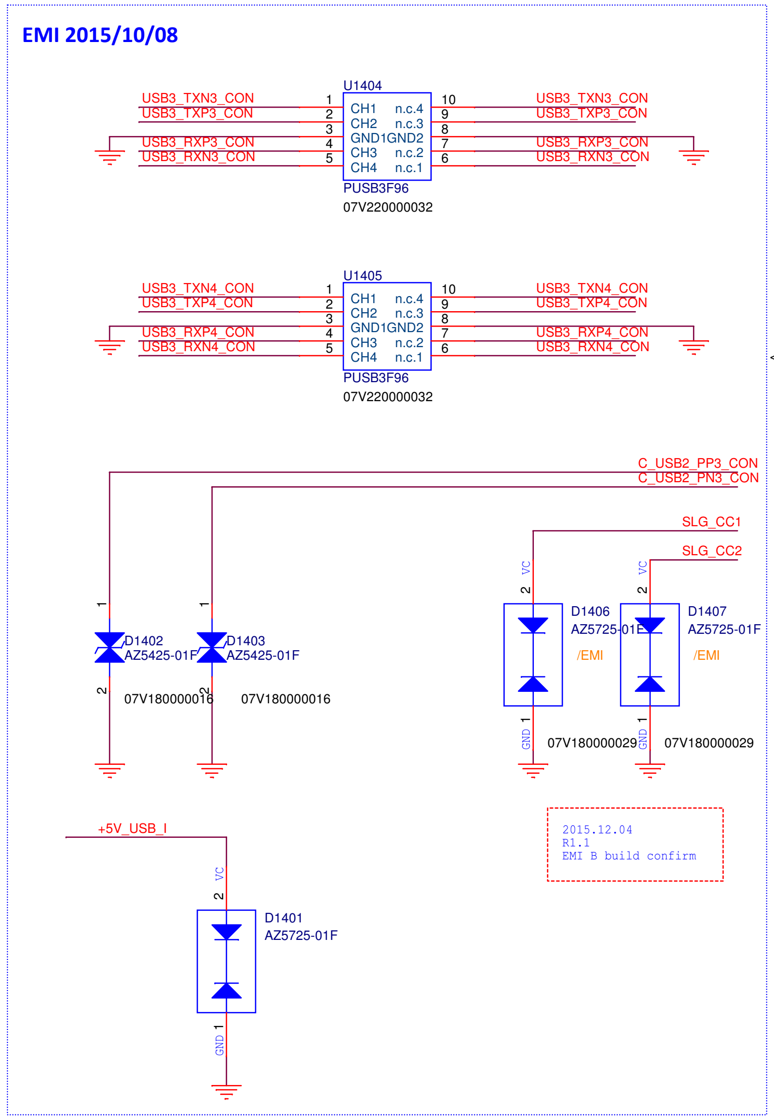
Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 13 of 96

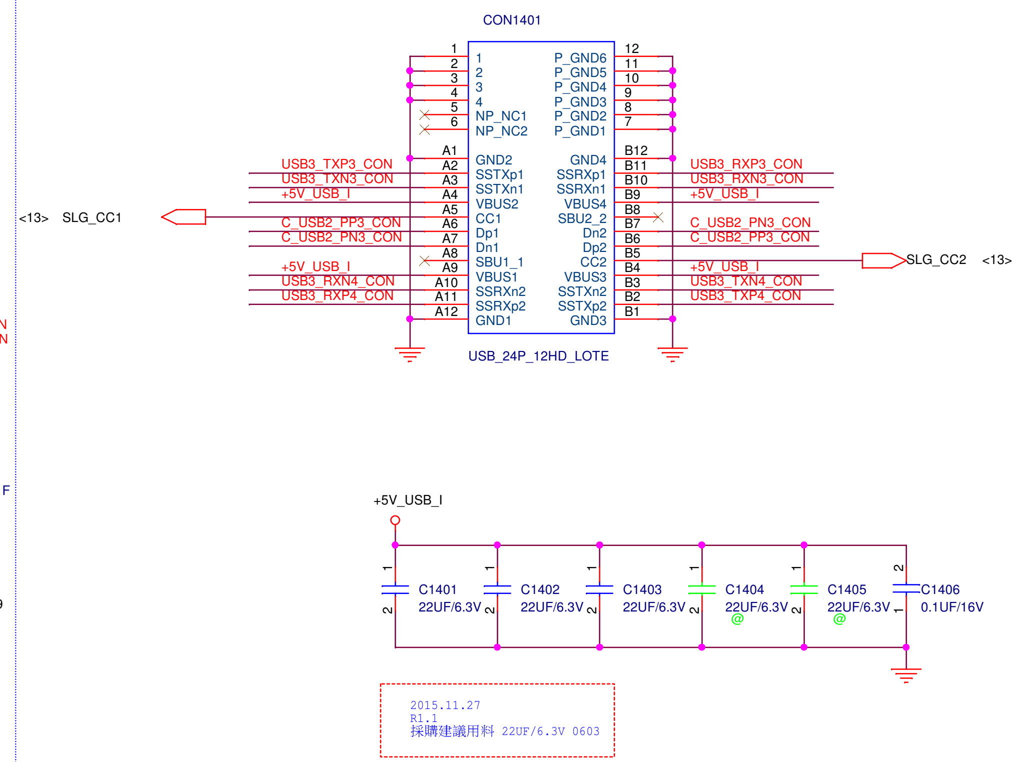
Type C CONN





USB Type C Connector

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1



Title : Type C CONN

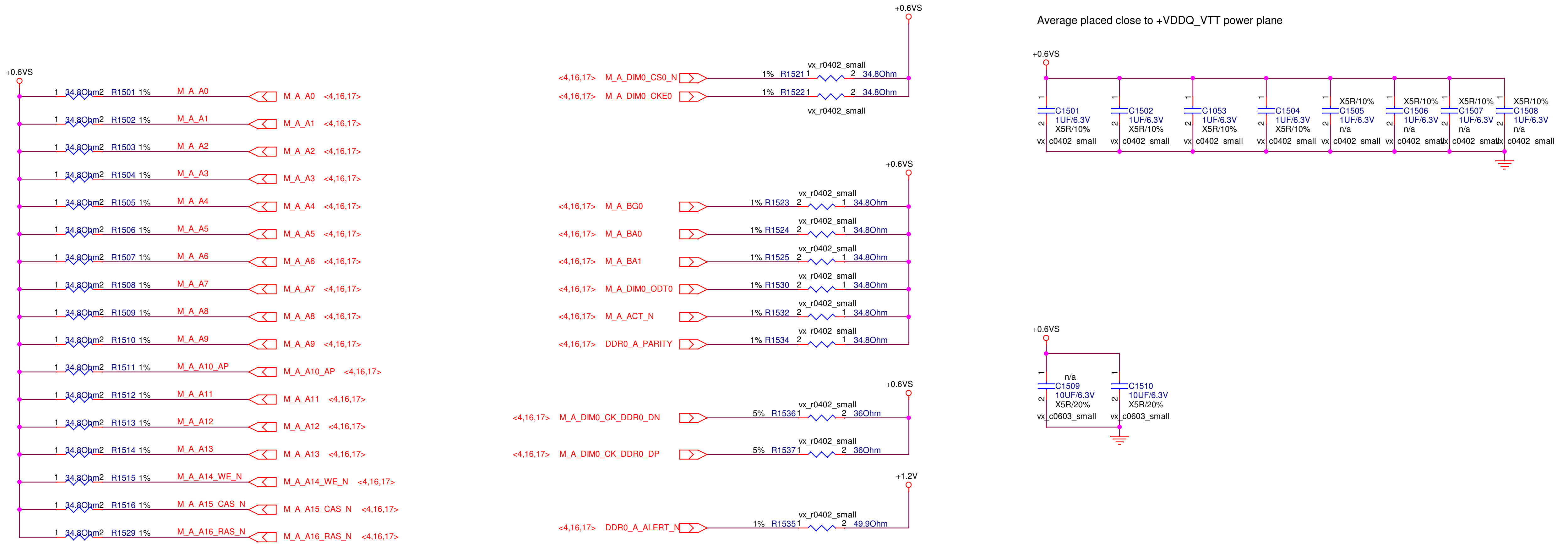
BG1-NB4

Engineer: Leo_Zhang

Size: C | Project Name: P5HCJ_KBL | Rev: 1.2

Date: Monday, June 20, 2016 | Sheet 14 of 96

DDR4(0)_Termination



PEGATRON Title : DDR4(0)_Termination

PEGATRON PROPRIETARY AND CONFIDENTIAL

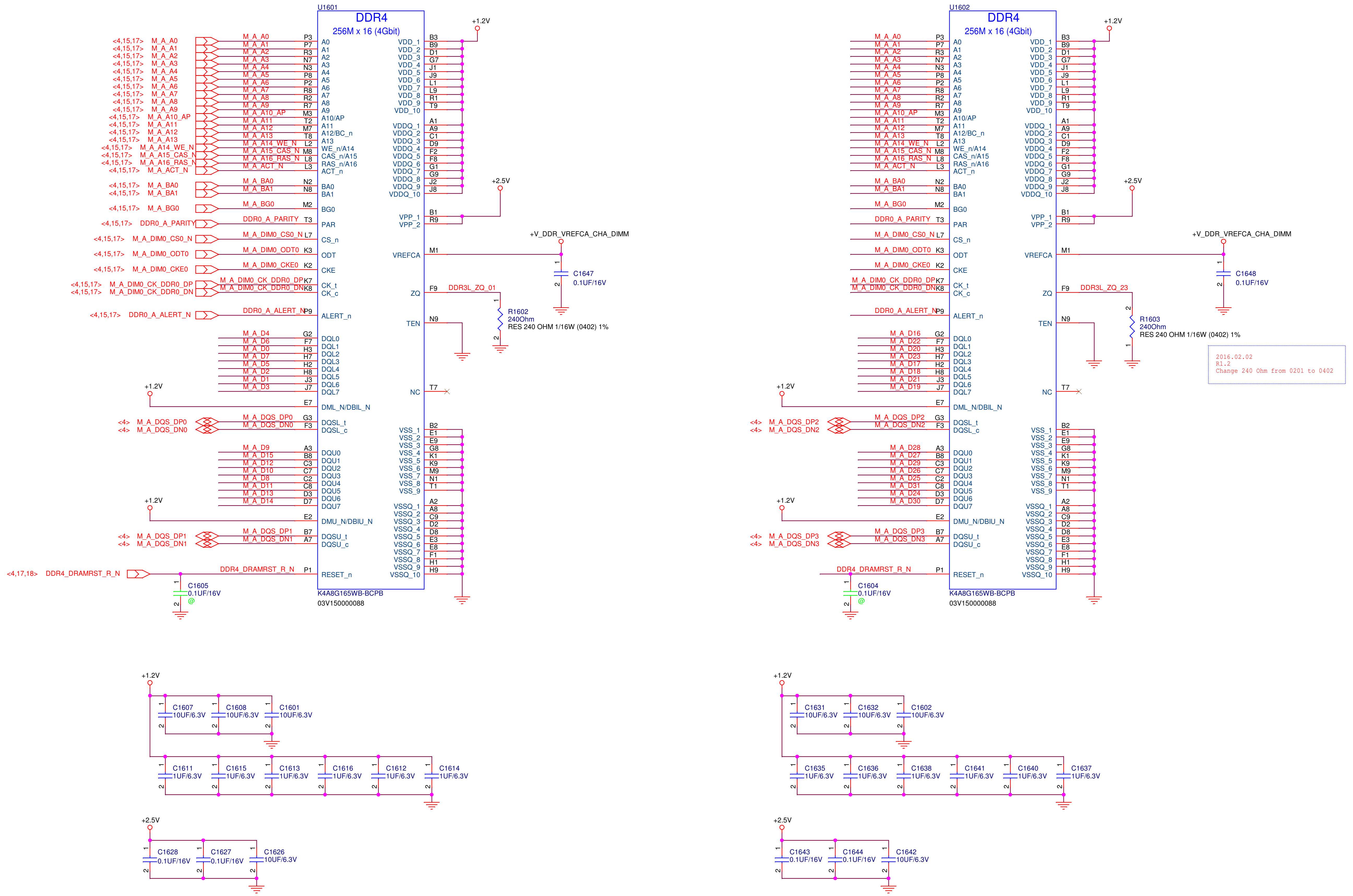
BG1-NB4 Engineer:

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 15 of 96

M_A_D[0:31] <4>

DDR4(1)_CH0



PEGATRON

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Title : DDR4(1)_CH0

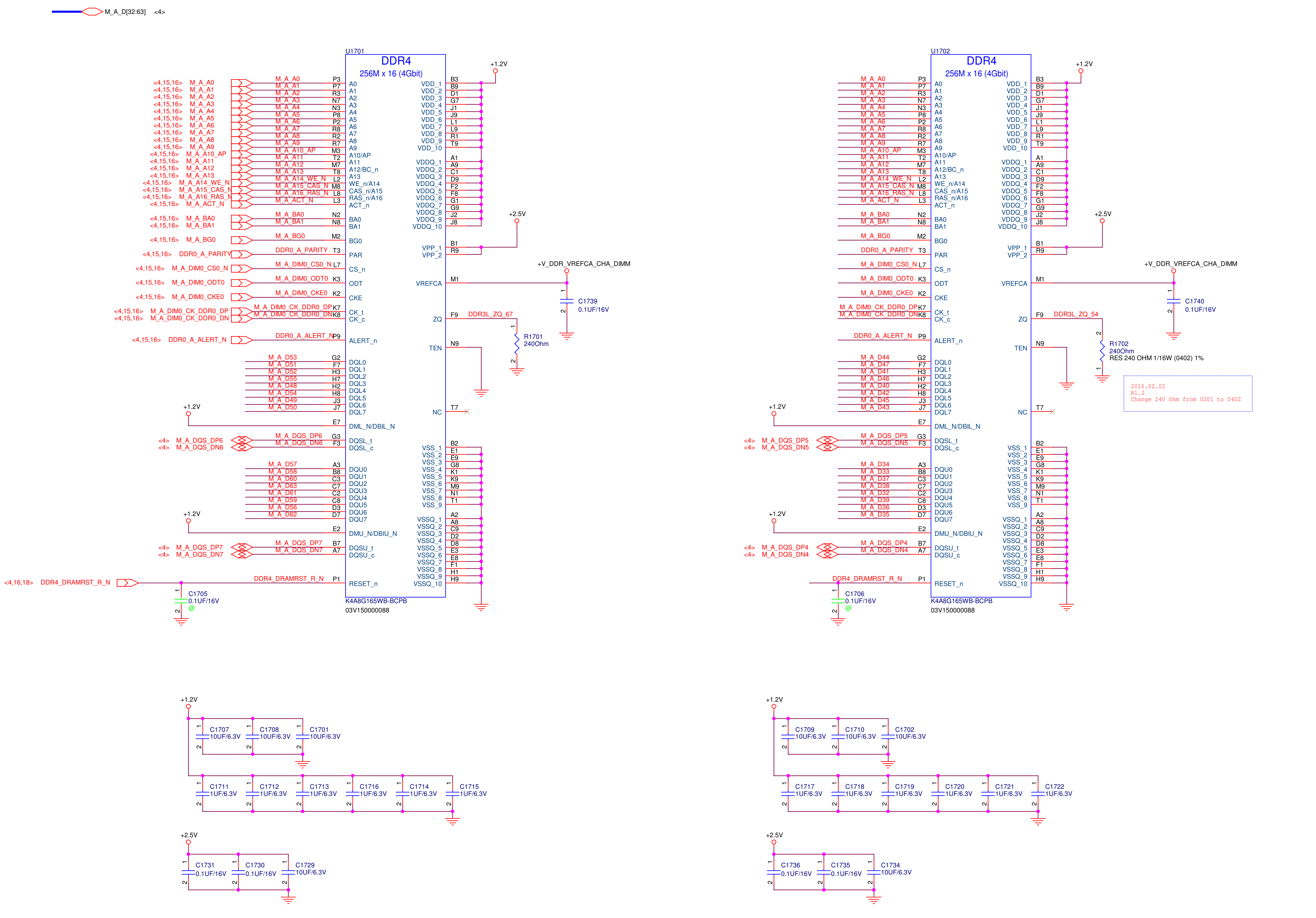
BG1-NB4

Engineer:

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 16 of 96

DDR4(2)_CH0



PEGATRON Title : DDR4(2)_CH0

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BG1-NB4

Engineer:

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

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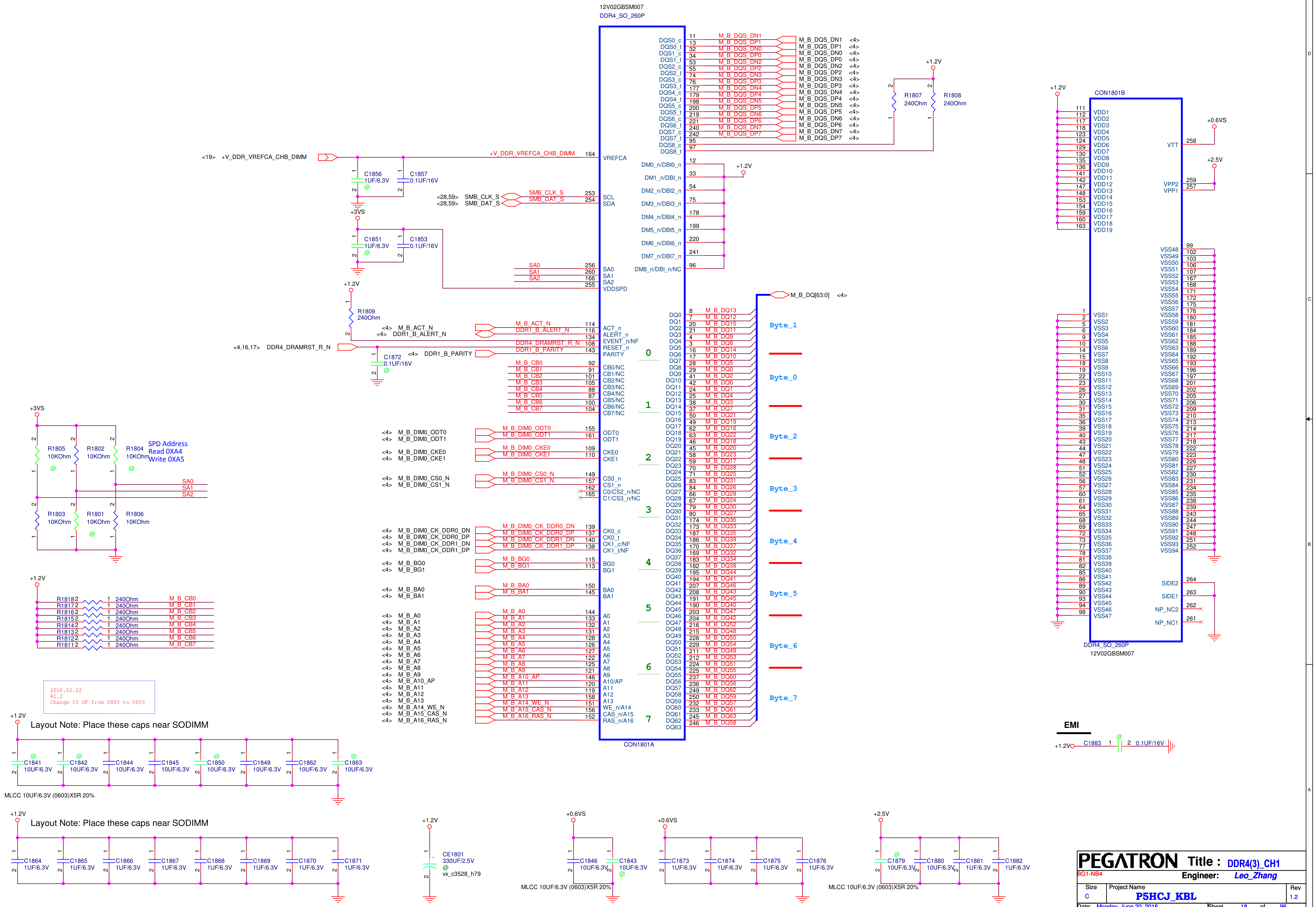
DDR4(2)_SODIMM



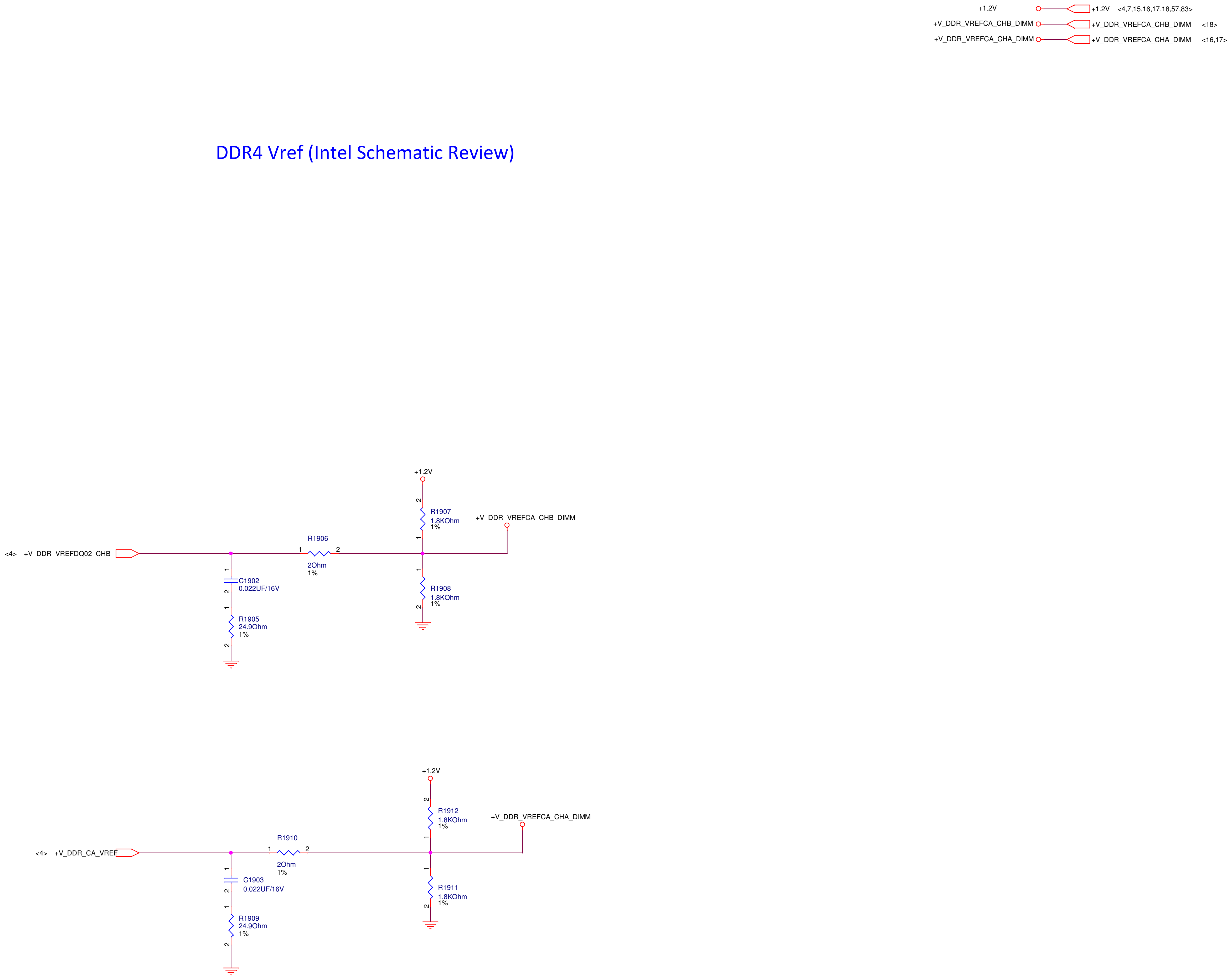
PEGATRON Title : DDR4(3)_CH1
BG1-NB4
Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 18 of 96

DDR4(3)_CA/DQ Voltage

DDR4 Vref (Intel Schematic Review)



PEGATRON	Title : DDR4(3)_CA/DQ Voltage	
BG1-NB4	Engineer: Leo_Zhang	
Size: C	Project Name: P5HCJ_KBL	Rev: 1.2
Date: Monday, June 20, 2016	Sheet 19 of 96	

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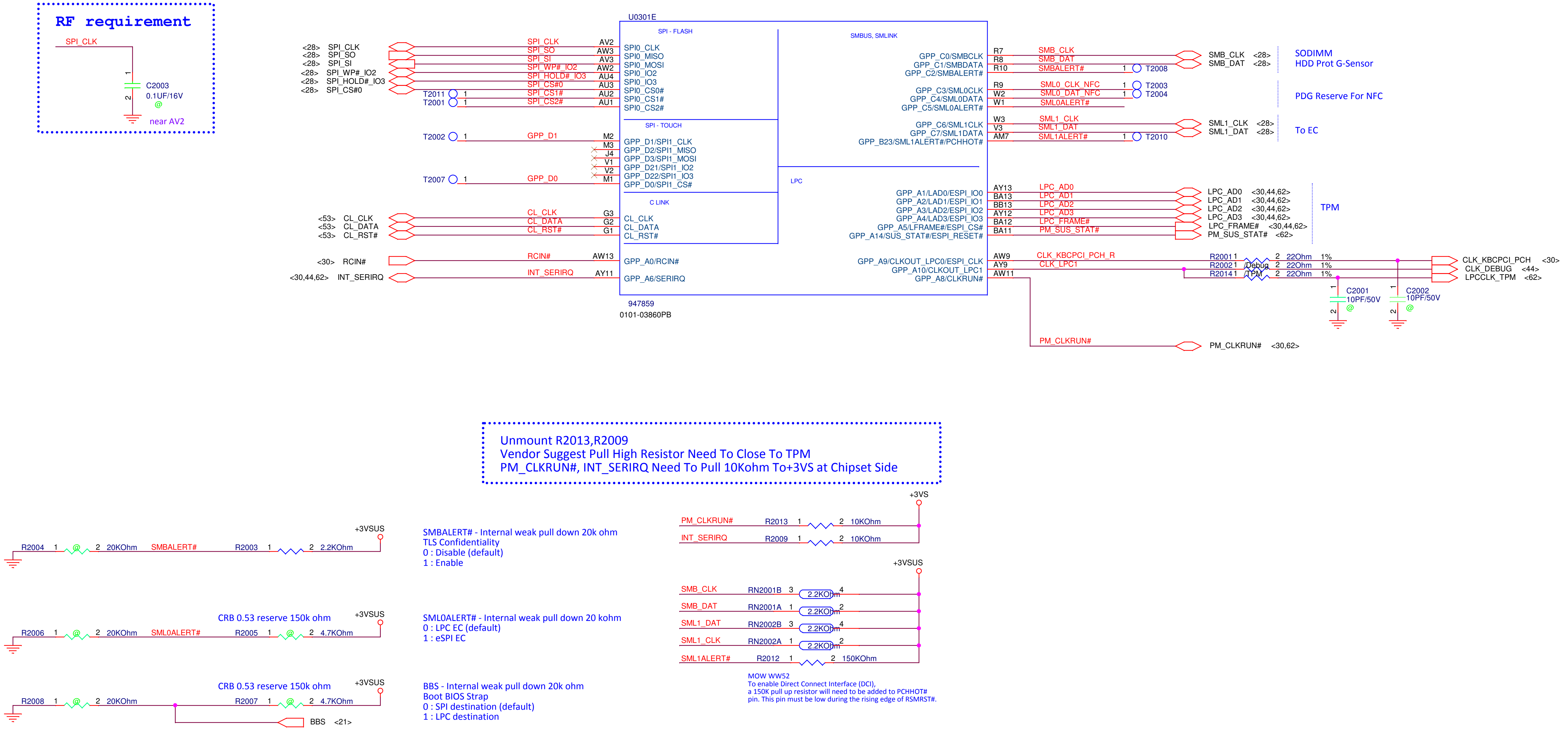
PCH(1)_SPI/LPC



Unmount R2013,R2009
Vendor Suggest Pull High Resistor Need To Close To TPM
PM_CLKRUN#, INT_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

SMBALERT# - Internal weak pull down 20k ohm
TLS Confidentiality
0 : Disable (default)
1 : Enable

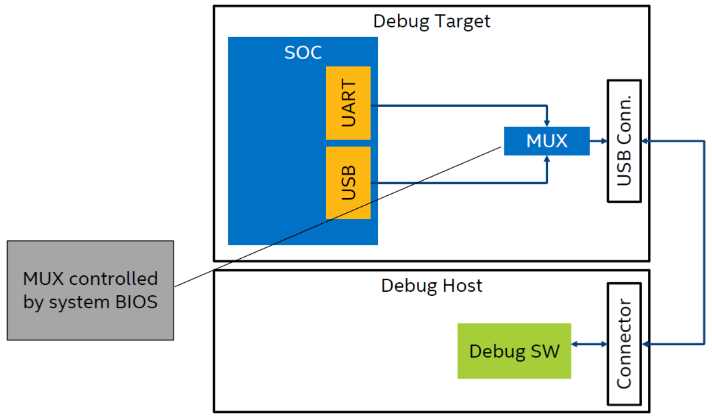
SML0ALERT# - Internal weak pull down 20 kohm
0 : LPC EC (default)
1 : eSPI EC

BBS - Internal weak pull down 20k ohm
Boot BIOS Strap
0 : SPI destination (default)
1 : LPC destination

PCH(2)_ISH

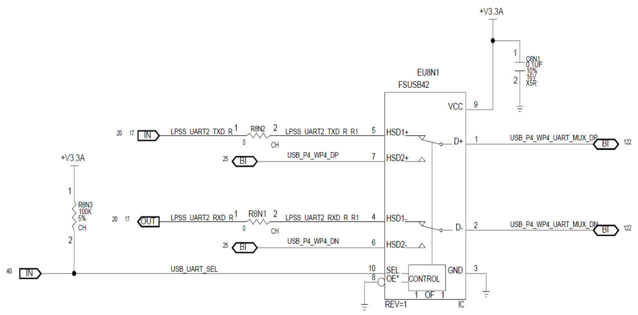
Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

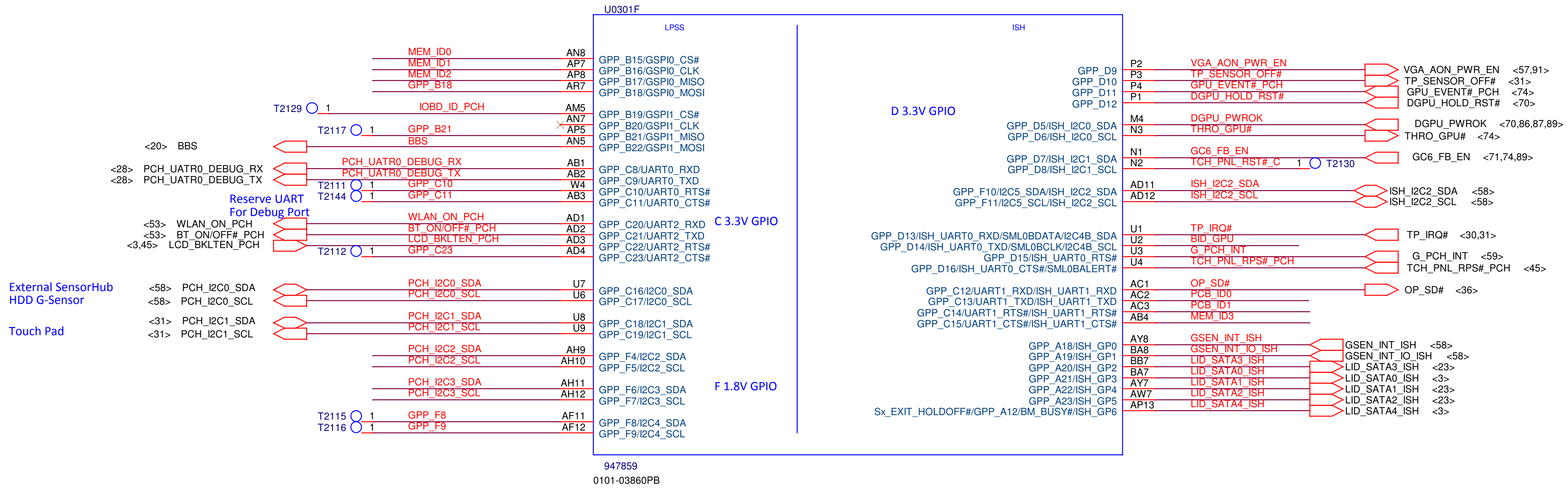
With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required



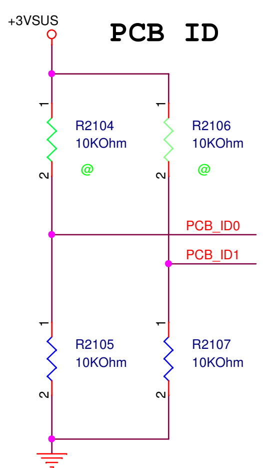
To implement UART for WIN7 WHCK requirement if need

Please refer to Intel document #548689 - RVP5

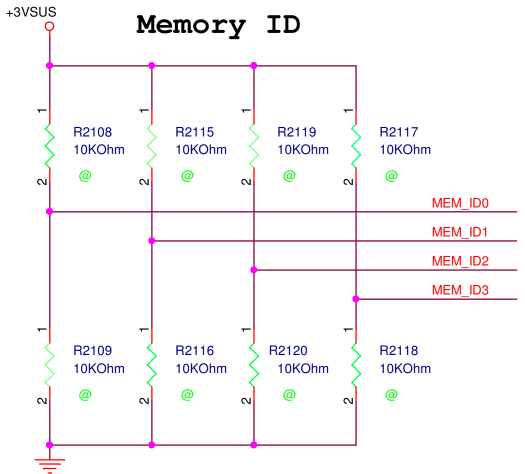




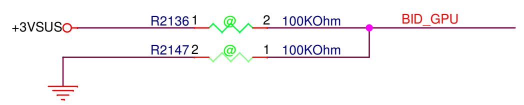
PCB ID



Memory ID



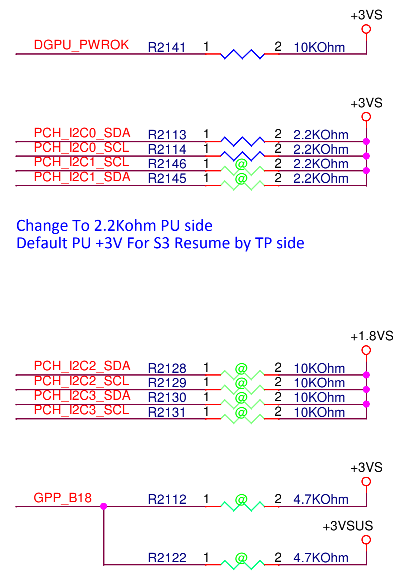
MB BD ID



	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R10	0	0
R11	0	1
R12	1	0

	MEM_ID3 (GPP_C15)	MEM_ID2 (GPP_B17)	MEM_ID1 (GPP_B16)	MEM_ID0 (GPP_B15)
SAMSUNG K4A8G165WB-BCPB 2133MT 8Gb	0	0	0	0
SAMSUNG K4A8G165WB-BCRC 2400MT 8Gb	0	0	0	1
MICRON MT40A512M16JY-083E:B 2400MT 8Gb	0	0	1	0
HYNIX H5AN8G6NAFR-UHC 2400MT 8Gb	0	0	1	1
	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1

	MBBD_ID_PCH	location
UMA	0	R2147
DIS	1	R2136



Change To 2.2Kohm PU side
Default PU +3V For S3 Resume by TP side

GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

Default is GPO, to reserve pull high to +3VSUS_ORG

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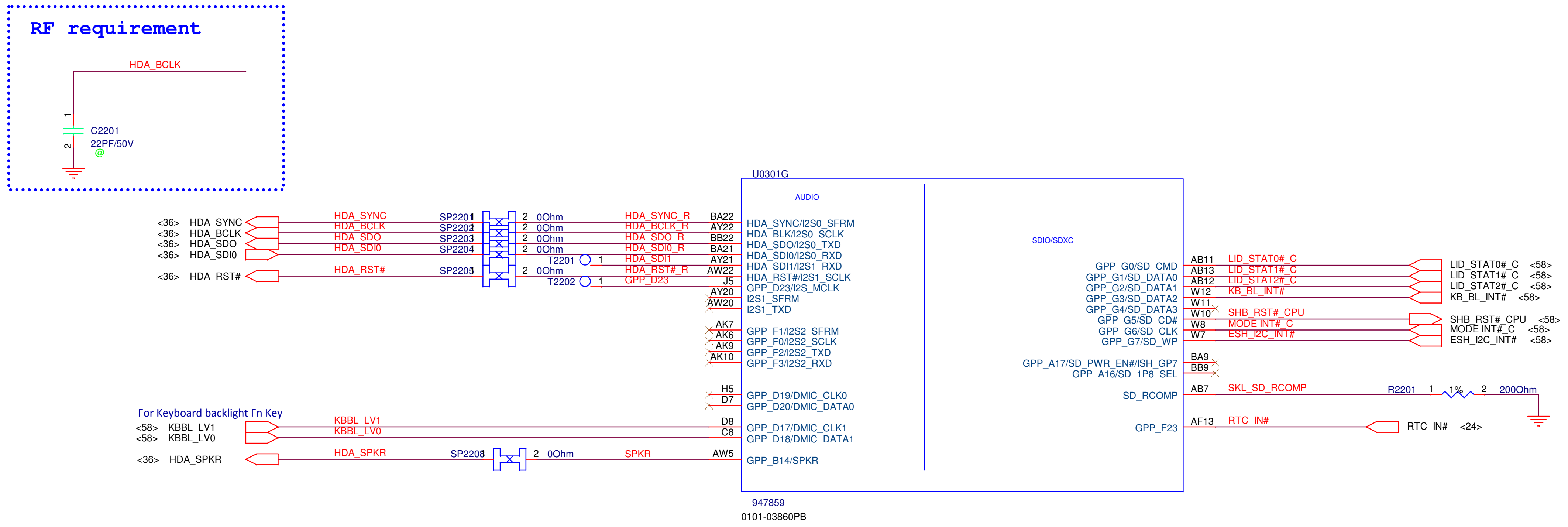
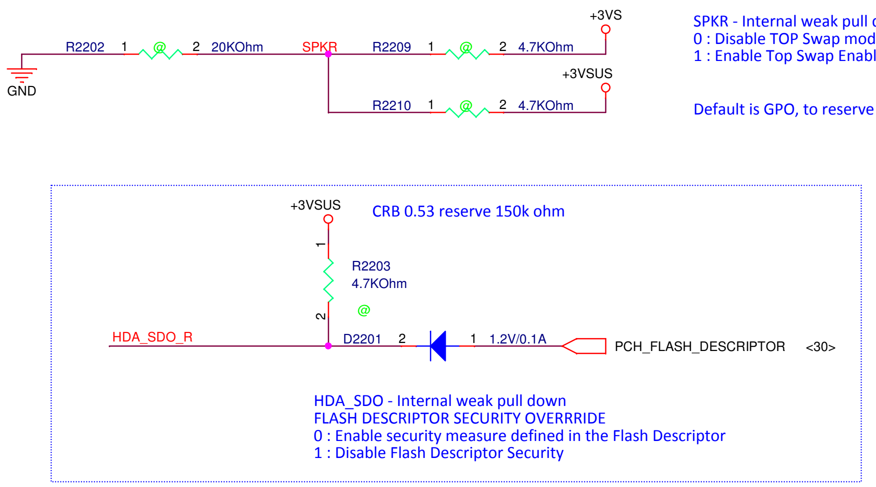
PCH(3)_HDA_SDIO





SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS_ORG

* The signal has a weak internal Pull-down.

Name	P5HCJ_KBL	Description
GPP_B14	0	0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode.
GPP_B18	0	0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode
GPP_B22	0	0 = SPI (Default) 1 = LPC
GPP_C5	0	0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC.
HDA_SDO	0	0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override).
GPP_C2	0	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
GPP_E19	0	0 = Port B is not detected. (Default) 1 = Port B is detected.
GPP_E21	0	0 = Port C is not detected. (Default) 1 = Port C is detected.

From EDS_Intel_PCH(Skylake.UY_Kabylake.UY)_Vol1_545659_Rev2p0 Page.55-57

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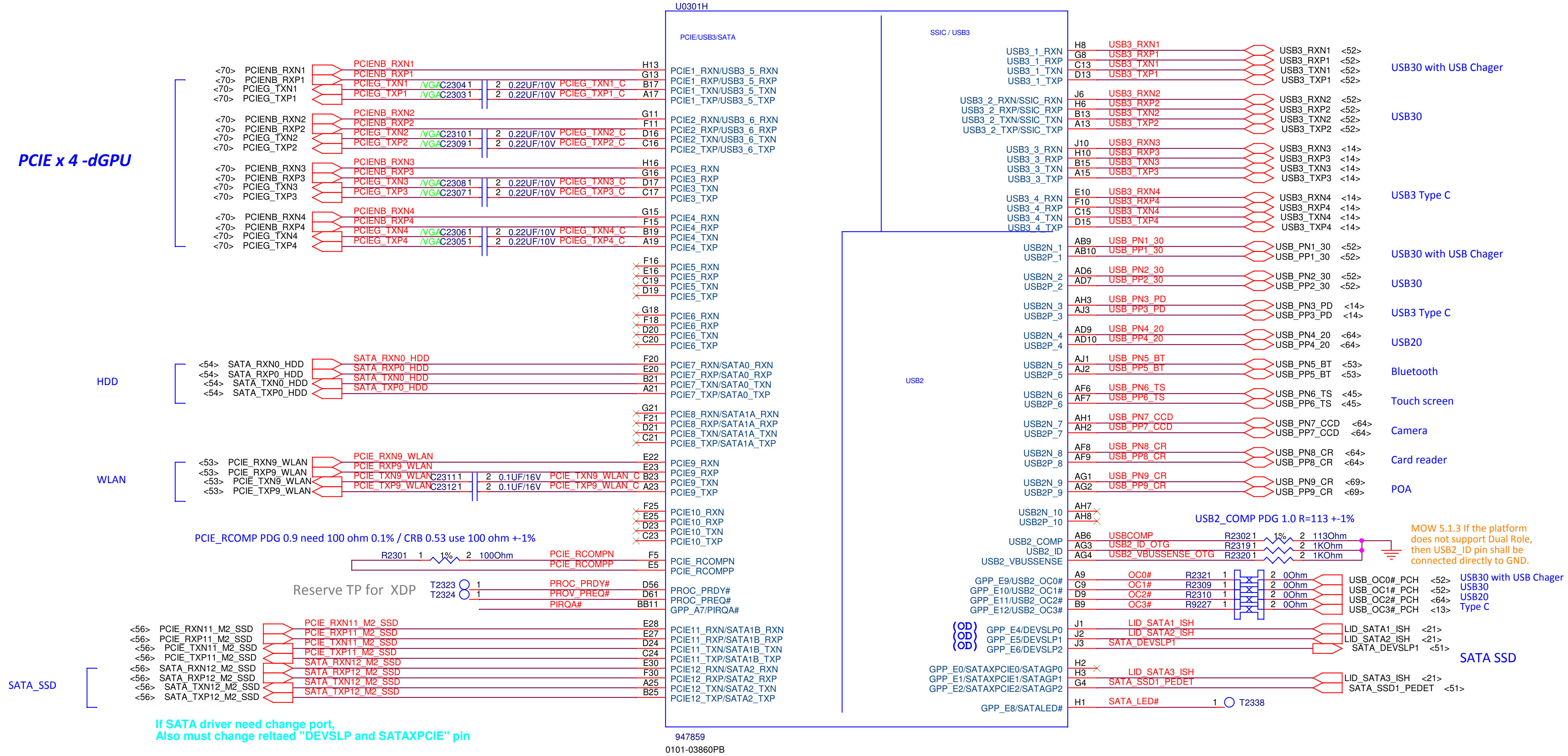
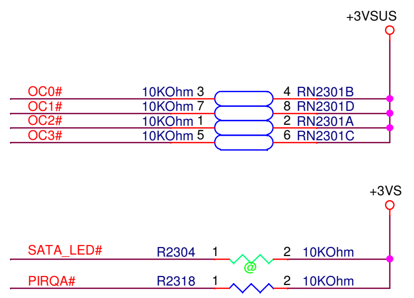
PCH(4)_USB/PCIE/SATA





Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

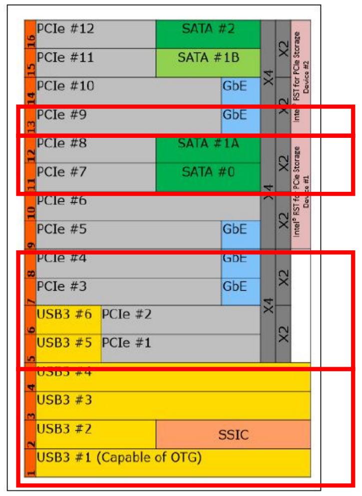


Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

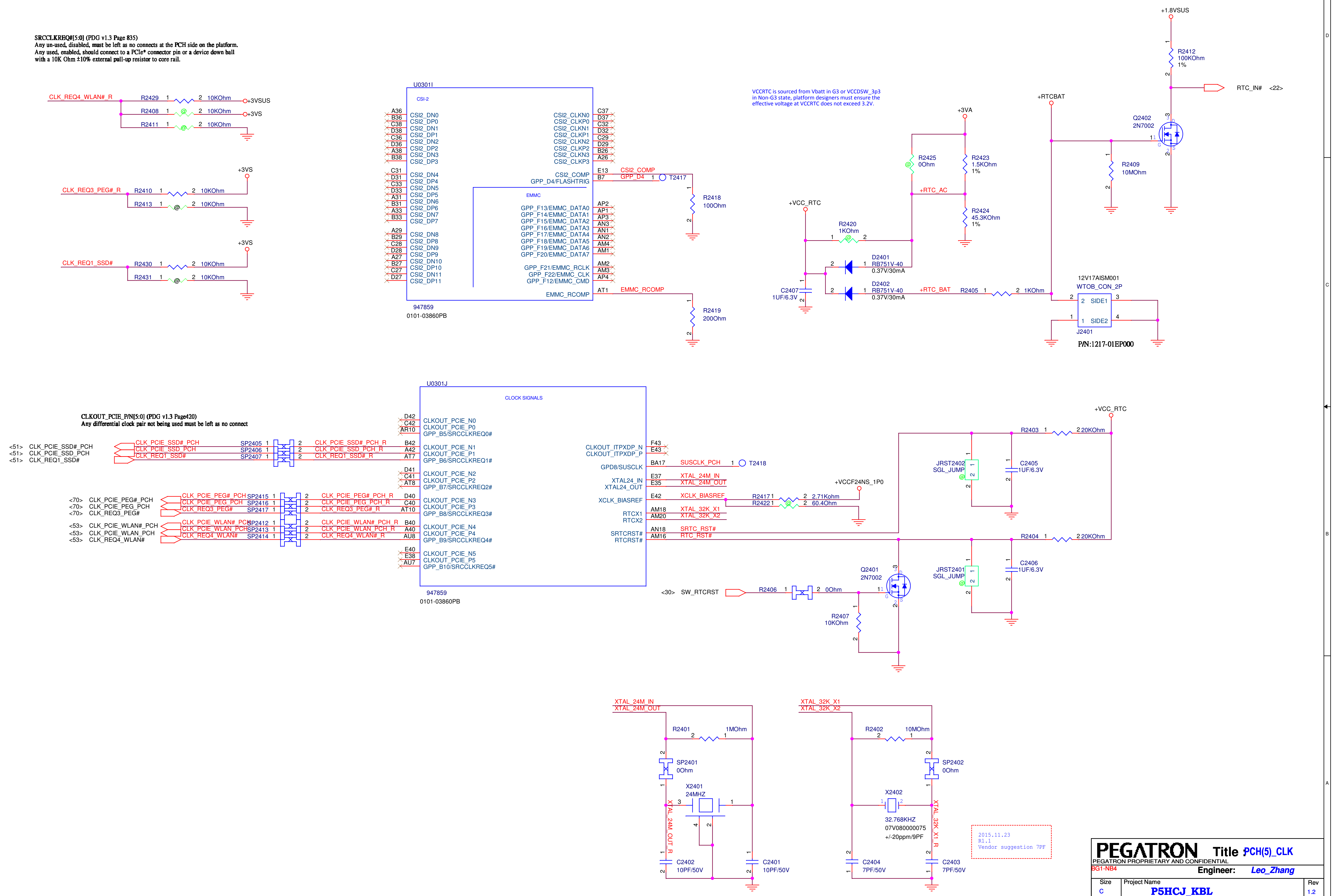
Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe / LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe / LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe / LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

24

PCH(5)_CLK



PEGATRON Title PCH(5)_CLK
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4 Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 24 of 96

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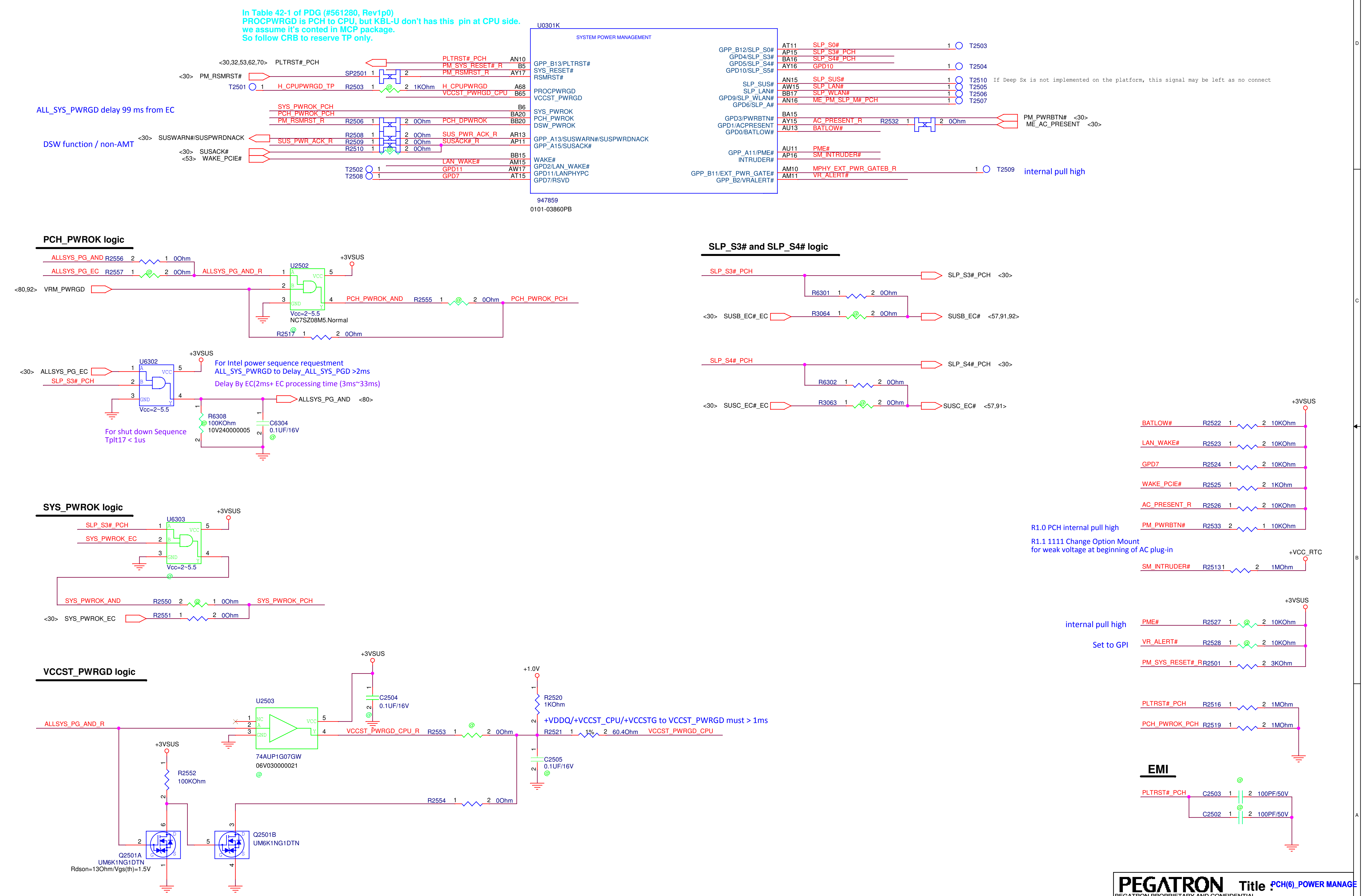
PCH(6)_POWER MANAGE



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4

Title : PCH(6)_POWER MANAGE		
Engineer: Leo_Zhang		
Size: C	Project Name: P5HCJ_KBL	Rev: 1.2
Date: Monday, June 20, 2016	Sheet 25 of 96	

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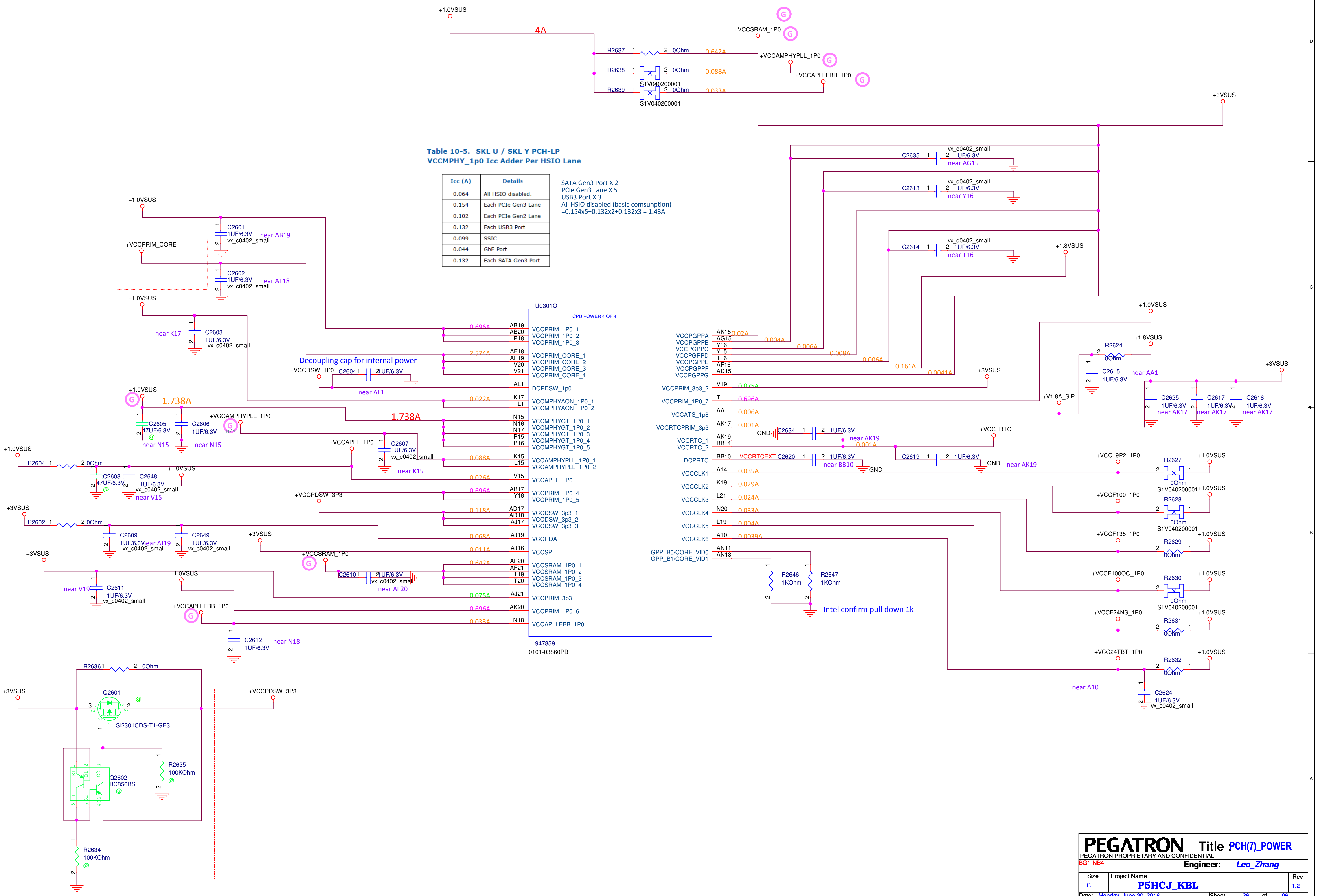
PCH(7)_POWER

Table 10-5. SKL U / SKL Y PCH-LP
VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

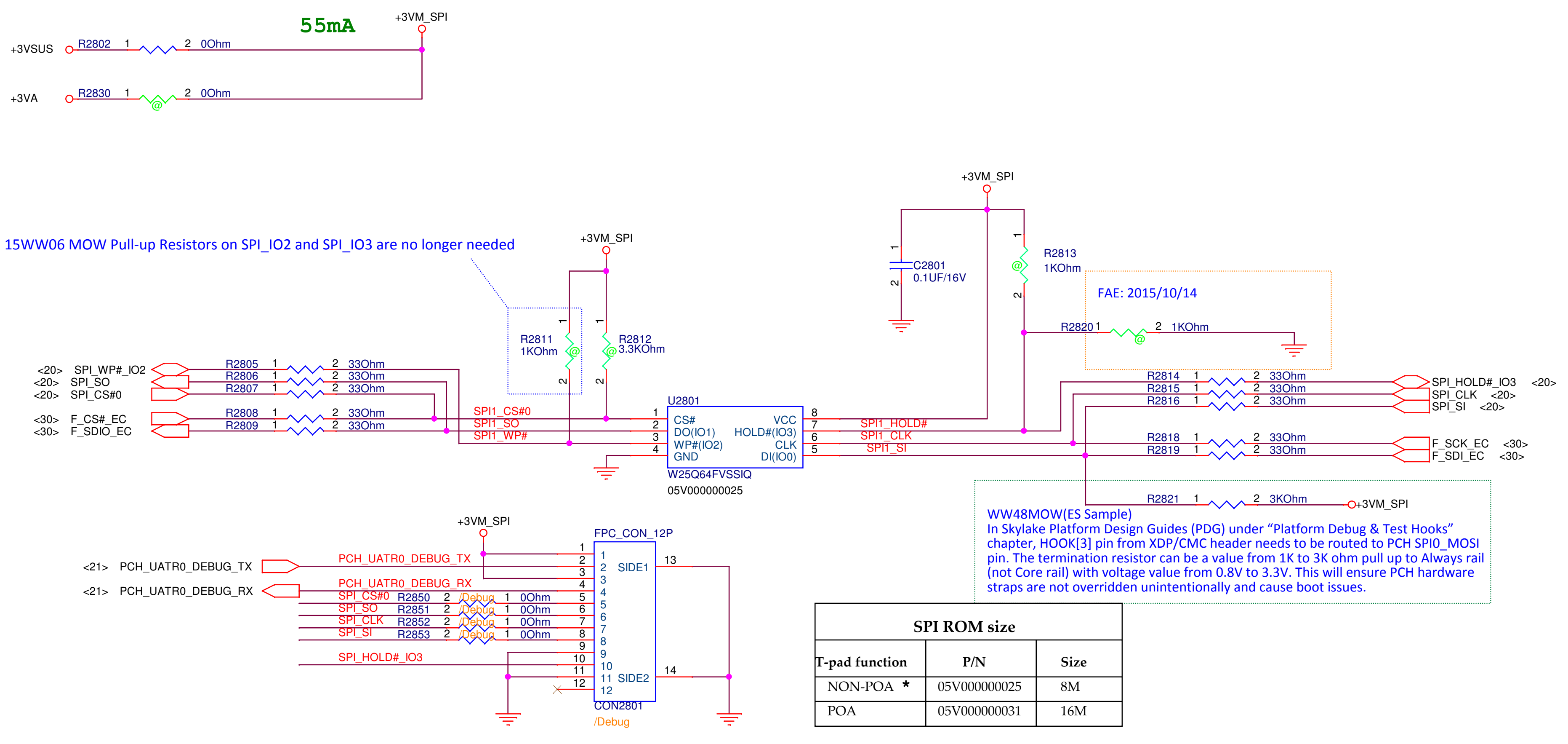
SATA Gen3 Port X 2
PCIe Gen3 Lane X 5
USB3 Port X 3
All HSIO disabled (basic comsunption)
=0.154x5+0.132x2+0.132x3 = 1.43A



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4

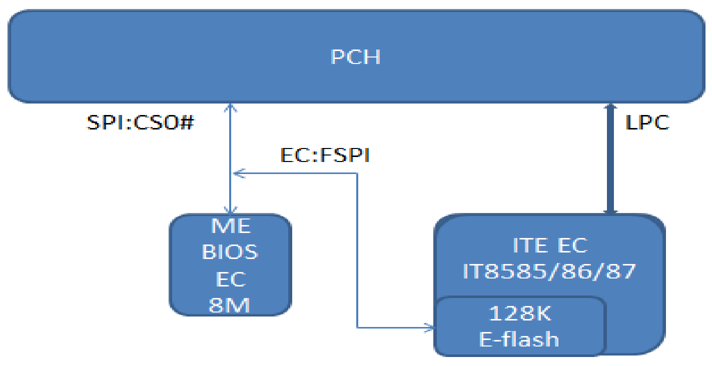
Title	PCH(7)_POWER		
Engineer:	Leo_Zhang		
Size	Project Name		Rev
C	P5HCJ_KBL		1.2
Date:	Monday, June 20, 2016	Sheet 26 of 96	

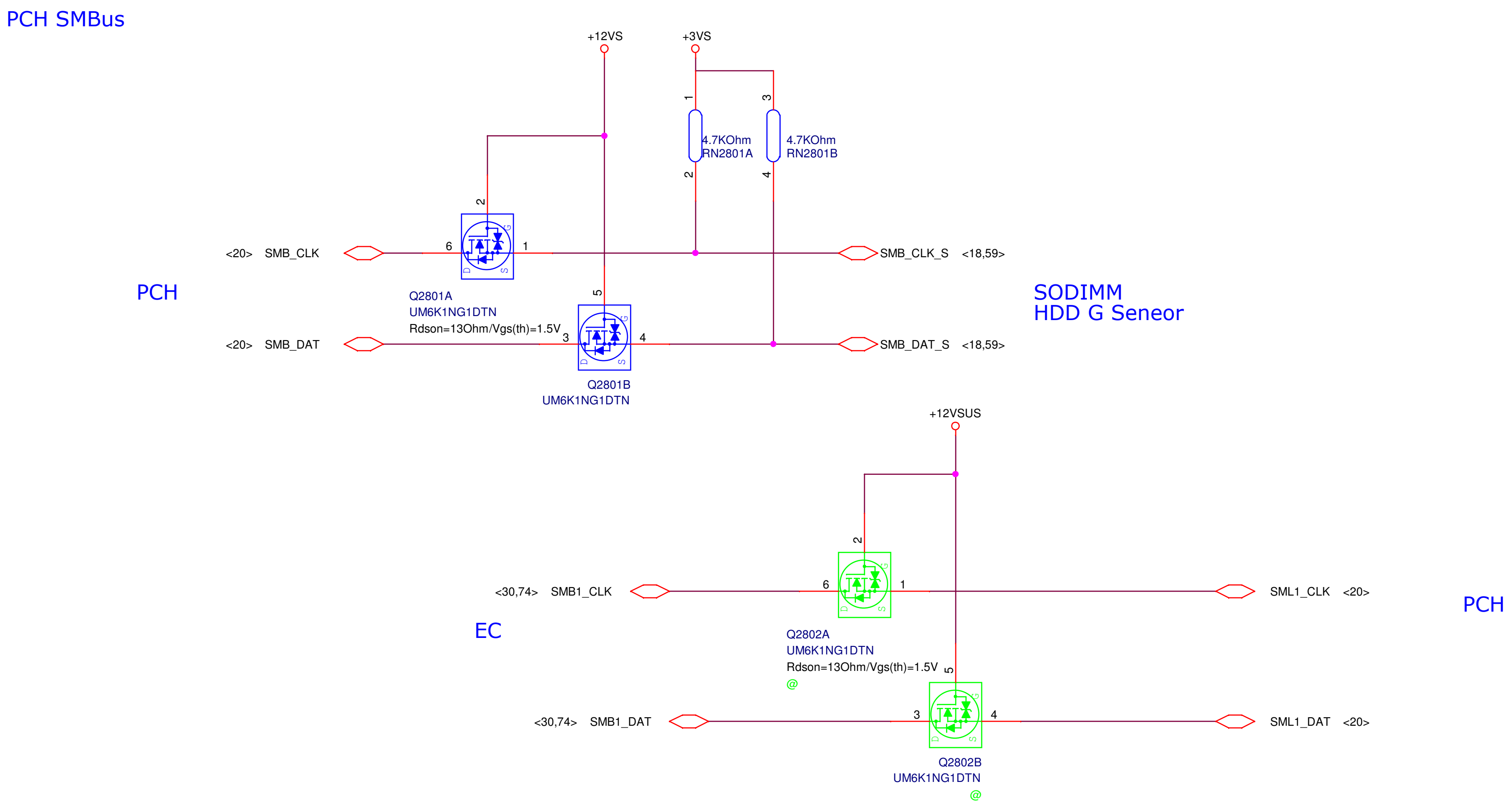
PCH(9)_SPI_SMB



T-pad function	P/N	Size
NON-POA ★	05V000000025	8M
POA	05V000000031	16M

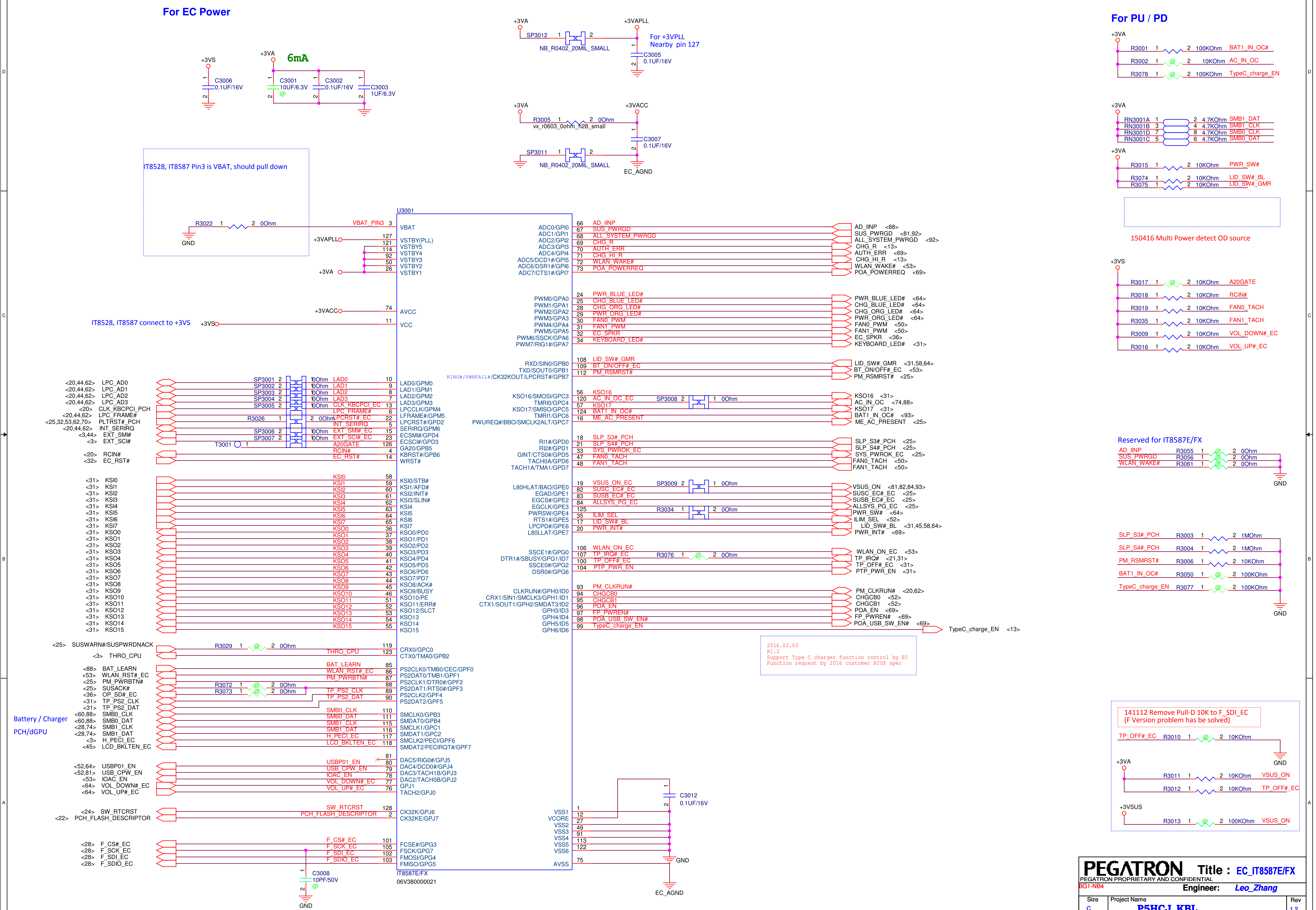
SPI ROM size





30

EC_IT8587E/FX



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4

Title : EC_IT8587E/FX

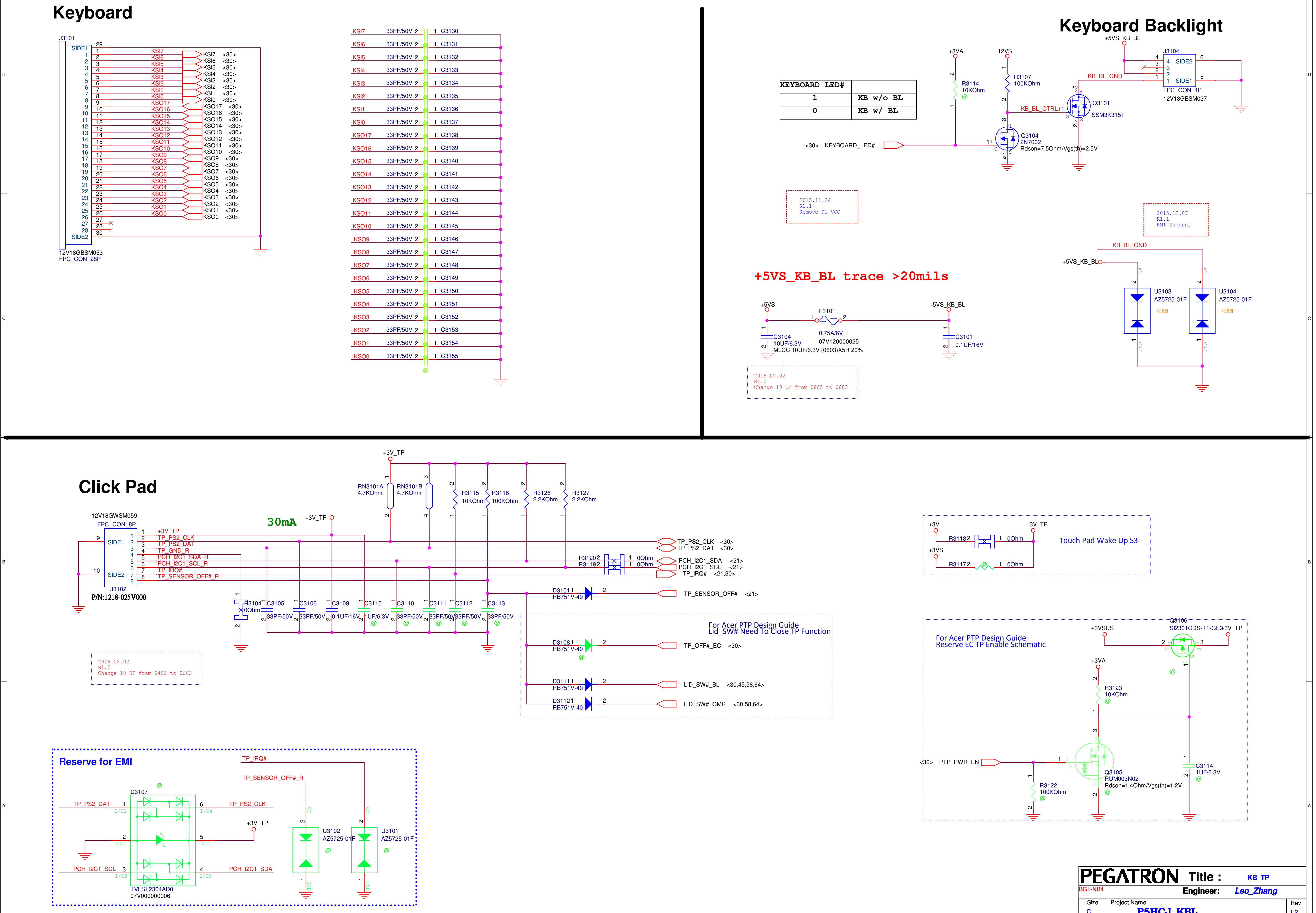
Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 30 of 96

N/A

31 KB_TP



KEYBOARD_LED#	
1	KB w/o BL
0	KB w/ BL

PEGATRON BG1-NB4

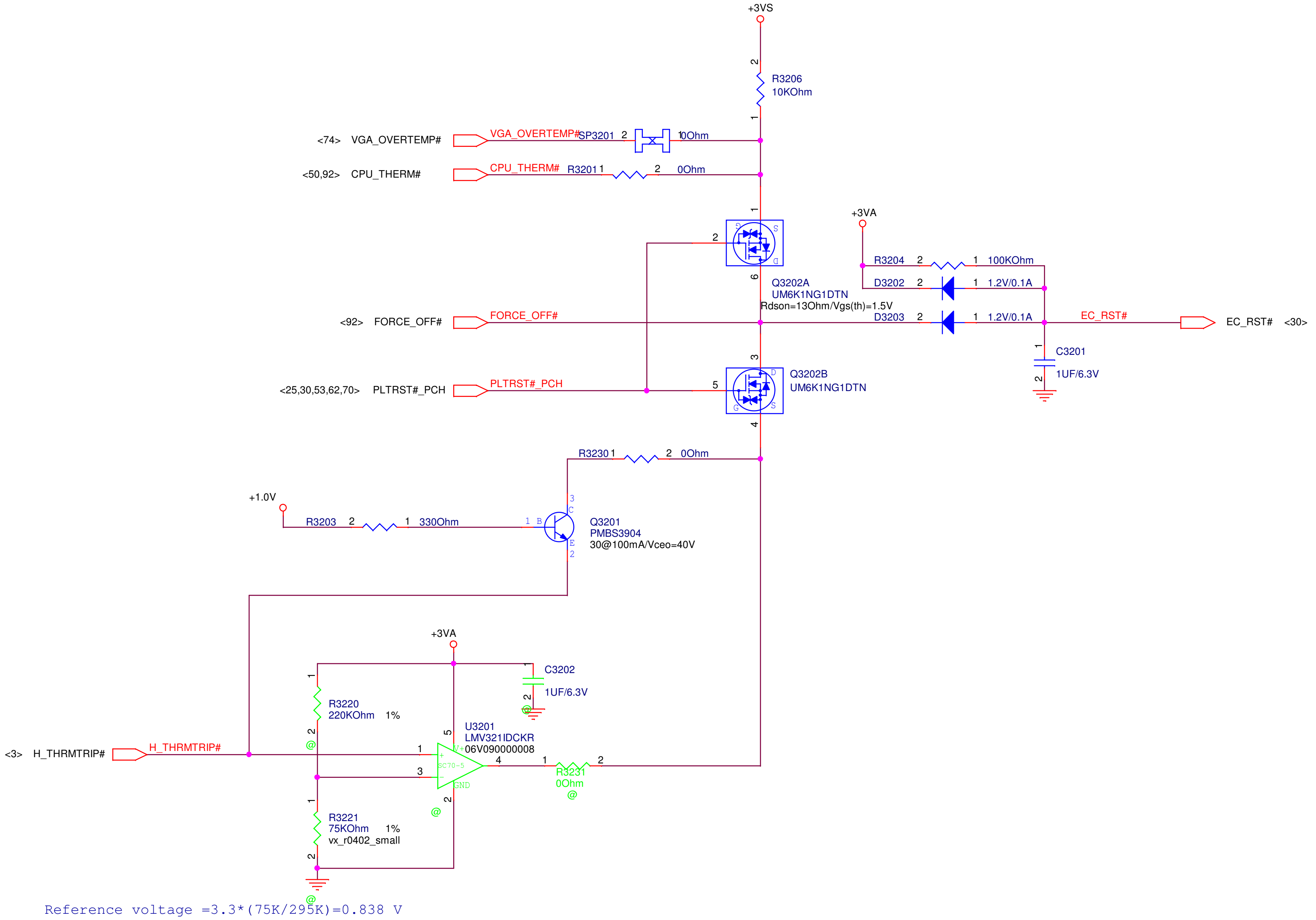
Title : KB_TP

Engineer: Leo_Zhang

Size C | Project Name P5HCJ_KBL | Rev 1.2

Date: Monday, June 20, 2016 | Sheet 31 of 96

RST_Reset Circuit



Reference voltage =3.3*(75K/295K)=0.838 V

PEGATRON PEGATRON PROPRIETARY AND CONFIDENTIAL BG1-NB4	Title : RST_Reset Circuit	Engineer: Leo_Zhang
Size: C	Project Name: P5HCJ_KBL	Rev: 1.2
Date: Monday, June 20, 2016	Sheet 32 of 96	

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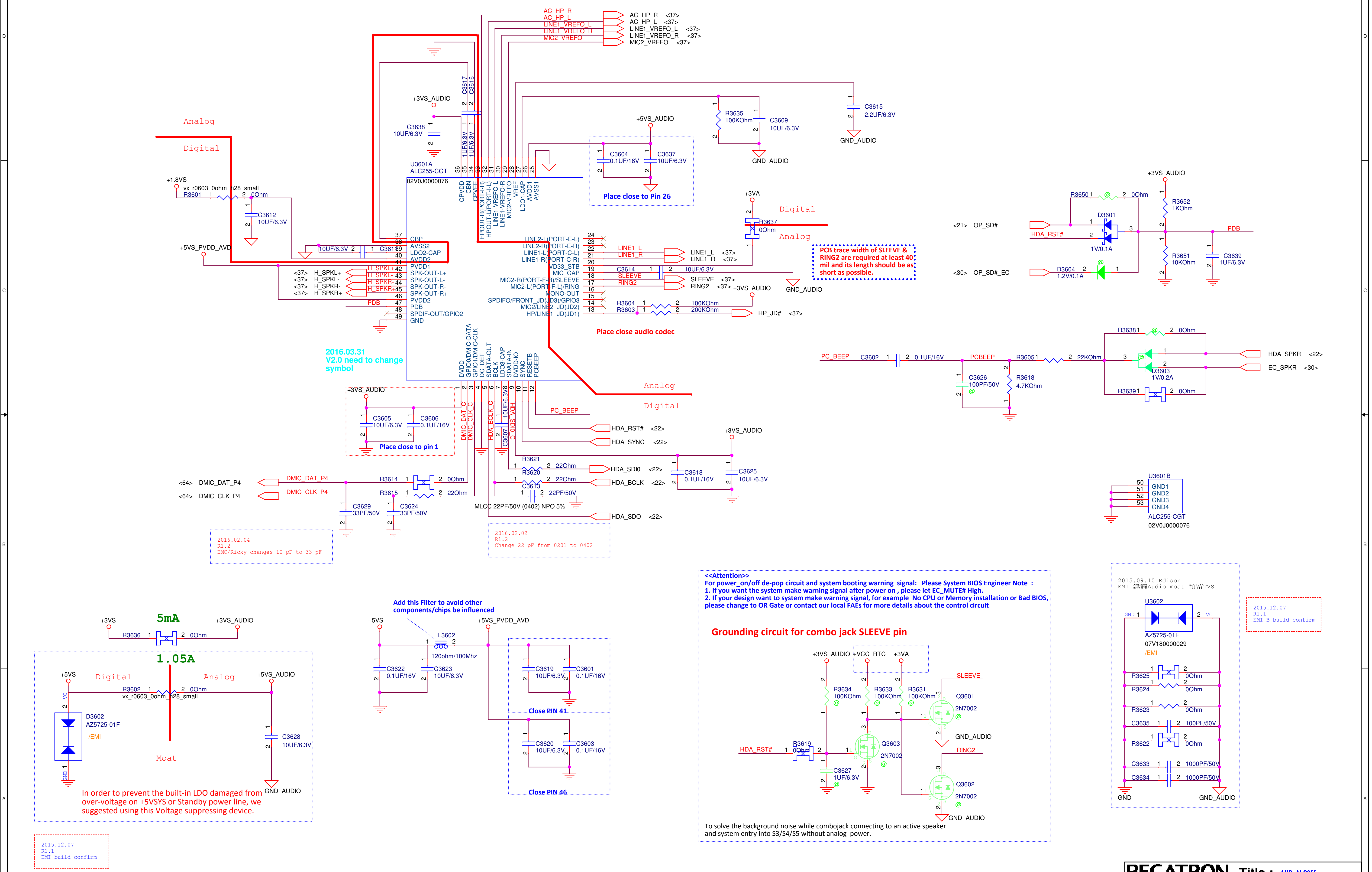
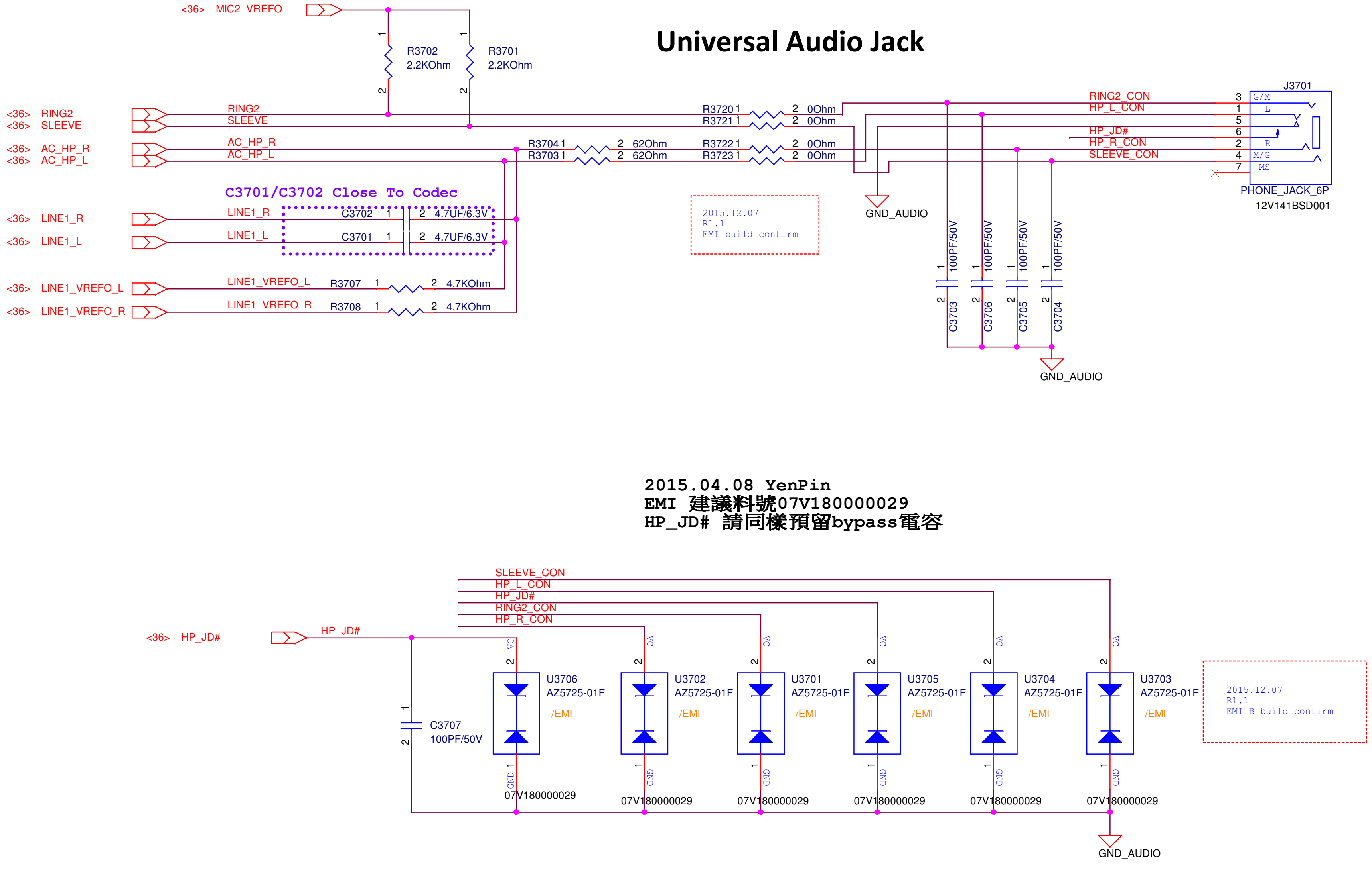
AUD_ALC255



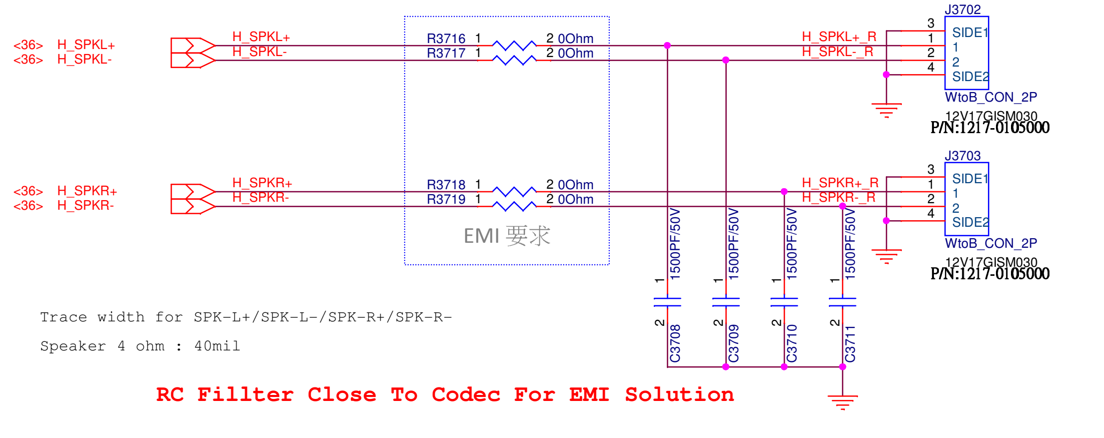
PEGATRON	Title : AUD_ALC255
BG1-NB4	Engineer: Leo_Zhang
Size: C	Project Name: P5HCJ_KBL	Rev: 1.2
Date: Monday, June 20, 2016	Sheet 36 of 96

AUD_HP/DMIC/SPK

Universal Audio Jack



Internal Speaker



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-

Speaker 4 ohm : 40mil

RC Fillter Close To Codec For EMI Solution

PEGATRON	Title : AUD_HP/DMIC/SPK	
PEGATRON PROPRIETARY AND CONFIDENTIAL BG1-NB4	Engineer: Leo_Zhang	
Size C	Project Name P5HCJ_KBL	Rev 1.2
Date: Monday, June 20, 2016	Sheet 37 of 96	

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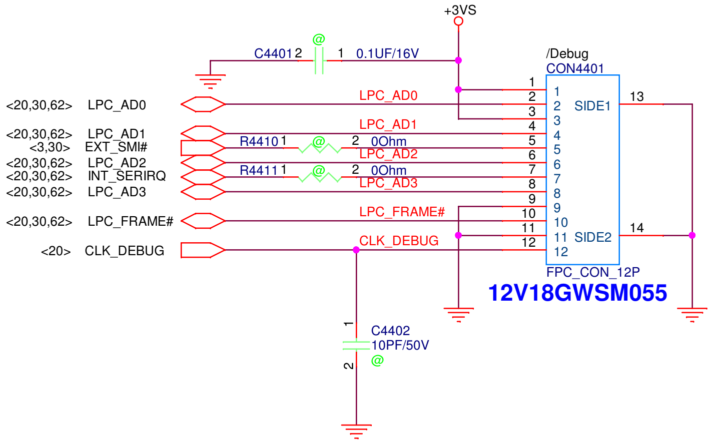
DEBUG CONN



PEGATRON	Title :	DEBUG CONN.
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1-NB4	Engineer:	Leo_Zhang
Size: C	Project Name: P5HCJ_KBL	Rev: 1.2
Date: Monday, June 20, 2016	Sheet 44 of 96	

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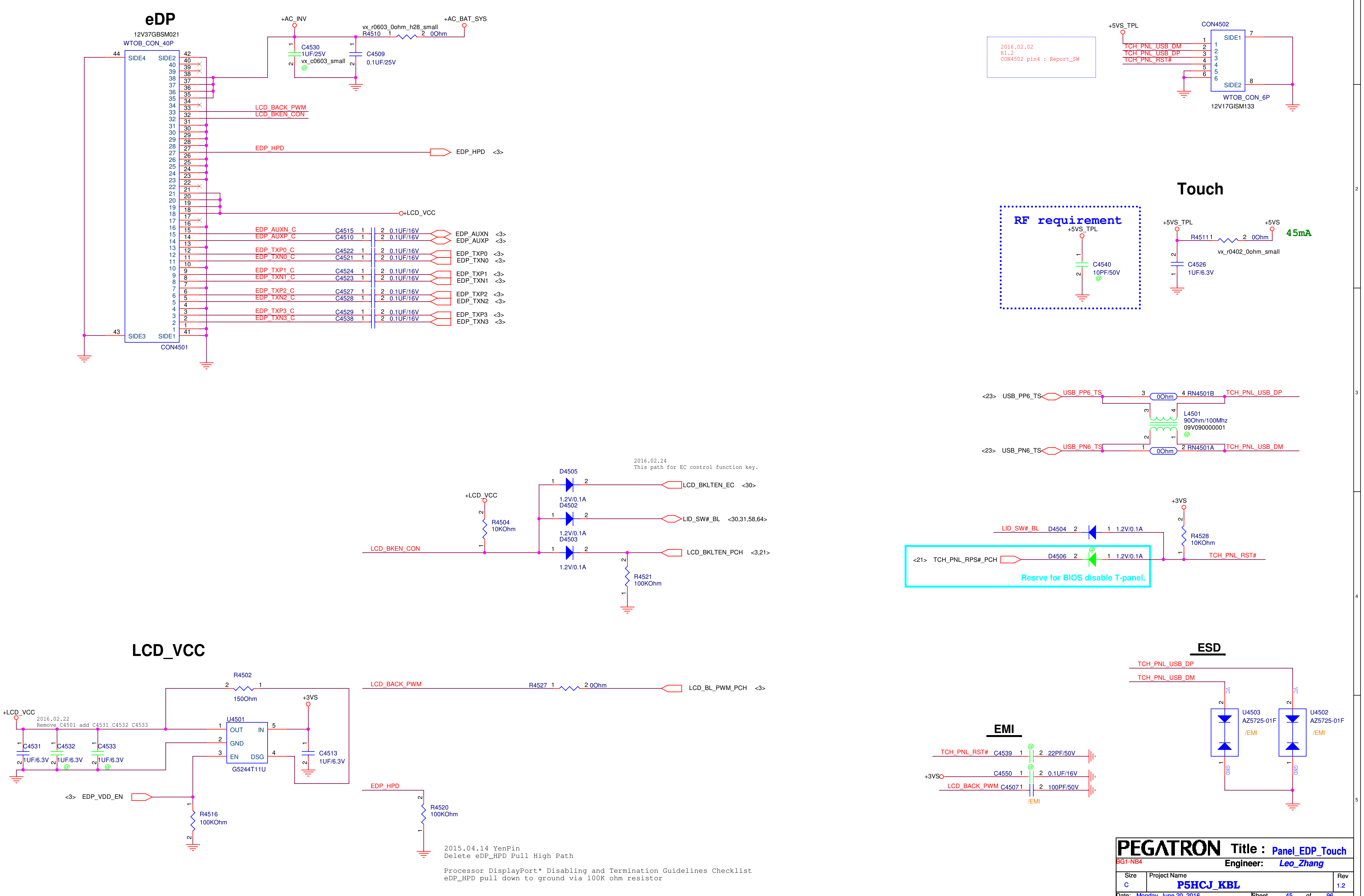
Panel_EDP_Touch



PEGATRON Title : Panel_EDP_Touch

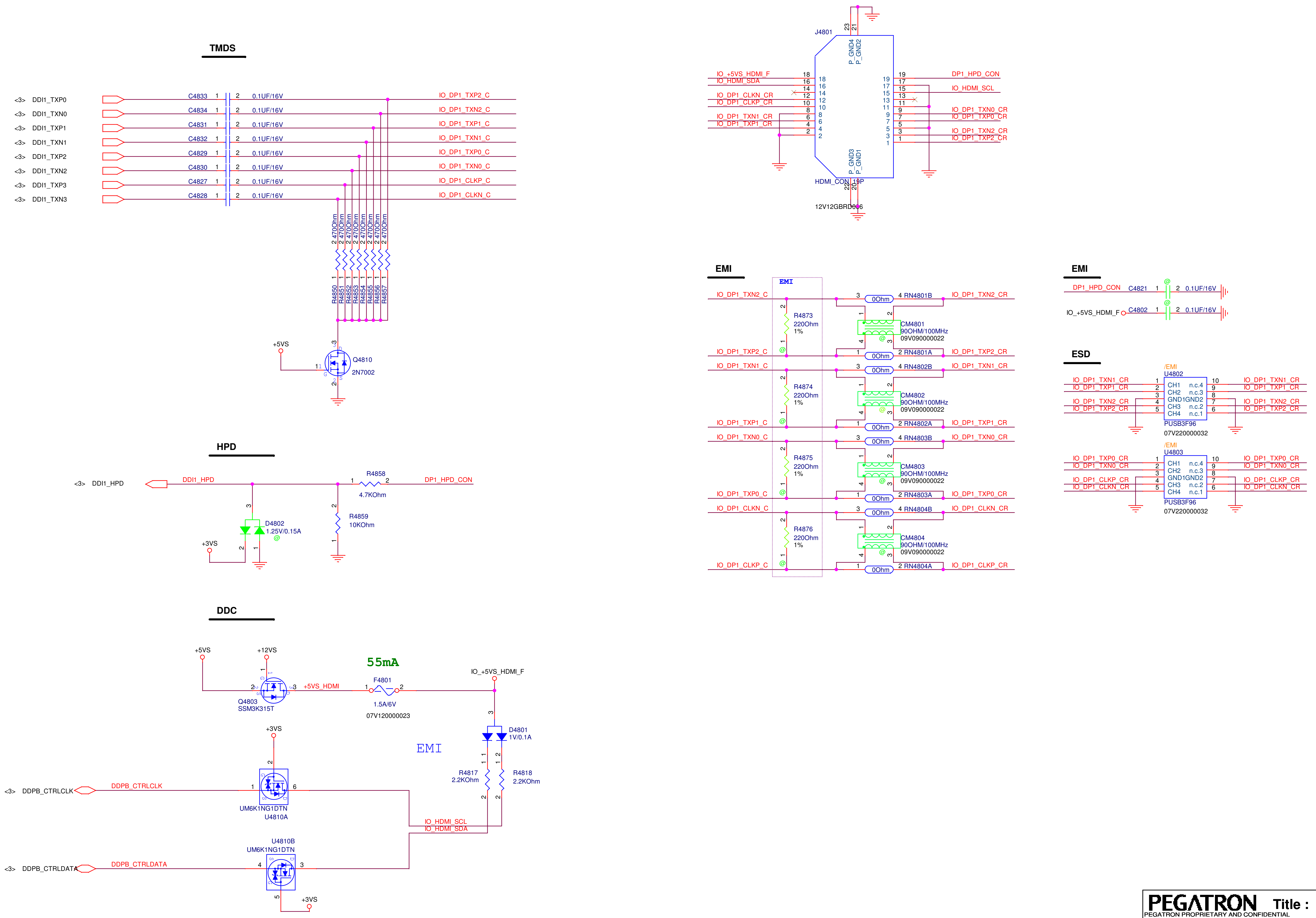
BG1-NB4

Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 45 of 96

HDMI



PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4

Title : HDMI

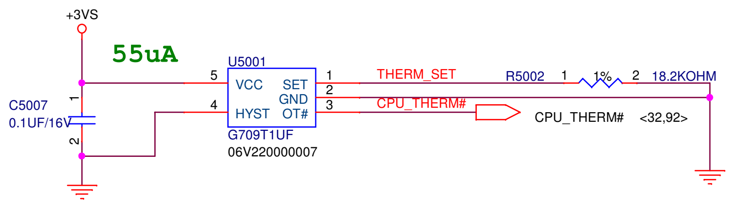
Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 48 of 96

Thermal_Fan

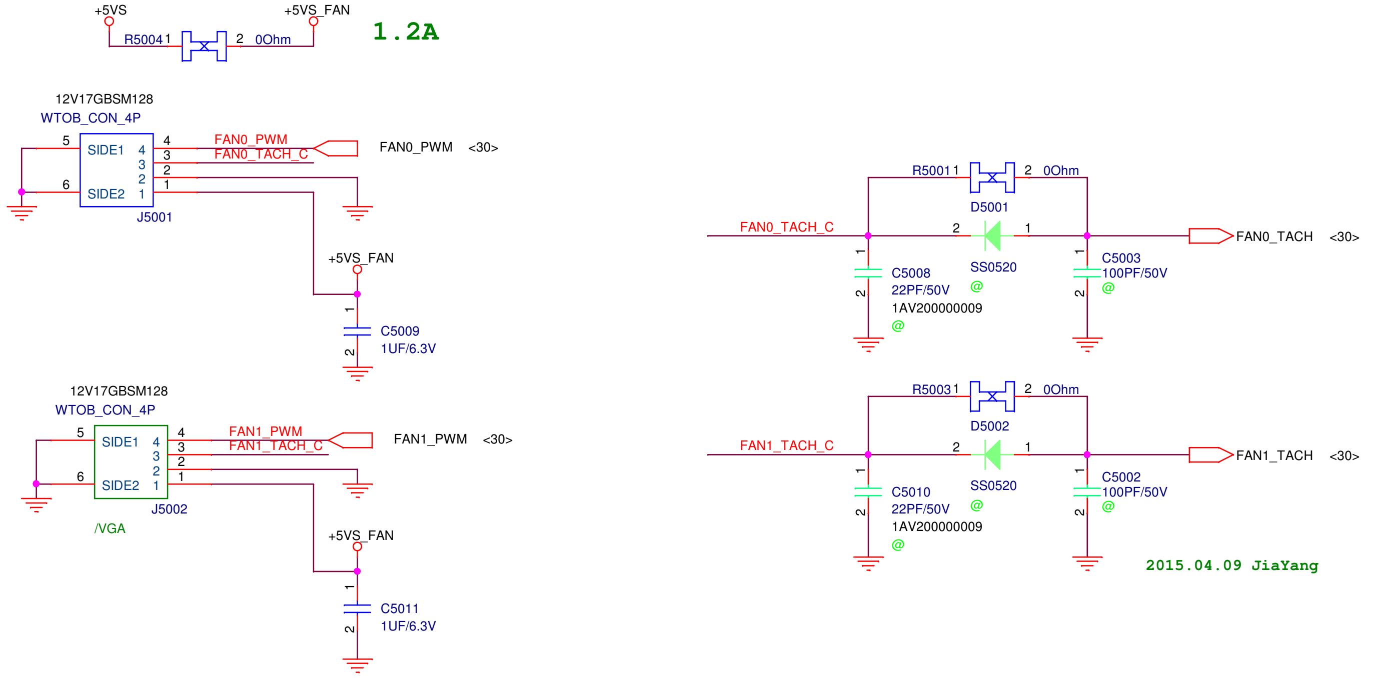
G709Thermal Sensor

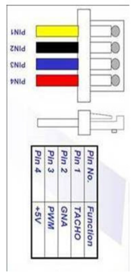


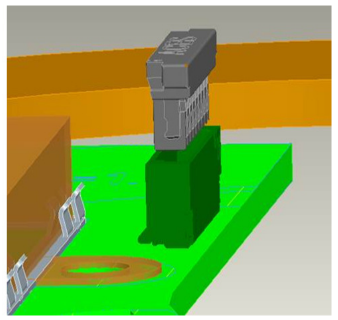
temp setting : 95 degree

RSET(kΩ)= 0.0012T2 − 0.9308T + 96.147

PWM FAN







PEGATRON	Title : Thermal_Fan		
BG1-NB4	Engineer: Leo_Zhang		
Size: C	Project Name: P5HCJ_KBL		Rev: 1.2
Date: Monday, June 20, 2016	Sheet 50 of 96		

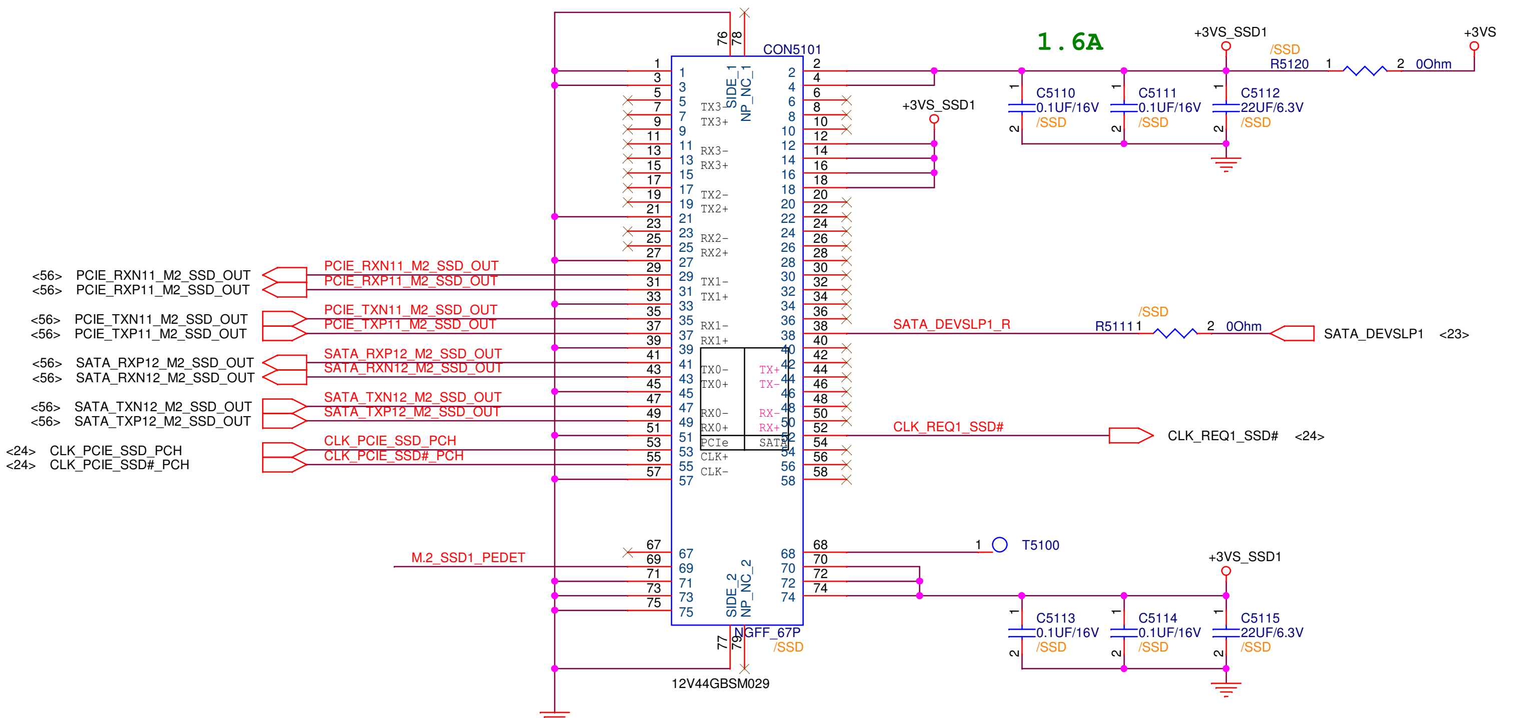
51 NGFF socket B -- SSD (Main)

SATA SSD_HDD

2015.12.10
R1.1
Remove +5VS_HDD

2015.11.12
R1.1
Support PCIE_SSD

2016.01.21
R1.2
Remove PCIE_SSD



PCIe_M.2_Electromechanical_Spec_Rev_0.9-3_07312013_RS_Clean

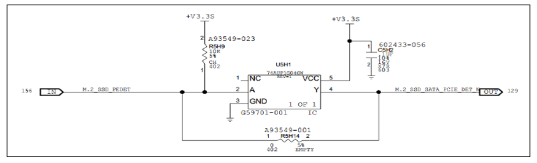
Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

36.3.2.3 PEDET Guidelines

PEDET is the interface detect used by PCH to determine the communication protocol that the M.2 card uses; PCIe* signaling (high) or SATA signaling (low) in conjunction with a platform located pull-up resistor.

Figure 36-6. PEDET Circuitry Example



For Skylake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the interface detect signaling from the M.2 device.

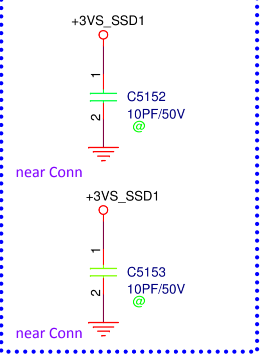
8.1.2 Pin Assignment

The following table describes all pins on the Edge Card connection.

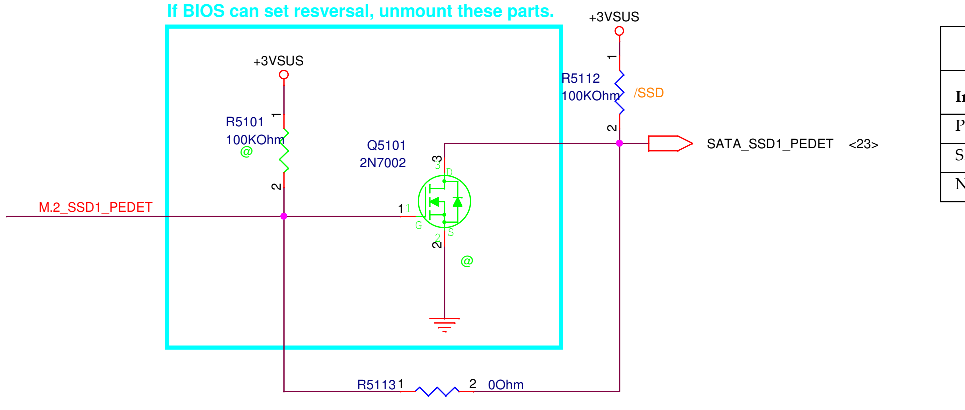
Table 8-1 Pin Assignment

Pin #	Name	Description	Pin #	Name	Description
1	CONFIG_3	Defines module type(low)	2	+3.3V	3.3V Source
3	GND	GND	4	+3.3V	3.3V Source
5	Reserved	NC	6	Reserved	NC
7	Reserved	NC	8	Reserved	NC
9	Reserved	NC	10	DAS/DSS	Drive Activity Signal /
11	Reserved	NC			
Notch			Notch		
			20	Reserved	NC
21	CONFIG_0	Defines module type(low)	22	Reserved	NC
23	Reserved	NC	24	Reserved	NC
25	Reserved	NC	26	Reserved	NC
27	GND	GND	28	Reserved	NC
29	Reserved	NC	30	Reserved	NC
31	Reserved	NC	32	Reserved	NC
33	GND	GND	34	Reserved	NC
35	Reserved	NC	36	Reserved	NC
37	Reserved	NC	38	DEVSLP	DEVSLP signal
39	GND	GND	40	Reserved	NC
41	B+	Host Receiver Differential Signal Pair	42	Reserved	NC
43	B-		44	Reserved	NC
45	GND	GND	46	Reserved	NC
47	A-	Host Transmitter Differential Signal Pair	48	Reserved	NC
49	A+		50	Reserved	NC
51	GND	GND	52	Reserved	NC
53	Reserved	NC	54	Reserved	NC
55	Reserved	NC	56	MFG1	Manufacturing pin. Must be a no-connect on the host board.
57	GND	GND	58	MFG2	
Notch			Notch		
67	Reserved	NC	68	Reserved	NC
69	CONFIG_1	Defines module type(low)	70	+3.3V	3.3V Source
71	GND	GND	72	+3.3V	3.3V Source
73	GND	GND	74	+3.3V	3.3V Source
75	CONFIG_2	Defines module type(low)			

RF requirement



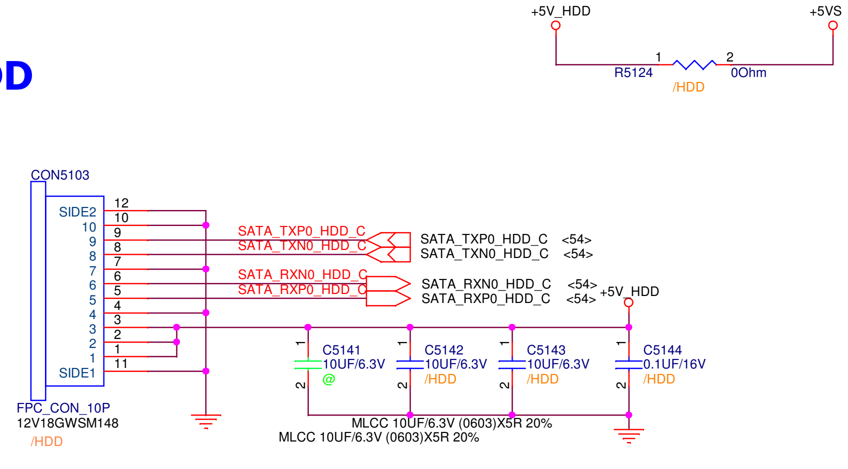
Reserve for resversal.
If BIOS can set resversal, unmount these parts.



SSD type detection

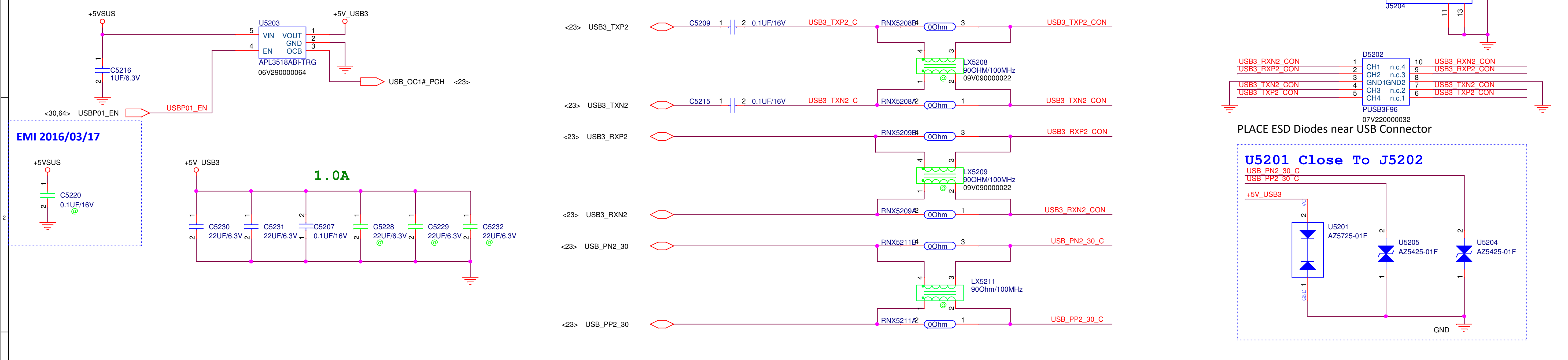
Interface	Device side	PCH side
PCIe	Hi-z	H
SATA	L	L
NO SSD	Hi-z	H

HDD



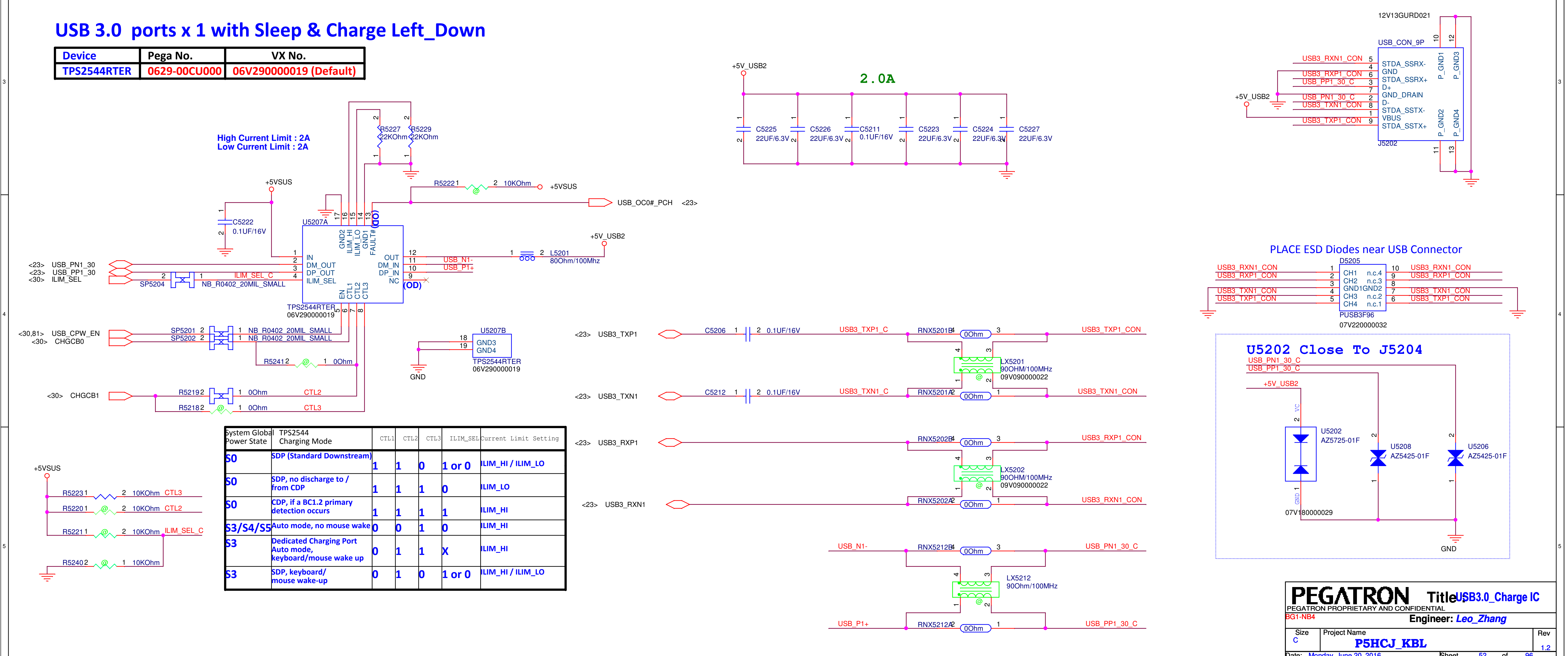
MB_HDD conn	
Pin	Signal name
12	GND
11	GND
10	GND
9	SATA_TXP0_HDD_C
8	SATA_TXN0_HDD_C
7	GND
6	SATA_RXN0_HDD_C
5	SATA_RXP0_HDD_C
4	GND
3	+5V_HDD
2	+5V_HDD
1	+5V_HDD

USB3.0_Charge IC



USB 3.0 ports x 1 with Sleep & Charge Left_Down

Device	Pega No.	VX No.
TPS2544RTER	0629-00CU000	06V290000019 (Default)



System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

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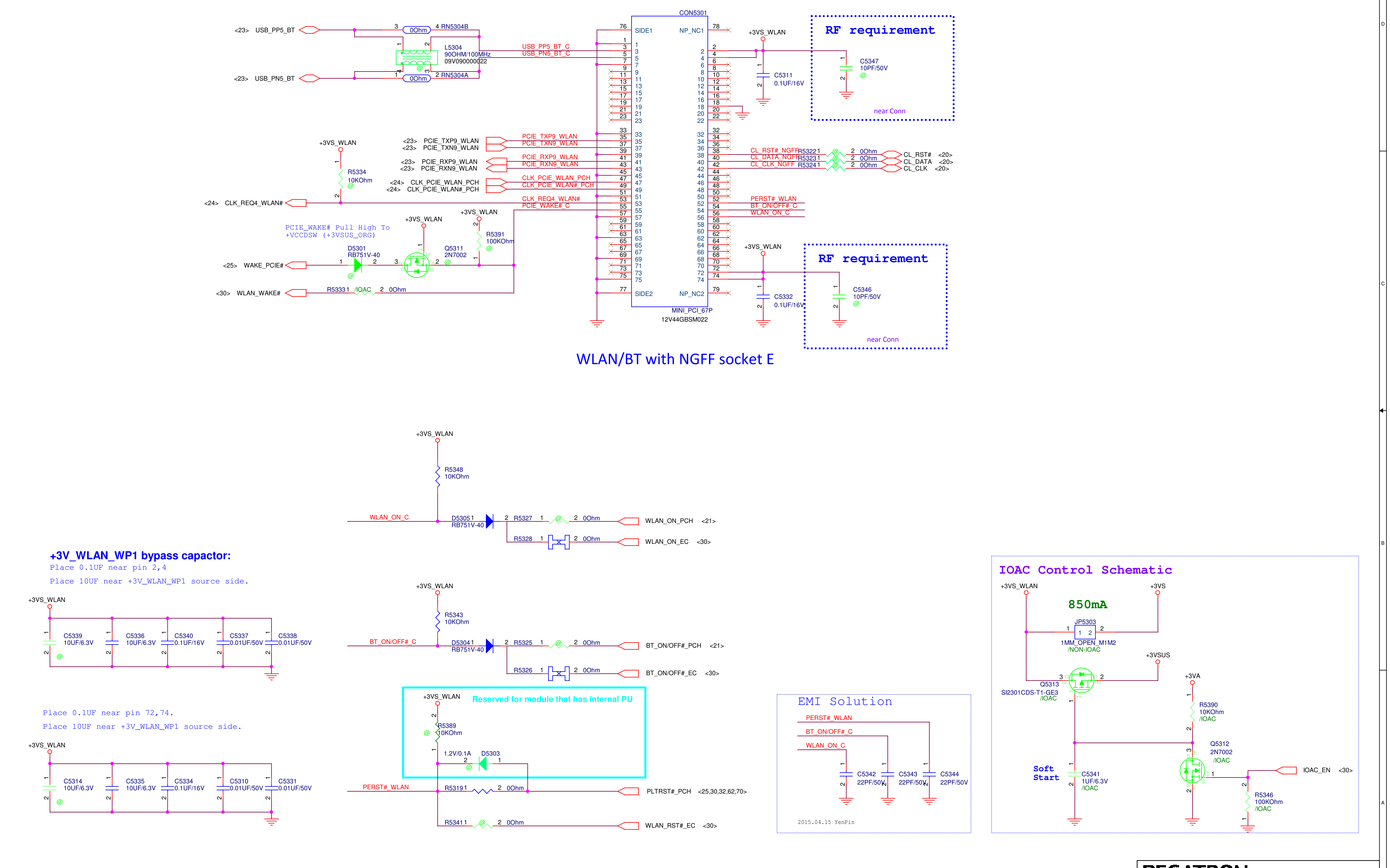
PCIE_WLAN_BT



PEGATRON

Title : PCIE_WLAN_BT

BG1-NB4

Engineer: Leo_Zhang

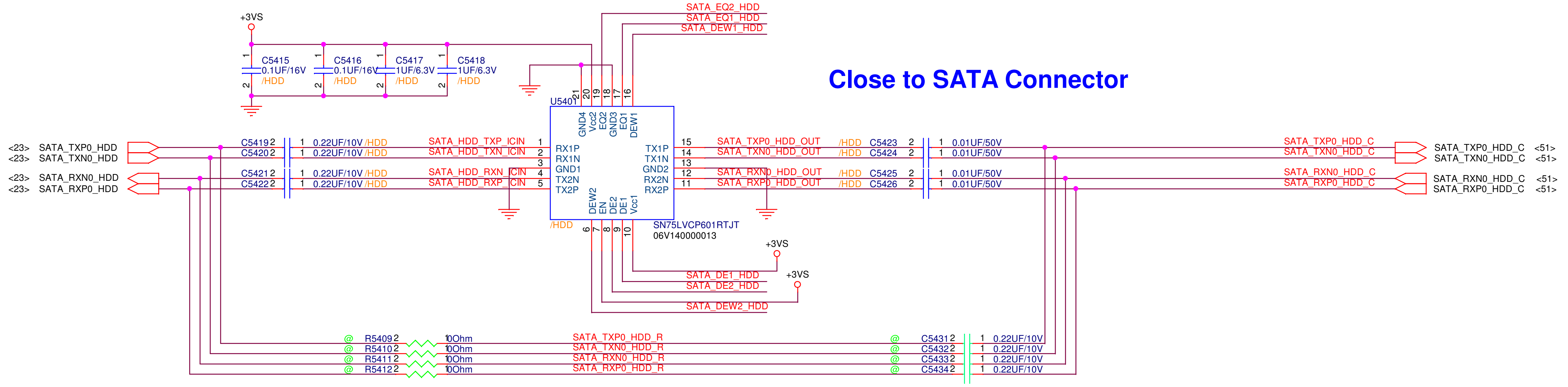
Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 53 of 96

SATA Repeater

HDD Redriver

Close to SATA Connector



EQ1	Resistor
0 dB	NC
7 dB	PD
14 dB	PU

EQ2	Resistor
0 dB	NC
7 dB	PD
14 dB	PU

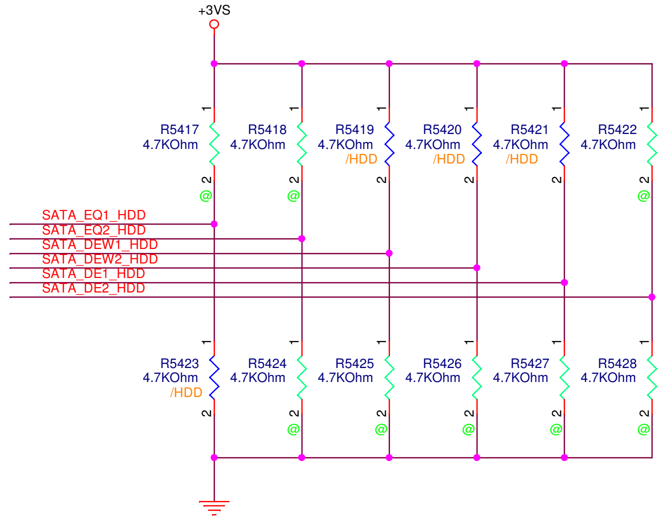
DE1	Resistor
0 dB	PD
-2 dB	PU
-4 dB	NC

DE2	Resistor
0 dB	PD
-2 dB	PU
-4 dB	NC

DEW1	Resistor
Short	PD
Long	PU

DEW2	Resistor
Short	PD
Long	PU

EN	Resistor
Standby	PD
Normal	PU



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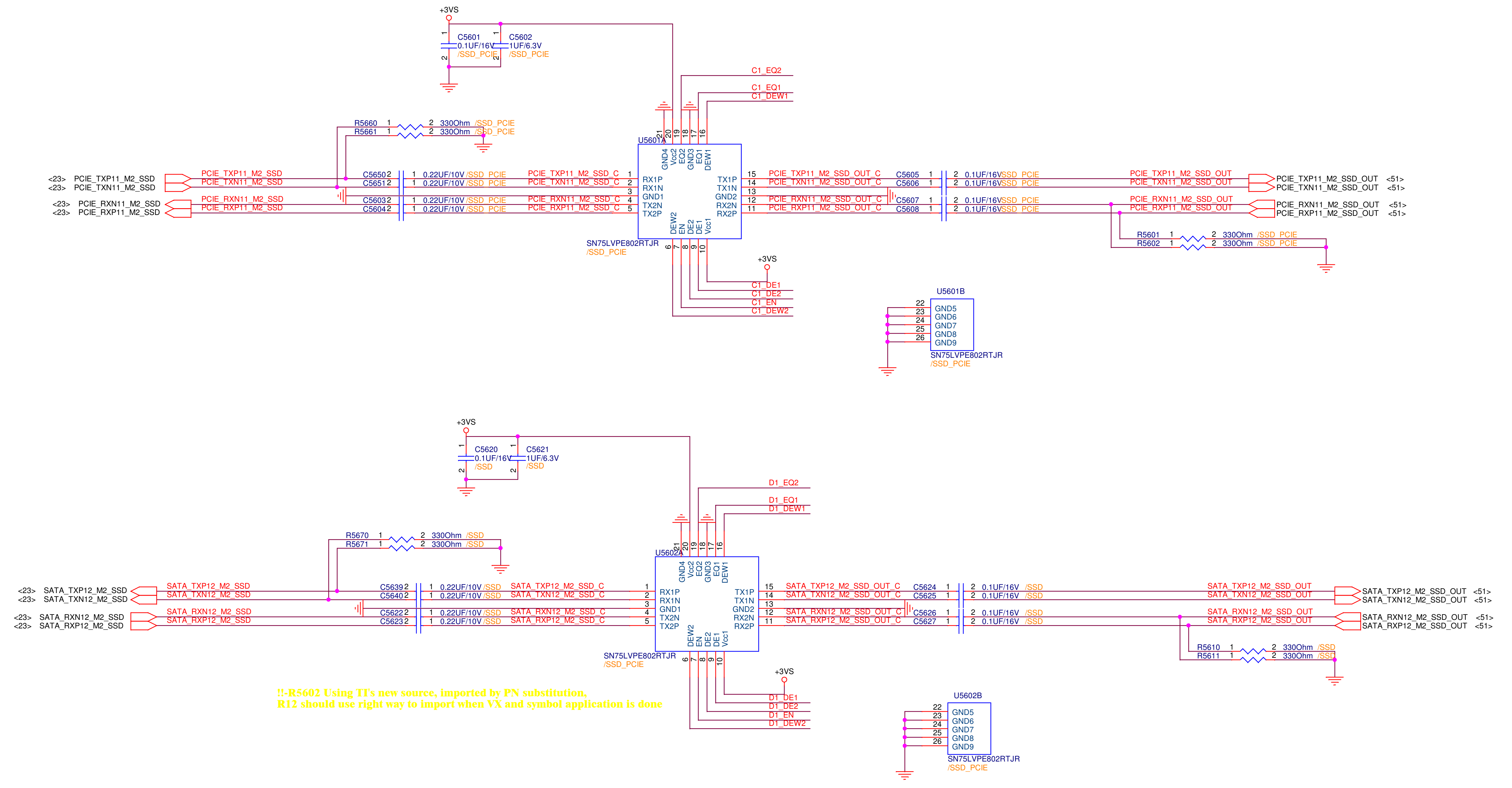
PCIE Re-driver



For project vendor suggest

Equalizer control

EQ1 / EQ2	Channel 1 / Channel 2
NC	0 dB (Default)
H	7 dB
L	14 dB

De-Emphasis setting

DE1 / DE2	Channel 1 / Channel 2
NC	-4 dB (Default)
H	0 dB
L	-2 dB

De-Emphasis width control

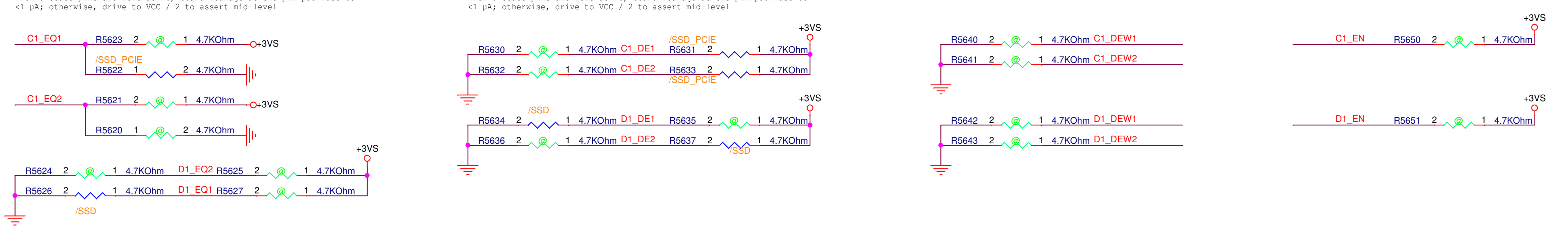
DEW1 or DEW2	Channel 1 Channel 2
H	De-emphasis plse duration, Long (Default)
L	De-emphasis plse duration, Sfort

Device enable

EN	Device
H	Device enabled (Default)
L	Device in standby mode

Internally biased to VCC / 2 with >200-Ωk pullup or ulldown.
When 3-state pins are left as NC, board leakage at the pin pad must be
<1 µA; otherwise, drive to VCC / 2 to assert mid-level

Internally biased to VCC / 2 with >200-Ωk pullup or ulldown.
When 3-state pins are left as NC, board leakage at the pin pad must be
<1 µA; otherwise, drive to VCC / 2 to assert mid-level



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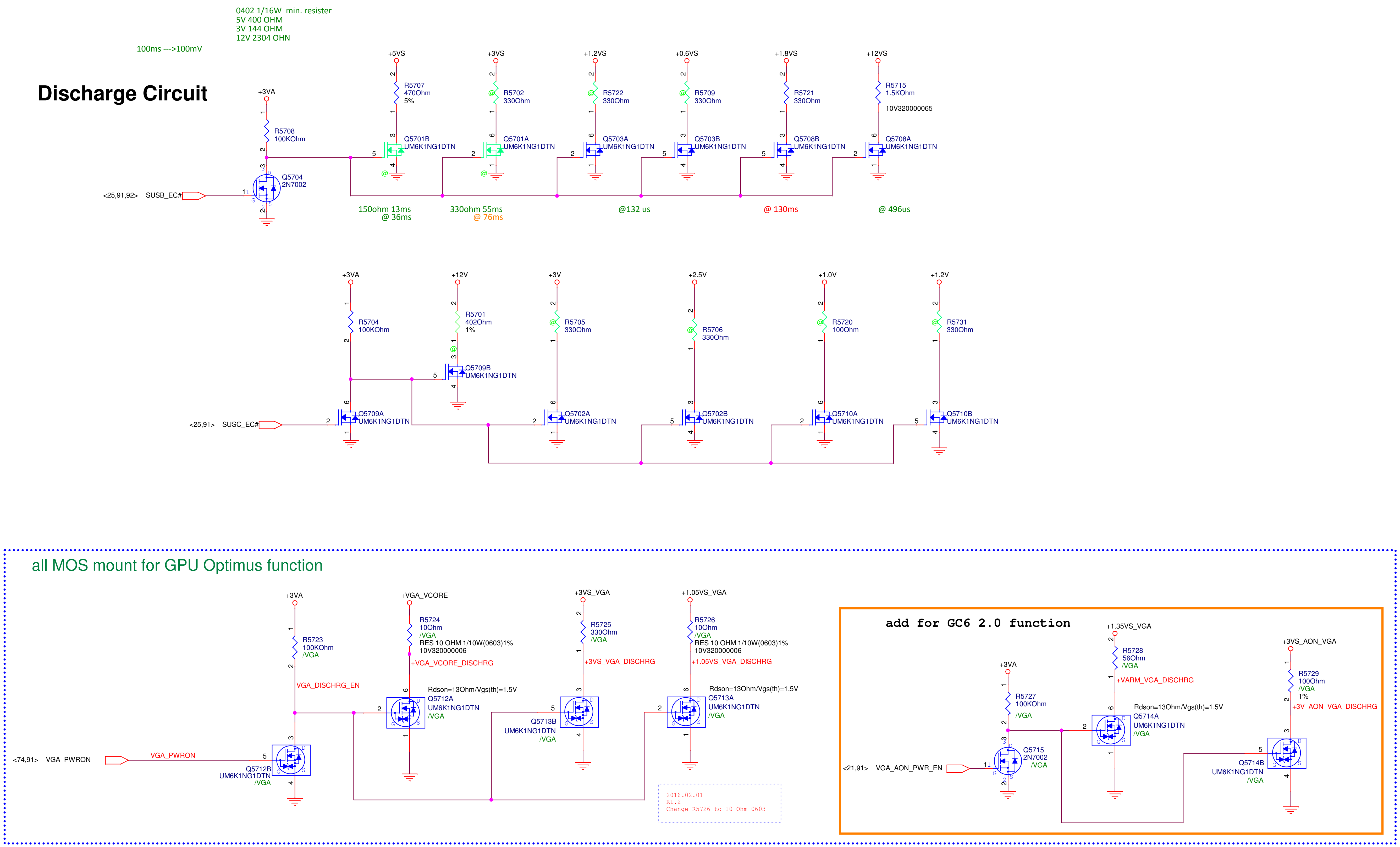
DISCHARGE



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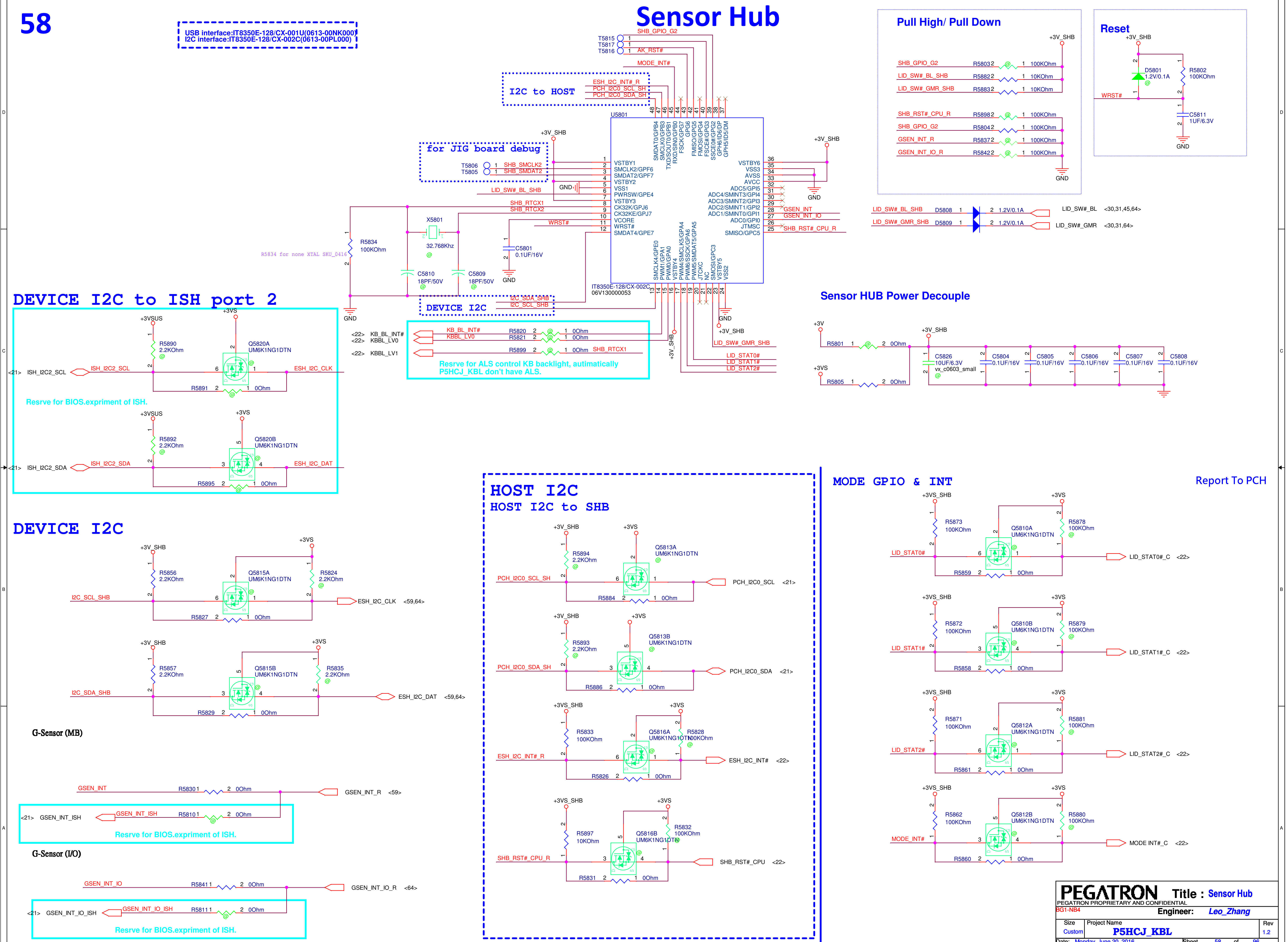
Sensor Hub



PEGATRON Title : Sensor Hub

PEGATRON PROPRIETARY AND CONFIDENTIAL

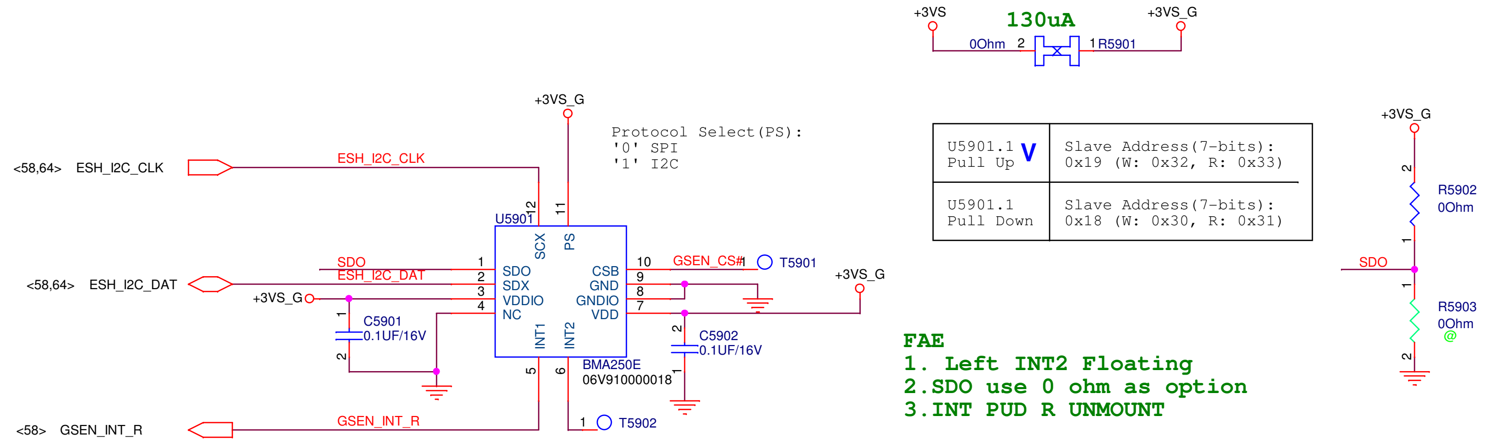
BG1-NB4

Engineer: Leo_Zhang

Size	Project Name	Rev
Custom	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 58 of 96

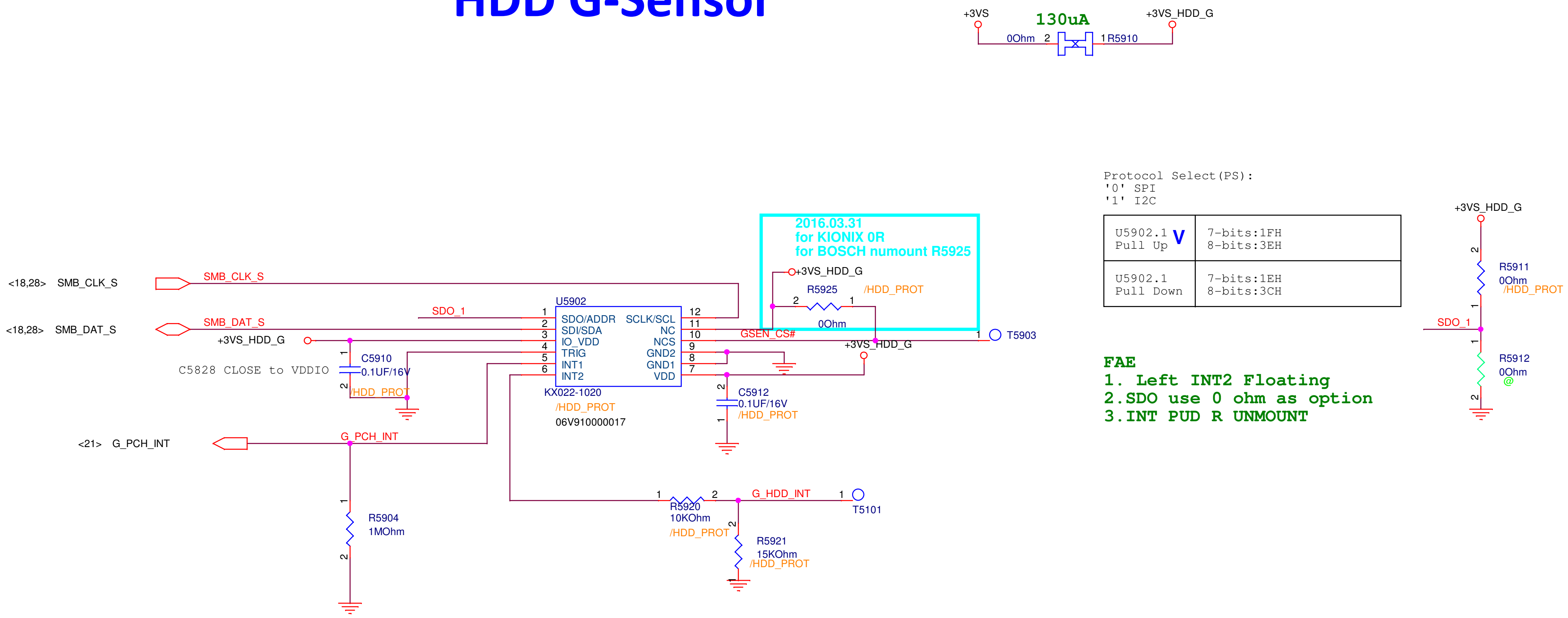
G Sensor



U5901.1 Pull Up V	Slave Address(7-bits): 0x19 (W: 0x32, R: 0x33)
U5901.1 Pull Down	Slave Address(7-bits): 0x18 (W: 0x30, R: 0x31)

FAE
1. Left INT2 Floating
2. SDO use 0 ohm as option
3. INT PUD R UNMOUNT

HDD G-Sensor

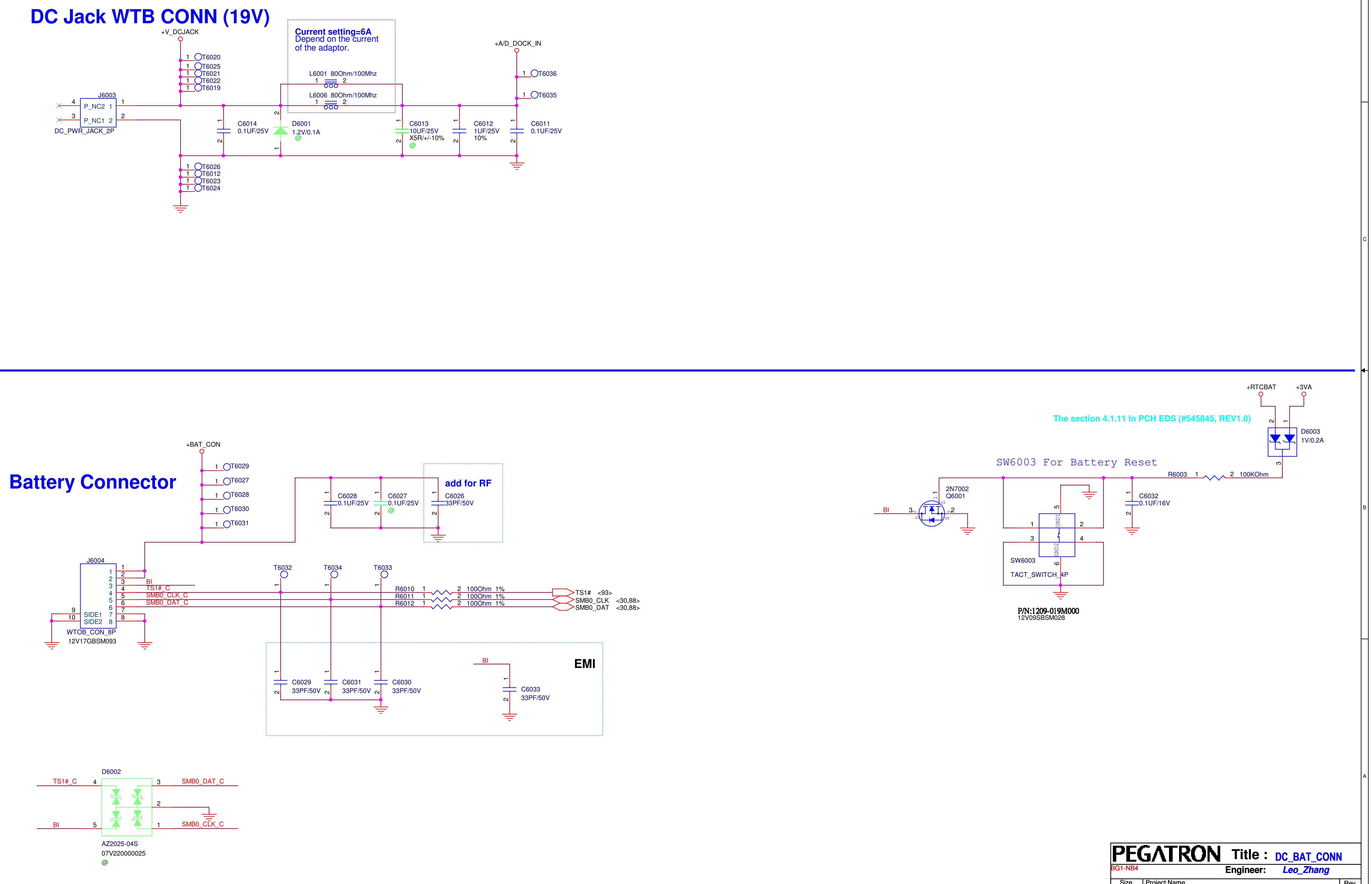


U5902.1 Pull Up V	7-bits:1FH 8-bits:3EH
U5902.1 Pull Down	7-bits:1EH 8-bits:3CH

FAE
1. Left INT2 Floating
2. SDO use 0 ohm as option
3. INT PUD R UNMOUNT

60

DC_BAT_CONN



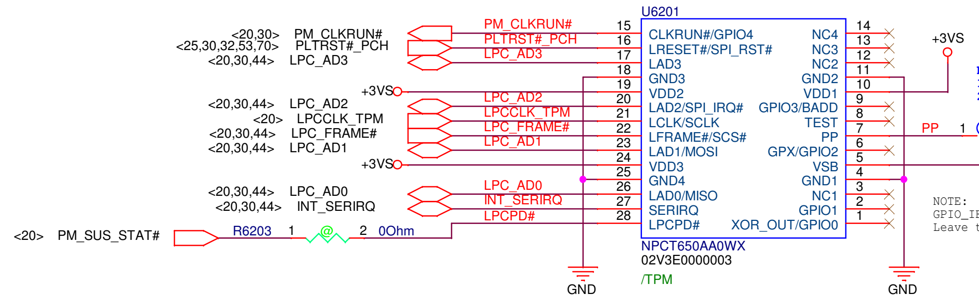
PEGATRON Title : DC_BAT_CONN

BG1-NB4 Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

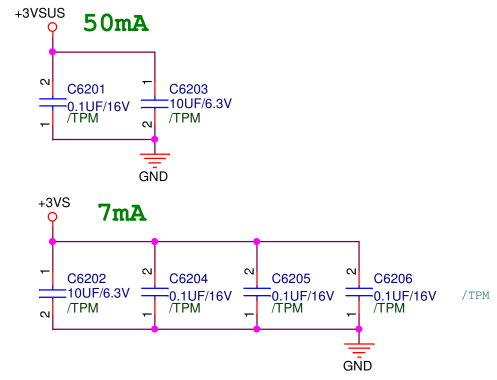
Date: Monday, June 20, 2016 Sheet 60 of 96

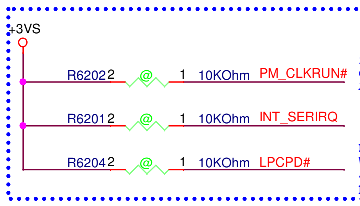
TPM NPCT650



NOTE:
1) The PP is an input signal with configurable polarity.
2) By default the PP functionality is disabled.

NOTE:
GPIO_IF[0..3] and PP are optional.
Leave them open if not used.





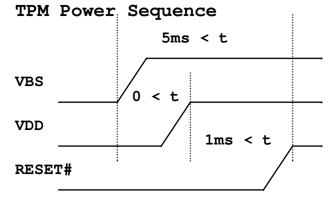
2015.04.09 YenPin
Chipset Have Pulled High 10Kohm
At PM_CLKRUN# and INT_SERIRQ

Note:
When LPCPD# functionality is not required, an internal pull-up resistor allows this pin to be left floating.

TPM

VDD: Power the I/O buffers of the GPIO ports and the Host Interface
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.

TPM Power Sequence

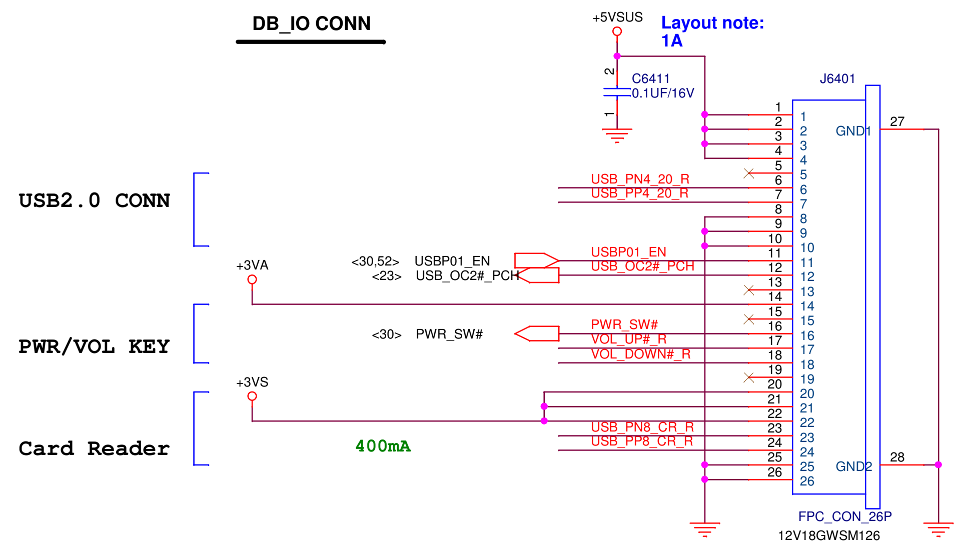


NOTE: RESET# is LRESET#, SPI_RST# or SRESET#.

NOTE:
1) For TPM 1.2:
The TPM VSB pin must be connected to the system's standby voltage (existing at S3 power state).
2) For TPM 2.0:
It is recommended to connect the TPM VSB pin to the system's standby voltage to improve performance.
3) TPM VDD pins should be connected to the same power rail that feeds the Chipset LPC interface.
4) RESET# must be asserted for at least 5 msec after VSB power-up.
5) VSB may come up anytime before VDD power-up, but not after VDD power-up.
6) RESET# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.

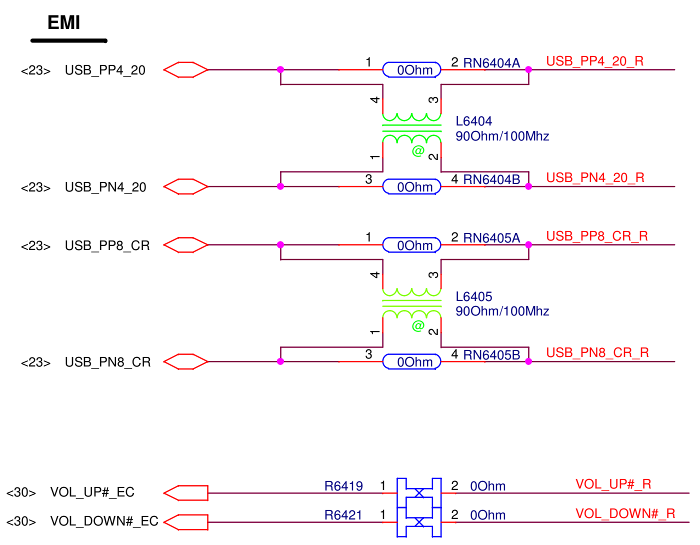
BYPASS EC SEQUENCE

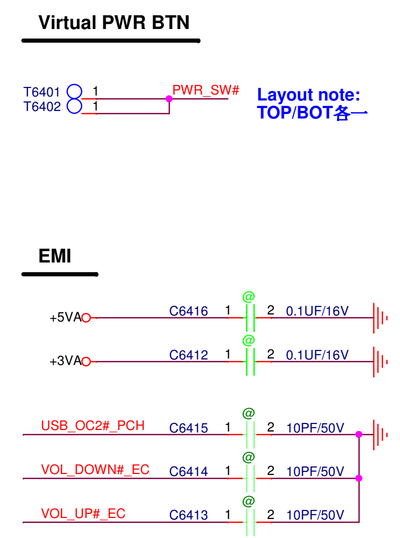
DB CONN



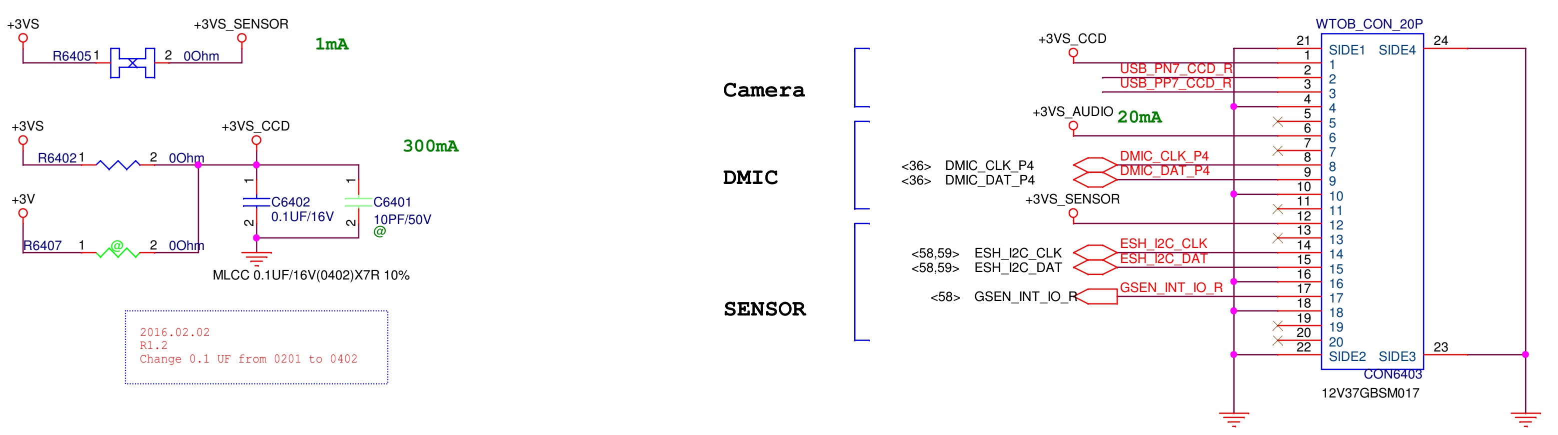
MB Connector Pin Define

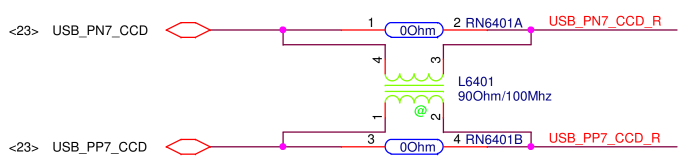
	R15
1	+5VSUS
2	+5VSUS
3	+5VSUS
4	+5VSUS
5	NC
6	USB_PN4_20_R
7	USB_PP4_20_R
8	GND
9	GND
10	GND
11	USBP01_EN
12	USB_OC2#_PCH
13	NC
14	+3VA
15	NC
16	PWR_SW#
17	VOL_UP#
18	VOL_DOWN#
19	NC
20	+3VS
21	+3VS
22	+3VS
23	USB_PN8_CR
24	USB_PP8_CR
25	GND
26	GND

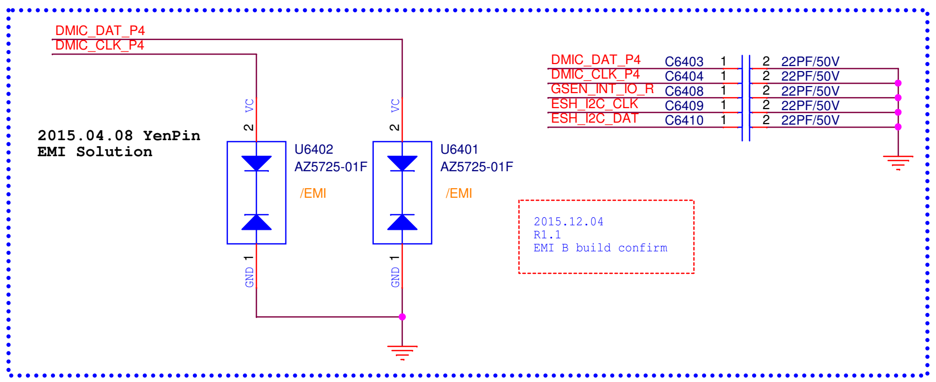




Sensor Board Conn



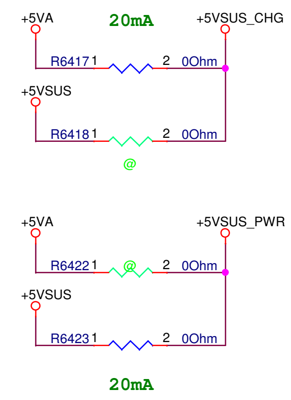




MB Connector Pin Define

	R15
1	+3VS_CCD
2	USB_PN7_CCD_R
3	USB_PP7_CCD_R
4	GND
5	NC
6	+3VS_AUDIO
7	NC
8	DMIC_CLK_P4
9	DMIC_DAT_P4
10	GND
11	NC
12	+3VS_SENSOR
13	NC
14	ESH_I2C_CLK
15	ESH_I2C_DAT
16	GND
17	GSEN_INT_IO_R
18	GND
19	NC
20	NC

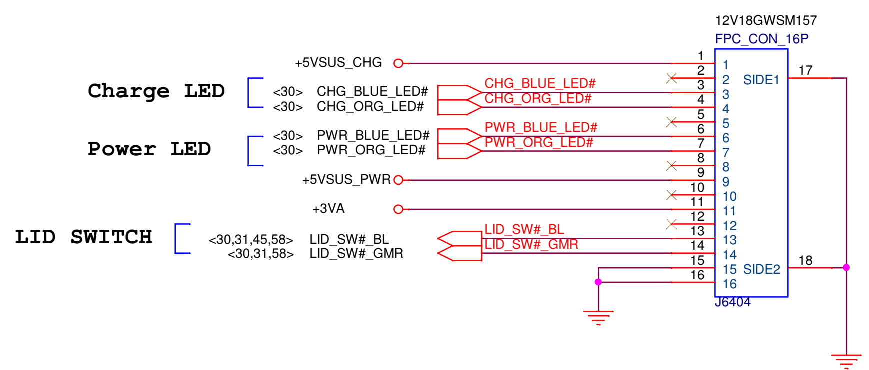
2016.02.03
R1.2
By 客戶BIOS/Erik回覆，當Battery電量<= 3%時，
若在S4/S5下按下Power button需要flash charging LED並禁止system power on
請將Charge LED的power plan修改至+5VA power plan



MB Connector Pin Define

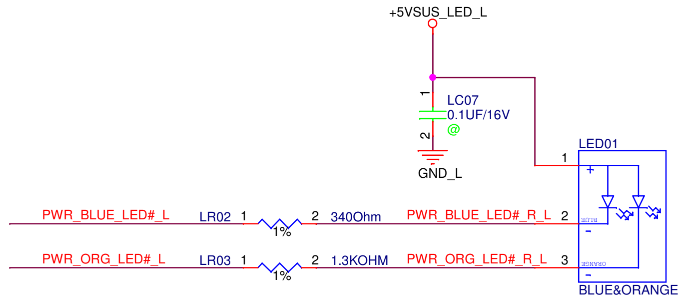
	R15
1	+5VSUS_CHG
2	NC
3	CHG_BLUE_LED#
4	CHG_ORG_LED#
5	NC
6	PWR_BLUE_LED#
7	PWR_ORG_LED#
8	NC
9	+5VSUS_PWR
10	NC
11	+3VA
12	NC
13	LID_SW#_BL
14	LID_SW#_GMR
15	GND
16	GND

LED Board Conn

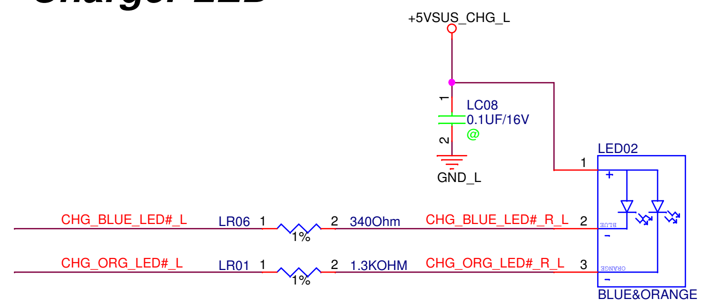


LED Board

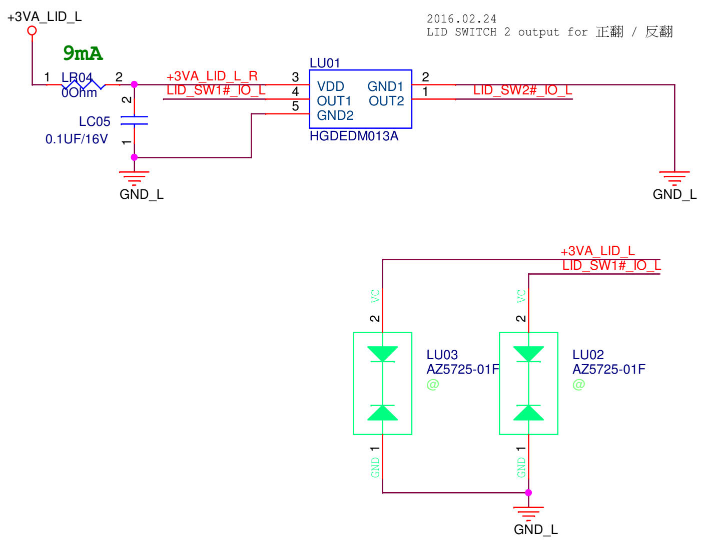
POWER LED

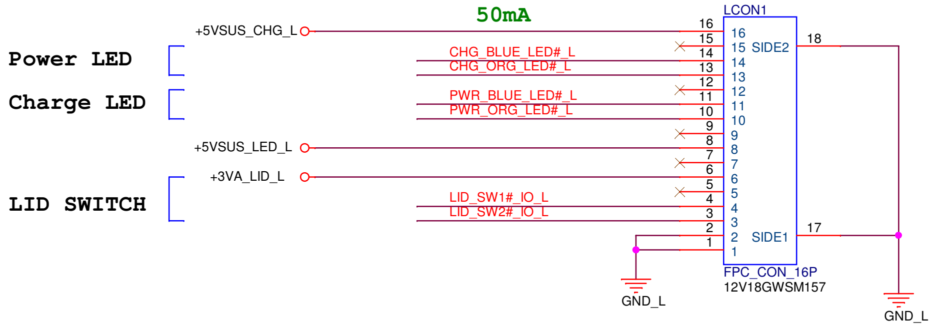


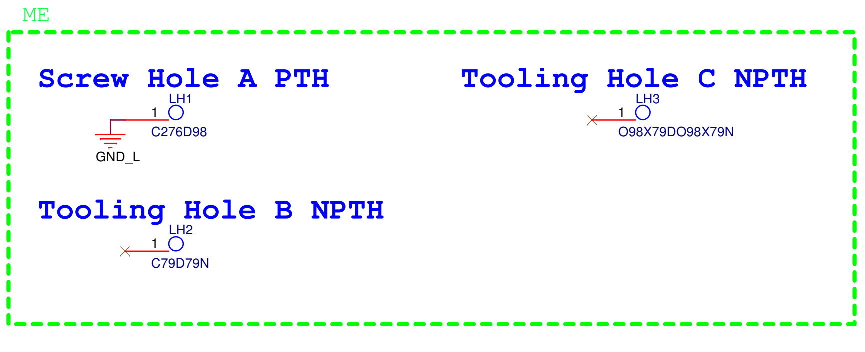
Charger LED



LID Switch







PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LED Board

BG1/HW4

Engineer: Leo_Zhang

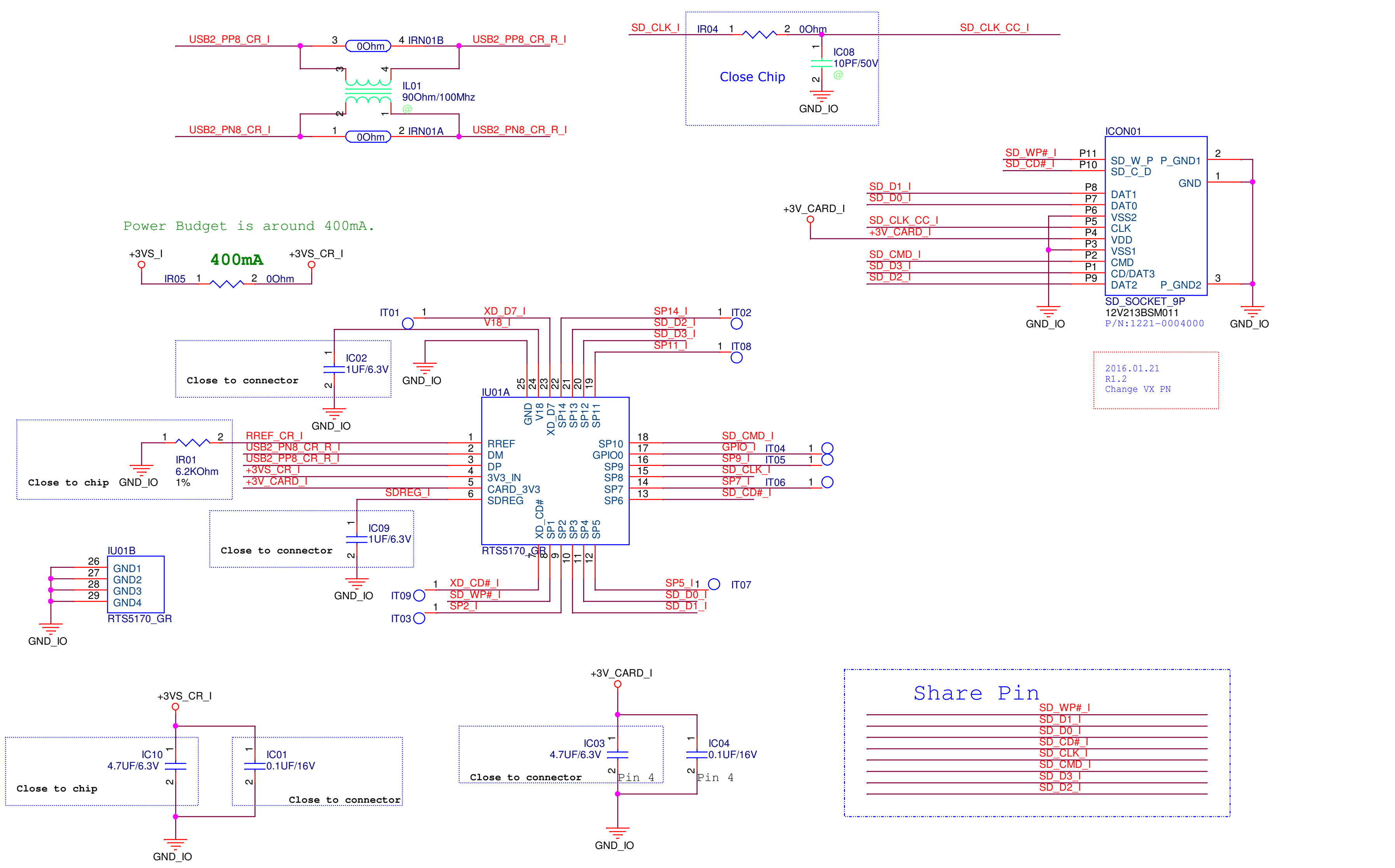
Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 65 of 110

66

IO Board

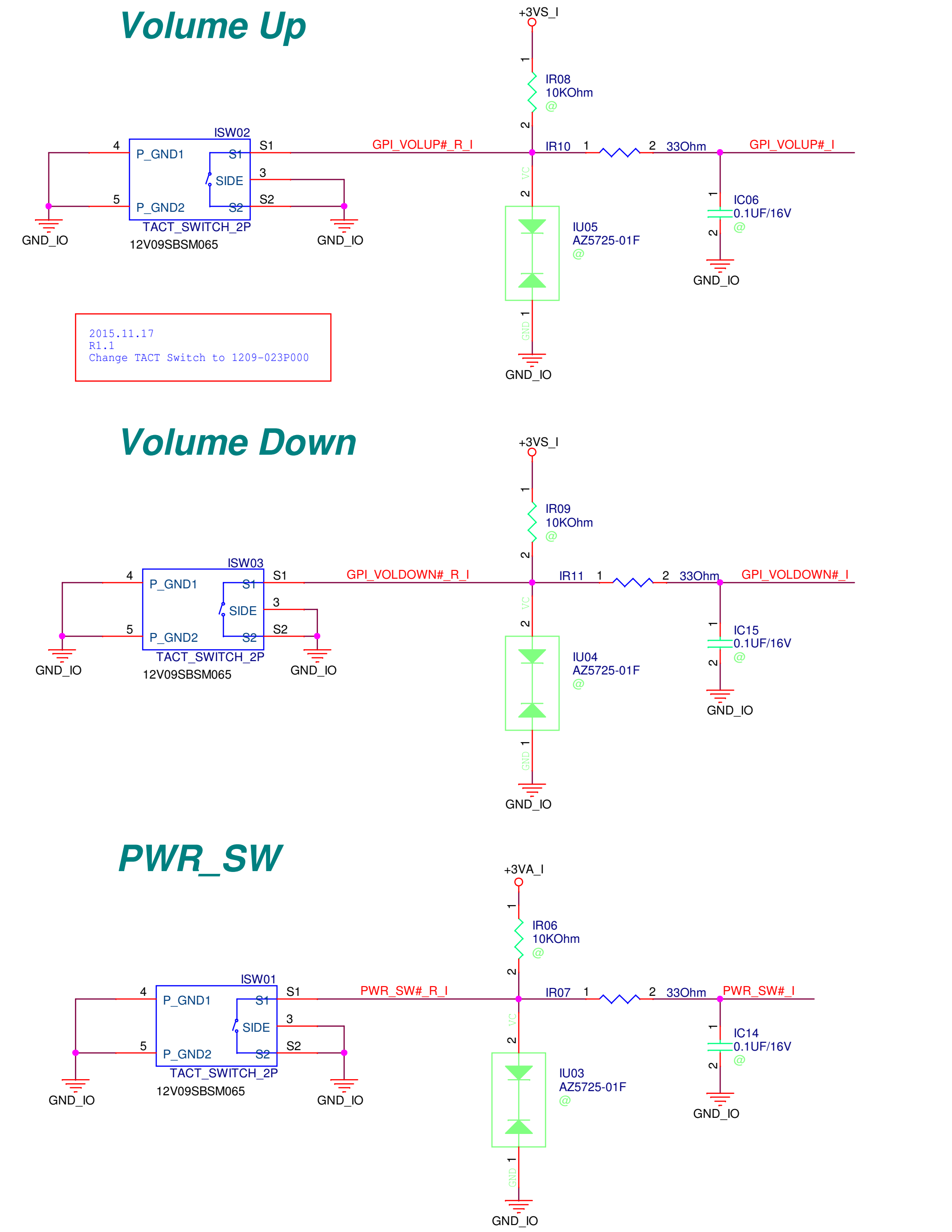
Card Reader



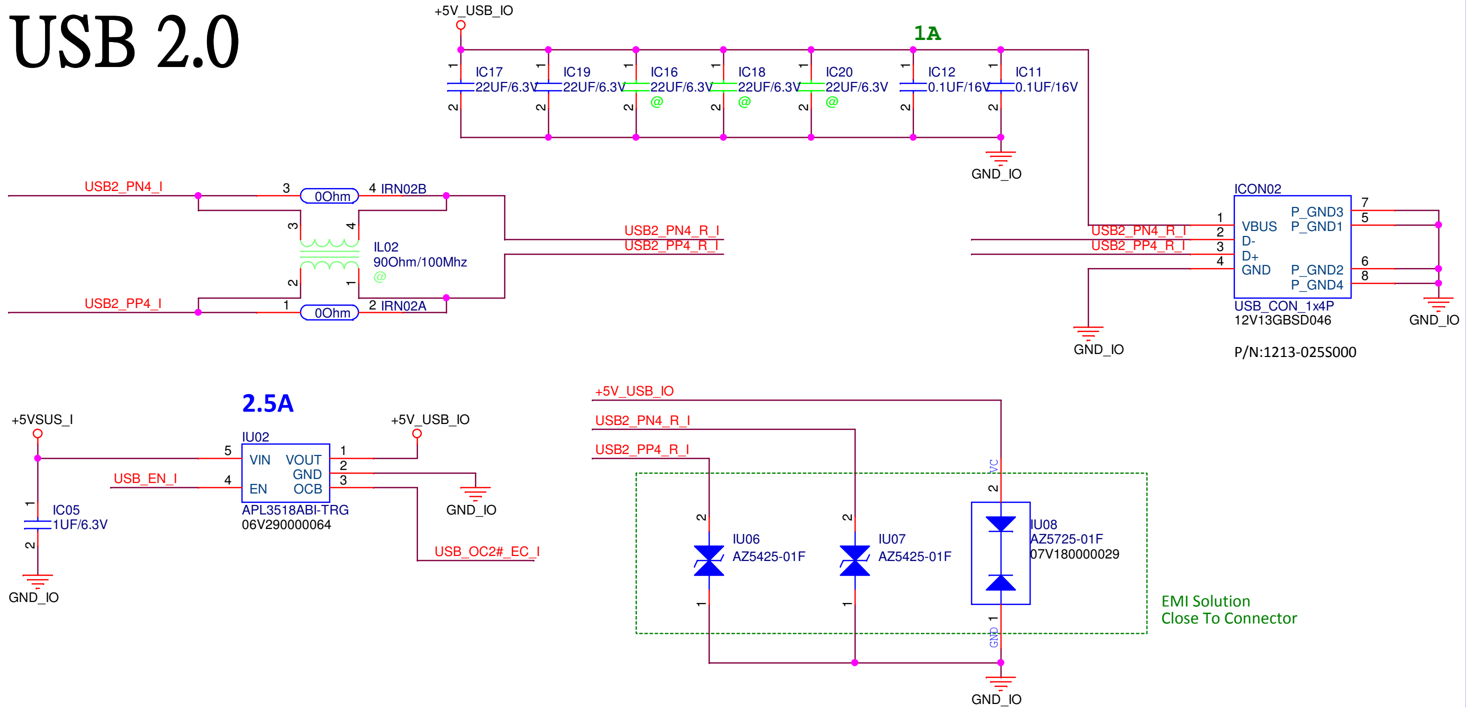
Volume Up

Volume Down

PWR_SW



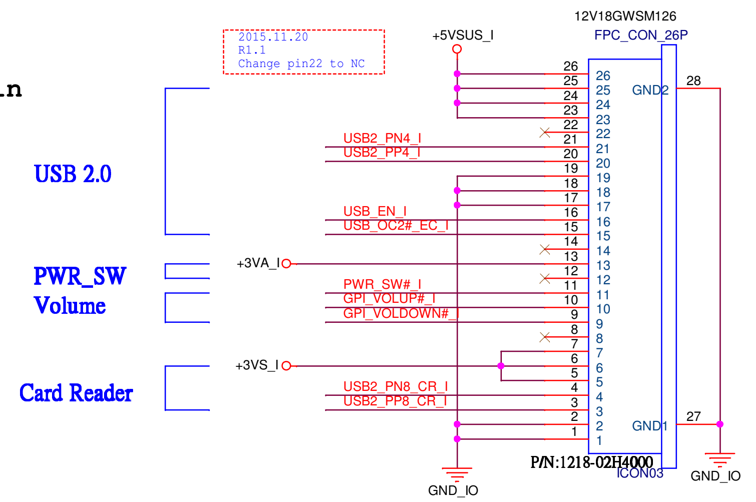
USB 2.0

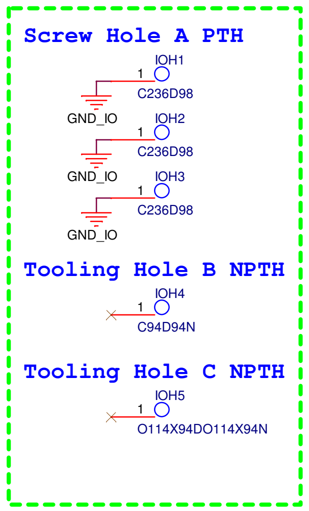


Connector

IO Connector Pin Define

R15	
26	+5VSUS
25	+5VSUS
24	+5VSUS
23	+5VSUS
22	NC
21	USB_PN4_20_R
20	USB_PP4_20_R
19	GND
18	GND
17	GND
16	USBP01_EN
15	USB_OC2#_PCH
14	NC
13	+3VA
12	NC
11	PWR_SW#
10	VOL_UP#
9	VOL_DOWN#
8	NC
7	+3VS
6	+3VS
5	+3VS
4	USB_PN8_CR
3	USB_PP8_CR
2	GND
1	GND





PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : IO Board

Engineer: Leo_Zhang

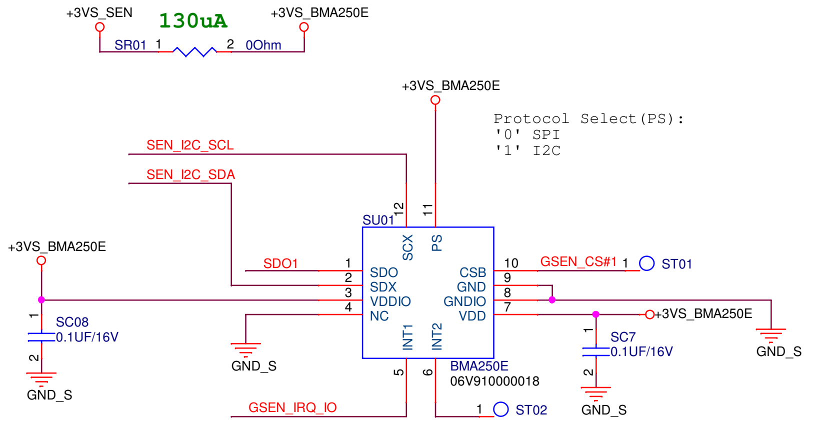
BG1/HW4

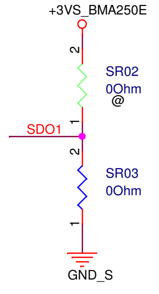
Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 66 of 110

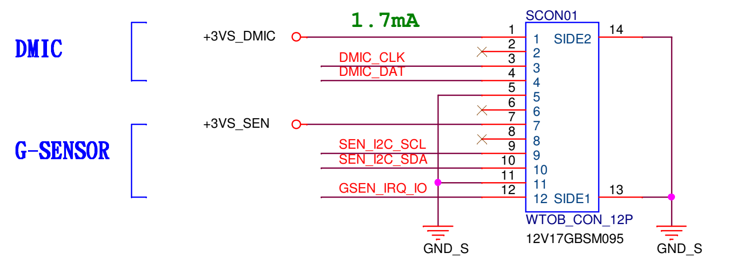
Sensor Board

G-Sensor

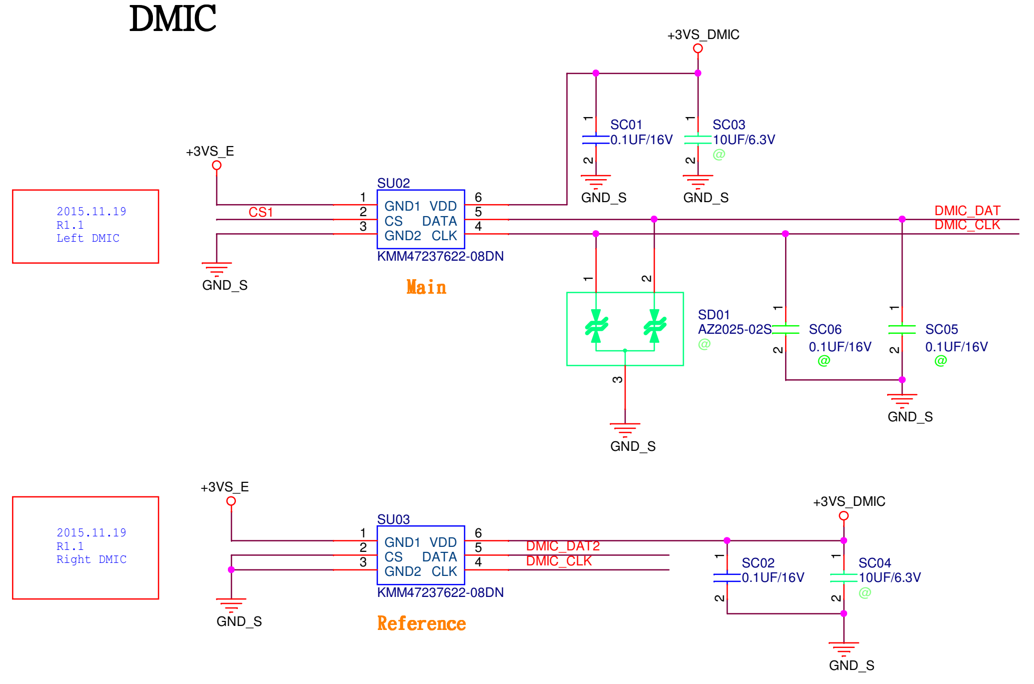


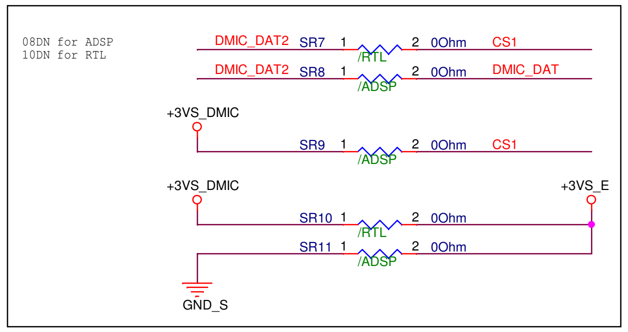


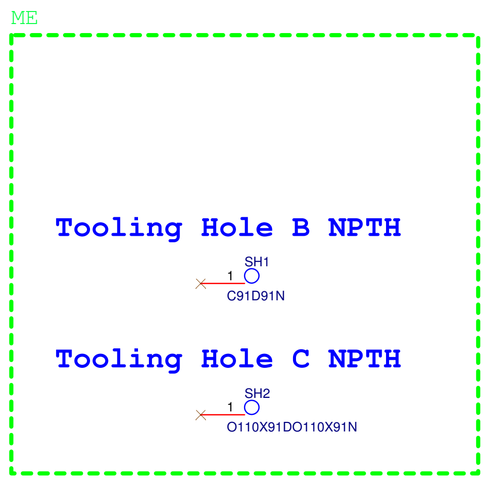
SU01.1 Pull Up	Slave Address(7-bits): 0x19 (W: 0x32, R: 0x33)
SU01.1 Pull Down V	Slave Address(7-bits): 0x18 (W: 0x30, R: 0x31)



DMIC



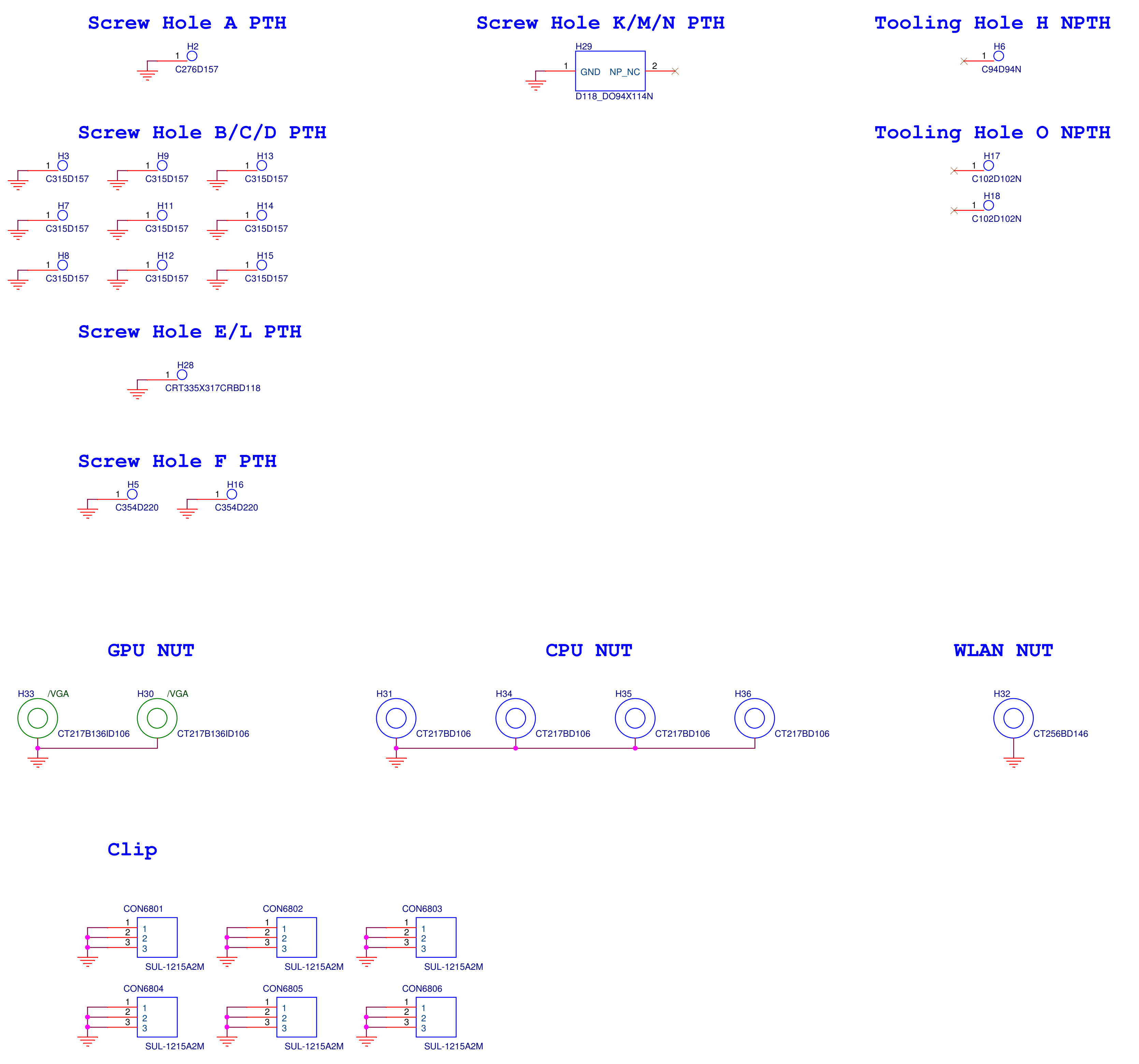




PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1/HW4

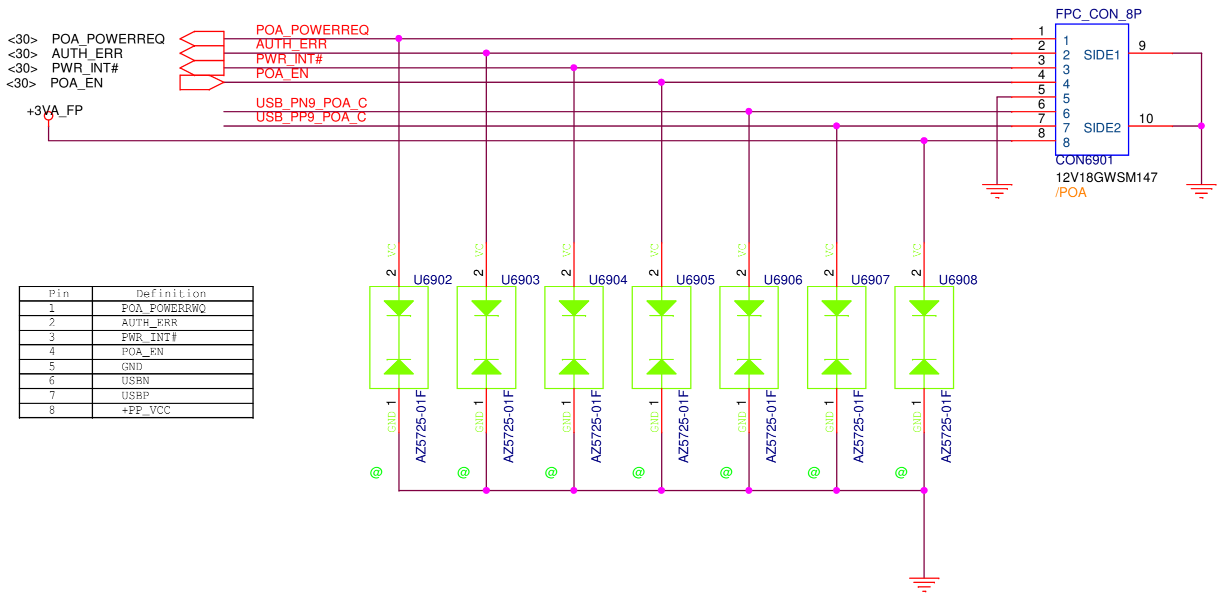
Title : Sensor Board		
Engineer: Leo_Zhang		
Size C	Project Name P5HCJ_KBL	Rev 1.2
Date: Monday, June 20, 2016	Sheet 67 of 110	

ME Hole

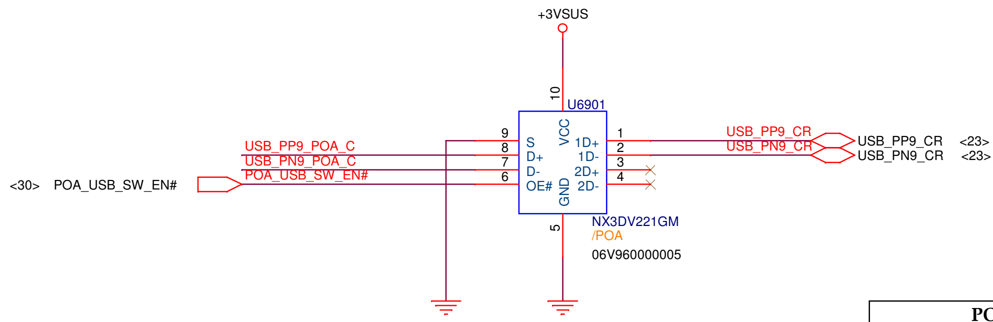


PEGATRON	Title : ME Hole		
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<OrgName>	Engineer: Leo_Zhang		
Size C	Project Name P5HCJ_KBL		Rev 1.2
Date: Monday, June 20, 2016	Sheet 68 of 96		

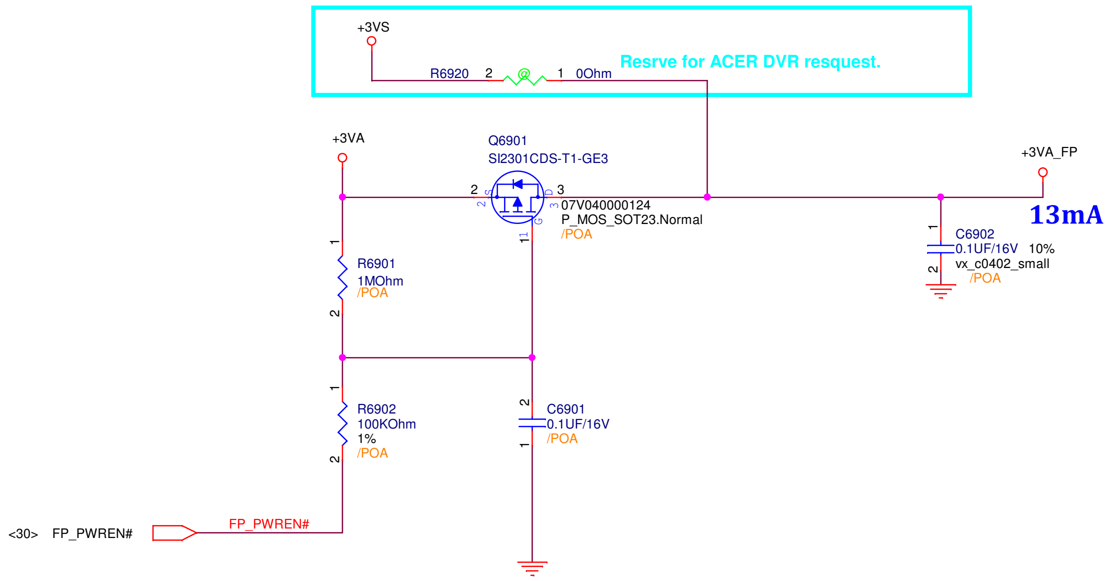
Finger printer



Pin	Definition
1	POA_POWERRWQ
2	AUTH_ERR
3	PWR_INT#
4	POA_EN
5	GND
6	USBN
7	USBP
8	+PP_VCC

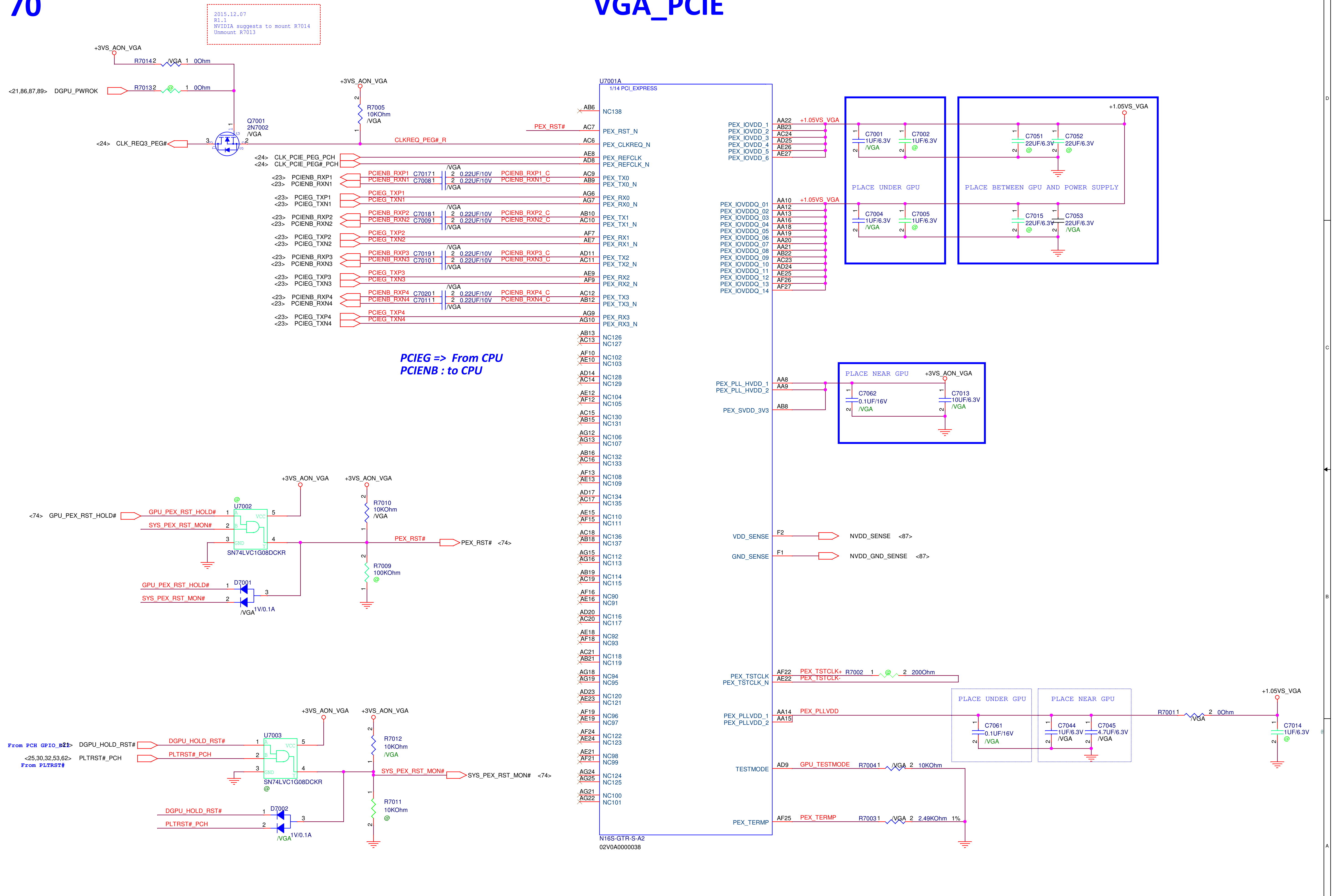


POA USB Switch		
Input		Channel
S	/OE	
L	L	Output = input 1
X	H	Switches off



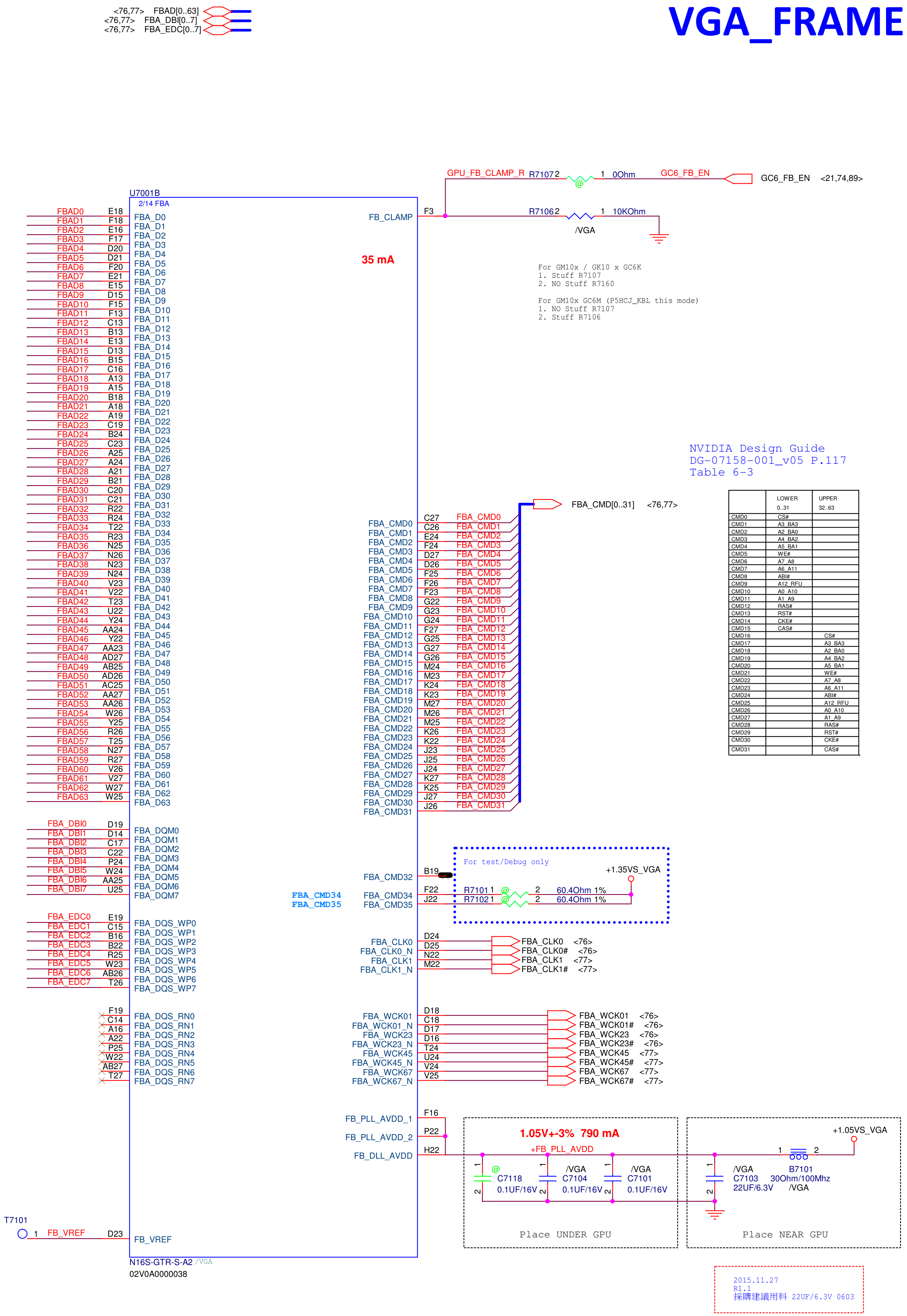
70

VGA_PCIE



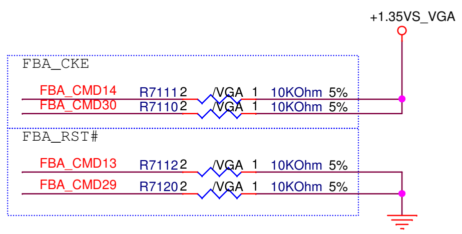
2015.12.07
R1.1
NVIDIA suggests to mount R7014
Unmount R7013
U7001A
1/14 PCI_EXPRESS
N16S-GTR-S-A2
02V0A0000038
PCIEG => From CPU
PCIENB : to CPU
PLACE UNDER GPU
PLACE BETWEEN GPU AND POWER SUPPLY
PLACE NEAR GPU
+1.05VS_VGA
+3VS_AON_VGA
Q7001
2N7002
U7002
SN74LVC1G08DCKR
U7003
SN74LVC1G08DCKR
D7001
D7002
PEX_RST#
CLKREQ_PEG#_R
DGPU_PWROK
CLK_REQ3_PEG#
CLK_PCIE_PEG_PCH
CLK_PCIE_PEG#_PCH
GPU_PEX_RST_HOLD#
SYS_PEX_RST_MON#
DGPU_HOLD_RST#
PLTRST#_PCH
From PCH GPIO_B22
From PLTRST#
VDD_SENSE
GND_SENSE
NVDD_SENSE
NVDD_GND_SENSE
PEX_TSTCLK
PEX_TSTCLK_N
PEX_PLLVDD
TESTMODE
PEX_TERMP

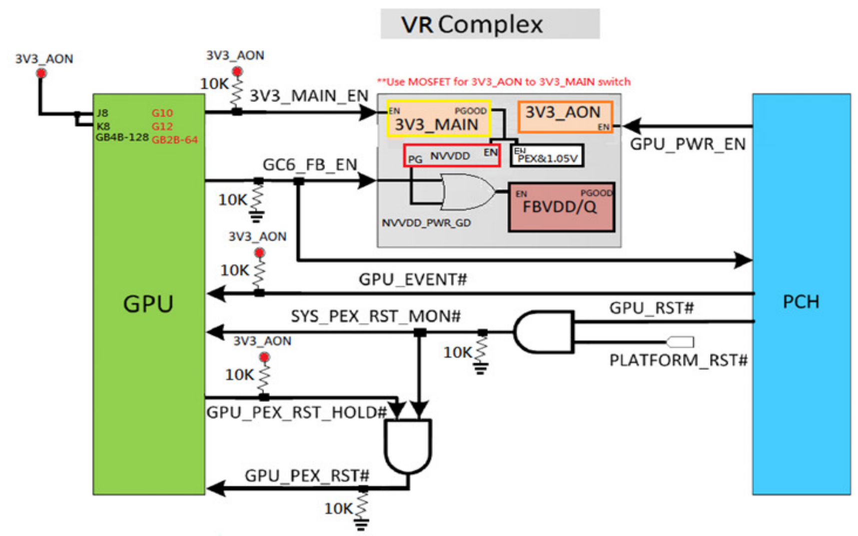
VGA_FRAME BUFFER



NVIDIA Design Guide
DG-07158-001_v05 P.117
Table 6-3

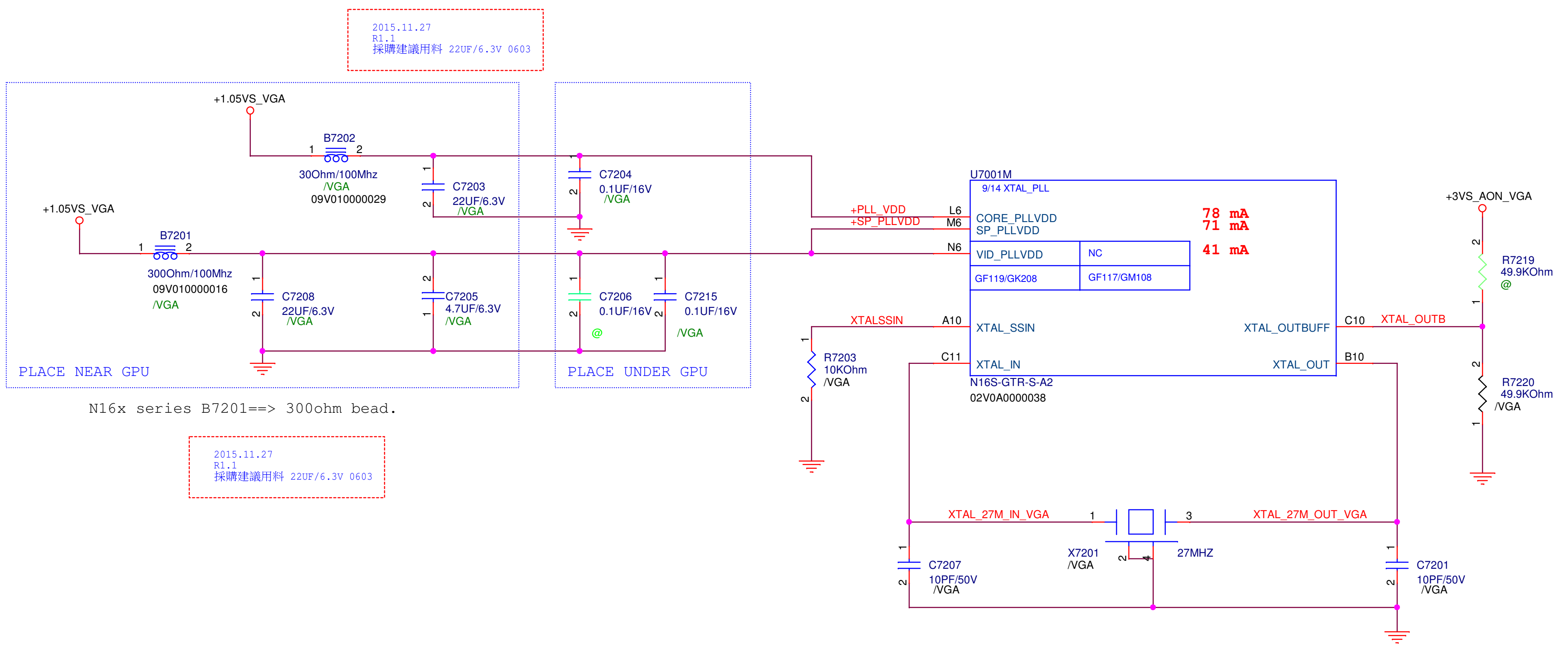
	LOWER 0..31	UPPER 32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#





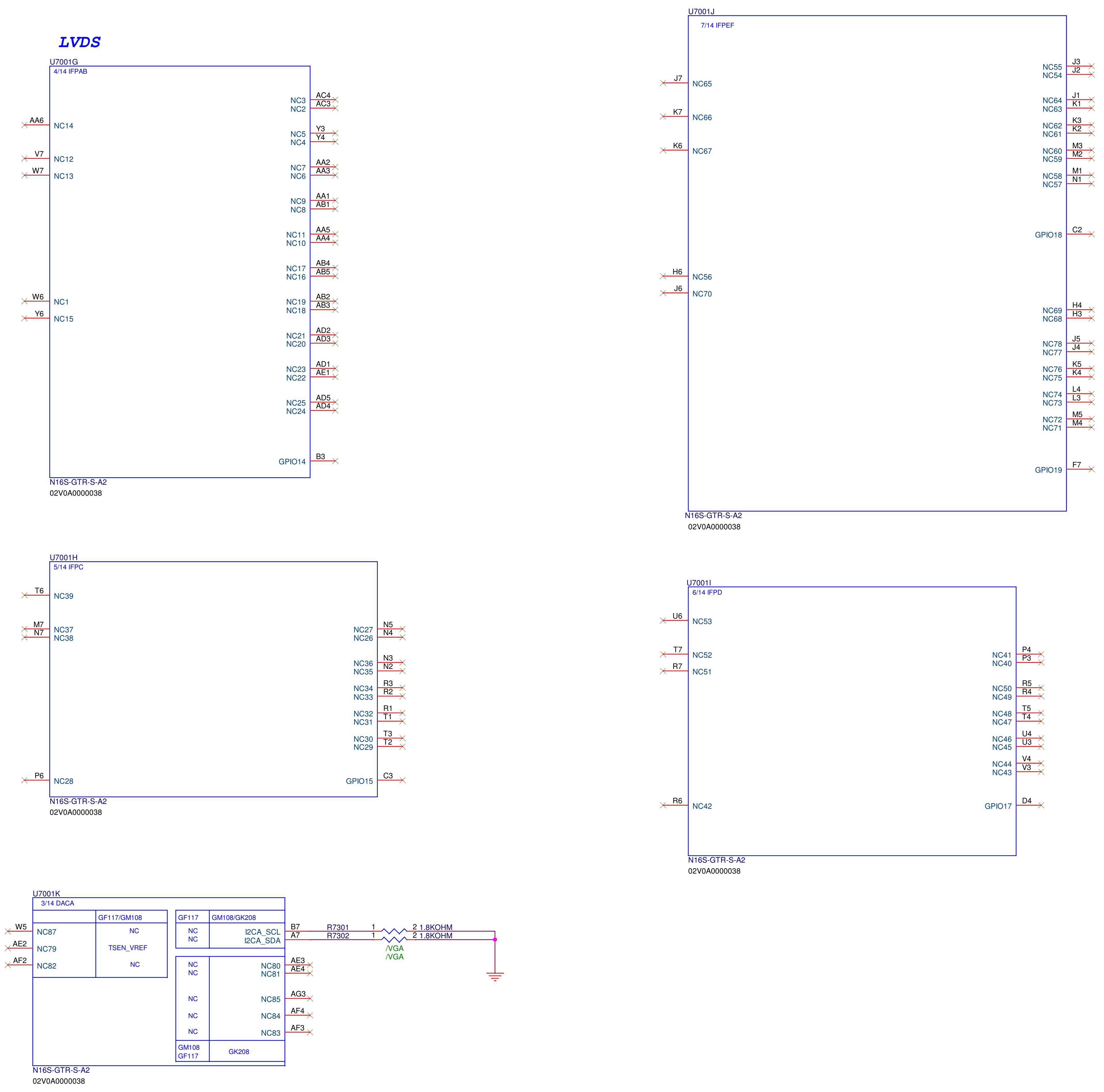
GC6 2.0 High-level Signal Connections

VGA_XTAL



2015.11.27
R1.1
採購建議用料 22UF/6.3V 0603
+1.05VS_VGA
B7202
30Ohm/100Mhz
/VGA
09V010000029
C7203
22UF/6.3V
/VGA
C7204
0.1UF/16V
/VGA
+1.05VS_VGA
B7201
300Ohm/100Mhz
09V010000016
/VGA
C7208
22UF/6.3V
/VGA
C7205
4.7UF/6.3V
/VGA
C7206
0.1UF/16V
@
C7215
0.1UF/16V
/VGA
PLACE NEAR GPU
PLACE UNDER GPU
N16x series B7201==> 300ohm bead.
2015.11.27
R1.1
採購建議用料 22UF/6.3V 0603
+PLL_VDD
+SP_PLLVDD
L6
M6
N6
U7001M
9/14 XTAL_PLL
CORE_PLLVDD
SP_PLLVDD
VID_PLLVDD
NC
GF119/GK208
GF117/GM108
78 mA
71 mA
41 mA
XTALSSIN
A10
XTAL_SSIN
C11
XTAL_IN
XTAL_OUTBUFF
XTAL_OUT
C10
B10
XTAL_OUTB
N16S-GTR-S-A2
02V0A0000038
R7203
10KOhm
/VGA
+3VS_AON_VGA
R7219
49.9KOhm
@
R7220
49.9KOhm
/VGA
XTAL_27M_IN_VGA
XTAL_27M_OUT_VGA
X7201
/VGA
27MHZ
C7207
10PF/50V
/VGA
C7201
10PF/50V
/VGA

VGA_DISPLAY



PEGATRON **Title :** VGA_DISPLAY

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-NB4

Engineer: *Leo_Zhang*

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

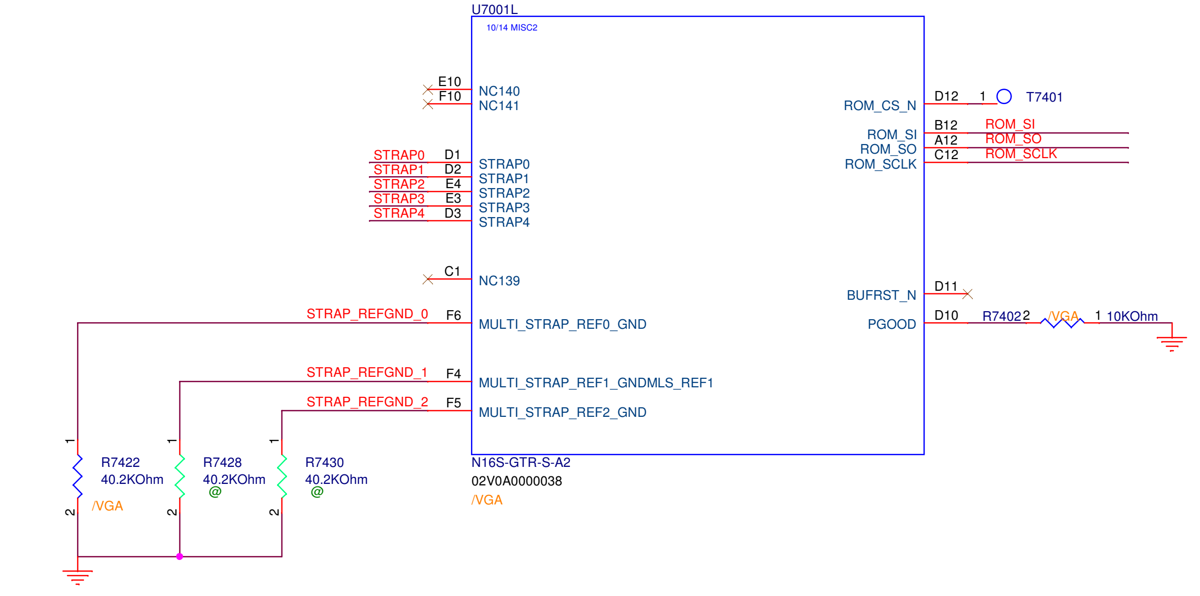
Date: Monday, June 20, 2016 Sheet 73 of 96

VGA_GPIO_STRAP

GPU DEVICE ID

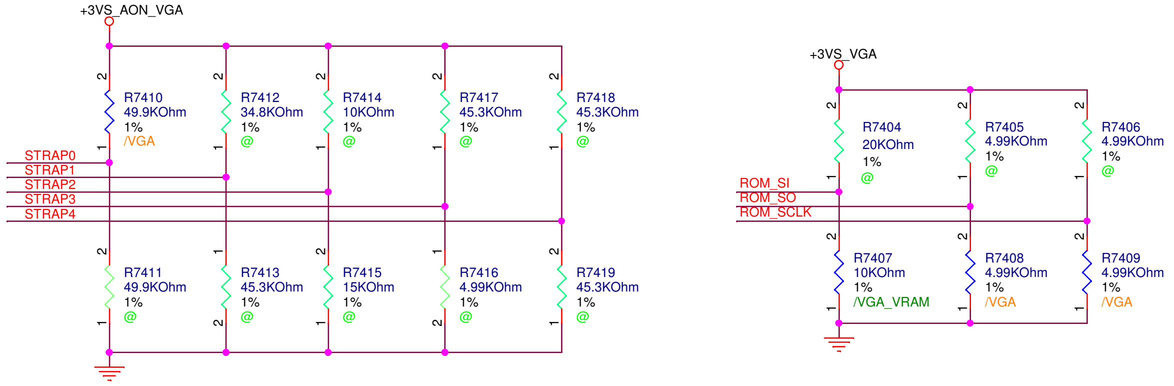
N16V-GM	N16S-GTR
	0x134D

N16S-GT-R	Strap Resistance Mapping to Hex Values	
Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111



For GB2B-64, GB4B-128, GB3B-256 Muti-Level modeStrapping (From DG-07158-001_v05 Table.15-3)

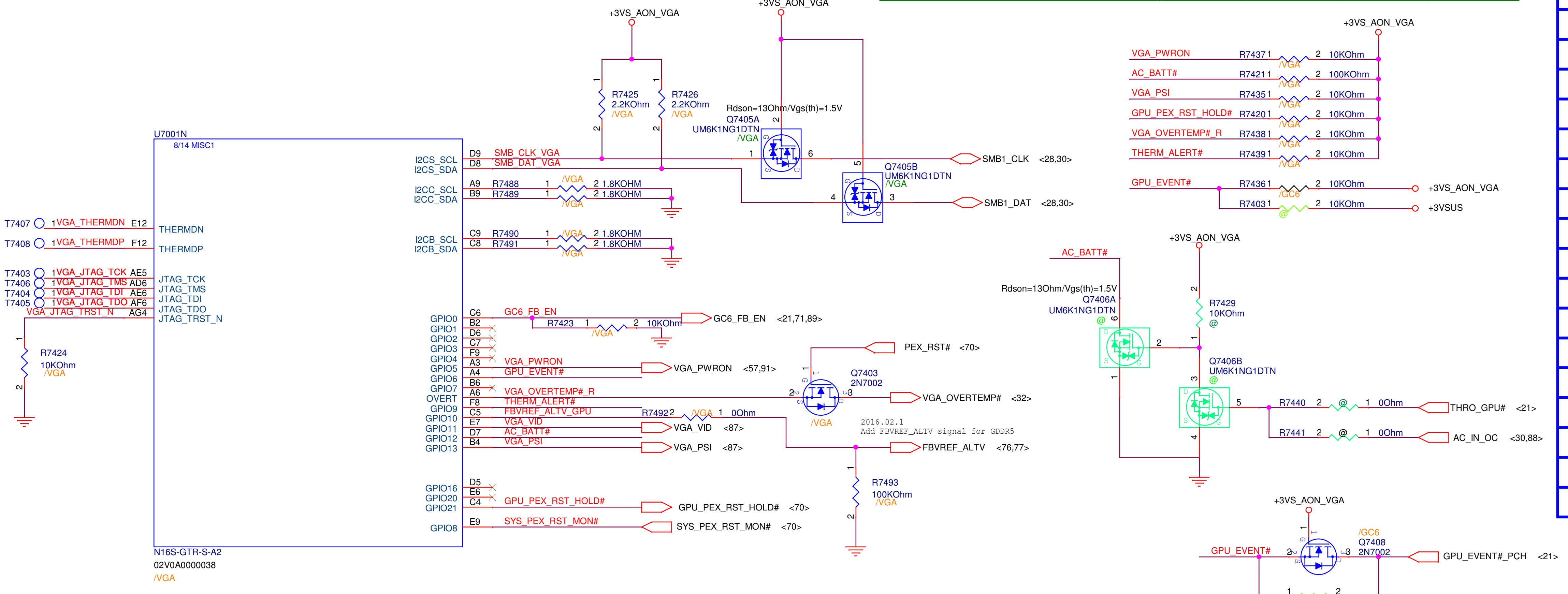
N16S-GTR	Multi-Level Mode Strapping			
Resistor Values	Bit3	Bit2	Bit1	Bit0
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kohm pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE



From RVL-07229-001_v14 Table.18

B build GB2B-64(N16V-GM/N16S-GTR)	Samsung(4G)	Hynix(4G)	Samsung(8G)	Micron(8G)
DEVICE ID	0x3	0x6	0x0	0x1
STRAP0	49.9K PU	49.9K PU	49.9K PU	49.9K PU
STRAP1	Reserved	Reserved	Reserved	Reserved
STRAP2	Reserved	Reserved	Reserved	Reserved
STRAP3	Reserved	Reserved	Reserved	Reserved
STRAP4	Reserved	Reserved	Reserved	Reserved
ROM_SCLK	4.99K PD	4.99K PD	4.99K PD	4.99K PD
ROM_SI	20K PD	34.8K PD	4.99K PD	10K PD
ROM_SO	4.99K PD	4.99K PD	4.99K PD	4.99K PD

GPIO Definition		
	NV SPEC Standard mode DG_07158_001_V05 Table 12-2	P5HCJ
GPIO0	GC6_FB_EN	FB_CLAMP_MON
GPIO1	MEM_VDD_CTL	NC
GPIO2	LCD_BL_PWM	NC
GPIO3	LCD_VCC	NC
GPIO4	LCD_BLEN	NC
GPIO5	3V3_MAIN_EN	GPIO5_PWM_VID_BOOT_EN
GPIO6	GPU_EVENT#	FB_CLAMP_TGL_REQ#
GPIO7	3DVision	NC
GPIO8	SYS_PEX_RST_MON#	VGA_OVERTEMP#
GPIO9	THERM_ALERT	VGA_THERM_ALERT#
GPIO10	MEM_VREF_CTL	NC
GPIO11	PWM_VID	VGA_VID
GPIO12	PWR_LEVEL	AC_BATT#
GPIO13	PSI	VGA_PSI#
GPIO14	HPD_A	
GPIO15	HPD_C	
GPIO16	FRAME_LOCK#	NC
GPIO17	HPD_D	
GPIO18	HPD_E	
GPIO19	HPD_F or HPD_B	
GPIO20	Reserved	NC
GPIO21	GPU_PEX_RST_HOLD#	NC
OVERT	OVERT	

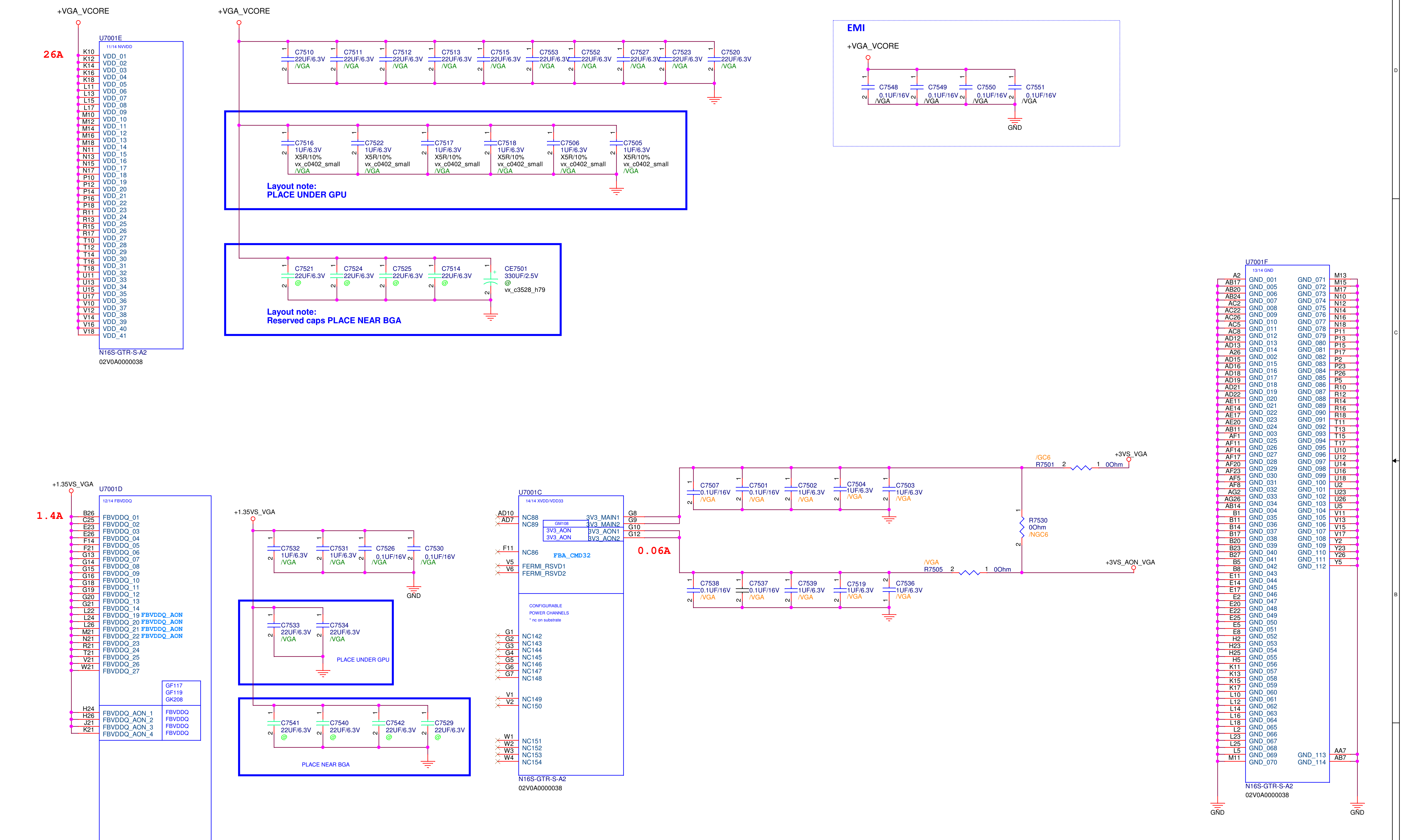


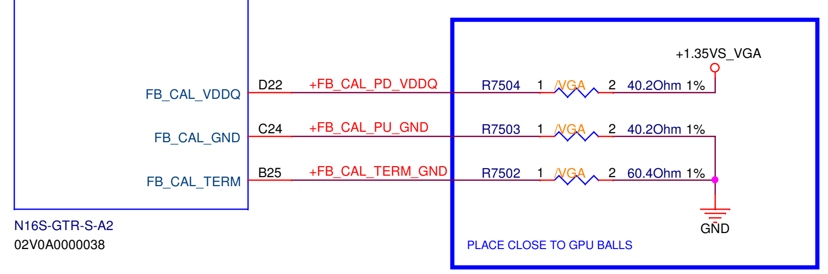
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-NB4
Title : VGA_GPIO,STRAP
Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 74 of 96

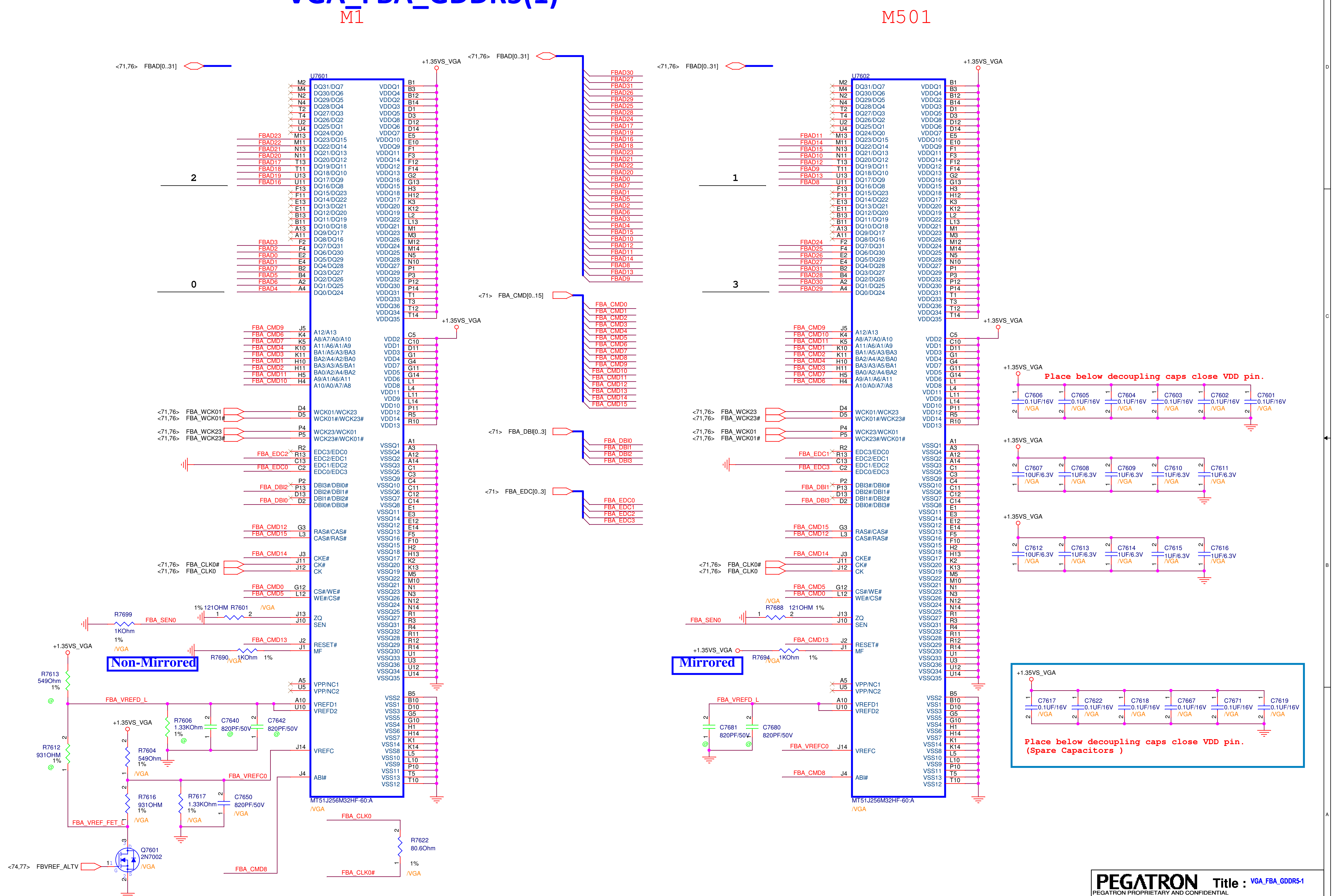
VGA_Power





Function / Feature Reserve	Component mount & un-mount	Verified or not	Note
N16V-GM without GC6 2.0	Mount: R7530 Un-mount: /N16S-GT_GC6	Basic function ok	Power BOM: Un-mount +3VS_VGA load switch schematic
N16S-GT with GC6 2.0	Mount: /N16S-GT_GC6 Un-mount: R7530	Not verify	Power BOM: Mount +3VS_VGA load switch schematic

VGA_FBA_GDDR5(1)



PEGATRON Title : VGA_FBA_GDDR5-1

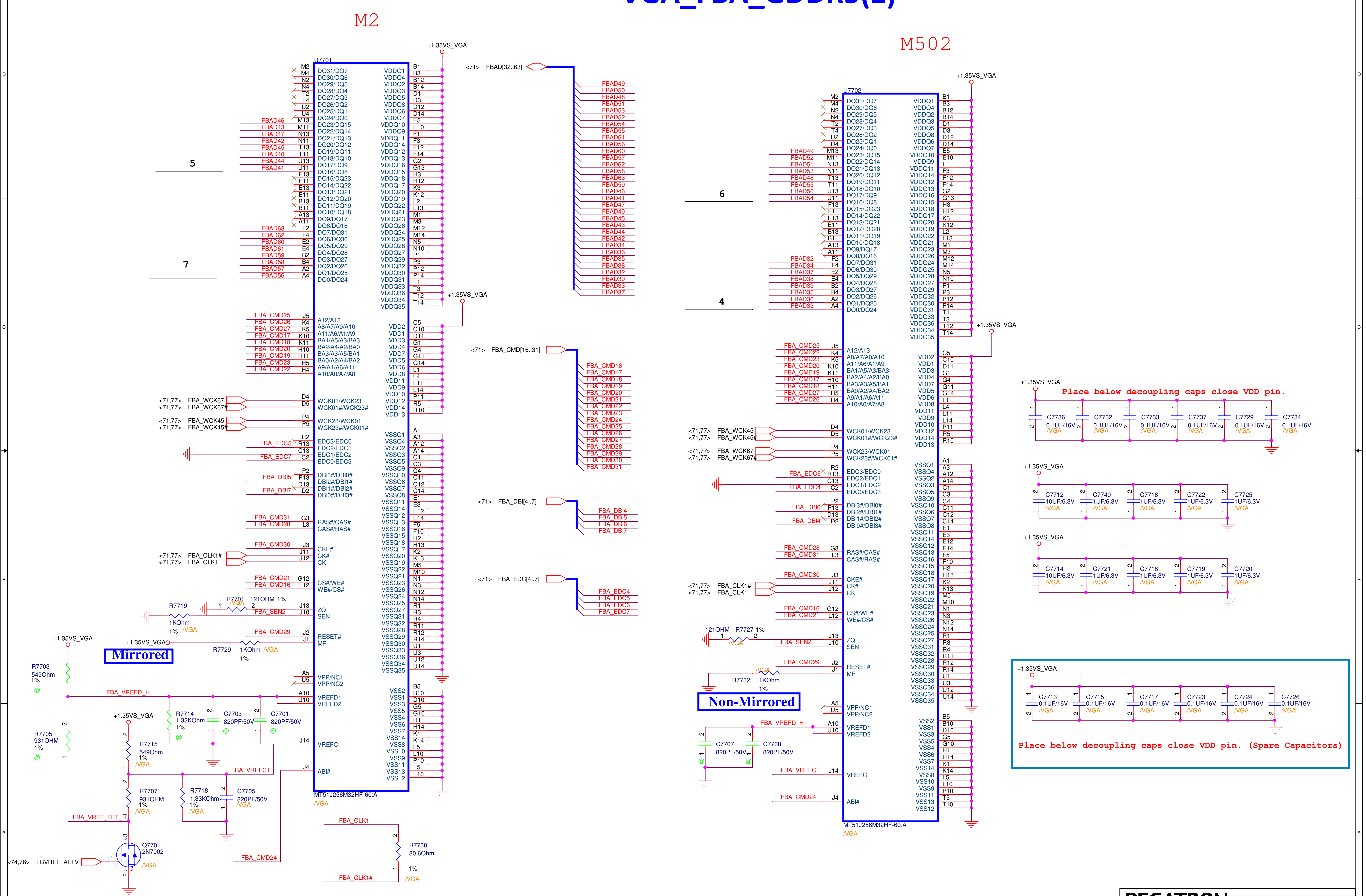
BG1-NB4

Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 76 of 96

VGA_FBA_GDDR5(2)



PEGATRON

Title : VGA_FBA_GDDR5-2

PEGATRON PROPRIETARY AND CONFIDENTIAL

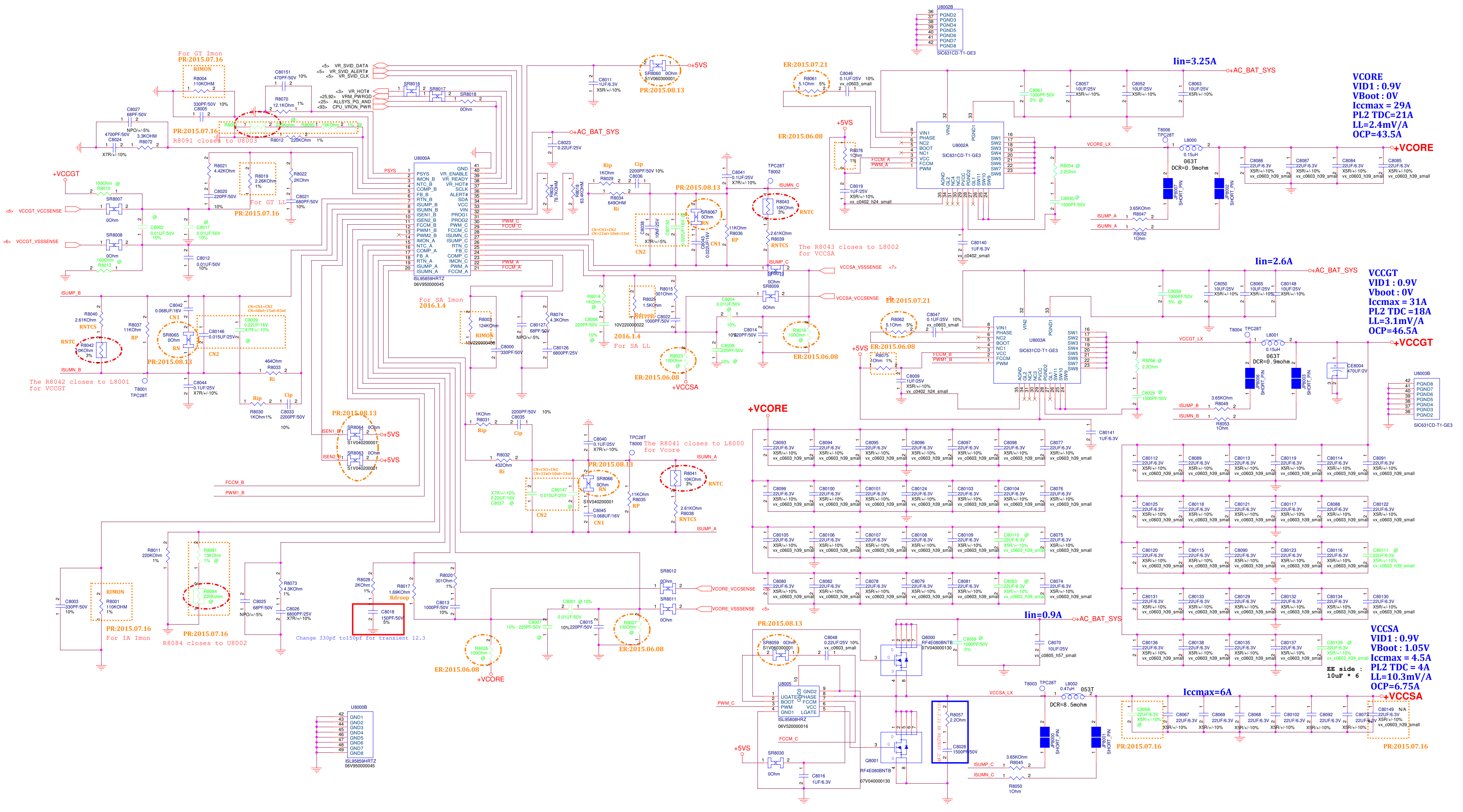
BG1-NB4

Engineer: Leo_Zhang

Size	Project Name	Rev
C	P5HCJ_KBL	1.2

Date: Monday, June 20, 2016 Sheet 77 of 96

Vcore Power Supply



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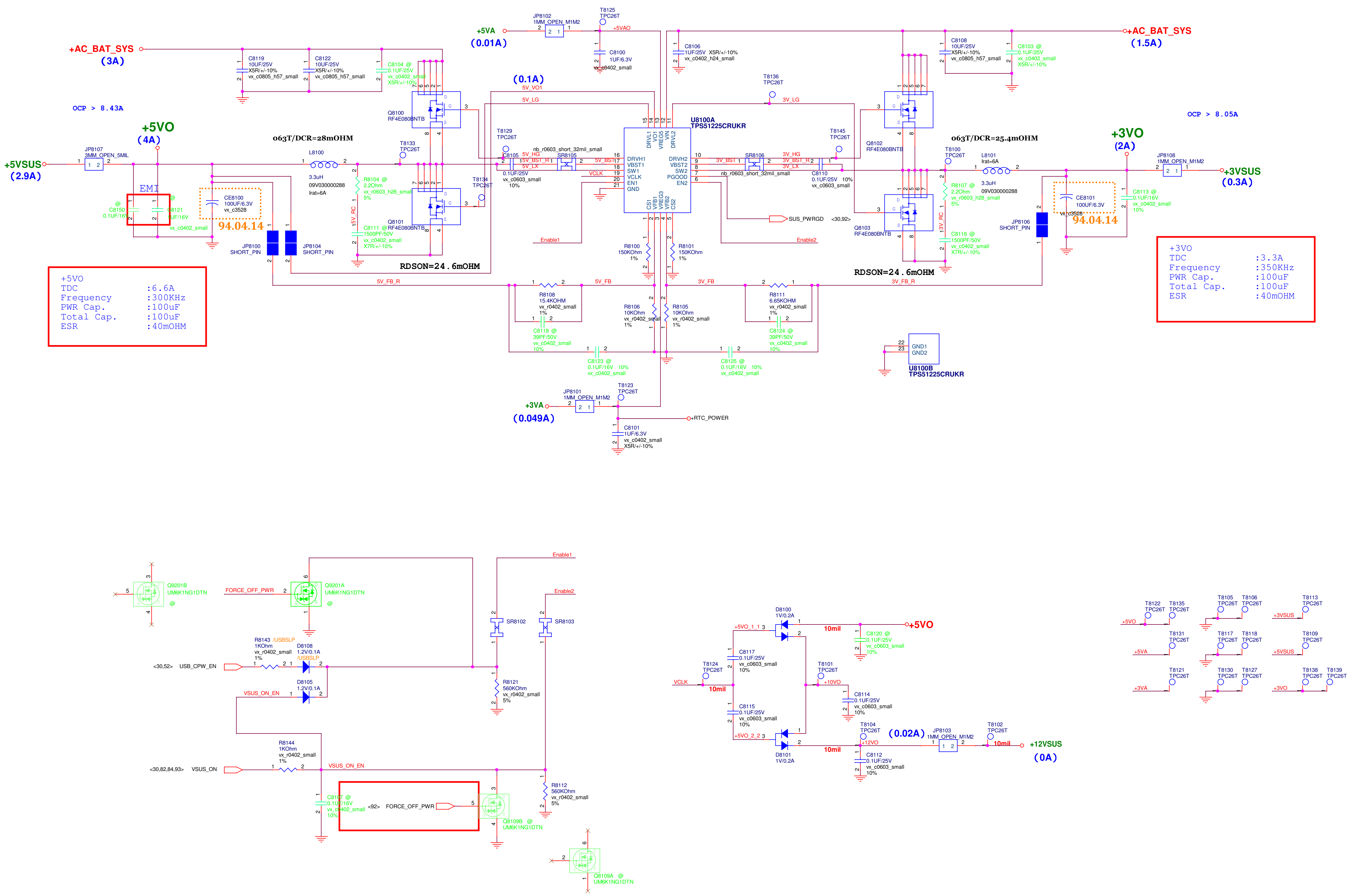
+5VO & +3VO POWER SUPPLY



PEGATRON PEGATRON PROPRIETARY AND CONFIDENTIAL

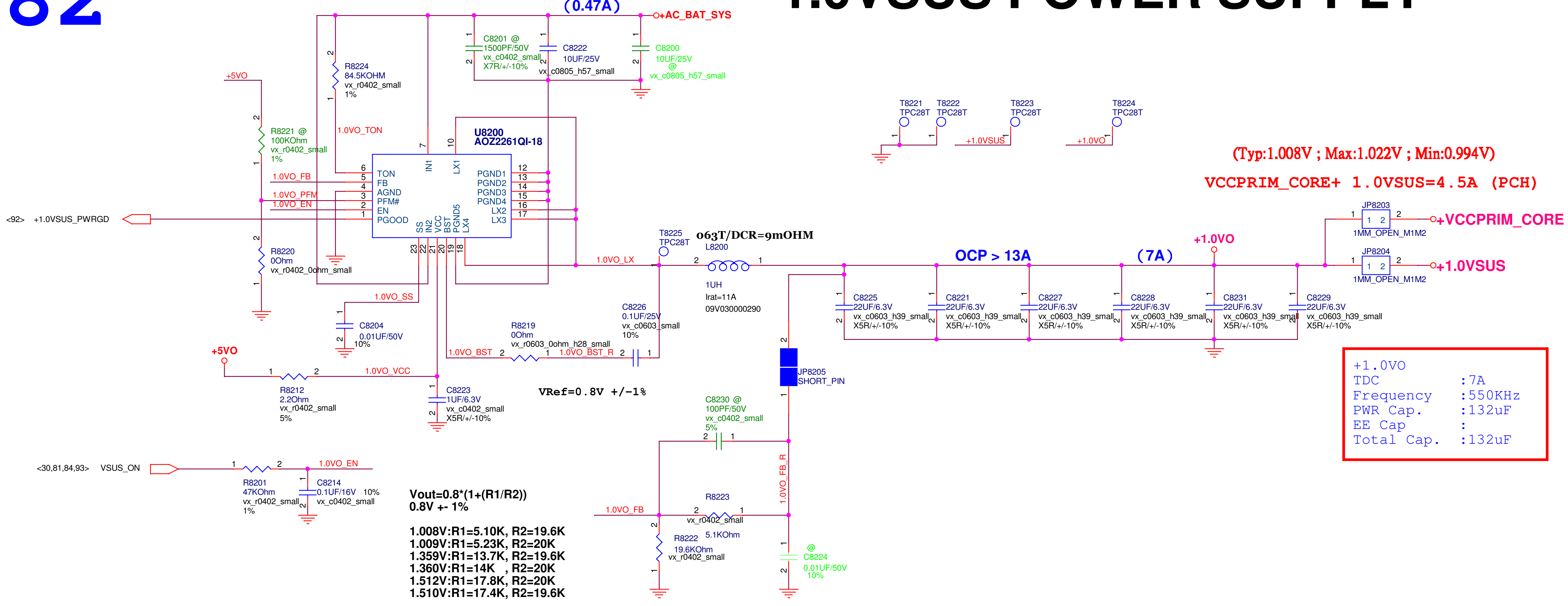
Title : POWER_SYSTEM

Engineer: Benson Lin

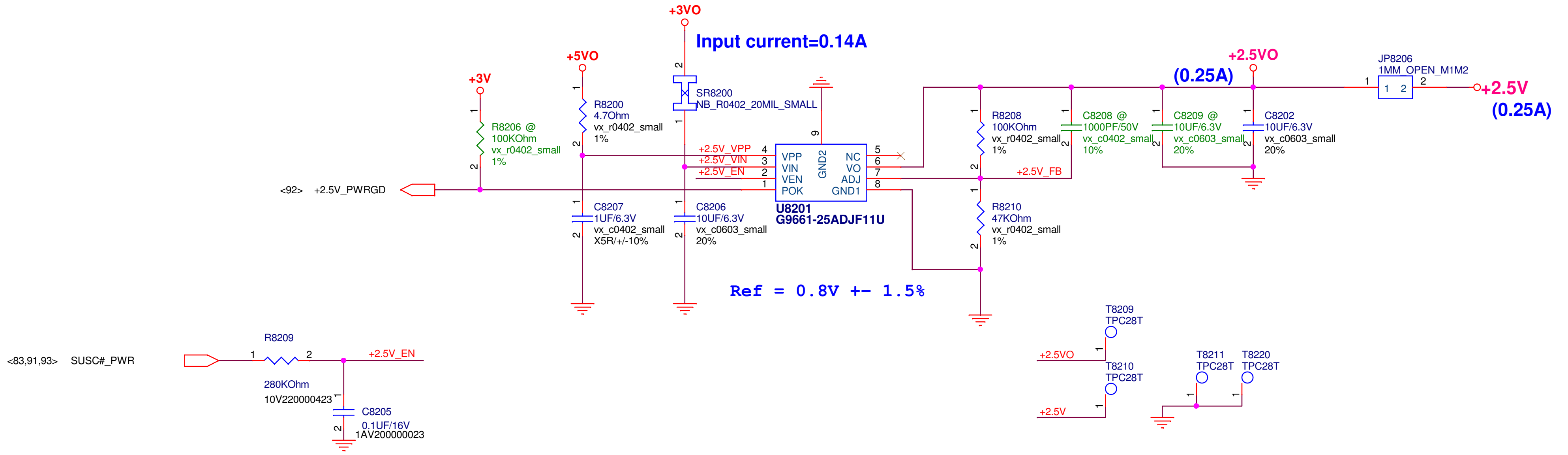
Project Name P5HCJ

Date: Monday, June 20, 2016 Sheet 81 of 94

1.0VSUS POWER SUPPLY



+2.5V POWER SUPPLY



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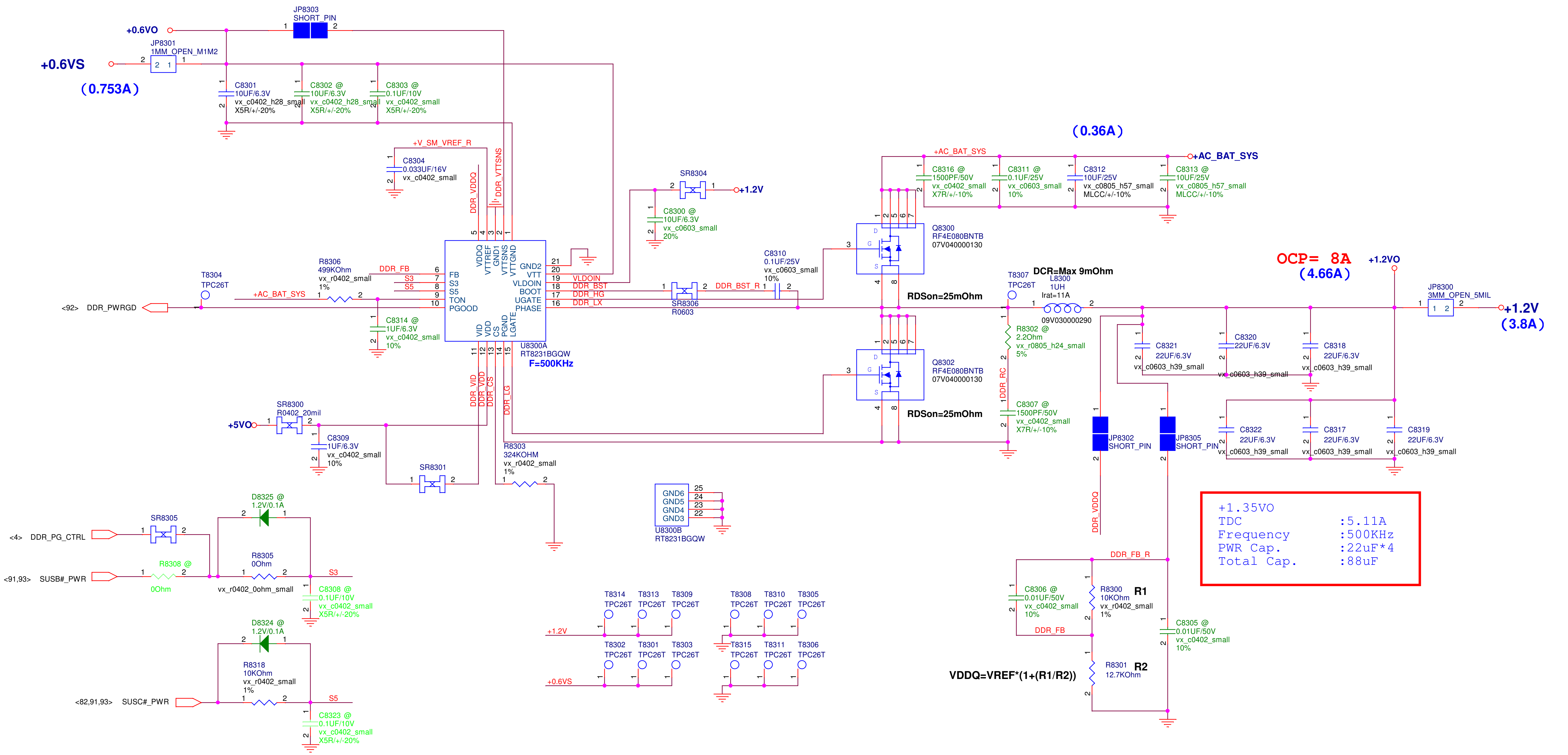
DDR & VTT POWER SUPPLY



VID	Reference Voltage (V)
High	0.675
Low	0.75

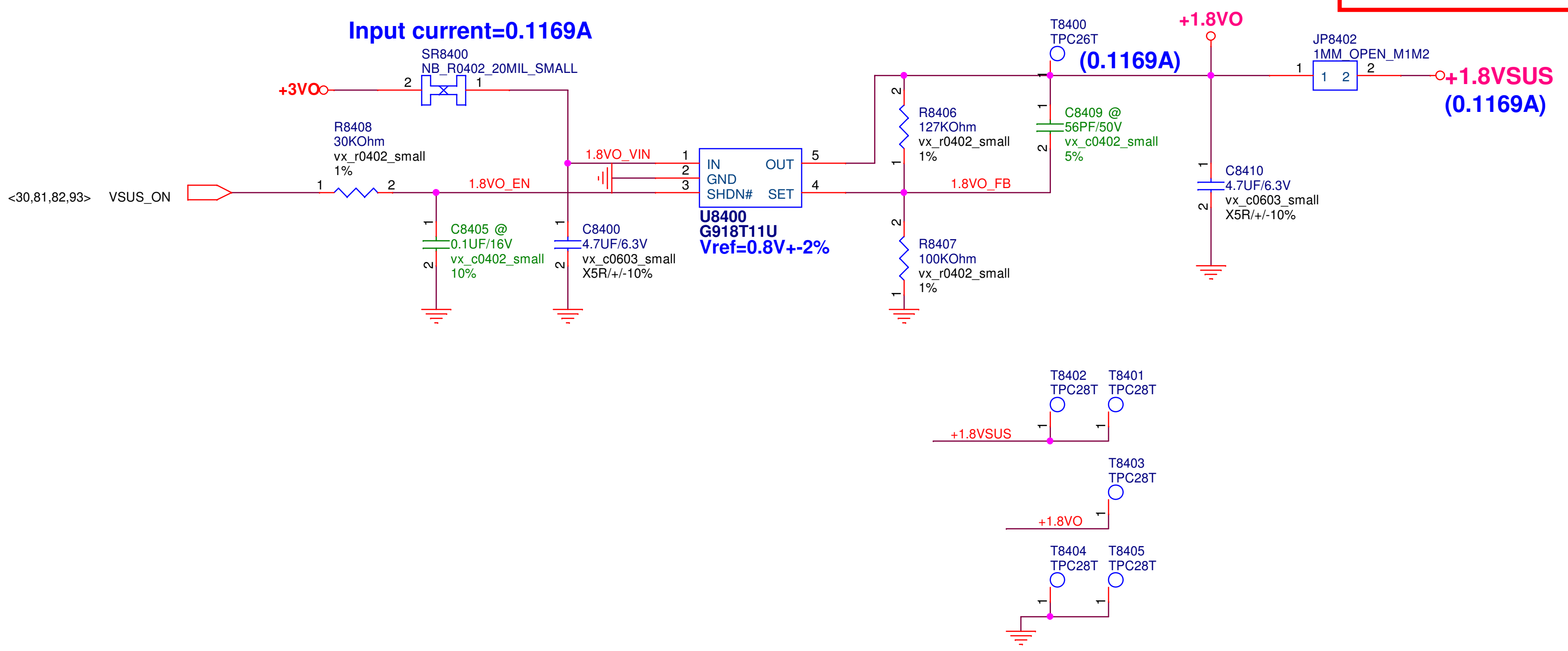
SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	4
DSC	0 ~ 8	2	5

PEGATRON

Title : POWER_DDR & VTT
Engineer: Benson Lin
BG1-POWER
Size: Custom | Project Name: P5HCJ | Rev: 2.0
Date: Monday, June 20, 2016 | Sheet 83 of 94

1.8VSUS POWER SUPPLY

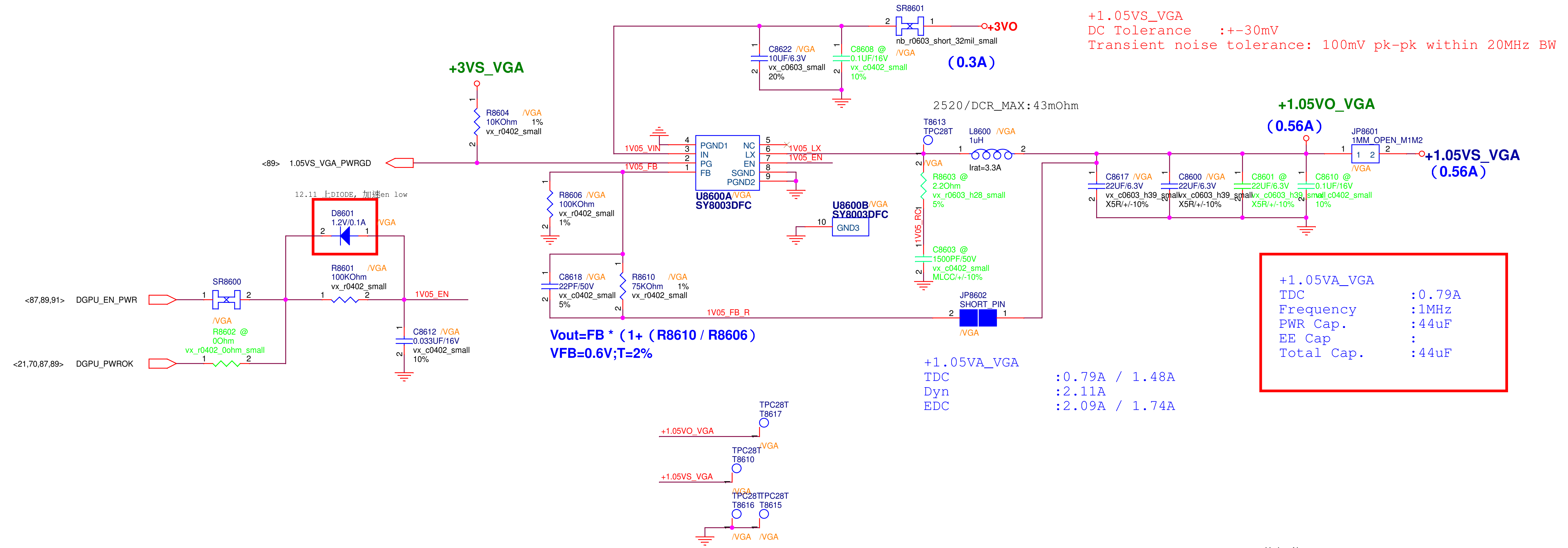
+1.8VO
MAX current :0.1169A
PWR Cap. :20uF
Total Cap. :20uF



<Variant Name>

PEGATRON	Title : PAGE 84 POWER 1	
PEGATRON PROPRIETARY AND CONFIDENTIAL	Engineer: Neil_Lin	
Size: Custom	Project Name: P5HCJ	Rev: 1.0
Date: Monday, June 20, 2016	Sheet 84 of 96	

+1.05VS_VGA POWER SUPPLY



VGA_CORE POWER SUPPLY

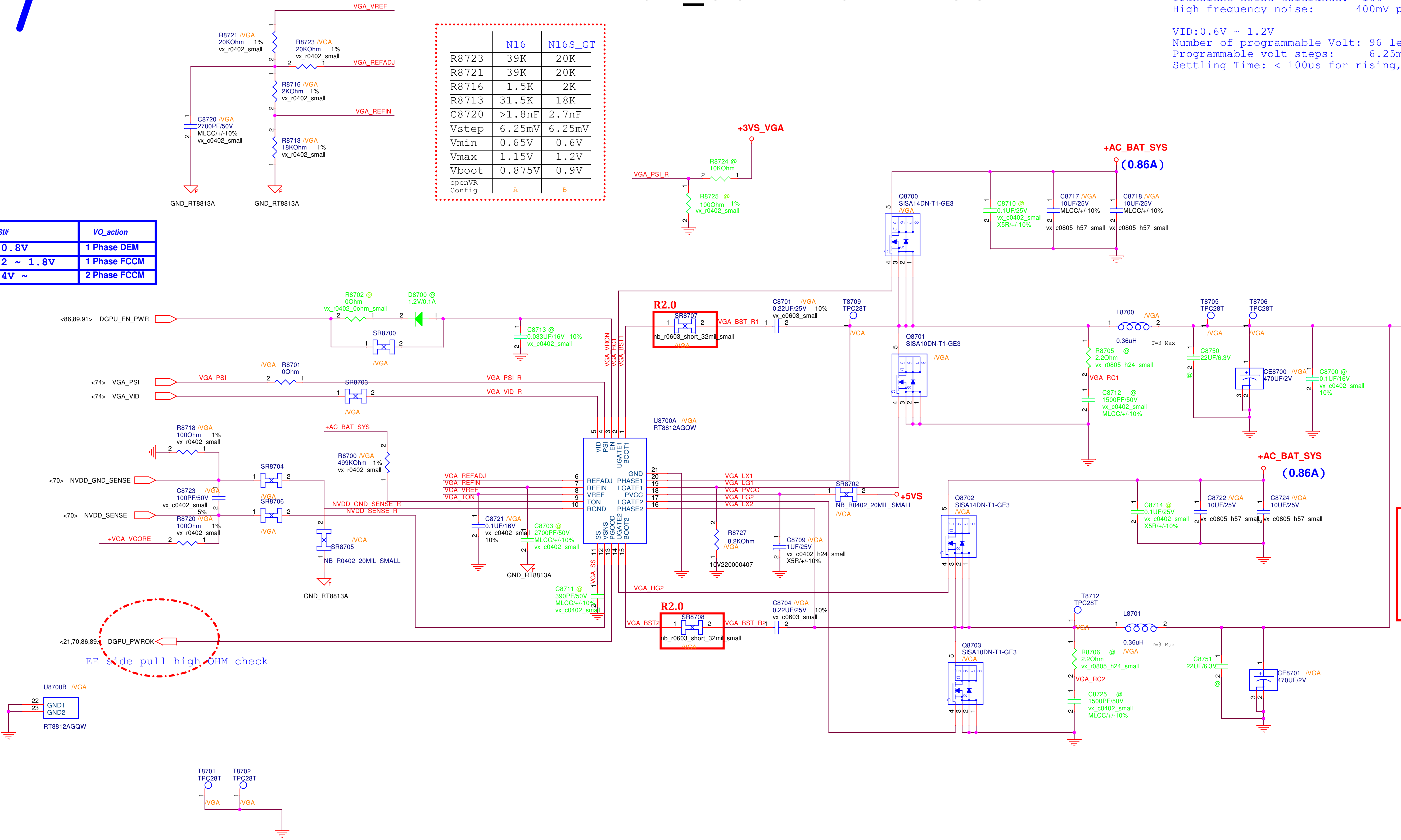
+VGA_VCORE(Package type:N16VS-GT)
DC Tolerance :+-20mV

Overshoot/undershoot
Transient noise tolerance: -10% ~ +20% within 20MHz BW
High frequency noise: 400mV pk-pk within 1GHz BW

VID:0.6V ~ 1.2V
Number of programmable Volt: 96 levels
Programmable volt steps: 6.25mV
Settling Time: < 100us for rising, no restriction on falling

	N16	N16S_GT
R8723	39K	20K
R8721	39K	20K
R8716	1.5K	2K
R8713	31.5K	18K
C8720	>1.8nF	2.7nF
Vstep	6.25mV	6.25mV
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.875V	0.9V
openVR Config	A	B

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM



2 PHASE 25W
N16S-GT
EDP=51A
TDC=26A
DYN= A
OCP:62A

+VGA_VCORE (2 Phase)	
TDC	:30A
Frequency	:305KHz
PWR Cap.	:940uF
EE Cap.	:139.5uF
Total Cap.	:1079.5uF
ESR	:3mOHM

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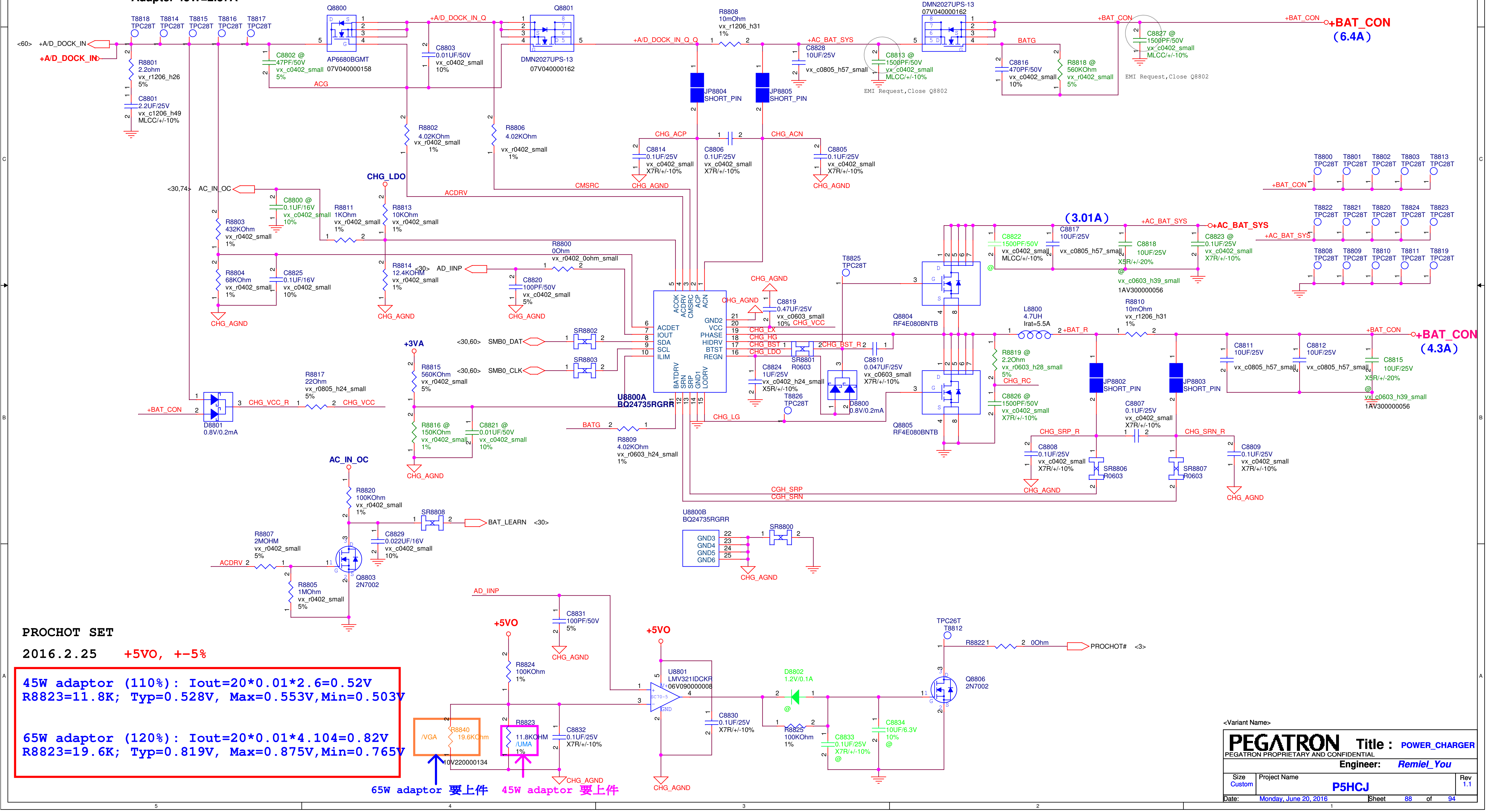
BATTERY CHARGER

Adapter 65W=3.42A
Adapter 45W=2.37A



PROCHOT SET

2016.2.25 +5VO, +-5%

45W adaptor (110%): Iout=20*0.01*2.6=0.52V
R8823=11.8K; Typ=0.528V, Max=0.553V,Min=0.503V

65W adaptor (120%): Iout=20*0.01*4.104=0.82V
R8823=19.6K; Typ=0.819V, Max=0.875V,Min=0.765V

<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: Remiel_You

Size	Project Name	Rev
Custom	P5HCJ	1.1

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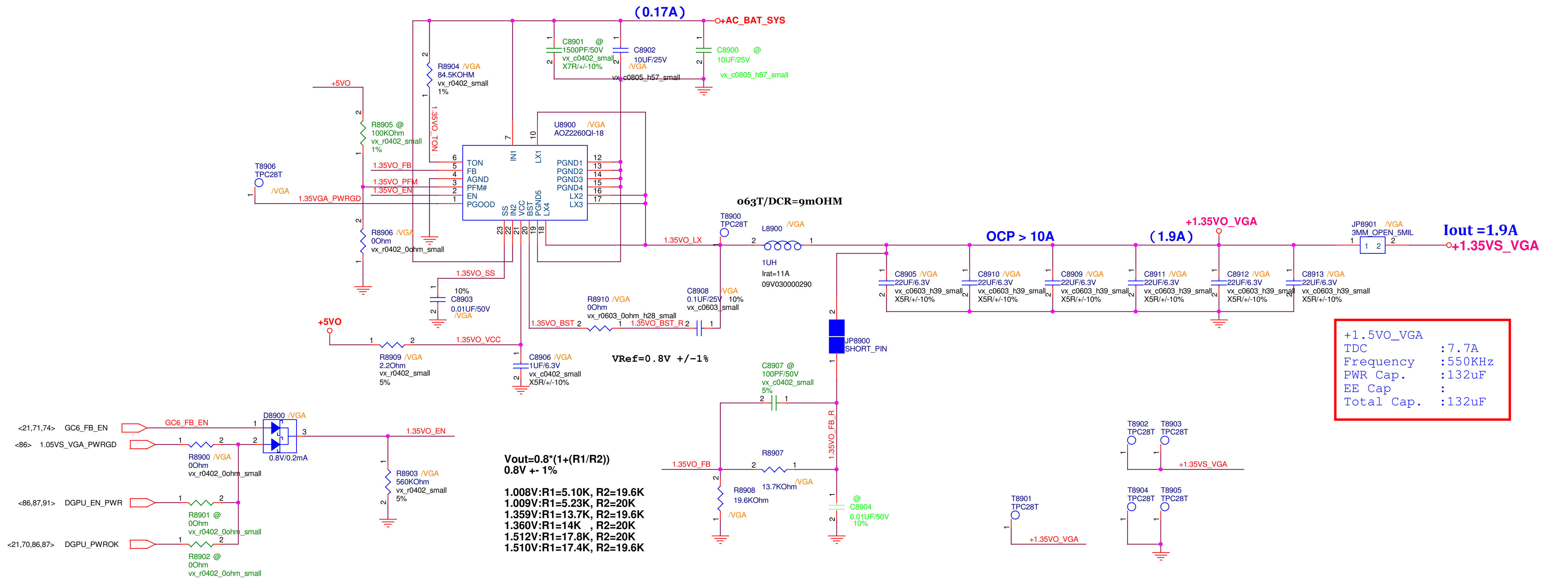
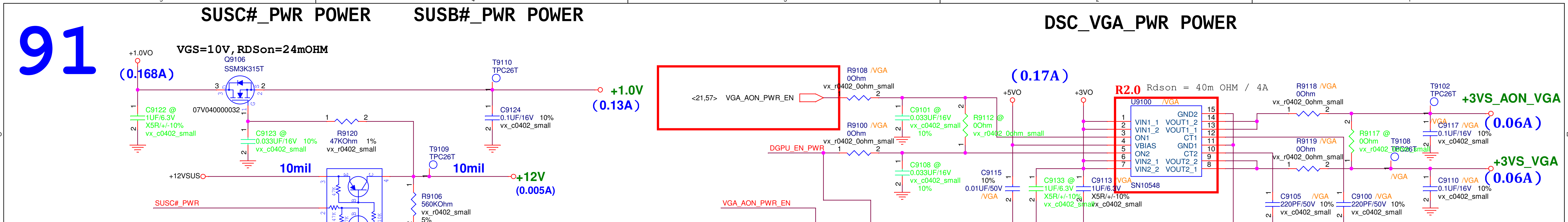
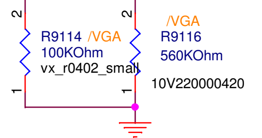
+1.35VS_VGA POWER SUPPLY



<Variant Name>

PEGATRON — PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : POWER_+1.05VS	
	Engineer: Remiel_You	
Size: Custom	Project Name: P5HCJ	Rev: 1.2
Date: Monday, June 20, 2016	Sheet 89 of 96	

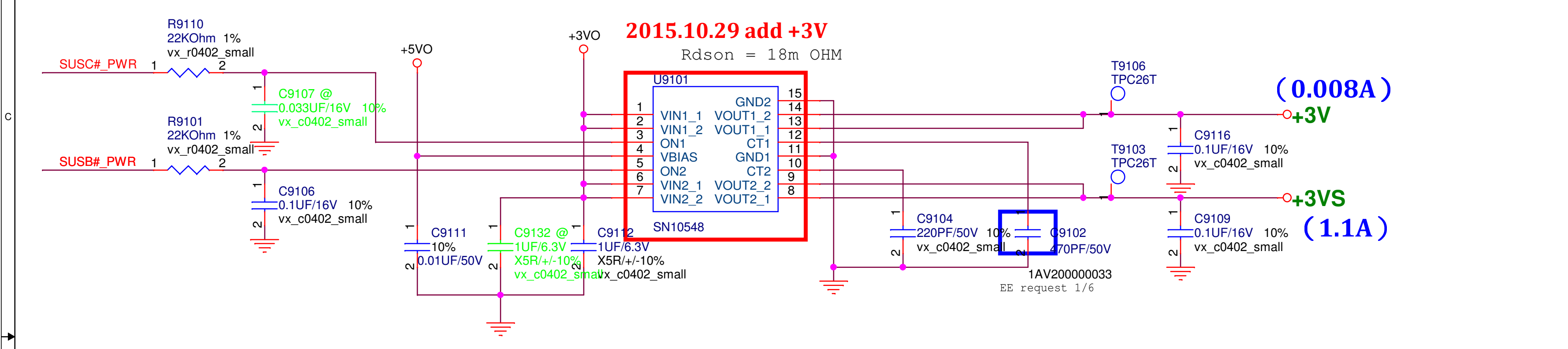




+3VS_VGA
DC Tolerance :+-5%

+1.35VA_VGA DDR3 Single
TDC :2.05A
Dyn :2.88A
EDC :3.62A

+1.35VA_VGA DDR3 Dual
TDC :2.75A
Dyn :4.14A
EDC :4.22A

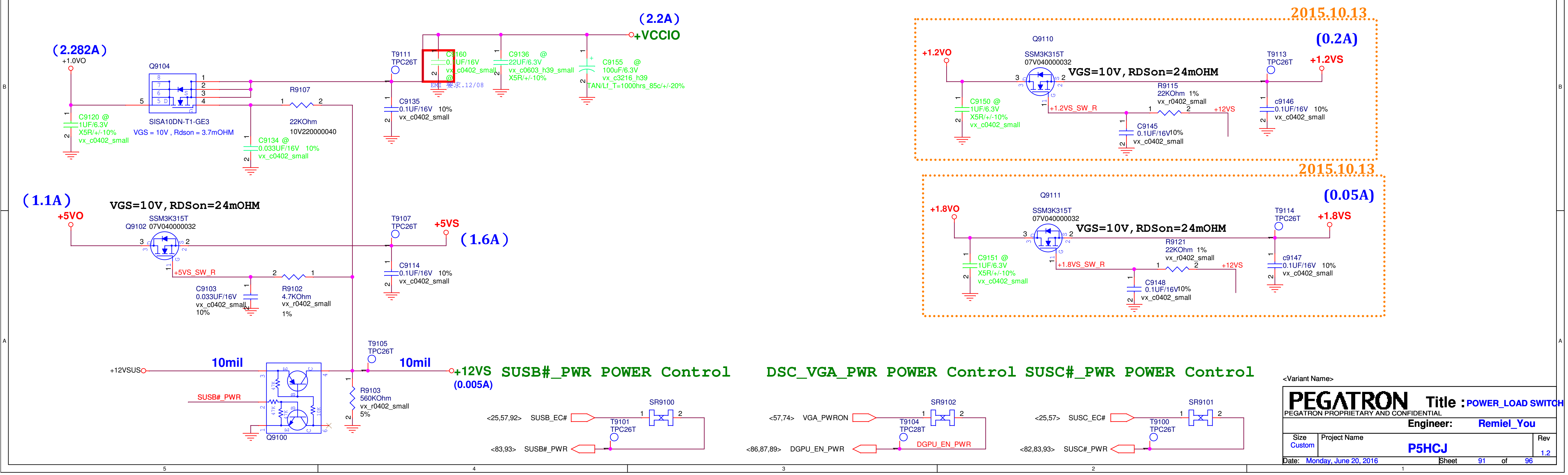


GC6 Cold boot/Optimus:
3V3_AON & 3V3_MAIN --> NVVDD --> PEX_VDD --> FBVDD/Q

GC6 2.0 Exit:
3V3_MAIN --> NVVDD --> PEX_VDD

Power up Sequencing
1.The ramp time for any rail must be more 40us and
  is recommended to be less than 2ms
2.The previous power rail must ramp up to 90%
  before the next power rail can start ramping up

Power down Sequencing
1.There is no specific power down sequence
2.Residual voltage from power down must not violate ther power up sequence
  when back to back GPU power down and power up event take place



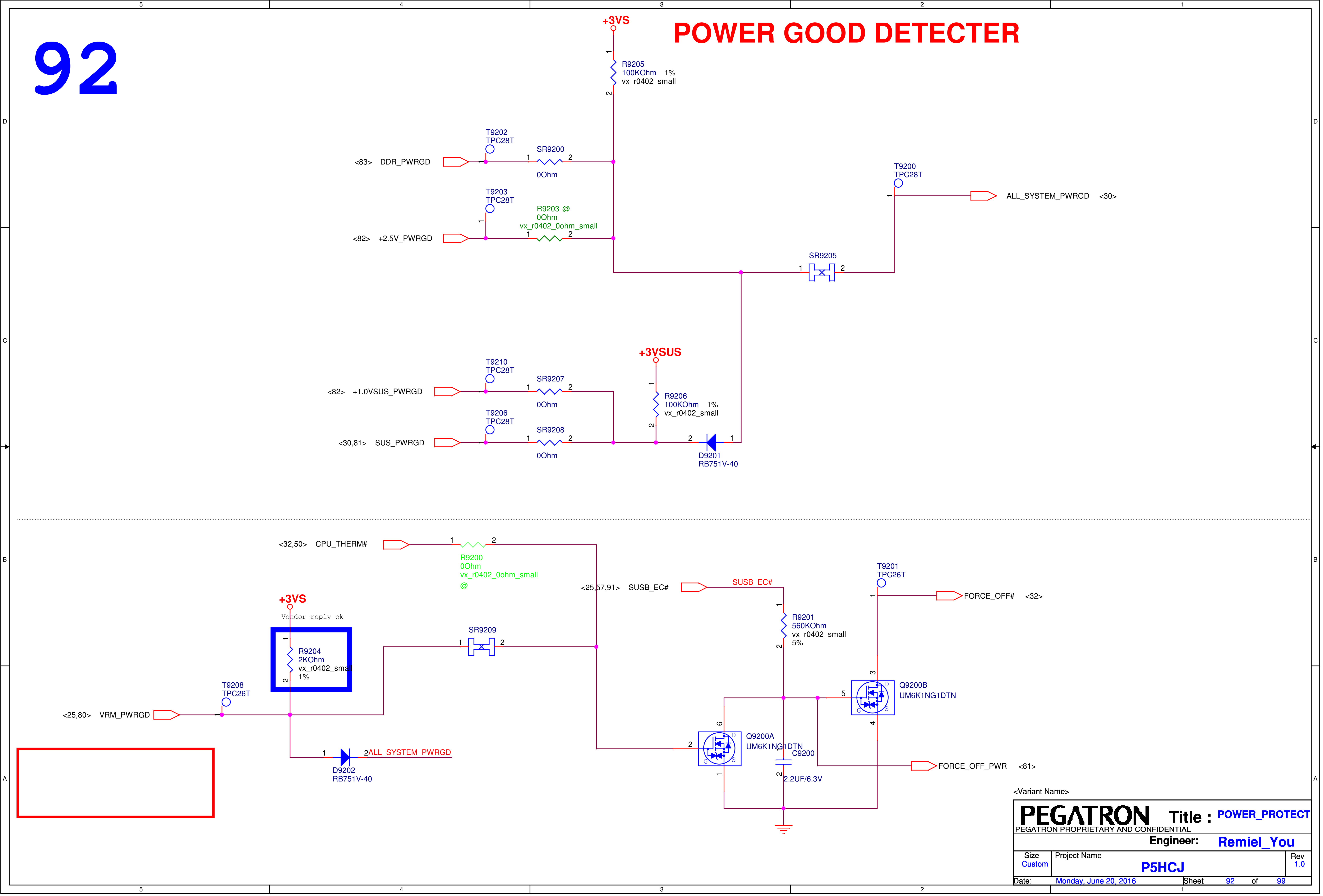
<Variant Name>

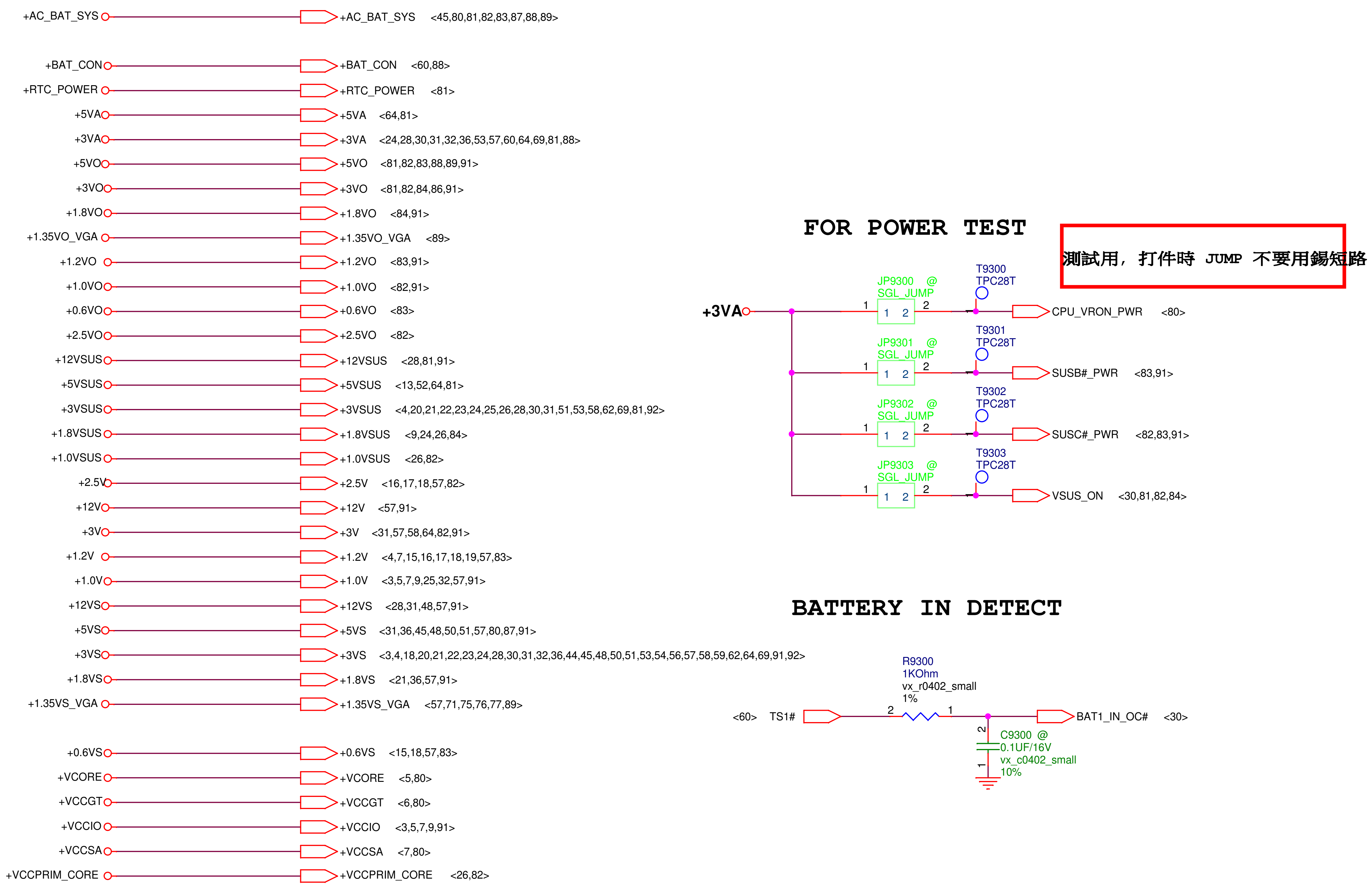
PEGATRON Title : POWER_LOAD SWITCH

Engineer: Remiel_You

Size	Project Name	Rev
Custom	P5HCJ	1.2

Date: Monday, June 20, 2016 Sheet 91 of 96


92
POWER GOOD DETECTER
+3VS
R9205
100KOhm 1%
vx_r0402_small
T9202
TPC28T
SR9200
0Ohm
<83> DDR_PWRGD
T9203
TPC28T
R9203 @
0Ohm
vx_r0402_0ohm_small
<82> +2.5V_PWRGD
T9200
TPC28T
ALL_SYSTEM_PWRGD <30>
SR9205
+3VSUS
T9210
TPC28T
SR9207
0Ohm
<82> +1.0VSUS_PWRGD
R9206
100KOhm 1%
vx_r0402_small
T9206
TPC28T
SR9208
0Ohm
<30,81> SUS_PWRGD
D9201
RB751V-40
<32,50> CPU_THERM#
R9200
0Ohm
vx_r0402_0ohm_small
@
<25,57,91> SUSB_EC#
SUSB_EC#
T9201
TPC26T
FORCE_OFF# <32>
+3VS
Vendor reply ok
R9201
560KOhm
vx_r0402_small
5%
SR9209
R9204
2KOhm
vx_r0402_small
1%
T9208
TPC26T
<25,80> VRM_PWRGD
Q9200B
UM6K1NG1DTN
Q9200A
UM6K1NG1DTN
C9200
2.2UF/6.3V
ALL_SYSTEM_PWRGD
D9202
RB751V-40
FORCE_OFF_PWR <81>
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : POWER_PROTECT
Engineer: Remiel_You
Size Custom
Project Name P5HCJ
Rev 1.0
Date: Monday, June 20, 2016
Sheet 92 of 99



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

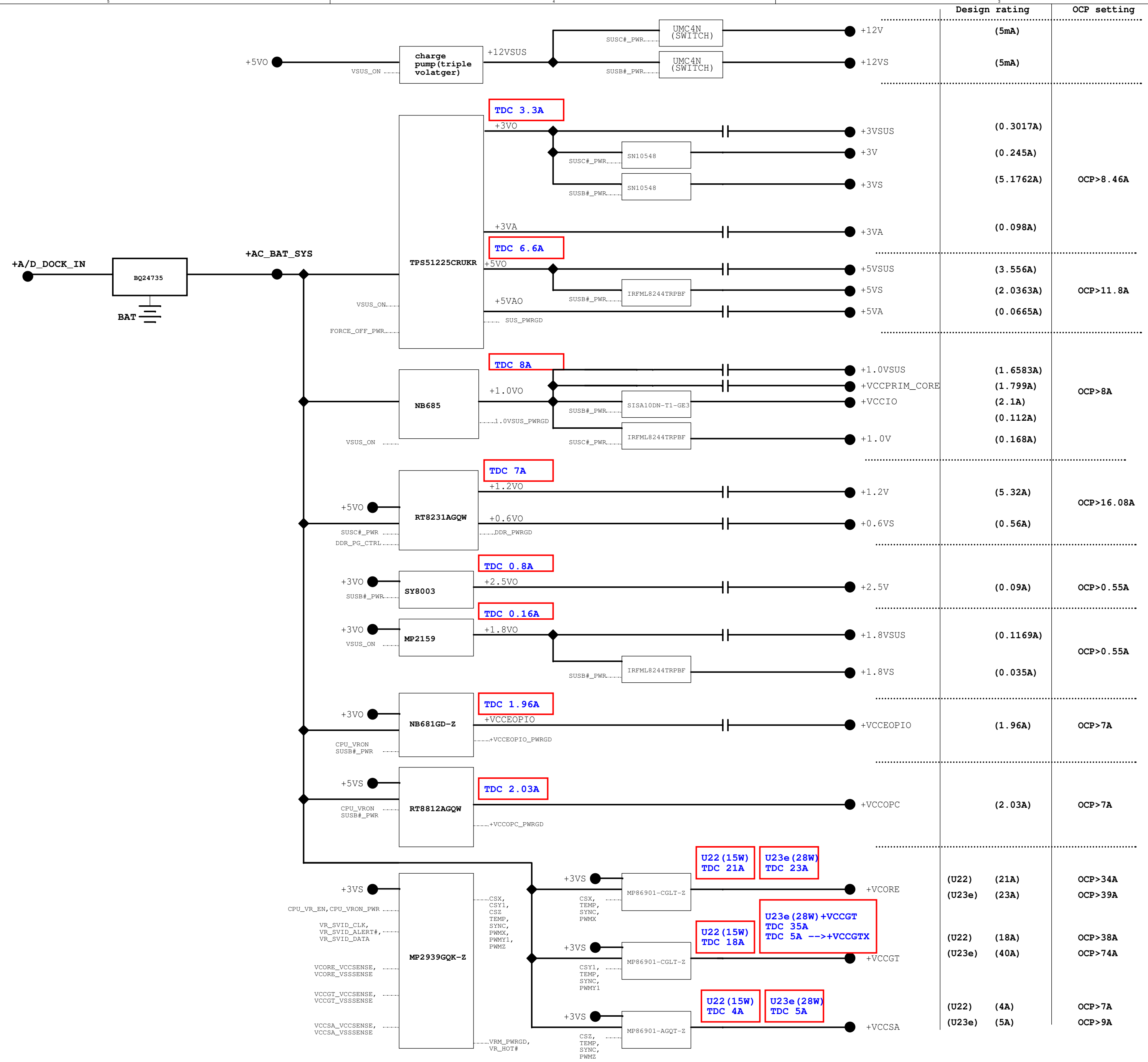
Title : POWER_SIGNAL

BG1-POWER

Engineer: Mike_Ke

Size	Project Name	Rev
B	P5HCJ	1.0

Date: Monday, June 20, 2016 Sheet 93 of 94



PEGATRON
Title: POWER_FLOWCHART
Engineer: Remiel_You
Project Name: P5HCJ

modify notice

Version Date	Description
2015/0626	Change all Jumper back (from Rsense) Remove 1.8VSUS snubber

<Variant Name>

PEGATRON PEGATRON PROPRIETARY AND CONFIDENTIAL	Title : POWER_History	
	Engineer: Remiel_You	
Size Custom	Project Name P5HCJ	Rev 1.0
Date: Monday, June 20, 2016	Sheet 96 of 96	