Jones/Cujo BLOCK DIAGRAM

01

PCB STACK UP

8L Dis.

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN2
LAYER 4 : SGND1
LAYER 5 : SVCC
LAYER 6 : IN2
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking PAGE 36
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 37
- SYSTEM POWER ISL6237IRZ-T PAGE 38
- DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAGE 42
- VCCP +1.5V AND GMCH 1.05V(RT8204) PAGE 39
- VGACORE(1.025V)Oz8119 PAGE 41
- CPU CORE ISL6262A PAGE 40

CPU Penryn
478P (uPGA)/35W
PAGE 3,4

CPU THERMAL SENSOR PAGE 4

FSB 667/800/1066

14.318MHz

CLOCK GEN
ALPRS355B MLF64PIN
PAGE 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Cantiga
PM45,GM45
PAGE 5~9

Level Shift PAGE 20

27MHz

DDRII-SODIMM1 PAGE 10 — DDRII 667/800 MHz

DDRII-SODIMM2 PAGE 10 — DDRII 667/800 MHz

PCI-Express 16X

nVIDIA
NB9M-GE 64 Bit
NB9P-GS 128 Bit
PAGE 12~18
969p

Dual Link

HDMI CON PAGE 20

CRT PAGE 20

LCD CONN PAGE 19

Mini PCI-E Card x2
Express Card x1
Cable Docking x1
4,7,10,11

DMI LINK

32.768KHz

NBSRCCLK, NBSRCCLK#

SOUTH BRIDGE
ICH9-M
PAGE 21,22,23,24

USB2.0

0,1,8,9 — **USB2.0 Ports X4** PAGE 29

5 — **BlueTooth** PAGE 29

3 — **Webcam** PAGE 29

2 — **Fingerprint** PAGE 29

SATA0 150MB — **SATA - HDD** PAGE 32

SATA1 150MB — **SATA - CD-ROM** PAGE 32

SATA4 150MB — **SATA - 2ndHDD** PAGE 32

SATA5 150MB — **E-SATA** PAGE 29

SMBUS — Accelerometer LIS3LV02DL PAGE 27

32.768KHz

LPC

PCI-E

24.576Hz

Azalia

X2 — **Mini PCI-E Card** (Wireless LAN/TV) PAGE 35

X1 — **LAN** Realtek PCIE-LAN RTL8102E/8111C (10/100/GagaLAN) PAGE 30,31

X1 — **Express Card** (NEW CARD) PAGE 32

X1 — **JMICRO 380 for Discrete** PAGE25

Analog IDT92HD75B3 PAGE 26

MDC CONN PAGE 33

25MHz

RJ45 PAGE 30

IEEE1394 connect for Discrete only PAGE 25

Memory CardReader PAGE 25

AUDIO Amplifier TPA6047 PAGE 27

AUDIO Amplifier TPA3007D1 PAGE 28

Keyboard Touch Pad PAGE 33 PAGE 34

Capacitive Sense SW PAGE 33

ENE KBC
KB3926 C0
PAGE 34

SPI PAGE 22

microphone PAGE 28

Audio Jacks (Phone/ MIC) PAGE 28

Jack to Speaker PAGE 27

Jack to Sub-Woofer PAGE 28

GMT G9931P1U
FAN PAGE 36

SPI PAGE 34

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	PV

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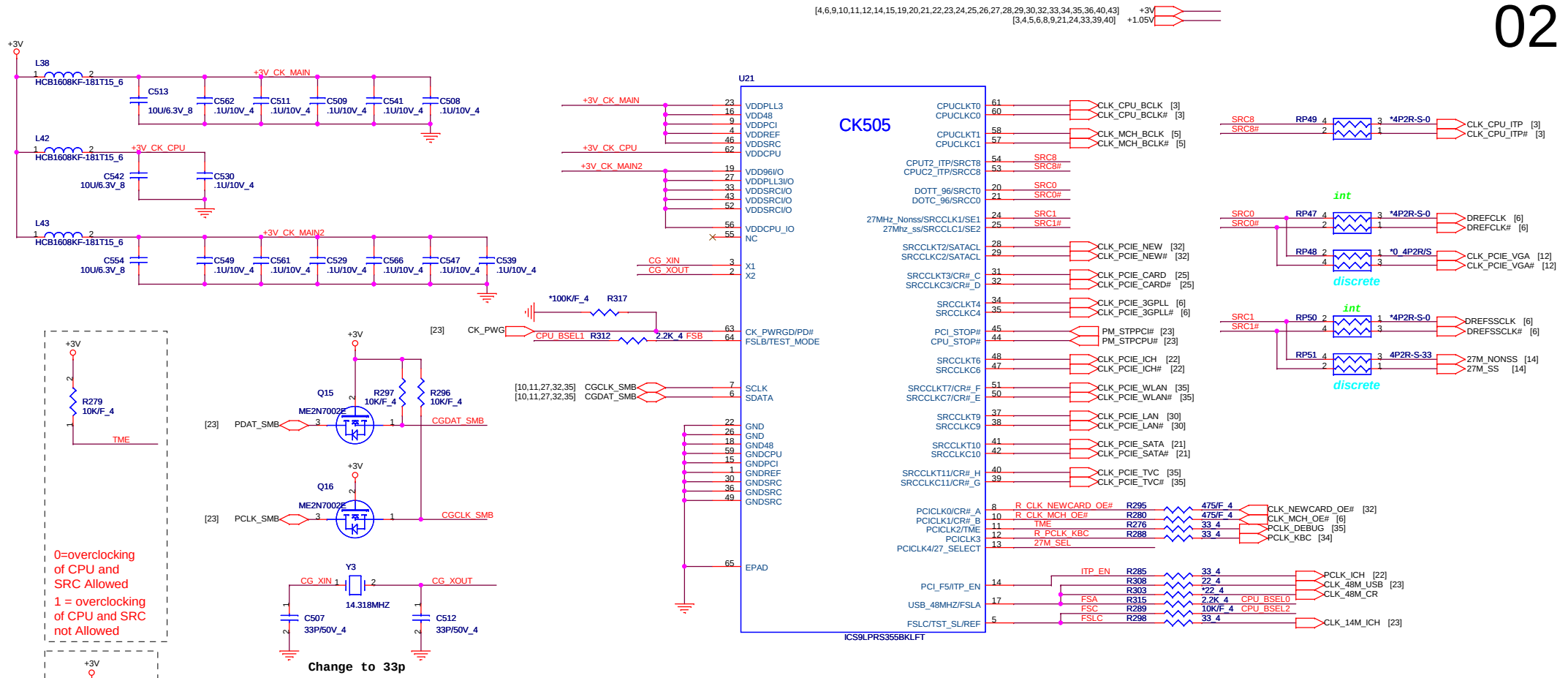
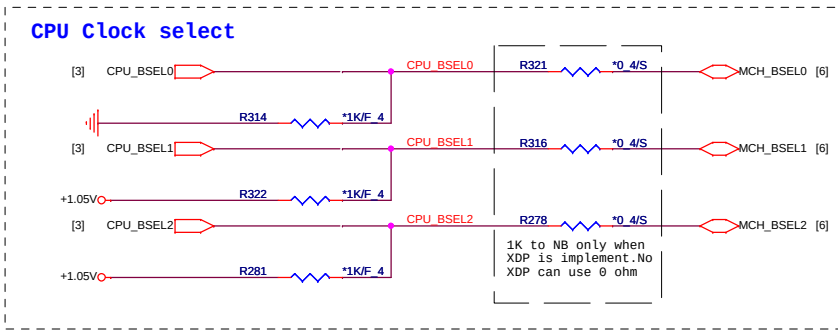


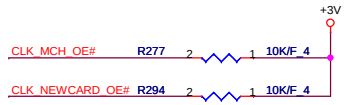
27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

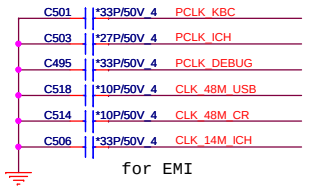
CK505 QFN64

ICS	ICS9LPRS355BKLF	ALPRS355000
Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000
SPECTRALINEAR	SL28541BQCT	AL028541000



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33





PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Clock Generator	PV

Date: Monday, October 20, 2008 Sheet 2 of 43

U34A

ADDR GROUP 0

ADDR GROUP 1

CONTROL

XDP/ITP SIGNALS

THERMAL

MISC

H CLK

Quard Core Only

Penryn Ball-out Rev 1a

U34B

DATA GRP 0

DATA GRP 1

DATA GRP 2

DATA GRP 3

Penryn Ball-out Rev 1a

For QC CPU

For QC CPU

For QC CPU

For QC CPU

DB modified

Add R61

R542 -->1.74K for Quad Core

	Rc
Dual Core	2K Ohm
Quard Core	1.74K Ohm

MODEL	UT5 Quad Core	UT3 Dual Core
R28	*0_4	0_4

	COMP0/2	COMP1/3
Dual Core	27.4 Ohm (CS02742FB19)	54.9 Ohm (CS05492FB19)
Quard Core	24.9 Ohm (CS02492FB29)	49.9 Ohm (CS04992FB31)

For QC Support

Don't install for DC

Change to +5V

Populate ITP700Flex for bringup

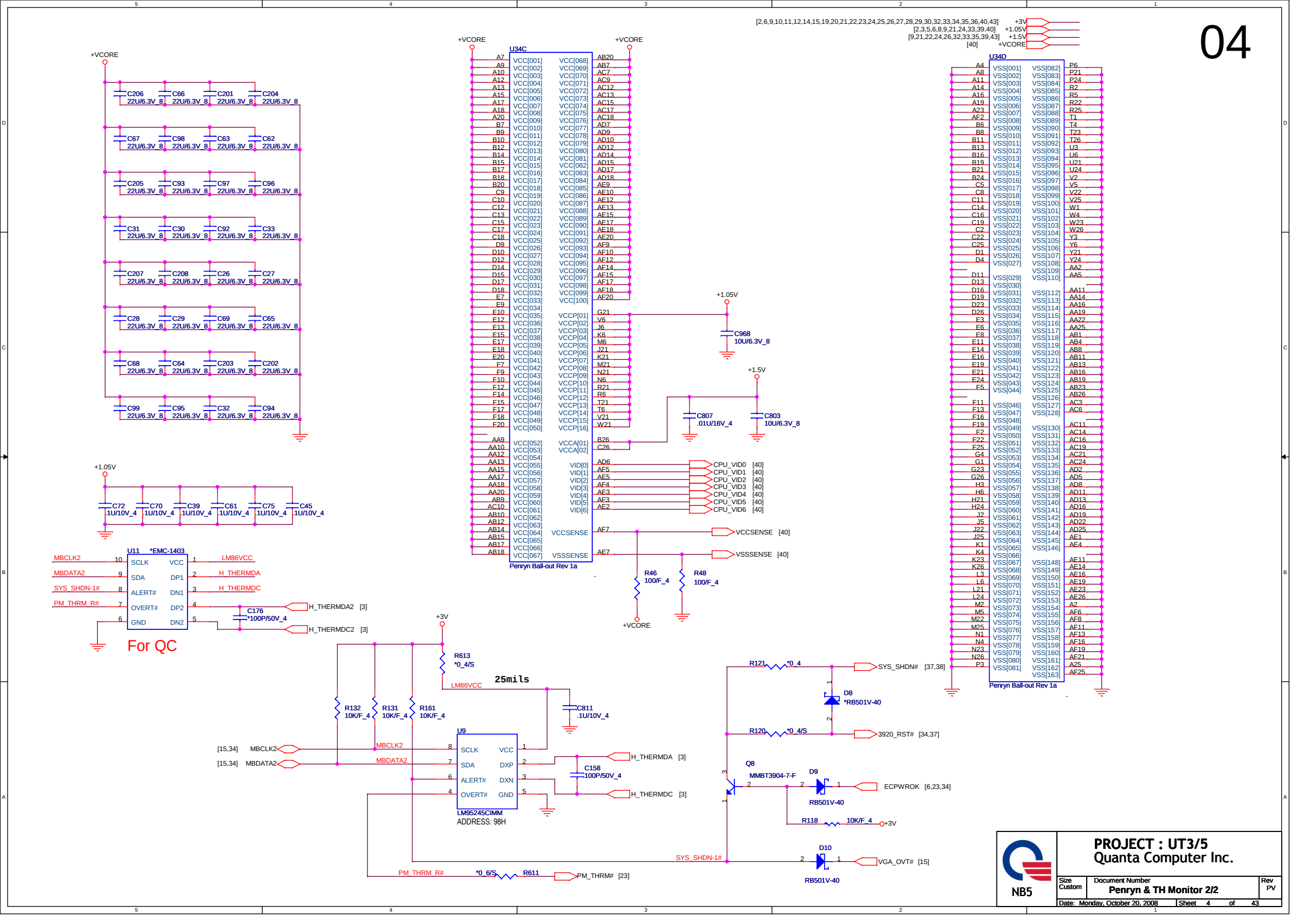
*ITP700Flex

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size: Custom | Document Number: Penryn 1/2 | Rev: PV

Date: Monday, October 20, 2008 | Sheet 3 of 43


04
+VCORE
C206 22U/6.3V_8
C66 22U/6.3V_8
C201 22U/6.3V_8
C204 22U/6.3V_8
C67 22U/6.3V_8
C98 22U/6.3V_8
C63 22U/6.3V_8
C62 22U/6.3V_8
C205 22U/6.3V_8
C93 22U/6.3V_8
C97 22U/6.3V_8
C96 22U/6.3V_8
C31 22U/6.3V_8
C30 22U/6.3V_8
C92 22U/6.3V_8
C33 22U/6.3V_8
C207 22U/6.3V_8
C208 22U/6.3V_8
C26 22U/6.3V_8
C27 22U/6.3V_8
C28 22U/6.3V_8
C29 22U/6.3V_8
C69 22U/6.3V_8
C65 22U/6.3V_8
C68 22U/6.3V_8
C64 22U/6.3V_8
C203 22U/6.3V_8
C202 22U/6.3V_8
C99 22U/6.3V_8
C95 22U/6.3V_8
C32 22U/6.3V_8
C94 22U/6.3V_8
+1.05V
C72 .1U/10V_4
C70 .1U/10V_4
C39 .1U/10V_4
C61 .1U/10V_4
C75 .1U/10V_4
C45 .1U/10V_4
U11 *EMC-1403
MBCLK2
MBDATA2
SYS_SHDN-1#
PM_THRM_R#
SCLK
SDA
ALERT#
OVERT#
GND
VCC
DP1
DN1
DP2
DN2
LM86VCC
H_THERMDA
H_THERMDC
C176 *100P/50V_4
H_THERMDA2 [3]
H_THERMDC2 [3]
For QC
+VCORE
U34C
VCC[001] VCC[002] VCC[003] VCC[004] VCC[005] VCC[006] VCC[007] VCC[008] VCC[009] VCC[010] VCC[011] VCC[012] VCC[013] VCC[014] VCC[015] VCC[016] VCC[017] VCC[018] VCC[019] VCC[020] VCC[021] VCC[022] VCC[023] VCC[024] VCC[025] VCC[026] VCC[027] VCC[028] VCC[029] VCC[030] VCC[031] VCC[032] VCC[033] VCC[034] VCC[035] VCC[036] VCC[037] VCC[038] VCC[039] VCC[040] VCC[041] VCC[042] VCC[043] VCC[044] VCC[045] VCC[046] VCC[047] VCC[048] VCC[049] VCC[050] VCC[052] VCC[053] VCC[054] VCC[055] VCC[056] VCC[057] VCC[058] VCC[059] VCC[060] VCC[061] VCC[062] VCC[063] VCC[064] VCC[065] VCC[066] VCC[067]
VCC[068] VCC[069] VCC[070] VCC[071] VCC[072] VCC[073] VCC[074] VCC[075] VCC[076] VCC[077] VCC[078] VCC[079] VCC[080] VCC[081] VCC[082] VCC[083] VCC[084] VCC[085] VCC[086] VCC[087] VCC[088] VCC[089] VCC[090] VCC[091] VCC[092] VCC[093] VCC[094] VCC[095] VCC[096] VCC[097] VCC[098] VCC[099] VCC[100]
VCCP[01] VCCP[02] VCCP[03] VCCP[04] VCCP[05] VCCP[06] VCCP[07] VCCP[08] VCCP[09] VCCP[10] VCCP[11] VCCP[12] VCCP[13] VCCP[14] VCCP[15] VCCP[16]
VCCA[01] VCCA[02]
VID[0] VID[1] VID[2] VID[3] VID[4] VID[5] VID[6]
VCCSENSE
VSSSENSE
Penryn Ball-out Rev 1a
+1.05V
C968 10U/6.3V_8
+1.5V
C807 .01U/16V_4
C803 10U/6.3V_8
CPU_VID0 [40]
CPU_VID1 [40]
CPU_VID2 [40]
CPU_VID3 [40]
CPU_VID4 [40]
CPU_VID5 [40]
CPU_VID6 [40]
VCCSENSE [40]
VSSSENSE [40]
R46 100/F_4
R48 100/F_4
+VCORE
[2,6,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[2,3,5,6,8,9,21,24,33,39,40] +1.05V
[9,21,22,24,26,32,33,35,39,43] +1.5V
[40] +VCORE
U34D
VSS[001] VSS[002] VSS[003] VSS[004] VSS[005] VSS[006] VSS[007] VSS[008] VSS[009] VSS[010] VSS[011] VSS[012] VSS[013] VSS[014] VSS[015] VSS[016] VSS[017] VSS[018] VSS[019] VSS[020] VSS[021] VSS[022] VSS[023] VSS[024] VSS[025] VSS[026] VSS[027] VSS[029] VSS[030] VSS[031] VSS[032] VSS[033] VSS[034] VSS[035] VSS[036] VSS[037] VSS[038] VSS[039] VSS[040] VSS[041] VSS[042] VSS[043] VSS[044] VSS[046] VSS[047] VSS[048] VSS[049] VSS[050] VSS[051] VSS[052] VSS[053] VSS[054] VSS[055] VSS[056] VSS[057] VSS[058] VSS[059] VSS[060] VSS[061] VSS[062] VSS[063] VSS[064] VSS[065] VSS[066] VSS[067] VSS[068] VSS[069] VSS[070] VSS[071] VSS[072] VSS[073] VSS[074] VSS[075] VSS[076] VSS[077] VSS[078] VSS[079] VSS[080] VSS[081]
VSS[082] VSS[083] VSS[084] VSS[085] VSS[086] VSS[087] VSS[088] VSS[089] VSS[090] VSS[091] VSS[092] VSS[093] VSS[094] VSS[095] VSS[096] VSS[097] VSS[098] VSS[099] VSS[100] VSS[101] VSS[102] VSS[103] VSS[104] VSS[105] VSS[106] VSS[107] VSS[108] VSS[109] VSS[110] VSS[112] VSS[113] VSS[114] VSS[115] VSS[116] VSS[117] VSS[118] VSS[119] VSS[120] VSS[121] VSS[122] VSS[123] VSS[124] VSS[125] VSS[126] VSS[127] VSS[128] VSS[130] VSS[131] VSS[132] VSS[133] VSS[134] VSS[135] VSS[136] VSS[137] VSS[138] VSS[139] VSS[140] VSS[141] VSS[142] VSS[143] VSS[144] VSS[145] VSS[146] VSS[148] VSS[149] VSS[150] VSS[151] VSS[152] VSS[153] VSS[154] VSS[155] VSS[156] VSS[157] VSS[158] VSS[159] VSS[160] VSS[161] VSS[162] VSS[163]
Penryn Ball-out Rev 1a
+3V
R613 *0_4/S
25mils
LM86VCC
C811 .1U/10V_4
R132 10K/F_4
R131 10K/F_4
R161 10K/F_4
U9
[15,34] MBCLK2
[15,34] MBDATA2
SCLK
SDA
ALERT#
OVERT#
VCC
DXP
DXN
GND
C158 100P/50V_4
H_THERMDA [3]
H_THERMDC [3]
LM95245CIMM
ADDRESS: 98H
PM_THRM_R#
*0_6/S
R611
PM_THRM# [23]
R121 *0_4
SYS_SHDN# [37,38]
D8 *RB501V-40
R120 *0_4/S
3920_RST# [34,37]
Q8 MMBT3904-7-F
D9 RB501V-40
ECPWROK [6,23,34]
R118 10K/F_4
+3V
SYS_SHDN-1#
D10 RB501V-40
VGA_OVT# [15]
PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size Custom
Document Number
Penryn & TH Monitor 2/2
Rev PV
Date: Monday, October 20, 2008
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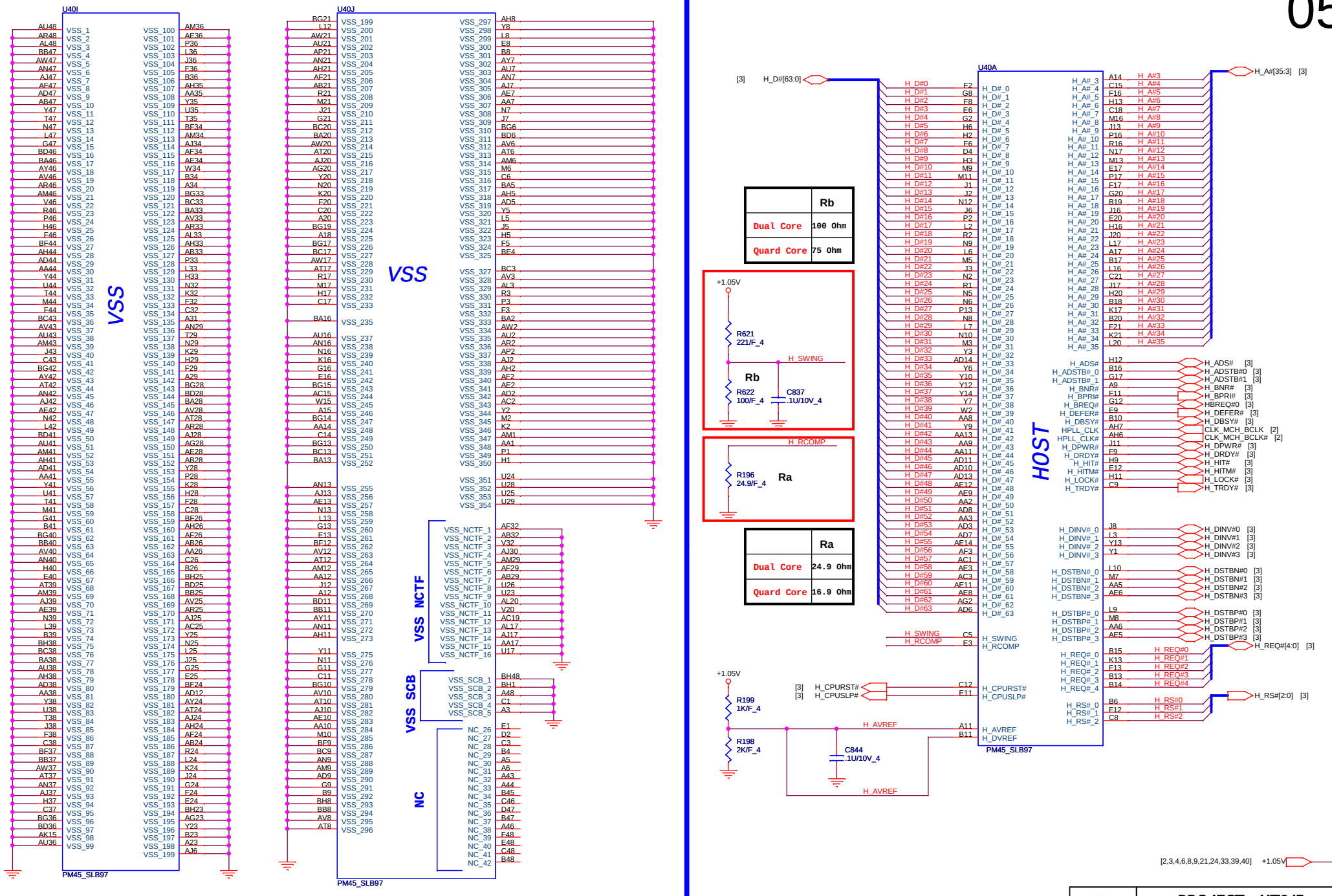

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga Host & VSS 1/5	PV

NB5

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MCH_CFG_5 DMIx2 selection
Low = DMI X2
High = DMI X4 (Default)

MCH_CFG_16 FSB Dynamic ODT
Low = Dynamic ODT disabled
High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal
Low = Normal operation (Default)
High = Reverse Lanes

MCH_CFG_6 iTPM Host Interface
Low =The iTPM Host Interface is enabled2
High = The iTPM Host Interface is disabled (default)

MCH_CFG_7 Intel (R) Management Engine Crypto
Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable
Low = Enabled3
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH_CFG_20

Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE
Low = Only digital display port (SDVO/DP/iHDMI) or PCIE is operational (default)

High = Digital display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port

MCH_CFG2:0

000 = FSB1066
010 = FSB800
011 = FSB667
Others = Reserved

U40B

RSVD
RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD22 RSVD23 RSVD24 RSVD25

DDR CLK/ CONTROL/COMPENSATION
SA_CK_0 SA_CK_1 SA_CK_0 SA_CK_1 SA_CK#_0 SA_CK#_1 SA_CK#_0 SA_CK#_1 SA_CKE_0 SA_CKE_1 SA_CKE_0 SA_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST#
M_A_CLK0 M_A_CLK1 M_B_CLK0 M_B_CLK1 M_A_CLK0# M_A_CLK1# M_B_CLK0# M_B_CLK1# M_A_CKE0 M_A_CKE1 M_B_CKE0 M_B_CKE1 M_A_CS#0 M_A_CS#1 M_B_CS#0 M_B_CS#1 M_A_ODT0 M_A_ODT1 M_B_ODT0 M_B_ODT1
SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL +0.9VSMVREF_MCH SW_PWROK_NB SM_REXT TP_SM_DRAMRST#
R219 80.6/F_4, R209 80.6/F_4, R237 10K/F_4, R207 499/F_4, TP34
+1.8VSUS

CLK
DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# PEG_CLK PEG_CLK#
DREFCLK DREFCLK# DREFSSCLK DREFSSCLK# CLK_PCIE_3GPLL CLK_PCIE_3GPLL#

ME JTAG
TP36 ME_JTAG_TCK, TP32 ME_JTAG_TDI, TP29 ME_JTAG_TDO, TP28 ME_JTAG_TMS

DMI
DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3
DMI_TXN0 DMI_TXN1 DMI_TXN2 DMI_TXN3 DMI_TXP0 DMI_TXP1 DMI_TXP2 DMI_TXP3
DMI_TXN[3:0] DMI_TXP[3:0] DMI_RXN[3:0] DMI_RXP[3:0]

CFG
MCH_BSEL0 MCH_BSEL1 MCH_BSEL2
MCH_CFG_3 MCH_CFG_4 MCH_CFG_5 MCH_CFG_6 MCH_CFG_7 MCH_CFG_8 MCH_CFG_9 MCH_CFG_10 MCH_CFG_11 MCH_CFG_12 MCH_CFG_13 MCH_CFG_14 MCH_CFG_15 MCH_CFG_16 MCH_CFG_17 MCH_CFG_18 MCH_CFG_19 MCH_CFG_20
CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

PM
PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR
PM_EXTTS#0 PM_EXTTS#1 R201 100/F_4 RST_IN#_MCH

GRAPHICS VID
GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VR_EN
GFXVR_VID_0 GFXVR_VID_1 GFXVR_VID_2 GFXVR_VID_3 GFXVR_VID_4 GFXVR_EN
TP66 TP65 TP33 TP31 TP30 TP67

ME
CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF
CL_CLK0 CL_DATA0 ECPWROK CL_RST#0 MCH_CLVREF
0.35 V
R257 1K/F_4, R258 499/F_4, C451 1U/10V_4

NC
NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22 NC_23 NC_24 NC_25 NC_26

MISC
DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# TSATN#
DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CLK SDVO_DATA CLK_MCH_OE# MCH_ICH_SYNC# MCH_TSATN
TP27 TP26 R200 56.2/F_4

HDA
HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC
ACZ_SDIN3_MCH R638 *0_4/S
ACZ_BITCLK_MCH ACZ_RST#_MCH ACZ_SDIN3 ACZ_SDOUT_MCH ACZ_SYNC_MCH

PM45_SLB97

U40C

LVDS
L_BKLT_CTRL L_BKLT_EN L_CTRL_CLK L_CTRL_DATA L_DDC_CLK L_DDC_DATA L_VDD_EN LVDS_IBG LVDS_VBG LVDS_VREFH LVDS_VREFL LVDSA_CLK# LVDSA_CLK LVDSB_CLK# LVDSB_CLK LVDSA_DATA#_0 LVDSA_DATA#_1 LVDSA_DATA#_2 LVDSA_DATA#_3 LVDSA_DATA_0 LVDSA_DATA_1 LVDSA_DATA_2 LVDSA_DATA_3 LVDSB_DATA#_0 LVDSB_DATA#_1 LVDSB_DATA#_2 LVDSB_DATA#_3 LVDSB_DATA_0 LVDSB_DATA_1 LVDSB_DATA_2 LVDSB_DATA_3
DPST_PWM DISP_ON LVDS_BLON EDIDCLK EDIDDATA LVDS_VBG LA_DATAN3 LA_DATAP3 LB_DATAN3 LB_DATAP3
DPST_PWM_INT LVDS_BLON_INT L_CTRL_CLK L_CTRL_DATA EDIDCLK_INT EDIDDATA_INT DISP_ON_INT LVDS_IBG LA_CLK# LA_CLK LB_CLK# LB_CLK LA_DATAN0 LA_DATAN1 LA_DATAN2 LA_DATAP0 LA_DATAP1 LA_DATAP2 LB_DATAN0 LB_DATAN1 LB_DATAN2 LB_DATAP0 LB_DATAP1 LB_DATAP2

TV
TVA_DAC TVB_DAC TVC_DAC TV_RTN TV_DCONSEL_0 TV_DCONSEL_1
TV_COMP1 TV_Y/G1 TV_C/R1 TV_DCONSEL0 TV_DCONSEL1
Change to 75 ohm to GND
Change to 0 ohm to GND

VGA
CRT_BLUE CRT_GREEN CRT_RED CRT_IRTN CRT_DDC_CLK CRT_DDC_DATA CRT_HSYNC CRT_TVO_IREF CRT_VSYNC
CRT_B CRT_G CRT_R DDCCLK DDCDATA HSYNC_COM VSYNC_COM
CRT_B_1 CRT_G_1 CRT_R_1 DDCCLK_INT DDCDATA_INT HSYNC_INT CRTIREF VSYNC_INT

PCI-EXPRESS GRAPHICS
PEG_TX#[15:0] PEG_TX[15:0] PEG_RX#[15:0] PEG_RX[15:0]
PEG_COMPI PEG_COMPO PEG_COMP R241 49.9/F_4
PEG_RX#_0 PEG_RX#_1 PEG_RX#_2 PEG_RX#_3 PEG_RX#_4 PEG_RX#_5 PEG_RX#_6 PEG_RX#_7 PEG_RX#_8 PEG_RX#_9 PEG_RX#_10 PEG_RX#_11 PEG_RX#_12 PEG_RX#_13 PEG_RX#_14 PEG_RX#_15
PEG_RX_0 PEG_RX_1 PEG_RX_2 PEG_RX_3 PEG_RX_4 PEG_RX_5 PEG_RX_6 PEG_RX_7 PEG_RX_8 PEG_RX_9 PEG_RX_10 PEG_RX_11 PEG_RX_12 PEG_RX_13 PEG_RX_14 PEG_RX_15
PEG_TX#_0 PEG_TX#_1 PEG_TX#_2 PEG_TX#_3 PEG_TX#_4 PEG_TX#_5 PEG_TX#_6 PEG_TX#_7 PEG_TX#_8 PEG_TX#_9 PEG_TX#_10 PEG_TX#_11 PEG_TX#_12 PEG_TX#_13 PEG_TX#_14 PEG_TX#_15
PEG_TX_0 PEG_TX_1 PEG_TX_2 PEG_TX_3 PEG_TX_4 PEG_TX_5 PEG_TX_6 PEG_TX_7 PEG_TX_8 PEG_TX_9 PEG_TX_10 PEG_TX_11 PEG_TX_12 PEG_TX_13 PEG_TX_14 PEG_TX_15
C_PEG_TX#0 C_PEG_TX#1 C_PEG_TX#2 C_PEG_TX#3 C_PEG_TX#4 C_PEG_TX#5 C_PEG_TX#6 C_PEG_TX#7 C_PEG_TX#8 C_PEG_TX#9 C_PEG_TX#10 C_PEG_TX#11 C_PEG_TX#12 C_PEG_TX#13 C_PEG_TX#14 C_PEG_TX#15
C_PEG_TX0 C_PEG_TX1 C_PEG_TX2 C_PEG_TX3 C_PEG_TX4 C_PEG_TX5 C_PEG_TX6 C_PEG_TX7 C_PEG_TX8 C_PEG_TX9 C_PEG_TX10 C_PEG_TX11 C_PEG_TX12 C_PEG_TX13 C_PEG_TX14 C_PEG_TX15
1U/10V_4
PEG_RX#0 PEG_RX#1 PEG_RX#2 PEG_RX#3 PEG_RX#4 PEG_RX#5 PEG_RX#6 PEG_RX#7 PEG_RX#8 PEG_RX#9 PEG_RX#10 PEG_RX#11 PEG_RX#12 PEG_RX#13 PEG_RX#14 PEG_RX#15
PEG_RX0 PEG_RX1 PEG_RX2 PEG_RX3 PEG_RX4 PEG_RX5 PEG_RX6 PEG_RX7 PEG_RX8 PEG_RX9 PEG_RX10 PEG_RX11 PEG_RX12 PEG_RX13 PEG_RX14 PEG_RX15
int
R182 *0_4 HDMI_HPD#
dis

PM45_SLB97

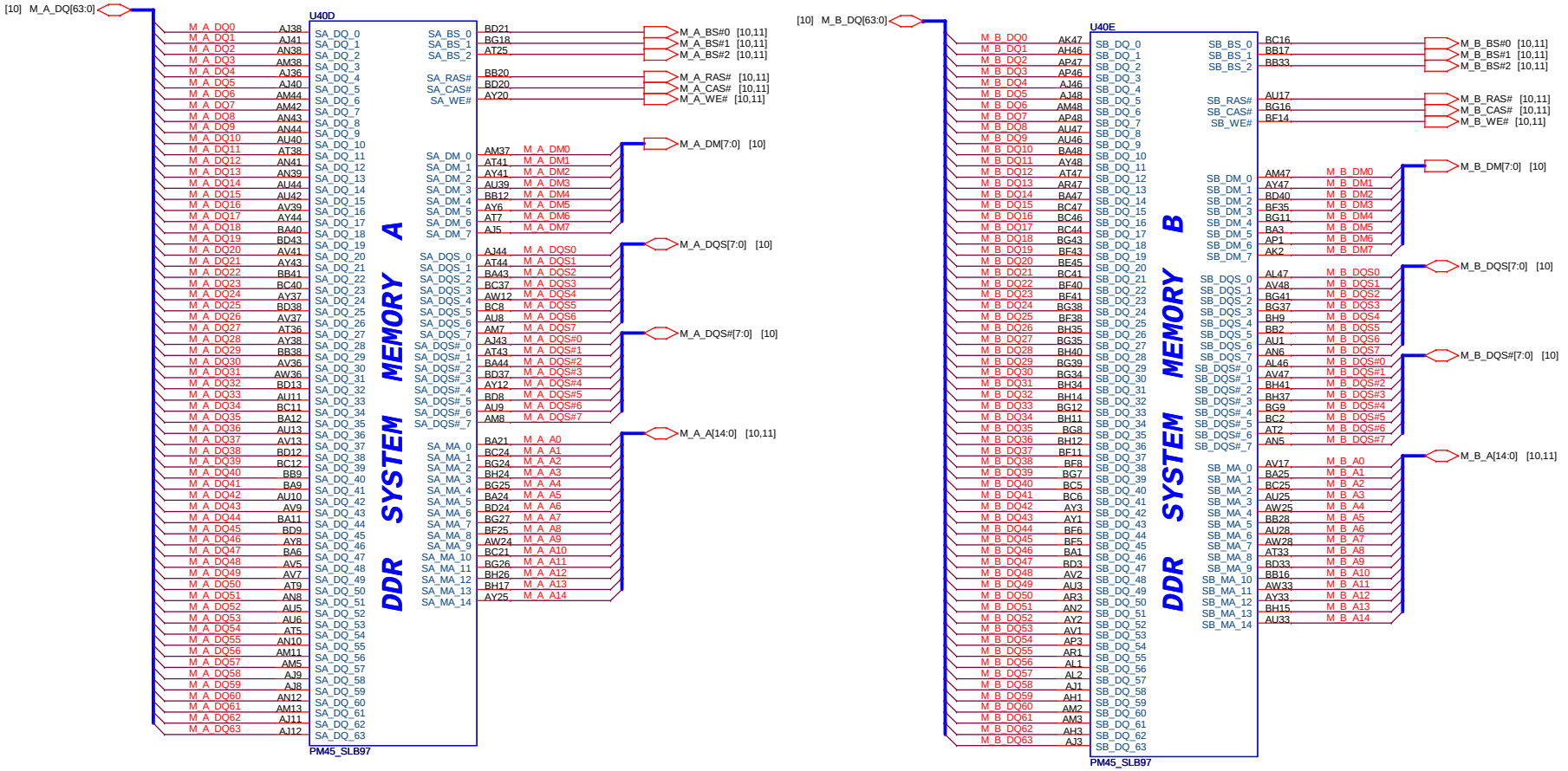
For UMA HDMI Function
RP58 RP59 RP60 RP61 *4P2R-S-0
PEG_TX0 PEG_TX#0 PEG_TX1 PEG_TX#1 PEG_TX2 PEG_TX#2 PEG_TX3 PEG_TX#3
IN_D2 IN_D2# IN_D1 IN_D1# IN_D0 IN_D0# IN_CLK IN_CLK#
C416,C423,C440,C431
C419,C418,C430,C424
Need to install for GM
Level: 0.9V
R552 *20K/F_4 HDMI_HPD#
[20] HDMI_HPD_CON
Q31 *ME2N7002E
R550 *7.5K/F_4
R558 *100K/F_4
HPD# Inverting Level Shifting Circuit

HP SVTP TEST
+1.8VSUS
R253 *1K/F_4
R254 *0_4/S
R251 *1K/F_4
C426 1U/10V_4
C425 470P/50V_4
+0.9VSMVREF_MCH
+0.9VSMVREF [10,42]

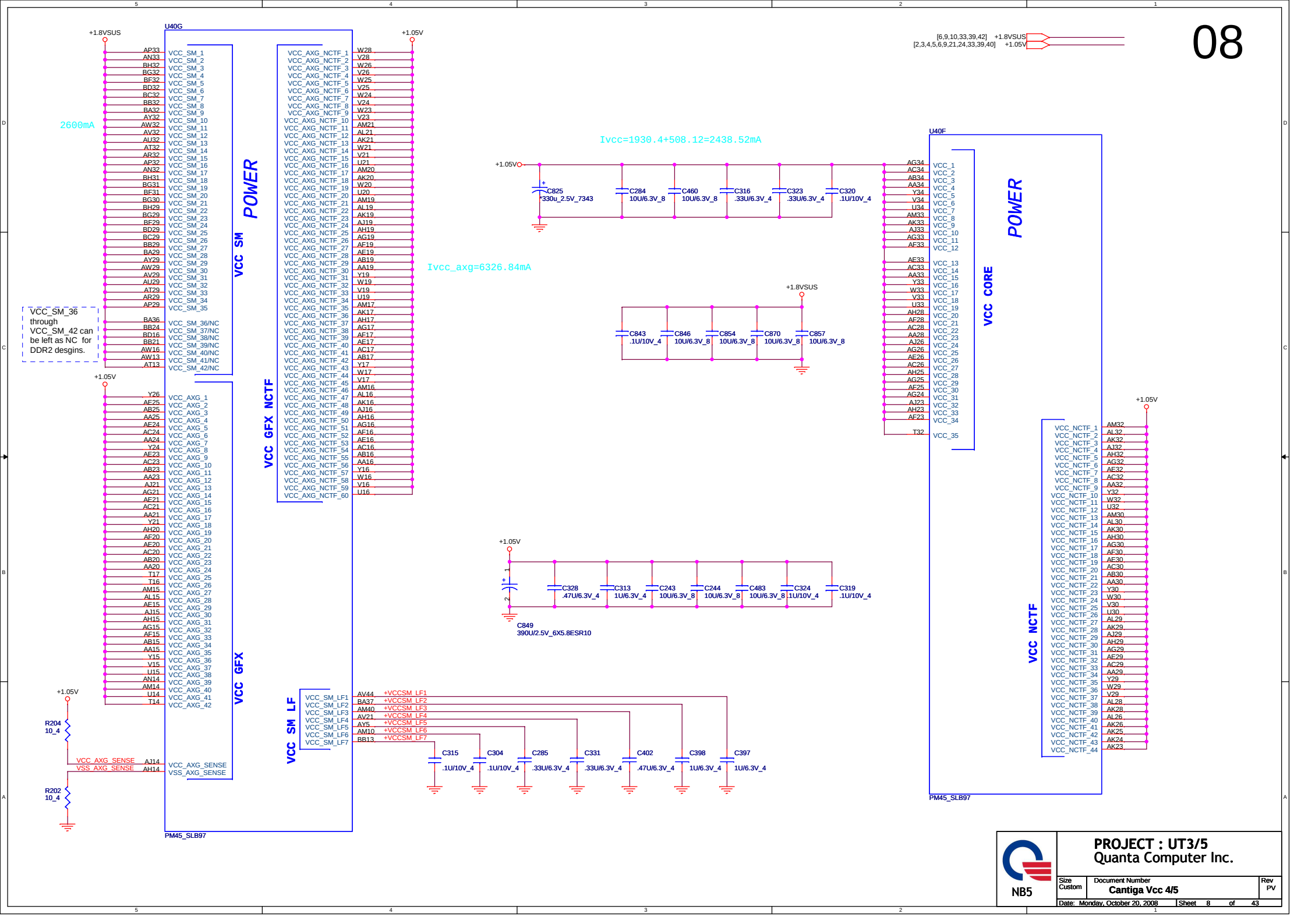
R225 1K/F_4
R222 3.01K/F_4
R218 1K/F_4
C363 .01U/16V_4
C356 2.2U/6.3V_6
C386 .01U/16V_4
C373 2.2U/6.3V_6
SM_RCOMP_VOH
SM_RCOMP_VOL

R634 *33_4
C874 *33P/50V_4
R235 10K/F_4 PM_EXTTS#0
R230 10K/F_4 PM_EXTTS#1

PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size: Custom
Document Number: Cantiga DMI/DISP 2/5
Rev: PV
Date: Monday, October 20, 2008
Sheet 6 of 43



NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size: Custom	Document Number: Cantiga DDR2 3/5	Rev: PV
Date: Monday, October 20, 2008	Sheet 7 of 43	



PROJECT : UT3/5	
Quanta Computer Inc.	
NB5	
Size: Custom	Document Number: Cantiga Vcc 4/5
Rev: PV	
Date: Monday, October 20, 2008	Sheet 8 of 43

+1.05V [2,3,4,5,6,8,21,24,33,39,40]
+3V [2,4,6,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43]
+1.5V [4,21,22,24,26,32,33,35,39,43]
+1.8VSUS [6,8,10,33,39,42]
+1.05V_PEG [2,3,4,5,6,8,21,24,33,39,40]

Change to CX000181016(180 ohm,1.5A) as current request
(L21,L22)

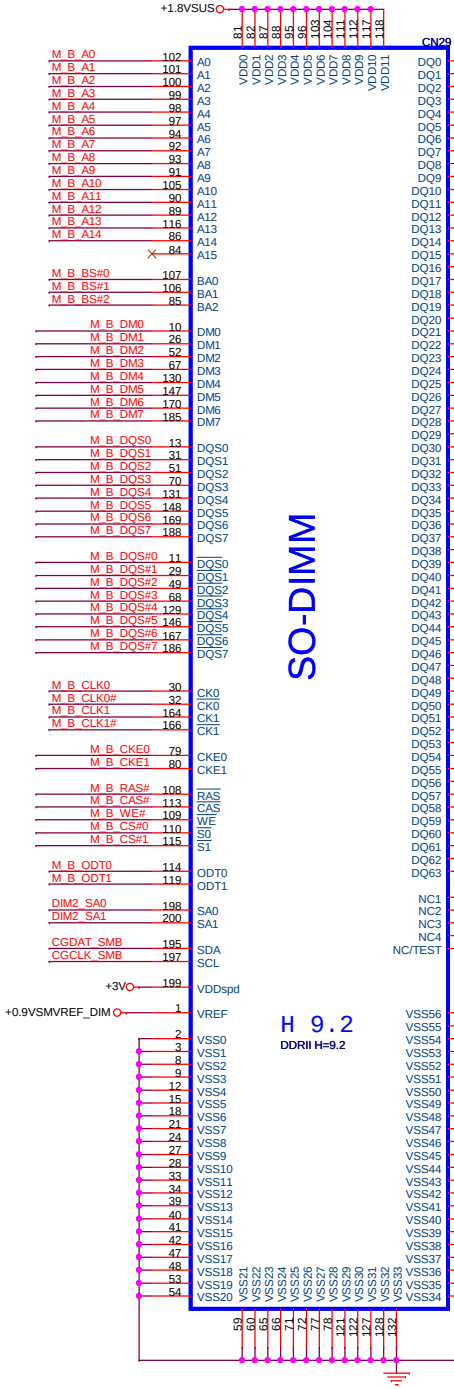
Intel Design Guide 1.5
thermal management is enabled on discrete graphics motherboard

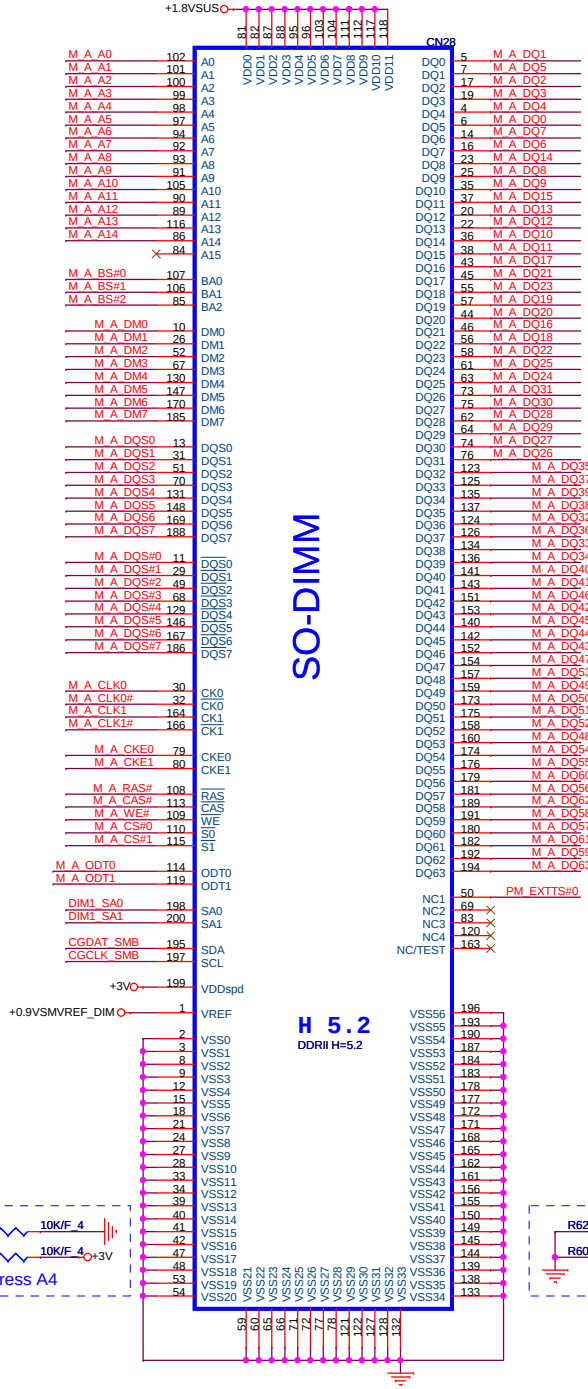
Modify to U40#AF1 power to +1.05V_MPLL as CRB change

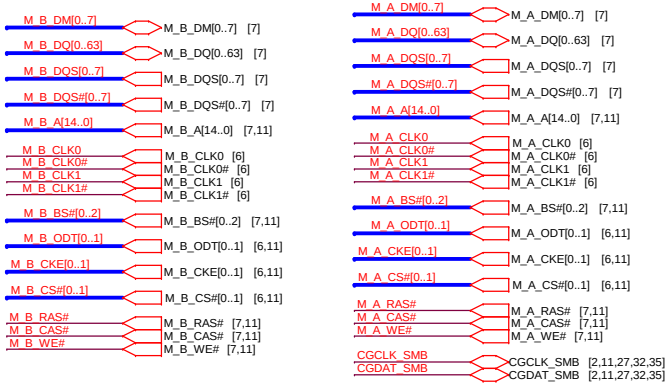
Modify 0829

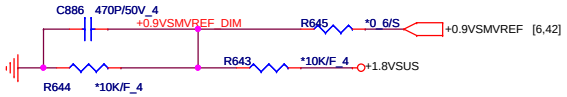
POWER

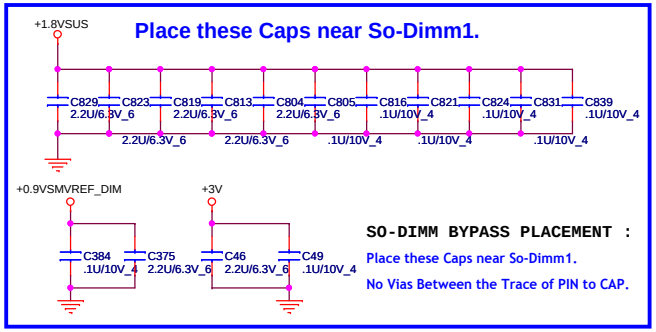
PROJECT : UT3/5
Quanta Computer Inc.
NB5
Size Custom | Document Number Cantiga Power 5/5 | Rev PV
Date: Monday, October 20, 2008 | Sheet 9 of 43

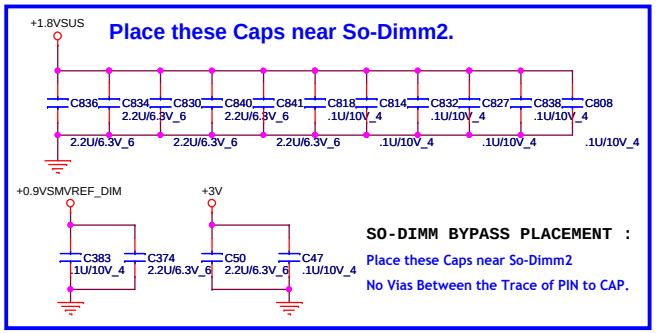












[6,8,9,33,39,42] +1.8VSUS
[2,4,6,9,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 DIMM	PV

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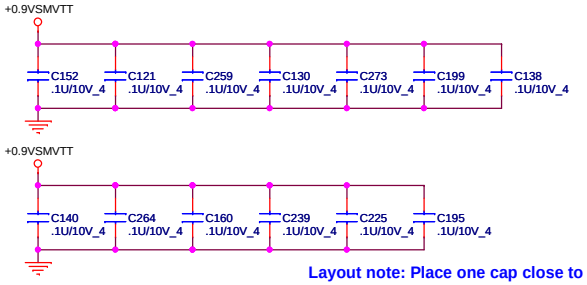
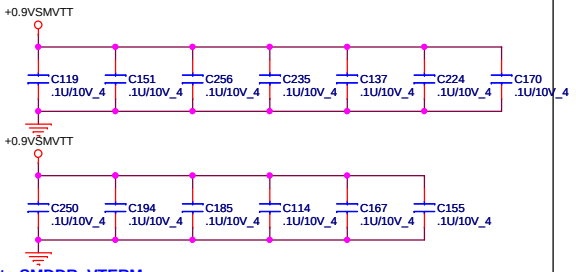
DDRII DUAL CHANNEL A,B.

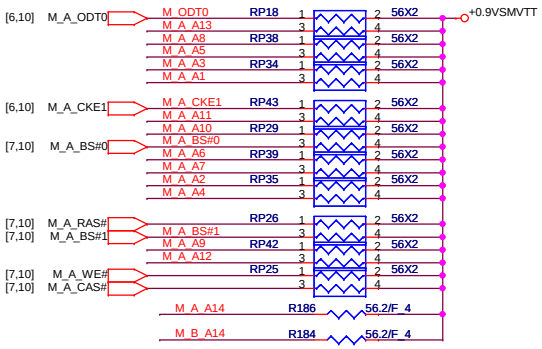
DDRII A CHANNEL

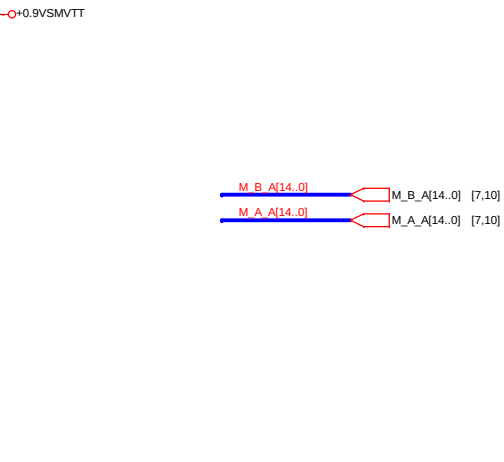


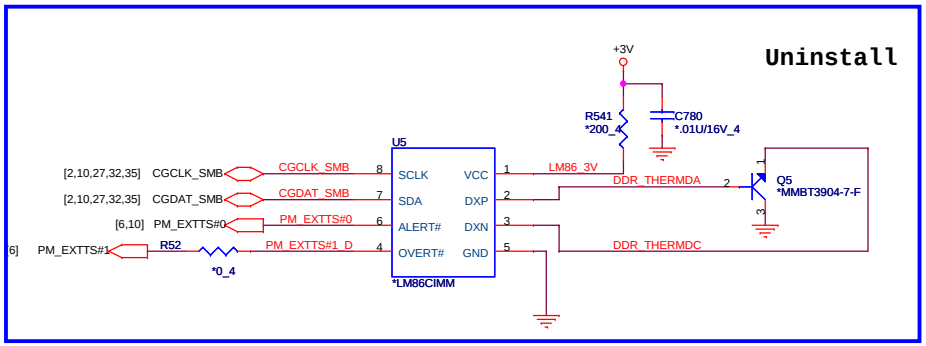
DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM







+0.9VSMVTT [42]

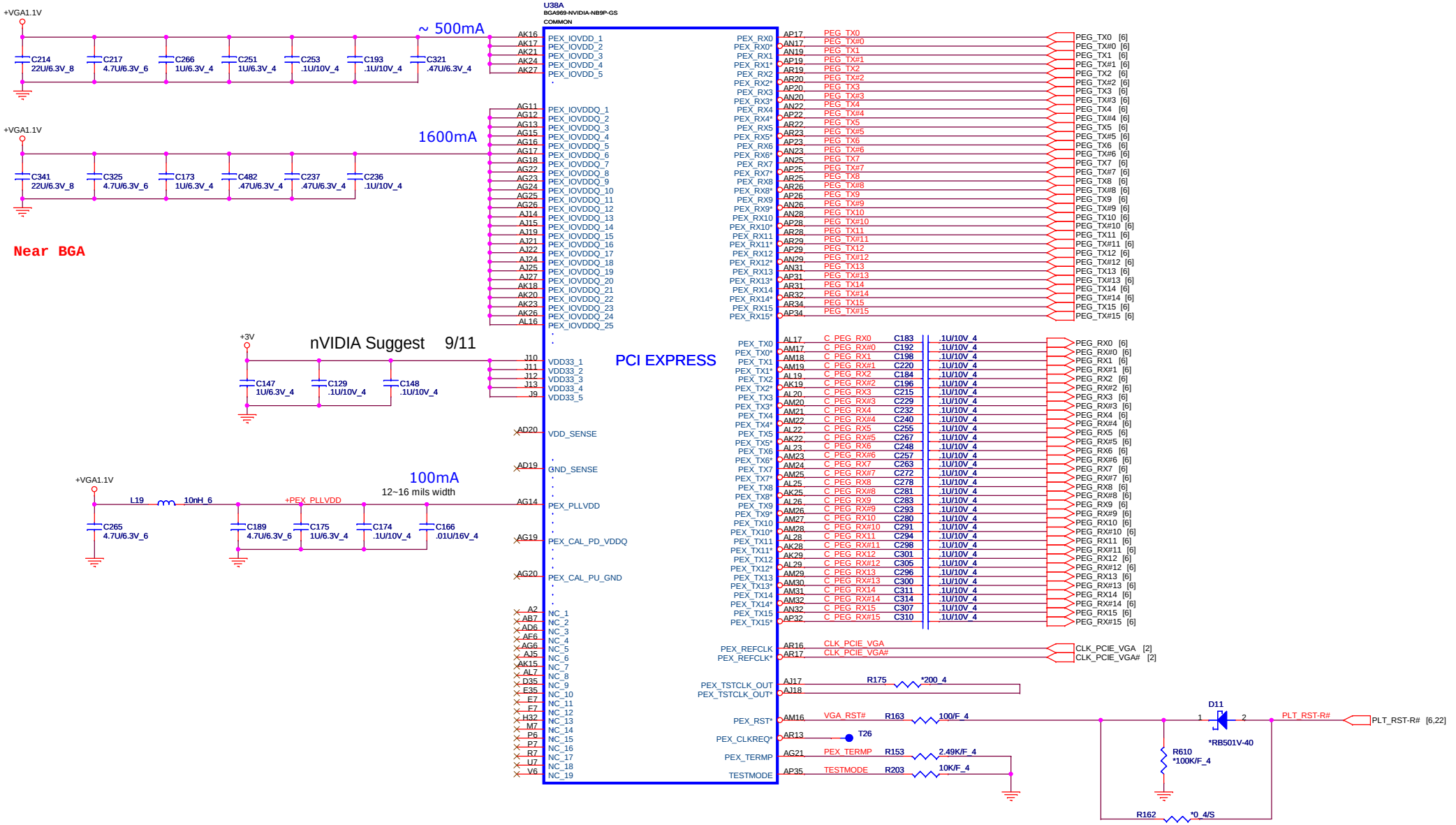
+3V [2,4,6,9,10,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43]

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	DDR2 termination	PV

Date: Monday, October 20, 2008 Sheet 11 of 43



PROJECT :	UT3/5
Quanta Computer Inc.	
Size: Custom	Document Number: NV9X (PCIE I/F) 1/5
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NB5

U38B
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F A

DB modified

U38C
BGA969-NVIDIA-NB9P-GS
COMMON

MEMORY I/F B

DB modified

for DDR2 need use CMD11(CKE) and CMD12(ODT)

use internal Vref, ext divider no stuff

15mils width

For Debug only

G96 only

R178 no stuff

R192 Install for DDR3

For G96 only
For NB9P-GS only

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	NV9X (MEMORY I/F) 2/5	PV

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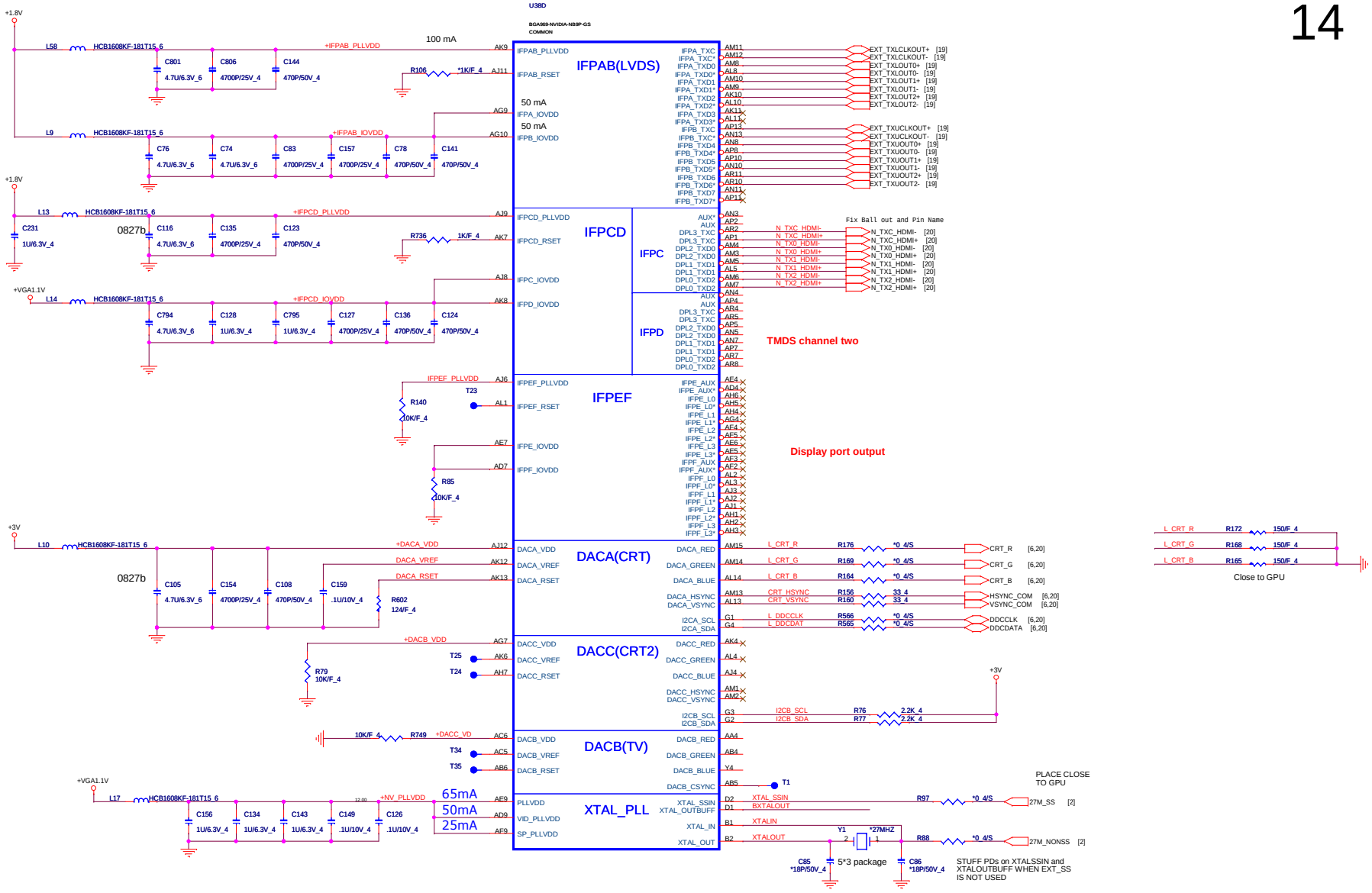

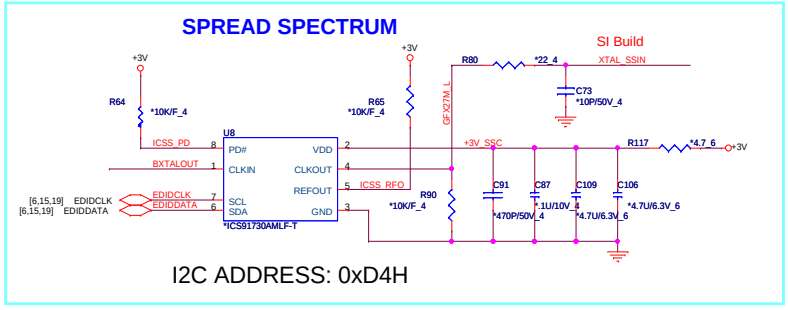

Install it when not connected to Spread spectrum device

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size: Custom	Document Number: NV9X (DISPLAY) 3/5	Rev: PV
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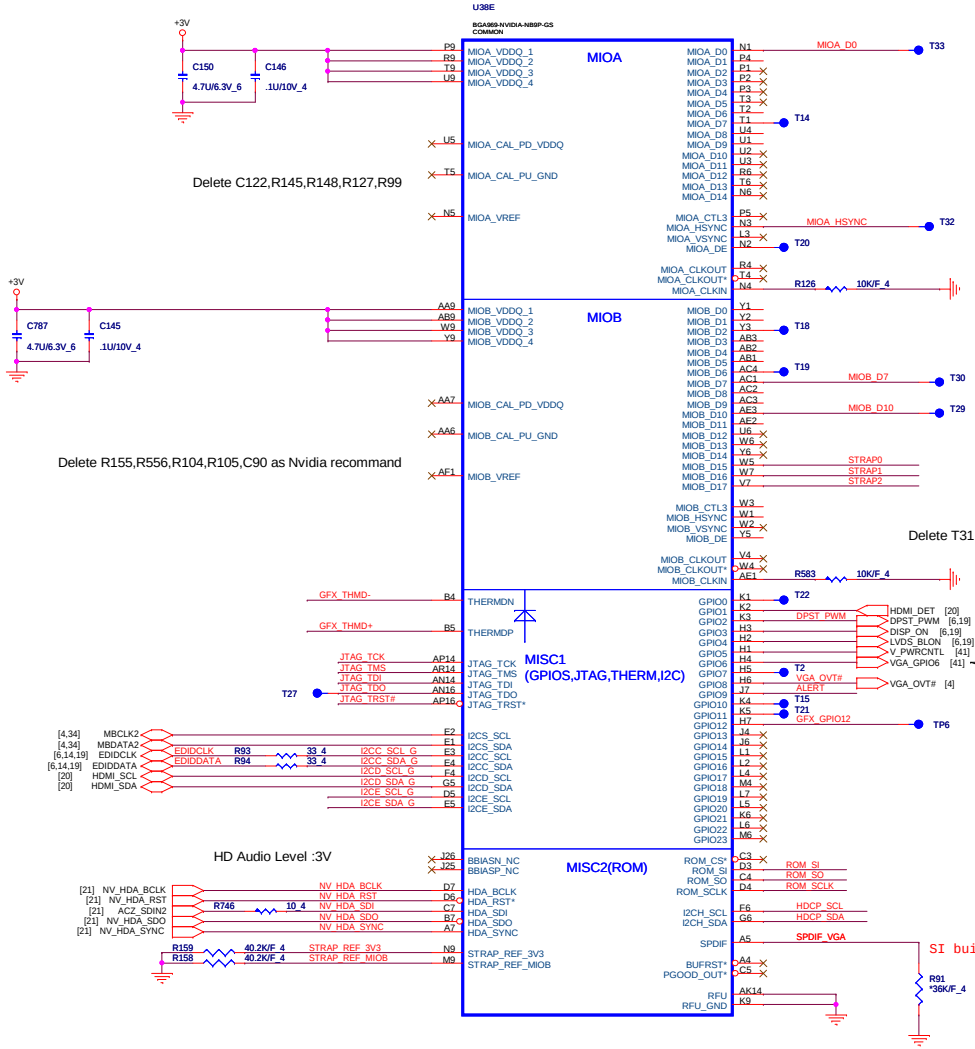
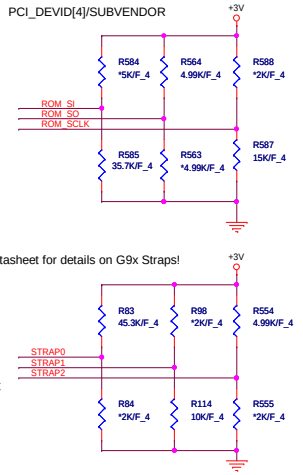


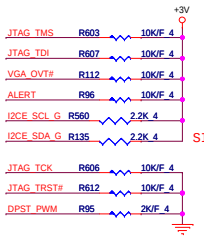
NB9P-GS (G96) Straps
NB9M-GE (G98) Straps
GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	PRIMARY DVI HOTPLUG
1	IN	N/A	SECONDARY DVI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	FBVDD VID0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	AC DETECT
13	OUT	LOW	PS CONTROL OR HDMI_CEC
14	OUT	HIGH	PS CONTROL



Logical Strap Bit Mapping

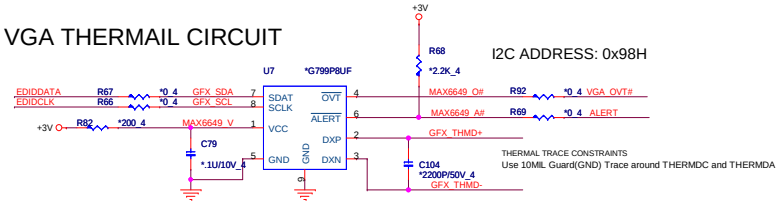
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



	Logical	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_277	TVMODE2]	TVMODE[1]	TVMODE[0]	1000
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM100	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VGA THERMAIL CIRCUIT

I2C ADDRESS: 0x98H



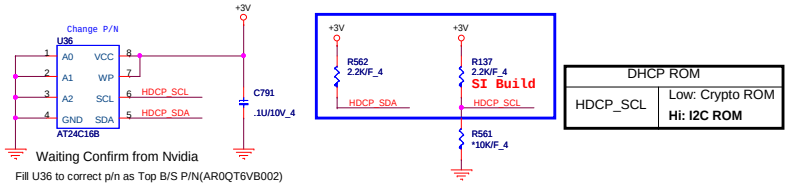
NB9X VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor	
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix	HY5PS121621CFP-25
0110	DDR2 32Mx16x8, 128bit, 512MB	Qimonda	HYB18T512161B2F-25
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung	K4N51163QE-ZC25
other	Reserved		
0000	DDR2 64Mx16x4, 128bit, 512MB	Hynix	HY5PS1G1631CFR-25
0001	DDR2 64Mx16x4, 128bit, 512MB	Samsung	K4N1G164QQ-HC25

HDCP ROM

PV-2

Change R562 and R137 from 10k to 2.2k as Nvidia request



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

PCI_DEVID: STRAP2 R554

NB9M-GE	0x06E	8	1000	PU	5K
NB9M-GS	0x06E	9	1001	PU	10K
NB9P-GE2	0x064	8	1000	PU	5K
NB9P-GS	0x064	9	1001	PU	10K

CS33012FB18 RES CHIP 30.1K 1/16W +-1%(0402)
CS33572FB13 RES CHIP 35.7K 1/16W +-1%(0402)
CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)

RAM ID: ROM_SI R585

32M*16	SAM	0101	PD	30.1K
	QIM	0110	PD	35.7K
	HYN	0111	PD	45.3K
64M*16	HYN	0000	PD	5K
	SAM	0001	PD	10K

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
C	NV9X (GPIO & STRRAPS) 4/5	PV

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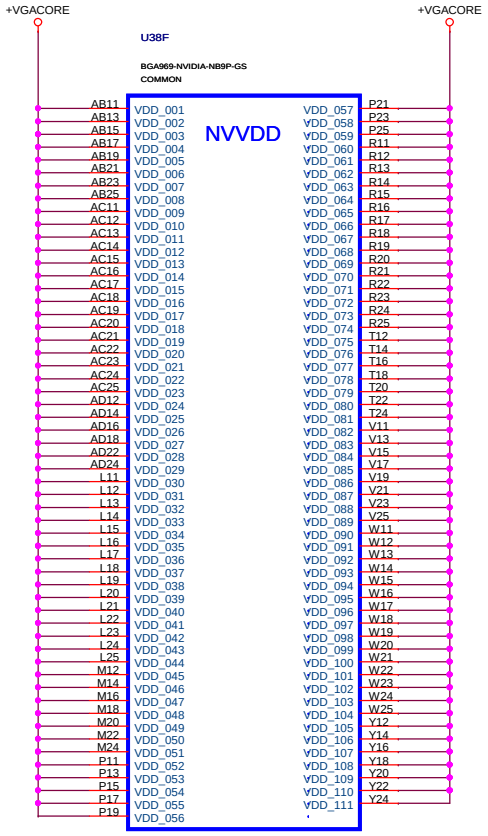
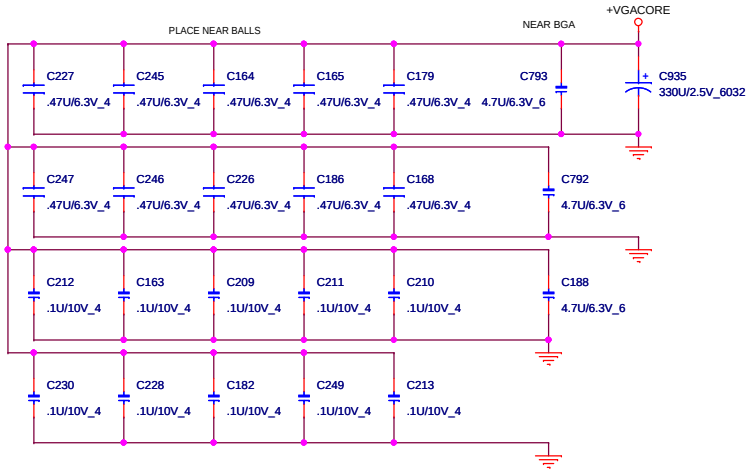
NB5

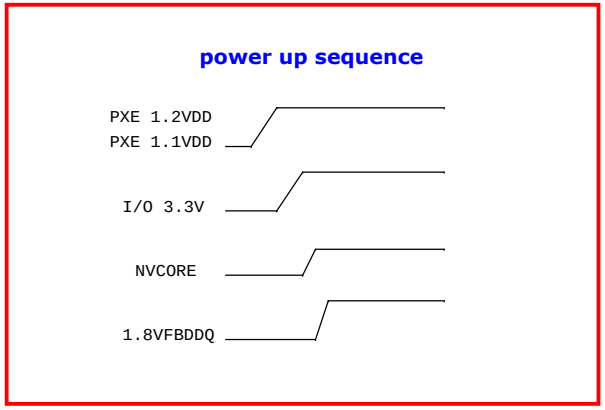
NVVDD Decoupling

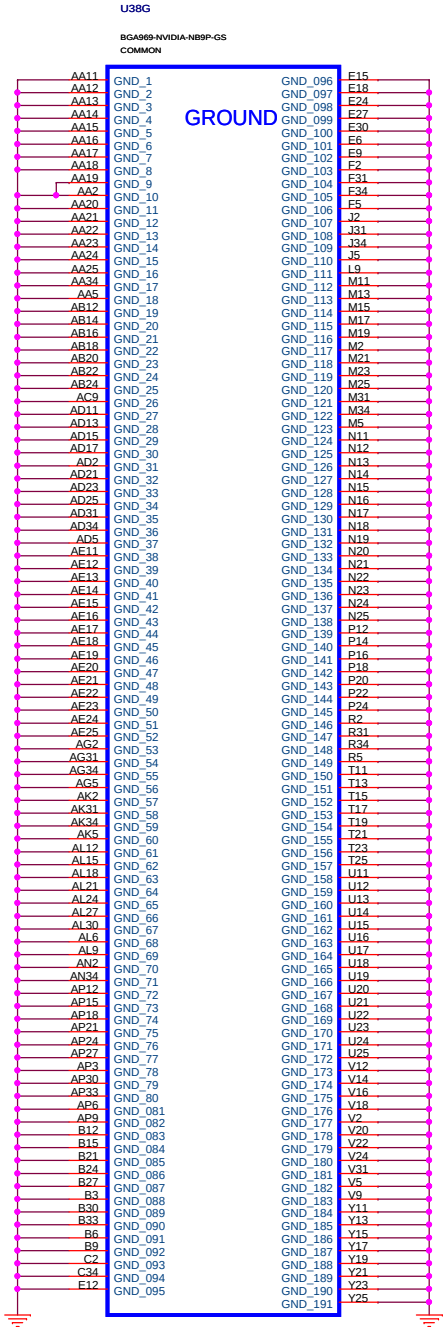




Follow Design Guide DG-03276-001 4.7uFx3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V





PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV9X (POWER & GND) 5/5	PV

NB5

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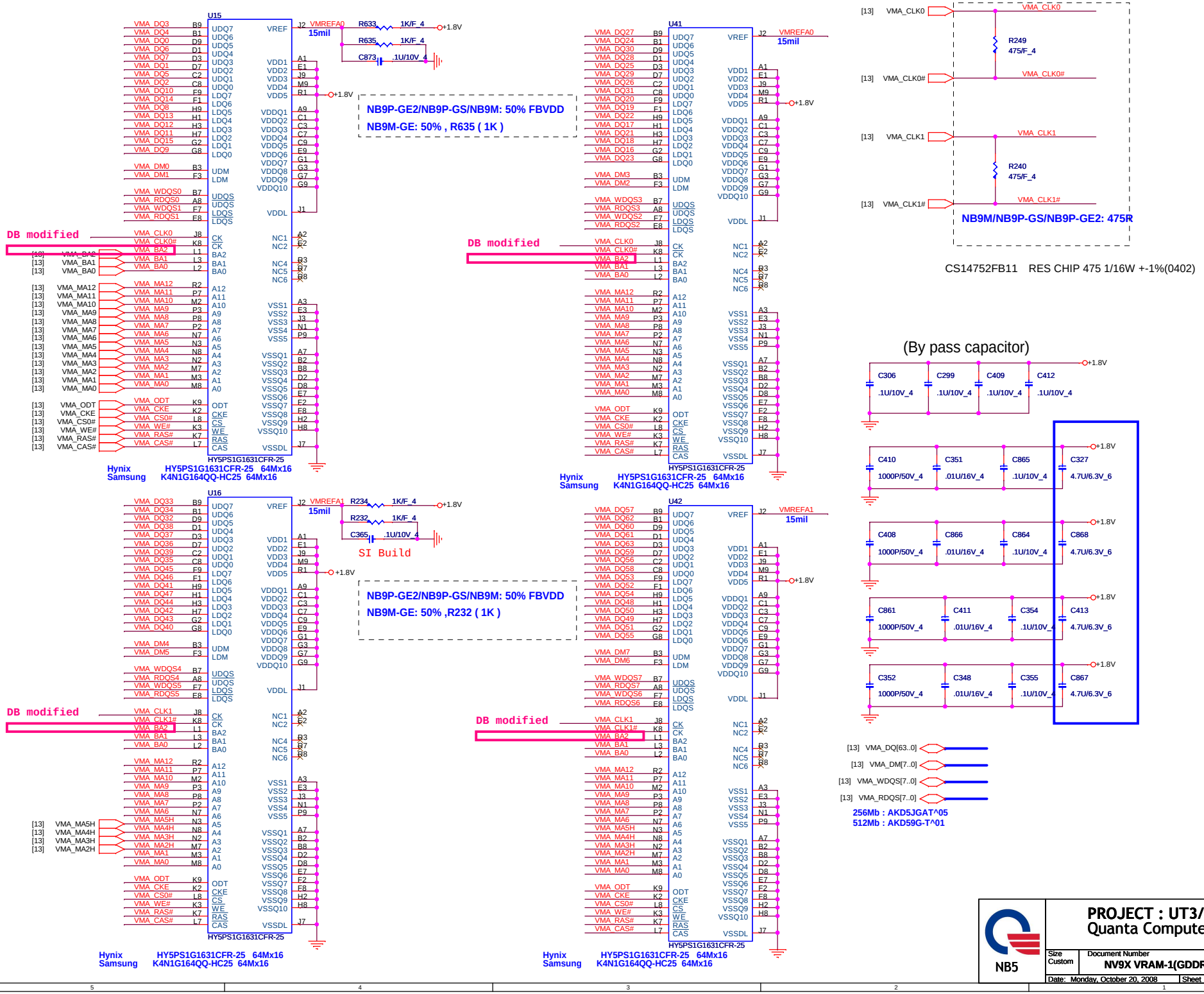

PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	NV9X VRAM-1(GDDR2 BGA84)	PV

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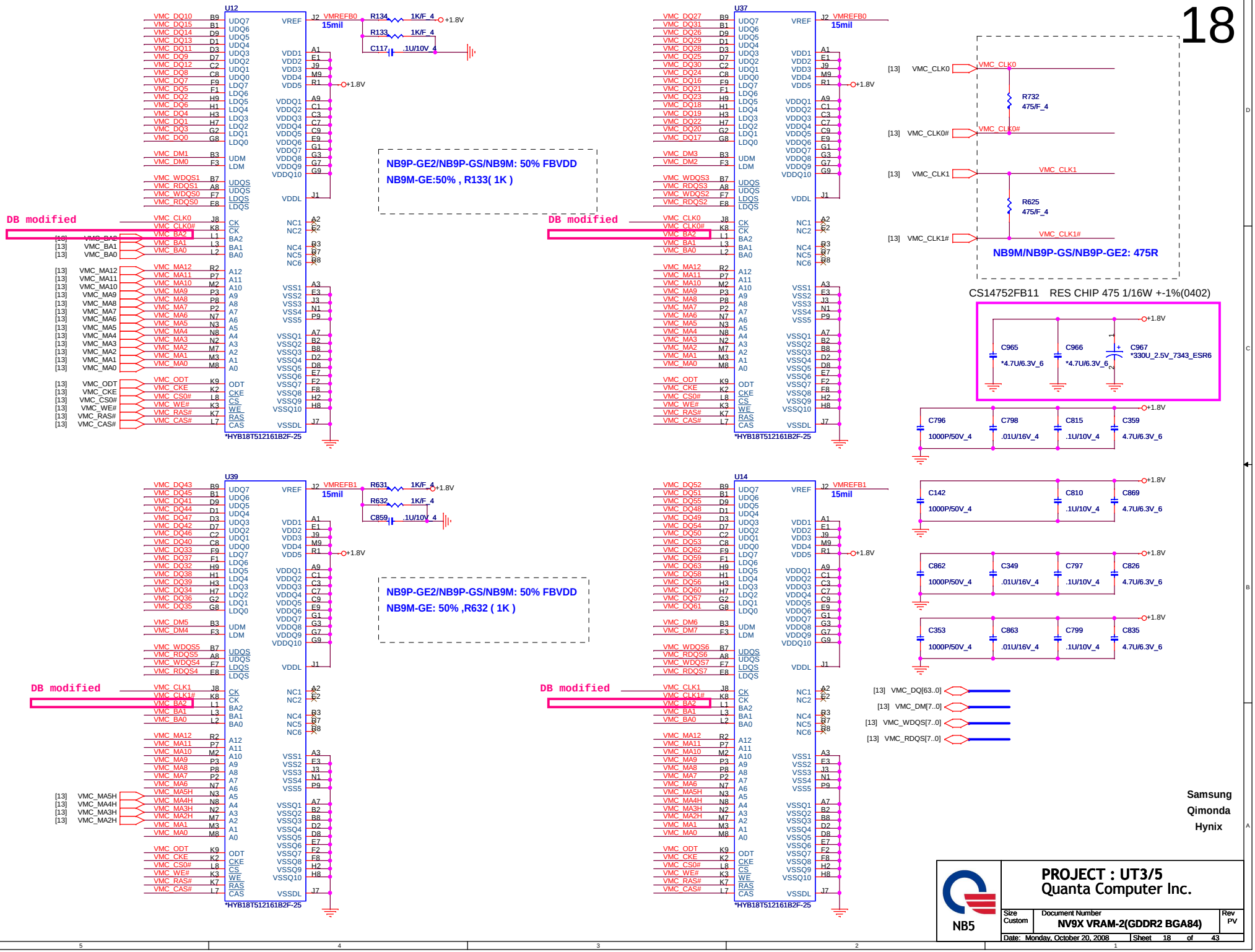

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
	Size: Custom Document Number: NV9X VRAM-2(GDDR2 BGA84)	Rev: PV
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1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

[6]	LA_CLK+	RP9	3	4	*4P2R-S-0	TXLCLKOUT+
[6]	LA_CLK#		1	2		TXLCLKOUT-
[6]	LA_DATAP0	RP1	1	2	*4P2R-S-0	TXLOUT0+
[6]	LA_DATAN0		3	4		TXLOUT0-
[6]	LA_DATAP1	RP4	1	2	*4P2R-S-0	TXLOUT1+
[6]	LA_DATAN1		3	4		TXLOUT1-
[6]	LA_DATAP2	RP7	3	4	*4P2R-S-0	TXLOUT2+
[6]	LA_DATAN2		1	2		TXLOUT2-
[6]	LB_CLK#	RP20	1	2	*4P2R-S-0	TXUCLKOUT-
[6]	LB_CLK		3	4		TXUCLKOUT+
[6]	LB_DATAP0	RP11	3	4	*4P2R-S-0	TXUOUT0+
[6]	LB_DATAN0		1	2		TXUOUT0-
[6]	LB_DATAP1	RP15	3	4	*4P2R-S-0	TXUOUT1+
[6]	LB_DATAN1		1	2		TXUOUT1-
[6]	LB_DATAN2	RP23	1	2	*4P2R-S-0	TXUOUT2-
[6]	LB_DATAP2		3	4		TXUOUT2+

OPTION SIGNAL FROM Nvidia to VGA

[14]	EXT_TXLCLKOUT+	RP8	1	2	*0_4P2R/S	TXLCLKOUT+
[14]	EXT_TXLCLKOUT-		3	4		TXLCLKOUT-
[14]	EXT_TXLOUT0-	RP2	1	2	*0_4P2R/S	TXLOUT0-
[14]	EXT_TXLOUT0+		3	4		TXLOUT0+
[14]	EXT_TXLOUT1+	RP3	3	4	*0_4P2R/S	TXLOUT1+
[14]	EXT_TXLOUT1-		1	2		TXLOUT1-
[14]	EXT_TXLOUT2+	RP6	1	2	*0_4P2R/S	TXLOUT2+
[14]	EXT_TXLOUT2-		3	4		TXLOUT2-
[14]	EXT_TXUCLKOUT+	RP19	1	2	*0_4P2R/S	TXUCLKOUT+
[14]	EXT_TXUCLKOUT-		3	4		TXUCLKOUT-
[14]	EXT_TXUOUT0+	RP10	1	2	*0_4P2R/S	TXUOUT0+
[14]	EXT_TXUOUT0-		3	4		TXUOUT0-
[14]	EXT_TXUOUT1-	RP14	3	4	*0_4P2R/S	TXUOUT1-
[14]	EXT_TXUOUT1+		1	2		TXUOUT1+
[14]	EXT_TXUOUT2-	RP22	3	4	*0_4P2R/S	TXUOUT2-
[14]	EXT_TXUOUT2+		1	2		TXUOUT2+

+3V — R520 2.2K_4 EDIDCLK
R522 2.2K_4 EDIDDATA

+VIN — L53 FBM2125 HM330-T — +VIN_BLIGHT
C753 .1U/50V_6 | C751 .01U/50V_4 | C750 .1U/50V_6 | C6 *10U/25V_12

0090 use 100 ohm and must change back to 75ohm

[2,4,6,9,10,11,12,14,15,20,21,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[3,20,24,26,27,29,32,33,36,43] +5V
[28,36,37,38,39,40,41,42,43] +VIN
[21,29,33,34,36,37,38,43] +3VPCU
[29,33,38,43] +12VALW

+3VLCD_CON — C9 1000P/50V_4 — +3V
[6,14,15] EDIDCLK
[6,14,15] EDIDDATA

CN1 GS12401-1011-9F

TXLOUT0- / TXLOUT0+
TXLOUT1- / TXLOUT1+
TXLOUT2- / TXLOUT2+
TXLCLKOUT- / TXLCLKOUT+
TXUOUT0- / TXUOUT0+
TXUOUT1- / TXUOUT1+
TXUOUT2- / TXUOUT2+
TXUCLKOUT- / TXUCLKOUT+
VADJ1
BLON_CON
+VIN_BLIGHT
+LOGO_PWR1

PV MODIFY

+5V — R12 75R/F_6 — +LOGO_PWR1
C758 1000P/50V_4

[6,15] DPST_PWM — R526 *0_4
[34] PWM_VADJ — R524 *0_4/S — VADJ1
C754 *4.7U/6.3V_6 | C756 .1U/10V_4

PN_BLON — D1 RB501V-40 — BLON_CON
R4 100K/F_4 | C8 22P/50V_4

+3VPCU — R8 33K_6 — D2 RB501V-40
[6,15] LVDS_BLON — R6 1K/F_4 — LID_EC# [33,34]
[23] LCD_BK — Q2 DTC144EUA

Close to EC

DISP_ON R525 100K/F_4
LVDS_BLON R7 100K/F_4

+5VSUS — R527 100K/F_4
14.5v
+12VALW — R10 330K_6
AO3404 ID current 5.8A
Q1 AO3404
LCDONG
+3V — C12 .1U/10V_4
+3VLCD
L52 PBY201209T-4A/08
R516 22_8
LCDDISCHG
+3VLCD_CON
C757 .01U/16V_4 | C746 .1U/10V_4 | C748 10U/6.3V_8
Q26 ME2N7002E
C759 .022U/16V_4
LCDON#
Q25 DTC144EUA
[6,15] DISP_ON
Q27 ME2N7002E

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
B	LCD CONN/Lid function	PV

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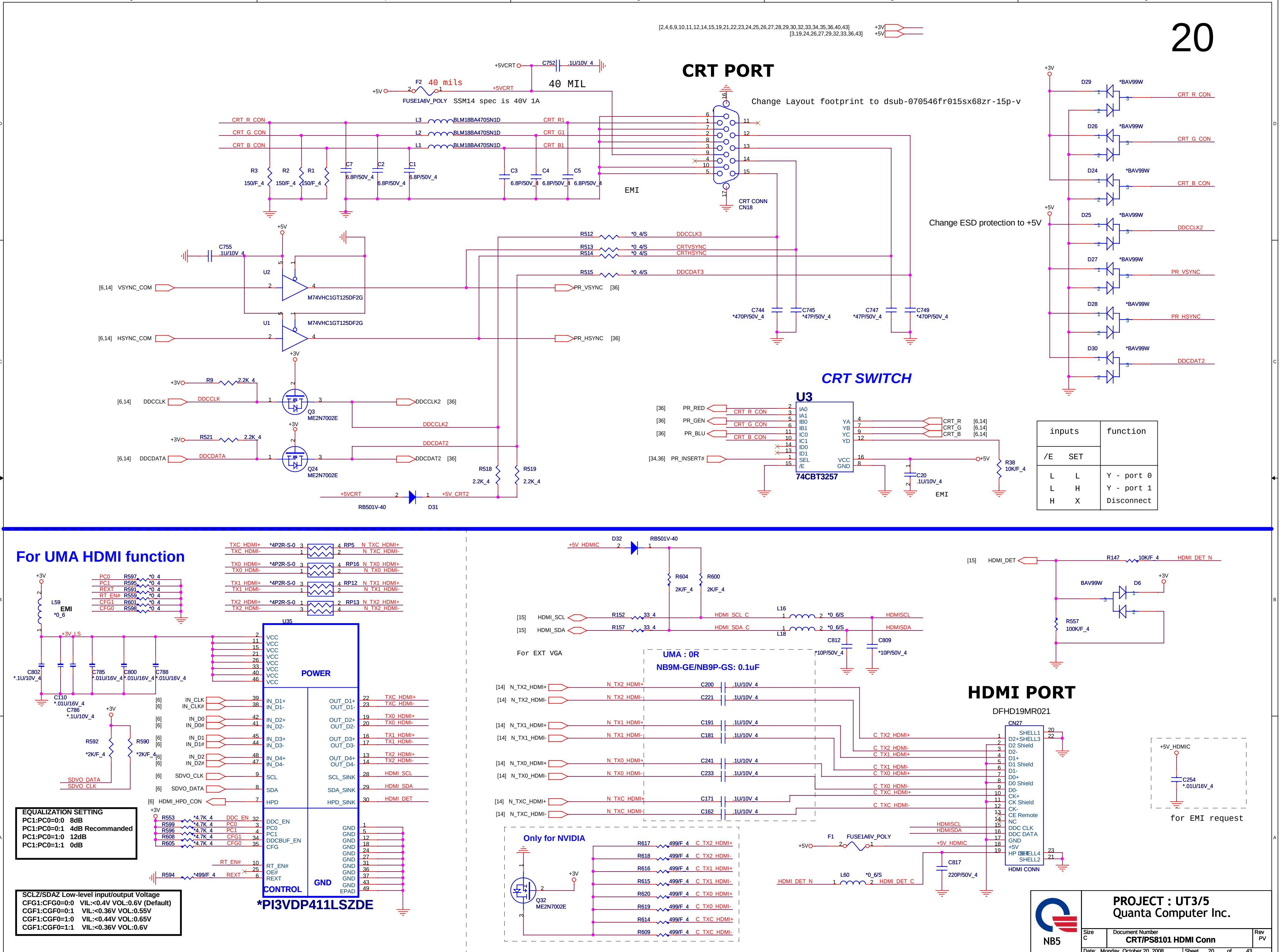

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

NB5
PROJECT : UT3/5
Quanta Computer Inc.

Size: C | Document Number: CRT/PS8101 HDMI Conn | Rev: PV

[19,29,33,34,36,37,38,43] +3VPCU
[24] +3VRTC
[2,4,6,9,10,11,12,14,15,19,20,22,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[4,9,22,24,26,32,33,35,39,43] +1.5V
[2,3,4,5,6,8,9,24,33,39,40] +1.05V
[22,23,24,32,43] +3VS5

SI build
RB500V-40 D19
RB500V-40 D20
SI build
+3VPCU
+3VRTC
+3VRTC_2
C905 1U/6.3V_4
R375 20K/F_4
R378 180K_4
C599 1U/6.3V_4
G3 *SHORT_PAD1
C624 .1U/10V_4
G4 *SHORT_PAD1
C908 15P/50V_4
Y7 32.768KHZ
C909 15P/50V_4
R335 10M_4
R393 1K/F_4
R346 1M/F_4
20MIL
+3VRTC_BAT
For CR2032(Large)
BT1 BAT_CONN
update footprint (0830)
+3V
C569 .1U/10V_4
R409 10K/F_4
[29] SATA_LED#
U26 MC74VHC1G08DFT2G
ICH_SATA_LED#
+1.5V
R320 24.9/F_4
GLAN_COMP
Notice: GPIO33 is also a strap pin. Don't pull it to high.
HP Request
BT_COMBO_EN#
R381 *1K/F_4
[35] BT_COMBO_EN#
TP87

U45A

RTC_X1 C23 RTCX1
RTC_X2 C24 RTCX2
RTC_RST# A25 RTCRST#
SRTC_RST F20 SRTCRST#
SM_INTRUDER# C22 INTRUDER#
ICH_INTVRMEN B22 INTVRMEN
LAN100_SLP A22 LAN100_SLP
GLAN_CLK E25 GLAN_CLK
LAN_RSTSYNC C13 LAN_RSTSYNC
LAN_RXD0 F14 LAN_RXD0
LAN_RXD1 G13 LAN_RXD1
LAN_RXD2 D14 LAN_RXD2
LAN_TXD0 D13 LAN_TXD0
LAN_TXD1 D12 LAN_TXD1
LAN_TXD2 E13 LAN_TXD2
GPIO56 B10 GPIO56
GLAN_COMPI B28
GLAN_COMPO B27
ACZ_BCLK AE6 HDA_BIT_CLK
ACZ_SYNC AH4 HDA_SYNC
ACZ_RST# AE7 HDA_RST#
[26] ACZ_SDIN0 AF4 HDA_SDIN0
[33] ACZ_SDIN1 AG4 HDA_SDIN1
[15] ACZ_SDIN2 AH3 HDA_SDIN2
[6] ACZ_SDIN3 AE5 HDA_SDIN3
ACZ_SDOUT AG5 HDA_SDOUT
AG7 HDA_DOCK_EN#/GPIO33
AE8 HDA_DOCK_RST#/GPIO34
ICH_SATA_LED# AG8 SATALED#
SATA0RXN AJ16
SATA0RXP AH16
SATA0TXN AF17
SATA0TXP AG17
SATA1RXN AH13
SATA1RXP AJ13
SATA1TXN AG14
SATA1TXP AF14
ICH9BM_SLB8Q

RTC LPC
LAN / GLAN CPU
IHDA
SATA

FWH0/LAD0 K5 LAD0 [34,35]
FWH1/LAD1 K4 LAD1 [34,35]
FWH2/LAD2 L6 LAD2 [34,35]
FWH3/LAD3 K2 LAD3 [34,35]
FWH4/LFRAME# K3 LFRAME# [34,35]
LDRQ0# J3 ICH_DRQ#0 TP60
LDRQ1#/GPIO23 J1 ICH_DRQ#1 TP80
R382 10K/F_4 +3V
A20GATE N7 GATEA20 [34]
A20M# AJ27 H_A20M# [3]
DPRSTP# AJ25 H_DPRSTP# [3,6,40]
DPSLP# AE23 H_DPSLP# [3]
FERR# AJ26 R330 49.9/F_4 H_FERR# [3]
CPUPWRGD AD22 H_PWRGD [3]
IGNNE# AF25 H_IGNNE# [3]
INIT# AE22 H_INIT# [3]
INTR AG25 H_INTR [3]
RCIN# L3 RCIN# [34]
R421 10K/F_4 +3V
NMI AF23 H_NMI [3]
SMI# AF24 H_SMI# [3]
STPCLK# AH27 H_STPCLK# [3]
THRMTRIP# AG26 H_THERMTRIP_R R326 49.9/F_4 PM_THRMTRIP# [3,6]
TP12 AG27 ICH_TP12 TP71
SATA4RXN AH11 SATA_RXN4_C C940 *.01U/16V_4 SATA_RXN4 [32]
SATA4RXP AJ11 SATA_RXP4_C C937 *.01U/16V_4 SATA_RXP4 [32]
SATA4TXN AG12 SATA_TXN4_C C939 *.01U/16V_4 SATA_TXN4 [32]
SATA4TXP AF12 SATA_TXP4_C C938 *.01U/16V_4 SATA_TXP4 [32]
SATA5RXN AH9 SATA_RXN5_C C611 .01U/16V_4 SATA_RXN5 [29]
SATA5RXP AJ9 SATA_RXP5_C C606 .01U/16V_4 SATA_RXP5 [29]
SATA5TXN AE10 SATA_TXN5_C C614 .01U/16V_4 SATA_TXN5 [29]
SATA5TXP AF10 SATA_TXP5_C C623 .01U/16V_4 SATA_TXP5 [29]
SATA_CLKN AH18 CLK_PCIE_SATA# [2]
SATA_CLKP AJ18 CLK_PCIE_SATA [2]
SATARBIAS# AJ7 SATA_RBIAS_PN
SATARBIAS AH7
R396 24.9/F_4

+1.05V
R329 *56.2/F_4
R337 *56.2/F_4
R331 49.9/F_4
R330 49.9/F_4
R327 49.9/F_4
Change R331,R327 to 49.9 ohm

For UT5 17" 2nd HDD only
SATA HDD2
DB modified
E-SATA CONNECT

SATA HDD1
[32] SATA_RXN0 C583 .01U/16V_4 SATA_RXN0_C
[32] SATA_RXP0 C579 .01U/16V_4 SATA_RXP0_C
[32] SATA_TXN0 C576 .01U/16V_4 SATA_TXN0_C
[32] SATA_TXP0 C578 .01U/16V_4 SATA_TXP0_C
SATA ODD
[32] SATA_RXN1 C590 .01U/16V_4 SATA_RXN1_C
[32] SATA_RXP1 C592 .01U/16V_4 SATA_RXP1_C
[32] SATA_TXN1 C588 .01U/16V_4 SATA_TXN1_C
[32] SATA_TXP1 C584 .01U/16V_4 SATA_TXP1_C

For HD Audio
ACZ_RST# R388 33_4 ACZ_RST#_AUDIO [26]
ACZ_SDOUT R404 33_4 ACZ_SDOUT_AUDIO [26]
ACZ_SYNC R400 33_4 ACZ_SYNC_AUDIO [26]
ACZ_BCLK R390 33_4 BIT_CLK_AUDIO [26]
C622 C632 C633 *10P/50V_4

For MDC
ACZ_RST# R387 33_4 ACZ_RST#_MDC [33]
ACZ_SDOUT R394 33_4 ACZ_SDOUT_MDC [33]
ACZ_SYNC R406 33_4 ACZ_SYNC_MDC [33]
ACZ_BCLK R398 33_4 BIT_CLK_MDC [33]
C635 C656 C657 *10P/50V_4

For UMA
ACZ_RST# R389 *33_4 ACZ_RST#_MCH [6]
ACZ_SDOUT R376 *33_4 ACZ_SDOUT_MCH [6]
ACZ_SYNC R377 *33_4 ACZ_SYNC_MCH [6]
ACZ_BCLK R395 *33_4 ACZ_BITCLK_MCH [6]
C631 C602 C601 *10P/50V_4

Close to U45
For Discrete
ACZ_RST# R745 22_4 NV_HDA_RST
ACZ_SDOUT R747 22_4 NV_HDA_SDO
ACZ_SYNC R748 22_4 NV_HDA_SYNC
ACZ_BCLK R744 22_4 NV_HDA_BCLK
NV_HDA_RST [15]
NV_HDA_SDO [15]
NV_HDA_SYNC [15]
NV_HDA_BCLK [15]
C691 C605 C693 *10P/50V_4

SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

+3VRTC R677 332K/F_4 ICH_INTVRMEN R674 *0_4
+3VRTC R679 332K/F_4 LAN100_SLP R678 *0_4
+3V R399 *1K/F_4 ACZ_SDOUT ICH_TP3 [23] R681 *1K/F_4

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)

*1K/F_4 R392 GNT0# [22]

A16 swap override strap	
PCI_GNT#3	Low = A16 swap override enabled Hi = Default

*1K/F_4 R391 GNT3# [22]

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

+3V R384 *1K/F_4 ACZ_SPKR [23,26,27]

TPM physical presence	
ICH_GPIO57	Low: Default

+3VS5 R704 *10K/F_4 ICH_GPIO57 [23] R706 100K/F_4

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M Host 1/4	PV

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SWAP PCIE PORT6 to PORT2 (Lan and New card swap) -->Rename the port name by function and port

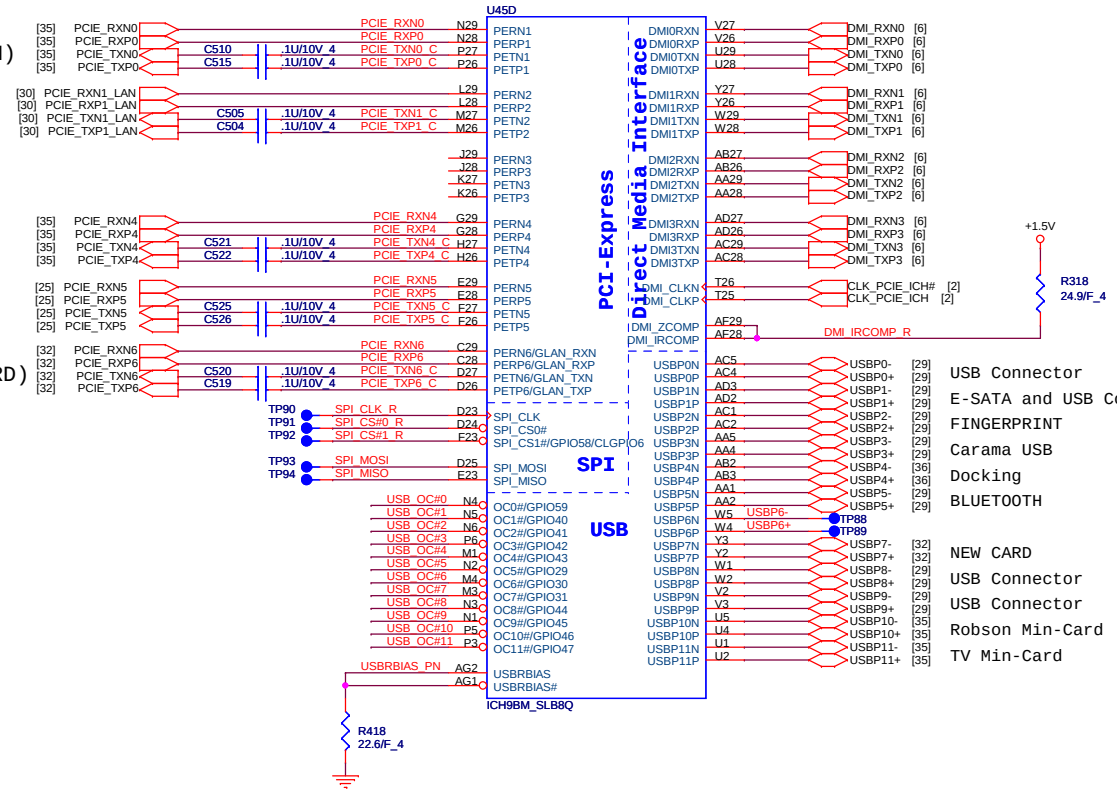
[4,9,21,24,26,32,33,35,39,43] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[23,29,35,39,40,41,43] +3VSUS

MINI CARD PCI-E(WLAN)

PCIE-LAN

TV CARD PCI-E

EXPRESS CARD (NEW CARD)



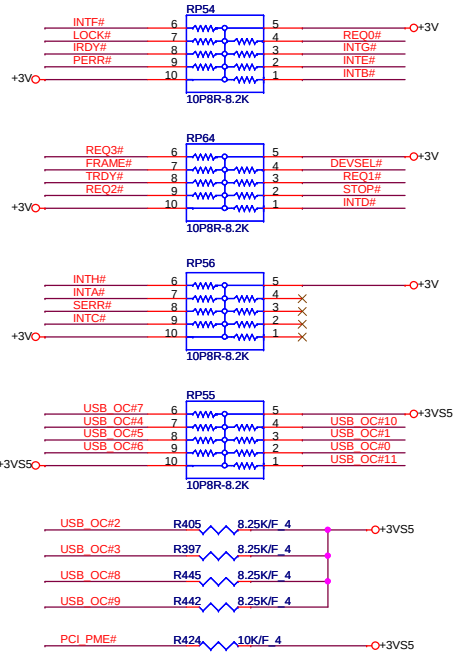
USB Connector
E-SATA and USB Connector
FINGERPRINT
Carama USB
Docking
BLUETOOTH

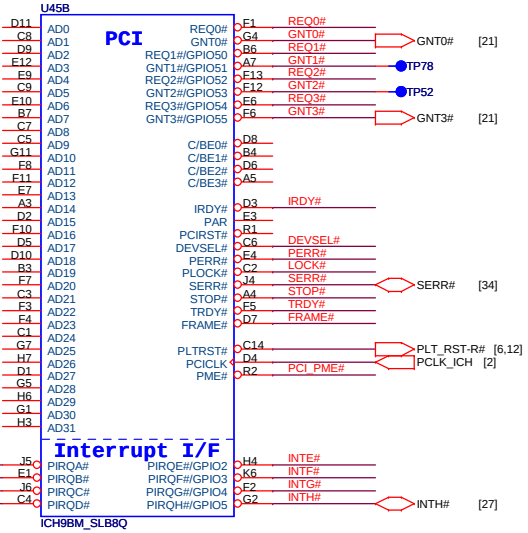
NEW CARD
USB Connector
USB Connector
Robson Min-Card
TV Min-Card

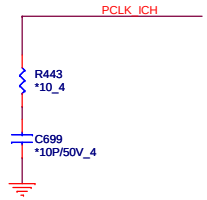
SI-2 Delete
Delete RP53,RP57 and tied from SB to CR(USB6)

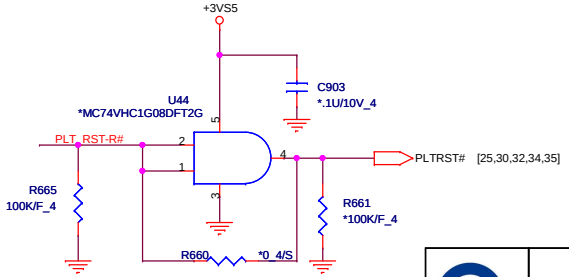
des

int

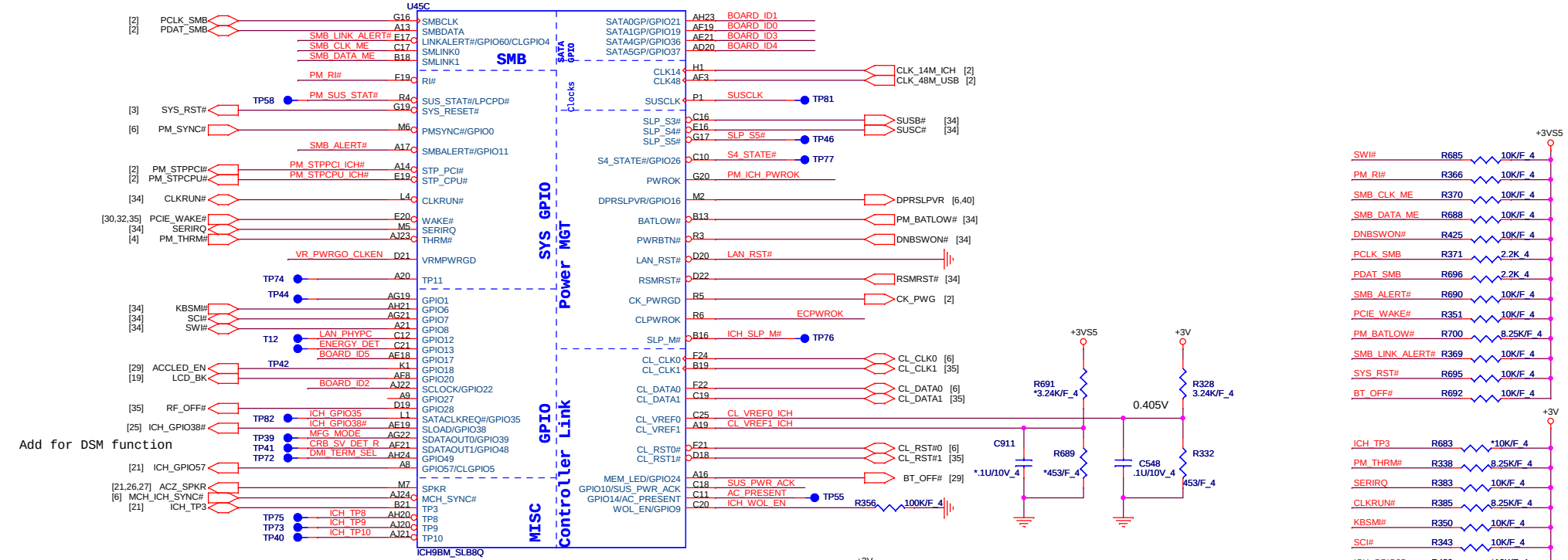




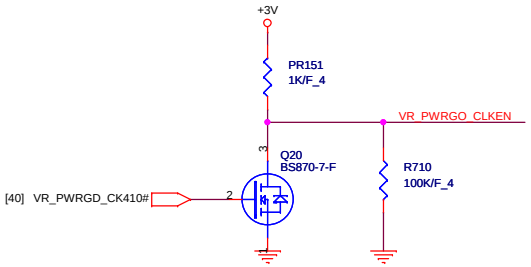


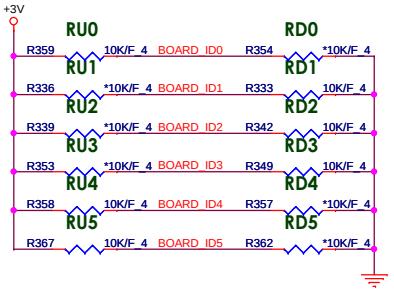


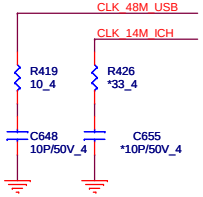
[4,9,21,22,24,26,32,33,35,39,43] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,32,33,34,35,36,40,43] +3V
[21,22,24,32,43] +3VS5
[29,35,39,40,41,43] +3VSUS

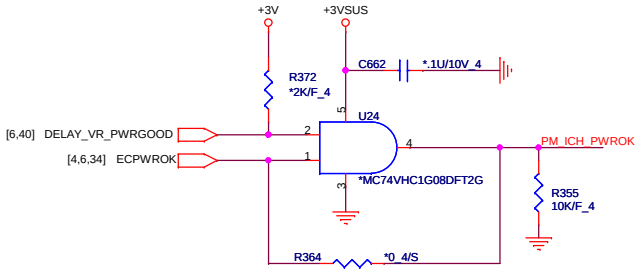


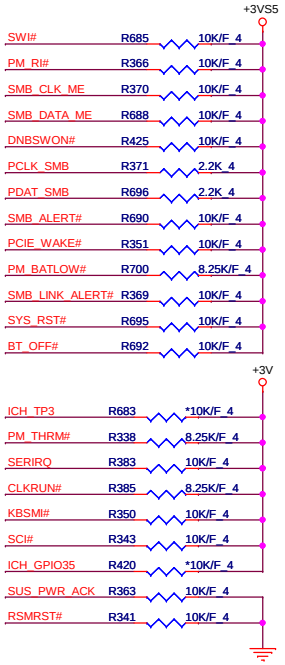
Add for DSM function











Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/Dis./9M	RD0 (0)	RU1 (1)	RD2 (0)	NC	NC	RD5 (0)
UT3/UMA	RD0 (0)	RD1 (0)	NC	NC	NC	NC
UT5/Dis./M92	RU0 (1)	RU1 (1)	RD2 (0)	NC	NC	RU5 (1)
UT5/Dis./M96	RU0 (1)	RU1 (1)	RU2 (1)	NC	NC	RD5 (0)
UT5/UMA	RU0 (1)	RD1 (0)	NC	NC	NC	NC
UT3D/Dis./M92	RD0 (0)	RU1 (1)	RD2 (0)	NC	NC	RU5 (1)
UT3D/Dis./M96	RD0 (0)	RU1 (1)	RU2 (1)	NC	NC	RD5 (0)

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UT3/5	0=UT3 1=UT5					
UMA/Dis.		0=UMA 1=Dis.				
NV9M			0			0
ATI M92			0			1
ATI M96			1			0

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M GPIO 3/4	PV

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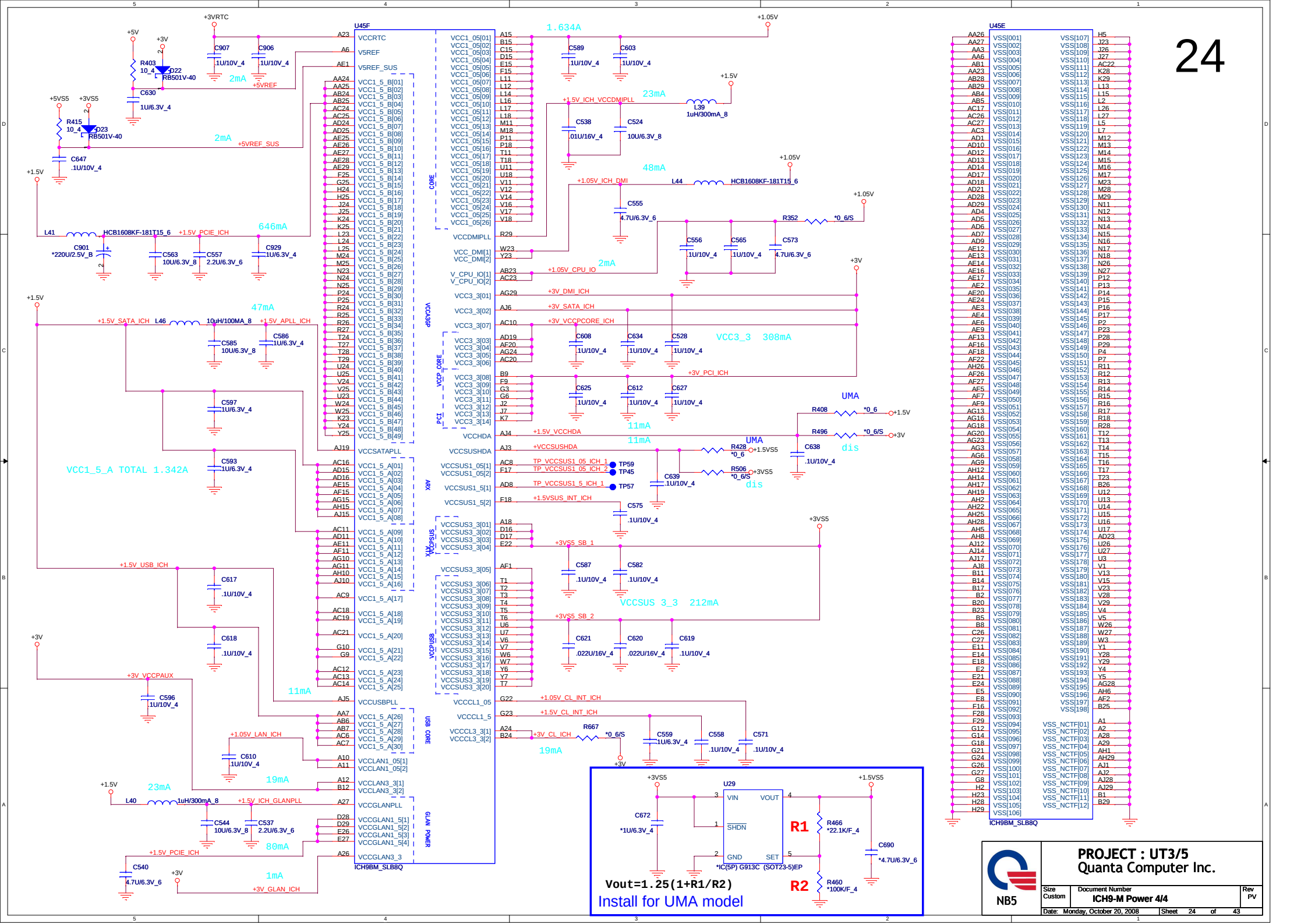
U45F
ICH9BM_SLB8Q
U45E
ICH9BM_SLB8Q
VCC1_5_A TOTAL 1.342A
VCC3_3 308mA
VCCSUS 3_3 212mA
1.634A
23mA
48mA
2mA
646mA
47mA
11mA
19mA
80mA
1mA
UMA
dis
U29
*IC(5P) G913C (SOT23-5)EP
Vout=1.25(1+R1/R2)
Install for UMA model
PROJECT : UT3/5
Quanta Computer Inc.
NB5
ICH9-M Power 4/4
Date: Monday, October 20, 2008
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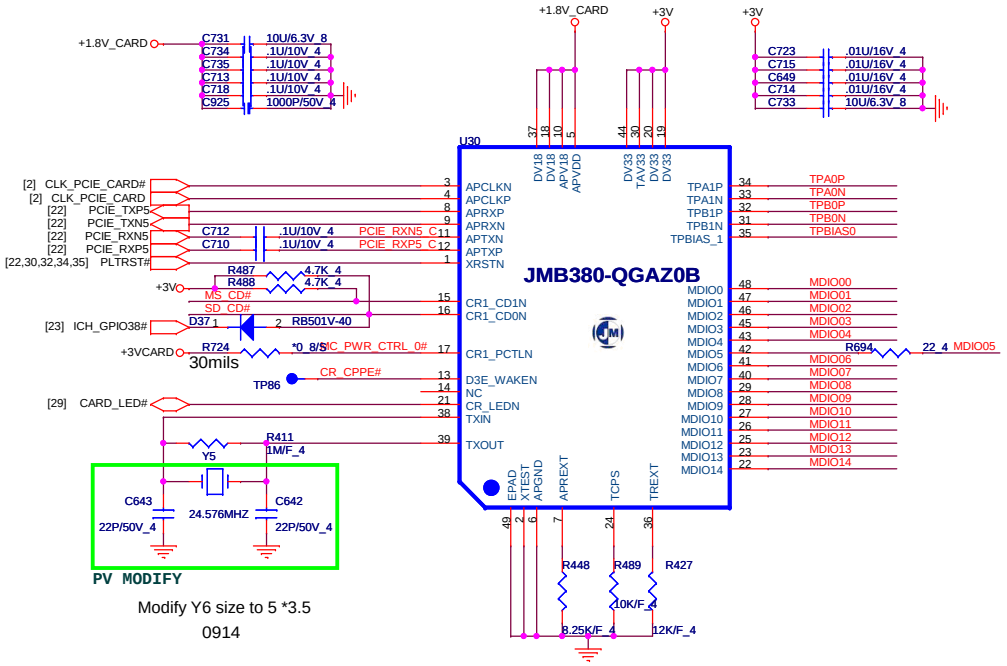
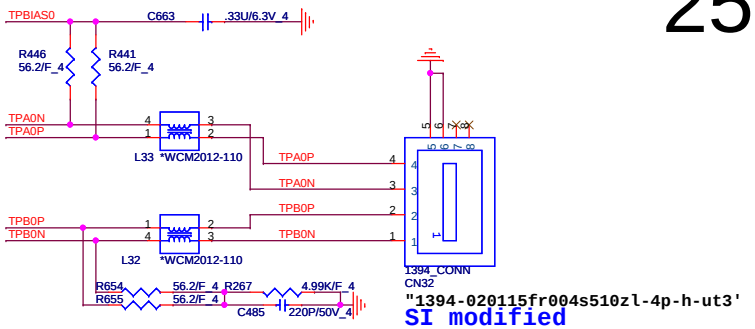
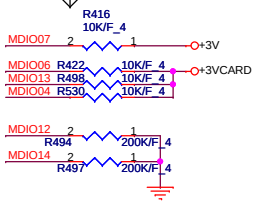




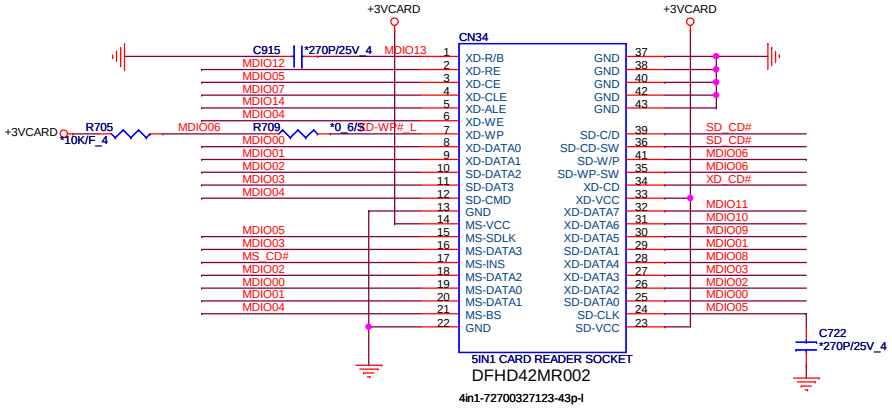
Change to 10K

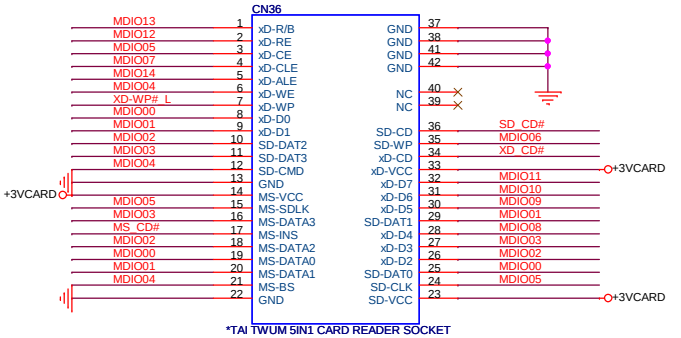


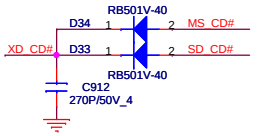
JMB 380 Note:

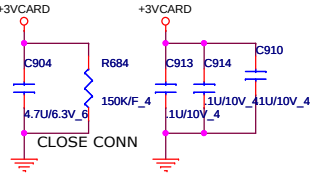
SD/MMC	MS	XD
MDID0	SD_DAT0	MS_D0	XD_D0
MDID1	SD_DAT1	MS_D1	XD_D1
MDID2	SD_DAT2	MS_D2	XD_D2
MDID3	SD_DAT3	MS_D3	XD_D3
MDID4	SD_CMD	MS_BS	XD_WE#
MDID5	SD_CLK	MS_SCLK	XD_CE#
MDID6	SD_WP		XD_WP#
MDID7			XD_CLE
MDID8	SD_DAT4		XD_D4
MDID9	SD_DAT5		XD_D5
MDID10	SD_DAT6		XD_D6
MDID11	SD_DAT7		XD_D7
MDID12			XD_RE#
MDID13			XD_R/B#
MDID14			XD_ALE
CR1_LEDN	SD1_LED#	MS1_LED#	XD_LED#
CR1_PCTLN	SD1_PCTL#	MS1_PCTL#	XD1_PCTL#
CR1_CD0	SD1_CD#		XD_CV#
CR1_CD1		MS1_CD#	XD_CD#

5 IN1 CARD READER
XD,MMC/SD,MS/MSP









NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5158 & CR SOCKET &HOLE	PV

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SI MODIFY

+3V_DVDD R571 *0_4 DVDD_LV

DB MODIFY

UMA +3V_1.5V_DVIO

+1.5V R454 *0_4
+3V_DVDD R517 *0_4/S
Dis
C688 1U/10V_4

+3V_DVDD C695 1U/10V_4, C685 1U/6.3V_4, C716 10U/6.3V_8, DVDD_LV
+4.75VAVDD C721 1U/10V_4, C738 1U/6.3V_4, C770 1U/6.3V_4, C737 .1U/10V_4
Close to Pin38
AGND

+3V_DVDD Close to Pin9
+3V
C684 1U/6.3V_4
C671 1U/10V_4
C669 10U/6.3V_8

U32

Digital

[21] ACZ_SDOUT_AUDIO
[21] BIT_CLK_AUDIO
[21] ACZ_SDIN0
[21] ACZ_SYNC_AUDIO
[21] ACZ_RST#_AUDIO
ADC_BITCLK
R452 22_4 ACZ_SDIN0_ADC
SDO
BITCLK
SDI_CODEC
SYNC
RESET#
DVDD_IO
DVDD_CORE

[29] DIGITAL_D1
[27] HP_EAPD
C762 10P/50V_4
R471 *0_6/S
VOL_UP/DMIC_0
VOL_DN/DMIC_1

[27] IDT_GPIO3#
IDT_GPIO3#
GPIO 3

[28] SUB-MUTE#
SUB-MUTE#
GPIO 5

[36] PR_INSERT#_IDT
PR_INSERT# IDT R726 *0_4/S
JACK_SEN# R723 *0_4
GPIO 6
GPIO 7 / SPDIF OUT1
DMIC_CLK

For IDT Dolby functionality.
[29] DIGITAL_CLK
R476 22_6
C763 *10P/50V_4

[36] SPDIF
[27] EAPD#
SPDIF0
EAPD/GPIO0/SPDIF OUT 0 or 1

PAD NC NC NC NC NC/OTP DVSS AVSS2** AVSS1 VREFFILT CAP2

Analog

DVDD_LV AVDD1 AVDD2**

PORTA_L
PORTA_R
C628 47U/6.3V_3528
C629 47U/6.3V_3528
R569 60.4_4
R570 60.4_4
DOCK_LSPK+ [36]
DOCK_RSPK+ [36]

TO DOCKING Speakers

PORTB_L
PORTB_R
VREFOUT-B
MIC1_L1 C711 2.2U/6.3V_6
MIC1_R1 C719 2.2U/6.3V_6
VREFOUT_B R482 4.7K_4
R492 4.7K_4
C717 1U/6.3V_4
EXT_MIC_L
EXT_MIC_R

TO Audio Jack MIC

SI MODIFY

LINE_OUTR R572 *0_4 SUB_OUTR [28]
LINE_OUTL R573 *0_4 SUB_OUTL [28]

TO Internal Speakers and Sub Woofer EQ

PORTC_L
PORTC_R
VREFOUT-C
C736 *1U/6.3V_4

PORT-D_L
PORT-D_R
LINE_OUTL
LINE_OUTR
LINE_OUTL [27]
LINE_OUTR [27]

PORTE_L
PORTE_R
VREFOUT-E / GPIO 4
DOCK_MIC_L1 C697 2.2U/6.3V_6
DOCK_MIC_R1 C706 2.2U/6.3V_6
VREFOUT_E R499 *4.7K_4
R485 *4.7K_4
C742 *1U/6.3V_4
DOCK_MIC_L2
DOCK_MIC_R2
R463 1.21K_4
R462 10K/F_4
R474 10K/F_4
R475 1.21K_4
DOCK_MIC_L [36]
DOCK_MIC_R [36]

TO DOCKING MIC

PORTF_L
PORTF_R
HP-L
HP-R
HP-L [27]
HP-R [27]

TO Headphone jack

PCBEEP/Mono
C692 1U/10V_4
R438 47K_4
R450 10K/F_4
C675 1U/10V_4
ACZ_SPKR [21,23,27]

SENSE_A
R449 2.49K/F_4
R523 39.2K/F_4 SB_A#
R456 20K/F_4 SA_B#
C680 1000P/50V_4
+4.75VAVDD

SENSE_B
R510 2.49K/F_4
R509 39.2K/F_4 SB_E#
R457 20K/F_4 SA_F#
C740 1000P/50V_4
+4.75VAVDD

AGND

IDT 92HD75B3

DB MODIFY

C743 10U/6.3V_8
C739 1U/6.3V_4

SA_A# -->DOCK HP
SB_A# -->EXT MIC
SB_E# -->DOCK MIC
SA_F# -->EXT HP

Audio JACK: Normal Open

ADC_BITCLK
ACZ_SDIN0_ADC
C687 *27P/50V_4
C686 *27P/50V_4
FOR EMI

Reserve for EAPD#
+3V_DVDD
R479 *5.11K/F_4
EAPD#

PORT	PLACE TO
MONO_OUT	X
PORT A	Docking Speakers
PORT B	M/B MIC
PORT C	X
PORT D	Internal Speckers
PORT E	Docking MIC
PORT F	HP OUT
DM	DIGITAL MIC

R501 *0_6/S
R500 *0_6/S
R480 *0_6/S
R473 *0_6/S
R440 *0_6/S
R491 *0_6/S
R472 *0_6/S
C741 1000P/50V_4

HP_EAPD

TPA6040A4	Low enable
TPA6047A4	High enable

Codec

	92HD71	92HD75
R571	POP	NA
C716	NA	POP
R449 R510	5.11K	2.49K

5.11K P/N: CS25112FB15

TO AUDIO/B CON.

DFFC12FR293
CN17
AUDIO CONN
C707 .1U/10V_4
+5VPCU
[34,36] CIR_IN
[27] HPOUT_L
[27] HPOUT_R
HPOUT_L
HPOUT_R
SA_F#
SA_B#
EXT_MIC_L
EXT_MIC_R
C705 *180P/50V_4
C704 *180P/50V_4
C703 *27P/50V_4
C702 *27P/50V_4
AGND
EMI 0828

DOCK MIC DETECT

+5V
R538 10K/F_4
R535 10K/F_4
SB_E#
Q30 ME2N7002E
DOCK_MIC_L
R536 10K/F_4
DKMIC_SEN
Q29
Q28 MMBT3904-7-F
R537 47K_4
C779 1U/6.3V_4
MMBT3904-7-F
AGND

+5V
R568 47K_4
R556 47K_4
SB_A#
Q37 ME2N7002E
Q38
[36] JACK_SEN#
R567 10K/F_4
MMBT3904-7-F
AGND

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Quanta Computer Inc.
NB5
Size Custom
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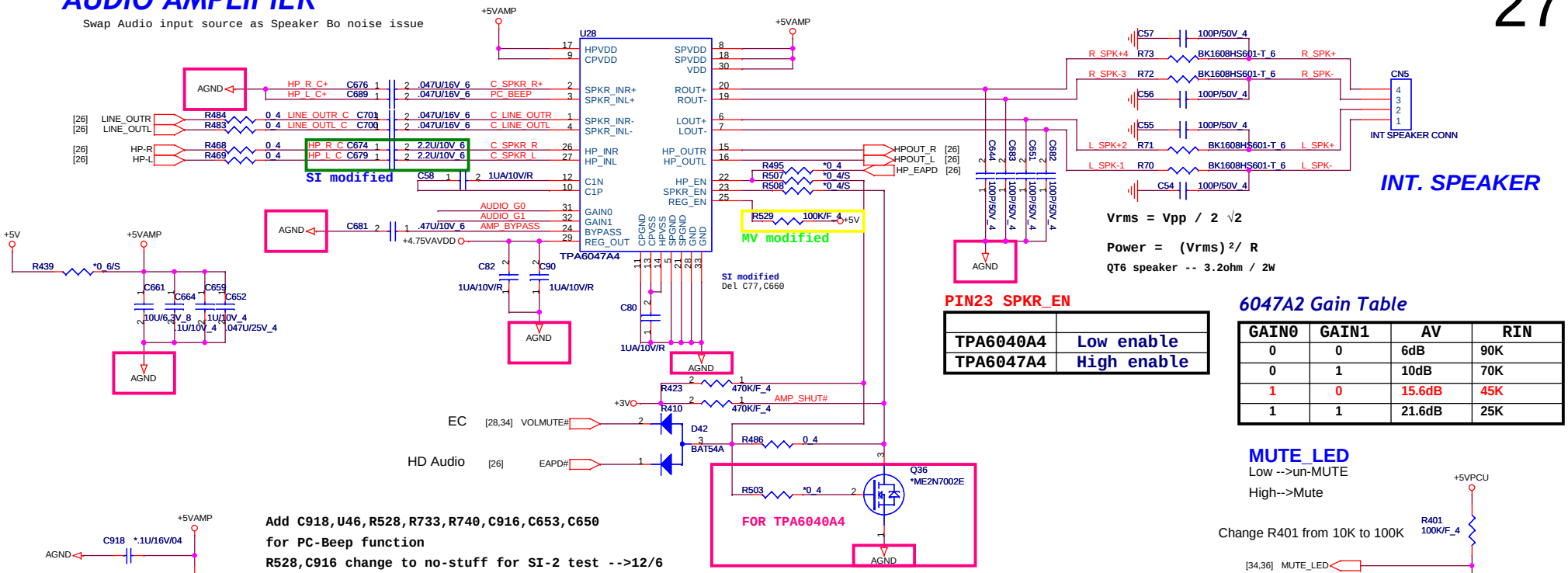
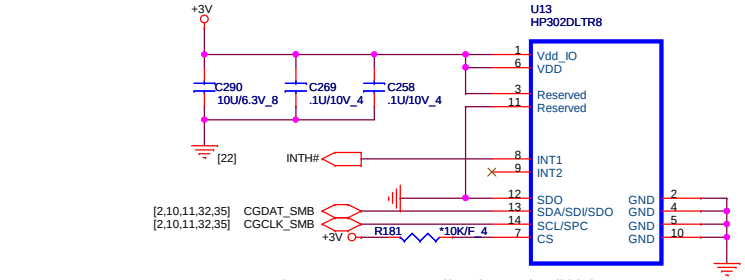
AUDIO AMPLIFIER

Swap Audio input source as Speaker Bo noise issue



Accelerometer Sensor

SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low



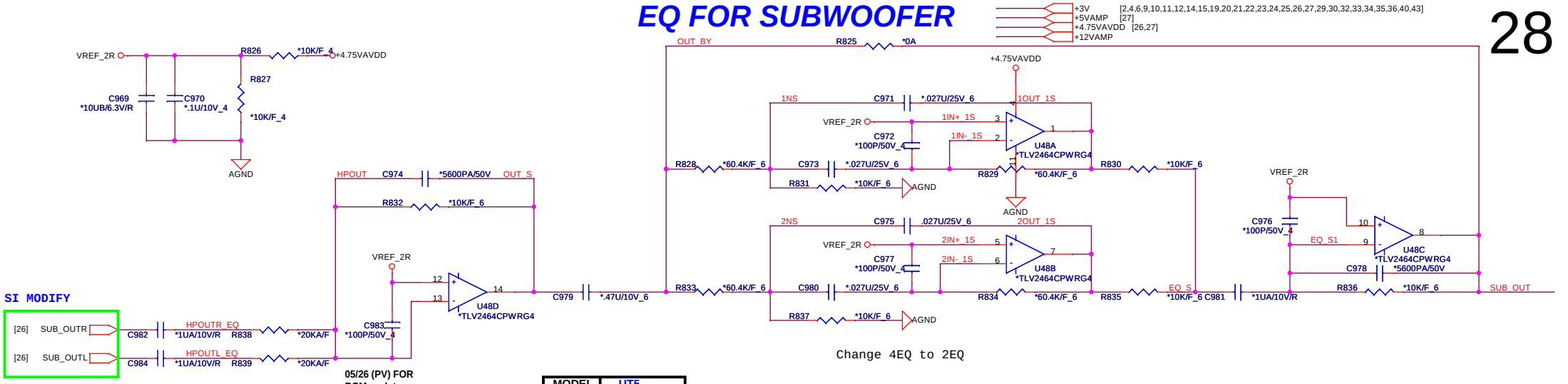
Change R181 to no stuff as internal pull high

Pin 12: Low 38hex

Pin 12: unconnected/floating 3Ahex

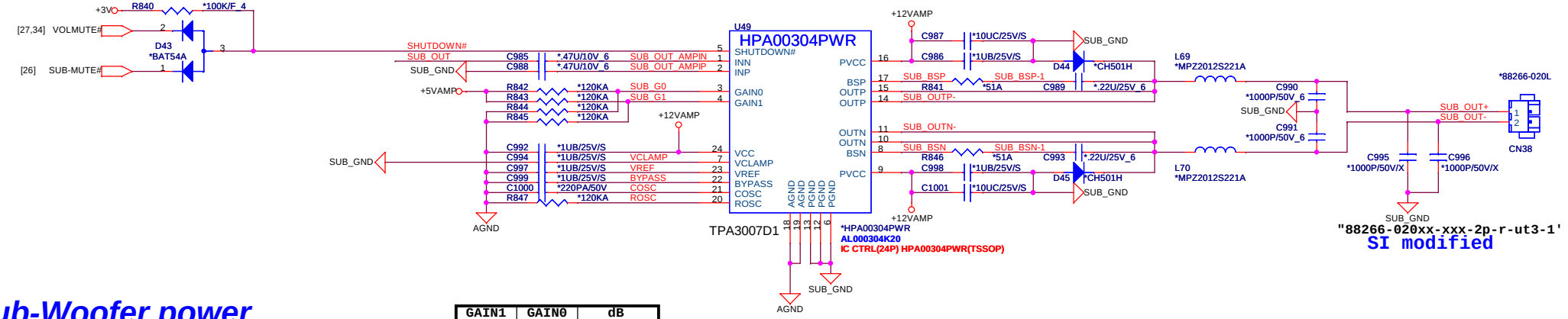
NB5	PROJECT : UT3/5 Quanta Computer Inc.
Size: Custom	Document Number: AMP_TPA6017/Accelerometer
Rev: PV	
Date: Monday, October 20, 2008	Sheet 27 of 43

EQ FOR SUBWOOFER

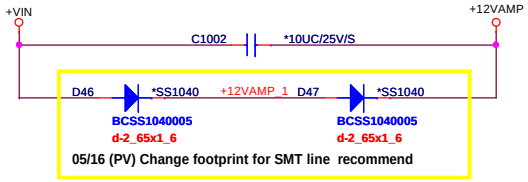


Change 4EQ to 2EQ

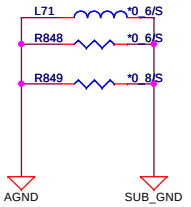
MODEL	UT5
R316	60.4K/F_6
R319	60.4K/F_6
R330	60.4K/F_6
R314	60.4K/F_6
C509	0.027U/25V_6
C510	0.027U/25V_6
C529	0.027U/25V_6
C543	0.027U/25V_6



Sub-Woofer power



GAIN1	GAIN0	dB
0	0	12
0	1	18
1	0	23.6
1	1	36



PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	SUBWOOFER(EQ & AMP.)	PV

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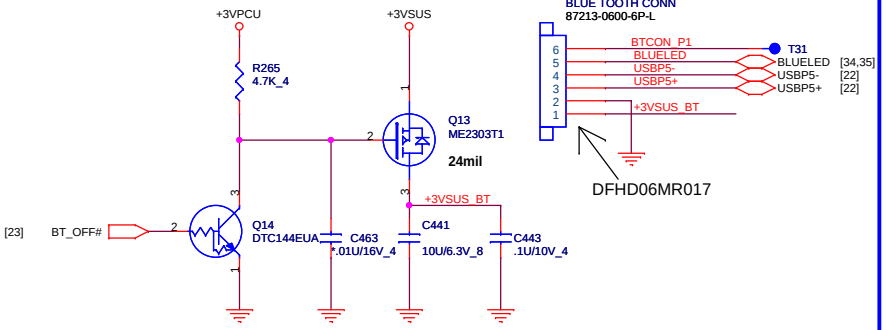
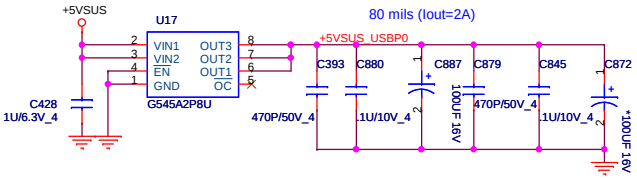
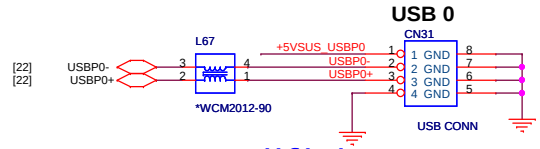
BLUETOOTH



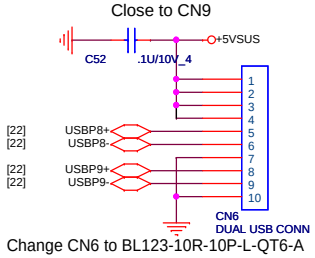
LEFT SIDE USBX1 and E-SATA/USB COMBO



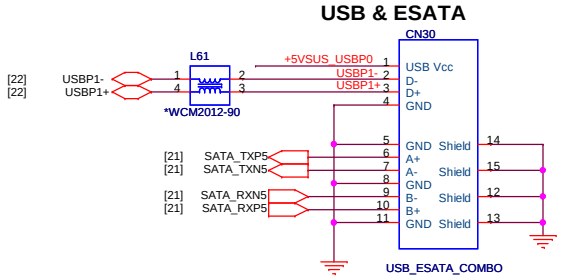


SI modified
usb-020173mr004s51-4p-r-h-ut3

RIGHT SIDE USBX2



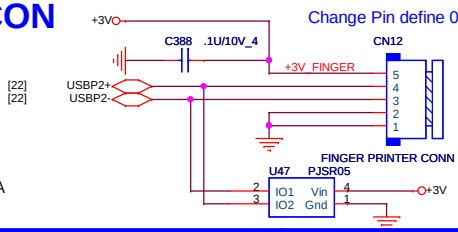
Change CN6 to BL123-10R-10P-L-QT6-A



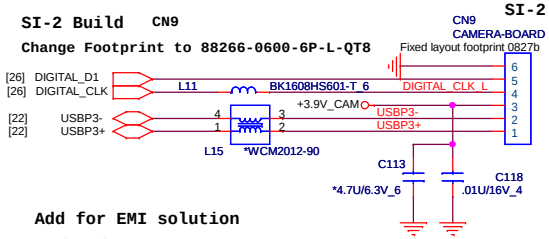
USB fingerprint CON

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

Change CN12 to BL123-05R-5P-L-QT6-A
Add U47 for Finger print USB signal

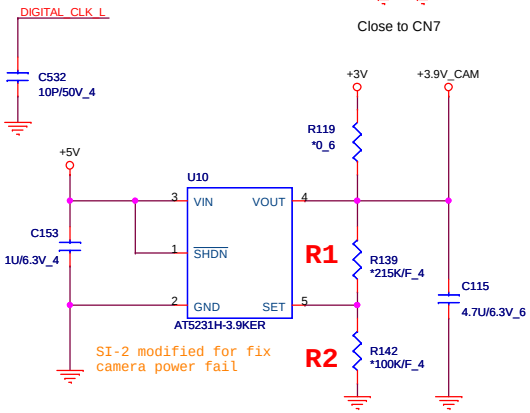


USB CAMERA /DIGITAL MIC CONNECT



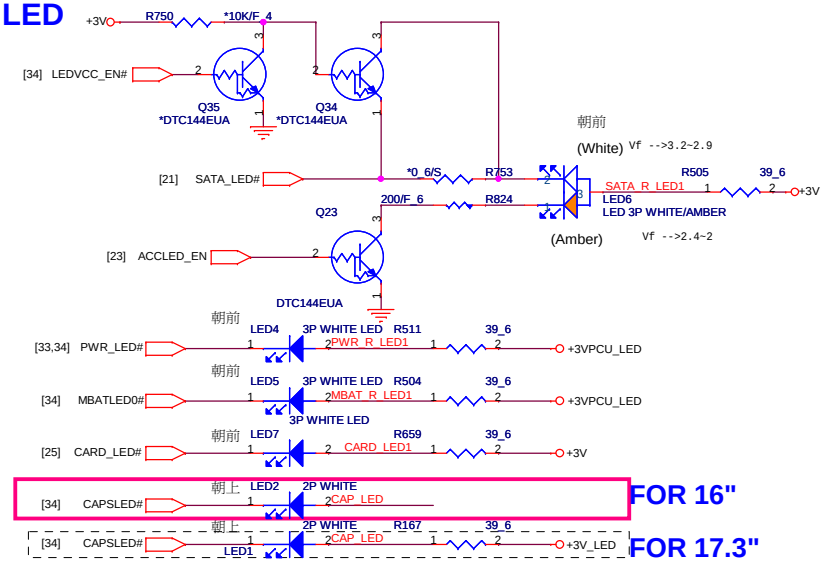
Add for EMI solution

Close to CN7



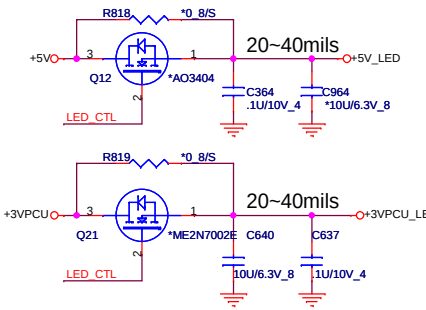
Vout=1.25(1+R1/R2)

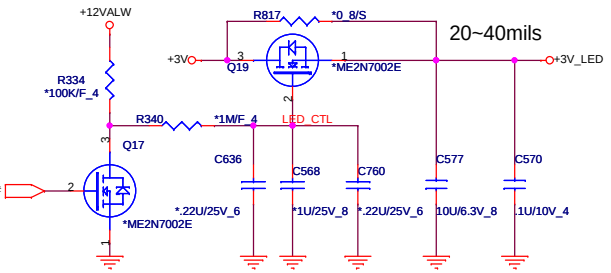
LED



LED PWR CONTROL

Change Q12 to AO3404 as LED current limited





NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size: Custom	Document Number: BT/WC/FT/TS/ESATA/USB	Rev: PV
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T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

For 8102E/8111C

[31] +CTRL15 — R648 *0_6 — +CTRL15_E
Stuffed for 8102E

[31] +FB12 — R641 *0_6/S — +LAN_A1.8_FB12
Stuffed for RTL8111C and nostuff 8102E

+LAN_D1.5 — R649 *0_6/S — +LAN_D1.5_SRVDD
Stuffed for 8102E/RTL8111C

+3VLANVCC — R647 *0_6/S — +CTRL15_E
C894 10U/6.3V_8 — C889 10U/6.3V_8 — C890 .1U/10V_4
+3VLANVCC — R247 *0_6/S — +3V_GVDD
enable switch regular
Stuffed for RTL8111C(10/100/1000)

Y2 25MHZ
C427 33P/50V_4 — C420 33P/50V_4
PV MODIFY
8102E No Mount
8111C No Mount ,R247 mount

C414 *.1U/10V_4 — C417 *.1U/10V_4 — R233 2.49K/F_4 — LANRSET

U18#63 wider than 40 mils
U18#1 wider than 60 mils

U18 RTL8111C-VB-GR
Pin 65

Isolate pull low:
1.Can only disable RTL8111C.
2.RTL8101E can't disable

for 93C56 used. NC if 93C46 is used.
R653 *10K/F_4 — U43 *M93C46-WMN6TP — C897 *.1U/10V_4
3.24K/F_4 R652

R263 *1K/F_4 — R262 15K/F_4
Change back to R261 at 1/24
ISOLATEB — R261 100/F_4 — D38 *RB501V-40 — LAN_DISABLE# [34]

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

R252 *0_6/S — R259 *0_6/S — LAN-AGND

C531 .1U/10V_4
New add and Close to Pin 5
From Vendor EMI suggest

R434
8111C = No Mount
8102E = Mount

T3 T4

PCIE_RXN1_LAN_L — C452 .1U/10V_4 — PCIE_RXN1_LAN [22]
PCIE_RXP1_LAN_L — C442 .1U/10V_4 — PCIE_RXP1_LAN [22]
CLK_PCIE_LAN# — CLK_PCIE_LAN# [2]
CLK_PCIE_LAN — CLK_PCIE_LAN [2]
[23,32,35] PCIE_WAKE# — PCIE_WAKE#
[22] PCIE_TXP1_LAN — PCIE_TXP1_LAN
[22] PCIE_TXN1_LAN — PCIE_TXN1_LAN
[22,25,32,34,35] PLTRST# — R248 *0_4/S
[34] LAN_REST# — R246 *0_4

Swap PCIE from Port 6 to PCIE Port 1
Swap PCIE from Port 6 to PCIE Port 2

AL08111C001 IC CTRL(64P) RTL8111C-VB-GR(QFN)
AL08102E001 IC CTRL(64P) RTL8102E-VB-GR(QFN)

Remove 8111B and 8101E support in PV Build
1. Delete R264 (For 8111B)
2. Delete R650 and T28
3. Delete R651 and U18#33 for 8111B support
4. Delete R231 as RSET
5. Delete R242,R243,R244,R245,C394,C395 8101E support

LAN_GLINK10# — D36 BAT54A
LAN_GLINK100#
LAN_GLINK1000# — D35 RB501V-40 — LAN_GLED#
LAN_TX# — R109 *0_4/S — LAN_YLED#
C48 *.01U/16V_4 — C88 *.01U/16V_4

Link

Stuffed for RTL8101E
+LAN_A1.8 — R589 *0_4
U33 NS892402
C782 .01U/16V_4 — C783 .01U/16V_4 — C789 .01U/16V_4 — C790 .01U/16V_4
MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
V_DAC

Add C898,C899,C900,C902 as HP request
SI Build
LAN_MCT0 — C898 0.01U/100V_0603 — R544 75/F_4 — LAN_MX0+ [36] / LAN_MX0- [36]
LAN_MCT1 — C899 0.01U/100V_0603 — R545 75/F_4 — LAN_MX1+ [36] / LAN_MX1- [36]
LAN_MCT2 — C900 0.01U/100V_0603 — R547 75/F_4 — LAN_MX2+ [36] / LAN_MX2- [36]
LAN_MCT3 — C902 0.01U/100V_0603 — R548 75/F_4 — LAN_MX3+ [36] / LAN_MX3- [36]
C781 1000P/3KV_1808

FOR EMI
C89 *.1U/10V_4
RJ45 CN24
+3V_LAN — R89 330/F_4 — LAN_GLED — LAN_GLED# — LED_GRE_P / LED_GRE_N
LAN_MX3- LAN_MX3+ LAN_MX1- LAN_MX2- LAN_MX2+ LAN_MX1+ LAN_MX0- LAN_MX0+ — RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+ — GND1 GND
FOR EMI
+3V_LAN — R87 330/F_4 — LAN_YLED — LAN_YLED# — LED_YEL_P / LED_YEL_N
SI Build
C81 *.1U/10V_4
RJ45_CONN

NS892402:GIGABIT
NS892405:10/100

DB0AT9LAN05
DB0ZB1LAN04

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111C/8101E/RJ45	PV

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T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

LANVCC
1.2W
364mA

+3VLANVCC

Power trace Layout 寬度> 30mil

+3V_LAN

C454 .1U/10V_4
C475 .1U/10V_4
C477 .1U/10V_4
C399 .1U/10V_4

these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

C385 4.7U/6.3V_6
C480 .1U/10V_4

+3V_A_LAN

C401 .1U/10V_4
C434 .1U/10V_4

these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

8111C CV-4706MN00
8102E CS00004JA40

For Giga must change L65 to Inductor (Chipset include switch power)

+CTRL18 will become to switch power phase

placement close to lan chipset

L54 for Gaga lan use 4.7uH power choke
A>500mA tolerance ±15%

SI Build

+CTRL18

L65 4.7UH_2016

+FB12 [30]

L63 *0_8/S

Power trace Layout 寬度> 30mil

+LAN_A1.8

C884 *4.7U/6.3V_6

C931 *10U/6.3V_8 SI build
C930 10U/6.3V_8 SI build
C881 4.7U/6.3V_6
C876 4.7U/6.3V_6
C878 .1U/10V_4

For 8102E

C891 .1U/10V_4
C892 .1U/10V_4
C875 .1U/10V_4
C893 .1U/10V_4

these cap are for lan chip LAN_A1.8 pins--5, 8, 11 and 14. placement close chip

STUFF 100 ohm BEAD

+LAN_E1.8

R250 *0_8/S

C422 Change to 1u for 8102E

C421 .1U/10V_4
C422 1U/6.3V_4

LAN-AGND

these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

Remove R250,L63,L66 -->For 8102E

L66 *0_8/S

Only For 8111C application

[30] +CTRL15

L64 *0_8

C883 *4.7U/6.3V_6
C888 *4.7U/6.3V_6
C895 *4.7U/6.3V_6
C896 *.1U/10V_4

For 8102E

+LAN_D1.5

Power trace Layout 寬度> 30mil

C474 .1U/10V_4
C479 .1U/10V_4
C459 .1U/10V_4
C456 .1U/10V_4
C472 .1U/10V_4
C461 .1U/10V_4
C476 .1U/10V_4
C415 .1U/10V_4
C478 .1U/10V_4
C400 .1U/10V_4

these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58.placement close lan chip

Power domain chart

	RTL8111C(P) RTL8102E
LANVCC	3.3V
LAN_D1.8	1.2V
LAN_A1.8	1.2V
LAN_D1.5	1.2V

C422 change to 1uf

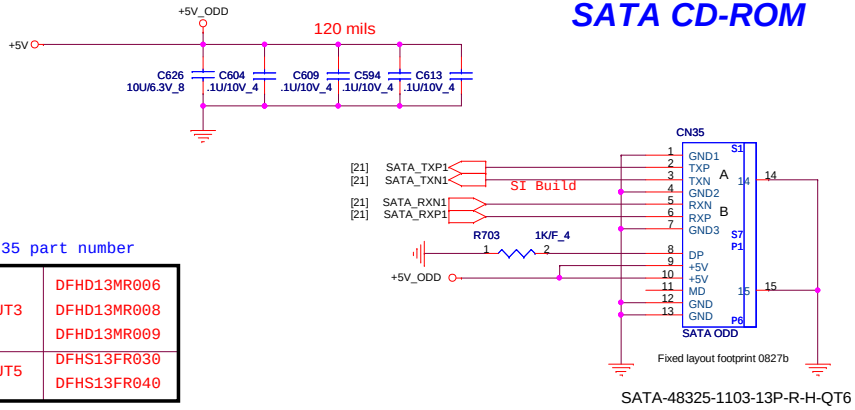
PROJECT : UT3/5
Quanta Computer Inc.

NB5

Size A3 | Document Number LAN Power | Rev PV

Date: Monday, October 20, 2008 | Sheet 31 of 43

SATA CD-ROM



CN35 part number

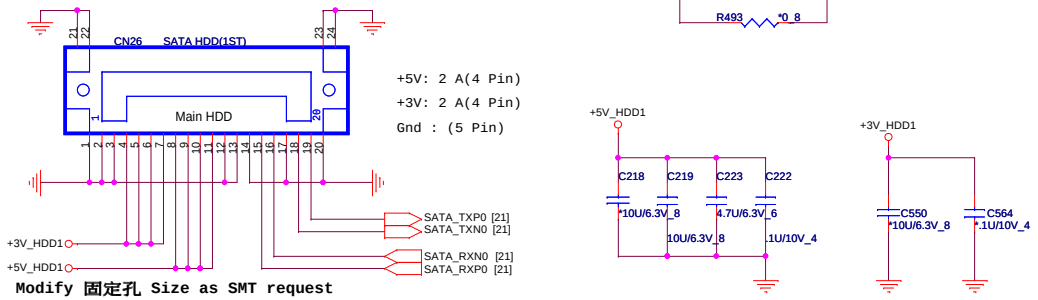
UT3	DFHD13MR006
	DFHD13MR008
	DFHD13MR009
UT5	DFHS13FR030
	DFHS13FR040

SATA-48325-1103-13P-R-H-QT6

SATA HDD CONNECTOR

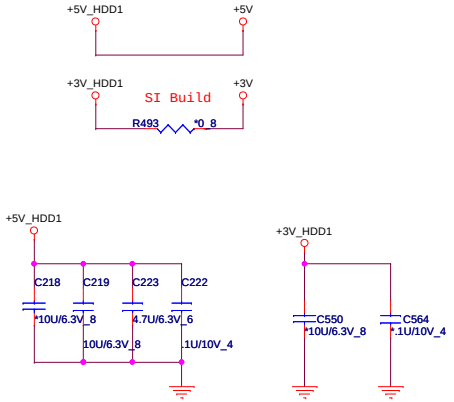
DFHD20MR005

DC Current rating: 0.5 A



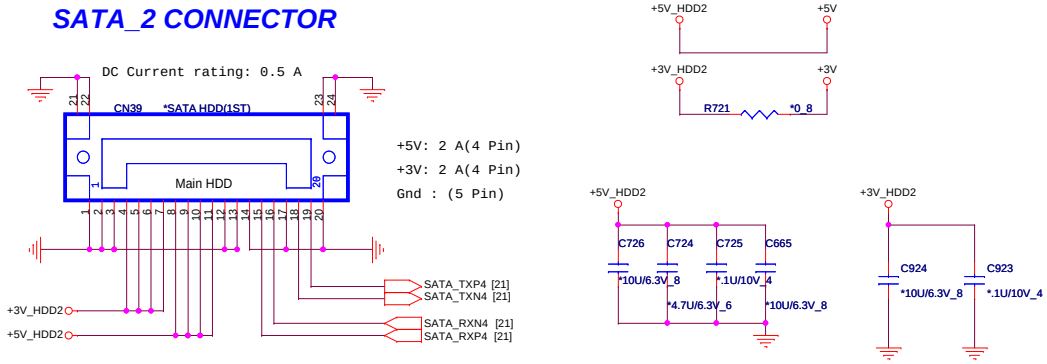
Modify 固定孔 Size as SMT request

GS12201-1011-9F-20P-L-QT6



DB modified

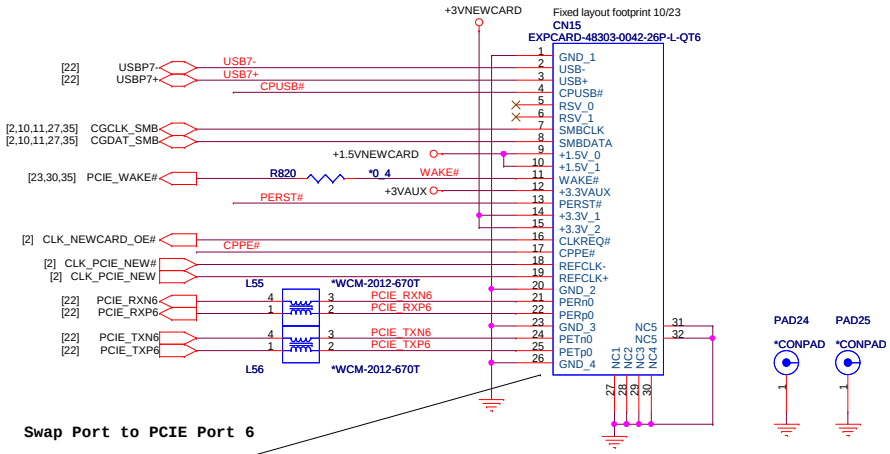
SATA_2 CONNECTOR



NEWCARD

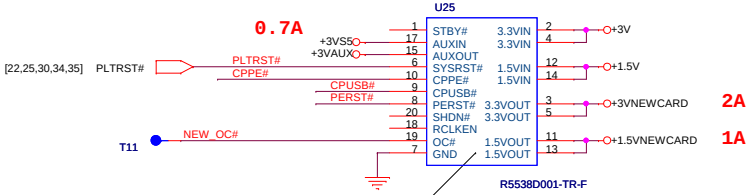
NEWCARD (PCIEXPRESS*1 + USB*1)

32

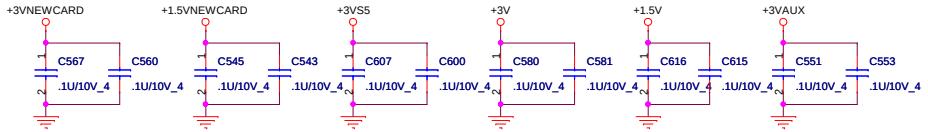


Swap Port to PCIE Port 6

Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



add Pin 21~25 as U25 Thermal pad tied to Gnd



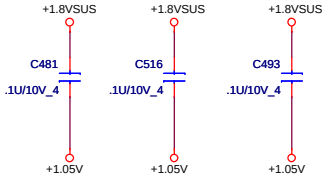
	Header	Housing
MLX	DFHD26MS012	DFHS26FR023
FOX	DFHD26MS013	DFHS26FR024
DGN	DFHD26MS017	DFHS26FR028

NB5

PROJECT : UT3/5
Quanta Computer Inc.

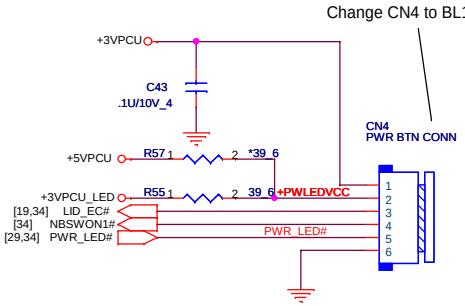
Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD	PV

Date: Monday, October 20, 2008 Sheet 32 of 43



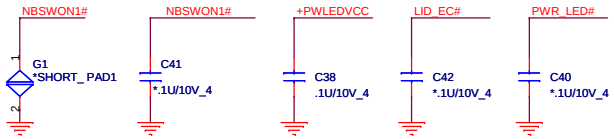
Close to U21 For EMI

Change CN4 to BL123-06R-6P-L-QT6-A



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

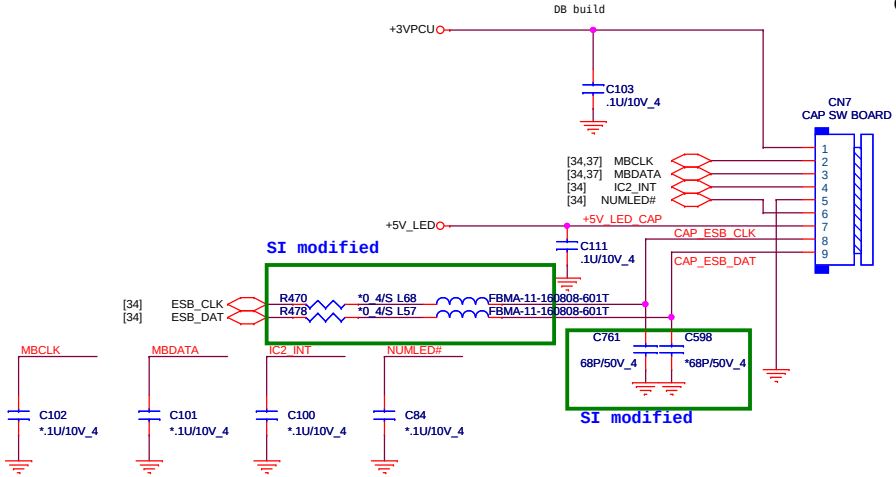
POWER BOTTON CONNECT



EMI 0828

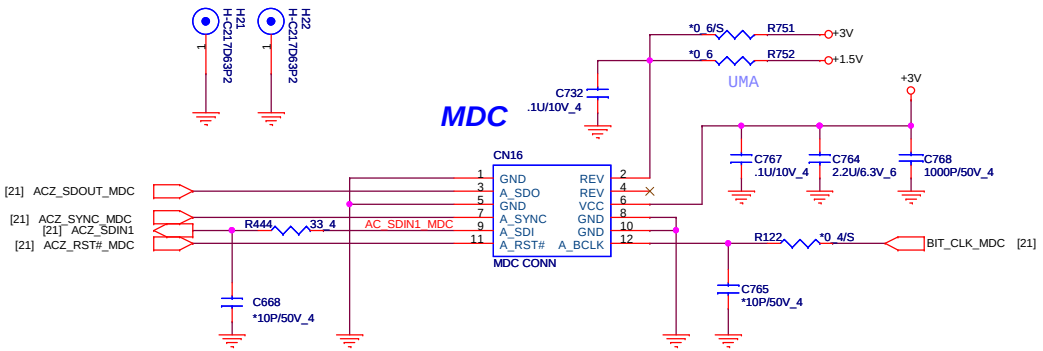
POWRER SW CONNECT

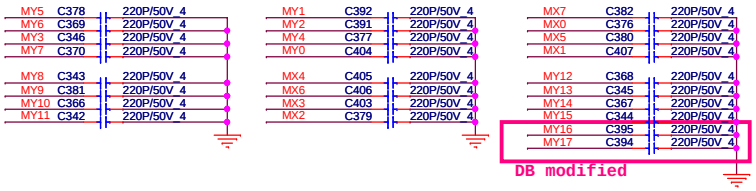
CAP SW CONNECT



1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT

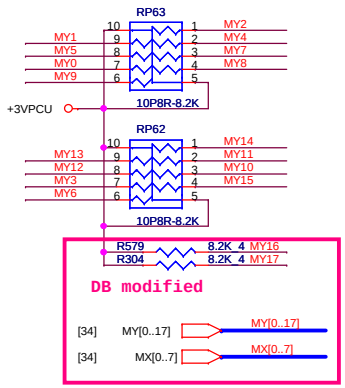
Modem CONN



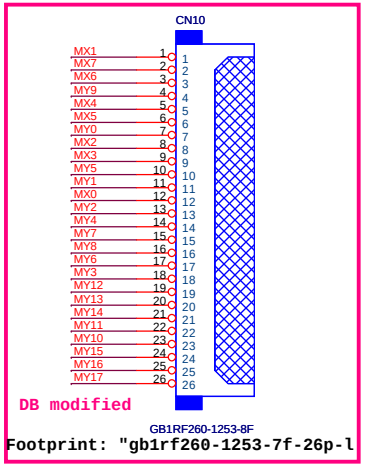


DB modified

KEYBOARD PULL-UP



DB modified

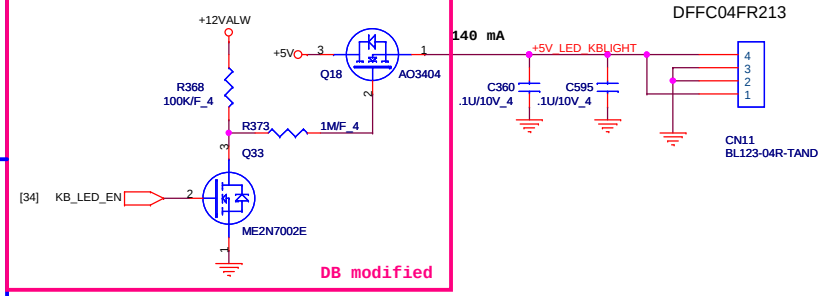


DB modified

Footprint: "gb1rf260-1253-7f-26p-l

clear ABS 758 resin for key cap.
7 LEDs for 15.4" (total LED current 140mA)
11 LEDs for 17" (Total LED current 220mA)

DFFC04FR213



DB modified

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
	Size: Custom Document Number: KB/CAP/POWER CONN/MDC	Rev: PV
	Date: Monday, October 20, 2008	Sheet 33 of 43

Change U20 layout footprint
to LQFP128-16X16-4-AA1

U20

KB3926QF C0

DB modified

SI modified

R323 remove for KB3926 C version

For KB3926 B, C version

ID	R374	R379
UT3	10K	N/A
UT5	N/A	10K

Hi ==> 120W
Low ==> 65W/90W

Change to RB500 as Current loss

R430 Change to 100k ohm ,pull low

Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier
Add T37,T38,T39 for EC
Delete T10 and tie pin 117 from Lan for DSM

TOUCH PAD CONNECTOR

25 mils

CN13
TOUCH PAD CONN
DFFC12FR293

TOUCH PAD L/R FOR 16"

TOUCH PAD ON/OFF FOR 16"

close conn

TOUCH PAD L/R FOR 17.3"

TOUCH PAD ON/OFF FOR 17.3"

DB modified

Socket: DG008000031

MXIC AKE38FP0Z00
WINBOND AKE38ZP0N01
EON AKE38ZA0Q00

2M byte
SPI
BIOS

R273
64.9K -->65W CS36492FB17
33.2K -->90W CS33322FB13
Change to 1SS355 as Current loss

PROJECT :	UT3/5
Quanta Computer Inc.	
Size: Custom	Document Number: KB3926/ROM/TP
Rev: PV	
Date: Monday, October 20, 2008	Sheet 34 of 43

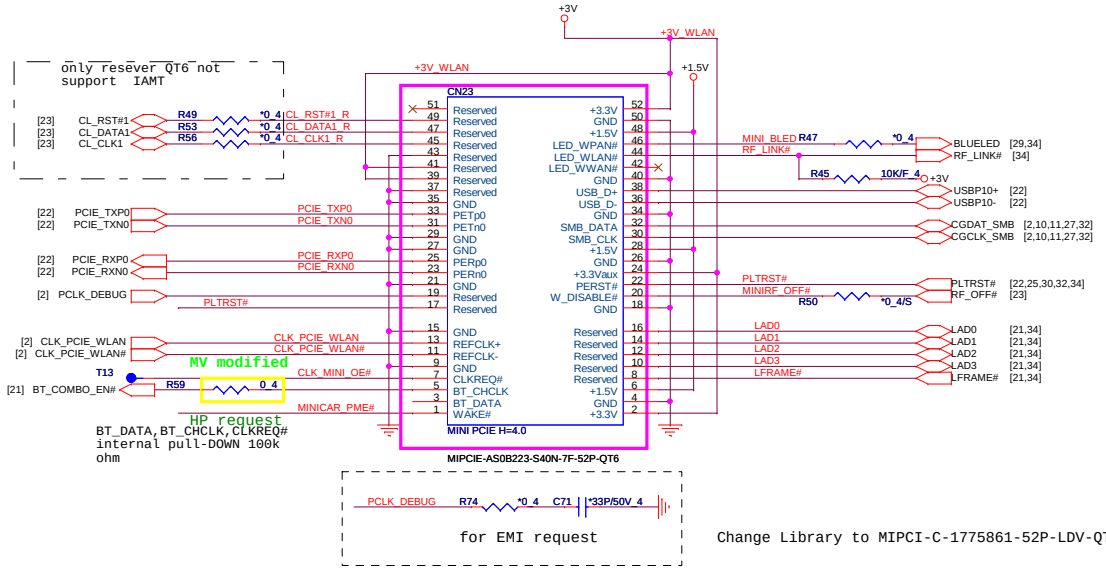
NB5

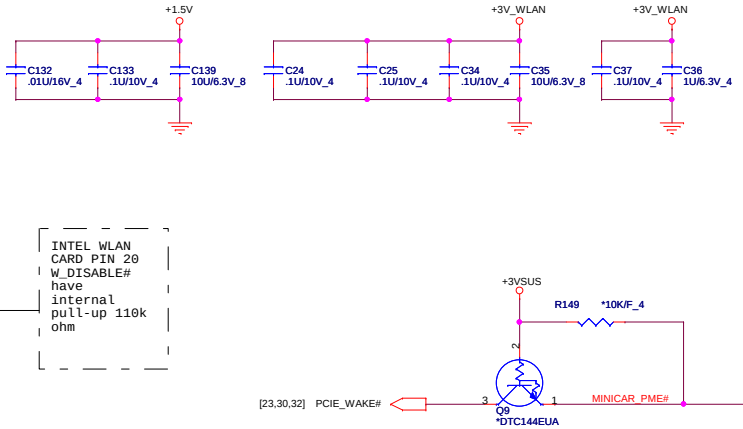
Mini PCI-E Card 1
WLAN

Delete R78 and tied the CN23#24 to R110 direction
Change CN23 layout footprint to MIPCIE-AS0B223-S40N-7F-52P-QT6 as ME drawing

Change net name

35





Change Library to MIPCI-C-1775861-52P-LDV-QT6 12/11

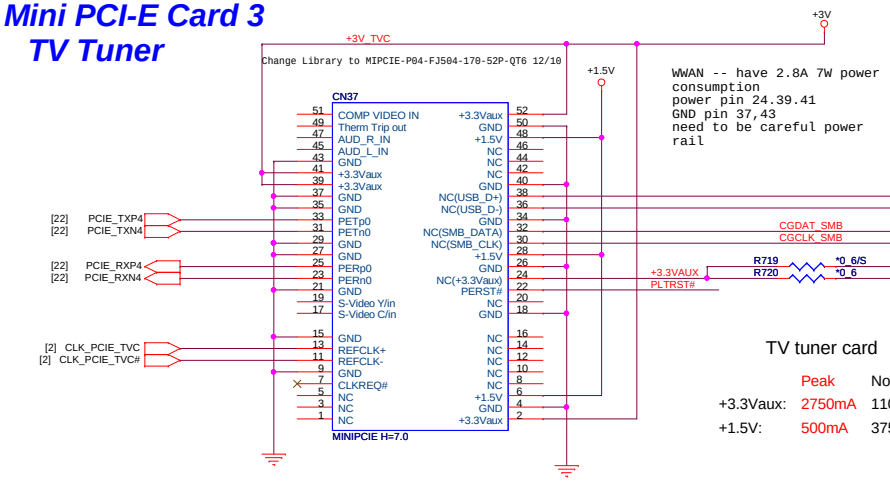
M/B Screw Hole

SI-2,h-e276x315d118p2

Modify H16 Hole size
H-TC256BC315D118P2

SI-2

Mini PCI-E Card 3
TV Tuner



TV tuner card

	Peak	Normal
+3.3Vaux:	2750mA	1100mA
+1.5V:	500mA	375mA

New add as ME request

RF PAD

ME PAD

Routed spring

Delete PAD14

New add as RF request

New add as RF request

ME Routed spring

EMI PAD

MV MODIFY

ME-Ground Pad

PV MODIFY

ME-Ground Pad

MV MODIFY

SI modified

ME-Ground Pad

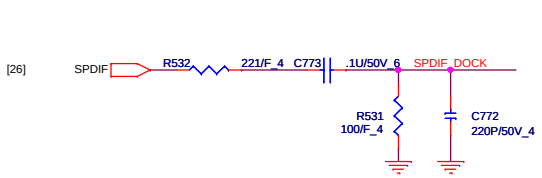
Del PAD18 (Same as PAD26)

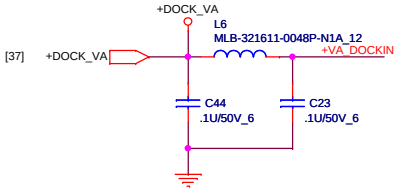
PROJECT :	UT3/5
Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X2 & HOLE
Rev: PV	
Date: Monday, October 20, 2008	Sheet 35 of 43

NB5

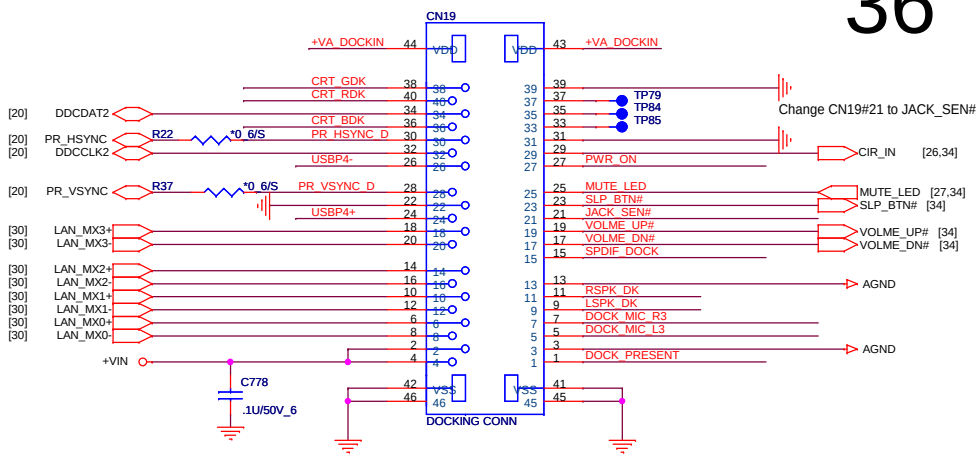
CABLE DOCK

support 6A 200mils
CX000480005

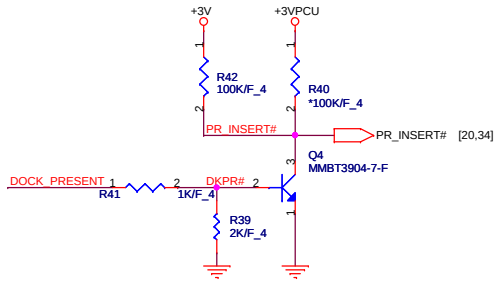


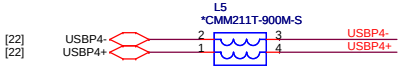


DFHS44FRC04



Change CN19#21 to JACK_SEN#



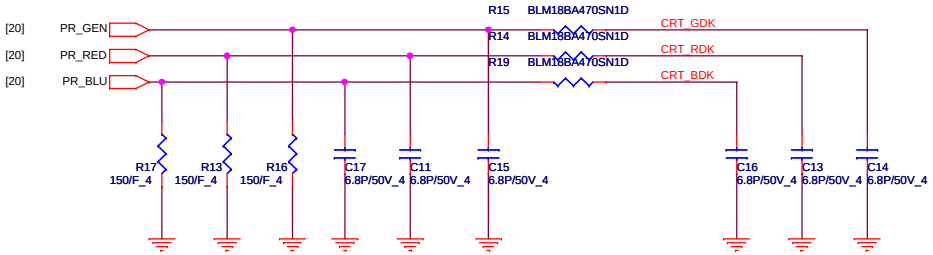


For IDT Dolby functionality. DB modified

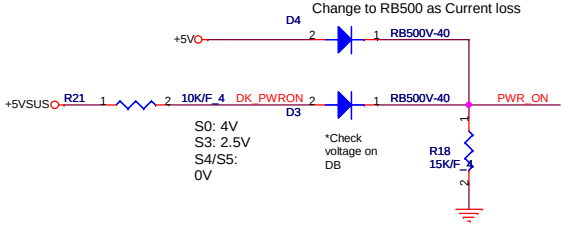
[26] PR_INSERT#_IDT — PR_INSERT#_IDT — R730 *0_4/S — R_INSERT#

R13,R16,R17 Change to install

Delete CX08T470000 as CRT rising time and falling time request

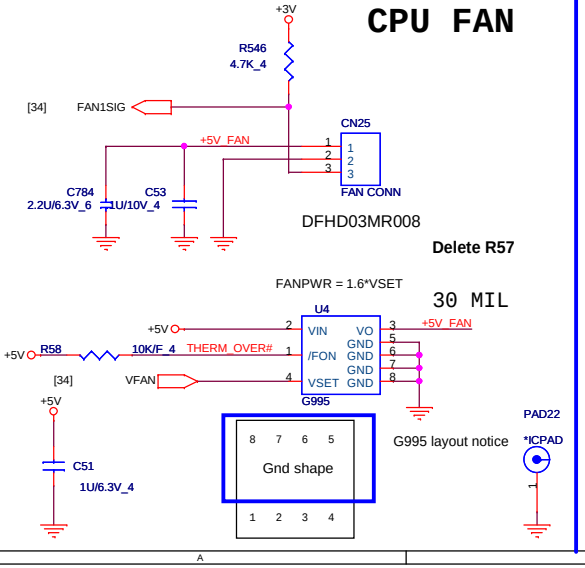


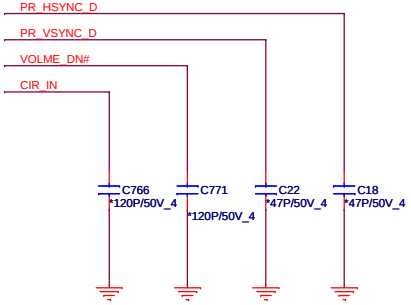
Change to RB500 as Current loss

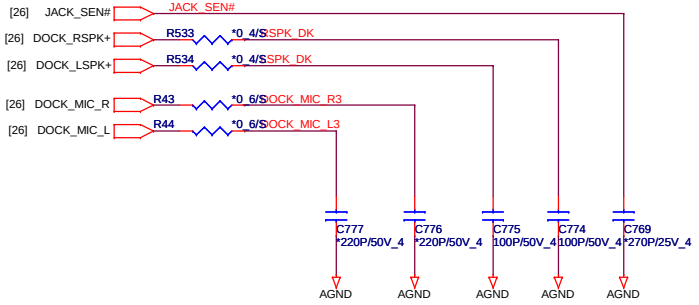


Add Loss net(GND Net)

CPU FAN







Change to Analog Gnd

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	PV

NB5

Date: Monday, October 20, 2008 Sheet 36 of 43

TOP DC_JACK
65W/90W

BATTERY CONNECTOR TYPE		
MODEL	PART NUMBER	FOOTPRINT
UT3	DFHD08MR015	BAT-BP02083-B09065-7F-9P-V-QT6
UT5	DFHD08MR030	bat-200045mr008g10jzr-8p-l-v

Change CN21 to BAT-BP02083-B09065-7F-9P-V-QT6

FOR 16"

FOR 17.3"

DB modified

SI modified

To PWR LED

EMI Solution

Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

Setting the Vin min to 12V
For ACSET 1.26V

Setting the Vin min to 17V
For EN = 1.06V

Charging Curret setting =
I chg = 165mV / Rsense * (Vchlim / 3.3V)

V ACLIM = VREF *
(Rl // 152K) / (Rhi // 152K + Rlow// 152K)
Input curretn = 2.9A (71.5K , 10K)
(0.05/Vref * Vaclim + 0.05) / Rsense

Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)

PROJECT : UT3/5	
Quanta Computer Inc.	
NB5	Size: Custom
Document Number: Charger (ISL6251)	Rev: PV
Date: Monday, October 20, 2008	Sheet 37 of 43

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 9A

SI modified

SI modified

Rds(on) 20m ohm

Rds(on) 20m ohm

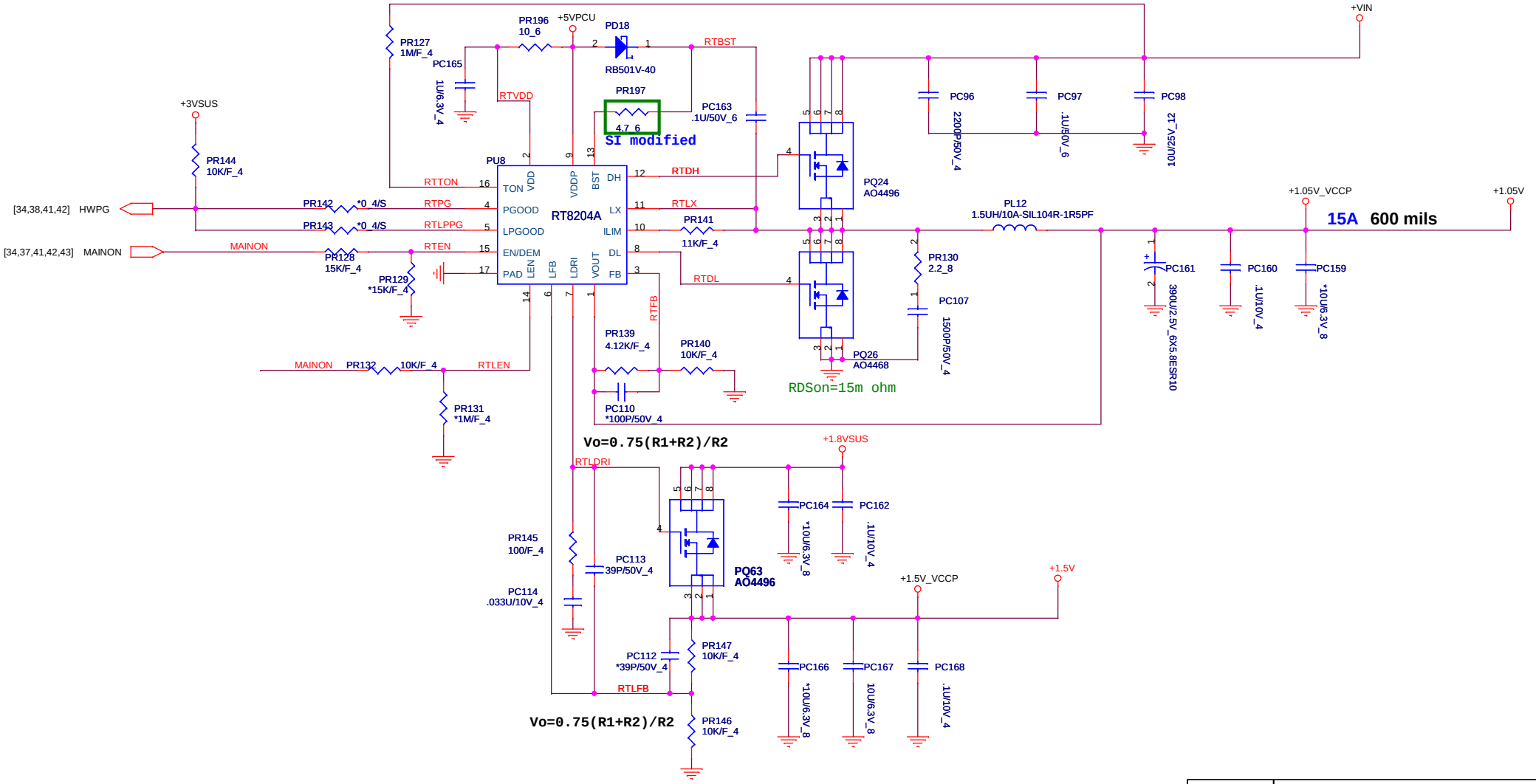
[4,37] SYS_SHDN#

HWPG [34,39,41,42]

NB5	PROJECT : UT3/5 Quanta Computer Inc.	
Size B	Document Number +5V/+3V (ISL6237)	Rev PV
Date: Monday, October 20, 2008	Sheet 38 of 43	

VCCP1.05V & +1.5V

+1.05Volt +/- 5%
Countinue current:7.5A
Peak current:10A
OCP minimum 15A

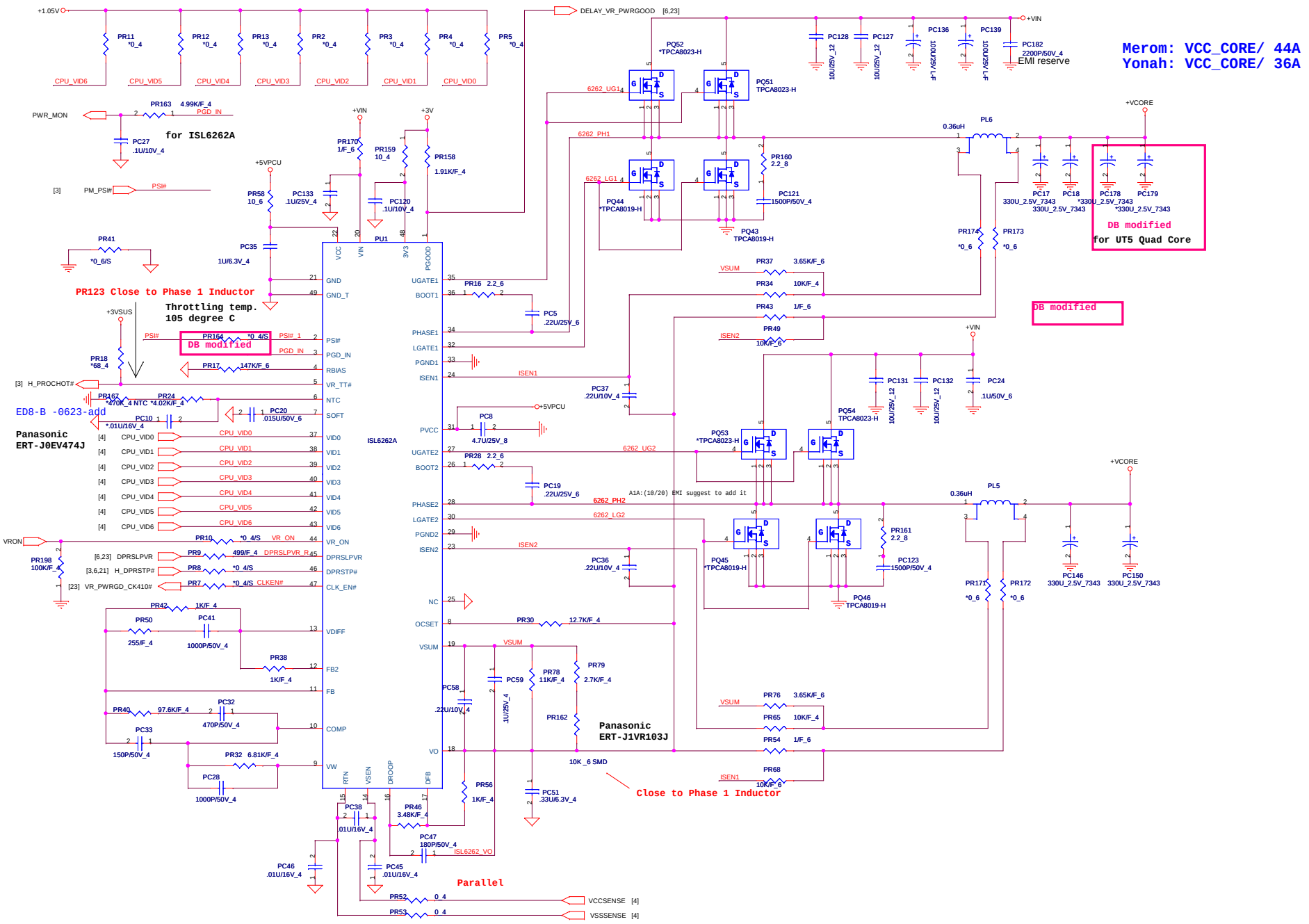


NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.05V/+1.5V (RT8204)	PV

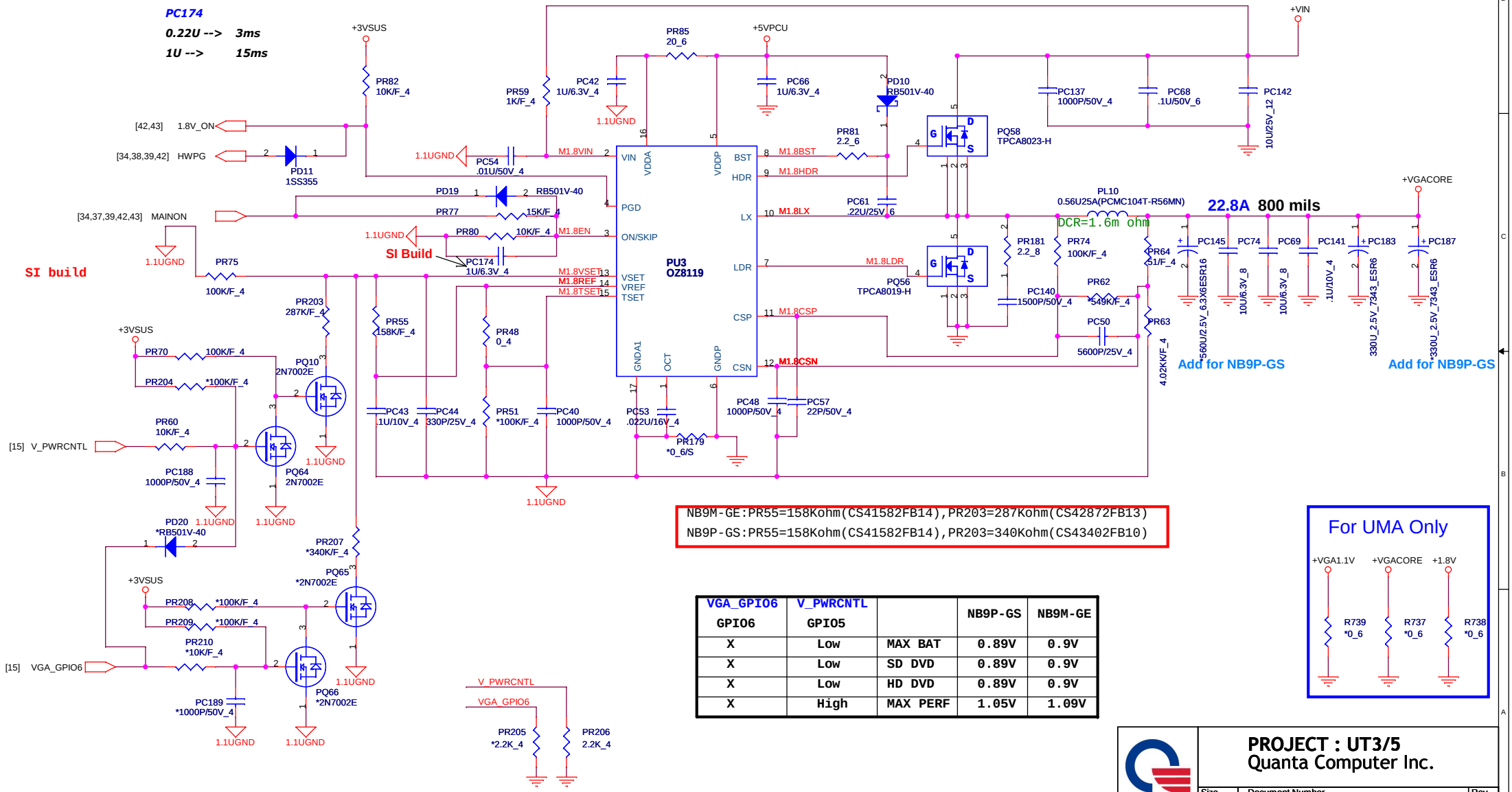
Date: Monday, October 20, 2008 Sheet 39 of 43



NB5	PROJECT : UT3/5 Quanta Computer Inc.		
	Size: Custom	Document Number: CPU Core (ISL6262A)	Rev: PV
	Date: Monday, October 20, 2008	Sheet 40 of 43	

VGA Core & VCC1.1

+1.1Volt +/- 5%
Countinue current:17.54A
Peak current:22.8A
OCP minimum 23A



NB9M-GE:PR55=158Kohm(CS41582FB14),PR203=287Kohm(CS42872FB13)
NB9P-GS:PR55=158Kohm(CS41582FB14),PR203=340Kohm(CS43402FB10)

VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5		NB9P-GS	NB9M-GE
X	Low	MAX BAT	0.89V	0.9V
X	Low	SD DVD	0.89V	0.9V
X	Low	HD DVD	0.89V	0.9V
X	High	MAX PERF	1.05V	1.09V

NB5

PROJECT : UT3/5
Quanta Computer Inc.

Size	Document Number	Rev
B	VGA Core OZ8119	PV

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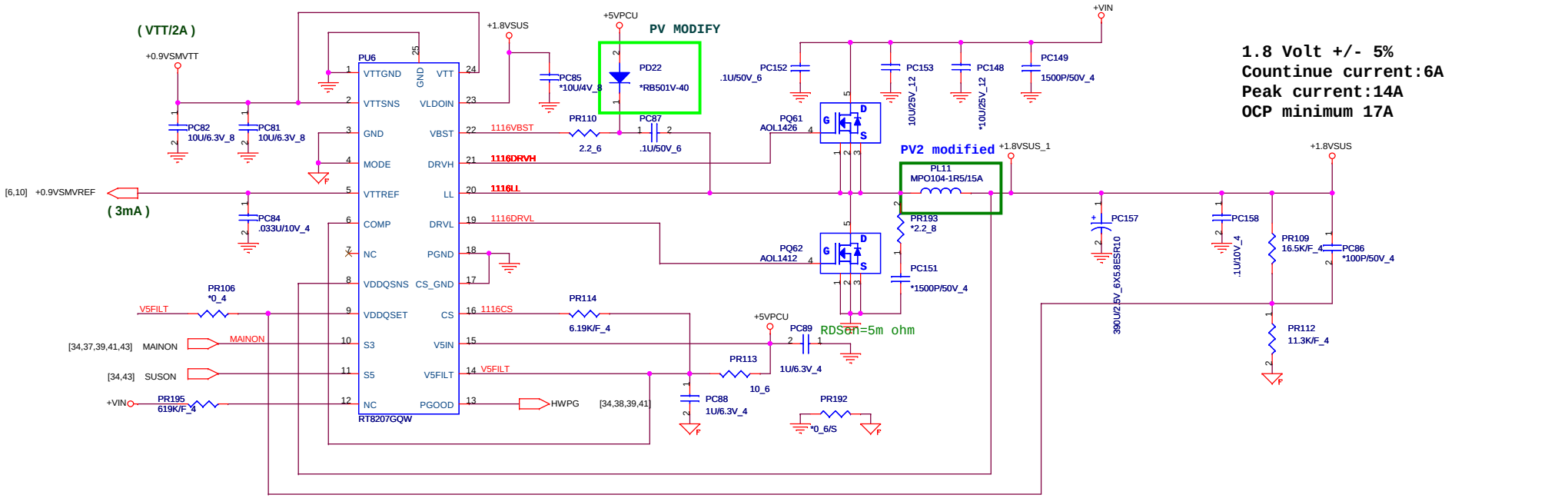
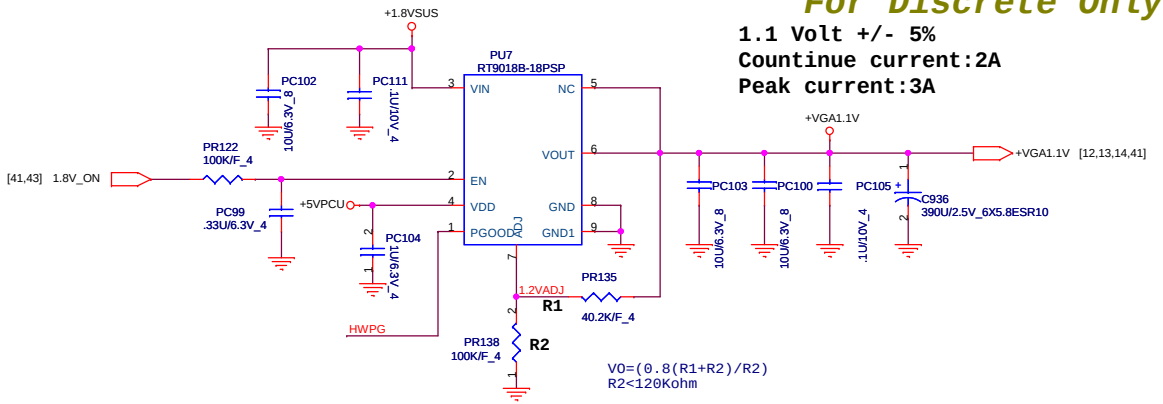
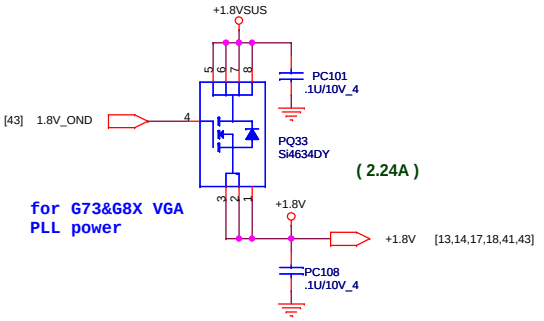
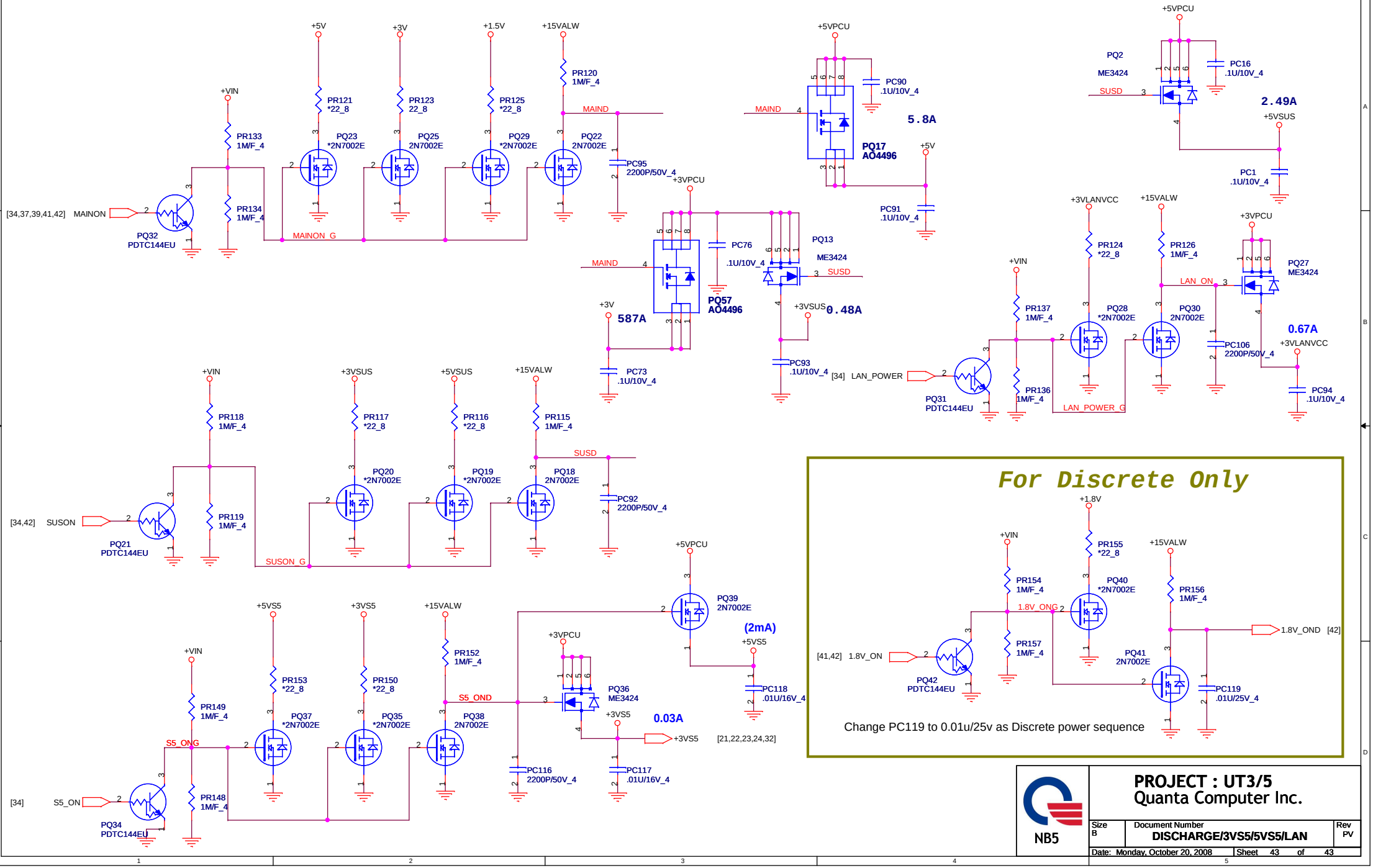


Change PR122 tied to 1.8V_ON as power sequence reuqest





NB5	PROJECT : UT3/5 Quanta Computer Inc.	
	Size: Custom Document Number: 1.8V/DDR_VTER/+1.8v/+1.1V	Rev: PV
	Date: Monday, October 20, 2008	Sheet 42 of 43


+5V
+3V
+1.5V
+15VALW
+VIN
PR121 *22_8
PR123 22_8
PR125 *22_8
PR120 1M/F_4
PR133 1M/F_4
PR134 1M/F_4
PQ23 *2N7002E
PQ25 2N7002E
PQ29 *2N7002E
PQ22 2N7002E
MAINON
[34,37,39,41,42] MAINON
PQ32 PDTC144EU
MAINON_G
MAIND
PC95 2200P/50V_4
+5VPCU
PC90 .1U/10V_4
PQ17 AO4496
5.8A
PC91 .1U/10V_4
+3VPCU
PC76 .1U/10V_4
PQ57 AO4496
587A
PC73 .1U/10V_4
PQ13 ME3424
SUSD
+3VSUS
0.48A
PC93 .1U/10V_4
PQ2 ME3424
PC16 .1U/10V_4
2.49A
+5VSUS
PC1 .1U/10V_4
+3VLANVCC
PR124 *22_8
PR126 1M/F_4
PR137 1M/F_4
PR136 1M/F_4
PQ28 *2N7002E
PQ30 2N7002E
LAN_ON
PQ27 ME3424
PC106 2200P/50V_4
0.67A
PC94 .1U/10V_4
[34] LAN_POWER
PQ31 PDTC144EU
LAN_POWER_G
PR118 1M/F_4
PR119 1M/F_4
PR117 *22_8
PR116 *22_8
PR115 1M/F_4
PQ21 PDTC144EU
[34,42] SUSON
SUSON_G
PQ20 *2N7002E
PQ19 *2N7002E
PQ18 2N7002E
PC92 2200P/50V_4
PQ39 2N7002E
(2mA)
PC118 .01U/16V_4
PR149 1M/F_4
PR148 1M/F_4
PR153 *22_8
PR150 *22_8
PR152 1M/F_4
PQ34 PDTC144EU
[34] S5_ON
S5_ONG
PQ37 *2N7002E
PQ35 *2N7002E
PQ38 2N7002E
S5_OND
PQ36 ME3424
0.03A
PC116 2200P/50V_4
PC117 .01U/16V_4
[21,22,23,24,32]
For Discrete Only
PR154 1M/F_4
PR155 *22_8
PR156 1M/F_4
PR157 1M/F_4
PQ42 PDTC144EU
[41,42] 1.8V_ON
1.8V_ONG
PQ40 *2N7002E
PQ41 2N7002E
1.8V_OND [42]
PC119 .01U/25V_4
Change PC119 to 0.01u/25v as Discrete power sequence
NB5
PROJECT : UT3/5
Quanta Computer Inc.
Size B
Document Number
DISCHARGE/3VS5/5VS5/LAN
Rev PV
Date: Monday, October 20, 2008
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