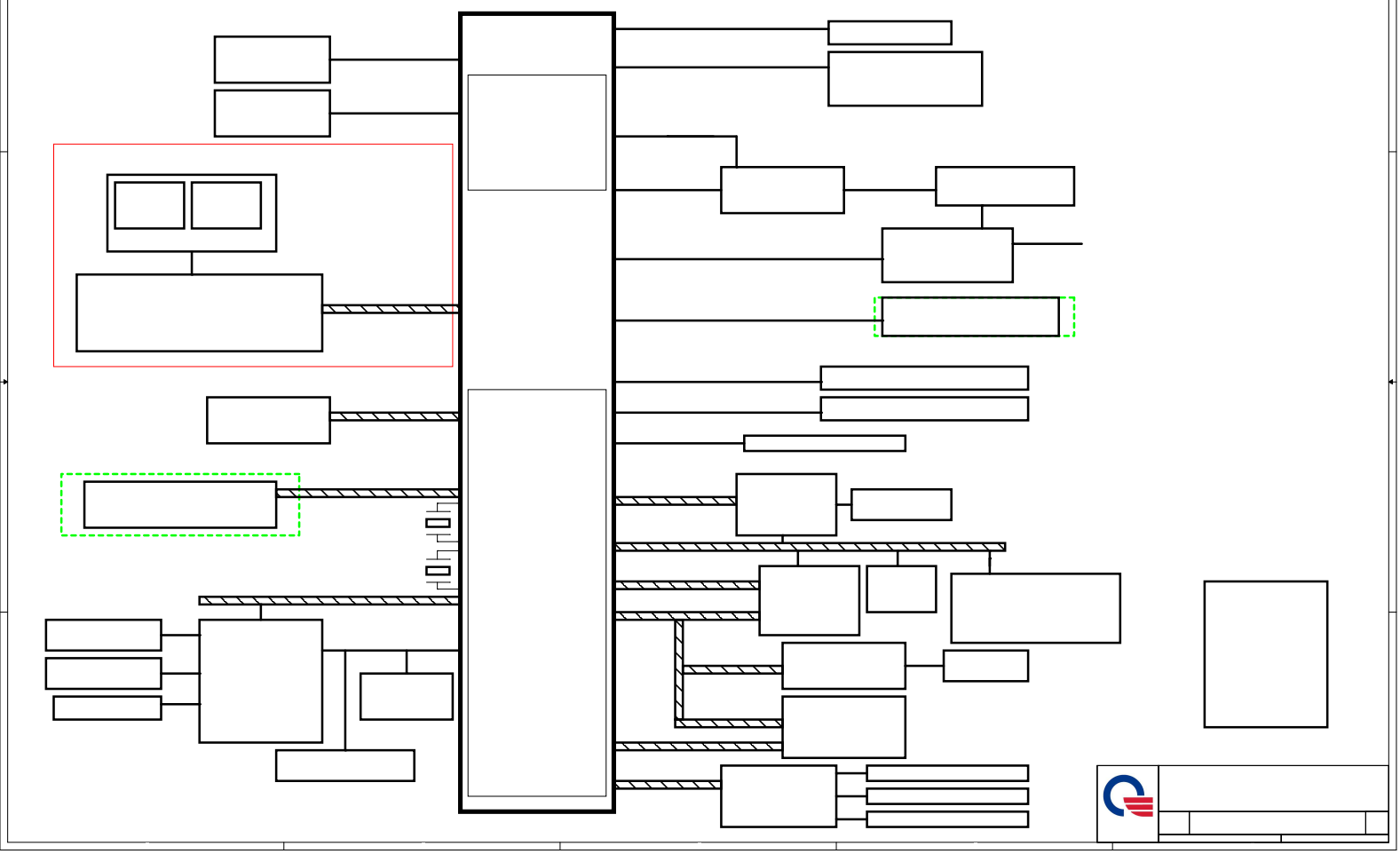
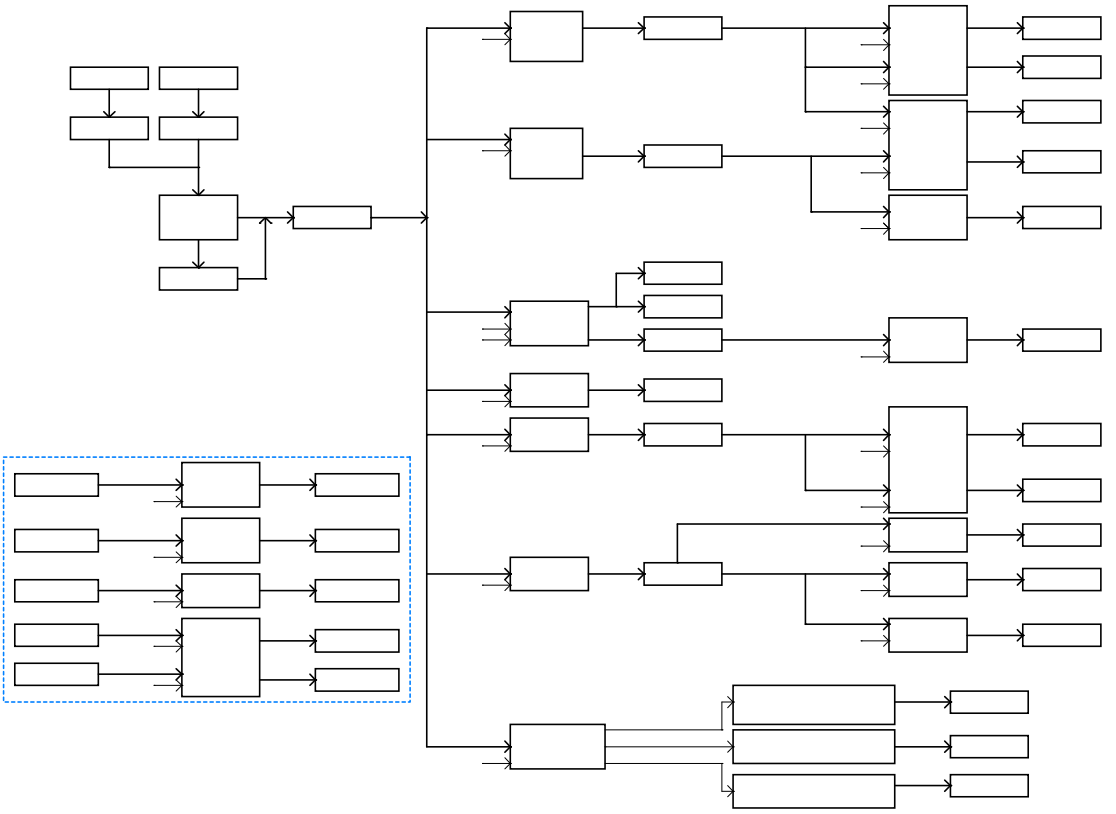
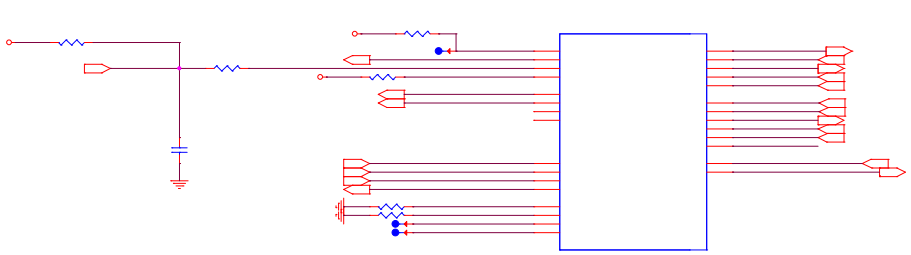
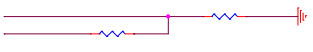
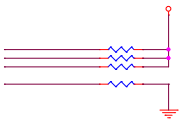
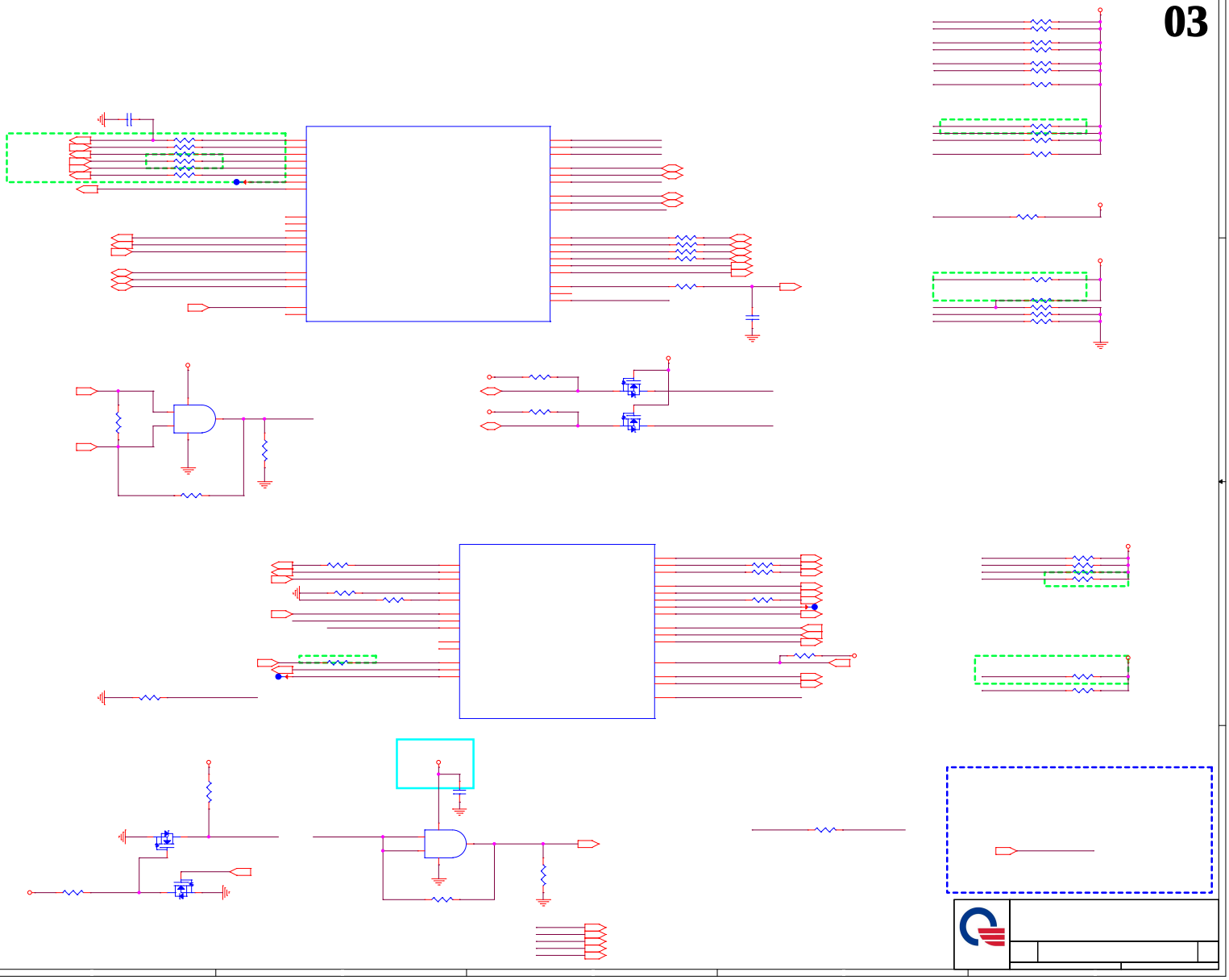


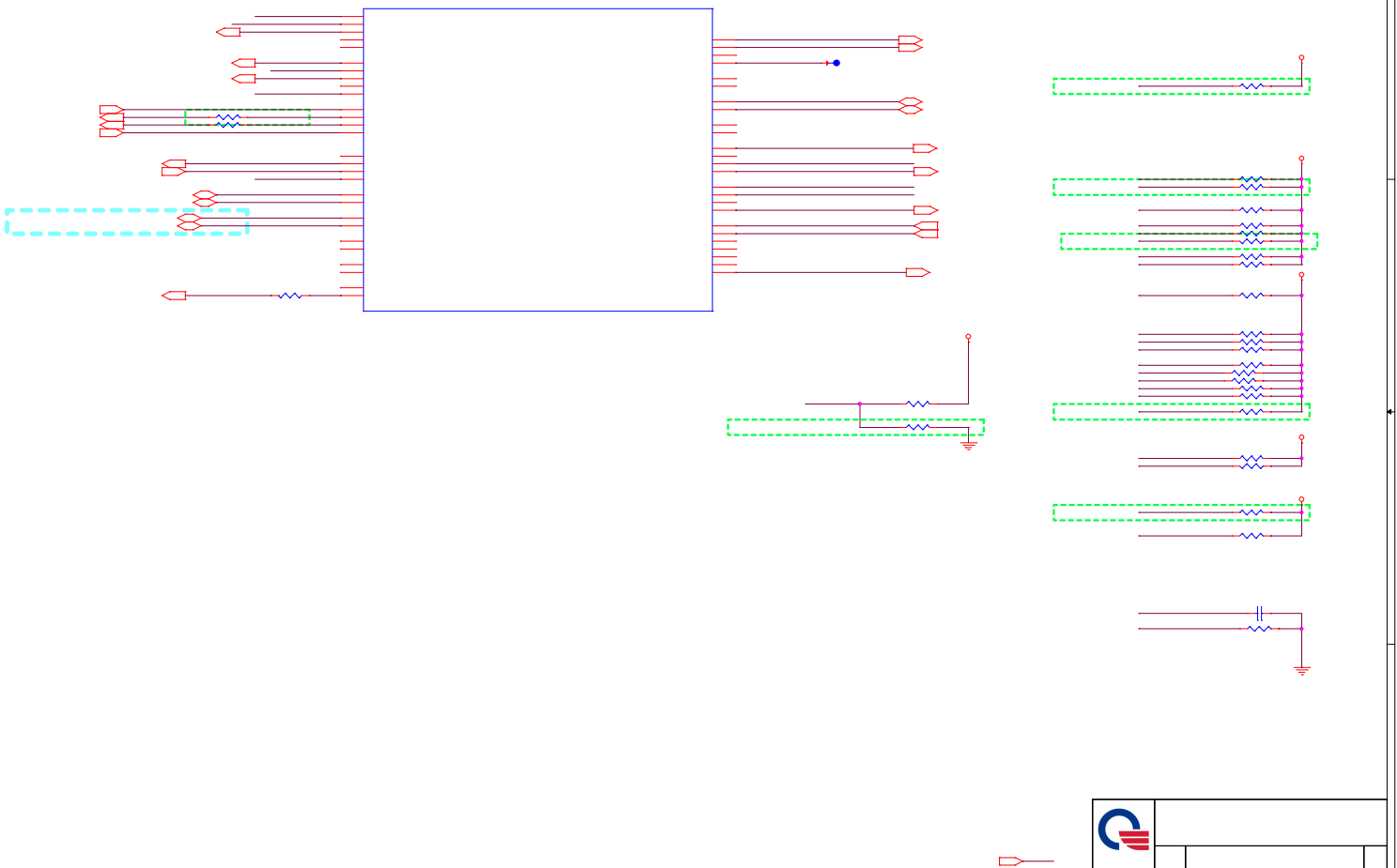


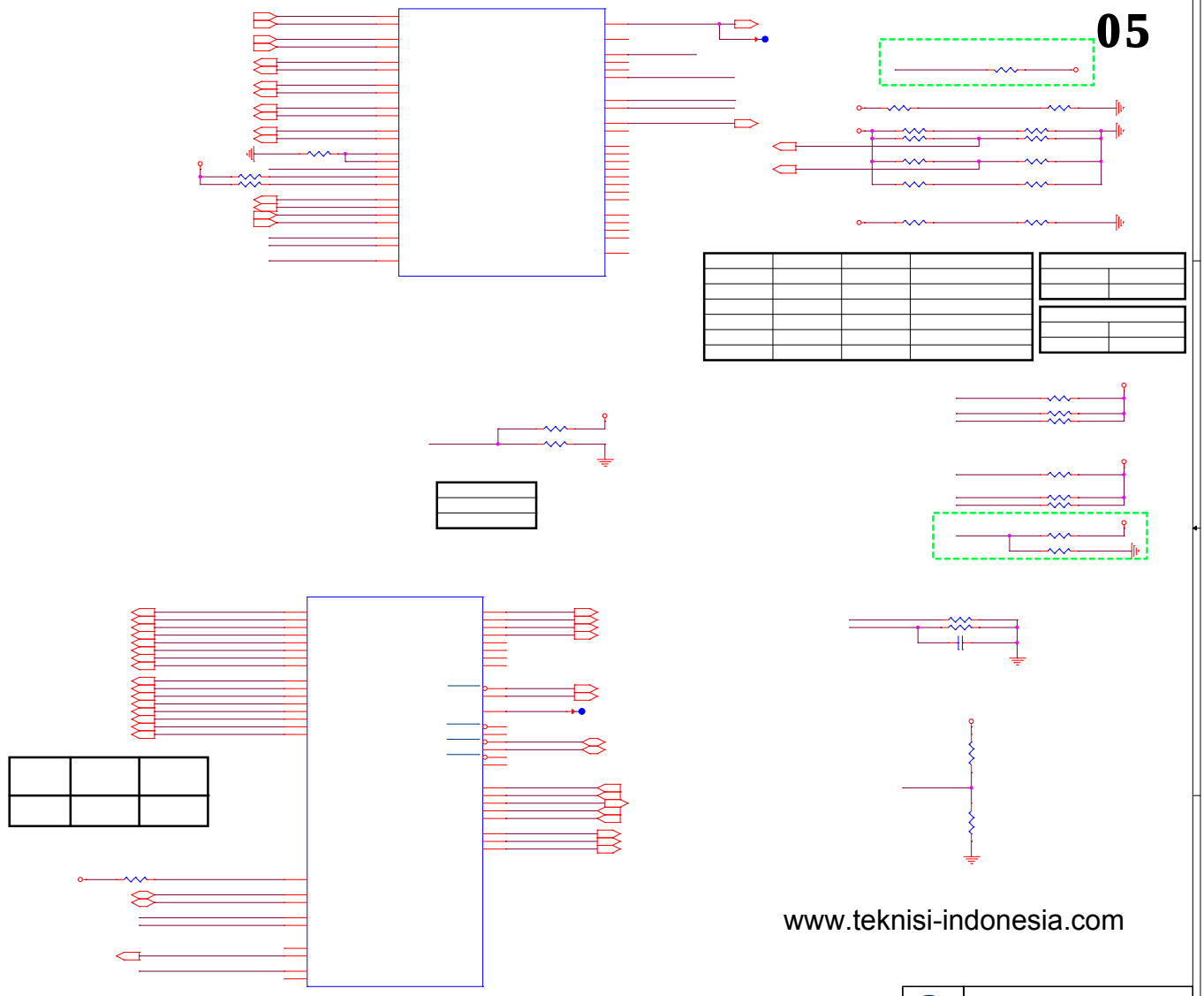


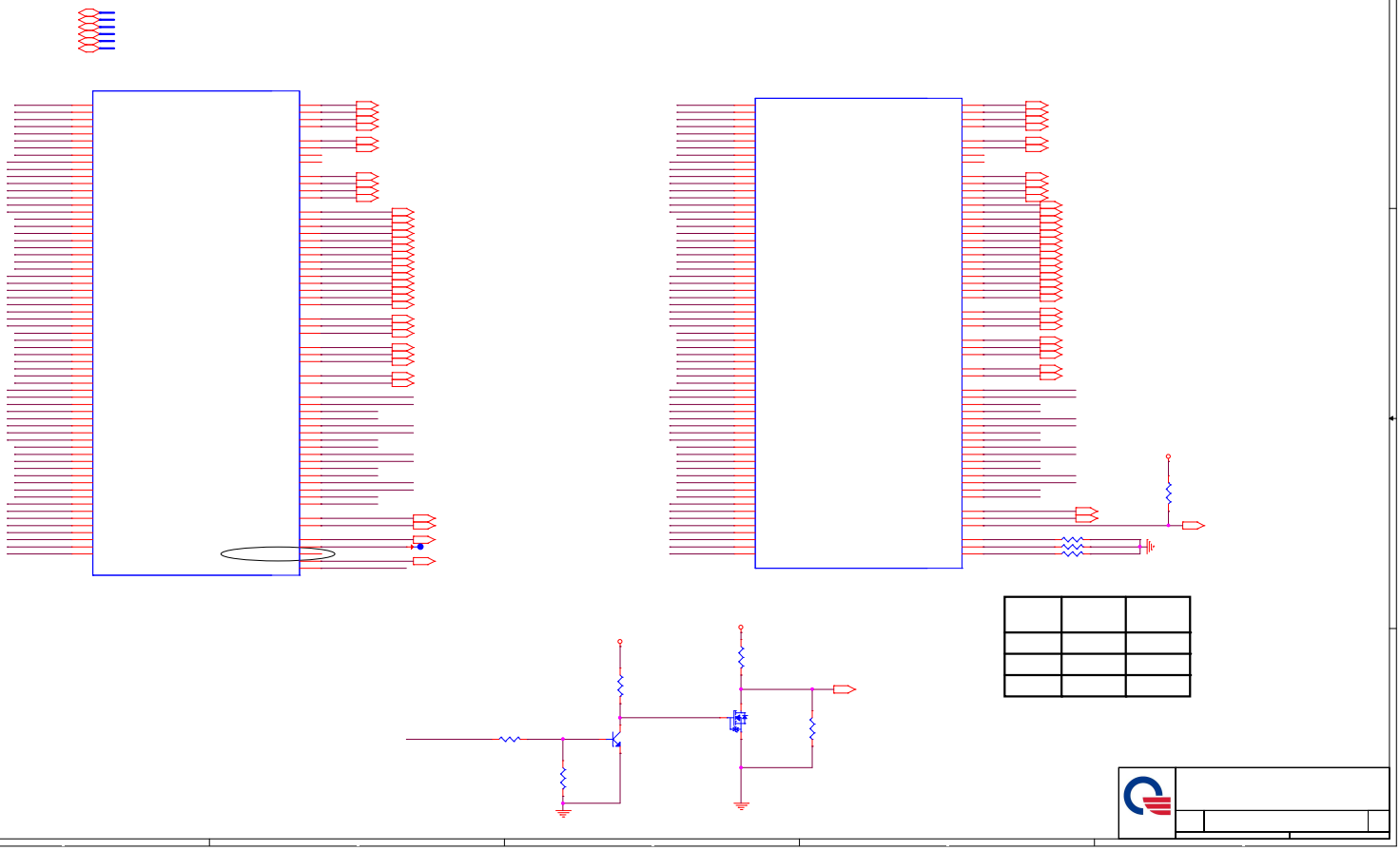


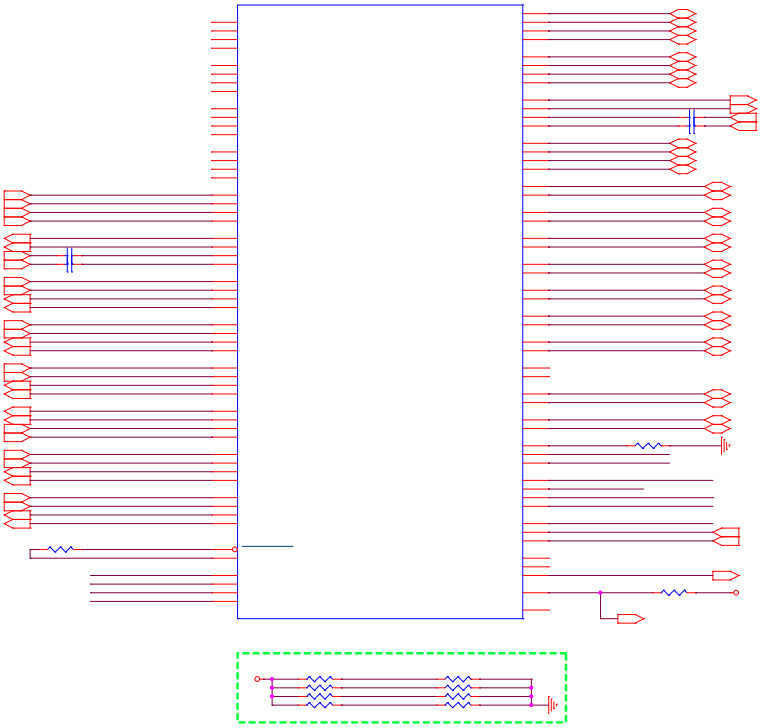


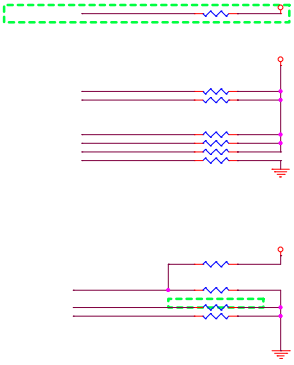


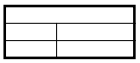


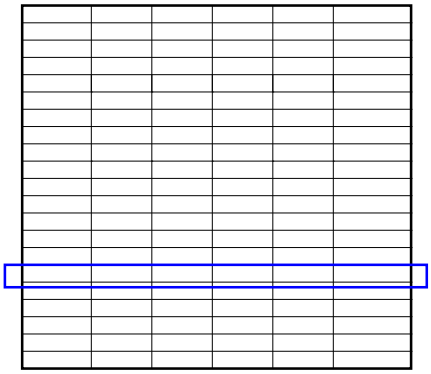


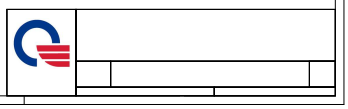


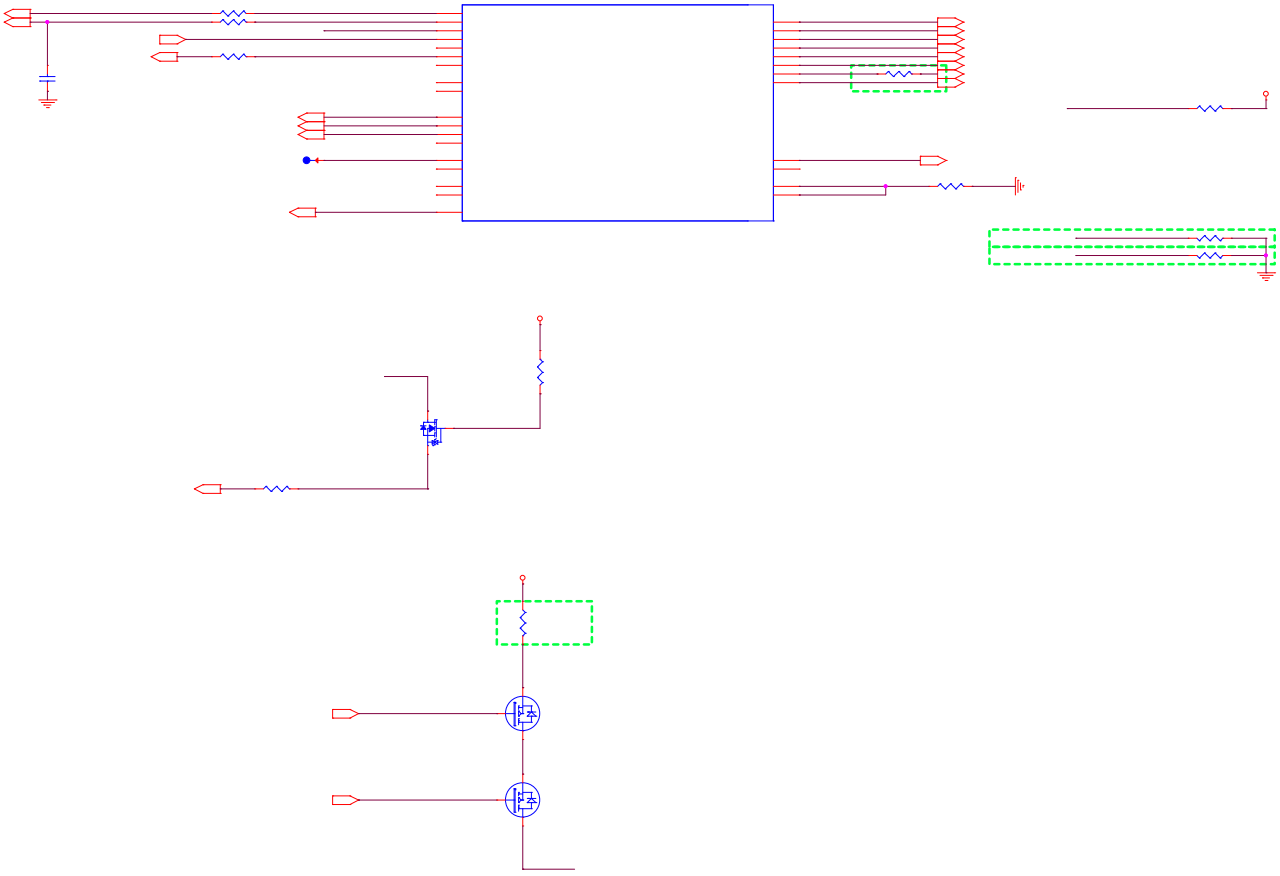


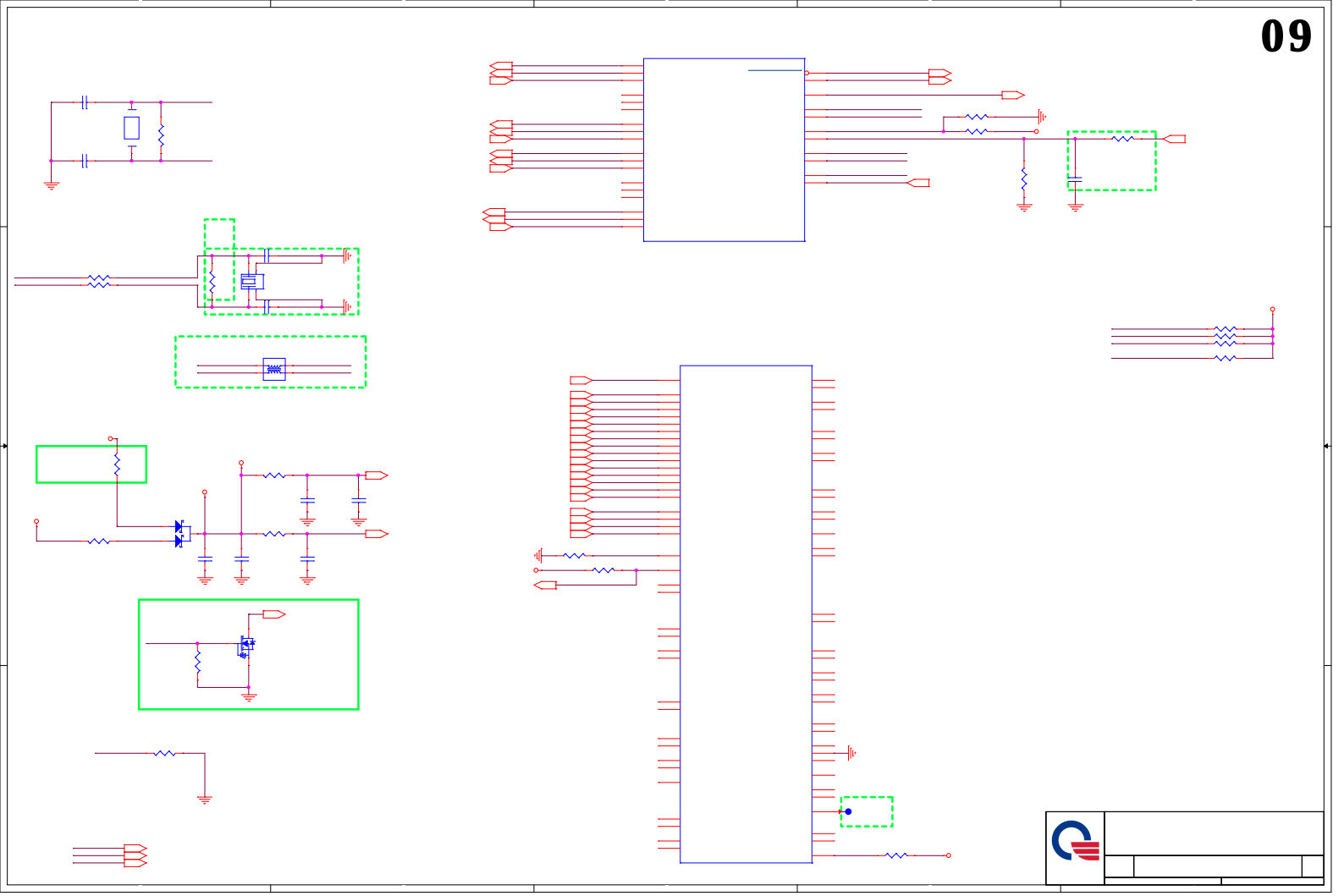


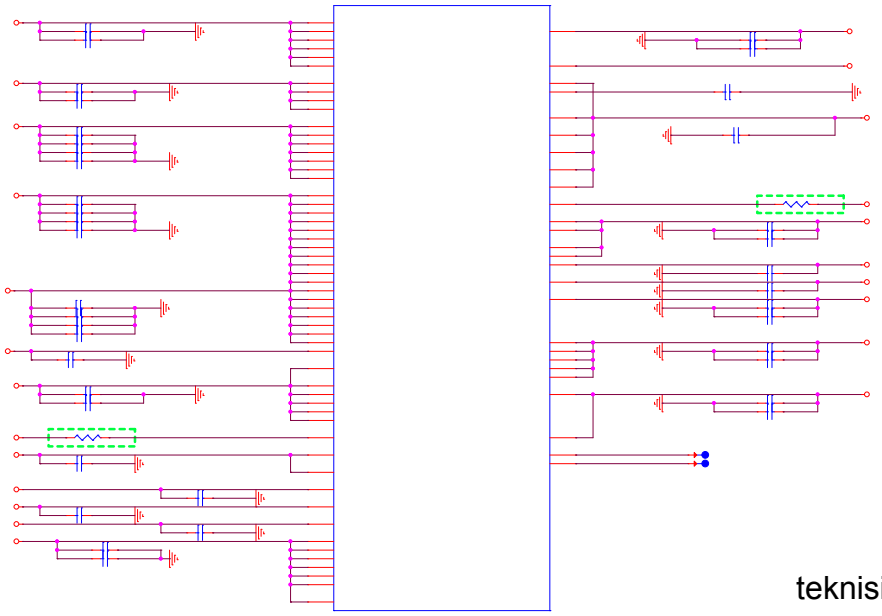


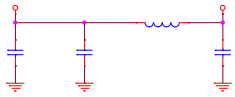


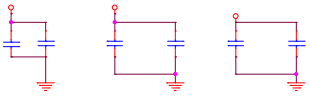


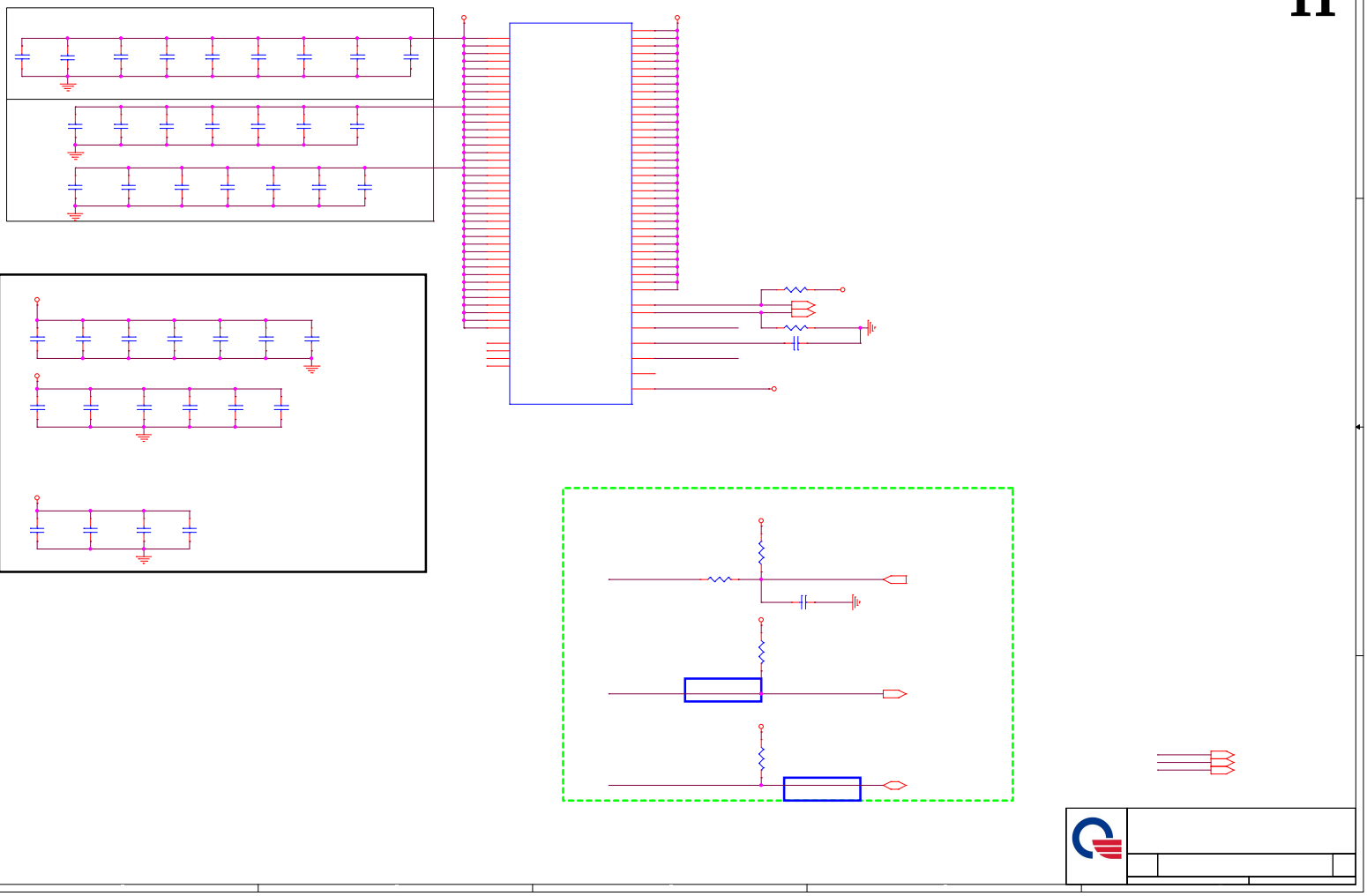


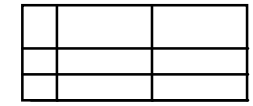


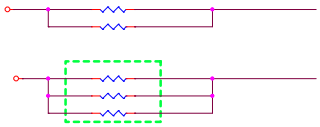


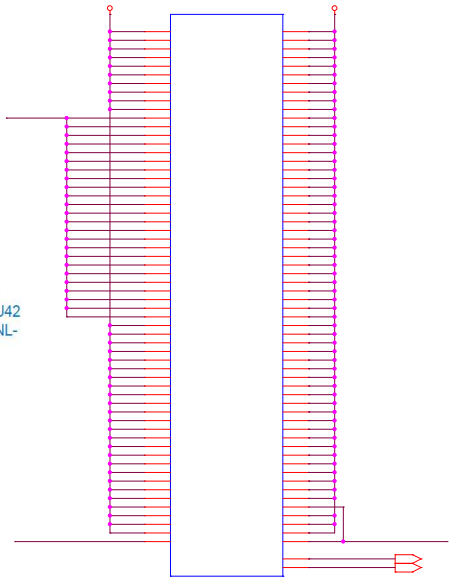


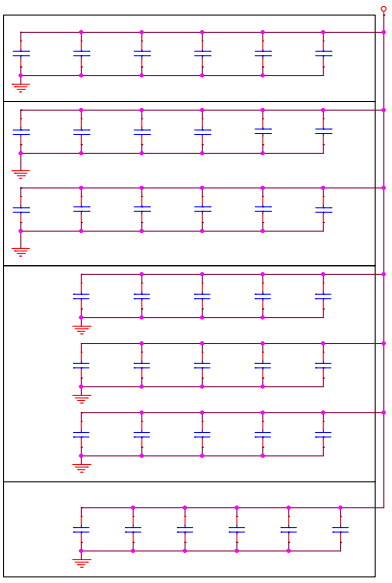




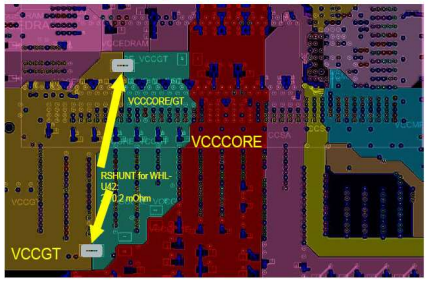






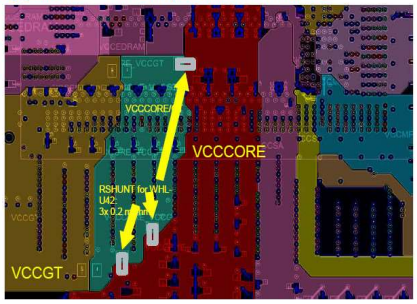


Routing guideline for RSHUNT placement for WHL ES1, CFL43e and CNLU22

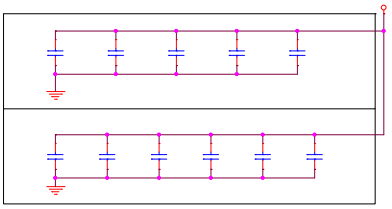


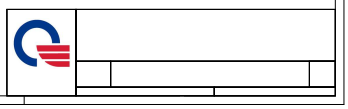
Place 2x 0.2 mOhm RSHUNT for WHL-U42 (ES1)/CFL-U43e/CNL-U22

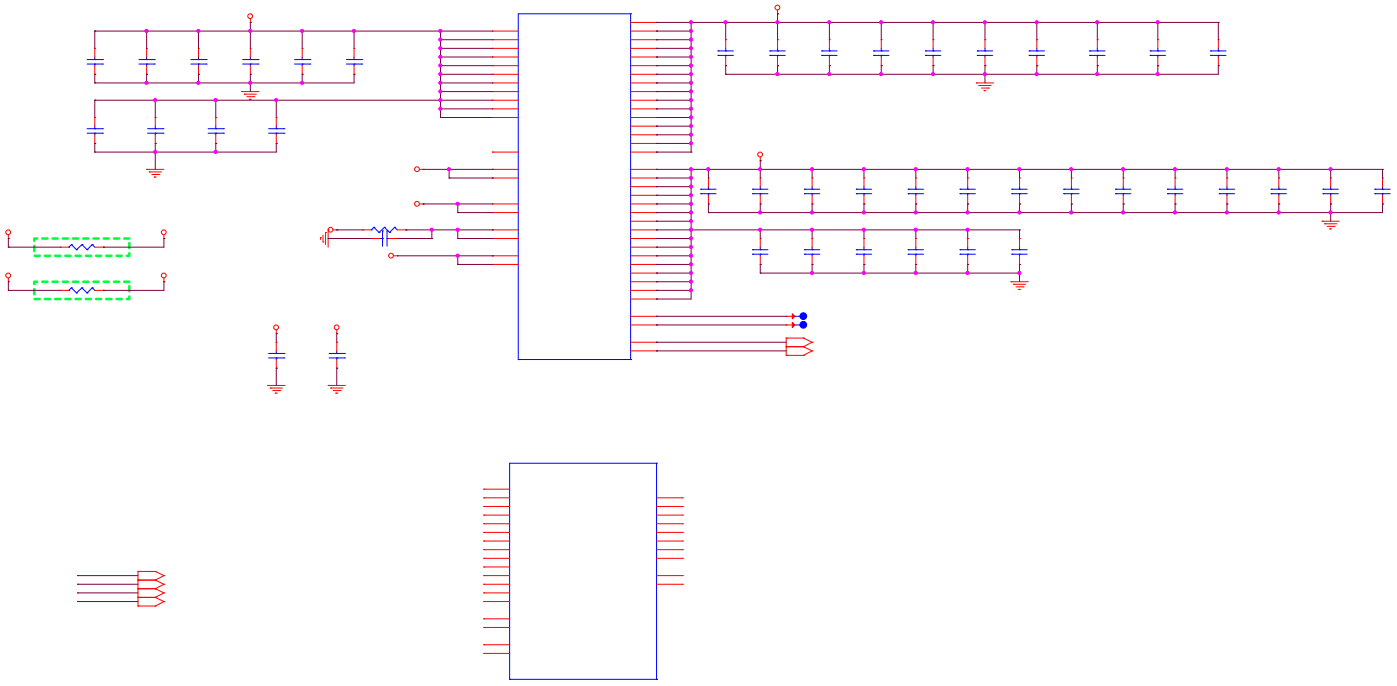
Routing guideline for RSHUNT placement for WHL ES2

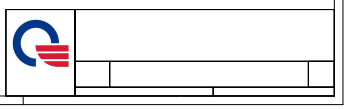


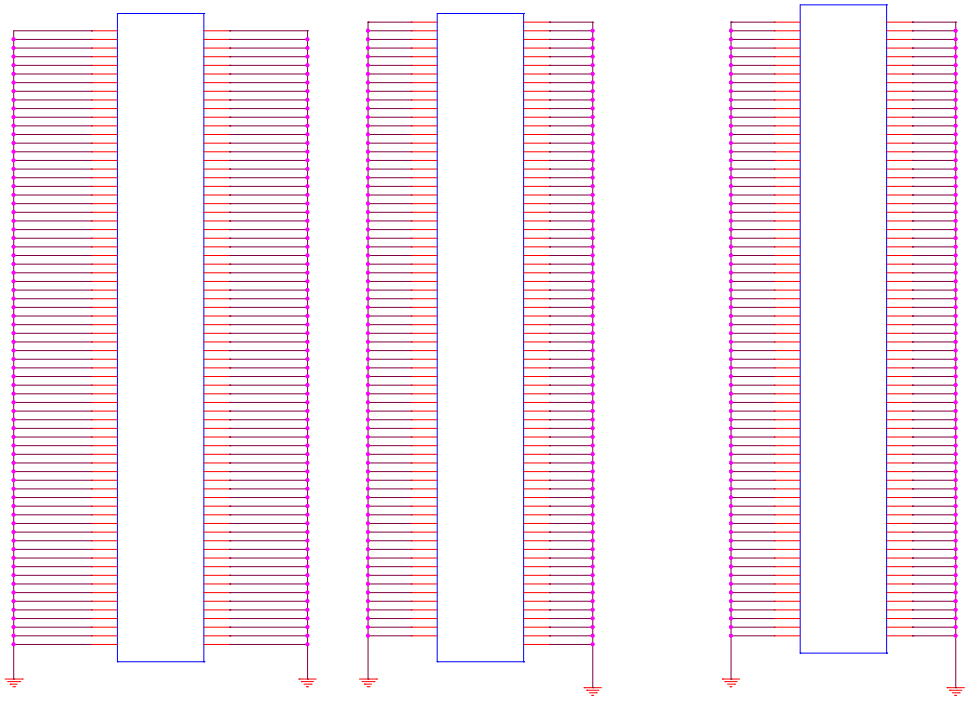
Place 3x 0.2 mOhm RSHUNT for WHL-U42 (ES2)

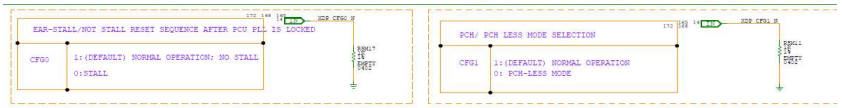




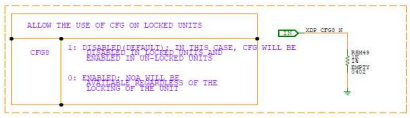


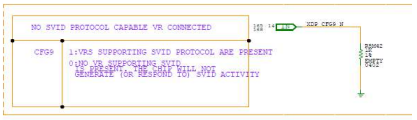


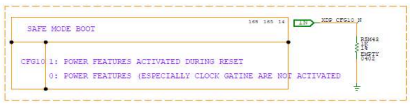


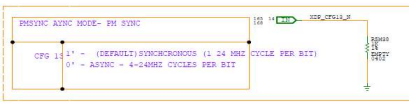

EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED
CFG0
1:(DEFAULT) NORMAL OPERATION; NO STALL
0:STALL

PCH/ PCH LESS MODE SELECTION
CFG1
1:(DEFAULT) NORMAL OPERATION
0: PCH-LESS MODE

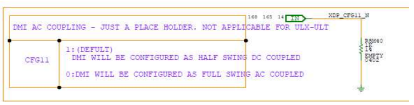

ALLOW THE USE OF CFG ON LOCKED UNITS
CFG8
1: DISABLED(DEFAULT) - IN THIS CASE, CFG WILL BE ENABLED IN UN-LOCKED UNITS
0: ENABLED; NCA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

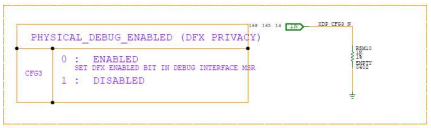

NO SVID PROTOCOL CAPABLE VR CONNECTED
CFG9
1:VRS SUPPORTING SVID PROTOCOL ARE PRESENT
0:NO VR SUPPORTING SVID PROTOCOL ARE PRESENT, THE PEAK WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

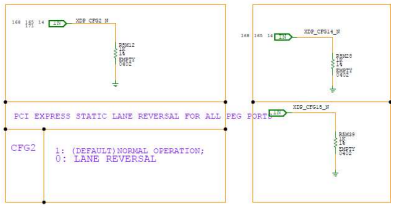

SAFE MODE BOOT
CFG10
1: POWER FEATURES ACTIVATED DURING RESET
0: POWER FEATURES (ESPECIALLY CLOCK GATING ARE NOT ACTIVATED

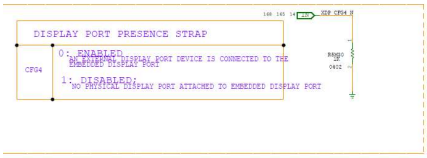

PMSYNC ASYNC MODE- PM SYNC
CFG 13
1' - (DEFAULT)SYNCHCRONOUS (1 24 MHZ CYCLE PER BIT)
0' - ASYNC - 4-24MHZ CYCLES PER BIT

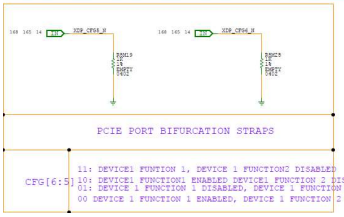

PM SYNC LEGACY
CFG 12
1' - (DEFAULT) PMSYNC 2.0
0' - LEGACY

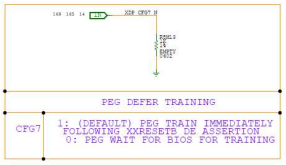

DMI AC COUPLING - JUST A PLACE HOLDER. NOT APPLICABLE FOR ULX-ULT
CFG11
1:(DEFAULT)
DMI WILL BE CONFIGURED AS HALF SWING DC COUPLED
0:DMI WILL BE CONFIGURED AS FULL SWING AC COUPLED

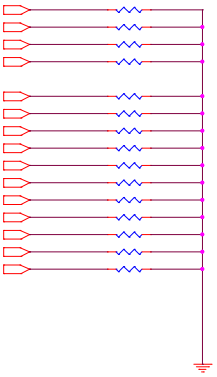

PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)
CFG3
0 : ENABLED
SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
1 : DISABLED

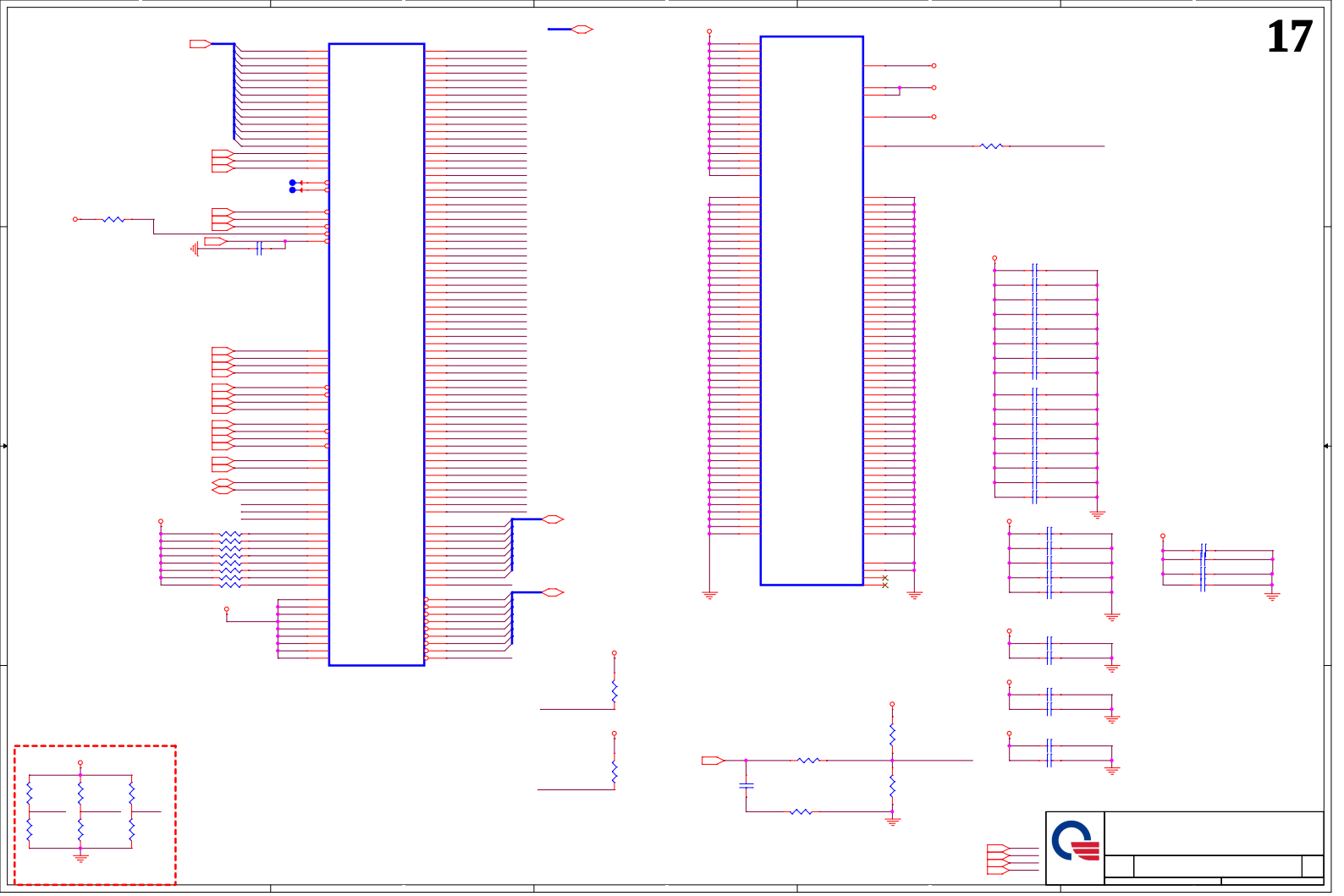

PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS
CFG2
1: (DEFAULT)NORMAL OPERATION;
0: LANE REVERSAL

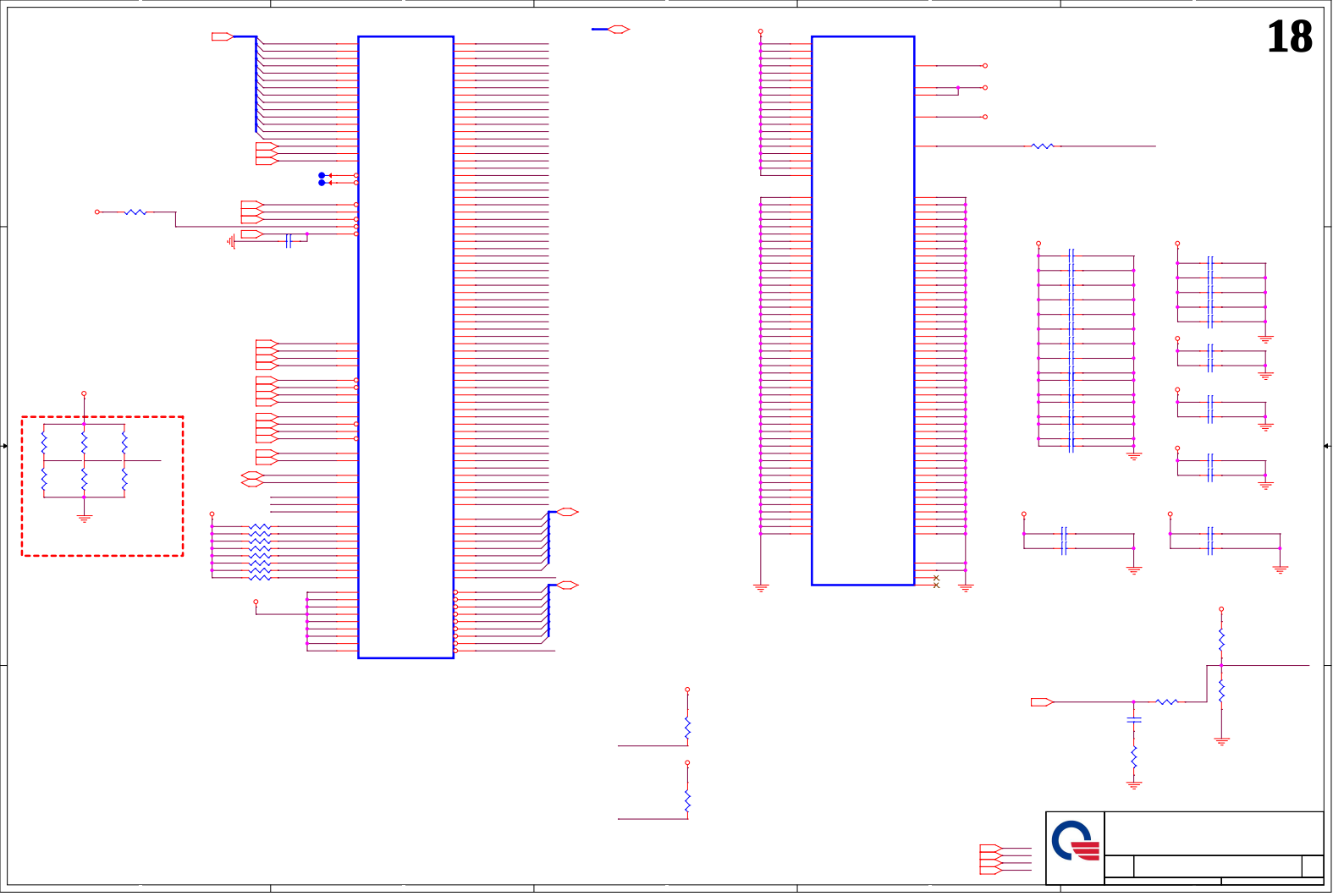

DISPLAY PORT PRESENCE STRAP
CFG4
0: ENABLED
1: DISABLED;

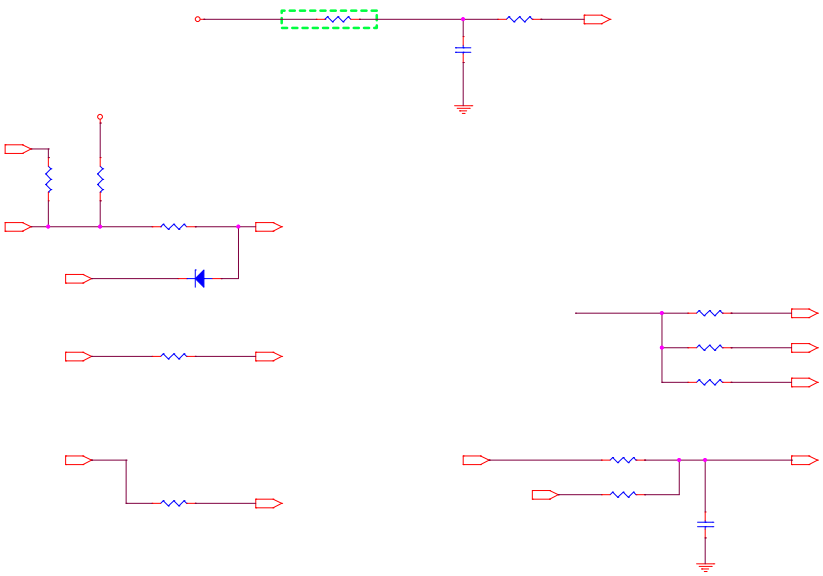

PCIE PORT BIFURCATION STRAPS
CFG[6:5]
11: DEVICE1 FUNTION 1, DEVICE 1 FUNCTION2 DISABLED
10: DEVICE1 FUNCTION1 ENABLED DEVICE1 FUNCTION 2 DISABLED
01: DEVICE 1 FUNCTION 1 DISABLED, DEVICE 1 FUNCTION 2 ENABLED
00 DEVICE 1 FUNCTION 1 ENABLED, DEVICE 1 FUNCTION 2 ENABLED

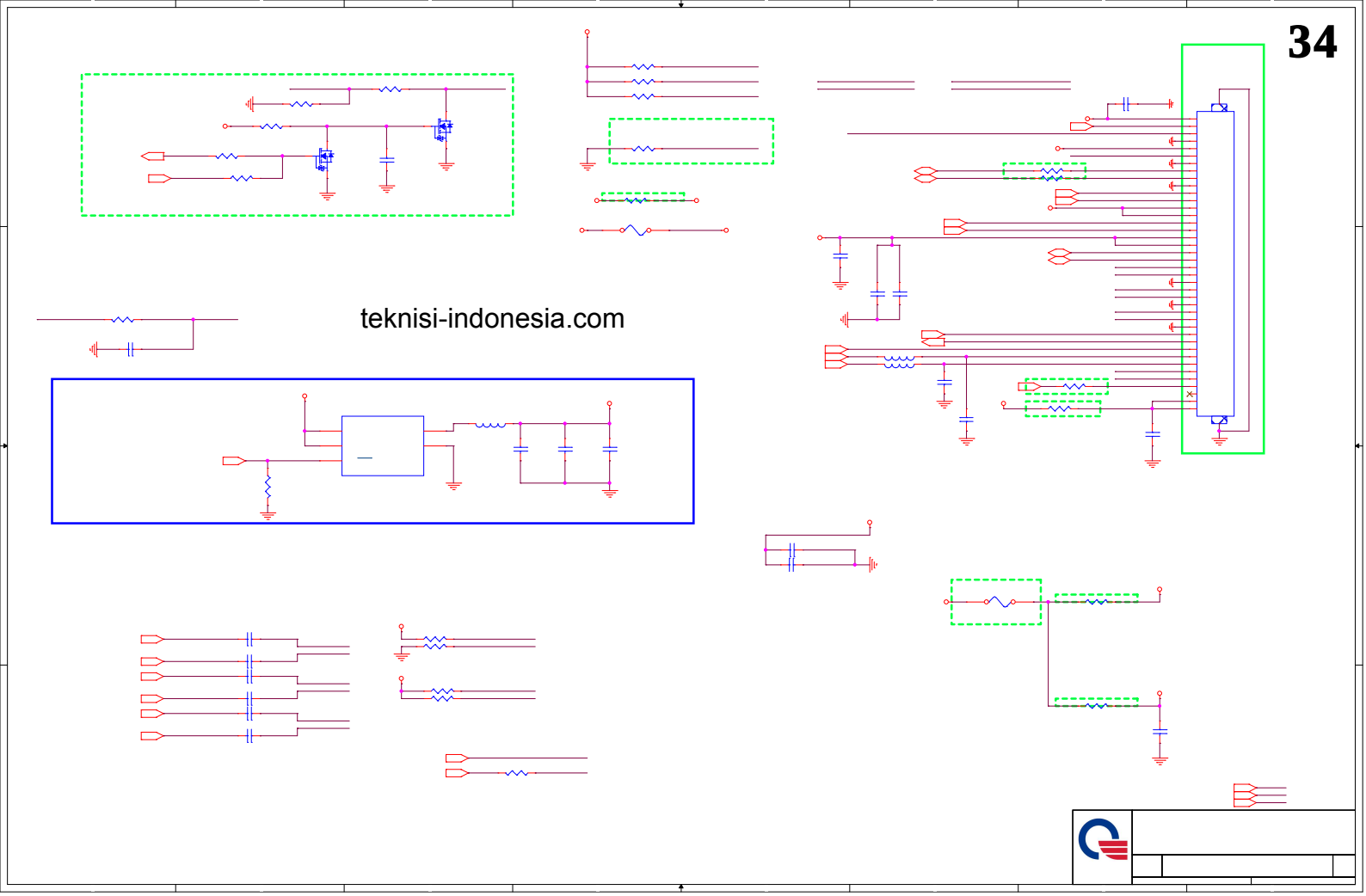

PEG DEFER TRAINING
CFG7
1: (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION
0: PEG WAIT FOR BIOS FOR TRAINING

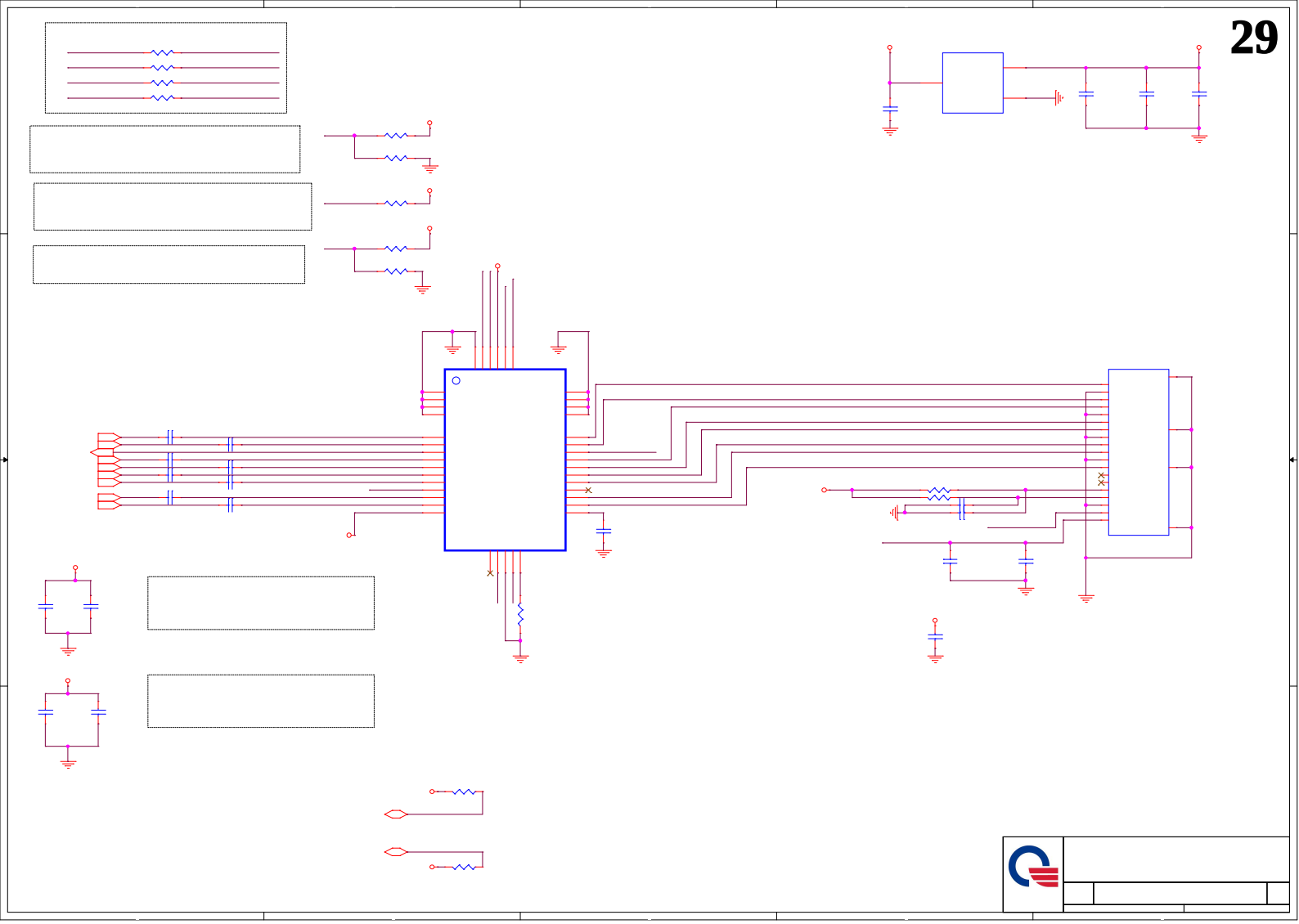


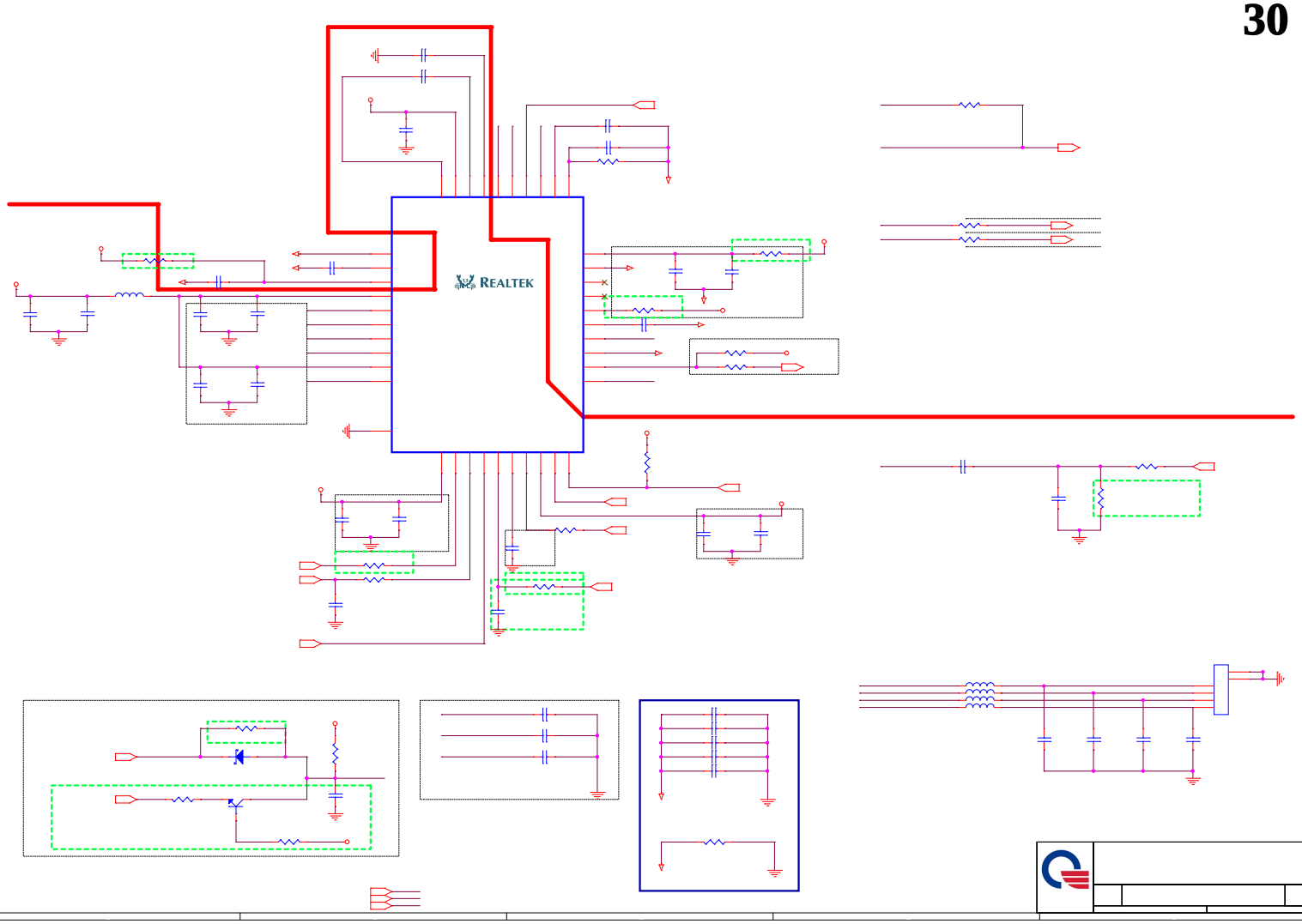


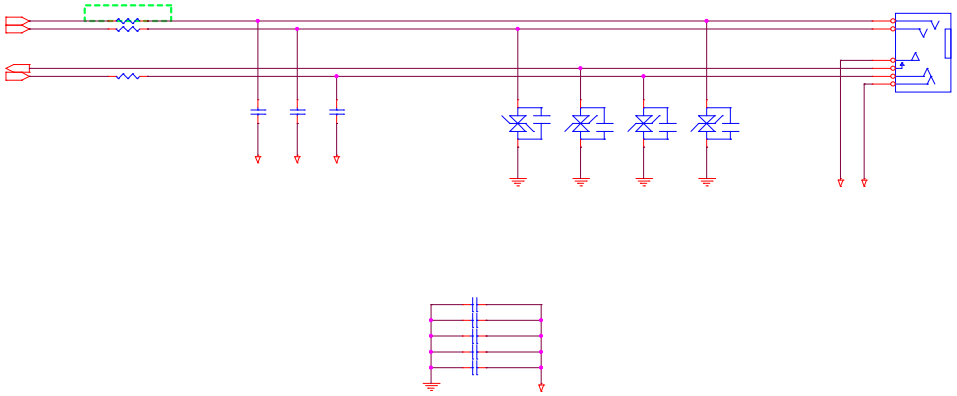




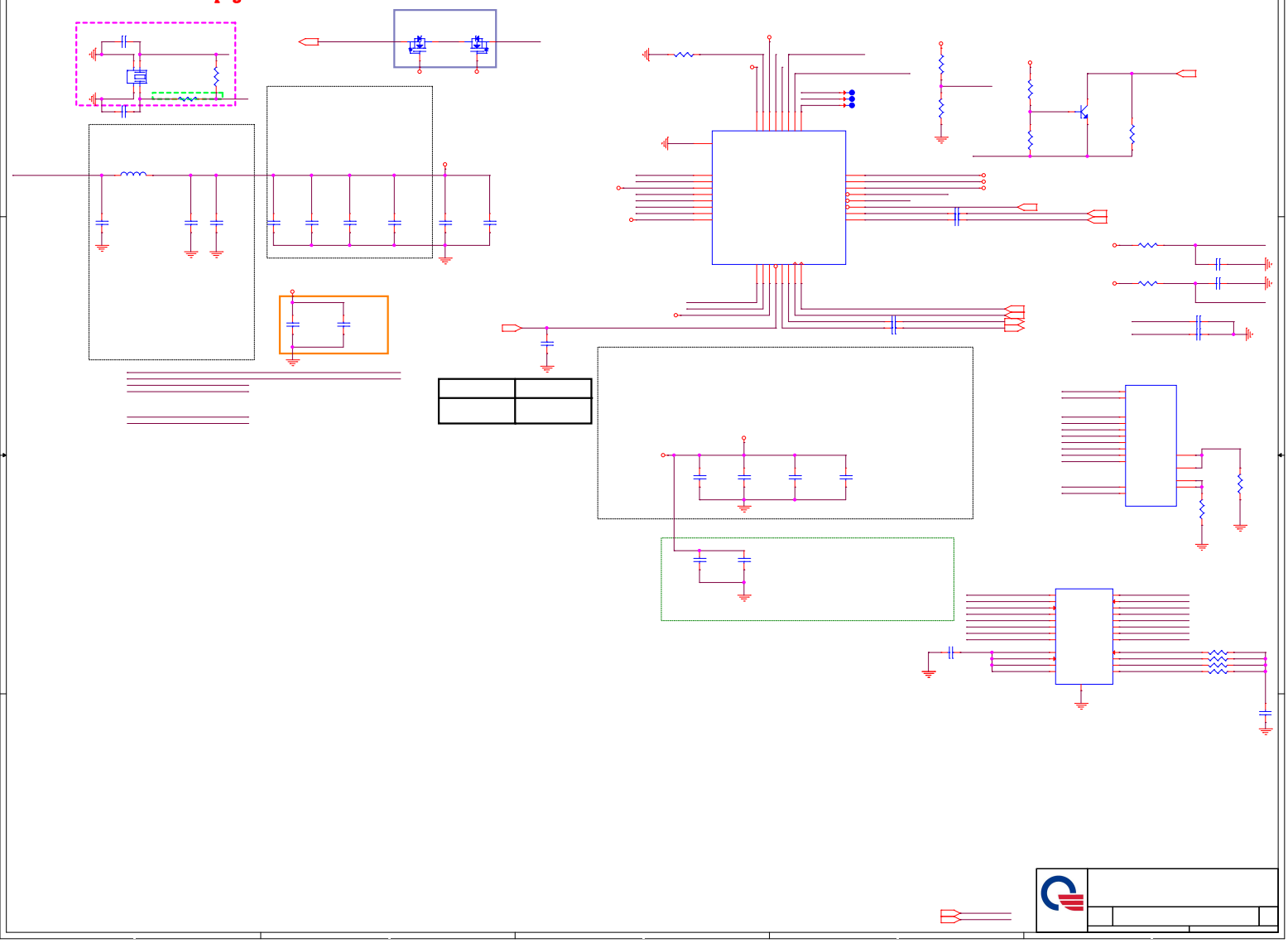


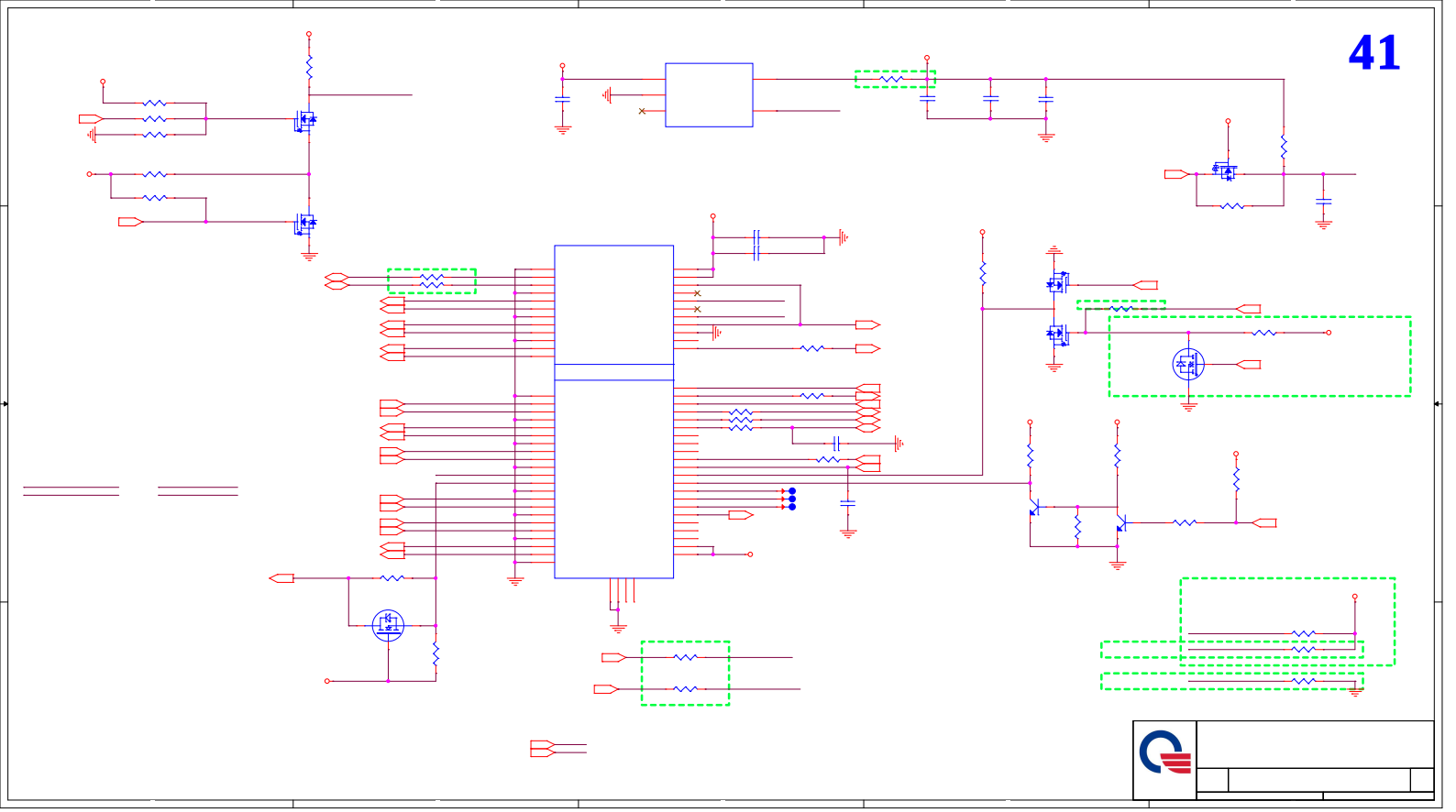


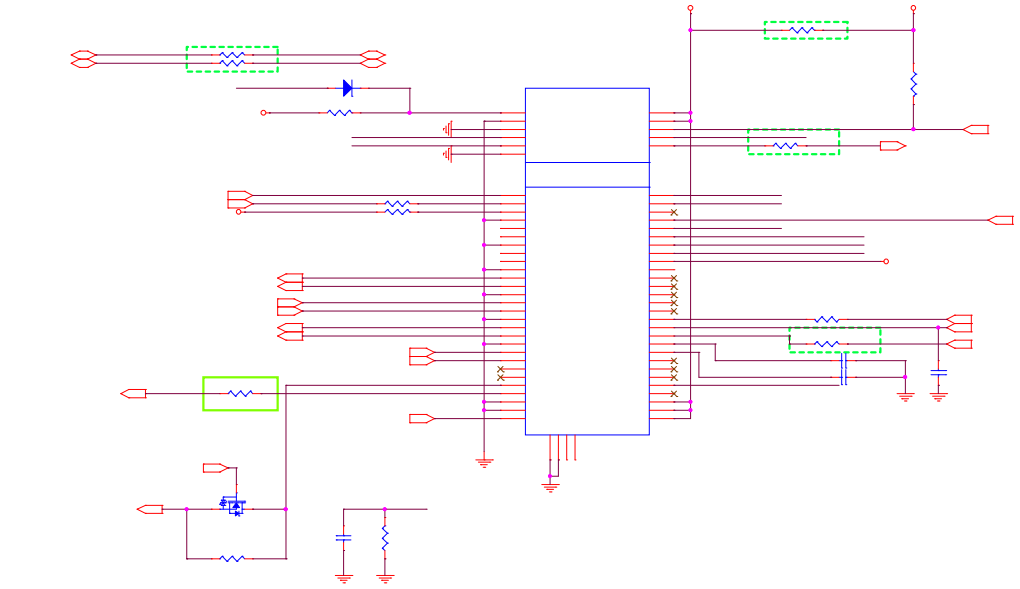

REALTEK

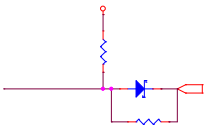


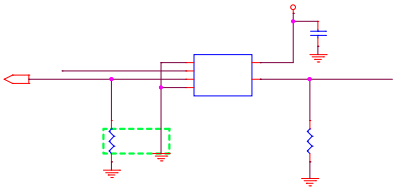
400 series 0930 whole page

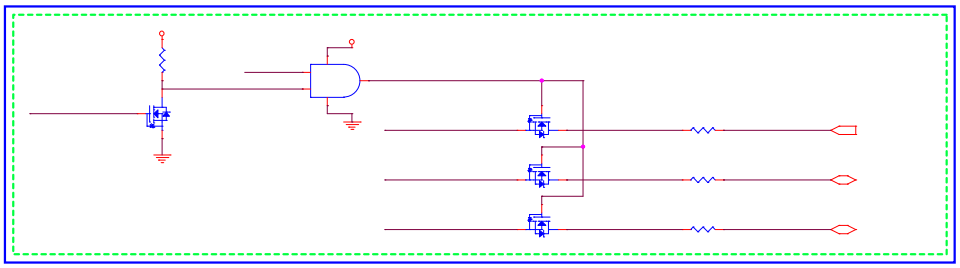


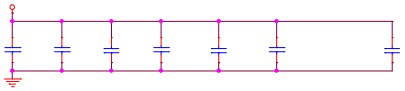


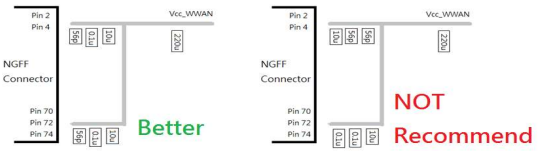


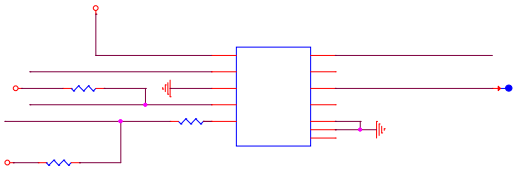


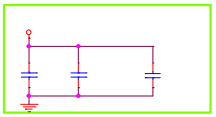




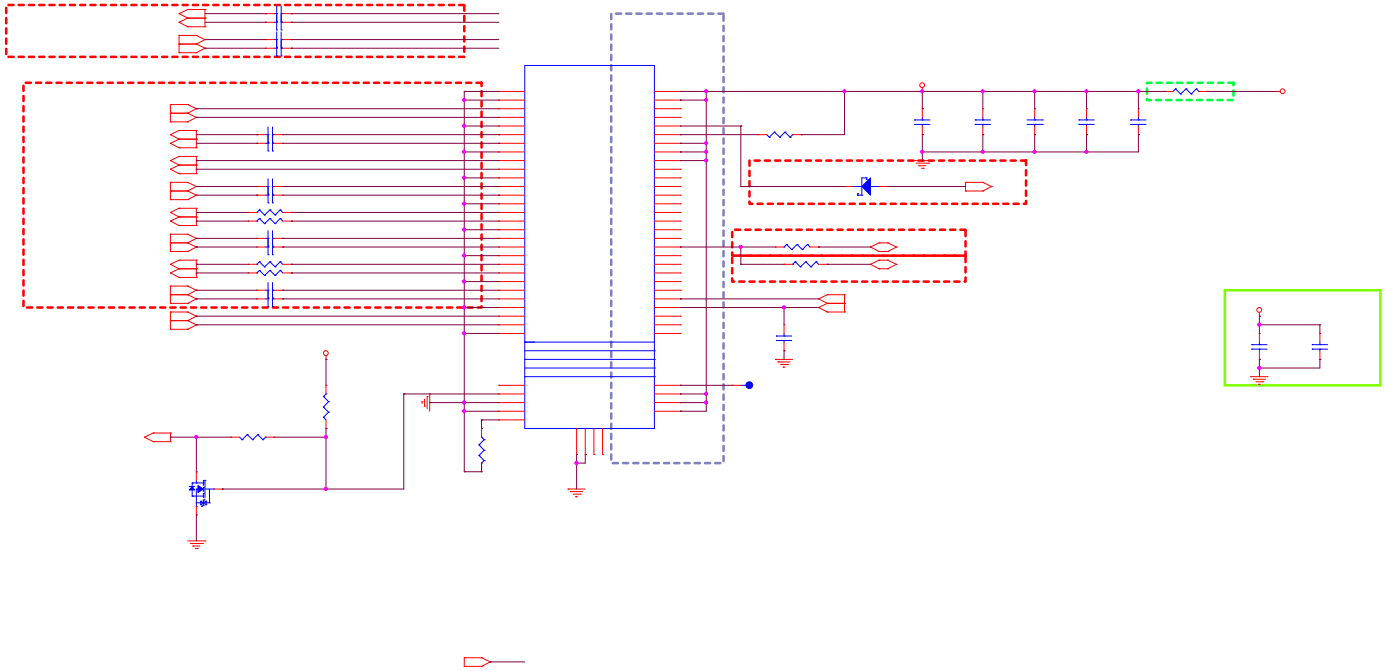


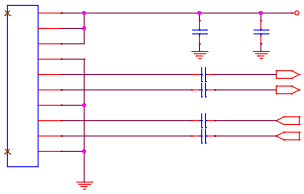


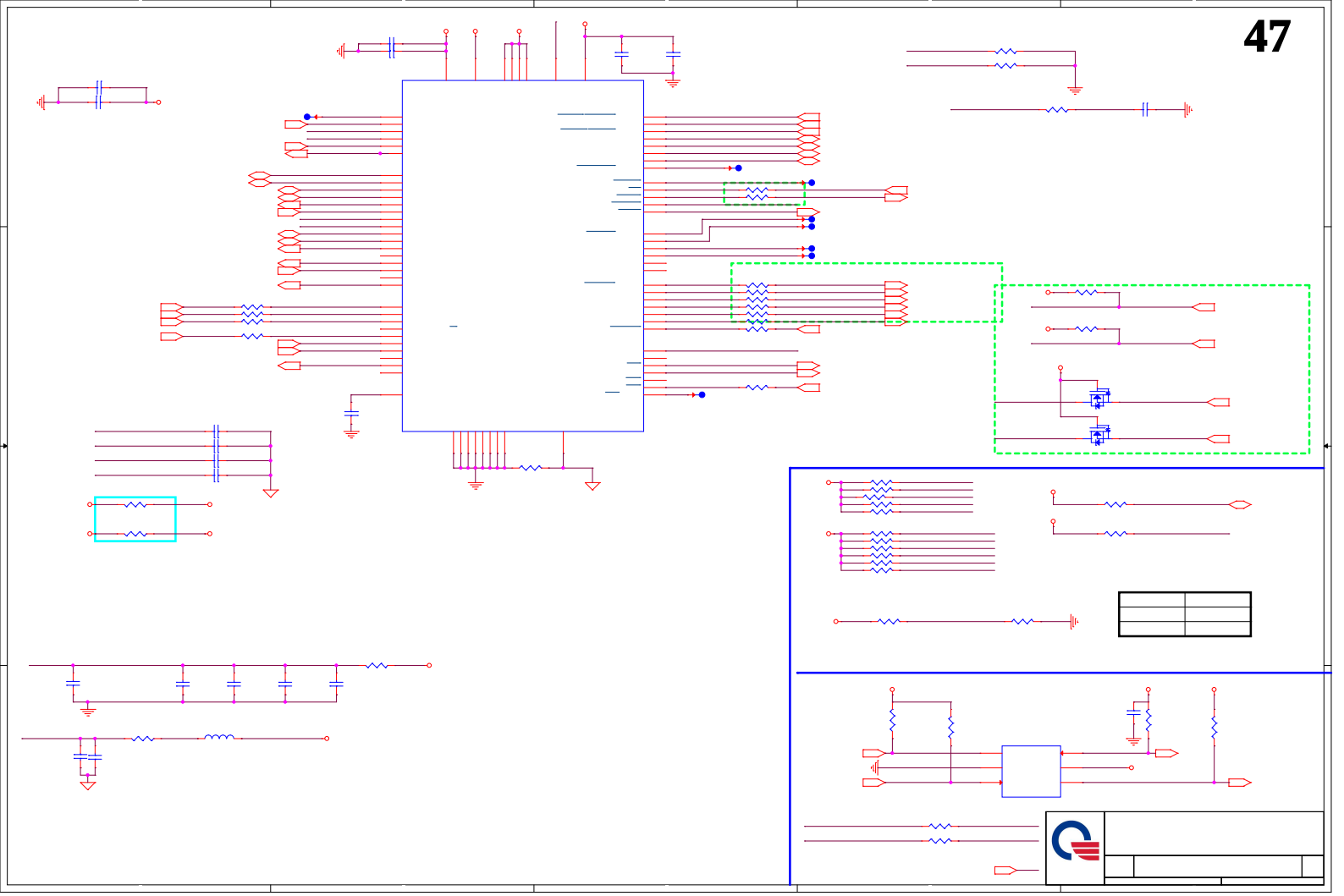


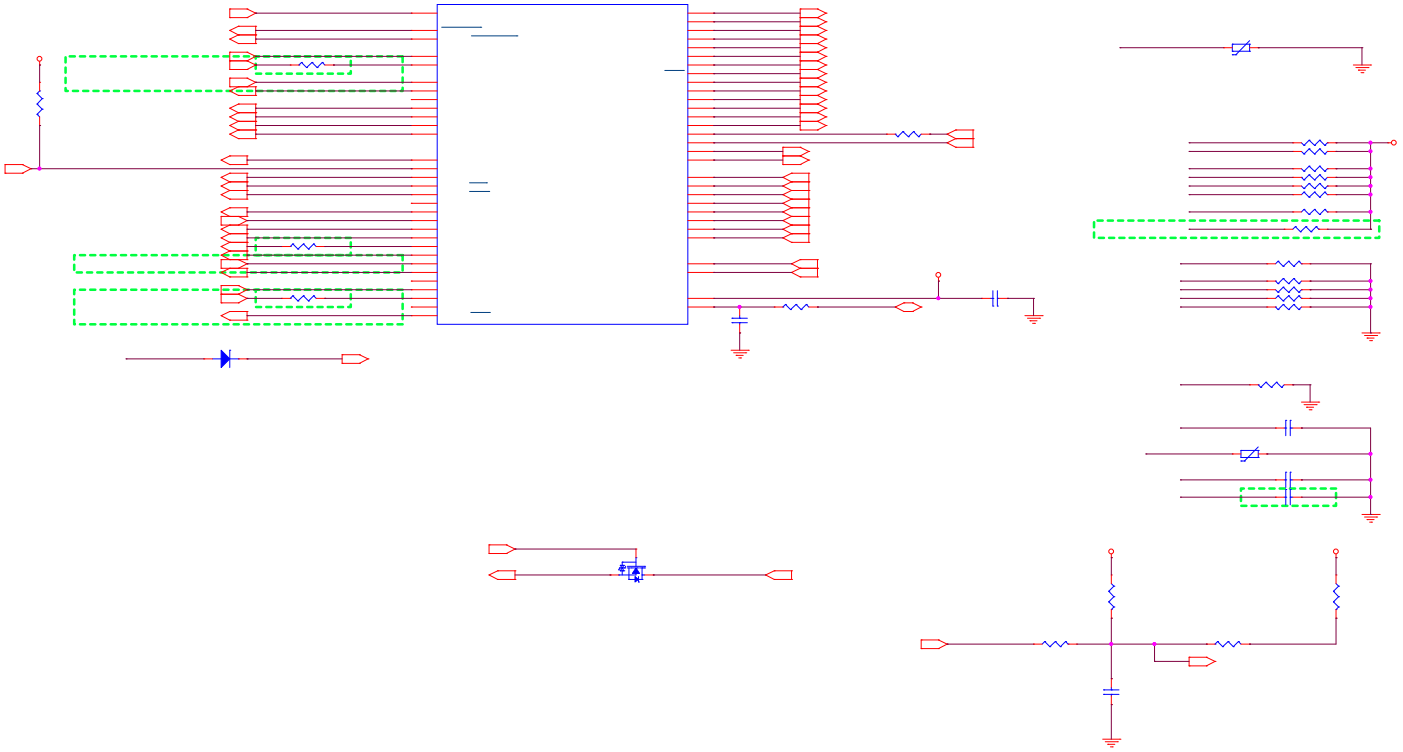


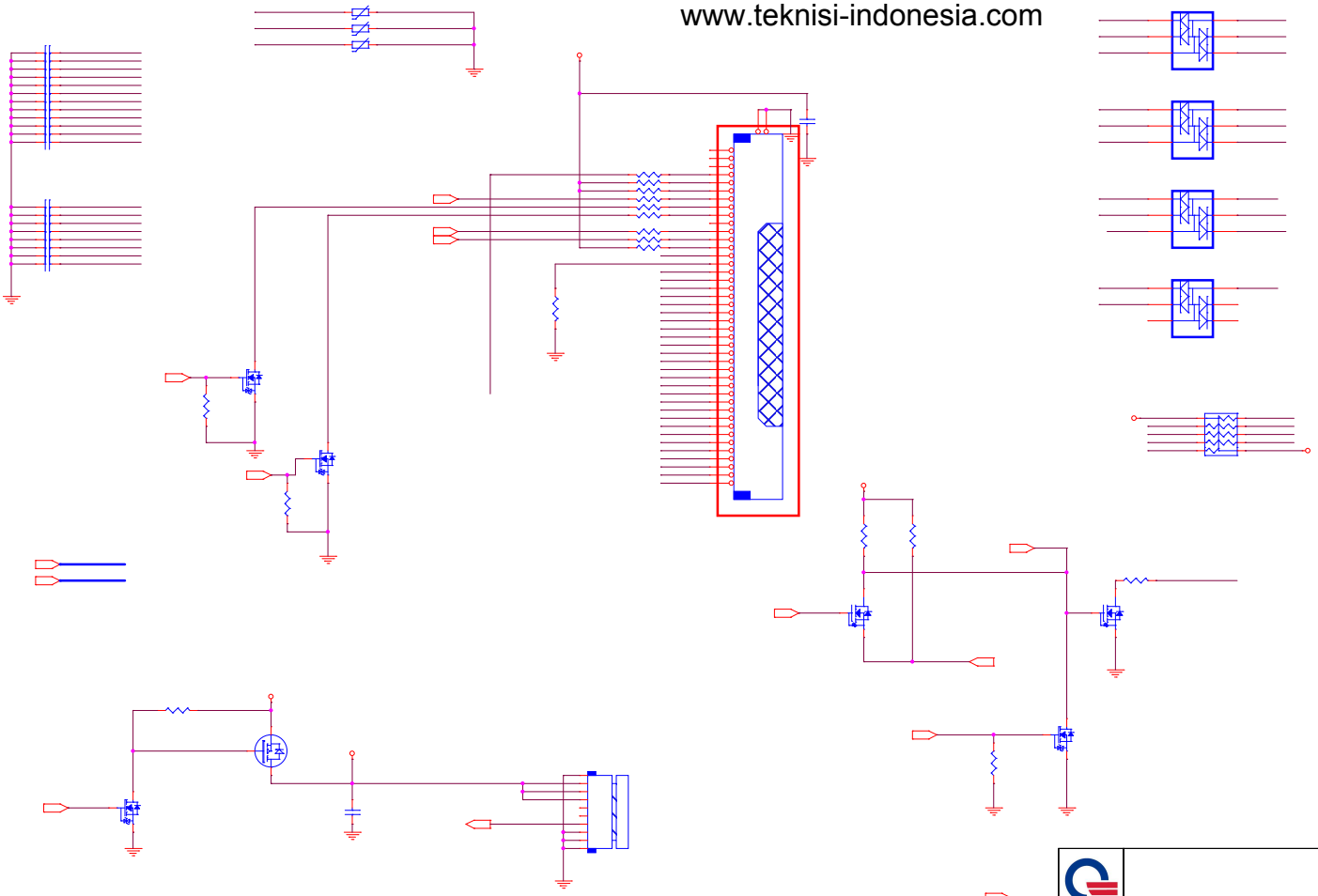
	+VCC	Power_On/Off (Pin6)	W_Disable (Pin8)	GPS_Disable (Pin26)
S0	ON	High	High	High
S3	ON	High	Low	Low
S4	ON	Low	Low	Low
S5	ON	Low	Low	Low

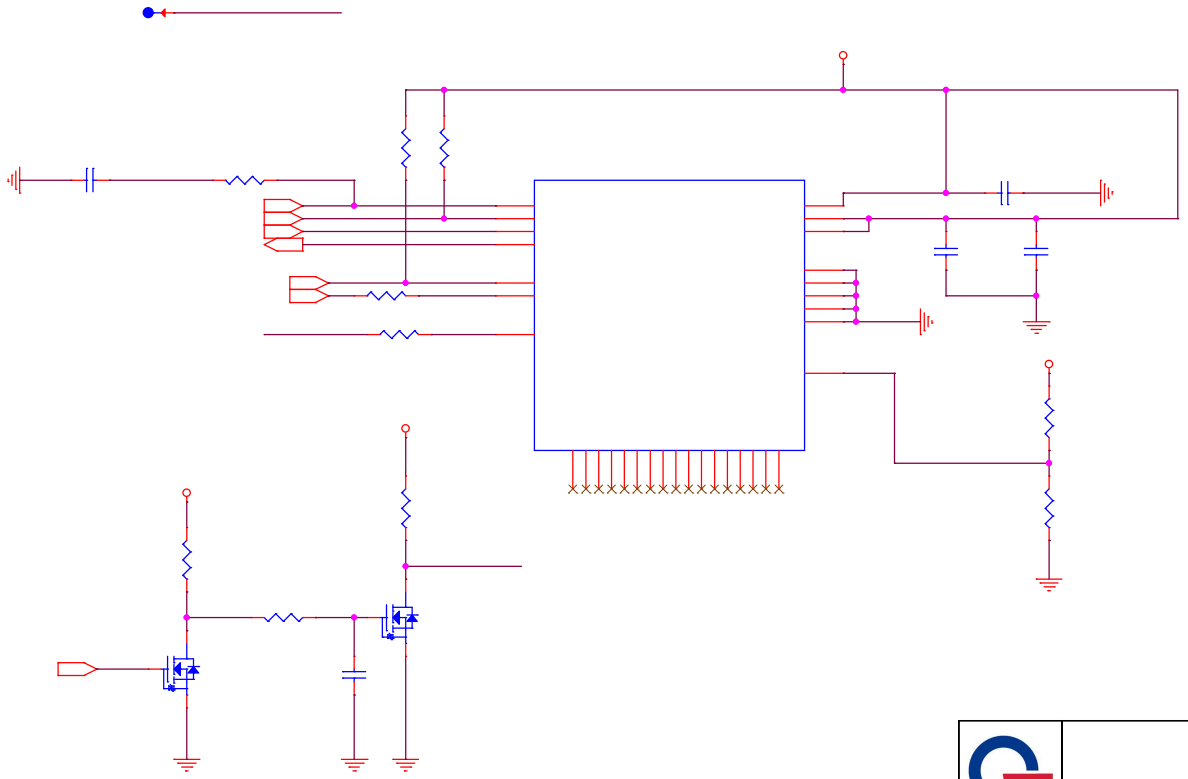


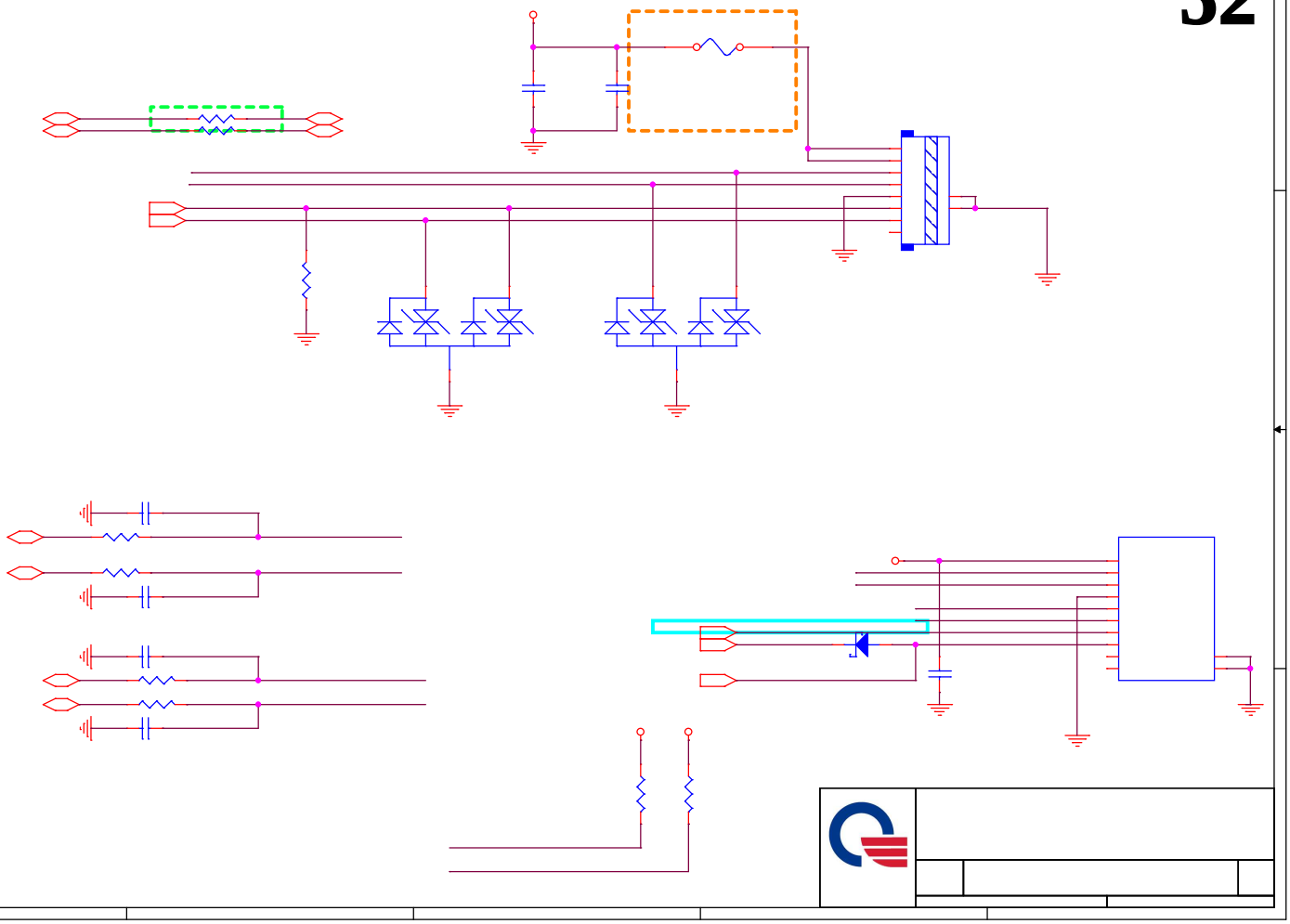


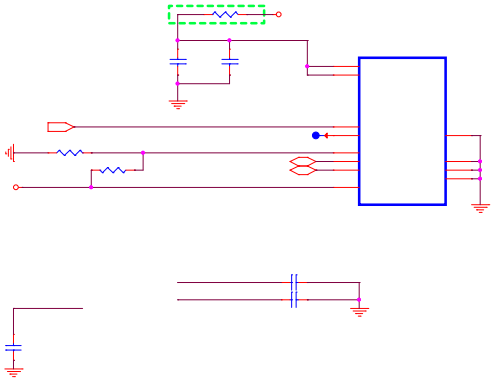


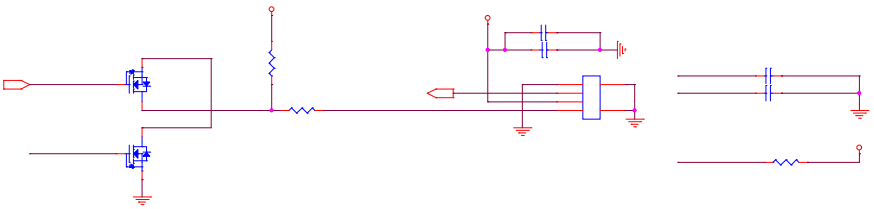


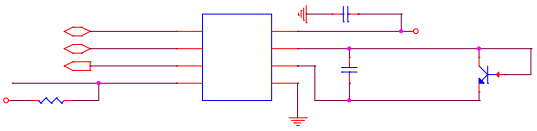


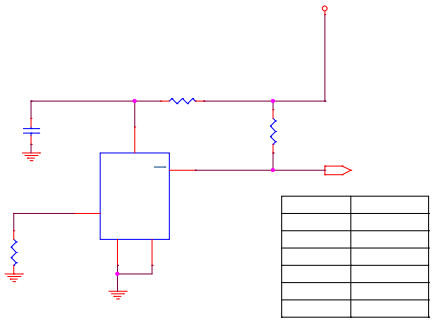


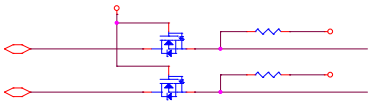


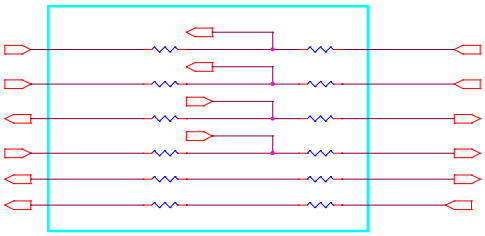


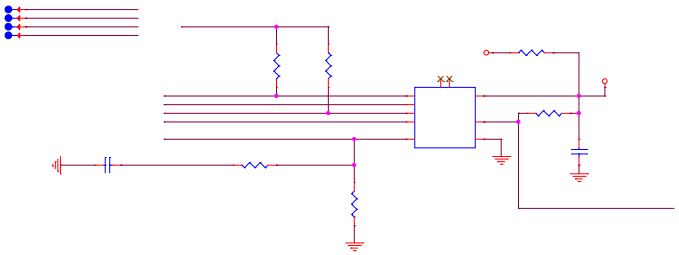


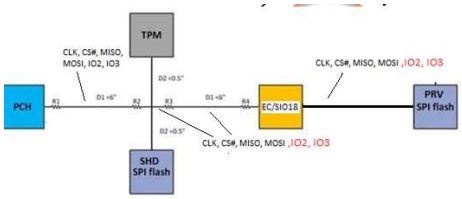








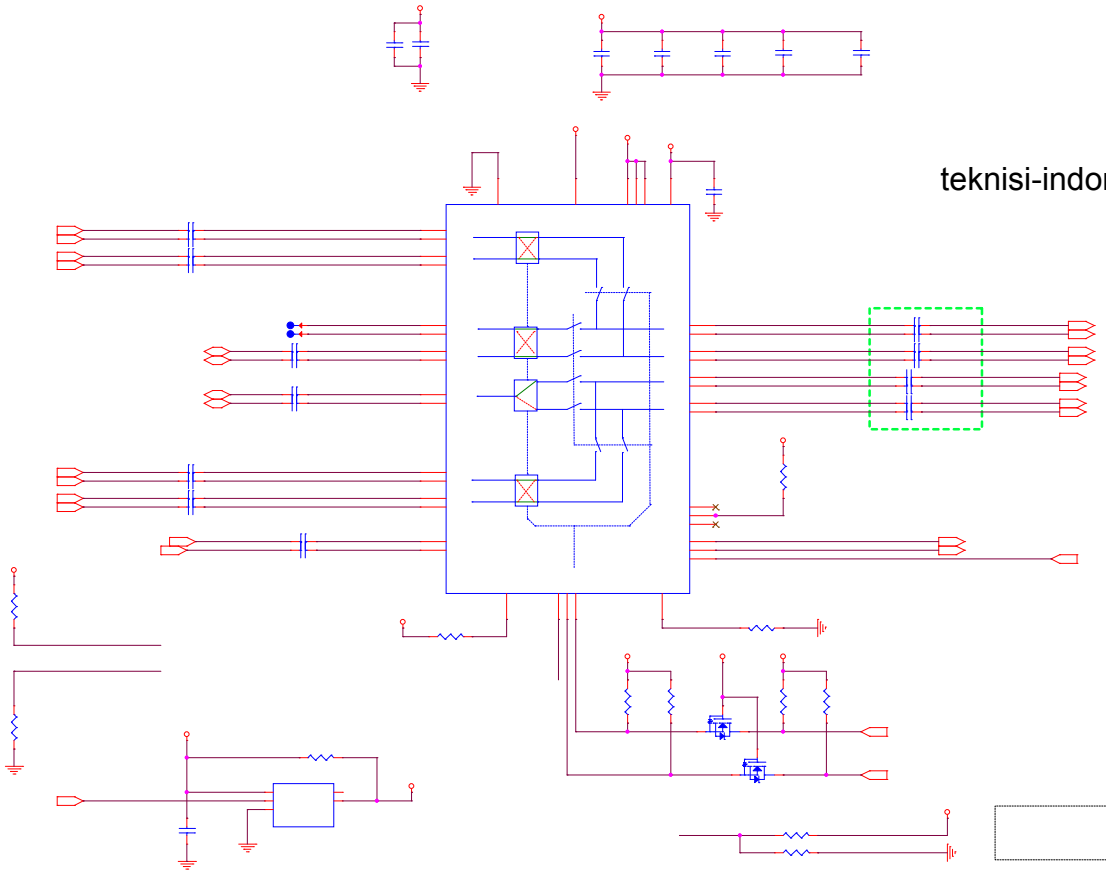


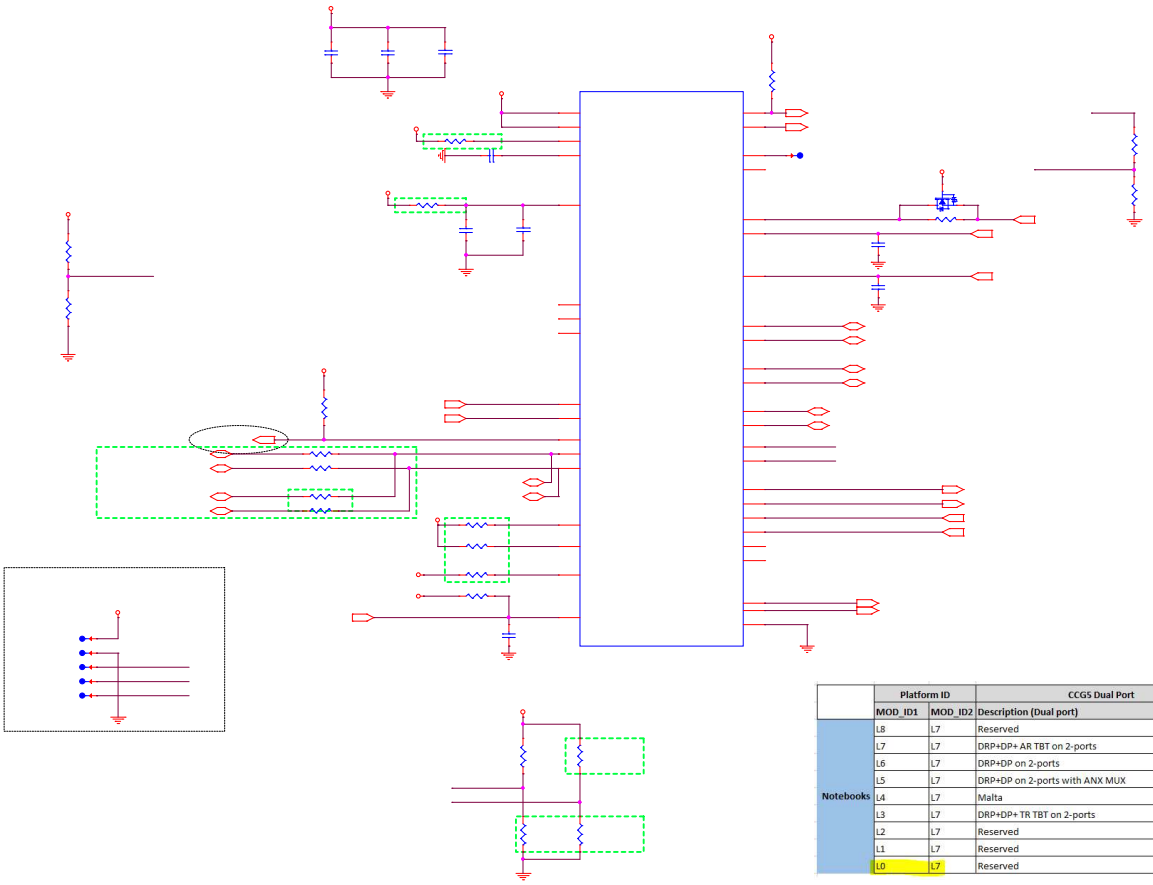


Based on EC18 testing: PCH to TPM/SPI flash = Quad I/O, SIO18 to SPI Flash = ~~Dual I/O~~ Quad I/O,
R1 = 4.7 ohm for CLK, CS#, MISO, MOSI; R1 = 0 ohm for IO2, IO3
R2 = 22 ohm for CLK, CS#, MISO, MOSI; R2 = 15 ohm for IO2, IO3
R3 = 22 ohm for CLK, CS#, MISO, MOSI; R3 = for IO2, IO3 22 ohm f
R4 = 4.7 ohm for CLK, CS#, MISO, MOSI; R4 = for IO2, IO3 4.7 ohm

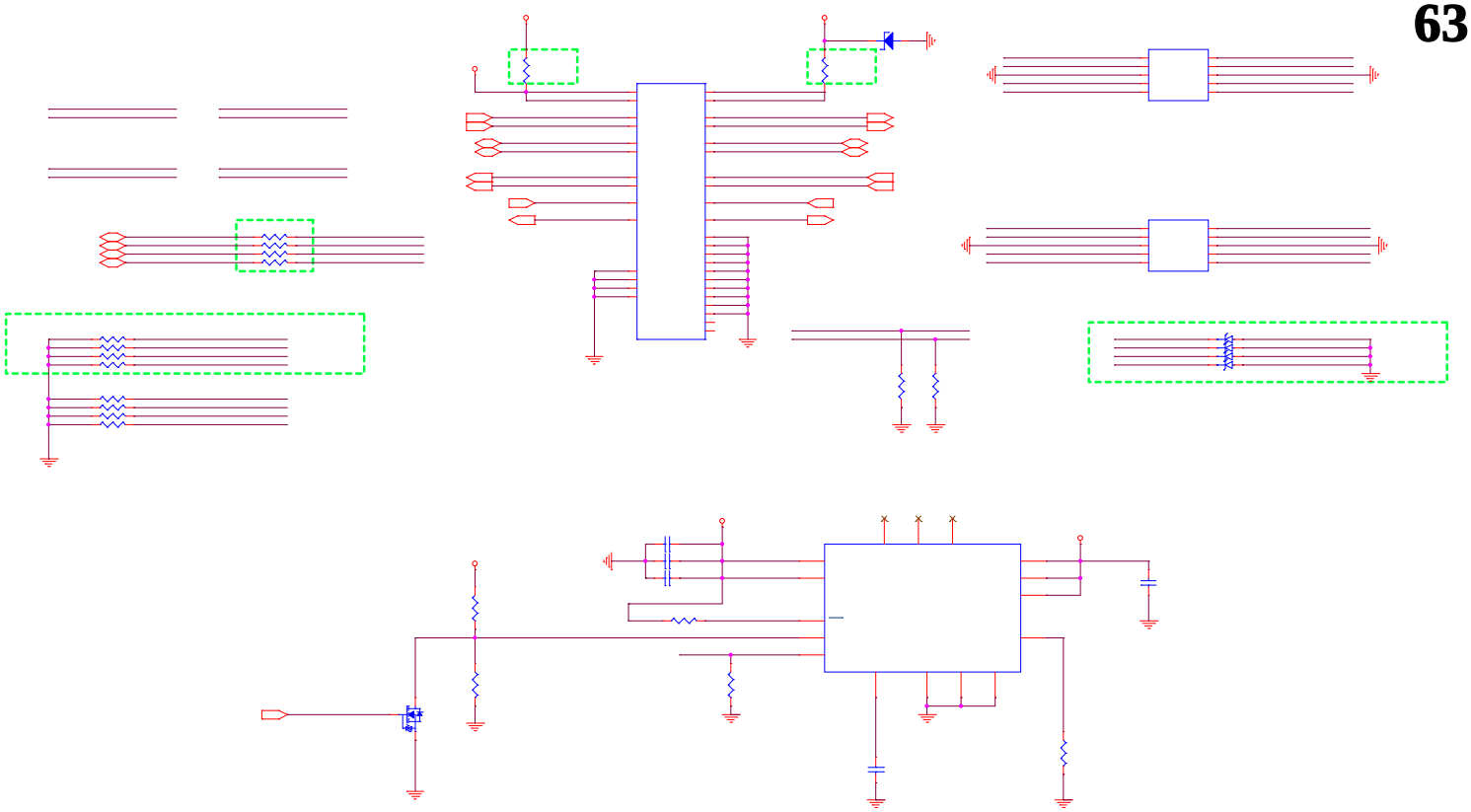
Use same values to start on IO2 and IO3

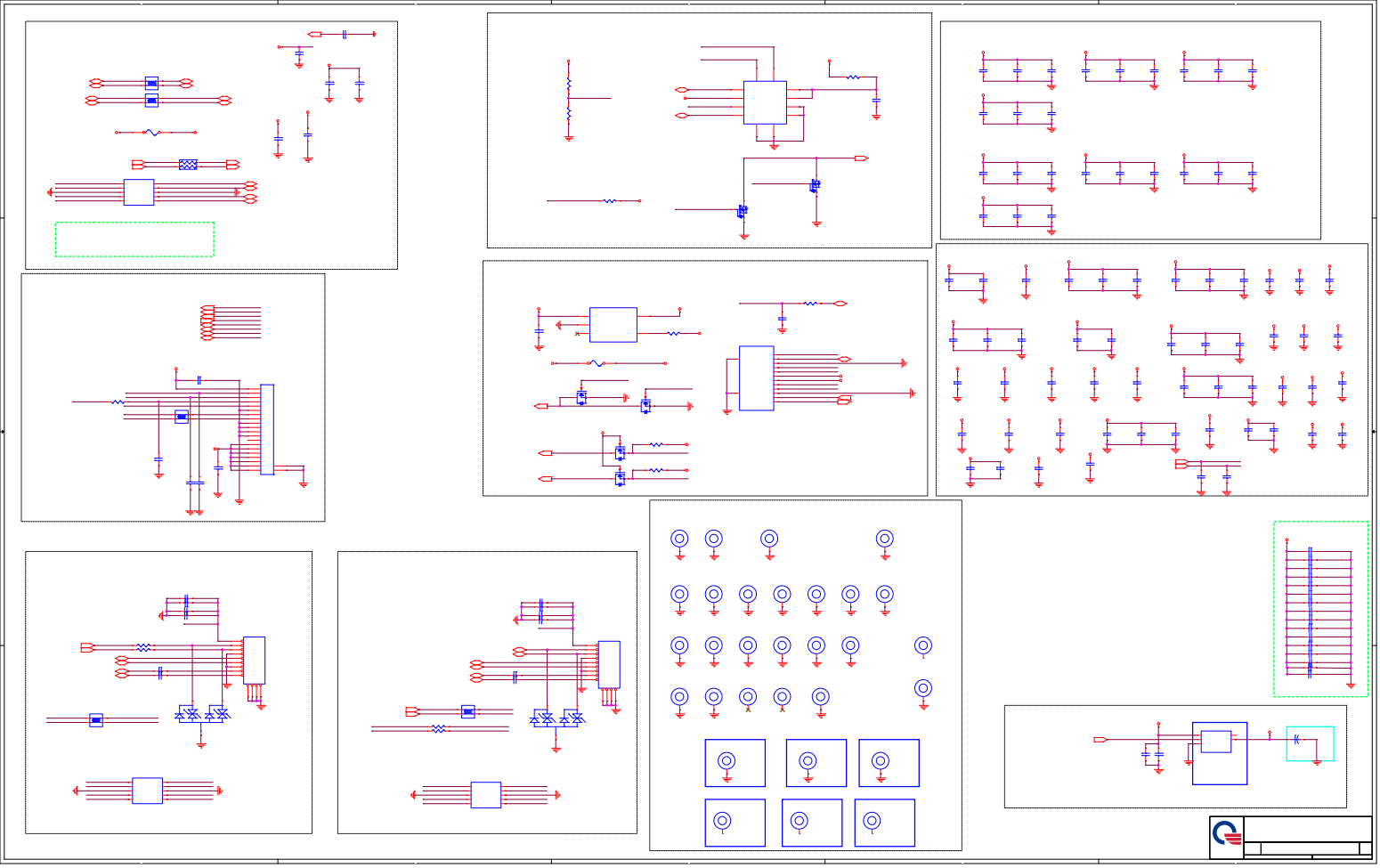
Note: The value of the resistors should be tuned according to the signal integrity simulations or actual PCB measurements.

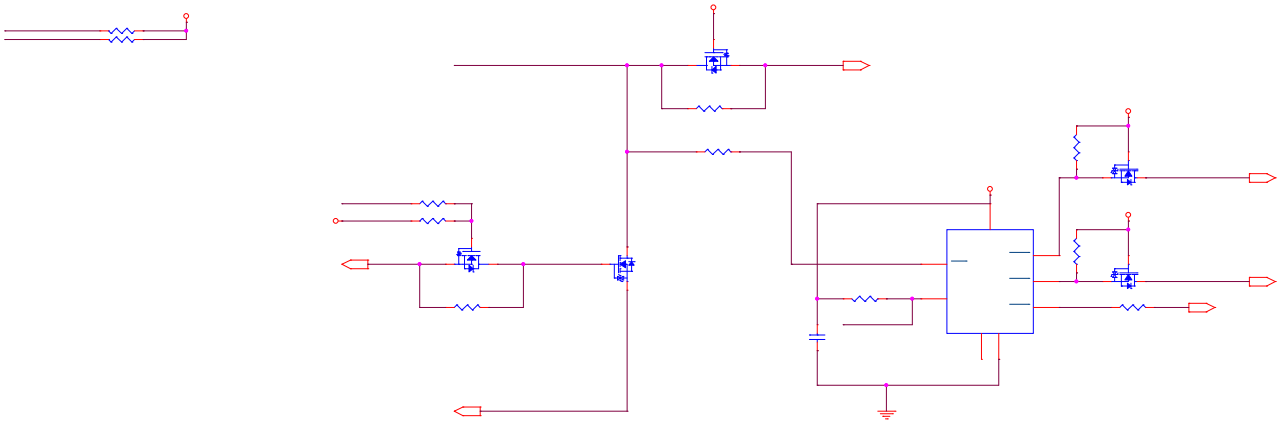


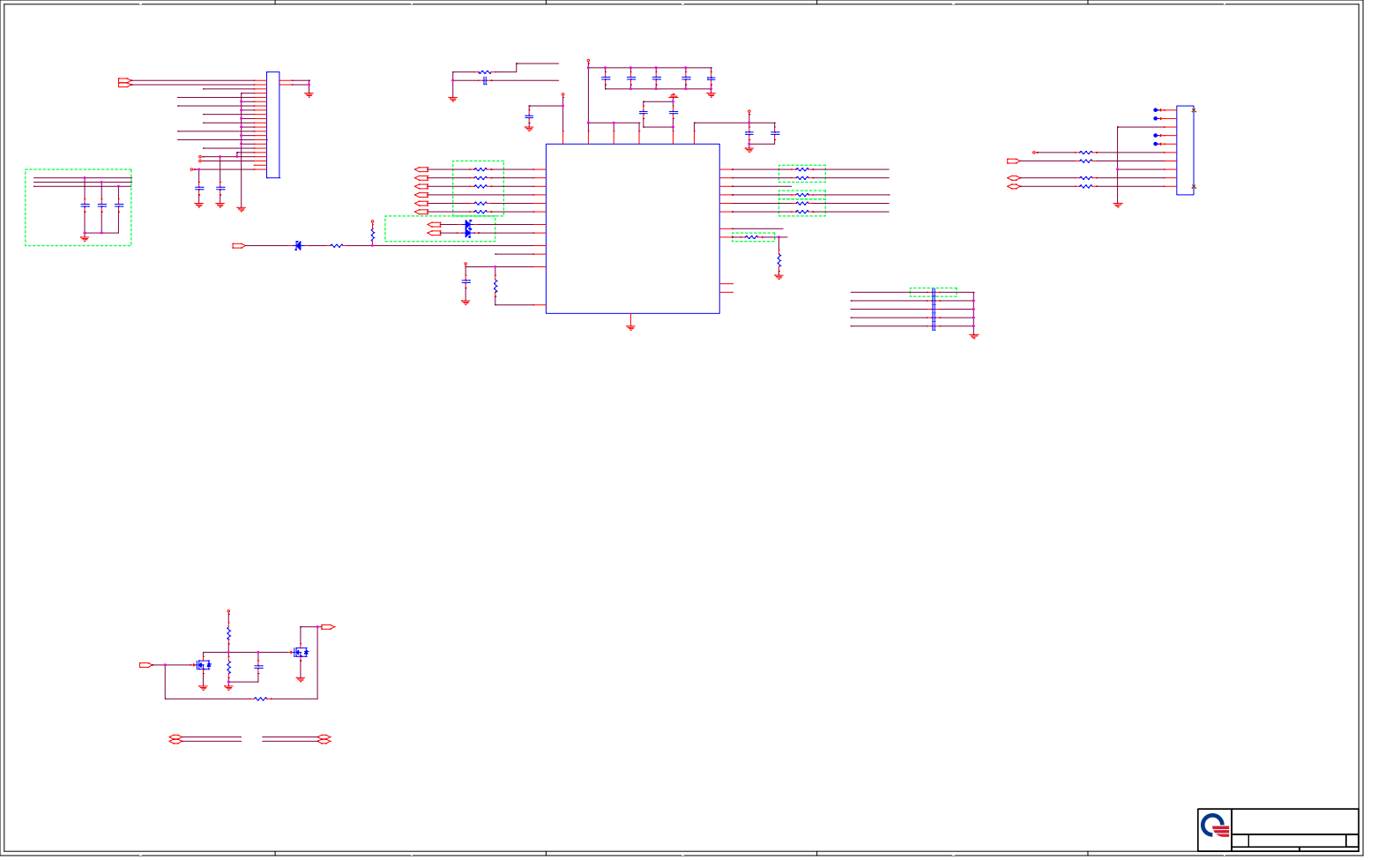


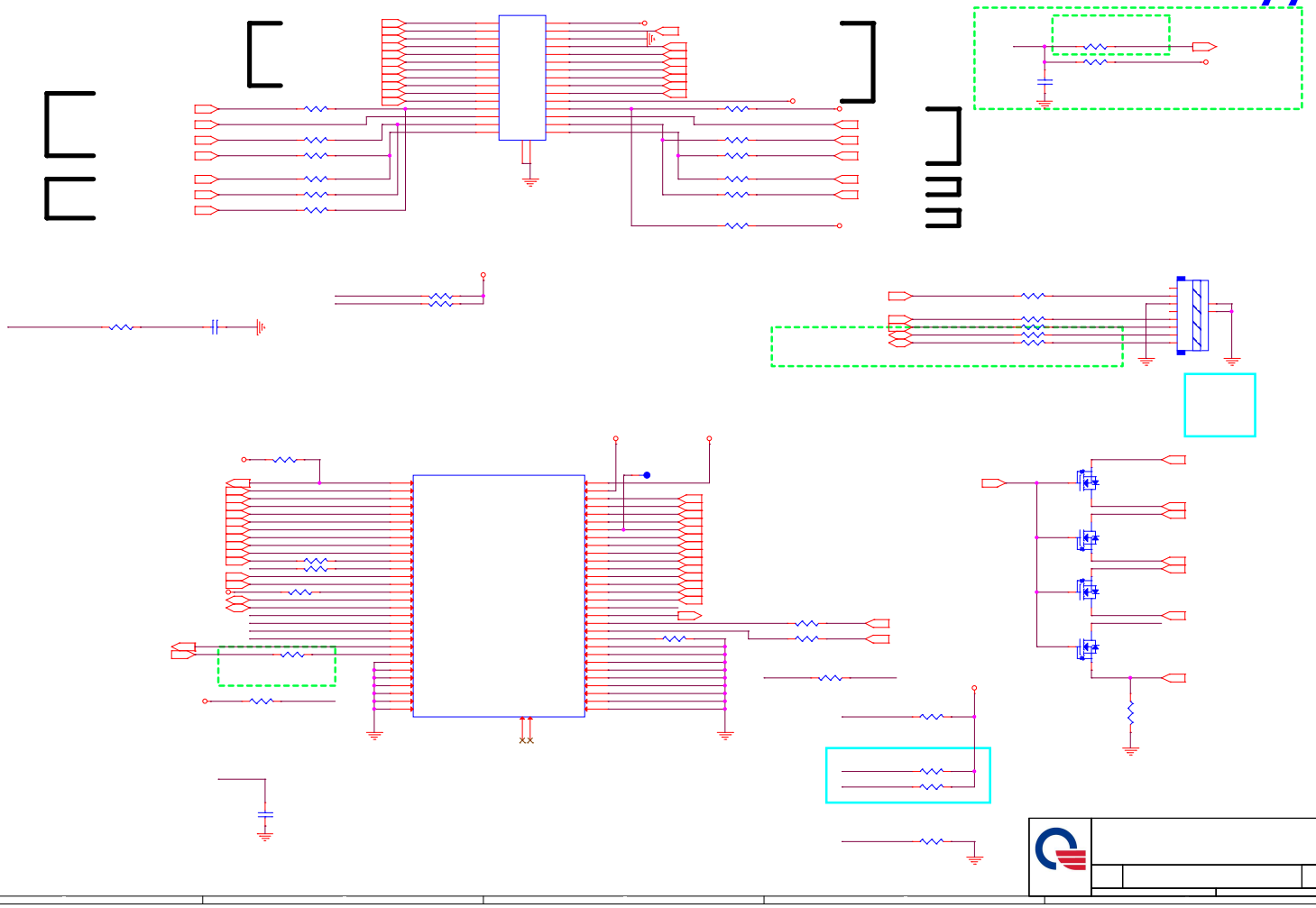
	Platform ID		CCG5 Dual Port	CCG5/CCG5C Single Port	L0 = 0V
	MOD_ID1	MOD_ID2	Description (Dual port)	Description (Single Port)	L1 = VDDD/8
Notebooks	L8	L7	Reserved	DRP+USB on 1-port with No MUX	L2 = 2* VDDD/8
	L7	L7	DRP+DP+ AR TBT on 2-ports	DRP+DP on 1-port with ANX MUX	L3 = 3* VDDD/8
	L6	L7	DRP+DP on 2-ports	DRP+DP+ TR TBT on 1-port	L4 = 4* VDDD/8
	L5	L7	DRP+DP on 2-ports with ANX MUX	DRP+DP+ AR TBT on 1-port (700, 800 Series)	L5 = 5* VDDD/8
	L4	L7	Malta	DRP+DP on 1-port with Parade MUX	L6 = 6* VDDD/8
	L3	L7	DRP+DP+ TR TBT on 2-ports	DRP+DP on 1-port (600/700 Series) - AMD SKU1	L7 = 7* VDDD/8
	L2	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU2	L8 = VDDD
	L1	L7	Reserved	DRP+DP on 1-port (600/700 Series) - AMD SKU3	
	L0	L7	Reserved	DRP+DP on 1-port with Parade MUX - 2019 S400 G6	

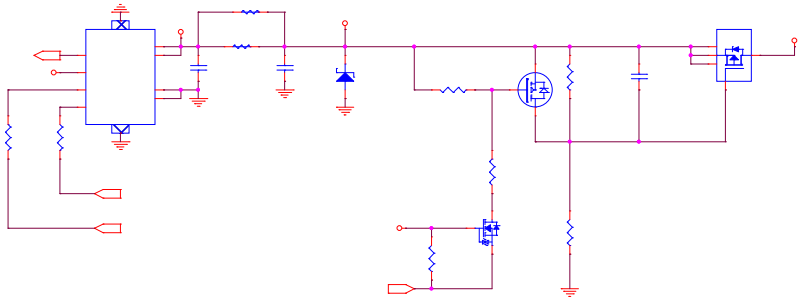


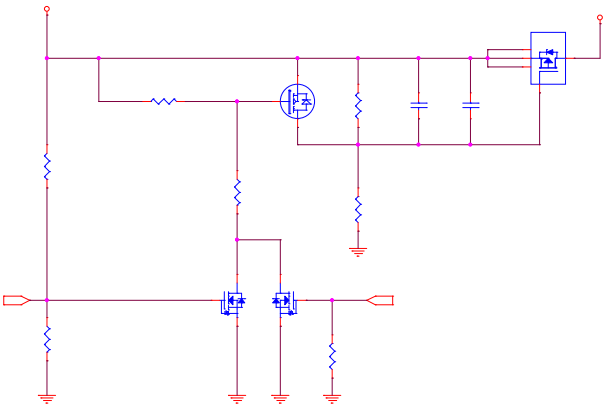


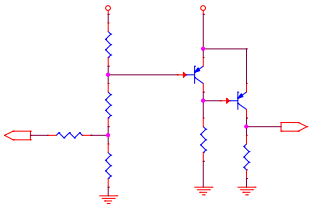


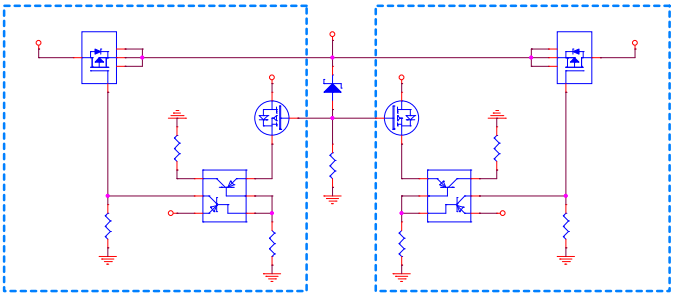


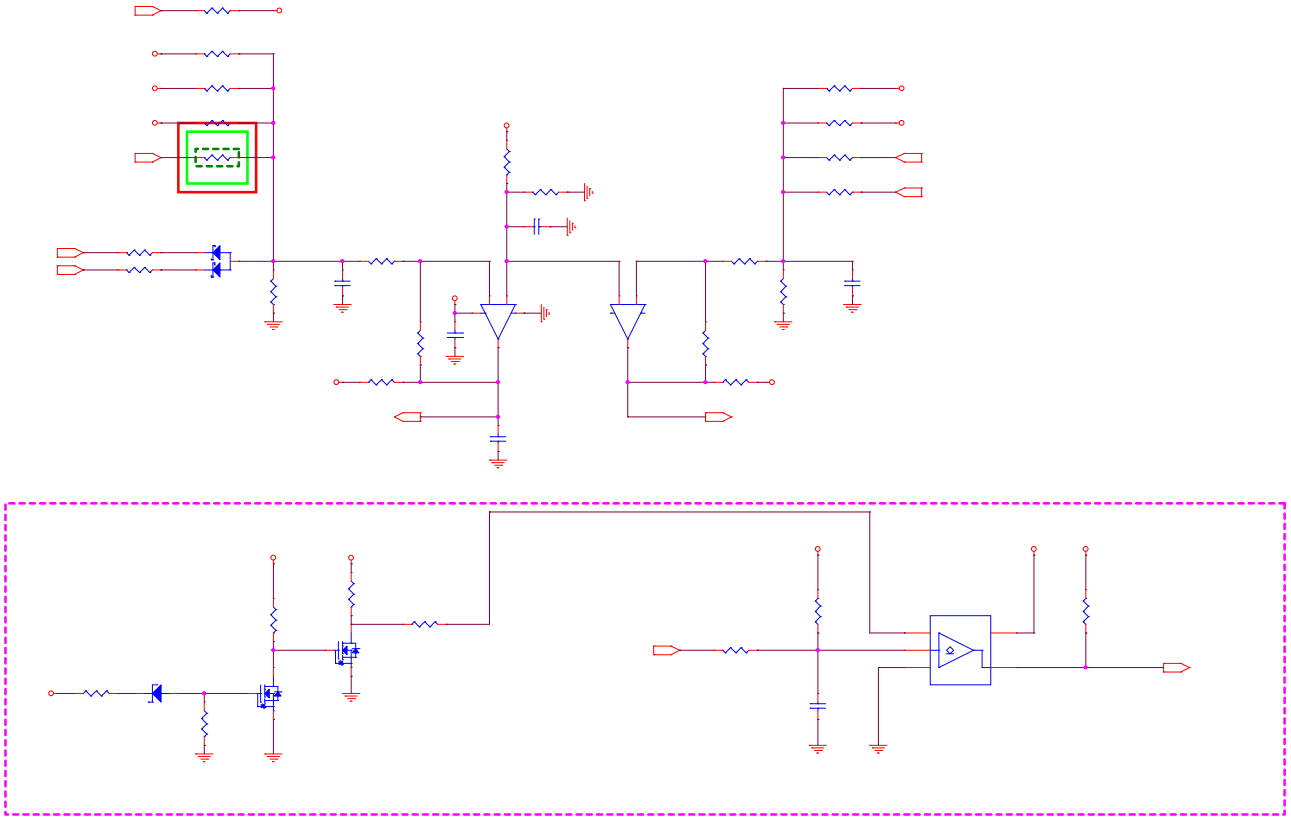


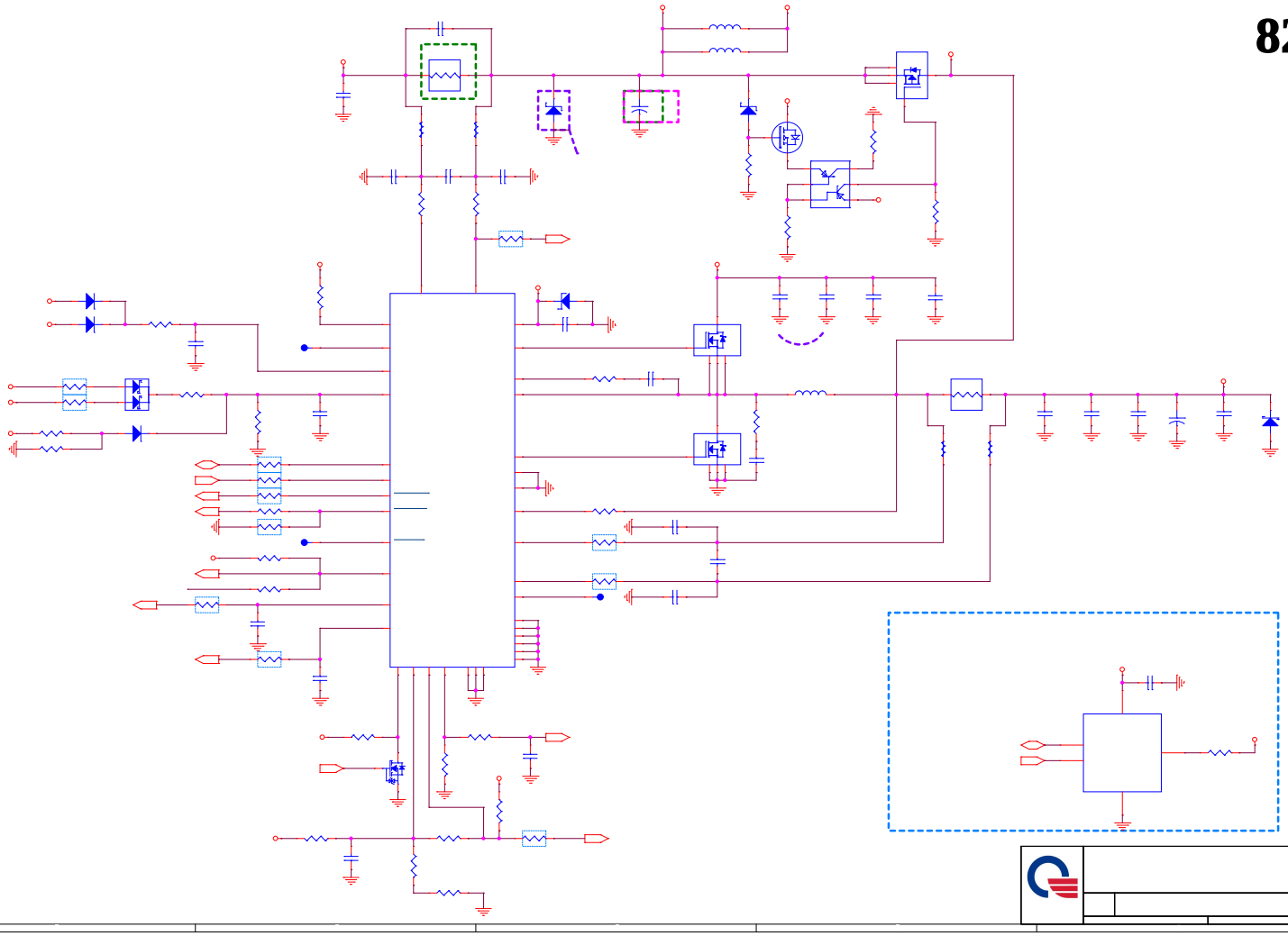


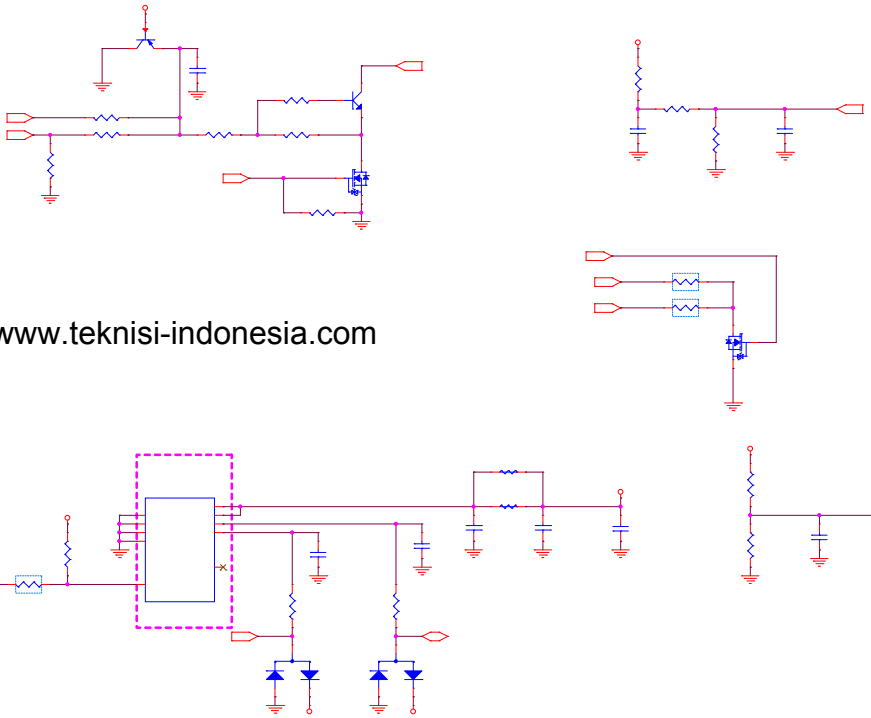


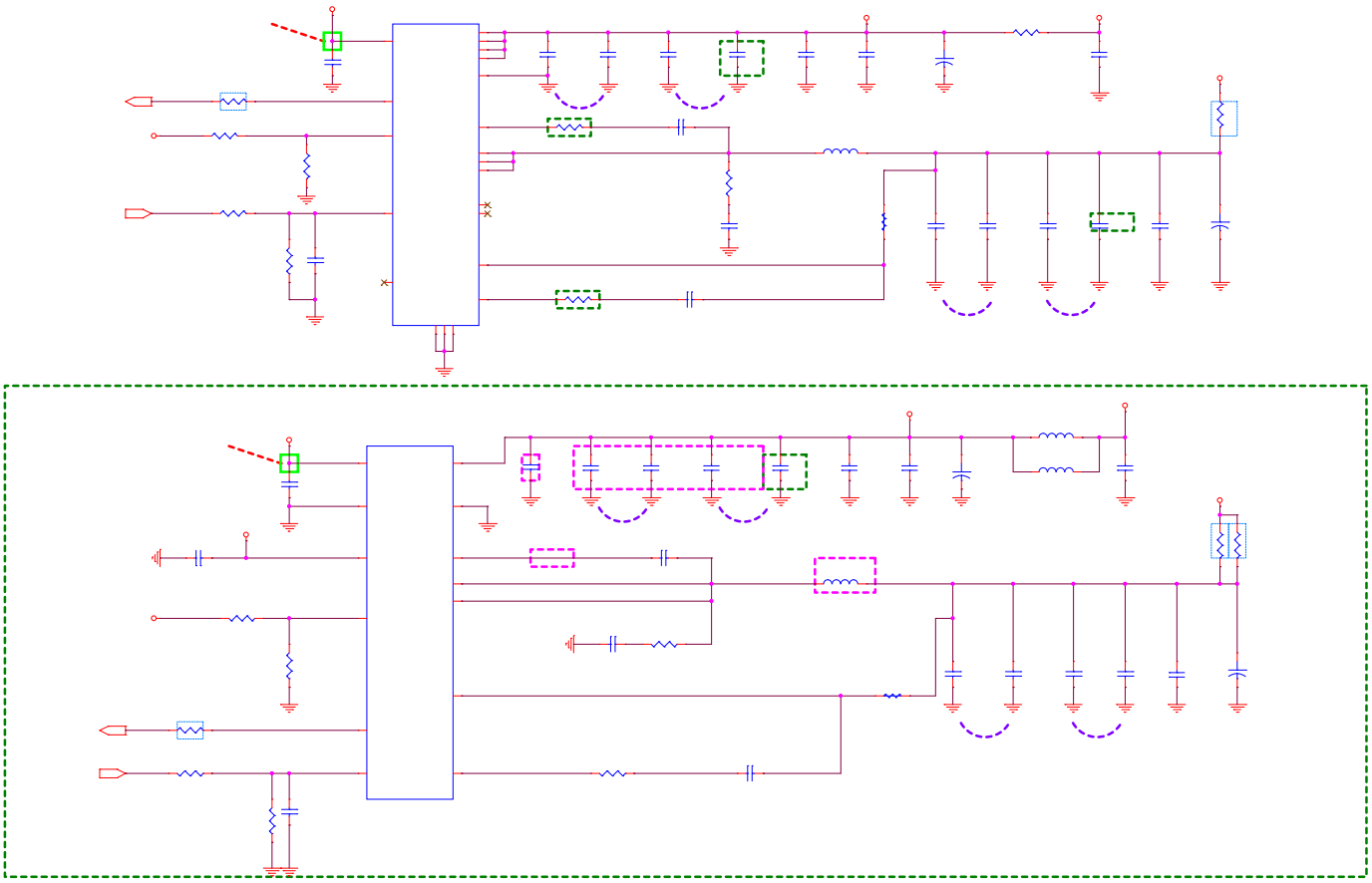


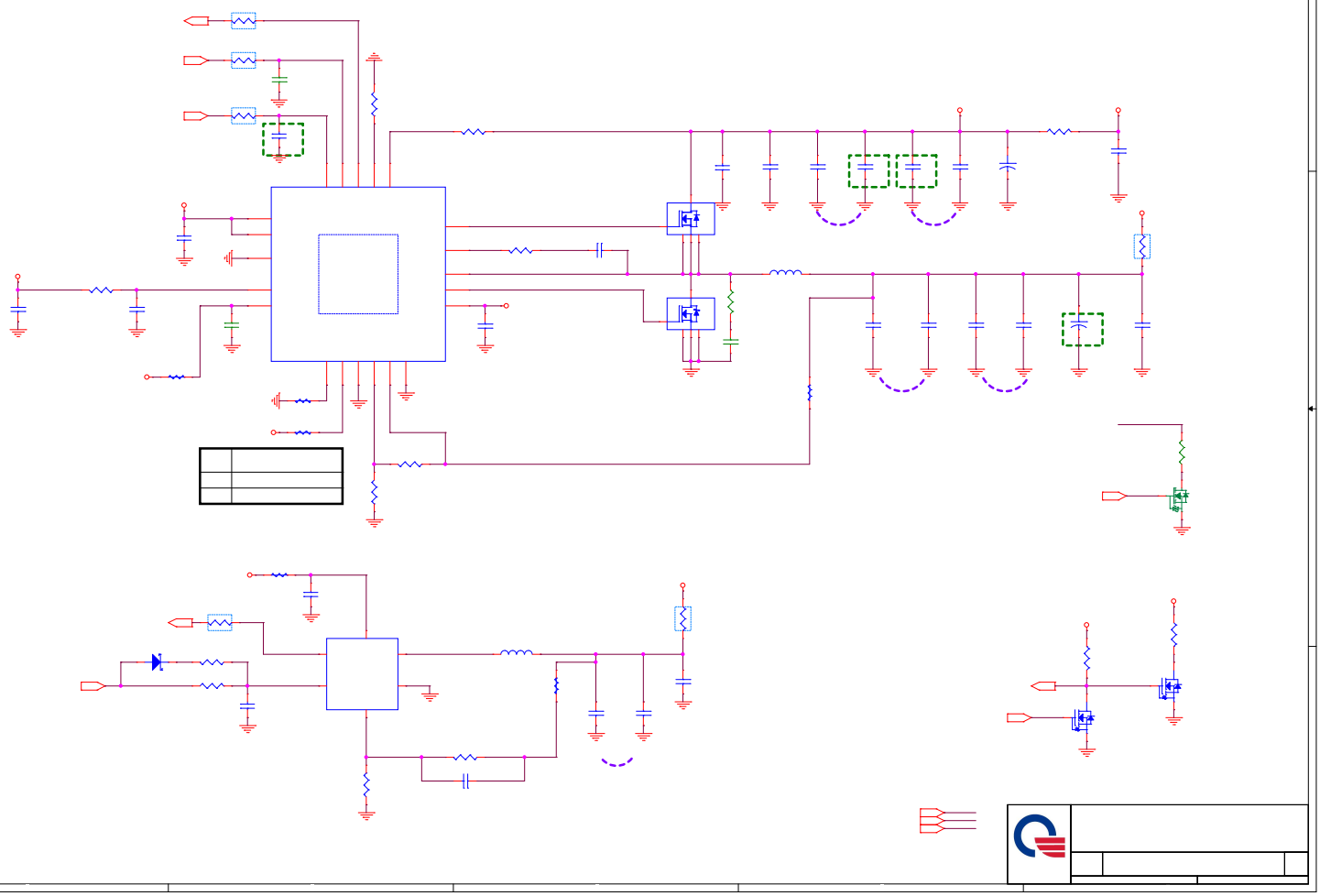


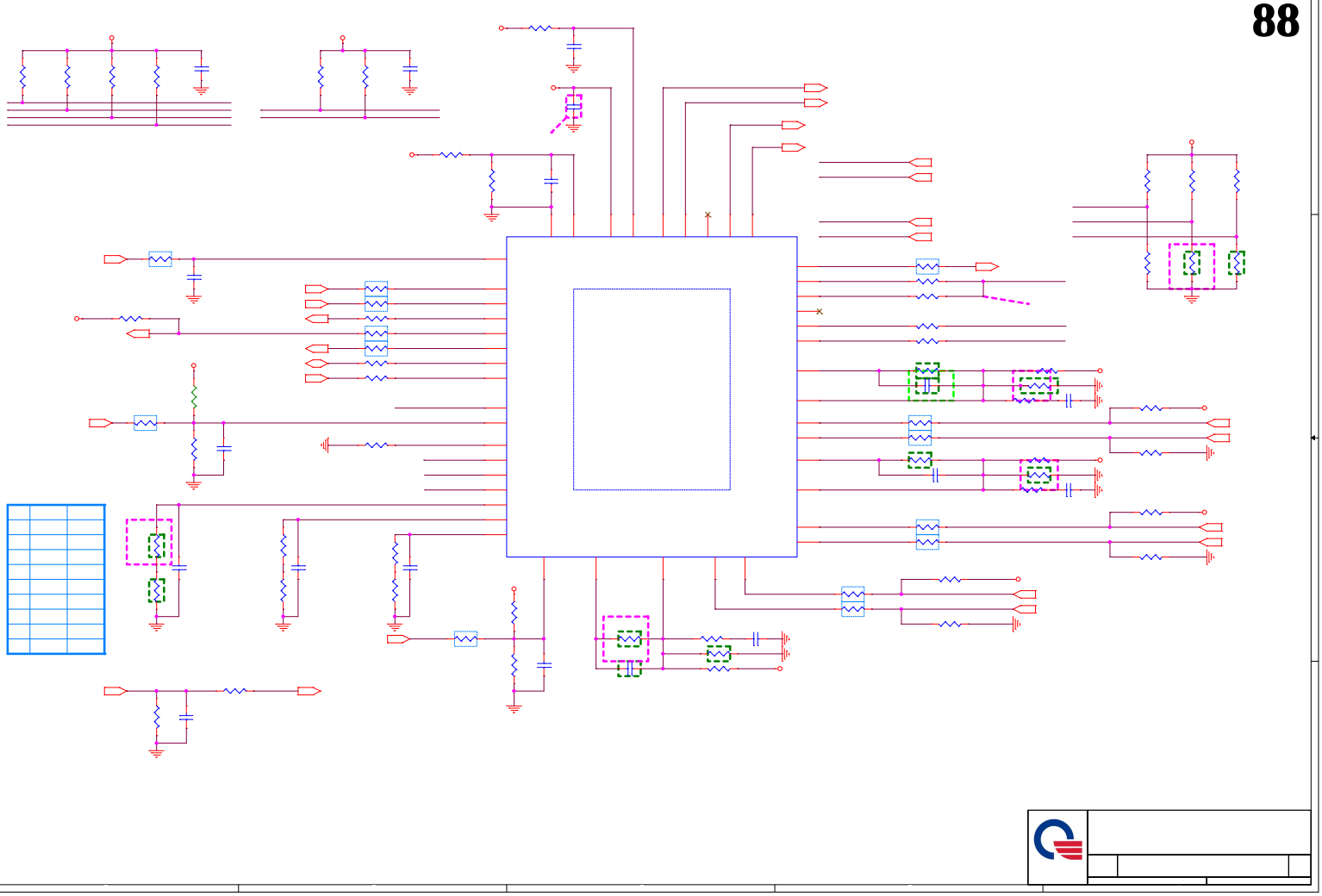


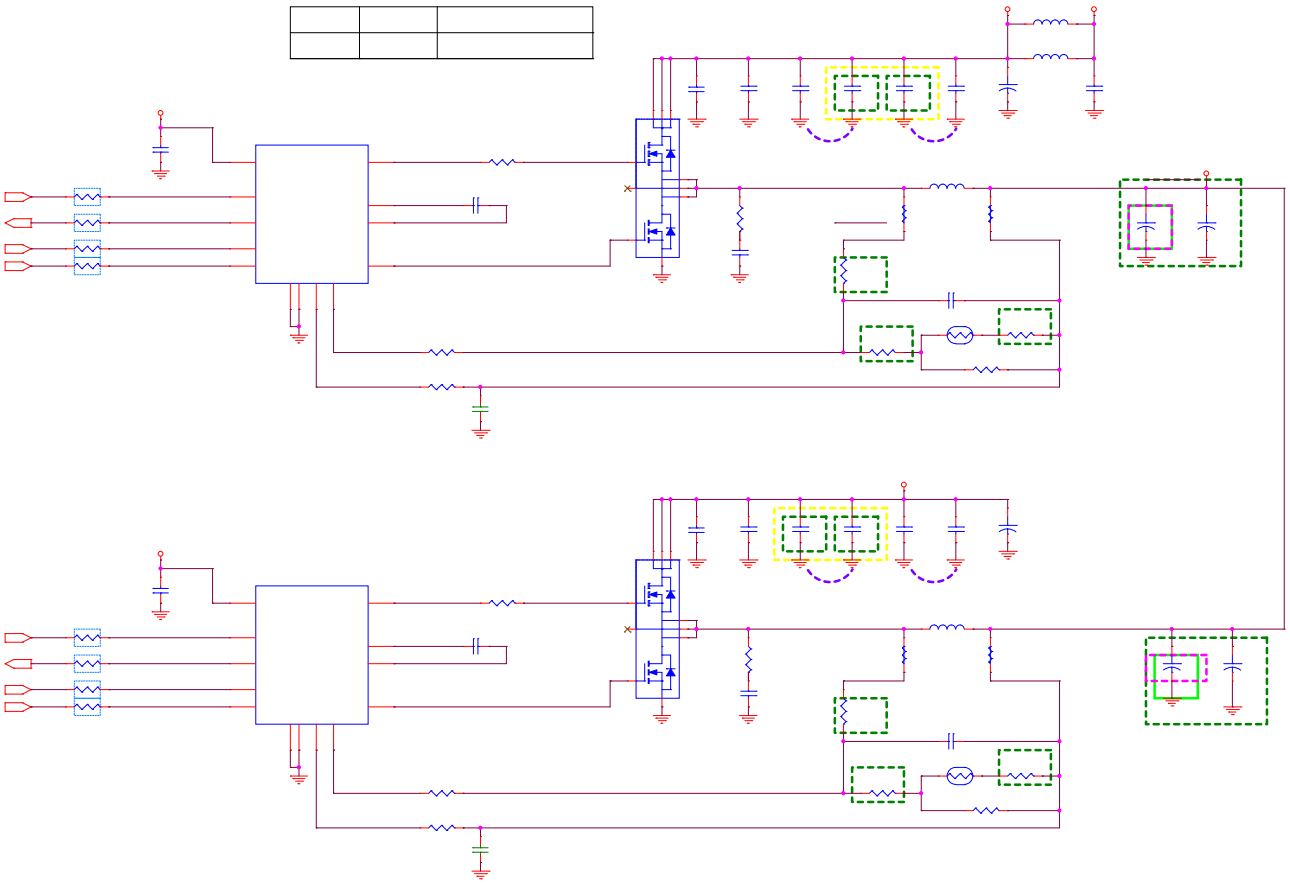


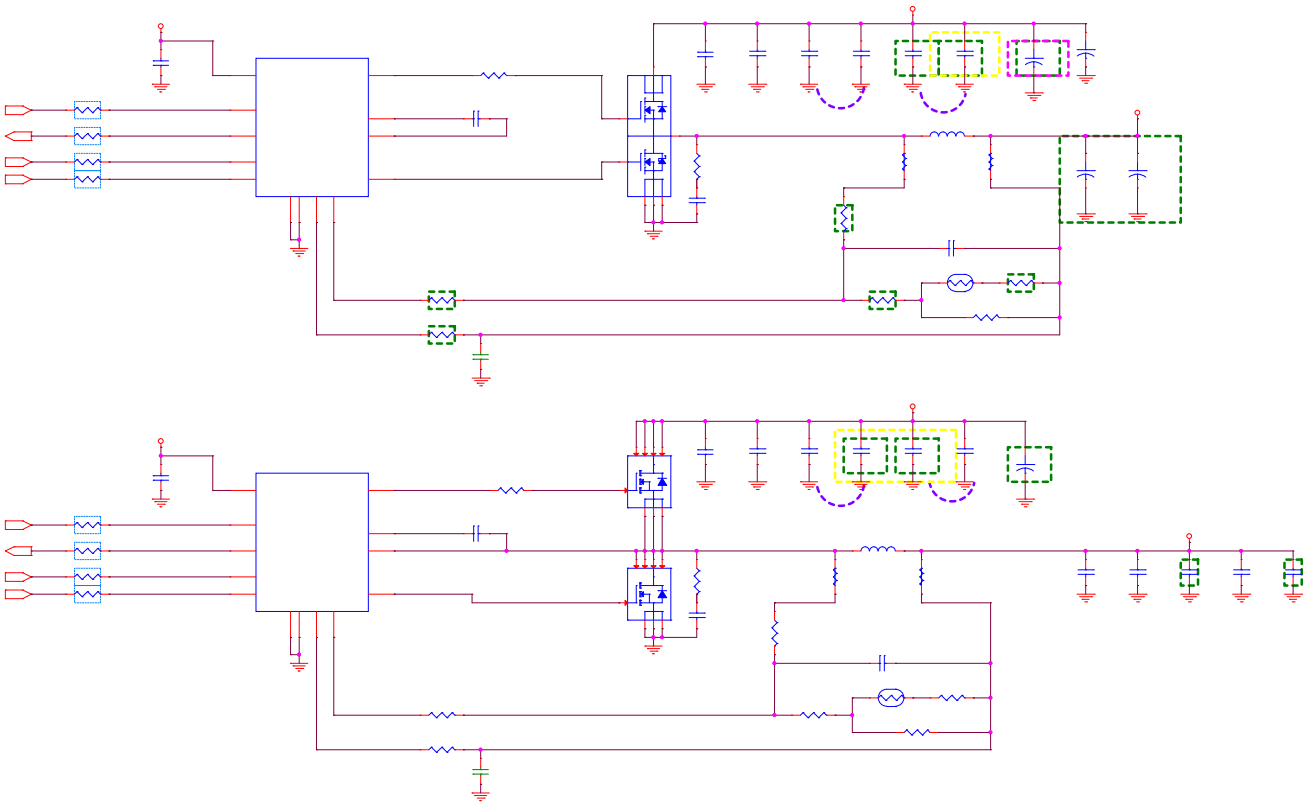


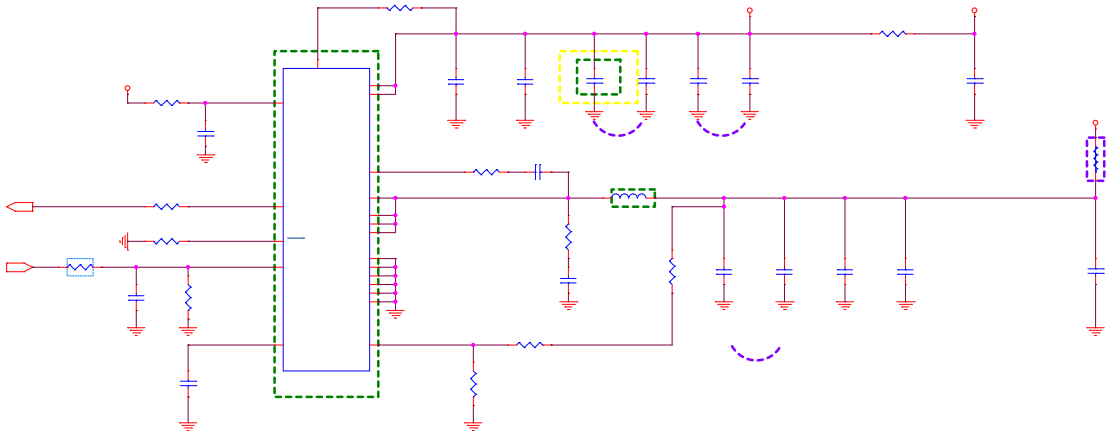


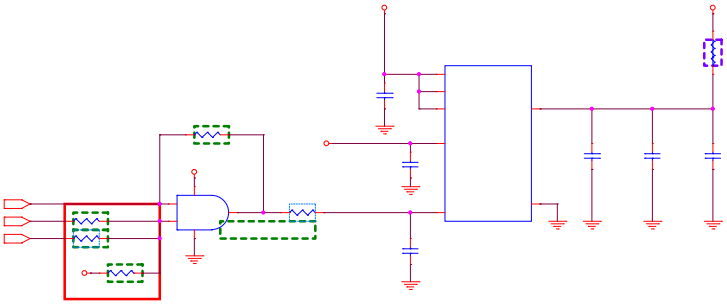


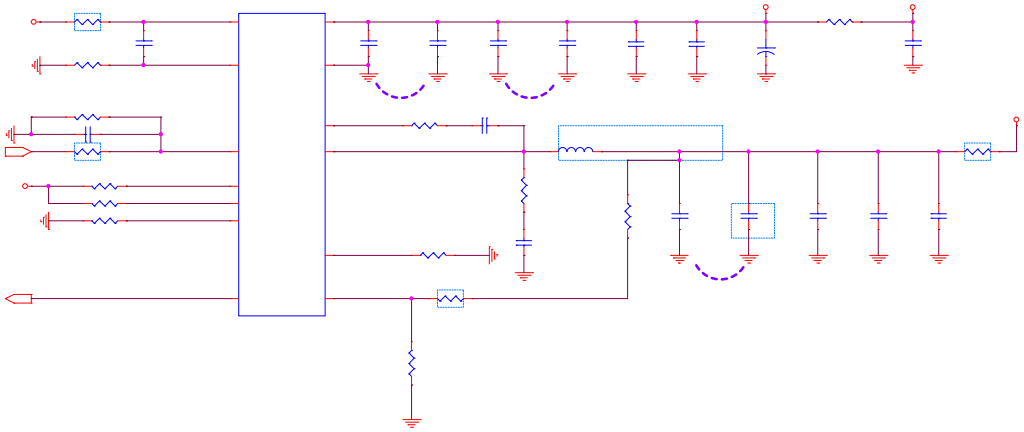






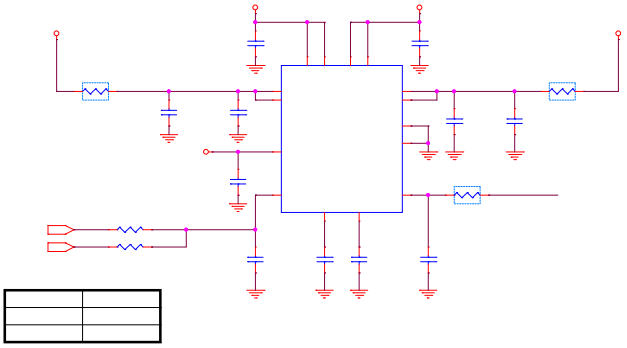


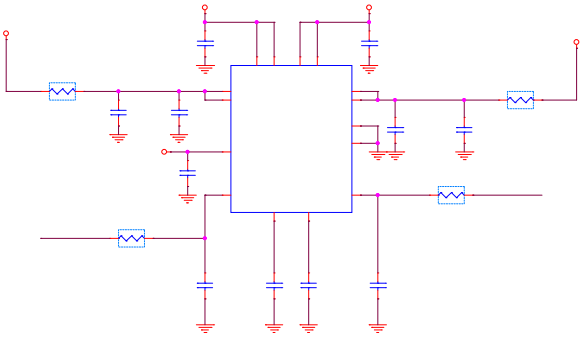


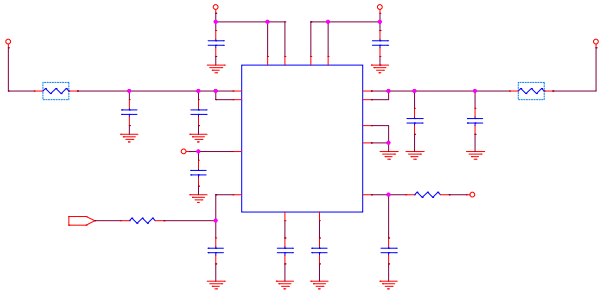


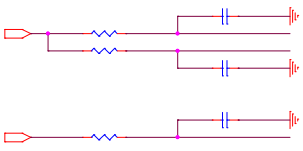
MODE	VR Rail	Resistor to GND (1% Accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230K
M3	EDRAM/V1.0A/EOPIO	100K
M4	Others	150K

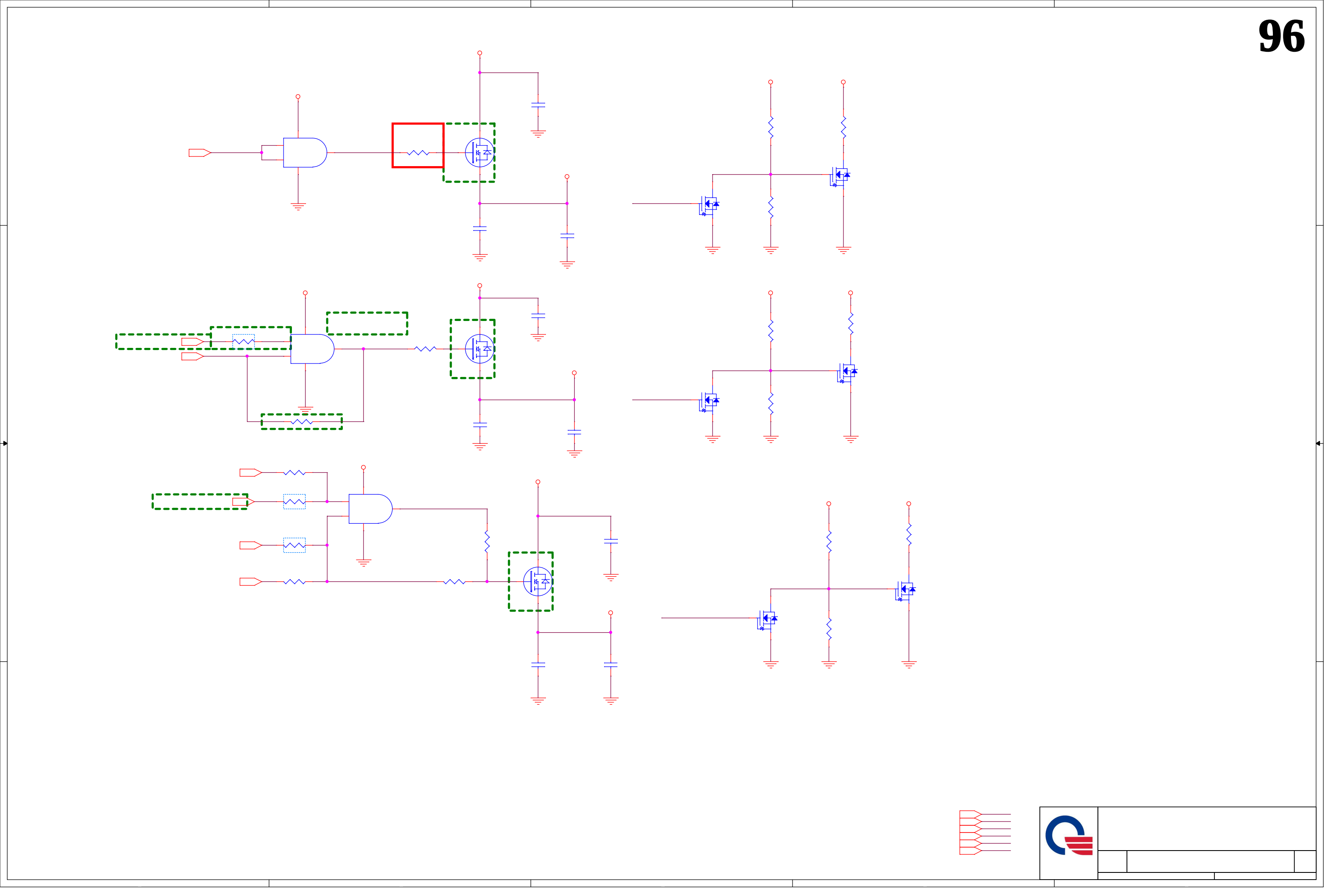
	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM _CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO/ V1.0A	0	X	X	0
	1	0	0	0.8 (MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

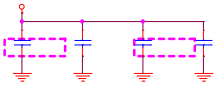


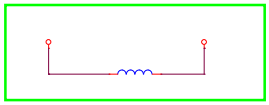












A0

A1

A2

A3

A4

A5

A6