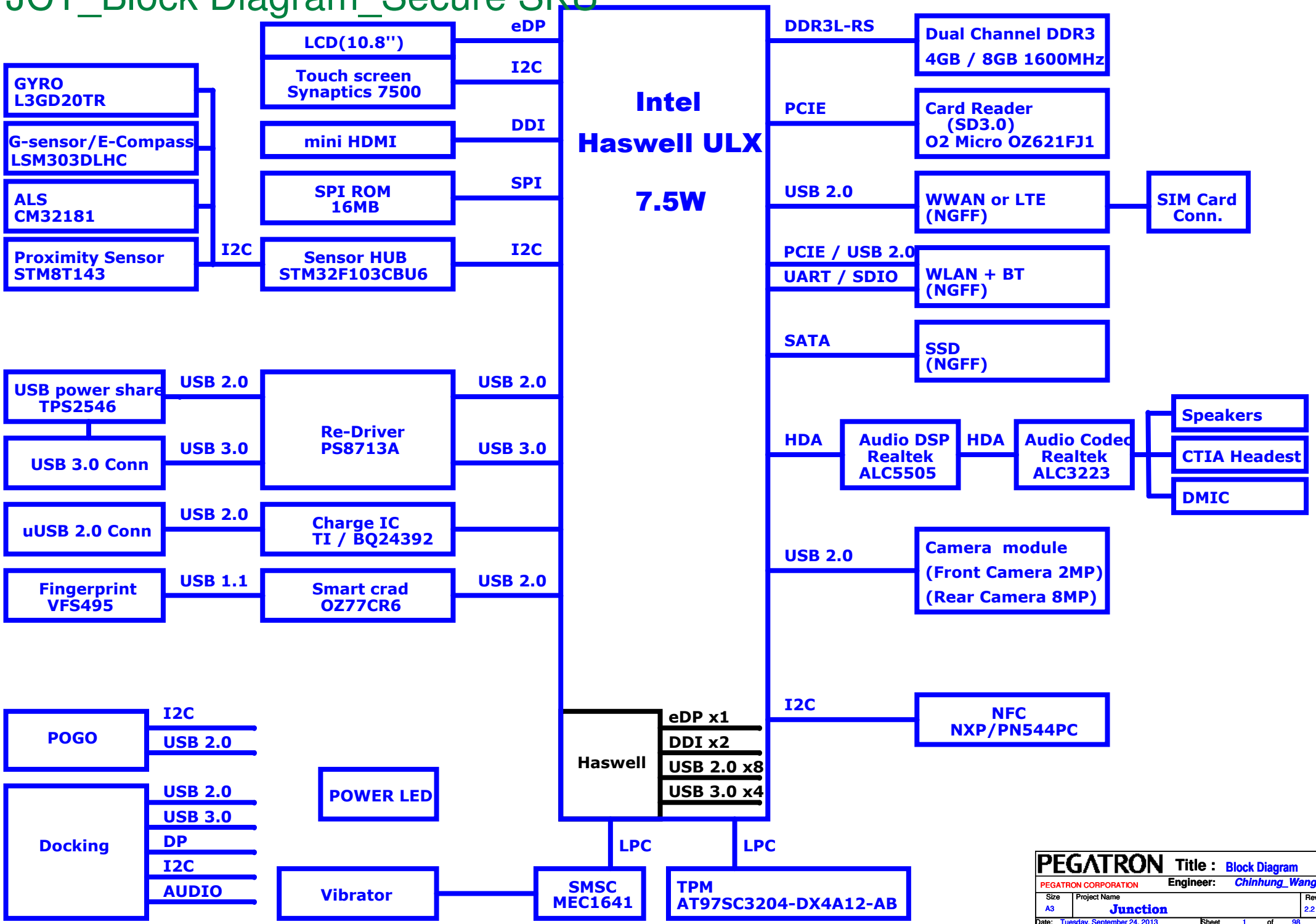
JCT_Block Diagram_Secure SKU



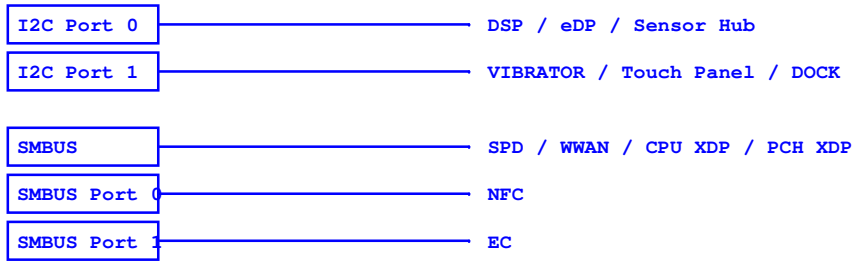
PEGATRON Title : Block Diagram

PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 1 of 98

I2C/SMBUS Block Diagram



I/O Port Mapping

PCIE 1	
PCIE 2	
PCIE 3	NGFF (WLAN)
PCIE 4	Card Reader
PCIE 5	
PCIE 6	

USB2.0 0	DOCK
USB2.0 1	USB3.0 (Debug Use)
USB2.0 2	CAMERA_2M
USB2.0 3	POGO
USB2.0 4	CAMERA_8M
USB2.0 5	WWAN
USB2.0 6	WLAN
USB2.0 7	USB HUB

USB3.0 0	DOCK
USB3.0 1	USB3.0

SATA 0	SSD
SATA 1	
SATA 2	

<Variant Name>

PEGATRON Title : REF PAGE

PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A2	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 2 of 98

<Variant Name>

PEGATRON

Title: CRU(1)_DMI,DP,PEG,FDI

PEGATRON CORPORATION

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 3 of 98

R1.0 PU/PD for JTAG signals

R1d

DDI Port 1: Mini HDMI

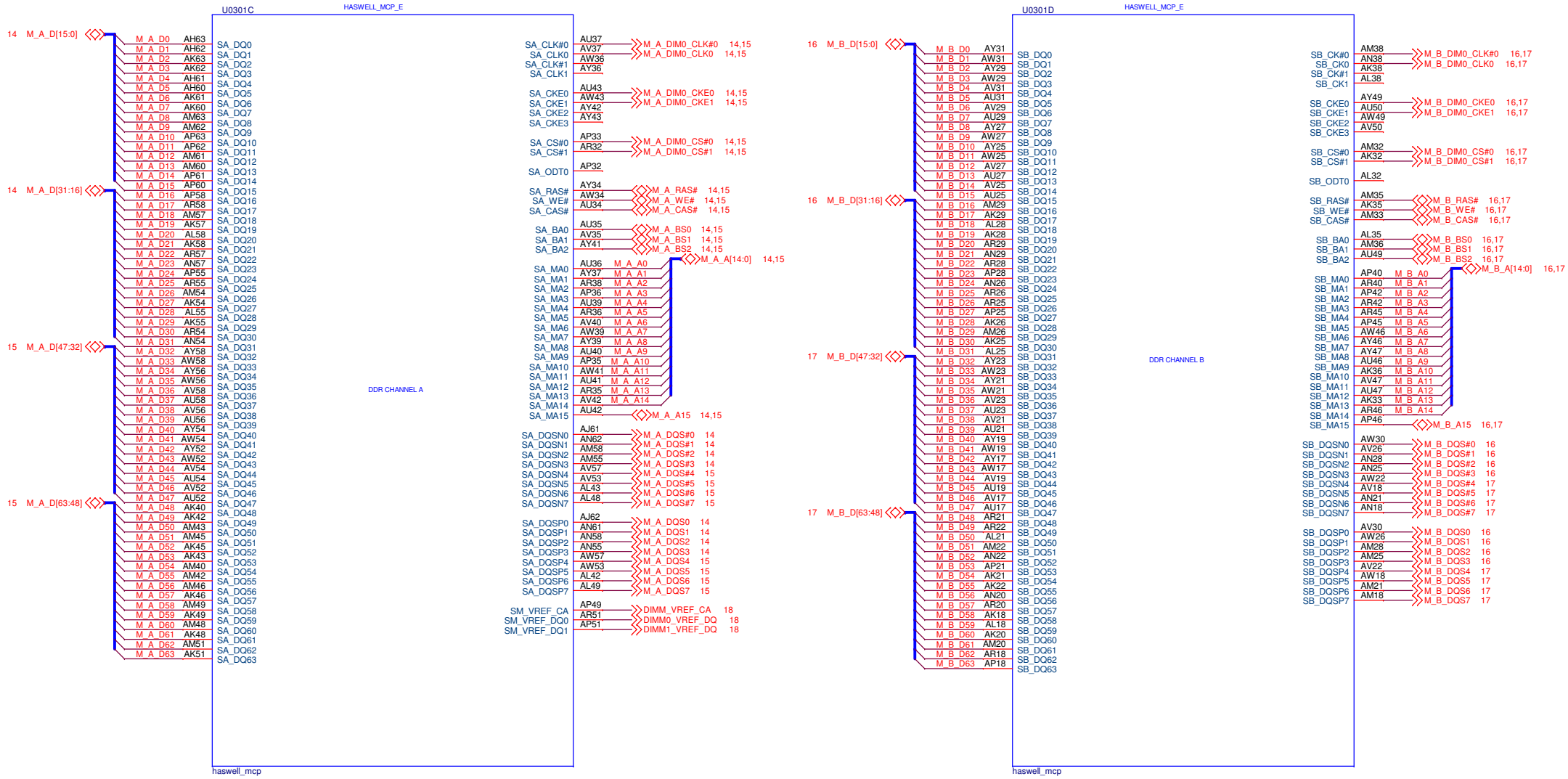
DDI Port 2: Dock

DDI signals Mapping, check 502636

eDP x 4

R2 R9

PEGATRON CORPORATION	Title : CPU(2)_MISC,JTAG,DDI,E		
	Engineer: Chinhung_Wang		
Size: A3	Project Name: Junction		Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 4 of 98		

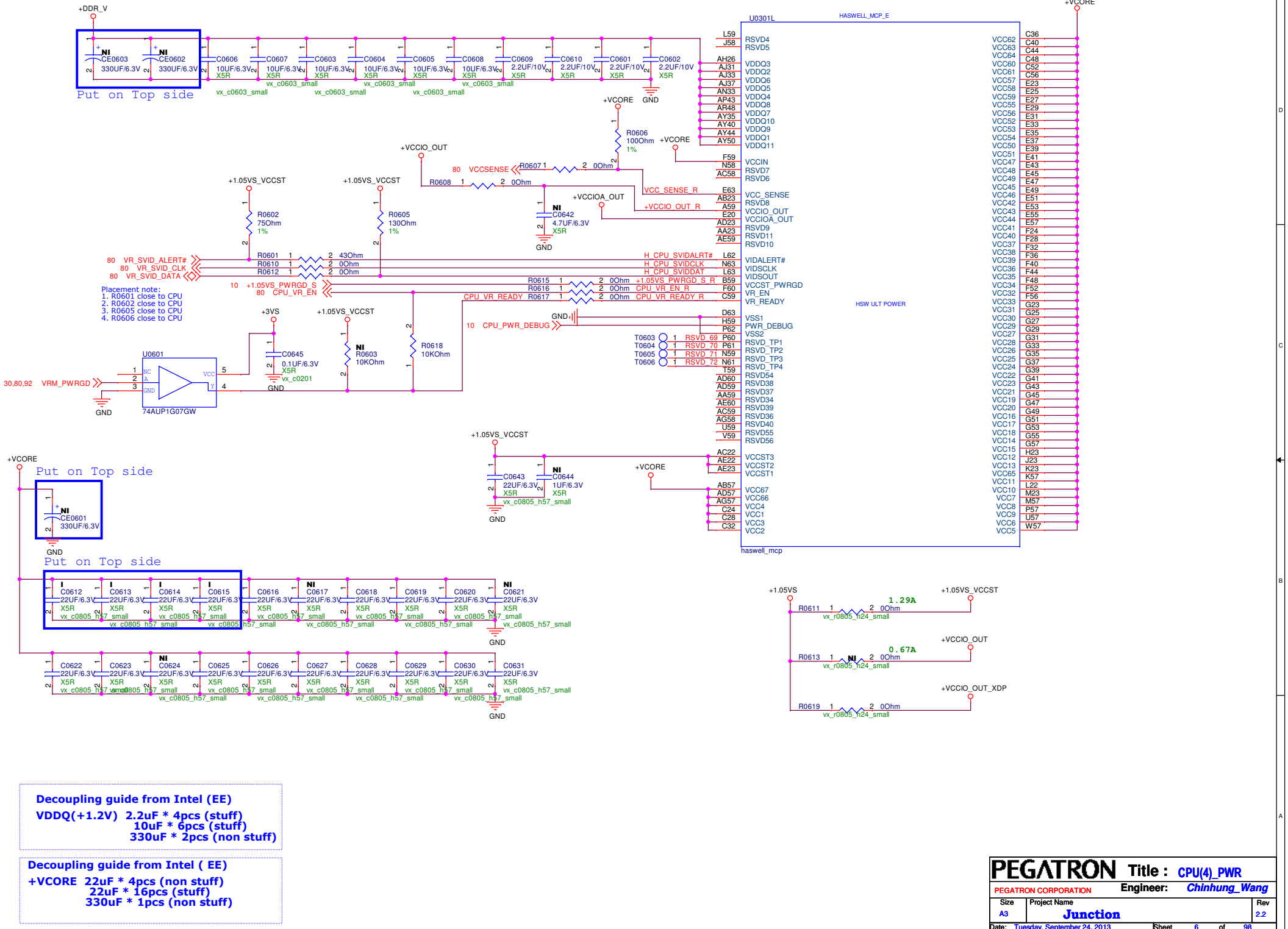


PEGATRON Title : CPU(3)_DDR3-rs

PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 5 of 98



Decoupling guide from Intel (EE)

VDDQ(+1.2V) 2.2uF * 4pcs (stuff)
10uF * 6pcs (stuff)
330uF * 2pcs (non stuff)

Decoupling guide from Intel (EE)

+VCORE 22uF * 4pcs (non stuff)
22uF * 16pcs (stuff)
330uF * 1pcs (non stuff)

PEGATRON CORPORATION

Title : CPU(4)_PWR

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 6 of 98

PEGATRON

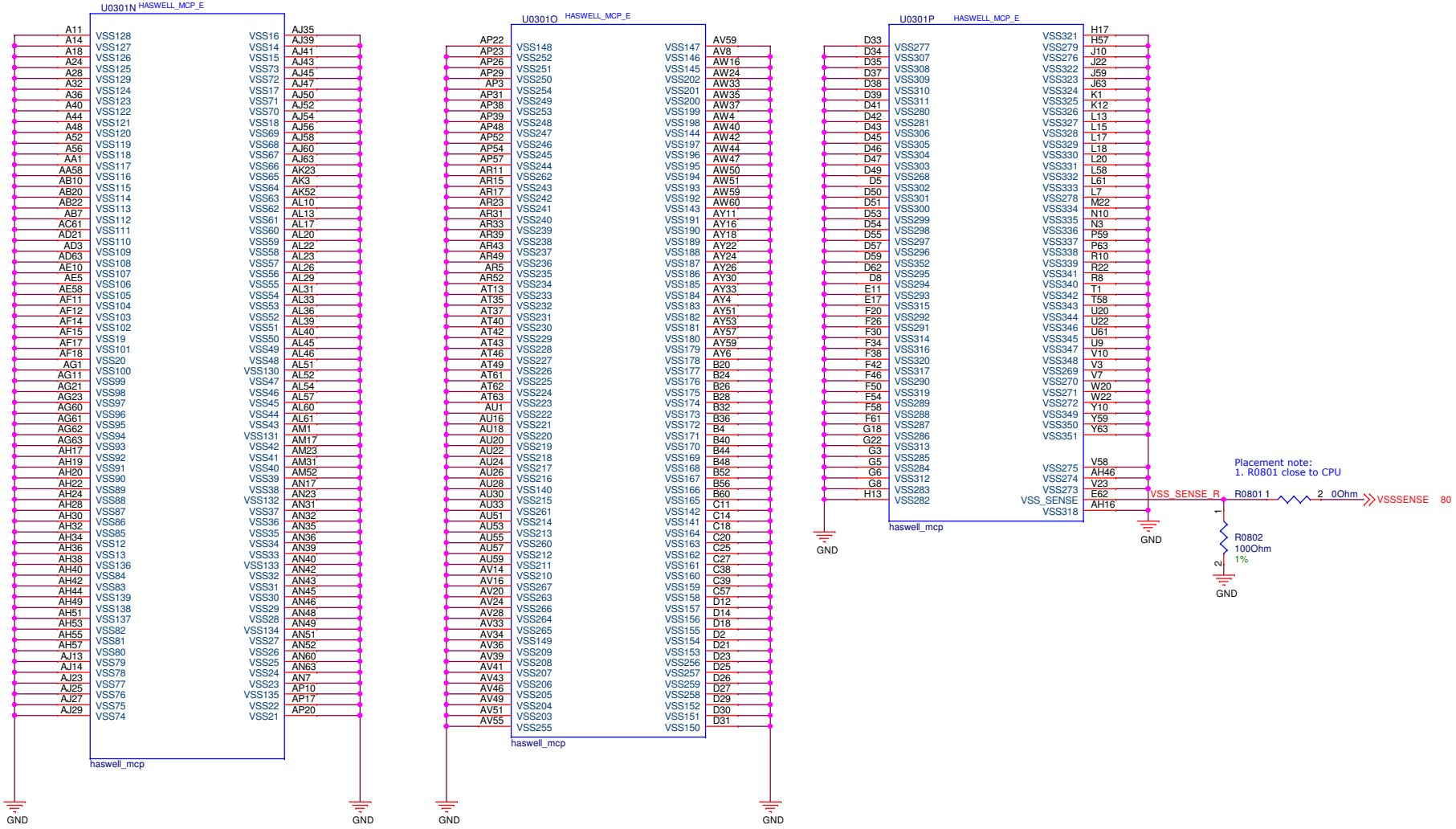
Title : CPU(5)_****

PEGATRON CORPORATION

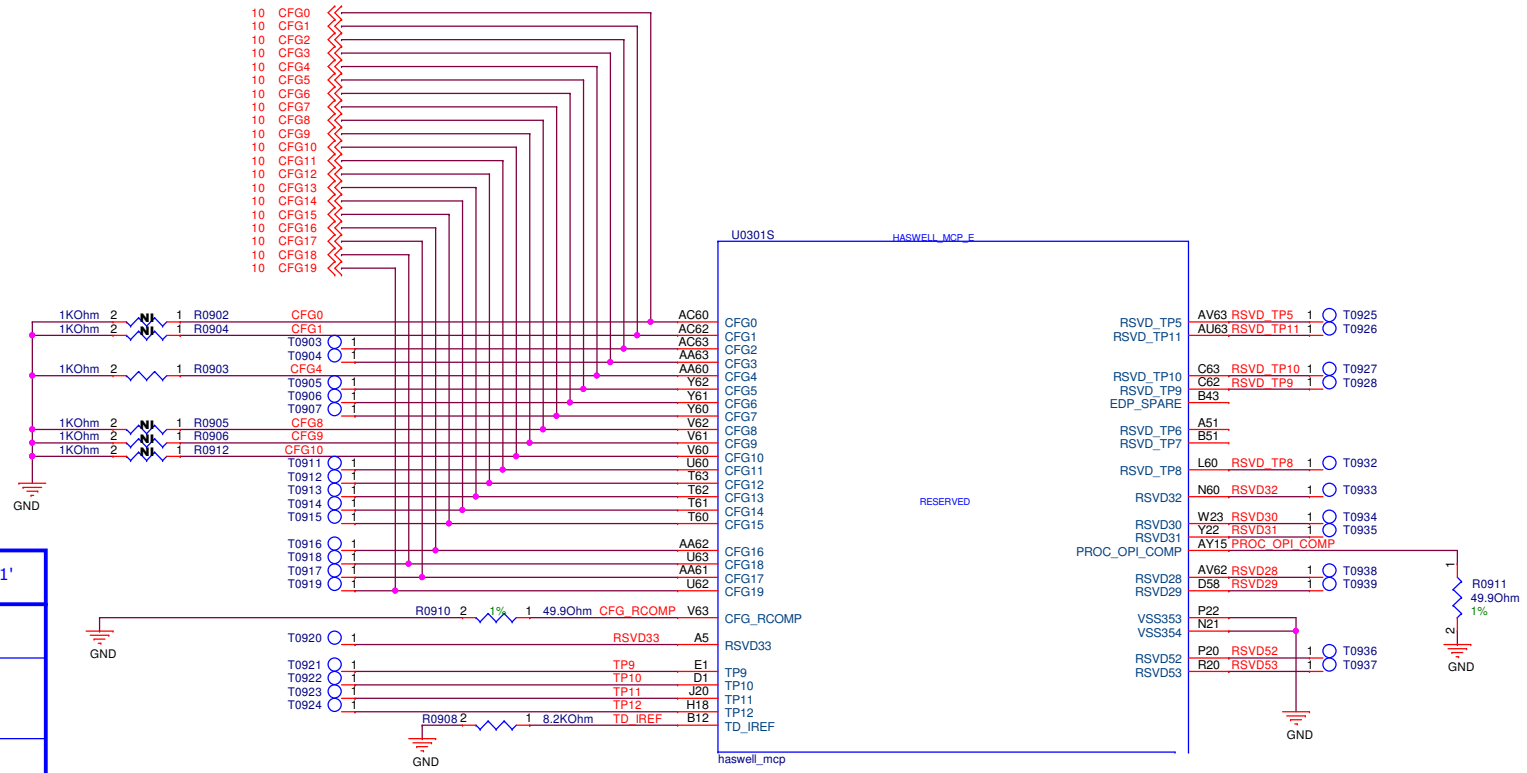
Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 7 of 98



PEGATRON	Title : CPU(6)_GND		
PEGATRON CORPORATION	Engineer: Chinhung_Wang		
Size: A3	Project Name: Junction		Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 8 of 98		



CFG strapping information: The CFG signals have a default value of '1'
CFG[20:0] - INT. PU

CFG[3:0]: Reserved configuration lane.
A test point may be placed on the board for these lanes.

CFG[4]: eDP enable

-1 = Disabled
-0 = Enabled

CFG[19:5]: Reserved configuration lanes.
A test point may be placed on the board for these lands.

Follow Harris Beach

CFG strapping information: The CFG signals have a default value of '1'

CFG[0]: EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED

-1 = (DEFAULT) NORMAL OPERATION; NO STALL
-0 = STALL

CFG[1]: PCH/ PCH LESS MODE SELECTION

-1 = (DEFAULT) NORMAL OPERATION
-0 = PCH-LESS MODE

CFG[8]: ALLOW THE USE OF NOA ON LOCKED UNITS

-1 = DISABLED(DEFAULT);
IN THIS CASE, NOA WILL BEDISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS
-0 = ENABLED;
NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT

CFG[9]: NO SVID PROTOCOL CAPABLE VR CONNECTED

-1 = VRS SUPPORTING SVID PROTOCOL ARE PRESENT
-0 = NO VR SUPPORTING SVID IS PRESENT.
THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY

CFG[10]: SAFE MODE BOOT

-1 = POWER FEATURES ACTIVATED DURING RESET
-0 = POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

PEGATRON CORPORATION

Title : CPU(7)_RESERVED

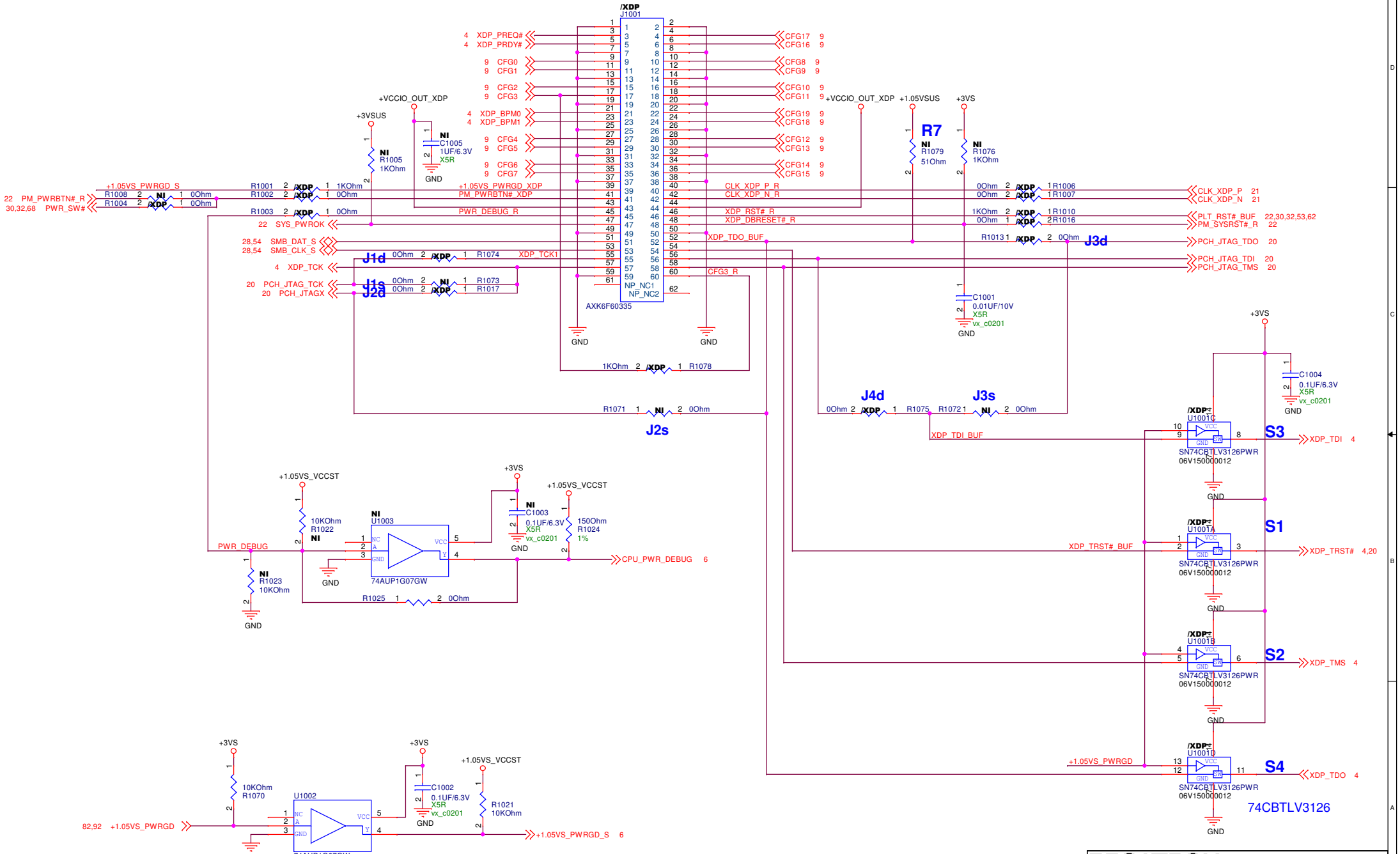
Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

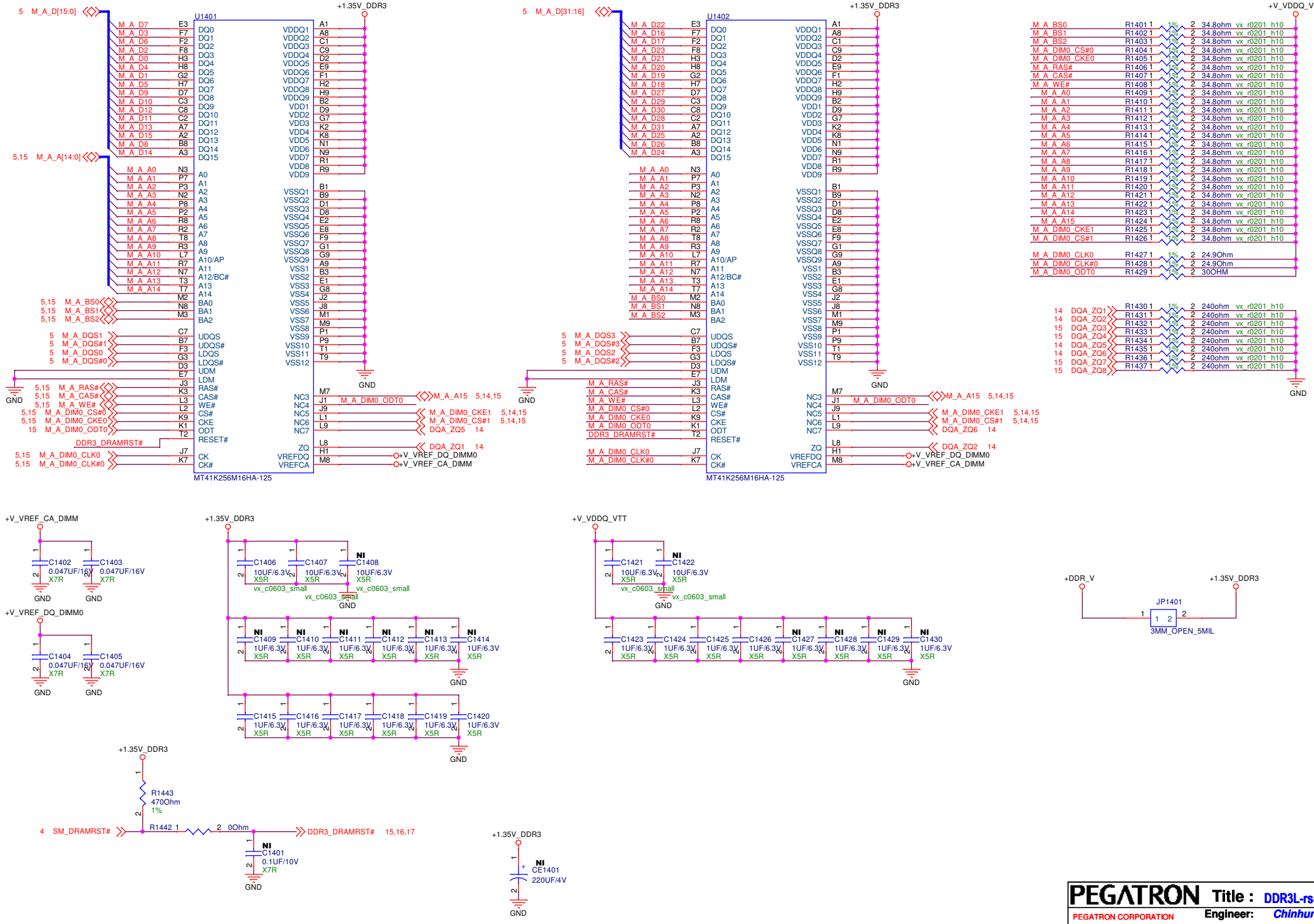
Date: Tuesday, September 24, 2013 Sheet 9 of 98

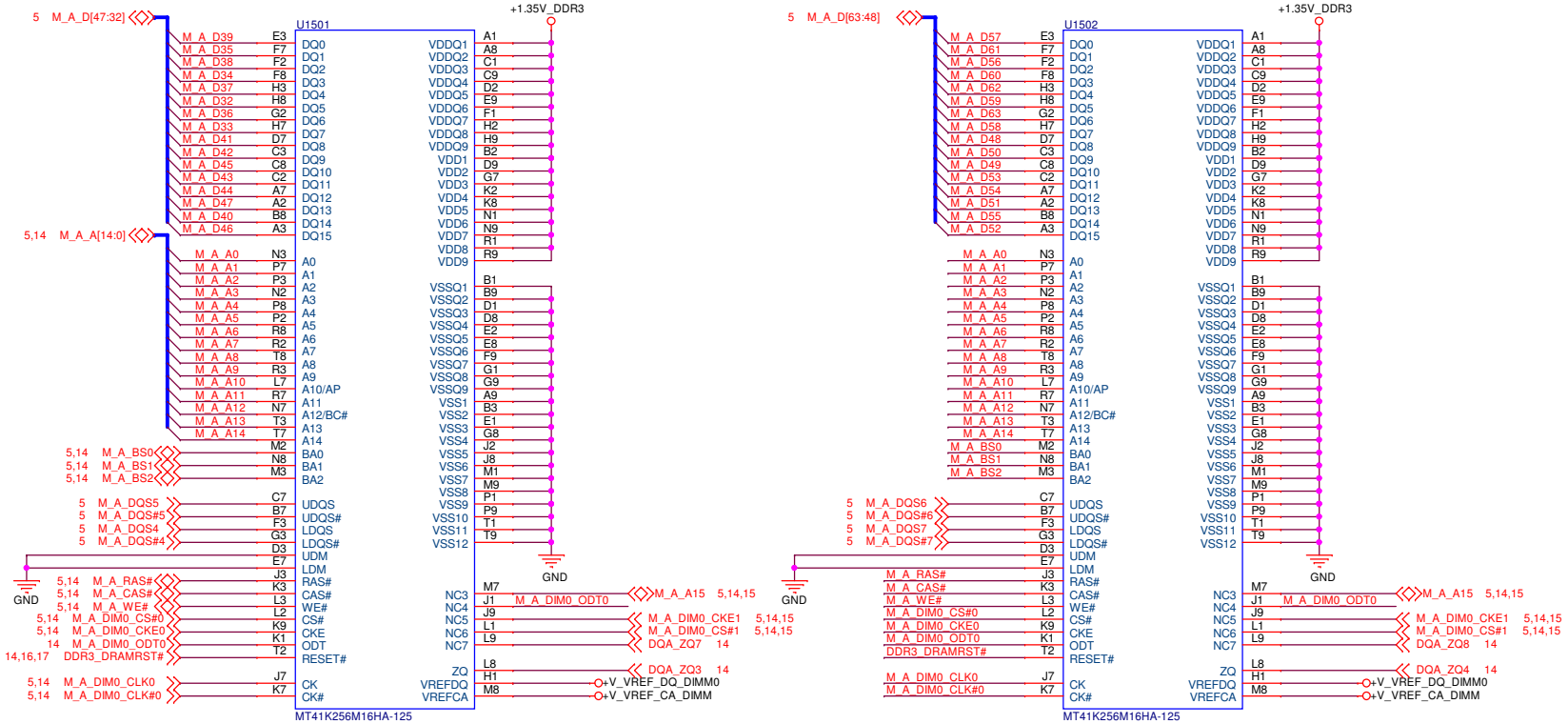
CPU XDP connector

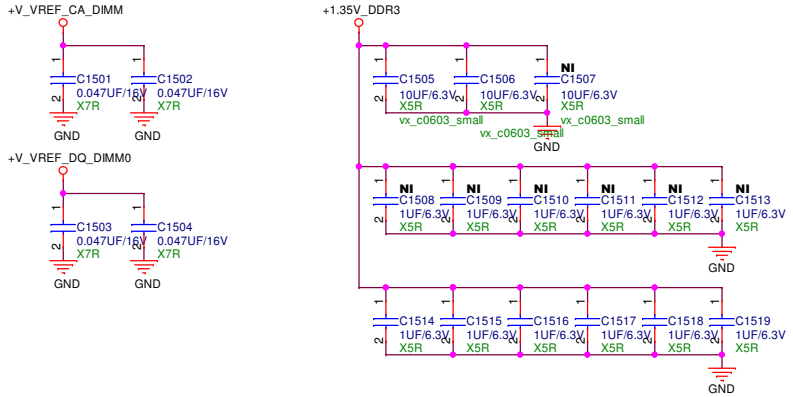
Intel recommend (R1.0 on 9/10)
XDP pin 40, 42/HOOK4, 5 should be left Open, unstuff R1006, R1007.



PEGATRON	Title :	CPU_PCH_XDP	
PEGATRON CORPORATION	Engineer:	Chinhung_Wang	
Size: A3	Project Name: Junction		Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 10 of 98		


U1401
MT41K256M16HA-125
U1402
MT41K256M16HA-125
+1.35V_DDR3
+V_VDDQ_VTT
+V_VREF_CA_DIMM
+V_VREF_DQ_DIMM0
+DDR_V
JP1401
3MM_OPEN_5MIL
R1443 470Ohm 1%
R1442 0Ohm
C1401 0.1UF/10V X7R
CE1401 220UF/4V
GND
PEGATRON
PEGATRON CORPORATION
Title : DDR3L-rs(1)_MEMORY D
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
Sheet 14 of 98





PEGATRON

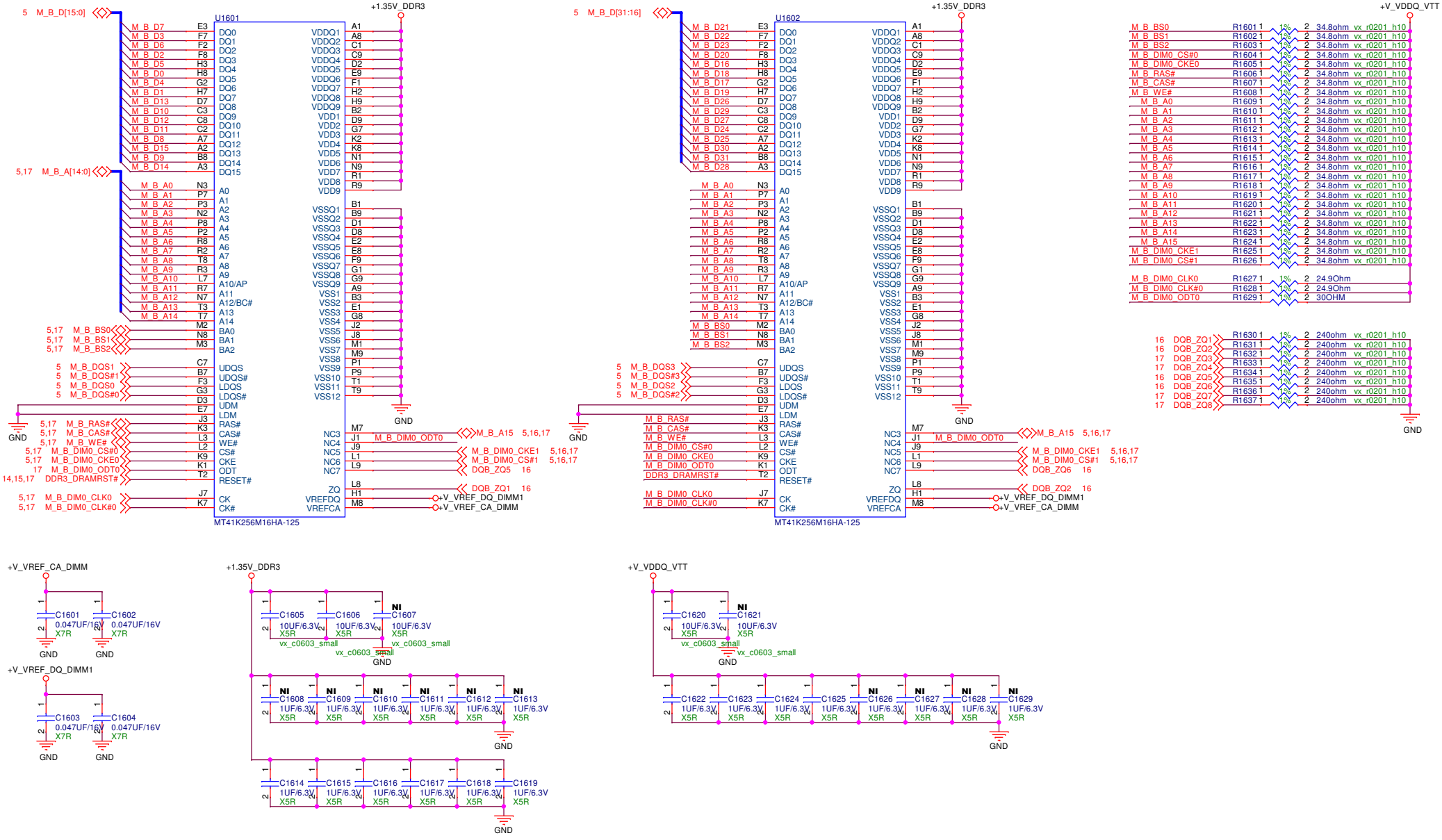
Title : DDR3L-rs(2)_MEMORY D

PEGATRON CORPORATION

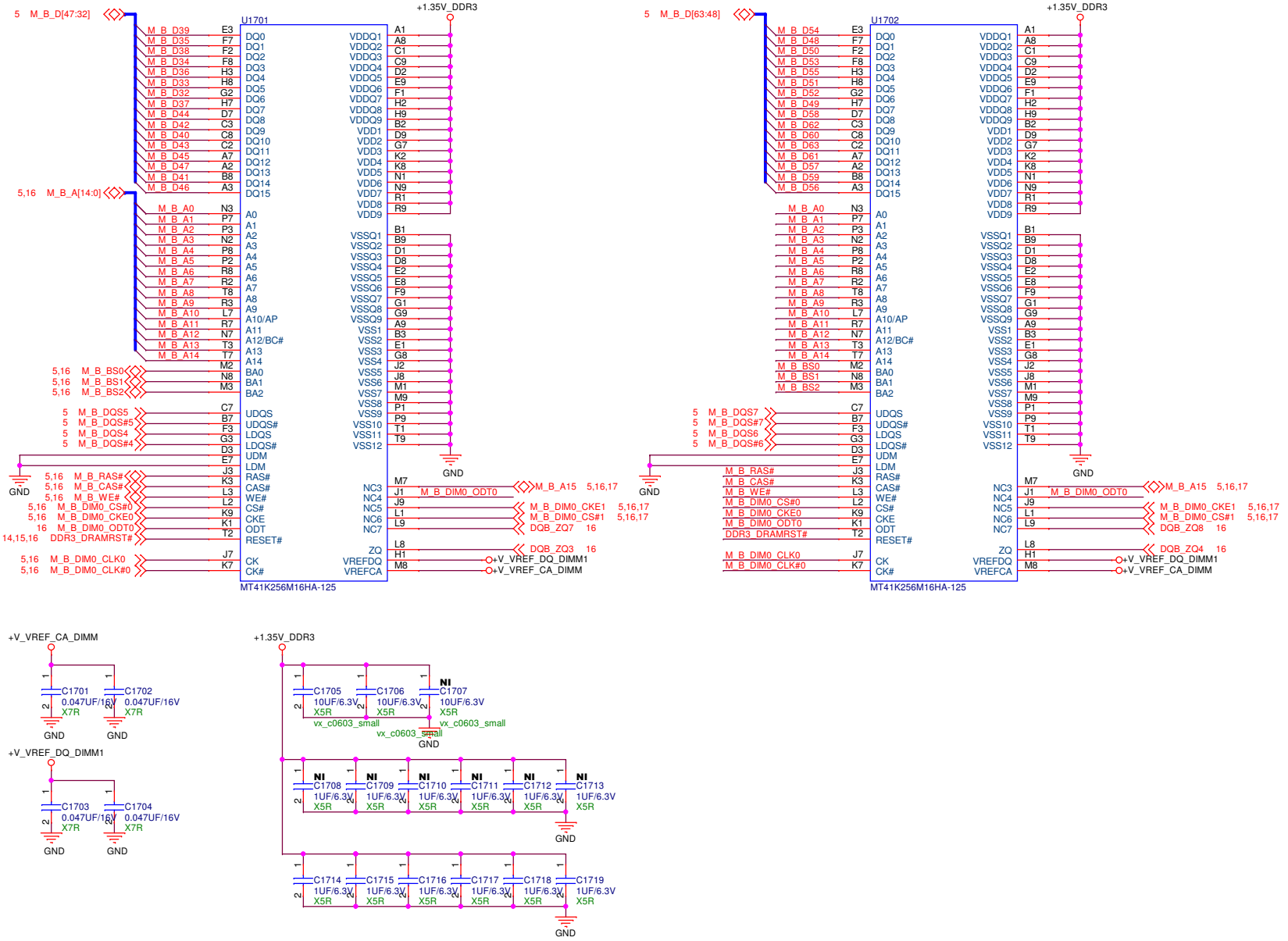
Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 15 of 98



PEGATRON	Title :	DDR3L-rs(3)_MEMORY D	
PEGATRON CORPORATION	Engineer:	Chinhung_Wang	
Size: A3	Project Name: Junction		Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 16 of 98		



PEGATRON

Title : DDR3L-rs(4)_MEMORY D

PEGATRON CORPORATION

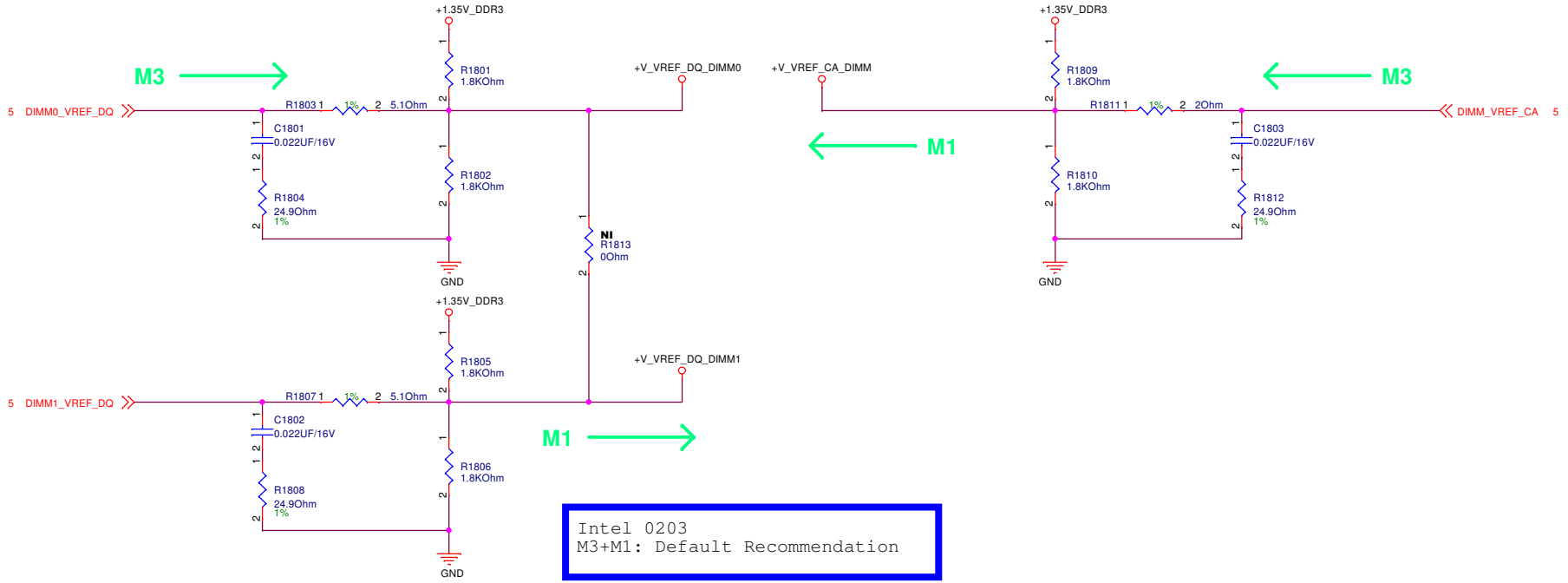
Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

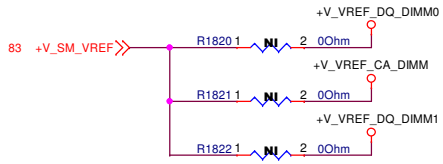
Date: Tuesday, September 24, 2013 Sheet 17 of 98

DDR3L Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



Intel 0203
M3+M1: Default Recommendation



<Variant Name>

PEGATRON Title : DDR3_rs(5)_CA/DQ Volta
PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 18 of 98

PEGATRON Title : VID Controller

PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 19 of 98

RTC battery

+RTCBAT, T2004, R2001 1KOhm, +RTC_BAT, D2001 0.8V/0.2mA, +3VA, +VCC_RTC, R2008 NI 0Ohm, C2003 1UF/6.3V X5R, J2001 WTOB_CON_2P 12V17GBSM083 (SIDE2, SIDE1), GND

GND, 18PF/50V C2001 NPO, XTAL_32K_X1, X2001 32.768KHZ, R2002 10MOhm, 18PF/50V C2002 NPO, XTAL_32K_X2

RTCRST# RC delay should be 18ms~25ms

+VCC_RTC, R2003 20KOhm, C2004 1UF/6.3V X5R, JRST2001 SGL_JUMP, GND

TPM Settings	JRST2001
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

R2005 1MOhm, GND

+VCC_RTC, R2006 330KOhm, NI, R2012 330KOhm, GND

T2002

SM_INTRUDER#, PCH_INTVRMEN, SRTC_RST#, RTC_RST#

R2004 20KOhm

CMOS Settings	JRST2002
Clear CMOS	Shunt
Keep CMOS	Open (Default)

C2005 1UF/6.3V X5R, JRST2002 SGL_JUMP, GND, GND

+AUD_DVDDIO, R2013 NI 1KOhm

HDA_BCLK_R, HDA_SYNC_R, HDA_RST#_R, HDA_SDI1_DSP, HDA_SDO_R (INT. PD), HDA_DOCK_EN#, HDA_DOCK_RST#, I2S1_SCLK

EC reset CMOS

30 SW_RTCRST, NI Q2001 2N7002, NI R2010 10KOhm, GND

R2015 33Ohm, R2014 33Ohm, R2016 33Ohm

36 HDA_BCLK_DSP, 36 HDA_SYNC_DSP, 36 HDA_RST#_DSP, 36 HDA_SDI0_DSP

HDA_SDO:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

2.HDA_SDOwhich sample high on the rising edge of PWROK
Will also disable Intel ME.

+3VA, R2034 1KOhm, Q2003 SI2301CDS-T1-GE3, 30 ME_WP#, +5VS, Q2002 2N7002, R2017 33Ohm, 36 HDA_SDO_DSP

C2006 10PF/50V NPO, C2007 10PF/50V NPO, C2008 10PF/50V NPO, C2009 10PF/50V NPO

+1.05VSUS, +3VSUS_ORG

R2024 51Ohm R4, R2023 51Ohm R3d, R2025 51Ohm R5, NI R2026 1KOhm R8

NI R2039 220Ohm 1%, NI R2038 220Ohm 1%, NI R2040 220Ohm 1%

4,10 XDP_TRST#
10 PCH_JTAG_TCK
10 PCH_JTAG_TDI
10 PCH_JTAG_TDO
10 PCH_JTAG_TMS
10 PCH_JTAGX

NI R2022 51Ohm R6, GND

NI R2043 100Ohm 1%, NI R2042 100Ohm 1%, NI R2041 100Ohm 1%, GND, GND, GND

U0301E — HASWELL_MCP_E

RTC: RTCX1, RTCX2, INTRUDER#, INTVRMEN, SRTCRST#, RTCRST#

AUDIO: HDA_BCLK/I2S0_SCLK, HDA_SYNC/I2S0_SFRM, HDA_RST#/I2S_MCLK#, HDA_SDI0/I2S0_RXD, HDA_SDI1/I2S1_RXD, HDA_SDO/I2S0_TXD, DOCKEN#/I2S1_TXD#, HDA_DOCK_RST#/I2S1_SFRM#, I2S1_SCLK

JTAG: PCH_TRST#, PCH_TCK, PCH_TDI, PCH_TDO, PCH_TMS, RSVD41, RSVD35, JTAGX, RSVD1

SATA: SATA_RN0/PERN6_L3, SATA_RP0/PERP6_L3, SATA_TN0/PETN6_L3, SATA_TP0/PETP6_L3, SATA_RN1/PERN6_L2, SATA_RP1/PERP6_L2, SATA_TN1/PETN6_L2, SATA_TP1/PETP6_L2, SATA_RN2/PERN6_L1, SATA_RP2/PERP6_L1, SATA_TN2/PETN6_L1, SATA_TP2/PETP6_L1, SATA_RN3/PERN6_L0, SATA_RP3/PERP6_L0, SATA_TN3/PETN6_L0, SATA_TP3/PETP6_L0, SATA0GP/GPIO34, SATA1GP/GPIO35, SATA2GP/GPIO36, SATA3GP/GPIO37, SATA_IREF, RSVD50, RSVD48, SATA_RCOMP, SATALED#

haswell_mcp

J5 SATA_RXN0 55, SATA_RXP0 55, SATA_TXN0 55, SATA_TXP0 55 — NGFF SSD

J8, J6, F5

V1 INT. PU, U1 INT. PU, V6 INT. PU SATA_ODD_PRSNT# R2044 NI 0Ohm, AC1 INT. PU

A12 SATA_IREF, L11, K10, C12, U3

+3VS, R2035 10KOhm, R2011 10KOhm, NI R2021 100KOhm

EXT_SMI# 30, CR_RST#_PCH 22, WWAN_PRESENCE 54, PCB_ID0 25

R2036 0Ohm, GND

+1.05VS_ASATA3PLL

SATA_COMP 3.01KOHM R2007, +3VS

SATALED# 10KOhm R2009

<Variant Name>

PEGATRON Title : PCH(1)_SATA,IHDA,RTC,
PEGATRON CORPORATION Engineer: Chinhung_Wang

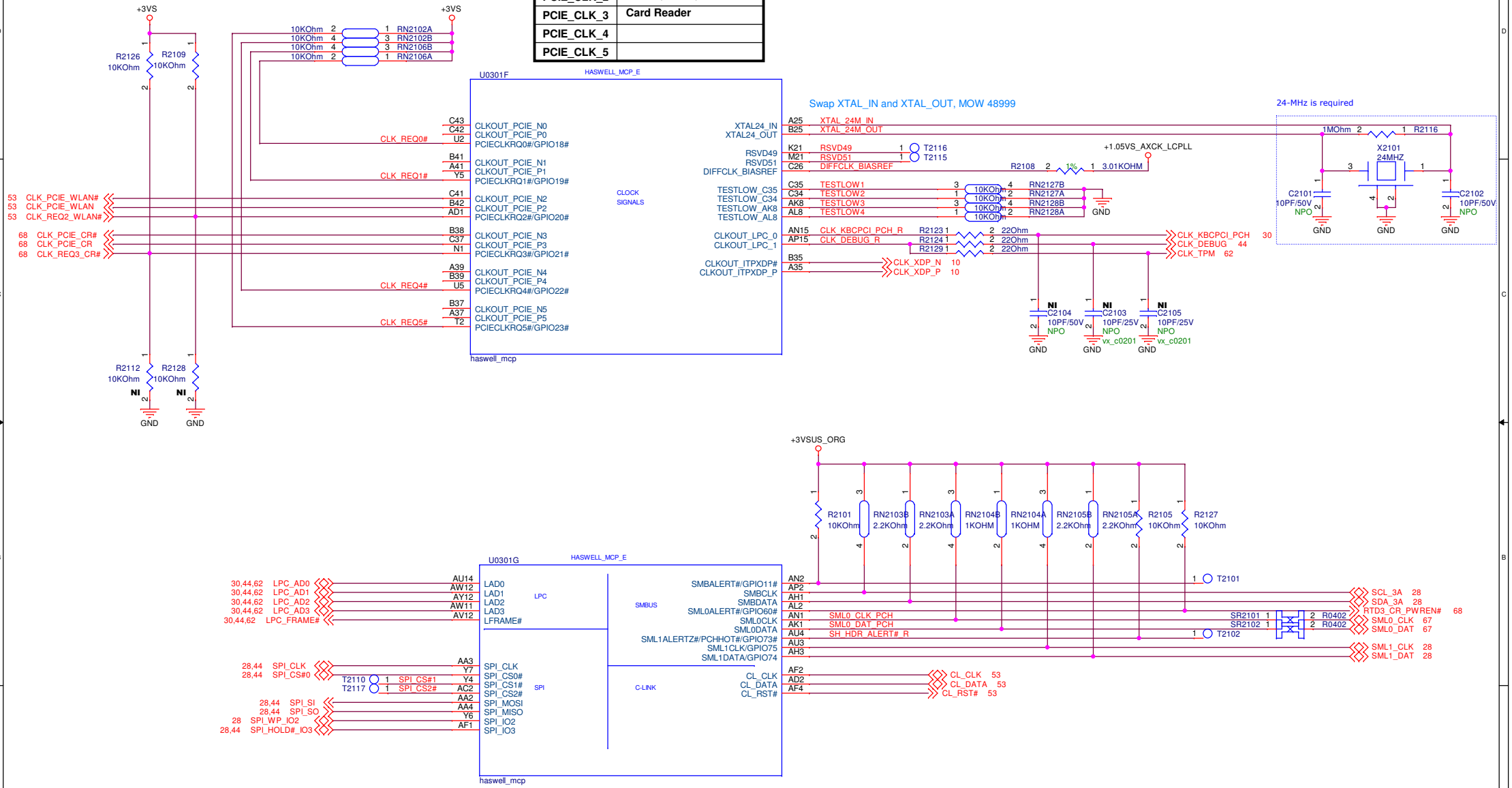
Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 20 of 98

PCIE_CLK_0	
PCIE_CLK_1	
PCIE_CLK_2	NGFF (WLAN)
PCIE_CLK_3	Card Reader
PCIE_CLK_4	
PCIE_CLK_5	

Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

PCH CLKREQ Setting:
Not connected to device.
PCIECLKRQ[5:0]# are core well powered.



<Variant Name>

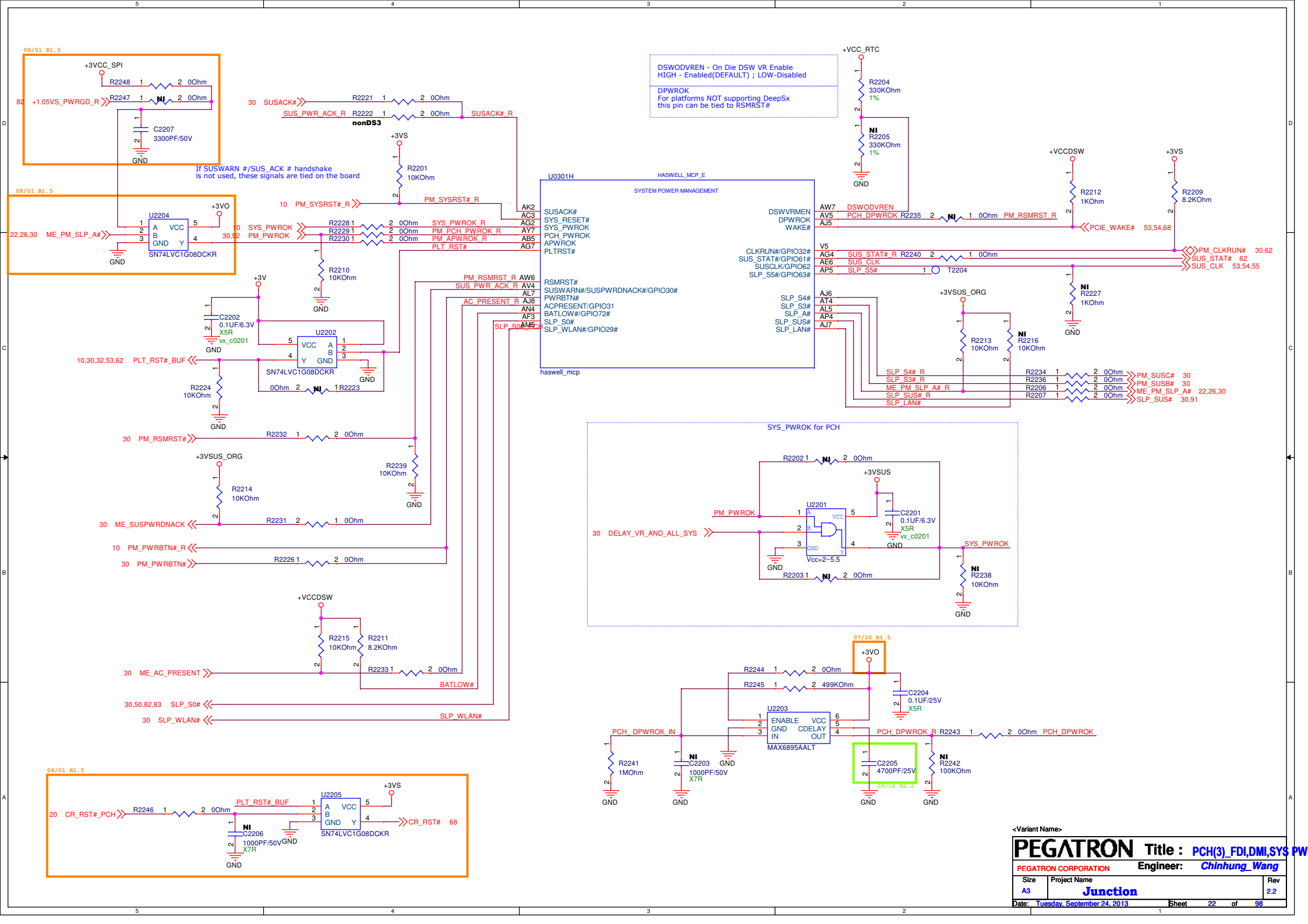
PEGATRON CORPORATION

Title : PCH(2)_PCIE,CLK,SMB,P

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 21 of 98



<Variant Name>

PEGATRON

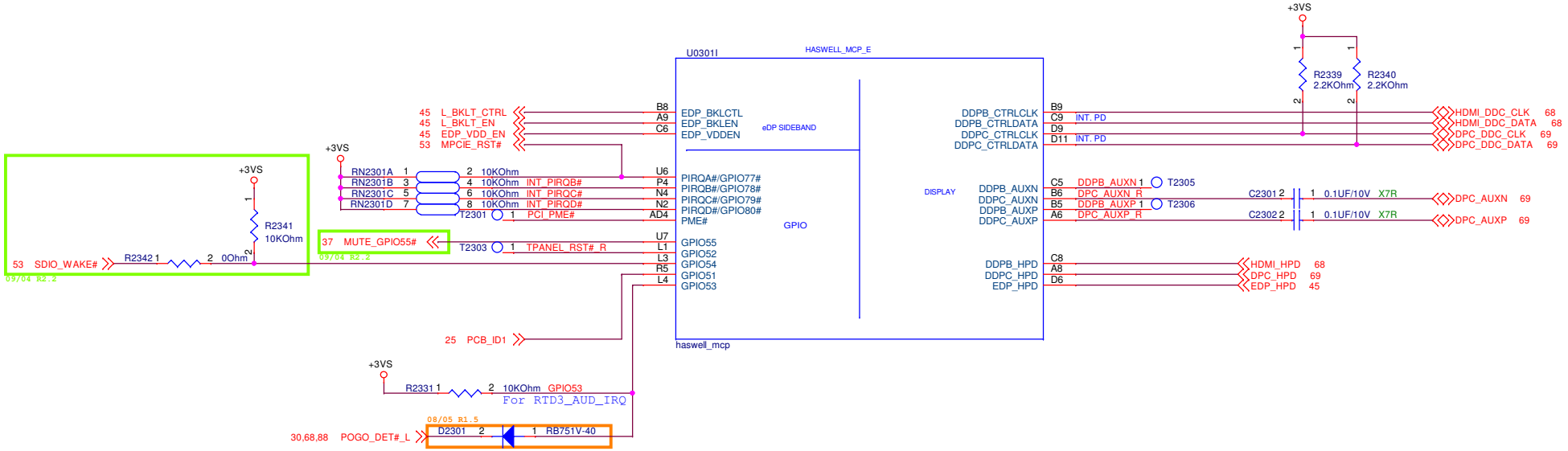
Title : PCH(3)_FDI,DMI,SYS PW

PEGATRON CORPORATION

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 22 of 98



<Variant Name>

PEGATRON CORPORATION

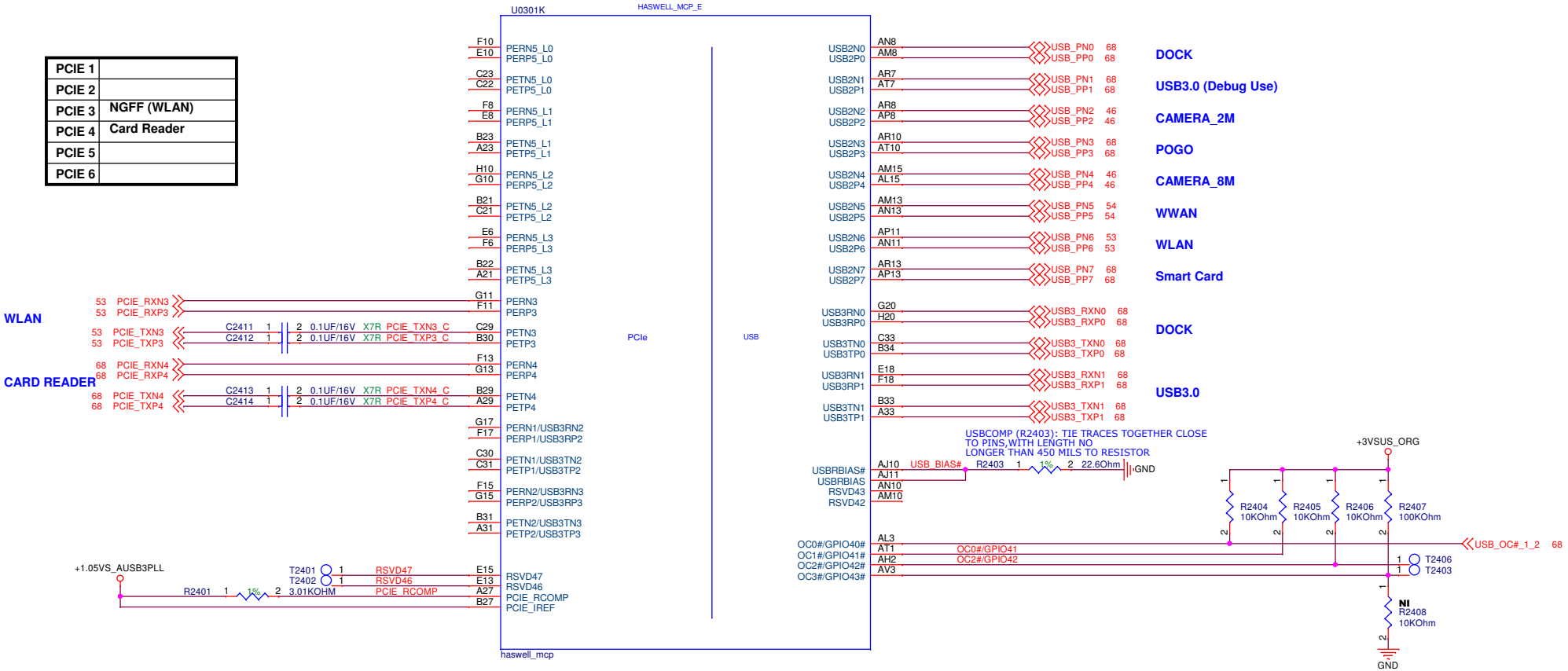
Title : PCH(4)_DP,LVDS,CRT

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 23 of 98

PCIE 1	
PCIE 2	
PCIE 3	NGFF (WLAN)
PCIE 4	Card Reader
PCIE 5	
PCIE 6	

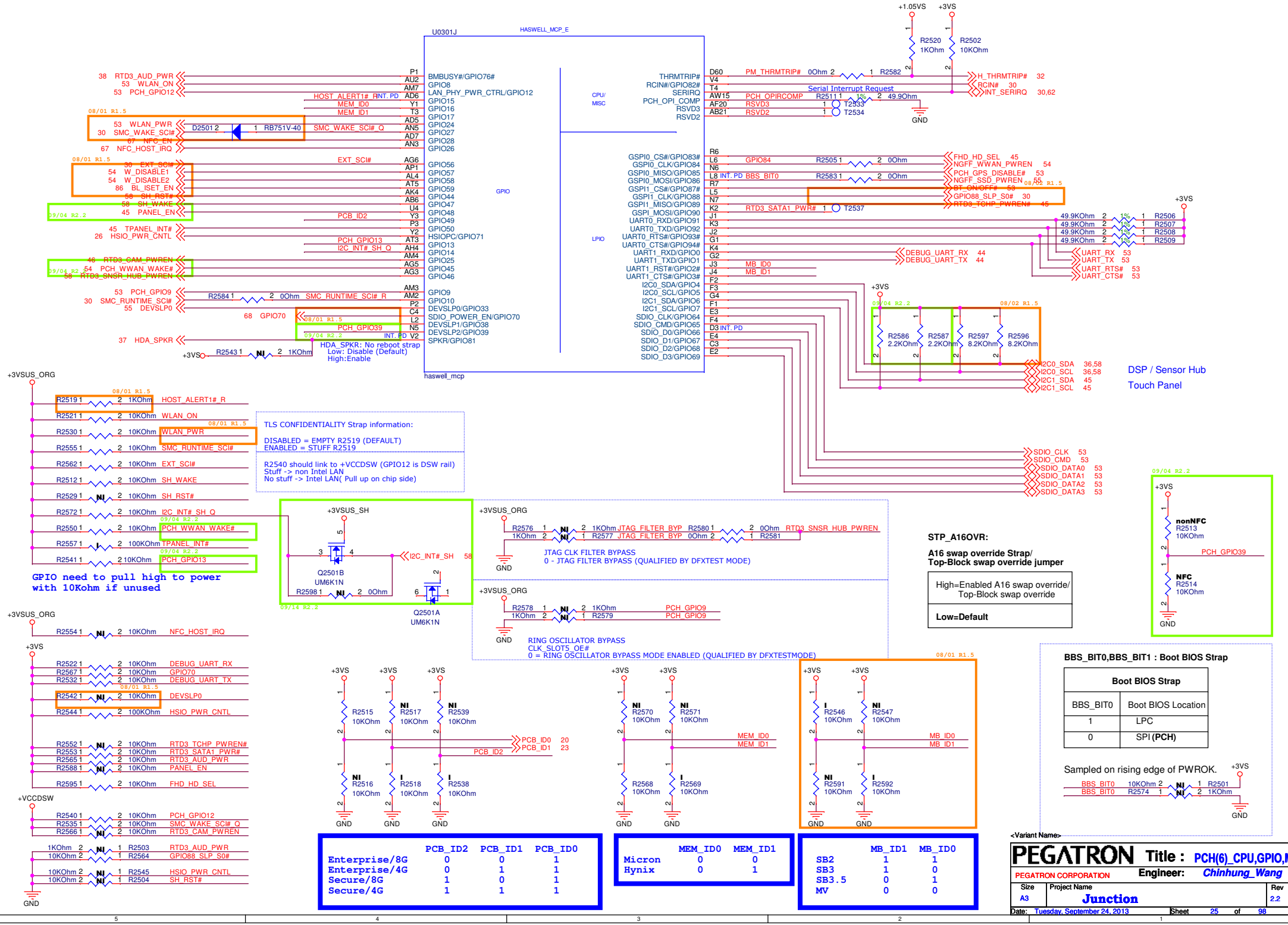


PEGATRON Title : PCH(5)_PCI,NVRAM,USB

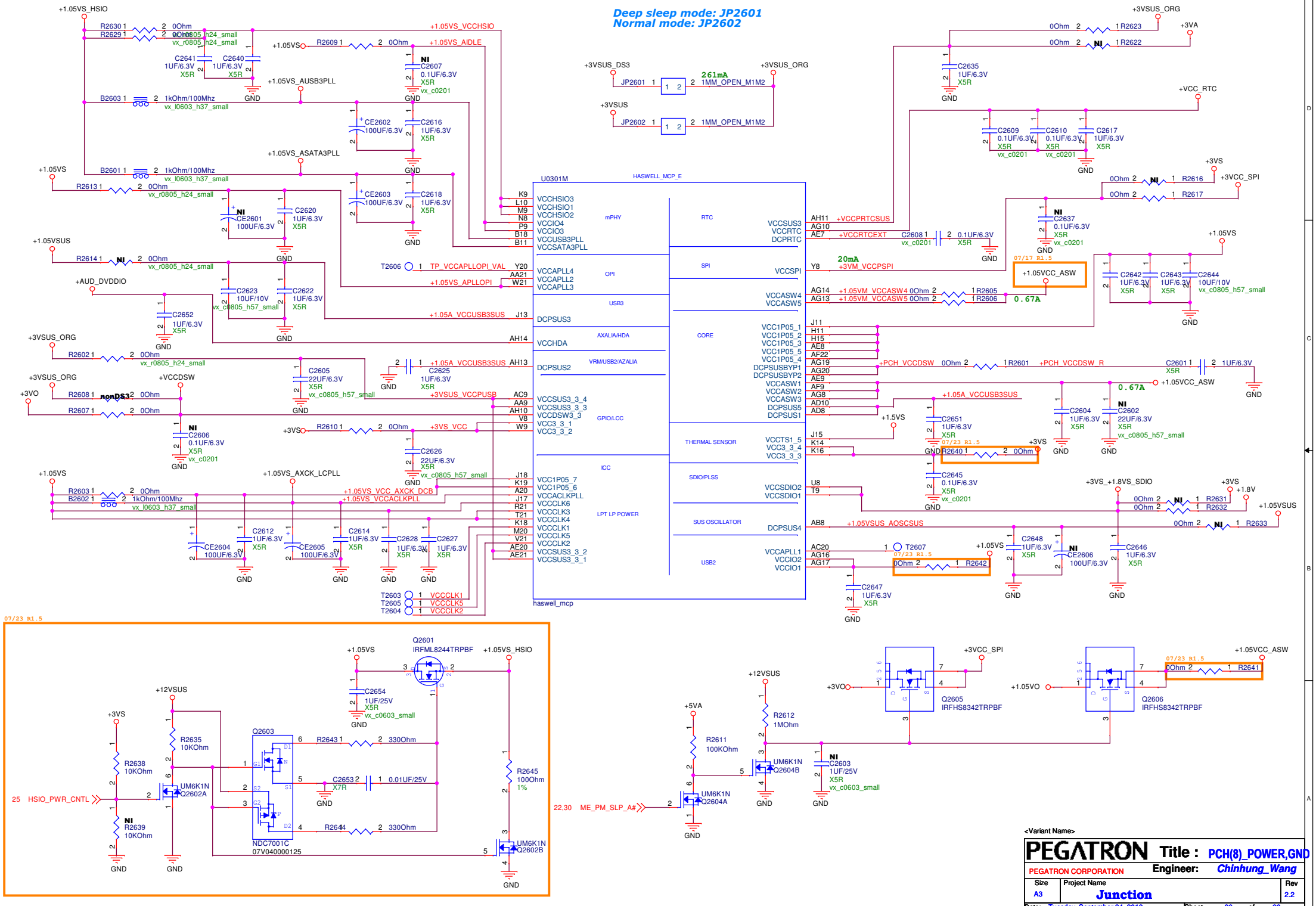
PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 24 of 98


U0301J
HASWELL_MCP_E
haswell_mcp
GPIO
CPU/ MISC
LPIO
BMBUSY#/GPIO76#
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
GPIO15
GPIO16
GPIO17
GPIO24
GPIO27
GPIO28
GPIO26
GPIO56
GPIO57
GPIO58
GPIO59
GPIO44
GPIO47
GPIO48
GPIO49
GPIO50
HSIOPC/GPIO71
GPIO13
GPIO14
GPIO25
GPIO45
GPIO46
GPIO9
GPIO10
DEVSLP0/GPIO33
SDIO_POWER_EN/GPIO70
DEVSLP1/GPIO38
DEVSLP2/GPIO39
SPKR/GPIO81
THRMTRIP#
RCIN#/GPIO82#
SERIRQ
PCH_OPI_COMP
RSVD3
RSVD2
GSPI0_CS#/GPIO83#
GSPI0_CLK/GPIO84
GSPI0_MISO/GPIO85
GSPI0_MOSI/GPIO86
GSPI1_CS#/GPIO87#
GSPI1_CLK/GPIO88
GSPI1_MISO/GPIO89
GSPI_MOSI/GPIO90
UART0_RXD/GPIO91
UART0_TXD/GPIO92
UART0_RTS#/GPIO93#
UART0_CTS#/GPIO94#
UART1_RXD/GPIO0
UART1_TXD/GPIO1
UART1_RST#/GPIO2#
UART1_CTS#/GPIO3#
I2C0_SDA/GPIO4
I2C0_SCL/GPIO5
I2C1_SDA/GPIO6
I2C1_SCL/GPIO7
SDIO_CLK/GPIO64
SDIO_CMD/GPIO65
SDIO_D0/GPIO66
SDIO_D1/GPIO67
SDIO_D2/GPIO68
SDIO_D3/GPIO69
+1.05VS
+3VS
R2520 1KOhm
R2502 10KOhm
D60 PM_THRMTRIP# 0Ohm R2582
H_THRMTRIP# 32
RCIN# 30
INT_SERIRQ 30,62
Serial Interrupt Request
PCH_OPIRCOMP R2511 1% 49.9Ohm
RSVD3 T2533
RSVD2 T2534
GND
38 RTD3_AUD_PWR
53 WLAN_ON
53 PCH_GPIO12
HOST_ALERT1# INT. PD
MEM_ID0
MEM_ID1
08/01 R1.5
53 WLAN_PWR
30 SMC_WAKE_SCI#
67 NFC_EN
67 NFC_HOST_IRQ
D2501 RB751V-40
SMC_WAKE_SCI# Q
EXT_SCI#
30 EXT_SCI#
54 W_DISABLE1
54 W_DISABLE2
86 BL_ISET_EN
59 SH_RST#
58 SH_WAKE
09/04 R2.2
45 PANEL_EN
PCB_ID2
45 TPANEL_INT#
26 HSIO_PWR_CNTL
PCH_GPIO13
I2C_INT# SH_Q
46 RTD3_CAM_PWREN
54 PCH_WWAN_WAKE#
58 RTD3_SNSR_HUB_PWREN
53 PCH_GPIO9
30 SMC_RUNTIME_SCI#
55 DEVSLP0
R2584 0Ohm SMC_RUNTIME_SCI# R
68 GPIO70
PCH_GPIO39
37 HDA_SPKR
R2543 NI 1KOhm
HDA_SPKR: No reboot strap
Low: Disable (Default)
High:Enable
GPIO88_SLP_S0# 30
RTD3_TCHP_PWREN# 45
BT_ONOFF# 59
FHD_HD_SEL 45
NGFF_WWAN_PWREN 54
PCH_GPS_DISABLE# 53
NGFF_SSD_PWREN 55
R2505 0Ohm
R2583 0Ohm
INT. PD BBS_BIT0
GPIO84
RTD3_SATA1_PWR# T2537
49.9KOhm R2506
49.9KOhm R2507
49.9KOhm R2508
49.9KOhm R2509
UART_RX 53
UART_TX 53
UART_RTS# 53
UART_CTS# 53
DEBUG_UART_RX 44
DEBUG_UART_TX 44
MB_ID0
MB_ID1
R2586 2.2KOhm
R2587 2.2KOhm
R2597 8.2KOhm
R2596 8.2KOhm
I2C0_SDA 36,58
I2C0_SCL 36,58
I2C1_SDA 45
I2C1_SCL 45
DSP / Sensor Hub
Touch Panel
SDIO_CLK 53
SDIO_CMD 53
SDIO_DATA0 53
SDIO_DATA1 53
SDIO_DATA2 53
SDIO_DATA3 53
+3VSUS_ORG
R2519 1KOhm HOST_ALERT1# R
R2521 10KOhm WLAN_ON
R2530 10KOhm WLAN_PWR
R2555 10KOhm SMC_RUNTIME_SCI#
R2562 10KOhm EXT_SCI#
R2512 10KOhm SH_WAKE
R2529 NI 10KOhm SH_RST#
R2572 10KOhm I2C_INT# SH_Q
R2550 10KOhm PCH_WWAN_WAKE#
R2557 I 100KOhm TPANEL_INT#
R2541 10KOhm PCH_GPIO13
GPIO need to pull high to power with 10Kohm if unused
TLS CONFIDENTIALITY Strap information:
DISABLED = EMPTY R2519 (DEFAULT)
ENABLED = STUFF R2519
R2540 should link to +VCCDSW (GPIO12 is DSW rail)
Stuff -> non Intel LAN
No stuff -> Intel LAN(Pull up on chip side)
+3VSUS_SH
Q2501B UM6K1N
R2598 NI 0Ohm
I2C_INT#_SH 58
Q2501A UM6K1N
+3VSUS_ORG
R2576 NI 1KOhm
R2577 JTAG_FILTER_BYP 0Ohm
R2580 0Ohm RTD3_SNSR_HUB_PWREN
R2581
JTAG CLK FILTER BYPASS
0 - JTAG FILTER BYPASS (QUALIFIED BY DFXTEST MODE)
R2578 NI 1KOhm PCH_GPIO9
R2579 PCH_GPIO9
RING OSCILLATOR BYPASS
CLK_SLOT5_OE#
0 = RING OSCILLATOR BYPASS MODE ENABLED (QUALIFIED BY DFXTESTMODE)
STP_A16OVR:
A16 swap override Strap/
Top-Block swap override jumper
High=Enabled A16 swap override/ Top-Block swap override
Low=Default
nonNFC R2513 10KOhm
NFC R2514 10KOhm
PCH_GPIO39
BBS_BIT0,BBS_BIT1 : Boot BIOS Strap
Boot BIOS Strap
BBS_BIT0 | Boot BIOS Location
1 | LPC
0 | SPI (PCH)
Sampled on rising edge of PWROK.
BBS_BIT0 10KOhm R2574 NI R2501 1KOhm
+3VSUS_ORG
R2554 NI 10KOhm NFC_HOST_IRQ
R2522 10KOhm DEBUG_UART_RX
R2567 10KOhm GPIO70
R2532 10KOhm DEBUG_UART_TX
R2542 NI 10KOhm DEVSLP0
R2544 100KOhm HSIO_PWR_CNTL
R2552 NI 10KOhm RTD3_TCHP_PWREN#
R2553 10KOhm RTD3_SATA1_PWR#
R2565 10KOhm RTD3_AUD_PWR
R2588 NI 10KOhm PANEL_EN
R2595 10KOhm FHD_HD_SEL
+VCCDSW
R2540 10KOhm PCH_GPIO12
R2535 10KOhm SMC_WAKE_SCI# Q
R2566 NI 10KOhm RTD3_CAM_PWREN
1KOhm NI R2503 RTD3_AUD_PWR
10KOhm R2564 GPIO88_SLP_S0#
10KOhm NI R2545 HSIO_PWR_CNTL
10KOhm NI R2504 SH_RST#
R2515 10KOhm
NI R2517 10KOhm
NI R2539 10KOhm
NI R2516 10KOhm
I R2518 10KOhm
I R2538 10KOhm
PCB_ID0 20
PCB_ID1 23
PCB_ID2
PCB_ID2 PCB_ID1 PCB_ID0
Enterprise/8G 0 0 1
Enterprise/4G 0 1 1
Secure/8G 1 0 1
Secure/4G 1 1 1
NI R2570 10KOhm
NI R2571 10KOhm
R2568 10KOhm
I R2569 10KOhm
MEM_ID0
MEM_ID1
MEM_ID0 MEM_ID1
Micron 0 1
Hynix 0 1
I R2546 10KOhm
NI R2547 10KOhm
NI R2591 10KOhm
I R2592 10KOhm
MB_ID0
MB_ID1
MB_ID1 MB_ID0
SB2 1 1
SB3 1 0
SB3.5 0 1
MV 0 0
GND
<Variant Name>
PEGATRON
Title : PCH(6)_CPU,GPIO,MISC
PEGATRON CORPORATION
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
Sheet 25 of 98

Deep sleep mode: JP2601
Normal mode: JP2602



<Variant Name>

PEGATRON Title : PCH(8)_POWER,GND

PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 26 of 98

PEGATRON

Title : PCH(7)_POWER,GND

PEGATRON CORPORATION

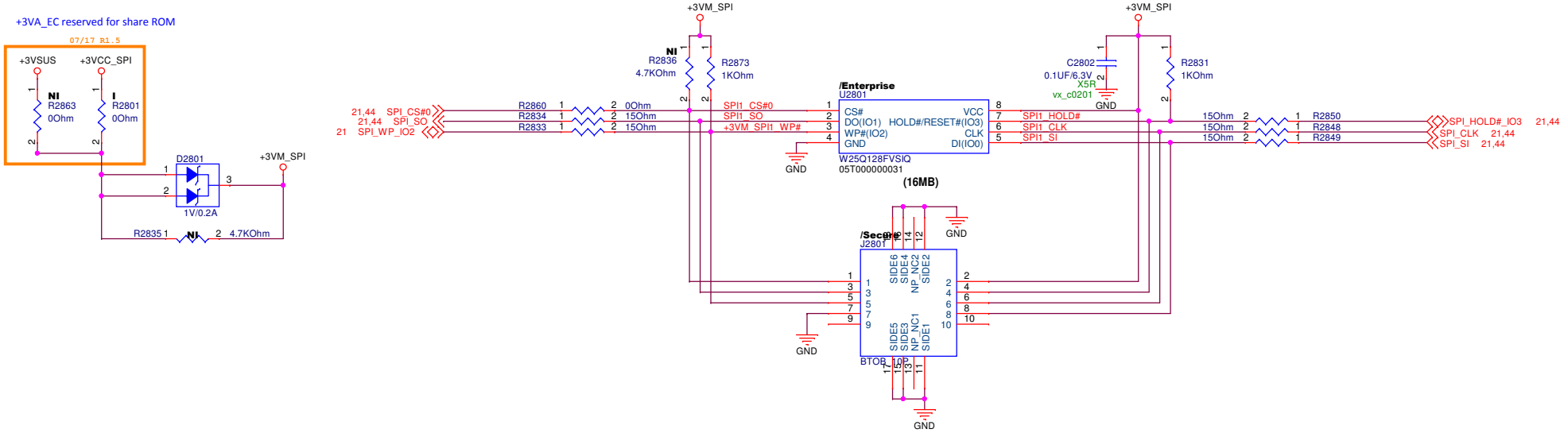
Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

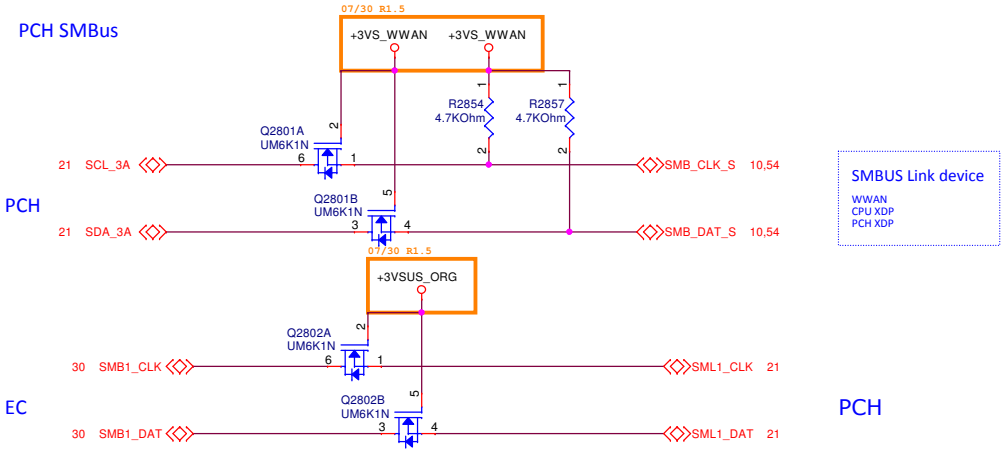
Date: Tuesday, September 24, 2013 Sheet 27 of 98

PCH SPI ROM

+3VA_EC reserved for share ROM



PCH SMBus

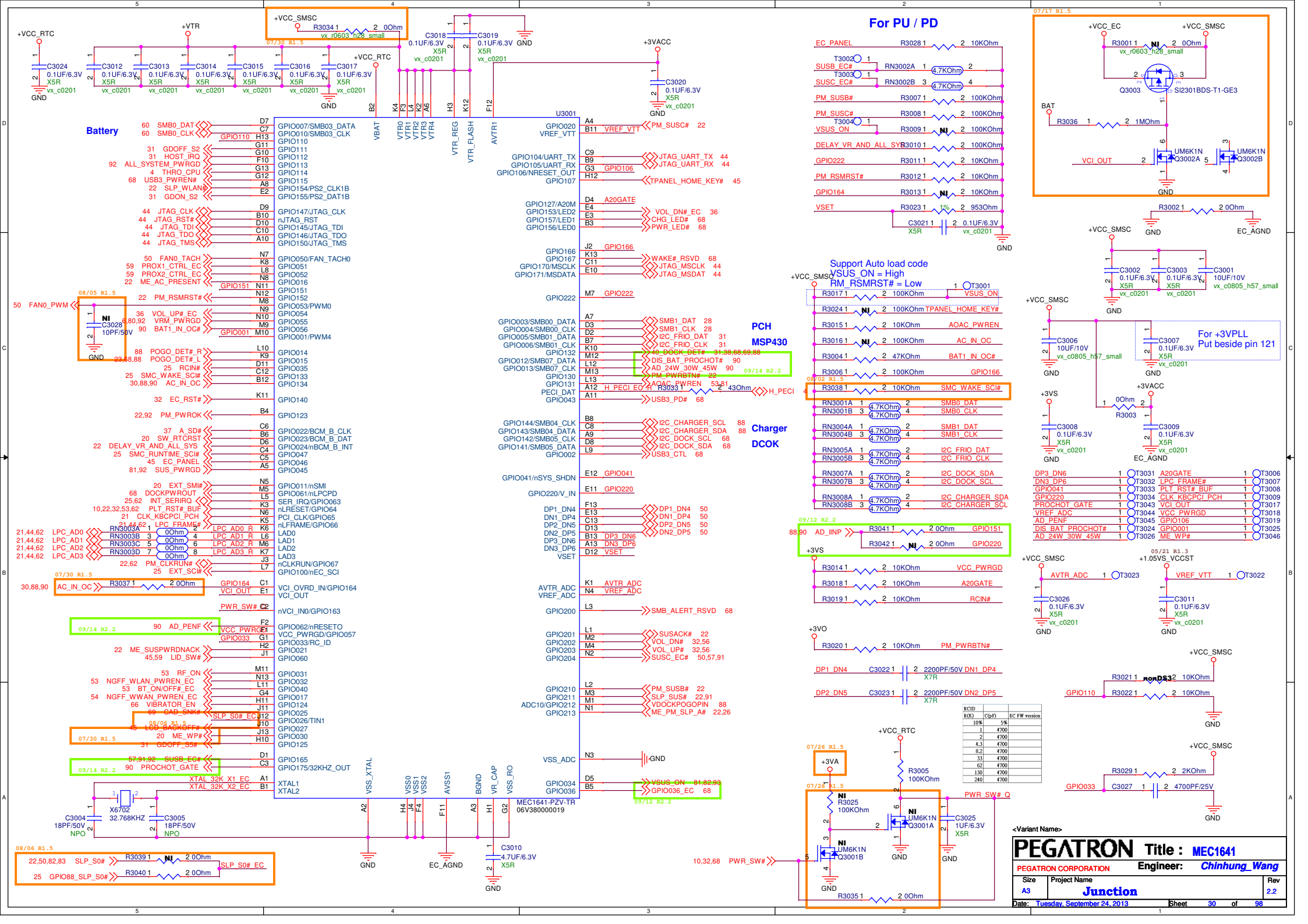


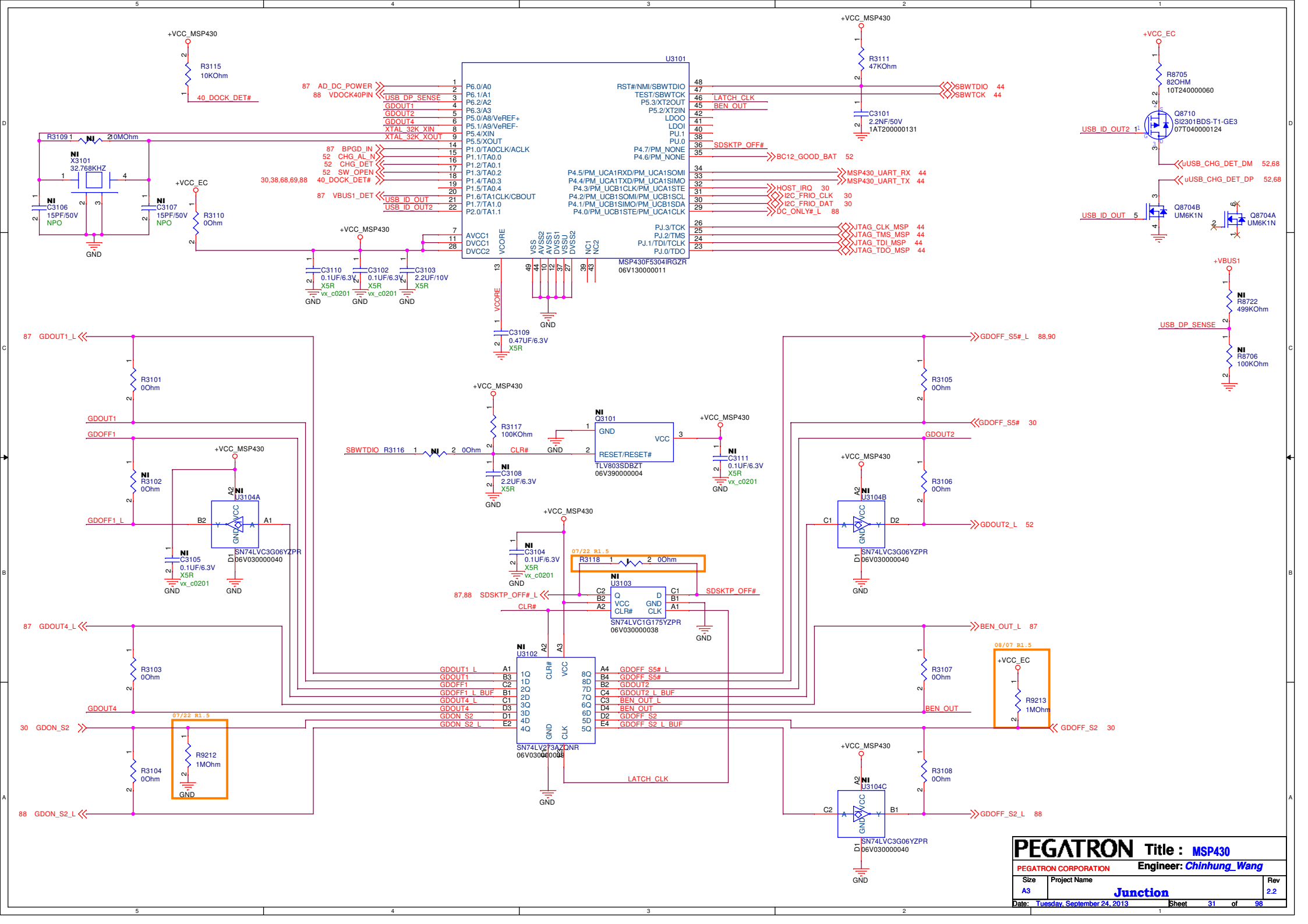
SMBUS Link device

WWAN
CPU XDP
PCH XDP

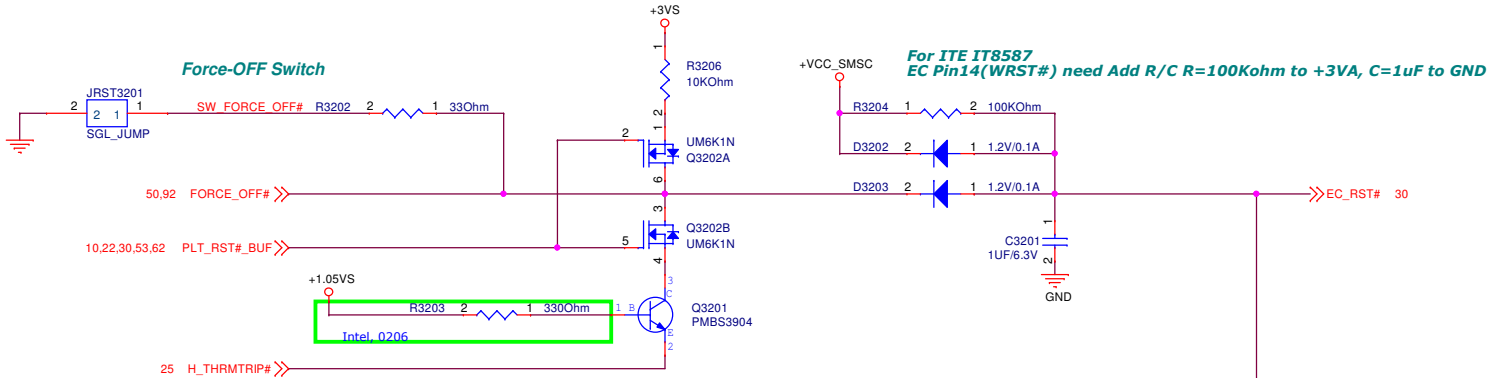
PCH

PEGATRON	Title : PCH(9)_SPI,SMB	
PEGATRON CORPORATION	Engineer: Chinhung_Wang	
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 28 of 98	

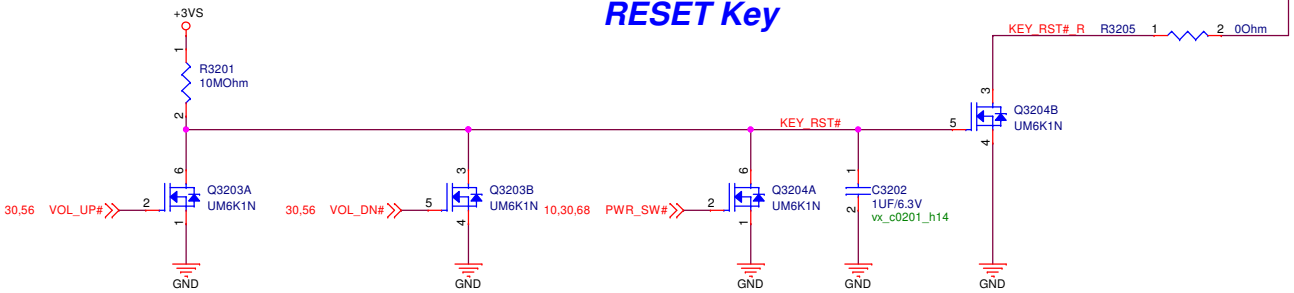

For PU / PD
Battery
PCH
MSP430
Charger
DCOK
Support Auto load code
VSUS_ON = High
RM_RSMRST# = Low
For +3VPLL
Put beside pin 121
MEC1641-PZV-TR
06V380000019
PEGATRON
Title : MEC1641
PEGATRON CORPORATION
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
Sheet 30 of 98


U3101
MSP430F5304IRGZR
06V130000011
+VCC_MSP430
+VCC_EC
R3115 10KOhm
R3111 47KOhm
R8705 82OHM 10T240000060
Q8710 SI2301BDS-T1-GE3 07T040000124
Q8704B UM6K1N
Q8704A UM6K1N
R3109 210MOhm
X3101 32.768KHZ
C3106 15PF/50V NPO
C3107 15PF/50V NPO
R3110 0Ohm
C3101 2.2NF/50V 1AT200000131
C3110 0.1UF/6.3V X5R
C3102 0.1UF/6.3V X5R
C3103 2.2UF/10V X5R
C3109 0.47UF/6.3V X5R
R8722 499KOhm
R8706 100KOhm
R3101 0Ohm
R3102 0Ohm
R3103 0Ohm
R3104 0Ohm
R3105 0Ohm
R3106 0Ohm
R3107 0Ohm
R3108 0Ohm
R9212 1MOhm
R9213 1MOhm
R3117 100KOhm
C3108 2.2UF/6.3V X5R
C3111 0.1UF/6.3V X5R
C3104 0.1UF/6.3V X5R
C3105 0.1UF/6.3V X5R
R3118 0Ohm
Q3101 TLV803SDBZT 06V390000004
U3104A U3104B U3104C SN74LVC3G06YZPR 06V030000040
U3102 SN74LVC273AZQNR 06V030000038
U3103 SN74LVC1G175YZPR 06V030000038
07/22 R1.5
08/07 R1.5
AD_DC_POWER
VDOCK40PIN
USB_DP_SENSE
GDOUT1
GDOUT4
XTAL_32K_XIN
XTAL_32K_XOUT
BPGD_IN
CHG_AL_N
CHG_DET
SW_OPEN
40_DOCK_DET#
VBUS1_DET
USB_ID_OUT
USB_ID_OUT2
LATCH_CLK
BEN_OUT
SDSKTP_OFF#
BC12_GOOD_BAT
MSP430_UART_RX
MSP430_UART_TX
HOST_IRQ
I2C_FRIO_CLK
I2C_FRIO_DAT
DC_ONLY#_L
JTAG_CLK_MSP
JTAG_TMS_MSP
JTAG_TDI_MSP
JTAG_TDO_MSP
SBWTDIO
SBWTCK
uUSB_CHG_DET_DM
uUSB_CHG_DET_DP
USB_ID_OUT
USB_ID_OUT2
USB_DP_SENSE
+VBUS1
GDOUT1_L
GDOUT1
GDOFF1
GDOFF1_L
GDOUT4_L
GDOUT4
GDON_S2
GDON_S2_L
SBWTDIO_R3116
CLR#
SDSKTP_OFF#_L
GDOFF_S5#_L
GDOFF_S5#
GDOUT2
GDOUT2_L
BEN_OUT_L
BEN_OUT
GDOFF_S2
GDOFF_S2_L
GDOUT1_L_BUF
GDOUT4_L
GDON_S2_L
GDOFF1_L_BUF
GDOFF_S2_L_BUF
GND
PEGATRON
PEGATRON CORPORATION
Title : MSP430
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
Sheet 31 of 98

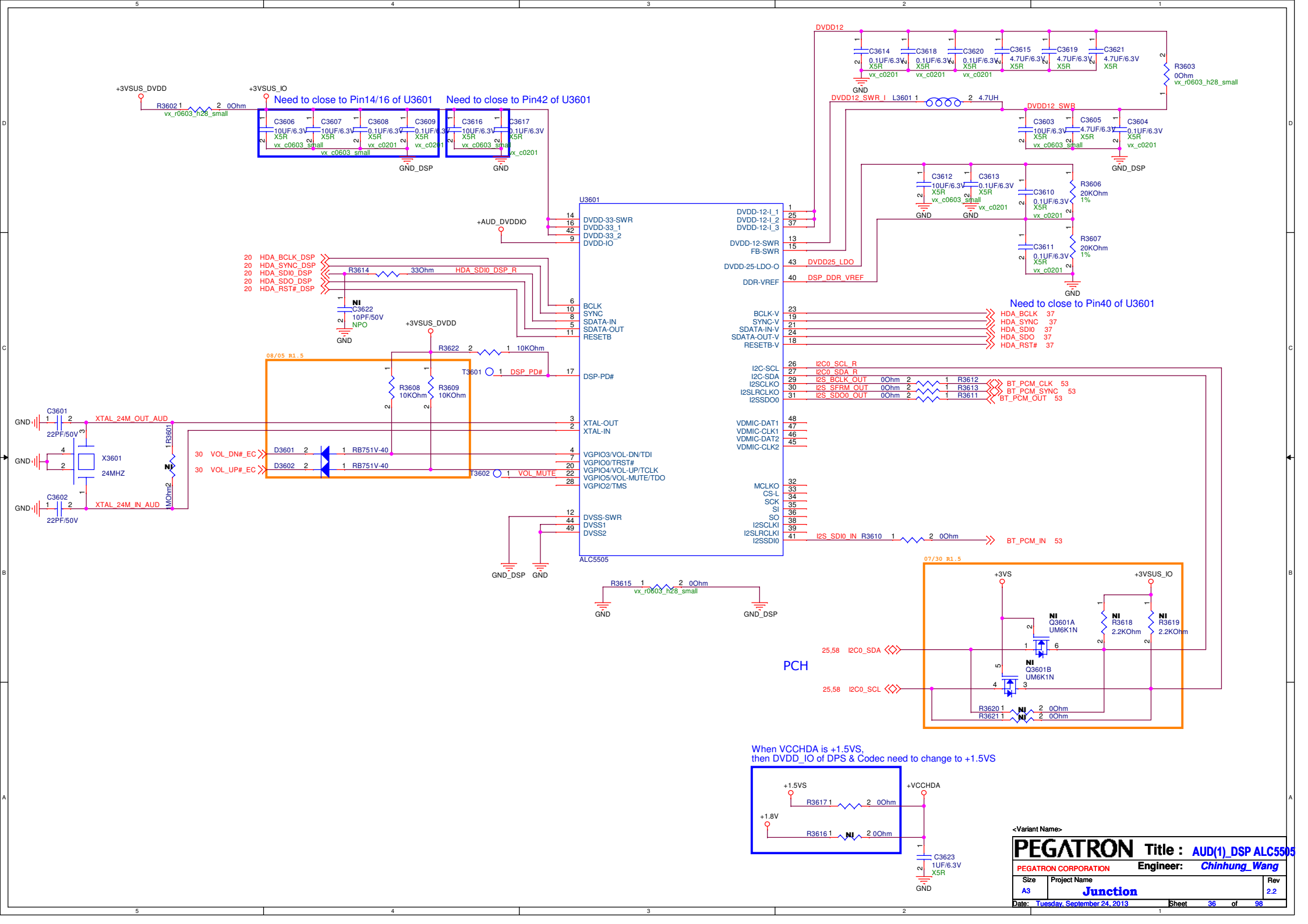
Thermal Policy

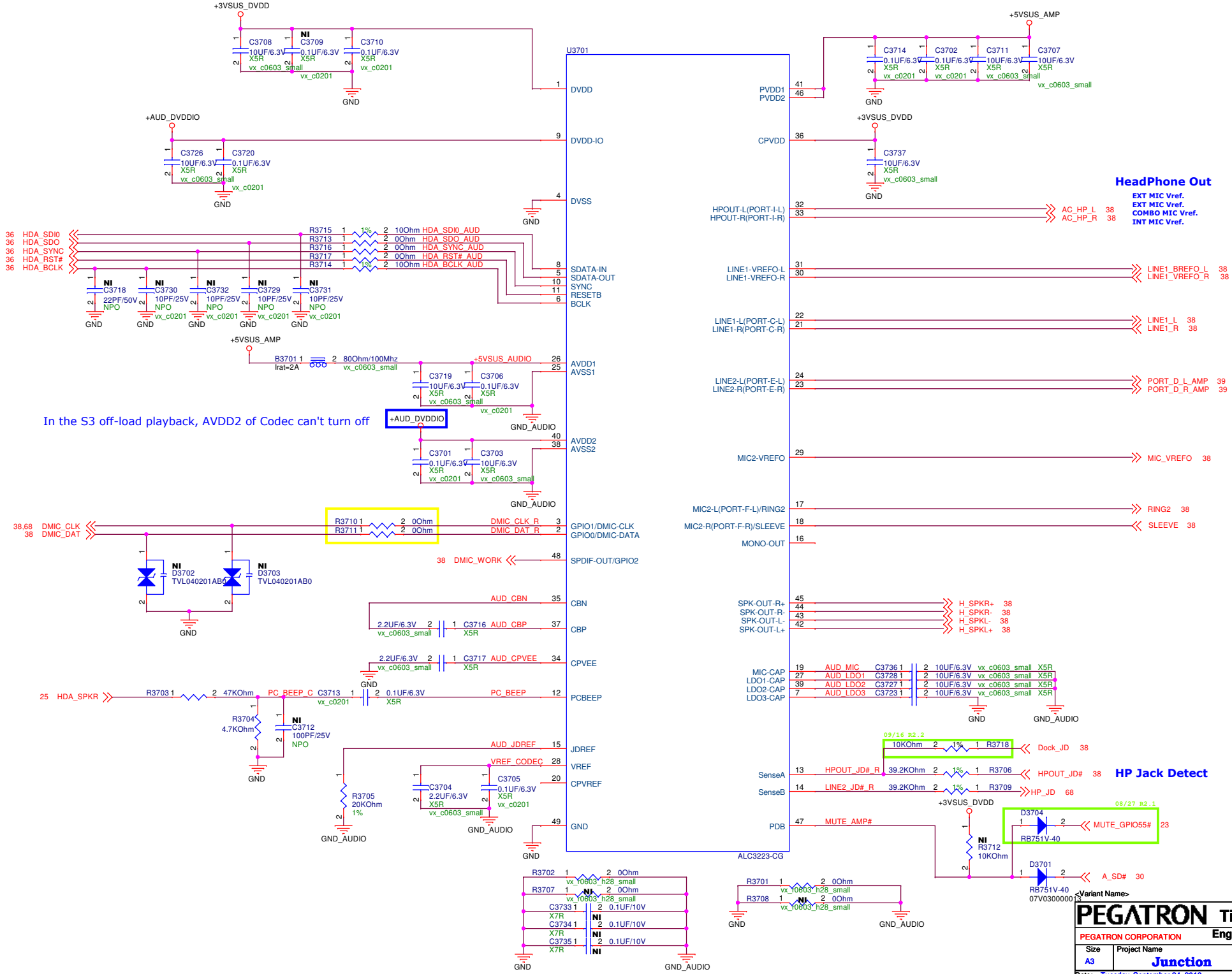


RESET Key



PEGATRON	Title : RST_Reset Circuit	
PEGATRON CORPORATION	Engineer: Chinhung_Wang	
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 32 of 98	


DVDD12
C3614 0.1UF/6.3V X5R vx_c0201
C3618 0.1UF/6.3V X5R vx_c0201
C3620 0.1UF/6.3V X5R vx_c0201
C3615 4.7UF/6.3V X5R
C3619 4.7UF/6.3V X5R
C3621 4.7UF/6.3V X5R
R3603 0Ohm vx_r0603_h28_small
GND
DVDD12_SWR_I L3601 1 2 4.7UH
DVDD12_SWR
C3603 10UF/6.3V X5R vx_c0603_small
C3605 4.7UF/6.3V X5R vx_c0603_small
C3604 0.1UF/6.3V X5R vx_c0201
GND_DSP
+3VSUS_DVDD
+3VSUS_IO
R3602 1 2 0Ohm vx_r0603_h28_small
Need to close to Pin14/16 of U3601
C3606 10UF/6.3V X5R vx_c0603_small
C3607 10UF/6.3V X5R vx_c0603_small
C3608 0.1UF/6.3V X5R vx_c0201
C3609 0.1UF/6.3V X5R vx_c0201
Need to close to Pin42 of U3601
C3616 10UF/6.3V X5R vx_c0603_small
C3617 0.1UF/6.3V X5R vx_c0201
GND_DSP
GND
C3612 10UF/6.3V X5R vx_c0603_small
C3613 0.1UF/6.3V X5R vx_c0201
C3610 0.1UF/6.3V X5R vx_c0201
R3606 20KOhm 1%
C3611 0.1UF/6.3V X5R vx_c0201
R3607 20KOhm 1%
GND
U3601
+AUD_DVDDIO
14 DVDD-33-SWR
16 DVDD-33_1
42 DVDD-33_2
9 DVDD-IO
1 DVDD-12-I_1
25 DVDD-12-I_2
37 DVDD-12-I_3
13 DVDD-12-SWR
15 FB-SWR
43 DVDD-25-LDO-O
DVDD25_LDO
40 DDR-VREF
DSP_DDR_VREF
20 HDA_BCLK_DSP
20 HDA_SYNC_DSP
20 HDA_SDI0_DSP
20 HDA_SDO_DSP
20 HDA_RST#_DSP
R3614 33Ohm HDA_SDI0_DSP_R
NI C3622 10PF/50V NPO
6 BCLK
10 SYNC
8 SDATA-IN
5 SDATA-OUT
11 RESETB
23 BCLK-V
19 SYNC-V
21 SDATA-IN-V
24 SDATA-OUT-V
18 RESETB-V
HDA_BCLK 37
HDA_SYNC 37
HDA_SDI0 37
HDA_SDO 37
HDA_RST# 37
Need to close to Pin40 of U3601
+3VSUS_DVDD
R3622 2 1 10KOhm
08/05 R1.5
T3601 1 DSP_PD#
17 DSP-PD#
R3608 10KOhm
R3609 10KOhm
26 I2C0_SCL_R
27 I2C0_SDA_R
I2C-SCL
I2C-SDA
I2SCLKO
I2SLRCLKO
I2SSDO0
29 I2S_BCLK_OUT 0Ohm R3612
30 I2S_SFRM_OUT 0Ohm R3613
31 I2S_SDO0_OUT 0Ohm R3611
BT_PCM_CLK 53
BT_PCM_SYNC 53
BT_PCM_OUT 53
C3601 22PF/50V
XTAL_24M_OUT_AUD
3 XTAL-OUT
2 XTAL-IN
X3601 24MHZ
1R3601
1MOhm2
C3602 22PF/50V
XTAL_24M_IN_AUD
30 VOL_DN#_EC
30 VOL_UP#_EC
D3601 2 1 RB751V-40
D3602 2 1 RB751V-40
T3602 1 VOL_MUTE
4 VGPIO3/VOL-DN/TDI
7 VGPIO0/TRST#
20 VGPIO4/VOL-UP/TCLK
22 VGPIO5/VOL-MUTE/TDO
28 VGPIO2/TMS
48 VDMIC-DAT1
47 VDMIC-CLK1
46 VDMIC-DAT2
45 VDMIC-CLK2
32 MCLKO
33 CS-L
34 SCK
35 SI
36 SO
38 I2SCLKI
39 I2SLRCLKI
41 I2SSDI0
I2S_SDI0_IN R3610 1 2 0Ohm
BT_PCM_IN 53
12 DVSS-SWR
44 DVSS1
49 DVSS2
GND_DSP
GND
ALC5505
R3615 1 2 0Ohm vx_r0603_h28_small
GND
GND_DSP
07/30 R1.5
+3VS
+3VSUS_IO
NI Q3601A UM6K1N
NI Q3601B UM6K1N
NI R3618 2.2KOhm
NI R3619 2.2KOhm
25,58 I2C0_SDA
25,58 I2C0_SCL
PCH
R3620 1 NI 2 0Ohm
R3621 1 NI 2 0Ohm
When VCCHDA is +1.5VS,
then DVDD_IO of DPS & Codec need to change to +1.5VS
+1.5VS
+1.8V
R3617 1 2 0Ohm
R3616 1 NI 2 0Ohm
+VCCHDA
C3623 1UF/6.3V X5R
GND
<Variant Name>
PEGATRON
Title : AUD(1)_DSP ALC5505
PEGATRON CORPORATION
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
Sheet 36 of 98



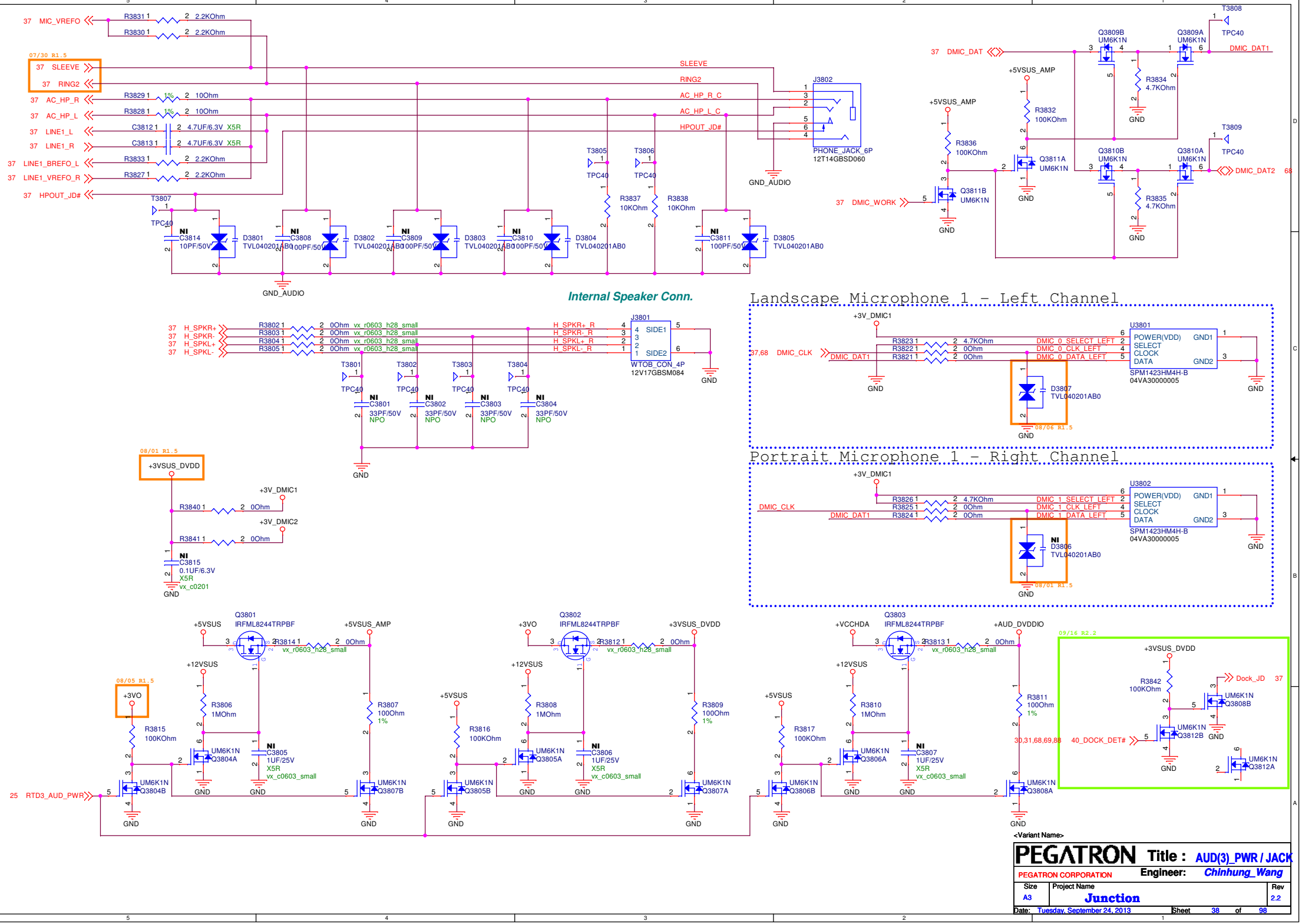
PEGATRON CORPORATION
Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Title : AUD(2)_ALC3223

Date: Tuesday, September 24, 2013 Sheet 37 of 98

<Variant Name>


37 MIC_VREFO
R3831 2.2KOhm
R3830 2.2KOhm
07/30 R1.5
37 SLEEVE
37 RING2
R3829 1% 10Ohm
37 AC_HP_R
R3828 1% 10Ohm
37 AC_HP_L
C3812 4.7UF/6.3V X5R
37 LINE1_L
C3813 4.7UF/6.3V X5R
37 LINE1_R
R3833 2.2KOhm
37 LINE1_BREFO_L
R3827 2.2KOhm
37 LINE1_VREFO_R
37 HPOUT_JD#
SLEEVE
RING2
AC_HP_R_C
AC_HP_L_C
HPOUT_JD#
J3802
PHONE_JACK_6P
12T14GBSD060
GND_AUDIO
T3807
TPC40
NI C3814 10PF/50V
D3801 TVL040201AB0
NI C3808 100PF/50V
D3802 TVL040201AB0
NI C3809 100PF/50V
D3803 TVL040201AB0
NI C3810 100PF/50V
D3804 TVL040201AB0
T3805
T3806
R3837 10KOhm
R3838 10KOhm
NI C3811 100PF/50V
D3805 TVL040201AB0
37 DMIC_DAT
Q3809B UM6K1N
Q3809A UM6K1N
T3808
TPC40
DMIC_DAT1
+5VSUS_AMP
R3834 4.7KOhm
R3832 100KOhm
R3836 100KOhm
Q3811A UM6K1N
Q3810B UM6K1N
Q3810A UM6K1N
T3809
TPC40
DMIC_DAT2 68
37 DMIC_WORK
Q3811B UM6K1N
R3835 4.7KOhm
GND
Internal Speaker Conn.
37 H_SPKR+
37 H_SPKR-
37 H_SPKL+
37 H_SPKL-
R3802 0Ohm vx_r0603_h28_small
R3803 0Ohm vx_r0603_h28_small
R3804 0Ohm vx_r0603_h28_small
R3805 0Ohm vx_r0603_h28_small
H_SPKR+_R
H_SPKR-_R
H_SPKL+_R
H_SPKL-_R
J3801
SIDE1
SIDE2
WTOB_CON_4P
12V17GBSM084
T3801
T3802
T3803
T3804
TPC40
NI C3801 33PF/50V NPO
NI C3802 33PF/50V NPO
NI C3803 33PF/50V NPO
NI C3804 33PF/50V NPO
Landscape Microphone 1 - Left Channel
+3V_DMIC1
37,68 DMIC_CLK
DMIC_DAT1
R3823 4.7KOhm
R3822 0Ohm
R3821 0Ohm
DMIC_0_SELECT_LEFT
DMIC_0_CLK_LEFT
DMIC_0_DATA_LEFT
U3801
POWER(VDD)
SELECT
CLOCK
DATA
GND1
GND2
SPM1423HM4H-B
04VA30000005
D3807 TVL040201AB0
08/06 R1.5
Portrait Microphone 1 - Right Channel
DMIC_CLK
DMIC_DAT1
R3826 4.7KOhm
R3825 0Ohm
R3824 0Ohm
DMIC_1_SELECT_LEFT
DMIC_1_CLK_LEFT
DMIC_1_DATA_LEFT
U3802
NI D3806 TVL040201AB0
08/01 R1.5
08/01 R1.5
+3VSUS_DVDD
+3V_DMIC1
R3840 0Ohm
+3V_DMIC2
R3841 0Ohm
NI C3815 0.1UF/6.3V X5R vx_c0201
Q3801 IRFML8244TRPBF
+5VSUS
+5VSUS_AMP
R3814 0Ohm vx_r0603_h28_small
+12VSUS
08/05 R1.5
+3VO
R3815 100KOhm
R3806 1MOhm
R3807 100Ohm 1%
NI C3805 1UF/25V X5R vx_c0603_small
UM6K1N Q3804A
UM6K1N Q3804B
UM6K1N Q3807B
25 RTD3_AUD_PWR
Q3802 IRFML8244TRPBF
+3VO
+3VSUS_DVDD
R3812 0Ohm vx_r0603_h28_small
R3816 100KOhm
R3808 1MOhm
R3809 100Ohm 1%
NI C3806 1UF/25V X5R vx_c0603_small
UM6K1N Q3805A
UM6K1N Q3805B
UM6K1N Q3807A
Q3803 IRFML8244TRPBF
+VCCHDA
+AUD_DVDDIO
R3813 0Ohm vx_r0603_h28_small
R3817 100KOhm
R3810 1MOhm
R3811 100Ohm 1%
NI C3807 1UF/25V X5R vx_c0603_small
UM6K1N Q3806A
UM6K1N Q3806B
UM6K1N Q3808A
30,31,68,69,88
09/16 R2.2
+3VSUS_DVDD
R3842 100KOhm
Dock_JD 37
UM6K1N Q3808B
UM6K1N Q3812B
40_DOCK_DET#
UM6K1N Q3812A
GND
<Variant Name>
PEGATRON
Title : AUD(3)_PWR / JACK
PEGATRON CORPORATION
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
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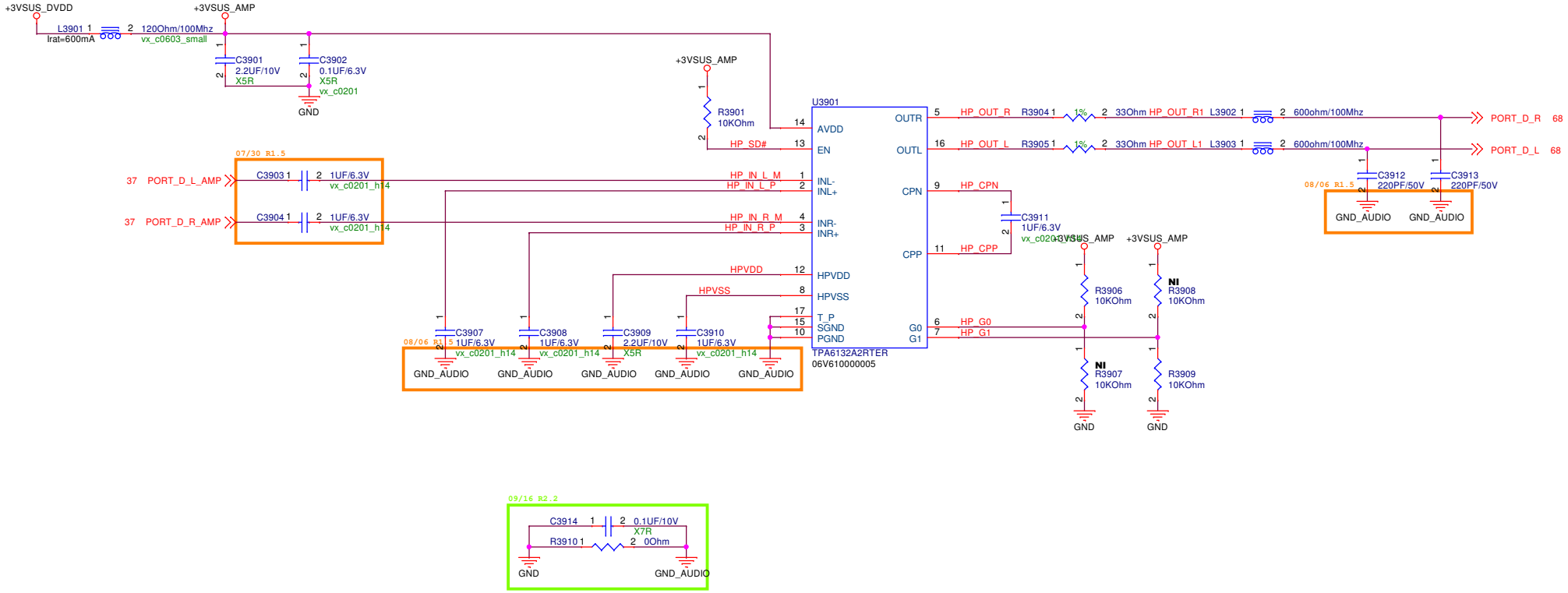
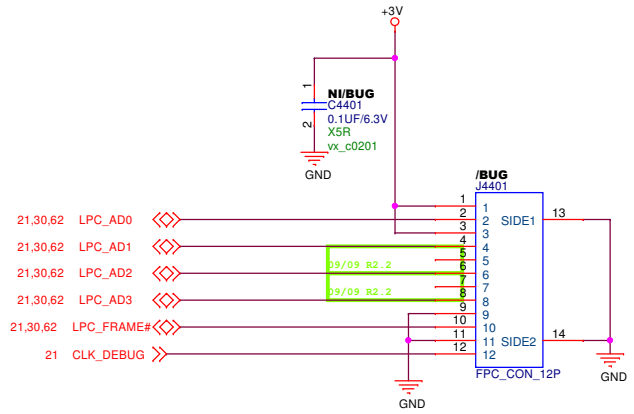
Docking Headphone out

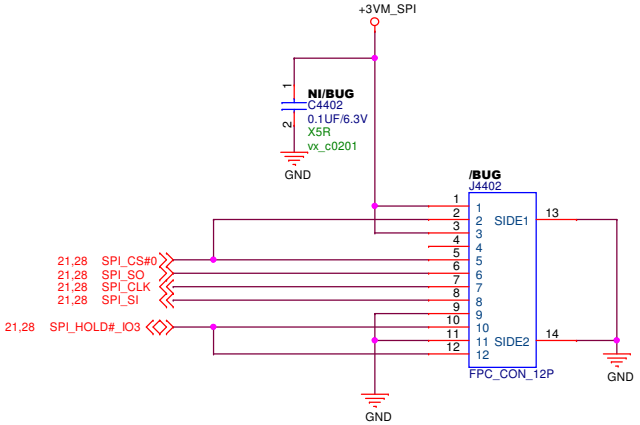


PEGATRON	Title :	AUD(4)_Docking Headph
PEGATRON CORPORATION	Engineer:	Chinhung_Wang
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 39 of 98	

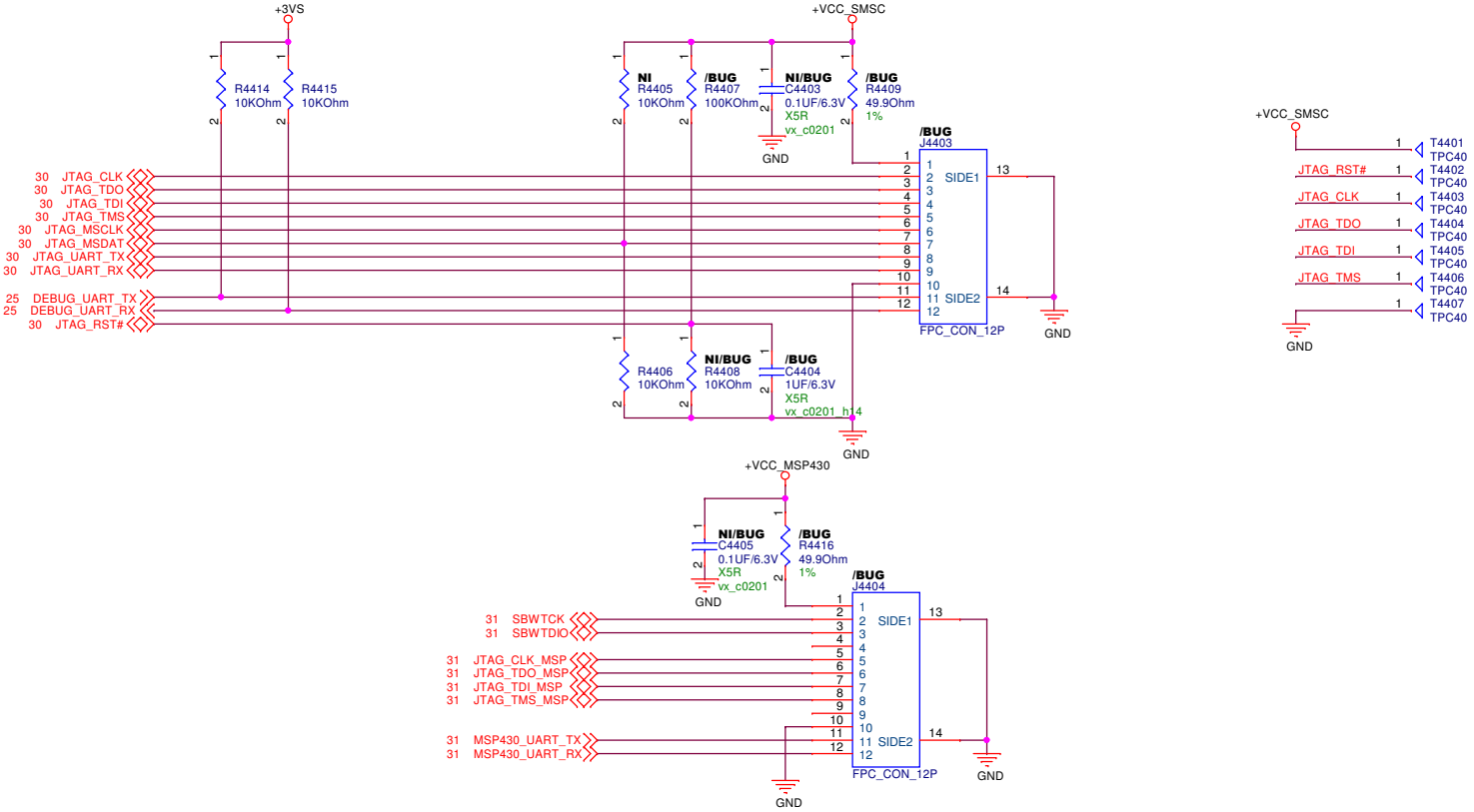
LPC Debug Port



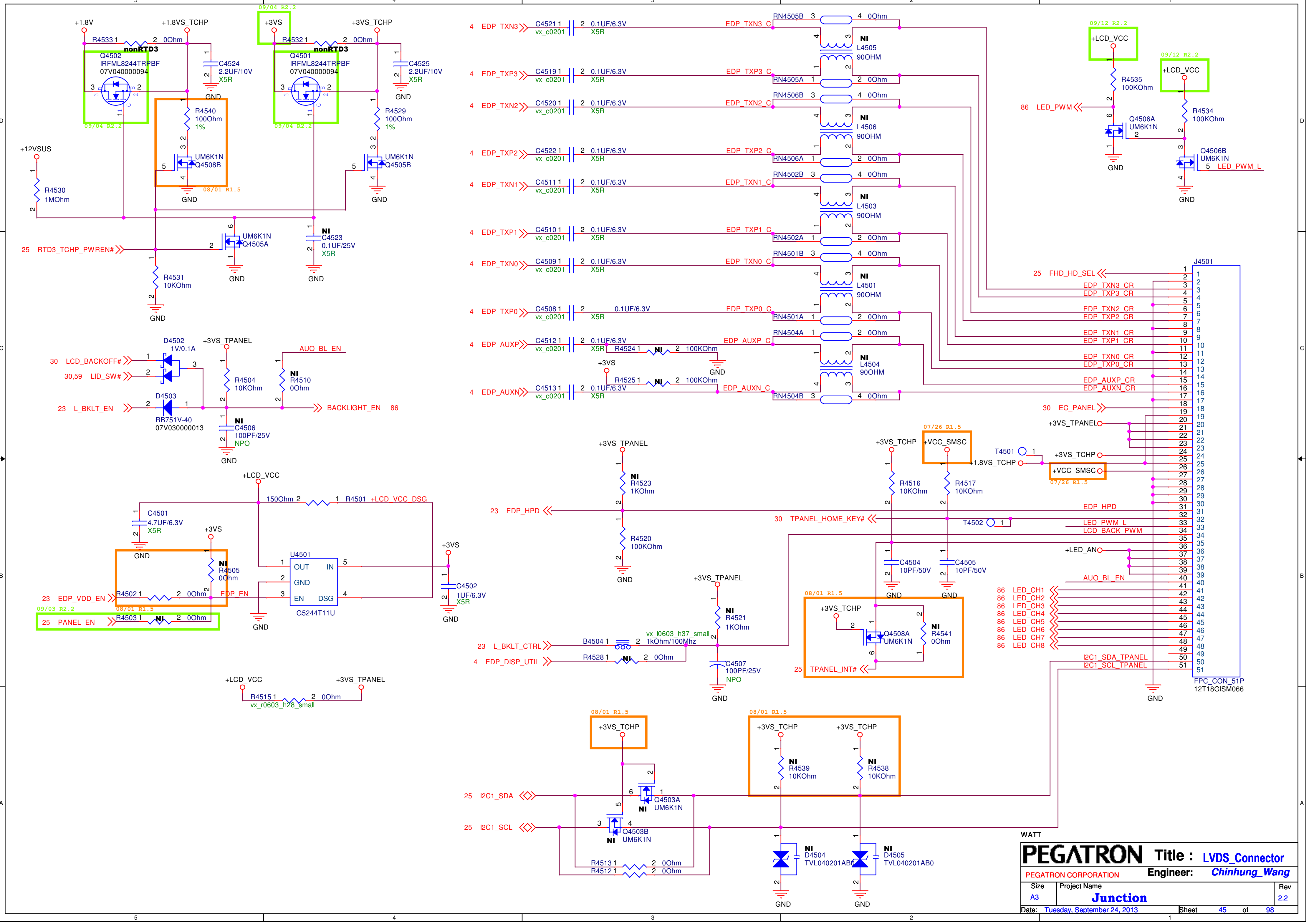
SPI Debug Port



JTAG Debug Port

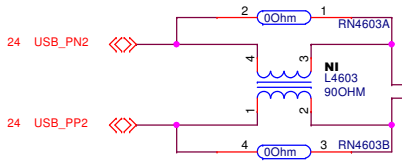


PEGATRON	Title : BUG_Debug	
PEGATRON CORPORATION	Engineer: Chinhung_Wang	
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 44 of 98	

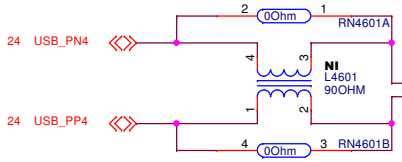


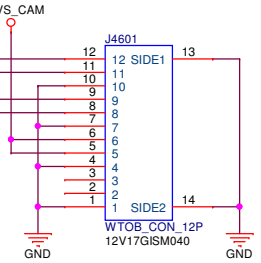
J4501
FPC_CON_51P
12T18GISM066
FHD_HD_SEL
EDP_TXN3 EDP_TXP3 EDP_TXN2 EDP_TXP2 EDP_TXN1 EDP_TXP1 EDP_TXN0 EDP_TXP0 EDP_AUXP EDP_AUXN
EDP_TXN3_CR EDP_TXP3_CR EDP_TXN2_CR EDP_TXP2_CR EDP_TXN1_CR EDP_TXP1_CR EDP_TXN0_CR EDP_TXP0_CR EDP_AUXP_CR EDP_AUXN_CR
L4505 L4506 L4503 L4501 L4504 90OHM
EC_PANEL
+3VS_TPANEL
+VCC_SMSC
+3VS_TCHP
EDP_HPD
TPANEL_HOME_KEY#
LED_PWM_L
LCD_BACK_PWM
+LED_AN
AUO_BL_EN
LED_CH1 LED_CH2 LED_CH3 LED_CH4 LED_CH5 LED_CH6 LED_CH7 LED_CH8
I2C1_SDA_TPANEL
I2C1_SCL_TPANEL
LED_PWM
RTD3_TCHP_PWREN#
LCD_BACKOFF#
LID_SW#
L_BKLT_EN
BACKLIGHT_EN
EDP_VDD_EN
PANEL_EN
+LCD_VCC_DSG
U4501
G5244T11U
L_BKLT_CTRL
EDP_DISP_UTIL
TPANEL_INT#
I2C1_SDA
I2C1_SCL
WATT
PEGATRON
PEGATRON CORPORATION
Title : LVDS_Connector
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
Sheet 45 of 98

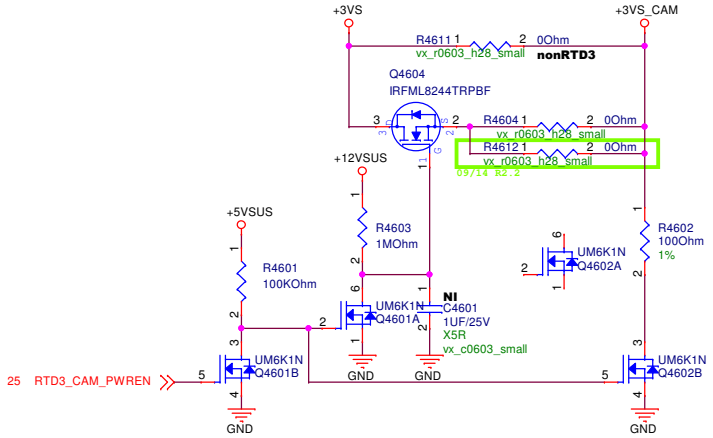
CAMERA_2M



CAMERA_8M



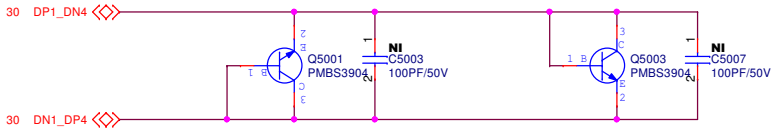


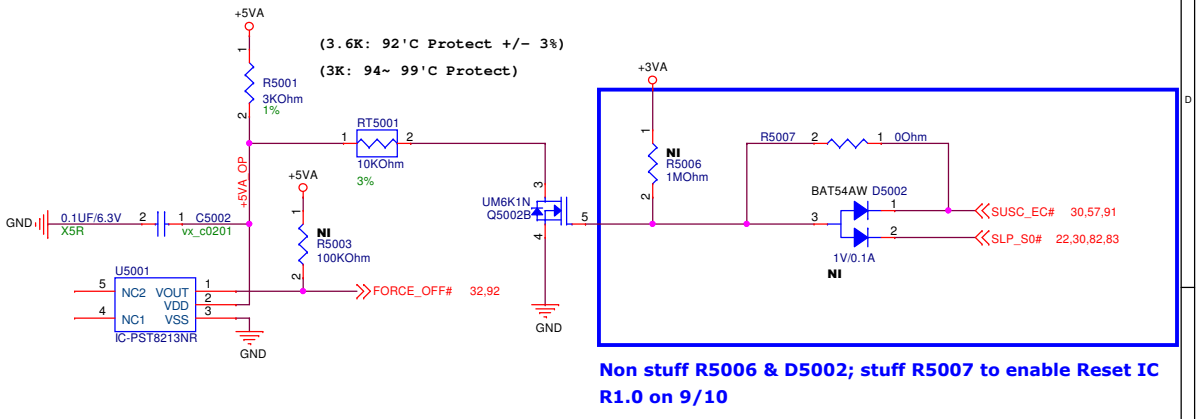


PEGATRON	Title : CAMERA / LED Flash Dri	
PEGATRON CORPORATION	Engineer: Chinhung_Wang	
Size: A3	Project Name: JCT	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 46 of 98	

DDR,VR Thermal Sensor

U5001 Close to DDR,U5003 Close to VR

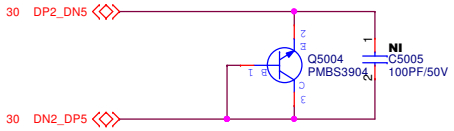




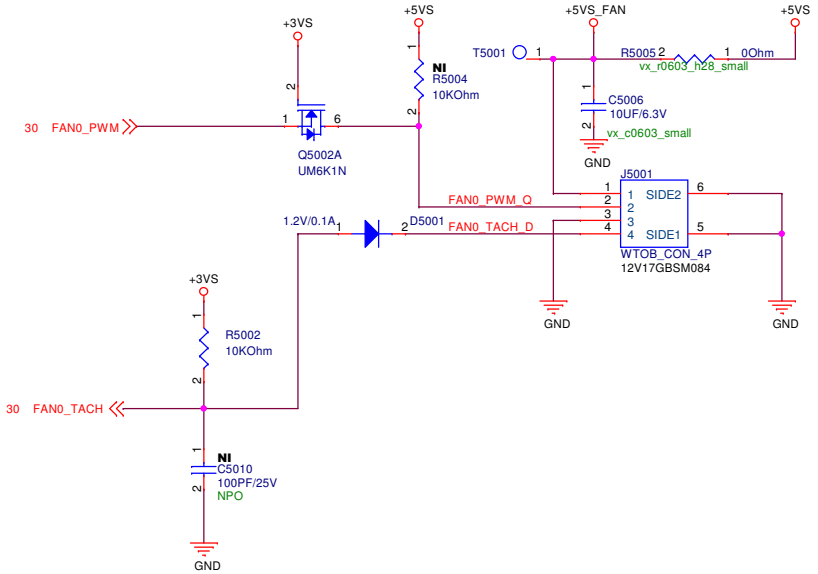
Non stuff R5006 & D5002; stuff R5007 to enable Reset IC
R1.0 on 9/10

FAN,BKLT Thermal Sensor

U5003 Close to LED Driver(U8901)



PWM FAN



PEGATRON

Title : THERMAL/ FAN

PEGATRON CORPORATION

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

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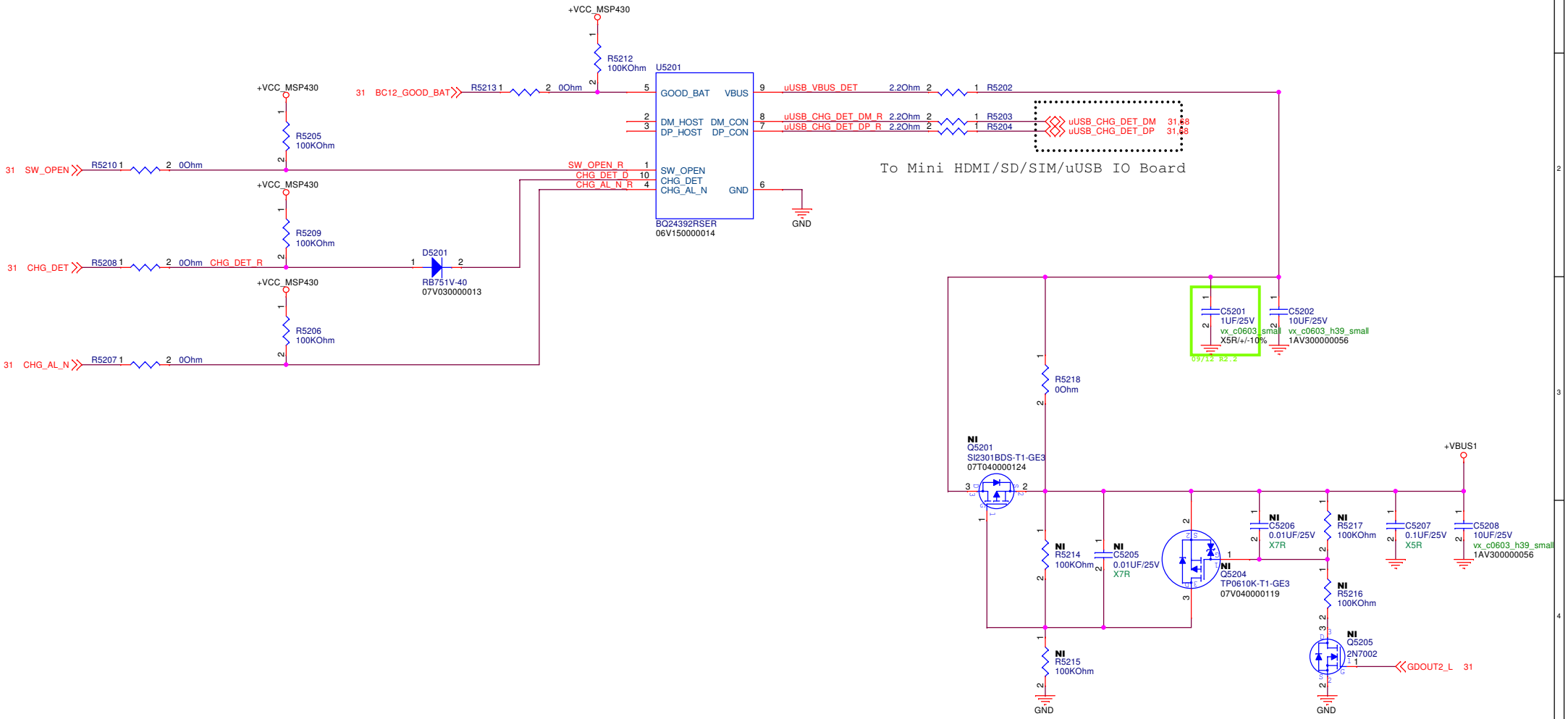


MidLand

PEGATRON

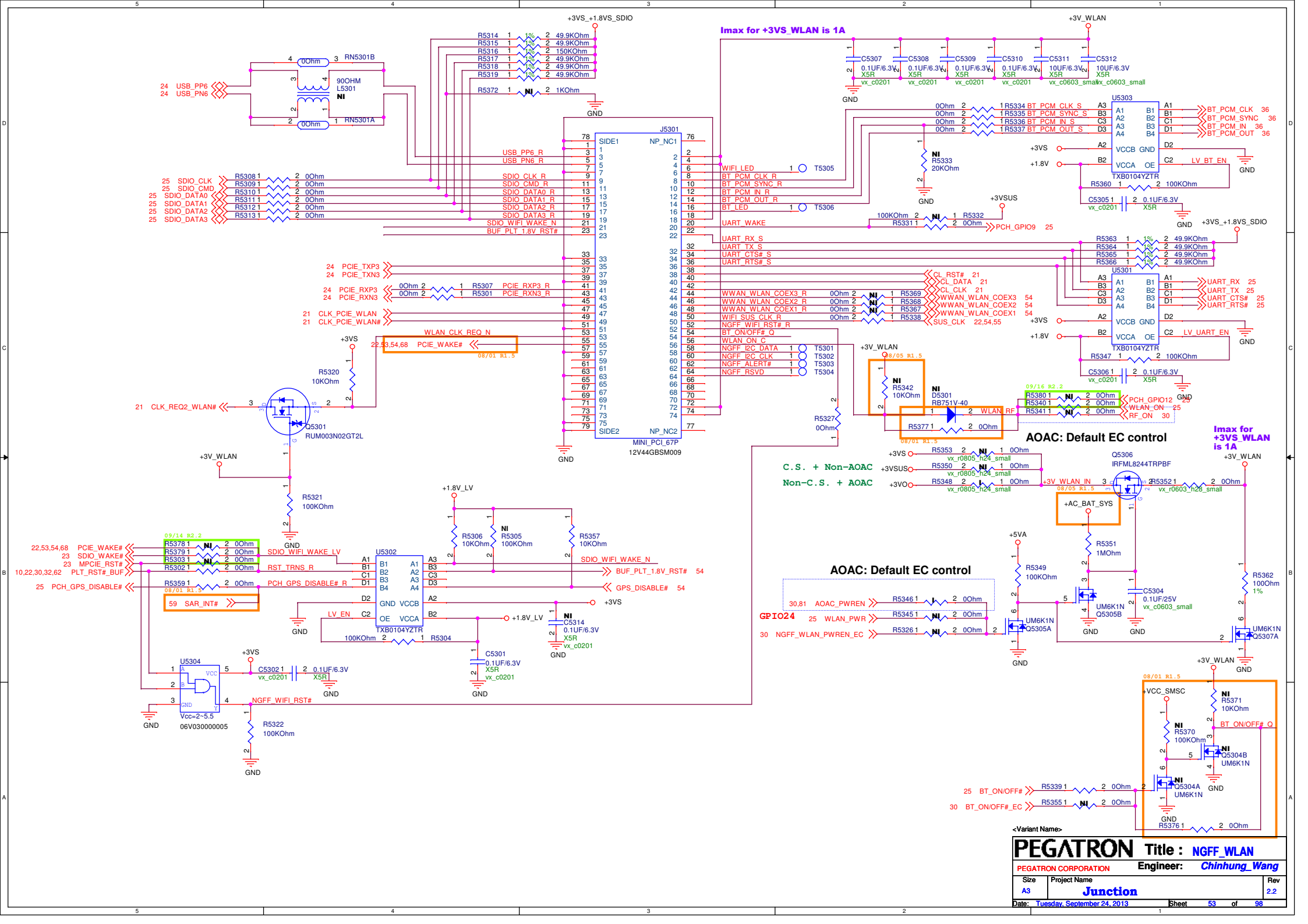
Title : uUSB charging detect

PEGATRON CORPORATION

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 52 of 98


+3VS_+1.8VS_SDIO
Imax for +3VS_WLAN is 1A
+3V_WLAN
RN5301B
RN5301A
L5301
90OHM
NI
J5301
SIDE1
SIDE2
NP_NC1
NP_NC2
MINI_PCI_67P
12V44GBSM009
GND
USB_PP6_R
USB_PN6_R
SDIO_CLK_R
SDIO_CMD_R
SDIO_DATA0_R
SDIO_DATA1_R
SDIO_DATA2_R
SDIO_DATA3_R
SDIO_WIFI_WAKE_N
BUF_PLT_1.8V_RST#
WIFI_LED
BT_PCM_CLK_R
BT_PCM_SYNC_R
BT_PCM_IN_R
BT_PCM_OUT_R
BT_LED
UART_WAKE
UART_RX_S
UART_TX_S
UART_CTS#_S
UART_RTS#_S
WWAN_WLAN_COEX3_R
WWAN_WLAN_COEX2_R
WWAN_WLAN_COEX1_R
WIFI_SUS_CLK_R
NGFF_WIFI_RST#_R
BT_ON/OFF#_Q
WLAN_ON_C
NGFF_I2C_DATA
NGFF_I2C_CLK
NGFF_ALERT#
NGFF_RSVD
T5305
T5306
T5301
T5302
T5303
T5304
PCIE_TXP3
PCIE_TXN3
PCIE_RXP3
PCIE_RXN3
PCIE_RXP3_R
PCIE_RXN3_R
CLK_PCIE_WLAN
CLK_PCIE_WLAN#
WLAN_CLK_REQ_N
PCIE_WAKE#
CLK_REQ2_WLAN#
Q5301
RUM003N02GT2L
U5303
TXB0104YZTR
BT_PCM_CLK_S
BT_PCM_SYNC_S
BT_PCM_IN_S
BT_PCM_OUT_S
BT_PCM_CLK
BT_PCM_SYNC
BT_PCM_IN
BT_PCM_OUT
LV_BT_EN
U5301
UART_RX
UART_TX
UART_CTS#
UART_RTS#
LV_UART_EN
CL_RST#
CL_DATA
CL_CLK
WWAN_WLAN_COEX3
WWAN_WLAN_COEX2
WWAN_WLAN_COEX1
SUS_CLK
PCH_GPIO9
+3VSUS
+3VS
+1.8V
+1.8V_LV
+5VA
+AC_BAT_SYS
C.S. + Non-AOAC
Non-C.S. + AOAC
AOAC: Default EC control
AOAC: Default EC control
Imax for +3VS_WLAN is 1A
D5301
RB751V-40
WLAN_RF
PCH_GPIO12
WLAN_ON
RF_ON
Q5306
IRFML8244TRPBF
+3V_WLAN_IN
UM6K1N
Q5305A
Q5305B
Q5307A
Q5304A
Q5304B
U5304
Vcc=2~5.5
06V030000005
U5302
TXB0104YZTR
PCH_GPS_DISABLE#
PCH_GPS_DISABLE#_R
RST_TRNS_R
SDIO_WIFI_WAKE_LV
SDIO_WIFI_WAKE_N
BUF_PLT_1.8V_RST#
GPS_DISABLE#
SAR_INT#
NGFF_WIFI_RST#
AOAC_PWREN
WLAN_PWR
NGFF_WLAN_PWREN_EC
GPIO24
BT_ON/OFF#
BT_ON/OFF#_EC
+VCC_SMSC
<Variant Name>
PEGATRON
Title : NGFF_WLAN
PEGATRON CORPORATION
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
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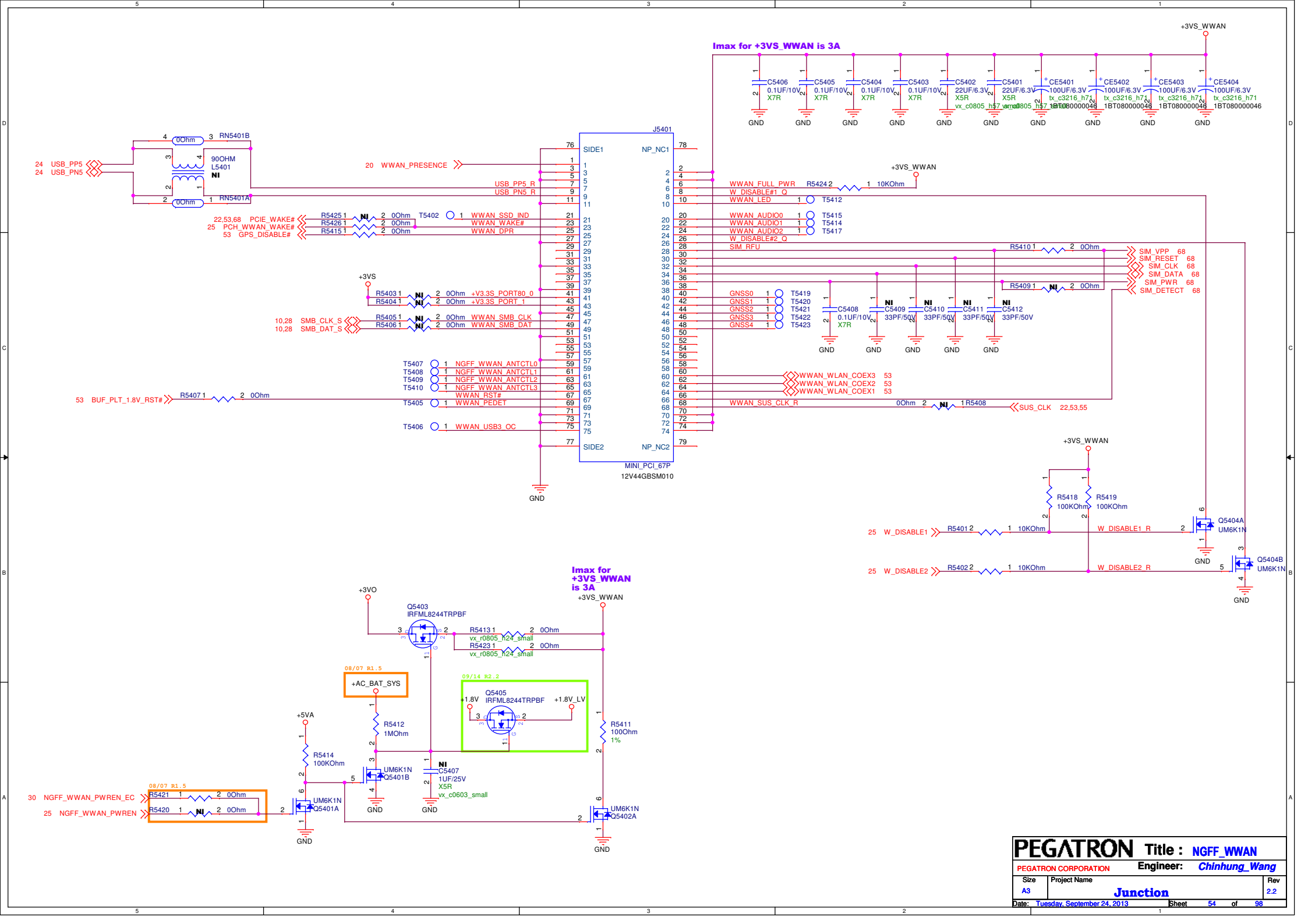
Imax for +3VS_WWAN is 3A
+3VS_WWAN
J5401
MINI_PCI_67P
12V44GBSM010
SIDE1
SIDE2
NP_NC1
NP_NC2
RN5401B
RN5401A
90OHM
L5401
USB_PP5
USB_PN5
USB_PP5_R
USB_PN5_R
WWAN_PRESENCE
PCIE_WAKE#
PCH_WWAN_WAKE#
GPS_DISABLE#
WWAN_SSD_IND
WWAN_WAKE#
WWAN_DPR
+3VS
SMB_CLK_S
SMB_DAT_S
WWAN_SMB_CLK
WWAN_SMB_DAT
+V3.3S_PORT80_0
+V3.3S_PORT_1
NGFF_WWAN_ANTCTL0
NGFF_WWAN_ANTCTL1
NGFF_WWAN_ANTCTL2
NGFF_WWAN_ANTCTL3
WWAN_RST#
WWAN_PEDET
WWAN_USB3_OC
BUF_PLT_1.8V_RST#
WWAN_FULL_PWR
W_DISABLE#1_Q
WWAN_LED
WWAN_AUDIO0
WWAN_AUDIO1
WWAN_AUDIO2
W_DISABLE#2_Q
SIM_RFU
GNSS0
GNSS1
GNSS2
GNSS3
GNSS4
WWAN_WLAN_COEX3
WWAN_WLAN_COEX2
WWAN_WLAN_COEX1
WWAN_SUS_CLK_R
SUS_CLK
SIM_VPP
SIM_RESET
SIM_CLK
SIM_DATA
SIM_PWR
SIM_DETECT
W_DISABLE1
W_DISABLE2
W_DISABLE1_R
W_DISABLE2_R
Q5404A
Q5404B
UM6K1N
Imax for +3VS_WWAN is 3A
+3VO
Q5403
IRFML8244TRPBF
+AC_BAT_SYS
+5VA
Q5405
+1.8V
+1.8V_LV
NGFF_WWAN_PWREN_EC
NGFF_WWAN_PWREN
Q5401A
Q5401B
Q5402A
GND
PEGATRON
Title : NGFF_WWAN
PEGATRON CORPORATION
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
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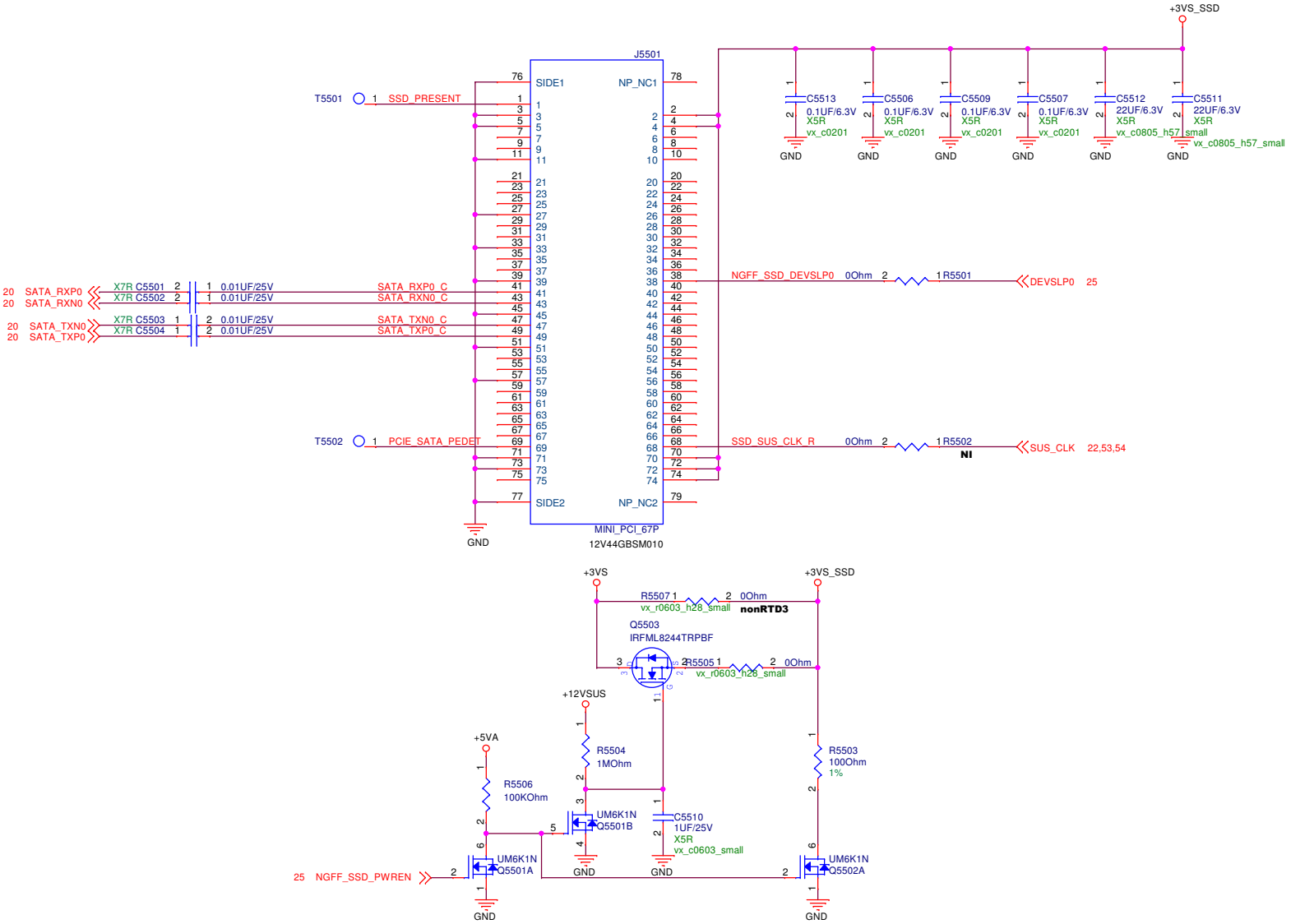
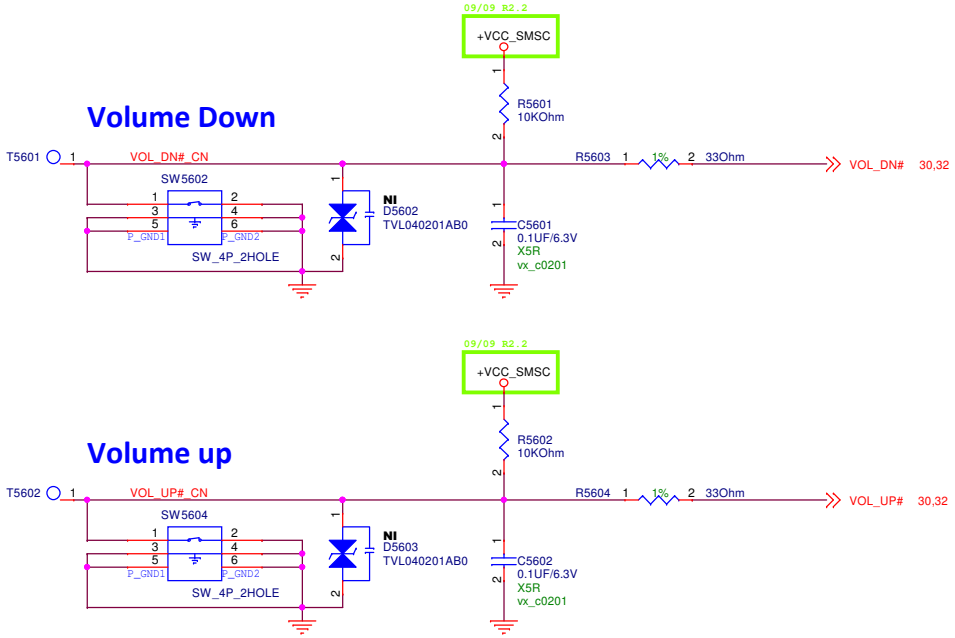


PEGATRON	Title : NGFF_SSD	
PEGATRON CORPORATION	Engineer: Chinhung_Wang	
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 55 of 98	



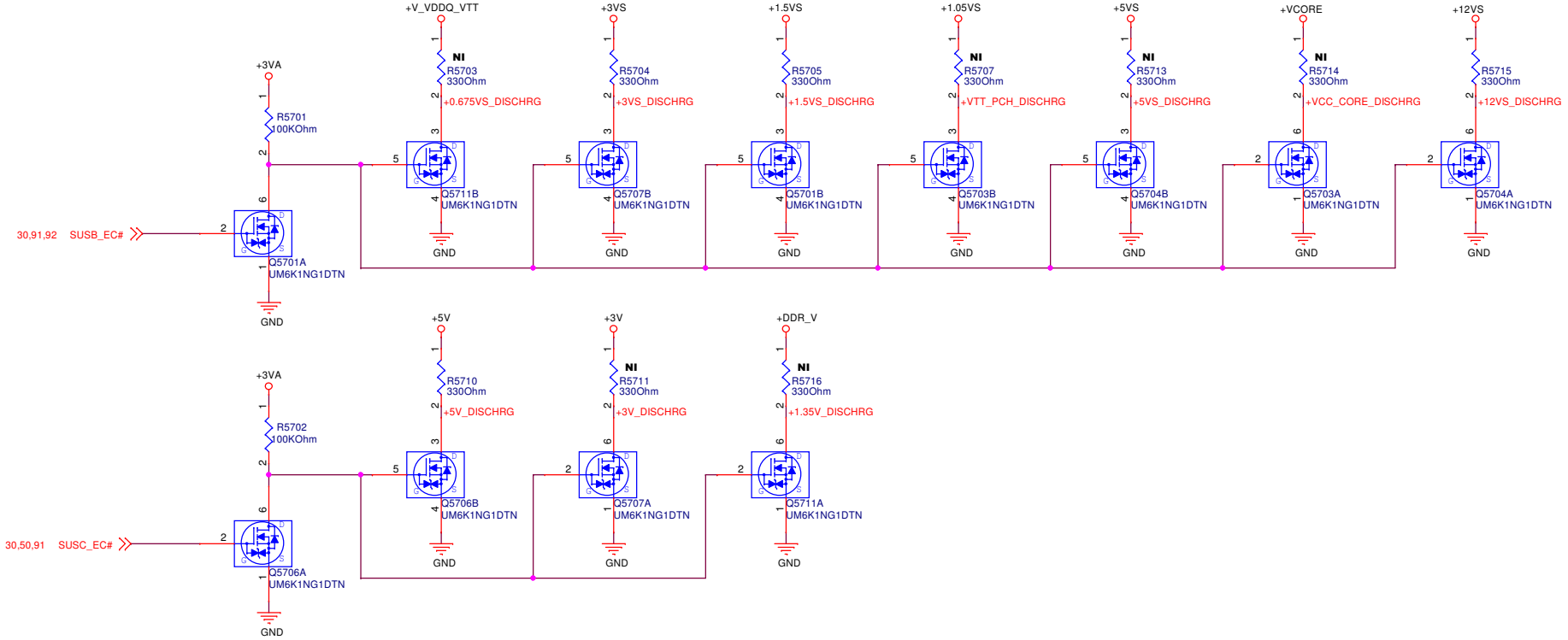
MidLand

PEGATRON Title : Volume Switch

PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 56 of 98



PEGATRON Title : DSG_Discharge

PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 57 of 98

Sensor Hub

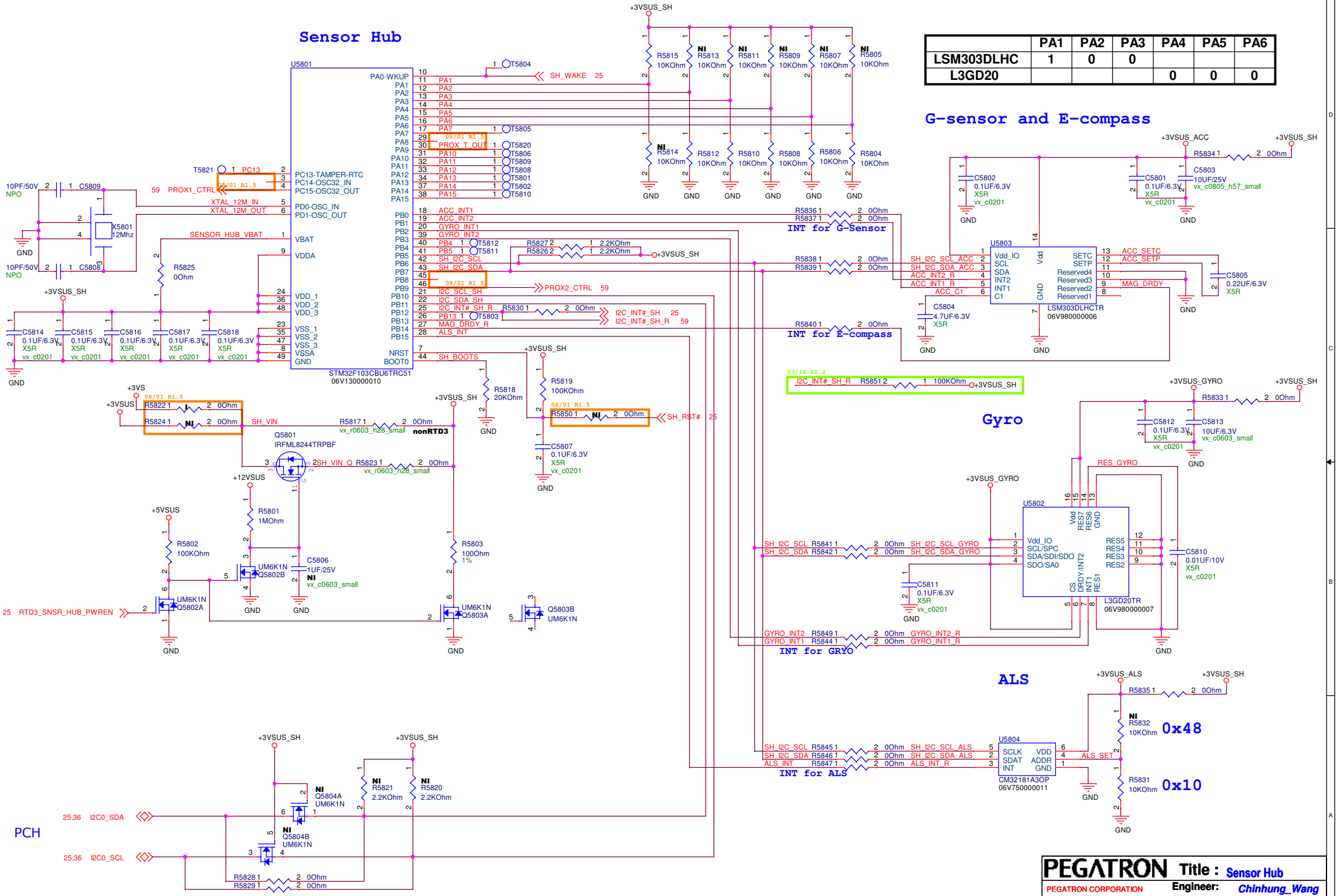
	PA1	PA2	PA3	PA4	PA5	PA6
LSM303DLHC	1	0	0			
L3GD20				0	0	0

G-sensor and E-compass

Gyro

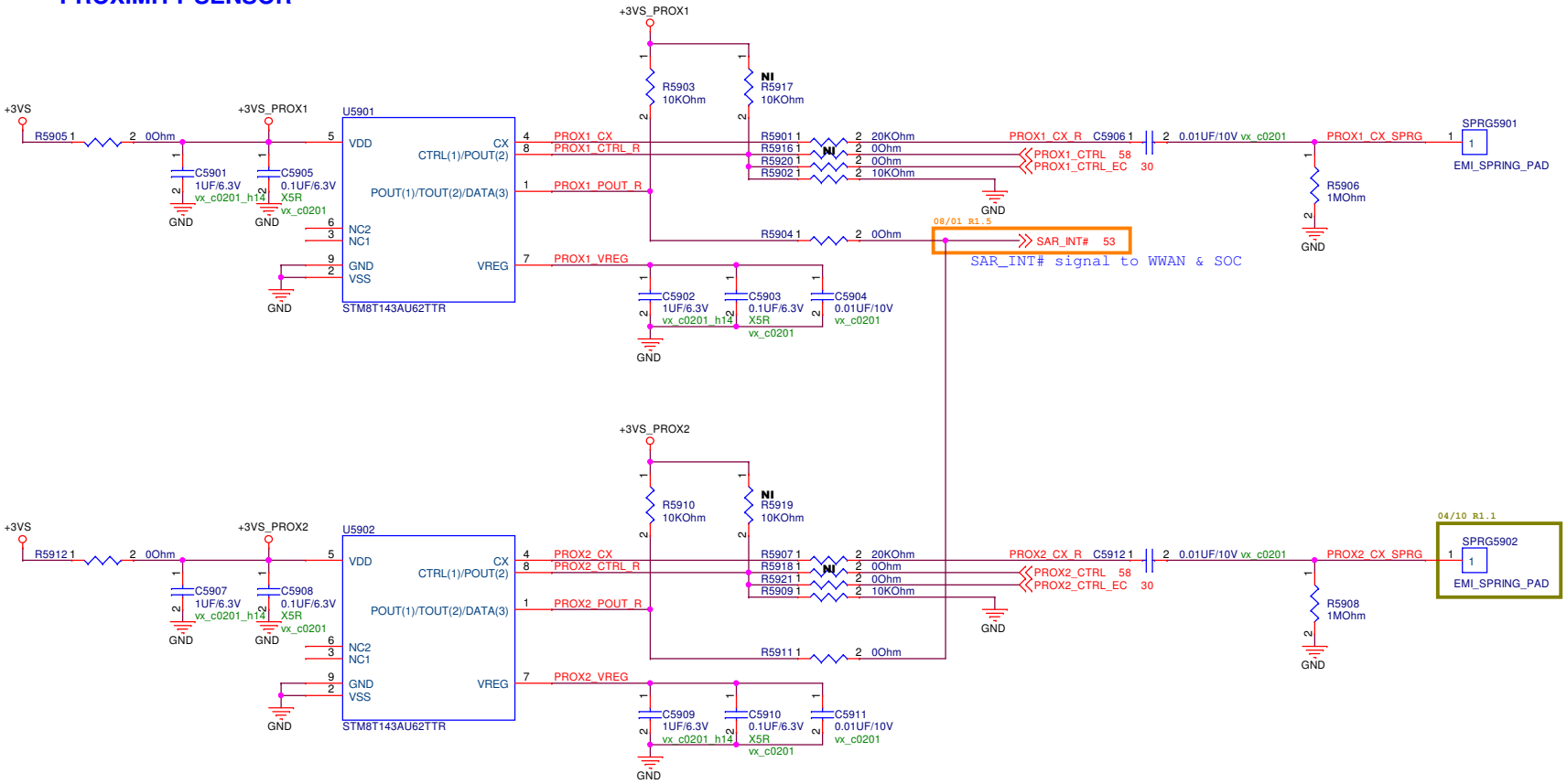
ALS

PCH

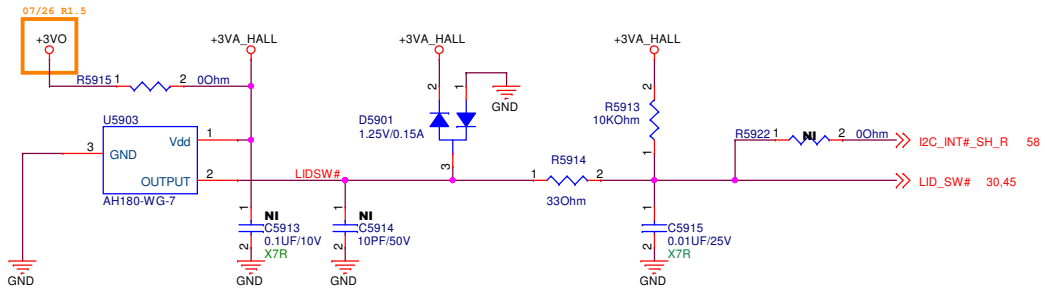


PEGATRON	Title : Sensor Hub
PEGATRON CORPORATION	Engineer: Chinhung_Wang
Size: A3	Project Name: Junction
Rev: 2.2	
Date: Tuesday, September 24, 2013	Sheet 58 of 98

PROXIMITY SENSOR

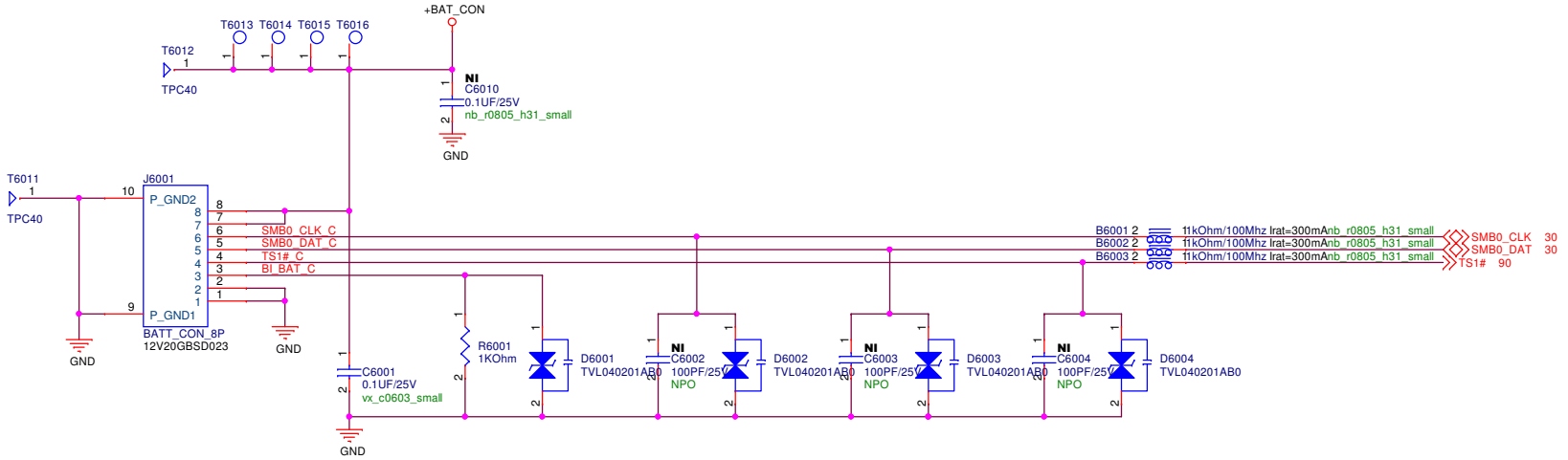


LID Switch

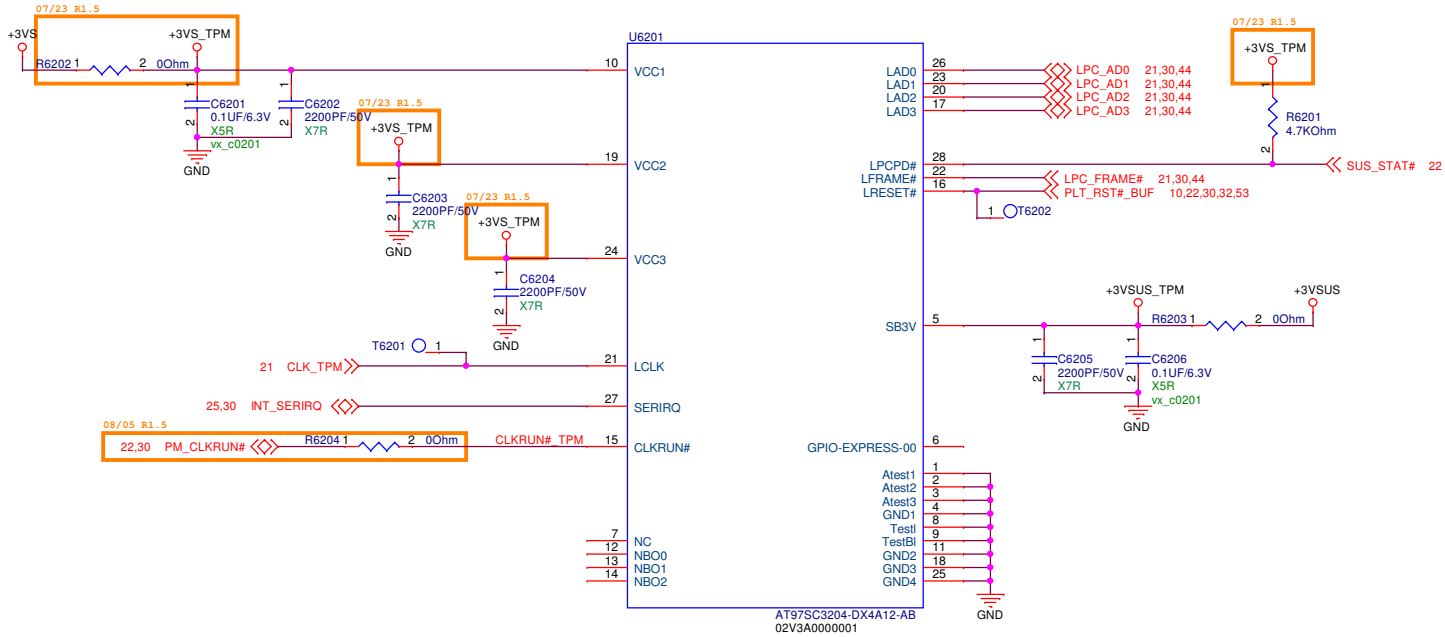


PEGATRON	Title : Proximity Sensor	
PEGATRON CORPORATION	Engineer: Chinhung_Wang	
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 59 of 98	

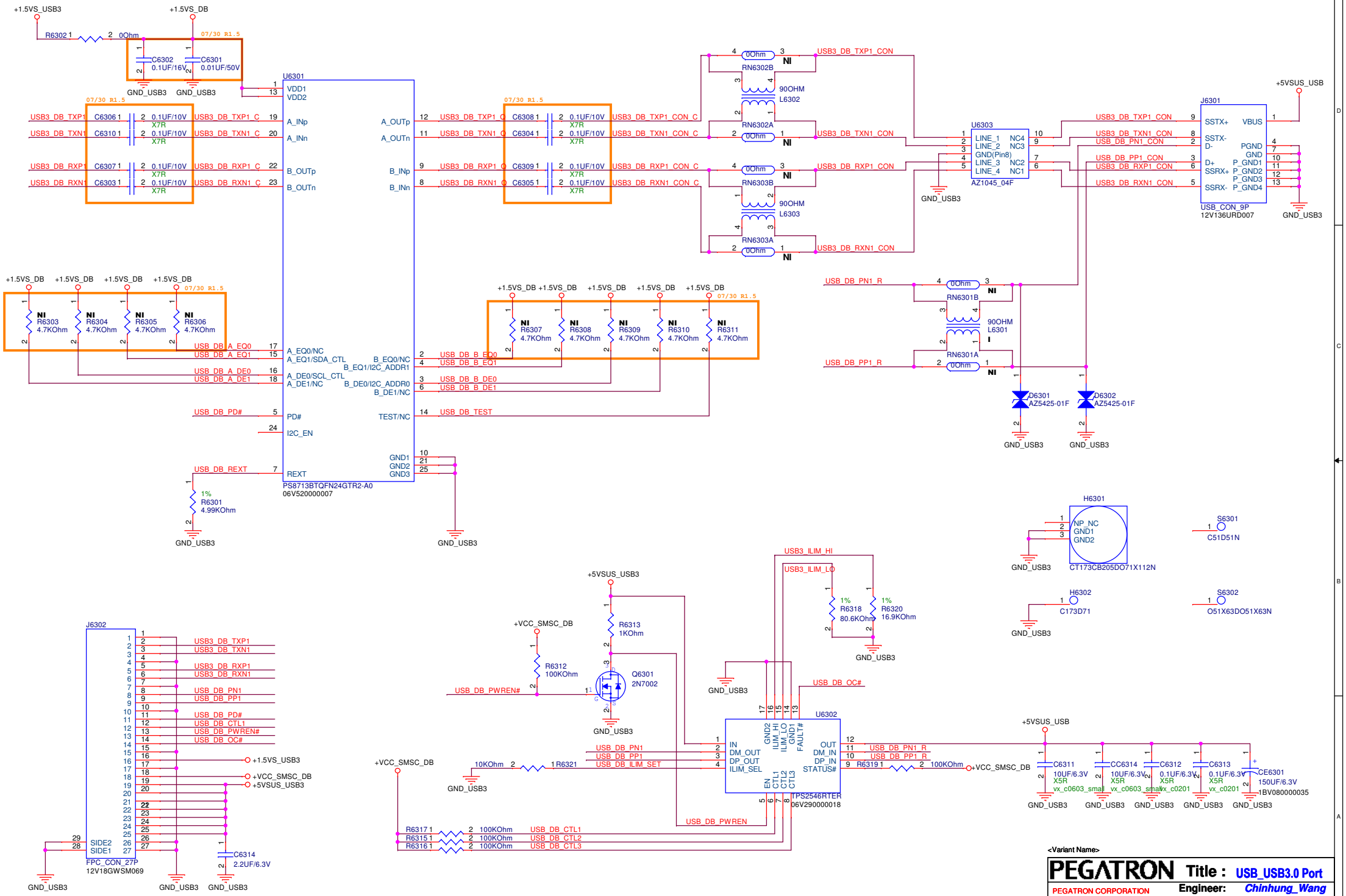
Battery Connector



PEGATRON	Title :	DC_DC/BAT CONN
PEGATRON CORPORATION	Engineer:	Chinhung_Wang
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 60 of 98	



PEGATRON	Title : TPM	
PEGATRON CORPORATION	Engineer: Chinhung_Wang	
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 62 of 98	



<Variant Name>

PEGATRON

Title : USB_USB3.0 Port

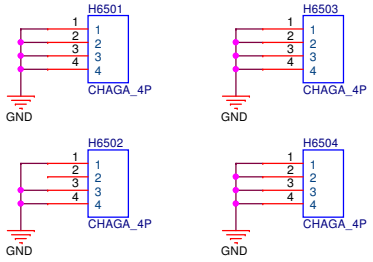
PEGATRON CORPORATION

Engineer: Chinhung_Wang

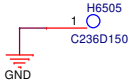
Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 63 of 98

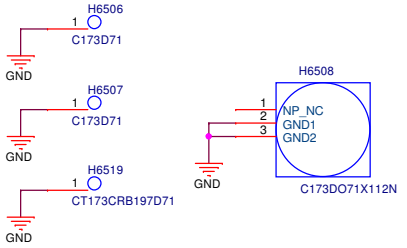
Chagall Support Matel



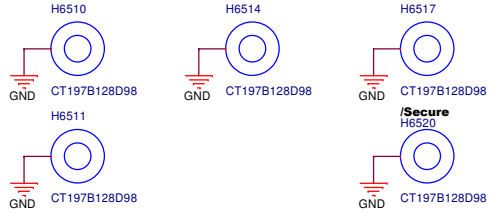
Scrow hole 3.8mm X 6.0mm



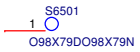
Scrow hole 1.8mm X 4.4mm



NUT H=2.3mm D=4 M1.6

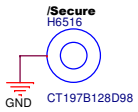


Tooling Hole 2.0mm*2.5mm

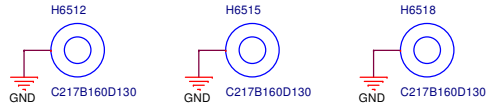


Tooling Hole 2.0mm

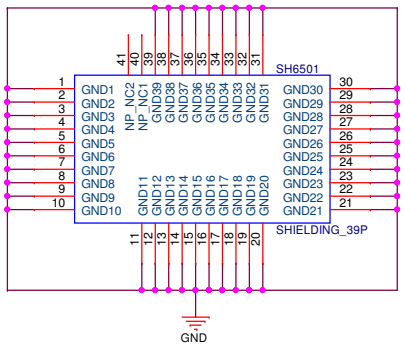
NUT H=6.95mm D=4 M1.6

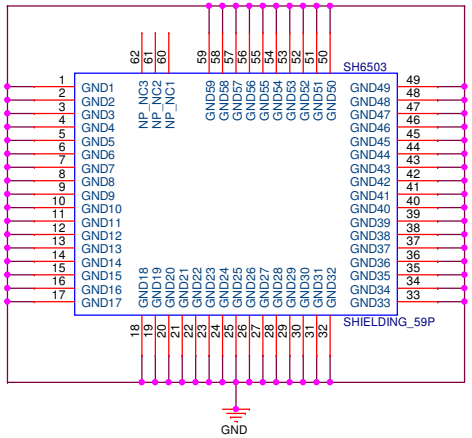


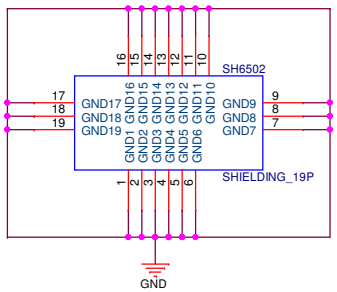
NUT



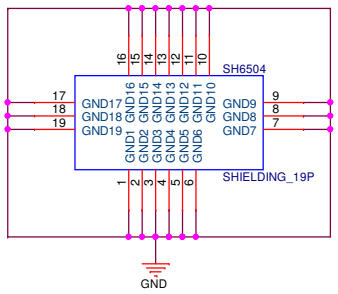
BOTTOM SHIELDING

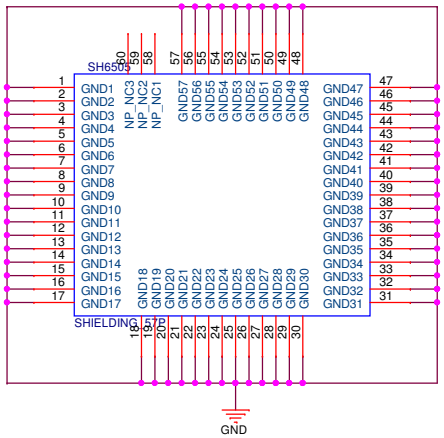


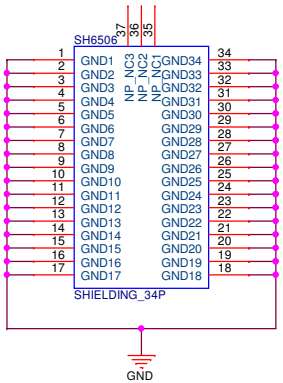


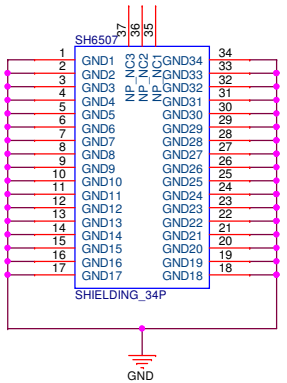


TOP SHIELDING









<Variant Name>

PEGATRON

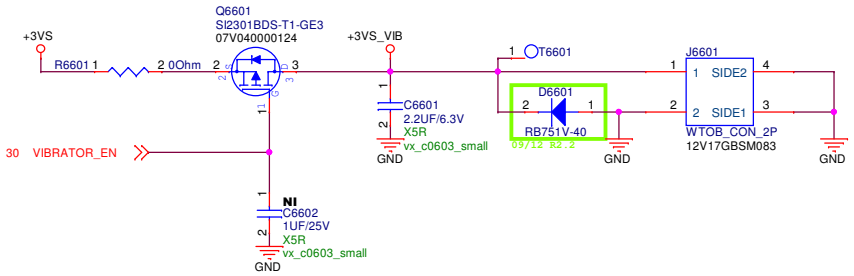
Title : ME_CONN,Skew Hole

PEGATRON CORPORATION

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 65 of 98



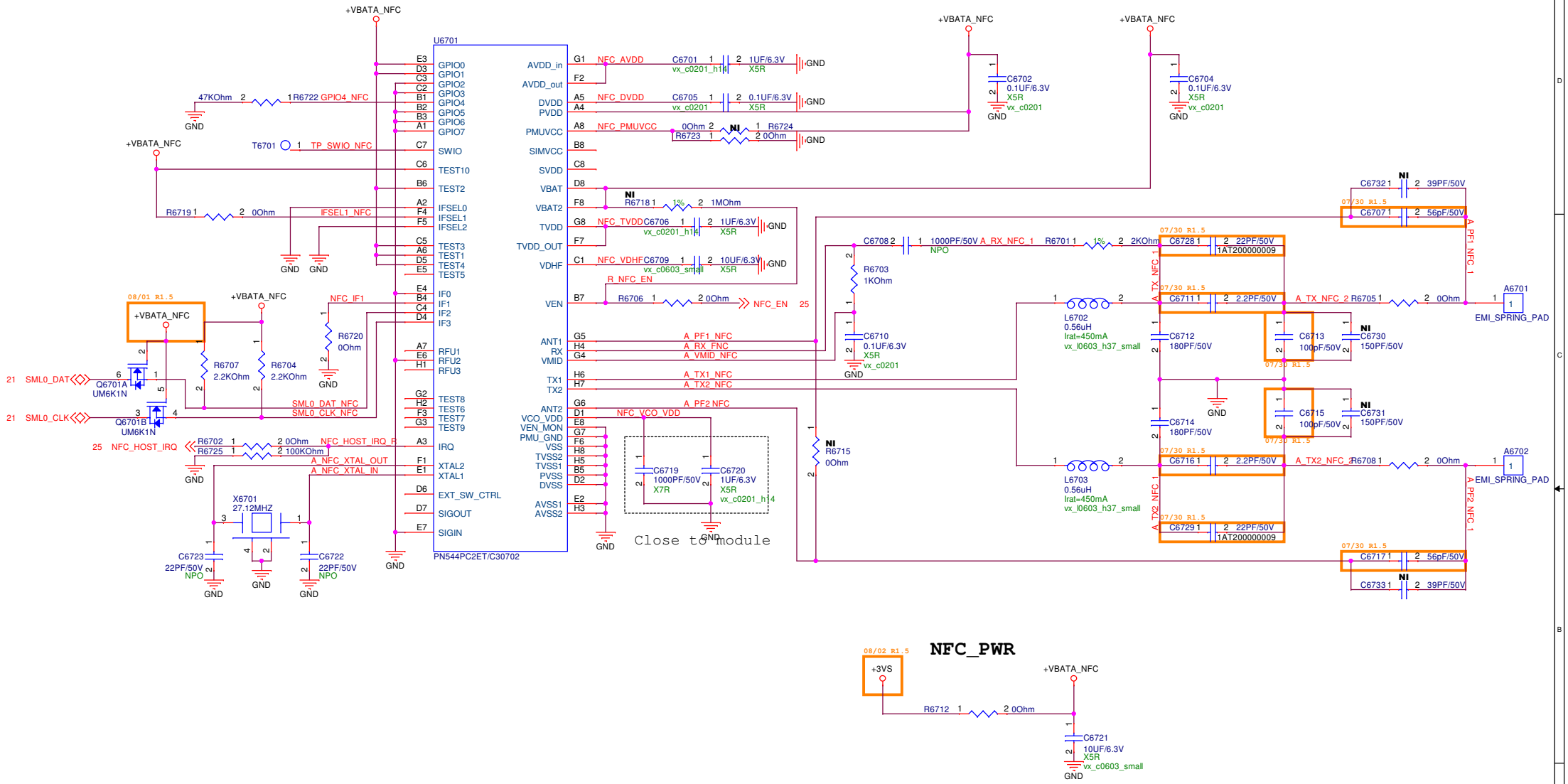
<Variant Name>

PEGATRON Title : VIBRATOR

PEGATRON CORPORATION Engineer: Chinhung_Wang

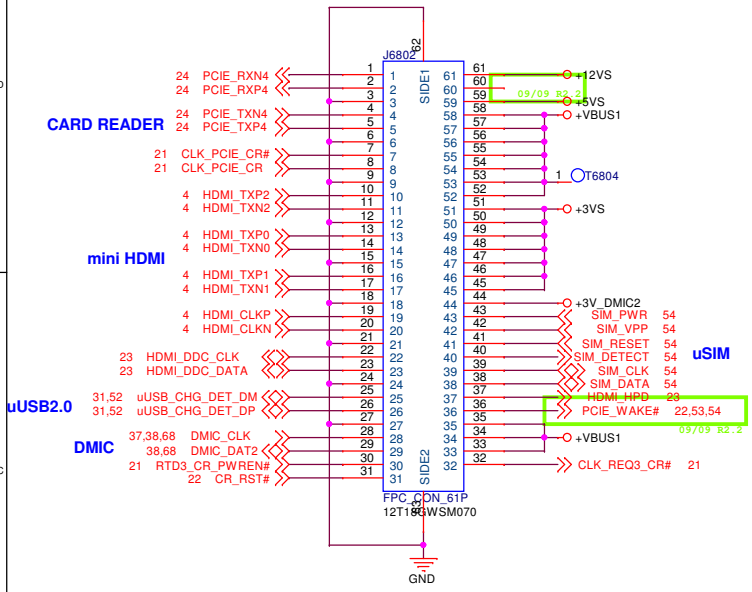
Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 66 of 98

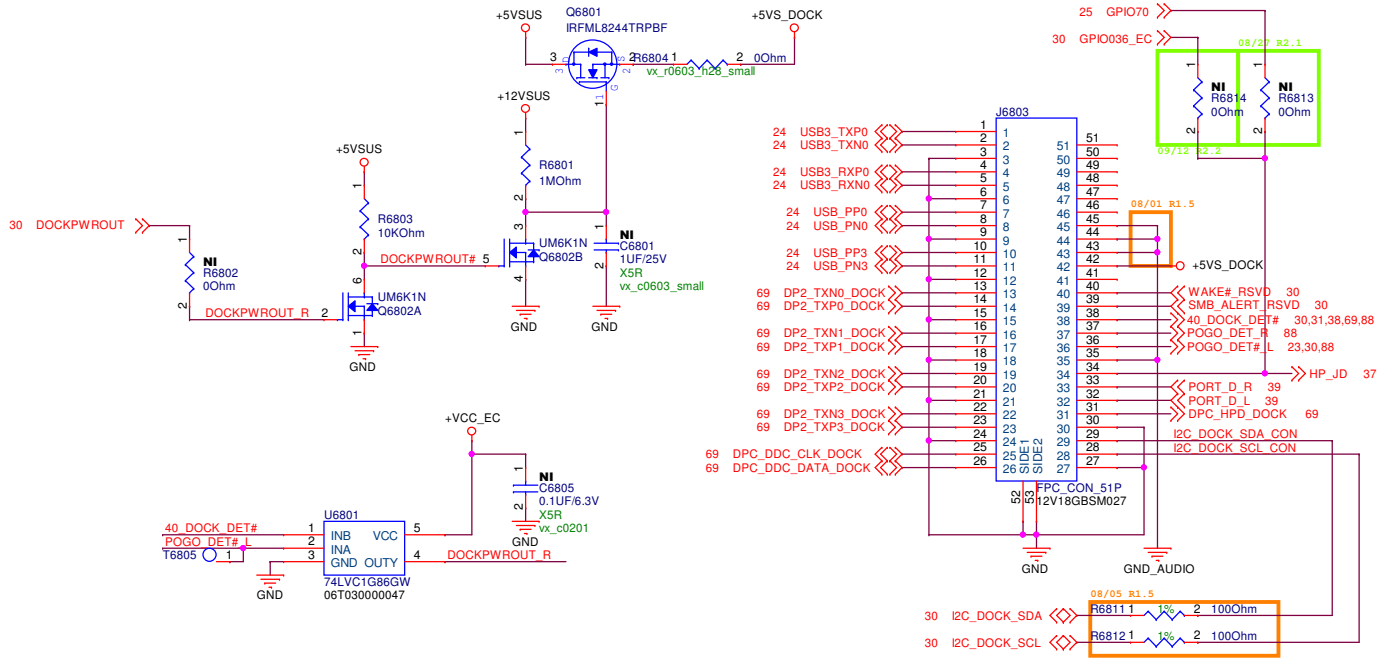


PEGATRON	Title : NFC		
PEGATRON CORPORATION	Engineer: Chinhung_Wang		
Size: A3	Project Name: Junction		Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 67 of 98		

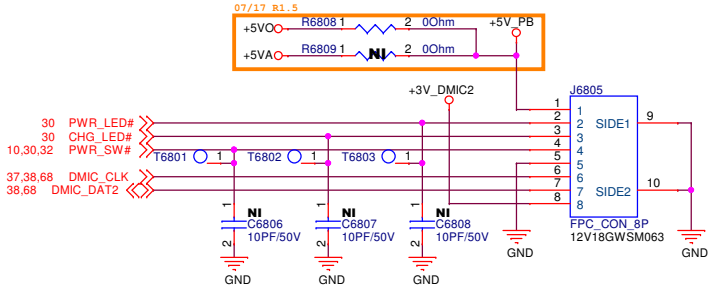
IO Board Conn (uSIM / Card reader / mini HDMI / uUSB2.0 / DMIC)



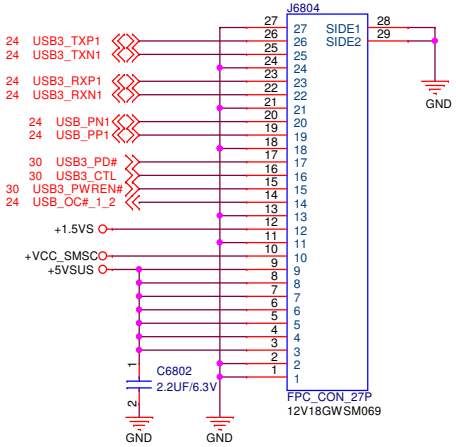
IO Board Conn (DOCK / POGO signal)



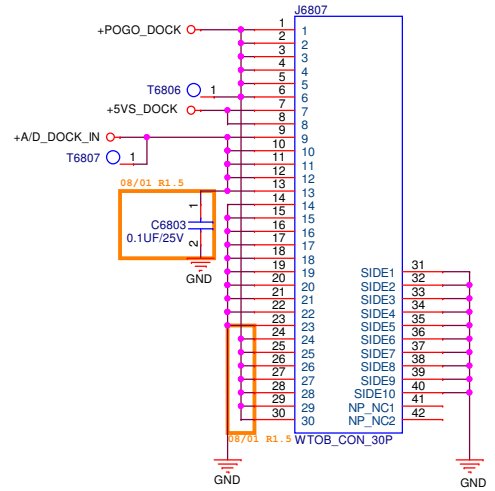
POWER BOTTOM



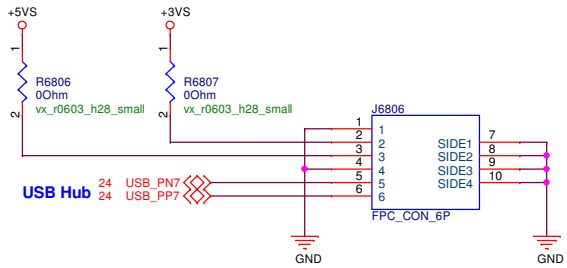
IO Board Conn (USB3.0)



IO Board Conn (DOCK / POGO power)



Smart Card/Finger Print Conn



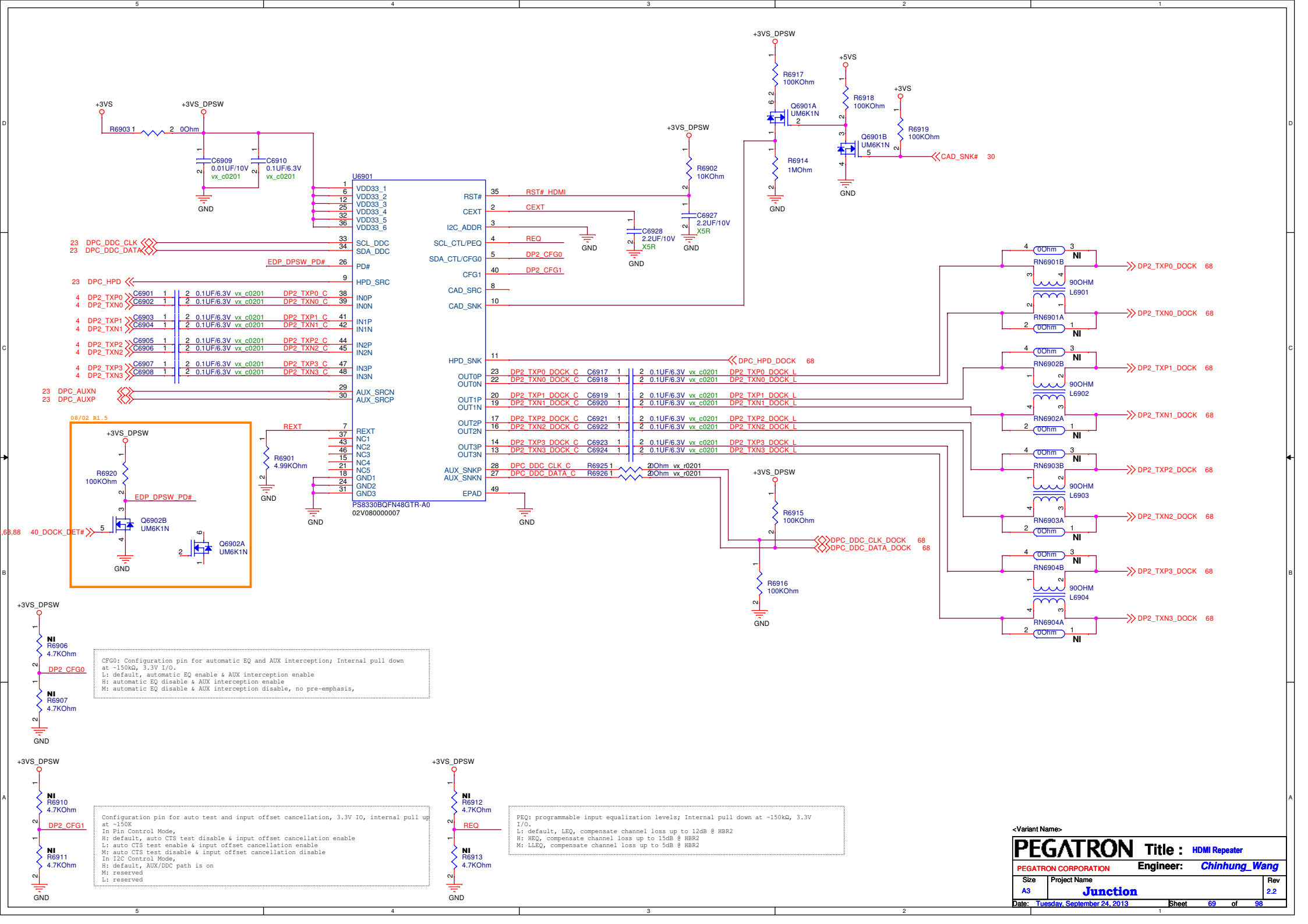
MO

PEGATRON Title : MB_to_Daughter_BD_CONN

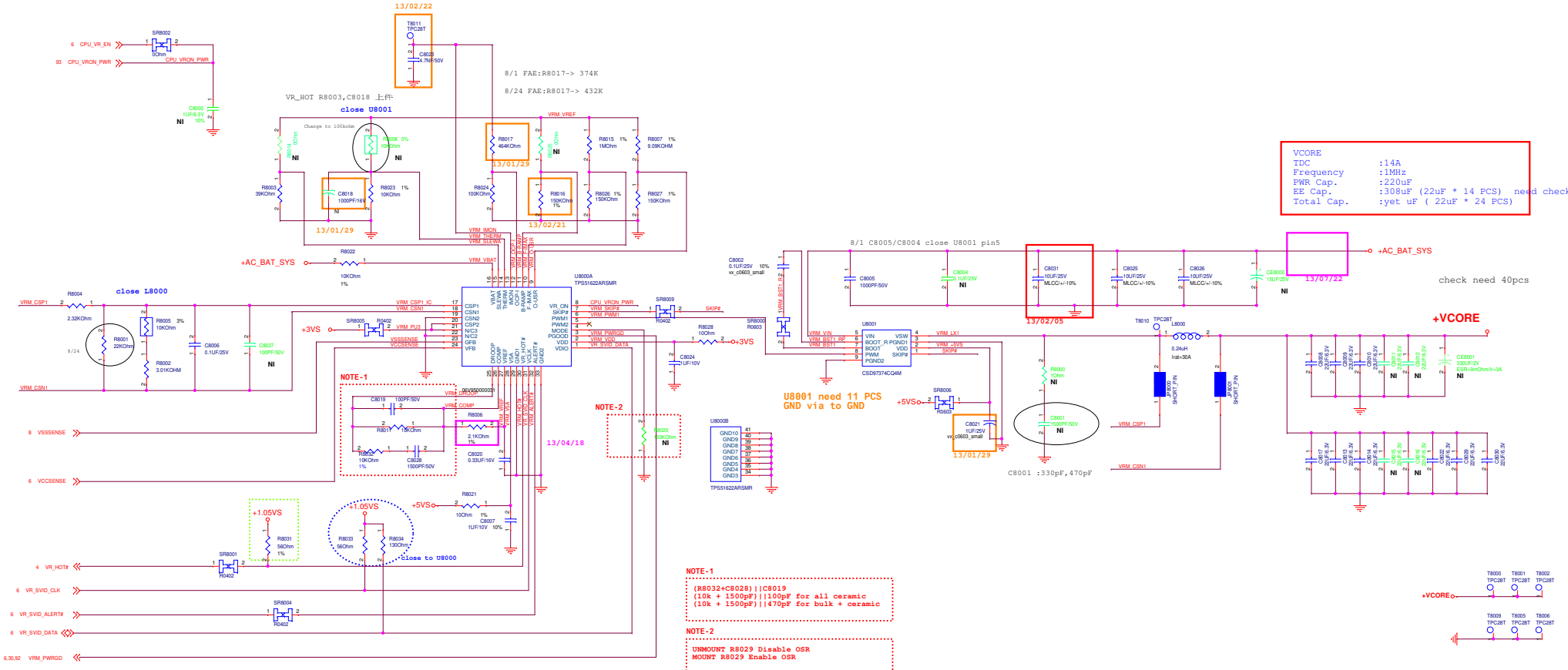
PEGATRON CORPORATION Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 68 of 98


U6901
PS8330BQFN48GTR-A0
02V080000007
08/02 R1.5
CFG0: Configuration pin for automatic EQ and AUX interception; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, automatic EQ enable & AUX interception enable
H: automatic EQ disable & AUX interception enable
M: automatic EQ disable & AUX interception disable, no pre-emphasis,
Configuration pin for auto test and input offset cancellation, 3.3V IO, internal pull up at ~150K
In Pin Control Mode,
H: default, auto CTS test disable & input offset cancellation enable
L: auto CTS test enable & input offset cancellation enable
M: auto CTS test disable & input offset cancellation disable
In I2C Control Mode,
H: default, AUX/DDC path is on
M: reserved
L: reserved
PEQ: programmable input equalization levels; Internal pull down at ~150kΩ, 3.3V I/O.
L: default, LEQ, compensate channel loss up to 12dB @ HBR2
H: HEQ, compensate channel loss up to 15dB @ HBR2
M: LLEQ, compensate channel loss up to 5dB @ HBR2
<Variant Name>
PEGATRON
Title : HDMI Repeater
PEGATRON CORPORATION
Engineer: Chinhung_Wang
Size A3
Project Name Junction
Rev 2.2
Date: Tuesday, September 24, 2013
Sheet 69 of 98

Shark bay ULV



<variant_name>

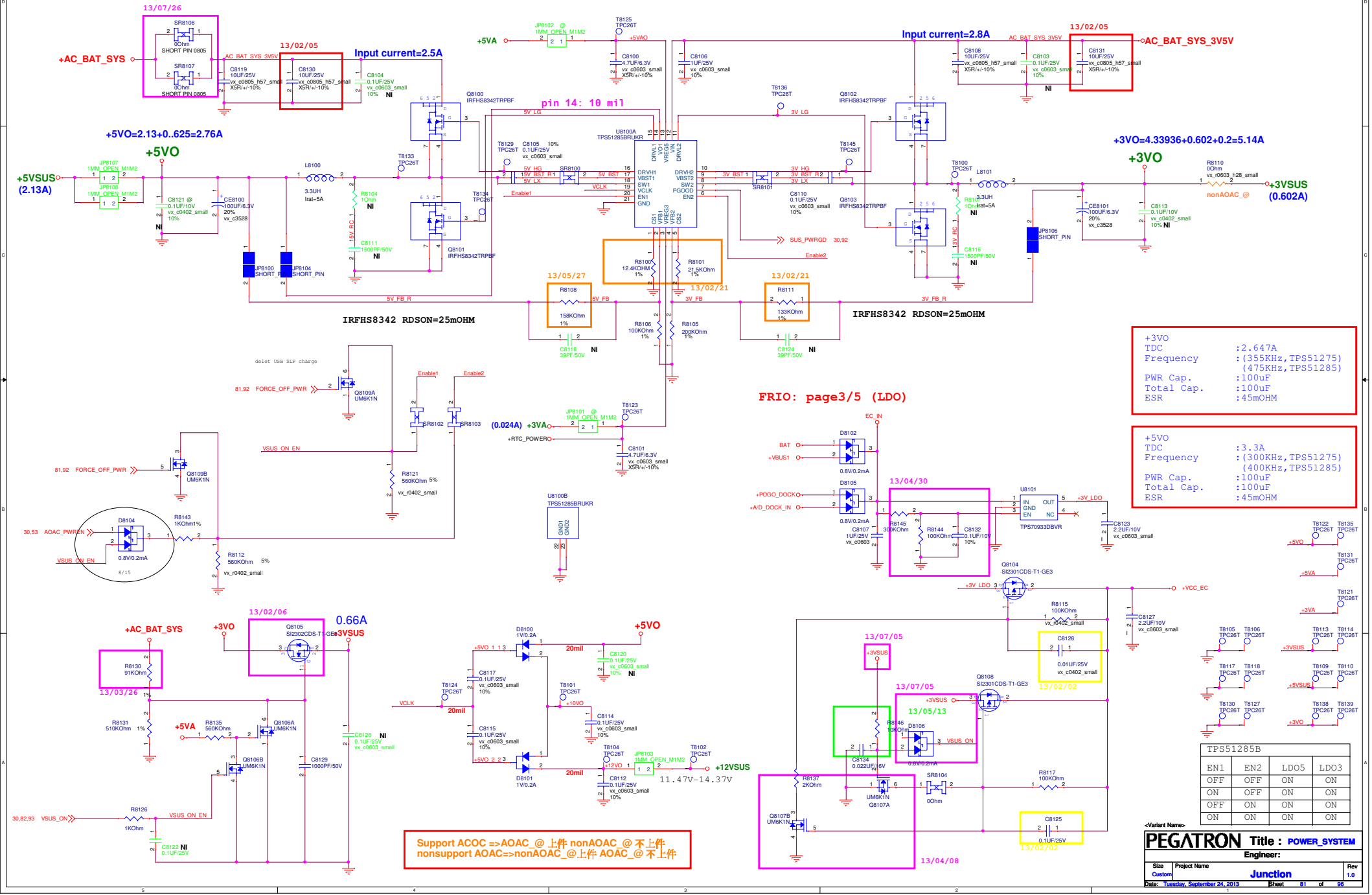
PEGATRON Title : POWER_VCORE

Engineer:

Size	Project Name	Rev
Custom	Junction	1.0

Date: Tuesday, September 24, 2013 Sheet 80 of 96

+5VO & +3VO POWER SUPPLY



+3VO	
TDC	:2.647A
Frequency	:(355KHz,TPS51275) (475KHz,TPS51285)
PWR Cap.	:100uF
Total Cap.	:100uF
ESR	:45mOHM

+5VO	
TDC	:3.3A
Frequency	:(300KHz,TPS51275) (400KHz,TPS51285)
PWR Cap.	:100uF
Total Cap.	:100uF
ESR	:45mOHM

TPS51285B			
EN1	EN2	LDO5	LDO3
OFF	OFF	ON	ON
ON	OFF	ON	ON
OFF	ON	ON	ON
ON	ON	ON	ON

<Variant Name>

PEGATRON Title : POWER_SYSTEM

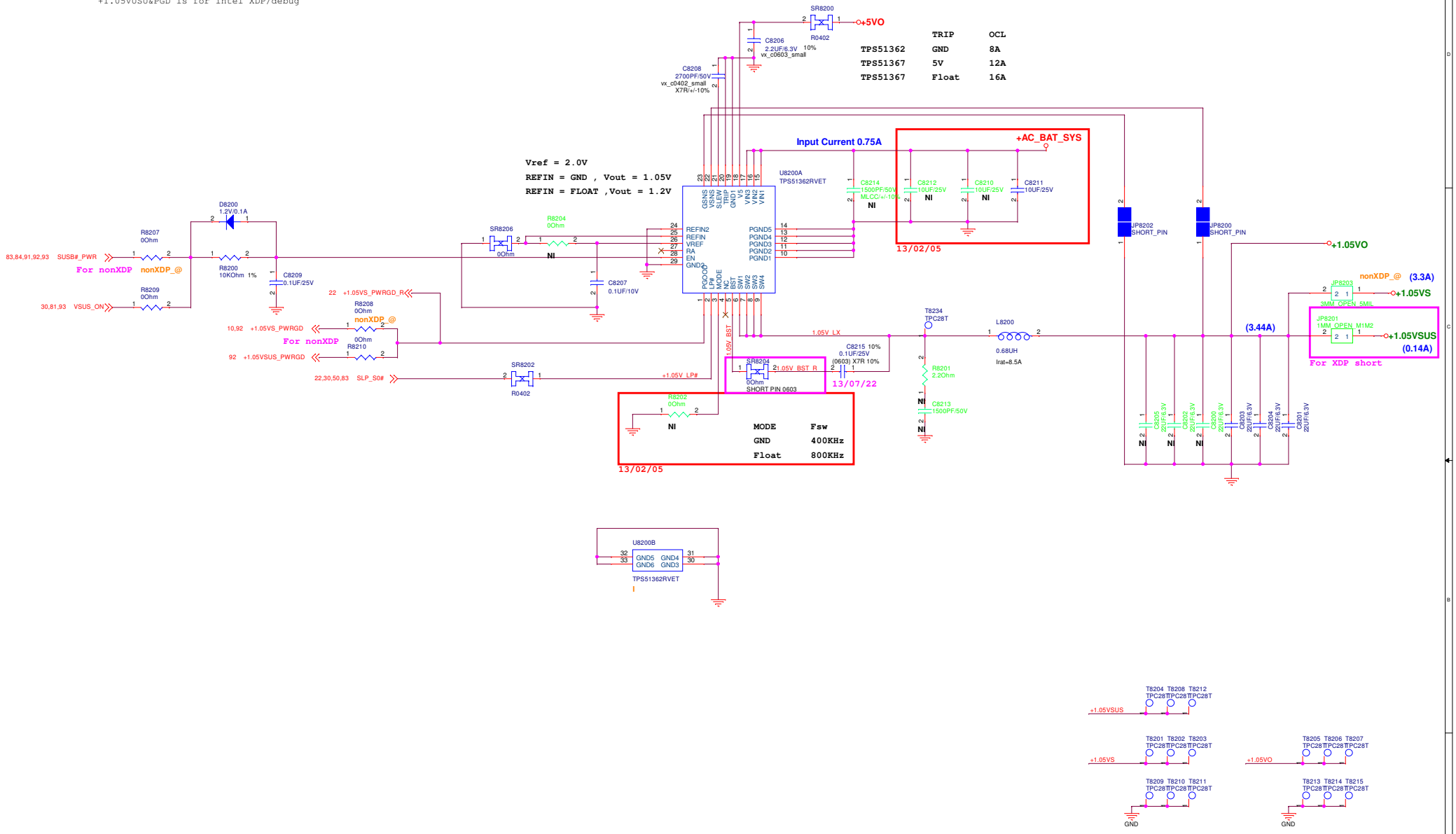
Engineer:

Size	Project Name	Rev
Custom	Junction	1.0

Date: Tuesday, September 24, 2013 Sheet 81 of 96

+1.05VS/+1.05VSUS POWER SUPPLY

8/7 +1.05VO enable from Susb change to Vsus_on;
+1.05VUSU&PGD is for intel XDP/debug



<Variant Name>

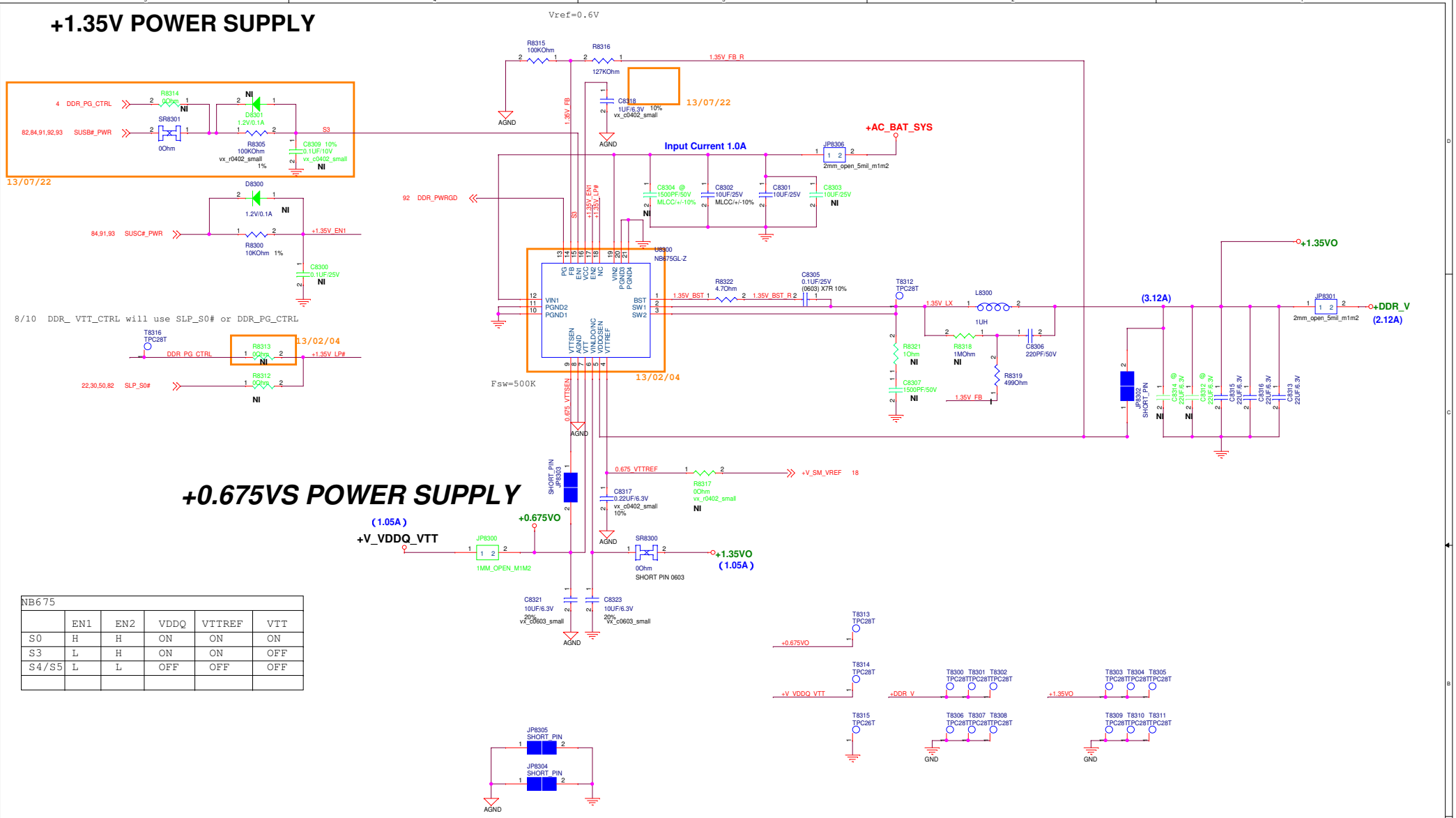
PEGATRON Title : POWER_+1.05VS

Engineer:

Size	Project Name	Rev
Custom	Junction	1.0

Date: Tuesday, September 24, 2013 Sheet 82 of 96

+1.35V POWER SUPPLY



+0.675VS POWER SUPPLY

NB675					
	EN1	EN2	VDDQ	VTTREF	VTT
S0	H	H	ON	ON	ON
S3	L	H	ON	ON	OFF
S4/S5	L	L	OFF	OFF	OFF

<Variant Name>

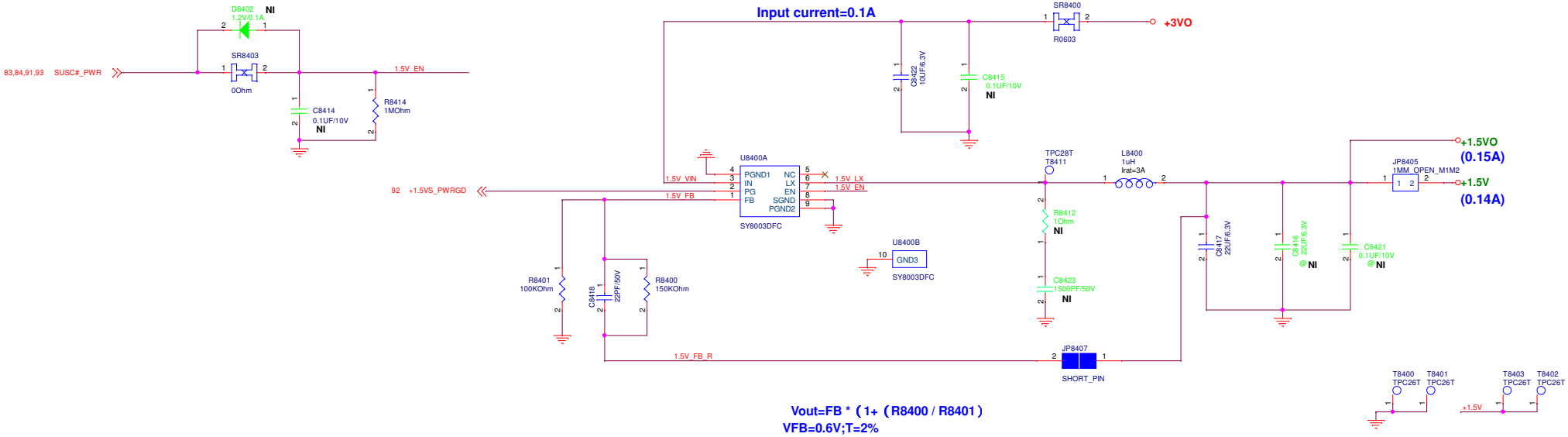
PEGATRON Title : POWER_DDR

Engineer:

Size	Project Name	Rev
C	Junction	1.0

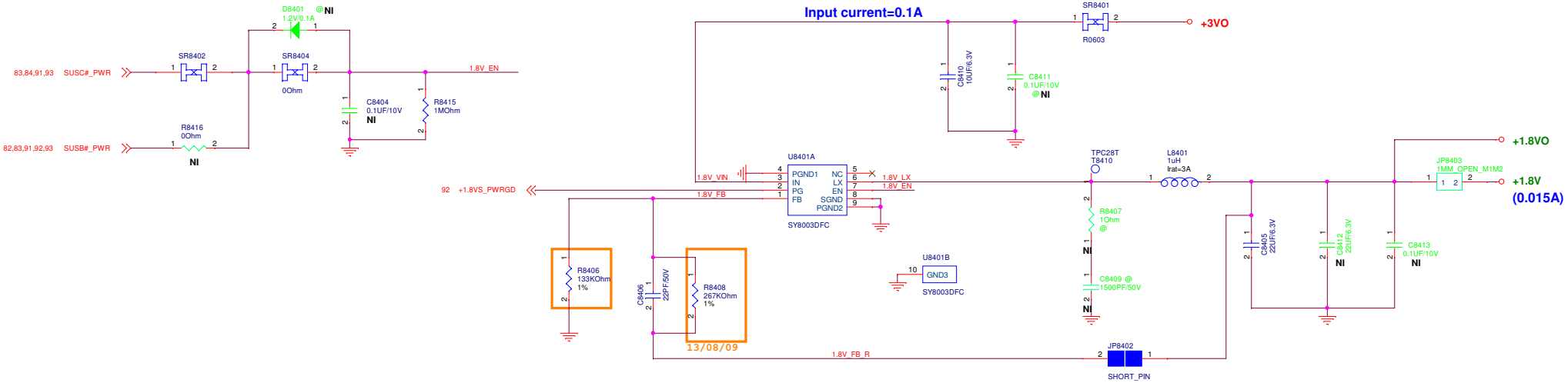
Date: Tuesday, September 24, 2013 Sheet 83 of 96

1.5V POWER SUPPLY



Vout=FB * (1+ (R8400 / R8401)
VFB=0.6V;T=2%

+1.8V POWER SUPPLY



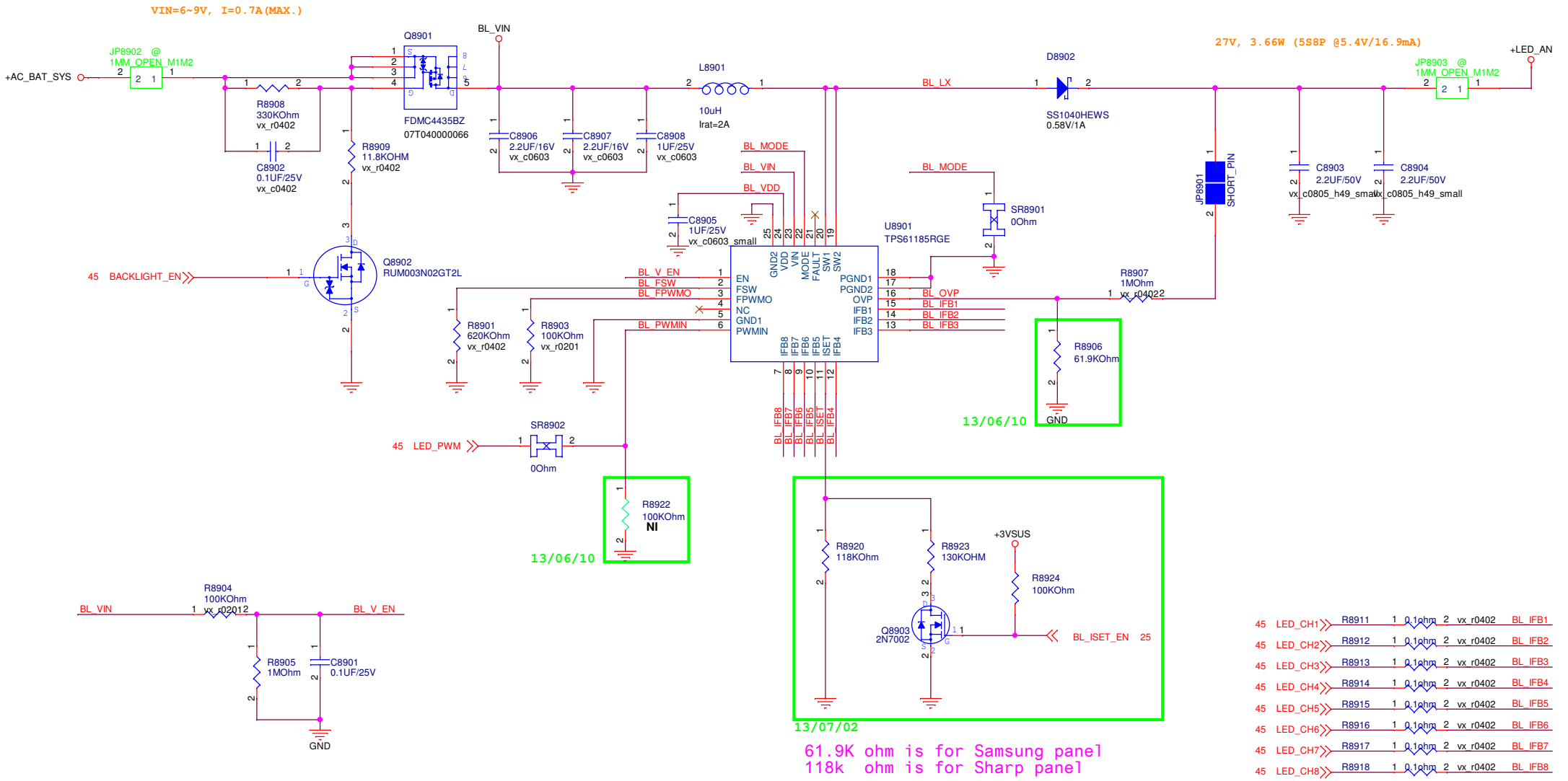
<Variant Name>

PEGATRON Title : POWER_1.8VS/+1.5V

Engineer:

Size	Project Name	Rev
Custom		1.0

Date: Tuesday, September 24, 2013 Sheet 84 of 96



MIDLAND

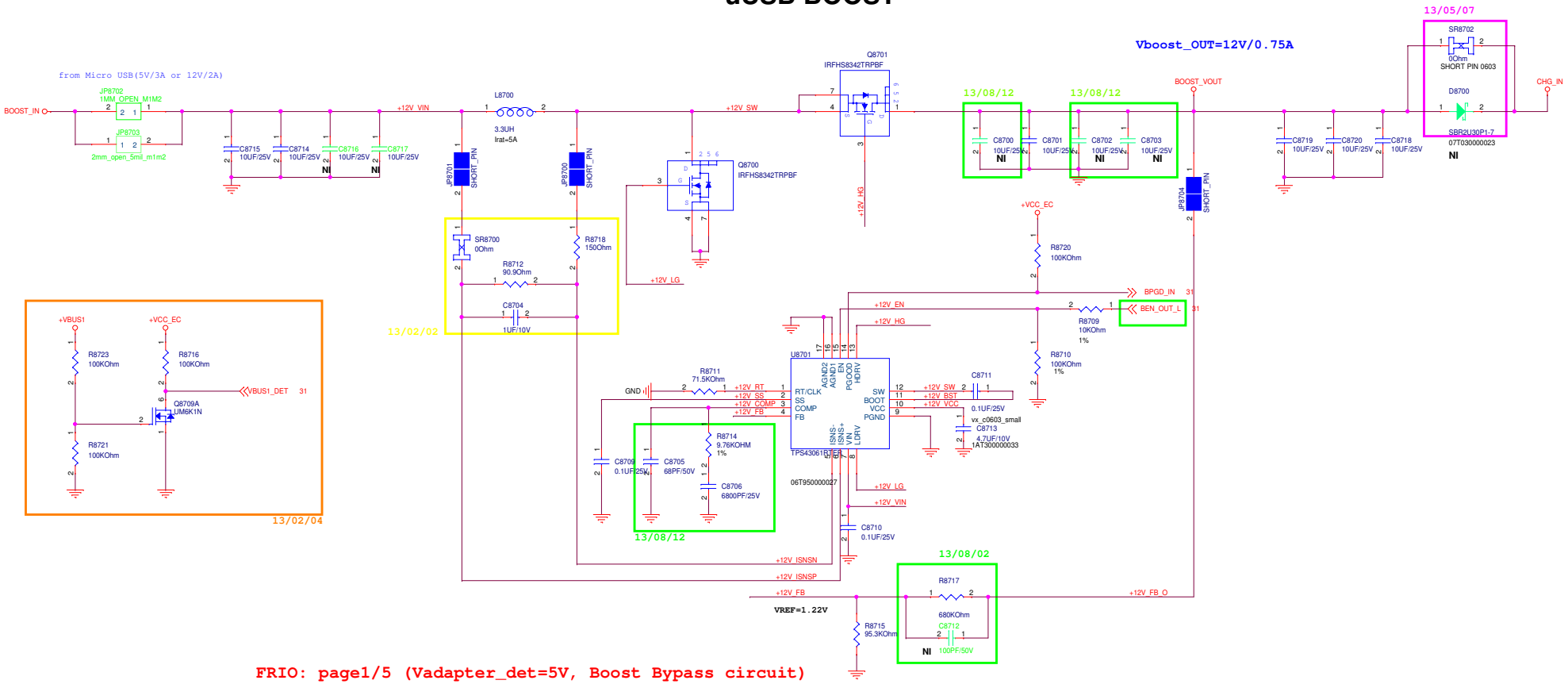
PEGATRON Title :POWER_N/A

Engineer:

Size	Project Name	Rev
B		R1.4

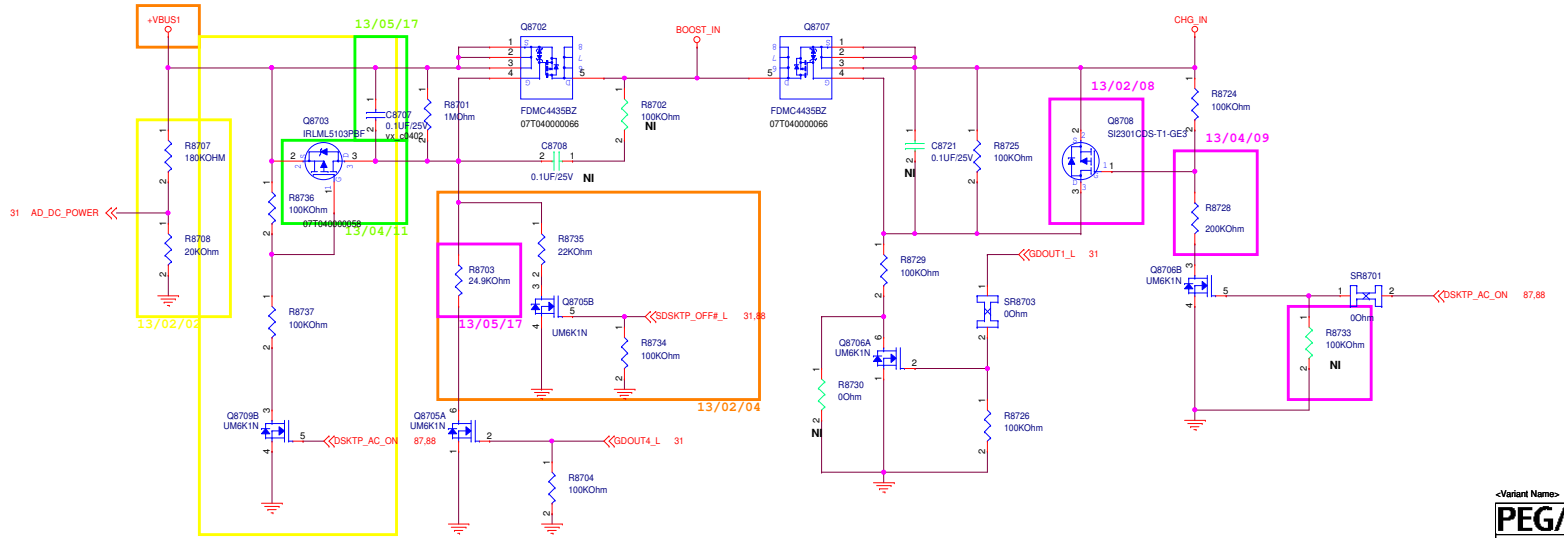
Date: Tuesday, September 24, 2013 Sheet 86 of 97

uUSB BOOST



FRIO: page1/5 (Vadapter_det=5V, Boost Bypass circuit)

S7 S8



<Variant Name>

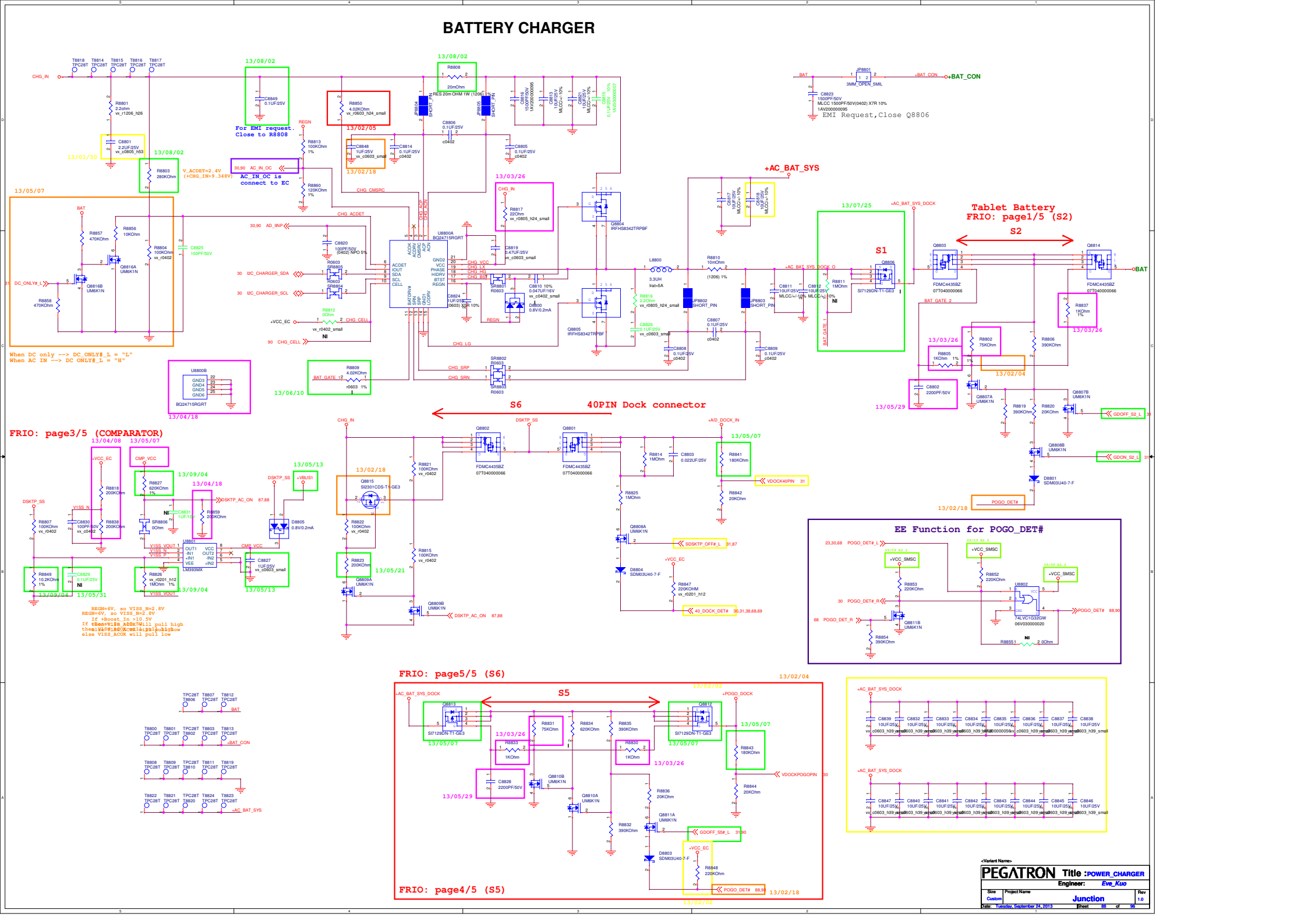
PEGATRON Title : +12VUSB

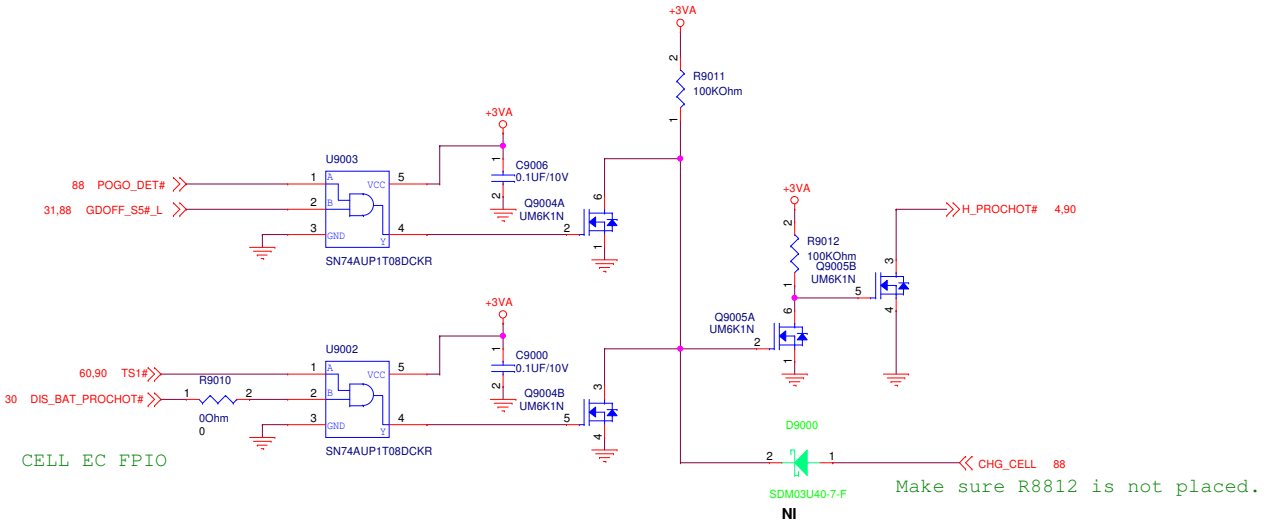
Engineer:

Size	Project Name	Rev
C		1.0

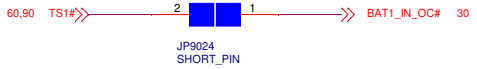
Date: Tuesday, September 24, 2013 Sheet 87 of 96

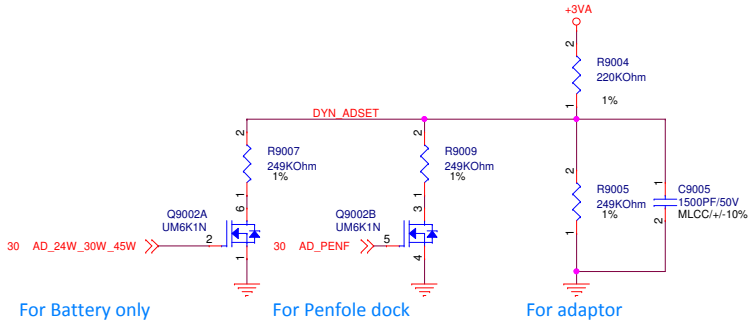
BATTERY CHARGER





BATTERY IN DETECT



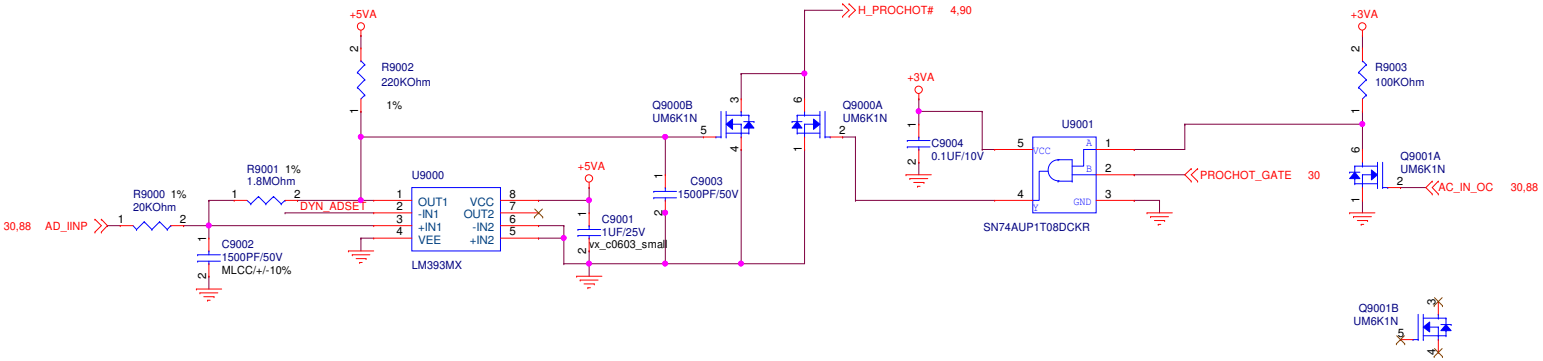


1. 24W dual voltage or 45W adapter:
   - o De-assert “AD_PENF”,
   - o De-assert “AD_24W_30W_45W”

   VIpeak-dual = 1.752V
   Ipeak-dual = 2.214A
2. AC via Penfolds dock:
   - o Assert “AD_PENF”
   - o De-assert “AD_24W_30W_45W”

   VIpeak-penfold = 1.193V
   Ipeak-penfold = 1.507A
3. Battery only: (Tablet or KBDock Battery.)
   - o De-assert “AD_PENF”
   - o Assert “AD_24W_30W_45W”

   VIpeak-battery = 1.193V
   Ipeak-dual = 7.537A



<Variant Name>

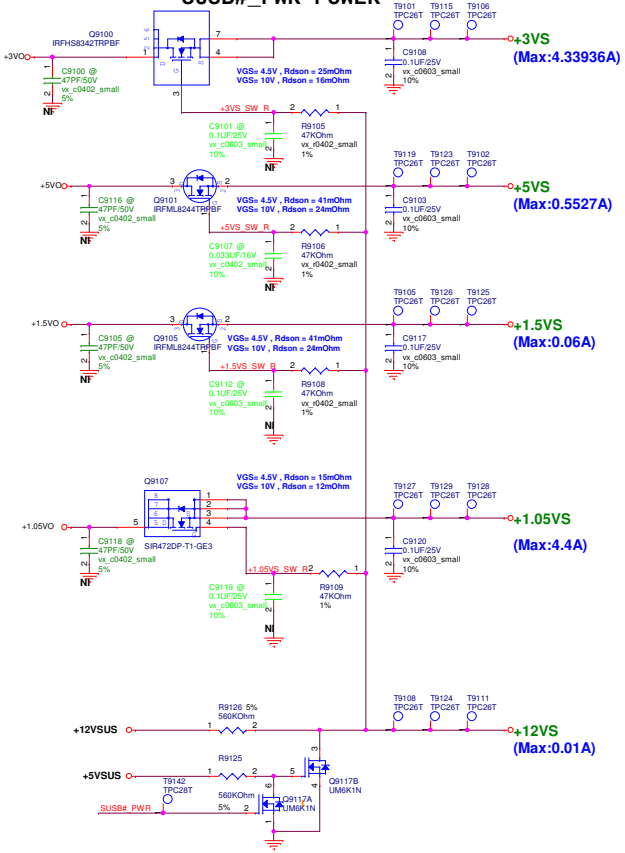
PEGATRON Title : POWER_DETECT

Engineer: Eve_Kuo

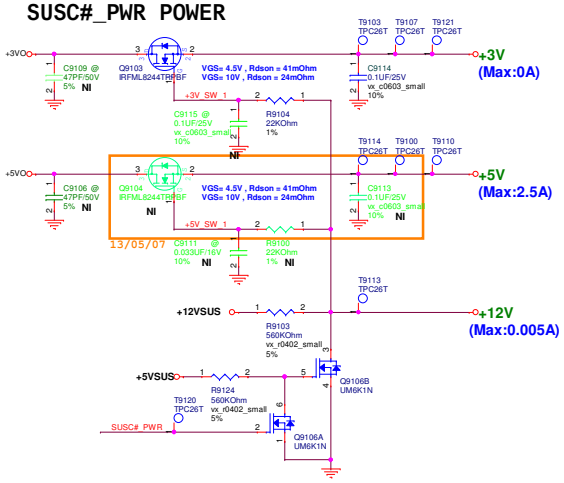
Size	Project Name	Rev
Custom	Junction	1.0

Date: Tuesday, September 24, 2013 Sheet 90 of 96

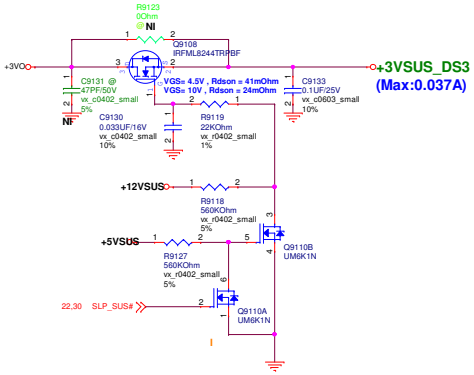
SUSB#_PWR POWER



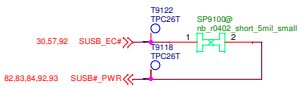
SUSC#_PWR POWER



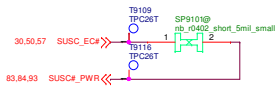
DS3 POWER



SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



<Variant Name>

PEGATRON Title : POWER_LOAD SWITCH

Engineer: Eve_Kuo

Size	Project Name	Rev
Custom	Junction	1.0

Date: Tuesday, September 24, 2013 Sheet 91 of 96

POWER GOOD DETECTER

Only for XDP

+3V
+1.05VS

R9208 100KOhm 1%
R9209 100KOhm 1%
R9210 100KOhm 1%
R9207 5% 560KOhm
C9201 0.047UF/16V X7R
Q9202 PMBS3904
Q9203 2N7002
GND

SUSB#_PWR 82,83,84,91,93
+1.05VS_PWRGD 10,82,92

+3VS
R9205 100KOhm 1%

T9203 TPC28T
84 +1.5VS_PWRGD
SR9204 R0402

T9202 TPC28T
83 DDR_PWRGD
SR9200 R0402

T9212 TPC28T
84 +1.8VS_PWRGD
SR9205 R0402

T9210 TPC28T
10,82,92 +1.05VS_PWRGD
For nonXDP
R9203 0Ohm
nonXDP_@

8/7
VR12.5:ALL_SYSTEM_PWRGD to EC,EC to PM_PWROK&delay 99ms ,EC enable CPU_VRON

VR12.6:ALL_SYSTEM_PWRGD to EC,EC to PM_PWROK&delay 99ms, EC enable DELAY_VR_AND_ALL_SYS

SR9203 R0402
T9200 TPC28T
ALL_SYSTEM_PWRGD 30
R9202 0Ohm
NI
PM_PWROK 22,30

+3VSUS
R9206 100KOhm 1%

T9206 TPC28T
30,81 SUS_PWRGD
SR9207 R0402
D9201 1.2V/0.1A

T9211 TPC28T
82 +1.05VSUS_PWRGD
R9211 0Ohm

For XDP

SR9206 R0402

T9201 TPC28T
30,57,91 SUSB_EC#
SUSB_EC#
D9200 1.2V/0.1A
R9201 560KOhm 5%
Q9200A UM6K1N
Q9200B UM6K1N
C9200 4.7UF/6.3V 10%
FORCE_OFF# 32,50
FORCE_OFF_PWR 81

+3VS
R9204 100KOhm 1%
T9208 TPC28T
6,30,80 VRM_PWRGD
Check with EE function&net name for C10/C9

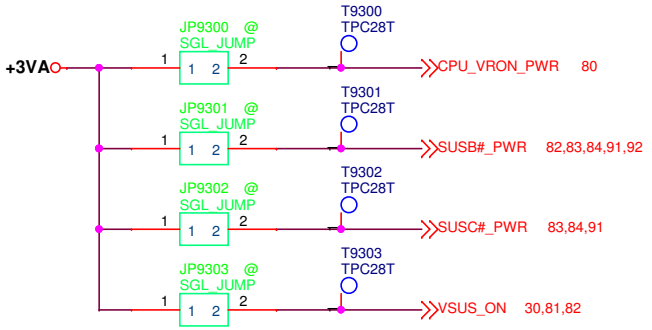
<Variant Name>

PEGATRON Title : POWER_PROTECT
Engineer:

Size	Project Name	Rev
Custom	Junction	1.0

Date: Tuesday, September 24, 2013 Sheet 92 of 96

FOR POWER TEST



+VCORE +VCORE 6,57,80

<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Eve_Kuo

Size	Project Name	Rev
Custom	Junction	1.0

Date: Tuesday, September 24, 2013 Sheet 93 of 96

modify notice

Version	Date	Description
	2012/10/22	禁用料修改 1.C8108,C8119 1AV600000003 ->1AV500000015 10UF/25V 0805 2.R8000,R8104,R8107,R8201,R8321,R8407,R8412 10V340000009=>10V340000005 1OHM 3.C8130,C8126,C8104,C8103,C8413,C8404,C8414,C8421,C8411,C8415 1AV200000045=> 1AV300000007 0.1UF/25V 0603 4.C8101,C8100 1AV300000016->1AV200000038 10UF/6.3V 0402 1.Add SR8002,JP8007,JP8108,JP8205,JP8306,SR8004S,R8401 Delete R8029,R8102,R8205,R8311,R8413,R8410 2.Add P8600
	2012/10/24	1.Delete JP8002 2.R8016 CHANGE TO 100KOHM 3.R8010 Change to 100ohm 4.R8009 Change to 100ohm 5.R8604 Change to 20Kohm 6.C8606 Change to 2200pF 7.Change page 80 GND_VCORE to GND
	2012/10/26	1.C8100,C8101 Change to 4.7uF/6.3V 2.C8208 CHANGE TO 2700PF/50V 3.C8306 CHANGE TO 330PF/50V 0402
	2012/10/26 19:00	1. Remove SR8301, and add R8322
	2012/10/31	1.C8306 CHANGE TO 220PF/50V 0402 2. 3.

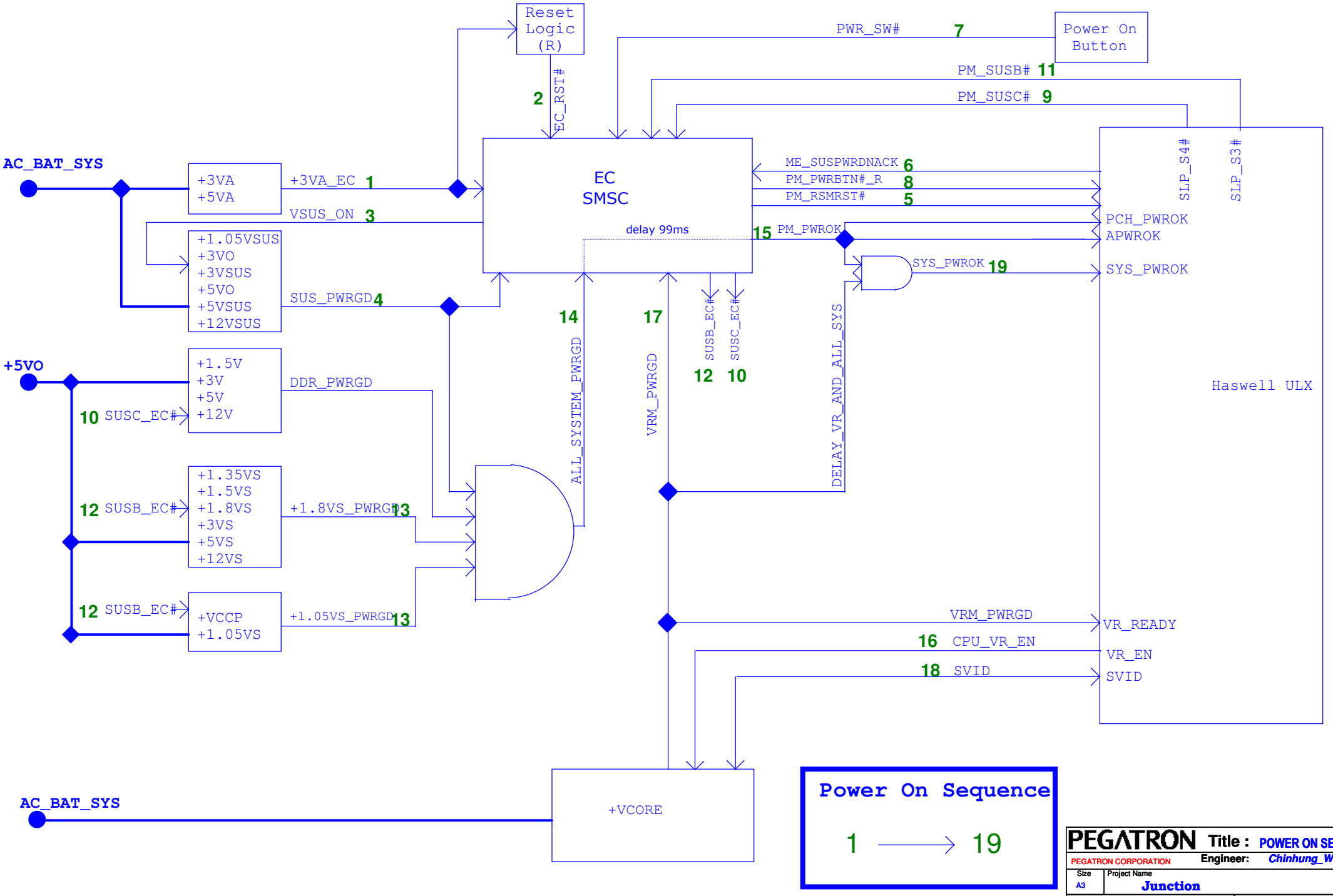
PEGATRON Title : Power History

PEGATRON CORPORATION Engineer: Eric_Kuo

Size: Custom | Project Name: Junction | Rev: 1A

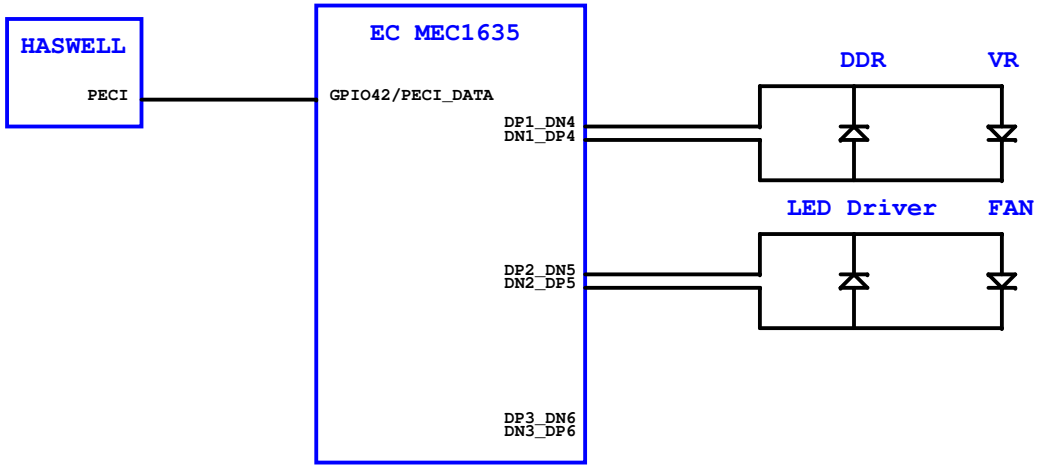
Date: Saturday, November 24, 2012 | Sheet 86 of 86

Power On Sequence Diagram G3-S0 (non Deep Sx Platform)



PEGATRON	Title : POWER ON SEQ	
PEGATRON CORPORATION	Engineer: Chinhung_Wang	
Size: A3	Project Name: Junction	Rev: 2.2
Date: Tuesday, September 24, 2013	Sheet 96 of 98	

THERMAL SENSE MAP



I2C_SMBus_Thermal Sense MAP

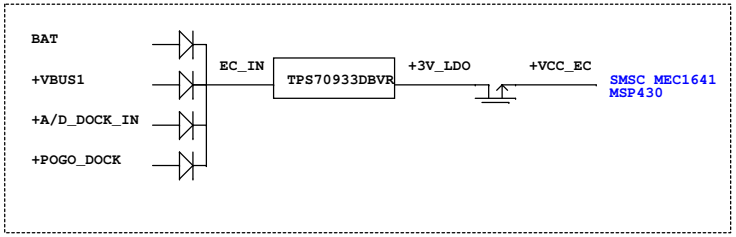
PEGATRON Title :

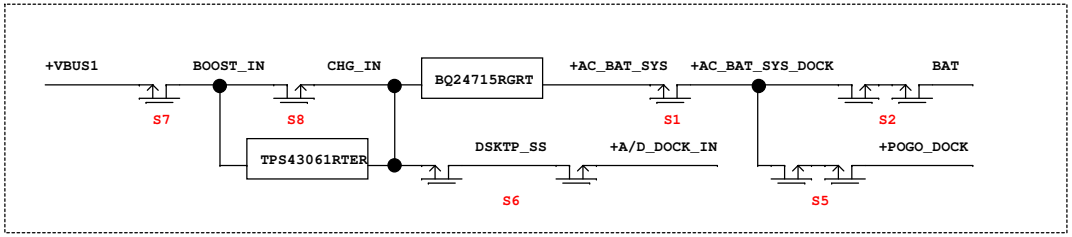
PEGATRON CORPORATION Engineer: Chinhung_Wang

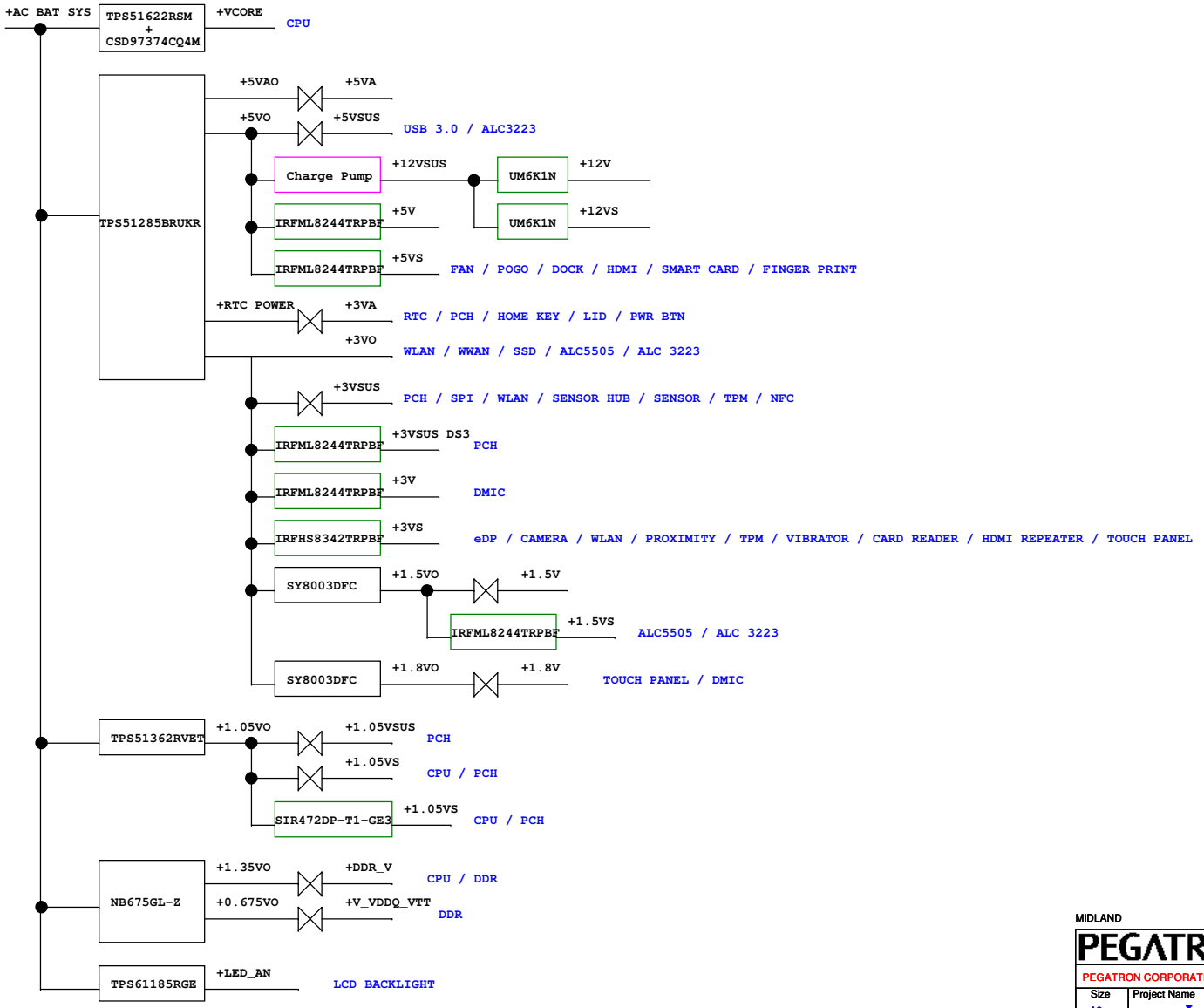
Size	Project Name	Rev
A3	Junction	2.2

Date: Tuesday, September 24, 2013 Sheet 97 of 98

FRIO SWITCH







MIDLAND

PEGATRON CORPORATION

Title : POWER TREE

Engineer: Chinhung_Wang

Size	Project Name	Rev
A3	Junction	2.2

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